3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.
4. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

Schematic / PCB #'s

<table>
<thead>
<tr>
<th>Schematic / PCB #s</th>
<th>Description</th>
<th>Reference</th>
<th>Critical</th>
<th>REV Option</th>
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<tr>
<td>SCHEM,MLB_LDO,K6</td>
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www.vinafix.vn
### BOM Variants

<table>
<thead>
<tr>
<th>BOM NUMBER</th>
<th>Alternate Parts</th>
<th>Module Parts</th>
<th>BOM Groups</th>
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<tbody>
<tr>
<td>516-0213</td>
<td>152S1135</td>
<td>337S3769</td>
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### Alternate Parts

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<th>BOM OPTION</th>
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</tbody>
</table>

### BOM Configuration

Apple Inc. 051-8563

### BOM Options

- **K6 Debug:** PROD
- **K6 Development:** PVT
- **K6 Engineering:** ENG
- **K6 Development:** DEVEL
- **K6 Prog Parts:** PROG

### BOM Groups

- **K6_Common**
- **K6 Misc**

### BOM Option

- **K6 MLB_LDO Development BOM**
  - PDC, SLGVT, PRQ, 2.26, 25W, 1066, R0, 3M, BGA, P7550
  - PDC, SLGLA, PRQ, 2.66, 25W, 1066, E0, 3M, BGA
  - PDC, SLGFG, PRQ, 2.53, 25W, 1066, R0, 3M, BGA
  - PCBA, MLB_LDO, BEST, K6
  - PDC, LGDZ, PRQ, 2.40, 25W, 1066, R0, 3M, BGA

- **IC, SMC, HS8/2117, 9X9MM, TLP, HF**
  - SMC External, K6

- **IC, CYPRUS, CY7C63803-LQXC, 4X4MM, USB, 24-QFN**
  - IC, PSOC+ W/ USB, 56 PIN, MLF, CY8C24794
  - IC, FLASH, SPI, 32MBIT, 3.3V, 86MHZ, 8-SOP

- **PDC, SLGVT, PRQ, 2.26, 25W, 1066, R0, 3M, BGA, P7550**
  - PDC, SLGLA, PRQ, 2.66, 25W, 1066, E0, 3M, BGA
  - PDC, SLGFG, PRQ, 2.53, 25W, 1066, R0, 3M, BGA
  - PCBA, MLB_LDO, BEST, K6

- **IC, TP PSOC, K17, K18**
  - IC, LP8545, LED BLKLT CTRLR, LLP24
  - IC, MCP89M-A01, 31X31MM, BGA1168
  - IC, 1MBIT, SPI FLASH, K17/18

- **EFI Unlocked, K6/K69**
  - EFI Unlocked, K6

### Alternate Parts

- SSM6P15FE As Alternate
- MOLEX As Alternate
- TOKO As Alternate
- INTEL P7550 CPU As Alternate
- DELTA As Alternate
- CYNTEC As Alternate
- CYNTEC As Alternate

### Table: BOM Groups

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<thead>
<tr>
<th>Reference Des</th>
<th>Description</th>
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</table>

### Diagram: K6 Board Stack-Up

**Top**
- SIGNAL
- GROUND
- SIGNAL (High Speed)
- POWER

**Middle**
- SIGNAL (High Speed)
- POWER
- GROUND

**Bottom**
- SIGNAL
CPU VCore HF and Bulk Decoupling
4x 330uF, 20x 22uF 0805

PLACEMENT NOTE (C1200-C1219):
CPU CAP:15&CPU CAP:12

1x 330uF, 6x 0.1uF 0402
VCCP (CPU I/O) DECOUPLING

1x 10uF, 1x 0.01uF
VCCA (CPU AVdd) DECOUPLING

PLACEMENT NOTE (C1240-C1243):
Place inside socket cavity on secondary side.

Place on secondary side.
Place on secondary side.
Place on secondary side.

PLACEMENT_NOTE (C1200-C1219):
4X 330UF. 20X 22UF 0805

PLACEMENT NOTE (C1240-C1243):
Place inside socket cavity on secondary side.

CPU Decoupling
Apple Inc.
www.vinafix.vn
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

The use of this adapter board to support CPU, MCP debugging.

MCP89-specific pinout

Direction of XHP module

on even-numbered side of J1300

Please avoid any obstructions
Current numbers from MCP89 A01 Bring-up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

PE ports are rms-capable. 1 RCs: x, x, x, x, x
PE ports are dm-only. 1 RCs: x, x

If PE[4:5] and PE1[0:1] are not used, +VIO_PE_AVDD0 and +VIO_PE_DVDD0 can be GND
If PE[3:0] are not used, +VIO_PE_AVDD0 and +VIO_PE_DVDD0 can be GND

Place near = U1400.U2: 12.7 mm
No stuffing

Apple Inc.

MCP PCIe Interfaces

Current numbers from MCP89 A01 Bring-up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). 4 OF 11

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DDC Mode Pull-downs

NOTE: 10k pull-downs required if DDC_DATA/DP_AUX_CH1 are used for DDC. If unused no pulls are necessary, if used for TMDS/HDMI only then only pull-ups are necessary.

GPIO Pull-Ups
Current numbers from MCP89 A01 Bring-up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

**Component Details:**

- **Current Numbers:**
  - PP3V3_ENET_MCP_RMGT
  - MF-LF 1/16W 5%
  - MF-LF 1/16W 402 5%
  - MF-LF 1/16W 8.2K

- **Pin Assignments:**
  - **MCP MII COMP GND**
  - **MCP MII COMP VDD**
  - **ENET_ENERGY_DET**
  - **ENET_RX_CTRL**
  - **ENET_RXD<0>**
  - **ENET_RXD<1>**
  - **ENET_RXD<2>**

- **Connect Instructions:**
  - Connect **RGMII_VREF** to 10K pull-down.
  - Connect **RGMII_COMP_VDD/_GND** must remain connected as shown.
  - Connect **RGMII_INTR** to 10K pull-down (if not used as GPIO).
  - Connect **RGMII_RXD<0:3>** together to 10K pull-down.
  - **Internal MAC Disable:**
    - Connect **RGMII_COMP_GND**
    - Connect **RGMII_COMP_VDD**
    - Connect **RGMII_INTR/GPIO_35**
    - Connect **RGMII_RXCTL**
    - Connect **RGMII_RXD2**
    - Connect **RGMII_RXD1**
    - Connect **RGMII_RXD0**

- **Other Pins:**
  - All other pins can be left TP or NC.

- **USB Ports:**
  - Only **USB8-11** support nV
  - **USB_OC2*/GPIO_27_MGPIO_0**
  - **USB_OC0*/GPIO_25**

- **Internal Pull-Downs:**
  - Internal 19.5K Pull-Downs on all USB pairs

- **FPCs:**
  - **BUF_25MHZ**
  - **OHCI1/EHCI1**

- **Other Connects:**
  - **USB_BT_N**
  - **USB_IR_P**
  - **USB_EXTB_N**
  - **USB_EXTB_P**
  - **USB_TPAD_N**
  - **USB_TPAD_P**
  - **USB_EXTD_N**
  - **USB_EXTD_P**
  - **USB_SDCARD_N**
  - **USB_SDCARD_P**
  - **USB_CAMERA_N**
  - **USB_CAMERA_P**
  - **USB_WM_P**
  - **USB_WM_N**
  - **USB_EXTC_P**
  - **USB_EXTC_N**

- **BI Connects:**
  - **BI**
  - **BI**
  - **BI**
  - **BI**
  - **BI**
  - **BI**
  - **BI**

- **Other Connects:**
  - **NC_USB_T57_P**
  - **NC_USB_T57_N**
  - **USB_MINI_P**
  - **USB_MINI_N**
  - **USB_EXTA_P**
  - **USB_EXTA_N**

- **MCP SATA, USB & Ethernet:**
  - **MCP SATA,**
  - **USB,**
  - **Ethernet**
  - **Apple Inc.**
  - **A13.0**

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- **Sync Date:**
  - 11/23/2009

- **Branch:**
  - 17 OF 80

- **Page Title:**
  - MCP SATA, USB & Ethernet

- **Page:**
  - 8
NOTE: "SW" rails are dynamically switched in the S0 state as needed, controlled by MCP89 GPIOs.

200 mA

NOTE: VDD_COREx_SENSE signals should NOT be used for remote sensing unless they are powered by separate regulators. Use VDD_COREx_SENSE as close to CORE A/B as possible.

MCP Power & Ground

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Q2300 helps reduce input rail drop during Q2300 turn-on.

---

**DIMM CKE Clamps**

cke must be held low to keep memory in self-refresh.

Clamps enable during MCP89 MEMVDD rail switched off.

Clamps release after MCP89 MEMVDD is up and CKEs are driven by MCP89.

Clamps enable before MCP89 MEMVDD rail switched off.

NO STUBS on CKE signals!

---

Approx. Ramp Time (EN to 1.35V, us): 7.91 + 0.0678 * R1(Kohms)

Gated Rail Savings: 0.10MW

NOTE: nVidia recommends Infineon BSC030N03MS for Q2300.

- Min Ramp-Up Time: 20 us (10% to 90%)
  - Max Ramp-Up Time: 65 us (10% to 90%)
  - FET Ron <= 3.8 mOhms

C2300 helps reduce input rail droop during Q2300 turn-on.
C2400 helps reduce input rail drop during Q2400 turn-on.

Approx. Ramp Time (EN to 1V, uS): 43.9 + 0.6943 * C1(pF)

Max Ramp-Up Time: 1500 uS (ENABLE to 90%)
Min Ramp-Up Time: 100 uS (10% to 90%)
FET Ron <= 2.5 mOhms
Gated Rail Savings: 860mW

NOTE: nVidia recommends Infineon BSC020N03MS for Q2400.

C2405 helps reduce input rail drop during Q2400 turn-on.

C2406 helps reduce input rail drop during Q2400 turn-on.

C2407 helps reduce input rail drop during Q2400 turn-on.

NOTE: nVidia recommends equip BSC020N03MS for Q2400.

Gated Rail Savings: 860mW

- If RGBDAC is used, requires ferrite (155S0382) plus 1x 4.7uF 0603 & 1x 0.1uF 0402 cap.
- If RGBDAC is not used, tie to GND.


- If RGBDAC is used, requires ferrite (155S0382) plus 1x 4.7uF 0603 & 1x 0.1uF 0402 cap.
- If RGBDAC is not used, tie to GND.


- If RGBDAC is used, requires ferrite (155S0382) plus 1x 4.7uF 0603 & 1x 0.1uF 0402 cap.
- If RGBDAC is not used, tie to GND.
**FireWire Port Power Switch**

- **FW_PWR_EN**
- **FW_PWR_EN_L**
- **FW_PWR_EN_R**
- **FW_PWR_EN_D**
- **FW_PWR_EN_F**

**Power aliases required by this page:**
- =FW_PWR_EN
- =FW_PWR_EN_L
- =FW_PWR_EN_R
- =FW_PWR_EN_D
- =FW_PWR_EN_F

**Signal aliases required by this page:**
- =PP1V0_FW_FET_R (1.0V FET Output)
- =PP1V05_S0_FWPWRCTL (5KPD Bias Rail)
- =PP3V3_S0_FWPWRCTL
- =PP3V3_S0_FWLATEVG
- =PP3V3_FW_FWPHY (PHY 3.3V Power)
- =PP3V3_FW_FET (3.3V FET Output)
- =PP3V3_FW_P3V3FWFET (3.3V FET Input)
- =PPBUS_FW_FET (FW VP FET Output)
- =PPBUS_S5_FWPWRSW (FW VP FET Input)

**Page Notes**

1. **FireWire PHY WAKE# Support**
   - When PHY is powered, **FW_PWR_EN** acts as legacy PME signal.
   - Dual-purpose output:
     - 1) Do pull-down detect when **FW_PWR_EN** is low.
     - 2) Pull-up provided on another page.

2. **FireWire Port 5K Pull-Down Detect**
   - All Firewire devices require pull-down on TPBIAS signal.
   - Must detect as load on TPBIAS signal.
   - Current source only active when **FW_PWR_EN** is low.

3. **Supervisor & CLKREQ# Isolation**
   - Pull-up provided on another page.
ODD Power Control

SATA ODD Port

PS8511A / PS8515A Straps

SATA Redriver

SATA HDD Port

U4510 ADD NO STUFF IN PRODUCTION!!!!

J5401 PINS ARE DIFFERENT FOR R4, DO NOT SYNC THIS PAGE FROM T27 DIRECTLY
IR Support

T57 Connector

**NOTES:**
- D4890 CONNECTION IS DIFFERENT, CANNOT DIRECTLY SYNC FROM T27
unsed pins have "SMC_PECI" names. Unsued pins designed as outputs can be left floating, those designated as inputs require pull-ups.

SMC PB3, SMC ADC15, SMC NB_DDR_ISENSE, SMC NB_CORE_ISENSE, SMC_ANALOG_ID, SMS_Y_AXIS, SMC FAN_3_TACH, SMC FAN_2_TACH, SMC FAN_0_TACH, SMC FAN_3_CTL, SMC FAN_2_CTL, SMC_RUNTIME_SCI_L, PM_BATLOW_L, MEM_EVENT_L, USB_DEBUGPRT_EN_L, SMB_0_S0_CLK, SMC_SYS_KBDLED, SMC_GFX_THROTTLE_L, SMB_MGMT_DATA, LPC_SERIRQ, LPC_CLK33M_SMC, LPC_FRAME_L, LPC_AD<2>, SMC_RSTGATE_L, SMC THRMTRIP, SMB_B_S0_CLK, SMB_BSA_CLK, SMB_BSA_DATA, SMC LID, SMC TMS, SMC_TCK, SMC_BC_ACOK, SMC_ONOFF_L, SMC_RX_L, PM_CLKRUN_L, SMC_BATT_ISENSE, SMC_PBUS_VSENSE, SMC_GPU_ISENSE, SMC_CPU_VSENSE, SMC_CPU_ISENSE, SMC_PROCHOT_3_3_L, SMC_ADAPTER_EN, SMC_PH3, SMC PECI_VSTP, SMC PECI, H8S2117-R.

If SMS interrupt is not used, pull up to SMC rail.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.

NOTE: P94 and P95 are shorted in some platforms.

NOTE: SMS interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.

SMC VCL

Apple Inc.

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CPU Voltage Sense / Filter

MCP Voltage Sense / Filter

PBUS Voltage Sense Enable & Filter

ENABLING PBUS VSENSE divider when high.

Place RC close to SMC.
CPU T-Diode Thermal Sensor

- **CPU THERM P**: Terminal for CPU thermal diode
- **CPU THERM N**: Terminal for CPU thermal diode
- **FIN-STACK TEMPERATURE**: Terminal for fin-stack temperature
- **C5520**: Capacitor 0.0022uF CERM 402
- **C5521**: Capacitor 0.0022uF CERM 402
- **Q5501**: Power transistor CRITICAL BC846BMXXH SOT732-3
- **R5515**: Resistor 1/16W 5% MF-LF 402 47
- **R5517**: Resistor 1/16W 5% MF-LF 402 47
- **R5516**: Resistor 1/16W 5% MF-LF 402 47
- **R5535**: Resistor 1/16W 5% MF-LF 402 47
- **R5536**: Resistor 1/16W 5% MF-LF 402 47
- **U5515**: Integrated circuit EMC1413
- **U5535**: Integrated circuit EMC1412-A
- **C5522**: Capacitor 0.0022uF CERM 402
- **C5523**: Capacitor 0.0022uF CERM 402
- **C5524**: Capacitor 0.0022uF CERM 402
- **C5525**: Capacitor 0.0022uF CERM 402
- **C5526**: Capacitor 0.0022uF CERM 402
- **C5527**: Capacitor 0.0022uF CERM 402
- **C5535**: Capacitor 0.1uF CERM 402
- **Placements**:
  - Place Q5501 near fin stack
  - Place U5515 near CPU
  - Place U5535 near MCP

MCP T-Diode Thermal Sensor

- **MCP THERM P**: Terminal for MCP thermal diode
- **MCP THERM N**: Terminal for MCP thermal diode
- **MCP THERMD P**: Terminal for MCP thermal diode
- **MCP THERMD N**: Terminal for MCP thermal diode
- **MCPTHMSNS THERM L**: Terminal for MCP thermal diode
- **CPUTHMSNS ALERT_L**: Terminal for CPU thermal diode
- **CPUTHMSNS_D2_N**: Terminal for CPU thermal diode
- **CPUTHMSNS_D2_P**: Terminal for CPU thermal diode

Thermal Sensors

- **Apple Inc.**
- **Notices**:
  - Notice of Proprietary Property
  - Notice of Conformity
  - Notice of Export Compliance

**Revision** A.13.0
**Draw Date** 08/27/2009
**Sheet** 3
**Branch** 87
**Revision** D
**Size** 54 x 54
**Drawing Number** 42 x 42

www.vinafix.vn
### SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.

Keys paired with PDPD power to isolate when PDPD is not powered.

Left shift, option & control keys combined with power button cause SMC RESET# assertion.

Keys paired with PDPD power to isolate when PDPD is not powered.
BOoster +18.5vDC FOR Sensors

If HIGH, keyboard backlight not present
If LOW, keyboard backlight present

- StartUp Time less than 2ms
- Power Consumption
  - Booster +18.5VDC for Sensors

- Min Line Width = 0.50MM
- Voltage = 5V

Keyboard Backlight Driver & Detection

To detect keyboard backlight, SMC will
tristate and read SMC.PPD1.KBDLED.
If LOW, keyboard backlight present.
If HIGH, keyboard backlight not present.
RS815 always stuck, Stick only
 grounded when EN KBD flex connected.

Keyboard Backlight Connector

SMC.PPD1.KBDLED is grounded
on keyboard backlight flex

PP3V3.S3.TPAD

PSOC.SCLK

Z2_HOST_INTN

Z2_SCLK

Z2_DEBUG3

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MCP89 SPI Frequency Select:

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<thead>
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<th>Frequency</th>
<th>SPI_MOSI</th>
<th>SPI_CLK</th>
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<tbody>
<tr>
<td>25.0 MHz</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>31.2 MHz</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>41.7 MHz</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>62.5 MHz</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Note: 42 & 62 MHz use FAST_READ command.

NOTE:If HOLD* is asserted
ROM will ignore SPI cycles.

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LINE INPUT VOLTAGE DIVIDER

CODEC VIN = 2VRMS
GND RIN = 10.36K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)
FC HP = 3.6 HZ
FC LP = 43KHZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS
MagSafe DC Power Jack

10. Supply needs to guarantee 3.31V delivered to SMC VRef generator

BATTERY CONNECTOR

3.425V "G3Hot" Supply

DC-In & Battery Connectors

www.vinafix.vn
Input impedance of ~40K meets ACIN pin threshold is 3.2V, +/- 50mV.
1.2V ENET Switcher

Vout = 1.2V
Max Current = 0.7A
F = 1.7MHz

1.5V S0 Regulator

Vout = 0.8V * (1 + Ra / Rb)

1.8V S0 Switcher

Vout = 0.8V * (1 + Ra / Rb)

BCM57765 Internal Switcher Support

(Max may be required to use BCM57765)

1.05V S0 MCP PLL LDO

Vout = 0.8V * (1 + Ra / Rb)

Vout = 1.508V
Max Current = 1.5A
F = 1.6MHz

MCP 0.9V S5 (AUXC) Switcher

Vout = 0.902V
Max Current = 1.5A
F = 1.6MHz

Misc Power Supplies

Apple Inc.

www.vinafix.vn
Power FETs

Apple Inc. 051-8563 2
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Loading
ID(max)
Rds(on)
Type
MOSFET

3.3V S0 FET

Q7910
Type: P-Channel
Max(V(DS)) 3.3V
Min(I(DS)) 1.0 A

3.3V S3 FET

Q7940
Type: N-Channel
Max(V(DS)) 4.5V
Min(I(DS)) 0.5 A

5V S0 FET

Q7900
Type: P-Channel
Max(V(DS)) 5.0V
Min(I(DS)) 0.5 A

3.3V ENET Switch

U7980
Type: Load Switch
Max(V(OUT)) 3.3V

0.9V ENET FET

Q7990
Type: N-Channel
Max(V(DS)) 2.5V
Min(I(DS)) 0.2 A
FOUR GROUND VIAS SHOULD BE DISTRIBUTED ALONG THE GROUND SHAPE THAT BOUND THE CONNECTOR BODY.
P-TYPE 43 mOhm @4.5V MOSFET CHANNEL RDS(ON) LOADING LOAD FDC638APZ PPBUS S0 LCDBkLT FET 0.65 A (EDP) F9800 2AMP-32V 0402-HF R9808 402 MF-LF 1/16W 1% 301K R9809 402 MF-LF 1/16W 1% 147K C9802 0.1UF 402 X5R 16V 10% SSOT6-HF Q9806 FDC638APZ_SBMS001 CRITICAL 24 LCD Backlight Support LCD_BKLT_EN=PPBUS_S0_LCDBKLT BKLT_PLT_RST_L LCDBKLT_EN_DIV LCDBKLT_DISABLE LCDBKLT_EN_L LCD_BACKLIGHT_PROGRAMMING VOLTAGE=12.6V MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.25 mm PPBUS_S0_LCDBKLT_FUSED PPBUS_SW_LCDBKLT_PWR VOLTAGE=12.6V MIN_NECK_WIDTH=0.25 mm MIN_LINE_WIDTH=0.4 mm
### FSB (Front-Side Bus) Constraints

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<td>FSB_DSTB2_50S</td>
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<td>FSB_ADDR_GROUP3</td>
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<td>FSB_DATA</td>
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<td>FSB_DSTB</td>
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### CPU Signal Constraints

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<td>FSB_DRDY_L</td>
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<td>FSB_DEFER_L</td>
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<td>FSB_DBSY_L</td>
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<tr>
<td>FSB_DINV_L&lt;2&gt;</td>
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<tr>
<td>FSB_DATA_L&lt;47..32&gt;</td>
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<td>FSB_DINV_L&lt;1&gt;</td>
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### MCP FSB COMP Signal Constraints

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<td>CPU_VCCSENSE_P</td>
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<td>CPU_VCCSENSE</td>
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### FSB Clock Constraints

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<td>FSB_CLK_ITP_P</td>
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<td>FSB_CLK_CPU_P</td>
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### CPU / FSB Net Properties

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<tr>
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<td>FSB_DSTB1</td>
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<tr>
<td>FSB_DSTB2</td>
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<tr>
<td>FSB_DSTB_50S</td>
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<td>FSB_DSTB0_50S</td>
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</tr>
<tr>
<td>FSB_DSTB1_50S</td>
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<tr>
<td>FSB_DSTB2_50S</td>
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<tr>
<td>FSB_DATA_GROUP0</td>
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<td>FSB_DATA_GROUP1</td>
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<tr>
<td>FSB_DATA_GROUP2</td>
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<tr>
<td>FSB_DATA_GROUP3</td>
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<td>FSB_DATA</td>
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</tr>
<tr>
<td>FSB_DSTB</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

### Notes

- Intel recommends routing only on internal layers for differential pairs with a maximum spacing of 5 mils.
- The recommended spacing for the VCC sense pair is 7 mils, which should be kept consistent with the 7 mil spacing Intel recommends.
- Additional guidance for routing FSB signals can be found in the Santa Rosa Platform DG, Rev. 1.5 (#22294), Sections 4.2 & 4.3.
**Memory Bus Constraints**

<table>
<thead>
<tr>
<th>Source: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.2</th>
</tr>
</thead>
</table>

**Memory Net Properties**

<table>
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**Memory Bus Spacing Group Assignments**

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**MCP MEM COMP Signal Constraints**

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<th>Source: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.2</th>
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### MCP89 Net Properties

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<th>Signal 3</th>
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</tbody>
</table>

### Analog Video Signal Constraints

- LVDS intra-pair matching should be 5 mils. Pairs should be matched within 100 mils.

### Digital Video Signal Constraints

- LVDS intra-pair matching should be 5 mils. Pairs should be matched within 100 mils.
- CLK_PCIE should be matched as close as possible and within 100 mils.

### SATA Interface Constraints

- SATA intra-pair matching should be 5 mils.
- Max trace length: 12 inches for SATA Gen3/Gen2.

Source: MCP89 Interface DO (MN-00645-001_v3.9), Section 2.4

**NEED PCIe Gen1/Gen2 notes!**
### LPC Bus Constraints

<table>
<thead>
<tr>
<th>Constraint Code</th>
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<td>1.5x_DIELECTRIC</td>
<td>90_OHM_DIFF</td>
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### USB 2.0 Interface Constraints

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### SMBus Interface Constraints

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### HD Audio Interface Constraints

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### SIO Signal Constraints

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<td>90_OHM_DIFF</td>
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### SPI Interface Constraints

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**Source:** MCP89 Interface DG (DG-04625-001_v0.9), Section 2.12
**SD Card Interface Constraints**

**RGMII (Ethernet) Constraints**

**SD Card Net Properties**

**Ethernet Net Properties**

**SD Card Interface Constraints**

**RGMII Net Properties**

**SOURCE:** MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

**PHYSICAL RULE SET**

**SPACING RULE SET**

**B**

**C**

**D**

**A**

---

**NOTE:** SD_D<7..5> are different to support BCM5764M/BCM57765 co-layout.

---

**SYNC_DATE=11/23/2009**

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**SYNC_MASTER=T27_MLB**

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**THE POSESSOR AGREES TO THE FOLLOWING:**

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**Apple Computer, Inc.**

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### SMBus Net Properties

<table>
<thead>
<tr>
<th>NET_TYPE</th>
<th>SPACING</th>
<th>TABLE_PHYSICAL_RULE_ITEM</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMBUS_SMC_0_S0_SCL</td>
<td>0.1 MM</td>
<td></td>
</tr>
<tr>
<td>SMBUS_SMC_B_S0_SCL</td>
<td>0.1 MM</td>
<td></td>
</tr>
<tr>
<td>SMBUS_SMC_A_S3_SCL</td>
<td>0.1 MM</td>
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### SMBus Charger Net Properties

<table>
<thead>
<tr>
<th>NET_TYPE</th>
<th>SPACING</th>
<th>TABLE_PHYSICAL_RULE_ITEM</th>
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</thead>
<tbody>
<tr>
<td>CHGR_CSI_P</td>
<td>0.1 MM</td>
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<tr>
<td>CHGR_CSI_N</td>
<td>0.1 MM</td>
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</tr>
<tr>
<td>CHGR_CSI_R_N</td>
<td>0.1 MM</td>
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</tr>
</tbody>
</table>

### SMC Constraints

- **SYNC_MASTER**: T27_MLB
- **SYNC_DATE**: 07/28/2009
- **NET_TYPE**: 1TO1_DIFFPAIR
- **SPACING**: 0.1 MM
### MCP Fanout Constraint Relaxations

#### SPACING_RULE_SET

<table>
<thead>
<tr>
<th>NET_SPACING_TYPE1</th>
<th>NET_SPACING_TYPE2</th>
</tr>
</thead>
<tbody>
<tr>
<td>OVERRIDE</td>
<td>OVERRIDE</td>
</tr>
<tr>
<td>OVERRIDE</td>
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<td>OVERRIDE</td>
<td>OVERRIDE</td>
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</tbody>
</table>

#### Power Net Properties

<table>
<thead>
<tr>
<th>AREA_TYPE</th>
<th>SPACING_RULE_SET</th>
</tr>
</thead>
<tbody>
<tr>
<td>SB_POWER</td>
<td>DP_90D</td>
</tr>
<tr>
<td>SB_POWER</td>
<td>LVDS_100D</td>
</tr>
<tr>
<td>GND_P2MM</td>
<td>GND_P2MM</td>
</tr>
<tr>
<td>GND_P2MM</td>
<td>CPU_VCCSENSE</td>
</tr>
<tr>
<td>GND_P2MM</td>
<td>CPU_GTLREF</td>
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<tr>
<td>GND_P2MM</td>
<td>ENET_MDI</td>
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#### Audio Net Properties

<table>
<thead>
<tr>
<th>AREA_TYPE</th>
<th>SPACING_RULE_SET</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND_P2MM</td>
<td>DP_90D</td>
</tr>
<tr>
<td>GND_P2MM</td>
<td>LVDS_100D</td>
</tr>
</tbody>
</table>

#### Physical Net Properties

<table>
<thead>
<tr>
<th>NET_TYPE</th>
<th>PHYSICAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>DISPLAYPORT</td>
<td>DP_90D</td>
</tr>
<tr>
<td>LVDS</td>
<td>LVDS_100D</td>
</tr>
<tr>
<td>SATA</td>
<td>SATA_90D</td>
</tr>
<tr>
<td>USB</td>
<td>USB_90D</td>
</tr>
</tbody>
</table>

### Override Conditions

- OVERRIDE OVERRIDE OVERRIDE OVERRIDE OVERRIDE OVERRIDE OVERRIDE OVERRIDE

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*Note: The page contains detailed electronic component placements and net properties, including specific spacing rules and area type definitions. The content is structured in tables and diagrams to facilitate detailed analysis and design processes.*
### PHYSICAL RULE SET

<table>
<thead>
<tr>
<th>TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM</th>
<th>1:1_DIFFPAIR</th>
<th>110_OHM_DIFF</th>
<th>110_OHM_DIFF</th>
<th>110_OHM_DIFF</th>
<th>100_OHM_DIFF</th>
<th>100_OHM_DIFF</th>
<th>100_OHM_DIFF</th>
<th>90_OHM_DIFF</th>
<th>90_OHM_DIFF</th>
<th>27P4_OHM_SE</th>
<th>40_OHM_SE</th>
<th>55_OHM_SE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

ON LAYER?

Y | N | Y | Y | Y | Y | Y | Y | Y | Y | Y | Y |

MINIMUM LINE WIDTH

0.077 MM | 0.075 MM | 0.091 MM | 0.075 MM | 0.112 MM | 0.095 MM | 0.185 MM | 0.222 MM | 0.310 MM | 0.126 MM | 0.165 MM | 0.115 MM | 0.090 MM |

MINIMUM NECK WIDTH

= STANDARD | 0.075 MM | 0.112 MM | 0.185 MM | 0.109 MM | 0.310 MM | 0.100 MM | 0.076 MM | 0.115 MM | 0.076 MM | = DEFAULT |

MAXIMUM NECK LENGTH

= STANDARD | 0.075 MM | 0.112 MM | 0.185 MM | 0.109 MM | 0.310 MM | 0.100 MM | 0.076 MM | 0.115 MM | 0.076 MM | = DEFAULT |

DIFFPAIR PRIMARY GAP

= STANDARD | 0.220 MM | 0.234 MM | 0.224 MM | 0.224 MM | 0.224 MM | 0.224 MM | 0.224 MM | 0.224 MM | 0.224 MM | = DEFAULT |

DIFFPAIR NECK GAP

= STANDARD | 0.234 MM | 0.234 MM | 0.234 MM | 0.234 MM | 0.234 MM | 0.234 MM | 0.234 MM | 0.234 MM | 0.234 MM | = DEFAULT |

LINE-TO-LINE SPACING

0.25 MM | 0.15 MM | 0.4 MM | 0.3 MM | 0.3 MM | 0.3 MM | 0.2 MM | 0.1 MM | 0.1 MM | 0.1 MM | = DEFAULT |

NET_PHYSICAL_TYPE

MEM_40S | CLK_PCIE | CLK_PCIE | MEM_40S | MEM_40S | MEM_40S | MEM_40S | MEM_40S | MEM_40S | MEM_40S |

SYNC_MASTER


NET_SPACING_TYPE1

MEM_40S | MEM_40S | MEM_40S | MEM_40S | MEM_40S | MEM_40S | MEM_40S | MEM_40S | MEM_40S | MEM_40S |

NET_SPACING_TYPE2

MEM_40S | MEM_40S | MEM_40S | MEM_40S | MEM_40S | MEM_40S | MEM_40S | MEM_40S | MEM_40S | MEM_40S |

### SPACING RULE SET

<table>
<thead>
<tr>
<th>TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM</th>
<th>2.5:1_SPACING</th>
<th>1.5:1_SPACING</th>
<th>1.5X_DIELECTRIC</th>
<th>4X_DIELECTRIC</th>
<th>3X_DIELECTRIC</th>
<th>2X_DIELECTRIC</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

LINE-TO-LINE SPACING

0.25 MM | 0.15 MM | 0.4 MM | 0.3 MM | 0.3 MM | 0.3 MM | 0.2 MM |

WEIGHT

MEM_40S | MEM_40S | MEM_40S | MEM_40S | MEM_40S | MEM_40S | MEM_40S |

BGA_P3MM | BGA_P2MM | BGA_P2MM | BGA_P1MM | BGA_P1MM | BGA_P1MM | BGA_P1MM |

LAYER

* | * | * | * | * | * | * |

INDEX OF SPACING ASSIGNMENT

* | * | * | * | * | * | * |

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