PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 12
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

1. PREPREG (3MIL)
   SIGNAL (1/3 OZ + COPPER PLATING)

2. PREPREG (3MIL)
   GROUND (1/2 OZ)

3. LAMINATE (4MIL)
   SIGNAL (1/2 OZ)

4. PREPREG (3MIL)
   SIGNAL (1/2 OZ)

5. LAMINATE (4MIL)
   GROUND (1/2 OZ)

6. PREPREG (2MIL)
   CUT POWER PLANE (1 OZ)

7. LAMINATE (3MIL)
   CUT POWER PLANE (1 OZ)

8. PREPREG (2MIL)
   GROUND (1/2 OZ)

9. LAMINATE (4MIL)
   SIGNAL (1/2 OZ)

10. PREPREG (3MIL)
    SIGNAL (1/2 OZ)

11. LAMINATE (4MIL)
    GROUND (1/2 OZ)

12. PREPREG (3MIL)
    SIGNAL (1/3 OZ + COPPER PLATING)
SEL = LOW; HOST = B PORT; A PORT = 1000ΩM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 1000ΩM TO GND
MEM_MUXSEL_H<0> AND MEM_MUXSEL_L<0> ARE ACTIVE LOW
MEM_MUXSEL_H<1> AND MEM_MUXSEL_L<1> ARE ACTIVE HIGH

ADDED 0 ΩM RESISTORS IN CASE POLARITY IS WRONG
null
NOTE: Target differential impedance for Line To Line: 15 mils
For 4.15V cells, $V_{CTL} = 0.123 \times \text{REFIN}$

$V = \text{CELLS} \times (4.096 + (0.4096 \times \frac{V}{V_{CELL}}))$
<table>
<thead>
<tr>
<th>Group</th>
<th>Signal Name</th>
<th>Rise_Trap</th>
<th>Pulse_Param</th>
<th>Scale</th>
</tr>
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<tbody>
<tr>
<td>MAXBUS</td>
<td>I2C_GPIO42</td>
<td>250.0000</td>
<td>200.0000</td>
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<tr>
<td></td>
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<td>100.0000</td>
<td>100.0000</td>
<td>3</td>
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<td></td>
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<td>500.0000</td>
<td>500.0000</td>
<td>3</td>
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</tbody>
</table>

**DIGITAL SIGNALS GROUP 4/5**

- **Control**
  - MEM_CAS_L
  - MEM_RAS_L
  - MEM_CKE<3..0>
  - RAM_CS_L<3..0>
  - MEM_CS_L<3..0>
  - MEM_DQS<7>
  - RAM_DQM_B<6>
  - RAM_DQM_A<6>
  - MEM_DQM<6>
  - RAM_DQS_A<6>
  - MEM_DQS<6>
  - RAM_DATA_B<55..48>
  - RAM_DATA_A<55..48>
  - MEM_DATA<55..48>
  - RAM_DQM_A<5..4>
  - RAM_DQS_B<5..4>
  - RAM_DQS_A<5..4>
  - MEM_DQS<5..4>
  - RAM_DATA_B<47..32>
  - RAM_DQM_B<3..2>
  - RAM_DQS_A<3..2>
  - RAM_DATA_A<31..16>
  - MEM_DATA<31..16>
  - RAM_DQS_B<1>
  - MEM_DQS<1>
  - RAM_DATA_B<15..8>
  - RAM_DQM_B<0>
  - RAM_DQM_A<0>
  - MEM_DQS<0>
  - MEM_DATA<7..0>

**CPU**

-CPU_TT<0..4>
- CPU_HIT_L
- CPU_GBL_L
- CPU_DRDY_L
- CPU_DATA<0..31>
- CPU_ADDR<0..31>
- CPU_AACK_L
- CPU_TA_L
- CPU_BR_L
- FIREWIRE
- MAP31
- CRYSTALS
- SHT

**CLOCK LINE CONSTRAINTS**

- GPU_FBCLK0
- INT_AGP_FB_IN
- INT_AGP_FB_OUT
- INT_REF_CLK_IN
- INT_REF_CLK_OUT
- SYSCLK_DDRCLK_A1_L
- SYSCLK_DDRCLK_A1
- SYSCLK_DDRCLK_A0
- SYSCLK_DDRCLK_B0_UF
- SYSCLK_DDRCLK_A1_UF
- INT_CPUFB_OUT_NORM
- SYSCLK_CPU

**MEMORY**

- DDRCLK_B1
- DDRCLK_B0
- DDRCLK_A1
- DDRCLK_A0

SHOULD BE AT MOST 4 VIAS FOR CLK
THERE'S ANOTHER 280MIL LEG
<table>
<thead>
<tr>
<th><strong>Digital Signals (cont'd)</strong></th>
<th><strong>PCI</strong></th>
<th><strong>Ultra ATA-1</strong></th>
<th><strong>IDE</strong></th>
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<tbody>
<tr>
<td><strong>AGP</strong></td>
<td><strong>PCI</strong></td>
<td><strong>Ultra ATA-1</strong></td>
<td><strong>IDE</strong></td>
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<tr>
<td>AGP VTSX1</td>
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<td>AGP VTSX2</td>
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<td>AGP VTSX3</td>
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<td>AGP VTSX5</td>
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<td>AGP VTSX9</td>
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<tr>
<td><strong>PCI</strong></td>
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<tr>
<td><strong>Ultra ATA-1</strong></td>
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</tr>
<tr>
<td><strong>IDE</strong></td>
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<td></td>
<td></td>
</tr>
<tr>
<td><strong>SIGNAL CONSTRAINTS</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**INTERNAL LAYER**
- \( E_R = 4.3 \) (DIELECTRIC CONSTANT)
- \( W = 4.0 \) MIL (TRACE WIDTH)
- \( B = 12.2 \) MIL (DIST BETW 2 GND PLANES)
- \( T = 0.7 \) MIL (TRACE THICKNESS)
- \( S = 10 \) MIL (SEPARATION OF DIFF TRACES)
- \( z_{single} = 51.570 \) OHM
- \( z_{diff} = 99.860 \) OHM

For Firewire:
- \( E_R = 4.3 \) (DIELECTRIC CONSTANT)
- \( W = 3.4 \) MIL (TRACE WIDTH)
- \( B = 12.2 \) MIL (DIST BETW 2 GND PLANES)
- \( T = 0.7 \) MIL (TRACE THICKNESS)
- \( S = 10 \) MIL (SEPARATION OF DIFF TRACES)
- \( z_{single} = 53.370 \) OHM
- \( z_{diff} = 107.170 \) OHM

**INTERNAL LAYER (USB1.1/USB 2.0)**
- \( E_R = 4.3 \) (DIELECTRIC CONSTANT)
- \( W = 4.0 \) MIL (USB 1.1)/ 5.0 (USB 2.0) (TRACE WIDTH)
- \( B = 12.2 \) MIL (DIST BETW 2 GND PLANES)
- \( T = 0.7 \) MIL (TRACE THICKNESS)
- \( S = 10 \) MIL (SEPARATION OF DIFF TRACES)
- \( z_{single} = 51.500 \) OHM (USB 1.1)/ 46.400 (USB 2.0)
- \( z_{diff} = 89.300 \) (USB 1.1)/ 89.400 (USB 2.0)

---

**Differential Signals**

<table>
<thead>
<tr>
<th>SIGNAL</th>
<th>DIFFERENTIAL</th>
<th>S</th>
<th>DIFF</th>
<th>DIFFERENTIAL</th>
<th>S</th>
<th>DIFF</th>
<th>DIFFERENTIAL</th>
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<tr>
<td>TMDS_D0</td>
<td>TMDS_DP&lt;0&gt;</td>
<td>25</td>
<td>19</td>
<td>TMDS_D1</td>
<td>13</td>
<td>28</td>
<td>TMDS_DP&lt;1&gt;</td>
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<tr>
<td>TMDS_D1</td>
<td>TMDS_DP&lt;1&gt;</td>
<td>25</td>
<td>19</td>
<td>TMDS_D2</td>
<td>13</td>
<td>28</td>
<td>TMDS_DP&lt;2&gt;</td>
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<tr>
<td>TMDS_D2</td>
<td>TMDS_DP&lt;2&gt;</td>
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<td>TMDS_D3</td>
<td>13</td>
<td>28</td>
<td>TMDS_DP&lt;3&gt;</td>
</tr>
</tbody>
</table>

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**POWER**
- \( V_{CC} = 5.00 \) V (USB 1.1)/ 3.30 (USB 2.0)
- \( V_{CC} = 12.00 \) V (USB 1.1)/ 15.00 (USB 2.0)

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<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
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<tbody>
<tr>
<td><strong>FUNCTIONAL TEST POINTS</strong></td>
<td><strong>FUNCTIONAL TEST POINTS</strong></td>
<td><strong>FUNCTIONAL TEST POINTS</strong></td>
<td><strong>FUNCTIONAL TEST POINTS</strong></td>
</tr>
<tr>
<td><strong>JTAG_ASIC_TDO</strong></td>
<td><strong>JTAG_CPU_TDO_TP</strong></td>
<td><strong>VGA_B</strong></td>
<td><strong>NEC_RIGHT_USB_OVERCURRENT</strong></td>
</tr>
<tr>
<td><strong>CPU_CHKSTP_OUT_L</strong></td>
<td><strong>JTAG_CPU_TMS</strong></td>
<td><strong>LVDS_L0P</strong></td>
<td><strong>SHT</strong></td>
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<td><strong>JTAG_ASIC_TCK</strong></td>
<td><strong>CPU_SRESET_L</strong></td>
<td><strong>LVDS_L1N</strong></td>
<td><strong>COMM_GPIO_L</strong></td>
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<td><strong>JTAG_ASIC_TMS</strong></td>
<td><strong>INT_I2C_DATA1</strong></td>
<td><strong>LVDS_L2N</strong></td>
<td><strong>COMM_DTR_L</strong></td>
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<td><strong>FUNC_TEST=YES</strong></td>
<td><strong>INT_I2C_DATA2</strong></td>
<td><strong>ROM_RW_L</strong></td>
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<td><strong>FUNC_TEST=YES</strong></td>
<td><strong>INT_I2C_CLK2</strong></td>
<td><strong>SND_SCLK</strong></td>
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<td><strong>FUNC_TEST=YES</strong></td>
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<td><strong>BT_USB_DP</strong></td>
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<td><strong>ID_290</strong></td>
<td><strong>DCDC_EN</strong></td>
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<td><strong>INT_MOD_DTI</strong></td>
<td><strong>JTAG_CPU_TRST_L</strong></td>
<td><strong>MODEM_USB_DP</strong></td>
<td><strong>ADAPTER_DET</strong></td>
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<td><strong>MAIN_RESET_L</strong></td>
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<td><strong>NEC_LEFT_USB_OVERCURRENT</strong></td>
<td><strong>PWR_BUTTON_L</strong></td>
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<td><strong>I294</strong></td>
<td><strong>I298</strong></td>
<td><strong>FUNCTIONAL TEST POINTS</strong></td>
<td><strong><a href="http://www.vinafix.vn">www.vinafix.vn</a></strong></td>
</tr>
</tbody>
</table>
REVISION HISTORY

12/11/03
1) ADD CPU_TEMP_DM NETNAME AND CPU_THERM_DM
2) ADD PLL CONFIG STUFFING FOR NEW CPU
3) R751 VALUE FROM 10K OHM CHANGE TO 604 OHM
4) D8 FROM 1N5227B CHANGE TO BZX84C2V7LT1
5) GPU_DVOD<0..12> NETNAME CHANGE TO GPU_DVOD<0..23>

12/15/03
1) ADD R867 (0 OHM) FOR IPOD ACTION
2) ADD C935 (0.1UF)
3) 09/17/2004

09/17/2004
1) REPLACE BOOT BANGER EEPROM U32 WITH 32KX M24256B FUNC_TP_WRONG_SIDE.LOG
2) CHANGE TEST POINT FUNC_TEST=NO FOR FUNC_TP_WRONG_SIDE.LOG
3) ADD R465 FROM MF 1/16W TO FF 1/10W
4) CHANGE PIN 11 OF J11 TO NC
5) CHANGE PIN 4 (DCDC_EN) ON J11 TO NEC_RIGHT_USBOVERCURRENT
6) CHANGE JTAG_ASIC_TDI TO CONNECT TO ETHERNET PHY'S TDI
7) CHANGE JTAG_ASIC_TDO_TP TO JTAG_ASIC_TDO AND MOVED IT TO INTREPID'S TDO
8) ADD R608 TO DISCONNECT INT_GPIO0 FROM CG_FSEL
9) ADD R284 AND R604 TO ADD OPTION FOR PD_L OF U42 (CLOCK CHIP) TO BE DRIVEN BY JTAG_ASIC_TDO FROM INTREPID
10) ADD CPU AVDD LDO (U6)

09/20/2004
1) ADD R676 (1K0,1000OHM,STAB) ON DCDC питания
2) ADD R676 (1K0,1000OHM,STAB)

09/21/2004
1) ADD R676 (1K0,1000OHM,STAB) ON DCDC питания
2) ADD R676 (1K0,1000OHM,STAB)

09/22/2004
1) ADD R676 (1K0,1000OHM,STAB) ON DCDC питания
2) ADD R676 (1K0,1000OHM,STAB) ON DCDC питания

09/23/2004
1) ADD R676 (1K0,1000OHM,STAB) ON DCDC питания
2) ADD R676 (1K0,1000OHM,STAB) ON DCDC питания

09/24/2004
1) ADD R676 (1K0,1000OHM,STAB) ON DCDC питания
2) ADD R676 (1K0,1000OHM,STAB) ON DCDC питания

10/04/2004
1) QUINTA EE, PLEASE ADD SCHEMATIC UPDATE DETAILS HERE.
2) UPDATE DIFF NET_SPACING_TYPE PROPERTY ON POWER SUPPLY SENSE AND THERMAL DIODE DIFF PAIRS
3) CHANGED R657 (EXTPLL_SDWNPOL BOOT STRAP) TO NO STUFF AND REMOVED NO STUFF FROM R153
4) FIXED MISSED CONNECTION WITH MAXBUS_SLEEP TO CPU
5) CHANGED GPU_THERM_DM TO GPU_THERM_DM_TP
6) CHANGED CPU_TEMP_DM TO CPU_THERM_DM
7) CHANGED CPU_TEMP_DM TO CPU_THERM_DM
8) CHANGED CPU TEMP_DM TO CPU_THERM_DM

10/05/2004
1) ADD VPO (0 OHM)

09/24/2004
1) REMOVED ALTERNATE BOM OPTION FROM ALTERNATE ETHERNET CRYSTALS
2) CHANGED CPU PLL CONFIG TO 9X HIGH AND 5X LOW
3) REMOVED XW11 - JUMPER ON 1.8V SWITCHER OUTPUT
4) 21) CHANGED MAX VIA COUNT ON ALL AGP STB NETS TO 5 TO CLEAR DRCS
5) CHANGED FIREWIRE OSCILLATOR (G1) TO NEW PREFERRED SUNNY PART
6) UPDATE DIFF NET_SPACING_TYPE PROPERTY ON POWER SUPPLY SENSE AND THERMAL DIODE DIFF PAIRS
7) CHANGED R657 (EXTPLL_SDWN_POL BOOT STRAP) TO NO STUFF AND REMOVED NO STUFF FROM R153
8) ADD R608 TO DISCONNECT INT_GPIO0 FROM CG_FSEL
9) ADD R284 AND R604 TO ADD OPTION FOR PD_L OF U42 (CLOCK CHIP) TO BE DRIVEN BY JTAG_ASIC_TDO FROM INTREPID
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6) CHANGED CPU_TEMP_DM TO CPU_THERM_DM
7) CHANGED CPU TEMP_DM TO CPU_THERM_DM
8) CHANGED CPU TEMP_DM TO CPU_THERM_DM
9) CHANGED CPU TEMP_DM TO CPU_THERM_DM
10) CHANGED CPU TEMP_DM TO CPU_THERM_DM

10/05/2004
1) ADD VPO (0 OHM)

09/22/2004
1) ADD R878 AND R879 (0 OHM; NO_STUFF)
2) ADD A 0-OHM RESISTOR TO BY-PASS THE N-FET ON EACH FAN

09/21/2004
1) ADD R878 (470K OHM; NO_STUFF)
2) ADD R876 (470K OHM; NO_STUFF)
3) ADD R877 (10K OHM)
4) ADD R877 (10K OHM)

09/20/2004
1) ADD R876 (10K OHM)
2) ADD R876 (10K OHM)

09/19/2004
1) ADD R876 (10K OHM)
2) ADD R876 (10K OHM)

09/17/2004
1) ADD R876 (10K OHM)
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09/16/2004
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09/15/2004
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09/14/2004
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4) ADD R876 (10K OHM)

09/13/2004
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4) ADD R876 (10K OHM)

09/12/2004
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3) ADD R876 (10K OHM)
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09/11/2004
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4) ADD R876 (10K OHM)