1. All resistance values are in ohms; 0.1 watt ±5%.
2. All capacitance values are in microfarads.
3. All crystals & oscillator values are in hertz.
### Module Parts

<table>
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### Bar Code Labels / EEE #’s

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### BOM Configuration

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| M87_DEBUG | SMC_DEBUG_YES, XDP, XDP_CONN, LPCPLUS |

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**Notes:**

- All parts are subject to change without notice.
- Critical parts are marked with "CRITICAL."
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Drawing Number

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Size

1.2.0: 06/27/07 -- Aliasing: Cleanup

0.6.0: 04/26/07 -- Clock Termination: Added S0-powered AND gate between GPU_PGOOD and SLG2AP101 enable pin to eliminate leakage path (rdar://5086613)

0.11.0: 04/26/07 -- Power Control: Removed U7858 and R7860. Tied SMC_PM_G2_EN/PM_G2_EN directly to S5 regulators

0.12.0: 06/27/07 -- MUX Gfx: Delete GPU PGOOD Monitor

0.1.0: 04/26/07 -- Design branched from 051-7225-A

0.7.0: 05/08/07 -- GPU Straps: Added SIGNAL_MODEL=EMPTY properties to current sense diff pairs (rdar://5192397)

0.9.0: 05/08/07 -- GPU Straps: Changed R8728 to put GPU PEG I/F into mobile mode (rdar://5192397)

0.10.0: 05/10/07 -- Current Sensors: Changed R5425/35/45 to RES_SENSE symbol which implements kelvin sensing without the need for XW shorts

0.11.0: 05/10/07 -- Thermal Sensors: Added SIGNAL_MODEL=EMPTY properties to thermal sense diff pairs (rdar://5192397)

0.12.0: 05/10/07 -- SB Misc: Removed EXTGPU_RST_L support for reseting the GPU (hardware control only)

0.1.0: 05/14/07 -- SB Decoupling: Replaced L2700 with 155S0333 for AVL updates

0.2.0: 05/14/07 -- SB Decoupling: Changed C7365 to 10µF, 0603 for future memory expansion

0.3.0: 05/10/07 -- Current Sensors: Added SIGNAL_MODEL=EMPTY properties to current sense diff pairs (rdar://5192397)

0.4.0: 05/14/07 -- Power Control: Added C7365 to 10µF, 0603 to allow soft-start control of S5 regulators (rdar://TMD)

0.5.0: 05/08/07 -- SB Decoupling: Changed C2703 to 138S0578 per Intel recommendations (rdar://5185100)

0.6.0: 05/08/07 -- SB Decoupling: Changed C7365 to 10µF, 0603 for future memory expansion

0.7.0: 05/08/07 -- SB Decoupling: Changed C2703 to 138S0578 per Intel recommendations (rdar://5185100)

0.8.0: 05/08/07 -- SB Decoupling: Changed C2703 to 138S0578 per Intel recommendations (rdar://5185100)

0.9.0: 05/08/07 -- SB Decoupling: Changed C2703 to 138S0578 per Intel recommendations (rdar://5185100)

1.0.0: 05/08/07 -- SB Decoupling: Changed C2703 to 138S0578 per Intel recommendations (rdar://5185100)

2.0.0: 05/14/07 -- Power Control: Added C7365 to 10µF, 0603 to allow soft-start control of S5 regulators (rdar://TMD)

3.0.0: 05/08/07 -- SB Decoupling: Changed C2703 to 138S0578 per Intel recommendations (rdar://5185100)

4.0.0: 05/08/07 -- SB Decoupling: Changed C2703 to 138S0578 per Intel recommendations (rdar://5185100)

5.0.0: 05/08/07 -- SB Decoupling: Changed C2703 to 138S0578 per Intel recommendations (rdar://5185100)

6.0.0: 05/08/07 -- SB Decoupling: Changed C2703 to 138S0578 per Intel recommendations (rdar://5185100)

7.0.0: 05/08/07 -- SB Decoupling: Changed C2703 to 138S0578 per Intel recommendations (rdar://5185100)

8.0.0: 05/08/07 -- SB Decoupling: Changed C2703 to 138S0578 per Intel recommendations (rdar://5185100)

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10.0.0: 05/08/07 -- SB Decoupling: Changed C2703 to 138S0578 per Intel recommendations (rdar://5185100)

11.0.0: 05/08/07 -- SB Decoupling: Changed C2703 to 138S0578 per Intel recommendations (rdar://5185100)
## Functional Test Points

**Fan Connectors**
- FFSX_3V5L_FAN
- FFSX_5V_L_FAN
- FFSX_12V_FAN
- FFSX_12V2_FAN
- FFSX_12V3_FAN
- FFSX_12V4_FAN
- Left ALS Connector

**Battery Digital Connector**
- BATT
- BATT

**LPC+ Debug Connector**
- SOC_D0
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**Thermal Module Holes**

Top CPU Right

- Left CPU Right

- Top GPU Right

**RAM Door (Torx) Holes**

**Frame Holes**

- Board Edge Notches (Can't be PTH)

- Tooling Holes (Can't be PTH)

**Digital Ground**

**Signal Aliases**

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**DRAWING NUMBER**

**SHEET OF**

**SIZE**

**REV. A**

**SCALE**

**REV.**

**DRAWING NUMBER**
CPU VCORE HF AND BULK DECOUPLING

- Critical
- Placement Note: Place near CPU pin B26.

C1200, C1202, C1204, C1205, C1206, C1208, C1209

1x 330uF, 20x 22uF 0402

VCCP (CPU I/O) DECOUPLING

- Critical
- Placement Note: Place in CPU center cavity.

C1220, C1221, C1223, C1224, C1225, C1226, C1227, C1228

1x 470uF, 6x 0.1uF 0402

VCCA (CPU AVdd) DECOUPLING

- Critical
- Placement Note: Place in CPU center cavity.

C1230, C1231, C1232, C1233, C1234, C1235

1x 10uF, 1x 0.1uF

CPU VCORE VID CONNECTIONS

- Critical

C1240, C1241

6.3V 20%

22uF CERM-X5R805
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0451 adapter board to support CPU, NB & SB debugging.
Leave GFX_VID<3..0> and GFX_VR_EN as NC.

Tie VCC_AxG and VCC_AxG_NCTF to GND.

Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore).

Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).

Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.

TV_DCONSELx to GND.

Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and filtered at all times!

VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC, all CRT/TVDAC rails must be powered. All

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND.

Component: DACA, DACB & DACC

S-Video:   DACB & DACC only

Composite: DACA only

If SDVO is used, VCCA_SDVO must remain powered with proper
decoupling. Otherwise, tie VCCA_SDVO to GND also.

Note: SR DG says to tie LVDS_VREFH/L to GND. This causes

a glitch during wake-up on LVDS DATA/CHE pairs. Heres

recommendation is to float both signals, see Radar #5267336.

LVDS disable

See above all signals NC if LVDS is not implemented.

Tie VCU_LVDS and VCU_LVDS to GND.

If SDVO is used, VCU_SDVO must remain powered with proper
decoupling. Otherwise, tie VCU_SDVO to GND also.

Note: SR DG says to tie LVDS_VREFH/L to GND. This causes

a glitch during wake-up on LVDS DATA/CHE pairs. Heres

recommendation is to float both signals, see Radar #5267336.

Unused DAC outputs must remain powered, but can

omit filtering components. Unused DAC outputs

must be terminated with 75-ohm resistors.

LVDS disable / CRT Enable

Tie VCU_LVDS and VCU_LVDS to GND. Must power all

TVDAC calls. VCU_TV_DAC and VCU_TV_DAC_B can

share filtering with VCU_CRT_DAC.

CRT Enable / TV-Out Disable

Tie k/EE/EE2/EE2 to GND. HSYNC and VSYNC to GND.

All CRT/TVDAC calls must be powered. All

rails must be filtered except for VCCA_CRT.

CRT & TV-Out Disable

Tie DPLL_AxG to GND or 0/1/0/0/1/0, SYNC, VSYNC, CRT_VDCREF to GND.

Can tie the following calls to GND:

CS.CV.SDT.SDA., CRT.VDCREF.CRT.,

VCC_CRT, VCC_DPLLA and VCC_DPLLB.

NOTE: Must keep VCC_TV_DAC powered

and filtered at all times!

Internal Graphics Disable

Filtering instructions for SDVO are CRT & TV-Out Disable above.

Can also tie CRT_DDC_, L_CTRL_, L_DDC_, SDVO_CTRL_ and

TV_SCHERIES to GND.

Tie TVDVO_1 and TVDVO_1 to VCC (VCore).

Tie LVDS_VREFL and LVDS_VREFH to VCC (VCore).

Tie VCU_AUD and VCU_AUD оформите to GND.

Refer to VCC_DPLLA and VCC_DPLLB as RC.
Crestline Thermal Diode Pins

Mainly for investigation. If not used, alias these nets directly to GND.

NOTE: U3 = _P

NOTE: TDE = _P

NOTE: T3 = _P

NOTE: T2 = _P

NOTE: Y4 = _P

NOTE: Y3 = _P

NOTE: Y2 = _P

NOTE: Y1 = _P

NOTE: Y0 = _P

NOTE: Y = _P

NOTE: W4 = _P

NOTE: W3 = _P

NOTE: W2 = _P

NOTE: W1 = _P

NOTE: W0 = _P

NOTE: V4 = _P

NOTE: V3 = _P

NOTE: V2 = _P

NOTE: V1 = _P

NOTE: V0 = _P

NOTE: U4 = _P

NOTE: U3 = _P

NOTE: U2 = _P

NOTE: U1 = _P

NOTE: U0 = _P

NOTE: Z4 = _P

NOTE: Z3 = _P

NOTE: Z2 = _P

NOTE: Z1 = _P

NOTE: Z0 = _P

NOTE: T4 = _P

NOTE: T3 = _P

NOTE: T2 = _P

NOTE: T1 = _P

NOTE: T0 = _P

NOTE: Y4 = _P

NOTE: Y3 = _P

NOTE: Y2 = _P

NOTE: Y1 = _P

NOTE: Y0 = _P

NOTE: W4 = _P

NOTE: W3 = _P

NOTE: W2 = _P

NOTE: W1 = _P

NOTE: W0 = _P

NOTE: V4 = _P

NOTE: V3 = _P

NOTE: V2 = _P

NOTE: V1 = _P

NOTE: V0 = _P

NOTE: U4 = _P

NOTE: U3 = _P

NOTE: U2 = _P

NOTE: U1 = _P

NOTE: U0 = _P

NOTE: Z4 = _P

NOTE: Z3 = _P

NOTE: Z2 = _P

NOTE: Z1 = _P

NOTE: Z0 = _P

NOTE: T4 = _P

NOTE: T3 = _P

NOTE: T2 = _P

NOTE: T1 = _P

NOTE: T0 = _P

NOTE: Y4 = _P

NOTE: Y3 = _P

NOTE: Y2 = _P

NOTE: Y1 = _P

NOTE: Y0 = _P

NOTE: W4 = _P

NOTE: W3 = _P

NOTE: W2 = _P

NOTE: W1 = _P

NOTE: W0 = _P

NOTE: V4 = _P

NOTE: V3 = _P

NOTE: V2 = _P

NOTE: V1 = _P

NOTE: V0 = _P

NOTE: U4 = _P

NOTE: U3 = _P

NOTE: U2 = _P

NOTE: U1 = _P

NOTE: U0 = _P

NOTE: Z4 = _P

NOTE: Z3 = _P

NOTE: Z2 = _P

NOTE: Z1 = _P

NOTE: Z0 = _P

NOTE: T4 = _P

NOTE: T3 = _P

NOTE: T2 = _P

NOTE: T1 = _P

NOTE: T0 = _P

NOTE: Y4 = _P

NOTE: Y3 = _P

NOTE: Y2 = _P

NOTE: Y1 = _P

NOTE: Y0 = _P

NOTE: W4 = _P

NOTE: W3 = _P

NOTE: W2 = _P

NOTE: W1 = _P

NOTE: W0 = _P

NOTE: V4 = _P

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NOTE: V0 = _P

NOTE: U4 = _P

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NOTE: T0 = _P

NOTE: Y4 = _P

NOTE: Y3 = _P

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NOTE: Y1 = _P

NOTE: Y0 = _P

NOTE: W4 = _P

NOTE: W3 = _P

NOTE: W2 = _P

NOTE: W1 = _P

NOTE: W0 = _P

NOTE: V4 = _P

NOTE: V3 = _P

NOTE: V2 = _P

NOTE: V1 = _P

NOTE: V0 = _P

NOTE: U4 = _P

NOTE: U3 = _P

NOTE: U2 = _P

NOTE: U1 = _P

NOTE: U0 = _P

NOTE: Z4 = _P

NOTE: Z3 = _P

NOTE: Z2 = _P

NOTE: Z1 = _P

NOTE: Z0 = _P

NOTE: T4 = _P

NOTE: T3 = _P

NOTE: T2 = _P

NOTE: T1 = _P

NOTE: T0 = _P

NOTE: Y4 = _P

NOTE: Y3 = _P

NOTE: Y2 = _P

NOTE: Y1 = _P

NOTE: Y0 = _P

NOTE: W4 = _P

NOTE: W3 = _P

NOTE: W2 = _P

NOTE: W1 = _P

NOTE: W0 = _P

NOTE: V4 = _P

NOTE: V3 = _P

NOTE: V2 = _P

NOTE: V1 = _P

NOTE: V0 = _P

NOTE: U4 = _P

NOTE: U3 = _P

NOTE: U2 = _P

NOTE: U1 = _P

NOTE: U0 = _P

NOTE: Z4 = _P

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NOTE: Z2 = _P

NOTE: Z1 = _P

NOTE: Z0 = _P

NOTE: T4 = _P

NOTE: T3 = _P

NOTE: T2 = _P

NOTE: T1 = _P

NOTE: T0 = _P

NOTE: Y4 = _P

NOTE: Y3 = _P

NOTE: Y2 = _P

NOTE: Y1 = _P

NOTE: Y0 = _P

NOTE: W4 = _P

NOTE: W3 = _P

NOTE: W2 = _P

NOTE: W1 = _P

NOTE: W0 = _P

NOTE: V4 = _P

NOTE: V3 = _P

NOTE: V2 = _P

NOTE: V1 = _P

NOTE: V0 = _P

NOTE: U4 = _P

NOTE: U3 = _P

NOTE: U2 = _P

NOTE: U1 = _P

NOTE: U0 = _P

NOTE: Z4 = _P

NOTE: Z3 = _P

NOTE: Z2 = _P

NOTE: Z1 = _P

NOTE: Z0 = _P

NOTE: T4 = _P

NOTE: T3 = _P

NOTE: T2 = _P

NOTE: T1 = _P

NOTE: T0 = _P

NOTE: Y4 = _P

NOTE: Y3 = _P

NOTE: Y2 = _P

NOTE: Y1 = _P

NOTE: Y0 = _P

NOTE: W4 = _P

NOTE: W3 = _P

NOTE: W2 = _P

NOTE: W1 = _P

NOTE: W0 = _P

NOTE: V4 = _P

NOTE: V3 = _P

NOTE: V2 = _P

NOTE: V1 = _P

NOTE: V0 = _P

NOTE: U4 = _P

NOTE: U3 = _P
NOTE: This filter is required even if using only external graphics.

These 2 caps should be within 4.15 mm of BB node.

Crestline LVDS Strapping

Crestline LVDS Strapping

NOTE: This filter is required even if using only external graphics.

These 2 caps should be within 4.15 mm of BB node.
Coin-Cell Connector

RTC Power Sources

Platform Reset Connections

Unbuffered

SB RTC Crystal

System Reset "Button"

VRMPWRGD Inverter

PWROK Circuit

CPU VCore ForcePSI

Platform Reset Connections

PCI Reset Connections

SB Misc
One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector
ENET Enable Generation

3.3V ENET FET

NOTE: S3 term is guaranteed by source of R3800 & Q3810, MUST BE S3 RAIL.

WLAN Enable Generation

"WLAN" = "S0" || ("S3" && "AC" && "WOW_EN")

Yukon AVDDL LDO

1.9V for Yukon Ultra, 2.5V for Yukon EC

Yukon Ultra requires 1.9V on its magnetics to pass compliance tests

ENET Enable Generation

"ENET" = "S0" || ("S3" && "AC" && "WOL_EN")

Yukon Power Control

APPLE INC.

CRITICAL

SON LREG_TPS79501DRB

10%

402

CERM

6.3V

1UF 1UF

6.3V

CERM

402

10%

16.9K

1%

1/16W MF-LF

402

SOT-23 NTR4101P

5%

50V

402

3.3PF SM-3.2X2.5MM

CRITICAL

CERM402

50V 5%

18PF CERM

5% 50V

CERM

402

18PF

35

35

2N7002DW-X-F SOT-363

SOT-363

13 24

35

2N7002DW-X-F SOT-363

SOT-363

13 24

35

2N7002DW-X-F SOT-363

SOT-363

13 24

5% 50V

402 X5R

0.033UF 5% 1/16W

10K MF-LF

402

5% 1/16W

10K

5% 1/16W

10

5% 1/16W

10K

16V CERM

402

0.01UF 402

10%

35

35

2N7002DW-X-F SOT-363

SOT-363

13 24

35

2N7002DW-X-F SOT-363

SOT-363

13 24

5% 50V

402 X5R

0.033UF 5% 1/16W

10K MF-LF

402

5% 1/16W

10K

5% 1/16W

10

5% 1/16W

10K

16V CERM

402

0.01UF 402

10%

SYNC_DATE=03/16/2007

SYNC_MASTER=T9_NOME

www.vinafix.vn
Transformers should be mirrored on opposite sides of the board.

Place one cap at each pin of transformers

C3900  C3901  C3902  C3903

Place close to connector

R3900  R3901  R3902  R3903

Ethernet Connector

Ethernet Connector

- Place one cap at each pin of transformers
- Transformers should be mirrored on opposite sides of the board
- Place close to connector
FireWire PHY Config Straps

Configures PHY for:
- 2-port Portable Power Class (8)
- Port "a" Data-Stream only (1394A)
- Port "b" Bilingual (1998)

Termination
Place close to FireWire PHY to ensure accurate signal integrity.

Note: Trace PPVP_FW_PORT0 must handle up to 5A

Late-VG Protection Power

PPV4_PHY_LATEOS needs to be biased to at least 2.4V to prevent signal integrity and should be biased in 2.4V for margin. R4390 should be 100 Ohms and a 5.9V rail.
IDE (ODD) Connector

Unused SATA Ports

FATA Connector

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Place L4600 and L4605 at connector pin

External USB Connector

If power source is S3, can tie EN to IN.

SEL=0 Choose SMC

SEL=1 Choose USB

CRITICAL 0603 FERR-220-OHM-2A

6.3V 100UF POLYB2 20%

CRITICAL 6.3V20%

603X5R 10UF 10UF

603X5R 6.3V 20%

0.1UF 20%

10V CERM402

CRITICAL 10V

0.1UF 20%

SMC_DEBUG_YES

24 83

24 83

CERM402 20%

10V

0.1UF

SMC_DEBUG_YES

10K MF-LF402 5% 1/16W

90-OHM-100MA

7 45 46 47

7 45 46 47

DLP11S CRITICAL

90-OHM-100MA

SMC_DEBUG_NO 1/16W MF-LF 0 5%

402

402

0

SMC_DEBUG_NO

16V 20%

402

CERM

0.01uF

External USB Connector

USB2_EXTA_MUXED_P

USB2_EXTA_MUXED_N USB2_RT_N

USB2_RT_P

MIN_NECK_WIDTH=0.5 mm

MIN_LINE_WIDTH=0.5 mm

VOLTAGE=5V

PP5V_S3_RTUSB_ILIM

USB_DEBUGPRT_EN_L USB_EXTA_N

USB_EXTA_P

MIN_NECK_WIDTH=0.5 mm

MIN_LINE_WIDTH=0.5 mm

VOLTAGE=5V

PP5V_S3_RTUSB

USB_EXTA_OC_L

=USB_EXTA_EN

Sync master=M88
Sync date=08/02/2007
NOTE: Unused pins have "SMC_Pxx" names.
Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

If SMS interrupt is not used, pull up to SMC rail.
LPC+ Connector

FWH_INIT_L Generation

PLACEMENT_NOTE=Place Q5190 close to R5190
PLACEMENT_NOTE=Place R5190 to minimize CPU_INIT_L stub

SYNC_DATE=03/19/2007
SYNC_MASTER=M76_MLB

LPC+ Debug Connector

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MMDT3904XF
SOT-363-LF
LPCPLUS

330
1/16W
5%
402
LPCPLUS
5%
1/16W
MF-LF
402
1.3K
LPCPLUS
330
402
MF-LF
5%
1/16W

PLACEMENT_NOTE=Place Q5190 close to R5190
PLACEMENT_NOTE=Place R5190 to minimize CPU_INIT_L stub

LPC_AD<0>
LPC_AD<1>
LPC_FRAME_L
PM_CLKRUN_L
BOOT_LPC_SPI_L
SMC_TMS
SMC_RX_L
LPC_AD<2>
LPC_AD<3>
INT_SERIRQ
PM_SUS_STAT_L
SMC_TDI
SMC_TCK
SMC_RESET_L
SMC_NMI
SMC_MD1
SMC_TX_L
DEBUG_RESET_L
SMC_TRST_L
SMC_TDO

CPU_INIT_LS3V3
CPU_INIT_R_L
PCI_CLK33M_LPCPLUS

LINDACARD_GPIO

www.vinafix.vn
CPU T-Diode Thermal Sensor

(TC0P)

(BM02B-ACHKS-GAN-TF-LF-SN-M)

518S0487

GPU/Heat Pipe & Bottom Case Skin Thermal Sensor

(Th0H)

GPU Die Thermal Sensor

(TG0P)

(TG0T)

Thermal Sensors

(A051-7413 11.0.0)

APPLE INC.
**Left ALS Filter**

Left ALS circuit has 1K series-R

**Right ALS Circuit**

**Keyboard LED Driver**

---

**ALS Support**

---

**Notice of Proprietary Property**

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**Website:** www.vinafix.vn
I2C addresses:
- ADDR low => 0x30, 0x31
- ADDR high => 0x32, 0x33

Alias SCL/SDA to GND if using analog outputs only

Desired orientation when placed on board top-side:
- Package Top
- Top-through View

Desired orientation when placed on board bottom-side:
- +Z (up)
- +Z (down)

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Sudden Motion Sensor (SMS)

SYNC_MASTER=M76_MLB  SYNC_DATE=03/19/2007

www.vinafix.vn
Vout = 0.75V * (1 + Ra / Rb)

Vout = 1.50V

4.5A max output

(L7620 limit)

1.5V Power Supply

VOLTAGE=0V MIN_NECK_WIDTH=0.25 mm MIN_LINE_WIDTH=0.6 mm

VOLTAGE=5V MIN_NECK_WIDTH=0.2 mm MIN_LINE_WIDTH=0.6 mm

GATE_NODE=TRUE

MIN_NECK_WIDTH=0.2 mm MIN_LINE_WIDTH=0.6 mm

MIN_NECK_WIDTH=0.2 mm MIN_LINE_WIDTH=0.25 mm

GATE_NODE=TRUE

MIN_NECK_WIDTH=0.2 mm

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SYNC_DATE=03/12/2007
SYNC_MASTER=M76_MLB

www.vinafix.vn
3.3V FW PHY Supply

Backup power in case of FW bus VP short to keep PHY powered.

Vout = 1.25V * (1 + Ra / Rb)

1.95V FW PHY Supply

Vout = 3.316V
200mA max output (Switcher limit)

VOLTAGE=33V
MIN_NECK_WIDTH=0.25 mm
MIN_LINE_WIDTH=0.5 mm
1.8V Frame Buffer Regulator

Vout = 0.6V * (1 + Ra / Rb)

10A max output

Vout = 1.8V

1.8V Frame Buffer Regulator

CERM25V10%

0.0047uF

402

MF-LF

5%

402

1/16W

0

NO STUFF

603

16V

0.22UF

10%

X7R

CRITICAL

PWRPK-1212-8

SI7110DN

CRITICAL

PWRPK-1212-8

SI7108DNS

MF-LF

5.62K

1%/16W

402

22UF

CRITICAL

CASE-D2-LF

20%

25V

POLY

330UF

2.5V

POLY

20%

CASE-C2S

CRITICAL

402MF-LF

10

1/16W5%

X5R

603

25V

1UF

10%

20%

POLY2.5V

330UF

CASE-C2S

CRITICAL

X5R16V

603

10%

2.2UF

SM

X5R16V10%

2.2UF

603

25V

603X5R

1UF

10%

ISL6269BCRZ

QFN

CRITICAL

402-1

68PF

50VCERM

5%

402

680PF

CERM50V10%

MF-LF1/16W1%

402

40.2K

402

1/16W

MF-LF

30.1K

1%

CERM

10%

16V

0.01UF

402

6.3V20%

X5R

603

10UF

10UF

6.3VX5R

20%

603

2.0K

1%

MF-LF1/16W

1/16W

1%

1K

MF-LF 402

CRITICAL

1.0UH-22A

IHLP2525CZ-SM

1.8V FB Power Supply

051-7413

SYNC_DATE=(MASTER) SYNC_MASTER=(MASTER)

=PP1V8_S0GPU_REG

SWITCH_NODE=TRUE

MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm

PP5V_S5_1V8GPU_VCC

MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm

PP1V8_FB_FB

MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.6 mm

PP1V8_FB_LG

MIN_LINE_WIDTH=0.25 mm

PP1V8_FB_PGOOD

MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm

PP1V8_FB_PHASE

MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm

PP1V8_FB_BOOT

MIN_LINE_WIDTH=0.25 mm

PP5V_S5_1V8GPU_VCC

CRITICAL
Left ALS Connector

White colored version of 518S0369

SATA HDD & IR & SIL Flex Connector

NOTE: SATA UF nets cross DDR2 signals and are to remove this noise from SATA signals.

Top-Case Connector

CRITICAL 90-OHM-100MA 1210-4SM1
Some signals require 27.4-ohm single-ended impedance. Most CPU signals with impedance requirements are 55-ohm single-ended.

CPU Signal Constraints

Design Guide recommends each strobe/signal group is routed on the same layer. Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.

FSB (Front-Side Bus) Constraints

All FSB signals with impedance requirements are 55-ohm single-ended. Worst-case spacing is 2:1 within Addr bus, with 2:1 spacing to the ADDRs.

CPU / FSB Net Properties

Table of net properties with spacing rules.
### Video Signal Constraints

#### SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5

- **50-ohm +/- 15% from first to second termination resistor.**
- **CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedance.**
- **55-ohm +/- 15% from second termination resistor to connector.**
- **37.5-ohm +/- 15% from GMCH to first termination resistor.**

**CRT & TVDAC signal single-ended impedance varies by location:**

- **LVDS signals are 100-ohm +/- 20% differential impedance.**

---

### PCI-Express / DMI Bus Constraints

- **CRT_SYNC2SYNC**
- **LVDS_100D**
- **CRT_SYNC 25 MIL**
- **CRT_50S = 50_OHM_SE**

**TABLE_PHYSICAL_RULE_ITEM**

- **AREA_TYPE SPACING_RULE_SET**
- **NET_SPACING_TYPE1 NET_SPACING_TYPE2**

**TABLE_SPACING_ASSIGNMENT_ITEM**

- **TABLE_SPACING_ASSIGNMENT_HEAD**
- **TABL...
### Disk Interface Constraints

<table>
<thead>
<tr>
<th>Source/Section</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1</td>
<td>USB 2.0 Interface Constraints</td>
</tr>
<tr>
<td>Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.17</td>
<td>USB 2.0 Interface Constraints</td>
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<td>Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.13.2</td>
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### USB 2.0 Interface Constraints

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<th>SPI_CE_L&lt;0&gt;</th>
<th>SPI_CE_L&lt;1&gt;</th>
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<tbody>
<tr>
<td>SPI_CE_R_L&lt;0&gt;</td>
<td>SPI_A_SI_R</td>
<td>SPI_B_SCLK_R</td>
<td>SPI_A_SCLK_R</td>
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<td>USB_EXTC_P</td>
<td>USB_EXTC_N</td>
<td>USB_EXTB_P</td>
<td>USB_EXTB_N</td>
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<tr>
<td>USB_IR_P</td>
<td>USB_TPAD</td>
<td>USB_BT_P</td>
<td>USB_BT_N</td>
</tr>
<tr>
<td>USB_CAMERA_P</td>
<td>USB_CAMERA_N</td>
<td>USB_EXD_P</td>
<td>USB_EXD_N</td>
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<tr>
<td>USB_MINI_P</td>
<td>USB_MINI_N</td>
<td>USB_EXTA_MUXED_P</td>
<td>USB_EXTA_MUXED_N</td>
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<tr>
<td>USB_RBIAS</td>
<td>USB_TPAD_N</td>
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### Internal Interface Constraints

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<td>USB_IR_P</td>
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<td>USB_MINI_P</td>
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<td>USB_CAMERA</td>
<td>USB_CAMERA_N</td>
<td>USB_EXTD_P</td>
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### HD Audio Interface Constraints

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<td>USB 2.0 Interface Constraints</td>
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### Internal Interface Constraints

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**Ethernet (Yukon) Constraints**

*SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30*

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**PCI Bus Constraints**

*SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19*

| PCI_55S * =55_OHM_SE | 55_OHM_SE |

**Controller Link (AMT) Constraints**

*SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30*

**Ethernet (Yukon) Constraints**

*SOURCE: Based on Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30*
### Video Signal Constraints

**GDDR3 Frame Buffer Signal Constraints**

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### G84M Net Properties

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### GPU (G84M) Constraints

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This page appears to be a technical document detailing various signal constraints and net properties for video and GPU signals, along with other electrical and physical constraints. The content is specific to the design of a video signal buffer and related components, including constraints for GDDR3 frame buffer signals and G84M nets. The document includes tables and diagrams illustrating these constraints and properties.
Memory Constraint Relaxations
Allow 0.127 mm nails for >0.127 mm lines for GND bus.
Allow 0.1 mm nails for >0.1 mm lines between thru-hole SO-DIMM pins.

Graphics, SATA Constraint Relaxations
Alternate daisy chain with gap through BGA fanout areas (95-ohm diff)
### M75 Board-Specific Spacing & Physical Constraints

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<th>LAYER</th>
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### PCB Rule Definitions

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**NOTE:** 100_OHM_DIFF is 100-ohm differential impedance on outer layers and 95-ohm on inner layers.