1. All resistance values are in ohms, 0.1 watt +/- 5%.
2. All capacitance values are in microfarads.
3. All crystal & oscillator values are in hertz.
### BOM Variants

<table>
<thead>
<tr>
<th>Part Number</th>
<th>BOM Name</th>
<th>BOM Options</th>
</tr>
</thead>
<tbody>
<tr>
<td>600-9010</td>
<td>BOM_1</td>
<td>600-9010 BOM_1 OPTIONS</td>
</tr>
<tr>
<td>600-9011</td>
<td>BOM_2</td>
<td>600-9011 BOM_2 OPTIONS</td>
</tr>
</tbody>
</table>

### BOM Groups

<table>
<thead>
<tr>
<th>Part Number</th>
<th>BOM Name</th>
<th>BOM Options</th>
</tr>
</thead>
<tbody>
<tr>
<td>M88_000001</td>
<td>M88_COMMON</td>
<td>M88_COMMON BOM_1 OPTIONS</td>
</tr>
<tr>
<td>M88_000002</td>
<td>M88_COMMON1</td>
<td>M88_COMMON1 BOM_1 OPTIONS</td>
</tr>
</tbody>
</table>

### Bar Code Labels / EEE #’s

<table>
<thead>
<tr>
<th>Part Number</th>
<th>QTY</th>
<th>Description</th>
<th>Reference Use</th>
<th>Critical</th>
<th>BOM Options</th>
</tr>
</thead>
<tbody>
<tr>
<td>826-4393</td>
<td>1</td>
<td>LBL, P/N LABEL, PCB, 28MM X 6 MM</td>
<td>CRITICAL</td>
<td>826-4393 CRITICAL EEE_Z3L</td>
<td></td>
</tr>
</tbody>
</table>

### Module Parts

<table>
<thead>
<tr>
<th>Part Number</th>
<th>QTY</th>
<th>Description</th>
<th>Reference Use</th>
<th>Critical</th>
<th>BOM Options</th>
</tr>
</thead>
<tbody>
<tr>
<td>U1000</td>
<td>1</td>
<td>IC, SR, 2.6G, 35W, 800FSB, 6M, BGA</td>
<td>CRITICAL</td>
<td>1338S0509</td>
<td></td>
</tr>
<tr>
<td>U4900</td>
<td>1</td>
<td>IC, 16MBIT 8-PIN SPI SERIAL FLASH, SOIC8</td>
<td>CRITICAL</td>
<td>335S0384</td>
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</tr>
</tbody>
</table>

### Alternate Parts

<table>
<thead>
<tr>
<th>Part Number</th>
<th>QTY</th>
<th>Description</th>
<th>Reference Use</th>
<th>Critical</th>
<th>BOM Options</th>
</tr>
</thead>
<tbody>
<tr>
<td>U1400</td>
<td>1</td>
<td>IC, 88E8058, GIGABIT ENET XCVR, 64P QFN</td>
<td>CRITICAL</td>
<td>338S0386 1</td>
<td></td>
</tr>
<tr>
<td>U2900</td>
<td>1</td>
<td>IC, SLG2AP101, LW PWR CLK GEN, CK505, QFN68</td>
<td>CRITICAL</td>
<td>359S0130 1</td>
<td></td>
</tr>
<tr>
<td>U7100</td>
<td>1</td>
<td>IC, ISL9504B, 2PH IMVP6 REG, PMON, QFN48</td>
<td>CRITICAL</td>
<td>ISL9504B 1353S1651</td>
<td></td>
</tr>
<tr>
<td>U1400</td>
<td>1</td>
<td>IC, SMC, 16MBIT 8-PIN SPI SERIAL FLASH, SOIC8</td>
<td>CRITICAL</td>
<td>338S0274 1</td>
<td></td>
</tr>
<tr>
<td>U2900</td>
<td>1</td>
<td>IC, 88E8058, GIGABIT ENET XCVR, 64P QFN</td>
<td>CRITICAL</td>
<td>338S0386 1</td>
<td></td>
</tr>
</tbody>
</table>

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Functional Test Points

Fan Connectors

Battery Digital Connector

Left I/O Power Connector

LPC+ Debug Connector

RTC Battery Connector

Current Sense Calibration

System Validation TPs

Backlight Connector

IR & Sleep LED Connector

Functional / ICT Test

NOTE: 10 additional GND test points are requested for at least 10 GND test points. 15 additional GND test points are ruled out separately in these notes.

Functional Test Points

ICT Test Points

CPU FSB NO_TESTS

NB NO_TESTS

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DRAWING NUMBER
SHT OF
SIZE

Thermal Module Holes

All holes are plated through holes with two exceptions:

- Chassis GNDs
  - GND CHASSIS BATTCONN HOLE (to the left of DIMM cutout near board edge)
- Digital Ground
- RAM door (Torx) holes
- Frame holes
- Thermal Module Holes
  - GND CHASSIS RAMDOOR HOLE
  - GND CHASSIS RAMDOOR_HOLE_0
  - GND CHASSIS RAMDOOR_HOLE_1

GND CHASSIS BATTCONN_HOLE

Frame holes

- Chassis connection to be made at the mounting hole east of the LVDS connector

Digital Ground

- Holes are plated through holes with two exceptions:

  - GND CHASSIS RAMDOOR HOLE
  - GND CHASSIS RAMDOOR_HOLE_0
  - GND CHASSIS RAMDOOR_HOLE_1

Signal Aliases

- MAKE_BASE = TRUE
- IPHS_SW_INT
- Sync_DATE = 08/23/2006
- MIN_LINE_WIDTH = 0.6mm
- MIN_NECK_WIDTH = 0.25mm
- VOLTAGE = 0V

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PLACE R1024 near ITP connector (if present)
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
Use with 920-0451 adapter board to support CPU, NB & NB debugging.

Direction of XDP module
Please avoid any obstructions on even-numbered side of J1300

www.vinafix.vn
Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore).
Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).

Internal Graphics Disable

NOTE: Must keep VDDC_TVDAC powered
VCCD_CRT, VCCD_QDAC and VCC_SYNC.
VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC,
Can tie the following rails to GND:
rails must be filtered except for VCCA_CRT.
All CRT/TVDAC rails must be powered.  All
TV-Out Disable / CRT Enable

Internal Graphics Disable

TV-out signal setup:
S-Video:  G, B & RGB only
Component:  G, B & RGB
Unused SAC outputs must remain powered, but can
omit filtering components.  Unused SAC outputs
must not pull up to 75-ohm resistors.

TV-out disable / CRT Enable

Can tie the following signals to GND:
VCC_CRT, VCC_OVF, and VCC_SYNC.

CRT & TV-Out Disable

Can tie the following signals to GND:
VCC_SYNC, VCC_RED, VCC_GREEN,
VCC_BLUE, VCC_LVDS, and VCC_VREFH.

Note:  Must keep VCC_OVF powered
and filtered at all times.

Internal Graphics Disable

Please follow instructions for TV-Out and CRT & TV-Out Disable above.
Can also tie CRT_VEC_C, CRT_VEC_H, CRT_VEC_V, and
TV_SCHEDI to GND.

Tie VCC_Red to GND, VCC_Green to GND,
and VCC_Blue to GND.

Internal Graphics Disable

TV-Out Disable / CRT Enable

Can tie the following signals to GND:
VCC_CRT, VCC_OVF, and VCC_SYNC.

Note:  Must keep VDDC_TVDAC powered
and filtered at all times.

Internal Graphics Disable

Please follow instructions for TV-Out and CRT & TV-Out Disable above.
Can also tie CRT_VEC_C, L_CTRL, H_CTRL, and
TV_SCHEDI to GND.

Tie VCC_Red to GND, VCC_Green to GND,
and VCC_Blue to GND.

Internal Graphics Disable

Please follow instructions for TV-Out and CRT & TV-Out Disable above.
Can also tie CRT_VEC_C, CRT_VEC_H, CRT_VEC_V, and
TV_SCHEDI to GND.

Tie VCC_Red to GND, VCC_Green to GND,
and VCC_Blue to GND.

Internal Graphics Disable

Please follow instructions for TV-Out and CRT & TV-Out Disable above.
Can also tie CRT_VEC_C, L_CTRL, H_CTRL, and
TV_SCHEDI to GND.

Tie VCC_Red to GND, VCC_Green to GND,
and VCC_Blue to GND.
Crestline Thermal Diode Pins

Mainly for investigation. If not used, alias these nets directly to GND.

NOTE: TDB = _N
NOTE: TDE = _P
Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.
Left I/O Board Connector

Place caps close to SB

PCIE_MINI_D2R_N
PCIE_MINI_D2R_P
TP_PCIE_EXCARD_D2R_P
TP_PCIE_EXCARD_D2R_N
C3420
C3421
C3411
C3410

Place caps close to SB

USB_MINI_P
USB_MINI_N
PCIE_EXCARD_R2D_P
PCIE_EXCARD_R2D_N
TP_PCIE_EXCARD_R2D_P
TP_PCIE_EXCARD_R2D_N

TP_PCIE_EXCARD_D2R_P
TP_PCIE_EXCARD_D2R_N

PCIE_CLK100M_MINI_N
PCIE_CLK100M_MINI_P
PCIE_MINI_R2D_P
PCIE_MINI_R2D_N

PCIE_MINI_R2D_C_N
PCIE_MINI_R2D_C_P
PCIE_EXCARD_R2D_C_N
PCIE_EXCARD_R2D_C_P

PCIE_EXCARD_R2D_P
PCIE_EXCARD_R2D_N
PCIE_EXCARD_D2R_P
PCIE_EXCARD_D2R_N

PCR one side EN_L
PCR one side EN_P
PCR one side OC_L
PCR one side OC_P

M-ST-SM
QT500806-L121-9F
51650348

10% X5R
0.1uF
16V
C3421

10% X5R
0.1uF
16V
C3420

10% X5R
0.1uF
16V
C3411

10% X5R
0.1uF
16V
C3410

Full-up on LIO, FETS to GND on MLB

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Page Notes

- **ENET_CLKREQ_L**: NC/TP for Yukon EC
- **ENET_VMAIN_AVLBL**: See note by pin

Signal aliases required by this page:
- **PP3V3_ENET_PHY**: Yukon Ultra

---

**Yukon EC (2.5V)**

- 10 Mbps: 179 mA
- 100 Mbps: 126 mA
- 1000 Mbps: 218 mA

**Yukon Ultra (1.8V)**

- 10 Mbps: 179 mA
- 100 Mbps: 150 mA
- 1000 Mbps: 218 mA

---

**Instructions for dual Yukon EC**

1. Place C3730 close to southbridge.
2. **R3741**: 49.9Ω 1% 1/16W
3. **C3742**: 402µF 10% X5R 402 16V
4. **C3736**: 0.1µF 10% X5R 402 16V
5. **R3744**: 0.001µF X5R 402 16V
6. **CERM**: 6.3V 20% 603
7. **R3760**: 1/16W 1%

---

**Note:**

- Yukon EC: Pin 42 should be NC (or TP) net.

---

**Table 1:**

- **IC,FLASH,88E8058 ETHERNET VPD,IIC,SO8**
- **IC,88E8058,GIGABIT ENET XCVR,64P QFN**

---

**Reference:**

- Yukon EC and Ultra on the same board.

---

**Ethernet (Yukon)**

- **ENET_RESET_L**: Yukon Ultra
- **PCIE_CLK100M_ENET_N**: Yukon EC

---

**Notes:**

- Use **YUKON_EC_PP2V5_ENET** to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1µF and 1x 0.001µF caps.

---

**References:**

- [Apple Inc.](www.vinafix.vn)
ENET Enable Generation

NOTE: S3 term is guaranteed by source of R3800 & Q3810, MUST BE S3 RAIL.

WLAN Enable Generation

NOTE: S3 term is guaranteed by FET & pull-up source, MUST BE S3 RAIL.

Yukon AVDDL LDO

Yukon Ultra requires 1.9V on its magnetics to pass compliance tests

Yukon Crystal

Yukon Power Control
Transformers should be mirrored on opposite sides of the board.

Place one cap at each pin of transformers.

10% 6.3V 1uF
CERM
402
C3902
1
2

10% 6.3V 1uF
CERM
402
C3901
1
2

10% 6.3V 1uF
CERM
402
C3903
1
2

Ethernet Connector

ENET_CTAP0
ENET_CTAP1
ENET_CTAP2
ENET_CTAP3

Ethernet Connector

ENETCONN_N<0>
ENETCONN_P<0>
ENETCONN_N<1>
ENETCONN_P<1>
ENETCONN_N<2>
ENETCONN_P<2>
ENETCONN_N<3>
ENETCONN_P<3>

ENET_MDI_P<0>
ENET_MDI_P<1>
ENET_MDI_P<2>
ENET_MDI_P<3>
ENET_MDI_N<0>
ENET_MDI_N<1>
ENET_MDI_N<2>
ENET_MDI_N<3>

ENET_CTAP0
ENET_CTAP1
ENET_CTAP2
ENET_CTAP3

1000BT-824-00275
CRITICAL
T3900
1
2

1000BT-824-00275
CRITICAL
T3901
1
2

Place close to connector

OMIT
CRITICAL
J3900
9
10
11
12
1
2
3
4
5
6
7
8
9
10
11
12

OMIT
CRITICAL
T3900
1
2

OMIT
CRITICAL
T3901
1
2

100PF 1206
C3904
1 2

1000PF 2KV
CERM
1000PF
C3904
1 2

1000BT-824-00275
CRITICAL
T3900
1
2

1000BT-824-00275
CRITICAL
T3901
1
2

Short shielded RJ-45

514-0277
Current Limit/Active Late-VG Protection

Late-VG Event Detection

Enable port power when machine is running or on AC.

FW_PORT_FAULT_PU

Signal aliases required by this page:
- =PPVP_FW_SUMNODE (power passthru summation node)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPBUS_S5_FWPWRSW (system supply for bus power)

Power aliases required by this page:

Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PPVP_FW_LATEVG
- =PPVP_FW_PORTB_UF
- =PPVP_FW_PORTB_ISENSE
- =PPVP_FW_PORTA_UF
- =PPVP_FW_PORTA_ISENSE
- =PPVP_FW_PORTM_ISENSE
- =PPVP_FW_PORTM_UF
- =PPVP_FW_PORTB
- =PPVP_FW_PORTA
- =PPVP_FW_PORTM

Input aliases required by this page:

BOM options provided by this page:
- (NONE)

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A necessary supplement to this document is the drawing:

Left Clutch Barrel Interconnect

SYNC_DATE=08/28/2007
SYNC_MASTER=M87_MLB
NOTE: Unused pins have "NC" name. Unused
pins designated as outputs can be left floating,
those designated as inputs require pull-ups.

NOTE: SMI Interrupt can be active high or low, rename net accordingly.
If SMI interrupt is not used, pull up to 5V rail.

MIN_NECK_WIDTH=0.20 MM
Apple Inc.

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REV. A

SHT OF SIZE D

516S0394

LPC_PLUS Connector FWH_INIT_L Generation

PLACEMENT NOTE=Place Q5190 close to R5190

PLACEMENT NOTE=Place R5190 to minimize CPU_INIT_L stub

SYNC_MASTER=M87_MLB

SYNC_DATE=08/28/2007

LPC+ Debug Connector

LPC+ Debug Connector

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Battery Current Sense

P/N opposite VIN+/- to measure discharge current.

DCIn Current Sense

Battery Charger Thermal Sensor

Placement Note:
Place sensor on bottom side near L8300 and Q8301 and Q8302.

Placement Note:
Place near R8308.

Battery Current Sense

Critical

SOT23-5
INA193
U5705
2

15
3 4

1uF
6.3V
CERM
402
C5715
1

2

10V
CERM
0.1uF
20%
402
C5750
1

2

Note:

Current & Thermal Sensors

SYNC_MASTER=M87_LIO_SYNC
SYNC_DATE=08/23/2007

PP3V3_S0_PBATTISENS
PP3V3_S0_PDCISENS
LIO_BATT_ISENSE
LIO_DCIN_ISENSE
CHGR_CSI_P
CHGR_CSI_R_P
CHGR_CSO_R_P
CHGR_CSO_R_N

=PP3V3_S0_TMPSNSR
=SMBUS_TMPSNSR_SCL
=SMBUS_TMPSNSR_SDA

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Left ALS Filter

Left ALS circuit has 1K series-R

Keyboard LED Driver

Right ALS Circuit

RTALS_OP_IN and RTALS_OP_COMP need to be matched

Critical

---

AL S Support

100KOHM-5%

---

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I2C addresses:
- Addr low => 0x32, 0x33
- Addr high => 0x30, 0x31

Alias SCL/SDA to GND if using analog outputs only

Desired orientation when placed on board top-side:
- Package Top

Desired orientation when placed on board bottom-side:
- Top-through View

Reset circuit:
- SMS_MOT_EN
- SMS_MOT_DIS

Synced signals:
- SMS_X_AXIS = I2C_SMS_SDA
- SMS_Y_AXIS = I2C_SMS_SCL
- SMS_Z_AXIS = PP3V3_S3_SMS
- SMC_SMS_INT

Sudden Motion Sensor (SMS)
TPS51120 LDO/Buffer outputs

Vout = 5.0V
8A max output (L7320 limit)

Vout = 3.3V
5.5A max output (L7360 limit)

50mA max load when EN5 & EN3 high
100mA max load when EN5 high

50mA max load when EN5 & EN3 high
100mA max load when EN5 high

When both are low TPS51120 VIN current drops from 100-150uA to 10-20uA.

EN3 can float or tie to VREG5 for automatic 3.3V LDO enable

NOTE: EN5 can float or tie to VIN for automatic 5V LDO enable

NOTE: EN5 can float or tie to VIN for automatic 5V LDO enable

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3.3V FW PHY Supply

Vout = 3.316V
200mA max output
(Switcher limit)

Vout = 1.25V \times (1 + \frac{R_a}{R_b})

Backup power in case of FW bus
VP short to keep PHY powered.

1.95V FW PHY Supply

Vout = 1.95V
200mA max output

Backup power in case of FW bus
VP short to keep PHY powered.
1.8V Frame Buffer Regulator

Vout = 0.6V * (1 + Ra / Rb)
Most CPU signals with impedance requirements are 55-ohm single-ended.

NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.

FSB_DSTB_55S = 1:1_DIFFPAIR

7 MIL 7 MIL

CPU_2TO1 *

FSB_DSTB_55S = 1:1_DIFFPAIR

Intel says to route with 7 mil spacing without 7 mil gap is for VCCSense pair, which

NOTE: 7 mil gap is for VCCSense pair, which

DG recommends at least 25 mils, >50 mils preferred

SOURCE: Santa Rosa Platform DD, Rev 0.9 (#DS017), Sections 4.2 & 4.3

CPU Signal Constraints

<table>
<thead>
<tr>
<th>Net</th>
<th>Layer</th>
<th>Min. Width</th>
<th>Max. Width</th>
<th>Min. Length</th>
<th>Max. Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU_VCCSENSE</td>
<td>1</td>
<td>25 MIL</td>
<td>70 MIL</td>
<td>10 MIL</td>
<td>20 MIL</td>
</tr>
<tr>
<td>CPU_VCCSENSECPU_27P4S</td>
<td>1</td>
<td>25 MIL</td>
<td>70 MIL</td>
<td>10 MIL</td>
<td>20 MIL</td>
</tr>
<tr>
<td>CPU_2TO1CPU_55S</td>
<td>1</td>
<td>25 MIL</td>
<td>70 MIL</td>
<td>10 MIL</td>
<td>20 MIL</td>
</tr>
<tr>
<td>CPU_VID&lt;6..0&gt;</td>
<td>1</td>
<td>25 MIL</td>
<td>70 MIL</td>
<td>10 MIL</td>
<td>20 MIL</td>
</tr>
<tr>
<td>CPU_COMPCPU_55S</td>
<td>1</td>
<td>25 MIL</td>
<td>70 MIL</td>
<td>10 MIL</td>
<td>20 MIL</td>
</tr>
<tr>
<td>CPU_BSEL&lt;1&gt;CPU_55S</td>
<td>1</td>
<td>25 MIL</td>
<td>70 MIL</td>
<td>10 MIL</td>
<td>20 MIL</td>
</tr>
<tr>
<td>CPU_FROM_SB</td>
<td>1</td>
<td>25 MIL</td>
<td>70 MIL</td>
<td>10 MIL</td>
<td>20 MIL</td>
</tr>
<tr>
<td>CPU_A20M_L</td>
<td>1</td>
<td>25 MIL</td>
<td>70 MIL</td>
<td>10 MIL</td>
<td>20 MIL</td>
</tr>
<tr>
<td>CPU_PROCHOT_LCPU_55S</td>
<td>1</td>
<td>25 MIL</td>
<td>70 MIL</td>
<td>10 MIL</td>
<td>20 MIL</td>
</tr>
<tr>
<td>CPU_FERR_L</td>
<td>1</td>
<td>25 MIL</td>
<td>70 MIL</td>
<td>10 MIL</td>
<td>20 MIL</td>
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<tr>
<td>FSB_ADDR_GROUP1FSB_55S</td>
<td>1</td>
<td>25 MIL</td>
<td>70 MIL</td>
<td>10 MIL</td>
<td>20 MIL</td>
</tr>
<tr>
<td>FSB_ADSTB0</td>
<td>1</td>
<td>25 MIL</td>
<td>70 MIL</td>
<td>10 MIL</td>
<td>20 MIL</td>
</tr>
<tr>
<td>FSB_DATA_GROUP3FSB_55S</td>
<td>1</td>
<td>25 MIL</td>
<td>70 MIL</td>
<td>10 MIL</td>
<td>20 MIL</td>
</tr>
<tr>
<td>FSB_DSTB1</td>
<td>1</td>
<td>25 MIL</td>
<td>70 MIL</td>
<td>10 MIL</td>
<td>20 MIL</td>
</tr>
<tr>
<td>FSB_DSTB0</td>
<td>1</td>
<td>25 MIL</td>
<td>70 MIL</td>
<td>10 MIL</td>
<td>20 MIL</td>
</tr>
<tr>
<td>FSB_CPURST_L</td>
<td>1</td>
<td>25 MIL</td>
<td>70 MIL</td>
<td>10 MIL</td>
<td>20 MIL</td>
</tr>
<tr>
<td>FSB_COMMON</td>
<td>1</td>
<td>25 MIL</td>
<td>70 MIL</td>
<td>10 MIL</td>
<td>20 MIL</td>
</tr>
<tr>
<td>XDP_BPM_L&lt;5&gt;</td>
<td>1</td>
<td>25 MIL</td>
<td>70 MIL</td>
<td>10 MIL</td>
<td>20 MIL</td>
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SOURCE: Santa Rosa Platform DD, Rev 0.9 (#DS017), Sections 4.2 & 4.3

CPU/FSB Constraints

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Video Signal Constraints

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<td>Santa Rosa Platform DG, Rev 1.0 (#21112)</td>
<td>Sections 7.2, 9.2 &amp; 10.5</td>
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**Video Signal Constraints**

- CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedance.
- 55-ohm +/- 15% from second termination resistor to connector.
- 37.5-ohm +/- 15% from GMCH to first termination resistor.
- LVDS signals are 100-ohm +/- 20% differential impedance.

**PCI-Express / DMI Bus Constraints**

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**PCI-Express / DMI Bus Constraints**

- 50-ohm +/- 15% from first to second termination resistor.

**NB Constraints**

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**NB Constraints**

- CRT_DAC/CRT_DAC signals are 100-ohm differential impedance.
- CRT & TDA3 signal single-ended impedance varies by location.
- TDA3 & CRT signals are 100-ohm +/- 15% from GMCH to first termination resistor.
- CRT signals are 100-ohm +/- 15% from first to second termination resistor.
- CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedance.

**Video Signal Constraints**

- CRT_DAC/CRT_DAC signals are 100-ohm differential impedance.
- CRT & TDA3 signal single-ended impedance varies by location.
- TDA3 & CRT signals are 100-ohm +/- 15% from GMCH to first termination resistor.
- CRT signals are 100-ohm +/- 15% from first to second termination resistor.
- CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedance.

**PCI-Express / DMI Bus Constraints**

- 50-ohm +/- 15% from first to second termination resistor.

**NB Constraints**

- CRT_DAC/CRT_DAC signals are 100-ohm differential impedance.
- CRT & TDA3 signal single-ended impedance varies by location.
- TDA3 & CRT signals are 100-ohm +/- 15% from GMCH to first termination resistor.
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- CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedance.

**PCI-Express / DMI Bus Constraints**

- 50-ohm +/- 15% from first to second termination resistor.

**NB Constraints**

- CRT_DAC/CRT_DAC signals are 100-ohm differential impedance.
- CRT & TDA3 signal single-ended impedance varies by location.
- TDA3 & CRT signals are 100-ohm +/- 15% from GMCH to first termination resistor.
- CRT signals are 100-ohm +/- 15% from first to second termination resistor.
- CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedance.
## DDR2 Memory Bus Constraints

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Source: Santa Kona Platform DS, Rev 1.0 (#21112), Sections 10.7 & 10.9

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Source: Santa Kona Platform DS, Rev 1.0 (#21112), Sections 10.12.2

### Internal Interface Constraints

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Source: Santa Platform DS, Rev 1.0 (#21112), Section 10.17
### PCI Bus Constraints

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### Controller Link (AMT) Constraints

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### Ethernet (Yukon) Constraints

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### SB Constraints (2 of 2)

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Clock Signal Constraints

Clock Net Properties

SMC SMBus Net Properties

Clock & SMC Constraints

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6
### FireWire Interface Constraints

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### FireWire Net Properties

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### FireWire Constraints

- **Sync Master**: T9_0, N0, E0
- **Sync Date**: 01/25/2007

**Port 2 Not Used**
GPU (G84M) Constraints

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** rpm-pcb-v7-pcb **

Apple Inc. 11051-7431

www.vinafix.vn
Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

Memory Constraint Relaxations
Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.
Allow 0.1 mm necks for >0.1 mm lines between thru-hole 50-DIP66 pins.

Graphics, SATA Constraint Relaxations
Alternate diffpair width/gap through BGA fanout areas (90-ohm diff)
<table>
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<th>LAYER</th>
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<th>MAXIMUM NECK LENGTH</th>
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**NOTE:** 100_OHM_DIFF is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.