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- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM, BKUP BAT/RT USB, PB17"

07/24/2003

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
A		285242	PRODUCTION RELEASED	07/25/03	?

D

D

C

C

B


B

A

A

PAGE	CONTENTS
1	TITLE PAGE AND CONTENTS
2	PCB NOTES AND HOLES
3	BACK UP BATTERY
4	RIGHT USB PORT
5	CONSTRAINTS / REVISION HISTORY
6	SIGNAL LOCATIONS
7	COMPONENT LOCATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6475	1	SCHEM, BKUP BAT/RT USB, PB17INCH	SCH1	
820-1537	1	PCBF, BKUP BAT/RT USB, PB17INCH	PCB1	

DIMENSIONS ARE IN MILLIMETERS		METRIC		Apple Computer Inc.	
XX : _____		DRAPTER	DESIGN CK	NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	
X.XX : _____		ENG APPD	MFG APPD		
X.XXX : _____		QA APPD	DESIGNER		
ANGLES : _____		RELEASE	SCALE		
DO NOT SCALE DRAWING		SCALE NONE		TITLE	
 THIRD ANGLE PROJECTION		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE D	DRAWING NUMBER
				405686	REV. AA
				SHT 1 OF 7	

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PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
 1/2 OZ CU THICKNESS: 0.7 MILS
 1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
 DIELECTRIC: FR-4
 LAYER COUNT: 12
 SIGNAL TRACE WIDTH: 4 MILS
 SIGNAL TRACE SPACING: 4 MILS
 PREPREG THICKNESS: 2-3 MILS

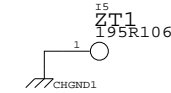
SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

20R10 TH VIA OR VIA IN PAD

1	SIGNAL (1/3 OZ + COPPER PLATING)
2 PREPREG (3MIL)	GROUND (1/2 OZ)
3 LAMINATE (4MIL)	SIGNAL (1/2 OZ)
4 PREPREG (3MIL)	SIGNAL (1/2 OZ)
5 LAMINATE (4MIL)	GROUND (1/2 OZ)
6 PREPREG (2MIL)	CUT POWER PLANE(1 OZ)
7 LAMINATE (3MIL)	CUT POWER PLANE(1 OZ)
8 PREPREG (2MIL)	GROUND (1/2 OZ)
9 LAMINATE (4MIL)	SIGNAL (1/2 OZ)
10 PREPREG (3MIL)	SIGNAL (1/2 OZ)
11 LAMINATE (4MIL)	GROUND (1/2 OZ)
12 PREPREG (3MIL)	SIGNAL (1/3 OZ + COPPER PLATING)

BOARD HOLES



PCB BOARD STANDOFFS

BOARD INFORMATION

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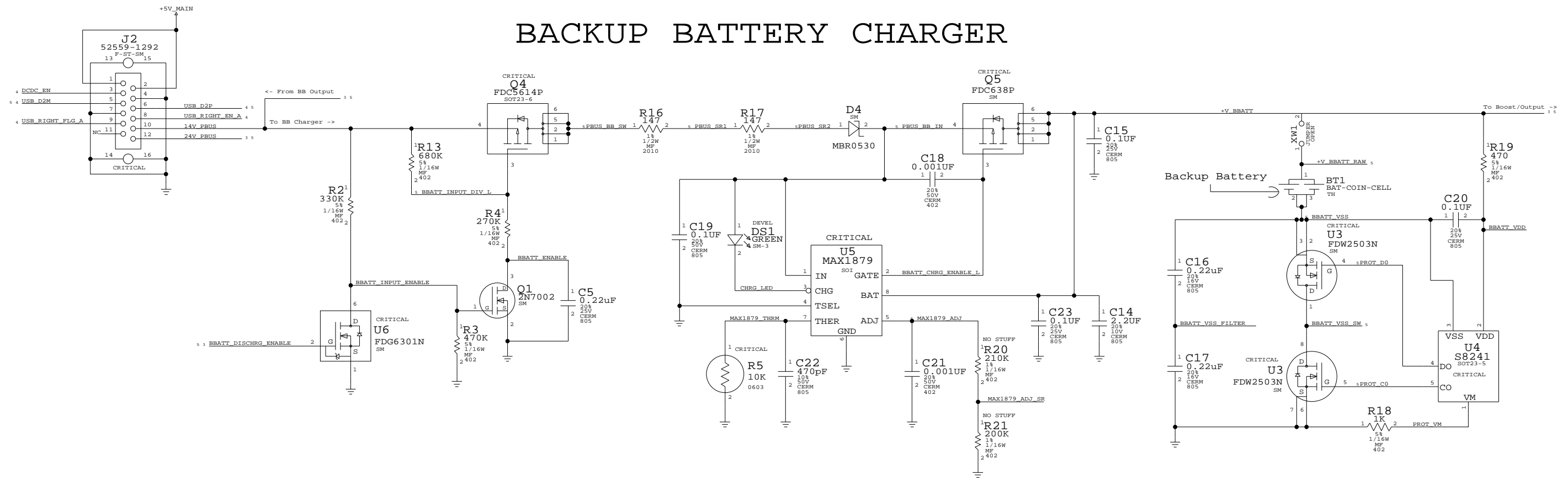
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



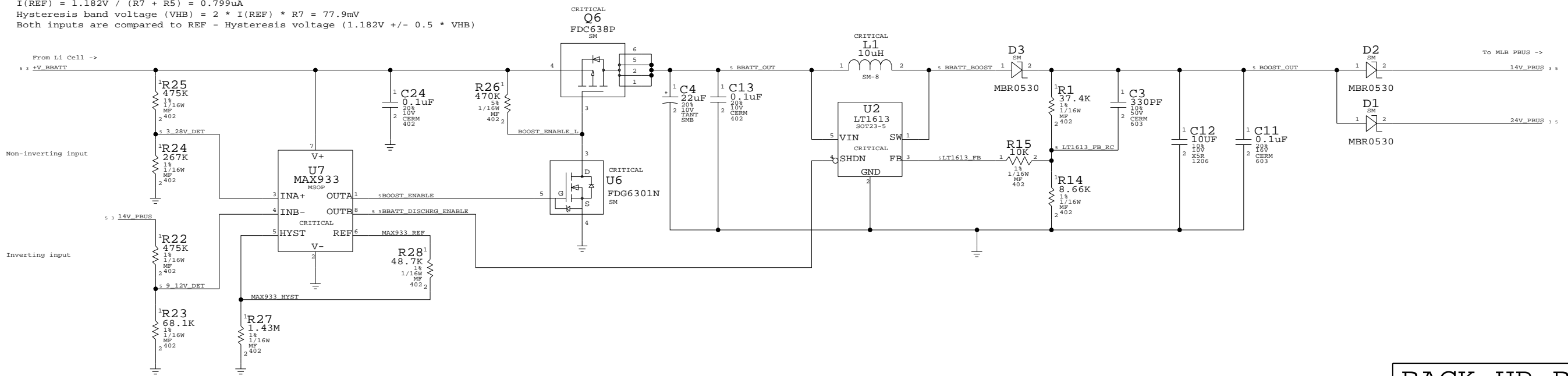
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	405686	AA
SCALE	SHT	OF
NONE	2	7

BACKUP BATTERY CHARGER



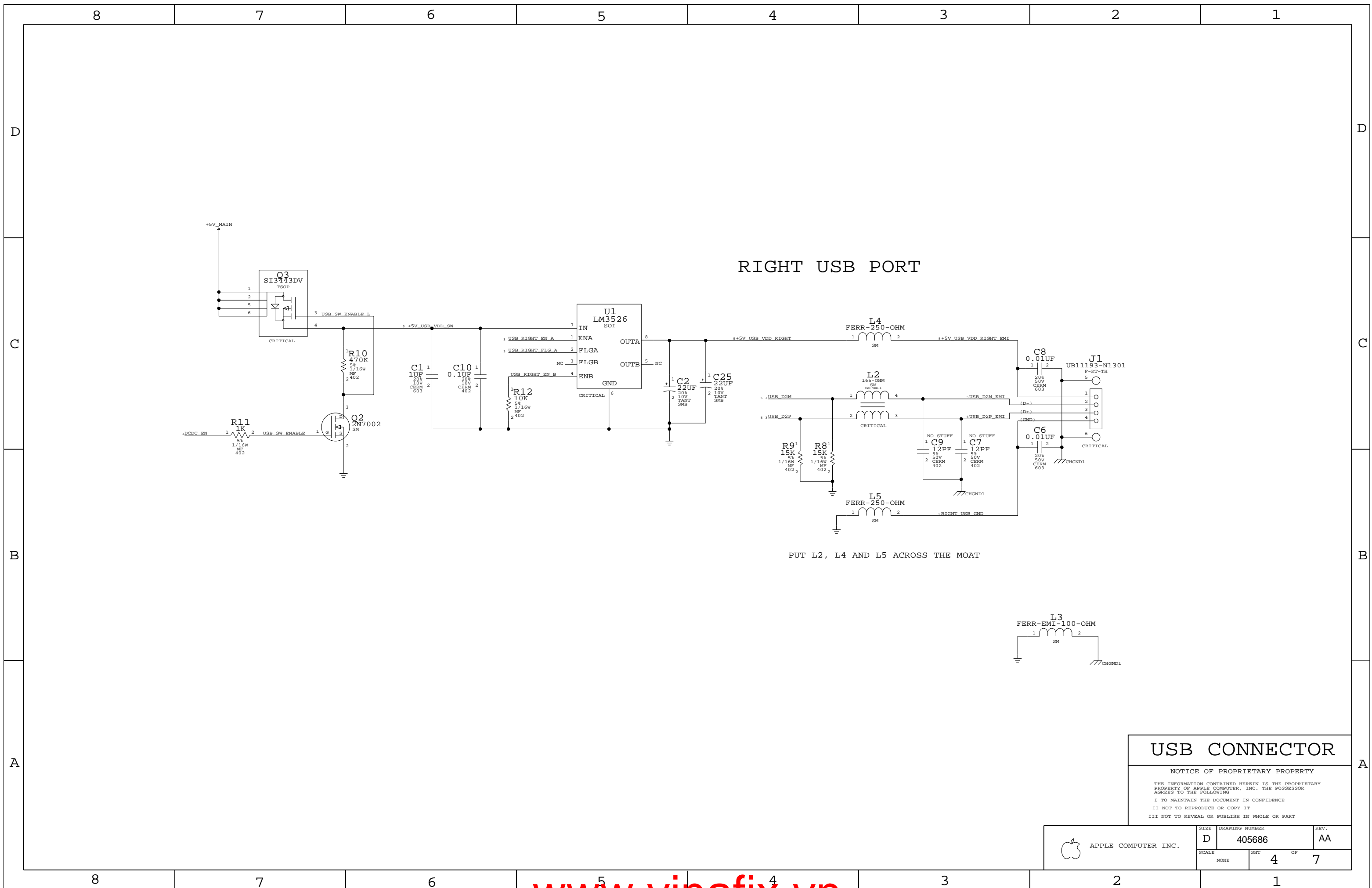
$I(REF) = 1.182V / (R7 + R5) = 0.799\mu A$
 Hysteresis band voltage (VHB) = $2 * I(REF) * R7 = 77.9mV$
 Both inputs are compared to REF - Hysteresis voltage ($1.182V \pm 0.5 * VHB$)



BACK UP BATTERY

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	D	405686	AA
SCALE	SHT	OF	
NONE	3	7	



RIGHT USB PORT

PUT L2, L4 AND L5 ACROSS THE MOAT

USB CONNECTOR

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	D	405686	AA
SCALE	SHT 4 OF 7		
NONE			

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Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR	MATCHED_DELAY
USB	USB_D2M	USB_D2	USB_D2:J2.5:L2.1:200
	USB_D2P	USB_D2	USB_D2:J2.6:L2.2:200
	USB_D2M_EMI	USB_D2_EMI	USB_D2_EMI:L2.4:J1.2:200
	USB_D2P_EMI	USB_D2_EMI	USB_D2_EMI:L2.3:J1.3:200

REVISION HISTORY

04/22/03 - DESIGN ORIGINATED FROM 051-6283
 04/23/03 - (PG. 3) CHANGED C12 TO LOW-PROFILE PART
 EVI 04/28/03 - (PG. 4) REPLACED R6 & R7 WITH 250-OHM 2A FERRITES (TABLE ITEM)
 04/29/03 - (PG. 4) CHANGED R6 & R7 TO L4 & L5 (PAD CHANGE FOR FERRITES)
 07/24/03 - PRODUCTION RELEASE

Power Signals

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH
BATTERY	24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	14V_PBUS	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	PBUS_BB_IN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	PBUS_SR2	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	PBUS_SR1	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	PBUS_BB_SW	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	+V_BBATT	VOLTAGE=4.2V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	+V_BBATT_RAW	VOLTAGE=4.2V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	BBATT_VSS	VOLTAGE=0V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	BBATT_VSS_SW	VOLTAGE=0V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
MAX1879	MAX1879_ADJ	VOLTAGE=1.4V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10
	BBATT_INPVT_DIV_L	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
S8241	PROT_D0	VOLTAGE=4.2V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10
	PROT_C0	VOLTAGE=4.2V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10
MAX933	9_12V_DET	VOLTAGE=1.2V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10
	3_28V_DET	VOLTAGE=1.2V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10
	BOOST_ENABLE	VOLTAGE=4.2V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10
	BBATT_DISCHRG_ENABLE	VOLTAGE=4.2V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10
LT1613	BBATT_OUT	VOLTAGE=4.2V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	BBATT_BOOST	VOLTAGE=6.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	BOOST_OUT	VOLTAGE=6.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	LT1613_FB	VOLTAGE=1.3V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10
USB	LT1613_FB_RC	VOLTAGE=1.3V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10
	+5V_USB_VDD_SW	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	+5V_USB_VDD_RIGHT	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	+5V_USB_VDD_RIGHT_EMI	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	RIGHT_USB_GND	VOLTAGE=0V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	GND	VOLTAGE=0V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10

SIGNAL CONSTRAINTS

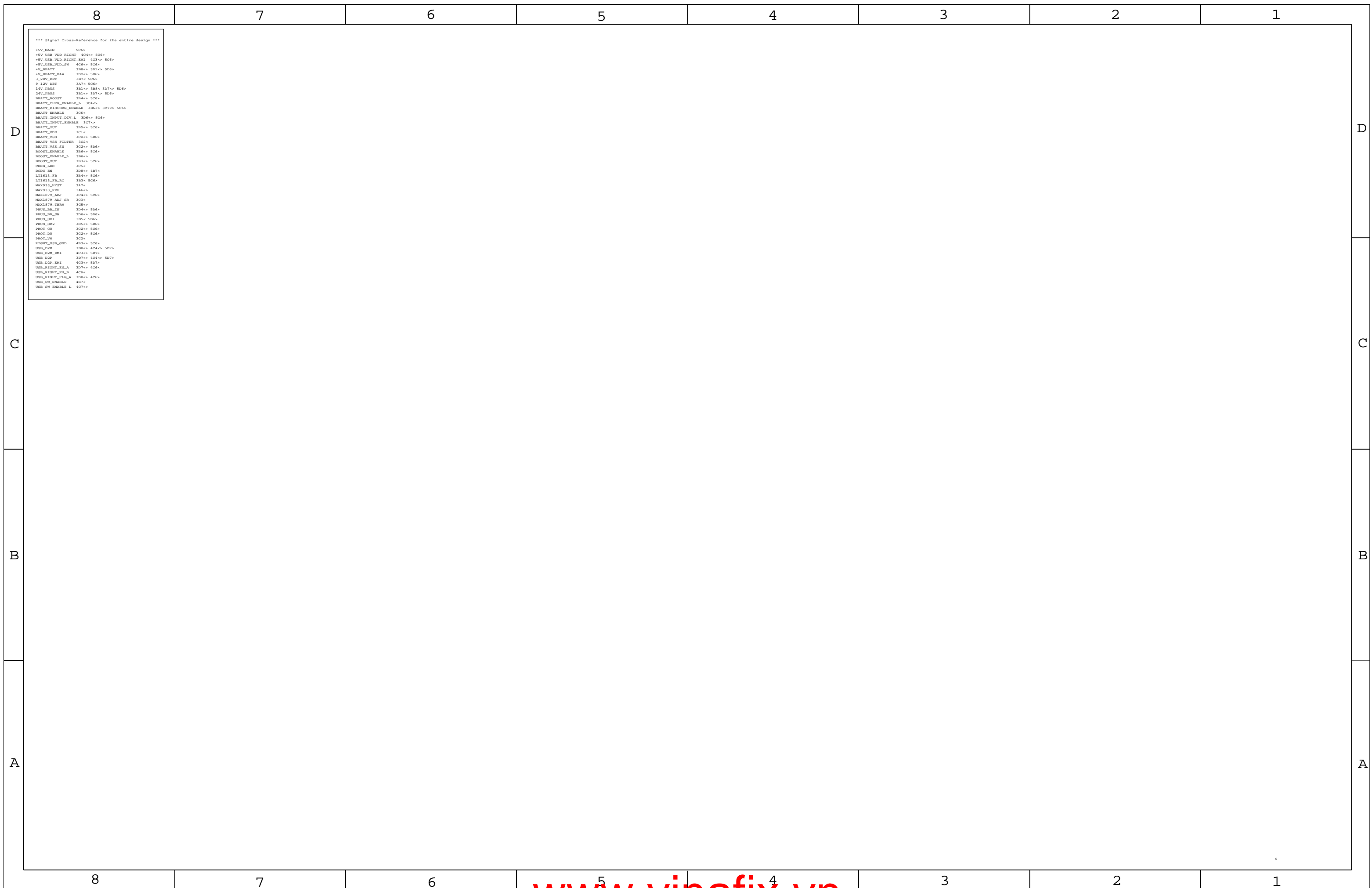
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SIZE	DRAWING NUMBER	REV.
D	405686	AA
SCALE	SHT	OF
NONE	5	7



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*** Signal Cross-Reference for the entire design ***
+SV_MAIN 506>
+SV_USB_VDD_RIGHT 404<> 506>
+SV_USB_VDD_RIGHT_BMI 403<> 506>
+SV_USB_VDD_SW 406<> 506>
+V_BBATT 386<> 302<> 506>
+V_BBATT_RAM 302<> 506>
3_2FV_DET 387<> 506>
6_13V_DET 3A7<> 506>
14V_PBUS 381<> 388< 3D7<> 506>
24V_PBUS 381<> 3D7<> 506>
BBATT_BOOST 384<> 506>
BBATT_CHRG_ENABLE_L 3C4<>
BBATT_DISCHRG_ENABLE 386<> 3C7<> 506>
BBATT_ENABLE 3C6<>
BBATT_INPUT_DIV_L 3D6<> 506>
BBATT_OUT 385<> 506>
BBATT_VDD 3C1<>
BBATT_VSS_FILTER 3C2<>
BBATT_VSS_SW 3C2<> 506>
BOOST_ENABLE 386<> 506>
BOOST_ENABLE_L 386<>
BOOST_OUT 383<> 506>
CHRG_LED 3C5<>
COSC_BH 3D8<> 487<
LT1613_FB 384<> 506>
LT1613_FB_IC 383<> 506>
MAX933_BYP 3A7<>
MAX933_BEP 3A6<>
MAX1879_ADJ 3C5<> 506>
MAX1879_ADJ_SR 3C3<>
MAX1879_THERM 3C5<>
PWR0_BH_IN 3D4<> 506>
PWR0_BH_SW 3D6<> 506>
PWR0_SH1 3D6<> 506>
PWR0_SH2 3D5<> 506>
PWR0_CD 3C2<> 506>
PWR0_D0 3C2<> 506>
PWR0_IN 3C2<>
RIGHT_USB_GND 483<> 506>
USB_D2M 3D8<> 404<> 5D7>
USB_D2M_BMI 403<> 5D7>
USB_D2P 3D7<> 404<> 5D7>
USB_D2P_BMI 403<> 5D7>
USB_RIGHT_EN_A 3D7<> 406<>
USB_RIGHT_EN_B 406<>
USB_RIGHT_FL2_A 3D8<> 406>
USB_SW_ENABLE 487<
USB_SW_ENABLE_L 4C7<>

```

