

8

7

6

5

4

3

2

1

- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
02		384356	ENGINEERING RELEASED	06/03/05	?

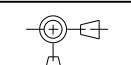
BOZEMAN

EVT

PDF	CSA	CONTENTS	SYNC MASTER	DATE
1	1	Table Of Contents	N/A	N/A
2	2	Board Information	N/A	N/A
3	3	System Block Diagram	MARIAS	06/03/2005
4	4	Power Block Diagram	MARIAS	06/03/2005
5	5	Revision History	N/A	N/A
6	6	Q41C Pin Swaps	N/A	N/A
7	7	Functional Test Points	MARIAS	06/03/2005
8	8	I2C Connections	MARIAS	06/03/2005
9	9	JTAG Connections	MARIAS	06/03/2005
10	10	Power Synonyms	MARIAS	06/03/2005
11	11	Signal Synonyms	MARIAS	06/03/2005
12	12	Power Inputs	MARIAS	06/03/2005
13	13	Battery Charger	MARIAS	06/03/2005
14	14	12.8V PBUS/PMU Supplies	MARIAS	06/03/2005
15	15	5V/3.3V Supplies	MARIAS	06/03/2005
16	16	1.8V/1.5V Supplies	MARIAS	06/03/2005
17	17	2.5V Supply	MARIAS	06/03/2005
18	19	Vesta Power & Misc	MARIAS	06/03/2005
19	21	I2 Power	MARIAS	06/03/2005
20	22	I2 Power Supplies	MARIAS	06/03/2005
21	23	I2 Supplemental	MARIAS	06/03/2005
22	24	I2 Miscellaneous	MARIAS	06/03/2005
23	25	PCI Clock Buffer	MARIAS	06/03/2005
24	26	LEDs/Reset/Debug	MARIAS	06/03/2005
25	27	Power Management Unit (PMU05)	MARIAS	06/03/2005
26	29	Power Sequencing	MARIAS	06/03/2005
27	30	Fan Controller	MARIAS	06/03/2005
28	31	ALS Support	MARIAS	06/03/2005
29	32	Sudden Motion Sensor	MARIAS	06/03/2005
30	33	Q41C Internal I/O I	N/A	N/A
31	34	Q41C Internal I/O II	N/A	N/A
32	35	I2 Processor Interface	MARIAS	06/03/2005
33	36	A8 MaxBus (CPU0)	MARIAS	06/03/2005
34	37	A8 Configuration Straps	MARIAS	06/03/2005
35	38	A8 Power (CPU0)	MARIAS	06/03/2005
36	39	CPU VCore Supply	MARIAS	06/03/2005
37	46	CPU AVDD Supply	MARIAS	06/03/2005
38	47	I2 Memory Interface	MARIAS	06/03/2005
39	48	Memory Series Termination	MARIAS-NDIFF	N/A
40	50	DDR2 SO-DIMM Slot A	MARIAS-MDIFF	N/A

PDF	CSA	CONTENTS	SYNC MASTER	DATE
41	52	DDR2 SO-DIMM Slot B	MARIAS-MDIFF	N/A
42	55	M11 Frame Buffer Constraints	MARIAS	06/03/2005
43	56	I2 AGP Interface	MARIAS	06/03/2005
44	57	GPU (M11) AGP Interface	MARIAS	06/03/2005
45	58	GPU VCore Supply	MARIAS	06/03/2005
46	59	GPU (M11) Core Power	MARIAS	06/03/2005
47	60	GPU (M11) I/O Power	MARIAS	06/03/2005
48	61	GPU (M11) Frame Buffer I/F	MARIAS	06/03/2005
49	62	GPU Frame Buffer A	MARIAS	06/03/2005
50	63	GPU Frame Buffer B	MARIAS	06/03/2005
51	64	GPU (M11) GPIOs/Straps	MARIAS	06/03/2005
52	65	GPU (M11) Clocks/Misc	MARIAS	06/03/2005
53	66	GPU (M11) DVI/DAC Outputs	MARIAS	06/03/2005
54	67	Lower TMDS Transmitter	MARIAS	06/03/2005
55	68	Upper TMDS Transmitter	MARIAS	06/03/2005
56	69	Internal Display Conns	MARIAS	06/03/2005
57	70	External Display Conns	MARIAS-PDIFF	06/02/2005
58	71	BOOTROM	MARIAS	06/03/2005
59	72	I2 PCI Interface	MARIAS	06/03/2005
60	73	Q85 AIRPORT/BT CONN	MARIAS-MDIFF	N/A
61	74	Cardbus	MARIAS	06/03/2005
62	75	NEC USB2	MARIAS	06/03/2005
63	81	I2 UATA Interface	MARIAS	06/03/2005
64	82	HDD/ODD Connectors	MARIAS-PDIFF	06/02/2005
65	84	I2 Ethernet Interface	MARIAS	06/03/2005
66	85	Vesta Ethernet PHY	MARIAS	06/03/2005
67	86	Ethernet Connector	N/A	N/A
68	88	I2 FireWire Interface	MARIAS	06/03/2005
69	89	Vesta FireWire PHY	MARIAS	06/03/2005
70	90	FireWire Ports	MARIAS-PDIFF	06/02/2005
71	91	FireWire Series Term	MARIAS	06/03/2005
72	92	I2 USB Interface	MARIAS	06/03/2005
73	93	NEC USB2 Interface	MARIAS	06/03/2005
74	100	Audio Board Connector	N/A	N/A
75	110	Spacing & Physical Constraints	MARIAS	06/03/2005
76	111	Spacing & Physical Constraints 2	MARIAS	06/03/2005
77	112	Cross Reference Page		
78	113	Cross Reference Page		
79	114	Cross Reference Page		
80	115	Cross Reference Page		

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6839	1	SCHEM,BOZEMAN,Q41C	SCH1	
820-1810	1	PCBF,BOZEMAN,Q41C	PCB1	
826-4393	1	LBL,P/N LABEL,PCB,28MM x 6MM	[EEE:SYV]	VRAM_SAMSUNG
826-4393	1	LBL,P/N LABEL,PCB,28MM x 6MM	[EEE:TML]	VRAM_HYNIX

DIMENSIONS ARE IN MILLIMETERS		METRIC		Apple Computer Inc.	
XX :	_____	DRAPFER	/	DESIGN CK	/
X.XX :	_____	ENG APPD	/	MFG APPD	/
X.XXX :	_____	QA APPD	/	DESIGNER	/
ANGLES :	_____	RELEASE	/	SCALE	NONE
DO NOT SCALE DRAWING		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE D	
 THIRD ANGLE PROJECTION		DRAWING NUMBER		REV. 02	
		051-6839		SHT 1 OF 115	

Design-Specific Rules

TABLE_SPACING_RULE	STANDARD	DEFAULT	1MM	BGA_P1MM	1.25MM	0.1MM	12.5MM	15.0MM
TABLE_SPACING_RULE	STANDARD	=DEFAULT	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT
TABLE_SPACING_RULE	BGA_P1MM	10	*	0.10 MM	1.25 MM	0.1 MM	12.5 MM	15.0 MM
TABLE_SPACING_RULE	BGA_P2MM	20	*	0.20 MM	1.25 MM	0.1 MM	12.5 MM	15.0 MM
TABLE_SPACING_RULE	DEFAULT	*	*	0.1 MM	2.5 MM	0.15 MM	10.0 MM	15.0 MM

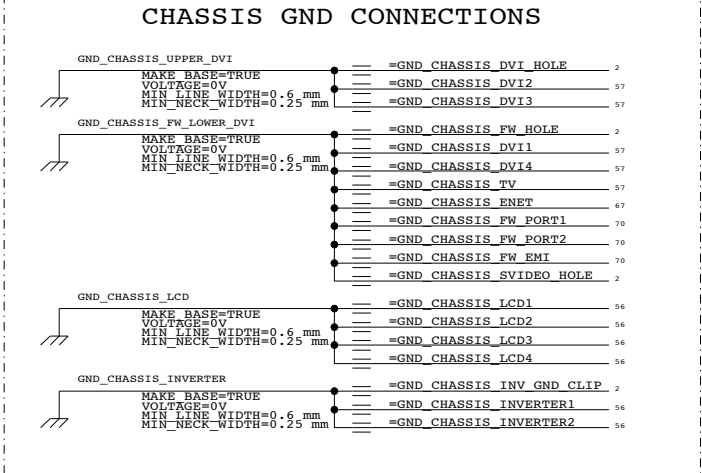
"1MM" area defined around BGAs to reduce DRCs caused by fan-out.
 "BGA_P2MM" rule ensures these critical signals do not fan-out routed next to any other signals.

TABLE_SPACING_RULE	90_OHM_DIFF	TOP,BOTTOM	2.5MM	0.200MM	2.5MM	1.0MM
TABLE_SPACING_RULE	90_OHM_DIFF	*	2.5 MM	0.200 MM	2.5 MM	1.0 MM
TABLE_PHYSICAL_RULE	90_OHM_DIFF	TOP,BOTTOM	Y	0.118 MM	0.1 MM	5 MM
TABLE_PHYSICAL_RULE	90_OHM_DIFF	*	Y	0.125 MM	0.1 MM	5 MM

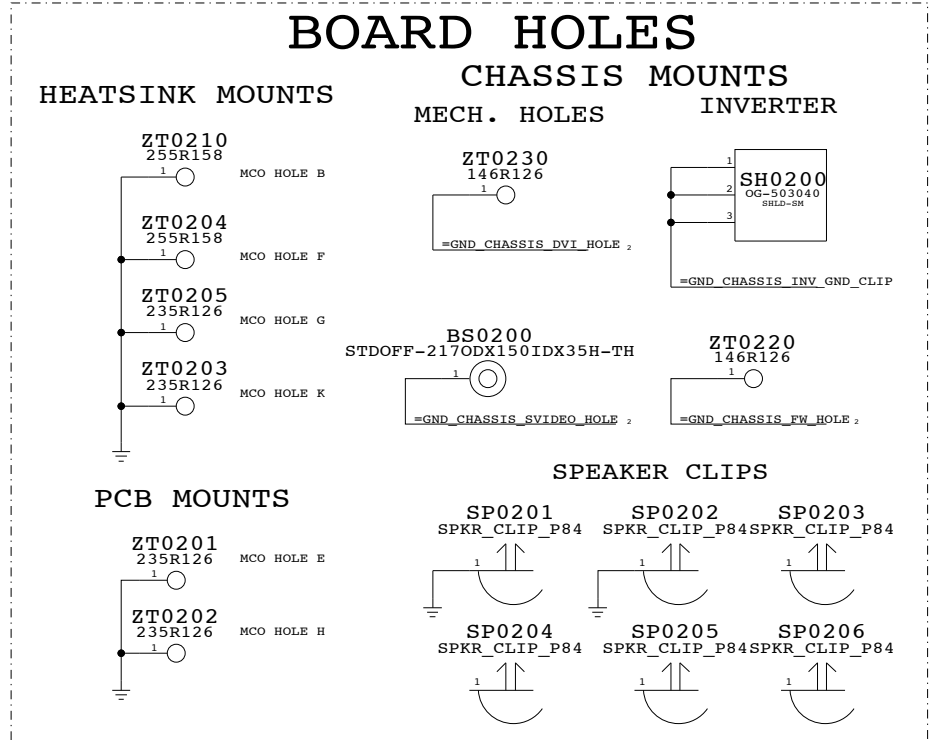
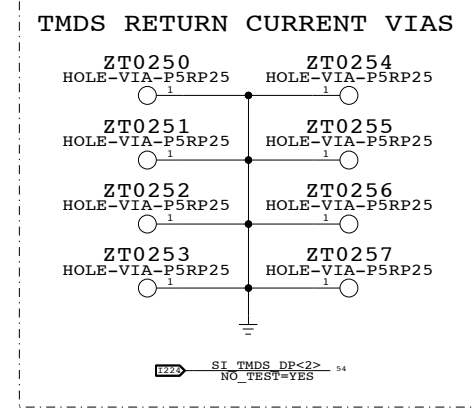
TABLE_SPACING_RULE	100_OHM_DIFF	TOP,BOTTOM	2.5MM	0.200MM	2.5MM	1.0MM
TABLE_SPACING_RULE	100_OHM_DIFF	*	2.5 MM	0.200 MM	2.5 MM	1.0 MM
TABLE_PHYSICAL_RULE	100_OHM_DIFF	TOP,BOTTOM	Y	0.092 MM	0.1 MM	5 MM
TABLE_PHYSICAL_RULE	100_OHM_DIFF	*	Y	0.100 MM	0.1 MM	5 MM

TABLE_SPACING_RULE	110_OHM_DIFF	TOP,BOTTOM	2.5MM	0.330MM	2.5MM	1.0MM
TABLE_SPACING_RULE	110_OHM_DIFF	*	2.5 MM	0.300 MM	2.5 MM	1.0 MM
TABLE_PHYSICAL_RULE	110_OHM_DIFF	TOP,BOTTOM	Y	0.080 MM	0.1 MM	5 MM
TABLE_PHYSICAL_RULE	110_OHM_DIFF	*	Y	0.085 MM	0.1 MM	5 MM

TABLE_SPACING_RULE	AGP	201	*	0.2MM			
TABLE_SPACING_RULE	AGP	201	*	0.2 MM			
TABLE_SPACING_RULE	AGP_STB	251	*	0.25 MM			
TABLE_SPACING_RULE	VGA	151	*	0.15 MM	=DEFAULT	=DEFAULT	=DEFAULT
TABLE_SPACING_RULE	TV	151	*	0.15 MM	=DEFAULT	=DEFAULT	=DEFAULT
TABLE_PHYSICAL_RULE	VGA	*	=60_OHM_SE	=60_OHM_SE	=60_OHM_SE	=60_OHM_SE	
TABLE_PHYSICAL_RULE	TV	*	=60_OHM_SE	=60_OHM_SE	=60_OHM_SE	=60_OHM_SE	



TABLE_PHYSICAL_RULE	60_OHM_SE	*	Y	0.076MM	=50_OHM_SE	=50_OHM_SE
TABLE_PHYSICAL_RULE	60_OHM_SE	*	Y	0.076 MM	=50_OHM_SE	=50_OHM_SE
TABLE_SPACING_RULE	50_OHM_SE	*		2.5 MM	0.125 MM	2.5 MM
TABLE_PHYSICAL_RULE	50_OHM_SE	*	Y	0.100 MM	0.100 MM	1.25 MM



BOARD STACK-UP AND CONSTRUCTION

Layer	Material	Thickness
1	PREPREG	SIGNAL (1/2 OZ + COPPER PLATING)
2	CORE	GROUND (1/2 OZ)
3	PREPREG	SIGNAL (1/2 OZ)
4	CORE	SIGNAL (1/2 OZ)
5	PREPREG	GROUND (1/2 OZ)
6	CORE	CUT POWER PLANE (1 OZ)
7	PREPREG	CUT POWER PLANE (1 OZ)
8	CORE	GROUND (1/2 OZ)
9	PREPREG	SIGNAL (1/2 OZ)
10	CORE	SIGNAL (1/2 OZ)
11	PREPREG	GROUND (1/2 OZ)
12	PREPREG	SIGNAL (1/2 OZ + COPPER PLATING)

BOM OPTIONS

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7017	PCBA,MLB,BESTMHZ,BOZEMAN,VRAM_S,Q41C	COMMON,ALTERNATE,VRAM_SAMSUNG,gQ41C,gCommon
630-7186	PCBA,MLB,BESTMHZ,BOZEMAN,VRAM_H,Q41C	COMMON,ALTERNATE,VRAM_HYNIX,gQ41C,gCommon

BOM GROUP	BOM OPTIONS
gCommon	5V_HD_LOGIC, BACKUP_BATT, CPU_A7PM, I2_FW_BETA, I2_MAXBUS_50OHM, MAXBUS_1V8, gCommon1
gCommon1	MMM_ACCEL_KIONIX, GPU_PWRPLAY, GPU_SS, GPU_LVDDR_2V8, GPU_MEMIO_1V8, gCommon2
gCommon2	I2_REV1_NOT, I2_MAXBUS_FBCLK_MATCHED, I2_AGP_FBCLK_MATCHED, I2_PCI_FBCLK_MATCHED, gCommon3
gCommon3	CPU_VCORE_3STATES, I2_MAXBUS_166MHZ, CPU0_BUSRATIO_10.0X, I2VCORE_1V5, I2VCORE_BURST, gCommon4
gCommon4	VESTA_PORT2_DISABLE, DVO_1V8, TMD5_DUAL, VCORE_OFFSET, VCORE_OFFSET_SW, gUSB
gUSB	USB2_NEG, USB1P1_I2
gQ41C	Q41C_PARTS, A7PM_1P67_LGA, BOOTROM_PROG, PMU_PROG, DEVELOPMENT, MAXBUS_TBEN_SYNC

Module Components

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S0325	1	IC, ASIC, I2, REV1.1, NB/SB, 974 BGA	U2100	CRITICAL	
337S3135	1	IC, PMU05, BLANK, QFP	U2700	CRITICAL	PMU_BLANK
341S1772	1	IC, PMU05, Vxxx, QFP	U2700	CRITICAL	PMU_PROG
337S3181	1	IC, A7PM, R1.5, 1.67GHZ, LGA, 1.28V, 25W, 85C	U3600	CRITICAL	A7PM_1P67_LGA
337S3077	1	IC, A8, xxxGHZ	U3600	CRITICAL	CPU_A8
338S0252	1	IC, GPU, M11P	U5700	CRITICAL	
335S0088	1	BOOTROM, BLANK	U7100	CRITICAL	BOOTROM_BLANK
341S1739	1	IC, BOOTROM, B, Q41C	U7100	CRITICAL	BOOTROM_PROG
343S0356	1	IC, ASIC, VESTA, V1.3, LF	U8500	CRITICAL	
333S0317	4	IC, GDDR SDRAM, 2MX32X4, 300MHZ, LF FBGA144	U6200, U6250, U6300, U6350	CRITICAL	VRAM_SAMSUNG
333S0314	4	IC, GDDR SDRAM, 2MX32X4, 300MHZ, LF FBGA144	U6200, U6250, U6300, U6350	CRITICAL	VRAM_HYNIX

Board Information

SYNC_MASTER=N/A SYNC_DATE=N/A

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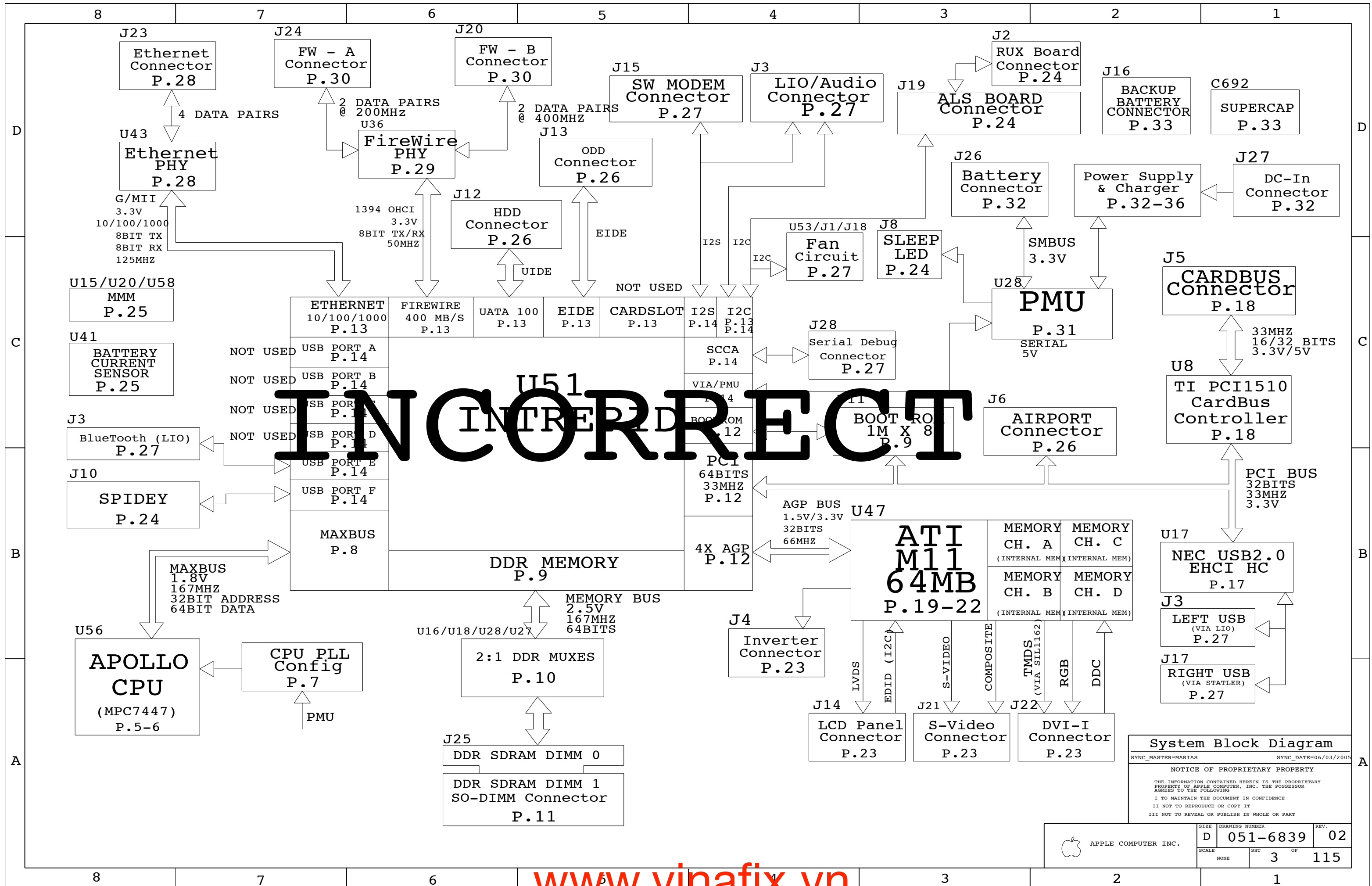
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APPLE COMPUTER INC.

SIZE: D 051-6839 02

SCALE: NONE 2 OF 115

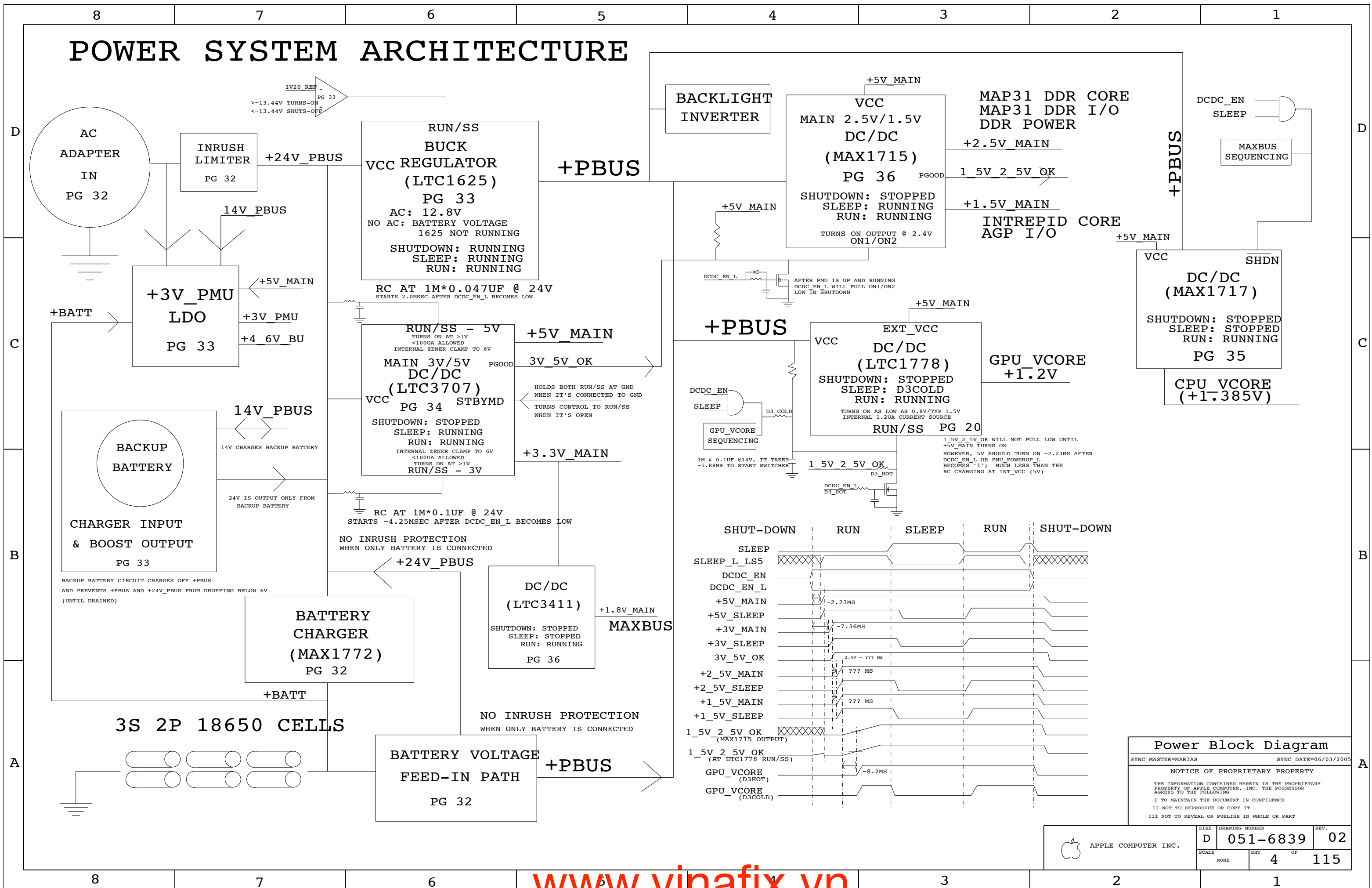


INCORRECT

System Block Diagram
 SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6839	REV. 02
	SCALE NONE	SHEET 3	OF 115

POWER SYSTEM ARCHITECTURE



Power Block Diagram
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6839	02
SCALE	SHT		OF
NONE	4		115

REVISION HISTORY

PROTO

- 04/05/2005 - Beginning revision history
- Sync'd FB pin swaps from 051-5838
- Pinned out audio connector per flex cable
- Pinned out fire USB/ATA connector per flex cable
- 04/07/2005 - Moved modem connector to non-shared page
- Updated chassis ground connections
- Pin swapped DDR2 according to layout
- 04/11/2005 - Changed bulk caps to XSR (CA050, CA051)
- 04/12/2005 - Updated wireless connector pinout according to flex
- Implemented more DDR2 pin swaps
- Implemented pin swaps on FW data lines
- Added RAM DQS pull-downs
- Corrected mosF line and neck width properties
- 04/14/2005 - Switched GPU to M11
- 04/15/2005 - Added CPU Vcore mux circuit
- Added NO TEST property to buses between JTAG enabled devices
- 04/19/2005 - Pinned FB 1/2 for M11
- Corrected ENET power rail to PWRON instead of RUN (Wake-on-LAN)
- 04/20/2005 - Corrected Vesta reset and Ethernet LOWPWR circuits
- Changed R5880 to 6.34K to take GPU Vcore to 1.3V/1.05V
- Added page 6 and modified pages 11,35,81 for design specific pin swaps
- Separated GPU MVREF into two dividers
- 04/26/2005 - Added 5 vias for TMD5 return current
- Added LVDS electrical constraint set properties
- 04/27/2005 - Added NO TEST property to SI TMD5 DP<2> (no room for TP)
- Changed MIN NECK WIDTH property on TMD5 power rails to 0.2 mm
- Changed gender of debug connector
- Removed 06867 due to MCO violation
- 04/29/2005 - Schematic released as REV 01 for PROTO

EVT

- 05/04/2005 - Added SYNONYMS to allow DVO and USB pulldown pinswaps
- 05/09/2005 - Added missing pullup to SYS LID OPEN
- Added missing pull-down to Vesta LPWR 1394
- 05/16/2005 - Lead-free resistor replacement on page 86
- Various lead-free replacements
- 05/17/2005 - Added Hynix VRAM option and PCBA
- 05/25/2005 - Added 2 0.1uF caps to VGA sync buffers
- Added NEC USB2 controller and PCI clock buffer
- Various lead-free replacements
- 05/26/2005 - Added pullup to BATT0 DET
- Removed SWF PIC microcontroller
- 05/31/2005 - Added 2 0.1uF caps to GPU Vcore output
- Corrected USB diff pair and spacing/physical rules on ports
- 06/01/2005 - Corrected caps on firewire vr rail to 50V
- Various lead-free replacements

02

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	D	051-6839	02
SCALE		SHT	OF
NONE		5	115

	8	7	6	5	4	3	2	1													
D	<h3>I2S Series Rs</h3> <pre> MAKE_BASE=TRUE 22 I2S0_SB_TO_DEV.DTO_R == RP1150P1 11 11 ==RP1150P8 == I2S0_SB_TO_DEV.DTO 7 74 MAKE_BASE=TRUE MAKE_BASE=TRUE 22 I2S0_BITCLK_R == RP1150P2 11 11 ==RP1150P7 == I2S0_BITCLK 7 74 MAKE_BASE=TRUE MAKE_BASE=TRUE 22 I2S0_MCLK_R == RP1150P3 11 11 ==RP1150P6 == I2S0_MCLK 7 74 MAKE_BASE=TRUE MAKE_BASE=TRUE 22 I2S0_SYNC_R == RP1150P4 11 11 ==RP1150P5 == I2S0_SYNC 7 74 MAKE_BASE=TRUE MAKE_BASE=TRUE 22 I2S1_SB_TO_DEV.DTO_R == RP1151P1 11 11 ==RP1151P8 == I2S1_SB_TO_DEV.DTO 30 MAKE_BASE=TRUE MAKE_BASE=TRUE 22 I2S1_SYNC_R == RP1151P2 11 11 ==RP1151P7 == I2S1_SYNC 30 MAKE_BASE=TRUE MAKE_BASE=TRUE 22 I2S1_MCLK_R == RP1151P3 11 11 ==RP1151P6 == I2S1_MCLK 30 MAKE_BASE=TRUE MAKE_BASE=TRUE 22 I2S1_BITCLK_R == RP1151P4 11 11 ==RP1151P5 == I2S1_BITCLK 30 MAKE_BASE=TRUE </pre>			<h3>Lower DVO Series Rs</h3> <pre> MAKE_BASE=TRUE 53 GPU_DVOD_R<0> == RP6720P1 54 54 ==RP6720P8 == GPU_DVOD<0> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<1> == RP6720P2 54 54 ==RP6720P7 == GPU_DVOD<1> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<2> == RP6720P3 54 54 ==RP6720P6 == GPU_DVOD<2> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<3> == RP6720P4 54 54 ==RP6720P5 == GPU_DVOD<3> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<11> == RP6721P1 54 54 ==RP6721P8 == GPU_DVOD<11> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<10> == RP6721P2 54 54 ==RP6721P7 == GPU_DVOD<10> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<9> == RP6721P3 54 54 ==RP6721P6 == GPU_DVOD<9> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<8> == RP6721P4 54 54 ==RP6721P5 == GPU_DVOD<8> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<6> == RP6722P1 54 54 ==RP6722P8 == GPU_DVOD<6> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<4> == RP6722P2 54 54 ==RP6722P7 == GPU_DVOD<4> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<7> == RP6722P3 54 54 ==RP6722P6 == GPU_DVOD<7> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<5> == RP6722P4 54 54 ==RP6722P5 == GPU_DVOD<5> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVO_HSYNC_R == RP6723P1 54 54 ==RP6723P8 == GPU_DVO_HSYNC 54 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVO_VSYNC_R == RP6723P2 54 54 ==RP6723P7 == GPU_DVO_VSYNC 54 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVO_DE_R == RP6723P3 54 54 ==RP6723P6 == GPU_DVO_DE 54 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVO_CLKP_R == RP6723P4 54 54 ==RP6723P5 == GPU_DVO_CLKP 54 55 MAKE_BASE=TRUE </pre>			D														
C	<h3>UATA Series Rs</h3> <pre> MAKE_BASE=TRUE 63 UATA_DD_R<12> == RP8150P1 63 63 ==RP8150P8 == UATA_DD<12> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_CS0_L_R == RP8150P2 63 63 ==RP8150P7 == UATA_CS0_L 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<14> == RP8150P3 63 63 ==RP8150P6 == UATA_DD<14> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<11> == RP8150P4 63 63 ==RP8150P5 == UATA_DD<11> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<7> == RP8151P1 63 63 ==RP8151P8 == UATA_DD<7> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<2> == RP8151P2 63 63 ==RP8151P7 == UATA_DD<2> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<3> == RP8151P3 63 63 ==RP8151P6 == UATA_DD<3> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<15> == RP8151P4 63 63 ==RP8151P5 == UATA_DD<15> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<9> == RP8152P1 63 63 ==RP8152P8 == UATA_DD<9> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<4> == RP8152P2 63 63 ==RP8152P7 == UATA_DD<4> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<6> == RP8152P3 63 63 ==RP8152P6 == UATA_DD<6> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<5> == RP8152P4 63 63 ==RP8152P5 == UATA_DD<5> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DA_R<2> == RP8153P1 63 63 ==RP8153P8 == UATA_DA<2> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<8> == RP8153P2 63 63 ==RP8153P7 == UATA_DD<8> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<10> == RP8153P3 63 63 ==RP8153P6 == UATA_DD<10> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DA_R<0> == RP8153P4 63 63 ==RP8153P5 == UATA_DA<0> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<13> == RP8154P1 63 63 ==RP8154P8 == UATA_DD<13> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<0> == RP8154P2 63 63 ==RP8154P7 == UATA_DD<0> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<1> == RP8154P3 63 63 ==RP8154P6 == UATA_DD<1> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DA_R<1> == RP8154P4 63 63 ==RP8154P5 == UATA_DA<1> 7 63 64 MAKE_BASE=TRUE </pre>			<h3>Upper DVO Series Rs</h3> <pre> MAKE_BASE=TRUE 53 GPU_DVOD_R<13> == RP6821P1 55 55 ==RP6821P8 == GPU_DVOD<13> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<12> == RP6821P2 55 55 ==RP6821P7 == GPU_DVOD<12> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<14> == RP6821P3 55 55 ==RP6821P6 == GPU_DVOD<14> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<15> == RP6821P4 55 55 ==RP6821P5 == GPU_DVOD<15> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<18> == RP6822P1 55 55 ==RP6822P8 == GPU_DVOD<18> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<19> == RP6822P2 55 55 ==RP6822P7 == GPU_DVOD<19> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<16> == RP6822P3 55 55 ==RP6822P6 == GPU_DVOD<16> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<17> == RP6822P4 55 55 ==RP6822P5 == GPU_DVOD<17> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<21> == RP6823P1 55 55 ==RP6823P8 == GPU_DVOD<21> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<20> == RP6823P2 55 55 ==RP6823P7 == GPU_DVOD<20> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<23> == RP6823P3 55 55 ==RP6823P6 == GPU_DVOD<23> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<22> == RP6823P4 55 55 ==RP6823P5 == GPU_DVOD<22> 55 MAKE_BASE=TRUE </pre>			C														
B	<h3>MAXBUS Pullups</h3> <pre> MAKE_BASE=TRUE 33 MAXBUS_TS_L == RP3510P1 32 32 MAKE_BASE=TRUE 32 MAXBUS_CPU1_BG_L == RP3510P2 32 32 MAKE_BASE=TRUE 33 MAXBUS_CPU0_DBG_L == RP3510P3 32 32 MAKE_BASE=TRUE 32 MAXBUS_TBN_I2 == RP3510P4 32 32 MAKE_BASE=TRUE 33 MAXBUS_CPU0_BG_L == RP3511P1 32 32 MAKE_BASE=TRUE 32 MAXBUS_CPU1_HIT_L == RP3511P2 32 32 MAKE_BASE=TRUE 33 MAXBUS_CPU0_HIT_L == RP3511P3 32 32 MAKE_BASE=TRUE 32 MAXBUS_CPU0_BR_L == RP3511P4 32 32 MAKE_BASE=TRUE 32 MAXBUS_CPU1_BR_L == RP3512P1 32 32 MAKE_BASE=TRUE 33 MAXBUS_TA_L == RP3512P2 32 32 MAKE_BASE=TRUE 34 MAXBUS_CPU0_INT_L == RP3512P3 32 32 MAKE_BASE=TRUE 32 MAXBUS_CPU1_INT_L == RP3512P4 32 32 MAKE_BASE=TRUE 33 MAXBUS_CPU0_DRDY_L == RP3513P2 32 32 MAKE_BASE=TRUE 32 MAXBUS_CPU1_DRDY_L == RP3513P3 32 32 MAKE_BASE=TRUE 33 MAXBUS_AACK_L == RP3513P4 32 32 MAKE_BASE=TRUE 33 MAXBUS_ARTRY_L == RP3514P1 32 32 MAKE_BASE=TRUE 32 MAXBUS_CPU1_DBG_L == RP3514P2 32 32 MAKE_BASE=TRUE 33 MAXBUS_TEA_L == RP3514P3 32 32 </pre>		<h3>AGP Pullups</h3> <pre> MAKE_BASE=TRUE 44 AGP_TRDY_L == RP5610P1 43 43 MAKE_BASE=TRUE 44 AGP_IRDY_L == RP5610P2 43 43 MAKE_BASE=TRUE 44 AGP_REQ_L == RP5610P3 43 43 MAKE_BASE=TRUE 44 AGP_RBF_L == RP5610P4 43 43 MAKE_BASE=TRUE 44 AGP_FRAME_L == RP5611P1 43 43 MAKE_BASE=TRUE 44 AGP_DEVSEL_L == RP5611P2 43 43 MAKE_BASE=TRUE 44 AGP_STOP_L == RP5611P3 43 43 MAKE_BASE=TRUE 44 AGP_GNT_L == RP5611P4 43 43 </pre>		<h3>USB Pulldowns</h3> <pre> 72 ==RP9210P8 == USB2_I2_LEFT_PORT_P 11 MAKE_BASE=TRUE 72 ==RP9210P7 == USB2_I2_LEFT_PORT_N 11 MAKE_BASE=TRUE 72 ==RP9210P6 == USB2_I2_P<1> 72 MAKE_BASE=TRUE 72 ==RP9210P5 == USB2_I2_N<1> 72 MAKE_BASE=TRUE 72 ==RP9211P8 == USB2_I2_RIGHT_PORT_P 11 MAKE_BASE=TRUE 72 ==RP9211P7 == USB2_I2_RIGHT_PORT_N 11 MAKE_BASE=TRUE 72 ==RP9211P6 == USB2_I2_P<3> 72 MAKE_BASE=TRUE 72 ==RP9211P5 == USB2_I2_N<3> 72 MAKE_BASE=TRUE 72 ==RP9212P8 == USB_I2_BT_P 11 MAKE_BASE=TRUE 72 ==RP9212P7 == USB_I2_BT_N 11 MAKE_BASE=TRUE 72 ==RP9212P6 == USB_I2_TPAD_P 11 MAKE_BASE=TRUE 72 ==RP9212P5 == USB_I2_TPAD_N 11 MAKE_BASE=TRUE 72 ==RP9300P8 == USB2_NEC_LEFT_PORT_P 11 MAKE_BASE=TRUE 72 ==RP9300P7 == USB2_NEC_LEFT_PORT_N 11 MAKE_BASE=TRUE 72 ==RP9300P6 == USB2_NEC_RIGHT_PORT_N 11 MAKE_BASE=TRUE 72 ==RP9300P5 == USB2_NEC_RIGHT_PORT_P 11 MAKE_BASE=TRUE 72 ==RP9301P8 == USB_NEC_BT_P 11 MAKE_BASE=TRUE 72 ==RP9301P7 == USB_NEC_BT_N 11 MAKE_BASE=TRUE 72 ==RP9301P6 == USB_NEC_TPAD_N 11 MAKE_BASE=TRUE 72 ==RP9301P5 == USB_NEC_TPAD_P 11 MAKE_BASE=TRUE </pre>		B														
A	<h3>FW Series Rs</h3> <pre> MAKE_BASE=TRUE 68 9 FW_D_R<3> == RP9100P1 71 71 ==RP9100P8 == FW_D<3> 9 69 MAKE_BASE=TRUE MAKE_BASE=TRUE 68 9 FW_D_R<1> == RP9100P2 71 71 ==RP9100P7 == FW_D<1> 9 69 MAKE_BASE=TRUE MAKE_BASE=TRUE 68 9 FW_D_R<0> == RP9100P3 71 71 ==RP9100P6 == FW_D<0> 9 69 MAKE_BASE=TRUE MAKE_BASE=TRUE 68 9 FW_D_R<2> == RP9100P4 71 71 ==RP9100P5 == FW_D<2> 9 69 MAKE_BASE=TRUE MAKE_BASE=TRUE 68 9 FW_D_R<7> == RP9101P1 71 71 ==RP9101P8 == FW_D<7> 9 69 MAKE_BASE=TRUE MAKE_BASE=TRUE 68 9 FW_D_R<5> == RP9101P2 71 71 ==RP9101P7 == FW_D<5> 9 69 MAKE_BASE=TRUE MAKE_BASE=TRUE 68 9 FW_D_R<6> == RP9101P3 71 71 ==RP9101P6 == FW_D<6> 9 69 MAKE_BASE=TRUE MAKE_BASE=TRUE 68 9 FW_D_R<4> == RP9101P4 71 71 ==RP9101P5 == FW_D<4> 9 69 MAKE_BASE=TRUE </pre>			<h3>PCI Pullups</h3> <pre> MAKE_BASE=TRUE 11 PCI_AIRPORT_GNT_L == RP7250P1 59 59 MAKE_BASE=TRUE 60 59 PCI_TRDY_L == RP7250P2 59 59 MAKE_BASE=TRUE 60 59 PCI_IRDY_L == RP7250P3 59 59 MAKE_BASE=TRUE 60 59 PCI_STOP_L == RP7250P4 59 59 MAKE_BASE=TRUE 11 PCI_CBUS_REQ_L == RP7251P1 59 59 MAKE_BASE=TRUE 11 PCI_AIRPORT_REQ_L == RP7251P2 59 59 MAKE_BASE=TRUE 11 PCI_CBUS_GNT_L == RP7251P3 59 59 MAKE_BASE=TRUE 60 59 PCI_FRAME_L == RP7251P4 59 59 </pre>			A														
	<div style="text-align: center;"> <h2>Q41C Pin Swaps</h2> <p>SYNC_MASTER=N/A SYNC_DATE=N/A</p> <p style="text-align: center;">NOTICE OF PROPRIETARY PROPERTY</p> <p style="text-align: center;">THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</p> <p style="text-align: center;">I TO MAINTAIN THE DOCUMENT IN CONFIDENCE</p> <p style="text-align: center;">II NOT TO REPRODUCE OR COPY IT</p> <p style="text-align: center;">III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</p> </div>																				
	APPLE COMPUTER INC.		<table border="1"> <tr> <td>SIZE</td> <td>DRAWING NUMBER</td> <td>REV.</td> </tr> <tr> <td>D</td> <td>051-6839</td> <td>02</td> </tr> <tr> <td>SCALE</td> <td>SHT</td> <td>OF</td> </tr> <tr> <td>NONE</td> <td>6</td> <td>115</td> </tr> </table>	SIZE	DRAWING NUMBER	REV.	D	051-6839	02	SCALE	SHT	OF	NONE	6	115						
SIZE	DRAWING NUMBER	REV.																			
D	051-6839	02																			
SCALE	SHT	OF																			
NONE	6	115																			
	8	7	6	5	4	3	2	1													

Enhanced MAC-1 Test Coverage

Functional test points use a P6 pad placed on bottom side.

Category	Test Point	Pin	Function	Notes	
POWER	PP24V_ADAPTER	10	FUNC_TEST=YES	Place 2 TPs @ connector.	
	PP24V_ALL_PBUS	10	FUNC_TEST=YES		
	PP12V8_ALL_PBUSB	10	FUNC_TEST=YES	Place within 50 mm of power supply.	
	PPVCORE_RUN_GPU	10	FUNC_TEST=YES		
	PPVCORE_RUN_CPU	10	FUNC_TEST=YES		
	PP1V8_PWRON	10	FUNC_TEST=YES		
	PP2V5_PWRON	10	FUNC_TEST=YES	Place 5-10 GND TPs.	
	PP5V_PWRON	10	FUNC_TEST=YES		
	PP3V3_PWRON	10	FUNC_TEST=YES		
	PP5V_RUN	10	FUNC_TEST=YES		
	PP3V3_ALL	10	FUNC_TEST=YES		
	=FTP_GND	7 10	FUNC_TEST=YES		
	LVDS	LVDS_U0_P	53 56	FUNC_TEST=YES	Place within 25 mm of LVDS connector.
		LVDS_U0_N	53 56	FUNC_TEST=YES	
LVDS_U1_P		53 56	FUNC_TEST=YES		
LVDS_U1_N		53 56	FUNC_TEST=YES		
LVDS_U2_P		53 56	FUNC_TEST=YES		
LVDS_U2_N		53 56	FUNC_TEST=YES		
CLKLVDS_U_P		53 56	FUNC_TEST=YES		
CLKLVDS_U_N		53 56	FUNC_TEST=YES		
LVDS_L0_P		53 56	FUNC_TEST=YES		
LVDS_L0_N		53 56	FUNC_TEST=YES		
LVDS_L1_P		53 56	FUNC_TEST=YES		
LVDS_L1_N		53 56	FUNC_TEST=YES		
LVDS_L2_P		53 56	FUNC_TEST=YES		
LVDS_L2_N		53 56	FUNC_TEST=YES		
CLKLVDS_L_P		53 56	FUNC_TEST=YES		
CLKLVDS_L_N		53 56	FUNC_TEST=YES		
LVDS_DDC_CLK		51 56	FUNC_TEST=YES		
LVDS_DDC_DATA		51 56	FUNC_TEST=YES		
=PP3V3_DDC_LCD	10 56	FUNC_TEST=YES			
PP3V3_LCD_CONN	56	FUNC_TEST=YES			
INVERTER	PPBUS_INVERTER	56	FUNC_TEST=YES	Place within 25 mm of inverter connector.	
	PP5V_INV_SW	56	FUNC_TEST=YES		
	BRIGHT_PWM	56	FUNC_TEST=YES		
	GND_INVERTER	56	FUNC_TEST=YES		
UATA	=PP5V_RUN_ODD	10 64	FUNC_TEST=YES	Place within 50 mm of ODD/HDD connector.	
	=PP5V_RUN_HDD	10 64	FUNC_TEST=YES		
	PP3V3R5V_RUN_HDD_LOGIC	64	FUNC_TEST=YES		
	UATA_DD<15..0>	6 63 64	FUNC_TEST=YES		
	UATA_DMAR0	63 64	FUNC_TEST=YES		
	UATA_DSTROBE	63 64	FUNC_TEST=YES		
	UATA_DMACK_L	63 64	FUNC_TEST=YES		
	UATA_DA<2..0>	6 63 64	FUNC_TEST=YES		
	UATA_CS0_L	6 63 64	FUNC_TEST=YES		
	UATA_CS1_L	63 64	FUNC_TEST=YES		
	UATA_RESET_L	63 64	FUNC_TEST=YES		
	UATA_HSTROBE	63 64	FUNC_TEST=YES		
	UATA_STOP	63 64	FUNC_TEST=YES		
	UATA_INTRQ	63 64	FUNC_TEST=YES		
AUDIO	PP5V_PWRON_AUDIO_PVDD	74	FUNC_TEST=YES	Place within 25 mm of audio connector.	
	PP5V_PWRON_AUDIO_AVDD	74	FUNC_TEST=YES		
	PP3V3_PWRON_AUDIO_AVDD	74	FUNC_TEST=YES		
	=PP3V3_RUN_AUDIO	10 74	FUNC_TEST=YES		
	=I2C_AUDIO_SCL	8 74	FUNC_TEST=YES		
	=I2C_AUDIO_SDA	8 74	FUNC_TEST=YES		
	I2S0_MCLK	6 74	FUNC_TEST=YES		
	I2S0_BITCLK	6 74	FUNC_TEST=YES		
	I2S0_SYNC	6 74	FUNC_TEST=YES		
	I2S0_SB_TO_DEV_DTO	6 74	FUNC_TEST=YES		
	I2S0_DEV_TO_SB_DTI	22 74	FUNC_TEST=YES		
	AUDIO_LO_MUTE_L	22 74	FUNC_TEST=YES		
	AUDIO_SPKR_MUTE_L	22 74	FUNC_TEST=YES		
	AUDIO_CODEC_RESET_L	22 74	FUNC_TEST=YES		
	AUDIO_SPDIFRX_RESET_L	22 74	FUNC_TEST=YES		
	AUDIO_LO_DET_L	22 74	FUNC_TEST=YES		
	AUDIO_LI_DET_L	22 74	FUNC_TEST=YES		
	AUDIO_LO_OPTICAL_PLUG_L	22 74	FUNC_TEST=YES		
AUDIO_LI_OPTICAL_PLUG_L	22 74	FUNC_TEST=YES			
AUDIO_I2S_DTIB_SEL	22 74	FUNC_TEST=YES			
AUDIO_EXT_MCLK_SEL	22 74	FUNC_TEST=YES			
AUDIO_GPIO_11	22 74	FUNC_TEST=YES			
GND_AUDIO_AGND	74	FUNC_TEST=YES			
GND_AUDIO_PGND	74	FUNC_TEST=YES			

Category	Test Point	Pin	Function	Notes
SYSTEM	PP5V_TPAD_F	30	FUNC_TEST=YES	Place within 25 mm of TPAD connector.
	USB_TPAD_P	11 30	FUNC_TEST=YES	
	USB_TPAD_N	11 30	FUNC_TEST=YES	
	PP3V3_PWRON_DS1775_R	30	FUNC_TEST=YES	
	SYS_OVERTEMP_L	11 25 30	FUNC_TEST=YES	
	PP3V3_ALL_HALL_EFFRECT_R	30	FUNC_TEST=YES	
	SYS_LID_OPEN_F	30	FUNC_TEST=YES	
	SYS_POWER_BUTTON_L_F	30	FUNC_TEST=YES	
	=FTP_SLEEP_LED	74	FUNC_TEST=YES	
	SYS_CHARGE_LED_L	24 31	FUNC_TEST=YES	
	SYS_ADAPTER_ANALOG_AC_DET	12 31	FUNC_TEST=YES	
	KBDLED_ANODE	28 30	FUNC_TEST=YES	
	KBDLED_RETURN	28 30	FUNC_TEST=YES	
	=I2C_DS1775_SDA	8 30	FUNC_TEST=YES	
=I2C_DS1775_SCL	8 30	FUNC_TEST=YES		
CPU FAN	=PP5V_FAN1_PWR	10 31	FUNC_TEST=YES	Place within 25 mm of fan connector.
	FAN1_TACH	27 31	FUNC_TEST=YES	
	FAN1_PWM	27 31	FUNC_TEST=YES	
	=FTP_GND	7 10	FUNC_TEST=YES	
GPU FAN	=PP5V_FAN2_PWR	10 31	FUNC_TEST=YES	Place within 25 mm of fan connector.
	FAN2_TACH	27 31	FUNC_TEST=YES	
	FAN2_PWM	27 31	FUNC_TEST=YES	
	=FTP_GND	7 10	FUNC_TEST=YES	
ALS	=PP3V3_PWRON_LEFT_ALS	10 31	FUNC_TEST=YES	Place within 25 mm of ALS connector.
	ALS_0_OUT	25 31	FUNC_TEST=YES	
	ALS_GAIN_BOOST	25 28 31	FUNC_TEST=YES	
SCCA	SCCA_RXD	22 24	FUNC_TEST=YES	Place within 25 mm of debug connector.
	SCCA_TXD_L	22 24	FUNC_TEST=YES	
BACKUP BATT	=PPVIO_BU_BATT	10 31	FUNC_TEST=YES	Place within 25 mm of battery connector.
	=PPVOUT_BU_BATT	10 31	FUNC_TEST=YES	
RT USB	=PP5V_PWRON_RIGHT_USB	10 31	FUNC_TEST=YES	Place within 25 mm of right USB connector.
	USB2_RIGHT_PORT_P	11 31	FUNC_TEST=YES	
	USB2_RIGHT_PORT_N	11 31	FUNC_TEST=YES	
LT USB	=PP5V_PWRON_LEFT_USB	10 31	FUNC_TEST=YES	Place within 25 mm of left USB connector.
	USB2_LEFT_PORT_P	11 31	FUNC_TEST=YES	
	USB2_LEFT_PORT_N	11 31	FUNC_TEST=YES	

Functional Test Points

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6839	02
SCALE	SHT	OF
NONE	7	115

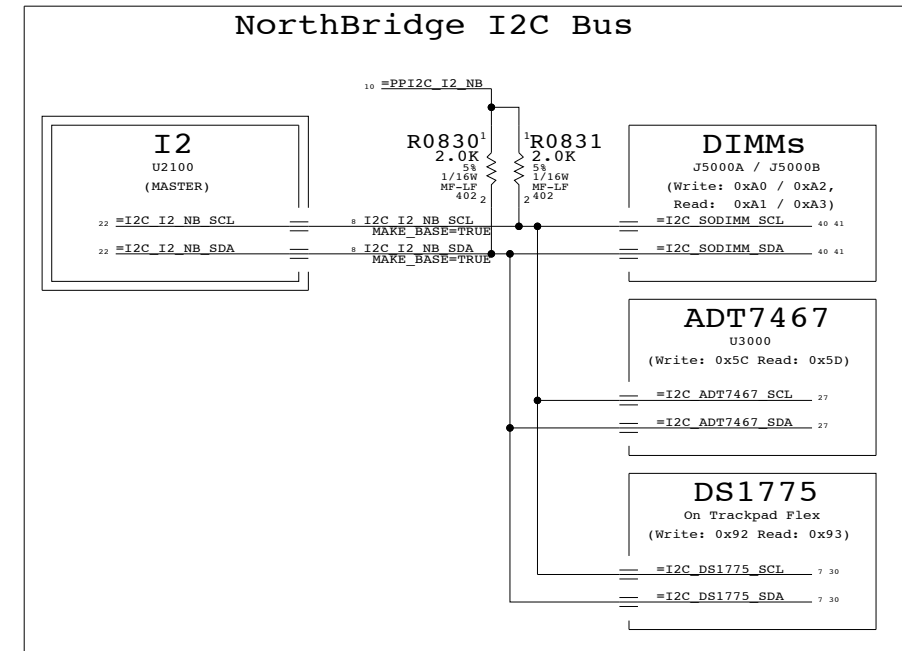
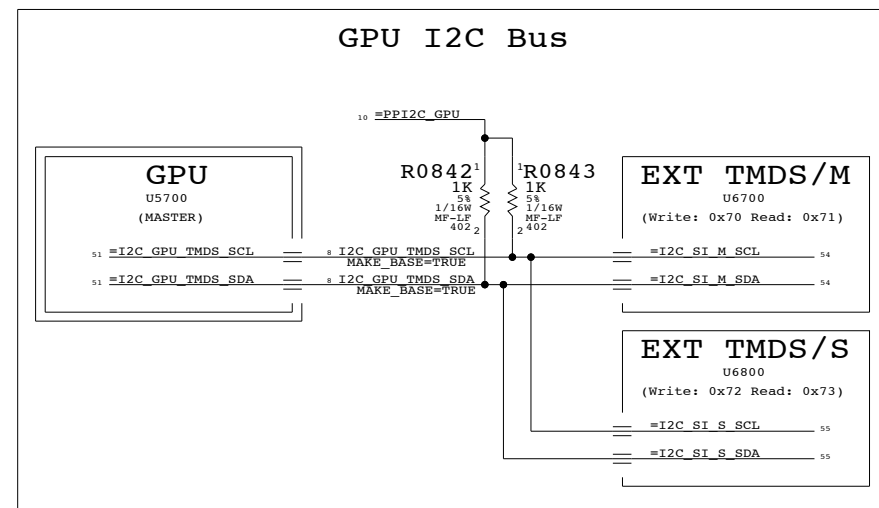
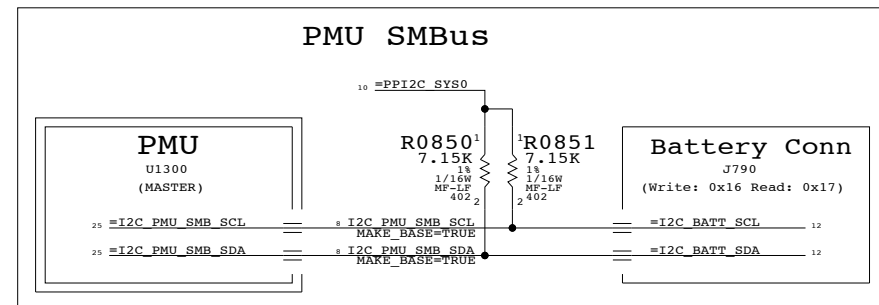
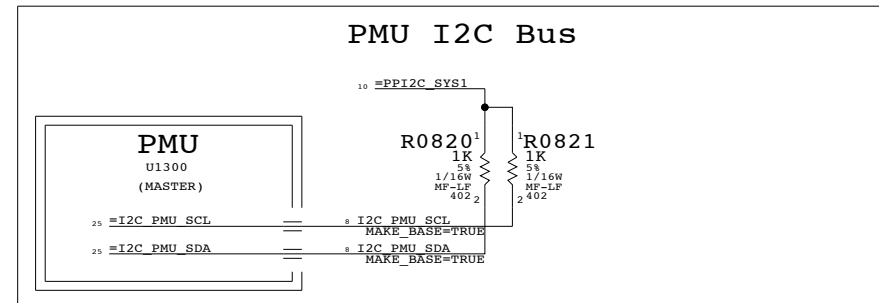
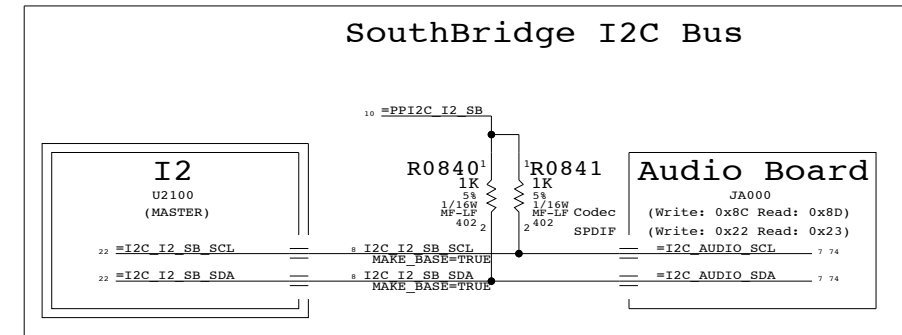
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I2C_PMU_SMB_SDA	I2C	I2C	
I2C_PMU_SCL	I2C	I2C	
I2C_PMU_SDA	I2C	I2C	
I2C_NB	I2C	I2C	
I2C_NB	I2C	I2C	
I2C_I2_SB_SCL	I2C	I2C	
I2C_I2_SB_SDA	I2C	I2C	
I2C_GPU_TMDS_SCL	I2C	I2C	
I2C_GPU_TMDS_SDA	I2C	I2C	

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- GOV_I2C / GOV_I2C_BYPASS
Allows bypassing Governor I2C bus.
Most devices are connected directly to PMU instead. One ADT7467 connects to NB I2C bus 1 to resolve address conflict.
- MMM_PWR_ALL / MMM_PWR_PWRON
Selects whether MMM MCU is powered all the time or only when the system is on. ALL moves the MCU to the PMU I2C bus so it can be monitored by in shutdown.
NOTE: Neither option is necessary when MMM_MCU_PMU BOM option is selected.



I2C Connections

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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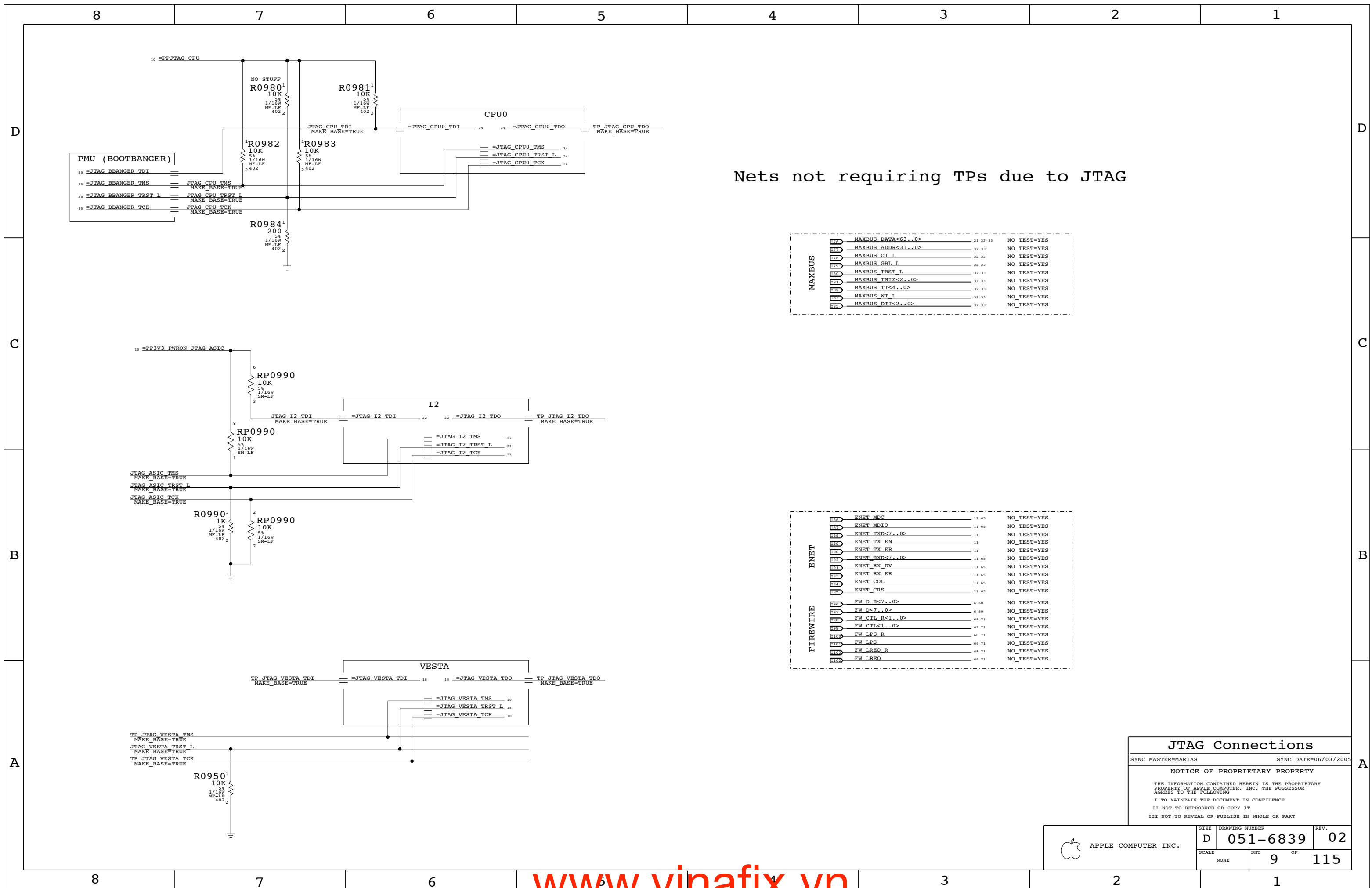
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	D	051-6839	02
SCALE	SHT	OF	
NONE	8	115	



Nets not requiring TPs due to JTAG

NET	MAXBUS DATA<63..0>	21 32 33	NO_TEST=YES
MAXBUS	MAXBUS ADDR<31..0>	32 33	NO_TEST=YES
MAXBUS	MAXBUS CI L	32 33	NO_TEST=YES
MAXBUS	MAXBUS GBL L	32 33	NO_TEST=YES
MAXBUS	MAXBUS TRST L	32 33	NO_TEST=YES
MAXBUS	MAXBUS TSI<2..0>	32 33	NO_TEST=YES
MAXBUS	MAXBUS TT<4..0>	32 33	NO_TEST=YES
MAXBUS	MAXBUS WT L	32 33	NO_TEST=YES
MAXBUS	MAXBUS DTI<2..0>	32 33	NO_TEST=YES

NET	ENET MDC	11 65	NO_TEST=YES
ENET	ENET MDIO	11 65	NO_TEST=YES
ENET	ENET TXD<7..0>	11	NO_TEST=YES
ENET	ENET TX_EN	11	NO_TEST=YES
ENET	ENET TX_ER	11	NO_TEST=YES
ENET	ENET RXD<7..0>	11 65	NO_TEST=YES
ENET	ENET RX_DV	11 65	NO_TEST=YES
ENET	ENET RX_ER	11 65	NO_TEST=YES
ENET	ENET COL	11 65	NO_TEST=YES
ENET	ENET CRS	11 65	NO_TEST=YES
FIREWIRE	FW D R<7..0>	6 69	NO_TEST=YES
FIREWIRE	FW D<7..0>	6 69	NO_TEST=YES
FIREWIRE	FW CTL R<1..0>	69 71	NO_TEST=YES
FIREWIRE	FW CTL<1..0>	69 71	NO_TEST=YES
FIREWIRE	FW LPS_R	69 71	NO_TEST=YES
FIREWIRE	FW LPS	69 71	NO_TEST=YES
FIREWIRE	FW LREQ_R	69 71	NO_TEST=YES
FIREWIRE	FW LREQ	69 71	NO_TEST=YES

JTAG Connections

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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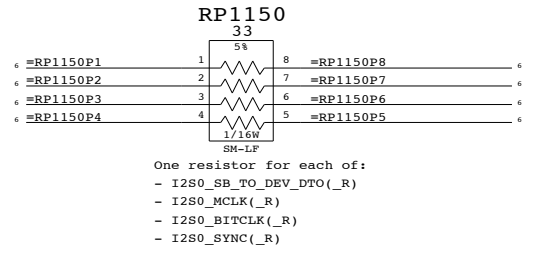
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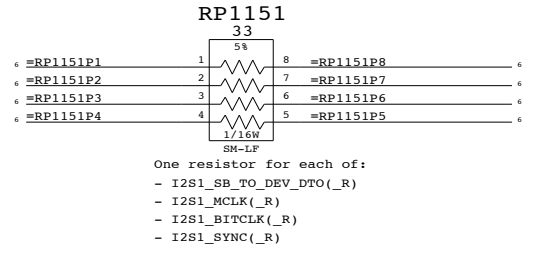
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SCALE	SHT	OF	
NONE	9	115	

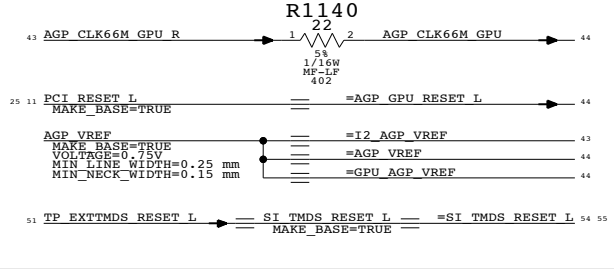
I2S0 Series Rs



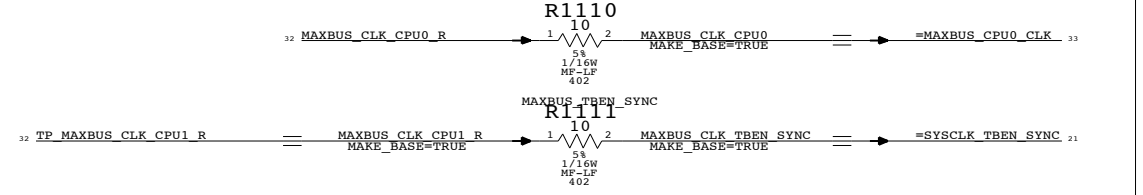
I2S1 Series Rs



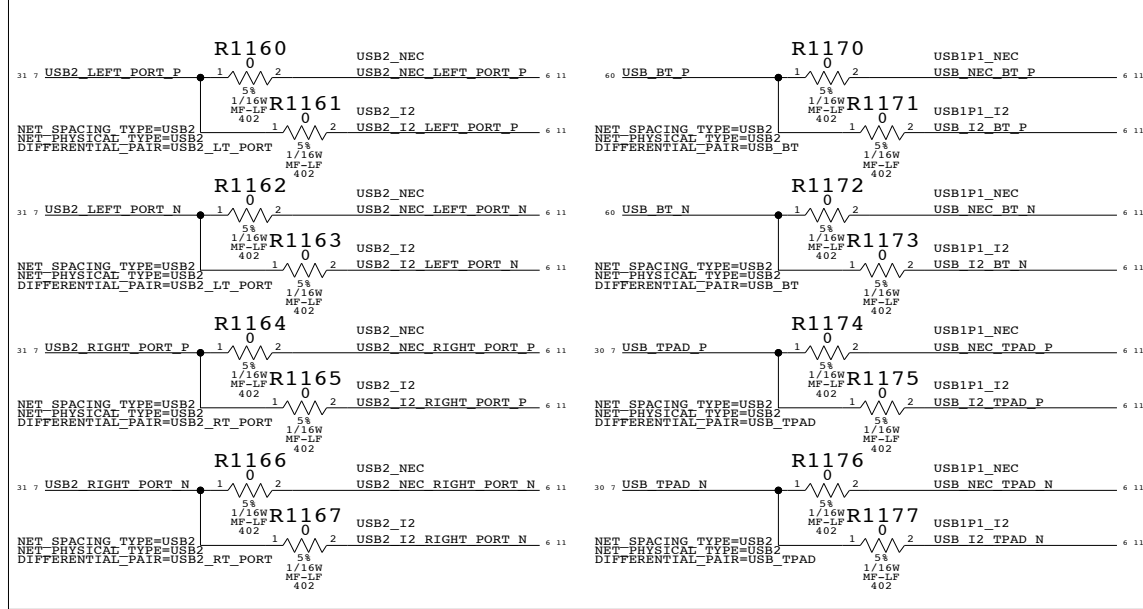
GPU



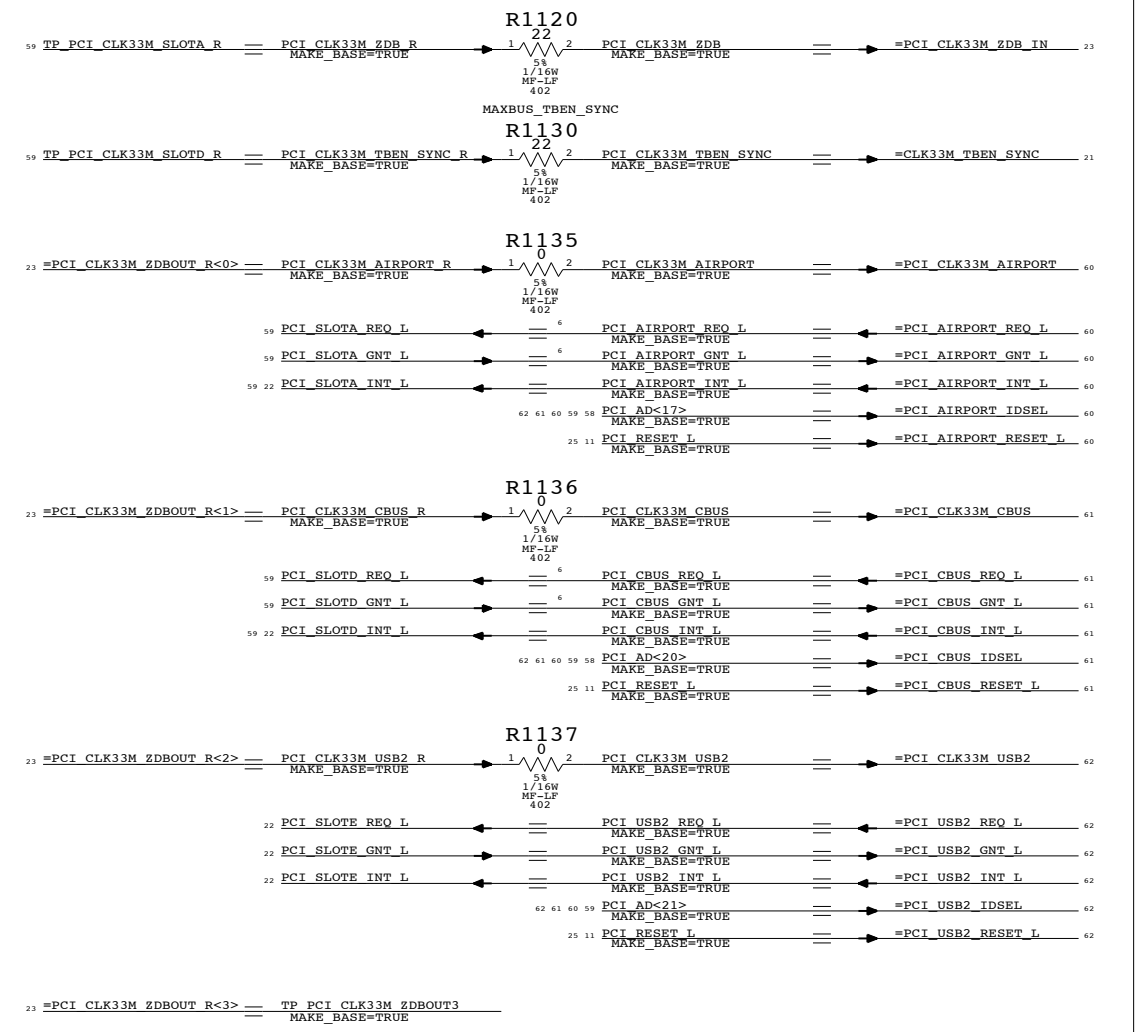
CPU Clocks



USB Controller Mux



PCI



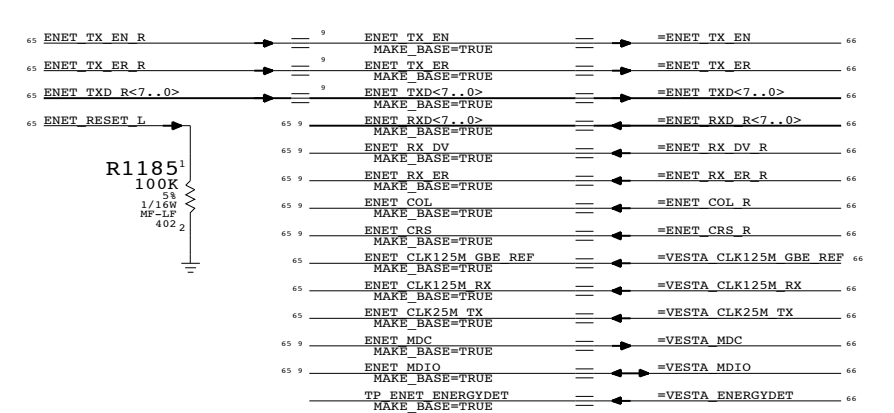
USB Port Assignments

11 6	USB2_I2_LEFT_PORT_P	==	USB2_I2_P<0>	72	11 6	USB2_NEC_LEFT_PORT_P	==	USB2_NEC_P<0>	73
11 6	USB2_I2_LEFT_PORT_N	==	USB2_I2_N<0>	72	11 6	USB2_NEC_LEFT_PORT_N	==	USB2_NEC_N<0>	73
11 6	USB2_I2_RIGHT_PORT_P	==	USB2_I2_P<2>	72	11 6	USB2_NEC_RIGHT_PORT_P	==	USB2_NEC_P<1>	73
11 6	USB2_I2_RIGHT_PORT_N	==	USB2_I2_N<2>	72	11 6	USB2_NEC_RIGHT_PORT_N	==	USB2_NEC_N<1>	73
11 6	USB_I2_BT_P	==	USB2_I2_P<4>	72	11 6	USB_NEC_BT_P	==	USB2_NEC_P<2>	73
11 6	USB_I2_BT_N	==	USB2_I2_N<4>	72	11 6	USB_NEC_BT_N	==	USB2_NEC_N<2>	73
11 6	USB_I2_TPAD_P	==	USB2_I2_P<5>	72	11 6	USB_NEC_TPAD_P	==	USB2_NEC_P<3>	73
11 6	USB_I2_TPAD_N	==	USB2_I2_N<5>	72	11 6	USB_NEC_TPAD_N	==	USB2_NEC_N<3>	73

PMU Connections

20 25	SYS_OVERTEMP_L	==	ADT7467_THERM_L	27	24	SYS_PWRSEQ_1	==	TP_PMU_AN_P0_1	25
13	PMU_CHARGE_V	==	TP_PMU_P7_5	25	24	SYS_PWRSEQ_2	==	TP_PMU_AN_P0_2	25
25	PMU_CPU_HRESET_L	==	CPU_HRESET_L	34	24	SYS_PWRSEQ_3_L	==	TP_PMU_AN_P0_3	25
12	SYS_PMU_ANALOG_AC_DET	==	TP_PMU_AN_P10_6	25	24	SYS_PWRSEQ_4	==	TP_PMU_AN_P0_4	25
25	GOV_RESET_L	==	TP_GOV_RESET_L	22	24	SYS_PWRSEQ_5	==	TP_PMU_AN_P0_5	25
25	PMU_CPU_CLK_EN	==	I2_STOPCPU_L	22	24	SYS_PWRSEQ_6_L	==	TP_PMU_P7_4	25
25	PMU_SYS_CLK_EN	==	I2_STOPXTAL_L	22	24	SYS_PWRSEQ_FINAL	==	TP_PMU_AN_P10_5	25

Vesta Ethernet



MISC

25	PCI_RESET_L	==	ROM_PWD_L	54		
32	TP_MAXBUS_CPU1_OACK_L	==	NC_MAXBUS_CPU1_OACK_L			
22	I2_GPIO_11	==	TP_I2_GPIO_11			
22	I2_GPIO_EXT_02	==	CPU0_VID_AB_SEL	==	CPU0_VID_AB_SEL	36
22	SPI_I2_REQ	==	CPU0_MAXI1717_AB_SEL	==	CPU0_MAXI1717_AB_SEL	36
24	SLEEP_LED_IOUT	==	SLEEP_LED_IOUT	==	SLEEP_LED_CONN	74

Signal Synonyms

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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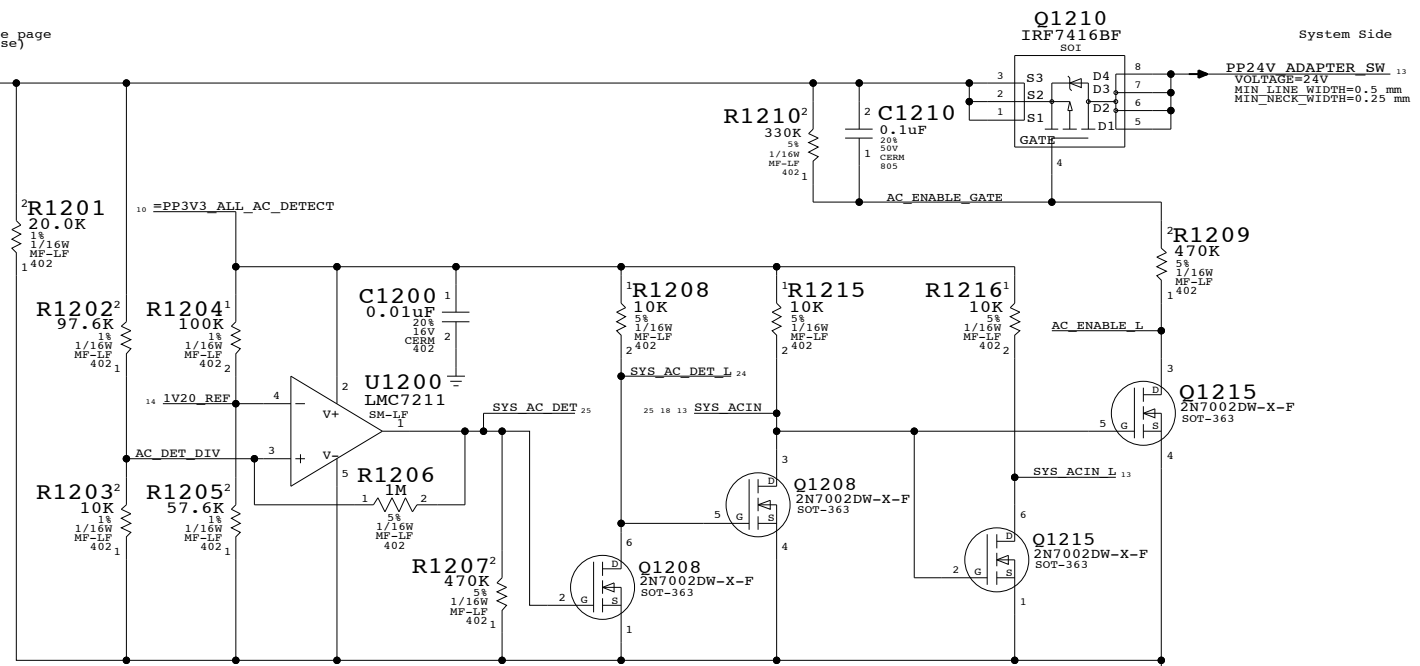
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	D	051-6839	02
SCALE	SHEET	OF	
NONE	11	115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
PP3V3	THERM	THERM	BATTERY_ISNS
PP3V3	THERM	THERM	BATTERY_ISNS

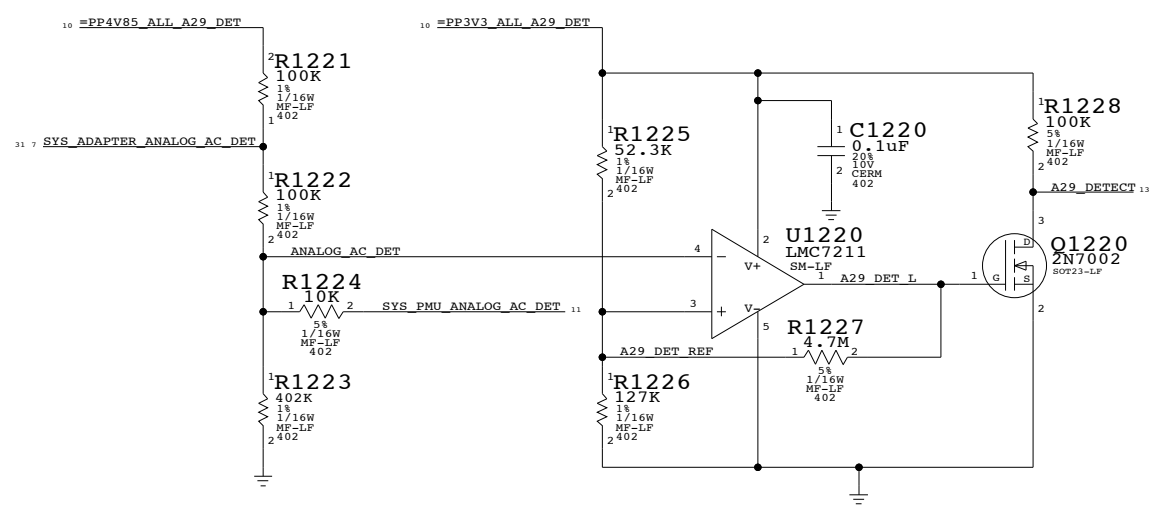
ADAPTER INPUT/INRUSH LIMITER

Adapter Connector Side
(Connector is on separate page to facilitate design reuse)



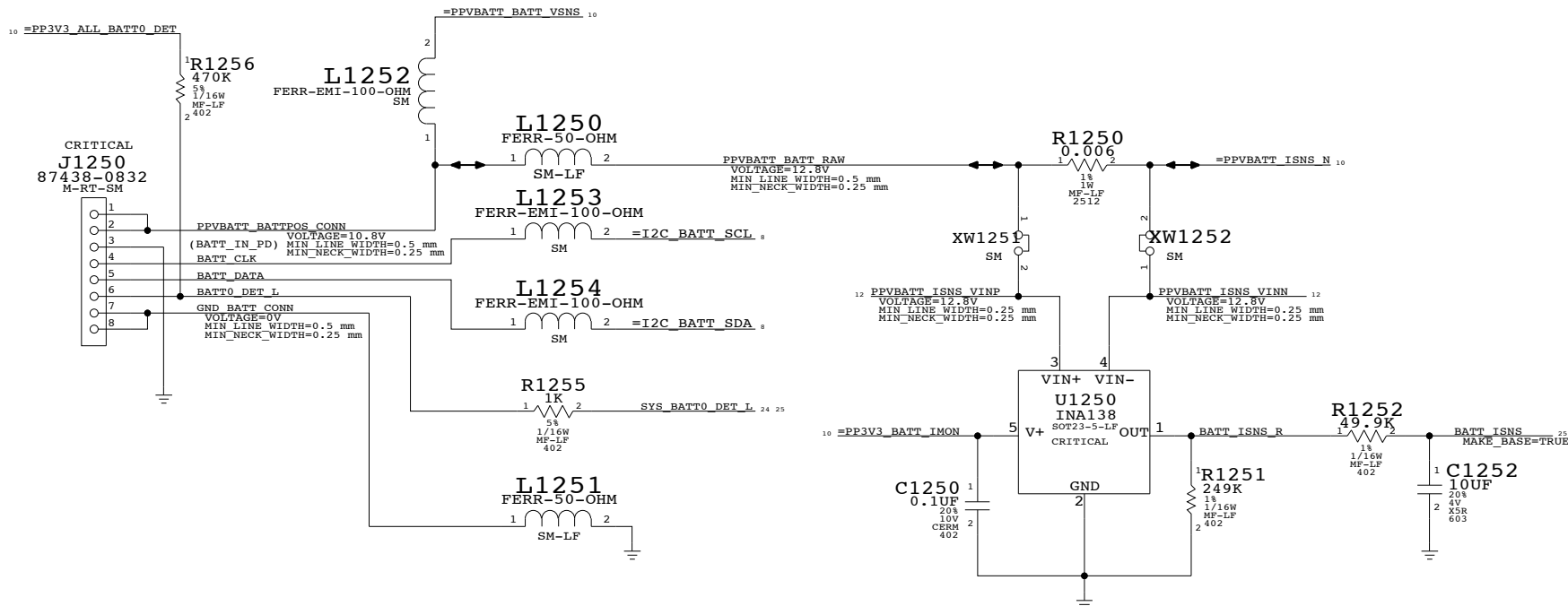
GREATER THAN 13.1V DETECT SYS AC DET indicates adapter presence. SYS ACIN is code-controlled signal to enable use of AC in system. Q1208 ensures SYS ACIN goes low as soon as SYS AC DET goes low. Therefore, hardware immediately disables the AC upon removal but only software can enable AC after detection by the PMU.

A29 ADAPTER DETECTION



ADAPTER IDS		
ADAPTER	ID RANGE	PIN VOLTAGE
Q11 (65W)	1.65-2.31V	2.007-2.066V
A29 (45W)	2.31-2.97V	2.558-2.661V
AIRLINE	0.33-0.99V	0.589-0.663V

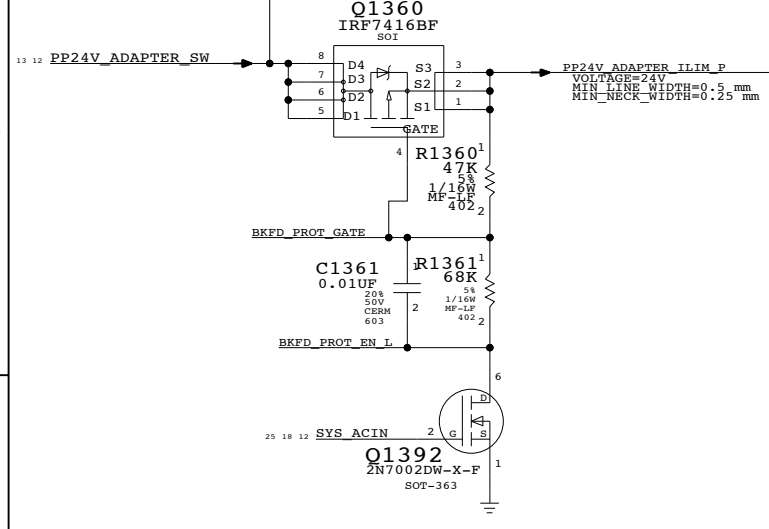
BATTERY INPUT/CURRENT SENSE



Power Inputs
 SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005
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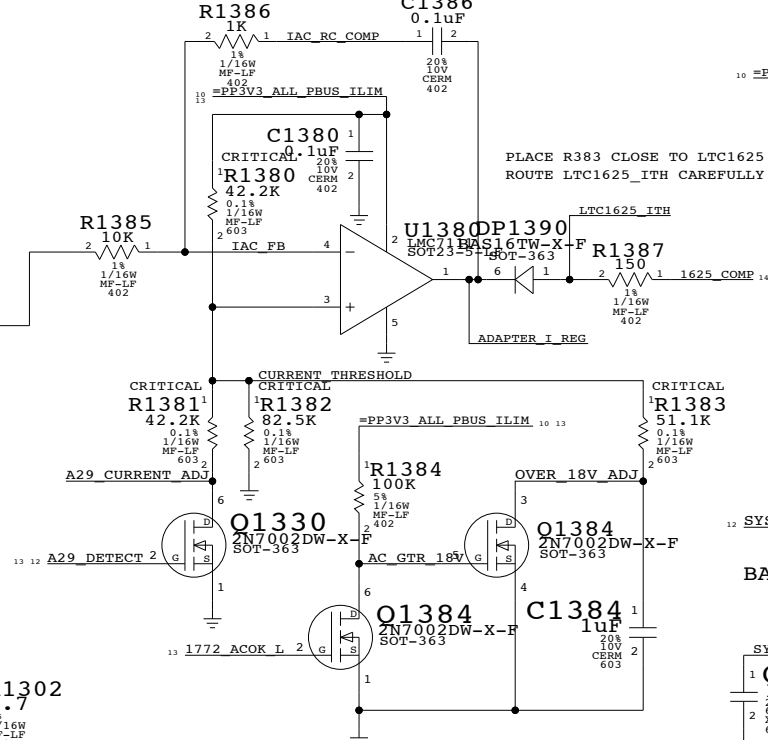
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	NONE	051-6839	02
SCALE		SHT	OF
NONE		12	115

BACKFEED PROTECTION

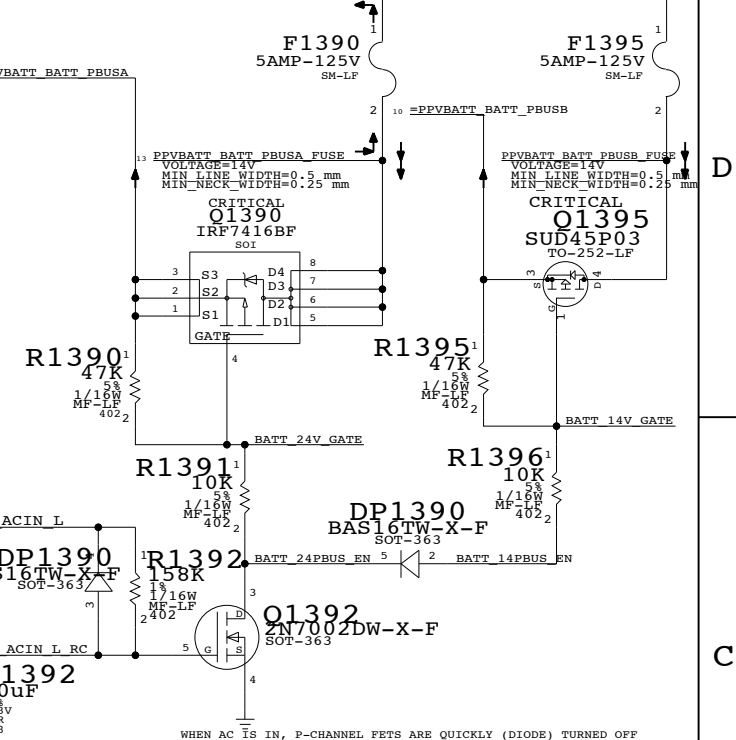


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11480343	1	RES,20K,1%,1/16W,MF-LF,402	R1345	Q16C_PARTS
11480382	1	RES,48.7K,1%,1/16W,MF-LF,402	R1345	Q41C_PARTS

+PBUS CURRENT LIMIT

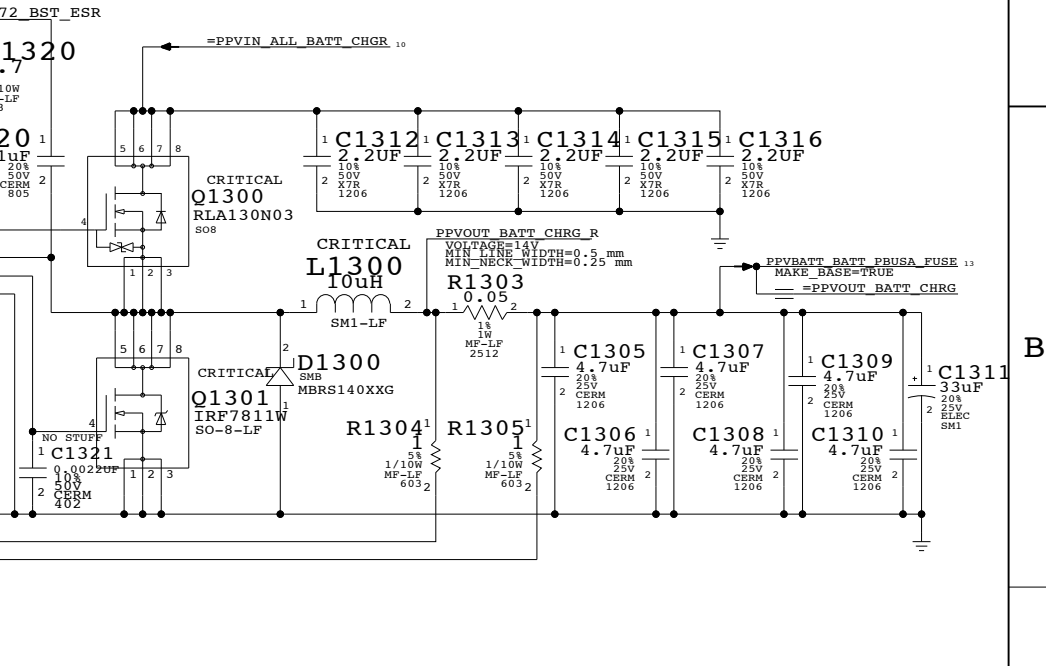
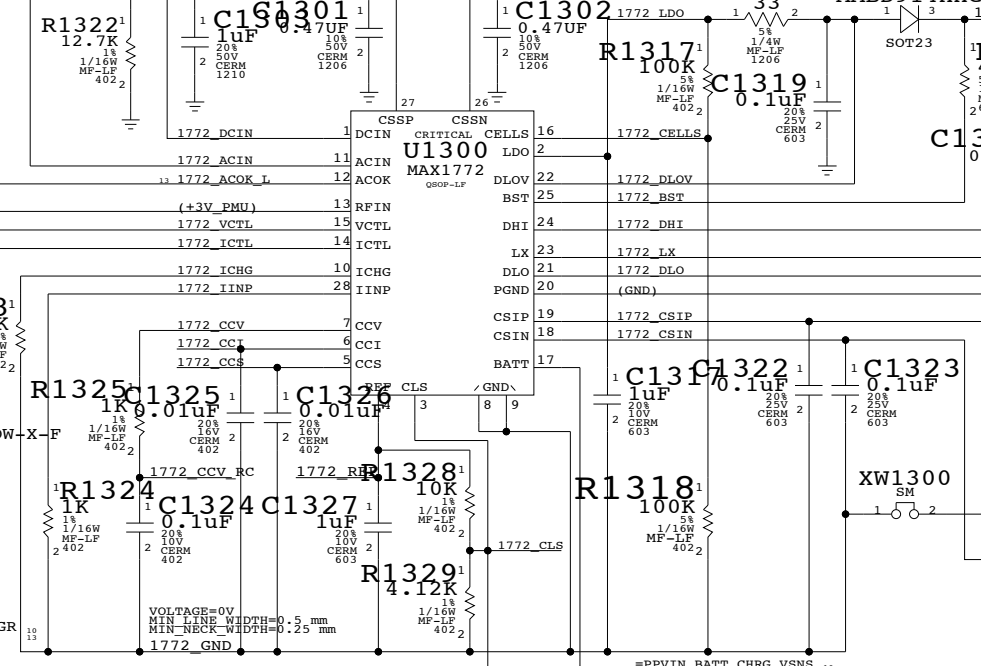
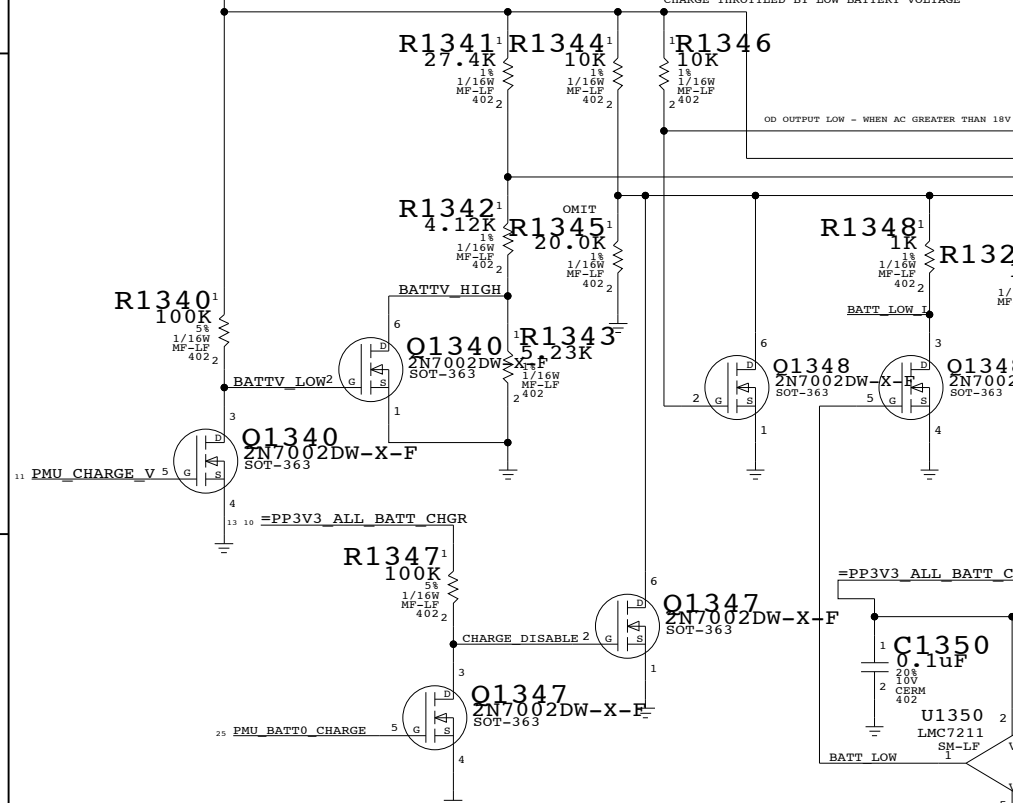


BATTERY SWITCH-OVER CIRCUIT



SWITCHER VOLTAGE CONTROL

SWITCHER CURRENT CONTROL



$V_{BATT} = CELLS \times (4.096 + (0.4096 \times V_{VCTL} / V_{REFIN}))$
 For 4.15V cells, $V_{VCTL} = 0.123 \text{ REFIN}$
 For 4.20V cells, $V_{VCTL} = 0.245 \text{ REFIN}$
 $I_{CHG} = (0.2048 / R_{62}) \times (V_{ICTL} / V_{REFIN})$

Battery Charger

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

NOTICE OF PROPRIETARY PROPERTY

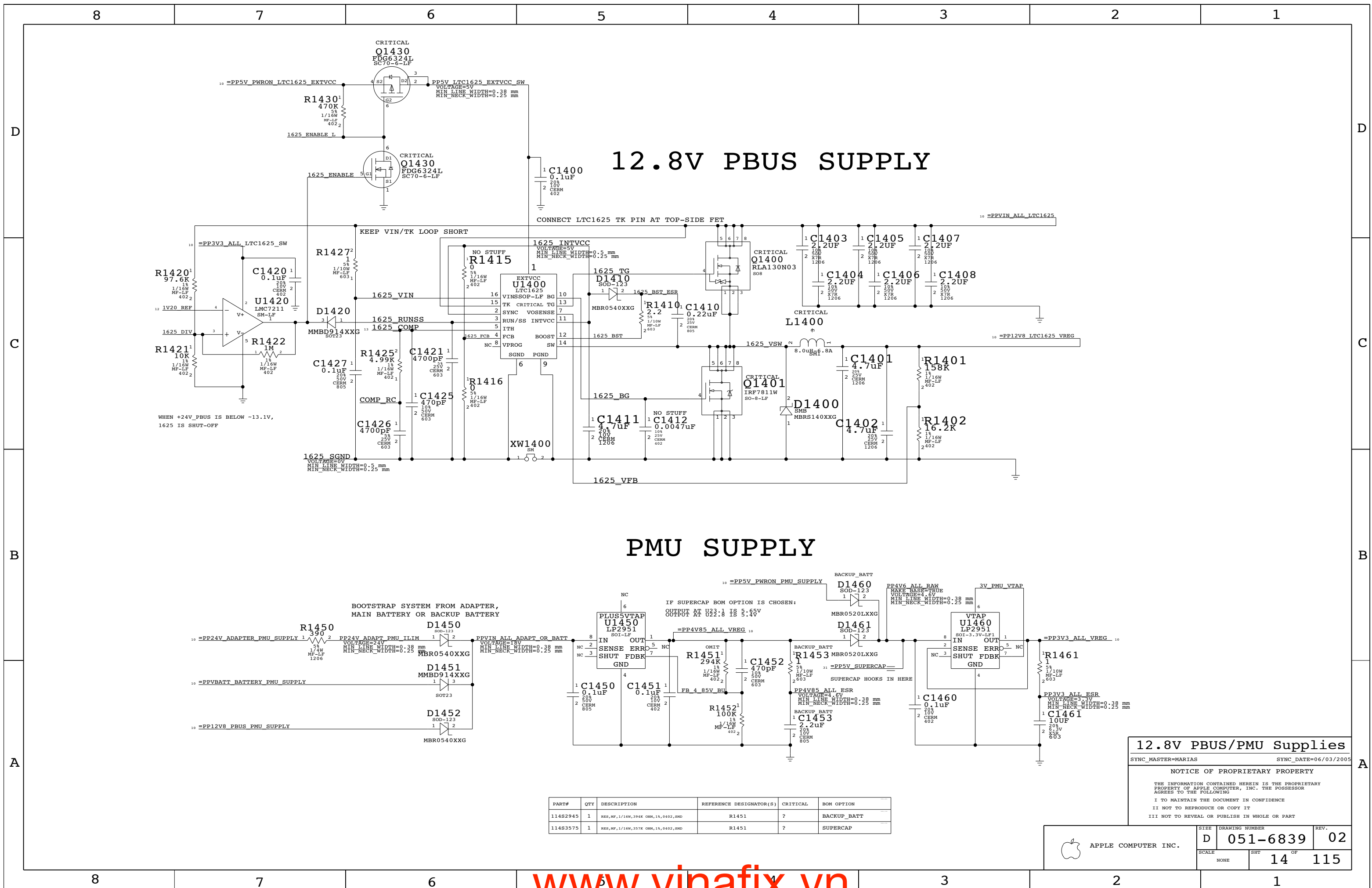
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SCALE	SHT	OF	
NONE	13	115	



12.8V PBUS SUPPLY

PMU SUPPLY

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S2945	1	RES, MF, 1/16W, 394K OHM, 1%, 0402, SMD	R1451	?	BACKUP_BATT
114S3575	1	RES, MF, 1/16W, 357K OHM, 1%, 0402, SMD	R1451	?	SUPERCAP

12.8V PBUS/PMU Supplies

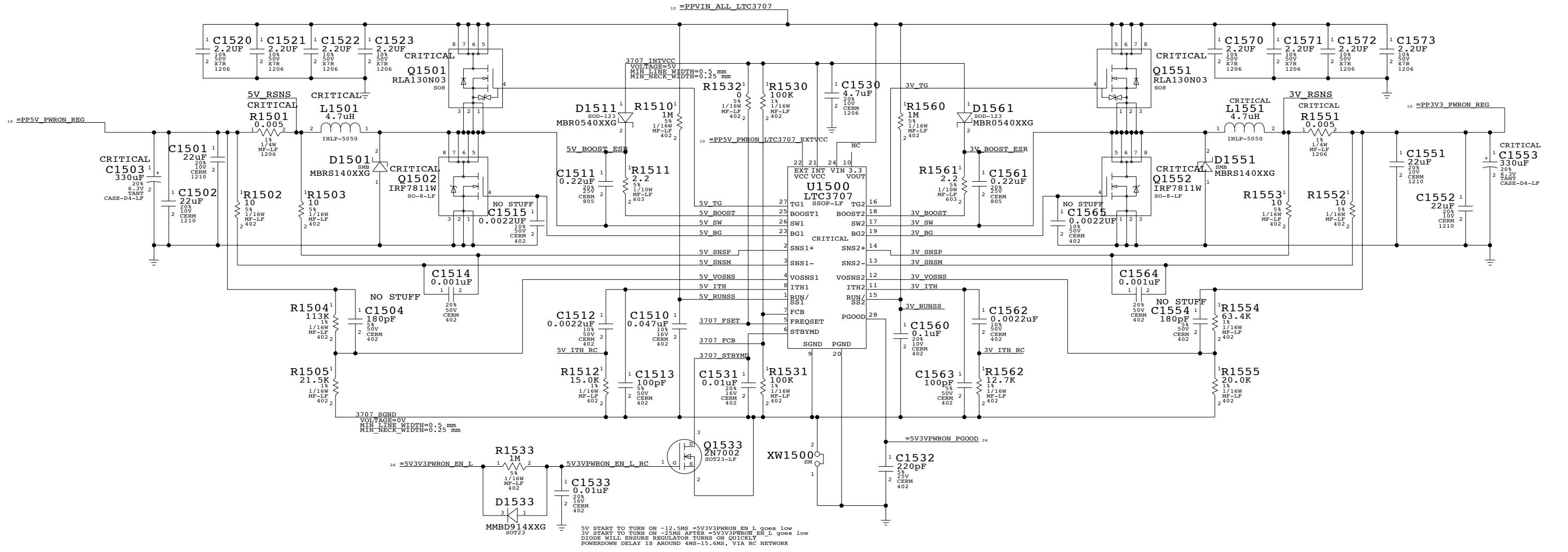
SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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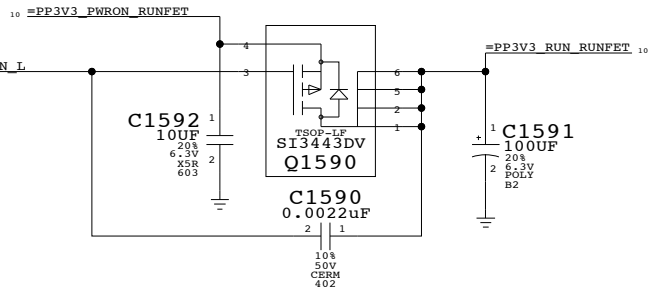
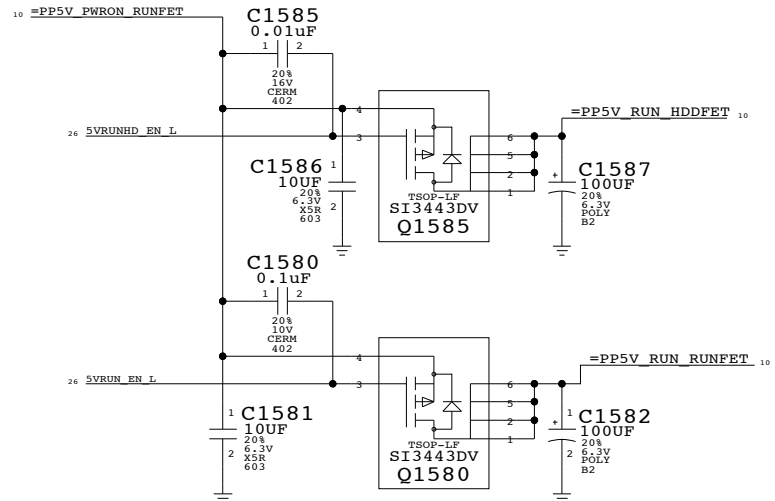
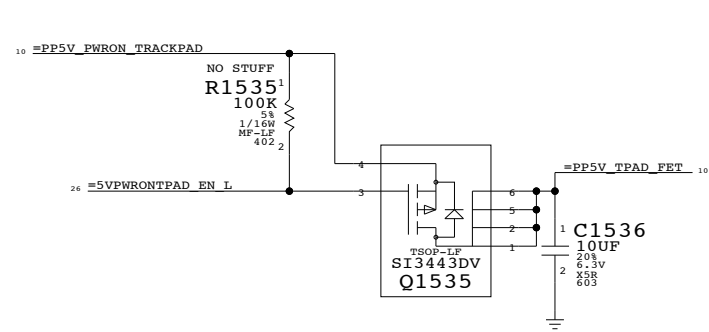
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APPLE COMPUTER INC.	SCALE	DRAWING NUMBER	REV.
	NONE	D 051-6839	02
SHEET		OF	
14		115	

3.3V/5V SWITCHER



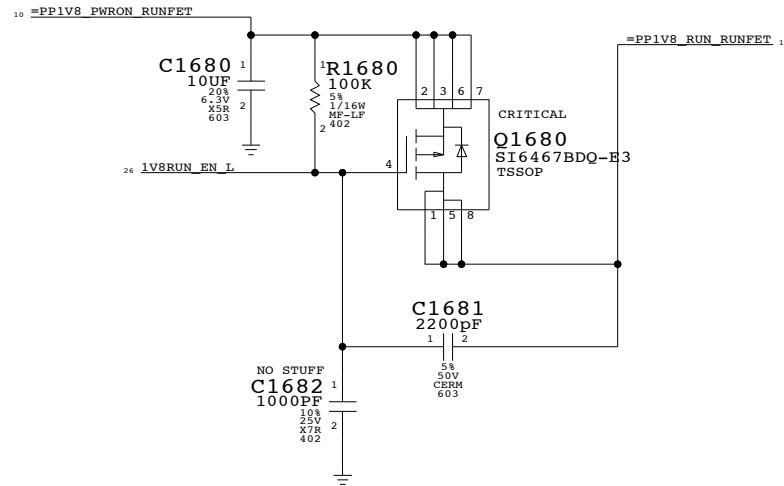
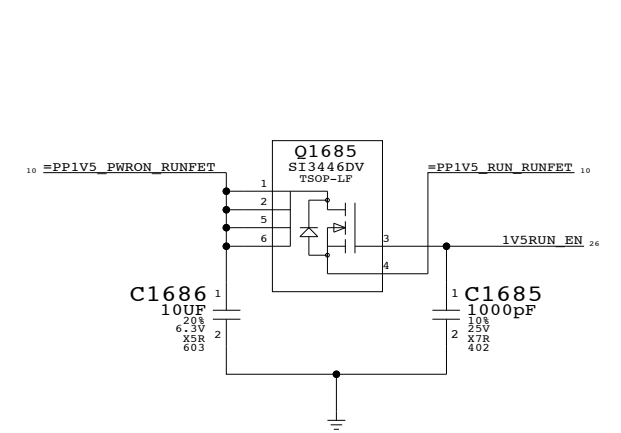
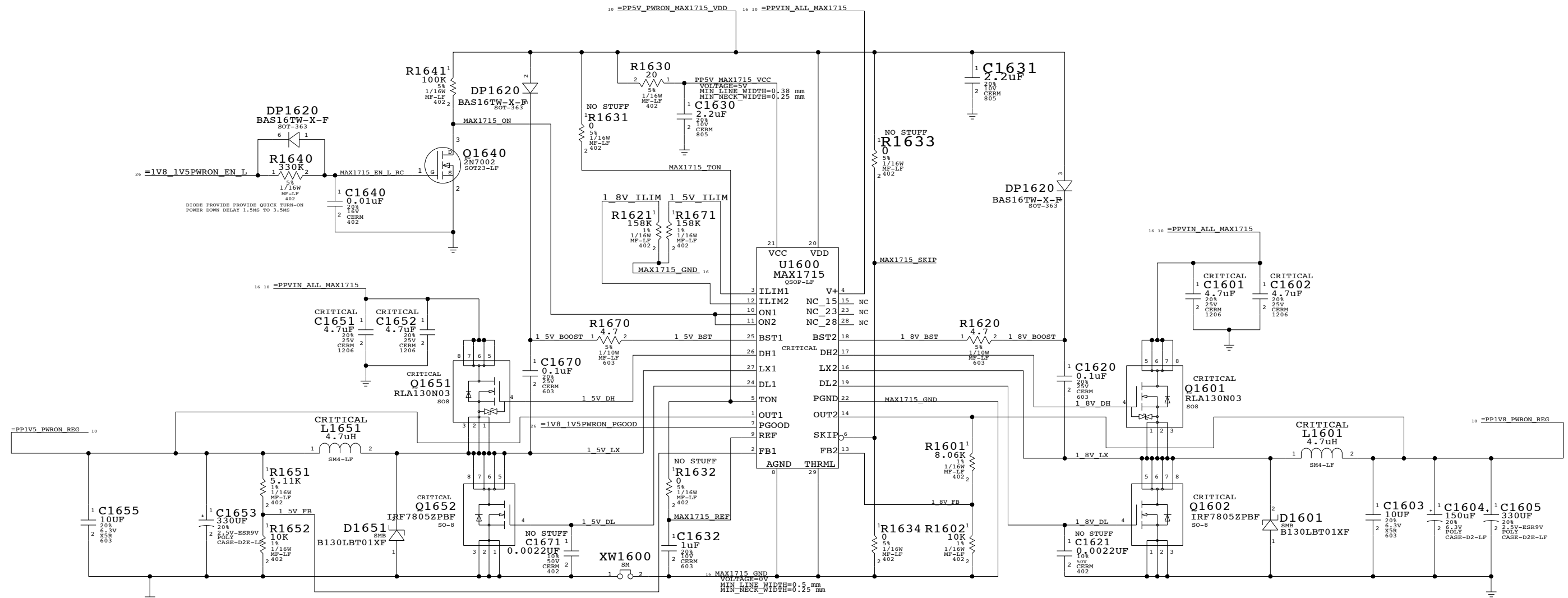
5V START TO TURN ON -12.5MS =5V3VPWRON_EN L goes low
 3V START TO TURN ON -25MS AFTER =5V3VPWRON_EN L goes low
 DIODE WILL ENSURE REGULATOR TURNS ON QUICKLY
 POWERDOWN DELAY IS AROUND 4MS-15.6MS, VIA RC NETWORK



5V/3.3V Supplies
 SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005
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SCALE	NONE	SHT	15 OF 115

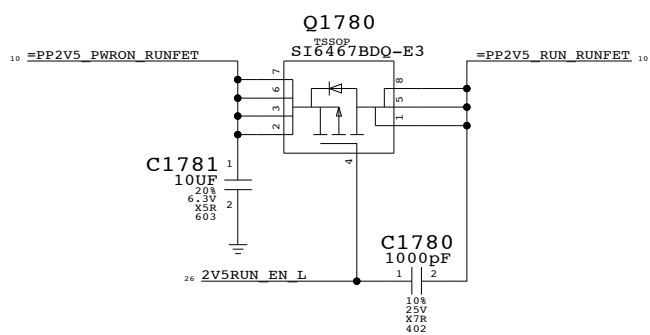
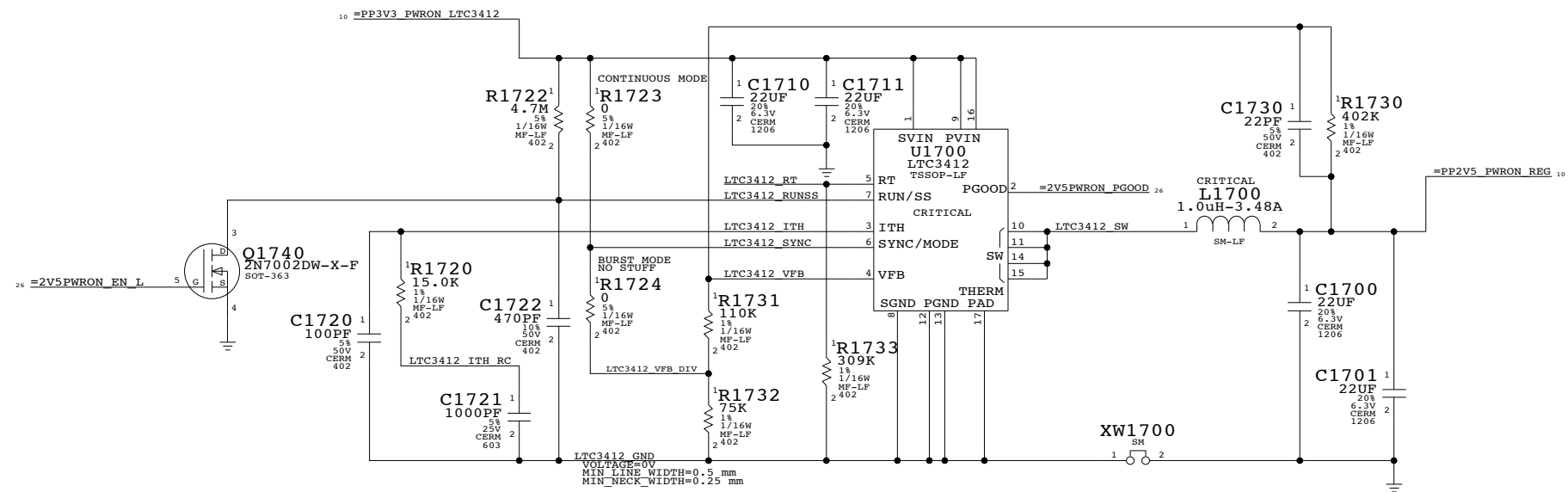
1.5V/1.8V SWITCHER



1.8V/1.5V Supplies
 SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005
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2.5V SWITCHER



2.5V Supply

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SCALE	SHT OF		
NONE	17 OF		115

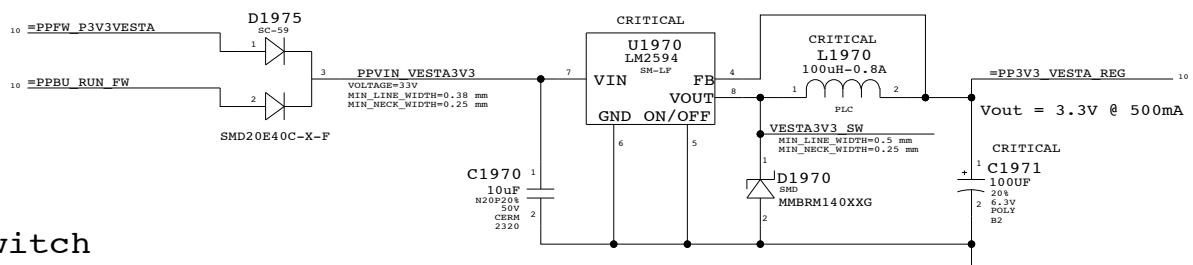
Page Notes

Power aliases required by this page:
 - =PPBUS_FW (system supply for bus power)
 - =PPBUS_RUN_FW (backup PHY power)
 - =PP3V3_RUN_FWPORTFWRWSW

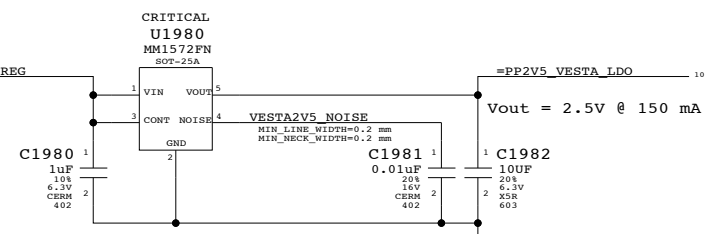
Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - VESTA1V2_BURST / VESTA1V2_PULSE
 Controls operating mode of Vesta 1.2V regulator. If both options are off the regulator will be in continuous mode.

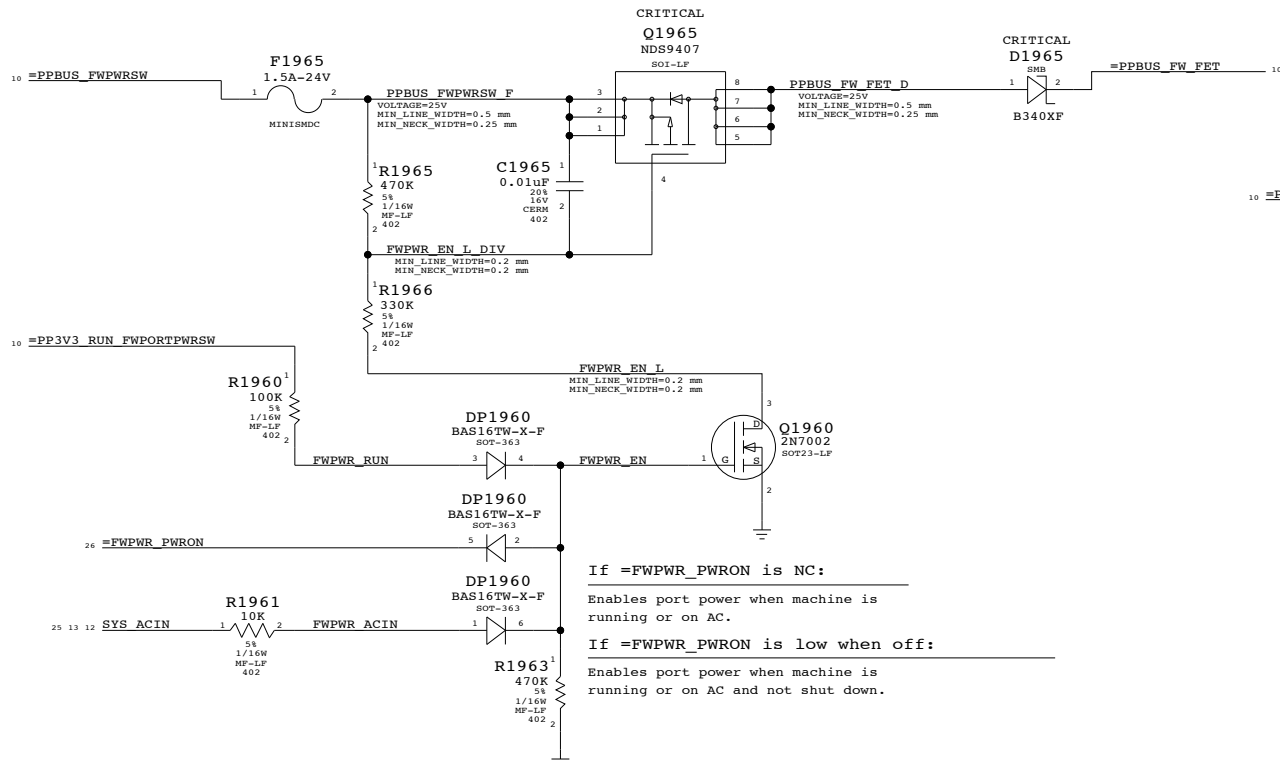
3.3V Regulator



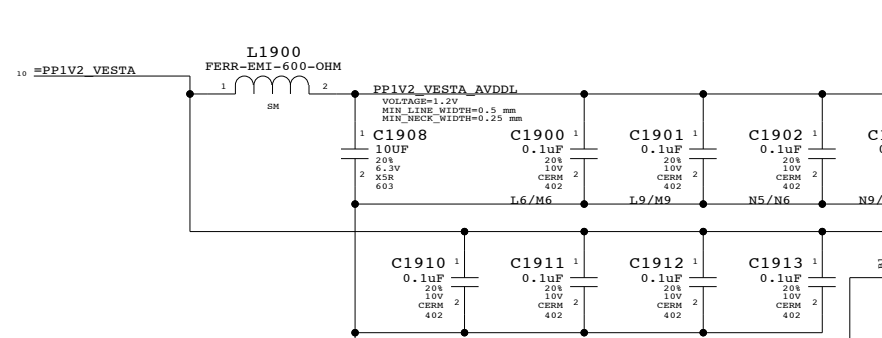
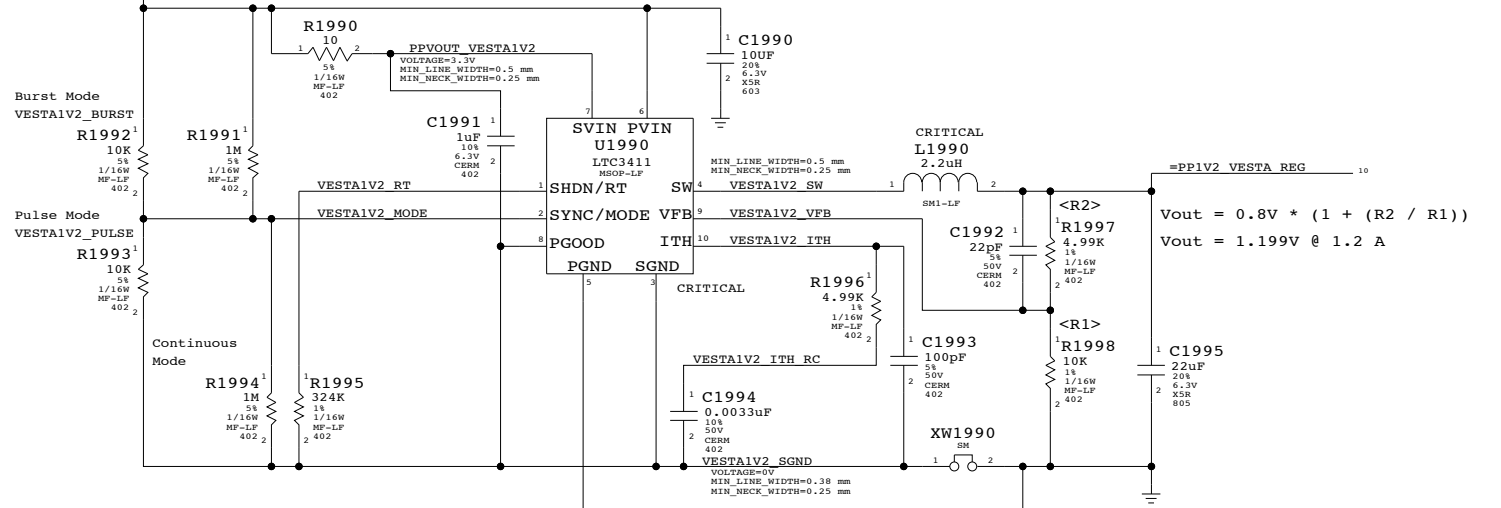
2.5V LDO



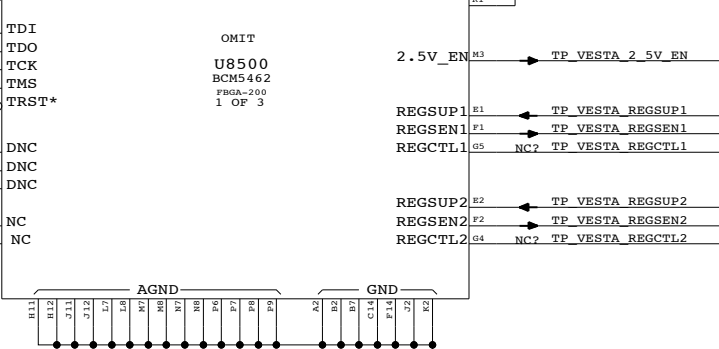
Port Power Switch



1.2V Regulator



VESTA MISC



Vesta Power & Misc
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SCALE	SHT	OF	
NONE	19	115	

Page Notes

Power aliases required by this page:

- =PPVCORE_PWRON_I2
- =PP1V5_PWRON_I2_PLL
- =PP3V3_PWRON_I2_IO1
- =PP3V3_PWRON_I2_IO2
- =PP3V3_PWRON_I2_MAXBUS
- =PP3V3_PWRON_I2_AGPPCI
- =PP3V3_PWRON_I2_MAXBUS

NOTE: The four 3.3V rails are meant to be aliased together. They are called out separately for test purposes.
NOTE: When these four rails are not aliased together, make sure there is at least one 10uF cap per rail.

Signal aliases required by this page:

(NONE)

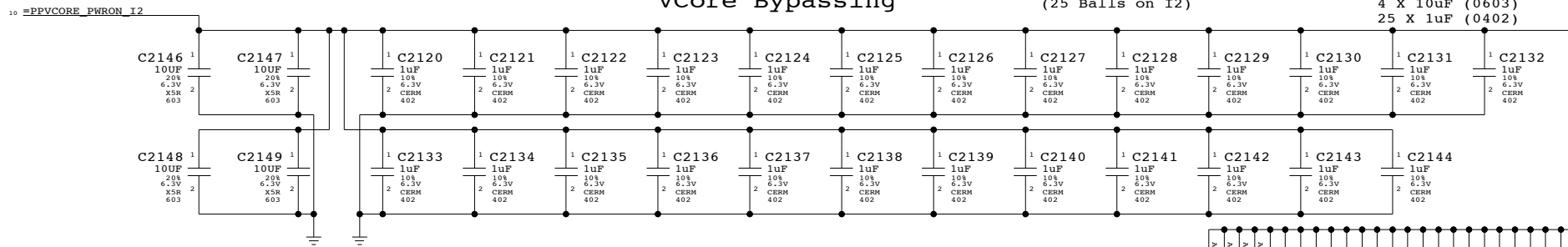
BOM options provided by this page:

(NONE)

VCore Bypassing

(25 Balls on I2)

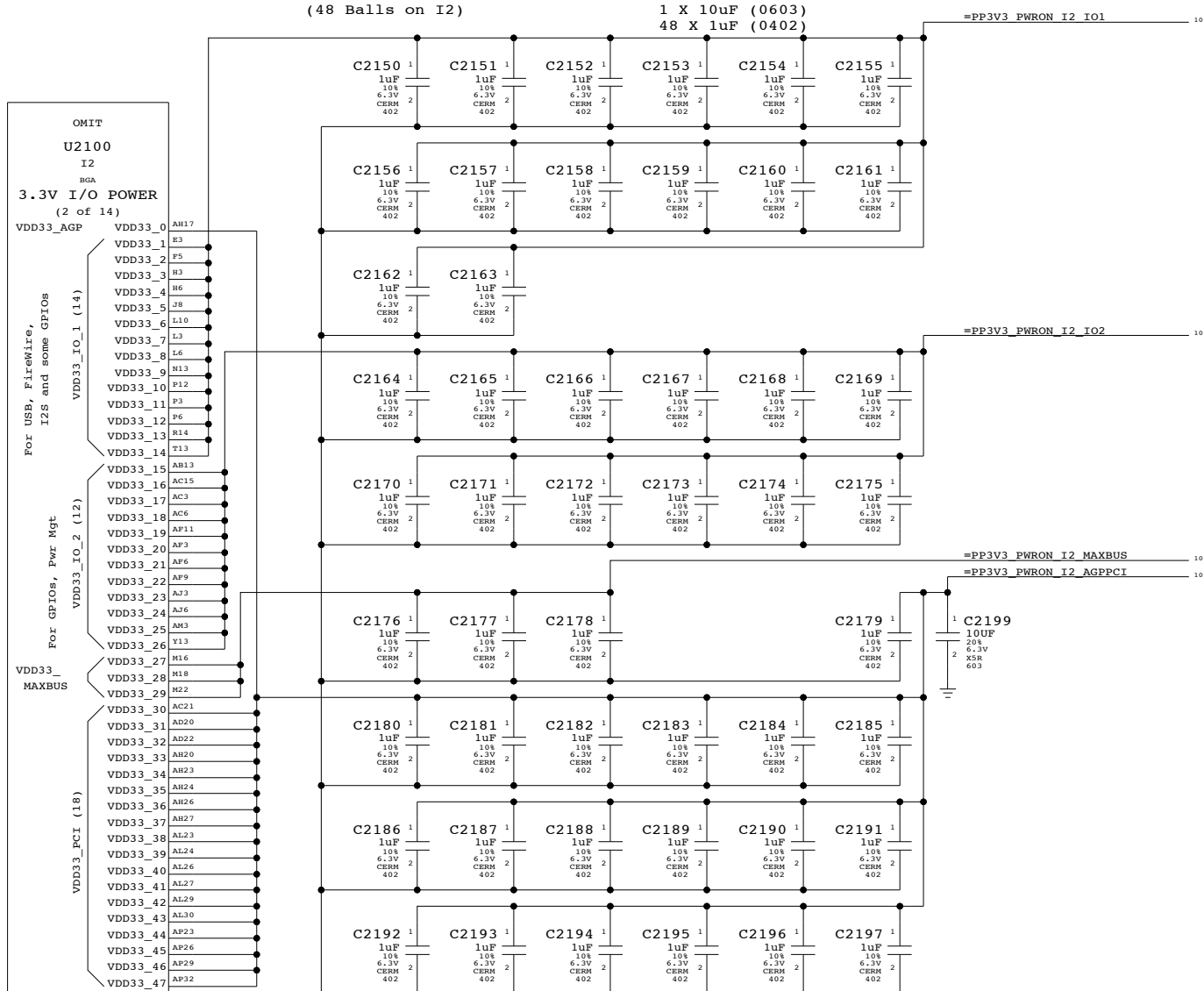
4 X 10uF (0603)
25 X 1uF (0402)



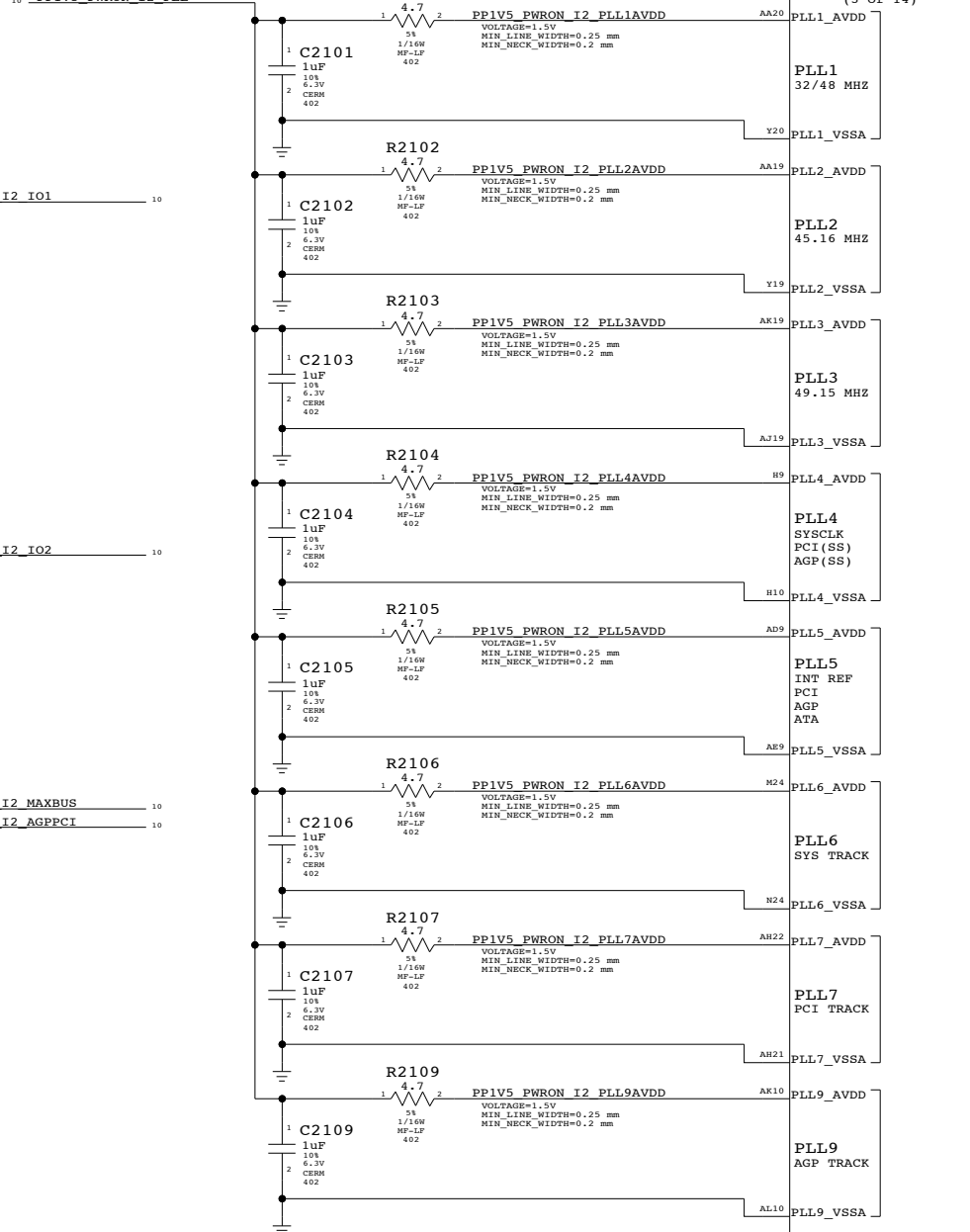
3.3V I/O DECOUPLING

(48 Balls on I2)

1 X 10uF (0603)
48 X 1uF (0402)



10=PP1V5_PWRON_I2_PLL



I2 Power

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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NONE	21	115	

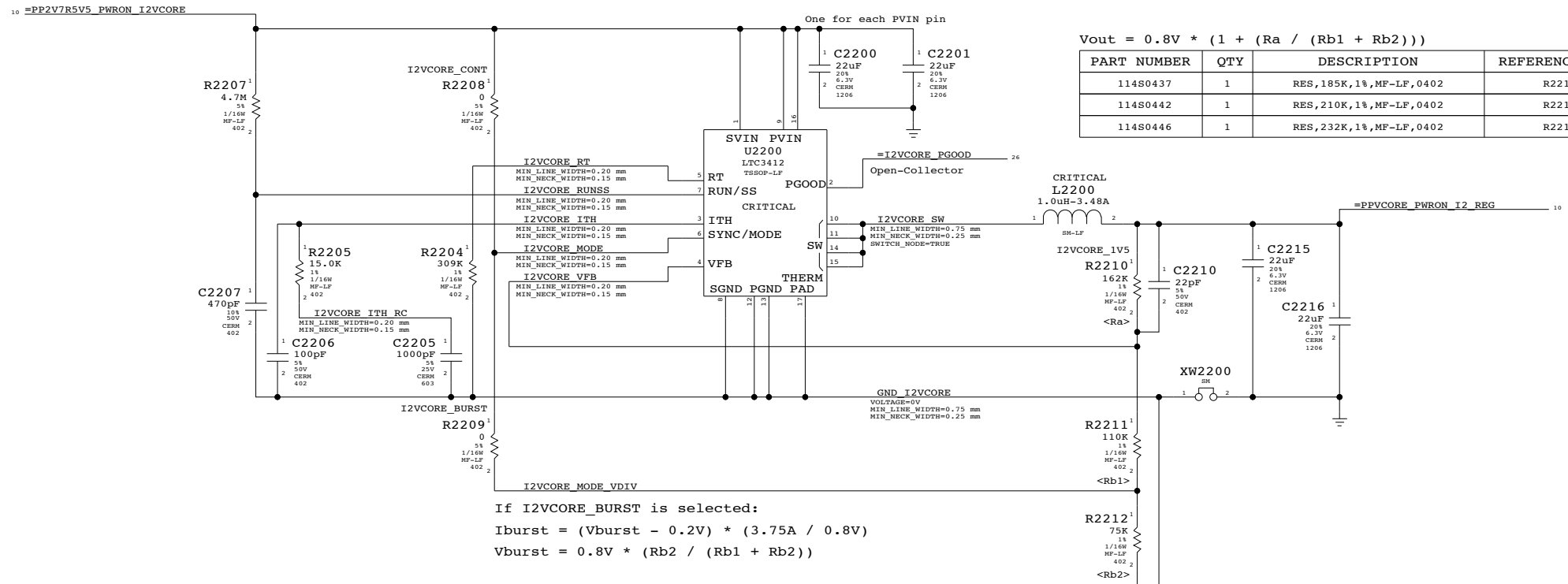
Page Notes

Power aliases required by this page:
 - =PP2V7R5V5_PWRON_I2VCORE
 - =PPVCORE_PWRON_I2_REG
 - =PPVIN_PWRON_I2PLLVD
 - =PP1V5_PWRON_I2PLLVD_LDO

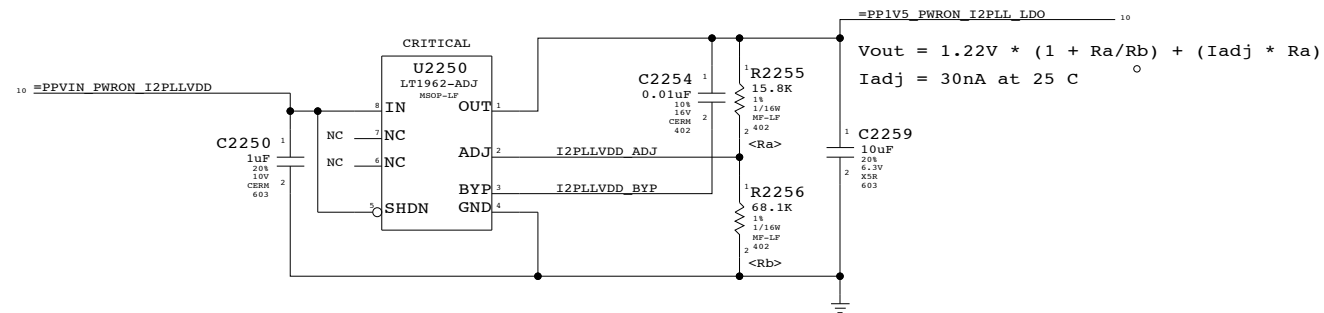
Signal aliases required by this page:
 - =I2VCORE_PGOOD

BOM options provided by this page:
 - I2VCORE_CONT / I2VCORE_BURST
 Selects between forced continuous and burst mode for LTC3412 regulator.
 - I2VCORE_xv
 Selects appropriate resistor for the indicated LTC3412 output voltage.

I2 VCore Regulator



I2 PLL LDO



I2 Power Supplies
 SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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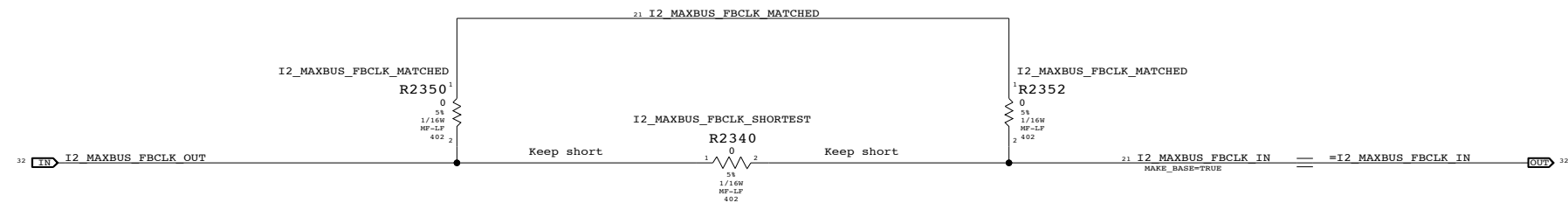
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6839	02
SCALE	SHT	OF	
NONE	22	115	

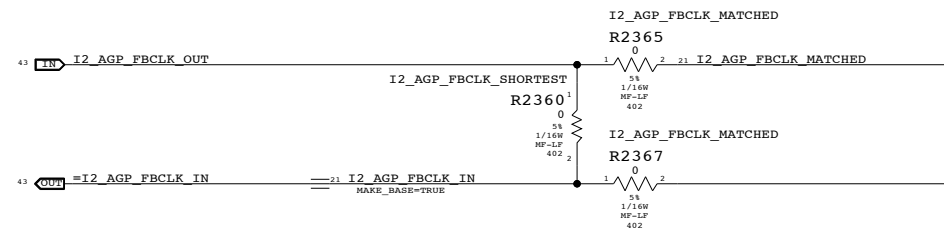
ELECTRICAL_CONSTRAINT_SET	NET_TYPE	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
	I2_FBCLK	12	I2_FBCLK	
	I2_FBCLK	12	I2_FBCLK	
	I2_FBCLK	12	I2_FBCLK	
	I2_FBCLK	12	I2_FBCLK	
H105	I2_FBCLK	12	I2_FBCLK	
H105	I2_FBCLK	12	I2_FBCLK	
H115	CLOCK	CLOCK	CLOCK	
H120	CLOCK	CLOCK	CLOCK	

I2_MAXBUS_FBCLK_IN	21
I2_MAXBUS_FBCLK_MATCHED	21
I2_AGP_FBCLK_IN	21
I2_AGP_FBCLK_MATCHED	21
I2_PCI_FBCLK_IN	21
I2_PCI_FBCLK_MATCHED	21
=CLK33M_TBEN_SYNC	11 21
=SYSCLK_TBEN_SYNC	11 21

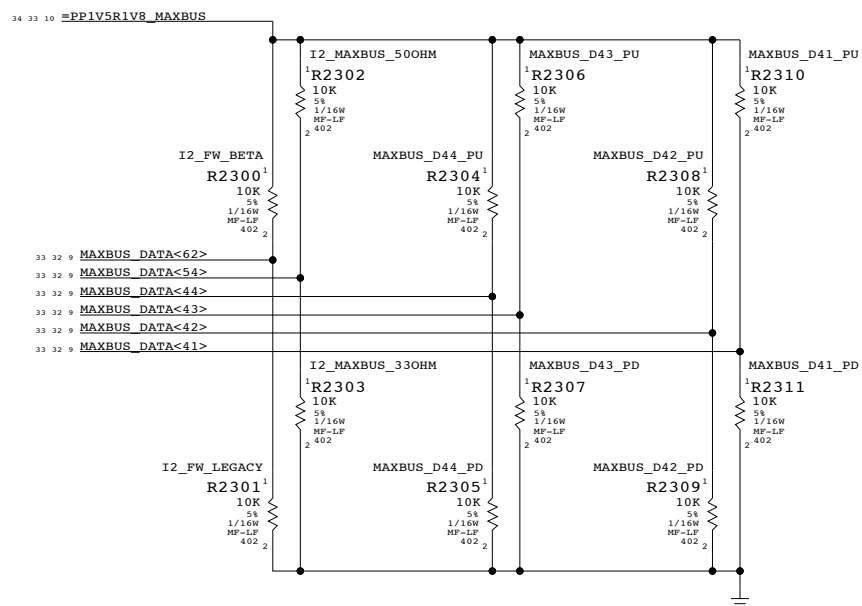
MaxBus Feedback Clock Network



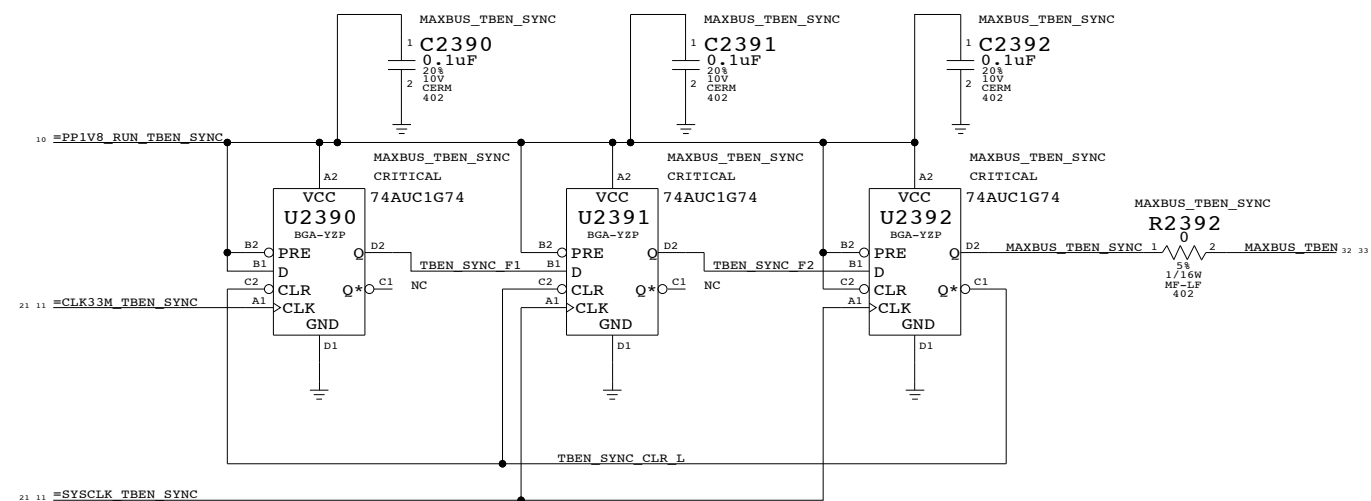
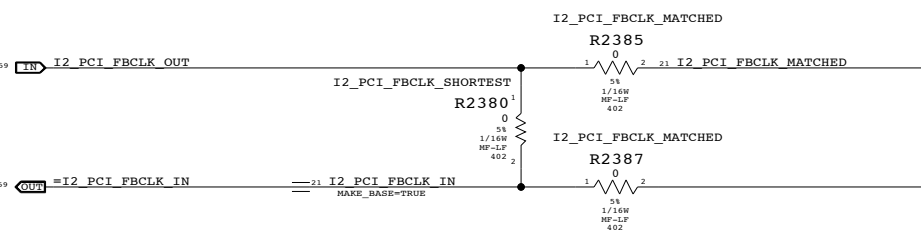
AGP Feedback Clock Ladder



I2 Configuration Straps



PCI Feedback Clock Ladder



Signal	Tied	Description
MAXBUS_DATA<62>	HIGH	1394b Support (Beta Mode)
	LOW	1394a Support (Legacy Mode)
MAXBUS_DATA<54>	HIGH	50-Ohm MaxBus Drivers
	LOW	33-Ohm MaxBus Drivers
MAXBUS_DATA<44:41>		See Table Below

BOM GROUP	Tied	Description	BOM OPTIONS
I2_MAXBUS_133MHZ	0000	133.12MHz CPU / 266.24MHz DDR	MAXBUS_D44_PD,MAXBUS_D43_PD,MAXBUS_D42_PD,MAXBUS_D41_PD
I2_MAXBUS_150MHZ	1000	149.76MHz CPU / 299.52MHz DDR	MAXBUS_D44_PU,MAXBUS_D43_PD,MAXBUS_D42_PD,MAXBUS_D41_PD
I2_MAXBUS_166MHZ	0100	166.40MHz CPU / 332.80MHz DDR	MAXBUS_D44_PD,MAXBUS_D43_PU,MAXBUS_D42_PD,MAXBUS_D41_PD
I2_MAXBUS_172MHZ	1100	171.95MHz CPU / 342.90MHz DDR	MAXBUS_D44_PU,MAXBUS_D43_PU,MAXBUS_D42_PD,MAXBUS_D41_PD
I2_MAXBUS_177MHZ	0010	177.49MHz CPU / 354.98MHz DDR	MAXBUS_D44_PD,MAXBUS_D43_PD,MAXBUS_D42_PU,MAXBUS_D41_PD
I2_MAXBUS_183MHZ	1010	183.04MHz CPU / 366.08MHz DDR	MAXBUS_D44_PU,MAXBUS_D43_PD,MAXBUS_D42_PU,MAXBUS_D41_PD
I2_MAXBUS_189MHZ	0110	188.59MHz CPU / 377.18MHz DDR	MAXBUS_D44_PD,MAXBUS_D43_PU,MAXBUS_D42_PU,MAXBUS_D41_PD
I2_MAXBUS_194MHZ	1110	194.13MHz CPU / 388.26MHz DDR	MAXBUS_D44_PU,MAXBUS_D43_PU,MAXBUS_D42_PU,MAXBUS_D41_PD
I2_MAXBUS_200MHZ	0001	199.68MHz CPU / 399.36MHz DDR	MAXBUS_D44_PD,MAXBUS_D43_PD,MAXBUS_D42_PD,MAXBUS_D41_PU

I2 Supplemental

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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	D	051-6839	02
SCALE	SHT	OF	REV.
NONE	23	115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
I280_DTT	I280	128	128	I280_DEV_TO_SB_DTT
I280_DTO	I280	128	128	I280_SB_TO_DEV_DTO_R
I280_MCLK	I280	128	128	I280_MCLK_R
I280_BITCLK	I280	128	128	I280_BITCLK_R
I280_SYNC	I280	128	128	I280_SYNC_R
I281_DTT	I281	128	128	I281_DEV_TO_SB_DTT
I281_DTO	I281	128	128	I281_SB_TO_DEV_DTO_R
I281_MCLK	I281	128	128	I281_MCLK_R
I281_BITCLK	I281	128	128	I281_BITCLK_R
I281_SYNC	I281	128	128	I281_SYNC_R
I2_CLK18M_XOUT_R	XTAL	XTAL	XTAL	I2_CLK18M_XOUT_R
I2_CLK18M_XOUT	XTAL	XTAL	XTAL	I2_CLK18M_XOUT
I2_CLK18M_XIN	XTAL	XTAL	XTAL	I2_CLK18M_XIN

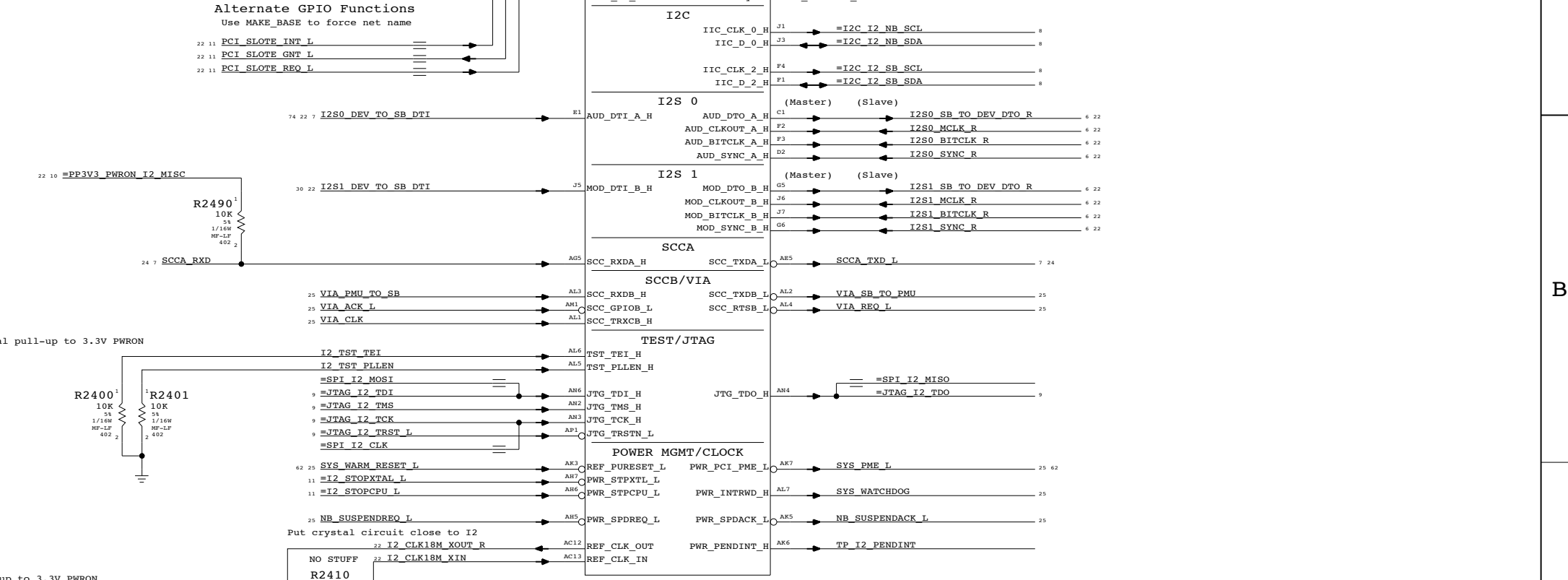
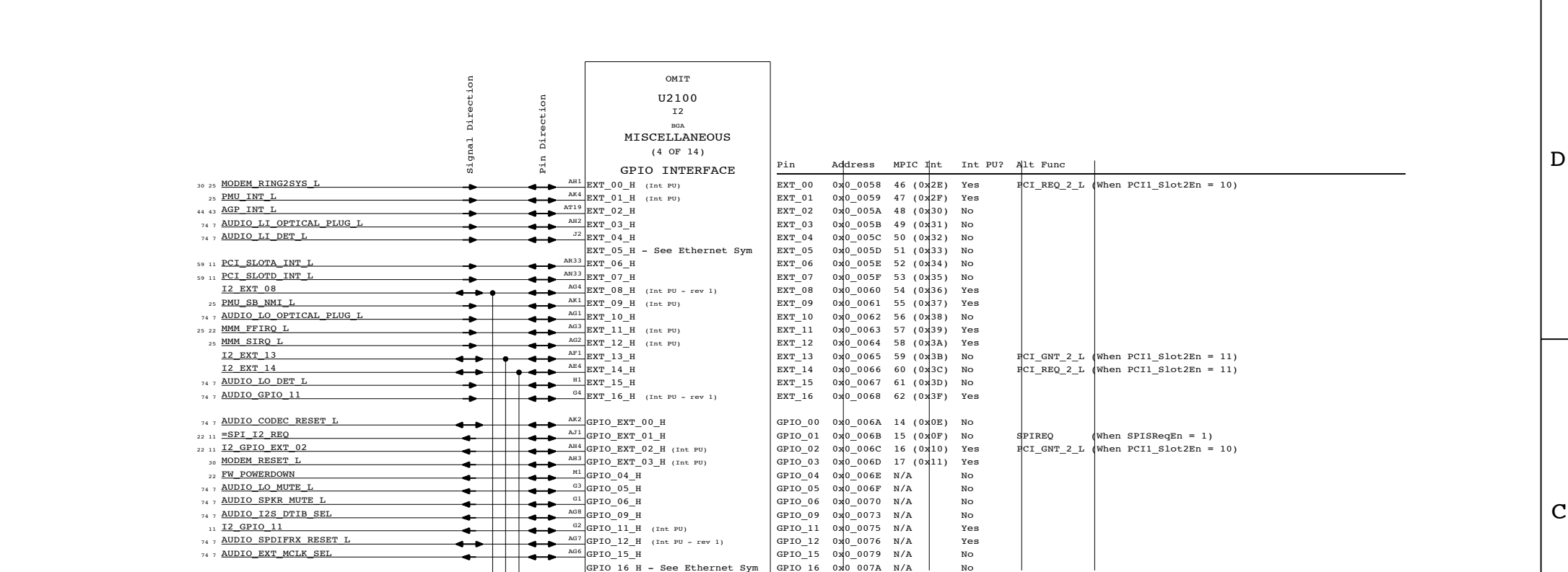
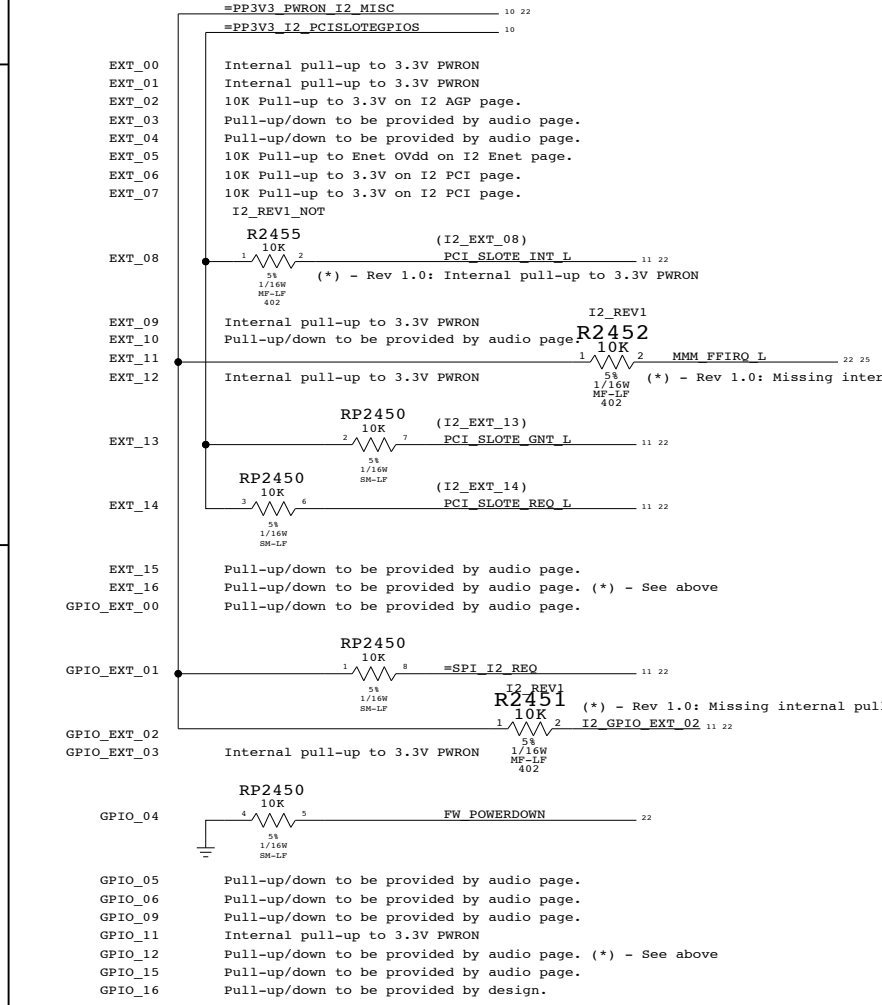
Page Notes

Power aliases required by this page:
 - =PP3V3_PWRON_I2_GPIO
 - =PP3V3_I2_PCISLOTEGPIO (PWRON or PCI)
 Should be same as =PP3V3_PCI if slot E is used, or else =PP3V3_PWRON_I2_GPIO.

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - I2_REV1_NOT
 Use for I2 revisions > 1.0

GPIO Pull-ups / Pull-downs



I2 Miscellaneous		
SYNC_MASTER=MARIAS	SYNC_DATE=06/03/2005	
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		SHEET: 24	OF: 115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		DIFFERENTIAL_PAIR
	SPACING	PHYSICAL	
PCI_ZDBOUT0	CLOCK	CLOCK	
PCI_ZDBOUT1	CLOCK	CLOCK	
PCI_ZDBOUT2	CLOCK	CLOCK	
PCI_ZDBOUT3	CLOCK	CLOCK	

```

=PCI_CLK33M_ZDB_IN 11 23
=PCI_CLK33M_ZDBOUT_R<0> 11 23
=PCI_CLK33M_ZDBOUT_R<1> 11 23
=PCI_CLK33M_ZDBOUT_R<2> 11 23
=PCI_CLK33M_ZDBOUT_R<3> 11 23

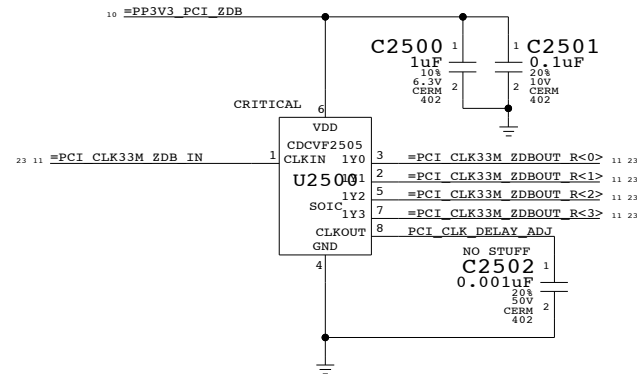
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Page Notes

Power aliases required by this page:
- =PP3V3_PWRON_I2_GPIO
- =PP3V3_I2_PCISLOTEGPIO (PWRON or PCI)
Should be same as =PP3V3_PCI if slot E is used, or else =PP3V3_PWRON_I2_GPIO.

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- I2_REV1_NOT
Use for I2 revisions > 1.0



PCI Clock Buffer

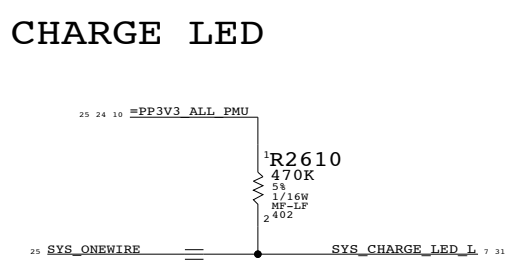
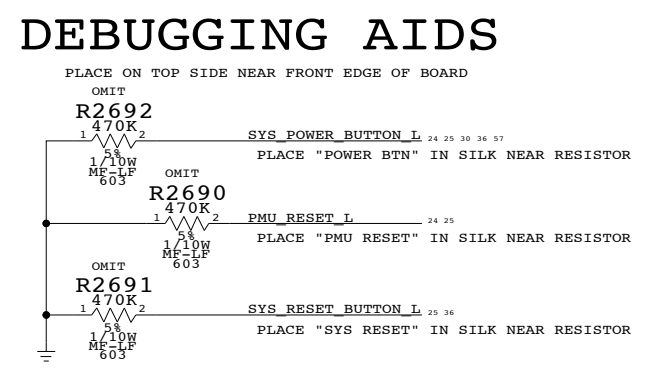
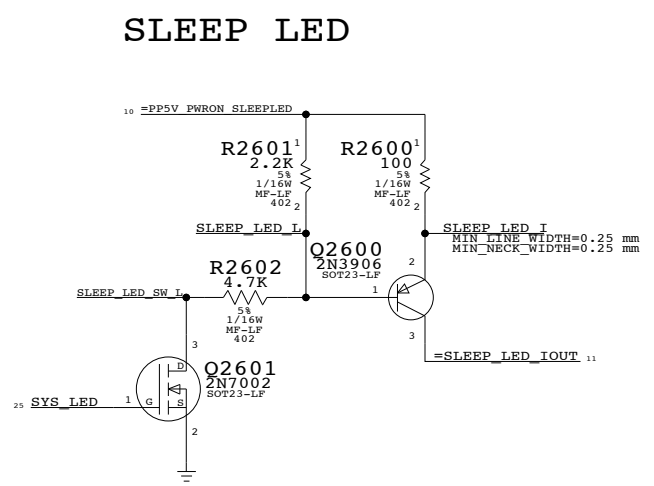
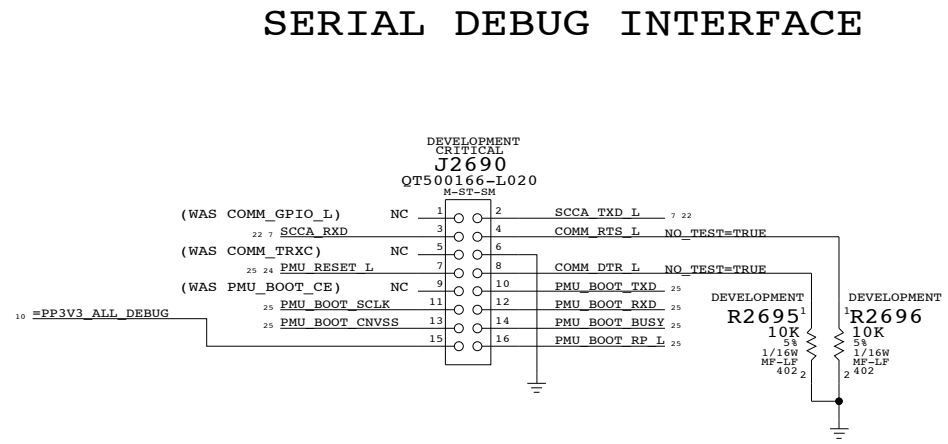
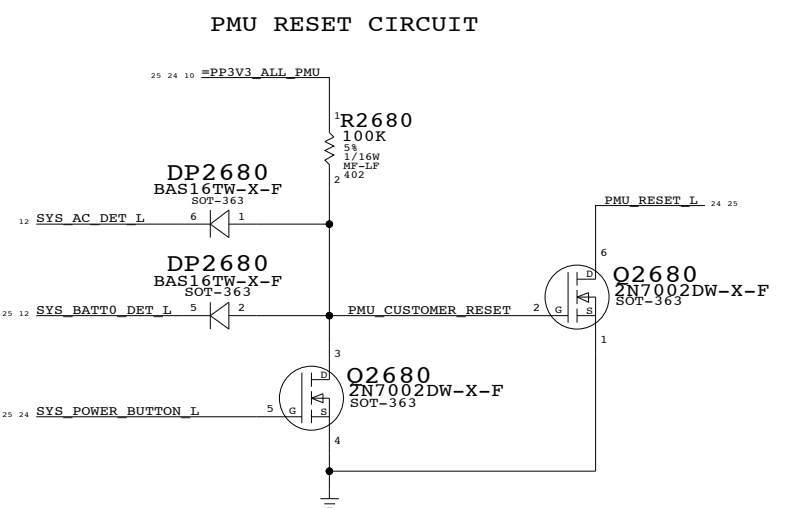
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SCALE	SHT OF		
NONE	25 OF		115



LEDs/Reset/Debug

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	D	051-6839	02
SCALE	SHT	OF	
NONE	26	115	

Power Management Unit

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		SPACING	PHYSICAL	DIFFERENTIAL_PAIR
PMU_CLK10M_XTAL	XTAL		XTAL	PMU_CLK10M_XIN
	XTAL		XTAL	PMU_CLK10M_XOUT
	XTAL		XTAL	PMU_CLK10M_XOUT_R
PMU_CLK32K_XTAL	XTAL		XTAL	PMU_CLK32K_XIN
	XTAL		XTAL	PMU_CLK32K_XOUT
	XTAL		XTAL	PMU_CLK32K_XOUT_R

Page Notes

Power aliases required by this page:

- =PP3V3_ALL_PMU
- =PP3V3_PWRON_PMU
- =PPVREF_PMU (PMU AVCC or 2.5V reference)

Signal aliases required by this page:

- =I2C_PMU_SCL
- =I2C_PMU_SDA
- =I2C_PMU_SMB_SCL
- =I2C_PMU_SMB_SDA
- =JTAG_BBANGER_TCK
- =JTAG_BBANGER_TDI
- =JTAG_BBANGER_TMS
- =JTAG_BBANGER_TRST_L

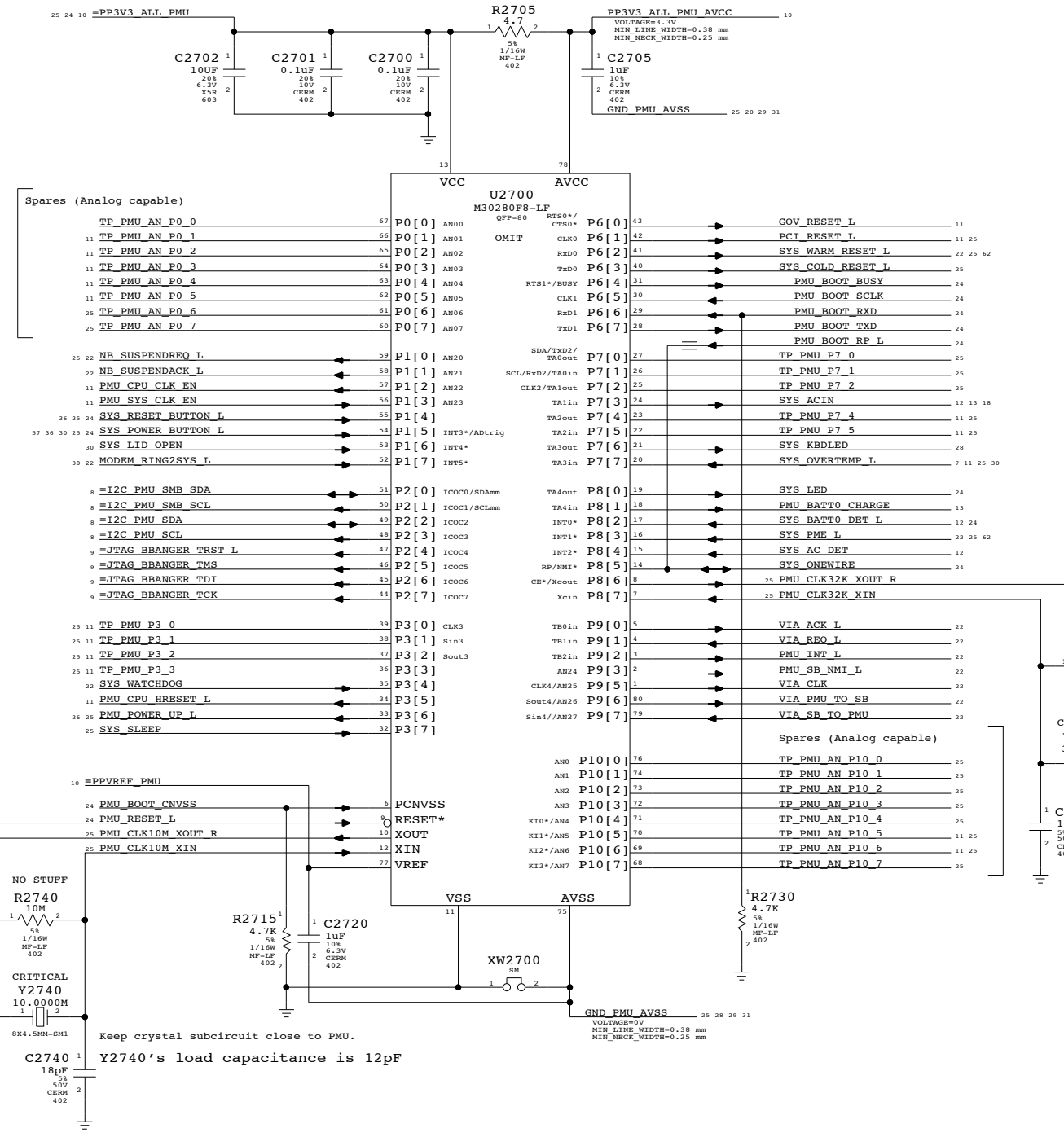
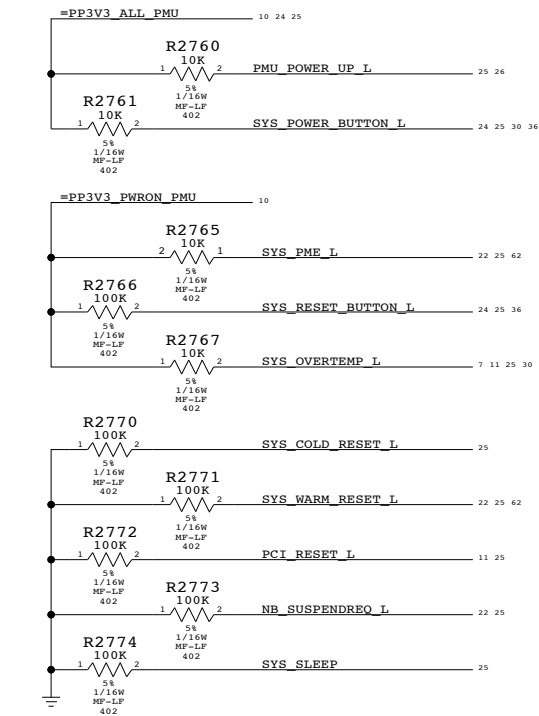
NOTE: Boot-banger pins can be aliased to TP_ or NC_ if not implemented.

BOM options provided by this page: (NONE)

NOTE: TP_PMU_Fx_x signals are general-purpose spares. Some pins are reserved for alternate functions. TP_PMU_AN_Fx_x signals are general-purpose spares that can also be used as analog inputs.

NOTE: All analog inputs to PMU should have a 100pF capacitor to the PMU AVSS signal (GND_PMU_AVSS). None of those capacitors are provided on this page.

PMU Pull-ups / pull-downs



Additional PMU05 "Modules"

MMM	ALS	SPI Dual Battery Charger	Battery Current Mon
TP_PMU_AN_P10_0	TP_PMU_AN_P10_3	TP_PMU_P3_0	TP_PMU_AN_P10_7
TP_PMU_AN_P10_1	TP_PMU_AN_P10_4	TP_PMU_P3_1	
TP_PMU_AN_P10_2	TP_PMU_P7_2	TP_PMU_P3_2	
TP_PMU_P7_0		TP_PMU_P3_3	
TP_PMU_P7_1		TP_PMU_P7_4	
TP_PMU_AN_P0_7		TP_PMU_P7_5	
TP_PMU_AN_P0_6			

Power Management Unit (PMU05)

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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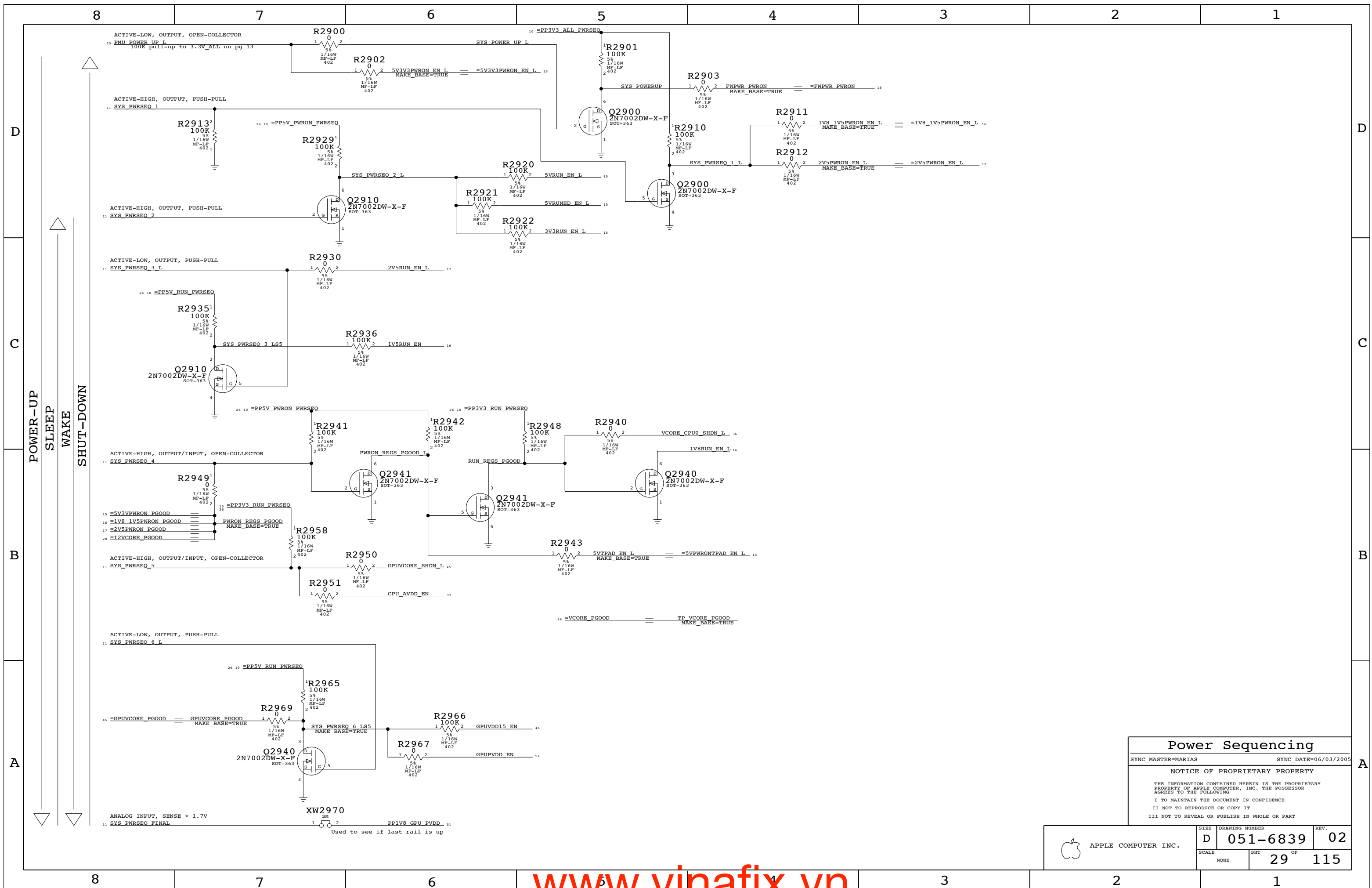
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		SHEET: 27	OF: 115



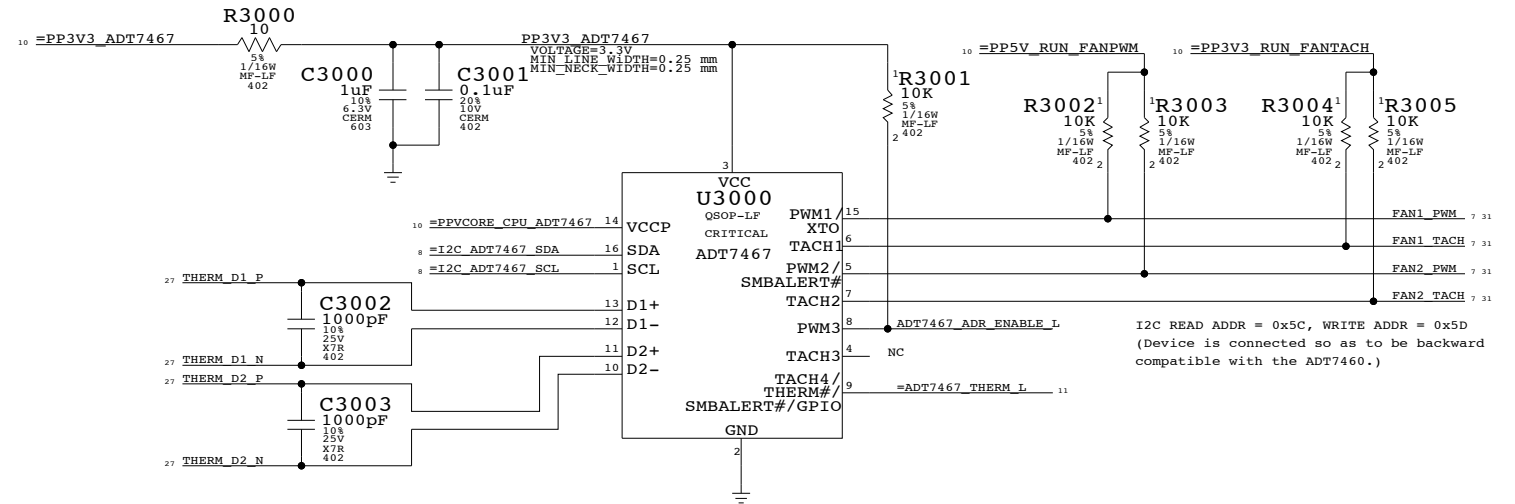
POWER-UP
SLEEP
WAKE
SHUT-DOWN

Power Sequencing
 SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005
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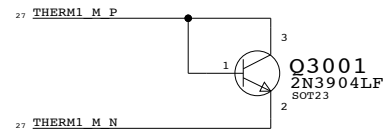
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	NONE	051-6839	02
SCALE		SHT	OF
NONE		29	115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			DIFFERENTIAL_PAIR
	SPACING	PHYSICAL		
E520	THERM	THERM	THERM1_M	THERM1_M_P
E520	THERM	THERM	THERM1_M	THERM1_M_N
E530	THERM	THERM	THERM2_M	THERM2_M_P
E530	THERM	THERM	THERM2_M	THERM2_M_N
E532	THERM	THERM	THERM1_A	THERM1_A_P
E532	THERM	THERM	THERM1_A	THERM1_A_N
E532	THERM	THERM	THERM2_A	THERM2_A_P
E532	THERM	THERM	THERM2_A	THERM2_A_N
E532	THERM	THERM	THERM_D1	THERM_D1_P
E532	THERM	THERM	THERM_D1	THERM_D1_N
E532	THERM	THERM	THERM_D2	THERM_D2_P
E532	THERM	THERM	THERM_D2	THERM_D2_N

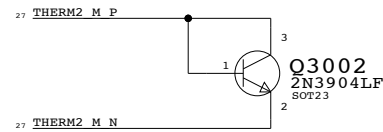
FAN CONTROLLER



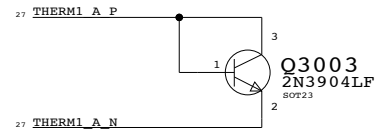
PLACE CLOSE TO CPU MAIN1



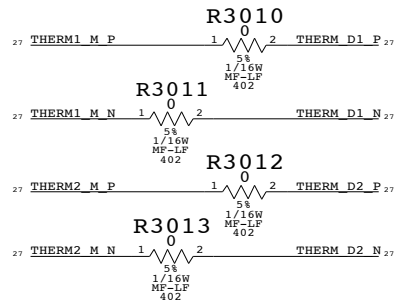
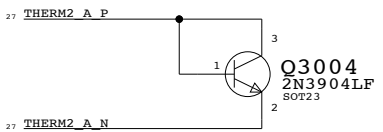
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY MAIN2



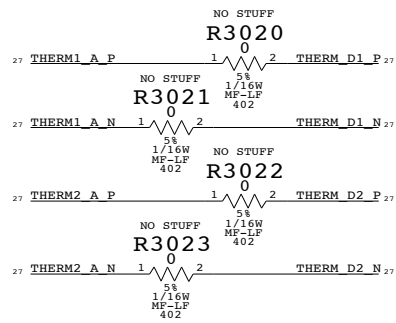
PLACE UNDERNEATH UPPER RAM ALTERNATE1



PLACE CLOSE TO BATTERY CHARGER/VCORE ALTERNATE2

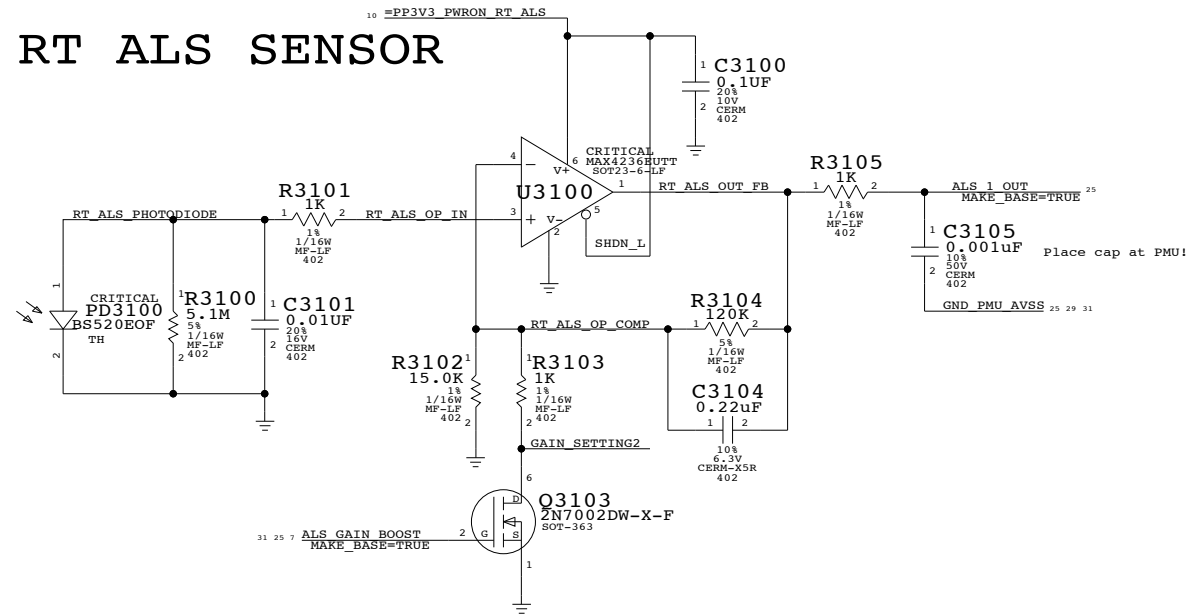


KEEP STUFFING RESISTORS CLOSE TO ADT7467 CONTROLLER



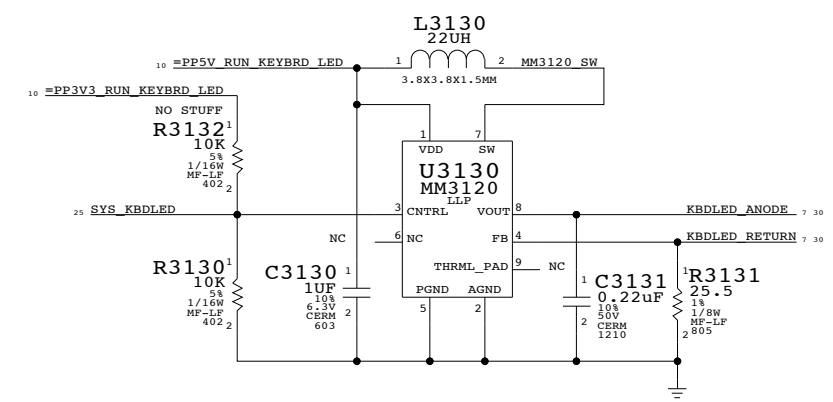
Fan Controller
 SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005
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SCALE	SHT	OF	
NONE	30	115	



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0856	353S0504	?	U3100	

Keyboard LED Driver



ALS Support

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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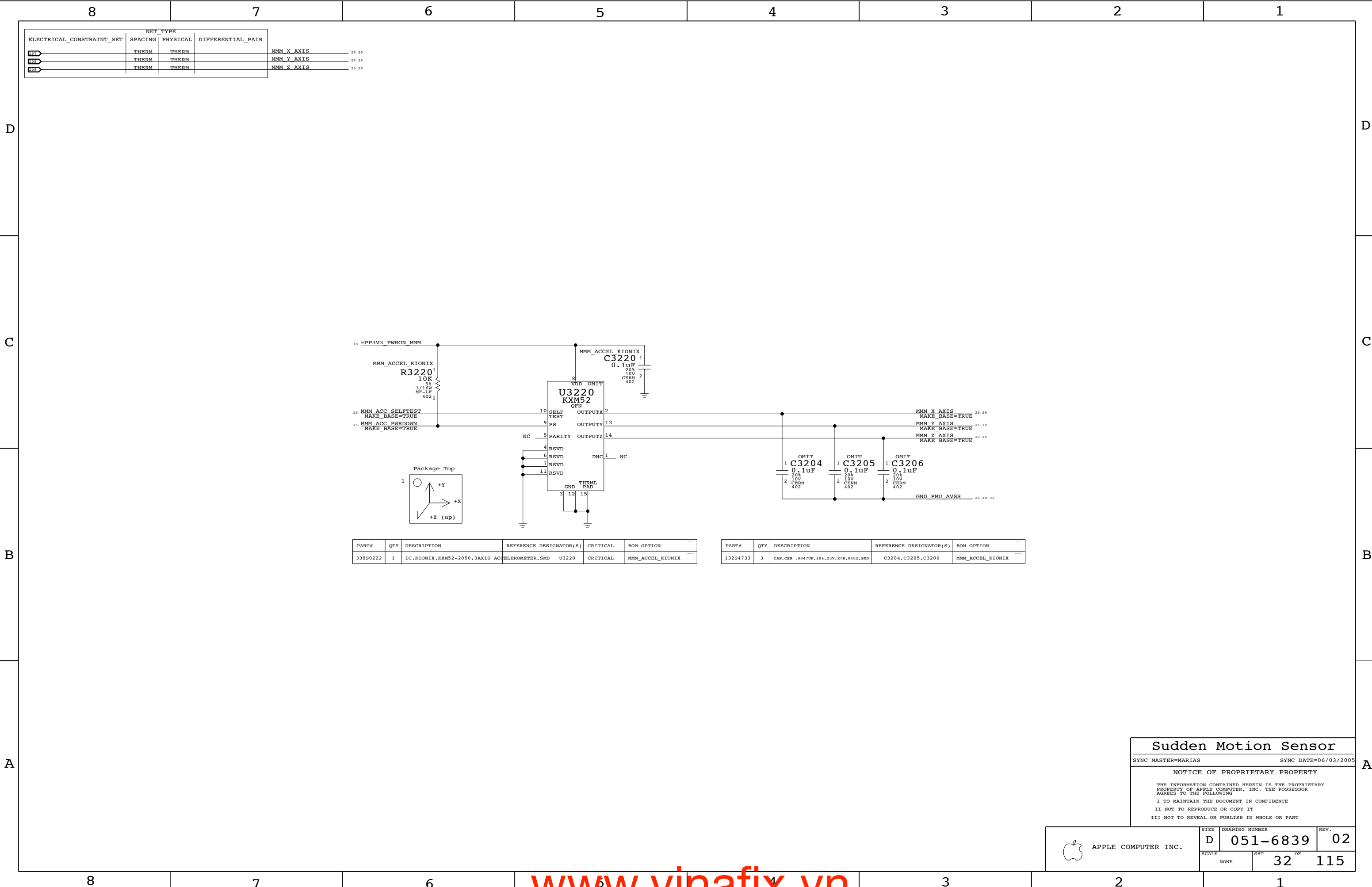
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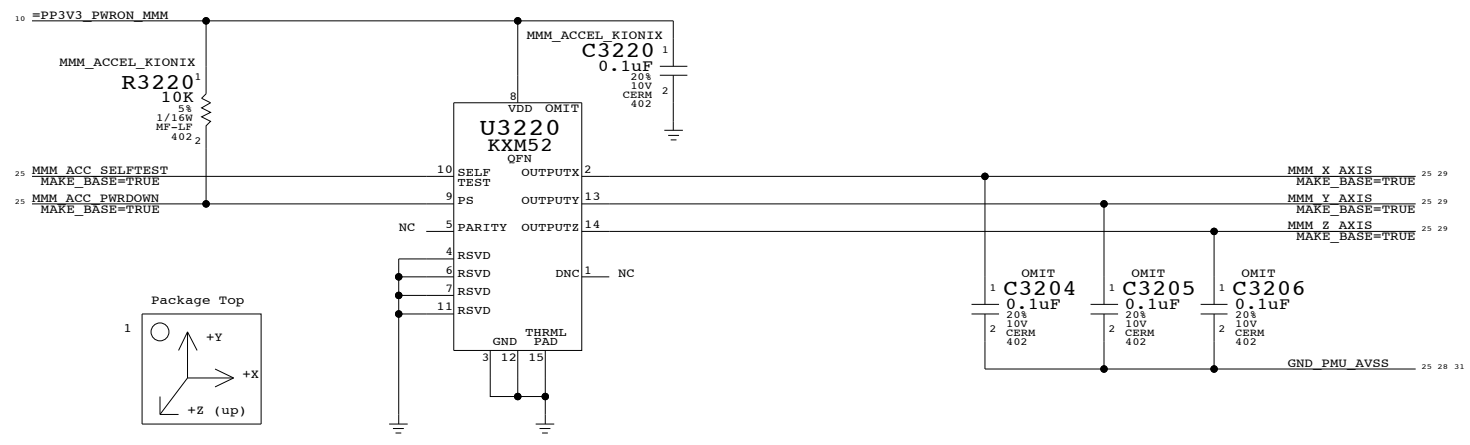
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6839	02
SCALE	SHT	OF	
NONE	31	115	



ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
E57	THERM	THERM	MMM_X_AXIS 25 29
E58	THERM	THERM	MMM_Y_AXIS 25 29
E59	THERM	THERM	MMM_Z_AXIS 25 29



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33880222	1	IC, KIONIX, KXM52-2050, 3AXIS ACCELEROMETER, SMD	U3220	CRITICAL	MMM_ACCEL_KIONIX

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
13284733	3	CAP, CER .0047UF, 10%, 25V, X7R, 0402, SMD	C3204, C3205, C3206	MMM_ACCEL_KIONIX

Sudden Motion Sensor

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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	D	051-6839	02
SCALE	SHT OF		
NONE	32 OF		115

8

7

6

5

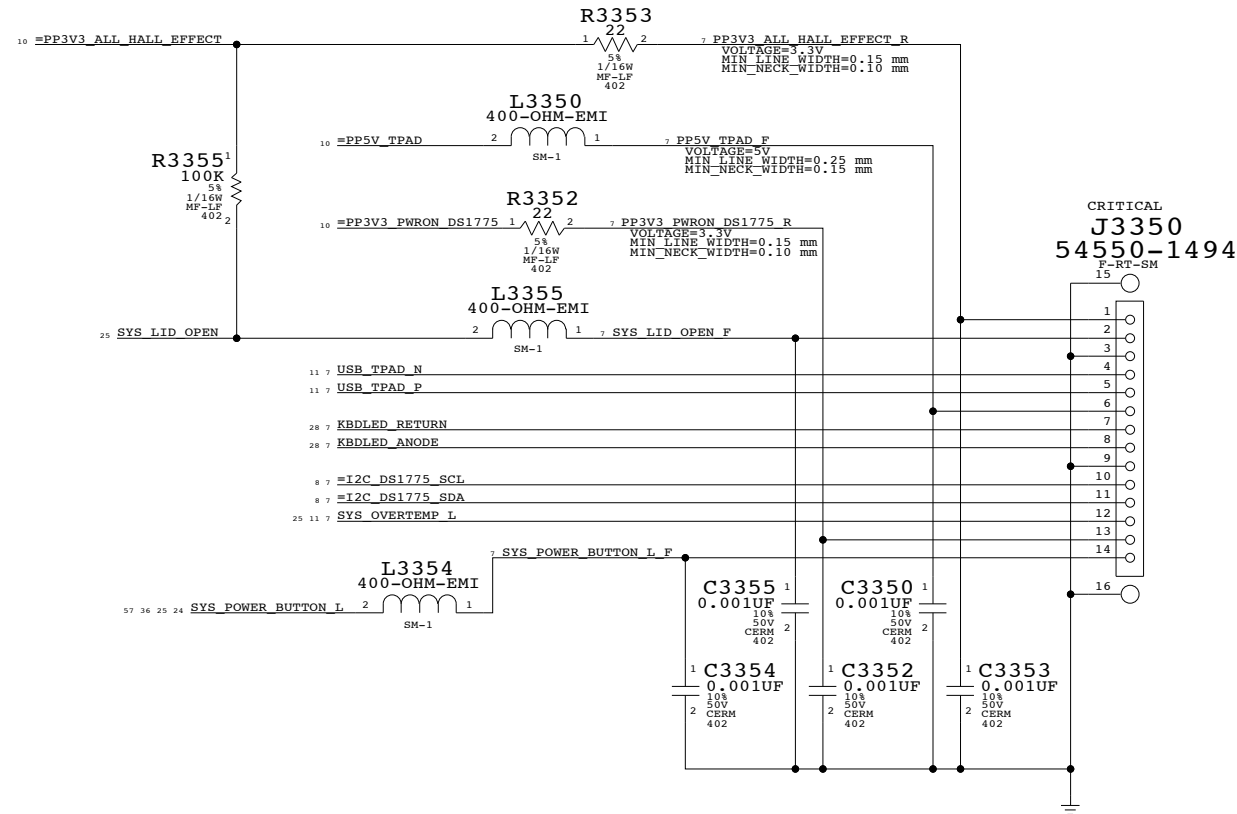
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3

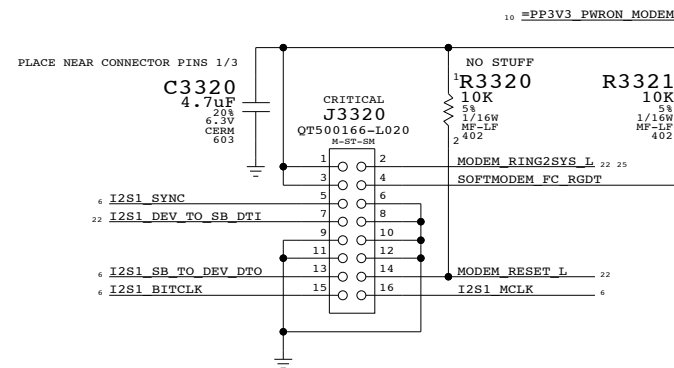
2

1

USB Trackpad Conn



SOFT MODEM CONN



Q41C Internal I/O I

SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-6839	02
SCALE	NONE	SHT	OF
		33	115

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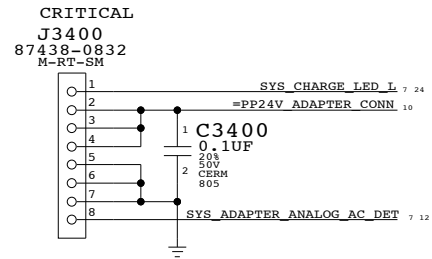
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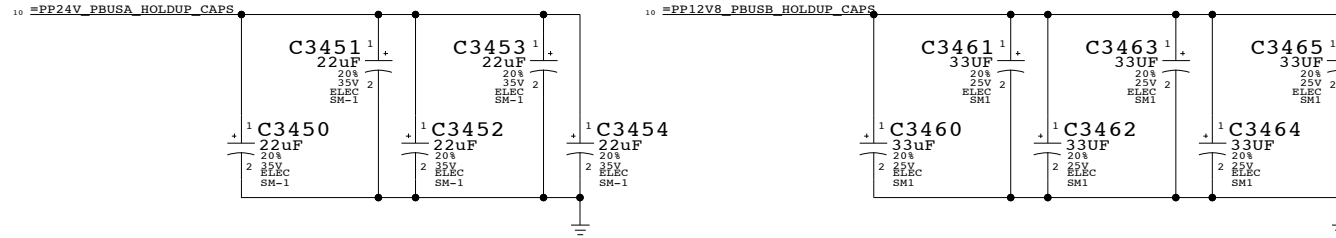
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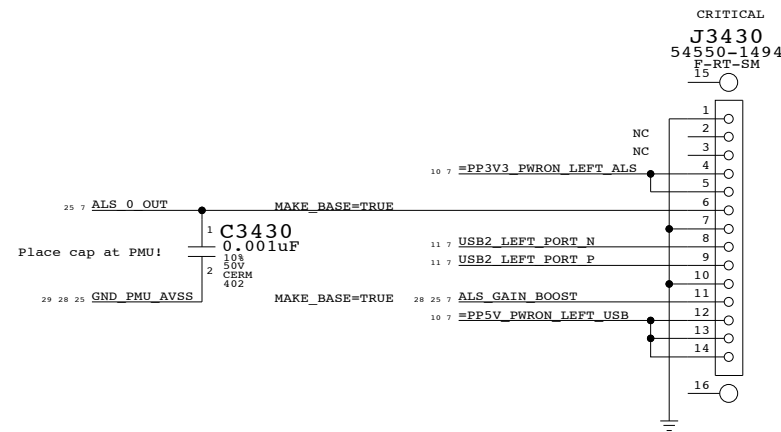
ADAPTER CONNECTOR



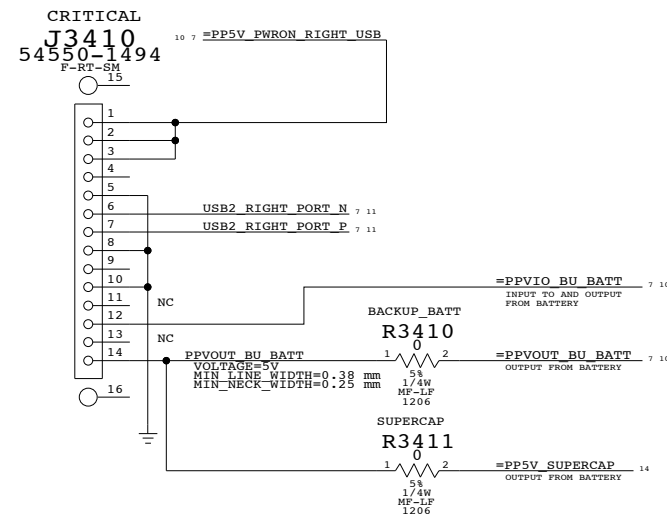
PBUS HOLD-UP CAPS



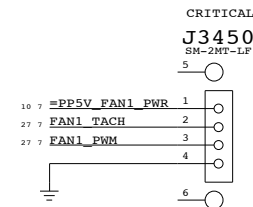
LEFT USB/LEFT ALS



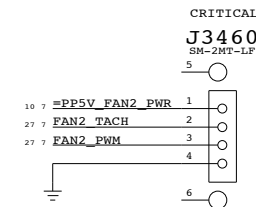
BACKUP BATTERY / RT USB CONNECTOR



CPU FAN



GPU FAN



Q41C Internal I/O II

SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-6839	02
SCALE	NONE	SHT	OF
		34	115

8

7

6

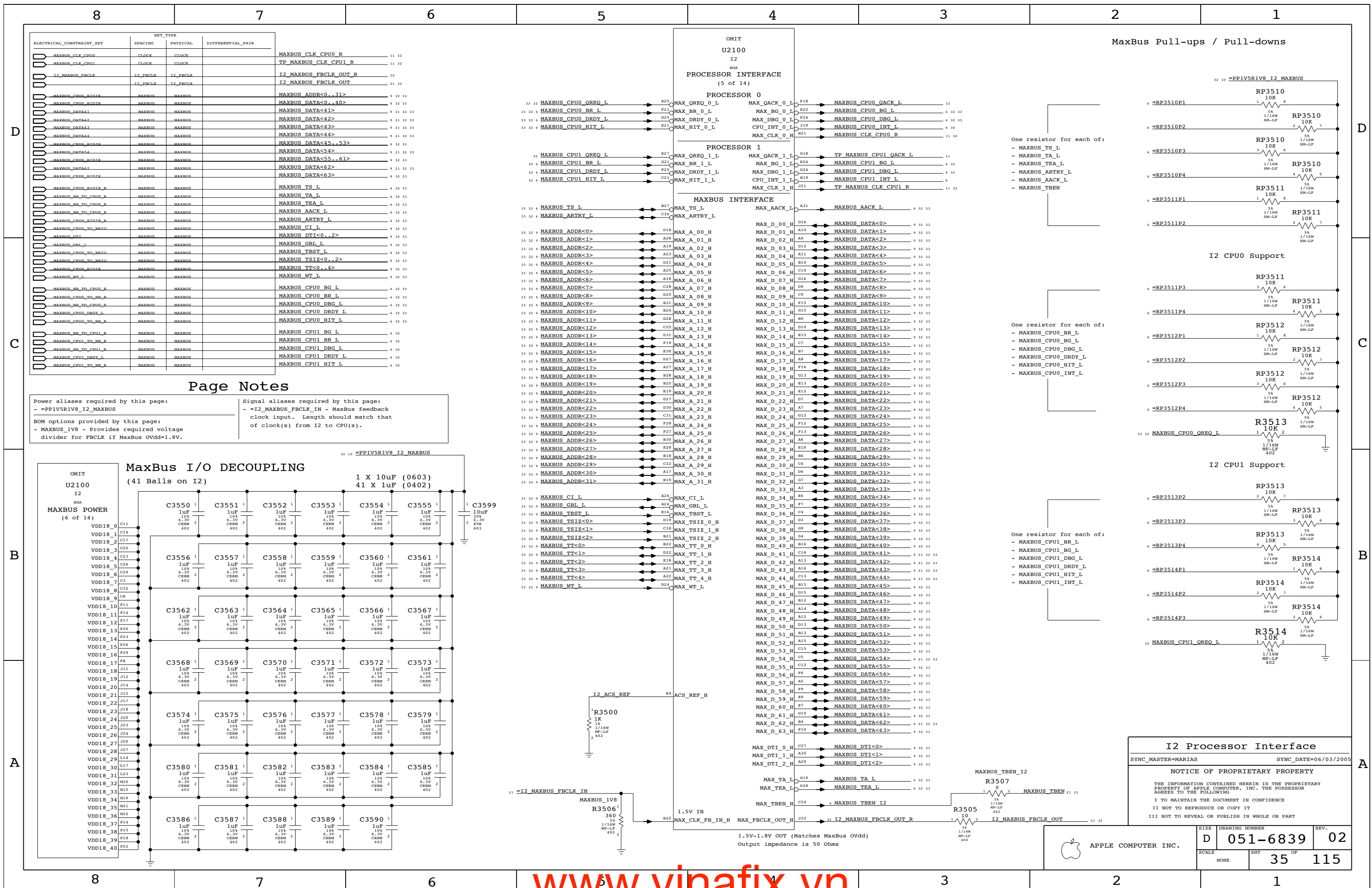
5

4

3

2

1



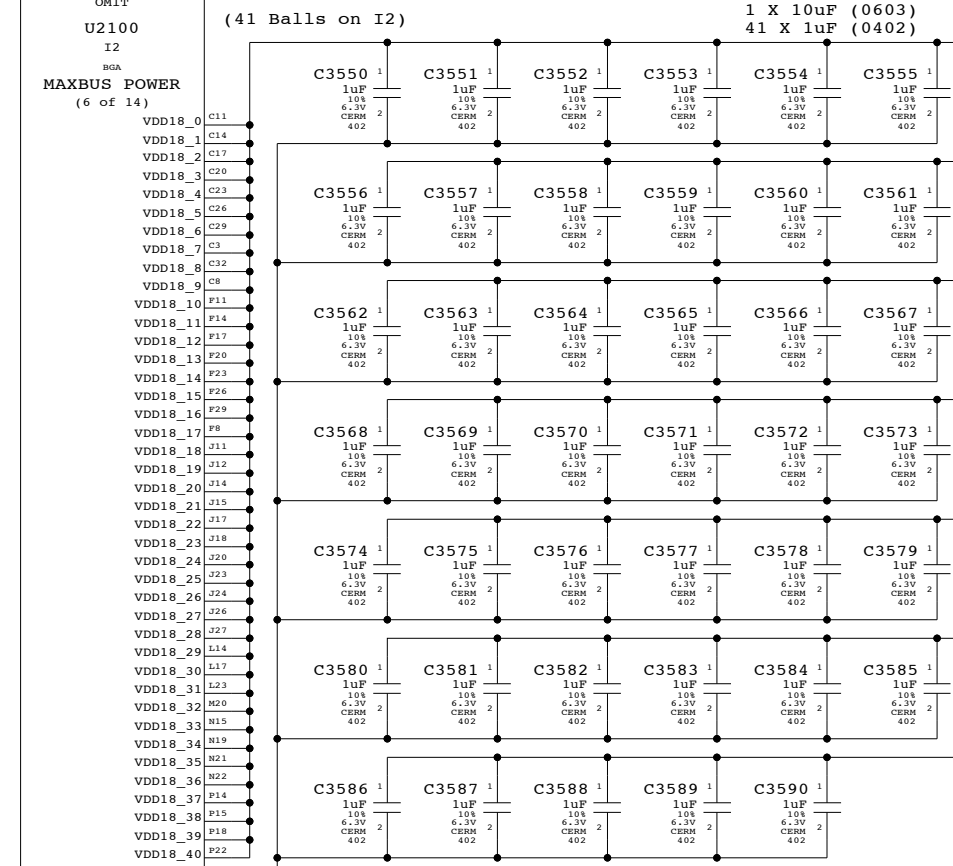
Page Notes

Power aliases required by this page:
 - =PP1V5R1V8_I2_MAXBUS

BOM options provided by this page:
 - MAXBUS_1V8 - Provides required voltage divider for FBCLK if MaxBus OVdd=1.8V.

Signal aliases required by this page:
 - =I2_MAXBUS_FBCLK_IN - MaxBus feedback clock input. Length should match that of clock(s) from I2 to CPU(s).

MaxBus I/O DECOUPLING



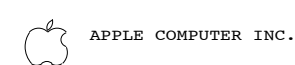
I2 Processor Interface

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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SCALE	SHT	OF
NONE	35	115



ELECTRICAL_CONSTRAINT_SET	NET_TYPE	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
8022	CLOCK	CLOCK		

Page Notes

Power aliases required by this page:
 - =PP1V5R1V8_MAXBUS

Signal aliases required by this page:
 - =MAXBUS_CPU0_CLK

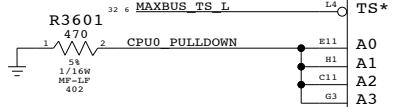
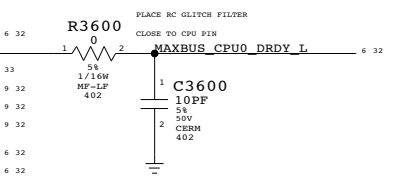
BOM options provided by this page:
 (NONE)

- 32 9 MAXBUS_DATA<0> R15 D0
- 32 9 MAXBUS_DATA<1> M15 D1
- 32 9 MAXBUS_DATA<2> T14 D2
- 32 9 MAXBUS_DATA<3> V16 D3
- 32 9 MAXBUS_DATA<4> W16 D4
- 32 9 MAXBUS_DATA<5> T15 D5
- 32 9 MAXBUS_DATA<6> U15 D6
- 32 9 MAXBUS_DATA<7> P14 D7
- 32 9 MAXBUS_DATA<8> V13 D8
- 32 9 MAXBUS_DATA<9> W13 D9
- 32 9 MAXBUS_DATA<10> T13 D10
- 32 9 MAXBUS_DATA<11> P13 D11
- 32 9 MAXBUS_DATA<12> U14 D12
- 32 9 MAXBUS_DATA<13> W14 D13
- 32 9 MAXBUS_DATA<14> R12 D14
- 32 9 MAXBUS_DATA<15> T12 D15
- 32 9 MAXBUS_DATA<16> W12 D16
- 32 9 MAXBUS_DATA<17> V12 D17
- 32 9 MAXBUS_DATA<18> M11 D18
- 32 9 MAXBUS_DATA<19> M10 D19
- 32 9 MAXBUS_DATA<20> R11 D20
- 32 9 MAXBUS_DATA<21> U11 D21
- 32 9 MAXBUS_DATA<22> M11 D22
- 32 9 MAXBUS_DATA<23> T11 D23
- 32 9 MAXBUS_DATA<24> R10 D24
- 32 9 MAXBUS_DATA<25> M9 D25
- 32 9 MAXBUS_DATA<26> P10 D26
- 32 9 MAXBUS_DATA<27> U10 D27
- 32 9 MAXBUS_DATA<28> R9 D28
- 32 9 MAXBUS_DATA<29> W10 D29
- 32 9 MAXBUS_DATA<30> U9 D30
- 32 9 MAXBUS_DATA<31> V9 D31
- 32 9 MAXBUS_DATA<32> W5 D32
- 32 9 MAXBUS_DATA<33> U6 D33
- 32 9 MAXBUS_DATA<34> T5 D34
- 32 9 MAXBUS_DATA<35> U5 D35
- 32 9 MAXBUS_DATA<36> W7 D36
- 32 9 MAXBUS_DATA<37> R6 D37
- 32 9 MAXBUS_DATA<38> P7 D38
- 32 9 MAXBUS_DATA<39> V6 D39
- 32 9 MAXBUS_DATA<40> P17 D40
- 32 21 MAXBUS_DATA<41> M19 D41
- 32 21 MAXBUS_DATA<42> V18 D42
- 32 21 MAXBUS_DATA<43> R18 D43
- 32 21 MAXBUS_DATA<44> V19 D44
- 32 9 MAXBUS_DATA<45> T19 D45
- 32 9 MAXBUS_DATA<46> U19 D46
- 32 9 MAXBUS_DATA<47> M19 D47
- 32 9 MAXBUS_DATA<48> U18 D48
- 32 9 MAXBUS_DATA<49> M17 D49
- 32 9 MAXBUS_DATA<50> W18 D50
- 32 9 MAXBUS_DATA<51> T18 D51
- 32 9 MAXBUS_DATA<52> T18 D52
- 32 9 MAXBUS_DATA<53> T17 D53
- 32 21 MAXBUS_DATA<54> M3 D54
- 32 9 MAXBUS_DATA<55> V17 D55
- 32 9 MAXBUS_DATA<56> U4 D56
- 32 9 MAXBUS_DATA<57> U8 D57
- 32 9 MAXBUS_DATA<58> U7 D58
- 32 9 MAXBUS_DATA<59> R7 D59
- 32 9 MAXBUS_DATA<60> P6 D60
- 32 9 MAXBUS_DATA<61> R8 D61
- 32 21 MAXBUS_DATA<62> W8 D62
- 32 9 MAXBUS_DATA<63> T8 D63

U3600
 BGA
 (2 OF 6)
 XXGHZ-XXV
 AB-X-X

OMIT
 CRITICAL

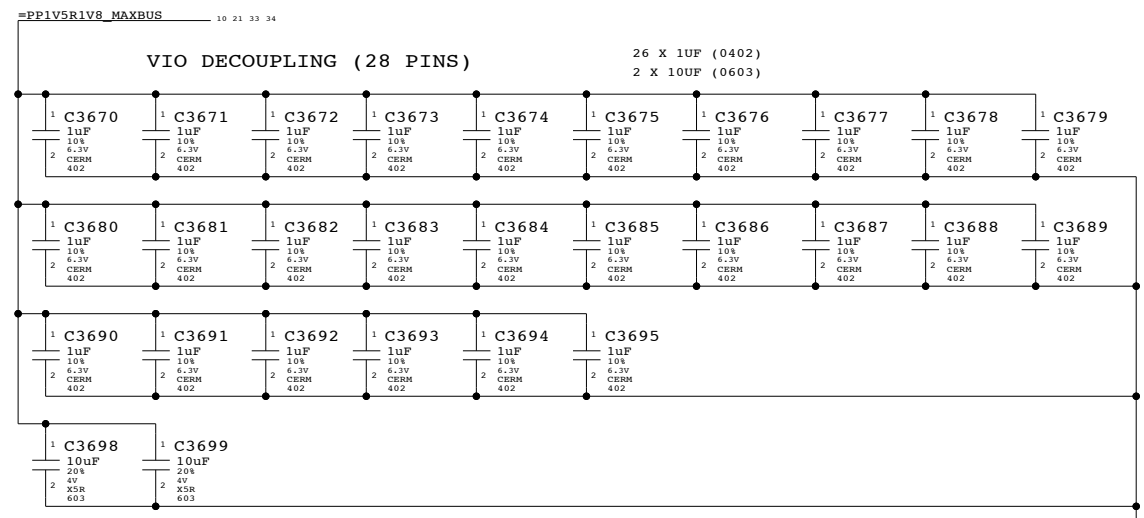
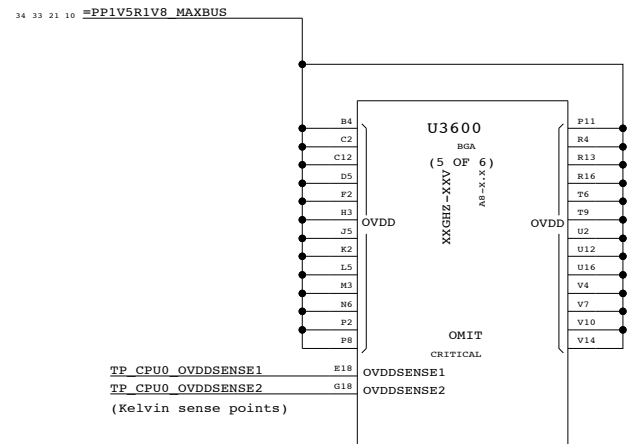
- DP0 T3 NC
- DP1 W4 NC
- DP2 T4 NC
- DP3 W9 NC
- DP4 M6 NC
- DP5 V3 NC
- DP6 N8 NC
- DP7 W6 NC
- DBG* M2 MAXBUS_CPU0_DBG_L 6 32
- DRDY* R3 MAXBUS_CPU0_DRDY_L_R 6 32
- DTIO G1 MAXBUS_EDTI 33
- DTI1 K1 MAXBUS_DTI<0> 9 32
- DTI2 P1 MAXBUS_DTI<1> 9 32
- DTI3 N1 MAXBUS_DTI<2> 9 32
- TA* K6 MAXBUS_TA_L 6 32
- TEA* L1 MAXBUS_TEA_L 6 32
- HIT* B2 MAXBUS_CPU0_HIT_L 6 32



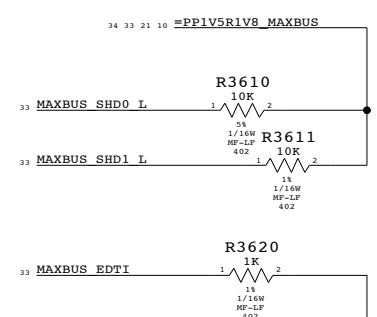
U3600
 BGA
 (1 OF 6)
 XXGHZ-XXV
 AB-X-X

OMIT
 CRITICAL

- AP0 C1 NC
- AP1 E2 NC
- AP2 H6 NC
- AP3 F5 NC
- AP4 G7 NC
- TT0 E5 MAXBUS_TT<0> 9 32
- TT1 E6 MAXBUS_TT<1> 9 32
- TT2 F6 MAXBUS_TT<2> 9 32
- TT3 E9 MAXBUS_TT<3> 9 32
- TT4 C5 MAXBUS_TT<4> 9 32
- TBST* F11 MAXBUS_TBST_L 9 32
- TSIZ0 G6 MAXBUS_TSIZ<0> 9 32
- TSIZ1 F7 MAXBUS_TSIZ<1> 9 32
- TSIZ2 E7 MAXBUS_TSIZ<2> 9 32
- GBL* B2 MAXBUS_GBL_L 9 32
- WT* D3 MAXBUS_WT_L 9 32
- CI* J1 MAXBUS_CI_L 9 32
- AACK* R1 MAXBUS_AACK_L 6 32
- ARTRY* N2 MAXBUS_ARTRY_L 6 32
- SHD0* E4 MAXBUS_SHD0_L 33
- SHD1* H5 MAXBUS_SHD1_L 33
- SYSCLK A10 =MAXBUS_CPU0_CLK 11 33
- CLK_OUT H2 TP_CPU0_CLKOUT 21 32
- TBEN E1 MAXBUS_TBEN 21 32
- QREQ* F4 MAXBUS_CPU0_QREQ_L 32
- QACK* G5 MAXBUS_CPU0_QACK_L 32
- CKSTP_IN* A3 32
- CKSTP_OUT* B1 CPU_CHKSTP_OUT_L 34



MAXBUS Straps



A8 MaxBus (CPU0)
 SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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Page Notes

Power aliases required by this page:

- =PPIV5R1V8_MAXBUS
- =PP3V3_PWRON_FLTSEL

Signal aliases required by this page:

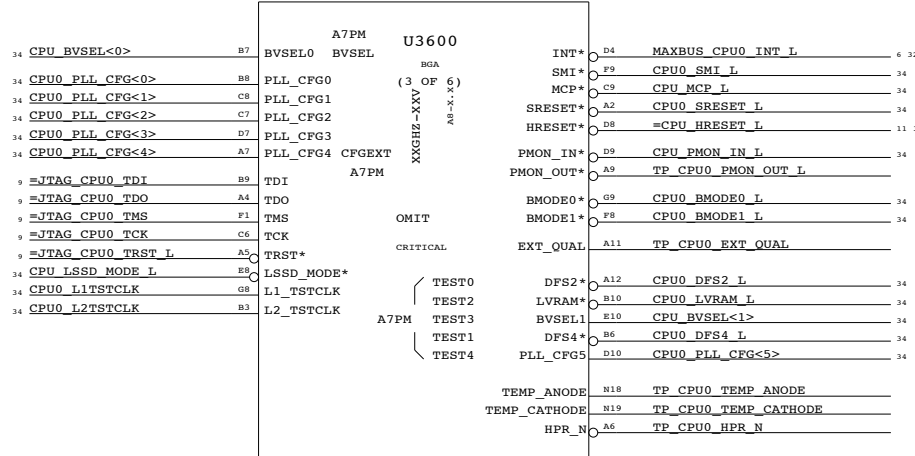
- =CPU0_JTAG_TDI
- =CPU0_JTAG_TDO
- =CPU0_JTAG_TMS
- =CPU0_JTAG_TCK
- =CPU0_JTAG_TRST_L
- =CPU_HRESET_L (Reset given to all processors)

BOM options provided by this page:

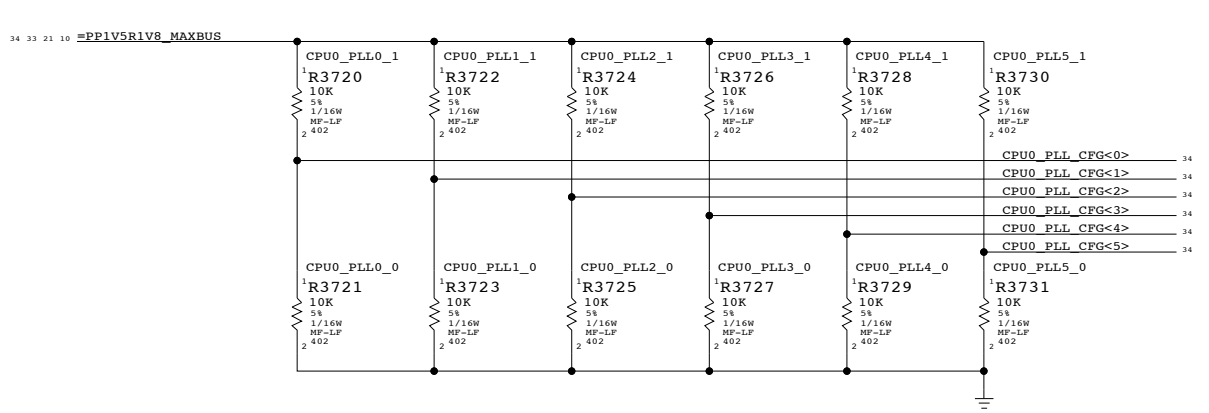
- CPU0_PLL0_0/1
- CPU0_PLL1_0/1
- CPU0_PLL2_0/1
- CPU0_PLL3_0/1
- CPU0_PLL4_0/1
- CPU0_PLL5_0/1

These must be selected to set the CPU core to Maxbus frequency ratio to attain the desired spec

- MAXBUS_1V5 - MAXBUS_1V8
- One of these must be selected to set the Maxbus voltage
- * the MAXBUS_1V5 option does not exist for A7PM
- CPU_A7PM - CPU_A8
- One of these must be selected to ensure the the above strap is interpreted correctly



CPU0 PLL CONFIG CIRCUITRY

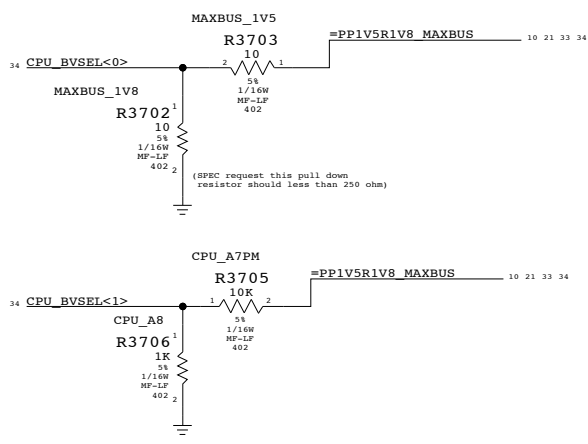


BUS TYPE SELECT

SIGNAL	TIED	MODE
CPU0_BMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE



MAXBUS VSEL



CPU0 FREQUENCY CONFIGURATION

() Indicates DFS setting supported by A8 only

BOM GROUP	DFS SUPPORT	F/2	F/4	PLL BITS 012345	BOM OPTIONS
CPU0_BUSRATIO_1.0X	-	-	-	001100	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_2.0X	-	-	-	010000	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_3.0X	-	-	-	100000	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_4.0X	2.0X	-	-	101000	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_5.0X	2.5X	-	-	101100	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_5.5X	(2.75X)	-	-	100100	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_6.0X	3.0X	-	-	110100	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_6.5X	(3.25X)	-	-	010100	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_7.0X	3.5X	-	-	001000	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_7.5X	(3.75X)	-	-	000100	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_8.0X	4.0X	2.0X	-	110000	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_8.5X	(4.25X)	-	-	011000	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_9.0X	4.5X	(2.25X)	-	011100	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_9.5X	(4.75X)	-	-	011100	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_10.0X	5.0X	2.5X	-	101010	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_10.5X	(5.25X)	-	-	100010	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_11.0X	5.5X	(2.75X)	-	100110	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_11.5X	(5.75X)	-	-	000000	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_12.0X	6.0X	3.0X	-	101110	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_12.5X	(6.25X)	-	-	111110	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_13.0X	6.5X	(3.25X)	-	010110	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_13.5X	(6.75X)	-	-	111000	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_14.0X	7.0X	3.5X	-	110010	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_15.0X	7.5X	(3.75X)	-	000110	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_16.0X	8.0X	4.0X	-	110110	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_17.0X	8.5X	(4.25X)	-	000010	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_18.0X	9.0X	4.5X	-	001010	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_20.0X	10.0X	5.0X	-	001110	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_21.0X	10.5X	(5.25X)	-	010010	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_24.0X	12.0X	6.0X	-	011010	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_28.0X	14.0X	7.0X	-	111010	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0

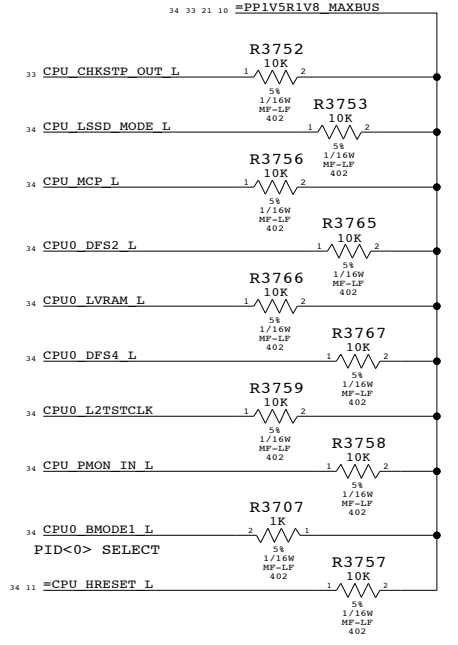
A7PM

OVDD	BVSEL0	BVSEL1
1.8V INTERFACE	GND	OVDD
2.5V INTERFACE	OVDD	OVDD
2.5V INTERFACE	CPU_HRESET_L	OVDD
RESERVED(1.5V)	CPU_HRESET_INV	OVDD

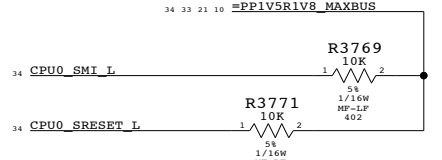
A8

OVDD	BVSEL0	BVSEL1
1.8V INTERFACE	GND	GND
1.5V INTERFACE	OVDD	GND
RESERVED	CPU_HRESET_L	GND
RESERVED	CPU_HRESET_INV	GND
2.5V INTERFACE	GND	OVDD
2.5V INTERFACE	OVDD	OVDD
RESERVED	CPU_HRESET_L	OVDD
RESERVED	CPU_HRESET_INV	OVDD

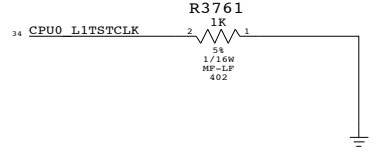
CPU PULLUPS



INTERRUPT PULL-UPS



CPU PULLDOWNS

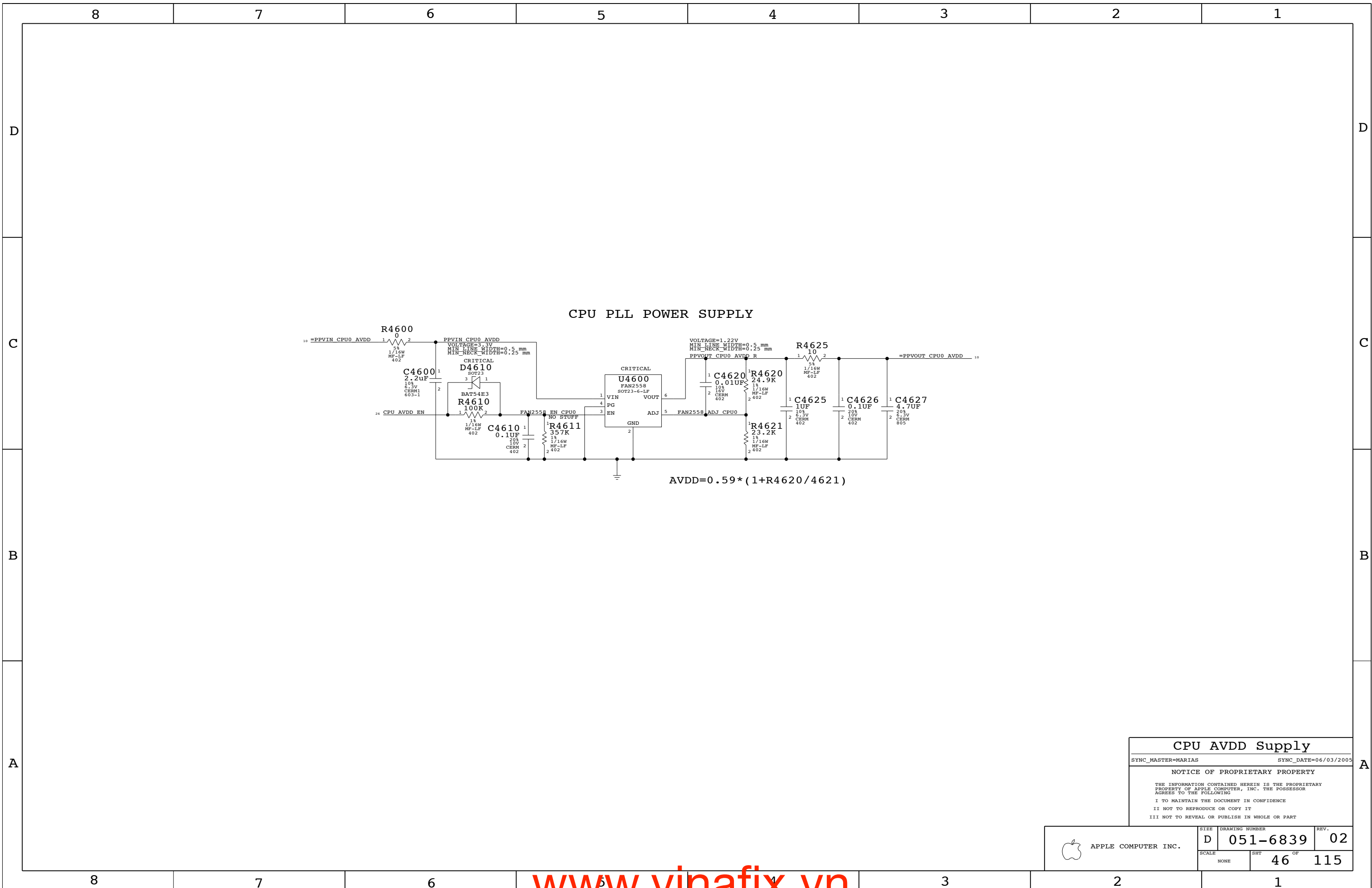


A8 Configuration Straps
 SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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NONE	37	115



CPU AVDD Supply

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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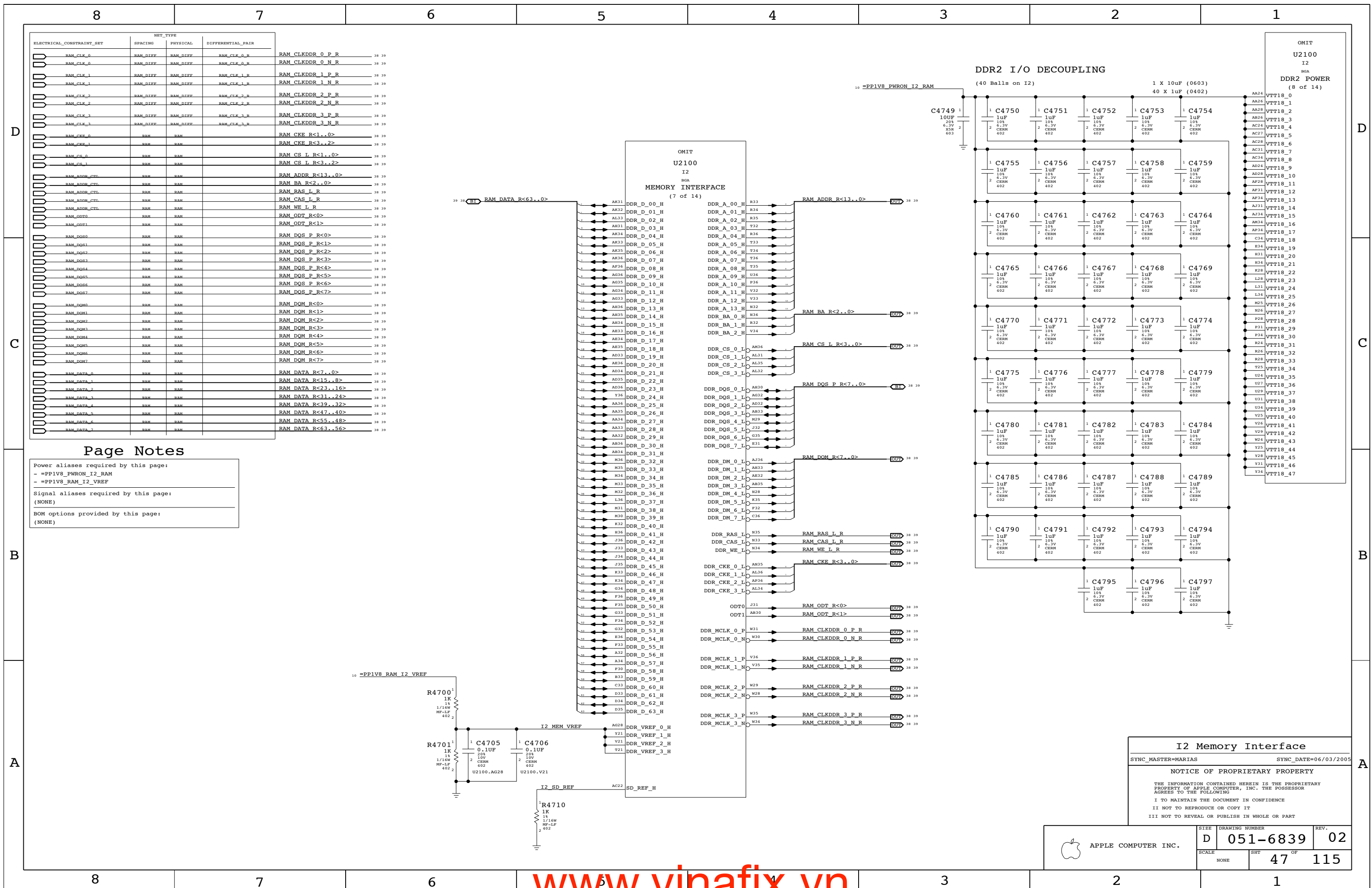
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SCALE	SHT		OF
NONE	46		115



ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	NET_TYPE
				RAM_CLK_0
				RAM_CLK_0
				RAM_CLK_1
				RAM_CLK_1
				RAM_CLK_2
				RAM_CLK_2
				RAM_CLK_3
				RAM_CLK_3
				RAM_CKE_0
				RAM_CKE_1
				RAM_CS_0
				RAM_CS_1
				RAM_ADDR_CTL
				RAM_ADDR_CTL
				RAM_ADDR_CTL
				RAM_ADDR_CTL
				RAM_ODT0
				RAM_ODT1
				RAM_DQS_0
				RAM_DQS_1
				RAM_DQS_2
				RAM_DQS_3
				RAM_DQS_4
				RAM_DQS_5
				RAM_DQS_6
				RAM_DQS_7
				RAM_DQM_0
				RAM_DQM_1
				RAM_DQM_2
				RAM_DQM_3
				RAM_DQM_4
				RAM_DQM_5
				RAM_DQM_6
				RAM_DQM_7
				RAM_DATA_0
				RAM_DATA_1
				RAM_DATA_2
				RAM_DATA_3
				RAM_DATA_4
				RAM_DATA_5
				RAM_DATA_6
				RAM_DATA_7

				RAM_CLKDDR_0_P_R
				RAM_CLKDDR_0_N_R
				RAM_CLKDDR_1_P_R
				RAM_CLKDDR_1_N_R
				RAM_CLKDDR_2_P_R
				RAM_CLKDDR_2_N_R
				RAM_CLKDDR_3_P_R
				RAM_CLKDDR_3_N_R
				RAM_CKE_R<1..0>
				RAM_CKE_R<3..2>
				RAM_CS_L_R<1..0>
				RAM_CS_L_R<3..2>
				RAM_ADDR_R<13..0>
				RAM_BA_R<2..0>
				RAM_RAS_L_R
				RAM_CAS_L_R
				RAM_WE_L_R
				RAM_ODT_R<0>
				RAM_ODT_R<1>
				RAM_DQS_P_R<0>
				RAM_DQS_P_R<1>
				RAM_DQS_P_R<2>
				RAM_DQS_P_R<3>
				RAM_DQS_P_R<4>
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				RAM_DQS_P_R<7>
				RAM_DQM_R<0>
				RAM_DQM_R<1>
				RAM_DQM_R<2>
				RAM_DQM_R<3>
				RAM_DQM_R<4>
				RAM_DQM_R<5>
				RAM_DQM_R<6>
				RAM_DQM_R<7>
				RAM_DATA_R<7..0>
				RAM_DATA_R<15..8>
				RAM_DATA_R<23..16>
				RAM_DATA_R<31..24>
				RAM_DATA_R<39..32>
				RAM_DATA_R<47..40>
				RAM_DATA_R<55..48>
				RAM_DATA_R<63..56>

Page Notes

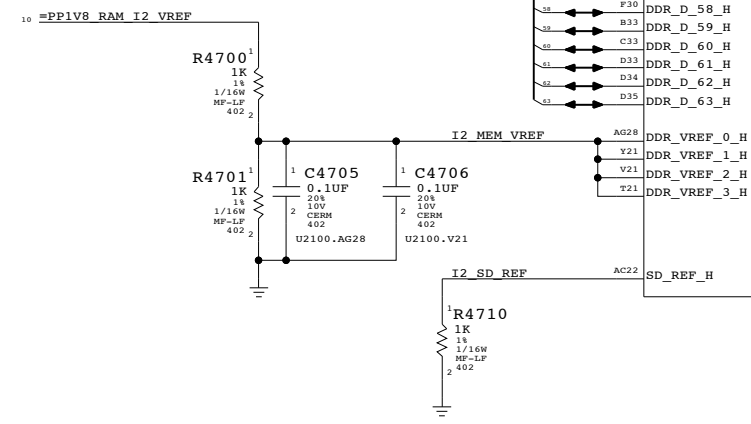
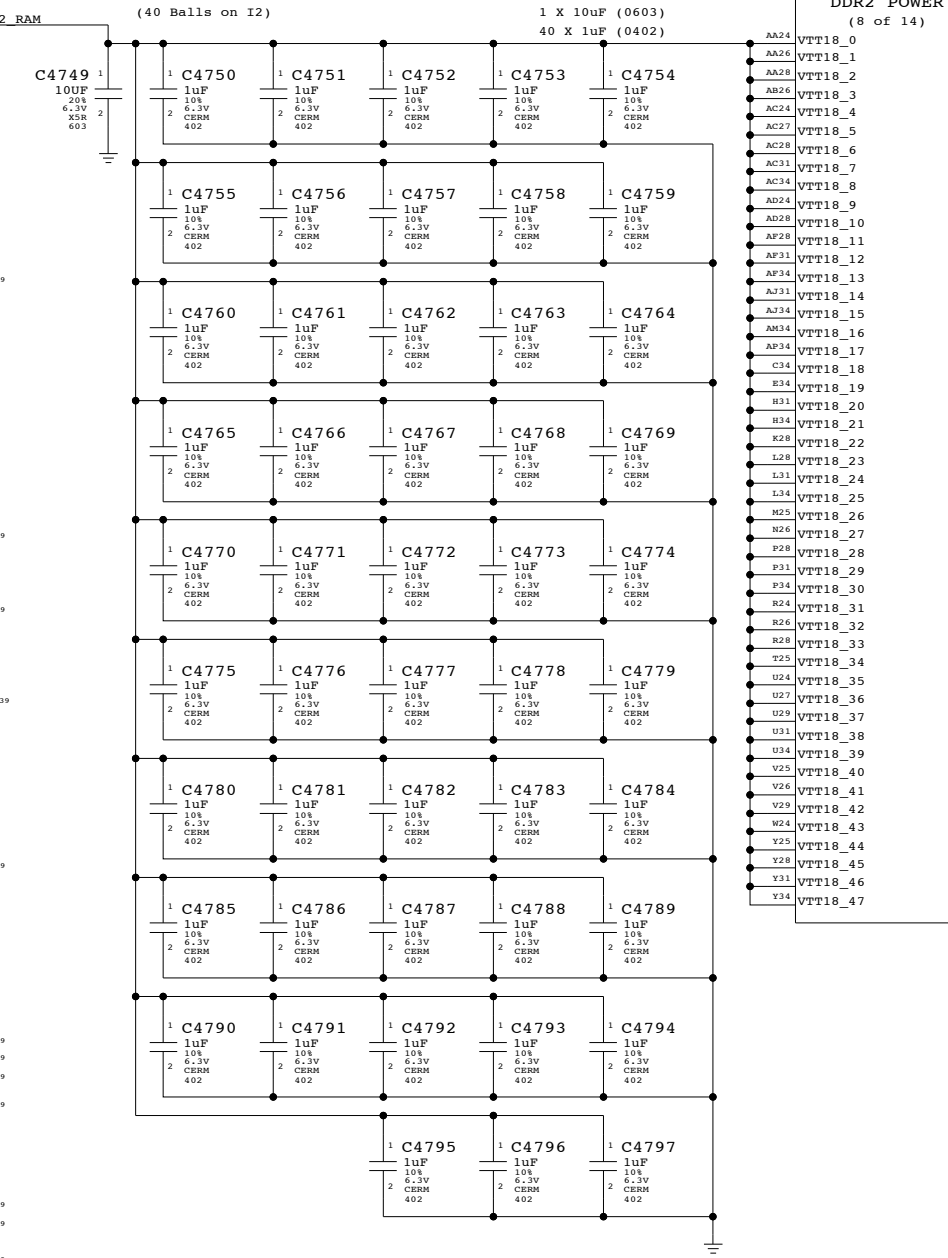
Power aliases required by this page:
 - =PP1V8_PWRON_I2_RAM
 - =PP1V8_RAM_I2_VREF

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

OMIT
 U2100
 I2
 BGA
MEMORY INTERFACE
 (7 of 14)

DDR2 I/O DECOUPLING
 (40 Balls on I2)



I2 Memory Interface

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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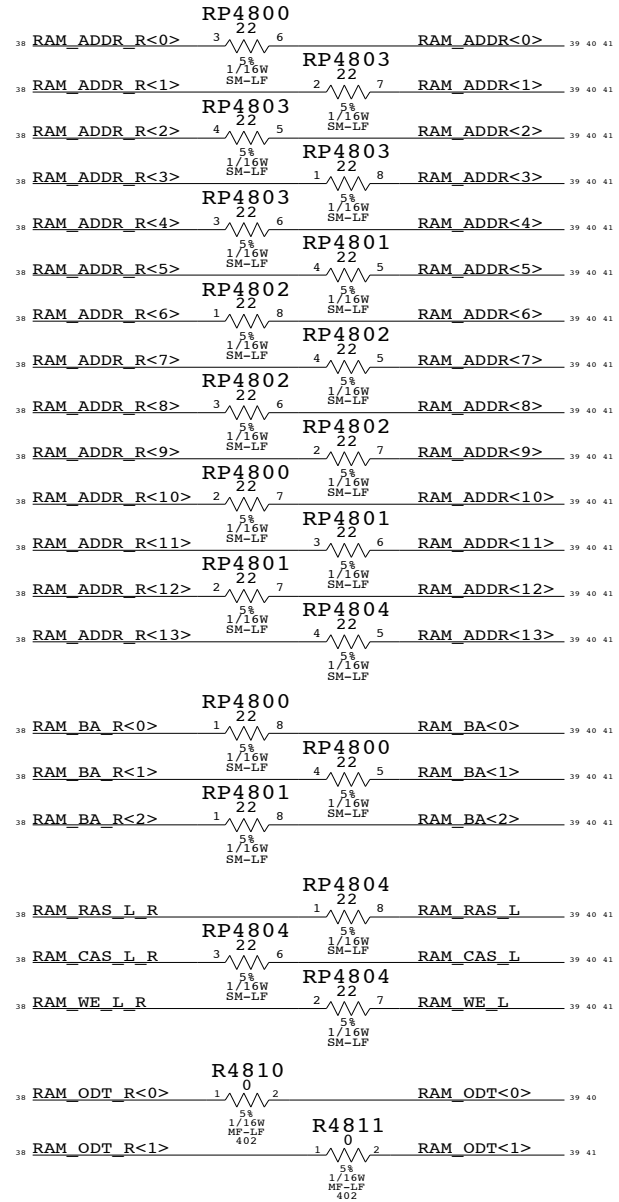
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	D	051-6839	02
SCALE	SHT	OF	
NONE	47	115	

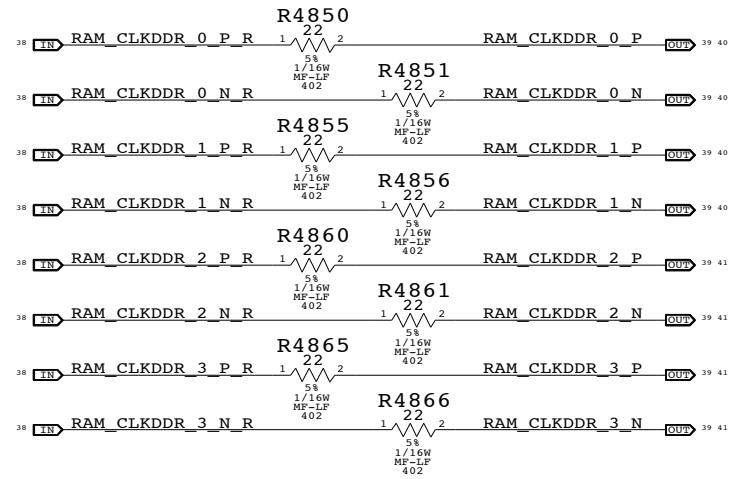
Main Memory Series Termination

SERIES RESISTORS FOR CONTROL SIGNALS

PINS ARE SWAPPABLE FOR RPAKS RP4800-RP4804

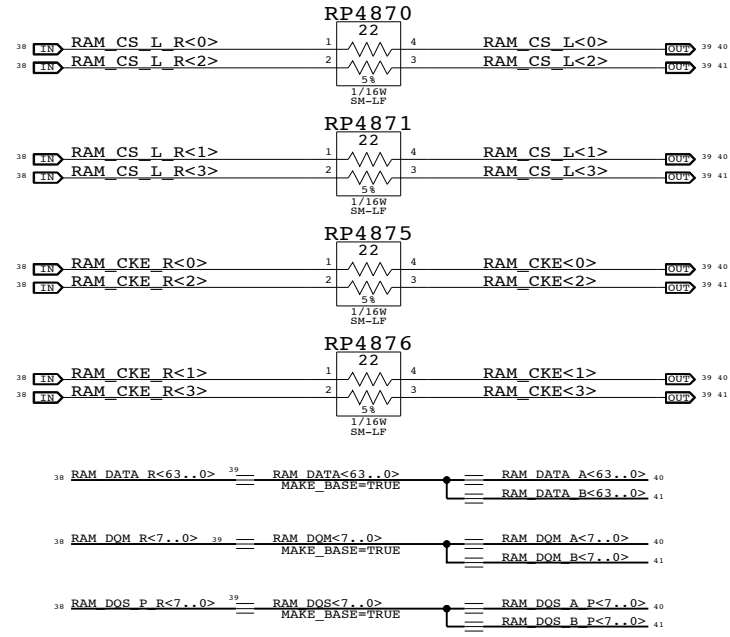


SERIES RESISTORS FOR CLOCKS



SERIES RESISTORS FOR CS / CKE

Do not swap with other RPAKS



ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
DIFF	RAM_DIFF	RAM_DIFF	RAM_CLK_0	RAM_CLKDDR_0_P 39 40
DIFF	RAM_DIFF	RAM_DIFF	RAM_CLK_0	RAM_CLKDDR_0_N 39 40
DIFF	RAM_DIFF	RAM_DIFF	RAM_CLK_1	RAM_CLKDDR_1_P 39 40
DIFF	RAM_DIFF	RAM_DIFF	RAM_CLK_1	RAM_CLKDDR_1_N 39 40
DIFF	RAM_DIFF	RAM_DIFF	RAM_CLK_2	RAM_CLKDDR_2_P 39 41
DIFF	RAM_DIFF	RAM_DIFF	RAM_CLK_2	RAM_CLKDDR_2_N 39 41
DIFF	RAM_DIFF	RAM_DIFF	RAM_CLK_3	RAM_CLKDDR_3_P 39 41
DIFF	RAM_DIFF	RAM_DIFF	RAM_CLK_3	RAM_CLKDDR_3_N 39 41
DIFF	RAM	RAM	RAM_CKE<3..0>	39 40 41
DIFF	RAM	RAM	RAM_CS_L<3..0>	39 40 41
DIFF	RAM	RAM	RAM_ADDR<13..0>	39 40 41
DIFF	RAM	RAM	RAM_BA<2..0>	39 40 41
DIFF	RAM	RAM	RAM_RAS_L	39 40 41
DIFF	RAM	RAM	RAM_CAS_L	39 40 41
DIFF	RAM	RAM	RAM_WE_L	39 40 41
DIFF	RAM	RAM	RAM_ODT<1..0>	39 40 41
DIFF	RAM	RAM	RAM_DOS<7..0>	39
DIFF	RAM	RAM	RAM_DQM<7..0>	39
DIFF	RAM	RAM	RAM_DATA<63..0>	39

ECSETS provided by memory controller.

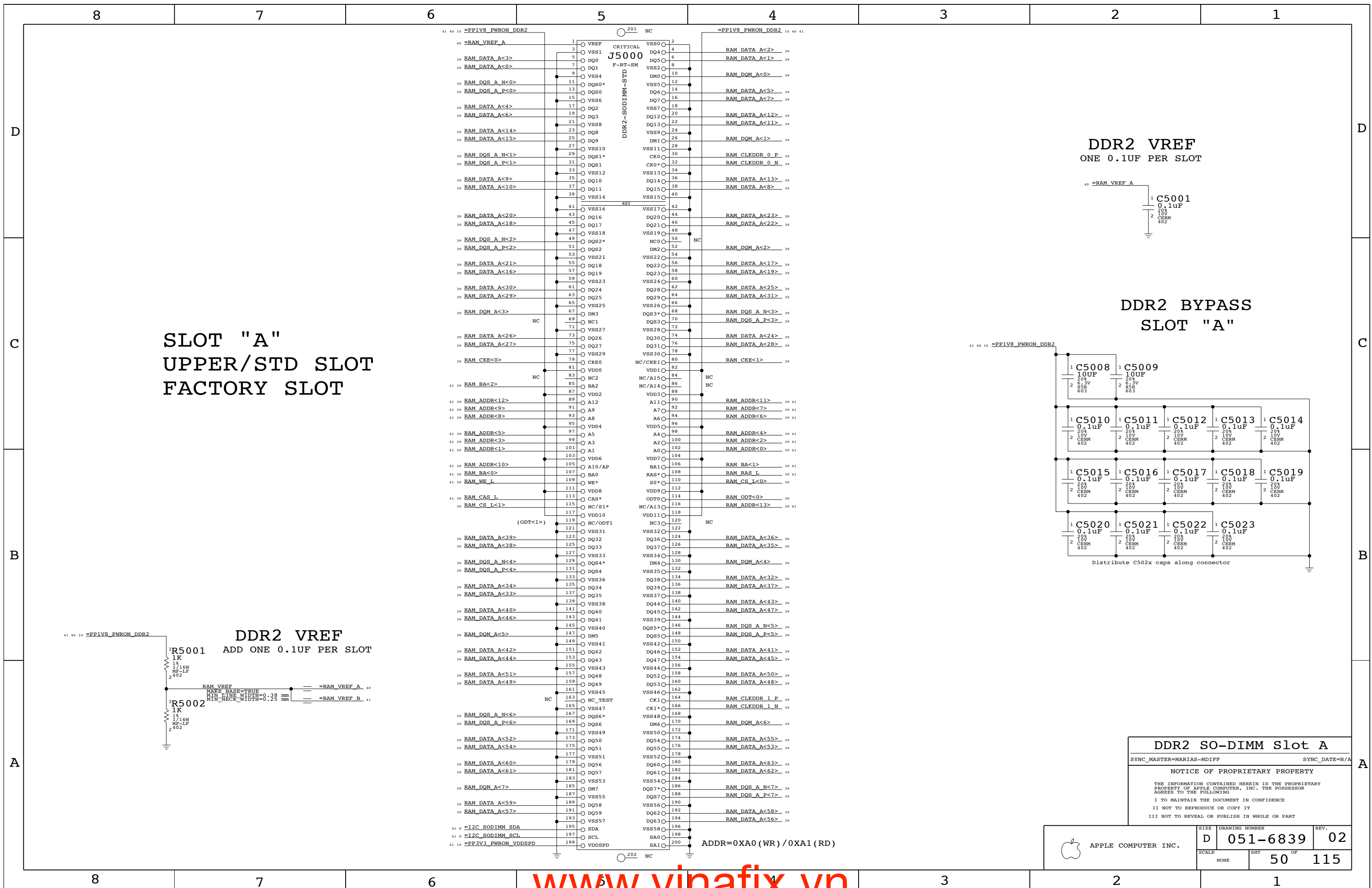
Memory Series Termination

SYNC_MASTER=MARIAS-NDIFF SYNC_DATE=N/A

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		48	115



**SLOT "A"
UPPER/STD SLOT
FACTORY SLOT**

DDR2 VREF
ONE 0.1UF PER SLOT

**DDR2 BYPASS
SLOT "A"**

DDR2 VREF
ADD ONE 0.1UF PER SLOT

DDR2 SO-DIMM Slot A

SYNC_MASTER=MARIAS-MDIFF SYNC_DATE=N/A

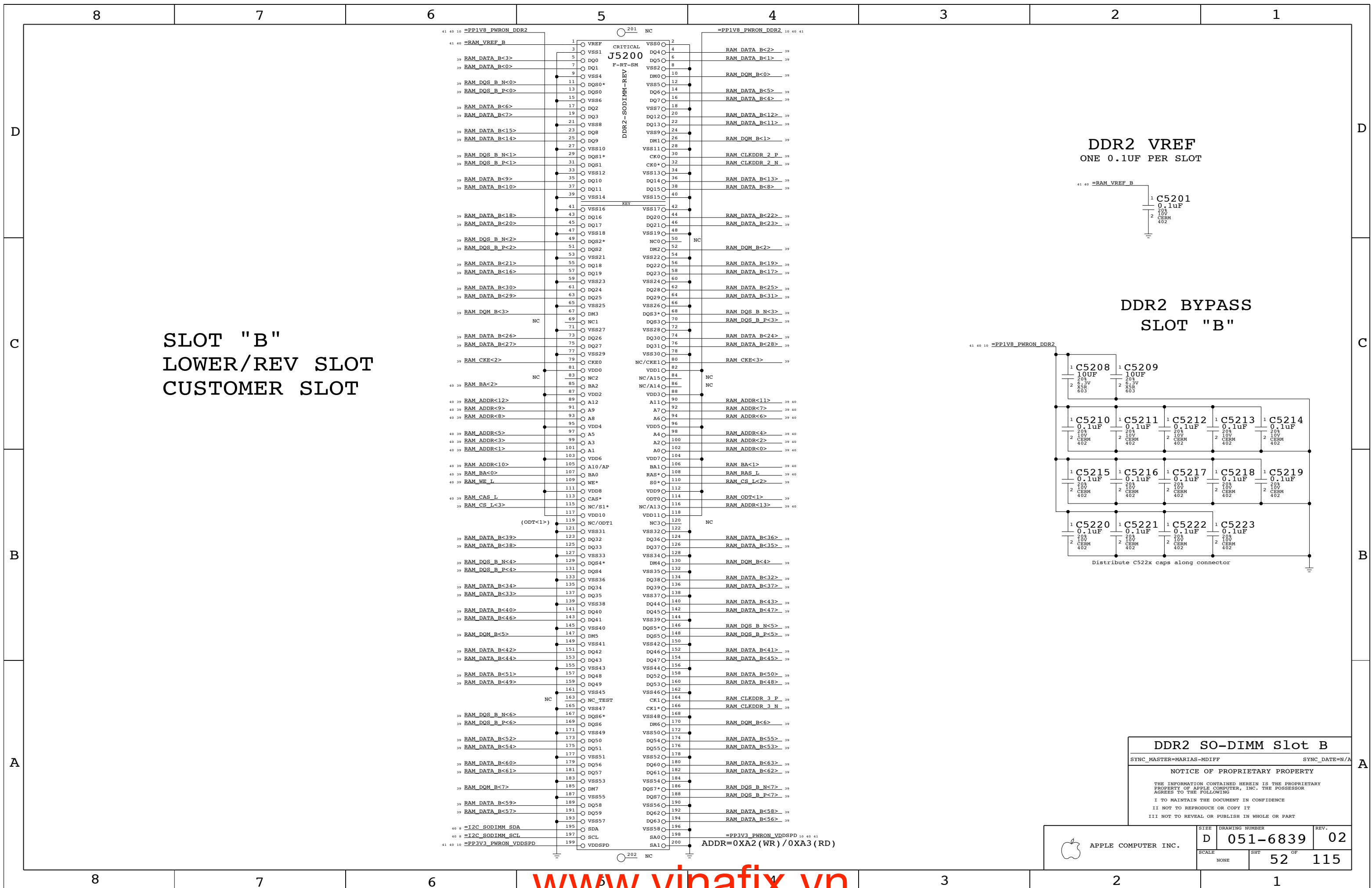
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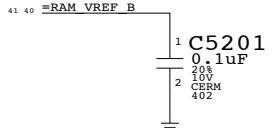
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
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SCALE	NONE	SHT	OF
		50	115

ADDR=0XA0 (WR) / 0XA1 (RD)

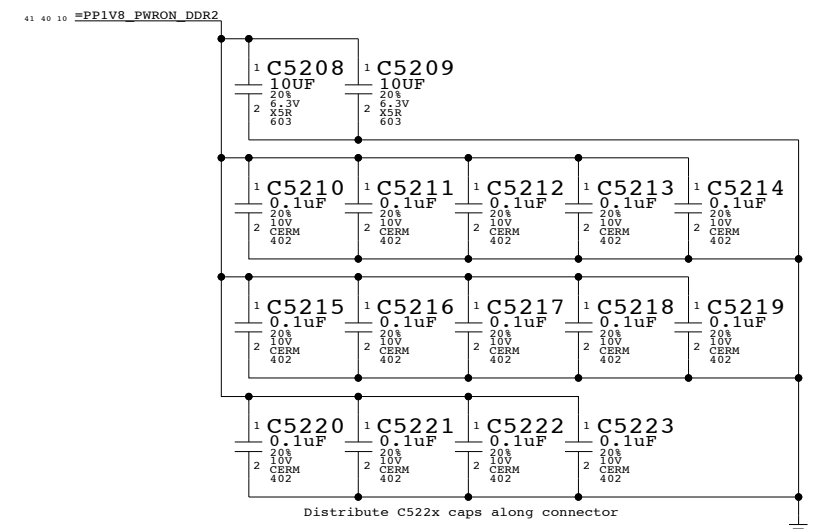


SLOT "B"
LOWER/REV SLOT
CUSTOMER SLOT

DDR2 VREF
ONE 0.1uF PER SLOT



DDR2 BYPASS
SLOT "B"



Distribute C522x caps along connector

DDR2 SO-DIMM Slot B
 SYNC_MASTER=MARIAS-MDIFF SYNC_DATE=N/A
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		52	115



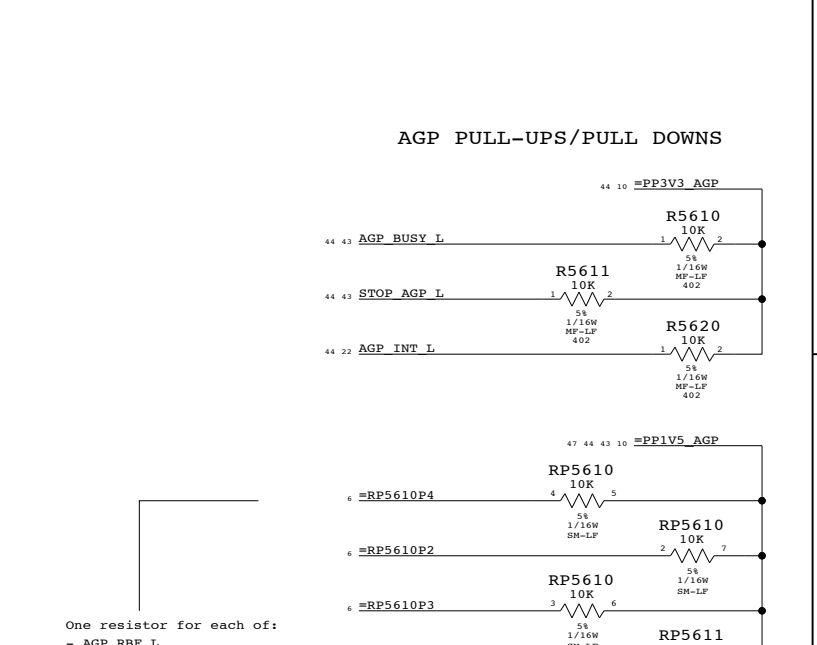
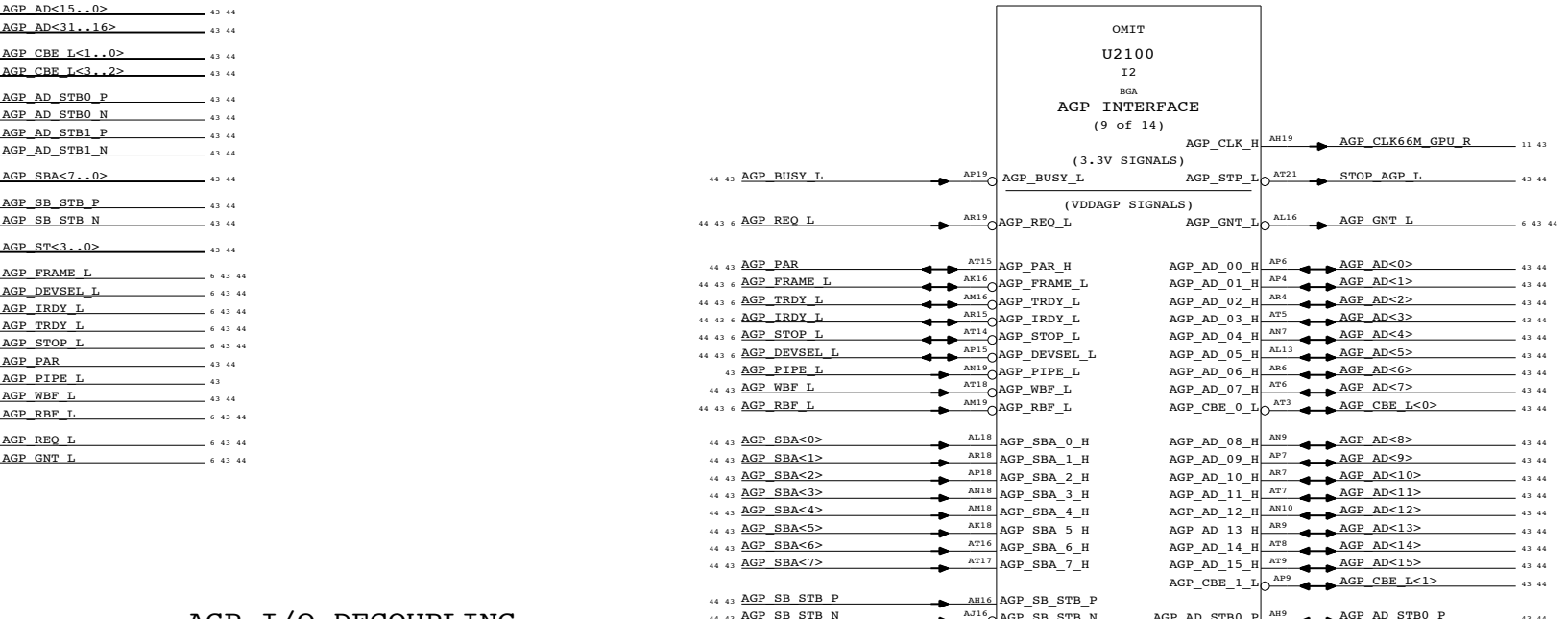
ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
FB_A_CLK_0	RAM_DIFF	RAM_DIFF	FB_A_CLK_0_R	FB A CLKDDR 0 P R
(provided above)	RAM_DIFF	RAM_DIFF	FB_A_CLK_0_R	FB A CLKDDR 0 N R
FB_A_CLK_1	RAM_DIFF	RAM_DIFF	FB_A_CLK_1_R	FB A CLKDDR 1 P R
(provided above)	RAM_DIFF	RAM_DIFF	FB_A_CLK_1_R	FB A CLKDDR 1 N R
FB_A_ADDR_CTL	RAM	RAM		FB A CKE R
FB_A_ADDR_CTL	RAM	RAM		FB A CS L R
FB_A_ADDR_CTL	RAM	RAM		FB A ADDR R<12..0>
FB_A_ADDR_CTL	RAM	RAM		FB A BA R<2..0>
FB_A_ADDR_CTL	RAM	RAM		FB A RAS L R
FB_A_ADDR_CTL	RAM	RAM		FB A CAS L R
FB_A_ADDR_CTL	RAM	RAM		FB A WE L R
FB_A_DQS0	RAM	RAM		FB A DQS R<0>
FB_A_DQS1	RAM	RAM		FB A DQS R<1>
FB_A_DQS2	RAM	RAM		FB A DQS R<2>
FB_A_DQS3	RAM	RAM		FB A DQS R<3>
FB_A_DQS4	RAM	RAM		FB A DQS R<4>
FB_A_DQS5	RAM	RAM		FB A DQS R<5>
FB_A_DQS6	RAM	RAM		FB A DQS R<6>
FB_A_DQS7	RAM	RAM		FB A DQS R<7>
FB_A_DQM0	RAM	RAM		FB A DQM R<0>
FB_A_DQM1	RAM	RAM		FB A DQM R<1>
FB_A_DQM2	RAM	RAM		FB A DQM R<2>
FB_A_DQM3	RAM	RAM		FB A DQM R<3>
FB_A_DQM4	RAM	RAM		FB A DQM R<4>
FB_A_DQM5	RAM	RAM		FB A DQM R<5>
FB_A_DQM6	RAM	RAM		FB A DQM R<6>
FB_A_DQM7	RAM	RAM		FB A DQM R<7>
FB_A_DO0	RAM	RAM		FB A DO R<7..0>
FB_A_DO1	RAM	RAM		FB A DO R<15..8>
FB_A_DO2	RAM	RAM		FB A DO R<23..16>
FB_A_DO3	RAM	RAM		FB A DO R<31..24>
FB_A_DO4	RAM	RAM		FB A DO R<39..32>
FB_A_DO5	RAM	RAM		FB A DO R<47..40>
FB_A_DO6	RAM	RAM		FB A DO R<55..48>
FB_A_DO7	RAM	RAM		FB A DO R<63..56>

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
FB_B_CLK_0	RAM_DIFF	RAM_DIFF	FB_B_CLK_0_R	FB B CLKDDR 0 P R
(provided above)	RAM_DIFF	RAM_DIFF	FB_B_CLK_0_R	FB B CLKDDR 0 N R
FB_B_CLK_1	RAM_DIFF	RAM_DIFF	FB_B_CLK_1_R	FB B CLKDDR 1 P R
(provided above)	RAM_DIFF	RAM_DIFF	FB_B_CLK_1_R	FB B CLKDDR 1 N R
FB_B_ADDR_CTL	RAM	RAM		FB B CKE R
FB_B_ADDR_CTL	RAM	RAM		FB B CS L R
FB_B_ADDR_CTL	RAM	RAM		FB B ADDR R<12..0>
FB_B_ADDR_CTL	RAM	RAM		FB B BA R<2..0>
FB_B_ADDR_CTL	RAM	RAM		FB B RAS L R
FB_B_ADDR_CTL	RAM	RAM		FB B CAS L R
FB_B_ADDR_CTL	RAM	RAM		FB B WE L R
FB_B_DQS0	RAM	RAM		FB B DQS R<0>
FB_B_DQS1	RAM	RAM		FB B DQS R<1>
FB_B_DQS2	RAM	RAM		FB B DQS R<2>
FB_B_DQS3	RAM	RAM		FB B DQS R<3>
FB_B_DQS4	RAM	RAM		FB B DQS R<4>
FB_B_DQS5	RAM	RAM		FB B DQS R<5>
FB_B_DQS6	RAM	RAM		FB B DQS R<6>
FB_B_DQS7	RAM	RAM		FB B DQS R<7>
FB_B_DQM0	RAM	RAM		FB B DQM R<0>
FB_B_DQM1	RAM	RAM		FB B DQM R<1>
FB_B_DQM2	RAM	RAM		FB B DQM R<2>
FB_B_DQM3	RAM	RAM		FB B DQM R<3>
FB_B_DQM4	RAM	RAM		FB B DQM R<4>
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FB_B_DQM6	RAM	RAM		FB B DQM R<6>
FB_B_DQM7	RAM	RAM		FB B DQM R<7>
FB_B_DO0	RAM	RAM		FB B DO R<7..0>
FB_B_DO1	RAM	RAM		FB B DO R<15..8>
FB_B_DO2	RAM	RAM		FB B DO R<23..16>
FB_B_DO3	RAM	RAM		FB B DO R<31..24>
FB_B_DO4	RAM	RAM		FB B DO R<39..32>
FB_B_DO5	RAM	RAM		FB B DO R<47..40>
FB_B_DO6	RAM	RAM		FB B DO R<55..48>
FB_B_DO7	RAM	RAM		FB B DO R<63..56>

M11 Frame Buffer Constraints
 SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005
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		SHT	OF
		55	115

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
AGP_CLK	CLOCK	CLOCK	
I2_AGP_FBCLK	I2_FBCLK	I2_FBCLK	
AGP_AD_0	AGP	AGP	
AGP_AD_1	AGP	AGP	
AGP_AD_2	AGP	AGP	
AGP_AD_3	AGP	AGP	
AGP_AD_4	AGP	AGP	
AGP_AD_5	AGP	AGP	
AGP_AD_6	AGP	AGP	
AGP_AD_7	AGP	AGP	
AGP_AD_8	AGP	AGP	
AGP_AD_9	AGP	AGP	
AGP_AD_10	AGP	AGP	
AGP_AD_11	AGP	AGP	
AGP_AD_12	AGP	AGP	
AGP_AD_13	AGP	AGP	
AGP_AD_14	AGP	AGP	
AGP_AD_15	AGP	AGP	
AGP_AD_16	AGP	AGP	
AGP_AD_17	AGP	AGP	
AGP_AD_18	AGP	AGP	
AGP_AD_19	AGP	AGP	
AGP_AD_20	AGP	AGP	
AGP_AD_21	AGP	AGP	
AGP_AD_22	AGP	AGP	
AGP_AD_23	AGP	AGP	
AGP_AD_24	AGP	AGP	
AGP_AD_25	AGP	AGP	
AGP_AD_26	AGP	AGP	
AGP_AD_27	AGP	AGP	
AGP_AD_28	AGP	AGP	
AGP_AD_29	AGP	AGP	
AGP_AD_30	AGP	AGP	
AGP_AD_31	AGP	AGP	
AGP_AD_32	AGP	AGP	
AGP_AD_33	AGP	AGP	
AGP_AD_34	AGP	AGP	
AGP_AD_35	AGP	AGP	
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AGP_AD_38	AGP	AGP	
AGP_AD_39	AGP	AGP	
AGP_AD_40	AGP	AGP	
AGP_AD_41	AGP	AGP	
AGP_AD_42	AGP	AGP	
AGP_AD_43	AGP	AGP	
AGP_AD_44	AGP	AGP	
AGP_AD_45	AGP	AGP	
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AGP_AD_96	AGP	AGP	
AGP_AD_97	AGP	AGP	
AGP_AD_98	AGP	AGP	
AGP_AD_99	AGP	AGP	
AGP_AD_100	AGP	AGP	



Page Notes

Power aliases required by this page:
 - =PP3V3_AGP
 - =PP1V5_AGP
 - =PP1V5_I2_AGP

Signal aliases required by this page:
 - =I2_AGP_VREF - VRef from graphics card or on-board graphics controller
 - =I2_AGP_FBCLK_IN - AGP feedback clock input. Length should match that of clock from I2 to AGP device.

BOM options provided by this page:
 (NONE)

NOTE: I2 implements an AGP 4x bridge. AGP 8x signals are not provided by this page.

I2 AGP Interface
 SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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	NONE	56	115	02

NET TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
7700	CLOCK	CLOCK	

AGP_CLK66M_GPU 11 44

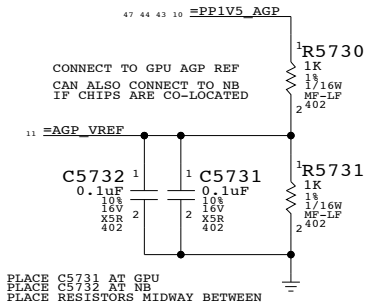
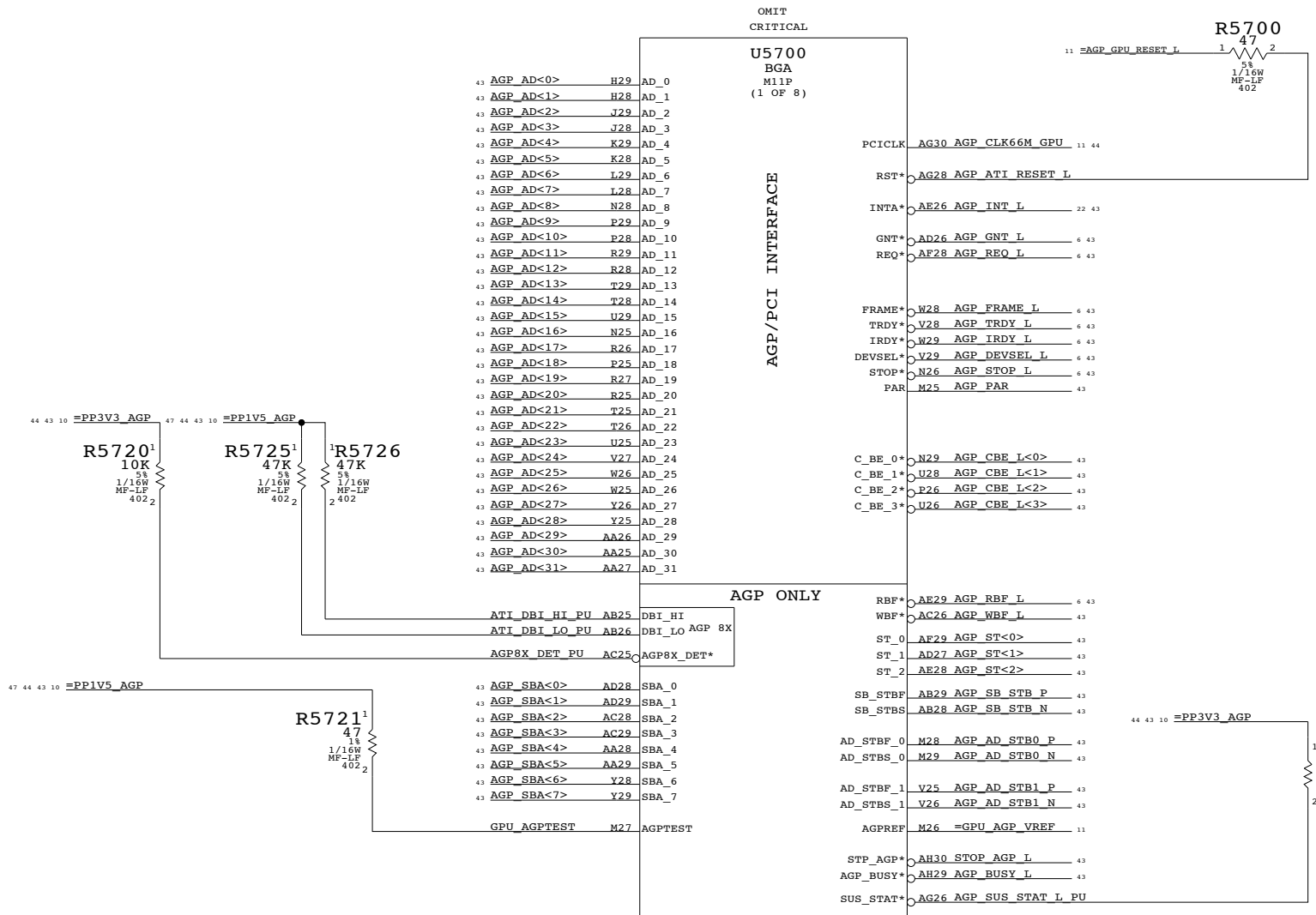
Page Notes

Power aliases required by this page:
 - =PP3V3_AGP
 - =PP1V5_AGP

Signal aliases required by this page:
 - =AGP_VREF - Vref divider output for both GPU and NB
 - =AGP_GPU_RESET_L - Active low reset for GPU

BOM options provided by this page:
 (NONE)

NOTE: AGP 8x signals are not provided by this page.



GPU (M11) AGP Interface

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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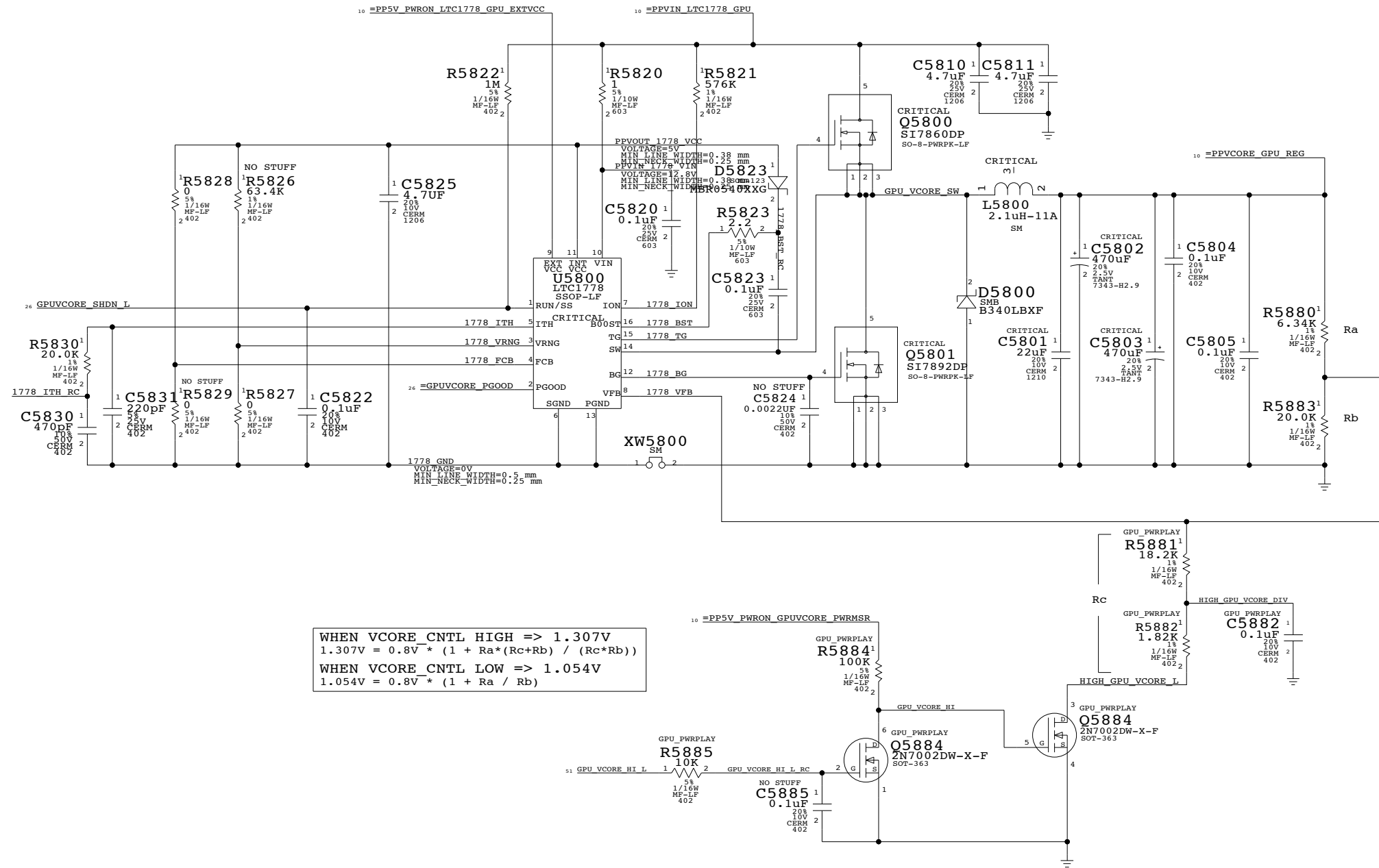
Power aliases required by this page:
 - =PPVIN_LTC1778_GPU
 - =PP5V_PWRON_LTC1778_GPU_EXTVCC
 - =PPVCORE_GPU_REG

Signal aliases required by this page:
 - =GPUVCORE_PGOOD - Active high Power Good signal for power sequencing

BOM options provided by this page:
 - GPU_PWRPLAY

NOTE: Implements "Power Miser" feature for ATI GPUs

GPU VCore SUPPLY



WHEN VCORE_CNTL HIGH => 1.307V
 $1.307V = 0.8V * (1 + Ra * (Rc + Rb) / (Rc * Rb))$
 WHEN VCORE_CNTL LOW => 1.054V
 $1.054V = 0.8V * (1 + Ra / Rb)$

GPU VCore Supply
 SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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SCALE	NONE	SHT	OF
		58	115

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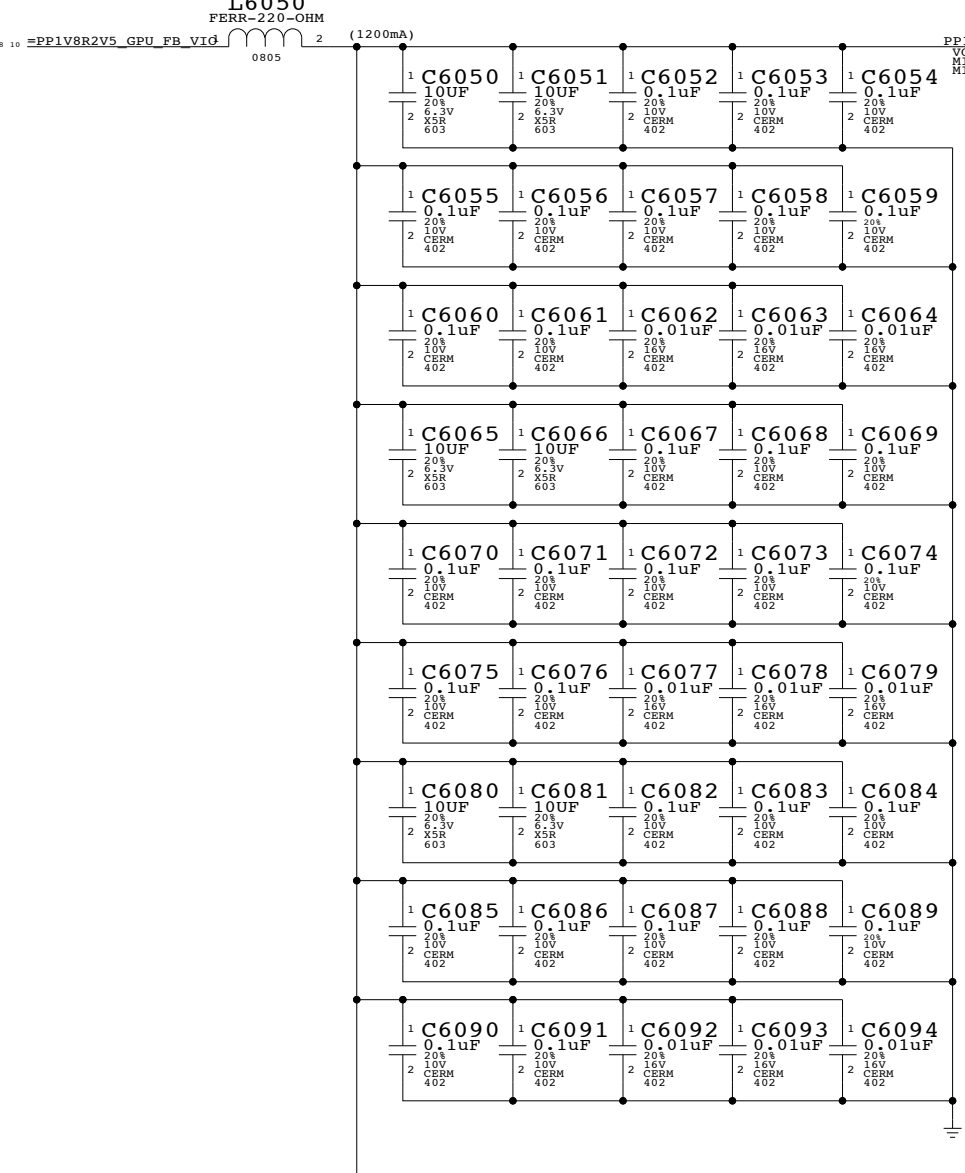
Power aliases required by this page:
 - =PP1V8R2V5_GPU_FB_VIO - =PP1V8_GPU_PANEL_IO
 - =PP3V3_GPU_VDDR3 - =PP1V8_GPU_LVDS_PLL
 - =PP1V5_GPU_DVO - =PP2V5_GPU_LVDS_IO
 - =PP1V8_GPU_DVO - =PP2V5_GPU_LVDS_IO
 - =PP1V5R3V3_DVO_VREF - =PP1V5_AGP

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - DVO_1V5 - GPU_LVDDR_2V5
 - DVO_1V8 - GPU_LVDDR_2V8

NOTE: Implements a low-swing DVO bus only

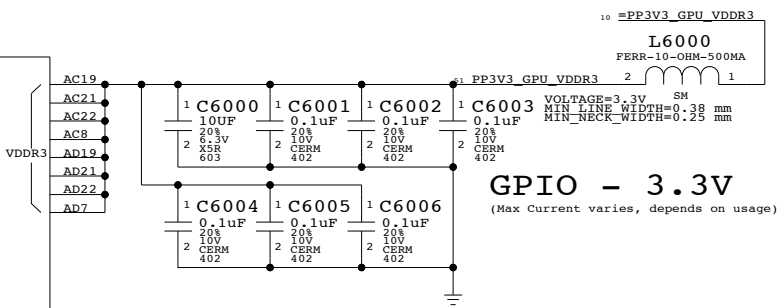
MEMORY I/O - 1.8V/2.5V



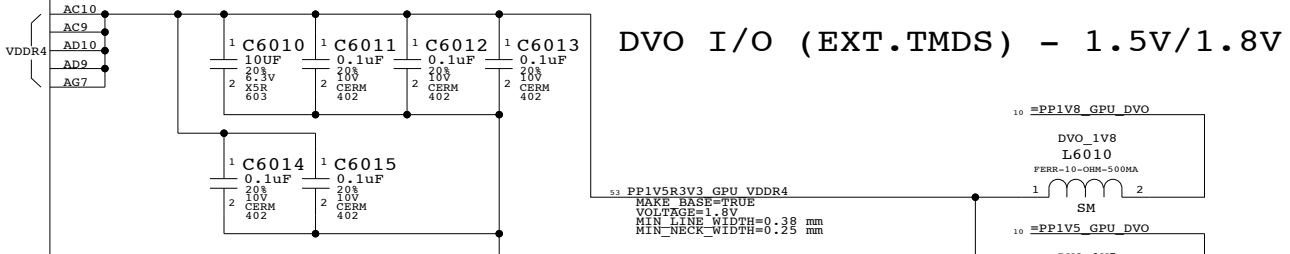
OMIT
 CRITICAL
U5700
 M11P
 BGA
 (7 OF 8)

- A15
- A21
- A28
- A3
- A9
- AA1
- AA4
- AA7
- AA8
- AD4
- B1
- B30
- D11
- D13
- D14
- D17
- D19
- D20
- D23
- D26
- D5
- D8
- E27
- F4
- G10
- G13
- G15
- G19
- G22
- G27
- H7
- H10
- H13
- H15
- H17
- H19
- H22
- J1
- J23
- J24
- J4
- J7
- J8
- L27
- L8
- M4
- N4
- N7
- N8
- R1
- R4
- T4
- T7
- T8
- V4
- V7
- V8

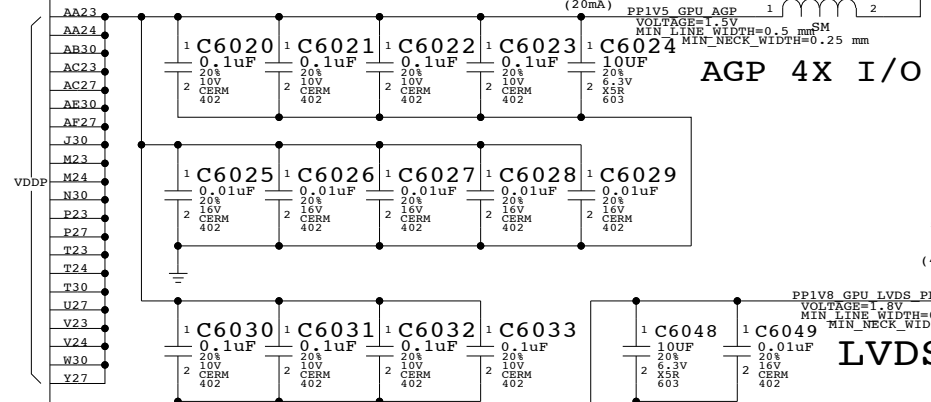
GPIO - 3.3V
 (Max Current varies, depends on usage)



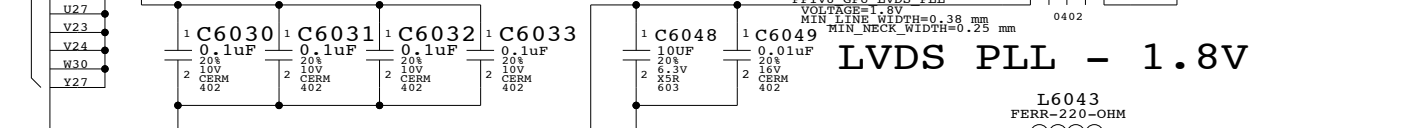
DVO I/O (EXT.TMDS) - 1.5V/1.8V



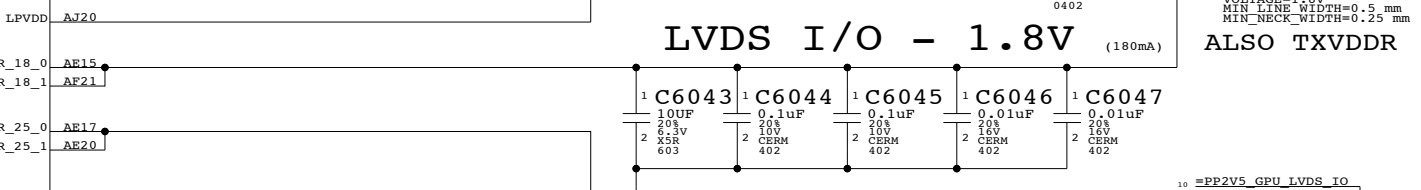
AGP 4X I/O - 1.5V



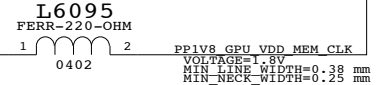
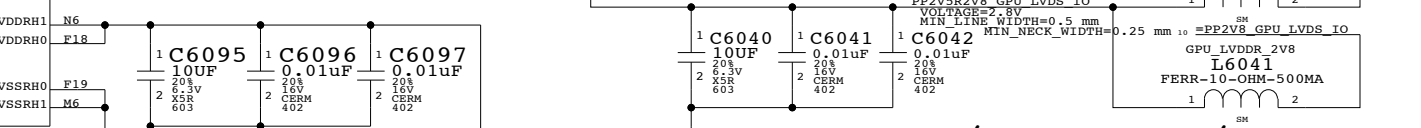
LVDS PLL - 1.8V



LVDS I/O - 1.8V
 (180mA) ALSO TXVDDR



LVDS I/O - 2.5V/2.8V



GPU (M11) I/O Power

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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	D	051-6839	02
SCALE	SHT	OF	
NONE	60	115	

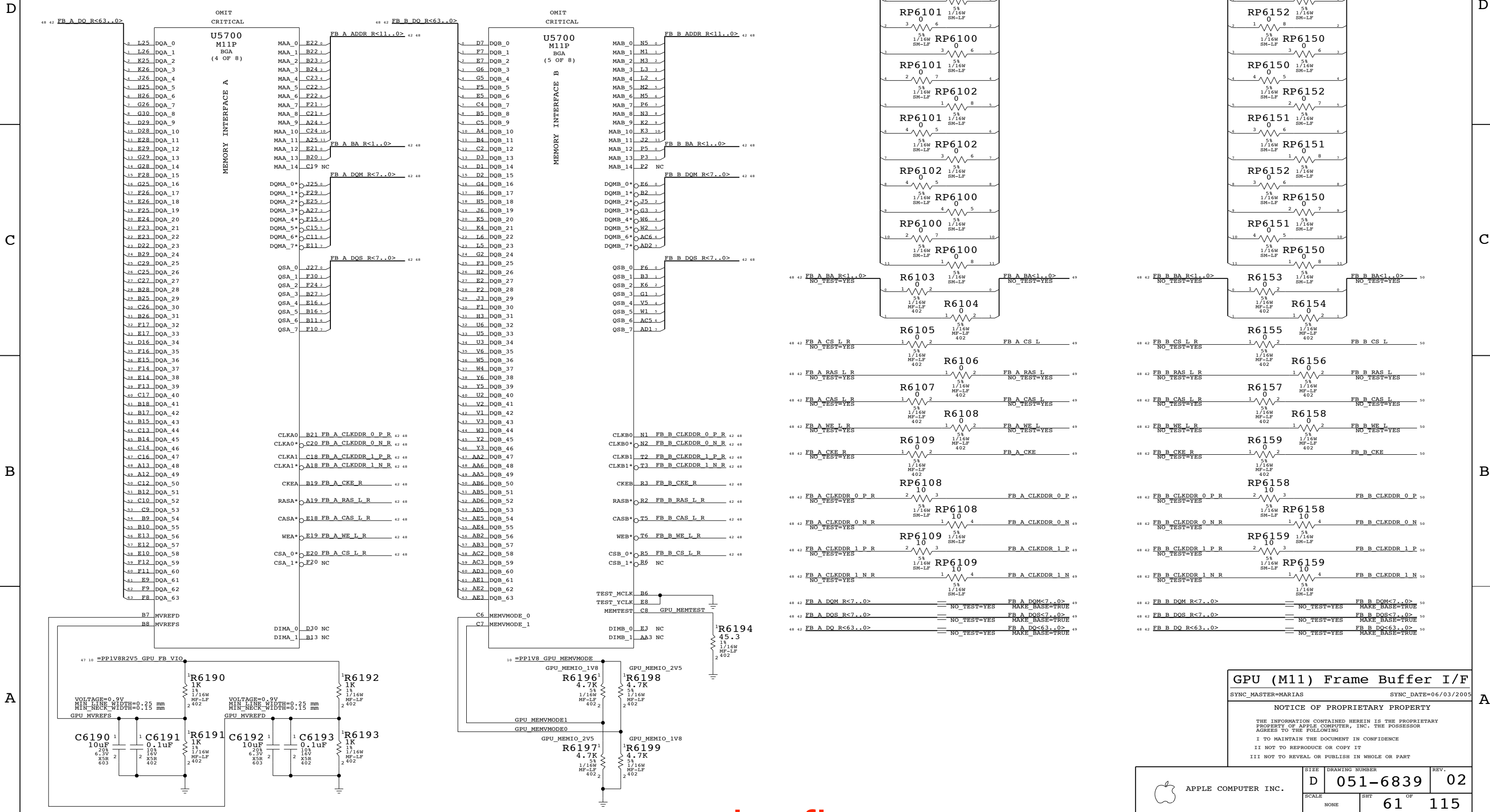
Page Notes

Power aliases required by this page:
 - =PP1V8R2V5_GPU_FB_VIO
 - =PP1V8_GPU_MEMVMODE

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - GPU_MEMIO_1V8
 - GPU_MEMIO_2V5

GPU Frame Buffer Series Term



GPU (M11) Frame Buffer I/F

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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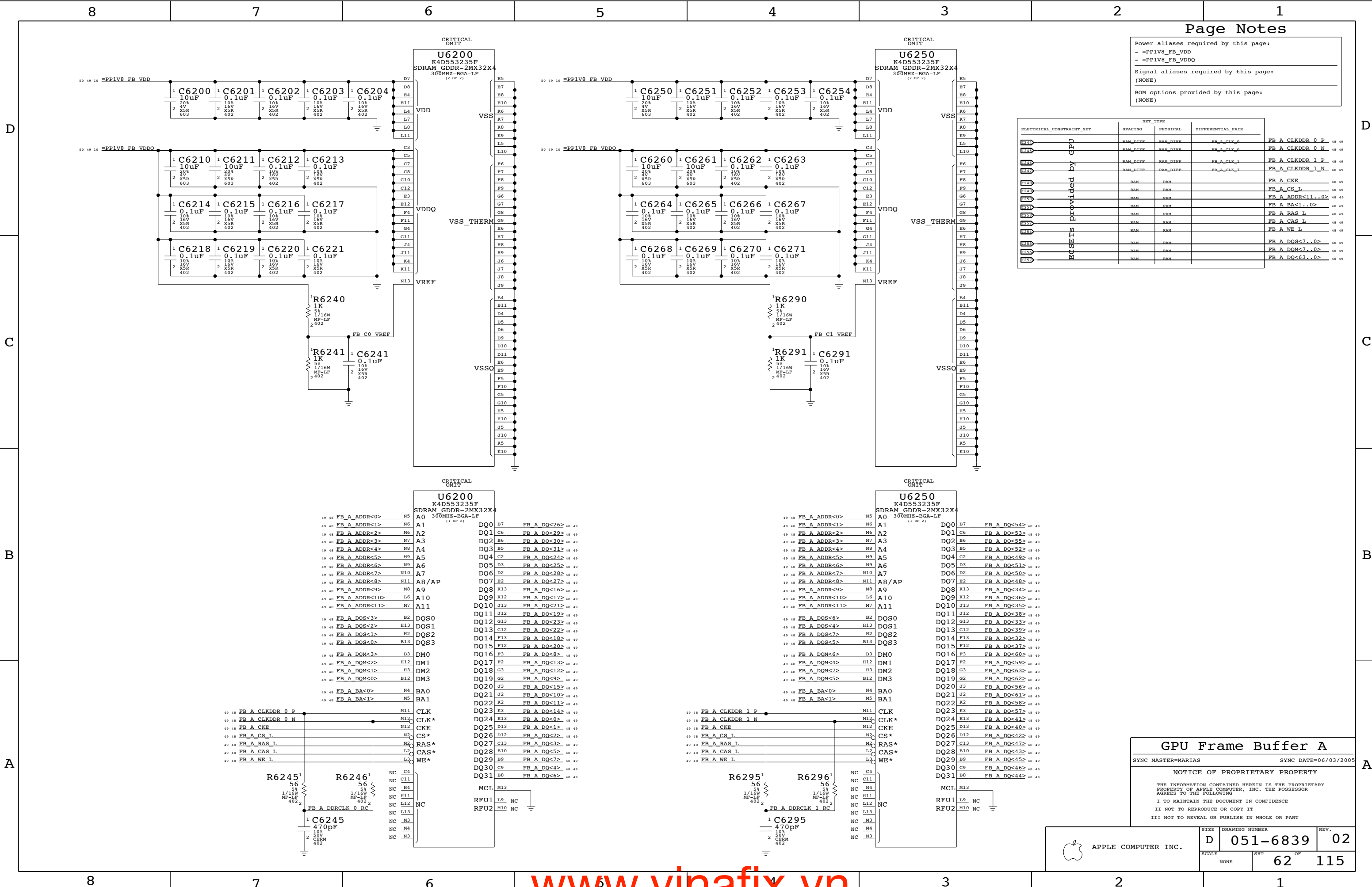
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6839	02
SCALE	SHT	OF	
NONE	61	115	

Power aliases required by this page:
 - =PPIV8_FB_VDD
 - =PPIV8_FB_VDDQ

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
FB00	RAM_DIFF	RAM_DIFF	FB_A_CLK_0
FB01	RAM_DIFF	RAM_DIFF	FB_A_CLK_0_N
FB02	RAM_DIFF	RAM_DIFF	FB_A_CLK_1
FB03	RAM_DIFF	RAM_DIFF	FB_A_CLK_1_P
FB04	RAM	RAM	FB_A_CLKDDR_1_N
FB05	RAM	RAM	FB_A_CKE
FB06	RAM	RAM	FB_A_CS_L
FB07	RAM	RAM	FB_A_ADDR<11..0>
FB08	RAM	RAM	FB_A_BA<1..0>
FB09	RAM	RAM	FB_A_RAS_L
FB10	RAM	RAM	FB_A_CAS_L
FB11	RAM	RAM	FB_A_WE_L
FB12	RAM	RAM	FB_A_DQS<7..0>
FB13	RAM	RAM	FB_A_DQM<7..0>
FB14	RAM	RAM	FB_A_DQ<63..0>



GPU Frame Buffer A

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

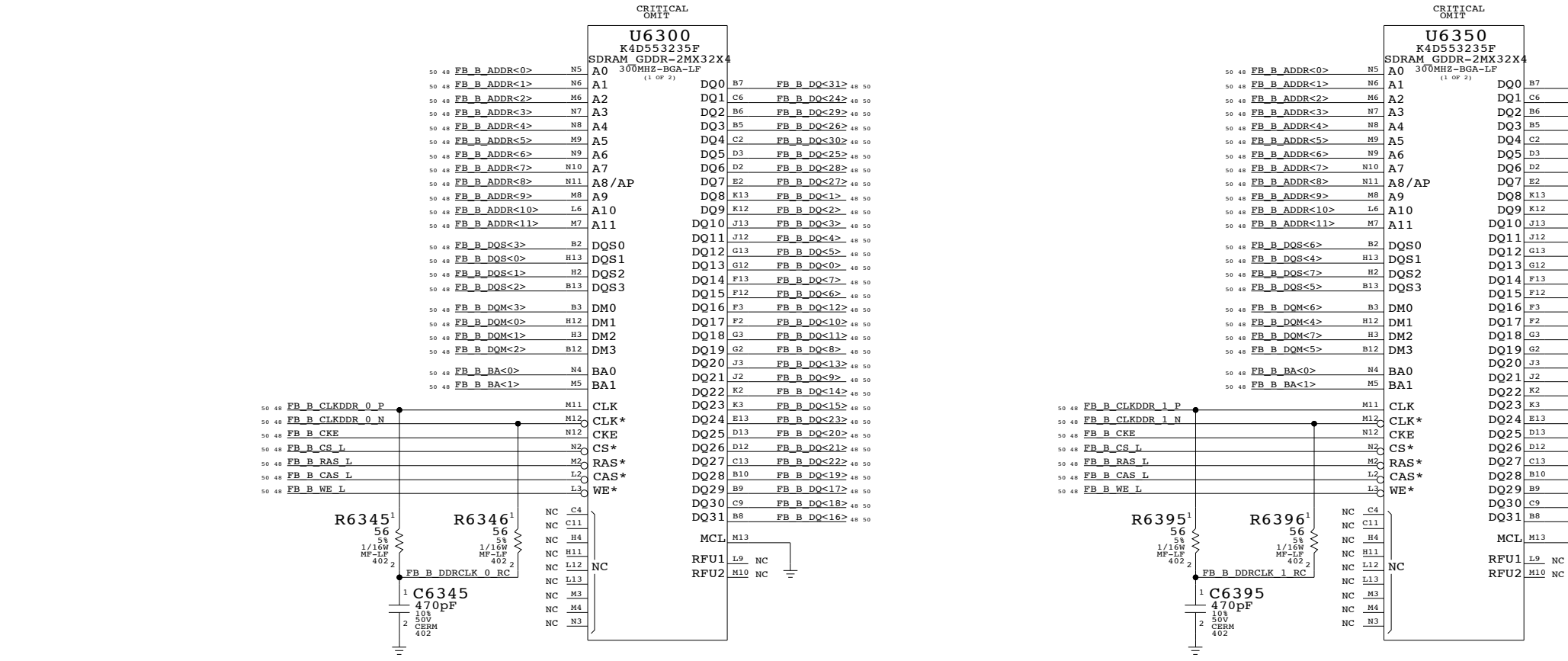
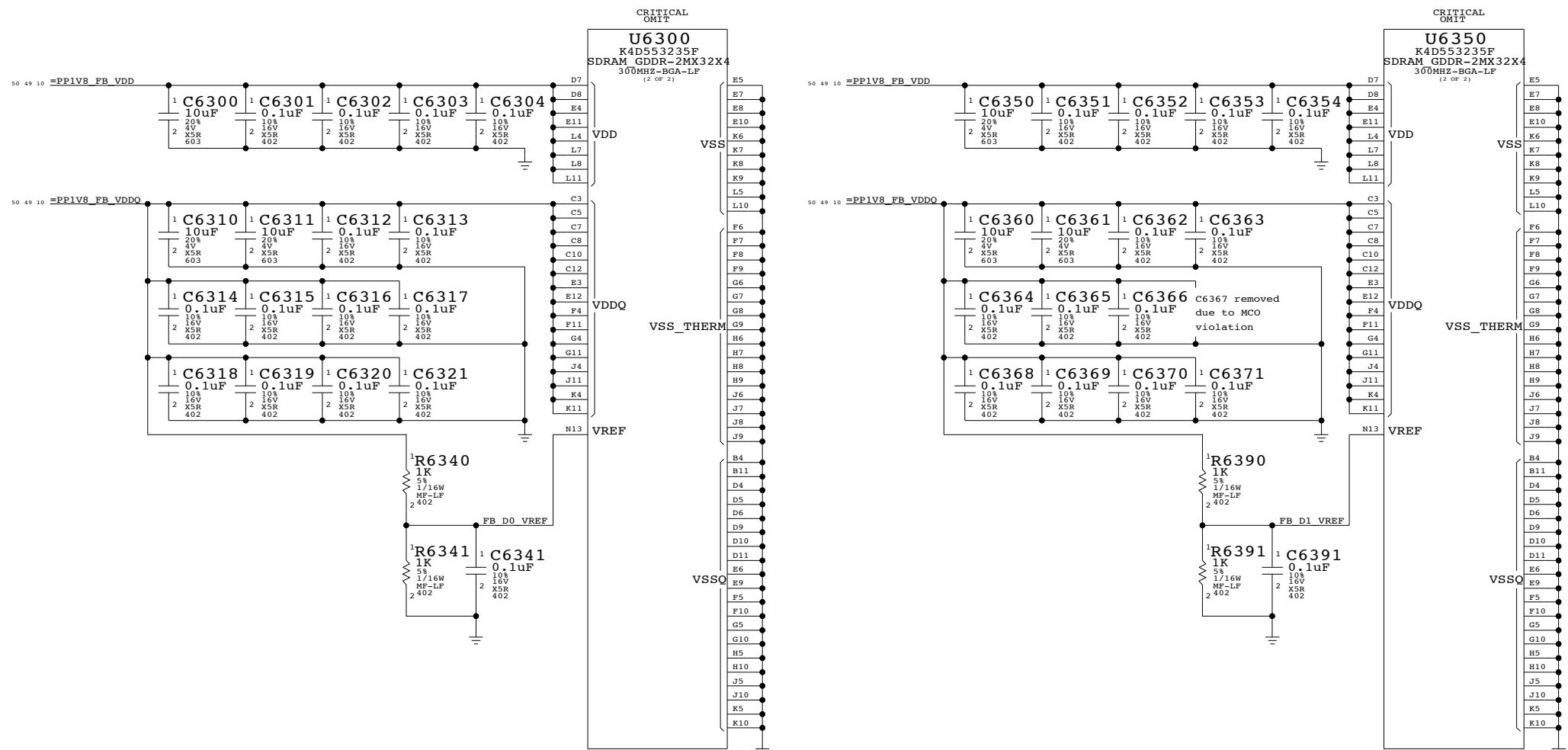
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SIZE	DRAWING NUMBER	REV.
D	051-6839	02
SCALE	SHT	OF
NONE	62	115

Power aliases required by this page:
- =PPIV8_FB_VDD
- =PPIV8_FB_VDDQ
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)

Table with columns: ELECTRICAL_CONSTRAINT_SET, SPACING, PHYSICAL, DIFFERENTIAL_PAIR. Lists constraints like FB_B_CLKDDR_0_P, FB_B_CLKDDR_0_N, etc.



GPU Frame Buffer B
SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005
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Table with columns: SIZE, DRAWING NUMBER, REV., SCALE, SHEET OF. Values: D, 051-6839, 02, NONE, 63 OF 115.

Page Notes

Power aliases required by this page:
 - =PP3V3_GPU_GPIOS
 - =PP2V5_PVDD
 - =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
 - =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
 - =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
 (NONE)

D

D

C

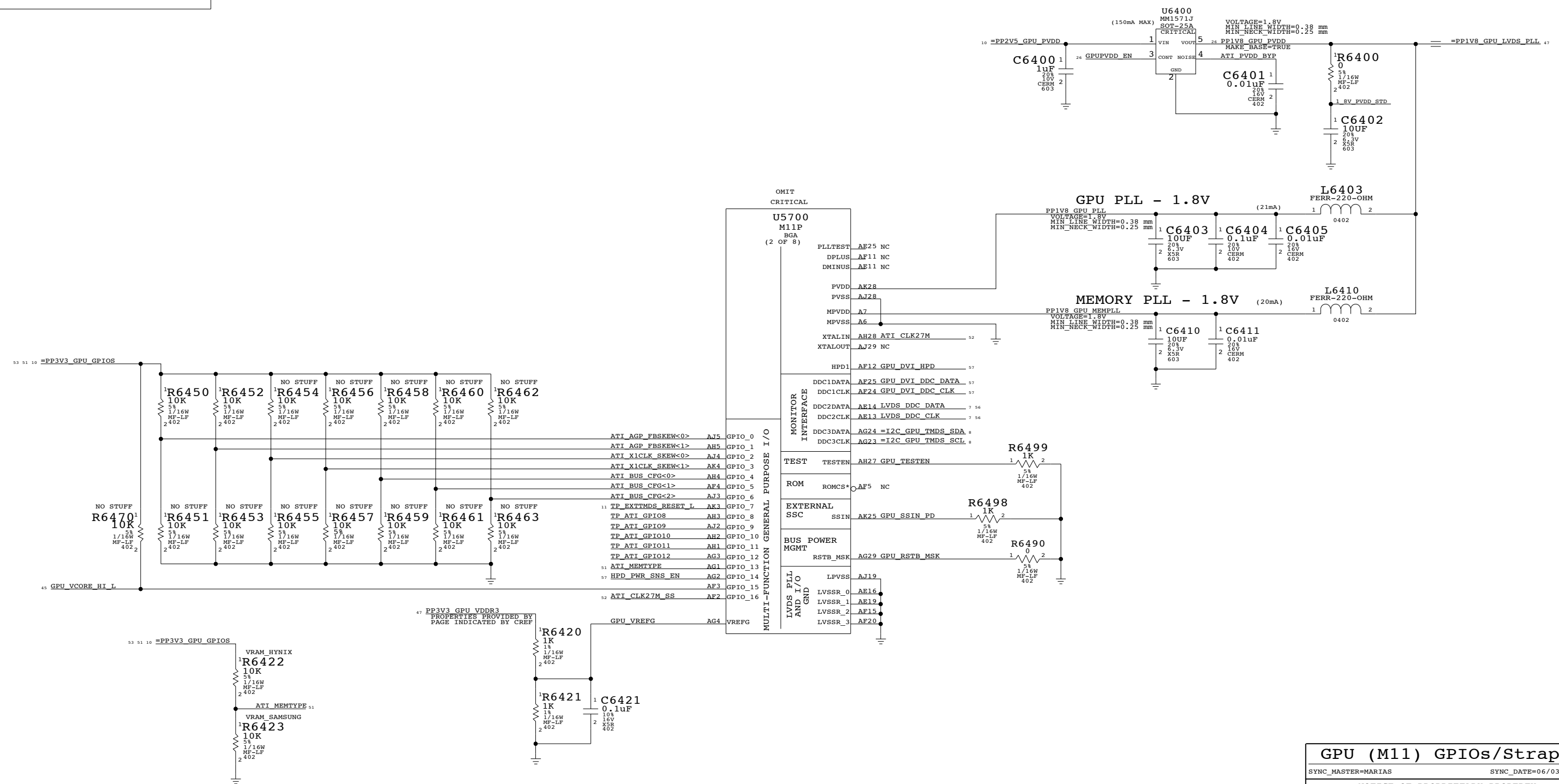
C

B

B

A

A



GPU (M11) GPIOs/Straps

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6839	02
SCALE	SHT	OF	
NONE	64	115	

Page Notes

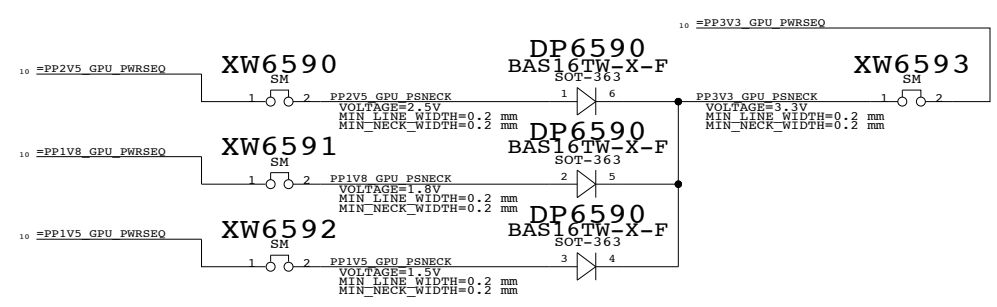
Power aliases required by this page:
 - =PP3V3_GPU_CLOCKS - =PP3V3_GPU_PWRSEQ
 - =PPVIN_GPU_LVDDR_LDO - =PP2V5_GPU_PWRSEQ
 - =PP2V5_GPU_LVDDR_LDO - =PP1V8_GPU_PWRSEQ
 - =PP1V5_GPU_PWRSEQ

Signal aliases required by this page:
 (NONE)

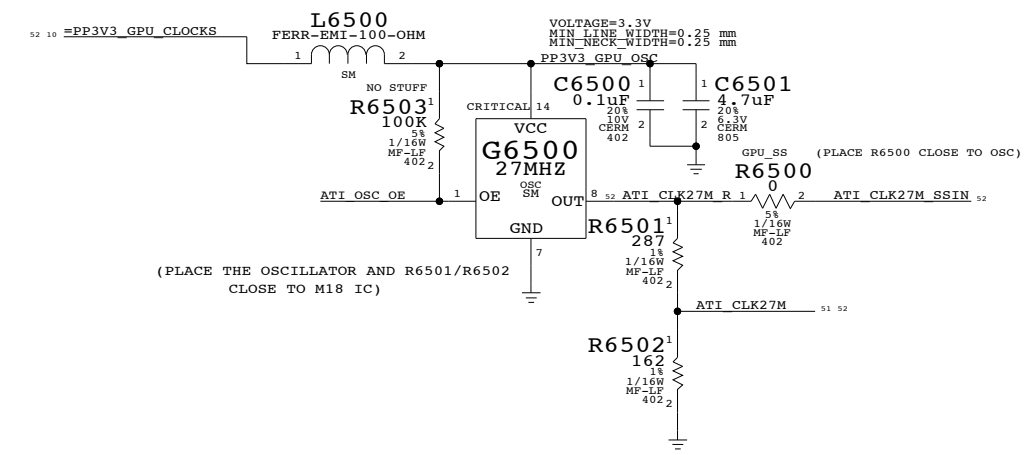
BOM options provided by this page:
 - GPU_SS - GPU_LVDDR_2V8

ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
R50	ATI_CLK27M	CLOCK	CLOCK
R54	ATI_CLK27M	CLOCK	CLOCK
R55	ATI_CLK27M	CLOCK	CLOCK
R51	ATI_CLK27M_SS	CLOCK	CLOCK
R52	ATI_CLK27M_SS	CLOCK	CLOCK

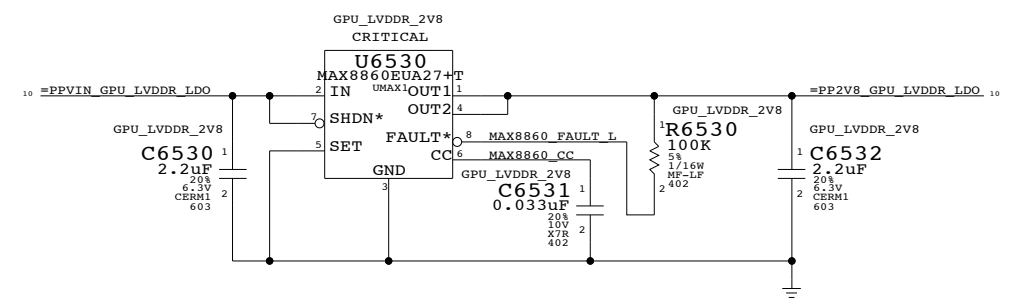
M11 Power Shutdown Sequencing



27M OSC

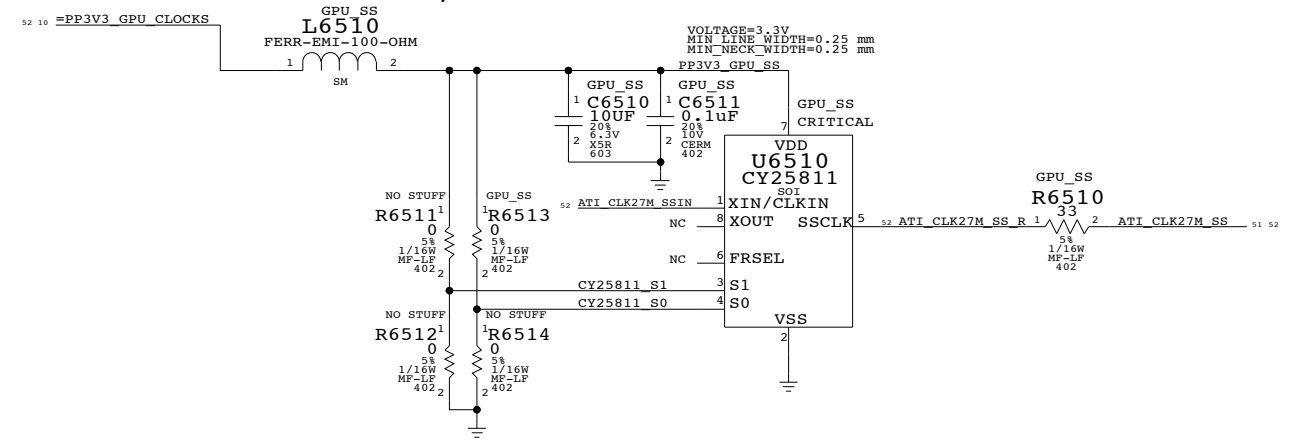


LVDDR 2.8V LDO



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
35380647	35381140	GPU_LVDDR_2V8	U6530	2.82V instead of 2.77V

SPREAD SPECTRUM SUPPORT
 S0=1;S1=M => -1.5% DOWN-SPREAD



GPU (M11) Clocks/Misc

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6839	02
SCALE	NONE	SHT OF	65 OF 115

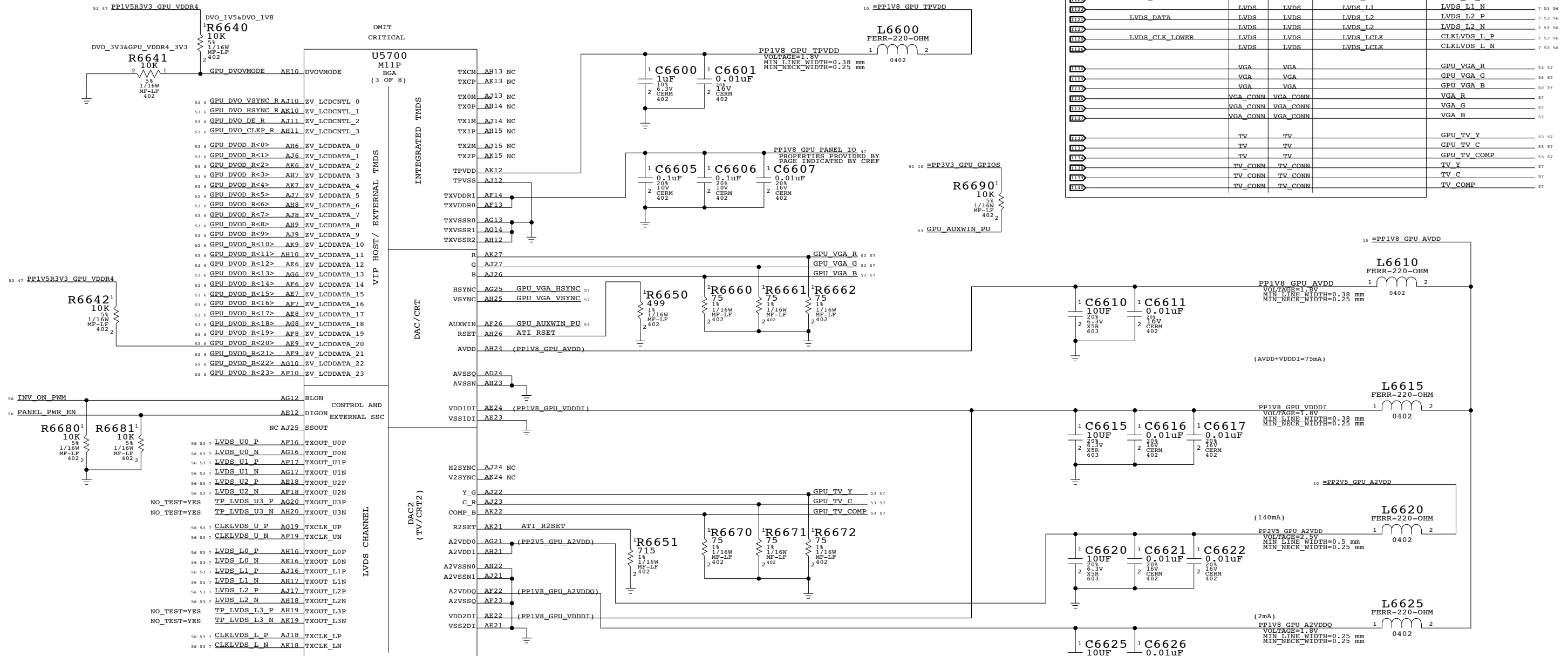
Page Notes

Power aliases required by this page:
 - =PP2V5_GPU_A2VDD - =PP1V8_GPU_AVDD
 - =PP1V8_GPU_TPVD - =PP3V3_GPU_GPIOS

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - DVO_1V5 - GPU_VDDR4_3V3
 - DVO_1V8 - DVO_3V3

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		DIFFERENTIAL_PAIR	
	SPACING	PHYSICAL		
R660	DVO	DVO	GPU DVOD R<23..0>	6 53
R660	DVO	DVO	GPU DVO_HSYNC_R	6 53
R660	DVO	DVO	GPU DVO_VSYNC_R	6 53
R660	DVO	DVO	GPU DVO_DE_R	6 53
R660	DVO	DVO	GPU DVO_CLKP_R	6 53
R660	LVDS_DATA	LVDS	LVDS_U0	7 53 56
R660	LVDS_DATA	LVDS	LVDS_U0_P	7 53 56
R660	LVDS_DATA	LVDS	LVDS_U0_N	7 53 56
R660	LVDS_DATA	LVDS	LVDS_U1_P	7 53 56
R660	LVDS_DATA	LVDS	LVDS_U1_N	7 53 56
R660	LVDS_DATA	LVDS	LVDS_U2_P	7 53 56
R660	LVDS_DATA	LVDS	LVDS_U2_N	7 53 56
R660	LVDS_CLK_UPPER	LVDS	LVDS_UCLK	7 53 56
R660	LVDS_CLK_UPPER	LVDS	CLKLVDS_U_P	7 53 56
R660	LVDS_CLK_UPPER	LVDS	CLKLVDS_U_N	7 53 56
R660	LVDS_DATA	LVDS	LVDS_L0	7 53 56
R660	LVDS_DATA	LVDS	LVDS_L0_P	7 53 56
R660	LVDS_DATA	LVDS	LVDS_L0_N	7 53 56
R660	LVDS_DATA	LVDS	LVDS_L1_P	7 53 56
R660	LVDS_DATA	LVDS	LVDS_L1_N	7 53 56
R660	LVDS_DATA	LVDS	LVDS_L2_P	7 53 56
R660	LVDS_DATA	LVDS	LVDS_L2_N	7 53 56
R660	LVDS_CLK_LOWER	LVDS	LVDS_LCLK	7 53 56
R660	LVDS_CLK_LOWER	LVDS	CLKLVDS_L_P	7 53 56
R660	LVDS_CLK_LOWER	LVDS	CLKLVDS_L_N	7 53 56
R660	VGA	VGA	GPU VGA_R	57
R660	VGA	VGA	GPU VGA_G	57
R660	VGA	VGA	GPU VGA_B	57
R660	VGA_CONN	VGA_CONN	VGA_R	57
R660	VGA_CONN	VGA_CONN	VGA_G	57
R660	VGA_CONN	VGA_CONN	VGA_B	57
R660	TV	TV	GPU TV_Y	57
R660	TV	TV	GPU TV_C	57
R660	TV	TV	GPU TV_COMP	57
R660	TV_CONN	TV_CONN	TV_Y	57
R660	TV_CONN	TV_CONN	TV_C	57
R660	TV_CONN	TV_CONN	TV_COMP	57



GPU (M11) DVI/DAC Outputs

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	D	051-6839	02
SCALE	SHT	OF	
NONE	66	115	

Page Notes

Power aliases required by this page:
 - =PP3V3_RUN_SI

Signal aliases required by this page:
 - =SI_I2C_CLK - =SI_TMDS_RESET_L
 - =SI_I2C_DATA - =RP68xxPy (pinswappable series R)

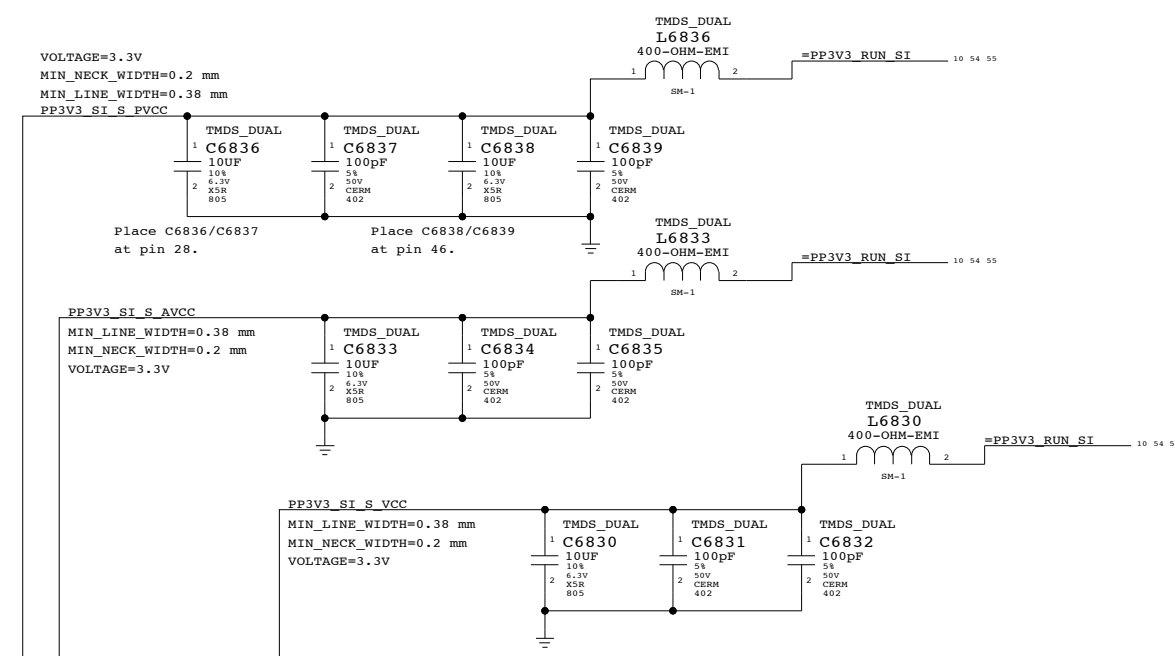
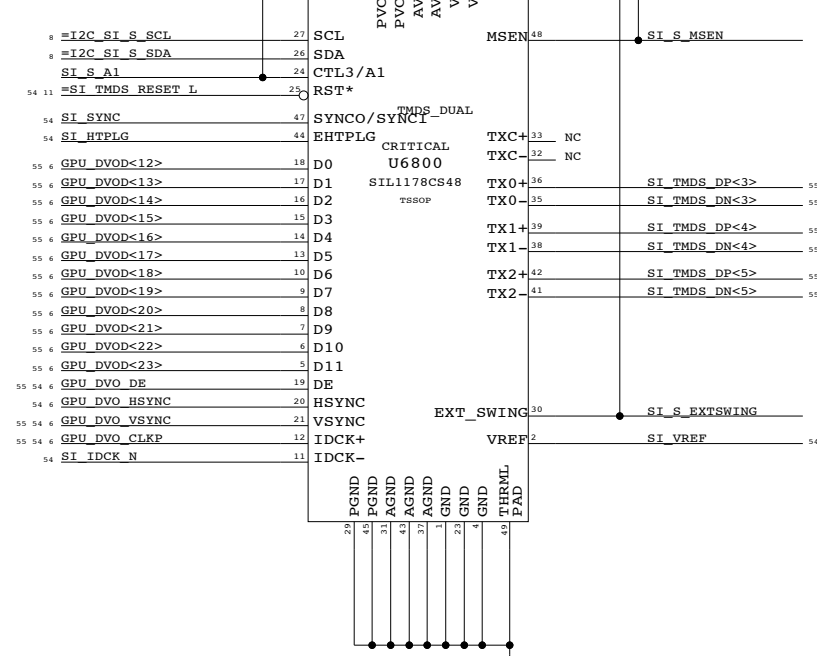
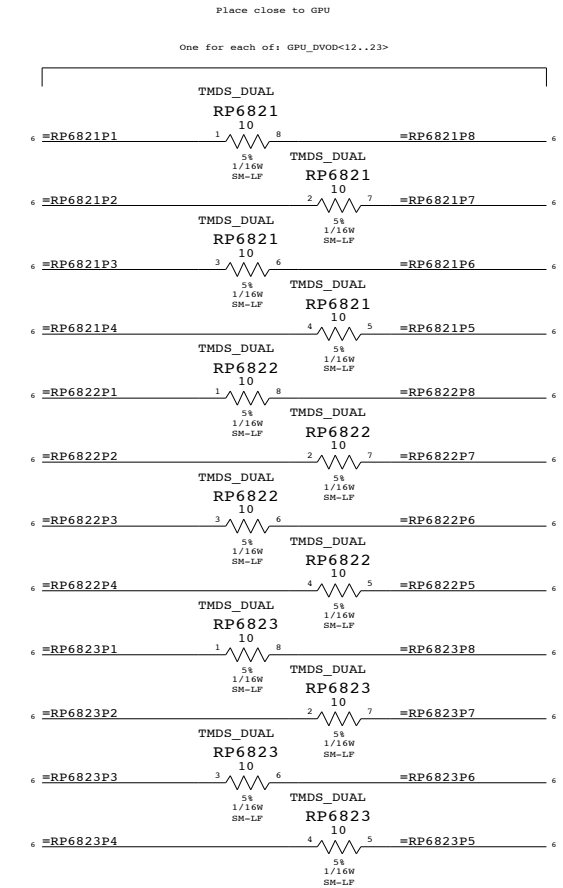
BOM options provided by this page:
 - TMDS_DUAL

Net Spacing Type: TMDS
 Net Physical Type: TMDS

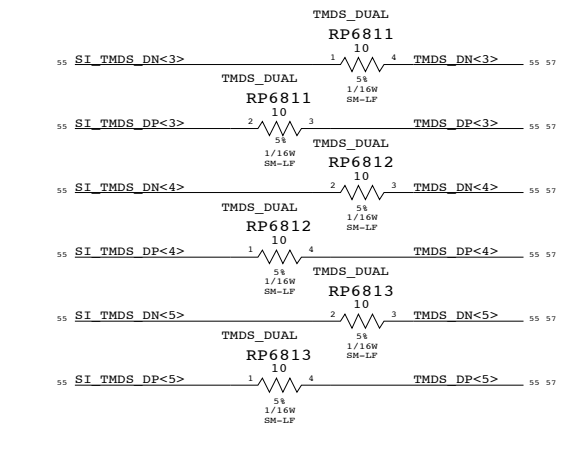
NOTE: Target differential impedance for TMDS data pairs is 100 ohms.

ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
GPU_DVO_UPPER	DVO	DVO	
GPU_DVOD20	DVO	DVO	
GPU_DVO_UPPER	DVO	DVO	
	PROVIDED BY LOWER TXMR		
	PROVIDED BY LOWER TXMR		
	PROVIDED BY LOWER TXMR		
TMDS_DATA	TMDS	TMDS	SI_TMDS_D3
TMDS_DATA	TMDS	TMDS	SI_TMDS_D3
TMDS_DATA	TMDS	TMDS	SI_TMDS_D4
TMDS_DATA	TMDS	TMDS	SI_TMDS_D4
TMDS_DATA	TMDS	TMDS	SI_TMDS_D5
TMDS_DATA	TMDS	TMDS	SI_TMDS_D5
	TMDS	TMDS	TMDS_D3
	TMDS	TMDS	TMDS_D3
	TMDS	TMDS	TMDS_D4
	TMDS	TMDS	TMDS_D4
	TMDS	TMDS	TMDS_D5
	TMDS	TMDS	TMDS_D5

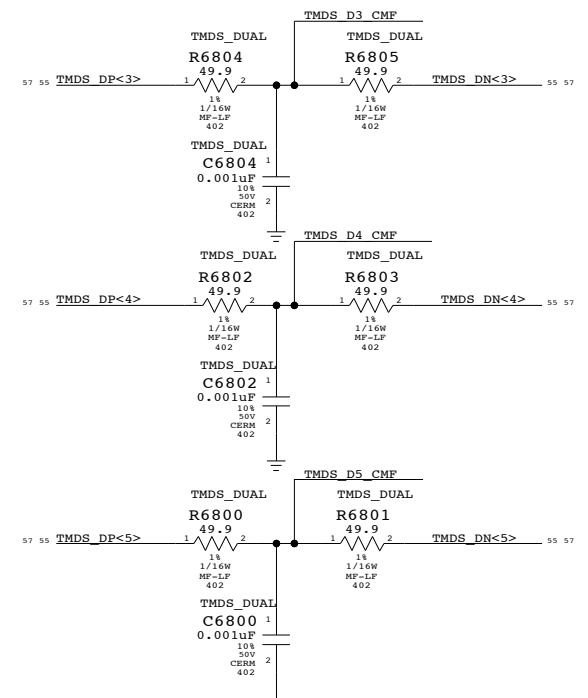
Upper DVO series termination



Upper Channel Series Termination



Upper Channel Common-mode Termination



Upper TMDS Transmitter
 SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

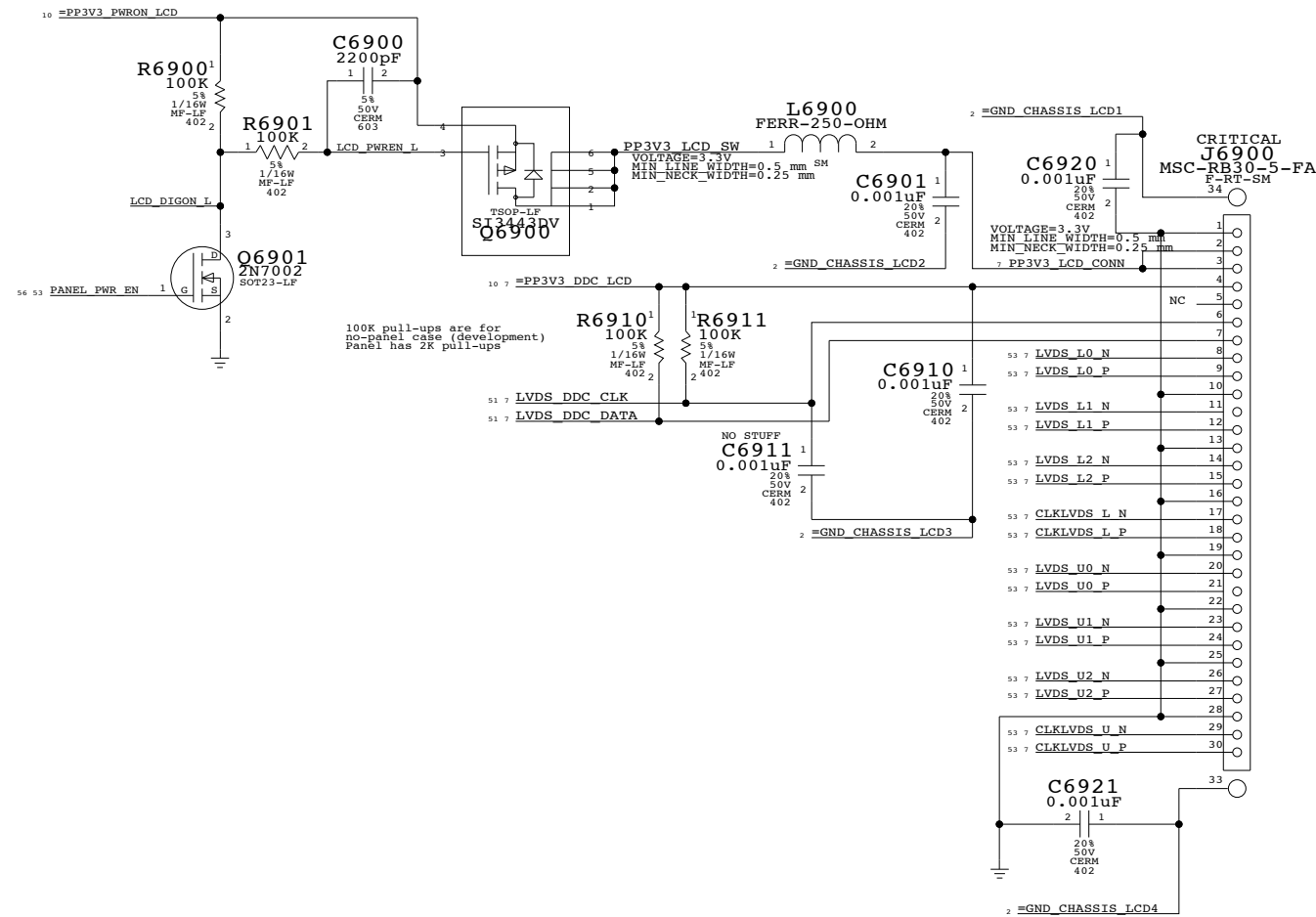
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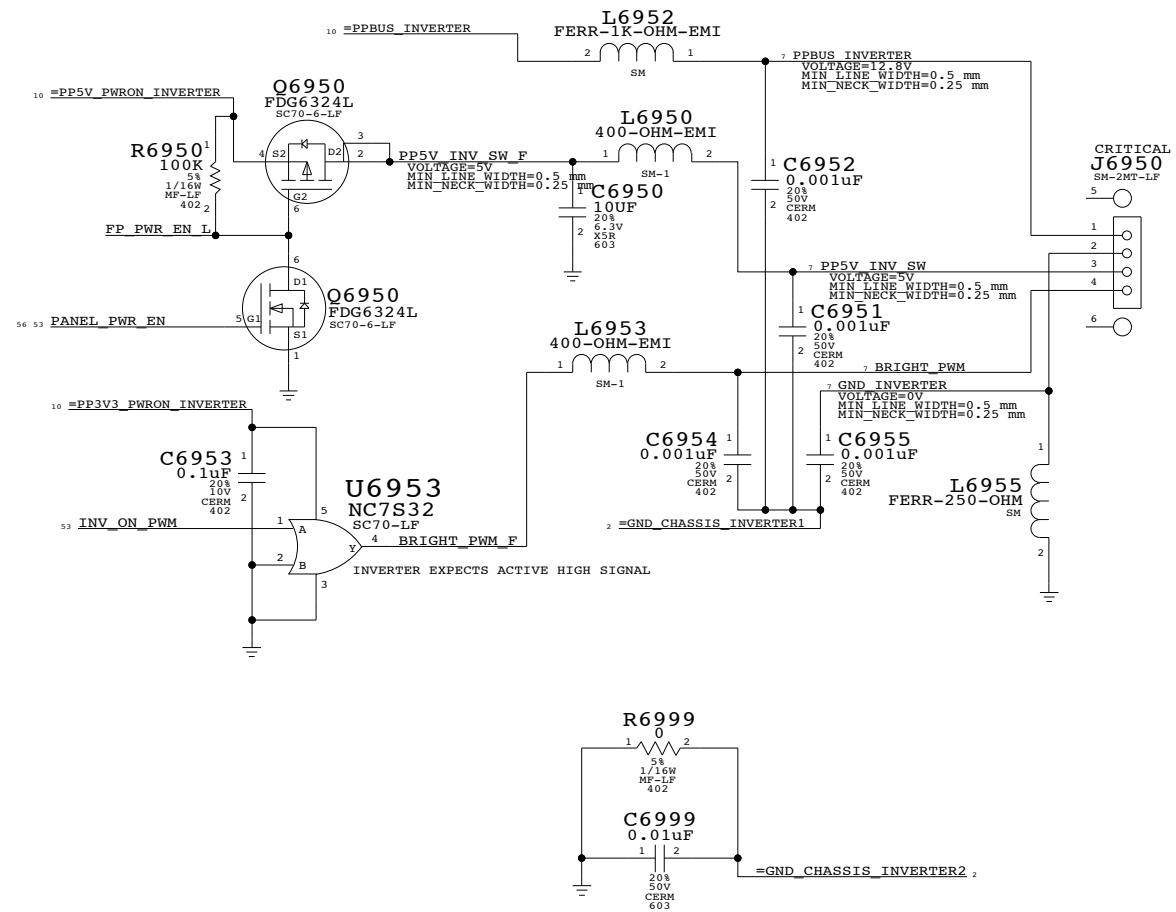
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SCALE	SHT	OF	
NONE	68	115	

LCD (LVDS) INTERFACE



INVERTER INTERFACE



Internal Display Conns

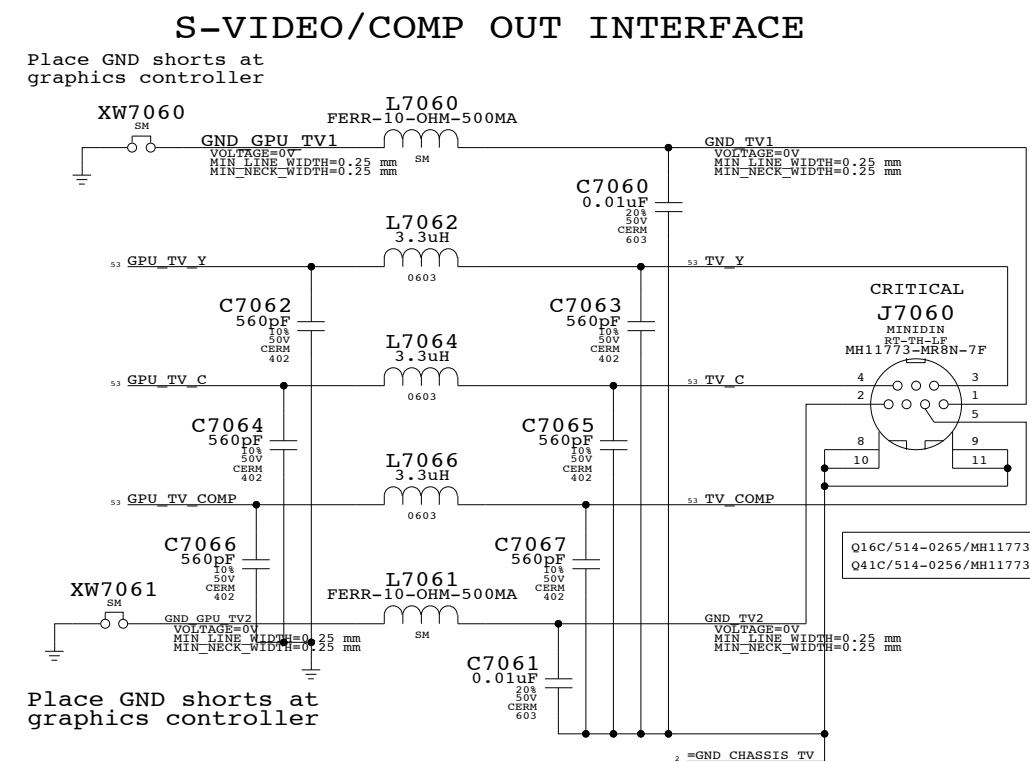
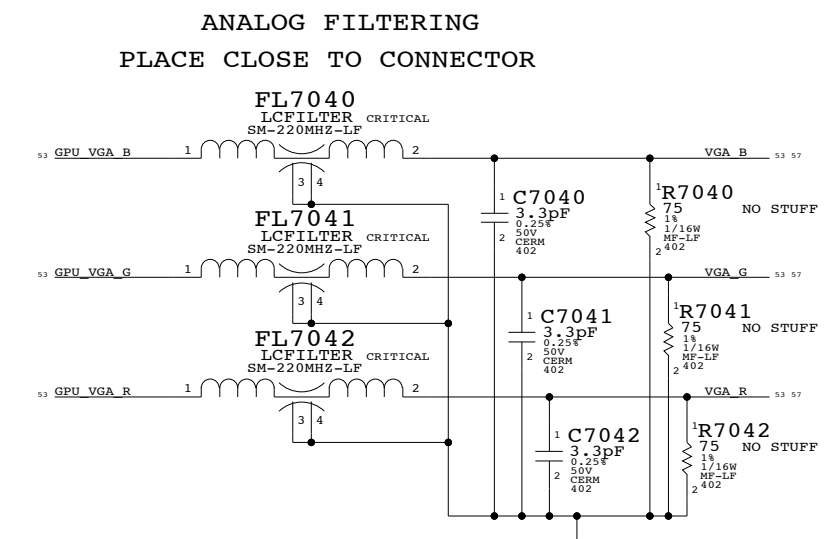
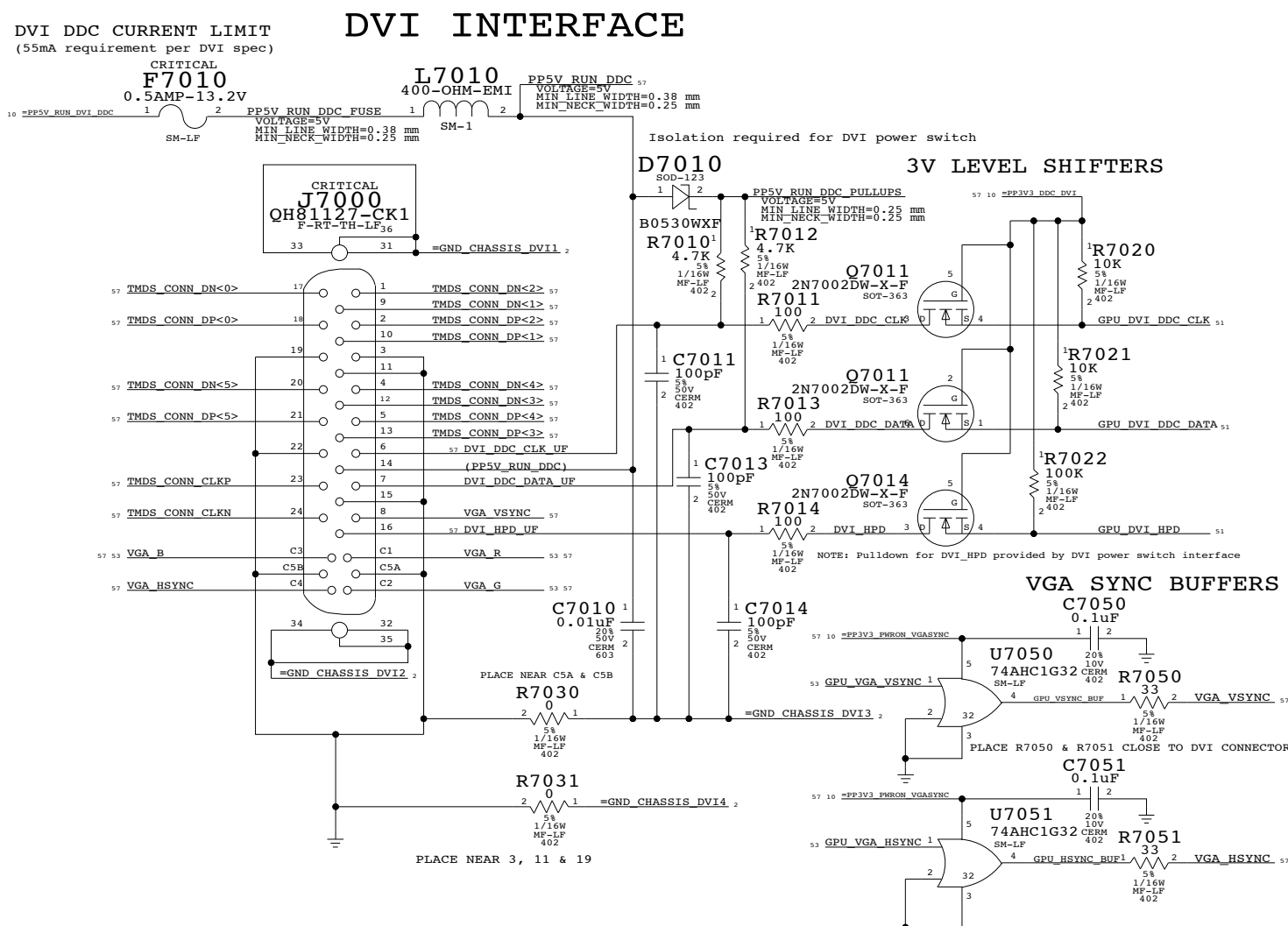
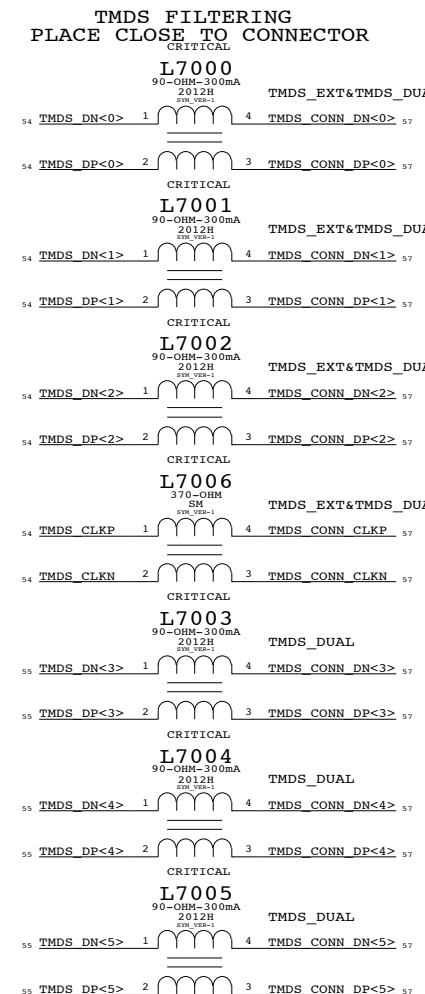
SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

NOTICE OF PROPRIETARY PROPERTY

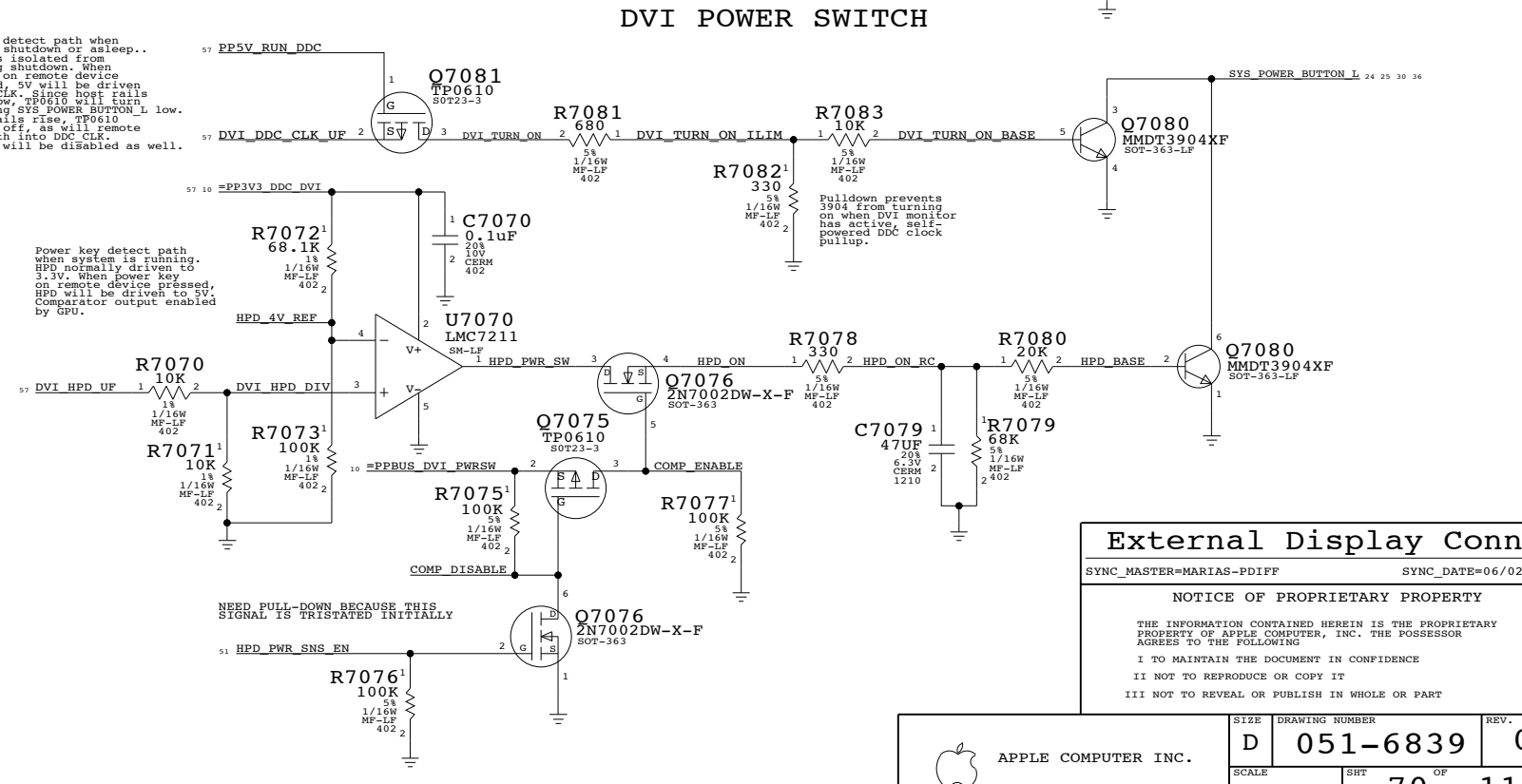
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	D	051-6839	02
SCALE	NONE	SHT	OF
		69	115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_CLK	TMDS_CONN_CLK
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_CLKN	TMDS_CONN_CLKN
E550	TMDS_CONN_TMDS_CONN		TMDS_CONN_D0	TMDS_CONN_DP<0>
E550	TMDS_CONN_TMDS_CONN		TMDS_CONN_D0	TMDS_CONN_DP<0>
E550	TMDS_CONN_TMDS_CONN		TMDS_CONN_D1	TMDS_CONN_DP<1>
E550	TMDS_CONN_TMDS_CONN		TMDS_CONN_D1	TMDS_CONN_DP<1>
E550	TMDS_CONN_TMDS_CONN		TMDS_CONN_D2	TMDS_CONN_DP<2>
E550	TMDS_CONN_TMDS_CONN		TMDS_CONN_D2	TMDS_CONN_DP<2>
E550	TMDS_CONN_TMDS_CONN		TMDS_CONN_D3	TMDS_CONN_DP<3>
E550	TMDS_CONN_TMDS_CONN		TMDS_CONN_D3	TMDS_CONN_DP<3>
E560	TMDS_CONN_TMDS_CONN		TMDS_CONN_D4	TMDS_CONN_DP<4>
E560	TMDS_CONN_TMDS_CONN		TMDS_CONN_D4	TMDS_CONN_DP<4>
E560	TMDS_CONN_TMDS_CONN		TMDS_CONN_D5	TMDS_CONN_DP<5>
E560	TMDS_CONN_TMDS_CONN		TMDS_CONN_D5	TMDS_CONN_DP<5>



Power key detect path when system is shutdown or asleep... DDC CLK is isolated from GPU during shutdown. When power key or remote device is pressed, 5V will be driven into DDC CLK. Since hot rails will be low, TP0610 will turn on, driving SYS_POWER_BUTTON_L low. As hot rails rise, TP0610 will turn off, as will remote device path into DDC CLK. Isolation will be disabled as well.



External Display Conns

SYNC_MASTER=MARIAS-PDIFF SYNC_DATE=06/02/2005

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SCALE	SHT	OF	
NONE	70	115	

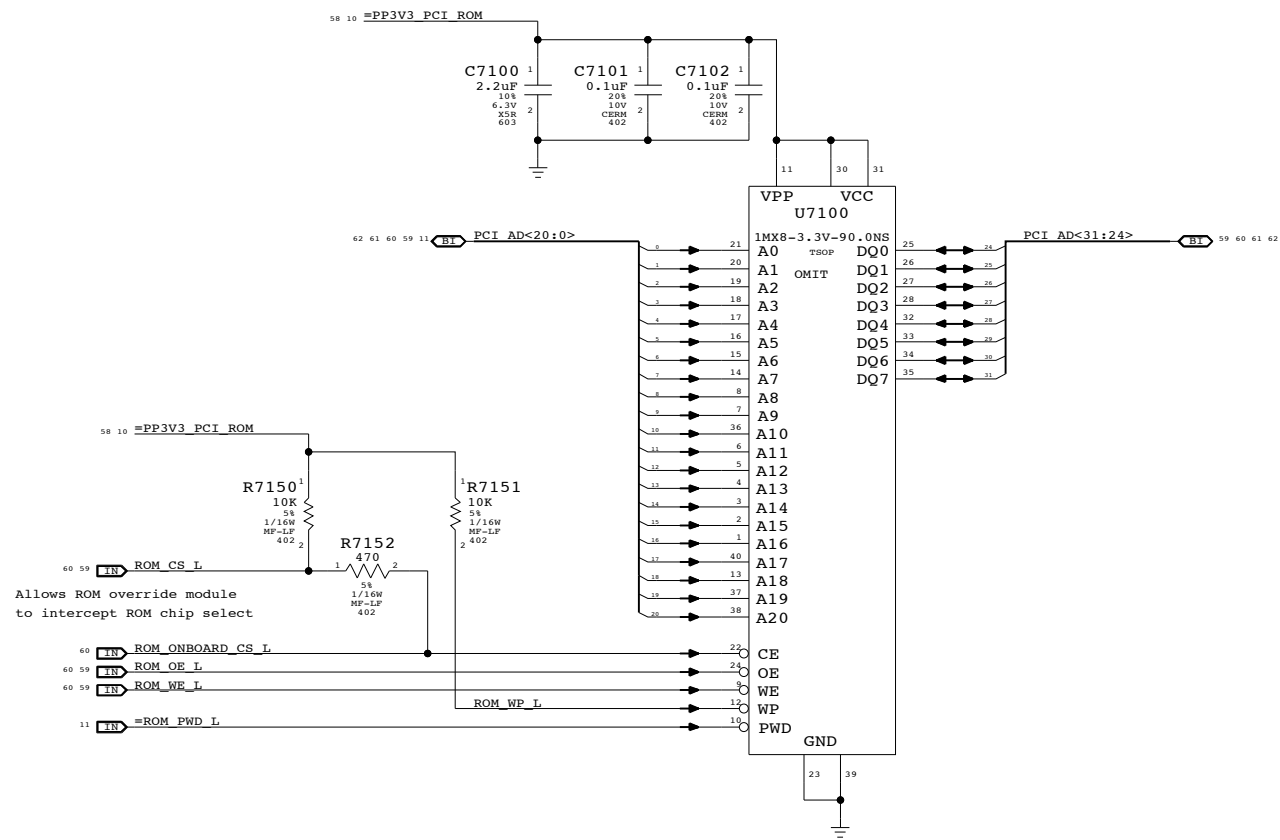
Page Notes

Power aliases required by this page:
 - =PP3V3_PCI_ROM

Signal aliases required by this page:
 - =ROM_PWD_L

BOM options provided by this page:
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NOTE: This page does not specify a BootROM part number. Must use a TABLE_x_ITEM symbol to declare U7100 part number.



BootROM

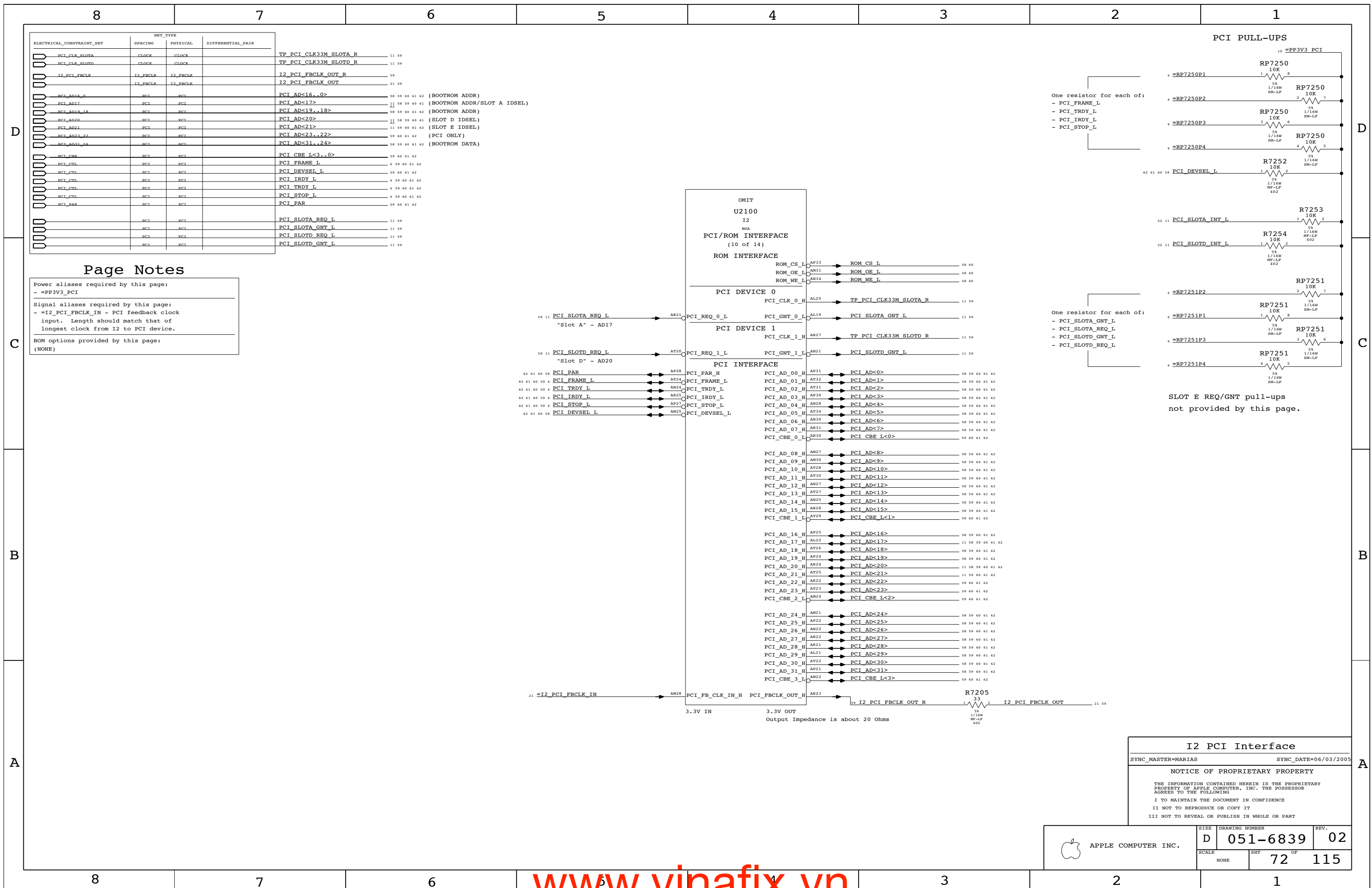
SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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	D	051-6839	02
SCALE	SHT	OF	
NONE	71	115	



ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
PCI_CLK_SLOTA	CLOCK	CLOCK	
PCI_CLK_SLOTD	CLOCK	CLOCK	
I2_PCI_FBCLK	I2_FBCLK	I2_FBCLK	
PCI_AD<16..0>	PCI	PCI	
PCI_AD<17>	PCI	PCI	
PCI_AD<19..18>	PCI	PCI	
PCI_AD<20>	PCI	PCI	
PCI_AD<21>	PCI	PCI	
PCI_AD<23..22>	PCI	PCI	
PCI_AD<31..24>	PCI	PCI	
PCI_CBE	PCI	PCI	
PCI_CBE_L<3..0>	PCI	PCI	
PCI_FRAME_L	PCI	PCI	
PCI_DEVSEL_L	PCI	PCI	
PCI_IRDY_L	PCI	PCI	
PCI_TRDY_L	PCI	PCI	
PCI_STOP_L	PCI	PCI	
PCI_PAR	PCI	PCI	
PCI_SLOTA_REQ_L	PCI	PCI	
PCI_SLOTA_GNT_L	PCI	PCI	
PCI_SLOTD_REQ_L	PCI	PCI	
PCI_SLOTD_GNT_L	PCI	PCI	

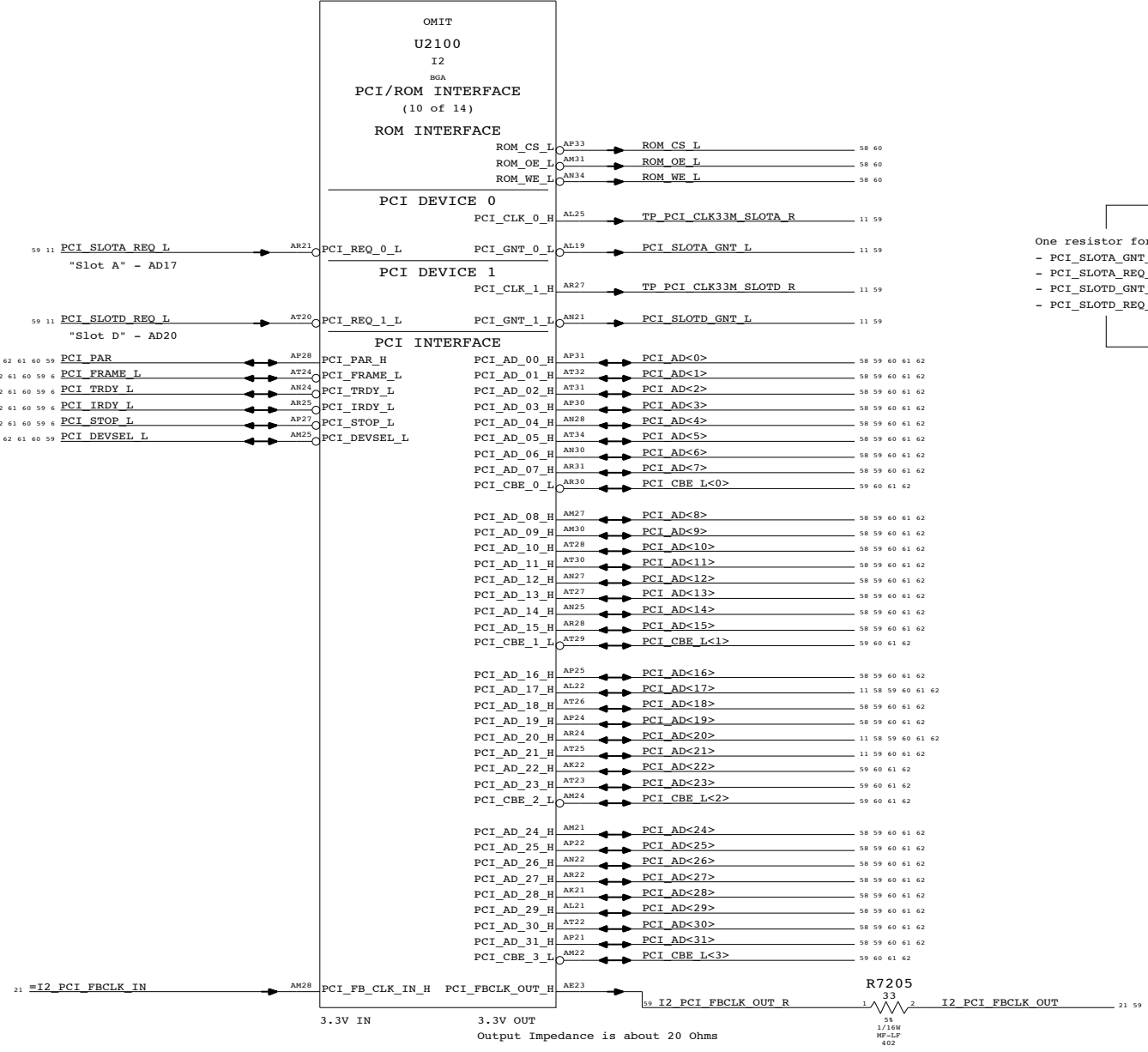
TP_PCI_CLK33M_SLOTA_R	11 59	
TP_PCI_CLK33M_SLOTD_R	11 59	
I2_PCI_FBCLK_OUT_R	59	
I2_PCI_FBCLK_OUT	21 59	
PCI_AD<16..0>	58 59 60 61 62	(BOOTROM ADDR)
PCI_AD<17>	11 58 59 60 61	(BOOTROM ADDR/SLOT A IDSEL)
PCI_AD<19..18>	58 59 60 61 62	(BOOTROM ADDR)
PCI_AD<20>	11 58 59 60 61	(SLOT D IDSEL)
PCI_AD<21>	11 59 60 61 62	(SLOT E IDSEL)
PCI_AD<23..22>	59 60 61 62	(PCI ONLY)
PCI_AD<31..24>	58 59 60 61 62	(BOOTROM DATA)
PCI_CBE_L<3..0>	59 60 61 62	
PCI_FRAME_L	6 59 60 61 62	
PCI_DEVSEL_L	59 60 61 62	
PCI_IRDY_L	6 59 60 61 62	
PCI_TRDY_L	6 59 60 61 62	
PCI_STOP_L	6 59 60 61 62	
PCI_PAR	59 60 61 62	
PCI_SLOTA_REQ_L	11 59	
PCI_SLOTA_GNT_L	11 59	
PCI_SLOTD_REQ_L	11 59	
PCI_SLOTD_GNT_L	11 59	

Page Notes

Power aliases required by this page:
 - =PP3V3_PCI

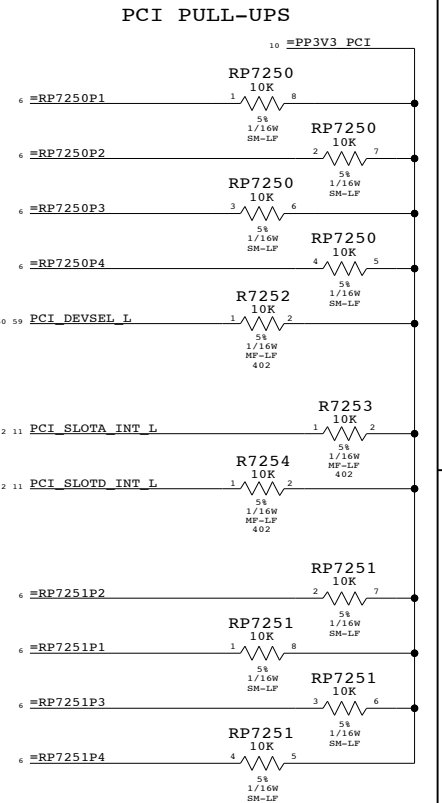
Signal aliases required by this page:
 - =I2_PCI_FBCLK_IN - PCI feedback clock input. Length should match that of longest clock from I2 to PCI device.

BOM options provided by this page:
 (NONE)



One resistor for each of:
 - PCI_FRAME_L
 - PCI_TRDY_L
 - PCI_IRDY_L
 - PCI_STOP_L

One resistor for each of:
 - PCI_SLOTA_GNT_L
 - PCI_SLOTA_REQ_L
 - PCI_SLOTD_GNT_L
 - PCI_SLOTD_REQ_L



SLOT E REQ/GNT pull-ups not provided by this page.

I2 PCI Interface

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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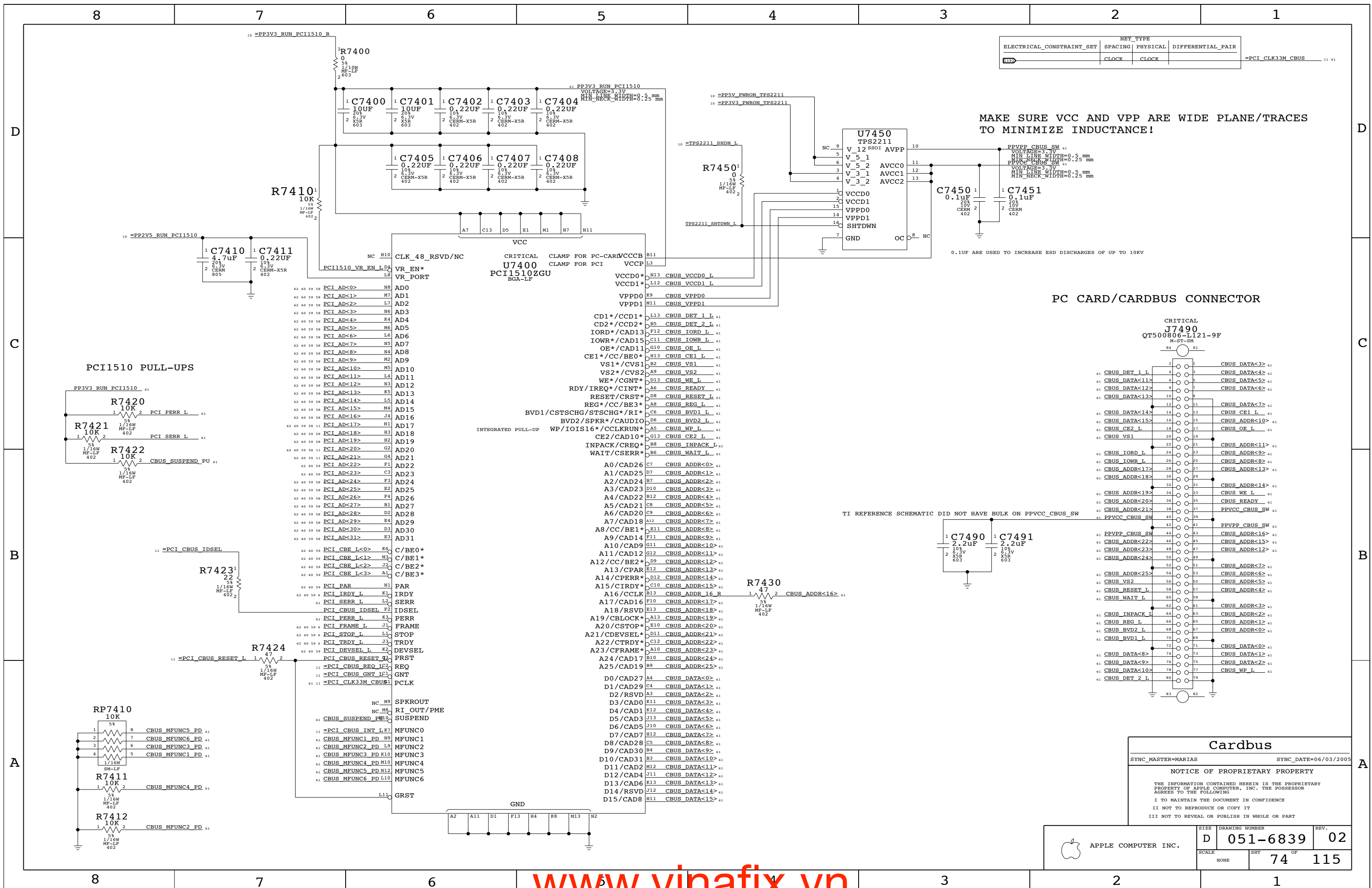
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SCALE	NONE	SHT	OF
		72	115

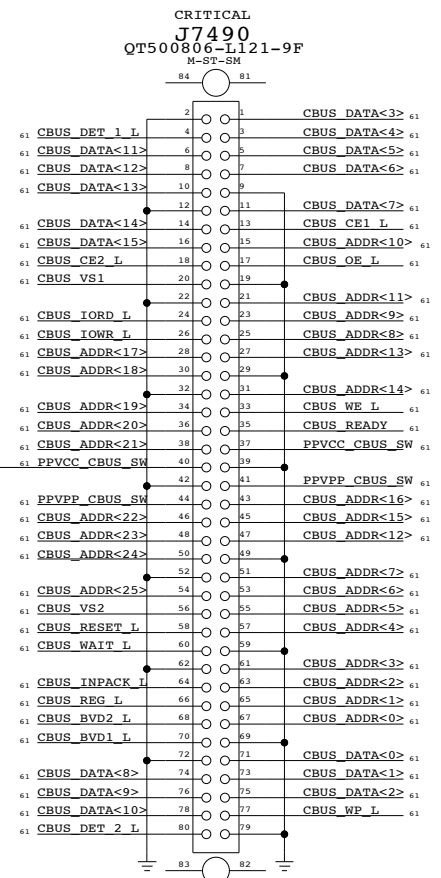


NET TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
E12	CLOCK	CLOCK	

MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES TO MINIMIZE INDUCTANCE!

0.1uF ARE USED TO INCREASE ESD DISCHARGES OF UP TO 10Kv

PC CARD/CARDBUS CONNECTOR



Cardbus

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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	D	051-6839	02
SCALE	SHT	OF	
NONE	74	115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		DIFFERENTIAL_PAIR
	SPACING	PHYSICAL	
10	CLOCK	CLOCK	

=PCI_CLK33M_USB2 11 02

Page Notes

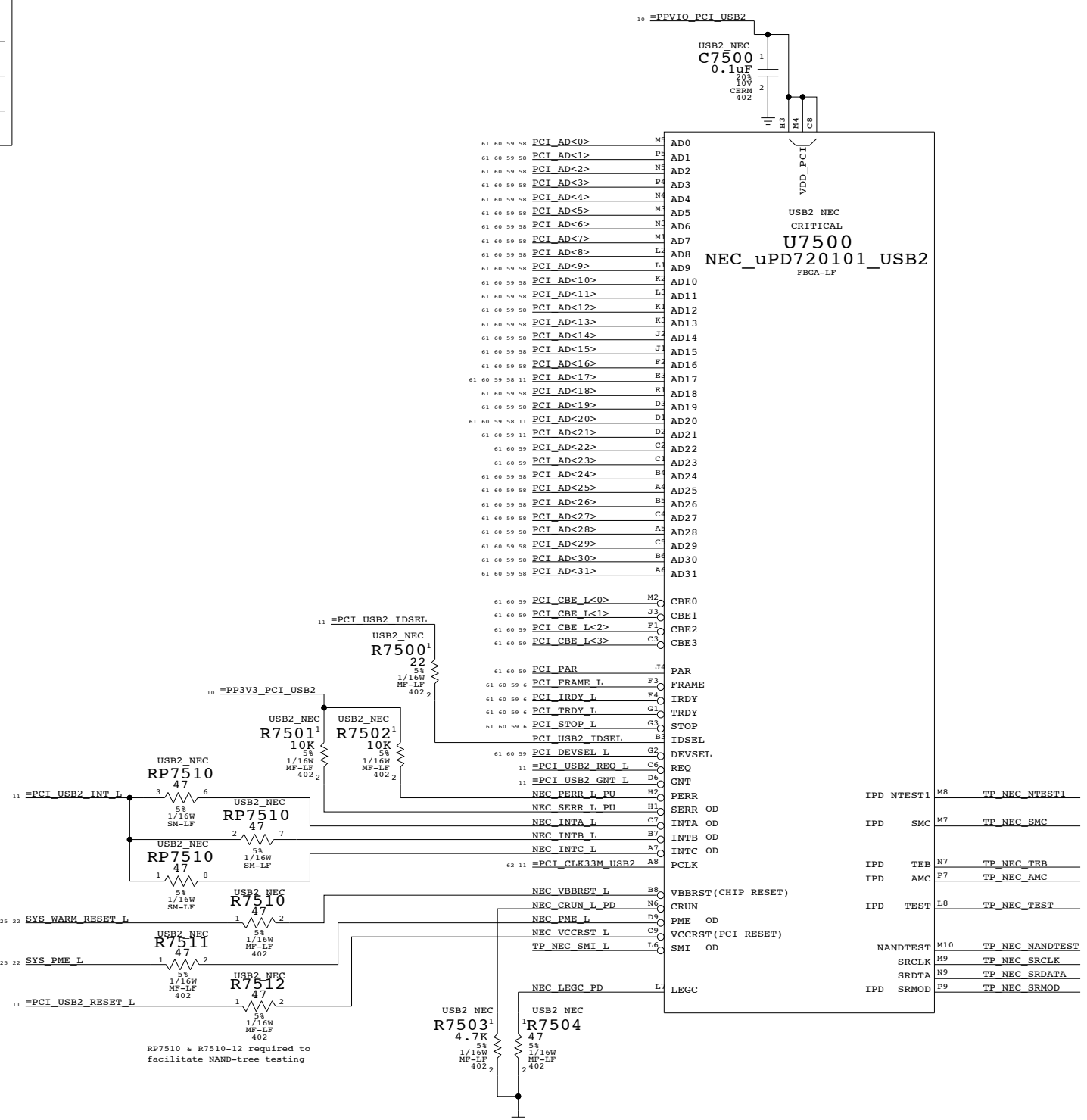
Power aliases required by this page:
 - =PPVIO_PCI (to 3.3V or 5V)
 - =PP3V3_PCI_USB2 (D3cold rail)

Signal aliases required by this page:
 - =PCI_CLK33M_USB2
 - =PCI_USB2_REQ_L - =PCI_USB2_IDSEL
 - =PCI_USB2_GNT_L - =PCI_USB2_RESET_L
 - =PCI_USB2_INT_L

BOM options provided by this page:
 - USB2_NEC

PCI Devices implemented on this page:
 AD27 (Slot "G") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports D3cold.



RP7510 & R7510-12 required to facilitate NAND-tree testing

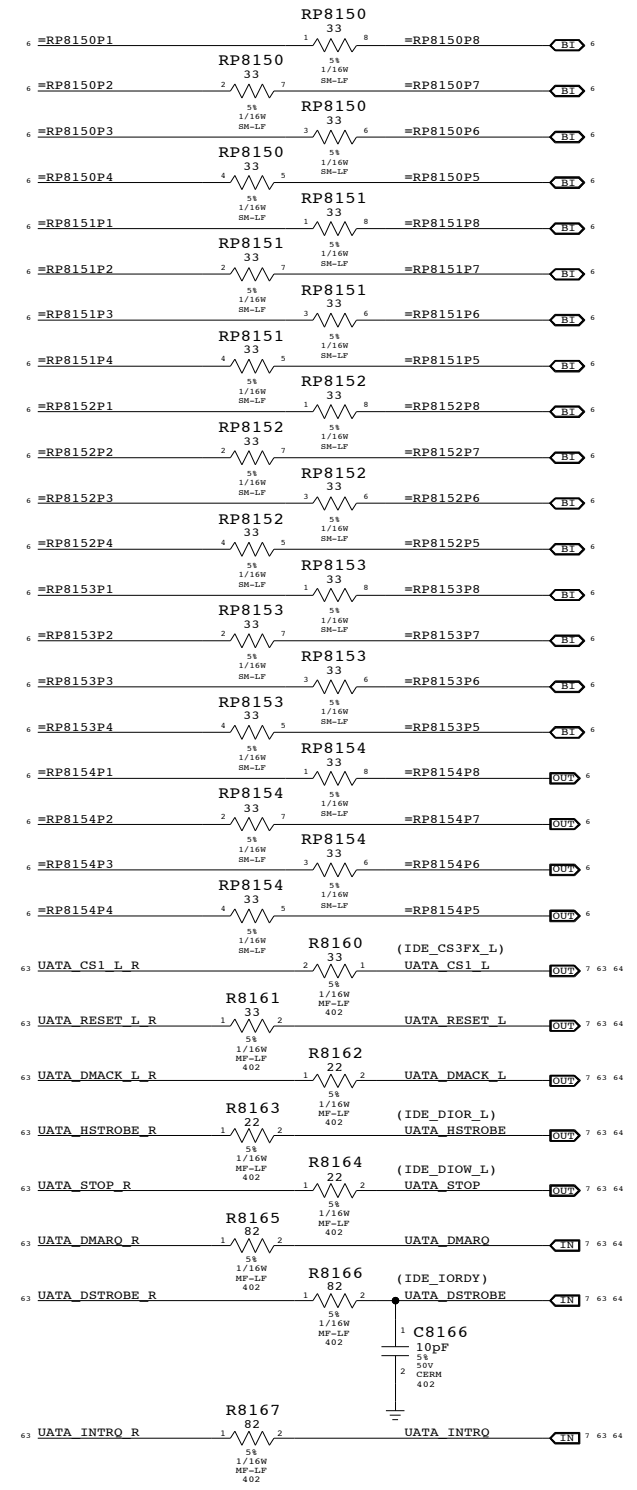
NEC USB2		
SYNC_MASTER=MARIAS	SYNC_DATE=06/03/2005	
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6839	02
SCALE	SHT	OF	
NONE	75	115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	SPACING	PHYSICAL		
UATA_DD R<15..8>	DATA	DATA	UATA_DD R<15..8>	6 63
UATA_DD7	DATA	DATA	UATA_DD R<7>	6 63
UATA_DD	DATA	DATA	UATA_DD R<6..0>	6 63
UATA_HOIST	DATA	DATA	UATA_DA R<2..0>	6 63
UATA_HOIST	DATA	DATA	UATA_CS0 L R	6 63
UATA_HOIST	DATA	DATA	UATA_CS1 L R	6 63
UATA_HSTROBE	DATA	DATA	UATA_HSTROBE R	6 63
UATA_HOIST	DATA	DATA	UATA_STOP R	6 63
UATA_HOIST_R	DATA	DATA	UATA_DMACK L R	6 63
UATA_HOIST_R	DATA	DATA	UATA_RESET L R	6 63
UATA_HSTROBE	DATA	DATA	UATA_DSTROBE R	6 63
UATA_DEV_R	DATA	DATA	UATA_DMARQ R	6 63
UATA_DEV_R	DATA	DATA	UATA_INTRQ R	6 63
UATA_DEV_R	DATA	DATA	UATA_DD<15..0>	6 7 64
UATA_DEV_R	DATA	DATA	UATA_DA<2..0>	6 7 64
UATA_DEV_R	DATA	DATA	UATA_CS0 L	6 7 64
UATA_DEV_R	DATA	DATA	UATA_CS1 L	6 7 63 64
UATA_DEV_R	DATA	DATA	UATA_HSTROBE	6 7 63 64
UATA_DEV_R	DATA	DATA	UATA_STOP	6 7 63 64
UATA_DEV_R	DATA	DATA	UATA_DMACK L	6 7 63 64
UATA_DEV_R	DATA	DATA	UATA_RESET L	6 7 63 64
UATA_DEV_R	DATA	DATA	UATA_DSTROBE	6 7 63 64
UATA_DEV_R	DATA	DATA	UATA_DMARQ	6 7 63 64
UATA_DEV_R	DATA	DATA	UATA_INTRQ	6 7 63 64

UATA100 SERIES TERMINATION

PLACE CLOSE TO I2



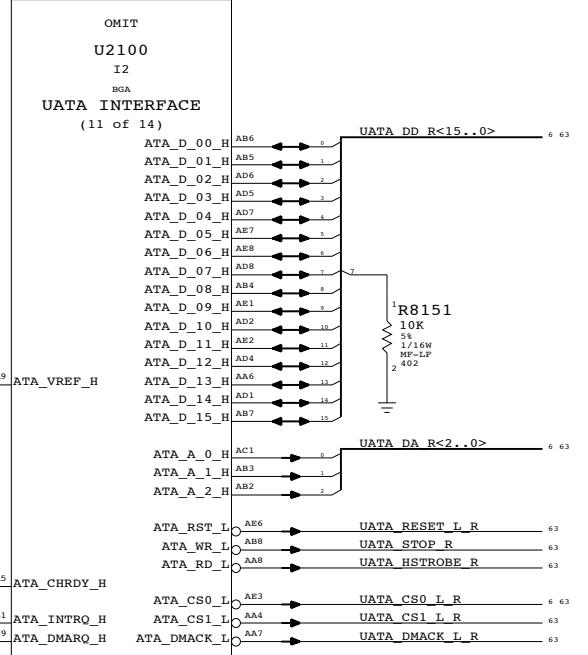
One resistor for each of:
 - UATA_DD<15..0>(_R)
 - UATA_DA<2..0>(_R)
 - UATA_CS0 L(_R)
 (IDE_CS1FX_L)

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



I2 UATA Interface
 SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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SCALE	NONE	SHT	OF
		81	115

D

D

C

C

B

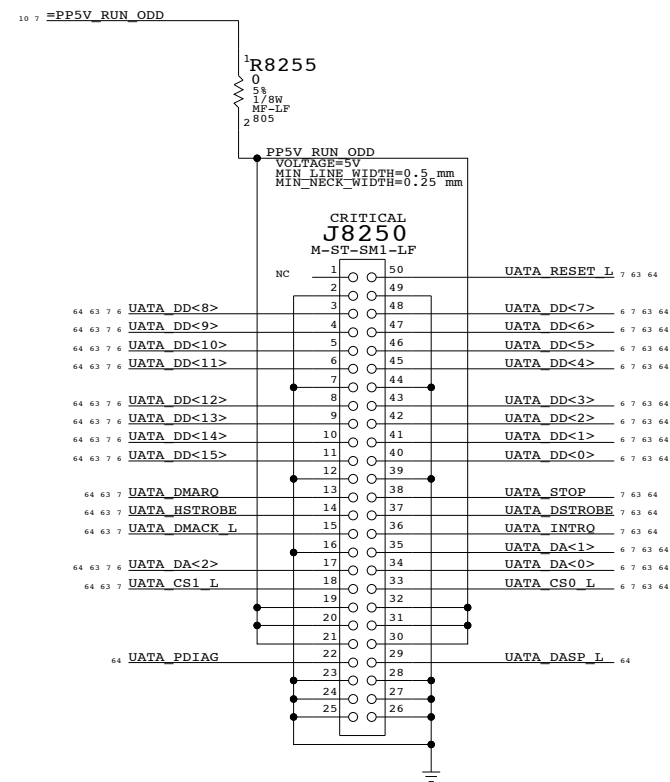
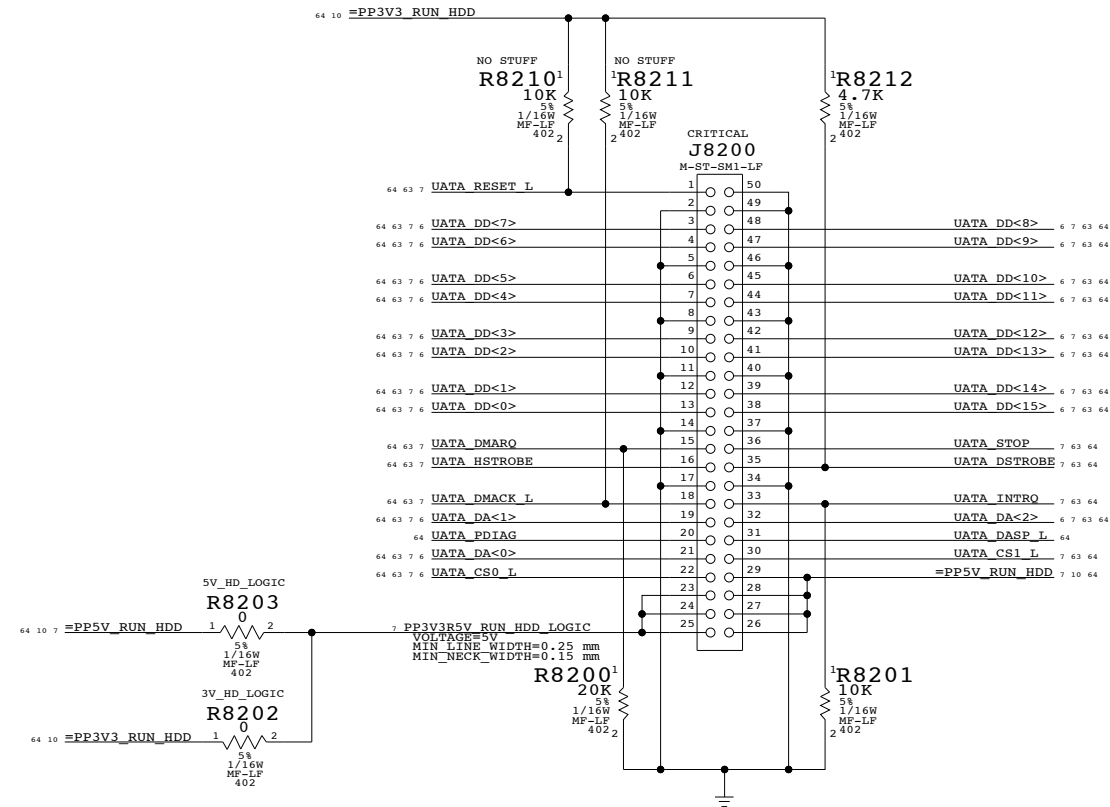
B

A

A

HDD CONNECTOR

ODD CONNECTOR



ATA Connectors
 Q16C/516S0357/M-ST-SM2-LF
 Q41C/516S0335/M-ST-SM1-LF

HDD/ODD Connectors
 SYNC_MASTER=MARIAS-PDIFF SYNC_DATE=06/02/2005
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	D	051-6839	02
SCALE	NONE	SHT	OF
		82	115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
ENET_CLK25M_TX	CLOCK	CLOCK		
ENET_CLK125M_RX	CLOCK	CLOCK		
ENET_GBE_REF	CLOCK	CLOCK		
ENET_TX_CLK	CLOCK	CLOCK		
ENET_RXD<0>	ENET	ENET		
ENET_RXD<1>	ENET	ENET		
ENET_RXD<2>	ENET	ENET		
ENET_RXD<3>	ENET	ENET		
ENET_RXD<4>	ENET	ENET		
ENET_RXD<5>	ENET	ENET		
ENET_RXD<6>	ENET	ENET		
ENET_RXD<7>	ENET	ENET		
ENET_RX_DV	ENET	ENET		
ENET_RX_ER	ENET	ENET		
ENET_COL	ENET	ENET		
ENET_CR	ENET	ENET		
ENET_MDC	ENET	ENET		
ENET_MDIO	ENET	ENET		

Page Notes

Power aliases required by this page:
 - =PP2V5R3V3_PWRON_I2_ENET

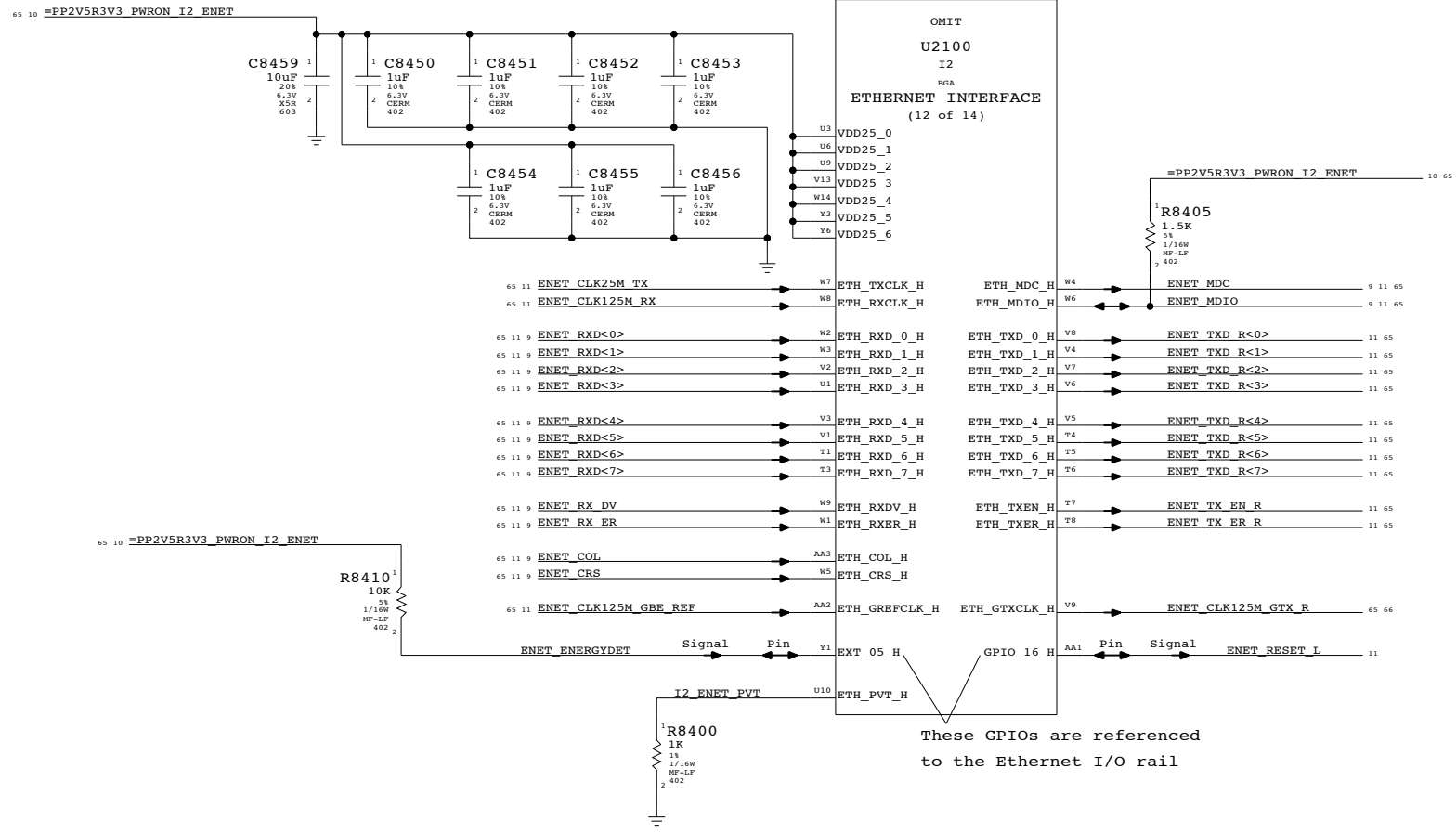
Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

NOTE: This page does not provide any series termination. Any termination, including clock signals, should be provided by the PHY page or a non-shared schematic page.

NOTE: All I2 GPIOs should have a pull-up or pull-down resistor. This page does not provide a resistor for GPIO 16. It must be provided by the PHY page or a non-shared schematic page.

NOTE: ENET_RX_DV has a hold spec violation on I2. May want to lengthen net by ~250ps. Net has a unique ECSet name to allow this.



I2 Ethernet Interface
 SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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	D	051-6839	02
SCALE	SHT	OF	
NONE	84	115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
R24	ENETCONN	ENETCONN	ENET_RJ45_0	ENETRJ45_0_P
R25	ENETCONN	ENETCONN	ENET_RJ45_0	ENETRJ45_0_N
R26	ENETCONN	ENETCONN	ENET_RJ45_1	ENETRJ45_1_P
R27	ENETCONN	ENETCONN	ENET_RJ45_1	ENETRJ45_1_N
R28	ENETCONN	ENETCONN	ENET_RJ45_2	ENETRJ45_2_P
R29	ENETCONN	ENETCONN	ENET_RJ45_2	ENETRJ45_2_N
R30	ENETCONN	ENETCONN	ENET_RJ45_3	ENETRJ45_3_P
R31	ENETCONN	ENETCONN	ENET_RJ45_3	ENETRJ45_3_N

Page Notes

Power aliases required by this page:
 - _PP2V5_ENET
 - _GND_CHASSIS_ENET

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

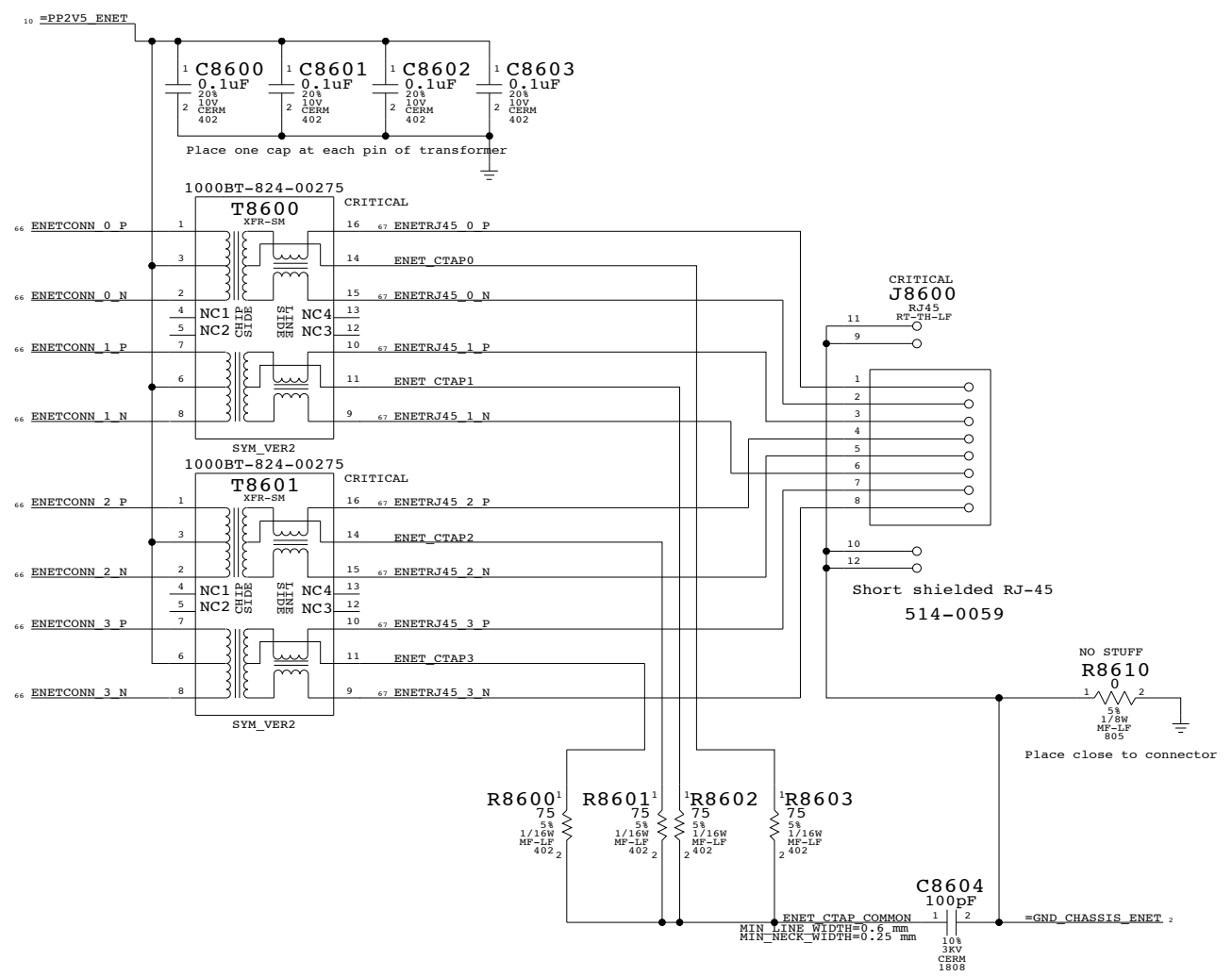
Ethernet routing priority:
 1. Decoupling caps
 2. TX SERIES TERMINATION - LOCATE NEAR LINK
 3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

Transformers should be mirrored on opposite sides of the board



Ethernet Connector

SYNC_MASTER=N/A SYNC_DATE=N/A

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SCALE	SHT	OF	
NONE	86	115	

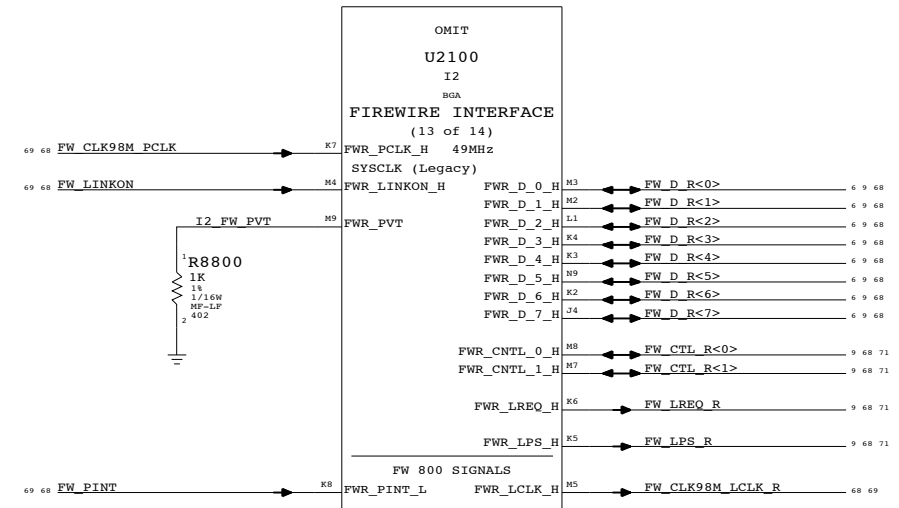
ELECTRICAL_CONSTRAINT_SET	NET_TYPE		DIFFERENTIAL_PAIR		
	SPACING	PHYSICAL			
FW_D_CTL	FW	FW		FW_D_R<7..0>	6 9 68
FW_D_CTL	FW	FW		FW_CTL_R<1..0>	9 68 71
FW_LREQ	FW	FW		FW_LREQ_R	9 68 71
	FW	FW		FW_LPS_R	9 68 71
	FW	FW		FW_LINKON	68 69
FW_CLK	CLOCK	CLOCK		FW_CLK98M_PCLK	68 69
FW_LCLK	CLOCK	CLOCK		FW_CLK98M_LCLK_R	68 69
FW_PINT	FW	FW		FW_PINT	68 69

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



I2 FireWire Interface
 SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005
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	D	051-6839	02
SCALE	SHT OF		
NONE	88 OF		115

ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
PROVIDED BY LINK PAGE	CLOCK	CLOCK	
FW_CLK98M_PCLK_R	CLOCK	CLOCK	
FW_CLK98M_LCLK	CLOCK	CLOCK	
FW_TPA0	FM_TP	FM_TP	FM_TPA0
FW_TPA0_P	FM_TP	FM_TP	FM_TPA0
FW_TPA0_N	FM_TP	FM_TP	FM_TPA0
FW_TP0_P	FM_TP	FM_TP	FM_TP0
FW_TP0_N	FM_TP	FM_TP	FM_TP0
FW_TPA1_P	FM_TP	FM_TP	FM_TPA1
FW_TPA1_N	FM_TP	FM_TP	FM_TPA1
FW_TPB1_P	FM_TP	FM_TP	FM_TPB1
FW_TPB1_N	FM_TP	FM_TP	FM_TPB1
FW_TPA2_P	FM_TP	FM_TP	FM_TPA2
FW_TPA2_N	FM_TP	FM_TP	FM_TPA2
FW_TPB2_P	FM_TP	FM_TP	FM_TPB2
FW_TPB2_N	FM_TP	FM_TP	FM_TPB2
VESTA_CLK24M_XTALI	XTAL	XTAL	
VESTA_CLK24M_XTALO	XTAL	XTAL	
VESTA_CLK24M_XTALO_R	XTAL	XTAL	

Page Notes

Power aliases required by this page:
 - =PPFW_PHY_CPS
 - =PP3V3_FW
 - =PP3V3_ENETFW
 - =PP2V5_ENETFW
 - =PP1V2_ENETFW

Signal aliases required by this page:
 - NONE

BOM options provided by this page:
 - VESTA_BILINGUAL_EN12
 If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.
 - VESTA_DS_ONLY_EN0
 If stuffed, adds external pull-up to counter internal pull-down in Vesta. See straps table for more information.
 - VESTA_PORT1_DISABLE
 If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.
 - VESTA_PORT2_DISABLE
 If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.
 - VESTA_PWR_CLASS_0
 If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.

Net Spacing Type: FW_TP

Line to Line: 0.38 mms
 Length Tolerance: 100 mils
 Primary Max Sep: 7.5 mils
 Secondary Max Sep: 100 mils
 Secondary Length: 500 mils

NOTE: Target differential impedance for FW data pairs is 110 ohms.

Vesta Config Straps:

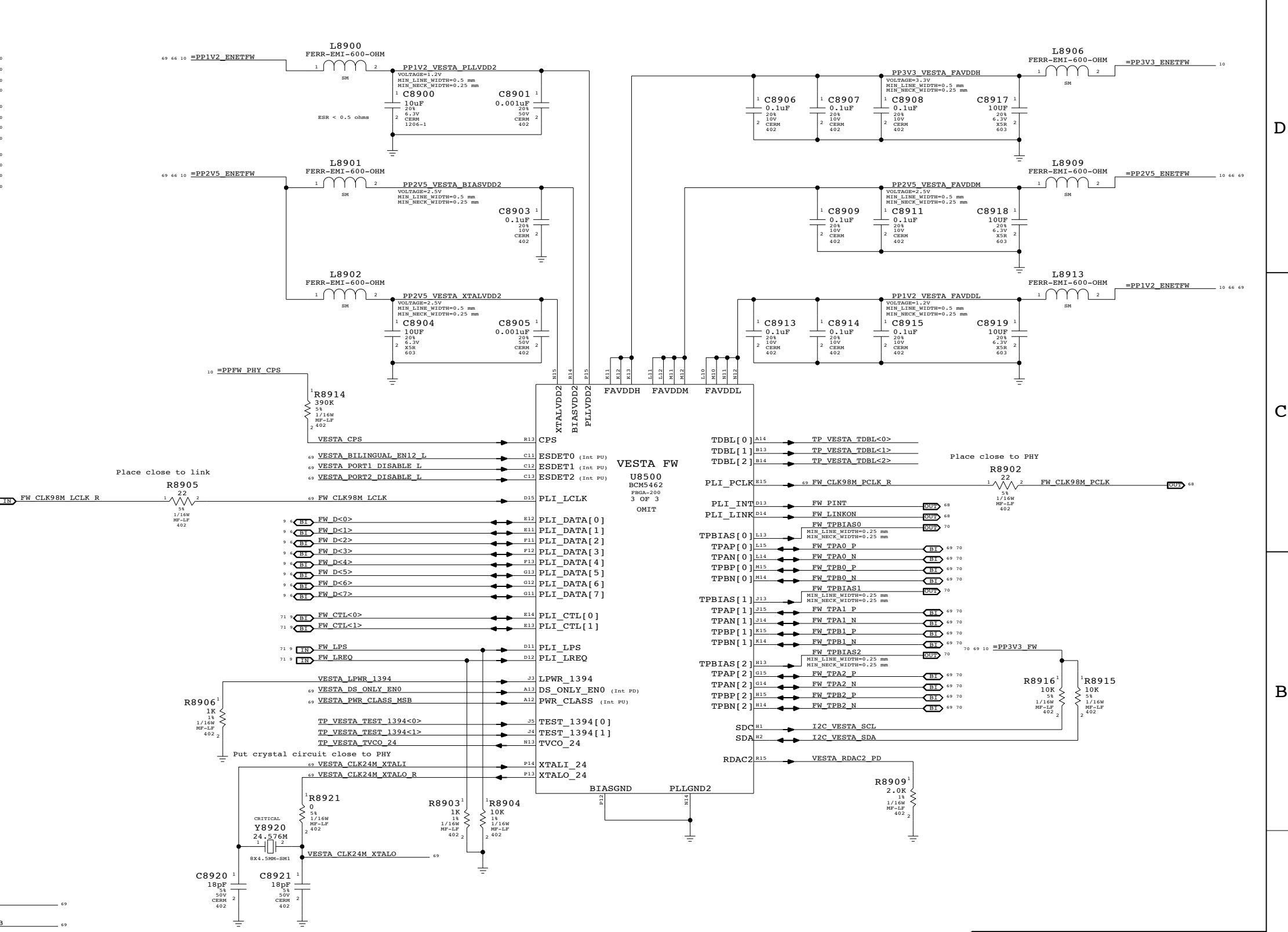
DS_ONLY_EN12 - Port 1&2 Data/Strobe
 1 - Port 1&2 Data/Strobe mode only
 0 - Port 1&2 Bilingual mode
 (Internal Pull-up)

DS_ONLY_EN0 - Port 0 Data/Strobe
 1 - Port 0 Data/Strobe mode only
 0 - Port 0 Bilingual mode
 (Internal Pull-down)

PORT1_ENABLE - Port 1 Enable
 1 - Port 1 Enabled
 0 - Port 1 Disabled (saves power)
 (Internal Pull-up)

PORT2_ENABLE - Port 2 Enable
 1 - Port 2 Enabled
 0 - Port 2 Disabled (saves power)
 (Internal Pull-up)

PWR_CLASS - FireWire Power Class
 1 - Sets Power Class to 0x4
 0 - Sets Power Class to 0x0
 (Internal Pull-up)



Vesta FireWire PHY

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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D	051-6839	02
SCALE	SHT	OF
NONE	89	115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
PROVIDED	FW	FW	FW_PORT1_TPA_P_FL
BY	FW	FW	FW_PORT1_TPA_N_FL
PHY	FW	FW	FW_PORT1_TPB_FL
PAGE	FW	FW	FW_PORT1_TPB_N_FL
	FW	FW	FW_PORT2_TPA_P_FL
	FW	FW	FW_PORT2_TPA_N_FL
	FW	FW	FW_PORT2_TPB_FL
	FW	FW	FW_PORT2_TPB_N_FL

Page Notes

Power aliases required by this page:
 - PPFW_PORT1
 - PPFW_PORT2
 - PPFW_PORT3
 - PP3V3_FW
 - GND_CHASSIS_FW_PORT1
 - GND_CHASSIS_FW_PORT2
 - GND_CHASSIS_FW_PORT3

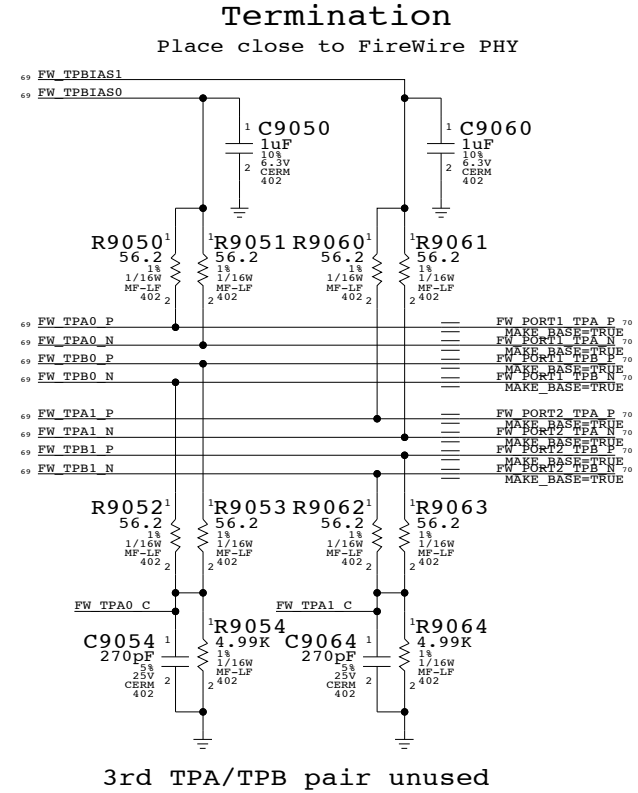
Signal aliases required by this page:
 (NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

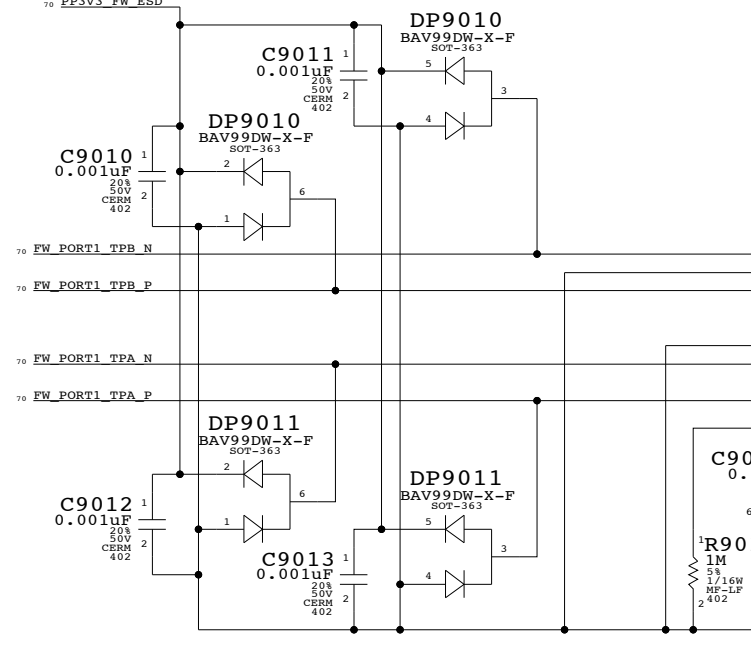
BOM options provided by this page:
 (NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

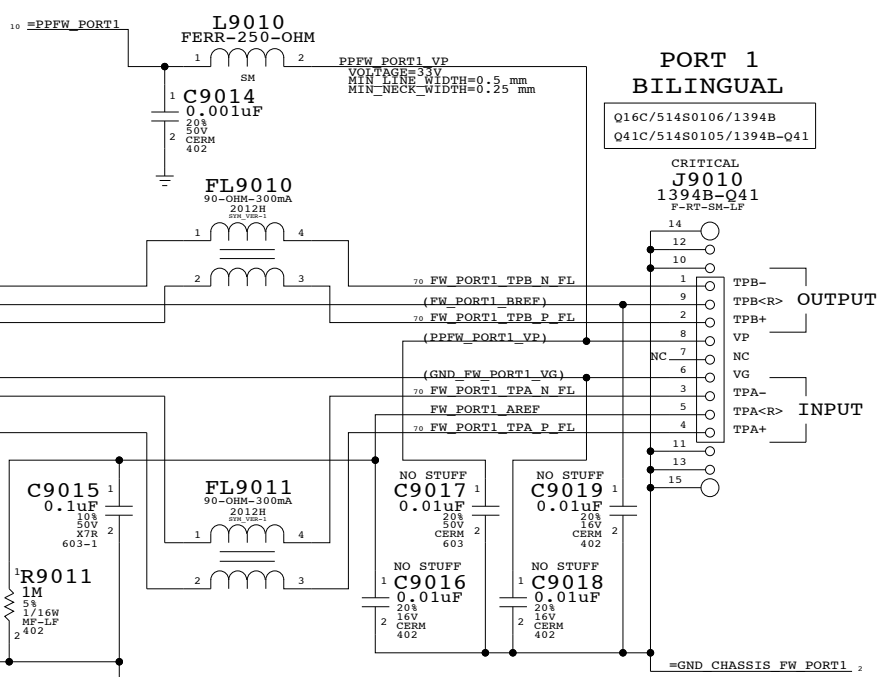
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)



"Snapback" & "Late VG" Protection



Cable Power

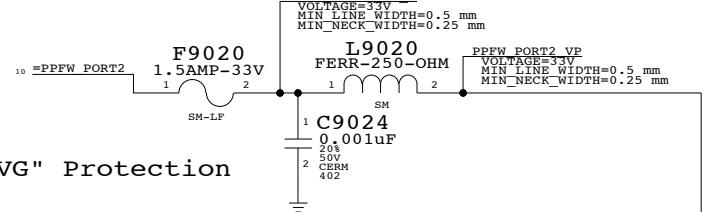


AREF needs to be isolated from all local grounds per 1394b spec

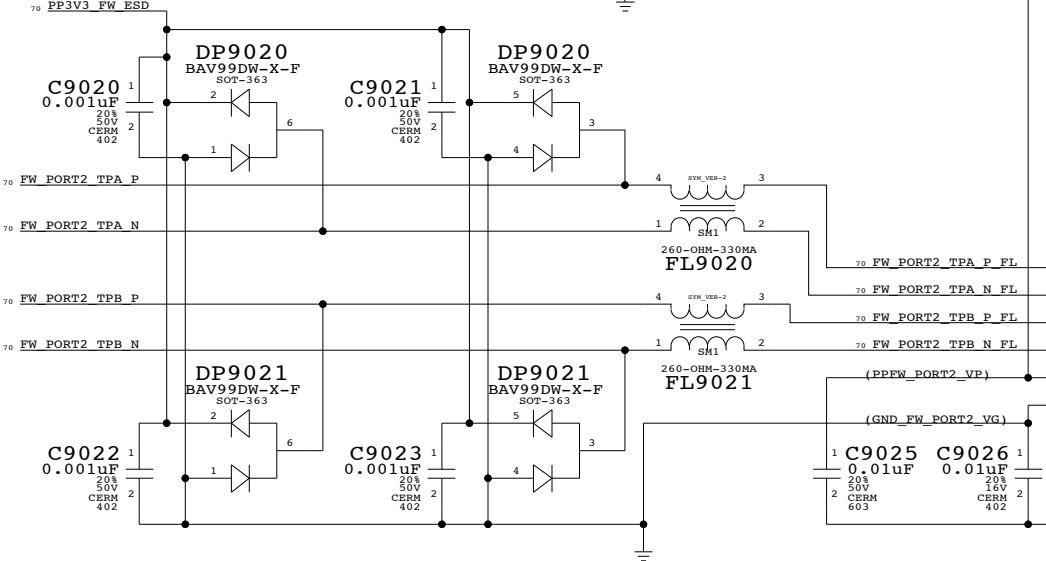
When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

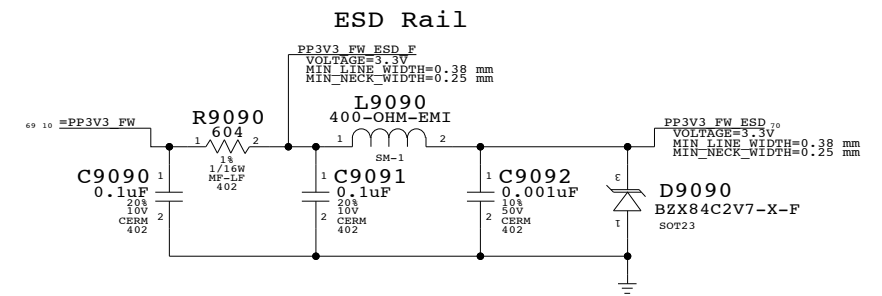
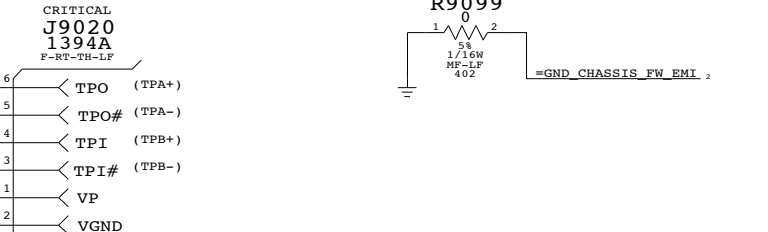
Cable Power



"Snapback" & "Late VG" Protection



PORT 2 1394A



FireWire Ports

SYNC_MASTER=MARIAS-PDIFF SYNC_DATE=06/02/2005

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	SCALE	SHT	OF
NONE		90	115

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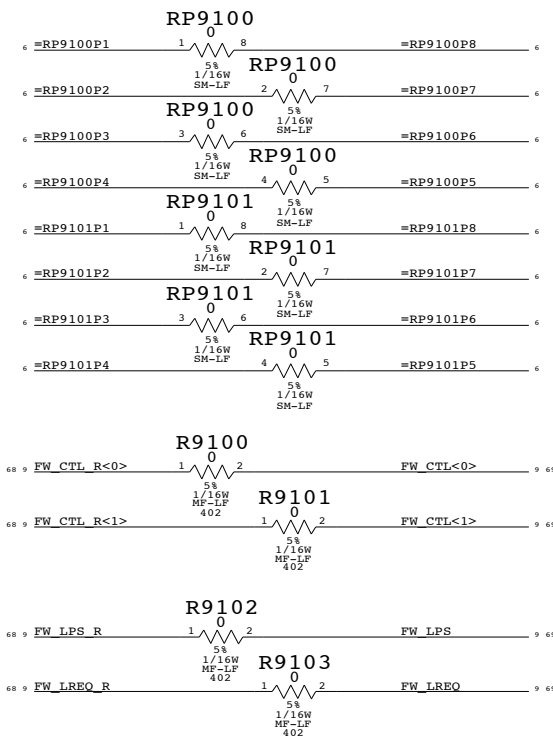
B

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Place series terminators approximately halfway between Vesta and NB.
(They should probably be slightly closer to Vesta than the NB.)



FireWire Series Term

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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SCALE	SHT OF		
NONE	91 OF		115

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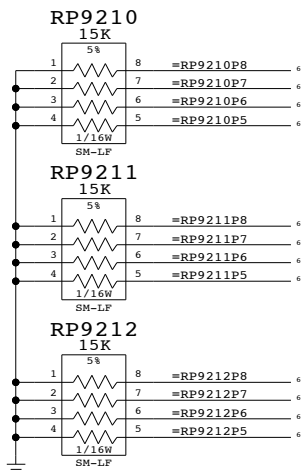
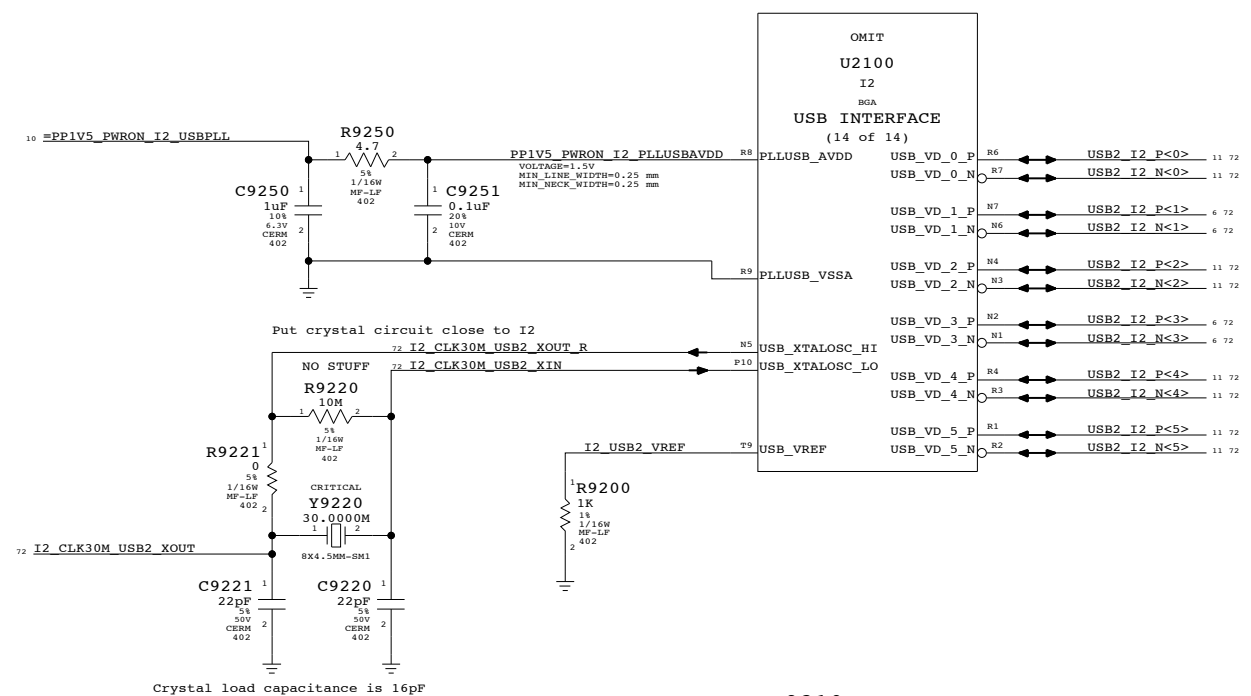
ELECTRICAL_CONSTRAINT_SET	NET_TYPE		DIFFERENTIAL_PAIR		
	SPACING	PHYSICAL			
USB2_0	USB2	USB2	USB2_I2_P<0>	USB2_I2_N<0>	11 72
			USB2_I2_P<0>	USB2_I2_N<0>	11 72
USB2_1	USB2	USB2	USB2_I2_P<1>	USB2_I2_N<1>	6 72
			USB2_I2_P<1>	USB2_I2_N<1>	6 72
USB2_2	USB2	USB2	USB2_I2_P<2>	USB2_I2_N<2>	11 72
			USB2_I2_P<2>	USB2_I2_N<2>	11 72
USB2_3	USB2	USB2	USB2_I2_P<3>	USB2_I2_N<3>	6 72
			USB2_I2_P<3>	USB2_I2_N<3>	6 72
USB2_4	USB2	USB2	USB2_I2_P<4>	USB2_I2_N<4>	11 72
			USB2_I2_P<4>	USB2_I2_N<4>	11 72
USB2_5	USB2	USB2	USB2_I2_P<5>	USB2_I2_N<5>	11 72
			USB2_I2_P<5>	USB2_I2_N<5>	11 72
USB2_I2_XTAL	XTAL	XTAL	I2_CLK30M_USB2_XOUT_R		72
(USB2_I2_XTAL)	XTAL	XTAL	I2_CLK30M_USB2_XOUT		72
(USB2_I2_XTAL)	XTAL	XTAL	I2_CLK30M_USB2_XIN		72

Page Notes

Power aliases required by this page:
 - =PP3V3_PWRON_USB
 Signal aliases required by this page:
 - =RP92xxPy (pinswappable USB pulldowns)
 BOM options provided by this page:
 (NONE)

Net Spacing Type: USB2

Line To Line: 19.5 mils
 Length Tolerance: 50 mils
 Primary Max Sep: 7.5 mils
 Secondary Max Sep: 100 mils
 Secondary Length: 500 mils
 NOTE: Target differential impedance for USB2 data pairs is 90 ohms.



I2 USB Interface
 SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005
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NONE	92	115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
E30	USB2	USB2	USB2_NEC_0
E31	USB2	USB2	USB2_NEC_0
E32	USB2	USB2	USB2_NEC_1
E33	USB2	USB2	USB2_NEC_1
E34	USB2	USB2	USB2_NEC_2
E35	USB2	USB2	USB2_NEC_2
E36	USB2	USB2	USB2_NEC_3
E37	USB2	USB2	USB2_NEC_3

ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
E40	XTAL	XTAL	NEC_CLK30M_XT1
E41	XTAL	XTAL	NEC_CLK30M_XT2
E42	XTAL	XTAL	NEC_CLK30M_XT2_R

Page Notes

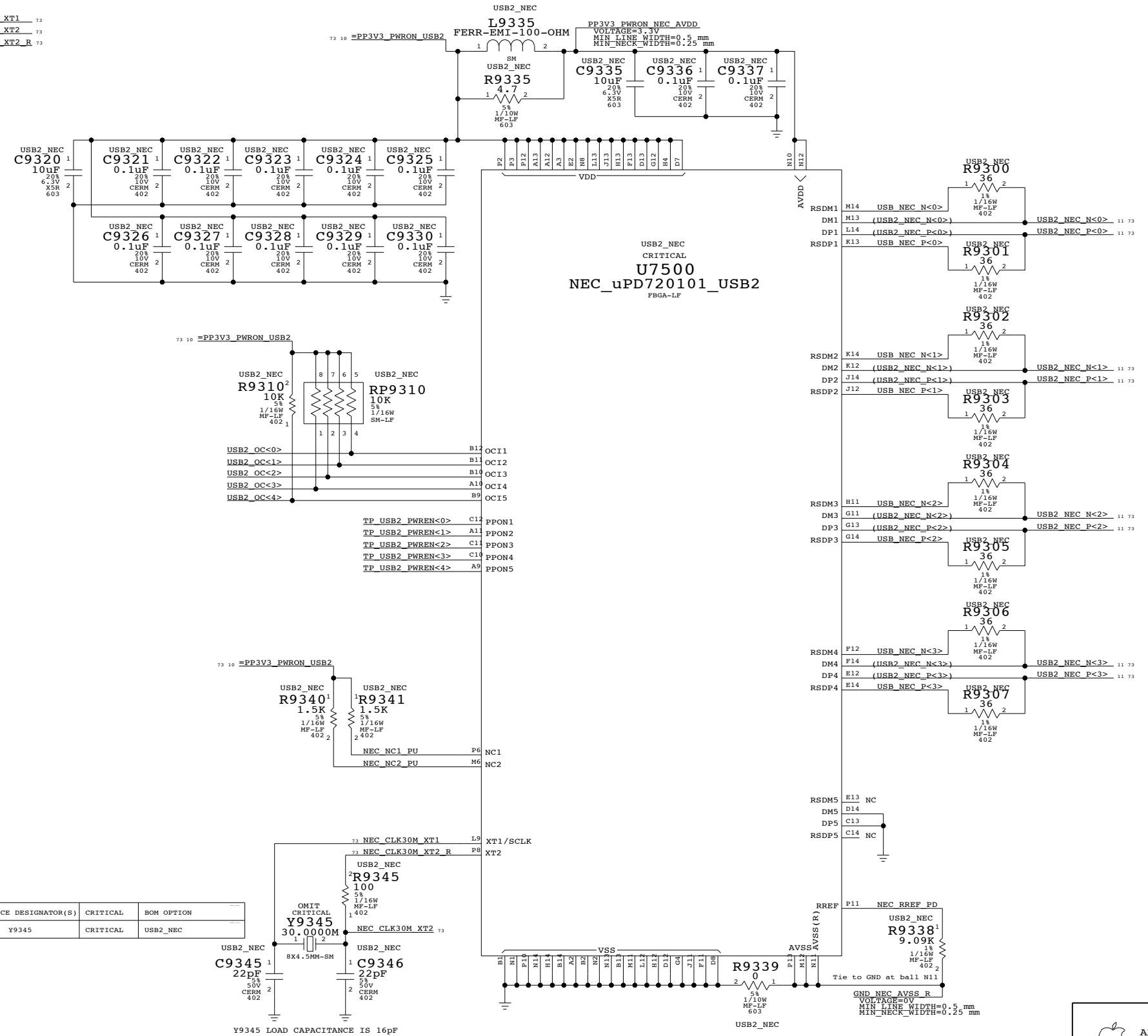
Power aliases required by this page:
 - =PP3V3_PWRON_USB2

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 USB2_NEC

Net Spacing Type: USB2

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
19750087	1	XTAL,CER,10.0000MHZ,LW PROF,8X4.5MM,SMD	Y9345	CRITICAL	USB2_NEC

NEC USB2 Interface

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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SCALE	SHT	OF	
NONE	93	115	

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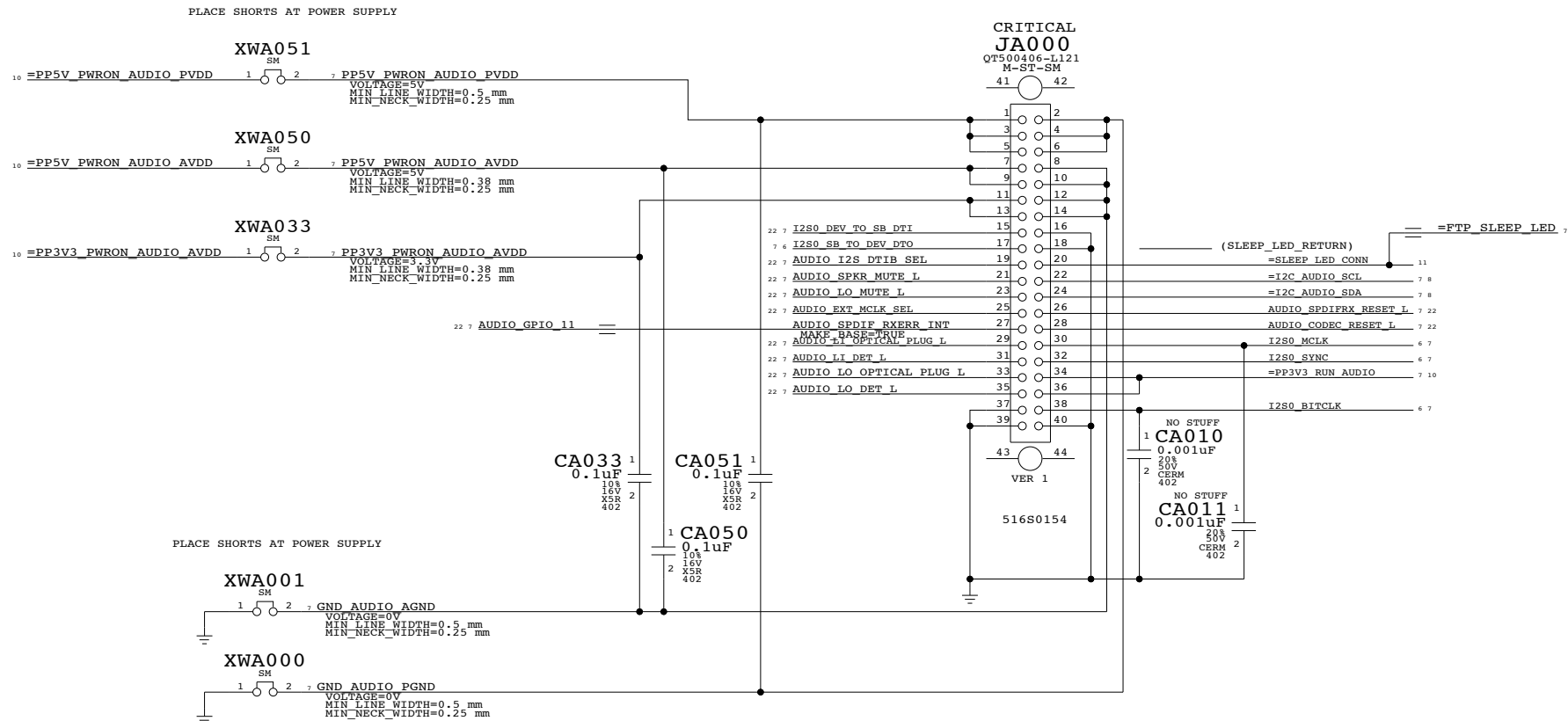
B

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AUDIO BOARD CONNECTOR

Place all shorts at output of 3.3V and 5V regulator



Audio Board Connector

SYNC_MASTER=N/A SYNC_DATE=N/A

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SCALE	SHT OF		
NONE	100		115

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D	AGP TABLE_SPACING_RULE TABLE_SPACING_RULE AGP 401 * 0.4 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_SPACING_RULE AGP_STB 601 * 0.6 MM 2.5 MM =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE AGP * =STANDARD =60_OHM_SE =60_OHM_SE =60_OHM_SE TABLE_PHYSICAL_RULE AGP_STB * =STANDARD =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF					AUDIO TABLE_SPACING_RULE TABLE_SPACING_RULE AUDIO 251 * 0.25 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE AUDIO * =50_OHM_SE =50_OHM_SE =50_OHM_SE =50_OHM_SE																
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	ENET (Ethernet Digital) TABLE_SPACING_RULE TABLE_SPACING_RULE ENET_SELF =STANDARD * =STANDARD =STANDARD =STANDARD =STANDARD =STANDARD TABLE_SPACING_RULE ENET 201 * 0.2 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE ENET * =STANDARD =50_OHM_SE =50_OHM_SE =50_OHM_SE					ENETCONN TABLE_SPACING_RULE TABLE_SPACING_RULE ENETCONN 501 * 0.50 MM 3.81 MM =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE ENETCONN * =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF																
	FW (FireWire Digital) TABLE_SPACING_RULE TABLE_SPACING_RULE FW_SELF =STANDARD * =STANDARD =STANDARD =STANDARD =STANDARD =STANDARD TABLE_SPACING_RULE FW 201 * 0.2 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE FW * =STANDARD =50_OHM_SE =50_OHM_SE =50_OHM_SE					FW_TP TABLE_SPACING_RULE TABLE_SPACING_RULE FW_TP 501 * 0.50 MM 3.81 MM =110_OHM_DIFF =110_OHM_DIFF =110_OHM_DIFF TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE FW_TP * =110_OHM_DIFF =110_OHM_DIFF =110_OHM_DIFF =110_OHM_DIFF																
	C	I2C TABLE_SPACING_RULE TABLE_SPACING_RULE I2C 201 * 0.2 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE I2C * =STANDARD =50_OHM_SE =50_OHM_SE =50_OHM_SE					I2_FBCLK / XTAL TABLE_SPACING_ASSIGNMENT TABLE_SPACING_ASSIGNMENT I2_FBCLK * * CLOCK TABLE_SPACING_ASSIGNMENT XTAL * * CLOCK TABLE_PHYSICAL_ASSIGNMENT TABLE_PHYSICAL_ASSIGNMENT I2_FBCLK * CLOCK TABLE_PHYSICAL_ASSIGNMENT XTAL * CLOCK															
		MaxBus TABLE_SPACING_RULE TABLE_SPACING_RULE MAXBUS 151 * 0.15 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE MAXBUS * =STANDARD =50_OHM_SE =50_OHM_SE =50_OHM_SE																				
		PCI TABLE_SPACING_RULE TABLE_SPACING_RULE PCI =STANDARD * =STANDARD =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE PCI * =STANDARD =50_OHM_SE =50_OHM_SE =50_OHM_SE																				
		RAM TABLE_SPACING_RULE TABLE_SPACING_RULE RAM 201 * 0.2 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_SPACING_RULE RAM_DIFF 251 * 0.25 MM 2.5 MM =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE RAM * =50_OHM_SE =50_OHM_SE =50_OHM_SE =50_OHM_SE TABLE_PHYSICAL_RULE RAM_DIFF * =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF																				
		UATA TABLE_SPACING_RULE TABLE_SPACING_RULE UATA 151 * 0.15 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE UATA * =50_OHM_SE =50_OHM_SE =50_OHM_SE =50_OHM_SE																				
		A	USB2 TABLE_SPACING_RULE TABLE_SPACING_RULE USB2 501 * 0.50 MM 3.81 MM =90_OHM_DIFF =90_OHM_DIFF =90_OHM_DIFF TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE USB2 * =90_OHM_DIFF =90_OHM_DIFF =90_OHM_DIFF =90_OHM_DIFF					Spacing & Physical Constraints SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005 NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART														
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TABLE_SPACING_RULE								
TABLE_SPACING_RULE	DVO	151	*	0.15 MM	=STANDARD	=STANDARD	=STANDARD	=STANDARD
TABLE_PHYSICAL_RULE	DVO							DVO
TABLE_PHYSICAL_RULE	DVO	*		=STANDARD	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	
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TABLE_SPACING_RULE	TV_CONN	151	*	=TV	=TV	=TV	=TV	=TV
TABLE_PHYSICAL_RULE	TV							S-VIDEO
TABLE_PHYSICAL_RULE	TV_CONN	*		=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	
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TABLE_SPACING_RULE								
TABLE_SPACING_RULE	VGA	151	*	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE
TABLE_SPACING_RULE	VGA_CONN	151	*	=VGA	=VGA	=VGA	=VGA	=VGA
TABLE_PHYSICAL_RULE	VGA							VGA
TABLE_PHYSICAL_RULE	VGA_CONN	*		=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	
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Spacing & Physical Constraints 2

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