1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

DRAWING REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
02		248015	ENGINEERING RELEASED	12/05/02?	

SCHEM,COOPER,Q16A

Fri Dec 26 17:52:43 2003

BOM OPTIONS (IN COMMON PARTS)

STUFF	NO STUFF
1_8V_MAXBUS	1_5V_MAXBUS
SSCG	NO_SSCG
5V_HD_LOGIC	3V_HD_LOGIC
NO_BBANG	BBANG
INT_2_5V_COLD	INT_2_5V_HOT
ATI_MEMIO_HI	ATI_MEMIO_LO
SOFT_MODEM	USB_MODEM
GPU_PWRMSR	EXT_TMDS
GPU_SS	
VGA_BUFFER_RES	
INT_TMDS	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6570	1	SCHEM,COOPER,Q16A	SCH1	
820-1600	1	PCBF,COOPER,Q16A	PCB1	
065-4818	1	CMNPRTS,MLB,Q16A	DMS1	DMS630-4968&DMS630-4969&DMS630-6310
065-4816	1	SELPRTS,MLB,Q16A,BTR	DMS2	DMS630-4968
065-4817	1	SELPRTS,MLB,Q16A,BST	DMS3	DMS630-4969
065-4958	1	SELPRTS,MLB,Q16A,BST128	DMS4	DMS630-6310

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

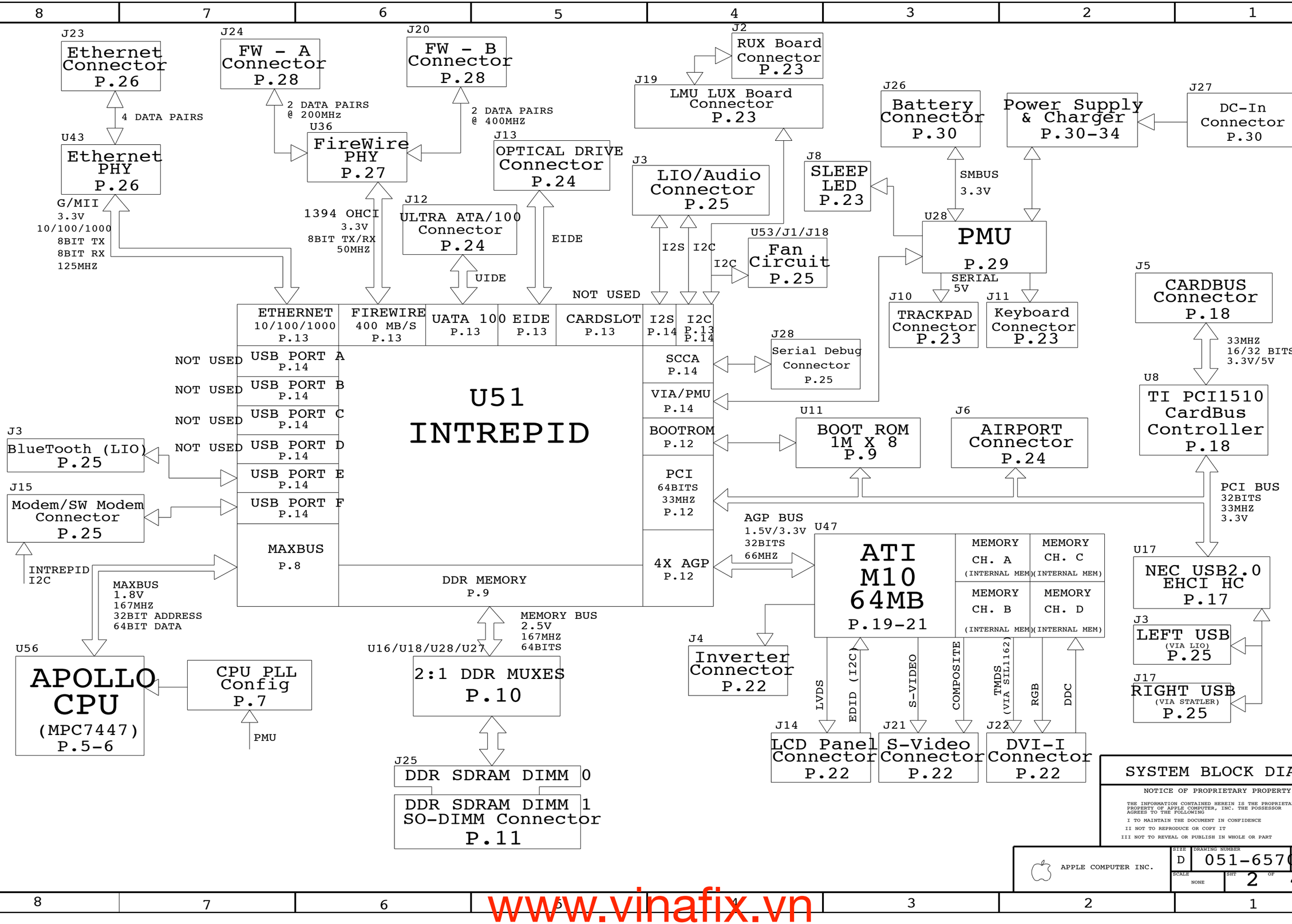
SIZE D

Apple Computer Inc.

TITLE: SCHEM,COOPER,Q16A

DRAWING NUMBER 051-6570 REV. 01

SHT 1 OF 44



POWER SYSTEM ARCHITECTURE

AC ADAPTER IN PG 30

INRUSH LIMITER PG 30

+24V_PBUS

1V20_REF
>~13.44V TURNS-ON
<~13.44V SHUTS-OFF
PG 31

RUN/SS
BUCK REGULATOR (LTC1625) PG 31
VCC
AC: 12.8V
NO AC: BATTERY VOLTAGE 1625 NOT RUNNING
SHUTDOWN: RUNNING
SLEEP: RUNNING
RUN: RUNNING

+PBUS

14V_PBUS

+3V_PMU LDO PG 31

+5V_MAIN
+3V_PMU
+4_6V_BU

+BATT

RC AT 1M*0.047UF @ 24V
STARTS 2.0MSEC AFTER DCDC_EN_L BECOMES LOW

RUN/SS - 5V
TURNS ON AT >1V
<100UA ALLOWED
INTERNAL ZENER CLAMP TO 6V

MAIN 3V/5V DC/DC (LTC3707) PG 32
VCC
PGOOD
STBYMD
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING

INTERNAL ZENER CLAMP TO 6V
<100UA ALLOWED
TURNS ON AT >1V
RUN/SS - 3V

+5V_MAIN
3V_5V_OK
HOLDS BOTH RUN/SS AT GND WHEN IT'S CONNECTED TO GND
TURNS CONTROL TO RUN/SS WHEN IT'S OPEN
+3.3V_MAIN

RC AT 1M*0.1UF @ 24V
STARTS ~4.25MSEC AFTER DCDC_EN_L BECOMES LOW

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

+24V_PBUS

DC/DC (LTC3411)
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING
PG 34

+1.8V_MAIN
MAXBUS

BACKUP BATTERY

14V_PBUS
14V CHARGES BACKUP BATTERY

24V IS OUTPUT ONLY FROM BACKUP BATTERY

CHARGER INPUT & BOOST OUTPUT PG 31

BACKUP BATTERY CIRCUIT CHARGES OFF +PBUS
AND PREVENTS +PBUS AND +24V_PBUS FROM DROPPING BELOW 6V
(UNTIL DRAINED)

BATTERY CHARGER (MAX1772) PG 30

+BATT

3S 2P 18650 CELLS

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

BATTERY VOLTAGE FEED-IN PATH PG 30

+PBUS

BACKLIGHT INVERTER

+5V_MAIN

VCC
MAIN 2.5V/1.5V DC/DC (MAX1715) PG 34
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING
TURNS ON OUTPUT @ 2.4V ON1/ON2

MAP31 DDR CORE
MAP31 DDR I/O
DDR POWER
+2.5V_MAIN

PGOOD
1_5V_2_5V_OK

+1.5V_MAIN
INTREPID CORE
AGP I/O

+5V_MAIN

DCDC_EN_L

AFTER PMU IS UP AND RUNNING
DCDC_EN_L WILL PULL ON1/ON2
LOW IN SHUTDOWN

+PBUS

+5V_MAIN

EXT_VCC
VCC
DC/DC (LTC1778)
SHUTDOWN: STOPPED
SLEEP: D3COLD
RUN: RUNNING
TURNS ON AS LOW AS 0.8V/TYP 1.5V
INTERNAL 1.2UA CURRENT SOURCE
RUN/SS PG 20

GPU_VCORE +1.2V

DCDC_EN
SLEEP
D3_COLD
GPU_VCORE SEQUENCING

1M & 0.1UF @14V, IT TAKES ~5.88MS TO START SWITCHER

1_5V_2_5V_OK
D3_HOT

1_5V_2_5V_OK WILL NOT PULL LOW UNTIL +5V_MAIN TURNS ON
HOWEVER, 5V SHOULD TURN ON ~2.23MS AFTER DCDC_EN_L OR PMU_POWERUP_L BECOMES '1'; MUCH LESS THAN THE RC CHARGING AT INT_VCC (5V)

DCDC_EN_L
D3_HOT

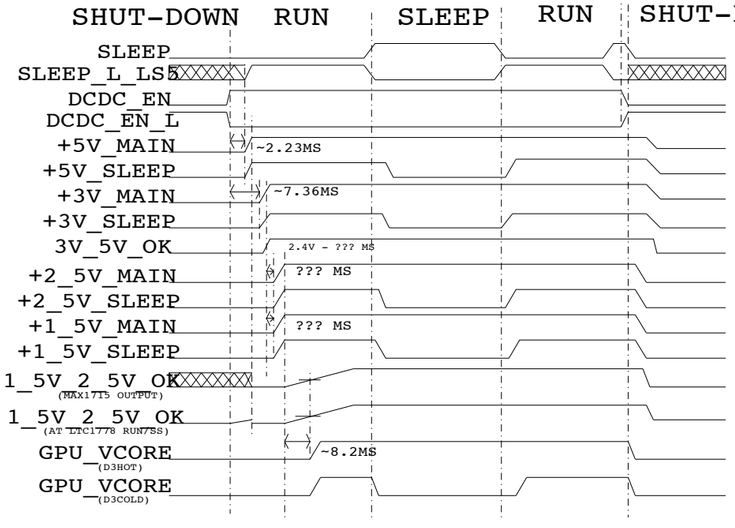
DCDC_EN
SLEEP
MAXBUS SEQUENCING

+PBUS

+5V_MAIN

VCC
SHDN
DC/DC (MAX1717)
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING
PG 33

CPU_VCORE (+1.385V)



POWER BLOCK DIAGRAM

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6570 | REV. 01

SCALE NONE | SHT 3 OF 44

PCB SPECS

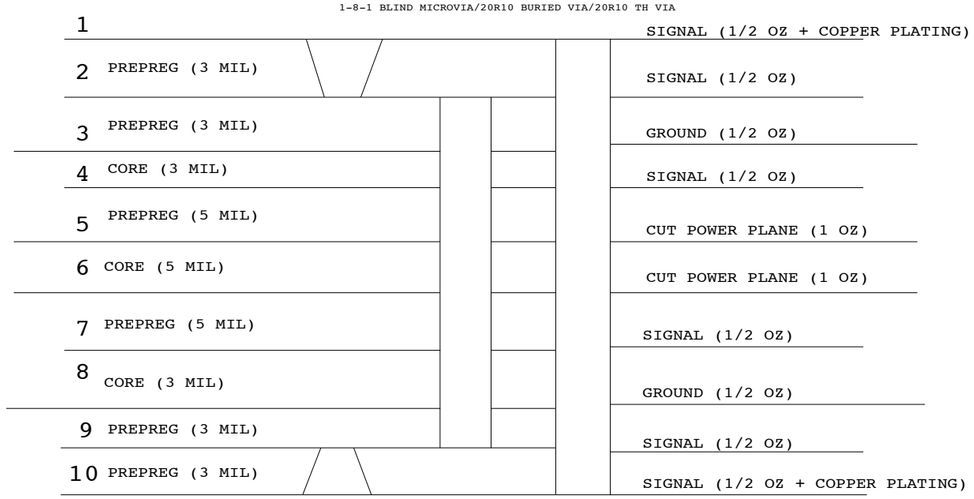
THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 10
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

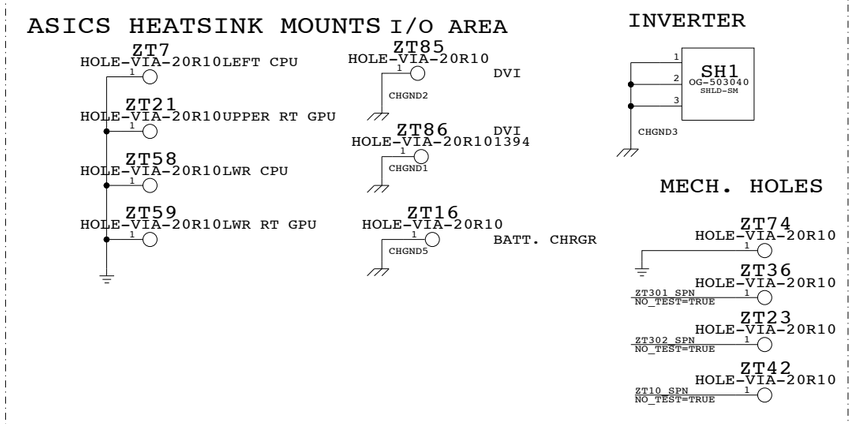
BOARD STACK-UP AND CONSTRUCTION

1-8-1 BLIND MICROVIA/20R10 BURIED VIA/20R10 TH VIA

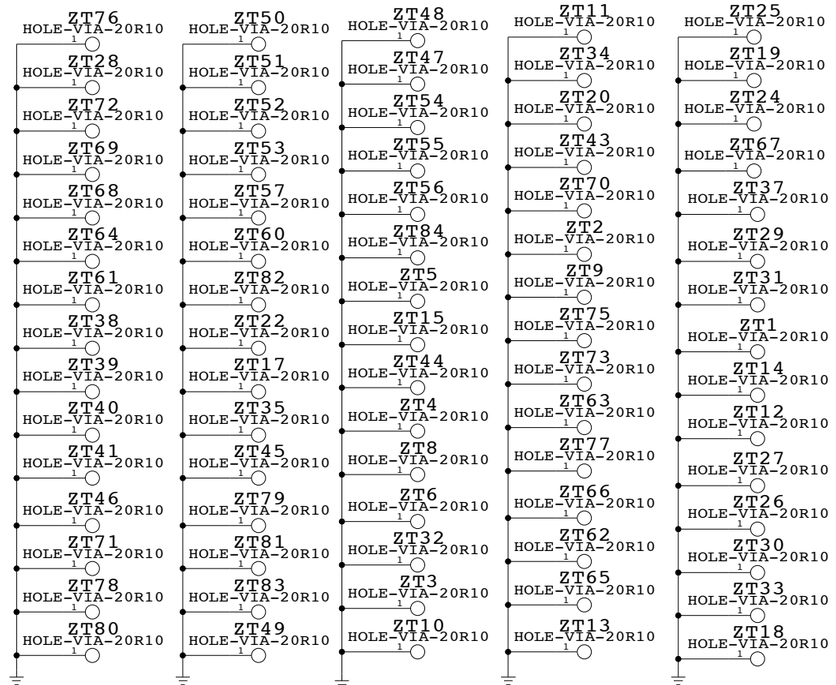


BOARD HOLES

CHASSIS MOUNTS



GROUND VIAS



BOARD INFORMATION

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	01
SCALE: NONE	SHT 4 OF 44	

CPU_VCORE DECOUPLING NETWORK

CPU_VCORE_SLEEP 5 6 33 38 39

R38 470 5% 1/16W MF 402

C32 10uF 20% 6.3V CERM 805 · C59 10uF 20% 6.3V CERM 805 · C104 10uF 20% 6.3V CERM 805

C33 10uF 20% 6.3V CERM 805 · C58 10uF 20% 6.3V CERM 805 · C107 0.1uF 20% 10V CERM 402

C34 2.2uF 20% 10V CERM 805 · C62 2.2uF 20% 10V CERM 805 · C109 0.1uF 20% 10V CERM 402

C26 0.1uF · C39 0.1uF · C50 0.1uF · C45 0.1uF · C29 0.1uF · C55 0.1uF · C2 0.1uF · C108 0.1uF

C30 0.1uF · C49 0.1uF · C31 0.1uF · C47 0.1uF · C27 0.1uF · C53 0.1uF · C103 0.1uF · C110 0.1uF

C28 0.1uF · C48 0.1uF · C56 0.1uF · C46 0.1uF · C25 0.1uF · C54 0.1uF · C68 0.1uF · C1 0.1uF

(all 20% 10V CERM 402)

MORE 0805 10UF CAPS ON VCORE POWER SUPPLY PAGE (PG 32)

OMIT
XW34
SM
25 ADT7460_VCORE_MON 1 2

CPU_OVDD DECOUPLING NETWORK

MAXBUS_SLEEP 5 6 7 8 15 16 33 38

R89 470 5% 1/16W MF 402

C38 0.1uF · C88 0.1uF · C44 0.1uF · C20 0.1uF · C87 0.1uF · C61 0.1uF

C18 0.1uF · C89 0.1uF · C72 0.1uF · C10 0.1uF · C69 0.1uF · C81 0.1uF

C86 0.1uF · C9 0.1uF · C75 0.1uF · C73 0.1uF · C17 0.1uF · C82 0.1uF

(all 20% 10V CERM 402)

VDD · OVDD · AVDD · OVDDSENSE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S2855	1	IC,APOLLO7 PM,R1.0,1.50GHZ,1.30V CORE U56		CRITICAL	CPU_BST
337S2856	1	IC,APOLLO7 PM,R1.0,1.33GHZ,1.23V CORE U56		CRITICAL	CPU_BTR

OMIT
U56
1.XXGHZ
APOLLO7-1.XXV
BGA
(1 OF 3)

CPU_BR_L (36)	D2	BR*
CPU_BG_L (36)	M1	BG*
NC		
CPU_TS_L (36)	L4	TS*
CPU_PULLDOWN (5)	E11	A0
	H1	A1
	C11	A2
	G3	A3
CPU_ADDR<0> (36)	F10	A4
CPU_ADDR<1> (36)	L2	A5
CPU_ADDR<2> (36)	D11	A6
CPU_ADDR<3> (36)	D1	A7
CPU_ADDR<4> (36)	C10	A8
CPU_ADDR<5> (36)	G2	A9
CPU_ADDR<6> (36)	D12	A10
CPU_ADDR<7> (36)	L3	A11
CPU_ADDR<8> (36)	G4	A12
CPU_ADDR<9> (36)	T2	A13
CPU_ADDR<10> (36)	F4	A14
CPU_ADDR<11> (36)	V1	A15
CPU_ADDR<12> (36)	J4	A16
CPU_ADDR<13> (36)	R2	A17
CPU_ADDR<14> (36)	K5	A18
CPU_ADDR<15> (36)	W2	A19
CPU_ADDR<16> (36)	J2	A20
CPU_ADDR<17> (36)	K4	A21
CPU_ADDR<18> (36)	N4	A22
CPU_ADDR<19> (36)	J3	A23
CPU_ADDR<20> (36)	M5	A24
CPU_ADDR<21> (36)	P5	A25
CPU_ADDR<22> (36)	N3	A26
CPU_ADDR<23> (36)	T1	A27
CPU_ADDR<24> (36)	V2	A28
CPU_ADDR<25> (36)	U1	A29
CPU_ADDR<26> (36)	N5	A30
CPU_ADDR<27> (36)	W1	A31
CPU_ADDR<28> (36)	B12	A32
CPU_ADDR<29> (36)	C4	A33
CPU_ADDR<30> (36)	G10	A34
CPU_ADDR<31> (36)	B11	A35
NC	C1	AP0
NC	E3	AP1
NC	H6	AP2
NC	F5	AP3
NC	G7	AP4
CPU_TT<0> (36)	E5	TT0
CPU_TT<1> (36)	E6	TT1
CPU_TT<2> (36)	F6	TT2
CPU_TT<3> (36)	E9	TT3
CPU_TT<4> (36)	C5	TT4
CPU_TBST_L (36)	F11	TBST*
CPU_TSIZ<0> (36)	G6	TSIZ0
CPU_TSIZ<1> (36)	F7	TSIZ1
CPU_TSIZ<2> (36)	E7	TSIZ2
CPU_GBL_L (36)	E2	GBL*
CPU_WT_L (36)	D3	WT*
CPU_CI_L (36)	J1	CI*
CPU_AACK_L (36)	R1	AACK*
CPU_ARTRY_L (36)	N2	ARTRY*
CPU_SHD0_L (5)	E4	SHD0*
CPU_SHD1_L (5)	H5	SHD1*
CPU_HIT_L (36)	B2	HIT*

BVSEL	B7	CPU_BUS_VSEL (7)
SYSCLK	A10	SYSCLK_CPU (8 35)
CLK_OUT	H2	CPU_CLKOUT_SPN — NO_TEST=TRUE
PLL_CFG0	B8	CPU_PLL_CFG<0> (7)
PLL_CFG1	C8	CPU_PLL_CFG<1> (7)
PLL_CFG2	C7	CPU_PLL_CFG<2> (7)
PLL_CFG3	D7	CPU_PLL_CFG<3> (7)
PLL_CFG4	A7	CPU_PLL_CFG<4> (7)
DBG*	M2	CPU_DBG_L (8 36)
DRDY*	R3	CPU_DRDY_L (8 36)
DTI0	G1	CPU_EDTI (5)
DTI1	K1	CPU_DTI<0> (8 36)
DTI2	P1	CPU_DTI<1> (8 36)
DTI3	N1	CPU_DTI<2> (8 36)
TDI	B9	JTAG_CPU_TDI (5 6 39)
TDO	A4	JTAG_CPU_TDO_TP (39)
TMS	F1	JTAG_CPU_TMS (5 6 39)
TCK	C6	JTAG_CPU_TCK (5 6 39)
TRST*	A5	JTAG_CPU_TRST_L (5 6 39)
LSSD_MODE*	E8	CPU_LSSD_MODE (5)
L1_TSTCLK	G8	CPU_L1TSTCLK (5)
L2_TSTCLK	B3	CPU_L2TSTCLK (5)
TA*	K6	CPU_TA_L (8 36)
TEA*	L1	CPU_TEA_L (8 36)
TBEN	E1	CPU_TBEN (5 8)
QREQ*	P4	CPU_QREQ_L (8 36)
QACK*	G5	CPU_QACK_L (8 36)
CKSTP_IN*	A3	
CKSTP_OUT*	B1	CPU_CHKSTP_OUT_L (5 39)
INT*	D4	MPIC_CPU_INT_L (5 14)
SMI*	F9	CPU_SMI_L (5 29)
MCP*	C9	CPU_MCP_L (5)
SRESET*	A2	CPU_SRESET_L (5 39)
HRESET*	D8	CPU_HRESET_L (5 6 7 39)
PMON_IN*	D9	CPU_PMONIN_L (5)
PMON_OUT*	A9	NC
BMODE0*	G9	CPU_EMODE0_L (7)
BMODE1*	F8	CPU_EMODE1_L (5)
EXT_QUAL	A11	CPU_PULLDOWN (5)
CHKS*	A12	CPU_CHKS_L (5)
SRW0*	B10	
SRW1*	E10	CPU_SRWX_L (5)
IARTRY0*	B6	CPU_PULLUP (5)
DX*	D10	CPU_PULLDOWN (5)

GND

CPU INTERNAL PLL FILTERING

For CPU DFS mode, Must stuff R748
NO STUFF

36 CPU_AVDD

R453 10 1% 1/16W MF 402 — 2 1 CPU_VCORE_SLEEP (5 6 33 38 39)

R748 10 1% 1/16W MF 402 — 2 1 38 CPU_AVDD_VOUT

C810 0.1uF 20% 10V CERM 402 · C811 2.2uF 20% 10V CERM 805

+3V_SLEEP

Vout=0.59*(1+R1/R2)
Place R449 & R452 close to U5 pin 6&5

R302 0 5% 1/10W MF 603 — 38 CPU_AVDD_VIN

U5 FAN2558 SOT23-6
1 VIN · 4 PG · 3 EN · 6 VOUT · 5 ADJ · 2 GND

C626 0.001uF 10% 50V CERM 402

R449 121K 1% 1/16W MF 402 — CPU_BST

R452 100K 1% 1/16W MF 402 — CPU_AVDD_ADJ

C102 1uF 10% 6.3V CERM 402

CPU_AVDD_SHDN_L

D17 SH MBR0530

C85 2.2uF 10% 6.3V CERM1 603

R455 100K 5% 1/16W MF 402

C502 0.1uF 20% 10V CERM 402

33 VCORE_SHDN_L

R755 0 5% 1/16W MF 402 — 470OHM FOR BOOT BANGER (39 6 5 JTAG_CPU_TMS)

VCORE_SHDN_L_3V

NO STUFF R775 200K 5% 1/16W MF 402 — 470OHM FOR BOOT BANGER (39 6 5 JTAG_CPU_TDI)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S1105	1	RES,110k ohm	(R1) R449		CPU_BTR

MPC7447 PULL-UPS

+1_5V_SLEEP — 1_5V_MAXBUS — R281 0 5% 1/16W MF 603

+1_8V_SLEEP — 1_8V_MAXBUS — R283 0 5% 1/16W MF 603

38 33 16 15 8 7 6 5 MAXBUS_SLEEP

CPU_TBEN (5 8)	R24 10K	
CPU_CHKS_L (5)	R4 10K	
CPU_SHD0_L (5)	R25 10K	
CPU_SHD1_L (5)	R46 10K	
CPU_MCP_L (5)	R13 10K	
CPU_LSSD_MODE (5)	R26 10K	
CPU_L2TSTCLK (5)	R8 10K	
CPU_CHKSTP_OUT_L (39 5)	R7 1K	
CPU_SRWX_L (5)	R28 10K	
CPU_PMONIN_L (5)	R27 10K	
CPU_EMODE1_L (5)	R33 10K	
CPU_PULLUP (5)	R3 1K	
CPU_HRESET_L (39 7 6 5)	R20 10K	
CPU_SMI_L (29 5)	R34 10K	
JTAG_CPU_TMS (39 6 5)	R32 470	
JTAG_CPU_TDI (39 6 5)	R2 470	
MPIC_CPU_INT_L (14 5)	R19 10K	
CPU_SRESET_L (39 5)	R6 10K	

All: 5% 1/16W MF 402

CPU_L1TSTCLK (5)	R37 10K	
CPU_EDTI (5)	R36 10K	
JTAG_CPU_TCK (39 6 5)	R11 10K	
CPU_PULLDOWN (5)	R45 470	

All: 5% 1/16W MF 402

MAXBUS_SLEEP (5 6 7 8 15 16 33 38)

BBANG

4700HM FOR BOOT BANGER

R9 470 5% 1/16W MF 402

JTAG_CPU_TRST_L (39 6 5)

NO_BBANG

R10 200 5% 1/16W MF 402

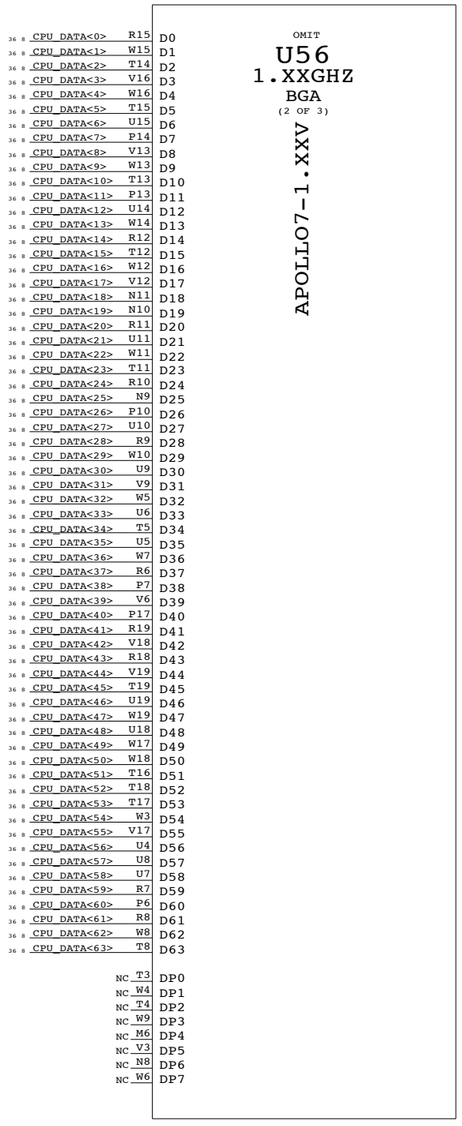
MPC7447 MAXBUS

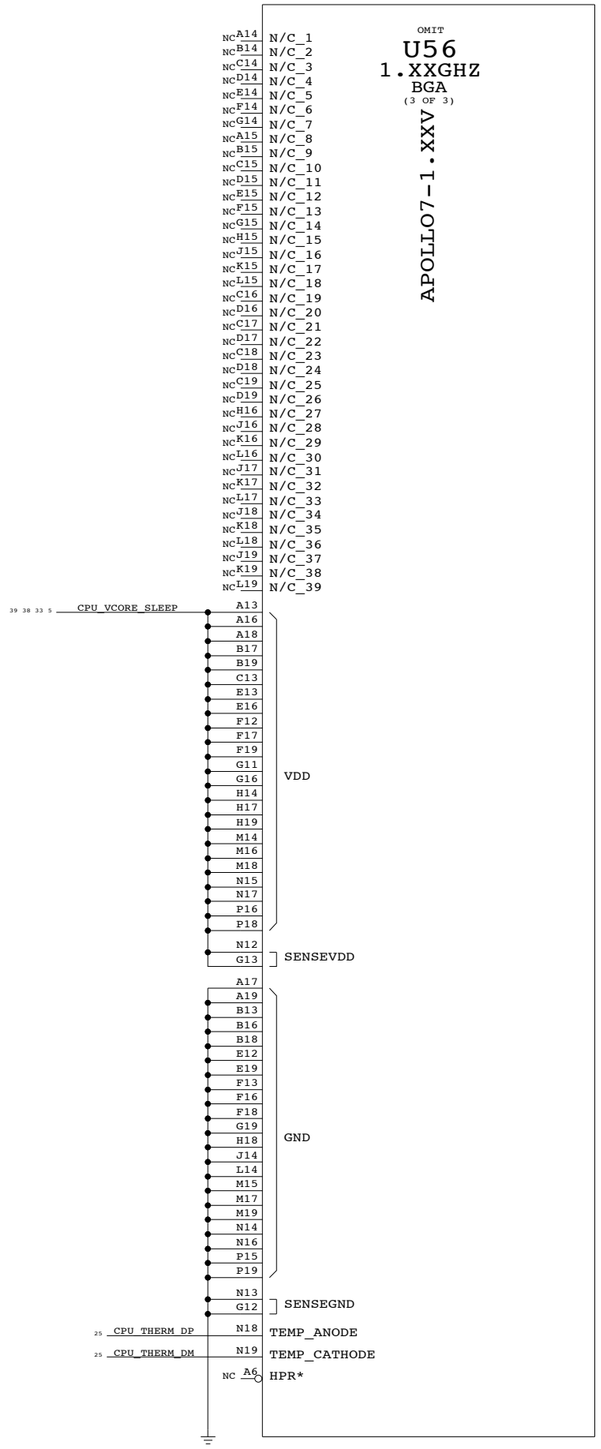
APPLE COMPUTER INC.

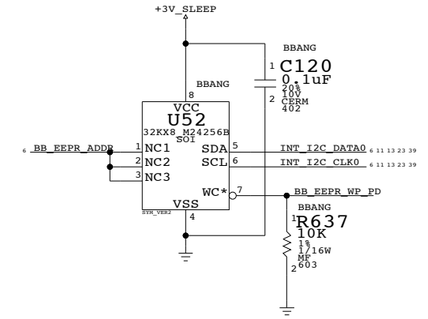
SIZE D · DRAWING NUMBER 051-6570 · REV: 01

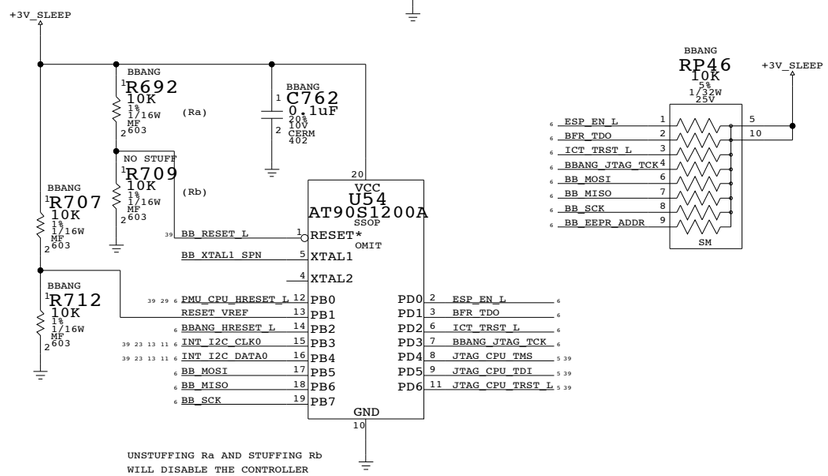
SCALE NONE · SHT 5 OF 44

BOOT BANGER - TWEAK PROCESSOR BITS AFTER POWER-ON



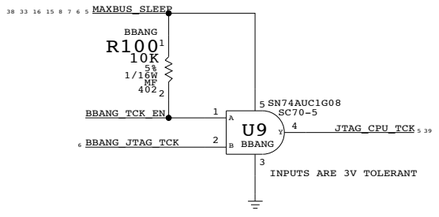


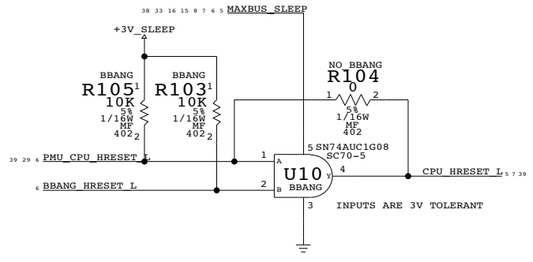




UNSTUFFING Ra AND STUFFING Rb
WILL DISABLE THE CONTROLLER

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1135	1	000-6240-TW-GT4_BBANGER MCU,PROGRAMMED W/ BBANGER	U54	BBANG





MPC7447/BBANG

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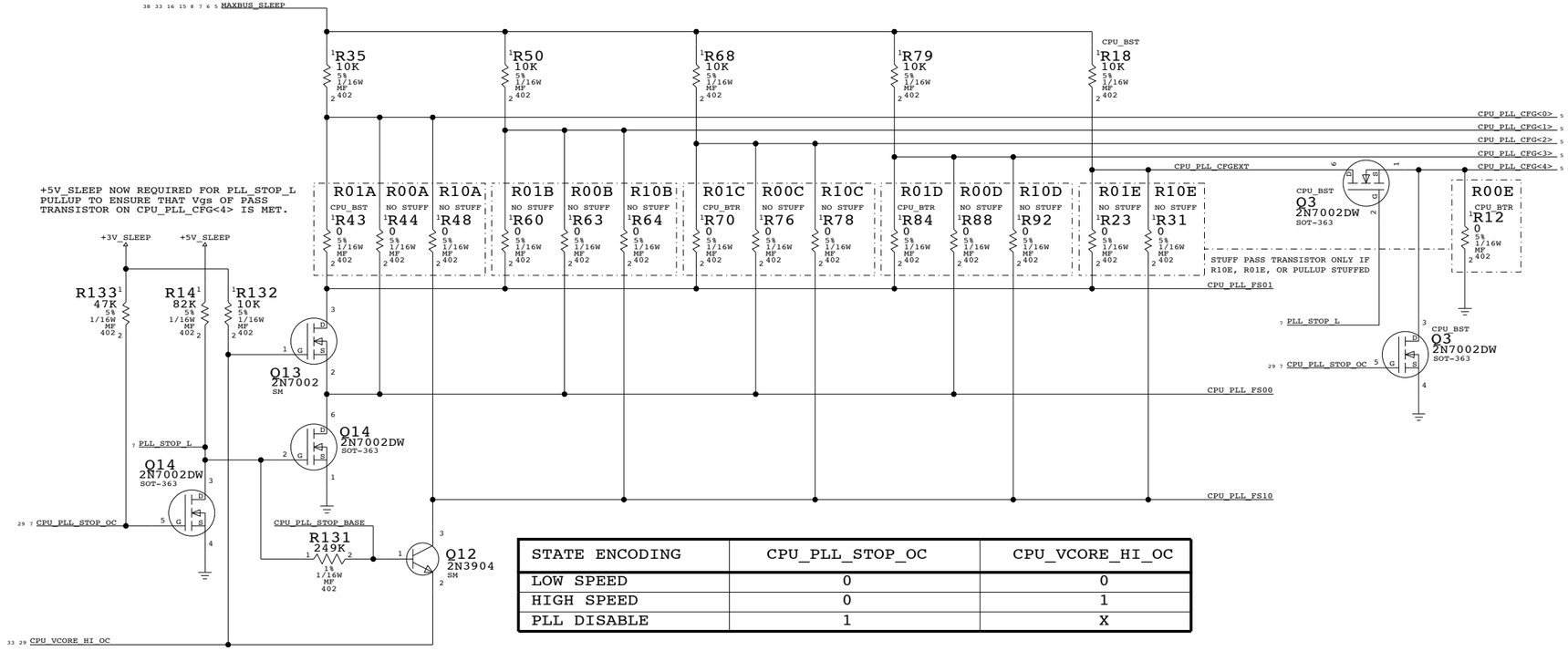
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	01
SCALE: NONE	SHT 6 OF 44	

CPU PLL CONFIG CIRCUITRY



STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

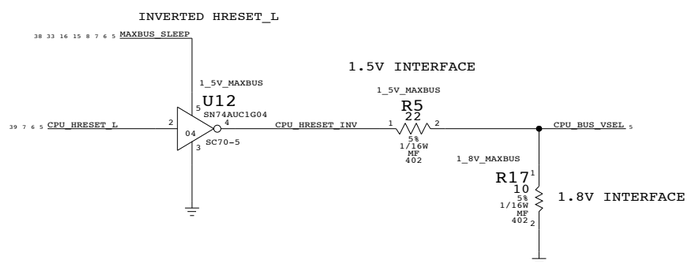
CPU FREQUENCY CONFIGURATION

APOLLO 7

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ (MHZ)	133MHZ (MHZ)	CPU_PLL_CFG 4 0123 E ABCD HEX
0.0X	PLL OFF		0 1111 0F
1.0X	PLL BYPASS		0 0011 03
2.0X	333	267	0 0100 04
3.0X	500	400	0 1000 08
4.0X	667	533	0 1010 0A
5.0X	833	667	0 1011 0B
5.5X	917	733	0 1001 09
6.0X	1000	800	0 1101 0D
6.5X	1083	867	0 0101 05
7.0X	1167	933	0 0010 02
7.5X	1250	1000	0 0001 01
8.0X	1333	1067	0 1100 0C
8.5X	1417	1133	0 0110 06
9.0X	1500	1200	1 0111 17
9.5X	1583	1267	0 0111 07
10.0X	1667	1333	1 1010 1A
10.5X	1750	1400	1 1000 18
11.0X	1833	1467	1 1001 19
11.5X	1917	1533	0 0000 00
12.0X	2000	1600	1 1011 1B
12.5X	2083	1667	1 1111 1F
13.0X	2167	1733	1 0101 15
13.5X	2250	1800	0 1110 0E
14.0X	2333	1867	1 1100 1C
15.0X	2500	2000	1 0001 11
16.0X	2667	2133	1 1101 1D
17.0X	2833	2267	1 0000 10
18.0X	3000	2400	1 0010 12
20.0X	3333	2667	1 0011 13
21.0X	3500	2800	1 0100 14
24.0X	4000	3200	1 0110 16
28.0X	4667	3733	1 1110 1E

CPU CONFIGURATION

MAXBUS VSEL



DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L NEED TO CHARACTERIZE

BUSTYPE SELECT

APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

CPU CONFIGURATION

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6570 | REV. 01

SCALE NONE | SHT 7 OF 44

INTREPID BOOT STRAPS

BIT 32 TO 39

MAXBUS_SLEEP

R640	R639	R638	R666	R622	R619	R618	R653	R621	R620	R652	R650
NO STUFF	NO STUFF	NO STUFF		NO STUFF							
10K 5% 1/16W MF 402											

CPU_DATA<32>
CPU_DATA<33>
CPU_DATA<34>
CPU_DATA<35>
CPU_DATA<36>
CPU_DATA<37>
CPU_DATA<38>
CPU_DATA<39>

R622: DDR TPDMode Enable_h 0: TDI, TDI output, (JTAG) 1: TDI input
R619: Reserved, Always Active
R618: DDR ATPGen Pol 0: Active Low 1: Active High
R653: ExtPLL SPwn Pol 0: Active High 1: Active Low
R621: Spare
R620: Spare
R652: Spare
R650: Spare

BIT 40 TO 47

MAXBUS_SLEEP

R641	R665	R664	R693	R694	R699
NO STUFF	SSCG	NO STUFF	NO_SSCG	NO STUFF	NO STUFF
10K 5% 1/16W MF 402					

CPU_DATA<40>
CPU_DATA<41>
CPU_DATA<42>
CPU_DATA<43>
CPU_DATA<44>
CPU_DATA<45>
CPU_DATA<46>
CPU_DATA<47>

R648	R677	R623	R651	R649	R678	R679	R684
			NO_SSCG		SSCG		
10K 5% 1/16W MF 402							

R648: Spare
R677: Spare
R623: BIT2
R651: BIT1
R649: BIT0
R678: InternalSpreadEn 0: Internal 1: Active
R679: PCI1 Source Clock (no spread) 0: PLL2 1: PLL4
R684: PCI0 Source Clock (no spread) 0: PLL2 1: PLL4

PLL4MODESEL_NXT[2:0]
000: 166.4MHz (2.5X)
001: 149.76MHz
010: 133.12MHZ (2.0X)
011: 99.84MHZ (1.5X)
100: 83.20MHZ

MODE A (2.5X) IS FOR STATIC OPERATION
MODE C (2.0X) IS FOR CLOCK SLEW OPERATION

BIT 48 TO 55

MAXBUS_SLEEP

R696	R695	R667	R668	R643	R642	R698
SSCG	SSCG		NO STUFF	NO STUFF	NO STUFF	
10K 5% 1/16W MF 402						

CPU_DATA<48>
CPU_DATA<49>
CPU_DATA<50>
CPU_DATA<51>
CPU_DATA<52>
CPU_DATA<53>
CPU_DATA<54>
CPU_DATA<55>

R681	R680	R654	R655	R625	R624	R683	R626
NO_SSCG	NO_SSCG	NO STUFF				NO STUFF	
10K 5% 1/16W MF 402							

R681: BUF_REF_CLK_OUTEnable_h 0: Active 1: Reserve
R680: SelPLL4ExtSrc 0: PLL4 1: External source
R654: OBSOLETE (Should remain high) En_PCI_ROM_P 0: Boot ROM on PCI (CardSlot 1) 1: Boot ROM on PCI
R655: TI 1394b work around 0: TI PHY 1394b workaround
R625: BIT2
R624: BIT1
R683: BIT0
R626: Spare

MaxBus output impedance
111: 28.6 ohm
011: 33.3 ohm
101: 40 ohm
001: 50 ohm
110: 66.6 ohm
010: 100 ohm
100: 200 ohm
000: 200 ohm

R159 / C187

+1_5V_INTREPID_PLL — R159 4.7 5% 1/16W MF 402 — +1_5V_INTREPID_PLL7

C187 0.22uF 20% 6.3V CERM 402

H26 VDD15A_7 (PLL6)

U51 INTREPID-REV2.1 BGA (1 OF 9) CRITCAL

CPU_BR_L	E29	BR	INPUT
CPU_BG_L	E26	BG	NO BUS KEEPER
CPU_TS_L	B27	TS	NO BUS KEEPER

CPU_ADDR<0>	D24	A_0
CPU_ADDR<1>	D25	A_1
CPU_ADDR<2>	A27	A_2
CPU_ADDR<3>	E24	A_3
CPU_ADDR<4>	G23	A_4
CPU_ADDR<5>	B26	A_5
CPU_ADDR<6>	A26	A_6
CPU_ADDR<7>	D23	A_7
CPU_ADDR<8>	A25	A_8
CPU_ADDR<9>	E23	A_9
CPU_ADDR<10>	J22	A_10
CPU_ADDR<11>	B25	A_11
CPU_ADDR<12>	H22	A_12
CPU_ADDR<13>	G22	A_13
CPU_ADDR<14>	D22	A_14
CPU_ADDR<15>	B24	A_15
CPU_ADDR<16>	B23	A_16
CPU_ADDR<17>	E22	A_17
CPU_ADDR<18>	J21	A_18
CPU_ADDR<19>	G21	A_19
CPU_ADDR<20>	E21	A_20
CPU_ADDR<21>	A24	A_21
CPU_ADDR<22>	D21	A_22
CPU_ADDR<23>	A23	A_23
CPU_ADDR<24>	H20	A_24
CPU_ADDR<25>	B22	A_25
CPU_ADDR<26>	H21	A_26
CPU_ADDR<27>	A22	A_27
CPU_ADDR<28>	E20	A_28
CPU_ADDR<29>	B21	A_29
CPU_ADDR<30>	D20	A_30
CPU_ADDR<31>	A21	A_31

MAXBUS INTERFACE

CPU_CI_L	G26	CI
CPU_GBL_L	A29	GBL
CPU_TBST_L	A28	TBST
CPU_TSIZ<0>	G24	TSIZ_0
CPU_TSIZ<1>	H24	TSIZ_1
CPU_TSIZ<2>	D26	TSIZ_2
CPU_TT<0>	E25	TT_0
CPU_TT<1>	G25	TT_1
CPU_TT<2>	B28	TT_2
CPU_TT<3>	D27	TT_3
CPU_TT<4>	J25	TT_4
CPU_WT_L	D28	WT

CPU_AACK_L	B29	AACK NO BUS KEEPER - PU
CPU_ARTRY_L	H23	ARTRY NO BUS KEEPER - PU
CPU_HIT_L	B31	HIT INPUT - PU
CPU_QREQ_L	A32	QREQ INPUT - PD
CPU_QACK_L	G27	QACK NO BUS KEEPER - ?
INT_SUSPEND_REQ_L	AK9	SUSPENDREQ
INT_SUSPEND_ACK_L	AM8	SUSPENDACK

Vin = Intrepid Vcore (1.5V)
Vout = MaxBus rail (1.8V)

FB BUFFER HAS 50 OHM OUTPUT IMPEDANCE

R169 511 1% 1/16W MF 402

INT_CPUFB_IN	J24	CPU_FB_IN	
INT_CPUFB_OUT	H16	CPU_FB_OUT	NO BUS KEEPER - PU
SYSCLK_LA_TP	G8	ANALYZER_CLK	
CPU_CLK_EN	AH9	STOPCPUCLK	INPUT - PU
INTREPID_ACS_REF	H13	ACS_REF	NO BUS KEEPER - ?
SYSCLK_CPU	J15	CPU_CLK	NO BUS KEEPER - PU
CPU_TBEN	A31	TBEN	NO BUS KEEPER - PU

R168 0 5% 1/16W MF 402

R161 1K 1% 1/16W MF 402

INTREPID OUTPUTS HIGH BY DEFAULT

VSSA_7 (PLL6) — H25

DBG	A30	CPU_DBG_L
DRDY	G28	CPU_DRDY_L
DTI_0	K25	CPU_DTI<0>
DTI_1	D29	CPU_DTI<1>
DTI_2	B30	CPU_DTI<2>
TA	E27	CPU_TA_L
TEA	E28	CPU_TEA_L

SHORT = 1" SHORTER THAN MATCHED LENGTH
LONG = 1" LONGER THAN MATCHED LENGTH

INT_CPUFB_OUT2 — R155 0 5% 1/16W MF 402 — INT_CPUFB_OUT_SHORT — R140 0 5% 1/16W MF 402 — INT_CPUFB_OUT_NORM — R128 0 5% 1/16W MF 402 — INT_CPUFB_LONG

R146 0 5% 1/16W MF 402 (NO STUFF)

R147 0 5% 1/16W MF 402

INT_CPUFB_IN

R141 0 5% 1/16W MF 402

R136 0 5% 1/16W MF 402 (NO STUFF) — INT_CPUFB_IN_NORM

THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:
1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
2/ D46 - SELPCI1SPREADCLK - SLEEP/WAKE CYCLE REQUIRED
3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT

IF A STRAP IS NOT LISTED, THEN
IT CANNOT BE CHANGED BY SOFTWARE

MAXBUS PULL-UPS

MAXBUS_SLEEP

CPU_TS_L	RP3 10K 5% 1/16W SM1	2 7
CPU_TA_L	RP3 10K 5% 1/16W SM1	1 8
CPU_ARTRY_L	RP3 10K 5% 1/16W SM1	4 5
CPU_BR_L	RP2 10K 5% 1/16W SM1	1 8
CPU_HIT_L	R152 10K 5% 1/16W MF 402	1 2
CPU_DRDY_L	RP2 10K 5% 1/16W SM1	3 6
CPU_TEA_L	RP2 10K 5% 1/16W SM1	4 5
CPU_AACK_L	RP2 10K 5% 1/16W SM1	2 7
CPU_DBG_L	R150 10K 5% 1/16W MF 402	1 2
CPU_BG_L	RP3 10K 5% 1/16W SM1	3 6
CPU_QREQ_L	R151 10K 5% 1/16W MF 402	1 2

INTREPID BOOT STRAPS

BIT 56 TO 63

MAXBUS_SLEEP

R669	R645	R697	R670	R644	R646
NO STUFF	NO STUFF	NO STUFF	NO STUFF		NO STUFF
10K 5% 1/16W MF 402					

CPU_DATA<56>
CPU_DATA<57>
CPU_DATA<58>
CPU_DATA<59>
CPU_DATA<60>
CPU_DATA<61>
CPU_DATA<62>
CPU_DATA<63>

R656	R685	R657	R628	R682	R658	R627	R629
						NO STUFF	
10K 5% 1/16W MF 402							

R656: Spare
R685: Spare
R657: OBSOLETE Reserved, Always 0 if: 0-15Fx / Reg 0-1FF / PCI1 / 2-3 PCI1
R628: PCI1_GNT2_L / PCI1_GPIO6
R682: PCI1_REQ2_L / PCI1_GPIO5
R658: PCI1_GNT1_L / PCI1_GPIO4
R627: PCI1_REQ1_L / PCI1_GPIO3
R629: FireWire PHY interface 0: Legacy interface 1: B-Mode interface
Processor Bus Mode 0: 60x Bus (G3) 1: MPX Bus (G4)

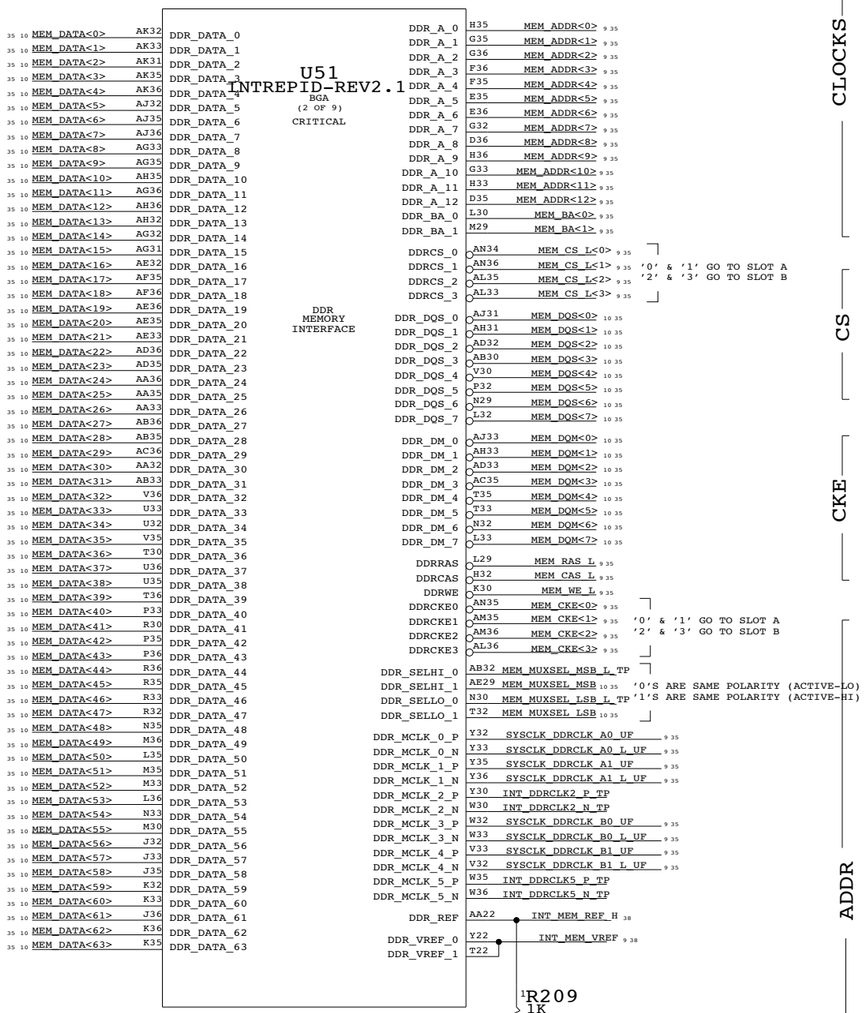
Intrepid MaxBus

APPLE COMPUTER INC.

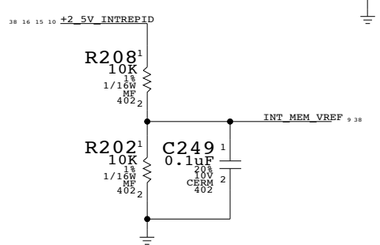
SIZE	DRAWING NUMBER	REV.
D	051-6570	01
SCALE: NONE	SHT 8 OF 44	

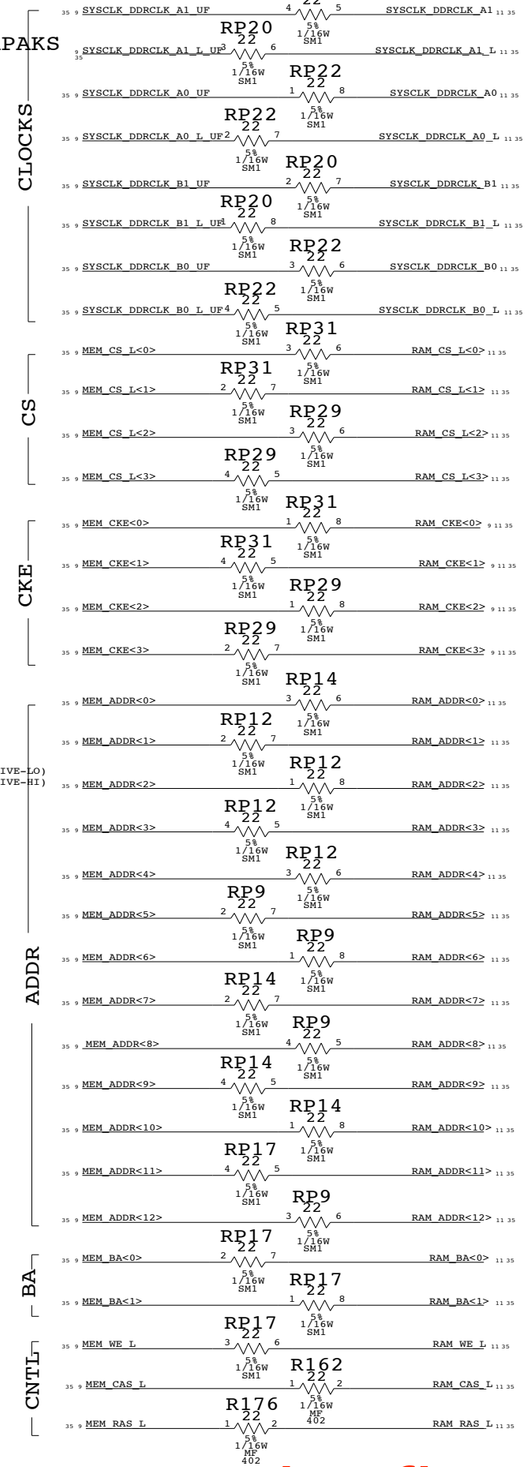
SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

PINS ARE SWAPABLE FOR RPAKS

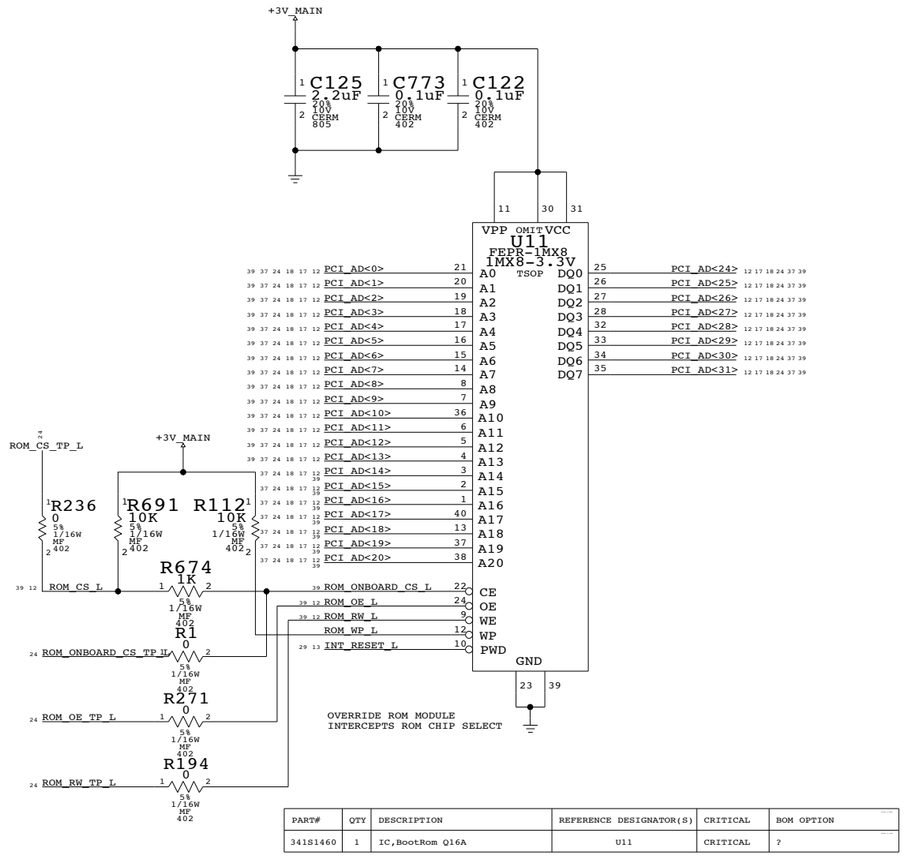


MEM_VREF



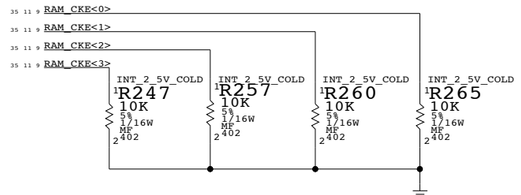


1MB BOOT ROM



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1460	1	IC,BootRom Q16A	U11	CRITICAL	?

Weak pulldowns ensure CKEs stay low
after 2.5V I/O to Intrepid shuts off.

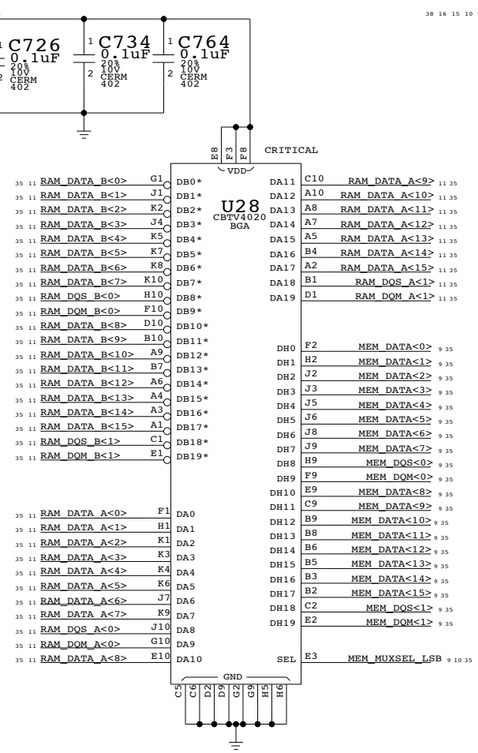


INT - DDR/BOOTROM

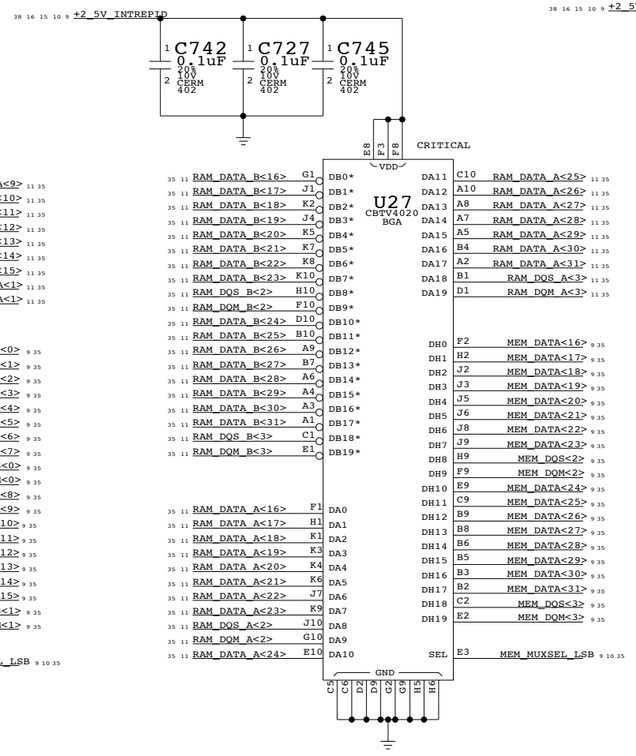
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	01
SCALE: NONE	SHT 9 OF 44	

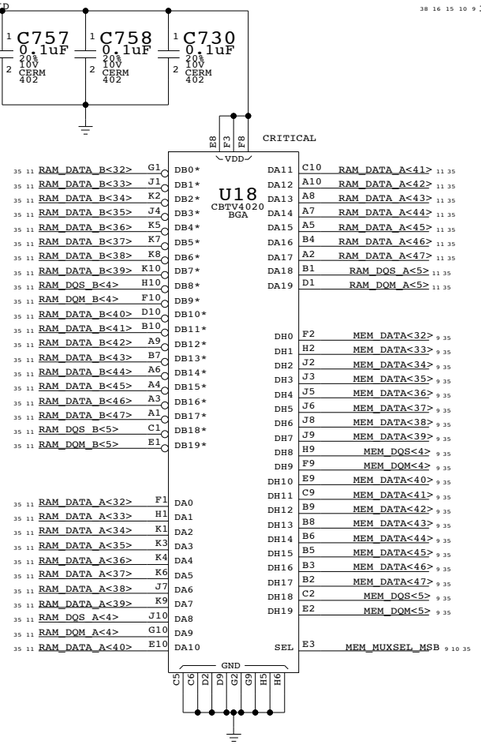
BIT 0..15



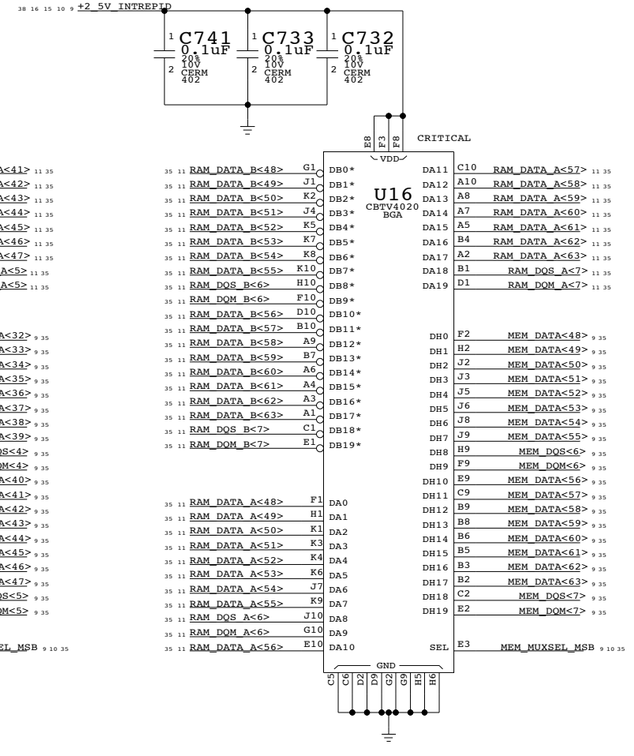
BIT 16..31



BIT 32..47



BIT 48..63



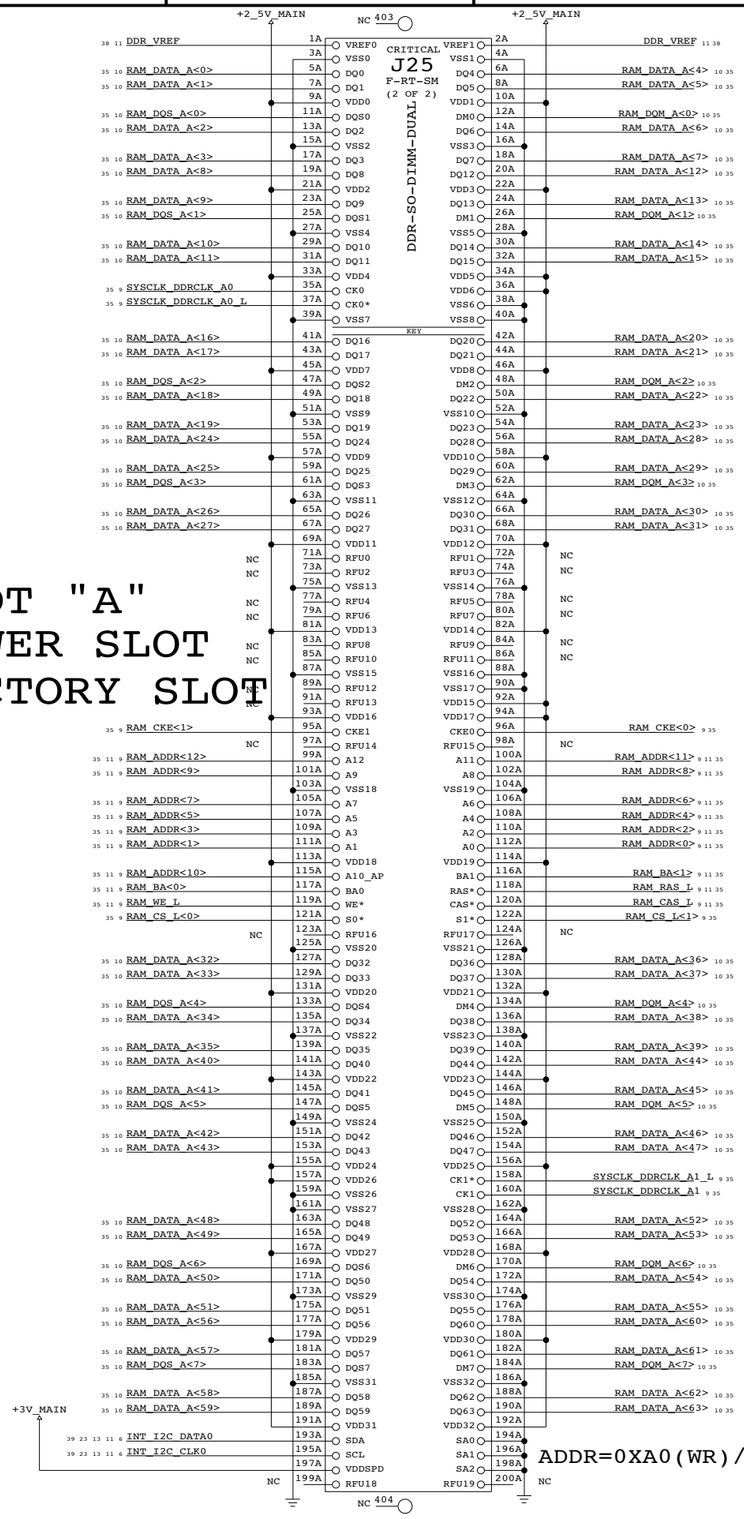
SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND

16BIT 2:1 DDR MUXES

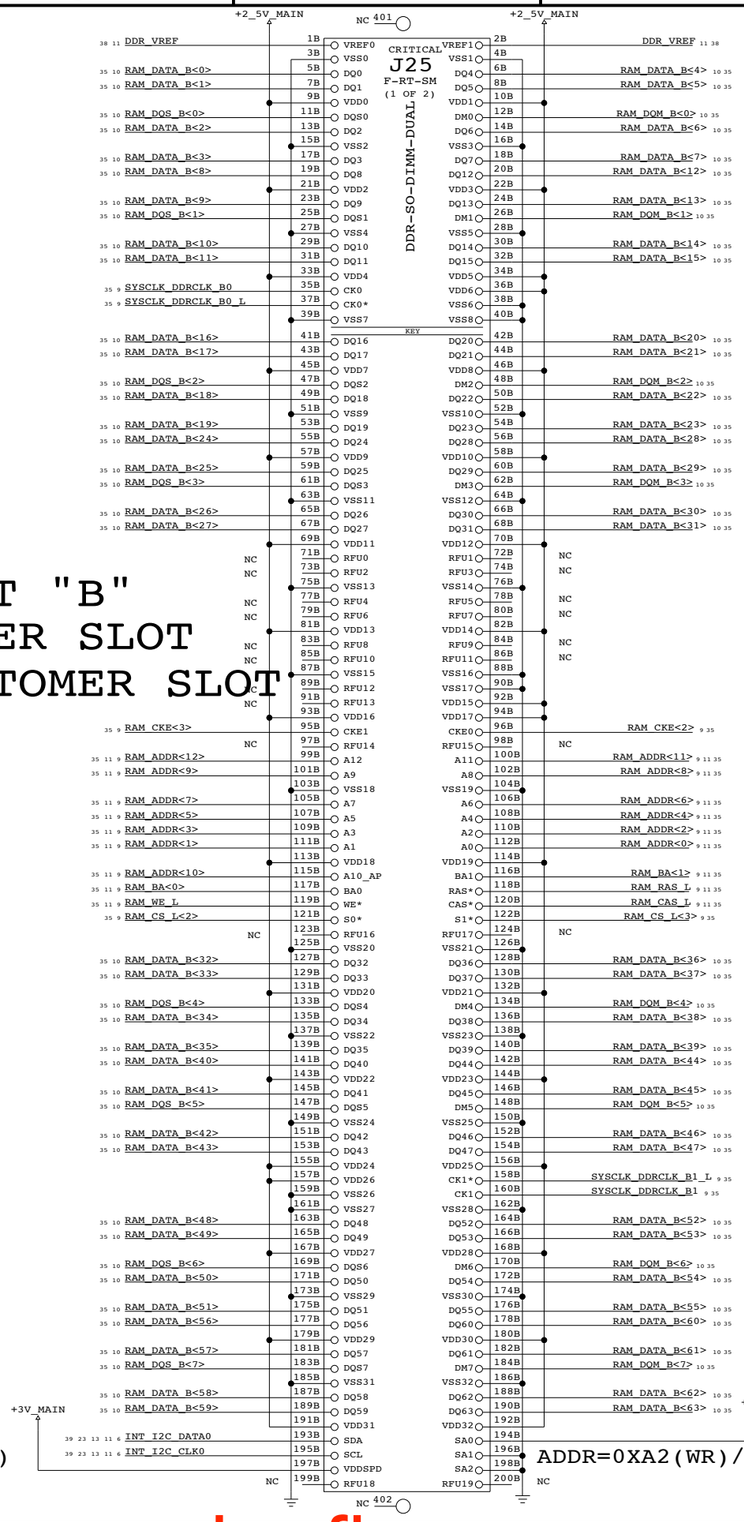
APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6570 | REV. 01

SCALE NONE | SHT 10 OF 44

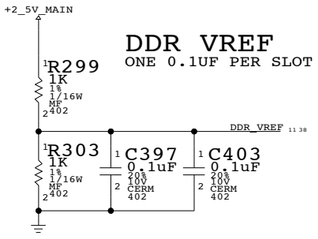


SLOT "A"
LOWER SLOT
FACTORY SLOT



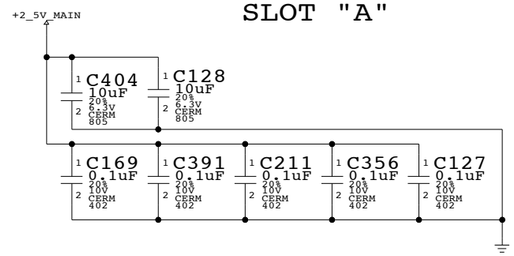
SLOT "B"
UPPER SLOT
CUSTOMER SLOT

NOTE: The SODIMM connector footprint has a through-hole slot on the PCB for additional mounting

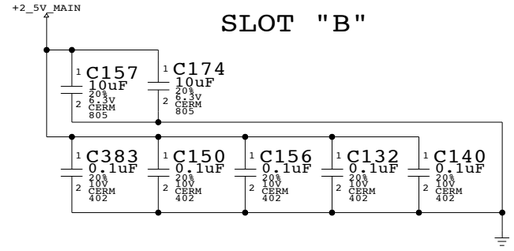


DDR VREF
ONE 0.1UF PER SLOT

DDR BYPASS
SLOT "A"



SLOT "B"

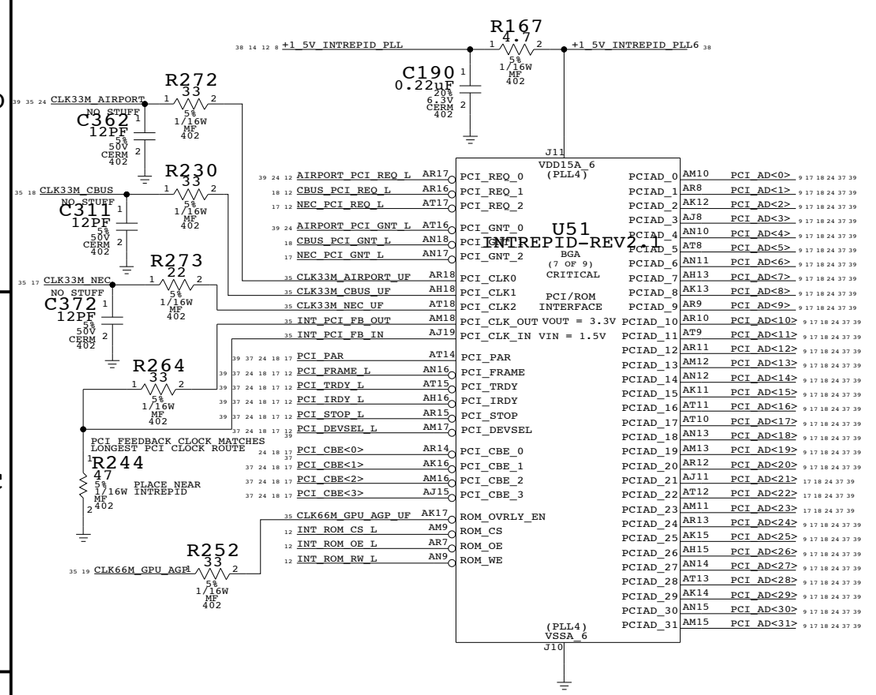


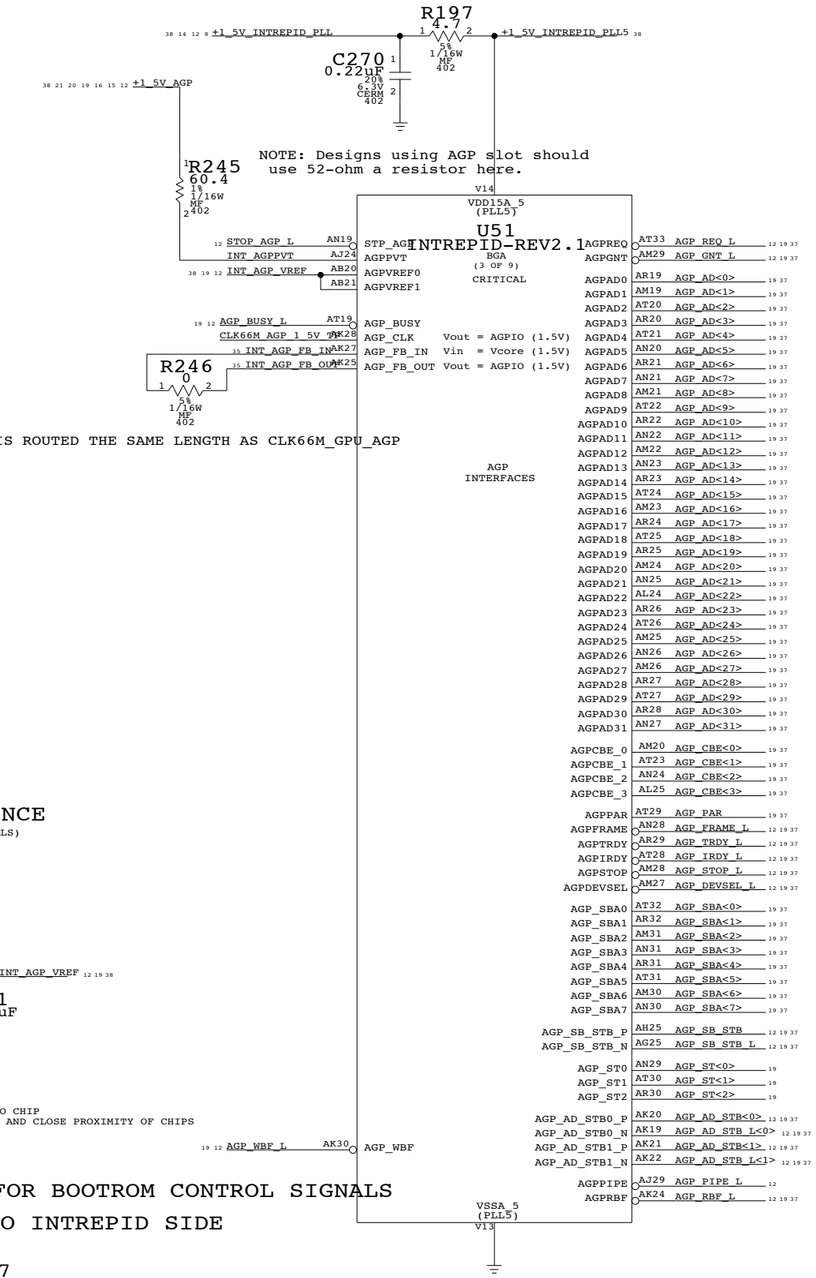
DDR SODIMM CONNS

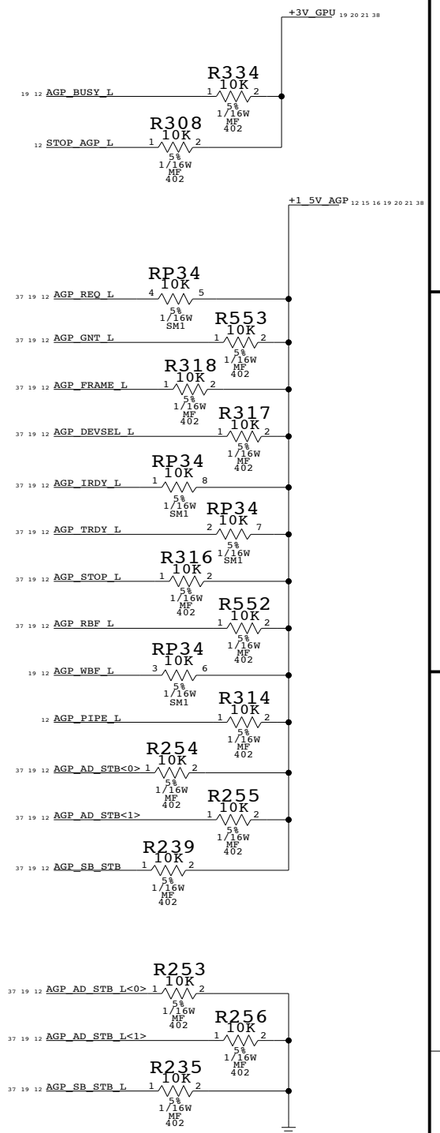
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	01
SCALE: NONE	SHT 11 OF 44	

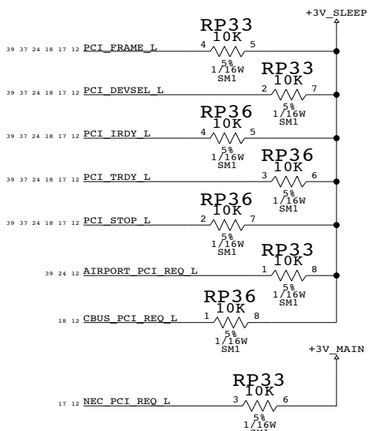
AGP PULL-UPS/PULL DOWNS







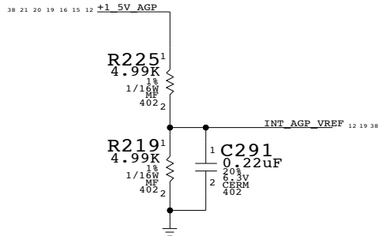
PCI PULL-UPS



NEC USB2 REQ REMAINS ON +3V_MAIN
BECAUSE THIS CHIP IS POWERED DURING SLEEP

AGP I/O REFERENCE

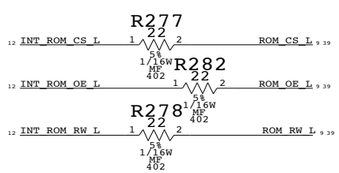
(PLACE CLOSE TO INTREPID AGP BALLS)



SIMPLY PROVIDING REFERENCE TO CHIP
BECAUSE SINGLE AGP PWR PLANE AND CLOSE PROXIMITY OF CHIPS

SERIES RESISTORS FOR BOOTROM CONTROL SIGNALS

PLACE CLOSE TO INTREPID SIDE

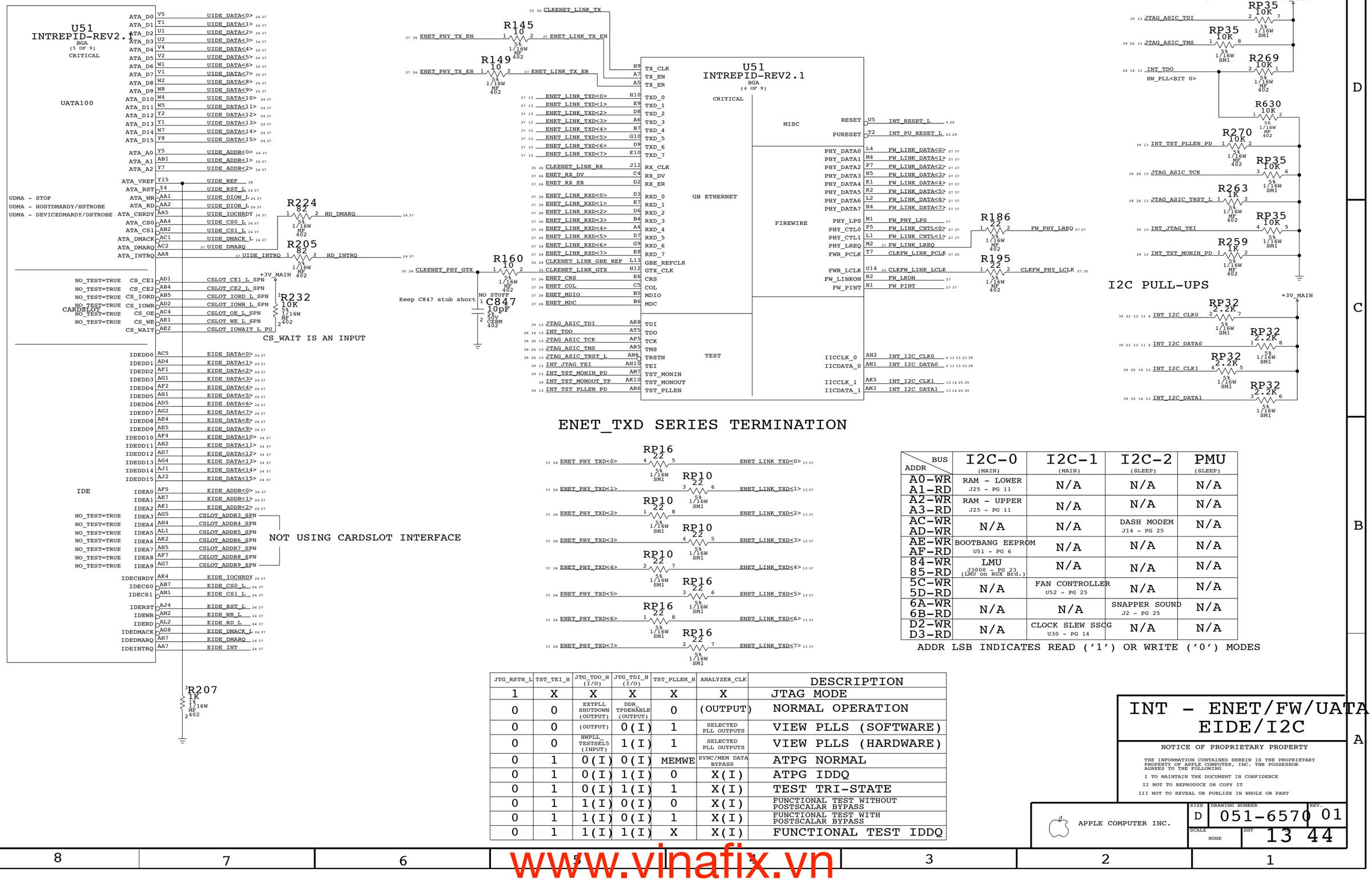


INTREPID AGP/PCI

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6570 | REV. 01

SCALE NONE | SHT 12 OF 44



BUS / ADDR	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
A0-WR A1-RD	RAM - LOWER J25 - PG 11	N/A	N/A	N/A
A2-WR A3-RD	RAM - UPPER J25 - PG 11	N/A	N/A	N/A
AC-WR AD-WR	N/A	N/A	DASH MODEM J14 - PG 25	N/A
AE-WR AF-RD	BOOTBANG EEPROM U51 - PG 6	N/A	N/A	N/A
84-WR 85-RD	LMU J3000 - PG 23 (LMU on RUX Brd.)	N/A	N/A	N/A
5C-WR 5D-RD	N/A	FAN CONTROLLER U52 - PG 25	N/A	N/A
6A-WR 6B-RD	N/A	N/A	SNAPPER SOUND J2 - PG 25	N/A
D2-WR D3-RD	N/A	CLOCK SLEW SSCG U30 - PG 14	N/A	N/A

JTG_RSTN_L	TST_TEI_H	JTG_TDO_H (I/O)	JTG_TDI_H (I/O)	TST_PLLEN_H	ANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	EXTPLL SHUTDOWN (OUTPUT)	DDR_ TPDENABLE (OUTPUT)	0	(OUTPUT)	NORMAL OPERATION
0	0	(OUTPUT)	0(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	HWPLL_ TESTSEL5 (INPUT)	1(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0(I)	0(I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0(I)	1(I)	0	X(I)	ATPG IDDQ
0	1	0(I)	1(I)	1	X(I)	TEST TRI-STATE
0	1	1(I)	0(I)	0	X(I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1(I)	0(I)	1	X(I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1(I)	1(I)	X	X(I)	FUNCTIONAL TEST IDDQ

USB PORT ASSIGNMENTS

PORT A - PORT D/UNUSED

R181 10K 5% 1/16W MF 402 — USB_DAM
R183 10K 5% 1/16W MF 402 — USB_DAP
R156 10K 5% 1/16W MF 402 — USB_DBM
R157 10K 5% 1/16W MF 402 — USB_DBP
R164 10K 5% 1/16W MF 402 — USB_DCM
R165 10K 5% 1/16W MF 402 — USB_DCP
R182 10K 5% 1/16W MF 402 — USB_DDM
R180 10K 5% 1/16W MF 402 — USB_DDP

PORT E/BLUETOOTH

R174 22 5% 1/16W MF 402 — USB_DEP — BT_USB_DP
R179 22 5% 1/16W MF 402 — USB_DEM — BT_USB_DM
R178 15K 5% 1/16W MF 402
R175 15K 5% 1/16W MF 402

PORT F/MODEM

R192 22 5% 1/16W MF 402 — USB_DFP — MODEM_USB_DP
R188 22 5% 1/16W MF 402 — USB_DFM — MODEM_USB_DM
R189 15K 5% 1/16W MF 402
R193 15K 5% 1/16W MF 402

INT - USB/GPIOS/I2S

APPLE COMPUTER INC.

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D	051-6570	01
SCALE: NONE	SHT 14 OF 44	

+2_5V_MAIN
R568 NO STUFF 0 5% 1/16W MF 603
+1_8V_MAIN
R565 0 5% 1/16W MF 603
LTC1962_INT_VIN
U49 LT1962-ADJ MSOP
IN, NC, NC, SHDN, OUT, ADJ, BYP, GND
LT1962_INT_ADJ
LT1962_INT_BYP
C721 1uF 10% 10V CERM 603
C392 0.01uF 20% 16V CERM 402
R574 18.7K 1% 1/16W MF 402
C723 10uF 20% 6.3V CERM 805
R567 68.1K 1% 1/16W MF 402
+1_5V_INTREPID_PLL
-> 1.55V OUTPUT

+3V_SLEEP
R148 10K 5% 1/16W MF 402 — CBUS_INT_L
R746 10K 5% 1/16W MF 402 — AIRPORT_PCI_INT_L
+3V_MAIN
R158 10K 5% 1/16W MF 402 — NEC_PCI_INT_L
PCI INTERRUPTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
359S0086	1	IC,CY28512-2	U31	CRITICAL	SSCG

+3V_MAIN
GPIO/EXTINT PULLUPS
R187 10K — USB_PWREN_EF_L
R191 10K — USB_OC_EF_L
RP11 10K — USB_OC_AB_L
RP11 10K — USB_PWREN_CD_L
RP8 10K — USB_PWREN_AB_L
RP11 10K — USB_OC_CD_L
RP8 10K — INT_EXTINT14_PU
RP5 10K — INT_EXTINT8_PU
RP6 10K — COMM_RING_DET_L
RP11 10K — INT_GPIO15_PU
RP6 10K — PMU_INT_NMI
RP6 10K — PMU_INT_L
R250 10K — PMU_REQ_L
RP7 10K — INT_GPIO12_PU
RP7 10K — INT_EXTINT13_PU
RP4 10K — INT_EXTINT16_PU
RP5 10K — INT_EXTINT11_PU
RP6 10K — INT_EXTINT10_PU
RP4 10K — INT_EXTINT12_PU
RP8 10K — INT_GPIO9_PU
RP8 10K — INT_GPIO1_PU
R153 10K — INT_EXTINT3_PU
RP15 10K (USB_MODEM) — INT_MOD_DTO_UF
RP15 10K (USB_MODEM) — INT_MOD_CLKOUT_UF
RP15 10K (USB_MODEM) — INT_MOD_DTI
RP15 10K (USB_MODEM) — INT_MOD_SYNC_UF
R206 10K (USB_MODEM) — INT_MOD_BITCLK_UF
R166 100K — SND_HW_RESET_L

+3V_MAIN
+2_5V_MAIN
L15 SSCG 400-OHM-EMI SM-1
L14 SSCG 400-OHM-EMI SM-1
+3V_CG_PLL_MAIN
MAIN_RESET_L
C400 SSCG 0.1uF 20% 10V CERM 402
C402 SSCG 1uF 20% 10V CERM 603
C399 SSCG 0.1uF 20% 10V CERM 402
+2_5V_CG_MAIN
C394 SSCG 0.1uF 20% 10V CERM 402
R286 NO STUFF 0 5% 1/16W MF 402
R287 SSCG 10K 5% 1/16W MF 402
R288 SSCG 10K 5% 1/16W MF 402
R295 NO STUFF 10K 5% 1/16W MF 402

U31 CY28512D TSSOP OMIT CRITICAL
INTERNAL 250K PULL-UP
OUTPUT IMPEDANCE ~18-20 OHMS
VDD0, VDD1, VDDA, VDDC, VDDQ
CLKIN — INT_REF_CLK_OUT
FSEL — CG_FSEL
SCLK — INT_I2C_CLK1
SDATA — INT_I2C_DATA1
ADDRSEL INTERNAL 250K PULL-DOWN — CG_ADDRSEL
RESET* — CG_RESET_L
PD* — CG_SYSCLK_EN
LOCK OPEN DRAIN OUTPUT — CG_LOCK
ODSEL INTERNAL 250K PULL-UP
VSSA, VSSC, VSSQ
CPU0 — CG_CLKOUT1 — R293 SSCG 33 5% 1/16W MF 402 — INT_REF_CLK_IN
R292 SSCG 75 5% 1/16W MF 402 — PLACE NEAR INTREPID TO MINIMIZE OVERSHOOT
R284 SSCG 0 5% 1/16W MF 402 — VCORE_VGATE
R296 10K 5% 1/16W MF 402
R142 SSCG 0 5% 1/16W MF 402 — VCORE_VGATE

R467 NO STUFF 0 — SYSTEM_CLK_EN
R457 0 5% 1/16W MF 402 — INT_TDO — CG_SYSCLK_EN
J9 U.FL-R_SMT F-ST-SM — NO STUFF — CLK18M_INT_EXT
R134 NO STUFF 0 5% 1/16W MF 402 — CLK18M_INT_XOUT
R113 NO STUFF 51 5% 1/16W MF 402
R144 NO STUFF 10M 5% 1/16W MF 402
R143 0 5% 1/16W MF 402
Y2 CRITICAL 18.432M 8X4.5MM-SM — CLK18M_XTAL_IN
C152 22pF 5% 50V CERM 402
C151 22pF 5% 50V CERM 402
CRYSTAL LOAD CAPACITANCE IS 16PF

R218 0 5% 1/16W MF 402 — INT_REF_CLK_OUT1 — INT_REF_CLK_OUT_UF — INT_REF_CLK_IN

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0004	197S0035		Y2	Alt. for Siward Part

HWPLL_TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES	RES-0402-V2	RESISTOR	10K		1/16W	5%	R292	NO_SSCG

R240 4.7 5% 1/16W MF 402 — +1_5V_INTREPID_PLL8
R280 4.7 — +1_5V_INTREPID_PLL4
R279 4.7 — +1_5V_INTREPID_PLL3
R243 4 — +1_5V_INTREPID_PLL2
R201 4.7 — +1_5V_INTREPID_PLL1
C337 0.22uF 20% 6.3V CERM 402
C389 0.22uF 20% 6.3V CERM 402
C388 0.22uF 20% 6.3V CERM 402
C386 0.22uF 20% 6.3V CERM 402
C387 0.22uF 20% 6.3V CERM 402

+3V_MAIN
L13 FERR-EMI-100-OHM SM
+3V_INTREPID_USB
C235 0.01uF 20% 16V CERM 402
C246 0.1uF 20% 10V CERM 402
C256 10uF 20% 6.3V CERM 805

R450 SSCG 0 5% 1/16W MF 402 — CG_FSEL

U51 INTREPID-REV2.1 BGA CRITICAL (6 OF 9)

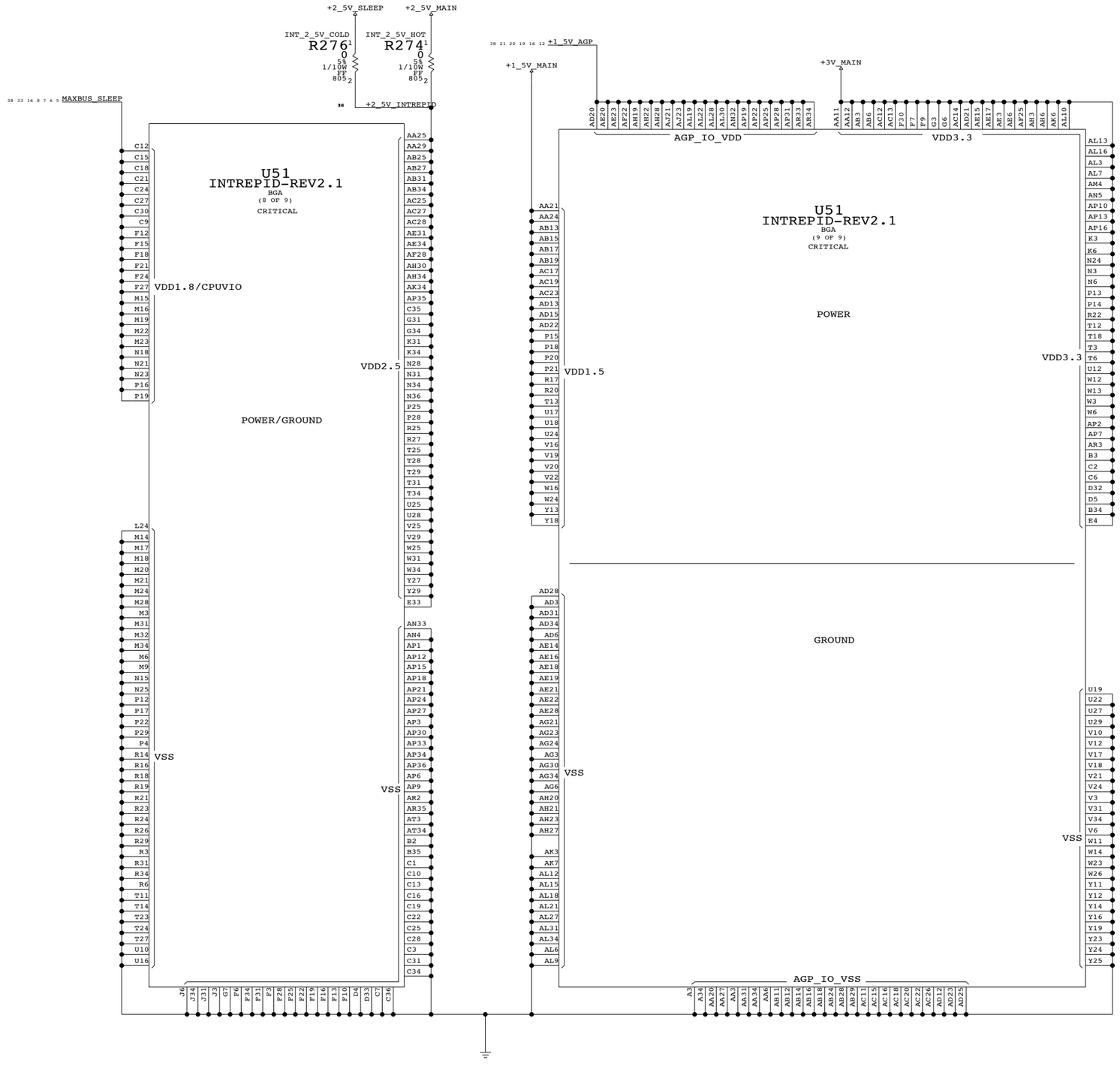
GPIO0	G5	VCORE A/B SEL	
GPIO1	E1		
GPIO2	J7	GENERAL PURPOSE I/O'S	
GPIO3	F2		
GPIO4	J8		
GPIO5	H5		
GPIO6	L9		
GPIO9	H4		
GPIO11	J5		
GPIO12	K8		
GPIO15	F1		
GPIO16	K7		
EXTINT0	F33	INTERRUPTS	
EXTINT1	E34		
EXTINT2	C33		
EXTINT3	D34		
EXTINT4	B33		
EXTINT5	A33		
EXTINT6	E31		
EXTINT7	G30		
EXTINT8	D31	POWERBOOK SPARE	
EXTINT9	C32		
EXTINT10	B32	CBUS_REG_L	
EXTINT11	E30	CBUS_IREQ_L	
EXTINT12	J9		
EXTINT13	F4		
EXTINT14	D1		
EXTINT15	E2		
EXTINT16	H7		
EXTINT17	G4		
CPU_INT	D30		
PCIPME	AJ7		
PROCSLEEPREQ	AK6		
PENDPROCINT	AN8		
XTAL_IN	U4		
XTAL_OUT	V15		
STOPXTAL	AN7	CLOCKS	
WATCHDOG	AT7		
BUF_REF_CLK_OUT	U15		
SS_REF_CLK_IN	K9		
PCI VDD15A_1 (PLL1)	AA16		
PCI VDD15A_2 (PLL2)	AJ12		
PCI VDD15A_3 (PLL3)	AJ17		
PCI VDD15A_4 (PLL7)	AJ18		
VDD15A_8 (PLL9)	AG29		
VDDU33_1	F8		
VDDU33_2	U8		
VSSA1 (PLL1)	AA15		
VSSA2 (PLL2)	AJ13		
VSSA3 (PLL3)	AJ16		
VSSA4 (PLL7)	AK18		
VSSA_8 (PLL9)	AH29		
VSSU_1	R9		
VSSU_2	R8		

SCCTXDA	AF9	COMM_TXD_L	25 39
SCCRTSA	AN3	COMM_RTS_L	25 39
SCCDTRA	AP10	COMM_DTR_L	25 39
SCCRXDA	AG11	COMM_RXD	25 39
SCCGPIOA	AG9	COMM_GPIO_L	25 39
SCCTRXCA	AT4	COMM_TRXC	25 39
VIA			
MISO	AR4	PMU_FROM_INT	29
REQ*	AL5	PMU_REQ_L	14 29
MOSI	AG10	PMU_TO_INT	29
ACK*	AP4	PMU_ACK_L	29
SCK	AM5	PMU_CLK	29
SCCTXDB	AR4	PMU_FROM_INT	29
SCCRTSB	AL5	PMU_REQ_L	14 29
SCCRXDB	AG10	PMU_TO_INT	29
SCCGPIOB	AP4	PMU_ACK_L	29
SCCTRXCB	AM5	PMU_CLK	29
USB_VD0_P	L8	USB_DAP	14
USB_VD0_N	L7	USB_DAM	14
USB_VD1_P	G2	USB_DBP	14
USB_VD1_N	G1	USB_DBM	14
USB_PRTPWR0	J4	USB_PWREN_AB_L	14
USB_PWRFLT0	K4	USB_OC_AB_L	14
USB_VD2_P	H2	USB_DCP	14
USB_VD2_N	H1	USB_DCM	14
USB_VD3_P	M7	USB_DDP	14
USB_VD3_N	M8	USB_DDM	14
USB_PRTPWR1	J2	USB_PWREN_CD_L	14
USB_PWRFLT1	J1	USB_OC_CD_L	14
USB_VD4_P	K5	USB_DEP	14 37
USB_VD4_N	L5	USB_DEM	14 37
USB_VD5_P	P8	USB_DFP	14 37
USB_VD5_N	N8	USB_DFM	14 37
USB_PRTPWR2	M5	USB_PWREN_EF_L	14
USB_PWRFLT2	N7	USB_OC_EF_L	14
USB			

AUD_DTO	R4	INT_I2S0_SND_TO_DAC_UF	25 39
AUD_DTI	R7	INT_I2S0_SND_FROM_ADC	25 39
AUD_SYNC	T5	INT_I2S0_SND_LRCLK_UF	
AUD_BITCLK	P2	INT_I2S0_SND_SCLK_UF	
AUD_CLKOUT	R5	INT_I2S0_SND_MCLK_UF	
MOD_DTO	R2	INT_MOD_DTO_UF	14
MOD_DTI (SIGNAL FROM MODEM)	T4	INT_MOD_DTI	14 25
MOD_SYNC	R1	INT_MOD_SYNC_UF	14
MOD_BITCLK	V8	INT_MOD_BITCLK_UF	14
MOD_CLKOUT	P1	INT_MOD_CLKOUT_UF	14
AUDIO/I2S			
IICCLK_2	AL4		
IICDATA_2	AH8		
IIC			

+3V_SLEEP
2K 5% 1/16W MF 402 — INT_I2C_CLK2
2K 5% 1/16W MF 402 — INT_I2C_DATA2

RP13 47 — INT_I2S0_SND_TO_DAC
RP13 47 — INT_I2S0_SND_LRCLK
RP13 47 — INT_I2S0_SND_SCLK
RP13 47 — INT_I2S0_SND_MCLK
SOFT_MODEM RP47 47 — INT_MOD_DTO
SOFT_MODEM RP47 47 — INT_MOD_SYNC
SOFT_MODEM RP47 47 — INT_MOD_BITCLK
SOFT_MODEM RP47 47 — INT_MOD_CLKOUT



Intrepid Power

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SCALE: NONE	SHT 15 OF 44	

INTREPID MAXBUS DECOUPLING

24 Balls
4 X 10UF (0805)
28 X 0.22UF (0402)

MAXBUS_SLEEP

C148 10uF, C142 10uF, C182 0.22uF, C178 0.22uF, C141 0.22uF, C145 0.22uF, C214 0.22uF, C163 0.22uF, C164 0.22uF, C225 0.22uF, C160 0.22uF, C159 0.22uF
C144 10uF, C146 10uF, C204 0.22uF, C166 0.22uF, C205 0.22uF, C223 0.22uF, C229 0.22uF, C181 0.22uF, C207 0.22uF, C208 0.22uF, C183 0.22uF, C180 0.22uF
C165 0.22uF, C206 0.22uF, C147 0.22uF, C149 0.22uF, C179 0.22uF, C162 0.22uF, C161 0.22uF, C213 0.22uF

INTREPID CORE DECOUPLING

30 Balls
4 X 10UF (0805)
29 X 0.22UF (0402)

+1_5V_MAIN

C324 10uF, C325 10uF, C299 0.22uF, C279 0.22uF, C262 0.22uF, C292 0.22uF, C248 0.22uF, C302 0.22uF, C300 0.22uF, C290 0.22uF, C272 0.22uF, C259 0.22uF
C201 10uF, C200 10uF, C301 0.22uF, C278 0.22uF, C226 0.22uF, C238 0.22uF, C250 0.22uF, C263 0.22uF, C224 0.22uF, C222 0.22uF, C261 0.22uF, C227 0.22uF
C271 0.22uF, C310 0.22uF, C288 0.22uF, C260 0.22uF, C303 0.22uF, C287 0.22uF, C258 0.22uF, C236 0.22uF, C289 0.22uF

INTREPID AGP I/O DECOUPLING

21 Balls
2 X 10UF (0805)
21 X 0.22UF (0402)

+1_5V_AGP

C381 10uF, C380 10uF, C367 0.22uF, C319 0.22uF, C330 0.22uF, C363 0.22uF, C366 0.22uF, C332 0.22uF, C361 0.22uF, C320 0.22uF, C328 0.22uF, C364 0.22uF
C382 10uF, C379 10uF, C365 0.22uF, C329 0.22uF, C345 0.22uF, C346 0.22uF, C373 0.22uF, C344 0.22uF, C331 0.22uF, C312 0.22uF, C354 0.22uF, C347 0.22uF
C321 0.22uF

INTREPID 3.3V DECOUPLING

57 Balls
4 X 10UF (0805)
40 X 0.22UF (0402)

+3V_MAIN

C378 10uF, C376 10uF, C170 0.22uF, C358 0.22uF, C268 0.22uF, C327 0.22uF, C342 0.22uF, C215 0.22uF, C352 0.22uF, C171 0.22uF, C158 0.22uF, C309 0.22uF
C377 10uF, C375 10uF, C175 0.22uF, C357 0.22uF, C351 0.22uF, C350 0.22uF, C286 0.22uF, C176 0.22uF, C189 0.22uF, C167 0.22uF, C371 0.22uF, C359 0.22uF
C285 0.22uF, C283 0.22uF, C269 0.22uF, C221 0.22uF, C234 0.22uF, C247 0.22uF, C257 0.22uF, C343 0.22uF, C313 0.22uF, C228 0.22uF
C360 0.22uF, C308 0.22uF, C318 0.22uF, C237 0.22uF, C317 0.22uF, C341 0.22uF, C177 0.22uF, C212 0.22uF, C349 0.22uF, C184 0.22uF

INTREPID DDR DECOUPLING

44 Balls
4 X 10UF (0805)
46 X 0.22UF (0402)

+2_5V_INTREPID

C314 10uF, C322 10uF, C304 0.22uF, C266 0.22uF, C172 0.22uF, C281 0.22uF, C243 0.22uF, C253 0.22uF, C334 0.22uF, C241 0.22uF, C348 0.22uF, C192 0.22uF
C191 10uF, C202 10uF, C306 0.22uF, C252 0.22uF, C275 0.22uF, C297 0.22uF, C240 0.22uF, C218 0.22uF, C274 0.22uF, C369 0.22uF, C368 0.22uF, C168 0.22uF
C265 0.22uF, C251 0.22uF, C216 0.22uF, C254 0.22uF, C305 0.22uF, C186 0.22uF, C219 0.22uF, C315 0.22uF, C264 0.22uF, C294 0.22uF
C323 0.22uF, C273 0.22uF, C242 0.22uF, C203 0.22uF, C333 0.22uF, C217 0.22uF, C230 0.22uF, C293 0.22uF, C231 0.22uF, C296 0.22uF
C239 0.22uF, C316 0.22uF, C185 0.22uF, C282 0.22uF, C295 0.22uF, C280 0.22uF

INTREPID/MAIN 2.5V DECOUPLING

10 X 0.22UF (0402)

+2_5V_MAIN

C770 0.22uF, C139 0.22uF, C335 0.22uF, C735 0.22uF, C245 0.22uF, C736 0.22uF, C739 0.22uF, C395 0.22uF, C374 0.22uF, C385 0.22uF

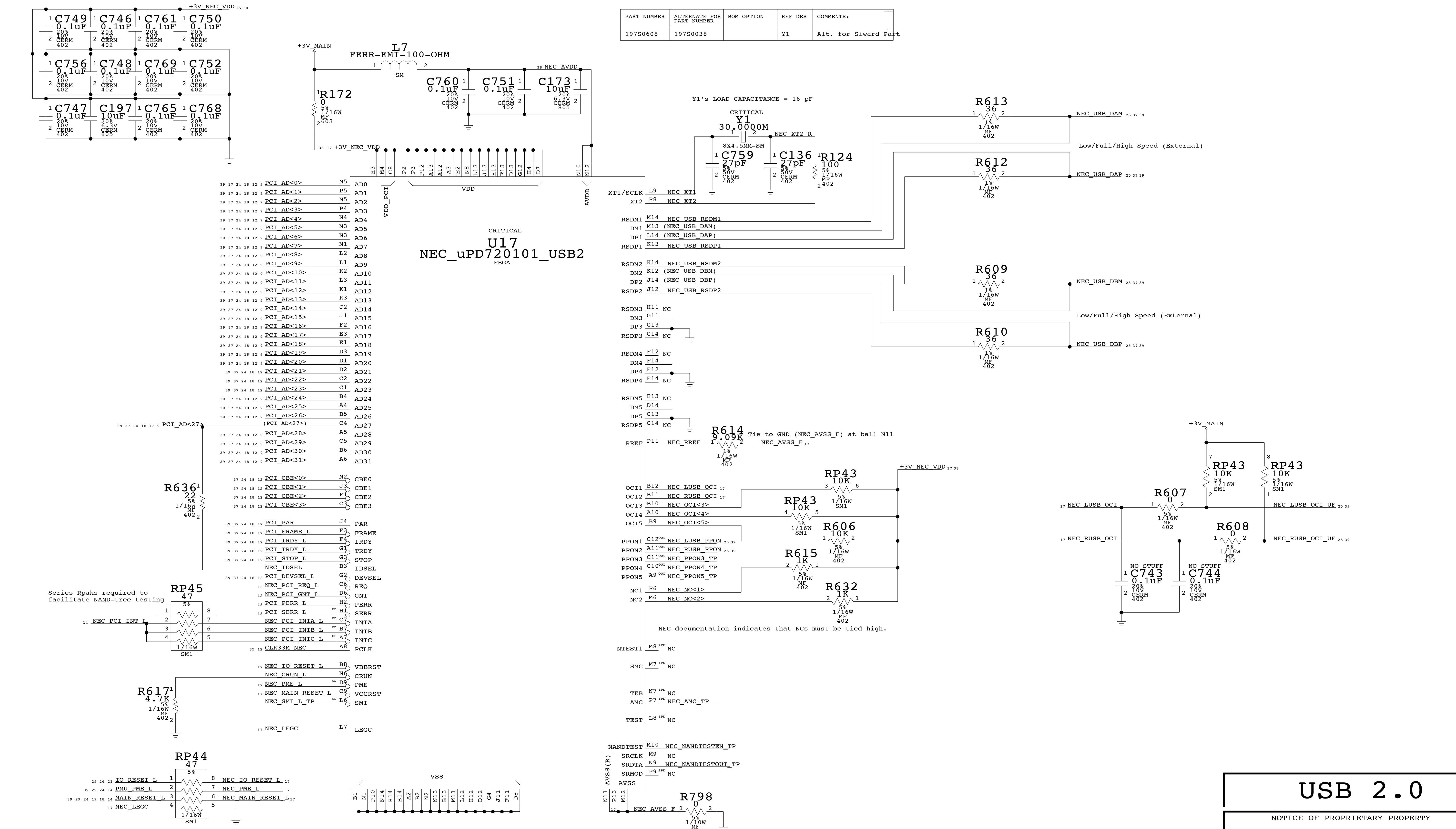
Place these 2.5V Decoupling Caps near the Edge of +2.5V_MAIN and +2.5V_INTREPID split

Intrepid Decoupling

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	01
SCALE: NONE	SHT 16 OF 44	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0608	197S0038		Y1	Alt. for Siward Part



USB 2.0

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APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6570 | REV. 01

SCALE NONE | SHT 17 OF 44

PCI1510 PULL-UPS

+3V_SLEEP
R756 0 5% 1/16W MF 603
+3V_SLEEP_PCCARD
C60 10uF 20% 6.3V CERM 805
C776 10uF 20% 6.3V CERM 805
C789 0.22uF 20% 6.3V CERM 402
C791 0.22uF 20% 6.3V CERM 402
C784 0.22uF 20% 6.3V CERM 402
C782 0.22uF 20% 6.3V CERM 402
C783 0.22uF 20% 6.3V CERM 402
C778 0.22uF 20% 6.3V CERM 402
C775 0.22uF 20% 6.3V CERM 402
R718 10K 5% 1/16W MF 402 — PCI_PERR_L
R714 10K 5% 1/16W MF 402 — PCI_SERR_L
R722 10K 5% 1/16W MF 402 — CBUS_SUSPEND_PU
R721 10K 5% 1/16W MF 402
+2_5V_SLEEP
C787 4.7uF 20% 6.3V CERM 805
C786 0.22uF 20% 6.3V CERM 402
A7 C13 D5 E1 M1 N7 N11 — VCC

+3V_MAIN
+5V_MAIN
U4 TPS2211 SSOI
NC 9 — V_12
5 — V_5_1
6 — V_5_2 — AVCC0
3 — V_3_1 — AVCC1
4 — V_3_2 — AVCC2
10 — AVPP — +VPP_CBUS_SW 18 38
11 — +VCC_CBUS_SW 18 38
12
13
1 — VCCD0
2 — VCCD1
15 — VPPD0
14 — VPPD1
16 — SHTDWN
7 — GND
8 — OC — NC
C40 0.1uF 20% 10V CERM 402
C37 0.1uF 20% 10V CERM 402
0.1UF ARE USED TO INCREASE ESD DISCHARGES OF UP TO 10KV
R726 0 5% 1/16W MF 402 — SLEEP_L_LS5
TPS2211_SHTDWN_L

MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES TO MINIMIZE INDUCTANCE!

U8 PCI1510GGU BGA

NC H10	CLK_48_RSVD/NC		
PCI1510_VR_EN_L D4	VR_EN*	CRITICAL	CLAMP FOR PC-CARD
L8	VR_PORT		CLAMP FOR PCI
		VCCCB B11	
		VCCP L3	
		VCCD0* N13	CBUS_VCCD0_L
		VCCD1* L12	CBUS_VCCD1_L
		VPPD0 K9	CBUS_VPPD0
		VPPD1 M11	CBUS_VPPD1
39 37 24 17 12 9 PCI_AD<0>	N8 AD0	CD1*/CCD1*	L13 CBUS_DET_1_L 18 39
39 37 24 17 12 9 PCI_AD<1>	M7 AD1	CD2*/CCD2*	B5 CBUS_DET_2_L 18 39
39 37 24 17 12 9 PCI_AD<2>	L7 AD2	IORD*/CAD13	F12 CBUS_IORD_L 18
39 37 24 17 12 9 PCI_AD<3>	N6 AD3	IOWR*/CAD15	C11 CBUS_IOWR_L 18
39 37 24 17 12 9 PCI_AD<4>	K4 AD4	OE*/CAD11	G10 CBUS_OE_L 18
39 37 24 17 12 9 PCI_AD<5>	M6 AD5	CE1*/CC/BE0*	H13 CBUS_CE1_L 18
39 37 24 17 12 9 PCI_AD<6>	L6 AD6	VS1*/CVS1	B2 CBUS_VS1 18
39 37 24 17 12 9 PCI_AD<7>	N5 AD7	VS2*/CVS2	A9 CBUS_VS2 18
39 37 24 17 12 9 PCI_AD<8>	N4 AD8	WE*/CGNT*	D13 CBUS_WE_L 18
39 37 24 17 12 9 PCI_AD<9>	M2 AD9	RDY/IREQ*/CINT*	A6 CBUS_READY 18
39 37 24 17 12 9 PCI_AD<10>	M5 AD10	RESET/CRST*	D8 CBUS_RESET_L 18
39 37 24 17 12 9 PCI_AD<11>	L4 AD11	REG*/CC/BE3*	A8 CBUS_REG_L 18
39 37 24 17 12 9 PCI_AD<12>	N3 AD12	BVD1/CSTSCHG/STSCHG*/RI*	C6 CBUS_BVD1_L 18
39 37 24 17 12 9 PCI_AD<13>	K5 AD13	BVD2/SPKR*/CAUDIO	D6 CBUS_BVD2_L 18
39 37 24 17 12 9 PCI_AD<14>	L5 AD14	INTEGRATED PULL-UP WP/IOIS16*/CCLKRUN*	A5 CBUS_WP_L 18
39 37 24 17 12 9 PCI_AD<15>	M4 AD15	CE2/CAD10*	G13 CBUS_CE2_L 18
39 37 24 17 12 9 PCI_AD<16>	J4 AD16	INPACK/CREQ*	B8 CBUS_INPACK_L 18
39 37 24 17 12 9 PCI_AD<17>	H1 AD17	WAIT/CSERR*	B6 CBUS_WAIT_L 18
39 37 24 17 12 9 PCI_AD<18>	H3 AD18	A0/CAD26	C7 CBUS_ADDR<0> 18
(PCI_AD<19>)	H2 AD19	A1/CAD25	D7 CBUS_ADDR<1> 18
39 37 24 17 12 9 PCI_AD<20>	G2 AD20	A2/CAD24	B7 CBUS_ADDR<2> 18
39 37 24 17 12 PCI_AD<21>	G4 AD21	A3/CAD23	D10 CBUS_ADDR<3> 18
39 37 24 17 12 PCI_AD<22>	F1 AD22	A4/CAD22	B12 CBUS_ADDR<4> 18
39 37 24 17 12 PCI_AD<23>	C3 AD23	A5/CAD21	C8 CBUS_ADDR<5> 18
39 37 24 17 12 9 PCI_AD<24>	F3 AD24	A6/CAD20	C9 CBUS_ADDR<6> 18
39 37 24 17 12 9 PCI_AD<25>	E2 AD25	A7/CAD18	A12 CBUS_ADDR<7> 18
39 37 24 17 12 9 PCI_AD<26>	F4 AD26	A8/CC/BE1*	E11 CBUS_ADDR<8> 18
39 37 24 17 12 9 PCI_AD<27>	B1 AD27	A9/CAD14	F11 CBUS_ADDR<9> 18
39 37 24 17 12 9 PCI_AD<28>	D2 AD28	A10/CAD9	G11 CBUS_ADDR<10> 18
39 37 24 17 12 9 PCI_AD<29>	E4 AD29	A11/CAD12	G12 CBUS_ADDR<11> 18
39 37 24 17 12 9 PCI_AD<30>	D3 AD30	A12/CC/BE2*	D9 CBUS_ADDR<12> 18
39 37 24 17 12 9 PCI_AD<31>	E3 AD31	A13/CPAR	E12 CBUS_ADDR<13> 18
37 24 17 12 PCI_CBE<0>	K6 C/BE0*	A14/CPERR*	D12 CBUS_ADDR<14> 18
37 24 17 12 PCI_CBE<1>	M3 C/BE1*	A15/CIRDY*	C10 CBUS_ADDR<15> 18
37 24 17 12 PCI_CBE<2>	J2 C/BE2*	A16/CCLK	B13 CBUS_ADDR_16_UF
37 24 17 12 PCI_CBE<3>	A1 C/BE3*	A17/CAD16	F10 CBUS_ADDR<17> 18
39 37 24 17 12 PCI_PAR	N1 PAR	A18/RSVD	E13 CBUS_ADDR<18> 18
39 37 24 17 12 PCI_IRDY_L	K1 IRDY	A19/CBLOCK*	A13 CBUS_ADDR<19> 18
39 37 24 17 12 PCI_SERR_L	L2 SERR	A20/CSTOP*	E10 CBUS_ADDR<20> 18
CBUS_PCI_IDSEL	F2 IDSEL	A21/CDEVSEL*	D11 CBUS_ADDR<21> 18
18 17 PCI_PERR_L	K3 PERR	A22/CTRDY*	C12 CBUS_ADDR<22> 18
39 37 24 17 12 PCI_FRAME_L	J1 FRAME	A23/CFRAME*	A10 CBUS_ADDR<23> 18
39 37 24 17 12 PCI_STOP_L	L1 STOP	A24/CAD17	B10 CBUS_ADDR<24> 18
39 37 24 17 12 PCI_TRDY_L	J3 TRDY	A25/CAD19	B9 CBUS_ADDR<25> 18
39 37 24 17 12 PCI_DEVSEL_L	K2 DEVSEL	D0/CAD27	A4 CBUS_DATA<0> 18
CBUS_PCI_RESET_L	G3 PRST	D1/CAD29	C4 CBUS_DATA<1> 18
12 CBUS_PCI_REQ_L	C2 REQ	D2/RSVD	A3 CBUS_DATA<2> 18
12 CBUS_PCI_GNT_L	C1 GNT	D3/CAD0	K11 CBUS_DATA<3> 18
35 12 CLK33M_CBUS	G1 PCLK	D4/CAD1	K12 CBUS_DATA<4> 18
NC M9	SPKROUT	D5/CAD3	J13 CBUS_DATA<5> 18
NC M8	RI_OUT/PME	D6/CAD5	J10 CBUS_DATA<6> 18
18 CBUS_SUSPEND_PU	N10 SUSPEND	D7/CAD7	H12 CBUS_DATA<7> 18
14 CBUS_INT_L	K7 MFUNC0	D8/CAD28	C5 CBUS_DATA<8> 18
18 CBUS_MFUNC1_PD	N9 MFUNC1	D9/CAD30	B4 CBUS_DATA<9> 18
18 CBUS_MFUNC2_PD	L9 MFUNC2	D10/CAD31	B3 CBUS_DATA<10> 18
18 CBUS_MFUNC3_PD	K10 MFUNC3	D11/CAD2	M12 CBUS_DATA<11> 18
18 CBUS_MFUNC4_PD	M10 MFUNC4	D12/CAD4	J11 CBUS_DATA<12> 18
18 CBUS_MFUNC5_PD	N12 MFUNC5	D13/CAD6	K13 CBUS_DATA<13> 18
18 CBUS_MFUNC6_PD	L10 MFUNC6	D14/RSVD	J12 CBUS_DATA<14> 18
	L11 GRST	D15/CAD8	H11 CBUS_DATA<15> 18

R719 22 5% 1/16W MF 402
R723 47 5% 1/16W MF 402 — MAIN_RESET_L 1 29 24 19 17 14
R724 47 5% 1/16W MF 402 — CBUS_ADDR<16> 18
RP1 10K 5% 1/32W 25V SM
5 10 — 6 4 7 3 9 8 2 1
CBUS_MFUNC1_PD 18
CBUS_MFUNC2_PD 18
CBUS_MFUNC3_PD 18
CBUS_MFUNC4_PD 18
CBUS_MFUNC5_PD 18
CBUS_MFUNC6_PD 18
GND
A2 A11 D1 F13 H4 K8 M13 N2

PC CARD/CARDBUS CONNECTOR

CRITICAL
J5 QT500806-L111 M-ST-SM1
84 81

	2	1	CBUS_DATA<3> 18
39 18 CBUS_DET_1_L	4	3	CBUS_DATA<4> 18
18 CBUS_DATA<11>	6	5	CBUS_DATA<5> 18
18 CBUS_DATA<12>	8	7	CBUS_DATA<6> 18
18 CBUS_DATA<13>	10	9	
	12	11	CBUS_DATA<7> 18
18 CBUS_DATA<14>	14	13	CBUS_CE1_L 18
18 CBUS_DATA<15>	16	15	CBUS_ADDR<10> 18
18 CBUS_CE2_L	18	17	CBUS_OE_L 18
18 CBUS_VS1	20	19	
	22	21	CBUS_ADDR<11> 18
18 CBUS_IORD_L	24	23	CBUS_ADDR<9> 18
18 CBUS_IOWR_L	26	25	CBUS_ADDR<8> 18
18 CBUS_ADDR<17>	28	27	CBUS_ADDR<13> 18
18 CBUS_ADDR<18>	30	29	
	32	31	CBUS_ADDR<14> 18
18 CBUS_ADDR<19>	34	33	CBUS_WE_L 18
18 CBUS_ADDR<20>	36	35	CBUS_READY 18
18 CBUS_ADDR<21>	38	37	+VCC_CBUS_SW 18 38
38 18 +VCC_CBUS_SW	40	39	
	42	41	+VPP_CBUS_SW 18 38
38 18 +VPP_CBUS_SW	44	43	CBUS_ADDR<16> 18
18 CBUS_ADDR<22>	46	45	CBUS_ADDR<15> 18
18 CBUS_ADDR<23>	48	47	CBUS_ADDR<12> 18
18 CBUS_ADDR<24>	50	49	
	52	51	CBUS_ADDR<7> 18
18 CBUS_ADDR<25>	54	53	CBUS_ADDR<6> 18
18 CBUS_VS2	56	55	CBUS_ADDR<5> 18
18 CBUS_RESET_L	58	57	CBUS_ADDR<4> 18
18 CBUS_WAIT_L	60	59	
	62	61	CBUS_ADDR<3> 18
18 CBUS_INPACK_L	64	63	CBUS_ADDR<2> 18
18 CBUS_REG_L	66	65	CBUS_ADDR<1> 18
18 CBUS_BVD2_L	68	67	CBUS_ADDR<0> 18
18 CBUS_BVD1_L	70	69	
	72	71	CBUS_DATA<0> 18
18 CBUS_DATA<8>	74	73	CBUS_DATA<1> 18
18 CBUS_DATA<9>	76	75	CBUS_DATA<2> 18
18 CBUS_DATA<10>	78	77	CBUS_WP_L 18
39 18 CBUS_DET_2_L	80	79	
	83	82	

TI REFERENCE SCHEMATIC DID NOT HAVE BULK ON +VCC_CBUS_SW
C796 2.2uF 20% 10V CERM 805
C800 2.2uF 20% 10V CERM 805

CARDBUS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	01
SCALE: NONE	SHT 18 OF 44	

SIL1162 DVI-Compliant Transmitter

Ext. TMDS source termination

M11 AGP INTERFACE

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	01
SCALE: NONE	SHT 19 OF 44	

SPREAD SPECTRUM SUPPORT
S0=1;S1=M => -1.5% DOWN-SPREAD

27M OSC

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0318	197S0048		G1	Alt. for Siward Part

Int.TMDS Termination

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN
CMF LINE SHOULD BE ROUTED AS 4MIL SURFACE
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS

GPU_TMDS_CLK_CMF
GPU_TMDS_D0_CMF
GPU_TMDS_D1_CMF
GPU_TMDS_D2_CMF

Place all TMDS 10 ohms close to GPU

GPU VCORE – 1.2V

(PUT ALL CAPs BELOW ATI ASIC)

M10 Power Shut down Sequencing

GPU VCORE SUPPLY

WHEN VCORE_CNTL HIGH => 1.2V
1.2V = 0.8V * (1 + R329 / (R328//R330))

WHEN VCORE_CNTL LOW => 1.0V
1.0V = 0.8V * (1 + R329 / R330)

M11 CORE PWR/LVDS/TMDS

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APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6570 | REV. 01
SCALE NONE | SHT 20 OF 44

GPU PLL - 1.8V

AGP 4X I/O - 1.5V

MEMORY I/O

MEMORY CORE - 2.5V

LVDS PLL - 1.8V

1.8V DVO POWER (EXT.TMDS)

MEMORY PLL - 1.8V

LVDS - 2.5V

3.3V IO SUPPLY

(Max Current varies, depends on usage)

LVDS/TMDS - 1.8V

1.5V

1.8V

1.8V

2.5V

2.5V

3.3V

GPU POWER SOURCES - 1.5V, 1.8V, 2.5V & 3.3V

ATI_64MB
CRITICAL
U47
RAGE MOBILITY
M11-CSP64
64MB
BGA
(4 OF 6)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S1058	1	IC,ATI,M11-CSP128,GRAPHICTLR,667BGA	U47	CRITICAL	ATI_128MB

M11 POWER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	01
SCALE: NONE	SHT 21 OF 44	

EXTERNAL VIDEO (DVI) INTERFACE

VGA SYNC BUFFERS

U40 74AHC1G32 SM
U39 74AHC1G32 SM
L38 FERR-60-OHM-0.1A 0402 OMIT
L36 FERR-60-OHM-0.1A 0402 OMIT
+3V_MAIN
ATI_VSYNC
ATI_VSYNC_BUF
VGA_VSYNC
ATI_HSYNC
ATI_HSYNC_BUF
VGA_HSYNC

PLACE L1002 & L1003 CLOSE TO DVI CONNECTOR

TMDS FILTERING
PLACE CLOSE TO CONNECTOR

L45 90-OHM-300mA 2012H CRITICAL
L47 90-OHM-300mA 2012H CRITICAL
L46 90-OHM-300mA 2012H CRITICAL
TMDS_DN<0>
TMDS_DP<0>
TMDS_CONN_DN<0>
TMDS_CONN_DP<0>
TMDS_DN<2>
TMDS_DP<2>
TMDS_CONN_DN<2>
TMDS_CONN_DP<2>
TMDS_DN<1>
TMDS_DP<1>
TMDS_CONN_DN<1>
TMDS_CONN_DP<1>

L37 370-OHM SM
TMDS_CLKP
TMDS_CLKN
TMDS_CONN_CLKP
TMDS_CONN_CLKN

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

L50 0.068uH SM
L49 0.068uH SM
L44 0.068uH SM
L43 0.068uH SM
L41 0.068uH SM
L40 0.068uH SM
GPU_B
GPU_B_FILTR
GPU_G
GPU_G_FILTR
GPU_R
GPU_R_FILTR
VGA_B
VGA_G
VGA_R
C642 4.7pF 5% 50V CERM 402
C641 3.3pF 0.25pF 50V CERM 402
C635 4.7pF 5% 50V CERM 402
C634 3.3pF 0.25pF 50V CERM 402
C632 4.7pF 5% 50V CERM 402
C631 3.3pF 0.25pF 50V CERM 402
R462 75 1% 1/16W MF 402
R458 75 1% 1/16W MF 402
R456 75 1% 1/16W MF 402

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)

+5V_SLEEP
F2 0.5AMP-13.2V CRITICAL SM
+5V_DDC_SLEEP_UF
L42 400-OHM-EMI SM-1
+5V_DDC_SLEEP
Isolation required for DVI power switch
D19 MBR0530 SM
DDC_CLK_ISO
R476 4.7K 5% 1/16W MF 402
R478 4.7K 5% 1/16W MF 402
R479 100 5% 1/16W MF 402
C654 100pF 5% 25V CERM 201
C655 100pF 5% 25V CERM 201
C667 0.01uF 10% 50V CERM 603
C653 100pF 5% 25V CERM 201
R464 0 5% 1/16W MF 402
PLACE NEAR C5A & C5B
R463 0 5% 1/16W MF 402
PLACE NEAR 3, 11 & 19
CHGND1
CHGND2

J22 QH1112 F-RT-TH CRITICAL
CHGND
TMDS_CONN_DN<2>
TMDS_CONN_DP<2>
TMDS_CONN_DN<1>
TMDS_CONN_DP<1>
(TMDS_DN<2>)
(TMDS_DP<2>)
(TMDS_DN<1>)
(TMDS_DP<1>)
(TMDS_DN<0>)
(TMDS_DP<0>)
(TMDS_DN<3>)
(TMDS_DP<3>)
(+5V_DDC_SLEEP)
DVI_DDC_CLK_UF
DVI_DDC_DATA_UF
VGA_VSYNC
DVI_HPD_UF
VGA_R
VGA_G
VGA_B
TMDS_CONN_CLKP
TMDS_CONN_CLKN

3V LEVEL SHIFTERS

+3V_SLEEP
Q39 2N7002DW SOT-363
Q40 2N7002DW SOT-363
R480 10K 5% 1/16W MF 402
R474 10K 5% 1/16W MF 402
R481 100K 5% 1/16W MF 402
DVI_DDC_CLK
DVI_DDC_DATA
DVI_HPD
GPU_DVI_DDC_CLK
GPU_DVI_DDC_DATA
GPU_HPD
NOTE: Pulldown for DVI_HPD provided by DVI power switch interface

DVI POWER SWITCH

Power key detect path when system is shutdown or asleep.. DDC_CLK is isolated from NV17M DURING SHUTDOWN. WHEN power key on remote device is pressed, 5V will be driven on DDC_CLK. since host rails will be low, TP0610 will turn on, driving SOFT_PWR_ON_L low. As host rails rise, TP0610 will turn off, as will remote device path to DDC_CLK. Isolation will be disabled as well.

Q38 TP0610 SM
DVI_DDC_CLK_UF
DVI_TURN_ON
R473 680 5% 1/16W MF 402
DVI_TURN_ON_ILIM
R460 10K 5% 1/16W MF 402
R459 330 5% 1/16W MF 402
Pulldown prevents 3904 from turning on when DVI monitor has active, self-powered DDC clock pullup.
DVI_TURN_ON_BASE
Q35 MMDT3904 SOT-363
SOFT_PWR_ON_L

Power key detect path when system is running, HPD normally driven to 3.3v. When power key on remote device pressed,1/16W HPD will be driven to 5V. COMPARATOR ENABLED BY NV17M GPIO.

R485 68.1K 1% 1/16W MF 402
C668 0.1uF 10% 16V CERM 402
U42 LMC7211 SM
R472 10K 1% 1/16W MF 402
R484 100K 1% 1/16W MF 402
R482 10K 1% 1/16W MF 402
R483 470K 5% 1/16W MF 402
R475 10K 5% 1/16W MF 402
R470 330 5% 1/16W MF 402
HPD_4V_REF
DVI_HPD_UF
DVI_HPD_DIV
HPD_REF_EN_L
HPD_PWR_SNS_EN
HPD_PWR_SW_BASE
HPD_PWR_SW
Q40 2N7002DW SOT-363
Q35 MMDT3904 SOT-363

LCD INTERFACE
LVDS INTERFACE

LCD POWER SWITCH

+3V_MAIN
R347 100K 5% 1/16W MF 402
C474 2200pF 5% 50V CERM 603
R354 100K 5% 1/16W MF 402
LCD_PWREN_L
LCD_DIGON_L
TSOP SI3443DV Q29
Q28 2N7002 SM
FP_PWR_EN
+3V_SLEEP
+3V_LCD_SW
L27 FERR-250-OHM SM
+3V_LCD
(LVDS DDC POWER)
C548 0.001uF 20% 50V CERM 402
C503 0.001uF 20% 50V CERM 402
C701 0.001uF 20% 50V CERM 402
C549 0.001uF 20% 50V CERM 402
R543 100K 5% 1/16W MF 402
R544 100K 5% 1/16W MF 402
J14 G-501973 F-RT-SM CRITICAL
LVDS_DDC_CLK
LVDS_DDC_DATA
LVDS_L0N
LVDS_L0P
LVDS_L1N
LVDS_L1P
LVDS_L2N
LVDS_L2P
CLKLVDS_LN
CLKLVDS_LP
LVDS_U0N
LVDS_U0P
LVDS_U1N
LVDS_U1P
LVDS_U2N
LVDS_U2P
CLKLVDS_UN
CLKLVDS_UP
100K pull-ups are for no-panel case (development) Panel has 2K pull-ups
NO STUFF
C702 0.001uF 10% 50V CERM 402
CHGND4

INVERTER INTERFACE

+PBUS
L73 FERR-1K-OHM-EMI SM
+14V_INV
+5V_MAIN
Q76 FDG6324L SC70-6
+5V_INV_UF_SW
L74 400-OHM-EMI SM-1
R750 100K 5% 1/16W MF 402
FP_PWR_EN
C813 10uF 20% 6.3V CERM 805
C812 0.001uF 10% 50V CERM 402
+5V_INV_SW
J4 SM-2MT CRITICAL
C815 0.001uF 10% 50V CERM 402
L72 400-OHM-EMI SM-1
BRIGHT_PWM
INV_GND
+3V_MAIN
C22 0.1uF 10% 16V CERM 402
C816 0.001uF 10% 50V CERM 402
C19 0.001uF 10% 50V CERM 402
L1 FERR-250-OHM SM
CHGND3
INV_ON_PWM
U2 NC7S32 SC70
BRIGHT_PWM_UF
INVERTER EXPECTS ACTIVE HIGH SIGNAL

S-VIDEO/COMP OUT INTERFACE

Place GND shorts at graphics controller

XW15 SM
XW14 SM
GPU_TV_GND1
GPU_TV_GND2
L54 FERR-10-OHM-500MA SM
L56 FERR-10-OHM-500MA SM
TV_GND1
TV_GND2
L53 3.3uH 0603
L57 3.3uH 0603
L55 3.3uH 0603
GPU_Y
GPU_C
GPU_COMP
C657 0.01uF 10% 50V CERM 603
C663 560pF 10% 50V CERM 402
C656 560pF 10% 50V CERM 402
C661 560pF 10% 50V CERM 402
C660 560pF 10% 50V CERM 402
C664 560pF 10% 50V CERM 402
C658 560pF 10% 50V CERM 402
C659 0.01uF 10% 50V CERM 603
J21 MINIDIN RT-TH MH11773-WMR8A CRITICAL
TV_C
TV_Y
TV_COMP
CHGND1

Place GND shorts at graphics controller

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S1331	2	DISCRETE,RES,33OHM,0402	L36,L38		VGA_BUFFER_RES

R753 0 5% 1/16W MF 402
C819 0.01uF 20% 50V CERM 603
CHGND3

VIDEO CONNECTORS

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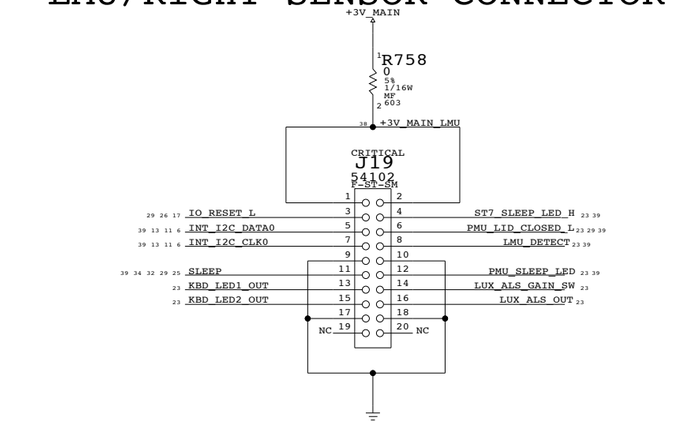
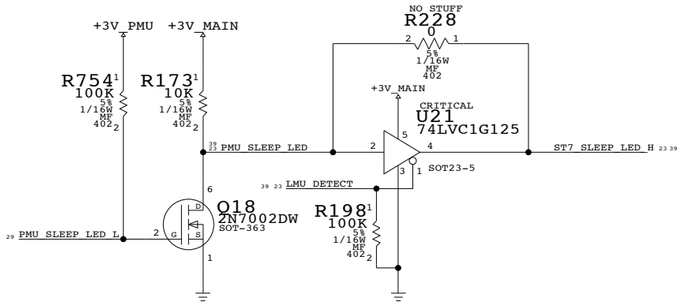
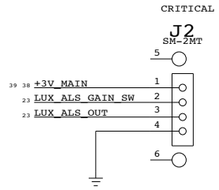
D	051-6570	01
SCALE: NONE	SHT: 22 44	

LMU/RIGHT SENSOR CONNECTOR

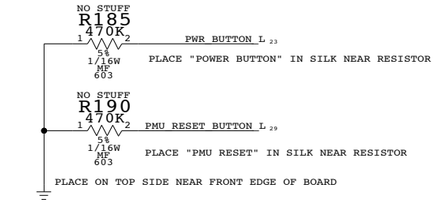




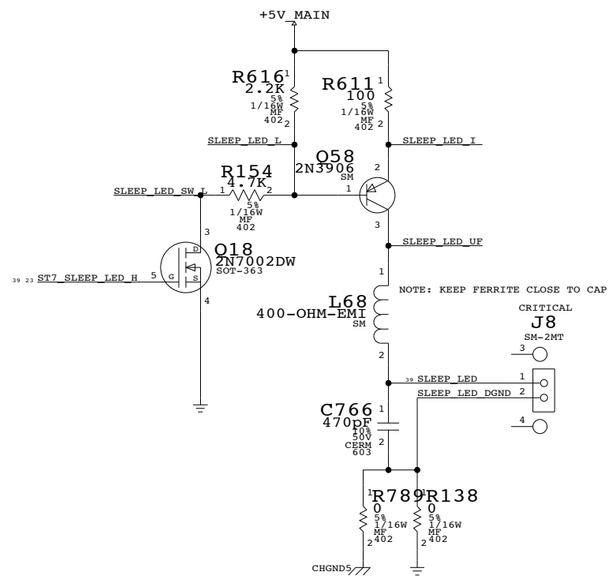
LEFT LIGHT SENSOR CONNECTOR



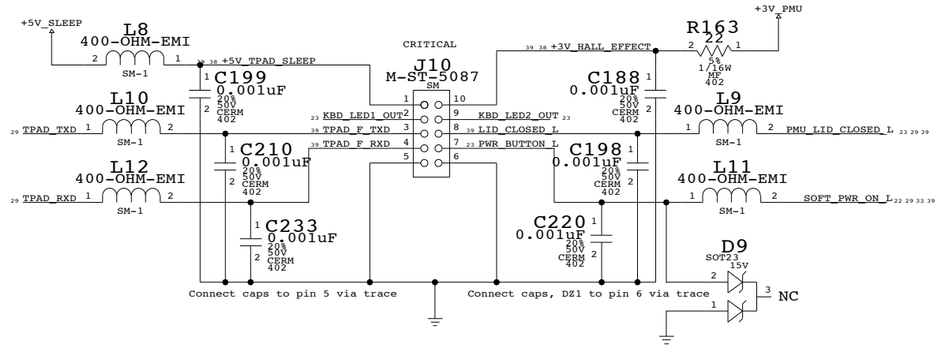
DEBUG HELPERS



SLEEP LED

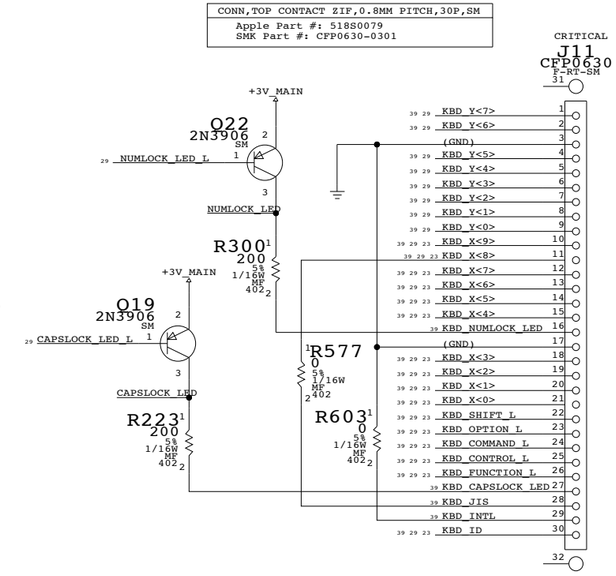


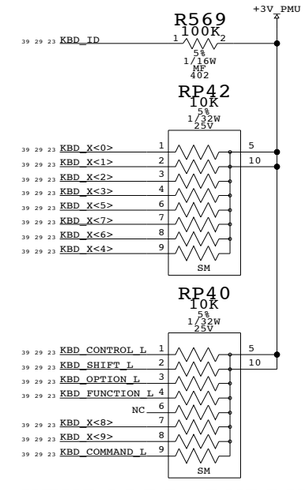
TRACKPAD/PWR BTN CONN



TOP CONTACT ZIF KEYBOARD CONN

CONN,TOP CONTACT ZIF,0.8MM PITCH,30P,SM
Apple Part #: 518S0079
SMK Part #: CFP0630-0301





KEYBOARD PULLUPS

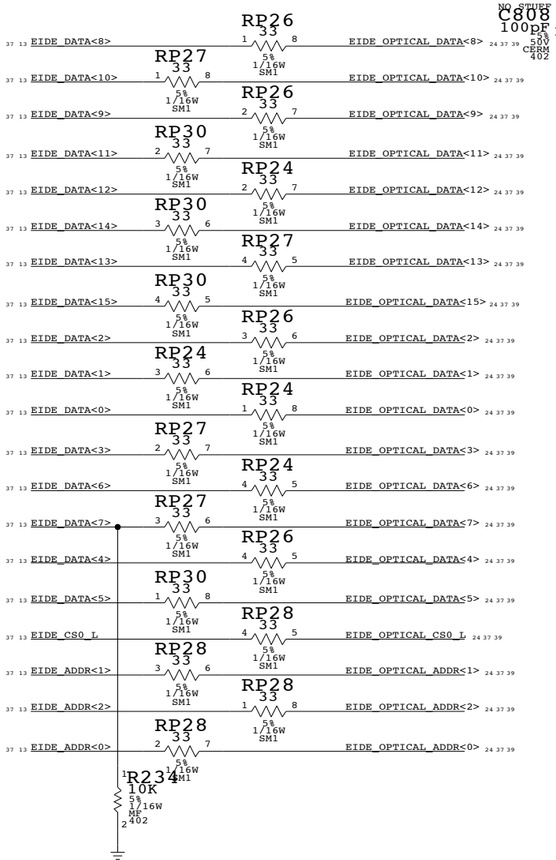
KEYBOARD/TPAD/SLEEP LED

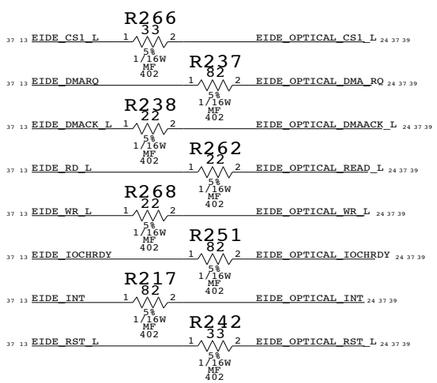
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	01
SCALE: NONE		SHT 23 OF 44

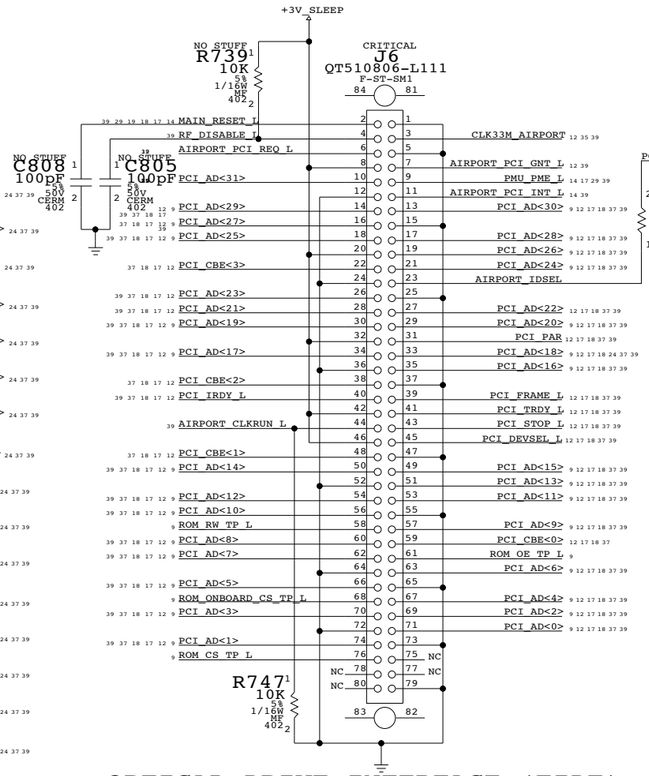
EIDE SERIES TERMINATION

PLACE TERMINATORS NEAR INTREPID

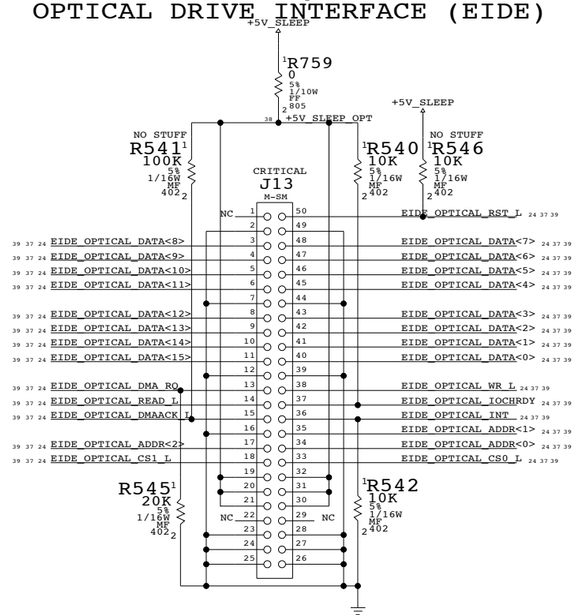




WIRELESS INTERFACE

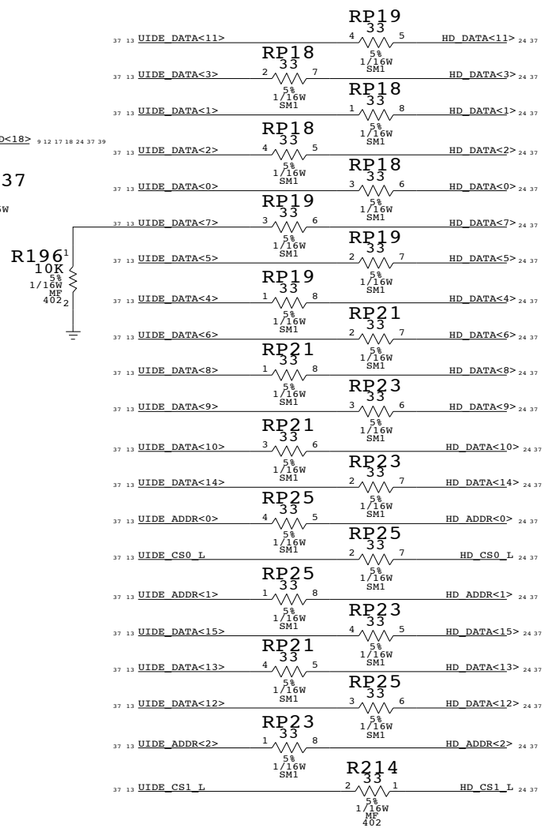


OPTICAL DRIVE INTERFACE (EIDE)

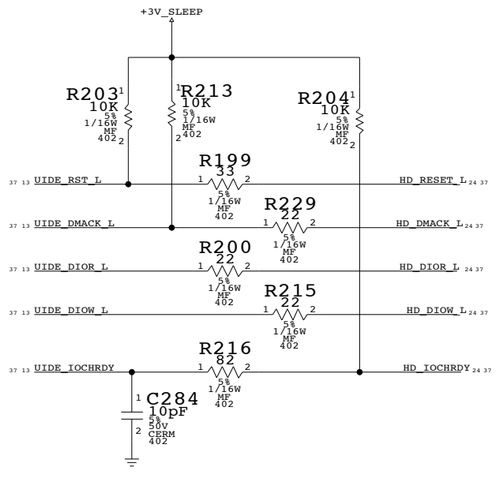


HARD DRIVE INTERFACE (UATA100)

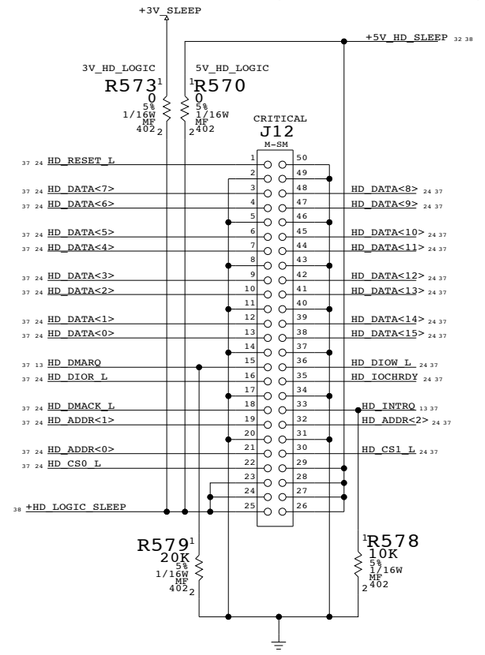
PLACE SERIES R CLOSE TO INTERPID



PLACE PULLUP RESISTORS CLOSE TO INTREPID



IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V



ANY SEQUENCING REQUIREMENT BETWEEN +5V_HD_SLEEP AND +3V_SLEEP

INTERNAL I/O CONNECTORS

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6570 | REV. 01

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LEFT I/O & AUDIO BOARD (LIO)

CRITICAL
J3
QT500406-L111
M-ST-SM1

+5V_MAIN
+3V_MAIN
Place it near J3
C848 150uF 20% 6.3V TANT SMD-1

ADAPTER_DET
CHARGE_LED_L
NEC_LUSB_PPON
NEC_LUSB_OCI_UF
BT_USB_DM
BT_USB_DP
INT_I2S0_SND_MCLK
INT_I2S0_SND_LRCLK
INT_I2S0_SND_TO_DAC
SND_HP_SENSE_L
SND_LIN_SENSE_L
NEC_USB_DAM
NEC_USB_DAP
SLEEP
INT_I2S0_SND_SCLK
INT_I2S0_SND_FROM_ADC
SND_HW_RESET_L
INT_I2C_CLK2
INT_I2C_DATA2
SND_HP_MUTE_LO
SND_AMP_MUTE
+3V_MAIN_AUD
+5V_MAIN_AUD
AUD_GND

NO STUFF C818 0.001uF 20% 50V CERM 402
NO STUFF C817 0.001uF 20% 50V CERM 402
C828 0.1uF 20% 10V CERM 402
C829 0.1uF 20% 10V CERM 402
OMIT XW30 SM

+5V_MAIN
R751 100K 5% 1/16W MF 402
SND_AMP_MUTE
Q77 2N7002DW SOT-363
SND_AMP_MUTE_L
R752 100K 5% 1/16W MF 402
SND_AMP_MUTE_CTRL
Q77 2N7002DW SOT-363
INT_PU_RESET_L

PREVENTS POWER-ON POP AND
GENERATES ACTIVE HIGH SPKR MUTE

+3V_MAIN
R768 100K 5% 1/16W MF 402
R769 100K 5% 1/16W MF 402
SND_HP_MUTE_LO
Q78 2N7002DW SOT-363
SND_HP_MUTE
Q78 2N7002DW SOT-363
SND_HP_MUTE_L
R770 100K 5% 1/16W MF 402
SND_AMP_MUTE_CTRL

PREVENTS POWER-ON POP AND
PROPAGATES ACTIVE LOW HP MUTE

PLACE CLOSE TO CPU
MAIN1

THERM1_M_DP
Q59 2N3904 SM
THERM1_M_DM

KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

R703 0 5% 1/16W MF 402 THERM1_M_DP
R704 0 5% 1/16W MF 402 THERM1_M_DM

PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY
MAIN2

THERM2_M_DP
Q46 2N3904 SM
THERM2_M_DM

R686 0 5% 1/16W MF 402 THERM2_M_DP
R687 0 5% 1/16W MF 402 THERM2_M_DM

PLACE UNDERNEATH UPPER RAM
ALTERNATE1

THERM1_A_DP
Q61 2N3904 SM
THERM1_A_DM

KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

NO STUFF R701 0 5% 1/16W MF 402 THERM1_A_DP
NO STUFF R702 0 5% 1/16W MF 402 THERM1_A_DM
NO STUFF R688 0 5% 1/16W MF 402 THERM2_A_DP
NO STUFF R689 0 5% 1/16W MF 402 THERM2_A_DM

PLACE CLOSE TO BATTERY CHARGER/VCORE
ALTERNATE2

THERM2_A_DP
Q67 2N3904 SM
THERM2_A_DM

NO STUFF R700 0 5% 1/16W MF 402 CPU_THERM_DP
NO STUFF R705 0 5% 1/16W MF 402 CPU_THERM_DM
NO STUFF R659 0 5% 1/16W MF 402 GPU_THERM_DP
NO STUFF R661 0 5% 1/16W MF 402 GPU_THERM_DM

USB MODEM/SOFT MODEM

+5V_MAIN
PLACE NEAR CONNECTOR PINS 15
C698 10uF 20% 6.3V CERM 805
NO STUFF C696 0.1uF 20% 10V CERM 402

+3V_MAIN
PLACE NEAR CONNECTOR PINS 16
C689 10uF 20% 6.3V CERM 805
NO STUFF C692 0.1uF 20% 10V CERM 402

+3V_MAIN
USB_MODEM R530 10K 5% 1/16W MF 402
+5V_MAIN

CRITICAL
J15
QT500166-L010
M-ST-SM1

INT_MOD_DTO
INT_MOD_CLKOUT
COMM_SHUTDOWN
COMM_RESET_L
INT_I2C_DATA2
INT_I2C_CLK2
INT_MOD_SYNC
INT_MOD_DTI
INT_MOD_BITCLK
MODEM_USB_DM
MODEM_USB_DP
COMM_RING_DET_L
+3V_MAIN

MODEM I2C ADDR ASSIGNED VIA FLEX CABLE

RIGHT USB BOARD

+5V_MAIN
CRITICAL
J17
QT500166-L010
M-ST-SM1
NEC_USB_DBM
NEC_USB_DBP
NEC_RUSB_OCI_UF
NEC_RUSB_PPON

SERIAL DEBUG INTERFACE

+5V_MAIN
CRITICAL
J28
M-ST-5087
SM
COMM_TXD_L
COMM_TRXC
COMM_GPIO_L
COMM_DTR_L
COMM_RTS_L
COMM_RXD

FAN INTERFACE

FAN CONTROLLER

+3V_MAIN
R806 10 5% 1/16W MF 402
ADT7460_VCC
C849 1uF 10% 6.3V CERM 603
C763 0.1uF 20% 10V CERM 402

U53
ADT7460 QSOP
CRITICAL
VCC
+2.5V/ SMBALERT#
SDA
SCL
D1+
D1-
D2+
D2-
GND
PWM1/ XTO
TACH1
PWM2/ SMBALERT#
TACH2
PWM3/ ADR ENABLE#
TACH3
TACH4/ ADR SELECT/ THERM#

ADT7460_VCORE_MON
INT_I2C_DATA1
INT_I2C_CLK1
THERM1_DP
THERM1_DM
THERM2_DP
THERM2_DM
C868 1000pF 10% 25V X7R 402
C869 1000pF 10% 25V X7R 402

R633 10K 5% 1/16W MF 402
R749 10K 5% 1/16W MF 402
R774 10K 5% 1/16W MF 402
R454 10K 5% 1/16W MF 402
R773 10K 5% 1/16W MF 402
+3V_SLEEP

FAN1_PWM_L
FAN1_TACH
FAN2_PWM_L
FAN2_TACH
ADT7460_ADR_ENABLE_L
ADT7460_TACH3_TP
ADT7460_THERM_L

+3V_PMU_AVCC
R817 100K 5% 1/16W MF 402
THERM_L_OC

+3V_MAIN
R808 100K 5% 1/16W MF 402
THERM_INV
Q83 2N7002DW SOT-363
R807 100K 5% 1/16W MF 402
Q83 2N7002DW SOT-363
C850 0.1uF 20% 10V CERM 402
ADT7460_THERM_L

CPU FAN

+5V_SLEEP
NO STUFF R771 10K 5% 1/16W MF 402
+5V_SLEEP
R547 0 5% 1/10W CRITICAL J1 SM04B-SSR M-RT-SM 805
+FAN_PWR
FAN1_TACH
FAN1_PWM
Q79 2N7002DW SOT-363
FAN1_PWM_L
C669 4.7uF 20% 6.3V CERM 805

GPU FAN

+5V_SLEEP
NO STUFF R772 10K 5% 1/16W MF 402
CRITICAL J18 SM04B-SSR M-RT-SM
+FAN_PWR
FAN2_TACH
FAN2_PWM
Q79 2N7002DW SOT-363
FAN2_PWM_L
C814 4.7uF 20% 6.3V CERM 805

FAN/MODEM/SOUND/BACKUP BATT.

APPLE COMPUTER INC.

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Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

+3V_MAIN

C680 10uF 20% 6.3V CERM 805

NO STUFF R513 0 5% 1/16W MF 402

3405_MODE

R507 0 5% 1/16W MF 402

U45 LTC3405 SOT23-6 — VIN, RUN, MODE, SW, VFB, GND

LTC3405_SW

CRITICAL L60 3.3uH SM1

R506 665K 1% 1/16W MF 402 R2A

C675 22PF 5% 50V CERM 402

R504 49.9K 1% 1/16W MF 402 R2B

3405_VFB

R503 182K 1% 1/16W MF 402 R1

C674 10uF 20% 6.3V CERM 805

+1_0V_MARVELL

VOUT = 0.8V*(1+R2EQV/R1)
R2EQV = R2A||R2B

PLACE ALL SERIES RES CLOSE TO PHY

R423 0 5% 1/16W MF 402 — CLKENET_LINK_TX ↔ CLKENET_PHY_TX

R421 0 5% 1/16W MF 402 — CLKENET_LINK_RX ↔ CLKENET_PHY_RX

R445 0 5% 1/16W MF 402 — CLKENET_LINK_GBE_REF ↔ CLKENET_PHY_GBE_REF

NO STUFF C851 10pF 5% 50V CERM 402

C852 10pF 5% 50V CERM 402

Keep C851 & C852 Stubs short

CRITICAL U43 88E1111 BCC

TX_CLK, RX_CLK, 125CLK, TXD0–TXD7, TX_EN, TX_ER, GTX_CLK, RXD0–RXD7, RX_DV, RX_ER, CRS, COL, MDC, MDIO, INT-/INT+, RESET, COMA, S_IN+, S_IN-, S_OUT+, S_OUT-, S_CLK+, S_CLK-, HSDAC+, HSDAC-, XTAL1, XTAL2, VSSC

CTRL10, DVDD, VDDO, VDDOH, VDDOX, AVDD, GND

MDI0+, MDI0-, MDI1+, MDI1-, MDI2+, MDI2-, MDI3+, MDI3-

LED_LINK10, LED_LINK100, LED_LINK1000, LED_DUPLEX, LED_RX, LED_TX

CONFIG0 (000), CONFIG1 (000), CONFIG2 (111), CONFIG3 (110), CONFIG4 (111), CONFIG5 (101), CONFIG6 (000)

TDI, TDO, TCK, TMS, TRST, RSET, SEL_OSC, SEL_2.5V

C594 C601 C608 C619 C603 C599 — 0.1uF / 0.01uF 20% 16V CERM 402

PLACE CAPS (IN ORDER) ON PINS 1, 6, 10/15, 57/62, 67/71, 85

C597 C612 C623 C600 C598 C595 — 0.1uF / 0.01uF 20% 16V CERM 402; C595 10uF 20% 6.3V CERM 805

PLACE CAPS (IN ORDER) ON PINS 5, 21/26, 48/52, 66/72, 88, 96

+2_5V_MARVELL

L35 FERR-EMI-600-OHM SM

+2_5V_MARVELL_AVDD

C614 C616 C618 C602 C592 — 0.1uF / 0.01uF / 10uF 20% 16V CERM 402

PLACE CAPS (IN ORDER) ON PINS 32/35, 36/40, 45 & 78

R442 0 5% 1/16W MF 603

C646 C648 C645 C647 — 0.1uF 20% 10V CERM 402

PLACE CAPS AT CONNECTOR PINS 5 & 6

CRITICAL J23 MJ-R0016 F-RT-TH

PRIMARY: 13, 11, 5 ENET_CTAP, 6 ENET_CTAP, 1 MDI_0+, 2 MDI_0-, 3 MDI_1+, 4 MDI_1-, 7 MDI_2+, 8 MDI_2-, 9 MDI_3+, 10 MDI_3-, 12, 14

RJ45 CHIP SIDE

CHGND1

1CT:1CT, 75 OHM

SECONDARY: J1 J2 J3 J4 J5 J6 J7 J8

RJ45 CABLE SIDE

SHIELD 1000PF, 2000V

R433 R435 R437 R439 — 49.9 1% 1/16W MF 402

R434 R436 R438 R440 — 49.9 1% 1/16W MF 402

MDI0_PD, MDI1_PD, MDI2_PD, MDI3_PD

C622 C613 C615 C617 — 0.01uF 20% 16V CERM 402

PLACE RESISTORS CLOSE TO PHY

SEE CONFIG TABLES (BELOW)

PLACES PHY IN "COMA" MODE WHEN ASLEEP ON BATTERY (SAVES POWER)

Q32 2N7002DW SOT-363

Q32 2N7002DW SOT-363

D15 1N914 SOT23

R431 10K 5% 1/16W MF 402

R430 10K 5% 1/16W MF 402

R432 1.5K 5% 1/16W MF 402

R422 1K 5% 1/16W MF 402

C611 2.2uF 20% 10V CERM 805

NO STUFF R425 20K 5% 1/16W MF 402

R441 0 5% 1/16W MF 402

CRITICAL Y5 SM-3 25.0000M

C604 27PF 5% 50V CERM 402

C624 27PF 5% 50V CERM 402

PUT CRYSTAL CIRCUIT CLOSE TO PHY

Y6 LOAD CAPACITANCE IS 16PF

NO STUFF R424 49.9 1% 1/16W MF 402

NO STUFF R429 49.9 1% 1/16W MF 402

R428 10K 5% 1/16W MF 402

R427 4.99K 1% 1/16W MF 402

CONFIG DEFINITIONS	
PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS			
PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

MARVELL 88E1111

10/100/1000 ETHERNET

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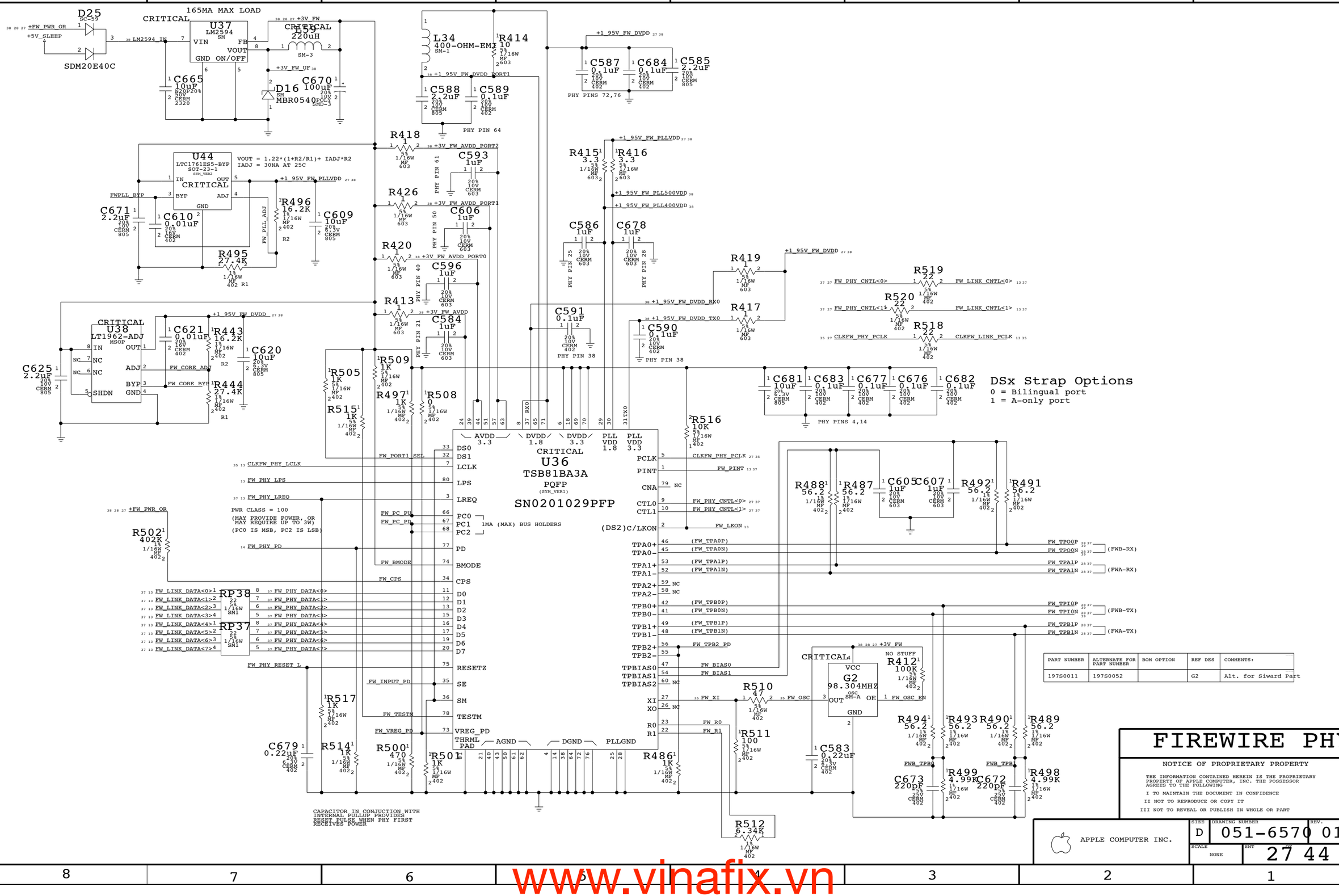

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0011	197S0052		G2	Alt. for Siward Part

FIREWIRE PHY

APPLE COMPUTER INC.

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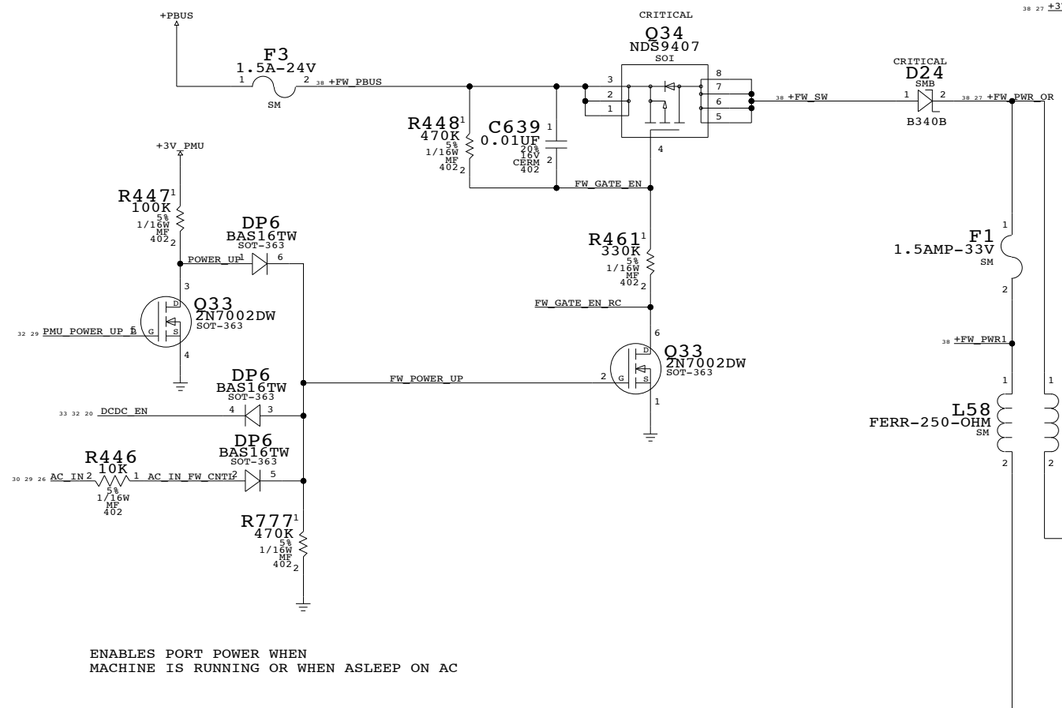
PORT POWER SWITCH

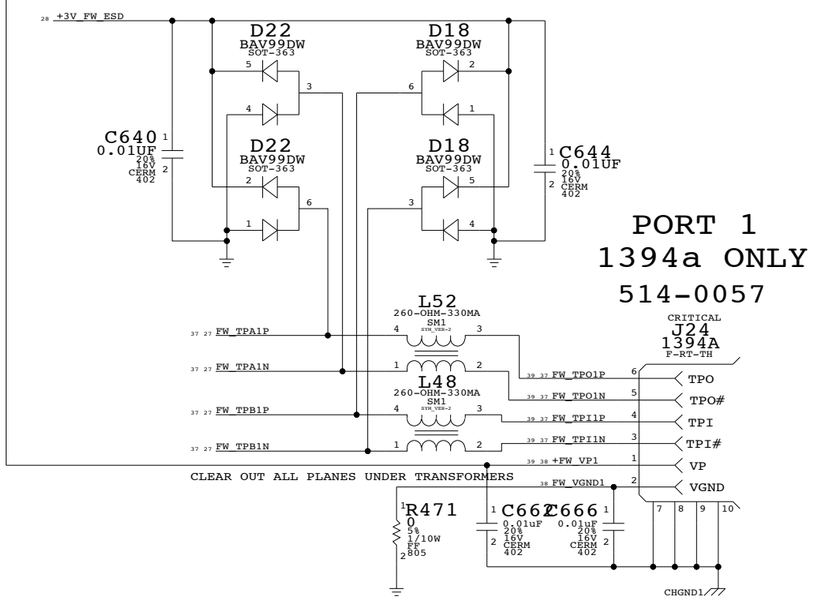


ENABLES PORT POWER WHEN
MACHINE IS RUNNING OR WHEN ASLEEP ON AC

PORT 0
1394a/b
(BILINGUAL)
514S0058

AREF NEEDS TO BE ISOLATED FROM ALL LOCAL GROUNDS PER 1394B SPEC SO WHEN A BILINGUAL DEVICE IS PLUGGED TO A BETA-ONLY DEVICE, THERE'S NO DC PATH BETWEEN THEM (TO AVOID GROUND OFFSET ISSUE)

BREF SHOULD BE HARD CONNECTED TO LOGIC GROUND FOR SPEED SIGNALING AND CONNECTION DETECTION CURRENTS PER 1394B V1.33



CLEAR OUT ALL PLANES UNDER TRANSFORMERS

PORT 1
1394a ONLY
514-0057

FIREWIRE PORTS

APPLE COMPUTER INC.

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D	051-6570	01
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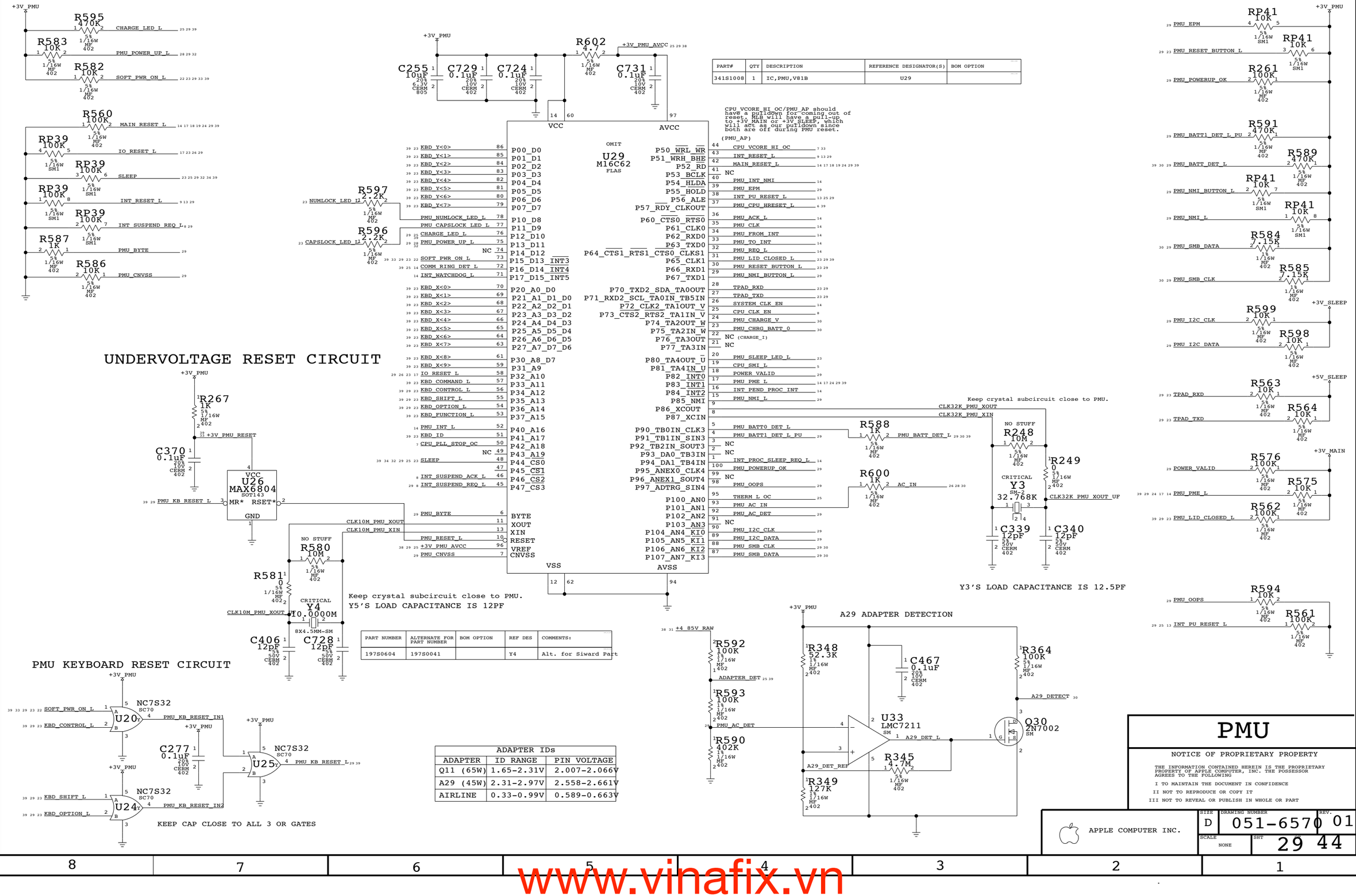

DC POWER INPUT

(POWER JACK, ETC. ON SEPARATE BOARD)

CRITICAL
J27
87438-0433
M-RT-SM

+ADAPTER

C35 0.1uF 10% 50V X7R 603

DC INRUSH LIMITER

Q68 SI4435DY SOI

R21 330K 5% 1/16W MF 402
C11 0.1uF 20% 50V CERM 805
AC_ENABLE_GATE
GATE

R51 20K 1% 1/16W MF 402
+3V_PMU
R40 97.6K 1% 1/16W MF 402
R16 100K 1% 1/16W MF 402
C801 0.01uF 20% 16V CERM 402
R15 10K 5% 1/16W MF 402
R29 470K 5% 1/16W MF 402
AC_ENABLE_L
38 31 1V20_REF
U1 LMC7211 SM
AC_DIV
AC_IN 26 28 29 30
R41 1M 5% 1/16W MF 402
R42 10K 1% 1/16W MF 402
R30 57.6K 1% 1/16W MF 402
AC_IN_L 30
Q1 2N7002DW SOT-363
R22 470K 5% 1/16W MF 402

GREATER THAN 13.1V DETECT

BACKFEED PROTECTION

38 +ADAPTER_SW

Q69 SI4435DY SOI

+ADAPTER_SENSE
BKFD_PROT_GATE
R732 47K 5% 1/16W MF 402
C803 0.1uF 20% 25V CERM 402
R734 68K 5% 1/16W MF 402
BKFD_PROT_EN_L
30 29 28 26 AC_IN
Q9 2N7002DW SOT-363

CRITICAL
U3 MAX4172 TSSOP
RS+ RS- PG OUT GND V+
NC NC NC NC
MAX4172_OUT
CRITICAL
R77 2.21K 0.1% 1/16W MF 603
C36 0.01uF 20% 50V CERM 603
+24V_PBUS

Place close to RS-
C826 0.01uF 20% 50V CERM 603

PLACE U24 NEXT TO R382

CRITICAL
R61 0.025 1% 1W MF 2512
R82 4.7 5% 1/16W MF 402
R87 4.7 5% 1/16W MF 402
1772_CSSP
1772_CSSN

R57 100K 1% 1/16W MF 402
D4 1N914 SOT23
R49 12.7K 1% 1/16W MF 402
C67 1uF 20% 50V CERM 1210
C71 0.47uF 20% 50V CERM 1206
C95 0.47uF 20% 50V CERM 1206

+PBUS CURRENT LIMIT

R728 1K 1% 1/16W MF 402
IAC_RC_COMP
C798 0.1uF 20% 10V CERM 402
+3V_PMU
C794 0.1uF 20% 10V CERM 402
CRITICAL
R745 42.2K 1% 1/16W MF 603
IAC_FB
U55 SMC7111 SOT23-5
R727 10K 1% 1/16W MF 402
MAX4172_OUT
DP1 BAS16TW SOT-363
R119 150 1% 1/16W MF 402
1625_COMP
LTC1625_ITH
ADAPTER_I_REG

PLACE R383 CLOSE TO LTC1625
ROUTE LTC1625_ITH CAREFULLY

CRITICAL
R736 42.2K 0.1% 1/16W PF 603
CURRENT_THRESHOLD
CRITICAL
R738 82.5K 0.1% 1/16W PF 603
+3V_PMU
CRITICAL
R742 51.1K 0.1% 1/16W PF 603
A29_CURRENT_ADJ
R744 100K 5% 1/16W MF 402
AC_GTR_18V
OVER_18V_ADJ
Q2 2N7002DW SOT-363
Q74 2N7002DW SOT-363
Q74 2N7002DW SOT-363
30 29 A29_DETECT
30 1772_ACOK_L
C809 1uF 20% 10V CERM 603

BATTERY SWITCH-OVER CIRCUIT

+PBUS
F4 5AMP-125V SM-2
F5 5AMP-125V SM-2
+24V_PBUS
38 +BATT_24V_FUSE
38 +BATT_14V_FUSE
CRITICAL
Q6 SI4435DY SOI
CRITICAL
Q7 SUD45P03 TO-252
R716 47K 5% 1/16W MF 402
R710 47K 5% 1/16W MF 402
BATT_24V_GATE
BATT_14V_GATE
R717 10K 5% 1/16W MF 402
R711 10K 5% 1/16W MF 402
DP1 BAS16TW SOT-363
BATT_24PBUS_EN 5
BATT_14PBUS_EN
30 AC_IN_L
DP1 BAS16TW SOT-363
R102 158K 1% 1/16W MF 402
Q9 2N7002DW SOT-363
AC_IN_L_RC
C118 10uF 10% 6.3V CERM 805

WHEN AC IS IN, P-CHANNEL FETS ARE QUICKLY (DIODE) TURNED OFF
WHEN AC IS NOT PLUGGED, P-CHANNEL FETS ARE ON
RC TIME IS 480K*10UF @ +3V_PMU

SWITCHER VOLTAGE CONTROL

PMU SELECTS BETWEEN TWO VOLTAGES

SWITCHER CURRENT CONTROL

CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V
CHARGE THROTTLED BY LOW BATTERY VOLTAGE

+3V_PMU
R73 27.4K 1% 1/16W MF 402
R62 10K 1% 1/16W MF 402
R58 10K 1% 1/16W MF 402
OD OUTPUT LOW - WHEN AC GREATER THAN 18V
R74 4.12K 1% 1/16W MF 402
R733 20K 1% 1/16W MF 402
R731 1K 1% 1/16W MF 402
R56 1K 1% 1/16W MF 402
BATTV_HIGH
BATT_LOW 1
R59 100K 5% 1/16W MF 402
BATTV_LOW
Q4 2N7002DW SOT-363
R75 5.23K 1% 1/16W MF 402
Q71 2N7002DW SOT-363
Q71 2N7002DW SOT-363
29 PMU_CHARGE_V
Q4 2N7002DW SOT-363

U6 MAX1772 QSOP

CSSP	27	26	CSSN
38 1772_DCIN	DCIN	CELLS	16 1772_CELLS
1772_ACIN	ACIN	LDO	2
30 1772_ACOK_L	ACOK	DLOV	22 38 1772_DLOV
(+3V_PMU)	RFIN	BST	25 1772_BST
1772_VCTL	VCTL	DHI	24 1772_DHI
1772_ICTL	ICTL	LX	23 38 1772_LX
1772_ICHG	ICHG	DLO	21 1772_DLO
1772_IINP	IINP	PGND	20 (GND)
		CSIP	19 37 1772_CSIP
1772_CCV	CCV	CSIN	18 37 1772_CSIN
1772_CCI	CCI	BATT	17
1772_CCS	CCS		
	REF CLS GND		

CRITICAL

R55 1K 1% 1/16W MF 402
C43 0.01uF 20% 16V CERM 402
C42 0.01uF 20% 16V CERM 402
1772_CCV_RC
1772_REF
R54 10K 1% 1/16W MF 402
R83 1K 1% 1/16W MF 402
C24 0.1uF 20% 10V CERM 402
C23 1uF 20% 10V CERM 603
R53 4.12K 1% 1/16W MF 402
1772_CLS
38 1772_GND

C41 1uF 20% 10V CERM 603
C98 0.1uF 20% 25V CERM 603
C99 0.1uF 20% 25V CERM 603
R94 100K 5% 1/16W MF 402
XW1 SM

R725 33 1% 1/8W PF 1206
D6 1N914 SOT23
1772_BST_ESR
1772_LDO
R52 100K 5% 1/16W MF 402
C97 0.1uF 20% 25V CERM 603
R96 4.7 5% 1/16W MF 603
C96 0.1uF 20% 50V CERM 805

CRITICAL
Q70 IRF7805 SM
C112 2.2uF 20% 50V CERM 1812
C117 2.2uF 20% 50V CERM 1812
C113 2.2uF 20% 50V CERM 1812
C115 2.2uF 20% 50V CERM 1812
C116 2.2uF 20% 50V CERM 1812

CRITICAL
L70 10uH SM1
+BATT_RSNS 38
R715 0.05 1% 1W MF 2512
+BATT_24V_FUSE 30 38
CRITICAL
D36 MBRS140T3 SM
CRITICAL
Q64 IRF7811W SO-8
NO STUFF
C853 1000pF 10% 25V CERM 402
C780 4.7uF 20% 25V CERM 1206
C795 4.7uF 20% 25V CERM 1206
C790 4.7uF 20% 25V CERM 1206
C779 33uF 20% 25V ELEC SM1
R720 1 5% 1/16W MF 603
R713 1 5% 1/16W MF 603
C777 4.7uF 20% 25V CERM 1206
C792 4.7uF 20% 25V CERM 1206
C785 4.7uF 20% 25V CERM 1206

+3V_PMU
R741 100K 5% 1/16W MF 402
Q72 2N7002DW SOT-363
CHARGE_DISABLE
Q72 2N7002DW SOT-363
29 PMU_CHRG_BATT_O

+3V_PMU
C799 0.1uF 20% 10V CERM 402
U57 LMC7211 SM
BATT_LOW
R729 100K 1% 1/16W MF 402
R740 499K 1% 1/16W MF 402
BATT_DIV
1V65_REF
R730 100K 1% 1/16W MF 402
R735 100K 1% 1/16W MF 402
C807 0.047uF 10% 25V CERM 402

R47 6.34K 1% 1/16W MF 402
A29_CLS_ADJ
30 29 A29_DETECT
Q2 2N7002DW SOT-363

$V_{BATT} = CELLS \times (4.096 + (4.096 * V_{VCTL} / V_{REFIN}))$

For 4.15V cells, VCTL = 0.123 REFIN
For 4.20V cells, VCTL = 0.245 REFIN

$I_{CHG} = (0.2048/R_{62}) * (V_{ICTL} / V_{REFIN})$

BATTERY CONNECTOR

CRITICAL
J26
87438-0833
M-RT-SM

+BATT_POS
(BATT_IN_PD)
BATT_CLK
BATT_DATA
PMU_BATT_DET_L 29 39
BATT_NEG

L5 FERR-EMI-100-OHM SM
L6 FERR-50-OHM SM
L4 FERR-EMI-100-OHM SM
PMU_SMB_CLK 29
L3 FERR-EMI-100-OHM SM
PMU_SMB_DATA 29
L2 FERR-50-OHM SM
+BATT

BATTERY CHARGER

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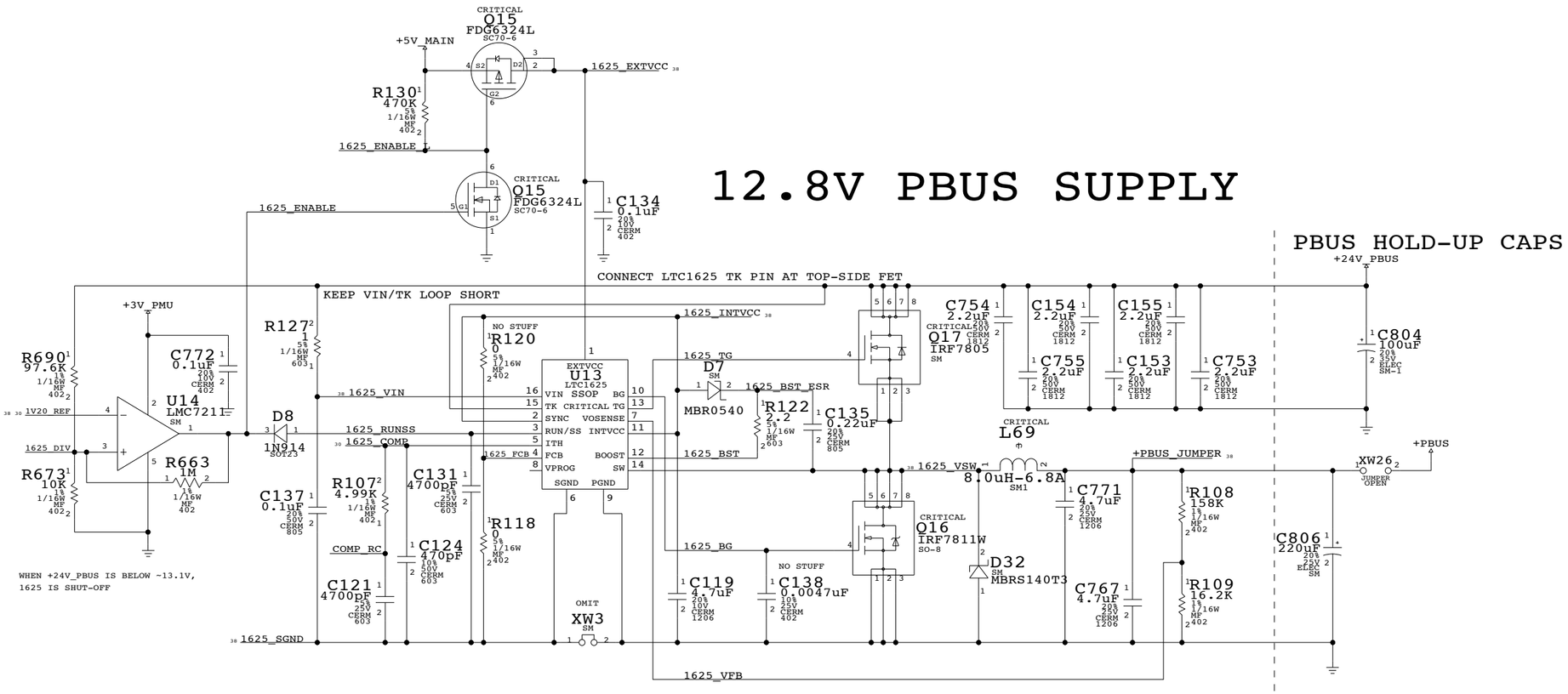
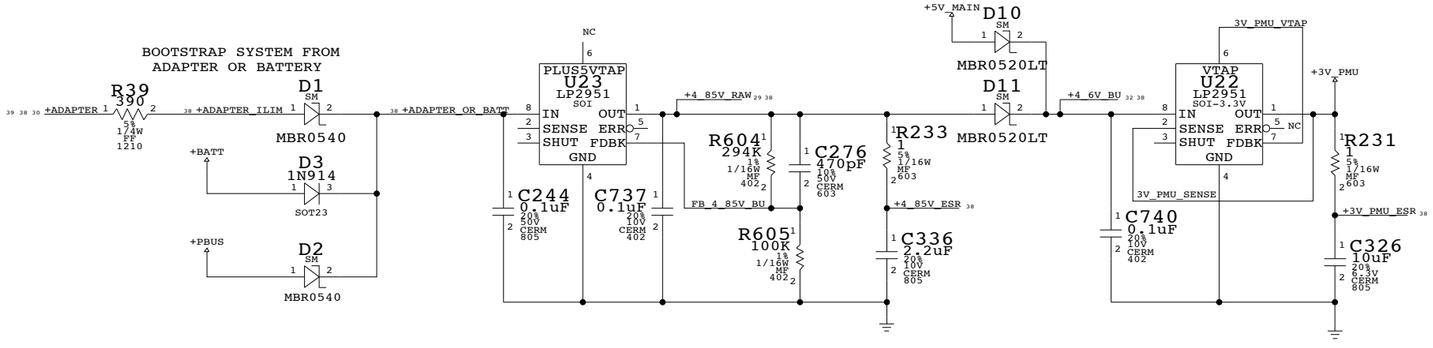
SIZE	DRAWING NUMBER	REV.
D	051-6570	01
SCALE: NONE	SHT 30 OF 44	

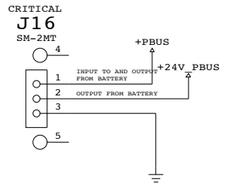
12.8V PBUS SUPPLY



PMU SUPPLY



BACKUP BATTERY



12.8V REGULATOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	01
SCALE: NONE	SHT 31 OF 44	

3.3V/5V MAIN SUPPLY

DCDC_EN TRUTH TABLE

PMU_POWER_UP_L	SLEEP	DCDC_EN	DCDC_EN_L	State
0	0	1	0	Run
1 (2.99V)	1	1	0	Sleep
1	0	0	1	Shutdown
+3V_PMU	+3V_PMU	+4_6V_BU	+3V_PMU	VOLTAGE

SLEEP LEVEL SHIFTER (3V -> 5V)

+5V_SLEEP LOADS

1) FAN
2) Headphone amplifier
3) OPTICAL DRIVE
4) DVI
5) TRACKPAD

+3V_SLEEP LOADS

1) CPU PLL CONFIG CONTROL
2) INTREPID - I2C PULLUPS & OSCILLATOR
3) MAP31 - 3V RAIL (IF USING D3COLD)
4) GRAPHIC CHIP SPREAD SPECTRUM CHIP
5) LVDS DDC PULL-UPS
6) DVI LEVEL SHIFTERS & PULLUPS & HPD
7) BOOT BANGER
8) HARD DRIVE (IF USING 3V LOGIC)
9) WIRELESS
10) PMU - I2C PULLUPS

5V START TO TURN ON ~12.5MS AFTER DCDC_EN_L
3V START TO TURN ON ~25MS AFTER DCDC_EN_L
DIODE WILL ENSURE DCDC_EN_L IS QUICKLY DISCHARGED DURING SHUT-DOWN
POWERDOWN DELAY IS AROUND 4MS-15.6MS

DISTRIBUTE CAPS ALONG TOP EDGE AND FAN CUT-OUT

THIS SIGNAL IS OPEN COLLECTOR TO GND WHEN POWER IS NOT GOOD
220PF IS USED TO QUIET NOISE ON PGOOD ONCE INTERNAL OPEN DRAIN IS DISENGAGED

3.3V/5V REGULATOR

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6570 | REV. 01

SCALE NONE | SHT 32 OF 44

VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage
(approx. 7ms delay)

1.300V->1.050V 1.50Ghz
1.250V->1.050V 1.33Ghz
(value without offset)

NOTE: When U15 MUX is removed => NO SW Support,
R794,R795,R796&R797 have to be stuffed

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
126S0036	7	CAP,AL,POLY,8.2uF,20%,16V,V CASE,SMD	C51,C52,C77,C78,C91,C92,C111	CRITICAL	

SEL = 0; Y1=A1
SEL = 1; Y1=B1

Keep trace fat (40-100 mils) and short!!

MAX1717 VID INPUTS ARE 3.3-5V TOLERANT

Note:No stuff R67 to set skip mode of VCore

Connect MAX1717 GND pin 13
to GND at bottom-side FET

Keep trace fat and short!!

PLACE THIS SHORT AT
PIN OF 1000uF CAP
CLOSEST TO CPU

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V, HENCE VOFFSET = 2.0V * (Rb / Ra) AND VCORE = VDAC + VOFFSET.
NOTE: Ra NO STUFFED FOR NO OFFSET CASE

(CPU Vcore value with offset)

1.50Ghz 1.330V->1.060V
1.33Ghz 1.260V->1.060V

ROUTE AS DIFFERENTIAL PAIR

OUTPUT VOLTAGE

V_{DAC} D4=0	V_{DAC} D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	A/B_ = Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1
If all pull-ups are >=100K and all
pull-downs are <=1K, A V = B V .

Fmax Test Connections

VCORE SUPPLY

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D	051-6570	01
SCALE: NONE	SHT 33 OF 44	

1.5V/2.5V SWITCHER

M11 Power Shut down Sequencing

+1_5V_SLEEP LOADS
1) AGP I/O - IF USING D3COLD
2) MAXBUS I/O - IF 1.5V INTERFACE

+1_5V_MAIN LOADS
1) INTREPID CORE

+2_5V_MAIN LOADS
1) MAP31 - FBCORE/FBIO IF USING D3HOT
2) GIGABIT ETHERNET - AVDDL
3) DDR SODIMMS - CORE/IO
4) DDR MUXES

+2_5V_SLEEP LOADS
1) FBCORE/FBIO IF USING D3COLD

Q53 SI3446DV TSOP
C717 10uF 20% 6.3V CERM 805
C718 1000pF 10% 25V X7R 402
DP3 BAS16TW SOT-363
R184 330K 1% 1/16W MF 402
Q10 2N7002 SM
C133 0.01uF 20% 16V CERM 402
R116 100K 5% 1/16W MF 402
R115 100K 5% 1/16W MF 402
Q11 2N7002DW SOT-363
R114 100K 5% 1/16W MF 402
C129 1000pF 10% 25V X7R 402
R117 100K 5% 1/16W MF 402
DP3 BAS16TW SOT-363
R177 20 5% 1/16W MF 402
C195 2.2uF 20% 10V CERM 805
R227 0 5% 1/16W MF 402
C194 2.2uF 20% 10V CERM 805
R226 0 5% 1/16W MF 402
DP3 BAS16TW SOT-363
R210 158K 1% 1/16W MF 402
R211 158K 1% 1/16W MF 402
U19 MAX1715 QSOP
C232 4.7uF 20% 25V CERM 1206
C209 4.7uF 20% 25V CERM 1206
C196 0.1uF 20% 25V CERM 603
R171 4.7 5% 1/16W MF 603
R170 4.7 5% 1/16W MF 603
C193 0.1uF 20% 25V CERM 603
Q56 IRF7805 SM
L67 4.7uH SM4
R212 5.11K 1% 1/16W MF 402
R222 10K 1% 1/16W MF 402
C738 10uF 20% 6.3V CERM 805
C307 150uF 20% 6.3V TANT SMD-1
C267 150uF 20% 6.3V TANT SMD-1
D31 MBRS130LT3 SM
Q57 IRF7811W SO-8
C844 0.001uF 10% 50V CERM 402
R221 0 5% 1/16W MF 402
C298 1uF 20% 10V CERM 603
R220 0 5% 1/16W MF 402
R468 15.4K 1% 1/16W MF 402
R601 10K 1% 1/16W MF 402
C338 4.7uF 20% 25V CERM 1206
C355 4.7uF 20% 25V CERM 1206
Q55 IRF7805 SM
Q54 IRF7811W SO-8
C845 0.001uF 20% 50V CERM 402
L65 4.7uH SM4
D30 MBRS130LT3 SM
C725 10uF 20% 6.3V CERM 805
C393 150uF 20% 6.3V TANT SMD-1
C405 150uF 20% 6.3V TANT SMD-1
C396 150uF 20% 6.3V TANT SMD-1
U48 SI6467BDQ TSSOP
C715 10uF 20% 6.3V CERM 805
C716 1000pF 10% 25V X7R 402
R557 100K 5% 1/16W MF 402
C714 1000pF 10% 25V X7R 402
R554 100K 5% 1/16W MF 402
XW8 XW21 XW23 XW10 SM
DP4 BAS16TW SOT-363
XW24 XW22 XW25 XW17 XW18 OMIT JUMPER OPEN

1.8V SWITCHER

+1_8V_MAIN LOADS
1) INTREPID PLLS

+1_8V_SLEEP LOADS
1) MPC7447 - MAXBUS I/O - IF 1.8V INTERFACE
2) CPU JTAG & MaxBus Pull-ups
3) CPU PLL Config Straps

R398 1M 5% 1/16W MF 402
R535 324K 1% 1/16W MF 402
Q31 2N7002 SM
C695 10uF 20% 6.3V CERM 805
R526 10K 5% 1/16W MF 402
R527 1M 5% 1/16W MF 402
R531 10 5% 1/16W MF 402
U46 LTC3411 MSOP
L63 2.2uH SM1
C693 10pF 5% 50V CERM 402
R529 887K 1% 1/16W MF 402
C697 22uF 20% 10V CERM 1210
R528 698K 1% 1/16W MF 402
R532 16.2K 1% 1/16W MF 402
C691 1000pF 5% 25V CERM 603
R536 10K 5% 1/16W MF 402
R525 1M 5% 1/16W MF 402
C690 1uF 20% 10V CERM 603
R566 100K 5% 1/16W MF 402
C719 10uF 20% 6.3V CERM 805
U50 SI3447DV TSOP
C722 1000pF 10% 25V X7R 402
C720 1000pF 10% 25V X7R 402
R571 100K 5% 1/16W MF 402

1.5V/1.8V/2.5V SUPPLIES

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SIZE D | DRAWING NUMBER 051-6570 | REV. 01
SCALE NONE | SHT 34 44

DIGITAL SIGNALS

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
				STUB_LENGTH OF 200 MILS NEEDED WHEN WE CONVERT TO 14.2				
GROUP 0	MEM_DATA<7..0>	L:S:1602:1700	7	500	(200)			167 MHZ
	MEM_DQM<0>	L:S:1602 MIL:1700 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<0>	L:S:1602 MIL:1700 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<7..0>	L:S:1903:2000	7	500	(200)			167 MHZ
	RAM_DQM_A<0>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<0>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<7..0>	L:S:2000:2100	7	500	(200)			167 MHZ
	RAM_DQM_B<0>	L:S:2000 MIL:2100 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<0>	L:S:2000 MIL:2100 MIL	7	500.0000	(200)			167.0 MHz
GROUP 1	MEM_DATA<15..8>	L:S:1344:1660	7	500	(200)			167 MHZ
	MEM_DQM<1>	L:S:1344 MIL:1660 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<1>	L:S:1344 MIL:1660 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<15..8>	L:S:1905:2000	7	500	(200)			167 MHZ
	RAM_DQM_A<1>	L:S:1905 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<1>	L:S:1905 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<15..8>	L:S:2004:2412	7	500	(200)			167 MHZ
	RAM_DQM_B<1>	L:S:2004 MIL:2412 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<1>	L:S:2004 MIL:2412 MIL	7	500.0000	(200)			167.0 MHz
GROUP 2	MEM_DATA<23..16>	L:S:1435:1500	7	500	(200)			167 MHZ
	MEM_DQM<2>	L:S:1435 MIL:1500 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<2>	L:S:1435 MIL:1500 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<23..16>	L:S:1707:1800	7	500	(200)			167 MHZ
	RAM_DQM_A<2>	L:S:1707 MIL:1800 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<2>	L:S:1707 MIL:1800 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<23..16>	L:S:1900:2000	7	500	(200)			167 MHZ
	RAM_DQM_B<2>	L:S:1900 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<2>	L:S:1900 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
GROUP 3	MEM_DATA<31..24>	L:S:1233:1485	7	500	(200)			167 MHZ
	MEM_DQM<3>	L:S:1233 MIL:1485 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<3>	L:S:1233 MIL:1485 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<31..24>	L:S:1700:2165	7	500	(200)			167 MHZ
	RAM_DQM_A<3>	L:S:1700 MIL:2165 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<3>	L:S:1700 MIL:2165 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<25..24>	L:S:1907:2356	7	500	(200)			167 MHZ
	RAM_DATA_B<26>	L:S:1907 MIL:2356 MIL	7		(200)			167.0 MHz
	RAM_DATA_B<31..27>	L:S:1907:2356	7	500	(200)			167 MHZ
	RAM_DQM_B<3>	L:S:1907 MIL:2356 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<3>	L:S:1907 MIL:2356 MIL	7	500.0000	(200)			167.0 MHz
GROUP 4	MEM_DATA<39..32>	L:S:1915:2000	7	500	(200)			167 MHZ
	MEM_DQM<4>	L:S:1915 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<4>	L:S:1915 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<39..32>	L:S:1205:1387	7	500	(200)			167 MHZ
DDR RAM	RAM_DQM_A<4>	L:S:1205 MIL:1387 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<4>	L:S:1205 MIL:1387 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<39..32>	L:S:1404:1686	7	500	(200)			167 MHZ
	RAM_DQM_B<4>	L:S:1404 MIL:1686 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<4>	L:S:1404 MIL:1686 MIL	7	500.0000	(200)			167.0 MHz
GROUP 5	MEM_DATA<47..40>	L:S:1719:1893	7	500	(200)			167 MHZ
	MEM_DQM<5>	L:S:1719 MIL:1893 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<5>	L:S:1719 MIL:1893 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<47..40>	L:S:1607:1898	7	500	(200)			167 MHZ
	RAM_DQM_A<5>	L:S:1607 MIL:1898 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<5>	L:S:1607 MIL:1898 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<47..40>	L:S:1716:2102	7	500	(200)			167 MHZ
	RAM_DQM_B<5>	L:S:1716 MIL:2102 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<5>	L:S:1716 MIL:2102 MIL	7	500.0000	(200)			167.0 MHz
GROUP 6	MEM_DATA<55..48>	L:S:2101:2170	7	500	(200)			167 MHZ
	MEM_DQM<6>	L:S:2101 MIL:2170 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<6>	L:S:2101 MIL:2170 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<55..48>	L:S:1204:1357	7	500	(200)			167 MHZ
	RAM_DQM_A<6>	L:S:1204 MIL:1357 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<6>	L:S:1204 MIL:1357 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<55..48>	L:S:1400:1546	7	500	(200)			167 MHZ
	RAM_DQM_B<6>	L:S:1400 MIL:1546 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<6>	L:S:1400 MIL:1546 MIL	7	500.0000	(200)			167.0 MHz
GROUP 7	MEM_DATA<63..56>	L:S:1903:2000	7	500	(200)			167 MHZ
	MEM_DQM<7>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<7>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<63..56>	L:S:1611:1696	7	500	(200)			167 MHZ
	RAM_DQM_A<7>	L:S:1611 MIL:1696 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<7>	L:S:1611 MIL:1696 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<63..56>	L:S:1809:1887	7	500	(200)			167 MHZ
	RAM_DQM_B<7>	L:S:1809 MIL:1887 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<7>	L:S:1809 MIL:1887 MIL	7	500.0000	(200)			167.0 MHz
ADDR	MEM_ADDR<12..0>	L:S::500	4					83 MHZ
	RAM_ADDR<12..0>	L:S:2000:3000	10		(200)			
	MEM_BA<1..0>	L:S::500	4					
	RAM_BA<1..0>	L:S:2000:3300	8		(200)			
CONTROL	MEM_CS_L<3..0>	L:S::500	4					
	RAM_CS_L<3..0>	L:S:2500:3200	7		(200)			
	MEM_CKE<3..0>	L:S::500	4					
	RAM_CKE<3..0>	L:S:2500:3200	7		(200)			
	MEM_RAS_L	L:S::500 MIL	4					
	RAM_RAS_L	L:S:2000 MIL:4100 MIL	7		(200)			
	MEM_CAS_L	L:S::500 MIL	4					
	RAM_CAS_L	L:S:2000 MIL:4100 MIL	7		(200)			
	MEM_WE_L	L:S::500 MIL	4					
	RAM_WE_L	L:S:2000 MIL:3100 MIL	8		(200)			
	MEM_MUXSEL_MSB	L:S:1700 MIL:3000 MIL	8					
	MEM_MUXSEL_LSB	L:S:1700 MIL:3000 MIL	7					

TOTAL LENGTH CONTROLLED BY SPREADSHEET

PRIORITY: 2
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9
GOAL: MINIMIZE
EXPOSED ROUTES
MINIMIZE VIAS

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME	PROPAGATION_DELAY	MATCHED_DELAY	MAX VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM
INTREPID CLOCKS	SYSCLK_CPU_UF	L:S::150 MIL					10 MIL SPACING	167.0 MHz
	SYSCLK_CPU	L:S:2650 MIL:2750 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz
	INT_CPUFB_OUT	L:S::150 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_OUT_SHORT	L:S:700 MIL:850 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_OUT_NORM	L:S:500 MIL:600 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_IN_NORM	L:S:500 MIL:600 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_LONG	L:S:1050 MIL:1150 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_IN	L:S:700 MIL:800 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0_UF	L:S:300 MIL:400 MIL	SYSCLK_DDRCLK_A0_UF	SYSCLK_DDRCLK_A0_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0_L_UF	L:S:300 MIL:400 MIL	SYSCLK_DDRCLK_A0_UF	SYSCLK_DDRCLK_A0_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1_UF	L:S:300 MIL:400 MIL	SYSCLK_DDRCLK_A1_UF	SYSCLK_DDRCLK_A1_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1_L_UF	L:S:300 MIL:400 MIL	SYSCLK_DDRCLK_A1_UF	SYSCLK_DDRCLK_A1_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0_UF	L:S:300 MIL:400 MIL	SYSCLK_DDRCLK_B0_UF	SYSCLK_DDRCLK_B0_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0_L_UF	L:S:300 MIL:400 MIL	SYSCLK_DDRCLK_B0_UF	SYSCLK_DDRCLK_B0_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1_UF	L:S:300 MIL:400 MIL	SYSCLK_DDRCLK_B1_UF	SYSCLK_DDRCLK_B1_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1_L_UF	L:S:300 MIL:400 MIL	SYSCLK_DDRCLK_B1_UF	SYSCLK_DDRCLK_B1_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A0	SYSCLK_DDRCLK_A0:G:L:S:0 MIL:25 MIL	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0_L	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A0	SYSCLK_DDRCLK_A0:G:L:S:0 MIL:25 MIL	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A1	SYSCLK_DDRCLK_A1:G:L:S:0 MIL:25 MIL	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1_L	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A1	SYSCLK_DDRCLK_A1:G:L:S:0 MIL:25 MIL	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B0	SYSCLK_DDRCLK_B0:G:L:S:0 MIL:25 MIL	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0_L	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B0	SYSCLK_DDRCLK_B0:G:L:S:0 MIL:25 MIL	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B1	SYSCLK_DDRCLK_B1:G:L:S:0 MIL:25 MIL	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1_L	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B1	SYSCLK_DDRCLK_B1:G:L:S:0 MIL:25 MIL	250.0000	(200)	10 MIL SPACING	167.0 MHz
	INT_REF_CLK_OUT_UF	L:S::400 MIL				(200)	10 MIL SPACING	49.92 MHz
	INT_REF_CLK_OUT	L:S:1000 MIL:1150 MIL		5	250.0000	(200)	10 MIL SPACING	49.92 MHz
	INT_REF_CLK_IN	L:S:1900 MIL:2000 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz
	CLK66M_GPU_AGP_UF	L:S::150 MIL				(200)	10 MIL SPACING	66.00 MHz
	CLK66M_GPU_AGP	L:S:1800 MIL:1900 MIL		6	400.0000	(200)	10 MIL SPACING	66.00 MHz
	INT_AGP_FB_OUT	L:S::150 MIL				(200)	10 MIL SPACING	66.00 MHz
	INT_AGP_FB_IN	L:S:1450 MIL:1550 MIL		6	500.0000	(200)	10 MIL SPACING	66.00 MHz
	CLK33M_CBUS_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz
	CLK33M_CBUS	L:S:5000 MIL:6000 MIL		9	500.0000	(200)	10 MIL SPACING	33.00 MHz
	CLK33M_AIRPORT_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz
	CLK33M_AIRPORT	L:S:9500 MIL:10500 MIL		6	500.0000	(200)	10 MIL SPACING	33.00 MHz
	CLK33M_NEC_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz
	CLK33M_NEC	L:S:4000 MIL:6000 MIL		7	500.0000	(200)	10 MIL SPACING	33.00 MHz
	INT_PCI_FB_OUT	L:S::300 MIL				(200)	10 MIL SPACING	33.00 MHz
	INT_PCI_FB_IN	L:S:6500 MIL:7500 MIL		7	500.0000	(200)	10 MIL SPACING	33.00 MHz
M10 & OSC	ATI_CLK27M_OSC	L:S::400 MIL		5		(200)	10 MIL SPACING	
	ATI_CLK27M_OSC_SS	L:S::400 MIL		5		(200)	10 MIL SPACING	
	ATI_CLK27M_IN	L:S::200 MIL		5		(200)	10 MIL SPACING	
	ATI_SSCLK_UF	L:S::200 MIL		5		(200)	10 MIL SPACING	
	ATI_SSCLK_IN	L:S::1800 MIL		5	500.0000	(200)	10 MIL SPACING	
CRYSTALS	CLK18M_INT_XIN	L:S:1400 MIL:1500 MIL					10 MIL SPACING	
	CLK18M_INT_XOUT	L:S:1250 MIL:1350 MIL					10 MIL SPACING	
	CLK18M_XTAL_IN	L:S::300 MIL					10 MIL SPACING	
	CLK18M_INT_EXT	L:S::400 MIL					10 MIL SPACING	
SOUND	INT_I2S0_SND_MCLK			6	500.0000	(200)	10 MIL SPACING	
ETHERNET	CLKENET_PHY_RX	L:S::300 MIL				(200)		125.0 MHz
	CLKENET_LINK_RX	L:S:8000 MIL:9000 MIL		6	800.0000	(200)	10 MIL SPACING	125.0 MHz
	CLKENET_PHY_GBE_REF	L:S::300 MIL				(200)		125.0 MHz
	CLKENET_LINK_GBE_REF	L:S:8000 MIL:9000 MIL		6	500.0000	(200)	10 MIL SPACING	125.0 MHz
	CLKENET_PHY_TX	L:S::300 MIL				(200)		25.00 MHz
	CLKENET_LINK_TX	L:S:8000 MIL:9000 MIL		6	500.0000	(200)	10 MIL SPACING	25.00 MHz
	CLKENET_LINK_GTX	L:S::300 MIL				(200)		125.0 MHz
	CLKENET_PHY_GTX	L:S:8000 MIL:9000 MIL		6	600.0000	(200)	10 MIL SPACING	125.0 MHz
FIREWIRE	CLKFW_PHY_PCLK	L:S::300 MIL				(200)		49.15 MHz
	CLKFW_LINK_PCLK	L:S:7500 MIL:8000 MIL		5	500.0000	(200)	10 MIL SPACING	49.15 MHz
	CLKFW_PHY_LCLK	L:S:7500 MIL:8000 MIL		5	500.0000	(200)	10 MIL SPACING	49.15 MHz
	CLKFW_LINK_LCLK	L:S::300 MIL				(200)		49.15 MHz
	FW_XI	L:S::500 MIL				(200)	10 MIL SPACING	98.03 MHz
	FW_OSC	L:S::300 MIL				(200)	10 MIL SPACING	98.03 MHz

PRIORITY: 1
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9
GOAL: MINIMIZE EXPOSURE ON LONG NETS

SIGNAL CONSTRAINTS - PAGE 1

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	01
SCALE: NONE	SHT 35	OF 44

DIGITAL SIGNALS

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
MAXBUS	CPU_AACK_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_ADDR<0..31>	L:S:1500:3100	7		(250)		TRUE	83 MHZ
	CPU_ARTRY_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_BG_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_BR_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_CI_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_DATA<0..31>	L:S:1100:2700	7		(250)		TRUE	83 MHZ
	CPU_DATA<32..63>	L:S:1100:2700	8		(250)			83 MHZ
	CPU_DBG_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_DTI<0..2>	L:S:1500:2950	7		(250)			
	CPU_DRDY_L	L:S:1500 MIL:3200 MIL	7		(250)			
	CPU_GBL_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_HIT_L	L:S:1500 MIL:2800 MIL	7		(250)			
	CPU_QACK_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_QREQ_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_TA_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_TBST_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_TEA_L	L:S:1500 MIL:3000 MIL	7		(250)			
	CPU_TS_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_TSIZ<0..2>	L:S:1500:3500	7		(250)			
	CPU_TT<0..4>	L:S:1500:3400	7		(250)			
	CPU_WT_L	L:S:1500 MIL:3100 MIL	7		(250)			

PRIORITY: 4
PRIMARY LAYERS: 9
SECONDARY LAYERS: 4,7
GOAL: MINIMIZE TH VIAS

STUB_LENGTH OF 250 MILS NEEDED WHEN DESIGN SWITCHED TO 14.2

Temporary Area for TMDS/DVO signal constraints

ALL TMDS GROUP SIGNALS ROUTE AT LAYER 4 OR 7 AND HAVE SAME WIDTH SPACING RULE AS OTHER TMDS SIGNALS

123	GPU_TMDS_CLKN	GPU_CLKTMDS	GPUTMDS:G:L:S:0 MIL:50 MIL		500.0000	100 OHM SPACING 100 OHM SPACING 5	19 20
123	GPU_TMDS_CLKP	GPU_CLKTMDS	GPUTMDS:G:L:S:0 MIL:50 MIL		500.0000	100 OHM SPACING 100 OHM SPACING 5	19 20
123	GPU_TMDS_DN<0>	GPU_TMDS_D0			500.0000	100 OHM SPACING 100 OHM SPACING 8	19 20
123	GPU_TMDS_DP<0>	GPU_TMDS_D0			500.0000	100 OHM SPACING 100 OHM SPACING 8	19 20
123	GPU_TMDS_DN<1>	GPU_TMDS_D1			500.0000	100 OHM SPACING 100 OHM SPACING 8	19 20
123	GPU_TMDS_DP<1>	GPU_TMDS_D1			500.0000	100 OHM SPACING 100 OHM SPACING 8	19 20
123	GPU_TMDS_DN<2>	GPU_TMDS_D2			500.0000	100 OHM SPACING 100 OHM SPACING 8	19 20
123	GPU_TMDS_DP<2>	GPU_TMDS_D2			500.0000	100 OHM SPACING 100 OHM SPACING 8	19 20

124	SI_TMDS_CLKN	SI_CLKTMDS	SITMDS:G:L:S:0 MIL:50 MIL			100 OHM SPACING 100 OHM SPACING 5	19
123	SI_TMDS_CLKP	SI_CLKTMDS	SITMDS:G:L:S:0 MIL:50 MIL			100 OHM SPACING 100 OHM SPACING 5	19
124	SI_TMDS_DN<0>	SI_TMDS_D0				100 OHM SPACING 100 OHM SPACING 8	19
124	SI_TMDS_DP<0>	SI_TMDS_D0				100 OHM SPACING 100 OHM SPACING 8	19
124	SI_TMDS_DN<1>	SI_TMDS_D1				100 OHM SPACING 100 OHM SPACING 8	19
124	SI_TMDS_DP<1>	SI_TMDS_D1				100 OHM SPACING 100 OHM SPACING 8	19
124	SI_TMDS_DN<2>	SI_TMDS_D2				100 OHM SPACING 100 OHM SPACING 8	19
124	SI_TMDS_DP<2>	SI_TMDS_D2				100 OHM SPACING 100 OHM SPACING 8	19

ALL THE DVOD GROUP SIGNALS ROUTE AT LAYER 4 OR 7 AND ROUTE AS STANDARD 50OHM SIGNALS AT 4 MILS

126	ATI_DVOD<11..0>	ATIDVOD:G:L:S:0 MIL:50 MIL		6	610		19 20
126	ATI_DVOD_DE	ATIDVOD:G:L:S:0 MIL:50 MIL		6	610.0000		19 20
126	ATI_DVO_HSYNC	ATIDVOD:G:L:S:0 MIL:50 MIL		6	610.0000		19 20
126	ATI_DVO_VSYNC	ATIDVOD:G:L:S:0 MIL:50 MIL		6	610.0000		19 20
126	ATI_DVO_CLKP	ATIDVOD:G:L:S:0 MIL:50 MIL		6	610.0000	165.0 MHz:::	19 20
125	GPU_DVOD<11..0>	GPUDVOD:G:L:S:0 MIL:50 MIL		6	700		19
125	GPU_DVOD_DE	GPUDVOD:G:L:S:0 MIL:50 MIL		6	500.0000		19
126	GPU_DVO_HSYNC	GPUDVOD:G:L:S:0 MIL:50 MIL		6	500.0000		19
126	GPU_DVO_VSYNC	GPUDVOD:G:L:S:0 MIL:50 MIL		6	500.0000		19
126	GPU_DVO_CLKP	GPUDVOD:G:L:S:0 MIL:50 MIL		6	500.0000	165.0 MHz:::	19

126	TMDS_CONN_CLKN	CLKCONN_TMDS	TMDS_CONN:G:L:S:0 MIL:50 MIL		500.0000	100 OHM SPACING 100 OHM SPACING 4	22 39
126	TMDS_CONN_CLKP	CLKCONN_TMDS	TMDS_CONN:G:L:S:0 MIL:50 MIL		500.0000	100 OHM SPACING 100 OHM SPACING 4	22 39
127	TMDS_CONN_DN<0>	CONN_TMDS_D0			500.0000	100 OHM SPACING 100 OHM SPACING 4	22
127	TMDS_CONN_DP<0>	CONN_TMDS_D0			500.0000	100 OHM SPACING 100 OHM SPACING 4	22
127	TMDS_CONN_DN<1>	CONN_TMDS_D1			500.0000	100 OHM SPACING 100 OHM SPACING 4	22
127	TMDS_CONN_DP<1>	CONN_TMDS_D1			500.0000	100 OHM SPACING 100 OHM SPACING 4	22
127	TMDS_CONN_DN<2>	CONN_TMDS_D2			500.0000	100 OHM SPACING 100 OHM SPACING 4	22
127	TMDS_CONN_DP<2>	CONN_TMDS_D2			500.0000	100 OHM SPACING 100 OHM SPACING 4	22

SIGNAL CONSTRAINTS - PAGE 1

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	01

SCALE: NONE | SHT 36 OF 44

Digital Signals (cont'd)

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
AGP	AGP_AD<15..0>	L:S:1050:1450	7					66 MHz
AGP BYTES 0-1	AGP_CBE<1..0>	L:S:1050:1450	7					66 MHz
	AGP_AD_STB<0>	L:S:1050 MIL:1450 MIL			(250)	8 MIL SPACING		133.0 MHz:::
	AGP_AD_STB_L<0>	L:S:1050 MIL:1450 MIL			(250)	8 MIL SPACING		133.0 MHz:::
AGP BYTES 2-3	AGP_AD<31..16>	L:S:1050:1450	7					66 MHz
	AGP_CBE<3..2>	L:S:1050:1450	7					66 MHz
	AGP_AD_STB<1>	L:S:1050 MIL:1450 MIL			(250)	8 MIL SPACING		133.0 MHz:::
	AGP_AD_STB_L<1>	L:S:1050 MIL:1450 MIL			(250)	8 MIL SPACING		133.0 MHz:::
AGP SIDEBAND	AGP_SBA<7..0>	L:S:1050:1450	7					66 MHz
	AGP_SB_STB	L:S:1050 MIL:1450 MIL			(350)	8 MIL SPACING		66.00 MHz:::
	AGP_SB_STB_L	L:S:1050 MIL:1450 MIL			(350)	8 MIL SPACING		66.00 MHz:::
AGP CONTROL	AGP_FRAME_L	L:S:1250 MIL:1950 MIL						66.00 MHz:::
	AGP_IRDY_L	L:S:1250 MIL:1950 MIL						66.00 MHz:::
	AGP_TRDY_L	L:S:1250 MIL:1950 MIL						66.00 MHz:::
	AGP_DEVSEL_L	L:S:1250 MIL:1950 MIL						66.00 MHz:::
	AGP_STOP_L	L:S:1250 MIL:1950 MIL						66.00 MHz:::
	AGP_PAR	L:S:1250 MIL:1950 MIL						66.00 MHz:::
	AGP_REQ_L	L:S:1250 MIL:1950 MIL						66.00 MHz:::
	AGP_GNT_L	L:S:1250 MIL:1950 MIL						66.00 MHz:::
	AGP_RBF_L	L:S:1250 MIL:1950 MIL						66.00 MHz:::
PCI	PCI_AD<31..0>	L:S:6000:12500				MIN_DAISY_CHAIN		33 MHz
	PCI_CBE<3..0>	L:S:6000:12500				MIN_DAISY_CHAIN		33 MHz
	PCI_FRAME_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHz:::
	PCI_IRDY_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHz:::
	PCI_TRDY_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHz:::
	PCI_DEVSEL_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHz:::
	PCI_STOP_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHz:::
	PCI_PAR	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHz:::
ULTRA ATA-100	UIDE_DATA<15..8>	L:S::710			(200)			100 MHZ
	UIDE_DATA<7>	U51_V1:RP19.3::600 MIL			(200)			100.0 MHz:::
	UIDE_DATA<6..0>	L:S::600			(200)			100 MHZ
	UIDE_ADDR<2..0>	L:S::650			(200)	NEED TO MATCH DELAY TO 250		100 MHZ
	UIDE_RST_L	L:S::400 MIL			(200)			100.0 MHz:::
	UIDE_DIOW_L	L:S::400 MIL			(200)			100.0 MHz:::
	UIDE_DIOR_L	L:S::600 MIL		10 MIL SPACING	(200)			100.0 MHz:::
	UIDE_DMACK_L	L:S::400 MIL			(200)			100.0 MHz:::
	UIDE_CS0_L	L:S::500 MIL			(200)			100.0 MHz:::
	UIDE_CS1_L	L:S::500 MIL			(200)			100.0 MHz:::
	UIDE_DMARQ	L:S::400 MIL			(200)			100.0 MHz:::
	UIDE_IOCHRDY	L:S::600 MIL		10 MIL SPACING	(200)			100.0 MHz:::
	UIDE_INTRQ	L:S::400 MIL			(200)			100.0 MHz:::
	HD_DATA<15..0>	L:S:5000:6500	7		(200)			100 MHZ
	HD_ADDR<2..0>	L:S:5000:6500	7		(200)			100 MHZ
	HD_RESET_L	L:S:4000 MIL:6000 MIL	7		(200)	TOTAL UIDE+HD SKEW <500MIL		100.0 MHz:::
	HD_DIOW_L	L:S:3000 MIL:5200 MIL	7		(200)			100.0 MHz:::
	HD_DIOR_L	L:S:6100 MIL:6150 MIL	7	10 MIL SPACING	(200)			100.0 MHz:::
	HD_DMACK_L	L:S:4500 MIL:6000 MIL	7		(200)			100.0 MHz:::
	HD_CS0_L	L:S:3000 MIL:6000 MIL	7		(200)			100.0 MHz:::
	HD_CS1_L	L:S:3000 MIL:6000 MIL	7		(200)			100.0 MHz:::
	HD_DMARQ	L:S:4500 MIL:6000 MIL	7		(200)			100.0 MHz:::
	HD_IOCHRDY	L:S:6200 MIL:6300 MIL	7	10 MIL SPACING	(200)			100.0 MHz:::
	HD_INTRQ	L:S:3000 MIL:5000 MIL	7					100.0 MHz:::
EIDE	EIDE_DATA<15..0>	L:S::850						33 MHZ
INTREPID	EIDE_ADDR<2..0>	L:S::850						33 MHZ
	EIDE_CS0_L	L:S::850 MIL						33.00 MHz:::
	EIDE_CS1_L	L:S::850 MIL						33.00 MHz:::
	EIDE_RD_L	L:S::500 MIL						33.00 MHz:::
	EIDE_WR_L	L:S::500 MIL						33.00 MHz:::
	EIDE_IOCHRDY	L:S::500 MIL						33.00 MHz:::
	EIDE_INT	L:S::500 MIL						33.00 MHz:::
	EIDE_RST_L	L:S::500 MIL						33.00 MHz:::
	EIDE_DMACK_L	L:S::500 MIL						33.00 MHz:::
	EIDE_DMARQ	L:S::500 MIL						33.00 MHz:::
OPTICAL	EIDE_OPTICAL_DATA<15..0>	L:S:4000:6000						33 MHZ
	EIDE_OPTICAL_ADDR<2..0>	L:S:4000:6000						33 MHZ
	EIDE_OPTICAL_CS0_L	L:S:4500 MIL:6500 MIL						33.00 MHz:::
	EIDE_OPTICAL_CS1_L	L:S:4500 MIL:6500 MIL						33.00 MHz:::
	EIDE_OPTICAL_READ_L	L:S:4500 MIL:6500 MIL						33.00 MHz:::
	EIDE_OPTICAL_WR_L	L:S:4500 MIL:6500 MIL						33.00 MHz:::
	EIDE_OPTICAL_IOCHRDY	L:S:4500 MIL:6500 MIL						33.00 MHz:::
	EIDE_OPTICAL_INT	L:S:5000 MIL:7000 MIL						33.00 MHz:::
	EIDE_OPTICAL_RST_L	L:S:4500 MIL:6500 MIL						33.00 MHz:::
	EIDE_OPTICAL_DMAACK_L	L:S:4500 MIL:6500 MIL						33.00 MHz:::
	EIDE_OPTICAL_DMA_RQ	L:S:4500 MIL:6500 MIL						33.00 MHz:::
ETHERNET MII	ENET_LINK_RXD<7..0>	L:S:8000:9000	7	(400)		(400)		
	ENET_RX_DV	L:S:8000 MIL:9000 MIL						
	ENET_RX_ER	L:S:8000 MIL:9000 MIL						
	ENET_PHY_TXD<7..0>	L:S:8000:9000	7	(400)		(400)		
	ENET_LINK_TXD<7..0>	L:S::600						
	ENET_PHY_TX_ER	L:S:8000 MIL:9000 MIL						
	ENET_LINK_TX_ER	L:S::400 MIL						
	ENET_PHY_TX_EN	L:S:8000 MIL:9000 MIL						
	ENET_LINK_TX_EN	L:S::400 MIL						
	ENET_MDIO	L:S:8000 MIL:9000 MIL						
	ENET_MDC	L:S:8000 MIL:9000 MIL						
	ENET_COL	L:S:8000 MIL:9000 MIL						
	ENET_CRS	L:S:8000 MIL:9000 MIL						
FIREWIRE MII	FW_LINK_DATA<7..0>	L:S:2700:3500	7	(400)		(400)		
	FW_PHY_DATA<7..0>	L:S:4700:5500	7	(400)		(400)		
	FW_LINK_CNTL<1..0>	L:S:9000:10000						
	FW_PHY_CNTL<1..0>	L:S::300						
	FW_LINK_LREQ	L:S::300 MIL						
	FW_PHY_LREQ	L:S:8500 MIL:9500 MIL						
	FW_PINT	L:S:8500 MIL:9500 MIL						

PRIORITY: 4
PRIMARY LAYERS: 9
SECONDARY LAYERS: 4,7
GOAL: MINIMIZE TH VIAS

PRIORITY: 7
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 6
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 8
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 5
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 5
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR	RELATIVE_PROPAGATION_DELAY	MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS
FIREWIRE Zo = 110	FW_TPI0N	FW_TPI0	FW_TPI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPI0P	FW_TPI0	FW_TPI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPO0N	FW_TPO0	FW_TPO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPO0P	FW_TPO0	FW_TPO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPBI0N	FW_TPBI0	FW_TPBI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPBI0P	FW_TPBI0	FW_TPBI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPAO0N	FW_TPAO0	FW_TPAO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPAO0P	FW_TPAO0	FW_TPAO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPA1N	FW_TPA1	FW_TPA1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPA1P	FW_TPA1	FW_TPA1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPB1N	FW_TPB1	FW_TPB1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPB1P	FW_TPB1	FW_TPB1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPI1N	FW_TPI1	FW_TPI1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPI1P	FW_TPI1	FW_TPI1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPO1N	FW_TPO1	FW_TPO1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPO1P	FW_TPO1	FW_TPO1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
ETHERNET Zo = 100	MDI_P<0>	ENET_MDI0	ENET_MDI0:G:U43.29:J23.1:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_M<0>	ENET_MDI0	ENET_MDI0:G:U43.31:J23.2:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_P<1>	ENET_MDI1	ENET_MDI1:G:U43.33:J23.3:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_M<1>	ENET_MDI1	ENET_MDI1:G:U43.34:J23.4:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_P<2>	ENET_MDI2	ENET_MDI2:G:U43.39:J23.7:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_M<2>	ENET_MDI2	ENET_MDI2:G:U43.41:J23.8:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_P<3>	ENET_MDI3	ENET_MDI3:G:U43.42:J23.9:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_M<3>	ENET_MDI3	ENET_MDI3:G:U43.43:J23.10:0 MIL:100 MIL		ENET 11 MIL SPACING	
LVDS Zo = 100 LOWER	CLKLVDS_LN	CLKLVDS_L	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4
	CLKLVDS_LP	CLKLVDS_L	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4
	LVDS_L0N	LVDS_L0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L0P	LVDS_L0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L1N	LVDS_L1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L1P	LVDS_L1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L2N	LVDS_L2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L2P	LVDS_L2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
UPPER	CLKLVDS_UN	CLKLVDS_U	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4
	CLKLVDS_UP	CLKLVDS_U	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4
	LVDS_U0N	LVDS_U0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U0P	LVDS_U0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U1N	LVDS_U1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U1P	LVDS_U1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U2N	LVDS_U2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U2P	LVDS_U2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
TMDS Zo = 100	TMDS_CLKN	CLKTMDS	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	5
	TMDS_CLKP	CLKTMDS	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	5
	TMDS_DN<0>	TMDS_D0		500.0000	100 OHM SPACING	8
	TMDS_DP<0>	TMDS_D0		500.0000	100 OHM SPACING	8
	TMDS_DN<1>	TMDS_D1		500.0000	100 OHM SPACING	8
	TMDS_DP<1>	TMDS_D1		500.0000	100 OHM SPACING	8
	TMDS_DN<2>	TMDS_D2		500.0000	100 OHM SPACING	8
	TMDS_DP<2>	TMDS_D2		500.0000	100 OHM SPACING	8
	ATI_TMDS_CLKN	ATI_CLKTMDS	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	5
	ATI_TMDS_CLKP	ATI_CLKTMDS	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	5
	ATI_TMDS_DN<0>	ATI_TMDS_D0		200.0000	100 OHM SPACING	8
	ATI_TMDS_DP<0>	ATI_TMDS_D0		200.0000	100 OHM SPACING	8
	ATI_TMDS_DN<1>	ATI_TMDS_D1		200.0000	100 OHM SPACING	8
	ATI_TMDS_DP<1>	ATI_TMDS_D1		200.0000	100 OHM SPACING	8
	ATI_TMDS_DN<2>	ATI_TMDS_D2		500.0000	100 OHM SPACING	8
	ATI_TMDS_DP<2>	ATI_TMDS_D2		500.0000	100 OHM SPACING	8
USB 1.1 Zo = 90	USB_DEM	USB_DE	USB_DE:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	USB_DEP	USB_DE	USB_DE:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	USB_DFM	USB_DF	USB_DF:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	USB_DFP	USB_DF	USB_DF:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
USB 2.0 Zo = 90	BT_USB_DM	BT_USB_D	BT_USB:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	BT_USB_DP	BT_USB_D	BT_USB:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	MODEM_USB_DM	MODEM_USB_D	MODEM_USB:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	MODEM_USB_DP	MODEM_USB_D	MODEM_USB:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	NEC_USB_DAM	USB_D1	USB_D1:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	
	NEC_USB_DAP	USB_D1	USB_D1:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	
	NEC_USB_DBM	USB_D2	USB_D2:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	
	NEC_USB_DBP	USB_D2	USB_D2:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	
POWER SUPPLIES	1772_CSSN	1772_CSS	1772_CSS:G:L:S:0 MIL:100 MIL			
	1772_CSSP	1772_CSS	1772_CSS:G:L:S:0 MIL:100 MIL			
	1772_CSIN	1772_CSI	1772_CSI:G:L:S:0 MIL:100 MIL			
	1772_CSIP	1772_CSI	1772_CSI:G:L:S:0 MIL:100 MIL			
	3V_SNSM	3V_SNS	3V_SNS:G:L:S:0 MIL:100 MIL			
	3V_SNSP	3V_SNS	3V_SNS:G:L:S:0 MIL:100 MIL			
	5V_SNSM	5V_SNS	5V_SNS:G:L:S:0 MIL:100 MIL			
	5V_SNSP	5V_SNS	5V_SNS:G:L:S:0 MIL:100 MIL			
THERMOSTAT	THERM1_DM		THERM1:G:L:S:0 MIL:100 MIL			
	THERM1_DP		THERM1:G:L:S:0 MIL:100 MIL			
	THERM2_DM		THERM2:G:L:S:0 MIL:100 MIL			
	THERM2_DP		THERM2:G:L:S:0 MIL:100 MIL			
	THERM1_M_DM	THERM1_MAIN	THERM1_MAIN:G:L:S:0 MIL:100 MIL			
	THERM1_M_DP	THERM1_MAIN	THERM1_MAIN:G:L:S:0 MIL:100 MIL			
	THERM2_M_DM	THERM2_MAIN	THERM2_MAIN:G:L:S:0 MIL:100 MIL			
	THERM2_M_DP	THERM2_MAIN	THERM2_MAIN:G:L:S:0 MIL:100 MIL			
	THERM1_A_DM	THERM1_ALT	THERM1_ALT:G:L:S:0 MIL:100 MIL			
	THERM1_A_DP	THERM1_ALT	THERM1_ALT:G:L:S:0 MIL:100 MIL			
	THERM2_A_DM	THERM2_ALT	THERM2_ALT:G:L:S:0 MIL:100 MIL			
	THERM2_A_DP	THERM2_ALT	THERM2_ALT:G:L:S:0 MIL:100 MIL			

PRIORITY: 3
PRIMARY LAYERS: 4,7 FOR CONTROLLED IMPEDANCE DIFF PAIRS
SECONDARY LAYERS: 2,9 FOR UNCONTROLLED IMPEDANCE DIFF PAIRS

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3MIL (TRACE WIDTH)
S = 11MIL (TRACE SEPERATION)
H = 16.8MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 106.2 OHMS
Zo(single) = 55.4 OHMS

Clear adjacent power plane!
Zo will be lower due to asymmetric stackup.

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3.1MIL (TRACE WIDTH)
S = 4.9MIL (TRACE SEPERATION)
H = 9.6MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 94 OHMS
Zo(single) = 50 OHMS

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3.9MIL (TRACE WIDTH)
S = 5.6MIL (TRACE SEPERATION)
H = 9.6MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 89.8 OHMS
Zo(single) = 46.6 OHMS

LAYERS 2 OR 9

SIGNAL CONSTRAINTS - PAGE 2

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6570 | REV. 01

SCALE NONE | SHT 37 OF 44

POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
MAIN/SLEEP	+24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+BATT	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23 39
	+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=6	MIN_NECK_WIDTH=6	39
	+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+2_5V_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	39
	+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP_VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30 31 39
	J38 +ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30 38
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30 38
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30 39
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30 39
	1772_DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		30
	1772_LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	30
	1772_LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		30
	1772_DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		30
	1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10		30
PMU	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	+4_85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		29 31
	+4_6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10		31 32
	+4_85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		31
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		31
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		25 29
MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24 32
	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24
TRACKPAD	+5V_TPAD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=10		23 39
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		23 39
VIDEO	+14V_INV	VOLTAGE=14V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	22 39
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
AUDIO	J39 +5V_MAIN_AUD	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 32
	J39 +3V_MAIN_AUD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 32
	J39 AUD_GND	VOLTAGE=0V	MIN_LINE_WIDTH=50		25
FAN	J40 +FAN_PWR	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 39
	FAN1_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	FAN2_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39

I/O AREA	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	IN	
	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN	CHGND1
INVERTER	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN	CHGND2
TRACKPAD	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN	CHGND3
LVDS	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN	CHGND4

ENET_CTAP_CHGND VOLTAGE=0V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=12

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 6 33 39
	CPU_AVDD	VOLTAGE=1.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 6 7 8 15 16 33
	I362 CPU_AVDD_VIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
	I363 CPU_AVDD_VOUT	VOLTAGE=1.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
DDR RAM	DDR_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		11
INTREPID	I348 +2_5V_INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	9 10 15 16
	+3V_INTREPID_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14
PLLS	+1_5V_INTREPID_PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	8 12 14
	+1_5V_INTREPID_PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	8
	+1_5V_INTREPID_PLL8	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
REFERENCE	INT_MEM_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		9
	INT_AGP_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		12 19
	INT_MEM_REF_H	VOLTAGE=0V	MIN_LINE_WIDTH=10		9
	UIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8		13
AIRPORT	+3V_AIRPORT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
CARDBUS	I365 +3V_SLEEP_PCCARD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
ATI M10	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	19 20 39
	+3V_GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 19 20 21
	+3V_GPU_FLT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+2_5V_GPU	VOLTAGE=2.5V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	21
	GPU_MEM_IO	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	19 21
	GPU_MEM_IO_FLT	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+2_5V_GPU_MEMCORE	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+1_8V_GPU	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	19 20 21
	+1_5V_AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 15 16 19 20 21
	+2_5V_GPU_PNLIO	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_8V_ATI_PVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20 21
	+1_5V_AGP_GPU	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_5V_GPU_VDD15	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	+1_8V_GPU_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_VDDDI	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	GPU_VCORE_VDDCI	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	+2_5V_GPU_A2VDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_PNLPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_PNLIO	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+2_5V_GPU_MCLK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_AVDDQ	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_MEMPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+3V_ATI_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	+3V_ATI_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	+GPU_VDD15_UF	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	I344 +2_5V_SLEEP_NECK1	VOLTAGE=2.5V	MIN_LINE_WIDTH=10		20
	I344 +3V_SLEEP_NECK	VOLTAGE=3V	MIN_LINE_WIDTH=10		34
	I344 +1_5V_AGP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		20
	I344 +1_8V_PVDD_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		20
	I345 GPU_VCORE_NECK	VOLTAGE=1.2V	MIN_LINE_WIDTH=10		20
	I345 +GPU_VDD15_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		20
	I345 +2_5V_SLEEP_NECK2	VOLTAGE=2.5V	MIN_LINE_WIDTH=10		34
	I345 +1_8V_SLEEP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		34
	I345 +1_5V_SLEEP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		34
	I346 +1_8V_ATI_TPVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	I346 +1_8V_GPU_TP_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
ETHERNET	+2_5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
88E1111	+2_5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
NEC USB2.0	+1_0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	I341 +3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
	I341 NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	17
FW	I342 LM2594_IN	VOLTAGE=33V	MIN_LINE_WIDTH=40	MIN_NECK_WIDTH=12	27
	I343 +FW_PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	+FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	I344 +FW_AMP_SENSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	
	+FW_PWR_OR	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	27 28
	I344 +FW_PWR1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	+FW_VP0	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28 39
	+FW_VP1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28 39
	+3V_FW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27 28
	+3V_FW_UF	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_PLLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	I345 FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	I345 FW_VDD_ON	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	1625_VSW	VOLTAGE=14V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+PBUS_JUMPER	VOLTAGE=14V	MIN_LINE_WIDTH=10		31
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		31
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		31
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		31
	1V20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	30 31
LTC3707 5V SWITCHER	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	32
	5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+5V_MAIN_JUMPER	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
3V SWITCHER	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+3V_MAIN_JUMPER	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		32
MAX1715 2.5V SWITCHER	2_5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	34
	2_5V_LX_F	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	34
	2_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	2_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	2_5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	2_5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
1.65V SWITCHER	1_5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8		34
	1_5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	34
	1_5V_LX_F	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	34
	1_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	1_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	1_5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	1_5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
CONTROL	1_5V_ILIM		MIN_LINE_WIDTH=8		34
	2_5V_ILIM		MIN_LINE_WIDTH=8		34
	MAX1715_TON		MIN_LINE_WIDTH=8		34
	MAX1715_SKIP		MIN_LINE_WIDTH=8		34
	MAX1715_REF	VOLTAGE=2.0V	MIN_LINE_WIDTH=8		34
	MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
MAX1717	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	33
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=200	MIN_NECK_WIDTH=10	33
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	33
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	33
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	33
	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	33
	VCORE_ILIM		MIN_LINE_WIDTH=8		33
	VCORE_REF		MIN_LINE_WIDTH=8		33
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8		33
	VCORE_CC		MIN_LINE_WIDTH=8		33
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		33 39
	VCORE_TIME		MIN_LINE_WIDTH=8		33
	VCORE_VGATE		MIN_LINE_WIDTH=8		14 33
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30		33
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8		33
	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		33
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8		33
	I431 VCORE_GNDA	VOLTAGE=0V	MIN_LINE_WIDTH=10		33
LTC1778	1778_VIN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1778_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1778_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	20
	1778_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	20
	1778_BST_RC	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	20
	1778_TG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1778_BG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	GPU_VCORE_SW	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	20
	GPU_VCORE_SW_F	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	20
	1778_ION		MIN_LINE_WIDTH=8		20
	1778_ITH		MIN_LINE_WIDTH=8		20
	1778_ITH_RC		MIN_LINE_WIDTH=8		20
	1778_VFB		MIN_LINE_WIDTH=8		20 39
	1778_FCB		MIN_LINE_WIDTH=8		20
	1778_VRNG		MIN_LINE_WIDTH=8		20
LTC3411	LTC3411_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	LTC3411_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
	1_8V_SW	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
	1_8V_SW_F	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
	1_8V_VFB		MIN_LINE_WIDTH=8		34
	LTC3411_ITH_RC		MIN_LINE_WIDTH=8		34
	LTC3411_ITH		MIN_LINE_WIDTH=8		34
	LTC3411_SYNC		MIN_LINE_WIDTH=8		34
	LTC3411_SHDN		MIN_LINE_WIDTH=8		34
LTC1962 INT PLLS	LTC1962_INT_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	14
CY28512D LMU CONN	I364 +3V_MAIN_SSCG	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	I364 +3V_MAIN_LMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23
OPT DRIVER	I367 +5V_SLEEP_OPT	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24

SIGNAL CONSTRAINTS - PAGE 3

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6570 | REV. 01

SCALE NONE | SHT 38 OF 44

FUNCTIONAL TEST POINTS

PROBES ARE ON BOTTOM SIDE. MINIMUM PAD/HOLE SIZE IS 25 MIL.
FUNC TEST IS ONLY PROPERTY USED BY THE TOOLS. FUNC QTY IS FOR REFERENCE AND LISTS THE NUMBER OF TEST POINTS ON THAT NET AND WITHIN THAT GROUP/CONNECTOR.
FUNC_DIST IS SIMILARLY USED TO DEFINE MAXIMUM DISTANCE FROM A CONNECTOR.

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
SCAN/TEST	J2 JTAG_ASIC_TMS	TRUE			13 26
	J3 JTAG_ASIC_TDI	TRUE			13
	J1 JTAG_ASIC_TDO_TP	TRUE			26
	J4 JTAG_ASIC_TCK	TRUE			13 26
	J6 JTAG_ASIC_TRST_L	TRUE			13 26
	J5 CPU_CHKSTP_OUT_L	TRUE			5
	J7 CPU_SRESET_L	TRUE			5
	J9 CPU_HRESET_L	TRUE			5 6 7
	J8 JTAG_CPU_TMS	TRUE			5 6
	J10 JTAG_CPU_TDI	TRUE			5 6
	J12 JTAG_CPU_TDO_TP	TRUE			5
	J11 JTAG_CPU_TCK	TRUE			5 6
	J13 JTAG_CPU_TRST_L	TRUE			5 6
	J18 INT_JTAG_TEI	TRUE			13
	J20 INT_TST_MONIN_PD	TRUE			13
	J19 INT_TST_MONOUT_TP	TRUE			13
	J21 INT_TST_PLLEN_PD	TRUE			13
INT I2C	J15 INT_I2C_CLK0	TRUE			6 11 13 23
	J14 INT_I2C_DATA0	TRUE			6 11 13 23
	J16 INT_I2C_CLK1	TRUE			13 14 25
	J17 INT_I2C_DATA1	TRUE			13 14 25
PWR/GND	L21 +PBUS	TRUE			38
	L21 +24V_PBUS	TRUE			38
	L25 GPU_VCORE	TRUE			19 20 38
	L24 1778_VFB	TRUE			20 38
	L27 CPU_VCORE_SLEEP	TRUE			5 6 33 38
	L26 VCORE_FB	TRUE			33 38
	L21 +1_8V_MAIN	TRUE			38
	L21 +2_5V_MAIN	TRUE			38
	L21 +5V_MAIN	TRUE	2		38 39
	L22 +5V_SLEEP	TRUE	2		38 39
	L22 +3V_MAIN	TRUE	4		23 38
		TRUE		1000	IN
	L22 +3V_PMU	TRUE			38
CARDBUS	K36 CBUS_DET_1_L	TRUE		2000	18
	K35 CBUS_DET_2_L	TRUE		2000	18
DVI	K37 TMDS_DN<0..2>	TRUE		1000	19 22 37
	K38 TMDS_DP<0..2>	TRUE		1000	19 22 37
	K40 TMDS_CONN_CLKN	TRUE		1000	22 36
	K39 TMDS_CONN_CLKP	TRUE		1000	22 36
	K42 VGA_R	TRUE		1000	22
	K41 VGA_G	TRUE		1000	22
	K44 VGA_B	TRUE		1000	22
	K43 VGA_HSYNC	TRUE		1000	22
	K46 VGA_VSYNC	TRUE		1000	22
	K45 DVI_DDC_CLK_UF	TRUE		1000	22
	K47 DVI_DDC_DATA_UF	TRUE		1000	22
	K48 DVI_HPD_UF	TRUE		1000	22
	K49 +5V_DDC_SLEEP	TRUE		2000	22 38
		TRUE	2	2000	IN
CHGND1		TRUE	6	1000	IN
LVDS	K52 LVDS_L0N	TRUE		1000	20 22 37
	K51 LVDS_L0P	TRUE		1000	20 22 37
	K53 LVDS_L1N	TRUE		1000	20 22 37
	K55 LVDS_L1P	TRUE		1000	20 22 37
	K54 LVDS_L2N	TRUE		1000	20 22 37
	K57 LVDS_L2P	TRUE		1000	20 22 37
	K56 CLKLVDS_LN	TRUE		1000	20 22 37
	K58 CLKLVDS_LP	TRUE		1000	20 22 37
	K59 LVDS_DDC_CLK	TRUE		1000	20 22
	K60 LVDS_DDC_DATA	TRUE		1000	20 22
	K62 +3V_LCD	TRUE	2	2000	22 38
	L22 +3V_SLEEP	TRUE		2000	38 39
		TRUE	2	2000	IN
CHGND4		TRUE	6	1000	IN
INVERTER	K67 +14V_INV	TRUE		2000	22 38
	K66 +5V_INV_SW	TRUE		2000	22 38
	K68 BRIGHT_PWM	TRUE		2000	22
	K24 INV_GND	TRUE		2000	22
		TRUE		1000	IN
S-VIDEO	K70 TV_C	TRUE		2000	22
	K72 TV_Y	TRUE		2000	22
	K71 TV_COMP	TRUE		2000	22
	K73 TV_GND1	TRUE		2000	22 38
	K74 TV_GND2	TRUE		2000	22 38
LIO	K76 INT_I2S0_SND_TO_DAC	TRUE		1000	14 25
	K75 INT_I2S0_SND_LRCLK	TRUE		1000	14 25
	K78 INT_I2S0_SND_MCLK	TRUE		1000	14 25 35
	K83 INT_I2S0_SND_SCLK	TRUE		1000	14 25
	K82 INT_I2S0_SND_FROM_ADC	TRUE		1000	14 25
	K77 SND_HP_MUTE_L	TRUE		1000	14 25
	K79 SND_AMP_MUTE	TRUE		1000	25
	K84 SND_HW_RESET_L	TRUE		1000	14 25
	K85 SND_HP_SENSE_L	TRUE		1000	14 25
	K86 SND_LIN_SENSE_L	TRUE		1000	14 25
	K81 INT_I2C_CLK2	TRUE		1000	14 25
	K80 INT_I2C_DATA2	TRUE		1000	14 25
	K87 ADAPTER_DET	TRUE		1000	25 29
	K88 CHARGE_LED_L	TRUE		1000	25 29
	K89 NEC_LUSB_OCI_UF	TRUE		1000	17 25
	K90 NEC_LUSB_PPON	TRUE		1000	17 25
	L22 +5V_MAIN	TRUE	2	2000	38 39
	L22 +5V_SLEEP	TRUE	2	3000	38 39
	L22 +3V_SLEEP	TRUE		2000	38 39

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
USB	K94 NEC_USB_DAM	TRUE			17 25 37
	K96 NEC_USB_DAP	TRUE			17 25 37
	K95 NEC_USB_DBM	TRUE			17 25 37
	K97 NEC_USB_DBP	TRUE			17 25 37
	K98 BT_USB_DM	TRUE			14 25 37
	K99 BT_USB_DP	TRUE			14 25 37
	K10 MODEM_USB_DM	TRUE			14 25 37
	K10 MODEM_USB_DP	TRUE			14 25 37
RT. USB	K10 NEC_RUSB_PPON	TRUE			17 25
	K10 NEC_RUSB_OCI_UF	TRUE			17 25
WIRELESS	K10 PCI_AD<0..31>	TRUE		1000	9 12 17 18 24 37
	K10 PCI_FRAME_L	TRUE		1000	12 17 18 24 37
	K10 PCI_TRDY_L	TRUE		1000	12 17 18 24 37
	K10 PCI_IRDY_L	TRUE		1000	12 17 18 24 37
	K10 PCI_DEVSEL_L	TRUE		1000	12 17 18 24 37
	K10 PCI_STOP_L	TRUE		1000	12 17 18 24 37
	K11 PCI_PAR	TRUE		1000	12 17 18 24 37
	K11 AIRPORT_PCI_REQ_L	TRUE		1000	12 24
	K11 AIRPORT_PCI_GNT_L	TRUE		1000	12 24
	K11 AIRPORT_PCI_INT_L	TRUE		1000	14 24
	K11 MAIN_RESET_L	TRUE		1000	14 17 18 19 24 29
	K11 CLK33M_AIRPORT	TRUE		1000	12 24 35
	K11 PMU_PME_L	TRUE		1000	14 17 24 29
	K11 ROM_ONBOARD_CS_L	TRUE		1000	9
	K11 ROM_OE_L	TRUE		1000	9 12
	K11 ROM_CS_L	TRUE		1000	9 12
	K11 ROM_RW_L	TRUE		1000	9 12
	K12 RF_DISABLE_L	TRUE		1000	24
	K12 AIRPORT_CLKRUN_L	TRUE		1000	24
	K12 +3V_AIRPORT	TRUE	4	2000	38
		TRUE	6	1000	IN
OPTICAL	K12 EIDE_OPTICAL_DATA<0..15>	TRUE		2000	24 37
	K12 EIDE_OPTICAL_DMA_RQ	TRUE		2000	24 37
	K12 EIDE_OPTICAL_READ_L	TRUE		2000	24 37
	K12 EIDE_OPTICAL_DMAACK_L	TRUE		2000	24 37
	K12 EIDE_OPTICAL_ADDR<0..2>	TRUE		2000	24 37
	K12 EIDE_OPTICAL_CS0_L	TRUE		2000	24 37
	K12 EIDE_OPTICAL_CS1_L	TRUE		2000	24 37
	K12 EIDE_OPTICAL_RST_L	TRUE		2000	24 37
	K12 EIDE_OPTICAL_WR_L	TRUE		2000	24 37
	K13 EIDE_OPTICAL_IOCHRDY	TRUE		2000	24 37
	K13 EIDE_OPTICAL_INT	TRUE		2000	24 37
TRACKPAD	K13 +5V_TPAD_SLEEP	TRUE		3000	23 38
	K13 TPAD_F_TXD	TRUE		3000	23
	K13 TPAD_F_RXD	TRUE		3000	23
	K13 LID_CLOSED_L	TRUE		3000	23
	K13 +3V_HALL_EFFECT	TRUE		3000	23 38
	K13 SOFT_PWR_ON_L	TRUE		3000	22 23 29 33
MODEM/ SERIAL	K14 COMM_RESET_L	TRUE		4000	14 25
	K14 COMM_SHUTDOWN	TRUE		4000	14 25
	K14 COMM_RING_DET_L	TRUE		4000	14 25 29
	K14 COMM_TXD_L	TRUE		4000	14 25
	K14 COMM_TRXC	TRUE		4000	14 25
	K14 COMM_GPIO_L	TRUE		4000	14 25
	K14 COMM_DTR_L	TRUE		4000	14 25
	K14 COMM_RTS_L	TRUE		4000	14 25
	K14 COMM_RXD	TRUE		4000	14 25
KEYBOARD	K14 KBD_ID	TRUE		3000	23 29
	K15 KBD_INTL	TRUE		3000	23
	K15 KBD_JIS	TRUE		3000	23
	K15 KBD_CAPSLOCK_LED	TRUE		3000	23
	K15 KBD_NUMLOCK_LED	TRUE		3000	23
	K15 KBD_FUNCTION_L	TRUE		3000	23 29
	K15 KBD_COMMAND_L	TRUE		3000	23 29
	K15 KBD_OPTION_L	TRUE		3000	23 29
	K15 KBD_CONTROL_L	TRUE		3000	23 29
	K15 KBD_SHIFT_L	TRUE		3000	23 29
	K15 KBD_X<0..9>	TRUE		3000	23 29
	K15 KBD_Y<0..7>	TRUE		3000	23 29
BATTERY	K16 +BATT_POS	TRUE	(100 MIL PROBE PREFERRED)	1000	30 38
	K16 BATT_NEG	TRUE	(100 MIL PROBE PREFERRED)	1000	30 38
	K16 BATT_CLK	TRUE		1000	30
	K16 BATT_DATA	TRUE		1000	30
	K16 PMU_BATT_DET_L	TRUE		1000	29 30
FANS	K16 +FAN_PWR	TRUE		3000	25 38
	K16 FAN1_TACH	TRUE		3000	25
	K16 FAN2_TACH	TRUE		3000	25
	K17 FAN1_GND	TRUE		3000	38
	K17 FAN2_GND	TRUE		3000	38
ETHERNET	K17 MDI_P<0..3>	TRUE		1000	26 37
	K17 MDI_M<0..3>	TRUE		1000	26 37
FIREWIRE	K17 FW_TPO0P	TRUE		1000	27 28 37
	K17 FW_TPO0N	TRUE		1000	27 28 37
	K17 FW_TPO0R	TRUE		1000	28
	K17 FW_TPI0P	TRUE		1000	27 28 37
	K17 FW_TPI0N	TRUE		1000	27 28 37
	K18 +FW_VP0	TRUE		1000	28 38
	K18 FW_VGND	TRUE		1000	39

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
FIREWIRE (CONT.)	K18 FW_TPO1P	TRUE		1000	28 37
	K18 FW_TPO1N	TRUE		1000	28 37
	K18 FW_TPI1P	TRUE		1000	28 37
	K18 FW_TPI1N	TRUE		1000	28 37
	K18 +FW_VP1	TRUE		1000	28 38
	K18 FW_VGND	TRUE		1000	39
DC PWR IN	K18 +ADAPTER	TRUE	3 (100 MIL PROBE PREFERRED)	1000	30 31 38
LMU/ALS	K25 ST7_SLEEP_LED_H	TRUE			23
	K25 PMU_SLEEP_LED	TRUE			23
	K25 PMU_LID_CLOSED_L	TRUE			23 29
	K25 LMU_DETECT	TRUE			23
		TRUE	6	1000	IN
MISC.			(100 MIL PROBE PREFERRED)		
	K19 SLEEP_LED	TRUE			23
	K19 PMU_KB_RESET_L	TRUE			29
	K19 SLEEP	TRUE			23 25 29 32 34
	K19 PMU_CPU_HRESET_L	TRUE			6 29
	K19 BB_RESET_L	TRUE			6
	K24 +3V_PMU_RESET	TRUE			29 33

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	01
SCALE: NONE	SHT 39 OF 44	

REVISION HISTORY

Proto Release

10/27/03 - 1. Schematic originated from Q16 MLB

11/10/03 - 1. Replace U56 symbol
2. Connect OVDDSENSE to MAXBUS_SLEEP
3. Modify SRN0, SRN1 and IARTRY0 connection
4. Connect VDD(Page 6) to CPU_VCORE_SLEEP(PAGE 5)
5. Connect SENSEVDD to CPU_VCORE_SLEEP
6. Connect SENSEGND to GND
7. Add 4 pcs 0 ohm resistor for AMD BootRom issue (R1,R194,R236,R271)
8. Connect TEMP_ANODE and TEMP_CATHODE to AD7460
9. Modify CPU PLL config
10. Add 10 ohm resistor on CG_FSEL Interpid side(R450)
11. Replace U47 symbol
12. Change R743 from 2m ohm to 1m ohm
13. Change C774,C781,C788,C793,C797,C802 from 220uF to 330uF
14. Change R748 from 410 ohm to 10 ohm

12/01/03 - 1. Modify CPU_VCORE setting.

12/02/03 - 1. Modify CPU_BTR CPU_VCORE VID setting

12/05/03 - 1. Add CPU_AVDD LDO (Page 5)
2. Change Q45 and Q41 to IRF7805 (376S0035)
3. Change Q47 and Q42 to IRF7811W (376S0104)
4. Change R402 and R409 to 4.7ohm resistors
5. Connect INT_TDO from intrepid to Cypress Chip PD* (U31)

12/12/03 - 1. Add R468 and R601 for MAX1715 2.5V adjust
2. Modify CPU_VCORE setting to Motorola new spec
3. Modify LDO power sequence

12/16/03 - 1. Add 10K pull down for INT_TDO on page 13

12/17/03 - 1. Change LDO Vin from +3V_MAIN to +3V_SLEEP
2. Connect INT_TDO from Intrepid to Marvell 88E1111(U43)
3. Add R755,R756,R758,R759 for power rail

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	01
SCALE: NONE	SHT 40	44

```
PMU_AC_IN          29B4<>
PMU_BATT0_DET_L    29B4<>
PMU_BATT1_DET_L_PU  29B4<> 29D2<
PMU_BATT_DET_L     29B3< 29D2< 30A4<> 39A3>
PMU_BYTE           29B6< 29C7<
PMU_CAPSLOCK_LED_L  29C4<>
PMU_CHARGE_V       29C4<> 30B8<>
PMU_CHRG_BATT_G    29C4<> 30A8<>
PMU_CLK            14C2<> 29C4<>
PMU_CNVSS          29B6< 29C7<
PMU_CPU_RESET_L    6A2< 6C3<> 29C4<> 39C1>
PMU_EPM            29C4<> 29D2<
PMU_FROM_INT       14C2<> 29C4<>
PMU_I2C_CLK        29B4<> 29C2<
PMU_I2C_DATA       29B4<> 29C2<
PMU_INT_L          14B5<> 14B7< 29B6<>
PMU_INT_NMI        14B5<> 14B7< 29D4<>
PMU_KB_RESET_IN1   29A7<>
PMU_KB_RESET_IN2   29A7<>
PMU_KB_RESET_L     29A6> 29B7< 39C1>
PMU_LID_CLOSED_L   23B< 23D6<> 29B2< 29C4<> 39D1>
PMU_NMI_BUTTON_L   29C2< 29C4<>
PMU_NMI_L          29C2< 29C4<>
PMU_RUNLOCK_LED_L  29C6<>
PMU_OOPS           29B2< 29B4<>
PMU_PME_L          14A5<> 17A8< 24D5<> 29B2< 29C4<>
                   39C3>
PMU_POWERUP_OK     29B4<> 29D2<
PMU_POWER_UP_L     28C8<> 29C6<> 29D7< 32B8<
PMU_RSQ_L          14B7< 14C2> 29C4<>
PMU_RESET_BUTTON_L  23A7< 29C4<> 29D2<
PMU_RESET_L        29B6<>
PMU_SLEEP_LED      23C7<> 23D6<> 39D1>
PMU_SLEEP_LED_L    23C8<> 29C4<>
PMU_SMB_CLK        29B4<> 29C2< 30A3<
PMU_SMB_DATA       29B4<> 29C2< 30A2<
PMU_TO_INT         14C2<> 29C4<>
POWER_UP           28D7<>
POWER_VALID        29B2< 29C4<>
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RAM_ADDR<12..0>    35A5>
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RAM_ADDR<2>        9B4< 11B3<> 11B6<>
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RAM_DATA_B<7>      10C8<> 11D5<>
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RAM_DATA_B<22>     10C6<> 11C3<>
RAM_DATA_B<23>     10C6<> 11C3<>
RAM_DATA_B<24>     10C6<> 11C5<>
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RAM_DATA_B<63..56>  35A5>
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RAM_DQM_B<4>       10C4<> 11B3<> 35B5>
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RAM_DQS_A<2>       10B6<> 11C8<> 35C5>
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RAM_DQS_A<6>       10B2<> 11A8<> 35B5>
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RAM_DQS_B<1>       10C8<> 11D5<> 35C5>
RAM_DQS_B<2>       10C6<> 11C5<> 35C5>
RAM_DQS_B<3>       10C6<> 11C5<> 35C5>
RAM_DQS_B<4>       10C4<> 11B5<> 35B5>
RAM_DQS_B<5>       10C4<> 11B5<> 35B5>
RAM_DQS_B<6>       10C2<> 11A5<> 35B5>
RAM_DQS_B<7>       10C2<> 11A5<> 35A5>
RAM_RAS_L          9A4< 11B3<> 11B6<> 35A5>
RAM_WE_L           9A4< 11B5<> 11B8<> 35A5>
RESET_VREF         6C3<>
RF_DISABLE_L       24D6<> 39C3>
ROM_CS_L           9B3< 12A4< 39C3>
ROM_CS_TP_L        9C3< 24B6<>
ROM_OE_L           9B3< 12A4< 39C3>
ROM_OE_TP_L        9B3< 24C5<>
ROM_ONBOARD_CS_L   9B3< 39C3>
ROM_ONBOARD_CS_TP_L  9B3< 24C6<>
ROM_RW_L           9B3< 12A4< 39C3>
ROM_RW_TP_L        9B3< 24C6<>
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SI_HPD             19C4<
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SLEEP_LED_UF       23D3<
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SLEEP_LS5_EN_L     32A5<>
SLEEP_L_LS5        18D5< 20A7<> 26A8<> 32A5<> 33C7<>
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SLEEP_L_LS5_EN_L   32A6<>
SLEEP_L_LS5_INV    34A3< 34C2< 34C8<>
SLEEP_L_LS5_NET    32B3<> 34C8<>
SLEEP_NET          32A3<>
SLEEP_NET_INV      32A3<>
SND_AMP_MUTE       25C7<> 25D6<> 39A6>
SND_AMP_MUTE_CTRL  25B5<> 25D6<>
SND_AMP_MUTE_L     14B5<> 25D5<>
SND_HP_MUTE        25C5<>
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SND_HP_SENSE_L     14B5<> 25C8<> 39A6>
SND_HW_RESET_L     14A7< 14B5<> 25D7<> 39A6>
SND_LIN_SENSE_L    14B5<> 25C8<> 39A6>
SOFT_PWR_ON_L      22D1<> 23A3< 29A8< 29C6<> 29D7<
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ST7_SLEEP_LED_H    23C5<> 23C6<> 23D6<> 39D1>
STOP_ASP_L         12D2< 12D4<>
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SYSCLK_CPU_UF      8A5<> 35D1>
SYSCLK_DDRCLK_A0   9D4< 11D8<> 35D1>
SYSCLK_DDRCLK_A0_L  9D4< 11D8<> 35C1>
SYSCLK_DDRCLK_A0_L_UF  9B6<> 9D5< 35D1>
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SYSCLK_DDRCLK_B1_L_UF  9B6<> 9D5< 35D1>
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SYSTEM_CLK_EN      14A5< 14B6< 29C4<>
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THERM1_M_DM        25B7< 25B8< 37A2>
THERM1_M_DP        25B7< 25B8< 37A2>
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THERM2_DM          25A5< 25A6< 25B5<> 25B6< 37A2>
THERM2_DP          25A5< 25A6< 25B5<> 25B6< 37A2>
THERM2_M_DM        25B7< 25B8< 37A2>
THERM2_M_DP        25B7< 25B8< 37A2>
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THERM_L_OC         25B1<> 29B4<>
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TMDS_CLKP          19B1< 19C1< 19D2< 22C8<> 37C2>
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TMDS_CONN_CLKP     22C7<> 22C7<> 36C1> 39C6>
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UIDE_RST_L         13C7<> 24A4< 37C5>
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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SCALE: NONE	SHT ?x2 OF ?	

*** Part Cross-Reference for the entire design ***

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RP40	RPAX10P2C	23
RP41	RPAK4P	29
RP42	RPAX10P2C	23
RP43	RPAK4P	17
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RP45	RPAK4P	17
RP46	RPAK10P2C	6
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RP60	RPAK4P	19
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U2	NC7832	22
U3	AMP_MAX4172	30
U4	PWR_CNTRL_TPS2211	18
U5	FAN2558	5
U6	MAX1772	30
U7	MAX1717	33
U8	PCI5100GU	18
U9	SN74AUC1G08	6
U10	SN74AUC1G08	6
U11	FEPB_1NKH	9
U12	SN74AUC1G04	7
U13	LTC1625	31
U14	COMPARATOR_LMC7211	31
U15	PI3B3257	33
U16	CBTV4020	10
U17	UPD720101_FBGA	17
U18	CBTV4020	10
U19	MAX1715	34
U20	NC7832	29
U21	741125	23
U22	VREG_LP2951	31
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U26	MAX6804	29
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U28	CBTV4020	10
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U30	CLK_GEN_CY25811	19
U31	CLK_GEN_CY28512	14
U32	LDC1778	20
U33	COMPARATOR_LMC7211	29
U34	VREG_MM1571J	21
U35	LDC3707	32
U36	T8B81BAJA	27
U37	VREG_LM2594	27

U38	VREG_LP1962	27
U39	741G32	22
U40	741G32	22
U42	COMPARATOR_LMC7211	22
U43	TRANSCEIVER_88E1111	26
U44	LTC1761	27
U45	LTC3405	26
U46	LTC3411	34
U47	RADE_MBLTY_H11_CBP64_667	19 20 21
U48	TRA_SI4467BDQ	34
U49	VREG_LT1962	14
U50	TRA_SI3447DV	34
U51	INTREPID 8 9 12 13 14 15	
U52	EEPROM_32KX8_M24256B	6
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U54	AT90S1200	6
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U56	APOLLO_MPC7447A_360	5 6
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XW14	SHORT	22
XW15	SHORT	22
XW16	JUMPER	32
XW17	SHORT	34
XW18	JUMPER	34
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XW32	SHORT	32
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Y2	CRYSTAL	14
Y3	CRYSTAL_4PIN	29
Y4	CRYSTAL	29
Y5	CRYSTAL_4PIN	26
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