

- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
				2012-02-23

SCHEM, MLB, J13

2/23/12

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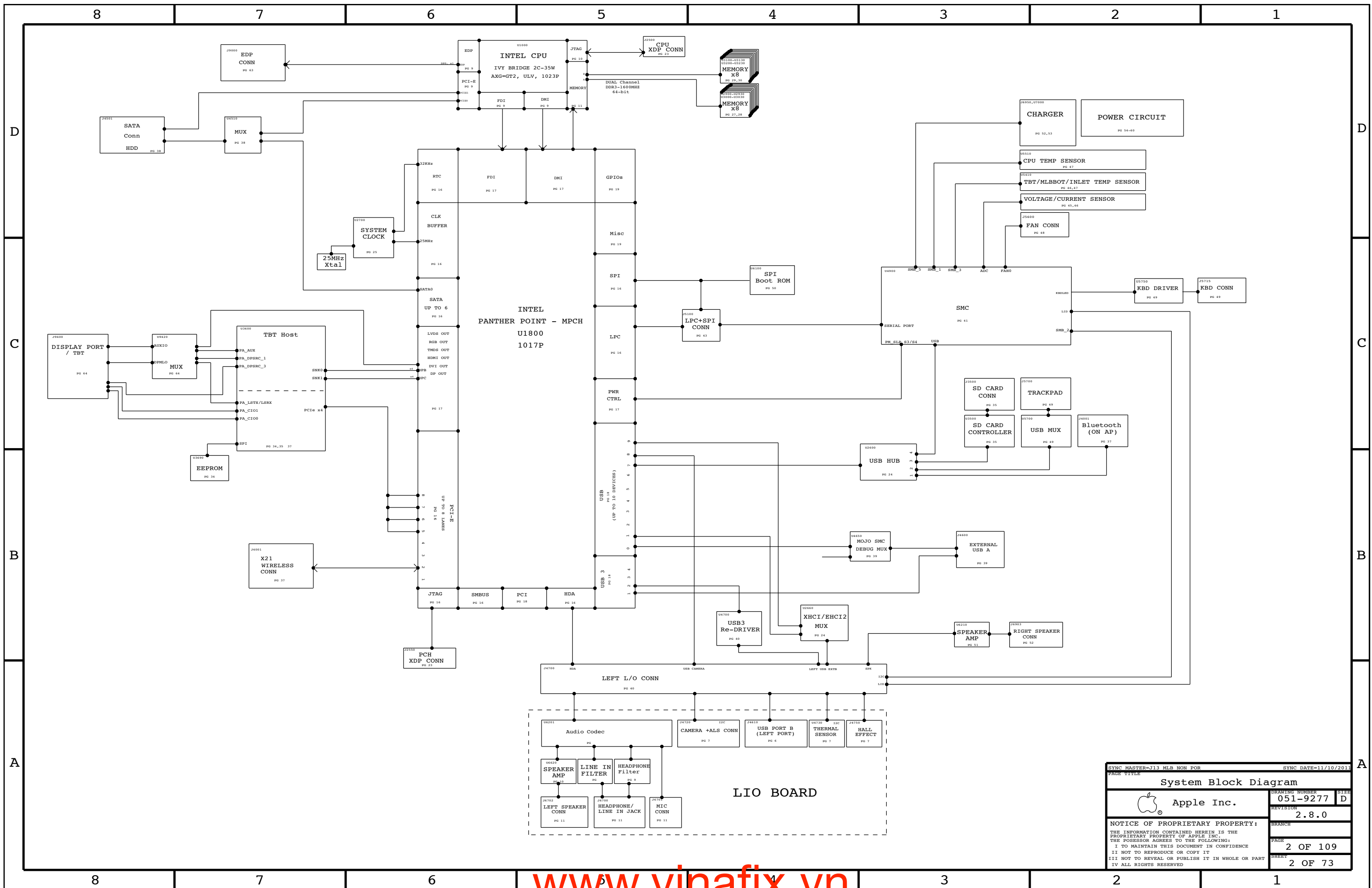
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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9277	1	SCHEM, MLB, J13	SCH	CRITICAL	
820-3209	1	PCBF, MLB, J13	PCB	CRITICAL	

DRAWING TITLE=MLB
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DRAWING TITLE		SCHEM, MLB, J13	
DRAWING NUMBER		051-9277	SIZE D
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SYNC MASTER=J13 MLB NON POR		SYNC DATE=11/10/2011	
System Block Diagram			
Apple Inc.		DRAWING NUMBER	SIZE
		051-9277	D
		REVISION	
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
085-3939	J13 MLB DEVELOPMENT BOM	J13_DEVEL_BOM
607-9090	CMN PTS,PCBA,MLB,J13	J13_CMNPTS
639-3552	PCBA,MLB,1.7GHZ,SA 4GB,J13	J13_CMNPTS,EEEE:DYRK,CPU:1.7GHZ,DDR3:SAMSUNG_4GB
639-3553	PCBA,MLB,1.5GHZ,SA 4GB,J13	J13_CMNPTS,EEEE:DYRN,CPU:1.5GHZ,DDR3:SAMSUNG_4GB
639-3554	PCBA,MLB,1.5GHZ,HY 4GB,J13	J13_CMNPTS,EEEE:DYRN,CPU:1.5GHZ,DDR3:HYNIX_4GB
639-3555	PCBA,MLB,1.5GHZ,HY 8GB,J13	J13_CMNPTS,EEEE:DYRL,CPU:1.5GHZ,DDR3:HYNIX_8GB
639-3556	PCBA,MLB,1.7GHZ,HY 8GB,J13	J13_CMNPTS,EEEE:DYRK,CPU:1.7GHZ,DDR3:HYNIX_8GB
639-3557	PCBA,MLB,1.7GHZ,HY 4GB,J13	J13_CMNPTS,EEEE:DYRN,CPU:1.7GHZ,DDR3:HYNIX_4GB
639-3645	PCBA,MLB,1.5GHZ,EL 8GB,J13	J13_CMNPTS,EEEE:F0TC,CPU:1.5GHZ,DDR3:ELPIDA_8GB
639-3644	PCBA,MLB,1.7GHZ,EL 8GB,J13	J13_CMNPTS,EEEE:F0TD,CPU:1.7GHZ,DDR3:ELPIDA_8GB
639-3760	PCBA,MLB,1.8GHZ,SA 4GB,J13	J13_CMNPTS,EEEE:F25Q,CPU:1.8GHZ,DDR3:SAMSUNG_4GB
639-3761	PCBA,MLB,1.8GHZ,HY 8GB,J13	J13_CMNPTS,EEEE:F25T,CPU:1.8GHZ,DDR3:HYNIX_8GB
639-3762	PCBA,MLB,1.8GHZ,HY 4GB,J13	J13_CMNPTS,EEEE:F25T,CPU:1.8GHZ,DDR3:HYNIX_4GB
639-3763	PCBA,MLB,1.8GHZ,EL 8GB,J13	J13_CMNPTS,EEEE:F25P,CPU:1.8GHZ,DDR3:ELPIDA_8GB
639-3764	PCBA,MLB,2.0GHZ,SA 4GB,J13	J13_CMNPTS,EEEE:F25N,CPU:2.0GHZ,DDR3:SAMSUNG_4GB
639-3765	PCBA,MLB,2.0GHZ,HY 8GB,J13	J13_CMNPTS,EEEE:F25N,CPU:2.0GHZ,DDR3:HYNIX_8GB
639-3766	PCBA,MLB,2.0GHZ,HY 4GB,J13	J13_CMNPTS,EEEE:F25N,CPU:2.0GHZ,DDR3:HYNIX_4GB
639-3767	PCBA,MLB,2.0GHZ,EL 8GB,J13	J13_CMNPTS,EEEE:F25V,CPU:2.0GHZ,DDR3:ELPIDA_8GB
639-3790	PCBA,MLB,1.7GHZ,SA 8GB,J13	J13_CMNPTS,EEEE:F27V,CPU:1.7GHZ,DDR3:SAMSUNG_8GB
639-3791	PCBA,MLB,1.8GHZ,SA 8GB,J13	J13_CMNPTS,EEEE:F27Q,CPU:1.8GHZ,DDR3:SAMSUNG_8GB
639-3792	PCBA,MLB,2.0GHZ,SA 8GB,J13	J13_CMNPTS,EEEE:F27B,CPU:2.0GHZ,DDR3:SAMSUNG_8GB
639-3793	PCBA,MLB,1.7GHZ,EL 4GB,J13	J13_CMNPTS,EEEE:F27W,CPU:1.7GHZ,DDR3:ELPIDA_4GB
639-3794	PCBA,MLB,1.8GHZ,EL 4GB,J13	J13_CMNPTS,EEEE:F27Y,CPU:1.8GHZ,DDR3:ELPIDA_4GB
639-3795	PCBA,MLB,2.0GHZ,EL 4GB,J13	J13_CMNPTS,EEEE:F27Y,CPU:2.0GHZ,DDR3:ELPIDA_4GB

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DYRK]	CRITICAL	EEEE:DYRK
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DYRL]	CRITICAL	EEEE:DYRL
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DYRM]	CRITICAL	EEEE:DYRM
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DYRN]	CRITICAL	EEEE:DYRN
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DYRP]	CRITICAL	EEEE:DYRP
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DYRQ]	CRITICAL	EEEE:DYRQ
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F0TC]	CRITICAL	EEEE:F0TC
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F0TD]	CRITICAL	EEEE:F0TD
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F25N]	CRITICAL	EEEE:F25N
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F25P]	CRITICAL	EEEE:F25P
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F25Q]	CRITICAL	EEEE:F25Q
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F25R]	CRITICAL	EEEE:F25R
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F25T]	CRITICAL	EEEE:F25T
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F25V]	CRITICAL	EEEE:F25V
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F25W]	CRITICAL	EEEE:F25W
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F25Y]	CRITICAL	EEEE:F25Y
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F27Q]	CRITICAL	EEEE:F27Q
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F27R]	CRITICAL	EEEE:F27R
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F27T]	CRITICAL	EEEE:F27T
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F27V]	CRITICAL	EEEE:F27V
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F27W]	CRITICAL	EEEE:F27W
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F27Y]	CRITICAL	EEEE:F27Y

Sub BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-3939	1	J13 MLB DEVELOPMENT	DEVEL	CRITICAL	DEVEL_BOM
607-9090	1	CMN PTS,PCBA,MLB,J13	CMNPTS	CRITICAL	J13_CMNPTS

SYNC MASTER=J13 MLB SYNC DATE=07/27/2011

Revision History

DRAWING NUMBER	051-9277	SIZE	D
REVISION	2.8.0	BRANCH	
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J13 BOM GROUPS

BOM GROUP	BOM OPTIONS
J13_COMMON	ALTERNATE, COMMON, J13_MISC, J13_DEBUG:ENG, J13_PROGPARTS, USBHUB2514B, EDP:YES, PCH_C1
J13_MISC	CPOMER_BLD:NO, BUR_NONREM,TWT, HNS:YES, PPSV2_DCN:NO, TPAD_PCH:NO, SKIP_SV3V1:INVALID, RFWP:14, TRVY:P15V, LVDR3_BH:YES, ARG_ACOUSTIC:NO
J13_PROGPARTS	BOOTROM_PROG, SMC_PROG, TBTROM:PROG
J13_DEVEL:ENG	ALTERNATE, MLT:ENG, XDP_CONN, XDP_CPU:RPM, XDP_PCH, LPCPLUS, DORVREF_DAC, VREFQ:ML3, VREFCA:LDO, S0POOD0_1SL, S3_S0_LED, VCCIOISNS_ENG, AIRPORTISNS_ENG, HDDISNS_ENG, LCDKBLTISNS_ENG
J13_DEVEL:PVT	LPCPLUS, XDP_CONN
J13_DEBUG:ENG	DEVEL_BOM, M0J0: YES, XDP
J13_DEBUG:PVT	DEVEL_BOM, MLT:PROG, M0J0: YES, XDP, XDP_CPU:RPM, VREFQ:LDO, VREFCA:LDO, VCCIOISNS_PROG, AIRPORTISNS_PROG, HDDISNS_PROG, LCDKBLTISNS_PROG
J13_DEBUG:PROG	MLT:PROG, M0J0: YES, XDP, XDP_CPU:RPM, VREFQ:LDO, VREFCA:LDO, LPCPLUS, VCCIOISNS_PROG, AIRPORTISNS_PROG, HDDISNS_PROG, LCDKBLTISNS_PROG
DDR3:HYNIX_4GB	RAMCFG0:L, RAMCFG1:L, RAMCFG2:L, RAMCFG3:L, DRAM_TYPE:HYNIX_4GB
DDR3:HYNIX_8GB	RAMCFG0:L, RAMCFG1:L, RAMCFG2:H, RAMCFG3:L, DRAM_TYPE:HYNIX_8GB
DDR3:SAMSUNG_4GB	RAMCFG0:L, RAMCFG1:H, RAMCFG2:L, RAMCFG3:L, DRAM_TYPE:SAMSUNG_4GB
DDR3:SAMSUNG_8GB	RAMCFG0:L, RAMCFG1:H, RAMCFG2:H, RAMCFG3:L, DRAM_TYPE:SAMSUNG_8GB
DDR3:ELPIDA_8GB	RAMCFG0:H, RAMCFG1:H, RAMCFG2:H, RAMCFG3:L, DRAM_TYPE:ELPIDA_8GB
DDR3:ELPIDA_4GB	RAMCFG0:H, RAMCFG1:H, RAMCFG2:L, RAMCFG3:L, DRAM_TYPE:ELPIDA_4GB

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
3358065	1	IC, SERIAL SPI EEPROM, 256KBIT, 20MHZ, MLPS	U3690	CRITICAL	TBTROM:BLANK
34183475	1	IC, EEPROM, CR, V24-1, J11/J13	U3690	CRITICAL	TBTROM:PROG
33881098	1	IC, SMC12-A3, 40MHZ/50KOPS MCU, 9X9, 1578GA	U4900	CRITICAL	SMC_BLANK
33881065	1	IC, SMC12-49MHZ/50KOPS MCU, 9X9, 1578GA	U4900	CRITICAL	SMC_BLANK
34183433	1	IC, SMC_V2-1A43, Proto18, J13	U4900	CRITICAL	SMC_PROG
33580809	1	64 MBIT SPI SERIAL SERIAL 1/0 FLASH, M0J0:ENG	U6100	CRITICAL	BOOTROM_BLANK
33580803	1	64 MBIT SPI SERIAL SERIAL 1/0 FLASH, M0J0:PVT	U6100	CRITICAL	BOOTROM_BLANK
34183482	1	IC, EFI ROM, PROTO18, J13 J11	U6100	CRITICAL	BOOTROM_PROG

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
37680855	37680613		ALL	Diodes alt to Toshiba
37680977	37680859		ALL	Diodes alt to Toshiba
37680972	37680612		ALL	Diodes alt to Toshiba
13880676	13880691		ALL	Murata alt to Samsung
37180709	37180652		ALL	ESP alt to NXP
13880671	13880673		ALL	Taiyo alt to Murata
37680790	37680928		ALL	TI alt to Fairchild
15281462	15281295		ALL	Toko alt for NEC inductor
15281085	15281307		ALL	Toko alt for Cystec
13880703	13880648		ALL	Murata alt to Taiyo Yuden
13880684	13880660		ALL	Murata alt to Taiyo Yuden
15281493	15281300		ALL	Colicraft alt to Murata

35383238	35381428		ALL	Intersil alt to OPAL333
37280186	37280185		ALL	ESP alt to Diodes
37681053	37680604		ALL	Diodes alt to Fairchild
37680855	37680613		ALL	Diodes alt to Toshiba
37680903	37680796		ALL	Fairchild alt to Siliconix
19780431	19780432		ALL	Epson alt to NDK
33784198	33784197		ALL	TDP 1.5GHZ alt to Nominal
33784236	33784196		ALL	TDP 1.7GHZ alt to Nominal
37180713	37180958		ALL	Diodes alt to ST Micro
12880333	998-4435		ALL	Sanyo alt to Kemet
12880357	998-4435		ALL	Sanyo alt to POS caps
998-4715	998-4435		ALL	Kemet_Rect alt to POS caps
998-4716	998-4435		ALL	Kemet_0045 Plate alt to POS caps

DRAM CFG CHART

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 2
4GB	0
8GB	1

DIE REV	CFG 3
A	0
B	1

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
33784197	1	IVB, QRP8, ES2, K0, 1.5, 17W, 2+2, 0.95, 4M, ULVB	U1000	CRITICAL	CPU:1.5GHZ
33784299	1	IVB, QCS5, QS, L0, 1.7, 17W, 2+2, 1.0, 3M, ULVBGA	U1000	CRITICAL	CPU:1.7GHZ
33784298	1	IVB, QCS4, QS, L0, 1.8, 17W, 2+2, 1.1, 3M, ULVBGA	U1000	CRITICAL	CPU:1.8GHZ
33784296	1	IVB, QCS2, QS, L0, 2.0, 17W, 2+2, 1.1, 4M, ULVBGA	U1000	CRITICAL	CPU:2.0GHZ
33784198	1	IVB, QRP8, ES2, K0, 1.5, 17W, 2+2, 0.95, 4M, ULVB	U1000	CRITICAL	CPU:1.5GHZTDP
33784236	1	IVB, QROP, R82, K0, 1.7, 17W, 2+2, 1.0, 4M, ULVB, TDP	U1000	CRITICAL	CPU:1.7GHZTDP
33784165	1	IC, PCH, PPT-MB, SFF, ES1	U1800	CRITICAL	PCH_ES1
33784180	1	IC, PCH, PPT-MB, SFF, ES2, B0	U1800	CRITICAL	PCH_ES2
33784235	1	IC, PCH, PPT-MB, SFF, P-QS, C0	U1800	CRITICAL	PCH_CO
33784275	1	IC, PCH, PPT-MB, QS77, C1, QS	U1800	CRITICAL	PCH_C1
33881047	1	IC, TBT, CR-4C, ES1, 288 FCBGA, 12X12MM	U3600	CRITICAL	TWT

33380622	4	IC, SDRAM, 2GBIT, 256MX8, DDR3-1600, 78P FBGA	U2900, U2910, U2920, U2930	CRITICAL	DRAM_TYPE:HYNIX_4GB
33380622	4	IC, SDRAM, 2GBIT, 256MX8, DDR3-1600, 78P FBGA	U3000, U3010, U3020, U3030	CRITICAL	DRAM_TYPE:HYNIX_4GB
33380622	4	IC, SDRAM, 2GBIT, 256MX8, DDR3-1600, 78P FBGA	U3100, U3110, U3120, U3130	CRITICAL	DRAM_TYPE:HYNIX_4GB
33380622	4	IC, SDRAM, 2GBIT, 256MX8, DDR3-1600, 78P FBGA	U3200, U3210, U3220, U3230	CRITICAL	DRAM_TYPE:HYNIX_4GB
33380625	4	IC, SDRAM, 4GBIT, 512MX8, DDR3-1600, 82 FBGA	U2900, U2910, U2920, U2930	CRITICAL	DRAM_TYPE:HYNIX_8GB
33380625	4	IC, SDRAM, 4GBIT, 512MX8, DDR3-1600, 82 FBGA	U3000, U3010, U3020, U3030	CRITICAL	DRAM_TYPE:HYNIX_8GB
33380625	4	IC, SDRAM, 4GBIT, 512MX8, DDR3-1600, 82 FBGA	U3100, U3110, U3120, U3130	CRITICAL	DRAM_TYPE:HYNIX_8GB
33380625	4	IC, SDRAM, 4GBIT, 512MX8, DDR3-1600, 82 FBGA	U3200, U3210, U3220, U3230	CRITICAL	DRAM_TYPE:HYNIX_8GB
33380623	4	IC, SDRAM, 2GBIT, DDR3-1600, 78P FBGA, D-DIE	U2900, U2910, U2920, U2930	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
33380623	4	IC, SDRAM, 2GBIT, DDR3-1600, 78P FBGA, D-DIE	U3000, U3010, U3020, U3030	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
33380623	4	IC, SDRAM, 2GBIT, DDR3-1600, 78P FBGA, D-DIE	U3100, U3110, U3120, U3130	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
33380623	4	IC, SDRAM, 2GBIT, DDR3-1600, 78P FBGA, D-DIE	U3200, U3210, U3220, U3230	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
33380642	4	IC, SDRAM, 4GBIT, DDR3-1600, 78P FBGA, C-DIE	U2900, U2910, U2920, U2930	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
33380642	4	IC, SDRAM, 4GBIT, DDR3-1600, 78P FBGA, C-DIE	U3000, U3010, U3020, U3030	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
33380642	4	IC, SDRAM, 4GBIT, DDR3-1600, 78P FBGA, C-DIE	U3100, U3110, U3120, U3130	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
33380642	4	IC, SDRAM, 4GBIT, DDR3-1600, 78P FBGA, C-DIE	U3200, U3210, U3220, U3230	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
33380629	4	IC, SDRAM, 4GBIT, DDR3L-1600, REV B, 78P FBGA	U2900, U2910, U2920, U2930	CRITICAL	DRAM_TYPE:ELPIDA_8GB
33380629	4	IC, SDRAM, 4GBIT, DDR3L-1600, REV B, 78P FBGA	U3000, U3010, U3020, U3030	CRITICAL	DRAM_TYPE:ELPIDA_8GB
33380629	4	IC, SDRAM, 4GBIT, DDR3L-1600, REV B, 78P FBGA	U3100, U3110, U3120, U3130	CRITICAL	DRAM_TYPE:ELPIDA_8GB
33380629	4	IC, SDRAM, 4GBIT, DDR3L-1600, REV B, 78P FBGA	U3200, U3210, U3220, U3230	CRITICAL	DRAM_TYPE:ELPIDA_8GB
33380628	4	IC, SDRAM, 2GBIT, DDR3L-1600, REV D, 78P FBGA	U2900, U2910, U2920, U2930	CRITICAL	DRAM_TYPE:ELPIDA_4GB
33380628	4	IC, SDRAM, 2GBIT, DDR3L-1600, REV D, 78P FBGA	U3000, U3010, U3020, U3030	CRITICAL	DRAM_TYPE:ELPIDA_4GB
33380628	4	IC, SDRAM, 2GBIT, DDR3L-1600, REV D, 78P FBGA	U3100, U3110, U3120, U3130	CRITICAL	DRAM_TYPE:ELPIDA_4GB
33380628	4	IC, SDRAM, 2GBIT, DDR3L-1600, REV D, 78P FBGA	U3200, U3210, U3220, U3230	CRITICAL	DRAM_TYPE:ELPIDA_4GB

35382929	1	IC, 16L6239, BANCHEMGER, 38, 48XMM, QFN28	U7000	CRITICAL	
946-3115	1	MLB, DYNAX UV EB 0.22GRAM, R21	GLUE	CRITICAL	

PD Module Parts

806-3142	1	CAN, T29, J11/J13	TBTFFENCE	CRITICAL	
806-3215	1	CAN_COVER, T29, J11/J13	TBTTCOVER	CRITICAL	
806-3214	1	CAN, TOPSIDE, J11/J13	TBTTOPSIDE_IP	CRITICAL	
806-3706	1	CAN, TOPSIDE_2Piece_Cover, J11/J13	TBTTOPSIDE_2P_COVER	CRITICAL	
806-3705	1	CAN, TOPSIDE_2Piece_Fence, J11/J13	TBTTOPSIDE_2P_FENCE	CRITICAL	
806-3216	1	CAN, MDP, J11/J13	MDPCAN	CRITICAL	
806-3083	1	SHLD, USB, MLB, J11/J13	USBCAN	CRITICAL	
806-2377	1	K78, mDP Spring	MDPSPRING	CRITICAL	NOSTUFF

SYNC MASTER=J30 MLB SYNC DATE=07/27/2011

BOM Configuration

Apple Inc.

DRAWING NUMBER: 051-9277 SIZE: D

REVISION: 2.8.0

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Functional Test Points

J4001: AirPort / BT Connector

FUNC_TEST	TP	NC
PP3V3 WLAN F	37 42	
WiFi_EVENT_I	37 41 42	
PCIE AP R2D N	37 69	
PCIE AP R2D P	37 69	
PCIE CLK100M AP N	16 37 69	
PCIE CLK100M AP P	16 37 69	
USB BT CONN P	37 68	
USB BT CONN N	37 68	
PCIE AP D2R P	16 37 69	
PCIE AP D2R N	16 37 69	
PCIE WAKE L	17 37	
AP_RESET_CONN_L	37	
AP_CLKREQ_O_L	37	
PP3V3 S3RS4 BT F	37	

(Need 5 TPs)

J5600: Fan Connector

FUNC_TEST	TP	NC
PP5V S0_FAN	7 48	
FAN_RT_TACH	48	
FAN_RT_PWM	48	

(Need to add 1 GND TP)

J5700: IPD Flex Connector

FUNC_TEST	TP	NC
PP3V3 TPAD_CONN	49	
PP5V TPAD_FILT	49	
PP3V42 G3H TPAD	7 49	
USB_TPAD_CONN_P	48	
USB_TPAD_CONN_N	48	
I2C_TPAD_SDA	44 49	
I2C_TPAD_SCL	44 49	
SMC_ONOFF_L	41 42 49	
SMC_LID	6 40 41 42 49	
SMC_TPAD_RST_L	42 49	
SMC_PME_S4_WAKE_L	41 42 49	

(Need to add 5 GND TPs)

J6903: Speaker Connector

FUNC_TEST	TP	NC
SPKRAMP_ROUT_P	51 52 72	
SPKRAMP_ROUT_N	51 52 72	

(Need to add 3 GND TPs)

J6950: Battery Connector

FUNC_TEST	TP	NC
PPVBAT_G3H_CONN	52 53	
SMBUS_BATT_SCL	44 52	
SMBUS_BATT_SDA	44 52	
SYS_DETECT_L	52	

(Need 4 TPs)

(Need to add 4 GND TPs near J6950 and 1 for shield)

J9000: Internal DP Connector

FUNC_TEST	TP	NC
PPVOUT_SW_LCDBKLT	63 65	
PP3V3_SW_LCD	63	
I2C_TCON_SDA_R	63	
I2C_TCON_SCL_R	63	
LED_RETURN_6	63 65	
LED_RETURN_5	63 65	
LED_RETURN_4	63 65	
LED_RETURN_3	63 65	
LED_RETURN_2	63 65	
LED_RETURN_1	63 65	
DP_INT_HPD_CONN	63	
DP_INT_AUX_CH_C_N	63 66	
DP_INT_AUX_CH_C_P	63 66	
DP_INT_ML_F_P<0>	63 66	
DP_INT_ML_F_N<0>	63 66	
DP_INT_ML_F_P<1>	66	
DP_INT_ML_F_N<1>	66	

(Need 2 TPs)

(Need 2 TPs)

Misc Voltages & Control Signals

FUNC_TEST	TP	NC
PPBUS_G3H	7 52	
PPVIN_SW_TBTBST	7 36	
PPBUS_S5_HS_COMPUTING_ISNS	7	
PPDCIN_G3H	7	
PP3V42_G3H	7	
PPVRTC_G3H	7	
PP5V_S5	7	
PP5V_SUS	7	
PP3V3_S5	7 72	
PP3V3_SUS	7	
PP3V3_S3	7	
PP1V8_S0	7	
PP3V3_S0	7 72	
PP1V5_S3	7 67	
PP1V5_S3RS0	7 67	
PP1V5_S0	7	
PP1V05_S0	7	
PPVTTDDR_S3	7	
PP0V75_S0_DDRVTT	7	
PPVCCSA_S0_CPU	7	
PP1V05_SUS	7	
PP15V_TBT	7	
PP3V3_TBTLC	7	
PP1V05_TBTLC	7 36	
PP1V05_S0_PCH_VCCADPLL	7	
PPVCCORE_S0_CPU	7	
PPVCCORE_S0_AXG	7	
PP1V5_S3_CPU_VCCDQ	7	
PP1V05_S0_CPU_VCCPQE	7	
PP1V8_S0_CPU_VCCPLL_R	7	
PP1V05_TBTICIO	7	
PPBUS_S5_HS_OTHER_ISNS	7	
PPDCIN_G3H_ISOL	7	
PP5V_S3	7	
PP5V_S0	7	
PP3V3_S4	7	

(Need to add 27 GND TPs)

J4501: SATA SSD Connector

FUNC_TEST	TP	NC
PP3V3_S0_SSD_FLT	38	
SATA_SSD_D2R_P	38 68	
SATA_SSD_D2R_N	38 68	
SMC_OOB1_RX_L	38 41	
SMC_OOB1_TX_L	38 41 42	
PCIE_CLK100M_SSD_P	16 38 66	
PCIE_CLK100M_SSD_N	16 38 66	
PCIE_SSD_R2D_P<1>	38 66	
PCIE_SSD_R2D_N<1>	38 66	
PCIE_SSD_D2R_P<1>	8 38 66	
PCIE_SSD_D2R_N<1>	8 38 66	
SATA_SSD_R2D_N	38 68	
SATA_SSD_R2D_P	38 68	
SSD_CLKREQ_L	16 38	
SATA_PCIE_SEL	38	
SSD_P3V3S0_EN	38	
SSD_RESET_L	25 38	

(Need to add 6 GND TPs)

J6900: DC-In Connector

FUNC_TEST	TP	NC
PP18V5_DCIN_CONN	7 52	
PP5V_S3_LIO_CONN	7 52	

(Need 6 TPs)

(Need to add 5 GND TPs)

NO_TEST Nets

FUNC_TEST	TP	NC
VCCSAS0_SREF	54	
VCCSAS0_SET1_R	54	
VCCSAS0_SETO	54	
VCCSAS0_SET1	54	
TP_CRT_IG_BLUE		NC CRT IG BLUE
TP_CRT_IG_GREEN		NC CRT IG GREEN
TP_CRT_IG_RED		NC CRT IG RED
TP_CRT_IG_DDC_CLK		NC CRT IG DDC_CLK
TP_CRT_IG_DDC_DATA		NC CRT IG DDC_DATA
TP_CRT_IG_HSYNC		NC CRT IG HSYNC
TP_CRT_IG_VSYNC		NC CRT IG VSYNC
TP_LVDS_IG_CTRL_CLK		NC LVDS_IG_CTRL_CLK
TP_LVDS_IG_CTRL_DATA		NC LVDS_IG_CTRL_DATA
TP_PCH_LVDS_VBG		NC PCH_LVDS_VBG
TP_HDA_SDI1		NC HDA_SDI1
TP_HDA_SDI2		NC HDA_SDI2
TP_HDA_SDI3		NC HDA_SDI3
TP_PCI_PME_L		NC PCI_PME_L
TP_PCI_CLK13M_OUT3		NC PCI_CLK13M_OUT3
TP_CLKIN_CLK		NC_CLKIN_CLK
TP_CLKIN_DATA		NC_CLKIN_DATA
TP_CLKIN_RESET_L		NC_CLKIN_RESET_L
TP_PCIE_CLK100M_PERN		NC_PCIE_CLK100M_PERN
TP_PCIE_CLK100M_PERP		NC_PCIE_CLK100M_PERP
XDP_PCH_AP_PWR_EN		
XDP_PCH_USB_HUB_SOFT_RST_L		
XDP_PCH_SDCONN_STATE_RST_L		
XDP_PCH_ENET_PWR_EN		
XDP_PCH_SDCONN_DET_L		
XDP_PCH_S5_PWRGD	23	
XDP_PCH_PWRBTN_L	23	
XDP_PCH_ISOLATE_CPU_MEN_L		
XDP_PCH_CLKREQ_L		
XDP_PCH_CLKREQ_L		
XDP_PCH_AID_IPHS_SWITCH_EN		
TP_SDVO_TVCLKINH		NC_SDVO_TVCLKINH
TP_SDVO_TVCLKINP		NC_SDVO_TVCLKINP
TP_SDVO_STALIN		NC_SDVO_STALIN
TP_SDVO_STALIP		NC_SDVO_STALIP
TP_SDVO_INN		NC_SDVO_INN
TP_SDVO_INTP		NC_SDVO_INTP
TP_XDP_PCH_OBSPN_A<0..1>		NC_TP_XDP_PCH_OBSPN_A<0..1>
TP_XDP_PCH_OBSPN_B<0..1>		NC_TP_XDP_PCH_OBSPN_B<0..1>
TP_XDP_PCH_HOOK2		NC_TP_XDP_PCH_HOOK2
TP_XDP_PCH_HOOK3		NC_TP_XDP_PCH_HOOK3
TP_XDP_PCH_OBSPN_D<0..1>		NC_TP_XDP_PCH_OBSPN_D<0..1>
TP_XDP_PCH_HOOK4		NC_TP_XDP_PCH_HOOK4
TP_XDP_PCH_HOOK5		NC_TP_XDP_PCH_HOOK5
TP_PCH_GPI064_CLKOUTFLEX0		NC_PCH_GPI064_CLKOUTFLEX0
TP_PCH_GPI065_CLKOUTFLEX1		NC_PCH_GPI065_CLKOUTFLEX1
TP_PCH_GPI066_CLKOUTFLEX2		NC_PCH_GPI066_CLKOUTFLEX2
TP_PCH_GPI067_CLKOUTFLEX3		NC_PCH_GPI067_CLKOUTFLEX3

FUNC_TEST	TP	NC
NC_EDP_TXP<0..3>		TP_EDP_TX_P<0..3>
MAKE_BASE=TRUE		TP_EDP_TX_N<0..3>
NC_EDP_TXN<0..3>		TP_EDP_AUX_P
MAKE_BASE=TRUE		TP_EDP_AUX_N
NC_EDP_AUXN		TP_CPU_THERMDA
MAKE_BASE=TRUE		TP_CPU_THERMDC
NC_CPU_THERMDA		TP_CPU_RSVD<30..45>
MAKE_BASE=TRUE		TP_CPU_RSVD<30..45>
NC_CPU_THERMDC		TP_CPU_RSVD<8..27>
MAKE_BASE=TRUE		TP_CPU_RSVD<8..27>
NC_CPU_RSVD<30..45>		TP_PEG_R2D_CP<15..2>
MAKE_BASE=TRUE		TP_PEG_R2D_C_P<15..2>
NC_PEG_R2D_CP<15..2>		TP_PEG_R2D_C_N<15..2>
MAKE_BASE=TRUE		TP_PEG_R2D_C_N<15..2>
NC_PEG_R2D_CN<15..2>		TP_PEG_D2R_P<15..2>
MAKE_BASE=TRUE		TP_PEG_D2R_P<15..2>
NC_PEG_D2R_P<15..2>		TP_PEG_D2R_N<15..2>
MAKE_BASE=TRUE		

FUNC_TEST	TP	NC
TP_PCIE_CLK100M_PEA4		NC_PCIE_CLK100M_PEA4
TP_PCIE_CLK100M_PEP4		NC_PCIE_CLK100M_PEP4
TP_PCIE_CLK100M_PEN4		NC_PCIE_CLK100M_PEN4
TP_PCIE_CLK100M_PEP5		NC_PCIE_CLK100M_PEP5
TP_PCIE_CLK100M_PEN5		NC_PCIE_CLK100M_PEN5
TP_PCIE_CLK100M_PEP6		NC_PCIE_CLK100M_PEP6
TP_PCIE_CLK100M_PEN6		NC_PCIE_CLK100M_PEN6
TP_PCIE_CLK100M_PEP7		NC_PCIE_CLK100M_PEP7
TP_PCIE_CLK100M_PEN7		NC_PCIE_CLK100M_PEN7
TP_PROC_P1_3		NC_PROC_P1_3
TP_SATA_B_D2RN		NC_SATA_B_D2RN
TP_SATA_B_D2RP		NC_SATA_B_D2RP
TP_SATA_B_R2D_CN		NC_SATA_B_R2D_CN
TP_SATA_B_R2D_CP		NC_SATA_B_R2D_CP
TP_SATA_D_D2RN		NC_SATA_D_D2RN
TP_SATA_D_D2RP		NC_SATA_D_D2RP
TP_SATA_D_R2D_CN		NC_SATA_D_R2D_CN
TP_SATA_D_R2D_CP		NC_SATA_D_R2D_CP
TP_SATA_E_D2RN		NC_SATA_E_D2RN
TP_SATA_E_D2RP		NC_SATA_E_D2RP
TP_SATA_E_R2D_CN		NC_SATA_E_R2D_CN
TP_SATA_E_R2D_CP		NC_SATA_E_R2D_CP
TP_SATA_F_D2RN		NC_SATA_F_D2RN
TP_SATA_F_D2RP		NC_SATA_F_D2RP
TP_SATA_F_R2D_CN		NC_SATA_F_R2D_CN
TP_SATA_F_R2D_CP		NC_SATA_F_R2D_CP

FUNC_TEST	TP	NC
TP_PCH_TP18		NC_PCH_TP18
TP_PCH_TP17		NC_PCH_TP17
TP_PCH_TP16		NC_PCH_TP16
TP_PCH_TP15		NC_PCH_TP15
TP_PCH_TP14		NC_PCH_TP14
TP_PCH_TP13		NC_PCH_TP13
TP_PCH_TP12		NC_PCH_TP12
TP_PCH_TP10		NC_PCH_TP10
TP_PCH_TP9		NC_PCH_TP9
TP_PCH_TP8		NC_PCH_TP8
TP_PCH_TP7		NC_PCH_TP7
TP_PCH_TP6		NC_PCH_TP6
TP_PCH_TP5		NC_PCH_TP5
TP_PCH_TP4		NC_PCH_TP4
TP_PCH_TP3		NC_PCH_TP3
TP_PCH_TP2		NC_PCH_TP2
TP_PCH_TP1		NC_PCH_TP1

FUNC_TEST	TP	NC
PCH_VSS_NCTF<2>		PCH_VSS_NCTF<15>
PCH_VSS_NCTF<1>		PCH_VSS_NCTF<17>
PCH_VSS_NCTF<5>		PCH_VSS_NCTF<19>
PCH_VSS_NCTF<9>		PCH_VSS_NCTF<21>
PCH_VSS_NCTF<11>		PCH_VSS_NCTF<23>
PCH_VSS_NCTF<12>		PCH_VSS_NCTF<25>
PCH_VSS_NCTF<13>		PCH_VSS_NCTF<27>
PCH_VSS_NCTF<14>		PCH_VSS_NCTF<29>
TP_LVDS_IG_B_CLKN		NC_LVDS_IG_B_CLKN
TP_LVDS_IG_B_CLKP		NC_LVDS_IG_B_CLKP
TP_LVDS_IG_BEL_PWM		NC_LVDS_IG_BEL_PWM
SMC_BS_ALERT_L		NC_SMC_BS_ALERT_L

SYNC MASTER=K21_MLB SYNC DATE=07/29/2011

Functional Test / No Test

Apple Inc.

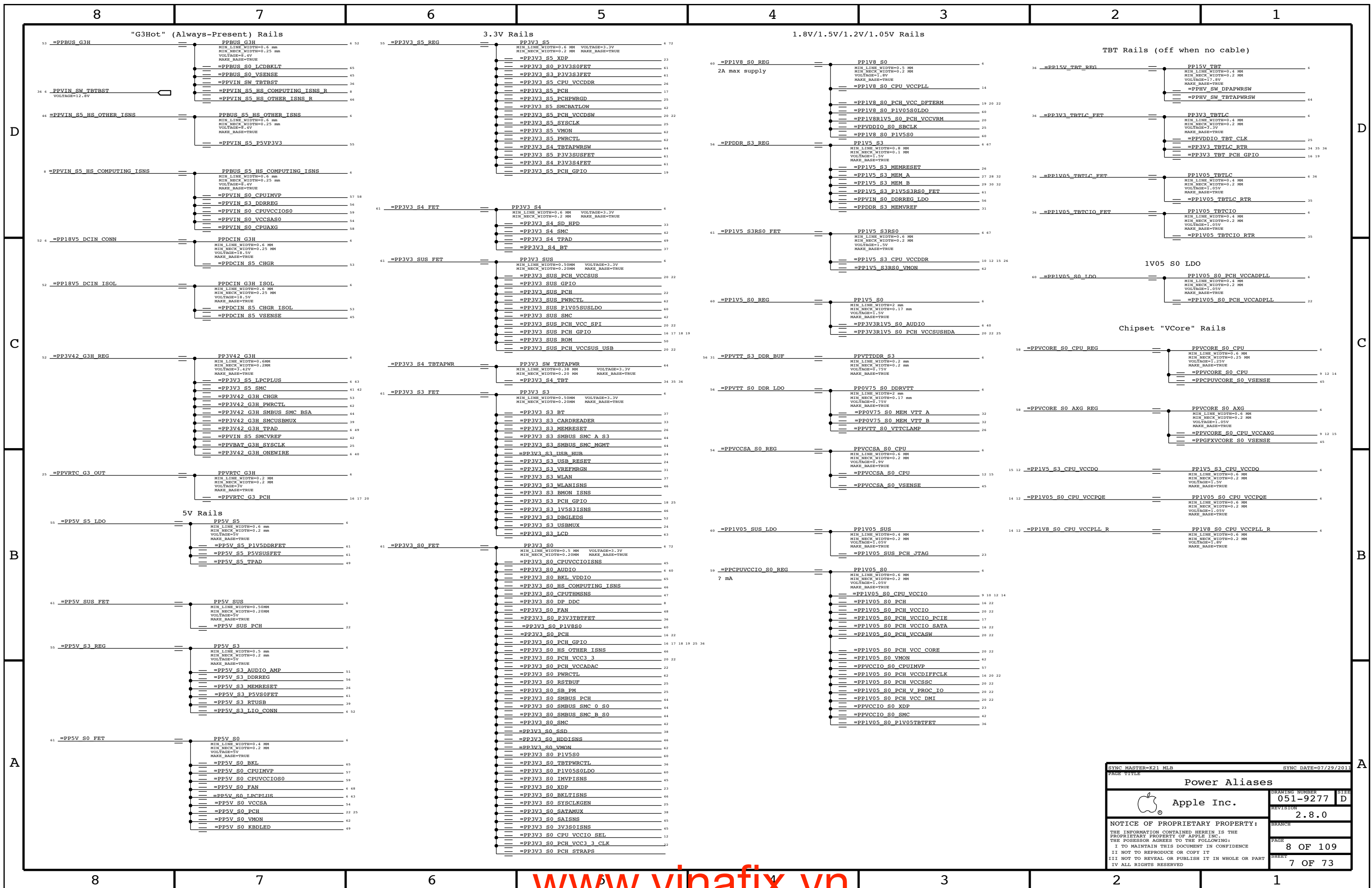
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SYNC MASTER=K21 MLB SYNC DATE=07/29/2011

PAGE TITLE

Power Aliases

Apple Inc.

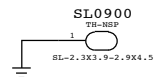
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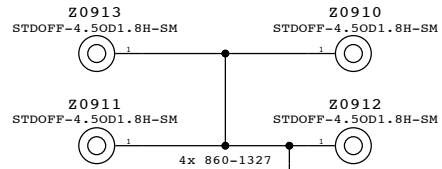
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BRANCH: PAGE: 8 OF 109 SHEET: 7 OF 73

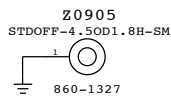
Plated Board Slot



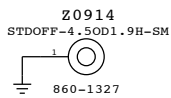
CPU Heat Sink Mounting Bosses



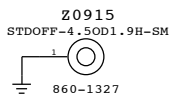
Fan Boss



X21 Boss

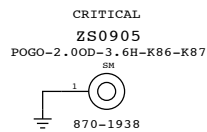


SSD Boss

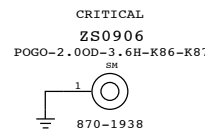


EMI I/O Pogo Pins

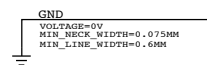
DisplayPort Pogo



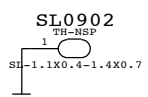
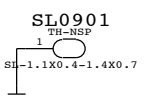
USB/SD Card Pogo



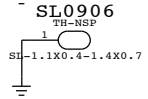
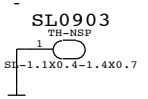
Digital Ground



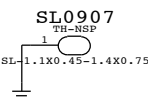
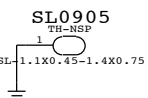
Can Slots



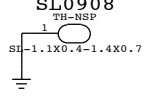
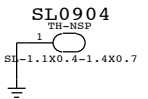
2x TBT pin diodes



2x MDP Connector



2x TBT chip



2x USB Connector

Unused PPT

Table of unused PPT signals including PCIE CLK100M ENET N, CPU signals, MEMVT EN, and various PCIE and MEM signals.

Table of unused MEM signals including MEM A CLK P<1>, MEM A CLK N<1>, MEM B CLK P<1>, and MEM B CLK N<1>.

Table of unused ENET and SATARDVR signals including ENET LOW PWR PCH, SATARDVR EN, and TP PCH CLKOUT signals.

Unused USB

Table of unused USB signals including USB_EXTC_P, USB_EXTC_N, USB3_EXTC_RX_P, and USB3_EXTD_RX_P.

Unused PGOOD signal

Table of unused PGOOD signals including TP_P1V5S3RS0_RAMP_DONE and TP_DDRREG_PGOOD.

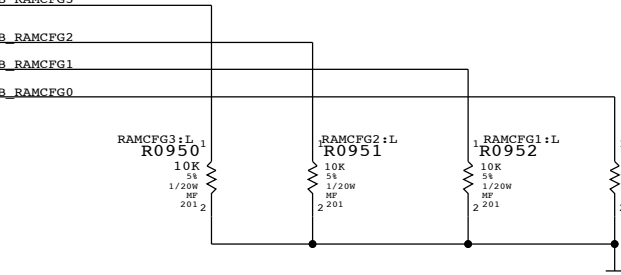
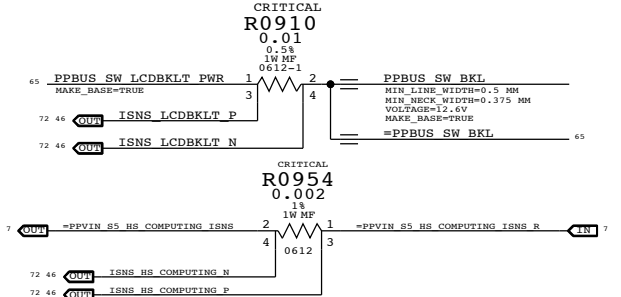
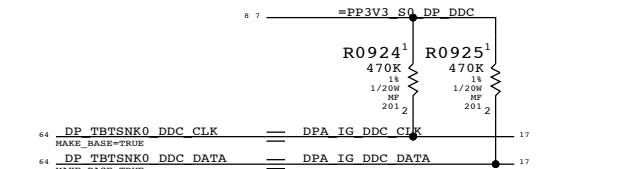
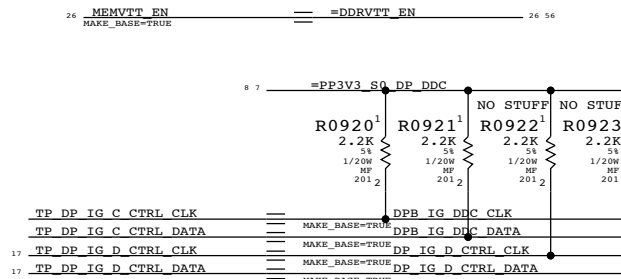
SATA Aliases

Table of SATA aliases including SATA_ODD_R2D_C_P, SATA_ODD_R2D_C_N, SATA_ODD_D2R_P, and SATA_ODD_D2R_N.

SSD PCIE Signals

Table of SSD PCIE signals including PEG_D2R_P<1..0>, PEG_D2R_N<1..0>, PEG_R2D_C_P<1..0>, and PEG_R2D_C_N<1..0>.

CPU signals



LVDS Aliases

Table of LVDS aliases including TP_LVDS_IG_B_CLKP, TP_LVDS_IG_B_CLKN, NC_LVDS_IG_B_DATAP<0..3>, TP_LVDS_IG_B_DATAN<0..3>, NC_LVDS_IG_A_DATAP<3>, TP_LVDS_IG_A_DATAN<3>, LCD_BKLT_PWM, LCD_IG_PWR_EN, and LCD_BKLT_EN.

SMC Aliases

Table of SMC aliases including SMC_SYS_LED and IR_RX_OUT_RC.

TBT DP Ports

Table of TBT DP ports including DPB_IG_HPD, DPA_IG_HPD, DP_TBT_SNK0_AUXCH_C_P, DP_TBT_SNK0_AUXCH_C_N, DP_TBT_SNK1_AUXCH_C_P, DP_TBT_SNK1_AUXCH_C_N, DP_TBT_SNK1_ML_C_P<3..0>, DP_TBT_SNK1_ML_C_N<3..0>, DP_TBT_SNK0_ML_C_P<3..0>, DP_TBT_SNK0_ML_C_N<3..0>, DP_TBT_SNK0_ML_C_P<1>, DP_TBT_SNK0_ML_C_N<1>, DP_TBT_SNK0_ML_C_P<3>, DP_TBT_SNK0_ML_C_N<3>, DP_TBT_SNK0_ML_C_P, DP_TBT_SNK0_ML_C_N, DP_TBT_SNK1_ML_C_P<1>, DP_TBT_SNK1_ML_C_N<1>, DP_TBT_SNK1_ML_C_P<3>, DP_TBT_SNK1_ML_C_N<3>, DP_TBT_SNK1_AUXCH_C_P, DP_TBT_SNK1_AUXCH_C_N, TBT_B_R2D_C_N<0>, TBT_B_R2D_C_P<0>, TBT_B_R2D_C_N<1>, TBT_B_R2D_C_P<1>, TBT_B_R2D_C_N<3>, TBT_B_R2D_C_P<3>, TBT_B_D2R_P<0>, TBT_B_D2R_N<0>, TBT_B_D2R_P<1>, TBT_B_D2R_N<1>, TBT_B_D2R_N<1>, TBT_B_CIO_SEL, DP_TBT_PR_HPD, TBT_B_CONFIG2_RC, TBT_B_CONFIG1_BUR, TBT_B_LSRX, and TBT_B_LSTX.

Signal Aliases table with Apple Inc. logo, drawing number 051-9277, revision 2.8.0, and page 9 of 109.

NOTE: Intel provides an internal pull-up of 5-15k to VCCIO on all CFG signals.

D

C

B

A

D

C

B

A

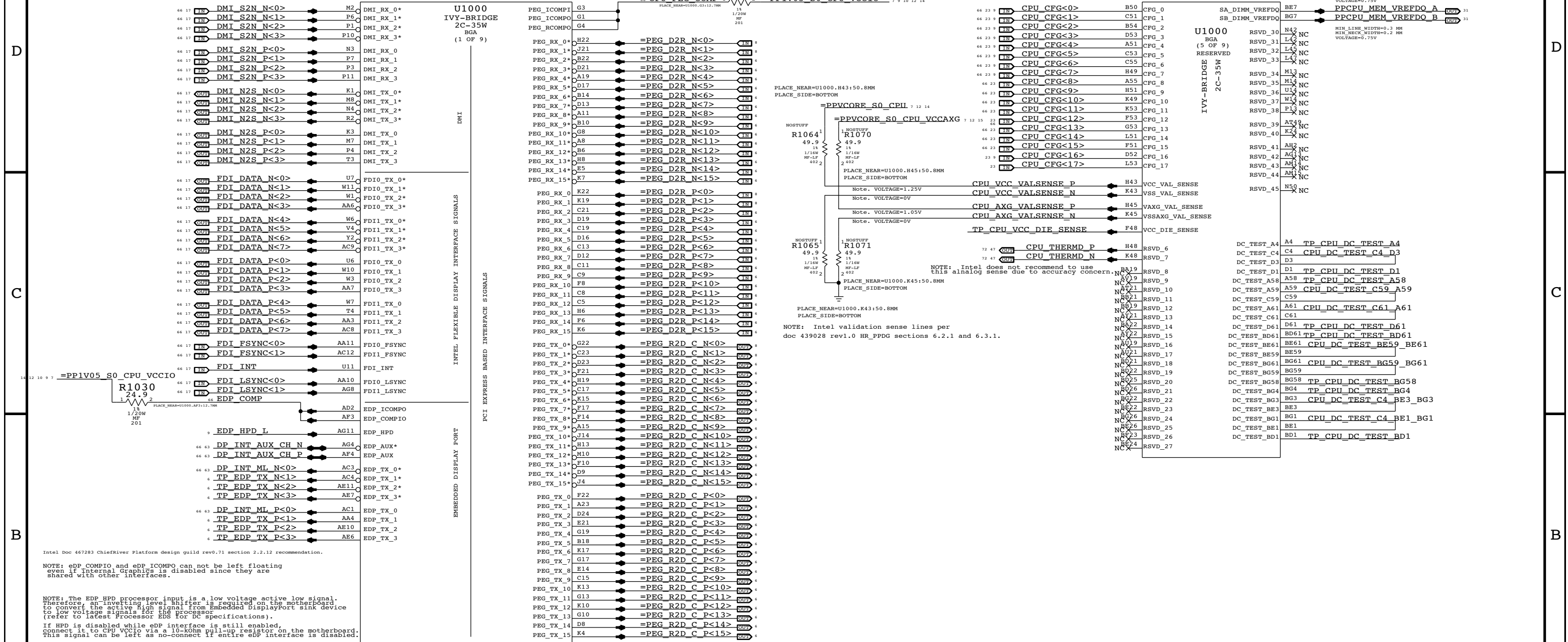
OMIT TABLE CRITICAL

OMIT TABLE CRITICAL

U1000
IVY-BRIDGE
2C-35W
BGA
(1 OF 9)

U1000
BGA
(5 OF 9)
RESERVED
IVY-BRIDGE
2C-35W

MIN LINE WIDTH=0.3 MM
MIN SPACE WIDTH=0.2 MM
VOLTAGE=0.75V

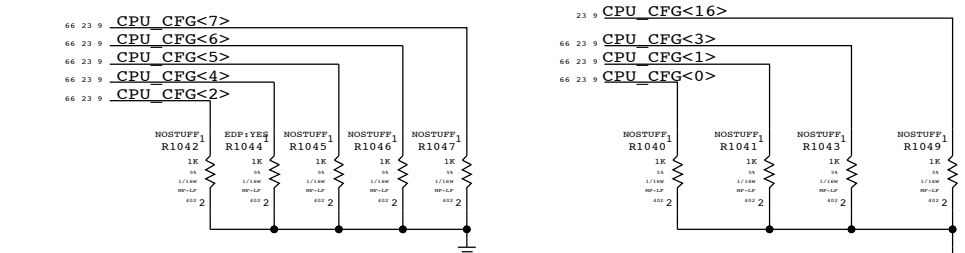


Intel Doc 467283 ChiefRiver Platform design guide rev0.71 section 2.2.12 recommendation.

NOTE: eDP COMPIO and eDP ICOMPO can not be left floating even if internal Graphics is disabled since they are shared with other interfaces.

NOTE: The EDP HPD processor input is a low voltage active low signal. Therefore an inverting level shifter is required on the motherboard to convert the active high signal from Embedded DisplayPort sink device to low voltage signals for the processor. (refer to latest Processor EDP specifications).

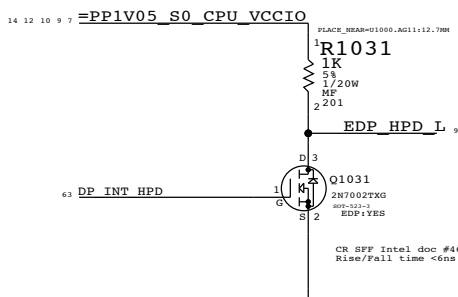
If HPD is disabled while eDP interface is still enabled, connect it to CPU VCCIO via a 10-kOhm pull-up resistor on the motherboard. This signal can be left as no-connect if entire eDP interface is disabled.



These can be Placed close to J2500 and Only for debug access

FOR IVYBRIDGE PROCESSOR

CFG [7] :PEG DEFER TRAINING	1 = (DEFAULT) IMMEDIATELY AFTER xRESETB 0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION	11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE	1 = DISABLED 0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL	1 = NORMAL OPERATION 0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL	1 = NORMAL OPERATION 0 = LANES REVERSED



CR SFF Intel doc #460452 Rise/Fall time <6ns

SYNC MASTER=J13 MLB NON POR SYNC DATE=10/17/2011

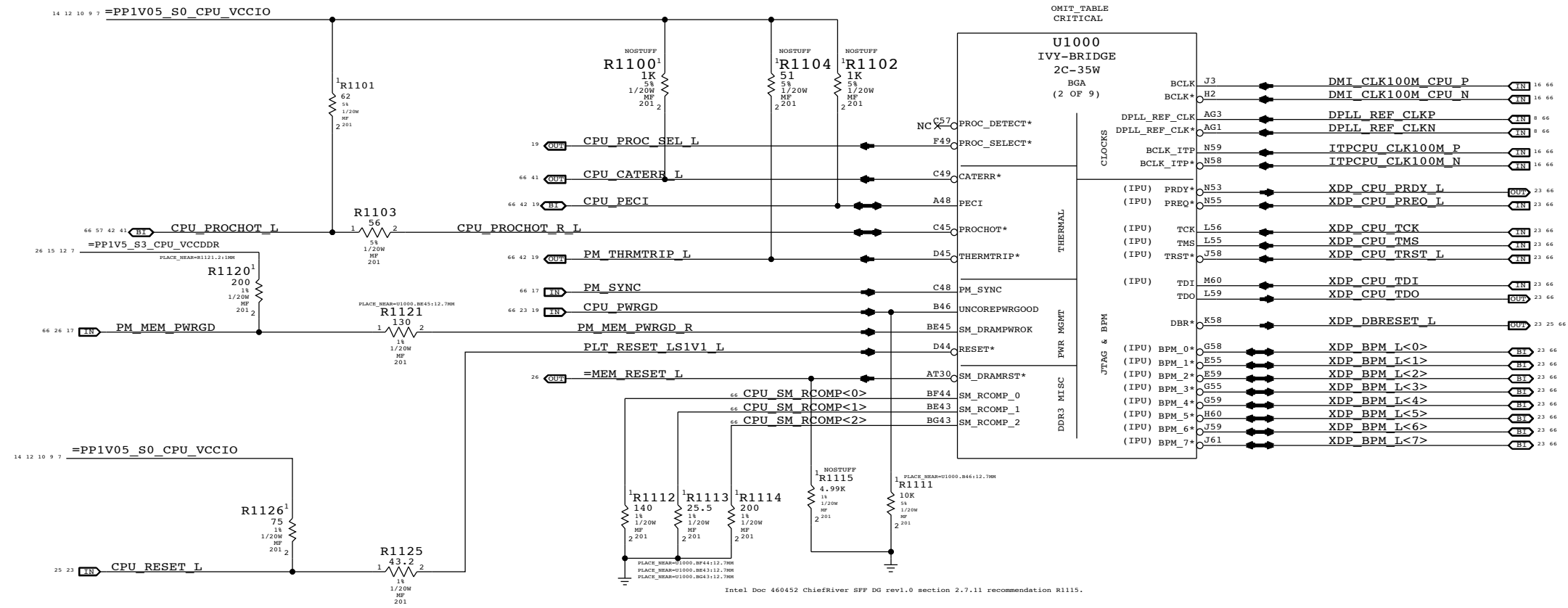
PAGE TITLE: CPU DMI/PEG/FDI/RSVD

Apple Inc. DRAWING NUMBER: 051-9277 SIZE: D

REVISION: 2.8.0

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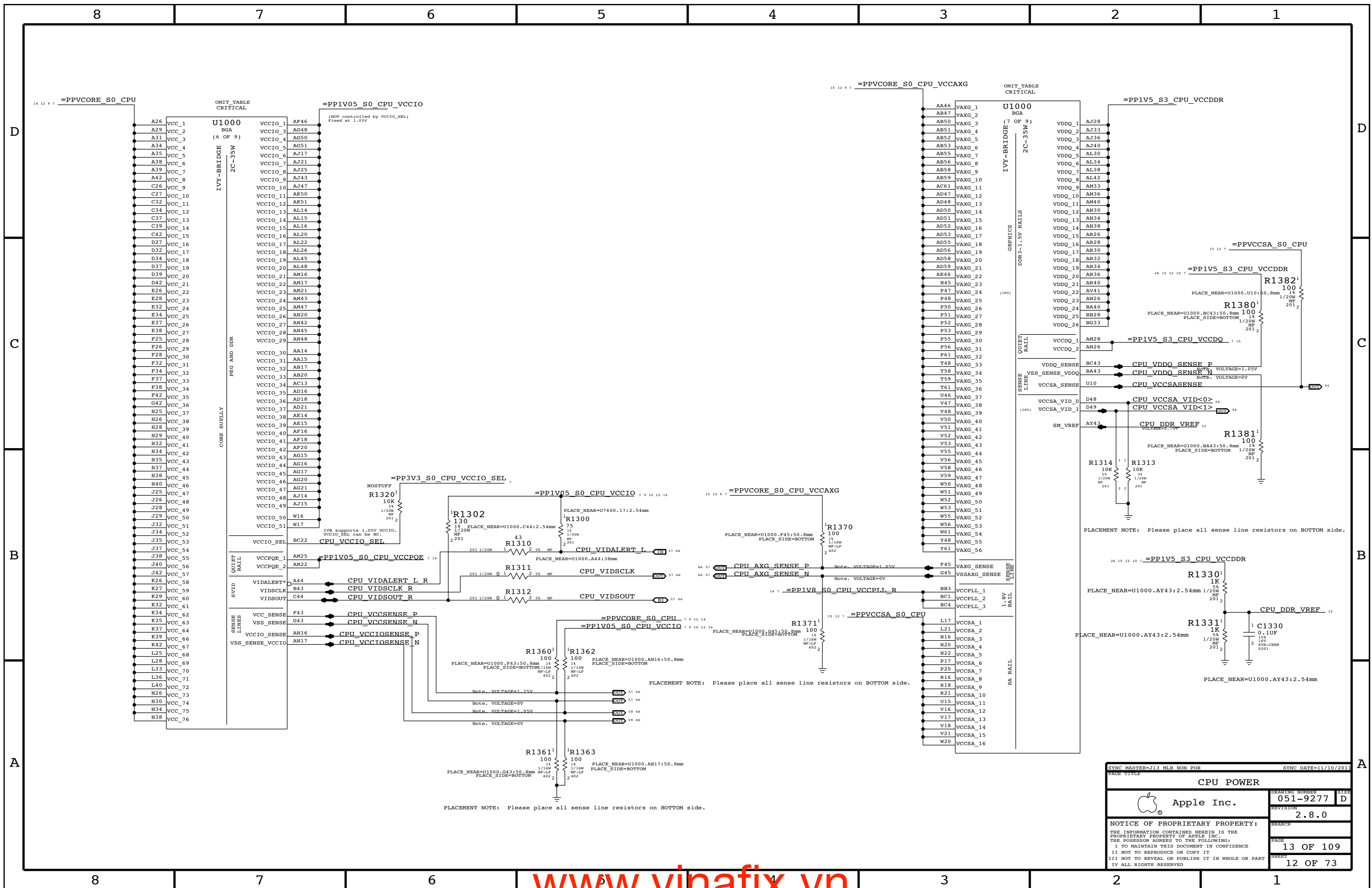
BRANCH: PAGE: 10 OF 109 SHEET: 9 OF 73



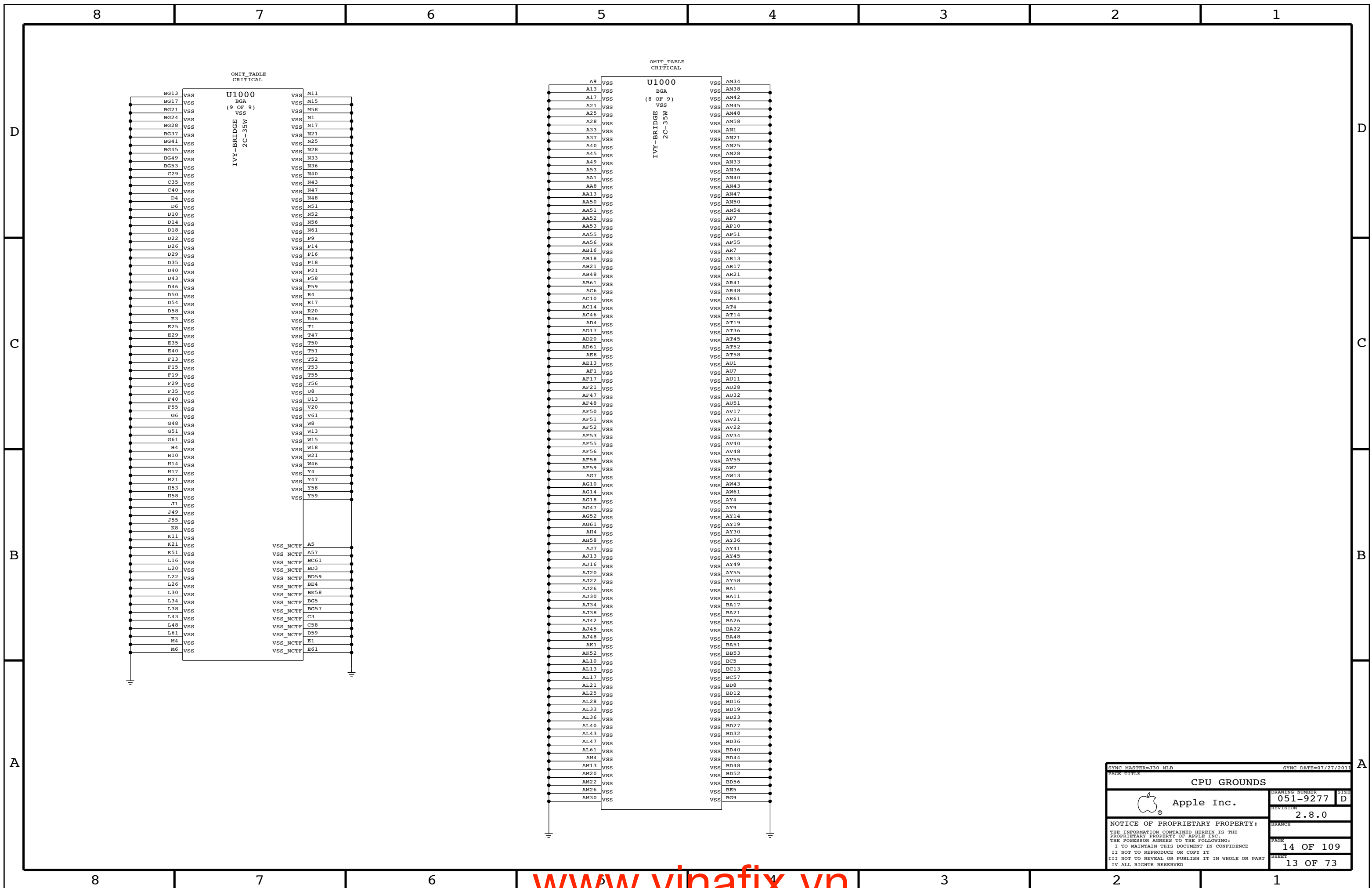
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PAGE TITLE CPU CLOCK/MISC/JTAG			
DRAWING NUMBER 051-9277		SIZE D	
REVISION 2.8.0		BRANCH	
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PAGE 11 OF 109		SHEET 10 OF 73	



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CPU DDR3 INTERFACES			
Apple Inc.		DRAWING NUMBER	051-9277
		REVISION	2.8.0
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SYNC MASTER=J13 MLB NON POR		SYNC DATE=11/10/2011	
PAGE TITLE			
CPU POWER		DRAWING NUMBER	SIZE
Apple Inc.		051-9277	D
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		2.8.0	13 OF 109
		SHEET	12 OF 73



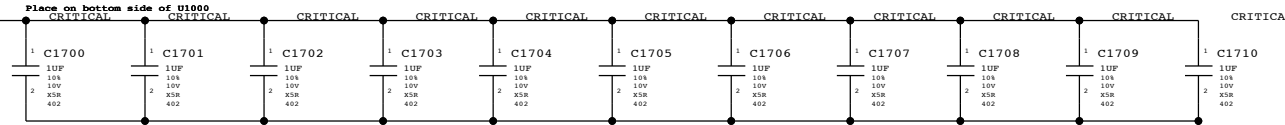
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PAGE TITLE			
CPU GROUNDS			
		DRAWING NUMBER	051-9277
		REVISION	2.8.0
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		PAGE	14 OF 109
		SHEET	13 OF 73

VAXG DECOUPLING

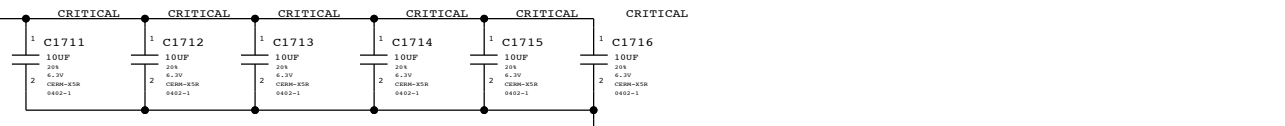
Graphics Load Line : -3.9 mOhms

Intel recommendation (section 6.3): 18x 1uF(9 no-stuff), 10x 104F(2 no-stuff), 8x 22uF(2 no stuff), 4x 470uF(2 no-stuff)

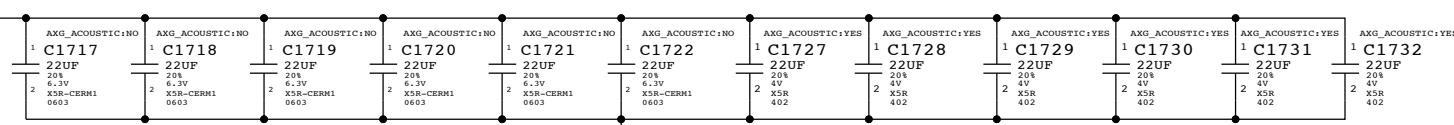
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PLACEMENT_NOTE (C1711-C1716):



PLACEMENT_NOTE (C1717-C1722):



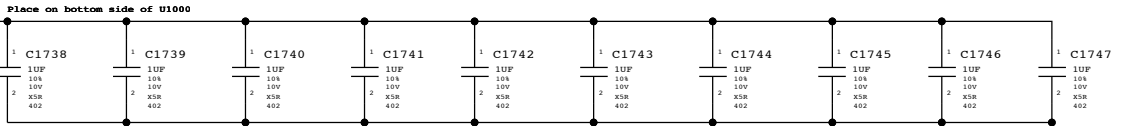
PLACEMENT_NOTE (C1723-C1724):



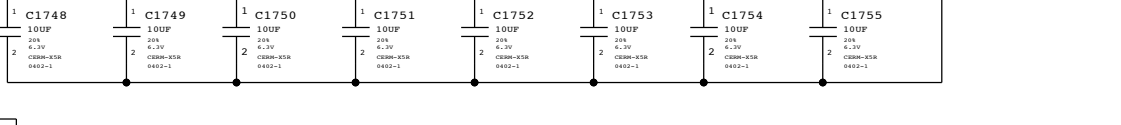
CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation (Section 6.13): 10x 1uF, 8x 10uF, 1x 330uF

PLACEMENT_NOTE (C1738-C1747):



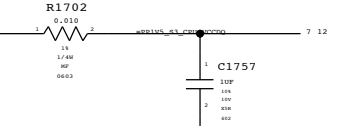
Place close to U1000 on bottom side



PLACEMENT_NOTE (C1756):



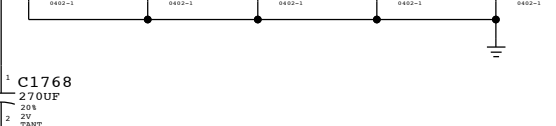
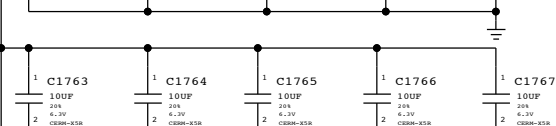
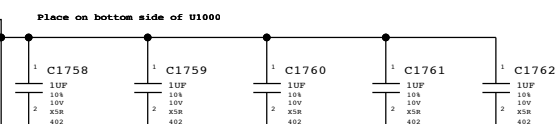
Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402



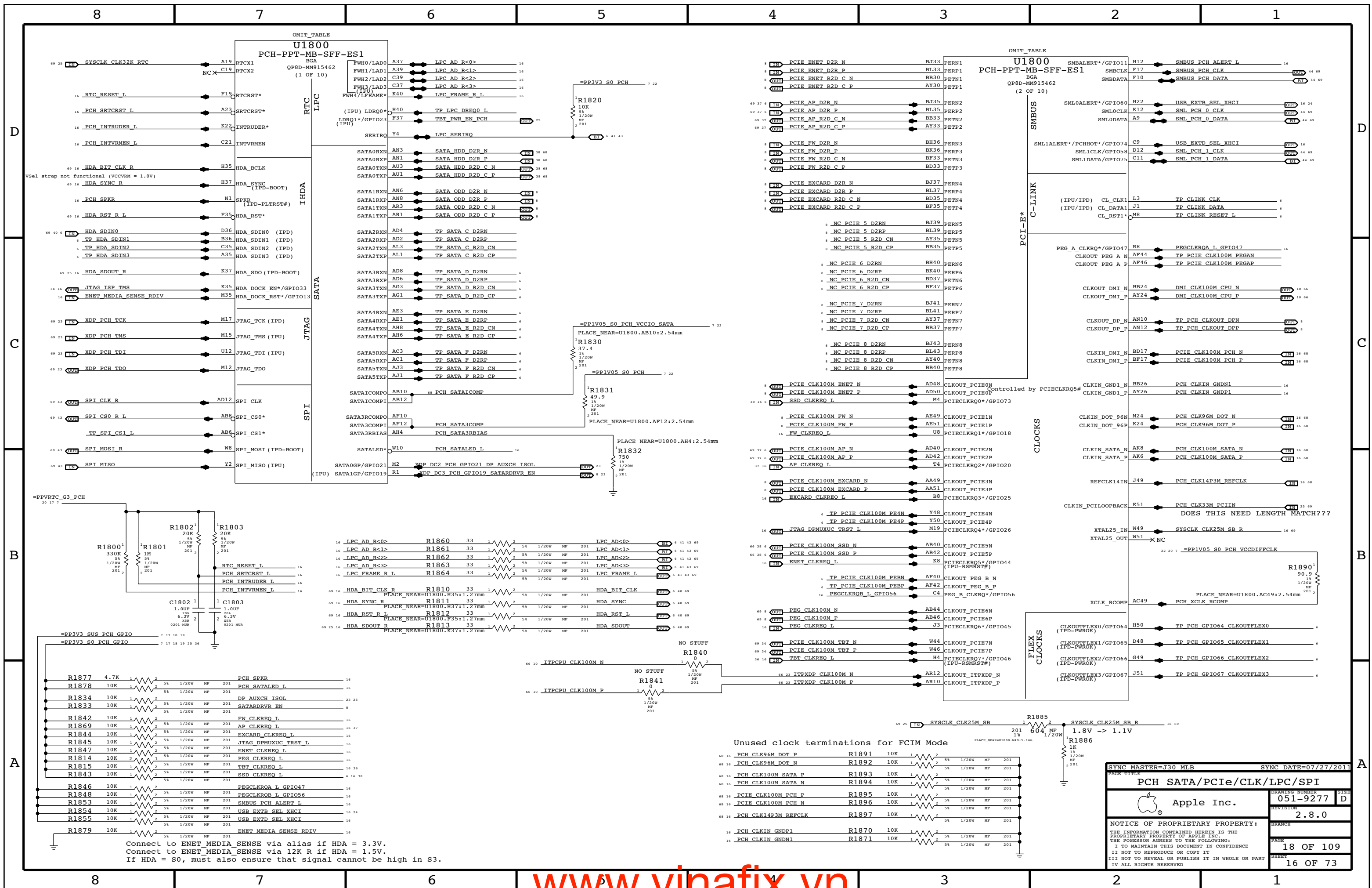
CPU VCCSA DECOUPLING

Intel recommendation (Section 6.6): 3x 1uF, 3x 10uF, 1x 330uF

PLACEMENT_NOTE (C1758-C1762):



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CPU DECOUPLING-II		051-9277		D
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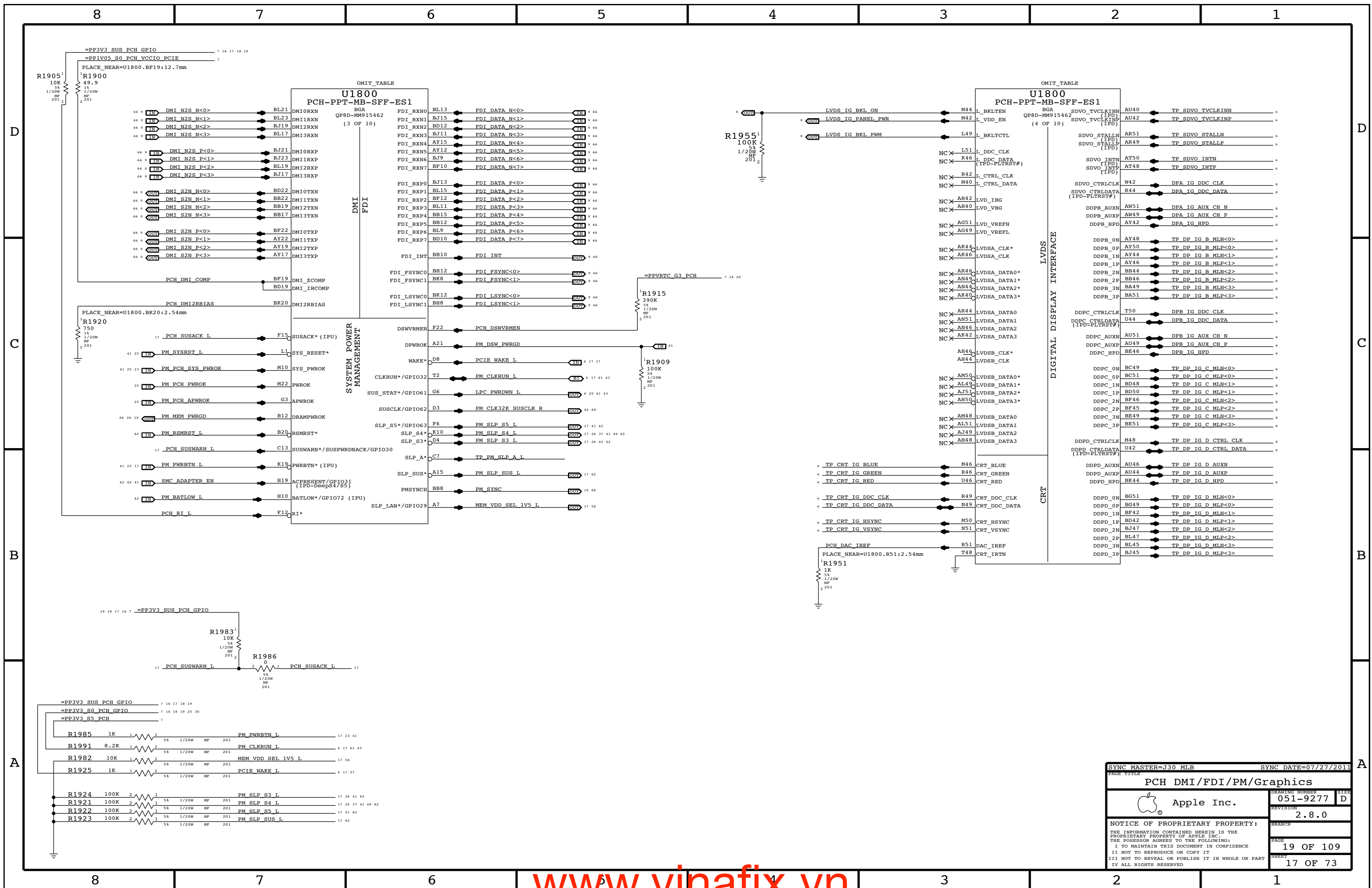


Connect to ENET_MEDIA_SENSE via alias if HDA = 3.3V.
 Connect to ENET_MEDIA_SENSE via 12K R if HDA = 1.5V.
 If HDA = S0, must also ensure that signal cannot be high in S3.

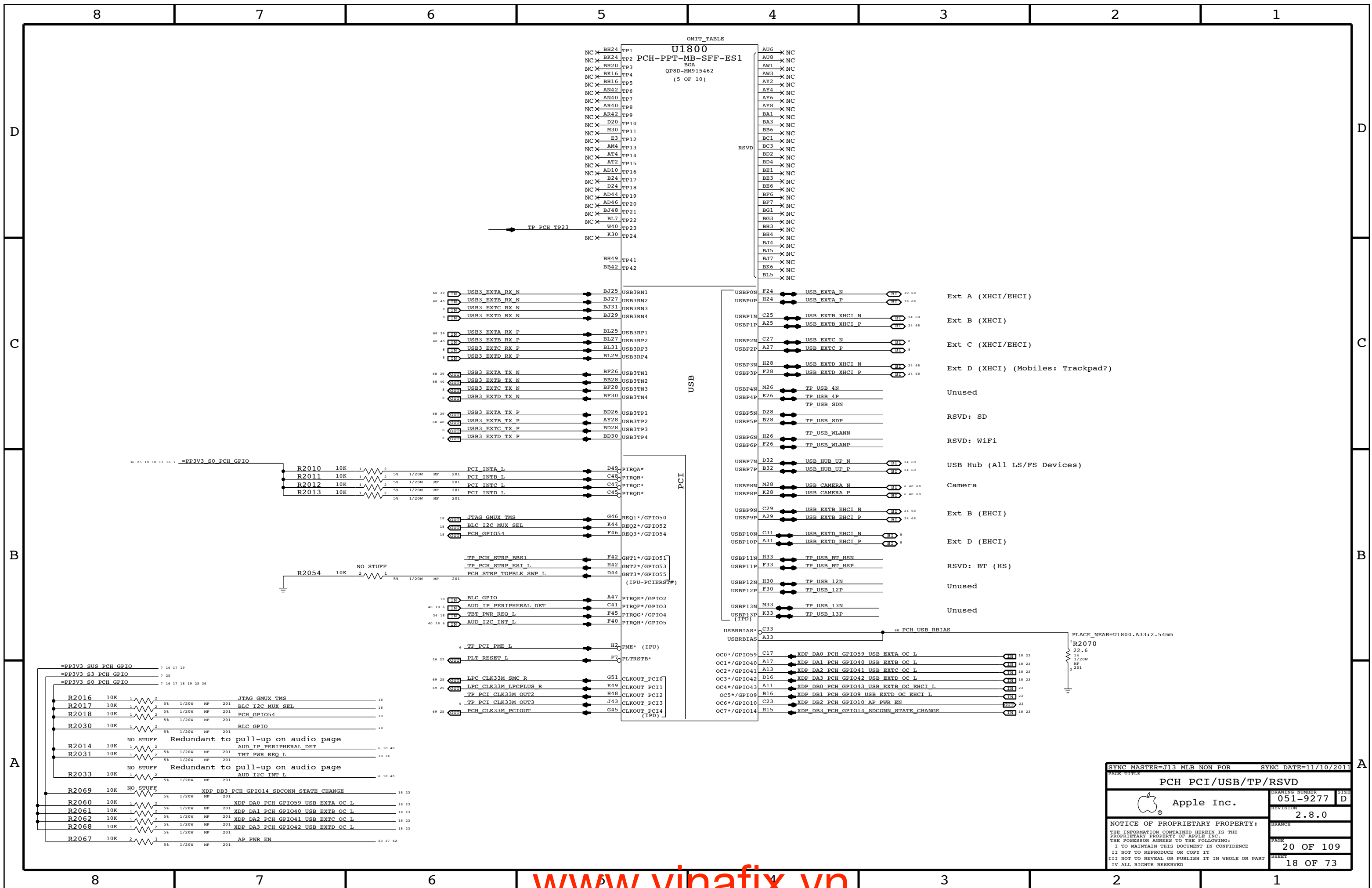
Unused clock terminations for FCIM Mode

69 16	PCH CLK96M DOT P	R1891	10K	1	2	5%	1/20W	HP	201
69 16	PCH CLK96M DOT N	R1892	10K	1	2	5%	1/20W	HP	201
69 16	PCH CLK100M SATA P	R1893	10K	1	2	5%	1/20W	HP	201
69 16	PCH CLK100M SATA N	R1894	10K	1	2	5%	1/20W	HP	201
69 16	PCIE CLK100M PCH P	R1895	10K	1	2	5%	1/20W	HP	201
69 16	PCIE CLK100M PCH N	R1896	10K	1	2	5%	1/20W	HP	201
69 16	PCH CLK14P3M REFCLK	R1897	10K	1	2	5%	1/20W	HP	201
69 16	PCH CLKIN GNDP1	R1870	10K	1	2	5%	1/20W	HP	201
69 16	PCH CLKIN GNDN1	R1871	10K	1	2	5%	1/20W	HP	201

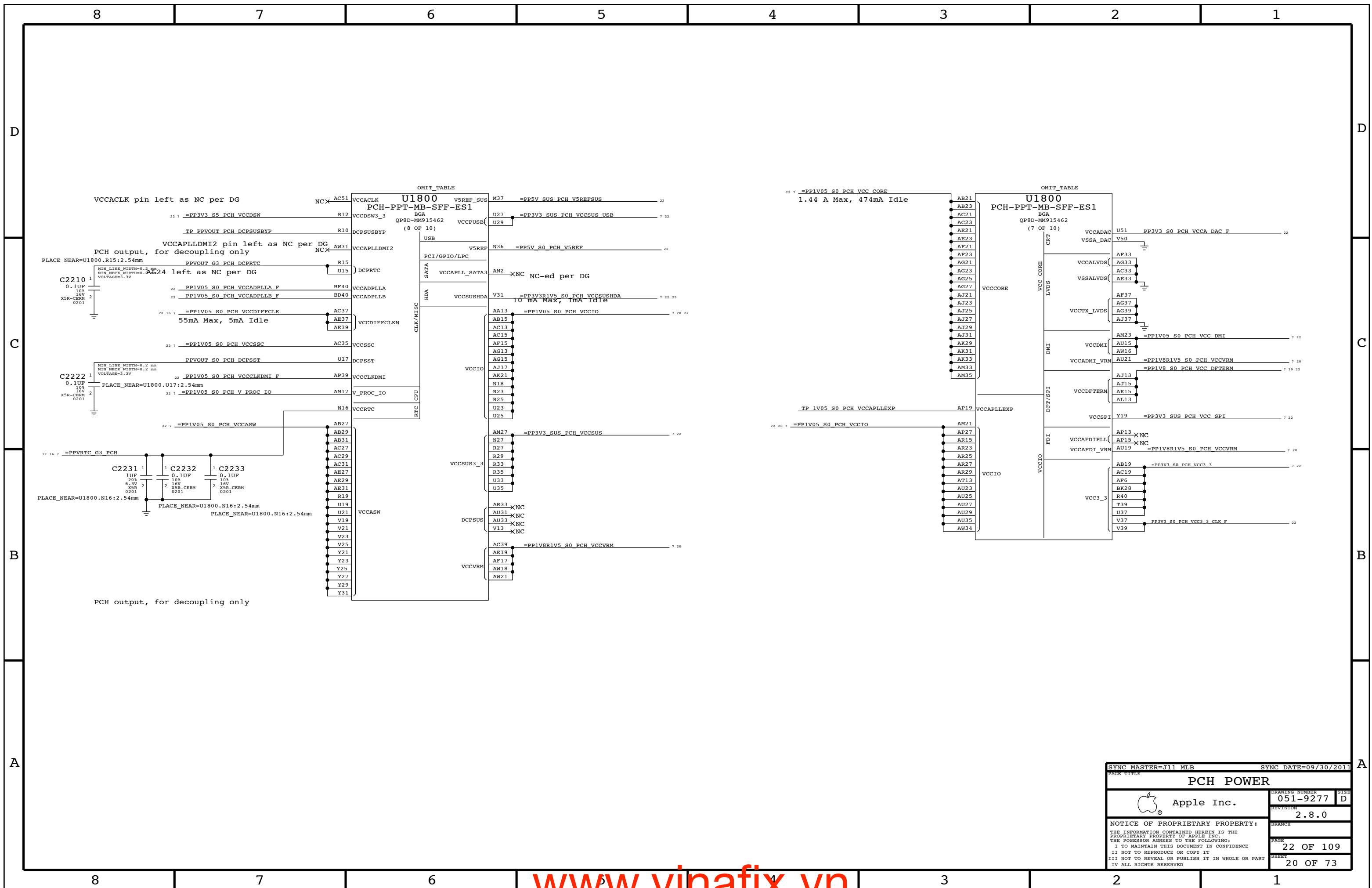
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PCH SATA/PCIE/CLK/LPC/SPI		DRAWING NUMBER	051-9277
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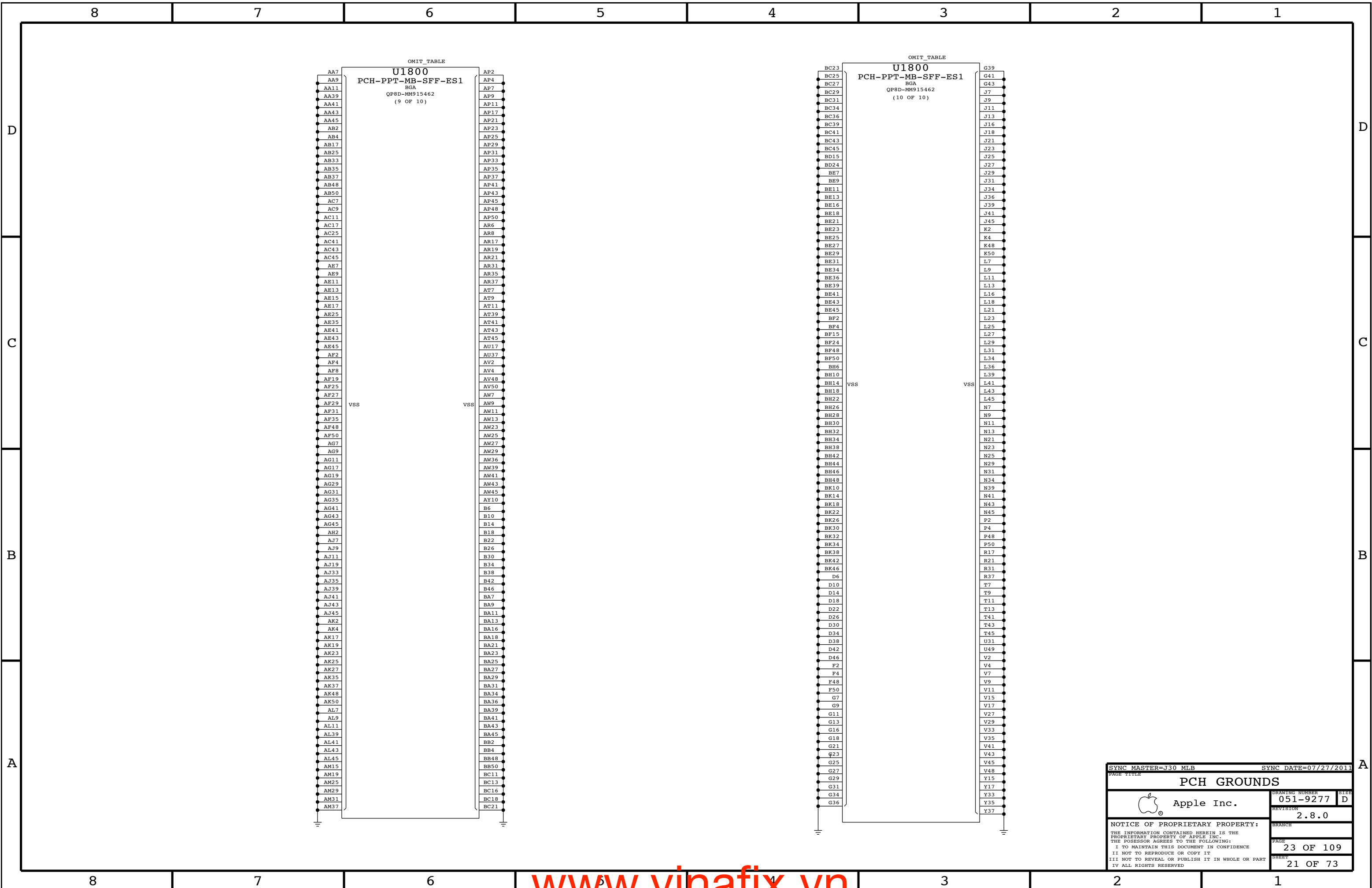
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PAGE TITLE			
PCH DMI/FDI/PM/Graphics		DRAWING NUMBER	051-9277
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PCH PCI/USB/TP/RSVD			
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PCH POWER			
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OMIT_TABLE

U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(9 OF 10)

AA7	AP2
AA9	AP4
AA11	AP7
AA39	AP9
AA41	AP11
AA43	AP17
AA45	AP21
AB2	AP23
AB4	AP25
AB17	AP29
AB25	AP31
AB33	AP33
AB35	AP35
AB37	AP37
AB48	AP41
AB50	AP43
AC7	AP45
AC9	AP48
AC11	AP50
AC17	AR6
AC25	AR8
AC41	AR17
AC43	AR19
AC45	AR21
AE7	AR31
AE9	AR35
AE11	AR37
AE13	AT7
AE15	AT9
AE17	AT11
AE25	AT39
AE35	AT41
AE41	AT43
AE43	AT45
AE45	AU17
AF2	AU37
AF4	AV2
AF8	AV4
AF19	AV48
AF25	AV50
AF27	AW7
AF29	AW9
AF31	AW11
AF35	AW13
AF48	AW23
AF50	AW25
AG7	AW27
AG9	AW29
AG11	AW36
AG17	AW39
AG19	AW41
AG29	AW43
AG31	AW45
AG35	AY10
AG41	B6
AG43	B10
AG45	B14
AH2	B18
AJ7	B22
AJ9	B26
AJ11	B30
AJ19	B34
AJ33	B38
AJ35	B42
AJ39	B46
AJ41	BA7
AJ43	BA9
AJ45	BA11
AK2	BA13
AK4	BA16
AK17	BA18
AK19	BA21
AK23	BA23
AK25	BA25
AK27	BA27
AK35	BA29
AK37	BA31
AK48	BA34
AK50	BA36
AL7	BA39
AL9	BA41
AL11	BA43
AL39	BA45
AL41	BB2
AL43	BB4
AL45	BB48
AM15	BB50
AM19	BC11
AM25	BC13
AM29	BC16
AM31	BC18
AM37	BC21

OMIT_TABLE

U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(10 OF 10)

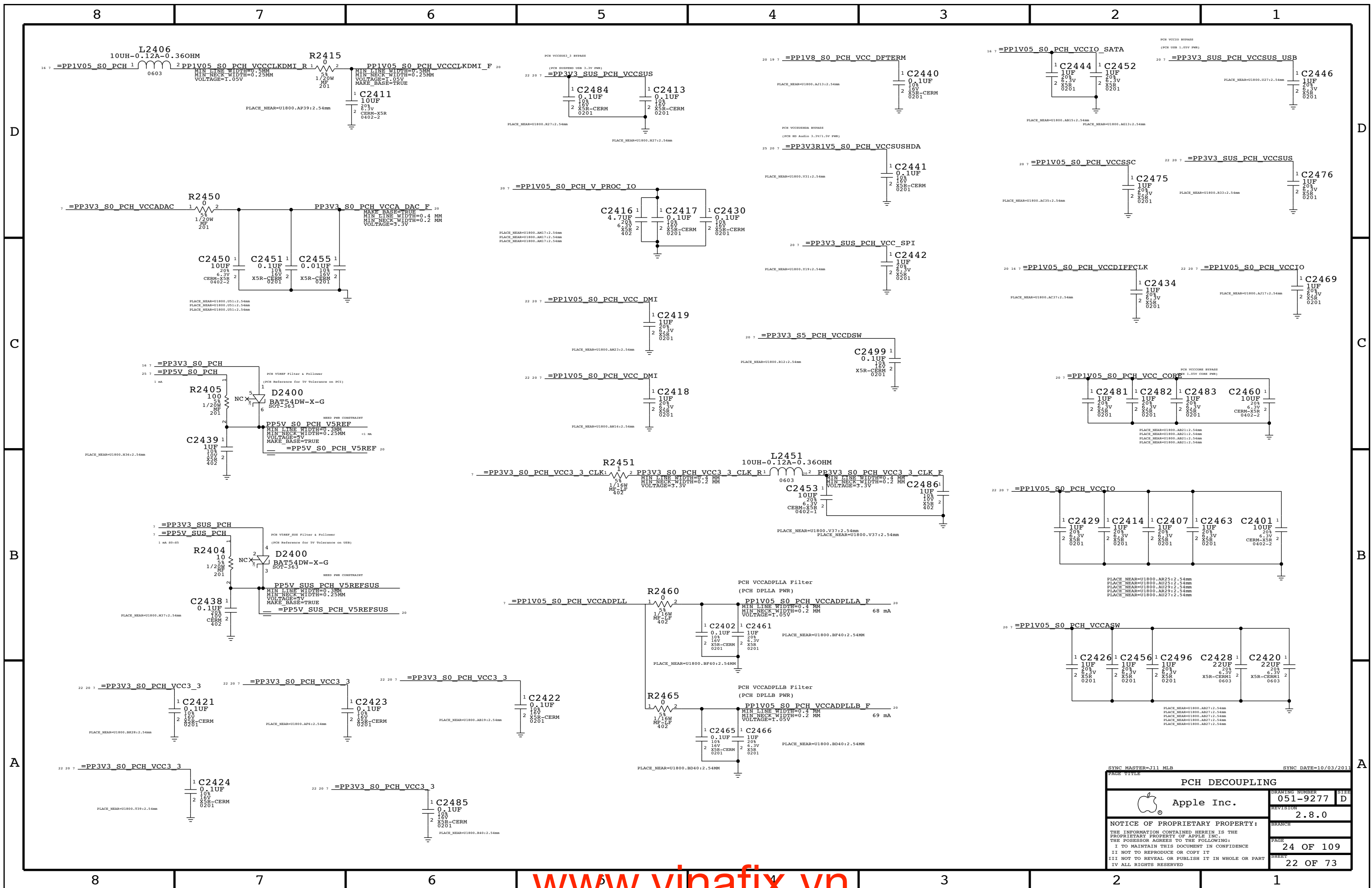
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BC25	G41
BC27	G43
BC29	J7
BC31	J9
BC34	J11
BC36	J13
BC39	J16
BC41	J18
BC43	J21
BC45	J23
BD15	J25
BD24	J27
BE7	J29
BE9	J31
BE11	J34
BE13	J36
BE16	J39
BE18	J41
BE21	J45
BE23	K2
BE25	K4
BE27	K48
BE29	K50
BE31	L7
BE34	L9
BE36	L11
BE39	L13
BE41	L16
BE43	L18
BE45	L21
BF2	L23
BF4	L25
BF15	L27
BF24	L29
BF48	L31
BF50	L34
BH6	L36
BH10	L39
BH14	L41
BH18	L43
BH22	L45
BH26	N7
BH28	N9
BH30	N11
BH32	N13
BH34	N21
BH38	N23
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BH46	N31
BH48	N34
BK10	N39
BK14	N41
BK18	N43
BK22	N45
BK26	P2
BK30	P4
BK32	P48
BK34	P50
BK38	R17
BK42	R21
BK46	R31
D6	R37
D10	T7
D14	T9
D18	T11
D22	T13
D26	T41
D30	T43
D34	T45
D38	U31
D42	U49
D46	V2
F2	V4
F4	V7
F48	V9
F50	V11
G7	V15
G9	V17
G11	V27
G13	V29
G16	V33
G18	V35
G21	V41
G23	V43
G25	V45
G27	V48
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G31	Y17
G34	Y33
G36	Y35
	Y37

SYNC MASTER=J30 MLB SYNC DATE=07/27/2011

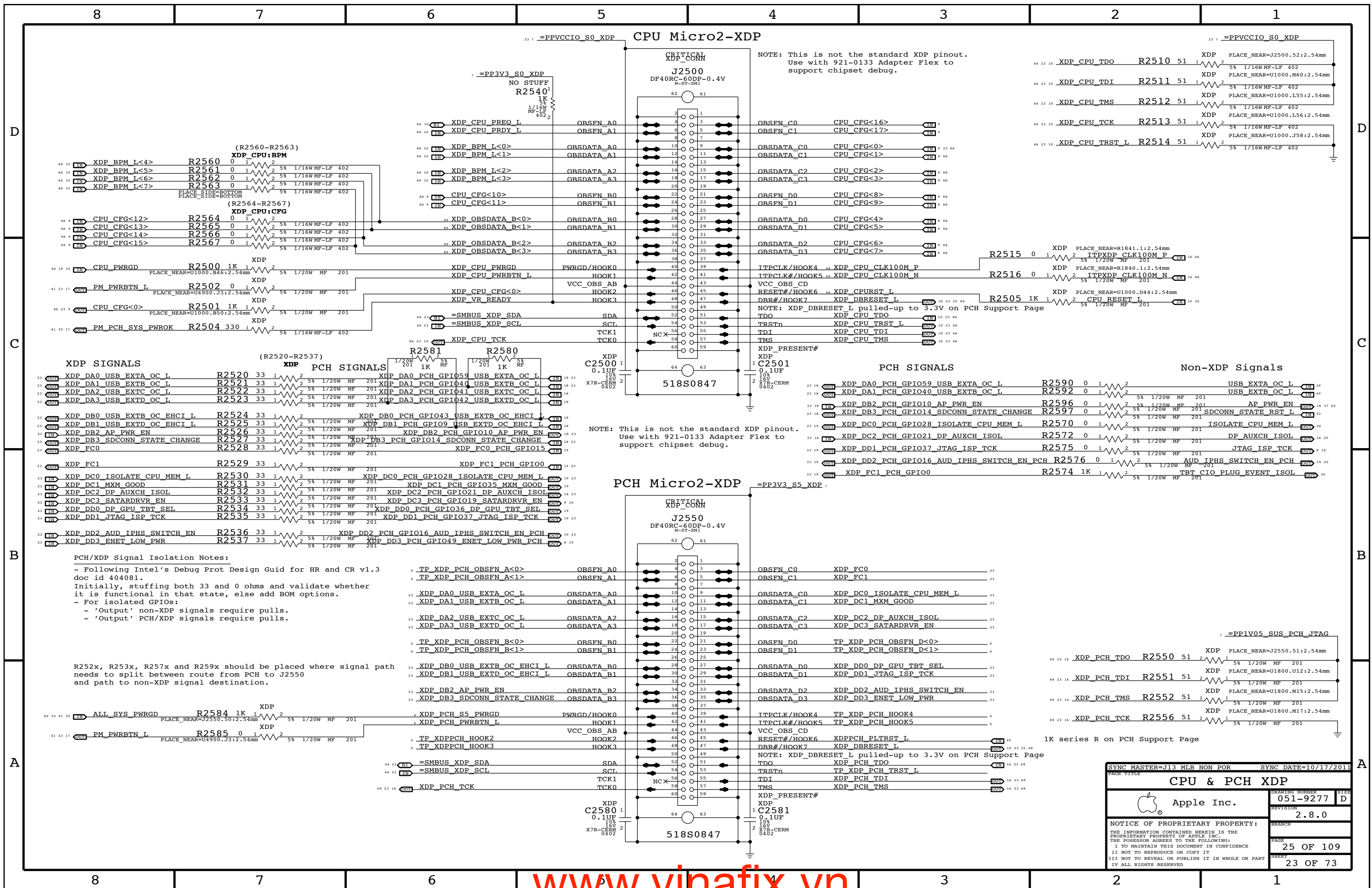
PCH GROUNDS

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PAGE TITLE		SYNC DATE=10/03/2011	
PCB DECOUPLING			
 Apple Inc.	DRAWING NUMBER	051-9277	SIZE
	REVISION	2.8.0	
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	PAGE	24 OF 109	
	SHEET	22 OF 73	



NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

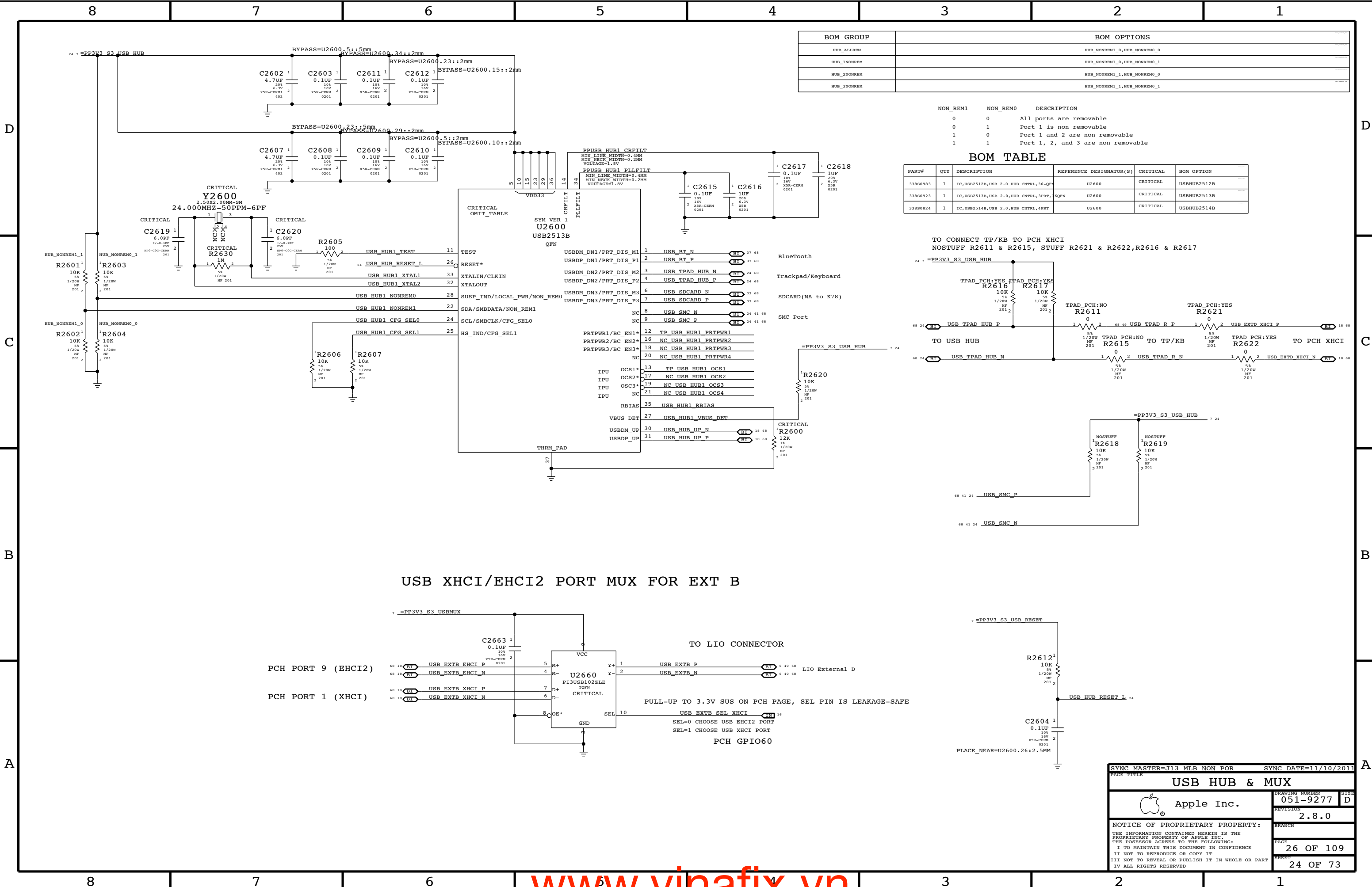
NOTE: XDP_DBRESET L pulled-up to 3.3V on PCH Support Page

1K series R on PCH Support Page

PCH/XDP Signal Isolation Notes:
 - Following Intel's Debug Prot Design Guid for HR and CR v1.3 doc id 404081.
 Initially, stuffing both 33 and 0 ohms and validate whether it is functional in that state, else add BOM options.
 - For isolated GPIOs:
 - 'Output' non-XDP signals require pulls.
 - 'Output' PCH/XDP signals require pulls.

R252x, R253x, R257x and R259x should be placed where signal path needs to split between route from PCH to J2550 and path to non-XDP signal destination.

PAGE TITLE		SYNC DATE=10/17/2011	
CPU & PCH XDP		DRAWING NUMBER	SIZE
Apple Inc.		051-9277	D
REVISION		2.8.0	
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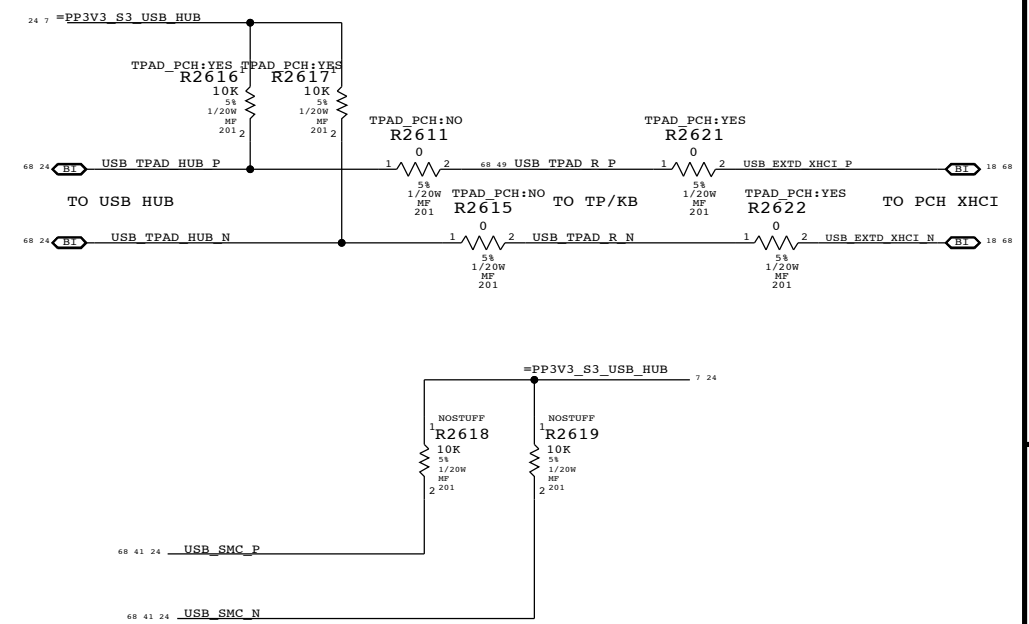
BOM GROUP		BOM OPTIONS	
HUB_ALLREM		HUB_NONREM1_0, HUB_NONREM0_0	
HUB_1NONREM		HUB_NONREM1_0, HUB_NONREM0_1	
HUB_2NONREM		HUB_NONREM1_1, HUB_NONREM0_0	
HUB_3NONREM		HUB_NONREM1_1, HUB_NONREM0_1	

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

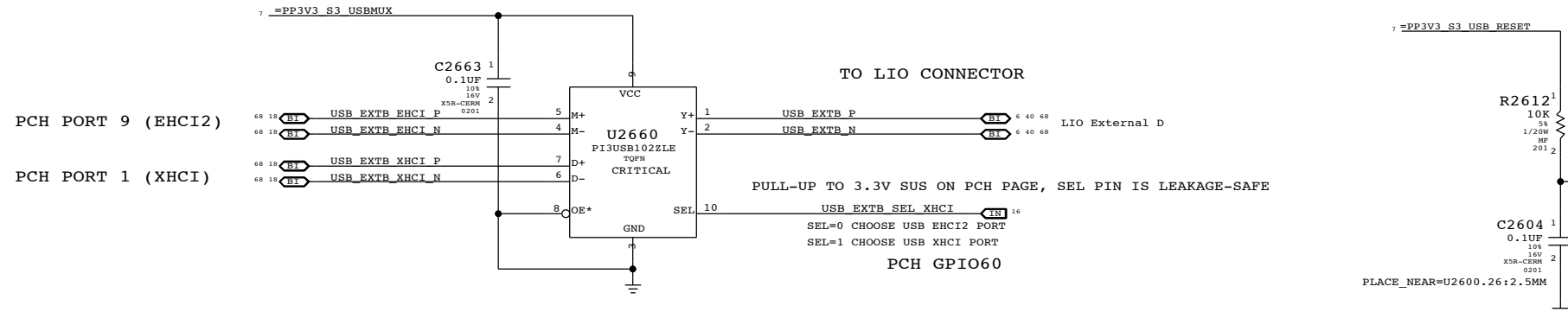
BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33880983	1	IC,USB2512B,USB 2.0 HUB CNTRL,36-QFN	U2600	CRITICAL	USBHUB2512B
33880923	1	IC,USB2513B,USB 2.0,HUB CNTRL,3PRT,46QFN	U2600	CRITICAL	USBHUB2513B
33880824	1	IC,USB2514B,USB 2.0,HUB CNTRL,4PRT	U2600	CRITICAL	USBHUB2514B

TO CONNECT TP/KB TO PCH XHCI
 NOSTUFF R2611 & R2615, STUFF R2621 & R2622, R2616 & R2617

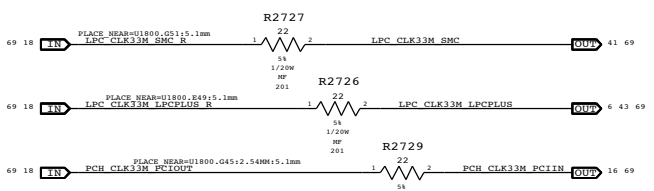
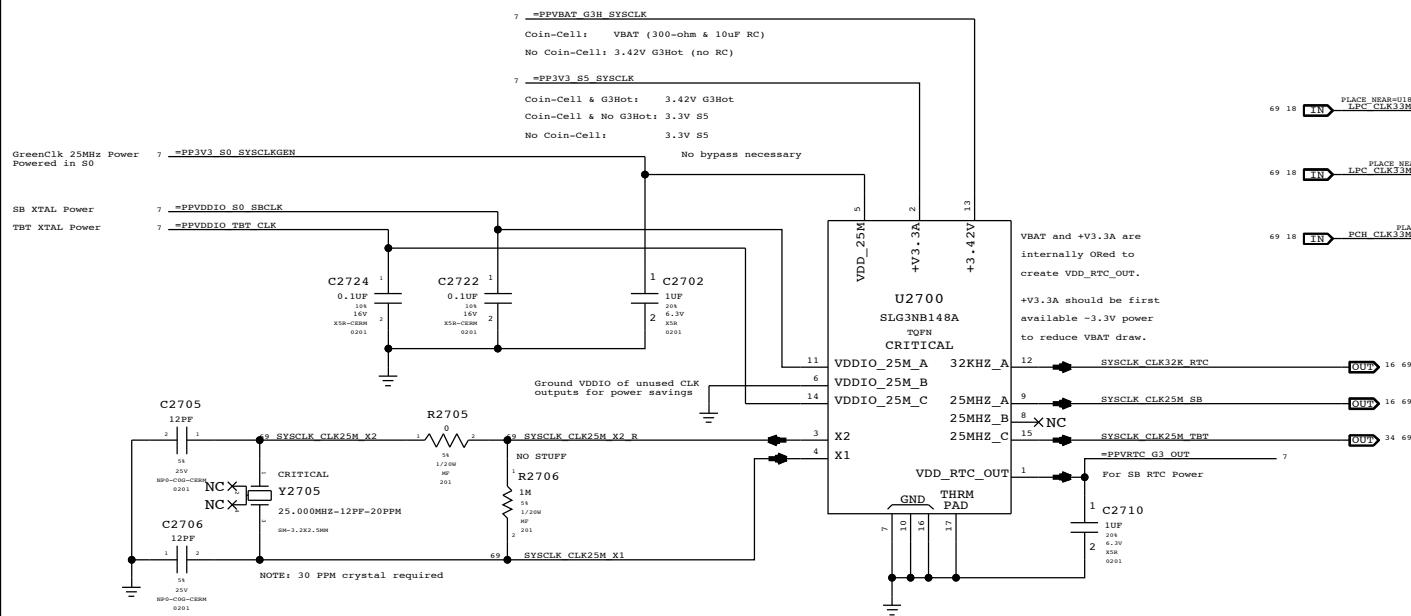


USB XHCI/EHCI2 PORT MUX FOR EXT B



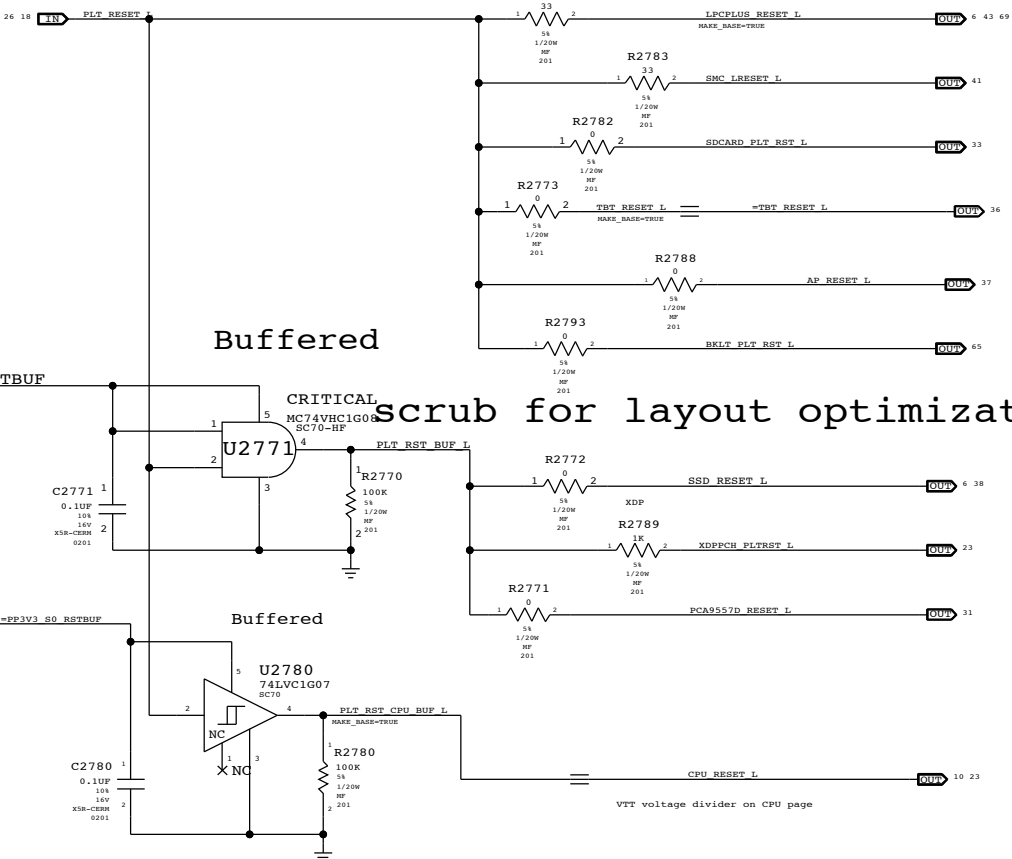
SYNC MASTER=J13 MLB NON POR		SYNC DATE=11/10/2011	
USB HUB & MUX			
Apple Inc.		DRAWING NUMBER	051-9277
		REVISION	2.8.0
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		SHEET	24 OF 73
		SIZE	D

System RTC Power Source & 32kHz / 25MHz Clock Generator

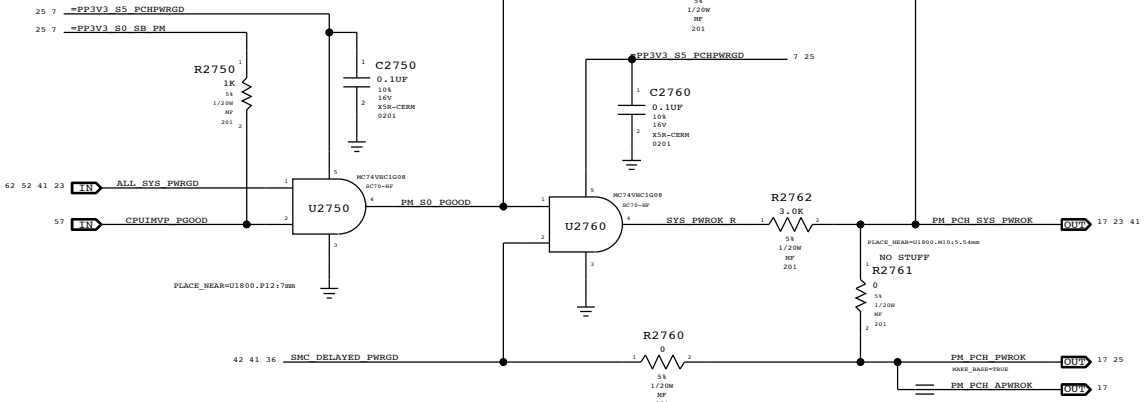


Platform Reset Connections
Unbuffered

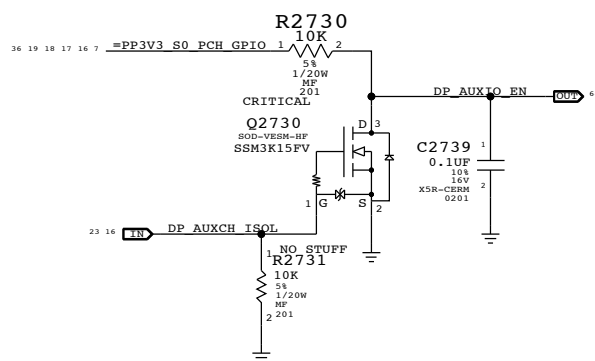
Buffered



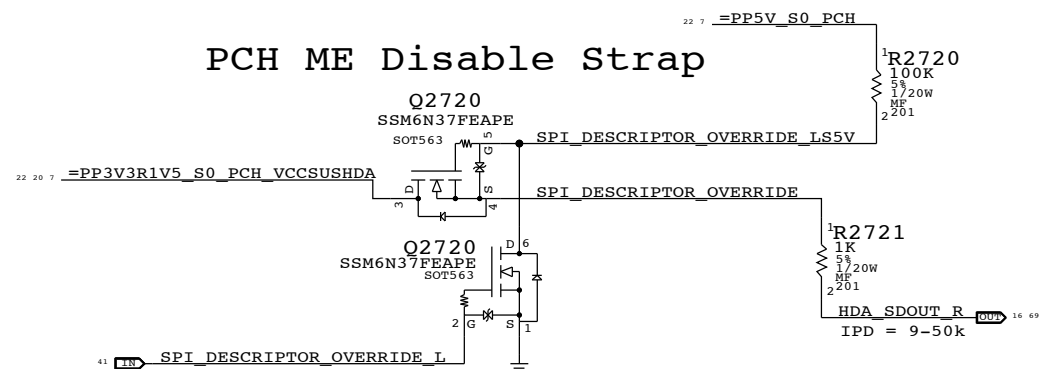
PCH S0 PWRGD



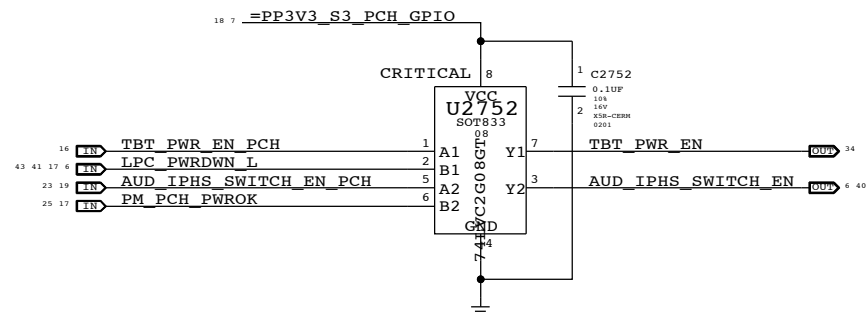
DP_AUXIO_EN Inversion



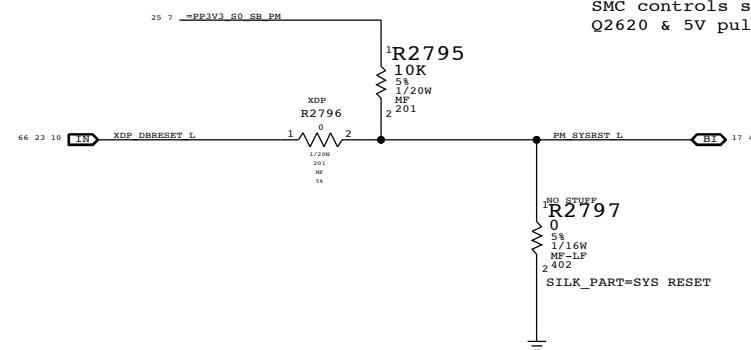
PCH ME Disable Strap



GPIO Glitch Prevention



PCH Reset Button



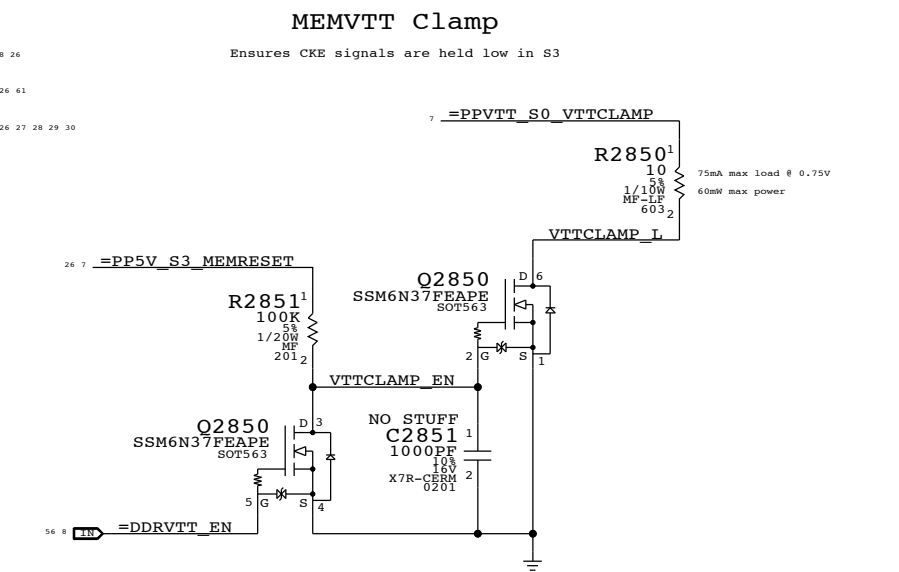
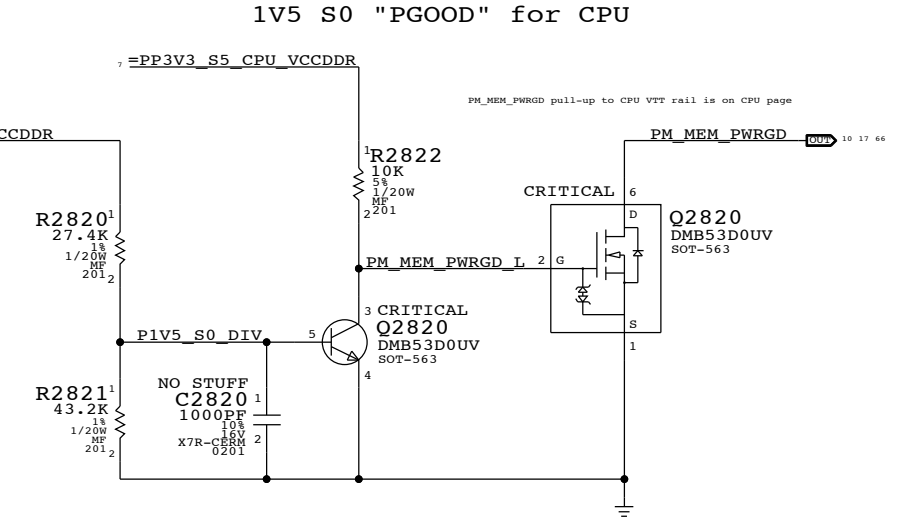
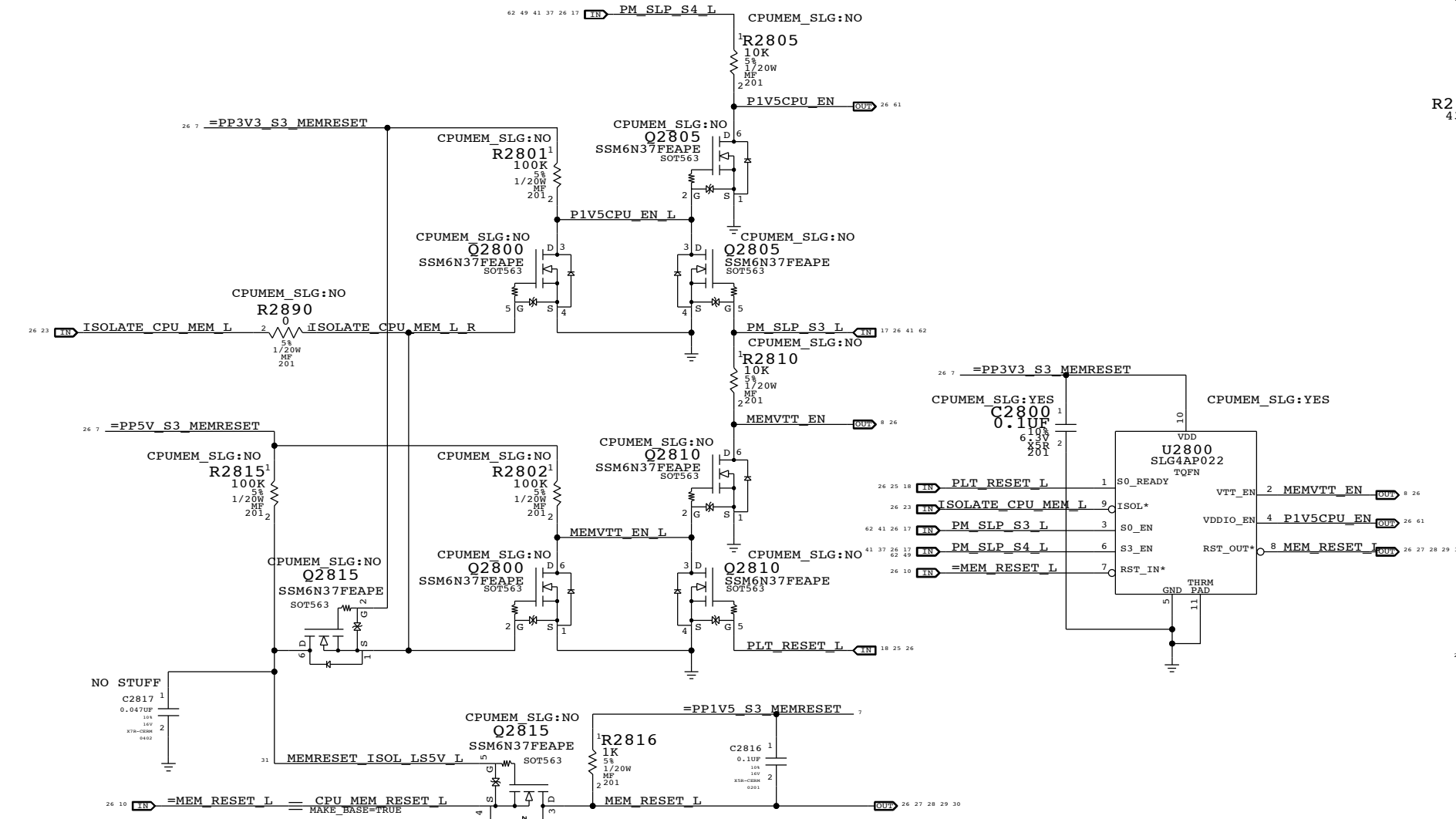
PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q2620 & 5V pull-up allows circuit to work regardless of HDA voltage.

PAGE TITLE		DRAWING NUMBER		SIZE
Clock (CK505) and Chipset Support		051-9277		D
Apple Inc.		REVISION		
		2.8.0		
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The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3->S0 transitions determines behavior of signals.
 WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
 WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

$P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L$
 $MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L$
 $MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L$

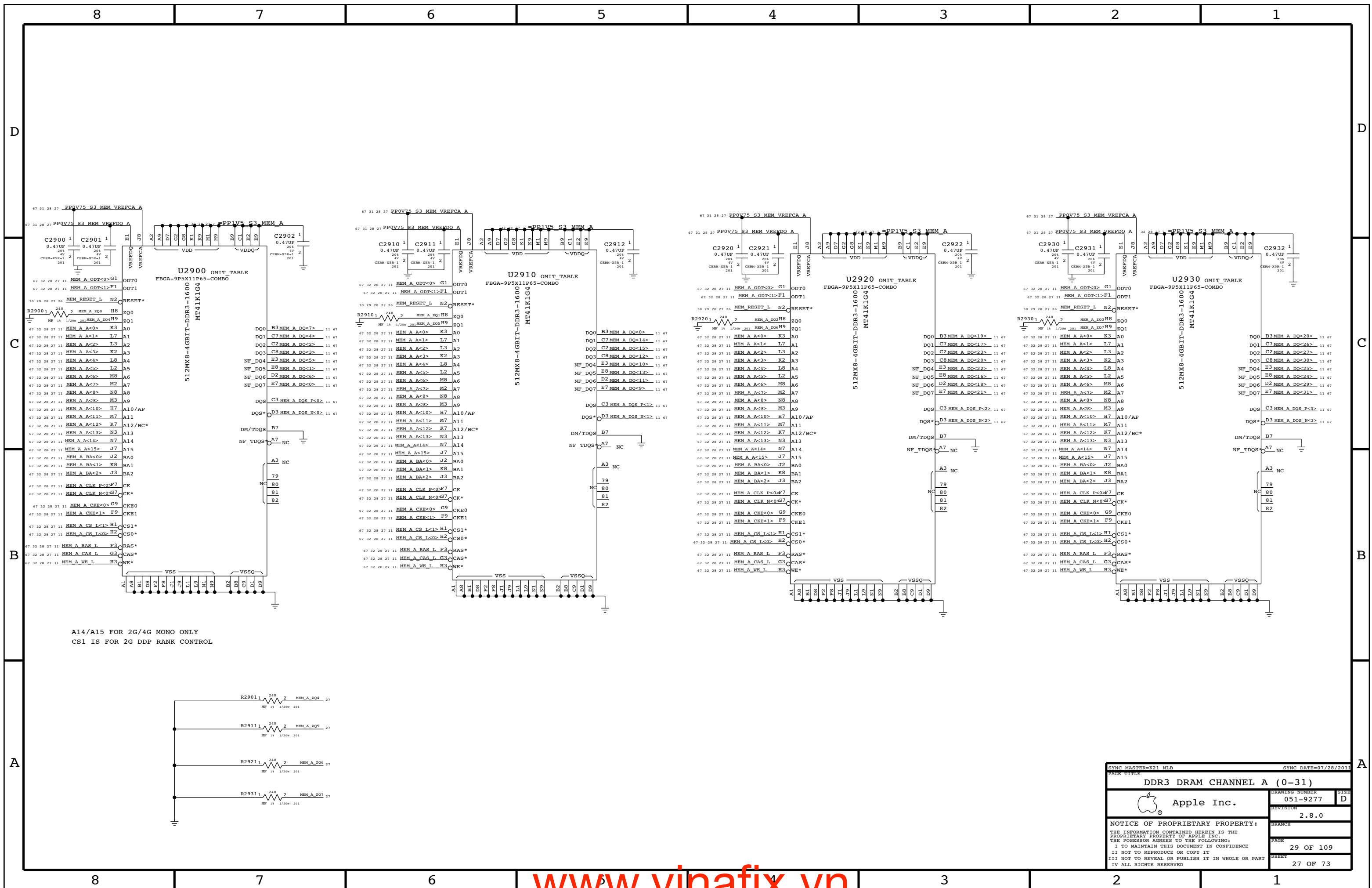


Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPUMEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPUMEM_RESET_L	1	1
to	1	0	1	1	1	1	0	1
2	0	0	0	1	1	0	0	1
3	0	0	0	1	X	0	0	1
S3	4	0	0	1	X	0	0	1
to	5	0	1	1	0 (*)	1	1	1
6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	CPUMEM_RESET_L	1	1

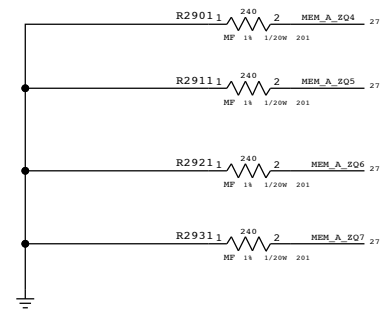
(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

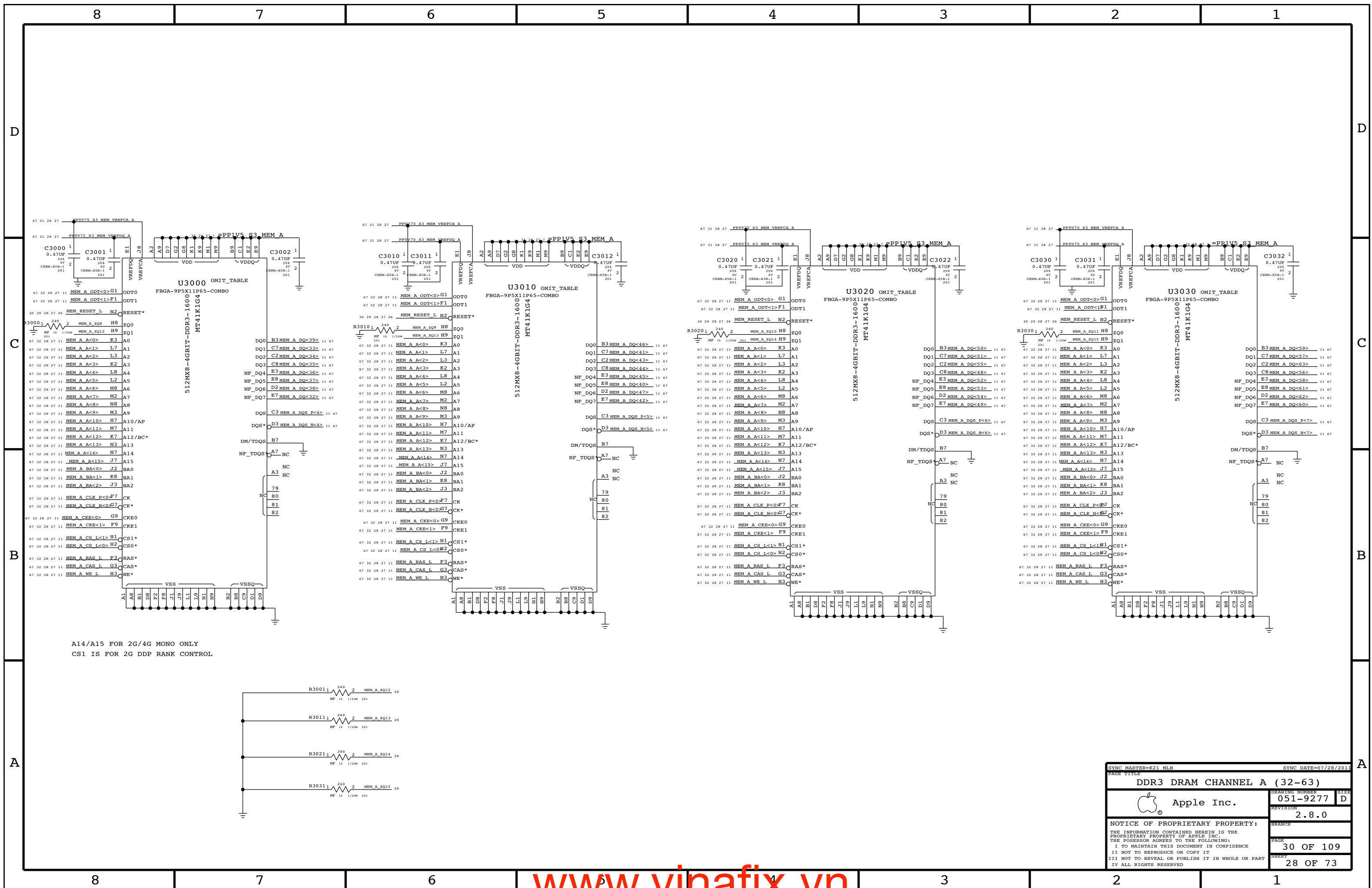
SYNC MASTER:113 MEM_REV:002 SYNC DATE:11/10/2011
 CPU Memory S3 Support
 Apple Inc.
 DRAWING NUMBER: 051-9277
 REVISION: 2.8.0
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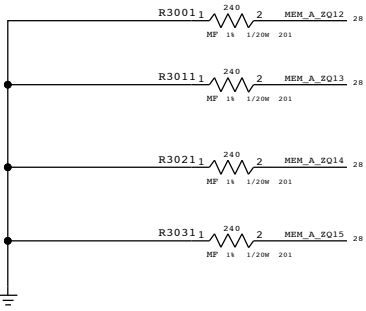
A14/A15 FOR 2G/4G MONO ONLY
 CS1 IS FOR 2G DDP RANK CONTROL



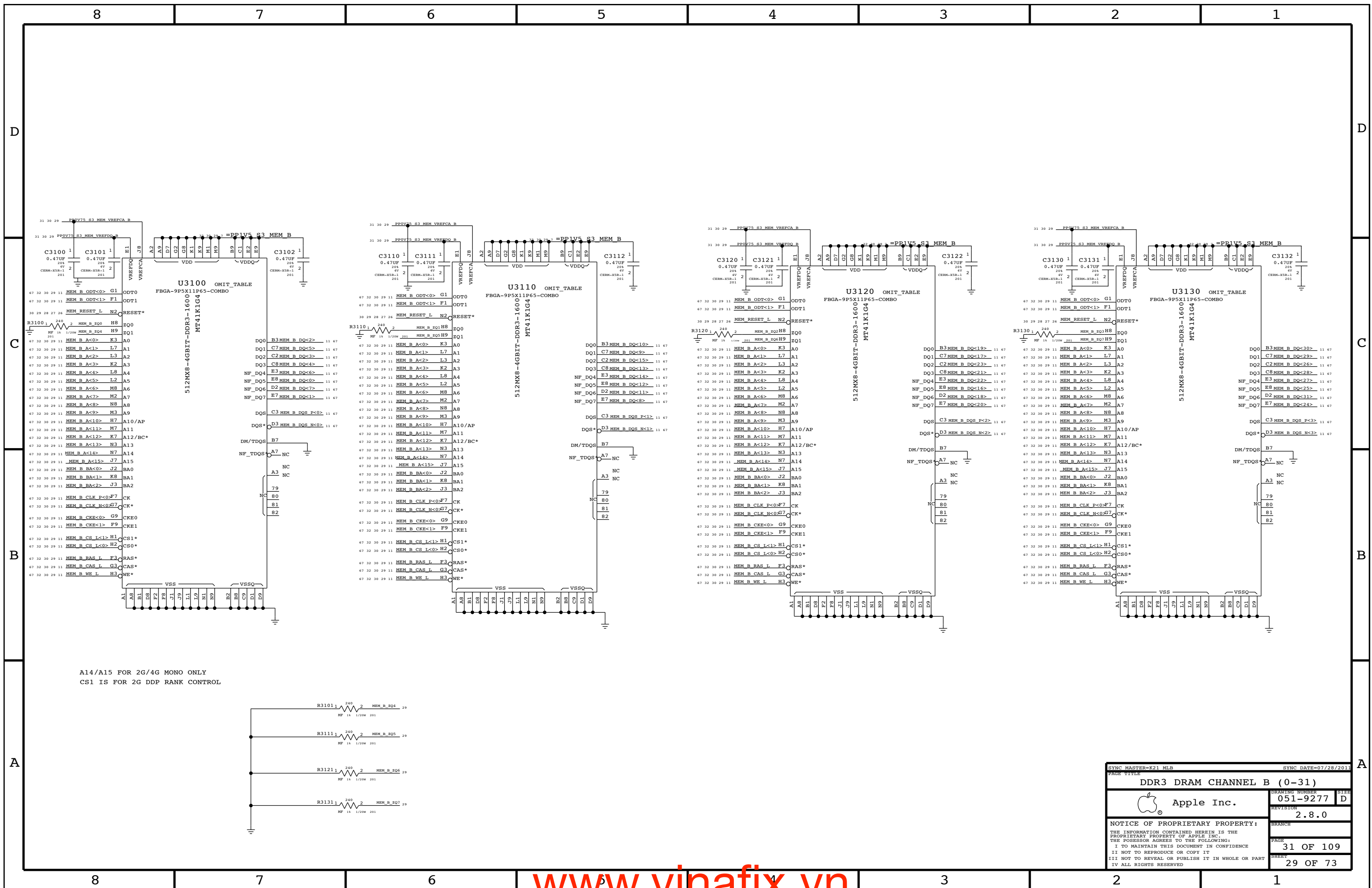
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PAGE TITLE			
DDR3 DRAM CHANNEL A (0-31)			
DRAWING NUMBER		SIZE	
051-9277		D	
REVISION		BRANCH	
2.8.0			
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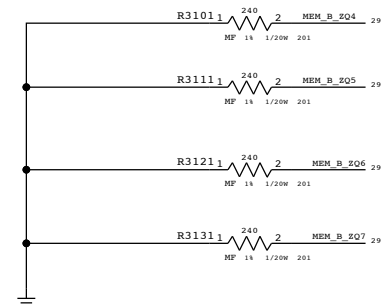
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 CS1 IS FOR 2G DDP RANK CONTROL



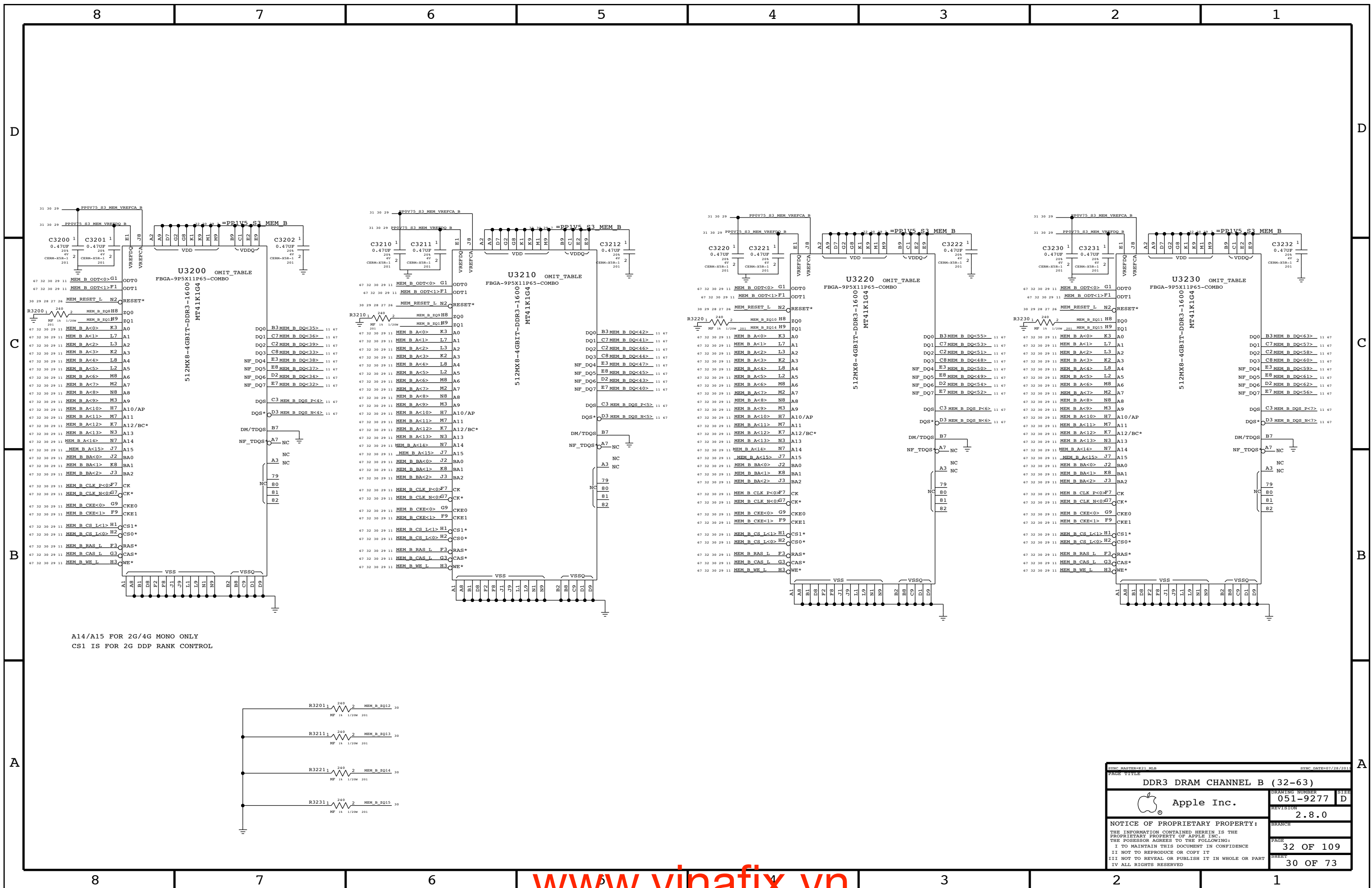
SYNC MASTER=K21 MLB		SYNC DATE=07/28/2011	
PAGE TITLE			
DDR3 DRAM CHANNEL A (32-63)			
Apple Inc.		DRAWING NUMBER	SIZE
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		2.8.0	
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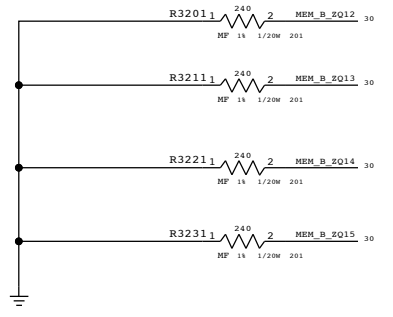
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SYNC MASTER=K21 MLB		SYNC DATE=07/28/2011	
PAGE TITLE			
DDR3 DRAM CHANNEL B (0-31)			
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A14/A15 FOR 2G/4G MONO ONLY
 CS1 IS FOR 2G DDP RANK CONTROL



SYNCH MASTER#11 MEM		SYNCH DATE#07/28/2011	
PAGE TITLE			
DDR3 DRAM CHANNEL B (32-63)			
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		REVISION	2.8.0
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NOTE: Must not enable more than two SO-DIMM margining buffers at once or Vref source may be overloaded.

D

D

C

C

B

B

A

A

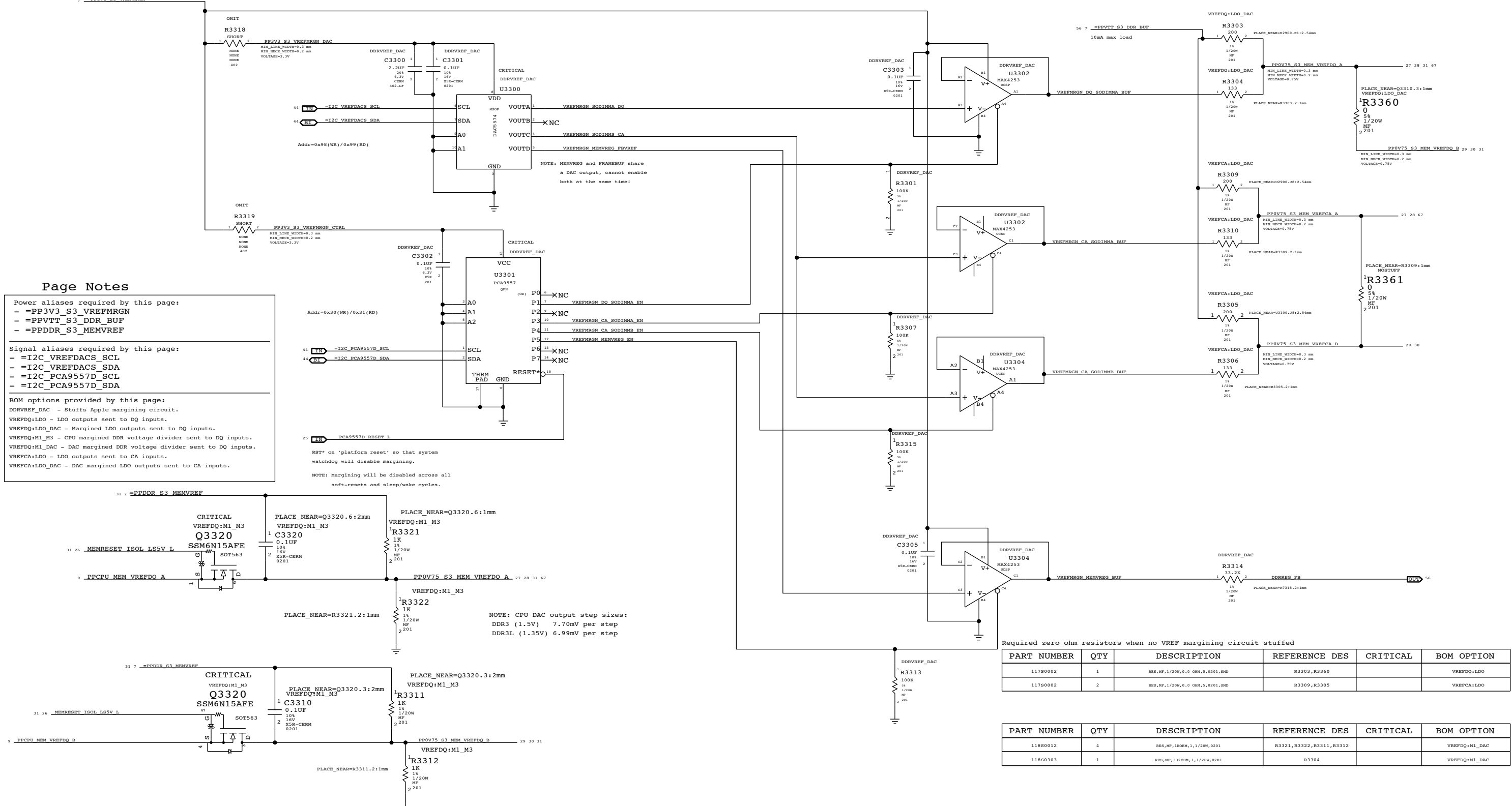
Page Notes

Power aliases required by this page:
 - =PP3V3_S3_VREFMRGN
 - =PPVTT_S3_DDR_BUF
 - =PPDDR_S3_MEMVREF

Signal aliases required by this page:
 - =I2C_VREFDACS_SCL
 - =I2C_VREFDACS_SDA
 - =I2C_PCA9557D_SCL
 - =I2C_PCA9557D_SDA

BOM options provided by this page:
 DDRVREF_DAC - Stuffs Apple margining circuit.
 VREFDQ:LDO - LDO outputs sent to DQ inputs.
 VREFDQ:LDO_DAC - Margined LDO outputs sent to DQ inputs.
 VREFDQ:M1_M3 - CPU margined DDR voltage divider sent to DQ inputs.
 VREFDQ:M1_DAC - DAC margined DDR voltage divider sent to DQ inputs.
 VREFCA:LDO - LDO outputs sent to CA inputs.
 VREFCA:LDO_DAC - DAC margined LDO outputs sent to CA inputs.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11780002	1	RES,HP,1/20W,0.0 OHM,S,0201,SMD	R3303,R3360		VREFDQ:LDO
11780002	2	RES,HP,1/20W,0.0 OHM,S,0201,SMD	R3309,R3305		VREFCA:LDO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11880012	4	RES,HP,180HM,1,1/20W,0201	R3321,R3322,R3311,R3312		VREFDQ:M1_DAC
11880303	1	RES,HP,3320HM,1,1/20W,0201	R3304		VREFDQ:M1_DAC

NOTE: CPU DAC output step sizes:
 DDR3 (1.5V) 7.70mV per step
 DDR3L (1.35V) 6.99mV per step

Required zero ohm resistors when no VREF margining circuit stuffed

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% Vref)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xF7)
Vref current:	+3.4mA - -3.4mA (- = sourced)				+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

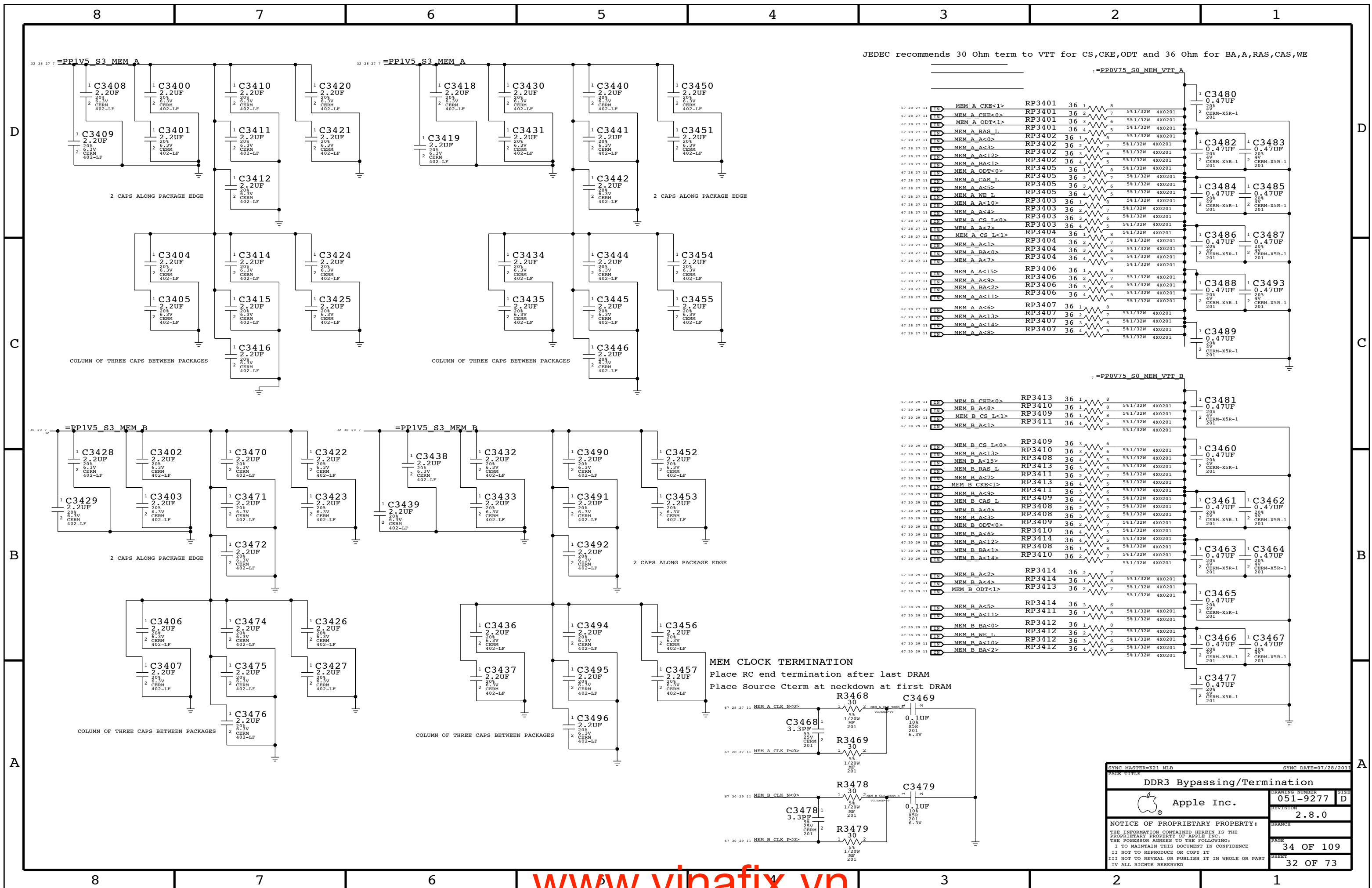
SYMC MASTER(1) MBR SYMC DATE(08/06/2015)
 PAGE TITLE

FSB/DDR3/FRAMBUF Vref Margining

Apple Inc.

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JEDEC recommends 30 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE

MEM CLOCK TERMINATION
Place RC end termination after last DRAM
Place Source Term at neckdown at first DRAM

SYNC MASTER=K21 MLB SYNC DATE=07/28/2011
PAGE TITLE

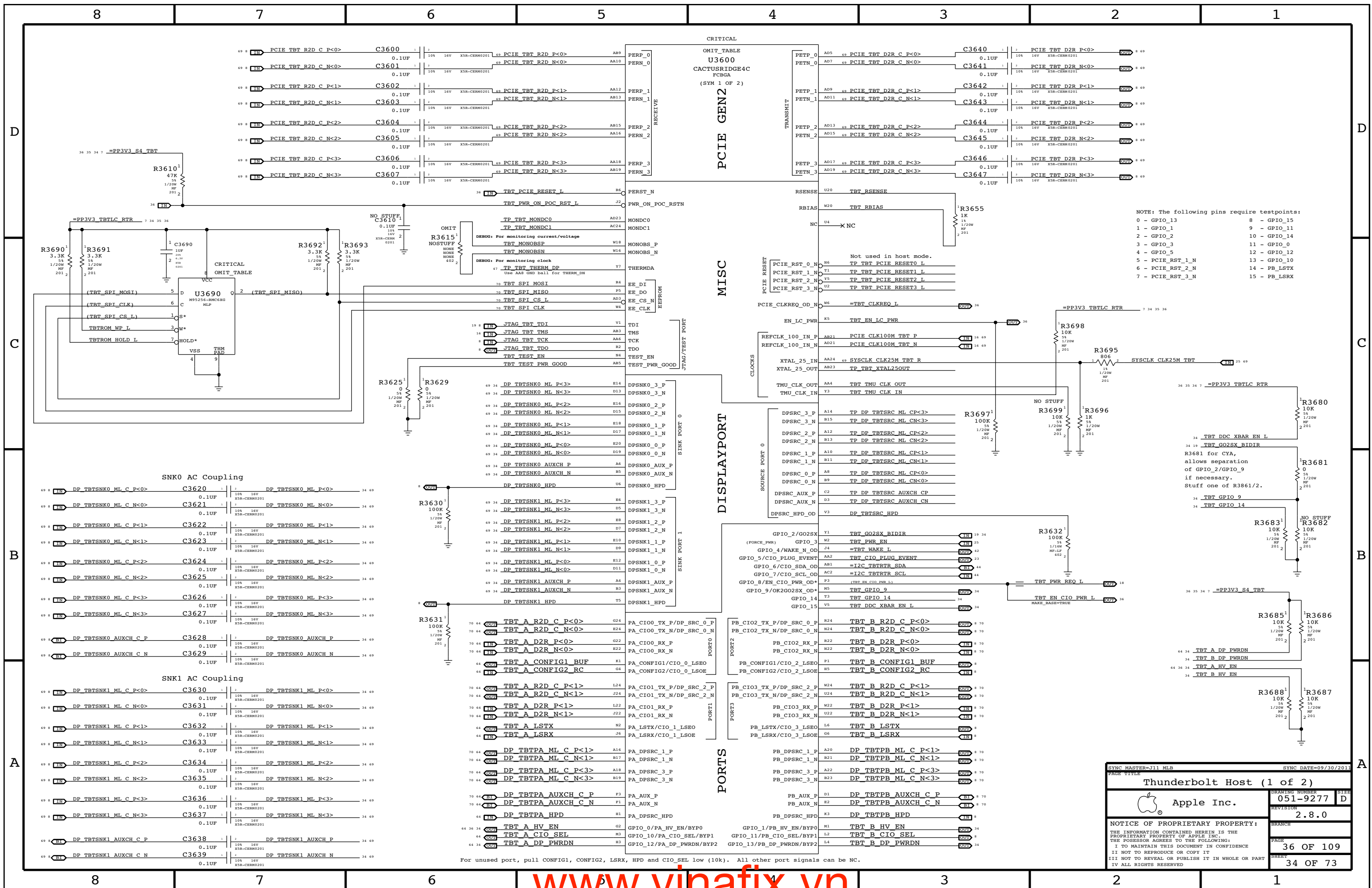
DDR3 Bypassing/Termination

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REVISION: 2.8.0

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SHEET: 32 OF 73



CRITICAL

U3600
CACTUSBRIDGE4C
FCBGA
(SYM 1 OF 2)

PCIE GEN2

MISC

DISPLAYPORT

PORTS

NOTE: The following pins require testpoints:

0 - GPIO_13	8 - GPIO_15
1 - GPIO_1	9 - GPIO_11
2 - GPIO_2	10 - GPIO_14
3 - GPIO_3	11 - GPIO_0
4 - GPIO_5	12 - GPIO_12
5 - PCIE_RST_1_N	13 - GPIO_10
6 - PCIE_RST_2_N	14 - PB_LSTX
7 - PCIE_RST_3_N	15 - PB_LSRX

SNK0 AC Coupling

SNK1 AC Coupling

SYNC MASTER=111 MLB SYNC DATE=09/30/2011

Thunderbolt Host (1 of 2)

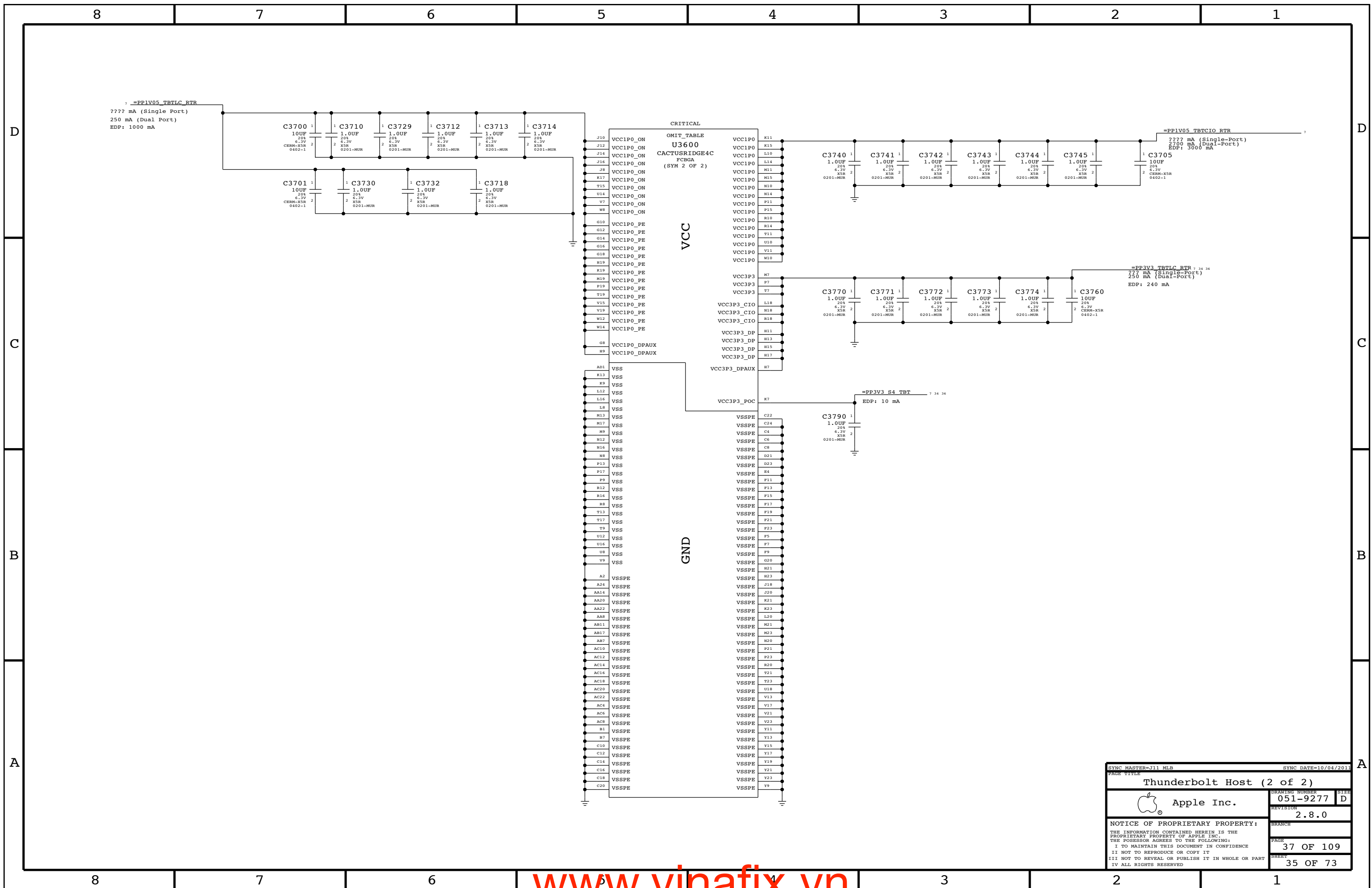
Apple Inc.

DRAWING NUMBER: 051-9277 SIZE: D

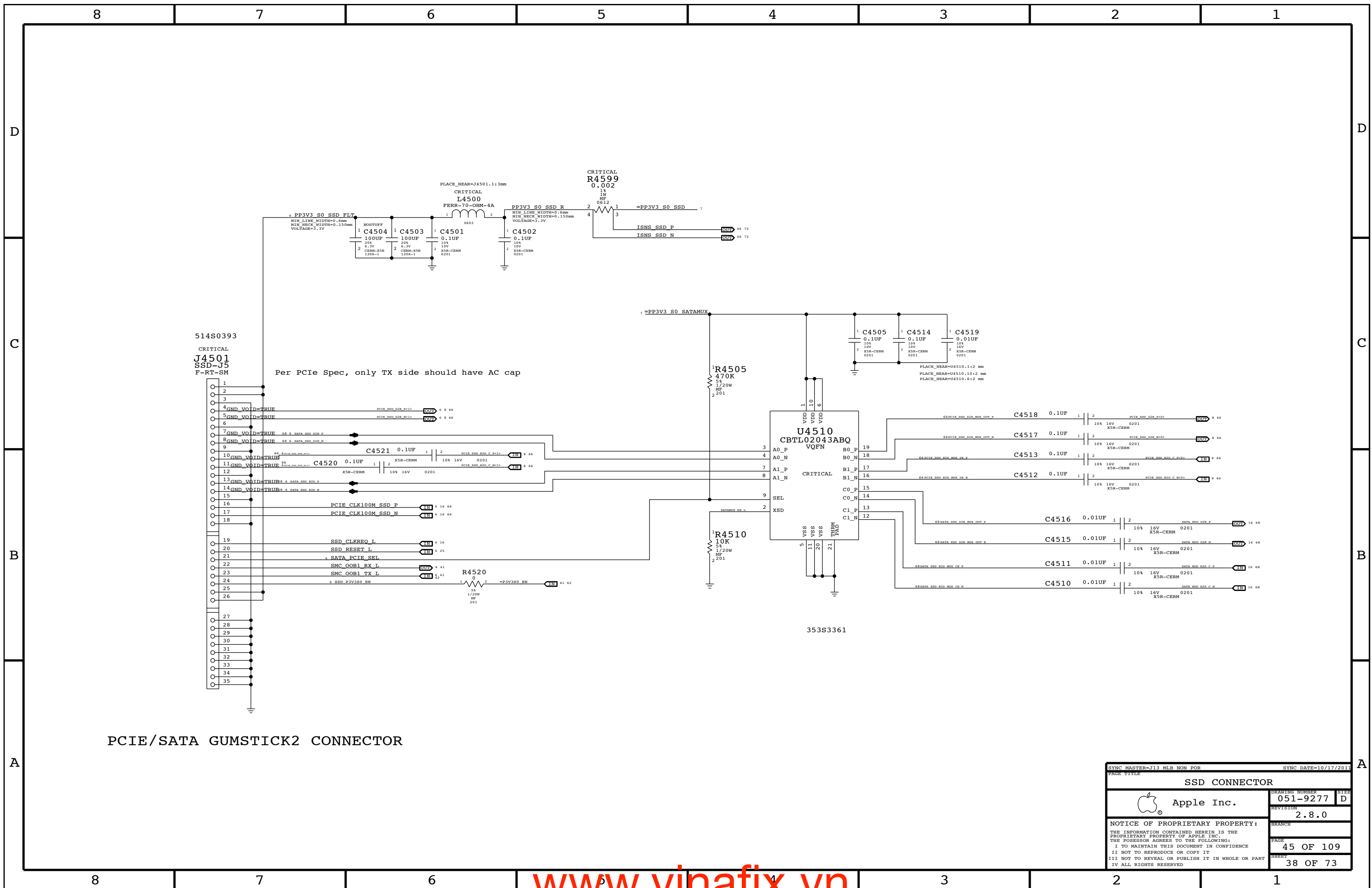
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SYNC MASTER=J11 MLB		SYNC DATE=10/04/2011	
Thunderbolt Host (2 of 2)			
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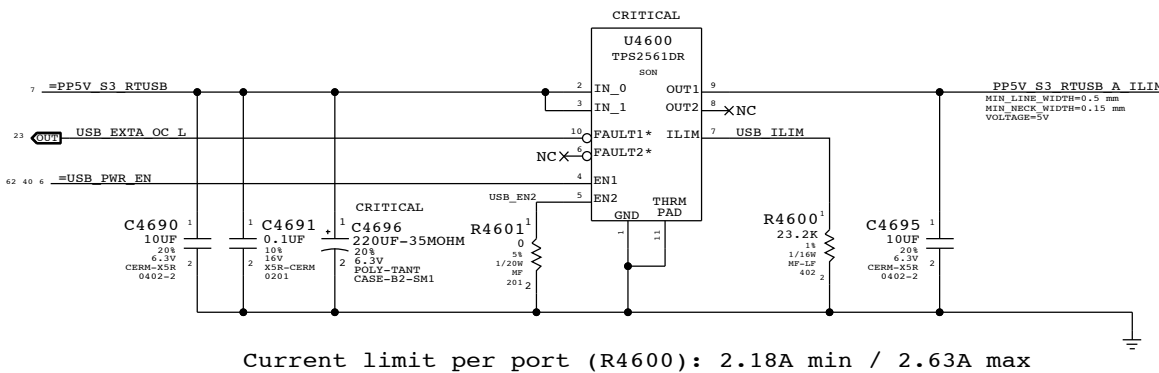


PCIE/SATA GUMSTICK2 CONNECTOR

SYNC MASTER=J13 MLB NON POR		SYNC DATE=10/17/2013	
SSD CONNECTOR			
Apple Inc.		DRAWING NUMBER	051-9277
		REVISION	2.8.0
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		PAGE	45 OF 109
		SHEET	38 OF 73

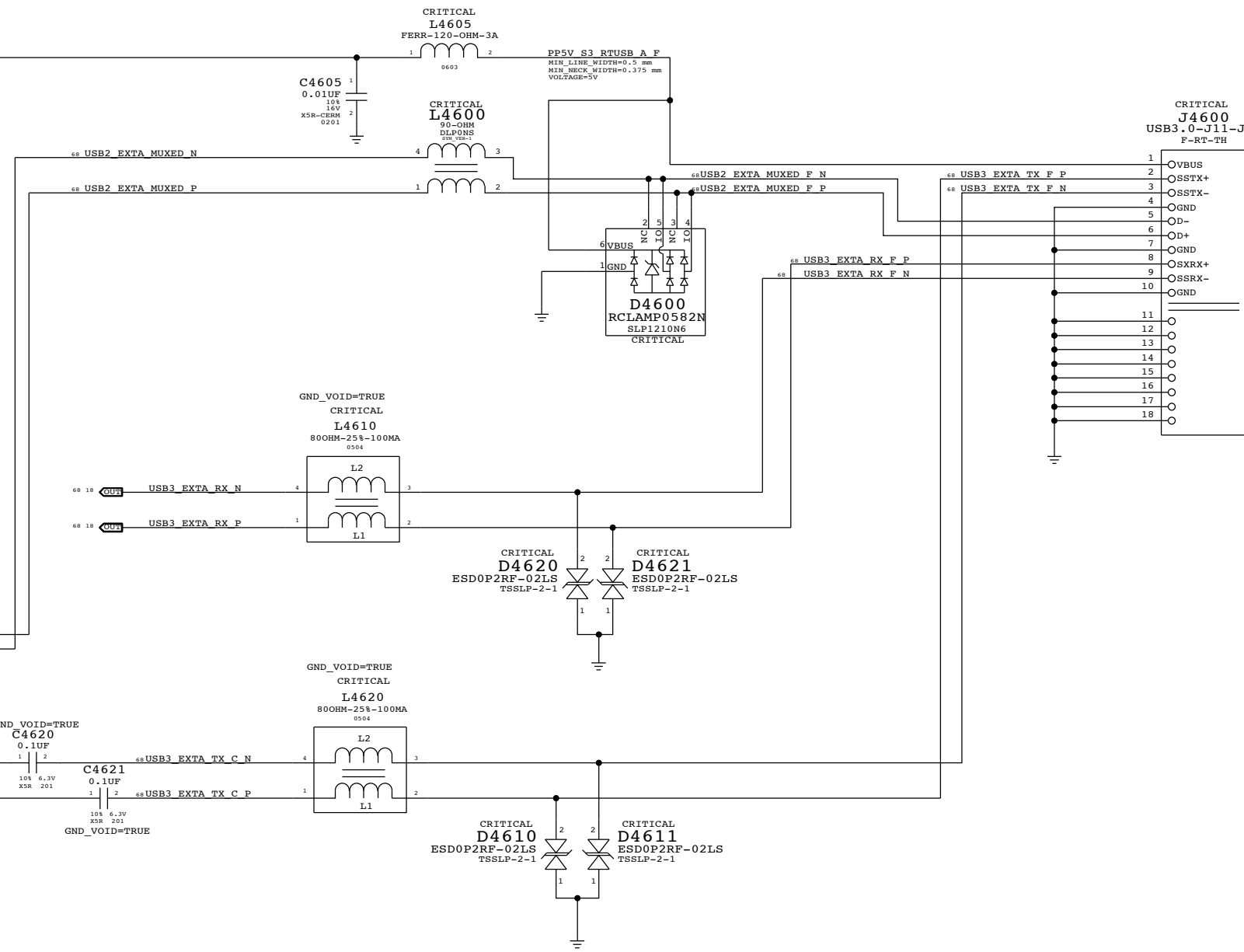
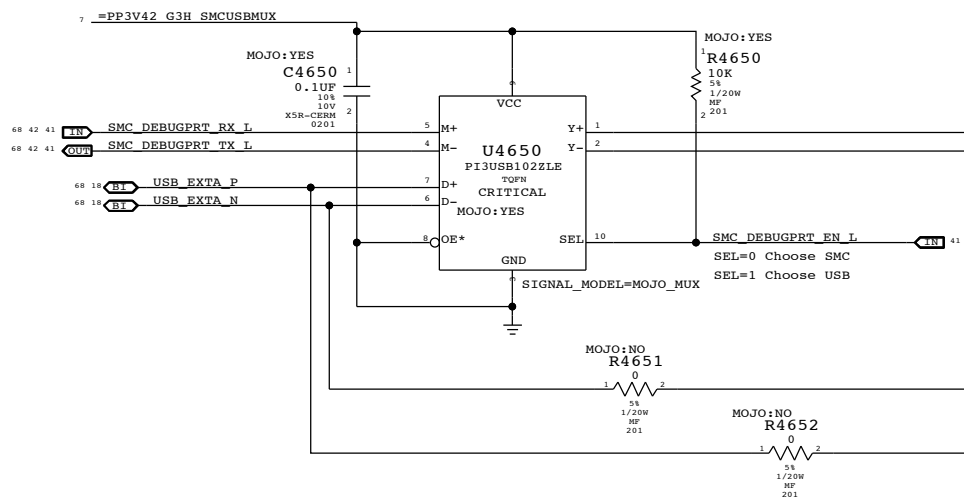
Right USB Port A

USB Port Power Switch

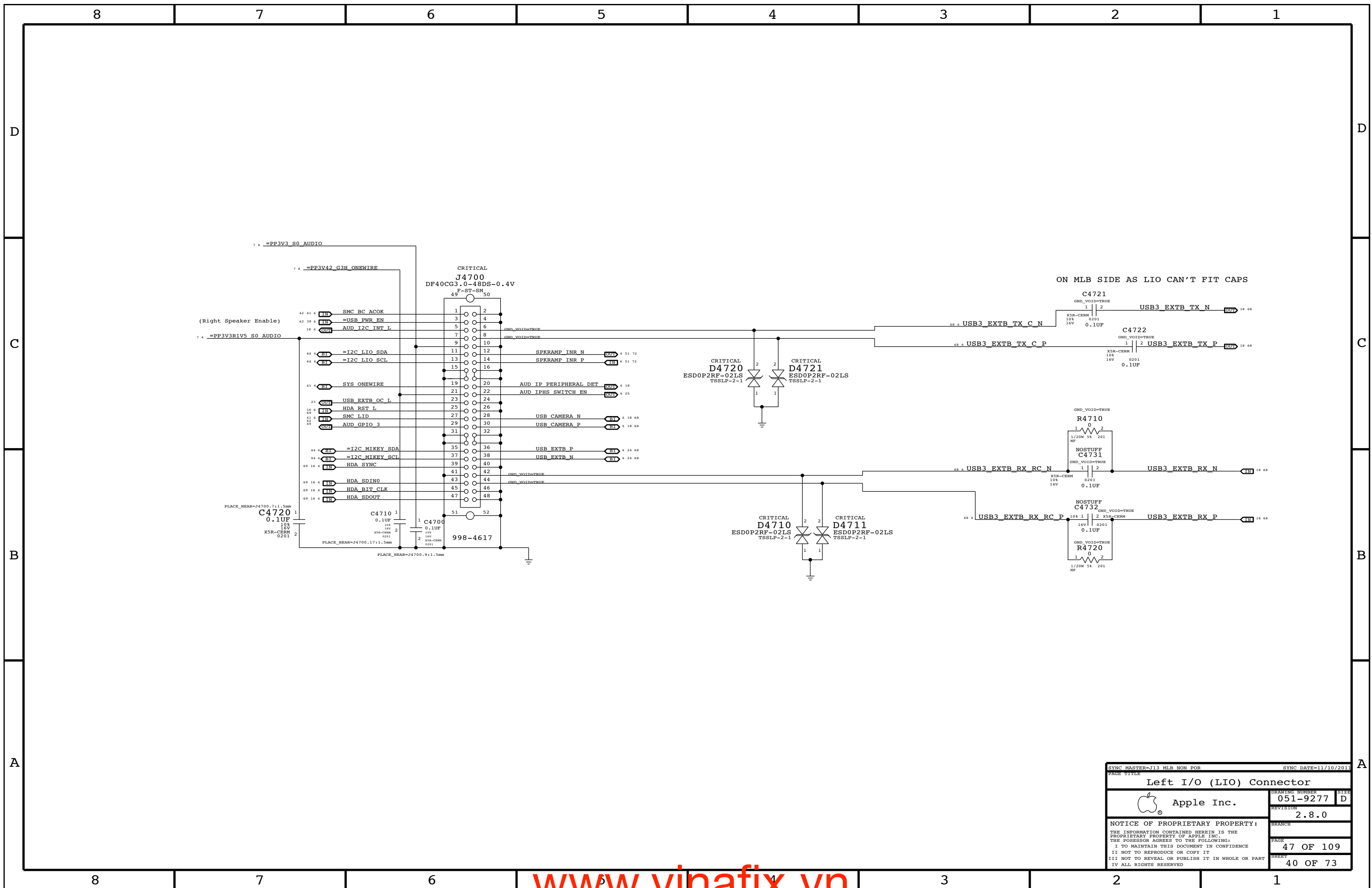


Current limit per port (R4600): 2.18A min / 2.63A max

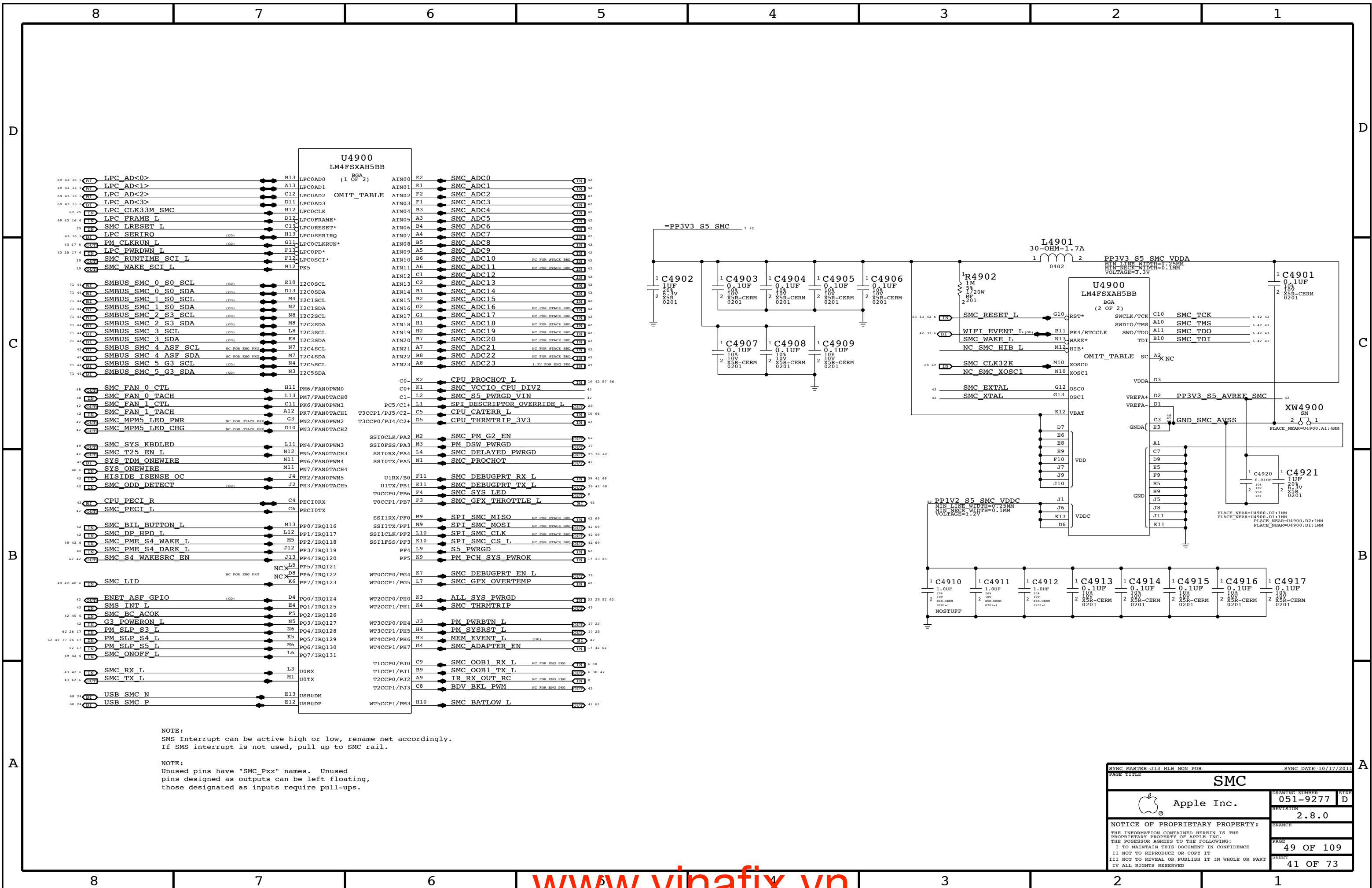
Mojo SMC Debug Mux



SYNC MASTER=J11_MLB		SYNC DATE=09/30/2013	
External A USB3 Connector			
Apple Inc.		DRAWING NUMBER	051-9277
		REVISION	2.8.0
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SYNC MASTER=J13 MLB NON POR		SYNC DATE=11/10/2011	
Left I/O (LIO) Connector			
Apple Inc.		DRAWING NUMBER	051-9277
		REVISION	2.8.0
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		PAGE	47 OF 109
		SHEET	40 OF 73

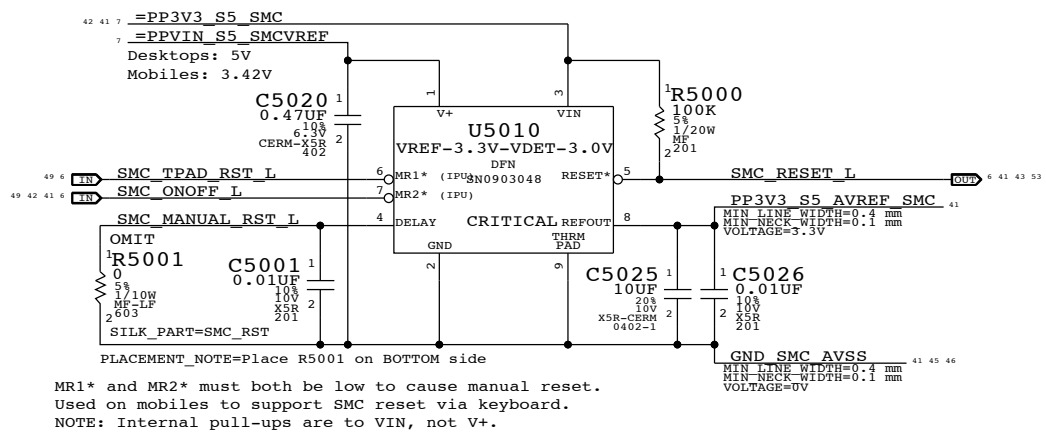


NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

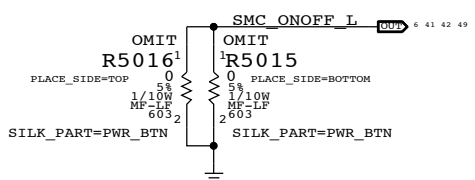
NOTE:
Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

PAGE TITLE		SYNC DATE=10/17/2011	
SMC		DRAWING NUMBER	SIZE
Apple Inc.		051-9277	D
		REVISION	
		2.8.0	
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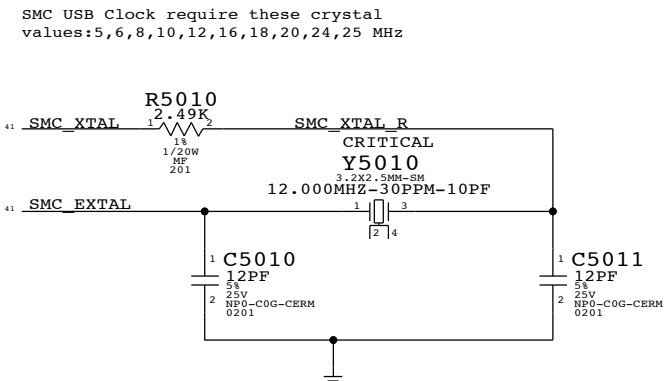
SMC Reset "Button", Supervisor & AVREF Supply



Debug Power "Buttons"



SMC Crystal Circuit

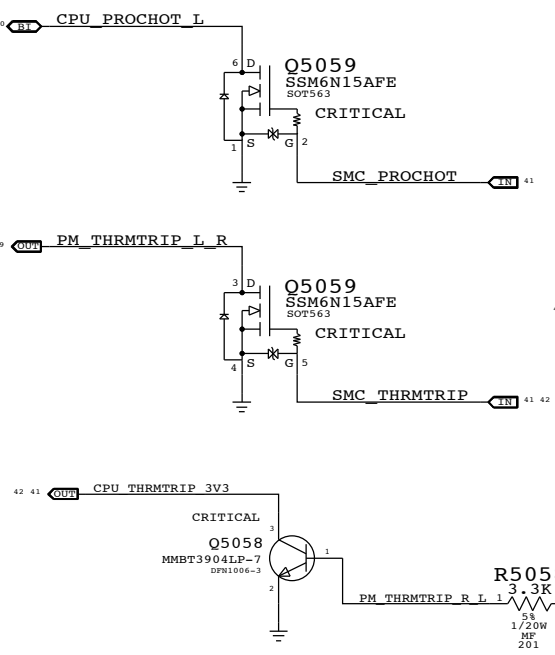
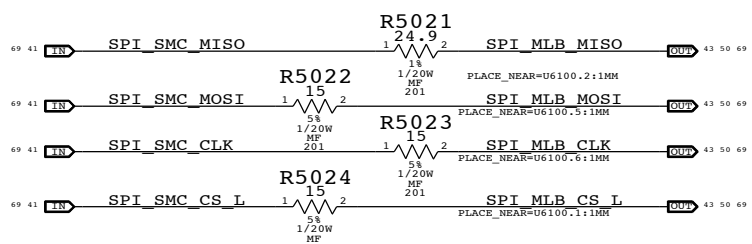


- SMC_ADC0 = SMC CPU VSENSE
- SMC_ADC1 = SMC CPU ISENSE
- SMC_ADC2 = SMC VCCSA VSENSE
- SMC_ADC3 = SMC DCIN VSENSE
- SMC_ADC4 = SMC DCIN ISENSE
- SMC_ADC5 = SMC PBUS VSENSE
- SMC_ADC6 = SMC HDD ISENSE
- SMC_ADC7 = SMC BMON ISENSE
- SMC_ADC8 = SMC HS COMPUTING ISENSE
- SMC_ADC9 = SMC OTHER HI ISENSE
- SMC_ADC10 = SMC 1V5S3 ISENSE
- SMC_ADC11 = SMC CPUVCCIO ISENSE
- SMC_ADC12 = SMC GFX VSENSE
- SMC_ADC13 = SMC CPU SA ISENSE
- SMC_ADC14 = SMC 3V3S0 ISENSE
- SMC_ADC15 = SMC WLAN ISENSE
- SMC_ADC16 = SMC LCDBKLT ISENSE
- SMC_ADC17 = NC SMC ADC17
- SMC_ADC18 = SMC GFX ISENSE
- SMC_ADC19 = NC SMC ADC19
- SMC_ADC20 = NC SMC ADC20
- SMC_ADC21 = NC SMC ADC21
- SMC_ADC22 = NC SMC ADC22
- SMC_ADC23 = SMC ADC23
- SMC_GFX_OVERTEMP = NC SMC GFX OVERTEMP
- SMC_GFX_THROTTLE_L = NC SMC GFX THROTTLE L
- SMC_FAN_1_CTL = NC SMC FAN_1_CTL
- SMC_FAN_1_TACH = NC SMC FAN_1_TACH
- ENET_ASF_GPIO = NC ENET_ASF_GPIO
- SMC_MPM5_LED_PWR = NC SMC MPM5_LED_PWR
- SMC_MPM5_LED_CHG = NC SMC MPM5_LED_CHG
- SYS_TDM_ONEWIRE = NC SYS_TDM_ONEWIRE

- SMC_DP_HPD_L = NC SMC DP_HPD_L
- CHGR_ACOK = SMC BC_ACOK
- HISIDE_ISENSE_OC = NC HISIDE_ISENSE_OC
- SMBUS_SMC_4_ASF_SCL = NC SMBUS_SMC_4_ASF_SCL
- SMBUS_SMC_4_ASF_SDA = NC SMBUS_SMC_4_ASF_SDA
- BDV_BKL_PWM = NC BDV_BKL_PWM
- SMC_PME_S4_DARK_L = SDCONN_STATE_CHANGE_SMC
- SMC_T25_EN_L = NC SMC T25_EN_L
- PM_CLK32K_SUSCLK_R1 = SMC_CLK32K

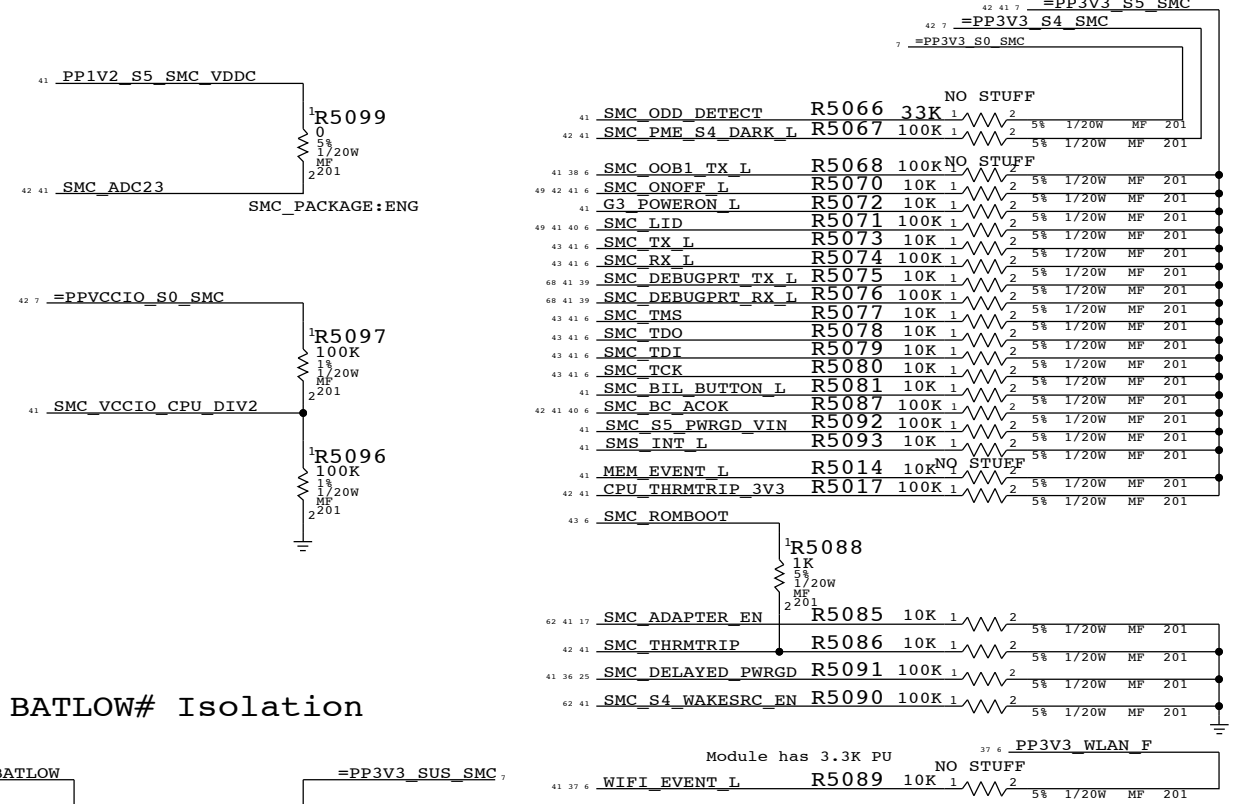
SMC12 SPI Support

Series resistors are no stuffed until the topology of 2 SPI Masters are verified.

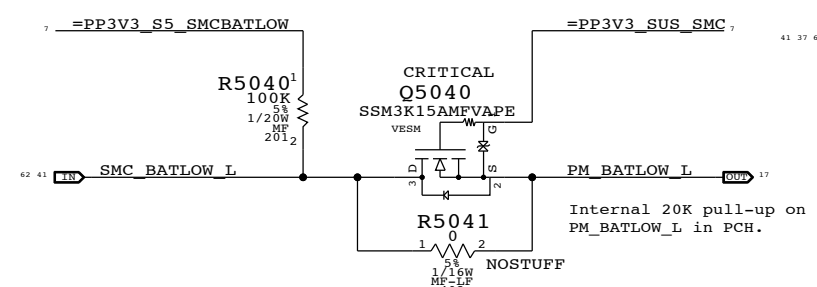


SMC12 Eng Pkg Support

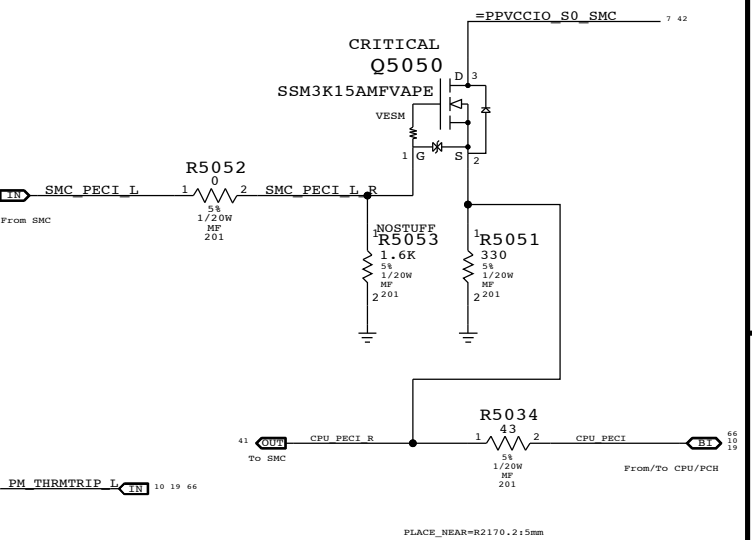
Eng Package requires 1.2V ON SMC_ADC23 pin.



BATLOW# Isolation



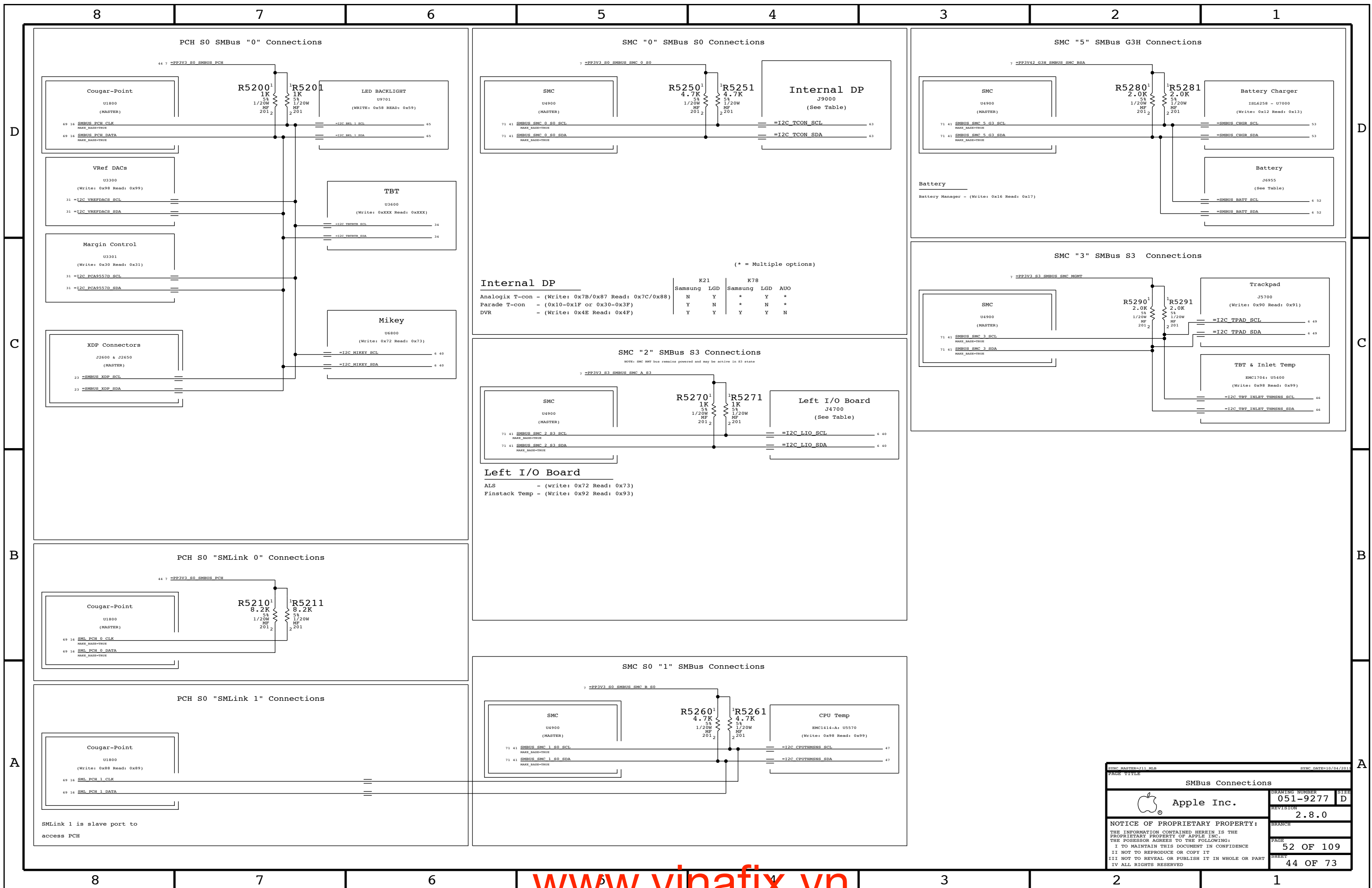
SMC12 PEIC Support



A

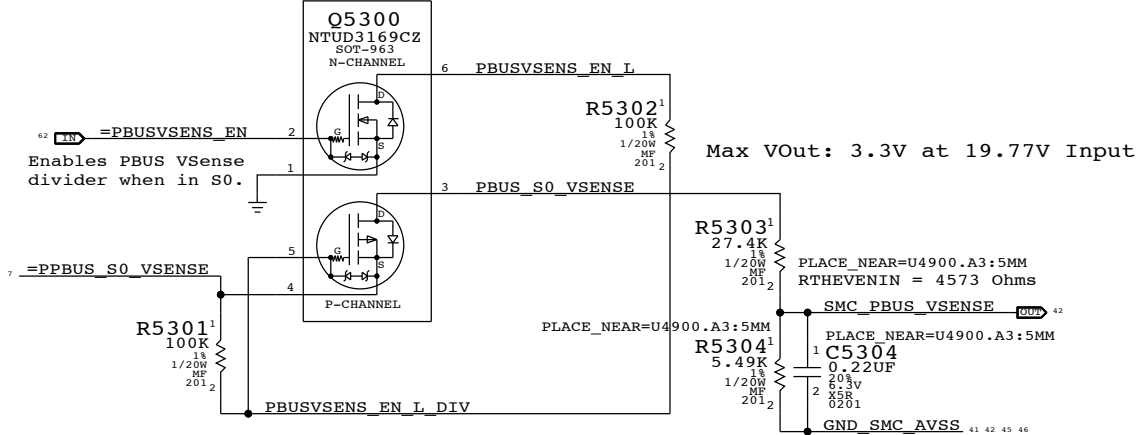
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SYNC MASTER=J13 MLB NON POR		SYNC DATE=11/10/2011	
SMC Support			
Apple Inc.		DRAWING NUMBER	SIZE
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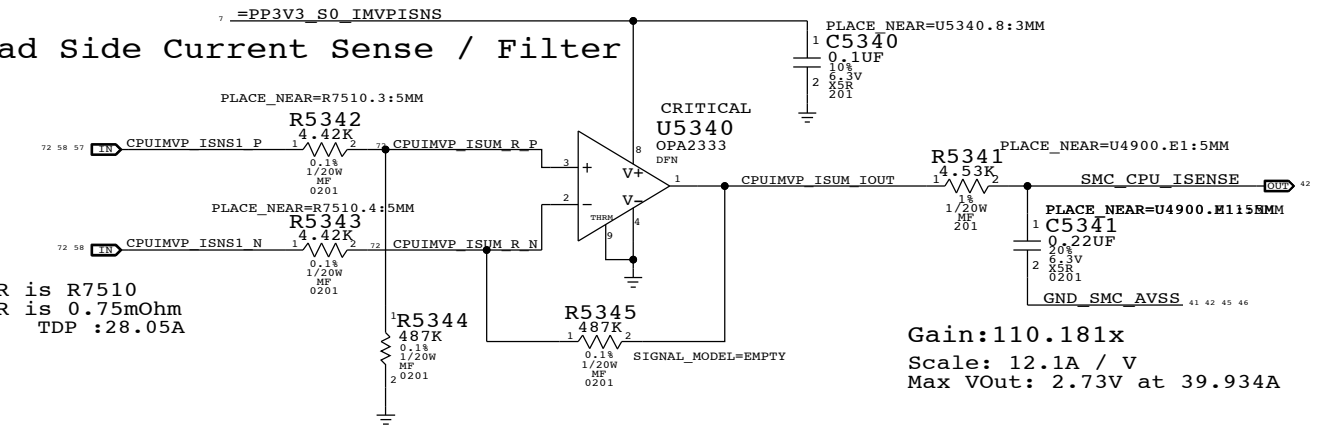
SYMC MASTER(1) MBR		SYMC DATE:10/04/2011	
PAGE TITLE			
SMBus Connections			
Apple Inc.		DRAWING NUMBER	SIZE
		051-9277	D
		REVISION	
		2.8.0	
		BRANCH	
		PAGE	
		52 OF 109	
		SHEET	
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PBUS Voltage Sense Enable & Filter



Max VOut: 3.3V at 19.77V Input

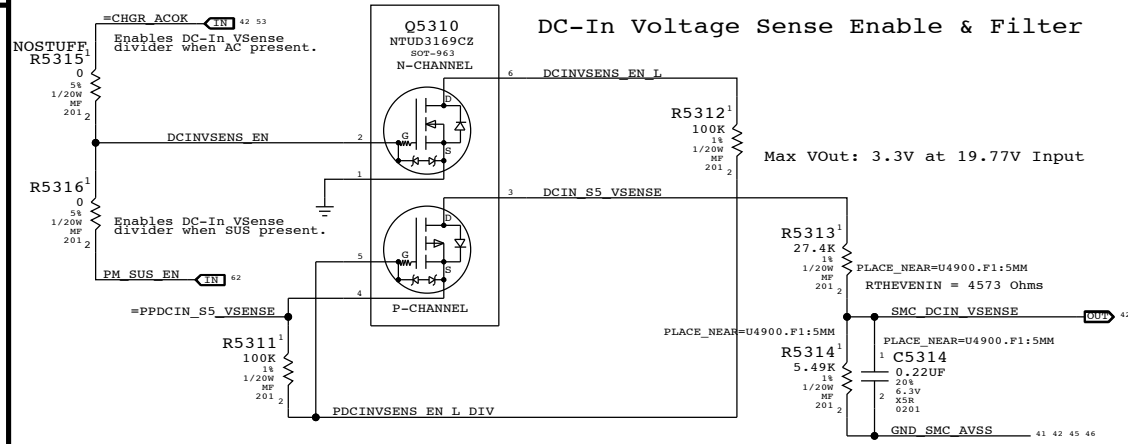
CPU VCore Load Side Current Sense / Filter



Sense R is R7510
Sense R is 0.75mOhm
EDP: 33A TDP :28.05A

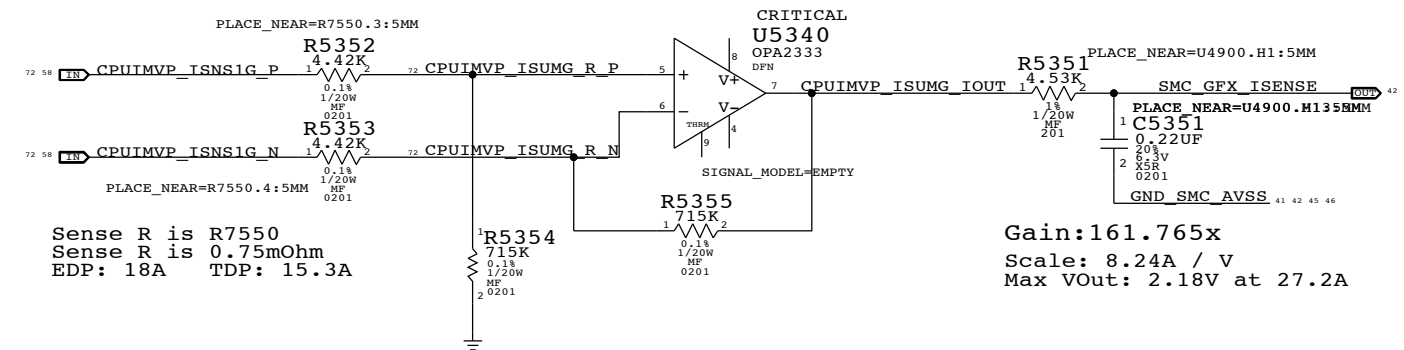
Gain:110.181x
Scale: 12.1A / V
Max VOut: 2.73V at 39.934A

DC-In Voltage Sense Enable & Filter



Max VOut: 3.3V at 19.77V Input

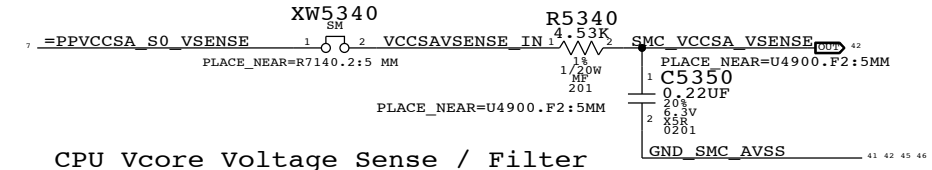
GFX/IG VCore Load Side Current Sense / Filter



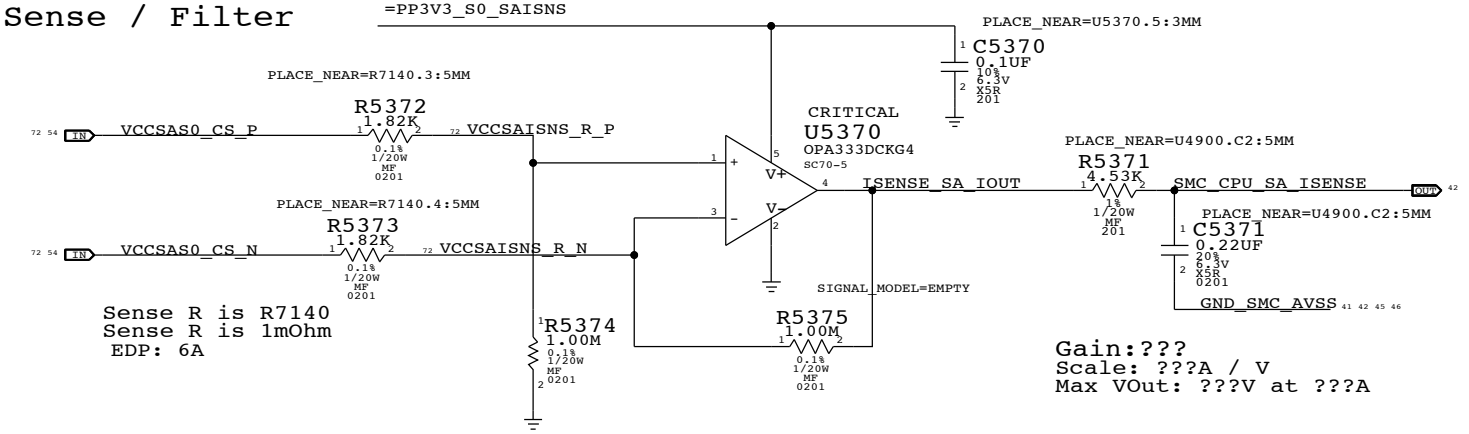
Sense R is R7550
Sense R is 0.75mOhm
EDP: 18A TDP: 15.3A

Gain:161.765x
Scale: 8.24A / V
Max VOut: 2.18V at 27.2A

VCCSA Voltage Sense / Filter



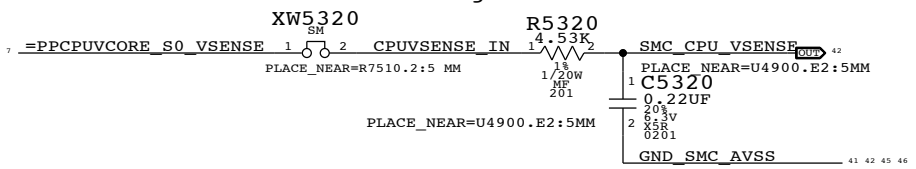
CPU SA Current Sense / Filter



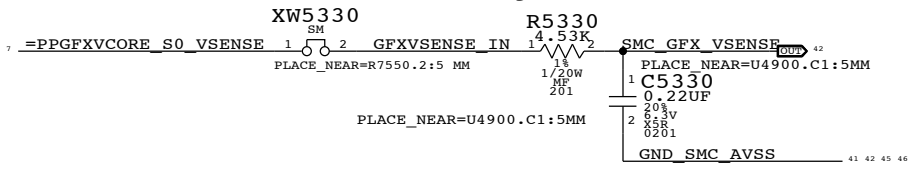
Sense R is R7140
Sense R is 1mOhm
EDP: 6A

Gain:???
Scale: ???A / V
Max VOut: ???V at ???A

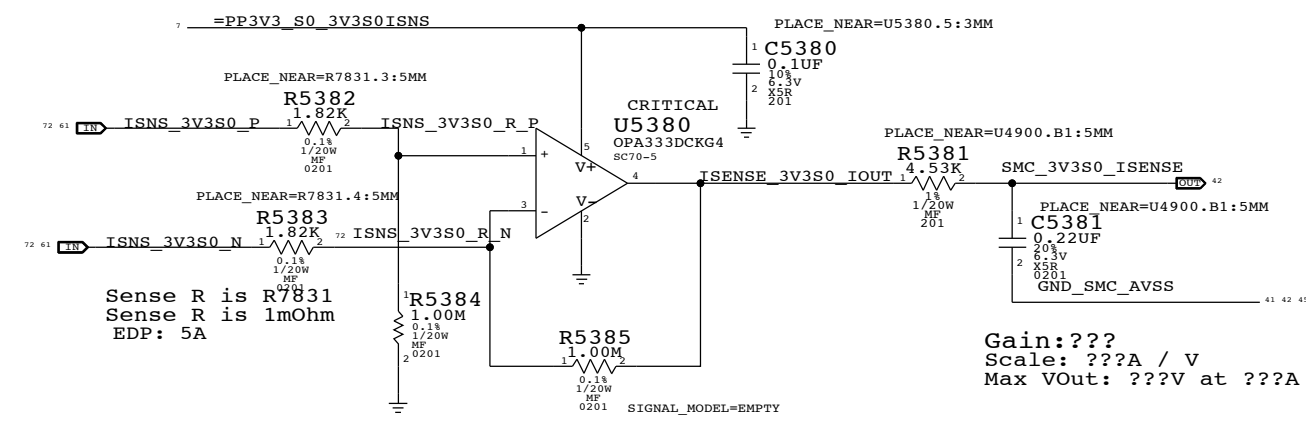
CPU Vcore Voltage Sense / Filter



GFX/IG Vcore Voltage Sense / Filter



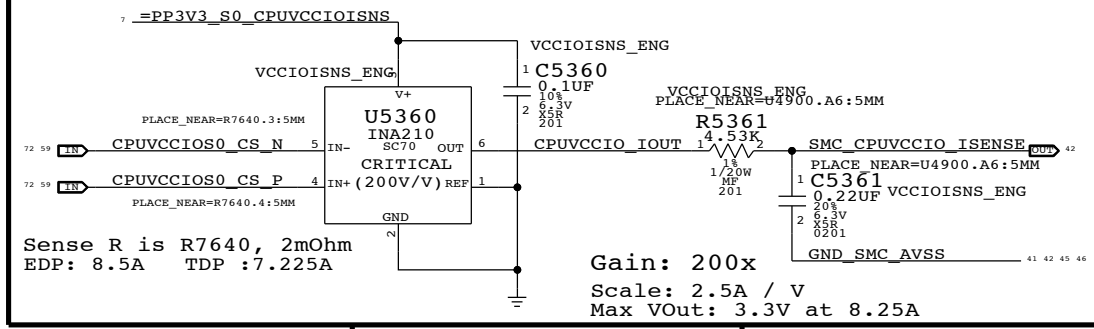
3.3V S0 FET Current Sense / Filter



Sense R is R7831
Sense R is 1mOhm
EDP: 5A

Gain:???
Scale: ???A / V
Max VOut: ???V at ???A

CPU 1.05V VCCIO Current Sense / Filter



Sense R is R7640, 2mOhm
EDP: 8.5A TDP :7.225A

Gain: 200x
Scale: 2.5A / V
Max VOut: 3.3V at 8.25A

SYNC MASTER=J11 MLB		SYNC DATE=12/02/2011	
Voltage & Load Side Current Sensing			
Apple Inc.		DRAWING NUMBER	051-9277
		REVISION	2.8.0
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C

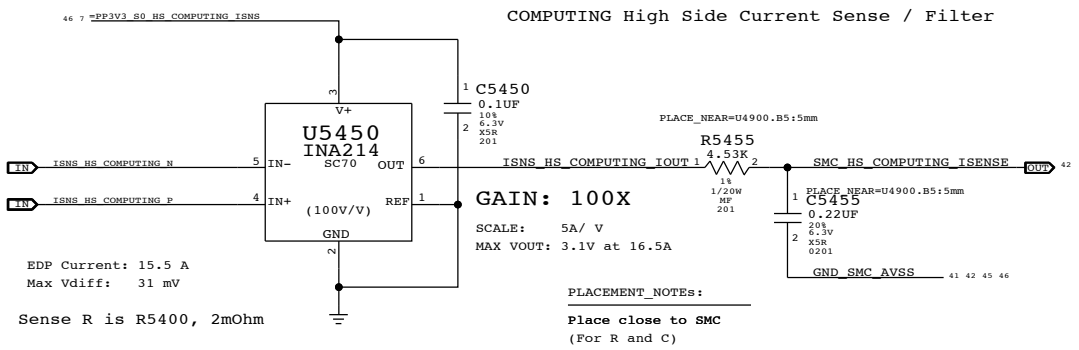
B

B

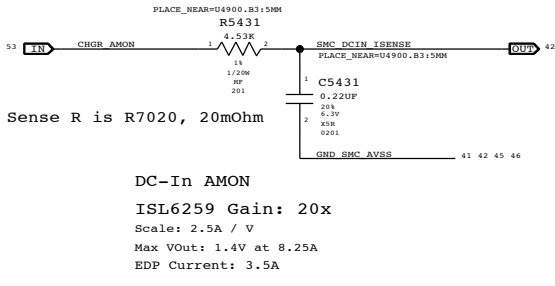
A

A

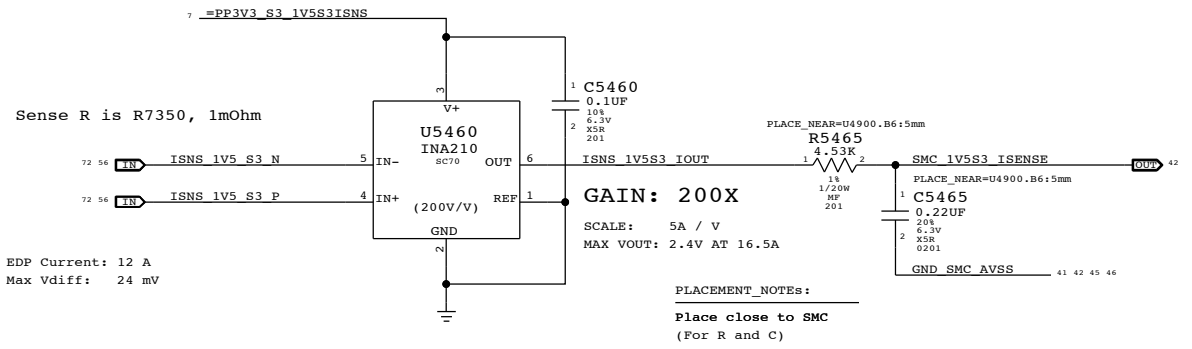
COMPUTING High Side Current Sense / Filter



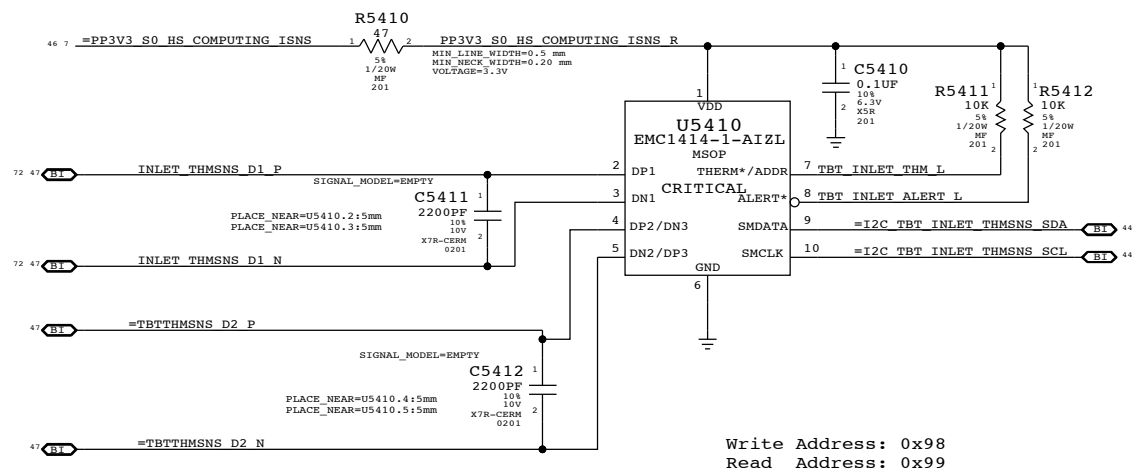
DC-IN (AMON) Current Sense Filter



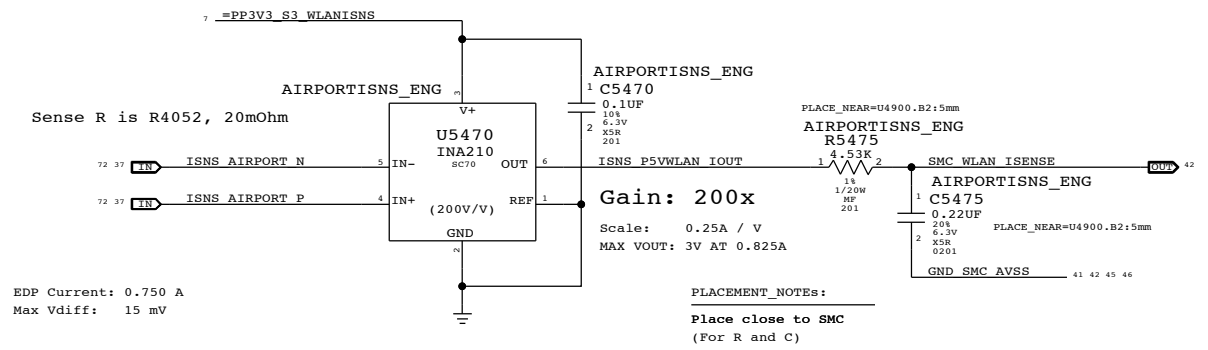
DDR3 1V5R1V35 Current Sense / Filter



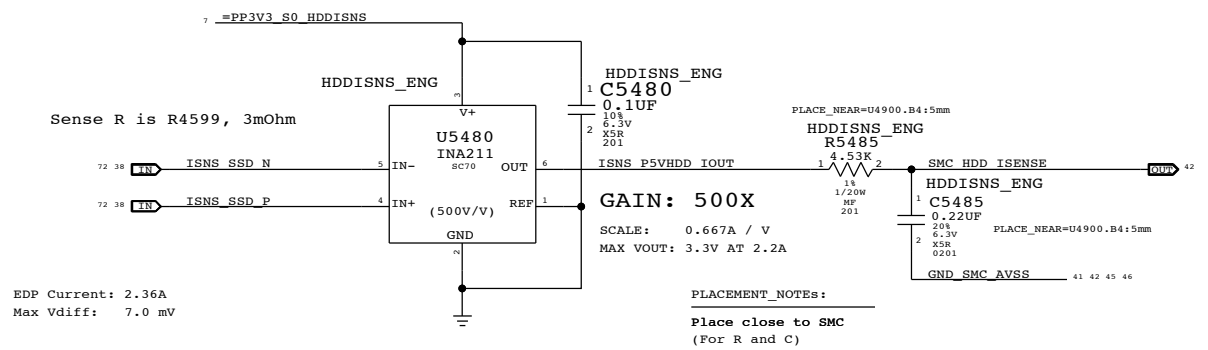
TBT/Inlet Temp Sensor



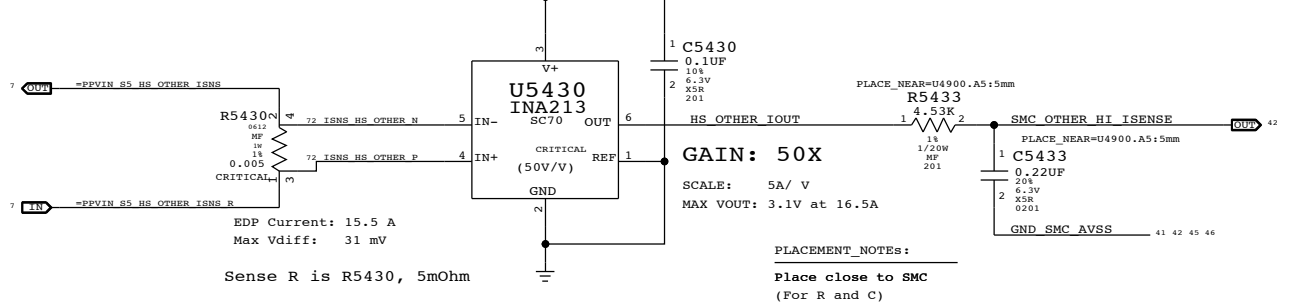
AirPort Current Sense / Filter



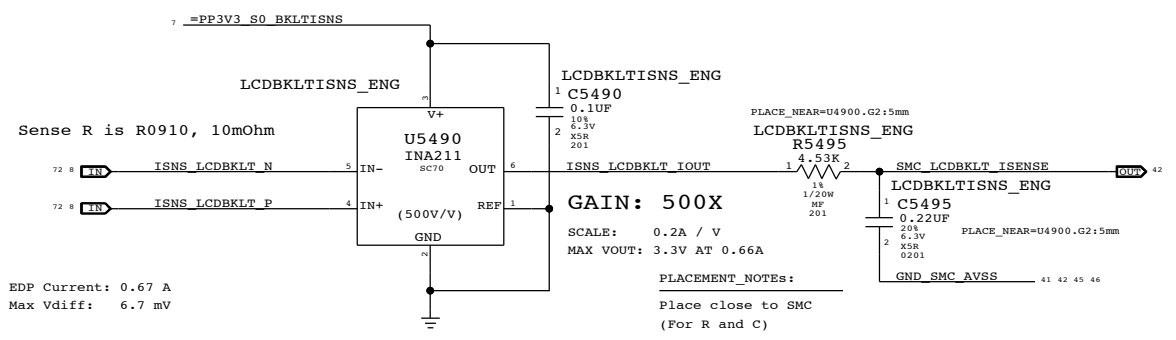
HDD Current Sense / Filter



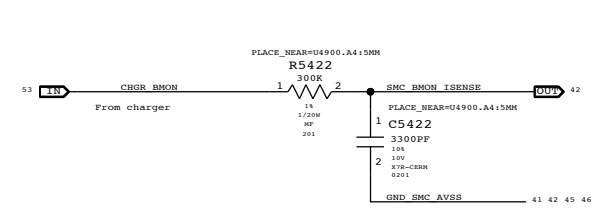
OTHER High Side Current Sense / Filter



LCD Backlight Driver Input Current Sense / Filter



CHARGER BMON High Side (BATTERY DISCHARGE) Current Sense, MUX & Filter



Charger BMON (Production) Solution

ISL6259 Gain: 36x

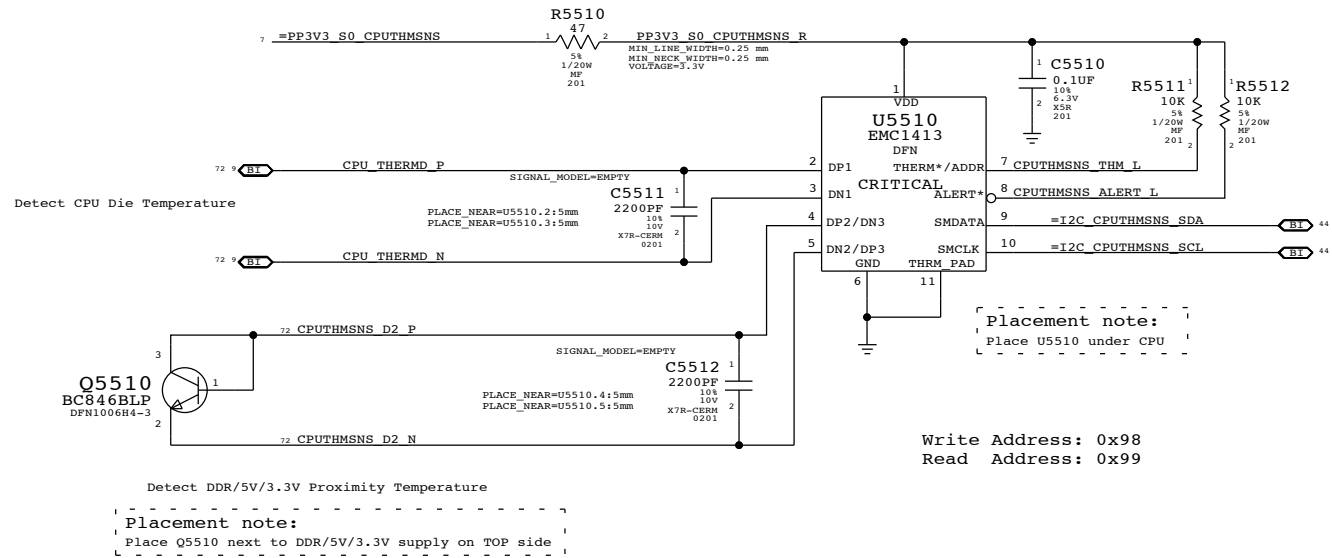
Scale: 2.78A / V

Max Vout: 3.3V at 9.167A

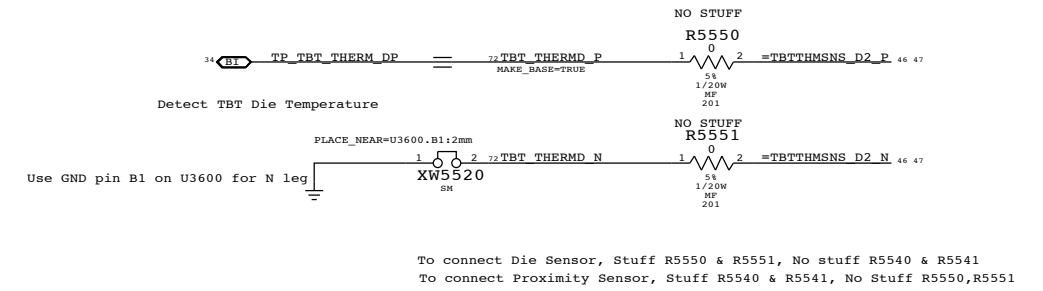
EDP Current: 310A

High Side Current Sensing		DRAWING NUMBER	SIZE
Apple Inc.		051-9277	D
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CPU Proximity Sensor



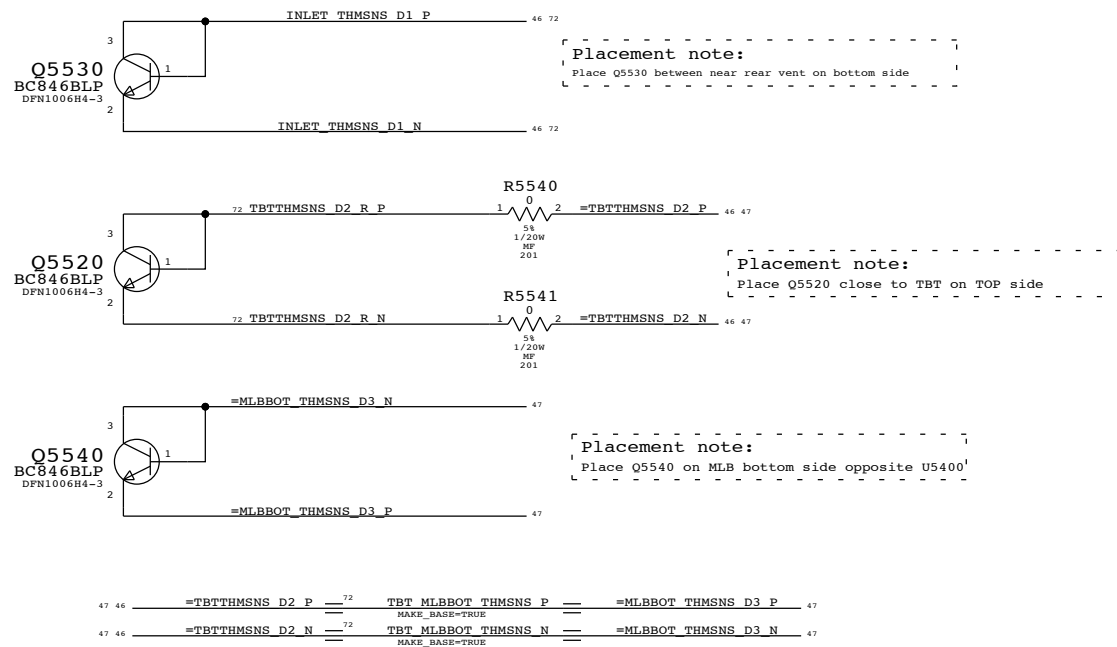
TBT Die



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES, MF, 1/20W, 100K OHM, 5, 0201, SMD	C5361		VCCIOISNS_PROD
117S0008	1	RES, MF, 1/20W, 100K OHM, 5, 0201, SMD	C5475		AIRPORTISNS_PROD
117S0008	1	RES, MF, 1/20W, 100K OHM, 5, 0201, SMD	C5485		HDDISNS_PROD
117S0008	1	RES, MF, 1/20W, 100K OHM, 5, 0201, SMD	C5495		LDCBKLTISNS_PROD

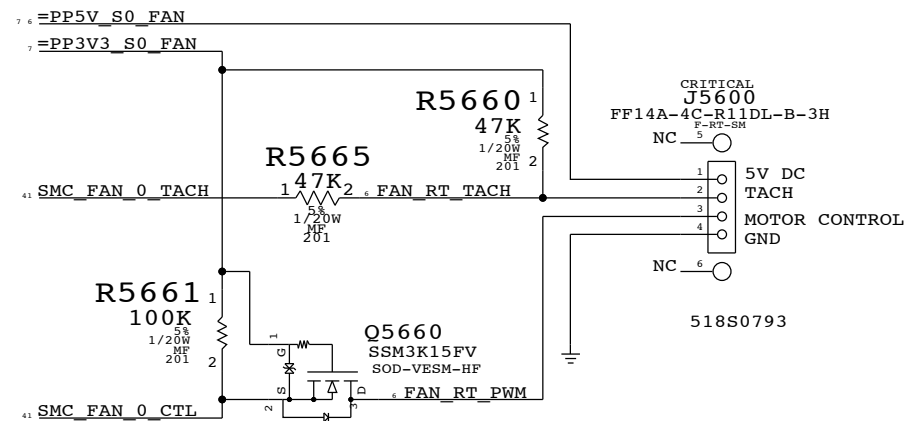
Replacing caps with 100K PD on ISENSE SMC inputs

TBT, MLB Bottom & Inlet Proximity Sensors



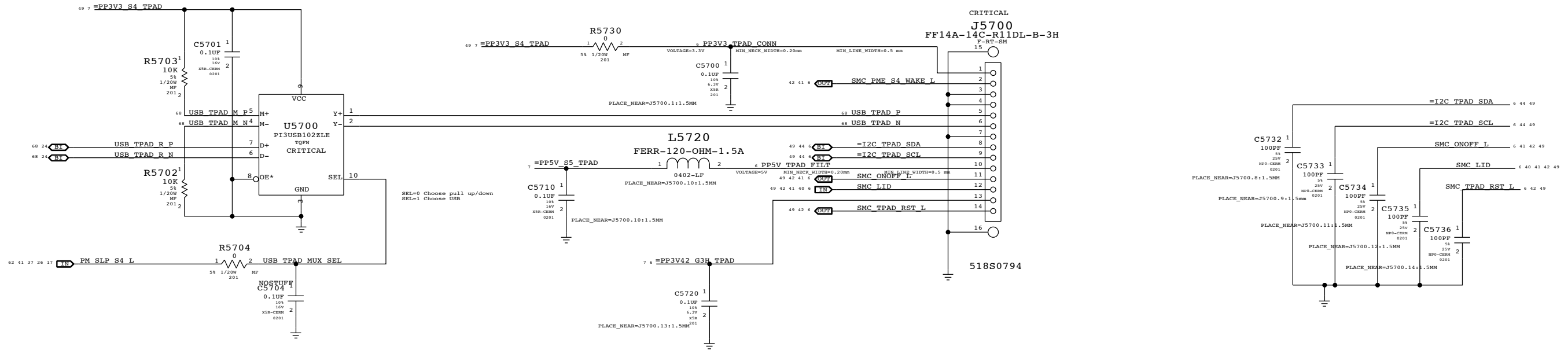
SYNC MASTER=J11 MLB		SYNC DATE=08/03/2011	
PAGE TITLE Thermal Sensors			
DRAWING NUMBER 051-9277		SIZE D	
REVISION 2.8.0		BRANCH	
PAGE 55 OF 109		SHEET 47 OF 73	
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FAN CONNECTOR

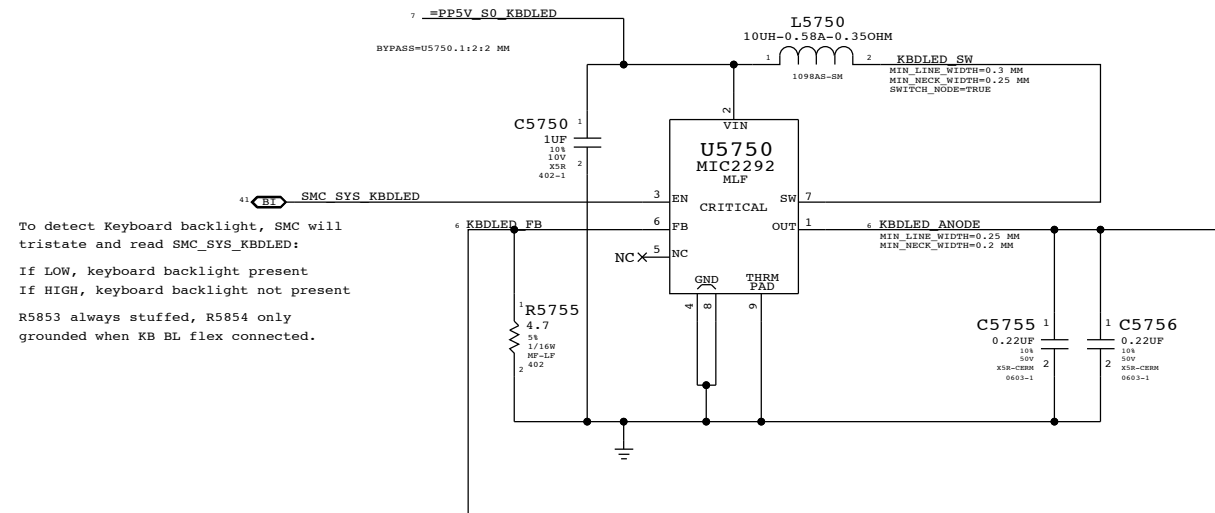


SYNC MASTER=K21 MLB		SYNC DATE=07/28/2011	
PAGE TITLE			
Fan			
Apple Inc.		DRAWING NUMBER	051-9277
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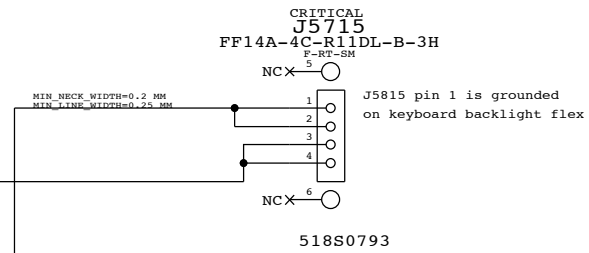
IPD Flex Connector



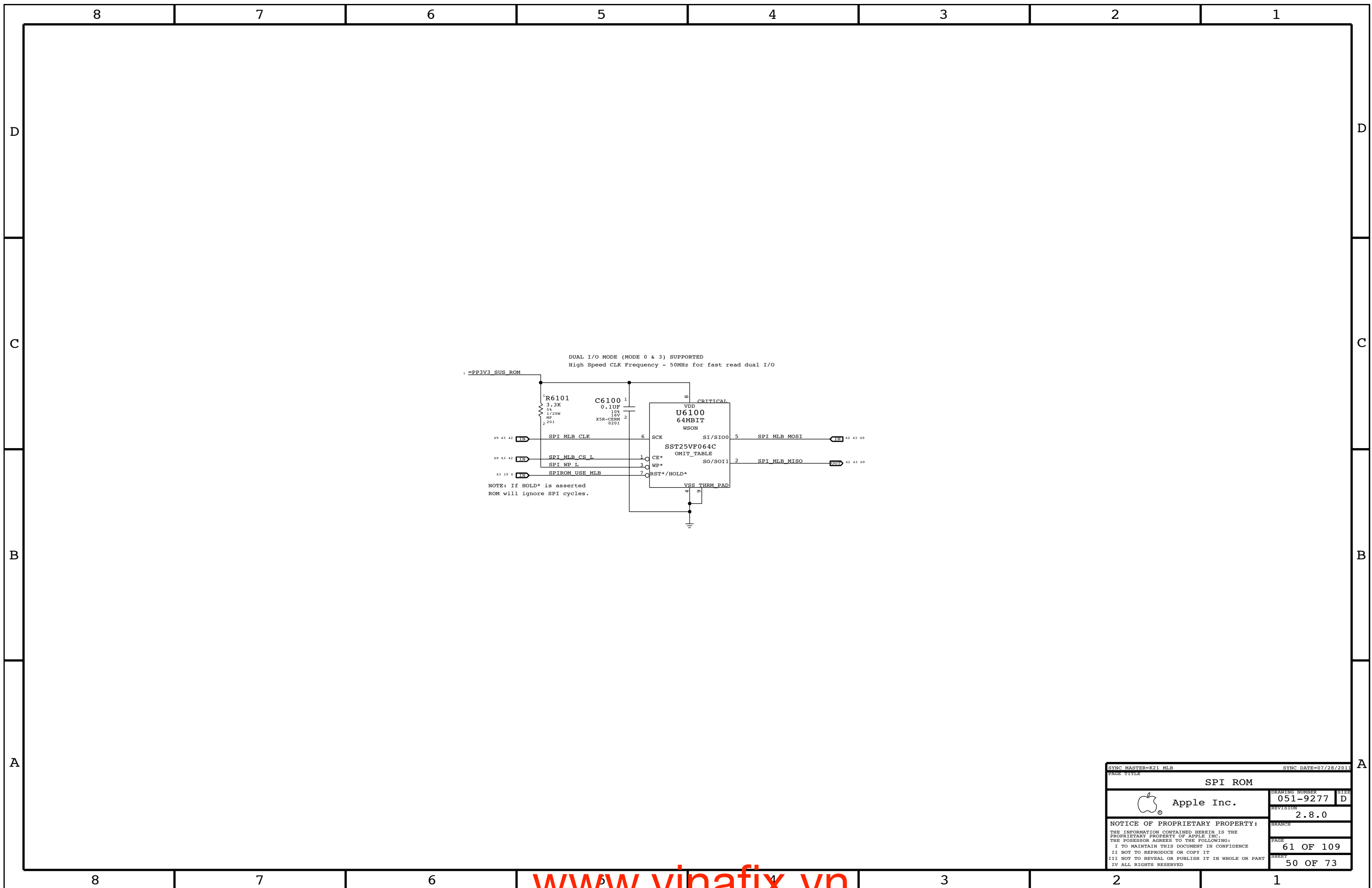
Keyboard Backlight Driver & Detection



Keyboard Backlight Connector



SYNC MASTER=J13 MLB NON POR		SYNC DATE=11/10/2011	
PAGE TITLE			
IPD / KBD Backlight			
Apple Inc.		DRAWING NUMBER	051-9277
		REVISION	2.8.0
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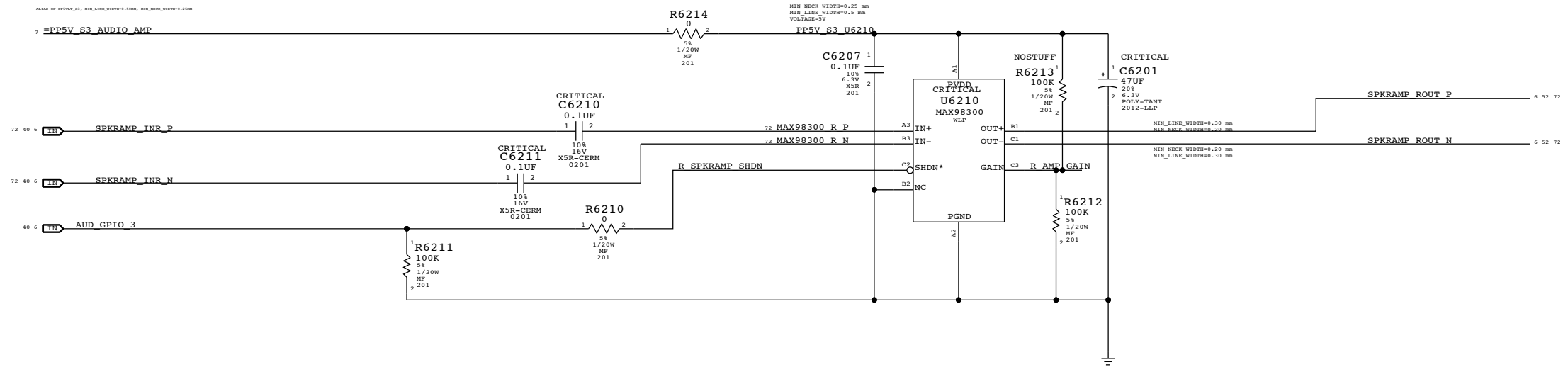


SYNC MASTER=K21_MLB		SYNC DATE=07/28/2011	
PAGE TITLE			
SPI ROM			
		DRAWING NUMBER	051-9277
		REVISION	2.8.0
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		SIZE	D

SPEAKER AMPLIFIERS

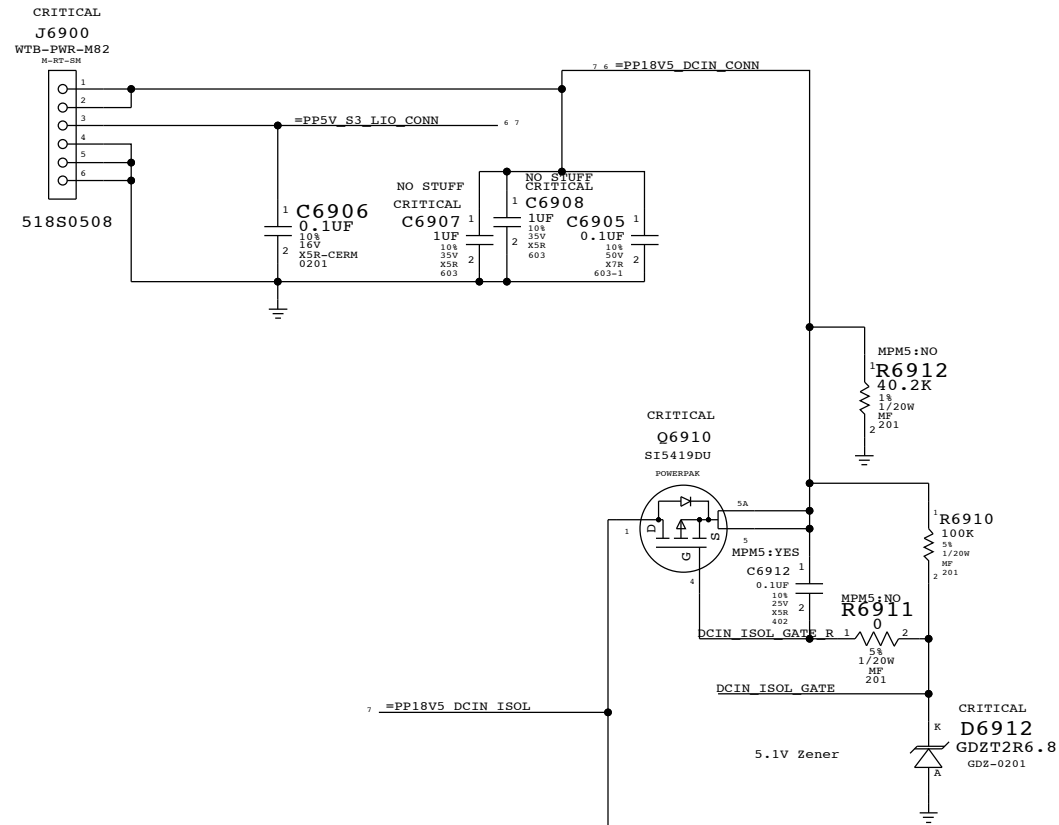
APN:353S2888

SPEAKER LOWPASS 80 HZ < FC < 132 HZ
GAIN 6DB

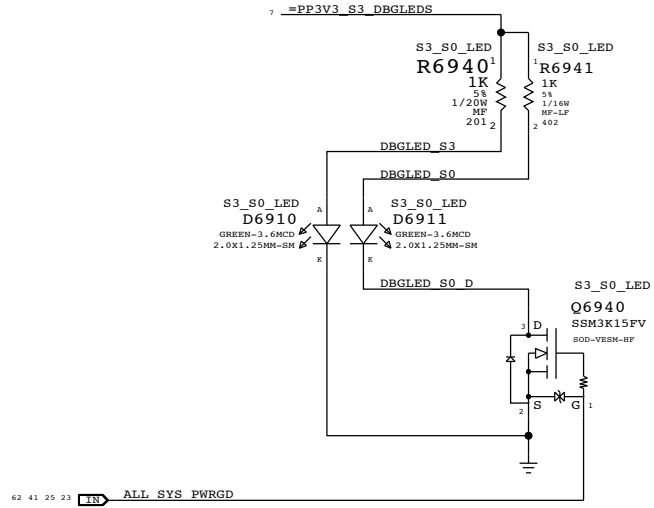


SYNC MASTER=J11 MLB		SYNC DATE=09/30/2011	
PAGE TITLE			
AUDIO: SPEAKER AMP			
DRAWING NUMBER		SIZE	
051-9277		D	
REVISION		PAGE	
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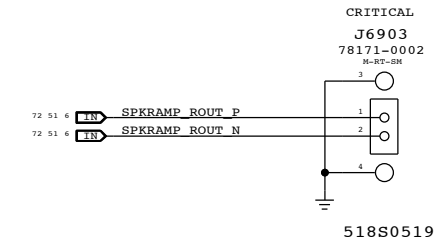
MLB to LIO Power Cable Connector



Debug LEDs
(For development only)



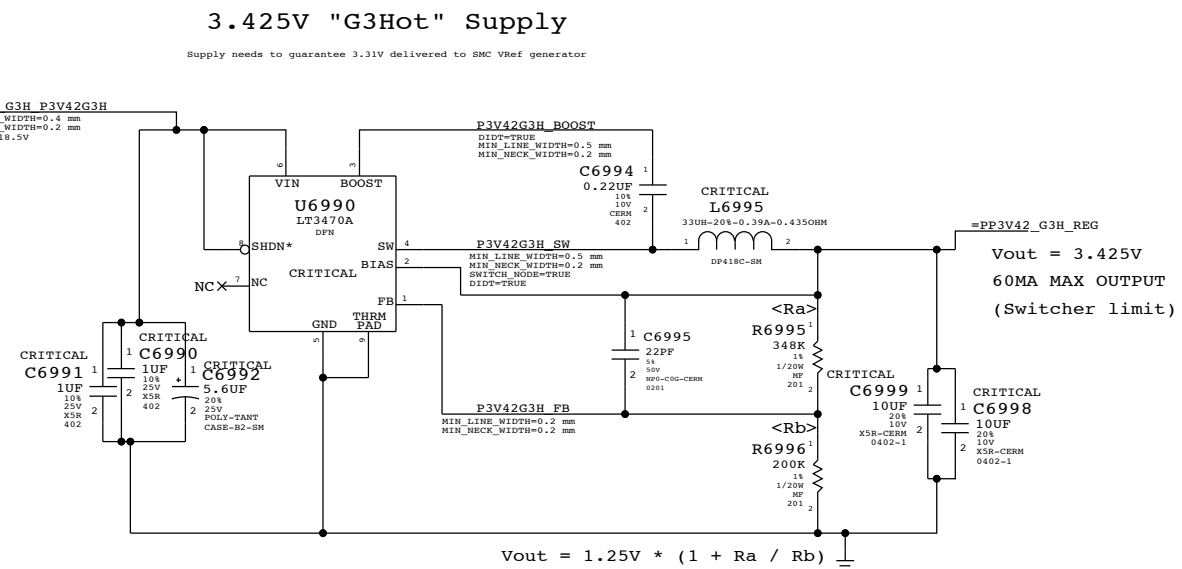
Right Speaker Connector



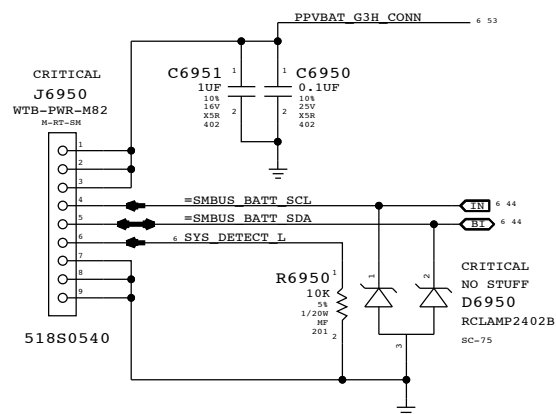
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11880560	1	RES, RP, 1/20W, 50, SECURM, 1,0201, SMD	R6912		MPM5: YES
11780008	1	RES, RP, 1/20W, 100KOHM, 1,0201, SMD	R6911		MPM5: YES

3.425V "G3Hot" Supply

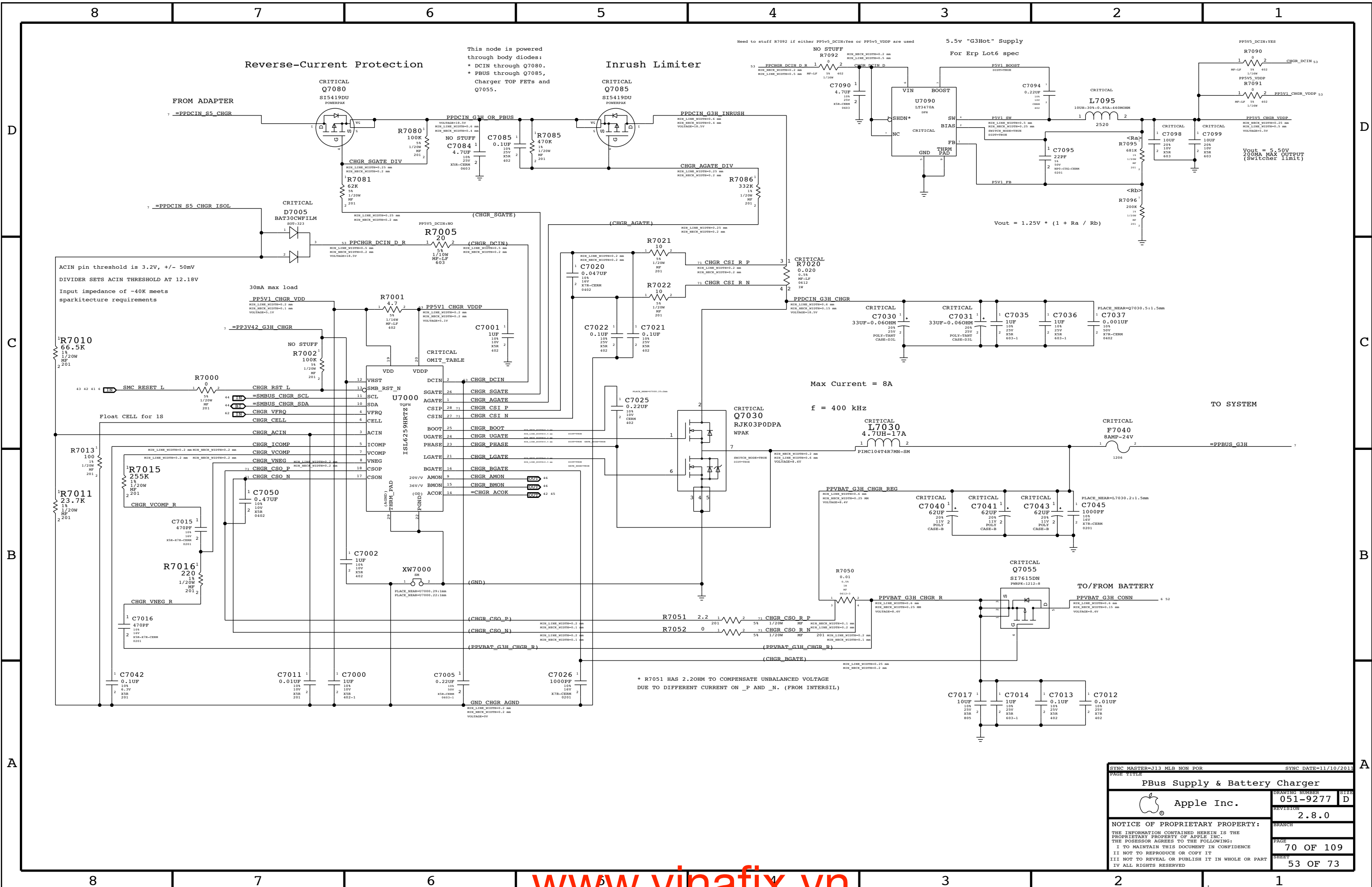
Supply needs to guarantee 3.31V delivered to SMC Vref generator



K16-Specific
Battery Connector



DC-In & Battery Connectors		DRAWING NUMBER	051-9277	SIZE	D
Apple Inc.		REVISION	2.8.0		
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This node is powered through body diodes:
 * DCIN through Q7080.
 * FBUS through Q7085,
 * CHARGER TOP FETs and Q7055.

Inrush Limiter

5.5v "G3Hot" Supply

PP5V5 DCIN: YES

Reverse-Current Protection

PP5V5_DCIN: NO
 (CHGR_DCIN)

(CHGR_AGATE)

Max Current = 8A

f = 400 kHz

30mA max load

ACIN pin threshold is 3.2V, +/- 50mV
 DIVIDER SETS ACIN THRESHOLD AT 12.18V
 Input impedance of ~40k meets
 sparkitecture requirements

PP5V1_CHGR_VDDP

PP3V42_G3H_CHGR

PP5V1_CHGR_VDD

PP5V1_CHGR_VDDP

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

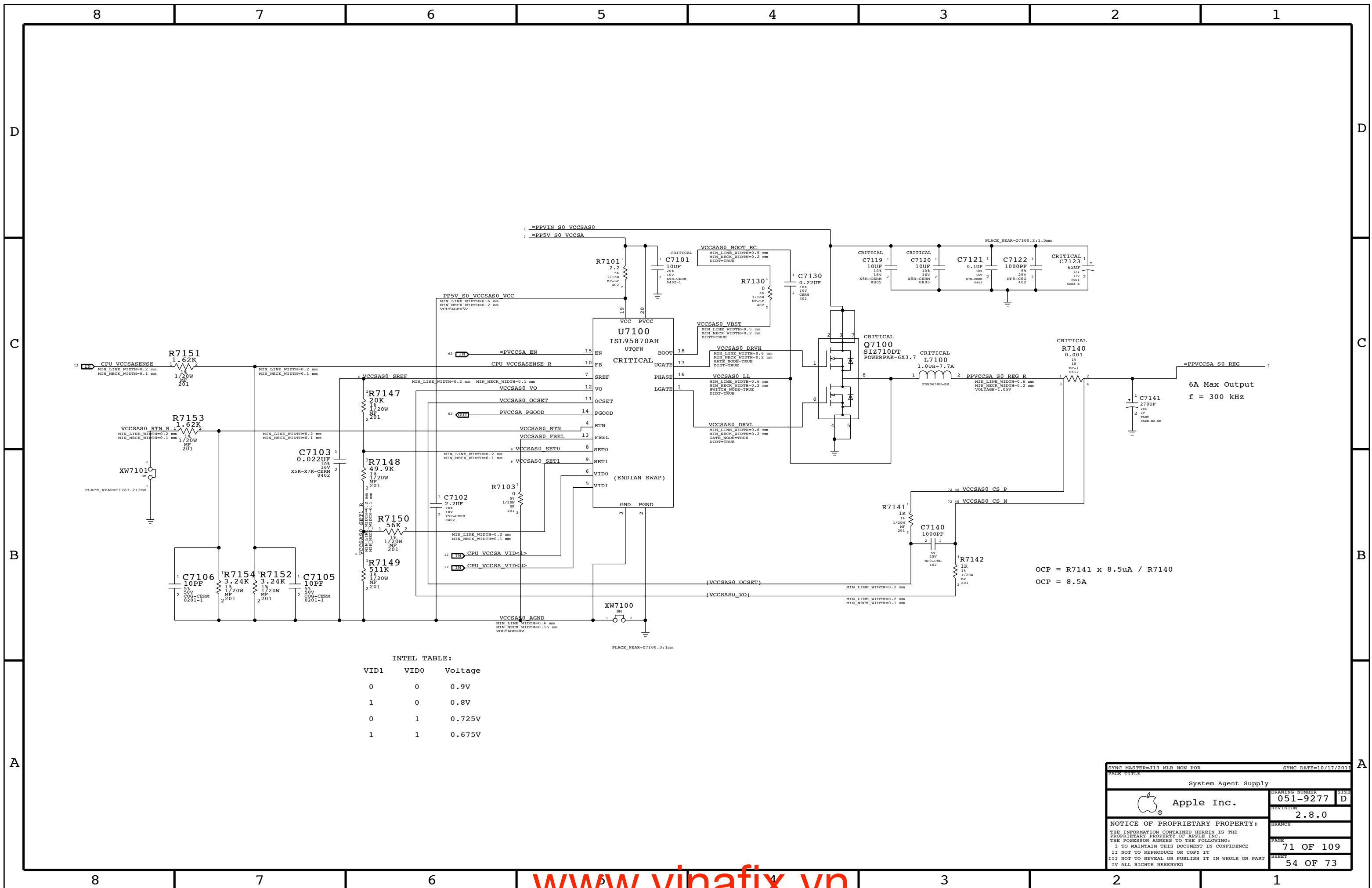
PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

PP5V1_CHGR_VDD

SYNC MASTER=113 MLB NON POR		SYNC DATE=11/10/2011	
PAGE TITLE			
PBus Supply & Battery Charger			
Apple Inc.		DRAWING NUMBER	051-9277
		REVISION	2.8.0
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BRANCH		PAGE	70 OF 109
SHEET		53 OF 73	



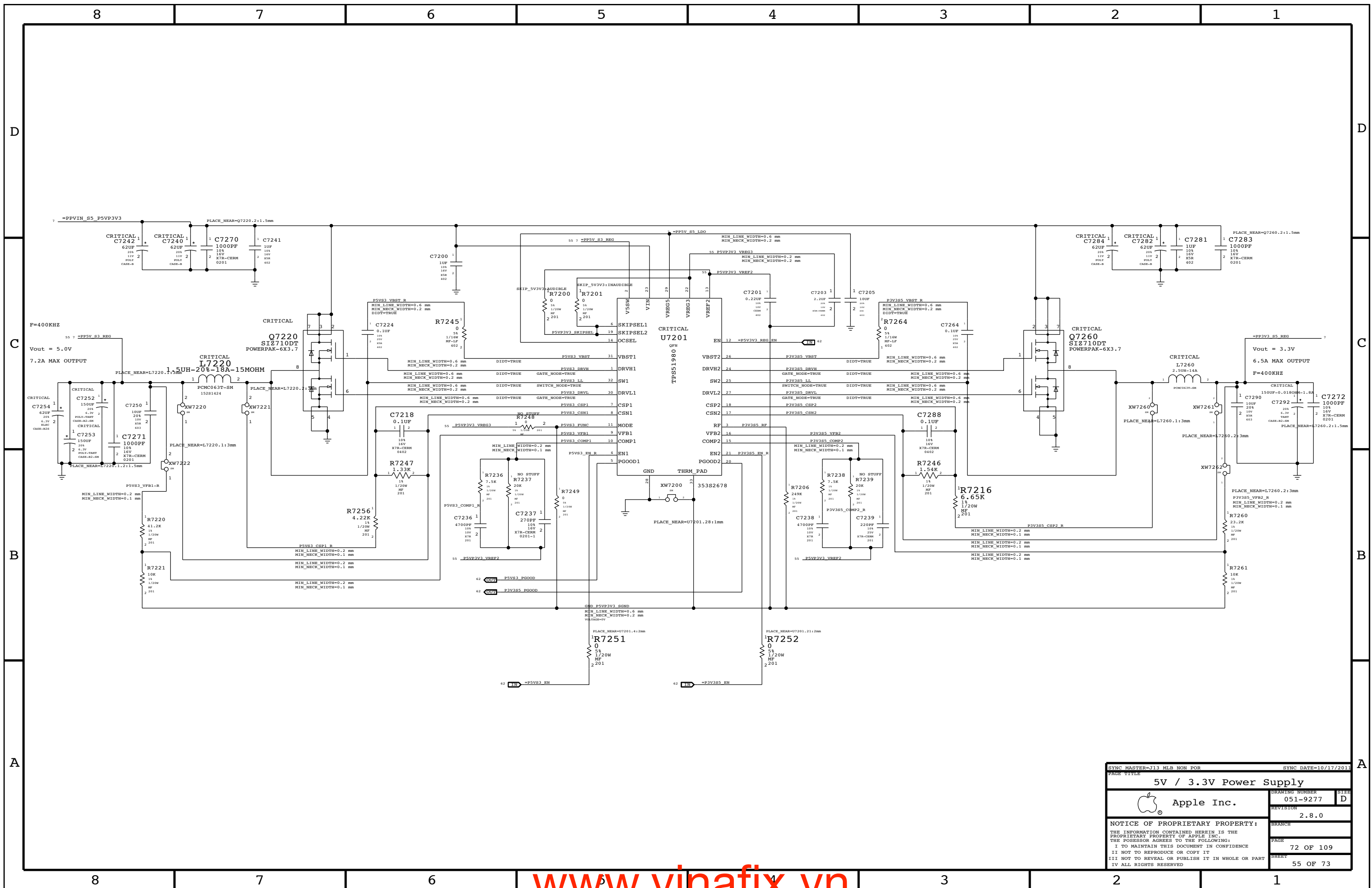
INTEL TABLE:

VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V
0	1	0.725V
1	1	0.675V

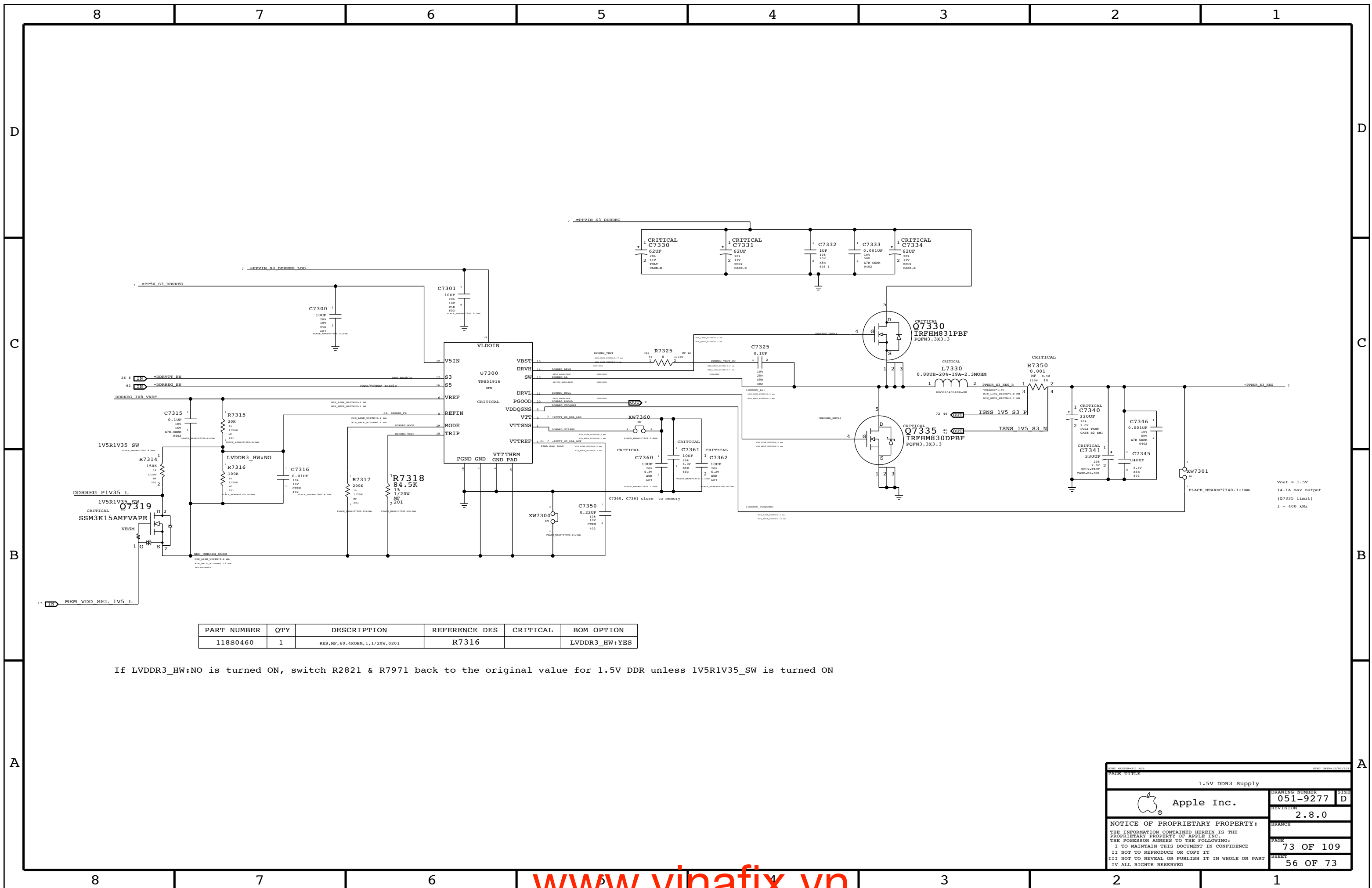
OCP = $R7141 \times 8.5\mu A / R7140$
OCP = 8.5A

6A Max Output
 $f = 300 \text{ kHz}$

SYNC MASTER=113 MLB NON POR		SYNC DATE=10/17/2011	
System Agent Supply			
Apple Inc.	DRAWING NUMBER	051-9277	SIZE D
	REVISION	2.8.0	
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SYNC MASTER=J13 MLB NON POR		SYNC DATE=10/17/2011	
PAGE TITLE			
5V / 3.3V Power Supply		DRAWING NUMBER	051-9277
Apple Inc.		REVISION	2.8.0
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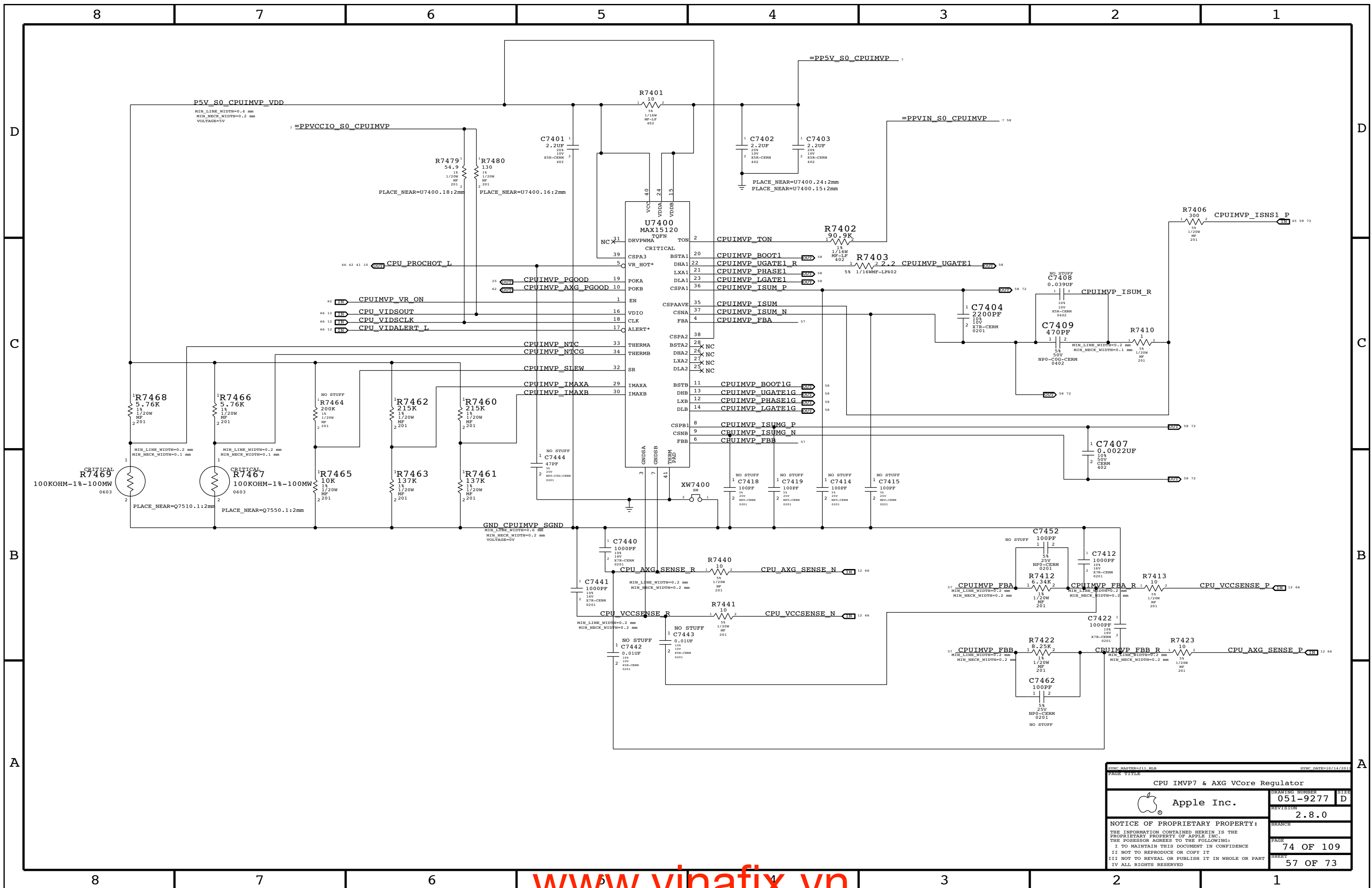
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0460	1	RES, MF, 60.4KOHM, 1, 1/20W, 0201	R7316		LVDDR3_HW:YES

If LVDDR3_HW:NO is turned ON, switch R2821 & R7971 back to the original value for 1.5V DDR unless 1V5R1V35_SW is turned ON

DRAWING NUMBER		051-9277	SIZE	D
REVISION		2.8.0	BRANCH	
PAGE		73 OF 109	SHEET	
SHEET		56 OF 73		

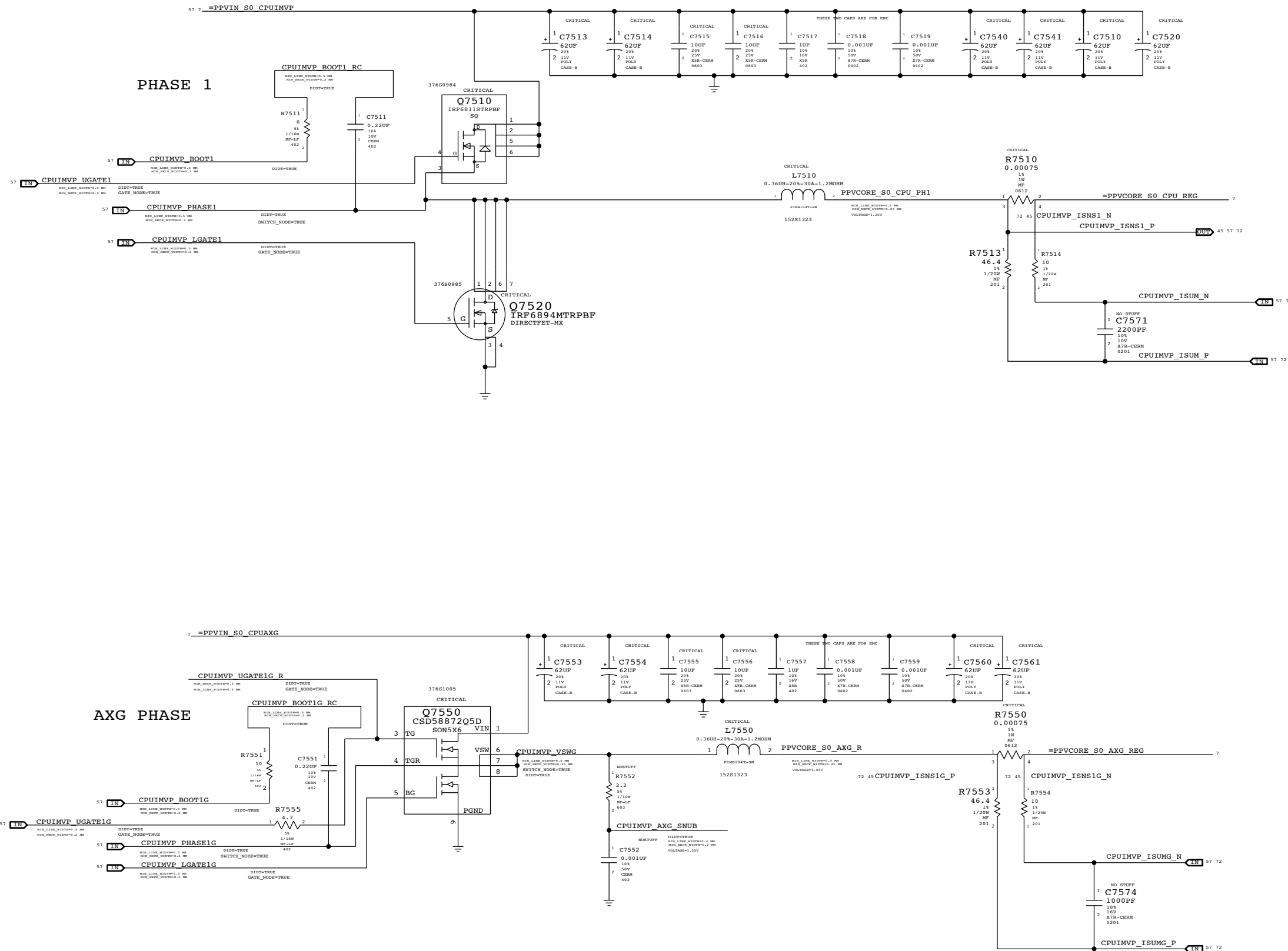
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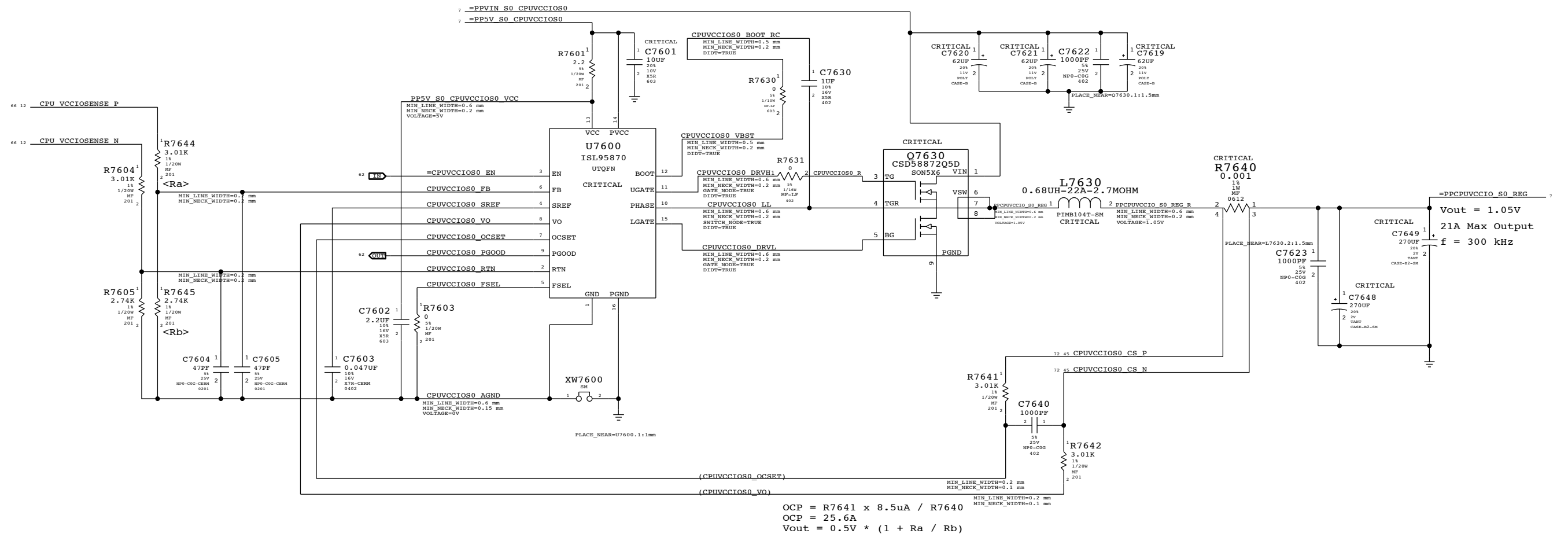
CPU IMVP7 & AXG VCore Regulator	
Apple Inc.	DRAWING NUMBER: 051-9277
REVISION: 2.8.0	SIZE: D
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CPU=IV Bridge ULV, AXG=GT2



PAGE TITLE		DRAWING NUMBER		SIZE
CPU IMVP7 & AXG VCore Output		051-9277		D
Apple Inc.		REVISION		
		2.8.0		
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CPU VCCIO (1.05V S0) Regulator



CPU VCCIO (1.05V) Power Supply	
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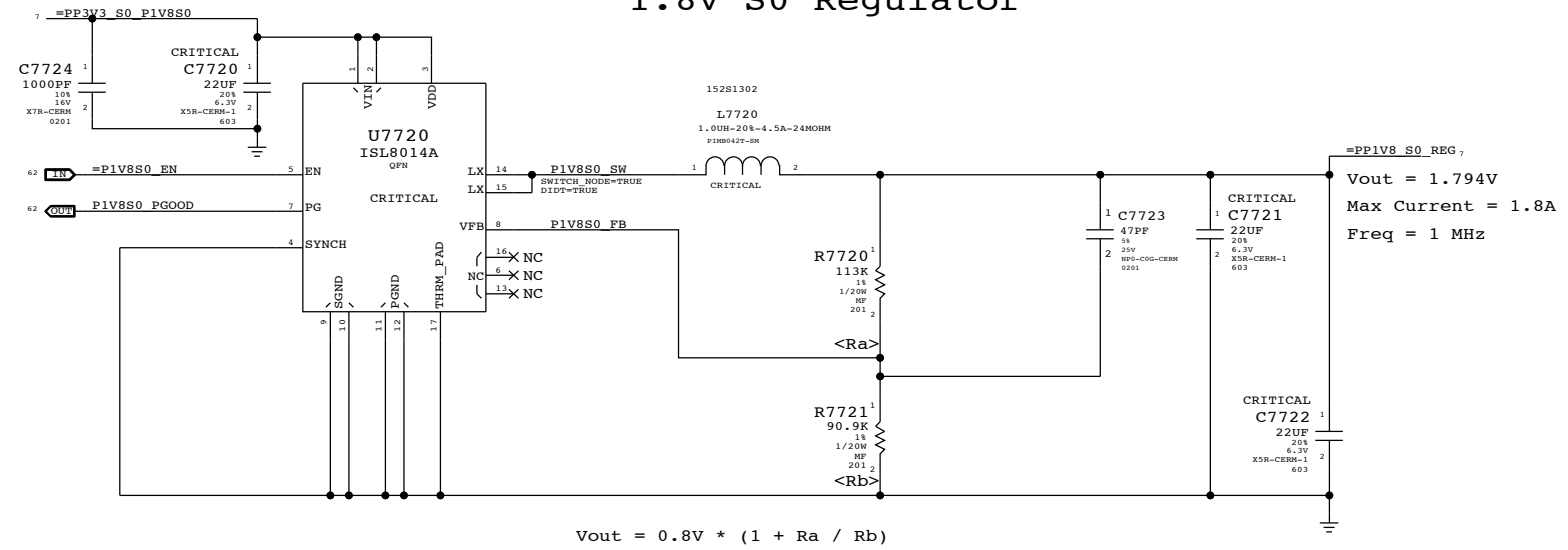
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B

A

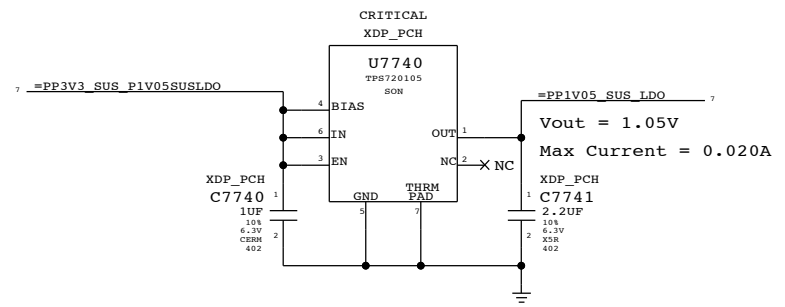
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1.8V S0 Regulator

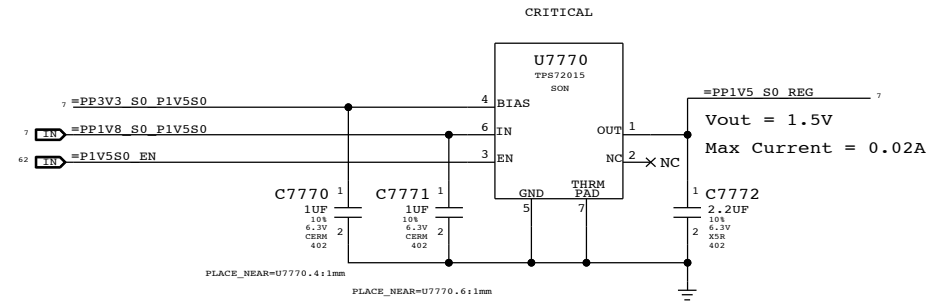


1.05V SUS LDO

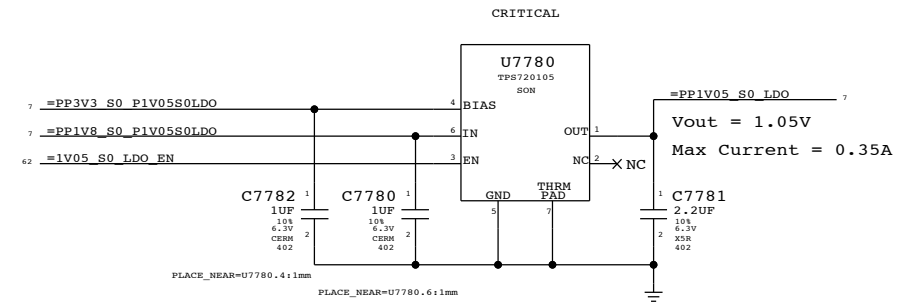
Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



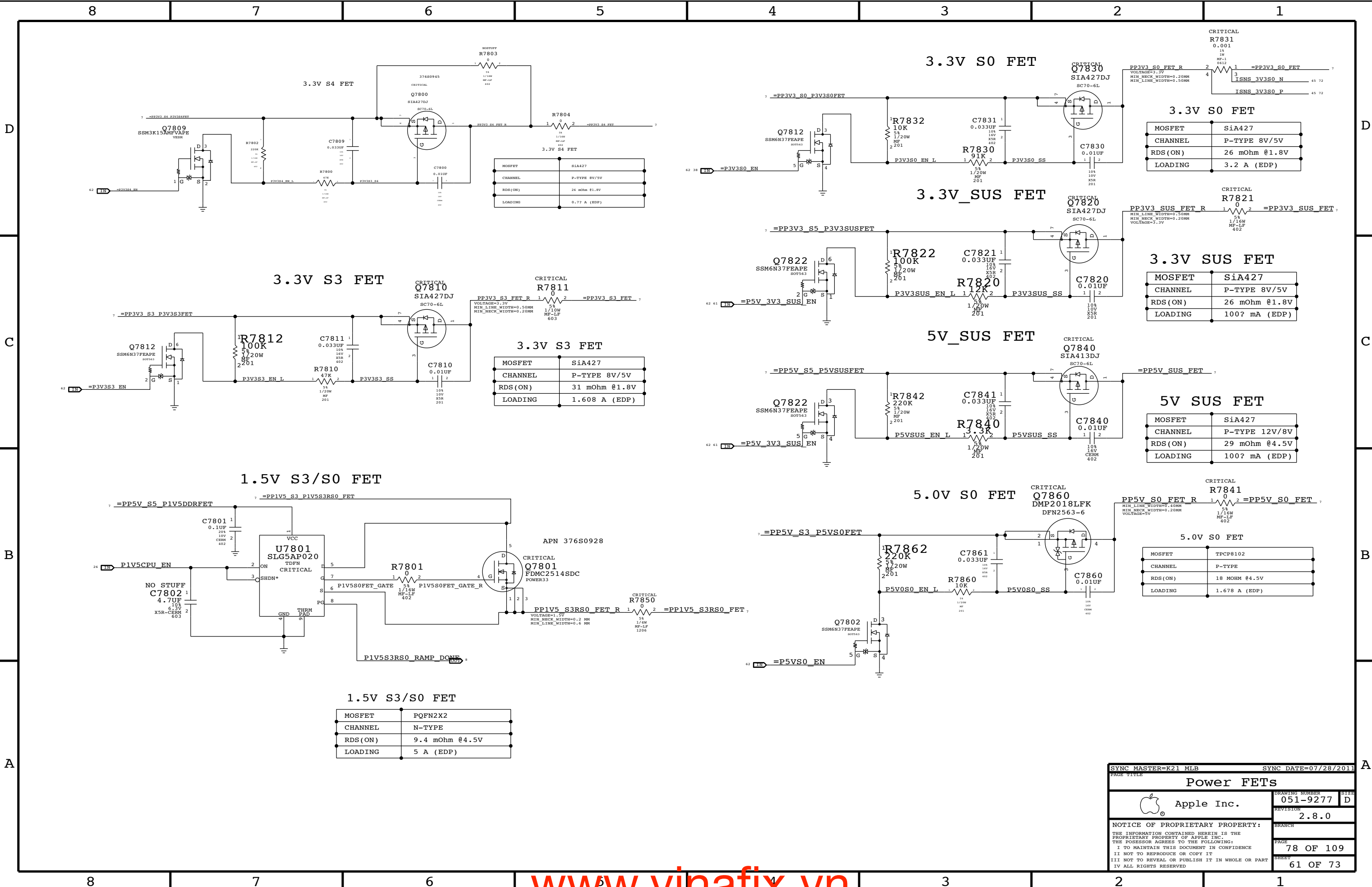
1.5V S0 LDO



1.05V S0 LDO



SYNC MASTER=K21.MLB		SYNC DATE=07/28/2011	
PAGE TITLE: Misc Power Supplies			
Apple Inc.	DRAWING NUMBER	051-9277	SIZE D
	REVISION	2.8.0	
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3.3V S4 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS (ON)	26 mOhm @1.8V
LOADING	0.77 A (EDP)

3.3V S0 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS (ON)	26 mOhm @1.8V
LOADING	3.2 A (EDP)

3.3V S3 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS (ON)	31 mOhm @1.8V
LOADING	1.608 A (EDP)

3.3V SUS FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS (ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)

5V SUS FET

MOSFET	SiA427
CHANNEL	P-TYPE 12V/8V
RDS (ON)	29 mOhm @4.5V
LOADING	100? mA (EDP)

1.5V S3/S0 FET

MOSFET	PQFN2X2
CHANNEL	N-TYPE
RDS (ON)	9.4 mOhm @4.5V
LOADING	5 A (EDP)

5.0V S0 FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS (ON)	18 MOHM @4.5V
LOADING	1.678 A (EDP)

PAGE TITLE		SYNC DATE=07/28/2011	
Power FETs			
Apple Inc.		DRAWING NUMBER	051-9277
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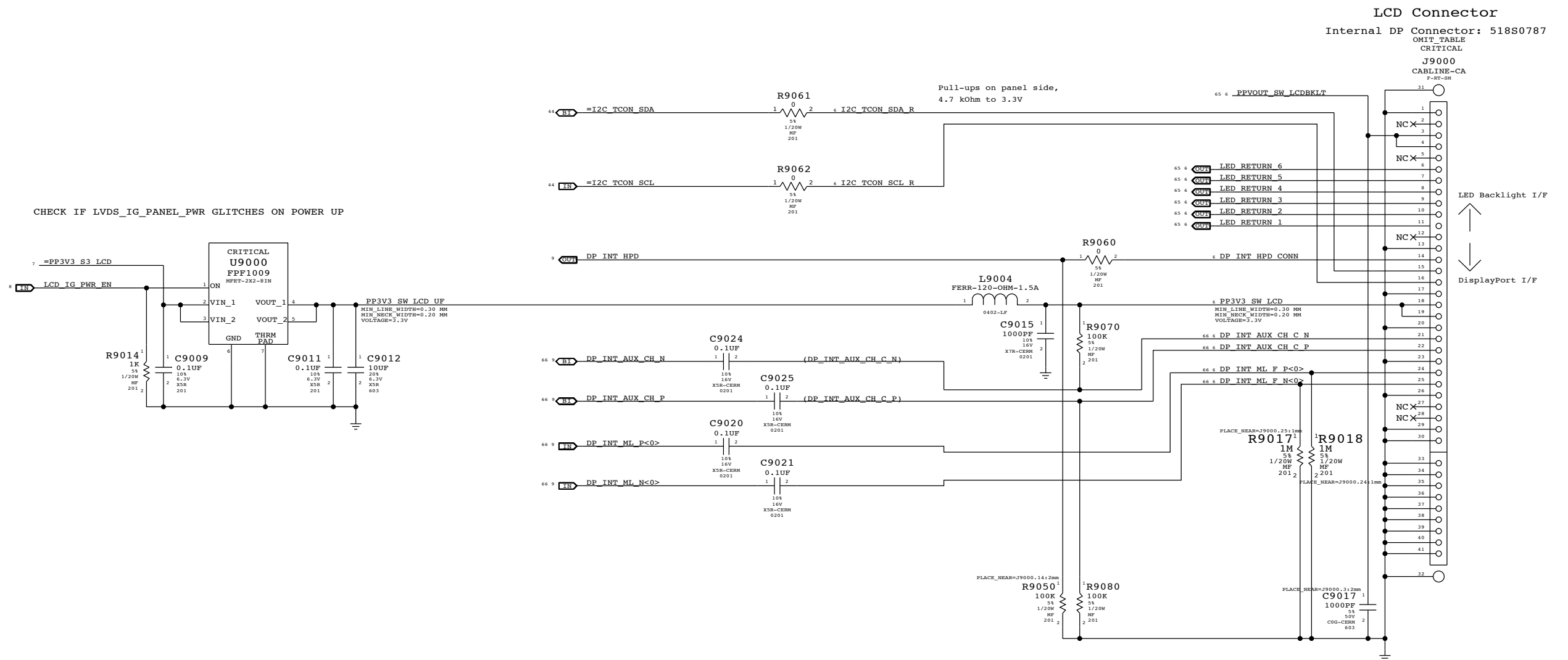
4

3

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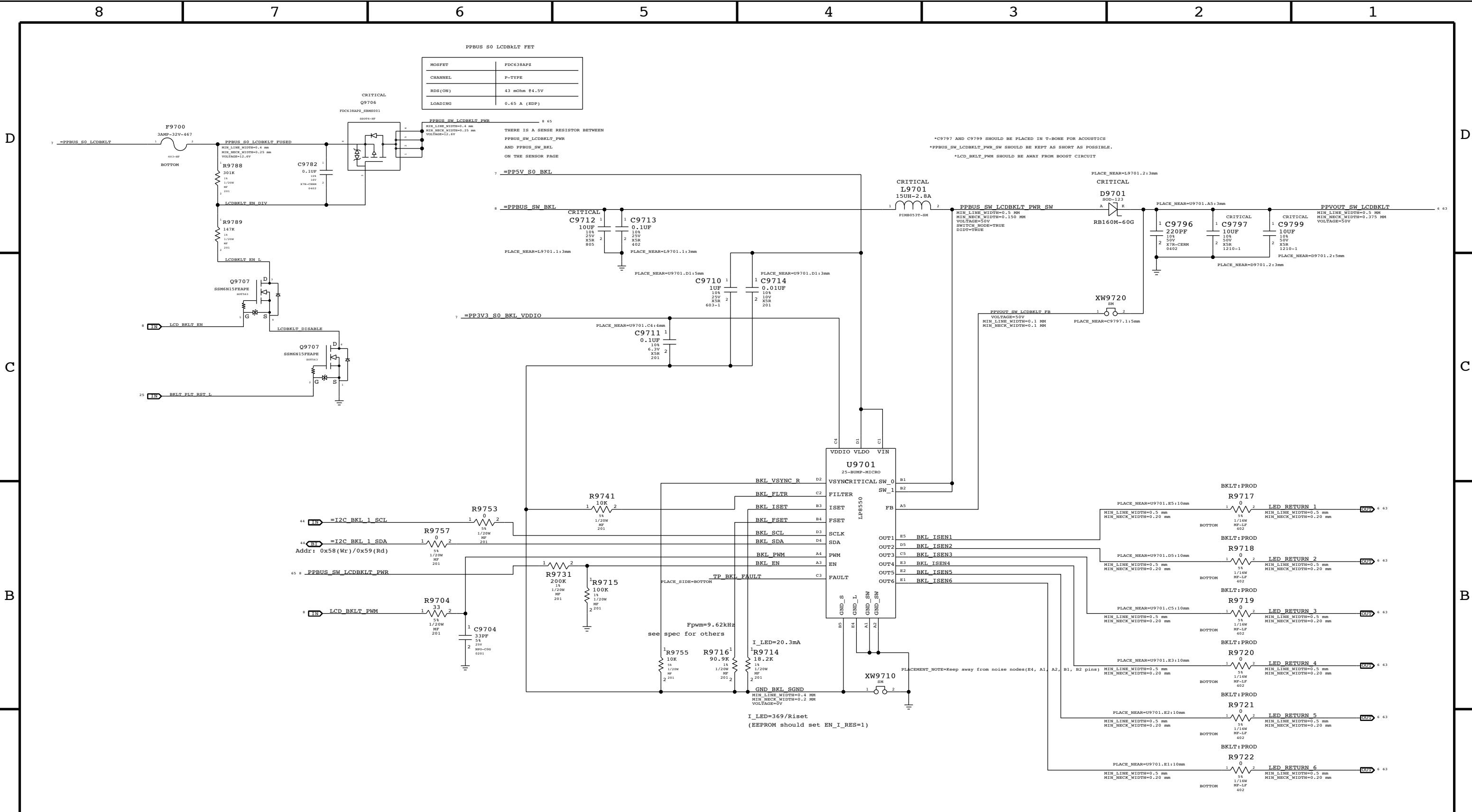
1

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
518S0829	1	CONNTRN=AX,P=0.4,30P,W=BOSS,HP	J9000		



SYNC MASTER=K21.MLB		SYNC DATE=07/28/2011	
Internal DisplayPort Connector			
Apple Inc.		DRAWING NUMBER	051-9277
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PPBUS SW LCDBKLT FET	
MOSFET	FDC638APE
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.65 A (EDP)



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES, THIN FILM, 1/16W, 10.2 OHM, 0.1, 0402, SM	R9717, R9718, R9719		BKLT:ENG
103S0198	3	RES, THIN FILM, 1/16W, 10.2 OHM, 0.1, 0402, SM	R9720, R9721, R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC MASTER=K21 MLB SYNC DATE=07/28/2011

LCD Backlight Driver

Apple Inc.

DRAWING NUMBER: 051-9277 SIZE: D

REVISION: 2.8.0

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.100 MM	0.100 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_AGTL	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_8MIL	*	*	CPU_8MIL_2ANY

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_ITP	*	*	CPU_ITP_2ANY

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	CPU_COMP	*	CPU_COMP_2SELF
CPU_COMP	*	*	CPU_COMP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_COMP_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	CPU_VCCSENSE	*	CPU_VCCSENSE_2SELF
CPU_VCCSENSE	*	*	CPU_VCCSENSE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?

PCI-Express Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
CLK_PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

PCIe Clock Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	CLK_PCIE	*	CLK_PCIE_2SELF
CLK_PCIE	*	*	CLK_PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CLK_PCIE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

CPU PCIe Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_CPU_TX	PCIE_CPU_TX	*	PCIE_TX2TX
PCIE_CPU_RX	PCIE_CPU_RX	*	PCIE_RX2RX
PCIE_CPU_TX	*_CPU_TX	*	PCIE_TX2OTHERTX
PCIE_CPU_RX	*_CPU_RX	*	PCIE_RX2OTHERRX
PCIE_CPU_TX	*_CPU_RX	*	PCIE_TX2RX
PCIE_CPU_RX	*_CPU_TX	*	PCIE_RX2TX
PCIE_CPU_TX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*	*	PCIE_2OTHER
PCIE_CPU_RX	*	*	PCIE_2OTHER

PCH PCIe Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_PCH_TX	PCIE_PCH_TX	*	PCIE_TX2TX
PCIE_PCH_RX	PCIE_PCH_RX	*	PCIE_RX2RX
PCIE_PCH_TX	*_PCH_TX	*	PCIE_TX2OTHERTX
PCIE_PCH_RX	*_PCH_RX	*	PCIE_RX2OTHERRX
PCIE_PCH_TX	*_PCH_RX	*	PCIE_TX2RX
PCIE_PCH_RX	*_PCH_TX	*	PCIE_RX2TX
PCIE_PCH_TX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*	*	PCIE_2OTHER
PCIE_PCH_RX	*	*	PCIE_2OTHER

Note: DisplayPort tables are on Page 103

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
DMI_S2N	PCIE_80D	PCIE_PCH_TX	DMI_S2N_P<3:0>
DMI_S2N	PCIE_80D	PCIE_PCH_TX	DMI_S2N_N<3:0>
DMI_N2S	PCIE_80D	PCIE_PCH_RX	DMI_N2S_P<3:0>
DMI_N2S	PCIE_80D	PCIE_PCH_RX	DMI_N2S_N<3:0>
FDI_DATA	PCIE_80D	PCIE_PCH_RX	FDI_DATA_P<7:0>
FDI_DATA	PCIE_80D	PCIE_PCH_RX	FDI_DATA_N<7:0>
CPU_45S	CPU_AGTL	CPU_AGTL	FDI_FSYNC<1..0>
CPU_45S	CPU_AGTL	CPU_AGTL	FDI_LSYNC<1..0>
CPU_45S	CPU_AGTL	CPU_AGTL	FDI_INT
CPU_PECT	CPU_45S	CPU_COMP	CPU_PECT
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD
CPU_45S	CPU_ITP	CPU_ITP	XDP_DBRESET_L
CPU_45S	CPU_ITP	CPU_ITP	XDP_CPU_PRDY_L
CPU_45S	CPU_ITP	CPU_ITP	XDP_CPU_PREQ_L
CPU_27P4S	CPU_COMP	CPU_COMP	EDP_COMP
CPU_27P4S	CPU_COMP	CPU_COMP	CPU_PEG_COMP
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0>
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1>
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2>
CPU_45S	CPU_ITP	CPU_ITP	CPU_CFG<11..0>
CPU_CATER_L	CPU_45S	CPU_AGTL	CPU_CATER_L
CPU_45S	CPU_AGTL	CPU_AGTL	CPU_VCCIO_SEL
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD
PM_THRMTRIP_L	CPU_45S	CPU_SMIT	PM_THRMTRIP_L
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_P
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_N
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKP
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKN
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_P
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_N
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_P
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_N
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_P
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_N
XDP_TDI	CPU_45S	CPU_ITP	XDP_CPU_TDI
XDP_TDO	CPU_45S	CPU_ITP	XDP_CPU_TDO
XDP_TMS	CPU_45S	CPU_ITP	XDP_CPU_TMS
XDP_TCK	CPU_45S	CPU_ITP	XDP_CPU_TCK
XDP_TRST_L	CPU_45S	CPU_ITP	XDP_CPU_TRST_L
XDP_BPM_L	CPU_45S	CPU_ITP	XDP_BPM_L<3..0>
(XDP_BPM_L_R_CFG)	CPU_45S	CPU_ITP	XDP_BPM_L<7..4>
(XDP_BPM_L_R_CFG)	CPU_45S	CPU_ITP	XDP_OBSDATA_B<3..0>
(FSB_CPURST_L)	CPU_45S	CPU_ITP	CPU_CFG<15..12>
CPU_VCCSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_P
CPU_VCCSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_N
CPU_VCCIOSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_P
CPU_VCCIOSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_N
CPU_AXG_SENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_P
CPU_AXG_SENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_N
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDO_SENSE_P
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDO_SENSE_N
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N
CPU_SVIDALERT_L	CPU_45S	CPU_COMP	CPU_VIDALERT_L
CPU_SVIDSCLK	CPU_45S	CPU_COMP	CPU_VIDSCLK
CPU_SVIDSOUT	CPU_45S	CPU_COMP	CPU_VIDSOUT
PCIE_CPU_MUX_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_P<0>
PCIE_CPU_MUX_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_N<0>
PCIE_CPU_MUX_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_R2D_MUX_IN_P
PCIE_CPU_MUX_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_R2D_MUX_IN_N
PCIE_CPU_MUX_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<0>
PCIE_CPU_MUX_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<0>
PCIE_CPU_MUX_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_MUX_OUT_P
PCIE_CPU_MUX_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_MUX_OUT_N
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_R2D_C_P<1>
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_R2D_C_N<1>
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_P<1>
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_N<1>
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<1>
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<1>
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_P<1>
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_N<1>
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_P
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_N
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_P<3..0>
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_N<3..0>
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_F_P<3..0>
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_F_N<3..0>
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_P
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_N
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_P
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_N

DMI/FDI

PCIe SSD

DP

SYNC MASTER=113 CONSTRAINTS SYNC DATE=01/11/2012

CPU Constraints

Apple Inc.

DRAWING NUMBER: 051-9277

REVISION: 2.8.0

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=3x_DIELECTRIC	?
MEM_CMD2CMD	*	=3x_DIELECTRIC	?
MEM_CMD2CTRL	*	=3x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=3x_DIELECTRIC	?
MEM_CLK2CLK	*	=6x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=PWR_P2MM	?
MEM_2GND	*	=GND_P2MM	?
MEM_2OTHER	*	=6x_DIELECTRIC	?

PalPilot Spacing

=2x_DIELECTRIC
=5.7x_DIELECTRIC
=3x_DIELECTRIC
=4x_DIELECTRIC
=4x_DIELECTRIC
=8.6x_DIELECTRIC
=5.7x_DIELECTRIC
=PWR_P2MM
=GND_P2MM
=8.6x_DIELECTRIC

"Real" Spacing

=2x_DIELECTRIC
=3x_DIELECTRIC
=3x_DIELECTRIC
=3x_DIELECTRIC
=3x_DIELECTRIC
=6x_DIELECTRIC
=4x_DIELECTRIC
=PWR_P2MM
=GND_P2MM
=6x_DIELECTRIC

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	*	*	MEM_2OTHER
MEM_A_DQS_1	*	*	MEM_2OTHER
MEM_A_DQS_2	*	*	MEM_2OTHER
MEM_A_DQS_3	*	*	MEM_2OTHER
MEM_A_DQS_4	*	*	MEM_2OTHER
MEM_A_DQS_5	*	*	MEM_2OTHER
MEM_A_DQS_6	*	*	MEM_2OTHER
MEM_A_DQS_7	*	*	MEM_2OTHER
MEM_B_DQS_0	*	*	MEM_2OTHER
MEM_B_DQS_1	*	*	MEM_2OTHER
MEM_B_DQS_2	*	*	MEM_2OTHER
MEM_B_DQS_3	*	*	MEM_2OTHER
MEM_B_DQS_4	*	*	MEM_2OTHER
MEM_B_DQS_5	*	*	MEM_2OTHER
MEM_B_DQS_6	*	*	MEM_2OTHER
MEM_B_DQS_7	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	MEM_*	*	MEM_2OTHERMEM

MEM_A_DATA_0	*	*	MEM_2OTHER
MEM_A_DATA_1	*	*	MEM_2OTHER
MEM_A_DATA_2	*	*	MEM_2OTHER
MEM_A_DATA_3	*	*	MEM_2OTHER
MEM_A_DATA_4	*	*	MEM_2OTHER
MEM_A_DATA_5	*	*	MEM_2OTHER
MEM_A_DATA_6	*	*	MEM_2OTHER
MEM_A_DATA_7	*	*	MEM_2OTHER
MEM_B_DATA_0	*	*	MEM_2OTHER
MEM_B_DATA_1	*	*	MEM_2OTHER
MEM_B_DATA_2	*	*	MEM_2OTHER
MEM_B_DATA_3	*	*	MEM_2OTHER
MEM_B_DATA_4	*	*	MEM_2OTHER
MEM_B_DATA_5	*	*	MEM_2OTHER
MEM_B_DATA_6	*	*	MEM_2OTHER
MEM_B_DATA_7	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PROPERTY	VALUE	MIN	MAX
	PHYSICAL	SPACING				
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK P<5..0>	5	11	27 28 32
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK N<5..0>	5	11	27 28 32
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM A CKE<3..0>	3	11	27 28 32
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM A CS L<3..0>	3	11	27 28 32
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM A ODT<3..0>	3	11	27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM A A<15..0>	15	11	27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM A BA<2..0>	2	11	27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM A RAS L	1	11	27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM A CAS L	1	11	27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM A WE L	1	11	27 28 32
MEM_A_DO_BYTE0	MEM_45S	MEM_A_DATA_0	MEM A DO<7..0>	7	11	27
MEM_A_DO_BYTE1	MEM_45S	MEM_A_DATA_1	MEM A DO<15..8>	15	11	27
MEM_A_DO_BYTE2	MEM_45S	MEM_A_DATA_2	MEM A DO<23..16>	23	11	27
MEM_A_DO_BYTE3	MEM_45S	MEM_A_DATA_3	MEM A DO<31..24>	31	11	27
MEM_A_DO_BYTE4	MEM_45S	MEM_A_DATA_4	MEM A DO<39..32>	39	11	28
MEM_A_DO_BYTE5	MEM_45S	MEM_A_DATA_5	MEM A DO<47..40>	47	11	28
MEM_A_DO_BYTE6	MEM_45S	MEM_A_DATA_6	MEM A DO<55..48>	55	11	28
MEM_A_DO_BYTE7	MEM_45S	MEM_A_DATA_7	MEM A DO<63..56>	63	11	28
MEM_A_DQS0	MEM_80D	MEM_A_DQS_0	MEM A DQS P<0>	0	11	27
MEM_A_DQS0	MEM_80D	MEM_A_DQS_0	MEM A DQS N<0>	0	11	27
MEM_A_DQS1	MEM_80D	MEM_A_DQS_1	MEM A DQS P<1>	1	11	27
MEM_A_DQS1	MEM_80D	MEM_A_DQS_1	MEM A DQS N<1>	1	11	27
MEM_A_DQS2	MEM_80D	MEM_A_DQS_2	MEM A DQS P<2>	2	11	27
MEM_A_DQS2	MEM_80D	MEM_A_DQS_2	MEM A DQS N<2>	2	11	27
MEM_A_DQS3	MEM_80D	MEM_A_DQS_3	MEM A DQS P<3>	3	11	27
MEM_A_DQS3	MEM_80D	MEM_A_DQS_3	MEM A DQS N<3>	3	11	27
MEM_A_DQS4	MEM_80D	MEM_A_DQS_4	MEM A DQS P<4>	4	11	28
MEM_A_DQS4	MEM_80D	MEM_A_DQS_4	MEM A DQS N<4>	4	11	28
MEM_A_DQS5	MEM_80D	MEM_A_DQS_5	MEM A DQS P<5>	5	11	28
MEM_A_DQS5	MEM_80D	MEM_A_DQS_5	MEM A DQS N<5>	5	11	28
MEM_A_DQS6	MEM_80D	MEM_A_DQS_6	MEM A DQS P<6>	6	11	28
MEM_A_DQS6	MEM_80D	MEM_A_DQS_6	MEM A DQS N<6>	6	11	28
MEM_A_DQS7	MEM_80D	MEM_A_DQS_7	MEM A DQS P<7>	7	11	28
MEM_A_DQS7	MEM_80D	MEM_A_DQS_7	MEM A DQS N<7>	7	11	28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK P<5..0>	5	11	29 30 32
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK N<5..0>	5	11	29 30 32
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM B CKE<3..0>	3	11	29 30 32
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM B CS L<3..0>	3	11	29 30 32
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM B ODT<3..0>	3	11	29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM B A<15..0>	15	11	29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM B BA<2..0>	2	11	29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM B RAS L	1	11	29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM B CAS L	1	11	29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM B WE L	1	11	29 30 32
MEM_B_DO_BYTE0	MEM_45S	MEM_B_DATA_0	MEM B DO<7..0>	7	11	29
MEM_B_DO_BYTE1	MEM_45S	MEM_B_DATA_1	MEM B DO<15..8>	15	11	29
MEM_B_DO_BYTE2	MEM_45S	MEM_B_DATA_2	MEM B DO<23..16>	23	11	29
MEM_B_DO_BYTE3	MEM_45S	MEM_B_DATA_3	MEM B DO<31..24>	31	11	29
MEM_B_DO_BYTE4	MEM_45S	MEM_B_DATA_4	MEM B DO<39..32>	39	11	30
MEM_B_DO_BYTE5	MEM_45S	MEM_B_DATA_5	MEM B DO<47..40>	47	11	30
MEM_B_DO_BYTE6	MEM_45S	MEM_B_DATA_6	MEM B DO<55..48>	55	11	30
MEM_B_DO_BYTE7	MEM_45S	MEM_B_DATA_7	MEM B DO<63..56>	63	11	30
MEM_B_DQS0	MEM_80D	MEM_B_DQS_0	MEM B DQS P<0>	0	11	29
MEM_B_DQS0	MEM_80D	MEM_B_DQS_0	MEM B DQS N<0>	0	11	29
MEM_B_DQS1	MEM_80D	MEM_B_DQS_1	MEM B DQS P<1>	1	11	29
MEM_B_DQS1	MEM_80D	MEM_B_DQS_1	MEM B DQS N<1>	1	11	29
MEM_B_DQS2	MEM_80D	MEM_B_DQS_2	MEM B DQS P<2>	2	11	29
MEM_B_DQS2	MEM_80D	MEM_B_DQS_2	MEM B DQS N<2>	2	11	29
MEM_B_DQS3	MEM_80D	MEM_B_DQS_3	MEM B DQS P<3>	3	11	29
MEM_B_DQS3	MEM_80D	MEM_B_DQS_3	MEM B DQS N<3>	3	11	29
MEM_B_DQS4	MEM_80D	MEM_B_DQS_4	MEM B DQS P<4>	4	11	30
MEM_B_DQS4	MEM_80D	MEM_B_DQS_4	MEM B DQS N<4>	4	11	30
MEM_B_DQS5	MEM_80D	MEM_B_DQS_5	MEM B DQS P<5>	5	11	30
MEM_B_DQS5	MEM_80D	MEM_B_DQS_5	MEM B DQS N<5>	5	11	30
MEM_B_DQS6	MEM_80D	MEM_B_DQS_6	MEM B DQS P<6>	6	11	30
MEM_B_DQS6	MEM_80D	MEM_B_DQS_6	MEM B DQS N<6>	6	11	30
MEM_B_DQS7	MEM_80D	MEM_B_DQS_7	MEM B DQS P<7>	7	11	30
MEM_B_DQS7	MEM_80D	MEM_B_DQS_7	MEM B DQS N<7>	7	11	30
MEM_PWR			PP1V5_S3RS0	6	7	
MEM_PWR			PP1V5_S3	6	7	
MEM_PWR			PP0V75_S3 MEM_VREFCA_A	27	28	31
MEM_PWR			PP0V75_S3 MEM_VREFDO_A	27	28	31

SYNC MASTER=113 CONSTRAINTS SYNC DATE=01/11/2012

Memory Constraints

Apple Inc.

DRAWING NUMBER: 051-9277 SIZE: D

REVISION: 2.8.0

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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ICOMP	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA3_PCH_TX	SATA3_PCH_TX	*	SATA3_TX2TX
SATA3_PCH_RX	SATA3_PCH_RX	*	SATA3_RX2RX
SATA3_PCH_TX	*_PCH_TX	*	SATA3_TX2OTHERTX
SATA3_PCH_RX	*_PCH_RX	*	SATA3_RX2OTHERRX
SATA3_PCH_TX	*_PCH_RX	*	SATA3_TX2RX
SATA3_PCH_RX	*_PCH_TX	*	SATA3_RX2TX
SATA3_PCH_TX	*_TX	*	SATA3_2OTHERHS
SATA3_PCH_RX	*_TX	*	SATA3_2OTHERHS
SATA3_PCH_TX	*_RX	*	SATA3_2OTHERHS
SATA3_PCH_RX	*_RX	*	SATA3_2OTHERHS
SATA3_PCH_TX	*	*	SATA3_2OTHER
SATA3_PCH_RX	*	*	SATA3_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
SATA3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
SATA3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
SATA3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA3_TX2TX	*	=2.5x_DIELECTRIC	?
SATA3_RX2RX	*	=2.5x_DIELECTRIC	?
SATA3_TX2OTHERTX	*	=4x_DIELECTRIC	?
SATA3_RX2OTHERRX	*	=4x_DIELECTRIC	?
SATA3_TX2RX	*	=6x_DIELECTRIC	?
SATA3_RX2TX	*	=6x_DIELECTRIC	?
SATA3_2OTHERHS	*	=4x_DIELECTRIC	?
SATA3_2OTHER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

UART Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
UART_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
UART	*	=2x_DIELECTRIC	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ixex Peak M (DG-398905-398905_v1.5), Section 3.8

USB 3.0 Interface Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_PCH_TX	USB3_PCH_TX	*	USB3_TX2TX
USB3_PCH_RX	USB3_PCH_RX	*	USB3_RX2RX
USB3_PCH_TX	*_PCH_TX	*	USB3_TX2OTHERTX
USB3_PCH_RX	*_PCH_RX	*	USB3_RX2OTHERRX
USB3_PCH_TX	*_PCH_RX	*	USB3_TX2RX
USB3_PCH_RX	*_PCH_TX	*	USB3_RX2TX
USB3_PCH_TX	*_TX	*	USB3_2OTHERHS
USB3_PCH_RX	*_TX	*	USB3_2OTHERHS
USB3_PCH_TX	*_RX	*	USB3_2OTHERHS
USB3_PCH_RX	*_RX	*	USB3_2OTHERHS
USB3_PCH_TX	*	*	USB3_2OTHER
USB3_PCH_RX	*	*	USB3_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	*	=2.5x_DIELECTRIC	?
USB3_RX2RX	*	=2.5x_DIELECTRIC	?
USB3_TX2OTHERTX	*	=4x_DIELECTRIC	?
USB3_RX2OTHERRX	*	=4x_DIELECTRIC	?
USB3_TX2RX	*	=6x_DIELECTRIC	?
USB3_RX2TX	*	=6x_DIELECTRIC	?
USB3_2OTHERHS	*	=4x_DIELECTRIC	?
USB3_2OTHER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		NET_NAME	NET_LAYER
	PHYSICAL	SPACING		
SATA_PCH_MUX_R2D	SATA_80D	SATA3_PCH_TX	SATA_HDD_R2D_C_P	16 38
SATA_PCH_MUX_R2D	SATA_80D	SATA3_PCH_TX	SATA_HDD_R2D_C_N	16 38
SATA_PCH_MUX_R2D	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_MUX_IN_P	38
SATA_PCH_MUX_R2D	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_MUX_IN_N	38
SATA_MUX_SSD_R2D	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_P	6 38
SATA_MUX_SSD_R2D	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_N	6 38
SATA_PCH_MUX_D2R	SATA_80D	SATA3_PCH_RX	SATA_HDD_D2R_P	16 38
SATA_PCH_MUX_D2R	SATA_80D	SATA3_PCH_RX	SATA_HDD_D2R_N	16 38
SATA_PCH_MUX_D2R	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_MUX_OUT_P	38
SATA_PCH_MUX_D2R	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_MUX_OUT_N	38
SATA_MUX_SSD_D2R	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_P	6 38
SATA_MUX_SSD_D2R	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_N	6 38
PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP	16
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_P	18 24
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_N	18 24
USB_BT	USB_80D	USB	USB_BT_P	24 37
USB_BT	USB_80D	USB	USB_BT_N	24 37
USB_BT	USB_80D	USB	USB_BT_CONN_P	6 37
USB_BT	USB_80D	USB	USB_BT_CONN_N	6 37
USB_BT	USB_80D	USB	USB_BT_WAKE_P	37
USB_BT	USB_80D	USB	USB_BT_WAKE_N	37
USB_TPAD	USB_80D	USB	USB_TPAD_P	49
USB_TPAD	USB_80D	USB	USB_TPAD_N	49
USB_TPAD	USB_80D	USB	USB_TPAD_CONN_P	6
USB_TPAD	USB_80D	USB	USB_TPAD_CONN_N	6
USB_TPAD_HUB	USB_80D	USB	USB_TPAD_HUB_P	24
USB_TPAD_HUB	USB_80D	USB	USB_TPAD_HUB_N	24
USB_TPAD_M	USB_80D	USB	USB_TPAD_R_P	24 49
USB_TPAD_M	USB_80D	USB	USB_TPAD_R_N	24 49
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_P	49
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_N	49
USB_SDCARD	USB_80D	USB	USB_SDCARD_P	24 33
USB_SDCARD	USB_80D	USB	USB_SDCARD_N	24 33
USB_SMC	USB_80D	USB	USB_SMC_P	24 41
USB_SMC	USB_80D	USB	USB_SMC_N	24 41
USB_CAMERA	USB_80D	USB	USB_CAMERA_P	6 18 40
USB_CAMERA	USB_80D	USB	USB_CAMERA_N	6 18 40
USB_EXT_A	USB_80D	USB	USB_EXT_A_P	18 39
USB_EXT_A	USB_80D	USB	USB_EXT_A_N	18 39
UART_45S	UART		SMC_DEBUGPRT_TX_L	39 41 42
UART_45S	UART		SMC_DEBUGPRT_RX_L	39 41 42
USB_80D	USB		USB2_EXT_A_MUXED_P	39
USB_80D	USB		USB2_EXT_A_MUXED_N	39
USB_80D	USB		USB2_EXT_A_MUXED_F_P	39
USB_80D	USB		USB2_EXT_A_MUXED_F_N	39
USB3_EXT_A_RX	USB_80D	USB3_PCH_RX	USB3_EXT_A_RX_P	18 39
USB3_EXT_A_RX	USB_80D	USB3_PCH_RX	USB3_EXT_A_RX_N	18 39
USB3_EXT_A_TX	USB_80D	USB3_PCH_TX	USB3_EXT_A_TX_P	18 39
USB3_EXT_A_TX	USB_80D	USB3_PCH_TX	USB3_EXT_A_TX_N	18 39
USB_80D	USB		USB3_EXT_A_RX_F_P	39
USB_80D	USB		USB3_EXT_A_RX_F_N	39
USB_80D	USB		USB3_EXT_A_TX_F_P	39
USB_80D	USB		USB3_EXT_A_TX_F_N	39
USB_80D	USB		USB3_EXT_A_TX_C_P	39
USB_80D	USB		USB3_EXT_A_TX_C_N	39
USB_EXT_B	USB_80D	USB	USB_EXT_B_P	6 24 40
USB_EXT_B	USB_80D	USB	USB_EXT_B_N	6 24 40
USB_EXT_B	USB_80D	USB	USB_EXT_B_EHCI_P	18 24
USB_EXT_B	USB_80D	USB	USB_EXT_B_EHCI_N	18 24
USB_EXT_B	USB_80D	USB	USB_EXT_B_XHCI_P	18 24
USB_EXT_B	USB_80D	USB	USB_EXT_B_XHCI_N	18 24
USB3_EXT_B_RX	USB_80D	USB3_PCH_RX	USB3_EXT_B_RX_P	18 40
USB3_EXT_B_RX	USB_80D	USB3_PCH_RX	USB3_EXT_B_RX_N	18 40
USB3_EXT_B_RX	USB_80D	USB3_PCH_RX	USB3_EXT_B_RX_RC_P	6 40
USB3_EXT_B_RX	USB_80D	USB3_PCH_RX	USB3_EXT_B_RX_RC_N	6 40
USB3_EXT_B_RX	USB_80D	USB3_PCH_RX	USB3_EXT_B_RX_CONN_P	6 40
USB3_EXT_B_RX	USB_80D	USB3_PCH_RX	USB3_EXT_B_RX_CONN_N	6 40
USB3_EXT_B_TX	USB_80D	USB3_PCH_TX	USB3_EXT_B_TX_P	18 40
USB3_EXT_B_TX	USB_80D	USB3_PCH_TX	USB3_EXT_B_TX_N	18 40
USB3_EXT_B_TX	USB_80D	USB3_PCH_TX	USB3_EXT_B_TX_C_P	6 40
USB3_EXT_B_TX	USB_80D	USB3_PCH_TX	USB3_EXT_B_TX_C_N	6 40
(USB_TPAD_HUB)	USB_80D	USB	USB_EXTD_XHCI_P	18 24
(USB_TPAD_HUB)	USB_80D	USB	USB_EXTD_XHCI_N	18 24
PCH_USB_RBBIAS	PCH_USB_RBBIAS		PCH_USB_RBBIAS	18
PCH_DIFPCLK_UNUSED	CLK_PCTE_80D	CLK_PCTE	PCIE_CLK100M_PCH_P	16
PCH_DIFPCLK_UNUSED	CLK_PCTE_80D	CLK_PCTE	PCIE_CLK100M_PCH_N	16
PCH_DIFPCLK_UNUSED	CLK_PCTE_80D	CLK_PCTE	PCH_CLK96M_DOT_P	16
PCH_DIFPCLK_UNUSED	CLK_PCTE_80D	CLK_PCTE	PCH_CLK96M_DOT_N	16
PCH_DIFPCLK_UNUSED	CLK_PCTE_80D	CLK_PCTE	PCH_CLK100M_SATA_P	16
PCH_DIFPCLK_UNUSED	CLK_PCTE_80D	CLK_PCTE	PCH_CLK100M_SATA_N	16
CPU_45S	CLK_PCTE	CLK_PCTE	PCH_CLK14P3M_REFCLK	16

SATA SSD

USB Hub nets

USB Camera nets

USB EXT_A nets (Right USB port)

USB EXT_B nets (Left USB port)

Unused USB nets

SYNC MASTER=113 CONSTRAINTS SYNC DATE=01/11/2012

PAGE TITLE: PCH Constraints 1

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=3x_DIELECTRIC	?
CLK_LPC	*	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ihex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S_R_50S	TOP,BOTTOM	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE		
SMB_45S_R_50S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ihex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=4x_DIELECTRIC	?

XDP Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_ITP	*	=2+1_SPACING	?

DisplayPort

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	*	=3x_DIELECTRIC	?	DP_2DP	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHERHS	*	=4x_DIELECTRIC	?	DP_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
DP_2OTHER	*	=3x_DIELECTRIC	?	DP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_AUX	*	=3x_DIELECTRIC	?	DP_AUX	TOP,BOTTOM	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP_TX	DP_TX	*	DP_2DP
DP_TX	*_TX	*	DP_2OTHERHS
DP_TX	*_RX	*	DP_2OTHERHS
DP_TX	*	*	DP_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
LPC_AD	LPC_45S	LPC	LPC AD<3..0>	6 16 41 43
LPC_FRAME_L	LPC_45S	LPC	LPC FRAME_L	6 16 41 43
LPC_45S	LPC_45S	LPC	LPCPLUS RESET_L	6 25 43
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC	25 41
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC_R	18 25
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS	6 25 43
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS_R	18 25
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	PCH_CLK33M_PCIIN	16 25
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	PCH_CLK33M_PCIOUT	18 25
SMBUS_PCH_CLK	SMB_45S_R_50S	SMB	SMBUS_PCH_CLK	16 44
SMBUS_PCH_DATA	SMB_45S_R_50S	SMB	SMBUS_PCH_DATA	16 44
SMBUS_PCH_0_CLK	SMB_45S_R_50S	SMB	SML_PCH_0_CLK	16 44
SMBUS_PCH_0_DATA	SMB_45S_R_50S	SMB	SML_PCH_0_DATA	16 44
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SML_PCH_1_CLK	16 44
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SML_PCH_1_DATA	16 44
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	6 16 40
HDA_45S	HDA_45S	HDA	HDA_BIT_CLK_R	16
HDA_SYNC	HDA_45S	HDA	HDA_SYNC	6 16 40
HDA_45S	HDA_45S	HDA	HDA_SYNC_R	16
HDA_RST_L	HDA_45S	HDA	HDA_RST_R_L	16
HDA_45S	HDA_45S	HDA	HDA_RST_L	6 16 40
HDA_SDINO	HDA_45S	HDA	HDA_SDINO	6 16 40
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	6 16 40
HDA_45S	HDA_45S	HDA	HDA_SDOUT_R	16 25
PM_SUS_CLK	CLK_SLOW_45S	CLK_SLOW	PM_CLK32K_SUSCLK_R	17 42
CLK_SLOW_45S	CLK_SLOW_45S	CLK_SLOW	SMC_CLK32K	41 42
SPT_CLK	SPT_45S	SPT	SPI_CLK_R	16 43
SPT_45S	SPT_45S	SPT	SPI_CLK	43
SPT_45S	SPT_45S	SPT	SPI_MOST_R	16 43
SPT_45S	SPT_45S	SPT	SPI_MOST	43
SPT_45S	SPT_45S	SPT	SPI_MISO	16 43
SPT_45S	SPT_45S	SPT	SPI_CS0_R_L	16 43
SPT_45S	SPT_45S	SPT	SPI_CS0_L	43
SPT_45S	SPT_45S	SPT	SPI_SMC_CLK	41 42
SPT_45S	SPT_45S	SPT	SPI_SMC_MOST	41 42
SPT_45S	SPT_45S	SPT	SPI_SMC_MISO	41 42
SPT_45S	SPT_45S	SPT	SPI_SMC_CS_L	41 42
SPT_45S	SPT_45S	SPT	SPI_MLB_CLK	42 43 50
SPT_45S	SPT_45S	SPT	SPI_MLB_MOST	42 43 50
SPT_45S	SPT_45S	SPT	SPI_MLB_MISO	42 43 50
SPT_45S	SPT_45S	SPT	SPI_MLB_CS_L	42 43 50
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE AP R2D_P	6 37
PCIE_80D	PCIE_80D	PCIE_PCH_TX	PCIE AP R2D_N	6 37
PCIE_80D	PCIE_80D	PCIE_PCH_TX	PCIE AP R2D_C_P	16 37
PCIE_80D	PCIE_80D	PCIE_PCH_TX	PCIE AP R2D_C_N	16 37
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE AP D2R_P	6 16 37
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE AP D2R_N	6 16 37
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_P	6 16 37
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_N	6 16 37
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE TBT R2D_P<3..0>	34
PCIE_80D	PCIE_80D	PCIE_PCH_TX	PCIE TBT R2D_N<3..0>	24
PCIE_80D	PCIE_80D	PCIE_PCH_TX	PCIE TBT R2D_C_P<3..0>	6 34
PCIE_80D	PCIE_80D	PCIE_PCH_TX	PCIE TBT R2D_C_N<3..0>	6 34
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE TBT D2R_P<3..0>	6 34
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE TBT D2R_N<3..0>	6 34
PCIE_80D	PCIE_80D	PCIE_PCH_RX	PCIE TBT D2R_C_P<3..0>	34
PCIE_80D	PCIE_80D	PCIE_PCH_RX	PCIE TBT D2R_C_N<3..0>	34
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_P	16 34
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_N	16 34
CLK_PCIE_80D	CLK_PCIE	CLK_PCIE	PEG_CLK100M_P	6 16
CLK_PCIE_80D	CLK_PCIE	CLK_PCIE	PEG_CLK100M_N	6 16
XDP_TDI	BCH_45S	BCH_ITP	XDP_PCH_TDI	16 23
XDP_TDO	BCH_45S	BCH_ITP	XDP_PCH_TDO	16 23
XDP_TMS	BCH_45S	BCH_ITP	XDP_PCH_TMS	16 23
XDP_TCK	BCH_45S	BCH_ITP	XDP_PCH_TCK	16 23

Chipset Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_P<3..0>	34
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_N<3..0>	34
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_C_P<3..0>	6 34
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_C_N<3..0>	6 34
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_P	34
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_N	34
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_P	6 34
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_N	6 34
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_P<3..0>	34
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_N<3..0>	34
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_C_P<3..0>	6 34
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_C_N<3..0>	6 34
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_P	34
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_N	34
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_P	6 34
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_N	6 34

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTC	16 25
SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB	16 25
SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB_R	16
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	25 34
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	34
SYSCLK_CLK25M_XTAL	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1	25
SYSCLK_CLK25M_XTAL	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2	25
SYSCLK_CLK25M_XTAL	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2_R	25

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_TX	TBTDP_TX	*	TBTDP_TX2TX	TBTDP_TX2TX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_RX	TBTDP_RX	*	TBTDP_RX2RX	TBTDP_RX2RX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_TX	TBTDP_RX	*	TBTDP_TX2RX	TBTDP_TX2RX	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_RX	TBTDP_TX	*	TBTDP_TX2RX	TBTDP_TX2RX	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_TX	*_TX	*	TBTDP_2OTHERHS	TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_RX	*_TX	*	TBTDP_2OTHERHS	TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_TX	*_RX	*	TBTDP_2OTHERHS	TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_RX	*_RX	*	TBTDP_2OTHERHS	TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_TX	*	*	TBTDP_2OTHER	TBTDP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?
TBTDP_RX	*	*	TBTDP_2OTHER	TBTDP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?
TBTDP_TX	*	*	TBTDP_2OTHER	TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_RX	*	*	TBTDP_2OTHER	TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_TX	*	*	TBTDP_2OTHER	TBTDP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?
TBTDP_RX	*	*	TBTDP_2OTHER	TBTDP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE		
	PHYSICAL	SPACING	
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT A R2D C P<1..0>
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT A R2D C N<1..0>
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT A R2D P<1..0>
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT A R2D N<1..0>
DP_TBTPA_ML1	DP_80D	DP_TX	DP TBTPA ML C P<1>
DP_TBTPA_ML1	DP_80D	DP_TX	DP TBTPA ML C N<1>
DP_TBTPA_ML3	DP_80D	DP_TX	DP TBTPA ML C P<3>
DP_TBTPA_ML3	DP_80D	DP_TX	DP TBTPA ML C N<3>
	DP_80D	DP_TX	DP TBTPA ML P<3..1:2>
	DP_80D	DP_TX	DP TBTPA ML N<3..1:2>
	DP_80D	DP_TX	DP A LSX ML P<1>
	DP_80D	DP_TX	DP A LSX ML N<1>
	TBTDP_80D	TBTDP_RX	TBT A D2R C P<1..0>
	TBTDP_80D	TBTDP_RX	TBT A D2R C N<1..0>
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT A D2R P<1>
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT A D2R N<1>
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT A D2R P<0>
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT A D2R N<0>
TBT_A_AUXCH	DP_80D	DP_AUX	DP TBTPA AUXCH C P
TBT_A_AUXCH	DP_80D	DP_AUX	DP TBTPA AUXCH C N
	DP_80D	DP_AUX	DP TBTPA AUXCH P
	DP_80D	DP_AUX	DP TBTPA AUXCH N
	DP_80D	DP_AUX	DP A AUXCH DDC P
	DP_80D	DP_AUX	DP A AUXCH DDC N
	TBTDP_80D	TBTDP_RX	TBT A D2R1 AUXDDC P
	TBTDP_80D	TBTDP_RX	TBT A D2R1 AUXDDC N
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT B R2D C P<1..0>
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT B R2D C N<1..0>
	TBTDP_80D	TBTDP_TX	TBT B R2D P<1..0>
	TBTDP_80D	TBTDP_TX	TBT B R2D N<1..0>
DP_TBTPB_ML	DP_80D	DP_TX	DP TBTPB ML C P<3..1:2>
DP_TBTPB_ML	DP_80D	DP_TX	DP TBTPB ML C N<3..1:2>
	DP_80D	DP_TX	DP TBTPB ML P<3..1:2>
	DP_80D	DP_TX	DP TBTPB ML N<3..1:2>
	DP_80D	DP_TX	DP B LSX ML P<1>
	DP_80D	DP_TX	DP B LSX ML N<1>
	TBTDP_80D	TBTDP_RX	TBT B D2R C P<1..0>
	TBTDP_80D	TBTDP_RX	TBT B D2R C N<1..0>
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT B D2R P<1..0>
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT B D2R N<1..0>
TBT_B_AUXCH	DP_80D	DP_AUX	DP TBTPB AUXCH C P
TBT_B_AUXCH	DP_80D	DP_AUX	DP TBTPB AUXCH C N
	DP_80D	DP_AUX	DP TBTPB AUXCH P
	DP_80D	DP_AUX	DP TBTPB AUXCH N
	DP_80D	DP_AUX	DP B AUXCH DDC P
	DP_80D	DP_AUX	DP B AUXCH DDC N
	TBTDP_80D	TBTDP_RX	TBT B D2R1 AUXDDC P
	TBTDP_80D	TBTDP_RX	TBT B D2R1 AUXDDC N

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE		
	PHYSICAL	SPACING	
	DP_80D	DP_TX	DP TBTSRC ML C P<3..0>
	DP_80D	DP_TX	DP TBTSRC ML C N<3..0>
	DP_80D	DP_AUX	DP TBTSRC AUXCH C P
	DP_80D	DP_AUX	DP TBTSRC AUXCH C N
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT SPI CLK
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT SPI MOSI
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT SPI MISO
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT SPI CS_L

Only used on hosts supporting Thunderbolt video-in

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
SMBUS_SMC_0_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SCL	41 44
SMBUS_SMC_0_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SDA	41 44
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL	41 44
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA	41 44
SMBUS_SMC_2_S3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_2_S3_SCL	41 44
SMBUS_SMC_2_S3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_2_S3_SDA	41 44
SMBUS_SMC_3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SCL	41 44
SMBUS_SMC_3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SDA	41 44
SMBUS_SMC_5_G3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SCL	41 44
SMBUS_SMC_5_G3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SDA	41 44

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSI_P	53
SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSI_N	53
	1:1_DIFFPAIR		CHGR_CSI_R_P	53
	1:1_DIFFPAIR		CHGR_CSI_R_N	53
SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSO_P	53
SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSO_N	53
	1:1_DIFFPAIR		CHGR_CSO_R_P	53
	1:1_DIFFPAIR		CHGR_CSO_R_N	53

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J11/J13 Specific Net Properties

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
SENSE_1T01_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
SENSE_1T01_P2MM	*	=1:1_DIFFPAIR	0.200 MM	0.100 MM	=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1T01_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
SPKR_DIFFPAIR	*	=1:1_DIFFPAIR	0.300 MM	0.100 MM	=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
GND	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	CLK_PCIE	*	GND_P2MM
GND	PCIE*	*	GND_P2MM
GND	SATA*	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	USB*	*	GND_P2MM
GND	LVDS*	*	GND_P2MM
SB_POWER	CLK_PCIE	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	INLET_THMSNS_D1_P	46 47
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	INLET_THMSNS_D1_N	46 47
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBT_THERMD_P	47
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBT_THERMD_N	47
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBT_MLBBOT_THMSNS_P	47
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBT_MLBBOT_THMSNS_N	47
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBTTHMSNS_D2_R_P	47
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBTTHMSNS_D2_R_N	47
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPU_THERMD_P	9 47
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPU_THERMD_N	9 47
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPU_THMSNS_D2_P	47
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPU_THMSNS_D2_N	47
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUVCCIOS0_CS_N	45 59
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUVCCIOS0_CS_P	45 59
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUIMVP_ISNS1_P	45 57 58
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUIMVP_ISNS1_N	45 58
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPUIMVP_ISUM_R_P	45
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPUIMVP_ISUM_R_N	45
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUIMVP_ISNS1G_P	45 58
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUIMVP_ISNS1G_N	45 58
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPUIMVP_ISUMG_R_P	45
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPUIMVP_ISUMG_R_N	45
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	VCCSAS0_CS_P	45 54
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	VCCSAS0_CS_N	45 54
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	VCCSAISNS_R_P	45
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	VCCSAISNS_R_N	45
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_3V3S0_P	45 61
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_3V3S0_N	45 61
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_3V3S0_R_P	45
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_3V3S0_R_N	45
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUIMVP_ISUMG_P	57 58
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUIMVP_ISUMG_N	57 58
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUIMVP_ISUM_P	57 58
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUIMVP_ISUM_N	57 58
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_HS_COMPUTING_N	8 46
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_HS_COMPUTING_P	8 46
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_HS_OTHER_N	46
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_HS_OTHER_P	46
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_1V5_S3_N	46 56
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_1V5_S3_P	46 56
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_AIRPORT_N	37 46
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_AIRPORT_P	37 46
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_SSD_N	38 46
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_SSD_P	38 46
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_LCDBKLT_N	8 46
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS_LCDBKLT_P	8 46
AUD_DIFF	1:1_DIFFPAIR	AUDIO	SPKRAMP_INR_P	6 40 51
AUD_DIFF	1:1_DIFFPAIR	AUDIO	SPKRAMP_INR_N	6 40 51
	1:1_DIFFPAIR	AUDIO	MAX98300_R_P	51
	1:1_DIFFPAIR	AUDIO	MAX98300_R_N	51
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT_P	6 51 52
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT_N	6 51 52
		SB_POWER	PP3V3_S5	6 7
		SB_POWER	PP3V3_S0	6 7
		GND	GND	

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J11/J13 Board-Specific Spacing & Physical Constraints

BOARD LAYERS		BOARD AREAS			BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM		NO_TYPE, BGA			MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	TOP, BOTTOM	Y	=50_OHM_SE	=50_OHM_SE			
DEFAULT	ISL2, ISL11	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL3, ISL10	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL4, ISL9	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	*	N	100 MM	100 MM	10 MM	0 MM	0 MM
STANDARD	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

Single-ended Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	ISL2, ISL11	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL3, ISL10	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL4, ISL9	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP, BOTTOM	Y	0.195 MM	0.195 MM			
35_OHM_SE	ISL2, ISL11	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL3, ISL10	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL4, ISL9	Y	0.125 MM	0.125 MM			
35_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL2, ISL11	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL3, ISL10	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL4, ISL9	Y	0.099 MM	0.099 MM			
40_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP, BOTTOM	Y	0.135 MM	0.135 MM			
45_OHM_SE	ISL2, ISL11	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL3, ISL10	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL4, ISL9	Y	0.080 MM	0.080 MM			
45_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Differential Pair Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	TOP, BOTTOM	Y	0.165 MM	0.165 MM		0.130 MM	0.130 MM
72_OHM_DIFF	ISL2, ISL11	Y	0.109 MM	0.109 MM		0.150 MM	0.150 MM
72_OHM_DIFF	ISL3, ISL10	Y	0.109 MM	0.109 MM		0.150 MM	0.150 MM
72_OHM_DIFF	ISL4, ISL9	Y	0.114 MM	0.114 MM		0.150 MM	0.150 MM
72_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	TOP, BOTTOM	Y	0.132 MM	0.132 MM		0.130 MM	0.130 MM
80_OHM_DIFF	ISL2, ISL11	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL3, ISL10	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL4, ISL9	Y	0.088 MM	0.088 MM		0.110 MM	0.110 MM
80_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Spacing Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.100 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP, BOTTOM	0.071 MM	?
1x_DIELECTRIC	ISL3, ISL10	0.053 MM	?
1x_DIELECTRIC	ISL4, ISL9	0.050 MM	?
1x_DIELECTRIC	*	0.090 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM

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