1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
D		428208	PRODUCTION RELEASED	03/04/05	

SCHEM,MLB,M1

03/03/2006

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7099	1	SCHEM,MLB,M1	SCH	CRITICAL	
820-1881	1	PCBF,MLB,M1	PCB	CRITICAL	

DRAWING
TITLE=M1_MLB
ABBREV=DRAWING
LAST_MODIFIED=Fri Mar 3 15:00:30 2006

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

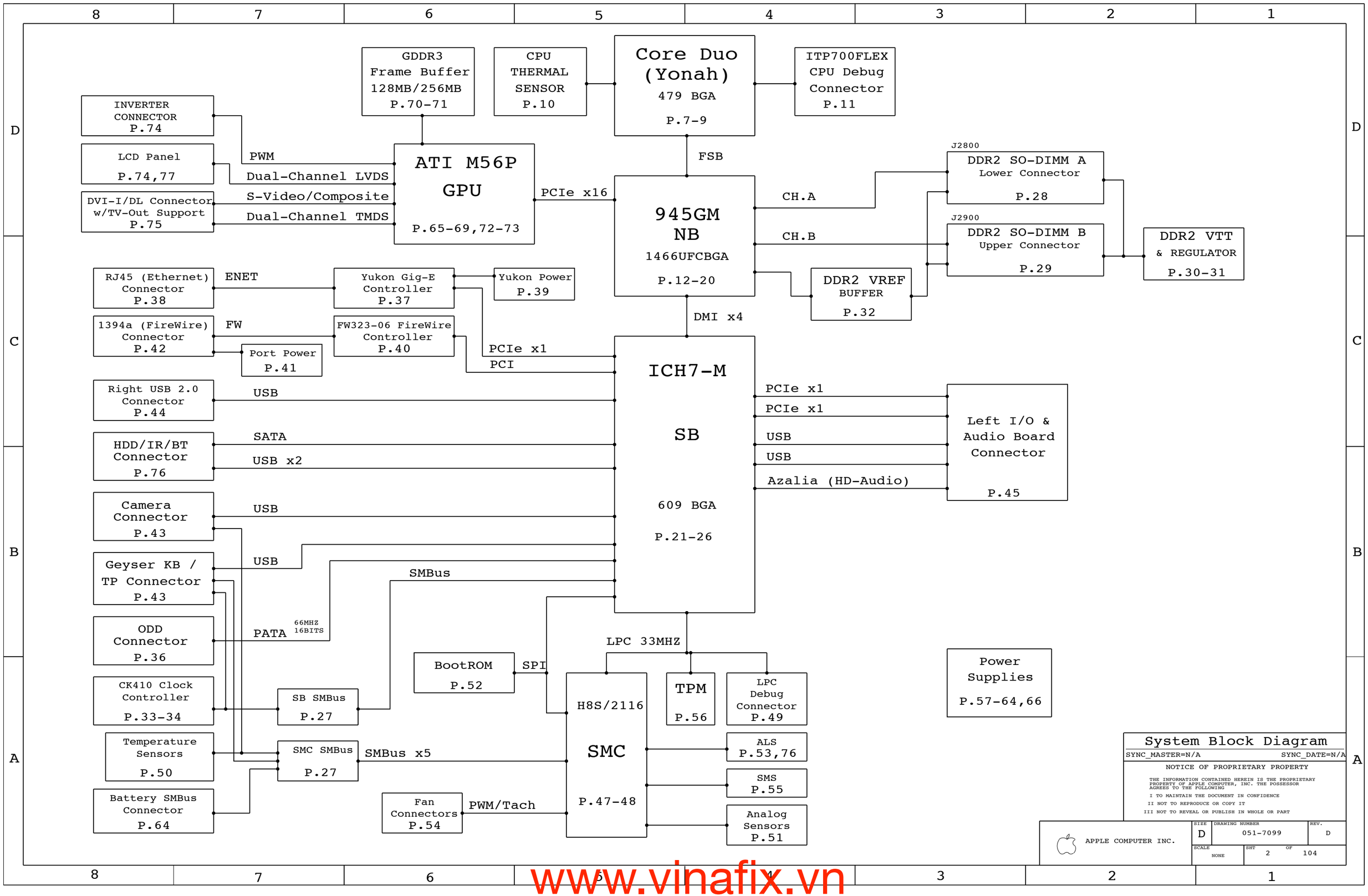
MATERIAL/FINISH NOTED AS APPLICABLE
SIZE D

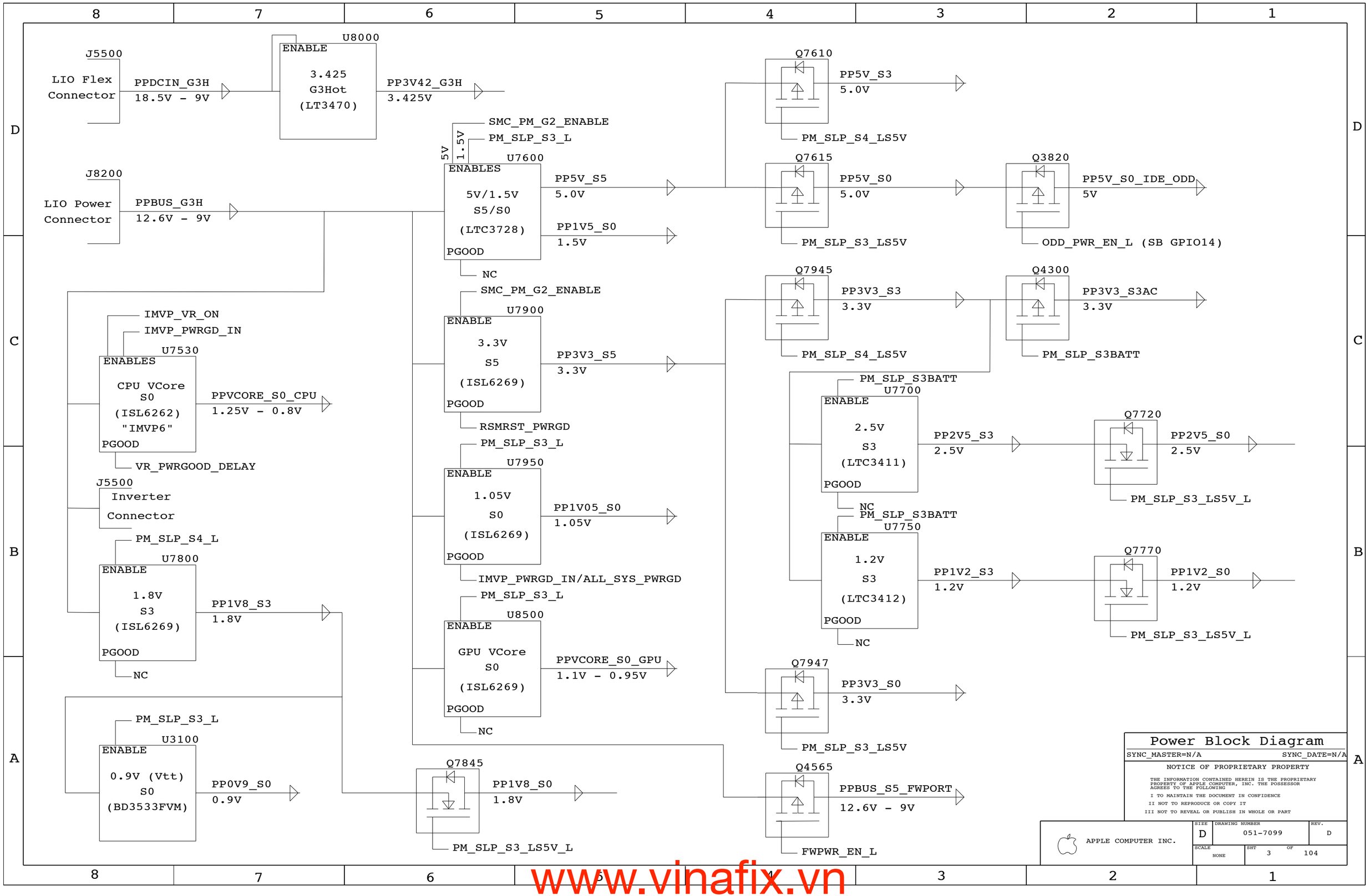
Apple Computer Inc.

TITLE
SCHEM,MLB,M1

DRAWING NUMBER 051-7099 REV. D

SHT 1 OF 104





"Better" BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7569	PCBA,1.83GHZ,128VRAM_M1_MBPRO_15	EEE_VHT,M1_COMMON,CPU_1_83GHZ,VRAM_SAM128

"Best" BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7570	PCBA,2.0GHZ,256VRAM_M1_MBPRO_15	EEE_VHU,M1_COMMON,CPU_2_0GHZ,VRAM_SAM256

"CTO" BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7571	PCBA,2.16GHZ,256VRAM_M1_MBPRO_15	EEE_VHV,M1_COMMON,CPU_2_16GHZ,VRAM_SAM256

BOMOPTION Groups

BOM GROUP	BOM OPTIONS
M1_COMMON	ALTERNATE,COMMON,M1_COMMON1,M1_COMMON2,M1_COMMON3
M1_COMMON1	BOOTROM_DEVEL,ENET_LOM_DISABLE,ENETPWR_S3AC,GPU_BB_CTL,GPUTHM_A_GPU,HSTHMSNS_HAS
M1_COMMON2	ITP,INVERTER_BUF,KBDLED_HAS,LPCPLUS,LVDS_PD,MEMVREF_S3,MEMVTT_EN_PU
M1_COMMON3	RTUSB_ESD,SMC_PRGRM,USB_C_OC_PU,USB_D_OC_PU,USB_E_OC_PU
VRAM_HY128	GPU_MEM_HYNIX,VRAM_128_HYNIX
VRAM_SAM128	VRAM_128_SAMSUNG
VRAM_HY256	GPU_MEM_256M,GPU_MEM_HYNIX,VRAM_256_HYNIX
VRAM_SAM256	GPU_MEM_256M,VRAM_256_SAMSUNG

Bar Code Label / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:VHT]	CRITICAL	EEE_VHT	M1,1.83GHZ,SAM128
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:VHU]	CRITICAL	EEE_VHU	M1,2.0GHZ,SAM256
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:VHV]	CRITICAL	EEE_VHV	M1,2.16GHZ,SAM256

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0354	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_SAMSUNG
333S0350	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_SAMSUNG
333S0358	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_HYNIX
333S0351	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_HYNIX
337S3282	1	IC,YDC,CO,1.83G,31W,667M,2M,479BGA	U0700	CRITICAL	CPU_1_83GHZ
337S3267	1	IC,YDC,CO,2.0G,31W,667M,2M,479BGA	U0700	CRITICAL	CPU_2_0GHZ
337S3268	1	IC,YDC,CO,2.16G,31W,667M,2M,479BGA	U0700	CRITICAL	CPU_2_16GHZ
341S1873	1	IC,EFI,BOOTROM DEVELOPMENT (NEW),M1	U6301	CRITICAL	BOOTROM_DEVEL
338S0274	1	IC,SMC,HS8/2116	U5800	CRITICAL	SMC_BLANK
341S1875	1	IC,PRGRM,SMC (NEW),M1	U5800	CRITICAL	SMC_PRGRM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0268	1	IC,FW32306,1394A LINK,BGA,129P	U4400	CRITICAL	
338S0269	1	IC,945GM,SOUTHBRIDGE	U1200	CRITICAL	
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN, NO	U4101	CRITICAL	
338S0309	1	IC,ATI,M56P,GRPHSCTRL,880BGA,LF	U8400	CRITICAL	
341S1789	1	IC, TPM, 28-PIN TSSOP	U6700	CRITICAL	
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U4102	CRITICAL	
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
353S1235	1	IC,CPU VOLTAGE REGULATOR,IMVP,TWO PHASE	U7530	CRITICAL	
359S0101	1	IC,CY28445-5,CLOCK GEN,68PIN QFN	U3301	CRITICAL	

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0094	128S0060		ALL	330uF,2V,9MOHM,D2
128S0095	128S0060		ALL	330uF,2V,6MOHM,D2
128S0081	128S0061		ALL	150uF,6.3V,25MOHM,C2
128S0077	128S0086		ALL	7mOhm alt for 8mOhm

BOM Configuration

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE NONE SHT 4 OF 104

Functional Test Points

Power Supply NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		IMVP6_RBIAS	57
TRUE		IMVP6_COMP	57
TRUE		P5VS5_RUNSS	58 62
TRUE		P1V5S0_RUNSS	58 62
TRUE		P2V5S3_MODE	59
TRUE		P2V5S3_SHDNRT	59
TRUE		P1V2S3_RT	59
TRUE		P1V2S3_RUNSS	39 59
TRUE		P1V8S3_COMP	60
TRUE		P1V8S3_FSET	60
TRUE		P3V3S5_COMP	61
TRUE		P3V3S5_FSET	61
TRUE		P1V05S0_COMP	61
TRUE		P1V05S0_FSET	61
TRUE		P3V42G3H_FB	62
TRUE		GPUVCORE_COMP	66
TRUE		GPUVCORE_FSET	66
TRUE		GPUBBP_ADJ	66

CPU FSB NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		FSB_A_L<31..3>	7 12 79
TRUE		FSB_ADS_L	7 12 79
TRUE	TRUE	FSB_ADSTB_L<1..0>	7 12 79
TRUE		FSB_BNR_L	7 12 79
TRUE		FSB_BREQ0_L	7 12 79
TRUE		FSB_D_L<63..0>	7 12 79
TRUE		FSB_DBSY_L	7 12 79
TRUE	TRUE	FSB_DINV_L<3..0>	7 12 79
TRUE		FSB_DRDY_L	7 12 79
TRUE	TRUE	FSB_DSTBN_L<3..0>	7 12 79
TRUE	TRUE	FSB_DSTBP_L<3..0>	7 12 79
TRUE		FSB_HIT_L	7 12 79
TRUE		FSB_HITM_L	7 12 79
TRUE		FSB_LOCK_L	7 12 79
TRUE		FSB_REQ_L<4..0>	7 12 79

EXPOSED_VIA property indicates that the net should have a via with 10-mil soldermask opening for use as engineering probe point.

Misc EXPOSED_VIA Nets

EXPOSED_VIA		
TRUE	DMI_N2S_P<1..0>	14 22
TRUE	DMI_N2S_N<1..0>	14 22
TRUE	SB_CLK100M_SATA_P	21 34
TRUE	SB_CLK100M_SATA_N	21 34

FUNC_TEST property removed since these test points are not on the proper side for Functional Test points.

Fan Connectors

FUNC_TEST	
TRUE	=PP5V_S0_FAN_LT 54 63
TRUE	FAN_LT_PWM 54
TRUE	FAN_LT_TACH 54
TRUE	FAN_RT_PWM 54
TRUE	FAN_RT_TACH 54

LPC+ Debug Connector

FUNC_TEST	
TRUE	=PP3V3_S5_LPCPLUS 49 63
TRUE	=PP5V_S0_LPCPLUS 49 63
TRUE	LPC_AD<0> 21 47 49 56
TRUE	LPC_AD<1> 21 47 49 56
TRUE	LPC_FRAME_L 21 47 49 56
TRUE	PM_CLKRUN_L 23 40 47 49 56
TRUE	BOOT_LPC_SPI_L 22 47 49
TRUE	SMC_TMS 47 48 49
TRUE	DEBUG_RST_L 26 49
TRUE	SMC_TRST_L 47 49
TRUE	SMC_TDO 47 48 49
TRUE	SMC_MD1 47 49
TRUE	SMC_TX_L 47 48 49
TRUE	FWH_INIT_L 21 48 49
TRUE	PCI_CLK_PORT80_LPC 34 49
TRUE	LPC_AD<2> 21 47 49 56
TRUE	LPC_AD<3> 21 47 49 56
TRUE	INT_SERIRQ 23 47 49 56
TRUE	PM_SUS_STAT_L 23 47 48 49 56
TRUE	SMC_TDI 47 48 49
TRUE	SMC_TCK 47 48 49
TRUE	SMC_RST_L 47 48 49
TRUE	SMC_NMI 47 49
TRUE	SMC_RX_L 47 48 49
TRUE	SV_SET_UP 23 49

Left ALS Connector

FUNC_TEST	
TRUE	=PP3V3_S3_LTALS 63 76
TRUE	ALS_GAIN 6 47 76
TRUE	LTALS_OUT 53 76
TRUE	GND

Camera Connector

FUNC_TEST	
TRUE	=PP5V_S3_CAMERA 43 63
TRUE	=USB2_CAMERA_N 6 43
TRUE	=USB2_CAMERA_P 6 43
TRUE	=SMBUS_ATS_SDA 27 43
TRUE	=SMBUS_ATS_SCL 27 43
TRUE	GND

Thermal Diode Connectors

FUNC_TEST	
TRUE	HSTHMSNS_DX_P 50
TRUE	HSTHMSNS_DX_N 50
TRUE	RSFSTHMSNS_D_P 50
TRUE	RSFSTHMSNS_D_N 50

Other Func Test Points

FUNC_TEST	
TRUE	=PP1V05_S0_REG 51 61 63
TRUE	PM_SYSRST_L 23 26 47
TRUE	SMC_ONOFF_L 43 47 48 51

Current Sense Calibration

FUNC_TEST	
TRUE	ISENSE_CAL_EN
TRUE	=PP5V_S0_ISENSECAL
TRUE	=PP1V8_S3_REG 51 60 63
TRUE	=PP1V5_S0_REG 58 63
TRUE	PPVCORE_S0_GPU 63
TRUE	PPVCORE_S0_CPU 63
TRUE	GND

2 TPs per

8 TPs, 2 with each of above TP pairs

Battery Digital Connector

FUNC_TEST	
TRUE	SMC_BS_ALRT_L 47 48 64
TRUE	=SMBUS_BATT_SCL 27 64
TRUE	=SMBUS_BATT_SDA 27 64
TRUE	GND_BATT 64

Left I/O Data Connector

FUNC_TEST	
TRUE	=PP1V5_S0_LIO 45 63
TRUE	=PPDCIN_G3H_LIO 45 63
TRUE	=PP5V_S5_LIO 45 63
TRUE	=PP3V42_G3H_LIO 45 63
TRUE	PP5V_S0_AUDIO_PWR 45
TRUE	PP5V_S0_AUDIO 45
TRUE	GND_AUDIO_PWR 45
TRUE	GND_AUDIO 45
TRUE	ACZ_SDATAIN<0> 21 45 79
TRUE	ACZ_SDATAOUT 21 45 79
TRUE	ACZ_BITCLK 21 45 79
TRUE	ACZ_RST_L 21 45 79
TRUE	EXCARD_OC_L 6 45 48
TRUE	LTUSB_OC_L 6 45
TRUE	LIO_BATT_ISENSE 45 51
TRUE	SMC_SYS_ISET 45 47
TRUE	SMC_BATT_ISET 45 47
TRUE	SMC_BATT_CHG_EN 45 47 48
TRUE	SMC_BC_ACOK 45 47 48
TRUE	SMC_ADAPTER_EN 41 45 47 48
TRUE	LIO_P3V3S0_EN_L 45 62
TRUE	LIO_DCIN_ISENSE 45 51
TRUE	LIO_P3V3S3_EN 45 62
TRUE	SMC_BATT_TRICKLE_EN_L 45 47 48
TRUE	SYS_ONEWIRE 45 47 48
TRUE	MINI_CLKREQ_L 34 45
TRUE	SMC_EXCARD_CP 45 47 48
TRUE	EXCARD_CLKREQ_L 34 45
TRUE	SMC_EXCARD_PWR_EN 45 47
TRUE	LIO_PLT_RESET_L 26 45
TRUE	ACZ_SYNC 21 45 79
TRUE	=USB2_LT_N 6 45
TRUE	=USB2_LT_P 6 45
TRUE	=USB2_EXCARD_N 6 45
TRUE	=USB2_EXCARD_P 6 45
TRUE	=PCIE_EXCARD_R2D_N 45 46
TRUE	=PCIE_EXCARD_R2D_P 45 46
TRUE	=PCIE_EXCARD_D2R_N 45 46
TRUE	=PCIE_EXCARD_D2R_P 45 46
TRUE	PCIE_CLK100M_EXCARD_P 34 45
TRUE	PCIE_CLK100M_EXCARD_N 34 45
TRUE	=PCIE_MINI_R2D_N 45 46
TRUE	=PCIE_MINI_R2D_P 45 46
TRUE	=PCIE_MINI_D2R_N 45 46
TRUE	=PCIE_MINI_D2R_P 45 46
TRUE	PCIE_CLK100M_MINI_P 34 45
TRUE	PCIE_CLK100M_MINI_N 34 45
TRUE	=SMBUS_LIO_SMC_SCL 27 45
TRUE	=SMBUS_LIO_SMC_SDA 27 45
TRUE	=SMBUS_LIO_SB_SCL 27 45
TRUE	=SMBUS_LIO_SB_SDA 27 45
TRUE	PCIE_WAKE_L 23 37 45

Left I/O Power Connector

FUNC_TEST	
TRUE	=PPBUS_G3H_LIO_CONN 63 64
TRUE	GND

Request for at least 10 GND test points

NOTE: 10 additional GND test points are called out separately in these notes.

Functional / ICT Test

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7099	REV. D
	SCALE NONE	SHT 5 OF 104	

NC_CPU_A32_L — TP_CPU_A32_L (7)
NC_CPU_A33_L — TP_CPU_A33_L (7)
NC_CPU_A34_L — TP_CPU_A34_L (7)
NC_CPU_A35_L — TP_CPU_A35_L (7)
NC_CPU_A36_L — TP_CPU_A36_L (7)
NC_CPU_A37_L — TP_CPU_A37_L (7)
NC_CPU_A38_L — TP_CPU_A38_L (7)
NC_CPU_A39_L — TP_CPU_A39_L (7)
NC_CPU_APM0_L — TP_CPU_APM0_L (7)
NC_CPU_APM1_L — TP_CPU_APM1_L (7)
NC_CPU_EXTBREF — TP_CPU_EXTBREF (7)
NC_CPU_HFPLL — TP_CPU_HFPLL (7)
NC_CPU_SPARE0 — TP_CPU_SPARE0 (7)
NC_CPU_SPARE1 — TP_CPU_SPARE1 (7)
NC_CPU_SPARE2 — TP_CPU_SPARE2 (7)
NC_CPU_SPARE4 — TP_CPU_SPARE4 (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_MEM_A_A<15..14> — MEM_A_A<15..14> (28)
NC_MEM_B_A<15..14> — MEM_B_A<15..14> (29)
MAKE_BASE=TRUE, NO_TEST=TRUE

TP_NB_CFG<4..3> — NB_CFG<4..3> (14)
TP_NB_CFG<6> — NB_CFG<6> (14)
TP_NB_CFG<8> — NB_CFG<8> (14)
TP_NB_CFG<11..10> — NB_CFG<11..10> (14)
TP_NB_CFG<15..14> — NB_CFG<15..14> (14)
TP_NB_CFG<17> — NB_CFG<17> (14)
MAKE_BASE=TRUE

NOTE: NB_CFG<13..12> require test access

TP_NB_CFG<13..12> — NB_CFG<13..12> (14)
MAKE_BASE=TRUE

TP_SB_SUS_CLK — SUS_CLK_SB (23)
MAKE_BASE=TRUE

NC_SB_XOR_T5 — TP_SB_XOR_T5 (21)
NC_SB_XOR_U5 — TP_SB_XOR_U5 (21)
NC_SB_XOR_V3 — TP_SB_XOR_V3 (21)
NC_SB_XOR_V4 — TP_SB_XOR_V4 (21)
NC_SB_XOR_W3 — TP_SB_XOR_W3 (21)
MAKE_BASE=TRUE, NO_TEST=TRUE

TP_SMC_RSTGATE_L — SMC_RSTGATE_L (47)
ALS_GAIN (76 47 5) — =RTALS_GAIN (53)
MAKE_BASE=TRUE

NC_ENET_CTRL12 — ENET_CTRL12 (37)
NC_ENET_CTRL25 — ENET_CTRL25 (37)
MAKE_BASE=TRUE, NO_TEST=TRUE

Ethernet Power Management Support

ENET_LOM_DISABLE
R0600
0
5%
1/16W
MF-LF
402

SB_GPIO30 (13) — 1 — 2 — ENET_LOM_DIS_L (37) (OUT)

NOTE: BOM options "USB_G_OC_PU" and "ENET_LOM_DISABLE" are mutually-exclusive.

USB Port "A" (Debug Port) = Right USB 2.0 Port

=USB2_RT_P (44) — USB2_RT_P — USB_A_P (22)
=USB2_RT_N (44) — USB2_RT_N — USB_A_N (22)
=RTUSB_OC_L (44) — RTUSB_OC_L — USB_A_OC_L (22)
MAKE_BASE=TRUE

USB Port "B" = Trackpad (Geyser)

=USB_TRACKPAD_P (43) — USB_TRACKPAD_P — USB_B_P (22)
=USB_TRACKPAD_N (43) — USB_TRACKPAD_N — USB_B_N (22)
MAKE_BASE=TRUE

UNUSED_USB_B_OC_L — USB_B_OC_L (22)
MAKE_BASE=TRUE

USB Port "C" = Left USB 2.0 Port

=USB2_LT_P (45 5) — USB2_LT_P — USB_C_P (22)
=USB2_LT_N (45 5) — USB2_LT_N — USB_C_N (22)
MAKE_BASE=TRUE

LTUSB_OC_L (45 5) — USB_C_OC_L (22)
MAKE_BASE=TRUE

USB Port "D" = Camera

=USB2_CAMERA_P (43 5) — USB2_CAMERA_P — USB_D_P (22)
=USB2_CAMERA_N (43 5) — USB2_CAMERA_N — USB_D_N (22)
MAKE_BASE=TRUE

UNUSED_USB_D_OC_L — USB_D_OC_L (22)
MAKE_BASE=TRUE

USB Port "E" = ExpressCard

=USB2_EXCARD_P (45 5) — USB2_EXCARD_P — USB_E_P (22)
=USB2_EXCARD_N (45 5) — USB2_EXCARD_N — USB_E_N (22)
MAKE_BASE=TRUE

EXCARD_OC_L (48 45 5) — USB_E_OC_L (22)
MAKE_BASE=TRUE

USB Port "F" = IR Receiver

=USB_IR_P (76) — USB_IR_P — USB_F_P (22)
=USB_IR_N (76) — USB_IR_N — USB_F_N (22)
MAKE_BASE=TRUE

USB Port "G" = Bluetooth (M13P)

=USB_BT_P (76) — USB_BT_P — USB_G_P (22)
=USB_BT_N (76) — USB_BT_N — USB_G_N (22)
MAKE_BASE=TRUE

USB Port "H" = Reserved (PCI-E Mini Card)

TP_USB2_HP — USB_H_P (22)
TP_USB2_HN — USB_H_N (22)
MAKE_BASE=TRUE

Trace deleted to make room for other diffpairs over RAM connector.

Chassis connection to be made at the mounting hole northwest of the DVI connector
ZT0600
HOLE-VIA-P5RP25
GND_CHASSIS_DVI_TOP
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
=GND_CHASSIS_DVI2 (75)
=GND_CHASSIS_DVI4 (75)

Chassis connection to be made at the mounting hole southwest of the USB connector
ZT0601
HOLE-VIA-P5RP25
GND_CHASSIS_DVI_BOT
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
=GND_CHASSIS_DVI1 (75)
=GND_CHASSIS_DVI3 (75)
=GND_CHASSIS_DVI5 (75)
=GND_CHASSIS_ENET (38)
=GND_CHASSIS_FW_EMI (42)
=GND_CHASSIS_FW_PORT1 (42)
=GND_CHASSIS_RTUSB (44)

Chassis connection to be made at the mounting hole east of the LVDS connector
ZT0602
HOLE-VIA-P5RP25
GND_CHASSIS_LVDS
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
=GND_CHASSIS_LCD1 (74)
=GND_CHASSIS_LCD2 (74)
=GND_CHASSIS_LCD3 (74)
=GND_CHASSIS_LCD4 (74)

SH0600
OG-503040
SHLD-SM-LF
GND_CHASSIS_INVERTER
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
=GND_CHASSIS_INVERTER (74)

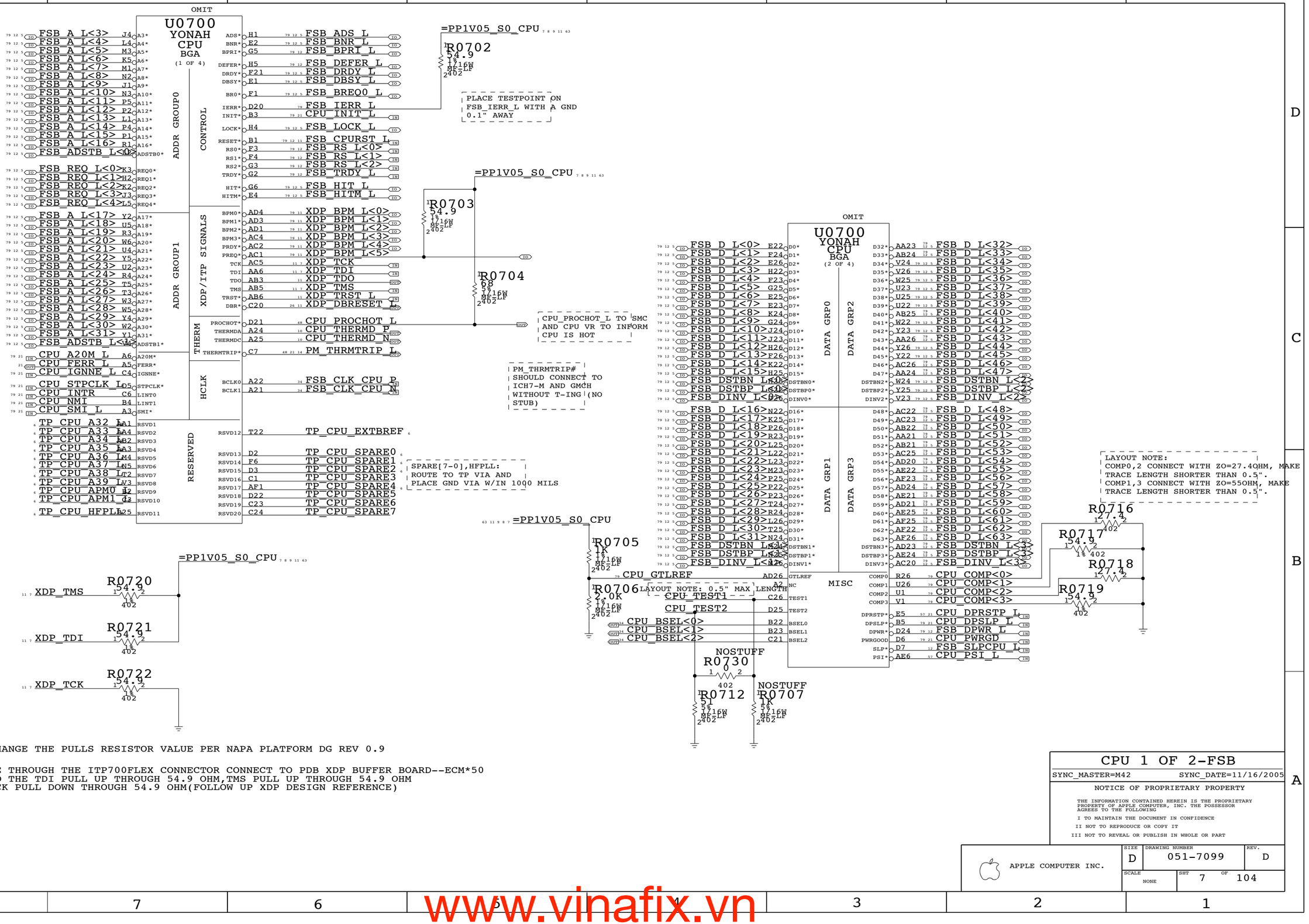
Signal Aliases

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE: NONE — SHT 6 OF 104



CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9

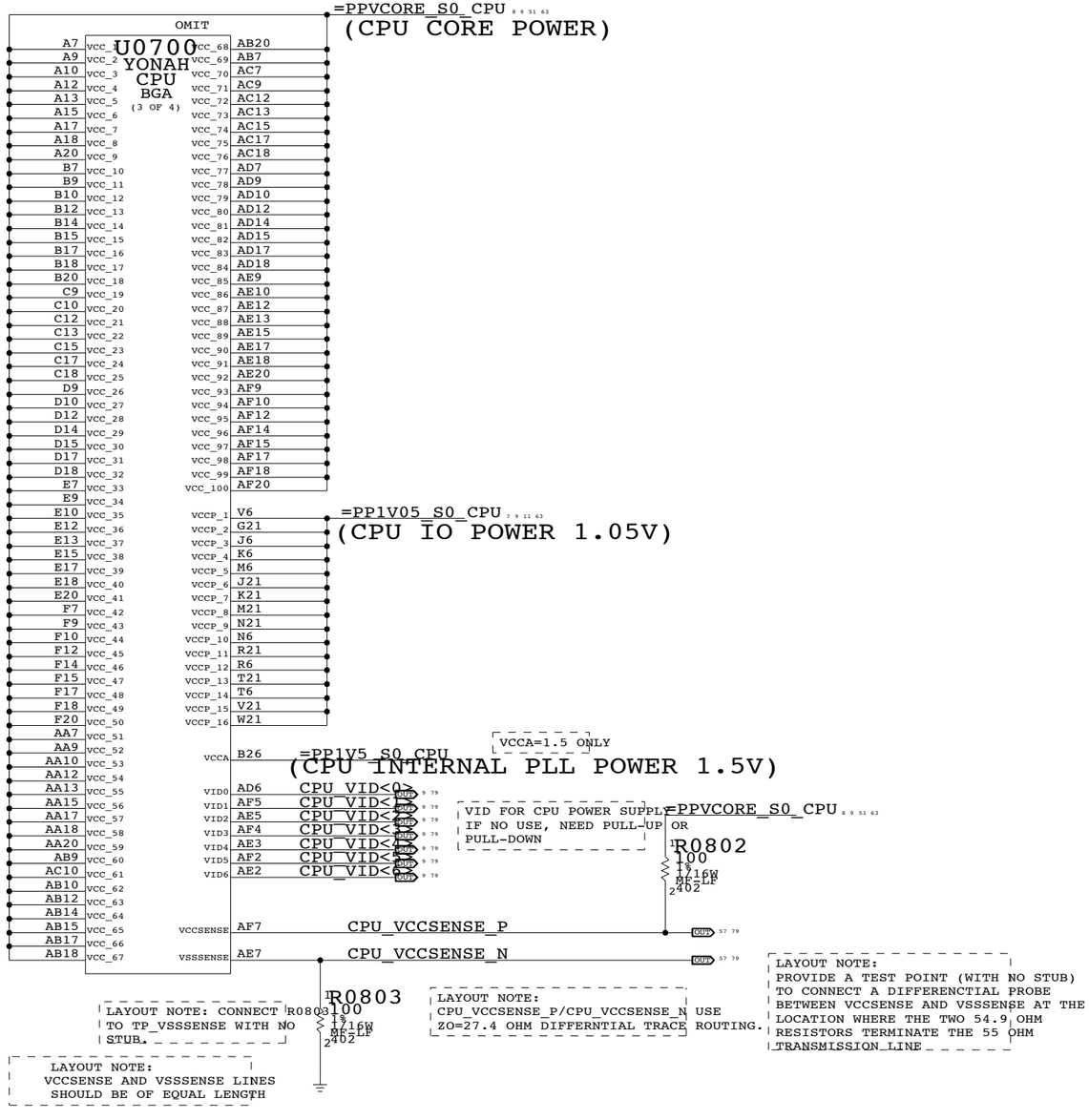
WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM*50
SO THE TDI PULL UP THROUGH 54.9 OHM,TMS PULL UP THROUGH 54.9 OHM
TCK PULL DOWN THROUGH 54.9 OHM(FOLLOW UP XDP DESIGN REFERENCE)

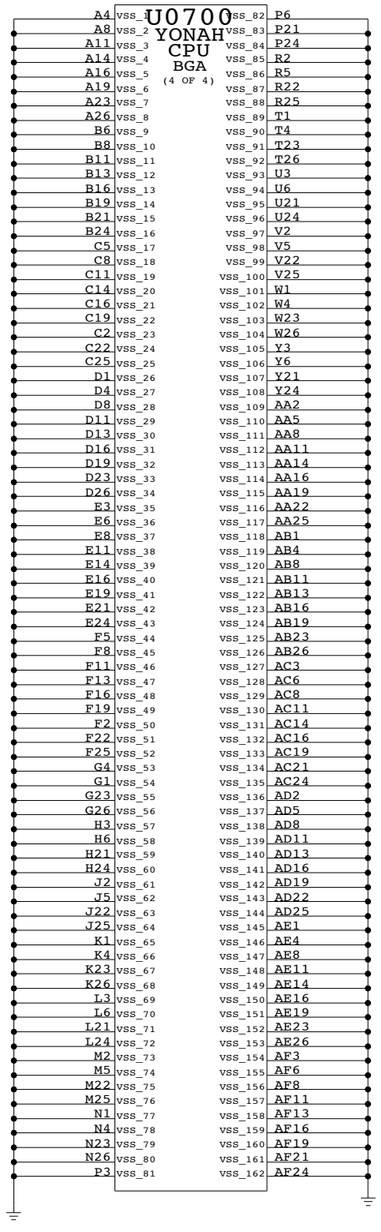
CPU 1 OF 2-FSB

SYNC_MASTER=M42 SYNC_DATE=11/16/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 7 OF 104	





CPU 2 OF 2-PWR/GND

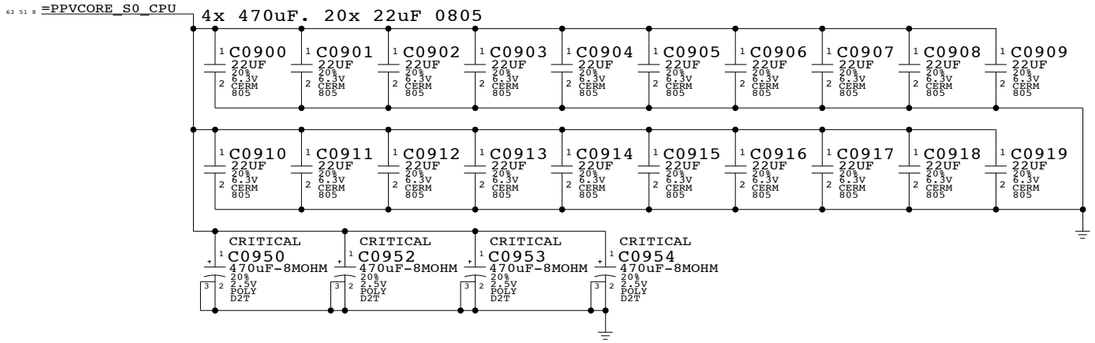
SYNC_MASTER=M42 SYNC_DATE=11/16/2005

APPLE COMPUTER INC.

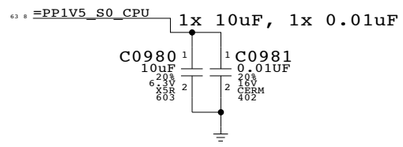
SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE NONE SHT 8 OF 104

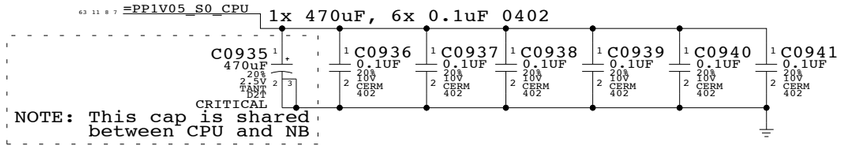
CPU VCORE HF AND BULK DECOUPLING



VCCA (CPU AVdd) Decoupling

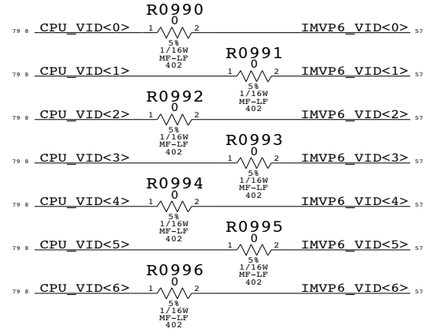


VCCP (CPU I/O) Decoupling



CPU VCORE VID Connections

Resistors to allow for override of CPU VID
Will probably be removed before production



CPU Decoupling & VID

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
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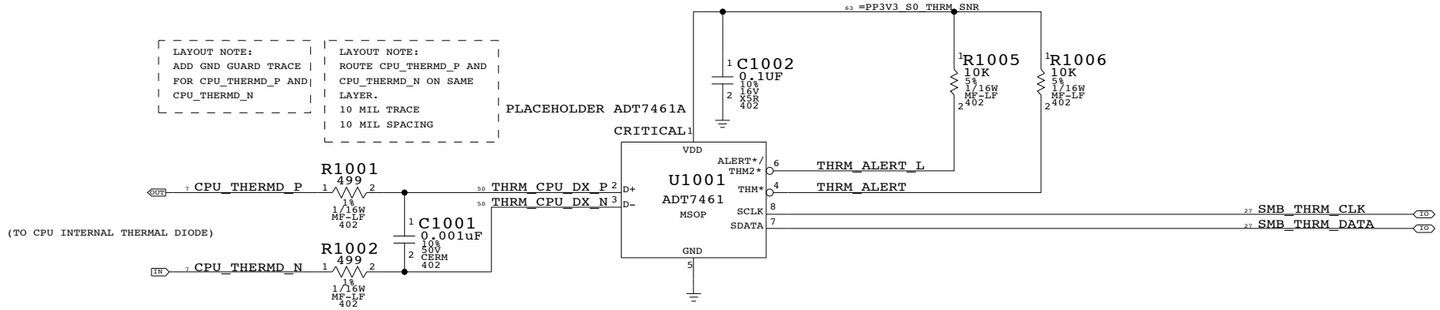
CPU ZONE THERMAL SENSOR



PLACE U1001 NEAR THE U1200

CPU MISC1-TEMP SENSOR

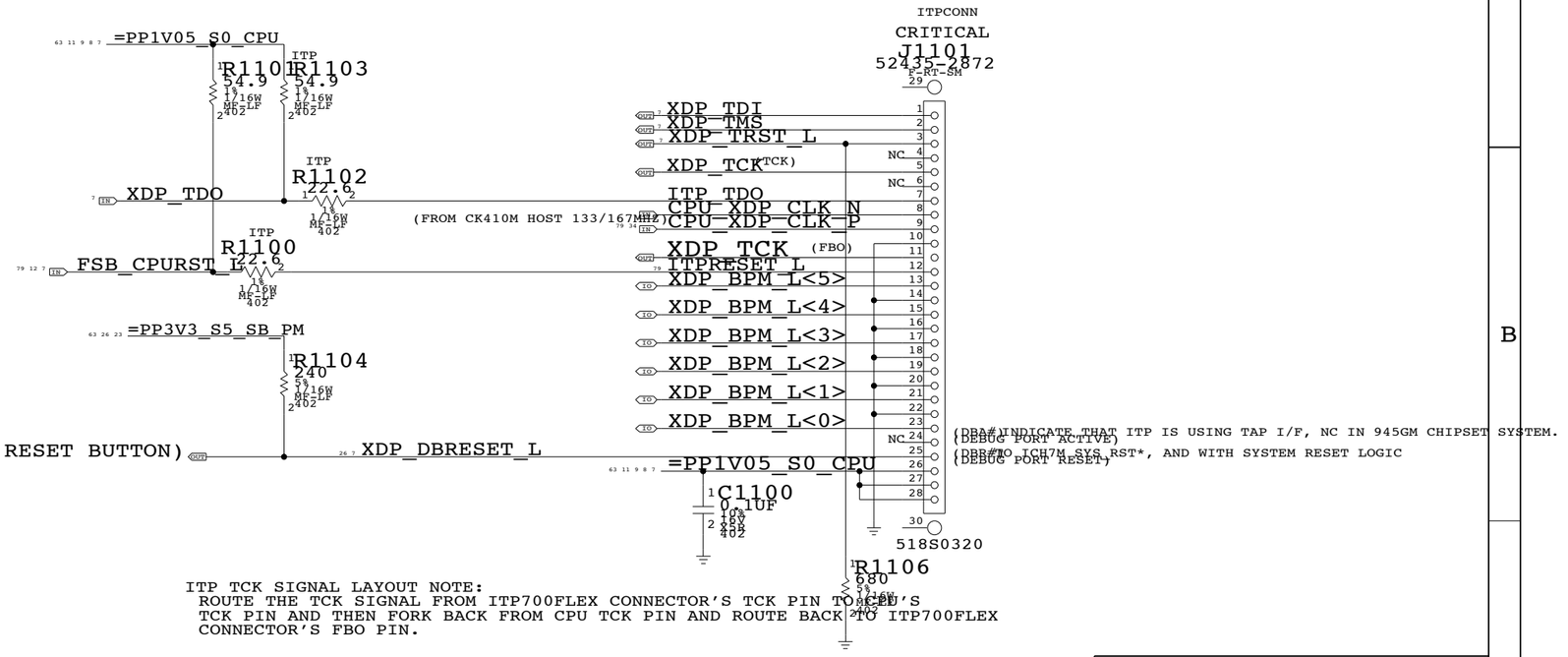
SYNC_MASTER=M42 SYNC_DATE=10/07/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	10	104

CPU ITP700FLEX DEBUG SUPPORT



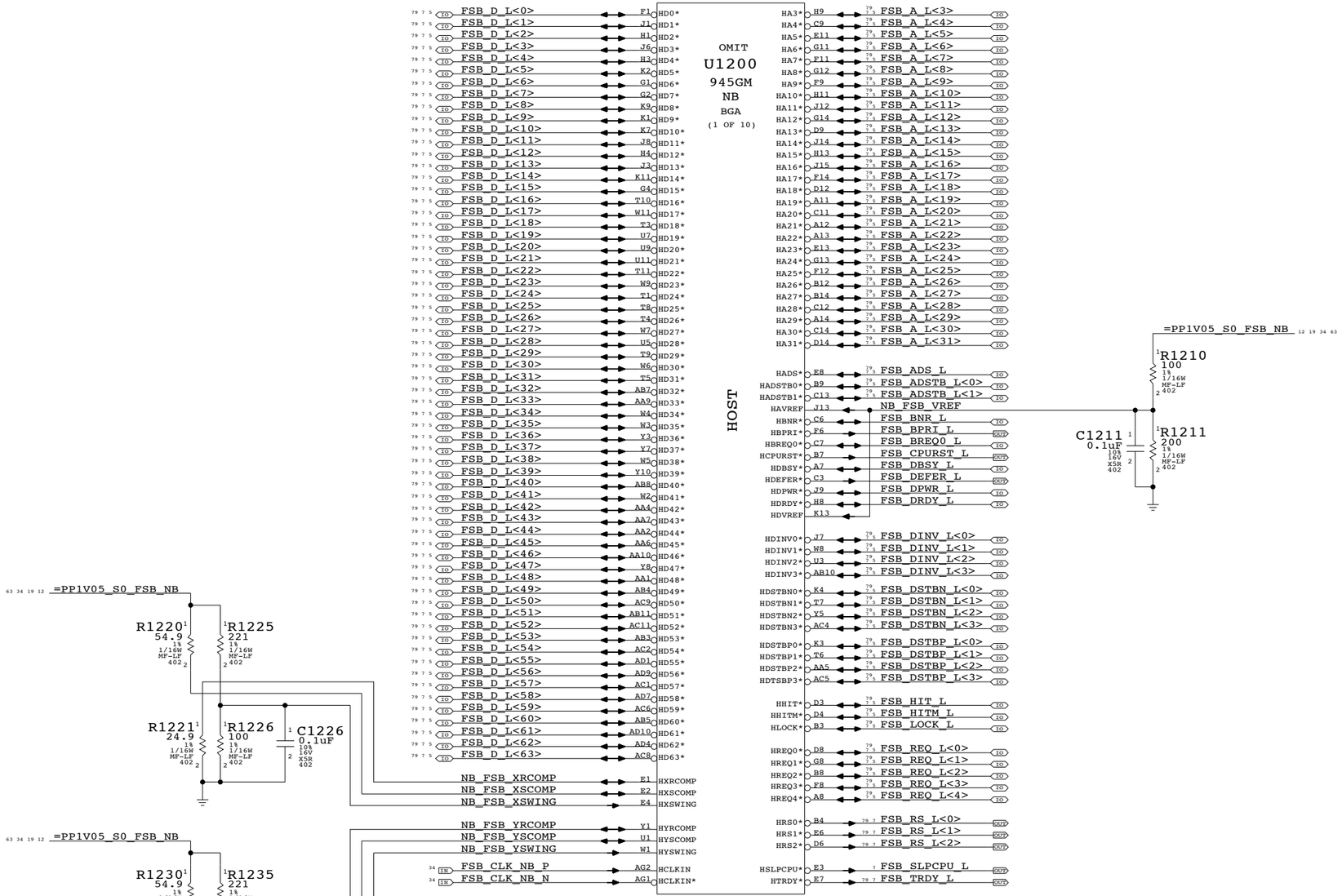
ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG

SYNC_MASTER=M52 SYNC_DATE=10/12/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 11 OF 104	



NB CPU Interface

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

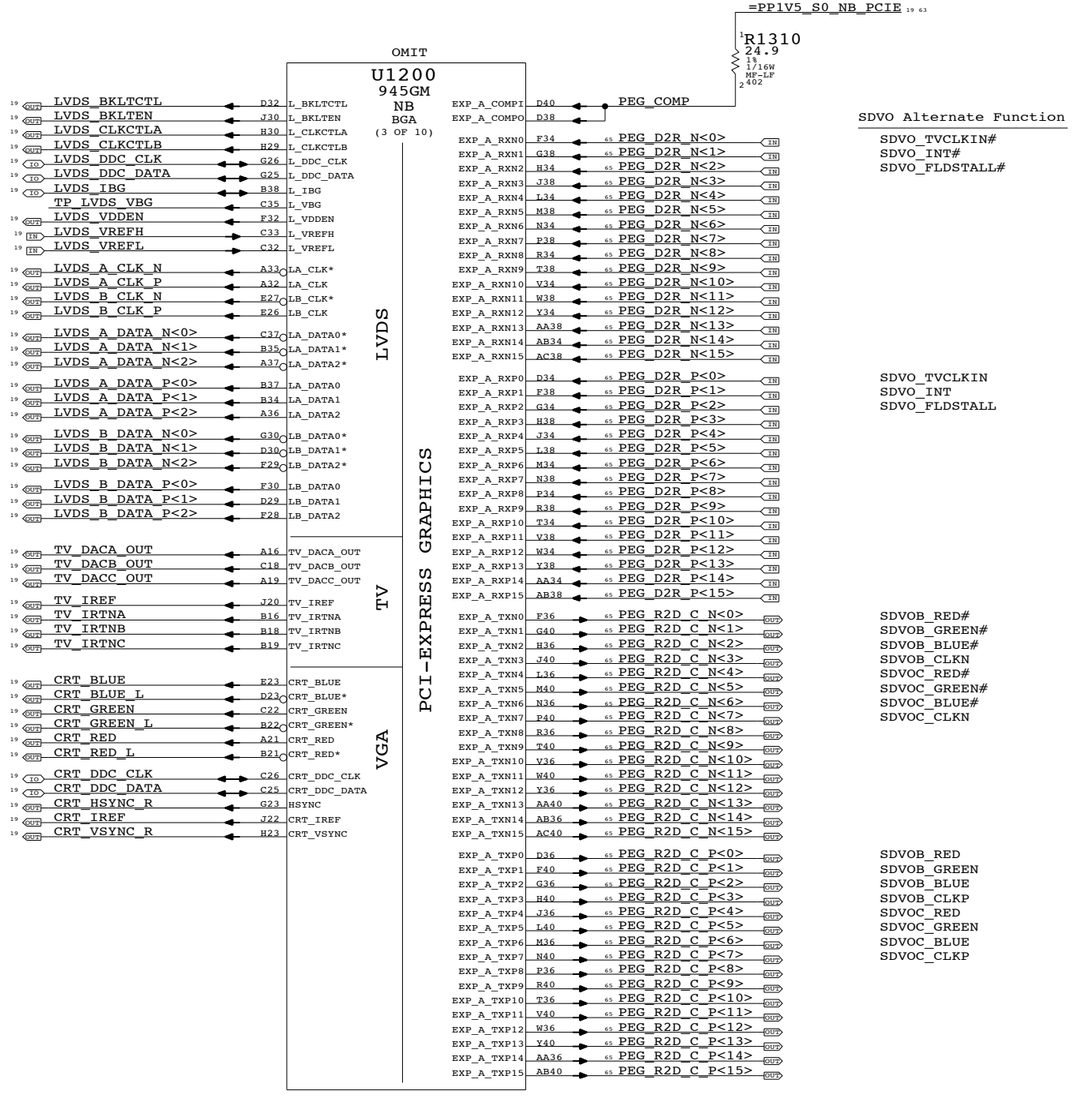
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.

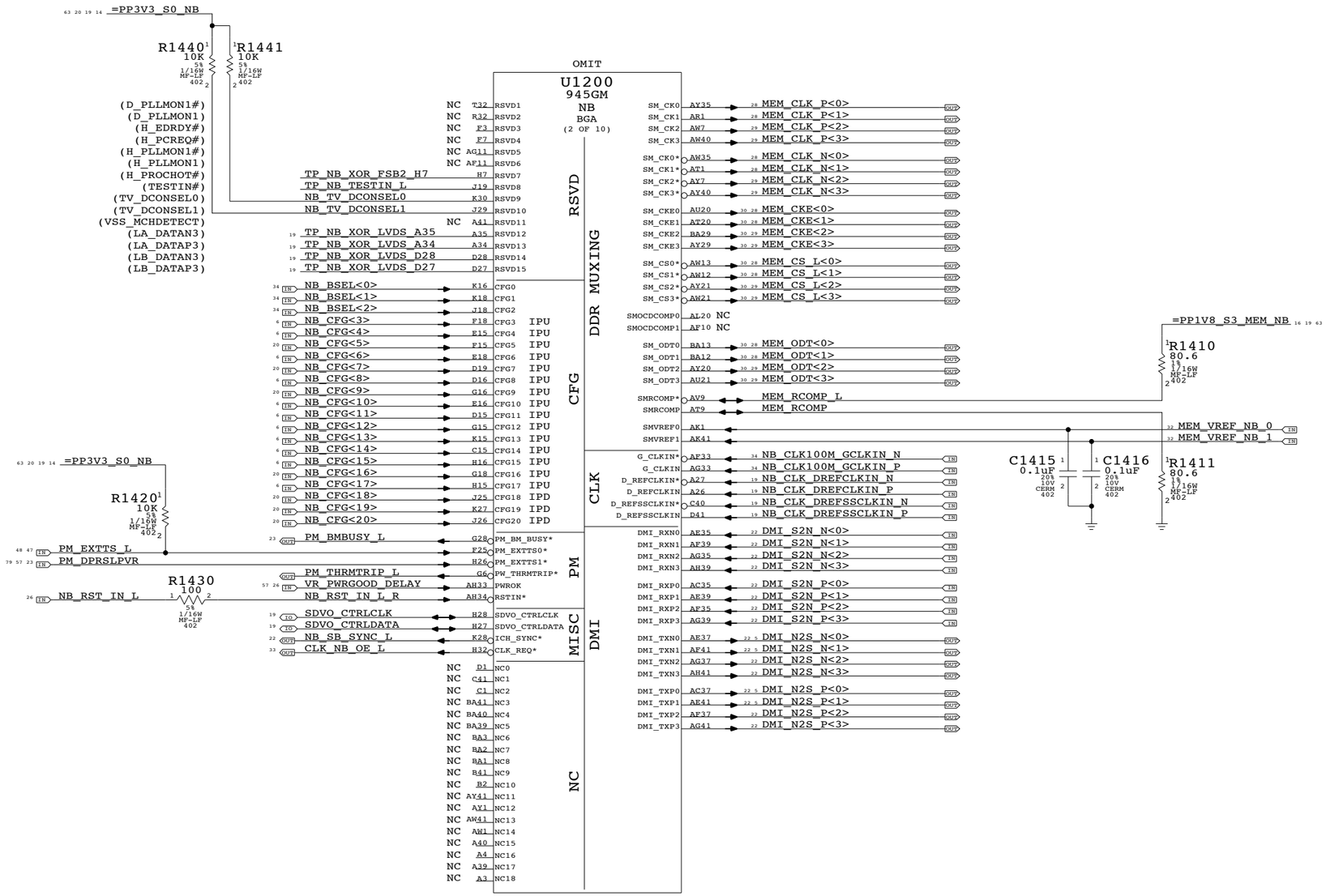


NB PEG / Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 13 OF 104	



NB Misc Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE: NONE

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OMIT

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NB
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DDR SYSTEM MEMORY A

MEM_A_DQ<0>	AJ35	SA_DQ0	SA_BS0	AU12	MEM_A_BS<0>
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MEM_A_DQ<4>	AJ36	SA_DQ4	SA_CAS*	AY13	MEM_A_CAS_L
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DDR SYSTEM MEMORY B

MEM_B_DQ<0>	AK39	SB_DQ0	SB_BS0	AT24	MEM_B_BS<0>
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MEM_B_DQ<4>	AJ38	SB_DQ4	SB_CAS*	AR24	MEM_B_CAS_L
MEM_B_DQ<5>	AK38	SB_DQ5	SB_DM0	AK36	MEM_B_DM<0>
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MEM_B_DQ<7>	AP41	SB_DQ7	SB_DM2	AT36	MEM_B_DM<2>
MEM_B_DQ<8>	AT40	SB_DQ8	SB_DM3	BA31	MEM_B_DM<3>
MEM_B_DQ<9>	AV41	SB_DQ9	SB_DM4	AL17	MEM_B_DM<4>
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MEM_B_DQ<12>	AP38	SB_DQ12	SB_DM7	AN4	MEM_B_DM<7>
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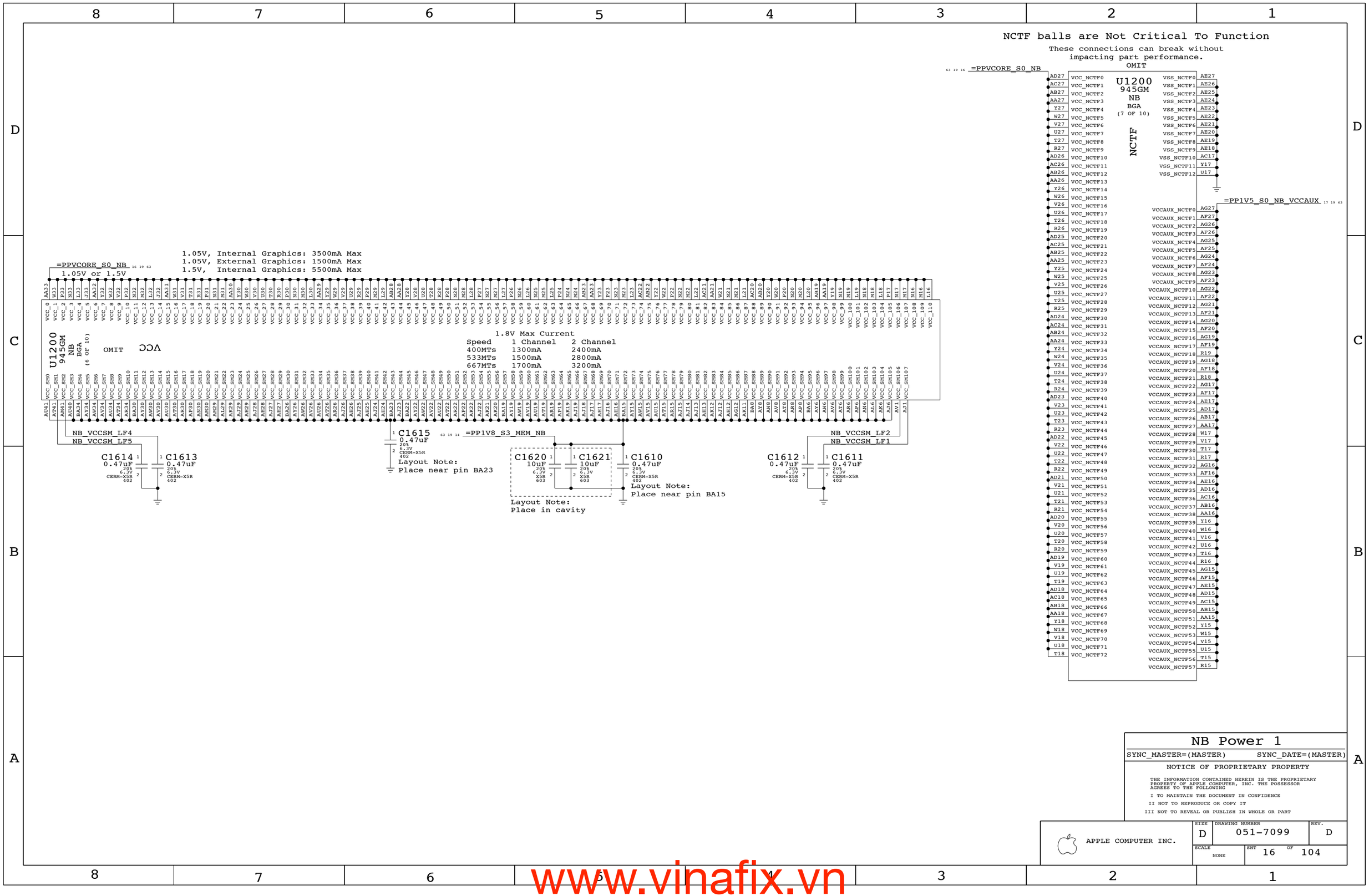
NB DDR2 Interfaces

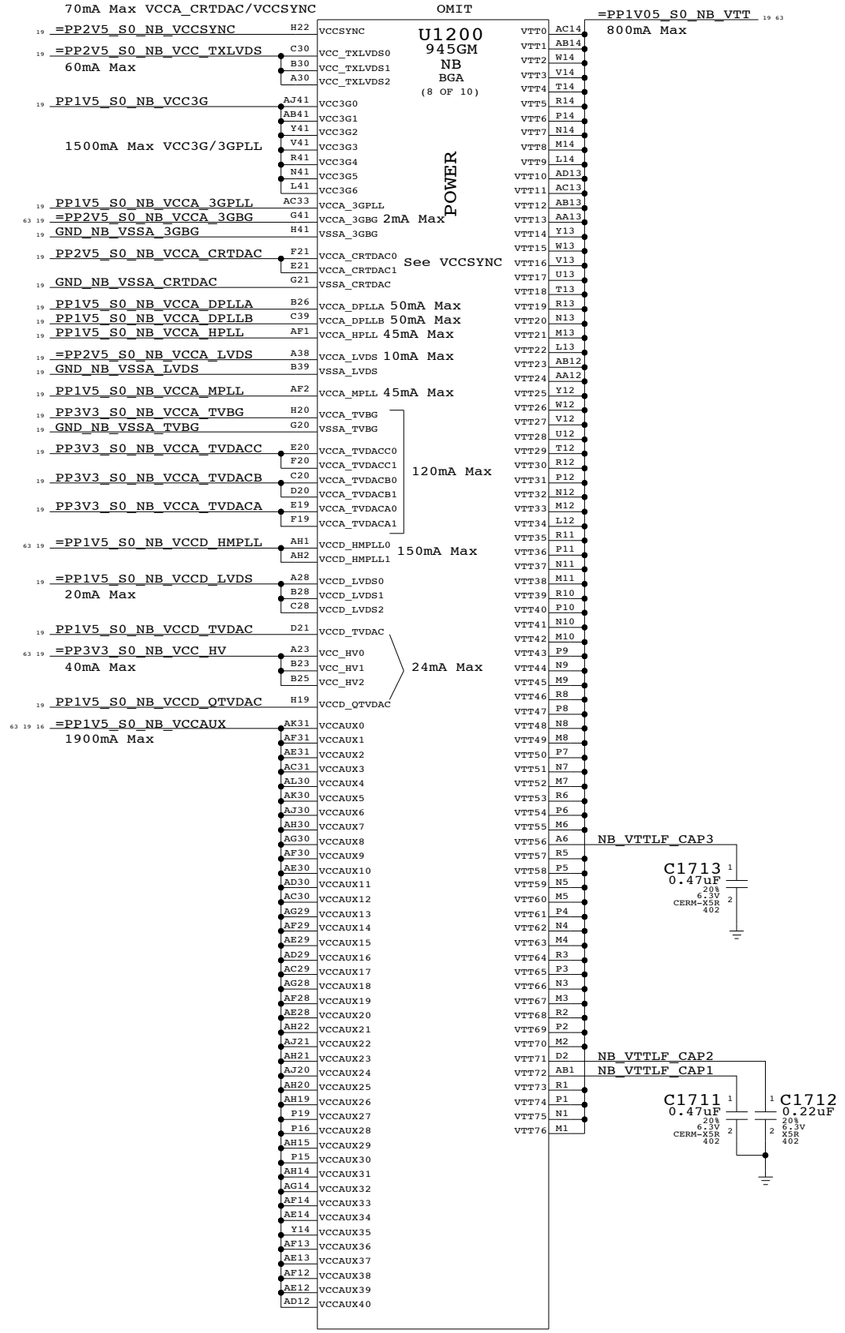
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	15	104





NB Power 2

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	17	104

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VSS

AC41	VSS_0	VSS_97	AK34
AA41	VSS_1	VSS_98	AG34
W41	VSS_2	VSS_99	AF34
T41	VSS_3	VSS_100	AE34
P41	VSS_4	VSS_101	AC34
M41	VSS_5	VSS_102	C34
J41	VSS_6	VSS_103	AW33
F41	VSS_7	VSS_104	AV33
AV40	VSS_8	VSS_105	AR33
AP40	VSS_9	VSS_106	AE33
AN40	VSS_10	VSS_107	AB33
AK40	VSS_11	VSS_108	Y33
AJ40	VSS_12	VSS_109	V33
AH40	VSS_13	VSS_110	T33
AG40	VSS_14	VSS_111	R33
AF40	VSS_15	VSS_112	M33
AE40	VSS_16	VSS_113	H33
B40	VSS_17	VSS_114	G33
AY39	VSS_18	VSS_115	F33
AW39	VSS_19	VSS_116	D33
AV39	VSS_20	VSS_117	B33
AR39	VSS_21	VSS_118	AH32
AN39	VSS_22	VSS_119	AG32
AJ39	VSS_23	VSS_120	AF32
AC39	VSS_24	VSS_121	AE32
AB39	VSS_25	VSS_122	AC32
AA39	VSS_26	VSS_123	AB32
Y39	VSS_27	VSS_124	G32
W39	VSS_28	VSS_125	B32
V39	VSS_29	VSS_126	AY31
T39	VSS_30	VSS_127	AV31
R39	VSS_31	VSS_128	AN31
P39	VSS_32	VSS_129	AJ31
N39	VSS_33	VSS_130	AG31
M39	VSS_34	VSS_131	AB31
L39	VSS_35	VSS_132	Y31
J39	VSS_36	VSS_133	AB30
H39	VSS_37	VSS_134	E30
G39	VSS_38	VSS_135	AT29
F39	VSS_39	VSS_136	AN29
D39	VSS_40	VSS_137	AB29
AT38	VSS_41	VSS_138	T29
AM38	VSS_42	VSS_139	N29
AH38	VSS_43	VSS_140	K29
AG38	VSS_44	VSS_141	G29
AF38	VSS_45	VSS_142	E29
AE38	VSS_46	VSS_143	C29
C38	VSS_47	VSS_144	B29
AK37	VSS_48	VSS_145	A29
AH37	VSS_49	VSS_146	BA28
AB37	VSS_50	VSS_147	AW28
AA37	VSS_51	VSS_148	AU28
Y37	VSS_52	VSS_149	AP28
W37	VSS_53	VSS_150	AM28
V37	VSS_54	VSS_151	AD28
T37	VSS_55	VSS_152	AC28
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P37	VSS_57	VSS_154	J28
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J37	VSS_61	VSS_158	AK27
H37	VSS_62	VSS_159	J27
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AG36	VSS_70	VSS_167	F26
AF36	VSS_71	VSS_168	D26
AE36	VSS_72	VSS_169	AK25
AC36	VSS_73	VSS_170	P25
C36	VSS_74	VSS_171	K25
B36	VSS_75	VSS_172	H25
BA35	VSS_76	VSS_173	E25
AV35	VSS_77	VSS_174	D25
AR35	VSS_78	VSS_175	A25
AH35	VSS_79	VSS_176	BA24
AB35	VSS_80	VSS_177	AU24
AA35	VSS_81	VSS_178	AL24
Y35	VSS_82	VSS_179	AW23
W35	VSS_83		
V35	VSS_84		
T35	VSS_85		
R35	VSS_86		
P35	VSS_87		
N35	VSS_88		
M35	VSS_89		
L35	VSS_90		
J35	VSS_91		
H35	VSS_92		
G35	VSS_93		
F35	VSS_94		
D35	VSS_95		
AN34	VSS_96		

OMIT

U1200
945GM
NB
BGA
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VSS

AT23	VSS_180	VSS_273	J11
AN23	VSS_181	VSS_274	D11
AM23	VSS_182	VSS_275	B11
AH23	VSS_183	VSS_276	AV10
AC23	VSS_184	VSS_277	AP10
W23	VSS_185	VSS_278	AL10
K23	VSS_186	VSS_279	AJ10
J23	VSS_187	VSS_280	AG10
F23	VSS_188	VSS_281	AC10
C23	VSS_189	VSS_282	W10
AA22	VSS_190	VSS_283	U10
K22	VSS_191	VSS_284	BA9
G22	VSS_192	VSS_285	AW9
F22	VSS_193	VSS_286	AR9
E22	VSS_194	VSS_287	AH9
D22	VSS_195	VSS_288	AB9
A22	VSS_196	VSS_289	Y9
BA21	VSS_197	VSS_290	R9
AV21	VSS_198	VSS_291	G9
AR21	VSS_199	VSS_292	E9
AN21	VSS_200	VSS_293	A9
AL21	VSS_201	VSS_294	AG8
AB21	VSS_202	VSS_295	AD8
Y21	VSS_203	VSS_296	AA8
P21	VSS_204	VSS_297	U8
K21	VSS_205	VSS_298	K8
J21	VSS_206	VSS_299	C8
H21	VSS_207	VSS_300	BA7
C21	VSS_208	VSS_301	AV7
AW20	VSS_209	VSS_302	AP7
AR20	VSS_210	VSS_303	AL7
AM20	VSS_211	VSS_304	AJ7
AA20	VSS_212	VSS_305	AH7
K20	VSS_213	VSS_306	AF7
B20	VSS_214	VSS_307	AC7
A20	VSS_215	VSS_308	R7
AN19	VSS_216	VSS_309	G7
AC19	VSS_217	VSS_310	D7
W19	VSS_218	VSS_311	AG6
K19	VSS_219	VSS_312	AD6
G19	VSS_220	VSS_313	AB6
C19	VSS_221	VSS_314	Y6
AH18	VSS_222	VSS_315	U6
P18	VSS_223	VSS_316	N6
H18	VSS_224	VSS_317	K6
D18	VSS_225	VSS_318	H6
A18	VSS_226	VSS_319	B6
AY17	VSS_227	VSS_320	AV5
AR17	VSS_228	VSS_321	AP5
AP17	VSS_229	VSS_322	AD5
AM17	VSS_230	VSS_323	AY4
AK17	VSS_231	VSS_324	AR4
AV16	VSS_232	VSS_325	AP4
AN16	VSS_233	VSS_326	AL4
AL16	VSS_234	VSS_327	AJ4
J16	VSS_235	VSS_328	Y4
F16	VSS_236	VSS_329	U4
C16	VSS_237	VSS_330	R4
AN15	VSS_238	VSS_331	J4
AM15	VSS_239	VSS_332	F4
AK15	VSS_240	VSS_333	C4
N15	VSS_241	VSS_334	AY3
M15	VSS_242	VSS_335	AW3
L15	VSS_243	VSS_336	AV3
B15	VSS_244	VSS_337	AL3
A15	VSS_245	VSS_338	AH3
BA14	VSS_246	VSS_339	AG3
AT14	VSS_247	VSS_340	AF3
AK14	VSS_248	VSS_341	AD3
AD14	VSS_249	VSS_342	AC3
AA14	VSS_250	VSS_343	AA3
U14	VSS_251	VSS_344	G3
K14	VSS_252	VSS_345	AT2
H14	VSS_253	VSS_346	AR2
E14	VSS_254	VSS_347	AP2
AV13	VSS_255	VSS_348	AK2
AR13	VSS_256	VSS_349	AJ2
AN13	VSS_257	VSS_350	AD2
AM13	VSS_258	VSS_351	AB2
AL13	VSS_259	VSS_352	Y2
AG13	VSS_260	VSS_353	U2
P13	VSS_261	VSS_354	T2
F13	VSS_262	VSS_355	N2
D13	VSS_263	VSS_356	J2
B13	VSS_264	VSS_357	H2
AY12	VSS_265	VSS_358	F2
AC12	VSS_266	VSS_359	C2
K12	VSS_267	VSS_360	AL1
H12	VSS_268		
E12	VSS_269		
AD11	VSS_270		
AA11	VSS_271		
Y11	VSS_272		

NB Grounds

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE NONE SHT 18 OF 104

Power Interface

These are the power signals that leave the NB "block"

Rail Totals:

2310mA Max?	IN	=PPVCORE_S0_NB	1500mA Max
	IN	=PP1V05_S0_FSB_NB	10mA Max?
	IN	=PP1V05_S0_NB_VTT	800mA Max
	IN	=PP1V05_S0_NB_CRT	?mA Max
3674mA Max	IN	=PP1V5_S0_NB	?mA Max
	IN	=PP1V5_S0_NB_3G	1500mA Max
	IN	=PP1V5_S0_NB_3GPLL	
	IN	=PP1V5_S0_NB_PCIE	?mA Max
	IN	=PP1V5_S0_NB_PLL	100mA Max
	IN	=PP1V5_S0_NB_TVDAC	24mA Max
	IN	=PP1V5_S0_NB_VCCD_HMPLL	150mA Max
	IN	=PP1V5_S0_NB_VCCAUX	1900mA Max
3200mA Max	IN	=PP1V8_S3_MEM_NB	3200mA Max
	IN	=PP2V5_S0_NB_VCCSYNC	70mA Max
132mA Max	IN	=PP2V5_S0_NB_VCC_TXLVDS	60mA Max
	IN	=PP2V5_S0_NB_VCCA_3GBG	2mA Max
	IN	=PP3V3_S0_NB	?mA Max
40mA Max?	IN	=PP3V3_S0_NB_VCC_HV	40mA Max

63 19 =PP1V05_S0_NB_CRT
- CRT_RED — 13
- CRT_GREEN — 13
- CRT_BLUE — 13
- CRT_RED_L — 13
- CRT_GREEN_L — 13
- CRT_BLUE_L — 13
- CRT_IREF — 13
- CRT_HSYNC_R — 13
- CRT_VSYNC_R — 13

TP_CRT_DDC_CLK (MAKE_BASE=TRUE) — CRT_DDC_CLK — 13

TP_CRT_DDC_DATA (MAKE_BASE=TRUE) — CRT_DDC_DATA — 13

63 19 =PP1V5_S0_NB_TVDAC
- TV_DACA_OUT — 13
- TV_DACB_OUT — 13
- TV_DACC_OUT — 13
- TV_IREF — 13
- TV_IRTNA — 13
- TV_IRTNB — 13
- TV_IRTNC — 13

TP_LVDS_BKLTCTL (MAKE_BASE=TRUE) — LVDS_BKLTCTL — 13

TP_LVDS_BKLTEN (MAKE_BASE=TRUE) — LVDS_BKLTEN — 13

TP_LVDS_CLKCTLA (MAKE_BASE=TRUE) — LVDS_CLKCTLA — 13

TP_LVDS_CLKCTLB (MAKE_BASE=TRUE) — LVDS_CLKCTLB — 13

TP_LVDS_DDC_CLK (MAKE_BASE=TRUE) — LVDS_DDC_CLK — 13

TP_LVDS_DDC_DATA (MAKE_BASE=TRUE) — LVDS_DDC_DATA — 13

NC_LVDS_IBG (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_IBG — 13

TP_LVDS_VDDEN (MAKE_BASE=TRUE) — LVDS_VDDEN — 13

NC_LVDS_VREFH (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_VREFH — 13

TP_LVDS_VREFL (MAKE_BASE=TRUE) — LVDS_VREFL — 13

NC_LVDS_A_CLKP (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_CLK_P — 13

NC_LVDS_A_CLKN (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_CLK_N — 13

NC_LVDS_A_DATAP<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_DATA_P<2..0> — 13

NC_LVDS_A_DATAN<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_DATA_N<2..0> — 13

NC_LVDS_B_CLKP (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_CLK_P — 13

NC_LVDS_B_CLKN (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_CLK_N — 13

NC_LVDS_B_DATAP<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_DATA_P<2..0> — 13

NC_LVDS_B_DATAN<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_DATA_N<2..0> — 13

NC_NB_XOR_LVDS_A34 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_A34 — 14

NC_NB_XOR_LVDS_A35 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_A35 — 14

NC_NB_XOR_LVDS_D27 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_D27 — 14

NC_NB_XOR_LVDS_D28 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_D28 — 14

TP_SDVO_CTRLCLK (MAKE_BASE=TRUE) — SDVO_CTRLCLK — 14

TP_SDVO_CTRLDATA (MAKE_BASE=TRUE) — SDVO_CTRLDATA — 14

(MCH LVDS DATA/CLK TX 2.5V PWR)
=PP2V5_S0_NB_VCC_TXLVDS — 17 19

(MCH LVDS DIGITAL 1.5V PWR)
=PP1V5_S0_NB_VCCD_LVDS — 17

(MCH LVDS ANALOG 2.5V PWR)
=PP2V5_S0_NB_VCCA_LVDS — 17

NC_GND_NB_VSSA_LVDS (MAKE_BASE=TRUE NO_TEST=TRUE) — GND_NB_VSSA_LVDS — 17

63 19 16 =PPVCORE_S0_NB

(MCH CRTDAC ANALOG 2.5V PWR)
PP2V5_S0_NB_VCCA_CRTDAC — 17

GND_NB_VSSA_CRTDAC — 17

(MCH H/V SYNC 2.5V PWR)
=PP2V5_S0_NB_VCCSYNC — 17 19

63 19 =PP1V5_S0_NB_TVDAC

(MCH TVDAC DEDICATED PWR 1.5V)
PP1V5_S0_NB_VCCD_TVDAC — 17

(MCH TVDAC DIGITAL QUIET 1.5V PWR)
PP1V5_S0_NB_VCCD_QTVDAC — 17

(MCH TV OUT CHANNEL A 3.3V PWR)
PP3V3_S0_NB_VCCA_TVDACA — 17

(MCH TV OUT CHANNEL B 3.3V PWR)
PP3V3_S0_NB_VCCA_TVDACB — 17

(MCH TV OUT CHANNEL C 3.3V PWR)
PP3V3_S0_NB_VCCA_TVDACC — 17

(MCH TV DAC BAND GAP 3.3V PWR)
PP3V3_S0_NB_VCCA_TVBG — 17

GND_NB_VSSA_TVBG — 17

(MCH DISPLAY A PLL 1.5V PWR)
TP_NB_VCCA_DPLLA (MAKE_BASE=TRUE) — PP1V5_S0_NB_VCCA_DPLLA — 17

(MCH DISPLAY B PLL 1.5V PWR)
TP_NB_VCCA_DPLLB (MAKE_BASE=TRUE) — PP1V5_S0_NB_VCCA_DPLLB — 17

NB_CLK_DREFCLKIN_P — 14

NB_CLK_DREFCLKIN_N — 14

NB_CLK_DREFSSCLKIN_P — 14

NB_CLK_DREFSSCLKIN_N — 14

63 19 16 =PPVCORE_S0_NB, 1500mA Max

GMCH CORE PWR 1.05V BYPASS

CRITICAL
C1900 470uF 20% 2.5V TANT D2T

C1902 10uF 20% 6.3V X5R 603

C1903 10uF 20% 6.3V X5R 603

C1904 1uF 10% 6.3V CERM 402

C1905 0.22uF 20% 6.3V X5R 402

C1906 0.22uF 20% 6.3V X5R 402

C1907 0.22uF 20% 6.3V X5R 402

63 19 17 =PP1V05_S0_NB_VTT, 800mA Max

MCH VTT BYPASS
(MCH FSB 1.05V PWR)

C1965 4.7uF 20% 6.3V CERM 603

C1966 2.2uF 20% 6.3V CERM1 603

Layout Note: Place in cavity

(SHARE C0940 470UF)

C1967 0.22uF 20% 6.3V X5R 402

Layout Note: Place on the edge

63 19 17 =PP3V3_S0_NB_VCC_HV, 40mA Max

MCH VCC_HV BYPASS
(MCH HV BUFFER 3.3V PWR)

C1914 10uF 20% 6.3V X5R 603

C1915 0.1uF 10% 10V CERM 402

63 19 17 =PP2V5_S0_NB_VCCA_3GBG, 2mA Max

MCH VCCA_3GBG BYPASS
(MCH PCIE/DMI BAND GAP 2.5V PWR)

C1916 0.1uF 20% 10V CERM 402

63 19 17 16 =PP1V5_S0_NB_VCCAUX, 1900mA Max

GMCH VCCAUX FILTER
(MCH DDR DLL&IO, FSB HSIO&IO PWR 1.5V)

C1918 0.1uF 20% 10V CERM 402

63 19 =PP1V5_S0_NB_PLL, 100mA Max

L1934 FERR-120-OHM-0.2A 0603

GMCH VCCA_HPLL FILTER
(HOST PLL 1.5V PWR)

PP1V5_S0_NB_VCCA_HPLL — 17
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
45mA Max

C1934 22UF 20% 6.3V CERM 805

C1935 0.1uF 20% 10V CERM 402

L1936 FERR-120-OHM-0.2A 0603

GMCH VCCA_MPLL FILTER
(MCH MEMORY PLL 1.5V PWR)

PP1V5_S0_NB_VCCA_MPLL — 17
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
45mA Max

C1936 22UF 20% 6.3V CERM 805

C1937 0.1uF 20% 10V CERM 402

1500mA Max

63 19 =PP1V5_S0_NB_3G

L1970 91nH 1210

Layout Note: Place L and C close to MCH

C1970 220UF 20% 2.5V POLY SMB2

GMCH VCC3G FILTER
(PCI-E/DMI ANALOG 1.5V PWR)

C1971 10uF 20% 6.3V X5R 603

C1972 10uF 20% 6.3V X5R 603

PP1V5_S0_NB_VCC3G — 17
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V

Layout Note: 10uF caps should be close to MCH on opposite side.

1500mA Max

63 19 =PP1V5_S0_NB_3GPLL, 1.0UH-220MA-0.12-OHM

L1975 0805

PP1V5_S0_NB_3GPLL_F
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=1.5V

R1975 0.51 1% 1/16W MF-LF 402

GMCH VCCA_3GPLL FILTER
(3GIO PLL 1.5V PWR)

PP1V5_S0_NB_VCCA_3GPLL — 17
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V

C1975 10uF 20% 6.3V X5R 603

C1976 0.1uF 20% 10V CERM 402

GND_NB_VSSA_3GBG — 17

Layout Note: 3GPLL 10uF cap should be placed in cavity

Layout Note: Route to caps, then GND

NB (GM) Decoupling

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 19 OF 104	

NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14 NB_CFG<5>
Internal pull-up

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

NBCFG_DMI_X2
R2075
2.2K
5%
1/16W
MF-LF
402

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14 NB_CFG<7>
Internal pull-up

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NO STUFF
R2077
2.2K
5%
1/16W
MF-LF
402

NB_CFG<8>	RESERVED

14 NB_CFG<9>
Internal pull-up

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NBCFG_PEG_REVERSE
R2079
2.2K
5%
1/16W
MF-LF
402

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14 NB_CFG<16>
Internal pull-up

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NBCFG_DYN_ODT_DISABLE
R2085
2.2K
5%
1/16W
MF-LF
402

NB_CFG<17>	RESERVED

=PP3V3_S0_NB 14 19 20 63
NBCFG_VCC_1V5
R2058
2.2K
5%
1/16W
MF-LF
402

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

14 NB_CFG<18>
Internal pull-down

=PP3V3_S0_NB 14 19 20 63
NBCFG_DMI_REVERSE
R2059
2.2K
5%
1/16W
MF-LF
402

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

14 NB_CFG<19>
Internal pull-down

945 External Design Spec says reserved

=PP3V3_S0_NB 14 19 20 63
NBCFG_SDVO_AND_PCIE
R2060
2.2K
5%
1/16W
MF-LF
402

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

14 NB_CFG<20>
Internal pull-down

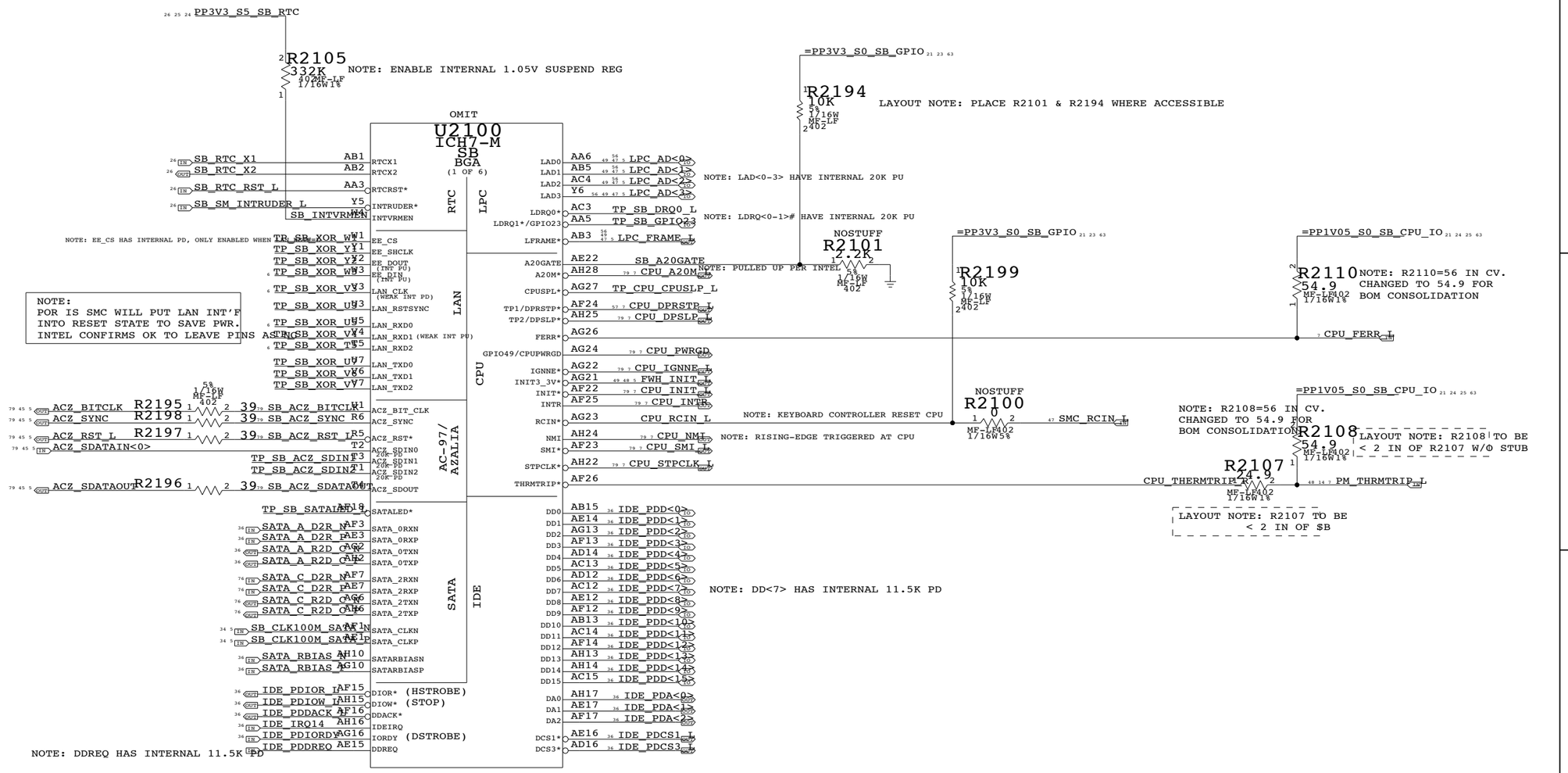
PROBABLY NOT NEEDED

NB Config Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 20 OF 104	



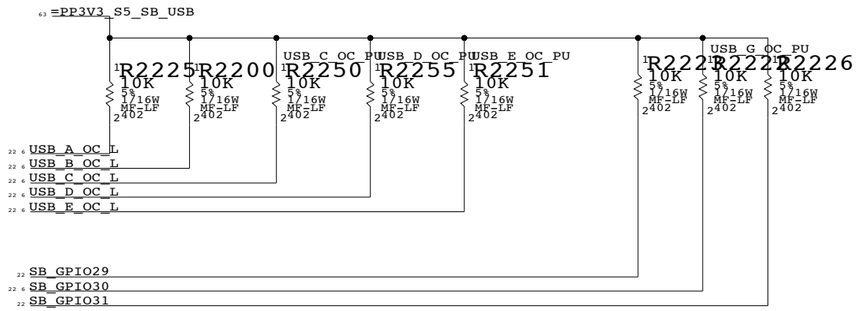
	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#	- LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

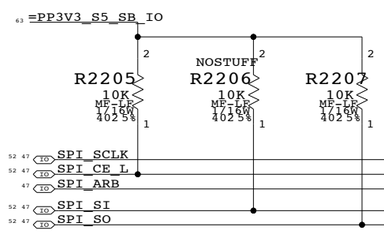
SB: 1 OF 4

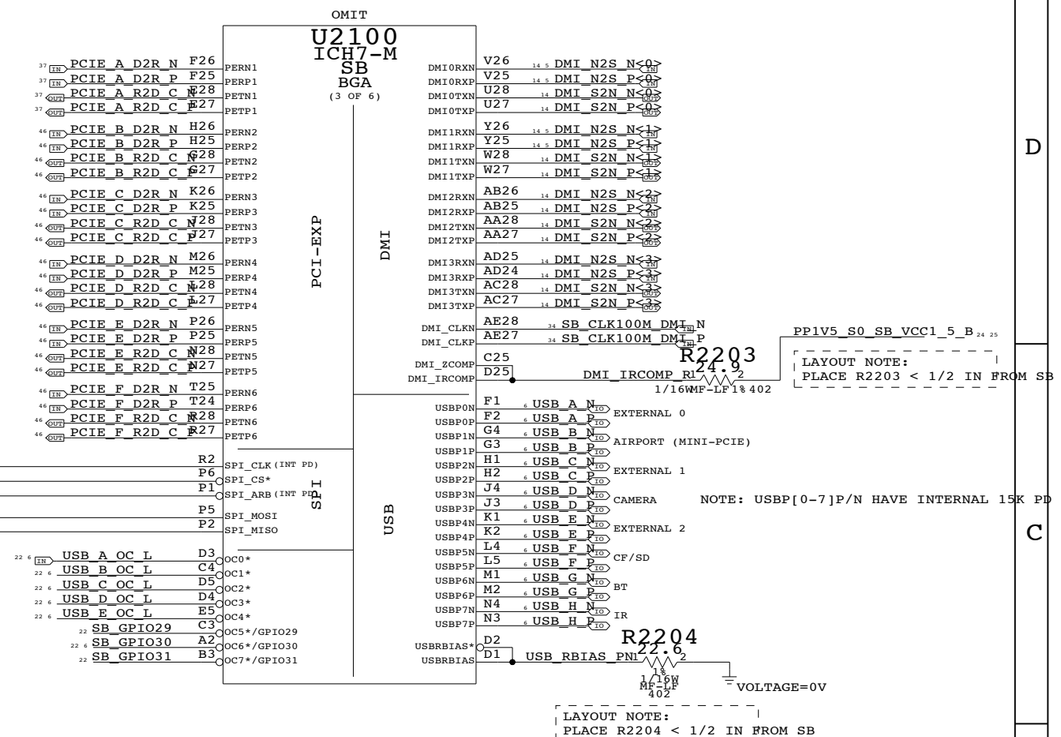
SYNC_MASTER=M38 SYNC_DATE=11/16/2005

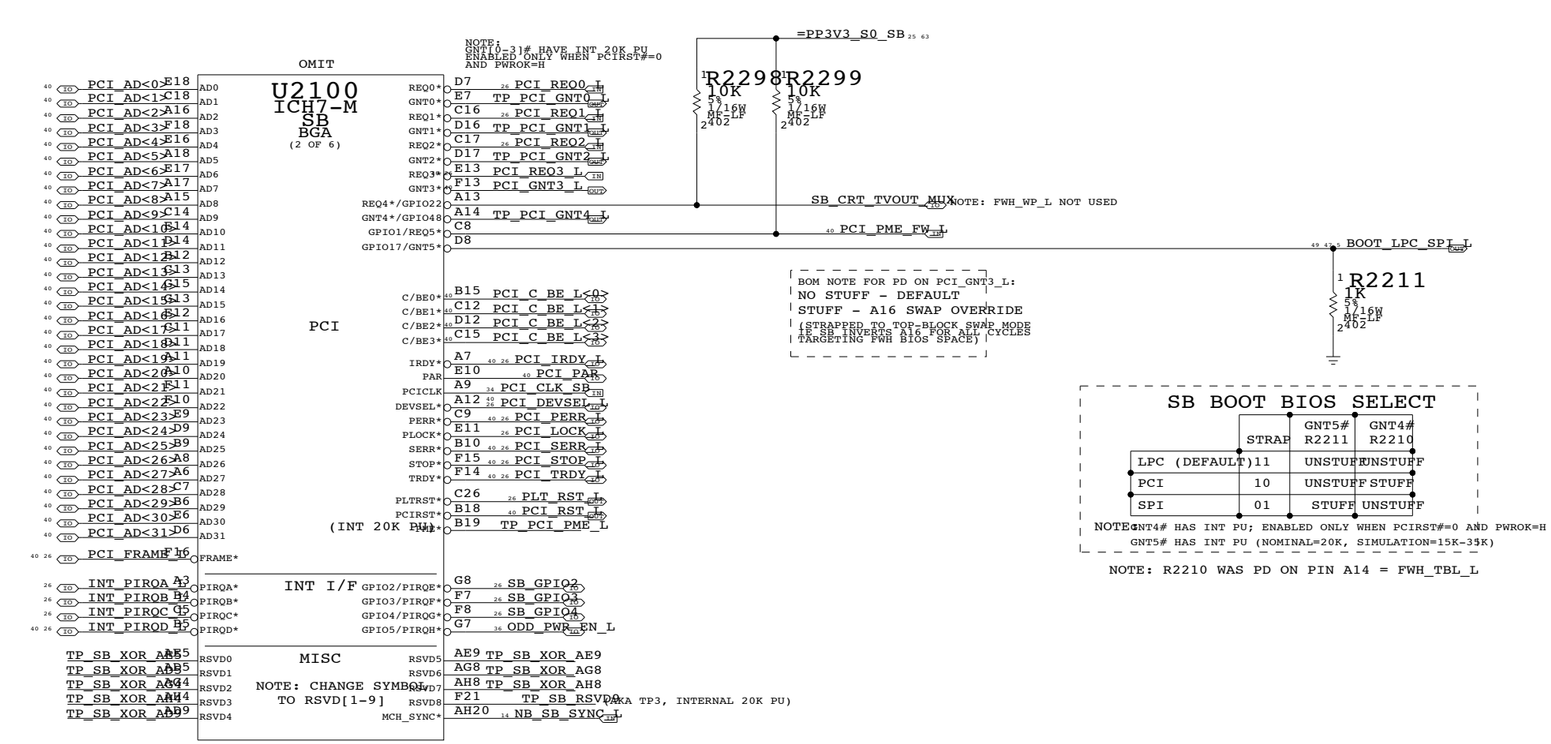
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 21 OF 104	









SB BOOT BIOS SELECT

STRAP	GNT5# R2211	GNT4# R2210
LPC (DEFAULT)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

NOTE: GNT4# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
GNT5# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)

NOTE: R2210 WAS PD ON PIN A14 = FWH_TBL_L

SB: 2 OF 4

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE: NONE | SHT 22 OF 104

NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING 1 PWROK_RISING:
SB WILL DISABLE TCO TIMER
SO SYSTEM WILL ENABLE
SYSTEM REBOOT FEATURE

=PP3V3_S0_SB_GPIO 21 23 63

=PP3V3_S5_SB 23 25 63

R2318 10K 5% 1/16W 402 2MF-LF
R2395 8.2K 5% 1/16W 402 2MF-LF
R2396 10K 5% 1/16W 402 2MF-LF
R2397 8.2K 5% 1/16W 402 2MF-LF
R2327 10K 5% 1/16W 402 2MF-LF
R2326 10K 5% 1/16W 402 2MF-LF
R2323 1K 5% 1/16W 402 2MF-LF
NOSTUFF NOSTUFF NO_REBOOT_MODE

RP2300 10K 5% 1/16W 8M-LF

63 25 23 =PP3V3_S5_SB

R2398 1K 5% 1/16W 402 2MF-LF
R2320 10K 5% 1/16W 402 2MF-LF
R2317 10K 5% 1/16W 402 2MF-LF
R2316 10K 5% 1/16W 402 2MF-LF

OMIT

U2100
ICH7-M
SB
BGA
(4 OF 6)

SMB

27 IO SMB_CLK	C22	SMBCLK
27 IO SMB_DATA	B22	SMBDATA
SMB_LINK_ALERT_L	A26	SMLINKALERT*
SMLINK<0>	B25	SMLINK0
NOT USED	SMLINK<1>	A25 SMLINK1
PM_RI_L	A28	RI*
SB_SPKR	A19	SPKR (INT WEAK PD)
56 49 48 47 5 OUT PM_SUS_STAT_L	A27	SUS_STAT*
47 26 5 IN PM_SYSRST_L	A22	SYS_RST*
14 IN PM_BMBUSY_L	AB18	GPIO0/BM_BUSY*
SMB_ALERT_L	B23	GPIO11/SMBALERT*
NOTE: RESERVED FOR FUTURE	AC20	GPIO18/STPPCI*
33 OUT PM_STPPCI_L	AF21	GPIO20/STPPCU*
34 OUT PM_STPCPU_L	A21	GPIO26
SB_GPIO26	B21	GPIO27
23 BIOS_REC	E23	GPIO28
23 FWH_MFG_MODE	AG18	GPIO32/CLKRUN*
56 49 47 40 5 IO PM_CLKRUN_L	AG19	GPIO33/AZ_DOCK_EN*
TP_AZ_DOCK_EN_L	AD22	GPIO34/AZ_DOCK_RST*
TP_AZ_DOCK_RST_L	F20	WAKE*
RESERVED FOR MOBILE AZALIA DOCKING INTF	AH21	SERIRQ
45 37 5 IN PCIE_WAKE_L	AF20	THRM*
56 49 47 5 IO INT_SERIRQ	AD21	VRMPWRGD
47 IN PM_THRM_L	AC21	GPIO6
26 IN VR_PWRGD_CK410	AC18	GPIO7
IO TP_SB_GPIO6	E21	GPIO8
47 IN SMC_RUNTIME_SCI_L		
47 IN SMC_EXTSMI_L		

SYS GPIO

CLKS

CLK14	AC1	34 SB_CLK14P3M_TIMER
CLK48	B2	34 SB_CLK48M_USBCTLR
SUSCLK	C20	6 SUS_CLK_SB

PWR MNGT

SLP_S3*	B24	62 47 41 PM_SLP_S3_L
SLP_S4*	D23	62 47 39 PM_SLP_S4_L
SLP_S5*	F22	48 47 PM_SLP_S5_L
PWROK	AA4	26 PM_SB_PWROK
GPIO16/DPRSLPVR	AC22	79 57 14 PM_DPRSLPVR
TP0/BATLOW*	C21	NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN
(INT 20K PU) PWRBTN*	C23	47 PM_PWRBTN_L
LAN_RST*	C19	47 PM_LAN_ENABLE
RSMRST*	Y4	NOTE: SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F IN RESET STATE TO SAVE PWR

GPIO

GPIO9	E20	48 47 SMS_INT_L
GPIO10	A20	47 SMC_SB_NMI
DEF=GPI GPIO12	F19	23 PATA_PWR_EN_L
GPIO13	E19	
DEF=GPI GPIO14	R4	36 IDE_RESET_L
GPIO15	E22	SV_SET_UP 5 23 49
GPIO24	R3	CRB_SV_DET 23
GPIO25	D20	TP_SB_GPIO25_DO_NOT_USE
OD GPIO35	AD21	33 SB_CLK100M_SATA_OE_L
GPIO38	AD20	TP_SB_GPIO38
DEF=GPI GPIO39	AE20	23 SATA_C_PWR_EN_L

SATA GPIO

GPIO21/SATA0GP	AF19	SB_GPIO21
GPIO19/SATA1GP	AH18	SB_GPIO19
GPIO36/SATA2GP	AH19	
GPIO37/SATA3GP	AE19	SB_GPIO37

R2302 100K 5% 1/16W 402 2MF-LF
R2303 100K 5% 1/16W 402 2MF-LF
R2305 100K 5% 1/16W 402 2MF-LF

36 SATA_C_DET_L

=PP3V3_S5_SB_PM 11 26 63

R2319 10K 5% 1/16W 402 2MF-LF
R2343 8.2K 5% 1/16W 402 2MF-LF

47 PM_BATLOW_L

42 PM_RSMRST_L

R2399 100K 5% 1/16W 402 2MF-LF

47 SMC_WAKE_SCI_L

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

63 25 23 =PP3V3_S5_SB

R2306 10K 5% 1/16W 402 2MF-LF
R2308 10K 5% 1/16W 402 2MF-LF

SV_SET_UP 5 23 49
CRB_SV_DET 23

R2307 10K 5% 1/16W 402 2MF-LF
R2309 0 5% 1/16W 402 2MF-LF

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

63 25 23 =PP3V3_S5_SB

R2313 10K 5% 1/16W 402 2MF-LF
R2310 10K 5% 1/16W 402 2MF-LF

FWH_MFG_MODE 23
BIOS_REC 23

R2314 0 5% 1/16W 402 2MF-LF
R2311 10K 5% 1/16W 402 2MF-LF

=PP3V3_S5_SB 23 25 63

R2390 10K 5% 1/16W 402 2MF-LF

23 PATA_PWR_EN_L

=PP3V3_S0_SB_GPIO 21 23 63

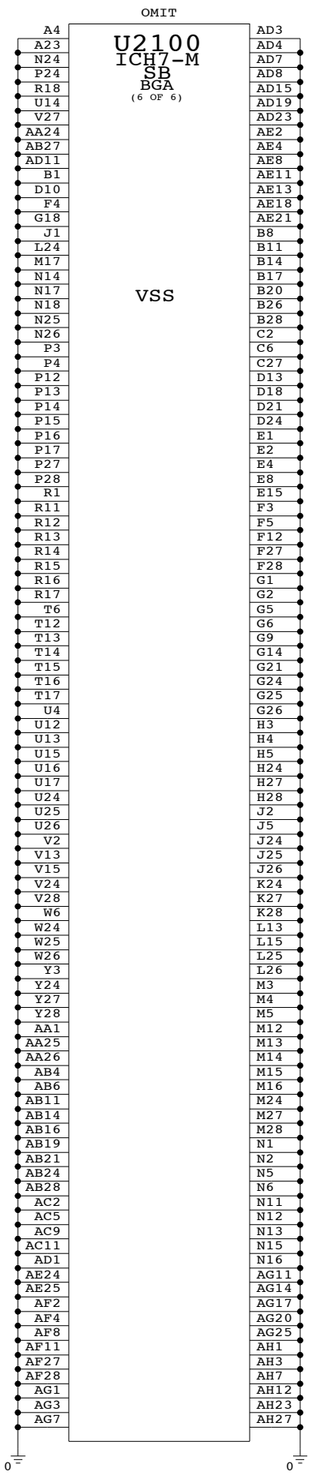
R2388 10K 5% 1/16W 402 2MF-LF

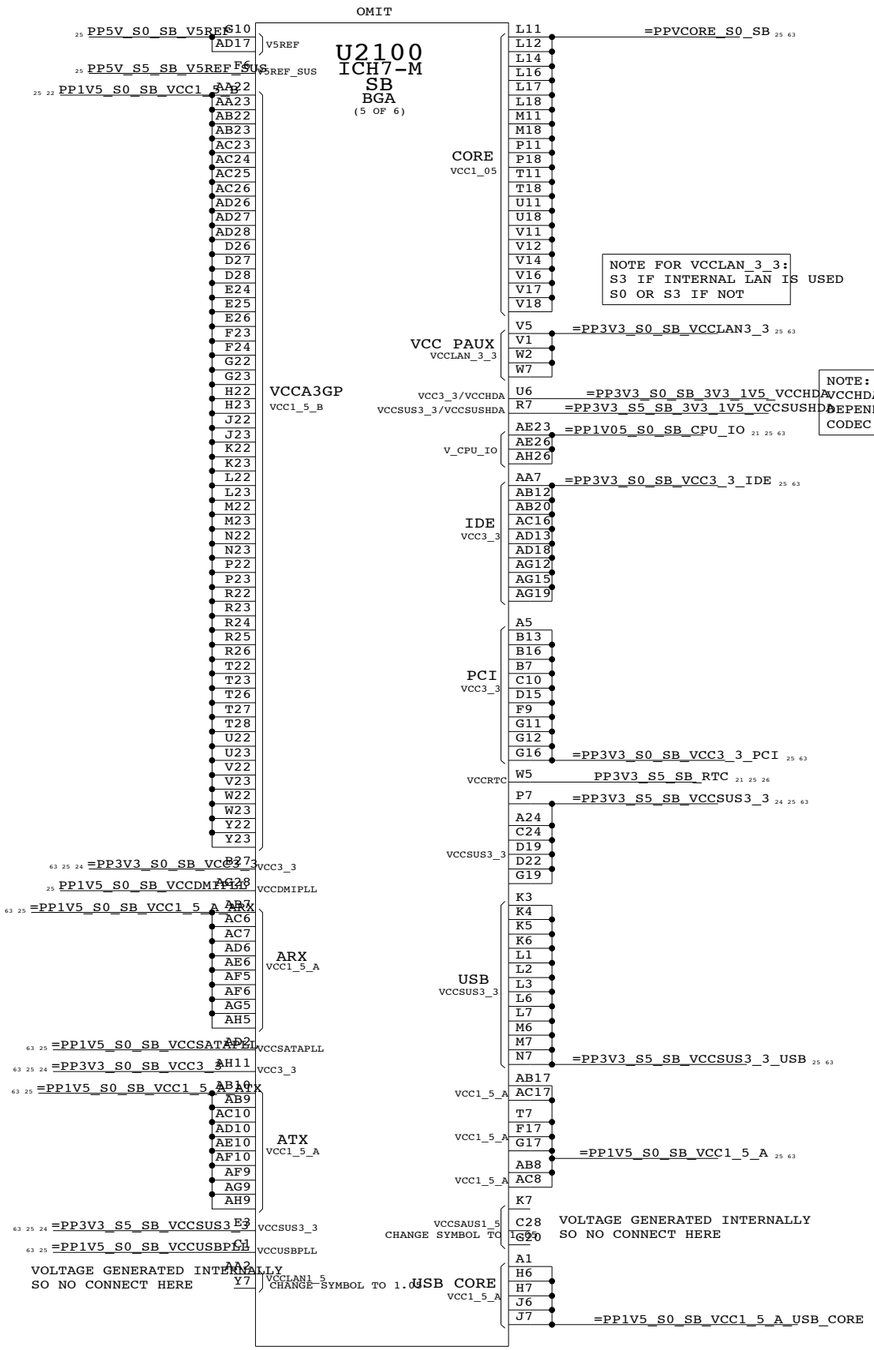
23 SATA_C_PWR_EN_L

SB: 3 OF 4
SYNC_MASTER=M38 SYNC_DATE=11/16/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 23 OF 104	





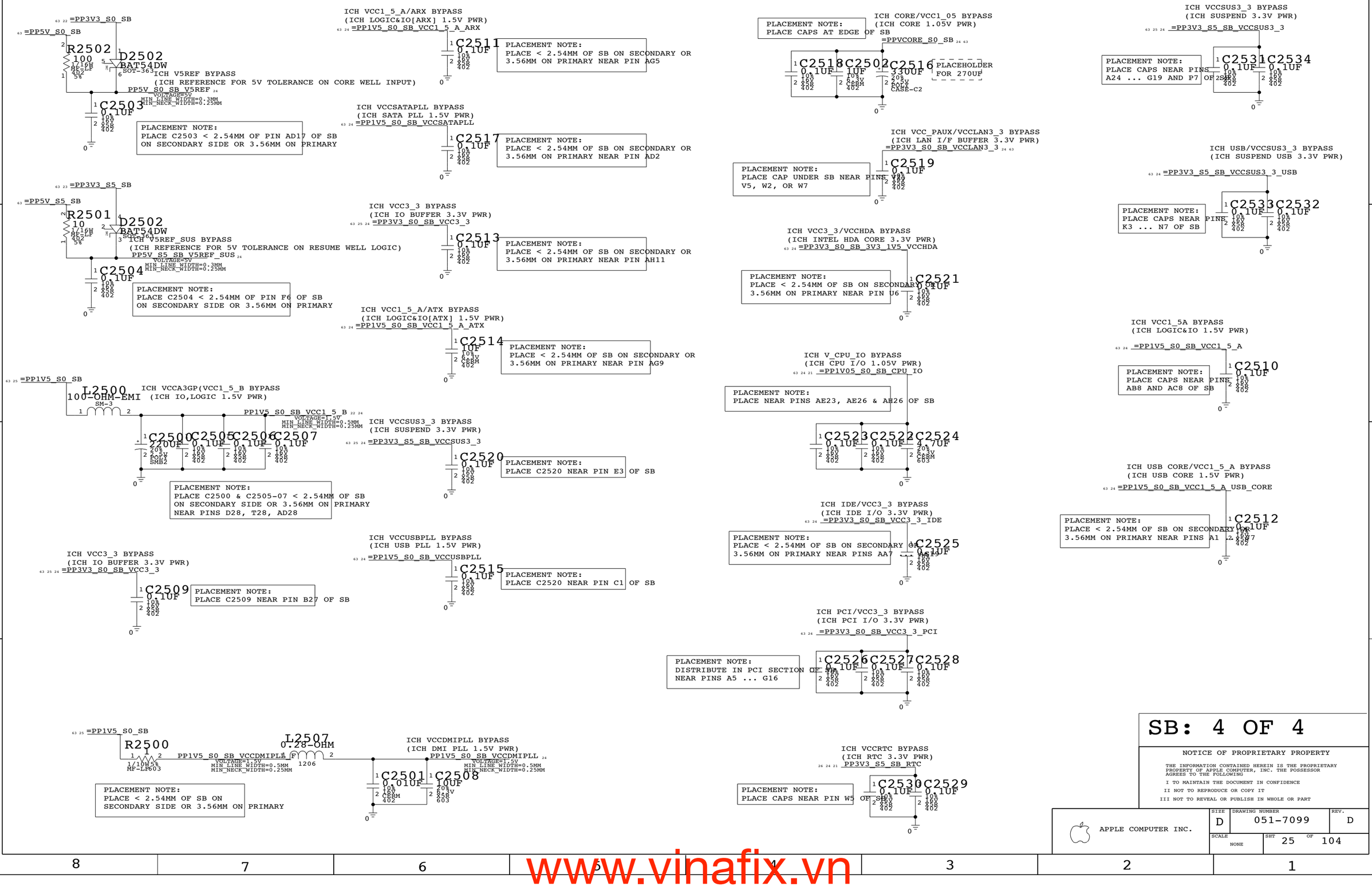
SB: 4 OF 4

SYNC_MASTER=M38 SYNC_DATE=11/16/2005

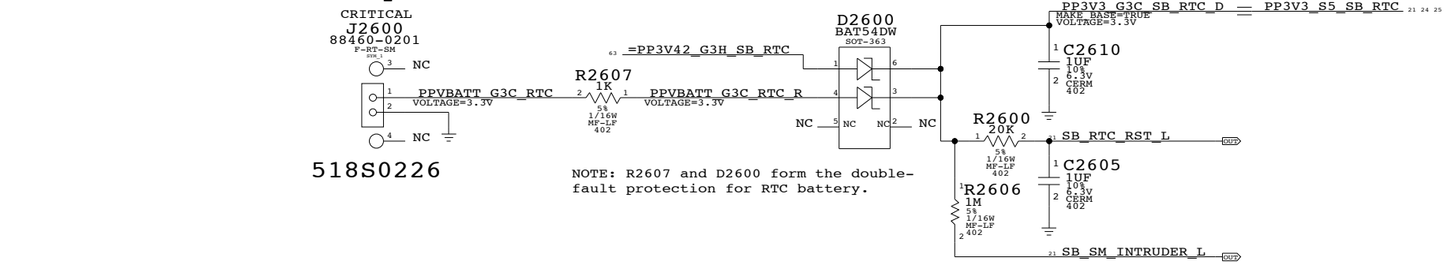
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	24	104



RTC Battery Connector

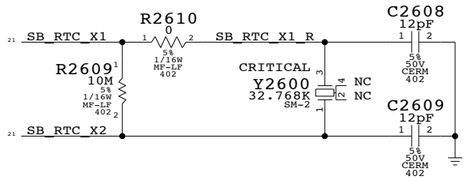


NOTE: R2607 and D2600 form the double-fault protection for RTC battery.

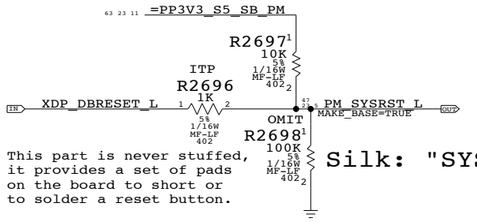
=PP3V3_S0_SB_PCI

PCI_FRAME_L	R2623	1	2	8.2K
PCI_IRDY_L	R2624	1	2	8.2K
PCI_TRDY_L	R2625	1	2	8.2K
PCI_STOP_L	R2626	1	2	8.2K
PCI_SERR_L	R2627	1	2	8.2K
PCI_DEVSEL_L	R2628	1	2	8.2K
PCI_PERR_L	R2630	1	2	8.2K
PCI_LOCK_L	R2629	1	2	8.2K
PCI_REQ0_L	R2632	1	2	8.2K
PCI_REQ1_L	R2631	1	2	8.2K
PCI_REQ2_L	R2633	1	2	8.2K
PCI_REQ3_L	R2634	1	2	8.2K
INT_PIRQA_L	R2637	1	2	8.2K
INT_PIRQB_L	R2636	1	2	8.2K
INT_PIRQC_L	R2638	1	2	8.2K
INT_PIRQD_L	R2639	1	2	8.2K
SB_GPIO2	R2640	1	2	8.2K
SB_GPIO3	R2642	1	2	8.2K
SB_GPIO4	R2641	1	2	8.2K

SB RTC Crystal Circuit



=PP3V3_S5_SB_PM

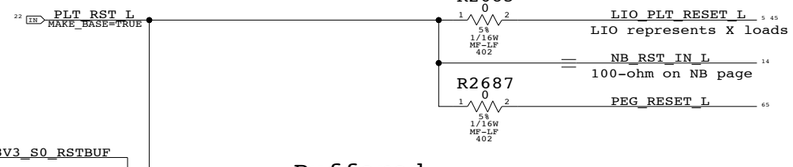


This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

Silk: "SYS RST"

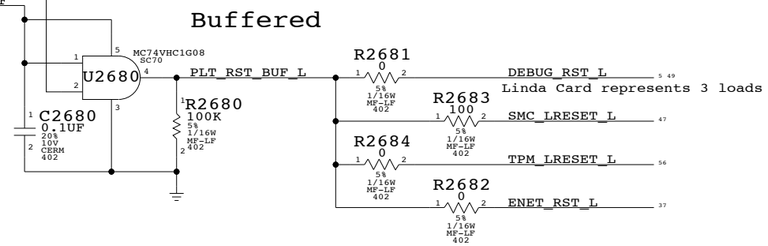
Platform Reset Connections

Unbuffered

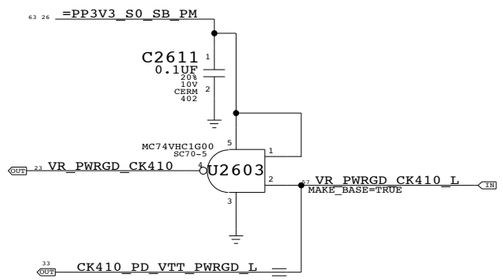


=PP3V3_S0_RSTBUF

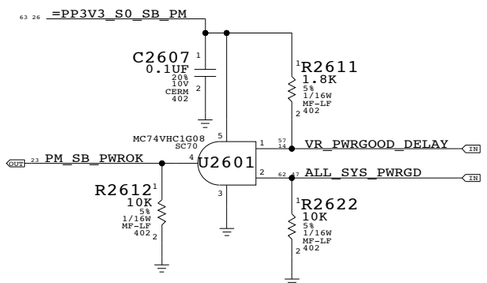
Buffered



Initial resistor values are based on CRB, but may change after characterization.



1G00 used as small & cheap inverter



SB Misc

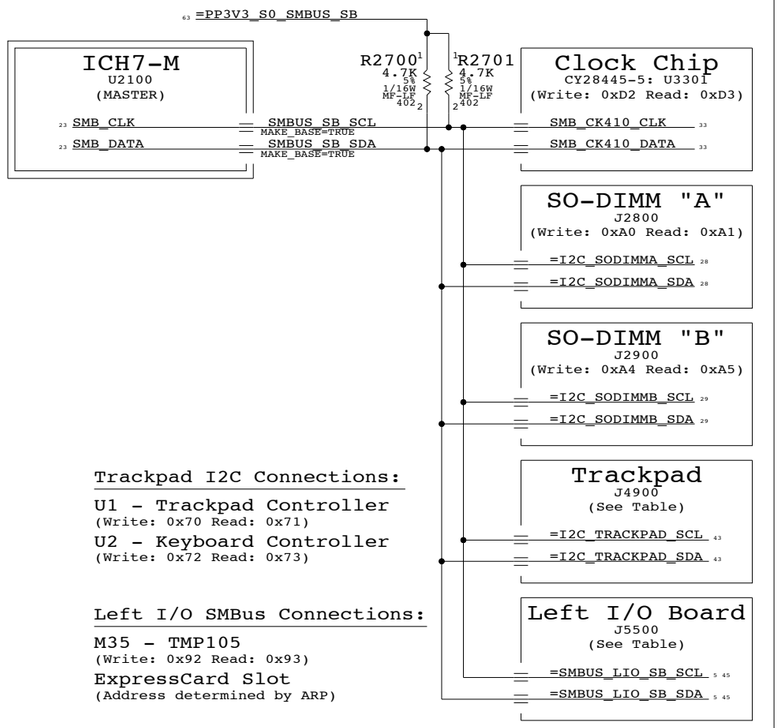
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

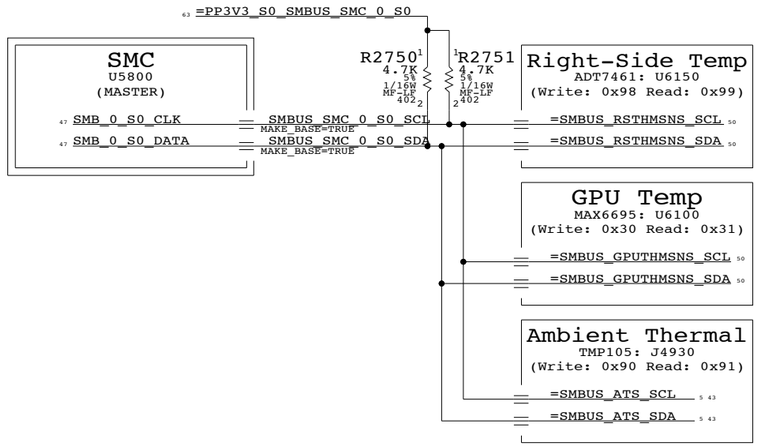
SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	26	104

ICH7-M SMBus Connections

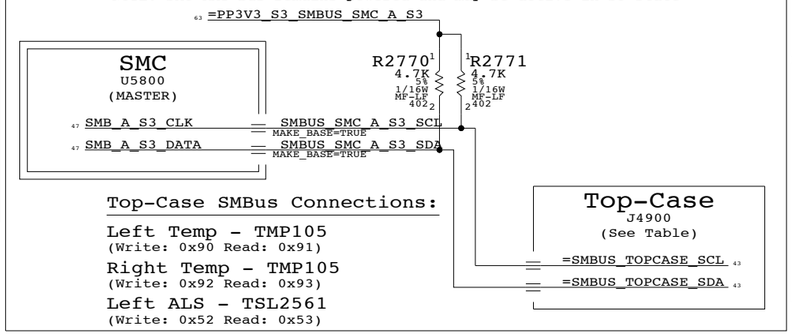


SMC "0" SMBus Connections

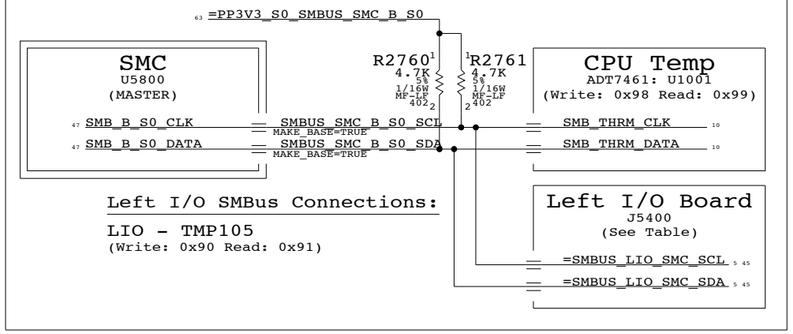


SMC "A" SMBus Connections

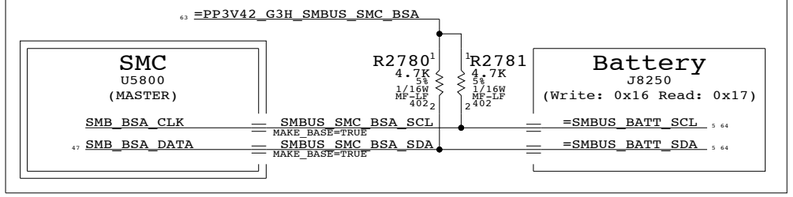
NOTE: SMC RMT bus remains powered and may be active in S3 state



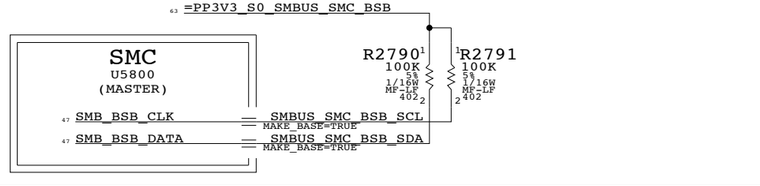
SMC "B" SMBus Connections



SMC "Battery A" SMBus Connections



SMC "Battery B" SMBus Connections



M1 SMBus Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	27	104

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF. The reference voltage must be provided by another page.

"Lower" (surface-mount) slot

=PP1V8_S3_MEM

MEM_VREF

C2801 2.2uF 20% 6.3V CERM 603

C2800 0.1uF 20% 10V CERM 402

NC

CRITICAL
J2800
F-RT-SM
DDR2-SODIMM-DUAL

	1A	VREF			2A	VSS0	
	3A	VSS1			4A	DQ4	MEM_A_DQ<8>
MEM_A_DQ<14>	5A	DQ0			6A	DQ5	MEM_A_DQ<12>
MEM_A_DQ<13>	7A	DQ1			8A	VSS2	
	9A	VSS4			10A	DM0	MEM_A_DM<1>
MEM_A_DQS_N<1>	11A	DQS0*			12A	VSS5	
MEM_A_DQS_P<1>	13A	DQS0			14A	DQ6	MEM_A_DQ<15>
	15A	VSS6			16A	DQ7	MEM_A_DQ<9>
MEM_A_DQ<10>	17A	DQ2			18A	VSS7	
MEM_A_DQ<11>	19A	DQ3			20A	DQ12	MEM_A_DQ<2>
	21A	VSS8			22A	DQ13	MEM_A_DQ<3>
MEM_A_DQ<5>	23A	DQ8			24A	VSS9	
MEM_A_DQ<4>	25A	DQ9			26A	DM1	MEM_A_DM<0>
	27A	VSS10			28A	VSS11	
MEM_A_DQS_N<0>	29A	DQS1*			30A	CK0	MEM_CLK_P<0>
MEM_A_DQS_P<0>	31A	DQS1			32A	CK0*	MEM_CLK_N<0>
	33A	VSS12			34A	VSS13	
MEM_A_DQ<6>	35A	DQ10			36A	DQ14	MEM_A_DQ<1>
MEM_A_DQ<7>	37A	DQ11			38A	DQ15	MEM_A_DQ<0>
	39A	VSS14	KEY		40A	VSS15	
	41A	VSS16			42A	VSS17	
MEM_A_DQ<19>	43A	DQ16			44A	DQ20	MEM_A_DQ<23>
MEM_A_DQ<18>	45A	DQ17			46A	DQ21	MEM_A_DQ<22>
	47A	VSS18			48A	VSS19	
MEM_A_DQS_N<2>	49A	DQS2*			50A	NC0	DIMM_OVERTEMP_L
MEM_A_DQS_P<2>	51A	DQS2			52A	DM2	MEM_A_DM<2>
	53A	VSS21			54A	VSS22	
MEM_A_DQ<20>	55A	DQ18			56A	DQ22	MEM_A_DQ<21>
MEM_A_DQ<16>	57A	DQ19			58A	DQ23	MEM_A_DQ<17>
	59A	VSS23			60A	VSS24	
MEM_A_DQ<28>	61A	DQ24			62A	DQ28	MEM_A_DQ<29>
MEM_A_DQ<25>	63A	DQ25			64A	DQ29	MEM_A_DQ<24>
	65A	VSS25			66A	VSS26	
MEM_A_DM<3>	67A	DM3			68A	DQS3*	MEM_A_DQS_N<3>
NC	69A	NC1			70A	DQS3	MEM_A_DQS_P<3>
	71A	VSS27			72A	VSS28	
MEM_A_DQ<27>	73A	DQ26			74A	DQ30	MEM_A_DQ<26>
MEM_A_DQ<30>	75A	DQ27			76A	DQ31	MEM_A_DQ<31>
	77A	VSS29			78A	VSS30	
MEM_CKE<0>	79A	CKE0			80A	NC/CKE1	MEM_CKE<1>
	81A	VDD0			82A	VDD1	
NC	83A	NC2			84A	NC/A15	MEM_A_A<15>
MEM_A_BS<2>	85A	BA2			86A	NC/A14	MEM_A_A<14>
	87A	VDD2			88A	VDD3	
MEM_A_A<12>	89A	A12			90A	A11	MEM_A_A<11>
MEM_A_A<9>	91A	A9			92A	A7	MEM_A_A<7>
MEM_A_A<8>	93A	A8			94A	A6	MEM_A_A<6>
	95A	VDD4			96A	VDD5	
MEM_A_A<5>	97A	A5			98A	A4	MEM_A_A<4>
MEM_A_A<3>	99A	A3			100A	A2	MEM_A_A<2>
MEM_A_A<1>	101A	A1			102A	A0	MEM_A_A<0>
	103A	VDD6			104A	VDD7	
MEM_A_A<10>	105A	A10/AP			106A	BA1	MEM_A_BS<1>
MEM_A_BS<0>	107A	BA0			108A	RAS*	MEM_A_RAS_L
MEM_A_WE_L	109A	WE*			110A	S0*	MEM_CS_L<0>
	111A	VDD8			112A	VDD9	
MEM_A_CAS_L	113A	CAS*			114A	ODT0	MEM_ODT<0>
MEM_CS_L<1>	115A	NC/S1*			116A	NC/A13	MEM_A_A<13>
	117A	VDD10			118A	VDD11	
MEM_ODT<1>	119A	NC/ODT1			120A	NC3	NC
	121A	VSS31			122A	VSS32	
MEM_A_DQ<35>	123A	DQ32			124A	DQ36	MEM_A_DQ<38>
MEM_A_DQ<39>	125A	DQ33			126A	DQ37	MEM_A_DQ<34>
	127A	VSS33			128A	VSS34	
MEM_A_DQS_N<4>	129A	DQS4*			130A	DM4	MEM_A_DM<4>
MEM_A_DQS_P<4>	131A	DQS4			132A	VSS35	
	133A	VSS36			134A	DQ38	MEM_A_DQ<32>
MEM_A_DQ<37>	135A	DQ34			136A	DQ39	MEM_A_DQ<36>
MEM_A_DQ<33>	137A	DQ35			138A	VSS37	
	139A	VSS38			140A	DQ44	MEM_A_DQ<57>
MEM_A_DQ<60>	141A	DQ40			142A	DQ45	MEM_A_DQ<63>
MEM_A_DQ<59>	143A	DQ41			144A	VSS39	
	145A	VSS40			146A	DQS5*	MEM_A_DQS_N<7>
MEM_A_DM<7>	147A	DM5			148A	DQS5	MEM_A_DQS_P<7>
	149A	VSS41			150A	VSS42	
MEM_A_DQ<58>	151A	DQ42			152A	DQ46	MEM_A_DQ<56>
MEM_A_DQ<61>	153A	DQ43			154A	DQ47	MEM_A_DQ<62>
	155A	VSS43			156A	VSS44	
MEM_A_DQ<43>	157A	DQ48			158A	DQ52	MEM_A_DQ<40>
MEM_A_DQ<45>	159A	DQ49			160A	DQ53	MEM_A_DQ<42>
	161A	VSS45			162A	VSS46	
NC	163A	NC_TEST			164A	CK1	MEM_CLK_P<1>
	165A	VSS47			166A	CK1*	MEM_CLK_N<1>
MEM_A_DQS_N<5>	167A	DQS6*			168A	VSS48	
MEM_A_DQS_P<5>	169A	DQS6			170A	DM6	MEM_A_DM<5>
	171A	VSS49			172A	VSS50	
MEM_A_DQ<41>	173A	DQ50			174A	DQ54	MEM_A_DQ<47>
MEM_A_DQ<46>	175A	DQ51			176A	DQ55	MEM_A_DQ<44>
	177A	VSS51			178A	VSS52	
MEM_A_DQ<51>	179A	DQ56			180A	DQ60	MEM_A_DQ<54>
MEM_A_DQ<50>	181A	DQ57			182A	DQ61	MEM_A_DQ<55>
	183A	VSS53			184A	VSS54	
MEM_A_DM<6>	185A	DM7			186A	DQS7*	MEM_A_DQS_N<6>
	187A	VSS55			188A	DQS7	MEM_A_DQS_P<6>
MEM_A_DQ<53>	189A	DQ58			190A	VSS56	
MEM_A_DQ<48>	191A	DQ59			192A	DQ62	MEM_A_DQ<52>
=PPSPD_S0_MEM	193A	VSS57			194A	DQ63	MEM_A_DQ<49>
=I2C_SODIMMA_SDA	195A	SDA			196A	VSS58	
=I2C_SODIMMA_SCL	197A	SCL			198A	SA0	
	199A	VDDSPD			200A	SA1	ADDR=0xA0(WR)/0xA1(RD)

516S0382

202 NC
204

203 NC
201

=PP1V8_S3_MEM

DDR2 Bypass Caps

(For return current)

=PP1V8_S3_MEM

C2808 10UF 20% 6.3V X5R 603

C2809 10UF 20% 6.3V X5R 603

C2810 0.1uF 20% 10V CERM 402

C2811 0.1uF 20% 10V CERM 402

C2812 0.1uF 20% 10V CERM 402

C2813 0.1uF 20% 10V CERM 402

C2814 0.1uF 20% 10V CERM 402

C2815 0.1uF 20% 10V CERM 402

C2816 0.1uF 20% 10V CERM 402

C2817 0.1uF 20% 10V CERM 402

C2818 0.1uF 20% 10V CERM 402

C2819 0.1uF 20% 10V CERM 402

C2820 0.1uF 20% 10V CERM 402

C2821 0.1uF 20% 10V CERM 402

DDR2 SO-DIMM Connector A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	28	104

Page Notes

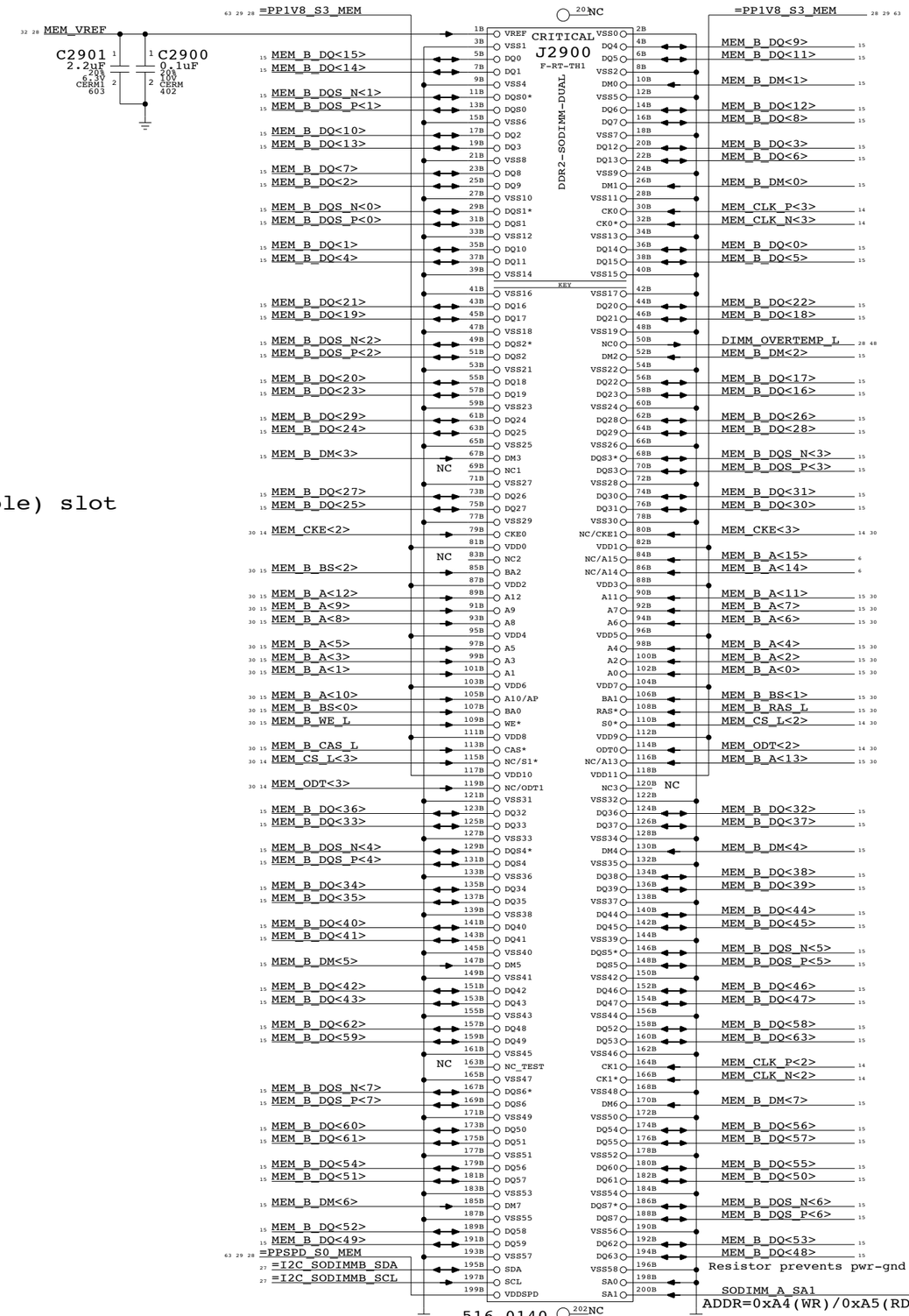
Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

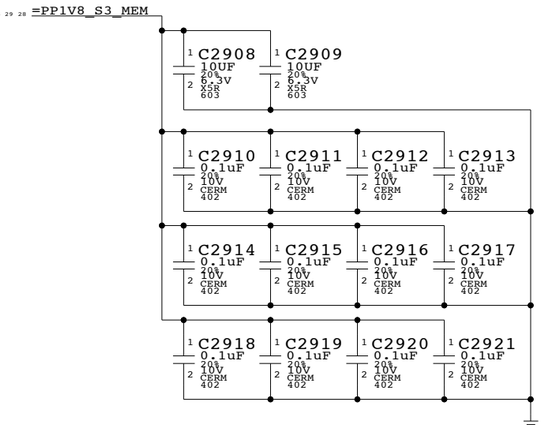
NOTE: This page does not supply VREF. The reference voltage must be provided by another page.

"Upper" (thru-hole) slot



DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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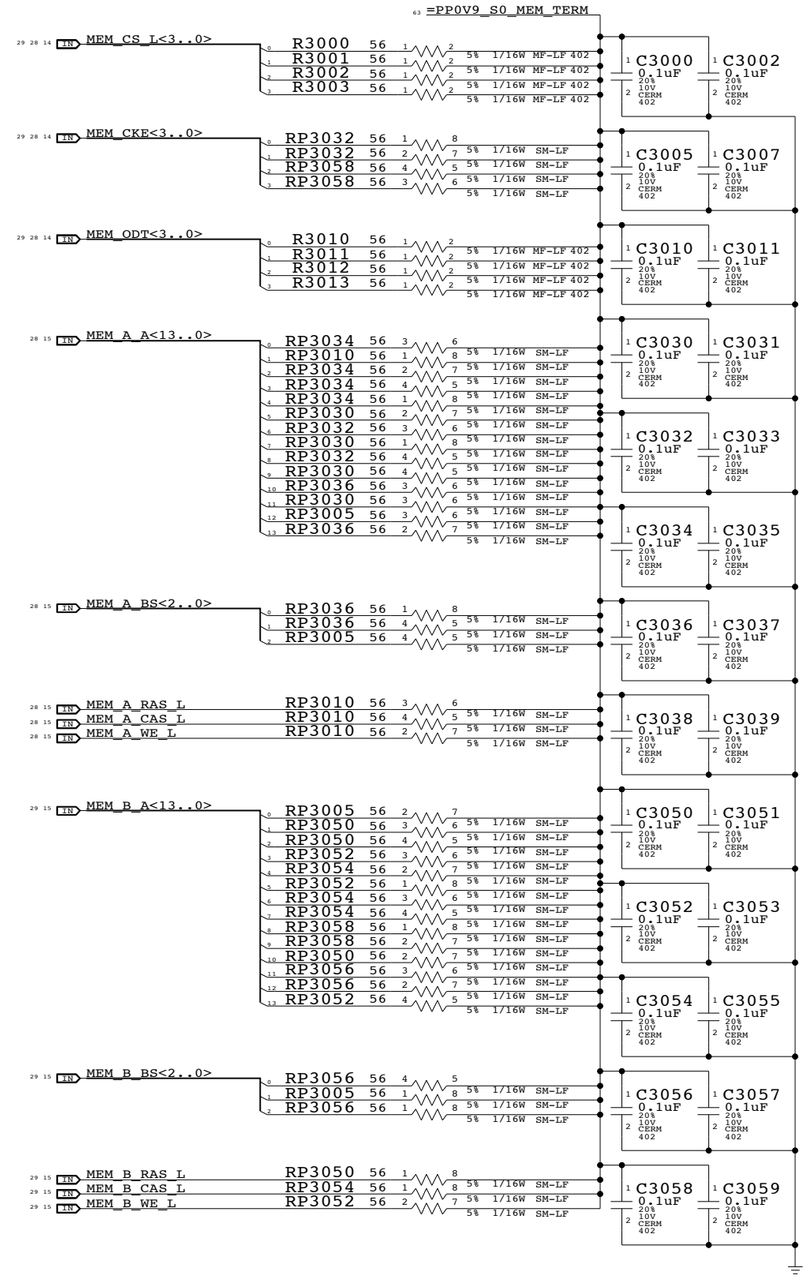
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 29 OF 104	

One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE NONE

SHT 30 OF 104

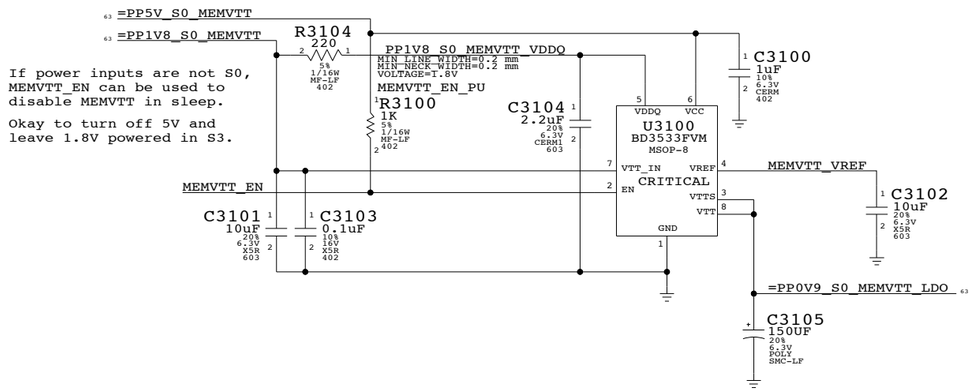
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



If power inputs are not S0, MEMVTT_EN can be used to disable MEMVTT in sleep.

Okay to turn off 5V and leave 1.8V powered in S3.

Memory Vtt Supply

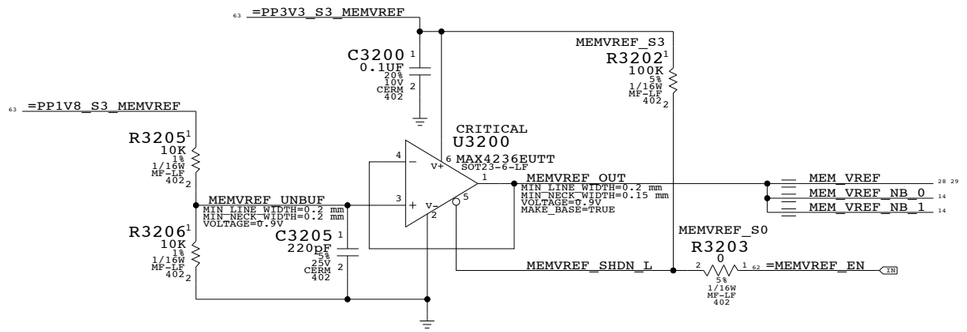
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE: NONE

SHT 31 OF 104



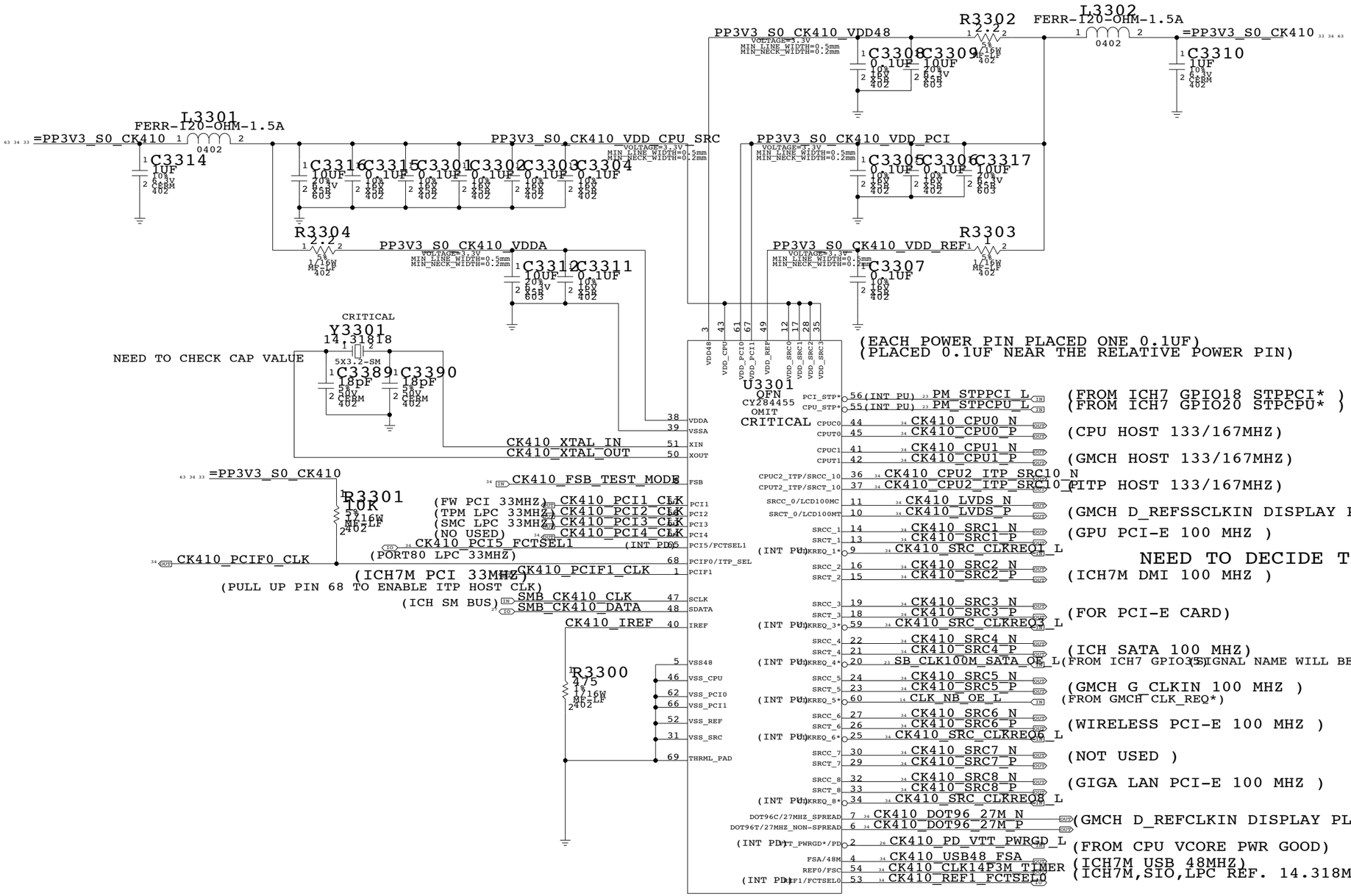
DDR2 VRef

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	32	104



FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M_NON_SPREAD	27M_SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	TBD	SRCT0	SRCC0	

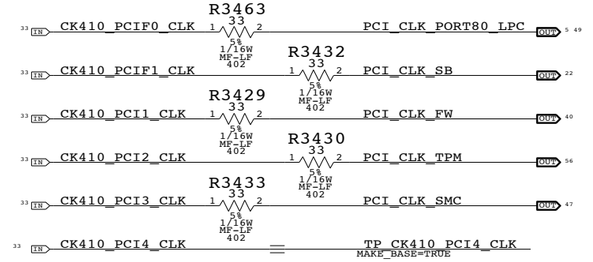
CLOCKS

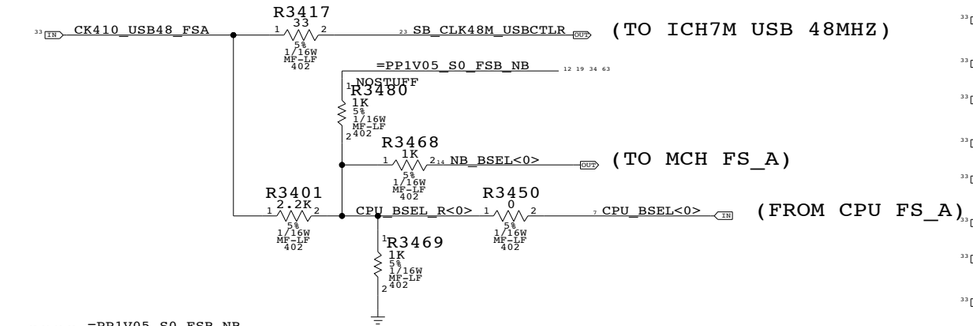
SYNC_MASTER=M87 SYNC_DATE=10/12/2005

APPLE COMPUTER INC.

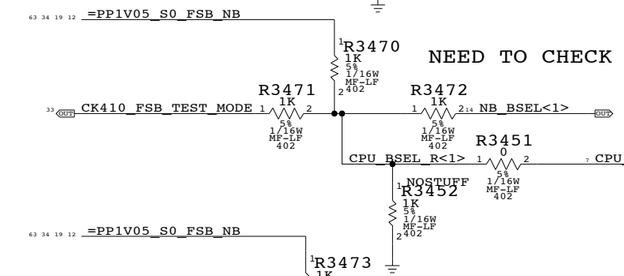
SIZE	DRAWING NUMBER	REV.
D	051-7099	D

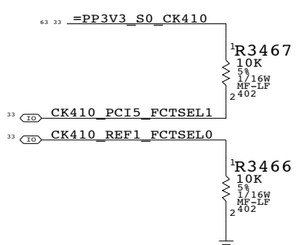
SCALE NONE SHT 33 OF 104





NEED TO CHECK THE BSEL PULLS

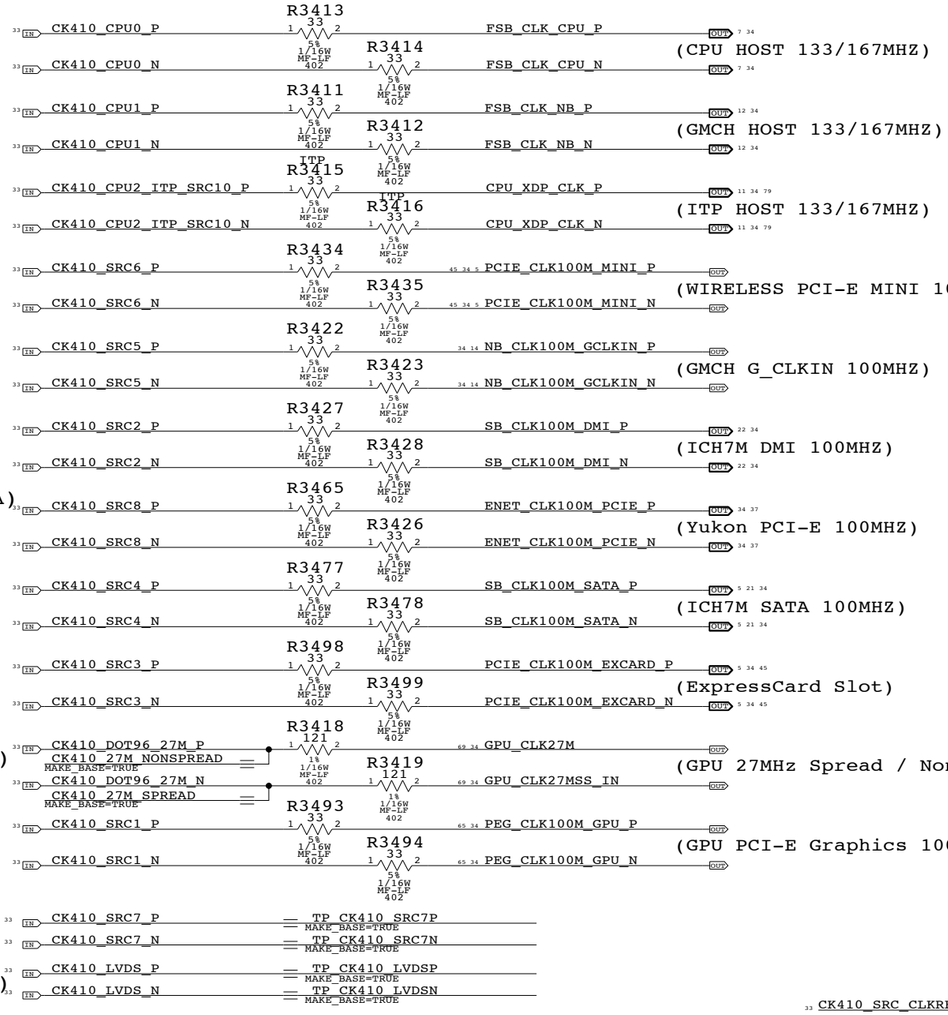


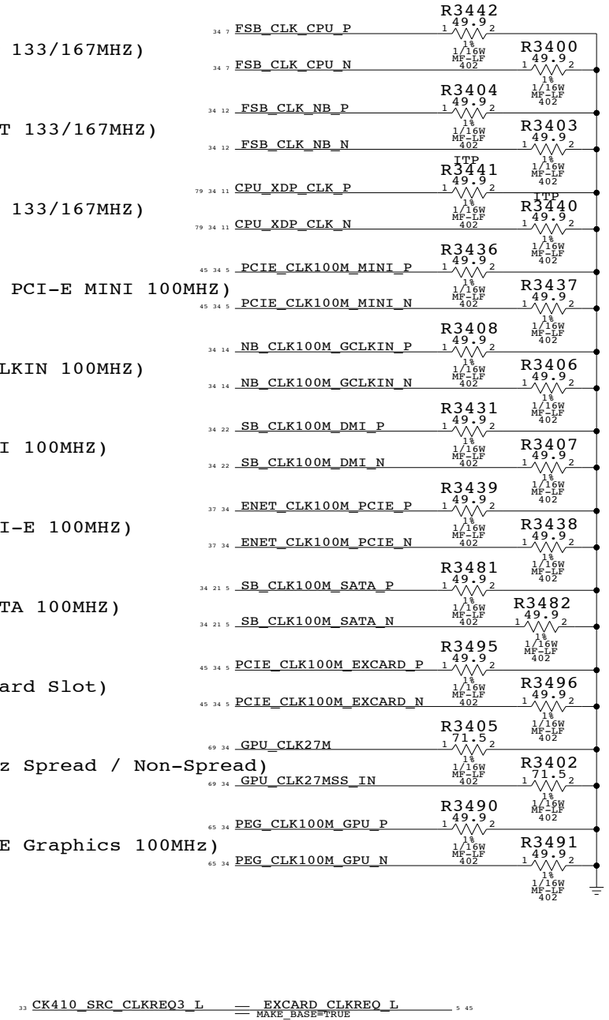


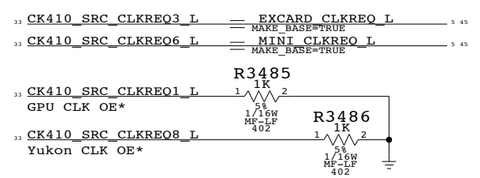
NOSTUFF R3450,R3451,R3453 FOR MANUAL CPU FREQUENCY

FS_C	FS_B	FS_A	CPU
0	0	0	266M
# 0	0	1	133M
# 0	1	0	166M
0	1	1	200M
1	0	0	100M
1	0	1	333M
1	1	0	400M
1	1	1	RESERVED

NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED







Clock Termination

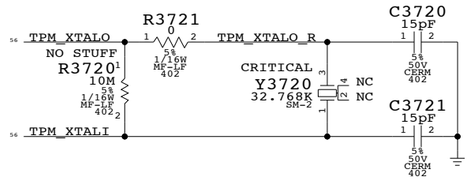
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

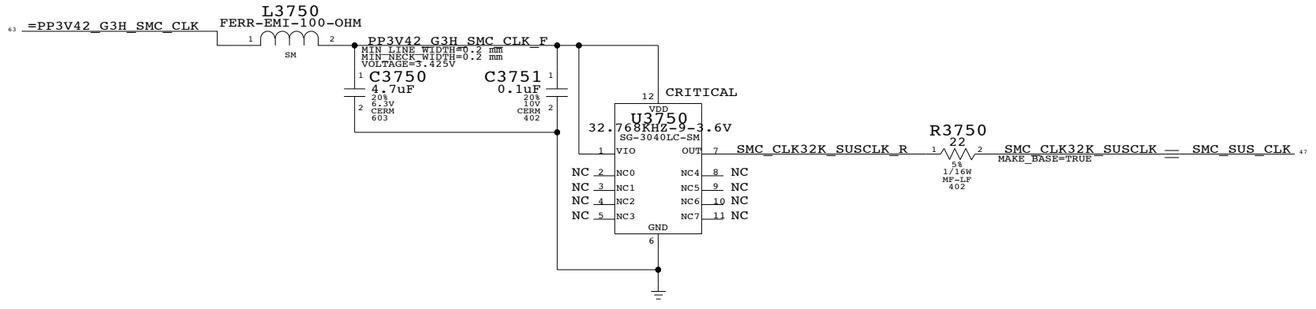
SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE: NONE SHT 34 OF 104

TPM Crystal Circuit



SMC G3Hot Oscillator



Mobile Clocking

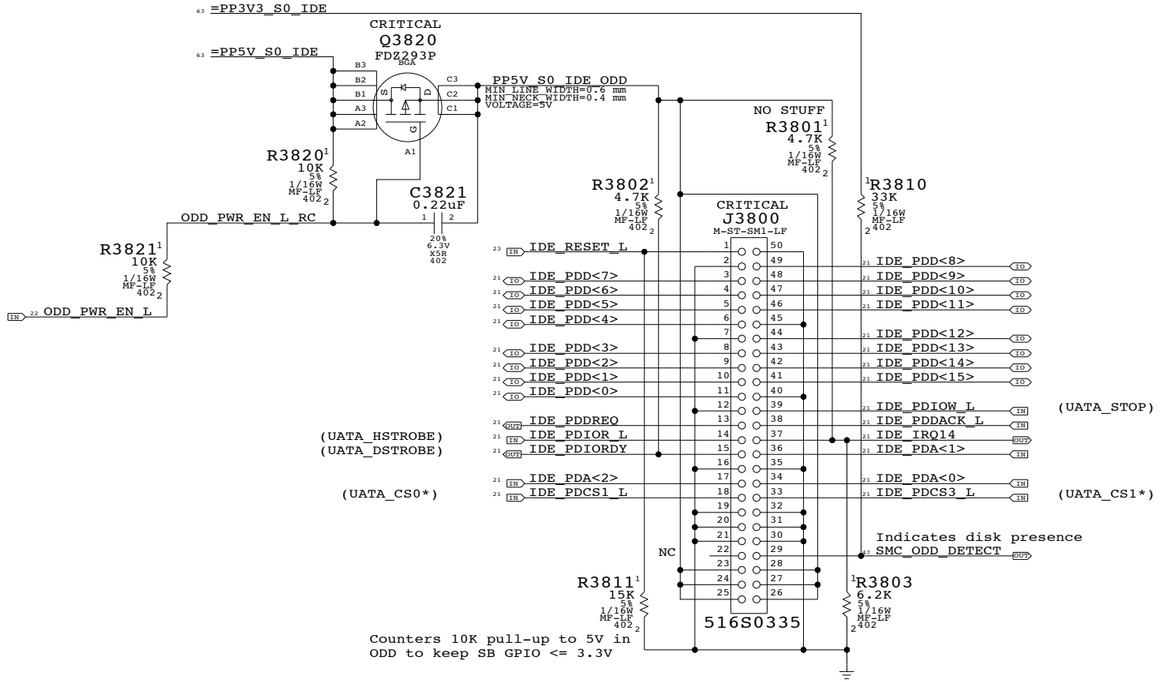
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

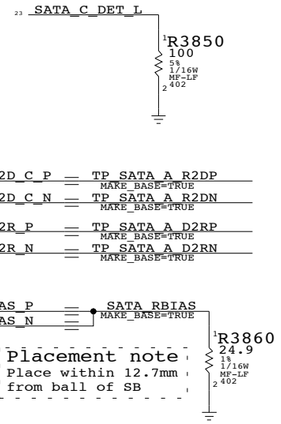
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	37	104

IDE (ODD) Connector





PATA Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 38 OF 104	

PLACE C4100-C4106 NEAR PINS AVDLL0-AVDLL6.
SCHEME MATCHES DOC MVL100258-01 MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.22MM
VOLTAGE=2.5V

38 PP2V5_S3_ENET_AVDD

C4100 1UF 10% 6.3V CERM 402
C4101 0.1UF 10% 16V X5R 402
C4102 0.1UF 10% 16V X5R 402
C4103 0.1UF 10% 16V X5R 402
C4104 0.1UF 10% 16V X5R 402
C4105 0.001UF 10% 50V CERM 402
C4106 0.001UF 10% 50V CERM 402
C4107 0.1UF 10% 16V X5R 402

L4100 FERR-120-OHM-1.5A 0402

=PP2V5_S3_ENET 63

PLACE C4107 NEAR U4101 AVDD

63 37 =PP3V3_S3_ENET

R4101 4.7K 5% 1/16W MF-LF 402

=PP1V2_S3_ENET 37 63

=PP3V3_S3_ENET 37 63

PLACE C4110 AND C4111 WITHIN
12 MIL OF U4101 PIN 49 AND 50

C4110 0.1UF 10% 16V X5R 402

PCIE_A_D2R_C_P — C4111 0.1UF 10% 16V X5R 402 — PCIE_A_D2R_C_N

PCIE_A_D2R_P 22 OUT2
PCIE_A_D2R_N 22 OUT2

C4112 0.1UF X5R 10% 16V 402

PCIE_A_R2D_P 22 IN2
PCIE_A_R2D_N 22 IN2

PLACE C4113 AND C4112 WITHIN
12 MIL OF U21U0 E27 AND E28

C4113 0.1UF 402 X5R 16V 10%

ENET_CLK100M_PCIE_P 34
ENET_CLK100M_PCIE_N 34

PCIE_WAKE_L 45 23 5 WAKE
ENET_RST_L 26 PERST

ENET_LOM_DIS_L 6 → LOM_DISABLE*

OPTIONAL EXTERNAL LDO

=ENET_VMAIN_AVLBL 62

OMIT
CRITICAL
U4101
88E8053
QFN

12	VAUX_AVLBL	
47	VMAIN_AVLBL	
NC 11	SWITCH_VCC	
NC 9	SWITCH_VAUX	
NC 24	HSDACP	ANALOG
NC 25	HSDACN	
4	CTRL25	
3	CTRL12	
16	RSET	
NC 59	LED_ACT*	
NC 60	LED_LINK10/100*	LED
NC 62	LED_LINK1000*	
NC 63	LINK*	
29	TSTPT	TEST
46	TESTMODE	

ENET_CTRL25 6 OUT2
ENET_CTRL12 6 OUT2

R4102 4.87K 1% 1/16W MF-LF 402

NO PULL-UP NEEDED

ENET_RSET

PCI EXPRESS

TX_P 49		
TX_N 50		
RX_P 54		
RX_N 53		
REFCLKP 55		
REFCLKN 56		
WAKE* 6		
PERST* 5		

MEDIA

MDIP0 17	ENET_MDI_P<0> 38
MDIN0 18	ENET_MDI_N<0> 38
MDIP1 20	ENET_MDI_P<1> 38
MDIN1 21	ENET_MDI_N<1> 38
MDIP2 26	ENET_MDI_P<2> 38
MDIN2 27	ENET_MDI_N<2> 38
MDIP3 30	ENET_MDI_P<3> 38
MDIN3 31	ENET_MDI_N<3> 38

TWSI

VPD_CLK 38	ENET_VPD_CLK 37
VPD_DATA 41	ENET_VPD_DATA 37

TEST

PU_VDDO_TTL0 42	ENET_PU_VDD_TTL0 37
PU_VDDO_TTL1 43	ENET_PU_VDD_TTL1 37

ASF IS UNAVAILABLE ON 8053

SPI

SPI_DI 35	NC
SPI_DO 34	NC
SPI_CLK 37	NC
SPI_CS 36	NC

INTERNAL PULL-UP

MAIN CLK

XTALI 15	CRITICAL ENET_XTALI
XTALO 14	ENET_XTALO

1. KEEP ENET_XTALI AND ENET_XTALO TRACE LENGTH <12MIL
2. DO NOT ROUTE UNDER CRYSTAL

Y4101 SM-3.2X2.5MM 25.0000M

C4150 27pF 5% 50V CERM 402
C4151 27pF 5% 50V CERM 402

THRML_PAD 65

R4106 49.9 1% 1/16W MF-LF 402
R4105 49.9 1% 1/16W MF-LF 402
R4104 49.9 1% 1/16W MF-LF 402
R4103 49.9 1% 1/16W MF-LF 402
R4120 49.9 1% 1/16W MF-LF 402
R4119 49.9 1% 1/16W MF-LF 402
R4118 49.9 1% 1/16W MF-LF 402
R4117 49.9 1% 1/16W MF-LF 402

ENET_MDI0
ENET_MDI1
ENET_MDI2
ENET_MDI3

C4116 0.001UF 10% 50V CERM 402
C4115 0.001UF 10% 50V CERM 402
C4117 0.001UF 10% 50V CERM 402
C4118 0.001UF 10% 50V CERM 402

PLACE RESISTORS CLOSE TO U4101

=PP3V3_S3_ENET 37 63

R4130 4.7K 5% 1/16W MF-LF 402
R4131 4.7K 5% 1/16W MF-LF 402

37 ENET_PU_VDD_TTL0
37 ENET_PU_VDD_TTL1

63 37 =PP3V3_S3_ENET

PLACE C4140 NEAR U4102 VCC

C4140 0.1UF 10% 16V X5R 402

OMIT
CRITICAL

U4102 M24C08 SO8

8	VCC	
3	E2	
2	NC1	
1	NC0	
7	WC*	
5	SDA	ENET_VPD_DATA 37
6	SCL	ENET_VPD_CLK 37
4	VSS	

R4122 4.7K 5% 1/16W MF-LF 402
R4123 4.7K 5% 1/16W MF-LF 402

PLACE C4127-C4134 NEAR PINS VDD0-VDD7 ON U4101
SCHEME MATCHES DOC MVL100258-01

63 37 =PP1V2_S3_ENET

C4126 0.1UF 10% 16V X5R 402
C4127 0.1UF 10% 16V X5R 402
C4128 0.1UF 10% 16V X5R 402
C4129 0.1UF 10% 16V X5R 402
C4130 0.1UF 10% 16V X5R 402
C4131 0.001UF 10% 50V CERM 402
C4132 0.001UF 10% 50V CERM 402
C4133 0.001UF 10% 50V CERM 402
C4134 0.001UF 10% 50V CERM 402

PLACE C4135-C4139 NEAR VDDO_TTL0-VDD_TTL4 ON U4101
SCHEME MATCHES DOC MVL100258-01

63 37 =PP3V3_S3_ENET

C4135 0.1UF 10% 16V X5R 402
C4136 0.1UF 10% 16V X5R 402
C4137 0.1UF 10% 16V X5R 402
C4138 0.001UF 10% 50V CERM 402
C4139 0.001UF 10% 50V CERM 402

ETHERNET CONTROLLER

SYNC_MASTER=M42 SYNC_DATE=10/12/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 41 OF 104	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED BY ETHERNET PHY	ENETCONN	ENET_100D	ENETCONN_P<0>
	ENETCONN	ENET_100D	ENETCONN_N<0>
	ENETCONN	ENET_100D	ENETCONN_P<1>
	ENETCONN	ENET_100D	ENETCONN_N<1>
	ENETCONN	ENET_100D	ENETCONN_P<2>
	ENETCONN	ENET_100D	ENETCONN_N<2>
	ENETCONN	ENET_100D	ENETCONN_P<3>
	ENETCONN	ENET_100D	ENETCONN_N<3>

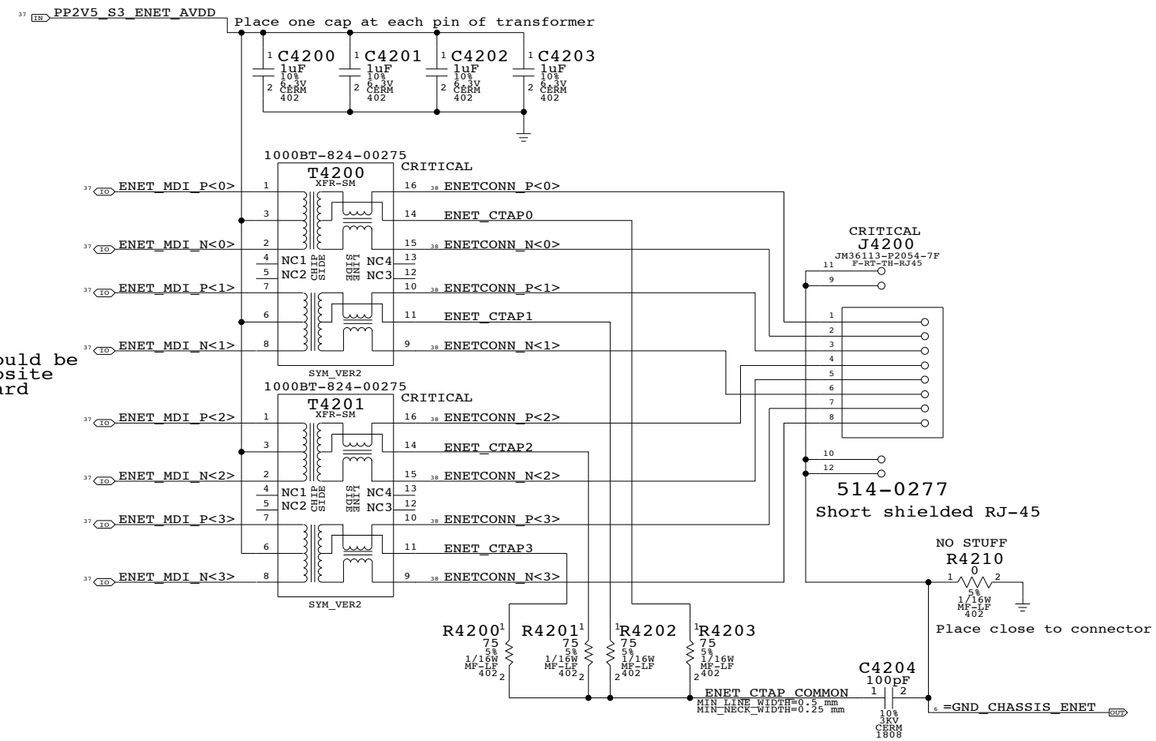
Page Notes

Power aliases required by this page:
- =PP2V5_ENET
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Transformers should be mirrored on opposite sides of the board



Ethernet Connector

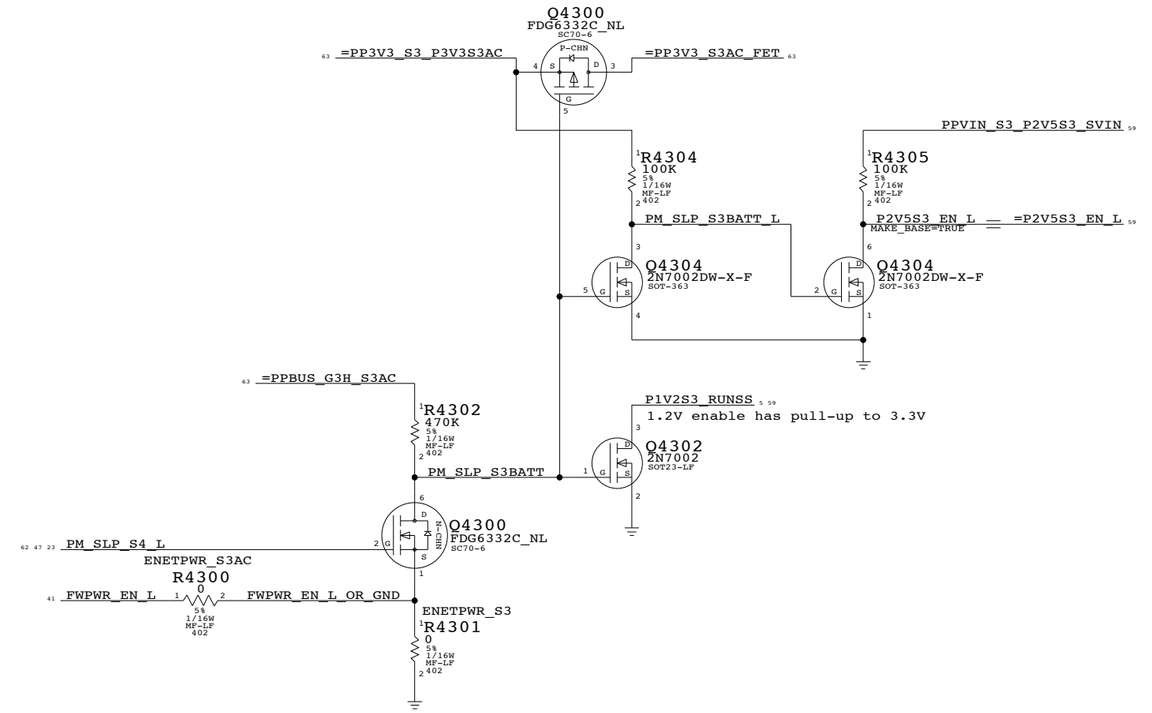
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 42 OF 104	

Yukon Power Control

Allows powering Yukon down during battery sleep to save power



When ENETPWR_S3AC BOMOPTION is active:

State	FWPWR_EN_L	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN_L	P1V2S3_RUNSS
S0 AC	0V	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S0 Batt	0V	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S3 AC	0V	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S3 Batt	PBUS	3.3V	PBUS (3.3V OFF)	0V	3.3V (2.5V OFF)	0V (1.2V OFF)
S5 AC	0V	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)
S5 Batt	PBUS	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)
G3H Batt	PBUS	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)

When ENETPWR_S3 BOMOPTION is active:

State	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN_L	P1V2S3_RUNSS
S0	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S3	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S5	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)
G3H	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)

Yukon Power Control

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-7099 | REV. D

SCALE NONE | SHT 43 OF 104

PAGE NOTES

INPUT
=PP3V3_S0_FW - 3.3V POWER FOR FIREWIRE (MOBILE: OFF DURING SLEEP)
=PP3V3_S0_PCI - 3.3V POWER FOR PCI FIREWIRE (MOBILE: OFF DURING SLEEP)
PCI_GNT3_L - PCI GRANT FROM SB
PCI_CLK_FW - NEED TO REFERENCE TO ALIAS PAGE
PCI_RST_L - PCI RESET FROM SB
FW_PC0 - FIREWIRE POWER CLASS IDENTIFIER

INPUT/OUTPUT
PCI_AD<0..31>,PCI_C_BE_L<0..3>,PCI_FRAME_L,PCI_IRDY_L,PCI_TRDY_L,
PCI_DEVSEL_L, PCI_STOP_L, PCI_PAR, PCI_PERR_L, PCI_SERR_L
FW_A_TPA_P/N, FW_A_TPB_P/N, FW_A_TPBIAS - PORT 0 FIREWIRE DIFF PAIRS
FW_B_TPA_P/N, FW_B_TPB_P/N, FW_B_TPBIAS - PORT 1 FIREWIRE DIFF PAIRS
FW_C_TPA_P/N, FW_C_TPB_P/N, FW_C_TPBIAS - PORT 2 FIREWIRE DIFF PAIRS

OUTPUT
PCI_REQ3_L - PCI REQUEST TO SB
PM_CLKRUN_L - CLOCK-RUN PCI PROTOCOL
INT_PIRQD_L - INTERRUPT TO SB
PCI_PME_FW_L - DEDICATED PME FOR FIREWIRE (SB GPIO1)

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
6/20/2005 - BGA VERSION OF FW323-06 ADDED
6/21/2005 - CHANGED INT* TO_INT_PIRQD_L (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED PCI_ID TO_AD19 (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED REQ/GNT TO_REQ3/GNT3 (PER ARCHITECTURAL DEFINITION)
6/22/2005 - ADDED 51OK PULL-DOWN ON RST* AND REMOVED CONNECTION TO PLT_RST_L
6/22/2005 - CHANGED CLK_PME_RLPE_PAIR_NAMES_TO_BE_RE-USE_COMPLIANT
6/22/2005 - REMOVED CONSTRAINT SETS AS THEY WILL BE MANAGED ON BOARD SIDE
6/22/2005 - REMOVED C4421 - REDUNDANT
6/22/2005 - BRING OUT PCI CONNECTION TO BE CONNECTED ON PORT PAGE
7/26/2005 - CONNECTED PIN E10 TO GND

0.001A DURING SLEEP

63 =PP3V3_S3_FW

PLACE ONE CAP PER TWO PINS STARTING WITH C4424 ON VDD0

C4424 10UF 20% 6.3V X5R 603
C4418 0.1UF 20% 10V CERM 402
C4422 0.1UF 20% 10V CERM 402
C4426 0.1UF 20% 10V CERM 402
C4428 0.1UF 20% 10V CERM 402
C4430 0.1UF 20% 10V CERM 402
C4432 0.1UF 20% 10V CERM 402

L4400
600-OHM-300MA
0402

PLACE ONE CAP PER TWO PINS STARTING WITH C4416 ON VDDA0

PP3V3_S3_FW_AVDD
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM

C4416 10UF 20% 6.3V X5R 603
C4417 0.1UF 10% 16V X5R 402
C4429 0.1UF 10% 16V X5R 402
C4425 0.1UF 10% 16V X5R 402

GND_FW_VSSA 40
VOLTAGE=0V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM

63 =PP3V3_S3_PCI

VDD0 G4, VDD1 N1, VDD2 N2, VDD3 K5, VDD4 K6, VDD5 K7, VDD6 L13, VDD7 H13, VDD9 A2
VDDA0 D10, VDDA1 A14, VDDA2 B13, VDDA3 A7, VDDA4 B8, VDDA5 D9

CONNECT TO VDD FOR 3.3V OPERATION

PCI_VIOS

PCI_AD<0>	F10	PCI_AD0
PCI_AD<1>	G10	PCI_AD1
PCI_AD<2>	H10	PCI_AD2
PCI_AD<3>	H12	PCI_AD3
PCI_AD<4>	J13	PCI_AD4
PCI_AD<5>	J12	PCI_AD5
PCI_AD<6>	K13	PCI_AD6
PCI_AD<7>	K10	PCI_AD7
PCI_AD<8>	L12	PCI_AD8
PCI_AD<9>	M13	PCI_AD9
PCI_AD<10>	L11	PCI_AD10
PCI_AD<11>	M12	PCI_AD11
PCI_AD<12>	M11	PCI_AD12
PCI_AD<13>	N12	PCI_AD13
PCI_AD<14>	M10	PCI_AD14
PCI_AD<15>	N11	PCI_AD15
PCI_AD<16>	M4	PCI_AD16
PCI_AD<17>	N5	PCI_AD17
PCI_AD<18>	N4	PCI_AD18
PCI_AD<19>	M3	PCI_AD19
PCI_AD<20>	M2	PCI_AD20
PCI_AD<21>	N3	PCI_AD21
PCI_AD<22>	K4	PCI_AD22
PCI_AD<23>	M1	PCI_AD23
PCI_AD<24>	K2	PCI_AD24
PCI_AD<25>	J4	PCI_AD25
PCI_AD<26>	K1	PCI_AD26
PCI_AD<27>	J2	PCI_AD27
PCI_AD<28>	J1	PCI_AD28
PCI_AD<29>	H2	PCI_AD29
PCI_AD<30>	H4	PCI_AD30
PCI_AD<31>	H1	PCI_AD31
PCI_C_BE_L<0>	K12	PCI_CBE0*
PCI_C_BE_L<1>	M9	PCI_CBE1*
PCI_C_BE_L<2>	L3	PCI_CBE2*
PCI_C_BE_L<3>	L4	PCI_CBE3*
PCI_PAR	N10	PCI_PAR
PCI_FRAME_L	N6	PCI_FRAME*
PCI_IRDY_L	M6	PCI_IRDY*
PCI_TRDY_L	N7	PCI_TRDY*
PCI_DEVSEL_L	N8	PCI_DEVSEL*
PCI_STOP_L	M7	PCI_STOP*
FW_PCI_IDSEL	L2	PCI_IDSEL
PCI_REQ3_L	E2	PCI_REQ*
PCI_GNT3_L	E1	PCI_GNT*
PCI_PERR_L	M8	PCI_PERR*
PCI_SERR_L	N9	PCI_SERR*
PCI_CLK_FW	G2	PCI_CLK
PM_CLKRUN_L	D1	CLKRUN*
FW_PCI_RST_L	F1	PCI_RST*
INT_PIRQD_L	D2	PCI_INTA*
PCI_PME_FW_L	F2	PCI_PME*

R4431 22 5% 1/16W MF-LF 402

R4432 100 1% 1/16W MF-LF 402

THIS IS FROM ICH-7M

CRITICAL
U4400
FW32306
BGA
OMIT

197S0178 3.2MMX2.5MM
CRITICAL

Y4403 SM-3.2X2.5MM 24.576MHZ

R4400 390 5% 1/16W MF-LF 402

C4411 22PF 5% 50V CERM 402
C4412 22PF 5% 50V CERM 402

NEED TO CHECK CRYSTAL LOAD CAPACITANCE

XI	A5	FW_XI	
XO	B5	FW_XO	
RESET*	B4	FW_PWRON_RST_L	
R1	A6	FW_R1	R4452 2.49K 1% 1/16W MF-LF 402
R0	B7	FW_R0	
TPBIAS0	B8	42 FW_A_TPBIAS	
TPA0_P	A9	42 FW_A_TPA_P	
TPA0_N	B9	42 FW_A_TPA_N	
TPB0_P	B10	42 FW_A_TPB_P	
TPB0_N	A10	42 FW_A_TPB_N	
TPBIAS1	D8	42 FW_B_TPBIAS	
TPA1_P	A11	42 FW_B_TPA_P	
TPA1_N	B11	42 FW_B_TPA_N	
TPB1_P	B12	42 FW_B_TPB_P	
TPB1_N	A12	42 FW_B_TPB_N	
TPBIAS2	C13	42 FW_C_TPBIAS	
TPA2_P	C11	42 FW_C_TPA_P	
TPA2_N	C12	42 FW_C_TPA_N	
TPB2_P	D13	42 FW_C_TPB_P	
TPB2_N	D12	42 FW_C_TPB_N	

SPEC RECOMMENDS 2.49K

C4420 0.1UF 10% 16V X5R 402
R4420 510K 5% 1/16W MF-LF 402

MODE_420	M5	MODE FOR EXTERNAL LINK	
MODE_A	B6		
PC0	E12	42 FW_PC0	DUAL PORT DEVICES ARE POWER CLASS 4 (‘100’) SINGLE PORT DEVICES ARE POWER CLASS 0 (‘000’)
PC1	F13		
PC2	F12		
CONTENDER	G12	LOW = NOT BUS MANAGER	
CARDBUSN	B1	LOW = PCI OPERATION	
MPCI_ACTN_323	E10		

TEST0	C2	
TEST1	C1	
ATEST	A4	
SE	A3	
SM	B3	

MANUFACTURING TEST PINS

XW4400 SM

VSS0	A1	
VSS1	B2	
VSS2	C3	
VSS3	D4	
VSS4	E4	
VSS5	E5	
VSS6	F4	
VSS7	F6	
VSS8	F7	
VSS9	F8	
VSS10	G1	
VSS11	G6	
VSS12	G7	
VSS13	G8	
VSS14	H6	
VSS15	H7	
VSS16	H8	
VSS17	J5	
VSS18	J9	
VSS19	J10	
VSS20	K8	
VSS21	K9	
VSS22	N13	
VSSA0	E13	
VSSA1	E9	
VSSA2	D9	
VSSA3	D7	
VSSA4	D5	

GND_FW_VSSA 40

FIREWIRE CONTROLLER

SYNC_MASTER=(M42) SYNC_DATE=08/29/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 44 OF 104	

Page Notes

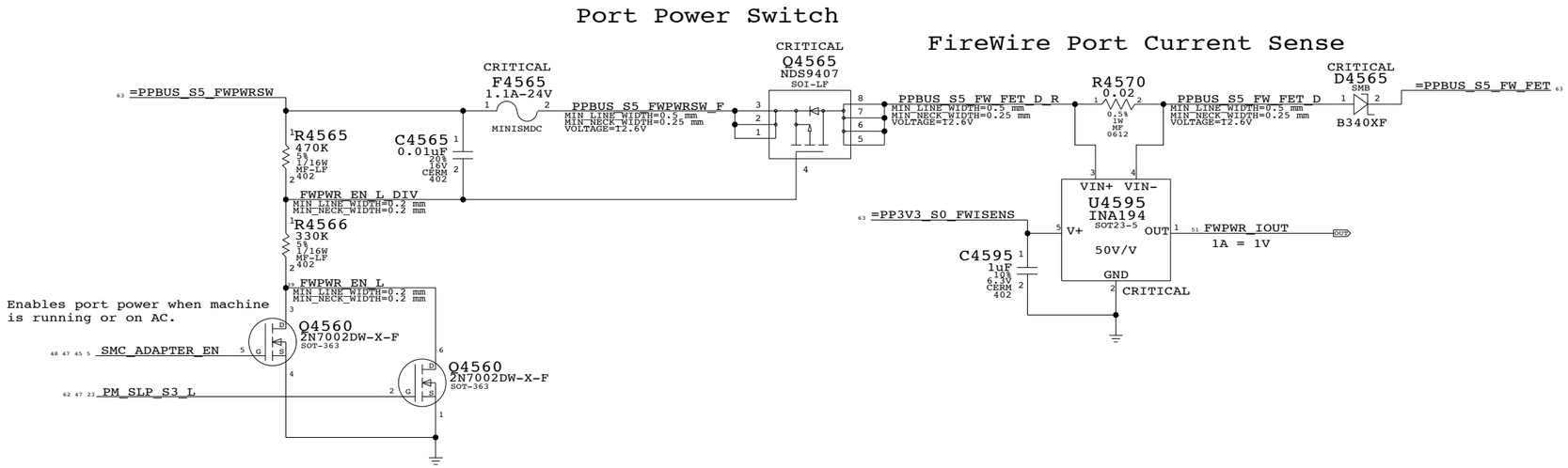
Power aliases required by this page:
- =PPBUS_S0_FWPWRSW (system supply for bus power)
- =PP3V3_S0_FWPORTPWRSW

Signal aliases required by this page:
- =FWPWR_PWRON (see related text note below)

BOM options provided by this page:
(NONE)

Port Power Switch

FireWire Port Current Sense



FireWire Port Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE: NONE

SHT 45 OF 104

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED BY PHY PAGE	FW	FW_110D	FW_PORT1_TPA_FL_P 42
	FW	FW_110D	FW_PORT1_TPA_FL_N 42
	FW	FW_110D	FW_PORT1_TPB_FL_P 42
	FW	FW_110D	FW_PORT1_TPB_FL_N 42

Page Notes

Power aliases required by this page:
- =PPFW_PORT1
- =PP3V3_S5_FWLATEVG
- =GND_CHASSIS_FW_PORT1

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

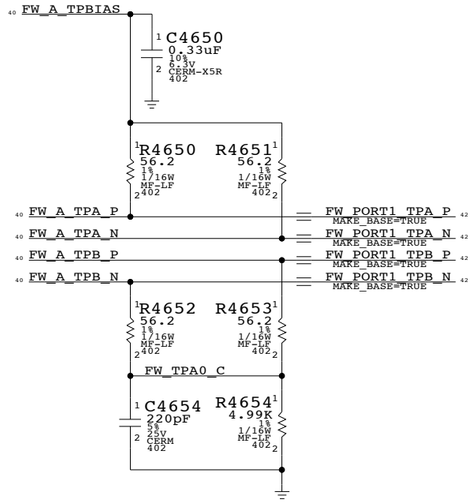
BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

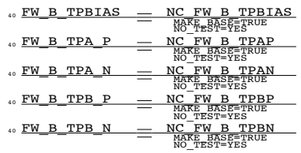
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

Termination

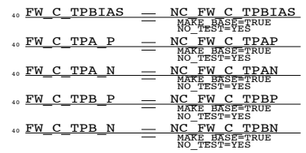
Place close to FireWire PHY



2nd TPA/TPB pair unused

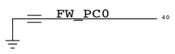


3rd TPA/TPB pair unused

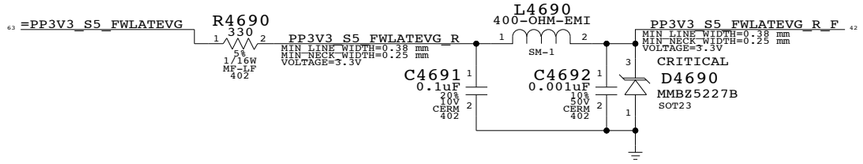


FW Power Class Strap

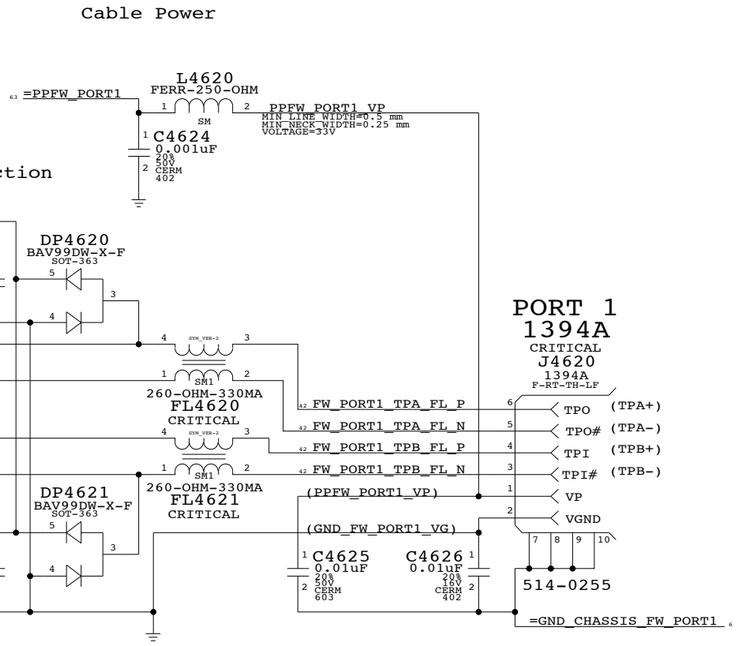
Single-port system sets PC=0



Late-VG Protection Power



Cable Power

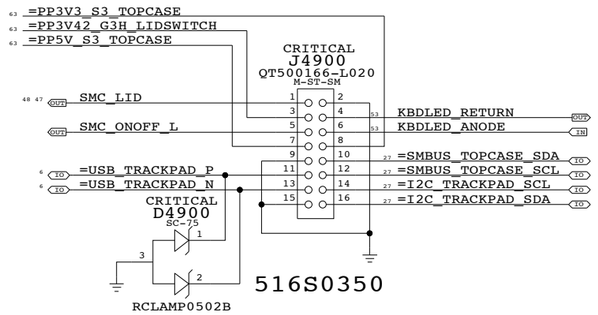


"Snapback" & "Late VG" Protection

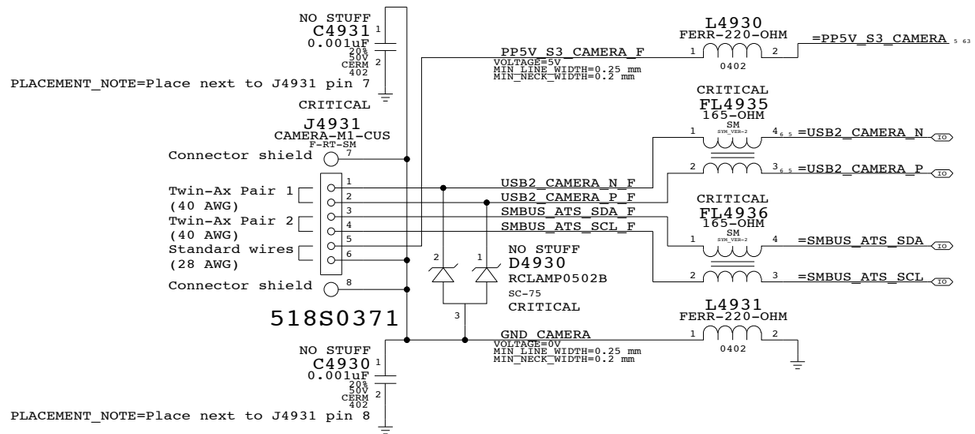
FireWire Ports	
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7099	D
	SCALE NONE	SHT 46 OF 104	

Top-Case Connector



Camera Connector



Internal USB Connections

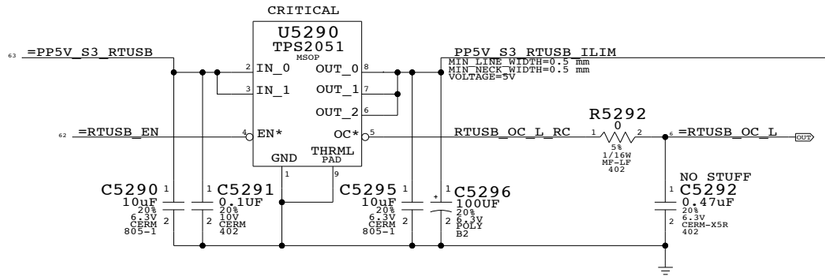
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

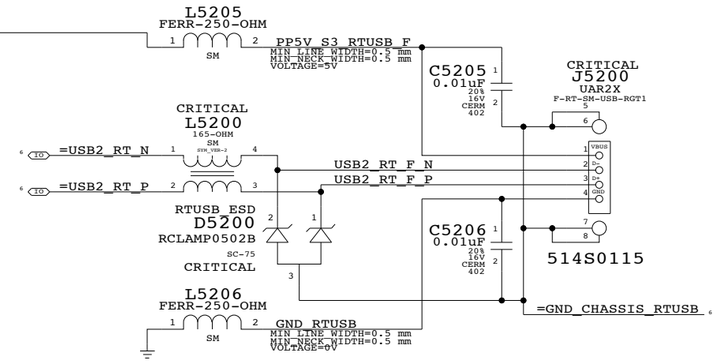
SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	49	104

Port Power Switch



Right USB Port



Place L5200, L5205 and L5206 across moat

External USB Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

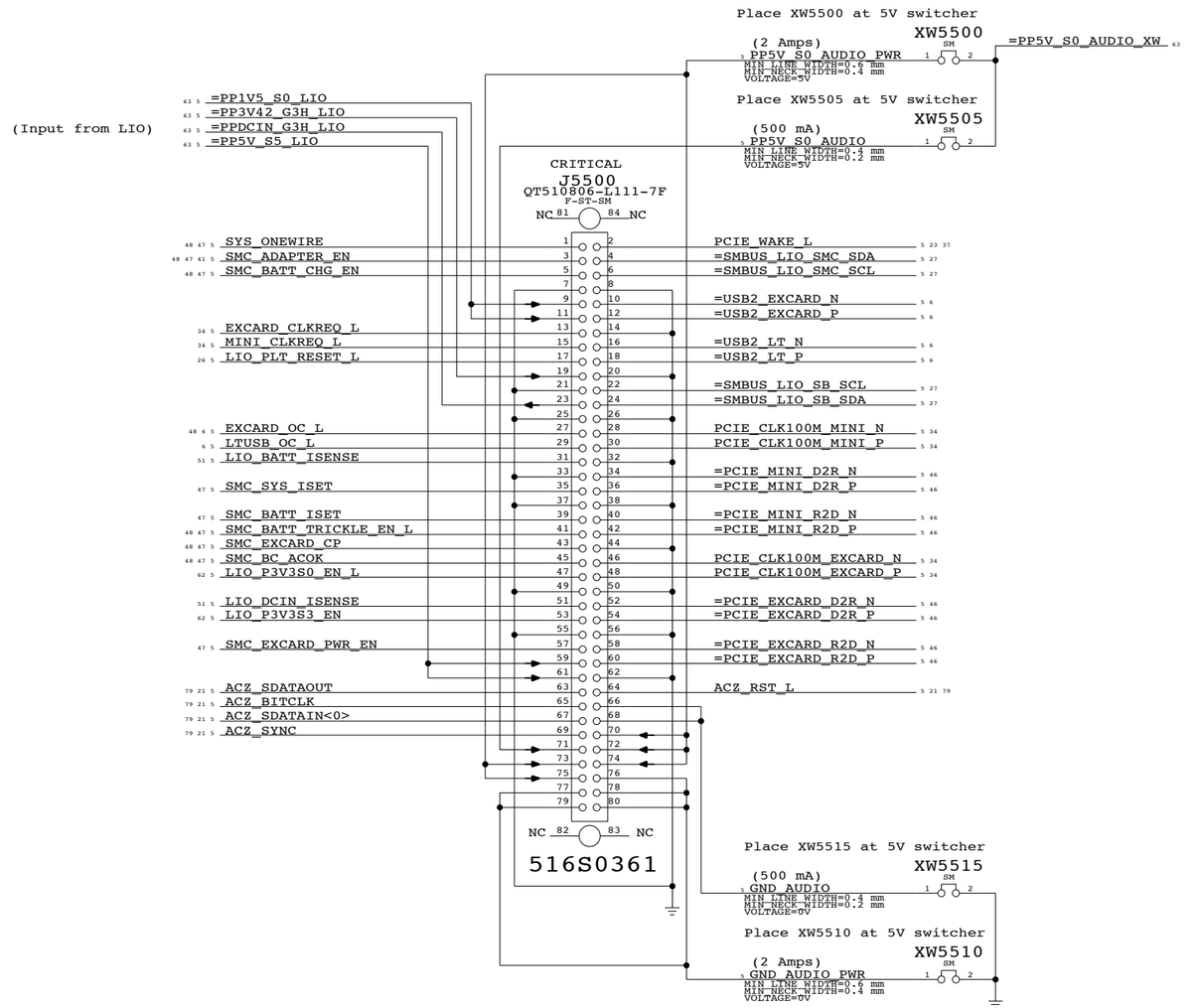
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE: NONE

SHT 52 OF 104

Left I/O Board Connector



Left I/O Board Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

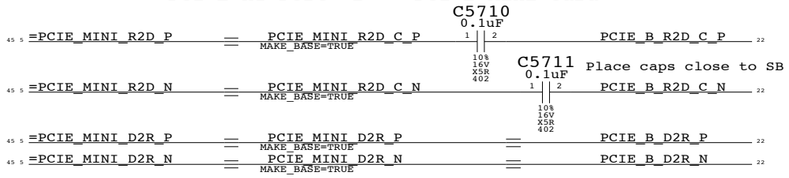
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

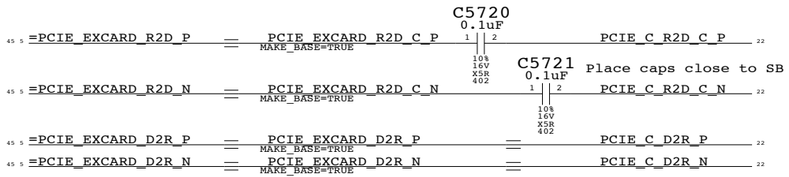
SCALE	SHT	OF
NONE	55	104

PCI-E x1 Port "A" = Ethernet (Yukon)

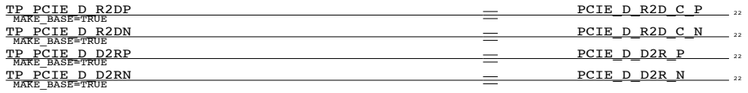
PCI-E x1 Port "B" = PCI-E Mini Card



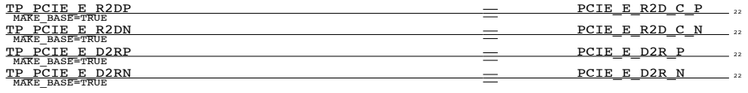
PCI-E x1 Port "C" = ExpressCard



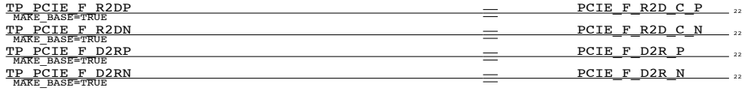
PCI-E x1 Port "D" = Unused



PCI-E x1 Port "E" = Unused



PCI-E x1 Port "F" = Unused



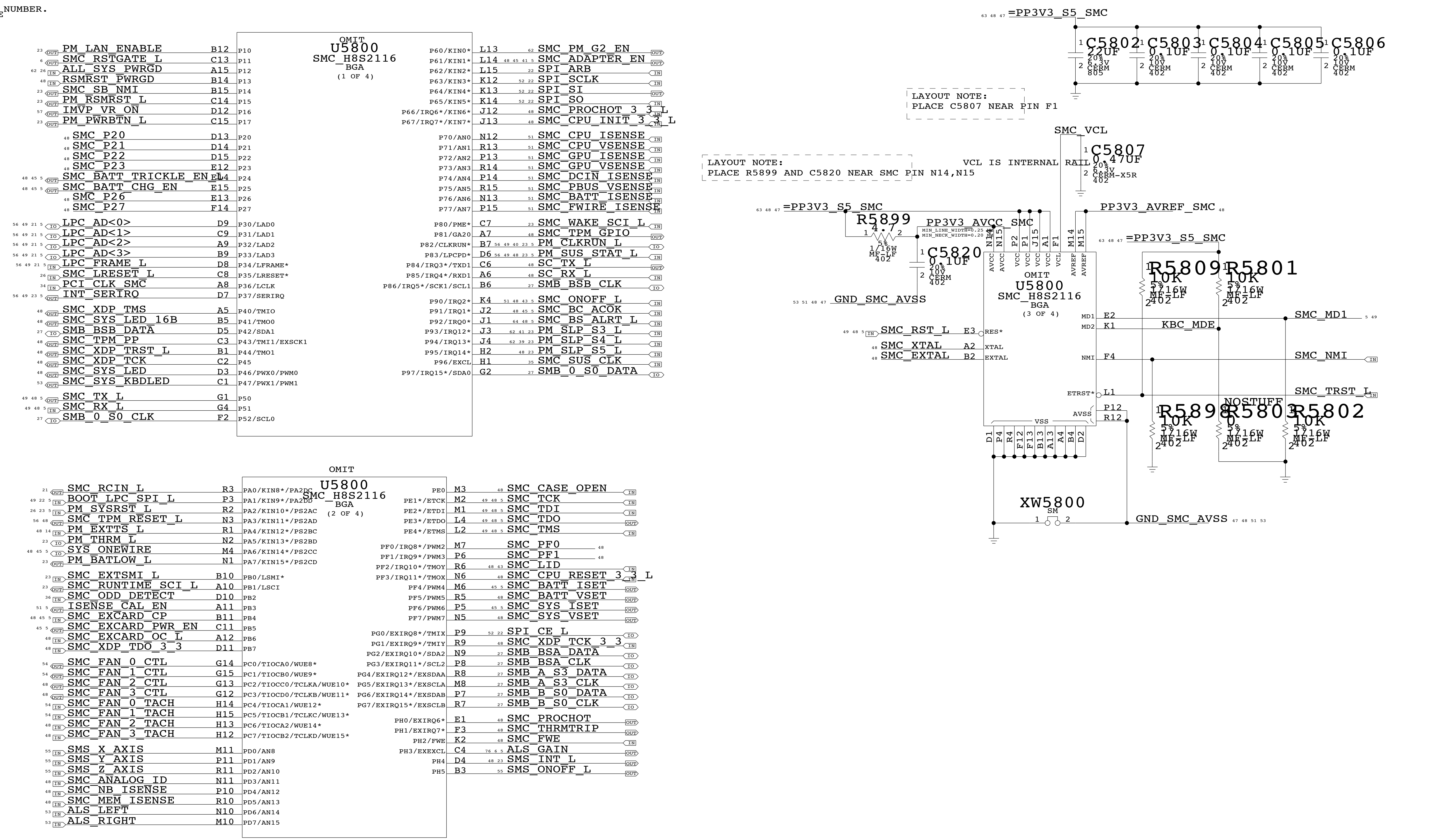
PCI-E Connections

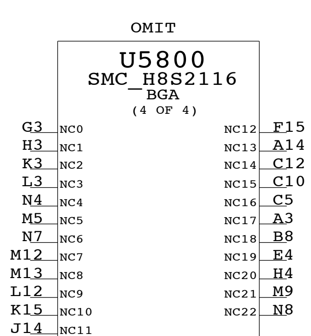
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 57 OF 104	

UNUSED PINS HAVE THE FORMAT SMC_XXX WHERE XXX IS THE PORT NUMBER. THEY ARE SET BY SOFTWARE TO BE DRIVEN OUTPUTS ALWAYS SO THEY CAN BE LEFT NO-CONNECTED.


OMIT
U5800
SMC_H8S2116
BGA
(1 OF 4)
PM_LAN_ENABLE B12 P10
SMC_RSTGATE_L C13 P11
ALL_SYS_PWRGD A15 P12
RSMRST_PWRGD B14 P13
SMC_SB_NMI B15 P14
PM_RSMRST_L C14 P15
IMVP_VR_ON D12 P16
PM_PWRBTN_L C15 P17
SMC_P20 D13 P20
SMC_P21 D14 P21
SMC_P22 D15 P22
SMC_P23 E12 P23
SMC_BATT_TRICKLE_EN_L E14 P24
SMC_BATT_CHG_EN E15 P25
SMC_P26 E13 P26
SMC_P27 F14 P27
LPC_AD<0> D9 P30/LAD0
LPC_AD<1> C9 P31/LAD1
LPC_AD<2> A9 P32/LAD2
LPC_AD<3> B9 P33/LAD3
LPC_FRAME_L D8 P34/LFRAME*
SMC_LRESET_L C8 P35/LRESET*
PCI_CLK_SMC A8 P36/LCLK
INT_SERIRQ D7 P37/SERIRQ
SMC_XDP_TMS A5 P40/TMI0
SMC_SYS_LED_16B B5 P41/TMO0
SMB_BSB_DATA D5 P42/SDA1
SMC_TPM_PP C3 P43/TMI1/EXSCK1
SMC_XDP_TRST_L B1 P44/TMO1
SMC_XDP_TCK C2 P45
SMC_SYS_LED D3 P46/PWX0/PWM0
SMC_SYS_KBDLED C1 P47/PWX1/PWM1
SMC_TX_L G1 P50
SMC_RX_L G4 P51
SMB_0_S0_CLK F2 P52/SCL0
P60/KIN0* L13 SMC_PM_G2_EN
P61/KIN1* L14 SMC_ADAPTER_EN
P62/KIN2* L15 SPI_ARB
P63/KIN3* K12 SPI_SCLK
P64/KIN4* K13 SPI_SI
P65/KIN5* K14 SPI_SO
P66/IRQ6*/KIN6* J12 SMC_PROCHOT_3_3_L
P67/IRQ7*/KIN7* J13 SMC_CPU_INIT_3_3_L
P70/AN0 N12 SMC_CPU_ISENSE
P71/AN1 R13 SMC_CPU_VSENSE
P72/AN2 P13 SMC_GPU_ISENSE
P73/AN3 R14 SMC_GPU_VSENSE
P74/AN4 P14 SMC_DCIN_ISENSE
P75/AN5 R15 SMC_PBUS_VSENSE
P76/AN6 N13 SMC_BATT_ISENSE
P77/AN7 P15 SMC_FWIRE_ISENSE
P80/PME* C7 SMC_WAKE_SCI_L
P81/GA20 A7 SMC_TPM_GPIO
P82/CLKRUN* B7 PM_CLKRUN_L
P83/LPCPD* D6 PM_SUS_STAT_L
P84/IRQ3*/TXD1 C6 SC_TX_L
P85/IRQ4*/RXD1 A6 SC_RX_L
P86/IRQ5*/SCK1/SCL1 B6 SMB_BSB_CLK
P90/IRQ2* K4 SMC_ONOFF_L
P91/IRQ1* J2 SMC_BC_ACOK
P92/IRQ0* J1 SMC_BS_ALRT_L
P93/IRQ12* J3 PM_SLP_S3_L
P94/IRQ13* J4 PM_SLP_S4_L
P95/IRQ14* H2 PM_SLP_S5_L
P96/EXCL H1 SMC_SUS_CLK
P97/IRQ15*/SDA0 G2 SMB_0_S0_DATA
=PP3V3_S5_SMC
C5802 22UF 20% 6.3V CERM 805
C5803 0.1UF 20% 10V CERM 402
C5804 0.1UF 20% 10V CERM 402
C5805 0.1UF 20% 10V CERM 402
C5806 0.1UF 20% 10V CERM 402
LAYOUT NOTE:
PLACE C5807 NEAR PIN F1
SMC_VCL
VCL IS INTERNAL RAIL
C5807 0.47UF 20% 6.3V CERM-X5R 402
LAYOUT NOTE:
PLACE R5899 AND C5820 NEAR SMC PIN N14,N15
=PP3V3_S5_SMC
R5899 4.7 5% 1/16W MF-LF 402
PP3V3_AVCC_SMC
MIN_LINE_WIDTH=0.25
MIN_NECK_WIDTH=0.20
C5820 0.1UF 20% 10V CERM 402
PP3V3_AVREF_SMC
=PP3V3_S5_SMC
GND_SMC_AVSS
OMIT
U5800
SMC_H8S2116
BGA
(3 OF 4)
R5809 10K 5% 1/16W MF-LF 402
R5801 10K 5% 1/16W MF-LF 402
MD1 E2 SMC_MD1
MD2 K1 KBC_MDE
SMC_RST_L E3 RES*
SMC_XTAL A2 XTAL
SMC_EXTAL B2 EXTAL
NMI F4 SMC_NMI
ETRST* L1 SMC_TRST_L
AVSS P12 R12
NOSTUFF
R5898 10K 5% 1/16W MF-LF 402
R5803 0 5% 1/16W MF-LF 402
R5802 10K 5% 1/16W MF-LF 402
XW5800 SM
GND_SMC_AVSS
OMIT
U5800
SMC_H8S2116
BGA
(2 OF 4)
SMC_RCIN_L R3 PA0/KIN8*/PA2DC
BOOT_LPC_SPI_L P3 PA1/KIN9*/PA2DD
PM_SYSRST_L R2 PA2/KIN10*/PS2AC
SMC_TPM_RESET_L N3 PA3/KIN11*/PS2AD
PM_EXTTS_L R1 PA4/KIN12*/PS2BC
PM_THRM_L N2 PA5/KIN13*/PS2BD
SYS_ONEWIRE M4 PA6/KIN14*/PS2CC
PM_BATLOW_L N1 PA7/KIN15*/PS2CD
SMC_EXTSMI_L B10 PB0/LSMI*
SMC_RUNTIME_SCI_L A10 PB1/LSCI
SMC_ODD_DETECT D10 PB2
ISENSE_CAL_EN A11 PB3
SMC_EXCARD_CP B11 PB4
SMC_EXCARD_PWR_EN C11 PB5
SMC_EXCARD_OC_L A12 PB6
SMC_XDP_TDO_3_3 D11 PB7
SMC_FAN_0_CTL G14 PC0/TIOCA0/WUE8*
SMC_FAN_1_CTL G15 PC1/TIOCB0/WUE9*
SMC_FAN_2_CTL G13 PC2/TIOCC0/TCLKA/WUE10*
SMC_FAN_3_CTL G12 PC3/TIOCD0/TCLKB/WUE11*
SMC_FAN_0_TACH H14 PC4/TIOCA1/WUE12*
SMC_FAN_1_TACH H15 PC5/TIOCB1/TCLKC/WUE13*
SMC_FAN_2_TACH H13 PC6/TIOCA2/WUE14*
SMC_FAN_3_TACH H12 PC7/TIOCB2/TCLKD/WUE15*
SMS_X_AXIS M11 PD0/AN8
SMS_Y_AXIS P11 PD1/AN9
SMS_Z_AXIS R11 PD2/AN10
SMC_ANALOG_ID N11 PD3/AN11
SMC_NB_ISENSE P10 PD4/AN12
SMC_MEM_ISENSE R10 PD5/AN13
ALS_LEFT N10 PD6/AN14
ALS_RIGHT M10 PD7/AN15
PE0 M3 SMC_CASE_OPEN
PE1*/ETCK M2 SMC_TCK
PE2*/ETDI M1 SMC_TDI
PE3*/ETDO L4 SMC_TDO
PE4*/ETMS L2 SMC_TMS
PF0/IRQ8*/PWM2 M7 SMC_PF0
PF1/IRQ9*/PWM3 P6 SMC_PF1
PF2/IRQ10*/TMOY R6 SMC_LID
PF3/IRQ11*/TMOX N6 SMC_CPU_RESET_3_3_L
PF4/PWM4 M6 SMC_BATT_ISET
PF5/PWM5 R5 SMC_BATT_VSET
PF6/PWM6 P5 SMC_SYS_ISET
PF7/PWM7 N5 SMC_SYS_VSET
PG0/EXIRQ8*/TMIX P9 SPI_CE_L
PG1/EXIRQ9*/TMIY R9 SMC_XDP_TCK_3_3
PG2/EXIRQ10*/SDA2 N9 SMB_BSA_DATA
PG3/EXIRQ11*/SCL2 P8 SMB_BSA_CLK
PG4/EXIRQ12*/EXSDAA R8 SMB_A_S3_DATA
PG5/EXIRQ13*/EXSCLA M8 SMB_A_S3_CLK
PG6/EXIRQ14*/EXSDAB P7 SMB_B_S0_DATA
PG7/EXIRQ15*/EXSCLB R7 SMB_B_S0_CLK
PH0/EXIRQ6* E1 SMC_PROCHOT
PH1/EXIRQ7* F3 SMC_THRMTRIP
PH2/FWE K2 SMC_FWE
PH3/EXEXCL C4 ALS_GAIN
PH4 D4 SMS_INT_L
PH5 B3 SMS_ONOFF_L

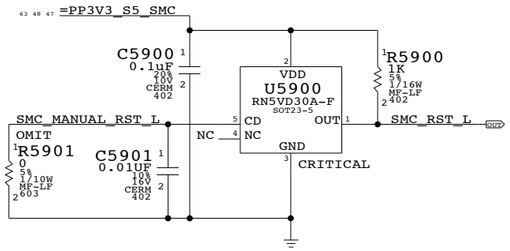


SMC

NOTICE OF PROPRIETARY PROPERTY

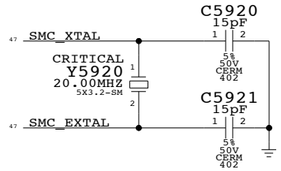
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7099	REV. D
	SCALE NONE	SHT 58	OF 104

SMC Reset Button / Brownout Detect

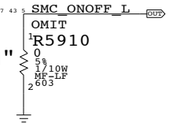


Silk: "SMC RST"

SMC Crystal Circuit

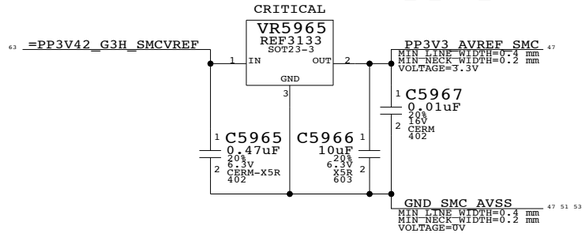


Debug Power Button

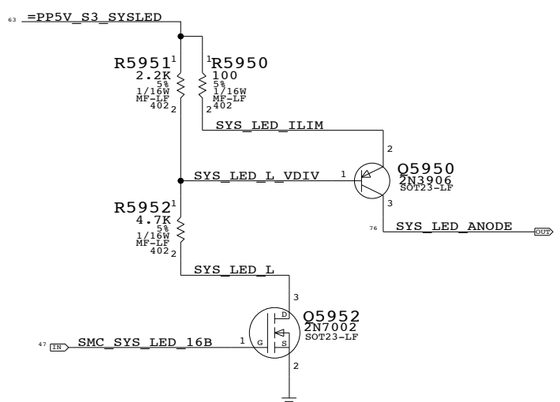


Silk: "PWR BTN"

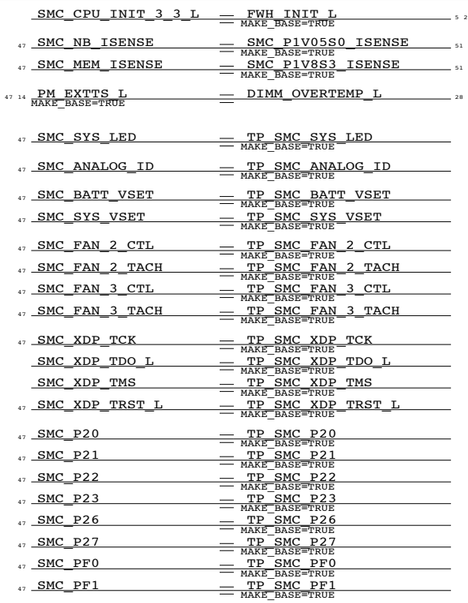
SMC AVREF Supply

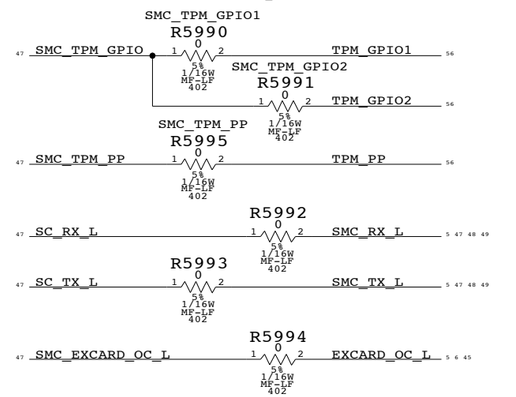


System (Sleep) LED Circuit



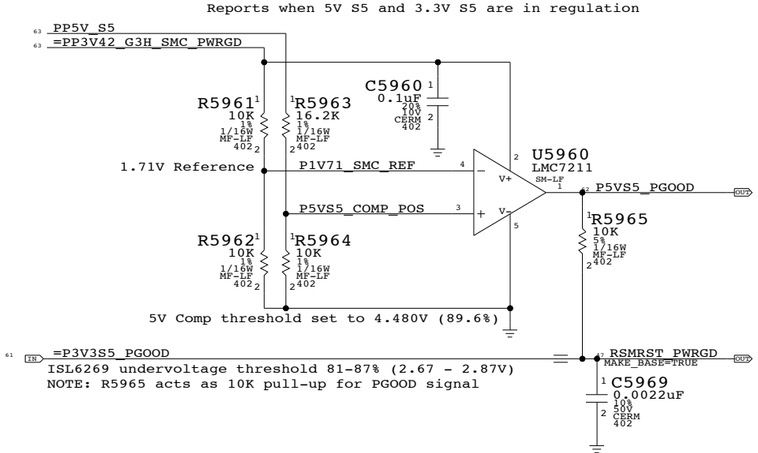
SMC_CPU_INIT_3_3_L



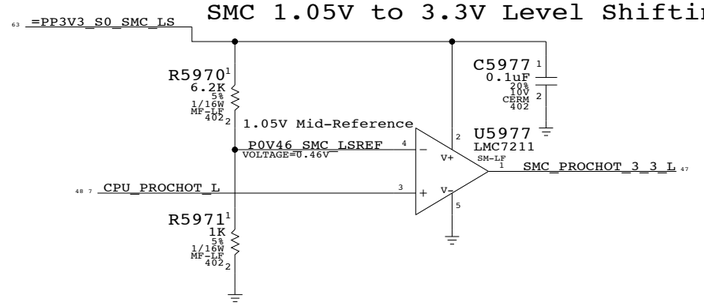


SMC PWRGD Circuit

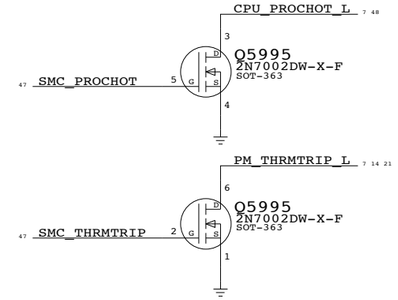
Reports when 5V S5 and 3.3V S5 are in regulation

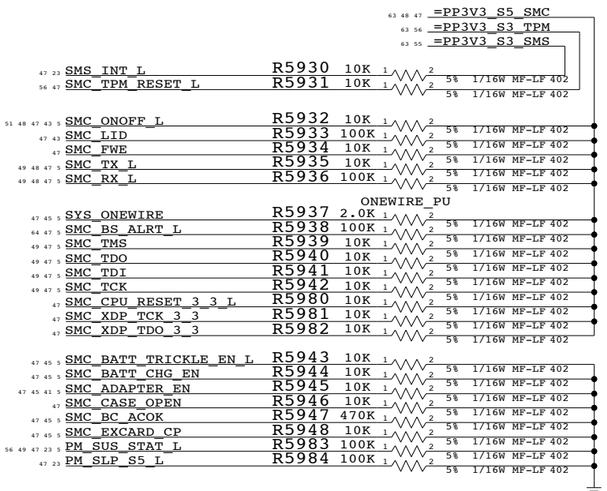


SMC 1.05V to 3.3V Level Shifting



SMC 3.3V to 1.05V Level Shifting

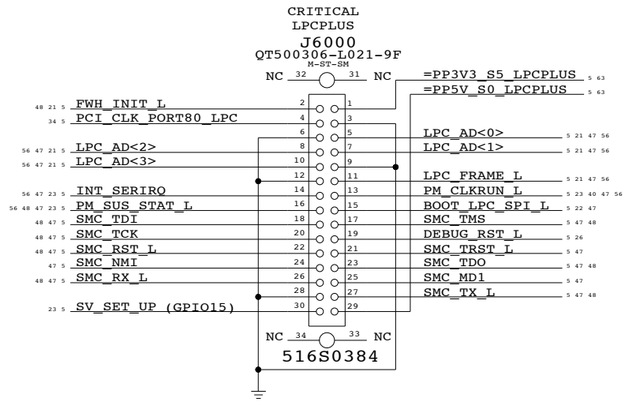




SMC Support

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7099	REV. D
	SCALE NONE	SHT 59 OF 104	



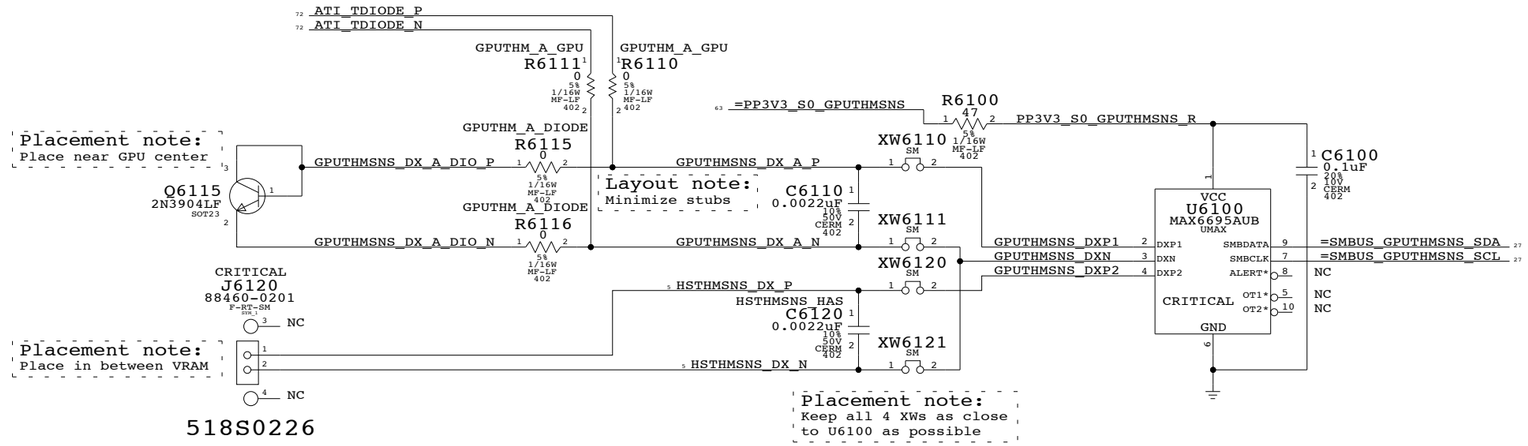
LPC+ Debug Connector

SYNC_MASTER=M42 SYNC_DATE=07/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 60 OF 104	

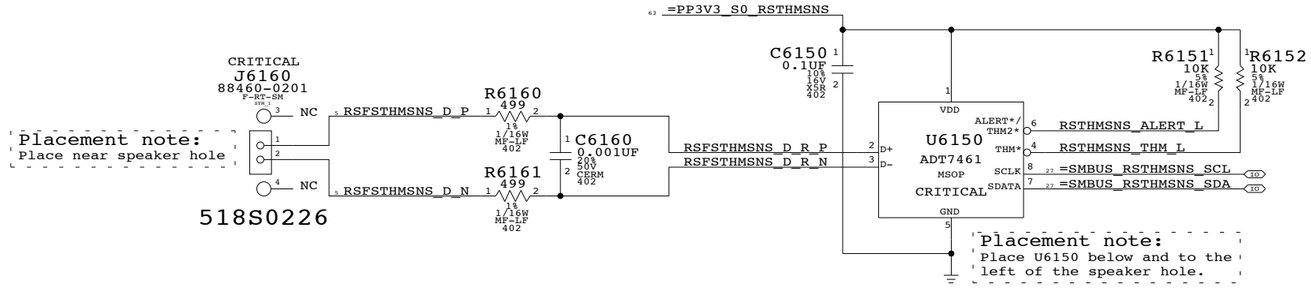
GPU / Heat Pipe Thermal Sensor



518S0226

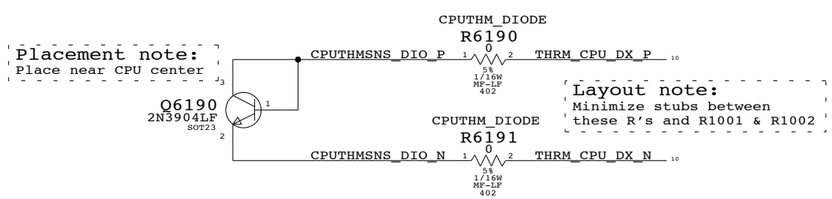
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,0,1/16W,0402	C6120		HSTHMSNS_NOT

Right-Side/Fin Stack Thermal Sensor



518S0226

CPU Back-Up Thermal Diode



R1001 / R1002 are not currently BOMOPTIONed. Can not programatically unstuff those parts to stuff these.

Thermal Sensors

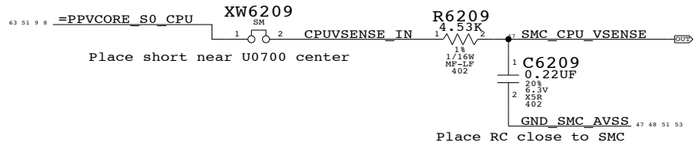
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE: NONE SHT 61 OF 104

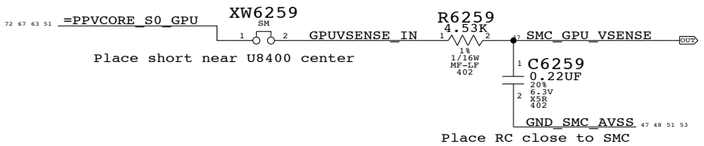
CPU Voltage Sense / Filter



Place short near U0700 center

Place RC close to SMC

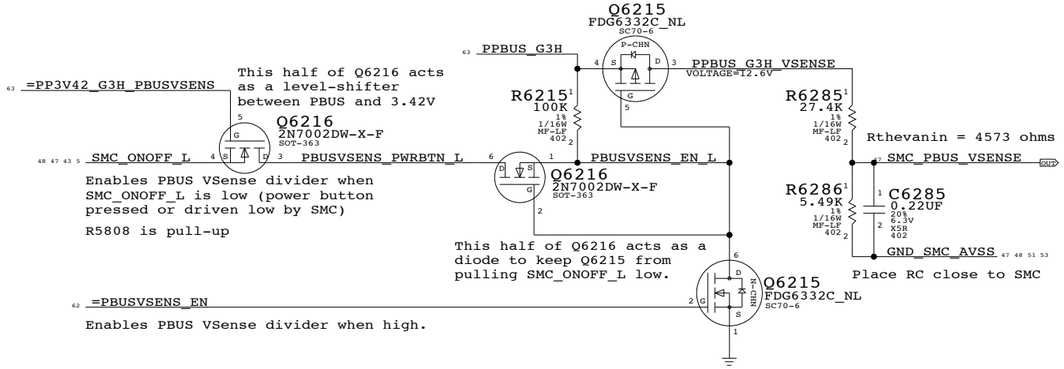
GPU Voltage Sense / Filter



Place short near U8400 center

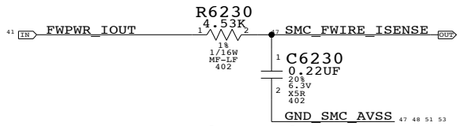
Place RC close to SMC

PBUS Voltage Sense Enable & Filter



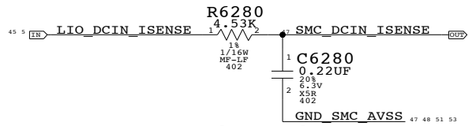
Place RC close to SMC

FireWire Current Sense Filter



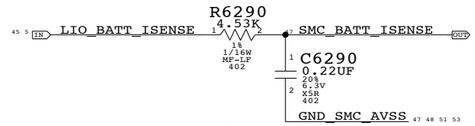
Place RC close to SMC

DCIN Current Sense Filter



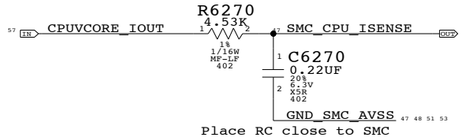
Place RC close to SMC

Battery Current Sense Filter



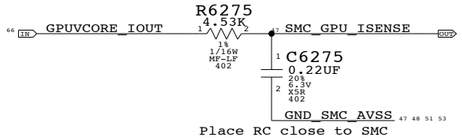
Place RC close to SMC

CPU Current Sense Filter



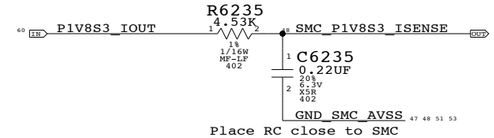
Place RC close to SMC

GPU Current Sense Filter



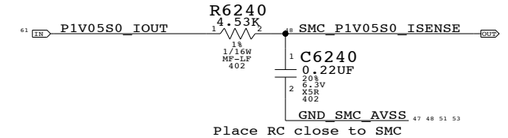
Place RC close to SMC

1.8V S3 (Memory) Current Sense Filter



Place RC close to SMC

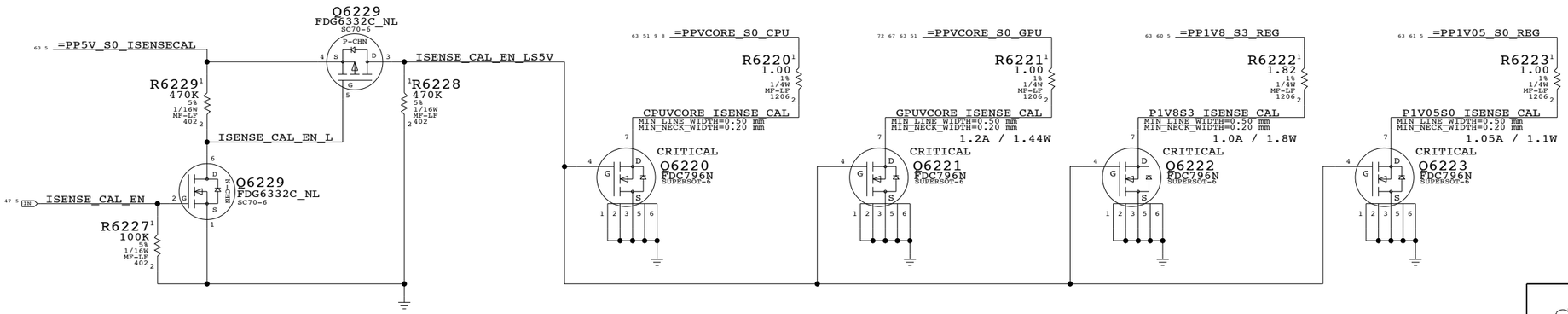
1.05V S0 (NB) Current Sense Filter



Place RC close to SMC

Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits

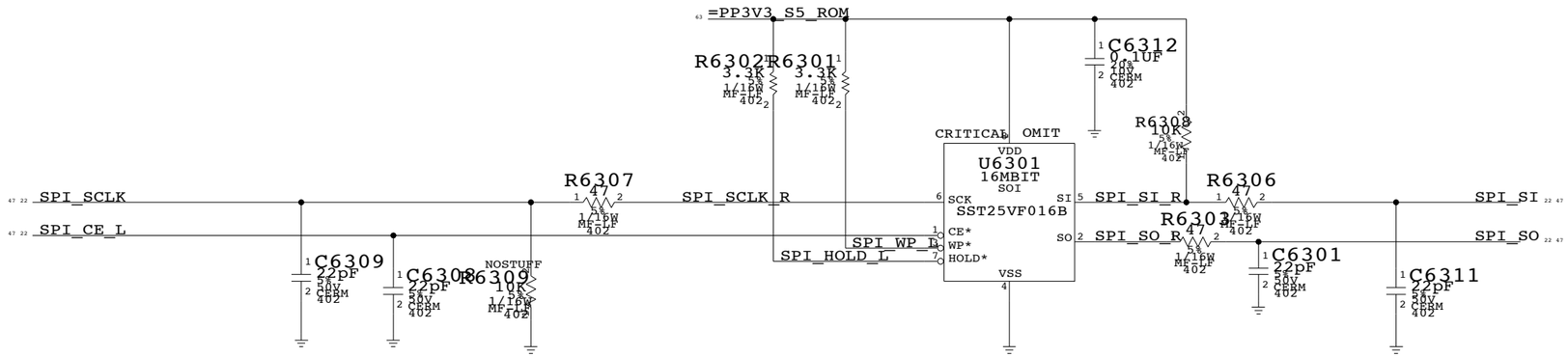


Current & Voltage Sensing

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 62 OF 104	



R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M

R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

SPI BOOTROM

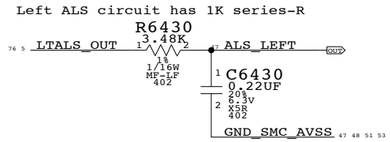
SYNC_MASTER=M87 SYNC_DATE=11/16/2005

APPLE COMPUTER INC.

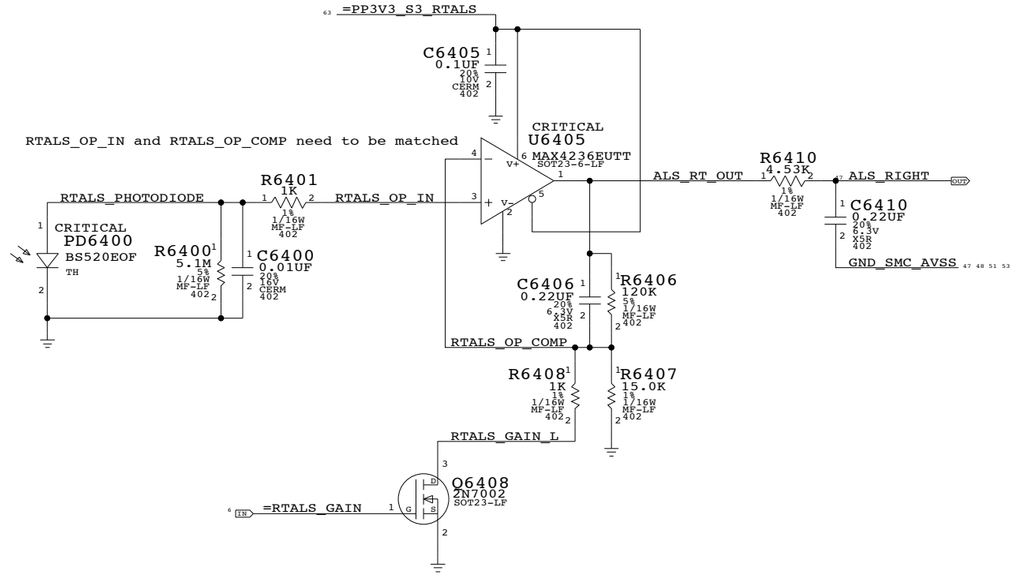
SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	63	104

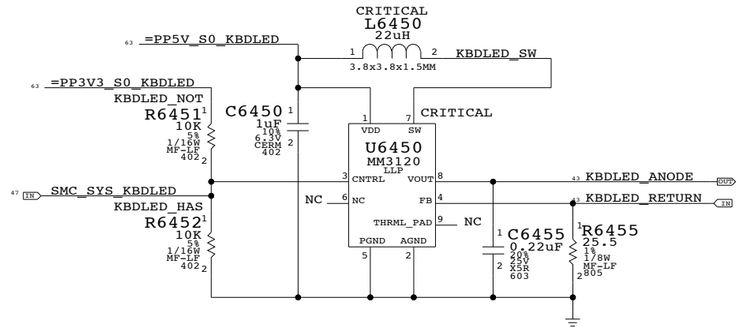
Left ALS Filter



Right ALS Circuit



Keyboard LED Driver



ALS Support

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

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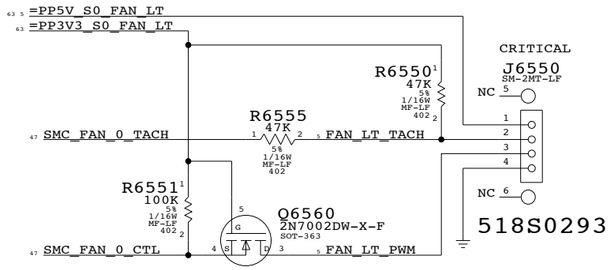
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

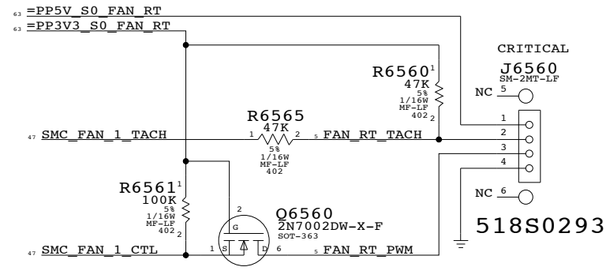
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 64 OF 104	

Left Fan



Right Fan



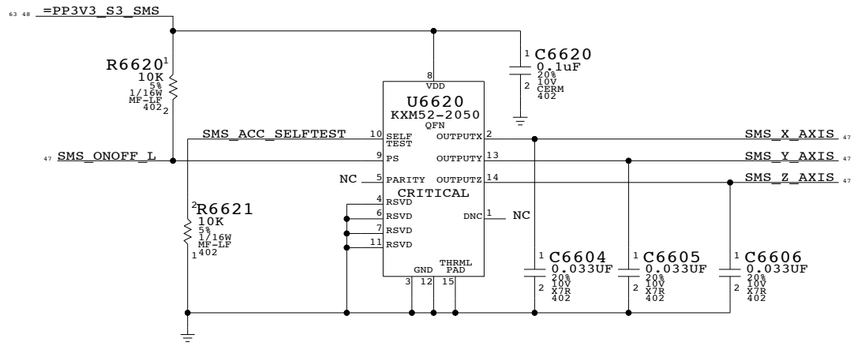
Fan Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

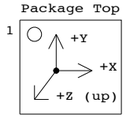
SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	65	104



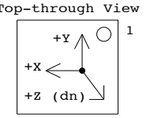
Desired orientation when placed on board top-side:

Package Top



Desired orientation when placed on board bottom-side:

Top-through View



M1 placement: Bottom-side

Sudden Motion Sensor (SMS)

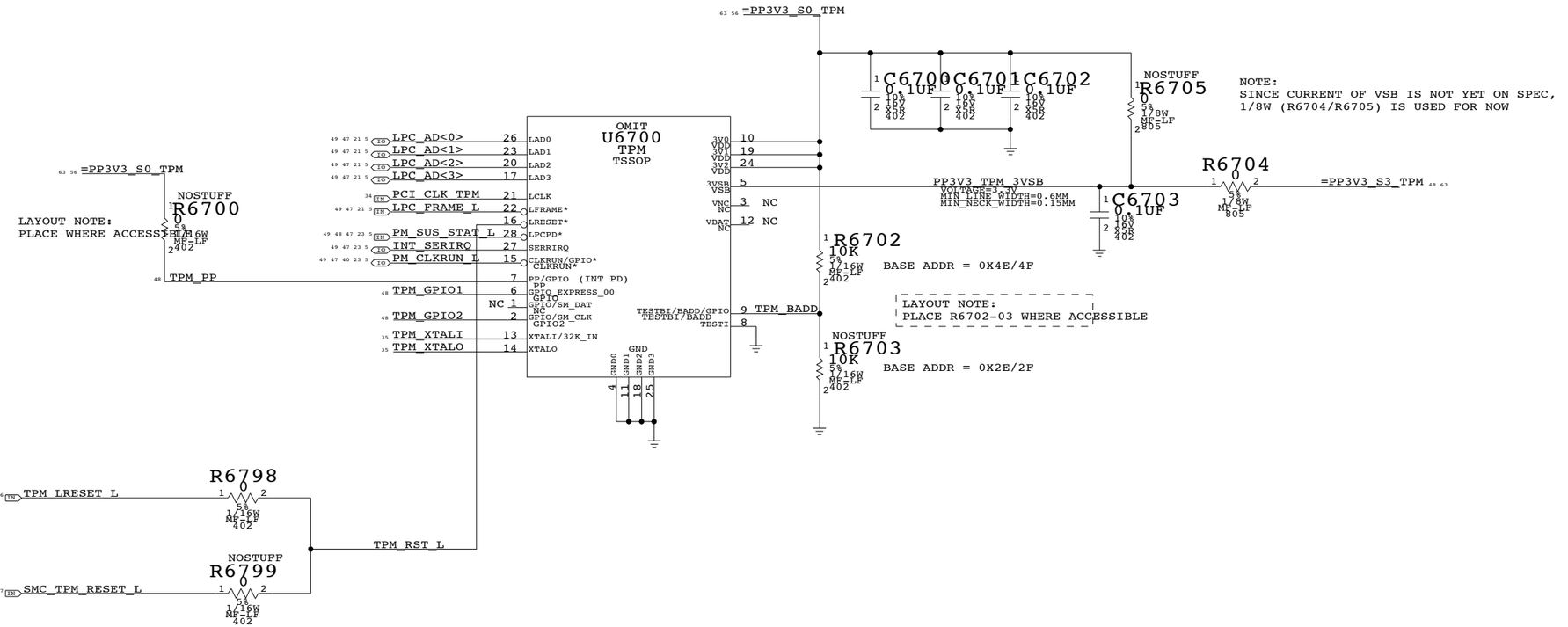
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE NONE

SHT 66 OF 104



TPM		
SYNC_MASTER=M38	SYNC_DATE=11/16/2005	

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7099	D
	SCALE: NONE	SHT 67 OF 104	

DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	1	0	1-Phase	DCM

These caps for Q7500

These caps for Q7550

=PPVOUT_S0_IMVP6_REG

Vout = Variable
36A max output
(Inductors limit)

CPU VCore Current Sense

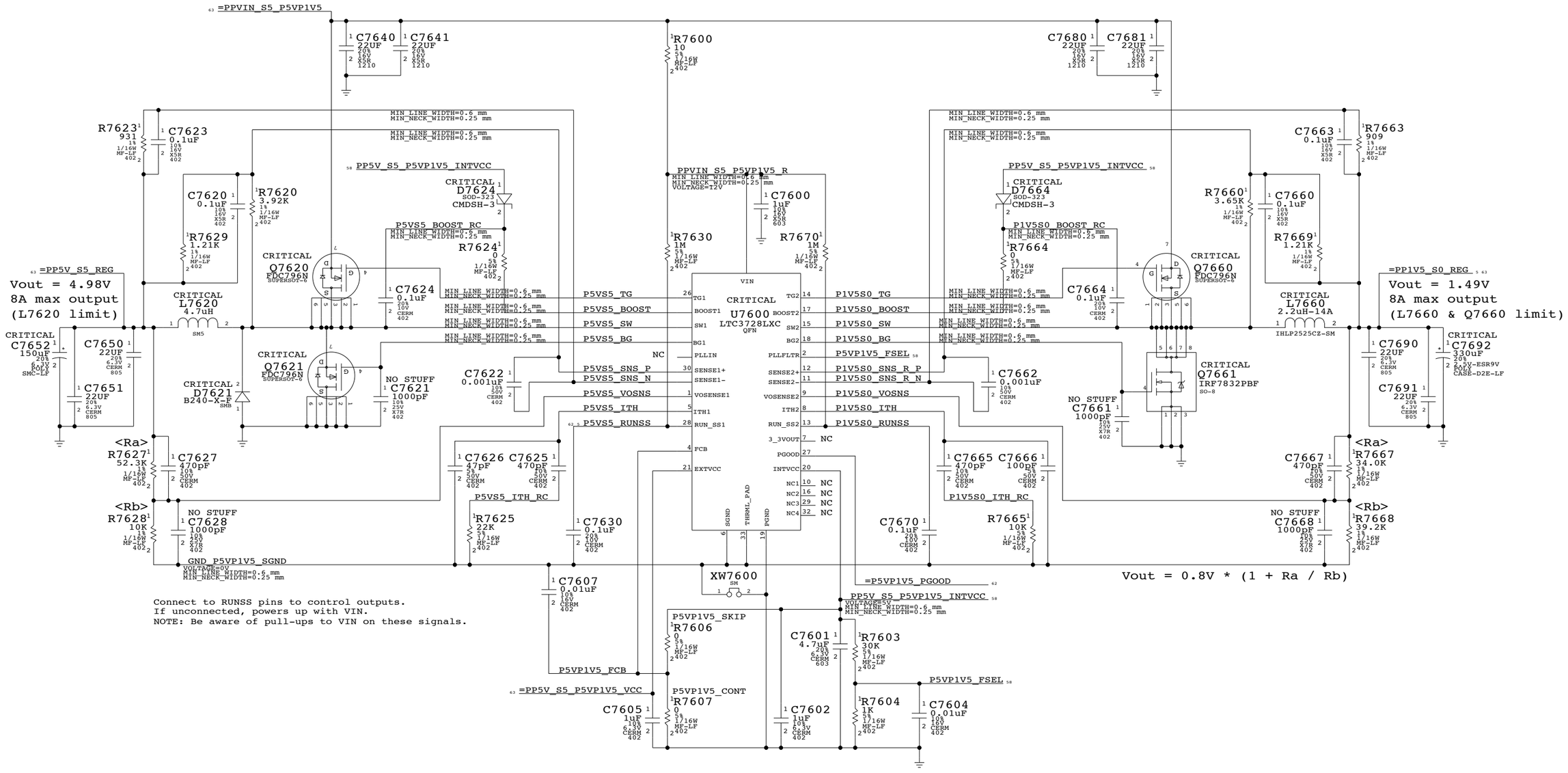
Vout = Gain * ((2.1 mV/A * Iload) + Voffset)
Voffset = (Vdrp_offset * Kdroop) + Vamp_offset
Gain = Rc / (Ra + Rb)
Voffset worst-case ~2.3mV (+/- ~1A offset)
Vout @ 36A = 2.44V-2.60V

IMVP6 CPU VCore Regulator

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 75 OF 104	



5V / 1.5V Power Supply

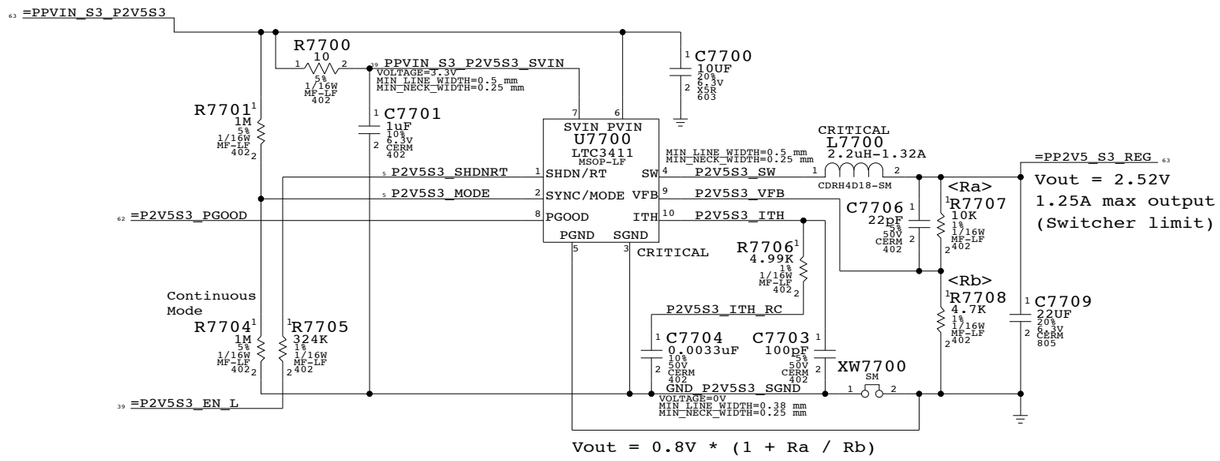
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

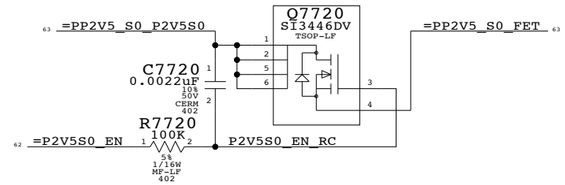
SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	76	104

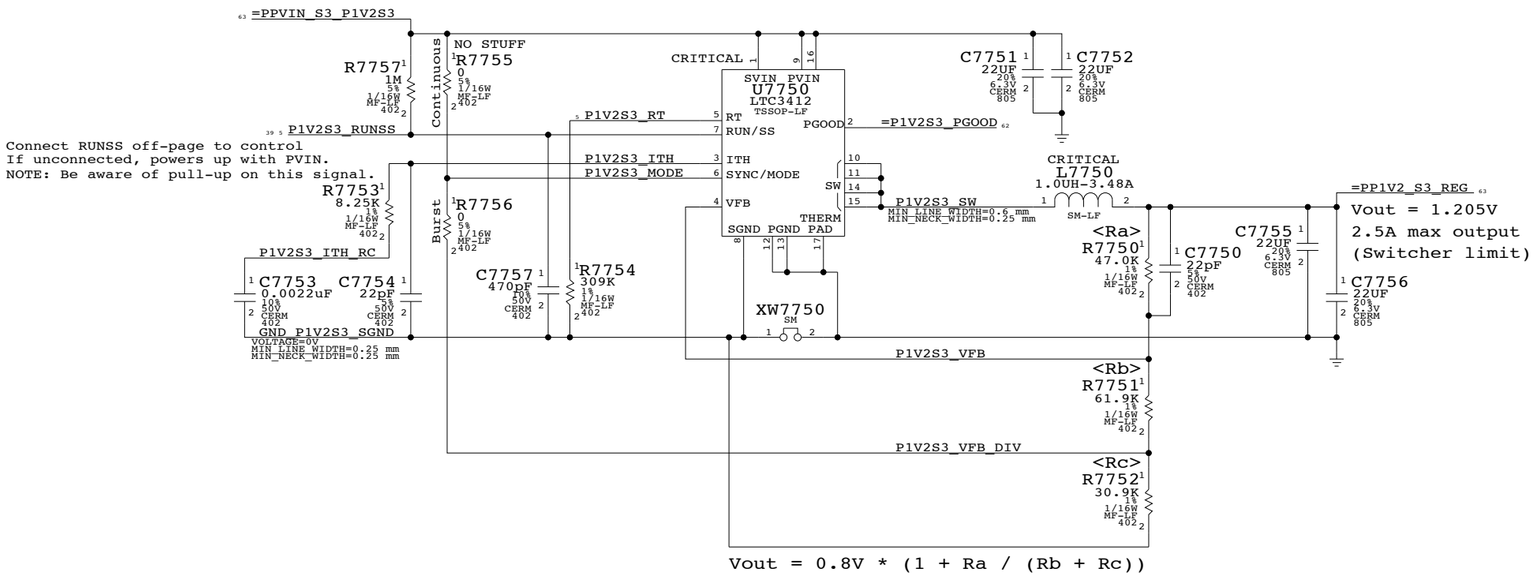
2.5V S3 Regulator



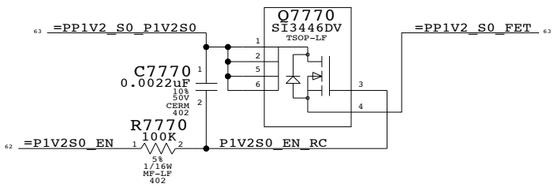
2.5V S0 FET



1.2V S3 Regulator



1.2V S0 FET



2.5V & 1.2V Regulators

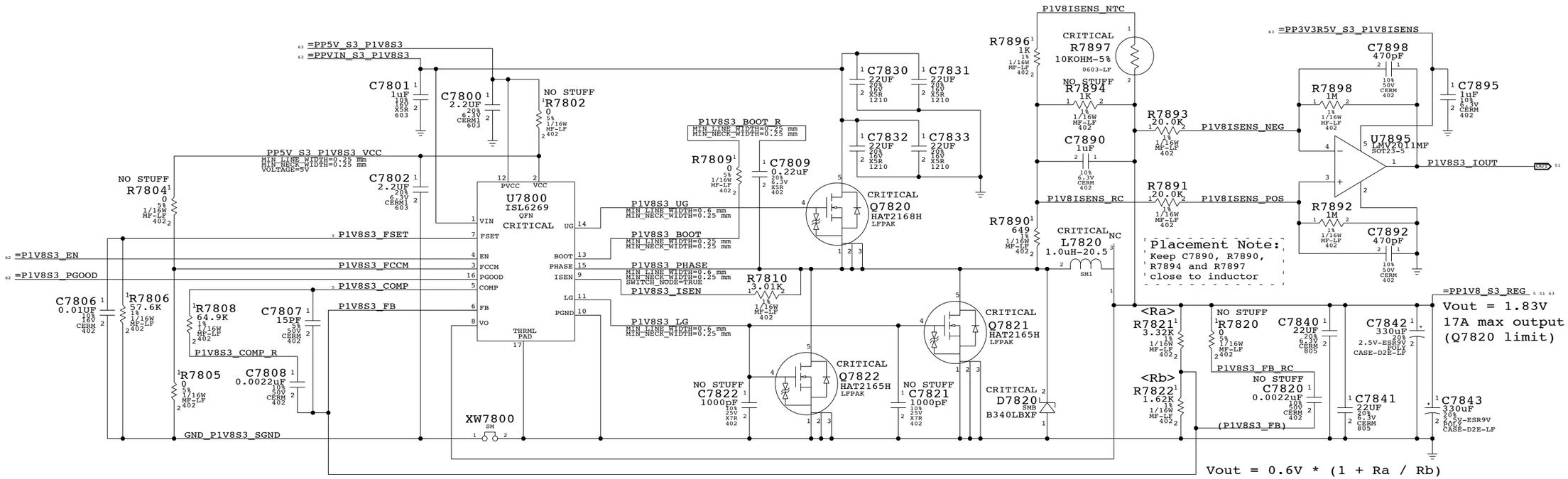
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

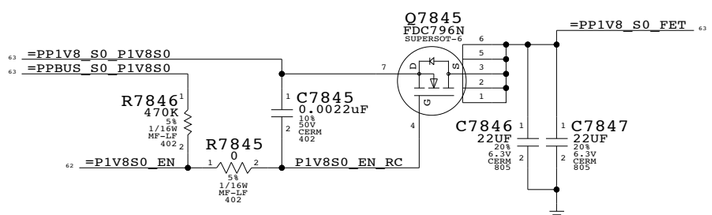
SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	77	104

1.8V S3 Current Sense



1.8V S0 FET



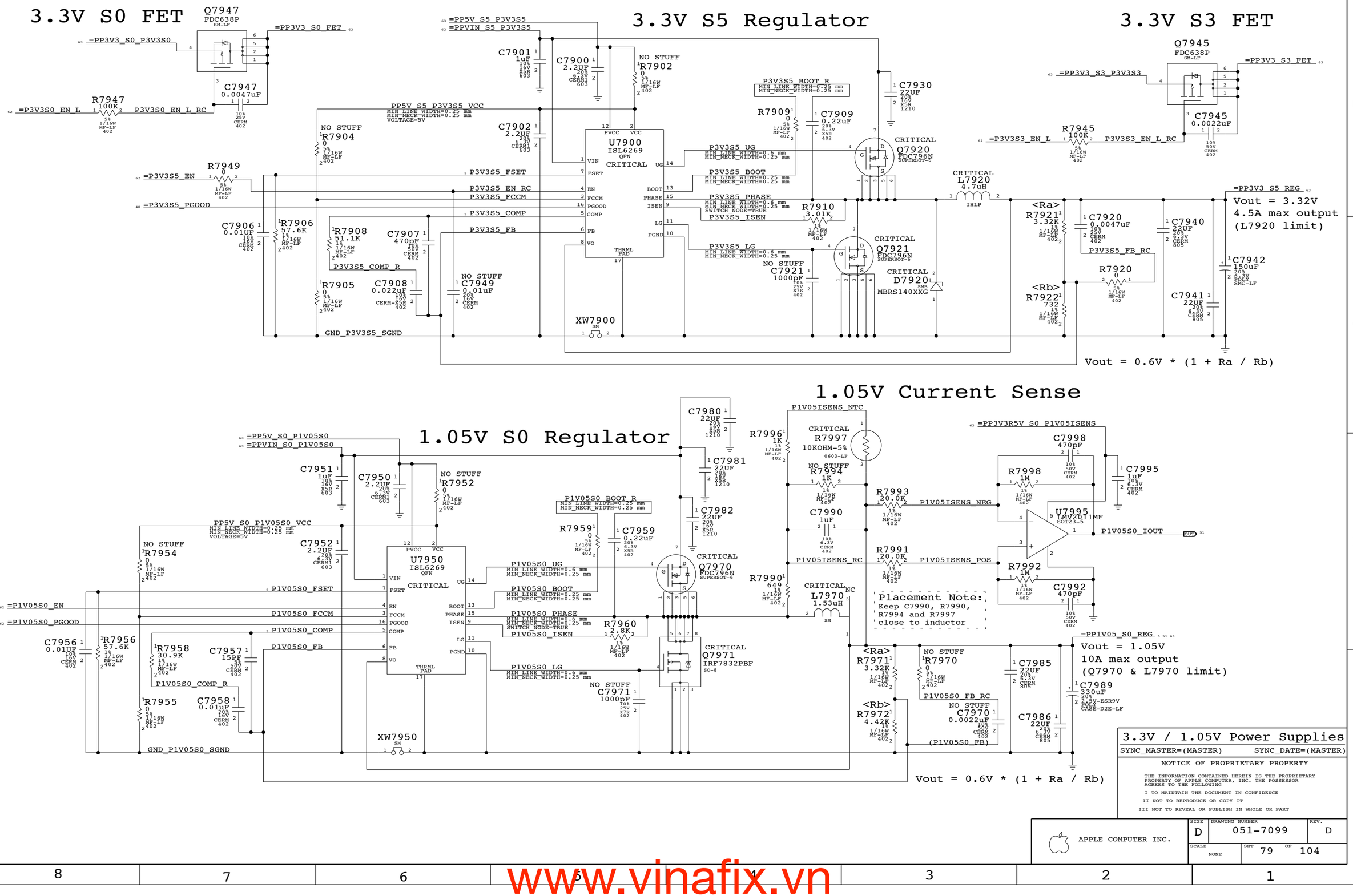
1.8V Supply

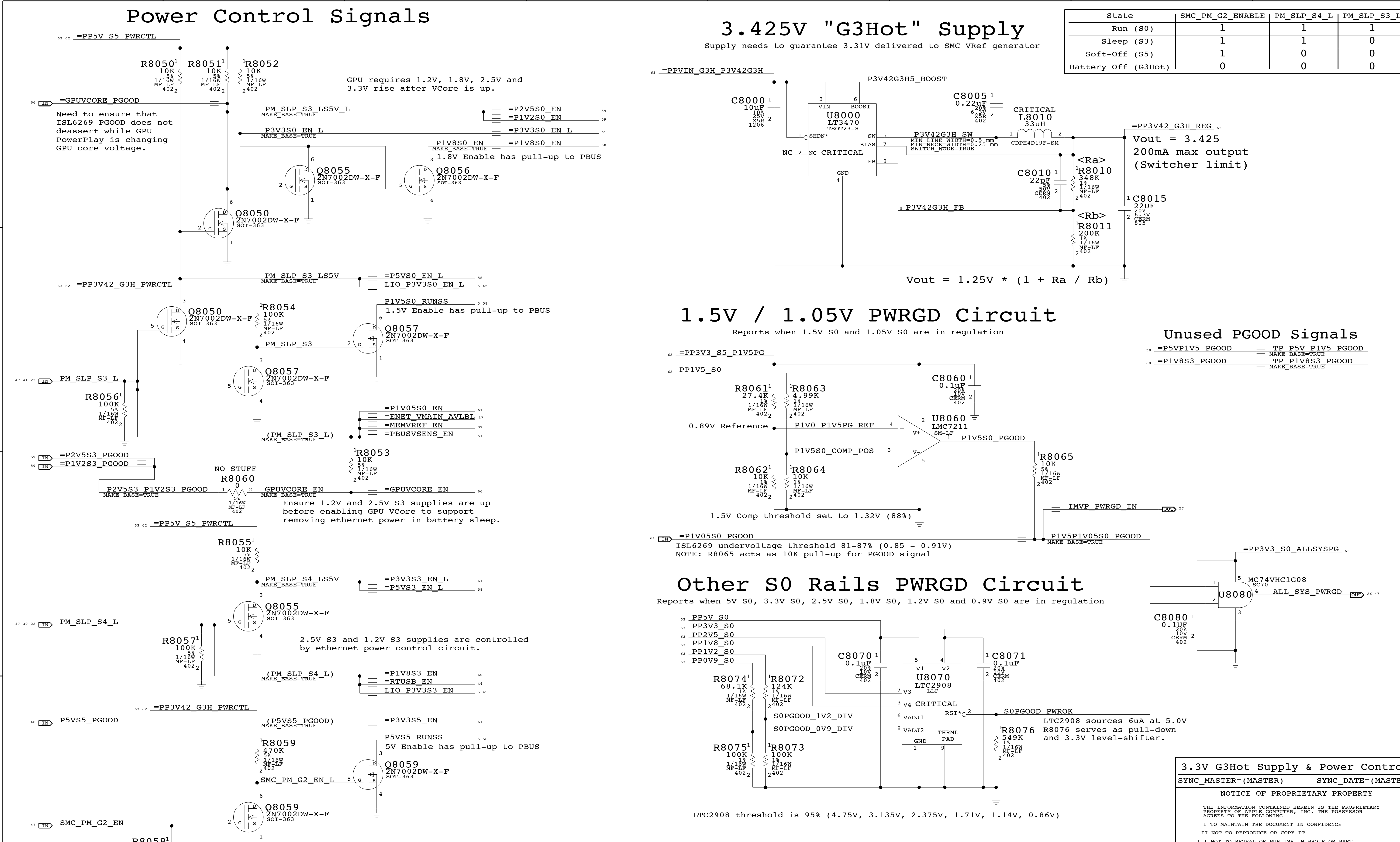
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	78	104





State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

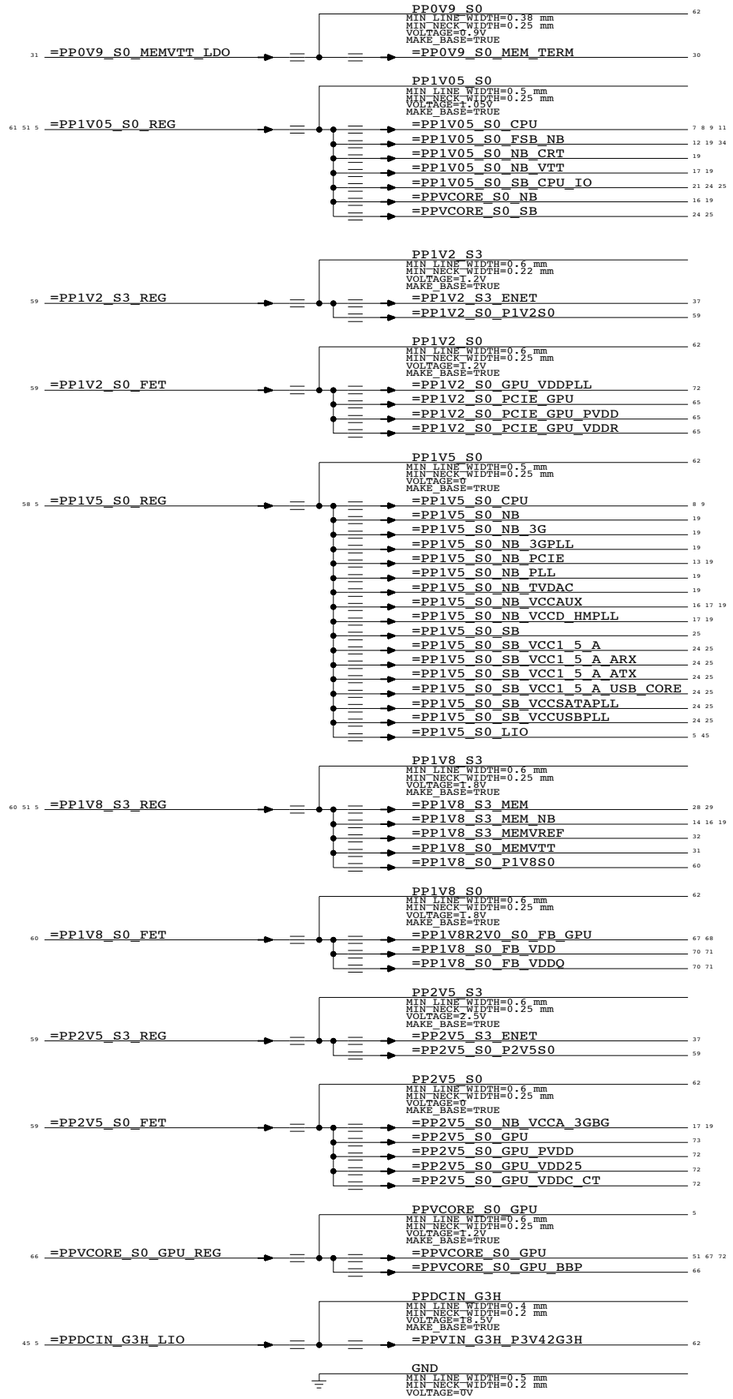
3.3V G3Hot Supply & Power Control

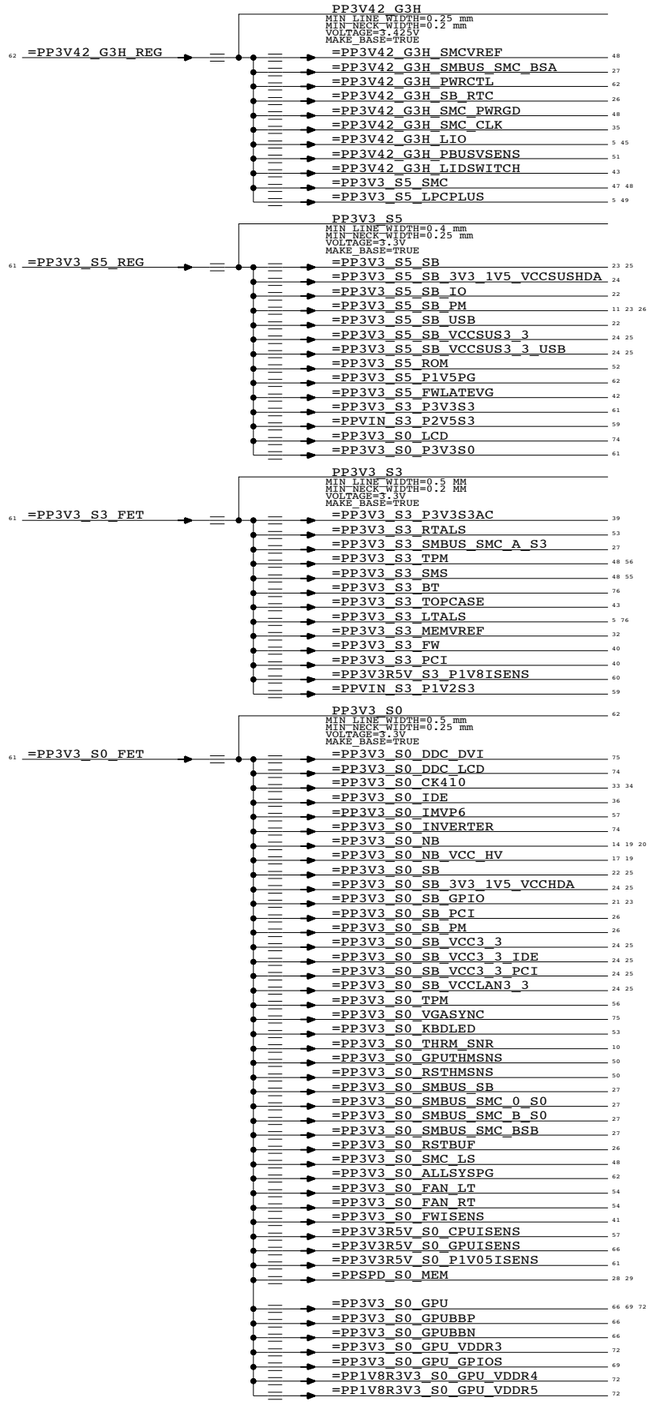
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

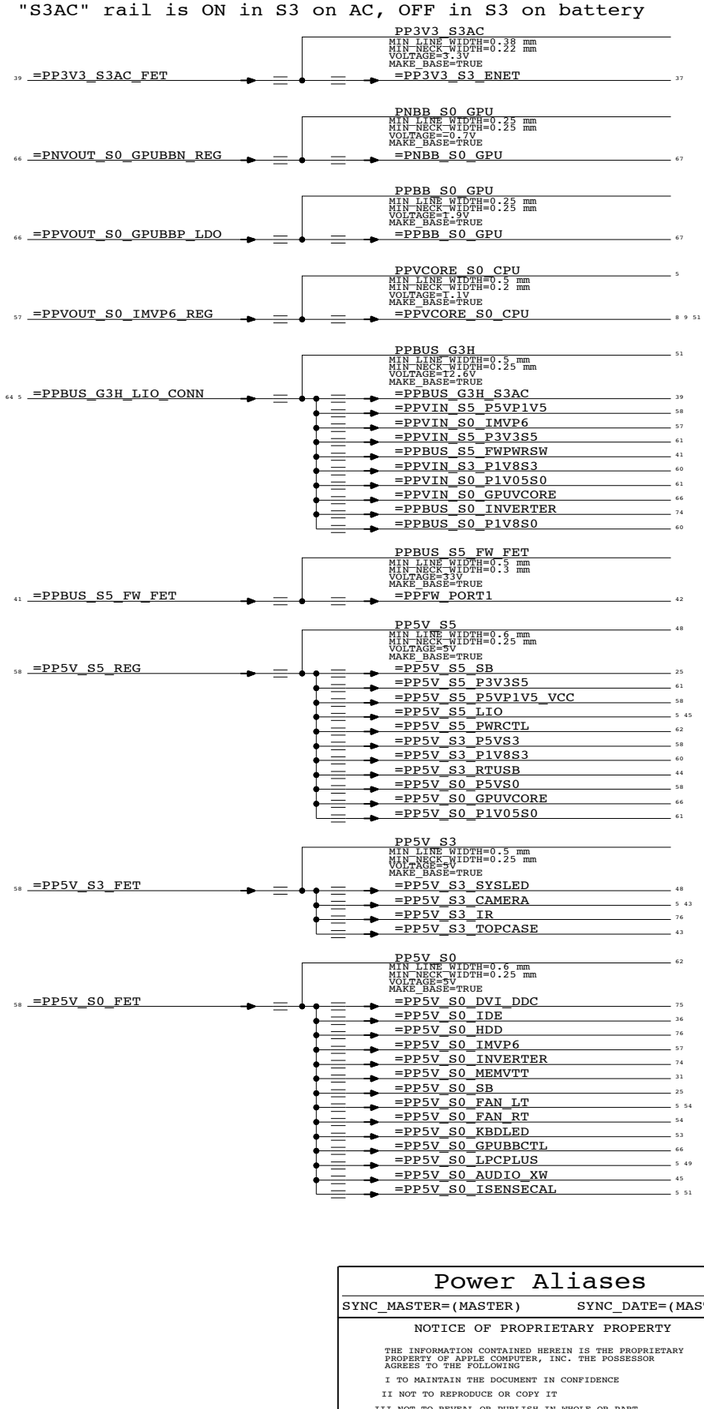
SIZE D | DRAWING NUMBER 051-7099 | REV. D

SCALE NONE | SHT 80 OF 104





"S3AC" rail is ON in S3 on AC, OFF in S3 on battery



Power Aliases

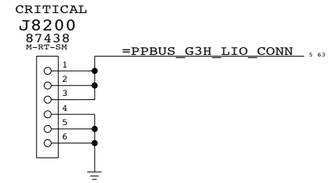
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

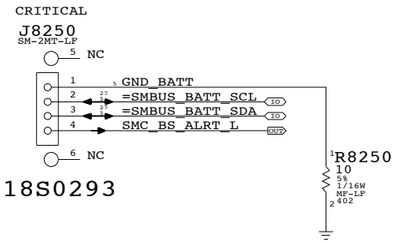
SCALE	SHT	OF
NONE	81	104

Left I/O Power Connector



518S0368

Battery Connector (Digital Signals)



518S0293

PBus-In & Battery Connectors

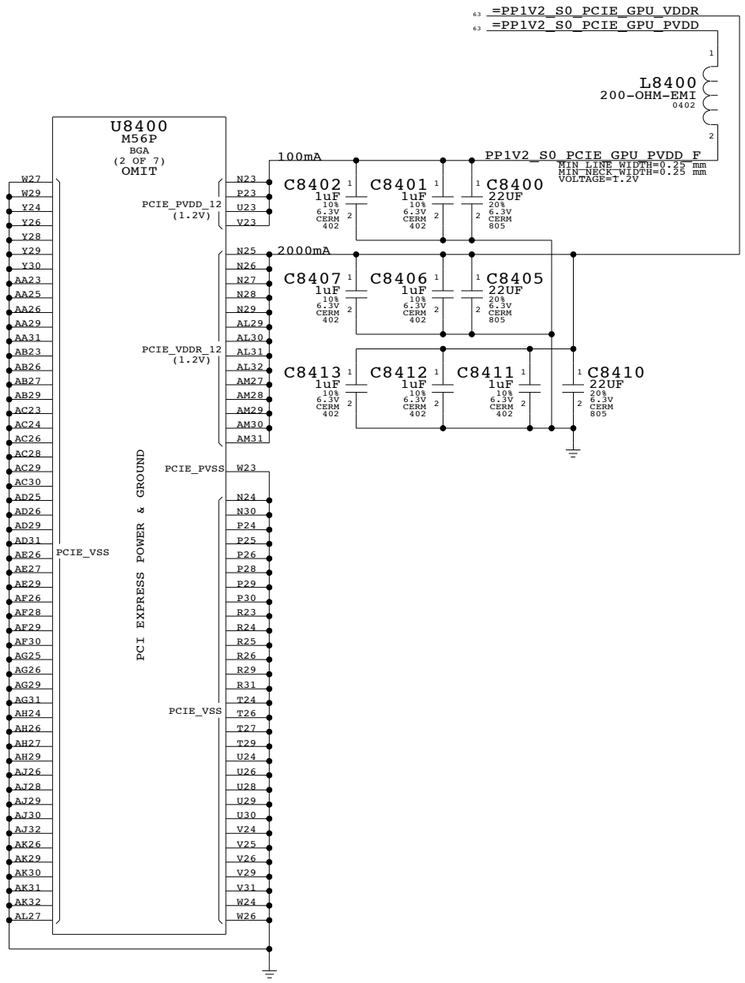
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

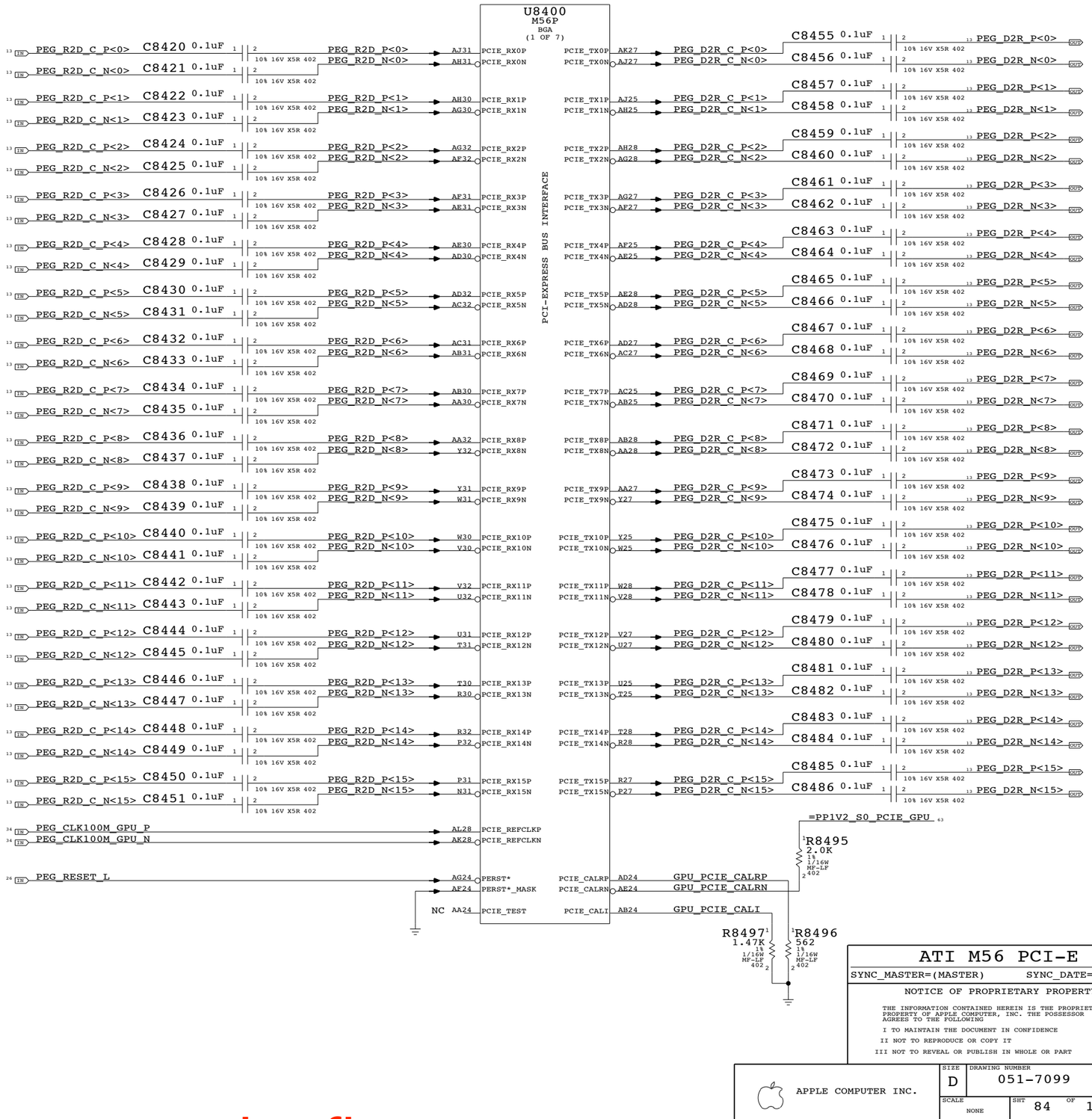
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE NONE

SHT 82 OF 104





ATI M56 PCI-E

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

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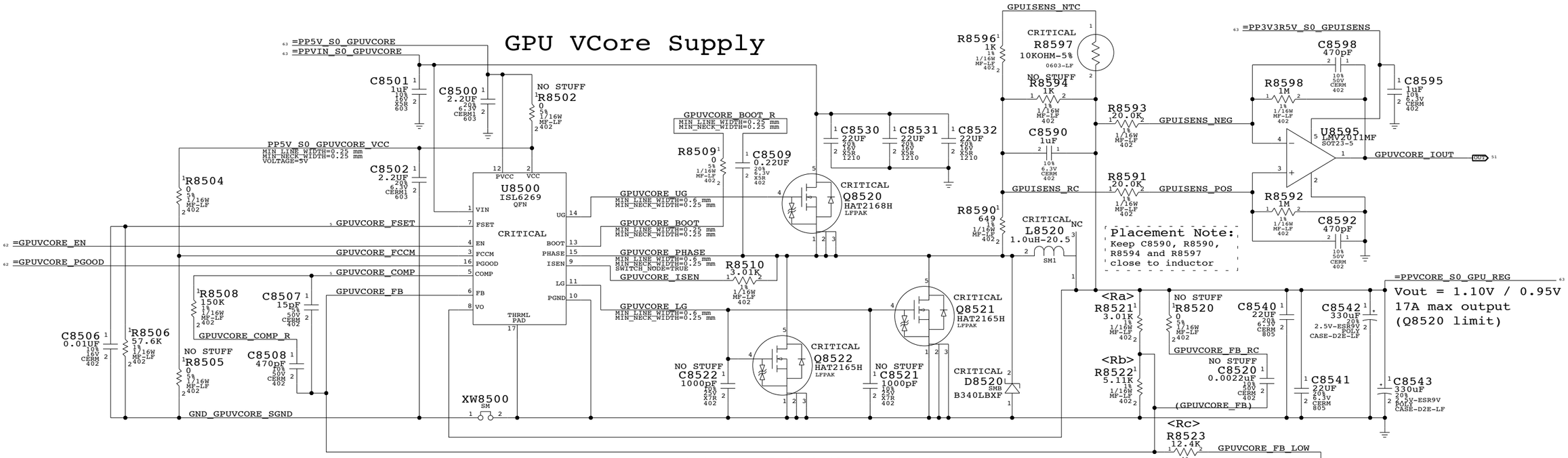
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	84	104

GPU VCore Supply

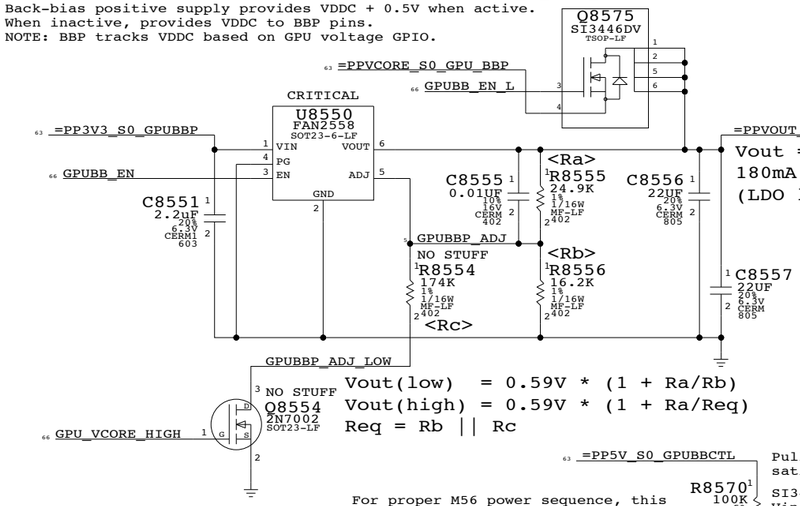


Vout(low) = 0.6V * (1 + Ra / Rb)
Vout(high) = 0.6V * (1 + Ra / Req)
Req = Rb || Rc

GPU VCore Current Sense

Back-Bias Positive Supply

Back-bias positive supply provides VDDC + 0.5V when active.
When inactive, provides VDDC to BBP pins.
NOTE: BBP tracks VDDC based on GPU voltage GPIO.



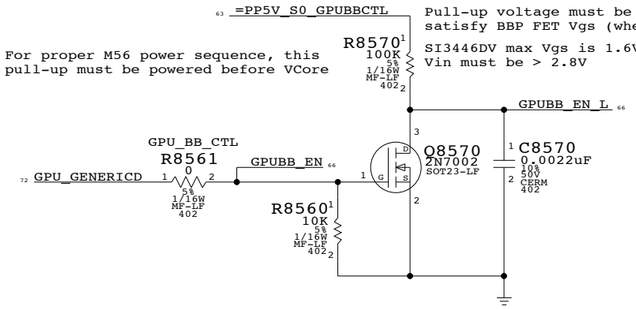
Vout(low) = 0.59V * (1 + Ra/Rb)
Vout(high) = 0.59V * (1 + Ra/Req)
Req = Rb || Rc

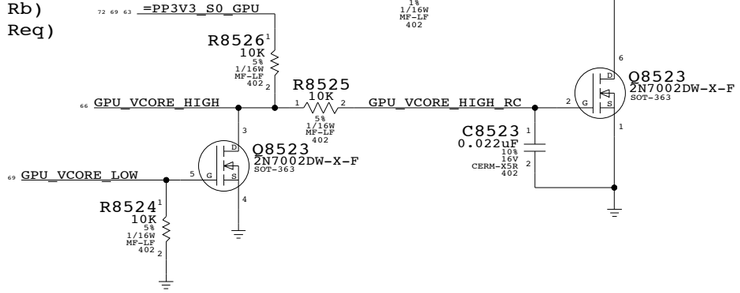
=PP5V_S0_GPUBBCTL

Pull-up voltage must be high enough to satisfy BBP FET Vgs (where Vs = 1.2V)

SI3446DV max Vgs is 1.6V
Vin must be > 2.8V

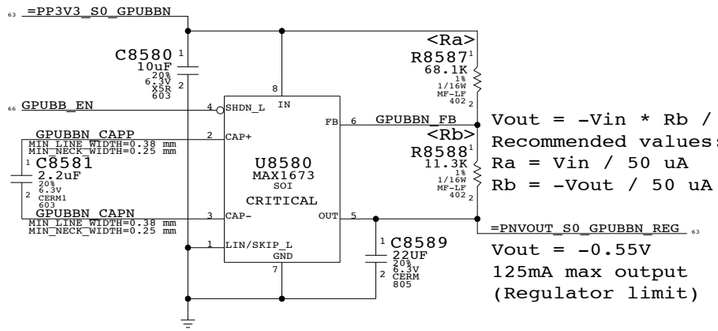
For proper M56 power sequence, this pull-up must be powered before VCore





Back-Bias Negative Supply

Back-bias negative supply provides VSS - 0.55V when active.
When inactive, provides VSS to BBN pins.



GPU (M56) Core Supplies		
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)	
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7099 REV. D
	SCALE NONE	SHT 85 OF 104

Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

63 =PPBB_S0_GPU 100mA (Preliminary)

C8690 22UF 20% 6.3V CERM 805
C8691 1uF 10% 6.3V CERM 402
C8692 0.1uF 10% 16V X5R 402

72 63 51 =PPVCORE_S0_GPU 14.2A @ 445/452MHz Core/Mem Clk for VDDC+VDDCI

C8600 22UF 20% 6.3V CERM 805
C8601 22UF 20% 6.3V CERM 805
C8604 C8605 C8606 C8607 C8608 C8609 C8610 1uF 10% 6.3V CERM 402
C8611 C8612 C8613 C8614 C8615 C8616 1uF 10% 6.3V CERM 402

R8630 0 5% 1/10W MF-LF 603

PPVCORE_S0_GPU_VDDCI
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm

C8630 22UF 20% 6.3V CERM 805
C8631 C8632 C8633 C8634 1uF 10% 6.3V CERM 402

68 63 =PP1V8R2V0_S0_FB_GPU 2.0A @ 500MHz 1.8V GDDR3

C8650 C8651 C8652 C8653 22UF 20% 6.3V CERM 805
C8655 C8656 C8657 C8658 C8659 C8660 C8661 C8662 C8663 C8664 C8665 C8666 C8667 C8668 C8669 C8670 C8671 C8672 C8673 C8674 C8675 C8676 C8677 C8678 C8679 C8680 C8681 C8682 C8683 1uF 10% 6.3V CERM 402

U8400
M56P
BGA
(7 OF 7)
OMIT

MEMORY & CORE POWER / GROUND

VDDC (1.0V/1.2V): K18 M23 V10 AC14 P14 P18 P19 R15 R17 R18 R19 T16 T17 T18 U15 U16 U17 V14 V15 V16 V18 W14 W15 W19 AC11 AC12 AD11
VDDCI (1.0V/1.2V): K14 P16 T14 T23 U19 W10 W17
VDDR1 (1.8V/2.0V): A3 A9 A12 A15 A18 A21 A24 A30 C1 C32 F32 H13 H19 J1 J10 J11 J13 J18 J19 J20 J32 K11 K13 K19 K20 K21 K24 L23 L24 L32 M1 M10 N9 N10 P8 P9 P10 R1 R9 V1 Y8 Y9 Y10 AA1
VSS: K23 A2 A8 A11 A13 A16 A19 A22 A25 A31 B1 B32 C4 C5 C6 C9 C10 C15 C18 C20 C21 C24 C27 D11 D30 E5 E8 E9 E12 E13 E16 E19 E25 E28 E30 E32 F3 F6 F10 F13 F15 F16 F18 F19 F21 F22 F24 F27 F30 G13 G16 G19 G20 G21 G22 G25 H1 H5 H7 H16 H20 H21 H28 H32 J3 J6 J9 J12 J16 J21 J24 J28 J30 K10 K12 K16 K17 K27 K30 L1 L6 L7 L29 M3
BBP: K15 R10 Y23 AC17
BBN: M6 M7 M8 M9 M24 M28 M32 N3 N7 N8 P1 P5 P6 P7 P15 P17 R3 R6 R14 R16 T10 T15 T19 U1 U5 U6 U7 U8 U9 U10 U14 U18 V3 V6 V17 V19 W16 W18 Y1 Y5 Y6 Y7 AA4 AA6 AC9 AC10 AD6 AD7 AD8 AD9 AD10 AD13 AD14 AD15 AD16 AD17 AE8 AE14 AE15 AE16 AE17 AF14 AF16 AG11 AG16 AG23 AH10 AH11 AH16 AJ10 AK16 AL1 AL13 AM2 AM13

C8697 0.1uF 10% 16V X5R 402
C8696 1uF 10% 6.3V CERM 402
C8695 22UF 20% 6.3V CERM 805

100mA (Preliminary) =PNBB_S0_GPU 63

ATI M56 Core Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

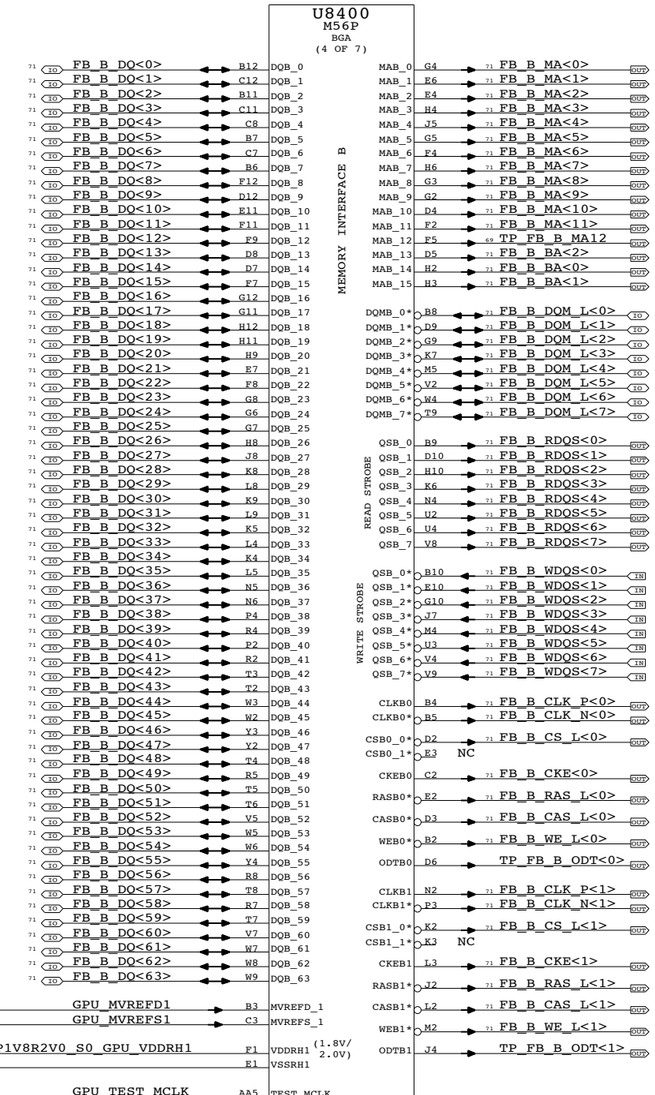
SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 86 OF 104	

Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	87	104

	Serial ROM	TestBus	Misc	Straps
GPU_GPIO_0	IPD	TESTIN[0]		TX_PWRS_ENb
GPU_GPIO_1	IPD	TESTIN[1]		TX_DEEMPH_EN
GPU_GPIO_2	VDD_VCL	TESTIN[2]		Reserved
GPU_GPIO_3		TESTIN[3]		Reserved
GPU_GPIO_4	IPD	TESTIN[4]		DEBUG_ACCESS
GPU_GPIO_5		TESTIN[5]		Reserved
GPU_GPIO_6		TESTIN[6]		Reserved
GPU_GPIO_7	ENA_BL	TESTIN[7]		
GPU_GPIO_8	ROMSO	TESTWR		Reserved
GPU_GPIO_9	IPD ROMSI			ROMIDCFG[3]
GPU_GPIO_10	ROMSCK	TESTOUT[8]		
GPU_GPIO_11	IPD	TESTOUT[9]		ROMIDCFG[0]
GPU_GPIO_12	IPD	TESTOUT[10]		ROMIDCFG[1]
GPU_GPIO_13	IPD	TESTOUT[11]		ROMIDCFG[2]
GPU_GPIO_14		TESTIN[8]		
GPU_GPIO_15		TESTIN[9]	PWRCNTL	
GPU_GPIO_16			SS_IN	
GPU_GPIO_17			Thm Mon Int	

GPU_GPIO_18 == NC_GPU_GPIO_18 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_19 == NC_GPU_GPIO_19 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_20 == NC_GPU_GPIO_20 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_21 == NC_GPU_GPIO_21 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_22 == NC_GPU_GPIO_22 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_23 == NC_GPU_GPIO_23 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_24 == GPU_MEM_256M (MAKE_BASE=TRUE)
GPU_GPIO_25 == NC_GPU_GPIO_25 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_26 == NC_GPU_GPIO_26 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_27 == GPU_MEMID (MAKE_BASE=TRUE)
GPU_GPIO_28 == NC_GPU_GPIO_28 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_29 == NC_GPU_GPIO_29 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_30 == NC_GPU_GPIO_30 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_31 == NC_GPU_GPIO_31 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_32 == NC_GPU_GPIO_32 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_33 == NC_GPU_GPIO_33 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_34 == NC_GPU_GPIO_34 (MAKE_BASE=TRUE, NO_TEST=TRUE)

63 =PP3V3_S0_GPU_GPIOS

R8800 1 10K 5% 1/16W MF-LF 402 2
R8801 1 10K 5% 1/16W MF-LF 402 2 GPU_DEEPMH_EN
R8802 1 10K 5% 1/16W MF-LF 402 2 NO STUFF
R8803 1 10K 5% 1/16W MF-LF 402 2 NO STUFF
R8804 1 10K 5% 1/16W MF-LF 402 2 NO STUFF
R8805 1 10K 5% 1/16W MF-LF 402 2
R8806 1 10K 5% 1/16W MF-LF 402 2 NO STUFF
R8808 1 10K 5% 1/16W MF-LF 402 2 NO STUFF
R8809 1 10K 5% 1/16W MF-LF 402 2 NO STUFF
R8811 1 10K 5% 1/16W MF-LF 402 2 NO STUFF
R8812 1 10K 5% 1/16W MF-LF 402 2 GPU_MEM_256M
R8813 1 10K 5% 1/16W MF-LF 402 2 GPU_MEM_64M
R8824 1 10K 5% 1/16W MF-LF 402 2 GPU_MEM_256M
R8827 1 10K 5% 1/16W MF-LF 402 2 GPU_MEM_HYNIX

ROMCFGID[3..0]
0000 = 128MB
0010 = 256MB
0100 = 64MB
0110 = Reserved

GPU_BLON == GPU_BLON (MAKE_BASE=TRUE) 74
TP_GPU_GPIO_10 == TP_GPU_GPIO_10 (MAKE_BASE=TRUE)
NC_GPU_GPIO_14 == NC_GPU_GPIO_14 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_VCORE_LOW == GPU_VCORE_LOW (MAKE_BASE=TRUE) 66
GPU_CLK27MSS_IN == GPU_CLK27MSS_IN (MAKE_BASE=TRUE) 34
NC_GPU_GPIO_17 == NC_GPU_GPIO_17 (MAKE_BASE=TRUE, NO_TEST=TRUE)

Required for debug access
Required for debug access
Required for debug access
Required for debug access

Renamed signals

34 GPU_CLK27M (MAKE_BASE=TRUE) == GPU_XTALIN 72

Unused signals

NC_GPU_XTALOUT (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_XTALOUT 72
NC_ATI_ROMCS_L (MAKE_BASE=TRUE)	NO_TEST=TRUE	TP_ATI_ROMCS_L 72
NC_FB_A_MA12 (MAKE_BASE=TRUE)	NO_TEST=TRUE	TP_FB_A_MA12 68
NC_FB_B_MA12 (MAKE_BASE=TRUE)	NO_TEST=TRUE	TP_FB_B_MA12 68
NC_GPU_GENERICA (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_GENERICA 72
NC_GPU_GENERICB (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_GENERICB 72
NC_GPU_GENERICC (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_GENERICC 72
NC_GPU_VGA_R (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_VGA_R 73
NC_GPU_VGA_G (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_VGA_G 73
NC_GPU_VGA_B (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_VGA_B 73
TP_GPU_VGA_HSYNC (MAKE_BASE=TRUE)		GPU_VGA_HSYNC 73
TP_GPU_VGA_VSYNC (MAKE_BASE=TRUE)		GPU_VGA_VSYNC 73
NC_GPU_TV_Y (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_TV_Y 73
NC_GPU_TV_C (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_TV_C 73
NC_GPU_TV_COMP (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_TV_COMP 73
NC_LVDS_U_DATAP<3> (MAKE_BASE=TRUE)	NO_TEST=TRUE	LVDS_U_DATA_P<3> 73
NC_LVDS_U_DATAN<3> (MAKE_BASE=TRUE)	NO_TEST=TRUE	LVDS_U_DATA_N<3> 73
NC_LVDS_L_DATAP<3> (MAKE_BASE=TRUE)	NO_TEST=TRUE	LVDS_L_DATA_P<3> 73
NC_LVDS_L_DATAN<3> (MAKE_BASE=TRUE)	NO_TEST=TRUE	LVDS_L_DATA_N<3> 73
NC_ATI_DVPCLK (MAKE_BASE=TRUE)	NO_TEST=TRUE	ATI_DVPCLK 72
NC_ATI_DVPCNTL<2..0> (MAKE_BASE=TRUE)	NO_TEST=TRUE	ATI_DVPCNTL<2..0> 72
NC_ATI_DVPDATA<15..0> (MAKE_BASE=TRUE)	NO_TEST=TRUE	ATI_DVPDATA<15..0> 72

Required for debug access

TP_ATI_DVPDATA<23..16> (MAKE_BASE=TRUE) == ATI_DVPDATA<23..16> 72

Also required: GPIO10 - GPIO13

72 66 63 =PP3V3_S0_GPU

R9390 1 4.7K 5% 1/16W MF-LF 402 2
R9391 1 4.7K 5% 1/16W MF-LF 402 2

73 GPU_DDC_B_CLK
73 GPU_DDC_B_DATA

GPU Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

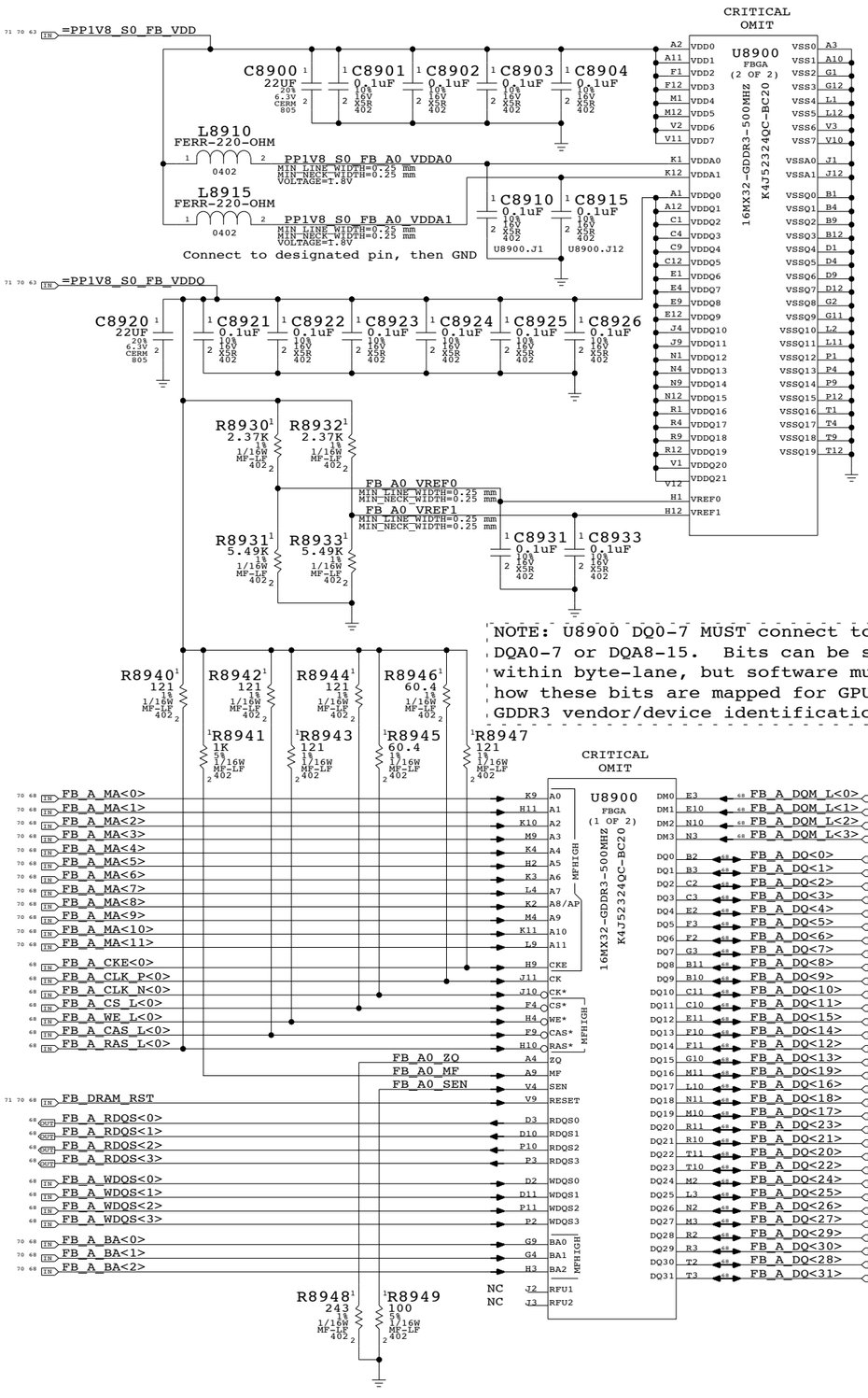
SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 88 OF 104	

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



GDDR3 Frame Buffer A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

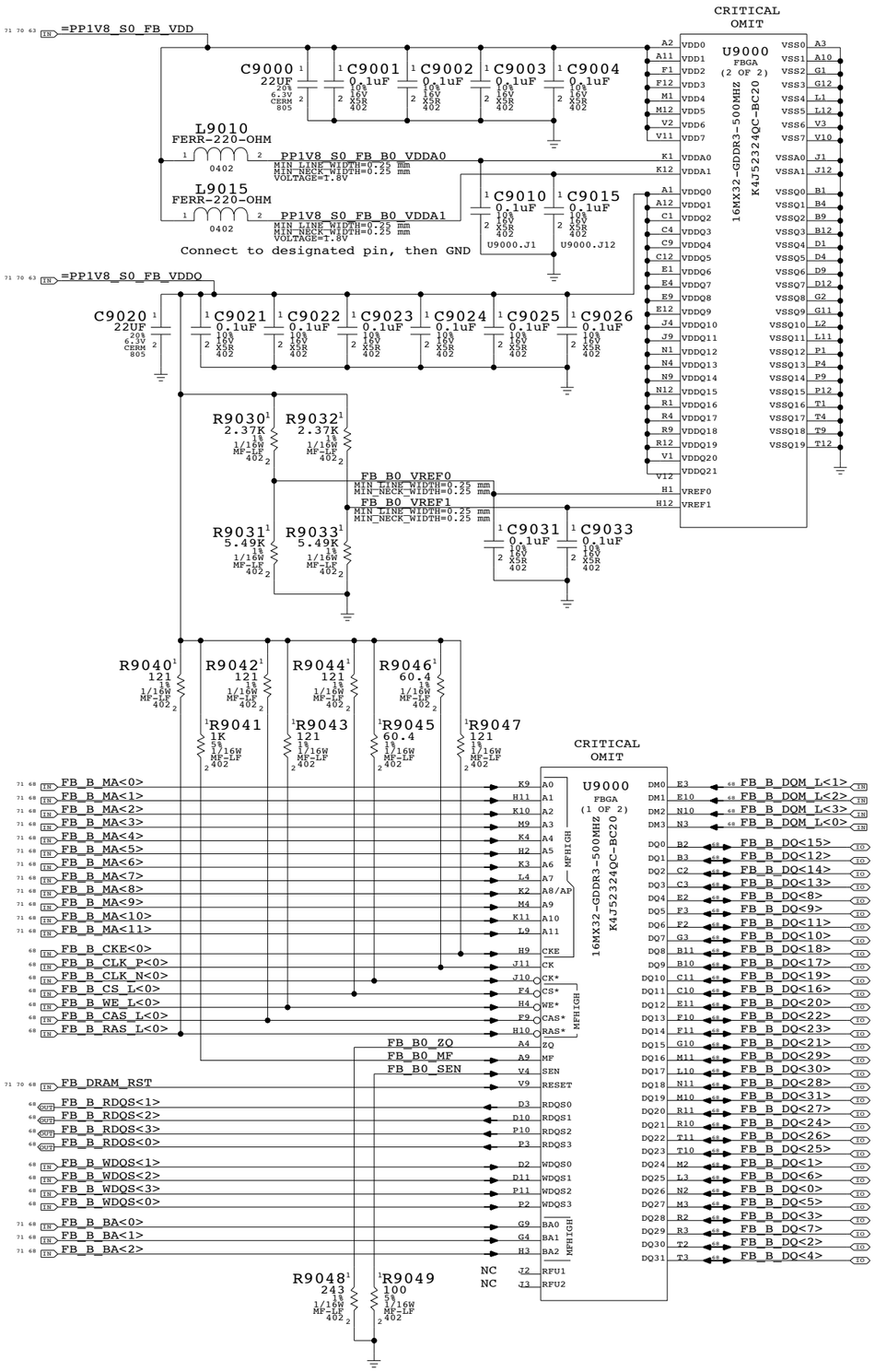
SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 89 OF 104	

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

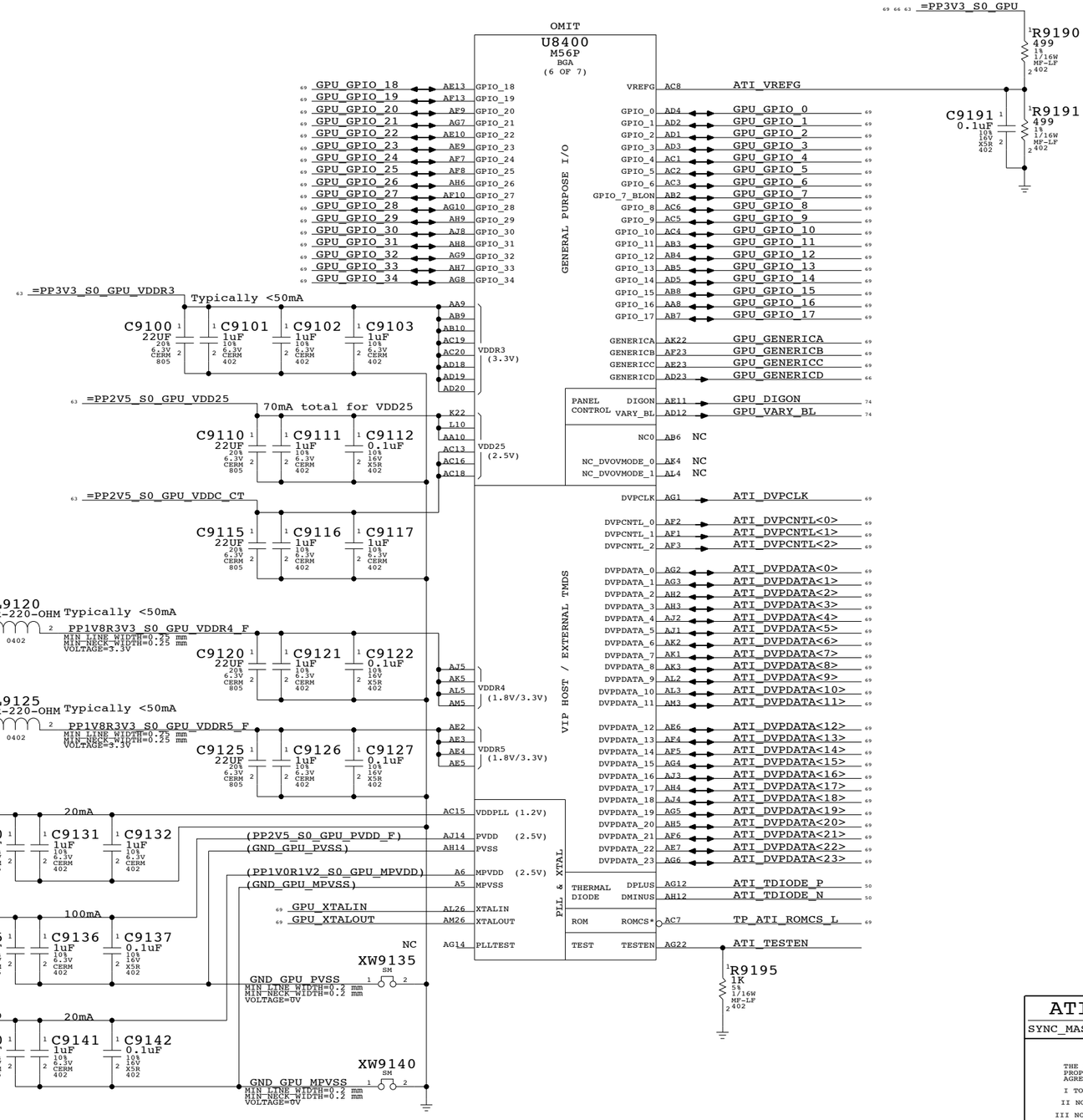
SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 90 OF 104	

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)



ATI M56 GPIO/DVO/Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 91 OF 104	

Page Notes

Power aliases required by this page:
- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

63 =PP2V5_S0_GPU

Sum of peak currents on this page: 605mA

L9300 FERR-220-OHM 0402 — PP2V5_S0_GPU_TPVDD — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
XW9300 SM — GND_GPU_TPVSS — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=0V
C9300 22UF 20% 6.3V CERM 805; C9301 1uF 10% 6.3V CERM 402; C9302 1uF 10% 6.3V CERM 402

L9305 FERR-220-OHM 0402 — PP2V5_S0_GPU_TXVDDR — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 150mA peak
XW9305 SM — GND_GPU_TXVSSR — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V
C9305 22UF 20% 6.3V CERM 805; C9306 1uF 10% 6.3V CERM 402; C9307 0.1uF 10% 16V X5R 402

L9310 FERR-220-OHM 0402 — PP2V5_S0_GPU_AVDD — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 65mA peak
XW9310 SM — GND_GPU_AVSSN — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V
C9310 22UF 20% 6.3V CERM 805; C9311 1uF 10% 6.3V CERM 402; C9312 0.1uF 10% 16V X5R 402

XW9314 SM — GND_GPU_AVSSQ — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V

L9315 FERR-220-OHM 0402 — PP2V5_S0_GPU_VDD1DI — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
C9315 22UF 20% 6.3V CERM 805; C9316 1uF 10% 6.3V CERM 402; C9317 0.1uF 10% 16V X5R 402

L9320 FERR-220-OHM 0402 — PP2V5_S0_GPU_A2VDD — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 130mA peak
XW9320 SM — GND_GPU_A2VSSN — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V
C9320 22UF 20% 6.3V CERM 805; C9321 1uF 10% 6.3V CERM 402; C9322 0.1uF 10% 16V X5R 402

L9325 FERR-220-OHM 0402 — PP2V5_S0_GPU_VDD2DI — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V
XW9324 SM — GND_GPU_A2VSSQ — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V — 20mA peak
C9325 22UF 20% 6.3V CERM 805; C9326 1uF 10% 6.3V CERM 402; C9327 0.1uF 10% 16V X5R 402

L9330 FERR-220-OHM 0402 — PP2V5_S0_GPU_LPVDD — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
XW9330 SM — GND_GPU_LPVSS — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=0V
C9330 22UF 20% 6.3V CERM 805; C9331 1uF 10% 6.3V CERM 402; C9332 1uF 10% 6.3V CERM 402

L9345 FERR-220-OHM 0402 — PP2V5_S0_GPU_LVDDR — MIN_LINE_WIDTH=0.35 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 200mA peak
XW9345 SM — GND_GPU_LVSSR — MIN_LINE_WIDTH=0.35 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V
C9340 22UF 20% 6.3V CERM 805; C9345 22UF 20% 6.3V CERM 805; C9341 1uF 10% 6.3V CERM 402; C9342 0.1uF 10% 16V X5R 402; C9346 0.1uF 10% 16V X5R 402; C9347 0.1uF 10% 16V X5R 402

ATI_RSET 73 — R9350 499 1% 1/16W MF-LF 402
ATI_R2SET 73 — R9351 715 1% 1/16W MF-LF 402

OMIT
U8400 M56P BGA (5 OF 7)

AM8	TPVDD (2.5V)		
AL8	TPVSS		
AJ6, AK6, AL6, AM6	TXVDDR (2.5V)		
AJ7, AK7, AK8, AL7, AM7	TXVSSR		
AL25	AVDD (2.5V)		
AM25			
AJ24	AVSS		
AK25			
AK23	AVSSQ		
AM23	VDD1DI (2.5V)		
AL23	VSS1DI		
AL22	RSET		
AL16	A2VDD (2.5V)		
AM16			
AL17	A2VSS		
AM17			
NC AL14	NC_A2VDDQ		
AK13	A2VSSQ		
AJ16	VDD2DI (2.5V)		
AJ17	VSS2DI		
AK14	R2SET		
AE19	LPVDD (2.5V)		
AE18	LPVSS		
AC21, AC22, AD21, AD22, AE20, AE21, AE22, AF19, AF20	LVDDR (2.5V)		
AF17, AF18, AF21, AF22, AG17, AG19, AH17, AH19, AJ19, AK17	LVSSR		
AF11	HPD1		

INTEGRATED TMDS

TXCP	AM9	79 78 74	TMDS_CLK_P
TXCM	AL9	79 78 74	TMDS_CLK_N
TX0P	AL10	79 78 74	TMDS_DATA_P<0>
TX0M	AK10	79 78 74	TMDS_DATA_N<0>
TX1P	AM11	79 78 74	TMDS_DATA_P<1>
TX1M	AL11	79 78 74	TMDS_DATA_N<1>
TX2P	AM12	79 78 74	TMDS_DATA_P<2>
TX2M	AL12	79 78 74	TMDS_DATA_N<2>
TX3P	AJ9	79 78 74	TMDS_DATA_P<3>
TX3M	AK9	79 78 74	TMDS_DATA_N<3>
TX4P	AJ11	79 78 74	TMDS_DATA_P<4>
TX4M	AK11	79 78 74	TMDS_DATA_N<4>
TX5P	AJ12	79 78 74	TMDS_DATA_P<5>
TX5M	AK12	79 78 74	TMDS_DATA_N<5>

DAC (CRT)

R	AK24	69	GPU_VGA_R
G	AM24	69	GPU_VGA_G
B	AL24	69	GPU_VGA_B
HSYNC	AJ23	69	GPU_VGA_HSYNC
VSYNC	AJ22	69	GPU_VGA_VSYNC

DAC2 (TV/CRT2)

R2	AK15	78 74	GPU_R2
G2	AM15	78 74	GPU_G2
B2	AL15	78 74	GPU_B2
H2SYNC	AF15	78	GPU_H2SYNC
V2SYNC	AG15	78	GPU_V2SYNC
Y	AJ15	69	GPU_TV_Y
C	AJ13	69	GPU_TV_C
COMP	AH15	69	GPU_TV_COMP

LVDS

TXCLK_UP	AJ21	74 74	LVDS_U_CLK_P
TXCLK_UN	AK21	74 74	LVDS_U_CLK_N
TXOUT_U0P	AG18	74 74	LVDS_U_DATA_P<0>
TXOUT_U0N	AH18	74 74	LVDS_U_DATA_N<0>
TXOUT_U1P	AK20	74 74	LVDS_U_DATA_P<1>
TXOUT_U1N	AJ20	74 74	LVDS_U_DATA_N<1>
TXOUT_U2P	AG20	74 74	LVDS_U_DATA_P<2>
TXOUT_U2N	AH20	74 74	LVDS_U_DATA_N<2>
TXOUT_U3P	AH21	69 74	LVDS_U_DATA_P<3>
TXOUT_U3N	AG21	69 74	LVDS_U_DATA_N<3>
TXCLK_LP	AH18	74 74	LVDS_L_CLK_P
TXCLK_LN	AL18	74 74	LVDS_L_CLK_N
TXOUT_L0P	AL19	74 74	LVDS_L_DATA_P<0>
TXOUT_L0N	AK19	74 74	LVDS_L_DATA_N<0>
TXOUT_L1P	AM20	74 74	LVDS_L_DATA_P<1>
TXOUT_L1N	AL20	74 74	LVDS_L_DATA_N<1>
TXOUT_L2P	AM21	74 74	LVDS_L_DATA_P<2>
TXOUT_L2N	AL21	74 74	LVDS_L_DATA_N<2>
TXOUT_L3P	AJ18	69 74	LVDS_L_DATA_P<3>
TXOUT_L3N	AK18	69 74	LVDS_L_DATA_N<3>

MONITOR IDENTIFICATION

DDC1CLK	AH23	74	GPU_DDC_A_CLK
DDC1DATA	AH22	74	GPU_DDC_A_DATA
DDC2CLK	AG13	69	GPU_DDC_B_CLK
DDC2DATA	AH13	69	GPU_DDC_B_DATA
DDC3CLK	AF12	74	GPU_DDC_C_CLK
DDC3DATA	AE12	74	GPU_DDC_C_DATA

73 ATI_RSET
73 ATI_R2SET
73 GPU_HPD

Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb

ATI M56 Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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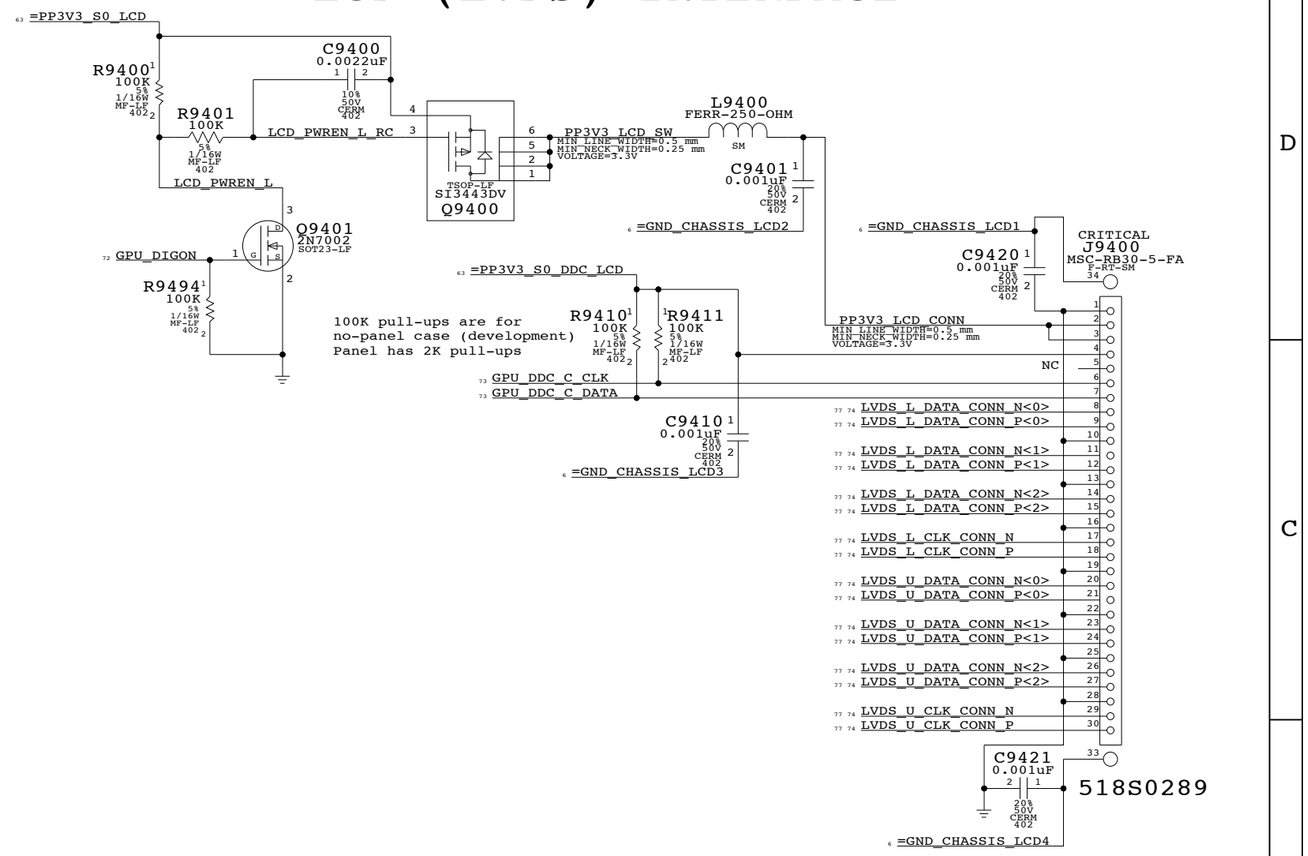
APPLE COMPUTER INC.

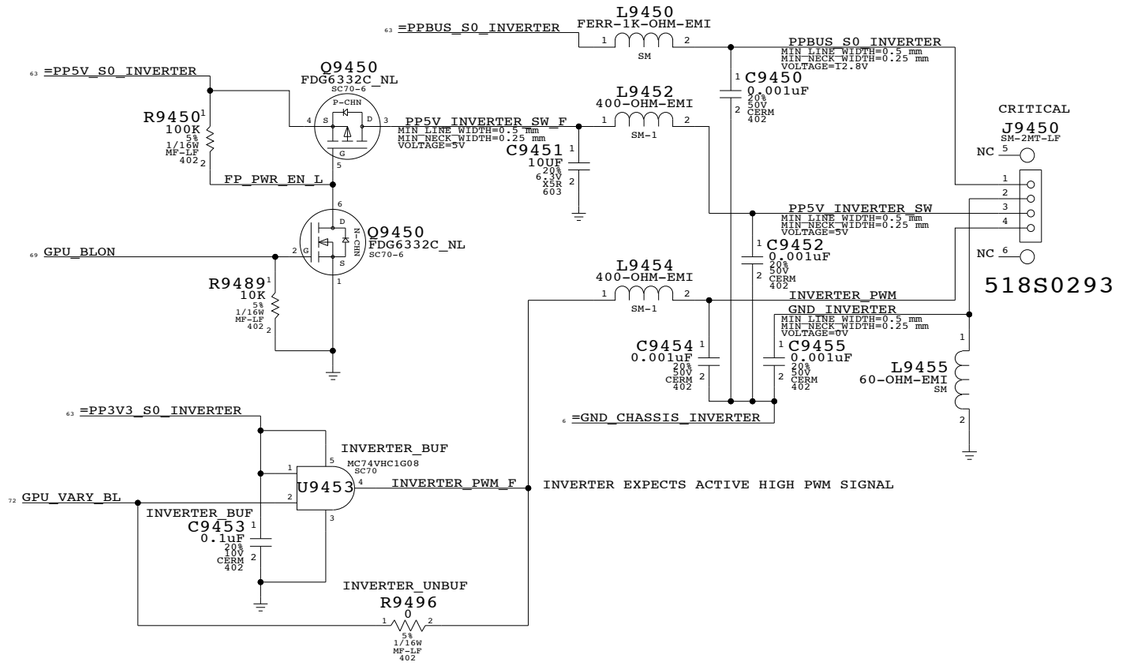
SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 93 OF 104	

LCD (LVDS) INTERFACE

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL		
	VGA	VGA	GPU_R2	73 75
	VGA	VGA	GPU_G2	73 75
	VGA	VGA	GPU_B2	73 75
	LVDS	LVDS	LVDS_U_CLK_P	73 77
	LVDS	LVDS	LVDS_U_CLK_N	73 77
	LVDS	LVDS	LVDS_U_DATA_P<2..0>	73 77
	LVDS	LVDS	LVDS_U_DATA_N<2..0>	73 77
	LVDS	LVDS	LVDS_L_CLK_P	73 77
	LVDS	LVDS	LVDS_L_CLK_N	73 77
	LVDS	LVDS	LVDS_L_DATA_P<2..0>	73 77
	LVDS	LVDS	LVDS_L_DATA_N<2..0>	73 77
	LVDS	LVDS	LVDS_U_CLK_CONN_P	74 77
	LVDS	LVDS	LVDS_U_CLK_CONN_N	74 77
	LVDS	LVDS	LVDS_U_DATA_CONN_P<2..0>	74 77
	LVDS	LVDS	LVDS_U_DATA_CONN_N<2..0>	74 77
	LVDS	LVDS	LVDS_L_CLK_CONN_P	74 77
	LVDS	LVDS	LVDS_L_CLK_CONN_N	74 77
	LVDS	LVDS	LVDS_L_DATA_CONN_P<2..0>	74 77
	LVDS	LVDS	LVDS_L_DATA_CONN_N<2..0>	74 77
	TMDS	TMDS	TMDS_CLK_P	73 75 79
	TMDS	TMDS	TMDS_CLK_N	73 75 79
	TMDS	TMDS	TMDS_DATA_P<5..3>	73 75 79
	TMDS	TMDS	TMDS_DATA_N<5..3>	73 75 79
	TMDS	TMDS	TMDS_DATA_P<2..0>	73 75 79
	TMDS	TMDS	TMDS_DATA_N<2..0>	73 75 79



INVERTER INTERFACE



Internal Display Connectors

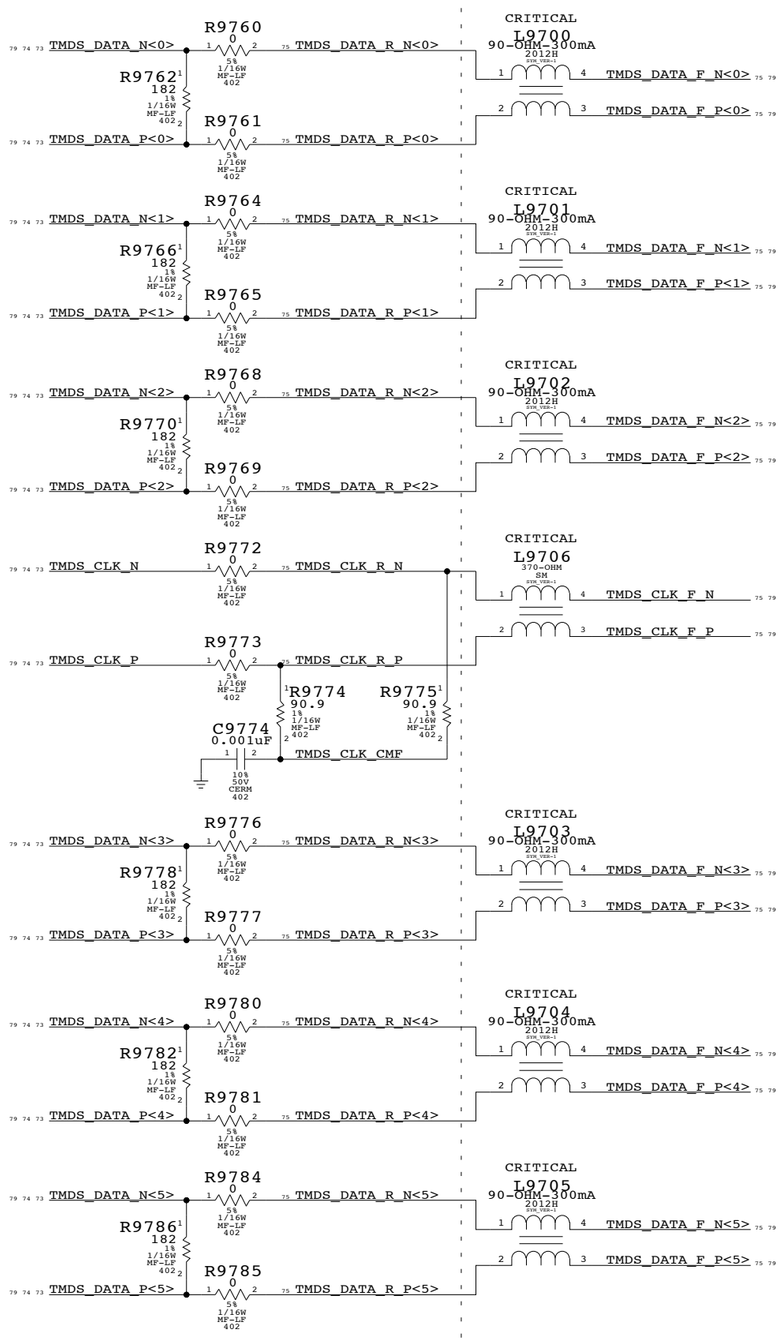
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

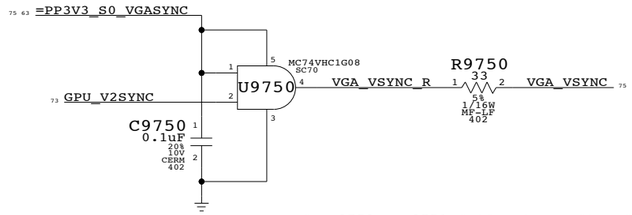
SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 94 OF 104	

TMDS Filtering

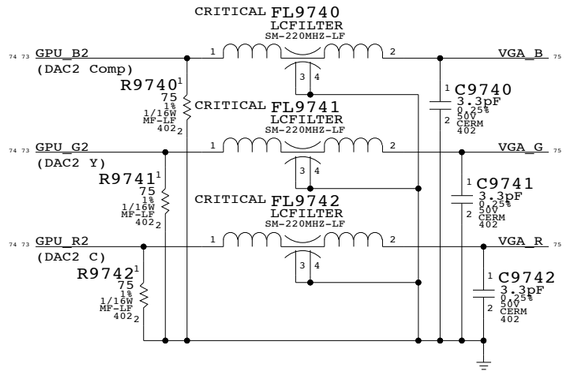
Place series R's and common-mode filtering close to GPU, common mode chokes near connector.



VGA SYNC BUFFERS

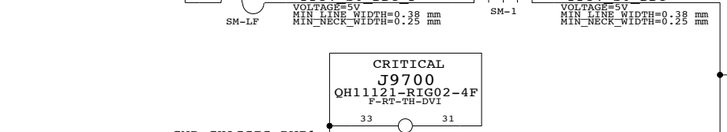


ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

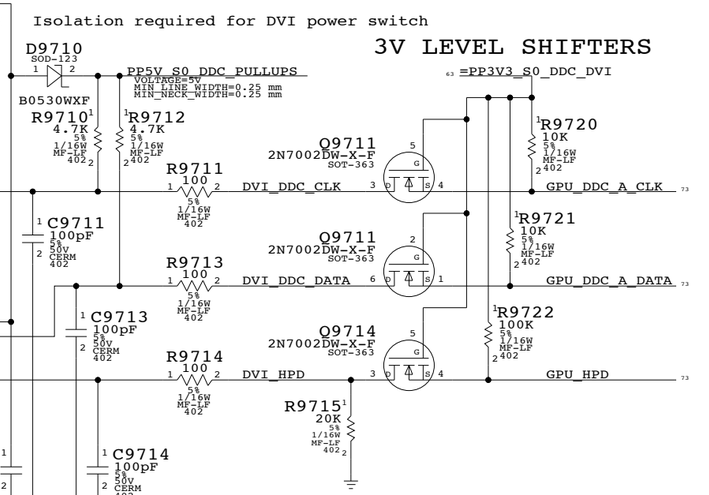


DVI INTERFACE

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)



Isolation required for DVI power switch



NET_TYPE		
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL
	TMDS	TMDS_CLK_R_P
	TMDS	TMDS_CLK_R_N
	TMDS	TMDS_DATA_R_P<5..0>
	TMDS	TMDS_DATA_R_N<5..0>
	TMDSCONN	TMDSCONN TMDS_CLK_F_P
	TMDSCONN	TMDSCONN TMDS_CLK_F_N
	TMDSCONN	TMDSCONN TMDS_DATA_F_P<5..0>
	TMDSCONN	TMDSCONN TMDS_DATA_F_N<5..0>

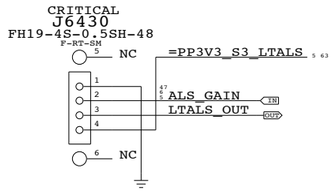
External Display Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

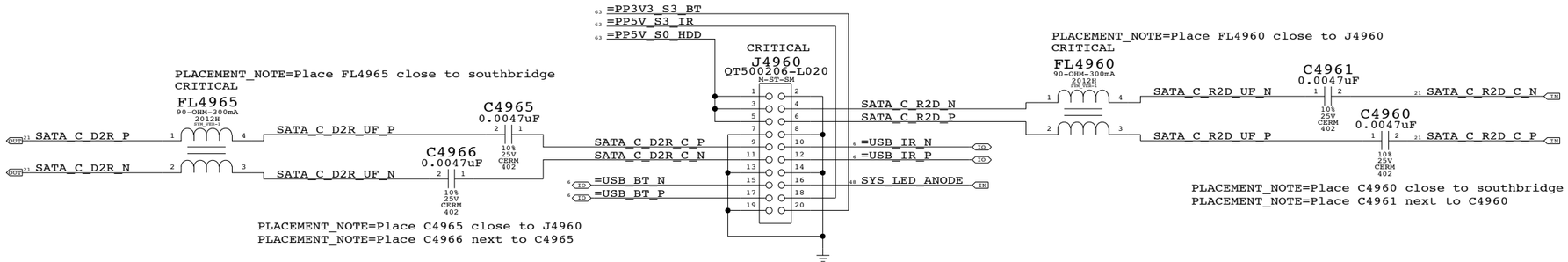
SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 97 OF 104	

Left ALS Connector



518S0395

Bluetooth (M13P), IR & SATA HDD Flex Connector



516S0412

NOTE: _UF_ nets cross DDR2 signals and pick up significant noise. Common-mode chokes are to remove this noise from SATA signals.

M1 Specific Connectors

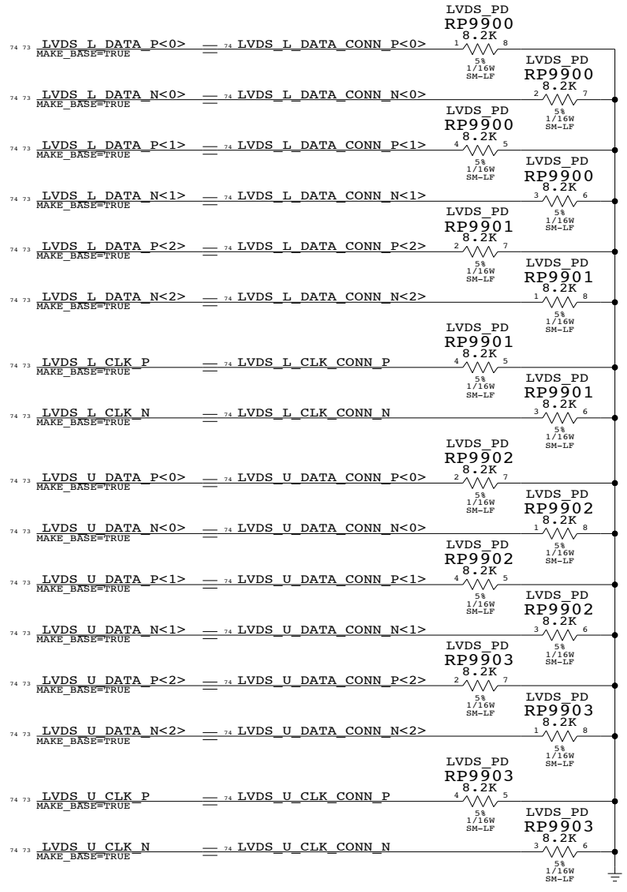
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 98 OF 104	

LVDS Interface Pull-downs

NOTE: These parts are to counter an invalid state caused by the M56 part. Bias voltage is present on LVDS interface pins even when they should be tri-stated to meet panel power sequence requirements. Resulting pump-up in LCD panel can cause startup and long-term reliability issues. Pull-down resistors reduce the pump-up in the panel, though some voltage will still be seen on LVDS signals when they should be 0V.



LVDS Interface Pull-downs

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 99 OF 104	

Date - Radar # - Description

DMS Release #03000 (RFA #394758)

2005/08/11 - 4214109 - Changed J4931 to proper 518S0342 part.
2005/08/12 - 4231030 - Changed pinout of J4960, added placement notes.

Changes from Proto Branch (DMS Release #04000):

2005/08/27 - 4230219 - Changed Y3301 to non-obsoleted part.
2005/08/27 - 4235208 - Changed value of R7707 to fix 2.5V S3 supply.
2005/08/27 - 4235213 - Changed R8305, R8310, R8315 to slow down FET RCs.
2005/08/27 - 4235401 - Moved a few pins at LIO BTB connector.
2005/08/27 - 4227325 - Removed S0 option for camera, now S3-only.
2005/08/27 - 4227369 - Removed SMC options for display/backlight, now GPU-only.
2005/08/27 - 4225433 - Changed PBUS voltage sense circuit.
2005/08/28 - 4217535 - Added Left ALS FFC connector.
2005/08/28 - 4232563 - Changed analog video from Y/C/Comp to G2/R2/B2.
2005/08/28 - 4235203 - Changed BOM settings to stuff R2251.
2005/08/28 - 4217524 - Added LEFT ALS connector (J6430).
2005/08/28 - 4217535 - OMITs and tables to change 4-pin WTB connector parts.
2005/08/28 - 4221973 - Added pull-up for SB GPIO22 (REQ4#).
2005/08/28 - 4225369 - Changed ISL6269 PVCC aliases, added RC for 3.3V S5.
2005/08/28 - 4225433 - Changed PBUS Voltage Sense circuit.
2005/08/28 - 4227322 - Changed FW323 PCI_VIOS pin from 3.3V S0 to 3.3V S3.
2005/08/28 - 4235179 - OMIT and table to change 8-pin DC-In connector to 6-pin.
2005/08/28 - 4235179 - Changed PBUS net names to merge PBUS A & PBUS B.
2005/08/28 - 4232715 - Added FireWire ISense resistor, changed INA193 to INA194.
2005/08/28 - 4235217 - Added RC on Q3820 gate to slow down ODD FET turn-on.
2005/08/28 - 4225369 - OMITs and tables for staged LeMenu BOM approach.
2005/08/28 - 4227323 - Repinned Top-Case Flex connector.

DMS Checkin #04001

2005/08/29 - 4235179 - Changed J8200 to proper 6-pin part.
2005/08/29 - 4232826 - Changed MEM_ODT* from RPAKs to discrete Rs.
2005/08/29 - 4217524 - Changed R6430 from 4.5K to 3.5K.
2005/08/29 - 4237119 - Changed LIO 5V S3 to 5V S5.
2005/08/29 - 4225369 - Changed 3.3V S5 sequence to follow 5V S5 PGOOD.
2005/08/29 - 4227336 - Changed Y5920 to 197S0169.
2005/08/29 - 4227309 - Resolved sync issues with M38 (SB page 21).
2005/08/29 - 4227310 - Resolved sync issues with M38 (SB page 22).
2005/08/29 - 4227312 - Resolved sync issues with M38 (SB page 23).
2005/08/29 - 4227322 - Sync page 44 with M42 to fix FW power net S-states.
2005/08/29 - 4227332 - Resolved sync issues with M38 (SMC page 58).
2005/08/29 - 4227335 - Changed U5900 to resolve ROHS issue.

DMS Checkin #04002

2005/08/30 - 4225433 - Fixed voltage divider values in PBUS VSense circuit.
2005/08/30 - 4217535 - Removed BOM tables and OMITs for new 4-pin WTB connector.
2005/08/31 - 4214109 - Reversed pinout of J4931 to match updated PCB footprint.
2005/08/31 - 4227328 - Added ESD protection diode on right USB port.
2005/08/31 - 4223808 - Various power supply R/C updates, plus some R/C adds.
2005/08/31 - 4227315 - Changed BSA bus pull-ups from 2K to 10K.
2005/08/31 - 4237025 - Added R8824 and R8827 for GPU memory configuration straps.

DMS Checkin #04003

2005/08/31 - 4240157 - Corrected pinout at SATA/BT conn (J4960) to match flex.
2005/08/31 - 4240150 - Swapped PCIE Mini Card R2D/D2R connections at J5500.
2005/08/31 - 4232563 - Corrected net properties on R2/G2/B2 nets.
2005/08/31 - 4227306 - Swapped primary & alt part numbers for CPU VCore caps.
2005/08/31 - 4240300 - Changed C6455 to a smaller part for cost & MCO.
2005/08/31 - 4240486 - Power line width & neck reductions at PCB request.
2005/08/31 - 4240257 - Swapped some top & bottom EMC connections at DVI connector.

DMS Checkin #04004

2005/08/31 - 4227328 - Changed EMI caps from 50V to 16V to fid in ESD protection.

DMS Checkin #04005

2005/09/02 - 4241087 - Fixed pinout of USB D+/D- at camera connector to match FHB.
2005/09/02 - 4243269 - Inverted GPU VCore control, adjusted supply R values.
2005/09/02 - 4244019 - Moved GPU-related power alias from PP3V3_S0 to PP3V3_S0_GPU.
2005/09/02 - 4240486 - Adjusted line/neck widths, changed J4931 to 518S0371.

DMS Checkin #04006

2005/09/03 - 4232534 - Fixed documentation of battery address on I2C page.
2005/09/03 - 4244484 - Changed P1V5S0_RUNSS circuit to work properly in G3Hot.
2005/09/03 - 4244539 - Added GPUVCORE_PGOOD to 1.2V, 1.8V, & 2.5V S0 sequence.
2005/09/03 - 4227315 - Changed SMBus pull-ups to 4.7K.
2005/09/03 - 4232534 - Added notes for power supplies and connectors.

DMS Checkin #04007

2005/09/06 - 4240486 - Removed NO_TEST property from GPU HSYNC and VSYNC.
2005/09/06 - 4246683 - Removed NO STUFF option from R8805 per ATI request.
2005/09/06 - 4232534 - Fixed label BOM tables to call out proper EEE #'s.

DMS Release #05000-07000 (Proto 2 releases)

2005/09/08 - 4247941 - Net property & name changes to support PCB/ICT requests.
2005/09/08 - 4248911 - Sync with M38 & M42.
2005/09/08 - 4214493 - Combined RTC coin cell diodes into dual-diode package.
2005/09/08 - 4229560 - First implementation of Physical Security Guidelines.
2005/09/16 - 4256660 - Updated FUNC_TEST property for merged PBUS.
2005/09/16 - 4229560 - Changed FW PCI REQ/GNT pair for Physical Security.
(11.1.0) 2005/09/19 - 4247941 - GND line/neck/voltage properties updated per PCB request.
(11.2.0) 2005/09/19 - 4235898 - Moved signal alias to improve schematic reuse.
2005/09/20 - 4214847 - Updated L1970 (old part no longer exists in library).
2005/09/21 - 4227306 - Changed CPU VCore caps to proper production part number.
2005/09/21 - 4234952 - Replaced FDG6324L parts with FDG6332C for cost & supply.
2005/09/26 - 4239505 - Updated J4200 (old part no longer exists in library).
2005/09/26 - 4274915 - Thermal sensor BOM updates from Proto 2 MLB branch.
2005/09/26 - 4274915 - U6301 part number updated to M1 development BootROM.

Date - Radar # - Description

DMS Checkin #07001

2005/09/28 - 4221965 - Added 2.2uF caps on SO-DIMM VREF pins.
2005/09/28 - 4278828 - Adjusted P5VS5_PGOOD R's, added cap on PM_RSMRST_L.
2005/09/29 - 4232826 - Swapped Vtt RPAK functions to free up unnecessary part.
2005/09/30 - 4261313 - Added placeholder connector for IR FFC connector.
2005/09/30 - 4282162 - Changed GPU BBN supply to MAX1673.
2005/09/30 - 4248911 - Sync with M38 & M42.
2005/09/30 - 4282349 - Added CRITICAL flags to parts identified in scrub.
2005/09/30 - 4274915 - C1001 stuffing change from Proto 2 MLB branch.

DMS Checkin #07002

2005/10/04 - 4256409 - Changed fan CTL series R's to 2N7002 level-shifter.
2005/10/04 - 4261313 - Deleted placeholder connector, grew HDD connector for IR.
2005/10/04 - 4281394 - BOM option change to stuff right USB ESD protection part.
2005/10/06 - 4227330 - Added ESD protection on top-case USB port.
2005/10/07 - 4286888 - BOM restructuring per EVT build plan.
2005/10/07 - 4292633 - Changed IMVP6 10K NTC from 10% to 5% part.
2005/10/07 - 4248911 - Sync with M38 & M42.

DMS Checkin #07003

2005/10/08 - 4214493 - Simplified FireWire port power circuit for BOM consolidation.
2005/10/08 - 4293072 - Various BOM / connection changes at IMVP6 (CPU VCore).
2005/10/08 - 4286729 - Changed value of TPM Xtal caps.
2005/10/08 - 4290735 - Swapped trackpad & PCIe Mini Card USB connections.
2005/10/09 - 4235898 - Part moves & refdes changes to support sync with M9.
2005/10/09 - 4214494 - Changed GPU VCore supply enable to use 1.2V/2.5V S3 PGOODs.
2005/10/09 - 4272237 - Changed 2.5V S0 FET RC to 100K to slow down turn-on.

DMS Checkin #07004

2005/10/10 - 4232826 - Swapped Vtt RPAK functions to optimize layout.
2005/10/10 - 4247941 - Net property updates found via back-annotation.

DMS Checkin #07005

2005/10/10 - 4229560 - Removed Physical Security circuitry.
2005/10/10 - 4214493 - Cost reductions to GPU power supply circuitry.
2005/10/10 - 4214847 - Changed 0-ohm resistor to solder jumper.
2005/10/10 - 4248911 - Sync with M38 & M42.
2005/10/10 - 4295280 - Changed sleep LED connection per new SMC ERS.

DMS Checkin #07006

2005/10/11 - 4261313 - Updated SATA connector pinout to match latest flex.
2005/10/11 - 4227308 - Deleted unnecessary MCH TVDAC filtering.
2005/10/11 - 4229560 - Changed SB GNT3#/GNT4# back to test points.
2005/10/12 - 4248911 - Sync with M38 & M42.
2005/10/12 - 4298899 - Changed stuffing option to disable PLT_RST gating.
2005/10/12 - 4297684 - Split FW323 VSSA from VSS to reduce noise.
2005/10/12 - 4223808 - Power supply changes per vendor feedback.
2005/10/12 - 4227320 - Updated SB pin name for GPIO 5 (ODD_PWR_EN_L).
2005/10/12 - 4244539 - Retasked FET to control 3.3V S0 FET from GPU VCore PGOOD.
2005/10/12 - 4247941 - Added properties to resolve a PCB constraint issue.
2005/10/12 - 4214493 - Consolidated 0.22uF caps in design.
2005/10/12 - 4298905 - Changed ethernet VMAIN_AVLBL connection.
2005/10/12 - 4298943 - Replaced last remaining non-RoHS compliant connector.
2005/10/12 - 4214494 - Implemented circuit to power down ethernet in S3 on battery.

DMS Checkin #07007

2005/10/13 - 4247941 - Swapped pins at trackpad ESD protection diode.

DMS Checkin #07008

2005/10/13 - 4247941 - Unswapped pins at trackpad ESD protection diode.

DMS Checkin #07009

2005/10/13 - 4247941 - Removed NO_TEST properties from CPU FSB strobe signals.
2005/10/13 - 4247941 - Spacing/Physical rule updates to match latest board database.
2005/10/14 - 4247941 - Restored NO_TEST properties, added EXPOSED_VIA properties.
2005/10/17 - 4292633 - Changed remaining 10K NTCs to new 5% part.
2005/10/17 - 4304248 - Updated GPU VCore / BBP voltages for B13/B24 support.

DMS Release #08000-11000 (EVT releases)

2005/10/20 - 4310267 - Synced 4 pages from mlb_evt branch back to trunk.
2005/10/21 - 4310267 - Synced 3 pages from mlb_evt branch back to trunk.
2005/10/21 - 4235898 - Synced 2 pages from m9/mlb.
2005/10/26 - 4310267 - Synced 4 pages from mlb_evt branch back to trunk.
2005/11/03 - 4310267 - Synced 6 pages from mlb_evt branch back to trunk.
2005/11/15 - 4310267 - Synced 5 pages from mlb_evt branch back to trunk.
2005/11/15 - 4298899 - Removed unused platform reset gate.
2005/11/15 - 4322537 - Updated thru-hole SO-DIMM connector part number.
2005/11/16 - 4345498 - Updated Ethernet & FireWire crystal part numbers.
2005/11/16 - 4235898 - Aliased connection to ALS_GAIN to support M9 request.
2005/11/16 - 4235898 - Changed Yukon power rail neck widths per M9 request.
2005/11/16 - 4227333 - Updated SMC net names per ERS v1.2.1.
2005/11/16 - 4345921 - FUNC_TEST updates per test team request.
2005/11/16 - 4346006 - Updated J5500 pinout to match updated LIO board pinout.
2005/11/16 - 4343202 - Changed USB overcurrent switch to TPS2051B, added OC* RC.
2005/11/16 - 4346184 - Inserted common-mode chokes on SATA R2D/D2R pairs.

DMS Checkin #11001

2005/11/16 - 4235898 - Sync with M38 & M42.
(11.1.0) 2005/11/16 - 4298899 - Fixed ethernet reset net name on page 26.
(11.2.0) 2005/11/16 - 4227333 - Fixed single-pin nets caused by SMC net name updates.
2005/11/18 - 4235898 - Changed R4210 package size per M9 request.
(11.3.0) 2005/11/18 - 4235898 - Changed C9710 GND connection per M9 request.
2005/11/19 - 4346184 - Fixed location of SATA R2D common-mode choke.
2005/11/19 - 4347717 - Changed SMS self-test pull-up to pull-down.
2005/11/19 - 4350840 - Simplified TMDS filtering to allow movement of filter.
2005/11/19 - 4229560 - Changed FW chip back to REQ/GNT3.
2005/11/19 - 4350849 - Added option to connect SB_GPIO30 to ENET_LOM_DIS_L.
2005/11/19 - 4340256 - Changed topcase flex trackpad power from 3.3V to 5V.
(11.4.0) 2005/11/19 - 4292165 - Refreshed schematic symbol for U3750 (library update).

Date - Radar # - Description

DMS Checkin #11002

2005/11/21 - 4351196 - Added 1K pull-down on IDE_RESET_L.
(11.5.0) 2005/11/21 - 4343202 - Changed RC value and net name for USB OC.
2005/11/22 - 4350840 - Swapped TMDS termination components for placement.
(11.6.0) 2005/11/22 - 4352020 - Changed 2.5V S3 supply inductor & compensation values.
(11.7.0) 2005/11/28 - 4347845 - Added pull-down resistors on LVDS interface.
2005/11/30 - 4227340 - Removed CPU VCore current sense input RC.
2005/11/30 - 4331670 - Added CRITICAL flags to some more parts.
2005/11/30 - 4343864 - Added EMI/ESD parts at camera connector.
2005/11/30 - 4351181 - Changed ITP connector BOM option.
2005/11/30 - 4351196 - Changed IDE_RESET_L pull-down from 1K to 15K.
2005/11/30 - 4358831 - Added pull-downs on two SB-to-SMC signals.
2005/12/01 - 4362404 - Changed TMDS diff term from 100-ohm to 180-ohm.
2005/12/01 - 4352020 - Changed 2.5V supply inductor to RoHS-compliant part.
2005/12/01 - 4227340 - Changed supply for 1.8V S3 current sense amp.
2005/12/01 - 4362566 - Restructured BOM for thick/thin PCB versions.
2005/12/01 - 4347845 - RPAK pinswaps to LVDS pull-downs for PCB layout.

DMS Checkin #11003

2005/12/02 - 4256256 - Added BOMOPTION to R8801 to allow per-project control.
2005/12/02 - 4363848 - Removed M56 GPU die rev B13 support from BOM.
2005/12/02 - 4363870 - Removed M1a support from BOM.
2005/12/02 - 4217524 - Updated part number for J6430.

DMS Release #12000-13000 (DVT releases)

2005/12/07 - 4375840 - Synced 4 pages from mlb_dvt branch back to trunk.
2005/12/12 - 4235898 - Changes to LVDS net names to support mux option.
2005/12/12 - 4362451 - Added MAKE_BASE=TRUE to SMC 32KHz SUSCLK net.
2006/01/03 - 4375840 - Synced 1 page from mlb_dvt branch back to trunk.
2006/01/03 - 4290282 - Removed BOM table, changed L9455 to 155S0002.
2006/01/03 - 4347845 - Changed LVDS pull-downs from 10K to 8.2K.
2006/01/03 - 4391436 - Swapped N/P signal names on one portion of SATA_R2D.
2006/01/03 - 4362451 - Changed SCH/PCB/BOM part descriptions for Rev A.
(13.1.0) 2006/01/03 - 4362451 - Removed power jumpers and 0-ohm resistor.
2006/01/05 - 4362566 - Removed 920- number for thin PCB option.
2006/01/05 - 4394079 - Added BOMOPTION to SYS_ONEWIRE pull-up.
2006/01/05 - 4362451 - Removed power jumpers and 0-ohm resistor.
2006/01/05 - 4362451 - Restructured BOM tables to eliminate LeMenu.
2006/01/06 - 4402184 - Changed R7540 value for IMVP6 load-line improvement.
2006/01/06 - 4362451 - Added System Block Diagram, updated Power Diagram.
2006/01/06 - 4362451 - Changed BOM options for production SMC, BootROM.

DMS Release #A000 (PVT Release)

2006/01/21 - 4412882 - Changed R7623 from 1.33K to 931 ohms.
(A.1.0) 2006/01/21 - 4414757 - Changed 138S0552 to 138S0580 & 138S0553 to 138S0581.
2006/01/26 - 4420815 - Changed 2x 128S0077 to 128S0068.

DMS Release #B000 (PVT BOM Update)

(B.0.0) 2006/02/09 - 4440116 - Pulled new schematic part number (051-7099).
2006/02/09 - 4440116 - Restructured BOM for 3 CPU configs.
2006/02/09 - 4440116 - Updated BootROM / SMC part numbers.

DMS Release #A000 (Ramp Config Update)

(A.0.0) 2006/02/13 - 4420815 - Changed remaining 128S0077 to 128S0086.
2006/02/13 - 4420815 - Added 128S0077 as alternate for 128S0086.
2006/02/13 - 4437189 - Changed R7757 to 1Mohm & R7770 to 100K.
(A.1.0) 2006/02/13 - 4431947 - Removed NO STUFF option from C3309.

DMS Release #B000 (PVT BOM Roll-In)

(B.0.0) 2006/02/17 - 4449123 - Changed C7537: 4.7nF -> 47pF, R7537: 3.57K -> 4.42K.

DMS Release #C000 (Ramp BOM Update)

(C.0.0) 2006/03/03 - 4457745 - Added 128S0094 & 128S0095 as alternates for 128S0060.
2006/03/03 - 4457801 - Added 128S0081 as alternate for 128S0061.
2006/03/03 - 4466770 - Changed R7920 from 5% to 1% to reduce variation.
2006/03/03 - 4399085 - Changed C7532 from 10nF to 15nF to slow CPU slew rate.
2006/03/03 - 4424175 - Changed 8 VRAM strap resistors to enable ICT testing.

DMS Release #D000 (Ramp BOM Update)

(D.0.0)

D

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE NONE SHT 100 OF 104

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	FSB_55S	FSB_COMMON	FSB_ADS_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_BNR_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_BPRI_L	7 12
	FSB_55S	FSB_COMMON	FSB_BREQ0_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_DBSY_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_DEFER_L	7 12
	FSB_55S	FSB_COMMON	FSB_DPWR_L	7 12
	FSB_55S	FSB_COMMON	FSB_DRDY_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_HIT_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_HITM_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_LOCK_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	7 12
	FSB_55S	FSB_COMMON	FSB_TRDY_L	7 12
	FSB_55S	FSB_COMMON	FSB_CPURST_L	7 11 12
	FSB_55S	FSB_DATA	FSB_D_L<63..0>	5 7 12
	FSB_55S	FSB_DATA	FSB_DINV_L<3..0>	5 7 12
	FSB_55S	FSB_DSTB	FSB_DSTBP_L<3..0>	5 7 12
	FSB_55S	FSB_DSTB	FSB_DSTBN_L<3..0>	5 7 12
	FSB_55S	FSB_ADDR	FSB_A_L<31..3>	5 7 12
	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	5 7 12
	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<3..0>	5 7 12
	CPU_55S		FSB_IERR_L	7
	CPU_55S		FSB_FERR_L	
	CPU_55S		CPU_PWRGD	7 21
	CPU_55S		CPU_INTR	7 21
	CPU_55S		CPU_NMI	7 21
	CPU_55S		CPU_A20M_L	7 21
	CPU_55S		CPU_DPSLP_L	7 21
	CPU_55S		CPU_IGNNE_L	7 21
	CPU_55S		CPU_INIT_L	7 21
	CPU_55S		CPU_SMI_L	7 21
	CPU_55S		CPU_STPCLK_L	7 21
	CPU_55S	CPU_2TO1	CPU_THERMTRIP_L	
	CPU_55S	CPU_2TO1	PM_DPRSLPVR	14 23 57
	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	57
	CPU_55S	CPU_GTLREF	CPU_GTLREF	7
	CPU_55S	CPU_COMP	CPU_COMP<3>	7
	CPU_27P4S	CPU_COMP	CPU_COMP<2>	7
	CPU_55S	CPU_COMP	CPU_COMP<1>	7
	CPU_27P4S	CPU_COMP	CPU_COMP<0>	7
	CPU_55S	CPU_ITP	XDP_BPM_L<5..0>	7 11
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_P	11 34
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_N	11 34
	CPU_55S	CPU_ITP	ITPRESET_L	11
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8 9 79
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8 9 79
THERM	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8 57
THERM	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	8 57
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	57
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	57

MEM_CLK	MEM_70D
MEM_CTRL	MEM_45S
MEM_CMD	MEM_55S
MEM_DATA	MEM_55S
MEM_DQS	MEM_85D
FB_CLK	FB_75D
FB_ADCTRL	FB_35S_TO_55S
FB_ADCTRL	FB_55S
FB_DATA	FB_40S
LVDS	LVDS_100D
TMDS	TMDS_100D
VGA	VGA_75S
PCIE	PCIE_100D
DMI	DMI_100D
SATA	SATA_100D
IDE	IDE_55S
USB2	USB2_90D
ENET	ENET_100D
FW	FW_110D
SMB	SMB_55S
SPI	SPI_55S
CLK_FSB	CLK_FSB_100D
CLK_PCIE	CLK_PCIE_100D
CLK_MED	CLK_MED_55S
CLK_SLOW	CLK_SLOW_55S

AUDIO_55S	AUDIO	SB_ACZ_BITCLK	21
AUDIO_55S	AUDIO	ACZ_BITCLK	5 21 45
AUDIO_55S	AUDIO	SB_ACZ_SYNC	21
AUDIO_55S	AUDIO	ACZ_SYNC	5 21 45
AUDIO_55S	AUDIO	SB_ACZ_RST_L	21
AUDIO_55S	AUDIO	ACZ_RST_L	5 21 45
AUDIO_55S	AUDIO	ACZ_SDATAIN<0>	5 21 45
AUDIO_55S	AUDIO	SB_ACZ_SDATAOUT	21
AUDIO_55S	AUDIO	ACZ_SDATAOUT	5 21 45

	TMDS	TMDS	TMDS_CLK_P	73 74 75
	TMDS	TMDS	TMDS_CLK_N	73 74 75
	TMDS	TMDS	TMDS_DATA_P<5..3>	73 74 75
	TMDS	TMDS	TMDS_DATA_N<5..3>	73 74 75
D0	TMDS	TMDS	TMDS_DATA_P<2..0>	73 74 75
D1	TMDS	TMDS	TMDS_DATA_N<2..0>	73 74 75
	TMDSCONN	TMDSCONN	TMDS_CLK_F_P	75
	TMDSCONN	TMDSCONN	TMDS_CLK_F_N	75
	TMDSCONN	TMDSCONN	TMDS_DATA_F_P<5..3>	75
	TMDSCONN	TMDSCONN	TMDS_DATA_F_N<5..3>	75
D2	TMDSCONN	TMDSCONN	TMDS_DATA_F_P<2..0>	75
D3	TMDSCONN	TMDSCONN	TMDS_DATA_F_N<2..0>	75

M1 Net Properties

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 104 OF 104	