1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM,MLB,M82

MACBOOK AIR (JAN 2007)

PRODUCTION

01/25/2009

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
J		667176	PRODUCTION RELEASED	01/25/09	

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7230	1	SCHEM,MLB,M82	SCH	CRITICAL	
820-2179	1	PCBF,MLB,M82	PCB	CRITICAL	

DRAWING
TITLE=M82_MLB
ABBREV=DRAWING
LAST_MODIFIED=Sun Jan 25 09:33:52 2009

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

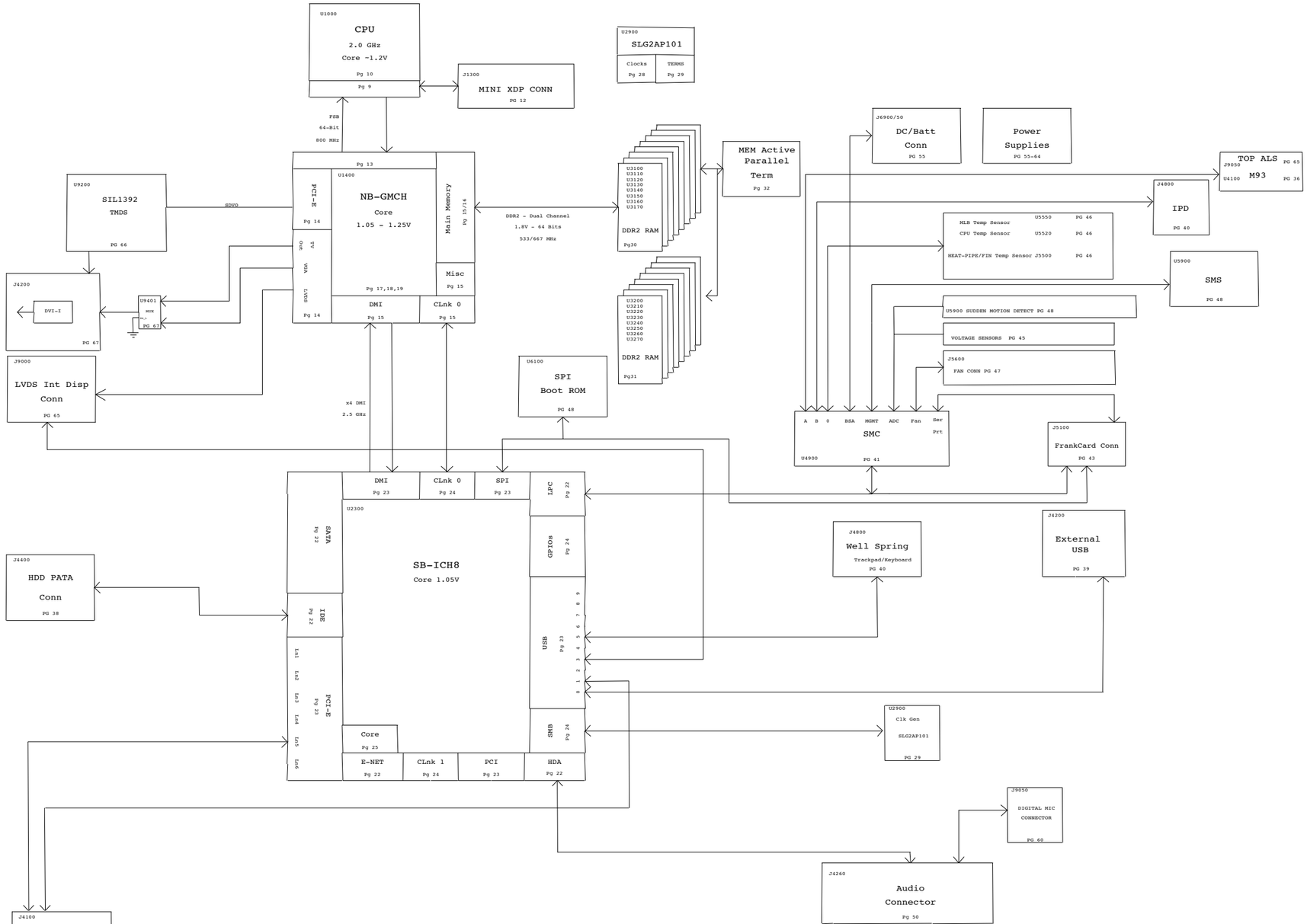
SIZE D

APPLE INC.

TITLE
SCHEM,MLB,M82

DRAWING NUMBER 051-7230 REV. J

SHT 1 OF 109



System Block Diagram

SYNC_MASTER=WFERRY-WF SYNC_DATE=05/11/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J

SCALE NONE SHT 2 OF 109

M82 POWER SYSTEM ARCHITECTURE

AC ADAPTER IN — J6980 — PP18V5_DCIN — 6A FUSE F6900 — =PP18V5_G3H_CHGR

=PPDCIN_G3H — D6901 — PPVBAT_G3H_R — D6901 — PPBUSB_G3H — D6901

ENABLE — 3.425V G3HOT — LT1934 — U7790 — (PAGE 62) — =PPDCIN_G3H — PP3V42_G3H_REG — (? A MAX CURRENT)

PP3V42_G3H_SMC — SMC PWRGD — RN5VD30A-F — U5000 — (PAGE 41) — SMC_RESET_L

SMC_BATT_CHG_EN — ENABLES — PBUS CONVERTER/ BATTERY CHARGER — ISL6258 — U7900 — VIN — (PAGE 63) — CHGR_SMBUS — VOUT

PPVBAT_G3H_CHGR_REG — 7A FUSE — PPBUSB_G3H — R7980 — =PBUSA_G3H

BATTERY 2S2P — Q7950 — R7930 — CHGR_BGATE — BATT_POS_F

VIN — 1.05V — ENA1 — VOUT1 — 1V05S0_RUNSS (S0) — PP1V05_S0_REG — (9.9 A MAX CURRENT)

1.5V — ENA2 — VOUT2 — 1V5S0_RUNSS (S0) — PP1V5_S0_REG — (3.3 A MAX CURRENT)

TPS51124 — U7300 — (PAGE 58) — PGOOD_1V5S0 — PGOOD_1V05S0

CLOCK — SLG2AP101 — U2900 — (PAGE 28) — CLK_PWRGD — PWRGD

NB_RESET_L — TMDS_RST_L — AIRPORT_RST_L — LCDBKLT_PLT_RST_L

ICH8M — CK_PWRGD — VRMPWRGD — PWROK — PWRBTN* — PLTRST* — RSMRST* — CPU_PWRGD(GPIO49) — U2300 — (PAGE 22)

U2803 — VR_PWRGD_CK505 — VR_PWRGD_CLKEN — PLT_RST_L — U2880 — CPU_PWRGD

PM_SB_PWROK — U2801

CPU — PWRGOOD — RESET* — U1000 — (PAGE 9)

CRESTLINE — PWROK — H_CPURST* — U1400 — (PAGE 13) — FSB_CPURST_L

Q7860 — DELAY — R=10K C=0.002uF — P5VS3_EN_L (S3) — DELAY — R=10K C=0.01uF — P3V3S3_EN_L (S3)

CPUVCORE — VIN — VOUT — CLKEN# — VR_ON — PGOOD — ISL6261CRZ — U7100 — (PAGE 56) — IMVP_VR_ON

PPVCORE_S0_CPU_REG — PPVCORE_S0_CPU — (30 A MAX CURRENT) — VR_PWRGD_CK505_L — VR_PWRGOOD_DELAY

PPBUS_G3H — =PPBUSB_G3H

ICH — PM_S4_STATE_L — PM_SLP_S3_L

SMC — PG2 PG3 — U4900 P60 — (PAGE 40) — SMC_PM_G2_EN (S5)

Q7000 — P5V_S0_EN — PP5V_S0 — TPS79933 — U2280 — (PAGE 21) — P3V3_S0_NB_TVDAC (205mA MAX CURRENT)

Q7865 — P5VS3_EN_L — PP5V_S3

VIN — 5V — VO1 — EN1 — 5VS5_RUNSS (S5) — PP5V_S5_REG — (? A MAX CURRENT)

EN2 — 3.3V — VO2 — 3V3S5_RUNSS (S5) — PP3V3_S5_REG — (? A MAX CURRENT)

TPS51120 — U7600 — (PAGE 60) — PGOOD1,2 — RSMRST_PWRGD

Q7866 — P3V3S3_EN_L — PP3V3_S3 — 1V25S0_RUNSS — 1.25V S0 — LTC3412A — U7750 — (PAGE 61) — PP1V25_S0_REG — (3 A MAX CURRENT)

Q7001 — P3V3S0_EN — PP3V3_S0

SMC_ADAPTER_PRESENT — WOW_EN — PM_WLAN_EN_L

GPU_VCORE — VIN — VCC — ADP3209 — U7200 — (PAGE 57) — EN — VOUT — PP5V_S0_NB_GFX_IMVP — GFX_VR_EN — GCORE_EN — =PPVCORE_S0_NB_GFX_IMVP — (13 A MAX CURRENT)

Q7004 — P1V8S0_EN — =PP1V8_S0_FET — =PP1V8_S0_NB_DPLL — MCH DPLL — TPS731125 — U2265 — (PAGE 21) — P1V25_S0_NB_DPLL

PP1V8_S3_FET — PP1V8_S3_REG — (11 A MAX CURRENT)

R7870 — 1V8S3_RUNSS — PM_SLP_S3_L — VIN — VLDOIN — S5 — 1.8V — VOUT1 — S3 — 0.9V — VOUT2 — TPS51116 — U7500 — (PAGE 59) — PP0V9_S0_REG — PGOOD_1V8S3

RUNSS_GATE_D — Q7006 — Q7007 — DELAY — R-330 C-0.022uF — 1V5S0_RUNSS (S0) — R-330 C-0.01uF — 1V05S0_RUNSS (S0) — R-330 C-1000PF — 1V25S0_RUNSS (S0)

U7002 — PP1V25_S0_FET — ALL_SYS_PWRGD_AND — PGOOD_1V5S0 — PGOOD_1V05S0 — PGOOD_SEQUENCER

SMC — RSMRST_OUT(P15) — PWRGD(P12) — 99ms DLY — IMVP_VR_ON(P16) — RSMRST_IN(P13) — PLT_RST* — PWR_BUTTON(P90) — P17(BTN_OUT) — RST* — SLP_S5_L(P95) — SLP_S4_L(P94) — SLP_S3_L(P93) — U4900 — (PAGE 40)

ALL_SYS_PWRGD — RSMRST_PWRGD — SMC_ONOFF_L — BATTERY ONLY: — ADAPTER IN :

PM_RSMRST_L — IMVP_VR_ON — SMC_LRESET_L — PM_PWRBTN_L — SMC_RESET_L

PM_SLP_S5_L — PM_S4_STATE_L — PM_SLP_S3_L

U7000 — RST* — ISL6130IRZA — UVLO_A — UVLO_B — UVLO_C — UVLO)D — ENABLE_1 — (PAGE 56) — GATE A — GATE B — GATE C — GATE D — P5VS0_EN — P3V3S0_EN — P1V8S0_EN — RUNSS_GATE_D

PGOOD_1V8S3 — PP5V_S0_FET — PP3V3_S0_FET — PP1V8_S0_FET — PM_SLP_S3_L

Power Block Diagram

SYNC_MASTER=POWER — SYNC_DATE=06/30/2005

NOTICE OF PROPRIETARY PROPERTY

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 3 OF 109	

BOMs

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7886	PCBA,MLB,1.6GHZ,MI 2GB,SS CAP,M82	EEE_XSC,M82_COMMON,M82_MICRON,CPU_PRQ_1_6GHZ,M82_SS_CAP
630-9024	PCBA,MLB,1.6GHZ,HY 2GB,SS CAP,M82	EEE_YMS,M82_COMMON,M82_HYNIX,CPU_PRQ_1_6GHZ,M82_SS_CAP
630-9133	PCBA,MLB,1.8GHZ,MI 2GB,SS CAP,M82	EEE_Z80,M82_COMMON,M82_MICRON,CPU_PRQ_1_8GHZ,M82_SS_CAP
630-9134	PCBA,MLB,1.8GHZ,HY 2GB,SS CAP,M82	EEE_Z81,M82_COMMON,M82_HYNIX,CPU_PRQ_1_8GHZ,M82_SS_CAP
630-9204	PCBA,MLB,1.6GHZ,HY 2GB,MU CAP,M82	EEE_ZU5,M82_COMMON,M82_HYNIX,CPU_PRQ_1_6GHZ,M82_MU_CAP
630-9205	PCBA,MLB,1.6GHZ,HY 2GB,TY CAP,M82	EEE_ZU6,M82_COMMON,M82_HYNIX,CPU_PRQ_1_6GHZ,M82_TY_CAP
630-9206	PCBA,MLB,1.6GHZ,MI 2GB,MU CAP,M82	EEE_ZU7,M82_COMMON,M82_MICRON,CPU_PRQ_1_6GHZ,M82_MU_CAP
630-9207	PCBA,MLB,1.6GHZ,MI 2GB,TY CAP,M82	EEE_ZU8,M82_COMMON,M82_MICRON,CPU_PRQ_1_6GHZ,M82_TY_CAP
630-9208	PCBA,MLB,1.8GHZ,HY 2GB,MU CAP,M82	EEE_ZU9,M82_COMMON,M82_HYNIX,CPU_PRQ_1_8GHZ,M82_MU_CAP
630-9209	PCBA,MLB,1.8GHZ,HY 2GB,TY CAP,M82	EEE_ZUA,M82_COMMON,M82_HYNIX,CPU_PRQ_1_8GHZ,M82_TY_CAP
630-9210	PCBA,MLB,1.8GHZ,MI 2GB,MU CAP,M82	EEE_ZUB,M82_COMMON,M82_MICRON,CPU_PRQ_1_8GHZ,M82_MU_CAP
630-9211	PCBA,MLB,1.8GHZ,MI 2GB,TY CAP,M82	EEE_ZUC,M82_COMMON,M82_MICRON,CPU_PRQ_1_8GHZ,M82_TY_CAP

Bar Code Label / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:XSC]	CRITICAL	EEE_XSC
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:YMS]	CRITICAL	EEE_YMS
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:Z80]	CRITICAL	EEE_Z80
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:Z81]	CRITICAL	EEE_Z81
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZU5]	CRITICAL	EEE_ZU5
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZU6]	CRITICAL	EEE_ZU6
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZU7]	CRITICAL	EEE_ZU7
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZU8]	CRITICAL	EEE_ZU8
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZU9]	CRITICAL	EEE_ZU9
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZUA]	CRITICAL	EEE_ZUA
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZUB]	CRITICAL	EEE_ZUB
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZUC]	CRITICAL	EEE_ZUC

BOMOPTION Groups

BOM GROUP	BOM OPTIONS
M82_COMMON	ALTERNATE,COMMON,M82_COMMON1,M82_COMMON2,M82_COMMON3
M82_COMMON1	ISL6258,BOOTROM_FINAL,SMC_PRGRM
M82_COMMON2	SMS_MOT_DIS,LPCPLUS,XDP,DRAM_2GB
M82_COMMON3	
M82_MICRON	DRAM_MICRON,DRAM_SPD_1
M82_HYNIX	DRAM_HYNIX,DRAM_SPD_2
M82_HYNIX_LP	DRAM_HYNIX_LP,DRAM_SPD_2
M82_SS_CAP	SS_CAP_1UF,SS_CAP_2_2UF,SS_CAP_10UF
M82_MU_CAP	MU_CAP_1UF,MU_CAP_2_2UF,MU_CAP_10UF
M82_TY_CAP	TY_CAP_1UF,TY_CAP_2_2UF,TY_CAP_10UF

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3522	1	IC,SANTAYNEZ,MEROM,1.6GHZ,ES,20W,956BGA	U1000	CRITICAL	CPU_1_6GHZ
337S3523	1	IC,SANTAYNEZ,MEROM,1.8GHZ,ES,20W,956BGA	U1000	CRITICAL	CPU_1_8GHZ
338S0514	1	IC,965GM,CRESTLINE,USFF BGA	U1400	CRITICAL	
338S0515	1	IC,ICH8M,USFF BGA	U2300	CRITICAL	
359S0130	1	LOW POWER CLOCK SYNTHESIZER,8LG2AP101,68PIN	U2900	CRITICAL	
335S0510	1	IC, 16MBIT 8-PIN SERIAL FLASH,VWQFN	U6100	CRITICAL	BOOTROM_BLANK_2MB
335S0509	1	IC, 32MBIT 8-PIN SERIAL FLASH, WSON8	U6100	CRITICAL	BOOTROM_BLANK_4MB
341S2111	1	IC,EFI,BOOTROM DEVELOPMENT (UNLOCKED),M82	U6100	CRITICAL	BOOTROM_DEVEL
341S2112	1	IC,EFI,BOOTROM FINAL (LOCKED),M82	U6100	CRITICAL	BOOTROM_FINAL
337S3477	1	SST89V54RD MICROCONTROLLER	U9300	CRITICAL	SST8051_BLANK
341S2173	1	IC,PRGM,SST SST89V54RD,UCNTRLR,M82	U9300	CRITICAL	SST8051_PRGRM
338S0422	1	IC,SMC,HS8/2117	U4900	CRITICAL	SMC_BLANK
341S2115	1	IC,PRGRM,SMC (NEW),M82	U4900	CRITICAL	SMC_PRGRM
333S0406	4	MICRON,DRAM,64M16,8x12.5	U3100,U3110,U3120,U3130	CRITICAL	DRAM_MICRON
333S0406	4	MICRON,DRAM,64M16,8x12.5	U3140,U3150,U3160,U3170	CRITICAL	DRAM_MICRON
333S0406	4	MICRON,DRAM,64M16,8x12.5	U3200,U3210,U3220,U3230	CRITICAL	DRAM_MICRON
333S0406	4	MICRON,DRAM,64M16,8x12.5	U3240,U3250,U3260,U3270	CRITICAL	DRAM_MICRON
333S0411	4	HYNIX,DRAM,64M16,8x13	U3100,U3110,U3120,U3130	CRITICAL	DRAM_HYNIX
333S0411	4	HYNIX,DRAM,64M16,8x13	U3140,U3150,U3160,U3170	CRITICAL	DRAM_HYNIX
333S0411	4	HYNIX,DRAM,64M16,8x13	U3200,U3210,U3220,U3230	CRITICAL	DRAM_HYNIX
333S0411	4	HYNIX,DRAM,64M16,8x13	U3240,U3250,U3260,U3270	CRITICAL	DRAM_HYNIX
333S0415	4	HYNIX,DRAM,64M16,8x13,LP	U3100,U3110,U3120,U3130	CRITICAL	DRAM_HYNIX_LP
333S0415	4	HYNIX,DRAM,64M16,8x13,LP	U3140,U3150,U3160,U3170	CRITICAL	DRAM_HYNIX_LP
333S0415	4	HYNIX,DRAM,64M16,8x13,LP	U3200,U3210,U3220,U3230	CRITICAL	DRAM_HYNIX_LP
333S0415	4	HYNIX,DRAM,64M16,8x13,LP	U3240,U3250,U3260,U3270	CRITICAL	DRAM_HYNIX_LP
353S1938	1	IC,ISL6258,REV2,BAT CHGR, 28P QFN	U7900	CRITICAL	ISL6258
197S0213	1	14.318MHZ XTAL, 2.5x2.0	Y9390	CRITICAL	SST8051_14MHZ
197S0231	1	20MHZ XTAL, 2.5x2.0	Y9390	CRITICAL	SST8051_20MHZ
197S0257	1	33MHZ XTAL, 2.5x2.0	Y9390	CRITICAL	SST8051_33MHZ
337S3563	1	IC,SANTAYNEZ,MEROM,1.6GHZ,PRQ,REV3,20W,956BGA	U1000	CRITICAL	CPU_PRQ_1_6GHZ
337S3564	1	IC,SANTAYNEZ,MEROM,1.8GHZ,PRQ,REV3,20W,956BGA	U1000	CRITICAL	CPU_PRQ_1_8GHZ

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
128S0093	128S0092	ALL	33UF 20% 16V DCASE	
376S0466	376S0410	ALL	Si4413 for Si4405	
740S0044	740S0028	ALL	0.5A OC FUSE	
104S0023	104S0018	ALL	1206 1/4W .002 OHM	
152S0684	152S0421	ALL	1.0UH,22A,10MOHM	
338S0616	338S0515	ALL	USFF PRQ ICH8M B2	

CONFIGURATION OPTIONS

SYNC_MASTER=(N/A) SYNC_DATE=(N/A)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 4 OF 109	

1UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0629	5	CAP, 1UF, 6.3V, 10%, 0402	C1801,C1802,C2104,C2201,C2270	CRITICAL	SS_CAP_1UF
138S0629	9	CAP, 1UF, 6.3V, 10%, 0402	C2260,C2280,C2400,C2701,C2800,C2900,C7009,C7108,C7110	CRITICAL	SS_CAP_1UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0628	5	CAP, 1UF, 6.3V, 10%, 0402	C1801,C1802,C2104,C2201,C2270	CRITICAL	MU_CAP_1UF
138S0628	9	CAP, 1UF, 6.3V, 10%, 0402	C2260,C2280,C2400,C2701,C2800,C2900,C7009,C7108,C7110	CRITICAL	MU_CAP_1UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0630	5	CAP, 1UF, 6.3V, 10%, 0402	C1801,C1802,C2104,C2201,C2270	CRITICAL	TY_CAP_1UF
138S0630	9	CAP, 1UF, 6.3V, 10%, 0402	C2260,C2280,C2400,C2701,C2800,C2900,C7009,C7108,C7110	CRITICAL	TY_CAP_1UF

2.2UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240,C1242,C1243,C1244,C1245,C1246,C1247,C1248,C1249	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1250,C1251,C1252,C1253,C1254,C1255,C1256,C1257,C1258,C1259	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1260,C1261,C1262,C1263,C1264,C1265,C1266,C1267	CRITICAL	SS_CAP_2_2UF
138S0632	6	CAP, 2.2UF, 6.3V, 20%, 0402	C2210,C2215,C2240,C2241,C2242,C2243	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9602,C9603,C9604,C9605,C9606,C9607,C9608,C9609	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9610,C9611,C9612,C9613,C9614,C9615,C9616,C9617,C9618,C9619	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9620,C9621,C9622,C9623,C9624,C9625,C9626,C9627,C9628,C9629	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9630,C9631,C9632,C9633,C9634,C9635,C9636,C9637,C9638,C9639	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9640,C9641,C9642,C9643,C9644,C9645,C9646,C9647,C9648,C9649	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C9650,C9651,C9652,C9653,C9654,C9655,C9656,C9657	CRITICAL	SS_CAP_2_2UF
138S0632	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1280,C1281,C1282,C1283,C1287,C1288,C1291,C1292,C1293,C1294,C1295,C1296	CRITICAL	SS_CAP_2_2UF
138S0632	3	CAP, 2.2UF, 6.3V, 20%, 0402	C1422,C1423,C2400	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C2409,C2411,C2412,C2505,C2510,C2511,C2512,C2513,C2514,C2515,C2516	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C2520,C2521,C2522,C2525,C2530,C2531,C2532,C2533,C2534,C2535,C2536	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C2542,C2543,C2545,C2546,C2550,C2551,C2552,C2555	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C2605,C2611,C2612,C2615,C2616,C2617,C2618,C2619,C2620,C2621	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C2622,C2623,C2624,C2625,C2626,C2627,C2628,C2629,C2630,C2631	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C2642,C2643,C2645,C2646,C2650,C2651,C2652,C2655	CRITICAL	SS_CAP_2_2UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240,C1242,C1243,C1244,C1245,C1246,C1247,C1248,C1249	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1250,C1251,C1252,C1253,C1254,C1255,C1256,C1257,C1258,C1259	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1260,C1261,C1262,C1263,C1264,C1265,C1266,C1267	CRITICAL	MU_CAP_2_2UF
138S0633	6	CAP, 2.2UF, 6.3V, 20%, 0402	C2210,C2215,C2240,C2241,C2242,C2243	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9602,C9603,C9604,C9605,C9606,C9607,C9608,C9609	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9610,C9611,C9612,C9613,C9614,C9615,C9616,C9617,C9618,C9619	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9620,C9621,C9622,C9623,C9624,C9625,C9626,C9627,C9628,C9629	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9630,C9631,C9632,C9633,C9634,C9635,C9636,C9637,C9638,C9639	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9640,C9641,C9642,C9643,C9644,C9645,C9646,C9647,C9648,C9649	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C9650,C9651,C9652,C9653,C9654,C9655,C9656,C9657	CRITICAL	MU_CAP_2_2UF
138S0633	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1280,C1281,C1282,C1283,C1287,C1288,C1291,C1292,C1293,C1294,C1295,C1296	CRITICAL	MU_CAP_2_2UF
138S0633	3	CAP, 2.2UF, 6.3V, 20%, 0402	C1422,C1423,C2400	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C2409,C2411,C2412,C2505,C2510,C2511,C2512,C2513,C2514,C2515,C2516	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C2520,C2521,C2522,C2525,C2530,C2531,C2532,C2533,C2534,C2535,C2536	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C2542,C2543,C2545,C2546,C2550,C2551,C2552,C2555	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C2605,C2611,C2612,C2615,C2616,C2617,C2618,C2619,C2620,C2621	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C2622,C2623,C2624,C2625,C2626,C2627,C2628,C2629,C2630,C2631	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C2642,C2643,C2645,C2646,C2650,C2651,C2652,C2655	CRITICAL	MU_CAP_2_2UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240,C1242,C1243,C1244,C1245,C1246,C1247,C1248,C1249	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1250,C1251,C1252,C1253,C1254,C1255,C1256,C1257,C1258,C1259	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1260,C1261,C1262,C1263,C1264,C1265,C1266,C1267	CRITICAL	TY_CAP_2_2UF
138S0634	6	CAP, 2.2UF, 6.3V, 20%, 0402	C2210,C2215,C2240,C2241,C2242,C2243	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9602,C9603,C9604,C9605,C9606,C9607,C9608,C9609	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9610,C9611,C9612,C9613,C9614,C9615,C9616,C9617,C9618,C9619	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9620,C9621,C9622,C9623,C9624,C9625,C9626,C9627,C9628,C9629	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9630,C9631,C9632,C9633,C9634,C9635,C9636,C9637,C9638,C9639	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9640,C9641,C9642,C9643,C9644,C9645,C9646,C9647,C9648,C9649	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C9650,C9651,C9652,C9653,C9654,C9655,C9656,C9657	CRITICAL	TY_CAP_2_2UF
138S0634	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1280,C1281,C1282,C1283,C1287,C1288,C1291,C1292,C1293,C1294,C1295,C1296	CRITICAL	TY_CAP_2_2UF
138S0634	3	CAP, 2.2UF, 6.3V, 20%, 0402	C1422,C1423,C2400	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C2409,C2411,C2412,C2505,C2510,C2511,C2512,C2513,C2514,C2515,C2516	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C2520,C2521,C2522,C2525,C2530,C2531,C2532,C2533,C2534,C2535,C2536	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C2542,C2543,C2545,C2546,C2550,C2551,C2552,C2555	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C2605,C2611,C2612,C2615,C2616,C2617,C2618,C2619,C2620,C2621	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C2622,C2623,C2624,C2625,C2626,C2627,C2628,C2629,C2630,C2631	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C2642,C2643,C2645,C2646,C2650,C2651,C2652,C2655	CRITICAL	TY_CAP_2_2UF

10UF 0603 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0626	10	CAP, 10UF, 6.3V, 20%, 0603	C1200,C1201,C1202,C1203,C1204,C1205,C1206,C1207,C1208,C1209	CRITICAL	SS_CAP_10UF
138S0626	10	CAP, 10UF, 6.3V, 20%, 0603	C1210,C1211,C1212,C1213,C1214,C1215,C1216,C1217,C1218,C1219	CRITICAL	SS_CAP_10UF
138S0626	10	CAP, 10UF, 6.3V, 20%, 0603	C1220,C1221,C1222,C1223,C1224,C1225,C1226,C1227,C1228,C1229	CRITICAL	SS_CAP_10UF
138S0626	3	CAP, 10UF, 6.3V, 20%, 0603	C1230,C1231,C1240	CRITICAL	SS_CAP_10UF
138S0626	9	CAP, 10UF, 6.3V, 20%, 0603	C2190,C2191,C2211,C2219,C2231,C2232,C2260,C2264,C2265	CRITICAL	SS_CAP_10UF
138S0626	5	CAP, 10UF, 6.3V, 20%, 0603	C2750,C2756,C2758,C2770,C2801	CRITICAL	SS_CAP_10UF
138S0626	6	CAP, 10UF, 6.3V, 20%, 0603	C2190,C2191,C2192,C2260,C2261,C2262	CRITICAL	SS_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	C2199,C2488,C2611,C2684,C7281,C7350,C7351	CRITICAL	SS_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	C7552,C7567,C7568,C7571,C7601,C7604,C7680,C7690	CRITICAL	SS_CAP_10UF
138S0626	5	CAP, 10UF, 6.3V, 20%, 0603	C9012,C9036,C9055,C9211,C9240	CRITICAL	SS_CAP_10UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0625	10	CAP, 10UF, 6.3V, 20%, 0603	C1200,C1201,C1202,C1203,C1204,C1205,C1206,C1207,C1208,C1209	CRITICAL	MU_CAP_10UF
138S0625	10	CAP, 10UF, 6.3V, 20%, 0603	C1210,C1211,C1212,C1213,C1214,C1215,C1216,C1217,C1218,C1219	CRITICAL	MU_CAP_10UF
138S0625	10	CAP, 10UF, 6.3V, 20%, 0603	C1220,C1221,C1222,C1223,C1224,C1225,C1226,C1227,C1228,C1229	CRITICAL	MU_CAP_10UF
138S0625	3	CAP, 10UF, 6.3V, 20%, 0603	C1230,C1231,C1240	CRITICAL	MU_CAP_10UF
138S0625	9	CAP, 10UF, 6.3V, 20%, 0603	C2190,C2191,C2211,C2219,C2231,C2232,C2260,C2264,C2265	CRITICAL	MU_CAP_10UF
138S0625	5	CAP, 10UF, 6.3V, 20%, 0603	C2750,C2756,C2758,C2770,C2801	CRITICAL	MU_CAP_10UF
138S0625	6	CAP, 10UF, 6.3V, 20%, 0603	C2190,C2191,C2192,C2260,C2261,C2262	CRITICAL	MU_CAP_10UF
138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	C2199,C2488,C2611,C2684,C7281,C7350,C7351	CRITICAL	MU_CAP_10UF
138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	C7552,C7567,C7568,C7571,C7601,C7604,C7680,C7690	CRITICAL	MU_CAP_10UF
138S0625	5	CAP, 10UF, 6.3V, 20%, 0603	C9012,C9036,C9055,C9211,C9240	CRITICAL	MU_CAP_10UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0627	10	CAP, 10UF, 6.3V, 20%, 0603	C1200,C1201,C1202,C1203,C1204,C1205,C1206,C1207,C1208,C1209	CRITICAL	TY_CAP_10UF
138S0627	10	CAP, 10UF, 6.3V, 20%, 0603	C1210,C1211,C1212,C1213,C1214,C1215,C1216,C1217,C1218,C1219	CRITICAL	TY_CAP_10UF
138S0627	10	CAP, 10UF, 6.3V, 20%, 0603	C1220,C1221,C1222,C1223,C1224,C1225,C1226,C1227,C1228,C1229	CRITICAL	TY_CAP_10UF
138S0627	3	CAP, 10UF, 6.3V, 20%, 0603	C1230,C1231,C1240	CRITICAL	TY_CAP_10UF
138S0627	9	CAP, 10UF, 6.3V, 20%, 0603	C2190,C2191,C2211,C2219,C2231,C2232,C2260,C2264,C2265	CRITICAL	TY_CAP_10UF
138S0627	5	CAP, 10UF, 6.3V, 20%, 0603	C2750,C2756,C2758,C2770,C2801	CRITICAL	TY_CAP_10UF
138S0627	6	CAP, 10UF, 6.3V, 20%, 0603	C2190,C2191,C2192,C2260,C2261,C2262	CRITICAL	TY_CAP_10UF
138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	C2199,C2488,C2611,C2684,C7281,C7350,C7351	CRITICAL	TY_CAP_10UF
138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	C7552,C7567,C7568,C7571,C7601,C7604,C7680,C7690	CRITICAL	TY_CAP_10UF
138S0627	5	CAP, 10UF, 6.3V, 20%, 0603	C9012,C9036,C9055,C9211,C9240	CRITICAL	TY_CAP_10UF

Acoustic Cap BOM Config Tables

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J

SCALE NONE SHT 5 OF 109

ICT Test Points

ICT_TEST

These nets have a ICT_TEST property   This indicates a MUSTHAVE requirement for ICT

	TRUE	PP18V5_DCIN	6 7 50 72
I95	TRUE	BATT_POS	6 7 50
I96	TRUE	PP3V3_S5	7 8 72
I97	TRUE	PP3V42_G3H	6 7 8 72
	TRUE	GND	
I100	TRUE	PM_SLP_S3_L	6 7 25 36 37 41 42 51 55
I99	TRUE	PM_S4_STATE_L	6 25 36 41 58
I101	TRUE	PM_SLP_S5_L	6 25 41 42
I102	TRUE	SMC_PM_G2_EN	6 41 58
I104	TRUE	IMVP_VR_ON	6 41 52
I103	TRUE	GFX_VR_EN	6 9 53
I105	TRUE	SMC_BATT_CHG_EN	6 41 42
I107	TRUE	SMC_ONOFF_L	6 7 40 41 42
I106	TRUE	ALL_SYS_PWRGD_AND	6 51
I108	TRUE	PPVBAT_G3H_CHGR_REG	6 59 72
I109	TRUE	CPU_PWRGD	6 10 13 23 66
I110	TRUE	PM_RSMRST_L	6 25 41
I112	TRUE	PM_PWRBTN_L	6 25 41
I111	TRUE	TP_PCI_RST_L	9
I113	TRUE	PLT_RST_L	6 7 24 28
I115	TRUE	SMC_RESET_L	6 41 42 43
I114	TRUE	PM_SYSRST_L	6 25 28 41
I116	TRUE	PP1V5_S0	6 7 8 72
I118	TRUE	PP1V05_S0	6 7 8 72
I117	TRUE	PP1V8_S0	6 7 8 72
I119	TRUE	PP1V8_S3	6 7 8 72
I120	TRUE	PP0V9_S0	6 7 8 72
I121	TRUE	PP0V9_S3	6 8 72
I122	TRUE	PP1V25_S0	6 7 8 72
I123	TRUE	PP5V_S5	6 7 8 72
I125	TRUE	PP5V_S3	6 7 8 72
I124	TRUE	PP5V_S0	6 7 8 72
I292	TRUE	PP3V3_S3	6 7 8 72
I294	TRUE	PP3V3_A_S0	6 8
I293	TRUE	PP3V3_B_S0	6 8
I295	TRUE	PPVCORE_S0_CPU	6 7 8 72
I297	TRUE	PPVCORE_S0_NB_GFX	6 7 8 72
I296	TRUE	XDP_TCK	6 7 10 13 66
I298	TRUE	XDP_TDI	6 7 10 13 66
I300	TRUE	XDP_TDO	6 7 10 13 66
I299	TRUE	XDP_TMS	6 7 10 13 66
I301	TRUE	XDP_TRST_L	6 7 10 13 66
I302	TRUE	XDP_CPURST_L	6 7 13 66
I303	TRUE	XDP_BPM_L<4>	6 7 10 13 66
I304	TRUE	XDP_BPM_L<5>	6 7 10 13 66
I305	TRUE	XDP_DBRESET_L	6 7 10 13 28
I307	TRUE	XDP_PWRGD	6 7 13
I306	TRUE	SPI_A_SCLK_R	6 43 49 69
I308	TRUE	SMC_MANUAL_RST_L	6 42
I309	TRUE	SMC_TCK	6 41 42 43
I310	TRUE	SMC_TDI	6 41 42 43
I338	TRUE	SMC_TDO	6 41 42 43
I337	TRUE	SMC_TMS	6 41 42 43
I339	TRUE	SMC_TRST_L	6 41 43
I341	TRUE	CPU_A20M_L	6 10 23 66
I340	TRUE	CPU_DPRSTP_L	6 10 16 23 52 66
I343	TRUE	CPU_DPSLP_L	6 10 23 66
I342	TRUE	CPU_FERR_L	6 10 23 66
I344	TRUE	NB_BSEL<0>	6 7 13 16 30 66
I346	TRUE	NB_BSEL<1>	6 7 13 16 30 66
I345	TRUE	NB_BSEL<2>	6 7 13 16 30 66
I347	TRUE	NB_CFG<16>	6 16
I348	TRUE	NB_CFG<19>	6 16
I349	TRUE	NB_CFG<20>	6 16

I126	TRUE	NB_CFG<3>	6 7 13 16
I128	TRUE	NB_CFG<4>	6 7 13 16
I127	TRUE	NB_CFG<5>	6 7 13 16
I129	TRUE	NB_CFG<6>	6 7 13 16
I131	TRUE	NB_CFG<7>	6 7 13 16
I130	TRUE	NB_CFG<8>	6 7 13 16
I132	TRUE	NB_CFG<9>	6 16
I134	TRUE	NB_RESET_L	6 16 28
I133	TRUE	NB_SB_SYNC_L	6 16 25
I135	TRUE	NB_TEST1	6 16
I136	TRUE	NB_TEST2	6 16
I137	TRUE	1V05S0_RUNSS	51 54
I138	TRUE	1V05S0_TRIP	54
I139	TRUE	1V25S0_RUNSS	51 57
I141	TRUE	1V51V05S0_V5FILT	54
I140	TRUE	1V5S0_RUNSS	51 54
I142	TRUE	1V5S0_TRIP	54
I143	TRUE	1V8S3_CS	55
I144	TRUE	1V8S3_V5FILT	55
I146	TRUE	1V8S3_VDDQSET	55
I145	TRUE	3V3S5_CS	56
I147	TRUE	5V3V3S5_TONSEL	56
I149	TRUE	5V3V3S5_V5FILT	56
I148	TRUE	5V3V3S5_VREF	56
I151	TRUE	5V3V3S5_VREG3	56
I150	TRUE	5VS5_CS	56
I152	TRUE	5VS5_VREG	56
I154	TRUE	ADAPTER_SENSE	50
I153	TRUE	AIRPORT_RST_L	7 28 36
I155	TRUE	ALL_SYSPWRGD_DLY	51
I156	TRUE	ALL_SYS_PWRGD	28 41 51 52
I157	TRUE	ALL_SYS_PWRGD_AND	6 51
I273	TRUE	ARB_DETECT_L	25
I274	TRUE	AUD_MIC_CLK	7 37 60
I275	TRUE	AUD_MIC_CLK_F	60
I276	TRUE	AUD_MIC_DATA	7 37 60
I277	TRUE	AUD_MIC_DATA_F	60
I278	TRUE	BATT_POS	6 7 50
I279	TRUE	BATT_POS_F	50 59
I280	TRUE	BOOTROM_OVR_EN_L	23 25 43
I281	TRUE	CHGR_AGATE	59
I283	TRUE	CHGR_AMON	59
I282	TRUE	CHGR_BGATE	59
I284	TRUE	CHGR_BMON	59
I286	TRUE	CHGR_BOOT	59
I285	TRUE	CHGR_CSIN	59
I287	TRUE	CHGR_CSIP	59
I288	TRUE	CHGR_CSON	59
I289	TRUE	CHGR_CSOP	59
I291	TRUE	CHGR_DCIN	59
I290	TRUE	CHGR_LOWCURRENT_GATE	59
I324	TRUE	CHGR_LOWCURRENT_REF	59
I325	TRUE	CHGR_SGATE	59
I326	TRUE	CHGR_SGATE_DIV	59
I327	TRUE	CHGR_VCOMP_R	59
I328	TRUE	CHGR_VDD	59
I329	TRUE	CHGR_VDDP	59
I330	TRUE	CHGR_VNEG	59
I331	TRUE	CHGR_VNEG_R	59
I332	TRUE	CK505_CLK14P3M_TIMER	29 30
I333	TRUE	CK505_FSA	30 71
I334	TRUE	CK505_FSB_TEST_MODE	29 30
I336	TRUE	CK505_FSC	30 71
I335	TRUE	CK505_PCI3_CLK	29 30 71

I158	TRUE	CK505_PCI5_FCTSEL1	29 30
I160	TRUE	CK505_PCIF0_CLK	29 30
I159	TRUE	CK505_PCIF1_CLK	29 30 71
I161	TRUE	CK505_SRC_CLKREQ6_L	7 29 36
I163	TRUE	CK505_USB48_FSA	29 30
I162	TRUE	CK505_XTAL_OUT	29
I164	TRUE	CLINK_NB_CLK	16 25 70
I166	TRUE	CLINK_NB_DATA	16 25 70
I165	TRUE	CLINK_NB_RESET_L	16 25 70
I167	TRUE	CLK_PWRGD	25 29
I168	TRUE	CPU_A20M_L	6 10 23 66
I169	TRUE	CPU_BSEL<0>	10 30 66
I170	TRUE	CPU_BSEL<1>	10 30 66
I171	TRUE	CPU_BSEL<2>	10 30 66
I173	TRUE	CPU_COMP<0>	10 66
I172	TRUE	CPU_COMP<1>	10 66
I174	TRUE	CPU_COMP<2>	10 66
I175	TRUE	CPU_COMP<3>	10 66
I176	TRUE	CPU_DPRSTP_L	6 10 16 23 52 66
I178	TRUE	CPU_DPSLP_L	6 10 23 66
I177	TRUE	CPU_FERR_L	6 10 23 66
I179	TRUE	CPU_GTLREF	10 66
I181	TRUE	CPU_IERR_L	10 66
I180	TRUE	CPU_IGNNE_L	10 23 66
I183	TRUE	CPU_INIT_L	10 23 66
I182	TRUE	CPU_INTR	10 23 66
I184	TRUE	CPU_NMI	10 23 66
I186	TRUE	CPU_PROCHOT_BUF	42
I185	TRUE	CPU_PROCHOT_L	10 42 52 66
I187	TRUE	CPU_PROCHOT_L_R	42
I188	TRUE	CPU_PWRGD	6 10 13 23 66
I189	TRUE	CPU_SMI_L	10 23 66
I254	TRUE	CPU_STPCLK_L	10 23 66
I255	TRUE	CPU_THERMD_N	10 46 66
I256	TRUE	CPU_THERMD_P	10 46 66
I257	TRUE	CPU_THERMTRIP_R	23
I258	TRUE	CPU_VCCSENSE_N	11 52 66
I259	TRUE	CPU_VCCSENSE_P	11 52 66
I260	TRUE	CPU_VID<6..0>	11 12 52 66
I261	TRUE	CRT_BLUE	63 67
I262	TRUE	CRT_GREEN	63 67
I264	TRUE	CRT_HSYNC_LS	63
I263	TRUE	CRT_HSYNC_LS_R	63
I265	TRUE	CRT_HSYNC_R	63 67
I267	TRUE	CRT_RED	63 67
I266	TRUE	CRT_TVO_IREF	63 67
I268	TRUE	CRT_VSYNC_LS	63
I269	TRUE	CRT_VSYNC_LS_R	63
I270	TRUE	CRT_VSYNC_R	63 67
I272	TRUE	DEBUG_RESET_L	28 43
I271	TRUE	DLY_OFF_A	51
I311	TRUE	DLY_OFF_B	51
I312	TRUE	DLY_OFF_C	51
I313	TRUE	DLY_OFF_D	51
I314	TRUE	DMI_IRCOMP_R	24
I315	TRUE	DMI_N2S_N<3..0>	16 24 67
I316	TRUE	DMI_N2S_P<3..0>	16 24 67
I317	TRUE	DMI_S2N_N<3..0>	16 24 67
I318	TRUE	DMI_S2N_P<3..0>	16 24 67
I319	TRUE	DVI_HOST	7 37 63
I320	TRUE	DVI_HOTPLUG_DET	24 61 62
I321	TRUE	DVI_HOTPLUG_DET_BUF	61 62
I323	TRUE	DVI_HOTPLUG_DET_DEL_L	62
I322	TRUE	DVI_HOTPLUG_DET_INT_L	62

I190	TRUE	DVI_HPDET_RC	62
I192	TRUE	EXCARD_OC_L	24
I191	TRUE	EXTAUSB_OC_F_L	39
I193	TRUE	EXTAUSB_OC_L	9
I195	TRUE	EXTBUSB_OC_L	9
I194	TRUE	EXTGPU_LVDS_EN	7 13 24
I196	TRUE	EXT_COMPVID_B	63 67
I198	TRUE	EXT_C_R	63 67
I197	TRUE	EXT_Y_G	63 67
I199	TRUE	FAN_RT_PWM	7 47
I200	TRUE	FAN_RT_TACH	7 47
I201	TRUE	FRANKCARD_GPIO	25 43
I202	TRUE	FSB_CLK_CPU_N	10 30 71
I203	TRUE	FSB_CLK_CPU_P	10 30 71
I205	TRUE	FSB_CLK_NB_N	14 30 71
I204	TRUE	FSB_CLK_NB_P	14 30 71
I206	TRUE	FSB_CPURST_L	10 13 14 66
I207	TRUE	FWH_MFG_MODE	25
I208	TRUE	GCORE_BST_D	53
I210	TRUE	GCORE_COMP_R	53
I209	TRUE	GCORE_CSFB	53
I211	TRUE	GCORE_FBRTN	53
I213	TRUE	GCORE_LLINE	53
I212	TRUE	GCORE_PMON	53
I215	TRUE	GCORE_PMONFS	53
I214	TRUE	GCORE_PWRGD	53
I216	TRUE	GCORE_RAMP	53
I218	TRUE	GCORE_RPM	53
I217	TRUE	GCORE_RT	53
I219	TRUE	GCORE_ST	53
I220	TRUE	GCORE_SW	53
I221	TRUE	GCORE_SW_R	53
I222	TRUE	GCORE_VARFREQ	53
I223	TRUE	GCORE_VCC	53
I224	TRUE	GCORE_VDC_DIV	53
I225	TRUE	GCORE_VRPM	53
I226	TRUE	GFX_VID<3..0>	16 22 53
I227	TRUE	GFX_VR_EN	6 9 53
I228	TRUE	GLAN_COMP	23 70
I229	TRUE	GND_1V51V05S0_SGND	54
I230	TRUE	GND_1V8S3_CSGND	55
I232	TRUE	GND_1V8S3_SGND	55
I231	TRUE	GND_5V3V3S5_SGND	56
I233	TRUE	GND_ALS_F	
I235	TRUE	GND_CHGR_SGND	59
I234	TRUE	GND_GCORE_PGND	53
I236	TRUE	GND_IMVP6_SGND	52
I237	TRUE	GND_LCDBKLT_GNDA	64
I238	TRUE	GND_P1V2S3_SGND	57
I240	TRUE	GND_SMC_AVSS	41 42 45 53 59
I239	TRUE	HDA_BIT_CLK	9 23 69
I241	TRUE	HDA_BIT_CLK_R	23 69
I242	TRUE	HDA_DOCK_EN_L	23
I243	TRUE	HDA_RST_L	9 23 37 69
I244	TRUE	HDA_RST_L_R	23 69
I245	TRUE	HDA_SDIN0	9 23 69
I246	TRUE	HDA_SDIN1	
I247	TRUE	HDA_SDOUT	9 23 69
I248	TRUE	HDA_SDOUT_R	23 69
I249	TRUE	HDA_SYNC	7 9 23 37 69
I250	TRUE	HDA_SYNC_R	23 69
I251	TRUE	HDMI_HOST	7 37 63
I253	TRUE	I2C_TOP_ALS_SCL_F	60
I252	TRUE	I2C_TOP_ALS_SDA_F	60

I414	TRUE	IDE_IRQ14	23 38 69
I415	TRUE	IDE_PDA<2..0>	23 38 69
I416	TRUE	IDE_PDCS1_L	23 38 69
I417	TRUE	IDE_PDCS3_L	23 38 69
I418	TRUE	IDE_PDD<15..0>	23 38 69
I419	TRUE	IDE_PDDACK_L	23 38 69
I420	TRUE	IDE_PDDREQ	23 38 69
I421	TRUE	IDE_PDIORDY	23 38 69
I422	TRUE	IDE_PDIOR_L	23 38 69
I424	TRUE	IDE_PDIOW_L	23 38 69
I423	TRUE	IDE_RESET_BUF_L	38
I425	TRUE	IDE_RESET_L	24 38
I427	TRUE	IMVP6_BOOT	52
I426	TRUE	IMVP6_BOOT_RC	52
I428	TRUE	IMVP6_COMP_R	52
I429	TRUE	IMVP6_DROOP	52
I430	TRUE	IMVP6_PHASE	52
I432	TRUE	IMVP6_PVCC	52
I431	TRUE	IMVP6_RBIAS	52
I433	TRUE	IMVP6_SOFT	52
I434	TRUE	IMVP6_VDIFF	52
I435	TRUE	IMVP6_VDIFF_RC	52
I436	TRUE	IMVP6_VO_R	52
I437	TRUE	IMVP6_VR_TT	52
I438	TRUE	IMVP6_VSEN_N	52 66
I439	TRUE	IMVP6_VSEN_P	52 66
I440	TRUE	IMVP6_VSUM	52
I441	TRUE	IMVP6_VW	52
I442	TRUE	IMVP_DPRSLPVR	52 66
I443	TRUE	IMVP_VR_ON	6 41 52
I445	TRUE	INT_PIRQA_L	24 70
I444	TRUE	INT_PIRQB_L	24 70
I447	TRUE	INT_PIRQC_L	24 70
I446	TRUE	INT_PIRQD_L	24 70
I448	TRUE	INT_PIRQE_L	24 70
I450	TRUE	INT_PIRQF_L	24 70
I449	TRUE	INT_SERIRQ	25 41 43
I452	TRUE	LAN_ENERGY_DET	23
I451	TRUE	LAN_PHYPC	23 25
I453	TRUE	LCDBKLT_ENA	64
I455	TRUE	LCDBKLT_ISET	64
I454	TRUE	LCDBKLT_OVP	64
I457	TRUE	LCDBKLT_PWM_UNBUF	9 64
I456	TRUE	LCDBKLT_PWREN	9 64
I458	TRUE	LCDBKLT_RT	64
I460	TRUE	LCDBKLT_RTN<6..1>	7 60 64
I459	TRUE	LCDBKLT_RTN_RC<6..1>	64
I462	TRUE	LCDBKLT_SSTCMP	64
I461	TRUE	LCDBKLT_SSTCMP_RC	64
I463	TRUE	LCDBKLT_VREF	64
I465	TRUE	LCDVDD_PWREN_L	60
I464	TRUE	LCDVDD_PWREN_L_R	60
I466	TRUE	LOCAL_CTRL_CLK	7 13 15
I468	TRUE	LOCAL_CTRL_DATA	7 13 15
I467	TRUE	LPC_AD<3..0>	23 41 43
I470	TRUE	LPC_FRAME_L	23 41 43
I469	TRUE	LSOC_H	
I471	TRUE	LSOC_H_R	7
I473	TRUE	LVDS_A_CLK_F_N	7 60
I472	TRUE	LVDS_A_CLK_F_P	7 60
I475	TRUE	LVDS_A_CLK_N	15 60 67
I474	TRUE	LVDS_A_CLK_P	15 60 67
I476	TRUE	LVDS_A_DATA_F_N<2..0>	60 67
I477	TRUE	LVDS_A_DATA_F_P<2..0>	60 67

I350	TRUE	LVDS_A_DATA_N<2>	7 15 60 67
I351	TRUE	LVDS_A_DATA_P<2>	7 15 60 67
I352	TRUE	LVDS_DDC_CLK	7 15 60
I353	TRUE	LVDS_DDC_DATA	7 15 60
I354	TRUE	LVDS_IBG	15 60 67
I355	TRUE	LVDS_VDD_EN	15 60
I356	TRUE	MEM_ODT<3..0>	16 31 32 33 68
I357	TRUE	MEM_RCOMP	16
I358	TRUE	MEM_RCOMP_L	16
I360	TRUE	MEM_RCOMP_VOH	16
I359	TRUE	MEM_RCOMP_VOL	16
I361	TRUE	NB_BSEL<0>	6 7 13 16 30 66
I363	TRUE	NB_BSEL<1>	6 7 13 16 30 66
I362	TRUE	NB_BSEL<2>	6 7 13 16 30 66
I364	TRUE	NB_CFG<16>	6 16
I365	TRUE	NB_CFG<19>	6 16
I366	TRUE	NB_CFG<20>	6 16
I368	TRUE	NB_CFG<3>	6 7 13 16
I367	TRUE	NB_CFG<4>	6 7 13 16
I369	TRUE	NB_CFG<5>	6 7 13 16
I370	TRUE	NB_CFG<6>	6 7 13 16
I371	TRUE	NB_CFG<7>	6 7 13 16
I372	TRUE	NB_CFG<8>	6 7 13 16
I373	TRUE	NB_CFG<9>	6 16
I374	TRUE	NB_CLINK_VREF	16 70
I375	TRUE	NB_CLK100M_DPLLSS_N	9 30 71
I376	TRUE	NB_CLK100M_DPLLSS_P	9 30 71
I377	TRUE	NB_CLK100M_PCIE_N	16 30 71
I378	TRUE	NB_CLK100M_PCIE_P	16 30 71
I379	TRUE	NB_CLK96M_DOT_N	9 30 71
I381	TRUE	NB_CLK96M_DOT_P	9 30 71
I380	TRUE	NB_CLKREQ_L	16 29
I383	TRUE	NB_FSB_RCOMP	14
I382	TRUE	NB_FSB_SCOMP	14
I384	TRUE	NB_FSB_SCOMP_L	14
I386	TRUE	NB_FSB_SWING	14
I385	TRUE	NB_FSB_VREF	14
I388	TRUE	NB_RESET_L	6 16 28
I387	TRUE	NB_SB_SYNC_L	6 16 25
I389	TRUE	NB_TEST1	6 16
I391	TRUE	NB_TEST2	6 16
I390	TRUE	NB_VCCSM_LF1	18 68
I393	TRUE	NB_VCCSM_LF2	18 68
I392	TRUE	NB_VCCSM_LF3	18 68
I394	TRUE	NB_VCCSM_LF4	18 68
I396	TRUE	NB_VCCSM_LF5	18 68
I395	TRUE	NB_VCCSM_LF6	18 68
I398	TRUE	NB_VCCSM_LF7	18 68
I397	TRUE	NB_VTTLF_CAP1	19
I399	TRUE	NB_VTTLF_CAP2	19
I401	TRUE	NB_VTTLF_CAP3	19
I400	TRUE	ODD_PWR_EN_L	24
I402	TRUE	ONEWIRE_DCIN_DIV	50
I404	TRUE	ONEWIRE_EN	50
I403	TRUE	ONEWIRE_ESD	50
I406	TRUE	ONEWIRE_OV	50
I405	TRUE	ONEWIRE_PWR_EN_L	50
I407	TRUE	ONEWIRE_PWR_EN_L_DIV	50
I409	TRUE	P1V25S0NBDPLL_FB	22
I408	TRUE	P1V25S0NBDPLL_RF	22
I411	TRUE	P1V25S0_ITH	57
I410	TRUE	P1V25S0_ITH_RC	57
I412	TRUE	P1V25S0_MODE	57
I413	TRUE	P1V25S0_RT	57

I478	TRUE	P1V8S0_EN	51
I480	TRUE	P3V3S0_EN	51
I479	TRUE	P3V3S3_EN_L	58
I481	TRUE	P3V3TVDAC_EN_RC	22
I482	TRUE	P3V3TVDAC_NOISE	22
I483	TRUE	P3V42G3H5_BOOST	57
I485	TRUE	P3V42G3H_SHDN_L	57
I484	TRUE	P3V42G3H_SHDN_L1	57
I486	TRUE	P5VS0_EN	51
I487	TRUE	P5VS3_EN_L	58
I488	TRUE	PBUS_ISENSE_IN_NEG	59
I490	TRUE	PBUS_ISENSE_VREG	59
I489	TRUE	PBUS_S0_SMC_VSENSE	45
I517	TRUE	PBUS_SMC_VSENSE_EN_L	59 42 45
I519	TRUE	PCIE_CLK100M_MINI_N	71 30 36
I518	TRUE	PCIE_CLK100M_MINI_N_F	7 36
I520	TRUE	PCIE_CLK100M_MINI_P	71 30 36
I521	TRUE	PCIE_CLK100M_MINI_P_F	7 36
I522	TRUE	PCIE_E_D2R_N	36
I523	TRUE	PCIE_E_D2R_N_F	7 36
I524	TRUE	PCIE_E_D2R_P	36
I525	TRUE	PCIE_E_D2R_P_F	7 36
I527	TRUE	PCIE_E_R2D_C_N	36
I526	TRUE	PCIE_E_R2D_C_N_F	7 36
I528	TRUE	PCIE_E_R2D_C_P	36
I529	TRUE	PCIE_E_R2D_C_P_F	7 36
I551	TRUE	PCIE_E_R2D_N	36
I553	TRUE	PCIE_E_R2D_P	36
I552	TRUE	PCIE_WAKE_L	7 25 36
I554	TRUE	PCI_CLK33M_LPCPLUS	30 43 71
I555	TRUE	PCI_CLK33M_SB	24 30 71
I556	TRUE	PCI_CLK33M_SMC	30 41 71
I557	TRUE	PCI_DEVSEL_L	24 70
I558	TRUE	PCI_FRAME_L	24 70
I559	TRUE	PCI_FW_GNT_L	24 70
I561	TRUE	PCI_FW_REQ_L	24 70
I560	TRUE	PCI_IRDY_L	24 70
I562	TRUE	PCI_LOCK_L	24 70
I563	TRUE	PCI_PERR_L	24 70
I564	TRUE	PCI_PME_FW_L	25
I565	TRUE	PCI_REQ1_L	24 70
I566	TRUE	PCI_REQ2_L	24 70
I568	TRUE	PCI_SERR_L	24 70
I567	TRUE	PCI_STOP_L	24 70
I569	TRUE	PCI_TRDY_L	24 70
I571	TRUE	PEG_COMP	15
I570	TRUE	PEG_D2R_N<1>	15 61 67
I577	TRUE	PEG_D2R_P<1>	15 61 67
I578	TRUE	PEG_R2D_C_N<3..0>	15 61 67
I579	TRUE	PEG_R2D_C_P<3..0>	15 61 67
I580	TRUE	PGOOD_1V25S0	51 57
I581	TRUE	PGOOD_1V8S3	51 55
I601	TRUE	PLT_RST_BUF_L	28
I603	TRUE	PLT_RST_L	6 7 24 28
I602	TRUE	PM_BATLOW_L	25 41
I604	TRUE	PM_BMBUSY_L	16 25
I606	TRUE	PM_CLKRUN_L	25 41 43
I605	TRUE	PM_DPRSLPVR	16 25 52 66
I608	TRUE	PM_EXTTS_L<0>	16 41
I607	TRUE	PM_EXTTS_L<1>	16 41
I609	TRUE	PM_LAN_ENABLE	25 41
I611	TRUE	PM_LAN_PWRGD	41 42
I610	TRUE	PM_LATRIGGER_L	7 13 24
I612	TRUE	PM_PWRBTN_L	6 25 41
I613	TRUE	PM_RI_L	25
I614	TRUE	PM_RSMRST_L	6 25 41
I616	TRUE	PM_S4_STATE_L	6 25 36 41 58
I615	TRUE	PM_SB_PWROK	9 25 28
I618	TRUE	PM_SLP_S3_L	51 55 6 7 25 36 37 41 42
I617	TRUE	PM_SLP_S4_LS5V	39 58
I619	TRUE	PM_SLP_S5_L	6 25 41 42
I836	TRUE	PM_STPCPU_L	25 29 30
I835	TRUE	PM_STPPCI_L	25 29 30
I837	TRUE	PM_SUS_STAT_L	25 41 43
I839	TRUE	PM_SYSRST_L	6 25 28 41
I838	TRUE	PM_THRMTRIP_L	10 16 23 42 66
I849	TRUE	PM_THRM_L	25
I850	TRUE	PM_WLAN_EN_L	36
I851	TRUE	PM_WLAN_EN_L1	36
I853	TRUE	PM_WLAN_EN_L2	36
I852	TRUE	PM_WLAN_EN_L_SS	36
I855	TRUE	PP0V9_S0	6 7 8 72
I854	TRUE	PP0V9_S3	6 8 72
I856	TRUE	PP18V5_DCIN	6 7 50 72

I493	TRUE	PP18V5_DCIN_ONEWIRE	50 72
I492	TRUE	PP18V5_G3H	7 8 72
I494	TRUE	PP18V5_S5_CHGR_SW_R	59 72
I495	TRUE	PP1V05_S0	6 7 8 72
I496	TRUE	PP1V05_S0_NB_VCCPEG	15 19 21 72
I498	TRUE	PP1V25_S0	6 7 8 72
I497	TRUE	PP1V25_S0M_NB_VCCA_HPLL	19 21 72
I499	TRUE	PP1V25_S0_NB_DPLL	22 72
I500	TRUE	PP1V25_S0_NB_PEGPLL	19 21 72
I501	TRUE	PP1V25_S0_NB_PEGPLL_RC	21 72
I503	TRUE	PP1V25_S0_NB_VCCA_DPLLA	19 22 72
I502	TRUE	PP1V25_S0_NB_VCCA_DPLLB	19 22 72
I508	TRUE	PP1V5_S0	6 7 8 72
I506	TRUE	PP1V5_S0_NB_QDAC	22 72
I507	TRUE	PP1V5_S0_NB_VCCD_CRT	22 72
I505	TRUE	PP1V5_S0_NB_VCCD_QDAC	19 22 72
I504	TRUE	PP1V5_S0_SB_VCC1_5_B	23 24 26 27 72
I514	TRUE	PP1V5_S0_SB_VCCDMIPLL	26 27 72
I512	TRUE	PP1V5_S0_SB_VCCDMIPLL_F	27 72
I513	TRUE	PP1V5_S0_SB_VCCSATAPLL	26 27 72
I511	TRUE	PP1V8_S0	6 7 8 72
I510	TRUE	PP1V8_S0_ANALOG_SDVO_F	61 72
I509	TRUE	PP1V8_S0_ANALOG_TMDS_F	61 72
I515	TRUE	PP1V8_S0_NB_VCCTXLVDS	19 22 72
I516	TRUE	PP1V8_S0_PVCC1_TMDS_F	61 72
I534	TRUE	PP1V8_S0_PVCC2_TMDS_F	61 72
I532	TRUE	PP1V8_S0_TMDS_F	61 72
I533	TRUE	PP1V8_S3	6 7 8 72
I531	TRUE	PP1V8_S3M_NB_VCCSMCK	19 21 72
I530	TRUE	PP1V8_S3_NB_VCCSMCK_RC	21 72
I540	TRUE	PP3V3_A_S0	6 8
I538	TRUE	PP3V3_B_S0	6 8
I539	TRUE	PP3V3_LCDVDD_SW	60 72
I537	TRUE	PP3V3_LCDVDD_SW_F	7 60 72
I536	TRUE	PP3V3_S0_ANALOG_SDVO_F	61 72
I535	TRUE	PP3V3_S0_CK505_VDD48	72
I544	TRUE	PP3V3_S0_CK505_VDDA	72
I545	TRUE	PP3V3_S0_CK505_VDDA_R	72
I541	TRUE	PP3V3_S0_CK505_VDD_CPU_SRC	29 72
I543	TRUE	PP3V3_S0_CK505_VDD_PCI	72
I542	TRUE	PP3V3_S0_CK505_VDD_REF	72
I549	TRUE	PP3V3_S0_HDCP_F	62
I550	TRUE	PP3V3_S0_IMVP6_3V3	52 72
I546	TRUE	PP3V3_S0_LCD_F	7 60 72
I548	TRUE	PP3V3_S0_NBCORE_FOLLOW_R	21 72
I547	TRUE	PP3V3_S0_NB_CRTDAC_F	22 72
I574	TRUE	PP3V3_S0_NB_TVDAC	22 72
I575	TRUE	PP3V3_S0_NB_TVDAC_F	22 72
I576	TRUE	PP3V3_S0_NB_TVDAC_FOLLOW	22 72
I573	TRUE	PP3V3_S0_NB_VCCA_CRTDAC	19 22 72
I572	TRUE	PP3V3_S0_NB_VCCA_DAC_BG	19 22 72
I582	TRUE	PP3V3_S0_NB_VCCA_TVDACA	19 22 72
I583	TRUE	PP3V3_S0_NB_VCCA_TVDACB	19 22 72
I584	TRUE	PP3V3_S0_NB_VCCA_TVDACC	19 22 72
I589	TRUE	PP3V3_S0_SPVCC_TMDS_F	61 72
I586	TRUE	PP3V3_S3	6 7 8 72
I585	TRUE	PP3V3_S3_ALS_F	
I588	TRUE	PP3V3_S3_AP_AUX	7 36 72
I587	TRUE	PP3V3_S5_AVREF_SMC	41 42 72
I594	TRUE	PP3V3_S5_SMC_AVCC	41 72
I591	TRUE	PP3V42G3H_SW	57 72
I590	TRUE	PP3V42_G3H	6 7 8 72
I593	TRUE	PP3V42_G3H_IPD_F	7 40
I592	TRUE	PP3V42_G3H_SMCUSBMUX_R	39 72
I599	TRUE	PP5V_S0	6 7 8 72
I597	TRUE	PP5V_S0_DVIPORT	7 37 63 72
I596	TRUE	PP5V_S0_DVIPORT_D	63 72
I595	TRUE	PP5V_S0_IMVP6_VDD	52 72
I598	TRUE	PP5V_S0_KBDLED_F	7 40 72
I600	TRUE	PP5V_S0_SB_V5REF	26 27 72
I834	TRUE	PP5V_S0_TMDS_FUSE	63 72
I832	TRUE	PP5V_S3	6 7 8 72
I833	TRUE	PP5V_S3_CAMERA_F	7 60 72
I830	TRUE	PP5V_S3_TOPCASE_F	7 40
I831	TRUE	PP5V_S3_USB2_EXTA	39 72
I844	TRUE	PP5V_S3_USB2_EXTA_F	7 37 39 72
I842	TRUE	PP5V_S5	6 7 8 72
I843	TRUE	PP5V_S5_SB_V5REF_SUS	26 27 72
I840	TRUE	PPBUS_G3H	7 8 72
I841	TRUE	PPBUS_R_G3H	7 8 72
I847	TRUE	PPDCIN_G3H	7 8 72
I848	TRUE	PPDCIN_G3H_R	50 72
I846	TRUE	PPVBATT_G3H_R	50 72

I639	TRUE	PPVBAT_G3H_CHGR_OUT	59 72
I641	TRUE	PPVBAT_G3H_CHGR_REG	6 59 72
I640	TRUE	PPVBAT_G3H_CHRGR_REG_0	59 72
I642	TRUE	PPVBAT_G3H_CHRGR_REG_R	59 72
I644	TRUE	PPVCORE_S0_CPU	6 7 8 72
I643	TRUE	PPVCORE_S0_NB_GFX	6 7 8 72
I646	TRUE	PPVDCIN_G3H_PRE	45 59 72
I645	TRUE	PPVDCIN_G3H_PRE2	59 72
I647	TRUE	PPVDCIN_G3H_PRE_0	59 72
I649	TRUE	PPVDCIN_G3H_PRE_R	59 72
I648	TRUE	PPVIN_S5_IMVP6_VIN	52 72
I650	TRUE	PPVOUT_S0_LCDBKLT	7 60 64 72
I651	TRUE	PPVOUT_S0_LCDBKLT_SW	64 72
I652	TRUE	RSMRST_PWRGD	41 42 56
I654	TRUE	RSVD_EXTGPU_LVDS_EN	25
I653	TRUE	RUNSS_GATE_D	51
I656	TRUE	RUNSS_GATE_D_L	51
I655	TRUE	S0PWRGD_1V8_DIV	51
I657	TRUE	S0PWRGD_3V3_DIV	51
I665	TRUE	S0PWRGD_5V_DIV	51
I664	TRUE	S0SEQ_BEGIN	51
I667	TRUE	SATA_B_DET_L	25
I666	TRUE	SB_A20GATE	23
I668	TRUE	SB_CLINK_VREF0	25 70
I669	TRUE	SB_CLINK_VREF1	25 70
I677	TRUE	SB_CLK100M_DMI_N	24 30 71
I676	TRUE	SB_CLK100M_DMI_P	24 30 71
I679	TRUE	SB_CLK14P3M_TIMER	25 30 71
I678	TRUE	SB_CLK48M_USBCTLR	25 30 71
I680	TRUE	SB_CRT_TVOUT_MUX_L	25 63
I681	TRUE	SB_GPIO10_CL1	23 25
I687	TRUE	SB_GPIO18	25
I686	TRUE	SB_GPIO30	7 13 24
I685	TRUE	SB_GPIO36	25
I689	TRUE	SB_GPIO40	7 13 24

I620	TRUE	SB_INTVRMEN	23
I621	TRUE	SB_LAN100_SLP	23
I622	TRUE	SB_RCIN_L	23
I627	TRUE	SB_RTC_RST_L	23 28
I624	TRUE	SB_RTC_X1	23 28
I623	TRUE	SB_RTC_X1_R	28
I626	TRUE	SB_RTC_X2	23 28
I625	TRUE	SB_SLOAD	25
I632	TRUE	SB_SM_INTRUDER_L	23 28
I629	TRUE	SB_SPKR	25
I628	TRUE	SDVO_CTRLCLK	16 61
I631	TRUE	SDVO_CTRLDATA	16 61
I630	TRUE	SMBUS_SB_ME_SCL	44
I637	TRUE	SMBUS_SB_ME_SDA	44
I635	TRUE	SMBUS_SB_SCL	44
I634	TRUE	SMBUS_SB_SDA	44
I633	TRUE	SMBUS_SMC_0_S0_SCL	7 44 71
I636	TRUE	SMBUS_SMC_0_S0_SDA	7 44 71
I638	TRUE	SMBUS_SMC_A_S3_SCL	44 71
I658	TRUE	SMBUS_SMC_A_S3_SDA	44 71
I659	TRUE	SMBUS_SMC_BSA_SCL	7 44 71
I660	TRUE	SMBUS_SMC_BSA_SDA	7 44 71
I661	TRUE	SMBUS_SMC_B_S3_SCL	44
I662	TRUE	SMBUS_SMC_B_S3_SDA	44
I663	TRUE	SMBUS_SMC_MGMT_SCL	44 71
I670	TRUE	SMBUS_SMC_MGMT_SDA	44 71
I671	TRUE	SMB_AIRPORT_CONN_CLK	7 36
I672	TRUE	SMB_AIRPORT_CONN_DATA	7 36
I673	TRUE	SMC_ACIN_VSENSE	41 45
I674	TRUE	SMC_ADAPTER_EN	9 41 42
I675	TRUE	SMC_BATTPACK_STAT	41 42
I684	TRUE	SMC_BATT_CHG_EN	6 41 42
I683	TRUE	SMC_BATT_ISENSE	41 59
I682	TRUE	SMC_BC_ACOK	41 42 50 59
I688	TRUE	SMC_BC_ACOK_ONEWIRE_R	50

I726	TRUE	SMC_BS_ALRT_L	7 41 42 50
I725	TRUE	SMC_CASE_OPEN	41 42
I728	TRUE	SMC_DCIN_ISENSE	41 59
I727	TRUE	SMC_EXTAL	41 42
I729	TRUE	SMC_FAN_0_CTL	41 47
I731	TRUE	SMC_FAN_0_TACH	41 47
I730	TRUE	SMC_GPU_ISENSE	41 53
I732	TRUE	SMC_GPU_VSENSE	41 45
I734	TRUE	SMC_KBC_MDE	41
I733	TRUE	SMC_LID	7 40 41 42
I736	TRUE	SMC_LRESET_L	28 41
I735	TRUE	SMC_MANUAL_RST_L	6 42
I737	TRUE	SMC_MANUAL_RST_L1	42
I739	TRUE	SMC_MD1	41 43
I738	TRUE	SMC_NMI	41 43
I741	TRUE	SMC_ODD_DETECT	41 42
I740	TRUE	SMC_ONOFF_H	40 42 57
I742	TRUE	SMC_ONOFF_L	6 7 40 41 42
I744	TRUE	SMC_PBUS_ISENSE	41 59
I743	TRUE	SMC_PBUS_VSENSE	41 45
I746	TRUE	SMC_PF3	41 42
I745	TRUE	SMC_PM_G2_EN	6 41 58
I747	TRUE	SMC_PROCHOT	41 42
I749	TRUE	SMC_PROCHOT_3_3_L	41 42
I748	TRUE	SMC_RESET_L	6 41 42 43
I750	TRUE	SMC_RUNTIME_SCI_L	25 41
I751	TRUE	SMC_RX_L	39 41 42 43
I752	TRUE	SMC_SMS_INT	9 48
I754	TRUE	SMC_SUS_CLK	41 42
I753	TRUE	SMC_SYS_KBDLED	7 40 41
I755	TRUE	SMC_SYS_LED	7 40 41
I756	TRUE	SMC_TCK	6 41 42 43
I757	TRUE	SMC_TDI	6 41 42 43
I759	TRUE	SMC_TDO	6 41 42 43
I758	TRUE	SMC_THRMTRIP	41 42

I691	TRUE	SMC_TMS	42 6 41 43
I690	TRUE	SMC_TRST_L	
I692	TRUE	SMC_TX_L	42 39 41 43
I693	TRUE	SMC_VCL	41
I694	TRUE	SMC_WAKE_SCI_L	25 7 13
I695	TRUE	SMC_XTAL	41 42
I696	TRUE	SMS_MOT_EN	48
I697	TRUE	SMS_ONOFF_L	41 48
I698	TRUE	SMS_X_AXIS	41 48
I700	TRUE	SMS_Y_AXIS	41 48
I701	TRUE	SMS_Z_AXIS	41 48
I699	TRUE	SPI_A_INT_CLK	49
I702	TRUE	SPI_A_INT_HOLD_L	49
I703	TRUE	SPI_A_INT_SI	49
I704	TRUE	SPI_A_INT_WP_L	69 49
I705	TRUE	SPI_A_SCLK_R	43 6
I706	TRUE	SPI_A_SI_R	69 43 49
I707	TRUE	SPI_A_SO_R	
I711	TRUE	SPI_CE_L<0>	69 43 49
I710	TRUE	SPI_CE_R_L<0>	24 49 69
I709	TRUE	SPI_CE_R_L<1>	
I708	TRUE	SPI_EXT_A_SCLK_R	43
I712	TRUE	SPI_EXT_A_SI_R	43
I713	TRUE	SPI_EXT_CE_L<0>	43
I714	TRUE	SPI_INT_CE_L<0>	43 49
I715	TRUE	SPI_SCLK_R	24 49 69
I716	TRUE	SPI_SI_R	
I717	TRUE	SPI_SO	49 24 43 69
I718	TRUE	SST8051_DDC_CLK	
I719	TRUE	SST8051_DDC_DATA	62
I720	TRUE	SST8051_DDC_EN	62
I722	TRUE	SST8051_DVI_HOTPLUG_DET	62
I721	TRUE	SST8051_EA_L	62
I724	TRUE	SST8051_P25_AUDIO_CONFIG	62
I723	TRUE	SST8051_P34_AUDIO_CONFIG	62

I796	TRUE	SST8051_RST	62
I795	TRUE	SST8051_SW_RESET_L	25 62
I798	TRUE	SST8051_UPDATE_L	25 62
I797	TRUE	SST8051_XTAL1	62
I799	TRUE	SST8051_XTAL2	62
I801	TRUE	SUS_CLK_SB	25 42
I800	TRUE	SYS_ONEWIRE	7 41 42 50
I802	TRUE	SYS_ONEWIRE_BILAT	50
I804	TRUE	THRM_CPU_ALERT_L	46
I803	TRUE	THRM_CPU_DXN	46
I806	TRUE	THRM_CPU_DXP	46
I805	TRUE	THRM_CPU_THM_L	46
I807	TRUE	TMDS_DDC_SCL	7 37 61 62 63 67
I809	TRUE	TMDS_DDC_SDA	7 37 61 62 63 67
I808	TRUE	TMDS_EXT_RES	61
I811	TRUE	TMDS_EXT_SWING	61
I810	TRUE	TMDS_HTPLG	7 37 61 63
I812	TRUE	TMDS_HTPLG_R	61
I814	TRUE	TMDS_HW_RESET_L	28 61 62
I813	TRUE	TMDS_INT_N	61 67
I816	TRUE	TMDS_INT_P	61 67
I815	TRUE	TMDS_LINT_L	61 62
I817	TRUE	TMDS_LSCL	61 62
I819	TRUE	TMDS_LSDA	61 62
I818	TRUE	TMDS_SDB_N	61 67
I820	TRUE	TMDS_SDB_P	61 67
I821	TRUE	TMDS_SDC_N	61 67
I822	TRUE	TMDS_SDC_P	61 67
I824	TRUE	TMDS_SDG_N	61 67
I823	TRUE	TMDS_SDG_P	61 67
I825	TRUE	TMDS_SDR_N	61 67
I826	TRUE	TMDS_SDR_P	61 67
I827	TRUE	TMDS_SW_RESET_L	25 61
I829	TRUE	TMDS_TX<2..0>	61
I828	TRUE	TMDS_TX_CLK	61

I761	TRUE	TMDS_TX_CLK_N	
I760	TRUE	TMDS_TX_CLK_P	
I762	TRUE	TMDS_TX_CONN_CLK_N	
I763	TRUE	TMDS_TX_CONN_CLK_P	
I764	TRUE	TMDS_TX_CONN_N<2..0>	63 7 37
I765	TRUE	TMDS_TX_CONN_P<2..0>	63 7 37
I766	TRUE	TMDS_TX_N<2..0>	
I767	TRUE	TMDS_TX_P<2..0>	
I768	TRUE	TV_A_DAC	
I770	TRUE	TV_B_DAC	
I771	TRUE	TV_C_DAC	
I769	TRUE	TV_DCONSEL<1>	
I772	TRUE	USB2_AIRPORT_N	9
I773	TRUE	USB2_AIRPORT_N_F	
I774	TRUE	USB2_AIRPORT_P	9
I775	TRUE	USB2_AIRPORT_P_F	
I776	TRUE	USB2_CAMERA_F_N	
I777	TRUE	USB2_CAMERA_F_P	
I781	TRUE	USB2_CAMERA_N	9
I780	TRUE	USB2_CAMERA_P	9
I779	TRUE	USB2_EXTA_F_N	
I778	TRUE	USB2_EXTA_F_P	
I782	TRUE	USB2_EXTA_N	9
I783	TRUE	USB2_EXTA_P	9
I784	TRUE	USB2_MUXED_EXTA_N	
I785	TRUE	USB2_MUXED_EXTA_P	
I786	TRUE	USB2_WSPRING_N	9
I787	TRUE	USB2_WSPRING_P	9
I788	TRUE	USB_DEBUGPRT_EN_L	39 41
I789	TRUE	USB_EXTC_OC_L	24
I790	TRUE	USB_EXTD_OC_L	7 13 24
I792	TRUE	USB_IR_N	9 24 69
I791	TRUE	USB_IR_P	9 24 69
I794	TRUE	USB_RBIAS	24 69
I793	TRUE	VCCCL1_5V	26

I857	TRUE	VGA_B	67 63
I858	TRUE	VGA_G	7 37
I860	TRUE	VGA_HSYNC	67 63
I859	TRUE	VGA_R	37 7
I864	TRUE	VGA_VSYNC	63 7 37
I863	TRUE	VR_PWRGD_CK505	
I861	TRUE	VR_PWRGD_CK505_L	28 52
I862	TRUE	VR_PWRGOOD_DELAY	28 52 9 16
I866	TRUE	WOL_EN	25
I865	TRUE	WOW_EN	24 7 13
I867	TRUE	XDP_BPM_L<0>	36
I868	TRUE	XDP_BPM_L<1>	66 13 7 10
I869	TRUE	XDP_BPM_L<2>	66 13 10 7
I870	TRUE	XDP_BPM_L<3>	
I871	TRUE	XDP_BPM_L<4>	13 6 7
I872	TRUE	XDP_BPM_L<5>	66 10
I874	TRUE	XDP_CLK_N	30 7 71
I873	TRUE	XDP_CLK_P	13 66
I875	TRUE	XDP_CPURST_L	66 6 7 13
I876	TRUE	XDP_DBRESET_L	6 7 10 13 28
I877	TRUE	XDP_OBS20	7 13
I878	TRUE	XDP_PWRGD	6 7 13
I879	TRUE	XDP_TCK	6 7 10 13 66
I880	TRUE	XDP_TDI	6 7 10 13 66
I882	TRUE	XDP_TDO	6 7 10 13 66
I881	TRUE	XDP_TMS	6 7 10 13 66
I883	TRUE	XDP_TRST_L	6 7 10 13 66

ICT Test Points

APPLE INC.

SIZE D DRAWING NUMBER 051-7230 REV. J

SCALE NONE SHT 6 OF 109

Functional Test Points

NB NO_TESTS

These are normally testpoints but become NC

NO_TEST

TP210	TRUE	TP_LVDS_VBG		NC_LVDS_VBG
TP211	TRUE	TP_NB_RSVD<31>		NC_NB_RSVD_31
TP212	TRUE	TP_NB_RSVD<32>		NC_NB_RSVD_32
TP213	TRUE	TP_NB_RSVD<33>		NC_NB_RSVD_33
TP270	TRUE	TP_MEM_A_RCVEN_L		NC_MEM_A_RCVEN_L
TP271	TRUE	TP_MEM_B_RCVEN_L		NC_MEM_B_RCVEN_L
TP272	TRUE	TP_NB_RSVD<1>		NC_NB_RSVD_1
TP273	TRUE	TP_NB_RSVD<2>		NC_NB_RSVD_2
TP274	TRUE	TP_NB_RSVD<3>		NC_NB_RSVD_3
TP275	TRUE	TP_NB_RSVD<4>		NC_NB_RSVD_4
TP276	TRUE	TP_NB_RSVD<5>		NC_NB_RSVD_5
TP277	TRUE	TP_NB_RSVD<6>		NC_NB_RSVD_6
TP278	TRUE	TP_NB_RSVD<7>		NC_NB_RSVD_7
TP279	TRUE	TP_NB_RSVD<8>		NC_NB_RSVD_8
TP245	TRUE	TP_NB_RSVD<14>		NC_NB_RSVD_14
TP246	TRUE	TP_NB_RSVD<21>		NC_NB_RSVD_21
TP247	TRUE	TP_NB_RSVD<22>		NC_NB_RSVD_22
TP248	TRUE	TP_NB_RSVD<23>		NC_NB_RSVD_23
TP249	TRUE	TP_NB_RSVD<24>		NC_NB_RSVD_24
TP250	TRUE	TP_NB_RSVD<25>		NC_NB_RSVD_25
TP251	TRUE	TP_NB_RSVD<26>		NC_NB_RSVD_26
TP252	TRUE	TP_NB_RSVD<27>		NC_NB_RSVD_27
TP253	TRUE	TP_NB_RSVD<35>		NC_NB_RSVD_35
TP254	TRUE	TP_NB_RSVD<36>		NC_NB_RSVD_36
TP280	TRUE	TP_NB_CFG<10>		NC_NB_CFG_10
TP281	TRUE	TP_NB_CFG<11>		NC_NB_CFG_11
TP241	TRUE	TP_NB_CFG<14>		NC_NB_CFG_14
TP240	TRUE	TP_NB_CFG<15>		NC_NB_CFG_15
TP242	TRUE	TP_NB_CFG<17>		NC_NB_CFG_17
TP243	TRUE	TP_NB_NC<1>		NC_NB_NC_1
TP320	TRUE	TP_NB_NC<2>		NC_NB_NC_2
TP321	TRUE	TP_NB_NC<3>		NC_NB_NC_3
TP322	TRUE	TP_NB_NC<4>		NC_NB_NC_4
TP323	TRUE	TP_NB_NC<5>		NC_NB_NC_5
TP324	TRUE	TP_NB_NC<6>		NC_NB_NC_6
TP325	TRUE	TP_NB_NC<7>		NC_NB_NC_7
TP326	TRUE	TP_NB_NC<8>		NC_NB_NC_8
TP327	TRUE	TP_NB_NC<9>		NC_NB_NC_9
TP328	TRUE	TP_NB_NC<10>		NC_NB_NC_10
TP329	TRUE	TP_NB_NC<11>		NC_NB_NC_11
TP330	TRUE	TP_NB_NC<12>		NC_NB_NC_12
TP331	TRUE	TP_NB_NC<13>		NC_NB_NC_13
TP332	TRUE	TP_NB_NC<14>		NC_NB_NC_14
TP333	TRUE	TP_NB_RSVD<29>		NC_NB_RSVD_29
TP334	TRUE	TP_NB_RSVD<28>		NC_NB_RSVD_28
TP335	TRUE	TP_NB_RSVD<30>		NC_NB_RSVD_30

MAKE_BASE=TRUE

TP337	TRUE	CRT_DDC_CLK		NC_CRT_DDC_CLK
TP338	TRUE	CRT_DDC_DATA		NC_CRT_DDC_DATA

MAKE_BASE=TRUE

Power Supply NO_TESTs

NO_TEST

CLOCK NO_TESTS

NO_TEST

LVDS NO_TESTS

NO_TEST

REQUIRED NETS

FUNC TEST - BATTERY CONNECTOR

x3	E647	TRUE	BATT_POS	6 50
x3	E649	TRUE	GND	
	E638	TRUE	SMC_BS_ALRT_L	6 41 42 50
	E640	TRUE	SMBUS_SMC_BSA_SCL	6 44 71
	E639	TRUE	SMBUS_SMC_BSA_SDA	6 44 71

FUNC TEST - DC-IN CONNECTOR

x2	E648	TRUE	PP18V5_DCIN	6 50 72
	E650	TRUE	SYS_ONEWIRE	6 41 42 50
x2	E700	TRUE	GND	

FUNC TEST - TEMP SENSOR CONNECTOR

	E673	TRUE	SMBUS_SMC_0_S0_SCL	6 44 71
	E674	TRUE	SMBUS_SMC_0_S0_SDA	6 44 71
	E675	TRUE	=PP3V3_S0_THRM_SNR	8 46

FUNC TEST - FAN CONNECTOR

	E668	TRUE	=PP5V_S0_FAN	8 47
	E667	TRUE	FAN_RT_PWM	6 47
	E669	TRUE	FAN_RT_TACH	6 47
	E714	TRUE	GND	

FUNC TEST - CAMERA USB, LVDS, ALS

x2	E654	TRUE	PP5V_S3_CAMERA_F	6 60 72
	E655	TRUE	USB2_CAMERA_F_P	6 60 69
	E656	TRUE	USB2_CAMERA_F_N	6 60 69
	E657	TRUE	LCDBKLT_RTN<1..6>	6 60 64
	E658	TRUE	LVDS_A_DATA_N<0..2>	6 15 60 67
	E659	TRUE	LVDS_A_DATA_P<0..2>	6 15 60 67
	E660	TRUE	PPVOUT_S0_LCDBKLT	6 60 64 72
	E663	TRUE	LVDS_A_CLK_F_N	6 60
	E662	TRUE	LVDS_A_CLK_F_P	6 60
	E665	TRUE	LVDS_DDC_CLK	6 15 60
	E664	TRUE	LVDS_DDC_DATA	6 15 60
	E666	TRUE	PP3V3_S0_LCD_F	6 60 72
x2	E661	TRUE	PP3V3_LCDVDD_SW_F	6 60 72
	E711	TRUE	=I2C_TOP_ALS_SDA	44 60
	E712	TRUE	=I2C_TOP_ALS_SCL	44 60
x10	E715	TRUE	GND	

FUNC TEST - AUDIO CONNECTOR

	E645	TRUE	HDA_SYNC	6 9 23 37 69
	E644	TRUE	HDA_BITCLK	9 37
	E735	TRUE	AUD_MIC_DATA	6 37 60
	E736	TRUE	HDA_SDATAOUT	9 37
	E737	TRUE	=PPVIN_S0_AUDIO	8 37
	E731	TRUE	HDA_SDATAIN0	9 37
	E740	TRUE	AUD_MIC_CLK	6 37 60
	E739	TRUE	PM_SLP_S3_L	6 25 36 37 41 42 51 55

FUNC TEST - IPD CONNECTOR

	E507	TRUE	SMC_LID	6 40 41 42
x14	E508	TRUE	PP3V42_G3H_IPD_F	6 40
	E503	TRUE	SMC_SYS_KBDLED	6 40 41
	E505	TRUE	SMC_SYS_LED	6 40 41
	E510	TRUE	=USB2_TRACKPAD_N	9 40
	E512	TRUE	=USB2_TRACKPAD_P	9 40
	E511	TRUE	SMC_ONOFF_L	6 7 40 41 42
	E513	TRUE	=USB2_IR_N	7 9 40
	E514	TRUE	=USB2_IR_P	7 9 40
	E515	TRUE	PP5V_S0_KBDLED_F	6 7 40 72
	E517	TRUE	PP5V_S3_TOPCASE_F	6 40
	E516	TRUE	=SMB_TOPCASE_SCL	40 44
	E518	TRUE	=SMB_TOPCASE_SDA	40 44
	E520	TRUE	SMC_ONOFF_L	6 7 40 41 42
	E519	TRUE	=USB2_IR_N	7 9 40
	E521	TRUE	=USB2_IR_P	7 9 40
	E670	TRUE	PP5V_S0_KBDLED_F	6 7 40 72
	E716	TRUE	LSOC_H_R	6

FUNC TEST - XDP/ITP CONNECTOR

	E695	TRUE	XDP_BPM_L<0..5>	6 10 13 66
	E695	TRUE	NB_BSEL<0..2>	6 13 30 66
	E680	TRUE	NB_CFG<3..8>	6 13 16
	E681	TRUE	XDP_PWRGD	6 13
	E685	TRUE	XDP_OBS20	6 13
	E682	TRUE	TP_XDP_HOOK2	13
	E684	TRUE	TP_XDP_HOOK3	13
	E685	TRUE	LOCAL_CTRL_DATA	6 13 15
	E687	TRUE	LOCAL_CTRL_CLK	6 13 15
	E688	TRUE	XDP_TCK	6 10 13 66
	E688	TRUE	SMC_WAKE_SCI_L	6 13 25 41
	E689	TRUE	USB_EXTA_OC_L	6 13 24
	E691	TRUE	SB_GPIO40	6 13 24
	E690	TRUE	USB_EXTD_OC_L	6 13 24
	E692	TRUE	WOW_EN	6 13 24 36
	E693	TRUE	PM_LATRIGGER_L	6 13 24
	E694	TRUE	EXTGPU_LVDS_EN	6 13 24
	E696	TRUE	SB_GPIO30	6 13 24
	E697	TRUE	USB_EXTB_OC_L	6 13 24
	E698	TRUE	XDP_CLK_P	6 13 30 66 71
	E699	TRUE	XDP_CLK_N	6 13 30 66 71
	E701	TRUE	XDP_CPURST_L	6 13 66
	E706	TRUE	XDP_DBRESET_L	6 10 13 28
	E702	TRUE	XDP_TDO	6 10 13 66
	E703	TRUE	XDP_TRST_L	6 10 13 66
	E704	TRUE	XDP_TDI	6 10 13 66
	E705	TRUE	XDP_TMS	6 10 13 66
	E707	TRUE	=PP3V3_S0_XDP	8 13
	E708	TRUE	=PP1V05_S0_XDP	8 13
x16	E709	TRUE	GND	

FUNC TEST - RIO HATCH CONNECTOR

	E716	TRUE	HDMI_HOST	6 37 63
	E717	TRUE	DVI_HOST	6 37 63
	E718	TRUE	TMDS_HTPLG	6 37 61 63
	E719	TRUE	TMDS_DDC_SDA	6 37 61 62 63 67
	E720	TRUE	TMDS_DDC_SCL	6 37 61 62 63 67
	E721	TRUE	VGA_VSYNC	6 37 63
	E722	TRUE	VGA_HSYNC	6 37 63
	E723	TRUE	TMDS_TX_CONN_CLK_P	6 37 63 67
	E724	TRUE	TMDS_TX_CONN_CLK_N	6 37 63 67
	E725	TRUE	TMDS_TX_CONN_P<0..2>	6 37 63
	E726	TRUE	TMDS_TX_CONN_N<0..2>	6 37 63
	E727	TRUE	USB2_EXTA_F_P	6 37 39 69
	E728	TRUE	USB2_EXTA_F_N	6 37 39 69
	E729	TRUE	PP5V_S3_USB2_EXTA_F	6 37 39 72
	E730	TRUE	PP5V_S0_DVIPORT	6 37 63 72
	E731	TRUE	VGA_B	6 37 63 67
	E732	TRUE	VGA_G	6 37 63 67
	E733	TRUE	VGA_R	6 37 63 67
x14	E710	TRUE	GND	

FUNC TEST - AIRPORT

	E741	TRUE	CK505_SRC_CLKREQ6_L	6 7 29 36
	E742	TRUE	PCIE_WAKE_L	6 7 25 36
	E743	TRUE	AIRPORT_RST_L	6 7 28 36
	E744	TRUE	=SMB_AIRPORT_CLK	36 44
	E745	TRUE	=SMB_AIRPORT_DATA	36 44
	E746	TRUE	GND	

NICE2HAVE NETS

FUNC TEST - Power Supplies

	E92	PPVCORE_S0_CPU	6 8 72
	E454	PP0V9_S0	6 8 72
	E455	PP1V05_S0	6 8 72
	E457	PP1V25_S0	6 8 72
	E460	PP1V5_S0	6 8 72
	E459	PP1V8_S0	6 8 72
	E458	PPVCORE_S0_NB_GFX	6 8 72
	E461	PP5V_S0	6 8 72
	E466	PP3V3_S0	72
	E465	PP1V8_S3	6 8 72
	E463	PP3V3_S3	6 8 72
	E462	PP5V_S3	6 8 72
	E467	PP3V3_S5	6 8 72
	E468	PP5V_S5	6 8 72
	E469	PP3V42_G3H	6 8 72
	E472	PP18V5_G3H	6 8 72
	E473	PPDCIN_G3H	6 8 72
	E472	PPBUS_G3H	6 8 72
	E471	PPBUS_R_G3H	6 8 72

FUNC TEST - M93 WIRELESS CONNECTOR

	E478	PLT_RST_L	6 24 28
	E475	PCIE_WAKE_L	6 7 25 36
	E479	CK505_SRC_CLKREQ6_L	6 7 29 36
	E478	PCIE_CLK100M_MINI_N_F	6 36
	E476	PCIE_CLK100M_MINI_P_F	6 36
	E477	PCIE_E_D2R_N_F	6 36
	E480	PCIE_E_D2R_P_F	6 36
	E483	PCIE_E_R2D_C_N_F	6 7 36
	E484	PCIE_E_R2D_C_P_F	6 7 36
	E482	AIRPORT_RST_L	6 7 28 36
	E499	SMB_AIRPORT_CONN_CLK	6 36
	E500	SMB_AIRPORT_CONN_DATA	6 36
	E501	PCIE_E_R2D_C_N_F	6 7 36
	E502	PCIE_E_R2D_C_P_F	6 7 36
	E503	PP3V3_S3_AP_AUX	6 36 72

x13	E522	GND	

Functional Test and No-Tests

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J

SCALE	SHT	OF
NONE	7	109

"S0,S0M" RAILS

(REGULATOR OUTPUT CPU VCORE PWR)

52 =PPVCORE_S0_CPU_REG — PPVCORE_S0_CPU — 6 7 72
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=0.9V
MAKE_BASE=TRUE

(CPU VCOR PWRE)

=PPVCORE_S0_CPU — 11 12 65

55 =PP0V9_S0_REG — PP0V9_S0 — 6 7 72
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE

(DDR2 TERMINATION 0.9V PWR)

=PP0V9_S3M_MEM_TERM — 33

(REGULATOR OUTPUT CPU 0.90V PWR)

55 =PP0V9_S3_VTTREF — PP0V9_S3 — 6 72
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE

(NB MEM VREF 0.9V PWR)

=PP0V9_S3M_MEM_NBVREFA — 31 32
=PP0V9_S3M_MEM_NBVREFB
=PP0V9_S3_MEM_VREF

R0800 0 5% 1/20W MF 201
2 — 1 — PP0V9_S3M_MEM_NBVREFA — 16 21 68
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V

R0801 0 5% 1/20W MF 201
2 — 1 — PP0V9_S3M_MEM_NBVREFB — 16 21 68
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V

54 =PP1V05_S0_REG — PP1V05_S0 — 6 7 72
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE

=PP1V05_S0_SB_CPU_IO — 23 26 27
=PPVCORE_S0_SB — 26 27
=PP1V05_S0_CPU — 10 11 12
=PP1V05_S0_NB_PCIE — 21
=PPVCORE_S0_NB — 18 21
=PP1V25R1V05_S0_FSB_NB — 14 30
=PP1V25R1V05_S0_NB_VTT — 19 21
=PP1V05_S0M_NB_VCCAXM — 18 21
=PP1V05_S0_XDP — 7 13
=PP1V05_S0_SMC_LS — 42

57 =PP1V25_S0_REG — PP1V25_S0 — 6 7 72
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE

=PP1V25_S0_NB_PLL — 21
=PP1V25_S0_NB_VCCDMI — 19 21
=PP1V25_S0_SB_DMI — 26 27
=PP1V25_S0_NB_VCCAXF — 21
=PP1V25_S0_NB_VCCA — 21
=PP1V25_S0_FET — 51

54 =PP1V5_S0_REG — PP1V5_S0 — 6 7 72
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE

=PP1V5_S0_CPU — 11 12
=PP1V5_S0_NB_TVDAC — 22
=PP1V5_S0_SB — 27
=PP1V5_S0_SB_VCC1_5_A_ARX — 26 27
=PP1V5_S0_SB_VCC1_5_A_ATX — 26 27
=PP1V5_S0_SB_VCC1_5_A — 26 27
=PP1V5_S0_SB_VCCUSBPLL — 26 27
=PP1V5_S0_SB_VCC1_5_A_USB_CORE — 26 27
=PP1V5_S0_NB_FOLLOW — 22

51 =PP1V8_S0_FET — PP1V8_S0 — 6 7 72
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE

=PP1V8_S0_NB_LVDS — 22
=PP1V8_S0_NB_DPLL — 22
=PP1V8_S0_TMDS — 61

53 45 =PPVCORE_S0_NB_GFX_IMVP — PPVCORE_S0_NB_GFX — 6 7 72
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE

=PPVCORE_S0_NB_GFX — 18 22 53 65

51 =PP5V_S0_FET — PP5V_S0 — 6 7 72
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=5V
MAKE_BASE=TRUE

=PP5V_S0_SB — 27
=PP5V_S0_LPCPLUS — 43
=PP5V_S0_FAN — 7 47
=PP5V_S0_CPU_IMVP — 52
=PP5V_S0_NB_GFX_IMVP — 53
=PP5V_S0_TMDS — 63
=PP5V_S0_NB_TVDAC — 22
=PP5V_S0_KBDLED — 40

51 =PP3V3_A_S0_FET — PP3V3_A_S0 — 6
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

=PP3V3_S0_NB_VCCHV — 16 19 21 22
=PP3V3_S0_NB_FOLLOW — 21
=PP3V3_S0_SB_GPIO — 23 25
=PP3V3_S0_SB_VCCGLAN3_3 — 26
=PP3V3_S0_SB_VCC3_3_PCI — 26 27
=PP3V3_S0_SB_VCC3_3_IDE — 26 27
=PP3V3_S0_SB_VCC3_3_VCCPCORE — 26
=PP3V3_S0_SB_VCC3_3_SATA — 26 27
=PP3V3_S0_SB_VCC3_3_DMI — 26 27
=PP3V3_S0_SB — 27
=PP3V3_S0_SB_PM — 28
=PP3V3_S0_RSTBUF — 28
=PP3V3_S0_LCDBKLT — 64
=PP3V3_S0_SMBUS_SB — 44
=PP3V3_S0_SMBUS_SMC_0_S0 — 44
=PP3V3_S0_THRM_SNR — 7 46
=PP3V3_S0_XDP — 7 13
=PP3V3_S0_SMC_LS — 42
=PP3V3_S0_IMVP — 52
=PP3V3_S0_NB_GFX_IMVP — 53
=PP3V3_S0_PDCISENS — 53
=PP3V3_S0MWOL_SB_VCCCL3_3 — 26
=PP3V3_S0_LCD — 60
=PP3V3_S0_NB — 63
=PP3V3R1V5_S0_SB_VCCHDA — 26 27
=PP3V3_S0_SB_PCI — 24
=PP3V3_S0_NB_VCCA_PEG_BG — 19 21
=PP3V3_S0MWOL_SB_VCCLAN3_3 — 26 27
=PP3V3_S0MWOL_SB_CLINK0 — 25
=PP3V3_S0_CK505 — 29 30
=PP3V3_S0_NB_VCCSYNC — 19 22

3V3_S0 split into 2
for layout optimization
of plane splits

51 =PP3V3_B_S0_FET — PP3V3_B_S0 — 6
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

3V3_B_S0 plane on right side
(peninsula)

=PP3V3_S0_TMDS — 61 63
=PP3V3_S0_PATA — 38
=PP3V3_S0_FAN — 47
=PP3V3_S0_IDE_RESET — 38
=PP3V3_S0_HDCP — 62

"S3" RAILS

55 =PP1V8_S3_REG — PP1V8_S3 — 6 7 72
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE

=PP1V8_S3_FET — 51
=PP1V8_S3_MEM — 31 32 34 35
=PP1V8_S3M_MEM_NB — 16 18 21 68
=PP1V8_S3_NB_VCC — 21

58 =PP3V3_S3_FET — PP3V3_S3 — 6 7 72
MIN_LINE_WIDTH=0.2mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=3.3V
MAKE_BASE=TRUE

=PP3V3_S3_BT — 36
=PP3V3_S3_SMS — 48
=PP3V3_S3_SMBUS_SMC_A_S3 — 44
=PP3V3_S3_PDCISENS — 51
=PP3V3_S3_SMBUS_SMC_MGMT — 44
=PP3V3_S3_SMBUS_SMC_B_S3 — 44
=PP3V3_S3_MIC — 60
=PP3V3_S3_SMC — 42

58 =PP5V_S3_FET — PP5V_S3 — 6 7 72
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE

=PP5V_S3_CAMERA — 60
=PP5V_S3_TOPCASE — 40

"S5" RAILS

56 =PP3V3_S5_REG — PP3V3_S5 — 6 7 72
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE

=PP3V3_S5_SB_PM — 28
=PP3V3_S5_SB_USB — 24
=PP3V3_S5_SB_GPIO — 25
=PP3V3_S5_SB — 25 27
=PP3V3_S5_FET — 51 58
=PP3V3_S5_SB_VCCSUS3_3_USB — 26 27
=PP3V3_S5_SB_VCCSUS3_3 — 26 27
=PP3V3_S5_SB_3V3_VCCSUSHDA — 26 27
=PP3V3_S5_AIRPORT_AUX — 36
=PP3V3_S5_SMBUS_SB_ME — 44
=PP3V3_S5_ROM — 43 49
=PP3V3_S5_LCD — 60
=PP3V3_S5_SB_CLINK1 — 25
=PP3V3_S5_P1V25S0 — 57

56 =PP5V_S5_REG — PP5V_S5 — 6 7 72
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE

=PP5V_S5_SB — 27
=PP5V_S5_USB — 39
=PP5V_S5_1V51V05S0 — 54
=PP5V_S5_1V8S30V9S0 — 55
=PP5V_S5_PWRCTL — 58
=PP5V_S5_FET — 51 58

"G3H" RAILS

57 =PP3V42_G3H_REG — PP3V42_G3H — 6 7 72
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.42V
MAKE_BASE=TRUE

=PP3V42_G3H_SMC — 41 42
=PP3V42_G3H_SMCVREF — 42
=PP3V42_G3H_SMBUS_SMC_BSA — 44
=PP3V42_G3H_IPD — 40
=PP3V42_G3H_SB_RTC — 28
=PP3V42_G3H_SMCUSBMUX — 39
=PP3V42_G3H_CHGR — 59
=PP3V42_G3H_LPCPLUS — 43

59 50 =PP18V5_G3H_CHGR — PP18V5_G3H — 6 7 72
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE

50 =PPDCIN_G3H — PPDCIN_G3H — 6 7 72
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V
MAKE_BASE=TRUE

=PPVIN_G3H_P3V42G3H — 57

59 42 =PPBUSA_G3H — PPBUS_R_G3H — 6 7 72
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V
MAKE_BASE=TRUE

=PPVIN_S5_CPU_IMVP — 52
=PPVIN_S5_NB_GFX_IMVP — 53
=PPVIN_S5_1V8S30V9S0 — 55
=PPVIN_S5_1V5S0 — 54
=PPVIN_S5_1V05S0 — 54

59 45 =PPBUSB_G3H — PPBUS_G3H — 6 7 72
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V
MAKE_BASE=TRUE

=PPVIN_S5_5VS5 — 56
=PPVIN_S5_3V3S5 — 56
=PPVIN_S0_LCDBKLT — 64
=PPVIN_S0_AUDIO — 7 37
=PPVIN_G3H_DCIN — 50

Power Aliases

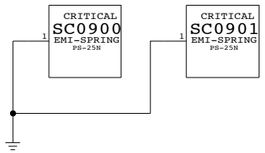
SYNC_MASTER=WFERRY SYNC_DATE=06/15/2006

APPLE INC.

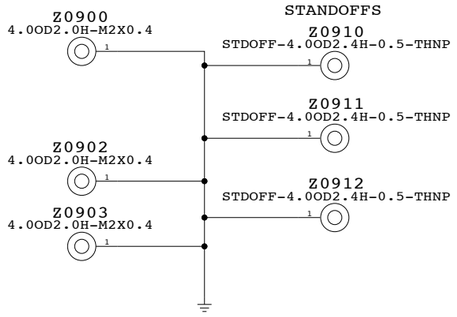
SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 8 OF 109	

EMI SPRING CLIPS

PLACE CLIPS PER MCO ON TOPSIDE NEAR BATTERY CONNECTOR J6900



BOSSES TO CONNECT TO HEATSINK



SMC ALIASES

NO-CONNECT UNUSED SMC INTERFACE PORTS

			NO_TEST
41	SMC_PA0	NC_SMC_PA0	TRUE
41	SMC_PA1	NC_SMC_PA1	TRUE
41	SMC_PB0	NC_SMC_PB0	TRUE
41	SMC_PG0	NC_SMC_PG0	TRUE
41	SMC_P14	NC_SMC_P14	TRUE
41	SMC_P20	NC_SMC_P20	TRUE
41	SMC_P21	NC_SMC_P21	TRUE
41	SMC_P22	NC_SMC_P22	TRUE
41	SMC_P23	NC_SMC_P23	TRUE
41	SMC_P26	NC_SMC_P26	TRUE
41	SMC_P27	NC_SMC_P27	TRUE
41	SMC_P41	NC_SMC_P41	TRUE
41	SMC_P43	NC_SMC_P43	TRUE
41	SMC_P44	NC_SMC_P44	TRUE
41	SMC_P46	NC_SMC_P46	TRUE
41	SMC_P62	NC_SMC_P62	TRUE
41	SMC_P63	NC_SMC_P63	TRUE
41	SMC_P64	NC_SMC_P64	TRUE
41	SMC_P67	NC_SMC_P67	TRUE
41	SMC_P81	NC_SMC_P81	TRUE
41	SMC_GFX_OVERTEMP_L	NC_SMC_GFX_OVERTEMP_L	TRUE
41	SMC_EXCARD_OC_L	NC_EXCARD_OC_L	TRUE
41	SMC_BATT_TRICKLE_EN_L	NC_SMC_BATT_TRICKLE_EN_L	TRUE
41	SMC_EXCARD_CP	NC_SMC_EXCARD_CP	TRUE
41	SMC_P45	NC_SMC_ENRGYSTR_LDO_EN	TRUE
41	SMC_PH4	NC_SMC_ENRGYSTR_LDO_PGOOD	TRUE
41	ALS_RIGHT	NC_ALS_RIGHT	TRUE
41	ALS_GAIN	NC_ALS_GAIN	TRUE
41	SMC_EXCARD_PWR_EN	NC_SMC_EXCARD_PWR_EN	TRUE
41	SMC_FAN_1_CTL	NC_SMC_FAN_1_CTL	TRUE
41	SMC_FAN_2_CTL	NC_SMC_FAN_2_CTL	TRUE
41	SMC_FAN_3_CTL	NC_SMC_FAN_3_CTL	TRUE
41	SMC_FAN_1_TACH	NC_SMC_FAN_1_TACH	TRUE
41	SMC_FAN_2_TACH	NC_SMC_FAN_2_TACH	TRUE
41	SMC_FAN_3_TACH	NC_SMC_FAN_3_TACH	TRUE
41	SMC_PF0	NC_SMC_PF0	TRUE
41	SMC_BATT_VSET	NC_SMC_BATT_VSET	TRUE
41	SMC_SYS_VSET	NC_SMC_SYS_VSET	TRUE
41	SMC_RSTGATE_L	NC_SMC_RSTGATE_L	TRUE
41	SMC_GFX_THROTTLE_L	NC_SMC_GFX_THROTTLE_L	TRUE
41	SMC_SYS_ISET	NC_SYS_ISET	TRUE
41	SMC_BATT_ISET	NC_BATT_ISET	TRUE
41	ISENSE_CAL_EN	NC_ISENSE_CAL_EN	TRUE
41	SMC_FWE	NC_SMC_FWE	TRUE
41	SMC_ANALOG_ID	NC_SMC_ANALOG_ID	TRUE
41	SMC_TEST_DAC1	NC_SMC_TEST_DAC1	TRUE
41	SMC_TEST_DAC2	NC_SMC_TEST_DAC2	TRUE
41	SMC_TEST_DAC3	NC_SMC_TEST_DAC3	TRUE

48 6 SMC_SMS_INT — =SMC_SMS_INT — 41

42 41 6 SMC_ADAPTER_EN — SMC_ADAPTER_PRESENT — 36

GND

VOLTAGE=0V
MIN_NECK_WIDTH=0.20 MM
MIN_LINE_WIDTH=0.30 MM

LVDS ALIASES

NO-CONNECT UNUSED LVDS INTERFACE PORTS

			NO_TEST
67 15	LVDS_B_CLK_N	NC_LVDS_B_CLK_N	TRUE
67 15	LVDS_B_CLK_P	NC_LVDS_B_CLK_P	TRUE
67 15	LVDS_B_DATA_N<0>	NC_LVDS_B_DATA_N0	TRUE
67 15	LVDS_B_DATA_N<1>	NC_LVDS_B_DATA_N1	TRUE
67 15	LVDS_B_DATA_N<2>	NC_LVDS_B_DATA_N2	TRUE
67	LVDS_B_DATA_N<3>	NC_LVDS_B_DATA_N3	TRUE
67 15	LVDS_B_DATA_P<0>	NC_LVDS_B_DATA_P0	TRUE
67 15	LVDS_B_DATA_P<1>	NC_LVDS_B_DATA_P1	TRUE
67 15	LVDS_B_DATA_P<2>	NC_LVDS_B_DATA_P2	TRUE
67	LVDS_B_DATA_P<3>	NC_LVDS_B_DATA_P3	TRUE
67	LVDS_A_DATA_P<3>	NC_LVDS_A_DATA_P3	TRUE
67	LVDS_A_DATA_N<3>	NC_LVDS_A_DATA_N3	TRUE

PCI_EXPRESS GRAPHICS ALIASES

NO-CONNECT UNUSED SDVO INTERFACE PORTS

67 15	PEG_D2R_N<0>	NC_PEG_D2R_N0
67 15	PEG_D2R_N<2>	NC_PEG_D2R_N2
67 15	PEG_D2R_N<3>	NC_PEG_D2R_N3
67 15	PEG_D2R_N<4>	NC_PEG_D2R_N4
67 15	PEG_D2R_N<5>	NC_PEG_D2R_N5
67 15	PEG_D2R_N<6>	NC_PEG_D2R_N6
67 15	PEG_D2R_N<7>	NC_PEG_D2R_N7
67 15	PEG_D2R_N<8>	NC_PEG_D2R_N8
67 15	PEG_D2R_N<9>	NC_PEG_D2R_N9
67 15	PEG_D2R_N<10>	NC_PEG_D2R_N10
67 15	PEG_D2R_N<11>	NC_PEG_D2R_N11
67 15	PEG_D2R_N<12>	NC_PEG_D2R_N12
67 15	PEG_D2R_N<13>	NC_PEG_D2R_N13
67 15	PEG_D2R_N<14>	NC_PEG_D2R_N14
67 15	PEG_D2R_N<15>	NC_PEG_D2R_N15
67 15	PEG_D2R_P<0>	NC_PEG_D2R_P0
67 15	PEG_D2R_P<2>	NC_PEG_D2R_P2
67 15	PEG_D2R_P<3>	NC_PEG_D2R_P3
67 15	PEG_D2R_P<4>	NC_PEG_D2R_P4
67 15	PEG_D2R_P<5>	NC_PEG_D2R_P5
67 15	PEG_D2R_P<6>	NC_PEG_D2R_P6
67 15	PEG_D2R_P<7>	NC_PEG_D2R_P7
67 15	PEG_D2R_P<8>	NC_PEG_D2R_P8
67 15	PEG_D2R_P<9>	NC_PEG_D2R_P9
67 15	PEG_D2R_P<10>	NC_PEG_D2R_P10
67 15	PEG_D2R_P<11>	NC_PEG_D2R_P11
67 15	PEG_D2R_P<12>	NC_PEG_D2R_P12
67 15	PEG_D2R_P<13>	NC_PEG_D2R_P13
67 15	PEG_D2R_P<14>	NC_PEG_D2R_P14
67 15	PEG_D2R_P<15>	NC_PEG_D2R_P15
67 15	PEG_R2D_C_N<4>	NC_PEG_R2D_C_N4
67 15	PEG_R2D_C_N<5>	NC_PEG_R2D_C_N5
67 15	PEG_R2D_C_N<6>	NC_PEG_R2D_C_N6
67 15	PEG_R2D_C_N<7>	NC_PEG_R2D_C_N7
67 15	PEG_R2D_C_N<8>	NC_PEG_R2D_C_N8
67 15	PEG_R2D_C_N<9>	NC_PEG_R2D_C_N9
67 15	PEG_R2D_C_N<10>	NC_PEG_R2D_C_N10
67 15	PEG_R2D_C_N<11>	NC_PEG_R2D_C_N11
67 15	PEG_R2D_C_N<12>	NC_PEG_R2D_C_N12
67 15	PEG_R2D_C_N<13>	NC_PEG_R2D_C_N13
67 15	PEG_R2D_C_N<14>	NC_PEG_R2D_C_N14
67 15	PEG_R2D_C_N<15>	NC_PEG_R2D_C_N15
67 15	PEG_R2D_C_P<4>	NC_PEG_R2D_C_P4
67 15	PEG_R2D_C_P<5>	NC_PEG_R2D_C_P5
67 15	PEG_R2D_C_P<6>	NC_PEG_R2D_C_P6
67 15	PEG_R2D_C_P<7>	NC_PEG_R2D_C_P7
67 15	PEG_R2D_C_P<8>	NC_PEG_R2D_C_P8
67 15	PEG_R2D_C_P<9>	NC_PEG_R2D_C_P9
67 15	PEG_R2D_C_P<10>	NC_PEG_R2D_C_P10
67 15	PEG_R2D_C_P<11>	NC_PEG_R2D_C_P11
67 15	PEG_R2D_C_P<12>	NC_PEG_R2D_C_P12
67 15	PEG_R2D_C_P<13>	NC_PEG_R2D_C_P13
67 15	PEG_R2D_C_P<14>	NC_PEG_R2D_C_P14
67 15	PEG_R2D_C_P<15>	NC_PEG_R2D_C_P15

SATA ALIASES

NO-CONNECT UNUSED SATA INTERFACE PORTS

69	SATA_A_D2R_N	NC_SATA_A_D2R_N
69	SATA_A_D2R_P	NC_SATA_A_D2R_P
69 23	SATA_A_R2D_C_N	NC_SATA_A_R2D_C_N
69 23	SATA_A_R2D_C_P	NC_SATA_A_R2D_C_P
69	SATA_B_D2R_N	NC_SATA_B_D2R_N
69	SATA_B_D2R_P	NC_SATA_B_D2R_P
69 23	SATA_B_R2D_C_N	NC_SATA_B_R2D_C_N
69 23	SATA_B_R2D_C_P	NC_SATA_B_R2D_C_P
69	SATA_C_D2R_N	NC_SATA_C_D2R_N
69	SATA_C_D2R_P	NC_SATA_C_D2R_P
69 23	SATA_C_R2D_C_N	NC_SATA_C_R2D_C_N
69 23	SATA_C_R2D_C_P	NC_SATA_C_R2D_C_P

CLOCK ALIASES

NO-CONNECT UNUSED CLOCK INTERFACE PORTS

29	TP_CK505_SRC1_N	NC_CK505_SRC1_N
29	TP_CK505_SRC1_P	NC_CK505_SRC1_P
29	TP_CK505_SRC_CLKREQ1_L	NC_CK505_SRC_CLKREQ1_L
29	TP_CK505_SRC3_N	NC_CK505_SRC3_N
29	TP_CK505_SRC3_P	NC_CK505_SRC3_P
29	TP_CK505_SRC_CLKREQ3_L	NC_CK505_SRC_CLKREQ3_L
29	TP_CK505_SRC4_N	NC_CK505_SRC4_N
29	TP_CK505_SRC4_P	NC_CK505_SRC4_P
29	TP_CK505_SRC_CLKREQ4_L	NC_CK505_SRC_CLKREQ4_L
29	TP_CK505_SRC7_N	NC_CK505_SRC7_N
29	TP_CK505_SRC7_P	NC_CK505_SRC7_P
29	TP_CK505_PGMODE	NC_CK505_PGMODE
29	TP_CK505_SRC8_N	NC_CK505_SRC8_N
29	TP_CK505_SRC8_P	NC_CK505_SRC8_P
29	TP_CK505_SRC_CLKREQ8_L	NC_CK505_SRC_CLKREQ8_L
29	TP_GPU_STOP_L	NC_GPU_STOP_L
29	TP_CK505_PCI1_CLK	NC_CK505_PCI1_CLK
29	TP_CK505_PCI2_CLK	NC_CK505_PCI2_CLK
29	TP_CK505_PCI4_CLK	NC_CK505_PCI4_CLK

SB ALIASES

NO-CONNECT UNUSED INTERFACE PORTS

25	VR_PWRGD_CLKEN	VR_PWRGD_CK505 — 6 28
25	=SB_CLINK_MPWROK	PM_SB_PWROK — 6 25 28
70 24	PCI_AD<0..31>	NC_PCI_AD<0..31> TRUE
70 24	PCI_C_BE_L<0..3>	NC_PCI_C_BE_L<0..3> TRUE
70 24	PCI_PAR	NC_PCI_PAR TRUE
24	PCI_RST_L	TP_PCI_RST_L — 6

NB ALIASES

16	=GFX_VR_EN	GFX_VR_EN — 6 53
16	=NB_CLINK_MPWROK	VR_PWRGOOD_DELAY — 4 16 28 52
16	=NB_CLK96M_DOT_P	NB_CLK96M_DOT_P — 6 30 71
16	=NB_CLK96M_DOT_N	NB_CLK96M_DOT_N — 6 30 71
16	=NB_CLK100M_DPLLSS_P	NB_CLK100M_DPLLSS_P — 6 30 71
16	=NB_CLK100M_DPLLSS_N	NB_CLK100M_DPLLSS_N — 6 30 71
15	LVDS_BKLT_CTL	LCDBKLT_PWM_UNBUF — 6 64
15	LVDS_BKLT_EN	LCDBKLT_PWREN — 6 64

AUDIO ALIASES

37 7	HDA_BITCLK	HDA_BIT_CLK — 6 23 69
69 37 23 9 7 6	HDA_SYNC	HDA_SYNC — 6 7 9 23 37 69
69 37 23 9 6	HDA_RST_L	HDA_RST_L — 6 9 23 37 69
37 7	HDA_SDATAIN0	HDA_SDIN0 — 6 23 69
37 7	HDA_SDATAOUT	HDA_SDOUT — 6 23 69

USB ALIASES

USB PORT [0] = External USB2.0 Port A

39	=USB2_EXTA_P	6 USB2_EXTA_P	USB_EXTA_P 24 69
39	=USB2_EXTA_N	6 USB2_EXTA_N	USB_EXTA_N 24 69
39	=EXTAUSB_OC_L	6 EXTAUSB_OC_L	USB_EXTA_OC_L 7 13 24
		39 6 USB2_MUXED_EXTA_N	USB_EXTA_MUXED_P 69
		39 6 USB2_MUXED_EXTA_P	USB_EXTA_MUXED_N 69

USB PORT [1] = PCI-E Mini Card

36	=USB2_AIRPORT_P	6 USB2_AIRPORT_P	USB_MINI_P 24 69
36	=USB2_AIRPORT_N	6 USB2_AIRPORT_N	USB_MINI_N 24 69

USB PORT [2] = Unused

	=USB2_3G_P	TP_USB2_3G_P — USB_EXTD_P 24 69
	=USB2_3G_N	TP_USB2_3G_N — USB_EXTD_N 24 69

USB PORT [3] = CAMERA

60	=USB2_CAMERA_P	6 USB2_CAMERA_P	USB_CAMERA_P 24 69
60	=USB2_CAMERA_N	6 USB2_CAMERA_N	USB_CAMERA_N 24 69

USB PORT [4] = IR CONTROLLER

40 7	=USB2_IR_P	69 24 9 6 USB_IR_P	USB_IR_P 6 9 24 69
40 7	=USB2_IR_N	69 24 9 6 USB_IR_N	USB_IR_N 6 9 24 69

USB PORT [5] = Trackpad(Wellspring)

40 7	=USB2_TRACKPAD_P	6 USB2_WSPRING_P	USB_TPAD_P 24 69
40 7	=USB2_TRACKPAD_N	6 USB2_WSPRING_N	USB_TPAD_N 24 69

USB PORT [6] = BLUETOOTH

	=USB2_BT_P	NC_USB_BT_P — USB_BT_P 24 69
	=USB2_BT_N	NC_USB_BT_N — USB_BT_N 24 69

USB PORT [7] = Unused

	NC_USB2_EXTB_P	USB_EXTB_P 24 69
	NC_USB2_EXTB_N	USB_EXTB_N 24 69
	=EXTAUSB_OC_L 6	EXTAUSB_OC_L — USB_EXTB_OC_L 7 13 24

USB PORT [8] = Unused

TP_USB_EXCARD_P	USB_EXCARD_P 24 69
TP_USB_EXCARD_N	USB_EXCARD_N 24 69

USB PORT [9] = Unused

TP_USB_EXTC_P	USB_EXTC_P 24 69
TP_USB_EXTC_N	USB_EXTC_N 24 69

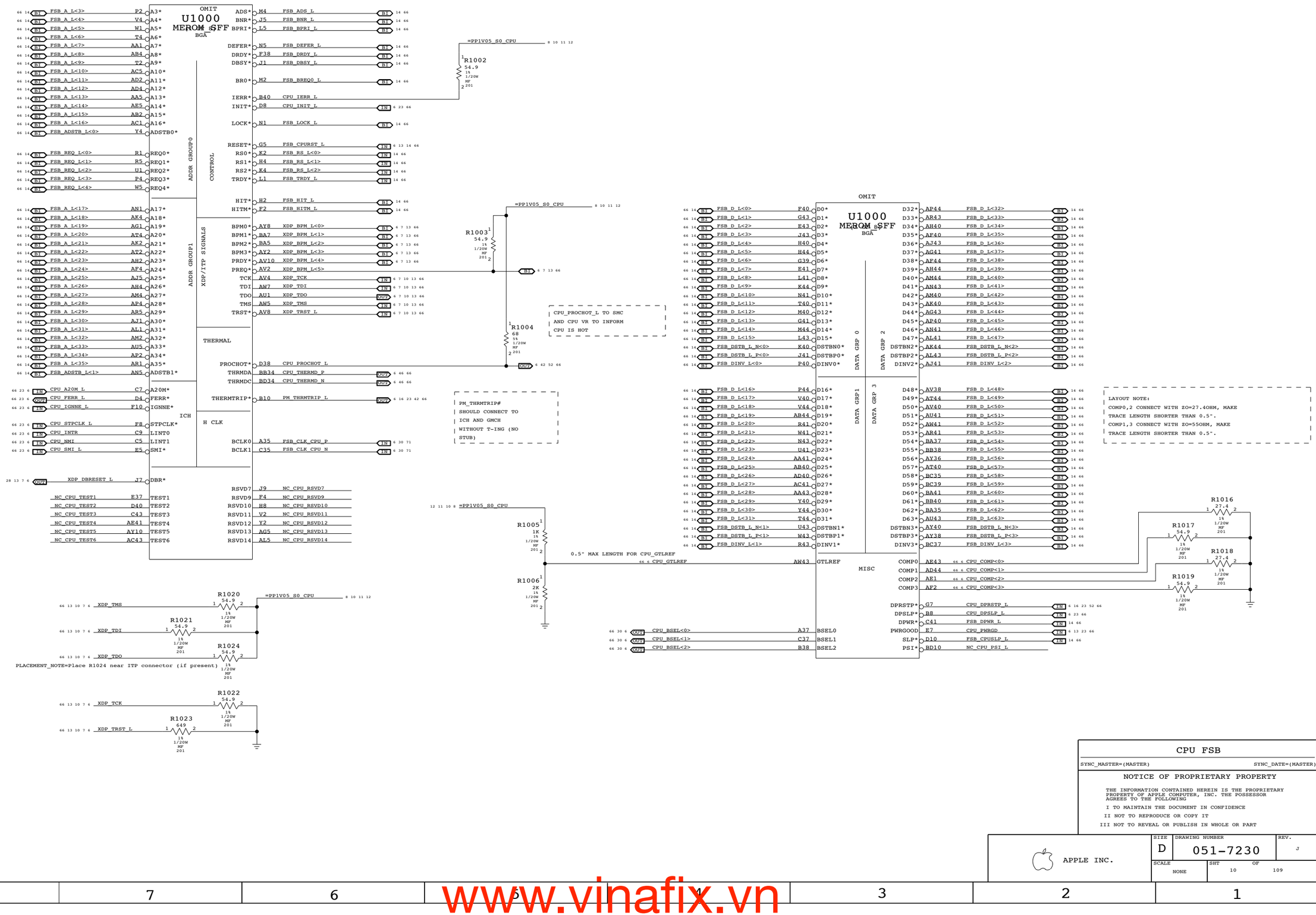
SIGNAL ALIAS /RESET

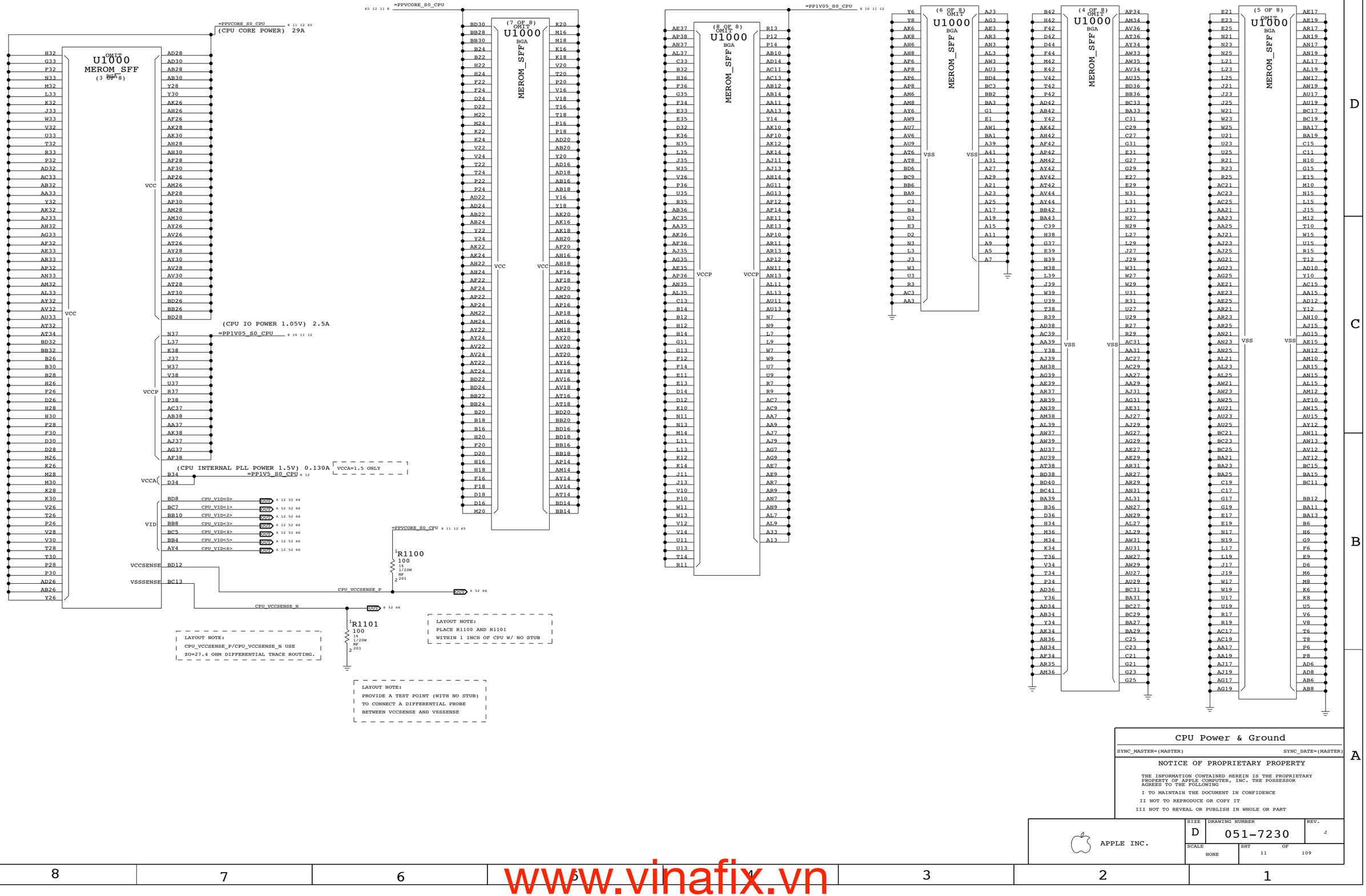
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J

SCALE: NONE SHT 9 OF 109





CPU Power & Ground

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 11 OF 109	

CPU VCORE HF AND BULK DECOUPLING

3x 330uF. 32x 10uF 0603, 28x 1uF 0402

Intel recommends 32+28 but is evaluating 24+24

65 11 8 =PPVCORE_S0_CPU

10UF 0603 = APN:138S0568 = MURATA,TAIYO,TDK,SAMSUNG

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C1200 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1201 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1202 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1203 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1204 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1205 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1206 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1207 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1208 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1209 10UF 20% 6.3V X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C1210 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1211 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1212 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1213 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1214 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1215 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1216 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1217 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1218 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1219 10UF 20% 6.3V X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C1220 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1221 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1222 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1223 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1224 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1225 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1226 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1227 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1228 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1229 10UF 20% 6.3V X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C1230 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1231 10UF 20% 6.3V X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C1240 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1241 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1242 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1243 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1244 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1245 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1246 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1247 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1248 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1249 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C1250 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1251 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1252 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1253 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1254 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1255 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1256 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1257 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1258 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1259 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C1260 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1261 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1262 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1263 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1264 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1265 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1266 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1267 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON SAME SIDE AS CPU

CRITICAL C1270 330UF 20% 2.0V TANT D2T
CRITICAL C1271 330UF 20% 2.0V TANT D2T

CRITICAL C1272 330UF 20% 2.0V TANT D2T

LAYOUT NOTE:
PLACE ON SAME SIDE AS CPU

Intel recommends 3x220UF @ 9mOHM

CPU VCORE VID CONNECTIONS

66 52 11 6 CPU_VID<0..6> — IMVP6_VID<0..6> 66
MAKE_BASE=TRUE

VCCA (CPU AVdd) DECOUPLING

11 8 =PP1V5_S0_CPU

1x 10uF, 1x 0.01uF

OMIT C1280 10uF 20% 6.3V X5R 603
C1281 0.01UF 10% 10V X5R 201

LAYOUT NOTE:
PLACE C1281 NEAR PIN B34 OF U1000

VCCP (CPU I/O) DECOUPLING

11 10 8 =PP1V05_S0_CPU

1X 330UF, 12X 2.2UF

OMIT C1283 2.2UF 20% 6.3V CERM 402-LF
OMIT C1284 2.2UF 20% 6.3V CERM 402-LF
OMIT C1285 2.2UF 20% 6.3V CERM 402-LF
OMIT C1286 2.2UF 20% 6.3V CERM 402-LF
OMIT C1287 2.2UF 20% 6.3V CERM 402-LF
OMIT C1288 2.2UF 20% 6.3V CERM 402-LF

CRITICAL C1290 330UF 20% 2.5V POLY CASE-C2-SM-1

OMIT C1291 2.2UF 20% 6.3V CERM 402-LF
OMIT C1292 2.2UF 20% 6.3V CERM 402-LF
OMIT C1293 2.2UF 20% 6.3V CERM 402-LF
OMIT C1294 2.2UF 20% 6.3V CERM 402-LF
OMIT C1295 2.2UF 20% 6.3V CERM 402-LF
OMIT C1296 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE C1290 CLOSE TO CPU
PLACE C1283-C1288 CLOSE TO FSB ADDRESS PINS
PLACE C1291-C1296 CLOSE TO FSB DATA PINS

CPU Decoupling & VID

SYNC_MASTER=MSARWAR SYNC_DATE=04/26/2006

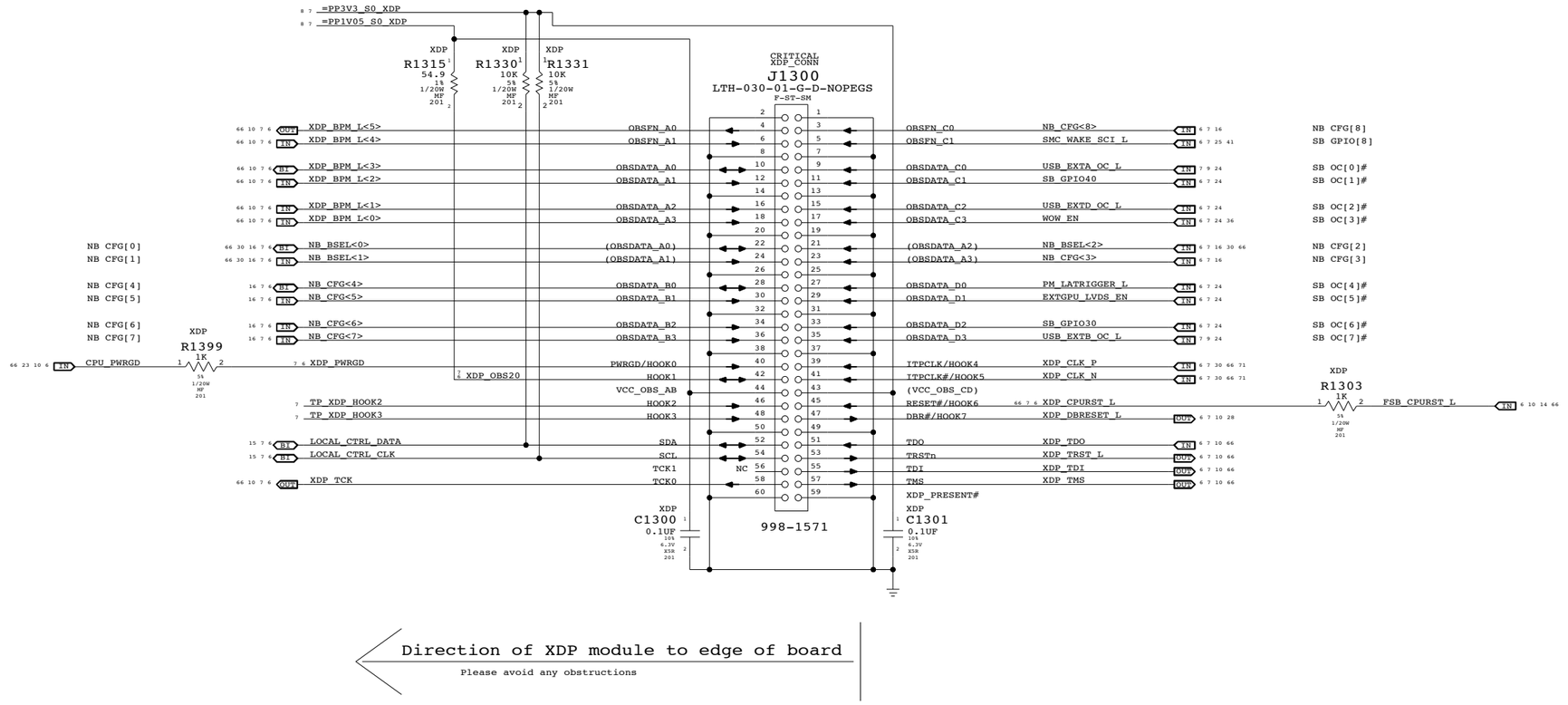
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 12 OF 109	

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0451 adapter board to support CPU, NB & SB debugging.



Direction of XDP module to edge of board

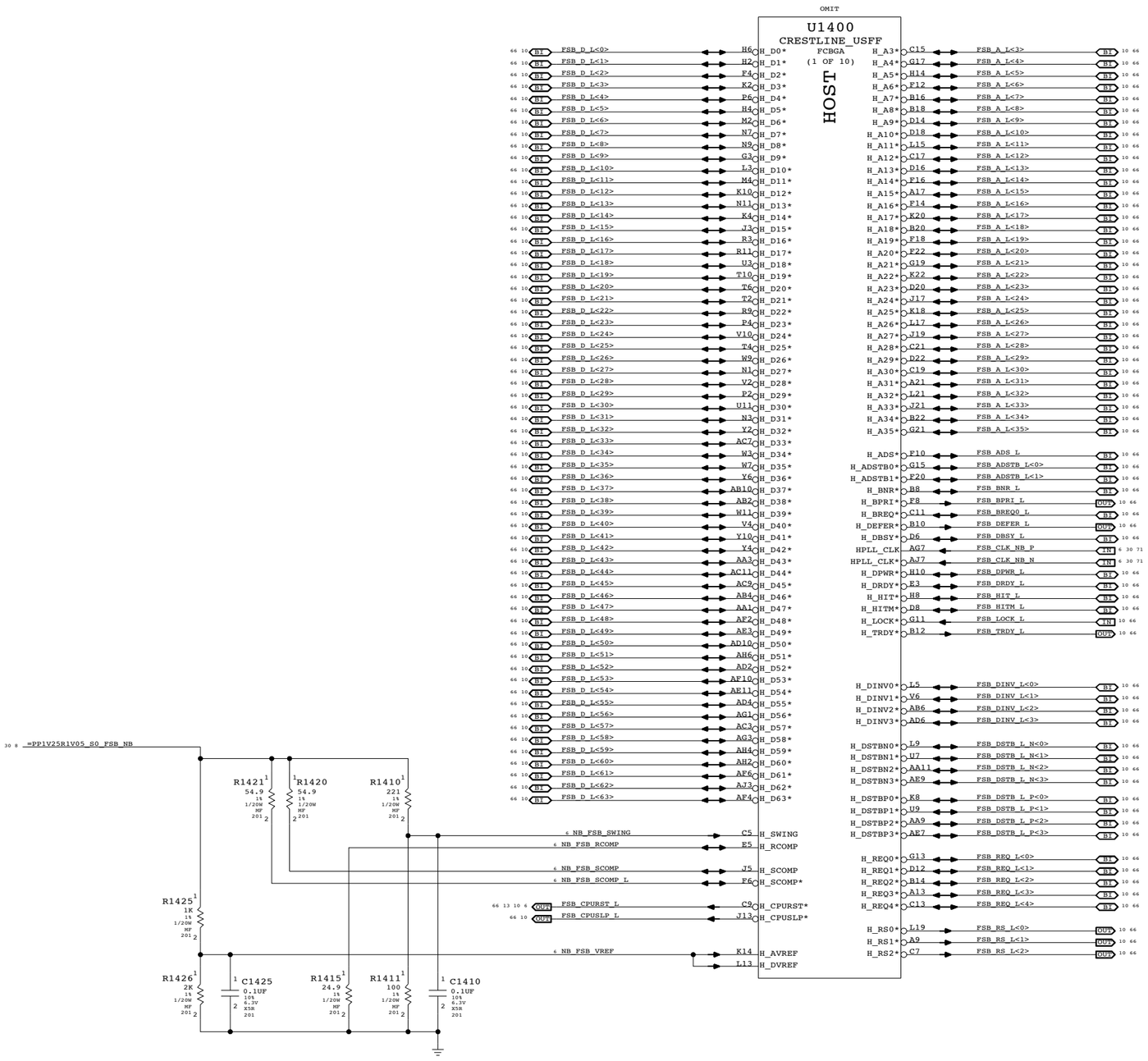
Please avoid any obstructions

eXtended Debug Port (XDP)

SYNC_MASTER=M75 SYNC_DATE=01/24/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 13 OF 109	



NB CPU Interface

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 14 OF 109	

LVDS Disable

Can leave all signals NC if LVDS is not implemented.
Tie VCC_TX_LVDS and VCCA_LVDS to GND.

If SDVO is used, VCCD_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable / CRT Enable

Tie TVx_DAC and TVx_RTN to GND. Must power all TVDAC rails. VCCA_TVx_DAC and VCCA_DAC_BG can share filtering with VCCA_CRT_DAC.

CRT Disable / TV-Out Enable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND.
All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA_CRT.

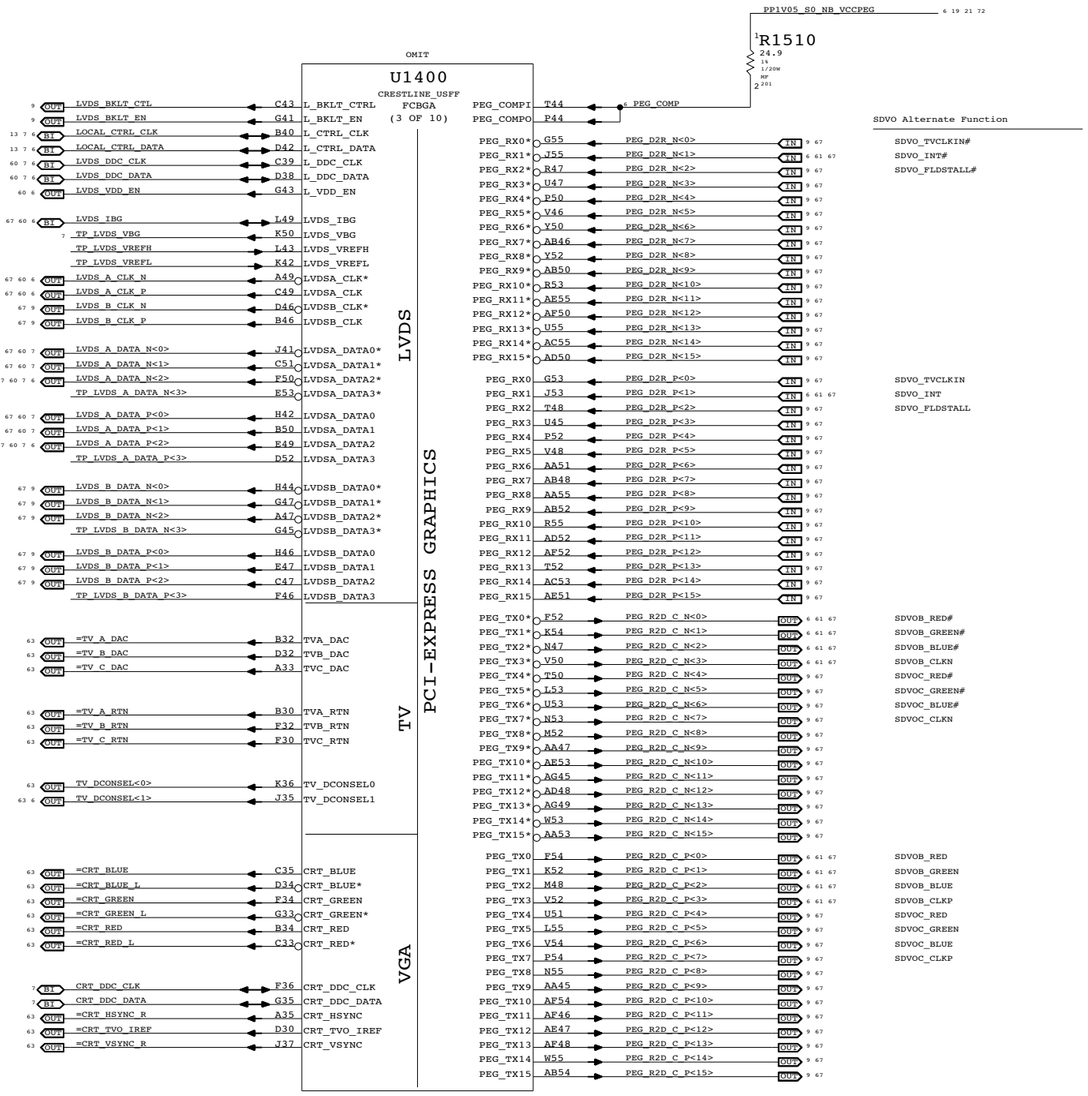
CRT & TV-Out Disable

Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT_TVO_IREF to GND.
Can tie the following rails to GND:
VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC, VCCD_CRT, VCCD_QDAC and VCC_SYNC.

NOTE: Must keep VDDC_TVDAC powered and filtered at all times!

Internal Graphics Disable

Follow instructions for LVDS and CRT & TV-Out Disable above.
Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and TV_DCONSELx to GND.
Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.
Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).
Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore).
Tie VCC_AXG and VCC_AXG_NCTF to GND.
Leave GFX_VID<3..0> and GFX_VR_EN as NC.



NB PEG / Video Interfaces	
SYNC_MASTER=M70	SYNC_DATE=01/09/2007

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	J
	SCALE: NONE	SHT 15 OF 109	

NB_CFG<3>	RESERVED
NB_CFG<4>	RESERVED
NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2
NB_CFG<6>	RESERVED
NB_CFG<7>	RESERVED
NB_CFG<8>	RESERVED
NB_CFG<9> PCIe Graphics Lane Reversal	High = Normal Low = Reversed
NB_CFG<10>	RESERVED
NB_CFG<11>	RESERVED
NB_CFG<12>	See Below
NB_CFG<13>	See Below
NB_CFG<14>	RESERVED
NB_CFG<15>	RESERVED
NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled
NB_CFG<17>	RESERVED
NB_CFG<18>	RESERVED
NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal
NB_CFG<20> Concurrent SDVO/PCIe x1	High = Both active Low = Only SDVO or PCIe x16

NB_CFG<13:12>

00 = RESERVED
01 = XOR Mode Enabled
10 = All-Z Mode Enabled
11 = Normal Operation

NB CFG<5> chooses DMI x4 w/ TP

NB_CFG<9> 6 16
NBCFG_PEG_REVERSE
R1659 4.02K 1% 1/20W MF 201

NB_CFG<16> 6 16
NBCFG_DYN_ODT_DISABLE
R1666 4.02K 1% 1/20W MF 201

=PP3V3_S0_NB_VCCHV 8 16 19 21 22
NBCFG_DMI_REVERSE
R1669 4.02K 1% 1/20W MF 201
NB_CFG<19> 6 16

=PP3V3_S0_NB_VCCHV 8 16 19 21 22
NBCFG_SDVO_AND_PCIE
R1670 4.02K 1% 1/20W MF 201
NB_CFG<20> 6 16

NB CFG<8:0> used for debug access

NB CFG<13:12> require ICT access

22 21 19 16 8 =PP3V3_S0_NB_VCCHV
R1630 10K 5% 1/20W MF 201
R1631 10K 5% 1/20W MF 201
41 6 IN PM_EXTTS_L<0>
41 6 IN PM_EXTTS_L<1>

OMIT

U1400
CRESTLINE_USFF
FCBGA
(2 OF 10)

RSVD bit ordering based on CRB numbering

TP_NB_RSVD<42>	A39	RSVD
7 TP_NB_RSVD<8>	AG11	
7 TP_NB_RSVD<7>	AG9	
7 TP_NB_RSVD<5>	AH10	
7 TP_NB_RSVD<6>	AJ11	
TP_NB_RSVD<12>	AJ43	
TP_NB_RSVD<11>	AL43	
TP_NB_RSVD<13>	AN43	
TP_NB_RSVD<10>	AR43	
TP_NB_RSVD<45>	B36	
TP_NB_RSVD<41>	B38	
7 TP_NB_RSVD<21>	B55	
7 TP_NB_RSVD<28>	BA33	
7 TP_NB_RSVD<35>	BB22	
7 TP_NB_RSVD<29>	BC33	
7 TP_NB_RSVD<30>	BF22	
7 TP_NB_RSVD<31>	BE23	
7 TP_NB_RSVD<24>	BH18	
7 TP_NB_RSVD<36>	BE27	
7 TP_NB_RSVD<22>	BJ17	
7 TP_NB_RSVD<25>	BK16	
7 TP_NB_RSVD<27>	BK18	
TP_NB_RSVD<34>	BK32	
7 TP_NB_RSVD<26>	BL17	
7 TP_NB_RSVD<23>	BL19	
TP_NB_RSVD<43>	C37	
TP_NB_RSVD<9>	D10	
TP_NB_RSVD<44>	D36	
7 TP_NB_RSVD<4>	G51	
7 TP_NB_RSVD<20>	G9	
7 TP_NB_RSVD<3>	H52	
7 TP_NB_RSVD<14>	J25	
7 TP_NB_RSVD<1>	M46	
7 TP_NB_RSVD<2>	N45	

DDR MUXING

SM_CK0	BC37	MEM_CLK_P<0>	OUT 31 33 68
SM_CK1	BC25	MEM_CLK_P<1>	OUT 31 33 68
SM_CK3	BB36	MEM_CLK_P<3>	OUT 32 33 68
SM_CK4	BB24	MEM_CLK_P<4>	OUT 32 33 68
SM_CK0*	BA37	MEM_CLK_N<0>	OUT 31 33 68
SM_CK1*	BC23	MEM_CLK_N<1>	OUT 31 33 68
SM_CK3*	BB34	MEM_CLK_N<3>	OUT 32 33 68
SM_CK4*	BB26	MEM_CLK_N<4>	OUT 32 33 68
SM_CKE0	BE33	MEM_CKE<0>	OUT 31 33 68
SM_CKE1	BE35	MEM_CKE<1>	OUT 31 33 68
SM_CKE3	BF40	MEM_CKE<3>	OUT 32 33 68
SM_CKE4	BE39	MEM_CKE<4>	OUT 32 33 68
SM_CS0*	BA23	MEM_CS_L<0>	OUT 31 33 68
SM_CS1*	BH16	MEM_CS_L<1>	OUT 31 33 68
SM_CS2*	BE15	MEM_CS_L<2>	OUT 32 33 68
SM_CS3*	BH14	MEM_CS_L<3>	OUT 32 33 68
SM_ODT0	BJ15	MEM_ODT<0>	OUT 6 31 33 68
SM_ODT1	BF20	MEM_ODT<1>	OUT 6 31 33 68
SM_ODT2	BE13	MEM_ODT<2>	OUT 6 32 33 68
SM_ODT3	BH12	MEM_ODT<3>	OUT 6 32 33 68
SM_RCOMP	BL13	6 MEM_RCOMP	
SM_RCOMP*	BK14	6 MEM_RCOMP_L	
SM_RCOMP_VOH	BK36	6 MEM_RCOMP_VOH	
SM_RCOMP_VOL	BL37	6 MEM_RCOMP_VOL	
SM_VREF0	AM54	PP0V9_S3M_MEM_NBVREFA	IN 8 21 68
SM_VREF1	AT12	PP0V9_S3M_MEM_NBVREFB	IN 8 21 68

68 21 18 8 =PP1V8_S3M_MEM_NB

R1610 20 1% 1/20W MF 201
R1620 1K 1% 1/20W MF 201
C1623 0.01UF 10% 10V X5R 201
OMIT C1622 2.2UF 20% 6.3V CERM 402-LF
R1622 3.01K 1% 1/20W MF 201
C1615 0.1UF 10% 6.3V X5R 201
C1616 0.1UF 10% 6.3V X5R 201
R1611 20 1% 1/20W MF 201
C1625 0.01UF 10% 10V X5R 201
OMIT C1624 2.2UF 20% 6.3V CERM 402-LF
R1624 1K 1% 1/20W MF 201

CLK

DPLL_REF_CLK	C45	=NB_CLK96M_DOT_P	IN 9
DPLL_REF_CLK*	B44	=NB_CLK96M_DOT_N	IN 9
DPLL_REF_SSCLK	H50	=NB_CLK100M_DPLLSS_P	IN 9
DPLL_REF_SSCLK*	G49	=NB_CLK100M_DPLLSS_N	IN 9
PEG_CLK	N51	NB_CLK100M_PCIE_P	IN 6 30 71
PEG_CLK*	M50	NB_CLK100M_PCIE_N	IN 6 30 71

Clk used for PEG and DMI

CFG

66 30 13 7 6 IN NB_BSEL<0>	H28	CFG0	
66 30 13 7 6 IN NB_BSEL<1>	G25	CFG1	
66 30 13 7 6 IN NB_BSEL<2>	C25	CFG2	
13 7 6 OUT NB_CFG<3>	K24	CFG3	IPU
13 7 6 BI NB_CFG<4>	B28	CFG4	IPU
13 7 6 BI NB_CFG<5>	G27	CFG5	IPU
13 7 6 OUT NB_CFG<6>	B26	CFG6	IPU
13 7 6 OUT NB_CFG<7>	D26	CFG7	IPU
13 7 6 OUT NB_CFG<8>	D24	CFG8	IPU
16 6 NB_CFG<9>	F26	CFG9	IPU
7 TP_NB_CFG<10>	A25	CFG10	IPU
7 TP_NB_CFG<11>	L23	CFG11	IPU
TP_NB_CFG<12>	D28	CFG12	IPU
TP_NB_CFG<13>	F24	CFG13	IPU
7 TP_NB_CFG<14>	C29	CFG14	IPU
7 TP_NB_CFG<15>	C27	CFG15	IPU
16 6 NB_CFG<16>	A29	CFG16	IPU
7 TP_NB_CFG<17>	J27	CFG17	IPU
TP_NB_CFG<18>	G31	CFG18	IPD
16 6 NB_CFG<19>	K30	CFG19	IPD
16 6 NB_CFG<20>	L37	CFG20	IPD

DMI

DMI_RXN0	AL45	DMI_S2N_N<0>	IN 6 24 67
DMI_RXN1	AK54	DMI_S2N_N<1>	IN 6 24 67
DMI_RXN2	AJ55	DMI_S2N_N<2>	IN 6 24 67
DMI_RXN3	AH52	DMI_S2N_N<3>	IN 6 24 67
DMI_RXP0	AM46	DMI_S2N_P<0>	IN 6 24 67
DMI_RXP1	AK52	DMI_S2N_P<1>	IN 6 24 67
DMI_RXP2	AJ53	DMI_S2N_P<2>	IN 6 24 67
DMI_RXP3	AH50	DMI_S2N_P<3>	IN 6 24 67
DMI_TXN0	AH48	DMI_N2S_N<0>	OUT 6 24 67
DMI_TXN1	AK48	DMI_N2S_N<1>	OUT 6 24 67
DMI_TXN2	AG55	DMI_N2S_N<2>	OUT 6 24 67
DMI_TXN3	AL53	DMI_N2S_N<3>	OUT 6 24 67
DMI_TXP0	AJ47	DMI_N2S_P<0>	OUT 6 24 67
DMI_TXP1	AK50	DMI_N2S_P<1>	OUT 6 24 67
DMI_TXP2	AG53	DMI_N2S_P<2>	OUT 6 24 67
DMI_TXP3	AL55	DMI_N2S_P<3>	OUT 6 24 67

PM

25 6 OUT PM_BMBUSY_L	F44	PM_BM_BUSY*	
66 52 23 10 6 IN CPU_DPRSTP_L	C41	PM_DPRSTP*	
	L39	PM_EXT_TS0*	
	J39	PM_EXT_TS1*	
52 28 9 6 IN VR_PWRGOOD_DELAY	AT50	PWROK	
28 6 IN NB_RESET_L	BB20	RSTIN*	
66 42 23 10 6 OUT PM_THRMTRIP_L	F28	THERMTRIP*	
66 52 25 6 IN PM_DPRSLPVR	F40	DPRSLPVR	

GRAPHICS VID

		GFX_VID<4>	OUT 53
GFX_VID0	G37	GFX_VID<0>	OUT 6 22 53
GFX_VID1	A45	GFX_VID<1>	OUT 6 22 53
GFX_VID2	B42	GFX_VID<2>	OUT 6 22 53
GFX_VID3	D44	GFX_VID<3>	OUT 6 22 53
GFX_VR_EN	F42	=GFX_VR_EN	OUT 9

NC

7 TP_NB_NC<14>	A52	NC
7 TP_NB_NC<13>	A54	
7 TP_NB_NC<12>	B54	
7 TP_NB_NC<10>	BH1	
7 TP_NB_NC<2>	BH55	
7 TP_NB_NC<9>	BK1	
7 TP_NB_NC<8>	BK2	
7 TP_NB_NC<4>	BK54	
7 TP_NB_NC<1>	BK55	
7 TP_NB_NC<7>	BL2	
7 TP_NB_NC<6>	BL4	
7 TP_NB_NC<5>	BL52	
7 TP_NB_NC<3>	BL54	
7 TP_NB_NC<11>	D55	

ME

CL_CLK	BF52	CLINK_NB_CLK	BI 6 25 70
CL_DATA	BE53	CLINK_NB_DATA	BI 6 25 70
CL_PWROK	AP50	=NB_CLINK_MPWROK	IN 9
CL_RST*	BH52	CLINK_NB_RESET_L	OUT 6 25 70
CL_VREF	BF54	70 6 NB_CLINK_VREF	

MISC

SDVO_CTRL_CLK	K38	SDVO_CTRLCLK	BI 6 61
SDVO_CTRL_DATA	K40	SDVO_CTRLDATA	BI 6 61
CLKREQ*	G39	NB_CLKREQ_L	OUT 6 29
ICH_SYNC*	D40	NB_SB_SYNC_L	OUT 6 25
TEST1	F38	6 NB_TEST1	
TEST2	K34	6 NB_TEST2	

R1691 20K 5% 1/20W MF 201
R1690 0 5% 1/20W MF 201

PP1V25_S0M_NB_VCCAXD 19 21
R1640 1K 1% 1/20W MF 201
C1640 0.1UF 10% 6.3V X5R 201
R1641 392 1% 1/20W MF 201

NOTE: GMCH CL_PWROK input must be PWRGD signal for PP3V3_S0M, PP3V3_S0MWOL, PP1V8_S3M, PP1V25_S0M, PP1V05_S0M, PP0V9_S3M and PP0V9_S0M.
If ME/AMT is not used, short CL_PWROK to PWROK.

NB Misc Interfaces

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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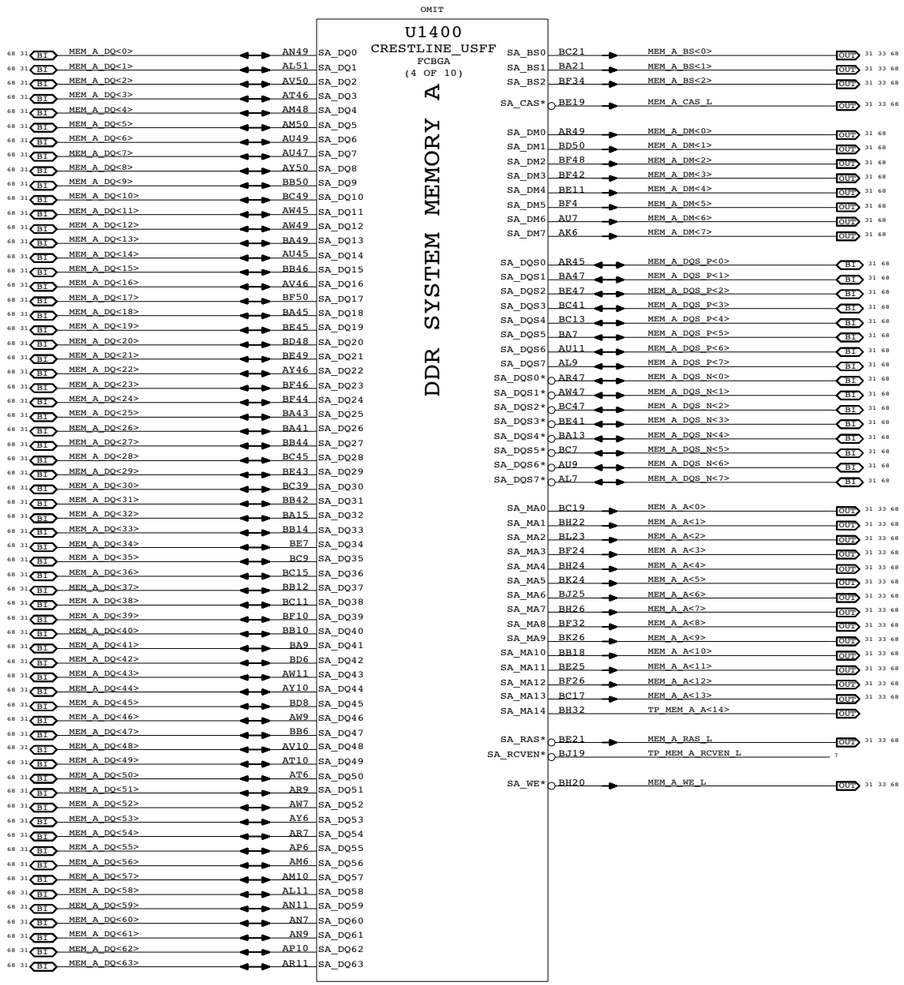
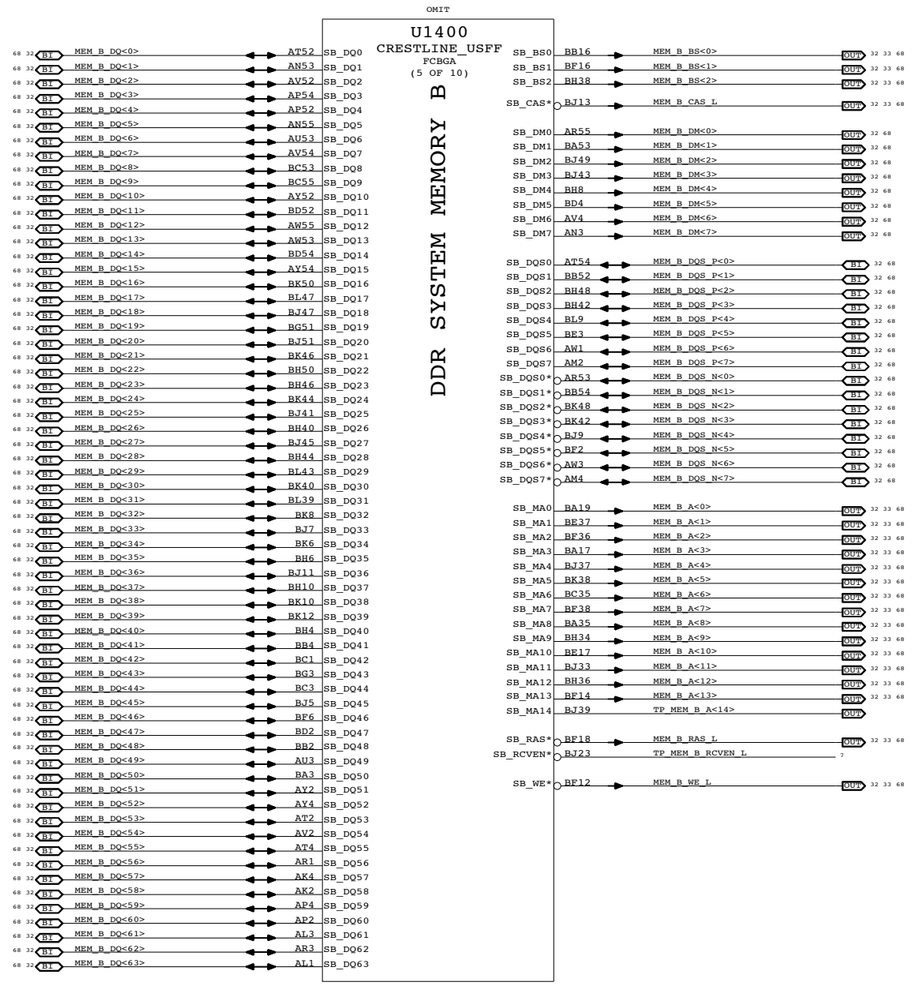
SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 16 OF 109	





NB DDR2 Interfaces

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SCALE	SHT	OF
NONE	17	109

NCTF balls are Not Critical To Function

These connections can break without impacting part performance.

=PPVCORE_S0_NB_GFX 8 18 22 53 65

=PPVCORE_S0_NB 21 18 8

1310 mA (Ext Graphics)
1600 mA (Int Graphics)

VCC_AXG_NCTF: AA13 AA15 AC13 AC16 AD15 AD16 AE13

OMIT
POWER
(6 OF 10)
U1400
FCBGA
CRESTLINE_USFF

VCC: AA32 AA34 AA35 AA38 AA37 AC32 AC34 AC35 AC37 AC38 AD34 AD35 AD37 AD38 AE35 AE37 AG35 AG37 AH37 AH38 L29 W35 W38 Y32 Y34 Y35 Y37 Y38

VCC_AXG_NCTF: AE15 AE16 AG13 AG15 AG16 AH16 AJ13 AJ15 AJ16 AL13 AL15 AM15 AN13 R27 R29 R31 T27 T29 T31 U27 U29 U31 Y15

=PPVCORE_S0_NB_GFX 8 18 22 53 65

7700 mA (Int Graphics)

W29 Y19 Y21 Y25 Y27 Y28 Y29 AA18 AA19 AA21 AA22 AA24 AA25 AA27 AA28 AA29 AC18 AC19 AC21 AC22 AC24 AC25 AC27 AC28 AC29 AD18 AD19 AD21 AD22 AD24 AD25 AD27 AD28 AD29 AD31 AE18 AE21 AE24 AE27 AE28 AE31 AG18 AG19 AG21 AG22 AG24 AG25 AG27 AG29 AH19 AH21

=PP1V8_S3M_MEM_NB 68 21 16 8

3300 mA (2 ch, 667MHz)
2700 mA (2 ch, 533MHz)
1700 mA (1 ch, 667MHz)
1395 mA (1 ch, 533MHz)
5 mA (standby)

VCC_SM: BA27 BA29 BA31 BB28 BB30 BB32 BC27 BC29 BC31 BD28 BD30 BE29 BE31 BF28 BF30 BG27 BG29 BG31 BH28 BH30 BJ29 BK28 BK30 BL29

VCC_SM_NCTF: AW36 AW38 AW40

VCC_SM_LF: AP46 BC43 BA39 BA25 BA11 BF8 AV6

VCC_AXG: AH22 AH24 AH25 AH27 AH28 AH29 AJ18 AJ21 AJ24 AJ27

VCC_AXG: AJ28 AJ22 AJ24 AJ25 AJ27 AJ28 W27

NB_VCCSM_LF1 68 6
NB_VCCSM_LF2 68 6
NB_VCCSM_LF3 68 6
NB_VCCSM_LF4 68 6
NB_VCCSM_LF5 68 6
NB_VCCSM_LF6 68 6
NB_VCCSM_LF7 68 6

C1807 0.1UF 10% 6.3V X5R 201
C1806 0.1UF 10% 6.3V X5R 201
C1805 0.22UF 20% 6.3V X5R 402
C1804 0.22UF 20% 6.3V X5R 402
C1803 0.47UF 10% 6.3V CERM-X5R 402
C1802 OMIT 1uF 10% 6.3V CERM 402
C1801 OMIT 1uF 10% 6.3V CERM 402

=PP1V25_S0M_NB_VCCA_SM 21
640mA

=PPVCORE_S0_NB 21 18 8

POWER
OMIT
(7 OF 10)
U1400
FCBGA
CRESTLINE_USFF

VCC_NCTF: AA40 AA41 AC40 AC41 AD40 AE40 AE41 AE43 AG40 AG41 AG43 AH40 AH41 R35 R38 R40 R43 T35 T38 T40 U35 U38 U40 U41 U43 W40 W41 Y40

VCCA_SM: AL18 AM18 AN22 AN24 AN37 AN38

VCCA_SM_NCTF: AN15 AN16 AR13 AR15 AR16 AR22 AR24 AR25 AR37 AR38 AT15 AT18 AT19 AT21 AT22 AT24 AT25 AT27 AT28 AT29 AT34 AT35 AT37 AT38 AU13 AU16 AU18 AU19 AU21 AU22 AU24 AU25 AU27 AU28 AU29 AU31 AU32 AU34 AU35 AW14 AW16 AW26 AW28 AW30 AW32

=PP1V05_S0M_NB_VCCAXM 21 18 8

540mA

VCC_AXM: AH31 AH32 AJ31 AJ32 AJ34 AJ35 AL31 AL32 AL34 AL35 AL37 AL38 AM31 AM32

=PP1V05_S0M_NB_VCCAXM 21 18 8

=PP1V05_S0M_NB_VCCAXM 21 18 8

VCC_AXM_NCTF: AL40 AL41 AM40 AM41 AN40 AN41 AR41 AT40 AT41 AU41 AU43 AW42

VSS_SCB: BL55 BL1 D1 B2 A4 A55

Current numbers from Crestline EDS, doc #21749.

NB Power 1

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SIZE	DRAWING NUMBER	REV.
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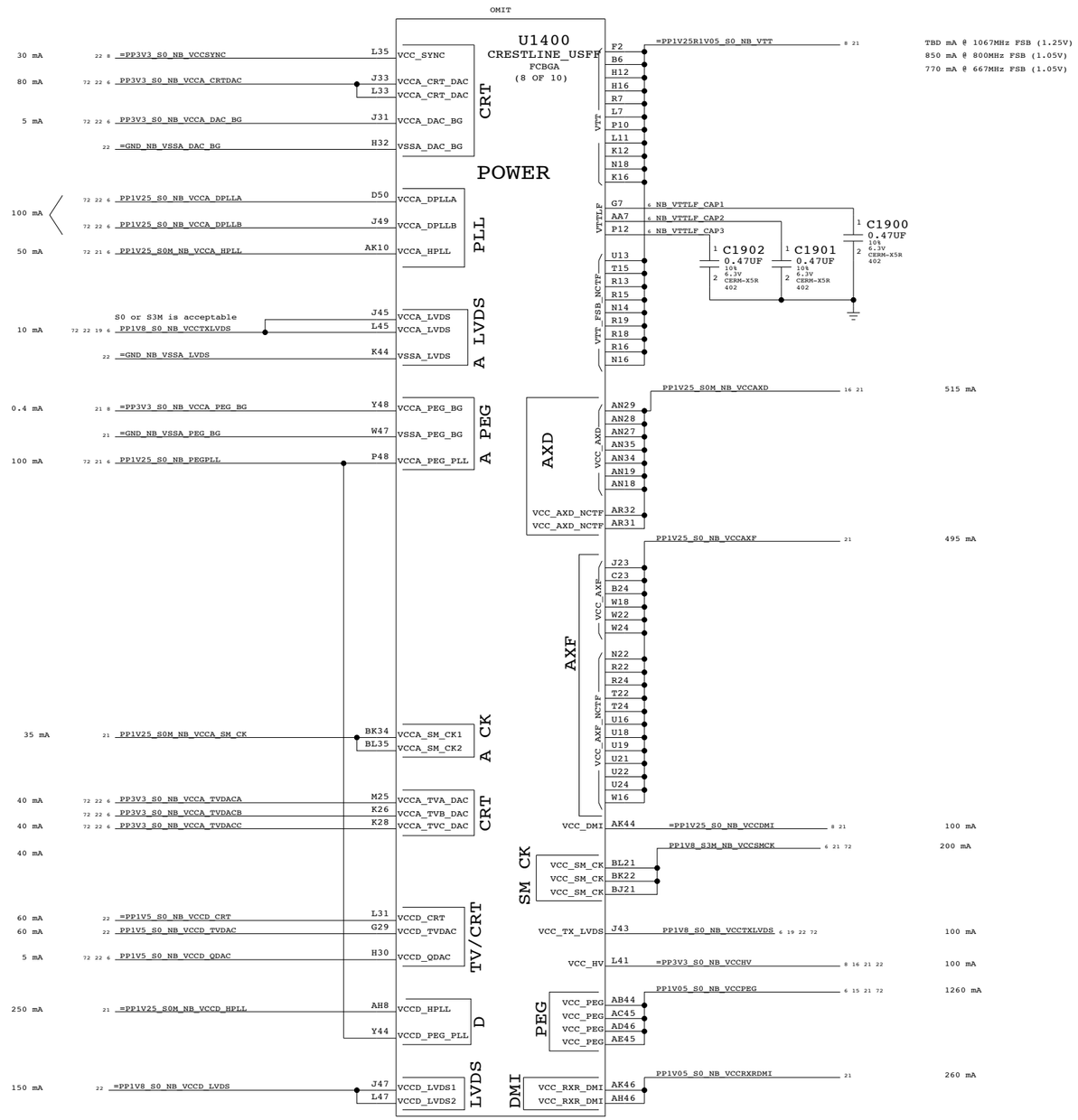

Current numbers from Crestline EDS, doc #21749.

NB Power 2

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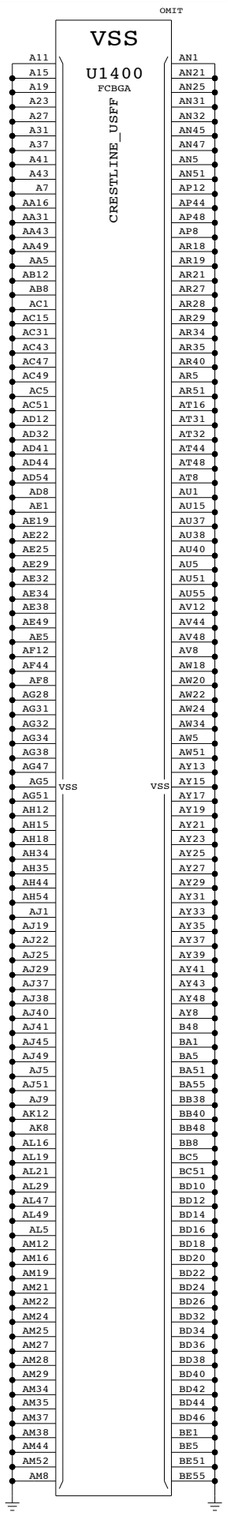
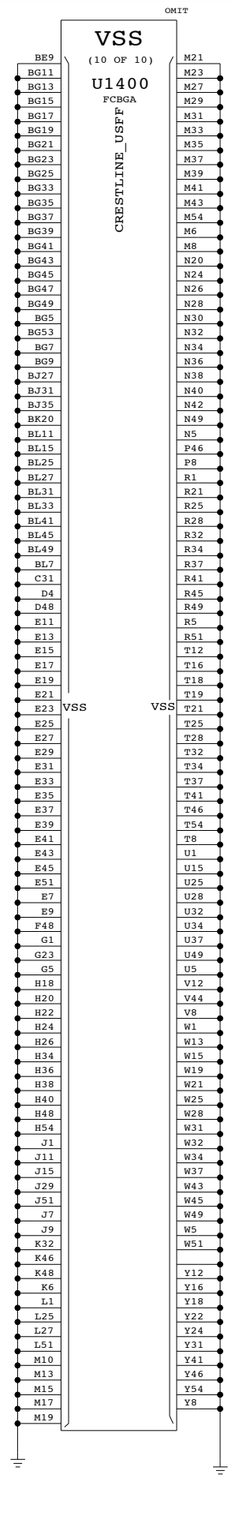
APPLE INC.

SIZE D | DRAWING NUMBER 051-7230 | REV. J

SCALE NONE | SHT 19 OF 109





NB Grounds

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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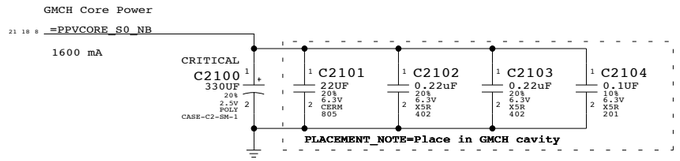

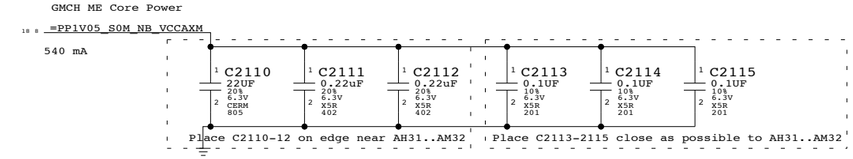

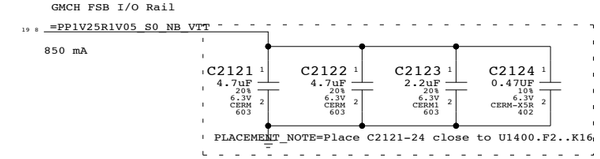

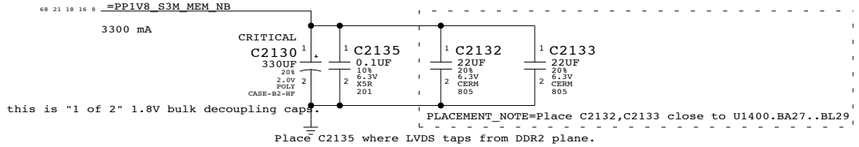

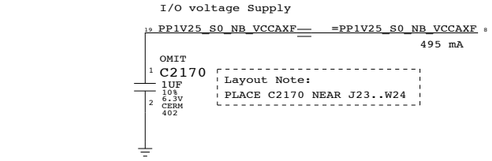

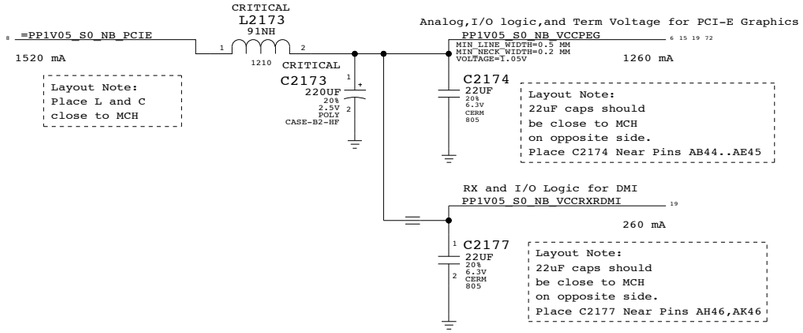

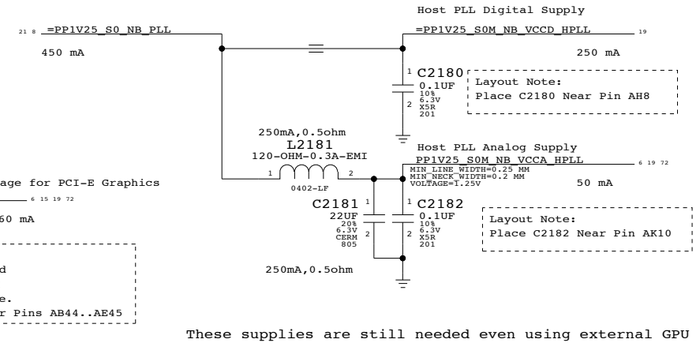

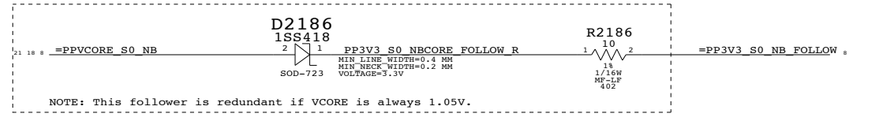

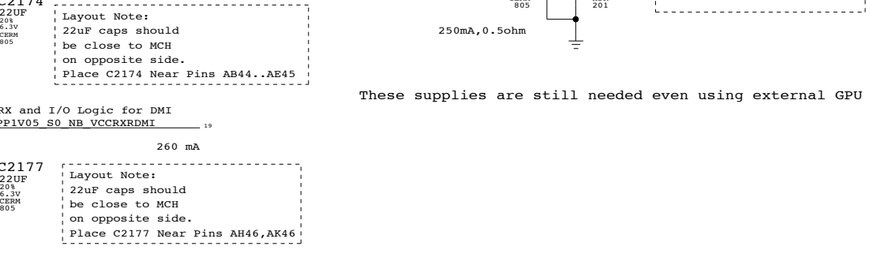

Current numbers from Crestline EDS Addendum, doc .....

NB Standard Decoupling

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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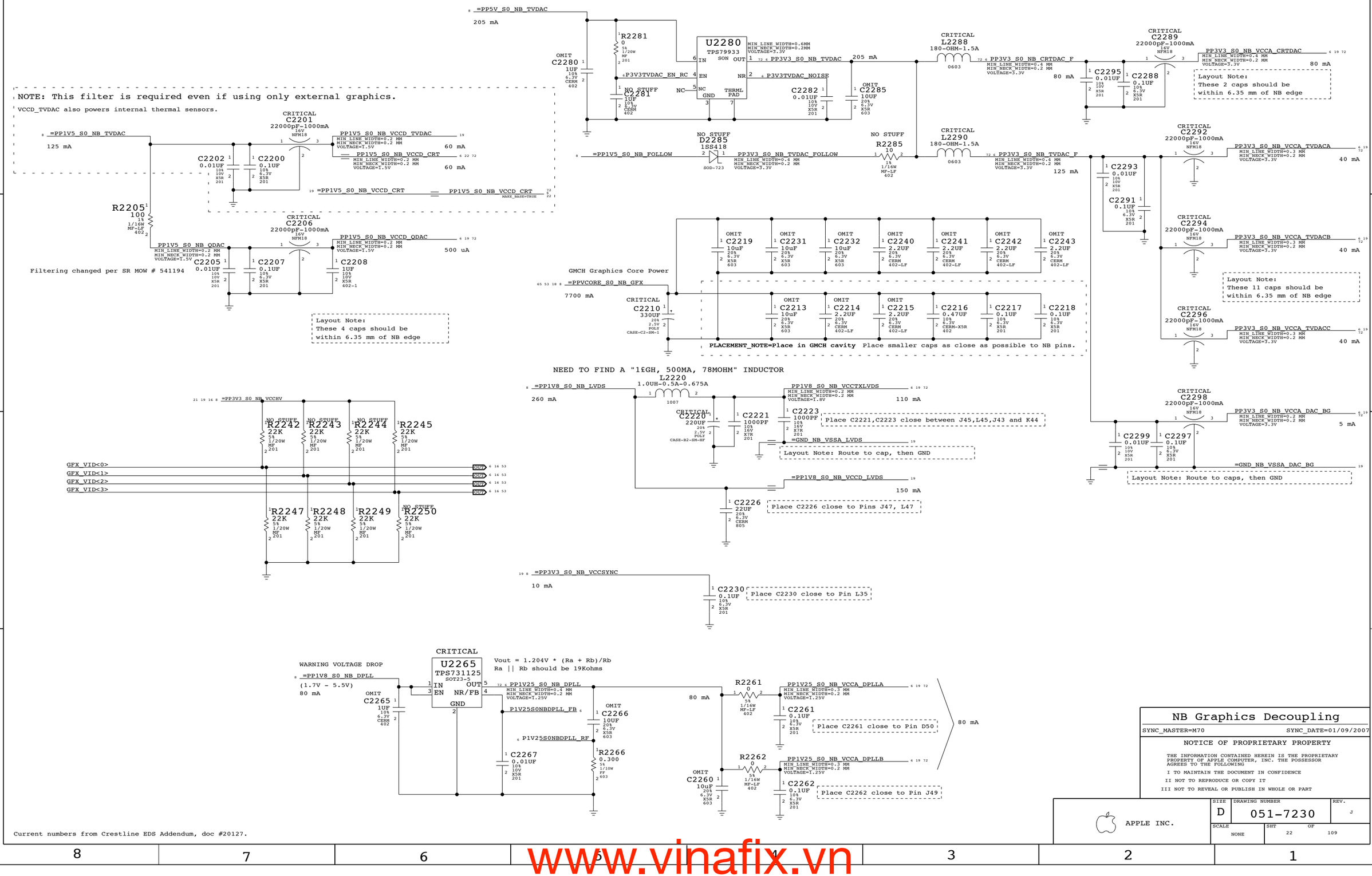

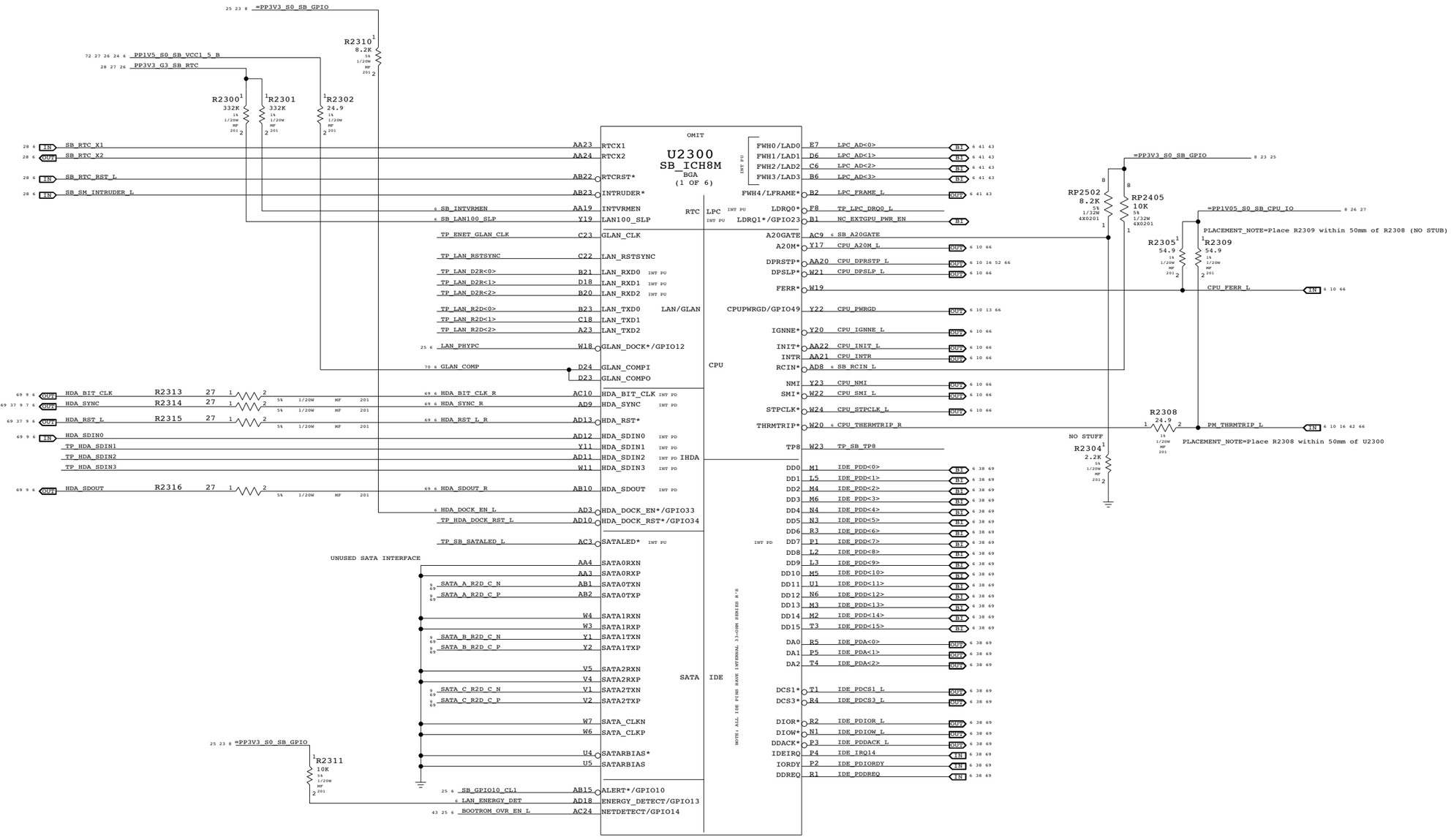

	HDA
HDA_BIT_CLK	24.000MHZ CLOCK W/INTERNAL WEAK PD
HDA_RST#	
HDA_SDIN[0-2]	INTEGRATED PDs
HDA_SDOUT	INTEGRATED PD
ACE_SYNC	INTEGRATED PD

SB Enet, Disk, FSB, LPC

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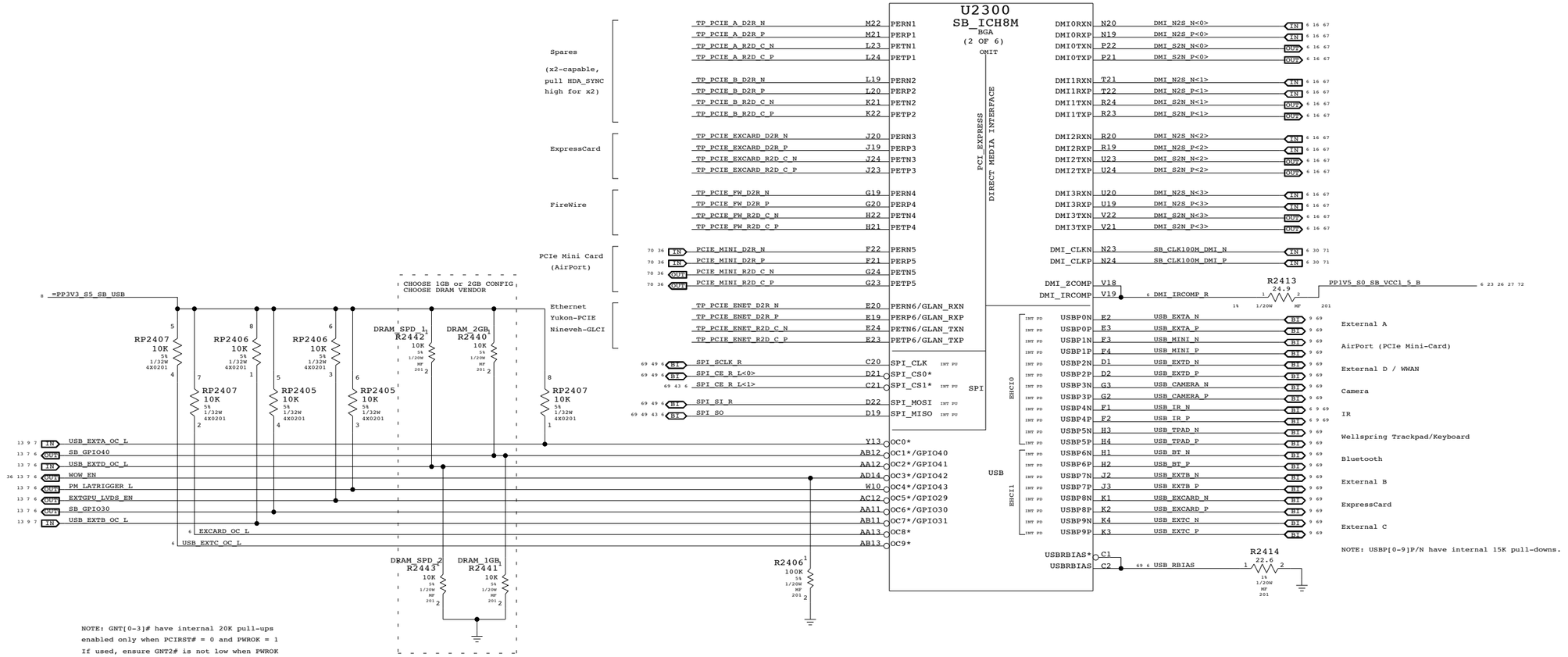

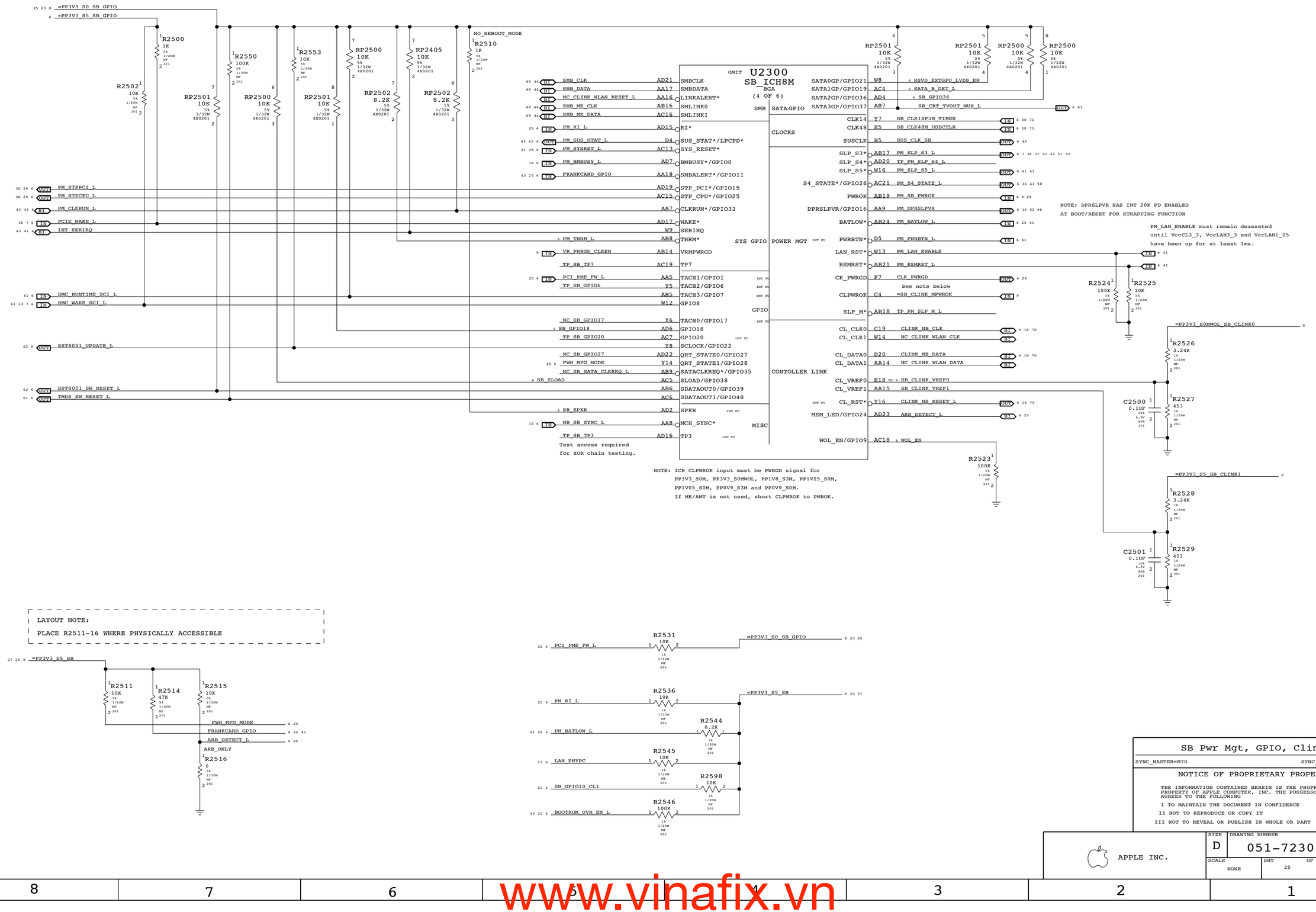

SB Pwr Mgt, GPIO, Clink	
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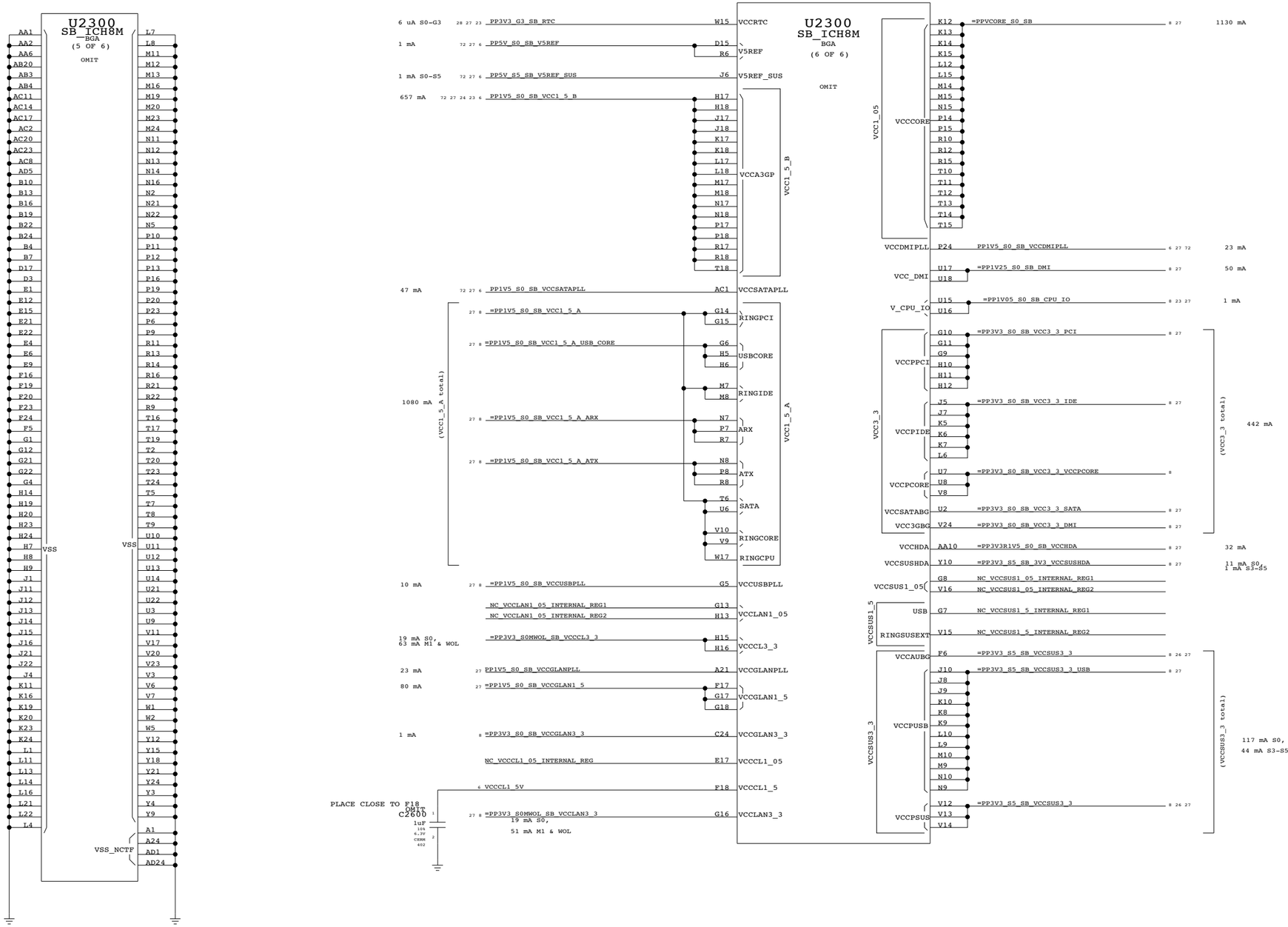
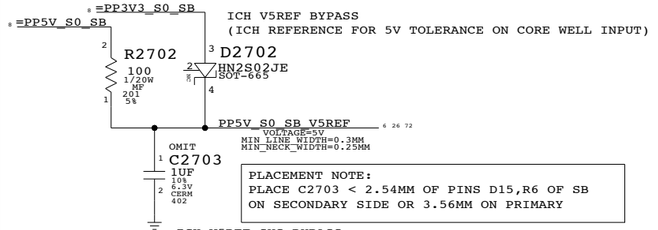
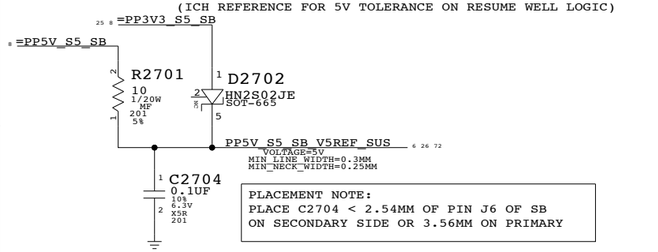
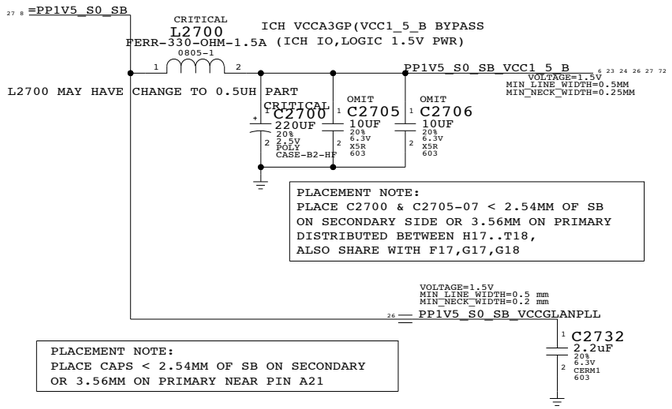
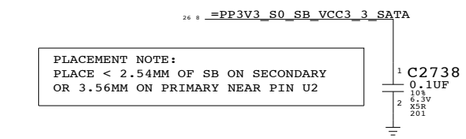
	SCALE: NONE	SHT 25 OF 109	

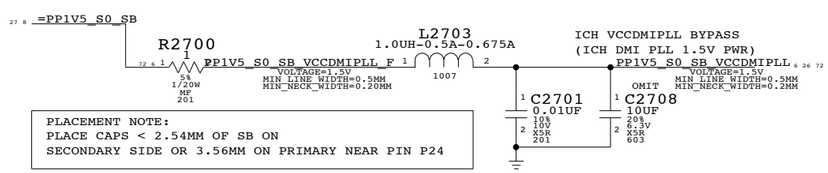


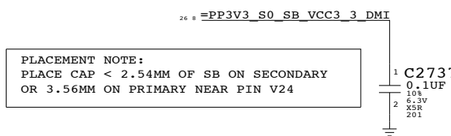


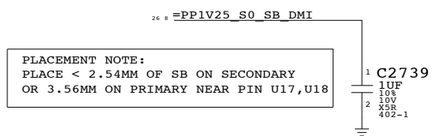


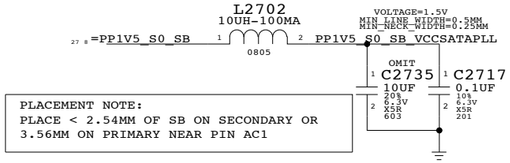


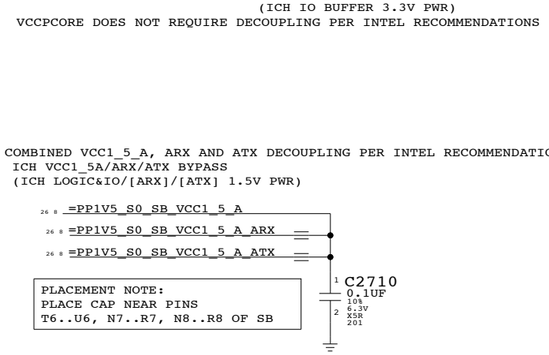


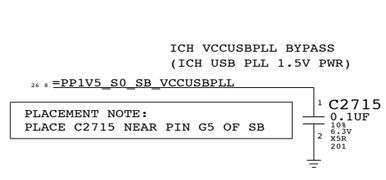


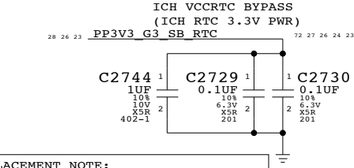


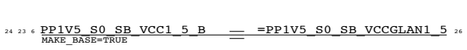


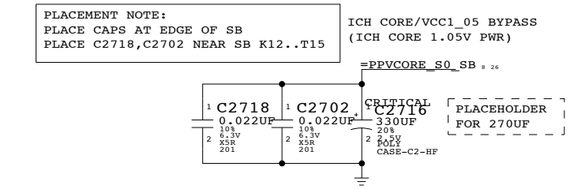


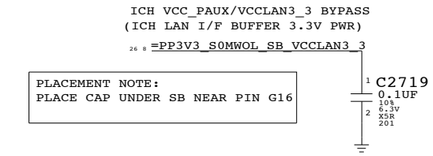


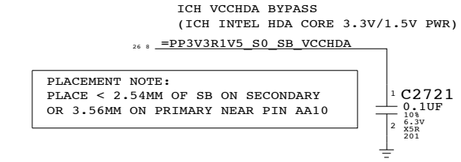


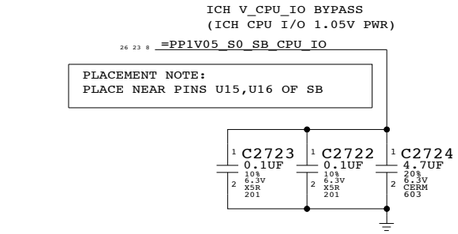


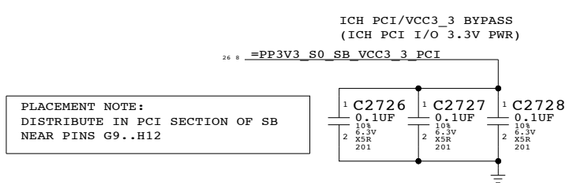


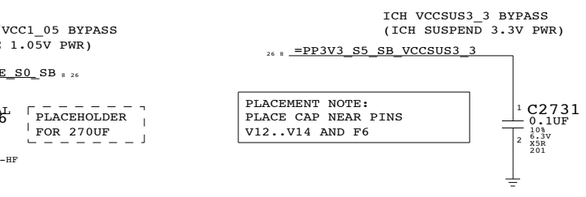


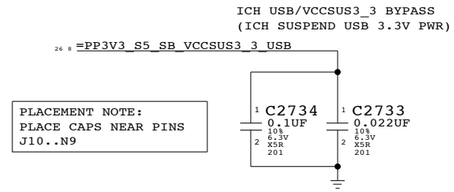


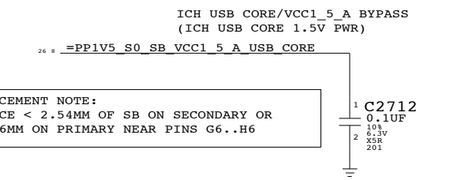




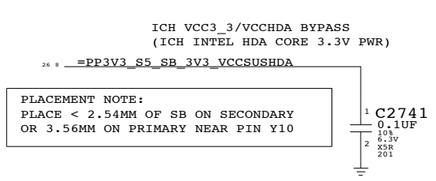








VCCCL3_3 DOES NOT REQUIRE DECOUPLING PER INTEL RECOMMENDATIONS

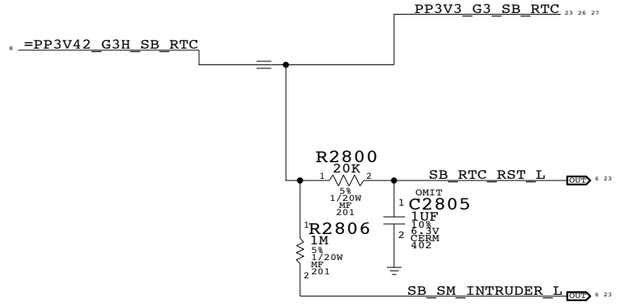


SB Decoupling

SYNC_MASTER=M70 SYNC_DATE=02/01/2007

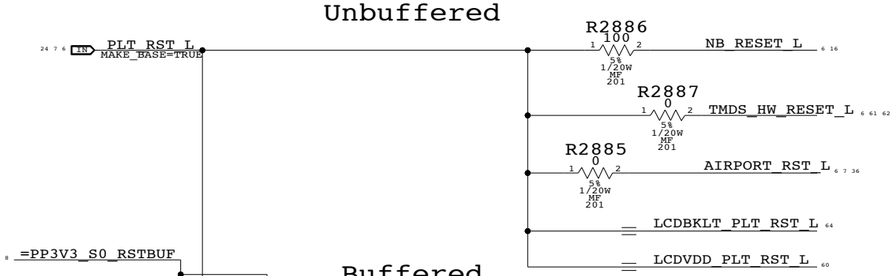
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 27 OF 109	

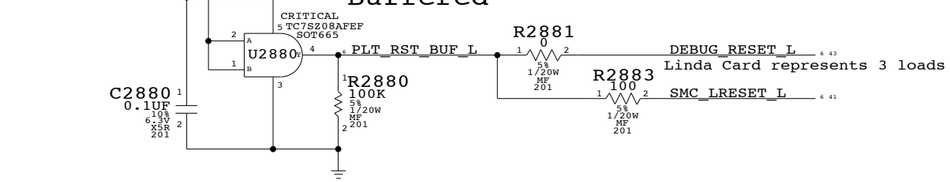


Platform Reset Connections

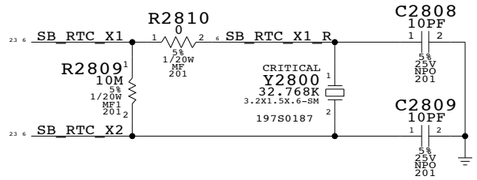
Unbuffered

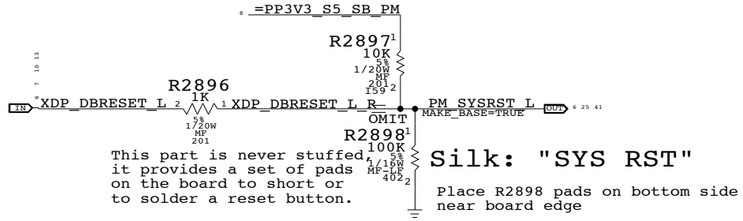


Buffered



SB RTC Crystal Circuit

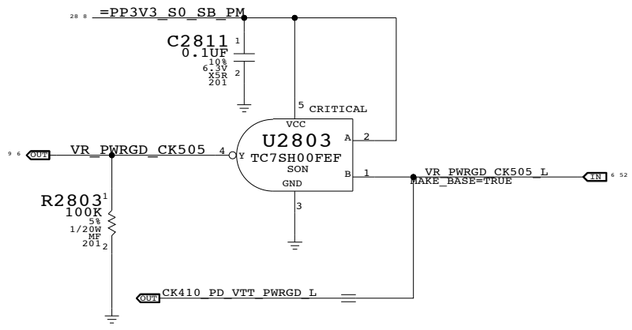


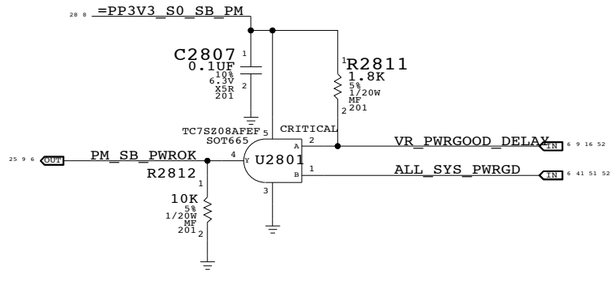


This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

Silk: "SYS RST"

Place R2898 pads on bottom side near board edge





SB Misc

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 28 OF 109	

Silego recommend to remove L2903,R2900,C2907,C2910
R2901,L2902,C2916,C2911,C2914 and R2902

=PP3V3_S0_CK505

CRITICAL
L2901
FERR-120-OHM-1.5A
0402-LF
MIN_LINE_WIDTH=0.5mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=3.3V
PP3V3_S0_CK505_VDD_CPU_SRC

OMIT C2900 1UF 10% 6.3V CERM 402
OMIT C2901 10UF 20% 6.3V X5R 603
C2902 0.1UF 10% 6.3V X5R 201
C2903 0.1UF 10% 6.3V X5R 201
C2904 0.1UF 10% 6.3V X5R 201
C2905 0.1UF 10% 6.3V X5R 201
C2906 0.1UF 10% 6.3V X5R 201
C2908 0.1UF 10% 6.3V X5R 201
C2909 0.1UF 10% 6.3V X5R 201
C2912 0.1UF 10% 6.3V X5R 201
C2913 0.1UF 10% 6.3V X5R 201
C2915 0.1UF 10% 6.3V X5R 201

CRITICAL
Y2901
SM-2.5X2.0MM
14.318MH2-35PPF-20PF
C2989 20PF 5% 25V NPO-C0G 201
C2990 20PF 5% 25V NPO-C0G 201

R2903 10K 5% 1/20W MF 201
(FW PCI 33MHZ)
(TPM LPC 33MHZ)
(SMC LPC 33MHZ)
(PCI SLOT)
(PORT80 LPC 33MHZ)
(ICH8M PCI 33MHZ)
(PULL UP PIN 68 TO ENABLE ITP HOST CLK)
(ICH SM BUS)

(EACH POWER PIN PLACED ONE 0.1UF)
(PLACED 0.1UF NEAR THE RELATIVE POWER PIN)

U2900
SLG2AP101
QFN

3	VDD_48			
43	VDD_CPU			
61	VDD_PCI			
67				
49	VDD_REF			
12	VDD_SRC			
17				
28				
35				
38	VDD_A			
39	VSS_A			
51	XTAL_IN	CK505_XTAL_IN		
50	XTAL_OUT	CK505_XTAL_OUT		
8	FS_B/TEST_MODE	CK505_FSB_TEST_MODE	IN	
57	PCI_1	TP_CK505_PCI1_CLK	OUT	
58	PCI_2	TP_CK505_PCI2_CLK	OUT	
63	PCI_3	CK505_PCI3_CLK	OUT	
64	PCI_4	TP_CK505_PCI4_CLK	OUT	
65	PCI_5/FCT_SEL	CK505_PCI5_FCTSEL1	BI	(NO INT PD)
68	PCIF_0/ITP_EN	CK505_PCIF0_CLK	OUT	(INT PU)
1	PCIF_1	CK505_PCIF1_CLK	OUT	(NO INT PU)
47	SCL	=SMBUS_CK505_SCL	IN	
48	SDA	=SMBUS_CK505_SDA	BI	
5	VSS_48			
46	VSS_CPU			
62				
66	VSS_PCI			
52	VSS_REF			
31	VSS_SRC			
69	THRM_PAD			
56	PCI_STOP*	PM_STPPCI_L	IN	(FROM ICH8M GPIO15 STPPCI*)
55	CPU_STOP*	PM_STPCPU_L	IN	(FROM ICH8M GPIO25 STPCPU*)
44	CPU_0*	CK505_CPU0_N	OUT	(CPU HOST 133/167MHZ)
45	CPU_0	CK505_CPU0_P	OUT	
41	CPU_1_MCH*	CK505_CPU1_N	OUT	(GMCH HOST 133/167MHZ)
42	CPU_1_MCH	CK505_CPU1_P	OUT	
36	CPU_ITP*/SRC_10*	CK505_CPU2_ITP_SRC10_N	OUT	(ITP HOST 133/167MHZ)
37	CPU_ITP/SRC_10	CK505_CPU2_ITP_SRC10_P	OUT	
11	SRC_0*/LCD_CLK*	CK505_LVDS_N	OUT	(GMCH D_REFSSCLKIN DISPLAY PLL B 100MHZ)
10	SRC_0/LCD_CLK	CK505_LVDS_P	OUT	
14	SRC_1*	TP_CK505_SRC1_N	OUT	(SLOT F - GPU PCI-E 100 MHZ)
13	SRC_1	TP_CK505_SRC1_P	OUT	
9	CLKREQ_1*	TP_CK505_SRC_CLKREQ1_L	IN	(INT PU)
16	SRC_2*	CK505_SRC2_N	OUT	(ICH8M DMI 100 MHZ)
15	SRC_2	CK505_SRC2_P	OUT	
19	SRC_3*	TP_CK505_SRC3_N	OUT	(SLOT D - 4 LANE PCI-E FOR EXPRESSCARD)
18	SRC_3	TP_CK505_SRC3_P	OUT	
59	CLKREQ_3*	TP_CK505_SRC_CLKREQ3_L	IN	(INT PU)
22	SRC_4*	TP_CK505_SRC4_N	OUT	(ICH SATA 100 MHZ)
21	SRC_4	TP_CK505_SRC4_P	OUT	(FROM ICH8M GPIO35)
20	CLKREQ_4*	TP_CK505_SRC_CLKREQ4_L	IN	(INT PU)
24	SRC_5*	CK505_SRC5_N	OUT	(GMCH G_CLKIN 100 MHZ)
23	SRC_5	CK505_SRC5_P	OUT	(FROM GMCH CLK_REQ*)
60	CLKREQ_5*	NB_CLKREQ_L	IN	(INT PU)
27	SRC_6*	CK505_SRC6_N	OUT	(WIRELESS PCI-E 100 MHZ)
26	SRC_6	CK505_SRC6_P	OUT	
25	CLKREQ_6*	CK505_SRC_CLKREQ6_L	IN	(INT PU)
30	SRC_7*	TP_CK505_SRC7_N	OUT	(DB400 SRC)
29	SRC_7	TP_CK505_SRC7_P	OUT	
40	CLKREQ_7*	TP_CK505_PGMODE		(INT PU)
32	SRC_8*	TP_CK505_SRC8_N	OUT	(SLOT E)
33	SRC_8	TP_CK505_SRC8_P	OUT	
34	CLKREQ_8*	TP_CK505_SRC_CLKREQ8_L	IN	(INT PU)
7	DOT_96*/27M_SS	CK505_DOT96_27M_N	OUT	(GMCH D_REFCLKIN DISPLAY PLL A 96MHZ)
6	DOT_96/27M	CK505_DOT96_27M_P	OUT	(INT PD)
2	CKPWRGD/PD*	CLK_PWRGD	IN	
4	48M/FS_A	CK505_USB48_FSA	OUT	(FROM ICH8M)
54	REF_0/FS_C/TEST_SEL	CK505_CLK14P3M_TIMER	OUT	(ICH8M USB 48MHZ)
53	GPU_STOP*	TP_GPU_STOP_L	BI	(ICH8M,SIO,LPC REF. 14.318MHZ)

FCTSEL1	PIN 6	PIN 7	PIN 10	PIN 11	
0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
1	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM

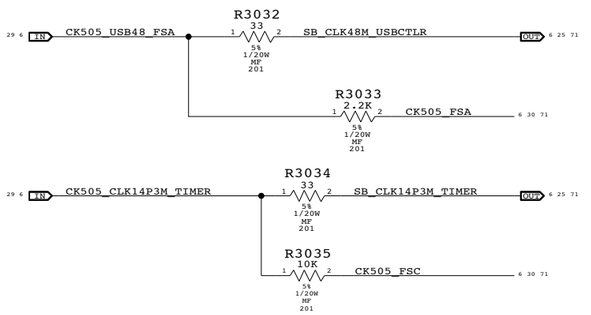
Clock (CK505)

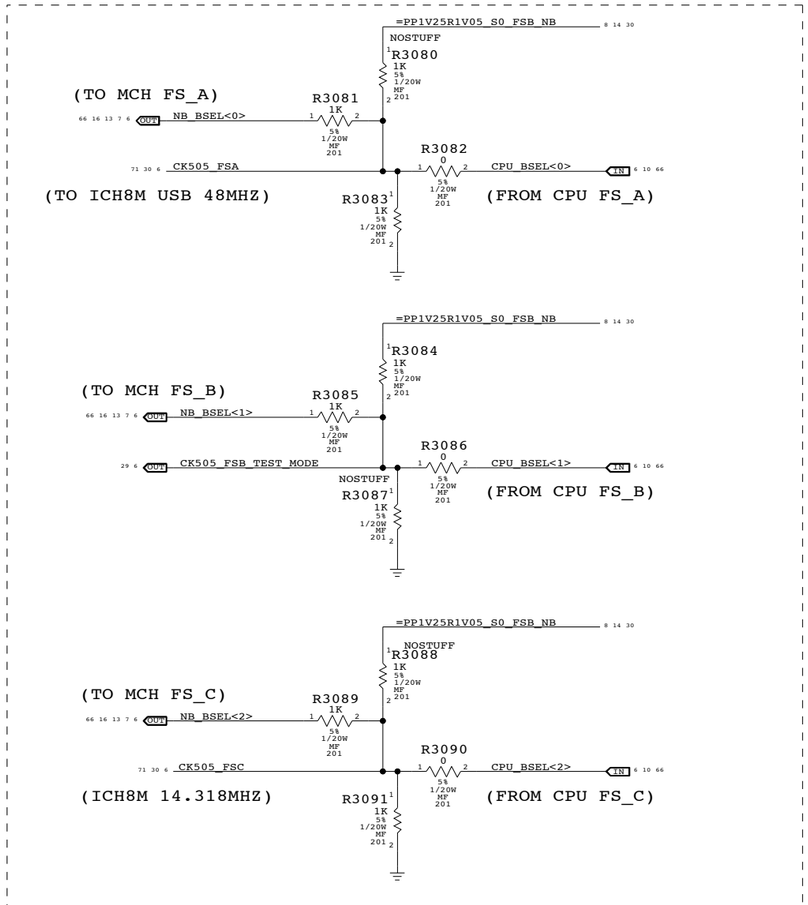
SYNC_MASTER=M70 SYNC_DATE=02/01/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J

SCALE	SHT	OF
NONE	29	109



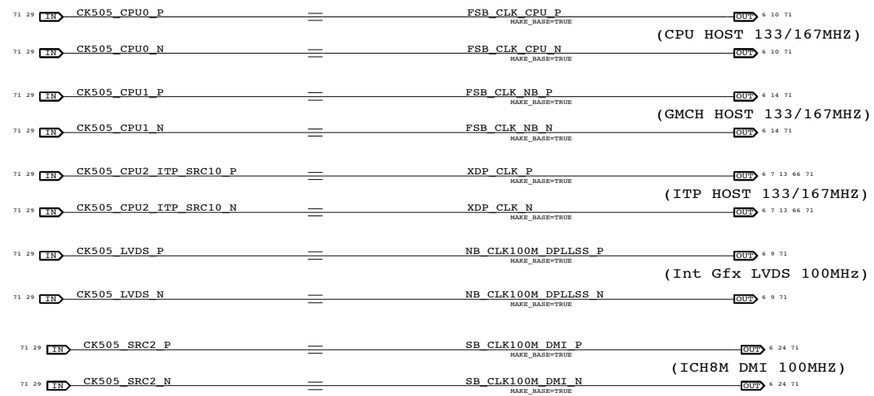


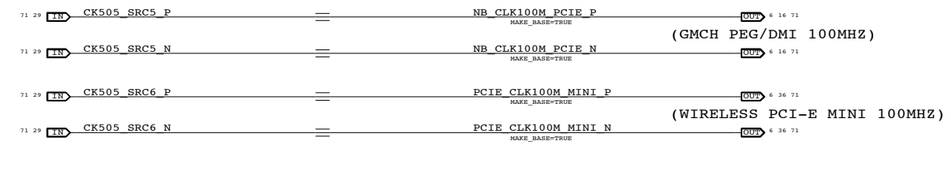
	FS_C	FS_B	FS_A	CPU
	0	0	0	266M
	0	0	1	133M
	0	1	1	166M
*	0	1	0	200M
	1	1	0	400M
	1	1	1	Resrvd
	1	0	1	100M
	1	0	0	333M

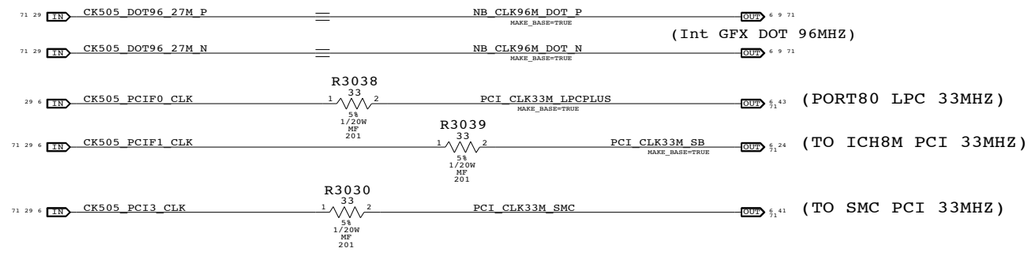
NOSTUFF R3082, R3086, R3090
FOR MANUAL CPU FREQUENCY

CPU speed is currently set to 200MHz

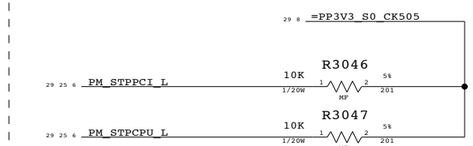
CLK Termination

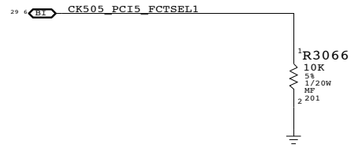






CLKREQ Controls



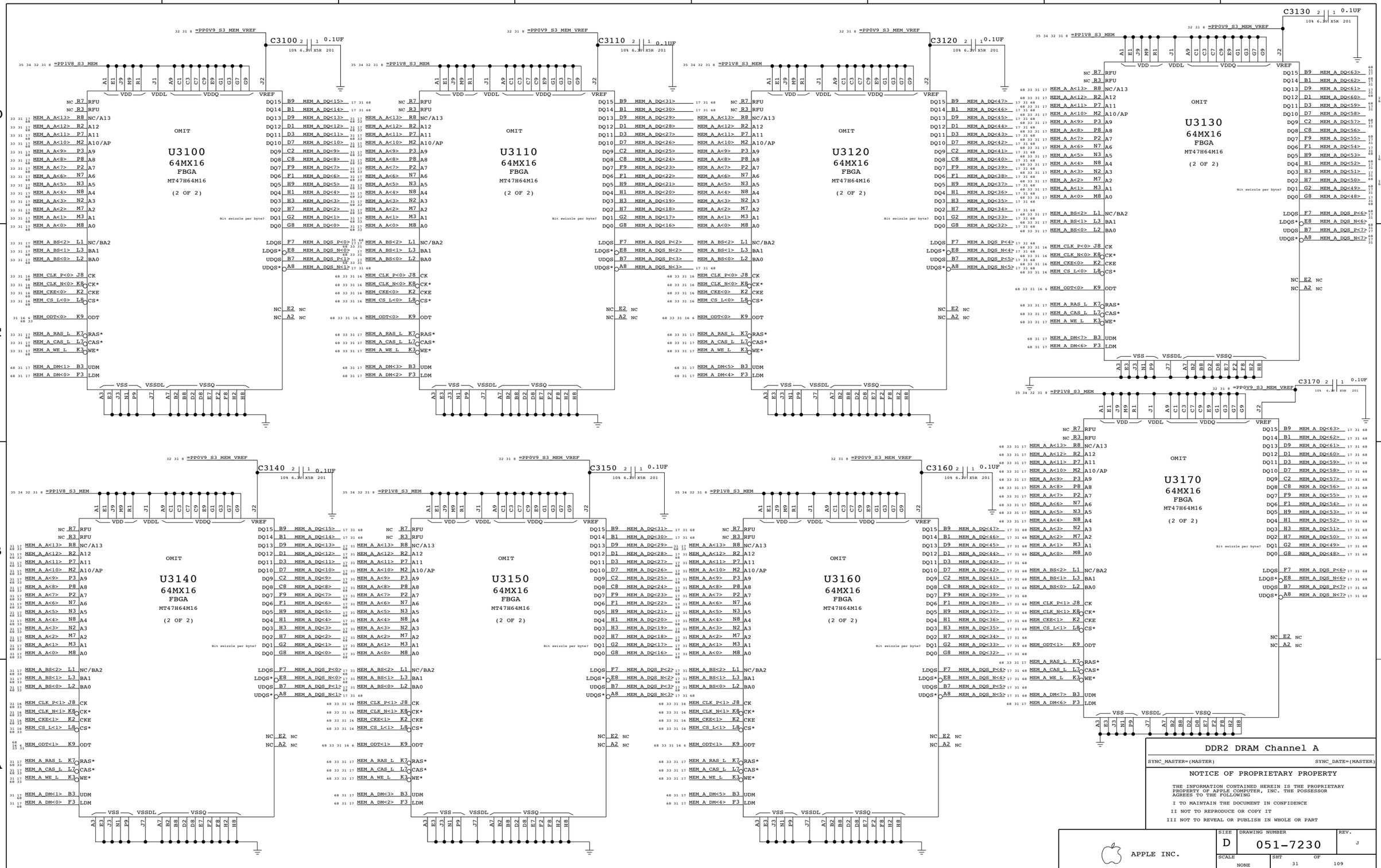


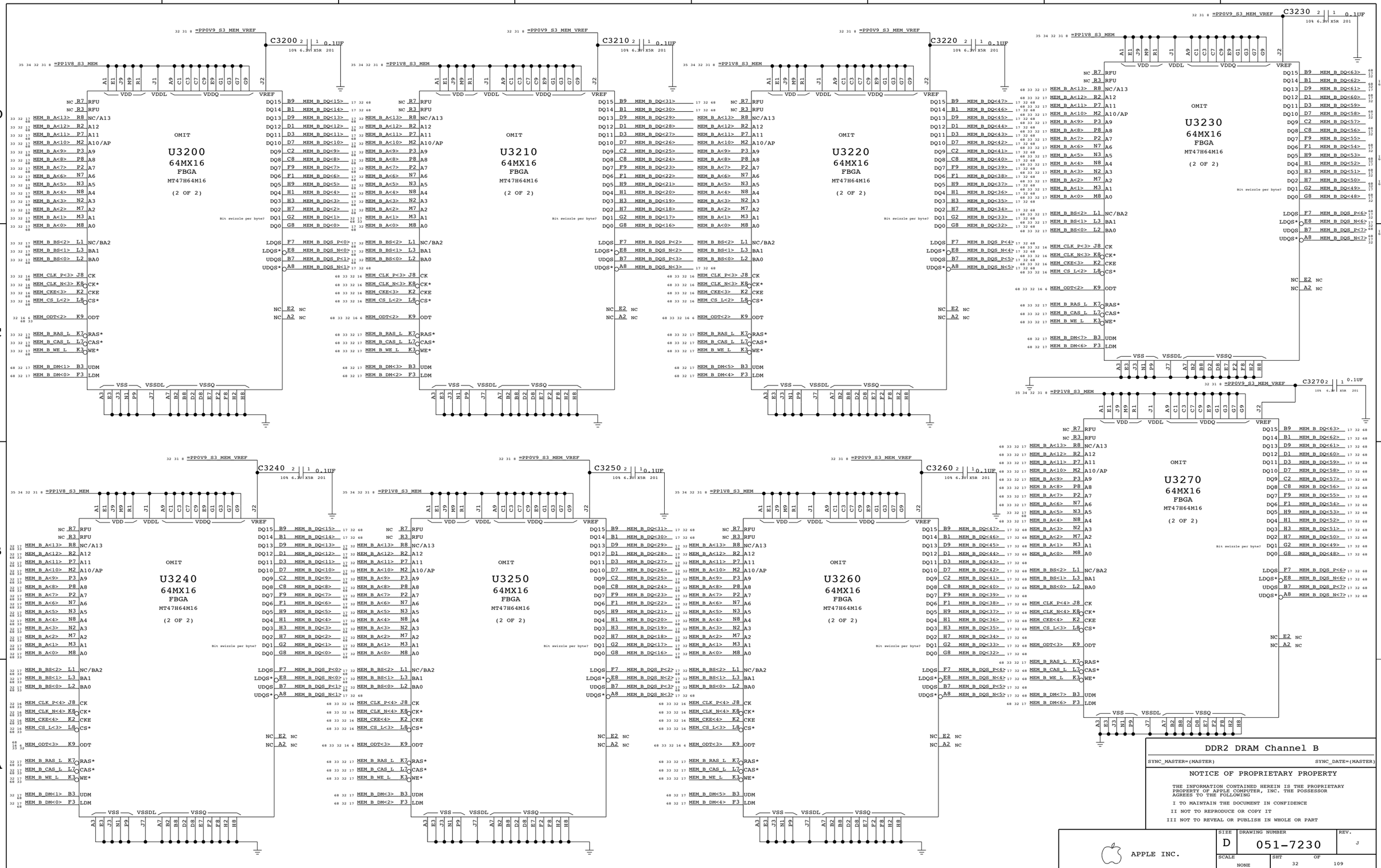
Clock Termination

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 30 OF 109	





DDR2 DRAM Channel B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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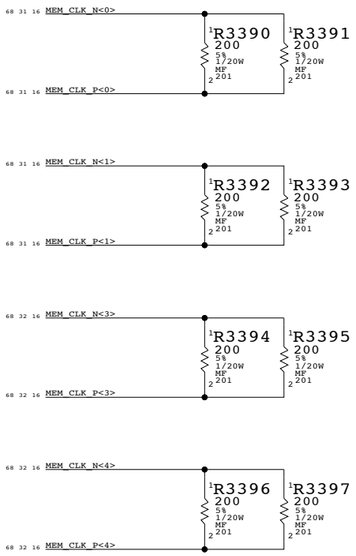
APPLE INC.

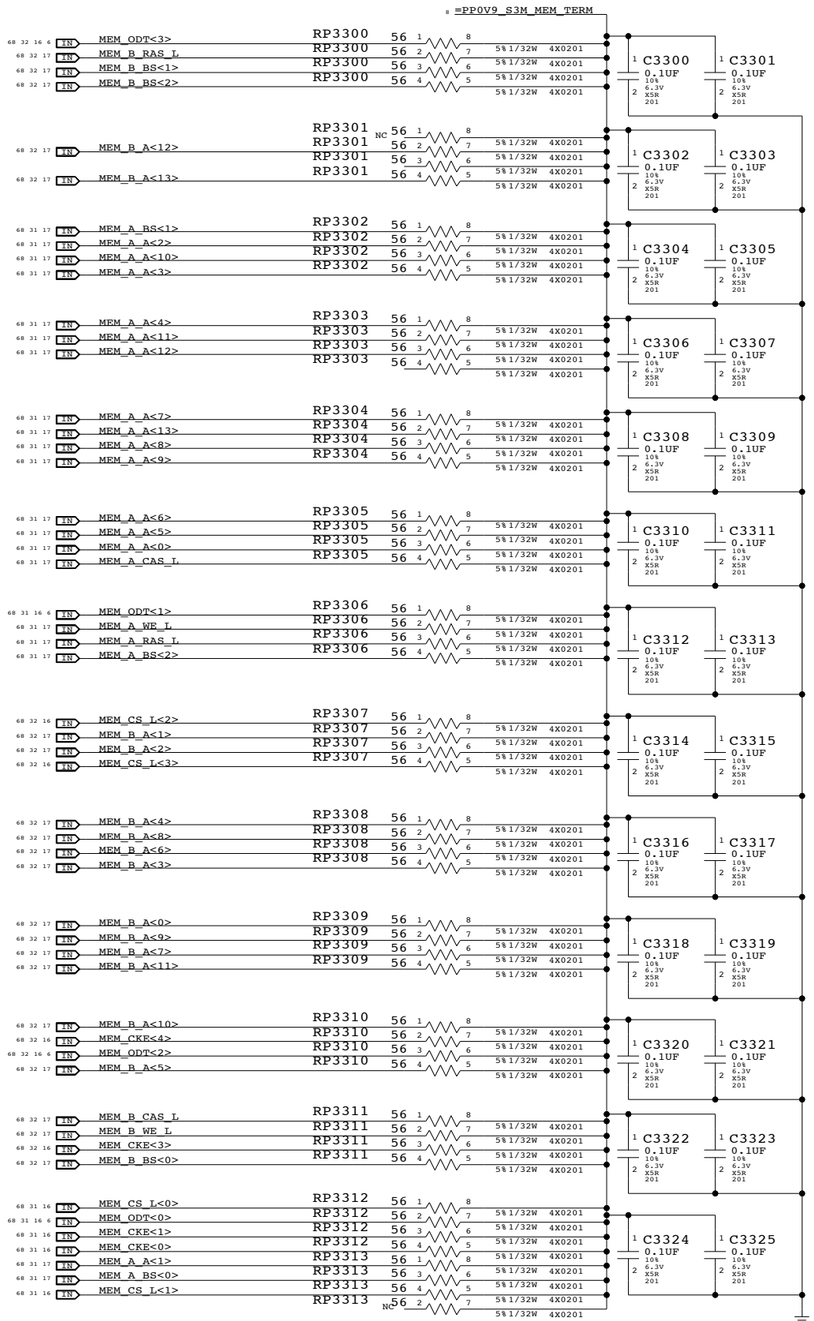
SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 32 OF 109	

MEM CLOCK TERMINATION

Place one resistor at each end of Y split



One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it

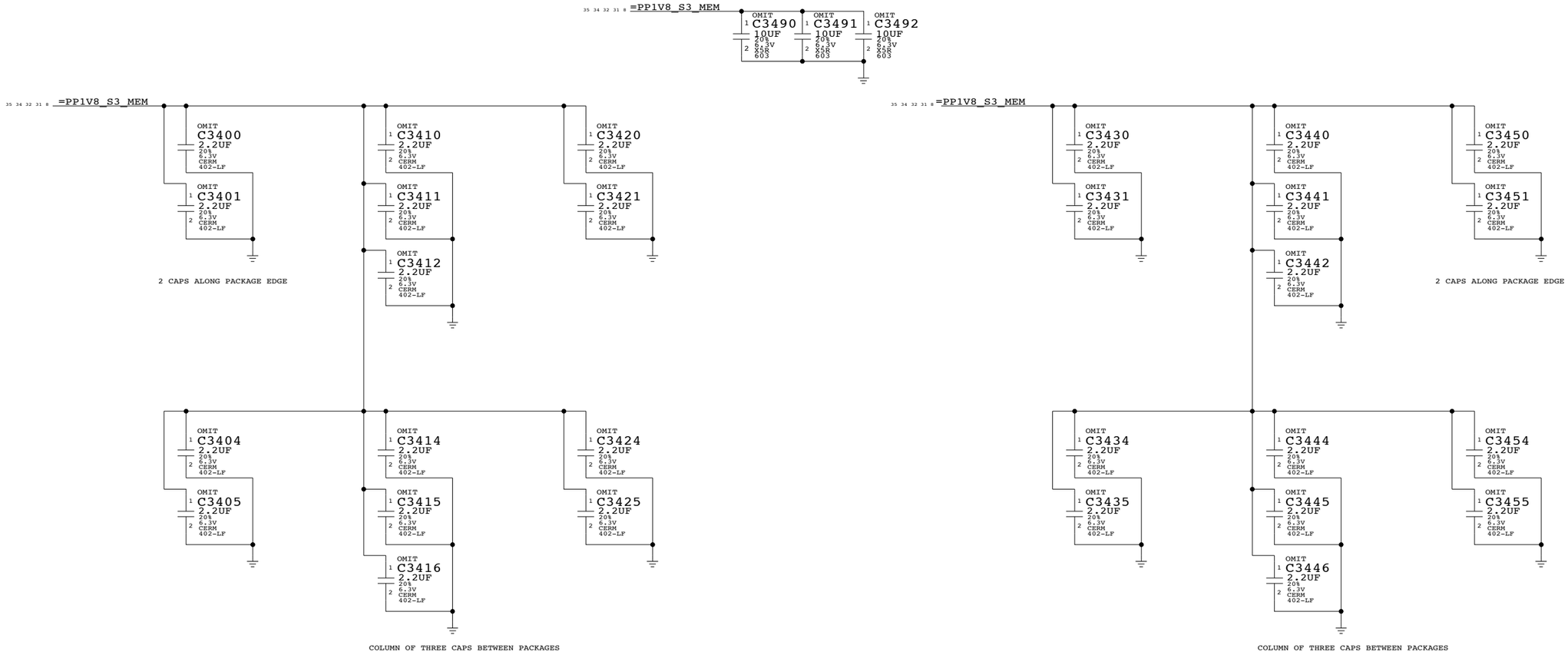


LAYOUT NOTE:PLACE ONE CAP CLOSE TO EVERY TWO PULLUP RESISTORS TERMINATED TO PP0V9_S0_MEM_TERM

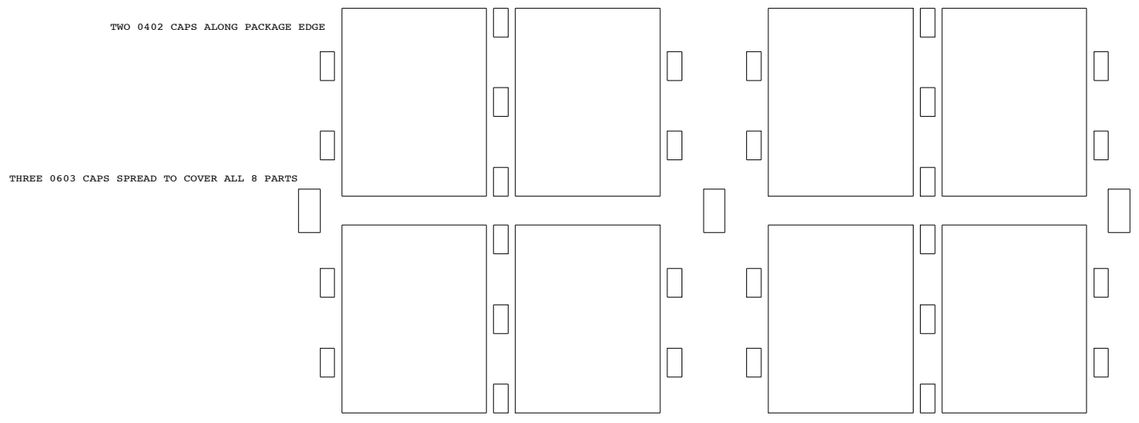
Memory Active Termination

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 33 OF 109	



APPROXIMATE CAP ARRANGEMENT



COLUMN OF THREE 0402 CAPS BETWEEN PACKAGES

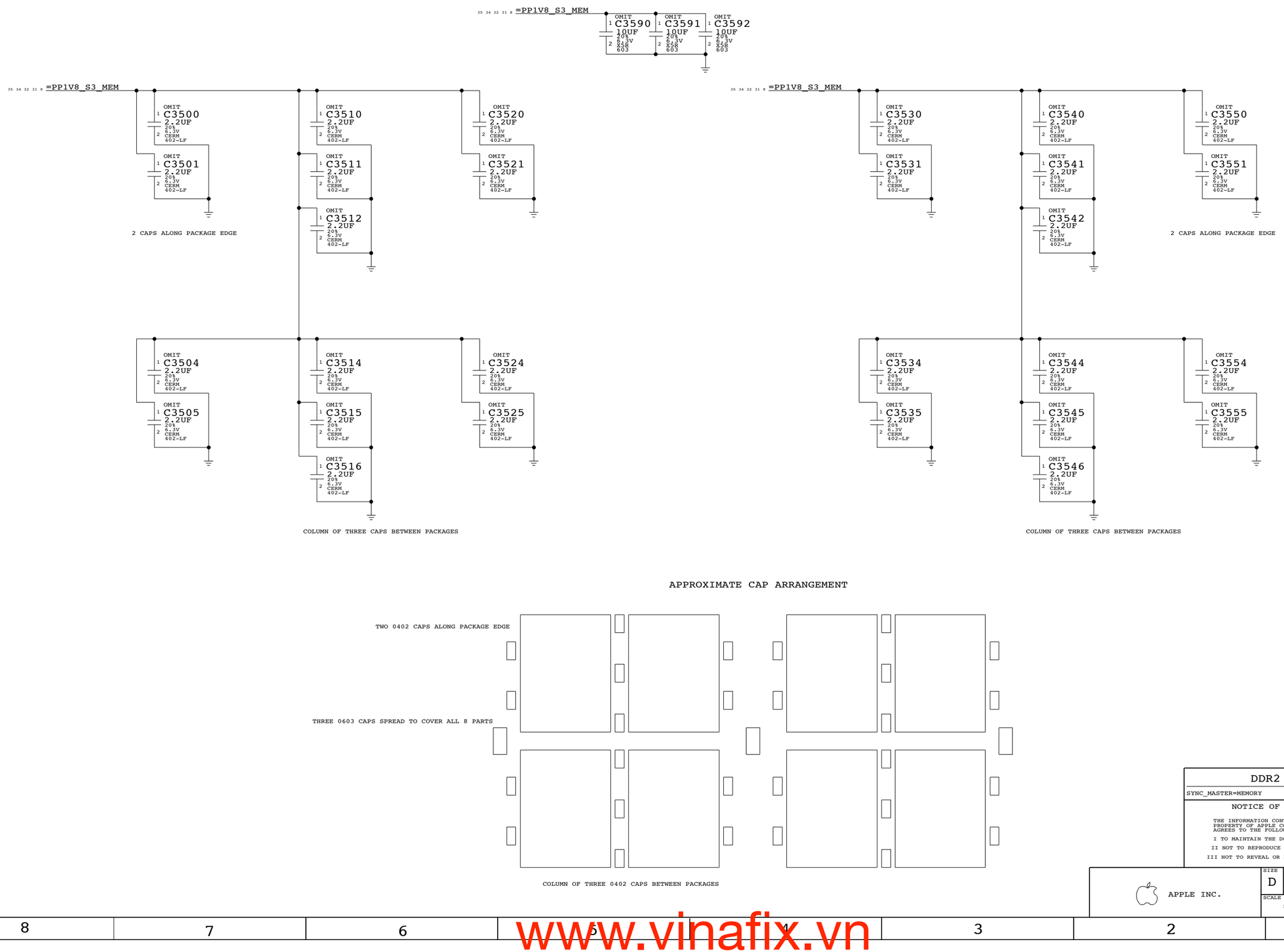
DDR2 BYPASSING 1

SYNC_MASTER=MEMORY SYNC_DATE=06/20/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J

SCALE	SHT	OF
NONE	34	109



DDR2 BYPASSING 2

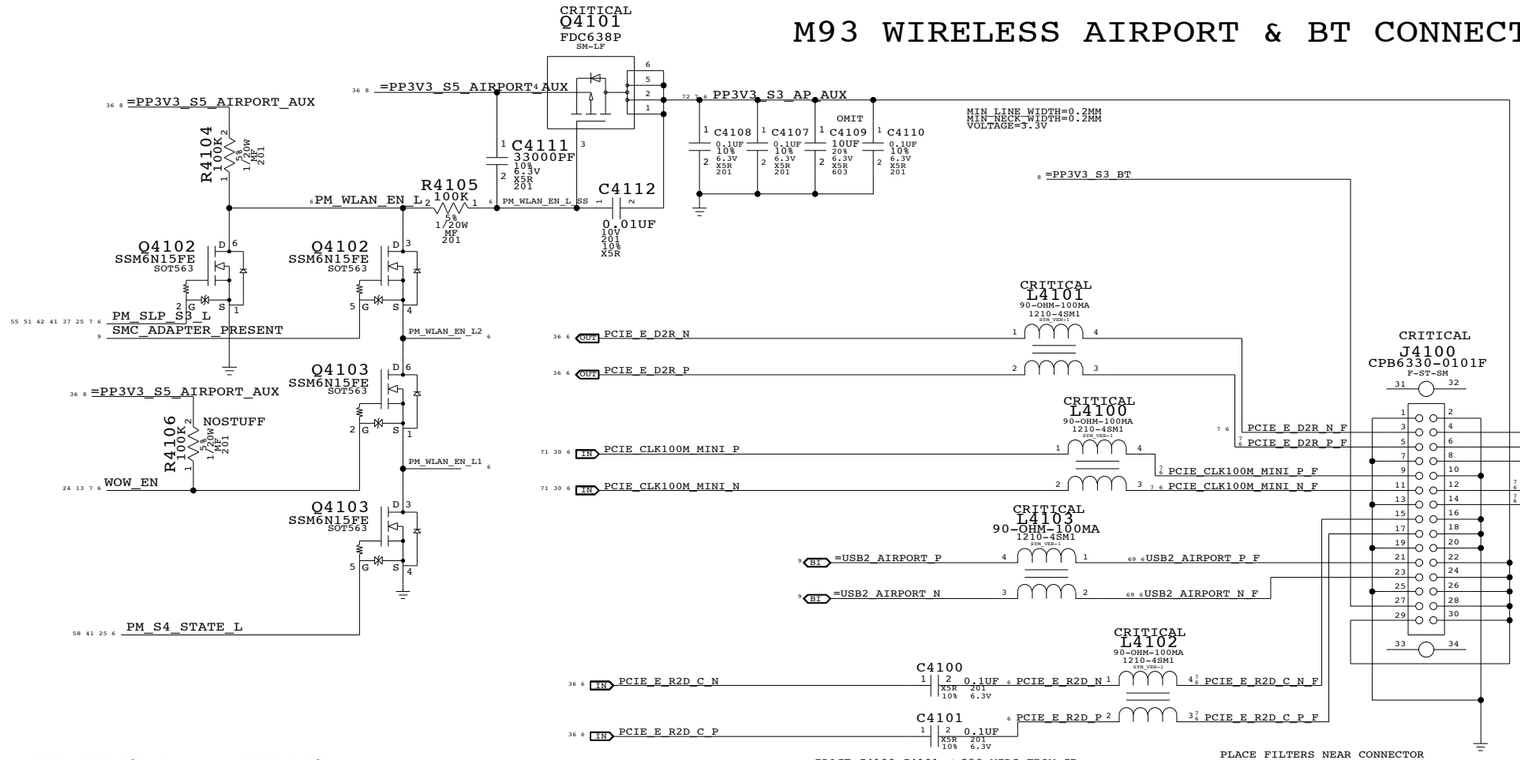
SYNC_MASTER=MEMORY SYNC_DATE=06/20/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J

SCALE	SHT	OF
NONE	35	109

M93 WIRELESS AIRPORT & BT CONNECTOR



APN:516S0580

Wireless M93 Connector

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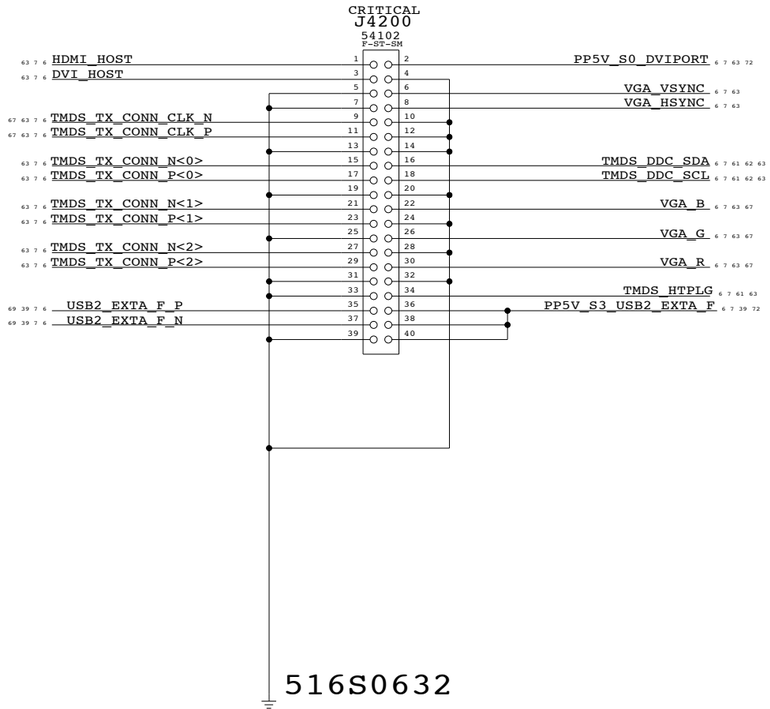
APPLE INC.

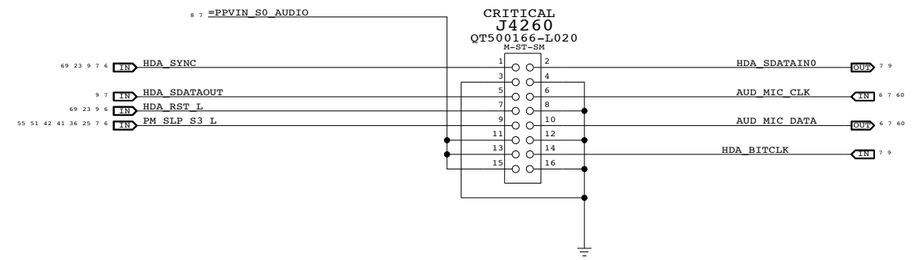
SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 41 OF 109	

Micro DVI, USB, to RIO Hatch Assembly



516S0632

Audio Connector



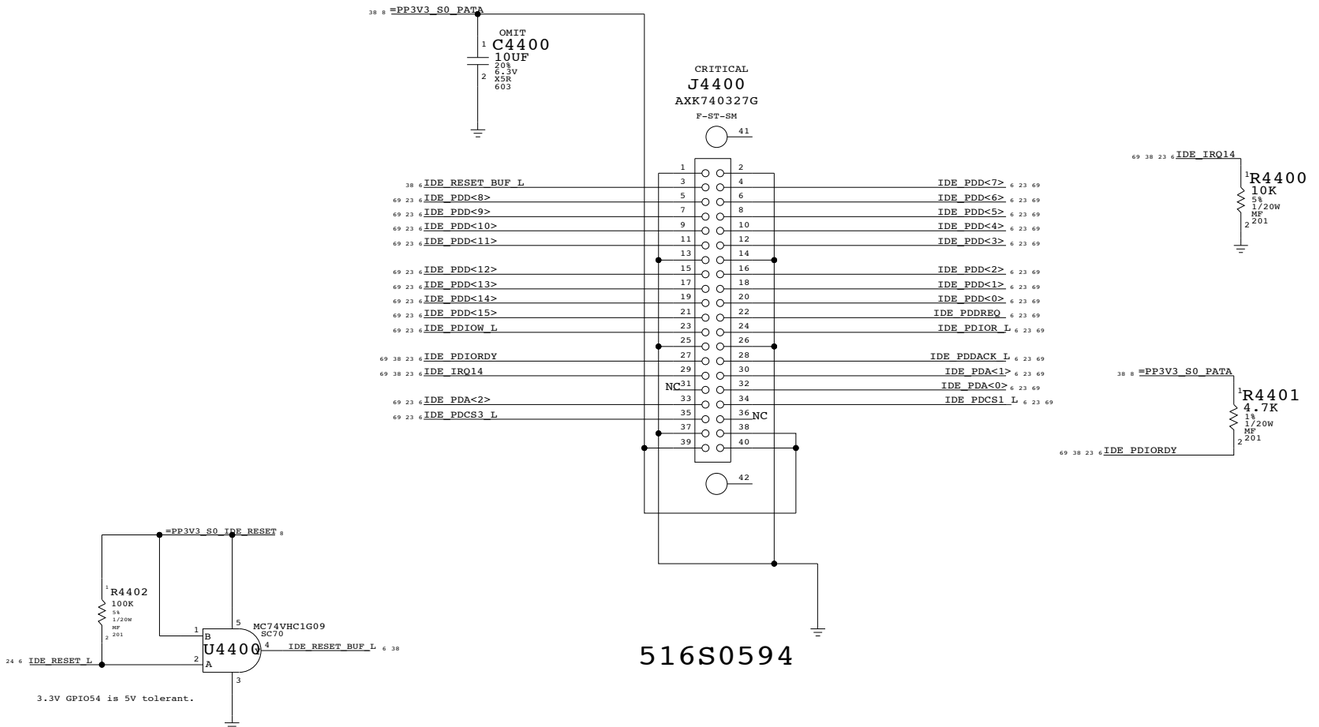
516S0350

Hatch and Audio Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE	SHT	OF
NONE	42	109



PATA HDD CONNECTOR

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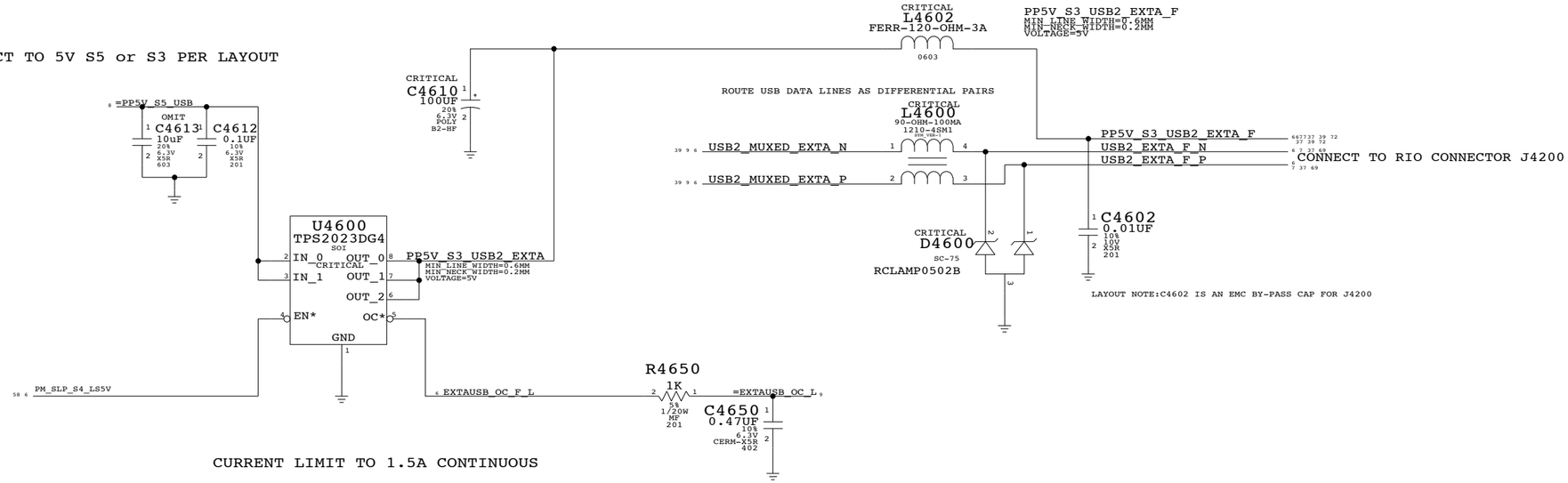
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 44 OF 109	

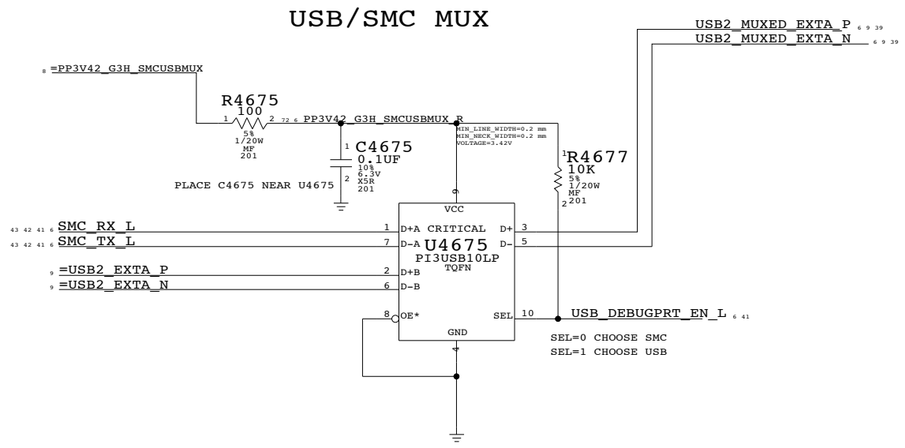
USB 2.0 CONNECTOR

CONNECT TO 5V S5 or S3 PER LAYOUT



CURRENT LIMIT TO 1.5A CONTINUOUS

USB/SMC MUX



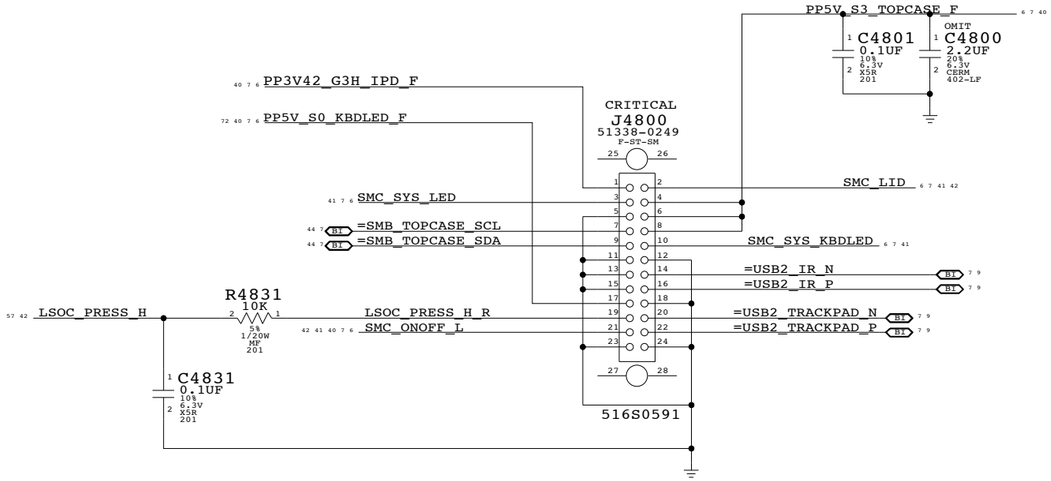
USB EXTERNAL CONNECTORS

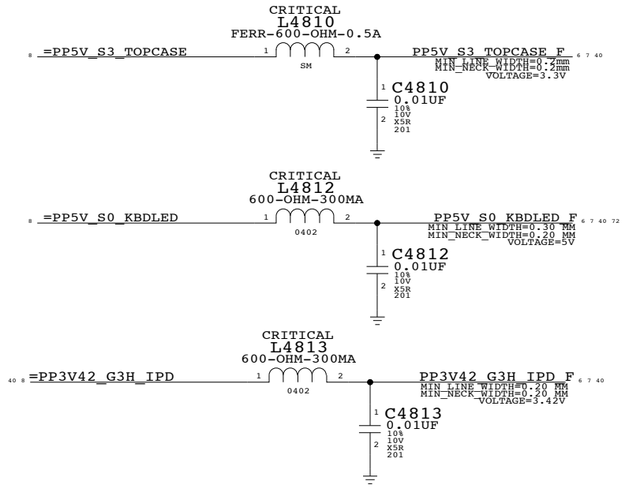
SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

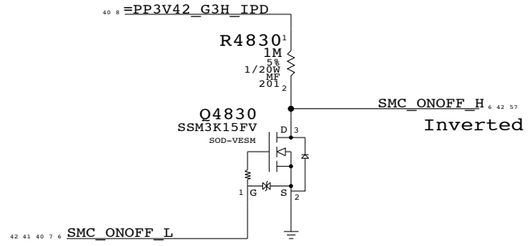
SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 46 OF 109	

IPD Connector





Power Button Inverter



Inverted to drive SMC_RESET logic

IPD Connector

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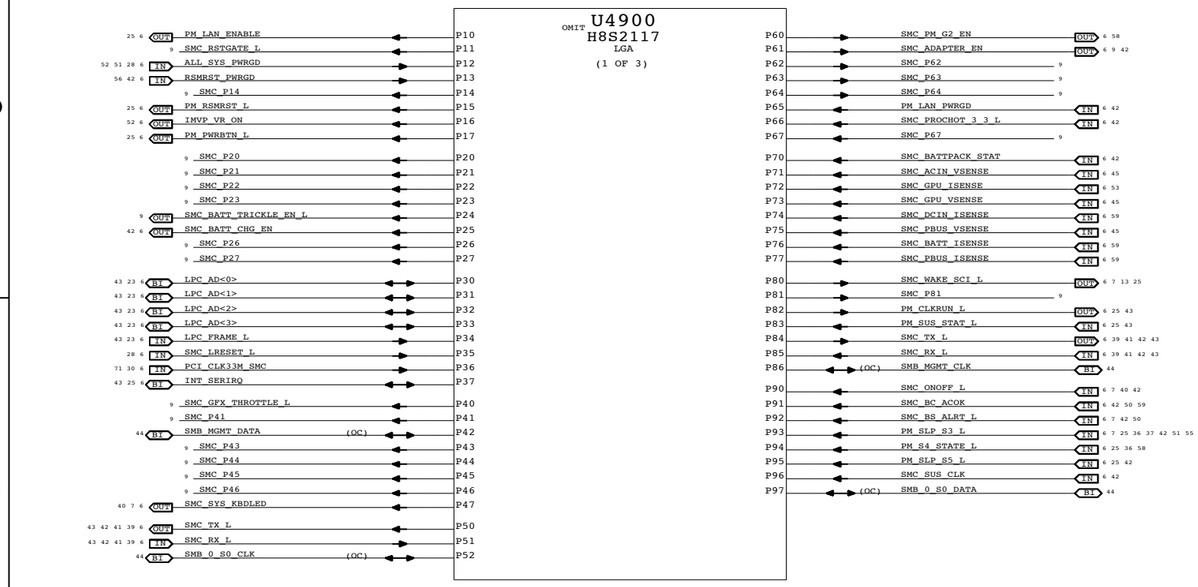
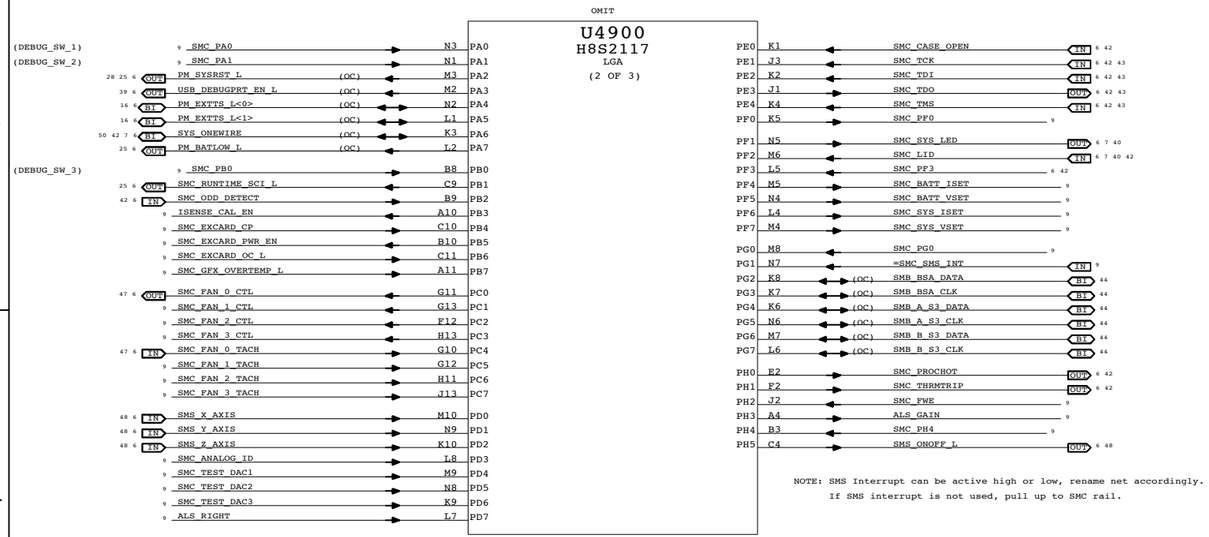
SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE	SHT	OF
NONE	48	109

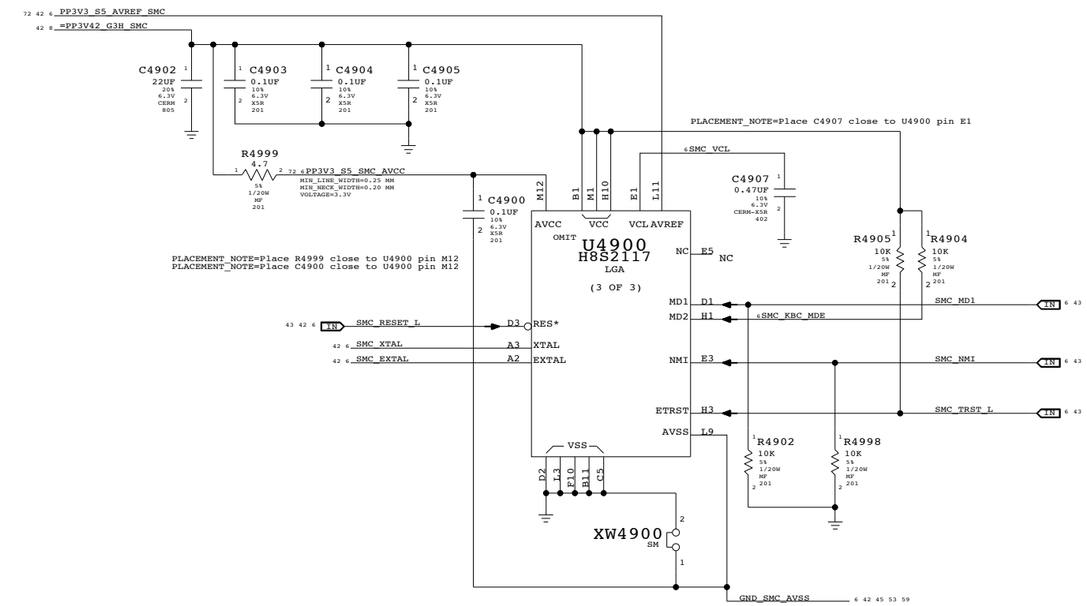
SMC

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





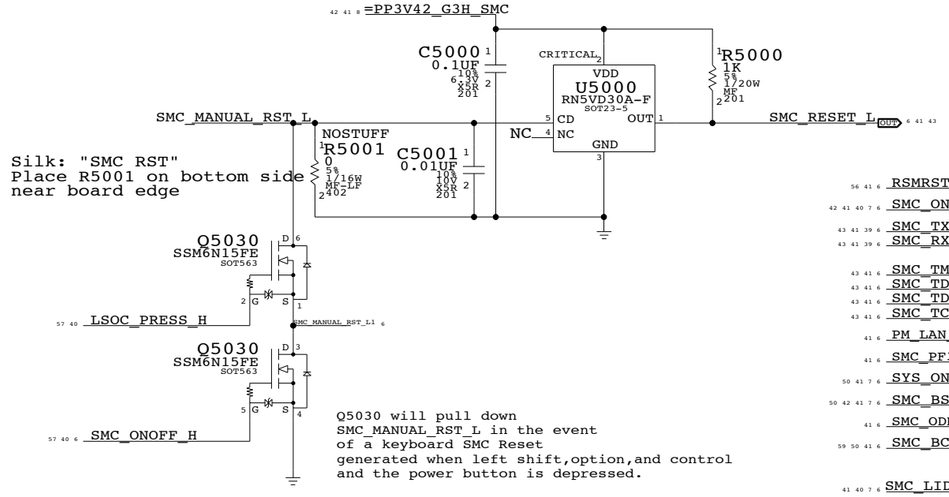
NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.



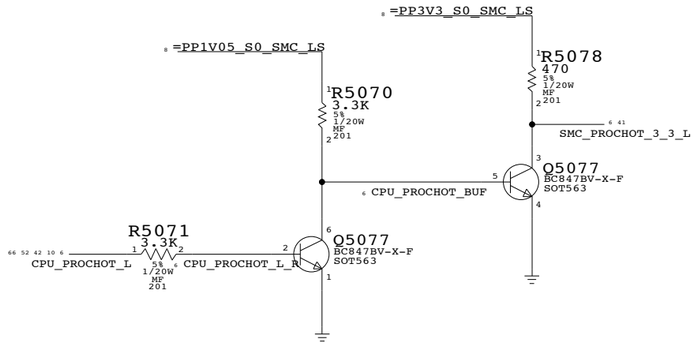
SMC	
SYNC_MASTER=M70	SYNC_DATE=01/09/2007

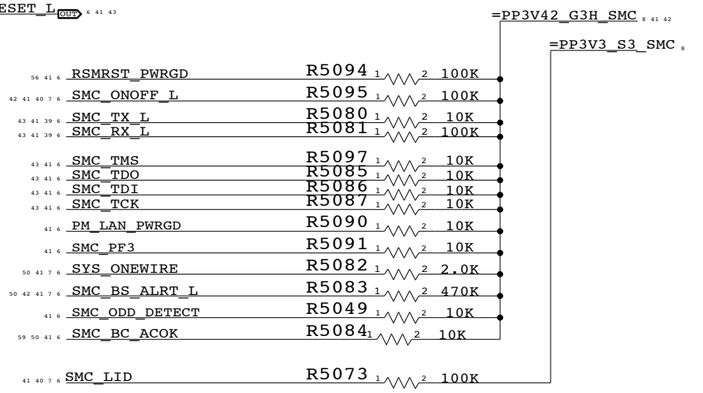
APPLE INC.	SIZE D	DRAWING NUMBER 051-7230	REV. J
	SCALE NONE	SHT 49	OF 109

SMC Reset Button / Brownout Detect

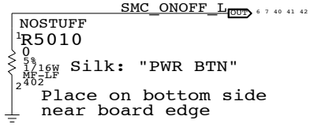


SMC 1.05V to 3.3V Level Shifting

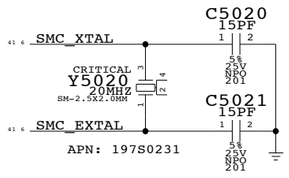




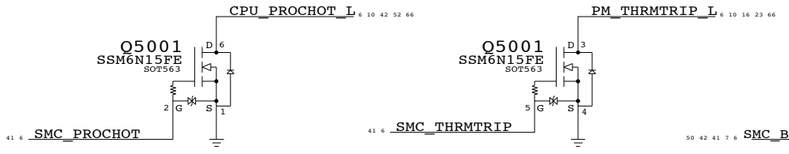
Debug Power Button



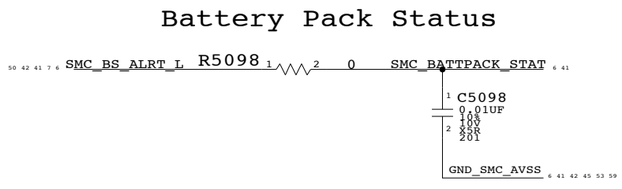
SMC Crystal Circuit



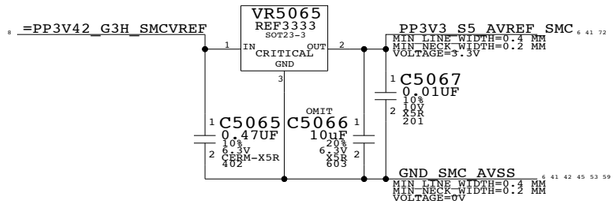
SMC 3.3V to 1.05V Level Shifting

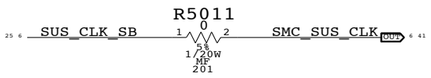


Battery Pack Status



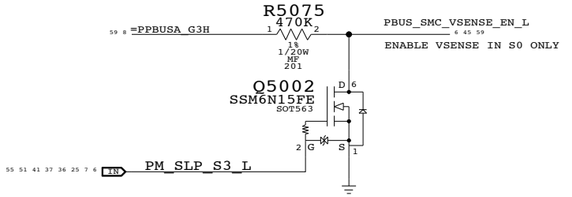
SMC AVREF Supply





R5011 CLOSE TO SB

3.3V TO PBUS LEVEL SHIFTING



SMC SUPPORT

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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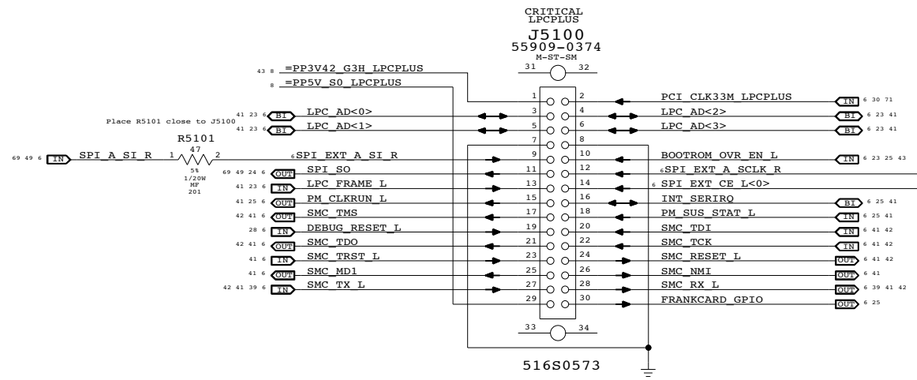
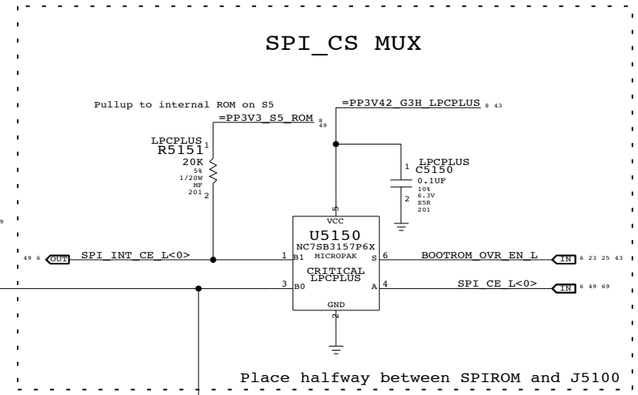
SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 50 OF 109	

LPC+SPI Connector



SPI_CS MUX



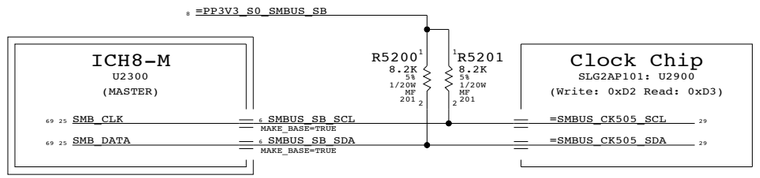
LPC+SPI Debug Connector

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

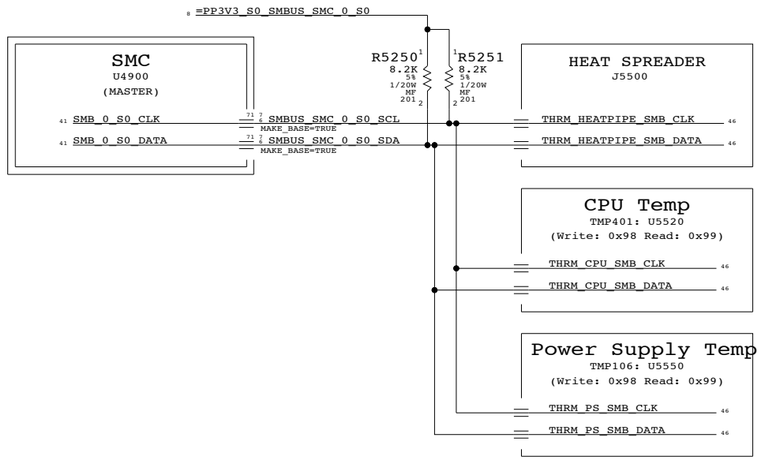
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 51 OF 109	

ICH8-M SMBus Connections

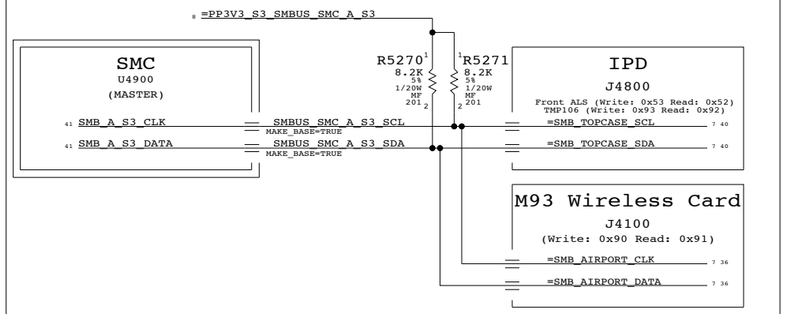


SMC "0" SMBus Connections

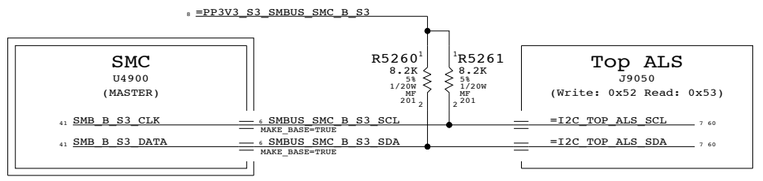


SMC "A" SMBus Connections

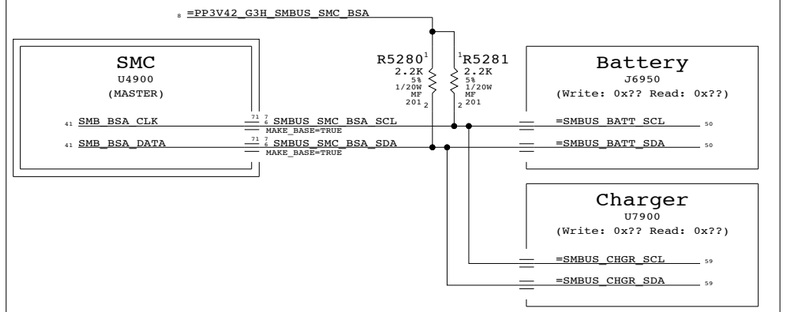
NOTE: SMC RMT bus remains powered and may be active in S3 state



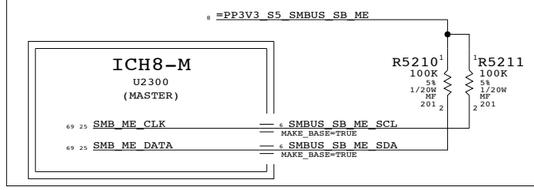
SMC "B" SMBus Connections



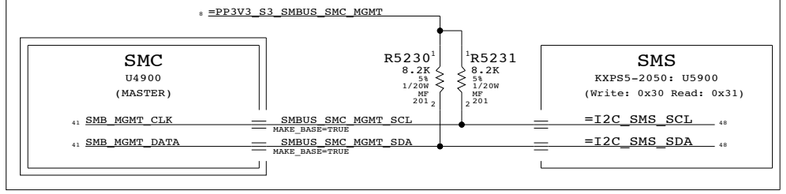
SMC "Battery A" SMBus Connections



ICH8-M ME SMBus Connections



SMC "Management" SMBus Connections



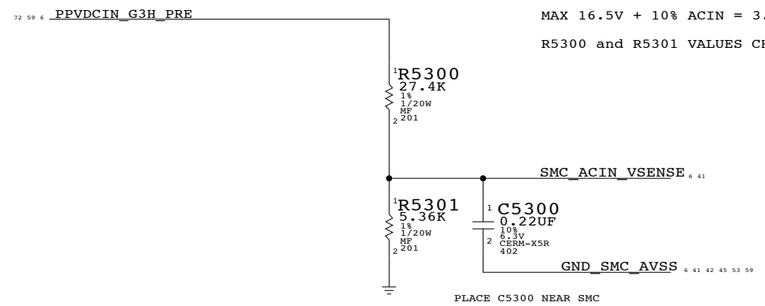
SMBUS CONNECTIONS

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 52 OF 109	

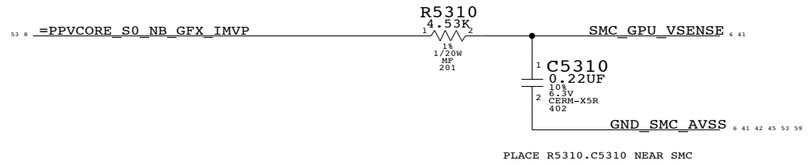
ACIN VOLTAGE SENSE



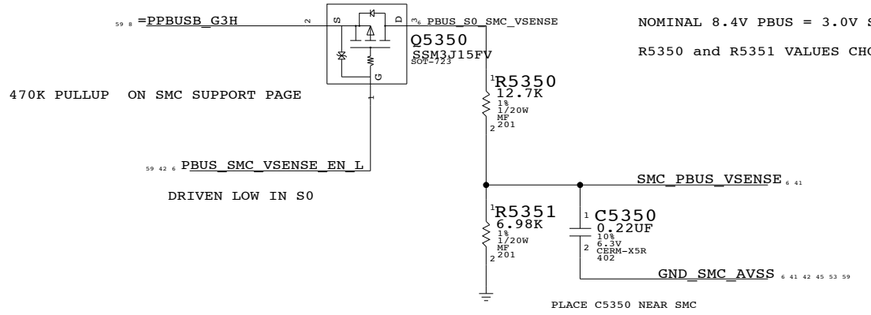
MAX 16.5V + 10% ACIN = 3.0V SMC_PBUS_VSENSE

R5300 and R5301 VALUES CHOSEN FOR RC FILTER @ 4.53KOHM THEVENIN RESISTANCE

GPU VOLTAGE SENSE



PBUS VOLTAGE SENSE



NOMINAL 8.4V PBUS = 3.0V SMC_PBUS_VSENSE

R5350 and R5351 VALUES CHOSEN FOR RC FILTER @ 4.53KOHM THEVENIN RESISTANCE

Voltage Sensors

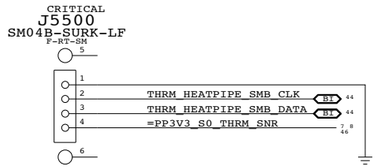
SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J

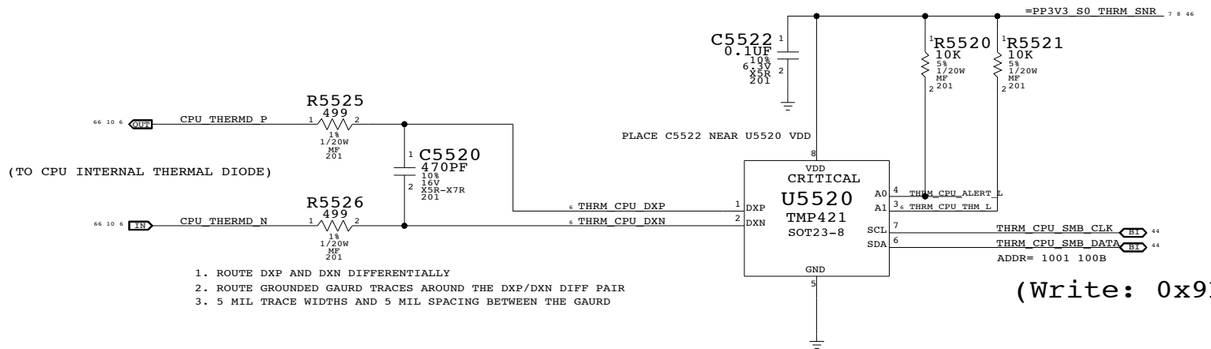
SCALE	SHT	OF
NONE	53	109

REMOTE TEMP AT HEAT SPREADER



APN:518S0354

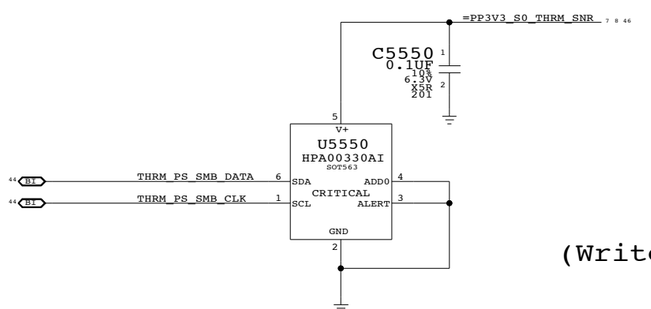
CPU THERMAL DIODE



1. ROUTE DXP AND DXN DIFFERENTIALLY
2. ROUTE GROUNDED GAURD TRACES AROUND THE DXP/DXN DIFF PAIR
3. 5 MIL TRACE WIDTHS AND 5 MIL SPACING BETWEEN THE GAURD

(Write: 0x9E Read: 0x9F)

LOCAL TEMP NEAR POWER SUPPLIES



(Write: 0x90 Read: 0x91)

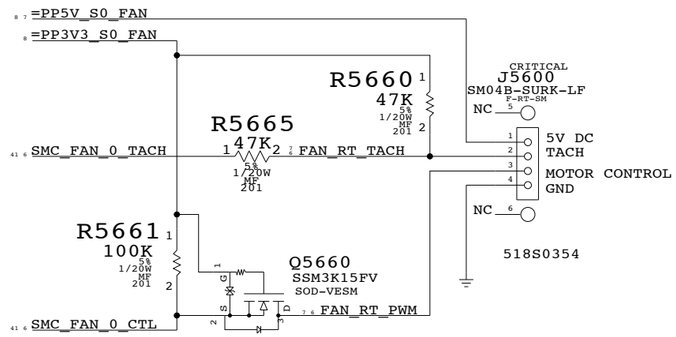
TEMPERATURE SENSORS

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 55 OF 109	

FAN CONNECTOR



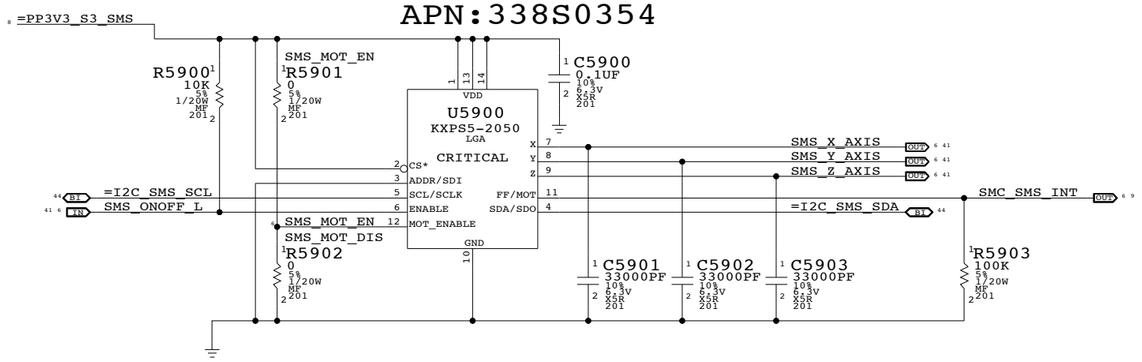
Fan	
SYNC_MASTER=M70	SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 56 OF 109	

SUDDEN MOTION SENSOR

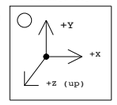
APN:338S0354



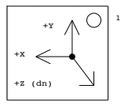
I2C addresses:

ADDR low => 0x30, 0x31
ADDR high => 0x32, 0x33
Alias SCL/SDA to GND if using analog outputs only

Desired orientation when placed on board top-side:



Desired orientation when placed on board bottom-side:



Sudden Motion Sensor (SMS)

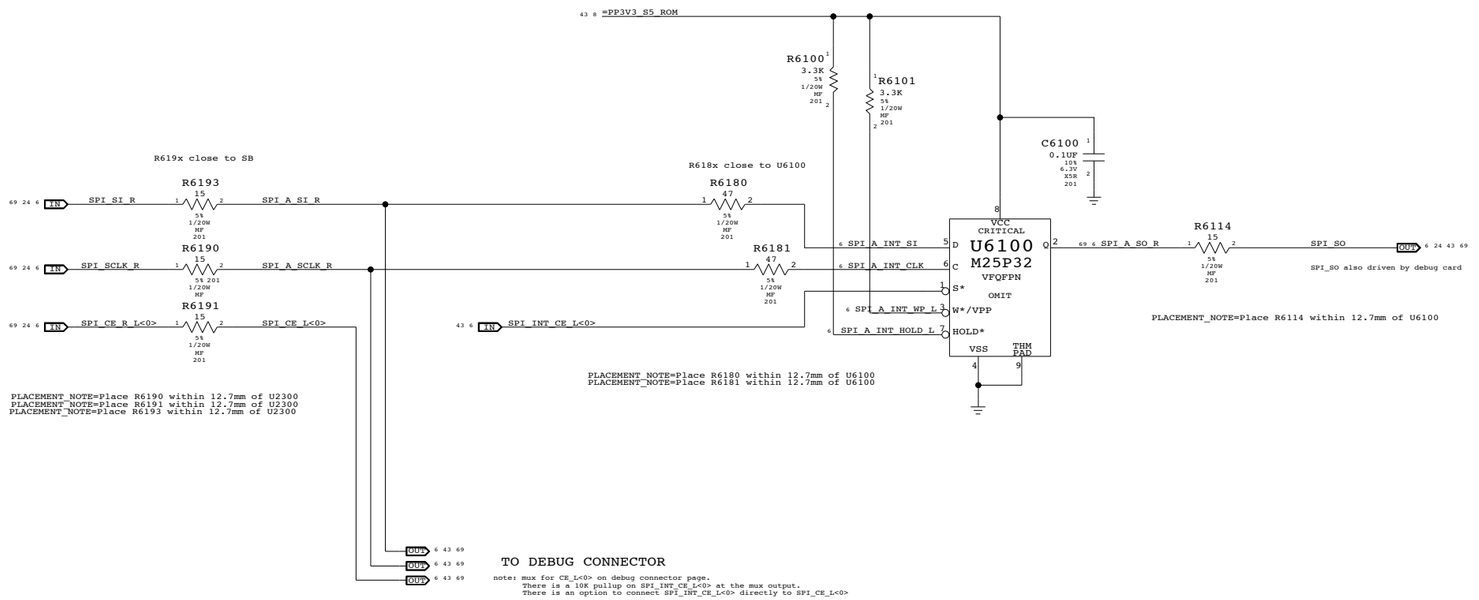
SYNC_MASTER=M76_MLB SYNC_DATE=01/12/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J

SCALE NONE SHT 59 OF 109

SPI ROM



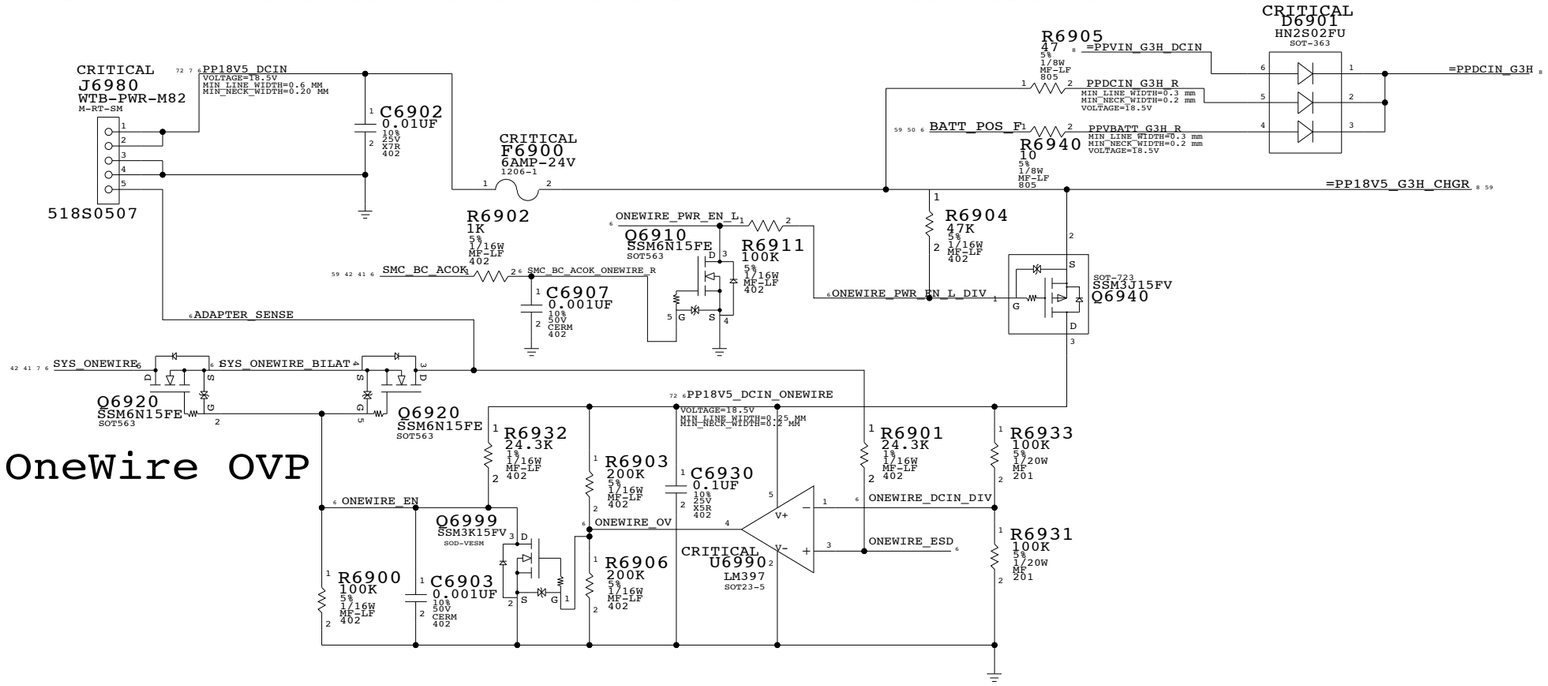
SPI ROMs

SYNC_MASTER=WFERRY SYNC_DATE=04/26/2006

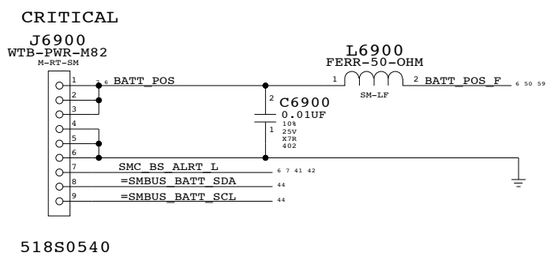
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 61 OF 109	

DC-JACK INTERFACE



BATTERY INTERFACE



DC-In & Battery Connectors

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 69 OF 109	

S0 FETS & POWER SEQUENCING & PGOOD

5V S0 FET

MOSFET	FDM6296
CHANNEL	N-TYPE
RDS(ON)	15 mOhm @4.5V
LOADING	4.061 A

3.3V S0 FET

MOSFET	FDC655BN
CHANNEL	N-TYPE
RDS(ON)	33 mOhm @4.5V
LOADING	1.063 A

3.3V S0 FET

MOSFET	FDC655BN
CHANNEL	N-TYPE
RDS(ON)	33 mOhm @4.5V
LOADING	.776 A

1.8V S0 FET

MOSFET	FDC655BN
CHANNEL	N-TYPE
RDS(ON)	33 mOhm @4.5V
LOADING	1.120 A

1.05V S0 RUN/SS CONTROL

1.25V S0 RUN/SS CONTROL

1.5V S0 RUN/SS CONTROL

DEASSERTED 160MS
AFTER UVLO_D VALID

~26MS

U7002.3 has int 90K pull-up

STUFF R7013,R7014 and UNSTUFF U7002,C7001,C7002
TO USE WIRE-AND OF ALL PGOODs INSTEAD OF TPS3808

S0 FETS & Power Sequencing

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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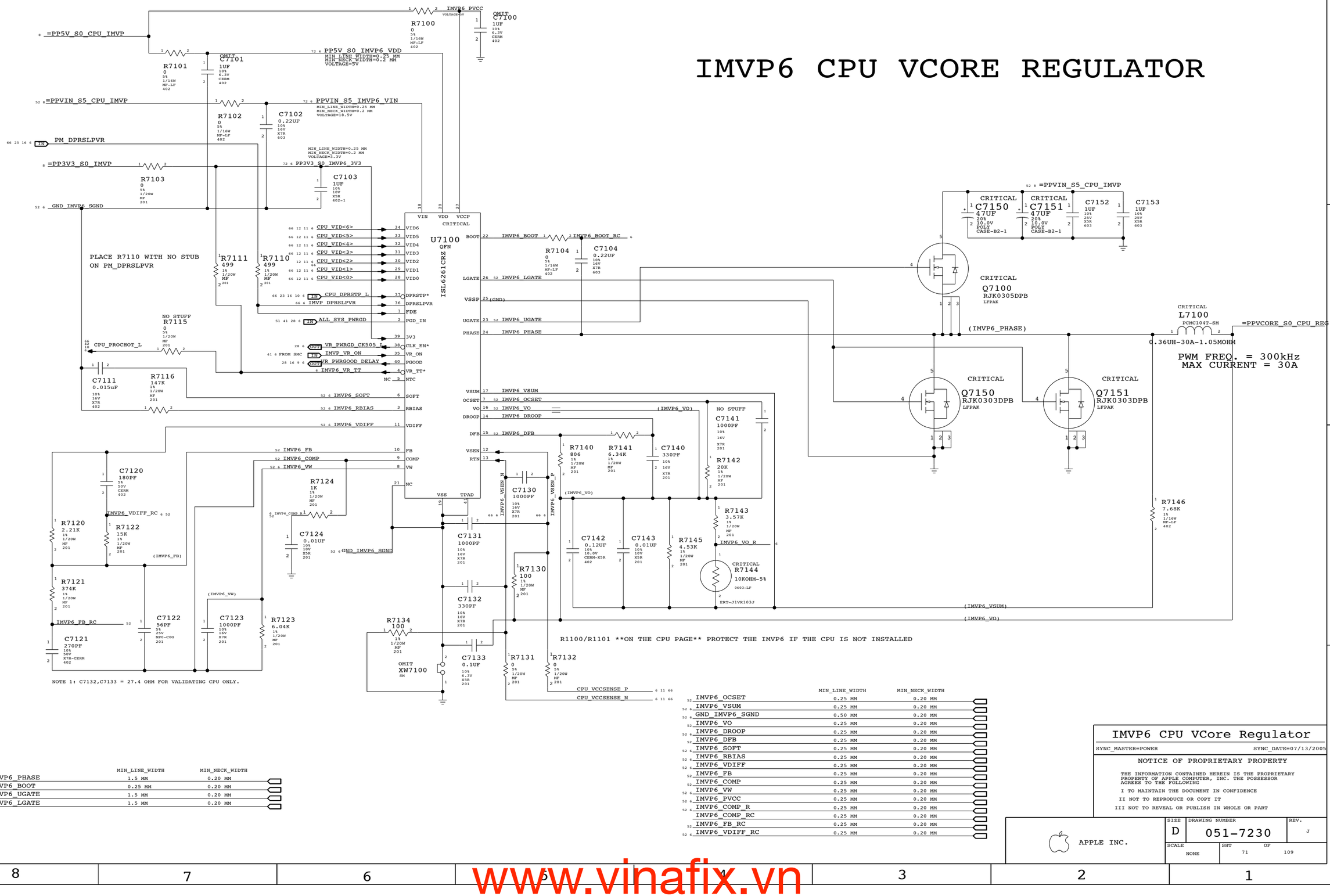
SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 70 OF 109	

IMVP6 CPU VCORE REGULATOR



NOTE 1: C7132,C7133 = 27.4 OHM FOR VALIDATING CPU ONLY.

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE	1.5 MM	0.20 MM
IMVP6_BOOT	0.25 MM	0.20 MM
IMVP6_UGATE	1.5 MM	0.20 MM
IMVP6_LGATE	1.5 MM	0.20 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.20 MM
IMVP6_PVCC	0.25 MM	0.20 MM
IMVP6_COMP_R	0.25 MM	0.20 MM
IMVP6_COMP_RC	0.25 MM	0.20 MM
IMVP6_FB_RC	0.25 MM	0.20 MM
IMVP6_VDIFF_RC	0.25 MM	0.20 MM

IMVP6 CPU VCore Regulator

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

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APPLE INC.

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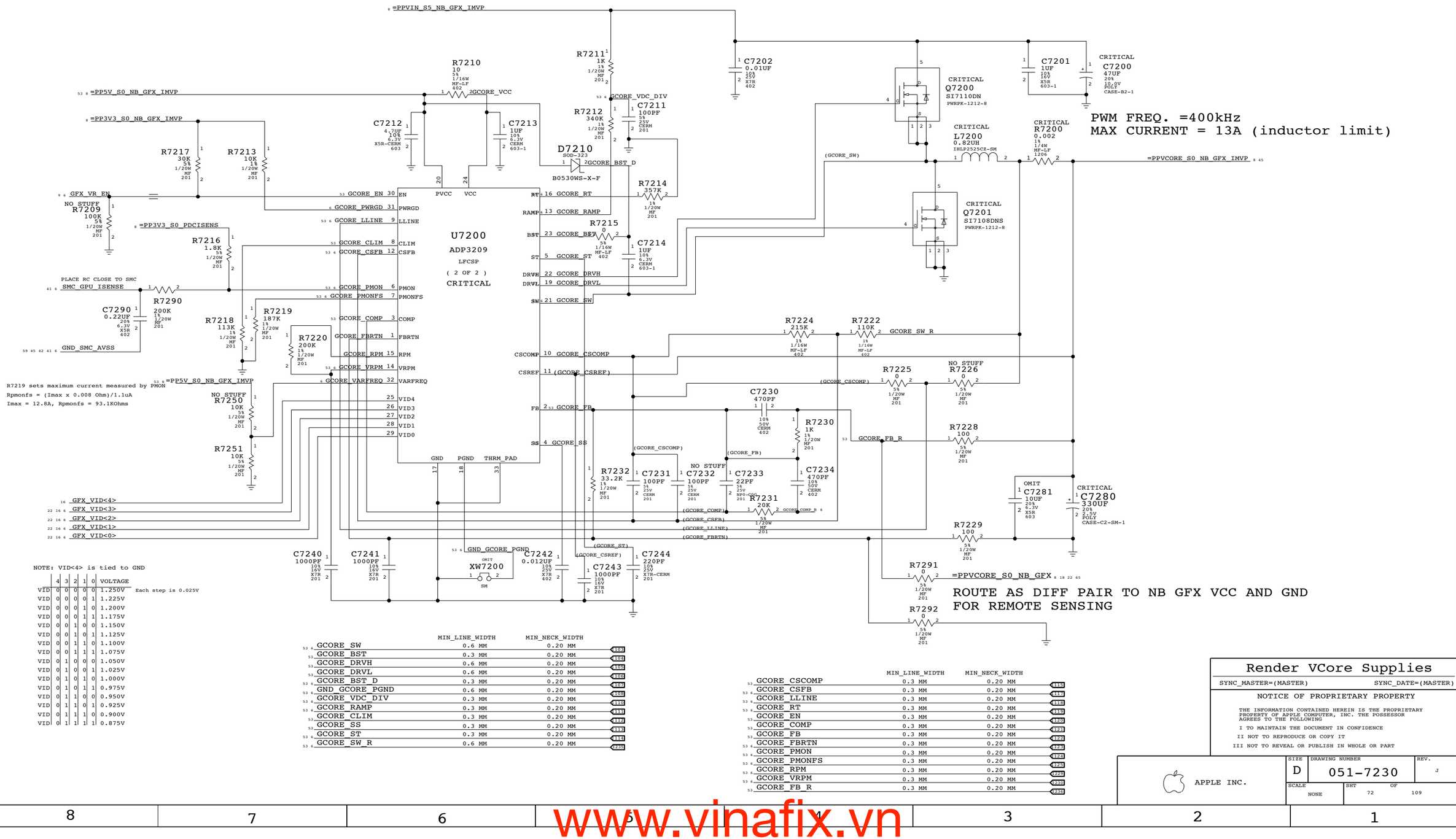
D	051-7230	J

SCALE	SHT	OF
NONE	71	109

RENDER VCORE POWER SUPPLY



NOTE: VID<4> is tied to GND

	4	3	2	1	0	VOLTAGE
VID	0	0	0	0	0	1.250V
VID	0	0	0	0	1	1.225V
VID	0	0	0	1	0	1.200V
VID	0	0	0	1	1	1.175V
VID	0	0	1	0	0	1.150V
VID	0	0	1	0	1	1.125V
VID	0	0	1	1	0	1.100V
VID	0	0	1	1	1	1.075V
VID	0	1	0	0	0	1.050V
VID	0	1	0	0	1	1.025V
VID	0	1	0	1	0	1.000V
VID	0	1	0	1	1	0.975V
VID	0	1	1	0	0	0.950V
VID	0	1	1	0	1	0.925V
VID	0	1	1	1	0	0.900V
VID	0	1	1	1	1	0.875V

Each step is 0.025V

		MIN_LINE_WIDTH	MIN_NECK_WIDTH	
53 6	GCORE_SW	0.6 MM	0.20 MM	103
53	GCORE_BST	0.3 MM	0.20 MM	104
53	GCORE_DRVH	0.6 MM	0.20 MM	105
53	GCORE_DRVL	0.6 MM	0.20 MM	106
53 6	GCORE_BST_D	0.3 MM	0.20 MM	107
53 6	GND_GCORE_PGND	0.6 MM	0.20 MM	108
53 6	GCORE_VDC_DIV	0.3 MM	0.20 MM	110
53 6	GCORE_RAMP	0.3 MM	0.20 MM	111
53	GCORE_CLIM	0.3 MM	0.20 MM	112
53	GCORE_SS	0.3 MM	0.20 MM	113
53 6	GCORE_ST	0.3 MM	0.20 MM	114
53 6	GCORE_SW_R	0.6 MM	0.20 MM	2235

		MIN_LINE_WIDTH	MIN_NECK_WIDTH	
53	GCORE_CSCOMP	0.3 MM	0.20 MM	115
53 6	GCORE_CSFB	0.3 MM	0.20 MM	117
53 6	GCORE_LLINE	0.3 MM	0.20 MM	118
53 6	GCORE_RT	0.3 MM	0.20 MM	119
53	GCORE_EN	0.3 MM	0.20 MM	120
53	GCORE_COMP	0.3 MM	0.20 MM	121
53	GCORE_FB	0.3 MM	0.20 MM	122
53 6	GCORE_FBRTN	0.3 MM	0.20 MM	123
53 6	GCORE_PMON	0.3 MM	0.20 MM	124
53 6	GCORE_PMONFS	0.3 MM	0.20 MM	125
53 6	GCORE_RPM	0.3 MM	0.20 MM	126
53 6	GCORE_VRPM	0.3 MM	0.20 MM	127
53	GCORE_FB_R	0.3 MM	0.20 MM	2236

Render VCore Supplies	
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)

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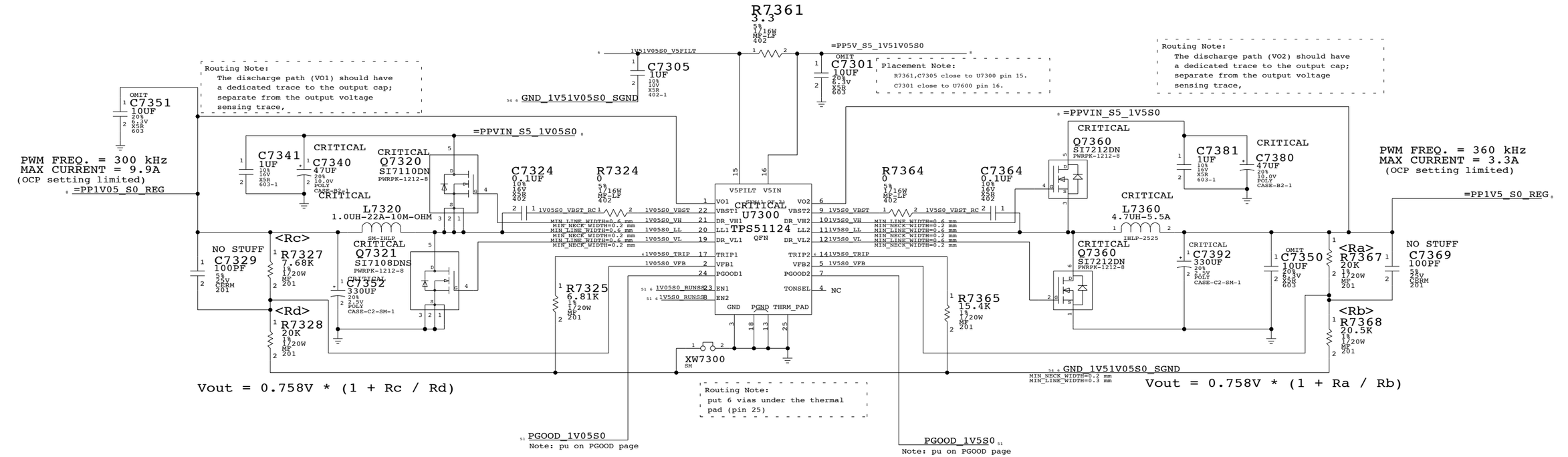
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 72 OF 109	

1.5V/1.05V POWER SUPPLY

State	PM_SLP_S3_L	PP1V5_S0	PP1V05_S0
S0	HIGH	1.5V	1.05V
S3/S5/G3Hot	LOW	0.0V	0.00V



1.5V/1.05V Supplies

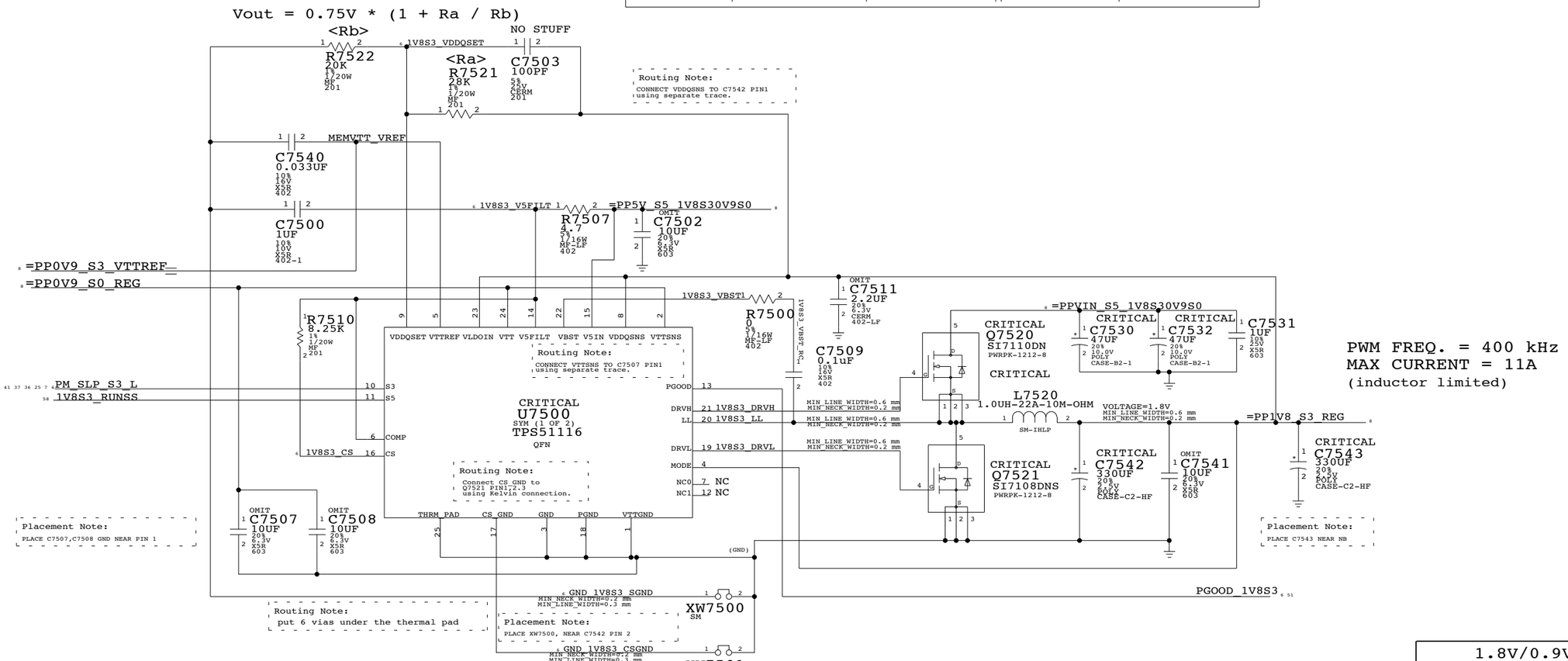
SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 73 OF 109	

1.8V/0.9V POWER SUPPLY

State	PM_S4_STATE_L	PM_SLP_S3_L	PP1V8_S3	PP0V9_S0
S0	HIGH	HIGH	1.8V	0.9V
S3	HIGH	LOW	1.8V	0.0V
S5/G3Hot	LOW	LOW	0.0V	0.0V



1.8V/0.9V Supplies

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

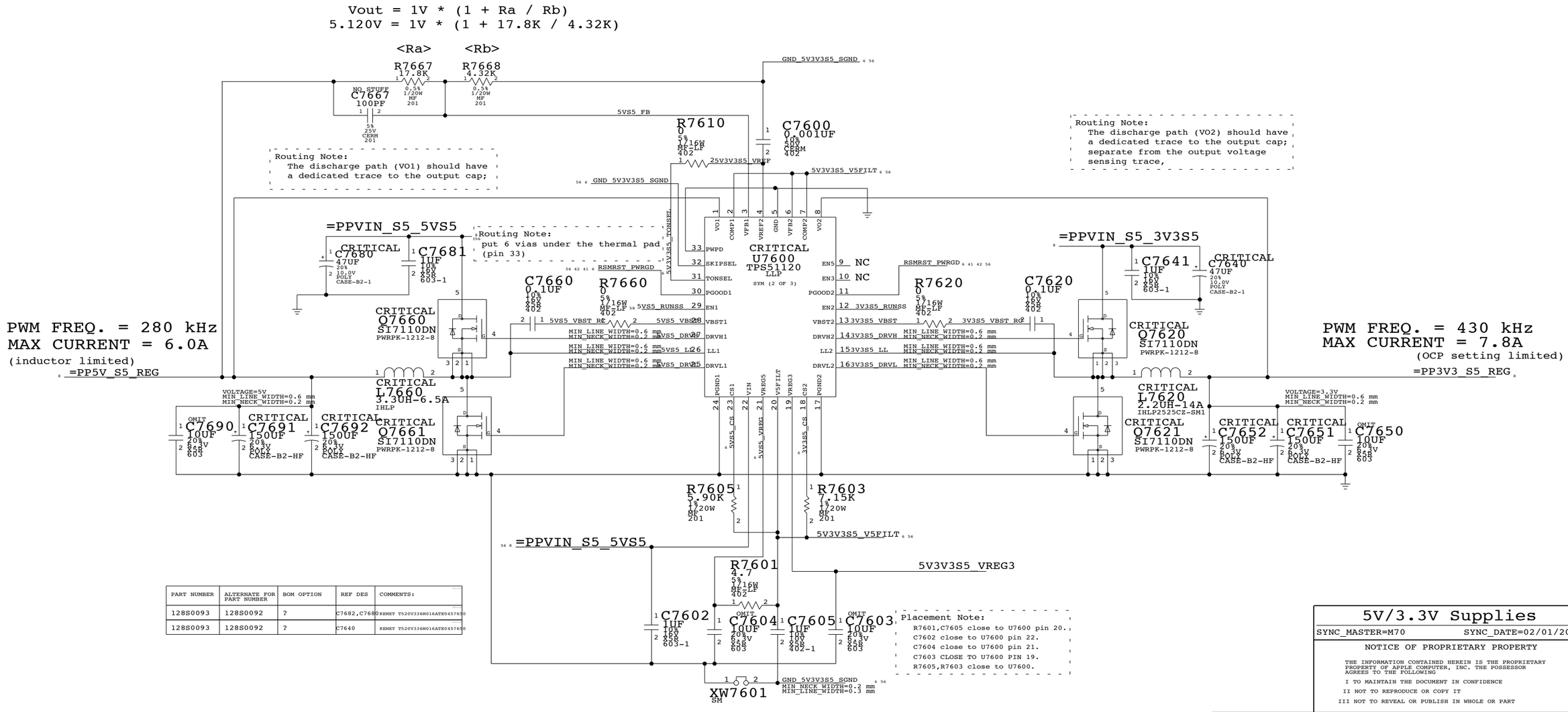
SIZE	DRAWING NUMBER	REV.
D	051-7230	J

SCALE	SHT	OF
NONE	75	109

5V/3.3V POWER SUPPLY

State	SMC_PM_G2_EN	PP3V3_G3H	PP5V_S5	PP3V3_S5
G3H	LOW	3.3V	0.0V	0.0V
S0/S3/S5	HIGH	3.3V	5.0V	3.3V

Vout = 1V * (1 + Ra / Rb)
5.120V = 1V * (1 + 17.8K / 4.32K)



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7682,C7680	KEMET T520V336M016ATE0457650
128S0093	128S0092	?	C7640	KEMET T520V336M016ATE0457650

5V/3.3V Supplies

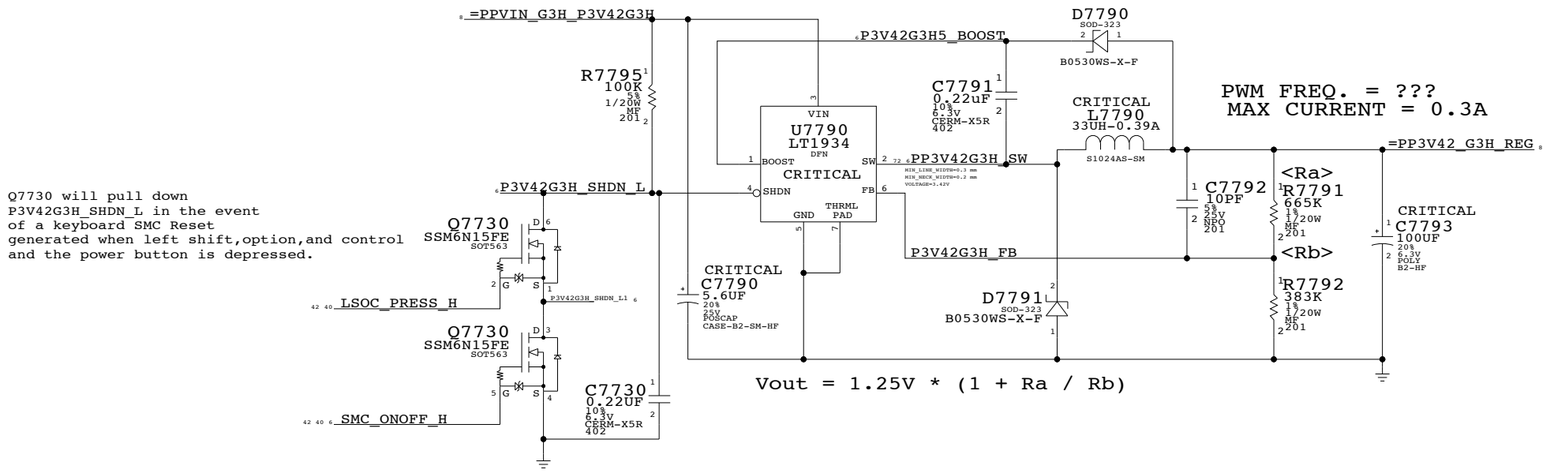
SYNC_MASTER=M70 SYNC_DATE=02/01/2007

APPLE INC.

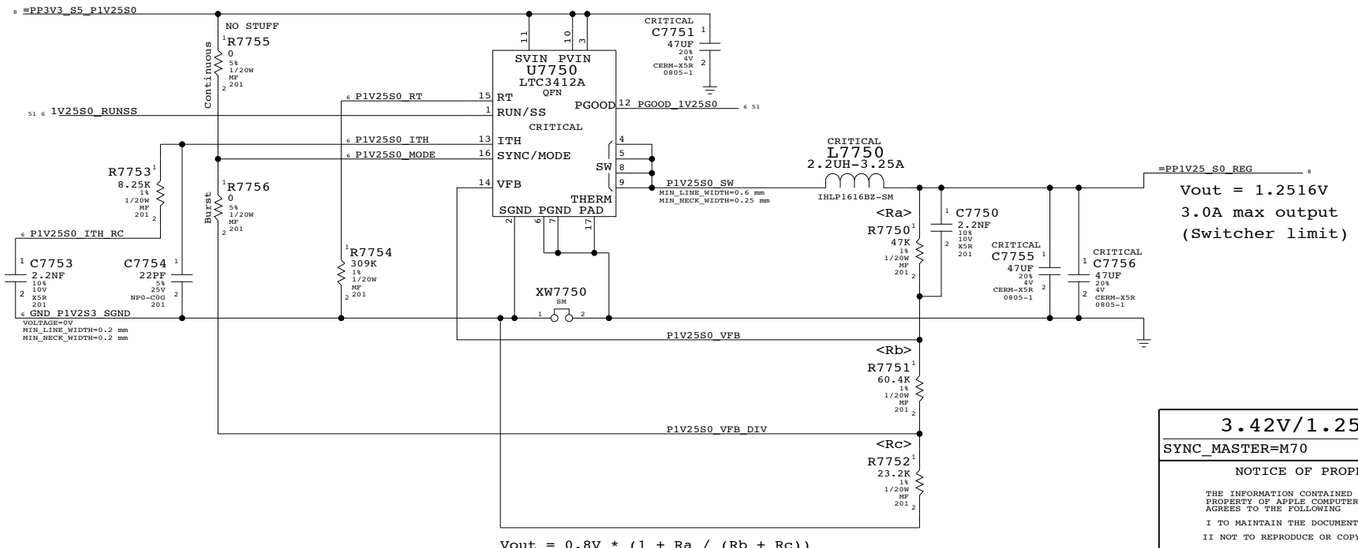
SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 76 OF 109	

3.425V G3H SUPPLY

Supply needs to guarantee 3.31V delivered to SMC VRef generator



1.25V S0 REGULATOR



3.42V/1.25V Switcher

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

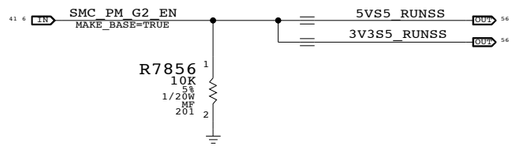
APPLE INC.

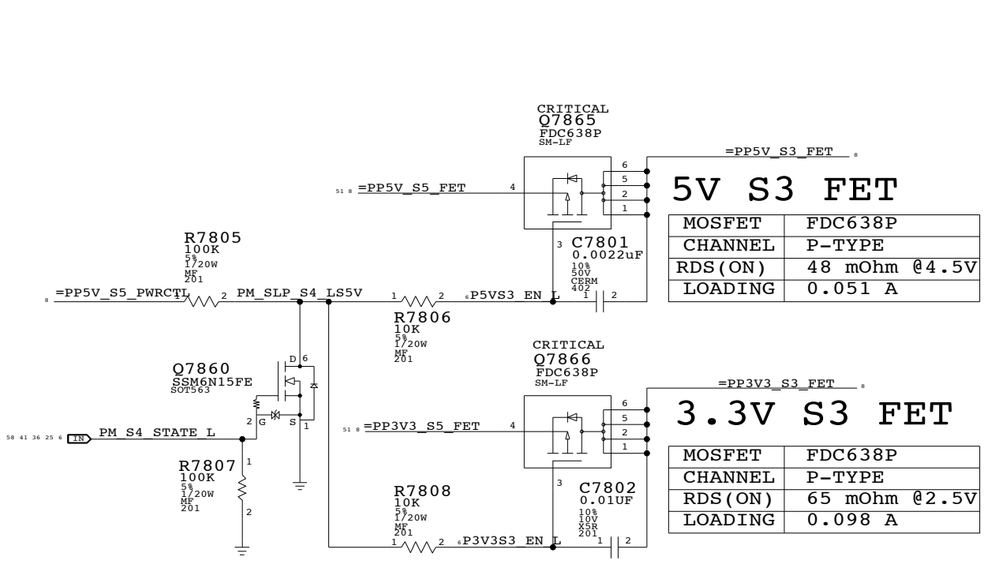
SIZE	DRAWING NUMBER	REV.
D	051-7230	J

SCALE	SHT	OF
NONE	77	109

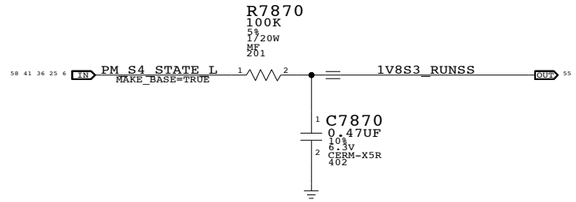
S3 FETS & S3/S5 CONTROL

5V/3.3V S5 RUN/SS CONTROL





1.8V S3 RUN/SS CONTROL



S3 FET & S3/S5 Control

SYNC_MASTER=M70 SYNC_DATE=02/01/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J

SCALE: NONE

SHT 78 OF 109

PBUS SUPPLY / BATTERY CHARGER

PBUS CURRENT SENSOR

=PPBUSB_G3H
R7981 21 1% 1/16W MF-LF 402
C7980 0.1UF 10% 25V X5R 402
U7980 LTC6102AP DFN
V+ -INF -INS +IN V- VREG OUT SHDN THM PAD
CRITICAL
PBUS_ISENSE_IN_NEG
PBUS_ISENSE_VREG
PLACE C CLOSE TO SMC
SMC_PBUS_ISENSE
=PPBUSA_G3H
R7989 4.53K 1% 1/20W MF 201
C7989 0.22UF 20% 2.2V X5R 402
GND_SMC_AVSS
PBUS_SMC_VSENSE_EN_L
LTC6102 DISABLED WHEN SHDN=1
LTC6102 ENABLED WHEN SHDN=0

=PP18V5_G3H_CHGR
CRITICAL D7910 SOD-323 B0530WS-X-F
C7900 0.1UF 10% 25V X5R 402
R7900 100K 5% 1/20W MF 201
CRITICAL Q7900 AO4409 SO1
PPVDCIN_G3H_PRE2
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
CRITICAL Q7901 AO4409 SO1
PPVDCIN_G3H_PRE
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
R7999 100K 5% 1/20W MF 201
CHGR_SGATE_DIV
R7962 62K 5% 1/20W MF 201
=PP3V42_G3H_CHGR
R7960 57.6K 1% 1/20W MF 201
R7961 1.82K 1% 1/20W MF 201
CHGR_AMON
CHGR_LOWCURRENT_REF
CHGR_LOWCURRENT_GATE
C7960 0.1UF 10% 25V X5R 402
CRITICAL U7960 TL331 SOT23-5
VCC GND
CHGR_DCIN
C7910 0.1UF 10% 25V X5R 402
R7901 62K 5% 1/20W MF 201
CHGR_SGATE
R7923 10 5% 1/20W MF 201
XW7920 SM
R7921 10 5% 1/20W MF 201
XW7921 SM
C7924 0.047UF 10% 16V X7R 402
CRITICAL R7920 0.02 0.5% 1W MF 2612
R7910 30.1K 1% 1/20W MF 201
R7911 9.76K 1% 1/20W MF 201
(CHGR_ACIN)
C7941 1UF 10% 10V X5R 402-1
R7940 4.7 5% 1/16W MF-LF 402
C7940 1UF 10% 10V X5R 402-1
CHGR_VDD
CHGR_VDDP
=PP3V42_G3H_CHGR
C7947 1UF 10% 10V X5R 402-1
C7995 0.1UF 10% 25V X5R 402
C7996 0.1UF 10% 25V X5R 402
GND_CHGR_SGND
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
PP18V5_S5_CHGR_SW_R
CRITICAL C7920 22UF 20% 25V POLY CASE-D2-LF
CRITICAL C7921 22UF 20% 25V POLY CASE-D2-LF
CRITICAL C7922 1UF 10% 25V X5R 603
C7923 1UF 10% 25V X5R 603
KELVIN CONNECTION
TO CURRENT SENSOR U7980
CRITICAL R7980 0.002 1% 1/4W MF-LF 1206
=PPBUSA_G3H
TO SYSTEM
=PPBUSB_G3H
CRITICAL F7900 7AMP-24V 1206
CRITICAL R7930 0.01 0.5% 1W MF 0612
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
PPVBAT_G3H_CHGR_OUT
C7935 1UF 10% 25V X5R 603
CRITICAL L7900 4.7UH-7.5A IHLP4040CZ-SM
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
PPVBAT_G3H_CHGR_REG
CRITICAL C7930 47UF 20% 10.0V POLY CASE-B2-1
CRITICAL C7931 47UF 20% 10.0V POLY CASE-B2-1
XW7930 SM
XW7931 SM
R7931 10 5% 1/20W MF 201
R7947 10 5% 1/20W MF 201
(CHGR_CSOP)
CRITICAL Q7920 FDM6296 MICROFET3X3
CRITICAL Q7921 FDM6296 MICROFET3X3
C7925 0.1UF 10% 25V X5R 402
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM

CRITICAL U7900 ISL6258 QFN
VDD VDDP VHST SCL SDA OMIT NC VREF ACIN ICOMP VCOMP VNEG CSOP CSON AGATE CSIP CSIN BGATE DCIN BOOT UGATE PHASE LGATE TRKL* AMON BMON ACOK THRM_PAD AGND PGND
pullups offpage
CHGR_SCL
CHGR_SDA
CHGR_AGATE
CHGR_CSIP
CHGR_CSIN
CHGR_BGATE
CHGR_DCIN
CHGR_BOOT
CHGR_UGATE
CHGR_PHASE
CHGR_LGATE
NC
CHGR_AMON
CHGR_BMON
CHGR_ACOK
C7942 33000PF 10% 6.3V X5R 201
C7944 0.01UF 10% 10V X5R 201
R7945 56.2K 1% 1/16W MF-LF 402
C7943 0.1UF 10% 16V X5R 402
C7945 0.001UF 10% 50V CERM 402
R7946 3.01K 1% 1/16W MF-LF 402
C7946 470PF 10% 50V CERM 402
XW7900 SM
C7926 1000PF 10% 16V X7R 201
GND_CHGR_SGND
(CHGR_CSOP)
(CHGR_CSON)

PWM FREQ. = 400 kHz
MAX CURRENT = ??A
(??? limited)

AMON PULLDOWN LOGIC

CHGR_AMON
=PP3V42_G3H_CHGR
R7974 1M 5% 1/20W MF 201
Q7970 SSM6N15FE SOT563
R7975 1M 5% 1/20W MF 201
NO_STUFF
CHGR_VDD
R7973 1M 5% 1/20W MF 201
Q7970 SSM6N15FE SOT563
CHGR_VDD_R

BATTERY CHARGING

CRITICAL Q7950 AO4409 SO1
PPVBAT_G3H_CHGR_OUT
C7950 0.01UF 10% 16V X5R 201
C7951 0.1UF 10% 16V X5R 402
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
BATT_POS_F
CHGR_BGATE
TO BATTERY

=SMBUS_CHGR_SCL — CHGR_SCL
=SMBUS_CHGR_SDA — CHGR_SDA
ACOK pullup/down on SMC page
SMC_BC_ACOK — CHGR_ACOK
MAKE_BASE=TRUE

PLACE RC CLOSE TO SMC
CHGR_BMON
SMC_BATT_ISENSE
R7971 0 5% 1/20W MF 201
C7972 0.68UF 10% 6.3V CERM 402
GND_SMC_AVSS

PLACE RC CLOSE TO SMC
CHGR_AMON
SMC_DCIN_ISENSE
R7970 0 5% 1/20W MF 201
C7971 0.68UF 10% 6.3V CERM 402
GND_SMC_AVSS

PBUS Supply/Battery Charger
SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 79 OF 109	

LCD + CAMERA CONNECTOR

=PP3V3_S5_LCD
R9002 100K 5% 1/20W MF 201
C9040 0.1UF 10% 6.3V X5R 201
R9014 100K 5% 1/20W MF 201
Q9004 SSM3K15FV SOD-VESM
LCDVDD_PLT_RST_L
LVDS_VDD_EN
U9040 TC7SZ08AFEF SOT665
LVDS_VDD_GATED_EN
R9023 10K 5% 1/20W MF 201
LCDVDD_PWREN_L
LCDVDD_PWREN_L_R
CRITICAL Q9003 FDC638P SM-LF
C9013 0.0033UF 10% 50V CERM 402
C9011 0.1UF 10% 6.3V X5R 201
C9012 10UF 20% 6.3V X5R 603 OMIT
PP3V3_LCDVDD_SW
VOLTAGE=3.3V MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM

=USB2_CAMERA_N
=USB2_CAMERA_P
CRITICAL L9007 90-OHM-100MA 1210-4SM1
CRITICAL L9005 FERR-120-OHM-1.5A 0402-LF
=PP5V_S3_CAMERA
C9016 1000PF 10% 16V X7R 201
CRITICAL L9004 FERR-120-OHM-1.5A 0402-LF
C9015 1000PF 10% 16V X7R 201

L9052 240-OHM-0.2A-0.8-OHM 0201
=I2C_TOP_ALS_SDA
I2C_TOP_ALS_SDA_F
L9051 240-OHM-0.2A-0.8-OHM 0201
=I2C_TOP_ALS_SCL
I2C_TOP_ALS_SCL_F
C9052 10PF 5% 25V NPO 201
C9051 10PF 5% 25V NPO 201

CRITICAL J9000 20347-130E-11 F-RT-SM
CAMERA I/F
LCD I/F
PP5V_S3_CAMERA_F
USB2_CAMERA_F_P
USB2_CAMERA_F_N
PP3V3_LCDVDD_SW_F
PP3V3_S0_LCD_F
LVDS_A_DATA_F_N<0>
LVDS_A_DATA_F_P<0>
LVDS_A_DATA_F_N<1>
LVDS_A_DATA_F_P<1>
LVDS_A_DATA_F_N<2>
LVDS_A_DATA_F_P<2>
LVDS_A_CLK_F_N
LVDS_A_CLK_F_P
LCDBKLT_RTN<1>
LCDBKLT_RTN<2>
LCDBKLT_RTN<3>
LCDBKLT_RTN<4>
LCDBKLT_RTN<5>
LCDBKLT_RTN<6>
PPVOUT_S0_LCDBKLT
518S0433

PLACE FILTERS AND CAPS NEAR PINS ON CONNECTOR

L9008 120-OHM-0.3A-EMI 0402-LF
=PP3V3_S0_LCD
(LVDS_DDC_POWER)
C9010 1000PF 10% 16V X7R 201
R9008 10K 5% 1/20W MF 201
R9009 10K 5% 1/20W MF 201
LVDS_DDC_CLK
LVDS_DDC_DATA

LVDS REFERENCE CURRENT,3.24K OHM PULL DOWN RESISTOR NEEDED
R9013 3.24K 1% 1/20W MF 201
LVDS_IBG
PLACE NEAR NB

CRITICAL L9010 90-OHM-100MA 1210-4SM1
LVDS_A_DATA_N<0>
LVDS_A_DATA_P<0>
CRITICAL L9011 90-OHM-100MA 1210-4SM1
LVDS_A_DATA_N<1>
LVDS_A_DATA_P<1>
CRITICAL L9012 90-OHM-100MA 1210-4SM1
LVDS_A_DATA_N<2>
LVDS_A_DATA_P<2>
CRITICAL L9006 90-OHM-100MA 1210-4SM1
LVDS_A_CLK_N
LVDS_A_CLK_P

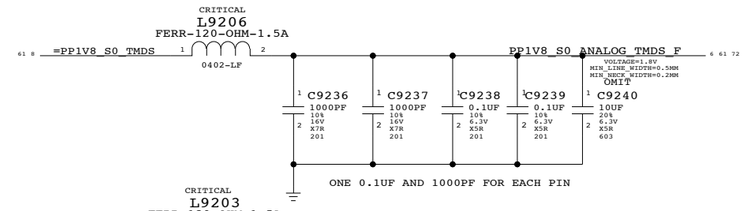
MIC CONNECTOR

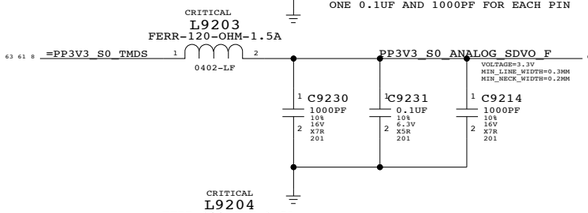
CRITICAL J9050 GS03067-11131-7F F-RT-SM
PP3V3_S3_MIC_F
NC
NC
GND_MIC_F
L9050 240-OHM-0.2A-0.8-OHM 0201
=PP3V3_S3_MIC
MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.20MM VOLTAGE=3.3V
AUD_MIC_DATA_F
AUD_MIC_CLK_F
L9030 240-OHM-0.2A-0.8-OHM 0201
AUD_MIC_DATA
L9031 240-OHM-0.2A-0.8-OHM 0201
AUD_MIC_CLK
L9053 240-OHM-0.2A-0.8-OHM 0201
C9050 0.01UF 10% 10V X5R 201
C9053 0.01UF 10% 10V X5R 201
NO STUFF C9030 10PF 5% 25V NPO 201
NO STUFF C9031 10PF 5% 25V NPO 201

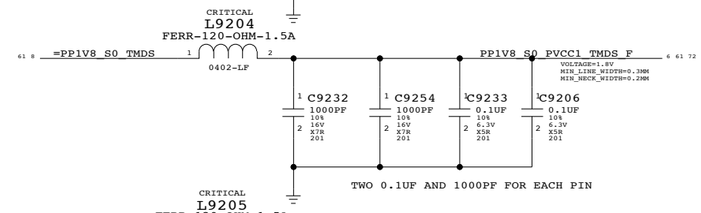
APN:518S0356

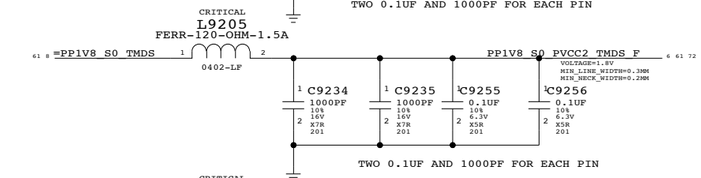
LVDS,Camera Conn. and ALS Conn.
SYNC_MASTER=GPU SYNC_DATE=06/23/2006

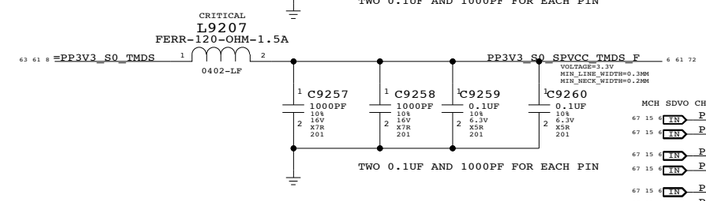
APPLE INC.
SIZE D | DRAWING NUMBER 051-7230 | REV. J
SCALE NONE | SHT 90 OF 109

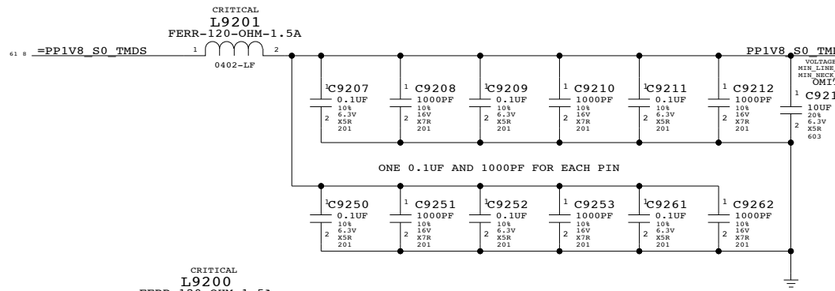


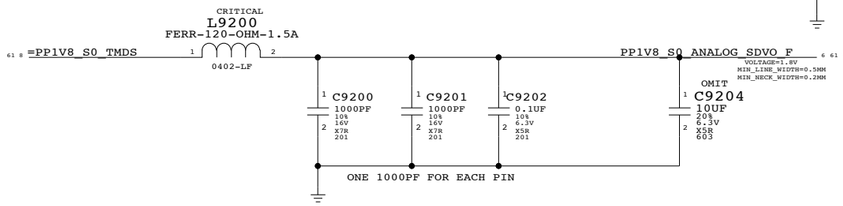


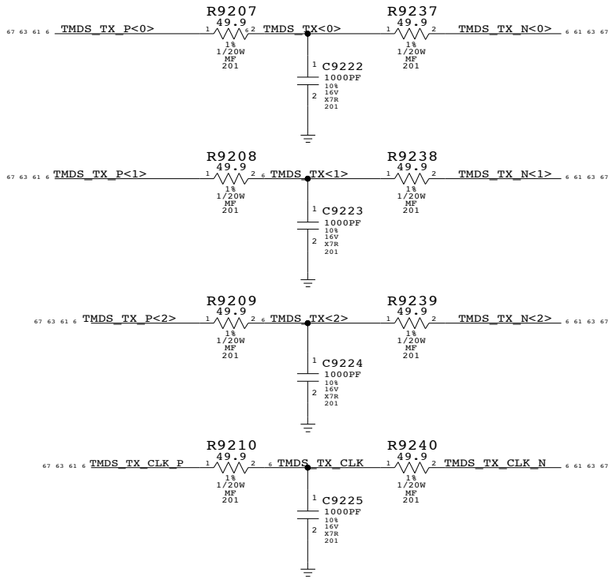


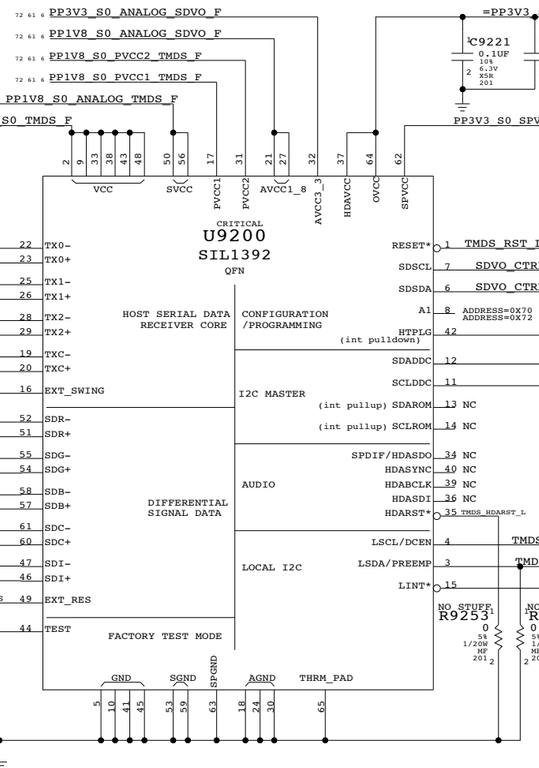


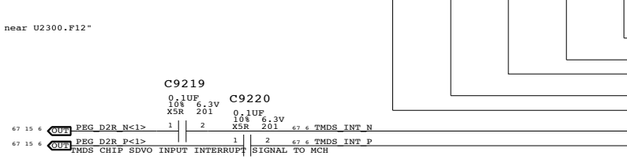


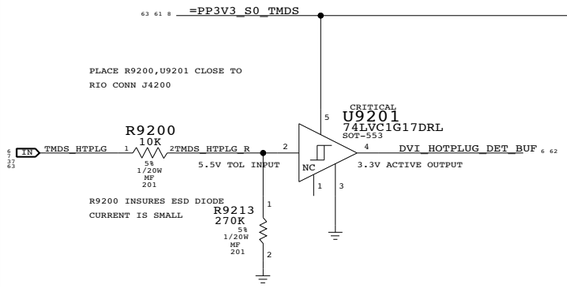


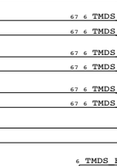












SDVO/TMDS Tx		
SYNC_MASTER=GRAPHIC	SYNC_DATE=06/06/2005	
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APPLE INC.	SIZE: D	DRAWING NUMBER: 051-7230
	REV: J	
	SCALE: NONE	SHT 92 OF 109

SST8051 microcontroller for HDCP support

=PP3V3_S0_HDCP

C9341 0.1UF 10% 6.3V X5R 201

DVI_HOTPLUG_DET_BUF

R9340 10K 5% 1/20W MF 201

U9340 74LVC2G132 US8

C9340 1UF 10% 6.3V CERM 603-1

10MS RC GENERATES ONE-SHOT LOW PULSE ON INT0# TO ALLOW PART TO WAKE UP AND XTAL TO START

L9300 FERR-120-OHM-1.5A 0402-LF

PP3V3_S0_HDCP_F

C9302 0.01UF 10% 10V X5R 201

C9301 0.1UF 10% 6.3V X5R 201

C9300 10UF 20% 6.3V X5R 603

MIN_LINE_WIDTH=0.30MM MIN_NECK_WIDTH=0.20MM VOLTAGE=3.3V

=PP3V3_S0_HDCP

R9306 4.7K 5% 1/20W MF 201

R9302 2.2K 5% 1/20W MF 201

R9303 2.2K 5% 1/20W MF 201

R9304 2.2K 5% 1/20W MF 201

R9305 2.2K 5% 1/20W MF 201

SST8051_DDC_EN

Q9300 SSM6N15FE SOT563

TMDS_DDC_SCL

TMDS_DDC_SDA

U9300 SST89V54RD WQFN

VDD OMIT CRITICAL

DVI_HOTPLUG_DET_INT_L	7	(INT0#)P3.2	
TMDS_LINT_L	8	(INT1#)P3.3	
TP_SST8051_RXD	5	(RXD)P3.0	
SST8051_P34_AUDIO_CONFIG	9	(T0)P3.4	
NC	10	(T1)P3.5	
NC	12	(RD#)P3.7	
NC	11	(WR#)P3.6	
TP_SST8051_TXD	6	(TXD)P3.1	
	34	P0.0(AD0)	NC
	33	P0.1(AD1)	
	32	P0.2(AD2)	
	31	P0.3(AD3)	
	30	P0.4(AD4)	
	29	P0.5(AD5)	
	28	P0.6(AD6)	
	27	P0.7(AD7)	
	36	P1.0(T2)	SST8051_PSEN_L
	37	P1.1(T2_EX)	DVI_HOTPLUG_DET_BUF
	38	P1.2(ECI)	SST8051_DVI_HOTPLUG_DET
	39	P1.3(CEX0)	NC
	40	P1.4(CEX1/SS*)	SST8051_DDC_CLK
	1	(CEX2/MOSI)P1.5	SST8051_DDC_DATA
	2	(CEX3/MISO)P1.6	
	3	(CEX4/SCK)P1.7	
	16	A8(P2.0)	NC
	17	A9(P2.1)	NC
	18	A10(P2.2)	NC
	19	A11(P2.3)	NC
	20	A12(P2.4)	NC
	21	P2.5(A13)	SST8051_P25_AUDIO_CONFIG
	22	P2.6(A14)	NC
	23	P2.7(A15)	NC
	14	XTAL1	
	13	XTAL2	
	4	RST	
	26	EA*	
NC	25	ALE/PROG*	
SST8051_PSEN_L	24	PSEN*	
	41	THRM_PAD	
	15	VSS	

C9390 22PF 5% 25V NP0-C0G 201

C9391 22PF 5% 25V NP0-C0G 201

Y9390 OMIT 14.318MHZ-35PPF-20PF 8M-2.5X2.0MM

SST8051_XTAL1

SST8051_XTAL2

SST8051_RST

SST8051_EA_L

TMDS_LSCL

TMDS_LSDA

=PP3V3_S0_HDCP

C9326 0.1UF 10% 6.3V X5R 201

U9325 TC7SH00FEF SON

TMDS_HW_RESET_L

SST8051_SW_RESET_L

R9325 10K 1% 1/20W MF 201

NO STUFF

R9350 0 5% 1/20W MF 201

SST8051_DVI_HOTPLUG_DET

DVI_HOTPLUG_DET

R9351 0 5% 1/20W MF 201

DVI_HOTPLUG_DET_BUF

STUFFING OPTION CHOOSES RAW OR CONTROLLER OUTPUT OF DVI_HOTPLUG_DET

=PP3V3_S0_HDCP

R9330 4.7K 1% 1/20W MF 201

SST8051_UPDATE_L

SST8051_PSEN_L

MAKE_BASE=TRUE

SST8051_UPDATE_L pulled up to 10K at SB

=PP3V3_S0_HDCP

R9301 10K 1% 1/20W MF 201

SST8051_EA_L

SST8051_P25_AUDIO_CONFIG

SST8051_P34_AUDIO_CONFIG

R9333 4.7K 1% 1/20W MF 201

AUDIO CONFIG OPTIONS

P25	P34	OPTION
0	0	HD AUDIO
0	1	SPDIF
1	0	NO AUDIO
1	1	RESERVED

HDCP uController

SYNC_MASTER= SYNC_DATE=

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D	051-7230	J

SCALE NONE SHT 93 OF 109

Video Connectors

TMDS(MICRO DVI) INTERFACE
EXTERNAL VIDEO (VGA) INTERFACE

NB VIDEO ALIASES

=CRT_TVO_IREF = CRT_TVO_IREF
=TV_A_DAC = TV_A_DAC
=TV_B_DAC = TV_B_DAC
=TV_C_DAC = TV_C_DAC
=CRT_BLUE = CRT_BLUE
=CRT_GREEN = CRT_GREEN
=CRT_RED = CRT_RED
=CRT_HSYNC_R = CRT_HSYNC_R
=CRT_VSYNC_R = CRT_VSYNC_R
(MAKE_BASE=TRUE)

Isolation required for DVI power switch

A 1.3K OHM 1% RESISTOR IS REQUIRED BETWEEN CRT_IREF AND GROUND

R9469 1.3K 1% 1/20W MF 201 — CRT_TVO_IREF

CRITICAL
F9404 0.5AMP-13.2V SM-LF
=PP5V_S0_TMDS → PP5V_S0_TMDS_FUSE
VOLTAGE=5V MIN_LINE_WIDTH=0.30 MM MIN_NECK_WIDTH=0.20 MM
VOLTAGE=5V MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM

L9444 600-OHM-300MA 0402
PP5V_S0_TMDS_FUSE → PP5V_S0_DVIPORT
VOLTAGE=5V MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.25 MM

C9404 0.1UF 10% 16V X5R 402

D9401 1SS418 SOD-723
PP5V_S0_DVIPORT_D
VOLTAGE=5V MIN_LINE_WIDTH=0.2 MM MIN_NECK_WIDTH=0.2 MM

=PP3V3_S0_NB
R9466 2.2K 5% 1/20W MF 201 — TV_DCONSEL<0>
R9467 2.2K 5% 1/20W MF 201 — TV_DCONSEL<1>

R9462 1K 5% 1/20W MF 201
R9463 1K 5% 1/20W MF 201

=PP3V3_S0_TMDS
R9480 10K 5% 1/20W MF 201 — DVI_HOST
HDMI_HOST
R9481 100K 5% 1/20W MF 201

TMDS_HTPLG
TMDS_DDC_SDA
TMDS_DDC_SCL
C9410 1000PF 10% 16V X7R 201
NOSTUFF C9411 100PF 5% 25V CERM 201
NOSTUFF C9412 100PF 5% 25V CERM 201

SB_CRT_TVOUT_MUX_L

PLACE R9450 R9451 CLOSE TO NB
R9450 150 1% 1/20W MF 201 — TV_A_DAC
R9451 150 1% 1/20W MF 201 — CRT_BLUE
=TV_A_RTN VOLTAGE=0V
=CRT_BLUE_L VOLTAGE=0V

PLACE R9452 R9453 CLOSE TO NB
R9452 150 1% 1/20W MF 201 — TV_B_DAC
R9453 150 1% 1/20W MF 201 — CRT_GREEN
=TV_B_RTN VOLTAGE=0V
=CRT_GREEN_L VOLTAGE=0V

PLACE R9454 R9455 CLOSE TO NB
R9454 150 1% 1/20W MF 201 — TV_C_DAC
R9455 150 1% 1/20W MF 201 — CRT_RED
=TV_C_RTN VOLTAGE=0V
=CRT_RED_L VOLTAGE=0V

PLACE U9401 NEAR NB
=PP3V3_S0_NB
C9439 0.1UF 10% 16V X5R 201
U9401 FSAV430 DQFN
CRITICAL
VCC, S, 1B1, 1B2, 1A, 2B1, 2B2, 2A, OE*, 4B1, 4B2, 4A, 3B1, 3B2, 3A, NC, GND, THMPAD

FL9400 210MHZ MEA2010P-SM
CRITICAL
EXT_C_R
EXT_Y_G
EXT_COMPVID_B
VGA_B
VGA_G
VGA_R

These nets connect to RIO connector J4200

PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR CONNECTOR
=PP3V3_S0_TMDS
C9460 0.1UF 10% 6.3V X5R 201
CRITICAL U9404 SN74LVC2G125DCU
R9460 39 5% 1/20W MF 201 — CRT_HSYNC_R → CRT_HSYNC_LS_R
R9470 39 5% 1/20W MF 201 — CRT_HSYNC_LS → VGA_HSYNC
NOSTUFF C9442 33PF 5% 25V NPO-C0G 201

PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR THE CONNECTOR
CRITICAL U9404 SN74LVC2G125DCU
R9461 39 5% 1/20W MF 201 — CRT_VSYNC_R → CRT_VSYNC_LS_R
R9471 39 5% 1/20W MF 201 — CRT_VSYNC_LS → VGA_VSYNC
NOSTUFF C9443 33PF 5% 25V NPO-C0G 201

CRITICAL L9405 90-OHM-100MA 1210-4SM1
TMDS_TX_P<2> / TMDS_TX_N<2>
CRITICAL L9407 90-OHM-100MA 1210-4SM1
TMDS_TX_P<1> / TMDS_TX_N<1>
CRITICAL L9406 90-OHM-100MA 1210-4SM1
TMDS_TX_P<0> / TMDS_TX_N<0>
CRITICAL L9404 300-OHM-100MA 1210-4SM
TMDS_TX_CLK_P / TMDS_TX_CLK_N

TMDS_TX_CONN_P<2>
TMDS_TX_CONN_N<2>
TMDS_TX_CONN_P<1>
TMDS_TX_CONN_N<1>
TMDS_TX_CONN_P<0>
TMDS_TX_CONN_N<0>
TMDS_TX_CONN_CLK_P
TMDS_TX_CONN_CLK_N

Place components near J4200
unless otherwise noted

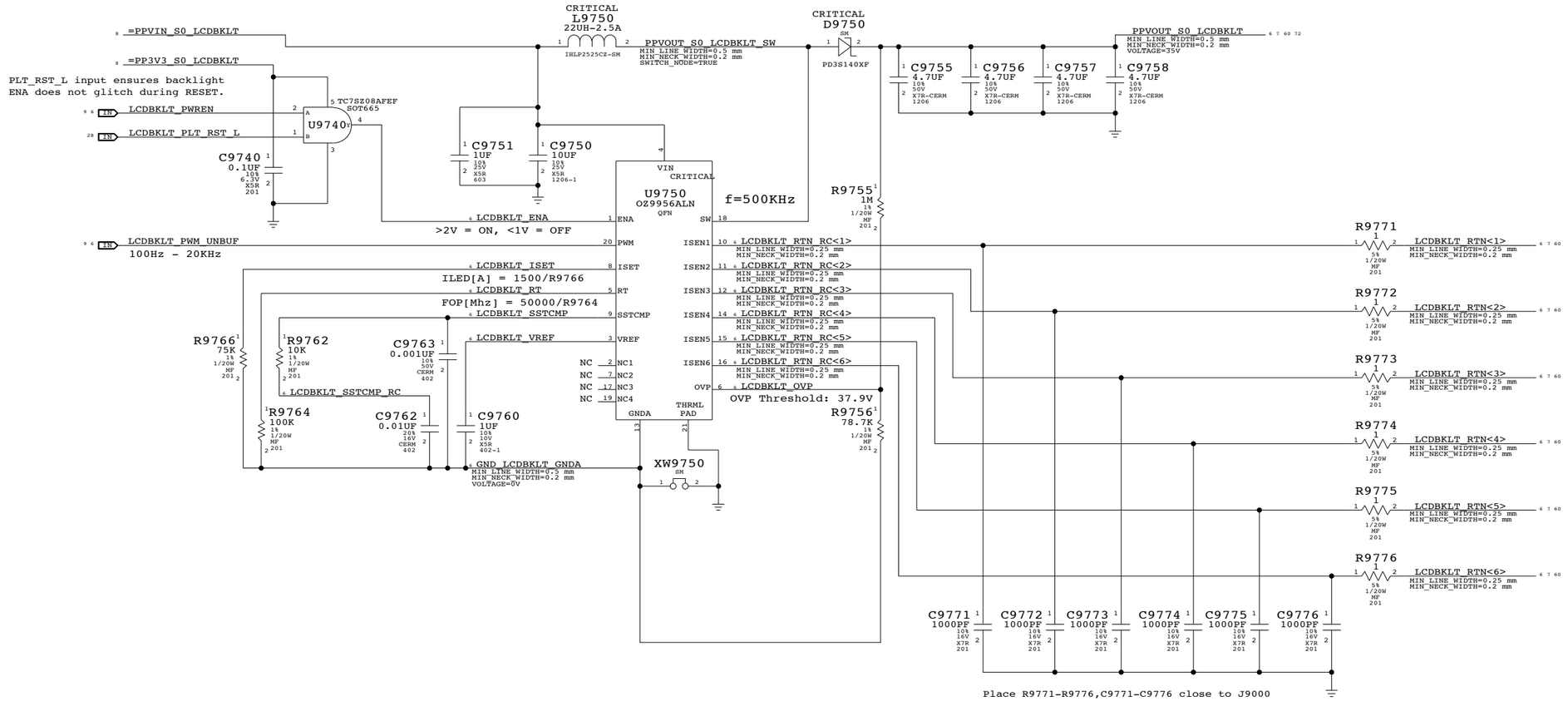
DVI CONNECTIONS

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 94 OF 109	

LED Backlight Driver



LED Backlight Driver

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J

SCALE: NONE SHT 97 OF 109

ADDITIONAL CPU VCORE HF DECOUPLING

40x 1uF 0402

12 11 8 =PPVCORE_S0_CPU

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C9900 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9901 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9902 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9903 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9904 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9905 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9906 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9907 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9908 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9909 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C9910 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9911 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9912 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9913 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9914 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9915 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9916 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9917 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9918 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9919 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C9920 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9921 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9922 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9923 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9924 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9925 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9926 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9927 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9928 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9929 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C9930 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9931 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9932 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9933 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9934 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9935 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9936 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9937 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9938 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C9939 2.2UF 20% 6.3V CERM 402-LF

ADDITIONAL GPU VCORE HF DECOUPLING

18x 1uF 0402

53 22 18 8 =PPVCORE_S0_NB_GFX

OMIT C9980 2.2UF 20% 6.3V CERM 402-LF
OMIT C9981 2.2UF 20% 6.3V CERM 402-LF
OMIT C9982 2.2UF 20% 6.3V CERM 402-LF
OMIT C9983 2.2UF 20% 6.3V CERM 402-LF
OMIT C9984 2.2UF 20% 6.3V CERM 402-LF
OMIT C9985 2.2UF 20% 6.3V CERM 402-LF
OMIT C9986 2.2UF 20% 6.3V CERM 402-LF
OMIT C9987 2.2UF 20% 6.3V CERM 402-LF
OMIT C9988 2.2UF 20% 6.3V CERM 402-LF
OMIT C9989 2.2UF 20% 6.3V CERM 402-LF

OMIT C9990 2.2UF 20% 6.3V CERM 402-LF
OMIT C9991 2.2UF 20% 6.3V CERM 402-LF
OMIT C9992 2.2UF 20% 6.3V CERM 402-LF
OMIT C9993 2.2UF 20% 6.3V CERM 402-LF
OMIT C9994 2.2UF 20% 6.3V CERM 402-LF
OMIT C9995 2.2UF 20% 6.3V CERM 402-LF
OMIT C9996 2.2UF 20% 6.3V CERM 402-LF
OMIT C9997 2.2UF 20% 6.3V CERM 402-LF

Additional CPU/GPU Decoupling

SYNC_MASTER= SYNC_DATE=

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D	051-7230	J
SCALE: NONE	SHT 99 OF 109	

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	ISL3,ISL10	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_4MIL	*	0.100 MM	?
FSB_9MIL	*	0.228 MM	?
FSB_DATA	*	=FSB_4MIL	?
FSB_DATA2DATA	*	=FSB_4MIL	?
FSB_DSTB	*	=FSB_9MIL	?
FSB_DATA2DSTB	*	=FSB_9MIL	?
FSB_ADDR	*	=FSB_4MIL	?
FSB_ADDR2ADDR	*	=FSB_4MIL	?
FSB_ADSTB	*	=FSB_9MIL	?
FSB_ADDR2ADSTB	*	=FSB_9MIL	?
FSB_COMMON	*	=FSB_4MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_70D	*	Y	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2TO1	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?
CPU_THERMD	*	25 MIL	?

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance.

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_ADS_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BNR_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BPRI_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BREQ0_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DBSY_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DEFER_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DPWR_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DRDY_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_HIT_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_HITM_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_LOCK_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_TRDY_L	10 14
FSB_CPURST_L	FSB_55S	FSB_COMMON	FSB_CPURST_L	6 10 13 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_D_L<15..0>	10 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_DINV_L<0>	10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<0>	10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<0>	10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_D_L<31..16>	10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_DINV_L<1>	10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<1>	10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<1>	10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_D_L<47..32>	10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_DINV_L<2>	10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<2>	10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<2>	10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_D_L<63..48>	10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_DINV_L<3>	10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<3>	10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<3>	10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_A_L<16..3>	10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	10 14
FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<0>	10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB_A_L<35..17>	10 14
FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<1>	10 14
CPU_IERR_L	CPU_55S		CPU_IERR_L	6 10
CPU_FERR_L	CPU_55S		CPU_FERR_L	6 10 23
CPU_PROCHOT_L	CPU_55S	CPU_2TO1	CPU_PROCHOT_L	6 10 42 52
CPU_PWRGD	CPU_55S		CPU_PWRGD	6 10 13 23
CPU_FROM_SB	CPU_55S		CPU_INTR	6 10 23
CPU_FROM_SB	CPU_55S		CPU_NMI	6 10 23
CPU_FROM_SB	CPU_55S		CPU_A20M_L	6 10 23
CPU_FROM_SB	CPU_55S		CPU_DPSLP_L	6 10 23
CPU_FROM_SB	CPU_55S		CPU_IGNNE_L	6 10 23
CPU_INIT_L	CPU_55S		CPU_INIT_L	6 10 23
CPU_FROM_SB	CPU_55S		CPU_SMI_L	6 10 23
CPU_FROM_SB	CPU_55S		CPU_STPCLK_L	6 10 23
PM_THRMTRIP_L	CPU_55S	CPU_2TO1	PM_THRMTRIP_L	6 10 16 23 42
FSB_CPUSLP_L	CPU_55S		FSB_CPUSLP_L	10 14
PM_DPRSLPVR	CPU_55S	CPU_2TO1	PM_DPRSLPVR	6 16 25 52
(See above)	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	6 52
CPU_BSEL0	CPU_55S	CPU_2TO1	CPU_BSEL<0>	6 10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<0>	6 7 13 16 30
CPU_BSEL1	CPU_55S	CPU_2TO1	CPU_BSEL<1>	6 10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<1>	6 7 13 16 30
CPU_BSEL2	CPU_55S	CPU_2TO1	CPU_BSEL<2>	6 10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<2>	6 7 13 16 30
CPU_DPRSTP_L	CPU_55S	CPU_2TO1	CPU_DPRSTP_L	6 10 16 23 52
CPU_GTLREF	CPU_55S	CPU_GTLREF	CPU_GTLREF	6 10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<3>	6 10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	6 10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<1>	6 10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	6 10
XDP_TDI	CPU_55S	CPU_ITP	XDP_TDI	6 7 10 13
XDP_TDO	CPU_55S	CPU_ITP	XDP_TDO	6 7 10 13
XDP_TMS	CPU_55S	CPU_ITP	XDP_TMS	6 7 10 13
XDP_TCK	CPU_55S	CPU_ITP	XDP_TCK	6 7 10 13
XDP_TRST_L	CPU_55S	CPU_ITP	XDP_TRST_L	6 7 10 13
XDP_BPM_L	CPU_55S	CPU_ITP	XDP_BPM_L<4..0>	6 7 10 13
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP_BPM_L<5>	6 7 10 13
	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	6 7 13 30 71
	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	6 7 13 30 71
(FSB_CPURST_L)	CPU_55S	CPU_ITP	XDP_CPURST_L	6 7 13
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	6 11 12 52
	CPU_55S	CPU_2TO1	IMVP6_VID<6..0>	12
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	6 11 52
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	6 11 52
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	6 52
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	6 52
	CPU_70D	CPU_THERMD	CPU_THERMD_P	6 10 46
	CPU_70D	CPU_THERMD	CPU_THERMD_N	6 10 46

CPU/FSB Constraints

SYNC_MASTER=T9 SYNC_DATE=01/30/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 100 OF 109	

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
PCIE_R2D_2_PCIE_R2D	*	0.228 MM	?
PCIE_D2R_2_PCIE_D2R	*	0.228 MM	?
PCIE_R2D_2_PCIE_D2R	*	0.300 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_N2S_2_DMI_N2S	*	0.228 MM	?
DMI_S2N_2_DMI_S2N	*	0.228 MM	?
DMI_N2S_2_DMI_S2N	*	0.300 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_R2D	PCIE_R2D	*	PCIE_R2D_2_PCIE_R2D
PCIE_D2R	PCIE_D2R	*	PCIE_D2R_2_PCIE_D2R
PCIE_R2D	PCIE_D2R	*	PCIE_R2D_2_PCIE_D2R

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_N2S	DMI_N2S	*	DMI_N2S_2_DMI_N2S
DMI_S2N	DMI_S2N	*	DMI_S2N_2_DMI_S2N
DMI_N2S	DMI_S2N	*	DMI_N2S_2_DMI_S2N

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_R2D	PWR	*	BUS2PWR_GND
PCIE_R2D	GND	*	BUS2PWR_GND
PCIE_D2R	PWR	*	BUS2PWR_GND
PCIE_D2R	GND	*	BUS2PWR_GND
DMI_N2S	PWR	*	BUS2PWR_GND
DMI_N2S	GND	*	BUS2PWR_GND
DMI_S2N	PWR	*	BUS2PWR_GND
DMI_S2N	GND	*	BUS2PWR_GND
LVDS	PWR	*	BUS2PWR_GND
LVDS	GND	*	BUS2PWR_GND
TMDS	PWR	*	BUS2PWR_GND
TMDS	GND	*	BUS2PWR_GND

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CRT_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TMDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	
LVDS	*	20 MIL	?	
CRT	*	25 MIL	?	DG Says 40 mil spacing minimum
CRT_2CRT	*	20 MIL	?	
CRT_SYNC	*	25 MIL	?	DG Says 30 mil spacing minimum
CRT_SYNC2SYNC	*	20 MIL	?	
TVDAC	*	25 MIL	?	DG Says 40 mil spacing minimum
TVDAC_2TVDAC	*	20 MIL	?	
LVDS2LVDS	*	0.300 MM	?	
TMDS	*	20 MIL	?	

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT
CRT_SYNC	CRT_SYNC	*	CRT_SYNC2SYNC
TVDAC	TVDAC	*	TVDAC_2TVDAC
LVDS	LVDS	*	LVDS2LVDS

LVDS signals are 100-ohm +/- 20% differential impedence.
CRT & TVDAC signal single-ended impedence varies by location:
- 37.5-ohm +/- 15% from GMCH to first termination resistor.
- 50-ohm +/- 15% from first to second termination resistor.
- 55-ohm +/- 15% from second termination resistor to connector.
CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedence.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PEG_R2D	PCIE_100D	PCIE_R2D	PEG_R2D_P<15..0>	
	PCIE_100D	PCIE_R2D	PEG_R2D_N<15..0>	
	PCIE_100D	PCIE_R2D	PEG_R2D_C_P<15..0>	6 9 15 61
	PCIE_100D	PCIE_R2D	PEG_R2D_C_N<15..0>	6 9 15 61
PEG_D2R	PCIE_100D	PCIE_D2R	PEG_D2R_P<15..0>	6 9 15 61
	PCIE_100D	PCIE_D2R	PEG_D2R_N<15..0>	6 9 15 61
	PCIE_100D	PCIE_D2R	PEG_D2R_C_P<15..0>	
	PCIE_100D	PCIE_D2R	PEG_D2R_C_N<15..0>	
DMI_N2S	DMI_100D	DMI_N2S	DMI_N2S_P<3..0>	6 16 24
	DMI_100D	DMI_N2S	DMI_N2S_N<3..0>	6 16 24
DMI_S2N	DMI_100D	DMI_S2N	DMI_S2N_P<3..0>	6 16 24
	DMI_100D	DMI_S2N	DMI_S2N_N<3..0>	6 16 24
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_P	6 15 60
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_N	6 15 60
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_P<2..0>	6 7 15 60
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_N<2..0>	6 7 15 60
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_F_P<2..0>	6 60
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_F_N<2..0>	6 60
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS_A_DATA_P<3>	9
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS_A_DATA_N<3>	9
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_P	9 15
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_N	9 15
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_P<2..0>	9 15
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_N<2..0>	9 15
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS_B_DATA_P<3>	9
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS_B_DATA_N<3>	9
LVDS_IBG		LVDS	LVDS_IBG	6 15 60
CRT_TVO_IREF		CRT	CRT_TVO_IREF	6 63
CRT_RED	CRT_50S	CRT	CRT_RED	6 63
CRT_GREEN	CRT_50S	CRT	CRT_GREEN	6 63
CRT_BLUE	CRT_50S	CRT	CRT_BLUE	6 63
CRT_SYNC	CRT_55S	CRT_SYNC	CRT_HSYNC_R	6 63
CRT_SYNC	CRT_55S	CRT_SYNC	CRT_VSYNC_R	6 63
TV_A_DAC	CRT_50S	TVDAC	TV_A_DAC	6 63
TV_B_DAC	CRT_50S	TVDAC	TV_B_DAC	6 63
TV_C_DAC	CRT_50S	TVDAC	TV_C_DAC	6 63
EXT_COMPVID_B	CRT_50S	CRT	EXT_COMPVID_B	6 63
EXT_Y_G	CRT_50S	CRT	EXT_Y_G	6 63
EXT_C_R	CRT_50S	CRT	EXT_C_R	6 63
VGA_R	CRT_50S	CRT	VGA_R	6 7 37 63
VGA_G	CRT_50S	CRT	VGA_G	6 7 37 63
VGA_B	CRT_50S	CRT	VGA_B	6 7 37 63
	PCIE_100D	PCIE_R2D	TMDS_SDB_P	6 61
	PCIE_100D	PCIE_R2D	TMDS_SDB_N	6 61
	PCIE_100D	PCIE_R2D	TMDS_SDC_P	6 61
	PCIE_100D	PCIE_R2D	TMDS_SDC_N	6 61
	PCIE_100D	PCIE_R2D	TMDS_SDG_P	6 61
	PCIE_100D	PCIE_R2D	TMDS_SDG_N	6 61
	PCIE_100D	PCIE_R2D	TMDS_SDR_P	6 61
	PCIE_100D	PCIE_R2D	TMDS_SDR_N	6 61
	TMDS_100D	TMDS	TMDS_TX_CLK_P	6 61 63
	TMDS_100D	TMDS	TMDS_TX_CLK_N	6 61 63
	PCIE_100D	PCIE_D2R	TMDS_INT_P	6 61
	PCIE_100D	PCIE_D2R	TMDS_INT_N	6 61
	TMDS_100D	TMDS	TMDS_TX_CONN_CLK_P	6 7 37 63
	TMDS_100D	TMDS	TMDS_TX_CONN_CLK_N	6 7 37 63
	TMDS_100D	TMDS	TMDS_CONN_P<3..0>	
	TMDS_100D	TMDS	TMDS_CONN_N<3..0>	
	TMDS_100D	TMDS	TMDS_TX_P<3..0>	6 61 63
	TMDS_100D	TMDS	TMDS_TX_N<3..0>	6 61 63
	SMB_55S	SMB	TMDS_DDC_SCL	6 7 37 61 62 63
	SMB_55S	SMB	TMDS_DDC_SDA	6 7 37 61 62 63

NB Constraints

SYNC_MASTER=T9 SYNC_DATE=01/30/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 101 OF 109	

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	ISL3,ISL10	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_87D	*	=87_OHM_DIFF	=87_OHM_DIFF	=87_OHM_DIFF	=87_OHM_DIFF	=87_OHM_DIFF	=87_OHM_DIFF
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=2.28:1_SPACING	?
MEM_CTRL2CTRL	*	=1:1_SPACING	?
MEM_CTRL2MEM	*	=2.28:1_SPACING	?
MEM_CMD2CMD	*	=1:1_SPACING	?
MEM_CMD2MEM	*	=2.28:1_SPACING	?
MEM_DATA2DATA	*	=1:1_SPACING	?
MEM_DATA2MEM	*	=2.28:1_SPACING	?
MEM_DQS2MEM	*	=2.28:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PP1V8_MEM	*	PWR_P2MM
MEM_CTRL	PP1V8_MEM	*	PWR_P2MM
MEM_DATA	PP1V8_MEM	*	PWR_P2MM
MEM_DQS	PP1V8_MEM	*	PWR_P2MM
MEM_CMD	PP1V8_MEM	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	NB_STATIC	*	PWR_P2MM
MEM_CTRL	NB_STATIC	*	PWR_P2MM
MEM_DATA	NB_STATIC	*	PWR_P2MM
MEM_DQS	NB_STATIC	*	PWR_P2MM
MEM_CMD	NB_STATIC	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

Need to support MEM_*-style wildcards!

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	PWR	*	BUS2PWR_GND
MEM_CLK	GND	*	BUS2PWR_GND
MEM_CTRL	PWR	*	BUS2PWR_GND
MEM_CTRL	GND	*	BUS2PWR_GND
MEM_CMD	PWR	*	BUS2PWR_GND
MEM_CMD	GND	*	BUS2PWR_GND
MEM_DATA	PWR	*	BUS2PWR_GND
MEM_DATA	GND	*	BUS2PWR_GND
MEM_DQS	PWR	*	BUS2PWR_GND
MEM_DQS	GND	*	BUS2PWR_GND

R93	PP0V9_S3M_MEM_NBVREFB	NET_SPACING_TYPE=NB_STATIC 8 16 21
R95	PP0V9_S3M_MEM_NBVREFA	NET_SPACING_TYPE=NB_STATIC 8 16 21
R94	NB_VCCSM_LF1	NET_SPACING_TYPE=NB_STATIC 6 18
R96	NB_VCCSM_LF2	NET_SPACING_TYPE=NB_STATIC 6 18
R97	NB_VCCSM_LF3	NET_SPACING_TYPE=NB_STATIC 6 18
R98	NB_VCCSM_LF4	NET_SPACING_TYPE=NB_STATIC 6 18
R99	NB_VCCSM_LF5	NET_SPACING_TYPE=NB_STATIC 6 18
R100	NB_VCCSM_LF6	NET_SPACING_TYPE=NB_STATIC 6 18
R101	NB_VCCSM_LF7	NET_SPACING_TYPE=NB_STATIC 6 18
R102	=PP1V8_S3M_MEM_NB	NET_SPACING_TYPE=PP1V8_MEM 8 16 18 21
	GND	NET_SPACING_TYPE=GND

Memory Net Properties

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
	MEM_87D	MEM_CLK	MEM_CLK_P<2..0> 16 31 33
	MEM_87D	MEM_CLK	MEM_CLK_N<2..0> 16 31 33
	MEM_45S	MEM_CTRL	MEM_CKE<1..0> 16 31 33
	MEM_45S	MEM_CTRL	MEM_CS_L<1..0> 16 31 33
	MEM_45S	MEM_CTRL	MEM_ODT<1..0> 6 16 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_A<13..0> 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_BS<2..0> 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_RAS_L 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_CAS_L 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_WE_L 17 31 33
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_A_DQ<7..0> 17 31
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A_DQ<15..8> 17 31
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_A_DQ<23..16> 17 31
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A_DQ<31..24> 17 31
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_A_DQ<39..32> 17 31
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_A_DQ<47..40> 17 31
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A_DQ<55..48> 17 31
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A_DQ<63..56> 17 31
MEM_A_DM0	MEM_55S	MEM_DATA	MEM_A_DM<0> 17 31
MEM_A_DM1	MEM_55S	MEM_DATA	MEM_A_DM<1> 17 31
MEM_A_DM2	MEM_55S	MEM_DATA	MEM_A_DM<2> 17 31
MEM_A_DM3	MEM_55S	MEM_DATA	MEM_A_DM<3> 17 31
MEM_A_DM4	MEM_55S	MEM_DATA	MEM_A_DM<4> 17 31
MEM_A_DM5	MEM_55S	MEM_DATA	MEM_A_DM<5> 17 31
MEM_A_DM6	MEM_55S	MEM_DATA	MEM_A_DM<6> 17 31
MEM_A_DM7	MEM_55S	MEM_DATA	MEM_A_DM<7> 17 31
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0> 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<0> 17 31
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1> 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<1> 17 31
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2> 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<2> 17 31
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3> 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<3> 17 31
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4> 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<4> 17 31
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5> 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<5> 17 31
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6> 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<6> 17 31
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7> 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<7> 17 31
	MEM_87D	MEM_CLK	MEM_CLK_P<5..3> 16 32 33
	MEM_87D	MEM_CLK	MEM_CLK_N<5..3> 16 32 33
	MEM_45S	MEM_CTRL	MEM_CKE<4..3> 16 32 33
	MEM_45S	MEM_CTRL	MEM_CS_L<3..2> 16 32 33
	MEM_45S	MEM_CTRL	MEM_ODT<3..2> 6 16 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_A<13..0> 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_BS<2..0> 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_RAS_L 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_CAS_L 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_WE_L 17 32 33
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B_DQ<7..0> 17 32
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_B_DQ<15..8> 17 32
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_B_DQ<23..16> 17 32
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B_DQ<31..24> 17 32
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B_DQ<39..32> 17 32
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B_DQ<47..40> 17 32
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_B_DQ<55..48> 17 32
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B_DQ<63..56> 17 32
MEM_B_DM0	MEM_55S	MEM_DATA	MEM_B_DM<0> 17 32
MEM_B_DM1	MEM_55S	MEM_DATA	MEM_B_DM<1> 17 32
MEM_B_DM2	MEM_55S	MEM_DATA	MEM_B_DM<2> 17 32
MEM_B_DM3	MEM_55S	MEM_DATA	MEM_B_DM<3> 17 32
MEM_B_DM4	MEM_55S	MEM_DATA	MEM_B_DM<4> 17 32
MEM_B_DM5	MEM_55S	MEM_DATA	MEM_B_DM<5> 17 32
MEM_B_DM6	MEM_55S	MEM_DATA	MEM_B_DM<6> 17 32
MEM_B_DM7	MEM_55S	MEM_DATA	MEM_B_DM<7> 17 32
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0> 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<0> 17 32
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1> 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<1> 17 32
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2> 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<2> 17 32
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3> 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<3> 17 32
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4> 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<4> 17 32
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5> 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<5> 17 32
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6> 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<6> 17 32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7> 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<7> 17 32

Memory Constraints

SYNC_MASTER=T9 SYNC_DATE=01/30/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 102 OF 109	

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_60S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	20 MIL	?
USB_2CLK	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	PWR	*	BUS2PWR_GND
USB	GND	*	BUS2PWR_GND

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
IDE_PDD	IDE_55S	IDE	IDE_PDD<15..0> 6 23 38
IDE_PDA	IDE_55S	IDE	IDE_PDA<2..0> 6 23 38
IDE_PDCS	IDE_55S	IDE	IDE_PDCS1_L 6 23 38
IDE_PDCS	IDE_55S	IDE	IDE_PDCS3_L 6 23 38
IDE_CNTL	IDE_55S	IDE	IDE_PDIOW_L 6 23 38
IDE_PDIOR_L	IDE_55S	IDE	IDE_PDIOR_L 6 23 38
IDE_CNTL	IDE_55S	IDE	IDE_PDDACK_L 6 23 38
IDE_CNTL	IDE_55S	IDE	IDE_PDDREQ 6 23 38
IDE_PDIORDY	IDE_55S	IDE	IDE_PDIORDY 6 23 38
IDE_IRQ14	IDE_55S	IDE	IDE_IRQ14 6 23 38
IDE_RST_L	IDE_55S	IDE	ODD_RST_5VTOL_L
SATA_A_R2D	SATA_100D	SATA	SATA_A_R2D_C_P 9 23
	SATA_100D	SATA	SATA_A_R2D_C_N 9 23
	SATA_100D	SATA	SATA_A_R2D_P
	SATA_100D	SATA	SATA_A_R2D_N
SATA_A_D2R	SATA_100D	GND	SATA_A_D2R_P 9
	SATA_100D	GND	SATA_A_D2R_N 9
	SATA_100D	SATA	SATA_A_D2R_C_P
	SATA_100D	SATA	SATA_A_D2R_C_N
SATA_B_R2D	SATA_100D	SATA	SATA_B_R2D_C_P 9 23
	SATA_100D	SATA	SATA_B_R2D_C_N 9 23
	SATA_100D	SATA	SATA_B_R2D_P
	SATA_100D	SATA	SATA_B_R2D_N
SATA_A_D2R	SATA_100D	GND	SATA_B_D2R_P 9
	SATA_100D	GND	SATA_B_D2R_N 9
	SATA_100D	SATA	SATA_B_D2R_C_P
	SATA_100D	SATA	SATA_B_D2R_C_N
SATA_C_R2D	SATA_100D	SATA	SATA_C_R2D_C_P 9 23
	SATA_100D	SATA	SATA_C_R2D_C_N 9 23
	SATA_100D	SATA	SATA_C_R2D_P
	SATA_100D	SATA	SATA_C_R2D_N
SATA_A_D2R	SATA_100D	GND	SATA_C_D2R_P 9
	SATA_100D	GND	SATA_C_D2R_N 9
	SATA_100D	SATA	SATA_C_D2R_C_P
	SATA_100D	SATA	SATA_C_D2R_C_N
SATA_RBIAS	SATA_55S		SATA_RBIAS
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK 6 9 23
	HDA_55S	HDA	HDA_BIT_CLK_R 6 23
HDA_SYNC	HDA_55S	HDA	HDA_SYNC 6 7 9 23 37
	HDA_55S	HDA	HDA_SYNC_R 6 23
HDA_RST_L	HDA_55S	HDA	HDA_RST_L 6 9 23 37
	HDA_55S	HDA	HDA_RST_L_R 6 23
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0 6 9 23
	HDA_55S	HDA	HDA_SDIN_CODEC
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT 6 9 23
	HDA_55S	HDA	HDA_SDOUT_R 6 23
USB_EXTA	USB_90D	USB	USB_EXTA_P 9 24
	USB_90D	USB	USB_EXTA_N 9 24
	USB_90D	USB	USB_EXTA_MUXED_P 9
	USB_90D	USB	USB_EXTA_MUXED_N 9
USB_MINI	USB_90D	USB	USB_MINI_P 9 24
	USB_90D	USB	USB_MINI_N 9 24
USB_EXTD	USB_90D	USB	USB_EXTD_P 9 24
	USB_90D	USB	USB_EXTD_N 9 24
USB_CAMERA	USB_90D	USB	USB_CAMERA_P 9 24
	USB_90D	USB	USB_CAMERA_N 9 24
USB_BT	USB_90D	USB	USB_BT_P 9 24
	USB_90D	USB	USB_BT_N 9 24
USB_TPAD	USB_90D	USB	USB_TPAD_P 9 24
	USB_90D	USB	USB_TPAD_N 9 24
USB_IR	USB_90D	USB	USB_IR_P 6 9 24
	USB_90D	USB	USB_IR_N 6 9 24
USB_EXTB	USB_90D	USB	USB_EXTB_P 9 24
	USB_90D	USB	USB_EXTB_N 9 24
USB_EXCARD	USB_90D	USB	USB_EXCARD_P 9 24
	USB_90D	USB	USB_EXCARD_N 9 24
USB_EXTC	USB_90D	USB	USB_EXTC_P 9 24
	USB_90D	USB	USB_EXTC_N 9 24
	USB_90D	USB	USB2_AIRPORT_P_F 6 36
	USB_90D	USB	USB2_AIRPORT_N_F 6 36
	USB_90D	USB	USB2_CAMERA_F_P 6 7 60
	USB_90D	USB	USB2_CAMERA_F_N 6 7 60
	USB_90D	USB	USB2_EXTA_F_P 6 7 37 39
	USB_90D	USB	USB2_EXTA_F_N 6 7 37 39
			USB2_3G_F_P
			USB2_3G_F_N
USB_RBIAS	USB_60S		USB_RBIAS 6 24
SMB_SB_SCL	SMB_55S	SMB	SMB_CLK 25 44
SMB_SB_SDA	SMB_55S	SMB	SMB_DATA 25 44
SMB_SB_ME_SCL	SMB_55S	SMB	SMB_ME_CLK 25 44
SMB_SB_ME_SDA	SMB_55S	SMB	SMB_ME_DATA 25 44
SPI_SCLK	SPI_55S	SPI	SPI_SCLK_R 6 24 49
	SPI_55S	SPI	SPI_SCLK
	SPI_55S	SPI	SPI_A_SCLK_R 6 43 49
	SPI_55S	SPI	SPI_B_SCLK_R
SPI_SI	SPI_55S	SPI	SPI_SI_R 6 24 49
	SPI_55S	SPI	SPI_SI
	SPI_55S	SPI	SPI_A_SI_R 6 43 49
	SPI_55S	SPI	SPI_B_SI_R
SPI_SO	SPI_55S	SPI	SPI_SO 6 24 43 49
	SPI_55S	SPI	SPI_A_SO_R 6 49
	SPI_55S	SPI	SPI_B_SO
	SPI_55S	SPI	SPI_B_SO_R
SPI_CE_L0	SPI_55S	SPI	SPI_CE_R_L<0> 6 24 49
	SPI_55S	SPI	SPI_CE_L<0> 6 43 49
SPI_CE_L1	SPI_55S	SPI	SPI_CE_R_L<1> 6 24 43
	SPI_55S	SPI	SPI_CE_L<1>

SB Constraints (1 of 2)

SYNC_MASTER=T9 SYNC_DATE=01/30/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J
SCALE: NONE	SHT 103 OF 109	

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?
PCIE_R2D	*	=PCIE	?
PCIE_D2R	*	=PCIE	?
PCIE_9MIL	*	0.228 MM	?
PCIE_12MIL	*	0.300 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_R2D	PCIE_R2D	*	PCIE_9MIL
PCIE_D2R	PCIE_D2R	*	PCIE_9MIL
PCIE_D2R	PCIE_R2D	*	PCIE_12MIL

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Platform LAN (Nineveh) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LAN_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
GLAN_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_CLK	*	=2.5:1_SPACING	?
ENET_GLAN	*	20 MILS	?
ENET_LAN	*	=1.5:1_SPACING	?
ENET_MDI	*	25 MILS	?

DG says 30 mils min separation.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Controller Link (AMT) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLINK_12MIL	*	=STANDARD	12 MILS	5 MILS	300 MILS	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLINK	*	=1.8:1_SPACING	?
CLINK_VREF	*	12 MILS	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
PCI_AD	PCI_55S	PCI	PCI_AD<18..0> 9 24
PCI_AD19	PCI_55S	PCI	PCI_AD<19> 9 24
PCI_AD20	PCI_55S	PCI	PCI_AD<20> 9 24
PCI_AD	PCI_55S	PCI	PCI_AD<31..21> 9 24
PCI_AD	PCI_55S	PCI	PCI_PAR 9 24
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0> 9 24
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L 6 24
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L 6 24
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L 6 24
PCI_LOCK_L	PCI_55S	PCI	PCI_LOCK_L 6 24
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L 6 24
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L 6 24
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L 6 24
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L 6 24
PCI_FW_REQ_L	PCI_55S	PCI	PCI_FW_REQ_L 6 24
PCI_FW_GNT_L	PCI_55S	PCI	PCI_FW_GNT_L 6 24
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L 6 24
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L
PCI_REQ2_L	PCI_55S	PCI	PCI_REQ2_L 6 24
PCI_GNT2_L	PCI_55S	PCI	PCI_GNT2_L
INT_PIRQA_L	PCI_55S	PCI	INT_PIRQA_L 6 24
INT_PIRQB_L	PCI_55S	PCI	INT_PIRQB_L 6 24
INT_PIRQC_L	PCI_55S	PCI	INT_PIRQC_L 6 24
INT_PIRQD_L	PCI_55S	PCI	INT_PIRQD_L 6 24
INT_PIRQE_L	PCI_55S	PCI	INT_PIRQE_L 6 24
INT_PIRQF_L	PCI_55S	PCI	INT_PIRQF_L 6 24
PCIE_A_R2D	PCIE_100D	PCIE_R2D	PCIE_A_R2D_C_P
	PCIE_100D	PCIE_R2D	PCIE_A_R2D_C_N
PCIE_A_D2R	PCIE_100D	PCIE_D2R	PCIE_A_D2R_P
	PCIE_100D	PCIE_D2R	PCIE_A_D2R_N
PCIE_B_R2D	PCIE_100D	PCIE_R2D	PCIE_B_R2D_C_P
	PCIE_100D	PCIE_R2D	PCIE_B_R2D_C_N
PCIE_B_D2R	PCIE_100D	PCIE_D2R	PCIE_B_D2R_P
	PCIE_100D	PCIE_D2R	PCIE_B_D2R_N
			PCIE_EXCARD_R2D_C_P
			PCIE_EXCARD_R2D_C_N
			PCIE_EXCARD_D2R_P
			PCIE_EXCARD_D2R_N
			PCIE_FW_R2D_C_P
			PCIE_FW_R2D_C_N
			PCIE_FW_D2R_P
			PCIE_FW_D2R_N
PCIE_MINI_R2D	PCIE_100D	PCIE_R2D	PCIE_MINI_R2D_C_P 24 36
	PCIE_100D	PCIE_R2D	PCIE_MINI_R2D_C_N 24 36
PCIE_MINI_D2R	PCIE_100D	PCIE_D2R	PCIE_MINI_D2R_P 24 36
	PCIE_100D	PCIE_D2R	PCIE_MINI_D2R_N 24 36
			PCIE_ENET_R2D_C_P
			PCIE_ENET_R2D_C_N
			PCIE_ENET_D2R_P
			PCIE_ENET_D2R_N
GLAN_COMP			GLAN_COMP 6 23
ENET_KBIAS			NINEVEH_KBIAS_P
ENET_RBIAS			NINEVEH_RBIAS
(PCIE_ENET_R2D)	GLAN_100D	ENET_GLAN	ENET_GLAN_R2D_P
	GLAN_100D	ENET_GLAN	ENET_GLAN_R2D_N
(PCIE_ENET_D2R)	GLAN_100D	ENET_GLAN	ENET_GLAN_D2R_C_P
	GLAN_100D	ENET_GLAN	ENET_GLAN_D2R_C_N
ENET_LAN	LAN_55S	ENET_LAN	LAN_RSTSYNC
ENET_LAN	LAN_55S	ENET_LAN	LAN_R2D<2..0>
ENET_LAN	LAN_55S	ENET_LAN	LAN_D2R<2..0>
ENET_GLAN_CLK	LAN_55S	ENET_CLK	ENET_GLAN_CLK_R
	LAN_55S	ENET_CLK	ENET_GLAN_CLK
ENET_MDI0	ENET_100D	ENET_MDI	ENET_MDI_P<0>
	ENET_100D	ENET_MDI	ENET_MDI_N<0>
ENET_MDI1	ENET_100D	ENET_MDI	ENET_MDI_P<1>
	ENET_100D	ENET_MDI	ENET_MDI_N<1>
ENET_MDI2	ENET_100D	ENET_MDI	ENET_MDI_P<2>
	ENET_100D	ENET_MDI	ENET_MDI_N<2>
ENET_MDI3	ENET_100D	ENET_MDI	ENET_MDI_P<3>
	ENET_100D	ENET_MDI	ENET_MDI_N<3>
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_CLK 6 16 25
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_DATA 6 16 25
CLINK_NB_RESET_L	CLINK_55S	CLINK	CLINK_NB_RESET_L 6 16 25
CLINK_WLAN	CLINK_55S	CLINK	CLINK_WLAN_CLK
CLINK_WLAN	CLINK_55S	CLINK	CLINK_WLAN_DATA
CLINK_WLAN_RESET_L	CLINK_55S	CLINK	CLINK_WLAN_RESET_L
NB_CLINK_VREF	CLINK_12MIL	CLINK_VREF	NB_CLINK_VREF 6 16
SB_CLINK_VREF0	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF0 6 25
SB_CLINK_VREF1	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF1 6 25

SB Constraints (2 of 2)

SYNC_MASTER=T9 SYNC_DATE=01/30/2007

APPLE INC.

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Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	PWR	*	BUS2PWR_GND
CLK_FSB	GND	*	BUS2PWR_GND
CLK_PCIE	PWR	*	BUS2PWR_GND
CLK_PCIE	GND	*	BUS2PWR_GND
CLK_MED	PWR	*	BUS2PWR_GND
CLK_MED	GND	*	BUS2PWR_GND

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CK505_CPU	CLK_FSB_100D	CLK_FSB	CK505_CPU0_P	29 30
CK505_CPU	CLK_FSB_100D	CLK_FSB	CK505_CPU0_N	29 30
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_P	29 30
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_N	29 30
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_P	29 30
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_N	29 30
CK505_PCIF0	CLK_MED_55S	CLK_MED	CK505_PCIF0_CLK_ITPEN	
CK505_PCIF1	CLK_MED_55S	CLK_MED	CK505_PCIF1_CLK	6 29 30
CK505_PCI1	CLK_MED_55S	CLK_MED	CK505_PCI1_CLK	
CK505_PCI2	CLK_MED_55S	CLK_MED	CK505_PCI2_CLK	
CK505_PCI3	CLK_MED_55S	CLK_MED	CK505_PCI3_CLK	6 29 30
CK505_PCI4	CLK_MED_55S	CLK_MED	CK505_PCI4_CLK	
CK505_PCI5	CLK_MED_55S	CLK_MED	CK505_PCI5_CLK_FCTSEL	
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_48M_FSA	
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_REF0_FSC	
CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_N	29 30
CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_N	29 30
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_P	
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_N	
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_N	29 30
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_P	
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_N	
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_P	
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_N	
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_N	29 30
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_N	29 30
CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_P	
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_N	
CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_P	
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_N	
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	6 10 30
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	6 10 30
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_P	6 14 30
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_N	6 14 30
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	6 7 13 30 66
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	6 7 13 30 66
(CK505_PCIF0)	CLK_MED_55S	CLK_MED	PCI_CLK33M_LPCPLUS	6 30 43
(CK505_PCIF1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SB	6 24 30
(CK505_PCI1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_FW	
(CK505_PCI2)	CLK_MED_55S	CLK_MED	PCI_CLK33M_TPM	
(CK505_PCI3)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SMC	6 30 41
			CK505 PCI4 is project-specific	
			CK505 PCI5 is project-specific	
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	SB_CLK48M_USBCTLR	6 25 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	SB_CLK14P3M_TIMER	6 25 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_FSA	6 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_FSC	6 30
(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_P	6 9 30
(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_N	6 9 30
(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_P	6 9 30
(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_N	6 9 30
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P	
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N	
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_P	6 24 30
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_N	6 24 30
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	
(CK505_SRC4)	SATA_100D	GND	SB_CLK100M_SATA_P	
(CK505_SRC4)	SATA_100D	GND	SB_CLK100M_SATA_N	
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_P	6 16 30
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_N	6 16 30
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	6 30 36
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	6 30 36
			CK505 SRC7 is project-specific	
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P	
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N	

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	6 44
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	6 44
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	
SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	6 7 44
SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	6 7 44
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	6 7 44
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	6 7 44
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	6 44
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	6 44

Clock & SMC Constraints

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1	PPBUS_G3H	NET_SPACING_TYPE=PWR	6 7 8
2	PPBUS_R_G3H	NET_SPACING_TYPE=PWR	6 7 8
3	PPDCIN_G3H	NET_SPACING_TYPE=PWR	6 7 8
4	PPDCIN_G3H_R	NET_SPACING_TYPE=PWR	6 50
5	PPVBATT_G3H_R	NET_SPACING_TYPE=PWR	6 50
6	PPVBAT_G3H_CHGR_OUT	NET_SPACING_TYPE=PWR	6 59
7	PPVBAT_G3H_CHGR_REG	NET_SPACING_TYPE=PWR	6 59
8	PPVBAT_G3H_CHRGR_REG_R	NET_SPACING_TYPE=PWR	6 59
9	PPVBAT_G3H_CHRGR_REG_0	NET_SPACING_TYPE=PWR	6 59
10	PPVCORE_S0_CPU	NET_SPACING_TYPE=PWR	6 7 8
11	PPVCORE_S0_NB_GFX	NET_SPACING_TYPE=PWR	6 7 8
12	PPVDCIN_G3H_PRE	NET_SPACING_TYPE=PWR	6 45 59
13	PPVDCIN_G3H_PRE_R	NET_SPACING_TYPE=PWR	6 59
14	PPVDCIN_G3H_PRE_0	NET_SPACING_TYPE=PWR	6 59
15	PPVDCIN_G3H_PRE2	NET_SPACING_TYPE=PWR	6 59
16	PPVIN_S5_IMVP6_VIN	NET_SPACING_TYPE=PWR	6 52
17	PPVOUT_S0_LCDBKLT	NET_SPACING_TYPE=PWR	6 7 60 64
18	PPVOUT_S0_LCDBKLT_SW	NET_SPACING_TYPE=PWR	6 64
19	PP0V9_S0	NET_SPACING_TYPE=PWR	6 7 8
21	PP0V9_S3	NET_SPACING_TYPE=PWR	6 8
20	PP1V5_S0	NET_SPACING_TYPE=PWR	6 7 8
23	PP1V5_S0_NB_QDAC	NET_SPACING_TYPE=PWR	6 22
100	PP1V5_S0_NB_VCCD_CRT	NET_SPACING_TYPE=PWR	6 22
101	PP1V5_S0_NB_VCCD_QDAC	NET_SPACING_TYPE=PWR	6 19 22
22	PP1V5_S0_NB_VCCDMIPLL	NET_SPACING_TYPE=PWR	
24	PP1V5_S0_NB_VCCDMIPLL_F	NET_SPACING_TYPE=PWR	
25	PP1V5_S0_SB_VCCDMIPLL	NET_SPACING_TYPE=PWR	6 26 27
26	PP1V5_S0_SB_VCCDMIPLL_F	NET_SPACING_TYPE=PWR	6 27
28	PP1V5_S0_SB_VCCSATAPLL	NET_SPACING_TYPE=PWR	6 26 27
27	PP1V5_S0_SB_VCC1_5_B	NET_SPACING_TYPE=PWR	6 23 24 26 27
30	PP1V8_S0	NET_SPACING_TYPE=PWR	6 7 8
29	PP1V8_S0_ANALOG_SDVO_F	NET_SPACING_TYPE=PWR	6 61
31	PP1V8_S0_ANALOG_TMDS_F	NET_SPACING_TYPE=PWR	6 61
33	PP1V8_S0_NB_VCCTXLVDS	NET_SPACING_TYPE=PWR	6 19 22
32	PP1V8_S0_PVCC1_TMDS_F	NET_SPACING_TYPE=PWR	6 61
35	PP1V8_S0_PVCC2_TMDS_F	NET_SPACING_TYPE=PWR	6 61
34	PP1V8_S0_TMDS_F	NET_SPACING_TYPE=PWR	6 61
36	PP1V8_S3		6 7 8
38	PP1V8_S3M_NB_VCCSMCK	NET_SPACING_TYPE=PWR	6 19 21
37	PP1V8_S3_NB_VCCSMCK_RC	NET_SPACING_TYPE=PWR	6 21
39	PP1V05_S0	NET_SPACING_TYPE=PWR	6 7 8
41	PP1V05_S0_NB_VCCPEG	NET_SPACING_TYPE=PWR	6 15 19 21
40	PP1V25_S0	NET_SPACING_TYPE=PWR	6 7 8
43	PP1V25_S0M_NB_VCCA_HPLL	NET_SPACING_TYPE=PWR	6 19 21
42	PP1V25_S0_NB_DPLL	NET_SPACING_TYPE=PWR	6 22
44	PP1V25_S0_NB_PEGPLL	NET_SPACING_TYPE=PWR	6 19 21
46	PP1V25_S0_NB_PEGPLL_RC	NET_SPACING_TYPE=PWR	6 21
45	PP1V25_S0_NB_VCCA_DPLLA	NET_SPACING_TYPE=PWR	6 19 22
48	PP1V25_S0_NB_VCCA_DPLLB	NET_SPACING_TYPE=PWR	6 19 22
47	PP3V3_LCDVDD_SW	NET_SPACING_TYPE=PWR	6 60
49	PP3V3_LCDVDD_SW_F	NET_SPACING_TYPE=PWR	6 7 60
50	PP3V3_S0	NET_SPACING_TYPE=PWR	7
52	PP3V3_S0_ANALOG_SDVO_F	NET_SPACING_TYPE=PWR	6 61
51	PP3V3_S0_CK505_VDDA	NET_SPACING_TYPE=PWR	6
54	PP3V3_S0_CK505_VDDA_R	NET_SPACING_TYPE=PWR	6
53	PP3V3_S0_CK505_VDD_CPU_SRC	NET_SPACING_TYPE=PWR	6 29
55	PP3V3_S0_CK505_VDD_PCI	NET_SPACING_TYPE=PWR	6
57	PP3V3_S0_CK505_VDD_REF	NET_SPACING_TYPE=PWR	6
56	PP3V3_S0_CK505_VDD48	NET_SPACING_TYPE=PWR	6
59	PP3V3_S0_IMVP6_3V3	NET_SPACING_TYPE=PWR	6 52
58	PP3V3_S0_LCD_F	NET_SPACING_TYPE=PWR	6 7 60
60	PP3V3_S0_NBCORE_FOLLOW_R	NET_SPACING_TYPE=PWR	6 21
62	PP3V3_S0_NB_CRTDAC_F	NET_SPACING_TYPE=PWR	6 22
61	PP3V3_S0_NB_TVDAC	NET_SPACING_TYPE=PWR	6 22
63	PP3V3_S0_NB_TVDAC_F	NET_SPACING_TYPE=PWR	6 22
65	PP3V3_S0_NB_TVDAC_FOLLOW	NET_SPACING_TYPE=PWR	6 22
64	PP3V3_S0_NB_VCCA_CRTDAC	NET_SPACING_TYPE=PWR	6 19 22
67	PP3V3_S0_NB_VCCA_DAC_BG	NET_SPACING_TYPE=PWR	6 19 22
66	PP3V3_S0_NB_VCCA_TVDACA	NET_SPACING_TYPE=PWR	6 19 22
68	PP3V3_S0_NB_VCCA_TVDACB	NET_SPACING_TYPE=PWR	6 19 22
70	PP3V3_S0_NB_VCCA_TVDACC	NET_SPACING_TYPE=PWR	6 19 22
69	PP3V3_S0_SPVCC_TMDS_F	NET_SPACING_TYPE=PWR	6 61
72	PP3V3_S3	NET_SPACING_TYPE=PWR	6 7 8
71	PP3V3_S3_AP_AUX	NET_SPACING_TYPE=PWR	6 7 36
73	PP3V3_S3_TOPCASE_F	NET_SPACING_TYPE=PWR	
74	PP3V3_S5	NET_SPACING_TYPE=PWR	6 7 8
76	PP3V3_S5_AVREF_SMC	NET_SPACING_TYPE=PWR	6 41 42
75	PP3V3_S5_SMC_AVCC	NET_SPACING_TYPE=PWR	6 41
78	PP3V42G3H_SW	NET_SPACING_TYPE=PWR	6 57
77	PP3V42_G3H	NET_SPACING_TYPE=PWR	6 7 8
79	PP3V42_G3H_SMC_F	NET_SPACING_TYPE=PWR	
81	PP3V42_G3H_SMCUSBMUX_R	NET_SPACING_TYPE=PWR	6 39
80	PP4V5_AUDIO_ANALOG	NET_SPACING_TYPE=PWR	
83	PP5V_S0	NET_SPACING_TYPE=PWR	6 7 8
82	PP5V_S0_AUDIO	NET_SPACING_TYPE=PWR	
84	PP5V_S0_AUDIO_AMP	NET_SPACING_TYPE=PWR	
86	PP5V_S0_DVIPORT	NET_SPACING_TYPE=PWR	6 7 37 63
85	PP5V_S0_DVIPORT_D	NET_SPACING_TYPE=PWR	6 63
87	PP5V_S0_IMVP6_VDD	NET_SPACING_TYPE=PWR	6 52
89	PP5V_S0_KBDLED_F	NET_SPACING_TYPE=PWR	6 7 40
88	PP5V_S0_SB_V5REF	NET_SPACING_TYPE=PWR	6 26 27
91	PP5V_S0_TMDS_FUSE	NET_SPACING_TYPE=PWR	6 63
90	PP5V_S0_3G_F	NET_SPACING_TYPE=PWR	
92	PP5V_S3	NET_SPACING_TYPE=PWR	6 7 8
94	PP5V_S3_CAMERA_F	NET_SPACING_TYPE=PWR	6 7 40
93	PP5V_S3_IR_F	NET_SPACING_TYPE=PWR	
96	PP5V_S3_USB2_EXTA	NET_SPACING_TYPE=PWR	6 39
95	PP5V_S3_USB2_EXTA_F	NET_SPACING_TYPE=PWR	6 7 37 39
97	PP5V_S5	NET_SPACING_TYPE=PWR	6 7 8
98	PP5V_S5_SB_V5REF_SUS	NET_SPACING_TYPE=PWR	6 26 27
99	PP18V5_DCIN	NET_SPACING_TYPE=PWR	6 7 50
102	PP18V5_DCIN_ONEWIRE	NET_SPACING_TYPE=PWR	6 50
103	PP18V5_G3H	NET_SPACING_TYPE=PWR	6 7 8
104	PP18V5_S5_CHGR_SW_R	NET_SPACING_TYPE=PWR	6 59

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PWR	*	=STANDARD	?
BUS2PWR_GND	*	0.228 MM	?

M82 Power and Ground Nets

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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M82 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,ISL12,ISL13,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.100 MM	0.076 MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
27P4_OHM_SE	ISL2,ISL4,ISL5	Y	0.215 MM	0.215 MM			
27P4_OHM_SE	ISL10,ISL11,ISL13	Y	0.215 MM	0.215 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	TOP,BOTTOM	Y	0.290 MM	0.290 MM			
45_OHM_SE	ISL2,ISL4,ISL5	Y	0.091 MM	0.091 MM			
45_OHM_SE	ISL10,ISL11,ISL13	Y	0.091 MM	0.091 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.235 MM	0.235 MM			
50_OHM_SE	ISL2,ISL4,ISL5	Y	0.070 MM	0.070 MM			
50_OHM_SE	ISL10,ISL11,ISL13	Y	0.070 MM	0.070 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.190 MM	0.190 MM			
55_OHM_SE	ISL2,ISL4,ISL5	Y	0.070 MM	0.070 MM	55OHM SE ON INTERNAL LAYERS NOT ACHIEVABLE IN M82 STACKUP USING 50OHM SE		
55_OHM_SE	ISL10,ISL11,ISL13	Y	0.070 MM	0.070 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	TOP,BOTTOM	Y	0.310 MM	0.310 MM		0.130 MM	0.130 MM
70_OHM_DIFF	ISL2,ISL4,ISL5	Y	0.132 MM	0.132 MM		0.200 MM	0.200 MM
70_OHM_DIFF	ISL10,ISL11,ISL13	Y	0.132 MM	0.132 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	TOP,BOTTOM	Y	0.230 MM	0.230 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL2,ISL4,ISL5	Y	0.090 MM	0.090 MM		0.200 MM	0.200 MM
85_OHM_DIFF	ISL10,ISL11,ISL13	Y	0.090 MM	0.090 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
87_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
87_OHM_DIFF	TOP,BOTTOM	Y	0.220 MM	0.220 MM		0.180 MM	0.180 MM
87_OHM_DIFF	ISL2,ISL4,ISL5	Y	0.082 MM	0.082 MM		0.200 MM	0.200 MM
87_OHM_DIFF	ISL10,ISL11,ISL13	Y	0.082 MM	0.082 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	TOP,BOTTOM	Y	0.190 MM	0.190 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL2,ISL4,ISL5	Y	0.085 MM	0.085 MM		0.250 MM	0.250 MM
90_OHM_DIFF	ISL10,ISL11,ISL13	Y	0.085 MM	0.085 MM		0.250 MM	0.250 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	TOP,BOTTOM	Y	0.170 MM	0.170 MM		0.205 MM	0.205 MM
100_OHM_DIFF	ISL2,ISL4,ISL5	Y	0.065 MM	0.065 MM		0.280 MM	0.280 MM
100_OHM_DIFF	ISL10,ISL11,ISL13	Y	0.065 MM	0.065 MM		0.280 MM	0.280 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
BGA_P3MM	*	0.3 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.28:1_SPACING	*	0.228 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V8_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
NB_STATIC	*	=STANDARD	?

M82 Rule Definitions

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	J

SCALE	SHT	OF
NONE	109	109