1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM,MLB,MBP17

PVT 12/18/2007

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
0.1		521911	Proto Release	?	?

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7431	1	SCHEM,MLB,MBP17	SCH	CRITICAL	
820-2262	1	PCBF,MLB,MBP17	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Tue Dec 18 15:43:01 2007

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES °
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

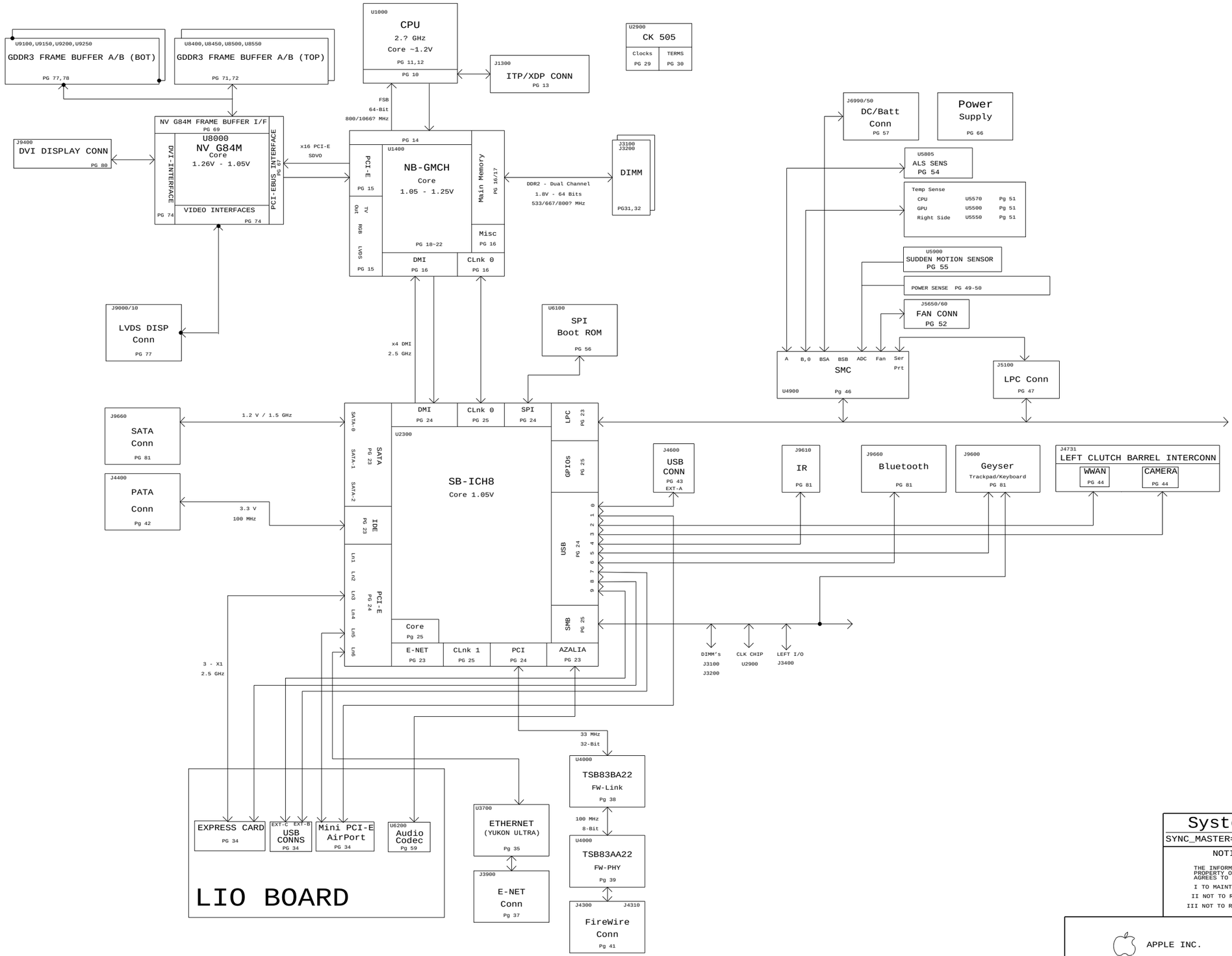
METRIC

DRAFTER / DESIGN CK
ENG APPD / MFG APPD
QA APPD / DESIGNER
RELEASE / SCALE NONE
MATERIAL/FINISH NOTED AS APPLICABLE
SIZE D

APPLE INC.

TITLE
SCHEM,MLB,MBP17

DRAWING NUMBER 051-7431
REV. A.0.0
SHT 1 OF 92



System Block Diagram

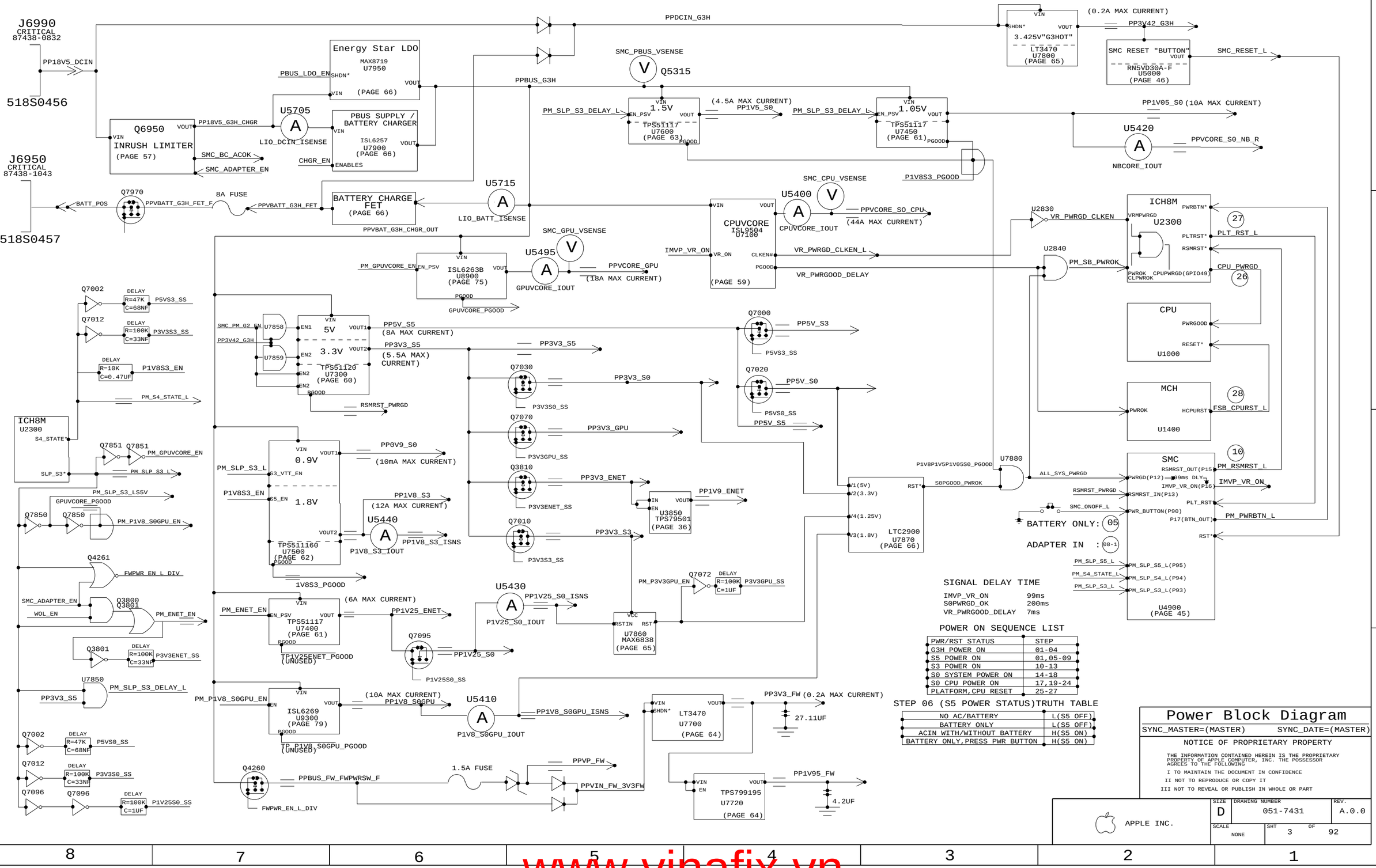
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 2 OF 92	

M88 POWER SYSTEM ARCHITECTURE



Power Block Diagram

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 4 OF 92	

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9092	PCBA,2.6GHZ,512VRAM-HY,M88	M88_COMMON,CPU_2_6GHZ,FB_512_HYNIX,EEE_Z3K
630-9093	PCBA,2.6GHZ,512VRAM-SAM,M88	M88_COMMON,CPU_2_6GHZ,FB_512_SAMSUNG,EEE_Z3L
630-9225	PCBA,2.5GHZ,512VRAM-HY,M88	M88_COMMON,CPU_2_5GHZ,FB_512_HYNIX,EEE_ZVW
630-9228	PCBA,2.5GHZ,512VRAM-SAM,M88	M88_COMMON,CPU_2_5GHZ,FB_512_SAMSUNG,EEE_ZVX

BOM Groups

BOM GROUP	BOM OPTIONS
M88_COMMON	COMMON,ALTERNATE,M88_COMMON1,M88_COMMON2,M88_DEBUG,M88_PROGPARTS
M88_COMMON1	BKLT_5V_PWR,ISL9504B,ONEWIRE_PU,GPUVID_1P23V
M88_COMMON2	P1V8S3_1V8,SMS_MOT_DIS,YUKON_ULTRA,VGA_TERM_CONN
M88_DEBUG	SMC_DEBUG_NO,XDP,LPCPLUS
M88_PROGPARTS	BOOTROM_PROG,SMC_PROG

BOM GROUP	BOM OPTIONS
FB_256_SAMSUNG	VRAM4,VRAM_16M,VRAM_SAMSUNG,VRAM_256_SAMSUNG
FB_256_HYNIX	VRAM4,VRAM_16M,VRAM_HYNIX,VRAM_256_HYNIX
FB_512_SAMSUNG	VRAM8,VRAM_16M,VRAM_SAMSUNG,VRAM_512_SAMSUNG
FB_512_HYNIX	VRAM8,VRAM_16M,VRAM_HYNIX,VRAM_512_HYNIX

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:Z3K]	CRITICAL	EEE_Z3K
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:Z3L]	CRITICAL	EEE_Z3L
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZVW]	CRITICAL	EEE_ZVW
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZVX]	CRITICAL	EEE_ZVX

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3559	1	IC,PDC,SR,PRQ,2.6G,35W,800FSB,6M,BGA	U1000	CRITICAL	CPU_2_6GHZ
337S3560	1	IC,PDC,SR,PRQ,2.5G,35W,800FSB,6M,BGA	U1000	CRITICAL	CPU_2_5GHZ
338S0509	1	IC,GPU,NV,G84M,BGA	U8000	CRITICAL	
338S0432	1	IC,NB,CRESTLINE,GM,C0,PRQ,ROHS-SPECIAL,965PM	U1400	CRITICAL	
338S0434	1	IC,SB,ICH8M,B1,PRQ,BGA	U2300	CRITICAL	
353S1651	1	IC,ISL9504B,2PH IMVP6 REG,PMON,QFN48	U7100	CRITICAL	ISL9504B
359S0130	1	IC,SLGZAP101,LW PWR CLK GEN,CK505,QFN68	U2900	CRITICAL	
338S0386	1	IC,88E8058,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	

338S0274	1	IC,SMC,HS8/2116	U4900	CRITICAL	SMC_BLANK
341S2194	1	IC,SMC,DEVELOPMENT,M88	U4900	CRITICAL	SMC_PROG
335S0384	1	IC,16MBIT 8-PIN SPI SERIAL FLASH,SOIC8	U6100	CRITICAL	BOOTROM_BLANK
341S2192	1	IC,EFI ROM,DEVELOPMENT,M87	U6100	CRITICAL	BOOTROM_PROG

333S0423	4	IC,SGRAM,GDDR3,16MX32,800MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_SAMSUNG
333S0423	8	IC,SGRAM,GDDR3,16MX32,800MHZ,136 FBGA	U8400,U8450,U8500,U8550,U8100,U8150,U8200,U8250	CRITICAL	VRAM_512_SAMSUNG
333S0424	4	IC,SGRAM,GDDR3,16MX32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_HYNIX
333S0424	8	IC,SGRAM,GDDR3,16MX32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550,U8100,U8150,U8200,U8250	CRITICAL	VRAM_512_HYNIX

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
157S0011	157S0030		ALL	E&E alt to TDK/BiTech magnetics
138S0603	138S0602		ALL	Murata alt to Samsung 22uF acoustic caps
353S1681	353S1294		ALL	TI alternate to National
376S0543	376S0466		ALL	ADS alternate to Silicon+ Si4413
152S0683	152S0276		ALL	Mag Layers alternate to Dale/Vishay
104S0024	104S0017		ALL	Panasonic alternate to Cyntec
128S0083	128S0165		ALL	alternate to halogen free Sanyo 330uF CI tant
128S0113	128S0160		ALL	alternate to halogen free Sanyo 220uF 2k mohm tant
128S0115	128S0150		ALL	alternate to halogen free Sanyo 150uF tant
128S0122	128S0157		ALL	alternate to halogen free Sanyo 220uF 1k mohm tant
128S0057	128S0147		ALL	alternate to halogen free Sanyo 100uF tant
128S0056	128S0175		ALL	alternate to halogen free Sanyo 330uF E5 tant
376S0448	376S0445		ALL	SiI7000ADN for FSM6206

BOM Configuration

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 5 OF 92	

Proto:

See earlier schematics for info about releases 0.0.1 - 4.0.0

EVT:

5.0.0:
08/03/07 -- Page 5: Removed Q4690 BOM table entry. BOM table is on CSA pg. 46
6.0.0 & 5.1.0:
08/10/07 -- Synced to M87 MLB label 4.3.0
08/10/07 -- Page 3: Revised power block diagram.
08/10/07 -- Page 10-12: Updated U1000 CPU part number to reflect latest Penryn pin-out.
08/10/07 -- Page 37: T3900,T3901 magnetics changed to 157S0053.
08/10/07 -- Page 65: Changed L7810 3.425V G3 Hot inductor to 152S0301. R7070 changed from 100K to 10K.
6.1.0:
08/14/07 -- Synced to M87 MLB label 5.1.0
08/14/07 -- Page 49: Changed Q5322 to SOT23 part same as M87.
08/14/07 -- Page 75: Changed GPU VID pull up/downs to 2.2K ohms.
6.2.0:
08/16/07 -- Removed Rev B Silego clock chip as alternate.
08/16/07 -- Page 51: Temp Sensors: Changed U5500 and U5570 to EMC1043-1 APN 353S1947.
7.0.0:
08/17/07 -- Page 48: Changed SMBus SMC "A" pull ups R5270 and R5271 to 3.3K to improve rise time on SCL..
7.1.0:
08/22/07 -- Page. 9,34: Added GPIOs to support iPhone headset. ICH8 GPIO 22 IPHS_SW_BIAS_EN_L routes to JJ3400.63
08/22/07 -- Page. 9,34: Removed R3410 and R3411. ICH8 GPIO 2 IPHS_SW_INT routes to JJ3400.65
08/22/07 -- Synced M87 MLB label 6.2.0
08/22/07 -- Page 51: Temp sensors: Added R5501,R5502,R5571,R5572 pull ups on U5500 and U5570.
08/22/07 -- Page 61: R7455 changed to 7.5K to change max load current margin on PP1V05.
08/22/07 -- Page 90: Changed frame buffer net physical type to GDDR3_50SE.
08/22/07 -- Synced M87 LIO label 1.5.0
08/22/07 -- Page 66: U7901 voltage follower changed from OPA333 to OPA705.
08/22/07 -- Page 82: Changed L9891,L9893,L9894 to 155S0220
7.2.0:
08/23/07 -- Page 5: Changed CPU parts to ES2, B1 for EVT
08/23/07 -- Page 9: IPHS_SW_BIAS_EN_L now connected to SB_SLOAD (GPIO 38).
08/23/07 -- Synced M87 MLB label 6.5.0
08/23/07 -- Page 50: Current Sensors: Changed U5410 and U5440 to MAX4245 Changed R5413 and R5443 to 0.005 ohm resistors.
08/23/07 -- Page 91: Added diff pair properties to new current sensor pairs.
08/23/07 -- Synced M87 LIO label 1.7.0
08/23/07 -- Page 66: Changed U7901 to MAX4245. Changed F7902 to 740S0055.
08/23/07 -- Page 82: Add BOMOPTION OMIT to RX9892.
8.0.0:
08/24/07 -- Page 25: Added NO STUFF to R2552 (was pull up on SB GPIO38 which is now used on IPHS).
08/24/07 -- Page 59: CPU Vcore supply changes per characterization. Changed L7100 and L7101 to 152S0624. Changed C7134 to 0.01uF 132S0042.
8.1.0:
08/24/07 -- Synced M87 MLB label 8.2.0
Page 5,75: Changed BOM option to GPUVID_1P23V
Page 73: Changed R5491 and R5493 to 6.81K to allow full resolution of GPUVCORE current sense
Page 50: Adding C5411,C5412,C5441,C5442 feedback caps for current sense op amps
Page 66: Changed R7920 to halogen free 107S0110.
8.2.0:
08/29/07 -- Synced m87_mlb CSA pgs. Major release label name : m87_mlb_051-7413_8.2.0
08/29/07 -- Changed net physical and net spacing to CRT_50S on these signals NB_CLK100M_DPLSS_P/N NB_CLK96M_DOT_P/N
8.3.0:
08/29/07 -- Changed the following filters to 155S0371 for supply issues: pg. 43 L4600 pg. 44 FL4735 pg. 76 L9010,L9011
08/29/07 -- pg. 80 L9460,L9464,L9468,L9476,L9480,L9484
8.4.0:
08/30/07 -- Changed the orientation on these filters to match layout: pg. 43 L4600 pg. 76 L9010,L9011
9.0.0:
08/30/07 -- RFA 529050 EVT Release of Schematic BOM and PCBF
9.1.0: BOM Changes only
09/04/07 -- Page 5: Added alternate sources for these parts:
09/04/07 -- 152S0683 is the Mag layers alternate for Dale/Vishay inductors.

09/04/07 -- 128S0164 is the Kemet alternate to Sanyo caps
09/04/07 -- 104S0023 is the Panasonic alternate to Cyntec resistors
09/04/07 -- Page 50: Changed R5425 and R5435 to 104S0023.
10.0.0:
09/06/07 -- HF capacitor substitution, with halogen parts as alternates. pg. 5 Alternates BOM table updates.
11.0.0:
09/11/07 -- Page 57: Removed NO STUFF from DZ6960 (377S0044), ESD diode on BATT_POS per Chris.
09/11/07 -- Page 5: Removed alternate to 128S0164 Kemet 220uF tantalum cap at C7540 and C7541.
09/11/07 -- Added BOM variants and EEE codes for 2.5GHz:
09/11/07 -- 630-9225: ZVW PCBA,2.5GHZ,512VRAM-HY,M88
09/11/07 -- 630-9228: ZVX PCBA,2.5GHZ,512VRAM-SAM,M88
09/11/07 -- Page 62: Removed OMIT property and BOM option table to make C7540 and C7541 only 128S0073.
09/11/07 -- Page 82: LCD Backlight Added OMIT properties and BOM option table to change these beads to 155S0220: L9891,L9893,L9894

DVT:

11.1.0:
09/12/07 -- Page 66: Swapped U7901 pins 1 and 3 signals (positive and negative inputs).
11.2.0:
09/26/07 -- Synced M*& MLB label 10.2.0
09/26/07 -- Page 50 & 75: GPUVCORE: Current sense to use IMVP6 IMON + Non-inverting Opamp removed R8992,C8992
09/26/07 -- Page 65: Changed C7860 to 0.0047uF (radar://5468257
12.0.0:
09/28/07 -- Removed BOM tables and OMIT BOM options from HF capacitor substitution, with halogen parts as alternates.
09/28/07 -- Synced M87 MLB label 10.3.0
09/28/07 -- Page 50: updating GPUVcore current sense resistor values for gain of 4.83
12.0.0:
10/01/07 -- Synced M87 LIO label 9.0.0 Added R9810
10/01/07 -- Synced M87 LIO label 7.0.0
10/01/07 -- <rdar://problem/5493576> M87/M88 MLB/LED: LED driver current mirror can not be disabled + power sequencing issue
<rdar://problem/5510696> TASK: M87 LIO changes to support LED board
10/01/07 -- Page 5: Added 376S0448 as alternate for 376S0445.
13.0.0:
10/05/07 -- Page 5: Removed HDCP ROM. Removed U8770, R8770,R871, C8770.
10/05/07 -- Page 75: GPU Vcore supply: Changed L8920 from 152S0525 to 152S0697.Dale 0.9uH 27A inductor has smaller pad size than Vishay IHLP4040.
13.1.0:
10/09/07 -- Synced m87_MLB label Change 72968 Page 5: Changed Module parts for new Penryn APNs.
10/09/07 -- Page 93: <rdar://problem/5525486> M87/88 1V8 FB DC converter transient response improve/BOM change
10/09/07 -- R9308 change to 40.2k, 0402, 1%; C9308 change to 680pF, 0402, 10V, 10% C9307 change to 68pF, 0402, 10V, 10%

DVT (cont):

14.0.0:
10/12/07 -- Page 81: Added FL9600 155S0372 to multi-touch trackpad power and GND.
10/12/07 -- Synced M87_MLB label: 12.1.0
10/12/07 -- Page 46: Changed to new Sleep LED circuit Deleted, Q5032,R5032,R5030 Added, C5030 Changed Q5030 to new LED Driver IC
10/12/07 -- Synced M*&_LIO label: 10.0.0
10/12/07 -- Changed R9807 to 5.1k Changed C9807 to 0.1uF Changed R9809 to 200k
14.1.0:
10/19/07 -- Synced M87_MLB label: 12.2.0 Page 50: Named unnamed net on Q5030.
10/19/07 -- Page 69: NO STUFF battery positive terminal varistor DZ6960
14.5.0:
10/24/07 -- Page 43: Changed L4605 ferrite bead to 155S0329 for lower DCR.
10/24/07 -- Page 57: Changed DZ6960-DZ6963 to 377S0068. These are NO STUFFs.
10/24/07 -- Page 90: Graphics constraints Changed all GDDR3_46SE constraints back to GDDR3_50SE.
16.0.0:
11/01/07 -- Page 53: Changed U5750 TMP102 to RevE part 353S2039 with old part 353S1807 as alternate.
11/01/07 -- Page 59: CPU Vcore power supply change C7134 to 0.022uF 132S0102 per Dayu
17.0.0:
11/06/07 -- Page 25: Removed NO STUFF BOM option from R2552, pull up on SB GPIO38.
11/06/07 -- Synced M87_LIO label 14.0.0 pg. 82 Changed C9805 to 2.2uF for LED power sequencing.

PVT:

18.0.0:
12/10/07 -- Page 98: Changed R9808 to 200K, R9809 to 100K, C9802 to 0.033uF, C9807 to 0.33uF to improve Q9806 Vgs and sequencing
18.1.0:
12/12/07 -- Page 5: Updated CPUs to PRQ parts, removed XDP_CONN and GPU_TMP401 bom options and changed to SMC_DEBUG_NO for PVT
12/12/07 -- Page 50: Removed ST SIL driver and returned to EVT's BJT-driven current source
12/12/07 -- Page 98: Changed C9805 to actual 2.2uF part (removed table entry)
18.2.0:
12/13/07 -- Page 13: NO STUFFed R1330/R1331 since the LVDS_CTRL_DATA/CLK lines are grounded
18.3.0:
12/16/07 -- Page 54: Added C8992/R8992 to provide differential sense option
A.0.0:
12/18/07 -- Release as Rev A

Revision History

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 6 OF 92	

Functional Test Points

Fan Connectors

FUNC_TEST

I498	TRUE	PP5V_S0	7 8 27 42 47 49 52 54 58 59 65 80 81 82
I497	TRUE	FAN_LT_PWM	52
I496	TRUE	FAN_LT_TACH	52
I495	TRUE	FAN_RT_PWM	52
I494	TRUE	FAN_RT_TACH	52

LPC+ Debug Connector

FUNC_TEST

I490	TRUE	PP3V42_G3H	6 28 42 45 46 47 48 57 58 59 81
I491	TRUE	PP5V_S0	7 8 27 42 47 49 52 54 58 59 65 80 81 82
I492	TRUE	LPC_AD<0>	23 45 47
I493	TRUE	LPC_AD<1>	23 45 47
I422	TRUE	LPC_FRAME_L	23 45 47
I423	TRUE	PM_CLKRUN_L	25 45 47
I492	TRUE	PCI_FW_GNT_L	24 38 47 87
I421	TRUE	SMC_TMS	45 46 47
I420	TRUE	DEBUG_RESET_L	28 47
I419	TRUE	SMC_TRST_L	45 47
I418	TRUE	SMC_TDO	45 46 47
I417	TRUE	SMC_MD1	45 47
I416	TRUE	SMC_TX_L	43 45 46 47
I415	TRUE	FWH_INIT_L	47
I414	TRUE	PCI_CLK33M_LPCPLUS	30 47 88
I413	TRUE	LPC_AD<2>	23 45 47
I412	TRUE	LPC_AD<3>	23 45 47
I411	TRUE	INT_SERIRQ	25 45 47
I410	TRUE	PM_SUS_STAT_L	25 45 46 47
I409	TRUE	SMC_TDI	45 46 47
I408	TRUE	SMC_TCK	45 46 47
I407	TRUE	SMC_RESET_L	45 46 47
I406	TRUE	SMC_NMI	45 47
I405	TRUE	SMC_RX_L	43 45 46 47
I403	TRUE	LINDACARD_GPIO	25 47

Left ALS

FUNC_TEST

I448	TRUE	ALS_GAIN	34 45 54
I447	TRUE	LTALS_OUT	34 54
	TRUE	GND	

Thermal Diode Connectors

FUNC_TEST

I568	TRUE	HSTHMSNS_D_P	51 91
I567	TRUE	HSTHMSNS_D_N	51 91
I443	TRUE	RSFSTHMSNS_D_P	51 91
I442	TRUE	RSFSTHMSNS_D_N	51 91
I520	TRUE	CPUTHMSNS_D2_P	51 91
I527	TRUE	CPUTHMSNS_D2_N	51 91

Battery Digital Connector

FUNC_TEST

I606	TRUE	SMC_BS_ALRT_L	45 46 57
I607	TRUE	SMBUS_SMC_BSA_SCL	45 48 57 88
I608	TRUE	SMBUS_SMC_BSA_SDA	45 48 57 88
I611	TRUE	BATT_POS	57 66
I430	TRUE	GND	
	TRUE	GND (HOST_DETECT_L)	

Left I/O Power Connector

FUNC_TEST

I429	TRUE	PP18V5_DCIN	57 — Request for 2 test points
I428	TRUE	PPBUS_G3H	82 — Request for 3 test points
	TRUE	GND	6 40 49 57 58 59 60 61 62 63 66 75 79

Request for at least 10 GND test points

NOTE: 10 additional GND test points are called out separately in these notes.

RTC Battery Connector

FUNC_TEST

I616	TRUE	PPVBATT_G3_RTC	28
	TRUE	GND	

Current Sense Calibration

FUNC_TEST

I431	TRUE	ISENSE_CAL_EN	45 49
I430	TRUE	PP5V_S0	7 8 27 42 47 49 52 54 58 59 65 80 81 82
I427	TRUE	PPVCORE_S0_CPU	8 11 12 49 59 — 2 TPs per
I426	TRUE	PPVCORE_GPU	8 49 68 75 — 2 TPs per
	TRUE	GND	

6 TPs, 2 with each of above TP pairs

Left Clutch Barrel Connector

FUNC_TEST

I636	TRUE	PP5V_S3_CAMERA_F	44
I614	TRUE	USB_CAMERA_F_N	44 91
I615	TRUE	USB_CAMERA_F_P	44 91

Other Func Test Points

FUNC_TEST

I433	TRUE	PM_SYSRST_L	25 28 45
I432	TRUE	SMC_ONOFF_L	45 46 81

Backlight Connector

FUNC_TEST

I633	TRUE	BKLT_PWR	81 82
I632	TRUE	BKLT_GND	81 82
I630	TRUE	BKLT_P5V_EN	81 82
I631	TRUE	BKLT_PWM	81 82
	TRUE	GND	

IR & Sleep LED Connector

FUNC_TEST

I639	TRUE	PP5V_S3	8 44 46 58 81
I640	TRUE	USB_IR_N	24 81 86
I642	TRUE	USB_IR_P	24 81 86
I644	TRUE	SYS_LED_ANODE	46 81
	TRUE	GND	

ICT Test Points

CPU FSB NO_TESTs

MAKE BASE	NO_TEST			
I638		TRUE	FSB_A_L<31..3>	10 14 83
I557		TRUE	FSB_ADS_L	10 14 83
I556		TRUE	FSB_ADSTB_L<1..0>	10 14 83
I555		TRUE	FSB_BNR_L	10 14 83
I554		TRUE	FSB_BREQ0_L	10 14 83
I552		TRUE	FSB_D_L<63..0>	10 14 83
I553		TRUE	FSB_DBSY_L	10 14 83
I636		TRUE	FSB_DINV_L<3..0>	10 14 83
I551		TRUE	FSB_DRDY_L	10 14 83
I640		TRUE	FSB_DSTB_L_N<3..0>	10 14 83
I647		TRUE	FSB_DSTB_L_P<3..0>	10 14 83
I648		TRUE	FSB_HIT_L	10 14 83
I649		TRUE	FSB_HITM_L	10 14 83
I641		TRUE	FSB_LOCK_L	10 14 83
I650		TRUE	FSB_REQ_L<4..0>	10 14 83
I672	TRUE	TRUE	NC_CPU_RSVD5 — NC_CPU_RSVD5	7 10

NB NO_TESTs

MAKE BASE	NO_TEST			
I655		TRUE	NC_NB_NC<1..16> — TP_NB_NC<1..16>	16
I569	TRUE 16	TRUE	NC_NB_RSVD<26..27> — TP_NB_RSVD<26..27>	
I570	TRUE	TRUE	NC_NB_RSVD<24> — TP_NB_RSVD<24>	16

System Validation TPs

FUNC_TEST

	TRUE	CPU_PWRGD	10 13 23 83
	TRUE	CPU_DPSLP_L	7 10 23 83
	TRUE	PM_DPRSLPVR	16 25 59 83
	TRUE	CPU_DPSLP_L	7 10 23 83
	TRUE	PM_LAN_ENABLE	25 45
	TRUE	PCI_RST_L	24 28
	TRUE	PM_RSMRST_L	25 45
	TRUE	PM_SB_PWROK	9 25 28
	TRUE	SB_RTC_RST_L	23 28
	TRUE	PM_STPCPU_L	25 29 30
	TRUE	PM_STPPCI_L	25 29 30
	TRUE	VR_PWRGD_CLKEN	25 28
	TRUE	VR_PWRGOOD_DELAY	9 16 28 59
	TRUE	FSB_CPURST_L	10 13 14 83
	TRUE	FSB_CPUSLP_L	10 14 83
	TRUE	FSB_DPWR_L	10 14 83
	TRUE	NB_SB_SYNC_L	16 25
I561	TRUE	PM_BMBUSY_L	16 25

FUNC_TEST

	TRUE	IMVP_VR_ON	45 59
	TRUE	IMVP_DPRSLPVR	59 83
	TRUE	PM_SLP_S3_L	25 35 36 40 45 49 58 62 65
	TRUE	PM_S4_STATE_L	25 34 43 45 58 65
	TRUE	PM_SLP_S5_L	25 45 46
	TRUE	PM_ENET_EN	36 61 65
	TRUE	P1V8P1V5P1V05S0_PGOOD	61 62 63 65
	TRUE	CPU_DPRSTP_L	10 16 23 59 83
	TRUE	IMVP6_VID<6..0>	12 59 83
	TRUE	FSB_CLK_CPU_N	10 29 30 88
	TRUE	FSB_CLK_CPU_P	10 29 30 88
	TRUE	PLT_RST_L	9 24 28 82
	TRUE	NB_RESET_L	16 28
	TRUE	GPU_RESET_L	28 67
	TRUE	SMC_LRESET_L	28 45
	TRUE	CPU_STPCLK_L	10 23 83
	TRUE	FSB_CLK_NB_P	14 29 30 88
	TRUE	FSB_CLK_NB_N	14 29 30 88
	TRUE	NB_CLKREQ_L	16 29
	TRUE	NB_CLK100M_PCIE_P	16 29 30 88
	TRUE	NB_CLK100M_PCIE_N	16 29 30 88
	TRUE	CPU_THERMTRIP_R	23

Functional / ICT Test

SYNC_MASTER=MASTER SYNC_DATE=MASTER

APPLE INC.

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"G3Hot" (Always-Present) Rails

PPBUS_G3H
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE

PPDCIN_G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V
MAKE_BASE=TRUE

PP3V42_G3H
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.42V
MAKE_BASE=TRUE

5V Rails

PP5V_S5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE

Chipset "VCore" Rails

PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.3 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE

GND

3.3V-2.5V Rails

PP3V3_S5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP1V25_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE

1.8V-0.9V Rails

PP1V8_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE

PP1V8_S3_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE

PP1V5_S0
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.25mm
VOLTAGE=1.5V
MAKE_BASE=TRUE

MAX I = ?.??A

PP1V25_S0_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE

PP1V05_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE

PPVCORE_S0_NB_R
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE

PPVCORE_S0_NB_R

PP0V9_S3_MEM_VREF
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE

PP0V9_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE

"ENET" Rails

PP3V3_ENET
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP1V9_ENET
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.9V
MAKE_BASE=TRUE

GND
Yukon EC will not be supported

PP1V25_ENET
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE

"FW" (FireWire) Rails

PPBUS_FW_FWPWRSW_F
MAKE_BASE=TRUE

PPVP_FW
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.3 mm
VOLTAGE=8.5V
MAKE_BASE=TRUE

PPVP_FW_PORTA_UF
MAKE_BASE=TRUE

PPVP_FW_PORTB_UF
MAKE_BASE=TRUE

PP3V3_FW
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP1V95_FW
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.95V
MAKE_BASE=TRUE

"GPU" Rails

PP3V3_S0GPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S0GPU_TMDS
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP1V8_S0GPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE

PP1V8_S0GPU_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE

PPVCORE_GPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE

Power Aliases

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
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NONE		

86 24 9 TP_USB_EXTDN — MAKE_BASE=TRUE — TP_USB_EXTDN (BI) 9 24 86

86 24 9 TP_USB_EXTDP — MAKE_BASE=TRUE — TP_USB_EXTDP (BI) 9 24 86

28 25 9 7 PM_SB_PWROK — MAKE_BASE=TRUE — PM_SB_PWROK 7 9 25 28

59 28 16 9 7 VR_PWRGOOD_DELAY — MAKE_BASE=TRUE — VR_PWRGOOD_DELAY 7 9 16 28 59

88 67 30 29 9 PEG_CLK100M_GPU_P — MAKE_BASE=TRUE — PEG_CLK100M_GPU_P 9 29 30 67 88

88 67 30 29 9 PEG_CLK100M_GPU_N — MAKE_BASE=TRUE — PEG_CLK100M_GPU_N 9 29 30 67 88

55 45 9 SMC_SMS_INT — MAKE_BASE=TRUE — SMC_SMS_INT 9 45 55

23 9 TP_EXTGPU_PWR_EN — MAKE_BASE=TRUE — TP_EXTGPU_PWR_EN 9 23

34 25 9 IPHS_SW_BIAS_EN_L — MAKE_BASE=TRUE — IPHS_SW_BIAS_EN_L 9 25 34

34 24 9 IPHS_SW_INT — MAKE_BASE=TRUE — IPHS_SW_INT 9 24 34

66 46 45 9 SMC_ENRGYSTR_LDO_EN — SMC_ENRGYSTR_LDO_EN 9 45 46 66

31 9 TP_MEM_A_A<15> — MAKE_BASE=TRUE — TP_MEM_A_A<15> 9 31

32 9 TP_MEM_B_A<15> — MAKE_BASE=TRUE — TP_MEM_B_A<15> 9 32

82 28 24 9 7 PLT_RST_L — PLT_RST_L 7 9 24 28 82

82 73 72 9 GPU_BL_PWM — GPU_BL_PWM 9 72 73 82

82 73 72 9 GPU_BKLT_EN — GPU_BKLT_EN 9 72 73 82

Thermal Module Holes

Top CPU TM "Hole"

Add 8 blind vias per side to GND

ZT0970 195R106 — Left CPU TM Hole

ZT0975 195R106 — Right CPU TM Hole

Top Right GPU TM Hole

ZT0985 195R106

ZT0980 195R106 — Bottom Left GPU TM Hole

All holes are plated through holes with two exceptions:

GND_CHASSIS_RIGHT_FAN_NOTCH (to the left of small well on lower board edge near USB)

GND_CHASSIS_BATTCONN_HOLE (to the left of DIMM cutout near board edge)

Chassis GNDs

ZT0901 195R106 — GND

ZT0900 195R106 — GND

Digital Ground

GND — MIN_LINE_WIDTH=0.6mm MIN_NECK_WIDTH=0.25mm VOLTAGE=0V

Frame holes

GND — MIN_LINE_WIDTH=0.6mm MIN_NECK_WIDTH=0.25mm VOLTAGE=0V

GND — MIN_LINE_WIDTH=0.6mm MIN_NECK_WIDTH=0.25mm VOLTAGE=0V

GND — MIN_LINE_WIDTH=0.6mm MIN_NECK_WIDTH=0.25mm VOLTAGE=0V

ZT0955 195R106

GND — MIN_LINE_WIDTH=0.6mm MIN_NECK_WIDTH=0.25mm VOLTAGE=0V

GND — MIN_LINE_WIDTH=0.6mm MIN_NECK_WIDTH=0.25mm VOLTAGE=0V

ZT0965 195R106

GND — MIN_LINE_WIDTH=0.6mm MIN_NECK_WIDTH=0.25mm VOLTAGE=0V

RAM door (Torx) holes

ZT0930 235R126 — GND — MIN_LINE_WIDTH=0.6mm MIN_NECK_WIDTH=0.25mm VOLTAGE=0V

ZT0935 235R126 — GND — MIN_LINE_WIDTH=0.6mm MIN_NECK_WIDTH=0.25mm VOLTAGE=0V

Chassis connection to be made at the mounting hole east of the LVDS connector

GND — MIN_LINE_WIDTH=0.6mm MIN_NECK_WIDTH=0.25mm VOLTAGE=0V MAKE_BASE=TRUE

SH0925 OG-503040 SHLD-SM-LF — pins 1, 2, 3 — GND, GND

Signal Aliases

SYNC_MASTER=MASTER SYNC_DATE=MASTER

APPLE INC.

SIZE D | DRAWING NUMBER 051-7431 | REV. A.0.0

SCALE NONE | SHT 9 OF 92

OMIT

U1000
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ADDR GROUP0
FSB_A_L<3> J4 A3*
FSB_A_L<4> L5 A4*
FSB_A_L<5> L4 A5*
FSB_A_L<6> K5 A6*
FSB_A_L<7> M3 A7*
FSB_A_L<8> N2 A8*
FSB_A_L<9> J1 A9*
FSB_A_L<10> N3 A10*
FSB_A_L<11> P5 A11*
FSB_A_L<12> P2 A12*
FSB_A_L<13> L2 A13*
FSB_A_L<14> P4 A14*
FSB_A_L<15> P1 A15*
FSB_A_L<16> R1 A16*
FSB_ADSTB_L<0> M1 ADSTB0*

REQ0* K3 FSB_REQ_L<0>
REQ1* H2 FSB_REQ_L<1>
REQ2* K2 FSB_REQ_L<2>
REQ3* J3 FSB_REQ_L<3>
REQ4* L1 FSB_REQ_L<4>

ADDR GROUP1
FSB_A_L<17> Y2 A17*
FSB_A_L<18> U5 A18*
FSB_A_L<19> R3 A19*
FSB_A_L<20> W6 A20*
FSB_A_L<21> U4 A21*
FSB_A_L<22> Y5 A22*
FSB_A_L<23> U1 A23*
FSB_A_L<24> R4 A24*
FSB_A_L<25> T5 A25*
FSB_A_L<26> T3 A26*
FSB_A_L<27> W2 A27*
FSB_A_L<28> W5 A28*
FSB_A_L<29> Y4 A29*
FSB_A_L<30> U2 A30*
FSB_A_L<31> V4 A31*
FSB_A_L<32> W3 A32*
FSB_A_L<33> AA4 A33*
FSB_A_L<34> AB2 A34*
FSB_A_L<35> AA3 A35*
FSB_ADSTB_L<1> V1 ADSTB1*

ICH
CPU_A20M_L A6 A20M*
CPU_FERR_L A5 FERR*
CPU_IGNNE_L C4 IGNNE*
CPU_STPCLK_L D5 STPCLK*
CPU_INTR C6 LINT0
CPU_NMI B4 LINT1
CPU_SMI_L A3 SMI*

RESERVED
TP_CPU_RSVD0 M4 RSVD0
TP_CPU_RSVD1 N5 RSVD1
TP_CPU_RSVD2 T2 RSVD2
TP_CPU_RSVD3 V3 RSVD3
TP_CPU_RSVD4 B2 RSVD4
NC_CPU_RSVD5 F6 RSVD5
TP_CPU_RSVD6 D2 RSVD6
TP_CPU_RSVD7 D22 RSVD7
TP_CPU_RSVD8 D3 RSVD8

CONTROL
ADS* H1 FSB_ADS_L
BNR* E2 FSB_BNR_L
BPRI* G5 FSB_BPRI_L
DEFER* H5 FSB_DEFER_L
DRDY* F21 FSB_DRDY_L
DBSY* E1 FSB_DBSY_L
BR0* F1 FSB_BREQ0_L
IERR* D20 CPU_IERR_L
INIT* B3 CPU_INIT_L
LOCK* H4 FSB_LOCK_L
RESET* C1 FSB_CPURST_L
RS0* F3 FSB_RS_L<0>
RS1* F4 FSB_RS_L<1>
RS2* G3 FSB_RS_L<2>
TRDY* G2 FSB_TRDY_L
HIT* G6 FSB_HIT_L
HITM* E4 FSB_HITM_L

XDP/ITP SIGNALS
BPM0* AD4 XDP_BPM_L<0>
BPM1* AD3 XDP_BPM_L<1>
BPM2* AD1 XDP_BPM_L<2>
BPM3* AC4 XDP_BPM_L<3>
PRDY* AC2 XDP_BPM_L<4>
PREQ* AC1 XDP_BPM_L<5>
TCK AC5 XDP_TCK
TDI AA6 XDP_TDI
TDO AB3 XDP_TDO
TMS AB5 XDP_TMS
TRST* AB6 XDP_TRST_L
DBR* C20 XDP_DBRESET_L

THERMAL
PROCHOT* D21 CPU_PROCHOT_L
THERMDA A24 CPU_THERMD_P
THERMDC B25 CPU_THERMD_N
THERMTRIP* C7 PM_THRMTRIP_L

H CLK
BCLK0 A22 FSB_CLK_CPU_P
BCLK1 A21 FSB_CLK_CPU_N

PP1V05_S0
R1002 54.9 1% 1/16W MF-LF 402
PLACE TESTPOINT ON FSB_IERR_L WITH A GND 0.1" AWAY

R1003 54.9 1% 1/16W MF-LF 402
R1004 68 5% 1/16W MF-LF 402
PM_THRMTRIP# SHOULD CONNECT TO ICH AND GMCH WITHOUT T (NO STUB)

R1005 1K 1% 1/16W MF-LF 402
R1006 2.0K 1% 1/16W MF-LF 402
NOSTUFF C1000 0.1uF 10% 16V X5R 402
PLACE C1000 CLOSE TO CPU_TEST4 PIN. MAKE SURE CPU_TEST4 IS REFERENCED TO GND

R1020 54.9 1% 1/16W MF-LF 402
R1021 54.9 1% 1/16W MF-LF 402
R1022 54.9 1% 1/16W MF-LF 402
R1023 649 1% 1/16W MF-LF 402
R1024 54.9 1% 1/16W MF-LF 402
XDP_TMS
XDP_TDI
XDP_TDO
XDP_TCK
XDP_TRST_L
PLACEMENT_NOTE=Place R1024 near ITP connector (if present)

0.5" MAX LENGTH FOR CPU_GTLREF

MISC
CPU_GTLREF AD26 GTLREF
CPU_TEST1 C23 TEST1
CPU_TEST2 D25 TEST2
TP_CPU_TEST3 C24 TEST3
CPU_TEST4 AF26 TEST4
TP_CPU_TEST5 AF1 TEST5
TP_CPU_TEST6 A26 TEST6
TP_CPU_TEST7 C3 TEST7
CPU_BSEL<0> B22 BSEL0
CPU_BSEL<1> B23 BSEL1
CPU_BSEL<2> C21 BSEL2

NOSTUFF R1030 0 5% 1/16W MF-LF 402
NOSTUFF R1012 1K 5% 1/16W MF-LF 402
NOSTUFF R1007 1K 5% 1/16W MF-LF 402

OMIT

U1000
PENRYN
FCBGA
2 OF 4

DATA GRP 0
FSB_D_L<0> E22 D0*
FSB_D_L<1> F24 D1*
FSB_D_L<2> E26 D2*
FSB_D_L<3> G22 D3*
FSB_D_L<4> F23 D4*
FSB_D_L<5> G25 D5*
FSB_D_L<6> E25 D6*
FSB_D_L<7> E23 D7*
FSB_D_L<8> K24 D8*
FSB_D_L<9> G24 D9*
FSB_D_L<10> J24 D10*
FSB_D_L<11> J23 D11*
FSB_D_L<12> H22 D12*
FSB_D_L<13> F26 D13*
FSB_D_L<14> K22 D14*
FSB_D_L<15> H23 D15*
FSB_DSTB_L_N<0> J26 DSTBN0*
FSB_DSTB_L_P<0> H26 DSTBP0*
FSB_DINV_L<0> H25 DINV0*

DATA GRP 1
FSB_D_L<16> N22 D16*
FSB_D_L<17> K25 D17*
FSB_D_L<18> P26 D18*
FSB_D_L<19> R23 D19*
FSB_D_L<20> L23 D20*
FSB_D_L<21> M24 D21*
FSB_D_L<22> L22 D22*
FSB_D_L<23> M23 D23*
FSB_D_L<24> P25 D24*
FSB_D_L<25> P23 D25*
FSB_D_L<26> P22 D26*
FSB_D_L<27> T24 D27*
FSB_D_L<28> R24 D28*
FSB_D_L<29> L25 D29*
FSB_D_L<30> T25 D30*
FSB_D_L<31> N25 D31*
FSB_DSTB_L_N<1> L26 DSTBN1*
FSB_DSTB_L_P<1> M26 DSTBP1*
FSB_DINV_L<1> N24 DINV1*

DATA GRP 2
D32* Y22 FSB_D_L<32>
D33* AB24 FSB_D_L<33>
D34* V24 FSB_D_L<34>
D35* V26 FSB_D_L<35>
D36* V23 FSB_D_L<36>
D37* T22 FSB_D_L<37>
D38* U25 FSB_D_L<38>
D39* U23 FSB_D_L<39>
D40* Y25 FSB_D_L<40>
D41* W22 FSB_D_L<41>
D42* Y23 FSB_D_L<42>
D43* W24 FSB_D_L<43>
D44* W25 FSB_D_L<44>
D45* AA23 FSB_D_L<45>
D46* AA24 FSB_D_L<46>
D47* AB25 FSB_D_L<47>
DSTBN2* Y26 FSB_DSTB_L_N<2>
DSTBP2* AA26 FSB_DSTB_L_P<2>
DINV2* U22 FSB_DINV_L<2>

DATA GRP 3
D48* AE24 FSB_D_L<48>
D49* AD24 FSB_D_L<49>
D50* AA21 FSB_D_L<50>
D51* AB22 FSB_D_L<51>
D52* AB21 FSB_D_L<52>
D53* AC26 FSB_D_L<53>
D54* AD20 FSB_D_L<54>
D55* AE22 FSB_D_L<55>
D56* AF23 FSB_D_L<56>
D57* AC25 FSB_D_L<57>
D58* AE21 FSB_D_L<58>
D59* AD21 FSB_D_L<59>
D60* AC22 FSB_D_L<60>
D61* AD23 FSB_D_L<61>
D62* AF22 FSB_D_L<62>
D63* AC23 FSB_D_L<63>
DSTBN3* AE25 FSB_DSTB_L_N<3>
DSTBP3* AF24 FSB_DSTB_L_P<3>
DINV3* AC20 FSB_DINV_L<3>

COMP0 R26 CPU_COMP<0>
COMP1 U26 CPU_COMP<1>
COMP2 AA1 CPU_COMP<2>
COMP3 Y1 CPU_COMP<3>
R1016 27.4 1% 1/16W MF-LF 402
R1017 54.9 1% 1/16W MF-LF 402
R1018 27.4 1% 1/16W MF-LF 402
R1019 54.9 1% 1/16W MF-LF 402

DPRSTP* E5 CPU_DPRSTP_L
DPSLP* B5 CPU_DPSLP_L
DPWR* D24 FSB_DPWR_L
PWRGOOD D6 CPU_PWRGD
SLP* D7 FSB_CPUSLP_L
PSI* AE6 CPU_PSI_L

LAYOUT NOTE:
COMP0,2 CONNECT WITH ZO=27.4OHM, MAKE TRACE LENGTH SHORTER THAN 0.5".
COMP1,3 CONNECT WITH ZO=55OHM, MAKE TRACE LENGTH SHORTER THAN 0.5".

CPU FSB

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

APPLE INC.

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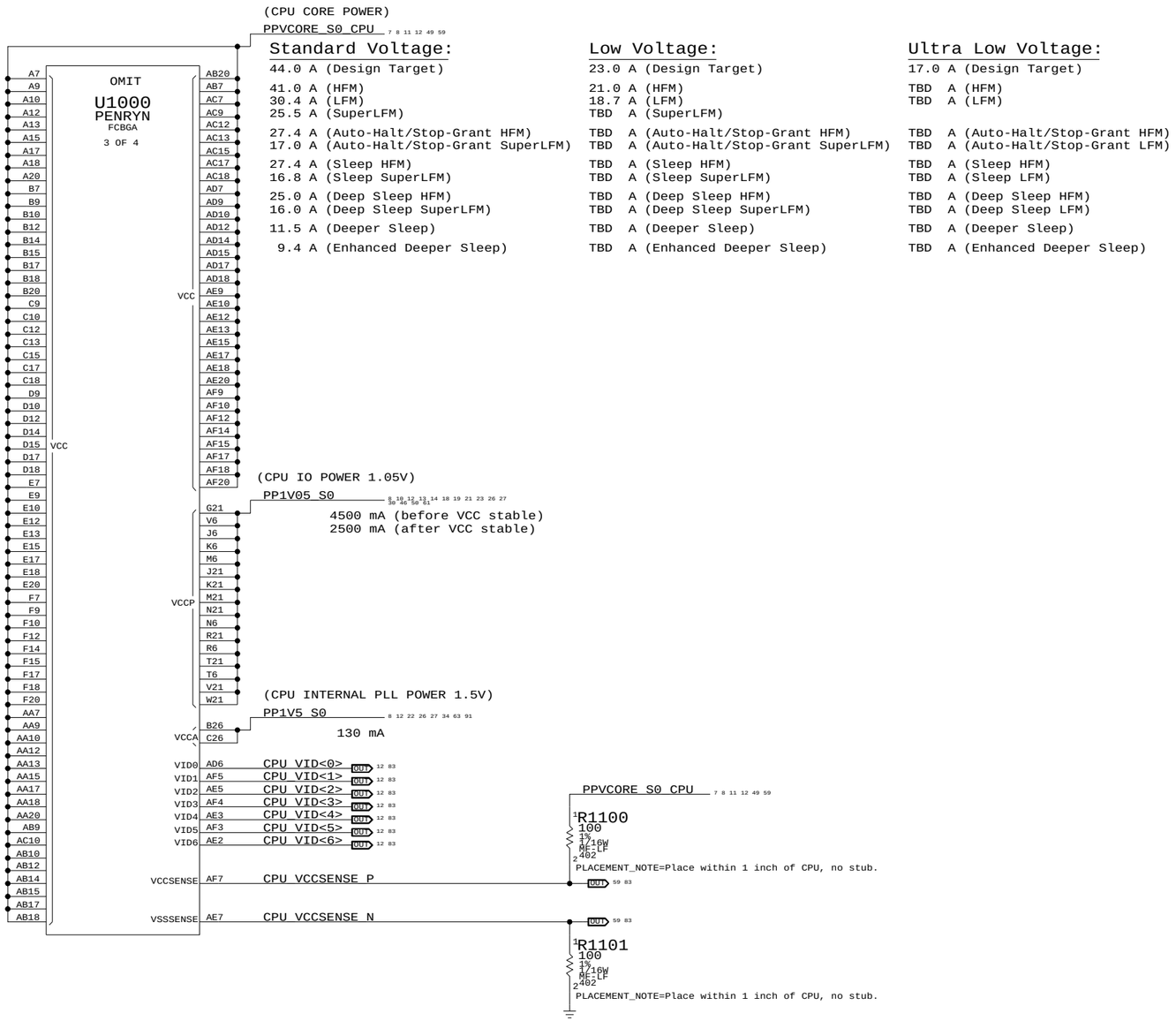
SCALE: NONE	SHT 10 OF 92	



CPU Power & Ground

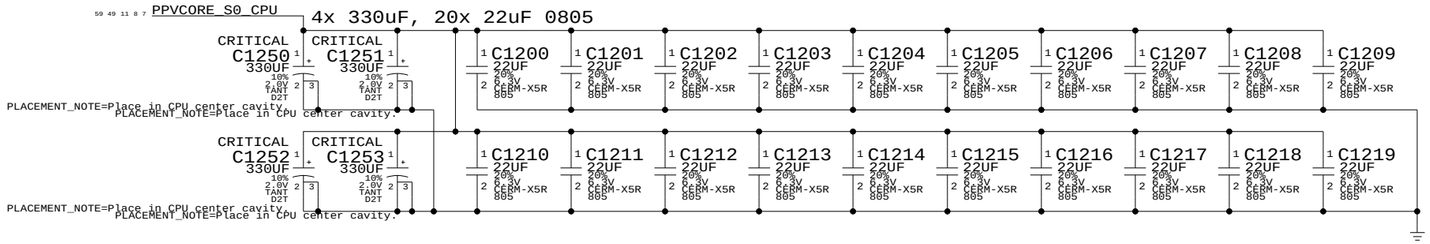
SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

APPLE INC.

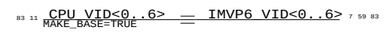
SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 11 OF 92	

Current numbers from Merom for Santa Rosa EMTS, doc #22221.

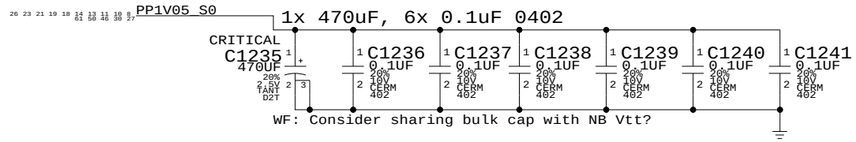
CPU VCORE HF AND BULK DECOUPLING



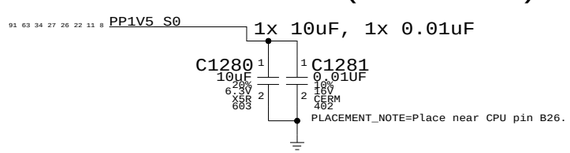
CPU VCORE VID CONNECTIONS



VCCP (CPU I/O) DECOUPLING



VCCA (CPU AVdd) DECOUPLING



CPU Decoupling & VID

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

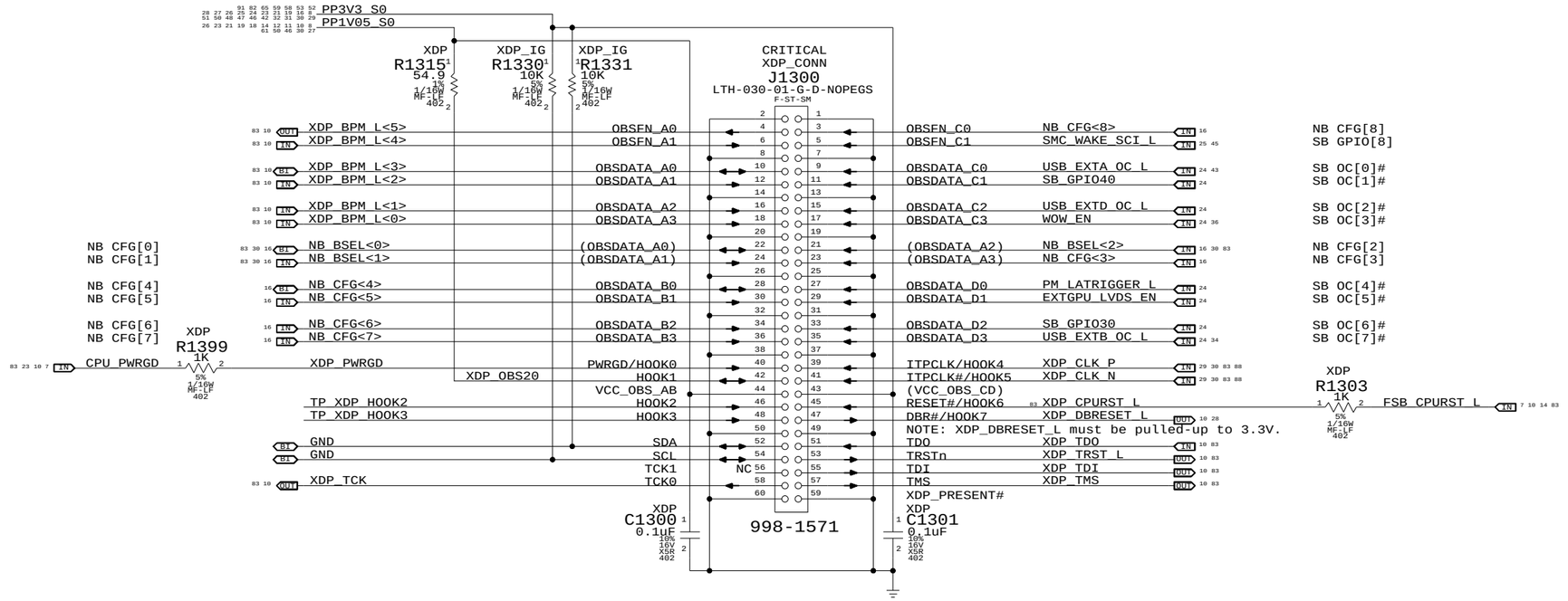
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 12 OF 92	

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0451 adapter board to support CPU, NB & SB debugging.



Direction of XDP module

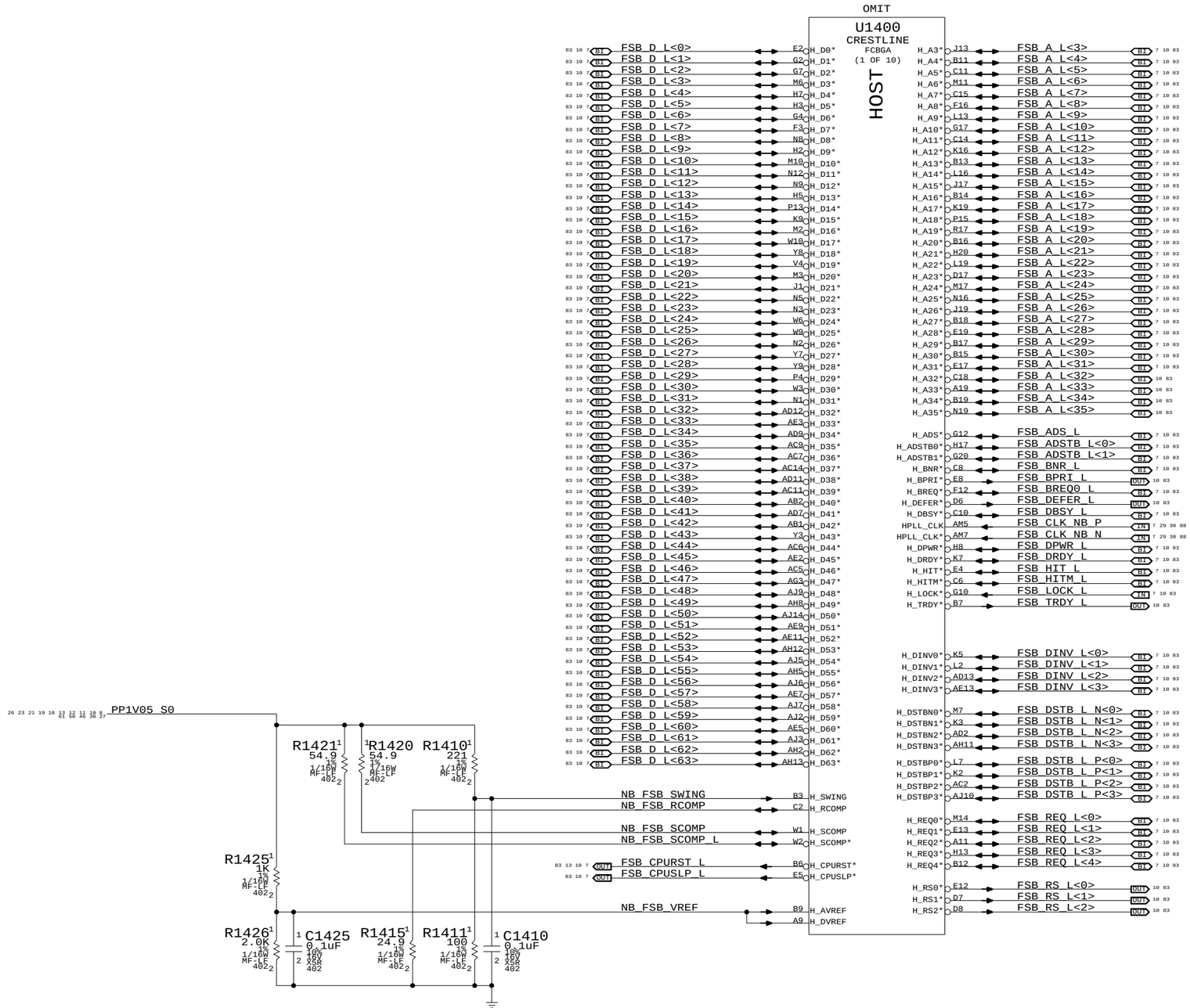
Please avoid any obstructions
on even-numbered side of J1300

eXtended Debug Port (XDP)

SYNC_MASTER=T9_NOME SYNC_DATE=01/22/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 13 OF 92	



NB CPU Interface

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

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D	051-7431	A.0.0
SCALE: NONE	SHT 14 OF 92	

LVDS Disable

Can leave all signals NC if LVDS is not implemented.
Tie VCC_TX_LVDS and VCCA_LVDS to GND.

If SDVO is used, VCCD_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD_LVDS to GND also.

Note: SR DG says to tie LVDS_VREFH/L to GND. This causes a glitch during wake-up on LVDS DATA/CLK pairs. New recommendation is to float both signals, see Radar #5067636.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable / CRT Enable

Tie TVx_DAC and TVx_RTN to GND. Must power all TVDAC rails. VCCA_TVx_DAC and VCCA_DAC_BG can share filtering with VCCA_CRT_DAC.

CRT Disable / TV-Out Enable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND.
All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA_CRT.

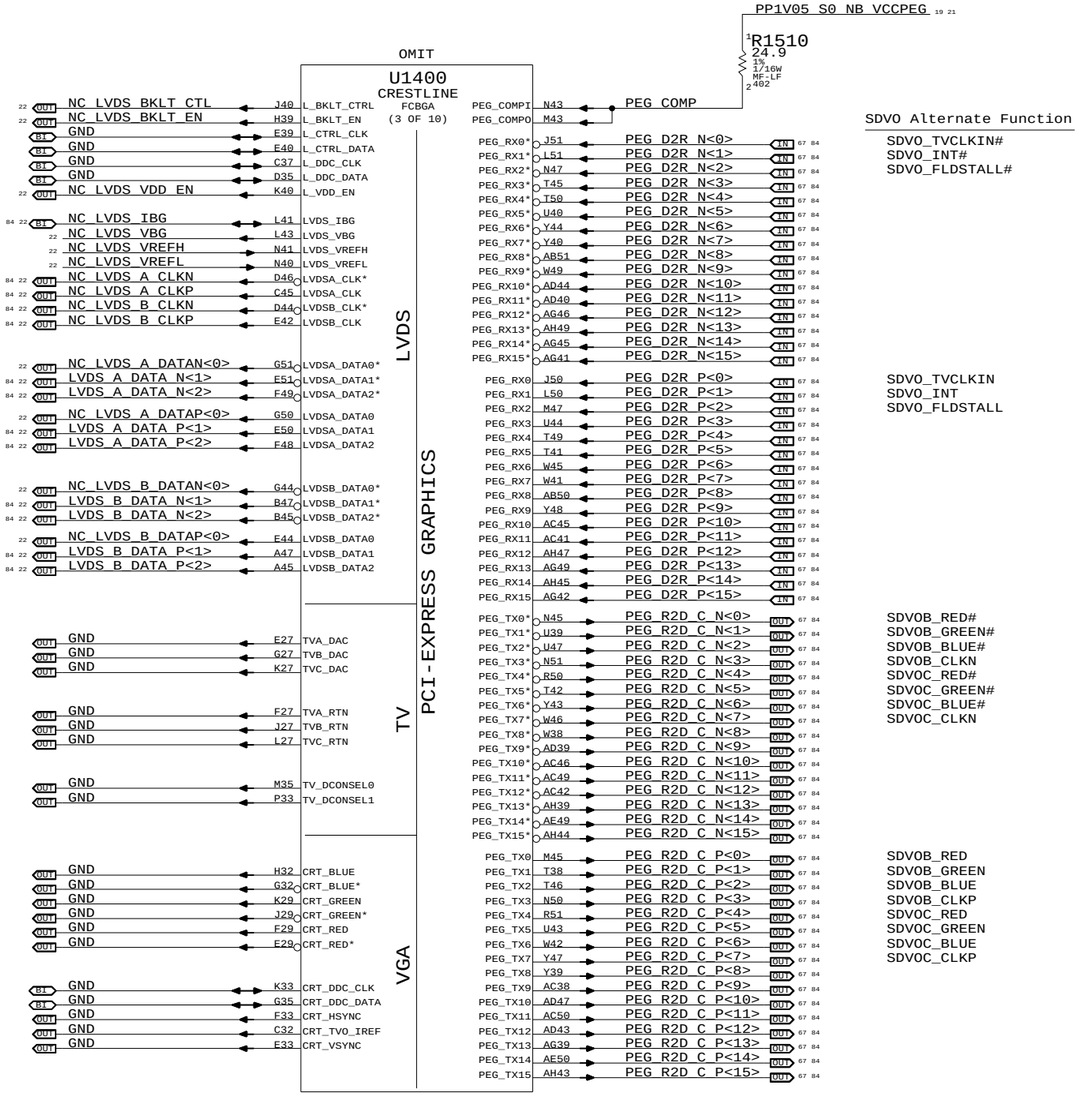
CRT & TV-Out Disable

Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT_TVO_IREF to GND.
Can tie the following rails to GND:
VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC, VCCD_CRT, VCCD_QDAC and VCC_SYNC.

NOTE: Must keep VDDC_TVDAC powered and filtered at all times!

Internal Graphics Disable

Follow instructions for LVDS and CRT & TV-Out Disable above.
Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and TV_DCONSELx to GND.
Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.
Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).
Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore).
Tie VCC_AXG and VCC_AXG_NCTF to GND.
Leave GFX_VID<3..0> and GFX_VR_EN as NC.



NB PEG / Video Interfaces

SYNC_MASTER=T9_NOME SYNC_DATE=03/19/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 15 OF 92	

NB_CFG<3>	RESERVED
NB_CFG<4>	RESERVED
NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2
NB_CFG<6>	RESERVED
NB_CFG<7>	RESERVED
NB_CFG<8>	RESERVED
NB_CFG<9> PCIe Graphics Lane Reversal	High = Normal Low = Reversed
NB_CFG<10>	RESERVED
NB_CFG<11>	RESERVED
NB_CFG<12>	See Below
NB_CFG<13>	See Below
NB_CFG<14>	RESERVED
NB_CFG<15>	RESERVED
NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled
NB_CFG<17>	RESERVED
NB_CFG<18>	RESERVED
NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal
NB_CFG<20> Concurrent SDVO/PCIe x1	High = Both active Low = Only SDVO or PCIe x16

NB_CFG<13:12>

00 = RESERVED
01 = XOR Mode Enabled
10 = All-Z Mode Enabled
11 = Normal Operation

NB_CFG<5> 13 16
NBCFG_DMI_X2
R1655 3.9K 5% 1/16W MF-LF 402

NB_CFG<9> 16
NBCFG_PEG_REVERSE
R1659 3.9K 5% 1/16W MF-LF 402

NB_CFG<16> 16
NBCFG_DYN_ODT_DISABLE
R1666 3.9K 5% 1/16W MF-LF 402

PP3V3_S0 52 53 58 59 65 82 91 8 13 16 19 23 24 25 26 27 28 29 30 31 32 42 46 47 48 50 51
NBCFG_DMI_REVERSE
R1669 3.9K 5% 1/16W MF-LF 402
NB_CFG<19> 16

PP3V3_S0 52 53 58 59 65 82 91 8 13 16 19 23 24 25 26 27 28 29 30 31 32 42 46 47 48 50 51
NBCFG_SDVO_AND_PCIE
R1670 3.9K 5% 1/16W MF-LF 402
NB_CFG<20> 16

NB CFG<8:0> used for debug access

NB CFG<13:12> require ICT access

PP3V3_S0 27 26 52 53 58 59 65 82 91 50 48 47 46 42 32 31 30 29 28
R1630 10K 5% 1/16W MF-LF 402
R1631 10K 5% 1/16W MF-LF 402
PM_EXTTS_L<0> 45 31 IN
PM_EXTTS_L<1> 45 32 IN

OMIT

U1400
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(2 OF 10)

RSVD

TP_NB_RSVD<1>	P36	RSVD1
TP_NB_RSVD<2>	P37	RSVD2
TP_NB_RSVD<3>	R35	RSVD3
TP_NB_RSVD<4>	N35	RSVD4
TP_NB_RSVD<5>	AR12	RSVD5
TP_NB_RSVD<6>	AR13	RSVD6
TP_NB_RSVD<7>	AM12	RSVD7
TP_NB_RSVD<8>	AN13	RSVD8
TP_NB_RSVD<9>	J12	RSVD9
TP_NB_RSVD<10>	AR37	RSVD10
TP_NB_RSVD<11>	AM36	RSVD11
TP_NB_RSVD<12>	AL36	RSVD12
TP_NB_RSVD<13>	AM37	RSVD13
TP_NB_RSVD<14>	D20	RSVD14
TP_NB_RSVD<20>	H10	RSVD20
TP_NB_RSVD<21>	B51	RSVD21
TP_NB_RSVD<22>	BJ20	RSVD22
TP_NB_RSVD<23>	BK22	RSVD23
7 NB_RSVD<24>	BF19	RSVD24
TP_NB_RSVD<25>	BH20	RSVD25
7 NC_NB_RSVD<26>	BK18	RSVD26
7 NC_NB_RSVD<27>	BJ18	RSVD27
TP_MEM_CLKP2	BF23	SM_CK2
TP_MEM_CLKN2	BG23	SM_CK2*
TP_MEM_CLKP5	BC23	SM_CK5
TP_MEM_CLKN5	BD24	SM_CK5*
85 33 31 OUT MEM_A_A<14>	BJ29	SA_MA14
85 33 32 OUT MEM_B_A<14>	BE24	SB_MA14
TP_NB_RSVD<34>	BH39	RSVD34
TP_NB_RSVD<35>	AW20	RSVD35
TP_NB_RSVD<36>	BK20	RSVD36
TP_LVDS_A_DATAN3	C48	RSVD37
TP_LVDS_A_DATAP3	D47	RSVD38
TP_LVDS_B_DATAN3	B44	RSVD39
TP_LVDS_B_DATAP3	C44	RSVD40
TP_NB_RSVD<41>	A35	RSVD41
TP_NB_RSVD<42>	B37	RSVD42
TP_NB_RSVD<43>	B36	RSVD43
TP_NB_RSVD<44>	B34	RSVD44
TP_NB_RSVD<45>	C34	RSVD45

CFG

83 30 13 IN NB_BSEL<0>	P27	CFG0	
83 30 13 IN NB_BSEL<1>	N27	CFG1	
83 30 13 IN NB_BSEL<2>	N24	CFG2	
13 OUT NB_CFG<3>	C21	CFG3	IPU
13 BI NB_CFG<4>	C23	CFG4	IPU
16 13 BI NB_CFG<5>	F23	CFG5	IPU
13 OUT NB_CFG<6>	N23	CFG6	IPU
13 OUT NB_CFG<7>	G23	CFG7	IPU
13 OUT NB_CFG<8>	J20	CFG8	IPU
16 NB_CFG<9>	C20	CFG9	IPU
TP_NB_CFG<10>	R24	CFG10	IPU
TP_NB_CFG<11>	L23	CFG11	IPU
TP_NB_CFG<12>	J23	CFG12	IPU
TP_NB_CFG<13>	E23	CFG13	IPU
TP_NB_CFG<14>	E20	CFG14	IPU
TP_NB_CFG<15>	K23	CFG15	IPU
16 NB_CFG<16>	M20	CFG16	IPU
TP_NB_CFG<17>	M24	CFG17	IPU
TP_NB_CFG<18>	L32	CFG18	IPD
16 NB_CFG<19>	N33	CFG19	IPD
16 NB_CFG<20>	L35	CFG20	IPD

PM

25 7 OUT PM_BMBUSY_L	G41	PM_BM_BUSY*
83 59 23 10 7 IN CPU_DPRSTP_L	L39	PM_DPRSTP*
	L36	PM_EXT_TS0*
	J36	PM_EXT_TS1*
59 28 16 9 7 IN VR_PWRGOOD_DELAY	AW49	PWROK
28 7 IN NB_RESET_L	AV20	RSTIN*
83 46 23 10 OUT PM_THRMTRIP_L	N20	THERMTRIP*
83 59 25 7 IN PM_DPRSLPVR	G36	DPRSLPVR

NC

7 TP_NB_NC<1>	BJ51	NC1
7 TP_NB_NC<2>	BK51	NC2
7 TP_NB_NC<3>	BK50	NC3
7 TP_NB_NC<4>	BL50	NC4
7 TP_NB_NC<5>	BL49	NC5
7 TP_NB_NC<6>	BL3	NC6
7 TP_NB_NC<7>	BL2	NC7
7 TP_NB_NC<8>	BK1	NC8
7 TP_NB_NC<9>	BJ1	NC9
7 TP_NB_NC<10>	E1	NC10
7 TP_NB_NC<11>	A5	NC11
7 TP_NB_NC<12>	C51	NC12
7 TP_NB_NC<13>	B50	NC13
7 TP_NB_NC<14>	A50	NC14
7 TP_NB_NC<15>	A49	NC15
7 TP_NB_NC<16>	BK2	NC16

DDR MUXING

SM_CK0	AV29	MEM_CLK_P<0> OUT 31 85
SM_CK1	BB23	MEM_CLK_P<1> OUT 31 85
SM_CK3	BA25	MEM_CLK_P<3> OUT 32 85
SM_CK4	AV23	MEM_CLK_P<4> OUT 32 85
SM_CK0*	AW30	MEM_CLK_N<0> OUT 31 85
SM_CK1*	BA23	MEM_CLK_N<1> OUT 31 85
SM_CK3*	AW25	MEM_CLK_N<3> OUT 32 85
SM_CK4*	AW23	MEM_CLK_N<4> OUT 32 85
SM_CKE0	BE29	MEM_CKE<0> OUT 31 33 85
SM_CKE1	AY32	MEM_CKE<1> OUT 31 33 85
SM_CKE3	BD39	MEM_CKE<3> OUT 32 33 85
SM_CKE4	BG37	MEM_CKE<4> OUT 32 33 85
SM_CS0*	BG20	MEM_CS_L<0> OUT 31 33 85
SM_CS1*	BK16	MEM_CS_L<1> OUT 31 33 85
SM_CS2*	BG16	MEM_CS_L<2> OUT 32 33 85
SM_CS3*	BE13	MEM_CS_L<3> OUT 32 33 85
SM_ODT0	BH18	MEM_ODT<0> OUT 31 33 85
SM_ODT1	BJ15	MEM_ODT<1> OUT 31 33 85
SM_ODT2	BJ14	MEM_ODT<2> OUT 32 33 85
SM_ODT3	BE16	MEM_ODT<3> OUT 32 33 85
SM_RCOMP	BL15	MEM_RCOMP
SM_RCOMP*	BK14	MEM_RCOMP_L
SM_RCOMP_VOH	BK31	MEM_RCOMP_VOH
SM_RCOMP_VOL	BL31	MEM_RCOMP_VOL
SM_VREF0	AR49	PP0V9_S3_MEM_VREF IN 8 16 31 32 62
SM_VREF1	AW4	PP0V9_S3_MEM_VREF IN 8 16 31 32 62

CLK

DPLL_REF_CLK	B42	GND IN
DPLL_REF_CLK*	C42	GND IN
DPLL_REF_SSCLK	H48	GND IN
DPLL_REF_SSCLK*	H47	GND IN
PEG_CLK	K44	NB_CLK100M_PCIE_P IN 7 29 30 88
PEG_CLK*	K45	NB_CLK100M_PCIE_N IN 7 29 30 88

Clk used for PEG and DMI

DMI

DMI_RXN0	AN47	DMI_S2N_N<0> IN 24 84
DMI_RXN1	AJ38	DMI_S2N_N<1> IN 24 84
DMI_RXN2	AN42	DMI_S2N_N<2> IN 24 84
DMI_RXN3	AN46	DMI_S2N_N<3> IN 24 84
DMI_RXP0	AM47	DMI_S2N_P<0> IN 24 84
DMI_RXP1	AJ39	DMI_S2N_P<1> IN 24 84
DMI_RXP2	AN41	DMI_S2N_P<2> IN 24 84
DMI_RXP3	AN45	DMI_S2N_P<3> IN 24 84
DMI_TXN0	AJ46	DMI_N2S_N<0> OUT 24 84
DMI_TXN1	AJ41	DMI_N2S_N<1> OUT 24 84
DMI_TXN2	AM40	DMI_N2S_N<2> OUT 24 84
DMI_TXN3	AM44	DMI_N2S_N<3> OUT 24 84
DMI_TXP0	AJ47	DMI_N2S_P<0> OUT 24 84
DMI_TXP1	AJ42	DMI_N2S_P<1> OUT 24 84
DMI_TXP2	AM39	DMI_N2S_P<2> OUT 24 84
DMI_TXP3	AM43	DMI_N2S_P<3> OUT 24 84

GRAPHICS VID

		GND OUT
GFX_VID0	E35	TP_GFX_VID<1> OUT 22
GFX_VID1	A39	GFX_VID<2> OUT 22
GFX_VID2	C38	GFX_VID<3> OUT 22
GFX_VID3	B39	GFX_VID<4> OUT 22
GFX_VR_EN	E36	TP_GFX_VR_EN OUT 22

MISC

CL_CLK	AM49	CLINK_NB_CLK BI 25 87
CL_DATA	AK50	CLINK_NB_DATA BI 25 87
CL_PWROK	AT43	VR_PWRGOOD_DELAY IN 7 9 16 28 59
CL_RST*	AN49	CLINK_NB_RESET_L OUT 25 87
CL_VREF	AM50	87 NB_CLINK_VREF
SDVO_CTRL_CLK	H35	GND BI
SDVO_CTRL_DATA	K36	GND BI
CLKREQ*	G39	NB_CLKREQ_L OUT 7 29
ICH_SYNC*	G40	NB_SB_SYNC_L OUT 7 25
TEST1	A37	NB_TEST1
TEST2	R32	NB_TEST2

R1691 20K 5% 1/16W MF-LF 402
R1690 0 5% 1/16W MF-LF 402

PP1V8_S3_ISNS 50 21 18 8
R1610 20 1% 1/16W MF-LF 402
R1620 1K 1% 1/16W MF-LF 402
C1623 0.01UF 10% 16V CERM 402
C1622 2.2UF 20% 6.3V CERM1 603
R1622 3.01K 1% 1/16W MF-LF 402
R1611 20 1% 1/16W MF-LF 402
C1625 0.01UF 10% 16V CERM 402
C1624 2.2UF 20% 6.3V CERM1 603
R1624 1K 1% 1/16W MF-LF 402

C1615 0.1UF 20% 10V CERM 402
C1616 0.1UF 20% 10V CERM 402

PP1V25_S0M_NB_VCCAXD 19 21
R1640 1K 1% 1/16W MF-LF 402
C1640 0.1UF 20% 10V CERM 402
R1641 392 1% 1/16W MF-LF 402

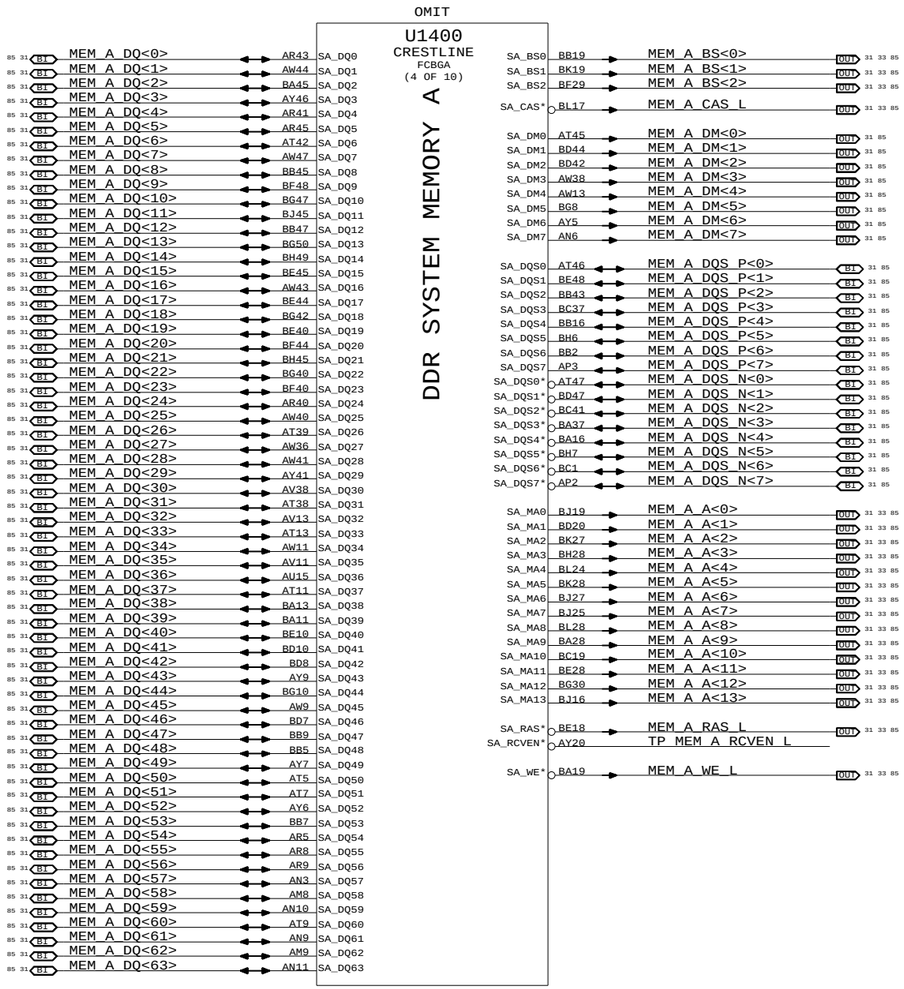
NOTE: GMCH CL_PWROK input must be PWRGD signal for PP3V3_S0M, PP3V3_S0MWOL, PP1V8_S3M, PP1V25_S0M, PP1V05_S0M, PP0V9_S3M and PP0V9_S0M.
If ME/AMT is not used, short CL_PWROK to PWROK.

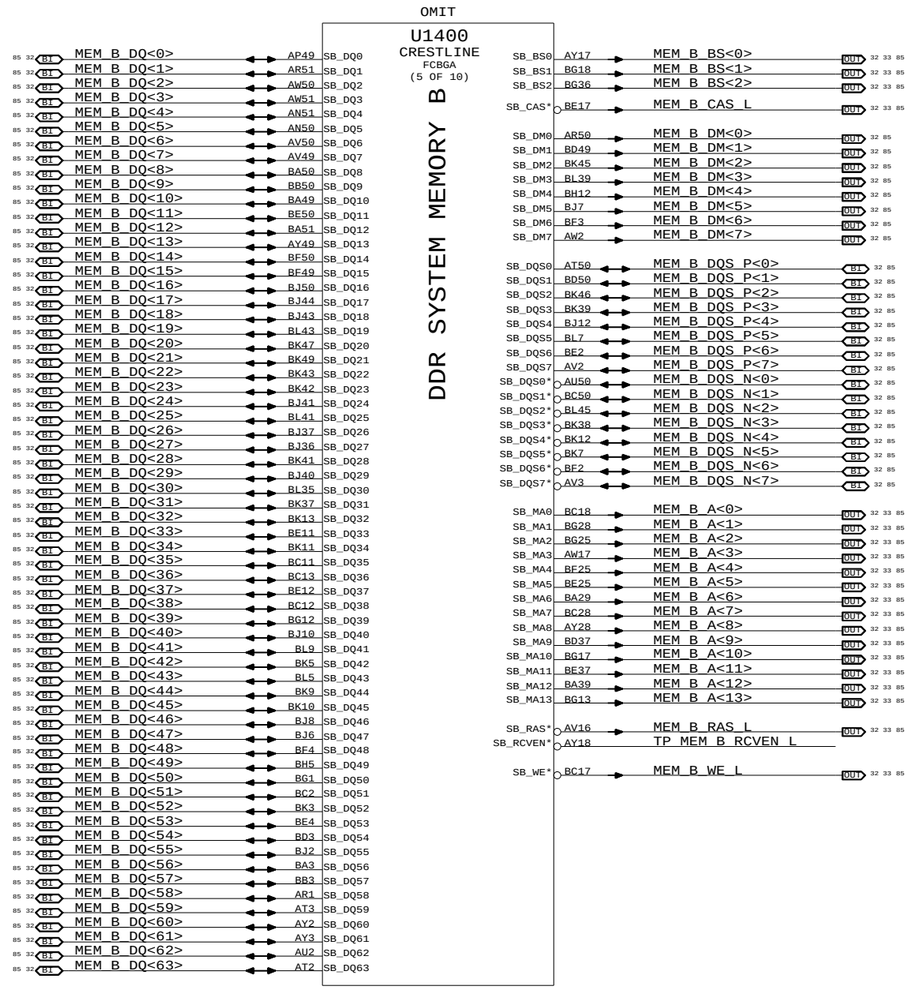
NB Misc Interfaces

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 16 OF 92	



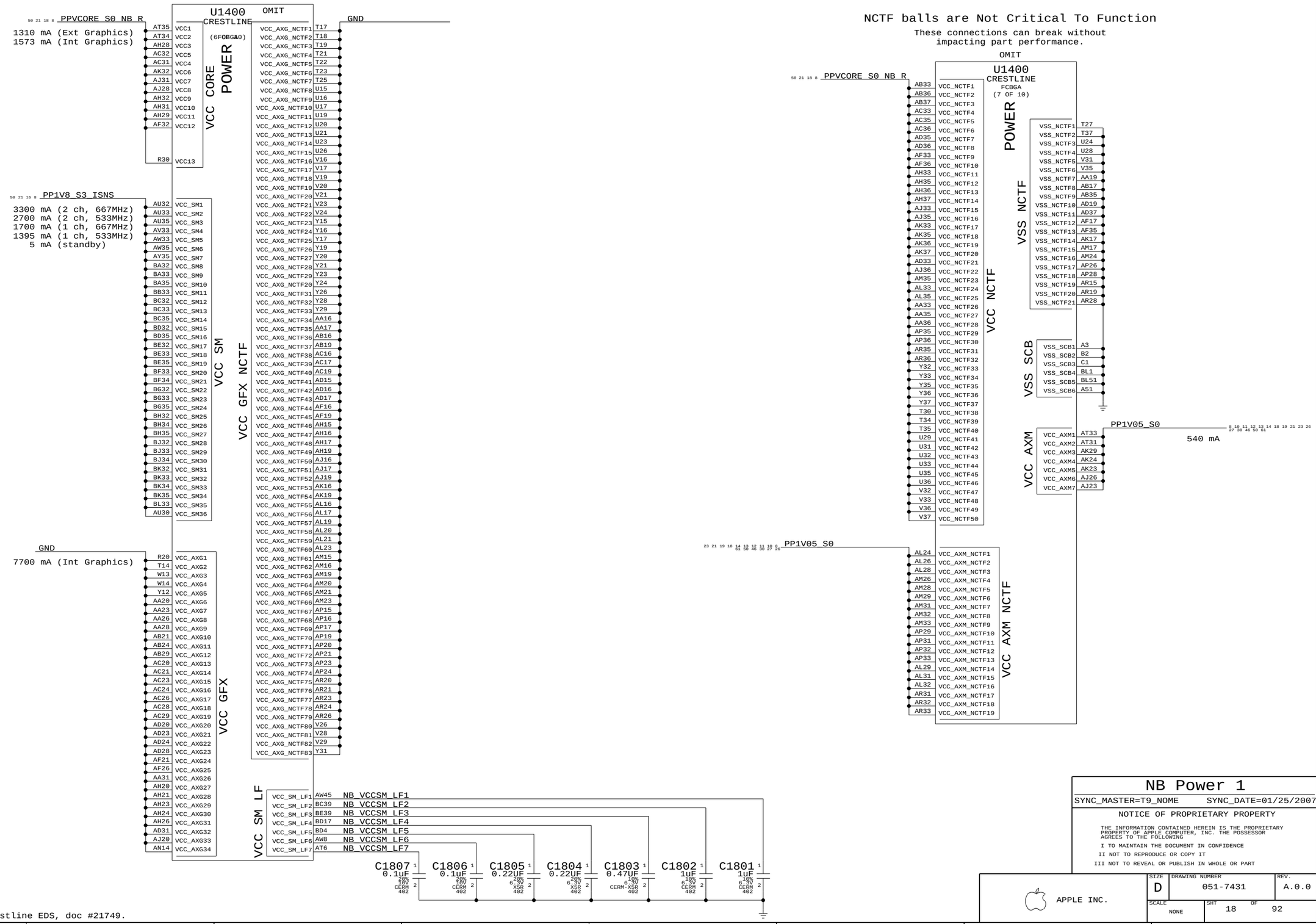


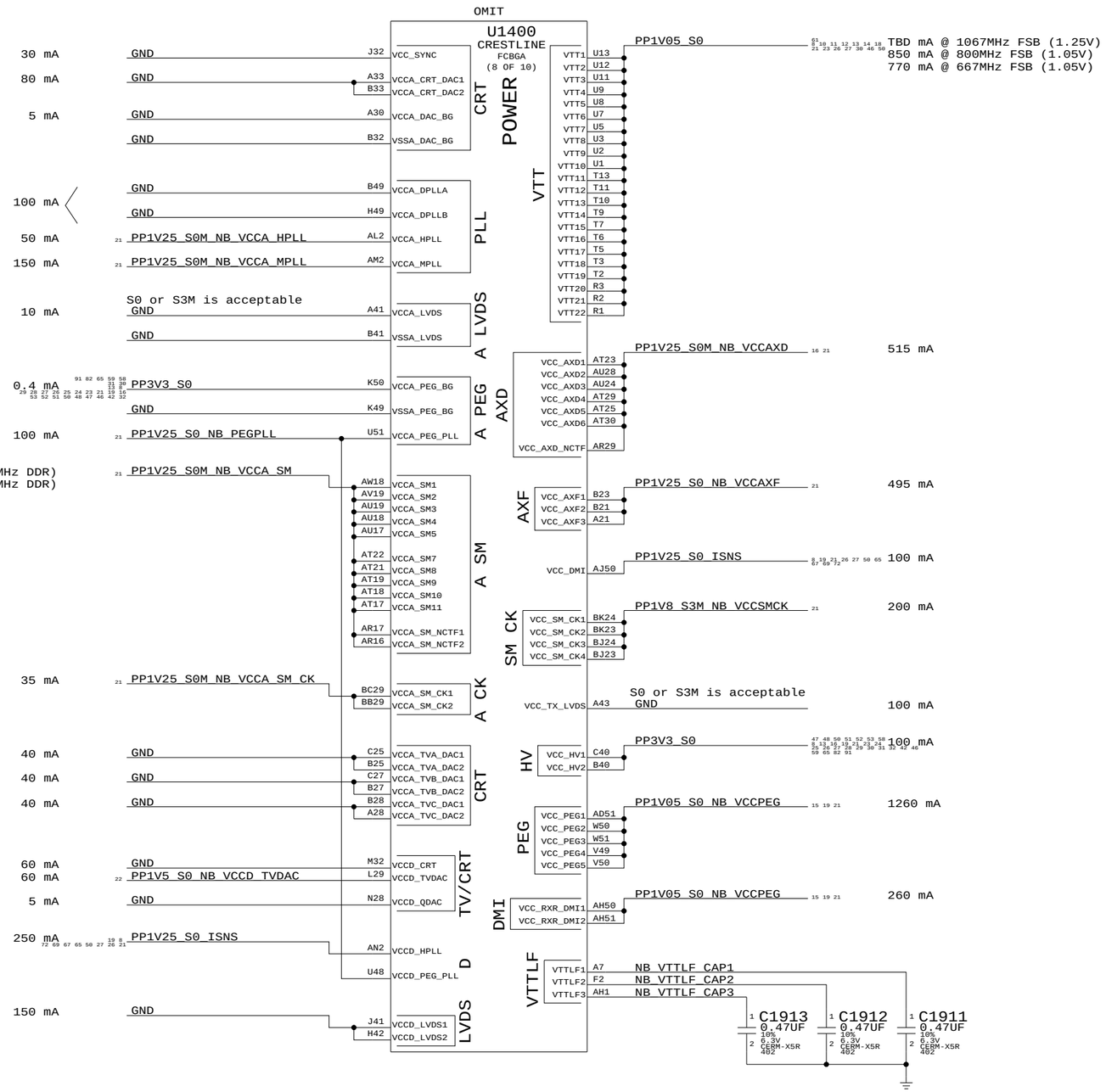
NB DDR2 Interfaces

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 17 OF 92	





Current numbers from Crestline EDS, doc #21749.

NB Power 2

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 19 OF 92	

OMIT

U1400
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(9 OF 10)
VSS

A13	VSS1	VSS100	AW24
A15	VSS2	VSS101	AW29
A17	VSS3	VSS102	AW32
A24	VSS4	VSS103	AW5
AA21	VSS5	VSS104	AW7
AA24	VSS6	VSS105	AY10
AA29	VSS7	VSS106	AY24
AB20	VSS8	VSS107	AY37
AB23	VSS9	VSS108	AY42
AB26	VSS10	VSS109	AY43
AB28	VSS11	VSS110	AY45
AB31	VSS12	VSS111	AY47
AC10	VSS13	VSS112	AY50
AC13	VSS14	VSS113	B10
AC3	VSS15	VSS114	B20
AC39	VSS16	VSS115	B24
AC43	VSS17	VSS116	B29
AC47	VSS18	VSS117	B30
AD1	VSS19	VSS118	B35
AD21	VSS20	VSS119	B38
AD26	VSS21	VSS120	B43
AD29	VSS22	VSS121	B46
AD3	VSS23	VSS122	B5
AD41	VSS24	VSS123	B8
AD45	VSS25	VSS124	BA1
AD49	VSS26	VSS125	BA17
AD5	VSS27	VSS126	BA18
AD50	VSS28	VSS127	BA2
AD8	VSS29	VSS128	BA24
AE10	VSS30	VSS129	BB12
AE14	VSS31	VSS130	BB25
AE6	VSS32	VSS131	BB40
AF20	VSS33	VSS132	BB44
AF23	VSS34	VSS133	BB49
AF24	VSS35	VSS134	BB8
AF31	VSS36	VSS135	BC16
AG2	VSS37	VSS136	BC24
AG38	VSS38	VSS137	BC25
AG43	VSS39	VSS138	BC36
AG47	VSS40	VSS139	BC40
AG50	VSS41	VSS140	BC51
AH3	VSS42	VSS141	BD13
AH40	VSS43	VSS142	BD2
AH41	VSS44	VSS143	BD28
AH7	VSS45	VSS144	BD45
AH9	VSS46	VSS145	BD48
AJ11	VSS47	VSS146	BD5
AJ13	VSS48	VSS147	BE1
AJ21	VSS49	VSS148	BE19
AJ24	VSS50	VSS149	BE23
AJ29	VSS51	VSS150	BE30
AJ32	VSS52	VSS151	BE42
AJ43	VSS53	VSS152	BE51
AJ45	VSS54	VSS153	BE8
AJ49	VSS55	VSS154	BF12
AK20	VSS56	VSS155	BF16
AK21	VSS57	VSS156	BF36
AK26	VSS58	VSS157	BG19
AK28	VSS59	VSS158	BG2
AK31	VSS60	VSS159	BG24
AK51	VSS61	VSS160	BG29
AL1	VSS62	VSS161	BG39
AM11	VSS63	VSS162	BG48
AM13	VSS64	VSS163	BG5
AM3	VSS65	VSS164	BG51
AM4	VSS66	VSS165	BH17
AM41	VSS67	VSS166	BH30
AM45	VSS68	VSS167	BH44
AN1	VSS69	VSS168	BH46
AN38	VSS70	VSS169	BH8
AN39	VSS71	VSS170	BJ11
AN43	VSS72	VSS171	BJ13
AN5	VSS73	VSS172	BJ38
AN7	VSS74	VSS173	BJ4
AP4	VSS75	VSS174	BJ42
AP48	VSS76	VSS175	BJ46
AP50	VSS77	VSS176	BK15
AR11	VSS78	VSS177	BK17
AR2	VSS79	VSS178	BK25
AR39	VSS80	VSS179	BK29
AR44	VSS81	VSS180	BK36
AR47	VSS82	VSS181	BK40
AR7	VSS83	VSS182	BK44
AT10	VSS84	VSS183	BK6
AT14	VSS85	VSS184	BK8
AT41	VSS86	VSS185	BL11
AT49	VSS87	VSS186	BL13
AU1	VSS88	VSS187	BL19
AU23	VSS89	VSS188	BL22
AU29	VSS90	VSS189	BL37
AU3	VSS91	VSS190	BL47
AU36	VSS92	VSS191	C12
AU49	VSS93	VSS192	C16
AU51	VSS94	VSS193	C19
AV39	VSS95	VSS194	C28
AV48	VSS96	VSS195	C29
AW1	VSS97	VSS196	C33
AW12	VSS98	VSS197	C36
AW16	VSS99	VSS198	C41

OMIT

U1400
CRESTLINE
FCBGA
(10 OF 10)
VSS

C46	VSS199	VSS287	W11
C50	VSS200	VSS288	W39
C7	VSS201	VSS289	W43
D13	VSS202	VSS290	W47
D24	VSS203	VSS291	W5
D3	VSS204	VSS292	W7
D32	VSS205	VSS293	Y13
D39	VSS206	VSS294	Y2
D45	VSS207	VSS295	Y41
D49	VSS208	VSS296	Y45
E10	VSS209	VSS297	Y49
E16	VSS210	VSS298	Y5
E24	VSS211	VSS299	Y50
E28	VSS212	VSS300	Y11
E32	VSS213	VSS301	P29
E47	VSS214		
F19	VSS215		
F36	VSS216	TDE_SENSE VSS302	T29
F4	VSS217		
F40	VSS218		
F50	VSS219	TDE_FORCE VSS303	T31
G1	VSS220		
G13	VSS221		
G16	VSS222	TDB_FORCE VSS304	T33
G19	VSS223		
G24	VSS224		
G28	VSS225	TDB_SENSE VSS305	R28
G29	VSS226		
G33	VSS227		
G42	VSS228		
G45	VSS229	VSS306	AA32
G48	VSS230	VSS307	AB32
G8	VSS231	VSS308	AD32
H24	VSS232	VSS309	AF28
H28	VSS233	VSS310	AF29
H4	VSS234	VSS311	AT27
H45	VSS235	VSS312	AV25
J11	VSS236	VSS313	H50
J16	VSS237		
J2	VSS238		
J24	VSS239		
J28	VSS240		
J33	VSS241		
J35	VSS242		
J39	VSS243		
K12	VSS245		
K47	VSS246		
K8	VSS247		
L1	VSS248		
L17	VSS249		
L20	VSS250		
L24	VSS251		
L28	VSS252		
L3	VSS253		
L33	VSS254		
L49	VSS255		
M28	VSS256		
M42	VSS257		
M46	VSS258		
M49	VSS259		
M5	VSS260		
M50	VSS261		
M9	VSS262		
N11	VSS263		
N14	VSS264		
N17	VSS265		
N29	VSS266		
N32	VSS267		
N36	VSS268		
N39	VSS269		
N44	VSS270		
N49	VSS271		
N7	VSS272		
P19	VSS273		
P2	VSS274		
P23	VSS275		
P3	VSS276		
P50	VSS277		
R49	VSS278		
T39	VSS279		
T43	VSS280		
T47	VSS281		
U41	VSS282		
U45	VSS283		
U50	VSS284		
V2	VSS285		
V3	VSS286		

Crestline Thermal Diode Pins

Mainly for investigation. If not used, alias these nets directly to GND.

TDE_SENSE T29 — GND

NOTE: TDE = _P

TDE_FORCE T31 — GND

TDB_FORCE T33 — GND

NOTE: TDB = _N

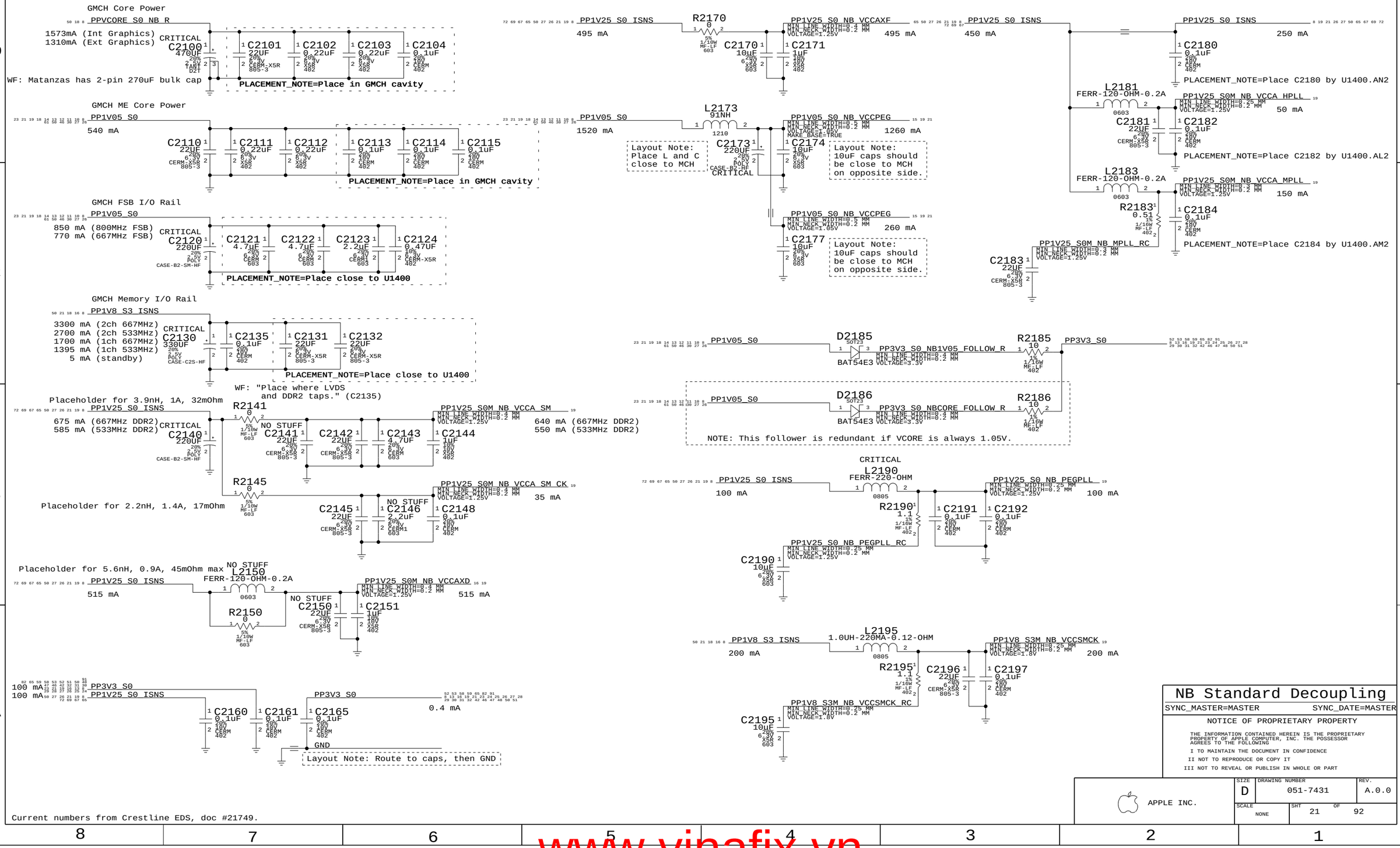
TDB_SENSE R28 — GND

NB Grounds

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

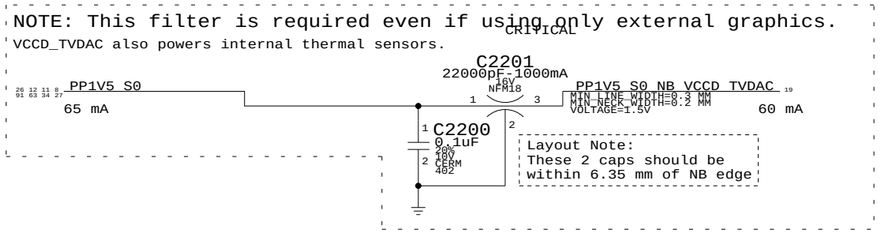
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 20 OF 92	



Crestline LVDS Strapping

NOTE: This filter is required even if using only external graphics.
VCCD_TVDAC also powers internal thermal sensors.



GND ×40

22 15	NC_LVDS_BKLT_CTL	NC_LVDS_BKLT_CTL	15 22
22 15	NC_LVDS_BKLT_EN	NC_LVDS_BKLT_EN	15 22
22 15	NC_LVDS_VDD_EN	NC_LVDS_VDD_EN	15 22
84 22 15	NC_LVDS_IBG	NC_LVDS_IBG	15 22 84
22 15	NC_LVDS_VBG	NC_LVDS_VBG	15 22
84 22 15	NC_LVDS_A_CLKN	NC_LVDS_A_CLKN	15 22 84
84 22 15	NC_LVDS_A_CLKP	NC_LVDS_A_CLKP	15 22 84
84 22 15	NC_LVDS_B_CLKN	NC_LVDS_B_CLKN	15 22 84
84 22 15	NC_LVDS_B_CLKP	NC_LVDS_B_CLKP	15 22 84
22 15	NC_LVDS_A_DATAN<0>	NC_LVDS_A_DATAN<0>	15 22
84 15	LVDS_A_DATA_N<1>	NC_LVDS_A_DATAN<1>	
84 15	LVDS_A_DATA_N<2>	NC_LVDS_A_DATAN<2>	
22 15	NC_LVDS_A_DATAP<0>	NC_LVDS_A_DATAP<0>	15 22
84 15	LVDS_A_DATA_P<1>	NC_LVDS_A_DATAP<1>	
84 15	LVDS_A_DATA_P<2>	NC_LVDS_A_DATAP<2>	
22 15	NC_LVDS_B_DATAN<0>	NC_LVDS_B_DATAN<0>	15 22
84 15	LVDS_B_DATA_N<1>	NC_LVDS_B_DATAN<1>	
84 15	LVDS_B_DATA_N<2>	NC_LVDS_B_DATAN<2>	
22 15	NC_LVDS_B_DATAP<0>	NC_LVDS_B_DATAP<0>	15 22
84 15	LVDS_B_DATA_P<1>	NC_LVDS_B_DATAP<1>	
84 15	LVDS_B_DATA_P<2>	NC_LVDS_B_DATAP<2>	
22 15	NC_LVDS_VREFH	NC_LVDS_VREFH	15 22
22 15	NC_LVDS_VREFL	NC_LVDS_VREFL	15 22
22 16	TP_GFX_VID<1>	TP_GFX_VID<1>	16 22
16	GFX_VID<2>	TP_GFX_VID<2>	
16	GFX_VID<3>	TP_GFX_VID<3>	
16	GFX_VID<4>	TP_GFX_VID<4>	
22 16	TP_GFX_VR_EN	TP_GFX_VR_EN	16 22

All rows: MAKE_BASE=TRUE NO_TEST=TRUE

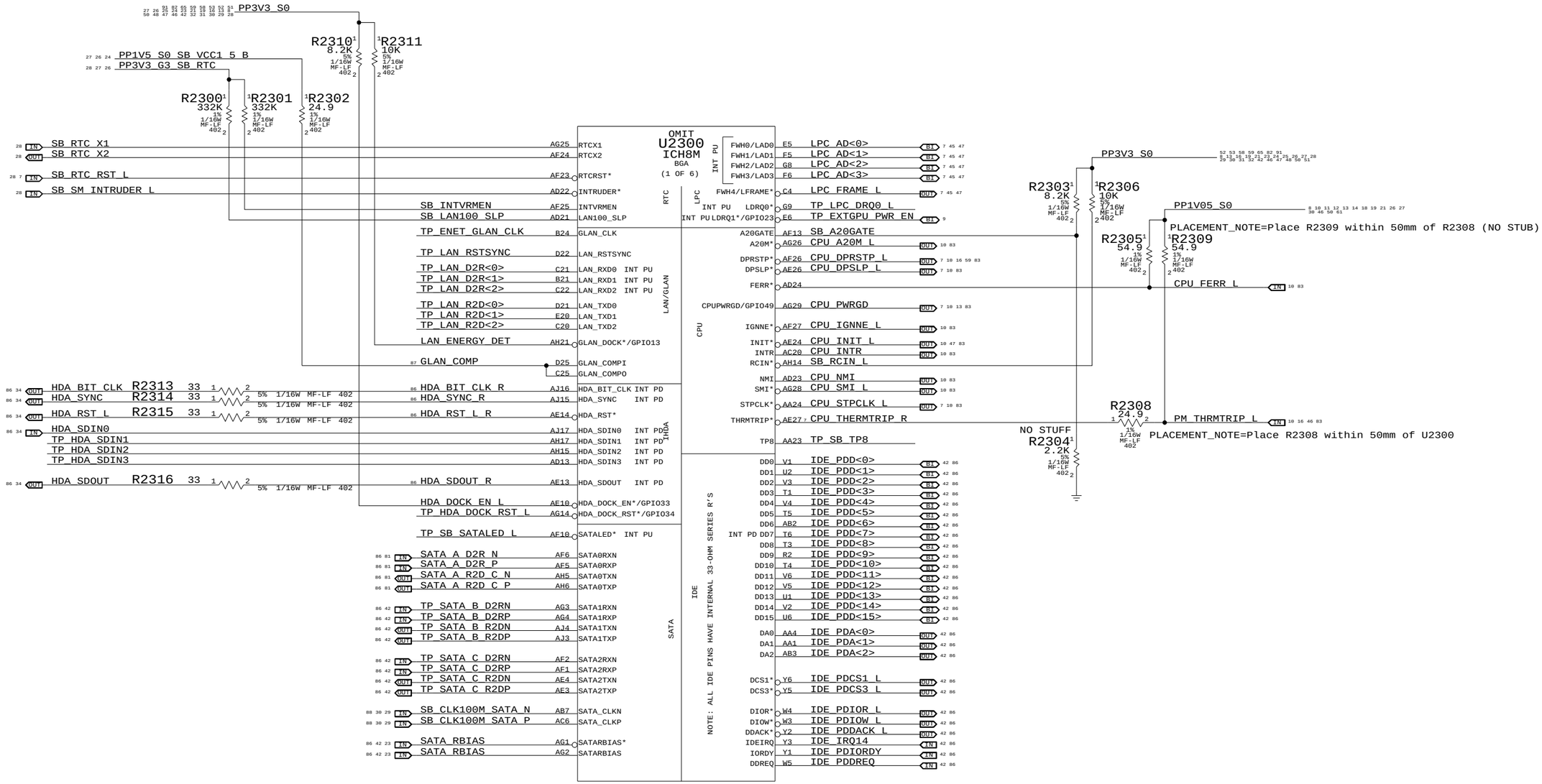
Current numbers from Crestline EDS Addendum, doc #20127.

NB Graphics Decoupling

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 22 OF 92	



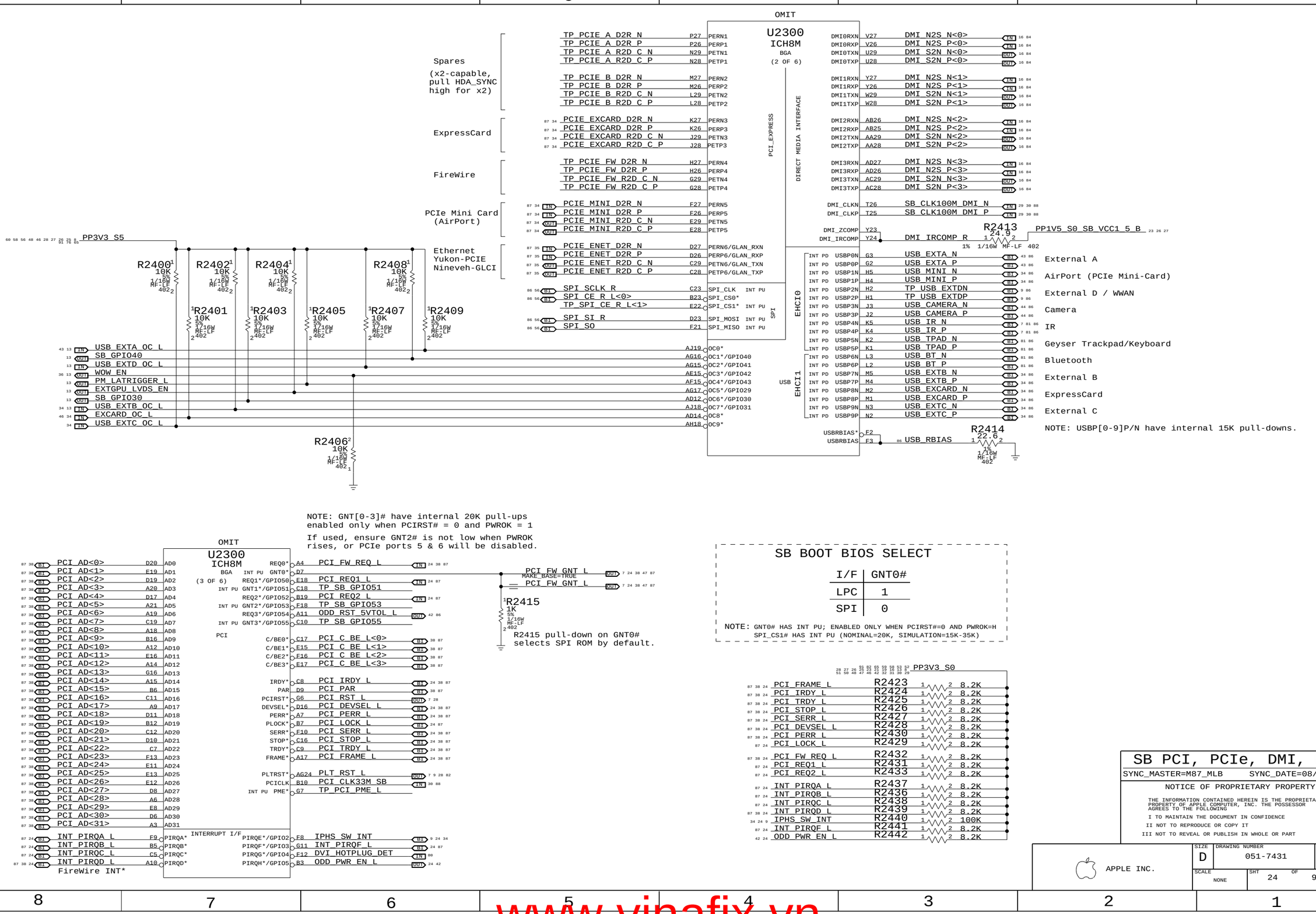
	HDA
HDA_BIT_CLK	24.000MHZ CLOCK W/INTERNAL WEAK PD
HDA_RST#	
HDA_SDIN[0-2]	INTEGRATED PDs
HDA_SDOUT	INTEGRATED PD
ACZ_SYNC	INTEGRATED PD

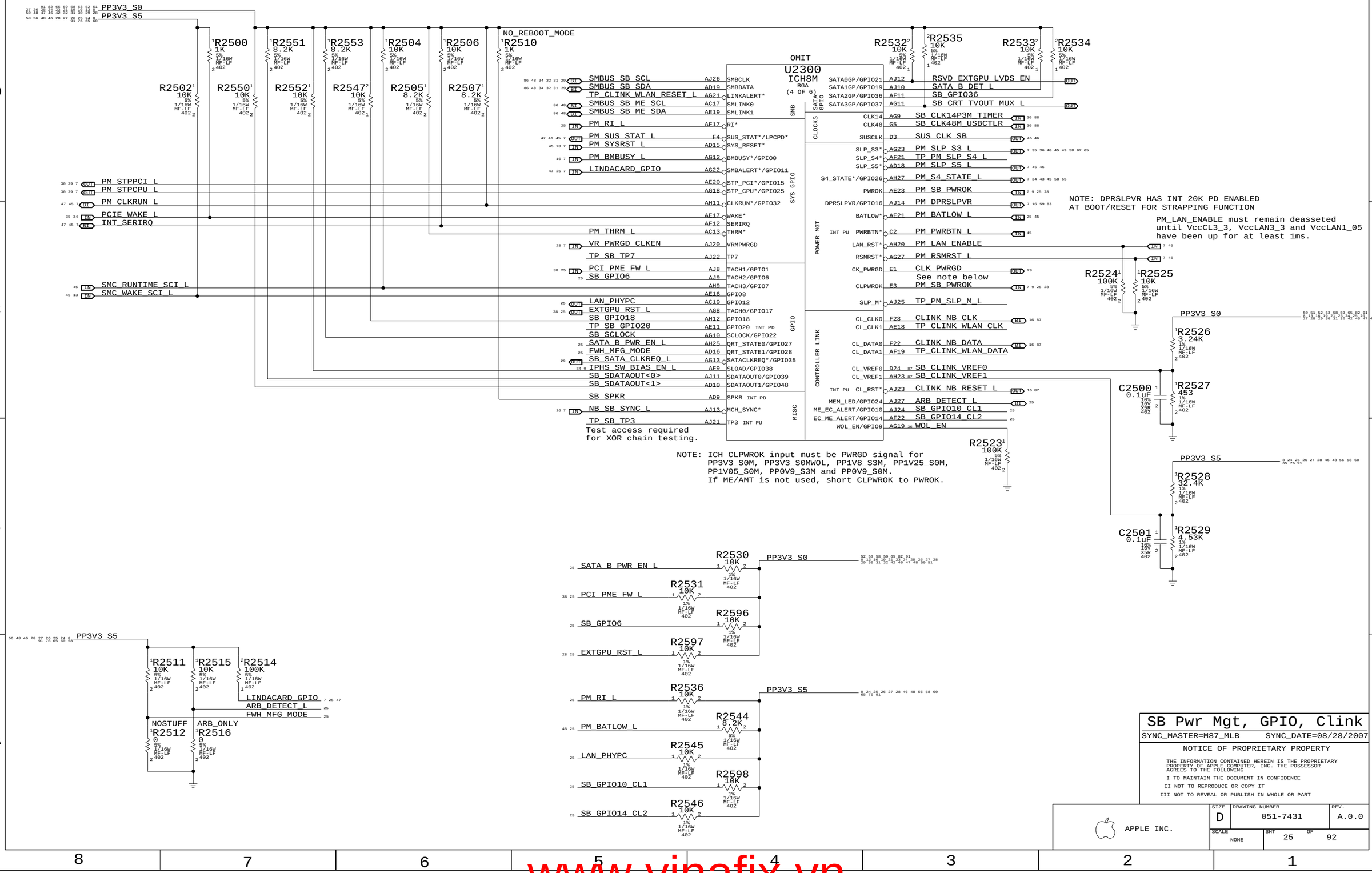
SB Enet, Disk, FSB, LPC

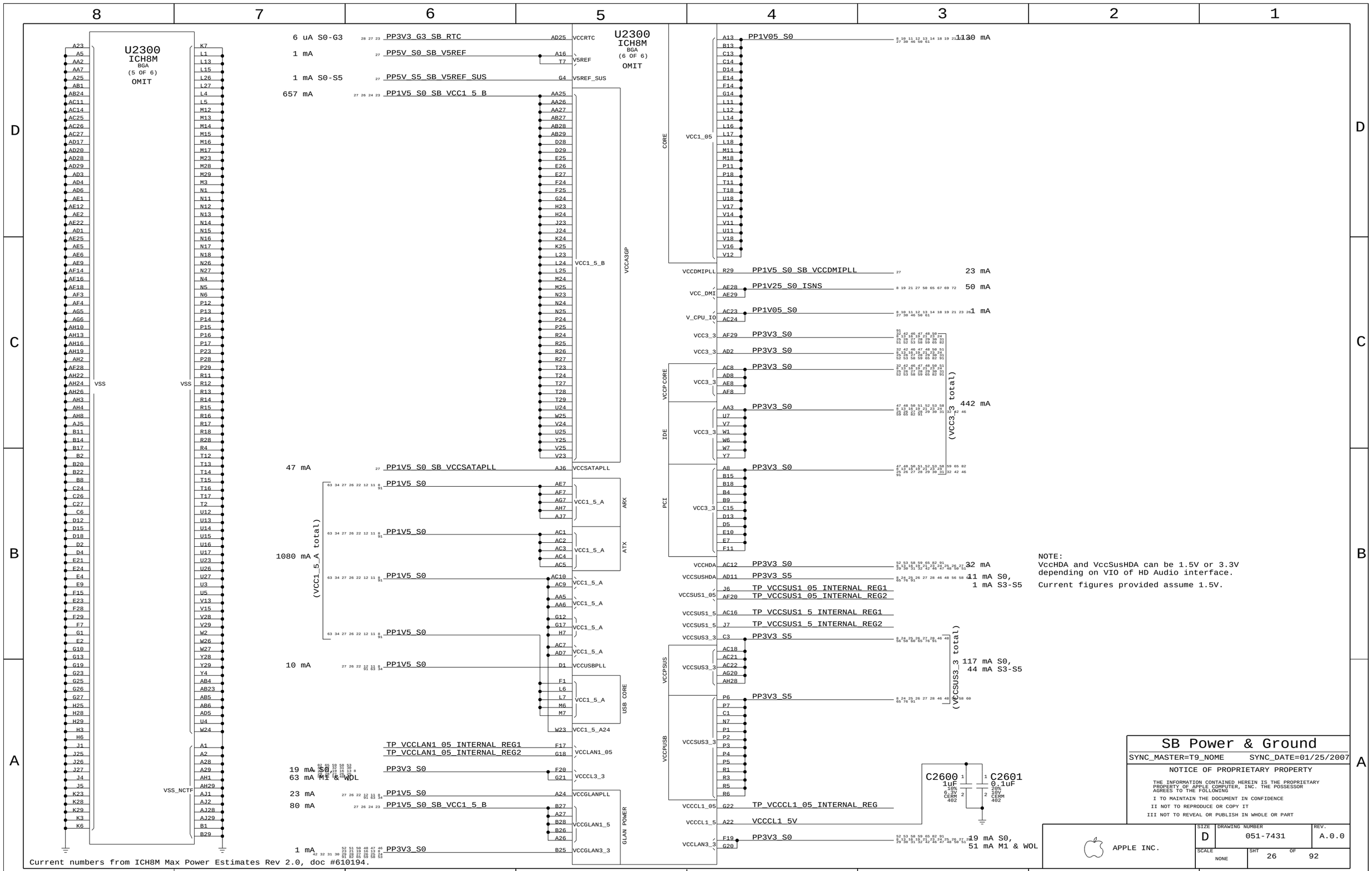
SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 23 OF 92	







PP3V3_S5
PP5V_S5
1 mA S0-S5
ICH V5REF_SUS Filter & Follower
(ICH Reference for 5V Tolerance on Resume Well Inputs)
R2701 10 5% 1/16W MF-LF 402
D2702 BAT54DW SOT-363
PP5V_S5_SB_V5REF_SUS
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=5V
C2704 0.1UF 10% 16V X5R 402
1 mA S0-S5
PLACEMENT NOTE:
PLACE C2704 < 2.54MM OF PIN G4 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY

PP3V3_S0
PP5V_S0
1 mA
ICH V5REF Filter & Follower
(ICH Reference for 5V Tolerance on Core Well Inputs)
R2702 100 5% 1/16W MF-LF 402
D2702 BAT54DW SOT-363
PP5V_S0_SB_V5REF
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=5V
C2703 1UF 10% 16V X5R 402
1 mA
PLACEMENT NOTE:
PLACE C2703 < 2.54MM OF PIN A16..T7 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY

PLACEMENT NOTE:
PLACE C2700 & C2705-07 < 2.54MM OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
DISTRIBUTED BETWEEN AA25..V23

ICH VCC1_5_B BYPASS
(ICH IO,LOGIC 1.5V PWR)
PP1V5_S0
837 mA
L2700 FERR-330-OHM-1.5A 0805-1
C2700 220UF 20% 6.3V CASE-B2-DE CRITICAL
C2705 22UF 20% 6.3V CERM-X5R 805-3
C2706 22UF 20% 6.3V CERM-X5R 805-3
C2707 2.2UF 20% 6.3V CERM1 603
PP1V5_S0_SB_VCC1_5_B
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
657 mA
PP1V5_S0_SB_VCC1_5_B
80 mA
C2736 4.7UF 20% 6.3V CERM 603
PLACEMENT NOTE:
PLACE C2736 NEAR PIN B27..A26

ICH VCCGLANPLL Filter
(ICH GLAN PLL PWR)
PP1V5_S0
33 mA
C2732 2.2UF 20% 6.3V CERM1 603
33 mA
PLACEMENT NOTE:
PLACE CAPS < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN A24

ICH VCCSATAPLL Filter
(ICH SATA PLL PWR)
R2735 0 5% 1/10W MF-LF 402
PP1V5_S0_SB_VCCSATAPLL_F
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.5V
47 mA
L2702 10UH-100MA 0805
C2735 10UF 20% 6.3V X5R 603
PP1V5_S0_SB_VCCSATAPLL
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.5V
47 mA
C2717 1UF 10% 6.3V CERM 402
PLACEMENT NOTE:
PLACE CAPS < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AJ6

ICH VCCDMIPLL Filter
(ICH DMI PLL PWR)
R2700 1 5% 1/10W MF-LF 603
PP1V5_S0_SB_VCCDMIPLL_F
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.5V
23 mA
L2703 1.0UH-0.5A 1210
C2708 10UF 10% 6.3V X5R 603
PP1V5_S0_SB_VCCDMIPLL
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.5V
23 mA
C2701 0.01UF 10% 16V CERM 402
PLACEMENT NOTE:
PLACE CAPS < 2.54MM OF SB ON
SECONDARY SIDE OR 3.56MM ON PRIMARY

Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.

ICH VCCRTC BYPASS
(ICH RTC 3.3V PWR)
0.6 uA G3
PP3V3_G3_SB_RTC
C2729 0.1UF 10% 16V X5R 402
C2730 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE CAPS NEAR PIN AD25 OF SB

ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
(VCCSUS3_3 Total)
PP3V3_S5
C2731 0.1UF 10% 16V X5R 402
C2734 0.1UF 10% 16V X5R 402
117 mA S0 /
44 mA S3-S5
PLACEMENT NOTE:
PLACE CAPS NEAR PINS AC18..AH28

ICH USB/VCCSUS3_3 BYPASS
(ICH SUSPEND USB 3.3V PWR)
PP3V3_S5
C2733 4.7UF 20% 6.3V CERM 603
PLACEMENT NOTE:
PLACE CAP NEAR PINS
P6..R6

ICH VCC_PAUX/VCCLAN3_3 BYPASS
(ICH LAN I/F BUFFER 3.3V PWR)
38 mA S0 /
114 mA M1 & WOL
PP3V3_S0
PP3V3_S0
C2719 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE CAP UNDER SB NEAR PINS
F19 AND G20

ICH IDE/VCC3_3 BYPASS
(ICH IDE I/O 3.3V PWR)
(VCC3_3 Total)
PP3V3_S0
C2725 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS AA3...Y7

PP3V3_S0
C2738 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AD2

442 mA
PP3V3_S0
C2737 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE CAP < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AF29

ICH PCI/VCC3_3 BYPASS
(ICH PCI I/O 3.3V PWR)
PP3V3_S0
C2726 0.1UF 10% 16V X5R 402
C2727 0.1UF 10% 16V X5R 402
C2728 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
DISTRIBUTE IN PCI SECTION OF SB
NEAR PINS A8 ... F11

ICH VCCHDA BYPASS
(ICH INTEL HDA CORE 3.3V/1.5V PWR)
32 mA
(@ 1.5V)
PP3V3_S0
C2721 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AC12

ICH VCCSUSHDA BYPASS
(ICH INTEL HDA SUSPEND 3.3V/1.5V PWR)
11 mA S0 /
1 mA S3-S5
(@ 1.5V)
PP3V3_S5
C2741 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AD11

ICH VCC1_5_A/ARX BYPASS
(ICH LOGIC&IO[ARX] 1.5V PWR)
(VCC1_5_A Total)
1080 mA
PP1V5_S0
C2711 1UF 10% 6.3V CERM 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS AE7..AJ7

ICH VCC1_5_A/ATX BYPASS
(ICH LOGIC&IO[ATX] 1.5V PWR)
PP1V5_S0
C2714 1UF 10% 6.3V CERM 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AC1..AC5

ICH USB CORE/VCC1_5_A BYPASS
(ICH USB CORE 1.5V PWR)
PP1V5_S0
C2712 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS F1..M7

ICH VCCUSBPLL BYPASS
(ICH USB PLL 1.5V PWR)
10 mA
PP1V5_S0
C2715 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE C2715 NEAR PIN D1 OF SB

50 mA
PP1V25_S0_ISNS
C2739 22UF 20% 6.3V CERM-X5R 805-3
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AE29

ICH CORE/VCC1_05 BYPASS
(ICH CORE 1.05V PWR)
1130 mA
PP1V05_S0
C2718 0.1UF 10% 16V X5R 402
C2702 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE CAPS AT EDGE OF SB

ICH V_CPU_IO BYPASS
(ICH CPU I/O 1.05V PWR)
1 mA
PP1V05_S0
C2724 4.7UF 20% 6.3V CERM 603
C2723 0.1UF 10% 16V X5R 402
C2722 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE NEAR PINS AC23,AC24 OF SB

SB Decoupling

SYNC_MASTER=MASTER SYNC_DATE=MASTER

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 27 OF 92	

RTC Power Sources

Coin-Cell Connector

CRITICAL
J2800
BM02B-ACHKS-GAN-TF-LF-SN-M
M-RT-SM

518S0487

PPVBATT_G3_RTC
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

R2800
1K
5%
1/10W
MF-LF
402

PP3V42_G3H

PPVBATT_G3_RTC_R
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

D2805
BAT54DW
SOT-363

NC NC NC NC

PP3V3_G3_SB_RTC
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

R2806
20K
5%
1/10W
MF-LF
402

SB_RTC_RST_L

R2805
1M
5%
1/10W
MF-LF
402

C2806
1UF
10%
6.3V
CERM
402

C2805
1UF
10%
6.3V
CERM
402

SB_SM_INTRUDER_L

NOTE: R2800 and D2805 form the double-
fault protection for RTC battery.

Platform Reset Connections

Unbuffered

PLT_RST_L
MAKE_BASE=TRUE

R2860
100
5%
1/16W
MF-LF
402
NB_RESET_L

R2861
0
5%
1/16W
MF-LF
402
FW_PLT_RST_L

R2862
100
5%
1/16W
MF-LF
402
SMC_LRESET_L

R2863
0
5%
1/16W
MF-LF
402
DEBUG_RESET_L

R2864
100
5%
1/16W
MF-LF
402
LIO_PLT_RST_L

R2865
0
5%
1/16W
MF-LF
402
ENET_RESET_L

SB RTC Crystal

SB_RTC_X1

R2810
0
5%
1/16W
MF-LF
402

SB_RTC_X1_R

C2810
12pF
5%
50V
CERM
402

R2811
10M
5%
1/16W
MF-LF
402

CRITICAL
Y2810
32.768K
SM-2

NC
NC

C2811
12pF
5%
50V
CERM
402

SB_RTC_X2

System Reset "Button"

PP3V3_S5

R2825
10K
5%
1/16W
MF-LF
402

ITP&XDP
R2826
1K
5%
1/16W
MF-LF
402

XDP_DBRESET_L
PM_SYSRST_L

OMIT
R2820
0
5%
1/10W
MF-LF
603

SILK_PART=SYS_RST
This part is never stuffed,
it provides a set of pads
on the board to short or
to solder a reset button.

VRMPWRGD Inverter

PP3V3_S0

C2830
0.1UF
20%
10V
CERM
402

MC74VHC1G00
SC70-5
U2830

VR_PWRGD_CLKEN_L
VR_PWRGD_CLKEN

PWROK Circuit

PP3V3_S0

C2840
0.1UF
20%
10V
CERM
402

MC74VHC1G08
SC70
U2840

VR_PWRGOOD_DELAY
ALL_SYS_PWRGD
PM_SB_PWROK

R2841
10K
5%
1/10W
MF-LF
402

R2840
10K
5%
1/16W
MF-LF
402

CPU VCore ForcePSI

CPU_PSI_L
MAKE_BASE=TRUE
CPU_PSI_L

PP3V3_S0

C2880
0.1UF
20%
10V
CERM
402

MC74VHC1G08
SC70
U2880

EXTGPU_RST_L
GPU_RESET_R_L

R2881
0
5%
1/16W
MF-LF
402

GPU_RESET_L

PCI Reset Connections

PCI_RST_L

R2890
100
5%
1/16W
MF-LF
402

PCI_FW_RST_L

SB Misc

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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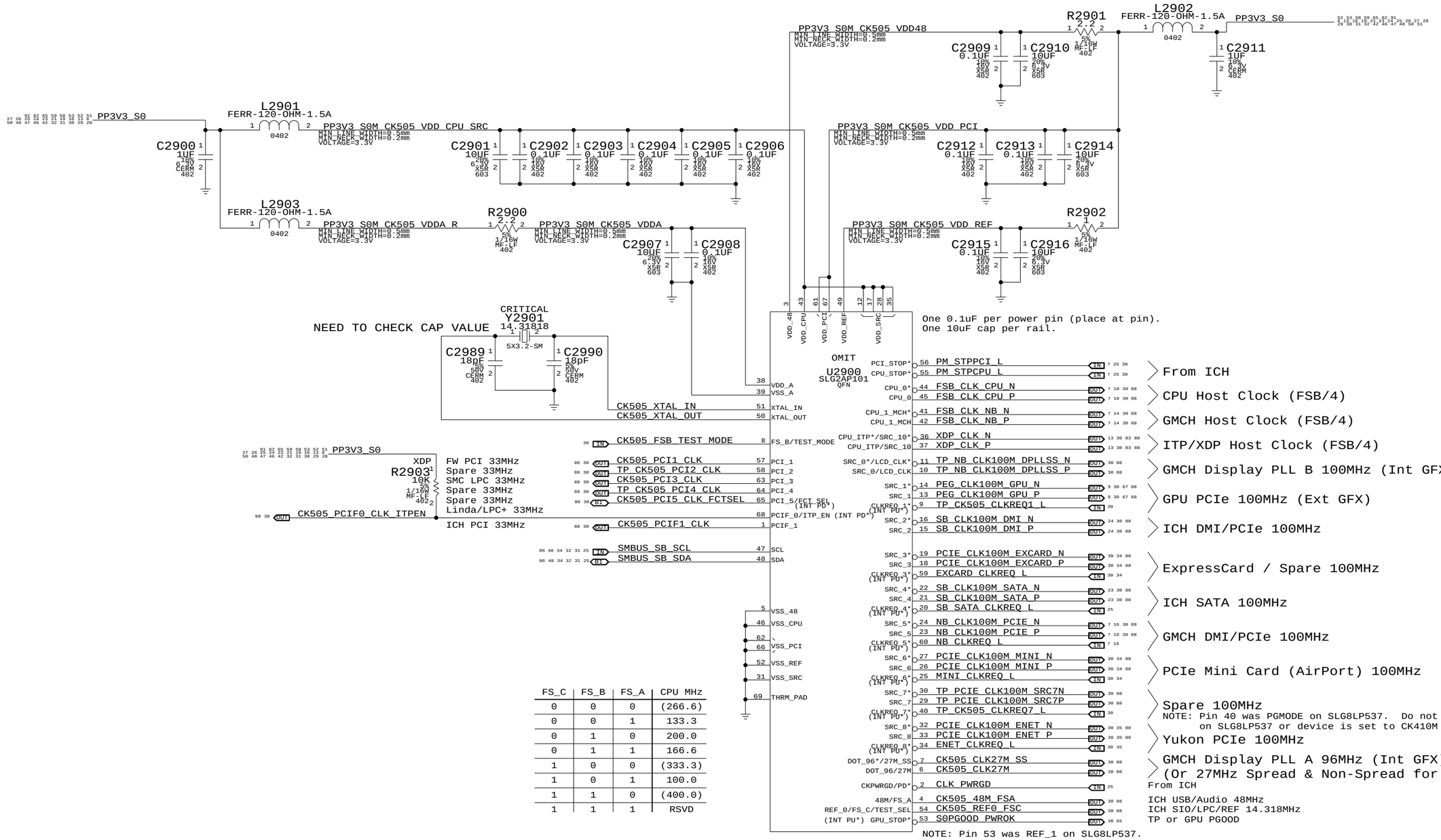
SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 28 OF 92	



FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

FCT_SEL	PIN 6	PIN 7	PIN 10	PIN 11	
0	DOT_96+	DOT_96-	LCD_CLK+	LCD_CLK-	(For Internal Graphics)
1	27M	27M w/SS	SRC_0+	SRC_0-	(For External Graphics)

Clock (CK505)

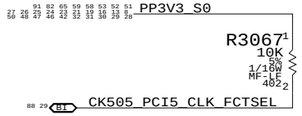
SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

APPLE INC.

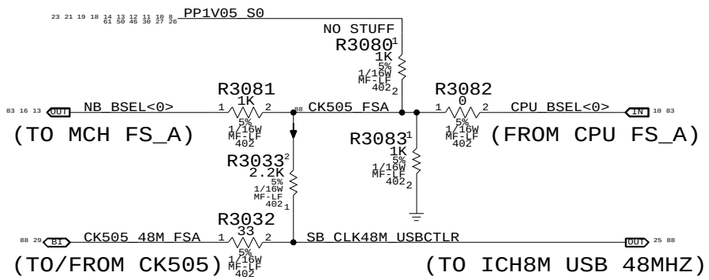
SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 29 OF 92	

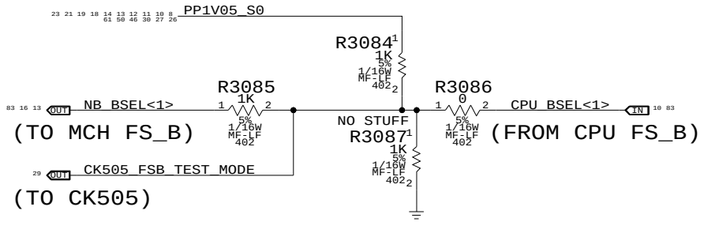
CK505 Configuration Straps

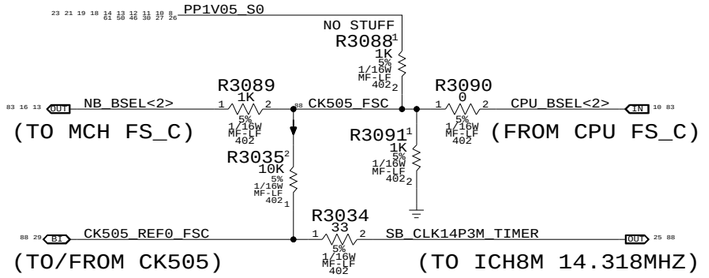
FCT_SEL (GFX clock select)



FS_A, FS_B, FS_C (Host clock freq select)







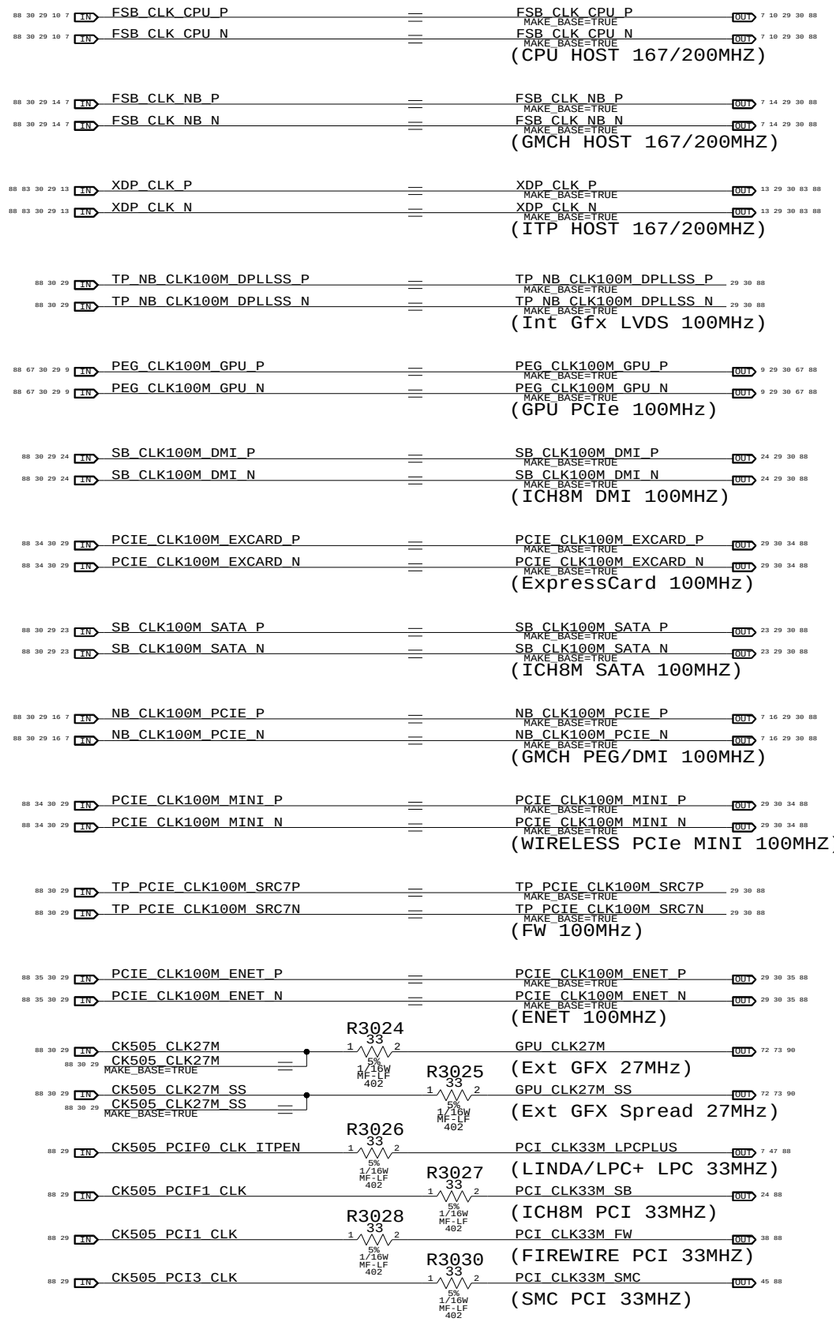
FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

NO STUFF R3082, R3086 & R3090 for manual CPU clk frequency.

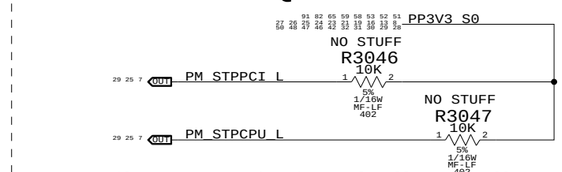
(Only 100-200MHz supported by SLG8LP536 and CY28545-5)

CLK Termination

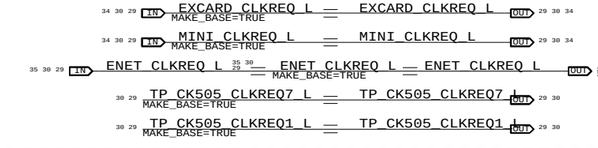
(Note: HOST/SRC/GFX clock termination removed. Silego SL8GLP536 or equiv. support only)



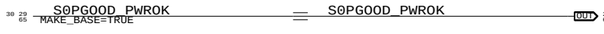
CLKREQ Controls



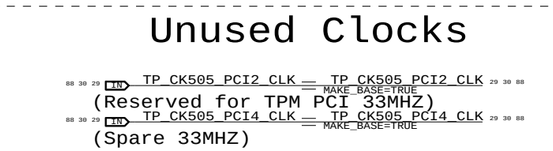
Silego SLG2AP101 has internal pull-ups on all CLKREQ# pins. Support for SL8GLP537 or equiv. only. NB and SATA CLKREQs are not remappable (and thus are not shown here).



GPU Clock Gating



Unused Clocks



Clock Termination

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0

SCALE: NONE SHT 30 OF 92

Page Notes

Power aliases required by this page:
- =PP1V8_S3M_MEM_A
- =PP0V9_S3M_MEM_DIMMVREFA
- =PPSPD_S0M_MEM_A (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

"Factory" (thru-hole) slot

62 32 16 8 PP0V9_S3_MEM_VREF

C3101 2.2uF 20% 6.3V CERM 603

C3100 0.1uF 20% 10V CERM 402

91 62 50 38 32 31 8 PP1V8_S3

201

CRITICAL
J3100
F-RT-TH1
DDR2-SODIMM-DUAL

		1B	VREF	VSS0	2B		
		3B	VSS1	DQ4	4B	MEM_A_DQ<9>	17 85
85 17	MEM_A_DQ<14>	5B	DQ0	DQ5	6B	MEM_A_DQ<15>	17 85
85 17	MEM_A_DQ<13>	7B	DQ1	VSS2	8B		
		9B	VSS4	DM0	10B	MEM_A_DM<1>	17 85
85 17	MEM_A_DQS_N<1>	11B	DQS0*	VSS5	12B		
85 17	MEM_A_DQS_P<1>	13B	DQS0	DQ6	14B	MEM_A_DQ<8>	17 85
		15B	VSS6	DQ7	16B	MEM_A_DQ<12>	17 85
85 17	MEM_A_DQ<10>	17B	DQ2	VSS7	18B		
85 17	MEM_A_DQ<11>	19B	DQ3	DQ12	20B	MEM_A_DQ<2>	17 85
		21B	VSS8	DQ13	22B	MEM_A_DQ<3>	17 85
85 17	MEM_A_DQ<7>	23B	DQ8	VSS9	24B		
85 17	MEM_A_DQ<0>	25B	DQ9	DM1	26B	MEM_A_DM<0>	17 85
		27B	VSS10	VSS11	28B		
85 17	MEM_A_DQS_N<0>	29B	DQS1*	CK0	30B	MEM_CLK_P<0>	16 85
85 17	MEM_A_DQS_P<0>	31B	DQS1	CK0*	32B	MEM_CLK_N<0>	16 85
		33B	VSS12	VSS13	34B		
85 17	MEM_A_DQ<6>	35B	DQ10	DQ14	36B	MEM_A_DQ<1>	17 85
85 17	MEM_A_DQ<4>	37B	DQ11	DQ15	38B	MEM_A_DQ<5>	17 85
		39B	VSS14	VSS15	40B		
				KEY			
		41B	VSS16	VSS17	42B		
85 17	MEM_A_DQ<17>	43B	DQ16	DQ20	44B	MEM_A_DQ<18>	17 85
85 17	MEM_A_DQ<21>	45B	DQ17	DQ21	46B	MEM_A_DQ<20>	17 85
		47B	VSS18	VSS19	48B		
85 17	MEM_A_DQS_N<2>	49B	DQS2*	NC0	50B	PM_EXTTS_L<0>	16 45
85 17	MEM_A_DQS_P<2>	51B	DQS2	DM2	52B	MEM_A_DM<2>	17 85
		53B	VSS21	VSS22	54B		
85 17	MEM_A_DQ<23>	55B	DQ18	DQ22	56B	MEM_A_DQ<22>	17 85
85 17	MEM_A_DQ<16>	57B	DQ19	DQ23	58B	MEM_A_DQ<19>	17 85
		59B	VSS23	VSS24	60B		
85 17	MEM_A_DQ<31>	61B	DQ24	DQ28	62B	MEM_A_DQ<26>	17 85
85 17	MEM_A_DQ<27>	63B	DQ25	DQ29	64B	MEM_A_DQ<24>	17 85
		65B	VSS25	VSS26	66B		
85 17	MEM_A_DM<3>	67B	DM3	DQS3*	68B	MEM_A_DQS_N<3>	17 85
	NC	69B	NC1	DQS3	70B	MEM_A_DQS_P<3>	17 85
		71B	VSS27	VSS28	72B		
85 17	MEM_A_DQ<30>	73B	DQ26	DQ30	74B	MEM_A_DQ<25>	17 85
85 17	MEM_A_DQ<28>	75B	DQ27	DQ31	76B	MEM_A_DQ<29>	17 85
		77B	VSS29	VSS30	78B		
85 33 16	MEM_CKE<0>	79B	CKE0	NC/CKE1	80B	MEM_CKE<1>	16 33 85
		81B	VDD0	VDD1	82B		
	NC	83B	NC2	NC/A15	84B	TP_MEM_A_A<15>	9
85 33 17	MEM_A_BS<2>	85B	BA2	NC/A14	86B	MEM_A_A<14>	16 33 85
		87B	VDD2	VDD3	88B		
85 33 17	MEM_A_A<12>	89B	A12	A11	90B	MEM_A_A<11>	17 33 85
85 33 17	MEM_A_A<9>	91B	A9	A7	92B	MEM_A_A<7>	17 33 85
85 33 17	MEM_A_A<8>	93B	A8	A6	94B	MEM_A_A<6>	17 33 85
		95B	VDD4	VDD5	96B		
85 33 17	MEM_A_A<5>	97B	A5	A4	98B	MEM_A_A<4>	17 33 85
85 33 17	MEM_A_A<3>	99B	A3	A2	100B	MEM_A_A<2>	17 33 85
85 33 17	MEM_A_A<1>	101B	A1	A0	102B	MEM_A_A<0>	17 33 85
		103B	VDD6	VDD7	104B		
85 33 17	MEM_A_A<10>	105B	A10/AP	BA1	106B	MEM_A_BS<1>	17 33 85
85 33 17	MEM_A_BS<0>	107B	BA0	RAS*	108B	MEM_A_RAS_L	17 33 85
85 33 17	MEM_A_WE_L	109B	WE*	S0*	110B	MEM_CS_L<0>	16 33 85
		111B	VDD8	VDD9	112B		
85 33 17	MEM_A_CAS_L	113B	CAS*	ODT0	114B	MEM_ODT<0>	16 33 85
85 33 16	MEM_CS_L<1>	115B	NC/S1*	NC/A13	116B	MEM_A_A<13>	17 33 85
		117B	VDD10	VDD11	118B		
85 33 16	MEM_ODT<1>	119B	NC/ODT1	NC3	120B	NC	
		121B	VSS31	VSS32	122B		
85 17	MEM_A_DQ<36>	123B	DQ32	DQ36	124B	MEM_A_DQ<35>	17 85
85 17	MEM_A_DQ<38>	125B	DQ33	DQ37	126B	MEM_A_DQ<39>	17 85
		127B	VSS33	VSS34	128B		
85 17	MEM_A_DQS_N<4>	129B	DQS4*	DM4	130B	MEM_A_DM<4>	17 85
85 17	MEM_A_DQS_P<4>	131B	DQS4	VSS35	132B		
		133B	VSS36	DQ38	134B	MEM_A_DQ<33>	17 85
85 17	MEM_A_DQ<37>	135B	DQ34	DQ39	136B	MEM_A_DQ<32>	17 85
85 17	MEM_A_DQ<34>	137B	DQ35	VSS37	138B		
		139B	VSS38	DQ44	140B	MEM_A_DQ<63>	17 85
85 17	MEM_A_DQ<56>	141B	DQ40	DQ45	142B	MEM_A_DQ<62>	17 85
85 17	MEM_A_DQ<59>	143B	DQ41	VSS39	144B		
		145B	VSS40	DQS5*	146B	MEM_A_DQS_N<7>	17 85
85 17	MEM_A_DM<7>	147B	DM5	DQS5	148B	MEM_A_DQS_P<7>	17 85
		149B	VSS41	VSS42	150B		
85 17	MEM_A_DQ<58>	151B	DQ42	DQ46	152B	MEM_A_DQ<57>	17 85
85 17	MEM_A_DQ<60>	153B	DQ43	DQ47	154B	MEM_A_DQ<61>	17 85
		155B	VSS43	VSS44	156B		
85 17	MEM_A_DQ<51>	157B	DQ48	DQ52	158B	MEM_A_DQ<55>	17 85
85 17	MEM_A_DQ<54>	159B	DQ49	DQ53	160B	MEM_A_DQ<50>	17 85
		161B	VSS45	VSS46	162B		
	NC	163B	NC_TEST	CK1	164B	MEM_CLK_P<1>	16 85
		165B	VSS47	CK1*	166B	MEM_CLK_N<1>	16 85
85 17	MEM_A_DQS_N<6>	167B	DQS6*	VSS48	168B		
85 17	MEM_A_DQS_P<6>	169B	DQS6	DM6	170B	MEM_A_DM<6>	17 85
		171B	VSS49	VSS50	172B		
85 17	MEM_A_DQ<48>	173B	DQ50	DQ54	174B	MEM_A_DQ<49>	17 85
85 17	MEM_A_DQ<53>	175B	DQ51	DQ55	176B	MEM_A_DQ<52>	17 85
		177B	VSS51	VSS52	178B		
85 17	MEM_A_DQ<43>	179B	DQ56	DQ60	180B	MEM_A_DQ<45>	17 85
85 17	MEM_A_DQ<42>	181B	DQ57	DQ61	182B	MEM_A_DQ<40>	17 85
		183B	VSS53	VSS54	184B		
85 17	MEM_A_DM<5>	185B	DM7	DQS7*	186B	MEM_A_DQS_N<5>	17 85
		187B	VSS55	DQS7	188B	MEM_A_DQS_P<5>	17 85
85 17	MEM_A_DQ<46>	189B	DQ58	VSS56	190B		
85 17	MEM_A_DQ<41>	191B	DQ59	DQ62	192B	MEM_A_DQ<44>	17 85
	PP3V3_S0	193B	VSS57	DQ63	194B	MEM_A_DQ<47>	17 85
	SMBUS_SB_SDA	195B	SDA	VSS58	196B		
	SMBUS_SB_SCL	197B	SCL	SA0	198B		
		199B	VDDSPD	SA1	200B	ADDR=0xA0(WR)/0xA1(RD)	

516-0140 202

91 62 50 38 32 31 8 PP1V8_S3

C3108 10UF 20% 6.3V X5R 603

C3109 10UF 20% 6.3V X5R 603

C3110 1UF 10% 6.3V CERM 402

C3111 1UF 10% 6.3V CERM 402

C3112 1UF 10% 6.3V CERM 402

C3113 1UF 10% 6.3V CERM 402

C3114 1UF 10% 6.3V CERM 402

C3115 1UF 10% 6.3V CERM 402

C3116 1UF 10% 6.3V CERM 402

C3117 1UF 10% 6.3V CERM 402

C3118 1UF 10% 6.3V CERM 402

C3119 1UF 10% 6.3V CERM 402

C3120 1UF 10% 6.3V CERM 402

C3121 1UF 10% 6.3V CERM 402

DDR2 Bypass Caps
(For return current)

DDR2 SO-DIMM Connector A

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE	SHT	OF
NONE	31	92

Page Notes

Power aliases required by this page:
- =PP1V8_S3M_MEM_B
- =PP0V9_S3M_MEM_DIMMVREFB
- =PPSPD_S0M_MEM_B (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

"Expansion" (surface-mount) slot

PP0V9_S3_MEM_VREF

C3201 2.2uF 20% 6.3V CERM 603

C3200 0.1uF 20% 10V CERM 402

PP1V8_S3

CRITICAL
J3200
F-RT-SM-M9
DDR2-SODIMM-DUAL

	1A	VREF	VSS0	2A			
	3A	VSS1	DQ4	4A	MEM_B_DQ<9>	17 85	
85 17	MEM_B_DQ<15>	5A	DQ0	DQ5	6A	MEM_B_DQ<11>	17 85
85 17	MEM_B_DQ<14>	7A	DQ1		8A		
	9A	VSS4	DM0	10A	MEM_B_DM<1>	17 85	
85 17	MEM_B_DQS_N<1>	11A	DQS0*	VSS5	12A		
85 17	MEM_B_DQS_P<1>	13A	DQS0	DQ6	14A	MEM_B_DQ<12>	17 85
	15A	VSS6	DQ7	16A	MEM_B_DQ<8>	17 85	
85 17	MEM_B_DQ<10>	17A	DQ2	VSS7	18A		
85 17	MEM_B_DQ<13>	19A	DQ3	DQ12	20A	MEM_B_DQ<3>	17 85
	21A	VSS8	DQ13	22A	MEM_B_DQ<6>	17 85	
85 17	MEM_B_DQ<7>	23A	DQ8	VSS9	24A		
85 17	MEM_B_DQ<2>	25A	DQ9	DM1	26A	MEM_B_DM<0>	17 85
	27A	VSS10	VSS11	28A			
85 17	MEM_B_DQS_N<0>	29A	DQS1*	CK0	30A	MEM_CLK_P<4>	16 85
85 17	MEM_B_DQS_P<0>	31A	DQS1	CK0*	32A	MEM_CLK_N<4>	16 85
	33A	VSS12	VSS13	34A			
85 17	MEM_B_DQ<1>	35A	DQ10	DQ14	36A	MEM_B_DQ<0>	17 85
85 17	MEM_B_DQ<4>	37A	DQ11	DQ15	38A	MEM_B_DQ<5>	17 85
	39A	VSS14	VSS15	40A			
		KEY					
	41A	VSS16	VSS17	42A			
85 17	MEM_B_DQ<21>	43A	DQ16	DQ20	44A	MEM_B_DQ<22>	17 85
85 17	MEM_B_DQ<19>	45A	DQ17	DQ21	46A	MEM_B_DQ<18>	17 85
	47A	VSS18	VSS19	48A			
85 17	MEM_B_DQS_N<2>	49A	DQS2*	NC0	50A	PM_EXTTS_L<1>	16 45
85 17	MEM_B_DQS_P<2>	51A	DQS2	DM2	52A	MEM_B_DM<2>	17 85
	53A	VSS21	VSS22	54A			
85 17	MEM_B_DQ<20>	55A	DQ18	DQ22	56A	MEM_B_DQ<17>	17 85
85 17	MEM_B_DQ<23>	57A	DQ19	DQ23	58A	MEM_B_DQ<16>	17 85
	59A	VSS23	VSS24	60A			
85 17	MEM_B_DQ<29>	61A	DQ24	DQ28	62A	MEM_B_DQ<26>	17 85
85 17	MEM_B_DQ<24>	63A	DQ25	DQ29	64A	MEM_B_DQ<28>	17 85
	65A	VSS25	VSS26	66A			
85 17	MEM_B_DM<3>	67A	DM3	DQS3*	68A	MEM_B_DQS_N<3>	17 85
	NC	69A	NC1	DQS3	70A	MEM_B_DQS_P<3>	17 85
	71A	VSS27	VSS28	72A			
85 17	MEM_B_DQ<27>	73A	DQ26	DQ30	74A	MEM_B_DQ<31>	17 85
85 17	MEM_B_DQ<25>	75A	DQ27	DQ31	76A	MEM_B_DQ<30>	17 85
	77A	VSS29	VSS30	78A			
85 33 16	MEM_CKE<3>	79A	CKE0	NC/CKE1	80A	MEM_CKE<4>	16 33 85
	81A	VDD0	VDD1	82A			
	NC	83A	NC2	NC/A15	84A	TP_MEM_B_A<15>	9
85 33 17	MEM_B_BS<2>	85A	BA2	NC/A14	86A	MEM_B_A<14>	16 33 85
	87A	VDD2	VDD3	88A			
85 33 17	MEM_B_A<12>	89A	A12	A11	90A	MEM_B_A<11>	17 33 85
85 33 17	MEM_B_A<9>	91A	A9	A7	92A	MEM_B_A<7>	17 33 85
85 33 17	MEM_B_A<8>	93A	A8	A6	94A	MEM_B_A<6>	17 33 85
	95A	VDD4	VDD5	96A			
85 33 17	MEM_B_A<5>	97A	A5	A4	98A	MEM_B_A<4>	17 33 85
85 33 17	MEM_B_A<3>	99A	A3	A2	100A	MEM_B_A<2>	17 33 85
85 33 17	MEM_B_A<1>	101A	A1	A0	102A	MEM_B_A<0>	17 33 85
	103A	VDD6	VDD7	104A			
85 33 17	MEM_B_A<10>	105A	A10/AP	BA1	106A	MEM_B_BS<1>	17 33 85
85 33 17	MEM_B_BS<0>	107A	BA0	RAS*	108A	MEM_B_RAS_L	17 33 85
85 33 17	MEM_B_WE_L	109A	WE*	S0*	110A	MEM_CS_L<2>	16 33 85
	111A	VDD8	VDD9	112A			
85 33 17	MEM_B_CAS_L	113A	CAS*	ODT0	114A	MEM_ODT<2>	16 33 85
85 33 16	MEM_CS_L<3>	115A	NC/S1*	NC/A13	116A	MEM_B_A<13>	17 33 85
	117A	VDD10	VDD11	118A			
85 33 16	MEM_ODT<3>	119A	NC/ODT1	NC3	120A	NC	
	121A	VSS31	VSS32	122A			
85 17	MEM_B_DQ<36>	123A	DQ32	DQ36	124A	MEM_B_DQ<32>	17 85
85 17	MEM_B_DQ<33>	125A	DQ33	DQ37	126A	MEM_B_DQ<37>	17 85
	127A	VSS33	VSS34	128A			
85 17	MEM_B_DQS_N<4>	129A	DQS4*	DM4	130A	MEM_B_DM<4>	17 85
85 17	MEM_B_DQS_P<4>	131A	DQS4	VSS35	132A		
	133A	VSS36	DQ38	134A	MEM_B_DQ<38>	17 85	
85 17	MEM_B_DQ<34>	135A	DQ34	DQ39	136A	MEM_B_DQ<39>	17 85
85 17	MEM_B_DQ<35>	137A	DQ35	VSS37	138A		
	139A	VSS38	DQ44	140A	MEM_B_DQ<56>	17 85	
85 17	MEM_B_DQ<57>	141A	DQ40	DQ45	142A	MEM_B_DQ<59>	17 85
85 17	MEM_B_DQ<60>	143A	DQ41	VSS39	144A		
	145A	VSS40	DQS5*	146A	MEM_B_DQS_N<7>	17 85	
85 17	MEM_B_DM<7>	147A	DM5	DQS5	148A	MEM_B_DQS_P<7>	17 85
	149A	VSS41	VSS42	150A			
85 17	MEM_B_DQ<61>	151A	DQ42	DQ46	152A	MEM_B_DQ<63>	17 85
85 17	MEM_B_DQ<62>	153A	DQ43	DQ47	154A	MEM_B_DQ<58>	17 85
	155A	VSS43	VSS44	156A			
85 17	MEM_B_DQ<48>	157A	DQ48	DQ52	158A	MEM_B_DQ<54>	17 85
85 17	MEM_B_DQ<51>	159A	DQ49	DQ53	160A	MEM_B_DQ<53>	17 85
	161A	VSS45	VSS46	162A			
	NC	163A	NC_TEST	CK1	164A	MEM_CLK_P<3>	16 85
	165A	VSS47	CK1*	166A	MEM_CLK_N<3>	16 85	
85 17	MEM_B_DQS_N<6>	167A	DQS6*	VSS48	168A		
85 17	MEM_B_DQS_P<6>	169A	DQS6	DM6	170A	MEM_B_DM<6>	17 85
	171A	VSS49	VSS50	172A			
85 17	MEM_B_DQ<50>	173A	DQ50	DQ54	174A	MEM_B_DQ<52>	17 85
85 17	MEM_B_DQ<55>	175A	DQ51	DQ55	176A	MEM_B_DQ<49>	17 85
	177A	VSS51	VSS52	178A			
85 17	MEM_B_DQ<40>	179A	DQ56	DQ60	180A	MEM_B_DQ<46>	17 85
85 17	MEM_B_DQ<47>	181A	DQ57	DQ61	182A	MEM_B_DQ<43>	17 85
	183A	VSS53	VSS54	184A			
85 17	MEM_B_DM<5>	185A	DM7	DQS7*	186A	MEM_B_DQS_N<5>	17 85
	187A	VSS55	DQS7	188A	MEM_B_DQS_P<5>	17 85	
85 17	MEM_B_DQ<42>	189A	DQ58	VSS56	190A		
85 17	MEM_B_DQ<45>	191A	DQ59	DQ62	192A	MEM_B_DQ<41>	17 85
PP3V3_S0	193A	VSS57	DQ63	194A	MEM_B_DQ<44>	17 85	
86 48 34 31 29 25	SMBUS_SB_SDA	195A	SDA	VSS58	196A	Resistor prevents pwr-gnd short	
86 48 34 31 29 25	SMBUS_SB_SCL	197A	SCL	SA0	198A		
	199A	VDDSPD	SA1	200A	SODIMM_B_SA1		

202 204 516S0471 203 201

ADDR=0xA4(WR)/0xA5(RD)

PP3V3_S0

R3200 10K 5% 1/16W MF-LF 402

Resistor prevents pwr-gnd short

PP1V8_S3

C3208 10UF 20% 6.3V X5R 603

C3209 10UF 20% 6.3V X5R 603

C3210 1UF 10% 6.3V CERM 402

C3211 0.1UF 20% 10V CERM 402

C3212 1UF 10% 6.3V CERM 402

C3213 1UF 10% 6.3V CERM 402

C3214 1UF 10% 6.3V CERM 402

C3215 1UF 10% 6.3V CERM 402

C3216 1UF 10% 6.3V CERM 402

C3217 0.1UF 20% 10V CERM 402

C3218 0.1UF 20% 10V CERM 402

C3219 0.1UF 20% 10V CERM 402

C3220 0.1UF 20% 10V CERM 402

C3221 0.1UF 20% 10V CERM 402

DDR2 Bypass Caps

(For return current)

DDR2 SO-DIMM Connector B

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

APPLE INC.

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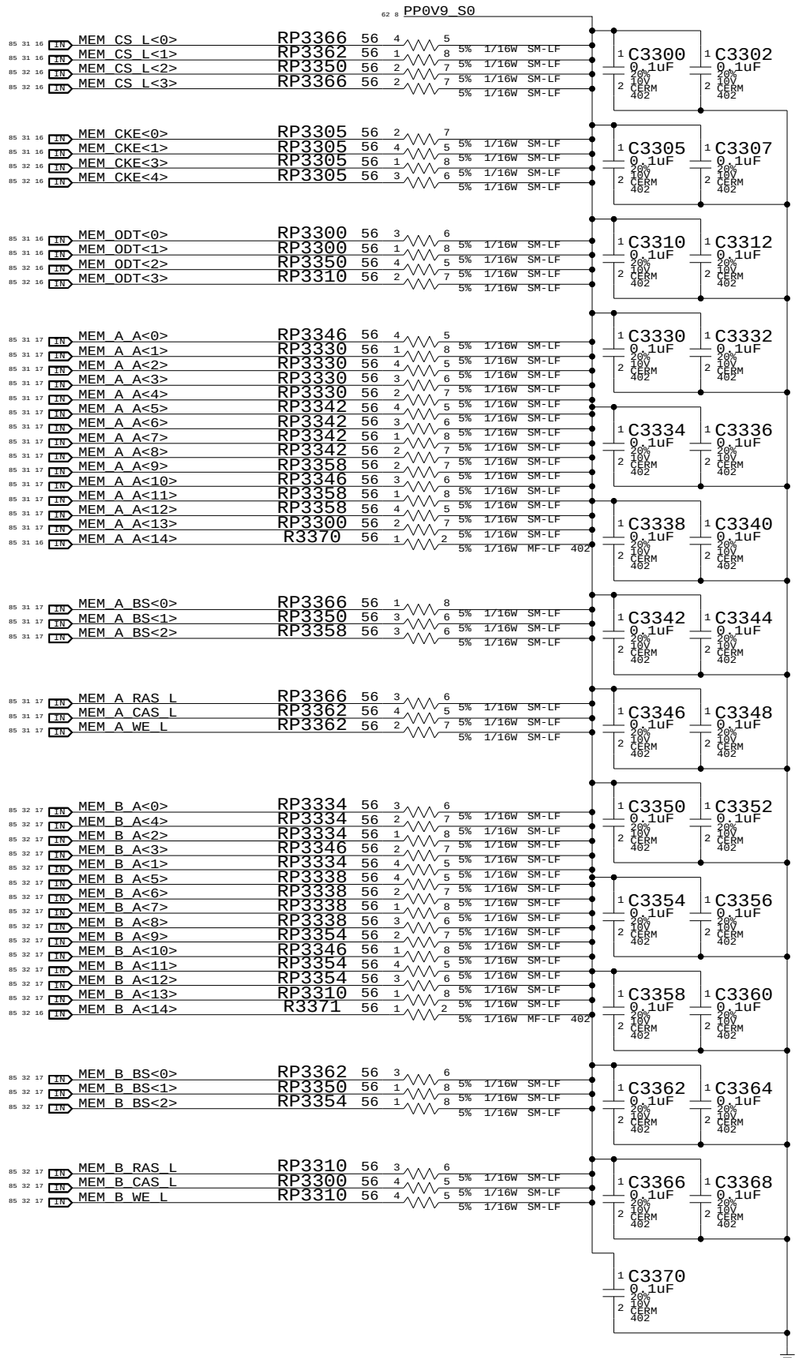
One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

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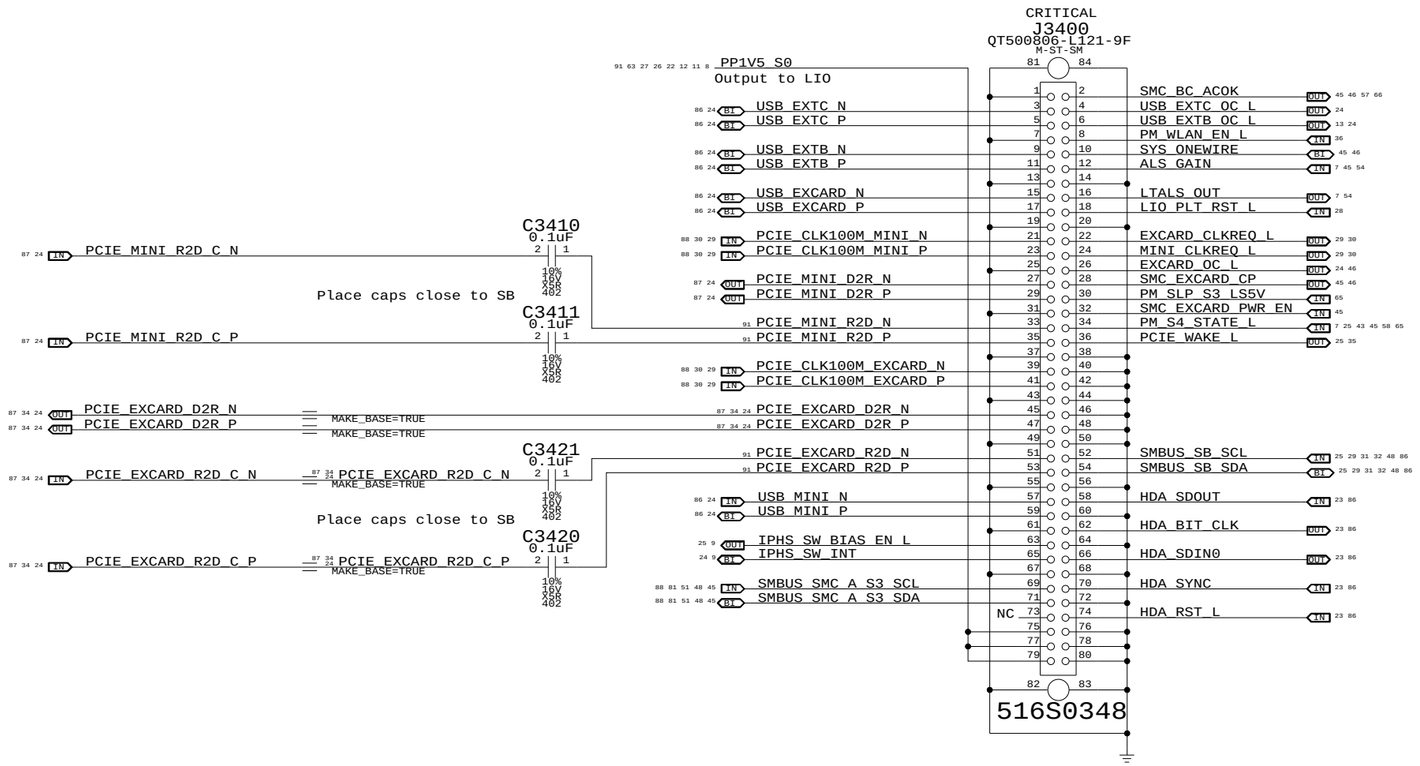
Left I/O Board Connector



Left I/O Board Connector		
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)	

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
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Page Notes

Power aliases required by this page:
- =PP3V3_ENET_PHY (EC / Ultra)
- =PP1V8R2V5_ENET_PHY (2.5V / 1.8V)
- =YUKON_EC_PP2V5_ENET (2.5V / GND)
- =PP1V2_ENET_PHY

Signal aliases required by this page:
- =ENET_CLKREQ_L (NC/TP for Yukon EC)
- =ENET_VMAIN_AVLBL (See note by pin)

BOM options provided by this page:
YUKON_EC - Selects Yukon EC RSET value.
YUKON_ULTRA - Selects Yukon Ultra RSET.

NOTE: See bottom of page for instructions for dual Yukon EC / Yukon Ultra schematic support.

PP1V25_ENET

Yukon EC		Yukon Ultra	
No link:	171 mA	No link:	130 mA
10 Mbps:	179 mA	10 Mbps:	130 mA
100 Mbps:	203 mA	100 Mbps:	150 mA
1000 Mbps:	426 mA	1000 Mbps:	290 mA

C3700 4.7UF 20% 6.3V CERM 603; C3701 0.1UF 10% 16V X5R 402; C3702 0.1UF 10% 16V X5R 402; C3703 0.1UF 10% 16V X5R 402; C3704 0.1UF 10% 16V X5R 402; C3705 0.1UF 10% 16V X5R 402; C3706 0.001UF 10% 50V CERM 402; C3707 0.001UF 10% 50V CERM 402; C3708 0.001UF 10% 50V CERM 402

PP3V3_ENET

Yukon EC		Yukon Ultra	
No link:	4 mA	No link:	60 mA
10 Mbps:	4 mA	10 Mbps:	70 mA
100 Mbps:	4 mA	100 Mbps:	70 mA
1000 Mbps:	4 mA	1000 Mbps:	80 mA

C3710 4.7UF 20% 6.3V CERM 603; C3711 0.1UF 10% 16V X5R 402; C3712 0.1UF 10% 16V X5R 402; C3713 0.1UF 10% 16V X5R 402; C3714 0.001UF 10% 50V CERM 402; C3715 0.001UF 10% 50V CERM 402

PP1V9_ENET — L3720 FERR-120-OHM-1.5A 0402 — PP1V8R2V5_ENET_PHY_AVDD
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

Yukon EC (2.5V)		Yukon Ultra (1.8V)	
No link:	82 mA	No link:	0 mA
10 Mbps:	108 mA	10 Mbps:	30 mA
100 Mbps:	126 mA	100 Mbps:	40 mA
1000 Mbps:	218 mA	1000 Mbps:	150 mA

(EC:2.5V)

C3720 4.7UF 20% 6.3V CERM 603; C3721 0.1UF 10% 16V X5R 402; C3722 0.1UF 10% 16V X5R 402; C3723 0.1UF 10% 16V X5R 402; C3724 0.001UF 10% 50V CERM 402

GND

Yukon EC: Alias to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF & 1x 0.001uF caps
Yukon Ultra: Alias to GND

PCIE_ENET_D2R_P — C3735 0.1uF 10% 16V X5R 402 — PCIE_ENET_D2R_C_P
PCIE_ENET_D2R_N — C3736 0.1uF 10% 16V X5R 402 — PCIE_ENET_D2R_C_N
PLACEMENT_NOTE=Place C3730 close to southbridge.
PCIE_ENET_R2D_C_P — C3730 0.1uF 10% 16V X5R 402 — PCIE_ENET_R2D_P
PCIE_ENET_R2D_C_N — C3731 0.1uF 10% 16V X5R 402 — PCIE_ENET_R2D_N
PLACEMENT_NOTE=Place C3731 close to southbridge.

PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N
Yukon EC: Pin 42 should be NC (or TP) net.
ENET_CLKREQ_L
PCIE_WAKE_L
ENET_RESET_L

ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<2>
ENET_MDI_N<2>
ENET_MDI_P<3>
ENET_MDI_N<3>

SIGNAL_MODEL=EMPTY
R3740 R3741 49.9 1% 1/16W MF-LF 402
R3742 R3743 49.9 1% 1/16W MF-LF 402
R3744 R3745 49.9 1% 1/16W MF-LF 402
R3746 R3747 49.9 1% 1/16W MF-LF 402

ENET_MDI0 — C3740 0.001UF 10% 50V CERM 402
ENET_MDI1 — C3742 0.001UF 10% 50V CERM 402
ENET_MDI2 — C3744 0.001UF 10% 50V CERM 402
ENET_MDI3 — C3746 0.001UF 10% 50V CERM 402

ENET_CLK25M_XTALI
ENET_CLK25M_XTALO

U3700 88E8058 QFN — CRITICAL, BOMOPTION=OMIT

PCIE_ENET_D2R_C_P	49	TX_P	
PCIE_ENET_D2R_C_N	50	TX_N	
PCIE_ENET_R2D_P	54	RX_P	
PCIE_ENET_R2D_N	53	RX_N	
PCI EXPRESS			
PCIE_CLK100M_ENET_P	55	REFCLKP	
PCIE_CLK100M_ENET_N	56	REFCLKN	
ENET_CLKREQ_L	42	CLKREQ*	EC:NO CONNECT
PCIE_WAKE_L	6	WAKE*	
ENET_RESET_L	5	PERST*	
ENET_MDI_P<0>	17	MDIP0	
ENET_MDI_N<0>	18	MDIN0	
ENET_MDI_P<1>	20	MDIP1	
ENET_MDI_N<1>	21	MDIN1	
ENET_MDI_P<2>	26	MDIP2	
ENET_MDI_N<2>	27	MDIN2	
ENET_MDI_P<3>	30	MDIP3	
ENET_MDI_N<3>	31	MDIN3	
ENET_CLK25M_XTALI	15	XTALI	
ENET_CLK25M_XTALO	14	XTALO	
MAIN CLK			
THRML_PAD	65		
ANALOG			
EC:CTRL25	CTRL18	4	TP_YUKON_CTRL18
	CTRL12	3	TP_YUKON_CTRL12
	RSET	16	YUKON_RSET
LED	LED_ACT*	59	NC
	LED_LINK10/100*	60	NC
	LED_LINK1000*	62	NC
	LED_DUPLEX*	63	NC
SPI	(IPU) SPI_DO	34	NC
	(IPU) SPI_DI	35	NC
	(IPU) SPI_CLK	37	NC
	(IPU) SPI_CS	36	NC
MEDIA			
TWSI	(IPU) VPD_CLK	38	YUKON_VPD_CLK
	(IPU) VPD_DATA	41	YUKON_VPD_DATA
	(IPD) TESTMODE	46	
TEST/RSVD	RSVD_24	24	NC
	RSVD_25	25	NC
	RSVD_29	29	NC
	RSVD_43	43	NC
	VMAIN_AVLBL	47	PM_SLP_S3_L
	SWITCH_VCC	11	NC
	LOM_DISABLE*	10	ENET_LOM_DIS_L
	VAUX_AVLBL	12	
	SWITCH_VAUX	9	NC

EC:AVDD 2.5V

R3760 4.7K 5% 1/10W MF-LF 402 — ENET_LOM_DIS_L

Must be high in S0 state (can use PP3V3_S0 as input)
PM_SLP_S3_L — IN 7 25 36 40 45 49 58 62 65

TP_YUKON_CTRL18 — OUT
TP_YUKON_CTRL12 — OUT

YUKON_ULTRA
R3765 4.99K 1% 1/10W MF-LF 402

VPD ROM
C3780 0.1UF 10% 16V X5R 402
U3780 M24C08 SO8 — CRITICAL
R3780 4.7K 5% 1/10W MF-LF 402
R3781 4.7K 5% 1/10W MF-LF 402
VCC, E2, NC1, NC0, WC*, SDA, SCL, VSS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0386	1	IC,88E8058,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	YUKON_ULTRA
341S2060	1	IC,FLASH,88E8058 ETHERNET VPD,IIC,SO8	U3780	CRITICAL	YUKON_ULTRA
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	YUKON_EC
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U3780	CRITICAL	YUKON_EC
114S0285	1	RES,4.87K,1%,1/16W,0402,LF	R3760		YUKON_EC

To support Yukon EC and Ultra on the same board:

- Alias =YUKON_EC_PP2V5_ENET to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF and 1x 0.001uF caps
- Use 0-ohm resistors or variable supply to provide 1.8V or 2.5V to =PP1V8R2V5_ENET_PHY and magnetics. Can also use BCP69T1 connected to CTRL18 pin 4 for internal VR.
- Connect =ENET_CLKREQ_L to clock generator via 0-ohm resistor (BOMOPTION: YUKON_ULTRA)
- Use YUKON_EC and YUKON_ULTRA BOMOPTIONs to select stuffed part

Ethernet (Yukon)

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

APPLE INC.

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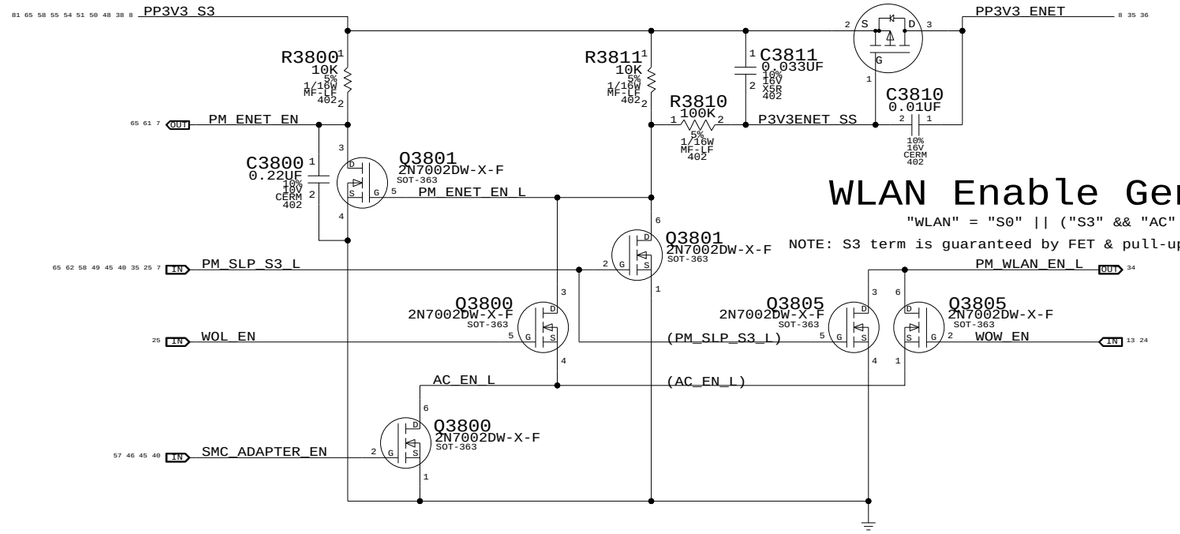
ENET Enable Generation

"ENET" = "S0" || ("S3" && "AC" && "WOL_EN")

NOTE: S3 term is guaranteed by source of R3800 & Q3810, MUST BE S3 RAIL.

3.3V ENET FET



WLAN Enable Generation

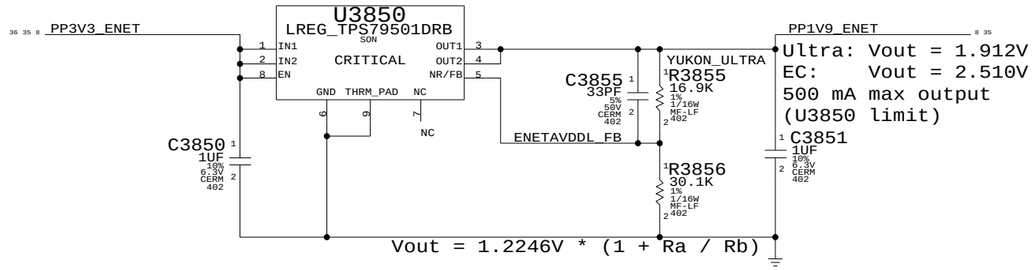
"WLAN" = "S0" || ("S3" && "AC" && "WOW_EN")

NOTE: S3 term is guaranteed by FET & pull-up source, MUST BE S3 RAIL.

Yukon AVDDL LDO

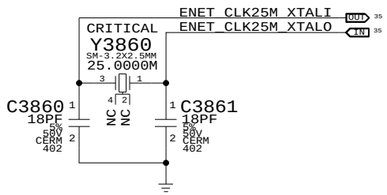
1.9V for Yukon Ultra, 2.5V for Yukon EC

Yukon Ultra requires 1.9V on its magnetics to pass compliance tests



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0363	1	RES,31.6K,1%,1/16W,402,LF	R3855		YUKON_EC

Yukon Crystal



Yukon Power Control

SYNC_MASTER=T9_NOME SYNC_DATE=03/19/2007

APPLE INC.

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D	051-7431	A.0.0
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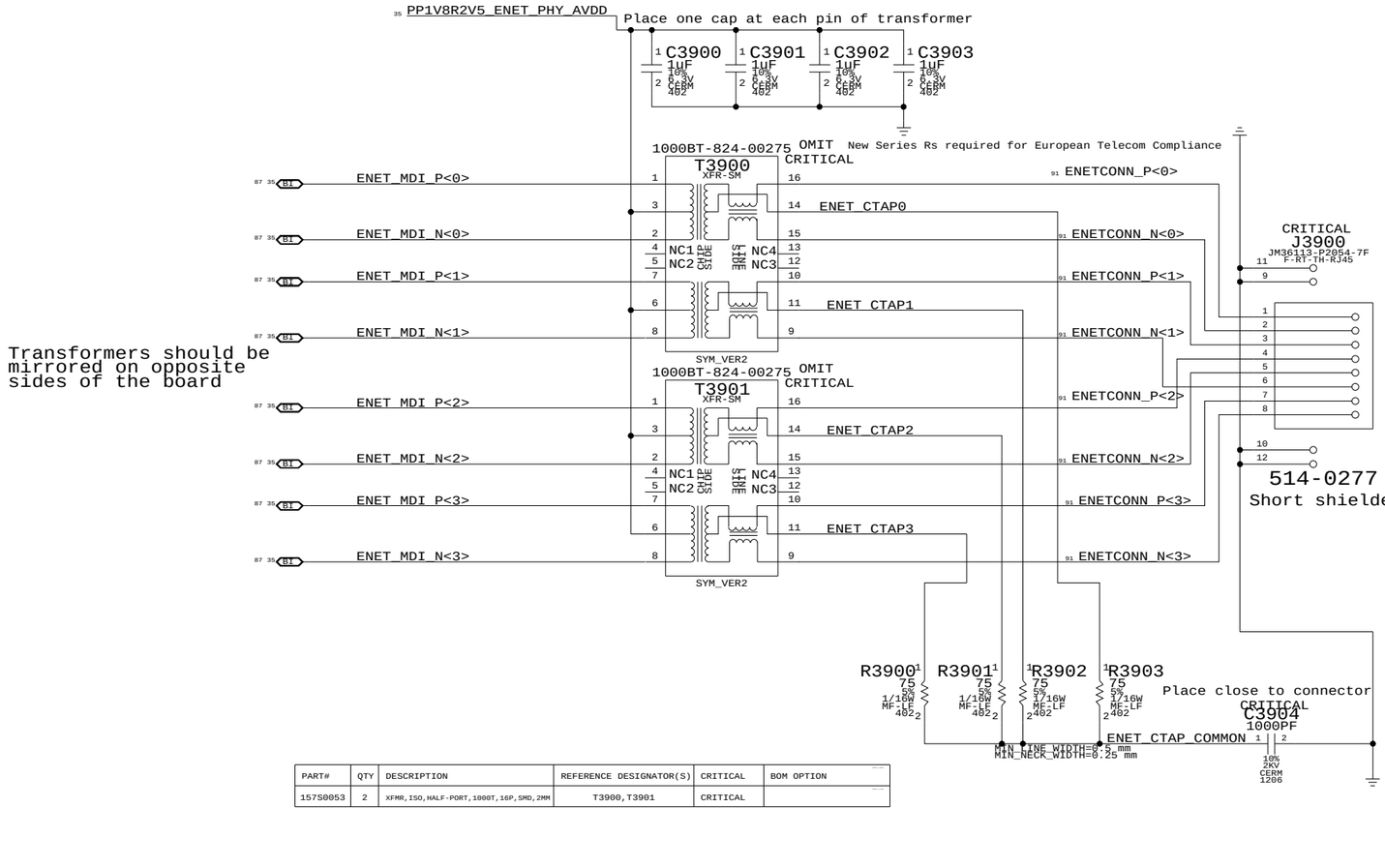
Page Notes

Power aliases required by this page:
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Transformers should be mirrored on opposite sides of the board

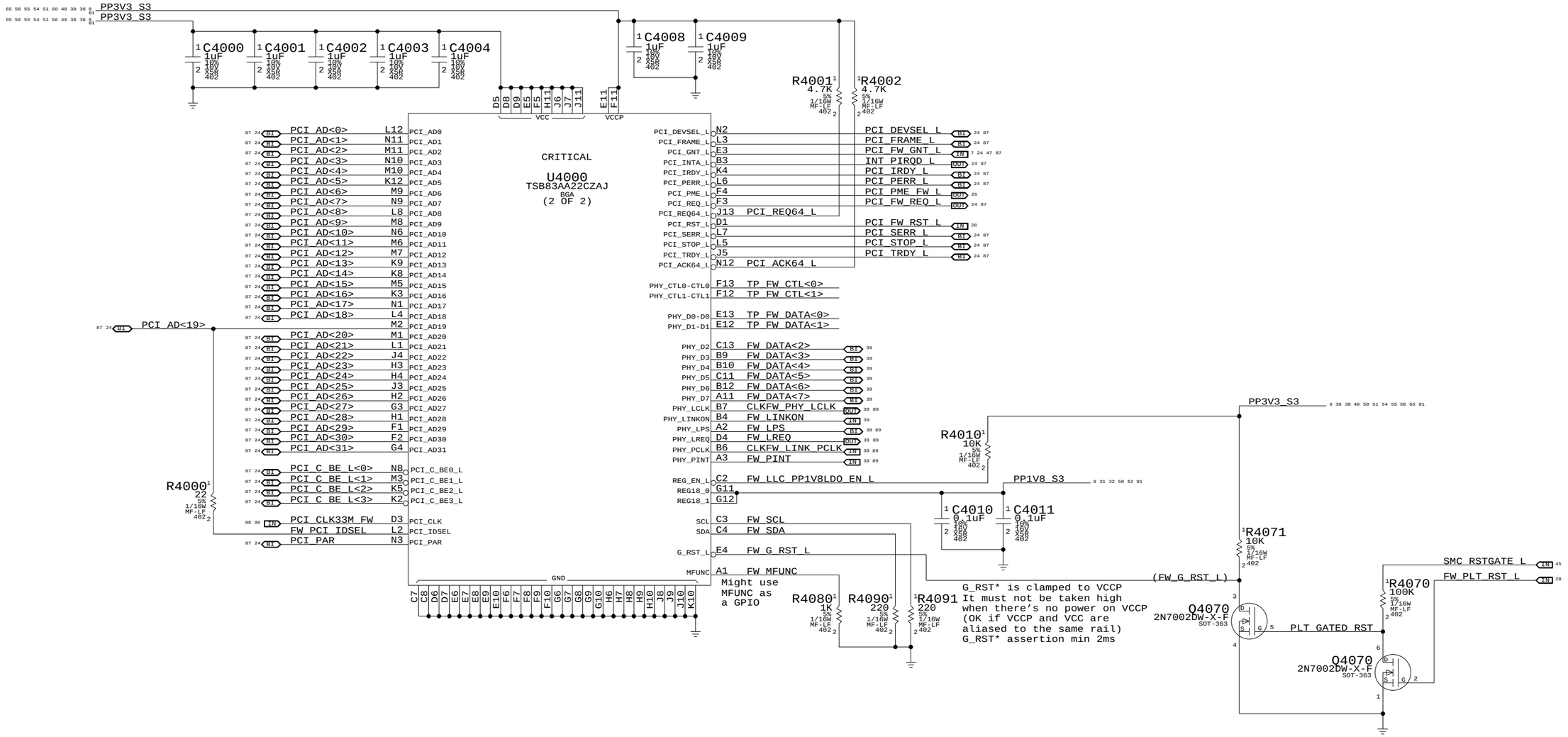
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
157S0053	2	XFMR,ISO,HALF-PORT,1000T,16P,SMD,2MM	T3900,T3901	CRITICAL	

Ethernet Connector

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 37 OF 92	



FireWire Link (TSB83AA22)

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
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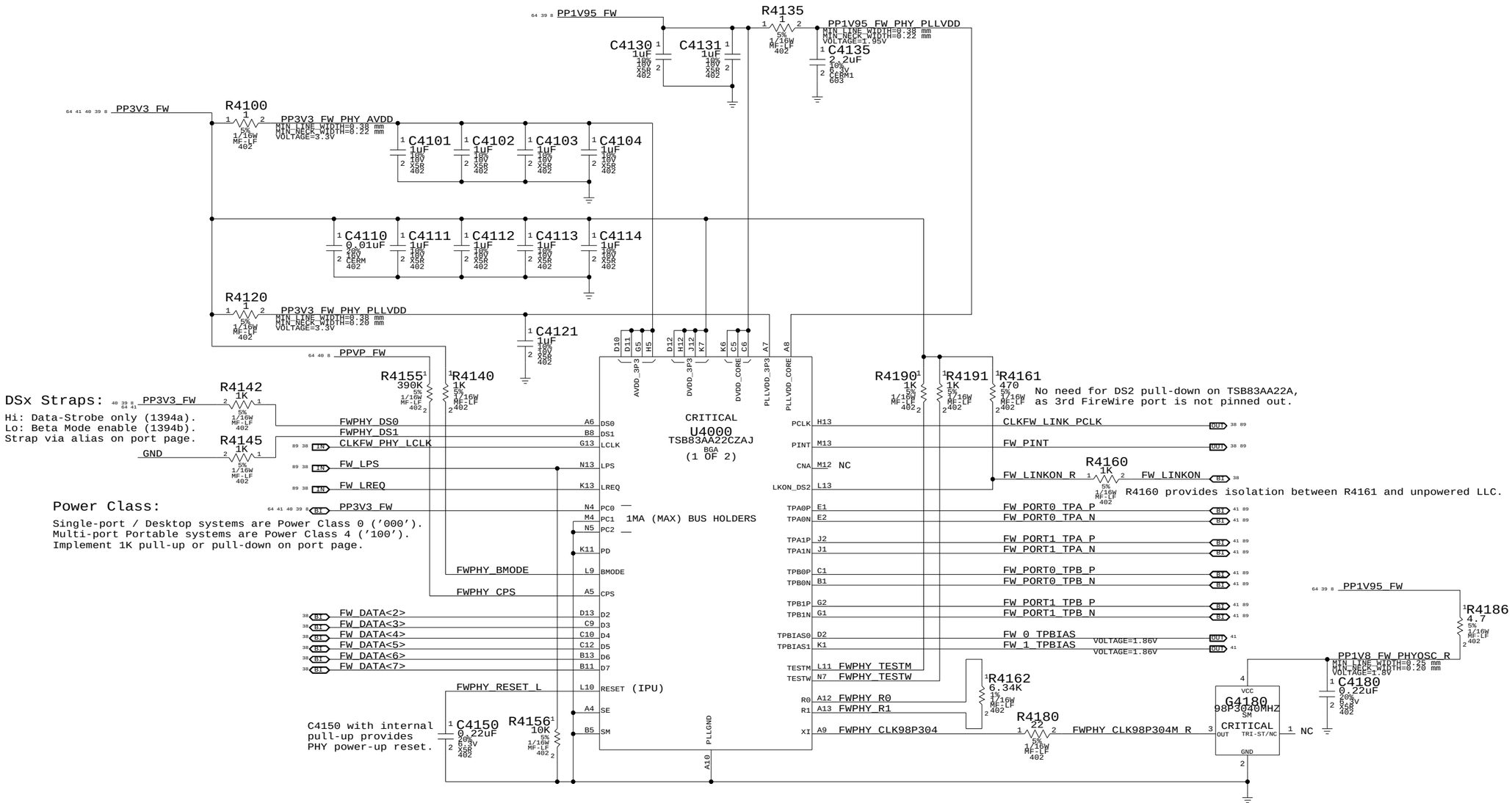

FireWire PHY (TSB83AA22)			
SYNC_MASTER=M87_MLB	SYNC_DATE=08/28/2007		
NOTICE OF PROPRIETARY PROPERTY			
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APPLE INC.	SIZE: D	DRAWING NUMBER: 051-7431	REV: A.0.0
	SCALE: NONE	SHT: 39	OF: 92

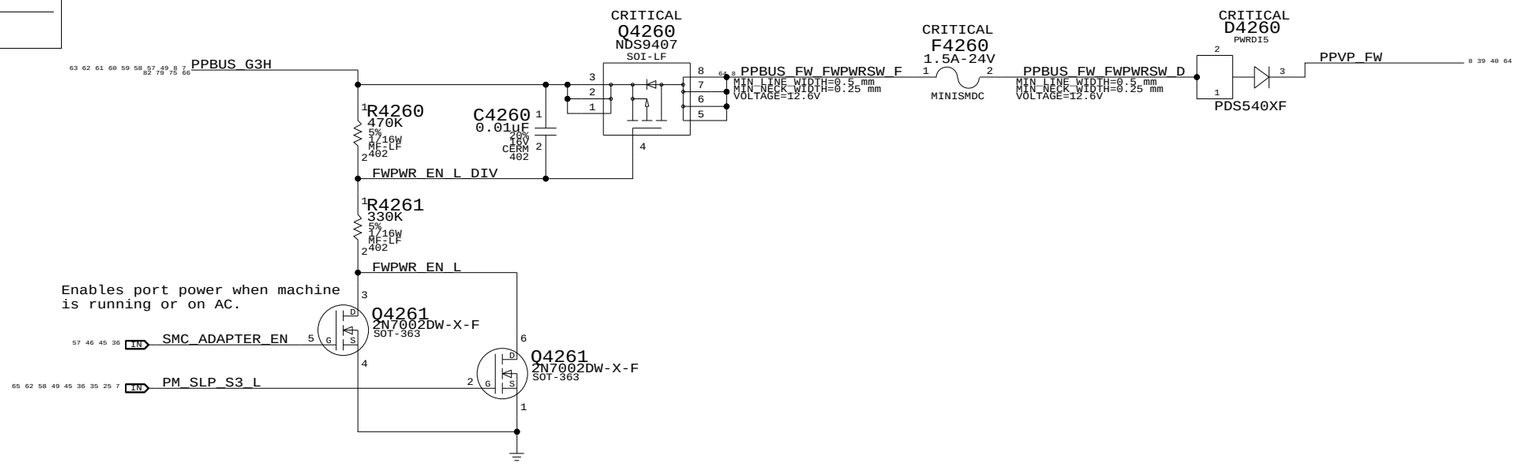
Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

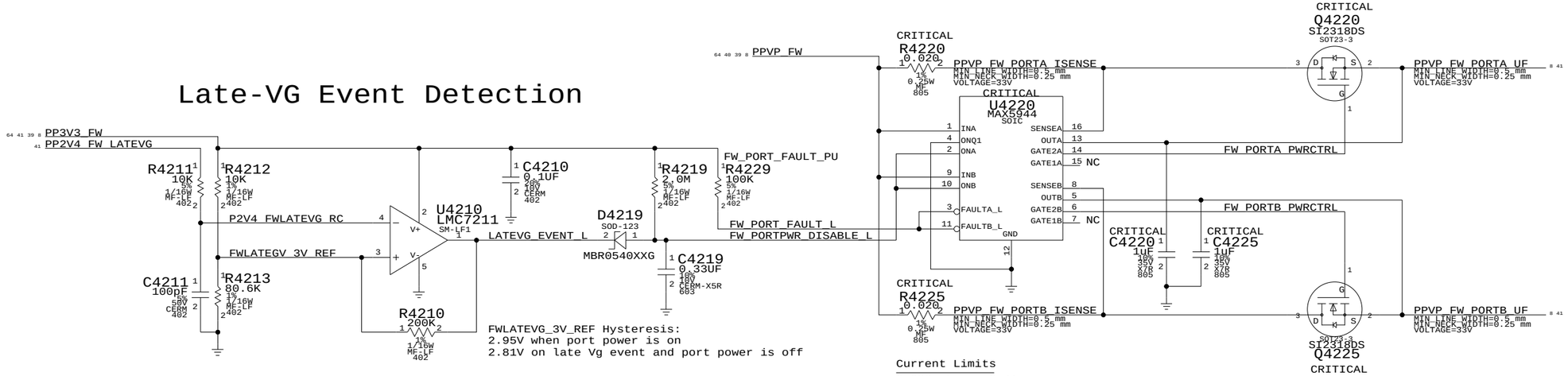
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- FW_PORT_FAULT_PU

FireWire Port Power Switch



Current Limit/Active Late-VG Protection



Current Limits

0.020 ohm => 2.4A
0.025 ohm => 2A
0.030 ohm => 1.66A (Ideal)
0.033 ohm => 1.5A

MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

Late-VG Event Detection

FireWire Port Power

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
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Page Notes

Power aliases required by this page:
- =PPVP_FW_PORT0
- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG
- =GND_CHASSIS_FW_PORT0L
- =GND_CHASSIS_FW_PORT0U
- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

Configures PHY for:
- 2-port Portable Power Class (4)
- Port "0" Data-Strobe only (1394A)
- Port "1" Bilingual (1394B)

64 41 40 39 8 PP3V3_FW
41 40 39 8 PP3V3_FW
40 39 8 PP3V3_FW
GND

Termination

Place close to FireWire PHY

TI PHYs require 1uF even though FW spec calls out 0.33uF

39 FW_1_TPBIAS
39 FW_0_TPBIAS
C4350 1uF 10% 6.3V CERM 402
C4360 1uF 10% 6.3V CERM 402
CRITICAL L4360 18NH-250MA 0402
CRITICAL L4361 18NH-250MA 0402
FW_B_TPA_L_P
FW_B_TPA_L_N
R4350 56.2 1% 1/16W MF-LF 402
R4351 56.2 1% 1/16W MF-LF 402
R4360 56.2 1% 1/16W MF-LF 402
R4361 56.2 1% 1/16W MF-LF 402

89 41 39 FW_PORT0_TPA_P — MAKE_BASE=TRUE — 39 41 89 FW_PORT0_TPA_P
89 41 39 FW_PORT0_TPA_N — MAKE_BASE=TRUE — 39 41 89 FW_PORT0_TPA_N
89 41 39 FW_PORT0_TPB_P — MAKE_BASE=TRUE — 39 41 89 FW_PORT0_TPB_P
89 41 39 FW_PORT0_TPB_N — MAKE_BASE=TRUE — 39 41 89 FW_PORT0_TPB_N
89 41 39 FW_PORT1_TPA_P — MAKE_BASE=TRUE — 39 41 89 FW_PORT1_TPA_P
89 41 39 FW_PORT1_TPA_N — MAKE_BASE=TRUE — 39 41 89 FW_PORT1_TPA_N
89 41 39 FW_PORT1_TPB_P — MAKE_BASE=TRUE — 39 41 89 FW_PORT1_TPB_P
89 41 39 FW_PORT1_TPB_N — MAKE_BASE=TRUE — 39 41 89 FW_PORT1_TPB_N

SIGNAL_MODEL=EMPTY
R4352 56.2 1% 1/16W MF-LF 402
R4353 56.2 1% 1/16W MF-LF 402
R4362 56.2 1% 1/16W MF-LF 402
R4363 56.2 1% 1/16W MF-LF 402
FW_B_TPB_L_N
FW_B_TPB_L_P
CRITICAL L4362 18NH-250MA 0402 SIGNAL_MODEL=EMPTY
CRITICAL L4363 18NH-250MA 0402 SIGNAL_MODEL=EMPTY
FW_PORT0_TPB_C
FW_PORT1_TPB_C
C4354 220pF 5% 25V CERM 402
R4354 4.99K 1% 1/16W MF-LF 402
C4364 220pF 5% 25V CERM 402
R4364 4.99K 1% 1/16W MF-LF 402

Late-VG Protection Power

64 41 40 39 8 PP3V3_FW
R4390 332 1% 1/16W MF-LF 402
PP2V4_FW_LATEVG MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=2.4V 40 41
CRITICAL D4390 MMBZ5227B SOT23

ESD and late-VG rail for snap-back diodes (Common to all ports)

PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin
R4390 should be 390 Ohms max for a 3.3V rail

Cable Power

"Snapback" & "Late VG" Protection

CRITICAL L4300 FERR-250-OHM SM — Note: Trace PPVP_FW_PORT0 must handle up to 5A
40 8 PPVP_FW_PORTA_UF
PPVP_FW_PORT0 MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=33V
C4304 0.01UF 10% 50V X7R 402
41 40 PP2V4_FW_LATEVG
DP4300 BAV99DW-X-F SOT-363
C4300 0.01uF 10% 50V X7R 402
C4301 0.01uF 10% 50V X7R 402
89 41 39 FW_PORT0_TPA_P
89 41 39 FW_PORT0_TPA_N
89 41 39 FW_PORT0_TPB_P
89 41 39 FW_PORT0_TPB_N
CRITICAL FL4300 90-OHM-100MA 1210-4SM1
CRITICAL FL4301 90-OHM-100MA 1210-4SM1
91 FW_PORT0_TPA_FL_P
91 FW_PORT0_TPA_FL_N
91 FW_PORT0_TPB_FL_P
91 FW_PORT0_TPB_FL_N
(GND_FW_PORT0_VG)
DP4301 BAV99DW-X-F SOT-363
C4302 0.01uF 10% 50V X7R 402
C4303 0.01uF 10% 50V X7R 402

PORT 0
1394A
CRITICAL J4300 1394A F-RT-TH-LF
6 TPO (TPA+)
5 TPO# (TPA-)
4 TPI (TPB+)
3 TPI# (TPB-)
1 VP
2 VGND
7 8 9 10
514-0255

Cable Power

"Snapback" & "Late VG" Protection

CRITICAL L4310 FERR-250-OHM SM — Note: Trace PPVP_FW_PORT1 must handle up to 5A
40 8 PPVP_FW_PORTB_UF
PPVP_FW_PORT1 MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=33V
C4314 0.01UF 10% 50V X7R 402
41 40 PP2V4_FW_LATEVG
DP4310 BAV99DW-X-F SOT-363
C4311 0.01uF 10% 50V X7R 402
C4310 0.01uF 10% 50V X7R 402
89 41 39 FW_PORT1_TPB_N
89 41 39 FW_PORT1_TPB_P
89 41 39 FW_PORT1_TPA_N
89 41 39 FW_PORT1_TPA_P
DP4311 BAV99DW-X-F SOT-363
C4312 0.01uF 10% 50V X7R 402
C4313 0.01uF 10% 50V X7R 402
C4319 0.1uF 10% 50V X7R 603-1
R4319 1M 5% 1/16W MF-LF 402

PORT 1
BILINGUAL
CRITICAL J4310 1394B-UG31903 F-RT-SM1
10
1 TPB- / 9 TPB<R> / 2 TPB+ / 8 VP — OUTPUT
NC 7 NC
6 VG / 3 TPA- / 5 TPA<R> / 4 TPA+ — INPUT
11
514S0133

(FW_PORT1_BREF)
(GND_FW_PORT1_VG)
FW_PORT1_AREF

PLACEMENT_NOTE=Place C4319 close to connector pin 5.

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

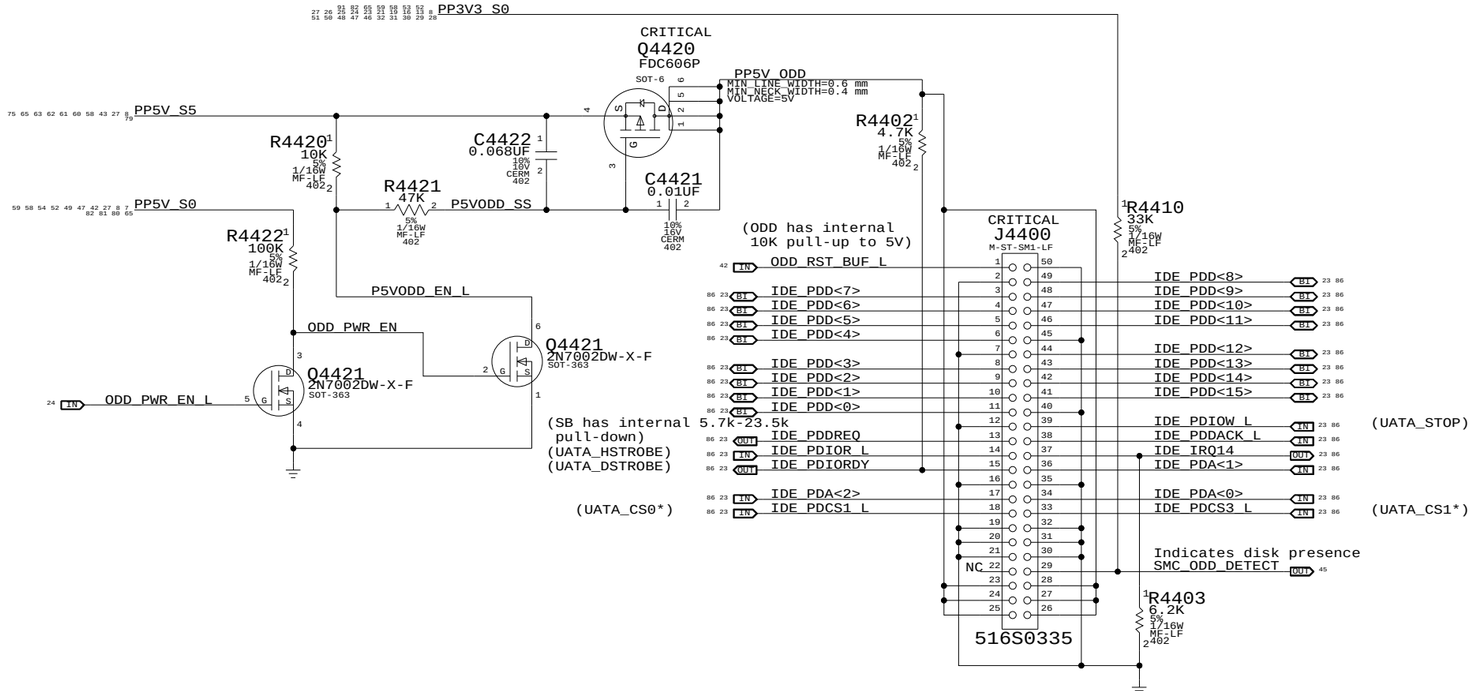
FireWire Ports

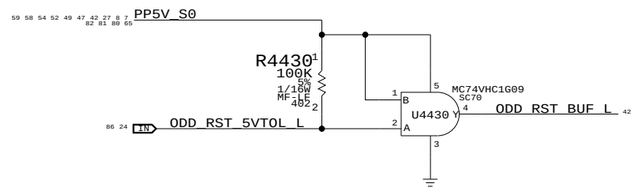
SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

APPLE INC.

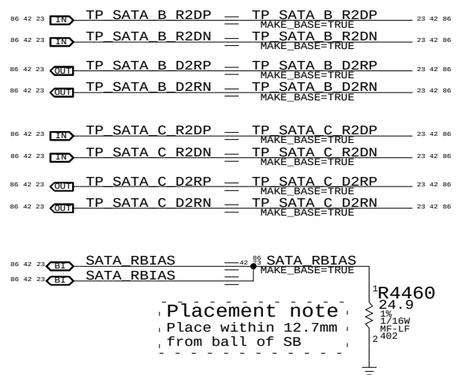
SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 41 OF 92	

IDE (ODD) Connector





Unused SATA Ports



PATA Connector

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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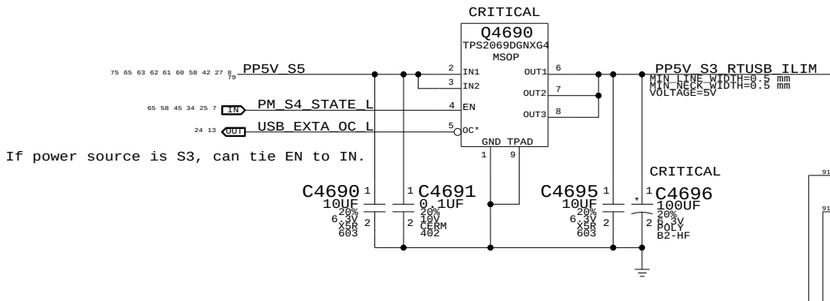
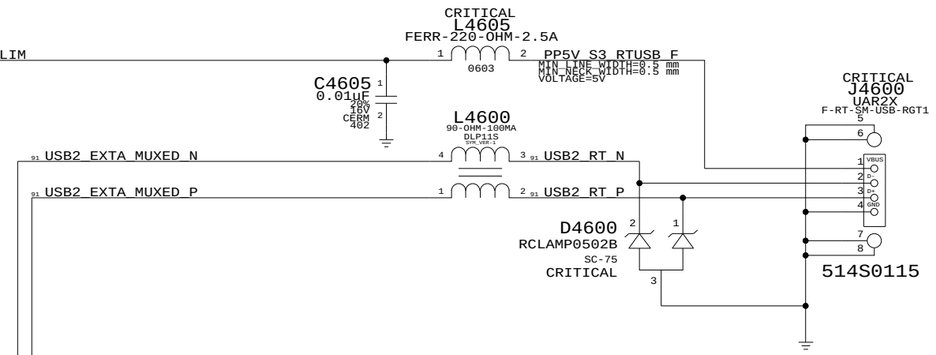
SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 42 OF 92	

Port Power Switch



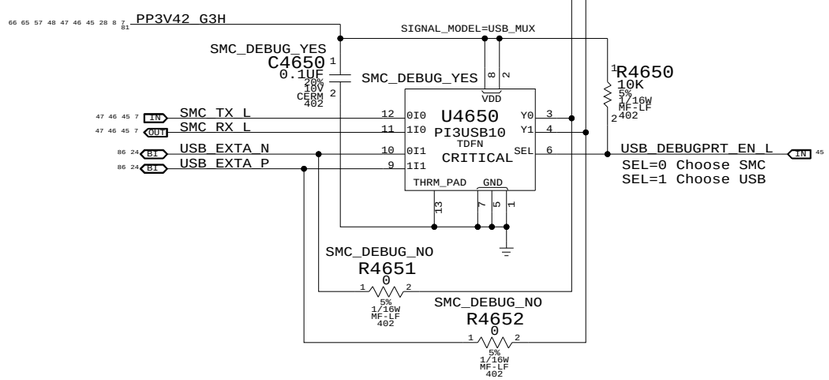
If power source is S3, can tie EN to IN.

Right USB Port



Place L4600 and L4605 at connector pin

USB/SMC Debug Mux



External USB Connector

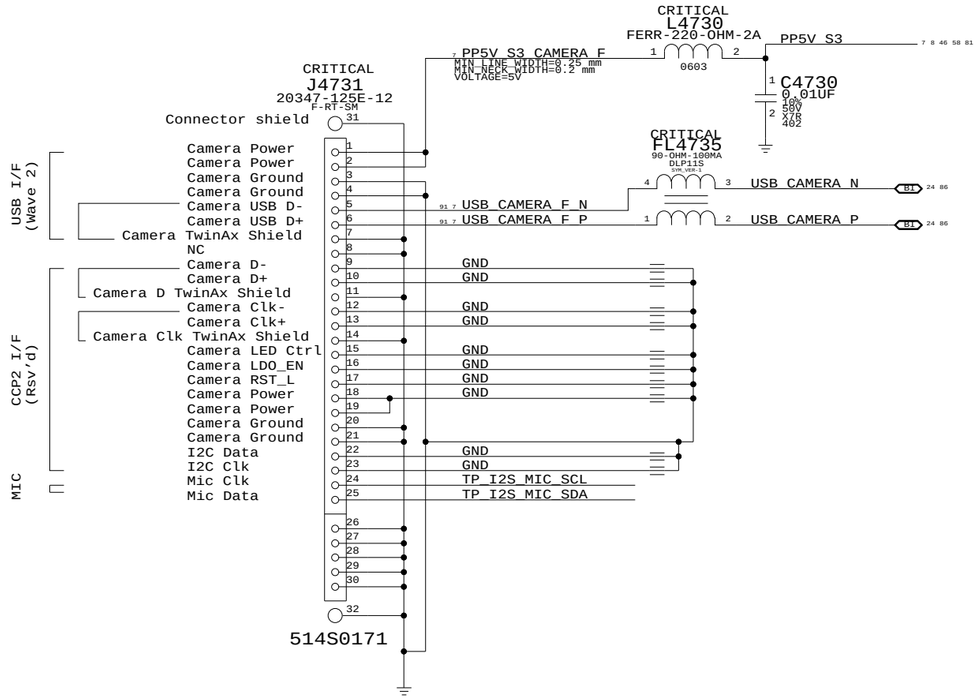
SYNC_MASTER=MASTER SYNC_DATE=MASTER

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0

SCALE	SHT	OF
NONE	43	92

Left Clutch Barrel Interconnect



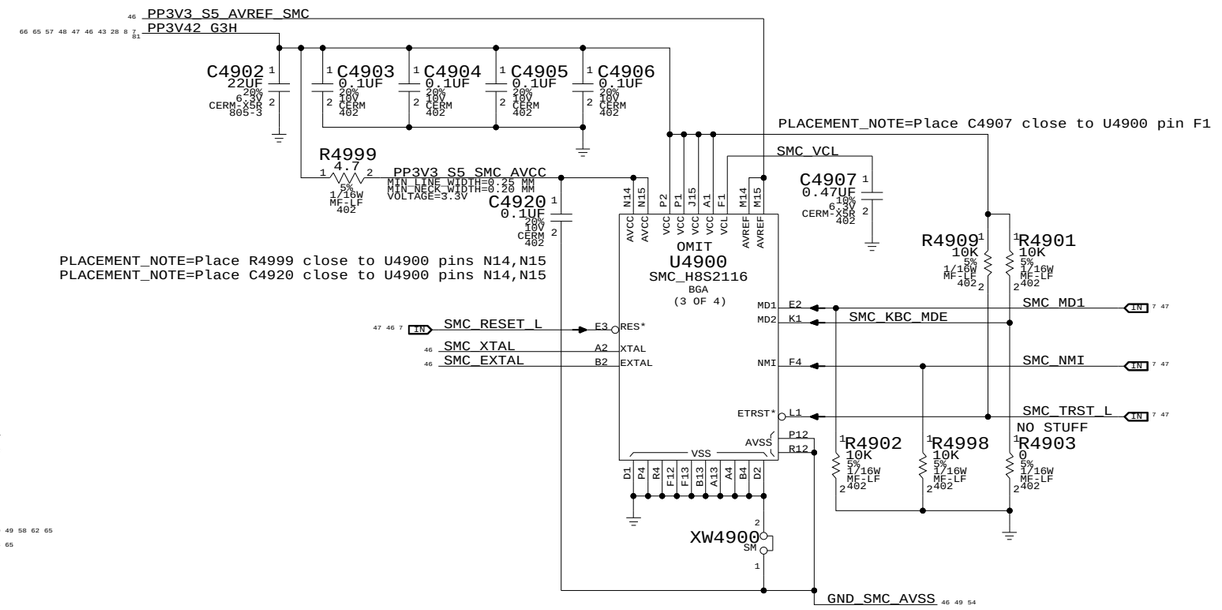
Left Clutch Barrel Interconnect

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

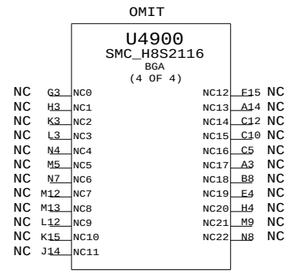
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 44 OF 92	

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.



SMC

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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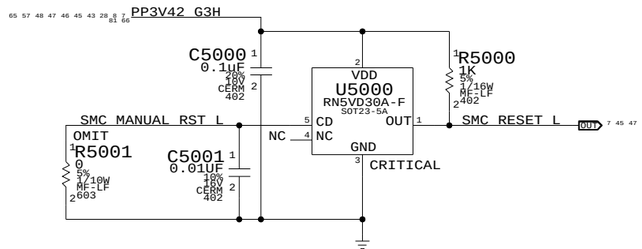
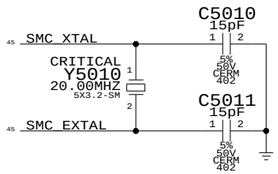
SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0

SCALE: NONE SHT 45 OF 92

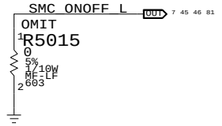
SMC Reset "Button" / Brownout Detect



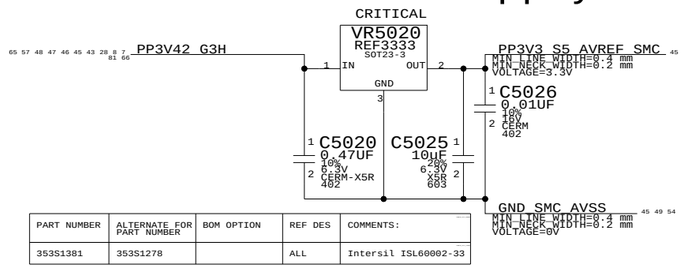
SMC Crystal Circuit



Debug Power "Button"

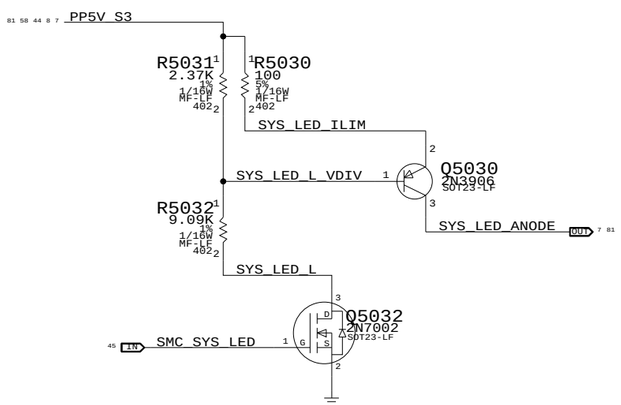


SMC AVREF Supply

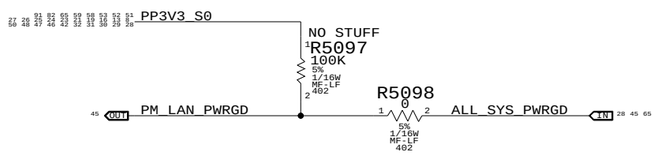


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1278		ALL	Intersil ISL60002-33

System (Sleep) LED Circuit

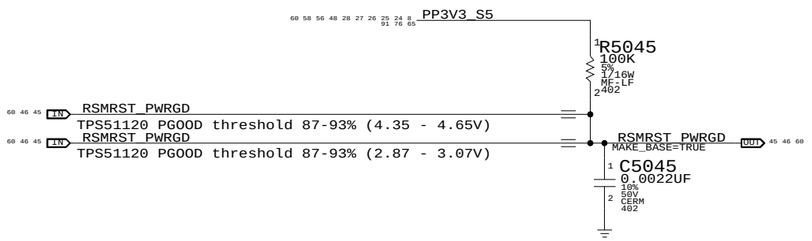


LAN PWRGD Circuit



S5 Rail PWRGD Circuit

Reports when 5V S5 and 3.3V S5 are in regulation



TP_SMC_FAN_2_CTL — TP_SMC_FAN_2_CTL (MAKE_BASE=TRUE)

TP_SMC_FAN_2_TACH — TP_SMC_FAN_2_TACH (MAKE_BASE=TRUE)

TP_SMC_FAN_3_CTL — TP_SMC_FAN_3_CTL (MAKE_BASE=TRUE)

TP_SMC_FAN_3_TACH — TP_SMC_FAN_3_TACH (MAKE_BASE=TRUE)

TP_SMC_GFX_OVERTEMP_L — TP_SMC_GFX_OVERTEMP_L (MAKE_BASE=TRUE)

TP_SMC_GFX_THROTTLE_L — TP_SMC_GFX_THROTTLE_L (MAKE_BASE=TRUE)

TP_SMC_BATT_VSET — TP_SMC_BATT_VSET (MAKE_BASE=TRUE)

TP_SMC_SYS_VSET — TP_SMC_SYS_VSET (MAKE_BASE=TRUE)

TP_SMC_P14 — TP_SMC_P14 (MAKE_BASE=TRUE)

TP_SMC_P20 — TP_SMC_P20 (MAKE_BASE=TRUE)

TP_SMC_P21 — TP_SMC_P21 (MAKE_BASE=TRUE)

TP_SMC_P22 — TP_SMC_P22 (MAKE_BASE=TRUE)

TP_SMC_P23 — TP_SMC_P23 (MAKE_BASE=TRUE)

TP_SMC_P26 — TP_SMC_P26 (MAKE_BASE=TRUE)

TP_SMC_P27 — TP_SMC_P27 (MAKE_BASE=TRUE)

TP_SMC_P43 — TP_SMC_P43 (MAKE_BASE=TRUE)

TP_SMC_P44 — TP_SMC_P44 (MAKE_BASE=TRUE)

TP_SMC_P46 — TP_SMC_P46 (MAKE_BASE=TRUE)

TP_SMC_P62 — TP_SMC_P62 (MAKE_BASE=TRUE)

TP_SMC_P63 — TP_SMC_P63 (MAKE_BASE=TRUE)

TP_SMC_P64 — TP_SMC_P64 (MAKE_BASE=TRUE)

TP_SMC_P81 — TP_SMC_P81 (MAKE_BASE=TRUE)

TP_SMC_PF0 — TP_SMC_PF0 (MAKE_BASE=TRUE)

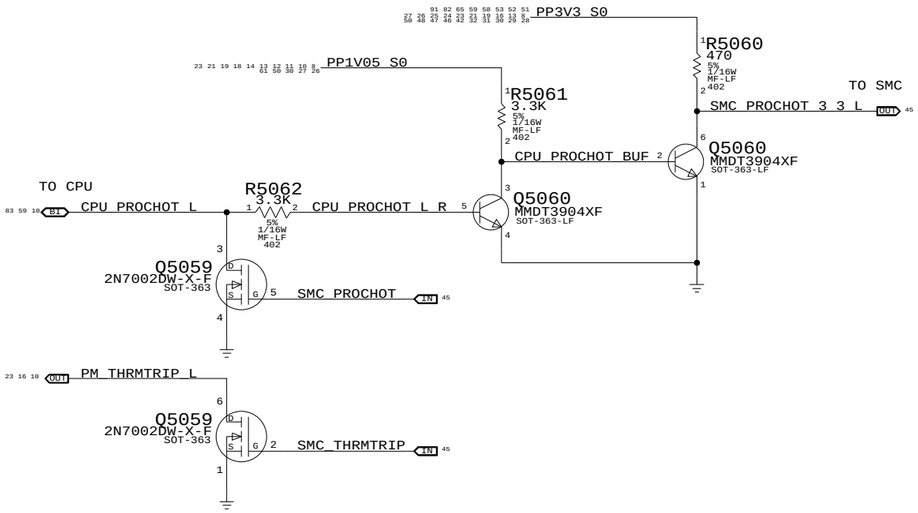
TP_SMC_PF1 — TP_SMC_PF1 (MAKE_BASE=TRUE)

SMC_EXCARD_OC_L — R5095 0 5% 1/10W MF-LF 402 — EXCARD_OC_L

SUS_CLK_SB — SUS_CLK_SB (MAKE_BASE=TRUE)

SMC_ENRGYSTR_LDO_EN — SMC_ENRGYSTR_LDO_EN (MAKE_BASE=TRUE) OUT

SMC FSB to 3.3V Level Shifting



PP3V42_G3H

SMC_PA0	R5091	100K	5% 1/16W MF-LF 402	
SMC_PA1	R5092	100K	5% 1/16W MF-LF 402	
SMC_PB0	R5093	100K	5% 1/16W MF-LF 402	
SMC_ONOFF_L	R5070	10K	5% 1/16W MF-LF 402	
SMC_LID	R5071	100K	5% 1/16W MF-LF 402	
SMC_FWE	R5072	10K	5% 1/16W MF-LF 402	
SMC_TX_L	R5073	10K	5% 1/16W MF-LF 402	
SMC_RX_L	R5074	100K	5% 1/16W MF-LF 402	
SYS_ONEWIRE	R5075	2.0K	ONEWIRE_PU 5% 1/16W MF-LF 402	
SMC_BS_ALRT_L	R5076	100K	5% 1/16W MF-LF 402	
SMC_TMS	R5077	10K	5% 1/16W MF-LF 402	
SMC_TDO	R5078	10K	5% 1/16W MF-LF 402	
SMC_TDI	R5079	10K	5% 1/16W MF-LF 402	
SMC_TCK	R5080	10K	5% 1/16W MF-LF 402	
SMC_P67	R5094	10K	5% 1/16W MF-LF 402	
SMC_PF3	R5081	10K	5% 1/16W MF-LF 402	
SMC_PG0	R5096	10K	5% 1/16W MF-LF 402	
SMC_PH4	R5082	10K	5% 1/16W MF-LF 402	
SMC_BATT_TRICKLE_EN_L	R5083	10K	5% 1/16W MF-LF 402	
SMC_BATT_CHG_EN	R5084	10K	5% 1/16W MF-LF 402	
SMC_ADAPTER_EN	R5085	10K	5% 1/16W MF-LF 402	
SMC_CASE_OPEN	R5086	10K	5% 1/16W MF-LF 402	
SMC_BC_ACOK	R5087	470K	5% 1/16W MF-LF 402	
SMC_EXCARD_CP	R5088	10K	5% 1/16W MF-LF 402	
PM_SUS_STAT_L	R5089	100K	5% 1/16W MF-LF 402	
PM_SLP_S5_L	R5090	100K	5% 1/16W MF-LF 402	

SMC Support

SYNC_MASTER=M87_MLB SYNC_DATE=10/15/2007

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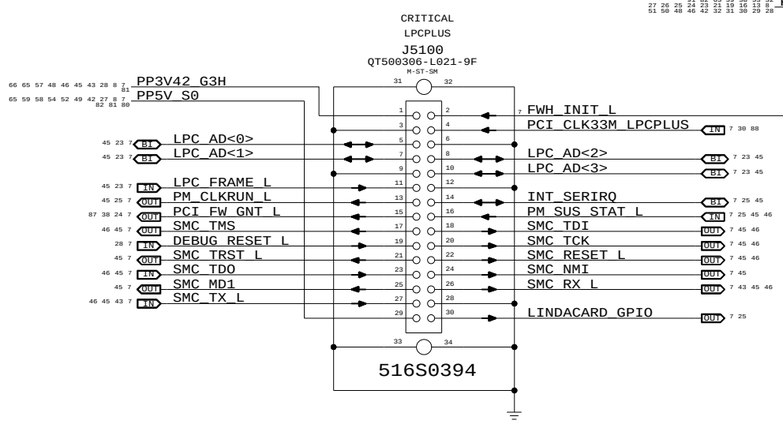
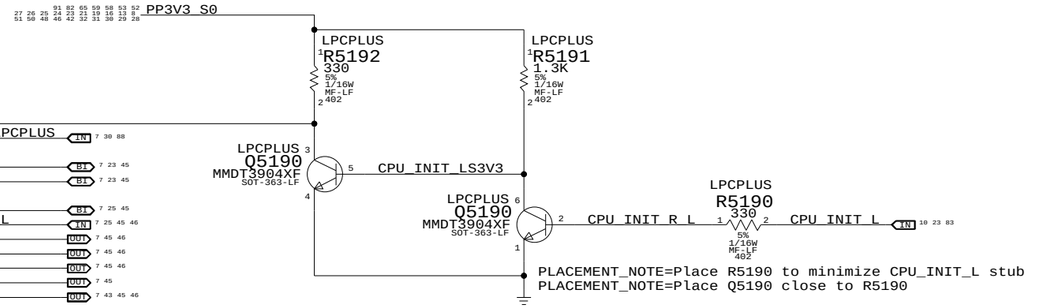
D	051-7431	A.0.0

SCALE: NONE SHT 46 OF 92

LPC+ Connector



FWH_INIT_L Generation



LPC+ Debug Connector

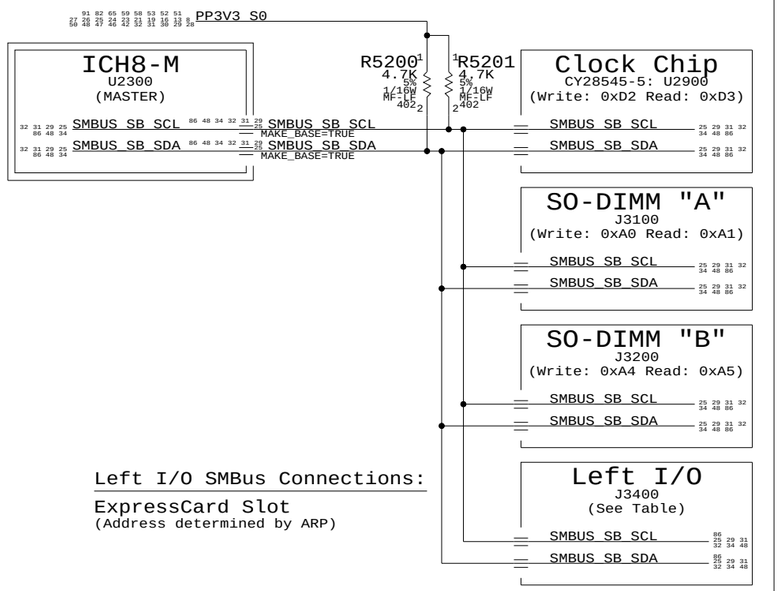
SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

APPLE INC.

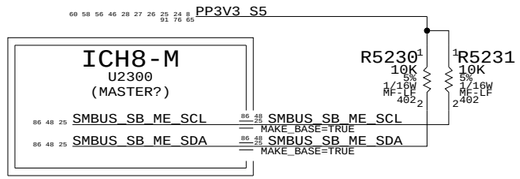
SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0

SCALE	SHT	OF
NONE	47	92

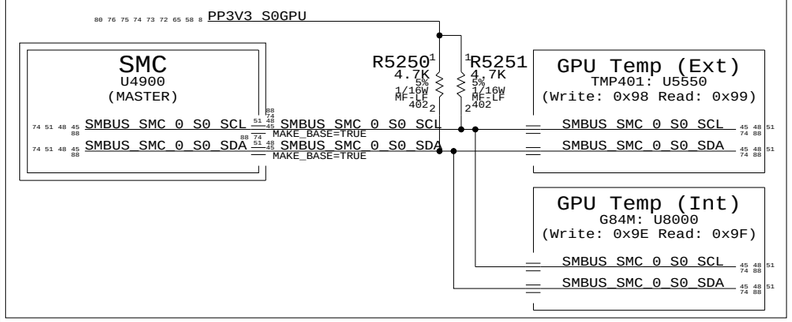
ICH8-M SMBus Connections



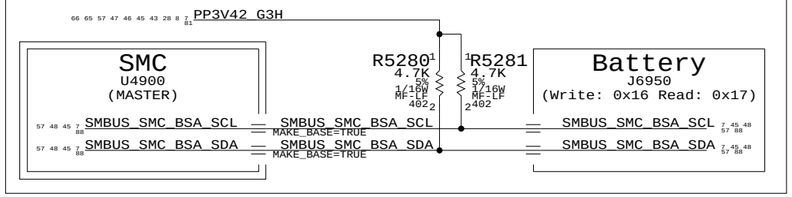
ICH8-M ME SMBus Connections



SMC "0" SMBus Connections

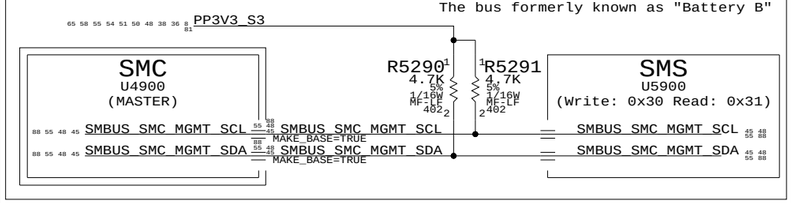


SMC "Battery A" SMBus Connections



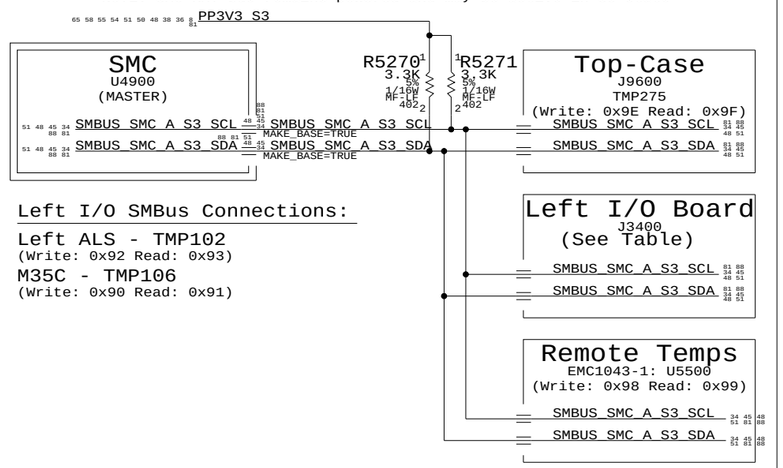
SMC "Management" SMBus Connections

The bus formerly known as "Battery B"

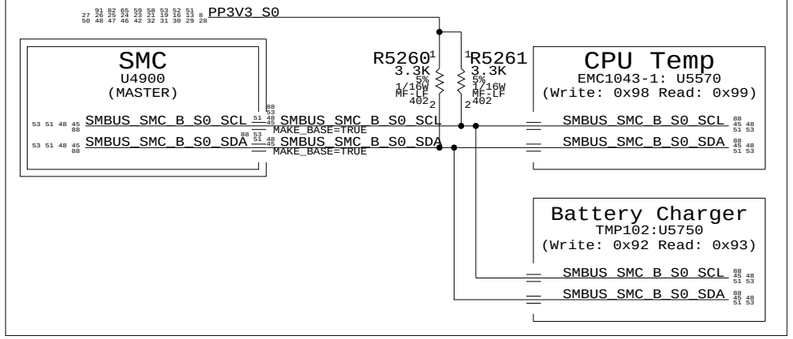


SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state



SMC "B" SMBus Connections



SMBus Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
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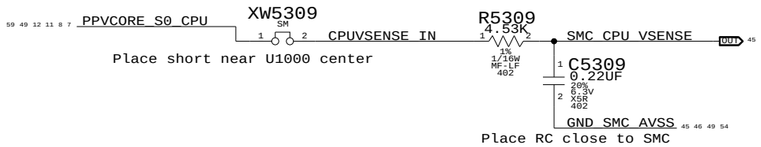
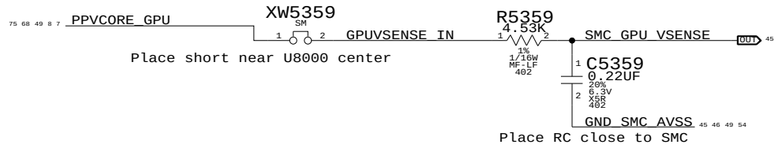
SCALE	SHT	OF
NONE	48	92

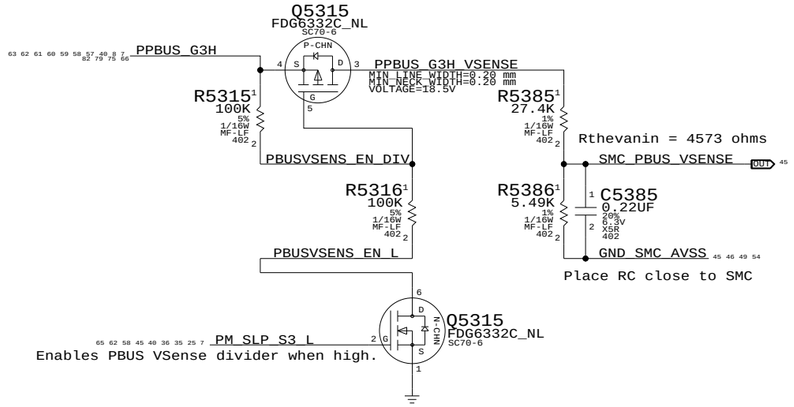
CPU Voltage Sense / Filter



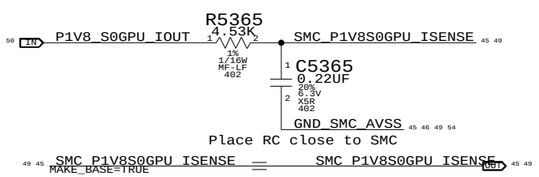
GPU Voltage Sense / Filter



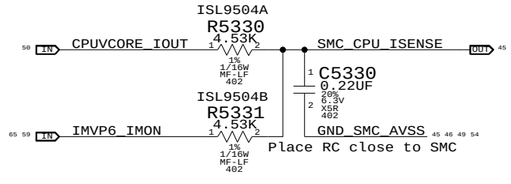
PBUS Voltage Sense & Filter



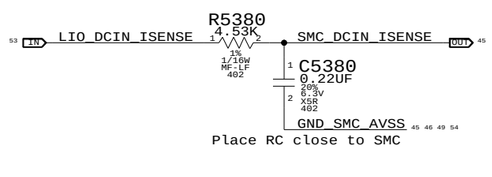
1.8V FB Current Sense Filter



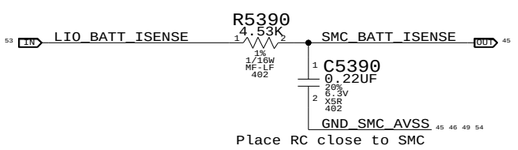
CPU Current Sense Filter



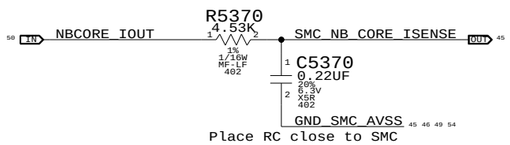
DCIN Current Sense Filter



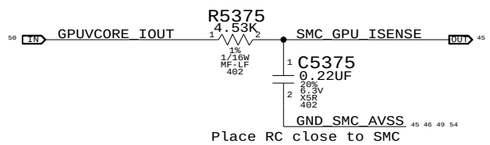
Battery (PBUS) Current Sense Filter



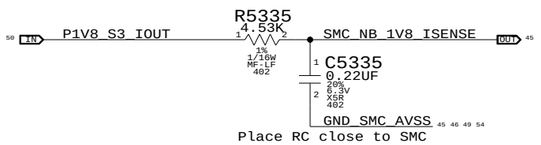
NB Core Current Sense Filter



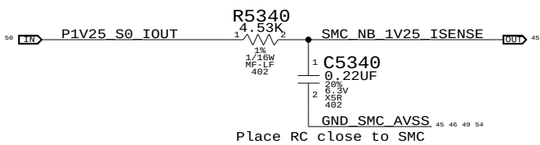
GPU Current Sense Filter



NB 1.8V Current Sense Filter

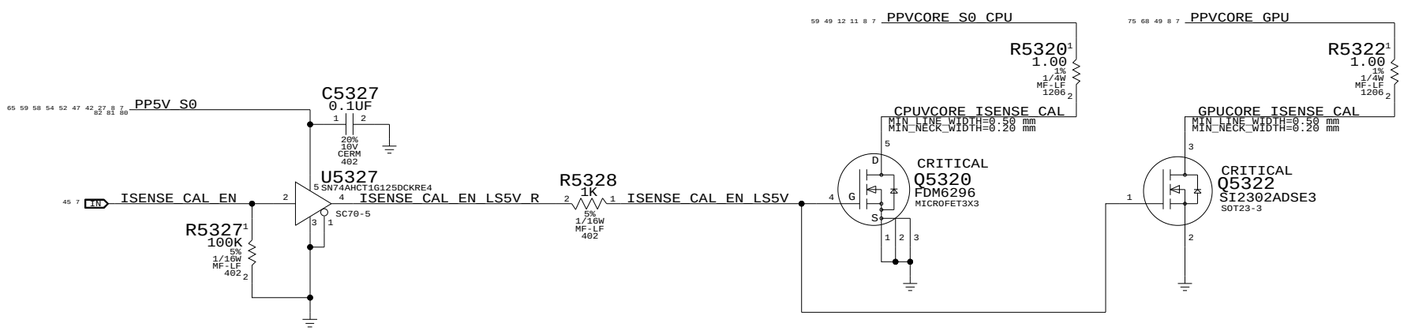


S0/GPU 1.25V Current Sense Filter



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



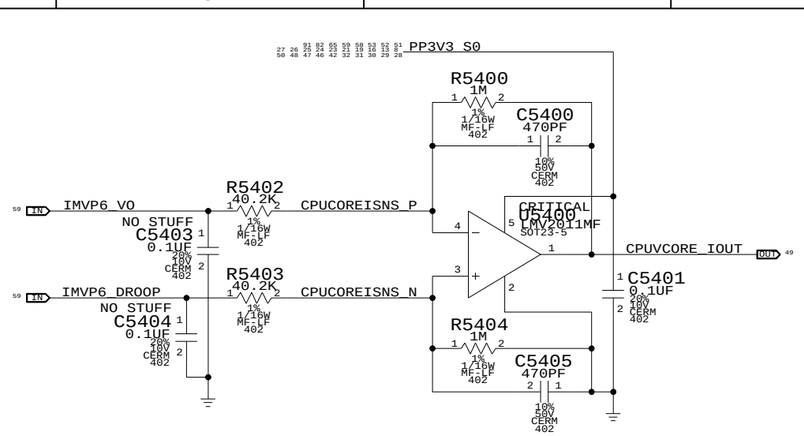
Current & Voltage Sensing

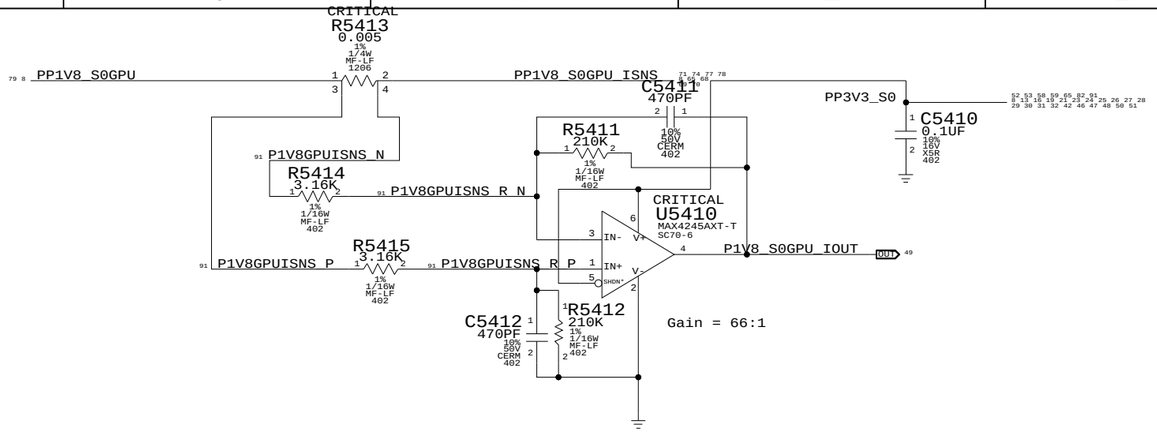
SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

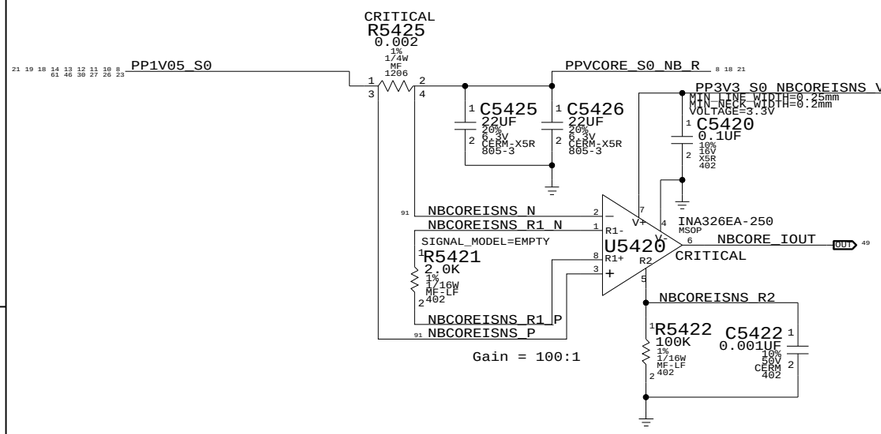
APPLE INC.

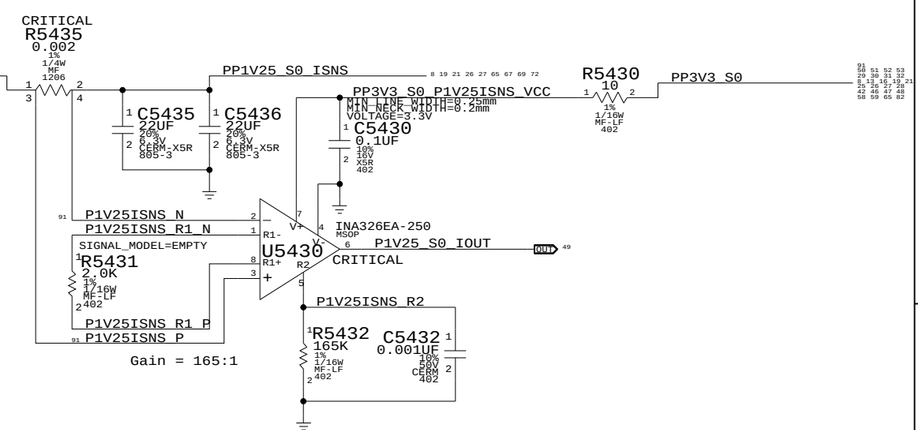
SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 49 OF 92	

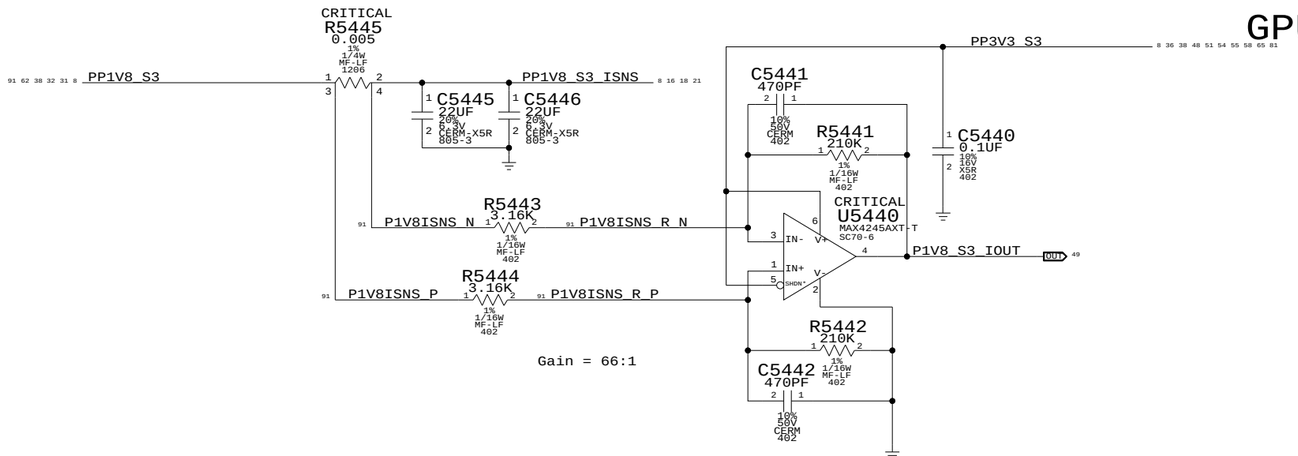
GPU VCore Current Sense

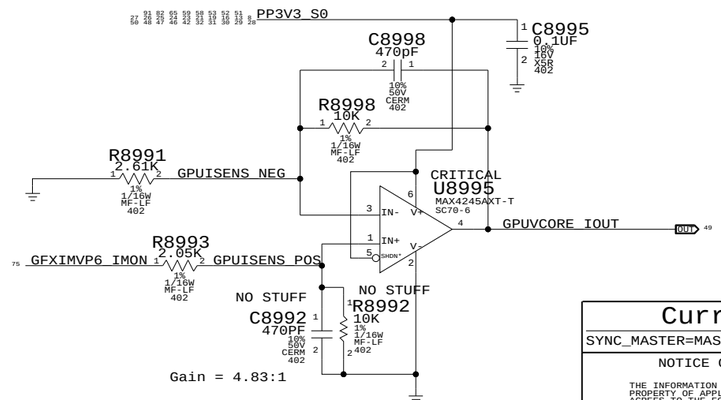












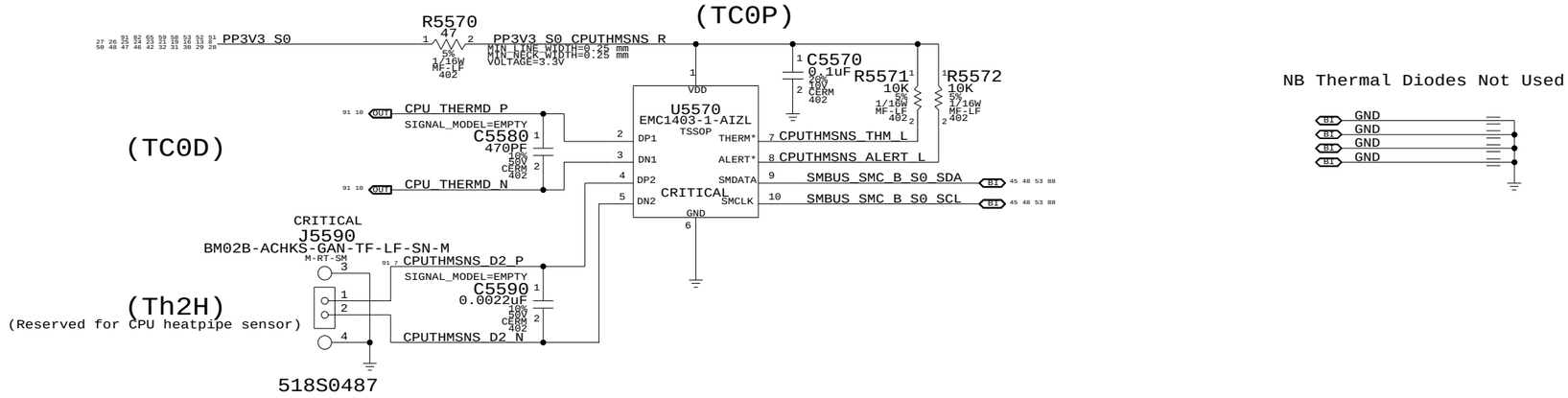
Current Sensing

SYNC_MASTER=MASTER SYNC_DATE=MASTER

APPLE INC.

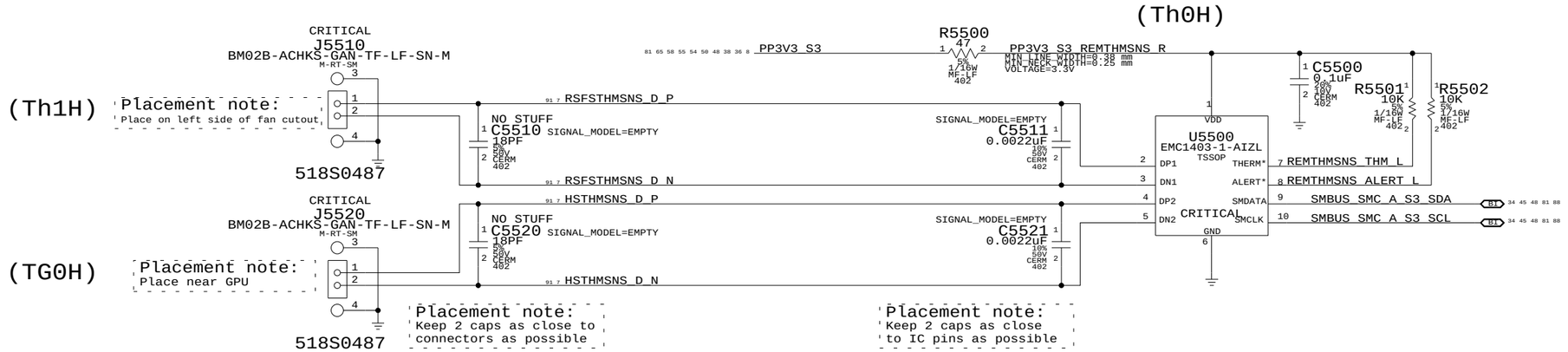
SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 50 OF 92	

CPU T-Diode Thermal Sensor

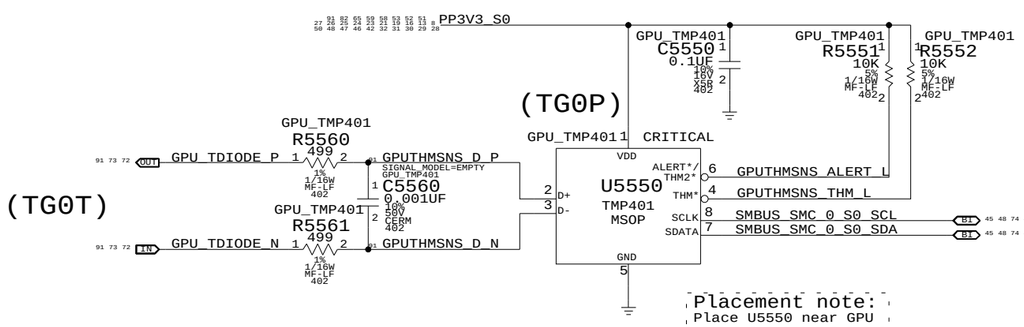


NB Thermal Diodes Not Used

GPU/Heat Pipe & Bottom Case Skin Thermal Sensor



GPU Die Thermal Sensor



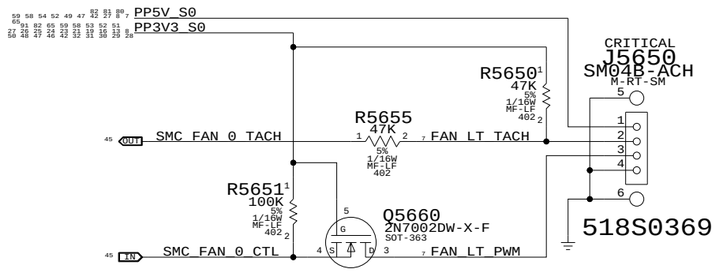
Thermal Sensors

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

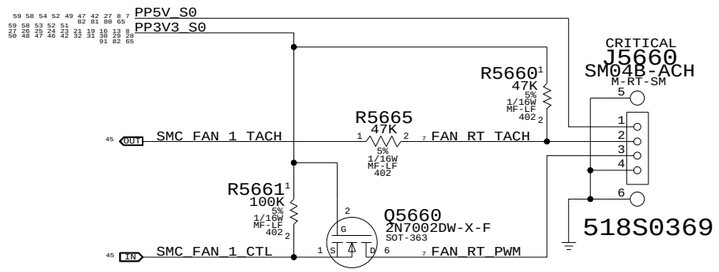
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 51 OF 92	

Left Fan



Right Fan



Fan Connectors

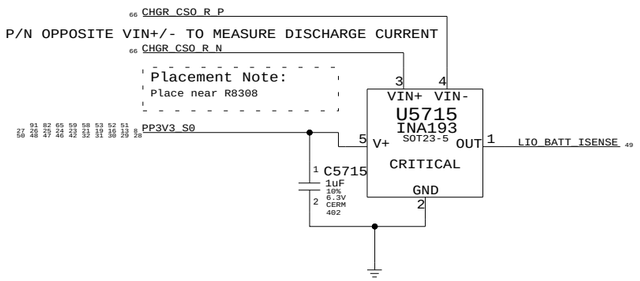
SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

APPLE INC.

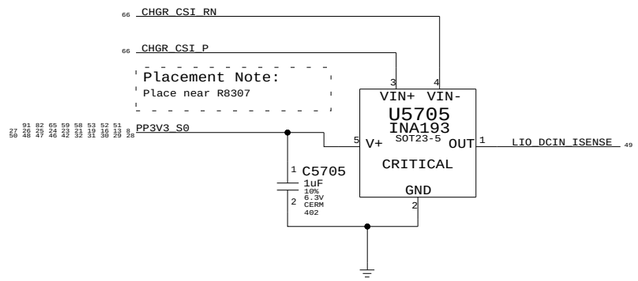
SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0

SCALE	SHT	OF
NONE	52	92

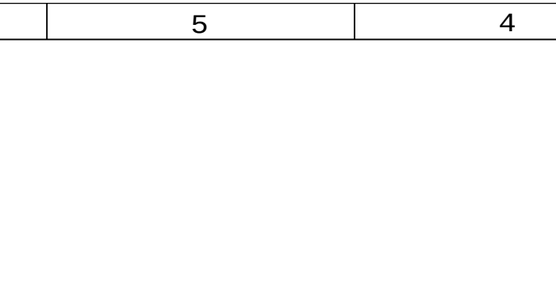
Battery Current Sense



DCIn Current Sense



Battery Charger Thermal Sensor



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S2039	1	revE of TMP102	U5750	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1807	353S2039		U5750	Alternate old version

Current & Thermal Sensors

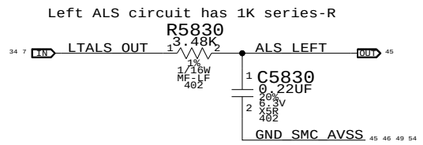
SYNC_MASTER=M87_LIO SYNC_DATE=11/06/2007

APPLE INC.

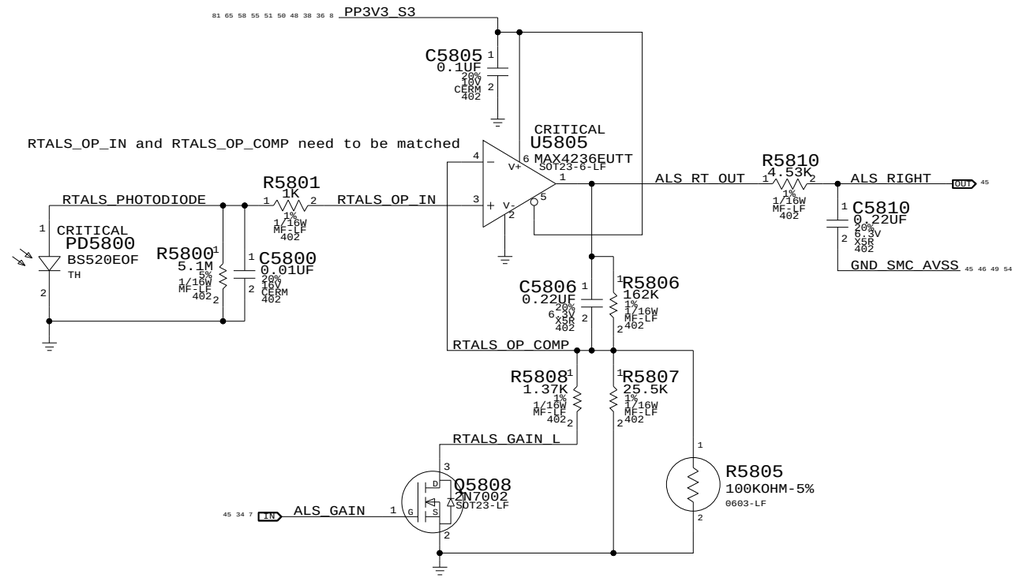
SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 53 OF 92	

Left ALS Filter

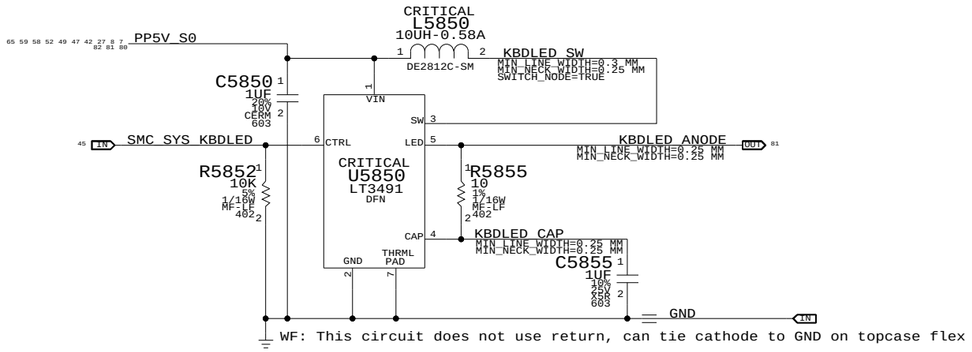
Left ALS circuit has 1K series-R



Right ALS Circuit



Keyboard LED Driver



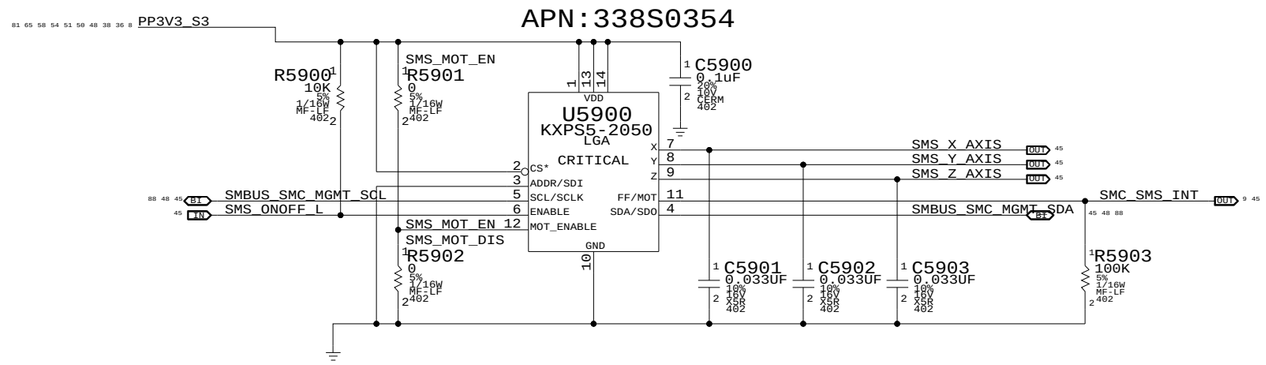
ALS Support

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 54 OF 92	

APN:338S0354

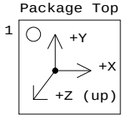


I2C addresses:

ADDR low => 0x30, 0x31
ADDR high => 0x32, 0x33
Alias SCL/SDA to GND if using analog outputs only

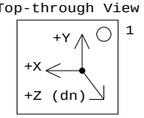
Desired orientation when placed on board top-side:

Package Top



Desired orientation when placed on board bottom-side:

Top-through View

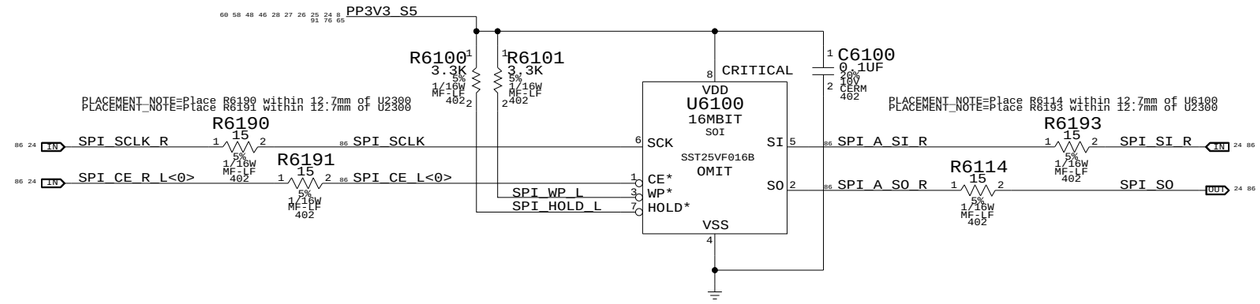


Sudden Motion Sensor (SMS)

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 55 OF 92	



SPI BootROM

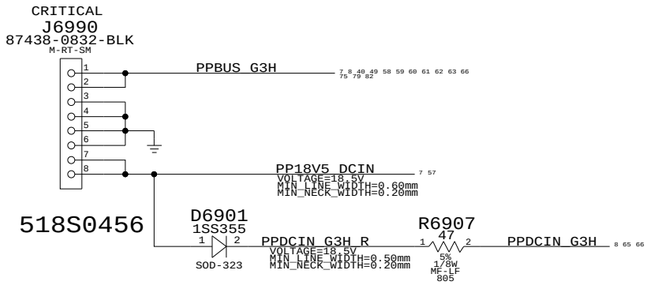
SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

APPLE INC.

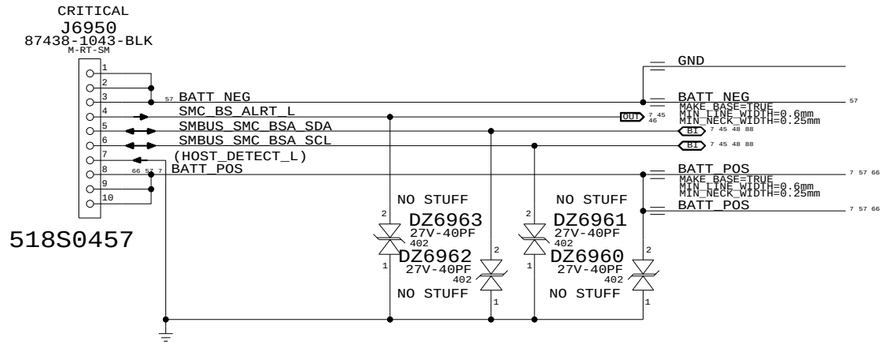
SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0

SCALE	SHT	OF
NONE	56	92

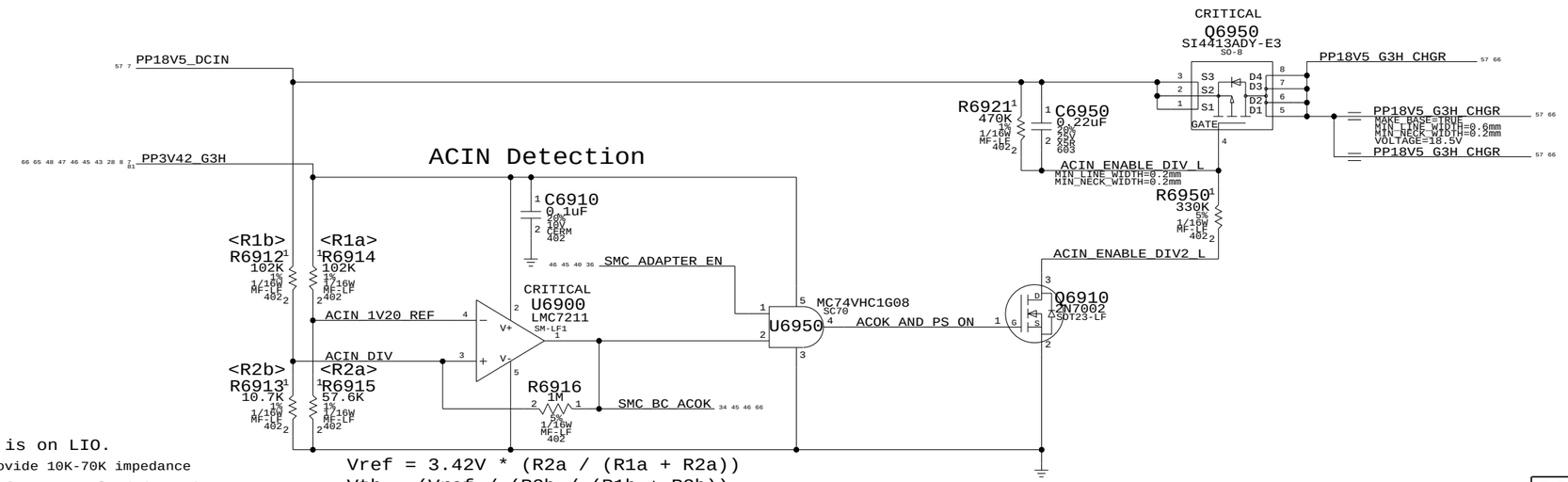
DC-In Connector



Battery Connector



Inrush Limiter



NOTE: R6910 is on LIO.
System must provide 10K-70K impedance
to A52 adapter for system load detection.
REQ of R6910 (on LIO), R6912, & R6913 is 36.9K.

Vref = 3.42V * (R2a / (R1a + R2a))
Vth = (Vref / (R2b / (R1b + R2b))

Vref = 1.23V
Vth = 13.0V

Assuming 1% variance for R6910-R6915 and 3.42V:
Worst case Vth: min:12.47V, max: 13.54V

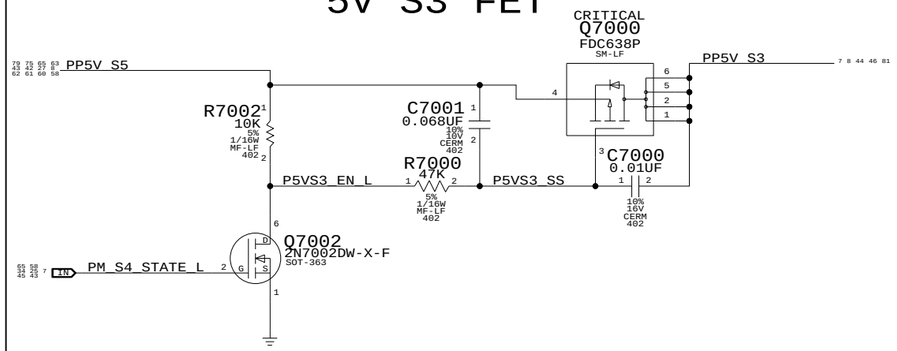
DC-In & Battery Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

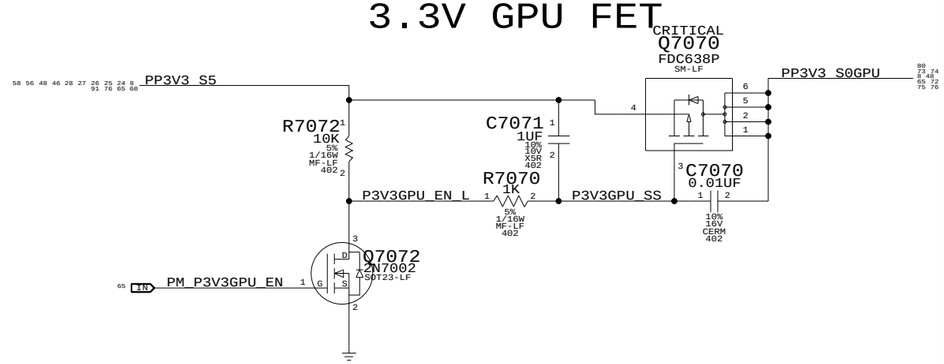
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 57 OF 92	

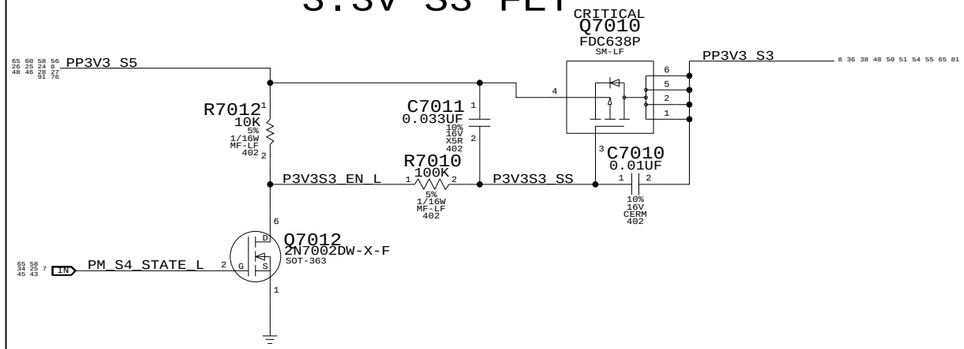
5V S3 FET



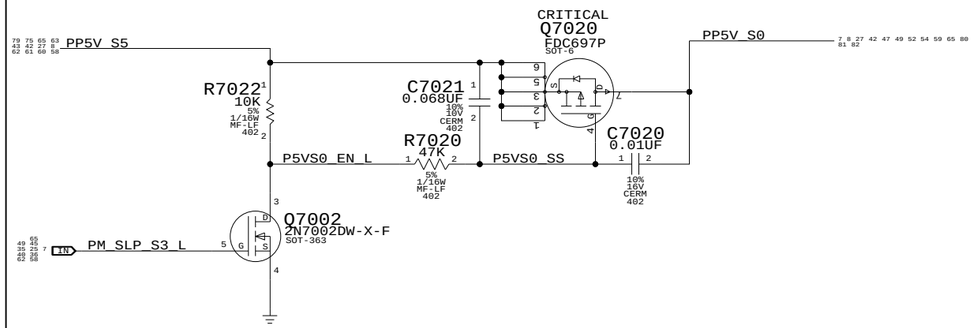
3.3V GPU FET



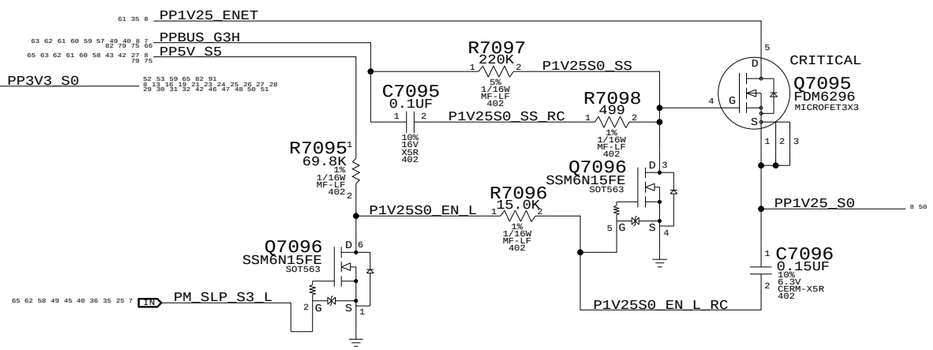
3.3V S3 FET



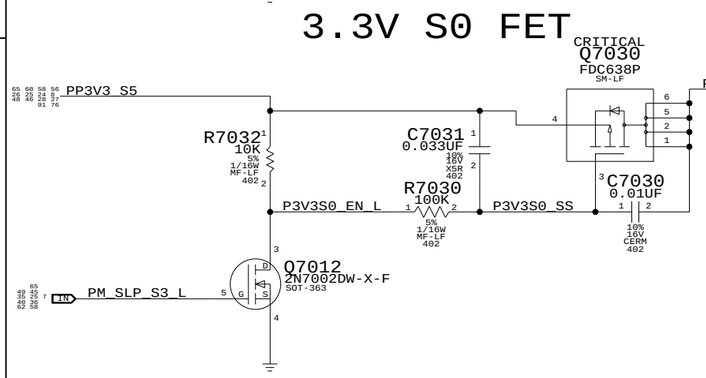
5V S0 FET



1.25V S0 FET



3.3V S0 FET



Power FETs

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 58 OF 92	

DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	0	0	1-Phase	DCM

These caps are for Q7100

These caps are for Q7102

Place R7131 Between L7100,L7101 and CPU

IMVP_VR_ON	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
IMVP6_OCSET	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
IMVP6_VO	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
IMVP6_DROOP	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
IMVP6_DFB	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
IMVP6_SOFT	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
IMVP6_RBIAS	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
IMVP6_VDIFF	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
IMVP6_FB2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
IMVP6_FB	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
IMVP6_COMP	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
IMVP6_VW	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM

IMVP6_PHASE1	MIN_LINE_WIDTH=1.5 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_BOOT1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_UGATE1	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_LGATE1	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_ISEN1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_VSUM1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM
IMVP6_VO1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM
IMVP6_VSEN_P	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM

IMVP6_PHASE2	MIN_LINE_WIDTH=1.5 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_BOOT2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_UGATE2	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_LGATE2	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_ISEN2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM
IMVP6_VSUM2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM
IMVP6_VO2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM
IMVP6_VSEN_N	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM

IMVP6 CPU VCore Regulator

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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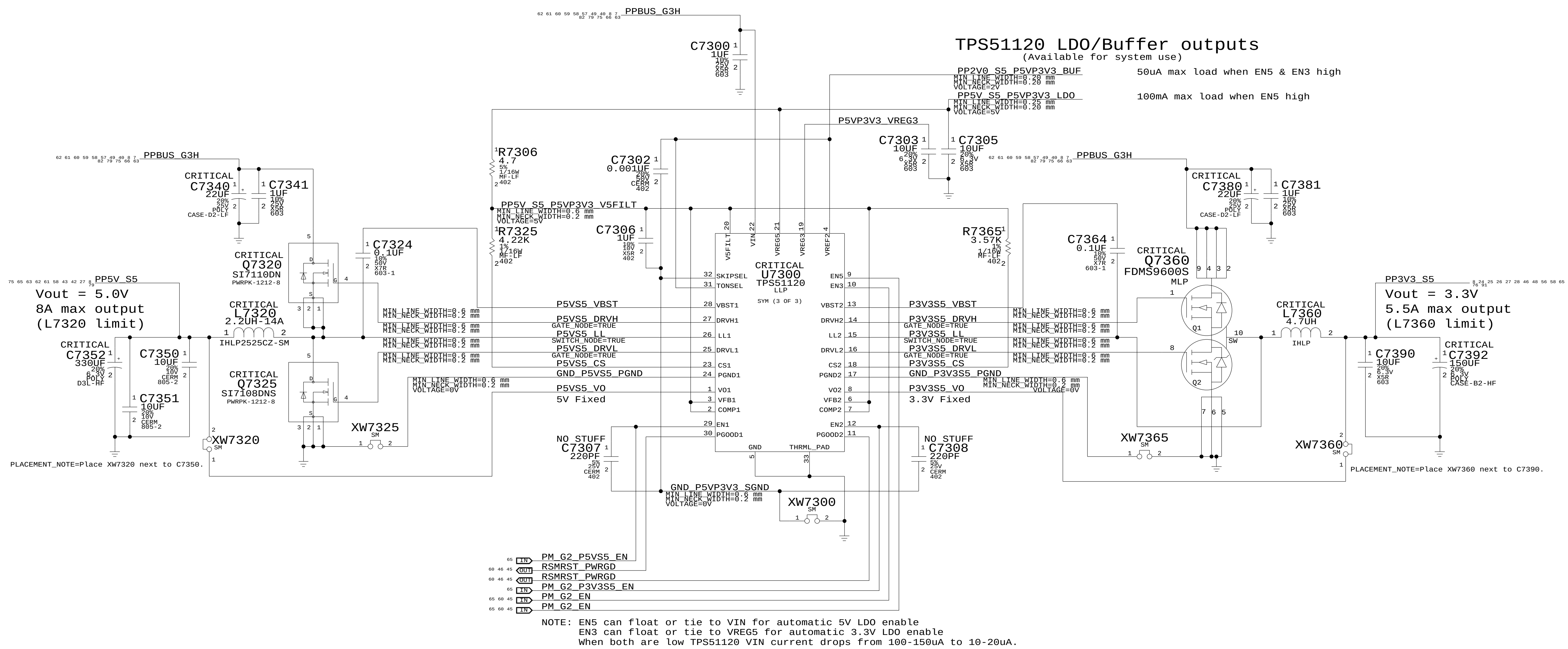
SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 59 OF 92	

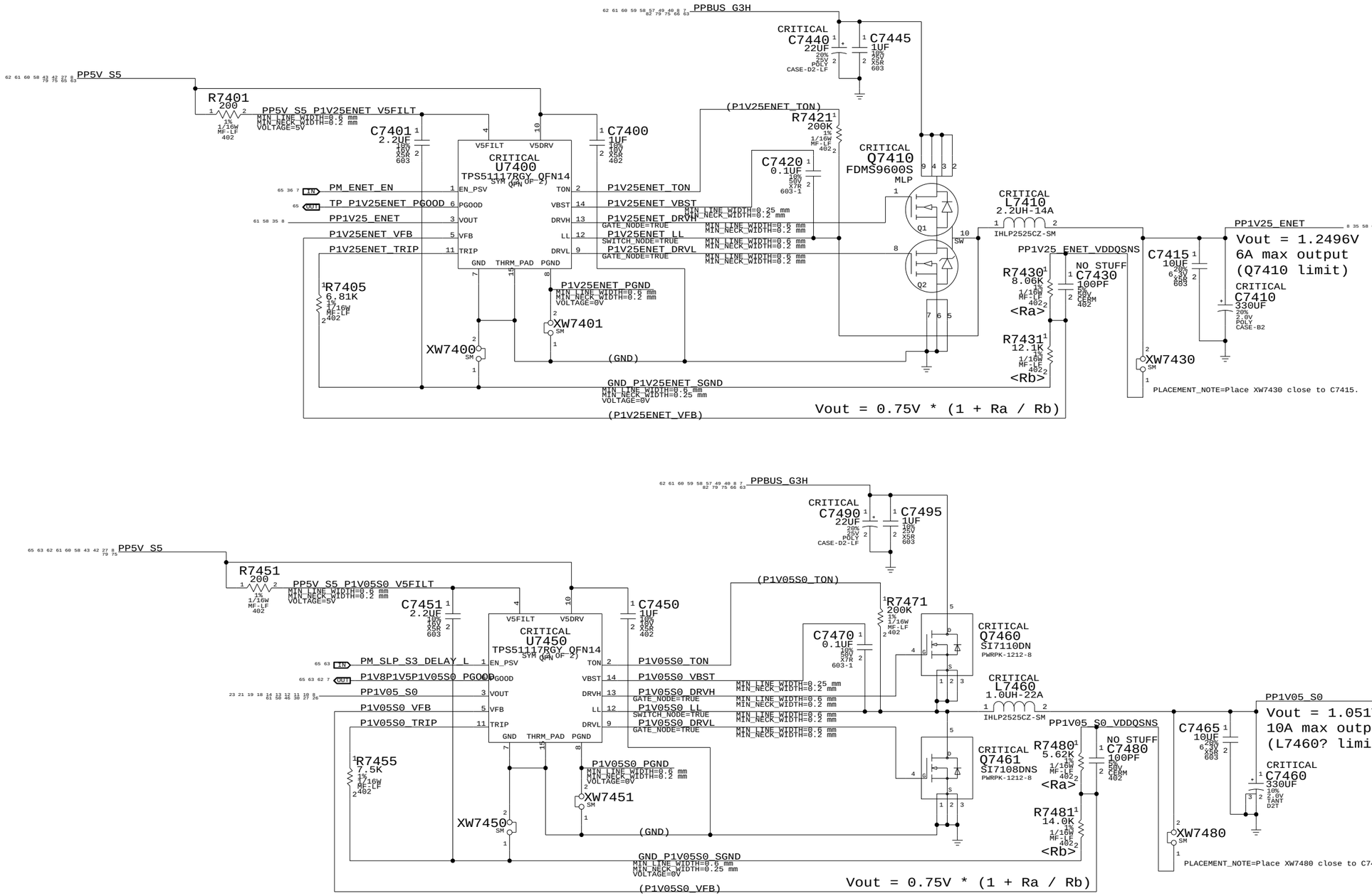


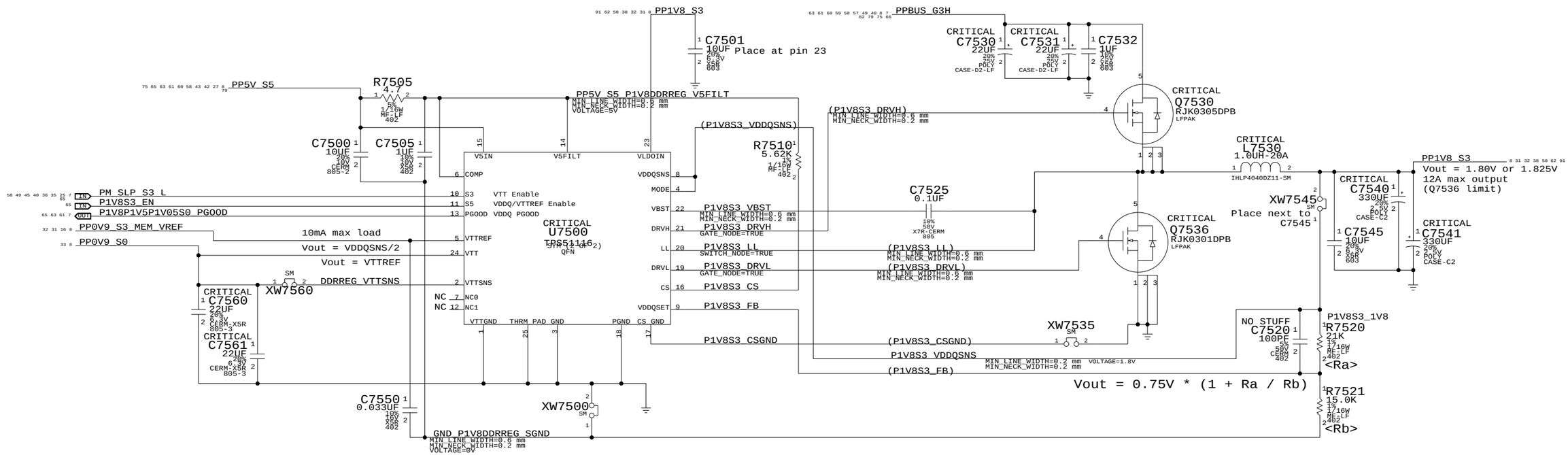
5V / 3.3V Power Supply

SYNC_MASTER=MASTER SYNC_DATE=MASTER

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE NONE	SHT 60 OF 92	

APPLE INC.





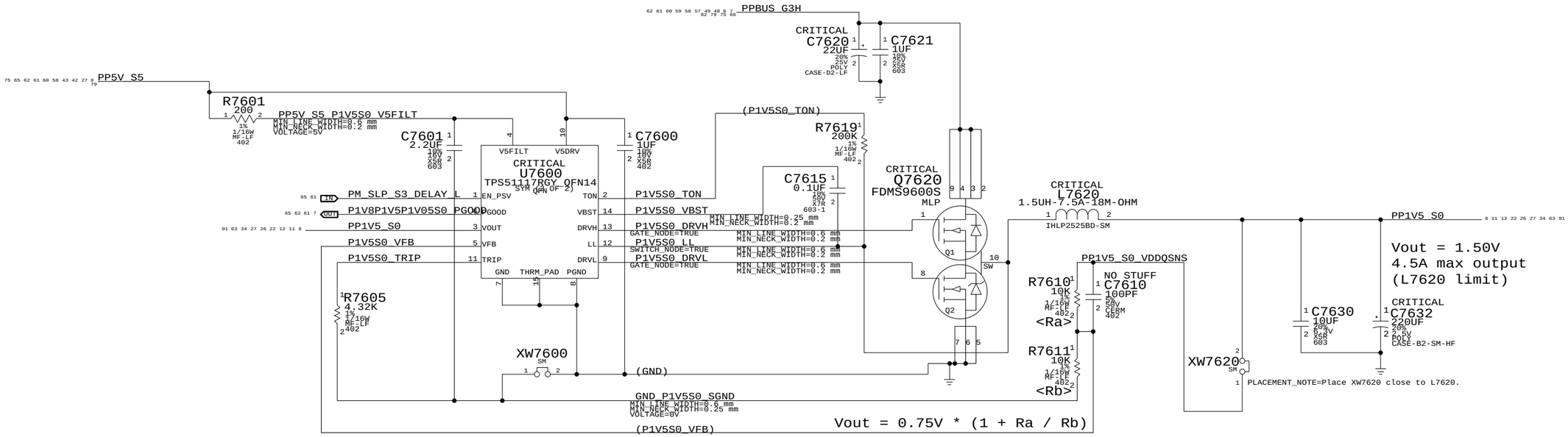
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0346	1	RES,MTL FILM,21.5K,1%,0402,SM,LF	R7520	CRITICAL	P1V8S3_1V825

1.8V DDR2 Supply

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 62 OF 92	



1.5V Power Supply

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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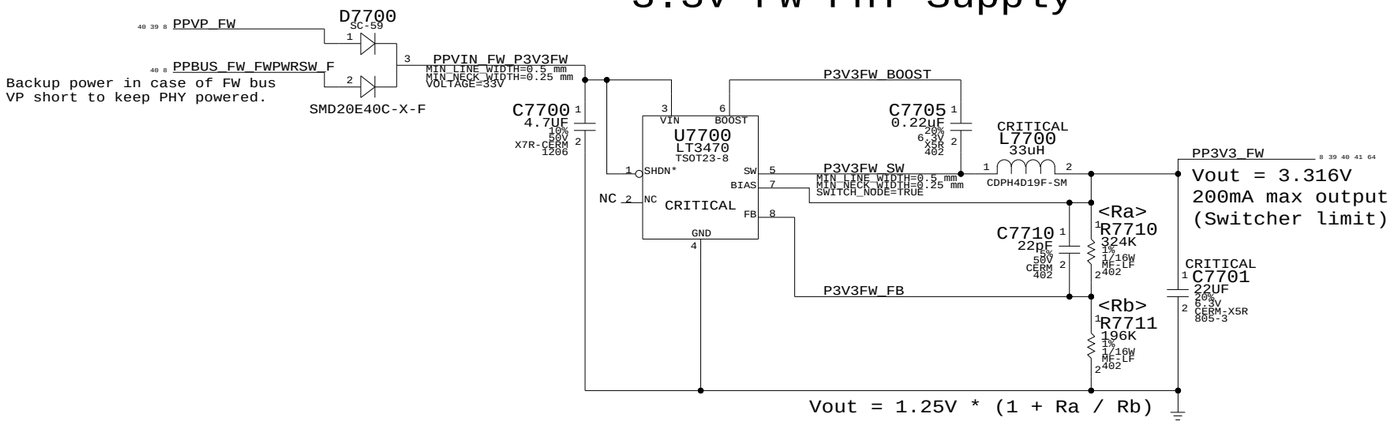
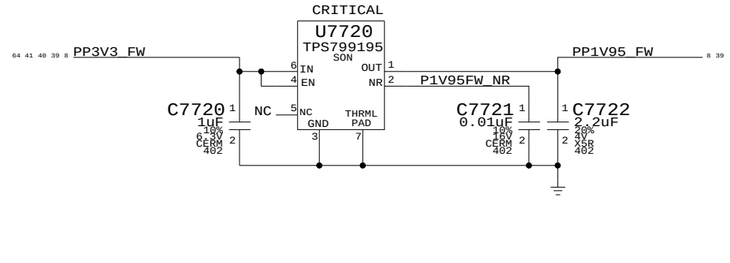
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 63 OF 92	

3.3V FW PHY Supply



1.95V FW PHY Supply



FW PHY Power Supplies

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0

SCALE	SHT	OF
NONE	64	92

Power Control Signals

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

PP5V_S5

R7850 10K 5% 1/16W MF-LF 402

R7851 10K 5% 1/16W MF-LF 402

R7852 100K 5% 1/16W MF-LF 402

R7854 10K 5% 1/16W MF-LF 402

PP3V3_S0GPU

G84M GPU requires rails to come up in the following order:
1) 1.2V
2) 3.3V
3) Vcore
4) 1.8V

PM_P1V8_S0GPU_EN

Need to ensure that TPS51117 PGOOD does not deassert while GPU VIDs are changing GPU core voltage.

PM_P1V8_S0GPU_EN — MAKE_BASE=TRUE — PM_P1V8_S0GPU_EN

PM_GPUVCORE_EN — MAKE_BASE=TRUE — PM_GPUVCORE_EN

Q7850 2N7002DW-X-F SOT-363

Q7851 2N7002DW-X-F SOT-363

PVCOREGPU_EN_L

C7851 0.1UF 20% 10V CERM 402

Q7851 2N7002DW-X-F SOT-363

PM_SLP_S3_LS5V — MAKE_BASE=TRUE — PM_SLP_S3_LS5V

Q7850 2N7002DW-X-F SOT-363

PM_SLP_S3_L

R7856 100K 5% 1/16W MF-LF 402

(PM_SLP_S3_L) — MAKE_BASE=TRUE

PM_SLP_S3_L

PP3V3_S0

PP3V3_S5

MC74VHC1G09 SC70 U7850

PM_SLP_S3_DELAY_L — MAKE_BASE=TRUE

R7859 10K 5% 1/16W MF-LF 402

NO STUFF C7859 0.047UF 10% 10V CERM 402

PM_SLP_S3_DELAY_L

PM_SLP_S3_DELAY_L

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

PPDCIN_G3H

P3V42G3H5_BOOST

C7800 10UF 20% 16V X5R 1206-1

U7800 LT3470 TSOT23-8

VIN BOOST SHDN* SW BIAS NC FB GND

NC CRITICAL

C7805 0.22UF 20% 6.3V X5R 402

CRITICAL L7810 33UH CDPH4D19F-SM

P3V42G3H_SW

MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE

P3V42G3H_FB

C7810 22pF 5% 50V CERM 402

<Ra> R7810 348K 1% 1/16W MF-LF 402

<Rb> R7811 200K 1% 1/16W MF-LF 402

PP3V42_G3H

Vout = 3.425
200mA max output
(Switcher limit)

C7815 22UF 20% 6.3V CERM-X5R 805-3

Vout = 1.25V * (1 + Ra / Rb)

Unused PGOOD Signals

TP_P1V25ENET_PGOOD — MAKE_BASE=TRUE — TP_P1V25ENET_PGOOD

TP_P1V8_S0GPU_PGOOD — MAKE_BASE=TRUE — TP_P1V8_S0GPU_PGOOD

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

PP1V25_S0_ISNS

R7860 154K 1% 1/16W MF-LF 402

PP3V3_S3

MAX6838 threshold is 93.5% @ 1.120V

U7860 MAX6838XSD0 SC70-4

VCC RESET-IN RESET+ GND

S0PGOOD_1V2_DIV

R7861 100K 1% 1/16W MF-LF 402

C7860 0.0047UF 10% 16V CERM 402

R7862 100K 5% 1/16W MF-LF 402

PM_P3V3GPU_EN — MAKE_BASE=TRUE — PM_P3V3GPU_EN

PM_P3V3GPU_EN

IMVP6_IMON

To CPU IMVP6

PP3V3_S5

R7865 100K 5% 1/16W MF-LF 402

ISL9504A

R7866 0 5% 1/16W MF-LF 402

P1V8P1V5P1V05S0_PGOOD

TPS51117 PGOOD threshold 92.5-97.5% (1.36 - 1.46V)

P1V8P1V5P1V05S0_PGOOD

TPS51117 PGOOD threshold 92.5-97.5% (0.98 - 1.02V)

P1V8P1V5P1V05S0_PGOOD

P1V8P1V5P1V05S0_PGOOD — MAKE_BASE=TRUE

PP3V3_S0

C7880 0.1UF 20% 16V CERM 402

MC74VHC1G08 SC70 U7880

ALL_SYS_PWRGD

PM_ENET_EN — (PM_ENET_EN) — MAKE_BASE=TRUE — PM_ENET_EN

PM_S4_STATE_L — (PM_S4_STATE_L) — MAKE_BASE=TRUE — PM_S4_STATE_L

R7857 10K 5% 1/16W MF-LF 402

R7855 10K 5% 1/16W MF-LF 402

P1V8S3_EN — MAKE_BASE=TRUE — P1V8S3_EN

C7855 0.47UF 10% 6.3V CERM-X5R 402

NOTE: 0.9V is not checked!

Other S0 Rails PWRGD Circuit

PP3V3GPU_EN IS A PROXY FOR 1.2V

PP5V_S0

PP3V3_S0

PP1V8_S0GPU_ISNS

PM_P3V3GPU_EN

C7872 0.1UF 20% 10V CERM 402

C7871 0.1UF 20% 10V CERM 402

C7870 0.1UF 20% 10V CERM 402

R7875 10K 5% 1/16W MF-LF 402

U7870 LTC2900 DFN

V1 V2 V3 V4 PBR* RST* VREF VPG CRT GND THRM_PAD

NC

S0PGOOD_VREF

S0PGOOD_PWROK

R7870 9.53K 1% 1/16W MF-LF 402

S0PGOOD_CRT

S0PGOOD_VPG

C7875 0.047UF 10% 16V CERM 402

R7871 93.1K 1% 1/16W MF-LF 402

Trst = 4.6ms/nF
Trst = 216ms

LTC2900 typical threshold is 93.5% (4.675V, 3.086V, 1.685V,1.120V)

PM_G2_EN — MAKE_BASE=TRUE — PM_G2_EN

C7858 0.1UF 20% 10V CERM 402

PP3V42_G3H

R7858 100K 5% 1/16W MF-LF 402

MC74VHC1G09 SC70 U7858

PM_G2_P5VS5_EN — MAKE_BASE=TRUE — PM_G2_P5VS5_EN

MC74VHC1G09 SC70 U7859

PM_G2_P3V3S5_EN — MAKE_BASE=TRUE — PM_G2_P3V3S5_EN

3.425V G3Hot Supply & Power Control

SYNC_MASTER=M87_MLB SYNC_DATE=09/26/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 65 OF 92	

PBus Supply & Battery Charger

PP18V5_G3H_CHGR
CHGR_VDD
Q7940 IRLML5203-2.6A SM
R7940 110K 1% 1/16W MF-LF 402
CHGR_ACSET
D7940 BAV99T-X-F SOT-523-3
NC
CHGR_ACSET_D
R7941 11.3K 1% 1/16W MF-LF 402
R7944 100K 1% 1/16W MF-LF 402
C7941 0.1uF 10% 10V X5R 402
CHGR_SGND
R7950 100K 1% 1/16W MF-LF 402
CHGR_EN
PP3V42_G3H
R7924 100K 1% 1/16W MF-LF 402
Q7950 SSM3K15FV SOD-VESM
CHGR_ACPRN
CHGR_SGND
CHGR_DCIN
C7940 0.1UF 20% 25V CERM 603
NO STUFF C7907 0.1UF 20% 25V CERM 603
CHGR_CSO_R_N
C7900 0.033uF 10% 16V X7R 402
C7901 1000PF 10% 25V X7R 402
CHGR_ICM_R
CHGR_VCOMP_C
R7902 3.01K 1% 1/16W MF-LF 402
CHGR_ICOMP
CHGR_VCOMP
TP_CHGR_VADJ
C7915 680pF 10% 50V CERM 402
NO STUFF
C7902 0.0082uF 10% 25V X7R 402
C7990 470PF 10% 50V CERM 402
CHGR_CSO_P
CHGR_CSO_N
CHGR_CHLIM
CHGR_VREF
CHGR_ACPRN
CHGR_ACSET
CHGR_SGND
C7911 1uF 10% 6.3V CERM 402
CHGR_SGND
CHGR_VDD
R7900 4.7 5% 1/16W MF-LF 402
CHGR_VDDP
C7912 1UF 20% 25V CERM 402
R7992 56.2K 1% 1/16W MF-LF 402
CHGR_ICMP
U7900 SL6257HRZ QFN
CRITICAL
VDD VDDP
ACLIM ICOMP VCOMP VADJ CELLS CSOP CSON CHLIM VREF ACPRN ACSET
SGATE CSIP CSIN BGATE DCIN BOOT UGATE PHASE LGATE EN DCPRN DCSET
THRML_PAD GND PGND
CHGR_SGATE
CHGR_CSI_P
CHGR_CSI_N
NC_CHGR_BGATE
CHGR_DCIN
CHGR_BOOT
CHGR_UGATE
CHGR_LGATE
CHGR_EN
TP_CHGR_DCPRN
TP_CHGR_DCSET
353S1510
XW7900 SM
CHGR_PHASE
R7970 49.9 1% 1/16W MF-LF 603
C7970 0.0022uF 10% 50V CERM 603
CHGR_SGND
Q7900 SI4413ADY-E3 SO-8
CRITICAL
D4 D3 D2 D1 S3 S2 S1 GATE
PPVDCIN_G3H_PRE
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.25mm
NO STUFF R7910 100K 1% 1/16W MF-LF 402
MIN_LINE_WIDTH=0.2mm
MIN_NECK_WIDTH=0.2mm
NO_TEST=TRUE
R7907 0.02 1% 1/2W MF 0612
XW7901 SM
XW7902 SM
PPVDCIN_G3H_R
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.25mm
CRITICAL C7916 2.2UF 10% 25V X5R-CERM 805
CRITICAL C7917 2.2UF 10% 25V X5R-CERM 805
CRITICAL C7905 22UF 20% 25V POLY CASE-D2-LF
CRITICAL C7906 22UF 20% 25V POLY CASE-D2-LF
C7904 0.1UF 20% 25V CERM 402
R7905 18 5% 1/16W MF-LF 402
CHGR_CSI_RN
NO_TEST=TRUE
R7903 2.2 5% 1/16W MF-LF 402
CHGR_BOOT_R
CRITICAL D7900 SOD-123 B0530WXF
CHGR_VDDP
C7903 0.1UF 20% 25V CERM 603
CRITICAL D7903 SOT23 MMBZ5235B
CHGR_PHASE
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.2mm
SWITCH_NODE=TRUE
Q7901 RJK0305DPB LFPAK
CRITICAL
Q7902 RJK0305DPB LFPAK
CRITICAL
CRITICAL L7900 4.7UH-10.2A FDA1254-SM
10A MAX, LIMITED BY L7900, Q7901
PPBUS_G3H
R7908 0.01 1% 1/2W MF 0612
PPVBAT_G3H_CHGR_OUT
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.25mm
CRITICAL C7908 22UF 20% 25V POLY CASE-D2-LF
XW7903 SM
XW7904 SM
C7910 1UF 10% 25V X5R 603
R7904 0 5% 1/16W MF-LF 402
CHGR_CSO_R_N
NO_TEST=TRUE
CHGR_CSO_N
R7906 2.2 5% 1/16W MF-LF 402
CHGR_CSO_R_P
CHGR_CSO_P

Energy Star LDO

VOLTAGE FOLLOWER GUARANTEES CURRENT LIMIT CIRCUITS ARE PROVIDED WITH SUFFICIENT CURRENT WITHOUT SINKING CURRENT FROM VREF.

PP3V42_G3H
CRITICAL U7901 MAX4245AXT-T SC70-6
CHGR_VREF
CHGR_VREF_VF
C7980 0.1UF 20% 25V CERM 402
CHGR_SGND

Adapter Input Current Limit

As shown, Isys =~4.6A max

PP3V42_G3H
R7969 10K 5% 1/16W MF-LF 402
R7968 3.48K 1% 1/16W MF-LF 402
R7960 3.01K 1% 1/16W MF-LF 402
CHGR_ACLIM_R
CHGR_ACLIM
Q7960 SSM6N15FE SOT563
R7963 20.0K 1% 1/16W MF-LF 402
C7961 0.047UF 10% 16V CERM 402
SMC_SYS_ISET
SMC_SYS_ISET_L
CHGR_SGND

Battery Charge Current Limit

As shown, Ichg = 4.5A max

PP3V42_G3H
R7979 10K 5% 1/16W MF-LF 402
R7964 3.57K 1% 1/16W MF-LF 402
R7967 158K 1% 1/16W MF-LF 402
R7962 17.8K 1% 1/16W MF-LF 402
CHGR_CHLIM_R
CHGR_CHLIM
Q7961 SSM6N15FE SOT563
R7966 11.3K 1% 1/16W MF-LF 402
C7962 0.01UF 10% 16V CERM 402
SMC_BATT_ISET
SMC_BATT_ISET_L
CHGR_SGND

U7950 MAX8719 TDFN
VCC IN SHDN* I.C. GND THRML PAD PGOOD FB OUT
PP18V5_G3H_CHGR
SMC_ENRGYSTR_LDO_EN
NC
LDO_FDBK
LDO_OUT
MIN_LINE_WIDTH=0.5mm
MIN_NECK_WIDTH=0.2MM
R7954 100K 5% 1/16W MF-LF 402
C7950 1UF 10% 25V X5R 603
R7952 200K 1% 1/16W MF-LF 402
R7953 19.6K 1% 1/16W MF-LF 402
D7950 BAT54CW-X-F SOT-323
PPBUS_G3H
C7951 1UF 10% 25V X5R 603

Battery Charge FETs

PPVBAT_G3H_CHGR_OUT
NO STUFF C7922 0.01UF 10% 16V CERM 402
C7921 0.1UF 10% 16V X5R 402
C7920 0.01UF 10% 16V CERM 402
R7930 470K 1% 1/16W MF-LF 402
C7925 0.22uF 10% 16V CERM 402
CRITICAL Q7920 SI4413ADY-E3 SO-8
PPVBAT_G3H_PRE
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.25mm
VOLTAGE=12.6V
CRITICAL R7920 27 5% 1/2W MF 2525-1
D7921 1SS355 SOD-323
PPVBAT_G3H_DIO
MIN_LINE_WIDTH=0.5mm
MIN_NECK_WIDTH=0.25mm
VOLTAGE=12.6V
R7921 47 5% 1/16W MF-LF 805
PPDCIN_G3H
CRITICAL Q7921 SI4413ADY-E3 SO-8
CRITICAL F7902 8AMP-24V 1206-1
CRITICAL Q7970 SI4413ADY-E3 SO-8
PPVBATT_G3H_FET
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.25mm
VOLTAGE=12.6V
PPVBATT_G3H_FET_F
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.25mm
BATT_POS
MIN_LINE_WIDTH=0.8mm
MIN_NECK_WIDTH=0.25mm
CHG_EN_DIV_L
CHG_EN_DIV2_L
R7931 330K 5% 1/16W MF-LF 402
NO STUFF C7924 0.01UF 10% 16V CERM 402
R7922 39.2K 1% 1/16W MF-LF 402
TCHG_EN_DIV_L
R7923 35.7K 1% 1/16W MF-LF 402
TCHG_EN_DIV2_L
R7972 330K 5% 1/16W MF-LF 402
PPVBATT_G3H_FET_GATE
R7971 470K 5% 1/16W MF-LF 402
C7971 0.1UF 10% 25V X5R 402
C7927 0.001UF 10% 50V CERM 402
GND
Q7924 SSM6N15FE SOT563
Q7922 SSM6N15FE SOT563
SMC_BATT_CHG_EN
CHGR_ACPRN
SMC_BC_ACOK
SMC_BATT_TRICKLE_EN_L

PBus Supply & Batt. Charger
SYNC_MASTER=MASTER
SYNC_DATE=MASTER

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APPLE INC.
SIZE D
DRAWING NUMBER 051-7431
REV. A.0.0
SCALE NONE
SHT 66 OF 92

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PEX 1.2V Current = 2A

PP1V25_S0_ISNS
PP1V25_S0_ISNS
PP1V25_S0_ISNS

NC_GPU_DFM
NO_TEST=TRUE
OMIT

U8000
NB8P-GS-W-A2
BGA
(2 OF 8)

A26	PEX_IOVDD_1	AD23
A28	PEX_IOVDD_2	AF23
B32	PEX_IOVDD_3	AF24
D1	PEX_IOVDD_4	AF25
D31	PEX_IOVDD_5	AG24
D32	PEX_IOVDD_6	AG25
F1		
F6		
G8	PEX_IOVDDQ_1	AC16
M5	PEX_IOVDDQ_2	AC17
U6	PEX_IOVDDQ_3	AC21
V1	PEX_IOVDDQ_4	AC22
V3	PEX_IOVDDQ_5	AE18
V4	PEX_IOVDDQ_6	AE21
V5	PEX_IOVDDQ_7	AE22
V6	NC PEX_IOVDDQ_8	AF12
W1	PEX_IOVDDQ_9	AF18
W3	PEX_IOVDDQ_10	AF21
W4	PEX_IOVDDQ_11	AF22
W5		
Y5		
Y6	PEX_PLLAVDD	AF15
AC26	PEX_PLLDVDD	AE15
AD26	PEX_PLLGND	AE16
AE26		
AG12		
AH13		
AH31		
AH32		
AM8		
AM9		

250mA
C8002 1UF 10% 6.3V CERM 402
C8001 4.7UF 20% 6.3V CERM 603
C8000 22UF 20% 6.3V CERM-X5R 805
C8003 1UF 10% 6.3V CERM 402
C8004 0.1UF 20% 10V CERM 402
C8005 0.1UF 20% 10V CERM 402

1500mA
C8008 1UF 10% 6.3V CERM 402
C8007 4.7UF 20% 6.3V CERM 603
C8006 22UF 20% 6.3V CERM-X5R 805
C8009 1UF 10% 6.3V CERM 402
C8010 0.1UF 20% 10V CERM 402
C8011 0.1UF 20% 10V CERM 402

180mA
PP1V2_GPU_PEX_PLLAVDD_F
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.2V
L8012 10NH-600MA 0603
C8014 0.1UF 20% 10V CERM 402
C8013 4.7UF 20% 6.3V CERM 603
C8012 4.7UF 20% 6.3V CERM 603

20mA
PP1V2_GPU_PEX_PLLDVDD_F
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.2V
L8015 10NH-600MA 0603
C8017 0.1UF 20% 10V CERM 402
C8016 4.7UF 20% 6.3V CERM 603
C8015 4.7UF 20% 6.3V CERM 603

OMIT

U8000
NB8P-GS-W-A2
BGA
(1 OF 8)

PCI-EXPRESS BUS INTERFACE

PEG_R2D_C_P<0>	C8020 0.1uF	PEG_R2D_P<0>	AK13	PEX_RX0	PEX_TX0 AJ15	PEG_D2R_C_P<0> C8055 0.1uF PEG_D2R_P<0>
PEG_R2D_C_N<0>	C8021 0.1uF	PEG_R2D_N<0>	AK14	PEX_RX0_L	PEX_TX0_L AK15	PEG_D2R_C_N<0> C8056 0.1uF PEG_D2R_N<0>
PEG_R2D_C_P<1>	C8022 0.1uF	PEG_R2D_P<1>	AM14	PEX_RX1	PEX_TX1 AH16	PEG_D2R_C_P<1> C8057 0.1uF PEG_D2R_P<1>
PEG_R2D_C_N<1>	C8023 0.1uF	PEG_R2D_N<1>	AM15	PEX_RX1_L	PEX_TX1_L AG16	PEG_D2R_C_N<1> C8058 0.1uF PEG_D2R_N<1>
PEG_R2D_C_P<2>	C8024 0.1uF	PEG_R2D_P<2>	AL15	PEX_RX2	PEX_TX2 AG17	PEG_D2R_C_P<2> C8059 0.1uF PEG_D2R_P<2>
PEG_R2D_C_N<2>	C8025 0.1uF	PEG_R2D_N<2>	AL16	PEX_RX2_L	PEX_TX2_L AH17	PEG_D2R_C_N<2> C8060 0.1uF PEG_D2R_N<2>
PEG_R2D_C_P<3>	C8026 0.1uF	PEG_R2D_P<3>	AK16	PEX_RX3	PEX_TX3 AG18	PEG_D2R_C_P<3> C8061 0.1uF PEG_D2R_P<3>
PEG_R2D_C_N<3>	C8027 0.1uF	PEG_R2D_N<3>	AK17	PEX_RX3_L	PEX_TX3_L AH18	PEG_D2R_C_N<3> C8062 0.1uF PEG_D2R_N<3>
PEG_R2D_C_P<4>	C8028 0.1uF	PEG_R2D_P<4>	AL17	PEX_RX4	PEX_TX4 AK18	PEG_D2R_C_P<4> C8063 0.1uF PEG_D2R_P<4>
PEG_R2D_C_N<4>	C8029 0.1uF	PEG_R2D_N<4>	AL18	PEX_RX4_L	PEX_TX4_L AJ18	PEG_D2R_C_N<4> C8064 0.1uF PEG_D2R_N<4>
PEG_R2D_C_P<5>	C8030 0.1uF	PEG_R2D_P<5>	AM18	PEX_RX5	PEX_TX5 AJ19	PEG_D2R_C_P<5> C8065 0.1uF PEG_D2R_P<5>
PEG_R2D_C_N<5>	C8031 0.1uF	PEG_R2D_N<5>	AM19	PEX_RX5_L	PEX_TX5_L AH19	PEG_D2R_C_N<5> C8066 0.1uF PEG_D2R_N<5>
PEG_R2D_C_P<6>	C8032 0.1uF	PEG_R2D_P<6>	AK19	PEX_RX6	PEX_TX6 AG20	PEG_D2R_C_P<6> C8067 0.1uF PEG_D2R_P<6>
PEG_R2D_C_N<6>	C8033 0.1uF	PEG_R2D_N<6>	AK20	PEX_RX6_L	PEX_TX6_L AH20	PEG_D2R_C_N<6> C8068 0.1uF PEG_D2R_N<6>
PEG_R2D_C_P<7>	C8034 0.1uF	PEG_R2D_P<7>	AL20	PEX_RX7	PEX_TX7 AG21	PEG_D2R_C_P<7> C8069 0.1uF PEG_D2R_P<7>
PEG_R2D_C_N<7>	C8035 0.1uF	PEG_R2D_N<7>	AL21	PEX_RX7_L	PEX_TX7_L AH21	PEG_D2R_C_N<7> C8070 0.1uF PEG_D2R_N<7>
PEG_R2D_C_P<8>	C8036 0.1uF	PEG_R2D_P<8>	AM21	PEX_RX8	PEX_TX8 AK21	PEG_D2R_C_P<8> C8071 0.1uF PEG_D2R_P<8>
PEG_R2D_C_N<8>	C8037 0.1uF	PEG_R2D_N<8>	AM22	PEX_RX8_L	PEX_TX8_L AJ21	PEG_D2R_C_N<8> C8072 0.1uF PEG_D2R_N<8>
PEG_R2D_C_P<9>	C8038 0.1uF	PEG_R2D_P<9>	AK22	PEX_RX9	PEX_TX9 AJ22	PEG_D2R_C_P<9> C8073 0.1uF PEG_D2R_P<9>
PEG_R2D_C_N<9>	C8039 0.1uF	PEG_R2D_N<9>	AK23	PEX_RX9_L	PEX_TX9_L AH22	PEG_D2R_C_N<9> C8074 0.1uF PEG_D2R_N<9>
PEG_R2D_C_P<10>	C8040 0.1uF	PEG_R2D_P<10>	AL23	PEX_RX10	PEX_TX10 AG23	PEG_D2R_C_P<10> C8075 0.1uF PEG_D2R_P<10>
PEG_R2D_C_N<10>	C8041 0.1uF	PEG_R2D_N<10>	AL24	PEX_RX10_L	PEX_TX10_L AH23	PEG_D2R_C_N<10> C8076 0.1uF PEG_D2R_N<10>
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PEG_R2D_C_N<11>	C8043 0.1uF	PEG_R2D_N<11>	AM25	PEX_RX11_L	PEX_TX11_L AJ24	PEG_D2R_C_N<11> C8078 0.1uF PEG_D2R_N<11>
PEG_R2D_C_P<12>	C8044 0.1uF	PEG_R2D_P<12>	AK25	PEX_RX12	PEX_TX12 AJ25	PEG_D2R_C_P<12> C8079 0.1uF PEG_D2R_P<12>
PEG_R2D_C_N<12>	C8045 0.1uF	PEG_R2D_N<12>	AK26	PEX_RX12_L	PEX_TX12_L AH25	PEG_D2R_C_N<12> C8080 0.1uF PEG_D2R_N<12>
PEG_R2D_C_P<13>	C8046 0.1uF	PEG_R2D_P<13>	AL26	PEX_RX13	PEX_TX13 AH26	PEG_D2R_C_P<13> C8081 0.1uF PEG_D2R_P<13>
PEG_R2D_C_N<13>	C8047 0.1uF	PEG_R2D_N<13>	AL27	PEX_RX13_L	PEX_TX13_L AG26	PEG_D2R_C_N<13> C8082 0.1uF PEG_D2R_N<13>
PEG_R2D_C_P<14>	C8048 0.1uF	PEG_R2D_P<14>	AM27	PEX_RX14	PEX_TX14 AK27	PEG_D2R_C_P<14> C8083 0.1uF PEG_D2R_P<14>
PEG_R2D_C_N<14>	C8049 0.1uF	PEG_R2D_N<14>	AM28	PEX_RX14_L	PEX_TX14_L AJ27	PEG_D2R_C_N<14> C8084 0.1uF PEG_D2R_N<14>
PEG_R2D_C_P<15>	C8050 0.1uF	PEG_R2D_P<15>	AL28	PEX_RX15	PEX_TX15 AJ28	PEG_D2R_C_P<15> C8085 0.1uF PEG_D2R_P<15>
PEG_R2D_C_N<15>	C8051 0.1uF	PEG_R2D_N<15>	AL29	PEX_RX15_L	PEX_TX15_L AH27	PEG_D2R_C_N<15> C8086 0.1uF PEG_D2R_N<15>
PEG_CLK100M_GPU_P			AH14	PEX_REFCLK	PEX_TSTCLK_OUT AM12	TP_GPU_PEXTSTCLK_P
PEG_CLK100M_GPU_N			AJ14	PEX_REFCLK_L	PEX_TSTCLK_OUT_L AM11	TP_GPU_PEXTSTCLK_N
GPU_RESET_L			AH15	PEX_RST_L		

All C_P/C_N caps: 0.1uF 10% 16V X5R 402

NV G84M PCI-E

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 67 OF 92	

Page Notes

Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PPVCORE_GPU

???A @ ???/???MHz Core/Mem Clk for VDD

C8100 1UF 20% 10V CERM 402
C8101 1UF 20% 10V CERM 402
C8102 1UF 20% 10V CERM 402
C8103 0.1UF 20% 10V CERM 402
C8104 0.1UF 20% 10V CERM 402
C8105 0.1UF 20% 10V CERM 402
C8106 0.1UF 20% 10V CERM 402
C8107 0.1UF 20% 10V CERM 402
C8108 0.1UF 20% 10V CERM 402
C8109 0.1UF 20% 10V CERM 402
C8110 0.1UF 20% 10V CERM 402
C8111 0.1UF 20% 10V CERM 402
C8112 0.1UF 20% 10V CERM 402
C8113 0.1UF 20% 10V CERM 402
C8114 0.1UF 20% 10V CERM 402
C8115 0.1UF 20% 10V CERM 402
C8116 0.1UF 20% 10V CERM 402
C8117 0.1UF 20% 10V CERM 402
C8118 0.1UF 20% 10V CERM 402
C8119 0.1UF 20% 10V CERM 402
C8120 0.1UF 20% 10V CERM 402
C8121 0.1UF 20% 10V CERM 402
C8122 0.1UF 20% 10V CERM 402

OMIT
U8000
NB8P-GS-W-A2
BGA
(7 OF 8)

K16 K17 N13 N14 N16 N17 N19 P13 P14 P16 P17 P19 R16 R17 T13 T14 T15 T18 T19 U13 U14 U15 U18 U19 V16 V17 W13 W14 W16 W17 W19 Y13 Y14 Y16 Y17 Y19 Y20 — VDD

P20 T20 T23 U20 U23 W20 — VDD_LP

GPU_VDD_SENSE — N20 VDD_SENSE
GPU_GND_SENSE — M21 GND_SENSE

A12 A18 A21 A24 A27 A3 A30 A6 A9 AA32 AD32 AG32 AK32 C32 F32 J32 M32 R32 — FBVDD

AA25 AA26 AB25 AB26 G11 G12 G15 G18 G21 G22 H11 H12 H15 H18 H21 H22 L25 L26 M25 M26 R25 R26 V25 V26 — FBVDDQ

AA23 AB23 H16 H17 J10 J23 J24 J9 K11 K12 K21 K22 K24 K9 L23 M23 T25 U25 — NC

FBVTT

PP1V8_S0GPU_ISNS

???A @ ???MHz 1.8V GDDR3

C8150 4.7UF 20% 6.3V CERM 603
C8151 4.7UF 20% 6.3V CERM 603
C8156 0.1UF 20% 10V CERM 402
C8157 0.1UF 20% 10V CERM 402
C8158 0.1UF 20% 10V CERM 402
C8159 0.1UF 20% 10V CERM 402
C8160 0.47UF 10% 6.3V CERM-X5R 402
C8161 0.47UF 10% 6.3V CERM-X5R 402
C8162 0.1UF 20% 10V CERM 402
C8163 0.1UF 20% 10V CERM 402
C8164 0.1UF 20% 10V CERM 402
C8165 0.1UF 20% 10V CERM 402
C8166 0.47UF 10% 6.3V CERM-X5R 402
C8167 0.47UF 10% 6.3V CERM-X5R 402
C8168 0.47UF 10% 6.3V CERM-X5R 402
C8169 0.47UF 10% 6.3V CERM-X5R 402
C8170 0.47UF 10% 6.3V CERM-X5R 402
C8171 0.47UF 10% 6.3V CERM-X5R 402

OMIT
U8000
NB8P-GS-W-A2
BGA
(8 OF 8)

AE17 AE27 AE6 AF11 AF26 AF29 AF4 AF7 AG10 AG11 AB27 AB6 AC10 AC23 AC29 AC4 AD16 AD17 AD2 AD31 AA12 AA2 AA21 AA31 AG13 AG14 AG15 AG19 AG2 AG22 AG31 AG8 AH24 AJ10 AJ13 AJ16 AJ17 AJ20 AJ23 AJ26 AJ29 AJ4 AJ7 AK2 AK28 AK31 AL10 AL11 AL14 AL19 AL22 AL25 AL3 AL6 AL9 AM10 AM13 AM16 AM17 AM20 AM23 AM26 AM29 B12 B15 B18 B21 B24 B27 B3 B30 B6 B9 C2 C31 D10 D13 — GND

D16 D17 D20 D23 D26 D29 D4 D7 F11 F14 F19 F2 F22 F25 F31 F8 G26 G29 G4 G7 H27 H6 J16 J17 J2 J31 K10 K23 K29 K4 L27 L6 M12 M2 M31 N15 N18 N29 N4 P15 P18 P27 P6 R13 R14 R15 R18 R19 R2 R20 R31 T16 T17 T24 T29 T4 U16 U17 U24 U29 U8 V13 V14 V15 V18 V19 V2 V20 V31 W15 W18 W27 W6 Y15 Y18 Y29 Y4 — GND

NV G84M Core/FB Power

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
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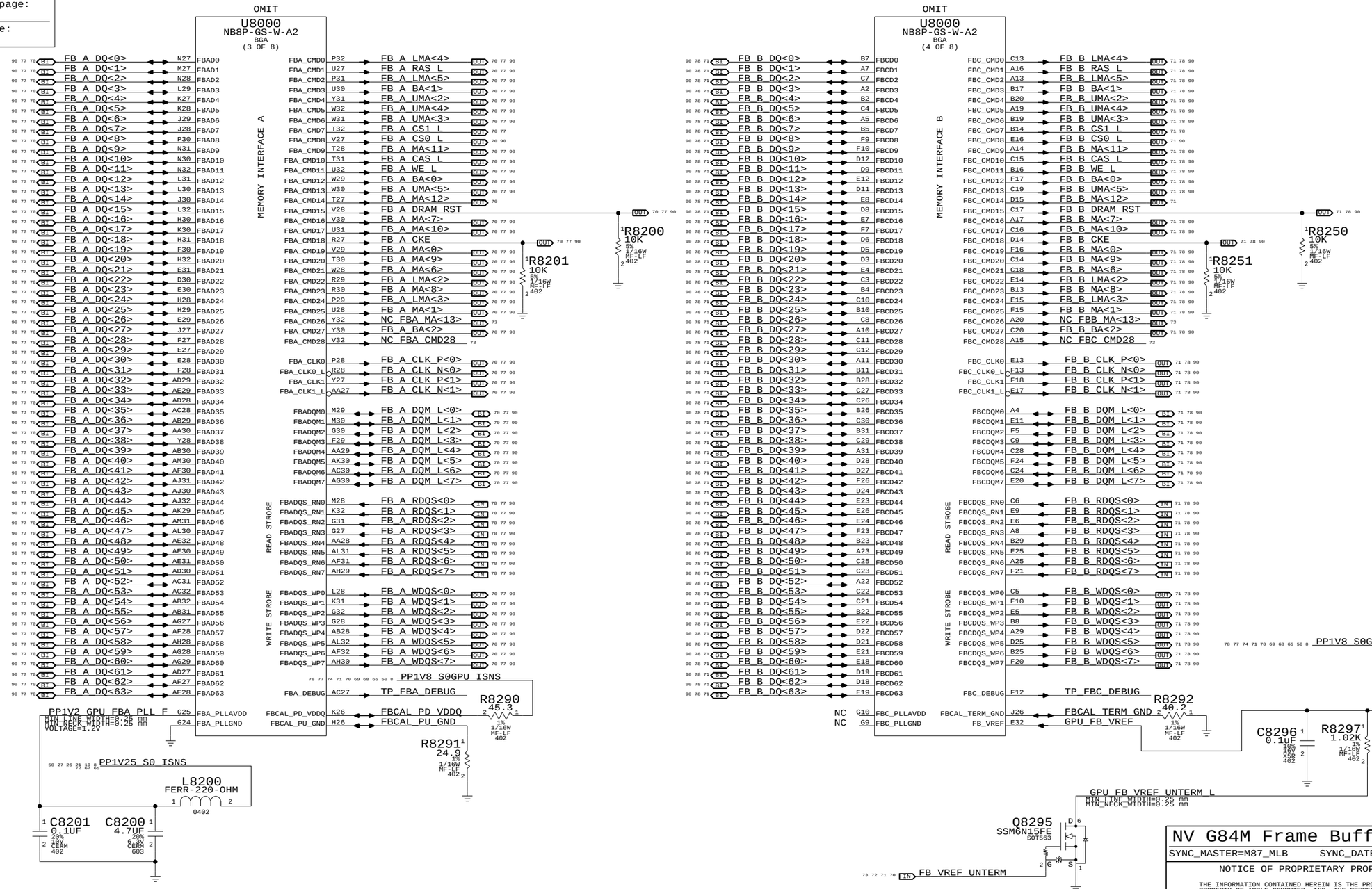
Page Notes

Power aliases required by this page:
- =PP1V2_GPU_FBPLLAVDD
- =PP1V8_GPU_FBIO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



NV G84M Frame Buffer I/F

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 69 OF 92	

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PP1V8_S0GPU_ISNS

CRITICAL
OMIT

U8400
FBGA
(2 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20

C8400 10UF 20% 6.3V X5R 603
C8401 C8402 C8403 C8404 0.1UF 10% 16V X5R 402

C8410 C8415 0.1UF 10% 16V X5R 402
U8400.J1 U8400.J12

Connect to designated pin, then GND

PP1V8_S0GPU_ISNS

C8420 10UF 20% 6.3V X5R 603
C8421 C8422 C8423 C8424 C8425 C8426 0.1UF 10% 16V X5R 402

R8430 2.37K 1% 1/16W MF-LF 402
R8433 2.37K 1% 1/16W MF-LF 402

FB_A0_VREF
FB_A2_VREF

R8431 5.49K 1% 1/16W MF-LF 402
R8432 2.21K 1% 1/16W MF-LF 402
C8431 0.01UF 10% 16V CERM 402
R8434 5.49K 1% 1/16W MF-LF 402
R8435 2.21K 1% 1/16W MF-LF 402
C8432 0.01UF 10% 16V CERM 402

FB_A2_VREF_UNTERM_L
FB_A0_VREF_UNTERM_L

FB_A_CLK0_TERM
VOLTAGE=0.9V

C8446 0.01UF 10% 16V CERM 402

FB_VREF_UNTERM

Q8400 SSM6N15FE SOT563

VRAM4
R8440 1K 1% 1/16W MF-LF 402
R8442 121 1% 1/16W MF-LF 402
R8444 121 1% 1/16W MF-LF 402
R8446 121 1% 1/16W MF-LF 402
R8447 121 1% 1/16W MF-LF 402

CRITICAL
OMIT

U8400
FBGA
(1 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20

FB_A_MA<0>
FB_A_MA<1>
FB_A_LMA<2>
FB_A_LMA<3>
FB_A_LMA<4>
FB_A_LMA<5>
FB_A_MA<6>
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FB_A_MA<10>
FB_A_MA<11>

FB_A_CKE
FB_A_CLK_P<0>
FB_A_CLK_N<0>
FB_A_CS0_L
FB_A_WE_L
FB_A_CAS_L
FB_A_RAS_L

FB_A0_ZQ
FB_A0_MF
FB_A0_SEN

FB_A_DRAM_RST

FB_A_RDQS<0>
FB_A_RDQS<1>
FB_A_RDQS<2>
FB_A_RDQS<3>

FB_A_WDQS<0>
FB_A_WDQS<1>
FB_A_WDQS<2>
FB_A_WDQS<3>

FB_A_BA<0>
FB_A_BA<1>
FB_A_BA<2>

FB_A_MA<12>
FB_A_CS1_L
(For 32Mx32 support)

R8448 243 1% 1/16W MF-LF 402
R8449 100 1% 1/16W MF-LF 402

FB_A_DQM_L<0>
FB_A_DQM_L<1>
FB_A_DQM_L<2>
FB_A_DQM_L<3>

FB_A_DQ<1>
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FB_A_DQ<2>
FB_A_DQ<0>
FB_A_DQ<5>
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FB_A_DQ<26>
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FB_A_DQ<30>

PP1V8_S0GPU_ISNS

CRITICAL
OMIT

U8450
FBGA
(2 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20

C8450 10UF 20% 6.3V X5R 603
C8451 C8452 C8453 C8454 0.1UF 10% 16V X5R 402

C8460 C8465 0.1UF 10% 16V X5R 402
U8400.J1 U8400.J12

Connect to designated pin, then GND

PP1V8_S0GPU_ISNS

C8470 10UF 20% 6.3V X5R 603
C8471 C8472 C8473 C8474 C8475 C8476 0.1UF 10% 16V X5R 402

R8480 2.37K 1% 1/16W MF-LF 402
R8483 2.37K 1% 1/16W MF-LF 402

FB_A1_VREF
FB_A3_VREF

R8481 5.49K 1% 1/16W MF-LF 402
R8482 2.21K 1% 1/16W MF-LF 402
C8481 0.01UF 10% 16V CERM 402
R8484 5.49K 1% 1/16W MF-LF 402
R8485 2.21K 1% 1/16W MF-LF 402
C8482 0.01UF 10% 16V CERM 402

FB_A3_VREF_UNTERM_L
FB_A1_VREF_UNTERM_L

FB_A_CLK1_TERM
VOLTAGE=0.9V

C8496 0.01UF 10% 16V CERM 402

FB_VREF_UNTERM

Q8450 SSM6N15FE SOT563

VRAM4
R8490 1K 1% 1/16W MF-LF 402
R8492 121 1% 1/16W MF-LF 402
R8494 121 1% 1/16W MF-LF 402
R8496 121 1% 1/16W MF-LF 402
R8497 121 1% 1/16W MF-LF 402

CRITICAL
OMIT

U8450
FBGA
(1 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20

FB_A_MA<0>
FB_A_MA<1>
FB_A_UMA<2>
FB_A_UMA<3>
FB_A_UMA<4>
FB_A_UMA<5>
FB_A_MA<6>
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FB_A_MA<10>
FB_A_MA<11>

FB_A_CKE
FB_A_CLK_P<1>
FB_A_CLK_N<1>
FB_A_CS0_L
FB_A_WE_L
FB_A_CAS_L
FB_A_RAS_L

FB_A1_ZQ
FB_A1_MF
FB_A1_SEN

FB_A_DRAM_RST

FB_A_RDQS<7>
FB_A_RDQS<5>
FB_A_RDQS<6>
FB_A_RDQS<4>

FB_A_WDQS<7>
FB_A_WDQS<5>
FB_A_WDQS<6>
FB_A_WDQS<4>

FB_A_BA<0>
FB_A_BA<1>
FB_A_BA<2>

FB_A_MA<12>
FB_A_CS1_L
(For 32Mx32 support)

R8498 243 1% 1/16W MF-LF 402
R8499 100 1% 1/16W MF-LF 402

FB_A_DQM_L<7>
FB_A_DQM_L<5>
FB_A_DQM_L<6>
FB_A_DQM_L<4>

FB_A_DQ<62>
FB_A_DQ<56>
FB_A_DQ<58>
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FB_A_DQ<38>

GDDR3 Frame Buffer A (Top)

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 70 OF 92	

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PP1V8_S0GPU_ISNS

C8500 10UF 20% 6.3V X5R 603 | C8501 0.1UF 10% 16V X5R 402 | C8502 0.1UF | C8503 0.1UF | C8504 0.1UF

C8510 0.1UF 10% 16V X5R 402 — U8500.J1 | C8515 0.1UF — U8500.J12

Connect to designated pin, then GND

PP1V8_S0GPU_ISNS

C8520 10UF 20% 6.3V X5R 603 | C8521 0.1UF 10% 16V X5R 402 | C8522 0.1UF | C8523 0.1UF | C8524 0.1UF | C8525 0.1UF | C8526 0.1UF

R8530 2.37K 1% 1/16W MF-LF 402 — R8533 2.37K 1% 1/16W MF-LF 402

R8531 5.49K 1% 1/16W MF-LF 402 | R8532 2.21K 1% 1/16W MF-LF 402 | C8531 0.01UF 10% 16V CERM 402 | R8534 5.49K 1% 1/16W MF-LF 402 | R8535 2.21K 1% 1/16W MF-LF 402 | C8532 0.01UF 10% 16V CERM 402

FB_B0_VREF — FB_B2_VREF

FB_B2_VREF_UNTERM_L
FB_B0_VREF_UNTERM_L

FB_B_CLK0_TERM
VOLTAGE=0.9V

C8546 0.01UF 10% 16V CERM 402 — FB_VREF_UNTERM

Q8500 SSM6N15FE SOT563 | Q8500 SSM6N15FE SOT563

R8540 1K 1% 1/16W MF-LF 402 | R8542 121 1% 1/16W MF-LF 402 | R8544 121 1% 1/16W MF-LF 402 | R8546 121 1% 1/16W MF-LF 402 | R8547 121 1% 1/16W MF-LF 402

VRAM4 R8543 121 1% 1/16W MF-LF 402 | VRAM4 R8545 121 1% 1/16W MF-LF 402

CRITICAL
OMIT

U8500 FBGA (2 OF 2) 16MX32-GDDR3-500MHZ-BC20 K4J52324QC-BC20

FB_B_MA<0>
FB_B_MA<1>
FB_B_LMA<2>
FB_B_LMA<3>
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FB_B_MA<7>
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FB_B_MA<10>
FB_B_MA<11>

FB_B_CKE
FB_B_CLK_P<0>
FB_B_CLK_N<0>
FB_B_CS0_L
FB_B_WE_L
FB_B_CAS_L
FB_B_RAS_L

FB_B0_ZQ
FB_B0_MF
FB_B0_SEN

FB_B_DRAM_RST

FB_B_RDQS<2>
FB_B_RDQS<1>
FB_B_RDQS<3>
FB_B_RDQS<0>

FB_B_WDQS<2>
FB_B_WDQS<1>
FB_B_WDQS<3>
FB_B_WDQS<0>

FB_B_BA<0>
FB_B_BA<1>
FB_B_BA<2>

FB_B_MA<12>
FB_B_CS1_L
(For 32Mx32 support)

FB_B_DQM_L<2>
FB_B_DQM_L<1>
FB_B_DQM_L<3>
FB_B_DQM_L<0>

FB_B_DQ<18>
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FB_B_DQ<11>
FB_B_DQ<24>
FB_B_DQ<28>
FB_B_DQ<29>
FB_B_DQ<31>
FB_B_DQ<30>
FB_B_DQ<25>
FB_B_DQ<26>
FB_B_DQ<27>
FB_B_DQ<2>
FB_B_DQ<1>
FB_B_DQ<6>
FB_B_DQ<0>
FB_B_DQ<7>
FB_B_DQ<4>
FB_B_DQ<5>
FB_B_DQ<3>

R8548 243 1% 1/16W MF-LF 402 | R8549 100 1% 1/16W MF-LF 402

PP1V8_S0GPU_ISNS

C8550 10UF 20% 6.3V X5R 603 | C8551 0.1UF 10% 16V X5R 402 | C8552 0.1UF | C8553 0.1UF | C8554 0.1UF

C8560 0.1UF 10% 16V X5R 402 — U8500.J1 | C8565 0.1UF — U8500.J12

Connect to designated pin, then GND

PP1V8_S0GPU_ISNS

C8570 10UF 20% 6.3V X5R 603 | C8571 0.1UF 10% 16V X5R 402 | C8572 0.1UF | C8573 0.1UF | C8574 0.1UF | C8575 0.1UF | C8576 0.1UF

R8580 2.37K 1% 1/16W MF-LF 402 — R8583 2.37K 1% 1/16W MF-LF 402

R8581 5.49K 1% 1/16W MF-LF 402 | R8582 2.21K 1% 1/16W MF-LF 402 | C8581 0.01UF 10% 16V CERM 402 | R8584 5.49K 1% 1/16W MF-LF 402 | R8585 2.21K 1% 1/16W MF-LF 402 | C8582 0.01UF 10% 16V CERM 402

FB_B1_VREF — FB_B3_VREF

FB_B3_VREF_UNTERM_L
FB_B1_VREF_UNTERM_L

FB_B_CLK1_TERM
VOLTAGE=0.9V

C8596 0.01UF 10% 16V CERM 402 — FB_VREF_UNTERM

Q8550 SSM6N15FE SOT563 | Q8550 SSM6N15FE SOT563

R8590 1K 1% 1/16W MF-LF 402 | R8592 121 1% 1/16W MF-LF 402 | R8594 121 1% 1/16W MF-LF 402 | R8596 121 1% 1/16W MF-LF 402 | R8597 121 1% 1/16W MF-LF 402

VRAM4 R8593 121 1% 1/16W MF-LF 402 | VRAM4 R8595 121 1% 1/16W MF-LF 402

CRITICAL
OMIT

U8550 FBGA (1 OF 2) 16MX32-GDDR3-500MHZ-BC20 K4J52324QC-BC20

FB_B_MA<0>
FB_B_MA<1>
FB_B_UMA<2>
FB_B_UMA<3>
FB_B_UMA<4>
FB_B_UMA<5>
FB_B_MA<6>
FB_B_MA<7>
FB_B_MA<8>
FB_B_MA<9>
FB_B_MA<10>
FB_B_MA<11>

FB_B_CKE
FB_B_CLK_P<1>
FB_B_CLK_N<1>
FB_B_CS0_L
FB_B_WE_L
FB_B_CAS_L
FB_B_RAS_L

FB_B1_ZQ
FB_B1_MF
FB_B1_SEN

FB_B_DRAM_RST

FB_B_RDQS<6>
FB_B_RDQS<5>
FB_B_RDQS<4>
FB_B_RDQS<7>

FB_B_WDQS<6>
FB_B_WDQS<5>
FB_B_WDQS<4>
FB_B_WDQS<7>

FB_B_BA<0>
FB_B_BA<1>
FB_B_BA<2>

FB_B_MA<12>
FB_B_CS1_L
(For 32Mx32 support)

FB_B_DQM_L<6>
FB_B_DQM_L<5>
FB_B_DQM_L<4>
FB_B_DQM_L<7>

FB_B_DQ<49>
FB_B_DQ<50>
FB_B_DQ<48>
FB_B_DQ<51>
FB_B_DQ<52>
FB_B_DQ<55>
FB_B_DQ<54>
FB_B_DQ<53>
FB_B_DQ<40>
FB_B_DQ<42>
FB_B_DQ<41>
FB_B_DQ<45>
FB_B_DQ<43>
FB_B_DQ<46>
FB_B_DQ<47>
FB_B_DQ<44>
FB_B_DQ<36>
FB_B_DQ<39>
FB_B_DQ<37>
FB_B_DQ<38>
FB_B_DQ<34>
FB_B_DQ<32>
FB_B_DQ<35>
FB_B_DQ<33>
FB_B_DQ<63>
FB_B_DQ<58>
FB_B_DQ<61>
FB_B_DQ<59>
FB_B_DQ<62>
FB_B_DQ<56>
FB_B_DQ<60>
FB_B_DQ<57>

R8598 243 1% 1/16W MF-LF 402 | R8599 100 1% 1/16W MF-LF 402

GDDR3 Frame Buffer B (Top)

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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Page Notes

Power aliases required by this page:
- =PP3V3_GPU_VDD33
- =PP3V3_GPI_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

OMIT
U8000
NB8P-GS-W-A2
BGA
(6 OF 8)

PP3V3_S0GPU
Typically <??mA
C8600 0.47UF 10% 6.3V CERM-X5R 402
C8601 0.47UF 10% 6.3V CERM-X5R 402
C8602 0.47UF 10% 6.3V CERM-X5R 402

AC11 VDD33_1
AC12 VDD33_2
AC24 VDD33_3
AD24 VDD33_4
AE11 VDD33_5
AE12 VDD33_6
H7 VDD33_7
J7 VDD33_8
K7 VDD33_9
L10 VDD33_10
L7 VDD33_11
L8 VDD33_12
M10 VDD33_13

GPIO0 K3 GPU_HPD
GPIO1 H1 NC_GPU_GPIO_1
GPIO2 K5 GPU_BL_PWM
GPIO3 G5 GPU_PANEL_EN
GPIO4 E2 GPU_BKLT_EN
GPIO5 J5 TP_GPU_GSTATE<0>
GPIO6 G6 GPU_GPIO_6
GPIO7 K6 GPU_VGA_EN_L
GPIO8 E1 NC_GPU_GPIO_8
GPIO9 D2 NC_GPU_GPIO_9
GPIO10 H5 FB_VREF_UNTERM
GPIO11 F4 GPU_VCORE_VID0
GPIO12 E3 GPU_VCORE_VID1
GPIO13 U3 GPU_VCORE_VID2
GPIO14 U4 GPU_VCORE_VID3

NC_GPU_ROM_CS_L AA4 ROMCS_L
NC_GPU_ROM_SCLK AA7 ROM_SCLK
NC_GPU_ROM_SI W2 ROM_SI
NC_GPU_ROM_SO AA6 ROM_SO

R8695 100K 5% 1/16W MF-LF 402
R8696 10K 5% 1/16W MF-LF 402

GPU_TESTMODE_PD H2 TESTMODE
GPU_SWAPRDY_A M6 SWAPRDY_A

SPDIF J6 NC_GPU_SPDIF
STEREO T3 NC_GPU_STEREO
BUFRST_L F3 TP_GPU_BUFRST_L

JTAG_TCK AJ11 TP_GPU_JTAG_TCK
JTAG_TDI AK12 TP_GPU_JTAG_TDI
JTAG_TDO AL12 TP_GPU_JTAG_TDO
JTAG_TMS AK11 TP_GPU_JTAG_TMS
(IPD) JTAG_TRST_L AL13 TP_GPU_JTAG_TRST_L

PP3V3_S0GPU
R8620 49.9 1% 1/10W MF-LF 402
R8621 49.9 1% 1/16W MF-LF 402
GPU_MIOA_PD_VDDQ
GPU_MIOB_PD_VDDQ
GPU_MIOA_PU_GND
GPU_MIOB_PU_GND
R8622 49.9 1% 1/10W MF-LF 402
R8623 49.9 1% 1/16W MF-LF 402

R8616 10K 5% 1/16W MF-LF 402
R8618 10K 5% 1/16W MF-LF 402
R8617 10K 5% 1/16W MF-LF 402
R8619 10K 5% 1/16W MF-LF 402
C8610 1UF 10% 6.3V CERM 402
C8611 1UF 10% 6.3V CERM 402
C8617 0.1UF 10% 16V X5R 402
C8619 0.1UF 10% 16V X5R 402

M7 MIOA_VDDQ_1
M8 MIOA_VDDQ_2
R8 MIOA_VDDQ_3
T8 MIOA_VDDQ_4
U9 MIOA_VDDQ_5
AA8 MIOB_VDDQ_1
AB7 MIOB_VDDQ_2
AB8 MIOB_VDDQ_3
AC6 MIOB_VDDQ_4
AC7 MIOB_VDDQ_5

GPU_MIOA_VREF L2 MIOA_VREF
GPU_MIOB_VREF Y2 MIOB_VREF
GPU_MIOA_PD_VDDQ L1 MIOACAL_PD_VDDQ
GPU_MIOA_PU_GND L3 MIOACAL_PU_GND
GPU_MIOB_PD_VDDQ Y1 MIOBCAL_PD_VDDQ
GPU_MIOB_PU_GND Y3 MIOBCAL_PU_GND

MIOA_CLKOUT R4 TP_GPU_MIOA_CLKOUT_P
MIOA_CLKOUT_L P4 TP_GPU_MIOA_CLKOUT_N
MIOA_CTL3 P3 TP_GPU_MIOA_CTL3
MIOA_DE P1 TP_GPU_MIOA_DE
MIOAD0 P2 GPU_MIOA_D<0>
MIOAD1 N2 GPU_MIOA_D<1>
MIOAD2 N1 GPU_MIOA_D<2>
MIOAD3 N3 GPU_MIOA_D<3>
MIOAD4 M1 GPU_MIOA_D<4>
MIOAD5 M3 GPU_MIOA_D<5>
MIOAD6 P5 GPU_MIOA_D<6>
MIOAD7 N6 TP_GPU_MIOA_D<7>
MIOAD8 N5 GPU_MIOA_D<8>
MIOAD9 M4 GPU_MIOA_D<9>
MIOAD10 L4 GPU_MIOA_D<10>
MIOAD11 L5 GPU_MIOA_D<11>
MIOA_HSYNC R3 TP_GPU_MIOA_HSYNC
MIOA_VSYNC R1 TP_GPU_MIOA_VSYNC

MIOB_CLKIN AE4 TP_GPU_MIOB_CLKIN
MIOB_CLKOUT AD4 TP_GPU_MIOB_CLKOUT_P
MIOB_CLKOUT_L AD5 TP_GPU_MIOB_CLKOUT_N
MIOB_CTL3 AD3 TP_GPU_MIOB_CTL3
MIOB_DE AD1 TP_GPU_MIOB_DE
MIOBD0 AC3 GPU_MIOB_D<0>
MIOBD1 AC1 GPU_MIOB_D<1>
MIOBD2 AC2 TP_GPU_MIOB_D<2>
MIOBD3 AB2 GPU_MIOB_D<3>
MIOBD4 AB1 GPU_MIOB_D<4>
MIOBD5 AA1 GPU_MIOB_D<5>
MIOBD6 AB3 GPU_MIOB_D<6>
MIOBD7 AA3 GPU_MIOB_D<7>
MIOBD8 AC5 GPU_MIOB_D<8>
MIOBD9 AB5 GPU_MIOB_D<9>
MIOBD10 AB4 GPU_MIOB_D<10>
MIOBD11 AA5 GPU_MIOB_D<11>
MIOB_HSYNC AF3 GPU_MIOB_HSYNC
MIOB_VSYNC AE3 TP_GPU_MIOB_VSYNC

THERMDP K1 GPU_TDIODE_P
THERMDN J1 GPU_TDIODE_N

PP1V25_S0_ISNS
L8630 FERR-220-OHM 0402
PP1V2_GPU_PLLVDD_F MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V 40mA
C8633 4.7UF 20% 6.3V CERM 603
C8630 4.7UF 20% 6.3V CERM 603
C8631 0.1UF 10% 16V X5R 402

T9 PLLVDD
U10 PLLGND
G23 H_PLLVDD
T10 VID_PLLVDD

L8635 FERR-220-OHM 0402
PP1V2_GPU_H_PLLVDD_F MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V 40mA
C8637 4.7UF 20% 6.3V CERM 603
C8635 4.7UF 20% 6.3V CERM 603
C8636 0.1UF 10% 16V X5R 402

L8640 FERR-220-OHM 0402
PP1V25_S0_ISNS
PP1V2_GPU_VID_PLLVDD_F MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V 40mA
C8643 4.7UF 20% 6.3V CERM 603
C8640 4.7UF 20% 6.3V CERM 603
C8641 0.1UF 10% 16V X5R 402

90 73 30 GPU_CLK27M U1 XTALIN
73 NC_GPU_XTALOUT U2 XTALOUT
73 GPU_XTALOUTBUFF T2 XTALOUTBUFF
90 73 30 GPU_CLK27M_SS T1 XTALSSIN

NV G84M GPIO/MIO/Misc

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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GPIOs

	Native Func		
GPU_HPD	HPD0	GPU_HPD	IN
NC_GPU_GPIO_1	HPD1	NC_GPU_GPIO_1	
GPU_BL_PWM	LCD0_BL_PWM	GPU_BL_PWM	OUT
GPU_PANEL_EN	LCD0_VDD	GPU_PANEL_EN	OUT
GPU_BKLT_EN	LCD0_BL_EN	GPU_BKLT_EN	OUT
TP_GPU_GSTATE<0>	VID0	TP_GPU_GSTATE<0>	
GPU_GPIO_6	VID1	TP_GPU_GSTATE<1>	
GPU_VGA_EN_L	MEM_VID	GPU_VGA_EN_L	
NC_GPU_GPIO_8	THERM	NC_GPU_GPIO_8	
NC_GPU_GPIO_9	FAN_PWM	NC_GPU_GPIO_9	
FB_VREF_UNTERM	MEM_VREF	FB_VREF_UNTERM	OUT
GPU_VCORE_VID0	SLI_SYNC	GPU_VCORE_VID0	OUT
GPU_VCORE_VID1	AC_DET	GPU_VCORE_VID1	OUT
GPU_VCORE_VID2	PWR_CTL0	GPU_VCORE_VID2	OUT
GPU_VCORE_VID3	PWR_CTL1	GPU_VCORE_VID3	OUT

Config Straps

PP3V3_S0GPU

	VRAM_SAMSUNG	VRAM_8M	VRAM8	NO STUFF	NO STUFF	NO STUFF	NO STUFF
	R8720 10K	R8722 10K	R8724 10K	R8726 10K	R8728 2.2K	R8729 2.2K	R8730 2.2K	R8731 2.2K	R8732 2.2K
Supported straps:									
RAMCFG0	GPU_MIOB_D<0>								
RAMCFG1		GPU_MIOB_D<1>							
RAMCFG2			GPU_MIOB_D<8>						
RAMCFG3				GPU_MIOB_D<9>					
3GIO_PADCFG0					GPU_MIOA_D<6>				
3GIO_PADCFG1						GPU_MIOA_D<8>			
3GIO_PADCFG2							GPU_MIOA_D<9>		
3GIO_PADCFG3								GPU_MIOB_HSYNC	
PEX_PLL_EN_TERM									GPU_MIOA_D<0>
SUBVENDOR (BIOS ROM PRESENT)									GPU_MIOA_D<1>

	VRAM_HYNIX	NO STUFF	VRAM_16M	VRAM4	
	R8721 10K	R8723 10K	R8725 10K	R8727 10K	R8733 2.2K
PCI_DEVID<3..0>					

PP3V3_S0GPU

	NO STUFF			
	R8734 2.2K	R8735 2.2K	R8736 2.2K	R8737 2.2K
PCI_DEVID3	GPU_MIOB_D<11>			
PCI_DEVID2		GPU_MIOB_D<3>		
PCI_DEVID1			GPU_MIOB_D<5>	
PCI_DEVID0				GPU_MIOB_D<4>

Straps not supported:

USER<3..0>	MIOA_D<5..2>
ROMTYPE<1..0>	MIOB_VSYNC, MIOB_D<10>
SLOT_CLOCK_CFG	MIOA_HSYNC
PCI_IOBAR	MIOB_D<7>
BAR2_SIZE	MIOB_DE
PCI_DEVID<4>	MIOB_CTL3

Analog Video Mux

PP3V3_S0GPU

C8700 0.1UF 20% 10V CERM 402

U8700 QFN TS3V340 (VCC, THRML PAD, GND)

GPU_VGA_R	S1A	DA	GPU_TV_C_VGA_R
GPU_VGA_G	S2A	DB	GPU_TV_Y_VGA_G
GPU_VGA_B	S1B	DC	GPU_TV_COMP_VGA_B
	S2B	DD	NC
GPU_TV_C	S1C	IN	GPU_VGA_EN_L
GPU_TV_Y	S2C	EN_L	
GPU_TV_COMP	S1D		
	S2D		

Place Rs near GPU: R8740 150 1%, R8741 150 1%, R8742 150 1%, R8743 150 1%, R8744 150 1%, R8745 150 1% (1/10W MF-LF 402)

R8700 10K 5% 1/16W MF-LF 402

Renamed signals

GPU_CLK27M	GPU_CLK27M
GPU_CLK27M_SS	GPU_CLK27M_SS
GPU_TDIODE_P	GPU_TDIODE_P
GPU_TDIODE_N	GPU_TDIODE_N
GPU_DVI_DDC_CLK	GPU_DVI_DDC_CLK
GPU_DVI_DDC_DATA	GPU_DVI_DDC_DATA
GPU_PANEL_DDC_CLK	GPU_PANEL_DDC_CLK
GPU_PANEL_DDC_DATA	GPU_PANEL_DDC_DATA
GPU_VDD_SENSE	GPU_VDD_SENSE
GPU_GND_SENSE	GPU_GND_SENSE

(all MAKE_BASE=TRUE)

Unused I2C Buses

NC_GPU_I2CA_SCL	NC_GPU_I2CA_SCL
NC_GPU_I2CA_SDA	NC_GPU_I2CA_SDA

(MAKE_BASE=TRUE, NO_TEST=TRUE)

I2CS ties into SMBus connection page
(I2CS requires pullups even if not used)

HDCP Support

PP3V3_S0GPU

HDCP C8770 0.1UF 20% 10V CERM 402

CRITICAL HDCP U8770 190-00001-0001 SOI (VCC, SCL, SDA, NC, NC, NC, GND)

HDCP R8770 10K 5% 1/16W MF-LF 402

HDCP R8771 10K 5% 1/16W MF-LF 402

GPU_I2CH_SCL (BI), GPU_I2CH_SDA (BI)

TMDS Backdrive Protection

PP3V3_S0GPU

CRITICAL Q8790 SI2305DS SOT-23 (D, G, S)

PP3V3_S0GPU_TMDS

R8790 10K 5% 1/16W MF-LF 402

GPU_TMDS_PWREN_L

Q8791 SSM6N15FE SOT563

PM_GPUVCORE_EN (IN)

R8791 100K 5% 1/10W MF-LF 402

Unused signals

NC_GPU_XTALOUT	NC_GPU_XTALOUT
NC_GPU_SPDIF	NC_GPU_SPDIF
NC_GPU_STEREO	NC_GPU_STEREO
NC_FBA_MA<13>	NC_FBA_MA<13>
NC_FBB_MA<13>	NC_FBB_MA<13>
NC_FBA_CMD28	NC_FBA_CMD28
NC_FBC_CMD28	NC_FBC_CMD28
NC_GPU_ROM_CS_L	NC_GPU_ROM_CS_L
NC_GPU_ROM_SCLK	NC_GPU_ROM_SCLK
NC_GPU_ROM_SI	NC_GPU_ROM_SI
NC_GPU_ROM_SO	NC_GPU_ROM_SO
NC_GPU_CSYNC	NC_GPU_CSYNC
NC_GPU_R2	NC_GPU_R2
NC_GPU_G2	NC_GPU_G2
NC_GPU_B2	NC_GPU_B2
NC_GPU_H2SYNC	NC_GPU_H2SYNC
NC_GPU_V2SYNC	NC_GPU_V2SYNC
NC_LVDS_U_DATAP<3>	NC_LVDS_U_DATAP<3>
NC_LVDS_U_DATAN<3>	NC_LVDS_U_DATAN<3>
NC_LVDS_L_DATAP<3>	NC_LVDS_L_DATAP<3>
NC_LVDS_L_DATAN<3>	NC_LVDS_L_DATAN<3>
TP_GPU_MIOA_CLKOUT_P	TP_GPU_MIOA_CLKOUT_P
TP_GPU_MIOA_CLKOUT_N	TP_GPU_MIOA_CLKOUT_N
TP_GPU_MIOA_CTL3	TP_GPU_MIOA_CTL3
TP_GPU_MIOA_DE	TP_GPU_MIOA_DE
TP_GPU_MIOA_D<5..2>	GPU_MIOA_D<5..2>
TP_GPU_MIOA_D<7>	TP_GPU_MIOA_D<7>
TP_GPU_MIOA_D<11..10>	GPU_MIOA_D<11..10>
TP_GPU_MIOA_HSYNC	TP_GPU_MIOA_HSYNC
TP_GPU_MIOA_VSYNC	TP_GPU_MIOA_VSYNC
TP_GPU_MIOB_CLKIN	TP_GPU_MIOB_CLKIN
TP_GPU_MIOB_CLKOUT_P	TP_GPU_MIOB_CLKOUT_P
TP_GPU_MIOB_CLKOUT_N	TP_GPU_MIOB_CLKOUT_N
TP_GPU_MIOB_CTL3	TP_GPU_MIOB_CTL3
TP_GPU_MIOB_DE	TP_GPU_MIOB_DE
TP_GPU_MIOB_D<2>	TP_GPU_MIOB_D<2>
TP_GPU_MIOB_D<7..6>	GPU_MIOB_D<7..6>
TP_GPU_MIOB_D<10>	GPU_MIOB_D<10>
TP_GPU_MIOB_VSYNC	TP_GPU_MIOB_VSYNC
NC_GPU_IFPD_CLK_P	NC_GPU_IFPD_CLK_P
NC_GPU_IFPD_CLK_N	NC_GPU_IFPD_CLK_N

(MAKE_BASE=TRUE, NO_TEST=TRUE)

Unused Clocks

GPU_CLK27M_SS
GPU_XTALOUTBUFF

R8780 10K 5% 1/16W MF-LF 402

GPU_SS_INT

R8781 10K 5% 1/16W MF-LF 402

GPU Straps

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

APPLE INC.

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Power aliases required by this page:
- =PP1V8_GPU_IFPX
- =PP3V3_GPU_IFPCD_IOVDD
- =PP3V3_GPU_DAC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Sum of peak currents: 240mA

PP1V8_S0GPU_ISNS

L8800 FERR-220-OHM 0402
C8800 4.7UF 20% 6.3V CERM 603
C8801 0.1UF 20% 10V CERM 402
C8803 0.1UF 20% 10V CERM 402
20mA peak per diff pair
160mA peak for all pairs
Place at AF9
Place at AF8

PP1V8_GPU_IFPAB_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

L8805 FERR-220-OHM 0402
C8805 4.7UF 20% 6.3V CERM 603
C8806 0.1UF 20% 10V CERM 402
40mA peak

PP1V8_GPU_IFPAB_PLLVDD_F
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

GPU_IFPAB_VPROBE
GPU_IFPAB_RSET

PP3V3_S0GPU_TMDS

L8810 FERR-220-OHM 0402
C8810 4.7UF 20% 6.3V CERM 603
C8811 0.1UF 20% 10V CERM 402
C8813 0.1UF 20% 10V CERM 402
20mA peak per diff pair
200mA peak for all pairs
Place at AD6
Place at AE7

PP3V3_GPU_IFPCD_IOVDD_F
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

L8815 FERR-220-OHM 0402
C8815 4.7UF 20% 6.3V CERM 603
C8816 0.1UF 20% 10V CERM 402
40mA peak

PP1V8_GPU_IFPCD_PLLVDD_F
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V

GPU_IFPCD_VPROBE
GPU_IFPCD_RSET

Sum of peak currents: 390mA

PP3V3_S0GPU

L8820 FERR-220-OHM 0402
C8820 4.7UF 20% 6.3V CERM 603
C8821 0.1UF 20% 10V CERM 402
120mA peak

PP3V3_GPU_DACA_VDD_F
MIN_LINE_WIDTH=0.35 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

GPU_DACA_VREF
GPU_DACA_RSET

L8830 FERR-220-OHM 0402
C8830 4.7UF 20% 6.3V CERM 603
C8831 0.1UF 20% 10V CERM 402
150mA peak

PP3V3_GPU_DACB_VDD_F
MIN_LINE_WIDTH=0.35 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

GPU_DACB_VREF
GPU_DACB_RSET

NO STUFF
L8840 FERR-220-OHM 0402
C8845 4.7UF 20% 6.3V CERM 603
C8840 4.7UF 20% 6.3V CERM 603
C8841 0.1UF 20% 10V CERM 402
120mA peak

PP3V3_GPU_DACC_VDD_F
MIN_LINE_WIDTH=0.35 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

GPU_DACC_VREF
GPU_DACC_RSET

GPU_PANEL_DDC_CLK
GPU_PANEL_DDC_DATA
GPU_I2CH_SCL
GPU_I2CH_SDA
SMBUS_SMC_0_S0_SCL
SMBUS_SMC_0_S0_SDA

I2CS must be pulled up if not used
I2CS addr fixed at 0x9E,0x9F

OMIT
U8000
NB8P-GS-W-A2
BGA
(5 OF 8)

AF9	IFPA_IOVDD	IFPA_TXC	AK9
AF8	IFPB_IOVDD	IFPA_TXC_L	AJ9
AC9	IFPAB_PLLVDD	IFPA_TXD0	AH6
AD9	IFPAB_PLLGND	IFPA_TXD0_L	AJ6
AM4	IFPAB_VPROBE	IFPA_TXD1	AH8
AL5	IFPAB_RSET	IFPA_TXD1_L	AH7
AD6	IFPC_IOVDD	IFPA_TXD2	AJ8
AE7	IFPD_IOVDD	IFPA_TXD2_L	AK8
AA10	IFPCD_PLLVDD	IFPA_TXD3	AJ5
AB10	IFPCD_PLLGND	IFPA_TXD3_L	AH5
AK3	IFPCD_VPROBE	IFPB_TXC	AK4
AH3	IFPCD_RSET	IFPB_TXC_L	AL4
AD10	DACA_VDD	IFPB_TXD4	AM6
AG9	DACA_IDUMP	IFPB_TXD4_L	AM5
AH10	DACA_VREF	IFPB_TXD5	AM7
AH9	DACA_RSET	IFPB_TXD5_L	AL7
V8	DACB_VDD	IFPB_TXD6	AK6
V7	DACB_IDUMP	IFPB_TXD6_L	AK5
R5	DACB_VREF	IFPB_TXD7	AK7
R7	DACB_RSET	IFPB_TXD7_L	AL8
AD7	DACC_VDD	IFPC_TXC	AM2
AG4	DACC_IDUMP	IFPC_TXC_L	AM3
AH4	DACC_VREF	IFPC_TXD0	AE2
AF5	DACC_RSET	IFPC_TXD0_L	AE1
G2	I2CC_SCL	IFPC_TXD1	AF1
G1	I2CC_SDA	IFPC_TXD1_L	AF2
G3	I2CH_SCL	IFPC_TXD2	AG1
H3	I2CH_SDA	IFPC_TXD2_L	AH1
C1	I2CS_SCL	IFPD_TXC	AG3
B1	I2CS_SDA	IFPD_TXC_L	AH2
		IFPD_TXD4	AK1
		IFPD_TXD4_L	AJ1
		IFPD_TXD5	AL2
		IFPD_TXD5_L	AL1
		IFPD_TXD6	AJ2
		IFPD_TXD6_L	AJ3
		DACA_RED	AH11
		DACA_GREEN	AJ12
		DACA_BLUE	AH12
		DACA_HSYNC	AF10
		DACA_VSYNC	AK10
		DACB_RED	R6
		DACB_GREEN	T5
		DACB_BLUE	T6
		DACB_CSYNC	U5
		DACC_RED	AF6
		DACC_GREEN	AG6
		DACC_BLUE	AE5
		DACC_HSYNC	AG7
		DACC_VSYNC	AG5
		I2CA_SCL	K2
		I2CA_SDA	J3
		I2CB_SCL	H4
		I2CB_SDA	J4

LVDS_L_CLK_P
LVDS_L_CLK_N
LVDS_L_DATA_P<0>
LVDS_L_DATA_N<0>
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TMDS_DATA_N<0>
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GPU_VGA_R
GPU_VGA_G
GPU_VGA_B
GPU_VGA_HSYNC
GPU_VGA_VSYNC
GPU_TV_C
GPU_TV_Y
GPU_TV_COMP
NC_GPU_CSYNC
NC_GPU_R2
NC_GPU_G2
NC_GPU_B2
NC_GPU_H2SYNC
NC_GPU_V2SYNC
NC_GPU_I2CA_SCL
NC_GPU_I2CA_SDA
GPU_DVI_DDC_CLK
GPU_DVI_DDC_DATA

Composite/S-Video	VGA	Component
C	R	Pr
Y	G	Y
Comp	B	Pb

GPU_IFPAB_RSET
GPU_IFPCD_RSET
GPU_DACA_RSET
GPU_DACB_RSET
GPU_DACC_RSET

NO STUFF R8850 1K 1% 1/16W ME-LF 402
NO STUFF R8851 1K 1% 1/16W ME-LF 402
R8852 124 1% 1/16W ME-LF 402
R8853 124 1% 1/16W ME-LF 402
R8854 124 1% 1/16W ME-LF 402

GPU_DACA_VREF
GPU_DACB_VREF
GPU_DACC_VREF

C8852 0.1UF 20% 10V CERM 402
C8853 0.1UF 20% 10V CERM 402
C8854 0.1UF 20% 10V CERM 402

GPU_IFPAB_VPROBE
GPU_IFPCD_VPROBE

NO STUFF C8855 0.01UF 20% 16V CERM 402
NO STUFF C8856 0.01UF 20% 16V CERM 402

NV G84M Video Interfaces

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

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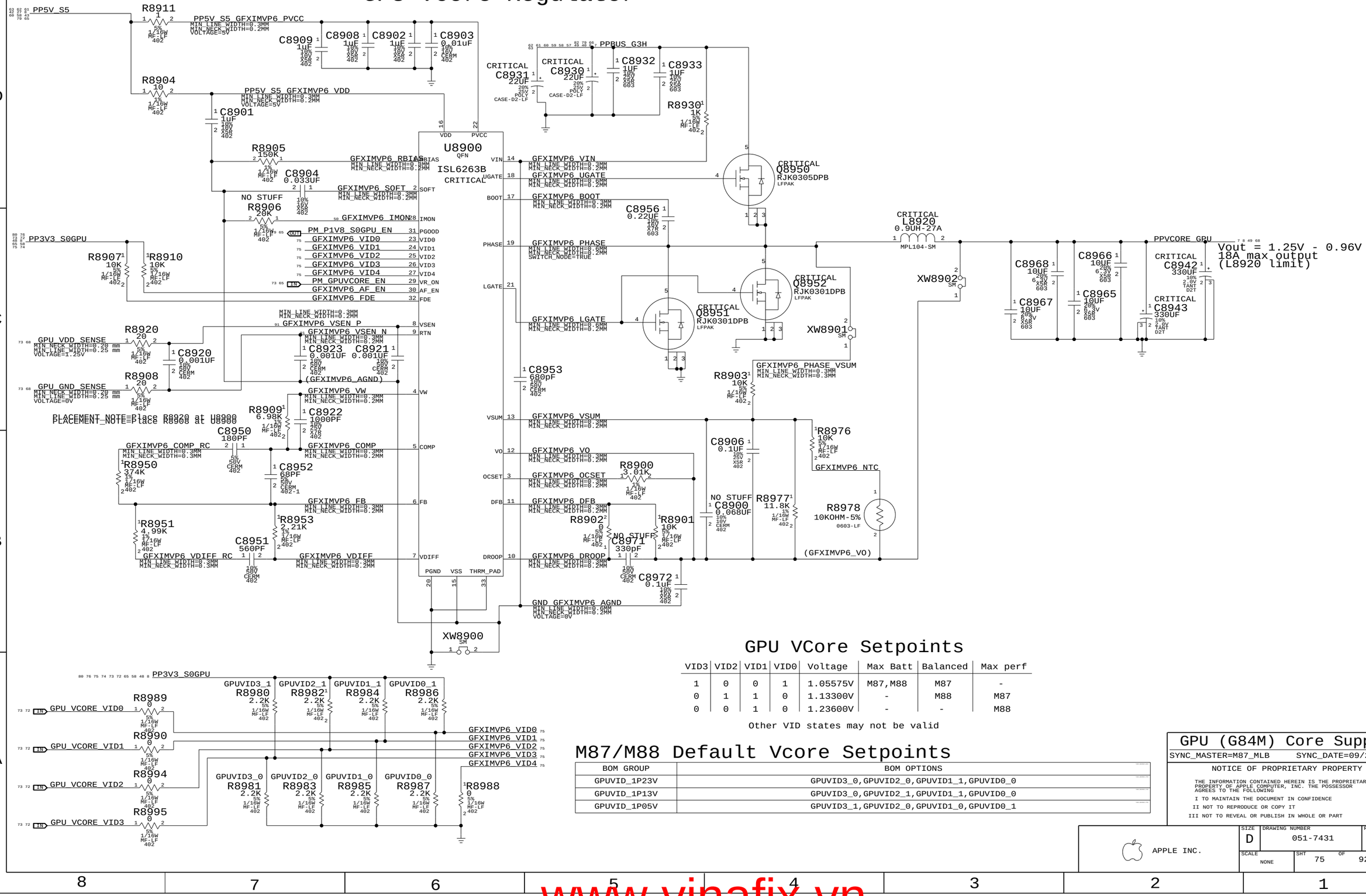
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 74 OF 92	

GPU VCore Regulator



GPU VCore Setpoints

VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	0	0	1	1.05575V	M87,M88	M87	-
0	1	1	0	1.13300V	-	M88	M87
0	0	1	0	1.23600V	-	-	M88

Other VID states may not be valid

M87/M88 Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_1P23V	GPUVID3_0,GPUVID2_0,GPUVID1_1,GPUVID0_0
GPUVID_1P13V	GPUVID3_0,GPUVID2_1,GPUVID1_1,GPUVID0_0
GPUVID_1P05V	GPUVID3_1,GPUVID2_0,GPUVID1_0,GPUVID0_1

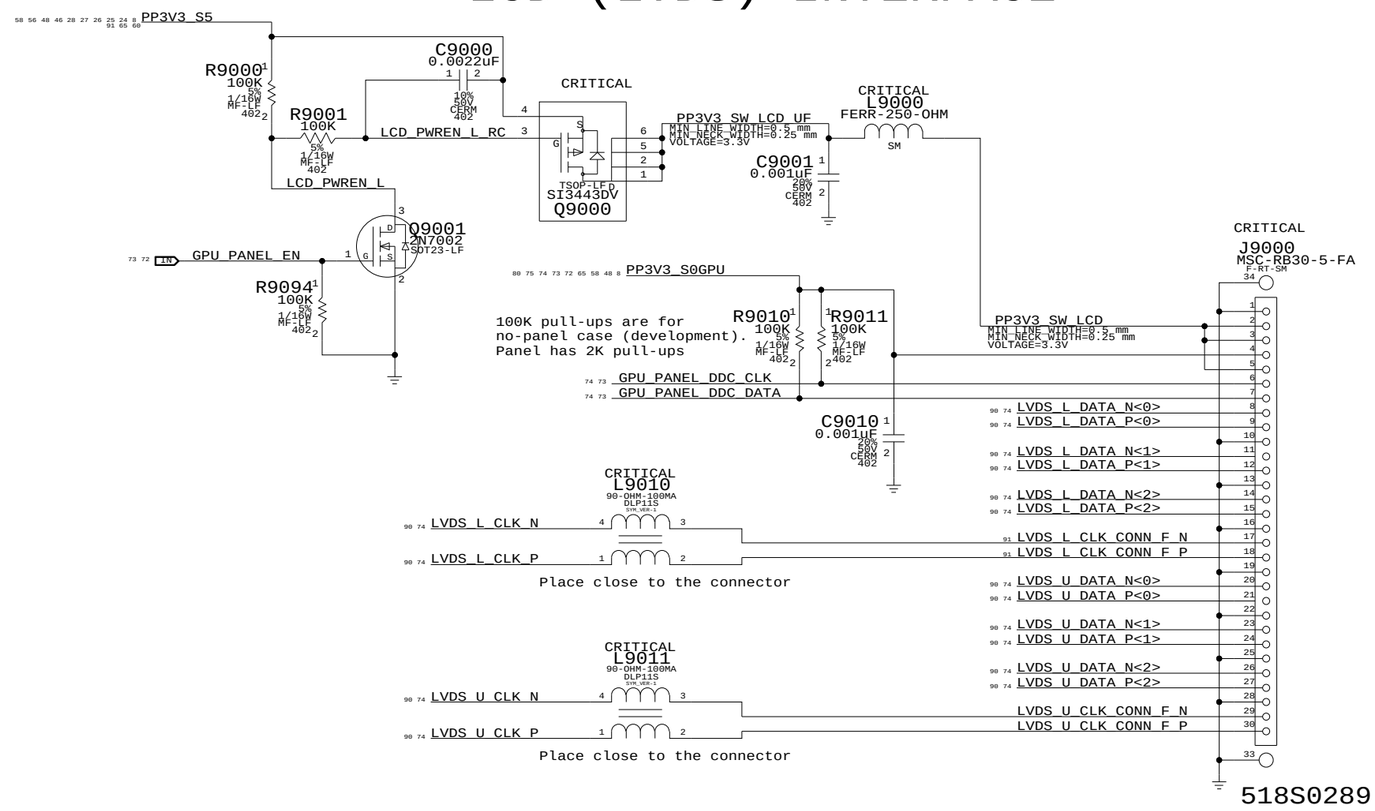
GPU (G84M) Core Supply

SYNC_MASTER=M87_MLB SYNC_DATE=09/26/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 75 OF 92	

LCD (LVDS) INTERFACE



LVDS Display Connector

SYNC_MASTER=MASTER SYNC_DATE=MASTER

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 76 OF 92	

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

CRITICAL
OMIT

U9100
FBGA
(2 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20

U9150
FBGA
(2 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20

PP1V8_S0GPU_ISNS

Connect to designated pin, then GND

U8400.J1
U8400.J12

VRAM8
C9100 10UF 20% 6.3V X5R 603
C9101 0.1UF 10% 16V X5R 402
C9102 0.1UF 10% 16V X5R 402
C9103 0.1UF 10% 16V X5R 402
C9104 0.1UF 10% 16V X5R 402
C9110 0.1UF 10% 16V X5R 402
C9115 0.1UF 10% 16V X5R 402
C9120 10UF 20% 6.3V X5R 603
C9121 0.1UF 10% 16V X5R 402
C9122 0.1UF 10% 16V X5R 402
C9123 0.1UF 10% 16V X5R 402
C9124 0.1UF 10% 16V X5R 402
C9125 0.1UF 10% 16V X5R 402
C9126 0.1UF 10% 16V X5R 402
C9150 10UF 20% 6.3V X5R 603
C9151 0.1UF 10% 16V X5R 402
C9152 0.1UF 10% 16V X5R 402
C9153 0.1UF 10% 16V X5R 402
C9154 0.1UF 10% 16V X5R 402
C9160 0.1UF 10% 16V X5R 402
C9165 0.1UF 10% 16V X5R 402
C9170 10UF 20% 6.3V X5R 603
C9171 0.1UF 10% 16V X5R 402
C9172 0.1UF 10% 16V X5R 402
C9173 0.1UF 10% 16V X5R 402
C9174 0.1UF 10% 16V X5R 402
C9175 0.1UF 10% 16V X5R 402
C9176 0.1UF 10% 16V X5R 402

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FB_A2_VREF
FB_A0_VREF
FB_A3_VREF
FB_A1_VREF

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FB_A_WE_L
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FB_A2_ZQ
FB_A2_MF
FB_A2_SEN
FB_A3_ZQ
FB_A3_MF
FB_A3_SEN

VRAM8
R9140 1K 5% 1/16W MF-LF 402
R9148 243 1% 1/16W MF-LF 402
R9149 100 5% 1/16W MF-LF 402
R9190 1K 5% 1/16W MF-LF 402
R9198 243 1% 1/16W MF-LF 402
R9199 100 5% 1/16W MF-LF 402

NC
NC

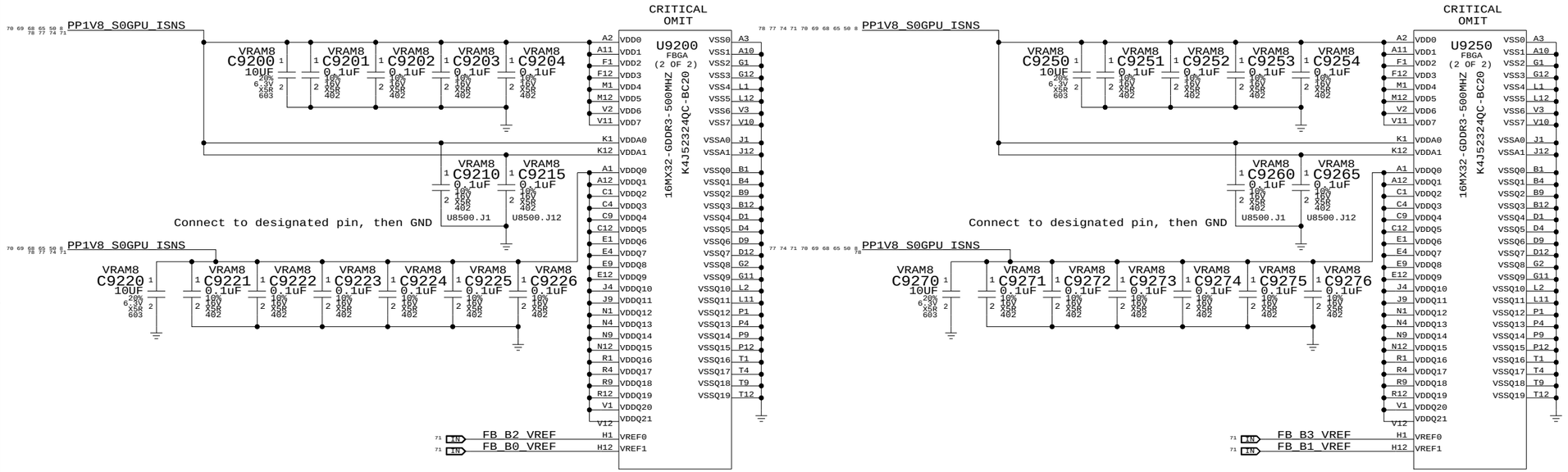
MFLOW

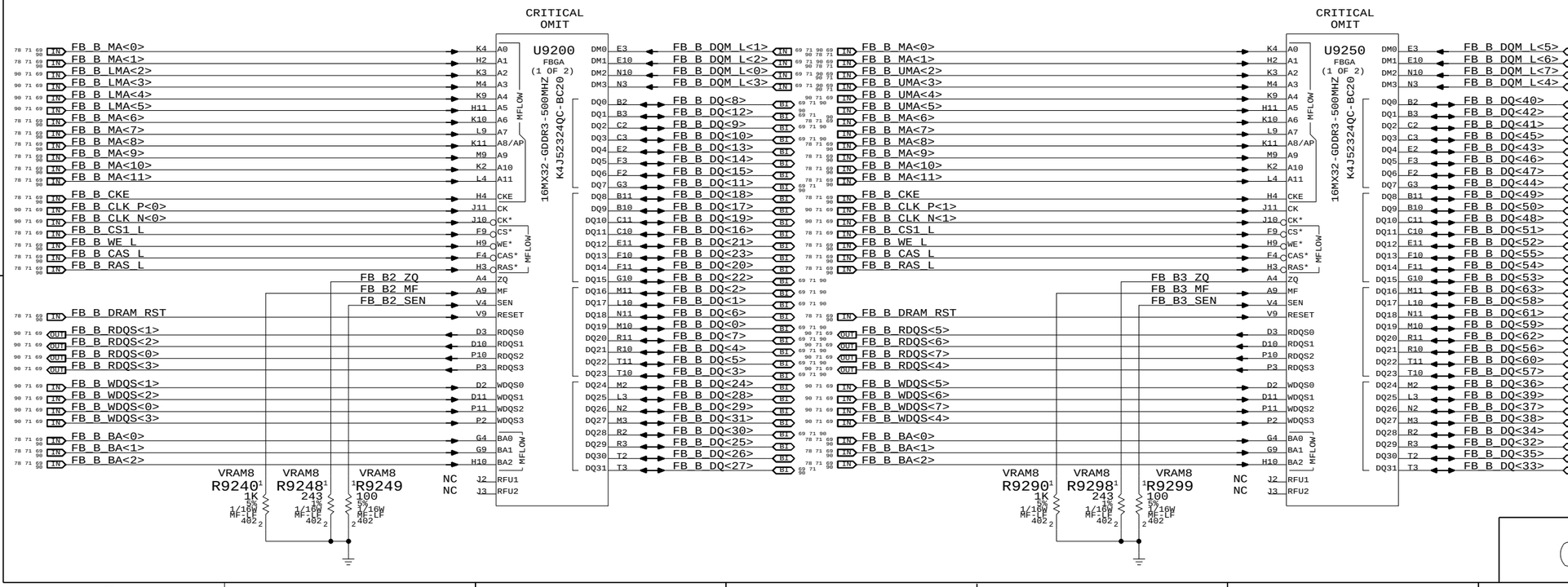
GDDR3 Frame Buffer A (Bot)

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 77 OF 92	





Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

GDDR3 Frame Buffer B (Bot)

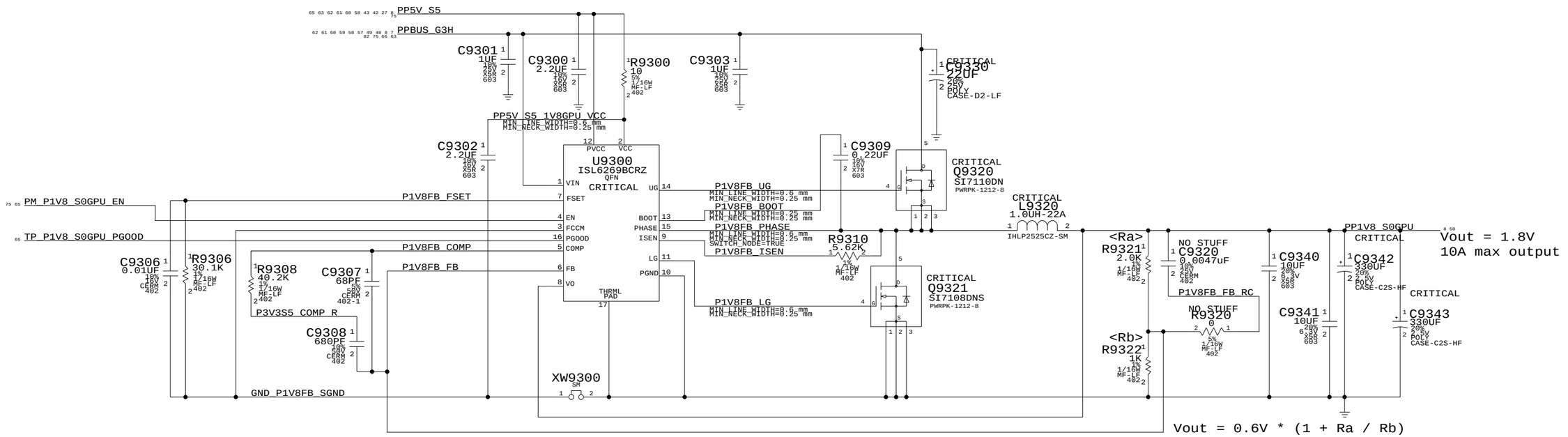
SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0

SCALE: NONE SHT 78 OF 92

1.8V Frame Buffer Regulator



1.8V FB Power Supply

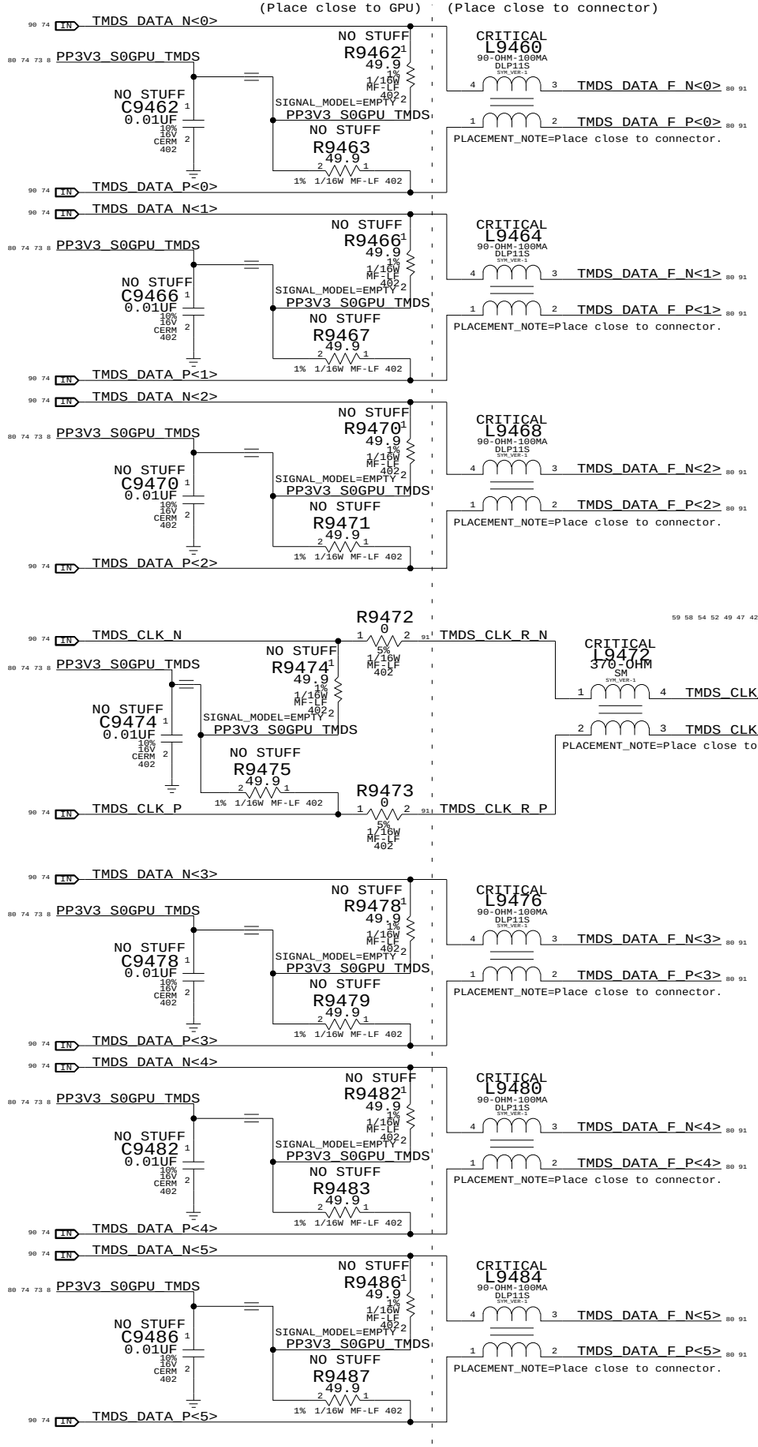
SYNC_MASTER=MASTER SYNC_DATE=MASTER

APPLE INC.

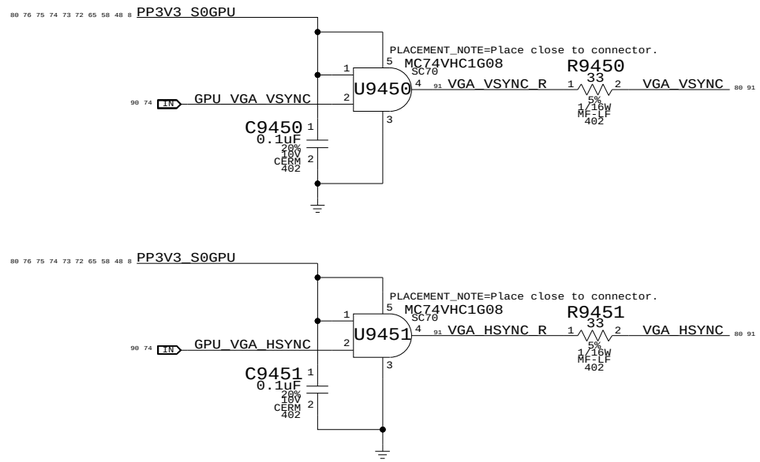
SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 79 OF 92	

TMDS Filtering

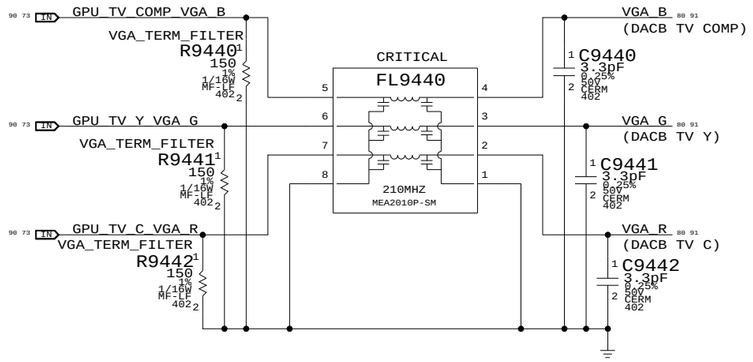
(Place close to GPU) (Place close to connector)



VGA SYNC Buffers



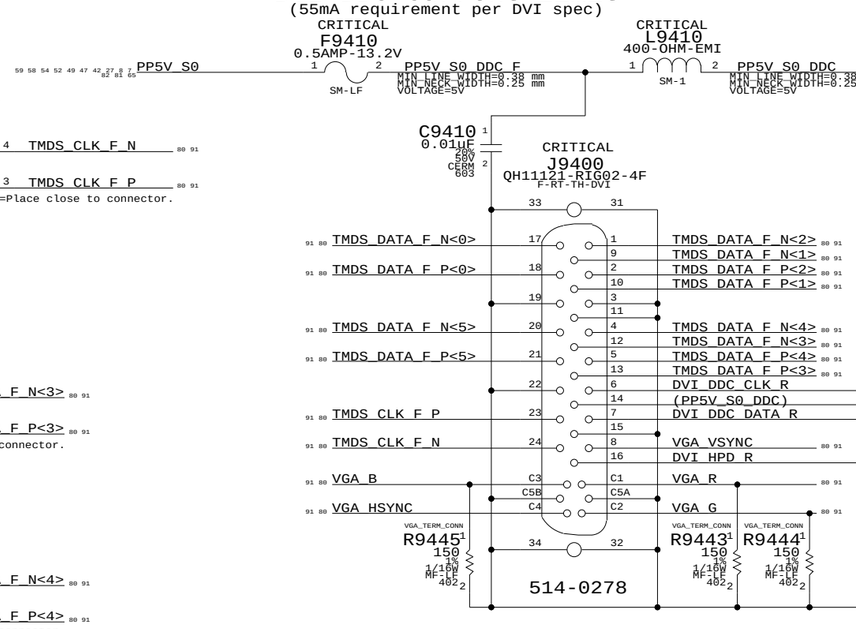
ANALOG FILTERING
PLACE CLOSE TO CONNECTOR



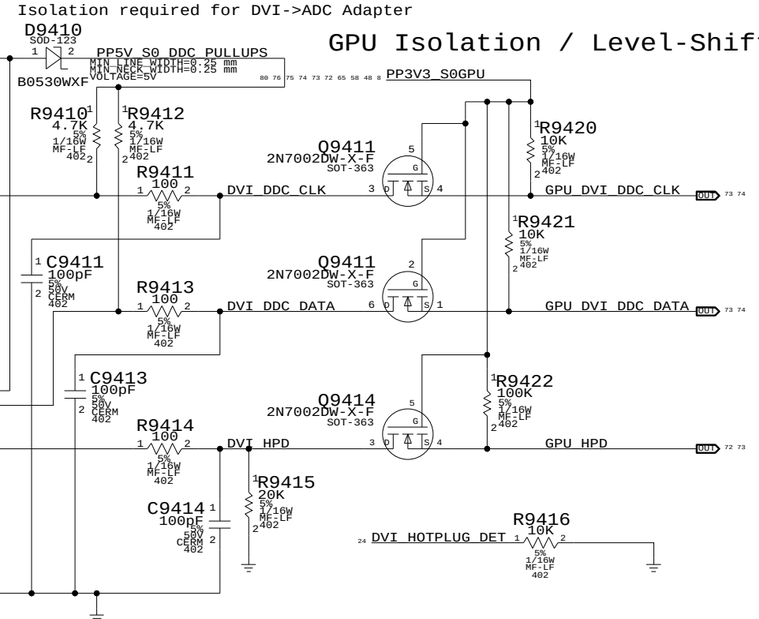
DVI INTERFACE

DVI DDC Current Limit

(55mA requirement per DVI spec)



Isolation required for DVI->ADC Adapter



GPU Isolation / Level-Shift

DVI Display Connector

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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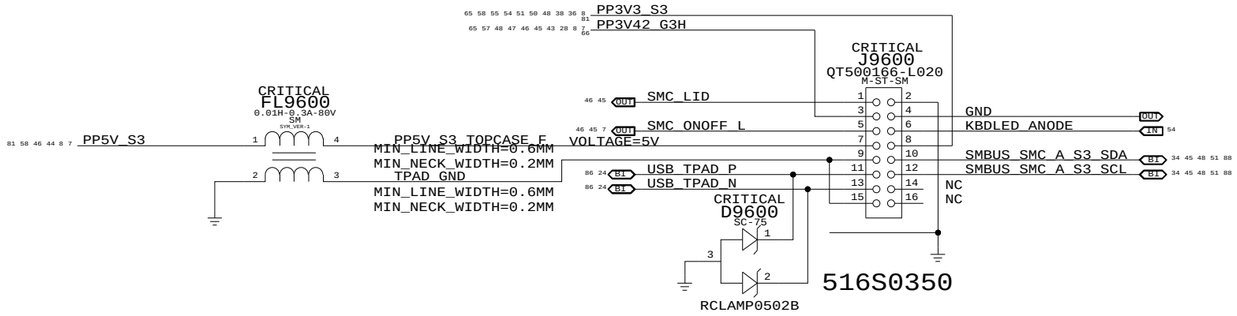
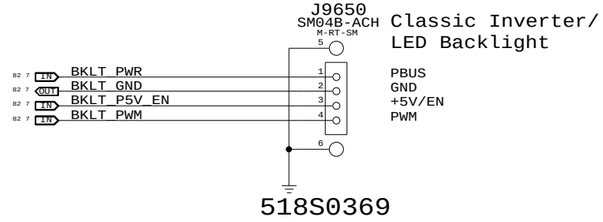
	D	051-7431	A.0.0
	SCALE: NONE	SHT 80 OF 92	

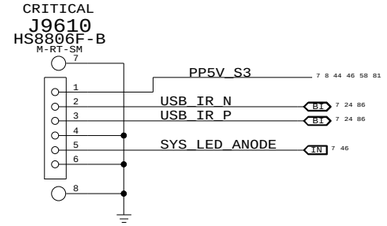
Top-Case Connector



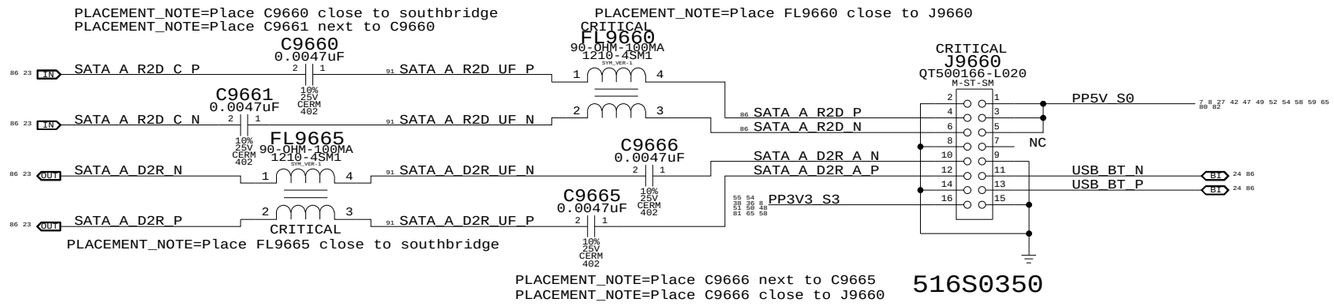
Backlight Connector



IR & Sleep LED Connector



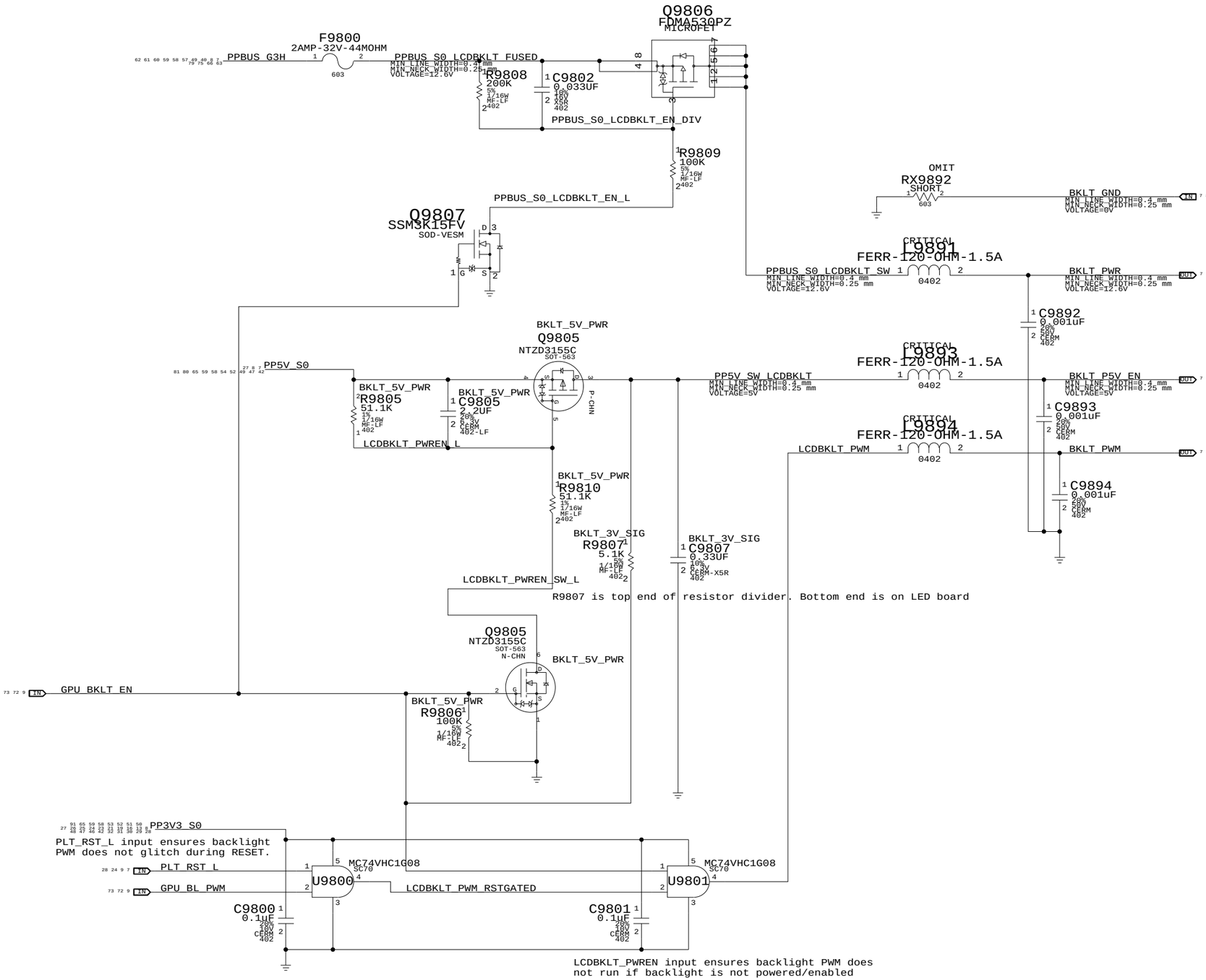
Bluetooth (M13P) & SATA HDD Flex Connector



Project Specific Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7431	A.0.0
	SCALE: NONE	SHT 81 OF 92	



LCD Backlight Support

SYNC_MASTER=M87_LIO SYNC_DATE=12/06/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 82 OF 92	

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	?
FSB_ADDR2ADDR	*	=2:1_SPACING	?
FSB_ADSTB	*	=3:1_SPACING	?
FSB_ADDR2ADSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=3:1_SPACING	?
FSB_DATA2DATA	*	=2:1_SPACING	?
FSB_DSTB	*	=3:1_SPACING	?
FSB_DATA2DSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2TO1	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_ADS_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BNR_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BPRI_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BREQ0_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DBSY_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DEFER_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DPWR_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DRDY_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_HIT_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_HITM_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_LOCK_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_TRDY_L	10 14
FSB_CPURST_L	FSB_55S	FSB_COMMON	FSB_CPURST_L	7 10 13 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_D_L<15..0>	7 10 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_DINV_L<0>	7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<0>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<0>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_D_L<31..16>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_DINV_L<1>	7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<1>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<1>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_D_L<47..32>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_DINV_L<2>	7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<2>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<2>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_D_L<63..48>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_DINV_L<3>	7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<3>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_A_L<16..3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	7 10 14
FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<0>	7 10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB_A_L<35..17>	7 10 14
FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<1>	7 10 14
CPU_IERR_L	CPU_55S		CPU_IERR_L	10
CPU_FERR_L	CPU_55S		CPU_FERR_L	10 23
CPU_PROCHOT_L	CPU_55S	CPU_2TO1	CPU_PROCHOT_L	10 46 59
CPU_PWRGD	CPU_55S		CPU_PWRGD	7 10 13 23
CPU_FROM_SB	CPU_55S		CPU_INTR	10 23
CPU_FROM_SB	CPU_55S		CPU_NMI	10 23
CPU_FROM_SB	CPU_55S		CPU_A20M_L	10 23
CPU_FROM_SB	CPU_55S		CPU_DPSLP_L	7 10 23
CPU_FROM_SB	CPU_55S		CPU_IGNNE_L	10 23
CPU_INIT_L	CPU_55S		CPU_INIT_L	10 23 47
CPU_FROM_SB	CPU_55S		CPU_SMI_L	10 23
CPU_FROM_SB	CPU_55S		CPU_STPCLK_L	7 10 23
PM_THRMTRIP_L	CPU_55S	CPU_2TO1	PM_THRMTRIP_L	10 16 23 46
FSB_CPUSLP_L	CPU_55S		FSB_CPUSLP_L	7 10 14
PM_DPRSLPVR	CPU_55S	CPU_2TO1	PM_DPRSLPVR	7 16 25 59
(See above)	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	7 59
CPU_BSEL0	CPU_55S	CPU_2TO1	CPU_BSEL<0>	10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<0>	13 16 30
CPU_BSEL1	CPU_55S	CPU_2TO1	CPU_BSEL<1>	10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<1>	13 16 30
CPU_BSEL2	CPU_55S	CPU_2TO1	CPU_BSEL<2>	10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<2>	13 16 30
CPU_DPRSTP_L	CPU_55S	CPU_2TO1	CPU_DPRSTP_L	7 10 16 23 59
CPU_GTLREF	CPU_55S	CPU_GTLREF	CPU_GTLREF	10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<3>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<1>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	10
XDP_TDI	CPU_55S	CPU_ITP	XDP_TDI	10 13
XDP_TDO	CPU_55S	CPU_ITP	XDP_TDO	10 13
XDP_TMS	CPU_55S	CPU_ITP	XDP_TMS	10 13
XDP_TCK	CPU_55S	CPU_ITP	XDP_TCK	10 13
XDP_TRST_L	CPU_55S	CPU_ITP	XDP_TRST_L	10 13
XDP_BPM_L	CPU_55S	CPU_ITP	XDP_BPM_L<4..0>	10 13
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP_BPM_L<5>	10 13
	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	13 29 30 88
	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	13 29 30 88
(FSB_CPURST_L)	CPU_55S	CPU_ITP	XDP_CPURST_L	13
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	11 12
	CPU_55S	CPU_2TO1	IMVP6_VID<6..0>	7 12 59
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11 59
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11 59
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	59
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	59

CPU/FSB Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0

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PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
DMI	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CRT_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	
LVDS	*	20 MIL	?	
CRT	*	25 MIL	?	DG Says 40 mil spacing minimum
CRT_2CRT	*	20 MIL	?	
CRT_SYNC	*	25 MIL	?	DG Says 30 mil spacing minimum
CRT_SYNC2SYNC	*	20 MIL	?	
TVDAC	*	25 MIL	?	DG Says 40 mil spacing minimum
TVDAC_2TVDAC	*	20 MIL	?	

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT
CRT_SYNC	CRT_SYNC	*	CRT_SYNC2SYNC
TVDAC	TVDAC	*	TVDAC_2TVDAC

LVDS signals are 100-ohm +/- 20% differential impedence.
CRT & TVDAC signal single-ended impedence varies by location:
- 37.5-ohm +/- 15% from GMCH to first termination resistor.
- 50-ohm +/- 15% from first to second termination resistor.
- 55-ohm +/- 15% from second termination resistor to connector.

CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedence.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PEG_R2D	PCIE_100D	PCIE	PEG_R2D_P<15..0>	67
	PCIE_100D	PCIE	PEG_R2D_N<15..0>	67
	PCIE_100D	PCIE	PEG_R2D_C_P<15..0>	15 67
	PCIE_100D	PCIE	PEG_R2D_C_N<15..0>	15 67
PEG_D2R	PCIE_100D	PCIE	PEG_D2R_P<15..0>	15 67
	PCIE_100D	PCIE	PEG_D2R_N<15..0>	15 67
	PCIE_100D	PCIE	PEG_D2R_C_P<15..0>	67
	PCIE_100D	PCIE	PEG_D2R_C_N<15..0>	67
DMI_N2S	DMI_100D	DMI	DMI_N2S_P<3..0>	16 24
	DMI_100D	DMI	DMI_N2S_N<3..0>	16 24
DMI_S2N	DMI_100D	DMI	DMI_S2N_P<3..0>	16 24
	DMI_100D	DMI	DMI_S2N_N<3..0>	16 24
LVDS_A_CLK	LVDS_100D	LVDS	NC_LVDS_A_CLKP	15 22
LVDS_A_CLK	LVDS_100D	LVDS	NC_LVDS_A_CLKN	15 22
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_P<2..0>	15 22
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_N<2..0>	15 22
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS_A_DATA_P<3>	
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS_A_DATA_N<3>	
LVDS_B_CLK	LVDS_100D	LVDS	NC_LVDS_B_CLKP	15 22
LVDS_B_CLK	LVDS_100D	LVDS	NC_LVDS_B_CLKN	15 22
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_P<2..0>	15 22
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_N<2..0>	15 22
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS_B_DATA_P<3>	
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS_B_DATA_N<3>	
LVDS_IBG		LVDS	NC_LVDS_IBG	15 22
CRT_TVO_IREF		CRT	CRT_TVO_IREF	
CRT_RED	CRT_50S	CRT	CRT_RED	
CRT_GREEN	CRT_50S	CRT	CRT_GREEN	
CRT_BLUE	CRT_50S	CRT	CRT_BLUE	
CRT_SYNC	CRT_55S	CRT_SYNC	CRT_HSYNC_R	
CRT_SYNC	CRT_55S	CRT_SYNC	CRT_VSYNC_R	
TV_A_DAC	CRT_50S	TVDAC	TV_A_DAC	
TV_B_DAC	CRT_50S	TVDAC	TV_B_DAC	
TV_C_DAC	CRT_50S	TVDAC	TV_C_DAC	

NB Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0

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DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

Need to support MEM_*-style wildcards!

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_CLK_P<2..0>	16 31
	MEM_70D	MEM_CLK	MEM_CLK_N<2..0>	16 31
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_CKE<1..0>	16 31 33
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_CS_L<1..0>	16 31 33
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_ODT<1..0>	16 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_A<14..0>	16 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_BS<2..0>	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_RAS_L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_CAS_L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_WE_L	17 31 33
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_A_DQ<7..0>	17 31
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A_DQ<15..8>	17 31
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_A_DQ<23..16>	17 31
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A_DQ<31..24>	17 31
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_A_DQ<39..32>	17 31
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_A_DQ<47..40>	17 31
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A_DQ<55..48>	17 31
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A_DQ<63..56>	17 31
MEM_A_DM0	MEM_55S	MEM_DATA	MEM_A_DM<0>	17 31
MEM_A_DM1	MEM_55S	MEM_DATA	MEM_A_DM<1>	17 31
MEM_A_DM2	MEM_55S	MEM_DATA	MEM_A_DM<2>	17 31
MEM_A_DM3	MEM_55S	MEM_DATA	MEM_A_DM<3>	17 31
MEM_A_DM4	MEM_55S	MEM_DATA	MEM_A_DM<4>	17 31
MEM_A_DM5	MEM_55S	MEM_DATA	MEM_A_DM<5>	17 31
MEM_A_DM6	MEM_55S	MEM_DATA	MEM_A_DM<6>	17 31
MEM_A_DM7	MEM_55S	MEM_DATA	MEM_A_DM<7>	17 31
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	17 31
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	17 31
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	17 31
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	17 31
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	17 31
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	17 31
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	17 31
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	17 31
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_CLK_P<5..3>	16 32
	MEM_70D	MEM_CLK	MEM_CLK_N<5..3>	16 32
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_CKE<4..3>	16 32 33
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_CS_L<3..2>	16 32 33
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_ODT<3..2>	16 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_A<14..0>	16 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_BS<2..0>	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_RAS_L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_CAS_L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_WE_L	17 32 33
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B_DQ<7..0>	17 32
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_B_DQ<15..8>	17 32
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_B_DQ<23..16>	17 32
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B_DQ<31..24>	17 32
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B_DQ<39..32>	17 32
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B_DQ<47..40>	17 32
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_B_DQ<55..48>	17 32
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B_DQ<63..56>	17 32
MEM_B_DM0	MEM_55S	MEM_DATA	MEM_B_DM<0>	17 32
MEM_B_DM1	MEM_55S	MEM_DATA	MEM_B_DM<1>	17 32
MEM_B_DM2	MEM_55S	MEM_DATA	MEM_B_DM<2>	17 32
MEM_B_DM3	MEM_55S	MEM_DATA	MEM_B_DM<3>	17 32
MEM_B_DM4	MEM_55S	MEM_DATA	MEM_B_DM<4>	17 32
MEM_B_DM5	MEM_55S	MEM_DATA	MEM_B_DM<5>	17 32
MEM_B_DM6	MEM_55S	MEM_DATA	MEM_B_DM<6>	17 32
MEM_B_DM7	MEM_55S	MEM_DATA	MEM_B_DM<7>	17 32
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	17 32
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	17 32
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	17 32
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	17 32
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	17 32
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	17 32
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	17 32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	17 32

Memory Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 85 OF 92	

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_60S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	20 MIL	?
USB_2CLK	*	25 MIL	?

DG says minimum spacing 50 mils to clocks

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.13.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
IDE_PDD	IDE_55S	IDE	IDE_PDD<15..0> 23 42
IDE_PDA	IDE_55S	IDE	IDE_PDA<2..0> 23 42
IDE_PDCS	IDE_55S	IDE	IDE_PDCS1_L 23 42
IDE_PDCS	IDE_55S	IDE	IDE_PDCS3_L 23 42
IDE_CNTL	IDE_55S	IDE	IDE_PDIOW_L 23 42
IDE_PDIOR_L	IDE_55S	IDE	IDE_PDIOR_L 23 42
IDE_CNTL	IDE_55S	IDE	IDE_PDDACK_L 23 42
IDE_CNTL	IDE_55S	IDE	IDE_PDDREQ 23 42
IDE_PDIORDY	IDE_55S	IDE	IDE_PDIORDY 23 42
IDE_IRQ14	IDE_55S	IDE	IDE_IRQ14 23 42
IDE_RST_L	IDE_55S	IDE	ODD_RST_5VTOL_L 24 42
SATA_A_R2D	SATA_100D	SATA	SATA_A_R2D_C_P 23 81
	SATA_100D	SATA	SATA_A_R2D_C_N 23 81
	SATA_100D	SATA	SATA_A_R2D_P 81
	SATA_100D	SATA	SATA_A_R2D_N 81
SATA_A_D2R	SATA_100D	SATA	SATA_A_D2R_P 23 81
	SATA_100D	SATA	SATA_A_D2R_N 23 81
	SATA_100D	SATA	SATA_A_D2R_C_P
	SATA_100D	SATA	SATA_A_D2R_C_N
SATA_B_R2D	SATA_100D	SATA	TP_SATA_B_R2DP 23 42
	SATA_100D	SATA	TP_SATA_B_R2DN 23 42
	SATA_100D	SATA	SATA_B_R2D_P
	SATA_100D	SATA	SATA_B_R2D_N
SATA_B_D2R	SATA_100D	SATA	TP_SATA_B_D2RP 23 42
	SATA_100D	SATA	TP_SATA_B_D2RN 23 42
	SATA_100D	SATA	SATA_B_D2R_C_P
	SATA_100D	SATA	SATA_B_D2R_C_N
SATA_C_R2D	SATA_100D	SATA	TP_SATA_C_R2DP 23 42
	SATA_100D	SATA	TP_SATA_C_R2DN 23 42
	SATA_100D	SATA	SATA_C_R2D_P
	SATA_100D	SATA	SATA_C_R2D_N
SATA_C_D2R	SATA_100D	SATA	TP_SATA_C_D2RP 23 42
	SATA_100D	SATA	TP_SATA_C_D2RN 23 42
	SATA_100D	SATA	SATA_C_D2R_C_P
	SATA_100D	SATA	SATA_C_D2R_C_N
SATA_RBIAS	SATA_55S		SATA_RBIAS 23 42
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK 23 34
	HDA_55S	HDA	HDA_BIT_CLK_R 23
HDA_SYNC	HDA_55S	HDA	HDA_SYNC 23 34
	HDA_55S	HDA	HDA_SYNC_R 23
HDA_RST_L	HDA_55S	HDA	HDA_RST_L 23 34
	HDA_55S	HDA	HDA_RST_L_R 23
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0 23 34
	HDA_55S	HDA	HDA_SDIN_CODEC
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT 23 34
	HDA_55S	HDA	HDA_SDOUT_R 23
USB_EXTA	USB_90D	USB	USB_EXTA_P 24 43
	USB_90D	USB	USB_EXTA_N 24 43
	USB_90D	USB	USB_EXTA_MUXED_P
	USB_90D	USB	USB_EXTA_MUXED_N
USB_MINI	USB_90D	USB	USB_MINI_P 24 34
	USB_90D	USB	USB_MINI_N 24 34
USB_EXTD	USB_90D	USB	TP_USB_EXTDP 9 24
	USB_90D	USB	TP_USB_EXTDN 9 24
USB_CAMERA	USB_90D	USB	USB_CAMERA_P 24 44
	USB_90D	USB	USB_CAMERA_N 24 44
USB_BT	USB_90D	USB	USB_BT_P 24 81
	USB_90D	USB	USB_BT_N 24 81
USB_TPAD	USB_90D	USB	USB_TPAD_P 24 81
	USB_90D	USB	USB_TPAD_N 24 81
USB_IR	USB_90D	USB	USB_IR_P 7 24 81
	USB_90D	USB	USB_IR_N 7 24 81
USB_EXTB	USB_90D	USB	USB_EXTB_P 24 34
	USB_90D	USB	USB_EXTB_N 24 34
USB_EXCARD	USB_90D	USB	USB_EXCARD_P 24 34
	USB_90D	USB	USB_EXCARD_N 24 34
USB_EXTC	USB_90D	USB	USB_EXTC_P 24 34
	USB_90D	USB	USB_EXTC_N 24 34
USB_RBIAS	USB_60S		USB_RBIAS 24
SMB_SB_SCL	SMB_55S	SMB	SMBUS_SB_SCL 25 29 31 32 34 48
SMB_SB_SDA	SMB_55S	SMB	SMBUS_SB_SDA 25 29 31 32 34 48
SMB_SB_ME_SCL	SMB_55S	SMB	SMBUS_SB_ME_SCL 25 48
SMB_SB_ME_SDA	SMB_55S	SMB	SMBUS_SB_ME_SDA 25 48
SPI_SCLK	SPI_55S	SPI	SPI_SCLK_R 24 56
	SPI_55S	SPI	SPI_SCLK 56
	SPI_55S	SPI	SPI_A_SCLK_R
	SPI_55S	SPI	SPI_B_SCLK_R
SPI_SI	SPI_55S	SPI	SPI_SI_R 24 56
	SPI_55S	SPI	SPI_SI
	SPI_55S	SPI	SPI_A_SI_R 56
	SPI_55S	SPI	SPI_B_SI_R
SPI_SO	SPI_55S	SPI	SPI_SO 24 56
	SPI_55S	SPI	SPI_A_SO_R 56
	SPI_55S	SPI	SPI_B_SO
	SPI_55S	SPI	SPI_B_SO_R
SPI_CE_L0	SPI_55S	SPI	SPI_CE_R_L<0> 24 56
	SPI_55S	SPI	SPI_CE_L<0> 56
SPI_CE_L1	SPI_55S	SPI	SPI_CE_R_L<1>
	SPI_55S	SPI	SPI_CE_L<1>

SB Constraints (1 of 2)

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE NONE	SHT 86 OF 92	

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Controller Link (AMT) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLINK_12MIL	*	=STANDARD	12 MILS	5 MILS	300 MILS	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLINK	*	=1.8:1_SPACING	?
CLINK_VREF	*	12 MILS	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Ethernet (Yukon) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MILS	?

SOURCE: Based on Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCI_AD	PCI_55S	PCI	PCI_AD<18..0>	24 38
PCI_AD19	PCI_55S	PCI	PCI_AD<19>	24 38
PCI_AD20	PCI_55S	PCI	PCI_AD<20>	24 38
PCI_AD	PCI_55S	PCI	PCI_AD<31..21>	24 38
PCI_AD	PCI_55S	PCI	PCI_PAR	24 38
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>	24 38
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L	24 38
PCI_LOCK_L	PCI_55S	PCI	PCI_LOCK_L	24
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L	24 38
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L	24 38
PCI_FW_REQ_L	PCI_55S	PCI	PCI_FW_REQ_L	24 38
PCI_FW_GNT_L	PCI_55S	PCI	PCI_FW_GNT_L	7 24 38 47
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L	24
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L	
PCI_REQ2_L	PCI_55S	PCI	PCI_REQ2_L	24
PCI_GNT2_L	PCI_55S	PCI	PCI_GNT2_L	
INT_PIRQA_L	PCI_55S	PCI	INT_PIRQA_L	24
INT_PIRQB_L	PCI_55S	PCI	INT_PIRQB_L	24
INT_PIRQC_L	PCI_55S	PCI	INT_PIRQC_L	24
INT_PIRQD_L	PCI_55S	PCI	INT_PIRQD_L	24 38
INT_PIRQF_L	PCI_55S	PCI	INT_PIRQF_L	24
PCIE_A_R2D	PCIE_100D	PCIE	PCIE_A_R2D_C_P	
	PCIE_100D	PCIE	PCIE_A_R2D_C_N	
PCIE_A_D2R	PCIE_100D	PCIE	PCIE_A_D2R_P	
	PCIE_100D	PCIE	PCIE_A_D2R_N	
PCIE_B_R2D	PCIE_100D	PCIE	PCIE_B_R2D_C_P	
	PCIE_100D	PCIE	PCIE_B_R2D_C_N	
PCIE_B_D2R	PCIE_100D	PCIE	PCIE_B_D2R_P	
	PCIE_100D	PCIE	PCIE_B_D2R_N	
PCIE_EXCARD_R2D	PCIE_100D	PCIE	PCIE_EXCARD_R2D_C_P	24 34
	PCIE_100D	PCIE	PCIE_EXCARD_R2D_C_N	24 34
PCIE_EXCARD_D2R	PCIE_100D	PCIE	PCIE_EXCARD_D2R_P	24 34
	PCIE_100D	PCIE	PCIE_EXCARD_D2R_N	24 34
PCIE_FW_R2D	PCIE_100D	PCIE	PCIE_FW_R2D_C_P	
	PCIE_100D	PCIE	PCIE_FW_R2D_C_N	
PCIE_FW_D2R	PCIE_100D	PCIE	PCIE_FW_D2R_P	
	PCIE_100D	PCIE	PCIE_FW_D2R_N	
PCIE_MINI_R2D	PCIE_100D	PCIE	PCIE_MINI_R2D_C_P	24 34
	PCIE_100D	PCIE	PCIE_MINI_R2D_C_N	24 34
PCIE_MINI_D2R	PCIE_100D	PCIE	PCIE_MINI_D2R_P	24 34
	PCIE_100D	PCIE	PCIE_MINI_D2R_N	24 34
GLAN_COMP			GLAN_COMP	23
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_CLK	16 25
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_DATA	16 25
CLINK_NB_RESET_L	CLINK_55S	CLINK	CLINK_NB_RESET_L	16 25
CLINK_WLAN	CLINK_55S	CLINK	CLINK_WLAN_CLK	
CLINK_WLAN	CLINK_55S	CLINK	CLINK_WLAN_DATA	
CLINK_WLAN_RESET_L	CLINK_55S	CLINK	CLINK_WLAN_RESET_L	
NB_CLINK_VREF	CLINK_12MIL	CLINK_VREF	NB_CLINK_VREF	16
SB_CLINK_VREF0	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF0	25
SB_CLINK_VREF1	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF1	25
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE_ENET_R2D_C_P	24 35
	PCIE_100D	PCIE	PCIE_ENET_R2D_C_N	24 35
	PCIE_100D	PCIE	PCIE_ENET_R2D_P	35
	PCIE_100D	PCIE	PCIE_ENET_R2D_N	35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE_ENET_D2R_P	24 35
	PCIE_100D	PCIE	PCIE_ENET_D2R_N	24 35
	PCIE_100D	PCIE	PCIE_ENET_D2R_C_P	35
	PCIE_100D	PCIE	PCIE_ENET_D2R_C_N	35
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<0>	35 37
	ENET_100D	ENET_MDI	ENET_MDI_N<0>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<1>	35 37
	ENET_100D	ENET_MDI	ENET_MDI_N<1>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<2>	35 37
	ENET_100D	ENET_MDI	ENET_MDI_N<2>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3>	35 37
	ENET_100D	ENET_MDI	ENET_MDI_N<3>	35 37

SB Constraints (2 of 2)

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 87 OF 92	

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
CK505_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	7 10 29 30 88
CK505_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	7 10 29 30 88
CK505_NB	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_P	7 14 29 30 88
CK505_NB	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_N	7 14 29 30 88
CK505_ITP	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	13 29 30 83 88
CK505_ITP	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	13 29 30 83 88
CK505_PCIF0	CLK_MED_55S	CLK_MED	CK505_PCIF0_CLK_ITPEN	29 30
CK505_PCIF1	CLK_MED_55S	CLK_MED	CK505_PCIF1_CLK	29 30
CK505_PCI1	CLK_MED_55S	CLK_MED	CK505_PCI1_CLK	29 30
CK505_PCI2	CLK_MED_55S	CLK_MED	TP_CK505_PCI2_CLK	29 30
CK505_PCI3	CLK_MED_55S	CLK_MED	CK505_PCI3_CLK	29 30
CK505_PCI4	CLK_MED_55S	CLK_MED	TP_CK505_PCI4_CLK	29 30
CK505_PCI5	CLK_MED_55S	CLK_MED	CK505_PCI5_CLK_FCTSEL	29 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_48M_FSA	29 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_REF0_FSC	29 30
CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	CK505_CLK27M	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_CLK27M_SS	29 30
CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	TP_NB_CLK100M_DPLLSS_P	29 30
	CLK_PCIE_100D	CLK_PCIE	TP_NB_CLK100M_DPLLSS_N	29 30
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_GPU_P	9 29 30 67 88
	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_GPU_N	9 29 30 67 88
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_P	24 29 30 88
	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_N	24 29 30 88
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	29 30 34 88
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	29 30 34 88
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_P	23 29 30 88
	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_N	23 29 30 88
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_P	7 16 29 30 88
	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_N	7 16 29 30 88
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	29 30 34 88
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	29 30 34 88
CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	TP_PCIE_CLK100M_SRC7P	29 30
	CLK_PCIE_100D	CLK_PCIE	TP_PCIE_CLK100M_SRC7N	29 30
CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P	29 30 35 88
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N	29 30 35 88
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	7 10 29 30 88
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	7 10 29 30 88
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_P	7 14 29 30 88
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_N	7 14 29 30 88
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	13 29 30 83 88
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	13 29 30 83 88
(CK505_PCIF0)	CLK_MED_55S	CLK_MED	PCI_CLK33M_LPCPLUS	7 30 47
(CK505_PCIF1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SB	24 30
(CK505_PCI1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_FW	30 38
(CK505_PCI2)	CLK_MED_55S	CLK_MED	PCI_CLK33M_TPM	
(CK505_PCI3)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SMC	30 45
			CK505 PCI4 is project-specific	
			CK505 PCI5 is project-specific	
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	SB_CLK48M_USBCTLR	25 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	SB_CLK14P3M_TIMER	25 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_FSA	30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_FSC	30
(CK505_DOT96)	CRT_50S	GND	NB_CLK96M_DOT_P	
(CK505_DOT96)	CRT_50S	GND	NB_CLK96M_DOT_N	
(CK505_LVDS)	CRT_50S	GND	NB_CLK100M_DPLLSS_P	
(CK505_LVDS)	CRT_50S	GND	NB_CLK100M_DPLLSS_N	
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_GPU_P	9 29 30 67 88
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_GPU_N	9 29 30 67 88
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_P	24 29 30 88
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_N	24 29 30 88
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	29 30 34 88
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	29 30 34 88
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_P	23 29 30 88
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_N	23 29 30 88
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_P	7 16 29 30 88
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_N	7 16 29 30 88
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	29 30 34 88
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	29 30 34 88
			CK505 SRC7 is project-specific	
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P	29 30 35 88
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N	29 30 35 88

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	34 45 48 51 81
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	34 45 48 51 81
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	45 48 51 53
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	45 48 51 53
SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	45 48 51 74
SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	45 48 51 74
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	7 45 48 57
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	7 45 48 57
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	45 48 55
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	45 48 55

Clock & SMC Constraints

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW	*	=2:1_SPACING	?
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FW_D_CTL	FW_55S	FW	FW_LINK<7..0>	
FW_D_CTL	FW_55S	FW	FW_CTL<1..0>	
FW_LCLK	CLK_MED_55S	CLK_MED	CLKFW_LINK_LCLK	
	CLK_MED_55S	CLK_MED	CLKFW_PHY_LCLK	38 39
FW_PCLK	CLK_MED_55S	CLK_MED	CLKFW_LINK_PCLK	38 39
	CLK_MED_55S	CLK_MED	CLKFW_PHY_PCLK	
FW_LKON	FW_55S	FW	FW_LKON	
	FW_55S	FW	FW_LKON_R	
FW_LPS	FW_55S	FW	FW_LPS	38 39
FW_LREQ	FW_55S	FW	FW_LREQ	38 39
FW_PINT	FW_55S	FW	FW_PINT	38 39
FWPHY_CLK98P304M_XI	CLK_MED_55S	CLK_MED	CLK98P304M_FW_XI_R	
	CLK_MED_55S	CLK_MED	CLK98P304M_FW_XI	
FW_0_TPA	FW_110D	FW_TP	FW_PORT0_TPA_P	39 41
FW_0_TPA	FW_110D	FW_TP	FW_PORT0_TPA_N	39 41
FW_0_TPB	FW_110D	FW_TP	FW_PORT0_TPB_P	39 41
FW_0_TPB	FW_110D	FW_TP	FW_PORT0_TPB_N	39 41
FW_1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_P	39 41
FW_1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_N	39 41
FW_1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_P	39 41
FW_1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_N	39 41
Port 2 Not Used				

FireWire Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0

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GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R55SE	*	=55_OHM_SE	=40_OHM_SE	=55_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR3_50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TMDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
VGA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TMDS	*	20 MIL	?
VGA	*	20 MIL	?
VGA_SYNC	*	20 MIL	?

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
FB_A_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<0> 69 70 77
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<0> 69 70 77
FB_B_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<1> 69 70 77
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<1> 69 70 77
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<1..0> 69 70 77
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<11..6> 69 70 77
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_BA<2..0> 69 70 77
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_RAS_L 69 70 77
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_CAS_L 69 70 77
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_WE_L 69 70 77
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_CKE 69 70 77
FB_AB_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_A_CS0_L 69 70
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_DRAM_RST 69 70 77
FB_A_CMD	GDDR3_50SE	GDDR3_CMD	FB_A_LMA<5..2> 69 70 77
FB_B_CMD	GDDR3_50SE	GDDR3_CMD	FB_A_UMA<5..2> 69 70 77
FB_A_WDQS0	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<0> 69 70 77
FB_A_WDQS1	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<1> 69 70 77
FB_A_WDQS2	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<2> 69 70 77
FB_A_WDQS3	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<3> 69 70 77
FB_A_RDQS0	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<0> 69 70 77
FB_A_RDQS1	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<1> 69 70 77
FB_A_RDQS2	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<2> 69 70 77
FB_A_RDQS3	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<3> 69 70 77
FB_A_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<7..0> 69 70 77
FB_A_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<15..8> 69 70 77
FB_A_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<23..16> 69 70 77
FB_A_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<31..24> 69 70 77
FB_A_DQM0	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<0> 69 70 77
FB_A_DQM1	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<1> 69 70 77
FB_A_DQM2	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<2> 69 70 77
FB_A_DQM3	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<3> 69 70 77
FB_B_WDQS0	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<4> 69 70 77
FB_B_WDQS1	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<5> 69 70 77
FB_B_WDQS2	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<6> 69 70 77
FB_B_WDQS3	GDDR3_50SE	GDDR3_DQS	FB_A_WDQS<7> 69 70 77
FB_B_RDQS0	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<4> 69 70 77
FB_B_RDQS1	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<5> 69 70 77
FB_B_RDQS2	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<6> 69 70 77
FB_B_RDQS3	GDDR3_50SE	GDDR3_DQS	FB_A_RDQS<7> 69 70 77
FB_B_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<39..32> 69 70 77
FB_B_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<47..40> 69 70 77
FB_B_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<55..48> 69 70 77
FB_B_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB_A_DQ<63..56> 69 70 77
FB_B_DQM0	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<4> 69 70 77
FB_B_DQM1	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<5> 69 70 77
FB_B_DQM2	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<6> 69 70 77
FB_B_DQM3	GDDR3_50SE	GDDR3_DATA	FB_A_DQM_L<7> 69 70 77

G84M Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
(CK505_DOT96)	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M 30 72 73
CK505_CLK27MSS	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS 30 72 73
LVDS_L_CLK	LVDS_100D	LVDS	LVDS_L_CLK_P 74 76
	LVDS_100D	LVDS	LVDS_L_CLK_N 74 76
LVDS_L_DATA	LVDS_100D	LVDS	LVDS_L_DATA_P<2..0> 74 76
	LVDS_100D	LVDS	LVDS_L_DATA_N<2..0> 74 76
U127	LVDS_100D	LVDS	NC_LVDS_L_DATAP<3> 73 74
U126	LVDS_100D	LVDS	NC_LVDS_L_DATAN<3> 73 74
LVDS_U_CLK	LVDS_100D	LVDS	LVDS_U_CLK_P 74 76
	LVDS_100D	LVDS	LVDS_U_CLK_N 74 76
LVDS_U_DATA	LVDS_100D	LVDS	LVDS_U_DATA_P<2..0> 74 76
	LVDS_100D	LVDS	LVDS_U_DATA_N<2..0> 74 76
U128	LVDS_100D	LVDS	NC_LVDS_U_DATAP<3> 73 74
U125	LVDS_100D	LVDS	NC_LVDS_U_DATAN<3> 73 74
TMDS_CLK	TMDS_100D	TMDS	TMDS_CLK_P 74 80
TMDS_CLK	TMDS_100D	TMDS	TMDS_CLK_N 74 80
TMDS_DATA	TMDS_100D	TMDS	TMDS_DATA_P<5..0> 74 80
TMDS_DATA	TMDS_100D	TMDS	TMDS_DATA_N<5..0> 74 80
VGA_R_TV_C	VGA_50S	VGA	GPU_TV_C_VGA_R 73 80
VGA_G_TV_Y	VGA_50S	VGA	GPU_TV_Y_VGA_G 73 80
VGA_B_TV_COMP	VGA_50S	VGA	GPU_TV_COMP_VGA_B 73 80
	VGA_50S	VGA	GPU_VGA_R 73 74
	VGA_50S	VGA	GPU_VGA_G 73 74
	VGA_50S	VGA	GPU_VGA_B 73 74
	VGA_50S	VGA	GPU_TV_C 73 74
	VGA_50S	VGA	GPU_TV_Y 73 74
	VGA_50S	VGA	GPU_TV_COMP 73 74
VGA_SYNC	VGA_55S	VGA_SYNC	GPU_VGA_HSYNC 74 80
VGA_SYNC	VGA_55S	VGA_SYNC	GPU_VGA_VSYNC 74 80

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
FB_C_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<0> 69 71 78
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<0> 69 71 78
FB_D_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<1> 69 71 78
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<1> 69 71 78
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<1..0> 69 71 78
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<11..6> 69 71 78
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_BA<2..0> 69 71 78
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_RAS_L 69 71 78
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_CAS_L 69 71 78
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_WE_L 69 71 78
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_CKE 69 71 78
FB_CD_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_B_CS0_L 69 71
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_DRAM_RST 69 71 78
FB_C_CMD	GDDR3_50SE	GDDR3_CMD	FB_B_LMA<5..2> 69 71 78
FB_D_CMD	GDDR3_50SE	GDDR3_CMD	FB_B_UMA<5..2> 69 71 78
FB_C_WDQS0	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<0> 69 71 78
FB_C_WDQS1	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<1> 69 71 78
FB_C_WDQS2	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<2> 69 71 78
FB_C_WDQS3	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<3> 69 71 78
FB_C_RDQS0	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<0> 69 71 78
FB_C_RDQS1	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<1> 69 71 78
FB_C_RDQS2	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<2> 69 71 78
FB_C_RDQS3	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<3> 69 71 78
FB_C_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<7..0> 69 71 78
FB_C_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<15..8> 69 71 78
FB_C_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<23..16> 69 71 78
FB_C_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<31..24> 69 71 78
FB_C_DQM0	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<0> 69 71 78
FB_C_DQM1	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<1> 69 71 78
FB_C_DQM2	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<2> 69 71 78
FB_C_DQM3	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<3> 69 71 78
FB_D_WDQS0	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<4> 69 71 78
FB_D_WDQS1	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<5> 69 71 78
FB_D_WDQS2	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<6> 69 71 78
FB_D_WDQS3	GDDR3_50SE	GDDR3_DQS	FB_B_WDQS<7> 69 71 78
FB_D_RDQS0	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<4> 69 71 78
FB_D_RDQS1	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<5> 69 71 78
FB_D_RDQS2	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<6> 69 71 78
FB_D_RDQS3	GDDR3_50SE	GDDR3_DQS	FB_B_RDQS<7> 69 71 78
FB_D_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<39..32> 69 71 78
FB_D_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<47..40> 69 71 78
FB_D_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<55..48> 69 71 78
FB_D_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB_B_DQ<63..56> 69 71 78
FB_D_DQM0	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<4> 69 71 78
FB_D_DQM1	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<5> 69 71 78
FB_D_DQM2	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<6> 69 71 78
FB_D_DQM3	GDDR3_50SE	GDDR3_DATA	FB_B_DQM_L<7> 69 71 78

GPU (G84M) Constraints

SYNC_MASTER=M87_MLB SYNC_DATE=10/02/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V8_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PP1V8_MEM	*	PWR_P2MM
MEM_CMD	PP1V8_MEM	*	PWR_P2MM
MEM_CTRL	PP1V8_MEM	*	PWR_P2MM
MEM_DATA	PP1V8_MEM	*	PWR_P2MM
MEM_DQS	PP1V8_MEM	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLINK_VREF	GND	*	GND_P2MM
CLK_MED	GND	*	GND_P2MM
CLK_PCIE	GND	*	GND_P2MM
DMI	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
DMI	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM
ENET_MDI	ENET_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_MED	FW_POWER	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_70D	BOTTOM			0.127 MM	6.35 MM		

Allow 0.1 mm necks for >0.1 mm lines between thru-hole SO-DIMM pins.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	2.54 MM OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D	ISL10			0.100 MM	2.54 MM		
MEM_85D	ISL4,ISL10			0.100 MM	2.54 MM		

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	BGA	100_DIFF_BGA
TMDS_100D	BGA	100_DIFF_BGA
SATA_100D	BGA	100_DIFF_BGA

M87 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
(PCIE_EXCARD)	PCIE_100D	PCIE	PCIE_EXCARD_R2D_P	34
(PCIE_EXCARD)	PCIE_100D	PCIE	PCIE_EXCARD_R2D_N	34
(PCIE_MINI)	PCIE_100D	PCIE	PCIE_MINI_R2D_P	34
(PCIE_MINI)	PCIE_100D	PCIE	PCIE_MINI_R2D_N	34
	ENET_100D	ENET_MDI	ENET_MDI_R_P<3..0>	
	ENET_100D	ENET_MDI	ENET_MDI_R_N<3..0>	
	ENET_100D	ENETCONN	ENETCONN_P<3..0>	37
	ENET_100D	ENETCONN	ENETCONN_N<3..0>	37
	FW_110D	FW_TP	FW_PORT0_TPA_FL_P	41
	FW_110D	FW_TP	FW_PORT0_TPA_FL_N	41
	FW_110D	FW_TP	FW_PORT0_TPB_FL_P	41
	FW_110D	FW_TP	FW_PORT0_TPB_FL_N	41
(SATA_A_R2D)	SATA_100D	SATA	SATA_A_R2D_UF_P	81
(SATA_A_R2D)	SATA_100D	SATA	SATA_A_R2D_UF_N	81
(SATA_A_D2R)	SATA_100D	SATA	SATA_A_D2R_UF_P	81
(SATA_A_D2R)	SATA_100D	SATA	SATA_A_D2R_UF_N	81
(USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_P	43
(USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_N	43
(USB_EXTA)	USB_90D	USB	USB2_RT_P	43
(USB_EXTA)	USB_90D	USB	USB2_RT_N	43
(USB_EXTD)	USB_90D	USB	USB_WWAN_F_P	
(USB_EXTD)	USB_90D	USB	USB_WWAN_F_N	
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_F_P	7 44
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_F_N	7 44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GFXIMVP6_VSEN_P	75
	SENSE_1TO1_55S	SENSE	GFXIMVP6_VSEN_N	75
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	NBCOREISNS_P	50
	SENSE_1TO1_55S	SENSE	NBCOREISNS_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8ISNS_P	50
	SENSE_1TO1_55S	SENSE	P1V8ISNS_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V25ISNS_P	50
	SENSE_1TO1_55S	SENSE	P1V25ISNS_N	50
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	7 51
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	7 51
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_P	10 51
	THERM_1TO1_55S	THERM	CPU_THERMD_N	10 51
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	51
	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N	51
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P	51 72 73
	THERM_1TO1_55S	THERM	GPU_TDIODE_N	51 72 73
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	HSTHMSNS_D_P	7 51
	THERM_1TO1_55S	THERM	HSTHMSNS_D_N	7 51
THERM_DIFFPAIR	THERM_1TO1_55S	THERM	RSFSTHMSNS_D_P	7 51
	THERM_1TO1_55S	THERM	RSFSTHMSNS_D_N	7 51
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_F_P	76
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_F_N	76
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8ISNS_R_P	50
	SENSE_1TO1_55S	SENSE	P1V8ISNS_R_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_R_P	50
	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_R_N	50
	TMDS_100D	TMDS	TMDS_CLK_R_P	80
	TMDS_100D	TMDS	TMDS_CLK_R_N	80
	TMDS_100D	TMDS	TMDS_CLK_F_P	80
	TMDS_100D	TMDS	TMDS_CLK_F_N	80
	TMDS_100D	TMDS	TMDS_DATA_F_P<5..0>	80
	TMDS_100D	TMDS	TMDS_DATA_F_N<5..0>	80
(VGA_R_TV_Y)	VGA_50S	VGA	VGA_R	80
(VGA_G_TV_C)	VGA_50S	VGA	VGA_G	80
(VGA_B_TV_COMP)	VGA_50S	VGA	VGA_B	80
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_HSYNC_R	80
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_VSYNC_R	80
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_HSYNC	80
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_VSYNC	80
		PP1V8_MEM	PP1V8_S3	8 31 32 38 50 62 91
		PP1V8_MEM	PP1V8_S3	8 31 32 38 50 62 91
		GND	GND	
		ENET_POWER		
		SB_POWER	PP3V3_S5	8 24 25 26 27 28 46 48 56 58 60 65 76
		SB_POWER	PP3V3_S0	52 53 58 59 65 82 8 13 14 15 17 23 24 25 26 27 28 29 30 31 32 42 46 47 48 50 51
		SB_POWER	PP1V5_S0	8 11 12 22 26 27 34 63
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_P	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_N	50
		FW_POWER		

Project Specific Constraints

SYNC_MASTER=M87_MLB SYNC_DATE=08/28/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0
SCALE: NONE	SHT 91 OF 92	

M75 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.100 MM	0.100 MM			
55_OHM_SE	ISL2,ISL11	Y	0.250 MM	0.076 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.125 MM	0.125 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
46_OHM_SE	TOP,BOTTOM	Y	0.126 MM	0.126 MM			
46_OHM_SE	*	Y	0.100 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.150 MM	0.150 MM			
45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.185 MM			
40_OHM_SE	*	Y	0.131 MM	0.131 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.335 MM	0.335 MM			
27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM
70_OHM_DIFF	ISL9,ISL10	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM
70_OHM_DIFF	ISL2,ISL11	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM
80_OHM_DIFF	ISL9,ISL10	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM
85_OHM_DIFF	ISL9,ISL10	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9,ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9,ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL2,ISL11	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PCB Rule Definitions

SYNC_MASTER=M87_MLB SYNC_DATE=10/03/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7431	A.0.0

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