1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
E		287417	PRODUCTION RELEASED	08/07/03	?

SCHEM,MLB,PB 17"

08/07/2003

BOM OPTIONS	STUFF	NO STUFF
D3_HOT		√
D3_COLD	√	
GPU_SS	√	
GPU_SWITCH	√	
SERIAL_DEBUG	√	
VCORE_OFFSET	√	
1_8V_MAXBUS	√	
1_5V_MAXBUS		√
NEC_USB		√
INTREPID_USB	√	
BBANG		√
NO_BBANG	√	
MAP31		√
MAP17	√	
SSCG		√
NO_SSCG	√	
5V_HD_LOGIC	√	
3V_HD_LOGIC		√
NO_4XVCORE	√	
4X_VCORE		√

MAP17/MAP31

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6469	1	SCHEM,MLB,PB 17	SCH1	
820-1502	1	PCBF,MLB,PB 17	PCB1	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0076	1	IC,ASSP,MAP17-464,GRPHCS CTLR,548 BGA	U43	CRITICAL	MAP17
338S0094	1	IC,ASSP,MAP31-464,GRPHCS CTLR,548 BGA	U43	CRITICAL	MAP31

DIMENSIONS ARE IN MILLIMETERS
XX ± _____
X.XX ± _____
X.XXX ± _____
ANGLES ± _____
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer Inc.

TITLE
SCHEM,MLB,PB 17"

DRAWING NUMBER 051-6469 REV. E

SHT 1 OF 44

U44 INTREPID

Ethernet
J18 Ethernet Connector P.27
4 DATA PAIRS
U49 Ethernet PHY P.27
G/MII
3.3V
10/100/1000
8BIT TX
8BIT RX
125MHZ

FireWire
J24 FW - A Connector P.29
2 DATA PAIRS @ 200MHz
J22 FW - B Connector P.29
2 DATA PAIRS @ 400MHZ
U28 FireWire PHY P.28
1394 OHCI
3.3V
8BIT TX/RX
50MHZ

Optical Drive
J11 OPTICAL DRIVE Connector P.24
EIDE

Ultra ATA/100
J13 ULTRA ATA/100 Connector P.24
UIDE

Sleep LED
SLEEP LED P.25
LMU

Audio
J14 TUBA (SOUND) Connector P.25
I2S
I2C

Fan
U48/J2/J4 Fan Circuit P.25
I2C

Battery / Power
J25 Battery Connector P.31
Power Supply & Charger P.31-35
J19 SUTRO (PWR) Connector P.31
SMBUS
3.3V

LMU
U36 LMU P.23
I2C

PMU
U39 PMU P.30
SERIAL
5V

CardBus
J10 CARDBUS Connector P.18
33MHZ
16/32 BITS
3.3V/5V

Trackpad / Keyboard
J15 TRACKPAD Connector | Keyboard Connector
KB LED LIGHT SENSOR P.23

Serial Debug
J5 Serial Debug Connector P.25

Left USB
J3 (SHARE WITH BLUETOOTH) LEFT USB P.24
USB 2.0

Right USB
J12 RIGHT USB BACKUP BATTERY P.32
NOT USED
USB 2.0

BlueTooth
J3 (SHARE WITH LEFT USB) BlueTooth P.24
NOT USED

Modem Board
J9 Modem Board Connector P.25
INTRPEID
I2C

Boot ROM
U17 BOOT ROM 1M X 8 P.10

USB 2.0 Controller
U52 USB 2.0 CONTROLLER P.26

TI PCI1510 CardBus Controller
U26 TI PCI1510 CardBus Controller P.18
PCI BUS
32BITS
33MHZ
3.3V

AirPort
J21 AIRPOPT Connector P.24

Main Bus Table

ETHERNET 10/100/1000 P.14	FIREWIRE 400 MB/S P.14	UATA 100 P.14	EIDE P.14	CARDSLOT P.14	I2S P.15	I2C P.14 P.15
USB PORT A P.15					SCCA P.15	
USB PORT B P.15					VIA/PMU P.15	
USB PORT C P.15					BOOTROM P.14	
USB PORT D P.15					PCI 64BITS 33MHZ P.13	
USB PORT E P.15						
USB PORT F P.15						
MAXBUS P.9					4X AGP P.13	

NOT USED

AGP / NVIDIA
AGP BUS
1.5V/3.3V
32BITS
66MHZ
U43 NVIDIA MAP17 64MB P.19-21
MEMORY CH. A (INTERNAL MEM)
MEMORY CH. C (INTERNAL MEM)
MEMORY CH. B (INTERNAL MEM)
MEMORY CH. D (INTERNAL MEM)

Inverter
J8 Inverter Connector P.22

Video Outputs
LVDS
EDID (I2C)
S-VIDEO
COMPOSITE
TMDS
RGB
(DDC TOO)

J7 LCD Panel Connector P.22
J17 S-Video Connector P.22
J16 DVI-I Connector P.22

MAXBUS
MAXBUS
1.8V
167MHZ
32BIT ADDRESS
64BIT DATA

APOLLO CPU
U42 APOLLO CPU (MPC7455) P.5-6
CPU PLL Config P.7
PMU

L3 Cache
L3 BUS
1.5V
250/300 MHZ
18BIT ADDRESS
64BIT DATA
U6/U7 L3 Cache P.8

DDR Memory
DDR MEMORY P.10
MEMORY BUS
2.5V
167MHZ
64BITS
U11/U12/U13/U14 2:1 DDR MUXES P.11
J20/J23 DDR SDRAM DIMM 0
DDR SDRAM DIMM 1 SO-DIMM Connector P.12

SYSTEM BLOCK DIAGRAM

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6469 | REV. E

SCALE NONE | SHT 2 OF 44

POWER SYSTEM ARCHITECTURE

AC ADAPTER IN PG 31

INRUSH LIMITER PG 30

+24V_PBUS

1V20_REF
>~13.44V TURNS-ON
<~13.44V SHUTS-OFF
U21 PG 31

RUN/SS
BUCK REGULATOR (LTC1625) PG 32
VCC
AC: 12.8V
NO AC: BATTERY VOLTAGE 1625 NOT RUNNING
SHUTDOWN: RUNNING
SLEEP: RUNNING
RUN: RUNNING

+PBUS (12.8V)

BACKLIGHT INVERTER

+5V_MAIN
VCC
MAIN 2.5V/1.5V DC/DC (MAX1715) PG 35
PGOOD
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING
TURNS ON OUTPUT @ 2.4V ON1/ON2

MAP17 DDR CORE
MAP17 DDR I/O
L3 CORE
DDR POWER
+2.5V_MAIN

1_5V_2_5V_OK

+1.5V_MAIN
INTREPID CORE
AGP I/O
L3 I/O

DCDC_EN
SLEEP
MAXBUS SEQUENCING

+PBUS

+5V_MAIN
VCC
SHDN
DC/DC (MAX1717) PG 34
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING

CPU_VCORE (+1.4V/+1.5V)

14V_PBUS

+3V_PMU LDO PG 32
+BATT
+5V_MAIN
+3V_PMU
+4_6V_BU

RC AT 1M*0.047UF @ 24V
STARTS 2.0MSEC AFTER DCDC_EN_L BECOMES LOW

DCDC_EN_L
AFTER PMU IS UP AND RUNNING
DCDC_EN_L WILL PULL ON1/ON2 LOW IN SHUTDOWN

RUN/SS - 5V
TURNS ON AT >1V
<100UA ALLOWED
INTERNAL ZENER CLAMP TO 6V
MAIN 3V/5V DC/DC (LTC3707) PG 33
VCC
PGOOD
STBYMD
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING
INTERNAL ZENER CLAMP TO 6V
<100UA ALLOWED
TURNS ON AT >1V
RUN/SS - 3V

+5V_MAIN
3V_5V_OK
HOLDS BOTH RUN/SS AT GND WHEN IT'S CONNECTED TO GND
TURNS CONTROL TO RUN/SS WHEN IT'S OPEN

+3.3V_MAIN

+PBUS (12.8V)

+5V_MAIN
EXT_VCC
VCC
DC/DC (LTC1778) PG 20
SHUTDOWN: STOPPED
SLEEP: D3HOT/D3COLD
RUN: RUNNING
TURNS ON AS LOW AS 0.8V/TYP 1.5V
INTERNAL 1.2UA CURRENT SOURCE
RUN/SS

GPU_VCORE +1.35V/+1.2V

DCDC_EN
SLEEP
D3_COLD
GPU_VCORE SEQUENCING
1M & 0.1UF @14V, IT TAKES ~5.88MS TO START SWITCHER
1_5V_2_5V_OK
D3_HOT
DCDC_EN_L
D3_HOT

1_5V_2_5V_OK WILL NOT PULL LOW UNTIL +5V_MAIN TURNS ON
HOWEVER, 5V SHOULD TURN ON ~2.23MS AFTER DCDC_EN_L OR PMU_POWERUP_L BECOMES '1'; MUCH LESS THAN THE RC CHARGING AT INT_VCC (5V)

BACKUP BATTERY
+PBUS
12.8V CHARGES BACKUP BATTERY
24V IS OUTPUT ONLY FROM BACKUP BATTERY
CHARGER INPUT & BOOST OUTPUT PG 32

BACKUP BATTERY CIRCUIT CHARGES OFF +PBUS AND PREVENTS +PBUS AND +24V_PBUS FROM DROPPING BELOW 6V (UNTIL DRAINED)

RC AT 1M*0.1UF @ 24V
STARTS ~4.25MSEC AFTER DCDC_EN_L BECOMES LOW

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED
+24V_PBUS

BATTERY CHARGER (MAX1772) PG 31

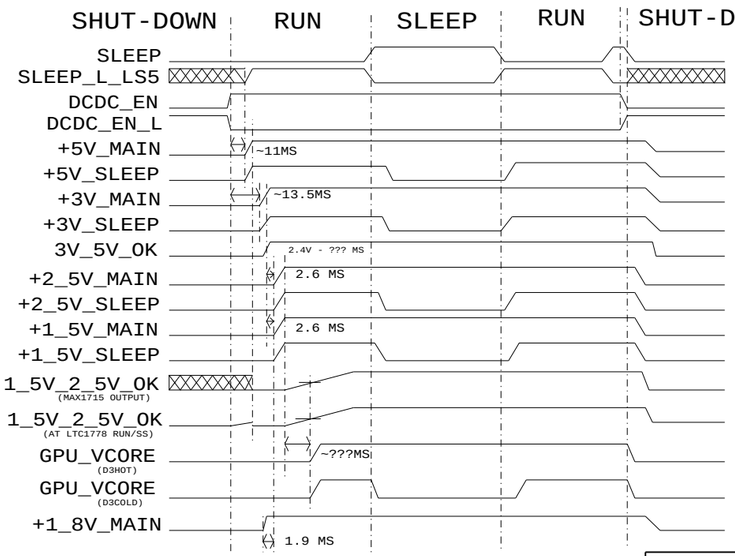
DC/DC (LTC3411) PG 35
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING
+1.8V_MAIN
MAXBUS BROADCOM

+BATT

3S 3P PRISMATIC CELLS

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

BATTERY VOLTAGE FEED-IN PATH PG 31
+PBUS



POWER BLOCK DIAGRAM

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6469 | REV. E

SCALE NONE | SHT 3 OF 44

PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 12
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

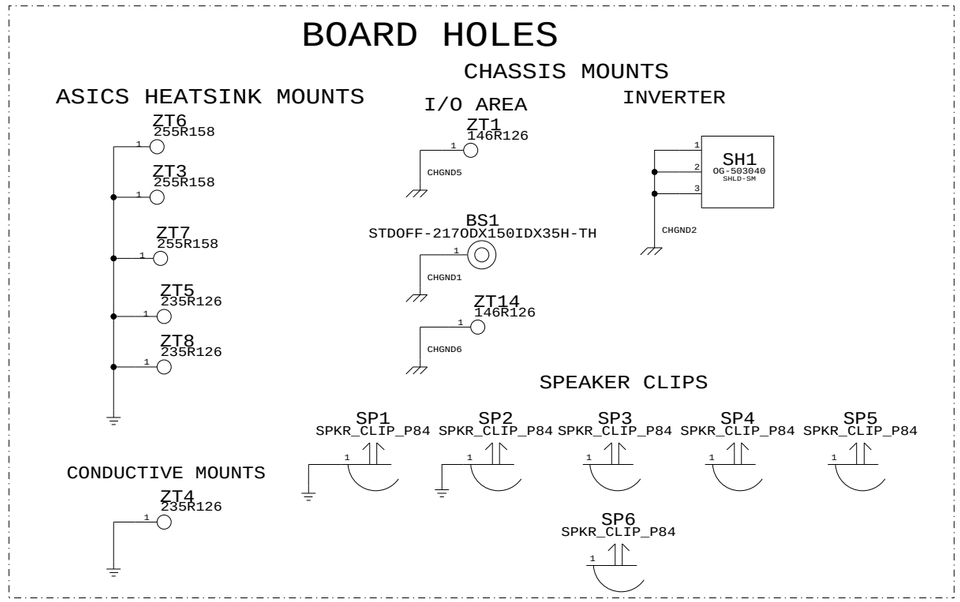
SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

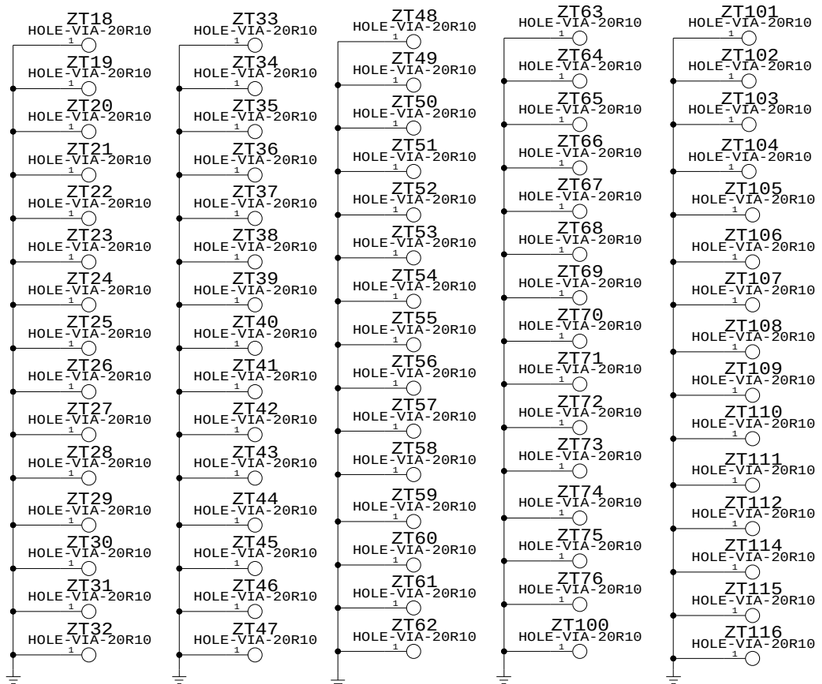
20R10 TH VIA OR VIA IN PAD

1		SIGNAL (1/3 OZ + COPPER PLATING)
2	PREPREG (3MIL)	GROUND (1/2 OZ)
3	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
4	PREPREG (3MIL)	SIGNAL (1/2 OZ)
5	LAMINATE (4MIL)	GROUND (1/2 OZ)
6	PREPREG (2MIL)	CUT POWER PLANE(1 OZ)
7	LAMINATE (3MIL)	CUT POWER PLANE(1 OZ)
8	PREPREG (2MIL)	GROUND (1/2 OZ)
9	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
10	PREPREG (3MIL)	SIGNAL (1/2 OZ)
11	LAMINATE (4MIL)	GROUND (1/2 OZ)
12	PREPREG (3MIL)	SIGNAL (1/3 OZ + COPPER PLATING)

BOARD HOLES



GROUND VIAS



BOARD INFORMATION

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6469	E
SCALE: NONE	SHT 4 OF 44	

CPU_VCORE DECOUPLING NETWORK

39 38 34 5 CPU_VCORE_SLEEP

R175 1 — 470 — 5% 1/16W MF 402 — 2

C153 10UF 20% 6.3V CERM 805	C141 10UF 20% 6.3V CERM 805	C108 0.1UF 20% 10V CERM 402	C200 0.1UF 20% 10V CERM 402	C173 0.1UF 20% 10V CERM 402	C140 0.1UF 20% 10V CERM 402		
C239 10UF 20% 6.3V CERM 805	C255 10UF 20% 6.3V CERM 805	C138 0.1UF 20% 10V CERM 402	C109 0.1UF 20% 10V CERM 402	C201 0.1UF 20% 10V CERM 402	C174 0.1UF 20% 10V CERM 402		
C204 2.2UF 20% 10V CERM 805	C180 2.2UF 20% 10V CERM 805	C172 0.1UF 20% 10V CERM 402	C139 0.1UF 20% 10V CERM 402	C110 0.1UF 20% 10V CERM 402	C202 0.1UF 20% 10V CERM 402		

MORE 0805 10UF CAPS ON VCORE POWER SUPPLY PAGE (PG 32)

CPU_OVDD DECOUPLING NETWORK

MAXBUS_SLEEP 5 7 9 16 17 23 34 38

R50 1 — 470 — 5% 1/16W MF 402 — 2

C31 0.1UF 20% 10V CERM 402	C73 0.1UF 20% 10V CERM 402	C51 0.1UF 20% 10V CERM 402	C203 0.1UF 20% 10V CERM 402				
C74 0.1UF 20% 10V CERM 402	C76 0.1UF 20% 10V CERM 402	C111 0.1UF 20% 10V CERM 402	C238 0.1UF 20% 10V CERM 402				
C30 0.1UF 20% 10V CERM 402	C45 0.1UF 20% 10V CERM 402	C95 0.1UF 20% 10V CERM 402	C75 0.1UF 20% 10V CERM 402				

J9 J11 J13 J16 K12 K14 L9 L11 L13 L16 M10 M12 M14 N9 N11 N13 P10 P12 P14 — VDD

B3 C5 C7 C10 D2 E3 E9 F5 G3 G9 H7 J5 K3 L7 M5 N3 P7 R4 T3 U5 U7 U11 U15 V3 V9 V13 Y2 Y5 Y7 Y10 Y17 Y19 AA4 AA15 — OVDD

CPU INTERNAL PLL FILTERING

CPU_VCORE_SLEEP 5 34 38 39

R5 2 — 10 — 5% 1/16W MF 402 — 1

38 CPU_AVDD

C29 1 — 0.1UF 20% 10V CERM 402 — 2

C9 1 — 2.2UF 20% 10V CERM 805 — 2

CRITICAL

U42
APOLLO
1GHZ-1.32V
R3.3-NDE5-85C-BGA
(1 OF 3)

36 9 CPU_BR_L	K1	BR
36 9 CPU_BG_L	R3	BG
NC	F2	NC12
36 9 CPU_TS_L	P5	TS
5 CPU_PULLDOWN	E10	A0
	N4	A1
	E8	A2
	N5	A3
36 9 CPU_ADDR<0>	C8	A4
36 9 CPU_ADDR<1>	R2	A5
36 9 CPU_ADDR<2>	A7	A6
36 9 CPU_ADDR<3>	M2	A7
36 9 CPU_ADDR<4>	A6	A8
36 9 CPU_ADDR<5>	M1	A9
36 9 CPU_ADDR<6>	A10	A10
36 9 CPU_ADDR<7>	U2	A11
36 9 CPU_ADDR<8>	N2	A12
36 9 CPU_ADDR<9>	P8	A13
36 9 CPU_ADDR<10>	M8	A14
36 9 CPU_ADDR<11>	W4	A15
36 9 CPU_ADDR<12>	N6	A16
36 9 CPU_ADDR<13>	U6	A17
36 9 CPU_ADDR<14>	R5	A18
36 9 CPU_ADDR<15>	Y4	A19
36 9 CPU_ADDR<16>	P1	A20
36 9 CPU_ADDR<17>	P4	A21
36 9 CPU_ADDR<18>	R6	A22
36 9 CPU_ADDR<19>	M7	A23
36 9 CPU_ADDR<20>	N7	A24
36 9 CPU_ADDR<21>	AA3	A25
36 9 CPU_ADDR<22>	U4	A26
36 9 CPU_ADDR<23>	W2	A27
36 9 CPU_ADDR<24>	W1	A28
36 9 CPU_ADDR<25>	W3	A29
36 9 CPU_ADDR<26>	V4	A30
36 9 CPU_ADDR<27>	AA1	A31
36 9 CPU_ADDR<28>	D10	A32
36 9 CPU_ADDR<29>	J4	A33
36 9 CPU_ADDR<30>	G10	A34
36 9 CPU_ADDR<31>	D9	A35
NC	L5	AP0
NC	L6	AP1
NC	J1	AP2
NC	H2	AP3
NC	G5	AP4
36 9 CPU_TT<0>	F1	TT0
36 9 CPU_TT<1>	F4	TT1
36 9 CPU_TT<2>	K8	TT2
36 9 CPU_TT<3>	A5	TT3
36 9 CPU_TT<4>	E1	TT4
36 9 CPU_TBST_L	B7	TBST
36 9 CPU_TSIZ<0>	L1	TSIZ0
36 9 CPU_TSIZ<1>	H3	TSIZ1
36 9 CPU_TSIZ<2>	D1	TSIZ2
36 9 CPU_GBL_L	M4	GBL
36 9 CPU_WT_L	L2	WT
36 9 CPU_CI_L	R1	CI
36 9 CPU_AACK_L	U1	AACK
36 9 CPU_ARTRY_L	T2	ARTRY
5 CPU_SHD0_L	L4	SHD0
5 CPU_SHD1_L	L8	SHD1
36 9 CPU_HIT_L	K2	HIT

AVDD	B2	
BVSEL	G6	CPU_BUS_VSEL 7
SYSCLK	D6	SYSCLK_CPU 9 36
CLK_OUT	N1	CPU_CLKOUT_SPN
PLL_CFG0	A2	CPU_PLL_CFG<0> 7
PLL_CFG1	F7	CPU_PLL_CFG<1> 7
PLL_CFG2	C2	CPU_PLL_CFG<2> 7
PLL_CFG3	D4	CPU_PLL_CFG<3> 7
PLL_EXT	H8	CPU_PLL_CFGEXT 7
DBG	V1	CPU_DBG_L 9 36
DRDY	T6	36 CPU_DRDY_L_UF
DTI0	P2	CPU_EDTI 5
DTI1	T5	CPU_DTI<0> 9 36
DTI2	U3	CPU_DTI<1> 9 36
DTI3	P6	CPU_DTI<2> 9 36
TDI	E4	JTAG_CPU_TDI 5 23 39
TDO	H1	JTAG_CPU_TDO_TP 39
TMS	K4	JTAG_CPU_TMS 5 23 39
TCK	J7	JTAG_CPU_TCK 5 23 39
TRST	C1	JTAG_CPU_TRST_L 5 23 39
LSSD_MODE	F6	CPU_LSSD_MODE 5
L1_TSTCLK	H4	CPU_L1TSTCLK 5
L2_TSTCLK	J2	CPU_L2TSTCLK 5
TA	N8	CPU_TA_L 9 36
TEA	T1	CPU_TEA_L 9 36
TBEN	L3	CPU_TBEN 5 9
QREQ	Y1	CPU_QREQ_L 9 36
QACK	K7	CPU_QACK_L 9 36
CKSTP_IN	F3	
CKSTP_OUT	K6	CPU_CHKSTP_OUT_L 5 39
TEST0	B10	CPU_CHKS_L 5
INT	J6	MPIC_CPU_INT_L 5 15
SMI	G8	CPU_SMI_L 5 30
MCP	B8	CPU_MCP_L 5
SRESET	G1	CPU_SRESET_L 5 39
HRESET	A3	CPU_HRESET_L 5 7 23 39
PMON_IN	E6	CPU_PMONIN_L 5
PMON_OUT	B4	NC
BMODE0	C6	CPU_EMODE0_L 7
BMODE1	C4	CPU_EMODE1_L 5
TEST6	A9	CPU_PULLDOWN 5
EXT_QUAL	B9	
TEST1	H6	CPU_PULLUP 5
TEST2	H10	
NC13	B6	NC
TEST3	D8	CPU_SRWX_L 5
TEST4	F9	
TEST5	F8	
SPARE0	A8	NC
SPARE1	D3	NC
SPARE2	A9	NC
SPARE3	J8	NC
NC3	A11	NC
NC2	B11	NC
NC1	C11	NC
NC4	D5	NC
NC5	D11	NC
NC6	E7	NC
NC7	E11	NC
NC8	F11	NC
NC9	G2	NC
NC10	G11	NC
NC11	H11	NC

RC GLITCH FILTER
PLACE CLOSE TO PIN

R51 — 0 — 5% 1/16W MF 402

CPU_DRDY_L 9 36

C77 1 — 10PF 5% 50V CERM 402 — 2

J10 J12 J14 K9 K11 K13 K15 L10 L12 L14 M9 M11 M13 N10 N12 N14 P9 P11 P13 P15 B1 B5 C3 C9 D7 E2 E5 F10 G4 G7 H5 J3 K5 M3 M6 P3 T4 T7 T9 T13 V2 V5 V8 V12 V15 W7 Y3 Y9 Y13 Y15 Y20 AA5 AA17 AB1 — GND

MPC7450 PULL-UPS

+1_5V_SLEEP — 1_5V_MAXBUS — R606 — 0 — 5% 1/16W MF 603

+1_8V_SLEEP — 1_8V_MAXBUS — R602 — 0 — 5% 1/16W MF 603

38 34 23 17 16 9 7 5 MAXBUS_SLEEP

9 5 CPU_TBEN	R39	10K
5 CPU_CHKS_L	R90	10K
5 CPU_SHD0_L	R518	10K
5 CPU_SHD1_L	R66	10K
5 CPU_MCP_L	R73	10K
5 CPU_LSSD_MODE	RP11	10K 8 SM1
5 CPU_L2TSTCLK	R24	10K
39 5 CPU_CHKSTP_OUT_L	R38	1K
5 CPU_SRWX_L	R84	10K
5 CPU_PMONIN_L	R55	10K
5 CPU_EMODE1_L	R44	10K
5 CPU_PULLUP	R56	1K
39 23 7 5 CPU_HRESET_L	R37	10K
30 5 CPU_SMI_L	R74	10K
470OHM FOR BOOT BANGER 39 23 5 JTAG_CPU_TMS	R13	470
470OHM FOR BOOT BANGER 39 23 5 JTAG_CPU_TDI	R12	470
15 5 MPIC_CPU_INT_L	RP11	10K
39 5 CPU_SRESET_L	RP11	10K SM1
5 CPU_L1TSTCLK	RP11	10K SM1
5 CPU_EDTI	R32	10K
39 23 5 JTAG_CPU_TCK	R65	10K
5 CPU_PULLDOWN	R91	470

All: 5% 1/16W MF 402

MAXBUS_SLEEP 5 7 9 16 17 23 34 38

BBANG

470OHM FOR BOOT BANGER — R19 — 470 — 5% 1/16W MF 402

39 23 5 JTAG_CPU_TRST_L

NO_BBANG

R23 — 200 — 5% 1/16W MF 402

MPC7450 MAXBUS

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6469	E

SCALE: NONE — SHT 5 OF 44

CRITICAL

U42
APOLLO
1GHZ-1.32V
R3.3-NDE5-85C-BGA
(2 OF 3)

36 9	CPU_DATA<0>	AB15	D0
36 9	CPU_DATA<1>	T14	D1
36 9	CPU_DATA<2>	R14	D2
36 9	CPU_DATA<3>	AB13	D3
36 9	CPU_DATA<4>	V14	D4
36 9	CPU_DATA<5>	U14	D5
36 9	CPU_DATA<6>	AB14	D6
36 9	CPU_DATA<7>	W16	D7
36 9	CPU_DATA<8>	AA11	D8
36 9	CPU_DATA<9>	Y11	D9
36 9	CPU_DATA<10>	U12	D10
36 9	CPU_DATA<11>	W13	D11
36 9	CPU_DATA<12>	Y14	D12
36 9	CPU_DATA<13>	U13	D13
36 9	CPU_DATA<14>	T12	D14
36 9	CPU_DATA<15>	W12	D15
36 9	CPU_DATA<16>	AB12	D16
36 9	CPU_DATA<17>	R12	D17
36 9	CPU_DATA<18>	AA13	D18
36 9	CPU_DATA<19>	AB11	D19
36 9	CPU_DATA<20>	Y12	D20
36 9	CPU_DATA<21>	V11	D21
36 9	CPU_DATA<22>	T11	D22
36 9	CPU_DATA<23>	R11	D23
36 9	CPU_DATA<24>	W10	D24
36 9	CPU_DATA<25>	T10	D25
36 9	CPU_DATA<26>	W11	D26
36 9	CPU_DATA<27>	V10	D27
36 9	CPU_DATA<28>	R10	D28
36 9	CPU_DATA<29>	U10	D29
36 9	CPU_DATA<30>	AA10	D30
36 9	CPU_DATA<31>	U9	D31
36 9	CPU_DATA<32>	V7	D32
36 9	CPU_DATA<33>	T8	D33
36 9	CPU_DATA<34>	AB4	D34
36 9	CPU_DATA<35>	Y6	D35
36 9	CPU_DATA<36>	AB7	D36
36 9	CPU_DATA<37>	AA6	D37
36 9	CPU_DATA<38>	Y8	D38
36 9	CPU_DATA<39>	AA7	D39
36 9	CPU_DATA<40>	W8	D40
36 9	CPU_DATA<41>	AB10	D41
36 9	CPU_DATA<42>	AA16	D42
36 9	CPU_DATA<43>	AB16	D43
36 9	CPU_DATA<44>	AB17	D44
36 9	CPU_DATA<45>	Y18	D45
36 9	CPU_DATA<46>	AB18	D46
36 9	CPU_DATA<47>	Y16	D47
36 9	CPU_DATA<48>	AA18	D48
36 9	CPU_DATA<49>	W14	D49
36 9	CPU_DATA<50>	R13	D50
36 9	CPU_DATA<51>	W15	D51
36 9	CPU_DATA<52>	AA14	D52
36 9	CPU_DATA<53>	V16	D53
36 9	CPU_DATA<54>	W6	D54
36 9	CPU_DATA<55>	AA12	D55
36 9	CPU_DATA<56>	V6	D56
36 9	CPU_DATA<57>	AB9	D57
36 9	CPU_DATA<58>	AB6	D58
36 9	CPU_DATA<59>	R7	D59
36 9	CPU_DATA<60>	R9	D60
36 9	CPU_DATA<61>	AA9	D61
36 9	CPU_DATA<62>	AB8	D62
36 9	CPU_DATA<63>	W9	D63
NC		AA2	DP0
NC		AB3	DP1
NC		AB2	DP2
NC		AA8	DP3
NC		R8	DP4
NC		W5	DP5
NC		U8	DP6
NC		AB5	DP7

B13 B15 B17 B19 D21 D12 D14 D16 D18 D21 E19 E13 F15 F17 F21 G19 H12 H14 H17 H19 K13 K17 K21 K19 M17 M21 N19 P17 P21 R15 R19 T17 T21 U19 U13 V17 V21 W19 Y21

GVDD

CRITICAL

U42
APOLLO
1GHZ-1.32V
R3.3-NDE5-85C-BGA
(3 OF 3)

36 8	L3_ADDR<0>	L18	L3A0
36 8	L3_ADDR<1>	K22	L3A1
36 8	L3_ADDR<2>	L16	L3A2
36 8	L3_ADDR<3>	K20	L3A3
36 8	L3_ADDR<4>	K18	L3A4
36 8	L3_ADDR<5>	J22	L3A5
36 8	L3_ADDR<6>	J20	L3A6
36 8	L3_ADDR<7>	H22	L3A7
36 8	L3_ADDR<8>	J18	L3A8
36 8	L3_ADDR<9>	K16	L3A9
36 8	L3_ADDR<10>	H20	L3A10
36 8	L3_ADDR<11>	G22	L3A11
36 8	L3_ADDR<12>	F22	L3A12
36 8	L3_ADDR<13>	G20	L3A13
36 8	L3_ADDR<14>	H18	L3A14
36 8	L3_ADDR<15>	E22	L3A15
36 8	L3_ADDR<16>	J16	L3A16
36 8	L3_ADDR<17>	F20	L3A17
36 8	L3_DATA<0>	AA19	L3D0
36 8	L3_DATA<1>	AB20	L3D1
36 8	L3_DATA<2>	U16	L3D2
36 8	L3_DATA<3>	W18	L3D3
36 8	L3_DATA<4>	AA20	L3D4
36 8	L3_DATA<5>	AB21	L3D5
36 8	L3_DATA<6>	AA21	L3D6
36 8	L3_DATA<7>	T16	L3D7
36 8	L3_DATA<8>	W20	L3D8
36 8	L3_DATA<9>	U18	L3D9
36 8	L3_DATA<10>	Y22	L3D10
36 8	L3_DATA<11>	R16	L3D11
36 8	L3_DATA<12>	V20	L3D12
36 8	L3_DATA<13>	W22	L3D13
36 8	L3_DATA<14>	T18	L3D14
36 8	L3_DATA<15>	U20	L3D15
36 8	L3_DATA<16>	N18	L3D16
36 8	L3_DATA<17>	N20	L3D17
36 8	L3_DATA<18>	N16	L3D18
36 8	L3_DATA<19>	N22	L3D19
36 8	L3_DATA<20>	M16	L3D20
36 8	L3_DATA<21>	M18	L3D21
36 8	L3_DATA<22>	M20	L3D22
36 8	L3_DATA<23>	M22	L3D23
36 8	L3_DATA<24>	R18	L3D24
36 8	L3_DATA<25>	T20	L3D25
36 8	L3_DATA<26>	U22	L3D26
36 8	L3_DATA<27>	T22	L3D27
36 8	L3_DATA<28>	R20	L3D28
36 8	L3_DATA<29>	P18	L3D29
36 8	L3_DATA<30>	R22	L3D30
36 8	L3_DATA<31>	M15	L3D31
36 8	L3_DATA<32>	G18	L3D32
36 8	L3_DATA<33>	D22	L3D33
36 8	L3_DATA<34>	E20	L3D34
36 8	L3_DATA<35>	H16	L3D35
36 8	L3_DATA<36>	C22	L3D36
36 8	L3_DATA<37>	F18	L3D37
36 8	L3_DATA<38>	D20	L3D38
36 8	L3_DATA<39>	B22	L3D39
36 8	L3_DATA<40>	G16	L3D40
36 8	L3_DATA<41>	A21	L3D41
36 8	L3_DATA<42>	G15	L3D42
36 8	L3_DATA<43>	E17	L3D43
36 8	L3_DATA<44>	A20	L3D44
36 8	L3_DATA<45>	C19	L3D45
36 8	L3_DATA<46>	C18	L3D46
36 8	L3_DATA<47>	A19	L3D47
36 8	L3_DATA<48>	A18	L3D48
36 8	L3_DATA<49>	G14	L3D49
36 8	L3_DATA<50>	E15	L3D50
36 8	L3_DATA<51>	C16	L3D51
36 8	L3_DATA<52>	A17	L3D52
36 8	L3_DATA<53>	A16	L3D53
36 8	L3_DATA<54>	C15	L3D54
36 8	L3_DATA<55>	G13	L3D55
36 8	L3_DATA<56>	C14	L3D56
36 8	L3_DATA<57>	A14	L3D57
36 8	L3_DATA<58>	E13	L3D58
36 8	L3_DATA<59>	C13	L3D59
36 8	L3_DATA<60>	G12	L3D60
36 8	L3_DATA<61>	A13	L3D61
36 8	L3_DATA<62>	E12	L3D62
36 8	L3_DATA<63>	C12	L3D63
NC	AB19		L3DP0
NC	AA22		L3DP1
NC	P22		L3DP2
NC	P16		L3DP3
NC	C20		L3DP4
NC	E16		L3DP5
NC	A15		L3DP6
NC	A12		L3DP7

A22 B14 B16 B18 B20 C21 C17 D15 D19 F13 F14 F16 F19 G17 G21 H13 H15 H18 J17 J21 K15 K19 L13 L21 M19 N17 N21 P19 R17 R21 T15 T19 U17 U21 V15 V19 W17 W21 AB22

GND

L3 DECOUPLING CAPS

PLACE 1 EACH NEAR PINS B15, D12, E19, F15, H17, K17, M19, R15, T17, AND V21 OF CPU

38 8 6 L3_OVDD

C237	0.1UF	20% 10V CERM	402
C297	0.1UF	20% 10V CERM	402
C290	0.1UF	20% 10V CERM	402
C265	0.1UF	20% 10V CERM	402
C236	0.1UF	20% 10V CERM	402
C296	0.1UF	20% 10V CERM	402
C179	0.1UF	20% 10V CERM	402
C266	0.1UF	20% 10V CERM	402
C171	0.1UF	20% 10V CERM	402
C295	0.1UF	20% 10V CERM	402

L3VSEL A4 CPU_L3_VSEL 7

L3CLK0 V22 L3_CLK<0> 8 36
L3CLK1 C17 L3_CLK<1> 8 36

L3CNTL0* L20 L3_CNTL<0> 8 36
L3CNTL1* L22 L3_CNTL<1> 8 36

L3ECHO_CLK0 V18 L3_ECHO_CLK<0> 8 36
L3ECHO_CLK1 P20 L3_ECHO_CLK<1> 8 36
L3ECHO_CLK2 E18 L3_ECHO_CLK<2> 8 36
L3ECHO_CLK3 E14 L3_ECHO_CLK<3> 8 36

L3_OVDD GENERATOR

THIS LDO WAS ADDED TO SUPPORT SCHMOO'ING OF L3_OVDD VOLTAGE

LDO OUTPUTS 1.41V (SAME AS P59)

+1_8V_SLEEP
+2_5V_SLEEP
+1_5V_SLEEP

NO STUFF R609 0 5% 1/16W MF 603
NO STUFF R627 0 5% 1/16W MF 603
NO STUFF R649 0 5% 1/16W MF 603
NO STUFF R640 0 5% 1/16W MF 603

38 LTC1962_L3_VOUT
38 LTC1962_L3_VIN
39 LTC1962_L3_ADJ
LT1962_L3_BYP

NO STUFF U47 LT1962-ADJ MSOP
IN 8
NC 7
NC 6
SHDN 5
OUT 1
ADJ 2
BYP 3
GND 4

NO STUFF C659 1UF 20% 10V CERM 603
NO STUFF C679 0.01UF 20% 10V CERM 402
NO STUFF C673 10UF 20% 6.3V CERM 805
NO STUFF R639 10.7K 1% 1/16W MF 402
NO STUFF R644 68.1K 1% 1/16W MF 402

L3_OVDD 6 8 38

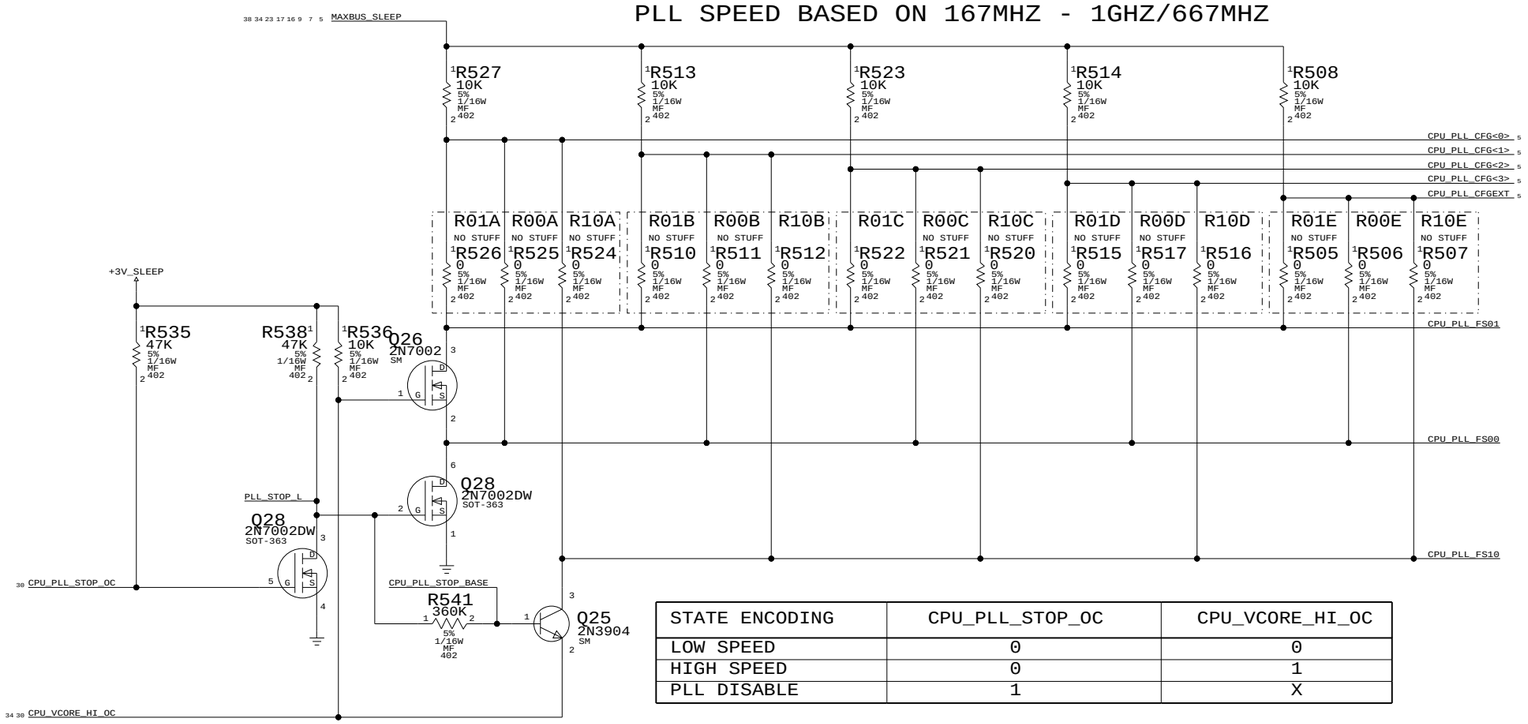
MPC7450 - L3

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6469	E
SCALE: NONE	SHT 6 OF 44	

CPU PLL CONFIG CIRCUITRY

PLL SPEED BASED ON 167MHZ - 1GHZ/667MHZ



STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

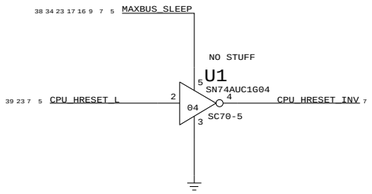
CPU FREQUENCY CONFIGURATION

APOLLO REV 3.0

MULTIPLIER	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ	133MHZ	CPU_PLL_CFG
(Bus-to-Core)	(MHZ)		E ABCD HEX
0.0X	PLL OFF		0 1111 0F
1.0X	PLL BYPASS		0 0011 03
2.0X	333	267	0 0100 04
3.0X	500	400	0 1000 08
4.0X	667	533	0 1010 0A
5.0X	833	667	0 1011 0B
5.5X	917	733	0 1001 09
6.0X	1000	800	0 1101 0D
6.5X	1083	867	0 0101 05
7.0X	1167	933	0 0010 02
7.5X	1250	1000	0 0001 01
8.0X	1333	1067	0 1100 0C
8.5X	1417	1133	0 0110 06
9.0X	1500	1200	1 0111 17
9.5X	1583	1267	0 0111 07
10.0X	1667	1333	1 1010 1A
10.5X	1750	1400	1 1000 18
11.0X	1833	1467	1 1001 19
11.5X	1917	1533	0 0000 00
12.0X	2000	1600	1 1011 1B
12.5X	2083	1667	1 1111 1F
13.0X	2167	1733	1 0101 15
13.5X	2250	1800	0 1110 0E
14.0X	2333	1867	1 1100 1C
15.0X	2500	2000	1 0001 11
16.0X	2667	2133	1 1101 1D
17.0X	2833	2267	1 0000 10
18.0X	3000	2400	1 0010 12
20.0X	3333	2667	1 0011 13
21.0X	3500	2800	1 0100 14
24.0X	4000	3200	1 0110 16
28.0X	4667	3733	1 1110 1E

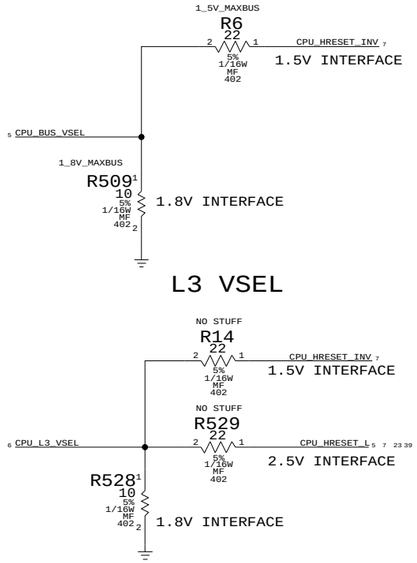
CPU CONFIGURATION

INVERTED HRESET_L



DESKTOP HAD PROBLEM USING
INVERTER TO INVERT HRESET_L
NEED TO CHARACTERIZE

MAXBUS VSEL



BUSTYPE SELECT

APOLLO ONLY SUPPORTS MAXBUS

L3 VSEL

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE
CPU_L3_VSEL (PROCESSOR)	CPU_HRESET_L or INT. PU	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

CPU CONFIGURATION

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6469	E
SCALE: NONE	SHT 7 OF 44	

L3 REFERENCE VOLTAGE

RP45 10K 5% 1/16W SM1
1 L3_DQPA<0> 8
2 L3_DQPB<0> 8
4 L3_DQPC<0> 8
3 L3_DQPD<0> 8

RP46 10K 5% 1/16W SM1
1 L3_DQPA<1> 8
2 L3_DQPB<1> 8
4 L3_DQPC<1> 8
3 L3_DQPD<1> 8

R624 470 5% 1/16W MF 402
1 L3_PULLDOWN<0> 8

R625 470 5% 1/16W MF 402
1 L3_PULLDOWN<1> 8

R641 1K 5% 1/16W MF 402
1 JTAG_L3_TCK 8 39

+2_5V_SLEEP

L3_OVDD 6 8 38

VDD: F5 F7 G5 G7 H5 H7 J5 J7 K5 K7 E4
VDDQ: E8 F4 F8 G4 G8 H3 H4 H8 H9 J4 J8 K4 K8 L4 L8

Addr lines swappable within a SRAM (except ADDR<0..1>)

CRITICAL
U7
300MHZ-128KX36
BGA

L3_ADDR<0> 36 8 6	C6	SA0	
L3_ADDR<1> 36 8 6	C7	SA1	
L3_ADDR<12> 36 8 6	B4	SA2	
L3_ADDR<11> 36 8 6	B8	SA3	
L3_ADDR<13> 36 8 6	C5	SA4	
L3_ADDR<10> 36 8 6	N6	SA5	
L3_ADDR<7> 36 8 6	P4	SA6	
L3_ADDR<6> 36 8 6	P5	SA7	
L3_ADDR<8> 36 8 6	P7	SA8	
L3_ADDR<16> 36 8 6	P8	SA9	
L3_ADDR<14> 36 8 6	A9	SA10	
L3_ADDR<5> 36 8 6	R4	SA11	
L3_ADDR<3> 36 8 6	R5	SA12	
L3_ADDR<4> 36 8 6	R7	SA13	
L3_ADDR<9> 36 8 6	R8	SA14	
L3_ADDR<2> 36 8 6	R9	SA15	
L3_ADDR<15> 36 8 6	A3	SA16	
L3_ADDR<17> 36 8 6	R3	NC/SA17	BALL R3 IS NC ON 4MBIT PART HAVE TO CONNECT L3_ADDR17 TO THIS PIN
L3_PULLDOWN<0> 8	R6	LBO*	
L3_CNTL<0> 36 8 6	A4	B1	
L3_CNTL<1> 36 8 6	A8	B2	
L3_PULLDOWN<0> 8	P6	B3	
L3_PULLDOWN<0> 8	H1	G*	
L3_ECHO_CLK<0> 36 6	M2	CQ1	
NC	E2	CQ1*	
L3_ECHO_CLK<1> 36 6	L10	CQ2	
NC	D10	CQ2*	
L3_VREF 38 8	H2	VREF1	
	H10	VREF2	
JTAG_L3_TMS 39 8	R10	TMS	
JTAG_L3_TDI_TP 39	R11	TDI	
JTAG_L3_SRAM2_TDI 8	R1	TDO	
JTAG_L3_TCK 39 8	R2	TCK	
NC	A1	NC_A1	
NC	A2	NC_A2	
NC	A5	NC_A5	
NC	A7	NC_A7	
NC	A10	NC_A10	
NC	A11	NC_A11	
NC	B1	NC_B1	
NC	B5	NC_B5	
NC	B7	NC_B7	
NC	B9	NC_B9	
NC	B10	NC_B10	
NC	C1	NC_C1	
NC	C2	NC_C2	
NC	C9	NC_C9	
NC	D1	NC_D1	
NC	D9	NC_D9	
NC	E1	NC_E1	
NC	E9	NC_E9	
NC	F1	NC_F1	
	F9	NC_F9	
NC F10		NC_F10	
NC G1		NC_G1	

	B6	K	L3_CLK<0> 6 36
	A6	K*	L3_CLK_REF 8 38
	H11	ZQ	L3_ZQ<0>
DQ0	P10	DQ0	L3_DATA<5> 6 36
DQ1	P11	DQ1	L3_DATA<1> 6 36
DQ2	N11	DQ2	L3_DATA<0> 6 36
DQ3	M10	DQ3	L3_DATA<6> 6 36
DQ4	M11	DQ4	L3_DATA<4> 6 36
DQ5	L11	DQ5	L3_DATA<3> 6 36
DQ6	K10	DQ6	L3_DATA<9> 6 36
DQ7	K11	DQ7	L3_DATA<2> 6 36
DQ8	J11	DQ8	L3_DATA<7> 6 36
DQ9	J10	DQ9	L3_DATA<14> 6 36
DQ10	G11	DQ10	L3_DATA<11> 6 36
DQ11	F11	DQ11	L3_DATA<24> 6 36
DQ12	E10	DQ12	L3_DATA<29> 6 36
DQ13	E11	DQ13	L3_DATA<16> 6 36
DQ14	D11	DQ14	L3_DATA<18> 6 36
DQ15	C10	DQ15	L3_DATA<21> 6 36
DQ16	C11	DQ16	L3_DATA<20> 6 36
DQ17	B11	DQ17	L3_DATA<31> 6 36
DQ18	B3	DQ18	L3_DATA<22> 6 36
DQ19	B2	DQ19	L3_DATA<23> 6 36
DQ20	C3	DQ20	L3_DATA<17> 6 36
DQ21	D3	DQ21	L3_DATA<30> 6 36
DQ22	D2	DQ22	L3_DATA<19> 6 36
DQ23	E3	DQ23	L3_DATA<28> 6 36
DQ24	F3	DQ24	L3_DATA<25> 6 36
DQ25	F2	DQ25	L3_DATA<27> 6 36
DQ26	G2	DQ26	L3_DATA<26> 6 36
DQ27	G3	DQ27	L3_DATA<15> 6 36
DQ28	J3	DQ28	L3_DATA<12> 6 36
DQ29	K3	DQ29	L3_DATA<8> 6 36
DQ30	L3	DQ30	L3_DATA<13> 6 36
DQ31	L2	DQ31	L3_DATA<10> 6 36
DQ32	M3	DQ32	L3_DQPA<0> 8
DQ33	N3	DQ33	L3_DQPB<0> 8
DQ34	N2	DQ34	L3_DQPC<0> 8
DQ35	P3	DQ35	L3_DQPD<0> 8
NC_P9	P9	NC_P9	NC
NC_P2	P2	NC_P2	NC
NC_P1	P1	NC_P1	NC
NC_N10	N10	NC_N10	NC
NC_N9	N9	NC_N9	NC
NC_N7	N7	NC_N7	NC
NC_N5	N5	NC_N5	NC
NC_N1	N1	NC_N1	NC
NC_M9	M9	NC_M9	NC
NC_M1	M1	NC_M1	NC
NC_L9	L9	NC_L9	NC
NC_L1	L1	NC_L1	NC
NC_K9	K9	NC_K9	
NC_K2	K2	NC_K2	NC
NC_K1	K1	NC_K1	NC
NC_J9	J9	NC_J9	NC
NC_J2	J2	NC_J2	NC
NC_J1	J1	NC_J1	NC
NC_G10	G10	NC_G10	NC
NC_G9	G9	NC_G9	NC

VSS: C4 C8 D4 D5 D6 D7 D8 E5 E6 E7 F6 G5 H6 J6 K6 L5 L6 L7 M4 M5 M6 M7 M8 N4 N8

1R616 249 1% 1/16W MF 402 2

Data lines swappable within a SRAM

SAMSUNG VERIFIED THAT ALL NC PINS ARE NOT CONNECTED IN THE SUBSTRATE BALL F9, K9 CONNECTED TO GND SO BYPASS CAP CAN BE PLACED DIRECTLY UNDERNEATH THE CHIPS

+2_5V_SLEEP

L3_OVDD 6 8 38

VDD: F5 F7 G5 G7 H5 H7 J5 J7 K5 K7 E4
VDDQ: E8 F4 F8 G4 G8 H3 H4 H8 H9 J4 J8 K4 K8 L4 L8

CRITICAL
U6
300MHZ-128KX36
BGA

L3_ADDR<0> 36 8 6	C6	SA0	
L3_ADDR<1> 36 8 6	C7	SA1	
L3_ADDR<12> 36 8 6	B4	SA2	
L3_ADDR<11> 36 8 6	B8	SA3	
L3_ADDR<13> 36 8 6	C5	SA4	
L3_ADDR<10> 36 8 6	N6	SA5	
L3_ADDR<7> 36 8 6	P4	SA6	
L3_ADDR<6> 36 8 6	P5	SA7	
L3_ADDR<8> 36 8 6	P7	SA8	
L3_ADDR<16> 36 8 6	P8	SA9	
L3_ADDR<14> 36 8 6	A9	SA10	
L3_ADDR<5> 36 8 6	R4	SA11	
L3_ADDR<3> 36 8 6	R5	SA12	
L3_ADDR<4> 36 8 6	R7	SA13	
L3_ADDR<9> 36 8 6	R8	SA14	
L3_ADDR<2> 36 8 6	R9	SA15	
L3_ADDR<15> 36 8 6	A3	SA16	
L3_ADDR<17> 36 8 6	R3	NC/SA17	BALL R3 IS NC ON 4MBIT PART HAVE TO CONNECT L3_ADDR17 TO THIS PIN
L3_PULLDOWN<1> 8	R6	LBO*	
L3_CNTL<0> 36 8 6	A4	B1	
L3_CNTL<1> 36 8 6	A8	B2	
L3_PULLDOWN<1> 8	P6	B3	
L3_PULLDOWN<1> 8	H1	G*	
L3_ECHO_CLK<2> 36 6	M2	CQ1	
NC	E2	CQ1*	
L3_ECHO_CLK<3> 36 6	L10	CQ2	
NC	D10	CQ2*	
L3_VREF 38 8	H2	VREF1	
	H10	VREF2	
JTAG_L3_TMS 39 8	R10	TMS	
JTAG_L3_SRAM2_TDI 8	R11	TDI	
JTAG_L3_TDO_TP 39	R1	TDO	
JTAG_L3_TCK 39 8	R2	TCK	
NC	A1	NC_A1	
NC	A2	NC_A2	
NC	A5	NC_A5	
NC	A7	NC_A7	
NC	A10	NC_A10	
NC	A11	NC_A11	
NC	B1	NC_B1	
NC	B5	NC_B5	
NC	B7	NC_B7	
NC	B9	NC_B9	
NC	B10	NC_B10	
NC	C1	NC_C1	
NC	C2	NC_C2	
NC	C9	NC_C9	
NC	D1	NC_D1	
NC	D9	NC_D9	
NC	E1	NC_E1	
NC	E9	NC_E9	
NC	F1	NC_F1	
	F9	NC_F9	
NC F10		NC_F10	
NC G1		NC_G1	

	B6	K	L3_CLK<1> 6 36
	A6	K*	L3_CLK_REF 8 38
	M11	ZQ	L3_ZQ<1>
DQ0	P10	DQ0	L3_DATA<35> 6 36
DQ1	P11	DQ1	L3_DATA<40> 6 36
DQ2	N11	DQ2	L3_DATA<42> 6 36
DQ3	M10	DQ3	L3_DATA<49> 6 36
DQ4	M11	DQ4	L3_DATA<55> 6 36
DQ5	L11	DQ5	L3_DATA<60> 6 36
DQ6	K10	DQ6	L3_DATA<43> 6 36
DQ7	K11	DQ7	L3_DATA<50> 6 36
DQ8	J11	DQ8	L3_DATA<62> 6 36
DQ9	J10	DQ9	L3_DATA<58> 6 36
DQ10	G11	DQ10	L3_DATA<51> 6 36
DQ11	F11	DQ11	L3_DATA<54> 6 36
DQ12	E10	DQ12	L3_DATA<56> 6 36
DQ13	E11	DQ13	L3_DATA<59> 6 36
DQ14	D11	DQ14	L3_DATA<63> 6 36
DQ15	C10	DQ15	L3_DATA<53> 6 36
DQ16	C11	DQ16	L3_DATA<57> 6 36
DQ17	B11	DQ17	L3_DATA<61> 6 36
DQ18	B3	DQ18	L3_DATA<52> 6 36
DQ19	B2	DQ19	L3_DATA<48> 6 36
DQ20	C3	DQ20	L3_DATA<47> 6 36
DQ21	D3	DQ21	L3_DATA<44> 6 36
DQ22	D2	DQ22	L3_DATA<41> 6 36
DQ23	E3	DQ23	L3_DATA<39> 6 36
DQ24	F3	DQ24	L3_DATA<46> 6 36
DQ25	F2	DQ25	L3_DATA<45> 6 36
DQ26	G2	DQ26	L3_DATA<36> 6 36
DQ27	G3	DQ27	L3_DATA<33> 6 36
DQ28	J3	DQ28	L3_DATA<38> 6 36
DQ29	K3	DQ29	L3_DATA<34> 6 36
DQ30	L3	DQ30	L3_DATA<37> 6 36
DQ31	L2	DQ31	L3_DATA<32> 6 36
DQ32	M3	DQ32	L3_DQPA<1> 8
DQ33	N3	DQ33	L3_DQPB<1> 8
DQ34	N2	DQ34	L3_DQPC<1> 8
DQ35	P3	DQ35	L3_DQPD<1> 8
NC_P9	P9	NC_P9	NC
NC_P2	P2	NC_P2	NC
NC_P1	P1	NC_P1	NC
NC_N10	N10	NC_N10	NC
NC_N9	N9	NC_N9	NC
NC_N7	N7	NC_N7	NC
NC_N5	N5	NC_N5	NC
NC_N1	N1	NC_N1	NC
NC_M9	M9	NC_M9	NC
NC_M1	M1	NC_M1	NC
NC_L9	L9	NC_L9	NC
NC_L1	L1	NC_L1	NC
NC_K9	K9	NC_K9	
NC_K2	K2	NC_K2	NC
NC_K1	K1	NC_K1	NC
NC_J9	J9	NC_J9	NC
NC_J2	J2	NC_J2	NC
NC_J1	J1	NC_J1	NC
NC_G10	G10	NC_G10	NC
NC_G9	G9	NC_G9	NC

VSS: C4 C8 D4 D5 D6 D7 D8 E5 E6 E7 F6 G6 H6 J6 K6 L5 L6 L7 M4 M5 M6 M7 M8 N4 N8

1R617 249 1% 1/16W MF 402 2

Data lines swappable within a SRAM

+2_5V_SLEEP

Split caps of same value evenly between SRAM chips

C654 C663 C662 C645 C648
C651 C666 C664 C667 C665
0.1UF 20% 10V CERM 402

+2_5V_SLEEP

Split caps of same value evenly between SRAM chips

C636 10UF 20% 6.3V CERM 805
C686 10UF 20% 6.3V CERM 805
C635 2.2UF 20% 10V CERM 805
C639 2.2UF 20% 10V CERM 805

L3_OVDD 38 8 6

Split caps of same value evenly between SRAM chips

C655 C650 C644 C671 C672
C649 C669 C674 C640 C641
C675 C630 C631 C638 C670
C653 C637 C647 C652 C646
0.1UF 20% 10V CERM 402

L3_OVDD 38 8 6

Split caps of same value evenly between SRAM chips

C661 10UF 20% 6.3V CERM 805
C642 10UF 20% 6.3V CERM 805
C687 2.2UF 20% 10V CERM 805
C684 2.2UF 20% 10V CERM 805

L3 CACHE

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6469	E
SCALE: NONE	SHT 8 OF 44	

INTREPID BOOT STRAPS

BIT 32 TO 39

38 34 23 17 16 9 7 5 MAXBUS_SLEEP

NO STUFF R557[1] 10K 5% 1/16W MF 402[2]	NO STUFF R96[1] 10K 5% 1/16W MF 402[2]	NO STUFF R87[1] 10K 5% 1/16W MF 402[2]	NO STUFF R111[1] 10K 5% 1/16W MF 402[2]	NO STUFF R121[1] 10K 5% 1/16W MF 402[2]	NO STUFF R134[1] 10K 5% 1/16W MF 402[2]	NO STUFF R565[1] 10K 5% 1/16W MF 402[2]	NO STUFF R133[1] 10K 5% 1/16W MF 402[2]
36 9 6 CPU_DATA<32>	36 9 6 CPU_DATA<33>	36 9 6 CPU_DATA<34>	36 9 6 CPU_DATA<35>	36 9 6 CPU_DATA<36>	36 9 6 CPU_DATA<37>	36 9 6 CPU_DATA<38>	36 9 6 CPU_DATA<39>
R97[1] 10K 5% 1/16W MF 402[2]	R558[1] 10K 5% 1/16W MF 402[2]	R554[1] 10K 5% 1/16W MF 402[2]	R571[1] 10K 5% 1/16W MF 402[2]	R578[1] 10K 5% 1/16W MF 402[2]	R586[1] 10K 5% 1/16W MF 402[2]	R103[1] 10K 5% 1/16W MF 402[2]	R587[1] 10K 5% 1/16W MF 402[2]
DDR_TPOMODEENABLE_h 0: TDI input 1: TDI output (JTAG)	Analyzerclk_En_h 0: Inactive 1: Active	Pcie_PLL_SSCon_Pol 0: Active high 1: Active low	IntrePLL_SSCon_Pol 0: Active high 1: Active low	Spare	Spare	Spare	Spare

BIT 40 TO 47

38 34 23 17 16 9 7 5 MAXBUS_SLEEP

NO STUFF R86[1] 10K 5% 1/16W MF 402[2]	NO STUFF R102[1] 10K 5% 1/16W MF 402[2]	NO STUFF R119[1] 10K 5% 1/16W MF 402[2]	NO STUFF R95[1] 10K 5% 1/16W MF 402[2]	NO STUFF R139[1] 10K 5% 1/16W MF 402[2]	NO_SSCG R132[1] 10K 5% 1/16W MF 402[2]	R110[1] 10K 5% 1/16W MF 402[2]	R120[1] 10K 5% 1/16W MF 402[2]
36 9 6 CPU_DATA<40>	36 9 6 CPU_DATA<41>	36 9 6 CPU_DATA<42>	36 9 6 CPU_DATA<43>	36 9 6 CPU_DATA<44>	36 9 6 CPU_DATA<45>	36 9 6 CPU_DATA<46>	36 9 6 CPU_DATA<47>
R555[1] 10K 5% 1/16W MF 402[2]	R566[1] 10K 5% 1/16W MF 402[2]	R579[1] 10K 5% 1/16W MF 402[2]	R559[1] 10K 5% 1/16W MF 402[2]	R595[1] 10K 5% 1/16W MF 402[2]	SSCG R588[1] 10K 5% 1/16W MF 402[2]	NO STUFF R572[1] 10K 5% 1/16W MF 402[2]	NO STUFF R580[1] 10K 5% 1/16W MF 402[2]
Spare	Spare	BIT2	BIT1	BIT0	Internalspreaden 1: Active	PCI1 Source Clock 0: PLL4 (NO SPREAD)	PCI0 Source Clock 0: PLL5 (NO SPREAD)

PLL4MODESEL_NXT[2:0]
000: 166.4MHZ (2.5X)
001: 149.76MHZ
010: 133.12MHZ (2.0X)
011: 99.84MHZ (1.5X)
100: 83.20MHZ

MODE A (2.5X) IS FOR STATIC OPERATION
MODE C (2.0X) IS FOR CLOCK SLEW OPERATION

BIT 48 TO 55

38 34 23 17 16 9 7 5 MAXBUS_SLEEP

SSCG R94[1] 10K 5% 1/16W MF 402[2]	SSCG R85[1] 10K 5% 1/16W MF 402[2]	NO STUFF R118[1] 10K 5% 1/16W MF 402[2]	NO STUFF R109[1] 10K 5% 1/16W MF 402[2]	NO STUFF R117[1] 10K 5% 1/16W MF 402[2]	NO STUFF R101[1] 10K 5% 1/16W MF 402[2]	NO STUFF R138[1] 10K 5% 1/16W MF 402[2]	NO STUFF R131[1] 10K 5% 1/16W MF 402[2]
36 9 6 CPU_DATA<48>	36 9 6 CPU_DATA<49>	36 9 6 CPU_DATA<50>	36 9 6 CPU_DATA<51>	36 9 6 CPU_DATA<52>	36 9 6 CPU_DATA<53>	36 9 6 CPU_DATA<54>	36 9 6 CPU_DATA<55>
NO_SSCG R560[1] 10K 5% 1/16W MF 402[2]	NO_SSCG R556[1] 10K 5% 1/16W MF 402[2]	NO STUFF R582[1] 10K 5% 1/16W MF 402[2]	R573[1] 10K 5% 1/16W MF 402[2]	R581[1] 10K 5% 1/16W MF 402[2]	R567[1] 10K 5% 1/16W MF 402[2]	NO STUFF R596[1] 10K 5% 1/16W MF 402[2]	R589[1] 10K 5% 1/16W MF 402[2]
BUF_REF_CLK_OUTEnable_h 1: Active	Spread_PLL4ExtSrc 1: External source	Spare	TI 1394b workaround 1: TI PHY workaround	BIT2	BIT1	BIT0	Spare

MaxBus output impedance
111: 28.6 ohm
011: 33.3 ohm
101: 40 ohm
001: 50 ohm
110: 66.6 ohm
010: 100 ohm
100: 200 ohm
000: 200 ohm

THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:

1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
2/ D46 - SELPCI1SPREADCLK - SLEEP/WAKE CYCLE REQUIRED
3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT

IF A STRAP IS NOT LISTED, THEN
IT CANNOT BE CHANGED BY SOFTWARE

38 15 13 +1_5V_INTREPID_PLL — R178 4.7 5% 1/10W MF 402 — 38 +1_5V_INTREPID_PLL7

C291 0.22UF 20% 6.3V CERM 402

H26 VDD15A_7 (PLL6)

CRITICAL

U44 INTREPID-REV2.1 BGA

(1 OF 9)

36 9 5 CPU_BR_L	E29	BR	INPUT
36 9 5 CPU_BG_L	E26	BG	NO BUS KEEPER
36 9 5 CPU_TS_L	B27	TS	NO BUS KEEPER
36 5 CPU_ADDR<0>	D24	A_0	
36 5 CPU_ADDR<1>	D25	A_1	
36 5 CPU_ADDR<2>	A27	A_2	
36 5 CPU_ADDR<3>	E24	A_3	
36 5 CPU_ADDR<4>	G23	A_4	
36 5 CPU_ADDR<5>	B26	A_5	
36 5 CPU_ADDR<6>	A26	A_6	
36 5 CPU_ADDR<7>	D23	A_7	
36 5 CPU_ADDR<8>	A25	A_8	
36 5 CPU_ADDR<9>	E23	A_9	
36 5 CPU_ADDR<10>	J22	A_10	
36 5 CPU_ADDR<11>	B25	A_11	
36 5 CPU_ADDR<12>	H22	A_12	
36 5 CPU_ADDR<13>	G22	A_13	
36 5 CPU_ADDR<14>	D22	A_14	
36 5 CPU_ADDR<15>	B24	A_15	
36 5 CPU_ADDR<16>	B23	A_16	
36 5 CPU_ADDR<17>	E22	A_17	
36 5 CPU_ADDR<18>	J21	A_18	
36 5 CPU_ADDR<19>	G21	A_19	
36 5 CPU_ADDR<20>	E21	A_20	
36 5 CPU_ADDR<21>	A24	A_21	
36 5 CPU_ADDR<22>	D21	A_22	
36 5 CPU_ADDR<23>	A23	A_23	
36 5 CPU_ADDR<24>	H20	A_24	
36 5 CPU_ADDR<25>	B22	A_25	
36 5 CPU_ADDR<26>	H21	A_26	
36 5 CPU_ADDR<27>	A22	A_27	
36 5 CPU_ADDR<28>	E20	A_28	
36 5 CPU_ADDR<29>	B21	A_29	
36 5 CPU_ADDR<30>	D20	A_30	
36 5 CPU_ADDR<31>	A21	A_31	
36 5 CPU_CI_L	G26	CI	
36 5 CPU_GBL_L	A29	GBL	
36 5 CPU_TBST_L	A28	TBST	
36 5 CPU_TSIZ<0>	G24	TSIZ_0	
36 5 CPU_TSIZ<1>	H24	TSIZ_1	
36 5 CPU_TSIZ<2>	D26	TSIZ_2	
36 5 CPU_TT<0>	E25	TT_0	
36 5 CPU_TT<1>	G25	TT_1	
36 5 CPU_TT<2>	B28	TT_2	
36 5 CPU_TT<3>	D27	TT_3	
36 5 CPU_TT<4>	J25	TT_4	
36 5 CPU_WT_L	D28	WT	
36 9 5 CPU_AACK_L	B29	AACK	NO BUS KEEPER - PU
36 9 5 CPU_ARTRY_L	H23	ARTRY	NO BUS KEEPER - PU
36 9 5 CPU_HIT_L	B31	HIT	INPUT - PU
36 9 5 CPU_QREQ_L	A32	QREQ	INPUT - PD
36 5 CPU_QACK_L	G27	QACK	NO BUS KEEPER - ?
30 INT_SUSPEND_REQ_L	AK9	SUSPENDREQ	
30 INT_SUSPEND_ACK_L	AM8	SUSPENDACK	
		CPU_FB_IN	Vin = Intrepid Vcore (1.5V) Vout = MaxBus rail (1.8V)
		CPU_FB_OUT	NO BUS KEEPER - PU
		ANALYZER_CLK	
30 CPU_CLK_EN	AH9	STOPCPUCLK	INPUT - PU
INTREPID_ACS_REF	H13	ACS_REF	NO BUS KEEPER - ?
36 SYSCLK_CPU_UF	J15	CPU_CLK	NO BUS KEEPER - PU
5 CPU_TBEN	A31	TBEN	NO BUS KEEPER - PU
		VSSA_7 (PLL6)	H25

MAXBUS INTERFACE

D_0	D10	CPU_DATA<0>	6 36
D_1	G12	CPU_DATA<1>	6 36
D_2	E11	CPU_DATA<2>	6 36
D_3	H11	CPU_DATA<3>	6 36
D_4	B9	CPU_DATA<4>	6 36
D_5	B8	CPU_DATA<5>	6 36
D_6	A9	CPU_DATA<6>	6 36
D_7	A8	CPU_DATA<7>	6 36
D_8	E12	CPU_DATA<8>	6 36
D_9	D11	CPU_DATA<9>	6 36
D_10	B10	CPU_DATA<10>	6 36
D_11	J13	CPU_DATA<11>	6 36
D_12	A10	CPU_DATA<12>	6 36
D_13	D12	CPU_DATA<13>	6 36
D_14	E13	CPU_DATA<14>	6 36
D_15	G13	CPU_DATA<15>	6 36
D_16	B11	CPU_DATA<16>	6 36
D_17	D13	CPU_DATA<17>	6 36
D_18	A11	CPU_DATA<18>	6 36
D_19	G14	CPU_DATA<19>	6 36
D_20	H14	CPU_DATA<20>	6 36
D_21	E14	CPU_DATA<21>	6 36
D_22	B12	CPU_DATA<22>	6 36
D_23	G15	CPU_DATA<23>	6 36
D_24	B13	CPU_DATA<24>	6 36
D_25	H15	CPU_DATA<25>	6 36
D_26	D14	CPU_DATA<26>	6 36
D_27	B14	CPU_DATA<27>	6 36
D_28	A12	CPU_DATA<28>	6 36
D_29	G16	CPU_DATA<29>	6 36
D_30	E15	CPU_DATA<30>	6 36
D_31	J16	CPU_DATA<31>	6 36
D_32	D15	CPU_DATA<32>	6 9 36
D_33	A14	CPU_DATA<33>	6 9 36
D_34	A13	CPU_DATA<34>	6 9 36
D_35	D16	CPU_DATA<35>	6 9 36
D_36	E16	CPU_DATA<36>	6 9 36
D_37	G17	CPU_DATA<37>	6 9 36
D_38	B15	CPU_DATA<38>	6 9 36
D_39	H17	CPU_DATA<39>	6 9 36
D_40	A15	CPU_DATA<40>	6 9 36
D_41	B16	CPU_DATA<41>	6 9 36
D_42	E17	CPU_DATA<42>	6 9 36
D_43	A16	CPU_DATA<43>	6 9 36
D_44	J18	CPU_DATA<44>	6 9 36
D_45	H18	CPU_DATA<45>	6 9 36
D_46	D17	CPU_DATA<46>	6 9 36
D_47	G18	CPU_DATA<47>	6 9 36
D_48	A17	CPU_DATA<48>	6 9 36
D_49	B17	CPU_DATA<49>	6 9 36
D_50	E18	CPU_DATA<50>	6 9 36
D_51	B18	CPU_DATA<51>	6 9 36
D_52	D18	CPU_DATA<52>	6 9 36
D_53	A18	CPU_DATA<53>	6 9 36
D_54	A19	CPU_DATA<54>	6 9 36
D_55	H19	CPU_DATA<55>	6 9 36
D_56	B19	CPU_DATA<56>	6 9 36
D_57	J19	CPU_DATA<57>	6 9 36
D_58	A20	CPU_DATA<58>	6 9 36
D_59	D19	CPU_DATA<59>	6 9 36
D_60	E19	CPU_DATA<60>	6 9 36
D_61	G19	CPU_DATA<61>	6 9 36
D_62	B20	CPU_DATA<62>	6 9 36
D_63	G20	CPU_DATA<63>	6 9 36
DBG	A30	CPU_DBG_L	5 9 36
DRDY	G28	CPU_DRDY_L	5 9 36
DTI_0	K25	CPU_DTI<0>	5 36
DTI_1	D29	CPU_DTI<1>	5 36
DTI_2	B30	CPU_DTI<2>	5 36
TA	E27	CPU_TA_L	5 9 36
TEA	E28	CPU_TEA_L	5 9 36

FB BUFFER HAS 50 OHM OUTPUT IMPEDANCE

R152[1] 511 1% 1/16W MF 402[2]

R104 0 5% 1/16W MF 402

36 5 SYSCLK_CPU — 1 — 2 — 36 SYSCLK_CPU_UF

R98[1] 1K 1% 1/16W MF 402[2]

INTREPID OUTPUTS HIGH BY DEFAULT

SHORT = 1" SHORTER THAN MATCHED LENGTH

R122 0 5% 1/16W MF 402

36 9 INT_CPUFB_OUT — 36 INT_CPUFB_OUT_SHORT

R168 0 5% 1/16W MF 402

36 INT_CPUFB_OUT_NORM

LONG = 1" LONGER THAN MATCHED LENGTH

NO STUFF R161 0 5% 1/16W MF 402

36 INT_CPUFB_LONG

NO STUFF R176[1] 0 5% 1/16W MF 402[2]

R177 0 5% 1/16W MF 402

36 9 INT_CPUFB_IN

R162[1] 0 5% 1/16W MF 402[2]

NO STUFF R151 0 5% 1/16W MF 402

36 INT_CPUFB_IN_NORM

MAXBUS PULL-UPS

MAXBUS_SLEEP 5 7 9 16 17 23 34 38

RP22 10K 5% 1/16W SM1	RP22 10K 5% 1/16W SM1	RP22 10K 5% 1/16W SM1	RP24 10K 5% 1/16W SM1
36 9 5 CPU_TS_L	36 9 5 CPU_TA_L	36 9 5 CPU_ARTRY_L	36 9 5 CPU_BR_L
RP25 10K 5% 1/16W SM1	RP24 10K 5% 1/16W SM1	RP24 10K 5% 1/16W SM1	RP24 10K 5% 1/16W SM1
36 9 5 CPU_HIT_L	36 9 5 CPU_DRDY_L	36 9 5 CPU_TEA_L	36 9 5 CPU_AACK_L
RP25 10K 5% 1/16W SM1	RP22 10K 5% 1/16W SM1	RP25 10K 5% 1/16W SM1	
36 9 5 CPU_DBG_L	36 9 5 CPU_BG_L	36 9 5 CPU_QREQ_L	

INTREPID BOOT STRAPS

BIT 56 TO 63

38 34 23 17 16 9 7 5 MAXBUS_SLEEP

NO STUFF R100[1] 10K 5% 1/16W MF 402[2]	NO STUFF R116[1] 10K 5% 1/16W MF 402[2]	NO STUFF R130[1] 10K 5% 1/16W MF 402[2]	NO STUFF R93[1] 10K 5% 1/16W MF 402[2]	NO STUFF R92[1] 10K 5% 1/16W MF 402[2]	NO STUFF R108[1] 10K 5% 1/16W MF 402[2]	R129[1] 10K 5% 1/16W MF 402[2]	NO STUFF R137[1] 10K 5% 1/16W MF 402[2]
36 9 6 CPU_DATA<56>	36 9 6 CPU_DATA<57>	36 9 6 CPU_DATA<58>	36 9 6 CPU_DATA<59>	36 9 6 CPU_DATA<60>	36 9 6 CPU_DATA<61>	36 9 6 CPU_DATA<62>	36 9 6 CPU_DATA<63>
R568[1] 10K 5% 1/16W MF 402[2]	R583[1] 10K 5% 1/16W MF 402[2]	R590[1] 10K 5% 1/16W MF 402[2]	R561[1] 10K 5% 1/16W MF 402[2]	R562[1] 10K 5% 1/16W MF 402[2]	R574[1] 10K 5% 1/16W MF 402[2]	NO STUFF R591[1] 10K 5% 1/16W MF 402[2]	R597[1] 10K 5% 1/16W MF 402[2]
Spare	Spare	Spare	PCI1_REQ2_L / PCI1_GNT2_L 0: GPIO 1: GPIO_OUT	PCI1_REQ1_L / PCI1_GNT1_L 0: GPIO 1: GPIO	PCI1_REQ0_L / PCI1_GNT0_L 0: GPIO 1: GPIO	61 remote PHY interface 0: B-MODE interface	Processor Bus Mode 0: 4x Bus (G3) 1: 8x Bus (G4)

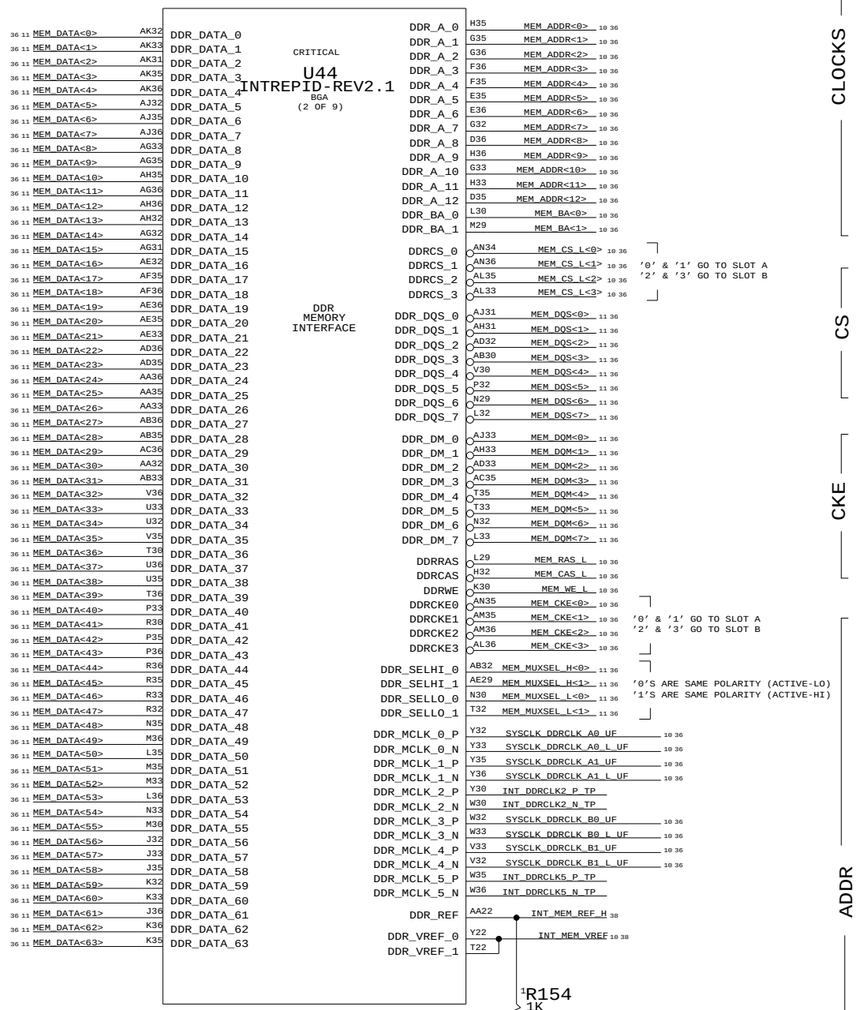
Intrepid MaxBus

APPLE COMPUTER INC.

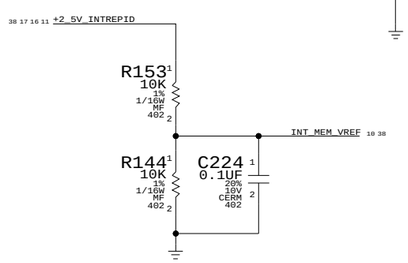
SIZE	DRAWING NUMBER	REV.
D	051-6469	E
SCALE: NONE	SHT 9 OF 44	

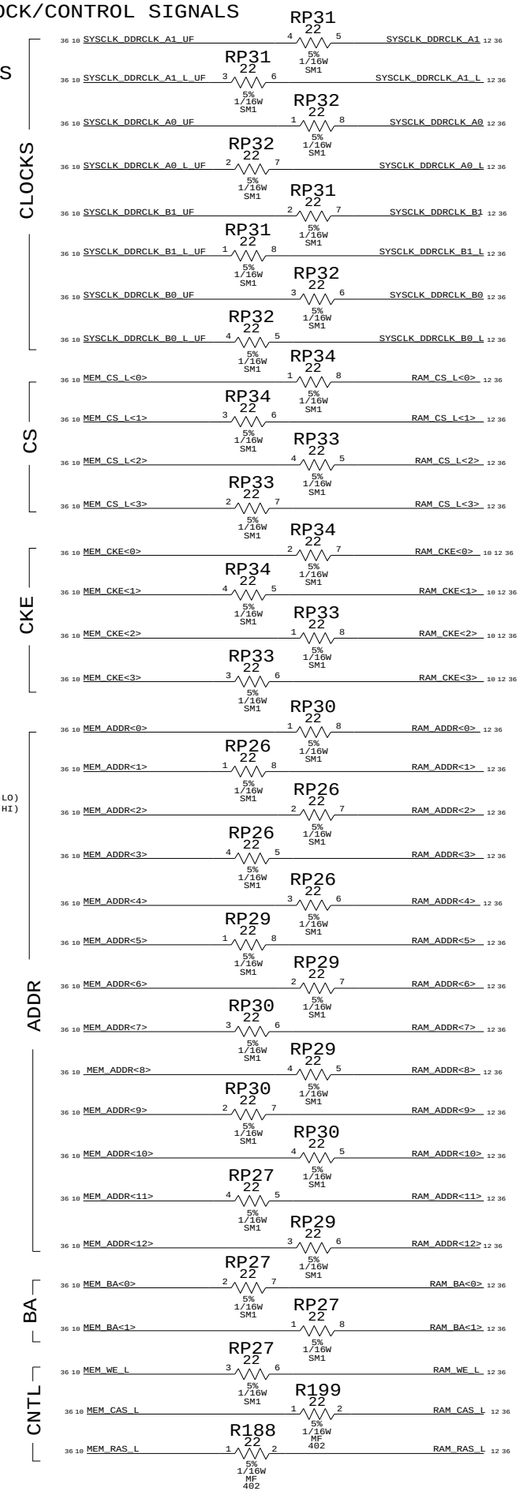
SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

PINS ARE SWAPABLE FOR RPAKS

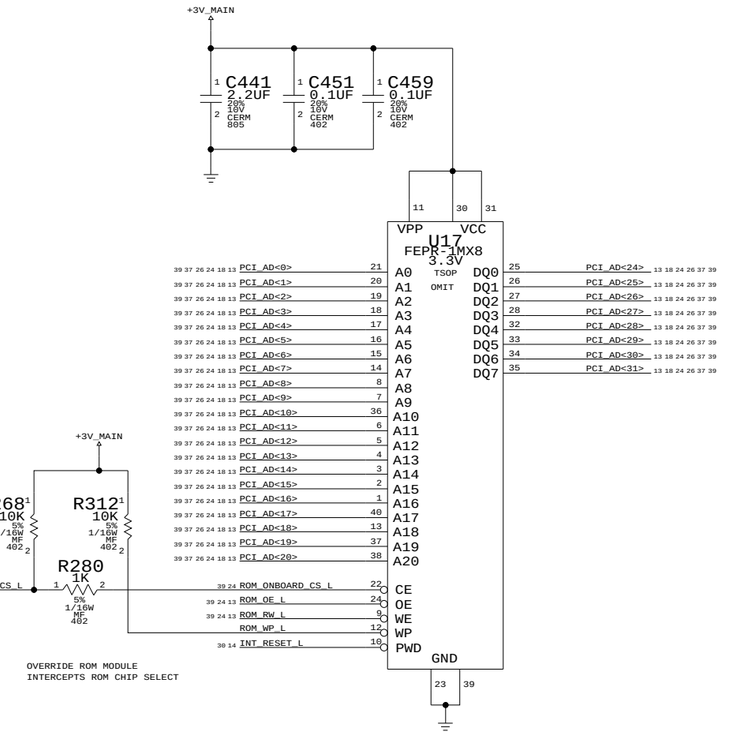


MEM_VREF





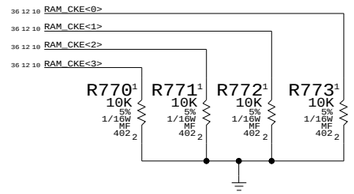
1MB BOOT ROM



OVERRIDE ROM MODULE
INTERCEPTS ROM CHIP SELECT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1241	1	BOOTROM,P84	U17	CRITICAL	?

PULL-DOWN RESISTORS TO ENSURE
CKE STAYS LOW AFTER INTREPID
2.5V I/O SHUTS OFF



INT - DDR/BOOTROM

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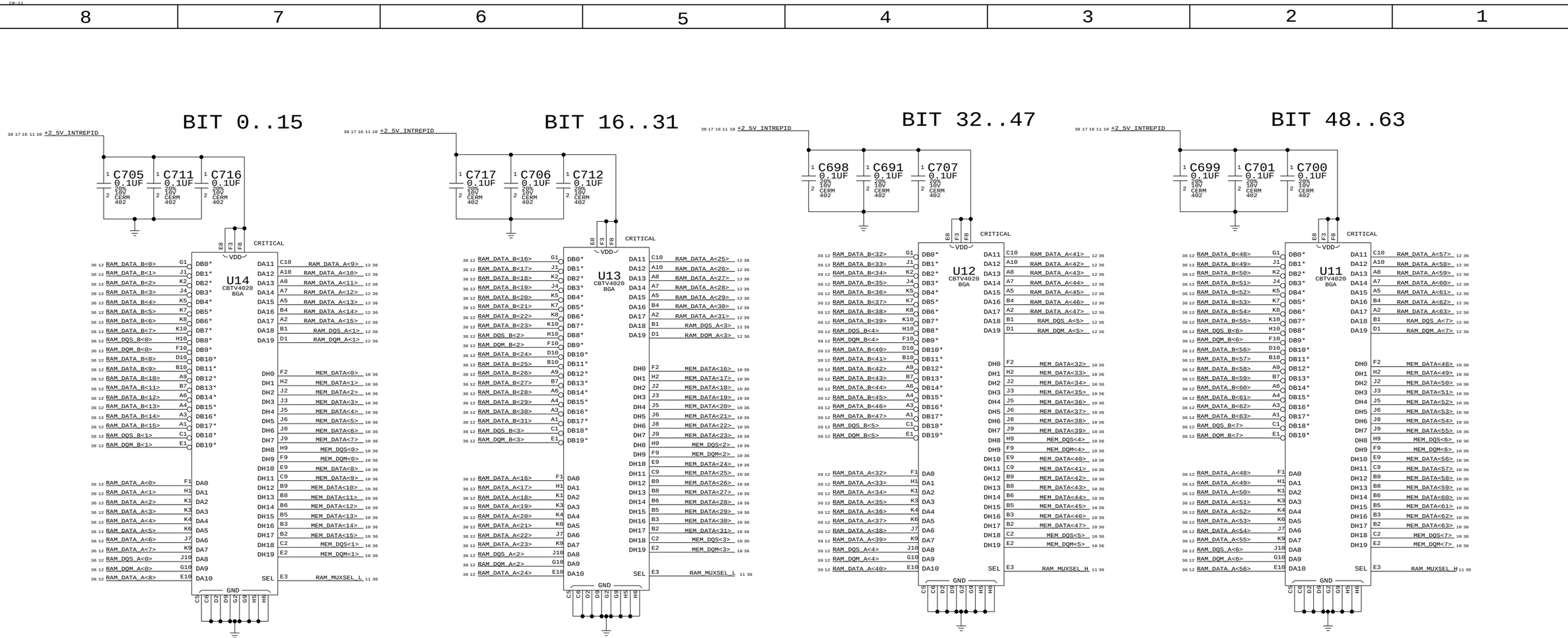
SCALE: NONE

SHT 10 OF 44



16BIT 2:1 DDR MUXES

APPLE COMPUTER INC.

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SCALE: NONE

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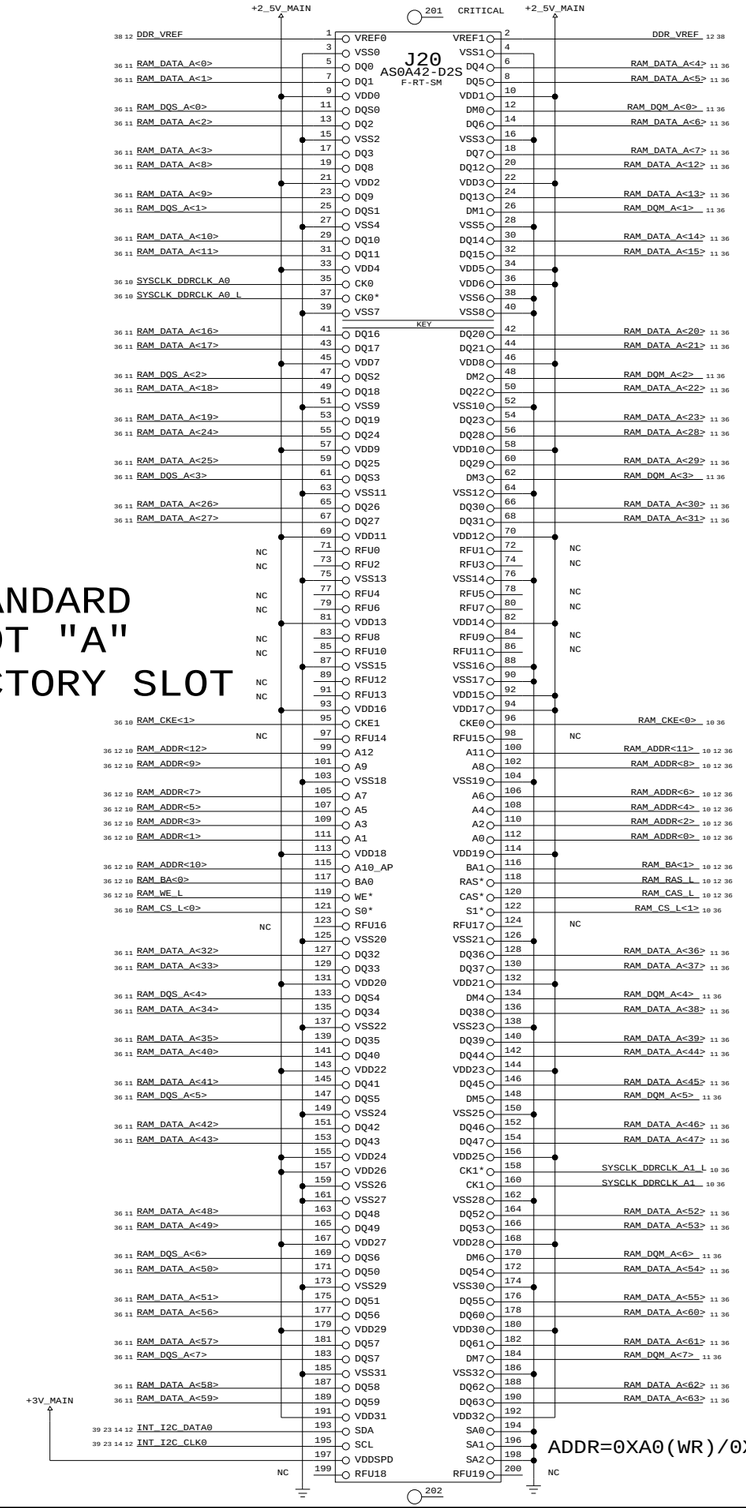
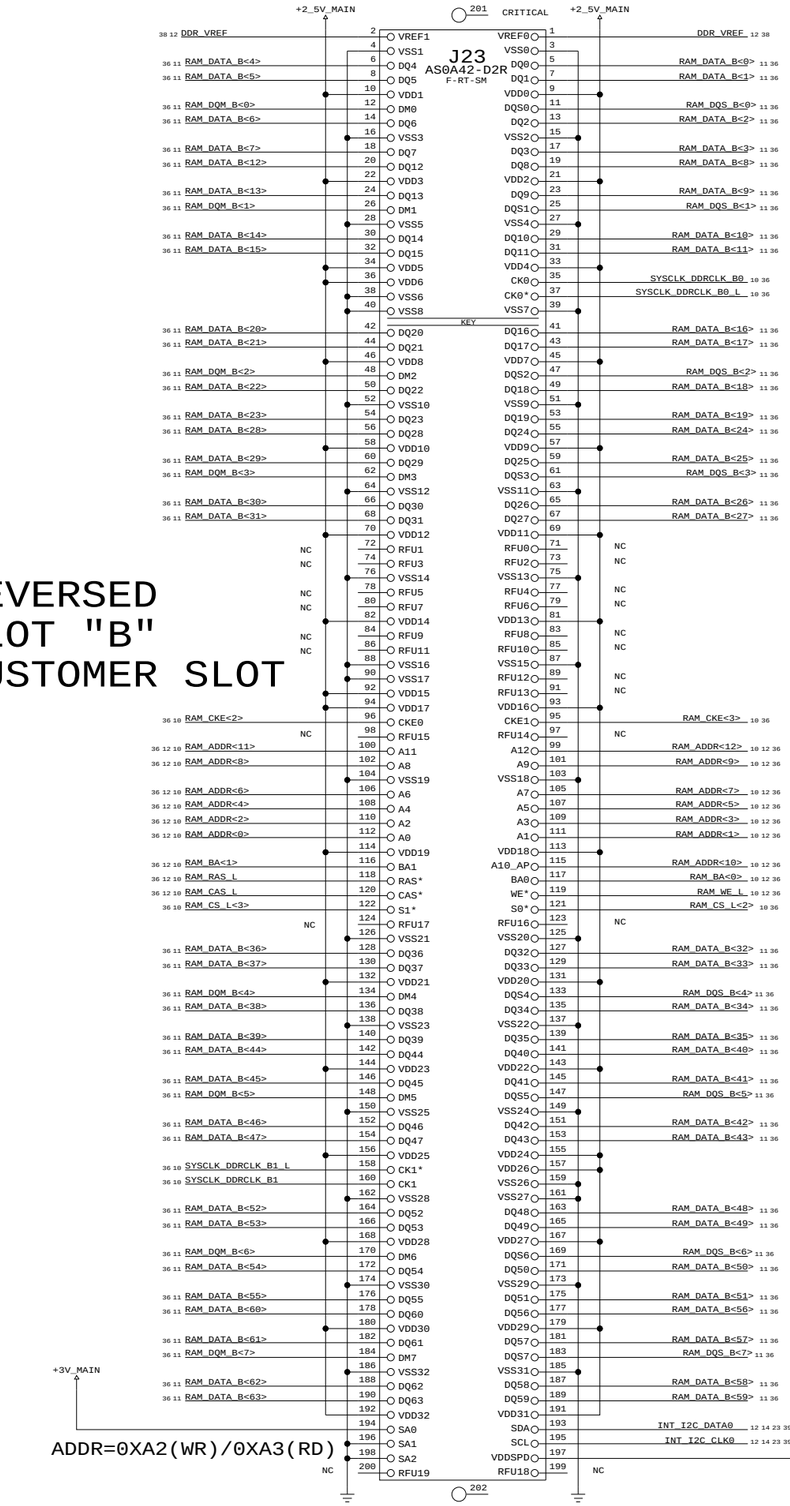
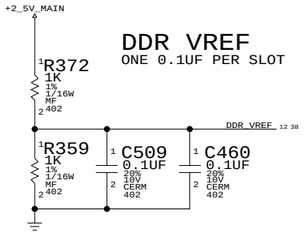
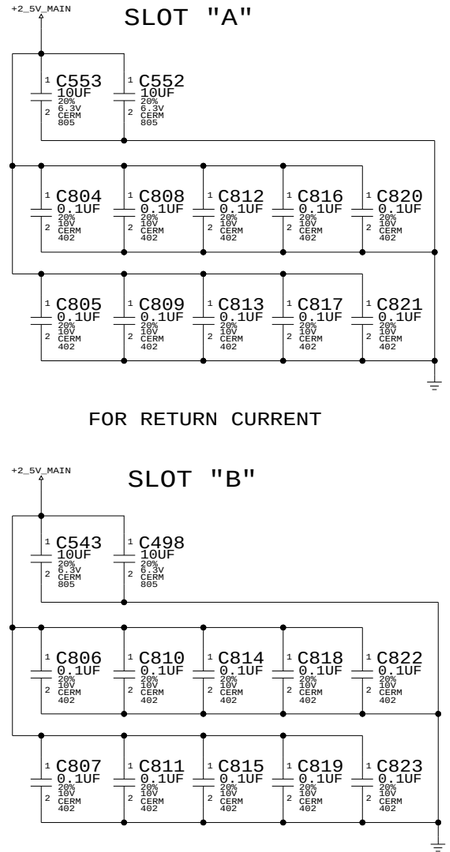


STANDARD
SLOT "A"
FACTORY SLOT



REVERSED
SLOT "B"
CUSTOMER SLOT





DDR SODIMM CONNS

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SCALE: NONE

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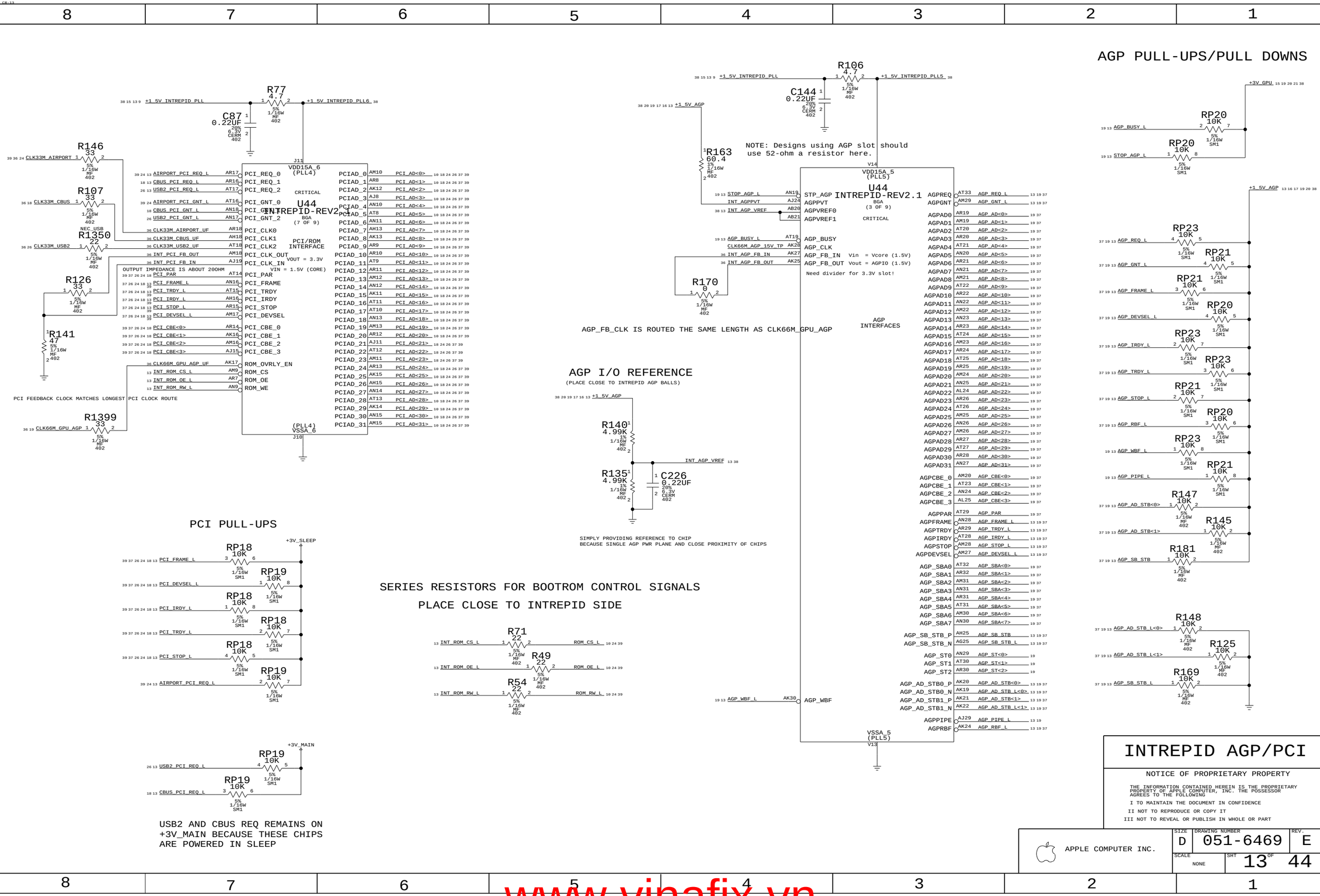

INTREPID AGP/PCI

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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SCALE: NONE

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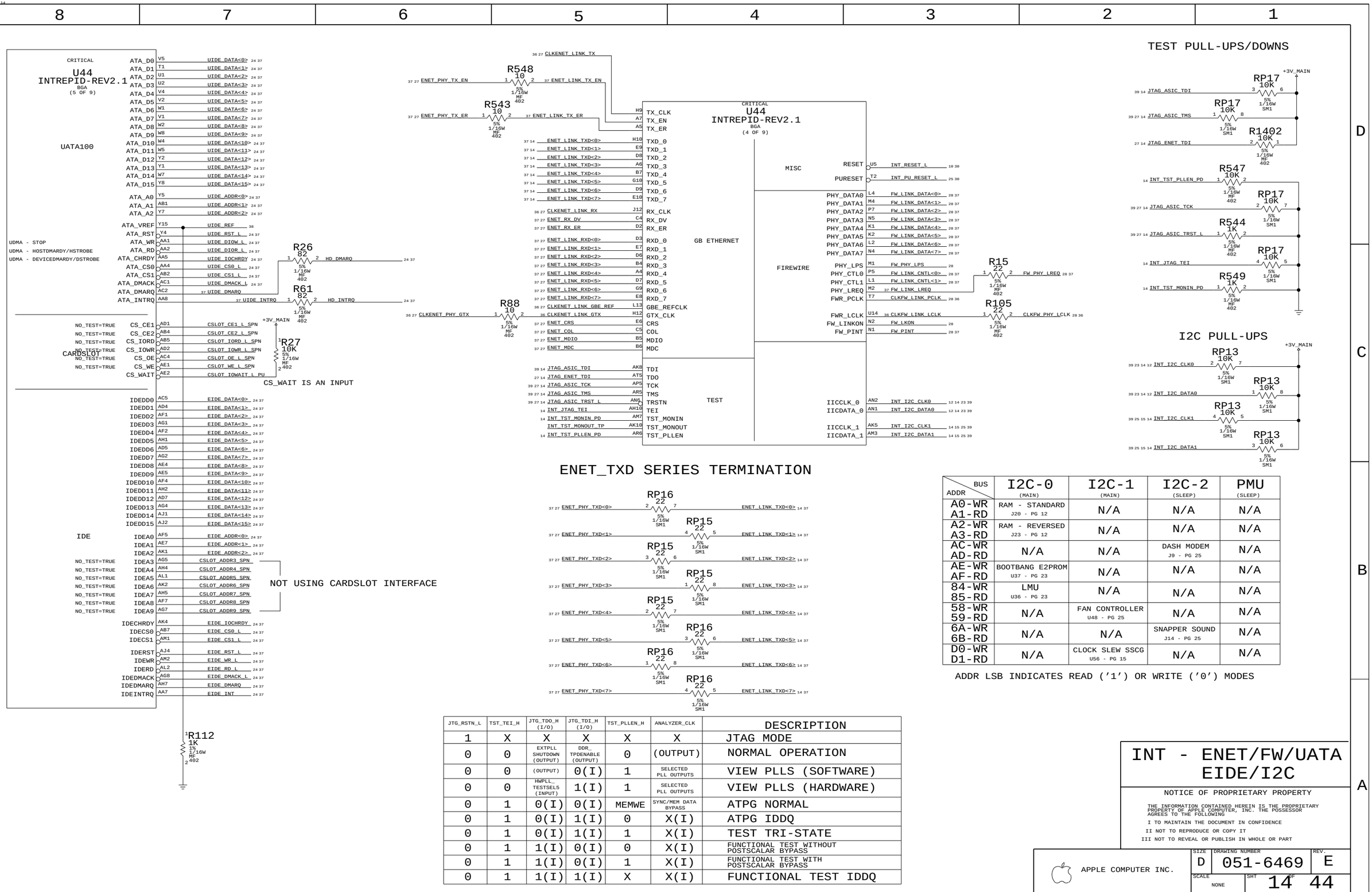

ADDR \ BUS	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
A0-WR A1-RD	RAM - STANDARD J20 - PG 12	N/A	N/A	N/A
A2-WR A3-RD	RAM - REVERSED J23 - PG 12	N/A	N/A	N/A
AC-WR AD-RD	N/A	N/A	DASH MODEM J9 - PG 25	N/A
AE-WR AF-RD	BOOTBANG E2PROM U37 - PG 23	N/A	N/A	N/A
84-WR 85-RD	LMU U36 - PG 23	N/A	N/A	N/A
58-WR 59-RD	N/A	FAN CONTROLLER U48 - PG 25	N/A	N/A
6A-WR 6B-RD	N/A	N/A	SNAPPER SOUND J14 - PG 25	N/A
D0-WR D1-RD	N/A	CLOCK SLEW SSCG U56 - PG 15	N/A	N/A

ADDR LSB INDICATES READ ('1') OR WRITE ('0') MODES

JTG_RSTN_L	TST_TEI_H	JTG_TDO_H (I/O)	JTG_TDI_H (I/O)	TST_PLLEN_H	ANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	EXTPLL SHUTDOWN (OUTPUT)	DDR_ TPDENABLE (OUTPUT)	0	(OUTPUT)	NORMAL OPERATION
0	0	(OUTPUT)	0(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	HWPLL_ TESTSEL5 (INPUT)	1(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0(I)	0(I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0(I)	1(I)	0	X(I)	ATPG IDDQ
0	1	0(I)	1(I)	1	X(I)	TEST TRI-STATE
0	1	1(I)	0(I)	0	X(I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1(I)	0(I)	1	X(I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1(I)	1(I)	X	X(I)	FUNCTIONAL TEST IDDQ

INT - ENET/FW/UATA EIDE/I2C

APPLE COMPUTER INC.

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SCALE	SHT	OF
NONE	14	44

USB PORT ASSIGNMENTS

PORT A - RIGHT USB 1

PORT B - UNUSED

PORT C - LEFT USB

PORT D - UNUSED

PORT E - BLUETOOTH

PORT F - MODEM

USB POWER FAULT SIGNALS

FOR D3COLD SUPPORT

CRYSTAL LOAD CAPACITANCE IS 16PF

PLACE R68 CLOSE TO INTREPID SIDE
OTHERWISE A LOT OF OVERSHOOT/UNDERSHOOT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES,METAL FILM,10 K OHM,5,1/16W,0402,SM	R68	NO_SSCG

HWPLL_TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

INT - USB/GPIOS/I2S

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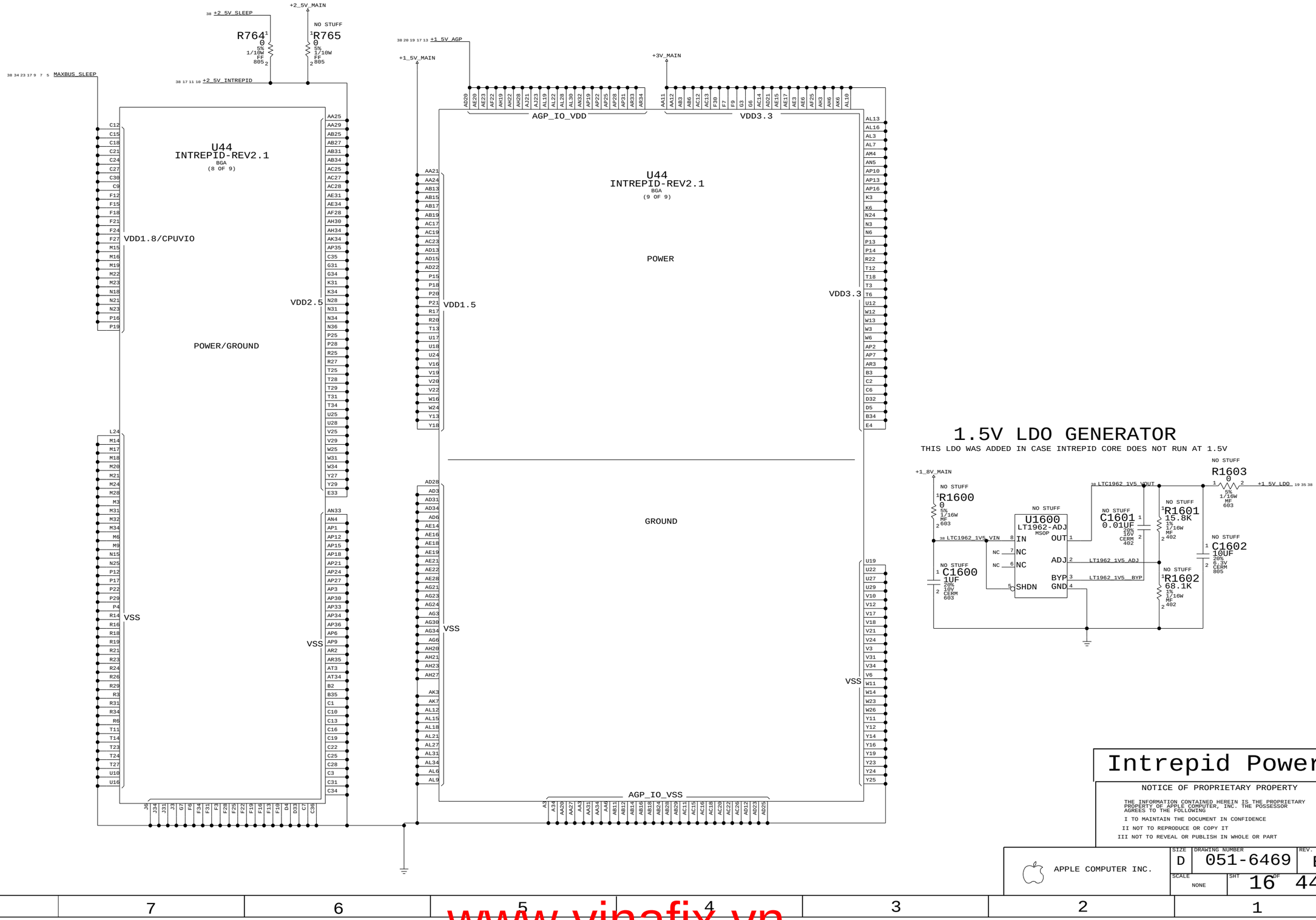

1.5V LDO GENERATOR

THIS LDO WAS ADDED IN CASE INTREPID CORE DOES NOT RUN AT 1.5V

Intrepid Power

APPLE COMPUTER INC.

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CR-17

INTREPID MAXBUS DECOUPLING

24 Balls
4 X 10UF (0805)
32 X 0.22UF (0402)

23 16 9 7 5 38 34 MAXBUS_SLEEP

C11 10uF 20% 6.3V CERM 805 · C326 10uF 20% 6.3V CERM 805 · C215 10uF 20% 6.3V CERM 805 · C181 10uF 20% 6.3V CERM 805

C218 C219 C328 C298 C160 C269 C299 C96 C267 C142 — 0.22uF 20% 6.3V CERM 402

C158 C183 C240 C216 C217 C97 C113 C220 C241 C300 — 0.22uF 20% 6.3V CERM 402

C157 C155 C159 C205 C156 C184 C114 C268 C115 C327 — 0.22uF 20% 6.3V CERM 402

C182 C186 — 0.22uF 20% 6.3V CERM 402

INTREPID AGP I/O DECOUPLING

21 Balls
4 X 10UF (0805)
24 X 0.22UF (0402)

38 20 19 16 13 +1_5V_AGP

C336 10uF 20% 6.3V CERM 805 · C210 10uF 20% 6.3V CERM 805 · C262 10uF 20% 6.3V CERM 805 · C374 10uF 20% 6.3V CERM 805

C334 C279 C249 C194 C333 C248 C229 C280 C357 C193 — 0.22uF 20% 6.3V CERM 402

C207 C209 C246 C358 C335 C208 C311 C373 C310 C309 — 0.22uF 20% 6.3V CERM 402

C230 C247 C228 — 0.22uF 20% 6.3V CERM 402

INTREPID DDR DECOUPLING

44 Balls
4 X 10UF (0805)
51 X 0.22UF (0402)

38 16 11 10 +2_5V_INTREPID

C403 10uF 20% 6.3V CERM 805 · C397 10uF 20% 6.3V CERM 805 · C398 10uF 20% 6.3V CERM 805 · C402 10uF 20% 6.3V CERM 805

C389 C371 C293 C303 C272 C370 C350 C306 C345 C346 — 0.22uF 20% 6.3V CERM 402

C347 C274 C277 C385 C273 C330 C308 C372 C365 C356 — 0.22uF 20% 6.3V CERM 402

C307 C304 C381 C392 C321 C349 C364 C276 C388 C387 — 0.22uF 20% 6.3V CERM 402

C386 C382 C366 C270 C367 C383 C332 C369 C292 C380 — 0.22uF 20% 6.3V CERM 402

C323 C271 C384 C379 C348 C320 C368 C275 C305 C322 — 0.22uF 20% 6.3V CERM 402

C302 — 0.22uF 20% 6.3V CERM 402

INTREPID CORE DECOUPLING

30 Balls
4 X 10UF (0805)
29 X 0.22UF (0402)

+1_5V_MAIN

C124 10uF 20% 6.3V CERM 805 · C103 10uF 20% 6.3V CERM 805 · C154 10uF 20% 6.3V CERM 805 · C301 10uF 20% 6.3V CERM 805

C136 C222 C243 C221 C206 C165 C131 C192 C259 C245 — 0.22uF 20% 6.3V CERM 402

C223 C189 C162 C163 C161 C143 C145 C146 C261 C260 — 0.22uF 20% 6.3V CERM 402

C133 C225 C188 C244 C164 C190 C175 C185 C191 — 0.22uF 20% 6.3V CERM 402

INTREPID 3.3V DECOUPLING

57 Balls
4 X 10UF (0805)
72 X 0.22UF (0402)

+3V_MAIN

C148 10uF 20% 6.3V CERM 805 · C377 10uF 20% 6.3V CERM 805 · C12 10uF 20% 6.3V CERM 805 · C10 10uF 20% 6.3V CERM 805

C355 C329 C56 C46 C23 C169 C38 C132 C119 C117 — 0.22uF 20% 6.3V CERM 402

C40 C168 C47 C42 C242 C63 C55 C177 C60 C21 — 0.22uF 20% 6.3V CERM 402

C17 C106 C58 C39 C121 C49 C79 C258 C35 C33 — 0.22uF 20% 6.3V CERM 402

C41 C26 C116 C135 C130 C37 C134 C98 C57 C53 — 0.22uF 20% 6.3V CERM 402

C78 C118 C54 C62 C147 C122 C100 C107 C59 C34 — 0.22uF 20% 6.3V CERM 402

C278 C227 C187 C61 C25 C22 C64 C48 C36 C27 — 0.22uF 20% 6.3V CERM 402

C167 C19 C52 C43 C18 C101 C378 C120 C123 C102 — 0.22uF 20% 6.3V CERM 402

Intrepid Decoupling

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PCI1510 PULL-UPS

+3V_MAIN

R670 10K 5% 1/16W MF 402 — CBUS_PCI_PERR_L 18
R669 10K 5% 1/16W MF 402 — CBUS_PCI_SERR_L 18
R662 10K 5% 1/16W MF 402 — CBUS_SUSPEND_PU 18

+3V_MAIN

C579 10UF 20% 6.3V CERM 805
C761 0.22UF 20% 6.3V CERM 402
C764 0.22UF 20% 6.3V CERM 402
C755 0.22UF 20% 6.3V CERM 402
C762 0.22UF 20% 6.3V CERM 402
C763 0.22UF 20% 6.3V CERM 402
C756 0.22UF 20% 6.3V CERM 402

R676 10K 5% 1/16W MF 402

+2_5V_MAIN

C754 0.22UF 20% 6.3V CERM 402

A7 C13 D5 E1 M1 N7 N11 — VCC

39 30 26 24 21 19 18 MAIN_RESET_L

THIS PROPERLY SHUTS DOWN
CARDBUS POWER FOR PSUEDO-D3COLD

R774 47 5% 1/16W MF 402

+3V_MAIN
+5V_MAIN

NO STUFF
R299 10K 5% 1/16W MF 402

U20
TPS2211 SSOI

NC	9		
V_12	5	AVPP	10
V_5_1	6		
V_5_2	3	AVCC0	11
V_3_1	4	AVCC1	12
V_3_2		AVCC2	13
VCCD0	1		
VCCD1	2		
VPPD0	15		
VPPD1	14		
SHTDWN	16		
GND	7	OC	8 NC

+VPP_CBUS_SW 18 38
38 18 +VCC_CBUS_SW

MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES
TO MINIMIZE INDUCTANCE!

C739 0.1UF 20% 16V CERM 402
C448 0.1UF 20% 16V CERM 402

0.1UF ARE USED TO INCREASE ESD DISCHARGES OF UP TO 10KV

TPS2211_SHDN_L_PU

CRITICAL
U26
PCI1510GGU
BGA

CLAMP FOR PC-CARD
CLAMP FOR PCI

NC	H10	CLK_48_RSVD/NC	
PCI1510_VR_EN_L	D4	VR_EN*	
	L8	VR_PORT	
	B11	VCCCB	
	L3	VCCP	
	N13	VCCD0*	CBUS_VCCD0_L
	L12	VCCD1*	CBUS_VCCD1_L
	K9	VPPD0	CBUS_VPPD0
	M11	VPPD1	CBUS_VPPD1
39 37 26 24 13 10 PCI_AD<0>	N8	AD0	
39 37 26 24 13 10 PCI_AD<1>	M7	AD1	
39 37 26 24 13 10 PCI_AD<2>	L7	AD2	
39 37 26 24 13 10 PCI_AD<3>	N6	AD3	
39 37 26 24 13 10 PCI_AD<4>	K4	AD4	
39 37 26 24 13 10 PCI_AD<5>	M6	AD5	
39 37 26 24 13 10 PCI_AD<6>	L6	AD6	
39 37 26 24 13 10 PCI_AD<7>	N5	AD7	
39 37 26 24 13 10 PCI_AD<8>	N4	AD8	
39 37 26 24 13 10 PCI_AD<9>	M2	AD9	
39 37 26 24 13 10 PCI_AD<10>	M5	AD10	
39 37 26 24 13 10 PCI_AD<11>	L4	AD11	
39 37 26 24 13 10 PCI_AD<12>	N3	AD12	
39 37 26 24 13 10 PCI_AD<13>	K5	AD13	
39 37 26 24 13 10 PCI_AD<14>	L5	AD14	
39 37 26 24 13 10 PCI_AD<15>	M4	AD15	
39 37 26 24 13 10 PCI_AD<16>	J4	AD16	
39 37 26 24 13 10 PCI_AD<17>	H1	AD17	
39 37 26 24 13 10 PCI_AD<18>	H3	AD18	
PCI_AD<19>	H2	AD19	
39 37 26 24 13 10 PCI_AD<20>	G2	AD20	
39 37 26 24 13 10 PCI_AD<21>	G4	AD21	
39 37 26 24 13 10 PCI_AD<22>	F1	AD22	
39 37 26 24 13 10 PCI_AD<23>	C3	AD23	
39 37 26 24 13 10 PCI_AD<24>	F3	AD24	
39 37 26 24 13 10 PCI_AD<25>	E2	AD25	
39 37 26 24 13 10 PCI_AD<26>	F4	AD26	
39 37 26 24 13 10 PCI_AD<27>	B1	AD27	
39 37 26 24 13 10 PCI_AD<28>	D2	AD28	
39 37 26 24 13 10 PCI_AD<29>	E4	AD29	
39 37 26 24 13 10 PCI_AD<30>	D3	AD30	
39 37 26 24 13 10 PCI_AD<31>	E3	AD31	
39 37 26 24 13 PCI_CBE<0>	K6	C/BE0*	
39 37 26 24 13 PCI_CBE<1>	M3	C/BE1*	
39 37 26 24 13 PCI_CBE<2>	J2	C/BE2*	
39 37 26 24 13 PCI_CBE<3>	A1	C/BE3*	
39 37 26 24 13 PCI_PAR	N1	PAR	
39 37 26 24 13 PCI_IRDY_L	K1	IRDY	
18 CBUS_PCI_SERR_L	L2	SERR	
CBUS_PCI_IDSEL	F2	IDSEL	
18 CBUS_PCI_PERR_L	K3	PERR	
39 37 26 24 13 PCI_FRAME_L	J1	FRAME	
39 37 26 24 13 PCI_STOP_L	L1	STOP	
39 37 26 24 13 PCI_TRDY_L	J3	TRDY	
39 37 26 24 13 PCI_DEVSEL_L	K2	DEVSEL	
CBUS_PCI_RESET_L	G3	PRST	
13 CBUS_PCI_REQ_L	C2	REQ	
13 CBUS_PCI_GNT_L	C1	GNT	
36 13 CLK33M_CBUS	G1	PCLK	
NC	M9	SPKROUT	
NC	M8	RI_OUT/PME	
18 CBUS_SUSPEND_PU	N10	SUSPEND	
15 CBUS_INT_L	K7	MFUNC0	
18 CBUS_MFUNC1_PD	N9	MFUNC1	
18 CBUS_MFUNC2_PD	L9	MFUNC2	
18 CBUS_MFUNC3_PD	K10	MFUNC3	
18 CBUS_MFUNC4_PD	M10	MFUNC4	
18 CBUS_MFUNC5_PD	N12	MFUNC5	
18 CBUS_MFUNC6_PD	L10	MFUNC6	
	L11	GRST	
	L13	CD1*/CCD1*	CBUS_DET_1_L 18 39
	B5	CD2*/CCD2*	CBUS_DET_2_L 18 39
	F12	IORD*/CAD13	CBUS_IORD_L 18
	C11	IOWR*/CAD15	CBUS_IOWR_L 18
	G10	OE*/CAD11	CBUS_OE_L 18
	H13	CE1*/CC/BE0*	CBUS_CE1_L 18
	B2	VS1*/CVS1	CBUS_VS1 18
	A9	VS2*/CVS2	CBUS_VS2 18
	D13	WE*/CGNT*	CBUS_WE_L 18
	A6	RDY/IREQ*/CINT*	CBUS_READY 18
	D8	RESET/CRST*	CBUS_RESET_L 18
	A8	REG*/CC/BE3*	CBUS_REG_L 18
	C6	BVD1/CSTSCHG/STSCHG*/RI*	CBUS_BVD1_L 18
	D6	BVD2/SPKR*/CAUDIO	CBUS_BVD2_L 18
INTEGRATED PULL-UP	A5	WP/IOIS16*/CCLKRUN*	CBUS_WP_L 18
	G13	CE2/CAD10*	CBUS_CE2_L 18
	B8	INPACK/CREQ*	CBUS_INPACK_L 18
	B6	WAIT/CSERR*	CBUS_WAIT_L 18
	C7	A0/CAD26	CBUS_ADDR<0> 18
	D7	A1/CAD25	CBUS_ADDR<1> 18
	B7	A2/CAD24	CBUS_ADDR<2> 18
	D10	A3/CAD23	CBUS_ADDR<3> 18
	B12	A4/CAD22	CBUS_ADDR<4> 18
	C8	A5/CAD21	CBUS_ADDR<5> 18
	C9	A6/CAD20	CBUS_ADDR<6> 18
	A12	A7/CAD18	CBUS_ADDR<7> 18
	E11	A8/CC/BE1*	CBUS_ADDR<8> 18
	F11	A9/CAD14	CBUS_ADDR<9> 18
	G11	A10/CAD9	CBUS_ADDR<10> 18
	G12	A11/CAD12	CBUS_ADDR<11> 18
	D9	A12/CC/BE2*	CBUS_ADDR<12> 18
	E12	A13/CPAR	CBUS_ADDR<13> 18
	D12	A14/CPERR*	CBUS_ADDR<14> 18
	C10	A15/CIRDY*	CBUS_ADDR<15> 18
	B13	A16/CCLK	CBUS_ADDR_16_UF
	F10	A17/CAD16	CBUS_ADDR<17> 18
	E13	A18/RSVD	CBUS_ADDR<18> 18
	A13	A19/CBLOCK*	CBUS_ADDR<19> 18
	E10	A20/CSTOP*	CBUS_ADDR<20> 18
	D11	A21/CDEVSEL*	CBUS_ADDR<21> 18
	C12	A22/CTRDY*	CBUS_ADDR<22> 18
	A10	A23/CFRAME*	CBUS_ADDR<23> 18
	B10	A24/CAD17	CBUS_ADDR<24> 18
	B9	A25/CAD19	CBUS_ADDR<25> 18
	A4	D0/CAD27	CBUS_DATA<0> 18
	C4	D1/CAD29	CBUS_DATA<1> 18
	A3	D2/RSVD	CBUS_DATA<2> 18
	K11	D3/CAD0	CBUS_DATA<3> 18
	K12	D4/CAD1	CBUS_DATA<4> 18
	J13	D5/CAD3	CBUS_DATA<5> 18
	J10	D6/CAD5	CBUS_DATA<6> 18
	H12	D7/CAD7	CBUS_DATA<7> 18
	C5	D8/CAD28	CBUS_DATA<8> 18
	B4	D9/CAD30	CBUS_DATA<9> 18
	B3	D10/CAD31	CBUS_DATA<10> 18
	M12	D11/CAD2	CBUS_DATA<11> 18
	J11	D12/CAD4	CBUS_DATA<12> 18
	K13	D13/CAD6	CBUS_DATA<13> 18
	J12	D14/RSVD	CBUS_DATA<14> 18
	H11	D15/CAD8	CBUS_DATA<15> 18

R684 22 5% 1/16W MF 402

R661 47 5% 1/16W MF 402 — CBUS_ADDR<16> 18

NO STUFF
R675 47 5% 1/16W MF 402 — IO_RESET_L 30 27 26 23 19

R763 47 5% 1/16W MF 402 — MAIN_RESET_L 39 30 26 24 21 19 18

RP38 10K 5% 1/32W 25V SM

5	6	CBUS_MFUNC1_PD 18
10	4	CBUS_MFUNC2_PD 18
	7	CBUS_MFUNC3_PD 18
	3	CBUS_MFUNC4_PD 18
	9	CBUS_MFUNC5_PD 18
	8	CBUS_MFUNC6_PD 18
	2	
	1	

GND
A2 A11 D1 F13 H4 K8 M13 N2

TI REFERENCE SCHEMATIC DID NOT HAVE BULK ON +VCC_CBUS_SW

C748 2.2UF 20% 10V CERM 805
C742 2.2UF 20% 10V CERM 805

PC CARD/CARDBUS CONNECTOR

CRITICAL
J10
QT500806-L111
M-ST-SM

39 18 CBUS_DET_1_L	4	3	CBUS_DATA<4> 18
18 CBUS_DATA<11>	6	5	CBUS_DATA<5> 18
18 CBUS_DATA<12>	8	7	CBUS_DATA<6> 18
18 CBUS_DATA<13>	10	9	
	12	11	CBUS_DATA<7> 18
18 CBUS_DATA<14>	14	13	CBUS_CE1_L 18
18 CBUS_DATA<15>	16	15	CBUS_ADDR<10> 18
18 CBUS_CE2_L	18	17	CBUS_OE_L 18
18 CBUS_VS1	20	19	
	22	21	CBUS_ADDR<11> 18
18 CBUS_IORD_L	24	23	CBUS_ADDR<9> 18
18 CBUS_IOWR_L	26	25	CBUS_ADDR<8> 18
18 CBUS_ADDR<17>	28	27	CBUS_ADDR<13> 18
18 CBUS_ADDR<18>	30	29	
	32	31	CBUS_ADDR<14> 18
18 CBUS_ADDR<19>	34	33	CBUS_WE_L 18
18 CBUS_ADDR<20>	36	35	CBUS_READY 18
18 CBUS_ADDR<21>	38	37	+VCC_CBUS_SW 18 38
38 18 +VCC_CBUS_SW	40	39	
	42	41	+VPP_CBUS_SW 18 38
38 18 +VPP_CBUS_SW	44	43	CBUS_ADDR<16> 18
18 CBUS_ADDR<22>	46	45	CBUS_ADDR<15> 18
18 CBUS_ADDR<23>	48	47	CBUS_ADDR<12> 18
18 CBUS_ADDR<24>	50	49	
	52	51	CBUS_ADDR<7> 18
18 CBUS_ADDR<25>	54	53	CBUS_ADDR<6> 18
18 CBUS_VS2	56	55	CBUS_ADDR<5> 18
18 CBUS_RESET_L	58	57	CBUS_ADDR<4> 18
18 CBUS_WAIT_L	60	59	
	62	61	CBUS_ADDR<3> 18
18 CBUS_INPACK_L	64	63	CBUS_ADDR<2> 18
18 CBUS_REG_L	66	65	CBUS_ADDR<1> 18
18 CBUS_BVD2_L	68	67	CBUS_ADDR<0> 18
18 CBUS_BVD1_L	70	69	
	72	71	CBUS_DATA<0> 18
18 CBUS_DATA<8>	74	73	CBUS_DATA<1> 18
18 CBUS_DATA<9>	76	75	CBUS_DATA<2> 18
18 CBUS_DATA<10>	78	77	CBUS_WP_L 18
39 18 CBUS_DET_2_L	80	79	

83 82

CARDBUS

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SIZE	DRAWING NUMBER	REV.
D	051-6469	E
SCALE: NONE	SHT 18 OF 44	

IMPORTANT NOTES ON MAP17

NEED TO RESET GRAPHIC CHIP DURING RESTARTS

MEMORY CORE - 2.5V

+2_5V_GPU_FB 19 38

C264 10UF 20% 6.3V CERM 805 · C289 0.1UF 20% 10V CERM 402 · C283 0.1UF 20% 10V CERM 402 · C288 0.1UF 20% 10V CERM 402 · C104 0.1UF 20% 10V CERM 402 · C93 0.1UF 20% 10V CERM 402 · C84 0.1UF 20% 10V CERM 402 · C251 0.1UF 20% 10V CERM 402 · C94 0.1UF 20% 10V CERM 402

AGP 4X I/O - 1.5V

38 20 19 17 16 13 +1_5V_AGP

BULK CAP ON INTREPID SIDE

C44 0.1UF 20% 10V CERM 402 · C92 0.1UF 20% 10V CERM 402 · C125 0.1UF 20% 10V CERM 402 · C150 0.1UF 20% 10V CERM 402

C65 0.01UF 20% 10V CERM 402 · C149 0.01UF 20% 10V CERM 402 · C196 0.01UF 20% 10V CERM 402 · C28 0.01UF 20% 10V CERM 402

MEMORY I/O - 2.5V

38 19 +2_5V_GPU_FB

C170 10UF 20% 6.3V CERM 805 · C80 0.1UF 20% 10V CERM 402 · C67 0.1UF 20% 10V CERM 402 · C81 0.1UF 20% 10V CERM 402

C317 0.1UF · C85 0.1UF · C72 0.1UF

C282 0.1UF · C318 0.1UF · C254 0.1UF · C313 0.1UF

C105 0.01UF · C314 0.01UF · C294 0.01UF · C66 0.01UF

U43 MAP31-64MB BGA (3 OF 5) OMIT

VDDFBC · VDDFBIO0 · VIPD

HARDWARE DEBUG PORT

K4 GPU_VIPD0_TP · J3 GPU_VIPD1_TP · H3 GPU_VIPD2_ROMTYPE<1> 21 · K5 GPU_VIPD3_PCI_DEVID<2> 21 · G2 GPU_VIPD4_PCI_DEVID<0> 21 · G1 GPU_VIPD5_PCI_DEVID<1> 21 · F1 GPU_VIPD6_CRYSTAL<1> 21 · G3 GPU_VIPD7_TP

VIPHAD0 C8 GPU_VIPHAD0_TP · VIPHAD1 C7 GPU_VIPHAD1_TP · VIPHCLK A5 GPU_VIPHCLK_TP · VIPHCTL B6 GPU_VIPHTCL_TP · VIPPCLK B7 VIPPCLK_PD

+2_5V_GPU_FB 19 38 · MAP31 R31 49.9 1% 1/16W MF 402

MEM_CAL_PD G30 · MEM_CAL_PU J30 · MEM_CAL_CLK K30

MAP31 R173 10K 5% 1/16W MF 402 · MAP31 R30 49.9 1% 1/16W MF 402 · MAP31 R29 49.9 1% 1/16W MF 402

FB SIGNALS USED FOR INTERNAL TESTING ONLY
CHANGE TO NC FOR NEXT SYMBOL UPDATE

NC A24 FBAA0_0 · NC B16 FBAA0_1

36 19 GPU_FBCLK0 C21 FBCLK0 · 36 19 GPU_FBCLK0_L C20 FBCLK0* · 36 19 GPU_FBCLK1 B4 FBCLK1 · 36 19 GPU_FBCLK1_L A4 FBCLK1* · GPU_FBACKE N28 FBACKE

FBACKE PULL-DOWN IS NEEDED
NC D28 FBD1 · NC D13 FBD33 · NC AA27 FBD8_0 · NC J28 FBD8_1 · 38 GPU_FB_VREF A18 FBVREF

THERE'S NO ON-CHIP VOLTAGE DIVIDER

NC C11 FBAWE* · GPU_ROMA14_TP J1 ROMA14 · GPU_ROMA15_TP F2 ROMA15 · GPU_ROMCS_TP AH2 ROMCS*

FBDQS0 F28 NC · FBDQS1 AA26 NC · FBDQS2 K28 NC · FBDQS3 E12 NC

R1900 10K 5% 1/16W MF 402 · R1901 10K 5% 1/16W MF 402 · R35 10K 5% 1/16W MF 402

AGP I/O REFERENCE

(PLACE CLOSE TO NV17M AGP BALLS)

38 20 19 17 16 13 +1_5V_AGP

R22 4.99K 1% 1/16W MF 402 · R28 4.99K 1% 1/16W MF 402 · C13 0.22UF 20% 6.3V CERM 402

GPU_AGP_VREF 19 38

USE SIMPLE REFERENCE TO CHIP
BECAUSE SINGLE AGP PWR PLANE AND CLOSE PROXIMITY OF CHIPS

U43 MAP31-64MB BGA (1 OF 5) OMIT

37 13 AGP_AD<0>	AD30	PCIAD0	VDDAGP0 AF30
37 13 AGP_AD<1>	AE30	PCIAD1	VDDAGP1 AG14
37 13 AGP_AD<2>	AD29	PCIAD2	VDDAGP2 AG17
37 13 AGP_AD<3>	AE29	PCIAD3	VDDAGP3 AG20
37 13 AGP_AD<4>	AD28	PCIAD4	VDDAGP4 AK14
37 13 AGP_AD<5>	AG30	PCIAD5	VDDAGP5 AK17
37 13 AGP_AD<6>	AF28	PCIAD6	VDDAGP6 AK20
37 13 AGP_AD<7>	AG29	PCIAD7	VDDAGP7 AK23
37 13 AGP_AD<8>	AH30	PCIAD8	VDDAGP8 AK26
37 13 AGP_AD<9>	AC28	PCIAD9	VDDAGP9 AK29
37 13 AGP_AD<10>	AH29	PCIAD10	
37 13 AGP_AD<11>	AE28	PCIAD11	
37 13 AGP_AD<12>	AJ30	PCIAD12	
37 13 AGP_AD<13>	AG28	PCIAD13	
37 13 AGP_AD<14>	AK30	PCIAD14	
37 13 AGP_AD<15>	AG27	PCIAD15	
37 13 AGP_AD<16>	AH23	PCIAD16	
37 13 AGP_AD<17>	AJ24	PCIAD17	
37 13 AGP_AD<18>	AH22	PCIAD18	
37 13 AGP_AD<19>	AK24	PCIAD19	
37 13 AGP_AD<20>	AH21	PCIAD20	
37 13 AGP_AD<21>	AJ22	PCIAD21	
37 13 AGP_AD<22>	AH20	PCIAD22	
37 13 AGP_AD<23>	AK22	PCIAD23	
37 13 AGP_AD<24>	AG21	PCIAD24	
37 13 AGP_AD<25>	AJ19	PCIAD25	
37 13 AGP_AD<26>	AG18	PCIAD26	
37 13 AGP_AD<27>	AK19	PCIAD27	
37 13 AGP_AD<28>	AG19	PCIAD28	
37 13 AGP_AD<29>	AJ18	PCIAD29	
37 13 AGP_AD<30>	AF19	PCIAD30	
37 13 AGP_AD<31>	AK18	PCIAD31	
37 13 AGP_CBE<0>	AH28	PCICBE0*	
37 13 AGP_CBE<1>	AJ27	PCICBE1*	
37 13 AGP_CBE<2>	AK25	PCICBE2*	
37 13 AGP_CBE<3>	AF21	PCICBE3*	
36 13 CLK66M_GPU_AGP	AJ12	PCICLK	
AGP_GPU_RESET_L	AH11	PCIRST*	
37 13 AGP_GNT_L	AG12	PCIGNT*	
37 13 AGP_REQ_L	AK12	PCIREQ*	
37 13 AGP_FRAME_L	AH24	PCIFRAME*	
37 13 AGP_IRDY_L	AJ25	PCIIRDY*	
37 13 AGP_TRDY_L	AH25	PCITRDY*	
37 13 AGP_DEVSEL_L	AK27	PCIDEVSEL*	
37 13 AGP_STOP_L	AH26	PCISTOP*	
37 13 AGP_PAR	AH27	PCIPAR	
15 AGP_NV_INT_L	AK11	PCIINTA*	
37 13 AGP_RBF_L	AJ13	AGPRBF*	
AGP_NV_WBF_L	AG15	AGPWBF*	
AGP_NV_PIPE_L	AF18	AGPPIPE*	
13 AGP_ST<0>	AF12	AGPST0	
13 AGP_ST<1>	AF13	AGPST1	
13 AGP_ST<2>	AG13	AGPST2	
37 13 AGP_AD_STB<1>	AK21	AGPADSTB1	
37 13 AGP_AD_STB_L<1>	AJ21	AGPADSTB1*	
37 13 AGP_AD_STB<0>	AK28	AGPADSTB0	
37 13 AGP_AD_STB_L<0>	AJ28	AGPADSTB0*	
13 AGP_BUSY_L	AF10	AGPBUSY*	
13 STOP_AGP_L	AG10	AGPSTOP*	
AGP_CAL_PD	AH15	AGP_CAL_PD	
AGP_CAL_PU	AH14	AGP_CAL_PU	
NC	AH19	AGP_DBI_LO	
NC	AK13	AGP_MB_DET*	
38 19 GPU_AGP_VREF	AC30	AGPVREF	
37 13 AGP_SBA<0>	AJ15	AGPSBA0	
37 13 AGP_SBA<1>	AF15	AGPSBA1	
37 13 AGP_SBA<2>	AK15	AGPSBA2	
37 13 AGP_SBA<3>	AG16	AGPSBA3	
37 13 AGP_SBA<4>	AK16	AGPSBA4	
37 13 AGP_SBA<5>	AF16	AGPSBA5	
37 13 AGP_SBA<6>	AJ16	AGPSBA6	
37 13 AGP_SBA<7>	AH18	AGPSBA7	
37 13 AGP_SB_STB	AH16	AGPSBSTB	
37 13 AGP_SB_STB_L	AH17	AGPSBSTB*	

NC: A1, A10, A11, A13, A14, A15, A16, A17, A2, A20, A21, A22, A23, A25, A26, A27, A28, A3, AA28, AA29, AA30, AA4, AA5, AB28, AB29, AB30, B1, B13, B15, B16, B18, B19, B21, B22, B24, B25, B27, B28, B3, C1, C10, C13, C14, C15, C16

D3COLD
R601 47 5% 1/16W MF 402 — 39 30 26 24 21 18 MAIN_RESET_L

D3HOT
R155 47 5% 1/16W MF 402 — 30 27 26 23 18 IO_RESET_L

MAIN_RESET_L IS TOGGLED FOR SLEEP
IO_RESET_L IS NOT TOGGLED FOR SLEEP

R115 0 5% 1/16W MF 402 — 13 AGP_WBF_L

R99 0 5% 1/16W MF 402 — 13 AGP_PIPE_L

38 20 19 17 16 13 +1_5V_AGP

MAP31 R128 49.9 1% 1/16W MF 402

MAP31 R136 49.9 1% 1/16W MF 402

FOR AGP 8X

FRAME BUFFER CLOCK TERMINATION

+2_5V_GPU_FB 19 38

NO STUFF R72 120 5% 1/16W MF 402 — GPU_FBCLK0 19 36

NO STUFF R82 100 5% 1/16W MF 402 — GPU_FBCLK0_L 19 36

NO STUFF R83 120 5% 1/16W MF 402

+2_5V_GPU_FB 19 38

NO STUFF R186 120 5% 1/16W MF 402 — GPU_FBCLK1 19 36

NO STUFF R185 100 5% 1/16W MF 402

NO STUFF R191 120 5% 1/16W MF 402 — GPU_FBCLK1_L 19 36

D3HOT VS. D3COLD POWER INTAKE

3V

+3V_MAIN · +3V_SLEEP

D3HOT R245 0 5% 1/10W FF 805 · D3COLD R244 0 5% 1/10W FF 805 — +3V_GPU 13 15 20 21 38

2.5V

+2_5V_MAIN · +2_5V_SLEEP

D3HOT R648 0 5% 1/10W FF 805 · D3COLD R647 0 5% 1/10W FF 805 — +2_5V_GPU_FB 19 38

1.5V

38 35 16 +1_5V_LDO

NO STUFF R1605 0 5% 1/16W MF 603 · +1_5V_MAIN D3HOT R635 0 5% 1/16W MF 603 · +1_5V_SLEEP D3COLD R634 0 5% 1/16W MF 603 — +1_5V_AGP 13 16 17 19 20 38

INTREPID AGP IS ALSO CONNECTED TO +1_5V_AGP

U43 MAP31-64MB BGA (4 OF 5) OMIT

GND · GND

MAP17 AGP/DDR RAM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6469	E

SCALE: NONE · SHT 19 OF 44

GPU VCORE SUPPLY

2.8V IFP PLL SUPPLY

TMDS TERMINATION

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN
CMF LINE SHOULD BE ROUTED AS 4MIL SURFACE
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS

I2C1 PULL-UP

MAP17 PWR/LVDS/TMDS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6469	E
SCALE: NONE	SHT 20 OF 44	

3.3V IO SUPPLY

MAP17 BOOT STRAPS

DVO VREF

PLACE CLOSE TO PIN

U43 MAP31-64MB

BGA
(2 OF 5)
OMIT

PLACE SERIES R CLOSE TO GPU

DVO<7..0> HARDWARE DEBUG PORT

DVOCLKOUT* NOT USED IN HIGH SWING

DVOCLKIN IS USED ONLY FOR EXTERNAL TV OUT SUPPORT

XTALSSIN: EXTERNAL SPREAD SPECTRUM CLOCK INPUT

XTALOUTBUFF GENERATED INTERNALLY

PTREEOUT

L4 / L5 / L53 400-OHM-EMI

PLL NOISE SHOULD BE LESS THAN 100MV PEAK-TO-PEAK

U55 SIL1162 TSSOP

NO STUFF

SILICON IMAGE 1162 TMDS

MAP TMDS

OKAY PER ICT

NO_TEST=TRUE

R166 / R156 VGA_VSYNC / VGA_HSYNC

R172 10M / R171 0 / Y2 SM-3

Y2 LOAD CAPACITANCE IS 18PF

C281 27.000M C351 CRITICAL 27PF

L19 FERR-EMI-100-OHM SM

SPREAD SPECTRUM SUPPORT

U46 CY25811 SOI

CRITICAL

R179 33 / R620 33

THERE'S 20K (10K/10K) RESISTOR DIVIDER ON CHIP - SO M IS TO FLOAT THE LINES
S0=1;S1=M => -1.5% DOWN-SPREAD

REPLACE WITH FERRITE IF NECESSARY

MSTRAPSEL WILL BE CONNECTED TO GND OR UNCONNECTED ON SUBSTRATE

ROM TYPE <1..0> = 00: ONLY (NVIDIA CONFIRMED OKAY)
BUS TYPE = 1: AGP
PCI_DEVID<3..0> = 1001: MAP17(464)
RAM CONFIG<3..0> = 1101: 4MX32, 1 DQS PER BYTE, LOW DRIVE STRENGTH
SUBVENDOR = 0: NO VIDEO BIOS ROM
PCI_AD = 1: NORMAL AGP PIN OUT
CRYSTAL = 2: 27MHZ AGP CRYSTAL

SHOULD BE 10MIL SPACING
CHANGED TO 8MIL BECAUSE OF PACKAGE PWR PINS

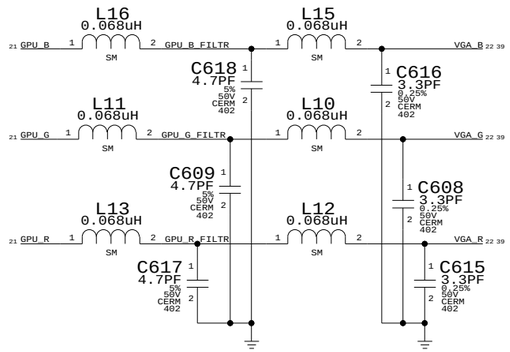
MAP17 ANALOG DAC/BOOT STRAPS

APPLE COMPUTER INC.

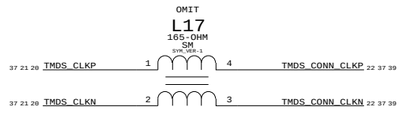
SIZE	DRAWING NUMBER	REV.
D	051-6469	E
SCALE: NONE	SHT 21 OF 44	

EXTERNAL VIDEO (DVI) INTERFACE

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

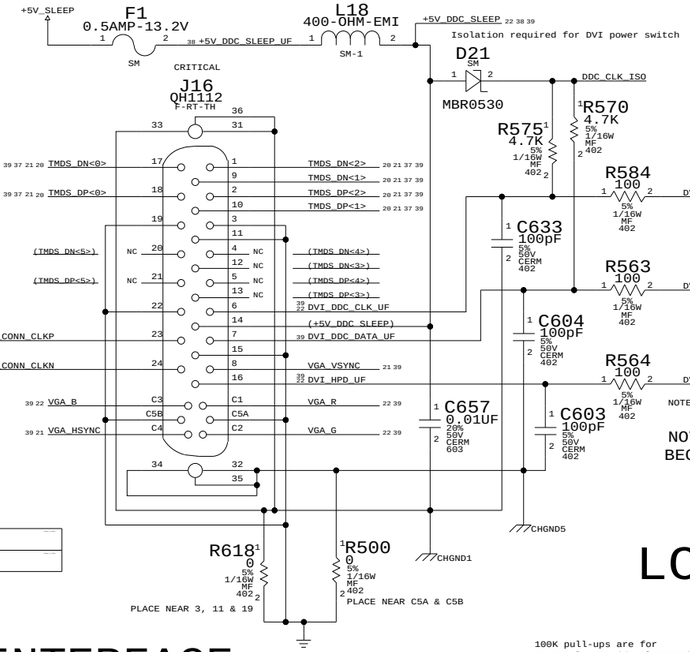


TMDS FILTERING
PLACE CLOSE TO CONNECTOR

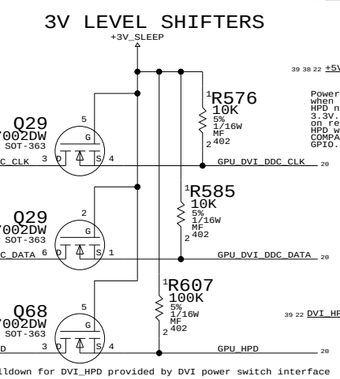


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S0147	1	CHOKE,COMM MODE 370OHM,2-LINE,SMD	L17	CRITICAL	

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)



3V LEVEL SHIFTERS

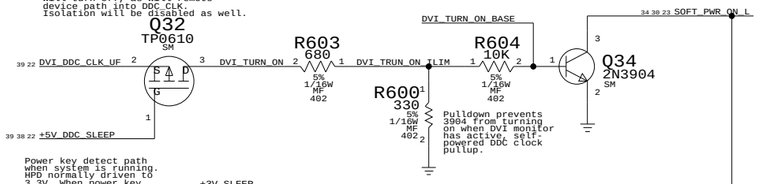


NOTE: Pulldown for DVI_HPD provided by DVI power switch interface

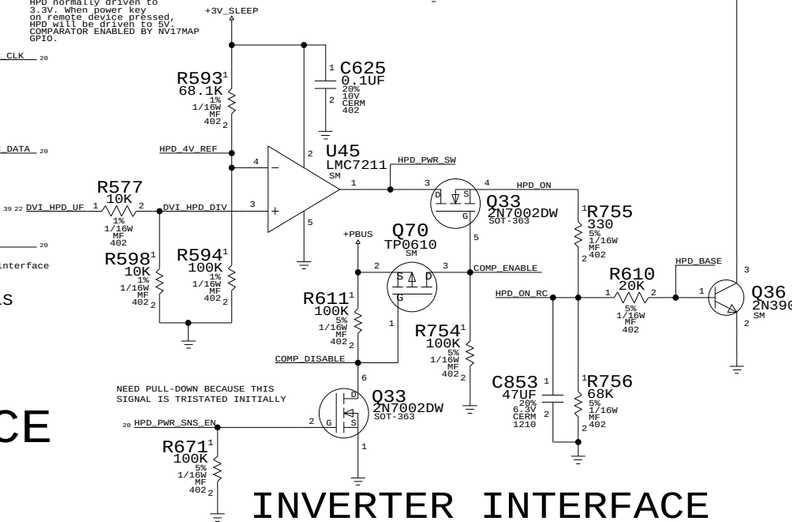
NOTE: DVI_HPD SHARES Q68 WITH ALS BECAUSE OF BOARD REAL ESTATE

DVI POWER SWITCH

Power key detect path when system is shutdown or asleep.. DDC_CLK is isolated from NV17M DURING SHUTDOWN. WHEN power key on remote device is pressed, 5V will be driven into DDC_CLK. Since host rails will be low, TP0610 will turn on, driving SOFT_PWR_ON_L low. As host rails rise, TP0610 will turn off, as will remote device path into DDC_CLK. Isolation will be disabled as well.



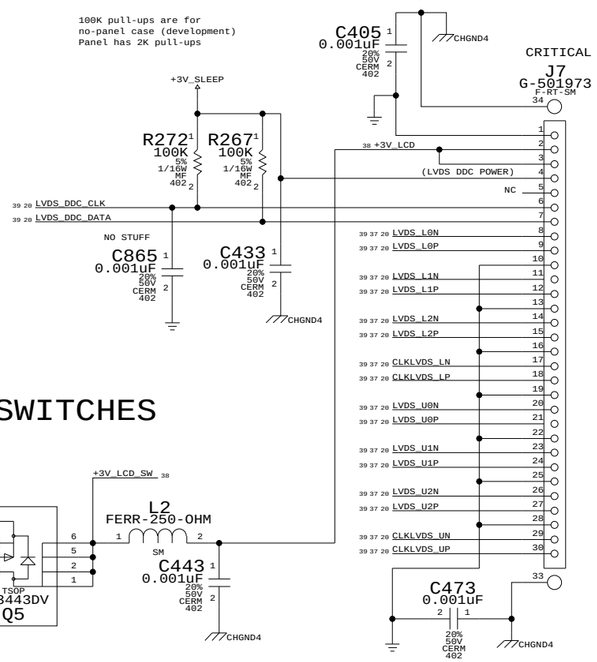
Power key detect path when system is running. HPD normally driven to 3.3V. When power key on remote device pressed, HPD will be driven to 5V. COMPARATOR ENABLED BY NV17MAP GPIO.



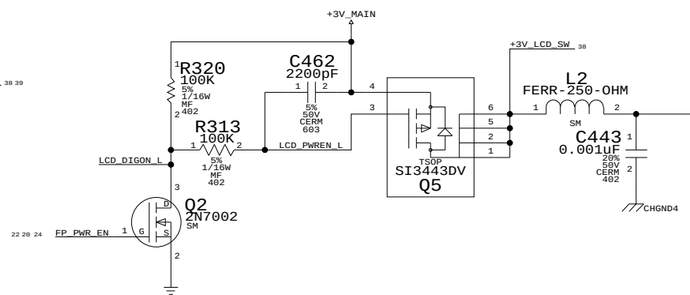
LCD INTERFACE

LVDS INTERFACE

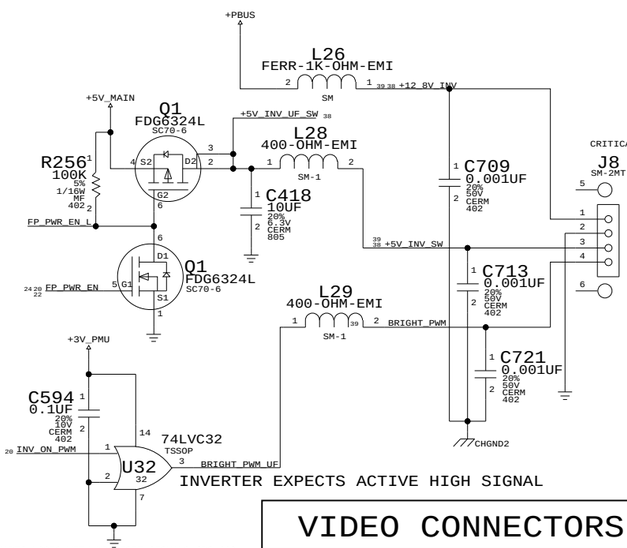
100K pull-ups are for no-panel case (development) Panel has 2K pull-ups



LCD POWER SWITCHES



INVERTER INTERFACE



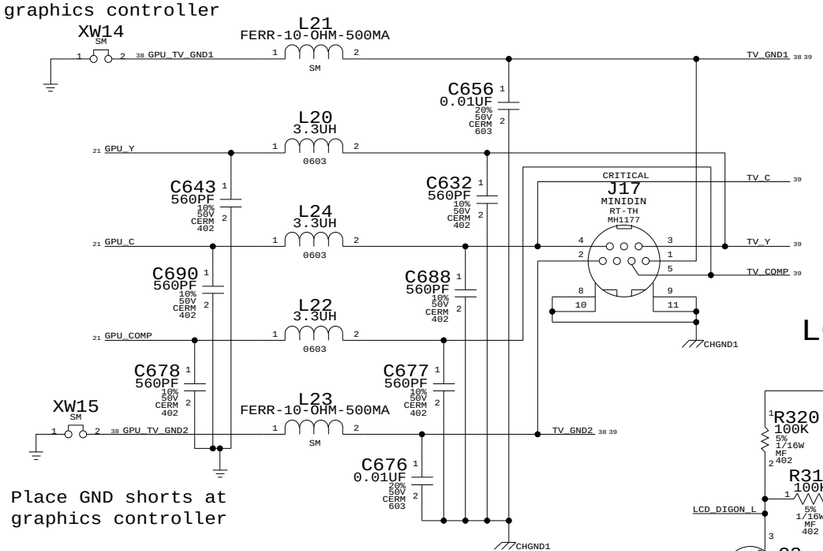
INVERTER EXPECTS ACTIVE HIGH SIGNAL

SHARES LOGIC WITH KB RESET SIGNALS (PG 28)

R2200 0
C601 0.01uF
CHGND2

S-VIDEO/COMP OUT INTERFACE

Place GND shorts at graphics controller



Place GND shorts at graphics controller

VIDEO CONNECTORS

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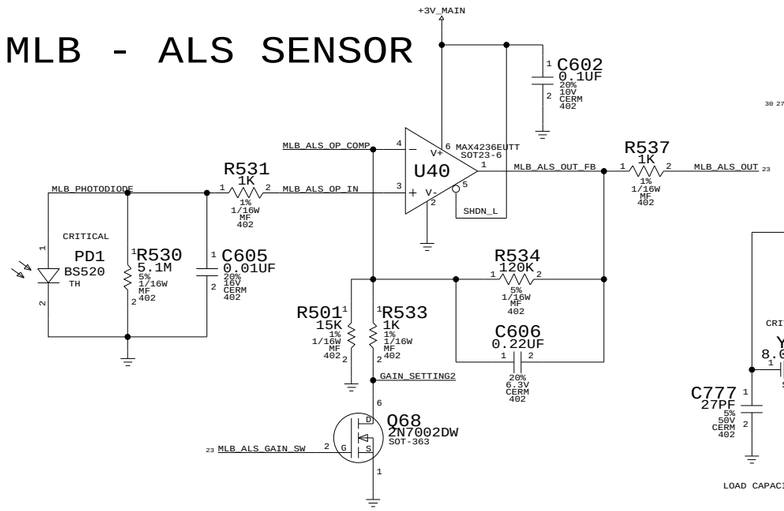
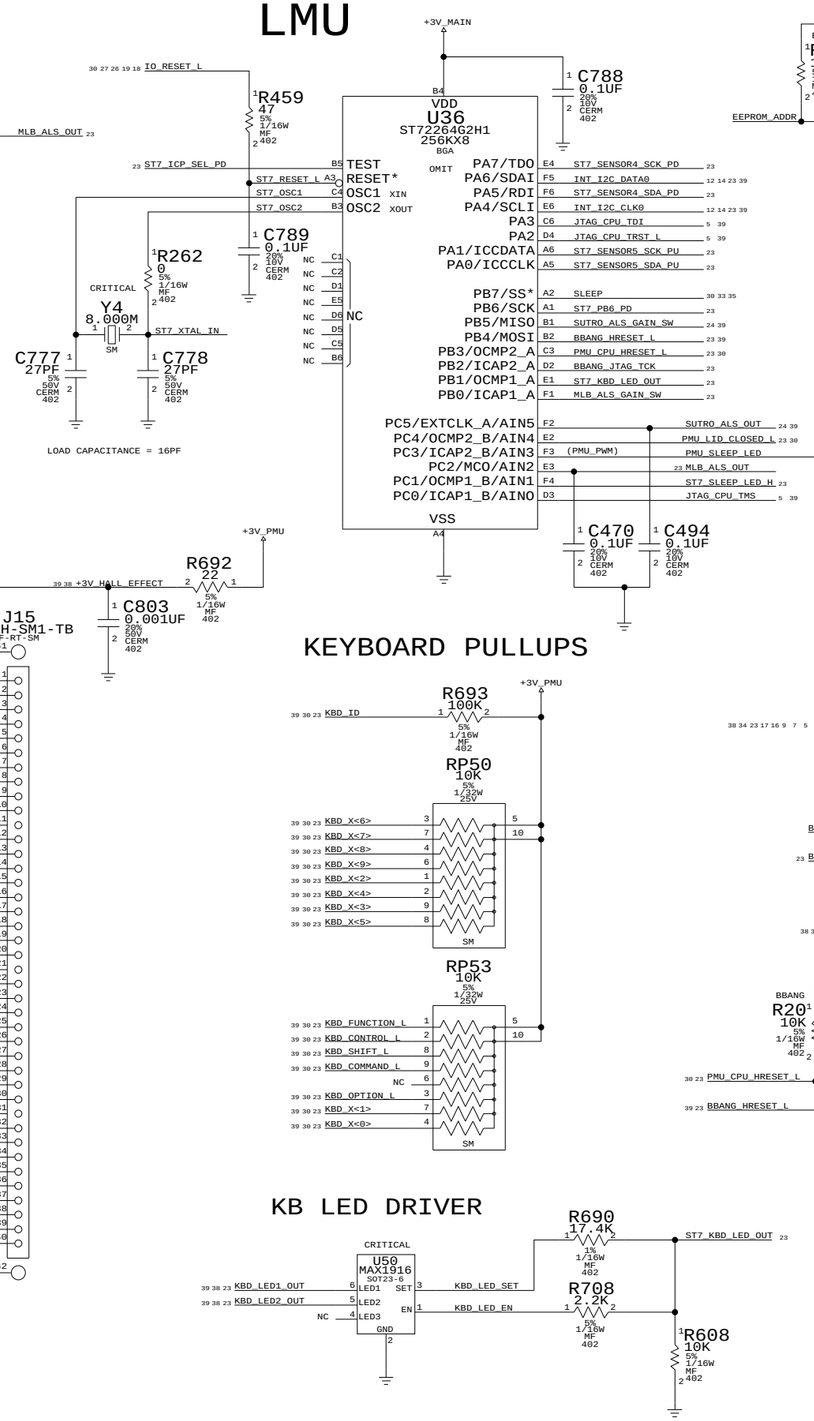
D	051-6469	E
SCALE: NONE	SHT 22 OF 44	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1194	1	IC,LMU,P84	U36	CRITICAL	?

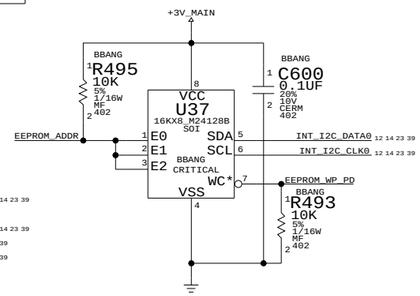
MLB - ALS SENSOR



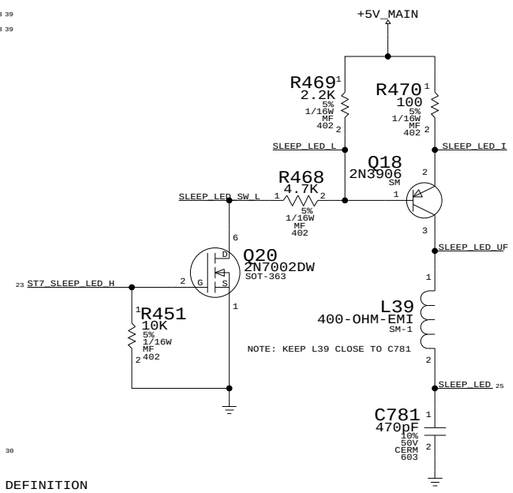
LMU



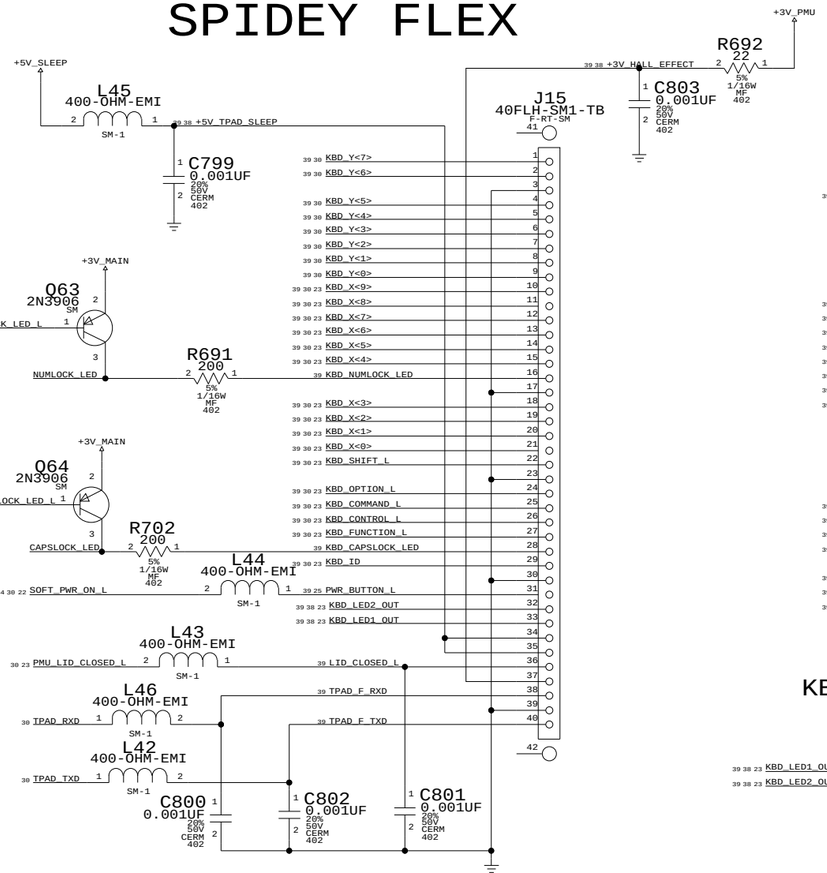
BOOT BANGER E2PROM



SLEEP LED



SPIDEY FLEX

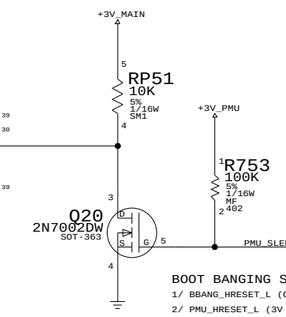


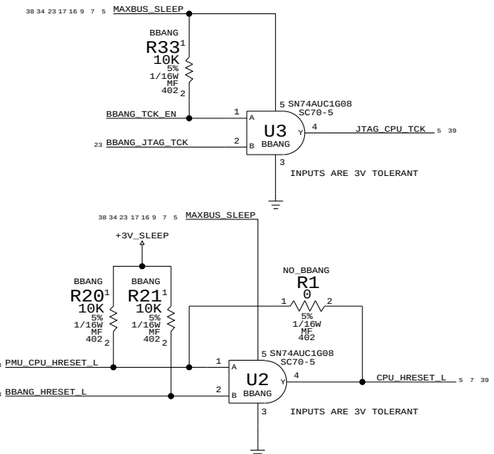
KEYBOARD PULLUPS

KB LED DRIVER

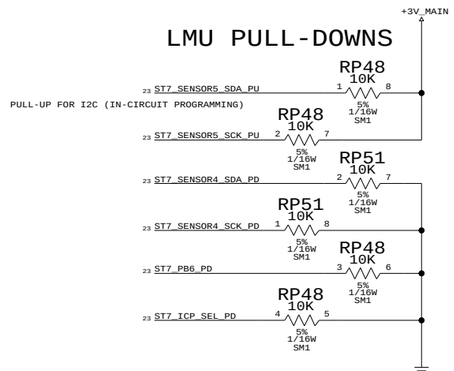
BOOT BANGING SIGNAL DEFINITION

1/ BBANG_HRESET_L (OPEN COLLECTOR OUTPUT - 10K PULLUP ON MLB)
2/ PMU_HRESET_L (3V INPUT INTO LMU)
3/ BBANG_JTAG_TCK (REGULAR OUTPUT)
4/ JTAG_CPU_TMS (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
5/ JTAG_CPU_TDI (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
6/ JTAG_CPU_TRST_L (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)





LMU PULL-DOWNS



LMU/BOOTBANGER/SPIDEY

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APPLE COMPUTER INC.

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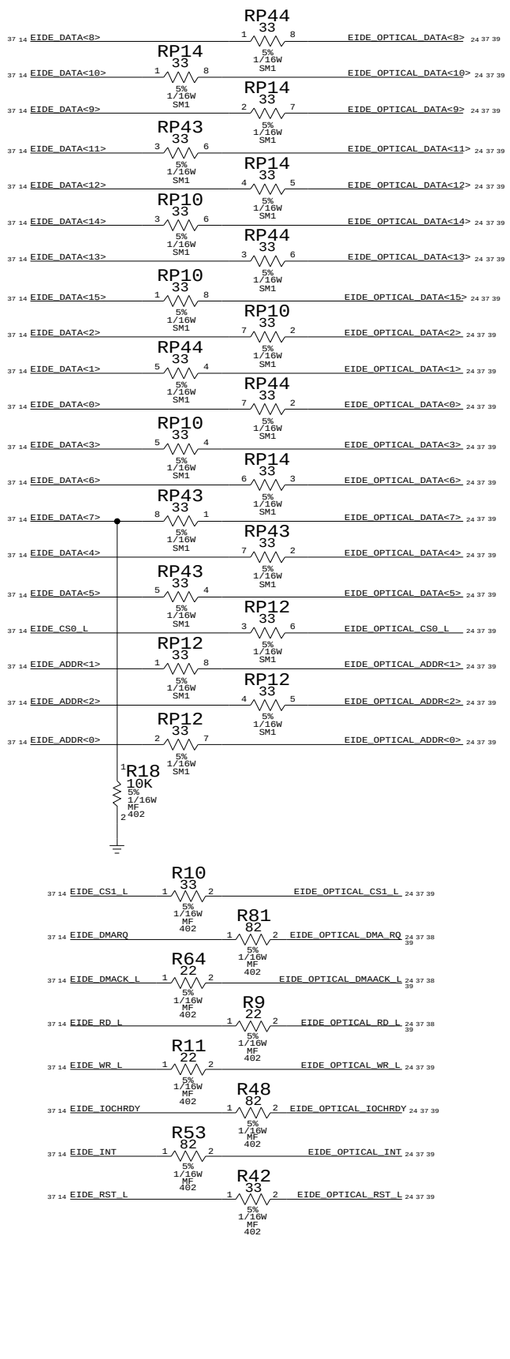
D	051-6469	E

SCALE	SHT	OF
NONE	23	44

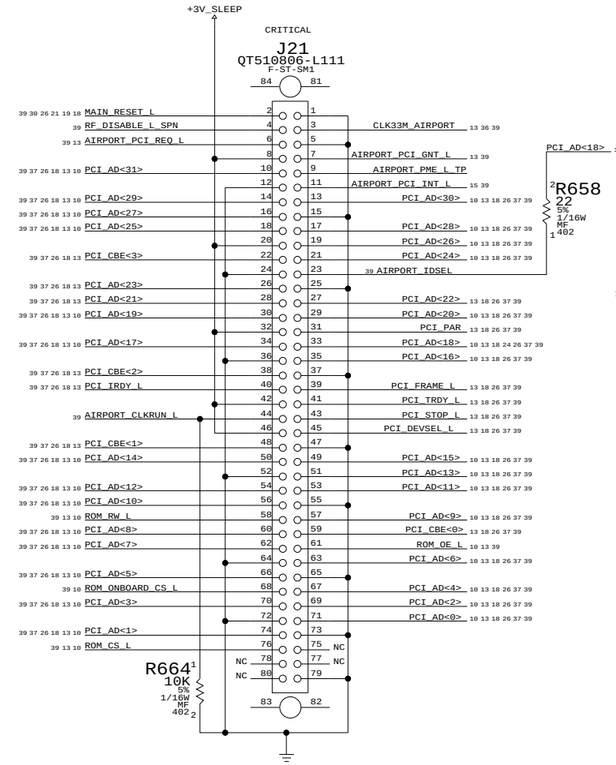
HARD DRIVE INTERFACE (UATA100)

EIDE SERIES TERMINATION

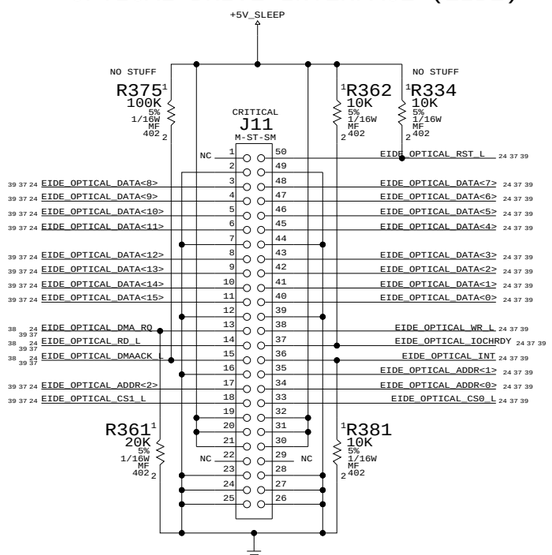
PLACE TERMINATORS NEAR INTREPID



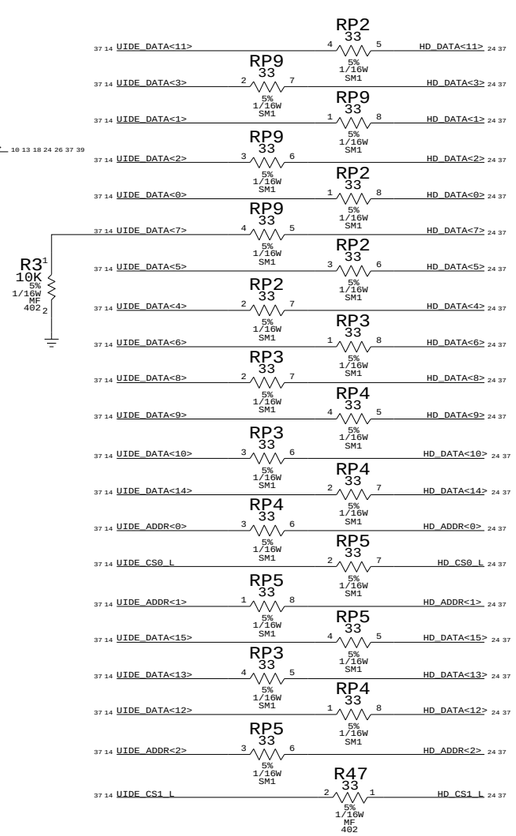
WIRELESS INTERFACE



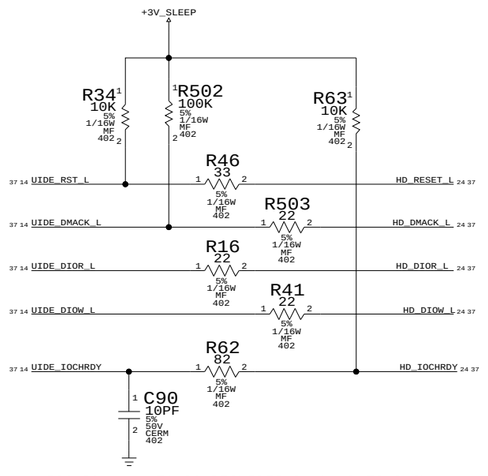
OPTICAL DRIVE INTERFACE (EIDE)



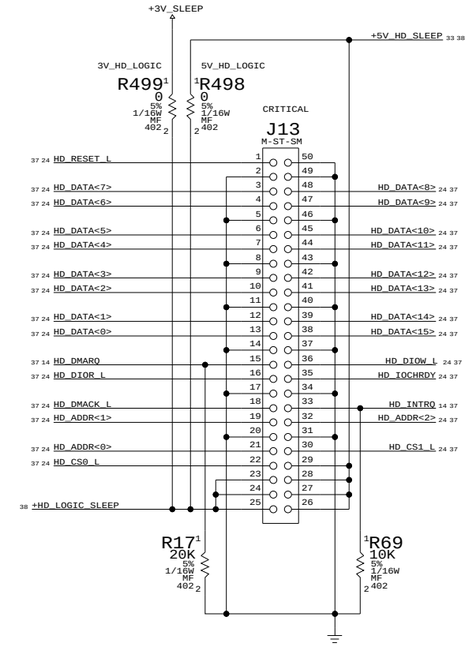
PLACE SERIES R CLOSE TO INTERPID



PLACE PULLUP RESISTORS CLOSE TO INTREPID

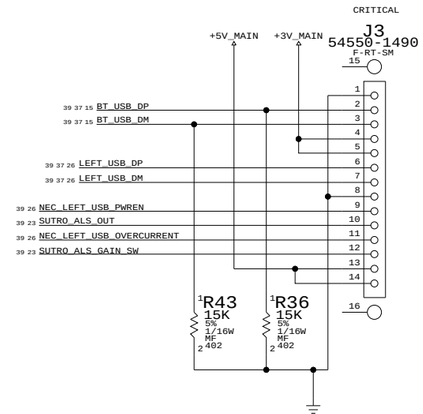


IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V



ANY SEQUENCING REQUIREMENT BETWEEN +5V_HD_SLEEP AND +3V_SLEEP?

BLUETOOTH/LEFT-SIDE USB



INTERNAL I/O CONNECTORS

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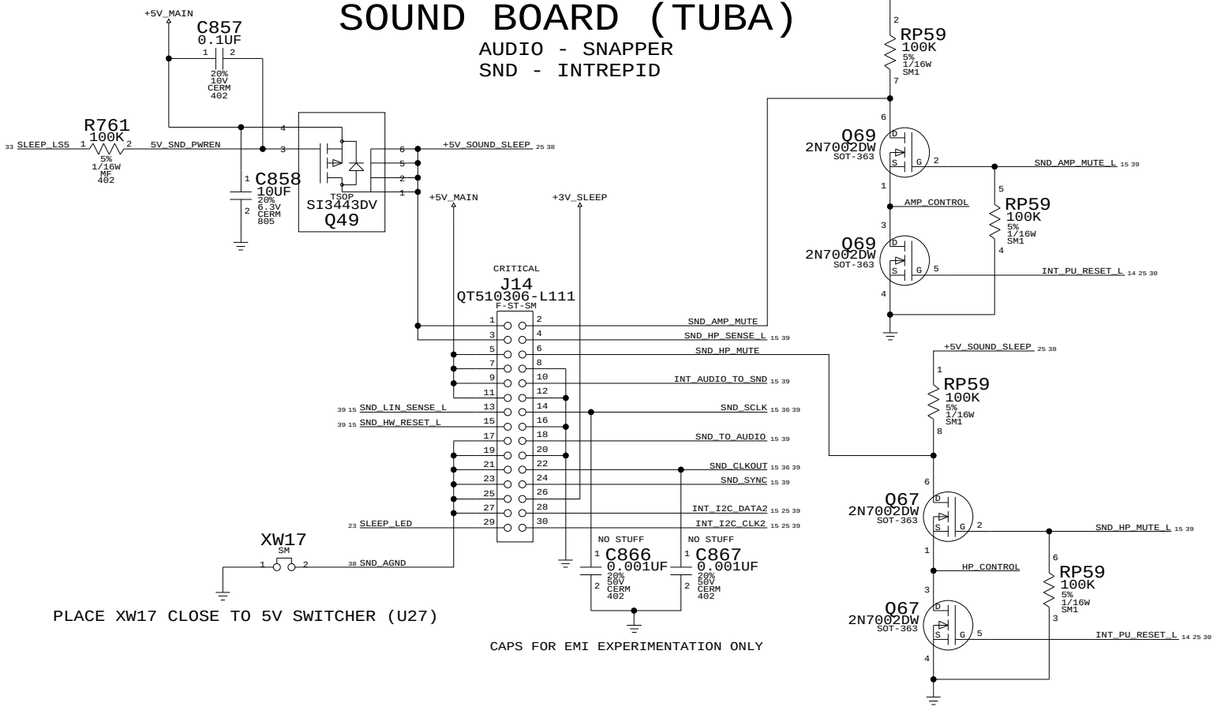
D	051-6469	E
SCALE: NONE	SHT 24 OF 44	

SOUND BOARD (TUBA)

AUDIO - SNAPPER
SND - INTREPID

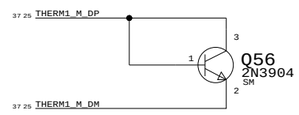


PLACE XW17 CLOSE TO 5V SWITCHER (U27)

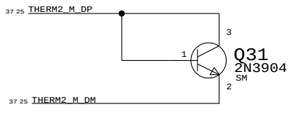
CAPS FOR EMI EXPERIMENTATION ONLY

FAN INTERFACE

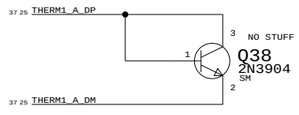
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY
MAIN1



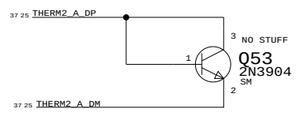
PLACE CLOSE TO CPU
MAIN2



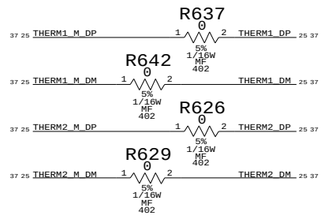
PLACE UNDERNEATH UPPER RAM
ALTERNATE1



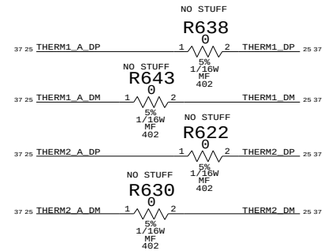
PLACE CLOSE TO BATTERY CHARGER/VCORE
ALTERNATE2



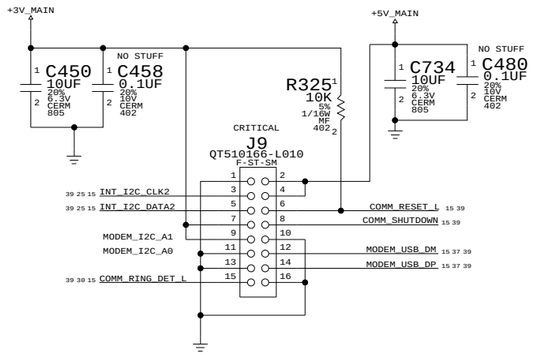
KEEP STUFFING RESISTORS CLOSE TO ADM1031 CONTROLLER



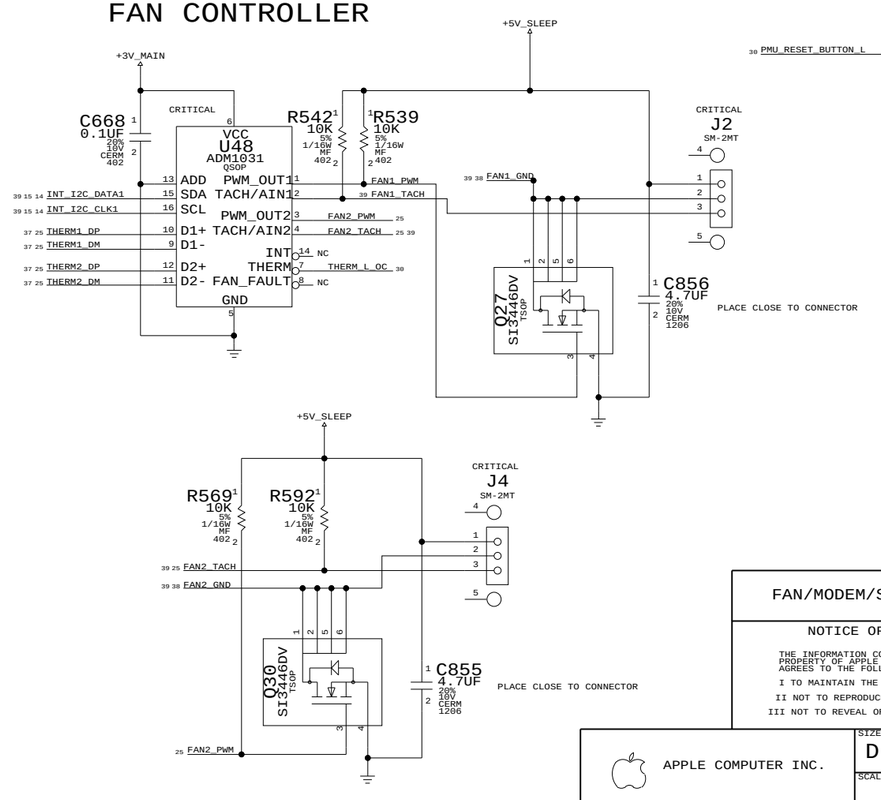
KEEP STUFFING RESISTORS CLOSE TO ADM1031 CONTROLLER



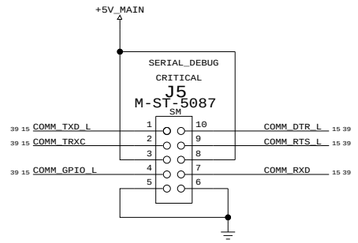
MODEM



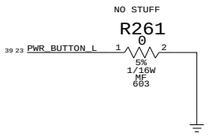
FAN CONTROLLER



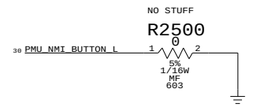
SERIAL DEBUG INTERFACE



DEBUG POWER BUTTON



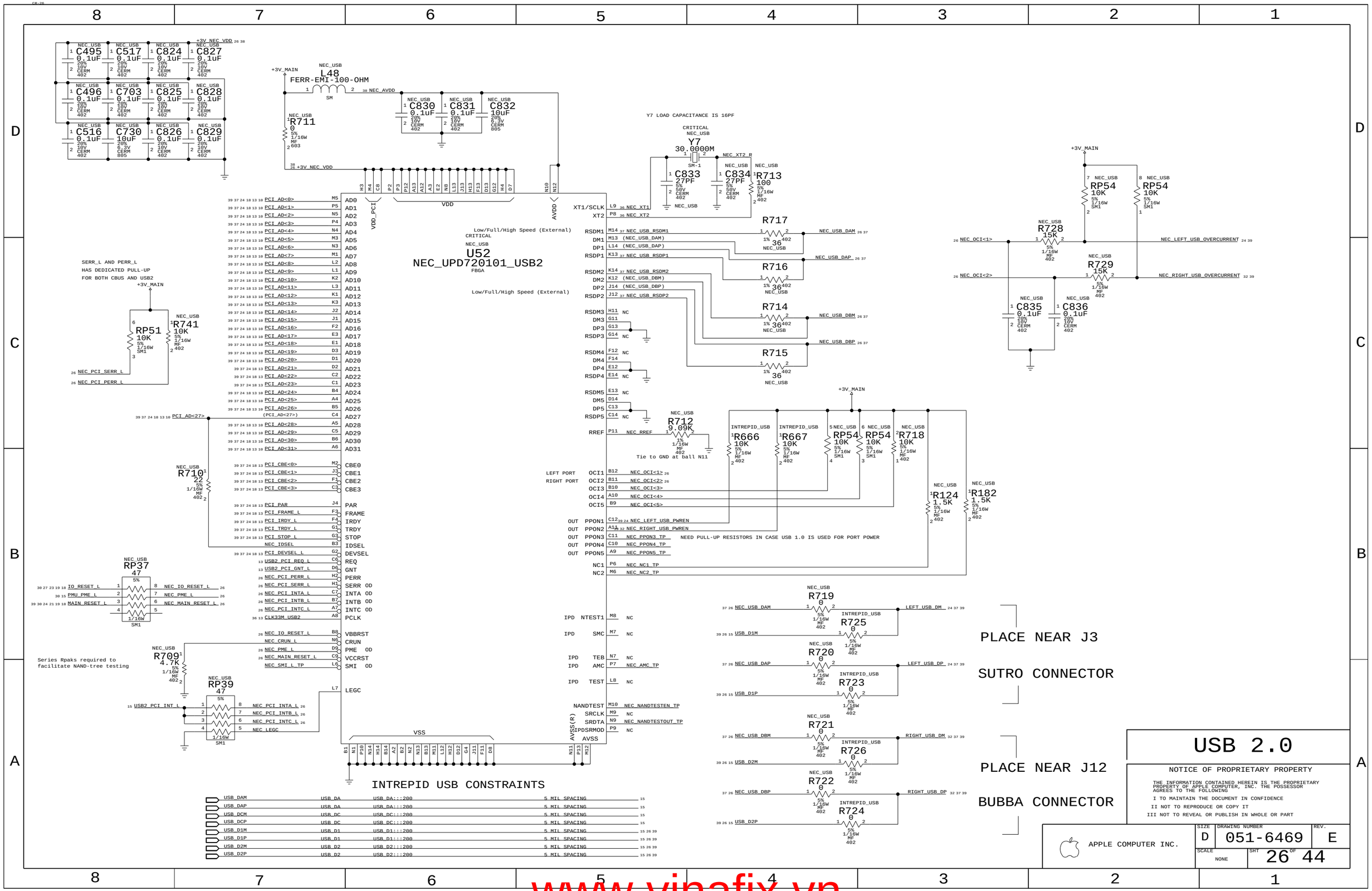
DEBUG JUMPERS

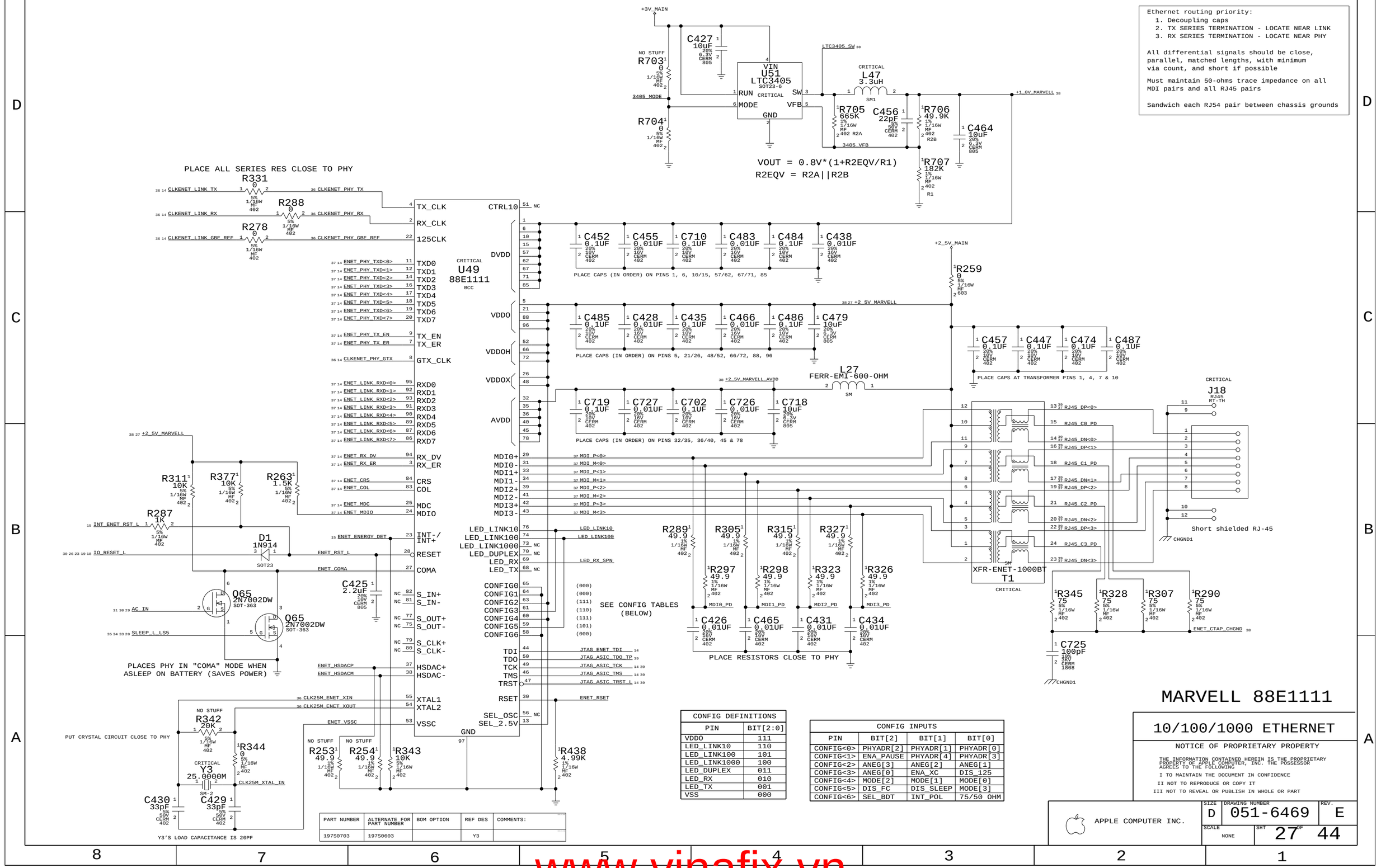


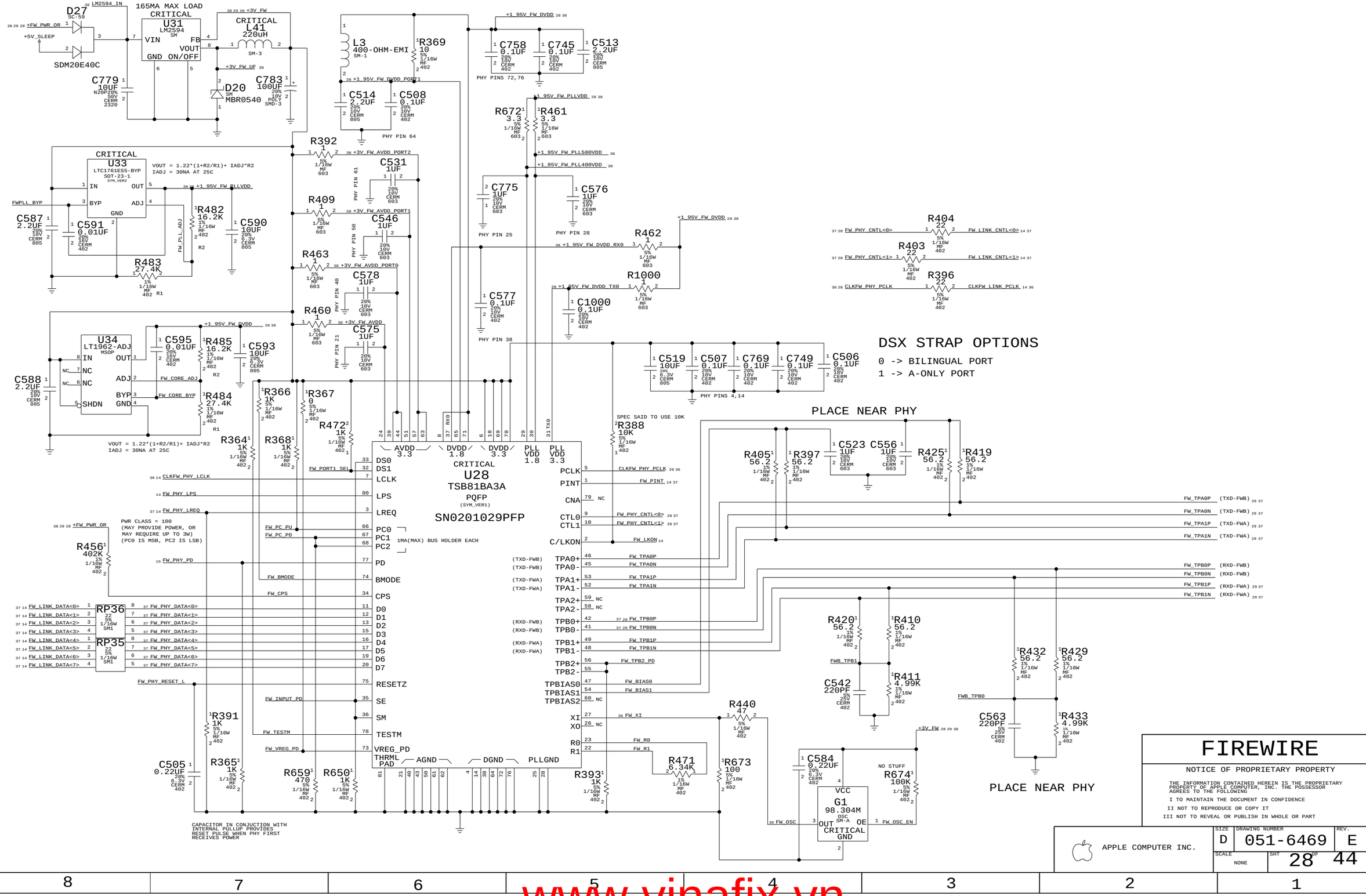
FAN/MODEM/SOUND/SLEEP LED/DEBUG

APPLE COMPUTER INC.

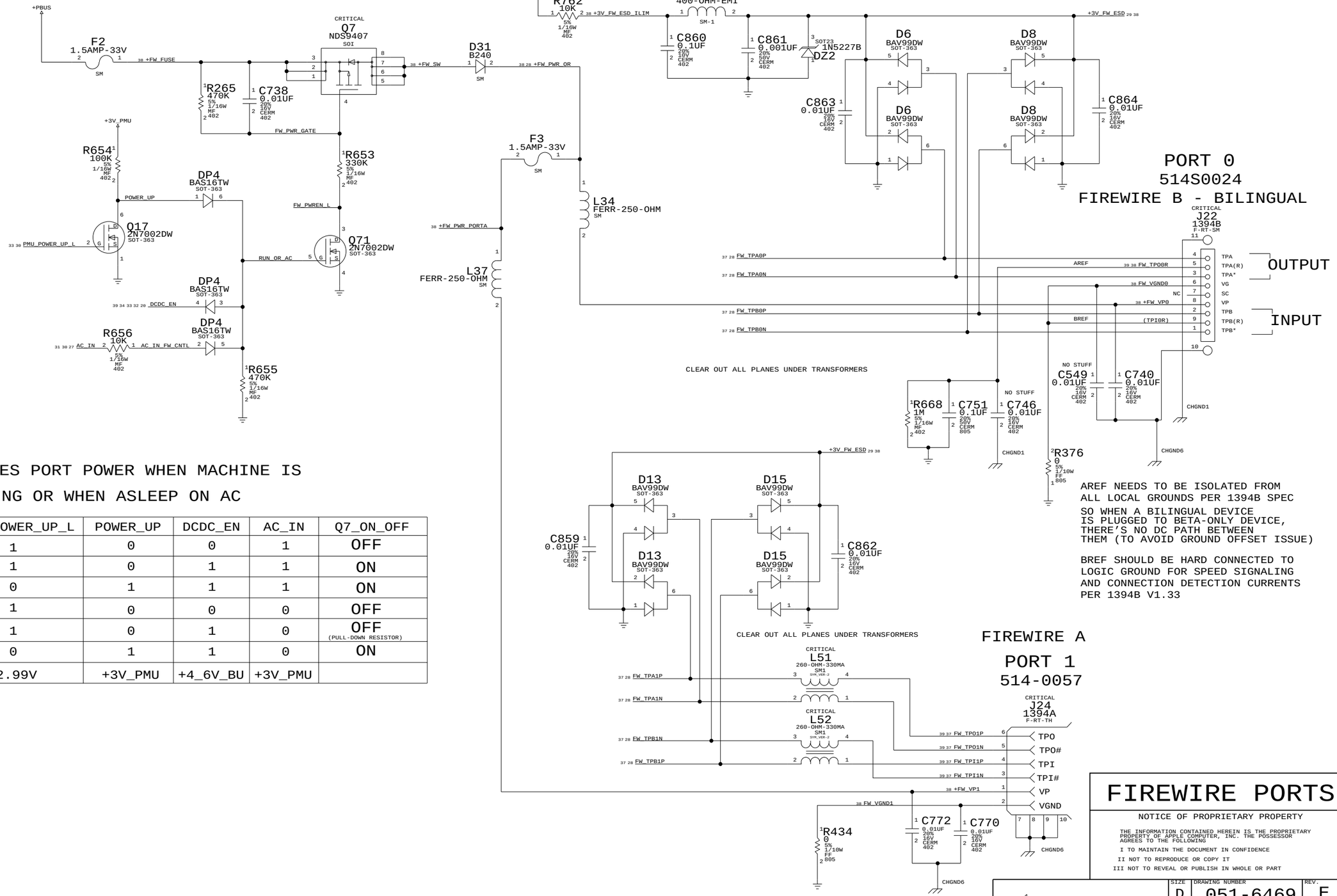
SIZE	DRAWING NUMBER	REV.
D	051-6469	E
SCALE: NONE	SHT 25 OF 44	







PORT POWER SWITCH



ENABLES PORT POWER WHEN MACHINE IS
RUNNING OR WHEN ASLEEP ON AC

STATE	PMU_POWER_UP_L	POWER_UP	DCDC_EN	AC_IN	Q7_ON_OFF
SHUTDOWN (AC)	1	0	0	1	OFF
SLEEP (AC)	1	0	1	1	ON
RUN (AC)	0	1	1	1	ON
SHUTDOWN (BATT)	1	0	0	0	OFF
SLEEP (BATT)	1	0	1	0	OFF (PULL-DOWN RESISTOR)
RUN (BATT)	0	1	1	0	ON
	2.99V	+3V_PMU	+4_6V_BU	+3V_PMU	

FIREWIRE PORTS

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D	051-6469	E
SCALE: NONE	SHT 29 OF 44	

+3V_PMU
R450 470K 1/16W MF 402 CHARGE_LED_L 30 31 39
R478 10K 1/16W MF 402 PMU_POWER_UP_L 29 30 33
R481 10K 1/16W MF 402 SOFT_PWR_ON_L 22 23 30 34
R695 100K 1/16W MF 402 MAIN_RESET_L 18 19 21 24 26 30 39
RP52 100K 1/16W SM1 IO_RESET_L 18 19 23 26 27 30
RP52 100K 1/16W SM1 SLEEP 23 30 33 35
RP52 100K 1/16W SM1 INT_RESET_L 10 14 30
RP52 100K 1/16W SM1 INT_SUSPEND_REQ_L 9 30
R689 1K 1/16W MF 402 PMU_BYTE 30
R490 10K 1/16W MF 402 PMU_CNVSS 30

+3V_PMU
C589 10UF 20% 6.3V CERM 805
C798 0.1UF 20% 10V CERM 402
C797 0.1UF 20% 10V CERM 402
R686 4.7 5% 1/16W MF 402 +3V_PMU_AVCC 30 38
C791 0.1UF 20% 10V CERM 402

VCC 14 60 97 AVCC
VSS 12 62 94

R448 2.2K 5% 1/16W MF 402 NUMLOCK_LED_L 23
R449 2.2K 5% 1/16W MF 402 CAPSLOCK_LED_L 23

U39 M16C62 FLAS OMIT

KBD_Y<0> 39 23	86	P00_D0	P50_WRL_WR
KBD_Y<1> 39 23	85	P01_D1	P51_WRH_BHE
KBD_Y<2> 39 23	84	P02_D2	P52_RD
KBD_Y<3> 39 23	83	P03_D3	P53_BCLK
KBD_Y<4> 39 23	82	P04_D4	P54_HLDA
KBD_Y<5> 39 23	81	P05_D5	P55_HOLD
KBD_Y<6> 39 23	80	P06_D6	P56_ALE
KBD_Y<7> 39 23	79	P07_D7	P57_RDY_CLKOUT
PMU_NUMLOCK_LED_L	78	P10_D8	P60_CTS0_RTS0
PMU_CAPSLOCK_LED_L	77	P11_D9	P61_CLK0
CHARGE_LED_L 39 31 30	76	P12_D10	P62_RXD0
PMU_POWER_UP_L 33 30 29	75	P13_D11	P63_TXD0
NC	74	P14_D12	P64_CTS1_RTS1_CTS0_CLKS1
SOFT_PWR_ON_L 34 30 23 22	73	P15_D13_INT3	P65_CLK1
COMM_RING_DET_L 39 25 15	72	P16_D14_INT4	P66_RXD1
INT_WATCHDOG_L 15	71	P17_D15_INT5	P67_TXD1
KBD_X<0> 39 23	70	P20_A0_D0	P70_TXD2_SDA_TA0OUT
KBD_X<1> 39 23	69	P21_A1_D1_D0	P71_RXD2_SCL_TA0IN_TB5IN
KBD_X<2> 39 23	68	P22_A2_D2_D1	P72_CLK2_TA1OUT_V
KBD_X<3> 39 23	67	P23_A3_D3_D2	P73_CTS2_RTS2_TA1IN_V
KBD_X<4> 39 23	66	P24_A4_D4_D3	P74_TA2OUT_W
KBD_X<5> 39 23	65	P25_A5_D5_D4	P75_TA2IN_W
KBD_X<6> 39 23	64	P26_A6_D6_D5	P76_TA3OUT
KBD_X<7> 39 23	63	P27_A7_D7_D6	P77_TA3IN
KBD_X<8> 39 23	61	P30_A8_D7	P80_TA4OUT_U
KBD_X<9> 39 23	59	P31_A9	P81_TA4IN_U
IO_RESET_L 30 27 26 23 19 18	58	P32_A10	P82_INT0
KBD_COMMAND_L 39 23	57	P33_A11	P83_INT1
KBD_CONTROL_L 39 30 23	56	P34_A12	P84_INT2
KBD_SHIFT_L 39 30 23	55	P35_A13	P85_NMI
KBD_OPTION_L 39 30 23	54	P36_A14	P86_XCOUT
KBD_FUNCTION_L 39 23	53	P37_A15	P87_XCIN
PMU_INT_L 15	52	P40_A16	P90_TB0IN_CLK3
KBD_ID 39 23	51	P41_A17	P91_TB1IN_SIN3
CPU_PLL_STOP_OC 7	50	P42_A18	P92_TB2IN_SOUT3
SLEEP 35 33 30 23	48	P43_A19	P93_DA0_TB3IN
	47	P44_CS0	P94_DA1_TB4IN
INT_SUSPEND_ACK_L 9	46	P45_CS1	P95_ANEX0_CLK4
INT_SUSPEND_REQ_L 30 9	45	P46_CS2	P96_ANEX1_SOUT4
		P47_CS3	P97_ADTRG_SIN4
PMU_BYTE 30	6	BYTE	P100_AN0
	11	XOUT	P101_AN1
	13	XIN	P102_AN2
PMU_RESET_L	10	RESET	P103_AN3
+3V_PMU_AVCC 38 30	96	VREF	P104_AN4_KI0
PMU_CNVSS 30	7	CNVSS	P105_AN5_KI1
			P106_AN6_KI2
			P107_AN7_KI3

CPU_VCORE_HI_OC/PMU_AP should have a pulldown for coming out of reset. MLB will have a pull-up to +3V_MAIN or +3V_SLEEP, which will act as our pulldown since both are off during PMU reset.

(PMU_AP)

44	CPU_VCORE_HI_OC	7 34
43	INT_RESET_L	10 14 30
42	MAIN_RESET_L	18 19 21 24 26 30 39
41	NC	
40	PMU_INT_NMI	15
39	PMU_EPM	30
38	INT_PU_RESET_L	14 25 30
37	PMU_CPU_HRESET_L	23
36	PMU_ACK_L	15
35	PMU_CLK	15
34	PMU_FROM_INT	15
33	PMU_TO_INT	15
32	PMU_REQ_L	15
31	PMU_LID_CLOSED_L	23 30
30	PMU_RESET_BUTTON_L	25 30
29	PMU_NMI_BUTTON_L	25 30
28	TPAD_RXD	23 30
27	TPAD_TXD	23 30
26	SYSTEM_CLK_EN	15
25	CPU_CLK_EN	9
24	PMU_CHARGE_V	31
23	PMU_CHRG_BATT_0	31
22	NC (CHARGE_I)	
21	NC	
20	PMU_SLEEP_LED_L	23
19	CPU_SMI_L	5
18	POWER_VALID	30
17	PMU_PME_L	15 26 30
16	INT_PEND_PROC_INT	15
15	PMU_NMI_L	30
9		
8	CLK32K_PMU_XOUT	
5	PMU_BATT0_DET_L	
4	PMU_BATT1_DET_L_PU	30
3	NC	
2	NC	
1	INT_PROC_SLEEP_REQ_L	15
100	PMU_POWERUP_OK	30
99	NC	
98	PMU_OOPS	30
95	THERM_L_OC	25 30
93	PMU_AC_IN	
92	PMU_AC_DET	30
91	NC	
90	PMU_I2C_CLK	30
89	PMU_I2C_DATA	30
88	PMU_SMB_CLK	30 31
87	PMU_SMB_DATA	30 31

Keep crystal subcircuit close to PMU.
CLK32K_PMU_XIN
R479 1K 1/16W MF 402 PMU_BATT_DET_L 30 31 39
R444 1K 1/16W MF 402 AC_IN 27 29 31
NO STUFF R688 10M 1/16W MF 402
R687 0 1/16W MF 402 CLK32K_PMU_XOUT_UF
CRITICAL Y6 SM-1
32.768K
C796 12PF 5% 50V CERM 402
C794 12PF 5% 50V CERM 402
Y6'S LOAD CAPACITANCE IS 12.5PF

+3V_PMU
R696 10K 5% 1/16W MF 402 PMU_EPM 30
R699 10K 5% 1/16W MF 402 PMU_RESET_BUTTON_L 30 25
R442 100K 5% 1/16W MF 402 PMU_POWERUP_OK 30
R477 470K 5% 1/16W MF 402 PMU_BATT1_DET_L_PU 30
R480 470K 5% 1/16W MF 402 PMU_BATT_DET_L 39 31 30
RP49 10K 5% 1/16W SM1 PMU_NMI_BUTTON_L 30 25
RP49 10K 5% 1/16W SM1 PMU_NMI_L 30
R446 7.15K 1% 1/16W MF 402 PMU_SMB_DATA 31 30
R447 7.15K 1% 1/16W MF 402 PMU_SMB_CLK 31 30
+3V_SLEEP
RP49 10K 5% 1/16W SM1 PMU_I2C_DATA 30
RP49 10K 5% 1/16W SM1 PMU_I2C_CLK 30
+5V_SLEEP
R700 10K 5% 1/16W MF 402 TPAD_RXD 30 23
R701 10K 5% 1/16W MF 402 TPAD_TXD 30 23
+3V_MAIN
R497 100K 5% 1/16W MF 402 POWER_VALID 30
R496 10K 5% 1/16W MF 402 PMU_PME_L 30 26 15
R698 100K 5% 1/16W MF 402 PMU_LID_CLOSED_L 30 23
+3V_PMU_AVCC 38 30
R436 100K 5% 1/16W MF 402 THERM_L_OC 30 25
R443 10K 5% 1/16W MF 402 PMU_OOPS 30
R697 100K 5% 1/16W MF 402 INT_PU_RESET_L 30 25 14

UNDERVOLTAGE RESET CIRCUIT

+3V_PMU
R492 1K 5% 1/16W MF 402
C597 0.1UF 20% 10V CERM 402
+3V_PMU_RESET 34
CRITICAL
U38 MAX6804 SOT143 VCC MR* RSET* GND
PMU_KB_RESET_L 39 30
CLK10M_PMU_XOUT
CLK10M_PMU_XIN
NO STUFF R491 10M 5% 1/16W MF 402
R489 0 5% 1/16W MF 402 CLK10M_PMU_XOUT_UF
CRITICAL Y5 10.00M SM
Keep crystal subcircuit close to PMU.
Y5'S LOAD CAPACITANCE IS 12PF
C592 12PF 5% 50V CERM 402
C598 12PF 5% 50V CERM 402

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0704	197S0604		Y5	Alt crystal size

PMU KEYBOARD RESET CIRCUIT

+3V_PMU
U32 74LVC32 TSSOP
SOFT_PWR_ON_L 34 30 23 22
KBD_CONTROL_L 39 30 23
PMU_KB_RESET_IN1
KBD_SHIFT_L 39 30 23
KBD_OPTION_L 39 30 23
PMU_KB_RESET_IN2
PMU_KB_RESET_L 30 39

Q11 ADAPTER DETECTION SCHEME

CASE	ADAPTER	PIN VOLT	ID VOLT RANGE	SYSTEM STATUS
1	Q11 (65W)	2.007V-2.066V	1.65V-2.31V	RECOGNIZES AS Q11 FULL FUNCTIONS
2	A29 (45W)	2.558V-2.661V	2.31V-2.97V	RECOGNIZES AS A29 LIMITED FUNCTIONS
3	AIRLINE	0.589V-0.663V	0.33V-0.99V	FULL FUNCTIONS NO BATTERY CHARGING
4	HOOPER	3.19V-3.28V	2.97V-3.30V	RECOGNIZES AS HOOPER LIMITED FUNCTIONS

A29 DETECT CIRCUIT

+3V_PMU
+4.85V_RAW 38 32
R430 100K 1% 1/16W MF 402
ADAPTER_DET 31 39
R445 100K 1% 1/16W MF 402
PMU_AC_DET 30
R902 402K 1% 1/16W MF 402
2.34V_REF
R266 5.23K 1% 1/16W MF 402
C257 0.1UF 20% 10V CERM 402
R324 10K 5% 1/16W MF 402
A29_DETECT 31
U53 LMC7211 SM
A29_DET_L
Q57 2N7002 SM
R270 499K 1% 1/16W MF 402
R269 12.7K 1% 1/16W MF 402
50MV OF HYSTERSIS

PMU

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SIZE D | DRAWING NUMBER 051-6469 | REV. E
SCALE NONE | SHT 30 OF 44

DC POWER INPUT

(POWER JACK, ETC. ON SEPARATE BOARD)

CRITICAL

J19
87438-0833
M-RT-SM

CHARGE_LED_L
+ADAPTER
ADAPTER_DET

R473 20K 1% 1/16W MF 402
R309 102K 1% 1/16W MF 402
R292 100K 1% 1/16W MF 402
R301 10K 1% 1/16W MF 402
R293 57.6K 1% 1/16W MF 402

C449 0.01UF 20% 16V CERM 402
R291 10K 5% 1/16W MF 402
R316 1M 5% 1/16W MF 402
U16 LMC7211 SM
1V20_REF
AC_DIV
AC_IN
AC_IN_L
Q4 2N7002DW SOT-363
R308 470K 5% 1/16W MF 402

GREATER THAN 13.5V DETECT

DC INRUSH LIMITER

Q8 SI4435DY SOI
Q10 SI4435DY SOI
+ADAPTER_SW
+ADAPTER_SENSE
GATE

R336 330K 5% 1/16W MF 402
C439 0.1UF 20% 50V CERM 805
R394 47K 5% 1/16W MF 402
AC_ENABLE_GATE
R300 470K 5% 1/16W MF 402
AC_ENABLE_L
BCKFD_PROT_GATE
C843 0.1UF 20% 50V CERM 805
R414 68K 5% 1/16W MF 402
BCKFD_PROT_EN_L
Q14 2N7002DW SOT-363
AC_IN

C532 0.01UF 20% 50V CERM 603

PLACE U24 NEXT TO R382

U24 SENSE VOLTAGE DROP ACROSS R382

U24 MAX4172 TSSOP
RS+ RS- NC1 NC2 PG OUT GND
MAX4172_OUT
R384 2.21K 0.1% 1/16W MF 603

R382 0.025 1% 1W MF 2512
IF A29 ADAPTER USED, ADJUST CURRENT SETTING

R406 4.7 5% 1/16W MF 402
R413 4.7 5% 1/16W MF 402
1772_CSSP
1772_CSSN
C534 0.47UF 20% 50V CERM 1206
C535 0.47UF 20% 50V CERM 1206

1MSEC INTEGRATION TIME

R744 1K 1% 1/16W MF 402
C757 0.1UF 20% 16V CERM 402
IAC_RC_COMP
+3V_PMU
C472 0.1UF 20% 16V CERM 402
R745 42.2K 0.1% 1/16W FF 603
U54 LMC7111 SOT23-5
IAC_FB
R742 10K 1% 1/16W MF 402
CURRENT_THRESHOLD

PLACE R383 CLOSE TO LTC1625
ROUTE LTC1625_ITH CAREFULLY

DP3 BAS16TW SOT-363
LTC1625_ITH
R383 150 1% 1/16W MF 402
1625_COMP
ADAPTER_I_REG

R743 42.2K 0.1% 1/16W FF 603
R371 82.5K 0.1% 1/16W MF 603
R746 51.1K 0.1% 1/16W MF 603
IF ADAPTER IS OVER 18V, ADJUST CURRENT SETTING
A29_CURRENT_ADJ
R747 100K 5% 1/16W MF 402
OVER_18V_ADJ
A29_DETECT
Q3100 2N7002DW SOT-363
AC_GTR_18V
C838 1UF 20% 10V CERM 603
Q66 2N7002DW SOT-363
1772_ACOK_L

BATTERY SWITCH-OVER CIRCUIT

+BATT
+24V_PBUS
+PBUS
F5 5AMP-125V SM-2
F4 5AMP-125V SM-2
+BATT_24V_FUSE
+BATT_14V_FUSE
D30 RS3AB SM
D28 RS3AB SM
Q16 SI4435DY SOI
Q60 IRF7416 SOI
R407 47K 5% 1/16W MF 402
R660 47K 5% 1/16W MF 402
BATT_24V_GATE
BATT_14V_GATE
R422 10K 5% 1/16W MF 402
R657 10K 5% 1/16W MF 402
DP3 BAS16TW SOT-363
BATT_24PBUS_EN
BATT_14PBUS_EN
AC_IN_L
AC_IN_L_RC
R415 470K 5% 1/16W MF 402
Q14 2N7002DW SOT-363
C551 10UF 20% 6.3V CERM 805

WHEN AC IS IN, P-CHANNEL FETS ARE QUICKLY (DIODE) TURNED OFF
WHEN AC IS NOT PLUGGED, P-CHANNEL FETS ARE ON
RC TIME IS 480K*10UF @ +3V_PMU

SWITCHER VOLTAGE CONTROL

PMU SELECTS BETWEEN TWO VOLTAGES

R476 27.4K 1% 1/16W MF 402
R464 10K 1% 1/16W MF 402
R457 10K 1% 1/16W MF 402
R466 4.12K 1% 1/16W MF 402
R474 48.7K 1% 1/16W MF 402
R467 100K 5% 1/16W MF 402
BATTV_HIGH
BATTV_LOW
Q19 2N7002DW SOT-363
R488 5.23K 1% 1/16W MF 402
Q19 2N7002DW SOT-363
PMU_CHARGE_V

SWITCHER CURRENT CONTROL

CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V
CHARGE THROTTLED BY LOW BATTERY VOLTAGE

R663 100K 1% 1/16W MF 402
D10 1N914 SOT23
C550 1UF 20% 50V CERM1 1210
R665 12.7K 1% 1/16W MF 402
OD OUTPUT LOW - WHEN AC GREATER THAN 18V

U30 MAX1772 QSOP
CRITICAL
CSSP CSSN DCIN ACIN ACOK RFIN VCTL ICTL ICHG IINP CCV CCI CCS REF CLS CELLS LDO DLOV BST DHI LX DLO PGND CSIP CSIN BATT GND

R475 1K 1% 1/16W MF 402
R455 1K 1% 1/16W MF 402
BATT_LOW_L
Q22 2N7002DW SOT-363
Q22 2N7002DW SOT-363
R435 1K 1% 1/16W MF 402
C570 0.01UF 20% 16V CERM 402
C565 0.01UF 20% 16V CERM 402
R412 1K 1% 1/16W MF 402
C569 0.1UF 20% 10V CERM 402
1772_CCV_RC
1772_REF
C580 1UF 20% 10V CERM 603
R683 10K 1% 1/16W MF 402
R679 4.12K 1% 1/16W MF 402
1772_CLS
C773 1UF 20% 10V CERM 603
C782 0.1UF 20% 25V CERM 603
C768 0.1UF 20% 25V CERM 603
R465 100K 1% 1/16W MF 402
XW20

R678 33 5% 1/8W FF 1206
D11 1N914 SOT23
1772_BST_ESR
R458 100K 5% 1/16W MF 402
C490 0.1UF 20% 25V CERM 603
R685 4.7 5% 1/16W MF 603
C557 0.1UF 20% 16V CERM 805
1772_LDO
1772_CELLS
1772_DLOV
1772_BST
1772_DHI
1772_LX
1772_DLO
1772_CSIP
1772_CSIN
(GND)

Q54 IRF7805 SM
CRITICAL
C515 2.2UF 20% 25V CERM 1812
C524 2.2UF 20% 25V CERM 1812
C525 2.2UF 20% 25V CERM 1812
C526 2.2UF 20% 25V CERM 1812
C527 2.2UF 20% 25V CERM 1812
L36 10uH SM1
CRITICAL
+BATT_RSNS
R677 0.05 1% 1W MF 2512
+BATT_24V_FUSE
Q55 IRF7811W SO-8
CRITICAL
D29 MBRS140T3 SM
C568 4.7UF 20% 25V CERM 1206
C582 4.7UF 20% 25V CERM 1206
C566 4.7UF 20% 25V CERM 1206
C795 33UF 20% 6V ELEC SM1
R441 1 5% 1/16W MF 603
R421 1 5% 1/16W MF 603
C581 4.7UF 20% 25V CERM 1206
C583 4.7UF 20% 25V CERM 1206
C567 4.7UF 20% 25V CERM 1206

BATTERY CONNECTOR

CRITICAL
J25
87438-0833
M-RT-SM
+BATT_POS
(BATT_IN_PD)
BATT_CLK
BATT_DATA
PMU_BATT_DET_L
BATT_NEG

L7 FERR-EMI-100-OHM SM
L40 FERR-50-OHM SM
L8 FERR-EMI-100-OHM SM
PMU_SMB_CLK
L6 FERR-EMI-100-OHM SM
PMU_SMB_DATA
L9 FERR-50-OHM SM

R486 100K 5% 1/16W MF 402
Q23 2N7002DW SOT-363
CHARGE_DISABLE
Q23 2N7002DW SOT-363
PMU_CHRG_BATT_0

C564 0.1UF 20% 10V CERM 402
U35 LMC7211 SM
BATT_LOW
BATT_DIV
1V65_REF
R680 100K 1% 1/16W MF 402
R487 499K 1% 1/16W MF 402
R682 100K 1% 1/16W MF 402
R681 100K 1% 1/16W MF 402
C774 0.047UF 20% 16V CERM 402

R332 6.34K 1% 1/16W MF 402
A29_CLS_ADJ
Q66 2N7002DW SOT-363
A29_DETECT

V_{BATT} = CELLS X (4.096 + (0.4096 * V_{VCTL} / V_{REFIN}))

For 4.15V cells, VCTL = 0.123 REFIN

For 4.20V cells, VCTL = 0.245 REFIN

I_{CHG} = (0.2048/R_{62}) * (V_{ICTL} / V_{REFIN})

BATTERY CHARGER

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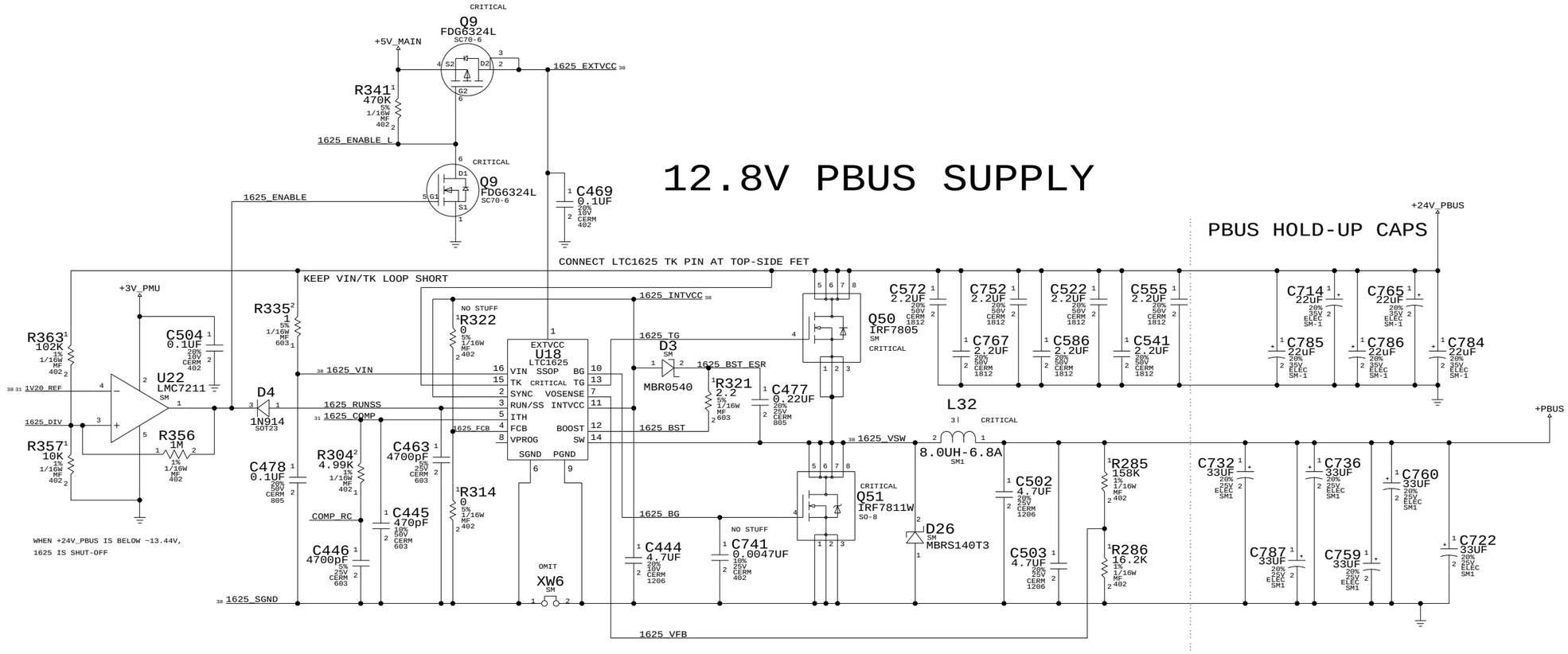
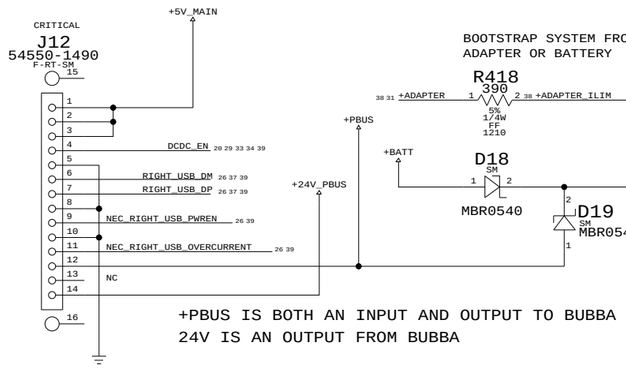
SCALE: NONE	SHT 31 OF 44	

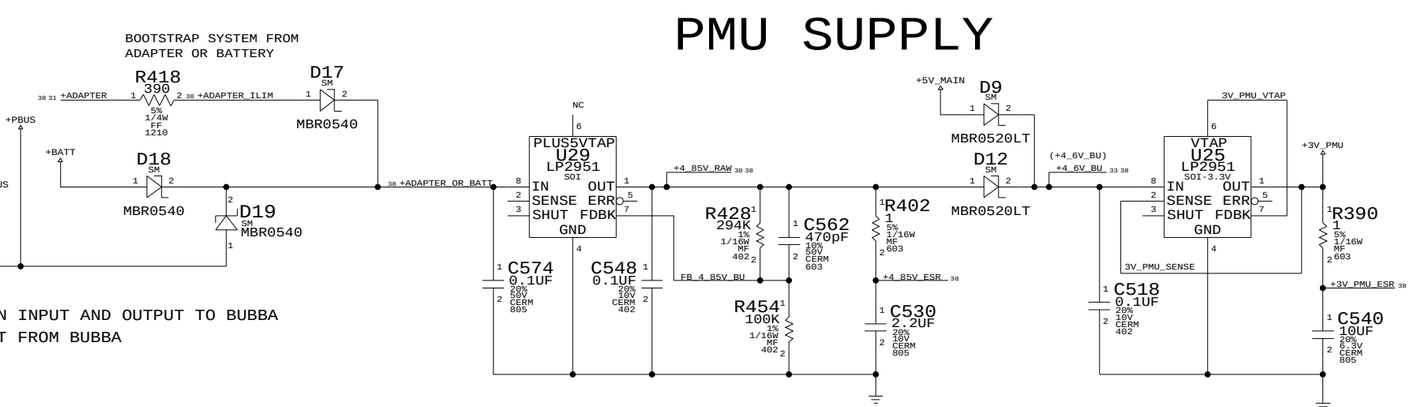
12.8V PBUS SUPPLY



BACKUP BATTERY / USB CONNECTOR



PMU SUPPLY



12.8V REGULATOR

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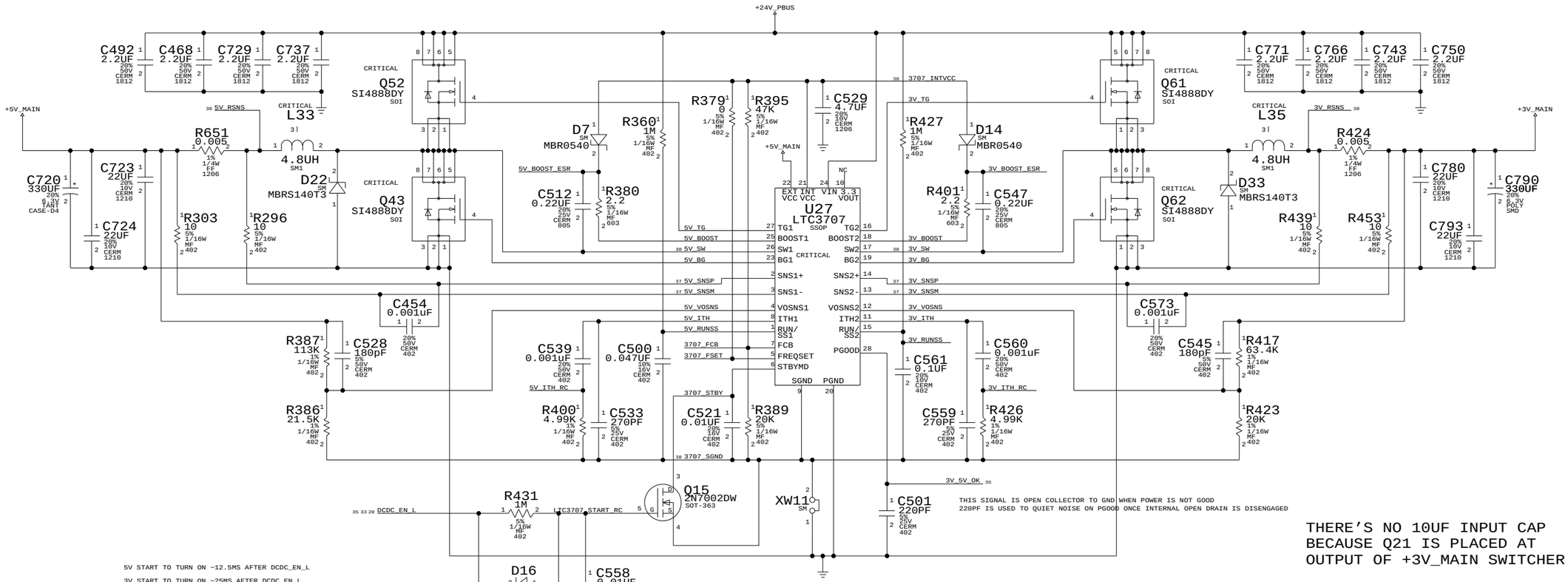
SCALE	SHT	OF
NONE	32	44

3.3V/5V MAIN SUPPLY



3.3V/5V REGULATOR

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SCALE	SHT	OF
NONE	33	44

VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage
(approx. 7ms delay)

NEW 1.35V->1.30V 1GHZ@1.32V->667MHZ@1.145V

MAXBUS_SLEEP
CPU_VCORE_PWR_SEQ
CPU_VCORE_SEQ_L
CPU_VCORE_SEQ
CPU_VCORE_HI_OC
SLEEP_L_LS5
DCDC_EN
INT_GPIO1_PU
MAX1717_AB_SEL
VCORE_VID<0>
VCORE_VID<1>
VCORE_VID<2>
VCORE_VID<3>
VCORE_VID<4>
VCORE_SLOW<1>
VCORE_SLOW<2>
VCORE_SLOW<3>
VCORE_SLOW<4>
VCORE_FAST<1>
VCORE_FAST<2>
VCORE_FAST<3>
VCORE_FAST<4>
VCORE_MUX_SEL
VCORE_MUX_EN
CPU_VCORE_SLEEP

MAX1717 VID CAN TAKE 3.3V TO 5.5V INPUTS

OUTPUT VOLTAGE

V_{DAC} D4=0	V_{DAC} D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

+20MV OFFSET

FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	A/B_ = Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1

If all pull-ups are >=100K and all
pull-downs are <=1K, $V_A = V_B$.

SEL = 0; Y1=A1
SEL = 1; Y1=B1

KEEP TRACE FAT (40-100 MILS) AND SHORT!!

Connect MAX1717 GND pin 13 to GND at bottom-side FET

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V, HENCE VOFFSET = 2.0V * (R1/(R1+R2)) AND VCORE = VDAC + VOFFSET.

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1000	1	RES	0402	RES,MTL FILM,1/16W,0 OHM,5%,0402,SMD	0		1/16W	5%	R306	VCORE_NO_OFFSET

NOTE: R310 (R2) NO STUFFED FOR NO OFFSET CASE

ROUTE AS DIFFERENTIAL PAIR

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
126S0036	7	CAP,AL CAP,AL,POLY,8.2UF,20,16V,V CASE,SMD	C412,C414,C415,C416,C417,C419	CRITICAL	C420

FMAX CONNECTOR

J6 M-ST-SM-52465-1217
VCORE_GNDDIV_TEST
VCORE_GNDSNS_TEST
+3V_PMU_RESET
SOFT_PWR_ON_L
NC (RFU)

VCORE SUPPLY

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SCALE: NONE	SHT 34 OF 44	

1.5V/2.5V SWITCHER

+1_5V_SLEEP LOADS

1) L3 I/O
1) AGP I/O - IF USING D3COLD
1) MAXBUS I/O - IF 1.5V INTERFACE

+1_5V_MAIN LOADS

1) INTREPID CORE
2) AGP I/O IF USING D3HOT

+2_5V_SLEEP LOADS

1) L3 CORE
2) FBCORE/FBIO IF USING D3COLD
3) L3 I/O IF L3_OVDD EXCEEDS 1.5V
4) INTREPID MEMORY I/O

+2_5V_MAIN LOADS

1) MAP17 - FBCORE/FBIO IF USING D3HOT
2) GIGABIT ETHERNET - AVDDL
3) DDR SODIMMS - CORE/IO
4) DDR MUXES
5) CLOCK SLEWING I/O
6) PCI1510 CORE

DIODE PROVIDE PROVIDE QUICK SHUT-DOWN
POWER DOWN DELAY 1.5MS TO 3.5MS

CHANGE R354 BACK TO 10K, 1%, AND STUFF 5.11K FOR 1.5V OPERATION
CONNECTING 1_5V_FB TO GND, FORCES 1.8V OUTPUT

1.8V SWITCHER

+1_8V_MAIN LOADS

1) INTREPID PLLS
2) +1_5V_LDO

+1_8V_SLEEP LOADS

1) MPC7450 - MAXBUS I/O - IF 1.8V INTERFACE
2) CPU JTAG & MaxBus Pull-ups
3) CPU PLL Config Straps
4) L3_OVDD (IF NOT USING 1.5V)

1.5V/1.8V/2.5V SUPPLIES

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SCALE: NONE	SHT 35 OF 44	

DIGITAL SIGNALS

GROUP	SIG_NAME	DELAY_RULE	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
MAXBUS	CPU_AACK_L	:::1500:2500	5		250	10 MIL SPACING			5 9
	CPU_ADDR<0..31>	:::1500:3100	5		250			83 MHZ	5 9
	CPU_ARTRY_L	:::1500:2500	5		250	10 MIL SPACING			5 9
	CPU_BG_L	:::1500:2500	5		250	10 MIL SPACING			5 9
	CPU_BR_L	:::1500:2500	5		250	10 MIL SPACING			5 9
	CPU_CI_L	:::1500:2700	5		250				5 9
	CPU_DATA<0..31>	:::1100:2500	5		250			83 MHZ	6 9
	CPU_DATA<32..63>	:::1100:2500	5		250			83 MHZ	6 9
	CPU_DBG_L	:::1500:2500	5		250	10 MIL SPACING			5 9
	CPU_DTI<0..2>	:::1500:2950	5		250				5 9
	CPU_DRDY_L_UF	:::500			250	10 MIL SPACING			5
	CPU_DRDY_L	:::1500:2500	5		250	10 MIL SPACING			5 9
	CPU_GBL_L	:::1500:2500	5		250				5 9
	CPU_HIT_L	:::1500:2800	5		250	10 MIL SPACING			5 9
	CPU_QACK_L	:::1500:2500	5		250	10 MIL SPACING			5 9
	CPU_QREQ_L	:::1500:2600	5		250	10 MIL SPACING			5 9
	CPU_TA_L	:::1500:2500	5		250	10 MIL SPACING			5 9
	CPU_TBST_L	:::1500:2600	5		250	10 MIL SPACING			5 9
	CPU_TEA_L	:::1500:3000	5		250				5 9
	CPU_TS_L	:::1500:2500	5		250	10 MIL SPACING			5 9
	CPU_TSIZ<0..2>	:::1500:3500	5		250				5 9
	CPU_TT<0..4>	:::1500:3400	5		250				5 9
	CPU_WT_L	:::1500:3100	5		250				5 9
L3 CACHE	L3_DATA<31..0>	:::750:1250	4		200				6 8
	L3_DATA<63..32>	:::750:1250	4		200				6 8
	L3_CNTL<1..0>	:::1200:1800	4		200				6 8
	L3_ADDR<17..0>	:::1200:1800	4		200				6 8
GROUP 0	MEM_DATA<7..0>	:::1600	4		200			167 MHZ	10 11
	RAM_DATA_A<7..0>	:::1550	4	RAM_GROUP0_A:::450	200			167 MHZ	11 12
	RAM_DATA_B<7..0>	:::2150	4	RAM_GROUP0_B:::600	200			167 MHZ	11 12
	MEM_DQS<0>	:::1600	4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200			167 MHZ	10 11
	RAM_DQS_A<0>	:::1550	4	RAM_GROUP0_A:::450	200			167 MHZ	11 12
	RAM_DQS_B<0>	:::2150	4	RAM_GROUP0_B:::600	200			167 MHZ	11 12
	MEM_DQM<0>	:::1600	4		200			167 MHZ	10 11
	RAM_DQM_A<0>	:::1550	4	RAM_GROUP0_A:::450	200			167 MHZ	11 12
	RAM_DQM_B<0>	:::2150	4	RAM_GROUP0_B:::600	200			167 MHZ	11 12
GROUP 1	MEM_DATA<15..8>	:::1500	4		200			167 MHZ	10 11
	RAM_DATA_A<15..8>	:::1550	4	RAM_GROUP1_A:::700	200			167 MHZ	11 12
	RAM_DATA_B<15..8>	:::2100	4	RAM_GROUP1_B:::700	200			167 MHZ	11 12
	MEM_DQS<1>	:::1500	4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200			167 MHZ	10 11
	RAM_DQS_A<1>	:::1550	4	RAM_GROUP1_A:::700	200			167 MHZ	11 12
	RAM_DQS_B<1>	:::2100	4	RAM_GROUP1_B:::700	200			167 MHZ	11 12
	MEM_DQM<1>	:::1500	4		200			167 MHZ	10 11
	RAM_DQM_A<1>	:::1550	4	RAM_GROUP1_A:::700	200			167 MHZ	11 12
	RAM_DQM_B<1>	:::2100	4	RAM_GROUP1_B:::700	200			167 MHZ	11 12
GROUP 2/3	MEM_DATA<31..16>	:::1650	4		200			167 MHZ	10 11
	RAM_DATA_A<31..16>	:::1700	4	RAM_GROUP23_A:::850	200			167 MHZ	11 12
	RAM_DATA_B<31..16>	:::2200	4	RAM_GROUP23_B:::850	200			167 MHZ	11 12
	MEM_DQS<3..2>	:::1650	4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200			167 MHZ	10 11
	RAM_DQS_A<3..2>	:::1700	4	RAM_GROUP23_A:::850	200			167 MHZ	11 12
	RAM_DQS_B<3..2>	:::2200	4	RAM_GROUP23_B:::850	200			167 MHZ	11 12
	MEM_DQM<3..2>	:::1650	4		200			167 MHZ	10 11
	RAM_DQM_A<3..2>	:::1700	4	RAM_GROUP23_A:::850	200			167 MHZ	11 12
	RAM_DQM_B<3..2>	:::2200	4	RAM_GROUP23_B:::850	200			167 MHZ	11 12
GROUP 4/5	MEM_DATA<47..32>	:::1500	4		200			167 MHZ	10 11
	RAM_DATA_A<47..32>	:::1850	4	RAM_GROUP45_A:::900	200			167 MHZ	11 12
	RAM_DATA_B<47..32>	:::2350	4	RAM_GROUP45_B:::950	200			167 MHZ	11 12
	MEM_DQS<5..4>	:::1500	4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200			167 MHZ	10 11
	RAM_DQS_A<5..4>	:::1850	4	RAM_GROUP45_A:::900	200			167 MHZ	11 12
	RAM_DQS_B<5..4>	:::2350	4	RAM_GROUP45_B:::950	200			167 MHZ	11 12
	MEM_DQM<5..4>	:::1500	4		200			167 MHZ	10 11
	RAM_DQM_A<5..4>	:::1850	4	RAM_GROUP45_A:::900	200			167 MHZ	11 12
	RAM_DQM_B<5..4>	:::2350	4	RAM_GROUP45_B:::950	200			167 MHZ	11 12
GROUP 6	MEM_DATA<55..48>	:::1650	4		200			167 MHZ	10 11
	RAM_DATA_A<55..48>	:::1800	4	RAM_GROUP6_A:::800	200			167 MHZ	11 12
	RAM_DATA_B<55..48>	:::2400	4	RAM_GROUP6_B:::800	200			167 MHZ	11 12
	MEM_DQS<6>	:::1650	4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200			167 MHZ	10 11
	RAM_DQS_A<6>	:::1800	4	RAM_GROUP6_A:::800	200			167 MHZ	11 12
	RAM_DQS_B<6>	:::2400	4	RAM_GROUP6_B:::800	200			167 MHZ	11 12
	MEM_DQM<6>	:::1650	4		200			167 MHZ	10 11
	RAM_DQM_A<6>	:::1800	4	RAM_GROUP6_A:::800	200			167 MHZ	11 12
	RAM_DQM_B<6>	:::2400	4	RAM_GROUP6_B:::800	200			167 MHZ	11 12
GROUP 7	MEM_DATA<63..56>	:::1600	4		200			167 MHZ	10 11
	RAM_DATA_A<63..56>	:::1600	4	RAM_GROUP7_A:::500	200			167 MHZ	11 12
	RAM_DATA_B<63..56>	:::2200	4	RAM_GROUP7_B:::500	200			167 MHZ	11 12
	MEM_DQS<7>	:::1600	4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200			167 MHZ	10 11
	RAM_DQS_A<7>	:::1600	4	RAM_GROUP7_A:::500	200			167 MHZ	11 12
	RAM_DQS_B<7>	:::2200	4	RAM_GROUP7_B:::500	200			167 MHZ	11 12
	MEM_DQM<7>	:::1600	4		200			167 MHZ	10 11
	RAM_DQM_A<7>	:::1600	4	RAM_GROUP7_A:::500	200			167 MHZ	11 12
	RAM_DQM_B<7>	:::2200	4	RAM_GROUP7_B:::500	200			167 MHZ	11 12
ADDR	MEM_ADDR<12..0>	:::500	4					83 MHZ	10
	RAM_ADDR<12..0>	::2000:3000	6		200				10 12
	MEM_BA<1..0>	:::500	4						10
	RAM_BA<1..0>	::2000:3300	6		200				10 12
CONTROL	MEM_CS_L<3..0>	:::500	4						10
	RAM_CS_L<3..0>	::1800:2500	6		200				10 12
	MEM_CKE<3..0>	:::500	4						10
	RAM_CKE<3..0>	::1800:2500	6		200				10 12
	MEM_RAS_L	:::500	4						10
	RAM_RAS_L	::2000:4100	6		200				10 12
	MEM_CAS_L	:::500	4						10
	RAM_CAS_L	::2000:4100	6		200				10 12
	MEM_WE_L	:::500	4						10
	RAM_WE_L	::2000:3100	6		200				10 12
	MEM_MUXSEL_H<1..0>	:::500	3						10 11
	MEM_MUXSEL_L<1..0>	:::500	3						10 11
	RAM_MUXSEL_H	::1800:2600	5						11
	RAM_MUXSEL_L	::1800:2600	5						11

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME	DELAY_RULE	MATCHED_DELAY	MAX VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM	
INTREPID CLOCKS	SYSCLK_CPU_UF	:::150					10 MIL SPACING	167 MHZ	9
	SYSCLK_CPU	::2650:2750		3	250	200	10 MIL SPACING	167 MHZ	5 9
	INT_CPUFB_OUT	:::150		3	250		10 MIL SPACING	167 MHZ	9
	INT_CPUFB_OUT_SHORT	::700:850		3	250		10 MIL SPACING	167 MHZ	9
	INT_CPUFB_OUT_NORM	::500:600		3	250		10 MIL SPACING	167 MHZ	9
	INT_CPUFB_IN_NORM	::500:600		3	250		10 MIL SPACING	167 MHZ	9
	INT_CPUFB_LONG	::1050:1150		3	250		10 MIL SPACING	167 MHZ	9
	INT_CPUFB_IN	::700:800		3	250	200	10 MIL SPACING	167 MHZ	9
	SYSCLK_DDRCLK_A0_UF	:::475:575		3	250	200	10 MIL SPACING	167 MHZ	10
	SYSCLK_DDRCLK_A0_L_UF	:::475:575		3	250	200	10 MIL SPACING	167 MHZ	10
	SYSCLK_DDRCLK_A1_UF	:::300:400		3	250	200	10 MIL SPACING	167 MHZ	10
	SYSCLK_DDRCLK_A1_L_UF	:::300:400		3	250	200	10 MIL SPACING	167 MHZ	10
	SYSCLK_DDRCLK_B0_UF	:::430:530		3	250	200	10 MIL SPACING	167 MHZ	10
	SYSCLK_DDRCLK_B0_L_UF	:::430:530		3	250	200	10 MIL SPACING	167 MHZ	10
	SYSCLK_DDRCLK_B1_UF	:::400:510		3	250	200	10 MIL SPACING	167 MHZ	10
	SYSCLK_DDRCLK_B1_L_UF	:::400:510		3	250	200	10 MIL SPACING	167 MHZ	10
	SYSCLK_DDRCLK_A0	::1850:1950 DDRCLK_A0	SYSCLK_DDRCLK_A0:::25	3	250	200	10 MIL SPACING	167 MHZ	10 12
	SYSCLK_DDRCLK_A0_L	::1850:1950 DDRCLK_A0	SYSCLK_DDRCLK_A0:::25	3	250	200	10 MIL SPACING	167 MHZ	10 12
	SYSCLK_DDRCLK_A1	::1925:2025 DDRCLK_A1	SYSCLK_DDRCLK_A1:::25	3	250	200	10 MIL SPACING	167 MHZ	10 12
	SYSCLK_DDRCLK_A1_L	::1925:2025 DDRCLK_A1	SYSCLK_DDRCLK_A1:::25	3	250	200	10 MIL SPACING	167 MHZ	10 12
	SYSCLK_DDRCLK_B0	::2375:2475 DDRCLK_B0	SYSCLK_DDRCLK_B0:::25	3	250	200	10 MIL SPACING	167 MHZ	10 12
	SYSCLK_DDRCLK_B0_L	::2375:2475 DDRCLK_B0	SYSCLK_DDRCLK_B0:::25	3	250	200	10 MIL SPACING	167 MHZ	10 12
	SYSCLK_DDRCLK_B1	::2450:2550 DDRCLK_B1	SYSCLK_DDRCLK_B1:::25	3	250	200	10 MIL SPACING	167 MHZ	10 12
	SYSCLK_DDRCLK_B1_L	::2450:2550 DDRCLK_B1	SYSCLK_DDRCLK_B1:::25	3	250	200	10 MIL SPACING	167 MHZ	10 12
	INT_REF_CLK_OUT	::1250:1400		3	250	200	10 MIL SPACING	49.92 MHZ	15
	INT_REF_CLK_IN	::1900:2000		4	250	200	10 MIL SPACING	167 MHZ	15
	CLK66M_GPU_AGP_UF	:::150				200	10 MIL SPACING	66 MHZ	13
	CLK66M_GPU_AGP	::1400:1500		4	400	200	10 MIL SPACING	66 MHZ	13 19
	INT_AGP_FB_OUT	:::150				200	10 MIL SPACING	66 MHZ	13
	INT_AGP_FB_IN	::1400:1500		4	500	200	10 MIL SPACING	66 MHZ	13
	CLK33M_CBUS_UF	:::250				200	10 MIL SPACING	33 MHZ	13
	CLK33M_CBUS	::5000:6000	SHOULD BE AT MOST 4 VIAS FOR CLK	6	500	200	10 MIL SPACING	33 MHZ	13 18
	CLK33M_AIRPORT_UF	:::250				200	10 MIL SPACING	33 MHZ	13
	CLK33M_AIRPORT	::11000:12000	SHOULD BE AT MOST 4 VIAS FOR CLK	6	500	200	10 MIL SPACING	33 MHZ	13 24 39
	CLK33M_USB2_UF	:::250				200	10 MIL SPACING	33 MHZ	13
	CLK33M_USB2	::4000:6000	SHOULD BE AT MOST 4 VIAS FOR CLK	6	500	200	10 MIL SPACING	33 MHZ	13 26
	INT_PCI_FB_OUT	:::300				200	10 MIL SPACING	33 MHZ	13
	INT_PCI_FB_IN	::6500:7500		3	500	200	10 MIL SPACING	33 MHZ	13
L3 CACHE	L3_CLK<0>	::900:1100		3	250	200	10 MIL SPACING	250 MHZ	6 8
	L3_ECHO_CLK<0..1>	::900:1100		3	250	200	10 MIL SPACING	250 MHZ	6 8
	L3_CLK<1>	::900:1100		3	250	200	10 MIL SPACING	250 MHZ	6 8
	L3_ECHO_CLK<2..3>	::900:1100		3	250	200	10 MIL SPACING	250 MHZ	6 8
MAP17	GPU_CLK27M_OUT	:::400		3		200	10 MIL SPACING		21
	GPU_CLK27M_UF	:::250		3		200	10 MIL SPACING		21
	GPU_SSCLK_UF	:::200				200	10 MIL SPACING		21
	GPU_SSCLK_IN	:::920		3	500	200	10 MIL SPACING		21
	GPU_FBCLK0	:::250		3		200	10 MIL SPACING		19
	GPU_FBCLK0_L	:::250		3		200	10 MIL SPACING		19
	GPU_FBCLK1	:::250		3		200	10 MIL SPACING		19
	GPU_FBCLK1_L	:::250		3		200	10 MIL SPACING		19
	GPU_DVO_CLKP	::600:1300		3	250	200	10 MIL SPACING		21
CRYSTALS	CLK27M_GPU_XOUT	:::150					10 MIL SPACING		21
	CLK27M_XTAL_IN	:::250					10 MIL SPACING		21
	CLK27M_GPU_XIN	::300:400					10 MIL SPACING		21
	CLK18M_INT_XIN	::1400:1500					10 MIL SPACING		15
	CLK18M_INT_XOUT	::1300:1400					10 MIL SPACING		15
	CLK18M_XTAL_IN	:::300					10 MIL SPACING		15
	CLK18M_INT_EXT	:::400					10 MIL SPACING		15
	CLK25M_ENET_XIN	:::650					10 MIL SPACING		27
	CLK25M_ENET_XOUT	:::400					10 MIL SPACING		27
	NEC_XT1	::600:700					10 MIL SPACING		26
	NEC_XT2	::300:400	THERE'S ANOTHER 280MIL LEG				10 MIL SPACING		26
SOUND	SND_SCLK			5	500	200	10 MIL SPACING		15 25 39
	SND_CLKOUT			5	500	200	10 MIL SPACING		15 25 39
ETHERNET MARVELL	CLKENET_PHY_RX	:::300				200		125 MHZ	27
	CLKENET_LINK_RX	::8000:9000		3	500	200	10 MIL SPACING	125 MHZ	14 27
	CLKENET_PHY_GBE_REF	:::300				200		125 MHZ	27
	CLKENET_LINK_GBE_REF	::8000:9000		3	500	200	10 MIL SPACING	125 MHZ	14 27
	CLKENET_PHY_TX	:::300				200		25 MHZ	27
	CLKENET_LINK_TX	::8000:9000		4	500	200	10 MIL SPACING	25 MHZ	14 27
	CLKENET_LINK_GTX	:::300				200		125 MHZ	14
	CLKENET_PHY_GTX	::8000:9000		3	500	200	10 MIL SPACING	125 MHZ	14 27
FIREWIRE	CLKFW_PHY_PCLK	:::300				200		49.152 MHZ	28
	CLKFW_LINK_PCLK	::7500:8000		3	500	200	10 MIL SPACING	49.152 MHZ	14 28
	CLKFW_PHY_LCLK	::7500:8000		3	500	200	10 MIL SPACING	49.152 MHZ	14 28
	CLKFW_LINK_LCLK	:::300				200		49.152 MHZ	14
	FW_XI	:::520				200	10 MIL SPACING	98.034 MHZ	28
	FW_OSC	:::300				200	10 MIL SPACING	98.034 MHZ	28

SIGNAL CONSTRAINTS - PAGE 1

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6469	E

SCALE: NONE

SHT 36 OF 44

Digital Signals (cont'd)

GROUP	SIG_NAME	DELAY_RULE	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
AGP	AGP_AD<15..0>	::1350:1650	5	100				66 MHZ	13 19
AGP BYTES 0-1	AGP_CBE<1..0>	::1350:1650	5	100				66 MHZ	13 19
	AGP_AD_STB<0>	::1500:1600	4	100	250	8 MIL SPACING		133 MHZ	13 19
	AGP_AD_STB_L<0>	::1500:1600	4	100	250	8 MIL SPACING		133 MHZ	13 19
AGP BYTES 2-3	AGP_AD<31..16>	::1350:1650	5	100				66 MHZ	13 19
	AGP_CBE<3..2>	::1350:1680	5	100				66 MHZ	13 19
	AGP_AD_STB<1>	::1500:1600	4	100	250	8 MIL SPACING		133 MHZ	13 19
	AGP_AD_STB_L<1>	::1500:1600	4	100	250	8 MIL SPACING		133 MHZ	13 19
AGP SIDEBAND	AGP_SBA<7..0>	::1100:1700	5	100				66 MHZ	13 19
	AGP_SB_STB	::1500:1700	4	100	350	8 MIL SPACING		66 MHZ	13 19
	AGP_SB_STB_L	::1500:1700	4	100	350	8 MIL SPACING		66 MHZ	13 19
AGP CONTROL	AGP_FRAME_L	::1200:1900	6	250				66 MHZ	13 19
	AGP_IRDY_L	::1200:1900	6	250				66 MHZ	13 19
	AGP_TRDY_L	::1200:1900	6	250				66 MHZ	13 19
	AGP_DEVSEL_L	::1200:1900	6	250				66 MHZ	13 19
	AGP_STOP_L	::1200:1900	6	250				66 MHZ	13 19
	AGP_PAR	::1200:1900	6	250				66 MHZ	13 19
	AGP_REQ_L	::1200:1900	6	250				66 MHZ	13 19
	AGP_GNT_L	::1200:1900	6	250				66 MHZ	13 19
	AGP_RBF_L	::1200:1900	6	250				66 MHZ	13 19
DVO	GPU_DVOD<0..11>	::600:1300	5	250					21
	GPU_DVO_HSYNC	::600:1300	5	250					21
	GPU_DVO_VSYNC	::600:1300	5	250					21
PCI	PCI_AD<31..0>	::8000:13500				MIN_DAISY_CHAIN		33 MHZ	10 13 18 24 26 39
	PCI_CBE<3..0>	::8000:13500				MIN_DAISY_CHAIN		33 MHZ	13 18 24 26 39
	PCI_FRAME_L	::8000:13500				MIN_DAISY_CHAIN		33 MHZ	13 18 24 26 39
	PCI_IRDY_L	::8000:13500				MIN_DAISY_CHAIN		33 MHZ	13 18 24 26 39
	PCI_TRDY_L	::8000:13500				MIN_DAISY_CHAIN		33 MHZ	13 18 24 26 39
	PCI_DEVSEL_L	::8000:13500				MIN_DAISY_CHAIN		33 MHZ	13 18 24 26 39
	PCI_STOP_L	::8000:13500				MIN_DAISY_CHAIN		33 MHZ	13 18 24 26 39
	PCI_PAR	::8000:13500				MIN_DAISY_CHAIN		33 MHZ	13 18 24 26 39
ULTRA ATA-100	UIDE_DATA<15..8>	:::710		NEED TO MATCH DELAY TO 250	200			100 MHZ	14 24
	UIDE_DATA<7>	U44.V1:RP9.4::600			200			100 MHZ	14 24
	UIDE_DATA<6..0>	:::600			200			100 MHZ	14 24
	UIDE_ADDR<2..0>	:::650			200			100 MHZ	14 24
	UIDE_RST_L	:::400			200			100 MHZ	14 24
	UIDE_DIOW_L	:::400			200			100 MHZ	14 24
	UIDE_DIOR_L	:::600		10 MIL SPACING	200			100 MHZ	14 24
	UIDE_DMACK_L	:::400			200			100 MHZ	14 24
	UIDE_CS0_L	:::500			200			100 MHZ	14 24
	UIDE_CS1_L	:::500			200			100 MHZ	14 24
	UIDE_DMARQ	:::400			200			100 MHZ	14
	UIDE_IOCHRDY	:::600		10 MIL SPACING	200			100 MHZ	14 24
	UIDE_INTRQ	:::400			200			100 MHZ	14
	HD_DATA<15..0>	::8000:9500	5	TOTAL UIDE+HD SKEW <500MIL	200	MATCHED_DELAY=HD_DATA:::1000		100 MHZ	24
	HD_ADDR<2..0>	::8000:9500	5		200			100 MHZ	24
	HD_RESET_L	::5000:7000	5		200			100 MHZ	24
	HD_DIOW_L	::6000:8000	5		200			100 MHZ	24
	HD_DIOR_L	::8000:9500	5	10 MIL SPACING	200	MATCHED_DELAY=HD_DATA:::1000		100 MHZ	24
	HD_DMACK_L	::7500:9000	5		200			100 MHZ	24
	HD_CS0_L	::6000:9000	5		200			100 MHZ	24
	HD_CS1_L	::6000:9000	5		200			100 MHZ	24
	HD_DMARQ	::7500:9000	5		200			100 MHZ	14 24
	HD_IOCHRDY	::8000:9500	5	10 MIL SPACING	200	MATCHED_DELAY=HD_DATA:::1000		100 MHZ	24
	HD_INTRQ	::6000:8000	5					100 MHZ	14 24
EIDE INTREPID	EIDE_DATA<15..0>	:::855						33 MHZ	14 24
	EIDE_ADDR<2..0>	:::900						33 MHZ	14 24
	EIDE_CS0_L	:::850						33 MHZ	14 24
	EIDE_CS1_L	:::850						33 MHZ	14 24
	EIDE_RD_L	:::500						33 MHZ	14 24
	EIDE_WR_L	:::500						33 MHZ	14 24
	EIDE_IOCHRDY	:::500						33 MHZ	14 24
	EIDE_INT	:::500						33 MHZ	14 24
	EIDE_RST_L	:::500						33 MHZ	14 24
	EIDE_DMACK_L	:::500						33 MHZ	14 24
	EIDE_DMARQ	:::500						33 MHZ	14 24
OPTICAL	EIDE_OPTICAL_DATA<15..0>	::4500:6500						33 MHZ	24 39
	EIDE_OPTICAL_ADDR<2..0>	::4500:6500						33 MHZ	24 39
	EIDE_OPTICAL_CS0_L	::5000:7000						33 MHZ	24 39
	EIDE_OPTICAL_CS1_L	::5000:7000						33 MHZ	24 39
	EIDE_OPTICAL_RD_L	::5000:7000						33 MHZ	24 39
	EIDE_OPTICAL_WR_L	::5000:7000						33 MHZ	24 39
	EIDE_OPTICAL_IOCHRDY	::5000:7000						33 MHZ	24 39
	EIDE_OPTICAL_INT	::5500:7500						33 MHZ	24 39
	EIDE_OPTICAL_RST_L	::5000:7000						33 MHZ	24 39
	EIDE_OPTICAL_DMAACK_L	::5000:7000						33 MHZ	24 39
	EIDE_OPTICAL_DMA_RQ	::5000:7000						33 MHZ	24 39
ETHERNET MII	ENET_LINK_RXD<7..0>	::8000:9000	5						14 27
	ENET_RX_DV	::8000:9000							14 27
	ENET_RX_ER	::8000:9000							14 27
	ENET_PHY_TXD<7..0>	::8300:9300	5						14 27
	ENET_LINK_TXD<7..0>	:::600							14
	ENET_PHY_TX_ER	::8000:9200	5						14 27
	ENET_LINK_TX_ER	:::400							14
	ENET_PHY_TX_EN	::8000:9200	5						14 27
	ENET_LINK_TX_EN	:::400							14
	ENET_MDIO	::8000:9000							14 27
	ENET_MDC	::8000:9000							14 27
	ENET_COL	::7500:9000							14 27
	ENET_CRS	::7500:9000							14 27
FIREWIRE MII	FW_LINK_DATA<7..0>	::2700:3500	5						14 28
	FW_PHY_DATA<7..0>	::4700:5500	5						28
	FW_LINK_CNTL<1..0>	::9000:10000							14 28
	FW_PHY_CNTL<1..0>	:::300							28
	FW_LINK_LREQ	:::300							14
	FW_PHY_LREQ	::8500:9500							14 28
	FW_PINT	::8500:9500							14 28

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR	MATCHED_DELAY	MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS	
ETHERNET	MDI_M<0>	ENET_MDI0	ENET_MDI0:U49.31:T1.11:100				27
	MDI_P<0>	ENET_MDI0	ENET_MDI0:U49.29:T1.12:100				27
	MDI_M<1>	ENET_MDI1	ENET_MDI1:U49.34:T1.8:100	SPACING DELETED BECAUSE			27
	MDI_P<1>	ENET_MDI1	ENET_MDI1:U49.33:T1.9:100	OF PHYSICAL CONSTRAINTS			27
	MDI_M<2>	ENET_MDI2	ENET_MDI2:U49.41:T1.5:100	AROUND MARVELL PHY			27
	MDI_P<2>	ENET_MDI2	ENET_MDI2:U49.39:T1.6:100				27
	MDI_M<3>	ENET_MDI3	ENET_MDI3:U49.43:T1.2:100				27
	MDI_P<3>	ENET_MDI3	ENET_MDI3:U49.42:T1.3:100				27
	RJ45_DN<0>	RJ45_DP0	RJ45_DP0:T1.14:J18.2:100		10 MIL SPACING		27 39
	RJ45_DP<0>	RJ45_DP0	RJ45_DP0:T1.13:J18.1:100		10 MIL SPACING		27 39
	RJ45_DN<1>	RJ45_DP1	RJ45_DP1:T1.17:J18.6:100		10 MIL SPACING		27 39
	RJ45_DP<1>	RJ45_DP1	RJ45_DP1:T1.16:J18.3:100		10 MIL SPACING		27 39
	RJ45_DN<2>	RJ45_DP2	RJ45_DP2:T1.20:J18.5:100		10 MIL SPACING		27 39
	RJ45_DP<2>	RJ45_DP2	RJ45_DP2:T1.19:J18.4:100		10 MIL SPACING		27 39
	RJ45_DN<3>	RJ45_DP3	RJ45_DP3:T1.23:J18.8:100		10 MIL SPACING		27 39
	RJ45_DP<3>	RJ45_DP3	RJ45_DP3:T1.22:J18.7:100		10 MIL SPACING		27 39
FIREWIRE	FW_TPA0N	FW_TPA0	FW_TPA0:::4%		MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPA0P	FW_TPA0	FW_TPA0:::4%		MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB0N	FW_TPB0	FW_TPB0:::4%		MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB0P	FW_TPB0	FW_TPB0:::4%		MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPI0N	FW_TPI0	FW_TPI0:::4%		MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPI0P	FW_TPI0	FW_TPI0:::4%		MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPO0N	FW_TPO0	FW_TPO0:::4%		MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPO0P	FW_TPO0	FW_TPO0:::4%		MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPA1N	FW_TPA1	FW_TPA1:::4%	500	MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPA1P	FW_TPA1	FW_TPA1:::4%	500	MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB1N	FW_TPB1	FW_TPB1:::4%	500	MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB1P	FW_TPB1	FW_TPB1:::4%	500	MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPI1N	FW_TPI1	FW_TPI1:::4%		MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 39
	FW_TPI1P	FW_TPI1	FW_TPI1:::4%		MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 39
	FW_TPO1N	FW_TPO1	FW_TPO1:::4%		MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 39
	FW_TPO1P	FW_TPO1	FW_TPO1:::4%		MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 39
LVDS LOWER	CLKLVDS_LN	CLKLVDS_L	LVDS:::110	500	10 MIL SPACING	4	20 22 39
	CLKLVDS_LP	CLKLVDS_L	LVDS:::110	500	10 MIL SPACING	4	20 22 39
	LVDS_L0N	LVDS_L0	LVDS:::110		10 MIL SPACING		20 22 39
	LVDS_L0P	LVDS_L0	LVDS:::110		10 MIL SPACING		20 22 39
	LVDS_L1N	LVDS_L1	LVDS:::110		10 MIL SPACING		20 22 39
	LVDS_L1P	LVDS_L1	LVDS:::110		10 MIL SPACING		20 22 39
	LVDS_L2N	LVDS_L2	LVDS:::110		10 MIL SPACING		20 22 39
	LVDS_L2P	LVDS_L2	LVDS:::110		10 MIL SPACING		20 22 39
UPPER	CLKLVDS_UN	CLKLVDS_U	LVDS:::110	500	10 MIL SPACING	4	20 22 39
	CLKLVDS_UP	CLKLVDS_U	LVDS:::110	500	10 MIL SPACING	4	20 22 39
	LVDS_U0N	LVDS_U0	LVDS:::110		10 MIL SPACING		20 22 39
	LVDS_U0P	LVDS_U0	LVDS:::110		10 MIL SPACING		20 22 39
	LVDS_U1N	LVDS_U1	LVDS:::110		10 MIL SPACING		20 22 39
	LVDS_U1P	LVDS_U1	LVDS:::110		10 MIL SPACING		20 22 39
	LVDS_U2N	LVDS_U2	LVDS:::110		10 MIL SPACING		20 22 39
	LVDS_U2P	LVDS_U2	LVDS:::110		10 MIL SPACING		20 22 39
TMDS	TMDS_CONN_CLKN	CLKCONN_TMDS	TMDS_CONN:::50	500	10 MIL SPACING	4	22 39
	TMDS_CONN_CLKP	CLKCONN_TMDS	TMDS_CONN:::50	500	10 MIL SPACING	4	22 39
	TMDS_CLKN	CLKTMDS	TMDS:::50	500	10 MIL SPACING	4	20 21 22
	TMDS_CLKP	CLKTMDS	TMDS:::50	500	10 MIL SPACING	4	20 21 22
	TMDS_DN<0>	TMDS_D0	TMDS:::50		10 MIL SPACING		20 21 22 39
	TMDS_DP<0>	TMDS_D0	TMDS:::50		10 MIL SPACING		20 21 22 39
	TMDS_DN<1>	TMDS_D1	TMDS:::50		10 MIL SPACING		20 21 22 39
	TMDS_DP<1>	TMDS_D1	TMDS:::50		10 MIL SPACING		20 21 22 39
	TMDS_DN<2>	TMDS_D2	TMDS:::50		10 MIL SPACING		20 21 22 39
	TMDS_DP<2>	TMDS_D2	TMDS:::50		10 MIL SPACING		20 21 22 39
USB	NEC_USB_DAM	NEC_USB_DA	NEC_USB_DA:::20	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_DAP	NEC_USB_DA	NEC_USB_DA:::20	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	USB_DEM	USB_DE	USB_DE:::200		5 MIL SPACING		15
	USB_DEP	USB_DE	USB_DE:::200		5 MIL SPACING		15
	NEC_USB_DBM	NEC_USB_DB	NEC_USB_DB:::20	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_DBP	NEC_USB_DB	NEC_USB_DB:::20	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	USB_DFM	USB_DF	USB_DF:::200		5 MIL SPACING		15
	USB_DFP	USB_DF	USB_DF:::200		5 MIL SPACING		15
	BT_USB_DM	BT_USB_D	BT_USB_D:::200		5 MIL SPACING		15 24 39
	BT_USB_DP	BT_USB_D	BT_USB_D:::200		5 MIL SPACING		15 24 39
	NEC_USB_RSDM1	NEC_USB_RSD1	NEC_USB_RSD1:::20	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_RSDP1	NEC_USB_RSD1	NEC_USB_RSD1:::20	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_RSDM2	NEC_USB_RSD2	NEC_USB_RSD2:::20	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_RSDP2	NEC_USB_RSD2	NEC_USB_RSD2:::20	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	MODEM_USB_DM	MODEM_USB_D	MODEM_USB:::200		5 MIL SPACING		15 25 39
	MODEM_USB_DP	MODEM_USB_D	MODEM_USB:::200		5 MIL SPACING		15 25 39
	LEFT_USB_DM	LEFT_USB	LEFT_USB:::20	MIN_LINE_WIDTH=5	10 MIL SPACING		24 26 39
	LEFT_USB_DP	LEFT_USB	LEFT_USB:::20	MIN_LINE_WIDTH=5	10 MIL SPACING		24 26 39
	RIGHT_USB_DM	RIGHT_USB	RIGHT_USB:::20	MIN_LINE_WIDTH=5	10 MIL SPACING		26 32 39
	RIGHT_USB_DP	RIGHT_USB	RIGHT_USB:::20	MIN_LINE_WIDTH=5	10 MIL SPACING		26 32 39
POWER SUPPLIES	1772_CSSN	1772_CSS	1772_CSS:::100				31
	1772_CSSP	1772_CSS	1772_CSS:::100				31
	1772_CSIN	1772_CSI	1772_CSI:::100				31
	1772_CSIP	1772_CSI	1772_CSI:::100				31
	3V_SNSM	3V_SNS	3V_SNS:::100				33
	3V_SNSP	3V_SNS	3V_SNS:::100				33
	5V_SNSM	5V_SNS	5V_SNS:::100				33
	5V_SNSP	5V_SNS	5V_SNS:::100				33
THERMOSTAT	THERM1_DM	THERM1	THERM1:::100				25
	THERM1_DP	THERM1	THERM1:::100				25
	THERM2_DM	THERM2	THERM2:::100				25
	THERM2_DP	THERM2	THERM2:::100				25
	THERM1_M_DM	THERM1_MAIN	THERM1_MAIN:::100				25
	THERM1_M_DP	THERM1_MAIN	THERM1_MAIN:::100				25
	THERM2_M_DM	THERM2_MAIN	THERM2_MAIN:::100				25
	THERM2_M_DP	THERM2_MAIN	THERM2_MAIN:::100				25
	THERM1_A_DM	THERM1_ALT	THERM1_ALT:::100				25
	THERM1_A_DP	THERM1_ALT	THERM1_ALT:::100				25
	THERM2_A_DM	THERM2_ALT	THERM2_ALT:::100				25
	THERM2_A_DP	THERM2_ALT	THERM2_ALT:::100				25

INTERNAL LAYER
ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.57OHM
ZDIFF = 99.80HM

FOR FIREWIRE
ER = 4.3 (DIELECTRIC CONSTANT)
W = 3.4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 53.37OHM
ZDIFF = 107.17OHM

INTERNAL LAYER (USB1.1/USB 2.0)
ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL(USB 1.1)/ 5MIL(USB 2.0) (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 5MIL (USB 1.1) (SEPERATION OF DIFF TRACES)
S = 10MIL (USB 2.0) (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.5OHM (USB 1.1)/ 46.2OHM (USB 2.0)
ZDIFF = 89.3OHM (USB 1.1)/ 89.4OHM (USB 2.0)

SIGNAL CONSTRAINTS - PAGE 2

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6469	E
SCALE: NONE	SHT 37 OF 44	

POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
MAIN/SLEEP	+24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+BATT	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	
	+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+2_5V_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	16
	+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	39
	+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	16 19 35
	+1_5V_SLEEP_VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	35
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31 32
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31 39
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31 39
	1772_DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	1772_LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	31
	1772_LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		31
	1772_DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		31
	1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10		31
PMU	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	+4_85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		30 32
	+4_6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10		32 33
	+4_85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		32
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		32
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		30
MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24 33
	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24
TRACKPAD	+5V_TPAD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=10		23 39
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		23 39
VIDEO	+12_8V_INV	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	22
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
KB LED	KBD_LED1_OUT	VOLTAGE=0V	MIN_LINE_WIDTH=10		23 23 39
	KBD_LED2_OUT	VOLTAGE=0V	MIN_LINE_WIDTH=10		23 23 39
FAN GND	FAN1_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23 25 39
	FAN2_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23 25 39
SOUND	+5V_SOUND_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25
	SND_AGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=15	25

I/O AREA	GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	
	CHGND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND1
INVERTER	CHGND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND2
TRACKPAD	CHGND3	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND3
LVDS	CHGND4	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND4
I/O AREA	CHGND5	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND5
I/O AREA	CHGND6	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND6
	ENET_CTAP_CHGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	27

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 34 39
	CPU_AVDD	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 7 9 16 17 23 34
L3 CACHE	L3_VREF	VOLTAGE=0.75V	MIN_LINE_WIDTH=10		8
	L3_CLK_REF	VOLTAGE=0.75V	MIN_LINE_WIDTH=10		8
	L3_OVDD	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	6 8
DDR RAM	DDR_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		12
INTREPID	+2_5V_INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	10 11 16 17
	+3V_INTREPID_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	15
PLLS	+1_5V_INTREPID_PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	9 13 15
	+1_5V_INTREPID_PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	15
	+1_5V_INTREPID_PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	15
	+1_5V_INTREPID_PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	15
	+1_5V_INTREPID_PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5	15
	+1_5V_INTREPID_PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5	13
	+1_5V_INTREPID_PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	13
	+1_5V_INTREPID_PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	9
	+1_5V_INTREPID_PLL8	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	15
			MIN_NECK_WIDTH REDUCED FOR TESTPOINTS		
REFERENCE	INT_MEM_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		10
	INT_AGP_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		13
	INT_MEM_REF_H	VOLTAGE=0V	MIN_LINE_WIDTH=10		10
	UIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8		14
CARDBUS	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
NVIDIA NV17MAP	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	20 39
	+2_5V_GPU_FB	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	19
	+3V_GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	13 15 19 20 21
	+3V_GPU_DVO	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	21
	+1_5V_AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	13 16 17 19 20
	+3V_DAC1VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+3V_DAC2VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+3V_GPU_AVDD1	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	20
	+3V_GPU_AVDD0	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	20
	+3V_GPU_PLLVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+3V_GPU_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+2_8V_IFP_PLLVDD	VOLTAGE=2.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	20
	GPU_AGP_VREF	VOLTAGE=0.75V	MIN_LINE_WIDTH=10		19
	GPU_FB_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		19
SILICON IMAGE	+3V_SI_PLLVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	21
	+3V_SI_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	21
	+3V_SI_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	21
88E1111	+2_5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+2_5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
	+1_0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
	LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
FW	LM2594_IN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_ESD_ILIM	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+3V_FW_ESD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+FW_FUSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_PWR_OR	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28 29
	+FW_VP0	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_PWR_PORTA	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_VP1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+3V_FW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28 29
	+3V_FW_UF	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	28
	+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	FW_TPO0R	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29 39
USB 2.0	NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
INTREPID SSCG	+3V_CG_PLL_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	15
	+2_5V_CG_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	15

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	1625_VSW	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		32
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		32
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		32
	1V20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	31 32
LTC3707 5V SWITCHER	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	33
	5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
3V SWITCHER	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		33
MAX1715 2.5V SWITCHER	2_5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	35
	2_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	2_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	2_5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	2_5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
1.5V SWITCHER	1_5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8		35
	1_5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	35
	1_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	1_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	1_5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	1_5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
CONTROL	1_5V_ILIM		MIN_LINE_WIDTH=8		35
	2_5V_ILIM		MIN_LINE_WIDTH=8		35
	MAX1715_TON		MIN_LINE_WIDTH=8		35
	MAX1715_SKIP		MIN_LINE_WIDTH=8		35
	MAX1715_REF	VOLTAGE=2.0V	MIN_LINE_WIDTH=8		35
	MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	35
MAX1717	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=200	MIN_NECK_WIDTH=10	34
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	VCORE_ILIM		MIN_LINE_WIDTH=8		34
	VCORE_REF		MIN_LINE_WIDTH=8		34
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8		34
	VCORE_CC		MIN_LINE_WIDTH=8		34
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		34 39
	VCORE_TIME		MIN_LINE_WIDTH=8		34
	VCORE_VGATE		MIN_LINE_WIDTH=8		15 34
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30		34
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8		34
	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		34
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8		34
LTC1778	1778_VIN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1778_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1778_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	20
	1778_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	20
	1778_BST_RC	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	20
	1778_TG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1778_BG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	GPU_VCORE_SW	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	20
	1778_ION		MIN_LINE_WIDTH=8		20
	1778_ITH		MIN_LINE_WIDTH=8		20
	1778_ITH_RC		MIN_LINE_WIDTH=8		20
	1_5V_2_5V_OK		MIN_LINE_WIDTH=8		20 35
	1778_VFB		MIN_LINE_WIDTH=8		20
	1778_FCB		MIN_LINE_WIDTH=8		20
	1778_VRNG		MIN_LINE_WIDTH=8		20
LTC3411	LTC3411_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	LTC3411_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	35
	1_8V_SW	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	35
	1_8V_VFB		MIN_LINE_WIDTH=8		35
	LTC3411_ITH_RC		MIN_LINE_WIDTH=8		35
	LTC3411_ITH		MIN_LINE_WIDTH=8		35
	LTC3411_SYNC		MIN_LINE_WIDTH=8		35
	LTC3411_SHDN		MIN_LINE_WIDTH=8		35
LTC1962 INT PLLS	LTC1962_INT_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	15
	LTC1962_L3_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	6
	LTC1962_L3_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	6
	LTC1962_1V5_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	16
	LTC1962_1V5_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	16

SIGNAL CONSTRAINTS - PAGE 3

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6469	E
SCALE: NONE	SHT 38 OF 44	

FUNCTIONAL TEST POINTS

FUNC_TEST=YES JTAG_ASIC_TMS 14 27
FUNC_TEST=YES JTAG_ASIC_TDI 14
FUNC_TEST=YES JTAG_ASIC_TDO_TP 27
FUNC_TEST=YES JTAG_ASIC_TCK 14 27
FUNC_TEST=YES JTAG_ASIC_TRST_L 14 27
FUNC_TEST=YES CPU_CHKSTP_OUT_L 5
FUNC_TEST=YES CPU_SRESET_L 5
FUNC_TEST=YES CPU_HRESET_L 5 7 23
FUNC_TEST=YES JTAG_CPU_TMS 5 23
FUNC_TEST=YES JTAG_CPU_TDI 5 23
FUNC_TEST=YES JTAG_CPU_TDO_TP 5
FUNC_TEST=YES JTAG_CPU_TCK 5 23
FUNC_TEST=YES JTAG_CPU_TRST_L 5 23
FUNC_TEST=YES JTAG_L3_TMS 8
FUNC_TEST=YES JTAG_L3_TDI_TP 8
FUNC_TEST=YES JTAG_L3_TDO_TP 8
FUNC_TEST=YES JTAG_L3_TCK 8
FUNC_TEST=YES INT_I2C_CLK0 12 14 23
FUNC_TEST=YES INT_I2C_DATA0 12 14 23
FUNC_TEST=YES INT_I2C_CLK1 14 15 25
FUNC_TEST=YES INT_I2C_DATA1 14 15 25
FUNC_TEST=YES CBUS_DET_1_L 18
FUNC_TEST=YES CBUS_DET_2_L 18
FUNC_TEST=TRUE TMDS_DN<0> 20 21 22 37
FUNC_TEST=TRUE TMDS_DP<0> 20 21 22 37
FUNC_TEST=TRUE TMDS_DN<1> 20 21 22 37
FUNC_TEST=TRUE TMDS_DP<1> 20 21 22 37
FUNC_TEST=TRUE TMDS_DN<2> 20 21 22 37
FUNC_TEST=TRUE TMDS_DP<2> 20 21 22 37
FUNC_TEST=YES TMDS_CONN_CLKN 22 37

FUNC_TEST=YES TMDS_CONN_CLKP 22 37
FUNC_TEST=YES VGA_R 22
FUNC_TEST=YES VGA_G 22
FUNC_TEST=YES VGA_B 22
FUNC_TEST=YES VGA_VSYNC 21 22
FUNC_TEST=YES VGA_HSYNC 21 22
FUNC_TEST=YES DVI_DDC_CLK_UF 22
FUNC_TEST=YES DVI_DDC_DATA_UF 22
FUNC_TEST=YES DVI_HPD_UF 22
FUNC_TEST=YES LVDS_L0N 20 22 37
FUNC_TEST=YES LVDS_L0P 20 22 37
FUNC_TEST=YES LVDS_L1N 20 22 37
FUNC_TEST=YES LVDS_L1P 20 22 37
FUNC_TEST=YES LVDS_L2N 20 22 37
FUNC_TEST=YES LVDS_L2P 20 22 37
FUNC_TEST=YES CLKLVDS_LN 20 22 37
FUNC_TEST=YES CLKLVDS_LP 20 22 37
FUNC_TEST=YES LVDS_U0N 20 22 37
FUNC_TEST=YES LVDS_U0P 20 22 37
FUNC_TEST=YES LVDS_U1N 20 22 37
FUNC_TEST=YES LVDS_U1P 20 22 37
FUNC_TEST=YES LVDS_U2N 20 22 37
FUNC_TEST=YES LVDS_U2P 20 22 37
FUNC_TEST=YES CLKLVDS_UN 20 22 37
FUNC_TEST=YES CLKLVDS_UP 20 22 37
FUNC_TEST=YES LVDS_DDC_CLK 20 22
FUNC_TEST=YES LVDS_DDC_DATA 20 22
FUNC_TEST=YES BRIGHT_PWM 22
FUNC_TEST=YES TV_GND1 22 38
FUNC_TEST=YES TV_GND2 22 38

FUNC_TEST=YES TV_C 22
FUNC_TEST=YES TV_Y 22
FUNC_TEST=YES TV_COMP 22
FUNC_TEST=YES SND_TO_AUDIO 15 25
FUNC_TEST=YES SND_SYNC 15 25
FUNC_TEST=YES SND_CLKOUT 15 25 36
FUNC_TEST=YES SND_HP_MUTE_L 15 25
FUNC_TEST=YES SND_AMP_MUTE_L 15 25
FUNC_TEST=YES INT_AUDIO_TO_SND 15 25
FUNC_TEST=YES SND_SCLK 15 25 36
FUNC_TEST=YES SND_HW_RESET_L 15 25
FUNC_TEST=YES SND_HP_SENSE_L 15 25
FUNC_TEST=YES SND_LIN_SENSE_L 15 25
FUNC_TEST=YES INT_I2C_DATA2 15 25
FUNC_TEST=YES INT_I2C_CLK2 15 25
FUNC_TEST=YES USB_D1M 15 26
FUNC_TEST=YES USB_D1P 15 26

NO LONGER NEED BY TEST GROUP

FUNC_TEST=YES USB_D2M 15 26
FUNC_TEST=YES USB_D2P 15 26
FUNC_TEST=YES BT_USB_DM 15 24 37
FUNC_TEST=YES BT_USB_DP 15 24 37
FUNC_TEST=YES MODEM_USB_DM 15 25 37
FUNC_TEST=YES MODEM_USB_DP 15 25 37
FUNC_TEST=TRUE PCI_AD<0> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<1> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<2> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<3> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<4> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<5> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<6> 10 13 18 24 26 37

FUNC_TEST=TRUE PCI_AD<7> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<8> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<9> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<10> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<11> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<12> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<13> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<14> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<15> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<16> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<17> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<18> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<19> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<20> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<21> 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<22> 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<23> 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<24> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<25> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<26> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<27> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<28> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<29> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<30> 10 13 18 24 26 37
FUNC_TEST=TRUE PCI_AD<31> 10 13 18 24 26 37
FUNC_TEST=YES PCI_FRAME_L 13 18 24 26 37
FUNC_TEST=YES PCI_TRDY_L 13 18 24 26 37
FUNC_TEST=YES PCI_IRDY_L 13 18 24 26 37
FUNC_TEST=YES PCI_DEVSEL_L 13 18 24 26 37
FUNC_TEST=YES PCI_STOP_L 13 18 24 26 37

FUNC_TEST=YES PCI_PAR 13 18 24 26 37
FUNC_TEST=TRUE PCI_CBE<0> 13 18 24 26 37
FUNC_TEST=TRUE PCI_CBE<1> 13 18 24 26 37
FUNC_TEST=TRUE PCI_CBE<2> 13 18 24 26 37
FUNC_TEST=TRUE PCI_CBE<3> 13 18 24 26 37
FUNC_TEST=YES AIRPORT_PCI_REQ_L 13 24
FUNC_TEST=YES AIRPORT_PCI_GNT_L 13 24
FUNC_TEST=YES AIRPORT_PCI_INT_L 15 24
FUNC_TEST=TRUE EIDE_OPTICAL_DATA<0> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_DATA<1> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_DATA<2> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_DATA<3> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_DATA<4> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_DATA<5> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_DATA<6> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_DATA<7> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_DATA<8> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_DATA<9> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_DATA<10> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_DATA<11> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_DATA<12> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_DATA<13> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_DATA<14> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_DATA<15> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DMA_RQ 24 36 24 37
FUNC_TEST=YES EIDE_OPTICAL_RD_L 24 36 24 37
FUNC_TEST=YES EIDE_OPTICAL_DMAACK_L 24 36 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_ADDR<0> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_ADDR<1> 24 37
FUNC_TEST=TRUE EIDE_OPTICAL_ADDR<2> 24 37

FUNC_TEST=YES EIDE_OPTICAL_CS0_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_CS1_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_RST_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_WR_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_IOCHRDY 24 37
FUNC_TEST=YES EIDE_OPTICAL_INT 24 37
FUNC_TEST=YES TPAD_F_TXD 23
FUNC_TEST=YES TPAD_F_RXD 23
FUNC_TEST=YES LID_CLOSED_L 23
FUNC_TEST=YES COMM_RESET_L 15 25
FUNC_TEST=YES COMM_SHUTDOWN 15 25
FUNC_TEST=YES COMM_RING_DET_L 15 25 30
FUNC_TEST=YES KBD_ID 23 30
FUNC_TEST=YES +5V_TPAD_SLEEP 23 38
FUNC_TEST=YES +3V_HALL_EFFECT 23 38
FUNC_TEST=YES KBD_CAPSLOCK_LED 23
FUNC_TEST=YES KBD_FUNCTION_L 23 30
FUNC_TEST=YES KBD_CONTROL_L 23 30
FUNC_TEST=YES KBD_COMMAND_L 23 30
FUNC_TEST=YES KBD_OPTION_L 23 30
FUNC_TEST=YES KBD_SHIFT_L 23 30
FUNC_TEST=TRUE KBD_X<0> 23 30
FUNC_TEST=TRUE KBD_X<1> 23 30
FUNC_TEST=TRUE KBD_X<2> 23 30
FUNC_TEST=TRUE KBD_X<3> 23 30
FUNC_TEST=TRUE KBD_X<4> 23 30
FUNC_TEST=TRUE KBD_X<5> 23 30
FUNC_TEST=TRUE KBD_X<6> 23 30
FUNC_TEST=TRUE KBD_X<7> 23 30
FUNC_TEST=TRUE KBD_X<8> 23 30

FUNC_TEST=TRUE KBD_X<9> 23 30
FUNC_TEST=TRUE KBD_Y<0> 23 30
FUNC_TEST=TRUE KBD_Y<1> 23 30
FUNC_TEST=TRUE KBD_Y<2> 23 30
FUNC_TEST=TRUE KBD_Y<3> 23 30
FUNC_TEST=TRUE KBD_Y<4> 23 30
FUNC_TEST=TRUE KBD_Y<5> 23 30
FUNC_TEST=TRUE KBD_Y<6> 23 30
FUNC_TEST=TRUE KBD_Y<7> 23 30
FUNC_TEST=YES KBD_NUMLOCK_LED 23
FUNC_TEST=YES +BATT_POS 31 38
FUNC_TEST=YES BATT_CLK 31
FUNC_TEST=YES BATT_DATA 31
FUNC_TEST=YES BATT_NEG 31 38
FUNC_TEST=YES PMU_BATT_DET_L 30 31
FUNC_TEST=YES FAN1_GND 25 38
FUNC_TEST=YES FAN1_TACH 25
FUNC_TEST=YES FAN2_GND 25 38
FUNC_TEST=YES FAN2_TACH 25
FUNC_TEST=TRUE RJ45_DP<0> 27 37
FUNC_TEST=TRUE RJ45_DN<0> 27 37
FUNC_TEST=TRUE RJ45_DP<1> 27 37
FUNC_TEST=TRUE RJ45_DN<1> 27 37
FUNC_TEST=TRUE RJ45_DP<2> 27 37
FUNC_TEST=TRUE RJ45_DN<2> 27 37
FUNC_TEST=TRUE RJ45_DP<3> 27 37
FUNC_TEST=TRUE RJ45_DN<3> 27 37

FUNC_TEST=YES FW_TPO0R 29 38

FUNC_TEST=YES FW_TPO1P 29 37
FUNC_TEST=YES FW_TPO1N 29 37
FUNC_TEST=YES FW_TPI1P 29 37
FUNC_TEST=YES FW_TPI1N 29 37
FUNC_TEST=YES CHARGE_LED_L 30 31
FUNC_TEST=YES ADAPTER_DET 30 31
FUNC_TEST=YES SUTRO_ALS_GAIN_SW 23 24
FUNC_TEST=YES SUTRO_ALS_OUT 23 24
FUNC_TEST=YES KBD_LED1_OUT 23 38
FUNC_TEST=YES KBD_LED2_OUT 23 38
FUNC_TEST=YES COMM_TXD_L 15 25
FUNC_TEST=YES COMM_TRXC 15 25
FUNC_TEST=YES COMM_GPIO_L 15 25
FUNC_TEST=YES COMM_DTR_L 15 25
FUNC_TEST=YES COMM_RTS_L 15 25
FUNC_TEST=YES COMM_RXD 15 25
FUNC_TEST=YES PMU_KB_RESET_L 30
FUNC_TEST=YES PWR_BUTTON_L 23 25
FUNC_TEST=TRUE +PBUS 38
FUNC_TEST=TRUE +24V_PBUS 38
FUNC_TEST=YES GPU_VCORE 20 38
FUNC_TEST=YES CPU_VCORE_SLEEP 5 34 38
FUNC_TEST=YES VCORE_FB 34 38
FUNC_TEST=TRUE +1_8V_MAIN 38
FUNC_TEST=TRUE +3V_PMU 38
FUNC_TEST=YES +5V_DDC_SLEEP 22 38
FUNC_TEST=YES +12_8V_INV 22 38

FUNC_TEST=YES +5V_INV_SW 22 38
FUNC_TEST=YES LEFT_USB_DM 24 26 37
FUNC_TEST=YES LEFT_USB_DP 24 26 37
FUNC_TEST=YES RIGHT_USB_DM 26 32 37
FUNC_TEST=YES RIGHT_USB_DP 26 32 37
FUNC_TEST=YES NEC_LEFT_USB_PWREN 24 26
FUNC_TEST=YES NEC_LEFT_USB_OVERCURRENT 24 26
FUNC_TEST=YES NEC_RIGHT_USB_PWREN 26 32
FUNC_TEST=YES NEC_RIGHT_USB_OVERCURRENT 26 32
FUNC_TEST=YES DCDC_EN 20 29 32 33 34
FUNC_TEST=YES BBANG_HRESET_L 23
FUNC_TEST=YES LT1962_L3_ADJ 6
FUNC_TEST=YES MAIN_RESET_L 18 19 21 24 26 30
FUNC_TEST=YES RF_DISABLE_L_SPN 24
FUNC_TEST=YES AIRPORT_CLKRUN_L 24
FUNC_TEST=YES ROM_RW_L 10 13 24
FUNC_TEST=YES ROM_ONBOARD_CS_L 10 24
FUNC_TEST=YES ROM_CS_L 10 13 24
FUNC_TEST=YES CLK33M_AIRPORT 13 24 36
FUNC_TEST=YES AIRPORT_IDSEL 24
FUNC_TEST=YES ROM_OE_L 10 13 24

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6469	E
SCALE: NONE	SHT 39 OF 44	

REVISION HISTORY

RELEASED FOR PROTO 1 RELEASED FOR PROTO 1

REV 1.1 - 08/14/02

149/ UPDATED SOME NETS FOR CONCEPT 14.2 COMPLIANCE (PG 30,36)
150/ CORRECTED PMU PART NUMBER (PG 28)
151/ DELETED 4 0805 BULK CAPS AND ADDED 20 0402 BYPASS CAPS ON DDR SODIMM CONNECTOR (PG 12)
152/ REPINNED OUT J13 (HARD DRIVE) CONNECTOR FOR BETTER FLEX ROUTING (PG 24)
153/ ADDED A FEW MORE COMPONENTS TO ALS CIRCUIT BASED ON THAI'S RECOMMENDATIONS (PG 23)
154/ REMOVED PROTO1 CONNECTOR OPTIONS (PG 1, 22, 26, 27)
155/ ADDED USB 2.0 CONTROLLER (PG 26)
156/ CHANGED TO SPIDEY 39PIN ZIF CONNECTOR AND PINOUT (PG 23)
157/ ADDED INTREPID SSCG CHIP SUPPORT (PG 15)
158/ CONSOLIDATED BOMS
159/ UPDATED USB 2.0 SIGNAL CONSTRAINTS (PG 26)
160/ CHANGED CPU CORE VOLTAGE TO 1.45V FAST/1.40V SLOW (PG 33)
161/ ADDED +3V_SLEEP TO TUBA CONNECTOR (PG 25)
162/ MERGED MAXBUS_MAIN WITH MAXBUS_SLEEP BECAUSE INTREPID MAXBUS I/O CAN BE POWERED DOWN IN SLEEP (PG 16,17)
163/ DELETED ZT17 AND ZT2 BECAUSE THEY ARE NO LONGER NEEDED (PG 4)
164/ CHANGED FL1 TO NEW COMMON MODE CHOKES FOR FIREWIRE A (PG 28)
165/ CHANGED CRYSTAL VOLTAGE DIVIDER FOR FIREWIRE PHY TO 50/100 (BILL'S RECOMMENDATION) (PG 28)
166/ ADDED 2N7002 TO PREVENT PMU_SLEEP_LED_L FROM PUMPING UP +3V_MAIN DURING SHUTDOWN (PG 23)

REV 2.0 - 08/26/02

167/ DELETED USB POWER FET (PG 23)
168/ CHANGED 14PIN ZIF CONNECTORS AND PINOUT (PG 24,31)
169/ CONNECTED VGATE TO EXTINT10 BECAUSE NEED INTERRUPT CONTROL (PG 15)
170/ UPDATED A FEW CONSTRAINTS
171/ ADDED NEW QUAD-VCORE CONTROL CIRCUITRY (PG 33)
172/ CHANGED OPTICAL CONNECTOR PINOUT (PG 24)
173/ ADDED PMU_LID_CLOSED_L SIGNAL TO LMU (PG 23)
174/ ADDED Q11 ADAPTER DETECTION SCHEME (PG 29)
175/ ADDED DEDICATED RC FILTERING FOR PORT0 TX 0 (PG 28)
176/ ADDED STUFFING OPTION FOR DS1 PIN ON FIREWIRE PHY (PG 28)
177/ CHANGED STUFFING OPTION TO RAISE PLL VOLTAGE TO 1.95V FOR FW (PG 28)
178/ DELETED C741 (100UF INPUT CAP TO +3V_SLEEP) (PG 32)
179/ DELETED C757 (0.22UF BYPASS CAP FOR PCI1510) TO EASE TESTPOINT CONSTRAINTS (PG 18)
180/ SEPERATED PULL-UP FOR PCI_SERR_L AND PCI_PERR_L (PG 18,26)
181/ CHANGED SYSCLK_CPU, INT_PCI_FB_OUT, AND INT_AGP_FB_OUT SERIES RESISTOR VALUE (PG 9, 13)
182/ CHANGED C533, C539 TO 270PF AND CHANGED CONNECTIONS (PG 32)
183/ ADDED 4.7NF CAP ON Q51 GATE (PG 31)
184/ ADDED EMI SHIELD FOR INVERTER CHGND (PG 4)
185/ UPDATED MORE CONSTRAINTS
186/ CHANGED STUFFING OPTION TO FORCE 3V/5V INTO FORCE CONTINUOUS MODE TO REDUCE INDUCTOR SINGING (PG 32)
187/ CHANGED FW DVDD LDO TO 1.95V PER BILL'S RECOMMENDATION (PG 28)
189/ REMOVED C195 - 1.5V AGP(DOUBLED BYPASS), C24,C20 - 3VMAIN (DOUBLED BYPASS) FOR TESTPOINTS (PG 17)
190/ REMOVED C91 - 1.5V AGP BULK CAP BECAUSE THERE ARE 4 ON INTREPID SIDE ALREADY! (PG 20)
191/ CHANGED STUFFING OPTION TO FORCE 14V INTO FORCE CONTINUOUS MODE TO REDUCE INDUCTOR SINGING (PG 31)
192/ CHANGED STUFFING OPTION TO RAISE MARVELL CORE VOLTAGE TO 1.32V (PG 27)
193/ REMOVED COMMON MODE CHOKE FOR FIREWIRE B SIGNALS (PG 28)
194/ CHANGED LINE_WIDTH FOR FIREWIRE SIGNALS TO MAKE THEM 55OHM SINGLE AND 110OHM DIFFERENTIAL (PG 36)
195/ CHANGED STUFFING OPTION TO ENABLE 1.5V_LDO AND MAKE 1.5V_MAIN INTO 1.8V (PG 16, 19, 34)
196/ ADDED BACK IN COMMON MODE CHOKE FOR FIREWIRE B TO ENSURE TESTABILITY (PG 28)

RELEASED FOR PROTO 2 RELEASED FOR PROTO 2

LAST MINUTE BOM CHANGES FOR PROTO2 (9/5/02)

197/ STUFFED 20K FEEDBACK RESISTOR FOR MARVELL 88E1111 CRYSTAL (PG 27)
198/ NO STUFFED 4700PF FOR 14V PBUS GATE - C741 (PG 31)
199/ NO STUFFED L4 AND L5, FIREWIRE COMMON MODE CHOKES (PG 28)
200/ CHANGED BOOTROM APN FOR SHARP DIE-SHRINK PACAKGE (PG 10)
201/ CHANGED VCORE STUFFING OPTION FOR 1GHZ PROCESSOR (PG 33)

REV 3.0 - 09/20/02

202/ COMBINED FIREWIRE FUSE INTO ONE TO LIMIT PORT POWER TO 22W@24V OR 13.5W@15V (PG 28)
203/ UPDATED L3 SYMBOLS TO REFLECT MISSING SA17 SIGNAL ON 4MBIT PARTS VS. 8MBIT PARTS (PG 8)
204/ CHANGED TO NEW SPIDEY CONNECTOR AND PINOUT (PG 23)
205/ REMOVED P93 SUPPORT CIRCUIT (PG 25)
206/ ADDED 0 OHM RESISTOR FOR 2.5V_MARVELL TO MEASURE CURRENT (PG 27)
207/ ADDED 0 OHM RESISTOR FOR POWER BUTTON - DEBUG (PG 25)
208/ ADDED 2 JUMPERS FOR PMU_RESET_BUTTON_L AND PMU_NMI_BUTTON_L (PG 25)
209/ CHANGED TO PROTO2 BOM OPTION - INTREPID REV 2.0, AND MARVELL 2.0 CHANGES

RELEASED FOR PROTO 2-ENCLOSURE RELEASED FOR PROTO 2-ENCLOSURE

LAST MINUTE BOM CHANGES FOR PROTO2-ENCLOSURE (9/25/02)

210/ CHANGED R474 TO 49.9K, 1%, R475 TO 1.0K, 1%, AND R683 TO 10.7K, 1% (PG 30)
211/ CHANGED INTRPEID PART NUMBER TO REV 2.0 (PG 9-16)

REV 4.0 - 10/24/02

212/ ADDED 10K PULL-UP STUFFING OPTION TO CG_ADDRSEL AND 10K PULL-DOWN STUFFING OPTION TO CG_FSEL (PG 15)
213/ REMOVED ZEBRA 15/16 SUPPORT (PG 28)
214/ REMOVED NO_TEST=TRUE PROPERTY ON MAXBUS/L3 BUS (PG 35)
215/ ADDED FUNCTIONAL TEST POINT DEFINITION (PG 38)
216/ REPLACED IRF7822 IN THE BATTERY CHARGER AND 14V SWITCHER SECTION WITH IRF7811W (PG 30, 31)
217/ DELETED CAPACITOR OPTION ON INT_CPUFB_IN - MAKE RISE/FALL TIME WORSE (PG 9)
218/ CHANGED POWER SUPPLY TO FAN TO +3V_SLEEP (PG 25)
219/ UPDATED TO NEW EMI SHIELD PART NUMBER, AND NEW 300MHZ SRAM PART NUMBER (PG 4, 8)
220/ SWITCHED TO NEW 16PIN MODEM CONNECTOR (PG 25)
221/ FIXED AGP CLOCK CONSTRAINTS (PG 13,35)
222/ DELETED PULL-UP RESISTOR TO VCORE_VCC ON VGATE SINCE THERE'S A 10K PULL-UP RESISTOR ON INTREPID SIDE (PG 33)
223/ ADDED BACK INDIVIDUAL FUSE FOR FIREWIRE PORT (PG 28)
224/ SEPARATED FW PORTS TO ANOTHER PAGE; UPDATED PIN DEFINITIONS (PG 28, 29)
225/ ADDED 2 10K PULL-UP TO USB NC PINS (M6 AND P6) - PER NEC (PG 26)
226/ CHANGED SMBUS PULL-UP RESISTOR TO 7.15K (DON'T HAVE ANOTHER 5% ~7K RESISTOR IN BOM) - PER IBOOK (PG 30)
227/ DELETED ALL INTREPID_REV1 STUFFING OPTION (PG 9-16)
228/ CHANGED TO NEW MOUNTING HOLE SIZES - ALL INCREASED BY 0.2MM IN DIAMETER EXCEPT FOR THREE CPU MTG HOLES (PG 4)
229/ CHANGED BOM OPTION TO 167MHZ BUS WITH PLL SET TO 1GHZ/833MHZ (PG 7,9)
230/ CHANGED TO 10K PULL-DOWN FOR MOD_DTI, MOD_SYNC, AND MOD_BITCLK - PER INTREPID PADS SPREADSHEET (PG 14)
231/ CHANGED JUMPER PADS FOR PMU_RESET_L AND PMU_NMI_L TO 0603 RESISTOR PADS (PG 25)
232/ ADDED DAMPING RESISTOR FOR 8MHZ CRYSTAL (PG 23)
233/ CHANGED INT_PLL_EN_PD TO PULL-DOWN AND CHANGED JTAG_ENET_TDI TO PULL-UP (PG 14)
234/ DISCONNECTED FW_LKON FROM INT_EXTINT3_PU BECAUSE FW_LKON OUTPUT NOW WORKS FINE (PG 15)
235/ CHANGED R21 TO +3V_SLEEP TO PREVENT LEAKAGE TO MAXBUS_SLEEP BEFORE LMU SETS OUTPUT AS OPEN-DRAIN (PG 23)
236/ CHANGED FW_PD AND FW_PU TO 5% RESISTORS (PG 28)
237/ ADDED FIREWIRE PORT CURRENT LIMITER (PG 29)
238/ CHANGED +14V_PBUS TO +PBUS SINCE THE VOLTAGE MAY CHANGE BACK AND FORTH (PG ALL)
239/ ADDED A29 ADAPTER DETECT (PG 30)
240/ ADDED NEW SYSTEM CURRENT MONITOR FOR +PBUS (PG 31)
241/ DELETED OLD BATTERY CURRENT LIMITER CIRCUIT (PG 31)
242/ ADDED C843 TO SPEED UP Q10 TURN ON AND CHANGED Q14 TURN ON TO AC_IN (PG 31)
243/ REMOVED C650 (2MILLOHM) SENSE RESISTOR FROM CPU_VCORE SWITCHER BECAUSE IT CAUSES TOO MUCH DROOP ON VOLTAGE (PG 34)
244/ REPLACED LMC6462 WITH LMC7111 BECAUSE ONLY NEED 1 OP-AMP (PG 31)
245/ CHANGED LTC4210 TIMER CAPACITOR TO ONE 0805 INSTEAD OF TWO 0402 (PG 29)
246/ FINALIZED ALL POWER SUPPLY CHANGES (PG 29-32)
247/ CHANGED TO NEW CALIFORNIA MICRO DEVICES LOW-CAPACITANCE ESD DIODES FOR FIREWIRE (PG 29)
248/ ADDED 1K PULL-DOWN TO FW_DS1, FW_SE, AND FW_SM INPUTS PER TI'S RECOMMENDATION (PG 28)
249/ CHANGED DS1 (PIN 32) TO PULL-UP FOR A-ONLY OPERATION (PG 28)
250/ ADDED MORE FUNCTIONAL TEST POINTS PER WAYNE'S INPUT (PG 39)
251/ CHANGED BACK TO OLD BAV99DW DIODES BECAUSE CMD1210 CAN ONLY HANDLE 8MA FORWARD CURRENT (PG 29)
252/ REMOVED COMMON MODE CHOKE PADS FOR FIREWIRE B (PG 29)
253/ ADDED PULL-UP TO PMU_SLEEP_LED_L AND CHANGED R451 TO PULL-DOWN SLEEP_LED_H TO ENSURE STATES WHEN CHIPS TRISTATE OUTPUTS (PG 23)
254/ ADDED SILICON IMAGE SI1162 - FIRST PASS (PG 21)
255/ UPDATED DVI_HPD CIRCUIT PER HYDRA IMPLEMENTATION (PG 22)
256/ REPINNED OUT TUBA CONNECTOR (PG 25)
257/ SWAPPED JTAG_CPU_TRST_L AND JTAG_CPU_TDI WITH SENSOR5_I2C*_PD BECAUSE 200OHM PULL-DOWN PREVENTS IN-CIRCUIT PROGRAMMING ON PA0
258/ REMOVED XW17 - CPU_VCORE_JUMPER - FOR HUGE COPPER POUR (PG 34)
259/ ADDED PART NUMBER TABLE FOR SPEAKER CLIP (PG 4)
260/ MIRRORED AIRPORT CONNECTOR BECAUSE CONNECTIONS ARE MIRRORED ON THE FLEX (PG 24)
261/ FINALIZED ALL CHANGES FOR SI1162 PART - RUNNING HIGH SWING MODE (PG 21)
262/ CHANGED TO SI3446DV FOR FAN FETS (PG 25)
263/ PULLED DS2 HIGH TO SHUT-OFF PORT 3 ON FIREWIRE PHY COMPLETELY (PG 28)
264/ ADDED ONE MORE 1000UF POSCAP ON CPU_VCORE_SLEEP TO REDUCE RIPPLE BY ANOTHER 10MV, AND CHANGED OFFSET TO +30MV (PG 34)
265/ FINE TUNED PCI SERIES RESISTOR R VALUES FOR EMI AND DIVIDED CY28512 OUTPUT FROM 2.5V TO 1.5V (PG 13,15)
266/ CY28512 NOW RUNS ON 3V_MAIN AND 2.5V_MAIN... UPDATED THE STRAPS TOO (PG 15)
267/ ALS SENSOR IS NOW RUNNING DURING SLEEP PER THAI'S REQUEST (PG 23, 24)
268/ CHGND1 NOW SPLITS INTO CHGND1 AND CHGND6 BECAUSE OF FIREWIRE B ROUTING ON THE SURFACE (PG 29)
269/ SEPARATED 0 OHM RESISTORS FOR EACH FIREWIRE GROUND PINS (PG 29)
270/ CY28512 RESET PIN NOW GOES TO +3V_MAIN - INT_RESET_L WILL NOT WORK (PG 15)
271/ CHANGED PULL-UPS FOR FAN CONTROL SIGNALS TO +3V_SLEEP - LEAKAGE PROBLEM THROUGH THE FAN (PG 25)
272/ NO STUFFED PULL-UP RESISTORS FOR EIDE_RESET AND EIDE_DMAACK_L - PER MKE DRIVE SPEC (PG 24)

RELEASED FOR EVT RELEASED FOR EVT

LAST MINUTE BOM CHANGES FOR PROTO2 (10/29/02)

273/ UPDATED BOMOPTION "NO SSCG" TO "NO_SSCG" (PG 9)
274/ FIXED SYSTEM BUS TO 167MHZ OPERATION BECAUSE WE ARE USING INTREPID 2.0 (PG 15)

REV 5.0 - 12/03/02

275/ P50 IS ONLY POWERED BY +3V_SLEEP NOW (PG 24)
276/ CHANGED TO ONE 1.5A FIREWIRE FUSE (PG 29)
277/ ADDED PULL-DOWN TO P50'S CLKRUN_L SIGNAL AND NO CONNECTED P50'S PME SIGNAL (PG 24)
278/ CHANGED PCI PULL-UP RESISTORS TO +3V_SLEEP TO SUPPORT P50 D3COLD (PG 13)
279/ ADDED TWO 4.7UF BULK CAPS NEAR THE FAN CONNECTORS (PG 25)
280/ FAN POWER GOES BACK TO +5V_SLEEP (PG 25)
281/ NEW PART NUMBERS FOR INTREPID 2.1, ZEBRA-17, BS520, 50&80PIN CONNECTORS, NEW CPU DESC.
282/ NEW BOOT ROM AND LMU PART NUMBERS (PG 11, 23)
283/ FIXED DRCS AROUND SIL1162 BY CHANGING CONSTRAINTS (PG 21)
284/ ADDED SLEEP FET FOR +5V_SOUND (PG 25)
285/ ADDED 5A FUSE FOR FIREWIRE PORT POWER - FOR SAFETY COMPLIANCE (PG 29)
286/ ADDED ESD AND LATE VG PROTECTION FOR FIREWIRE (PG 29)
287/ CHANGED NOMINAL VCORE VOLTAGE TO 1.36V BECAUSE OF +/-50 MV REQUIREMENT ON GPU_VCORE (PG 20)
288/ CHANGED SIL1162 TO RISING CLOCK EDGE - STUFFING CHANGE (PG 21)
289/ ADDED DUAL SCHOTTKY FOR FIREWIRE PHY POWER (PG 28)
290/ ADDED STUFFING OPTION TO FEED MAIN_RESET_L TO PCI1510 (PG 18)
291/ LOADED IN NEW MECHANICAL SYMBOLS FOR WIRELESS,CARDBUS, AND HARD/OPTICAL DRIVES
292/ NO STUFFED R888 BECAUSE THERE'S A WEAK INTERNAL PULL-UP ALREADY (PG 15)
293/ ADDED TWO 0805 ZERO OHM RESISTORS TO FEED IN EITHER +2_5V_SLEEP OR +2_5V_MAIN TO INTREPID (PG 16)
294/ CHANGED GPU_VCORE SWITCHER BOM OPTIONS TO REDUCE JITTER ON SUPPLY (PG 20)
295/ CONNECTED MAX4172 POWER TO +ADAPTER_SW TO SAVE 1MA WHEN RUNNING ON BATTERY ONLY (PG 31)
296/ CHANGED Q47 AND Q58 TO 7811W FOR BOM CONSOLIDATION - ALSO CHANGED R348 AND R353 TO 113K TO ADJUST CURRENT LIMIT (PG 35)
297/ UPDATED BOM OPTION FOR SSCG (PG 9, 15)
298/ CHANGED RESET CAP TO 0.22UF ON TI PHY PER TI'S RECOMMENDATION (PG 28)
299/ UPDATED TO NEW TUBA CONNECTOR PINOUT (PG 25)
300/ CHANGED BOOTROM RESET TO INT_RESET_L FOR ICT (PG 10)
301/ ADDED 4 ZERO OHM RESISTORS TO NO STUFF THE QUAD_VCORE OPTION (PG 34)
302/ CHANGED ALL 132S1061 (0805 PACKAGE) TO 132S0046 (0603 PACKAGE) - (PG ALL)
303/ CHANGED TO TOP CONTACT SPIDEY CONNECTOR (PG 23)
304/ ADDED BOM OPTION TO PCI CLOCK OUT FROM INTREPID TO USB CONTROLLER (PG 13)
305/ CHANGED TO NEW 30PIN TUBA CONNECTOR WITH SOLDER TAPS (PG 25)
306/ UPDATED ETHERNET SERIES R VALUES (PG 14, 27)
307/ CONSOLIDATED 1UF, 10% CAPS TO 1UF, 20% CAPS (PG 28,31)
308/ CHANGED CURRENT LIMIT SETTINGS FOR 1.5V AND 2.5V SWITCHER (PG 35)
309/ ADDED FOUR PULL-DOWN RESISTORS ON CKE FOR DDR MEMORY (PG 10)
310/ ADDED THREE 0402 CAP PADS ON SND_SCLK, SND_CLKOUT, AND LVDS_DDC_CLK FOR EMI (PG 22, 25)
311/ ADDED 5 SPEAKER CLIPS SYMBOLS (PG 4)
312/ CHANGED VCORE OFFSET TO 10MV -> EVT BOARD MEASURED: IDLE 1.407V, SMOKE 1.387V, TRANSIENT 1.37V (PG 34)
313/ ADDED RESISTOR TO TPS2211 SHUTDOWN# PIN TO SUPPORT PSUEDO-D3COLD (PG 18)

RELEASED FOR DVT RELEASED FOR DVT

LAST MINUTE BOM CHANGES FOR DVT (12/20/02)

314/ CHANGED CPU VCORE TO 1.32V@1GHZ AND 1.15V@667MHZ (PG 34)
315/ CHANGED STUFFING OPTION TO ENABLE PCI SPREADING (PG 9)
316/ CHANGED STUFFING OPTION FOR A/B* SELECT ON MAX1717 TO SUPPORT L3 AT SLOW SPEED (PG 34)
317/ NO STUFFED R694 AND STUFFED R727 TO RESTOR ORIGINAL VCORE STEPPING CONTROL (PG 34)
318/ CHANGED RP55 AND RP56 TO 22OHM RPAKS (PG 21)
319/ CHANGED R664 FROM 0OHM TO 10K BECAUSE IT SHOULD BE A WEAK PULL-DOWN (PG 24)

REV A - 01/14/03

320/ REMOVED LTC4210 BECAUSE OF RELIABILITY ISSUES, AND UPDATED PORT CONTROL WITH OLD METHOD PLUS A NEW 1.5A FUSE (PG 29)
321/ MOVED AMP AND HP MUTE CONTROL FROM TUBA TO MLB, AND INT_PU_RESET_L IS NOW "AND"ED WITH THE SIGNALS (PG 25)
322/ CHANGED ZT10 TO THE NEW PD STANDOFF, BS1 (PG 4)
323/ REMOVED ALL JUMPERS FOR PRODUCTION (PG TOO MANY)
324/ CHANGED R152 TO 511 OHM, 1% TO AVOID LOW CPU CLOCK AMPLITUDE (PG 9)
325/ CHANGED R451 TO 10K FROM 100K (PG 23) - OTHERWISE, IT MAY BE TOO WEAK
326/ REMOVED R621 AND CONNECTED R608 TO GROUND WITH 10K RESISTOR TO ENSURE KBD LED IS OFF WHEN LMU IS IN RESET (PG 23)
327/ SWAPPED R265 AND R653 VALUES BECAUSE BATTERY VOLTAGE CAN GO DOWN TO 10.4V, AND WE NEED TO ENSURE VGS<-4.5V (PG 29)
328/ UPDATED TO NEW S-VIDEO FILTER VALUES (PG 22)
329/ ADDED ONE MORE SPEAKER CLIP FOR PD (PG 4)
330/ SWITCHED FAN TACH AND GROUND ON CONNECTOR FOR PD (PG 25)
331/ CHANGED TO 330HM RPAKS FOR TMDS (PG 21)
332/ REMOVED U1 BECAUSE NO USING 1.5V MAXBUS NOR 1.5V L3 INTERFACE STRAPS (PG 7)

RELEASED FOR DVT2 RELEASED FOR DVT2

LAST MINUTE BOM CHANGES FOR DVT2 (1/18/03)

333/ CHANGED INPUT CAPS FOR CPU_VCORE FROM 4.7UF CERAMIC CAPS TO 22UF POSCAPS (PG 34)
334/ CHANGED R439 FROM 100K PULL-UP TO 470HM SERIES CONNECTED TO IO_RESET_L - MAKING SURE LMU RESETS ACROSS RESTART (PG 23)
335/ CHANGED SCHEMATIC NUMBER TO 051-6425 AND PCB NUMBER TO 820-1502 (PG 1)

ANOTHER LAST MINUTE BOM CHANGES FOR DVT2 (1/24/03)

336/ CHANGE R389 TO 20K AND R395 TO 47K TO ENABLE BURST MODE OPERATION ON LTC3707 (PG 33)
337/ RP55 AND RP56 CHANGED TO 22OHM AND L17 CHANGED TO 3700HM COMMON MODE CHOKE (PG 21)

RELEASED FOR PVT RELEASED FOR PVT

REV A (051-6442) - 02/28/03

338/ BOM OMITTED SANYO CAPS AND ADDED KEMET 10UF AND PANASONIC 8.2UF AL POLYMER CAPS AT 7 LOCATIONS (PG 34)
339/ CHANGED R8 AND R70 TO 4.7K INSTEAD OF 10K TO IMPROVE RISE/FALL TIME (PG 15)
340/ CHANGED SCHEMATIC NUMBER TO 051-6442 (PG 1)
341/ UPDATED SYMBOL FOR U28 - FIREWIRE A PHY (PG 28)
342/ UPDATED SYMBOL FOR D22,D26,D29,D31,AND D33 - TO CORRECT SCHOTTKY DIODE SYMBOL (PG 29,31-33)
343/ CHANGED C263 FROM 0.01UF TO 0.22UF TO FIX EXTERNAL BRIGHTNESS FLUCTUATION ON CRT (PG 21)
344/ CHANGED Q60 TO NEW SYMBOL WITH ONLY IRF ON AVL (PG 31)

RELEASED FOR PRODUCTION RELEASED FOR PRODUCTION

REV B (051-6442) - 03/06/03

345/ UPDATED FIREWIRE PHY TO NEW "REV A" PART NUMBER (PG 28)
346/ UPDATED BOOT ROM TO NEW "REV A" PART NUMBER (PG 10)
347/ CHANGED C550 TO NEW APN 138S0536 - ONLY TAIYO YUDEN APPROVED DUE TO MAX 1.9MM HEIGHT REQUIREMENT (PG 30)
348/ CHANGED ALL 14 4.7UF, 1210, X7R CAP FROM 138S0501 TO 138S0531 (4.7UF, 1206, X5R) DUE TO MAX 1.9MM HEIGHT REQUIREMENT

BOM UPDATE FOR PRODUCTION BOM UPDATE FOR PRODUCTION

REV A (051-6469) - 04/09/03

349/ UPDATED SCHEMATIC NUMBER TO 051-6469 (PG 1)
350/ CHANGED C591 AND C595 TO 0.01UF TO SPEED UP 1.95V_DVDD AND 1.95V_PLLVDD RAMP TIME (PG 28)

BOM UPDATE FOR PRODUCTION BOM UPDATE FOR PRODUCTION

REV B (051-6469) - 04/25/03

351/ CHANGED D31 FROM MBRS140T3 TO BS240 TO INCREASE THE CONSTANT CURRENT CAPABILITY FROM 1A TO 2A (PG 29)
352/ CHANGED C720 TO SANYO ONLY PART BECAUSE OF PROBLEMS AT THE FACTORY/FIELD (PG 1)

BOM UPDATE FOR PRODUCTION BOM UPDATE FOR PRODUCTION

REV C (051-6469) - 06/05/03

353/ CHANGED CPU P/N TO 337S2775 FOR THE SICOH PROCESSORS (PG 5,6)
354/ CHANGED L31 FROM 152S0036 TO 152S0125 (PG 34)
355/ CHANGED L32 FROM 152S1003 TO 152S0126 (PG 32)

BOM UPDATE FOR PRODUCTION

REV D (051-6469) - 07/22/03

356/ CHANGED J21 TO NEW GOLD PLATE 80PIN CONNECTOR 516S0142 (PG 24)

BOM UPDATE FOR PRODUCTION

REV E (051-6469) - 08/07/03

357/ DISQUALIFIED AND REMOVED KEMET POLYMER CAPS FOR CPU_VCORE(PG 34)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6469	E
SCALE: NONE	SHT 40 OF 44	

*** Signal Cross-Reference ***
--- for the entire design --

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6469	E
SCALE NONE	SHT 41 OF 44	

CR-42

USB_DEM	15B2 15C2 37B2
USB_DEP	15B2 15C2 37B2
USB_DFM	15B2 37B2
USB_DFP	15B2 37B2
USB_OC_AB_L	15B2 15C7
USB_OC_CD_L	15B2 15C7
USB_OC_EF_L	15B2 15C7
USB_PWREN_AB_L	15B2 15C7
USB_PWREN_CD_L	15B2 15C7
USB_PWREN_EF_L	15B2 15D7
VCORE_BOOST	34C4 38C1
VCORE_BST	34C5 38C1
VCORE_CC	34B6 38B1
VCORE_DH	34B5 38C1
VCORE_DL	34B5 38C1
VCORE_FAST<4..1>	34D2 34D3 34D5
VCORE_FB	34B5 38B1 39A2
VCORE_GND	34B5 38B1
VCORE_GNDA	34B6
VCORE_GNDDIV	34A5 34B5 38B1
VCORE_GNDDIV_TEST	34A4
VCORE_GNDSNS	34A1 34A5 38B1
VCORE_GNDSNS_TEST	34A4
VCORE_ILIM	34C6 38C1
VCORE_LX	34B5 38C1
VCORE_MUX_EN	34D5
VCORE_MUX_SEL	34D5
VCORE_REF	34B6 38C1
VCORE_SHDN_L	34C6
VCORE_SLOW<4..1>	34D6
VCORE_SNS	34A1 38B1
VCORE_TIME	34B4 38B1
VCORE_TON	34B6 38C1
VCORE_VCC	34C6 38C1
VCORE_VGATE	15B5 15B7 34B4 38B1
VCORE_VID<4..0>	34A3 34B8 34D4
VGA_B	22C6 22D7 39D7
VGA_G	22C5 22D7 39D7
VGA_HSYNC	21D4 22C6 39D7
VGA_R	22C5 22D7 39D7
VGA_VSYNC	21D4 22C5 39D7
VIPPCLK_PD	19C2

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6469	E

SCALE	SHT
NONE	42 OF 44

CR-43

*** Unit Cross-Reference ***
--- for the entire design --

BS1	PCB_STANDOFF	4D3
C1	CAP	34C2
C2	CAP	34D1
C3	CAP	34D2
C4	CAP	34C1
C5	CAP	34C1
C6	CAP	34D1
C7	CAP	34C1
C8	CAP	34D1
C9	CAP	5D4
C10	CAP	17C4
C11	CAP	17D8
C12	CAP	17C4
C13	CAP	19C5
C14	CAP	34C2
C15	CAP	35A6
C16	CAP	15A5
C17	CAP	17C3
C18	CAP	17B2
C19	CAP	17B3
C21	CAP	17C1
C22	CAP	17B2
C23	CAP	17C2
C24	CAP	21D3
C25	CAP	17B2
C26	CAP	17B3
C27	CAP	17B1
C28	CAP	19C5
C29	CAP	5D4
C30	CAP	5D6
C31	CAP	5D6
C32	CAP	34D1
C33	CAP	17C1
C34	CAP	17B1
C35	CAP	17C1
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C845	CAP	21D3
C846	CAP	21D2
C847	CAP	21D2
C848	CAP	21D2
C849	CAP	21D2
C850	CAP	21D2
C851	CAP	21D2
C852	CAP	21D1
C853	CAP	22C1
C854	CAP_P	34B2
C855	CAP	25A3
C856	CAP	25B2
C857	CAP	25D7
C858	CAP	25D7
C859	CAP	29B5
C860	CAP	29D4
C861	CAP	29D4
C862	CAP	29B3
C863	CAP	29D3
C864	CAP	29D2
C865	CAP	22B4
C866	CAP	25C6
C867	CAP	25C6
C1000	CAP	28C5
C1600	CAP	16B3
C1601	CAP	16B2
C1602	CAP	16B1
D1	DIODE	27B7
D2	DIODE_SCHOT	34C4
D3	DIODE_SCHOT	32C5
D4	DIODE	32C7
D5	DIODE	20C6
D6	DIODE_DUAL_6P	29D3
D7	DIODE_SCHOT	33D5
D8	DIODE_DUAL_6P	29D2
D9	DIODE_SCHOT	32B4
D10	DIODE	31C5
D11	DIODE	31C3
D12	DIODE_SCHOT	32A4
D13	DIODE_DUAL_6P	29B4
D14	DIODE_SCHOT	33D4
D15	DIODE_DUAL_6P	29B4
D16	DIODE	33B6
D17	DIODE_SCHOT	32B6
D18	DIODE_SCHOT	32A6
D19	DIODE_SCHOT	32A6
D20	DIODE_SCHOT	28D7
D21	DIODE_SCHOT	22D5
D22	DIODE_SCHOT	33C7
D23	DIODE_SCHOT	35B6
D24	DIODE_SCHOT	20C5
D25	DIODE	34B2
D26	DIODE_SCHOT	32C4
D27	DIODE_SCHOT_3P2	28D8
D28	DIODE	31D1
D29	DIODE_SCHOT	31B2
D30	DIODE	31D2
D31	DIODE_SCHOT	29D5
D32	DIODE_SCHOT	35B2
D33	DIODE_SCHOT	33C3
DP1	DPAK3P	34C7 34D7
DP2	DPAK3P	35C3 35D6 35D7
DP3	DPAK3P	31C1 31C2 31D3
DP4	DPAK3P	29C6 29D6
DP20	DPAK3P	20D7
DZ2	ZENER	29D3
F1	FUSE	22D6
F2	FUSE	29D7
F3	FUSE	29D5
F4	FUSE	31D1
F5	FUSE	31D1
G1	OSC	28A4
J1	CON_F1ST_S2MT_SM	15A6
J2	CON_3RTSM_125	25B2
J3	CON_F14RT_S2MT_SM	24B1
J4	CON_3RTSM_125	25A3
J5	CON_10STSM_5087	25D1
J6	CON_12	34A4
J7	CON_F30RT_S2MT_SM	22B3
J8	CON_4RT_WRIB	22B1
J9	CON_F16ST_D_SMA	25C3
J10	CON_M80ST_D4MT_SM	18C2
J11	CON_M50SM_5MM	24B5
J12	CON_F14RT_S2MT_SM	32B8
J13	CON_M50SM_5MM	24D1
J14	CON_F30ST_D_SM	25D6
J15	CON_F40RT_S2MT_SM	23C6
J16	CON_F30RT_T6MT_TH1	22D6
J17	CON_F5RT_MINIDIN_TH	22B6
J18	CON_RJ45_SHORT_4MT_TH	27C1
J19	CON_M8RT_S_SM	31D8
J20	CON_F200RT_DDRDIMM_SM1	12D7
J21	CON_F80ST_D4MT_SM	24D5
J22	CON_F9RT_S2MT_SMA	29C1
J23	CON_F200RT_DDRDIMM_SM2	12D4
J24	CON_F6RT_S4MT_TH1	29A2
J25	CON_M8RT_S_SM	31A4
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L2	IND	22A4
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L5	IND	21D3
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L12	IND	22D7
L13	IND	22D8
L14	IND	35A4
L15	IND	22D7
L16	IND	22D8
L17	FILTER_4P	22C8
L18	IND	22D5
L19	IND	21A4
L20	IND	22B7
L21	IND	22B7
L22	IND	22A7
L23	IND	22A7
L24	IND	22B7
L25	IND	20C5
L26	IND	22B2
L27	IND	27C4
L28	IND	22B2
L29	IND	22B2
L30	IND	35B7
L31	IND_3P	34C2
L32	IND_3P	32C4
L33	IND_3P	33D7
L34	IND	29C4
L35	IND_3P	33D2
L36	IND	31B2
L37	IND	29C5
L38	IND	35B2
L39	IND	23C1
L40	IND	31A3
L41	IND	28D7
L42	IND	23A7
L43	IND	23A7
L44	IND	23A7
L45	IND	23C7
L46	IND	23A7
L47	IND	27D3
L48	IND	26D7
L49	IND	15C6
L50	IND	15C5
L51	FILTER_4P	29B3
L52	FILTER_4P	29A3
L53	IND	21D1
L54	IND	29D4
PD1	PHOTODIODE_2P	23D8
Q1	TRA_FDG6324L	22B2
Q2	TRA_2N7002	22A6
Q3	TRA_2N7002DW	33A3 33A4
Q4	TRA_2N7002DW	31C6 31C7
Q5	TRA_SI3443DV	22A5
Q6	TRA_2N3904	34D7
Q7	TRA_NDS9407	29D6
Q8	TRA_SI4435DY	31D6
Q9	TRA_FDG6324L	32D6
Q10	TRA_SI4435DY	31D5
Q11	TRA_2N3904	34D7
Q12	TRA_2N7002DW	20B5 20C7
Q13	TRA_2N7002	35C6
Q14	TRA_2N7002DW	31C2 31C5
Q15	TRA_2N7002DW	33B5
Q16	TRA_SI4435DY	31D2
Q17	TRA_2N7002DW	29C7 33A6
Q18	TRA_2N3906	23C1
Q19	TRA_2N7002DW	31B7 31B8
Q20	TRA_2N7002DW	23C2 23C3
Q21	TRA_SI3443DV	33B2
Q22	TRA_2N7002DW	31B6
Q23	TRA_2N7002DW	31A7
Q24	TRA_SI3443DV	33A7
Q25	TRA_2N3904	7C6
Q26	TRA_2N7002	7C7
Q27	TRA_SI3446DV	25B3
Q28	TRA_2N7002DW	7C7
Q29	TRA_2N7002DW	22C4 22D4
Q30	TRA_SI3446DV	25A3
Q31	TRA_2N3904	25B6
Q32	TRA_TP0610	22D3
Q33	TRA_2N7002DW	22C2
Q34	TRA_2N3904	22D1
Q35	TRA_SI3443DV	33A7
Q36	TRA_2N3904	22C1
Q37	TRA_SI3446DV	35D7
Q38	TRA_2N3904	25A6
Q39	TRA_IRF7811W	20C6
Q40	TRA_IRF7805	34C3
Q41	TRA_IRF7805	34C4
Q42	TRA_IRF7805	20C6
Q43	TRA_SI4888DY	33C6
Q44	TRA_IRF7822	34B3
Q45	TRA_IRF7822	34B4
Q46	TRA_IRF7822	34B3
Q47	TRA_IRF7811W	35B6
Q48	TRA_IRF7805	35C6
Q49	TRA_SI3443DV	25D7
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Q51	TRA_IRF7811W	32C4
Q52	TRA_SI4888DY	33D6
Q53	TRA_2N3904	25A6
Q54	TRA_IRF7805	31B3
Q55	TRA_IRF7811W	31B3
Q56	TRA_2N3904	25B6
Q57	TRA_2N7002	30A3
Q58	TRA_IRF7811W	35B3
Q59	TRA_IRF7805	35C3
Q60	TRA_IRF7416	31D1
Q61	TRA_SI4888DY	33D3
Q62	TRA_SI4888DY	33C3
Q63	TRA_2N3906	23B8
Q64	TRA_2N3906	23B8
Q65	TRA_2N7002DW	27A7 27B7
Q66	TRA_2N7002DW	31A4 31C3
Q67	TRA_2N7002DW	25C5
Q68	TRA_2N7002DW	22C4 23C7
Q69	TRA_2N7002DW	25D5
Q70	TRA_TP0610	22C2
Q71	TRA_2N7002DW	29C6
Q2000	TRA_2N3904	20D7
Q2001	TRA_2N3904	20D7
Q3100	TRA_2N7002DW	31C3 31C4
R1	RES	23B3
R2	RES	15D8
R3	RES	24C4
R4	RES	15C1
R5	RES	5D4
R6	RES	7B6
R7	RES	15A6
R8	RES	15A3
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R24	RES	5C1
R25	RES	15A6
R26	RES	14C7
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R28	RES	19C6
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R35	RES	19B4
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R37	RES	5C1
R38	RES	5C1
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R45	RES	15C2
R46	RES	24A3
R47	RES	24B3
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R49	RES	13A5
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R51	RES	5C3
R52	RES	15D2
R53	RES	24A8
R54	RES	13A5
R55	RES	5C1
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R74	RES	5C1
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R76	RES	15A8
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R86	RES	9C8
R87	RES	9D7
R88	RES	14C5
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R91	RES	5A1
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R95	RES	9C7
R96	RES	9D8
R97	RES	9C8
R98	RES	9A6
R99	RES	19B8
R100	RES	9B2
R101	RES	9B7
R102	RES	9C8
R103	RES	9C7
R104	RES	9A6
R105	RES	14C3
R106	RES	13D3
R107	RES	13D8
R108	RES	9B1
R109	RES	9B7

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6469 | REV. E

SCALE NONE | SHT 43 OF 44

CR-44

R110	RES	9C7
R111	RES	9D7
R112	RES	14A7
R113	RES	15D4
R114	RES	15D4
R115	RES	19B8
R116	RES	9B2
R117	RES	9B7
R118	RES	9B7
R119	RES	9C7
R120	RES	9C6
R121	RES	9D7
R122	RES	9A5
R123	RES	15D4
R124	RES	26B3
R125	RES	13A1
R126	RES	13C8
R127	RES	21D4
R128	RES	19A8
R129	RES	9B1
R130	RES	9B2
R131	RES	9B6
R132	RES	9C7
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R135	RES	13B5
R136	RES	19A8
R137	RES	9B1
R138	RES	9B7
R139	RES	9C7
R140	RES	13C5
R141	RES	13C8
R142	RES	20B4
R143	RES	35B3
R144	RES	10A7
R145	RES	13B1
R146	RES	13D8
R147	RES	13B1
R148	RES	13B1
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R151	RES	9A4
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R156	RES	21D4
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R167	RES	20C4
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R172	RES	21B4
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R180	RES	21A5
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R182	RES	26B3
R183	RES	21D7
R184	RES	21B7
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R251	RES	34D5
R252	RES	34A4
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R257	RES	34D5
R258	RES	34D5
R259	RES	27C3
R260	RES	34D5
R261	RES	25C1
R262	RES	23D6
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R266	RES	30A4
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R583	RES	9B2
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R759	RES	15C7
R760	RES	21C7
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R2501	RES	25B1
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RP2	RPAK4P	24C3 24D3
RP3	RPAK4P	24B3 24C3
RP4	RPAK4P	24B3 24C3
RP5	RPAK4P	24B3 24C3
RP6	RPAK4P	15A8 15B8 15C8
RP7	RPAK4P	15A8 15C8 15D1
RP8	RPAK4P	15B2
RP9	RPAK4P	24D3
RP10	RPAK4P	24C7 24C8 24C8
RP11	RPAK4P	5B1 5D1
RP12	RPAK4P	24B7 24B8
RP13	RPAK4P	14C1
RP14	RPAK4P	24C7 24D7 24D8
RP15	RPAK4P	14B4 14B4 14B5 14B5
RP16	RPAK4P	14A4 14B4 14B5 14B5
RP17	RPAK4P	14C1 14D1
RP18	RPAK4P	13A7 13B7
RP19	RPAK4P	13A7 13B7
RP20	RPAK4P	13C1 13D1
RP21	RPAK4P	13B1 13C1
RP22	RPAK4P	9C2 9D2 9D2
RP23	RPAK4P	13B1 13C1
RP24	RPAK4P	9C2 9D2 9D2
RP25	RPAK4P	9C2 9C2 9D2 15A8
RP26	RPAK4P	10B4 10B5 10B5
RP27	RPAK4P	10A4 10A5 10A5
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RP31	RPAK4P	10D4 10D4 10D5 10D5
RP32	RPAK4P	10D4 10D4 10D5 10D5
RP33	RPAK4P	10C4 10C4 10C5 10C5
RP34	RPAK4P	10C4 10C4 10C5 10C5
RP35	RPAK4P	28A8
RP36	RPAK4P	28B8
RP37	RPAK4P	26B8
RP38	RPAK10P2C	18A8
RP39	RPAK4P	26A7
RP40	RPAK4P	15B8 15C1 15C2
RP41	RPAK4P	15C8
RP42	RPAK4P	15B8 15C8 15D1
RP43	RPAK4P	24C7 24C8 24D8
RP44	RPAK4P	24C7 24C8 24D7
RP45	RPAK4P	8D8
RP46	RPAK4P	8D8
RP47	RPAK4P	15B8 15C8
RP48	RPAK4P	23B1
RP49	RPAK4P	30C1 30C1 30D1
RP50	RPAK10P2C	23B5
RP51	RPAK4P	23B1 23C3 26C8
RP52	RPAK4P	30C8 30D8
RP53	RPAK10P2C	23B5
RP54	RPAK4P	26B3 26B4 26D2
RP55	RPAK4P	21B3
RP56	RPAK4P	21B3
RP57	RPAK4P	21B1
RP58	RPAK4P	21B1
RP59	RPAK4P	25C5 25C5 25D5 25D5
SH1	SHLD_3P_EMI	4D2
SP1	SPKR_CLIP_P84	4C3
SP2	SPKR_CLIP_P84	4C3
SP3	SPKR_CLIP_P84	4C2
SP4	SPKR_CLIP_P84	4C2
SP5	SPKR_CLIP_P84	4C2
SP6	SPKR_CLIP_P84	4C2
T1	XFR_ENET_1000BT	27B3
U1	SN74AUC1G04	7A7
U2	SN74AUC1G08	23A3
U3	SN74AUC1G08	23B3
U4	LTC3411	35A5
U5	TRA_SI3447DV	35A2
U6	SRAM_DDR_128KX36	8D2
U7	SRAM_DDR_128KX36	8D5
U8	LTC1761	20A7
U9	TRA_SI3447DV	35C1
U10	VREG_LT1962	15D6
U11	CBTV4020	11C2
U12	CBTV4020	11C4
U13	CBTV4020	11C5
U14	CBTV4020	11C7
U16	COMPARATOR_LMC7211	31C7
U17	FEPR_1MX8	10C2
U18	LTC1625	32C5
U19	LTC1778	20B7
U20	PWR_CNTRL_TPS2211	18D3
U21	MAX1717	34C5
U22	COMPARATOR_LMC7211	32C7
U23	MAX1715	35C4
U24	AMP_MAX4172	31D5
U25	VREG_LP2951	32B3
U26	PCI1510GGU	18C5
U27	LTC3707	33C4
U28	TSB81BA3	28B6
U29	VREG_LP2951	32B5
U30	MAX1772	31B5
U31	VREG_LM2594	28D7
U32	7432	22A2 30A7 30A8
U33	LTC1761	28D8
U34	VREG_LT1962	28C8
U35	COMPARATOR_LMC7211	31A6
U36	FEPR_256KX8_ST72264_BGA	23D5
U37	EEPROM_16KX8_M24128B	23D3
U38	MAX6804	30B7
U39	M16C62	30D5
U40	OPAMP_MAX4236EUTT	23D7
U41	PI3B3257	34D4
U42	APOLLO483	5C5 6D5 6D7
U43	MAP31_612P	19D1 19D3 19D6 20C3 21D5
U44	INTREPID	9D4 10D7 13D3 13D7 14D4 14D8 15C4 16D4 16D7
U45	COMPARATOR_LMC7211	22C2
U46	CLK_GEN_CY25811	21A4
U47	VREG_LT1962	6B3
U48	ADM1031	25B4
U49	TRANSCEIVER_88E1111	27C6
U50	MAX1916	23A5
U51	LTC3405	27D4
U52	UPD720101_FBGA	26C6
U53	COMPARATOR_LMC7211	30A3
U54	OPAMP_LMC7111	31D3
U55	SIL1162	21C2
U56	CLK_GEN_CY28512	15B6
U1600	VREG_LT1962	16B2
XW1	SHORT	35A4
XW2	SHORT	34B1
XW4	SHORT	20B7
XW6	SHORT	32B5
XW7	SHORT	34B4
XW8	SHORT	35B6
XW9	SHORT	34B4
XW11	SHORT	33B4
XW14	SHORT	22B8
XW15	SHORT	22A8
XW17	SHORT	25C7
XW18	SHORT	34C1
XW20	SHORT	31B3
Y1	CRYSTAL	15A5
Y2	CRYSTAL_4PIN	21B4
Y3	CRYSTAL	27A7
Y4	CRYSTAL	23C6
Y5	CRYSTAL	30B7
Y6	CRYSTAL_4PIN	30B3
Y7	CRYSTAL	26D4
ZT1	MTGHOLE	4D3
ZT3	MTGHOLE	4D4
ZT4	MTGHOLE	4C4
ZT5	MTGHOLE	4D4
ZT6	MTGHOLE	4D4
ZT7	MTGHOLE	4D4
ZT8	MTGHOLE	4C4
ZT14	MTGHOLE	4D3
ZT18	HOLE_VIA	4B4
ZT19	HOLE_VIA	4B4
ZT20	HOLE_VIA	4B4
ZT21	HOLE_VIA	4B4
ZT22	HOLE_VIA	4B4
ZT23	HOLE_VIA	4B4
ZT24	HOLE_VIA	4B4
ZT25	HOLE_VIA	4B4
ZT26	HOLE_VIA	4B4
ZT27	HOLE_VIA	4A4
ZT28	HOLE_VIA	4A4
ZT29	HOLE_VIA	4A4
ZT30	HOLE_VIA	4A4
ZT31	HOLE_VIA	4A4
ZT32	HOLE_VIA	4A4
ZT33	HOLE_VIA	4B4
ZT34	HOLE_VIA	4B4
ZT35	HOLE_VIA	4B4
ZT36	HOLE_VIA	4B4
ZT37	HOLE_VIA	4B4
ZT38	HOLE_VIA	4B4
ZT39	HOLE_VIA	4B4
ZT40	HOLE_VIA	4B4
ZT41	HOLE_VIA	4B4
ZT42	HOLE_VIA	4A4
ZT43	HOLE_VIA	4A4
ZT44	HOLE_VIA	4A4
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ZT46	HOLE_VIA	4A4
ZT47	HOLE_VIA	4A4
ZT48	HOLE_VIA	4B3
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ZT100	HOLE_VIA	4A3
ZT101	HOLE_VIA	4B2
ZT102	HOLE_VIA	4B2
ZT103	HOLE_VIA	4B2
ZT104	HOLE_VIA	4B2
ZT105	HOLE_VIA	4B2
ZT106	HOLE_VIA	4B2
ZT107	HOLE_VIA	4B2
ZT108	HOLE_VIA	4B2
ZT109	HOLE_VIA	4B2
ZT110	HOLE_VIA	4A2
ZT111	HOLE_VIA	4A2
ZT112	HOLE_VIA	4A2
ZT114	HOLE_VIA	4A2
ZT115	HOLE_VIA	4A2
ZT116	HOLE_VIA	4A2

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