1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

DRAWING REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
B		322174	PRODUCTION RELEASED	04/02/04?	

SCHEM,MLB,PB15

Fri Apr 2 16:49:30 2004

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20	M11 LVDS/TMDS/GPIO & GPU VCORE
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23	KBD,TPAD,HALL EFFECT,PWR BUTTON,LMU/SENSOR
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BOM OPTIONS (IN COMMON PARTS)

STUFF	NO STUFF
1_8V_MAXBUS	1_5V_MAXBUS
NO_SSCG	SSCG
5V_HD_LOGIC	3V_HD_LOGIC
NO_BBANG	BBANG
INT_2_5V_COLD	INT_2_5V_HOT
ATI_MEMIO_HI	ATI_MEMIO_LO
SOFT_MODEM	USB_MODEM
GPU_PWRMSR	EXT_TMDS
GPU_SS	
VGA_BUFFER_RES	
INT_TMDS	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6570	1	SCHEM,MLB,PB15	SCH1	
820-1600	1	PCBF,MLB,PB15	PCB1	

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES °
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

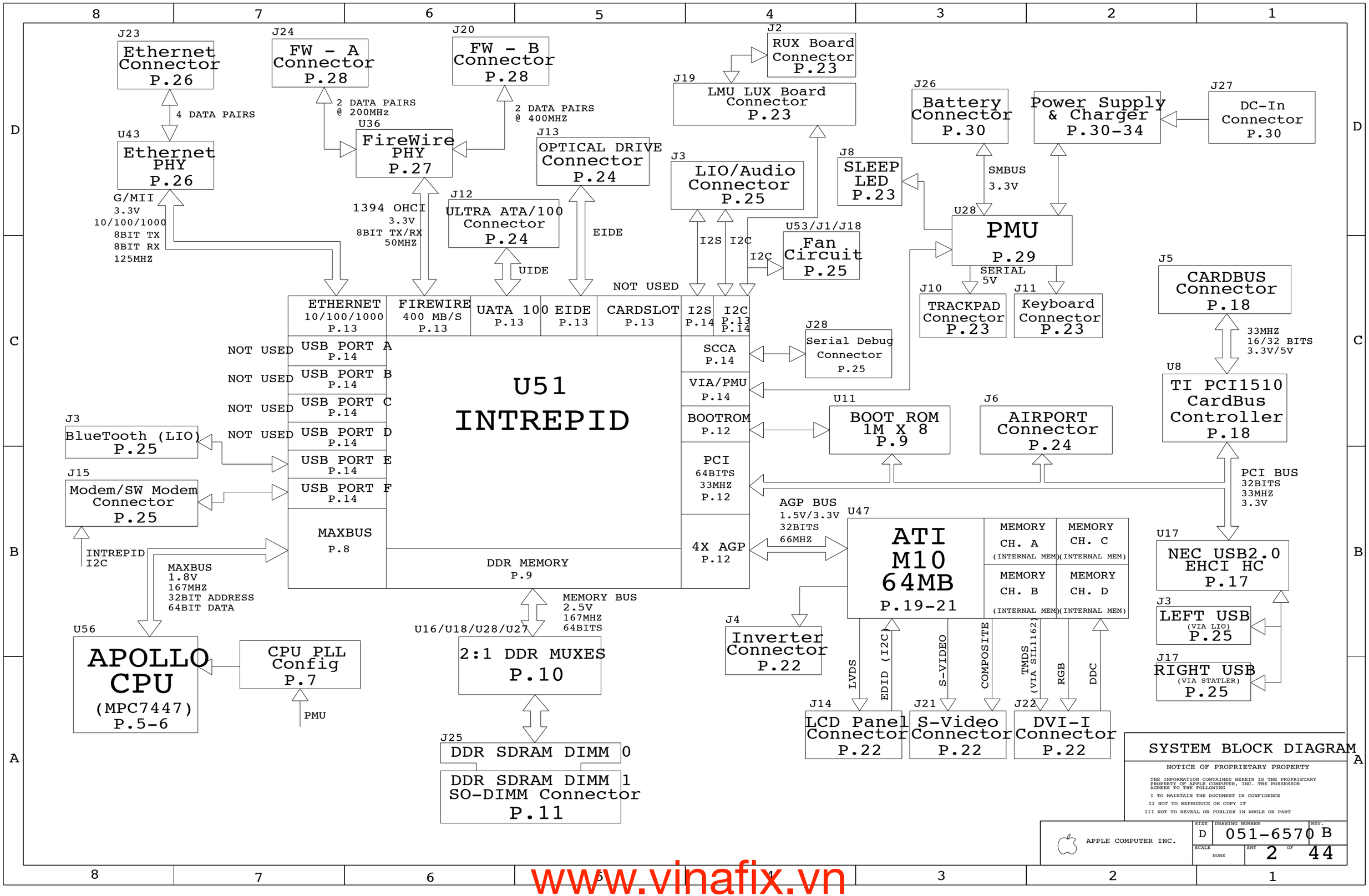
DRAFTER / DESIGN CK /
ENG APPD / MFG APPD /
QA APPD / DESIGNER /
RELEASE / SCALE NONE
MATERIAL/FINISH NOTED AS APPLICABLE
SIZE D

Apple Computer Inc.

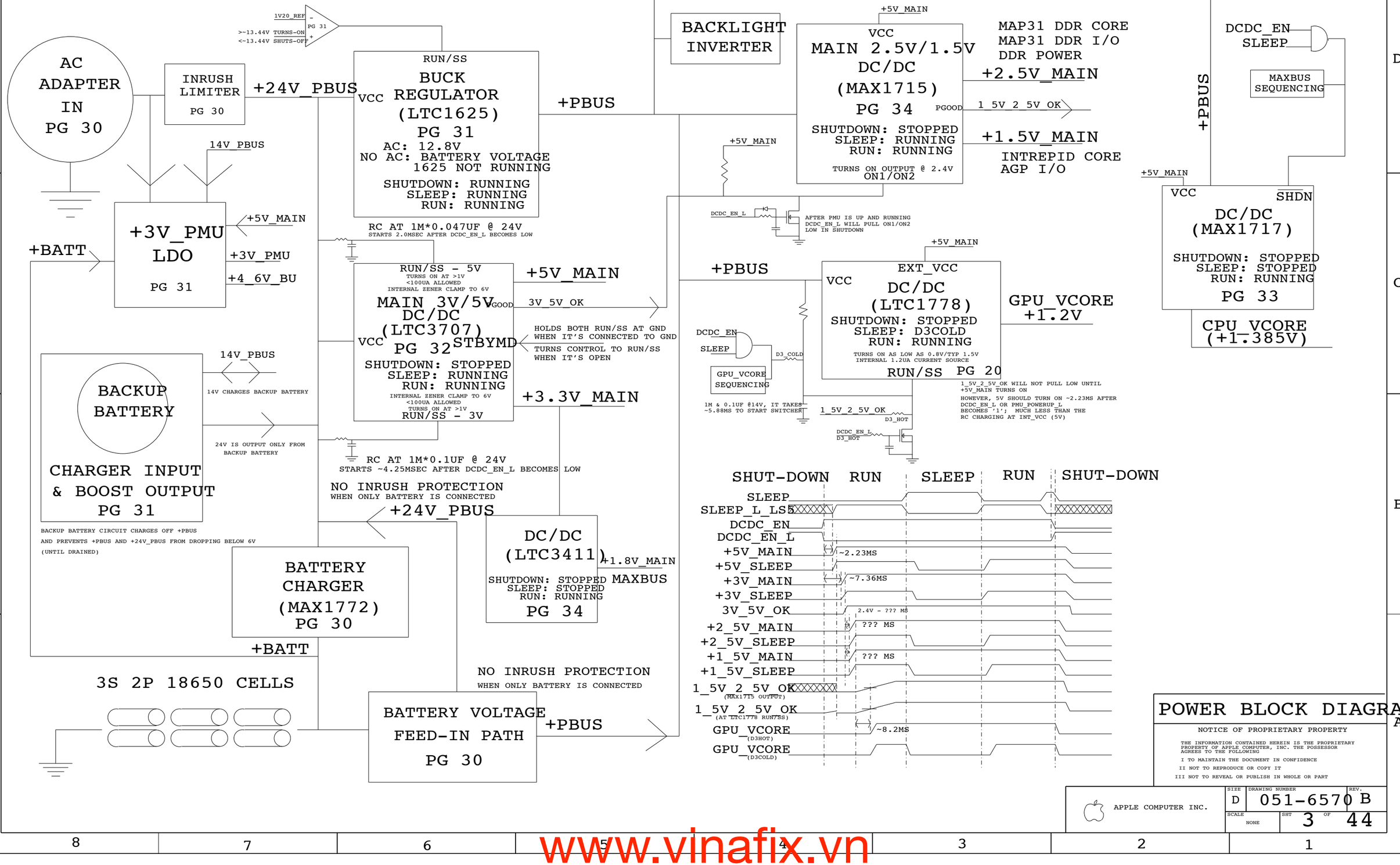
TITLE
SCHEM,MLB,PB15

DRAWING NUMBER 051-6570 REV. B

SHT 1 OF 44



POWER SYSTEM ARCHITECTURE



POWER BLOCK DIAGRAM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	B
SCALE: NONE	SHT 3 OF 44	

PCB SPECS

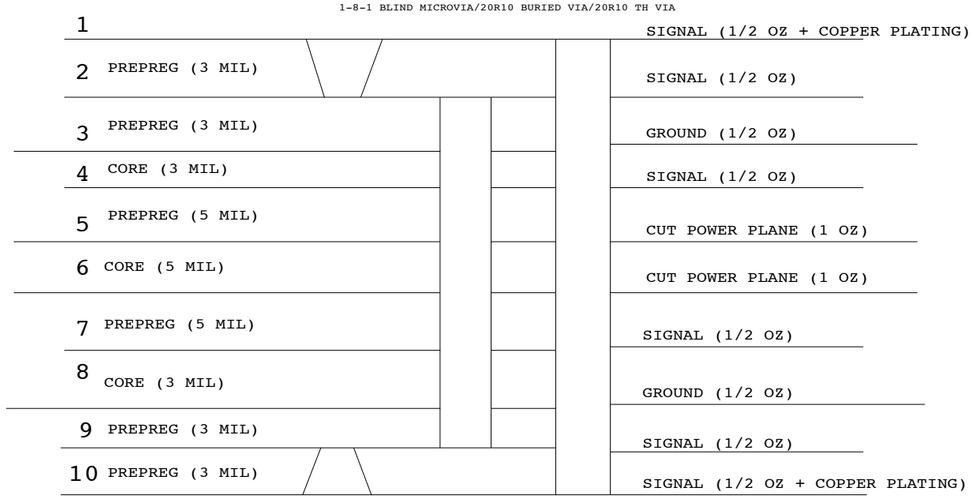
THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 10
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

1-8-1 BLIND MICROVIA/20R10 BURIED VIA/20R10 TH VIA



BOARD HOLES

CHASSIS MOUNTS

ASICS HEATSINK MOUNTS

ZT7 HOLE-VIA-20R10LEFT CPU
ZT21 HOLE-VIA-20R10UPPER RT GPU
ZT58 HOLE-VIA-20R10LWR CPU
ZT59 HOLE-VIA-20R10LWR RT GPU

I/O AREA

ZT85 HOLE-VIA-20R10 DVI — CHGND2
ZT86 HOLE-VIA-20R101394 DVI — CHGND1
ZT16 HOLE-VIA-20R10 BATT. CHRGR — CHGND5

INVERTER

SH1 OG-503040 SHLD-SM — CHGND3

MECH. HOLES

ZT74 HOLE-VIA-20R10
ZT36 HOLE-VIA-20R10 — ZT301 SPN NO_TEST=TRUE
ZT23 HOLE-VIA-20R10 — ZT302 SPN NO_TEST=TRUE
ZT42 HOLE-VIA-20R10 — ZT10 SPN NO_TEST=TRUE

GROUND VIAS

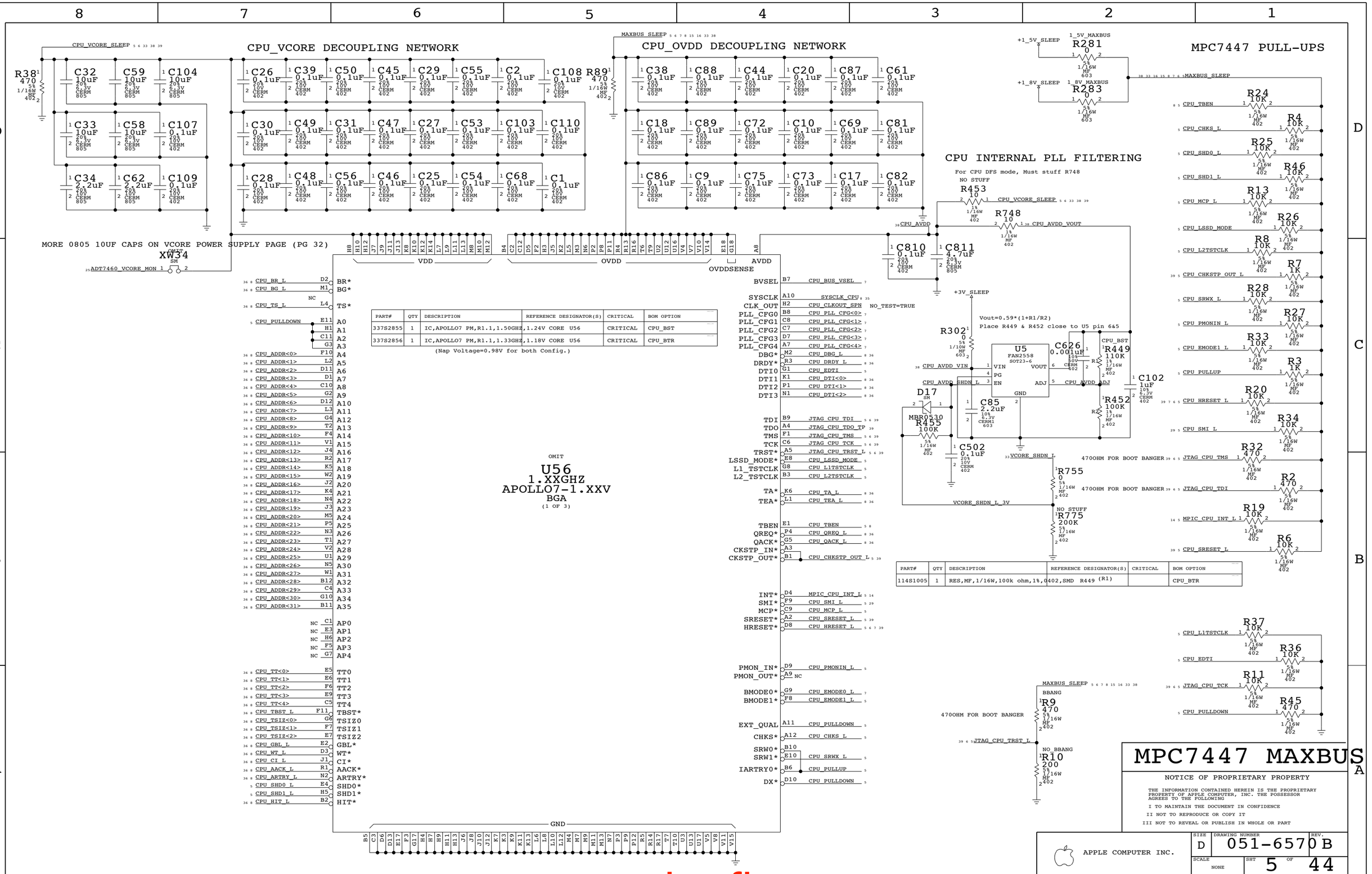
ZT76 ZT28 ZT72 ZT69 ZT68 ZT64 ZT61 ZT38 ZT39 ZT40 ZT41 ZT46 ZT71 ZT78 ZT80
ZT50 ZT51 ZT52 ZT53 ZT57 ZT60 ZT82 ZT22 ZT17 ZT35 ZT45 ZT79 ZT81 ZT83 ZT49
ZT48 ZT47 ZT54 ZT55 ZT56 ZT84 ZT5 ZT15 ZT44 ZT4 ZT8 ZT6 ZT32 ZT3 ZT10
ZT11 ZT34 ZT20 ZT43 ZT70 ZT2 ZT9 ZT75 ZT73 ZT63 ZT77 ZT66 ZT62 ZT65 ZT13
ZT25 ZT19 ZT24 ZT67 ZT37 ZT29 ZT31 ZT1 ZT14 ZT12 ZT27 ZT26 ZT30 ZT33 ZT18

(all HOLE-VIA-20R10)

BOARD INFORMATION

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	B
SCALE: NONE	SHT 4 OF 44	

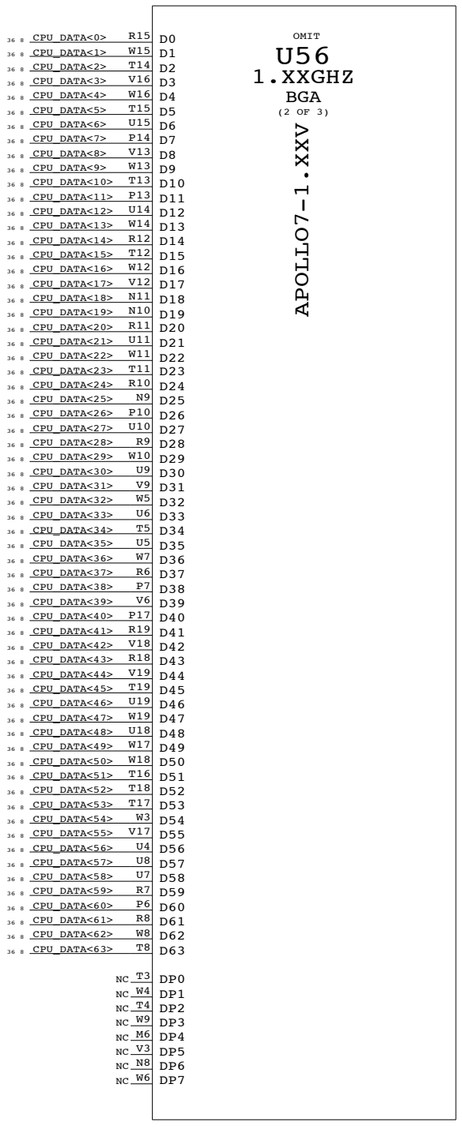


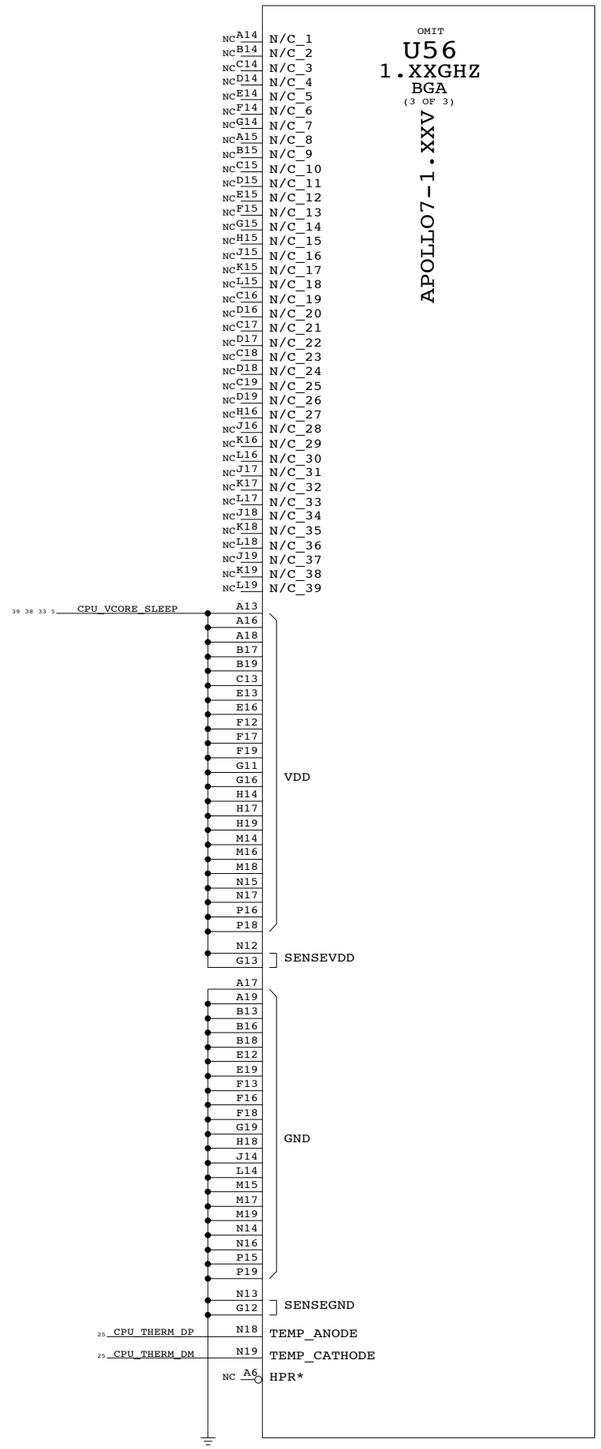
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S2855	1	IC,APOLLO7 PM,R1.1,1.50GHZ,1.24V CORE U56		CRITICAL	CPU_BST
337S2856	1	IC,APOLLO7 PM,R1.1,1.33GHZ,1.18V CORE U56		CRITICAL	CPU_BTR

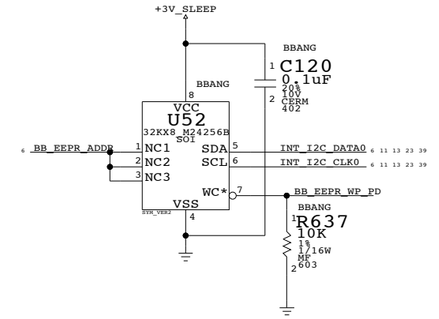
(Nap Voltage=0.98V for both Config.)

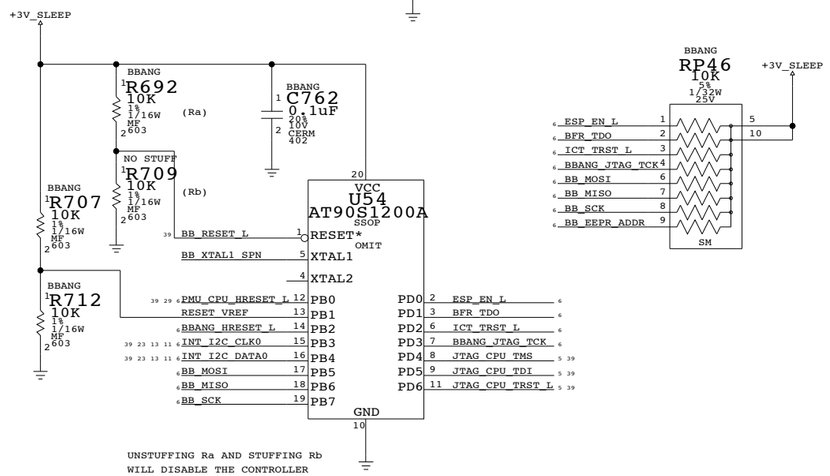
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S1005	1	RES,MF,1/16W,100k ohm,1%,0402,SMD	R449 (R1)		CPU_BTR

BOOT BANGER - TWEAK PROCESSOR BITS AFTER POWER-ON



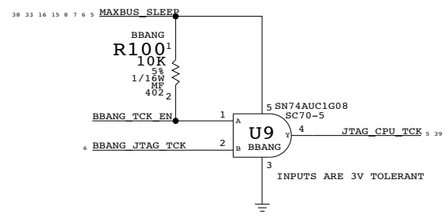


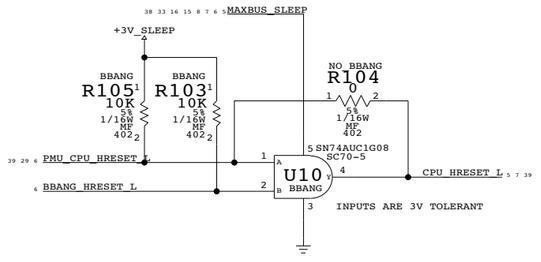




UNSTUFFING Ra AND STUFFING Rb
WILL DISABLE THE CONTROLLER

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1135	1	000-6240-TW-GT4_BBANGER MCU,PROGRAMMED W/ BBANGER	U54	BBANG





MPC7447/BBANG

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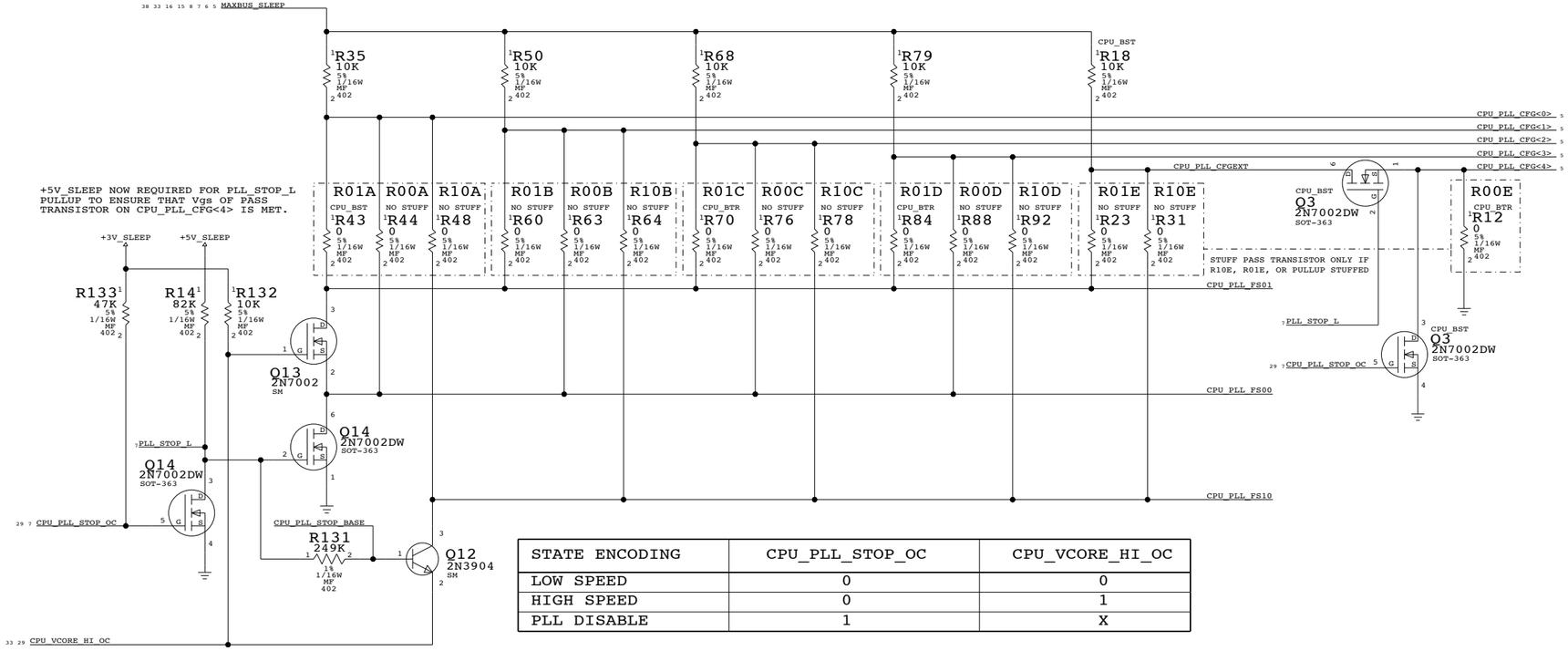
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	B
SCALE: NONE	SHT 6 OF 44	

CPU PLL CONFIG CIRCUITRY



STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

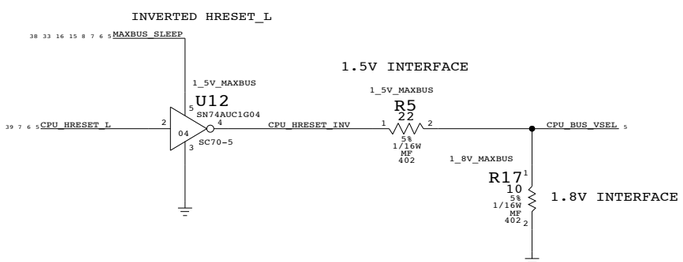
CPU FREQUENCY CONFIGURATION

APOLLO 7

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ (MHZ)	133MHZ (MHZ)	CPU_PLL_CFG 4 0123 E ABCD	HEX
0.0X	PLL OFF		0 1111	0F
1.0X	PLL BYPASS		0 0011	03
2.0X	333	267	0 0100	04
3.0X	500	400	0 1000	08
4.0X	667	533	0 1010	0A
5.0X	833	667	0 1011	0B
5.5X	917	733	0 1001	09
6.0X	1000	800	0 1101	0D
6.5X	1083	867	0 0101	05
7.0X	1167	933	0 0010	02
7.5X	1250	1000	0 0001	01
8.0X	1333	1067	0 1100	0C
8.5X	1417	1133	0 0110	06
9.0X	1500	1200	1 0111	17
9.5X	1583	1267	0 0111	07
10.0X	1667	1333	1 1010	1A
10.5X	1750	1400	1 1000	18
11.0X	1833	1467	1 1001	19
11.5X	1917	1533	0 0000	00
12.0X	2000	1600	1 1011	1B
12.5X	2083	1667	1 1111	1F
13.0X	2167	1733	1 0101	15
13.5X	2250	1800	0 1110	0E
14.0X	2333	1867	1 1100	1C
15.0X	2500	2000	1 0001	11
16.0X	2667	2133	1 1101	1D
17.0X	2833	2267	1 0000	10
18.0X	3000	2400	1 0010	12
20.0X	3333	2667	1 0011	13
21.0X	3500	2800	1 0100	14
24.0X	4000	3200	1 0110	16
28.0X	4667	3733	1 1110	1E

CPU CONFIGURATION

MAXBUS VSEL



DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L NEED TO CHARACTERIZE

BUSTYPE SELECT

APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

CPU CONFIGURATION

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6570 | REV. B

SCALE NONE | SHT 7 OF 44

INTREPID BOOT STRAPS

BIT 32 TO 39

MAXBUS_SLEEP

NO STUFF R640	NO STUFF R639	NO STUFF R638	R666				
CPU_DATA<32>	CPU_DATA<33>	CPU_DATA<34>	CPU_DATA<35>	CPU_DATA<36>	CPU_DATA<37>	CPU_DATA<38>	CPU_DATA<39>
R622	R619	R618	NO STUFF R653	R621	R620	R652	R650
DDR_TPDMode Enable_h 0: DDR1 Mode 1: DDR2 Mode (JTAG)	Early Wakeclk_En_h 0: Early Wakeclk Active	DDR_TPDen_Pol 0: Active High 1: Active Low	ExtPLL SPwn_Pol 0: Active High 1: Active Low	Spare	Spare	Spare	Spare

10K 5% 1/16W MF 402

BIT 40 TO 47

MAXBUS_SLEEP

NO STUFF R641	SSCG R665	NO STUFF R664	NO_SSCG R693	NO STUFF R694	NO STUFF R699		
CPU_DATA<40>	CPU_DATA<41>	CPU_DATA<42>	CPU_DATA<43>	CPU_DATA<44>	CPU_DATA<45>	CPU_DATA<46>	CPU_DATA<47>
R648	R677	R623	NO_SSCG R651	R649	SSCG R678	R679	R684
Spare	Spare	BIT2	BIT1	BIT0	Internal_SPDEN 0: Internal 1: Active	PCI1 Source (Clock spread) 0: PLL2 1: PLL4	PCI0 Source Clock (no spread) 0: PLL2 1: PLL4 (for spread)

10K 5% 1/16W MF 402

PLL4MODESEL_NXT[2:0]
000: 166.4MHz (2.5X)
001: 149.76MHz
010: 133.12MHZ (2.0X)
011: 99.84MHz (1.5X)
100: 83.20MHZ

MODE A (2.5X) IS FOR STATIC OPERATION
MODE C (2.0X) IS FOR CLOCK SLEW OPERATION

BIT 48 TO 55

MAXBUS_SLEEP

SSCG R696	SSCG R695	NO STUFF R667	NO STUFF R668	NO STUFF R643	NO STUFF R642	R698	
CPU_DATA<48>	CPU_DATA<49>	CPU_DATA<50>	CPU_DATA<51>	CPU_DATA<52>	CPU_DATA<53>	CPU_DATA<54>	CPU_DATA<55>
NO_SSCG R681	NO_SSCG R680	NO STUFF R654	R655	R625	R624	NO STUFF R683	R626
BUF_REF_CLK_OUTEnable_h 0: Active 1: Active	SelPLL4Extsrc 0: PLL4 1: External source	OBSOLETE (Should remain high) En_PCI_ROM_P 0: Boot ROM on PCI (CardSlot 1) 1: Boot ROM on FLT	TI 1394b work around NO TI PHY 1394b workaround	BIT2	BIT1	BIT0	Spare

10K 5% 1/16W MF 402

MaxBus output impedance
111: 28.6 ohm
011: 33.3 ohm
101: 40 ohm
001: 50 ohm
110: 66.6 ohm
010: 100 ohm
100: 200 ohm
000: 200 ohm

R159

+1_5V_INTREPID_PLL — 4.7 5% 1/16W MF 402 — +1_5V_INTREPID_PLL7

C187 0.22uF 20% 6.3V CERM 402

H26 VDD15A_7 (PLL6)

U51 INTREPID-REV2.1 BGA

(1 OF 9) CRITCAL

CPU_BR_L	E29	BR	INPUT
CPU_BG_L	E26	BG	NO BUS KEEPER
CPU_TS_L	B27	TS	NO BUS KEEPER
CPU_ADDR<0>	D24	A_0	
CPU_ADDR<1>	D25	A_1	
CPU_ADDR<2>	A27	A_2	
CPU_ADDR<3>	E24	A_3	
CPU_ADDR<4>	G23	A_4	
CPU_ADDR<5>	B26	A_5	
CPU_ADDR<6>	A26	A_6	
CPU_ADDR<7>	D23	A_7	
CPU_ADDR<8>	A25	A_8	
CPU_ADDR<9>	E23	A_9	
CPU_ADDR<10>	J22	A_10	
CPU_ADDR<11>	B25	A_11	
CPU_ADDR<12>	H22	A_12	
CPU_ADDR<13>	G22	A_13	
CPU_ADDR<14>	D22	A_14	
CPU_ADDR<15>	B24	A_15	
CPU_ADDR<16>	B23	A_16	
CPU_ADDR<17>	E22	A_17	
CPU_ADDR<18>	J21	A_18	
CPU_ADDR<19>	G21	A_19	
CPU_ADDR<20>	E21	A_20	
CPU_ADDR<21>	A24	A_21	
CPU_ADDR<22>	D21	A_22	
CPU_ADDR<23>	A23	A_23	
CPU_ADDR<24>	H20	A_24	
CPU_ADDR<25>	B22	A_25	
CPU_ADDR<26>	H21	A_26	
CPU_ADDR<27>	A22	A_27	
CPU_ADDR<28>	E20	A_28	
CPU_ADDR<29>	B21	A_29	
CPU_ADDR<30>	D20	A_30	
CPU_ADDR<31>	A21	A_31	
CPU_CI_L	G26	CI	
CPU_GBL_L	A29	GBL	
CPU_TBST_L	A28	TBST	
CPU_TSIZ<0>	G24	TSIZ_0	
CPU_TSIZ<1>	H24	TSIZ_1	
CPU_TSIZ<2>	D26	TSIZ_2	
CPU_TT<0>	E25	TT_0	
CPU_TT<1>	G25	TT_1	
CPU_TT<2>	B28	TT_2	
CPU_TT<3>	D27	TT_3	
CPU_TT<4>	J25	TT_4	
CPU_WT_L	D28	WT	
CPU_AACK_L	B29	AACK	NO BUS KEEPER - PU
CPU_ARTRY_L	H23	ARTRY	NO BUS KEEPER - PU
CPU_HIT_L	B31	HIT	INPUT - PU
CPU_QREQ_L	A32	QREQ	INPUT - PD
CPU_QACK_L	G27	QACK	NO BUS KEEPER - ?
INT_SUSPEND_REQ_L	AK9	SUSPENDREQ	
INT_SUSPEND_ACK_L	AM8	SUSPENDACK	

Vin = Intrepid Vcore (1.5V)
Vout = MaxBus rail (1.8V)

CPU_FB_IN			
CPU_FB_OUT		NO BUS KEEPER - PU	DBG
ANALYZER_CLK			
		INPUT - PU	DRDY
STOPCPUCLK			
		NO BUS KEEPER - ?	DTI_0
ACS_REF		NO BUS KEEPER - ?	DTI_1
		NO BUS KEEPER - ?	DTI_2
CPU_CLK		NO BUS KEEPER - PU	TA
		NO BUS KEEPER - PU	TEA
INTREPID OUTPUTS HIGH BY DEFAULT			
TBEN		VSSA_7 (PLL6)	
NO BUS KEEPER - PU			

INT_CPUFB_IN	J24		
INT_CPUFB_OUT	H16		
SYSCLK_LA_TP	G8		
CPU_CLK_EN	AH9		
INTREPID_ACS_REF	H13		
SYSCLK_CPU_UF	J15		
CPU_TBEN	A31		

H25

MAXBUS INTERFACE

D_0	D10	CPU_DATA<0>	6 36
D_1	G12	CPU_DATA<1>	6 36
D_2	E11	CPU_DATA<2>	6 36
D_3	H11	CPU_DATA<3>	6 36
D_4	B9	CPU_DATA<4>	6 36
D_5	B8	CPU_DATA<5>	6 36
D_6	A9	CPU_DATA<6>	6 36
D_7	A8	CPU_DATA<7>	6 36
D_8	E12	CPU_DATA<8>	6 36
D_9	D11	CPU_DATA<9>	6 36
D_10	B10	CPU_DATA<10>	6 36
D_11	J13	CPU_DATA<11>	6 36
D_12	A10	CPU_DATA<12>	6 36
D_13	D12	CPU_DATA<13>	6 36
D_14	E13	CPU_DATA<14>	6 36
D_15	G13	CPU_DATA<15>	6 36
D_16	B11	CPU_DATA<16>	6 36
D_17	D13	CPU_DATA<17>	6 36
D_18	A11	CPU_DATA<18>	6 36
D_19	G14	CPU_DATA<19>	6 36
D_20	H14	CPU_DATA<20>	6 36
D_21	E14	CPU_DATA<21>	6 36
D_22	B12	CPU_DATA<22>	6 36
D_23	G15	CPU_DATA<23>	6 36
D_24	B13	CPU_DATA<24>	6 36
D_25	H15	CPU_DATA<25>	6 36
D_26	D14	CPU_DATA<26>	6 36
D_27	B14	CPU_DATA<27>	6 36
D_28	A12	CPU_DATA<28>	6 36
D_29	G16	CPU_DATA<29>	6 36
D_30	E15	CPU_DATA<30>	6 36
D_31	J16	CPU_DATA<31>	6 36
D_32	D15	CPU_DATA<32>	6 8 36
D_33	A14	CPU_DATA<33>	6 8 36
D_34	A13	CPU_DATA<34>	6 8 36
D_35	D16	CPU_DATA<35>	6 8 36
D_36	E16	CPU_DATA<36>	6 8 36
D_37	G17	CPU_DATA<37>	6 8 36
D_38	B15	CPU_DATA<38>	6 8 36
D_39	H17	CPU_DATA<39>	6 8 36
D_40	A15	CPU_DATA<40>	6 8 36
D_41	B16	CPU_DATA<41>	6 8 36
D_42	E17	CPU_DATA<42>	6 8 36
D_43	A16	CPU_DATA<43>	6 8 36
D_44	J18	CPU_DATA<44>	6 8 36
D_45	H18	CPU_DATA<45>	6 8 36
D_46	D17	CPU_DATA<46>	6 8 36
D_47	G18	CPU_DATA<47>	6 8 36
D_48	A17	CPU_DATA<48>	6 8 36
D_49	B17	CPU_DATA<49>	6 8 36
D_50	E18	CPU_DATA<50>	6 8 36
D_51	B18	CPU_DATA<51>	6 8 36
D_52	D18	CPU_DATA<52>	6 8 36
D_53	A18	CPU_DATA<53>	6 8 36
D_54	A19	CPU_DATA<54>	6 8 36
D_55	H19	CPU_DATA<55>	6 8 36
D_56	B19	CPU_DATA<56>	6 8 36
D_57	J19	CPU_DATA<57>	6 8 36
D_58	A20	CPU_DATA<58>	6 8 36
D_59	D19	CPU_DATA<59>	6 8 36
D_60	E19	CPU_DATA<60>	6 8 36
D_61	G19	CPU_DATA<61>	6 8 36
D_62	B20	CPU_DATA<62>	6 8 36
D_63	G20	CPU_DATA<63>	6 8 36
DBG	A30	CPU_DBG_L	5 8 36
DRDY	G28	CPU_DRDY_L	5 8 36
DTI_0	K25	CPU_DTI<0>	5 36
DTI_1	D29	CPU_DTI<1>	5 36
DTI_2	B30	CPU_DTI<2>	5 36
TA	E27	CPU_TA_L	5 8 36
TEA	E28	CPU_TEA_L	5 8 36

FB BUFFER HAS 50 OHM OUTPUT IMPEDANCE

R169 511 1% 1/16W MF 402

R168 0 5% 1/16W MF 402 — SYSCLK_CPU

R161 1K 1% 1/16W MF 402

SHORT = 1" SHORTER THAN MATCHED LENGTH
LONG = 1" LONGER THAN MATCHED LENGTH

INT_CPUFB_OUT2	INT_CPUFB_OUT_SHORT	INT_CPUFB_OUT_NORM	INT_CPUFB_LONG	
R155 0	R140 0	R128 0		
	NO STUFF R146 0	R141 0	NO STUFF R136 0	
INT_CPUFB_IN	R147 0	INT_CPUFB_IN_NORM		

5% 1/16W MF 402

THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:
1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
2/ D46 - SELPCI1SPREADCLK - SLEEP/WAKE CYCLE REQUIRED
3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT

IF A STRAP IS NOT LISTED, THEN
IT CANNOT BE CHANGED BY SOFTWARE

MAXBUS PULL-UPS

MAXBUS_SLEEP

RP3 10K	CPU_TS_L						
RP3 10K	CPU_TA_L						
RP3 10K	CPU_ARTRY_L						
RP2 10K	CPU_BR_L						
R152 10K	CPU_HIT_L						
RP2 10K	CPU_DRDY_L						
RP2 10K	CPU_TEA_L						
RP2 10K	CPU_AACK_L						
R150 10K	CPU_DBG_L						
RP3 10K	CPU_BG_L						
R151 10K	CPU_QREQ_L						

5% 1/16W SM1 (MF 402 for R151)

INTREPID BOOT STRAPS

BIT 56 TO 63

MAXBUS_SLEEP

NO STUFF R669	NO STUFF R645	NO STUFF R697	NO STUFF R670	R644	NO STUFF R646		
CPU_DATA<56>	CPU_DATA<57>	CPU_DATA<58>	CPU_DATA<59>	CPU_DATA<60>	CPU_DATA<61>	CPU_DATA<62>	CPU_DATA<63>
R656	R685	R657	R628	R682	R658	NO STUFF R627	R629
Spare	Spare	OBSOLETE Reserved, Req PCI1 0: 0-15V / 3.3 1: GPIO8	PCI1_REQ#_L / PCI1_GNT3_L 0: REQ#/GNT# 1: GPIO7	PCI1_REQ1_L / PCI1_GNT1_L 0: REQ#/GNT# 1: GPIO6	PCI1_REQ0_L / PCI1_GNT0_L 0: REQ#/GNT# 1: GPIO5	Firewire PHY interface 0: Legacy Interface 1: B-Mode	Strap for Bus Mode 0: 66x Bus (G3) 1: 33x Bus

10K 5% 1/16W MF 402

Intrepid MaxBus

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	B
SCALE: NONE	SHT 8 OF 44	

SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

PINS ARE SWAPABLE FOR RPAKS

1MB BOOT ROM

U51
INTREPID-REV2.1
BGA
(2 OF 9)
CRITICAL

DDR MEMORY INTERFACE

MEM_DATA<0> AK32 — DDR_DATA_0
MEM_DATA<1> AK33 — DDR_DATA_1
MEM_DATA<2> AK31 — DDR_DATA_2
MEM_DATA<3> AK35 — DDR_DATA_3
MEM_DATA<4> AK36 — DDR_DATA_4
MEM_DATA<5> AJ32 — DDR_DATA_5
MEM_DATA<6> AJ35 — DDR_DATA_6
MEM_DATA<7> AJ36 — DDR_DATA_7
MEM_DATA<8> AG33 — DDR_DATA_8
MEM_DATA<9> AG35 — DDR_DATA_9
MEM_DATA<10> AH35 — DDR_DATA_10
MEM_DATA<11> AG36 — DDR_DATA_11
MEM_DATA<12> AH36 — DDR_DATA_12
MEM_DATA<13> AH32 — DDR_DATA_13
MEM_DATA<14> AG32 — DDR_DATA_14
MEM_DATA<15> AG31 — DDR_DATA_15
MEM_DATA<16> AE32 — DDR_DATA_16
MEM_DATA<17> AF35 — DDR_DATA_17
MEM_DATA<18> AF36 — DDR_DATA_18
MEM_DATA<19> AE36 — DDR_DATA_19
MEM_DATA<20> AE35 — DDR_DATA_20
MEM_DATA<21> AE33 — DDR_DATA_21
MEM_DATA<22> AD36 — DDR_DATA_22
MEM_DATA<23> AD35 — DDR_DATA_23
MEM_DATA<24> AA36 — DDR_DATA_24
MEM_DATA<25> AA35 — DDR_DATA_25
MEM_DATA<26> AA33 — DDR_DATA_26
MEM_DATA<27> AB36 — DDR_DATA_27
MEM_DATA<28> AB35 — DDR_DATA_28
MEM_DATA<29> AC36 — DDR_DATA_29
MEM_DATA<30> AA32 — DDR_DATA_30
MEM_DATA<31> AB33 — DDR_DATA_31
MEM_DATA<32> V36 — DDR_DATA_32
MEM_DATA<33> U33 — DDR_DATA_33
MEM_DATA<34> U32 — DDR_DATA_34
MEM_DATA<35> V35 — DDR_DATA_35
MEM_DATA<36> T30 — DDR_DATA_36
MEM_DATA<37> U36 — DDR_DATA_37
MEM_DATA<38> U35 — DDR_DATA_38
MEM_DATA<39> T36 — DDR_DATA_39
MEM_DATA<40> P33 — DDR_DATA_40
MEM_DATA<41> R30 — DDR_DATA_41
MEM_DATA<42> P35 — DDR_DATA_42
MEM_DATA<43> P36 — DDR_DATA_43
MEM_DATA<44> R36 — DDR_DATA_44
MEM_DATA<45> R35 — DDR_DATA_45
MEM_DATA<46> R33 — DDR_DATA_46
MEM_DATA<47> R32 — DDR_DATA_47
MEM_DATA<48> N35 — DDR_DATA_48
MEM_DATA<49> M36 — DDR_DATA_49
MEM_DATA<50> L35 — DDR_DATA_50
MEM_DATA<51> M35 — DDR_DATA_51
MEM_DATA<52> M33 — DDR_DATA_52
MEM_DATA<53> L36 — DDR_DATA_53
MEM_DATA<54> N33 — DDR_DATA_54
MEM_DATA<55> M30 — DDR_DATA_55
MEM_DATA<56> J32 — DDR_DATA_56
MEM_DATA<57> J33 — DDR_DATA_57
MEM_DATA<58> J35 — DDR_DATA_58
MEM_DATA<59> K32 — DDR_DATA_59
MEM_DATA<60> K33 — DDR_DATA_60
MEM_DATA<61> J36 — DDR_DATA_61
MEM_DATA<62> K36 — DDR_DATA_62
MEM_DATA<63> K35 — DDR_DATA_63

DDR_A_0 H35 MEM_ADDR<0>
DDR_A_1 G35 MEM_ADDR<1>
DDR_A_2 G36 MEM_ADDR<2>
DDR_A_3 F36 MEM_ADDR<3>
DDR_A_4 F35 MEM_ADDR<4>
DDR_A_5 E35 MEM_ADDR<5>
DDR_A_6 E36 MEM_ADDR<6>
DDR_A_7 G32 MEM_ADDR<7>
DDR_A_8 D36 MEM_ADDR<8>
DDR_A_9 H36 MEM_ADDR<9>
DDR_A_10 G33 MEM_ADDR<10>
DDR_A_11 H33 MEM_ADDR<11>
DDR_A_12 D35 MEM_ADDR<12>
DDR_BA_0 L30 MEM_BA<0>
DDR_BA_1 M29 MEM_BA<1>

DDRCS_0 AN34 MEM_CS_L<0>
DDRCS_1 AN36 MEM_CS_L<1> ‘0’ & ‘1’ GO TO SLOT A
DDRCS_2 AL35 MEM_CS_L<2> ‘2’ & ‘3’ GO TO SLOT B
DDRCS_3 AL33 MEM_CS_L<3>

DDR_DQS_0 AJ31 MEM_DQS<0>
DDR_DQS_1 AH31 MEM_DQS<1>
DDR_DQS_2 AD32 MEM_DQS<2>
DDR_DQS_3 AB30 MEM_DQS<3>
DDR_DQS_4 V30 MEM_DQS<4>
DDR_DQS_5 P32 MEM_DQS<5>
DDR_DQS_6 N29 MEM_DQS<6>
DDR_DQS_7 L32 MEM_DQS<7>

DDR_DM_0 AJ33 MEM_DQM<0>
DDR_DM_1 AH33 MEM_DQM<1>
DDR_DM_2 AD33 MEM_DQM<2>
DDR_DM_3 AC35 MEM_DQM<3>
DDR_DM_4 T35 MEM_DQM<4>
DDR_DM_5 T33 MEM_DQM<5>
DDR_DM_6 N32 MEM_DQM<6>
DDR_DM_7 L33 MEM_DQM<7>

DDRRAS L29 MEM_RAS_L
DDRCAS H32 MEM_CAS_L
DDRWE K30 MEM_WE_L

DDRCKE0 AN35 MEM_CKE<0>
DDRCKE1 AM35 MEM_CKE<1> ‘0’ & ‘1’ GO TO SLOT A
DDRCKE2 AM36 MEM_CKE<2> ‘2’ & ‘3’ GO TO SLOT B
DDRCKE3 AL36 MEM_CKE<3>

AB32 MEM_MUXSEL_MSB_L_TP
DDR_SELHI_0 AE29 MEM_MUXSEL_MSB ‘0’S ARE SAME POLARITY (ACTIVE-LO)
DDR_SELLO_0 N30 MEM_MUXSEL_LSB_L_TP ‘1’S ARE SAME POLARITY (ACTIVE-HI)
DDR_SELLO_1 T32 MEM_MUXSEL_LSB

DDR_MCLK_0_P Y32 SYSCLK_DDRCLK_A0_UF
DDR_MCLK_0_N Y33 SYSCLK_DDRCLK_A0_L_UF
DDR_MCLK_1_P Y35 SYSCLK_DDRCLK_A1_UF
DDR_MCLK_1_N Y36 SYSCLK_DDRCLK_A1_L_UF
DDR_MCLK_2_P Y30 INT_DDRCLK2_P_TP
DDR_MCLK_2_N W30 INT_DDRCLK2_N_TP
DDR_MCLK_3_P W32 SYSCLK_DDRCLK_B0_UF
DDR_MCLK_3_N W33 SYSCLK_DDRCLK_B0_L_UF
DDR_MCLK_4_P V33 SYSCLK_DDRCLK_B1_UF
DDR_MCLK_4_N V32 SYSCLK_DDRCLK_B1_L_UF
DDR_MCLK_5_P W35 INT_DDRCLK5_P_TP
DDR_MCLK_5_N W36 INT_DDRCLK5_N_TP

DDR_REF AA22 — INT_MEM_REF_H 38
DDR_VREF_0 Y22 — INT_MEM_VREF 9 38
DDR_VREF_1 T22

R209 1K 1% 1/16W MF 402 (INT_MEM_VREF to GND)

MEM_VREF

+2_5V_INTREPID 38 16 15 10
R208 10K 1% 1/16W MF 402 (+2_5V_INTREPID to INT_MEM_VREF)
R202 10K 1% 1/16W MF 402 (INT_MEM_VREF to GND)
C249 0.1uF 10% 10V CERM 402 (INT_MEM_VREF to GND)

CLOCKS
SYSCLK_DDRCLK_A1_UF — RP20 22 5% 1/16W SM1 — SYSCLK_DDRCLK_A1 11 35
SYSCLK_DDRCLK_A1_L_UF — RP20 22 5% 1/16W SM1 — SYSCLK_DDRCLK_A1_L 11 35
SYSCLK_DDRCLK_A0_UF — RP22 22 5% 1/16W SM1 — SYSCLK_DDRCLK_A0 11 35
SYSCLK_DDRCLK_A0_L_UF — RP22 22 5% 1/16W SM1 — SYSCLK_DDRCLK_A0_L 11 35
SYSCLK_DDRCLK_B1_UF — RP20 22 5% 1/16W SM1 — SYSCLK_DDRCLK_B1 11 35
SYSCLK_DDRCLK_B1_L_UF — RP20 22 5% 1/16W SM1 — SYSCLK_DDRCLK_B1_L 11 35
SYSCLK_DDRCLK_B0_UF — RP22 22 5% 1/16W SM1 — SYSCLK_DDRCLK_B0 11 35
SYSCLK_DDRCLK_B0_L_UF — RP22 22 5% 1/16W SM1 — SYSCLK_DDRCLK_B0_L 11 35

CS
MEM_CS_L<0> — RP31 22 5% 1/16W SM1 — RAM_CS_L<0> 11 35
MEM_CS_L<1> — RP31 22 5% 1/16W SM1 — RAM_CS_L<1> 11 35
MEM_CS_L<2> — RP29 22 5% 1/16W SM1 — RAM_CS_L<2> 11 35
MEM_CS_L<3> — RP29 22 5% 1/16W SM1 — RAM_CS_L<3> 11 35

CKE
MEM_CKE<0> — RP31 22 5% 1/16W SM1 — RAM_CKE<0> 9 11 35
MEM_CKE<1> — RP31 22 5% 1/16W SM1 — RAM_CKE<1> 9 11 35
MEM_CKE<2> — RP29 22 5% 1/16W SM1 — RAM_CKE<2> 9 11 35
MEM_CKE<3> — RP29 22 5% 1/16W SM1 — RAM_CKE<3> 9 11 35

ADDR
MEM_ADDR<0> — RP14 22 5% 1/16W SM1 — RAM_ADDR<0> 11 35
MEM_ADDR<1> — RP12 22 5% 1/16W SM1 — RAM_ADDR<1> 11 35
MEM_ADDR<2> — RP12 22 5% 1/16W SM1 — RAM_ADDR<2> 11 35
MEM_ADDR<3> — RP12 22 5% 1/16W SM1 — RAM_ADDR<3> 11 35
MEM_ADDR<4> — RP9 22 5% 1/16W SM1 — RAM_ADDR<4> 11 35
MEM_ADDR<5> — RP9 22 5% 1/16W SM1 — RAM_ADDR<5> 11 35
MEM_ADDR<6> — RP14 22 5% 1/16W SM1 — RAM_ADDR<6> 11 35
MEM_ADDR<7> — RP9 22 5% 1/16W SM1 — RAM_ADDR<7> 11 35
MEM_ADDR<8> — RP14 22 5% 1/16W SM1 — RAM_ADDR<8> 11 35
MEM_ADDR<9> — RP14 22 5% 1/16W SM1 — RAM_ADDR<9> 11 35
MEM_ADDR<10> — RP17 22 5% 1/16W SM1 — RAM_ADDR<10> 11 35
MEM_ADDR<11> — RP9 22 5% 1/16W SM1 — RAM_ADDR<11> 11 35
MEM_ADDR<12> — RP17 22 5% 1/16W SM1 — RAM_ADDR<12> 11 35

BA
MEM_BA<0> — RP17 22 5% 1/16W SM1 — RAM_BA<0> 11 35
MEM_BA<1> — RP17 22 5% 1/16W SM1 — RAM_BA<1> 11 35

CNTL
MEM_WE_L — RP17 22 5% 1/16W SM1 — RAM_WE_L 11 35
MEM_CAS_L — R162 22 5% 1/16W MF 402 — RAM_CAS_L 11 35
MEM_RAS_L — R176 22 5% 1/16W MF 402 — RAM_RAS_L 11 35

+3V_MAIN
C125 2.2uF 20% 10V CERM 805
C773 0.1uF 10% 10V CERM 402
C122 0.1uF 10% 10V CERM 402

U11
FEPR-1MX8
1MX8-3.3V
TSOP
VPP OMIT VCC (11, 30, 31)

PCI_AD<0> 39 37 24 18 17 12 — A0 21 — DQ0 25 — PCI_AD<24> 12 17 18 24 37 39
PCI_AD<1> — A1 20 — DQ1 26 — PCI_AD<25>
PCI_AD<2> — A2 19 — DQ2 27 — PCI_AD<26>
PCI_AD<3> — A3 18 — DQ3 28 — PCI_AD<27>
PCI_AD<4> — A4 17 — DQ4 32 — PCI_AD<28>
PCI_AD<5> — A5 16 — DQ5 33 — PCI_AD<29>
PCI_AD<6> — A6 15 — DQ6 34 — PCI_AD<30>
PCI_AD<7> — A7 14 — DQ7 35 — PCI_AD<31>
PCI_AD<8> — A8 8
PCI_AD<9> — A9 7
PCI_AD<10> — A10 36
PCI_AD<11> — A11 6
PCI_AD<12> — A12 5
PCI_AD<13> — A13 4
PCI_AD<14> — A14 3
PCI_AD<15> — A15 2
PCI_AD<16> — A16 1
PCI_AD<17> — A17 40
PCI_AD<18> — A18 13
PCI_AD<19> — A19 37
PCI_AD<20> — A20 38

ROM_CS_TP_L 24
NO STUFF R236 0 5% 1/16W MF 402
+3V_MAIN
R691 10K 5% 1/16W MF 402
R112 10K 5% 1/16W MF 402
ROM_CS_L 39 12 — R674 1K 5% 1/16W MF 402 — ROM_ONBOARD_CS_L 39 12 — CE 22
ROM_OE_L 39 12 — OE 24
ROM_RW_L 39 12 — WE 9
ROM_WP_L 39 12 — WP 12
INT_RESET_L 29 13 — PWD 10
ROM_ONBOARD_CS_TP_L 24 — R1 0 NO STUFF 5% 1/16W MF 402
ROM_OE_TP_L 24 — R271 0 NO STUFF 5% 1/16W MF 402
ROM_RW_TP_L 24 — R194 0 NO STUFF 5% 1/16W MF 402
GND (23, 39)

OVERRIDE ROM MODULE INTERCEPTS ROM CHIP SELECT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1460	1	IC,BootRom Q16A	U11	CRITICAL	?

Weak pulldowns ensure CKEs stay low after 2.5V I/O to Intrepid shuts off.

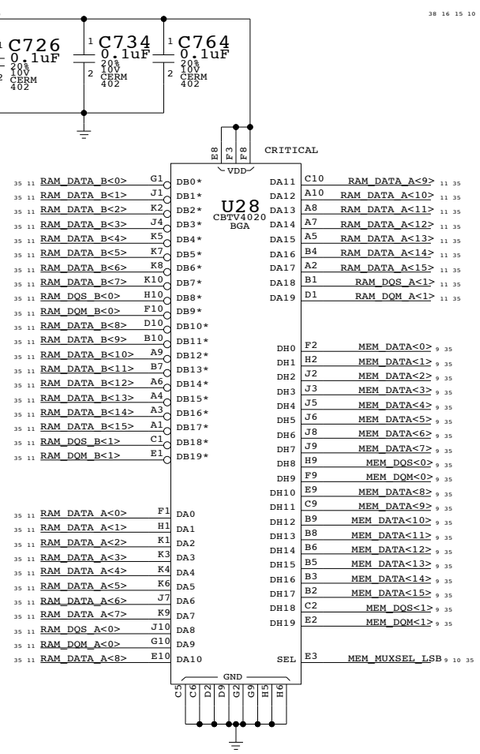
RAM_CKE<0> 35 11 9
RAM_CKE<1> 35 11 9
RAM_CKE<2> 35 11 9
RAM_CKE<3> 35 11 9
INT_2_5V_COLD R247 10K 5% 1/16W MF 402
INT_2_5V_COLD R257 10K 5% 1/16W MF 402
INT_2_5V_COLD R260 10K 5% 1/16W MF 402
INT_2_5V_COLD R265 10K 5% 1/16W MF 402

INT - DDR/BOOTROM

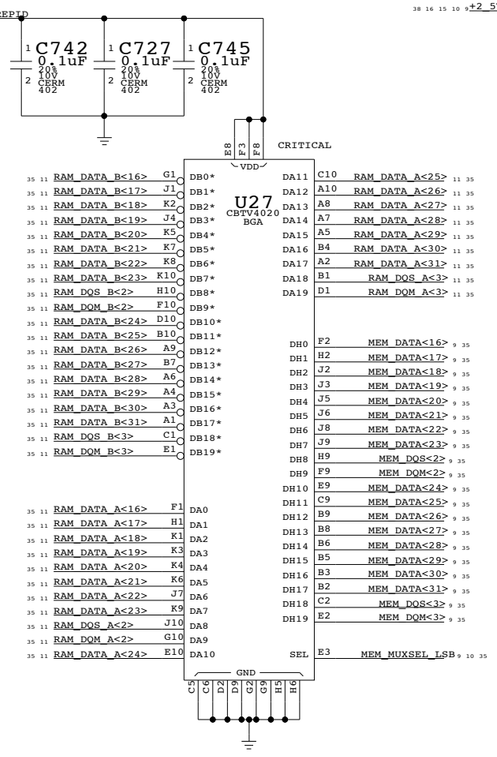
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	B
SCALE: NONE	SHT 9 OF 44	

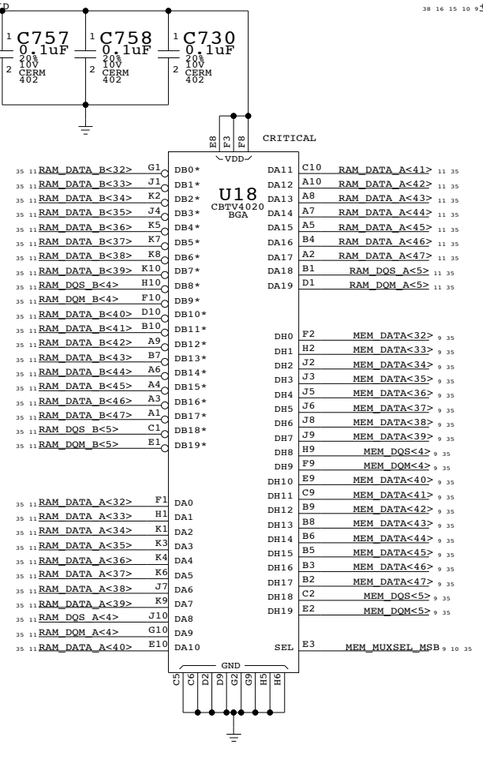
BIT 0..15



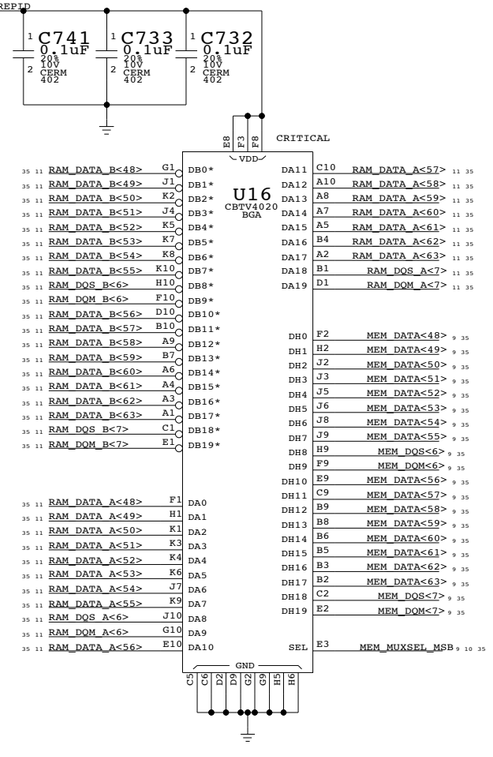
BIT 16..31



BIT 32..47



BIT 48..63

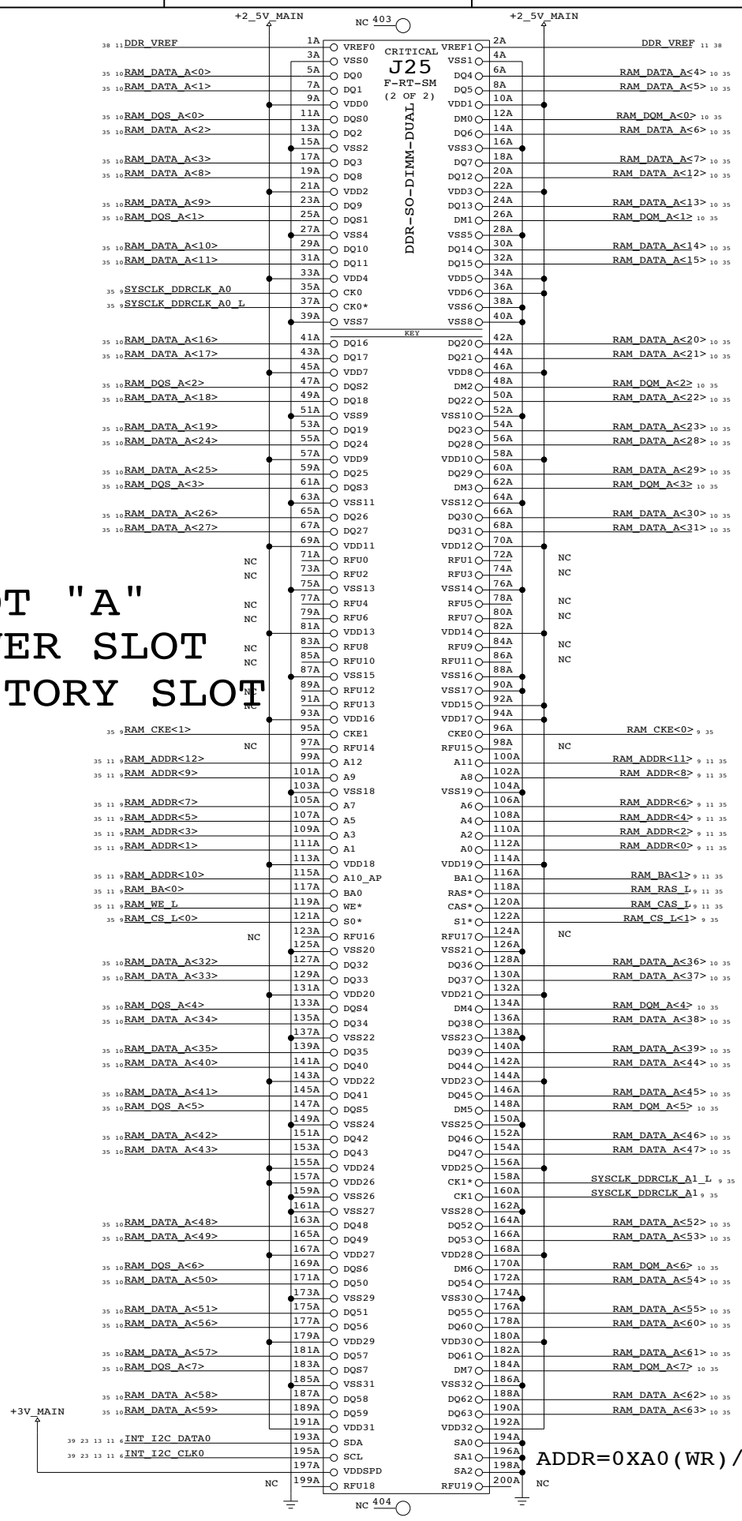


SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND

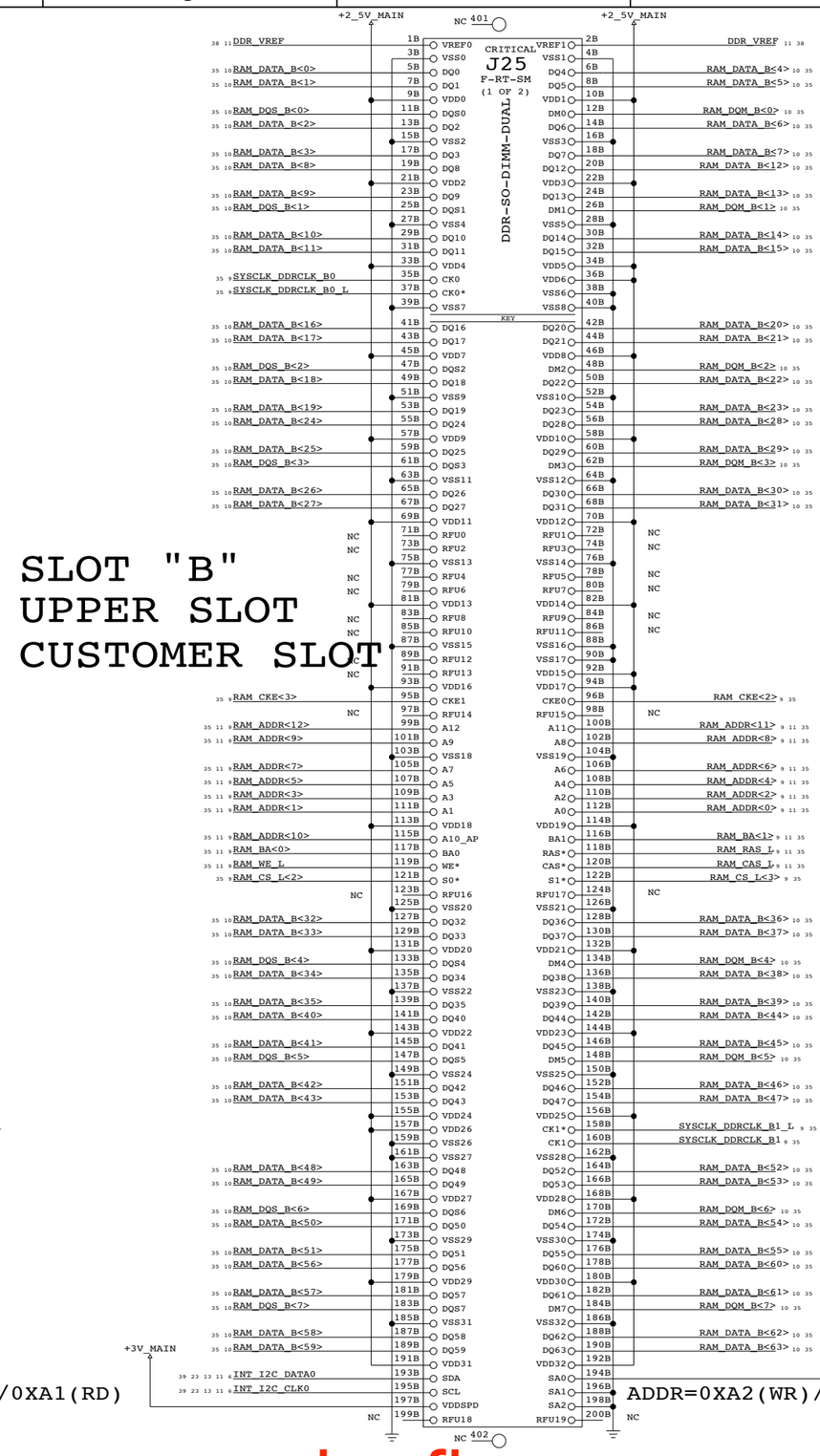
16BIT 2:1 DDR MUXES

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	B
SCALE: NONE	SHT 10 OF 44	

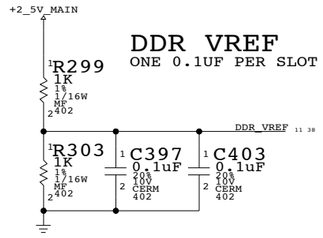


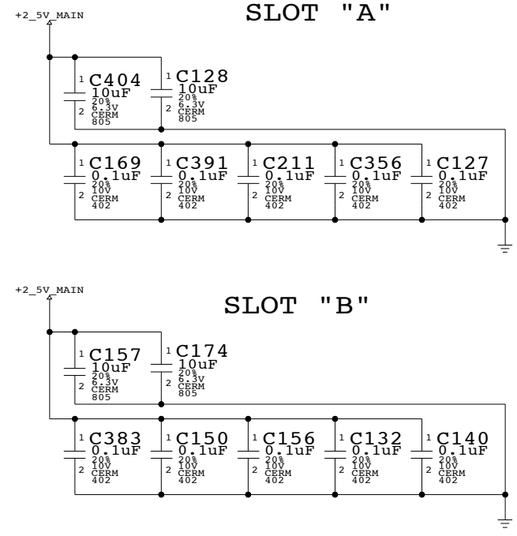
SLOT "A"
LOWER SLOT
FACTORY SLOT



SLOT "B"
UPPER SLOT
CUSTOMER SLOT

NOTE: The SODIMM connector footprint has a through-hole slot on the PCB for additional mounting

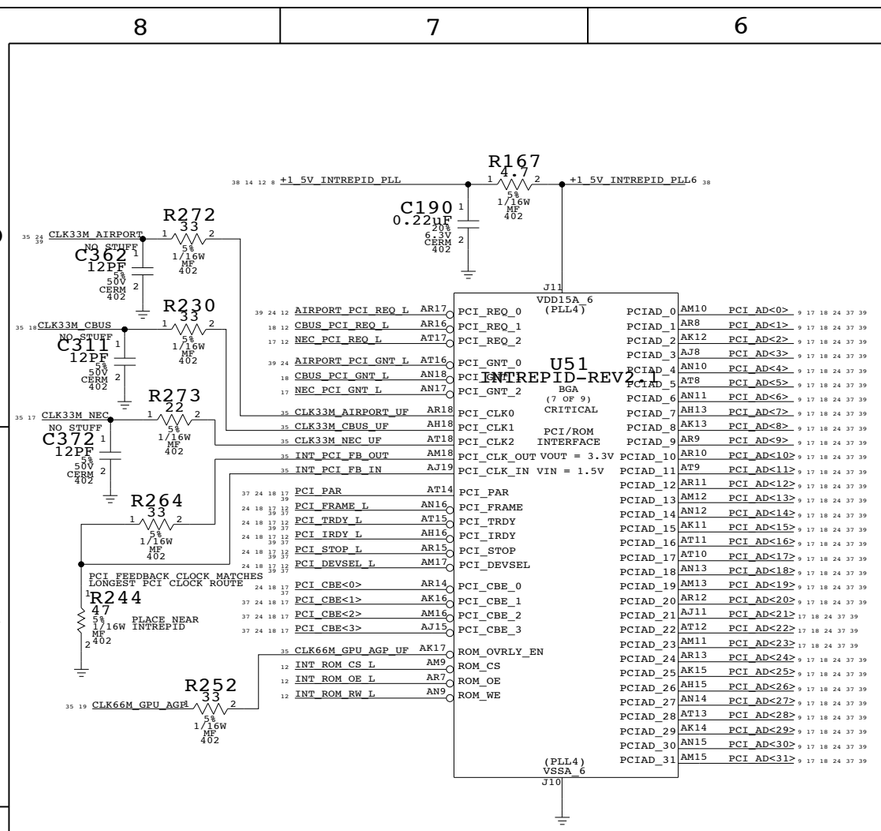


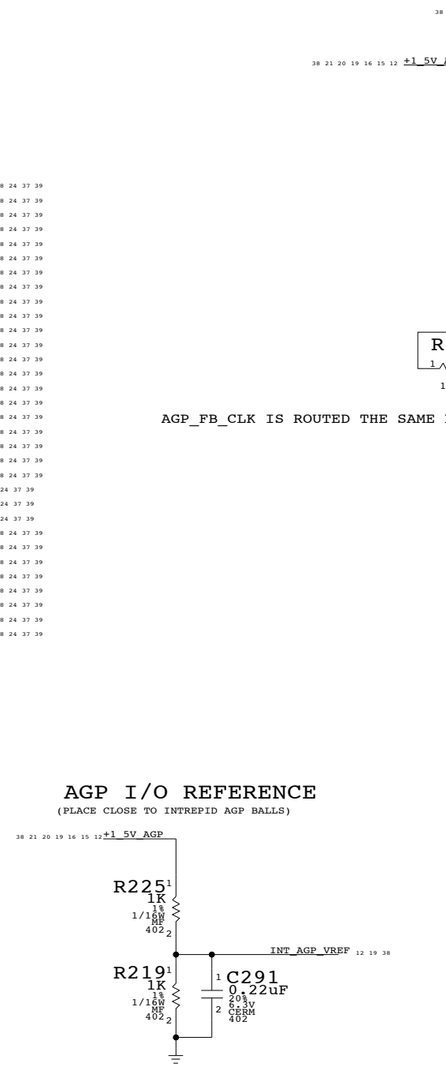


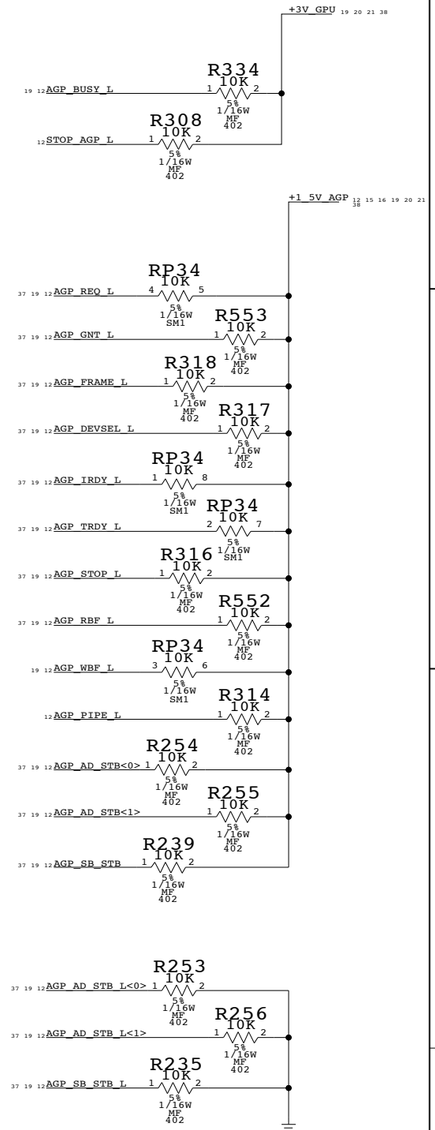
DDR SODIMM CONNS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	B
SCALE: NONE	SHT 11 OF 44	



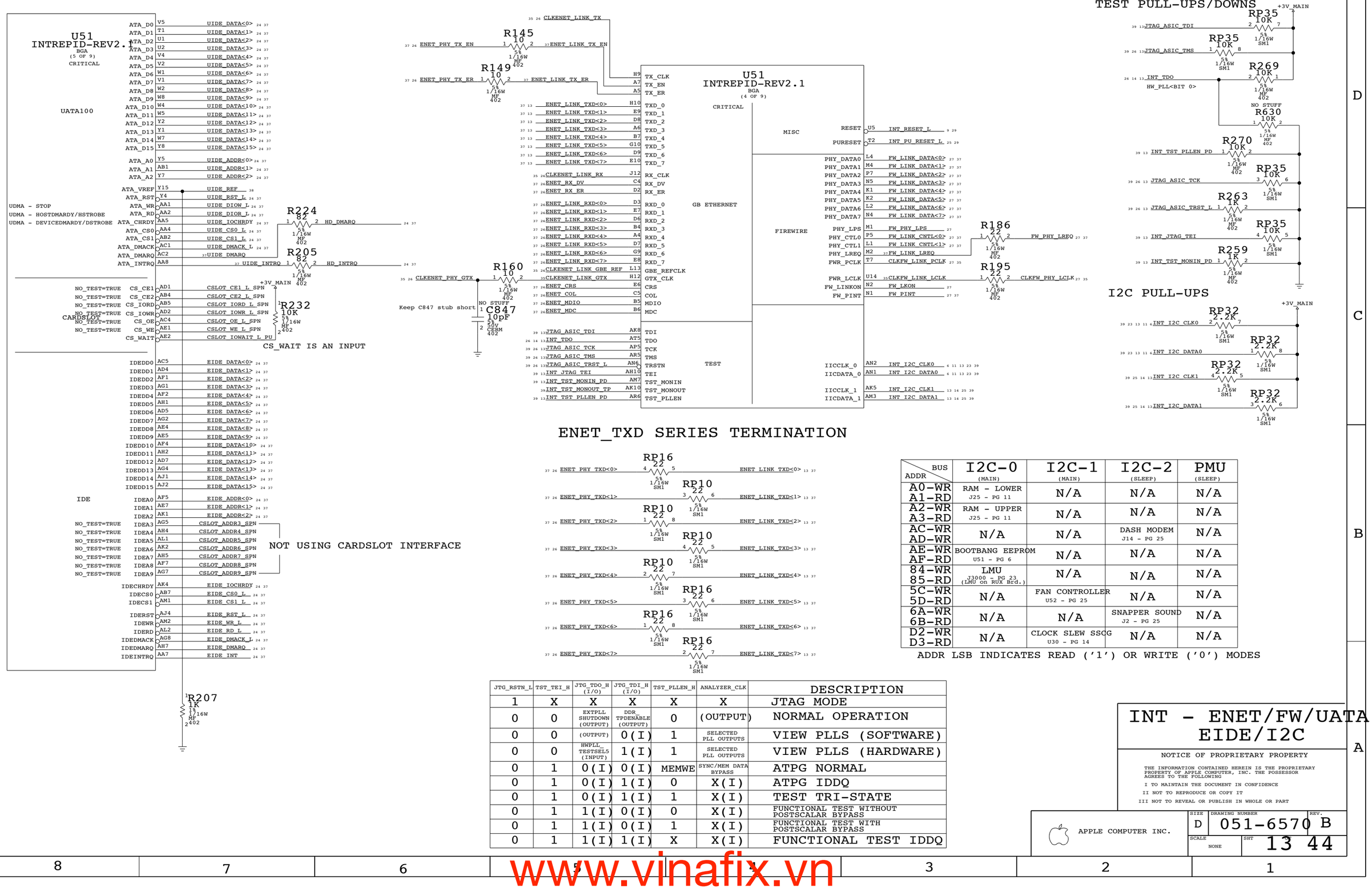




INTREPID AGP/PCI

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	B
SCALE: NONE	SHT 12 OF 44	



USB PORT ASSIGNMENTS

PORT A - PORT D/UNUSED

R181 10K 5% 1/16W MF 402 — USB_DAM
R183 10K 5% 1/16W MF 402 — USB_DAP
R156 10K 5% 1/16W MF 402 — USB_DBM
R157 10K 5% 1/16W MF 402 — USB_DBP
R164 10K 5% 1/16W MF 402 — USB_DCM
R165 10K 5% 1/16W MF 402 — USB_DCP
R182 10K 5% 1/16W MF 402 — USB_DDM
R180 10K 5% 1/16W MF 402 — USB_DDP

PORT E/BLUETOOTH

R174 22 5% 1/16W MF 402 — USB_DEP → BT_USB_DP
R179 22 5% 1/16W MF 402 — USB_DEM → BT_USB_DM
R178 15K 5% 1/16W MF 402
R175 15K 5% 1/16W MF 402

PORT F/MODEM

R192 22 5% 1/16W MF 402 — USB_DFP → MODEM_USB_DP
R188 22 5% 1/16W MF 402 — USB_DFM → MODEM_USB_DM
R189 15K 5% 1/16W MF 402
R193 15K 5% 1/16W MF 402

PCI INTERRUPTS

R148 10K 5% 1/16W MF 402 — CBUS_INT_L
R746 10K 5% 1/16W MF 402 — AIRPORT_PCI_INT_L
R158 10K 5% 1/16W MF 402 — NEC_PCI_INT_L

GPIO/EXTINT PULLUPS

R187 10K — USB_PWREN_EF_L
R191 10K — USB_OC_EF_L
RP11 10K — USB_OC_AB_L
RP11 10K — USB_PWREN_CD_L
RP8 10K — USB_PWREN_AB_L
RP11 10K — USB_OC_CD_L
RP8 10K — INT_EXTINT14_PU
RP5 10K — INT_EXTINT8_PU
RP6 10K — COMM_RING_DET_L
RP11 10K — INT_GPIO15_PU
RP6 10K — PMU_INT_NMI
RP6 10K — PMU_INT_L
R250 10K — PMU_REQ_L
RP7 10K — INT_GPIO12_PU
RP7 10K — INT_EXTINT13_PU
RP4 10K — INT_EXTINT16_PU
RP5 10K — INT_EXTINT11_PU
RP6 10K — INT_EXTINT10_PU
RP4 10K — INT_EXTINT12_PU
RP8 10K — INT_GPIO9_PU
RP8 10K — INT_GPIO1_PU
R153 10K — INT_EXTINT3_PU
RP15 10K (USB_MODEM) — INT_MOD_DTO_UF
RP15 10K (USB_MODEM) — INT_MOD_CLKOUT_UF
RP15 10K (USB_MODEM) — INT_MOD_DTI
RP15 10K (USB_MODEM) — INT_MOD_SYNC_UF
R206 10K (USB_MODEM)
R166 100K — SND_HW_RESET_L

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
359S0086	1	IC,CY28512-2	U31	CRITICAL	SSCG

U49 LT1962-ADJ MSOP: IN ← +2_5V_MAIN; +1_8V_MAIN via R565 0; OUT → +1_5V_INTREPID_PLL (-> 1.55V OUTPUT); ADJ ← LT1962_INT_ADJ; BYP ← LT1962_INT_BYP; SHDN ← +3V_SLEEP via R148; NC, NC
C721 1uF 10% 10V CERM 603
C392 0.01uF 20% 16V CERM 402
R574 18.7K 1% 1/16W MF 402
R567 68.1K 1% 1/16W MF 402
C723 10uF 20% 6.3V CERM 805

C337 0.22uF 20% 6.3V CERM 402
C389 0.22uF 20% 6.3V CERM 402
C388 0.22uF 20% 6.3V CERM 402
C386 0.22uF 20% 6.3V CERM 402
C387 0.22uF 20% 6.3V CERM 402

R240 4.7 5% 1/16W MF 402 — +1_5V_INTREPID_PLL8
R280 4.7 — +1_5V_INTREPID_PLL4
R279 4.7 — +1_5V_INTREPID_PLL3
R243 4 — +1_5V_INTREPID_PLL2
R201 4.7 — +1_5V_INTREPID_PLL1

L13 FERR-EMI-100-OHM SM — +3V_MAIN
+3V_INTREPID_USB

C235 0.01uF 20% 16V CERM 402
C246 0.1uF 20% 10V CERM 402
C256 10uF 20% 6.3V CERM 805

L15 400-OHM-EMI SM-1 (SSCG) — +3V_MAIN
L14 400-OHM-EMI SM-1 (SSCG) — +2_5V_MAIN

C400 0.1uF 20% 10V CERM 402
C402 1uF 20% 10V CERM 603
C399 0.1uF 20% 10V CERM 402
C394 0.1uF 20% 10V CERM 402

R286 0 (NO STUFF)
R287 10K
R288 10K
R295 10K (NO STUFF)
R450 0 — CG_FSEL

U51 INTREPID-REV2.1 BGA CRITICAL (6 OF 9)

GPIO0	G5	VCORE A/B SEL
GPIO1	E1	GENERAL PURPOSE I/O'S
GPIO2	J7	
GPIO3	F2	
GPIO4	J8	
GPIO5	H5	
GPIO6	L9	
GPIO9	H4	
GPIO11	J5	
GPIO12	K8	
GPIO15	F1	
GPIO16	K7	
EXTINT0	F33	INTERRUPTS
EXTINT1	E34	
EXTINT2	C33	
EXTINT3	D34	
EXTINT4	B33	
EXTINT5	A33	
EXTINT6	E31	
EXTINT7	G30	
EXTINT8	D31	
EXTINT9	C32	
EXTINT10	B32	CBUS_REG_L
EXTINT11	E30	CBUS_IREQ_L
EXTINT12	J9	
EXTINT13	F4	
EXTINT14	D1	
EXTINT15	E2	
EXTINT16	H7	
EXTINT17	G4	
CPU_INT	D30	
PCIPME	AJ7	POWERBOOK SPARE
PROCSLEEPREQ	AE6	
PENDPROCINT	AN8	
XTAL_IN	U4	CLOCKS
XTAL_OUT	V15	
STOPXTAL	AN7	
WATCHDOG	AT7	
BUF_REF_CLK_OUT	U15	
SS_REF_CLK_IN	K9	

PCI VDD15A_1 (PLL1) AA16; PCI VDD15A_2 (PLL2) AJ12; PCI VDD15A_3 (PLL3) AJ17; PCI VDD15A_4 (PLL7) AJ18; VDD15A_8 (PLL9) AG29
VDDU33_1 F8; VDDU33_2 U8
VSSA1 (PLL1) AA15; VSSA2 (PLL2) AJ13; VSSA3 (PLL3) AJ16; VSSA4 (PLL7) AK18; VSSA_8 (PLL9) AH29; VSSU_1 R9; VSSU_2 R8

USB:
SCCTXDA AF9 COMM_TXD_L; SCCRTSA AN3 COMM_RTS_L; SCCDTRA AF10 COMM_DTR_L; SCCRXDA AG11 COMM_RXD; SCCGPIOA AG9 COMM_GPIO_L; SCCTRXCA AT4 COMM_TRXC
VIA: MISO SCCTXDB AR4 PMU_FROM_INT; REQ* SCCRTSB AL5 PMU_REQ_L; MOSI SCCRXDB AG10 PMU_TO_INT; ACK* SCCGPIOB AP4 PMU_ACK_L; SCK SCCTRXCB AM5 PMU_CLK
USB_VD0_P L8 USB_DAP; USB_VD0_N L7 USB_DAM
USB_VD1_P G2 USB_DBP; USB_VD1_N G1 USB_DBM
USB_PRTPWR0 J4 USB_PWREN_AB_L; USB_PWRFLT0 K4 USB_OC_AB_L
USB_VD2_P H2 USB_DCP; USB_VD2_N H1 USB_DCM
USB_VD3_P M7 USB_DDP; USB_VD3_N M8 USB_DDM
USB_PRTPWR1 J2 USB_PWREN_CD_L; USB_PWRFLT1 J1 USB_OC_CD_L
USB_VD4_P K5 USB_DEP; USB_VD4_N L5 USB_DEM
USB_VD5_P P8 USB_DFP; USB_VD5_N N8 USB_DFM
USB_PRTPWR2 M5 USB_PWREN_EF_L; USB_PWRFLT2 N7 USB_OC_EF_L

AUDIO/I2S (SIGNAL FROM MODEM):
AUD_DTO R4 INT_I2S0_SND_TO_DAC_UF; AUD_DTI R7 INT_I2S0_SND_FROM_ADC_UF; AUD_SYNC T5 INT_I2S0_SND_LRCLK_UF; AUD_BITCLK P2 INT_I2S0_SND_SCLK_UF; AUD_CLKOUT R5 INT_I2S0_SND_MCLK_UF
MOD_DTO R2 INT_MOD_DTO_UF; MOD_DTI T4 INT_MOD_DTI_UF; MOD_SYNC R1 INT_MOD_SYNC_UF; MOD_BITCLK V8 INT_MOD_BITCLK_UF; MOD_CLKOUT P1 INT_MOD_CLKOUT_UF

IIC: IICCLK_2 AL4; IICDATA_2 AH8

R218 0 — INT_REF_CLK_OUT → INT_REF_CLK_OUT_UF
R134 0 (NO STUFF)
R113 51 (NO STUFF)
R144 10M (NO STUFF)
R143 0 (CRITICAL)
Y2 18.432M 8X4.5MM-SM — CLK18M_XTAL_IN
C152 22pF 5% 50V CERM 402
C151 22pF 5% 50V CERM 402
CRYSTAL LOAD CAPACITANCE IS 16PF

J9 U.FL-R_SMT F-ST-SM (NO STUFF) — CLK18M_INT_EXT
R467 0 (NO STUFF) — SYSTEM_CLK_EN
R457 0 — INT_TDO → CG_SYSCLK_EN

U31 CY28512D TSSOP OMIT — INTERNAL 250K PULL-UP; OUTPUT IMPEDANCE ~18-20 OHMS
CLKIN ← INT_REF_CLK_IN (R293 33)
CPU0 → CG_CLKOUT1
FSEL ← CG_FSEL
SCLK ← INT_I2C_CLK1
SDATA ← INT_I2C_DATA1
ADDRSEL INTERNAL 250K PULL-DOWN ← CG_ADDRSEL
RESET* ← CG_RESET_L
PD* ← CG_SYSCLK_EN
LOCK OPEN DRAIN OUTPUT → CG_LOCK
ODSEL INTERNAL 250K PULL-UP
VDD0 VDD1 VDDA VDDC VDDQ; VSSA VSSC VSSQ
R292 75 — PLACE NEAR INTREPID TO MINIMIZE OVERSHOOT
R284 0 — VCORE_VGATE
R296 10K
R142 0 — VCORE_VGATE

HWPLL_TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0004	197S0035		Y2	Alt. for Siward Part

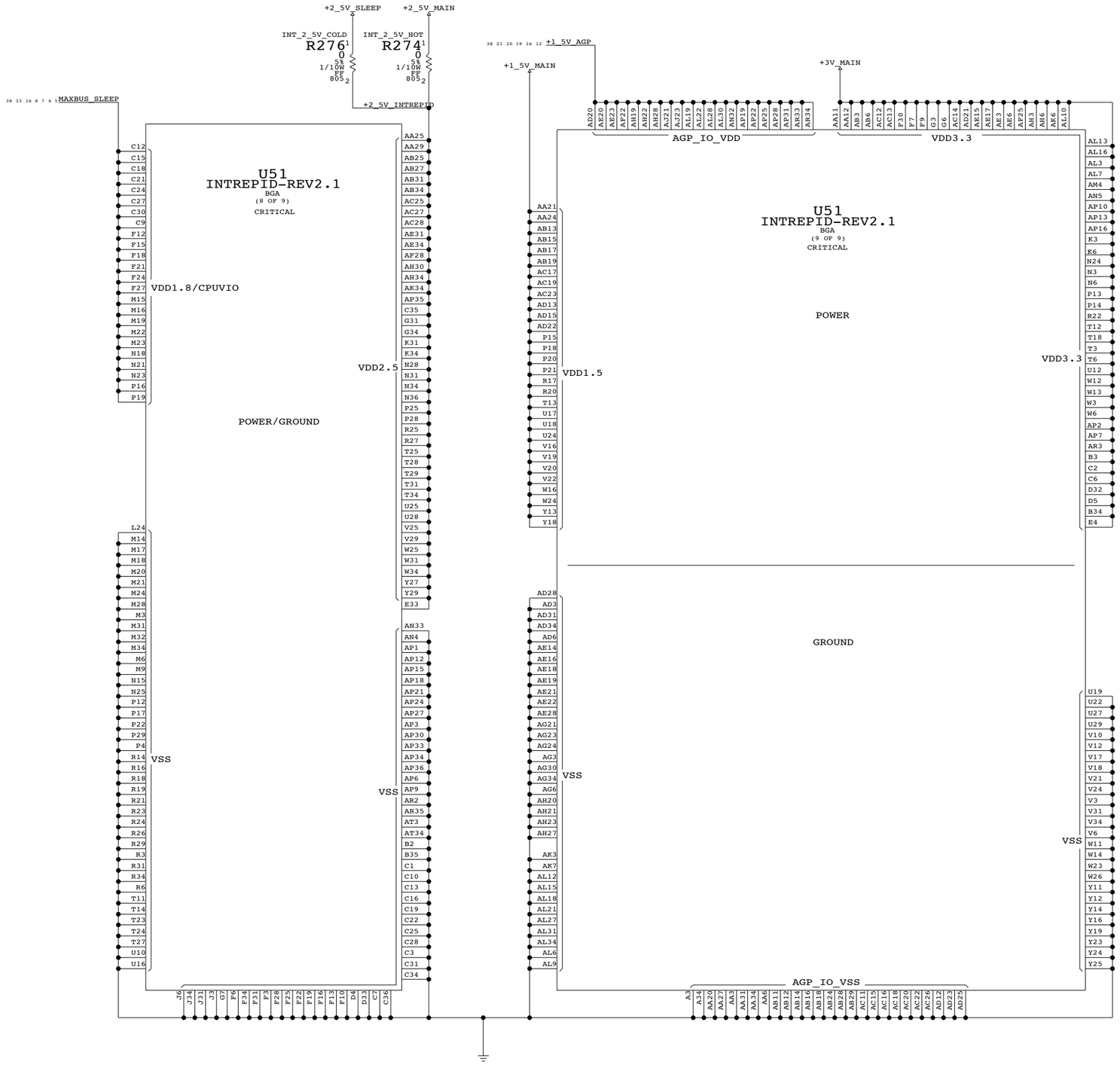
PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES	RES-0402-V2	RESISTOR	10K		1/16W	5%	R292	NO_SSCG

RP13 47 5% 1/16W SM1 — INT_I2S0_SND_TO_DAC; INT_I2S0_SND_LRCLK; INT_I2S0_SND_SCLK; INT_I2S0_SND_MCLK
SOFT_MODEM RP47 0K 5% 1/16W SM1 — INT_MOD_DTO; INT_MOD_SYNC; INT_MOD_BITCLK; INT_MOD_CLKOUT
+3V_SLEEP
R258 1K 5% 1/16W MF 402 — INT_I2C_CLK2
R241 1K 5% 1/16W MF 402 — INT_I2C_DATA2

INT - USB/GPIOS/I2S

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	B
SCALE: NONE	SHT 14 OF 44	



Intrepid Power

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	B
SCALE: NONE	SHT 15	OF 44

INTREPID MAXBUS DECOUPLING

24 Balls
4 X 10UF (0805)
28 X 0.22UF (0402)

33 15 8 7 6 5 MAXBUS_SLEEP

C148 10uF, C142 10uF, C182 0.22uF, C178 0.22uF, C141 0.22uF, C145 0.22uF, C214 0.22uF, C163 0.22uF, C164 0.22uF, C225 0.22uF, C160 0.22uF, C159 0.22uF
C144 10uF, C146 10uF, C204 0.22uF, C166 0.22uF, C205 0.22uF, C223 0.22uF, C229 0.22uF, C181 0.22uF, C207 0.22uF, C208 0.22uF, C183 0.22uF, C180 0.22uF
C165 0.22uF, C206 0.22uF, C147 0.22uF, C149 0.22uF, C179 0.22uF, C162 0.22uF, C161 0.22uF, C213 0.22uF

INTREPID CORE DECOUPLING

30 Balls
4 X 10UF (0805)
29 X 0.22UF (0402)

+1_5V_MAIN

C324 10uF, C325 10uF, C299 0.22uF, C279 0.22uF, C262 0.22uF, C292 0.22uF, C248 0.22uF, C302 0.22uF, C300 0.22uF, C290 0.22uF, C272 0.22uF, C259 0.22uF
C201 10uF, C200 10uF, C301 0.22uF, C278 0.22uF, C226 0.22uF, C238 0.22uF, C250 0.22uF, C263 0.22uF, C224 0.22uF, C222 0.22uF, C261 0.22uF, C227 0.22uF
C271 0.22uF, C310 0.22uF, C288 0.22uF, C260 0.22uF, C303 0.22uF, C287 0.22uF, C258 0.22uF, C236 0.22uF, C289 0.22uF

INTREPID AGP I/O DECOUPLING

21 Balls
4 X 10UF (0805)
21 X 0.22UF (0402)

30 21 20 19 15 12 +1_5V_AGP

C381 10uF, C380 10uF, C367 0.22uF, C319 0.22uF, C330 0.22uF, C363 0.22uF, C366 0.22uF, C332 0.22uF, C361 0.22uF, C320 0.22uF, C328 0.22uF, C364 0.22uF
C382 10uF, C379 10uF, C365 0.22uF, C329 0.22uF, C345 0.22uF, C346 0.22uF, C373 0.22uF, C344 0.22uF, C331 0.22uF, C312 0.22uF, C354 0.22uF, C347 0.22uF
C321 0.22uF

INTREPID 3.3V DECOUPLING

57 Balls
4 X 10UF (0805)
40 X 0.22UF (0402)

+3V_MAIN

C378 10uF, C376 10uF, C170 0.22uF, C358 0.22uF, C268 0.22uF, C327 0.22uF, C342 0.22uF, C215 0.22uF, C352 0.22uF, C171 0.22uF, C158 0.22uF, C309 0.22uF
C377 10uF, C375 10uF, C175 0.22uF, C357 0.22uF, C351 0.22uF, C350 0.22uF, C286 0.22uF, C176 0.22uF, C189 0.22uF, C167 0.22uF, C371 0.22uF, C359 0.22uF
C285 0.22uF, C283 0.22uF, C269 0.22uF, C221 0.22uF, C234 0.22uF, C247 0.22uF, C257 0.22uF, C343 0.22uF, C313 0.22uF, C228 0.22uF
C360 0.22uF, C308 0.22uF, C318 0.22uF, C237 0.22uF, C317 0.22uF, C341 0.22uF, C177 0.22uF, C212 0.22uF, C349 0.22uF, C184 0.22uF

INTREPID DDR DECOUPLING

44 Balls
4 X 10UF (0805)
46 X 0.22UF (0402)

38 15 10 9 +2_5V_INTREPID

C314 10uF, C322 10uF, C304 0.22uF, C266 0.22uF, C172 0.22uF, C281 0.22uF, C243 0.22uF, C253 0.22uF, C334 0.22uF, C241 0.22uF, C348 0.22uF, C192 0.22uF
C191 10uF, C202 10uF, C306 0.22uF, C252 0.22uF, C275 0.22uF, C297 0.22uF, C240 0.22uF, C218 0.22uF, C274 0.22uF, C369 0.22uF, C368 0.22uF, C168 0.22uF
C265 0.22uF, C251 0.22uF, C216 0.22uF, C254 0.22uF, C305 0.22uF, C186 0.22uF, C219 0.22uF, C315 0.22uF, C264 0.22uF, C294 0.22uF
C323 0.22uF, C273 0.22uF, C242 0.22uF, C203 0.22uF, C333 0.22uF, C217 0.22uF, C230 0.22uF, C293 0.22uF, C231 0.22uF, C296 0.22uF
C239 0.22uF, C316 0.22uF, C185 0.22uF, C282 0.22uF, C295 0.22uF, C280 0.22uF

INTREPID/MAIN 2.5V DECOUPLING

10 X 0.22UF (0402)

+2_5V_MAIN

C770 0.22uF, C139 0.22uF, C335 0.22uF, C735 0.22uF, C245 0.22uF, C736 0.22uF, C739 0.22uF, C395 0.22uF, C374 0.22uF, C385 0.22uF

Place these 2.5V Decoupling Caps near the Edge of +2.5V_MAIN and +2.5V_INTREPID split

Intrepid Decoupling

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	B
SCALE: NONE	SHT 16 OF 44	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0608	197S0038		Y1	Alt. for Siward Part

+3V_NEC_VDD 17 38

C749 0.1uF 20% 10V CERM 402
C746 0.1uF 20% 10V CERM 402
C761 0.1uF 20% 10V CERM 402
C750 0.1uF 20% 10V CERM 402
C756 0.1uF 20% 10V CERM 402
C748 0.1uF 20% 10V CERM 402
C769 0.1uF 20% 10V CERM 402
C752 0.1uF 20% 10V CERM 402
C747 0.1uF 20% 10V CERM 402
C197 10uF 20% 6.3V CERM 805
C765 0.1uF 20% 10V CERM 402
C768 0.1uF 20% 10V CERM 402

+3V_MAIN

L7 FERR-EMI-100-OHM SM

R172 0 5% 1/16W MF 603

C760 0.1uF 20% 10V CERM 402
C751 0.1uF 20% 10V CERM 402
C173 10uF 20% 6.3V CERM 805

38 NEC_AVDD

38 17 +3V_NEC_VDD

H3 M4 C8 P2 P3 P12 A13 A12 A3 E2 N8 L13 J13 H13 F13 D13 G12 H4 D7 — VDD
N10 N12 — AVDD

CRITICAL
U17
NEC_uPD720101_USB2
FBGA

PCI_AD<0>	M5	AD0
PCI_AD<1>	P5	AD1
PCI_AD<2>	N5	AD2
PCI_AD<3>	P4	AD3
PCI_AD<4>	N4	AD4
PCI_AD<5>	M3	AD5
PCI_AD<6>	N3	AD6
PCI_AD<7>	M1	AD7
PCI_AD<8>	L2	AD8
PCI_AD<9>	L1	AD9
PCI_AD<10>	K2	AD10
PCI_AD<11>	L3	AD11
PCI_AD<12>	K1	AD12
PCI_AD<13>	K3	AD13
PCI_AD<14>	J2	AD14
PCI_AD<15>	J1	AD15
PCI_AD<16>	F2	AD16
PCI_AD<17>	E3	AD17
PCI_AD<18>	E1	AD18
PCI_AD<19>	D3	AD19
PCI_AD<20>	D1	AD20
PCI_AD<21>	D2	AD21
PCI_AD<22>	C2	AD22
PCI_AD<23>	C1	AD23
PCI_AD<24>	B4	AD24
PCI_AD<25>	A4	AD25
PCI_AD<26>	B5	AD26
(PCI_AD<27>)	C4	AD27
PCI_AD<28>	A5	AD28
PCI_AD<29>	C5	AD29
PCI_AD<30>	B6	AD30
PCI_AD<31>	A6	AD31
PCI_CBE<0>	M2	CBE0
PCI_CBE<1>	J3	CBE1
PCI_CBE<2>	F1	CBE2
PCI_CBE<3>	C3	CBE3
PCI_PAR	J4	PAR
PCI_FRAME_L	F3	FRAME
PCI_IRDY_L	F4	IRDY
PCI_TRDY_L	G1	TRDY
PCI_STOP_L	G3	STOP
NEC_IDSEL	B3	IDSEL
PCI_DEVSEL_L	G2	DEVSEL
NEC_PCI_REQ_L	C6	REQ
NEC_PCI_GNT_L	D6	GNT
PCI_PERR_L	H2	PERR
PCI_SERR_L	H1	SERR
NEC_PCI_INTA_L	C7	INTA
NEC_PCI_INTB_L	B7	INTB
NEC_PCI_INTC_L	A7	INTC
CLK33M_NEC	A8	PCLK
NEC_IO_RESET_L	B8	VBBRST
NEC_CRUN_L	N6	CRUN
NEC_PME_L	D9	PME
NEC_MAIN_RESET_L	C9	VCCRST
NEC_SMI_L_TP	L6	SMI
NEC_LEGC	L7	LEGC

R636 22 5% 1/16W MF 402

Series Rpaks required to facilitate NAND-tree testing

RP45 47 5% 1/16W SM1

NEC_PCI_INT_L

R617 4.7K 5% 1/16W MF 402

RP44 47 5% 1/16W SM1

IO_RESET_L — NEC_IO_RESET_L
PMU_PME_L — NEC_PME_L
MAIN_RESET_L — NEC_MAIN_RESET_L
NEC_LEGC

VSS
B1 N1 P10 N14 H14 B14 A2 B2 N2 N13 B13 M11 L12 H12 D12 G4 J11 F11 D8

Y1's LOAD CAPACITANCE = 16 pF

CRITICAL
Y1 30.0000M 8X4.5MM-SM
NEC_XT2_R

C759 27pF 5% 50V CERM 402
C136 27pF 5% 50V CERM 402
R124 100 5% 1/16W MF 402

XT1/SCLK	L9	NEC_XT1
XT2	P8	NEC_XT2
RSDM1	M14	NEC_USB_RSDM1
DM1	M13	(NEC_USB_DAM)
DP1	L14	(NEC_USB_DAP)
RSDP1	K13	NEC_USB_RSDP1
RSDM2	K14	NEC_USB_RSDM2
DM2	K12	(NEC_USB_DBM)
DP2	J14	(NEC_USB_DBP)
RSDP2	J12	NEC_USB_RSDP2
RSDM3	H11	NC
DM3	G11	
DP3	G13	
RSDP3	G14	NC
RSDM4	F12	NC
DM4	F14	
DP4	E12	
RSDP4	E14	NC
RSDM5	E13	NC
DM5	D14	
DP5	C13	
RSDP5	C14	NC
RREF	P11	NEC_RREF

R614 9.09K 1% 1/16W MF 402 — Tie to GND (NEC_AVSS_F) at ball N11 — NEC_AVSS_F 17

R613 43.2 1% 1/16W MF 402 — NEC_USB_DAM 25 37 39
R612 43.2 1% 1/16W MF 402 — NEC_USB_DAP 25 37 39
Low/Full/High Speed (External)
R609 43.2 1% 1/16W MF 402 — NEC_USB_DBM 25 37 39
R610 43.2 1% 1/16W MF 402 — NEC_USB_DBP 25 37 39
Low/Full/High Speed (External)

+3V_NEC_VDD 17 38

RP43 10K 5% 1/16W SM1
RP43 10K 5% 1/16W SM1
RP43 10K 5% 1/16W SM1
R606 10K 5% 1/16W MF 402
R615 1K 5% 1/16W MF 402
R632 1K 5% 1/16W MF 402

OCI1	B12	NEC_LUSB_OCI 17
OCI2	B11	NEC_RUSB_OCI 17
OCI3	B10	NEC_OCI<3>
OCI4	A10	NEC_OCI<4>
OCI5	B9	NEC_OCI<5>
PPON1	C12 OUT	NEC_LUSB_PPON 25 39
PPON2	A11 OUT	NEC_RUSB_PPON 25 39
PPON3	C11 OUT	NEC_PPON3_TP
PPON4	C10 OUT	NEC_PPON4_TP
PPON5	A9 OUT	NEC_PPON5_TP
NC1	P6	NEC_NC<1>
NC2	M6	NEC_NC<2>

NEC documentation indicates that NCs must be tied high.

NTEST1	M8 IPD	NC
SMC	M7 IPD	NC
TEB	N7 IPD	NC
AMC	P7 IPD	NEC_AMC_TP
TEST	L8 IPD	NC
NANDTEST	M10	NEC_NANDTESTEN_TP
SRCLK	M9	NC
SRDTA	N9	NEC_NANDTESTOUT_TP
SRMOD	P9 IPD	NC
AVSS (R)	N11 P13 M12	AVSS

R798 0 5% 1/10W MF 603 — 17 NEC_AVSS_F

+3V_MAIN

RP43 10K 5% 1/16W SM1
RP43 10K 5% 1/16W SM1
R607 0 5% 1/16W MF 402
R608 0 5% 1/16W MF 402

17 NEC_LUSB_OCI — NEC_LUSB_OCI_UF 25 39
17 NEC_RUSB_OCI — NEC_RUSB_OCI_UF 25 39

NO STUFF C743 0.1uF 20% 10V CERM 402
NO STUFF C744 0.1uF 20% 10V CERM 402

USB 2.0

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6570 | REV. B

SCALE NONE | SHT 17 OF 44

PCI1510 PULL-UPS

+3V_SLEEP

R756 0 5% 1/16W MF 603

+3V_SLEEP_PCCARD

C60 10uF 20% 6.3V CERM 805
C776 10uF 20% 6.3V CERM 805
C789 0.22uF 20% 6.3V CERM 402
C791 0.22uF 20% 6.3V CERM 402
C784 0.22uF 20% 6.3V CERM 402
C782 0.22uF 20% 6.3V CERM 402
C783 0.22uF 20% 6.3V CERM 402
C778 0.22uF 20% 6.3V CERM 402
C775 0.22uF 20% 6.3V CERM 402

+3V_SLEEP_PCCARD

R718 10K 5% 1/16W MF 402 — PCI_PERR_L
R714 10K 5% 1/16W MF 402 — PCI_SERR_L
R722 10K 5% 1/16W MF 402 — CBUS_SUSPEND_PU

R721 10K 5% 1/16W MF 402

+2_5V_SLEEP

C787 4.7uF 20% 6.3V CERM 805
C786 0.22uF 20% 6.3V CERM 402

A7 C13 D5 E1 M1 N7 N11
VCC

+3V_MAIN

+5V_MAIN

SLEEP_L_LS5

R726 0 5% 1/16W MF 402

TPS2211_SHTDWN

U4
TPS2211
SSOI

NC	9		
V_12	5	AVPP	10
V_5_1	6		
V_5_2	3	AVCC0	11
V_3_1	4	AVCC1	12
V_3_2		AVCC2	13
VCCD0	1		
VCCD1	2		
VPPD0	15		
VPPD1	14		
SHTDWN	16		
GND	7	OC	8 (NC)

+VPP_CBUS_SW
+VCC_CBUS_SW

C40 0.1uF 20% 10V CERM 402
C37 0.1uF 20% 10V CERM 402

MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES TO MINIMIZE INDUCTANCE!

0.1UF ARE USED TO INCREASE ESD DISCHARGES OF UP TO 10KV

U8
PCI1510GGU
BGA

NC	H10	CLK_48_RSVD/NC	
PCI1510_VR_EN_L	D4	VR_EN*	
	L8	VR_PORT	
PCI_AD<0>	N8	AD0	
PCI_AD<1>	M7	AD1	
PCI_AD<2>	L7	AD2	
PCI_AD<3>	N6	AD3	
PCI_AD<4>	K4	AD4	
PCI_AD<5>	M6	AD5	
PCI_AD<6>	L6	AD6	
PCI_AD<7>	N5	AD7	
PCI_AD<8>	N4	AD8	
PCI_AD<9>	M2	AD9	
PCI_AD<10>	M5	AD10	
PCI_AD<11>	L4	AD11	
PCI_AD<12>	N3	AD12	
PCI_AD<13>	K5	AD13	
PCI_AD<14>	L5	AD14	
PCI_AD<15>	M4	AD15	
PCI_AD<16>	J4	AD16	
PCI_AD<17>	H1	AD17	
PCI_AD<18>	H3	AD18	
(PCI_AD<19>)	H2	AD19	
PCI_AD<20>	G2	AD20	
PCI_AD<21>	G4	AD21	
PCI_AD<22>	F1	AD22	
PCI_AD<23>	C3	AD23	
PCI_AD<24>	F3	AD24	
PCI_AD<25>	E2	AD25	
PCI_AD<26>	F4	AD26	
PCI_AD<27>	B1	AD27	
PCI_AD<28>	D2	AD28	
PCI_AD<29>	E4	AD29	
PCI_AD<30>	D3	AD30	
PCI_AD<31>	E3	AD31	
PCI_CBE<0>	K6	C/BE0*	
PCI_CBE<1>	M3	C/BE1*	
PCI_CBE<2>	J2	C/BE2*	
PCI_CBE<3>	A1	C/BE3*	
PCI_PAR	N1	PAR	
PCI_IRDY_L	K1	IRDY	
PCI_SERR_L	L2	SERR	
CBUS_PCI_IDSEL	F2	IDSEL	
PCI_PERR_L	K3	PERR	
PCI_FRAME_L	J1	FRAME	
PCI_STOP_L	L1	STOP	
PCI_TRDY_L	J3	TRDY	
PCI_DEVSEL_L	K2	DEVSEL	
CBUS_PCI_RESET_L	G3	PRST	
CBUS_PCI_REQ_L	C2	REQ	
CBUS_PCI_GNT_L	C1	GNT	
CLK33M_CBUS	G1	PCLK	
	M9	SPKROUT	
	M8	RI_OUT/PME	
CBUS_SUSPEND_PU	N10	SUSPEND	
CBUS_INT_L	K7	MFUNC0	
CBUS_MFUNC1_PD	N9	MFUNC1	
CBUS_MFUNC2_PD	L9	MFUNC2	
CBUS_MFUNC3_PD	K10	MFUNC3	
CBUS_MFUNC4_PD	M10	MFUNC4	
CBUS_MFUNC5_PD	N12	MFUNC5	
CBUS_MFUNC6_PD	L10	MFUNC6	
	L11	GRST	

CRITICAL
CLAMP FOR PC-CARD
CLAMP FOR PCI

VCCCB	B11	
VCCP	L3	
VCCD0*	N13	CBUS_VCCD0_L
VCCD1*	L12	CBUS_VCCD1_L
VPPD0	K9	CBUS_VPPD0
VPPD1	M11	CBUS_VPPD1
CD1*/CCD1*	L13	CBUS_DET_1_L
CD2*/CCD2*	B5	CBUS_DET_2_L
IORD*/CAD13	F12	CBUS_IORD_L
IOWR*/CAD15	C11	CBUS_IOWR_L
OE*/CAD11	G10	CBUS_OE_L
CE1*/CC/BE0*	H13	CBUS_CE1_L
VS1*/CVS1	B2	CBUS_VS1
VS2*/CVS2	A9	CBUS_VS2
WE*/CGNT*	D13	CBUS_WE_L
RDY/IREQ*/CINT*	A6	CBUS_READY
RESET/CRST*	D8	CBUS_RESET_L
REG*/CC/BE3*	A8	CBUS_REG_L
BVD1/CSTSCHG/STSCHG*/RI*	C6	CBUS_BVD1_L
BVD2/SPKR*/CAUDIO	D6	CBUS_BVD2_L
INTEGRATED PULL-UP WP/IOIS16*/CCLKRUN*	A5	CBUS_WP_L
CE2/CAD10*	G13	CBUS_CE2_L
INPACK/CREQ*	B8	CBUS_INPACK_L
WAIT/CSERR*	B6	CBUS_WAIT_L
A0/CAD26	C7	CBUS_ADDR<0>
A1/CAD25	D7	CBUS_ADDR<1>
A2/CAD24	B7	CBUS_ADDR<2>
A3/CAD23	D10	CBUS_ADDR<3>
A4/CAD22	B12	CBUS_ADDR<4>
A5/CAD21	C8	CBUS_ADDR<5>
A6/CAD20	C9	CBUS_ADDR<6>
A7/CAD18	A12	CBUS_ADDR<7>
A8/CC/BE1*	E11	CBUS_ADDR<8>
A9/CAD14	F11	CBUS_ADDR<9>
A10/CAD9	G11	CBUS_ADDR<10>
A11/CAD12	G12	CBUS_ADDR<11>
A12/CC/BE2*	D9	CBUS_ADDR<12>
A13/CPAR	E12	CBUS_ADDR<13>
A14/CPERR*	D12	CBUS_ADDR<14>
A15/CIRDY*	C10	CBUS_ADDR<15>
A16/CCLK	B13	CBUS_ADDR_16_UF
A17/CAD16	F10	CBUS_ADDR<17>
A18/RSVD	E13	CBUS_ADDR<18>
A19/CBLOCK*	A13	CBUS_ADDR<19>
A20/CSTOP*	E10	CBUS_ADDR<20>
A21/CDEVSEL*	D11	CBUS_ADDR<21>
A22/CTRDY*	C12	CBUS_ADDR<22>
A23/CFRAME*	A10	CBUS_ADDR<23>
A24/CAD17	B10	CBUS_ADDR<24>
A25/CAD19	B9	CBUS_ADDR<25>
D0/CAD27	A4	CBUS_DATA<0>
D1/CAD29	C4	CBUS_DATA<1>
D2/RSVD	A3	CBUS_DATA<2>
D3/CAD0	K11	CBUS_DATA<3>
D4/CAD1	K12	CBUS_DATA<4>
D5/CAD3	J13	CBUS_DATA<5>
D6/CAD5	J10	CBUS_DATA<6>
D7/CAD7	H12	CBUS_DATA<7>
D8/CAD28	C5	CBUS_DATA<8>
D9/CAD30	B4	CBUS_DATA<9>
D10/CAD31	B3	CBUS_DATA<10>
D11/CAD2	M12	CBUS_DATA<11>
D12/CAD4	J11	CBUS_DATA<12>
D13/CAD6	K13	CBUS_DATA<13>
D14/RSVD	J12	CBUS_DATA<14>
D15/CAD8	H11	CBUS_DATA<15>

R724 47 5% 1/16W MF 402 — CBUS_ADDR<16>

R723 47 5% 1/16W MF 402 — MAIN_RESET_L

RP1 10K 5% 1/32W 25V SM

CBUS_MFUNC1_PD
CBUS_MFUNC2_PD
CBUS_MFUNC3_PD
CBUS_MFUNC4_PD
CBUS_MFUNC5_PD
CBUS_MFUNC6_PD

GND
A2 A11 D1 F13 H4 K8 M13 N2

PC CARD/CARDBUS CONNECTOR

CRITICAL
J5
QT500806-L111
M-ST-SM1

CBUS_DET_1_L	4	3	CBUS_DATA<4>
CBUS_DATA<11>	6	5	CBUS_DATA<5>
CBUS_DATA<12>	8	7	CBUS_DATA<6>
CBUS_DATA<13>	10	9	
	12	11	CBUS_DATA<7>
CBUS_DATA<14>	14	13	CBUS_CE1_L
CBUS_DATA<15>	16	15	CBUS_ADDR<10>
CBUS_CE2_L	18	17	CBUS_OE_L
CBUS_VS1	20	19	
	22	21	CBUS_ADDR<11>
CBUS_IORD_L	24	23	CBUS_ADDR<9>
CBUS_IOWR_L	26	25	CBUS_ADDR<8>
CBUS_ADDR<17>	28	27	CBUS_ADDR<13>
CBUS_ADDR<18>	30	29	
	32	31	CBUS_ADDR<14>
CBUS_ADDR<19>	34	33	CBUS_WE_L
CBUS_ADDR<20>	36	35	CBUS_READY
CBUS_ADDR<21>	38	37	+VCC_CBUS_SW
+VCC_CBUS_SW	40	39	
	42	41	+VPP_CBUS_SW
+VPP_CBUS_SW	44	43	CBUS_ADDR<16>
CBUS_ADDR<22>	46	45	CBUS_ADDR<15>
CBUS_ADDR<23>	48	47	CBUS_ADDR<12>
CBUS_ADDR<24>	50	49	
	52	51	CBUS_ADDR<7>
CBUS_ADDR<25>	54	53	CBUS_ADDR<6>
CBUS_VS2	56	55	CBUS_ADDR<5>
CBUS_RESET_L	58	57	CBUS_ADDR<4>
CBUS_WAIT_L	60	59	
	62	61	CBUS_ADDR<3>
CBUS_INPACK_L	64	63	CBUS_ADDR<2>
CBUS_REG_L	66	65	CBUS_ADDR<1>
CBUS_BVD2_L	68	67	CBUS_ADDR<0>
CBUS_BVD1_L	70	69	
	72	71	CBUS_DATA<0>
CBUS_DATA<8>	74	73	CBUS_DATA<1>
CBUS_DATA<9>	76	75	CBUS_DATA<2>
CBUS_DATA<10>	78	77	CBUS_WP_L
CBUS_DET_2_L	80	79	
	83	82	

TI REFERENCE SCHEMATIC DID NOT HAVE BULK ON +VCC_CBUS_SW

C796 2.2uF 10% 10V CERM 805
C800 2.2uF 10% 10V CERM 805

CARDBUS

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	B
SCALE: NONE	SHT 18 OF 44	

SIL1162 DVI-Compliant Transmitter

Ext. TMDS source termination

M11 AGP INTERFACE

SPREAD SPECTRUM SUPPORT

S0=1;S1=M => -1.5% DOWN-SPREAD

27M OSC

(PLACE THE OSCILLATOR AND R304 AND R305 CLOSE TO ATI PIN AJ29)

(PLACE C408 CLOSE TO AGPREF PIN)

(PLACE R315 CLOSE TO OSC)

(SET TO LOW SWING MODE)

(PULL-UP to GPU_MEM_IO)

MAIN_RESET_L IS TOGGLED FOR SLEEP

PLACE VERF VOLTAGE DIVIDER CLOSE TO ATI M11 VREF PIN

PLL NOISE SHOULD BE LESS THAN 100mV PEAK-TO-PEAK

Place C879 close to SI pin#2

FOR 2.5 VDDR1
MEMVMODE0=1.8V
MEMVMODE1=GND

FOR 1.8 VDDR1
MEMVMODE0=GND
MEMVMODE1=1.8V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0318	197S0048		G1	Alt. for Siward Part

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	B
SCALE: NONE	SHT 19 OF 44	

Int.TMDS Termination

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN
CMF LINE SHOULD BE ROUTED AS 4MIL SURFACE
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS

GPU_TMDS_CLK_CMF
R374 49.9 1% 1/16W MF 402 — GPU_TMDS_CLKP
R377 49.9 1% 1/16W MF 402 — GPU_TMDS_CLKN
C536 470pF 10% 50V CERM 402
C572 470pF 10% 50V CERM 402

GPU_TMDS_D0_CMF
R367 75 1% 1/16W MF 402 — GPU_TMDS_D0P
R369 75 1% 1/16W MF 402 — GPU_TMDS_D0N
C511 470pF 10% 50V CERM 402
C507 470pF 10% 50V CERM 402

GPU_TMDS_D1_CMF
R362 75 1% 1/16W MF 402 — GPU_TMDS_D1P
R355 75 1% 1/16W MF 402 — GPU_TMDS_D1N
C487 470pF 10% 50V CERM 402
C497 470pF 10% 50V CERM 402

GPU_TMDS_D2_CMF
R350 75 1% 1/16W MF 402 — GPU_TMDS_D2P
R340 75 1% 1/16W MF 402 — GPU_TMDS_D2N
C479 470pF 10% 50V CERM 402
C469 470pF 10% 50V CERM 402

R765 0 5% 1/16W MF 402 — GPU_TMDS_DN<0> — ATI_TMDS_DN<0>
R767 0 5% 1/16W MF 402 — GPU_TMDS_DP<0> — ATI_TMDS_DP<0>
R760 0 5% 1/16W MF 402 — GPU_TMDS_DN<1> — ATI_TMDS_DN<1>
R762 0 5% 1/16W MF 402 — GPU_TMDS_DP<1> — ATI_TMDS_DP<1>
R764 0 5% 1/16W MF 402 — GPU_TMDS_DN<2> — ATI_TMDS_DN<2>
R766 0 5% 1/16W MF 402 — GPU_TMDS_DP<2> — ATI_TMDS_DP<2>
R761 0 5% 1/16W MF 402 — GPU_TMDS_CLKN — ATI_TMDS_CLKN
R763 0 5% 1/16W MF 402 — GPU_TMDS_CLKP — ATI_TMDS_CLKP

Place all TMDS 10 ohms close to GPU

+1_8V_GPU — R389 10K 5% 1/16W MF 402 — EXT TMDS R840 10K 5% 1/16W MF 402 — +3V_GPU
ZV_LCDDATA20_PU

R378 1K 5% 1/16W MF 402

NO STUFF R380 10K 5% 1/16W MF 402 — HPD_PWR_SNS_EN

R351 1K 1% 1/16W MF 402 — ATI_TESTEN

R558 10K 5% 1/16W MF 402 — GPU_VCORE_SEQ_L
R555 33K 5% 1/16W MF 402 — GPU_VCORE_SEQ
Q52 2N3904 SM
R559 100K 5% 1/16W MF 402 — +1_5V_AGP
R556 100K 5% 1/16W MF 402 — GPU_VCORE_PWR_SEQ
DP7 BAS16TW SOT-363 — SLEEP_L
DP7 BAS16TW SOT-363 — DCDC_EN
Q51 2N3904 SM

U47 ATI 64MB CRITICAL
RAGE MOBILITY M11-CSP64 64MB BGA (3 OF 6)

ATI_DVOD<0>	AJ5	ZV_LCDDATA0
ATI_DVOD<1>	AK5	ZV_LCDDATA1
ATI_DVOD<2>	AG6	ZV_LCDDATA2
ATI_DVOD<3>	AH6	ZV_LCDDATA3
ATI_DVOD<4>	AJ6	ZV_LCDDATA4
ATI_DVOD<5>	AK6	ZV_LCDDATA5
ATI_DVOD<6>	AG7	ZV_LCDDATA6
ATI_DVOD<7>	AH7	ZV_LCDDATA7
ATI_DVOD<8>	AJ7	ZV_LCDDATA8
ATI_DVOD<9>	AK7	ZV_LCDDATA9
ATI_DVOD<10>	AG8	ZV_LCDDATA10
ATI_DVOD<11>	AH8	ZV_LCDDATA11
NC	AJ8	ZV_LCDDATA12
NC	AK8	ZV_LCDDATA13
NC	AG9	ZV_LCDDATA14
NC	AH9	ZV_LCDDATA15
NC	AJ9	ZV_LCDDATA16
NC	AK9	ZV_LCDDATA17
NC	AG10	ZV_LCDDATA18
NC	AH10	ZV_LCDDATA19
NC	AJ10	ZV_LCDDATA20
NC	AK10	ZV_LCDDATA21
NC	AG11	ZV_LCDDATA22
NC	AH11	ZV_LCDDATA23
ATI_DVO_VSYNC	AJ4	ZV_LCDCNTL0
ATI_DVO_HSYNC	AK4	ZV_LCDCNTL1
ATI_DVOD_DE	AH5	ZV_LCDCNTL2
ATI_DVO_CLKP	AG5	ZV_LCDCNTL3
ATI_AGP_FBSKEW<0>	AJ2	GPIO0
ATI_AGP_FBSKEW<1>	AK2	GPIO1
ATI_X1CLK_SKEW<0>	AK1	GPIO2
ATI_X1CLK_SKEW<1>	AH3	GPIO3
ATI_BUS_CFG<0>	AH2	GPIO4
ATI_BUS_CFG<1>	AJ1	GPIO5
ATI_BUS_CFG<2>	AF4	GPIO6
ATI_GPIO7_SPN	AH1	GPIO7
ATI_GPIO8_PD	AG3	GPIO8
ATI_GPIO9_SPN	AF3	GPIO9
ATI_GPIO10_SPN	AG2	GPIO10
ATI_GPIO11_SPN	AF2	GPIO11
ATI_GPIO12_SPN	AG1	GPIO12
ATI_GPIO13_SPN	AF1	GPIO13
HPD_PWR_SNS_EN	AE2	GPIO14
GPU_VCORE_CNTL_L	AE1	GPIO15
ATI_SSCLK_IN	M1	GPIO16
ATI_TMDS_DN<0>	AJ13	TX0M
ATI_TMDS_DP<0>	AK13	TX0P
ATI_TMDS_DN<1>	AJ14	TX1M
ATI_TMDS_DP<1>	AK14	TX1P
ATI_TMDS_DN<2>	AJ15	TX2M
ATI_TMDS_DP<2>	AK15	TX2P
ATI_TMDS_CLKN	AJ12	TXCM
ATI_TMDS_CLKP	AK12	TXCP
ATI_CLK27M_IN	AJ29	XTALIN
NC	AJ30	XTALOUT
NC	AH24	TESTEN
NC	AJ26	SSIN
	B24	VSS
	B20	VSS
	A24	VSS

ROMCSB	AE5	NC
R	AK28	GPU_R
G	AK27	GPU_G
B	AK26	GPU_B
VSYNC	AG27	ATI_VSYNC
V2SYNC	AG25	NC
HSYNC	AG26	ATI_HSYNC
H2SYNC	AG24	NC
RSET	AK25	ATI_RSET
R2SET	AJ24	ATI_R2SET
Y_G	AK23	GPU_Y
C_R	AK24	GPU_C
COMP_B	AK22	GPU_COMP
DIGON	AE13	FP_PWR_EN
BLON	AF13	INV_ON_PWM
HPD1	AF11	GPU_HPD
AUXWIN	AJ27	AUXWIN_PU
DDC1DATA	AH28	GPU_DVI_DDC_DATA
DDC1CLK	AH27	GPU_DVI_DDC_CLK
DDC2DATA	AE12	LVDS_DDC_DATA
DDC2CLK	AF12	LVDS_DDC_CLK
DDC3DATA	AH26	SI_I2S_DATA
DDC3CLK	AH25	SI_I2C_CLK
TXOUT_U0N	AH18	LVDS_U0N
TXOUT_U0P	AG18	LVDS_U0P
TXOUT_U1N	AH19	LVDS_U1N
TXOUT_U1P	AG19	LVDS_U1P
TXOUT_U2N	AH20	LVDS_U2N
TXOUT_U2P	AG20	LVDS_U2P
TXOUT_U3N	AH22	LVDS_U3N_TP (NO ICT TEST)
TXOUT_U3P	AG22	LVDS_U3P_TP (NO ICT TEST)
TXCLK_UN	AH21	CLKLVDS_UN
TXCLK_UP	AG21	CLKLVDS_UP
TXOUT_L0N	AK16	LVDS_L0N
TXOUT_L0P	AJ16	LVDS_L0P
TXOUT_L1N	AK17	LVDS_L1N
TXOUT_L1P	AJ17	LVDS_L1P
TXOUT_L2N	AK18	LVDS_L2N
TXOUT_L2P	AJ18	LVDS_L2P
TXOUT_L3N	AK20	LVDS_L3N_TP (NO ICT TEST)
TXOUT_L3P	AJ20	LVDS_L3P_TP (NO ICT TEST)
TXCLK_LN	AK19	CLKLVDS_LN
TXCLK_LP	AJ19	CLKLVDS_LP
SSOUT	AJ25	NC
VSS	A20	
VSS	B21	

+1_5V_AGP — CRITICAL Q23 SI3446DV TSOP — GPU_CORE_OK — +GPU_VDD15_UF
C407 1000pF 10% 25V X7R 402

NO STUFF R346 75 1% 1/16W MF 402 — ATI_VSYNC
NO STUFF R342 75 1% 1/16W MF 402 — ATI_HSYNC
NO STUFF R341 75 1% 1/16W MF 402

R332 715 1% 1/16W MF 402 — R333 499 1% 1/16W MF 402 — GPU_VCORE
R359 75 1% 1/16W MF 402 — GPU_Y
R356 75 1% 1/16W MF 402 — GPU_C
R360 75 1% 1/16W MF 402 — GPU_COMP

+3V_GPU — R779 10K 5% 1/16W MF 402 — FP_PWR_EN
R366 10K 5% 1/16W MF 402 — INV_ON_PWM
R368 10K 5% 1/16W MF 402 — GPU_HPD

M10 Power Shut down Sequencing

+2_5V_SLEEP — XW11 SM — DP5 BAS16TW SOT-363 — +2_5V_SLEEP_NECK — XW9 SM
+1_8V_ATI_PVDD — +1_8V_PVDD_NECK
XW12 SM — DP5 BAS16TW SOT-363 — +1_5V_AGP_NECK — XW4
GPU_VCORE — GPU_VCORE_NECK
XW5 SM — DP5 BAS16TW SOT-363 — +GPU_VDD15_UF — +GPU_VDD15_NECK

U47 ATI 64MB CRITICAL
RAGE MOBILITY M11-CSP64 64MB BGA (5 OF 6)

VDD15	F12	
	L6	
	T6	
	AB6	
	F17	
	G25	
	R25	
	AB25	
	AJ3	
	AF25	
	AG4	
	AH4	
	AF5	
	F6	
	G6	
	H6	
	P6	
	AD26	
VDDC	V6	
	W6	
	AC6	
	AD6	
	AE6	
	F7	
	F10	
	AE10	
	F11	
	AE11	
	F13	
	F14	
	AE14	
	AF14	
	W26	
	AF15	
	AE17	
	AC25	
	AE18	
	F23	
	F24	
	AE24	
	F25	
	M25	
	N25	
	W25	
	V25	
VSS	G7	
	G8	
	G9	
	G10	
	G11	
	G12	
	G13	
	G14	
	G15	
	G16	
	G17	
	G18	
	G19	
	G20	
	G21	
	G22	
	G23	
	G24	
	H7	
	H8	
	H23	
	H24	
	J7	
	J24	
	K7	
	K24	
	L7	
	L24	
	M7	
	M24	
	N7	
	N24	
	P7	
	P24	
	R7	
	R24	
	T7	
	T24	
	U7	
	U24	
	V7	
	V24	
	W7	
	W24	
	Y7	
	Y24	
	AA7	
	AA24	
	AB7	
	AB24	
	AC7	
	AC8	
	AC23	
	AC24	
	AD7	
	AD8	
	AD9	
	AD10	
	AD11	
	AD12	
	AD13	
	AD14	
	AD15	
	AD16	
	AD17	
	AD18	
	AD19	
	AD20	
	AD21	
	AD22	
	AD23	

GPU VCORE - 1.2V

(PUT ALL CAPs BELOW ATI ASIC)

+1_5V_GPU_VDD15 (500mA)

C448 0.01uF 20% 16V CERM 402
C443 0.01uF 20% 16V CERM 402
C435 0.01uF 20% 16V CERM 402
C482 0.01uF 20% 16V CERM 402
C411 10uF 20% 6.3V CERM 805
C505 0.01uF 20% 16V CERM 402
C532 0.01uF 20% 16V CERM 402
C529 0.01uF 20% 16V CERM 402
C526 0.01uF 20% 16V CERM 402

C484 10uF 20% 6.3V CERM 805
C485 10uF 20% 6.3V CERM 805
C440 0.22uF 20% 6.3V CERM 402
C441 0.22uF 20% 6.3V CERM 402
C445 0.22uF 20% 6.3V CERM 402
C446 0.22uF 20% 6.3V CERM 402
C449 0.22uF 20% 6.3V CERM 402
C434 0.22uF 20% 6.3V CERM 402
C452 0.22uF 20% 6.3V CERM 402
C451 0.22uF 20% 6.3V CERM 402
C494 0.22uF 20% 6.3V CERM 402
C498 0.22uF 20% 6.3V CERM 402
C509 0.22uF 20% 6.3V CERM 402
C510 0.22uF 20% 6.3V CERM 402
C512 0.22uF 20% 6.3V CERM 402
C513 0.22uF 20% 6.3V CERM 402
C524 0.22uF 20% 6.3V CERM 402
C525 0.22uF 20% 6.3V CERM 402
C528 0.22uF 20% 6.3V CERM 402
C531 0.22uF 20% 6.3V CERM 402
C533 0.22uF 20% 6.3V CERM 402
C477 0.22uF 20% 6.3V CERM 402
C486 0.22uF 20% 6.3V CERM 402
C495 0.22uF 20% 6.3V CERM 402

+3V_GPU

R384 10K 5% 1/16W MF 402
R387 10K 5% 1/16W MF 402
NO STUFF R386 10K 5% 1/16W MF 402
NO STUFF R382 10K 5% 1/16W MF 402
NO STUFF R383 10K 5% 1/16W MF 402
NO STUFF R385 10K 5% 1/16W MF 402
NO STUFF R381 10K 5% 1/16W MF 402

(GPIO0)	ATI_AGP_FBSKEW<0>
(GPIO1)	ATI_AGP_FBSKEW<1>
(GPIO2)	ATI_X1CLK_SKEW<0>
(GPIO3)	ATI_X1CLK_SKEW<1>
(GPIO4)	ATI_BUS_CFG<0>
(GPIO5)	ATI_BUS_CFG<1>
(GPIO6)	ATI_BUS_CFG<2>

NO STUFF R393 10K 5% 1/16W MF 402
R396 10K 5% 1/16W MF 402
R395 10K 5% 1/16W MF 402
R391 10K 5% 1/16W MF 402
R392 10K 5% 1/16W MF 402
R394 10K 5% 1/16W MF 402
NO STUFF R390 10K 5% 1/16W MF 402

GPU VCORE SUPPLY

WHEN VCORE_CNTL HIGH => 1.2V
1.2V = 0.8V * (1 + R329 / (R328//R330))
WHEN VCORE_CNTL LOW => 1.0V
1.0V = 0.8V * (1 + R329 / R330)

+PBUS
+5V_MAIN

R327 1M 1% 1/16W MF 402
R331 1K 1% 1/16W MF 603
R326 576K 1% 1/16W MF 402
R343 0 5% 1/16W MF 402
NO STUFF R352 63.4K 1% 1/16W MF 402
C466 4.7uF 20% 25V CERM 1206 — 1778_GND
R357 100K 5% 1/16W MF 402 — 1778_SHDN_L
R339 20K 1% 1/16W MF 402 — 1778_ITH_RC
C455 470pF 10% 50V CERM 402
C465 220pF 5% 25V CERM 402
NO STUFF R344 0 5% 1/16W MF 402
NO STUFF R353 0 5% 1/16W MF 402
C480 0.1uF 20% 10V CERM 402
C431 0.1uF 20% 25V CERM 603
C481 0.1uF 20% 25V CERM 603
D12 1N914 SOT23
R358 2.2 5% 1/16W MF 603 — 1778_BST_RC

U32 LTC1778 SSOP — EXT INT VIN VCC VCC
RUN/SS — 1778_ION
ITH — 1778_ITH
VRNG — 1778_VRNG
FCB — 1778_FCB
PGOOD — GPU_CORE_OK
SGND PGND
BOOST — 1778_BST
TG — 1778_TG
SW
BG — 1778_BG
VFB — 1778_VFB

NO STUFF C838 0.001uF 20% 50V CERM 402
OMIT XW6 SM

1778_VCC
1778_VIN

CRITICAL Q48 SI7860DP SO-8-PWRPK
CRITICAL Q49 IRF7832 SO-8
C706 4.7uF 20% 25V CERM 1206
C708 4.7uF 20% 25V CERM 1206

GPU_VCORE_SW — CRITICAL L64 2.1uH-11A SM
D29 MBRS130LT3

C704 22uF 20% 10V CERM 1210
CRITICAL C705 330uF 20% 6.3V TANT CASE-D4
CRITICAL C707 330uF 20% 6.3V TANT CASE-D4
CRITICAL C711 330uF 20% 6.3V TANT CASE-D4

GPU_VCORE
1778_VFB
R329 4.99K 1% 1/16W MF 402
R328 18.2K 1% 1/16W MF 402
R330 20K 1% 1/16W MF 402
R361 1.82K 1% 1/16W MF 402
HIGH_VCORE_DIVD
HIGH_VCORE

+5V_MAIN
R786 100K 5% 1/16W MF 402
C846 0.1uF 20% 10V CERM 402
GPU_VCORE_CNTL_RC
GPU_VCORE_CNTL
Q25 2N7002DW SOT-363
Q25 2N7002DW SOT-363
GPU_VCORE_CNTL
R549 10K 5% 1/16W MF 402
NO STUFF C712 0.1uF 20% 10V CERM 402

M11 CORE PWR/LVDS/TMDS

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	B
SCALE: NONE	SHT 20 OF 44	

GPU PLL - 1.8V

U34 MM1571J SOT-25A CRITICAL (150mA MAX)
+2_5V_SLEEP → VIN; VOUT → +1_8V_ATI_PVDD; GPU_CORE_OK → CONT; NOISE → ATI_PVDD_BYP; GND
C830 1uF 20% 10V CERM 603
C553 0.01uF 20% 16V CERM 402
R787 0 5% 1/16W MF 402 (+1_8V_PVDD_STD)
C552 10uF 20% 6.3V CERM 805
L20 FERR-220-OHM 0402 (+1_8V_GPU_PLL)
C418 10uF 20% 6.3V CERM 805
C414 0.1uF 20% 10V CERM 402
C413 0.01uF 20% 16V CERM 402 (21mA)
L19 FERR-220-OHM 0402 (+1_8V_GPU)
C427 10uF 20% 6.3V CERM 805
C453 0.01uF 20% 16V CERM 402
C450 0.01uF 20% 16V CERM 402 (+1_8V_GPU_AVDD, AVDD+VDDDI=75mA)

L23 FERR-220-OHM 0402 (+2_5V_SLEEP → +2_5V_GPU_A2VDD, 140mA)
C459 10uF 20% 6.3V CERM 805
C460 0.01uF 20% 16V CERM 402
C461 0.01uF 20% 16V CERM 402

L21 FERR-220-OHM 0402 (+1_8V_GPU → +1_8V_GPU_AVDDQ, 2mA)
C464 10uF 20% 6.3V CERM 805
C463 0.01uF 20% 16V CERM 402

L24 FERR-220-OHM 0402 (+1_8V_GPU → +1_8V_GPU_VDDDI, AVD+VDDDI=75mA)
C478 10uF 20% 6.3V CERM 805
C462 0.01uF 20% 16V CERM 402
C454 0.01uF 20% 16V CERM 402

L28 FERR-220-OHM 0402 (+2_5V_SLEEP → +2_5V_GPU_MCLK)
C511 10uF 20% 6.3V CERM 805
C527 0.01uF 20% 16V CERM 402
C472 0.01uF 20% 16V CERM 402

AGP 4X I/O - 1.5V

L18 FERR-10-OHM-500MA SM (+1_5V_AGP → +1_5V_AGP_GPU, 20mA)
C438 0.1uF 20% 10V CERM 402
C444 0.1uF 20% 10V CERM 402
C423 0.1uF 20% 10V CERM 402
C424 0.1uF 20% 10V CERM 402
C422 10uF 20% 6.3V CERM 805
C439 0.01uF 20% 16V CERM 402
C447 0.01uF 20% 16V CERM 402
C425 0.01uF 20% 16V CERM 402
C417 0.01uF 20% 16V CERM 402

MEMORY CORE - 2.5V

L25 FERR-220-OHM 0805 (+2_5V_SLEEP → +2_5V_GPU_MEMCORE, 1800mA)
C470 0.1uF 20% 10V CERM 402
C539 0.1uF 20% 10V CERM 402
C475 0.1uF 20% 10V CERM 402
C419 0.1uF 20% 10V CERM 402
C483 10uF 20% 6.3V CERM 805
C471 0.01uF 20% 16V CERM 402
C538 0.01uF 20% 16V CERM 402
C504 0.01uF 20% 16V CERM 402
C420 0.01uF 20% 16V CERM 402

LVDS PLL - 1.8V

L32 FERR-220-OHM 0402 (+1_8V_ATI_PVDD → +1_8V_GPU_PNLPLL, 40mA)
C493 10uF 20% 6.3V CERM 805
C468 0.01uF 20% 16V CERM 402

MEMORY PLL - 1.8V

L30 FERR-220-OHM 0402 (+1_8V_ATI_PVDD → +1_8V_GPU_MEMPLL)
C537 10uF 20% 6.3V CERM 805
C523 0.01uF 20% 16V CERM 402
C831 10uF 20% 6.3V CERM 805
C832 0.01uF 20% 16V CERM 402 (+1_8V_GPU_TP_PLL)

LVDS - 2.5V

L26 FERR-10-OHM-500MA SM (+2_5V_SLEEP → +2_5V_GPU_PNLIO, 350mA)
C499 10uF 20% 6.3V CERM 805
C500 0.01uF 20% 16V CERM 402
C473 0.01uF 20% 16V CERM 402

LVDS/TMDS - 1.8V

L29 FERR-220-OHM 0402 (+1_8V_GPU → +1_8V_GPU_PNLIO, 180mA)
C514 10uF 20% 6.3V CERM 805
C492 0.1uF 20% 10V CERM 402
C496 0.1uF 20% 10V CERM 402
C489 0.1uF 20% 10V CERM 402
C491 0.1uF 20% 10V CERM 402
C501 0.01uF 20% 16V CERM 402
C506 0.01uF 20% 16V CERM 402

+1_5V_SLEEP → R275 0 5% 1/10W FF 805 → +1_5V_AGP — 1.5V
+1_8V_SLEEP → R363 0 5% 1/10W FF 805 → +1_8V_GPU — 1.8V
+1_8V_SLEEP +2_5V_SLEEP → ATI_MEMIO_LO R312 0 5% 1/10W FF 805; ATI_MEMIO_HI R319 0 5% 1/10W FF 805 → GPU_MEM_IO — 1.8V / 2.5V
+3V_SLEEP → R379 0 5% 1/10W FF 805 → +3V_GPU — 3.3V

GPU POWER SOURCES - 1.5V, 1.8V, 2.5V & 3.3V

U47 RAGE MOBILITY M11-CSP64 64MB BGA (4 OF 6) ATI_64MB CRITICAL

PVSS AK29	PVDD
AVSSQ AF22	AVDD0
A2VSSQ AJ22	AVDD1
A2VSSN0 AE22	A2VDD0
A2VSSN1 AE23	A2VDD1
A2VSSN0 AE19	A2VDDQ
A2VSSN1 AE20	VDD1DI
VSS1DI AG23	VDD2DI
VSS2DI AF19	VDDRH0
VSSRH0 F20	VDDRH1
VSSRH1 M6	
VDDR1 F5, G5, H5, J5, K5, L5, M5, N5, P5, R5, T5, U5, V5, W5, Y5, AA5, AB5, AC5, AD5, G26, K6, R6, Y6, AA6, F8, F9, F15, F16, F21, F22, H25, J25, J26	
VDDR4 AF6, AE7, AF7, AE8, AF8, AE9, AF9, AE10, AF10	
VDDR3 AD25, AE25, AE26, AF26	
LPVSS AJ21	LPVDD AK21
TPVSS AJ11	TPVDD AK11
MPVSS A6	MPVDD A7
LVSSR0 AH16	LVDDR_18 AE16
LVSSR1 AG17	LVDDR_18 AF16
LVSSR2 AH17	LVDDR_25 AG16
LVSSR3 AF18	LVDDR_25 AF17
DVOVMODE AH12	TXVDDR0 AG12
TXVSSR1 AH13	TXVDDR1 AG13
TXVSSR2 AH14	TXVDDR2 AG14
TXVSSR3 AH15	TXVDDR3 AG15
VDDP K25, L25, T25, Y28, K27, AA25, K26, L26, M26, N26, P26, R26, T26, U26, V26, Y26, AA26, AB26, AC26	
VDDM E5, E6, E12, E13, E18, E19, E20, E26, F26	
VDDR1 E7, H26, E9, E10, E11, E14, E15, E16, E17, E21, E22, E23, E24, E25	

MEMORY I/O

L31 FERR-220-OHM 0805 (+2_5V_SLEEP → +2_5V_GPU_MEM_IO, 1200mA)
C551 10uF 20% 6.3V CERM 805
C421 0.1uF 20% 10V CERM 402
C456 0.1uF 20% 10V CERM 402
C488 0.1uF 20% 10V CERM 402
C517 0.1uF 20% 10V CERM 402
C546 0.1uF 20% 10V CERM 402
C545 0.1uF 20% 10V CERM 402
C544 0.1uF 20% 10V CERM 402
C543 0.1uF 20% 10V CERM 402
C541 0.1uF 20% 10V CERM 402
C436 0.1uF 20% 10V CERM 402
C437 0.1uF 20% 10V CERM 402
C540 0.1uF 20% 10V CERM 402
C547 0.1uF 20% 10V CERM 402
C542 0.1uF 20% 10V CERM 402

1.8V DVO POWER (EXT.TMDS)

U60 MM1571J SOT-25A CRITICAL (150mA MAX)
+2_5V_SLEEP → VIN; VOUT → +1_8V_ATI_TPVDD; GPU_CORE_OK → CONT; NOISE → ATI_TPVDD_BYP; GND
C833 1uF 20% 10V CERM 603
C834 0.01uF 20% 16V CERM 402
L75 FERR-220-OHM 0402 (+1_8V_GPU → +1_8V_GPU_TP_PLL)
R788 0 5% 1/16W MF 402 (+1_8V_TPVDD_STD)
C835 10uF 20% 6.3V CERM 805
GPU_MEM_IO

L81 FERR-10-OHM-500MA SM (+1_8V_GPU → +1_8V_GPU_DVO, EXT TMDS)
C535 10uF 20% 6.3V CERM 805
C519 0.1uF 20% 10V CERM 402
C534 0.1uF 20% 10V CERM 402
C521 0.1uF 20% 10V CERM 402
R843 0 5% 1/16W MF 402 (INT TMDS)

3.3V IO SUPPLY

(Max Current varies, depends on usage)

L33 FERR-10-OHM-500MA SM (+3V_GPU → +3V_GPU_FLT)
C550 10uF 20% 6.3V CERM 805
C518 0.1uF 20% 10V CERM 402
C520 0.1uF 20% 10V CERM 402
C430 0.1uF 20% 10V CERM 402
C880 0.1uF 20% 10V CERM 402
C881 0.1uF 20% 10V CERM 402
C426 0.1uF 20% 10V CERM 402
R842 0 5% 1/16W MF 402 (EXT TMDS)
R841 0 5% 1/16W MF 402 (INT TMDS)
ATI_DVOVMODE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0158	1	IC,ATI,M11-CSP128,GRAPHICTLR,667BGA	U47	CRITICAL	ATI_128MB

M11 POWER

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	B
SCALE: NONE	SHT 21 OF 44	

EXTERNAL VIDEO (DVI) INTERFACE

VGA SYNC BUFFERS

U40 74AHC1G32 SM
L38 OMIT FERR-60-OHM-0.1A 0402
U39 74AHC1G32 SM
L36 OMIT FERR-60-OHM-0.1A 0402

PLACE L1002 & L1003 CLOSE TO DVI CONNECTOR

TMDS FILTERING
PLACE CLOSE TO CONNECTOR

L45 90-OHM-300mA 2012H
L46 90-OHM-300mA 2012H
L47 90-OHM-300mA 2012H

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

L37 370-OHM SM

L50 0.068uH SM
L49 0.068uH SM
L44 0.068uH SM
L43 0.068uH SM
L41 0.068uH SM
L40 0.068uH SM

C642 4.7pF 5% 50V CERM 402
C641 3.3pF 0.25pF 50V CERM 402
C635 4.7pF 5% 50V CERM 402
C634 3.3pF 0.25pF 50V CERM 402
C632 4.7pF 5% 50V CERM 402
C631 3.3pF 0.25pF 50V CERM 402

R462 75 1% 1/16W MF 402
R458 75 1% 1/16W MF 402
R456 75 1% 1/16W MF 402

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)

F2 CRITICAL 0.5AMP-13.2V SM
L42 400-OHM-EMI SM-1

Isolation required for DVI power switch

D19 MBR0530 SM
R476 4.7K 5% 1/16W MF 402
R478 4.7K 5% 1/16W MF 402
R479 100 5% 1/16W MF 402
R477 100 5% 1/16W MF 402
R469 100 5% 1/16W MF 402

C654 100pF 5% 25V CERM 201
C655 100pF 5% 25V CERM 201
C653 100pF 5% 25V CERM 201
C667 0.01uF 20% 50V CERM 603

R464 0 5% 1/16W MF 402
PLACE NEAR C5A & C5B
R463 0 5% 1/16W MF 402
PLACE NEAR 3, 11 & 19

J22 CRITICAL QH1112 F-RT-TH

3V LEVEL SHIFTERS

Q39 2N7002DW SOT-363
Q39 2N7002DW SOT-363
Q40 2N7002DW SOT-363

R480 10K 5% 1/16W MF 402
R474 10K 5% 1/16W MF 402
R481 100K 5% 1/16W MF 402

NOTE: Pulldown for DVI_HPD provided by DVI power switch interface

DVI POWER SWITCH

Power key detect path when system is shutdown or asleep.. DDC_CLK is isolated from NV17M DURING SHUTDOWN. WHEN power key on remote device is pressed, 5V will be driven on DDC_CLK. since host rails will be low, TP0610 will turn on, driving SOFT_PWR_ON_L low. As host rails rise, TP0610 will turn off, as will remote device path to DDC_CLK. Isolation will be disabled as well.

Q38 TP0610 SM
R473 680 5% 1/16W MF 402
R460 10K 5% 1/16W MF 402
R459 330 5% 1/16W MF 402
Pulldown prevents 3904 from turning on when DVI monitor has active, self-powered DDC clock pullup.
Q35 MMDT3904 SOT-363

Power key detect path when system is running, HPD normally driven to 3.3v. When power key on remote device pressed, HPD will be driven to 5V. COMPARATOR ENABLED BY NV17M GPIO.

R485 68.1K 1% 1/16W MF 402
C668 0.1uF 10% 16V CERM 402
U42 LMC7211 SM
R472 10K 1% 1/16W MF 402
R484 100K 1% 1/16W MF 402
R482 10K 1% 1/16W MF 402
R475 10K 5% 1/16W MF 402
R470 330 5% 1/16W MF 402
Q40 2N7002DW SOT-363
R483 470K 5% 1/16W MF 402

LCD INTERFACE
LVDS INTERFACE

LCD POWER SWITCH

R347 100K 5% 1/16W MF 402
C474 2200pF 5% 50V CERM 603
R354 100K 5% 1/16W MF 402
Q28 2N7002 SM
Q29 TSOP SI3443DV
L27 FERR-250-OHM SM
C503 0.001uF 20% 50V CERM 402
C548 0.001uF 20% 50V CERM 402
C549 0.001uF 20% 50V CERM 402
J14 CRITICAL G-501973 F-RT-SM

R543 100K 5% 1/16W MF 402
R544 100K 5% 1/16W MF 402
C701 0.001uF 20% 50V CERM 402
C702 0.001uF 20% 50V CERM 402

100K pull-ups are for no-panel case (development)
Panel has 2K pull-ups
NO STUFF

INVERTER INTERFACE

L73 FERR-1K-OHM-EMI SM
L74 400-OHM-EMI SM-1
L72 400-OHM-EMI SM-1
Q76 FDG6324L SC70-6
Q76 FDG6324L SC70-6
R750 100K 5% 1/16W MF 402
C812 0.001uF 20% 50V CERM 402
C813 10uF 20% 6.3V CERM 805
C815 0.001uF 20% 50V CERM 402
C816 0.001uF 20% 50V CERM 402
C19 0.001uF 20% 50V CERM 402
C22 0.1uF 10% 16V CERM 402
L1 FERR-250-OHM SM
J4 CRITICAL SM-2MT
U2 NC7S32 SC70

INVERTER EXPECTS ACTIVE HIGH SIGNAL

R753 0 5% 1/16W MF 402
C819 0.01uF 20% 50V CERM 603

S-VIDEO/COMP OUT INTERFACE

Place GND shorts at graphics controller

XW15 SM
XW14 SM
L54 FERR-10-OHM-500MA SM
L56 FERR-10-OHM-500MA SM
L53 3.3uH 0603
L57 3.3uH 0603
L55 3.3uH 0603
C657 0.01uF 20% 50V CERM 603
C663 560pF 10% 50V CERM 402
C656 560pF 10% 50V CERM 402
C661 560pF 10% 50V CERM 402
C660 560pF 10% 50V CERM 402
C664 560pF 10% 50V CERM 402
C658 560pF 10% 50V CERM 402
C659 0.01uF 20% 50V CERM 603
J21 CRITICAL MINIDIN RT-TH MH11773-WMR8A

Place GND shorts at graphics controller

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S1331	2	DISCRETE,RES,33OHM,0402	L36,L38		VGA_BUFFER_RES

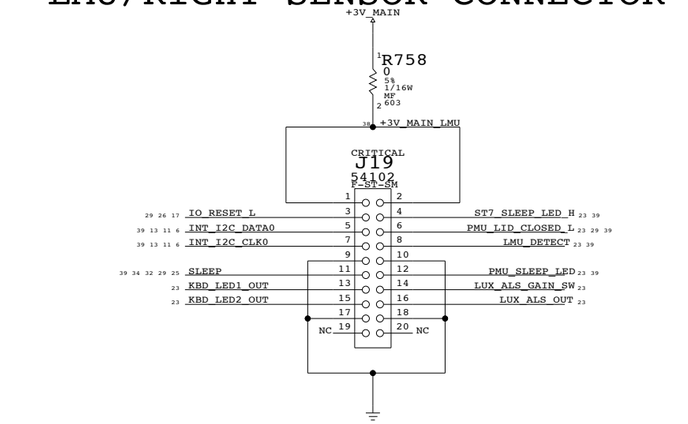
VIDEO CONNECTORS

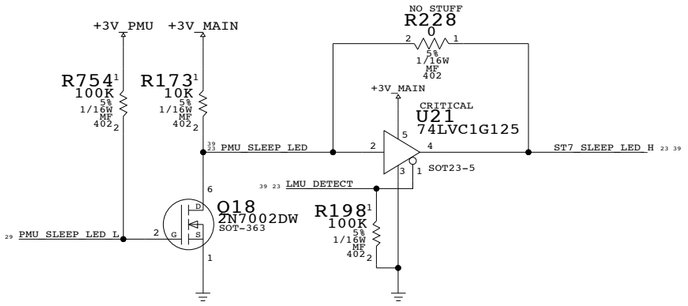
APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6570 | REV. B

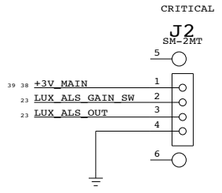
SCALE NONE | SHT 22 44

LMU/RIGHT SENSOR CONNECTOR

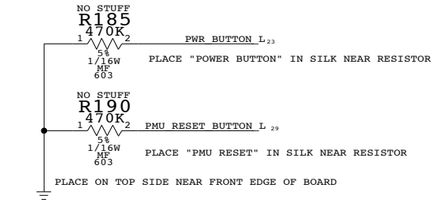




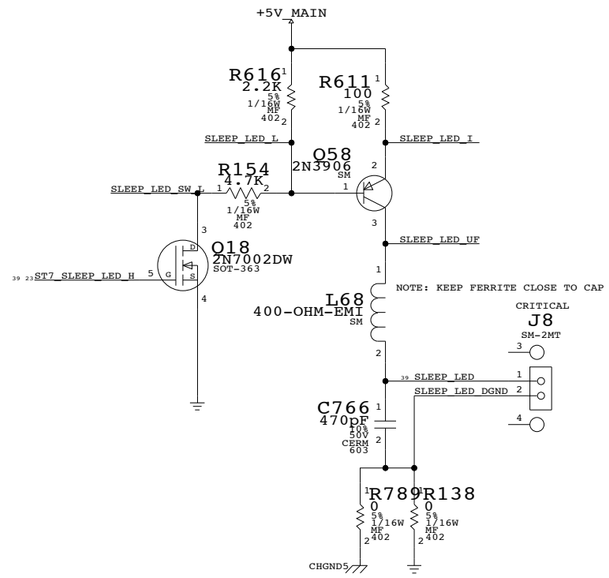
LEFT LIGHT SENSOR CONNECTOR



DEBUG HELPERS

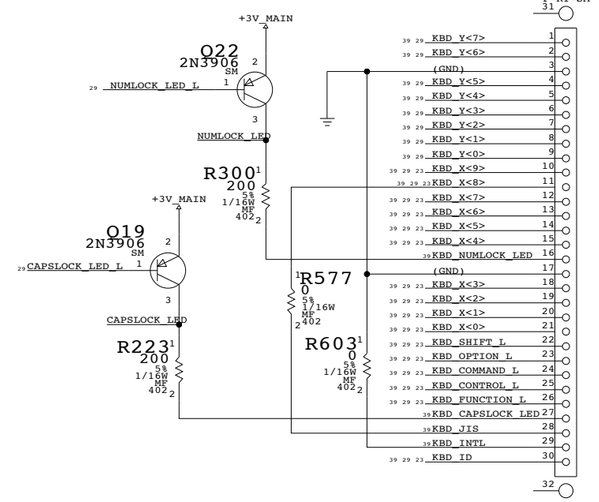


SLEEP LED

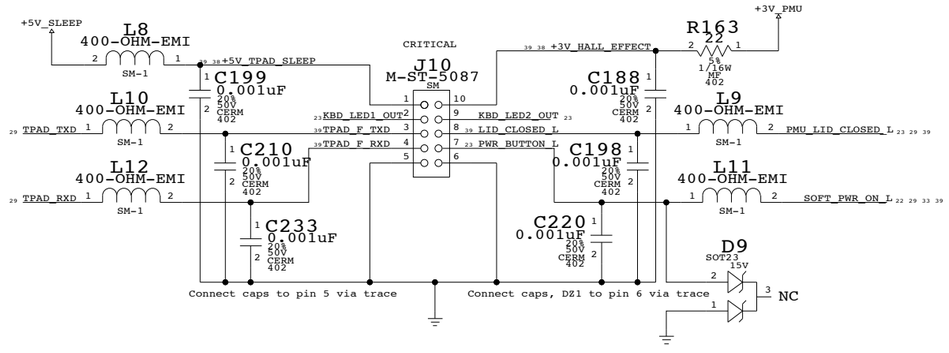


TOP CONTACT ZIF KEYBOARD CONN

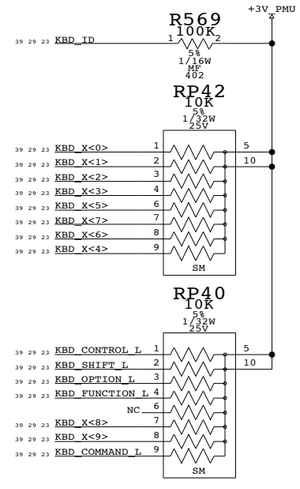
CONN,TOP CONTACT ZIF,0.8MM PITCH,30P,SM
Apple Part #: 518S0079
SMK Part #: CFP0630-0301



TRACKPAD/PWR BTN CONN



KEYBOARD PULLUPS



KEYBOARD/TPAD/SLEEP LED

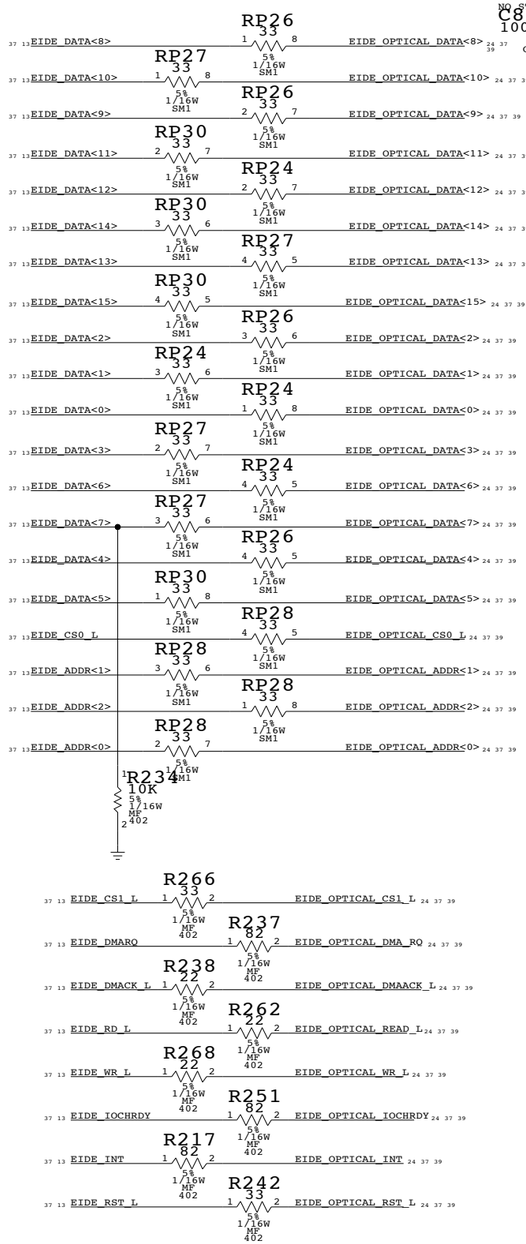
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	B
SCALE: NONE	SHT 23 OF 44	

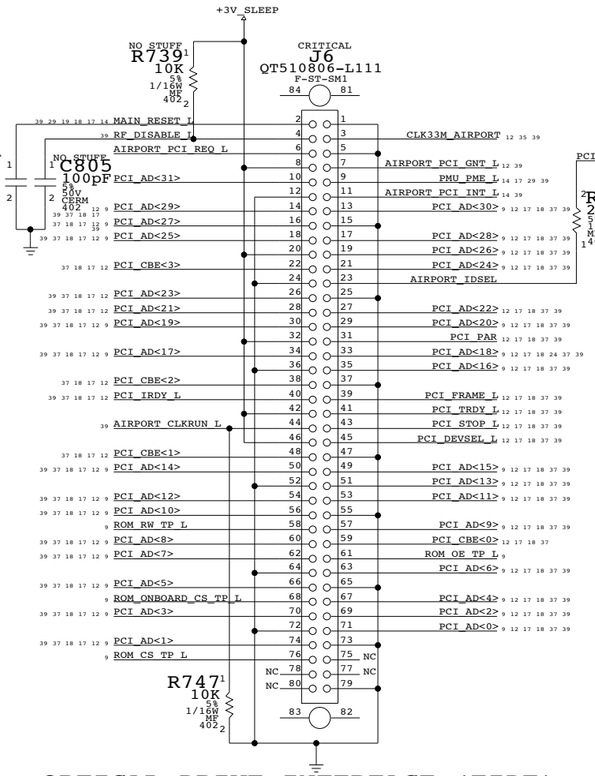
WIRELESS INTERFACE

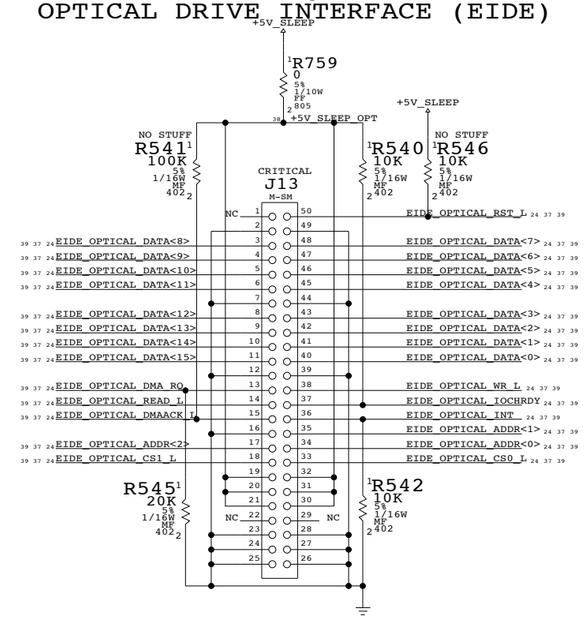
EIDE SERIES TERMINATION

PLACE TERMINATORS NEAR INTREPID



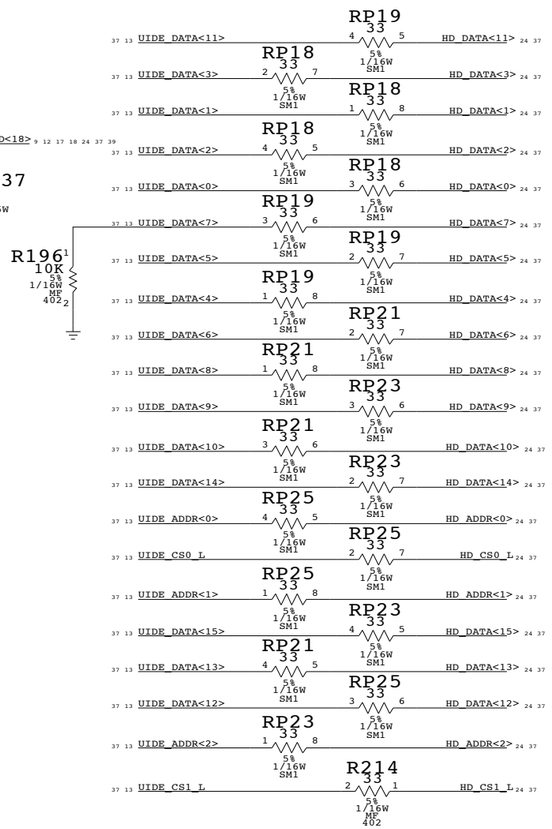
OPTICAL DRIVE INTERFACE (EIDE)

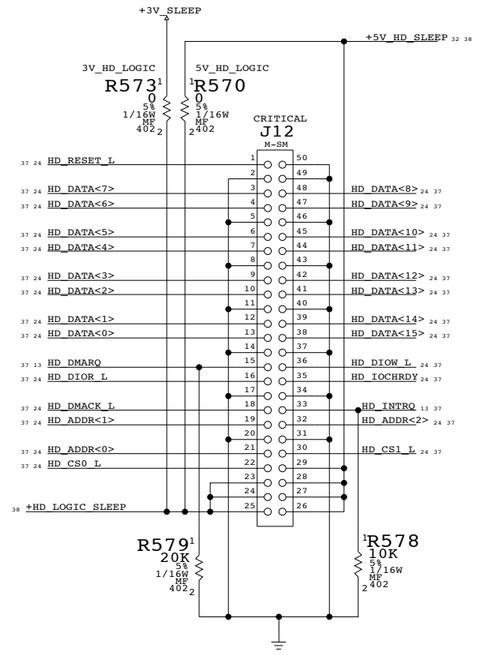




HARD DRIVE INTERFACE (UATA100)

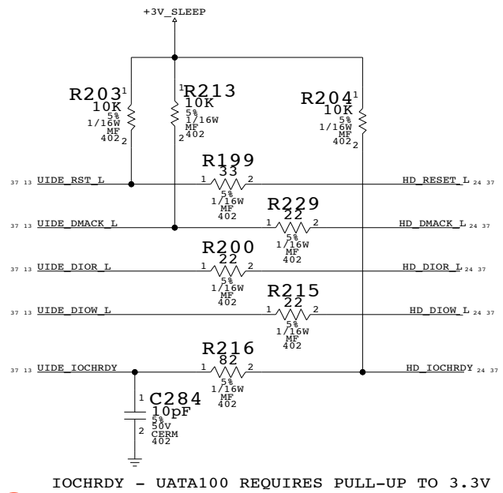
PLACE SERIES R CLOSE TO INTERPID





ANY SEQUENCING REQUIREMENT BETWEEN +5V_HD_SLEEP AND +3V_SLEEP

PLACE PULLUP RESISTORS CLOSE TO INTREPID



IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V

INTERNAL I/O CONNECTORS

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6570 | REV. B

SCALE NONE | SHT 24 OF 44

LEFT I/O & AUDIO BOARD (LIO)

CRITICAL
J3
QT500406-L111
M-ST-SM1

+5V_MAIN
+3V_MAIN

Place it near J3

ADAPTER_DET			
CHARGE_LED_L			
NEC_LUSB_PPON		NEC_USB_DAM	17 37 39
NEC_LUSB_OCI_UF		NEC_USB_DAP	17 37 39
BT_USB_DM		SLEEP	23 29 32 34 39
BT_USB_DP		INT_I2S0_SND_SCLK	39 14
		INT_I2S0_SND_FROM_ADC	14 39
INT_I2S0_SND_MCLK		SND_HW_RESET_L	14 39
		INT_I2C_CLK2	14 25 39
INT_I2S0_SND_LRCLK		INT_I2C_DATA2	14 25 39
INT_I2S0_SND_TO_DAC			
SND_HP_SENSE_L		SND_HP_MUTE_LO	25
SND_LIN_SENSE_L		SND_AMP_MUTE	25 39
		+3V_MAIN_AUD	32 38
		+5V_MAIN_AUD	32 38

C848 150uF 20% 6.3V TANT SMD-1

NO STUFF C818 0.001uF 50% 50V CERM 402

NO STUFF C817 0.001uF 20% 50V CERM 402

C828 0.1uF 20% 10V CERM 402

C829 0.1uF 20% 10V CERM 402

OMIT XW30 SM — AUD_GND

+5V_MAIN
R751 100K 5% 1/16W MF 402
SND_AMP_MUTE
Q77 2N7002DW SOT-363
SND_AMP_MUTE_L
SND_AMP_MUTE_CTRL
R752 100K 5% 1/16W MF 402
Q77 2N7002DW SOT-363
INT_PU_RESET_L

PREVENTS POWER-ON POP AND GENERATES ACTIVE HIGH SPKR MUTE

+3V_MAIN
R768 100K 5% 1/16W MF 402
R769 100K 5% 1/16W MF 402
SND_HP_MUTE_LO
Q78 2N7002DW SOT-363
SND_HP_MUTE
Q78 2N7002DW SOT-363
SND_HP_MUTE_L 14 39
R770 100K 5% 1/16W MF 402
SND_AMP_MUTE_CTRL

PREVENTS POWER-ON POP AND PROPAGATES ACTIVE LOW HP MUTE

PLACE CLOSE TO CPU
MAIN1

THERM1_M_DP — Q59 2N3904 SM — THERM1_M_DM

KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

R703 0 5% 1/16W MF 402 — THERM1_M_DP — THERM1_DP
R704 0 5% 1/16W MF 402 — THERM1_M_DM — THERM1_DM

PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY
MAIN2

THERM2_M_DP — Q46 2N3904 SM — THERM2_M_DM

R686 0 5% 1/16W MF 402 — THERM2_M_DP — THERM2_DP
R687 0 5% 1/16W MF 402 — THERM2_M_DM — THERM2_DM

PLACE UNDERNEATH UPPER RAM
ALTERNATE1

THERM1_A_DP — Q61 2N3904 SM — THERM1_A_DM

KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

NO STUFF R701 0 5% 1/16W MF 402 — THERM1_A_DP — THERM1_DP
NO STUFF R702 0 5% 1/16W MF 402 — THERM1_A_DM — THERM1_DM
NO STUFF R688 0 5% 1/16W MF 402 — THERM2_A_DP — THERM2_DP
NO STUFF R689 0 5% 1/16W MF 402 — THERM2_A_DM — THERM2_DM

PLACE CLOSE TO BATTERY CHARGER/VCORE
ALTERNATE2

THERM2_A_DP — Q67 2N3904 SM — THERM2_A_DM

USB MODEM/SOFT MODEM

+5V_MAIN — PLACE NEAR CONNECTOR PINS 15
C698 10uF 20% 6.3V CERM 805
NO STUFF C696 0.1uF 20% 10V CERM 402

+3V_MAIN — PLACE NEAR CONNECTOR PINS 16
C689 10uF 20% 6.3V CERM 805
NO STUFF C692 0.1uF 20% 10V CERM 402

+3V_MAIN
SOFT_MODEM
R778 10K 5% 1/16W MF 402
R530 10K 5% 1/16W MF 402
USB_MODEM
R776 0 5% 1/16W MF 402
COMM_SHUTDOWN

+5V_MAIN
+3V_MAIN
CRITICAL
J15
QT500166-L010
M-ST-SM1

INT_MOD_DTO		INT_MOD_SYNC	14
INT_MOD_CLKOUT		INT_MOD_DTI	14
		INT_MOD_BITCLK	14
	COMM_SHUTDOWN_PU		
39 14	COMM_RESET_L	MODEM_USB_DM	14 37 39
39 25 14	INT_I2C_DATA2	MODEM_USB_DP	14 37 39
39 25 14	INT_I2C_CLK2	COMM_RING_DET_L	14 29 39

USB MODEM I2C ADDR ASSIGNED VIA FLEX CABLE

FAN INTERFACE

FAN CONTROLLER

+3V_MAIN
R806 10 5% 1/16W MF 402
ADT7460_VCC
C849 1uF 10% 6.3V CERM 603
C763 0.1uF 20% 10V CERM 402

U53
ADT7460 QSOP CRITICAL
+2.5V/ SMBALERT#
SDA
SCL
D1+
D1-
D2+
D2-
GND
VCC
PWM1/ XTO
TACH1
PWM2/ SMBALERT#
TACH2
PWM3/ ADR ENABLE#
TACH3
TACH4/ ADR SELECT/ THERM#

ADT7460_VCORE_MON 14
INT_I2C_DATA1 16
INT_I2C_CLK1 1
THERM1_DP 13
THERM1_DM 12
THERM2_DP 11
THERM2_DM 10

C868 1000pF 10% 25V X7R 402
C869 1000pF 10% 25V X7R 402

+3V_SLEEP
R633 10K 5% 1/16W MF 402
R749 10K 5% 1/16W MF 402
R774 10K 5% 1/16W MF 402
R454 10K 5% 1/16W MF 402
R773 10K 5% 1/16W MF 402

FAN1_PWM_L 25
FAN1_TACH 25 39
FAN2_PWM_L
FAN2_TACH 25 39
ADT7460_ADR_ENABLE_L
ADT7460_TACH3_TP
ADT7460_THERM_L 25

CPU FAN

+5V_SLEEP
NO STUFF R771 10K 5% 1/16W MF 402
R547 0 5% 1/16W MF 805
CRITICAL
J1
SM04B-SSR
M-RT-SM

+FAN_PWR
FAN1_TACH
FAN1_PWM
Q79 2N7002DW SOT-363
FAN1_PWM_L 2
C669 4.7uF 20% 6.3V CERM 805

GPU FAN

+5V_SLEEP
NO STUFF R772 10K 5% 1/16W MF 402
CRITICAL
J18
SM04B-SSR
M-RT-SM

+FAN_PWR
FAN2_TACH
FAN2_PWM
Q79 2N7002DW SOT-363
FAN2_PWM_L 5
C814 4.7uF 20% 6.3V CERM 805

+3V_PMU_AVCC
R817 100K 5% 1/16W MF 402
THERM_L_OC 29

+3V_MAIN
R808 100K 5% 1/16W MF 402
THERM_INV
Q83 2N7002DW SOT-363
R807 100K 5% 1/16W MF 402
Q83 2N7002DW SOT-363
ADT7460_THERM_L
C850 0.1uF 20% 10V CERM 402

RIGHT USB BOARD

+5V_MAIN
CRITICAL
J17
QT500166-L010
M-ST-SM1

NEC_USB_DBM	39 37 17	NEC_RUSB_OCI_UF	17 39
NEC_USB_DBP	39 37 17	NEC_RUSB_PPON	17 39

SERIAL DEBUG INTERFACE

+5V_MAIN
NO STUFF
CRITICAL
J28
M-ST-5087
SM

COMM_TXD_L	39 14	COMM_DTR_L	14 39
COMM_TRXC	39 14	COMM_RTS_L	14 39
COMM_GPIO_L	39 14	COMM_RXD	14 39

FAN/MODEM/SOUND/BACKUP BATT.

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6570 | REV. B

SCALE NONE | SHT 25 OF 44

Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

PLACE ALL SERIES RES CLOSE TO PHY

R423 0 5% 1/16W MF 402
R421 0 5% 1/16W MF 402
R445 0 5% 1/16W MF 402
C851 10pF 5% 50V CERM 402 (NO STUFF)
C852 10pF 5% 50V CERM 402
Keep C851 & C852 Stubs short

CRITICAL
U43
88E1111
BCC

TX_CLK, RX_CLK, 125CLK, TXD0, TXD1, TXD2, TXD3, TXD4, TXD5, TXD6, TXD7, TX_EN, TX_ER, GTX_CLK, RXD0, RXD1, RXD2, RXD3, RXD4, RXD5, RXD6, RXD7, RX_DV, RX_ER, CRS, COL, MDC, MDIO, INT-/INT+, RESET, COMA, S_IN+, S_IN-, S_OUT+, S_OUT-, S_CLK+, S_CLK-, HSDAC+, HSDAC-, XTAL1, XTAL2, VSSC

CTRL10, DVDD, VDDO, VDDOH, VDDOX, AVDD, GND

+3V_MAIN
C680 10uF 20% 6.3V CERM 805
NO STUFF R513 0 5% 1/16W MF 402
R507 0 5% 1/16W MF 402
3405_MODE
U45 LTC3405 SOT23-6 (VIN, RUN, MODE, GND, SW, VFB)
LTC3405_SW
CRITICAL L60 3.3uH SM1
R506 665K 1% 1/16W MF 402 R2A
C675 22PF 5% 50V CERM 402
R504 49.9K 1% 1/16W MF 402 R2B
3405_VFB
R503 182K 1% 1/16W MF 402 R1
C674 10uF 20% 6.3V CERM 805
+1_0V_MARVELL

VOUT = 0.8V*(1+R2EQV/R1)
R2EQV = R2A||R2B

C594 0.1uF, C601 0.01uF, C608 0.1uF, C619 0.01uF, C603 0.1uF, C599 0.01uF (20% 10V CERM 402)
PLACE CAPS (IN ORDER) ON PINS 1, 6, 10/15, 57/62, 67/71, 85

C597 0.1uF, C612 0.01uF, C623 0.1uF, C600 0.01uF, C598 0.1uF (20% 10V CERM 402), C595 10uF 20% 6.3V CERM 805
PLACE CAPS (IN ORDER) ON PINS 5, 21/26, 48/52, 66/72, 88, 96

+2_5V_MARVELL
L35 FERR-EMI-600-OHM SM
+2_5V_MARVELL_AVDD

C614 0.1uF, C616 0.01uF, C618 0.1uF, C602 0.01uF, C592 10uF (20% 10V CERM 402)
PLACE CAPS (IN ORDER) ON PINS 32/35, 36/40, 45 & 78

+2_5V_MAIN
R442 0 5% 1/16W MF 603
C646 0.1uF, C648 0.1uF, C645 0.1uF, C647 0.1uF (20% 10V CERM 402)
PLACE CAPS AT CONNECTOR PINS 5 & 6

CRITICAL
J23
MJ-R0016
F-RT-TH

PRIMARY: 13, 11, 5 ENET_CTAP, 6 ENET_CTAP, 1 MDI_0+, 2 MDI_0-, 3 MDI_1+, 4 MDI_1-, 7 MDI_2+, 8 MDI_2-, 9 MDI_3+, 10 MDI_3-, 12, 14
RJ45 CHIP SIDE
CHGND1
1CT:1CT, 75 OHM
SECONDARY: J1, J2, J3, J4, J5, J6, J7, J8
RJ45 CABLE SIDE
SHIELD 1000PF, 2000V

ENET_ENERGY_DET
ENET_RST_L
ENET_COMA
ENET_HSDACP
ENET_HSDACM
ENET_VSSC
CLK25M_ENET_XIN
CLK25M_ENET_XOUT
ENET_RSET
LED_LINK10
LED_LINK100
LED_RX_SPN
INT_TDO
JTAG_ASIC_TDO_TP
JTAG_ASIC_TCK
JTAG_ASIC_TMS
JTAG_ASIC_TRST_L

R431 10K, R430 10K, R432 1.5K (5% 1/16W MF 402)
R422 1K 5% 1/16W MF 402
D15 1N914 SOT23
Q32 2N7002DW SOT-363 (AC_IN)
Q32 2N7002DW SOT-363 (SLEEP_L_LS5)
C611 2.2uF 20% 10V CERM 805
PLACES PHY IN "COMA" MODE WHEN ASLEEP ON BATTERY (SAVES POWER)

R425 20K 5% 1/16W MF 402 (NO STUFF)
PUT CRYSTAL CIRCUIT CLOSE TO PHY
R441 0 5% 1/16W MF 402
CRITICAL Y5 SM-3 25.0000M
C604 27PF 5% 50V CERM 402
C624 27PF 5% 50V CERM 402
Y6 LOAD CAPACITANCE IS 16PF

R424 49.9 1% 1/16W MF 402 (NO STUFF)
R429 49.9 1% 1/16W MF 402 (NO STUFF)
R428 10K 5% 1/16W MF 402
R427 4.99K 1% 1/16W MF 402

MDI0+, MDI0-, MDI1+, MDI1-, MDI2+, MDI2-, MDI3+, MDI3-

R433 49.9, R435 49.9, R437 49.9, R439 49.9 (1% 1/16W MF 402)
R434 49.9, R436 49.9, R438 49.9, R440 49.9 (1% 1/16W MF 402)
MDI0_PD, MDI1_PD, MDI2_PD, MDI3_PD
C622 0.01uF, C613 0.01uF, C615 0.01uF, C617 0.01uF (20% 16V CERM 402)
PLACE RESISTORS CLOSE TO PHY

SEE CONFIG TABLES (BELOW)

CONFIG0 (000)
CONFIG1 (000)
CONFIG2 (111)
CONFIG3 (110)
CONFIG4 (111)
CONFIG5 (101)
CONFIG6 (000)

CONFIG DEFINITIONS	
PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

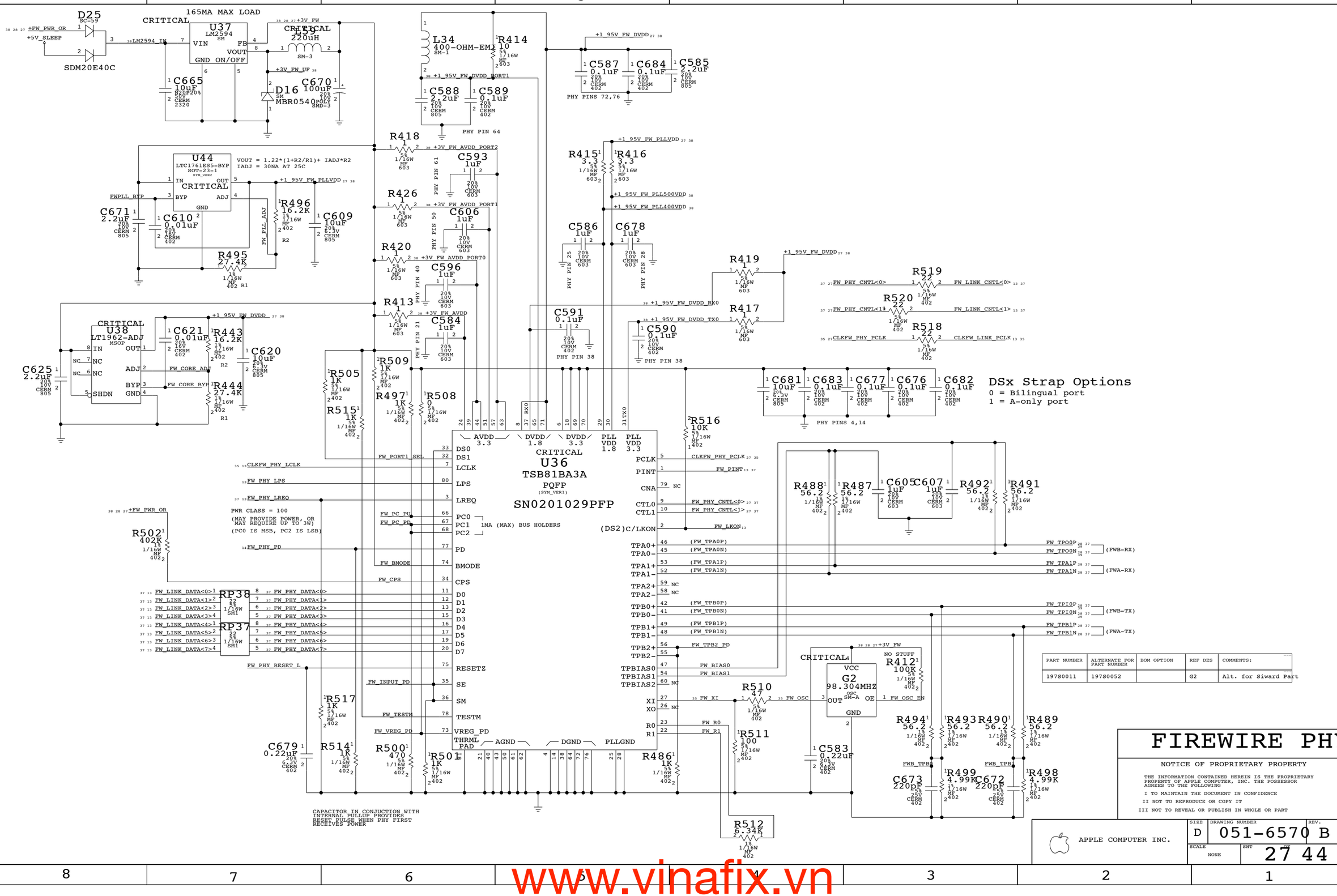
CONFIG INPUTS			
PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

MARVELL 88E1111

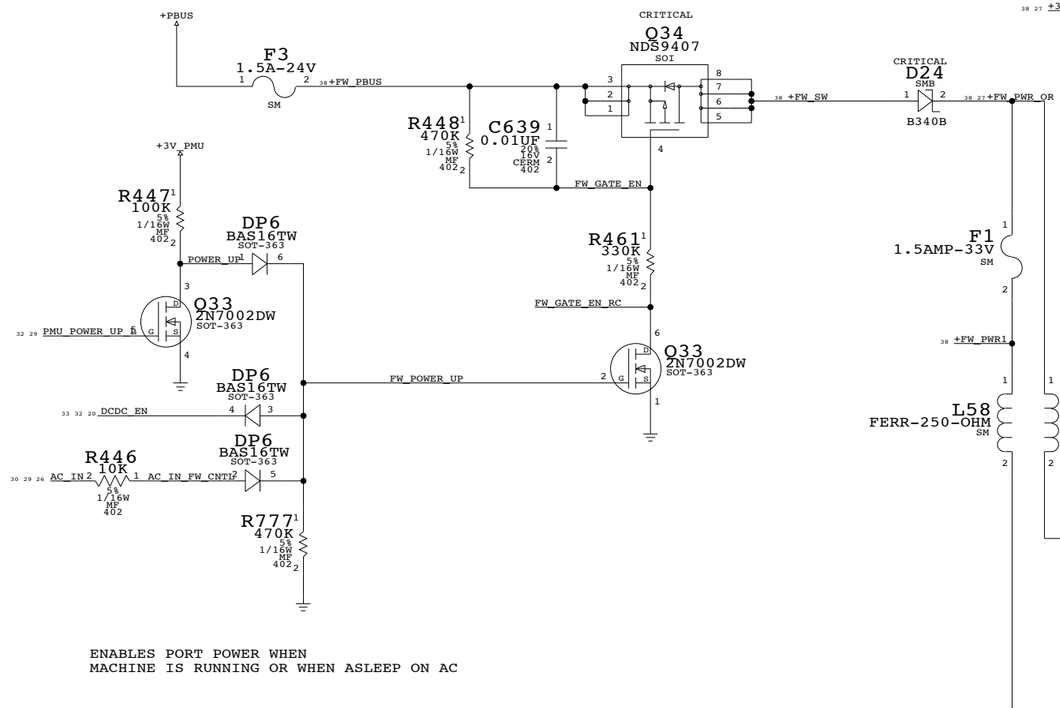
10/100/1000 ETHERNET

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6570 | REV. B
SCALE NONE | SHT 26 OF 44



PORT POWER SWITCH

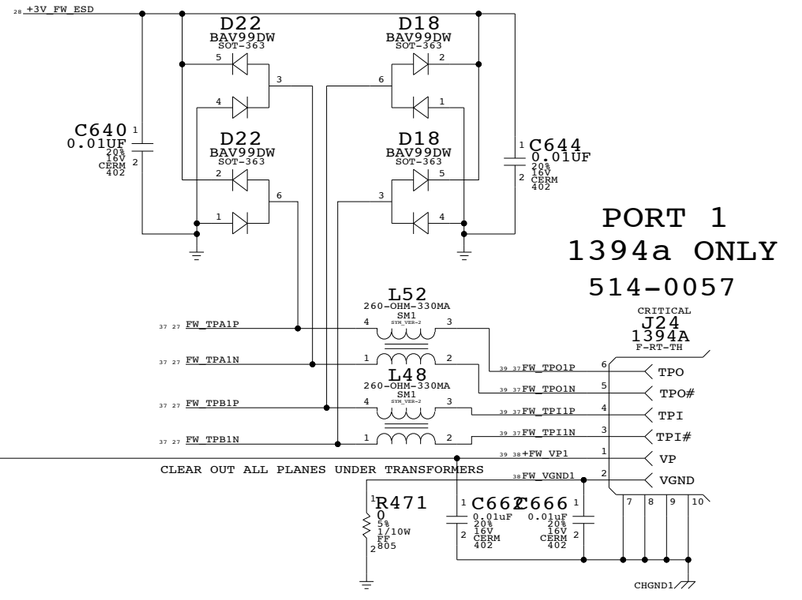


ENABLES PORT POWER WHEN
MACHINE IS RUNNING OR WHEN ASLEEP ON AC

PORT 0
1394a/b
(BILINGUAL)
514S0058

AREF NEEDS TO BE ISOLATED FROM ALL LOCAL GROUNDS PER 1394B SPEC SO WHEN A BILINGUAL DEVICE IS PLUGGED TO A BETA-ONLY DEVICE, THERE'S NO DC PATH BETWEEN THEM (TO AVOID GROUND OFFSET ISSUE)

BREF SHOULD BE HARD CONNECTED TO LOGIC GROUND FOR SPEED SIGNALING AND CONNECTION DETECTION CURRENTS PER 1394B V1.33



CLEAR OUT ALL PLANES UNDER TRANSFORMERS

PORT 1
1394a ONLY
514-0057

FIREWIRE PORTS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	B
SCALE: NONE	SHT 28 OF 44	

+3V_PMU

R595 470K 5% 1/16W MF 402 — CHARGE_LED_L (25 29 39)

R583 10K 5% 1/16W MF 402 — PMU_POWER_UP_L (28 29 32)

R582 10K 5% 1/16W MF 402 — SOFT_PWR_ON_L (22 23 29 33 39)

R560 100K 5% 1/16W MF 402 — MAIN_RESET_L (14 17 18 19 24 29 39)

RP39 100K 5% 1/16W SM1 — IO_RESET_L (17 23 26 29)

RP39 100K 5% 1/16W SM1 — SLEEP (23 25 29 32 34 39)

RP39 100K 5% 1/16W SM1 — INT_RESET_L (9 13 29)

RP39 100K 5% 1/16W SM1 — INT_SUSPEND_REQ_L (8 29)

R587 1K 5% 1/16W MF 402 — PMU_BYTE (29)

R586 10K 5% 1/16W MF 402 — PMU_CNVSS (29)

+3V_PMU

C255 10uF 20% 6.3V CERM 805 — C729 0.1uF 20% 10V CERM 402 — C724 0.1uF 20% 10V CERM 402

R602 4.7 5% 1/16W MF 402 — +3V_PMU_AVCC (25 29 38)

C731 0.1uF 20% 10V CERM 402

VCC (14, 60) — AVCC (97)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1008	1	IC,PMU,V81B	U29	

CPU_VCORE_HI_OC/PMU_AP should have a putldown for coming out of reset. MLB will have a pull-up to +3V_MAIN or +3V_SLEEP, which will act as our putldown since both are off during PMU reset.

OMIT

U29 M16C62 FLAS

23	KBD_Y<0>	86
23	KBD_Y<1>	85
23	KBD_Y<2>	84
23	KBD_Y<3>	83
23	KBD_Y<4>	82
23	KBD_Y<5>	81
23	KBD_Y<6>	80
23	KBD_Y<7>	79
	PMU_NUMLOCK_LED_L	78
	PMU_CAPSLOCK_LED_L	77
29 25	CHARGE_LED_L	76
29 28 32	PMU_POWER_UP_L	75
	NC	74
39 33 29 23 22	SOFT_PWR_ON_L	73
39 25 14	COMM_RING_DET_L	72
14	INT_WATCHDOG_L	71
23	KBD_X<0>	70
23	KBD_X<1>	69
23	KBD_X<2>	68
23	KBD_X<3>	67
23	KBD_X<4>	66
23	KBD_X<5>	65
23	KBD_X<6>	64
23	KBD_X<7>	63
23	KBD_X<8>	61
23	KBD_X<9>	59
29 26 23 17	IO_RESET_L	58
23	KBD_COMMAND_L	57
29 23	KBD_CONTROL_L	56
29 23	KBD_SHIFT_L	55
29 23	KBD_OPTION_L	54
23	KBD_FUNCTION_L	53
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23	KBD_ID	51
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8	INT_SUSPEND_ACK_L	46
8	INT_SUSPEND_REQ_L	45
29	PMU_BYTE	6
		11
		13
	PMU_RESET_L	10
38 29 25	+3V_PMU_AVCC	96
29	PMU_CNVSS	7

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P01_D1		85
P02_D2		84
P03_D3		83
P04_D4		82
P05_D5		81
P06_D6		80
P07_D7		79
P10_D8		78
P11_D9		77
P12_D10		76
P13_D11		75
P14_D12		74
P15_D13_INT3		73
P16_D14_INT4		72
P17_D15_INT5		71
P20_A0_D0		70
P21_A1_D1_D0		69
P22_A2_D2_D1		68
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P25_A5_D5_D4		65
P26_A6_D6_D5		64
P27_A7_D7_D6		63
P30_A8_D7		61
P31_A9		59
P32_A10		58
P33_A11		57
P34_A12		56
P35_A13		55
P36_A14		54
P37_A15		53
P40_A16		52
P41_A17		51
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P52_RD		42
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P62_RXD0		34
P63_TXD0		33
P64_CTS1_RTS1_CTS0_CLKS1		32
P65_CLK1		31
P66_RXD1		30
P67_TXD1		29
P70_TXD2_SDA_TA0OUT		28
P71_RXD2_SCL_TA0IN_TB5IN		27
P72_CLK2_TA1OUT_V		26
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P75_TA2IN_W		23
P76_TA3OUT		22
P77_TA3IN		21
P80_TA4OUT_U		20
P81_TA4IN_U		19
P82_INT0		18
P83_INT1		17
P84_INT2		16
P85_NMI		15
P86_XCOUT		9
P87_XCIN		8
P90_TB0IN_CLK3		5
P91_TB1IN_SIN3		4
P92_TB2IN_SOUT3		3
P93_DA0_TB3IN		2
P94_DA1_TB4IN		1
P95_ANEX0_CLK4		100
P96_ANEX1_SOUT4		99
P97_ADTRG_SIN4		98
P100_AN0		95
P101_AN1		93
P102_AN2		92
P103_AN3		91
P104_AN4_KI0		90
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44	CPU_VCORE_HI_OC	7 33
43	INT_RESET_L	9 13 29
42	MAIN_RESET_L	14 17 18 19 24 29 39
41	NC	
40	PMU_INT_NMI	14
39	PMU_EPM	29
38	INT_PU_RESET_L	13 25 29
37	PMU_CPU_HRESET_L	6 39
36	PMU_ACK_L	14
35	PMU_CLK	14
34	PMU_FROM_INT	14
33	PMU_TO_INT	14
32	PMU_REQ_L	14
31	PMU_LID_CLOSED_L	23 29 39
30	PMU_RESET_BUTTON_L	23 29
29	PMU_NMI_BUTTON_L	29
28		
27	TPAD_RXD	23 29
26	TPAD_TXD	23 29
25	SYSTEM_CLK_EN	14
24	CPU_CLK_EN	8
23	PMU_CHARGE_V	30
22	PMU_CHRG_BATT_0	30
21	NC (CHARGE_I)	
20	NC	
19	PMU_SLEEP_LED_L	23
18	CPU_SMI_L	5
17	POWER_VALID	29
16	PMU_PME_L	14 17 24 29 39
15	INT_PEND_PROC_INT	14
9	PMU_NMI_L	29
8	CLK32K_PMU_XOUT	
	CLK32K_PMU_XIN	
5	PMU_BATT0_DET_L	
4	PMU_BATT1_DET_L_PU	29
3	NC	
2	NC	
1	INT_PROC_SLEEP_REQ_L	14
100	PMU_POWERUP_OK	29
99	NC	
98	PMU_OOPS	29
95	THERM_L_OC	25
93	PMU_AC_IN	
92	PMU_AC_DET	29
91	NC	
90	PMU_I2C_CLK	29
89	PMU_I2C_DATA	29
88	PMU_SMB_CLK	29 30
87	PMU_SMB_DATA	29 30

Keep crystal subcircuit close to PMU.

R588 1K 5% 1/16W MF 402 — PMU_BATT_DET_L (29 30 39)

R600 1K 5% 1/16W MF 402 — AC_IN (26 28 30)

NO STUFF R248 10M 5% 1/16W MF 402

R249 0 5% 1/16W MF 402

CRITICAL Y3 SM-2 32.768K — CLK32K_PMU_XOUT_UF

C339 12pF 5% 50V CERM 402 — C340 12pF 5% 50V CERM 402

Y3'S LOAD CAPACITANCE IS 12.5PF

+3V_PMU

RP41 10K 5% 1/16W SM1 — PMU_EPM (29)

RP41 10K 5% 1/16W SM1 — PMU_RESET_BUTTON_L (29 23)

R261 10K 5% 1/16W MF 402 — PMU_POWERUP_OK (29)

R591 470K 5% 1/16W MF 402 — PMU_BATT1_DET_L_PU (29)

R589 470K 5% 1/16W MF 402 — PMU_BATT_DET_L (39 30 29)

RP41 10K 5% 1/16W SM1 — PMU_NMI_BUTTON_L (29)

RP41 10K 5% 1/16W SM1 — PMU_NMI_L (29)

R584 7.15K 1% 1/16W MF 402 — PMU_SMB_DATA (30 29)

R585 7.15K 1% 1/16W MF 402 — PMU_SMB_CLK (30 29)

+3V_SLEEP

R599 10K 5% 1/16W MF 402 — PMU_I2C_CLK (29)

R598 10K 5% 1/16W MF 402 — PMU_I2C_DATA (29)

+5V_SLEEP

R563 10K 5% 1/16W MF 402 — TPAD_RXD (29 23)

R564 10K 5% 1/16W MF 402 — TPAD_TXD (29 23)

+3V_MAIN

R576 100K 5% 1/16W MF 402 — POWER_VALID (29)

R575 10K 5% 1/16W MF 402 — PMU_PME_L (39 29 24 17 14)

R562 100K 5% 1/16W MF 402 — PMU_LID_CLOSED_L (39 29 23)

R594 10K 5% 1/16W MF 402 — PMU_OOPS (29)

R561 100K 5% 1/16W MF 402 — INT_PU_RESET_L (29 25 13)

UNDERVOLTAGE RESET CIRCUIT

+3V_PMU

R267 1K 5% 1/16W MF 402 — +3V_PMU_RESET (11)

C370 0.1uF 20% 10V CERM 402

U26 MAX6804 SOT143 — VCC, MR*, RSET*, GND

PMU_KB_RESET_L (39 29)

R597 2.2K 5% 1/16W MF 402 — NUMLOCK_LED_L (23)

R596 2.2K 5% 1/16W MF 402 — CAPSLOCK_LED_L (23)

NO STUFF R580 10M 5% 1/16W MF 402

R581 0 5% 1/16W MF 402

CRITICAL Y4 10.0000M 8X4.5MM-SM — CLK10M_PMU_XOUT

C406 12pF 5% 50V CERM 402 — C728 12pF 5% 50V CERM 402

Keep crystal subcircuit close to PMU.
Y5'S LOAD CAPACITANCE IS 12PF

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0604	197S0041		Y4	Alt. for Siward Part

PMU KEYBOARD RESET CIRCUIT

+3V_PMU

U20 NC7S32 SC70 — SOFT_PWR_ON_L (39 33 29 23 22), KBD_CONTROL_L (39 29 23) → PMU_KB_RESET_IN1

U24 NC7S32 SC70 — KBD_SHIFT_L (39 29 23), KBD_OPTION_L (39 29 23) → PMU_KB_RESET_IN2

C277 0.1uF 20% 10V CERM 402

U25 NC7S32 SC70 — PMU_KB_RESET_L (29 39)

KEEP CAP CLOSE TO ALL 3 OR GATES

ADAPTER IDs		
ADAPTER	ID RANGE	PIN VOLTAGE
Q11 (65W)	1.65-2.31V	2.007-2.066V
A29 (45W)	2.31-2.97V	2.558-2.661V
AIRLINE	0.33-0.99V	0.589-0.663V

A29 ADAPTER DETECTION

+3V_PMU

+4.85V_RAW (38 31)

R592 100K 1% 1/16W MF 402 — ADAPTER_DET (25 39)

R593 100K 1% 1/16W MF 402 — PMU_AC_DET (29)

R590 402K 1% 1/16W MF 402

R348 52.3K 1% 1/16W MF 402

C467 0.1uF 20% 10V CERM 402

R364 100K 5% 1/16W MF 402 — A29_DETECT (30)

U33 LMC7211 SM — A29_DET_REF, A29_DET_L

R345 4.7M 5% 1/16W MF 402

R349 127K 1% 1/16W MF 402

Q30 2N7002 SM

PMU

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	B
SCALE: NONE	SHT	29 44

DC POWER INPUT

(POWER JACK, ETC. ON SEPARATE BOARD)

CRITICAL
J27
87438-0433
M-RT-SM

+ADAPTER

C35 0.1uF 10% 50V X7R 603

DC INRUSH LIMITER

BACKFEED PROTECTION

Q68 SI4435DY SOI

Q69 SI4435DY SOI

+ADAPTER_SW

+ADAPTER_SENSE

R21 330K 5% 1/16W MF 402

C11 0.1uF 20% 50V CERM 805

AC_ENABLE_GATE

GATE

R732 47K 5% 1/16W MF 402

BKFD_PROT_GATE

C803 0.1uF 20% 16V CERM 402

R734 68K 5% 1/16W MF 402

BKFD_PROT_EN_L

Q9 2N7002DW SOT-363

C36 0.01uF 20% 50V CERM 603

CRITICAL
U3 MAX4172 TSSOP
RS+ RS- PG OUT GND
NC NC NC NC

+24V_PBUS

MAX4172_OUT

CRITICAL
R77 2.21K 0.1% 1/16W MF 603

R51 20K 1% 1/16W MF 402

+3V_PMU

R40 97.6K 1% 1/16W MF 402

R16 100K 1% 1/16W MF 402

C801 0.01uF 20% 16V CERM 402

R15 10K 5% 1/16W MF 402

R29 470K 5% 1/16W MF 402

AC_ENABLE_L

1V20_REF

U1 LMC7211 SM

AC_IN

Q1 2N7002DW SOT-363

AC_DIV

R42 10K 1% 1/16W MF 402

R30 57.6K 1% 1/16W MF 402

R41 1M 5% 1/16W MF 402

AC_IN_L

Q1 2N7002DW SOT-363

R22 470K 5% 1/16W MF 402

GREATER THAN 13.1V DETECT

PLACE U24 NEXT TO R382

CRITICAL
R61 0.025 1% 1W MF 2512

R82 4.7 5% 1/16W MF 402

R87 4.7 5% 1/16W MF 402

1772_CSSP

1772_CSSN

R57 100K 1% 1/16W MF 402

D4 1N914 SOT23

R49 12.7K 1% 1/16W MF 402

C67 1uF 20% 50V CERM 1210

C71 0.47uF 20% 50V CERM 1206

C95 0.47uF 20% 50V CERM 1206

+PBUS CURRENT LIMIT

R728 1K 1% 1/16W MF 402

IAC_RC_COMP

C798 0.1uF 20% 10V CERM 402

+3V_PMU

C794 0.1uF 20% 10V CERM 402

CRITICAL
R745 42.2K 1% 1/16W MF 603

IAC_FB

U55 SMC7111 SOT23-5

PLACE R383 CLOSE TO LTC1625

ROUTE LTC1625_ITH CAREFULLY

LTC1625_ITH

R727 10K 1% 1/16W MF 402

DP1 BAS16TW SOT-363

R119 150 1% 1/16W MF 402

1625_COMP

ADAPTER_I_REG

Place close to RS-

C826 0.01uF 20% 50V CERM 603

CURRENT_THRESHOLD

CRITICAL
R736 42.2K 0.1% 1/16W PF 603

CRITICAL
R738 82.5K 0.1% 1/16W PF 603

+3V_PMU

CRITICAL
R742 51.1K 0.1% 1/16W PF 603

A29_CURRENT_ADJ

R744 100K 5% 1/16W MF 402

OVER_18V_ADJ

Q2 2N7002DW SOT-363

A29_DETECT

Q74 2N7002DW SOT-363

AC_GTR_18V

Q74 2N7002DW SOT-363

1772_ACOK_L

C809 1uF 20% 10V CERM 603

BATTERY SWITCH-OVER CIRCUIT

+PBUS

F4 5AMP-125V SM-2

F5 5AMP-125V SM-2

+24V_PBUS

+BATT_24V_FUSE

+BATT_14V_FUSE

CRITICAL
Q6 SI4435DY SOI

CRITICAL
Q7 SUD45P03 TO-252

R716 47K 5% 1/16W MF 402

R710 47K 5% 1/16W MF 402

BATT_24V_GATE

BATT_14V_GATE

R717 10K 5% 1/16W MF 402

R711 10K 5% 1/16W MF 402

DP1 BAS16TW SOT-363

BATT_24PBUS_EN

BATT_14PBUS_EN

AC_IN_L

R102 158K 1% 1/16W MF 402

Q9 2N7002DW SOT-363

DP1 BAS16TW SOT-363

AC_IN_L_RC

C118 10uF 10% 6.3V CERM 805

WHEN AC IS IN, P-CHANNEL FETS ARE QUICKLY (DIODE) TURNED OFF

WHEN AC IS NOT PLUGGED, P-CHANNEL FETS ARE ON

RC TIME IS 480K*10UF @ +3V_PMU

SWITCHER VOLTAGE CONTROL

PMU SELECTS BETWEEN TWO VOLTAGES

SWITCHER CURRENT CONTROL

CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V

CHARGE THROTTLED BY LOW BATTERY VOLTAGE

OD OUTPUT LOW - WHEN AC GREATER THAN 18V

+3V_PMU

R73 27.4K 1% 1/16W MF 402

R62 10K 1% 1/16W MF 402

R58 10K 1% 1/16W MF 402

R74 4.12K 1% 1/16W MF 402

R733 20K 1% 1/16W MF 402

R731 1K 1% 1/16W MF 402

R56 1K 1% 1/16W MF 402

BATTV_HIGH

BATT_LOW

R59 100K 5% 1/16W MF 402

R75 5.23K 1% 1/16W MF 402

Q4 2N7002DW SOT-363

BATTV_LOW

PMU_CHARGE_V

Q71 2N7002DW SOT-363

Q71 2N7002DW SOT-363

R55 1K 1% 1/16W MF 402

C43 0.01uF 20% 16V CERM 402

C42 0.01uF 20% 16V CERM 402

1772_CCV_RC

1772_REF

R54 10K 1% 1/16W MF 402

C23 1uF 20% 10V CERM 603

R53 4.12K 1% 1/16W MF 402

1772_CLS

R83 1K 1% 1/16W MF 402

C24 0.1uF 20% 10V CERM 402

1772_GND

C41 1uF 20% 10V CERM 603

C98 0.1uF 20% 25V CERM 603

C99 0.1uF 20% 25V CERM 603

R94 100K 5% 1/16W MF 402

XW1 SM

NO STUFF

C853 1000pF 10% 25V X7R 402

Q64 IRF7811W SO-8

CRITICAL
L70 10uH SM1

D36 SM MBRS140T3

+BATT_RSNS

R715 0.05 1% 1W MF 2512

R720 1 5% 1/16W MF 603

R713 1 5% 1/16W MF 603

C780 4.7uF 20% 25V CERM 1206

C777 4.7uF 20% 25V CERM 1206

C795 4.7uF 20% 25V CERM 1206

C792 4.7uF 20% 25V CERM 1206

C790 4.7uF 20% 25V CERM 1206

C785 4.7uF 20% 25V CERM 1206

C779 33uF 20% 25V ELEC SM1

+3V_PMU

R741 100K 5% 1/16W MF 402

Q72 2N7002DW SOT-363

CHARGE_DISABLE

PMU_CHRG_BATT_0

Q72 2N7002DW SOT-363

+3V_PMU

C799 0.1uF 20% 10V CERM 402

U57 LMC7211 SM

BATT_LOW

R729 100K 1% 1/16W MF 402

R740 499K 1% 1/16W MF 402

BATT_DIV

1V65_REF

R730 100K 1% 1/16W MF 402

R735 100K 1% 1/16W MF 402

C807 0.047uF 10% 16V CERM 402

R47 6.34K 1% 1/16W MF 402

A29_CLS_ADJ

Q2 2N7002DW SOT-363

A29_DETECT

+BATT_VSNS

BATTERY CONNECTOR

CRITICAL
J26
87438-0833
M-RT-SM

+BATT_POS

(BATT_IN_PD)

BATT_CLK

BATT_DATA

PMU_BATT_DET_L

BATT_NEG

L5 FERR-EMI-100-OHM SM

L6 FERR-50-OHM SM

L4 FERR-EMI-100-OHM SM

PMU_SMB_CLK

L3 FERR-EMI-100-OHM SM

PMU_SMB_DATA

L2 FERR-50-OHM SM

+BATT

$V_{BATT} = CELLS \times (4.096 + (4.096 * V_{VCTL} / V_{REFIN}))$

For 4.15V cells, VCTL = 0.123 REFIN

For 4.20V cells, VCTL = 0.245 REFIN

$I_{CHG} = (0.2048/R_{62}) * (V_{ICTL} / V_{REFIN})$

U6 MAX1772 QSOP

CRITICAL

CSSP CSSN DCIN ACIN ACOK RFIN VCTL ICTL ICHG IINP CCV CCI CCS REF CLS GND CELLS LDO DLOV BST DHI LX DLO PGND CSIP CSIN BATT

1772_DCIN 1772_ACIN 1772_ACOK_L (+3V_PMU) 1772_VCTL 1772_ICTL 1772_ICHG 1772_IINP 1772_CCV 1772_CCI 1772_CCS 1772_CELLS 1772_DLOV 1772_BST 1772_DHI 1772_LX 1772_DLO (GND) 1772_CSIP 1772_CSIN

R725 33 1% 1W MF 1206

D6 1N914 SOT23

1772_BST_ESR

R52 100K 5% 1/16W MF 402

C97 0.1uF 20% 25V CERM 603

R96 4.7 5% 1/16W MF 603

C96 0.1uF 20% 50V CERM 805

Q70 IRF7805 SM

C112 2.2uF 20% 50V CERM 1812

C117 2.2uF 20% 50V CERM 1812

C113 2.2uF 20% 50V CERM 1812

C115 2.2uF 20% 50V CERM 1812

C116 2.2uF 20% 50V CERM 1812

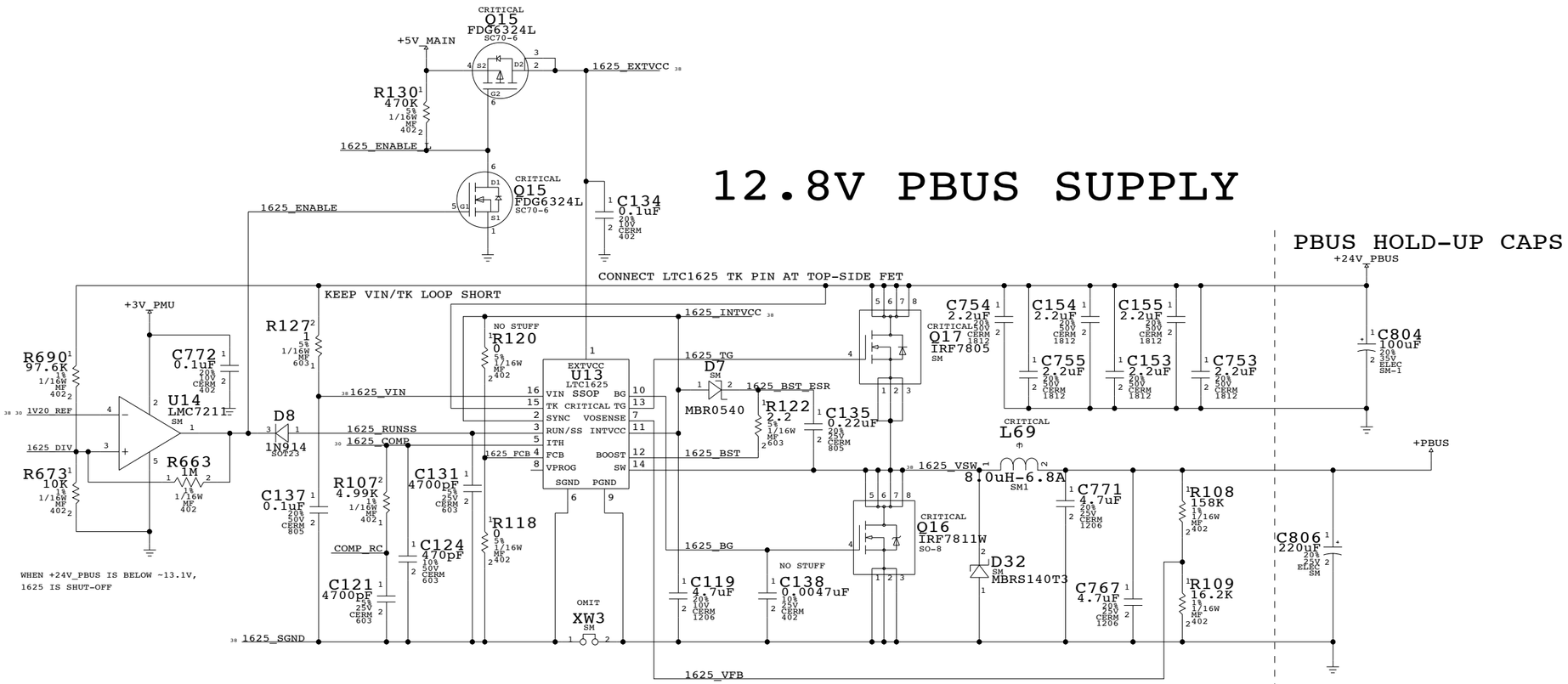
BATTERY CHARGER

APPLE COMPUTER INC.

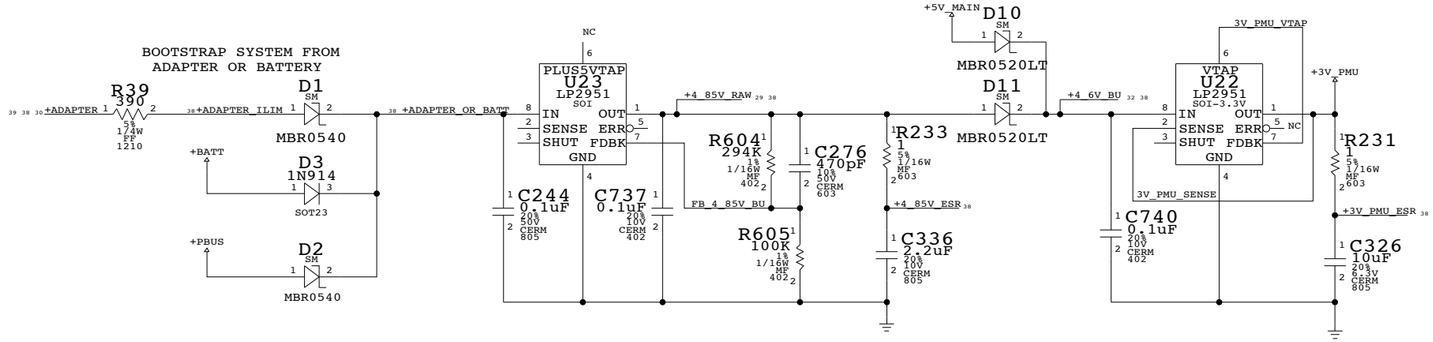
SIZE D | DRAWING NUMBER 051-6570 | REV. B

SCALE NONE | SHT 30 OF 44

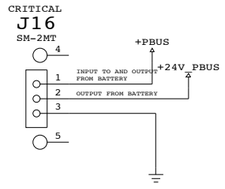
12.8V PBUS SUPPLY



PMU SUPPLY



BACKUP BATTERY



12.8V REGULATOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	B
SCALE: NONE	SHT	31 44

3.3V/5V MAIN SUPPLY

DCDC_EN TRUTH TABLE

PMU_POWER_UP_L	SLEEP	DCDC_EN	DCDC_EN_L	State
0	0	1	0	Run
1 (2.99V)	1	1	0	Sleep
1	0	0	1	Shutdown
+3V_PMU	+3V_PMU	+4_6V_BU	+3V_PMU	VOLTAGE

SLEEP LEVEL SHIFTER (3V -> 5V)

+5V_SLEEP LOADS

1) FAN
2) Headphone amplifier
3) OPTICAL DRIVE
4) DVI
5) TRACKPAD

+3V_SLEEP LOADS

1) CPU PLL CONFIG CONTROL
2) INTREPID - I2C PULLUPS & OSCILLATOR
3) MAP31 - 3V RAIL (IF USING D3COLD)
4) GRAPHIC CHIP SPREAD SPECTRUM CHIP
5) LVDS DDC PULL-UPS
6) DVI LEVEL SHIFTERS & PULLUPS & HPD
7) BOOT BANGER
8) HARD DRIVE (IF USING 3V LOGIC)
9) WIRELESS
10) PMU - I2C PULLUPS

5V START TO TURN ON ~12.5MS AFTER DCDC_EN_L
3V START TO TURN ON ~25MS AFTER DCDC_EN_L
DIODE WILL ENSURE DCDC_EN_L IS QUICKLY DISCHARGED DURING SHUT-DOWN
POWERDOWN DELAY IS AROUND 4MS-15.6MS

DISTRIBUTE CAPS ALONG TOP EDGE AND FAN CUT-OUT

THIS SIGNAL IS OPEN COLLECTOR TO GND WHEN POWER IS NOT GOOD
220PF IS USED TO QUIET NOISE ON PGOOD ONCE INTERNAL OPEN DRAIN IS DISENGAGED

3.3V/5V REGULATOR

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6570 | REV. B

SCALE NONE | SHT 32 OF 44

VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage
(approx. 7ms delay)

1.250V->0.975V 1.50Ghz
1.200V->0.975V 1.33Ghz
(value without offset)

NOTE: When U15 MUX is removed => NO SW Support,
R794,R795,R796&R797 have to be stuffed

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
126S0036	7	CAP,AL,POLY,8.2uF,20%,16V,V CASE,SMD	C51,C52,C77,C78,C91,C92,C111	CRITICAL	

SEL = 0; Y1=A1
SEL = 1; Y1=B1

Keep trace fat (40-100 mils) and short!!

MAX1717 VID INPUTS ARE 3.3-5V TOLERANT

Note:No stuff R67 to set skip mode of VCore

Connect MAX1717 GND pin 13
to GND at bottom-side FET

Keep trace fat and short!!

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V, HENCE VOFFSET = 2.0V*0.85*(Rb / Ra) AND VCORE = VDAC + VOFFSET.
NOTE: Ra NO STUFFED FOR NO OFFSET CASE

(R93 CPU_BTR BOM OPTION SEE BOM TABLE)

(CPU Vcore value with offset)

1.50Ghz 1.280V->0.990V
1.33Ghz 1.220V->0.990V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S2003	1	RES,MF,1/16W,2K OHM,1%,0402,SMD	R97	?	CPU_BTR
114S5903	1	RES,MF,1/16W,5.9K OHM,1%,0402,SMD	R93	?	CPU_BTR

ROUTE AS DIFFERENTIAL PAIR

PLACE THIS SHORT AT
PIN OF 1000uF CAP
CLOSEST TO CPU

OUTPUT VOLTAGE

V_{DAC} D4=0	V_{DAC} D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1
If all pull-ups are >=100K and all
pull-downs are <=1K, A V = B V .

Fmax Test Connections

VCORE SUPPLY

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	B
SCALE: NONE	SHT 33 OF 44	

1.5V/2.5V SWITCHER

M11 Power Shut down Sequencing

+2_5V_SLEEP
XW8 SM
DP4 BAS16TW SOT-363
XW21 SM
+3V_SLEEP
+1_8V_SLEEP
XW10 SM
DP4 BAS16TW SOT-363
+1_5V_SLEEP
XW23 SM
DP4 BAS16TW SOT-363

+1_5V_SLEEP LOADS

1) AGP I/O - IF USING D3COLD
2) MAXBUS I/O - IF 1.5V INTERFACE

+1_5V_MAIN LOADS

1) INTREPID CORE

+2_5V_MAIN LOADS

1) MAP31 - FBCORE/FBIO IF USING D3HOT
2) GIGABIT ETHERNET - AVDDL
3) DDR SODIMMS - CORE/IO
4) DDR MUXES

+2_5V_SLEEP LOADS

1) FBCORE/FBIO IF USING D3COLD

DIODE PROVIDE PROVIDE QUICK SHUT-DOWN
POWER DOWN DELAY 1.5MS TO 3.5MS

1.8V SWITCHER

+1_8V_MAIN LOADS

1) INTREPID PLLS

+1_8V_SLEEP LOADS

1) MPC7447 - MAXBUS I/O - IF 1.8V INTERFACE
2) CPU JTAG & MaxBus Pull-ups
3) CPU PLL Config Straps

1.5V/1.8V/2.5V SUPPLIES

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	B
SCALE: NONE	SHT	34 44

DIGITAL SIGNALS

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
				STUB_LENGTH OF 200 MILS NEEDED WHEN WE CONVERT TO 14.2				
GROUP 0	MEM_DATA<7..0>	L:S:1602:1700	7	500	(200)			167 MHZ
	MEM_DQM<0>	L:S:1602 MIL:1700 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<0>	L:S:1602 MIL:1700 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<7..0>	L:S:1903:2000	7	500	(200)			167 MHZ
	RAM_DQM_A<0>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<0>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<7..0>	L:S:2000:2100	7	500	(200)			167 MHZ
	RAM_DQM_B<0>	L:S:2000 MIL:2100 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<0>	L:S:2000 MIL:2100 MIL	7	500.0000	(200)			167.0 MHz
GROUP 1	MEM_DATA<15..8>	L:S:1344:1660	7	500	(200)			167 MHZ
	MEM_DQM<1>	L:S:1344 MIL:1660 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<1>	L:S:1344 MIL:1660 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<15..8>	L:S:1905:2000	7	500	(200)			167 MHZ
	RAM_DQM_A<1>	L:S:1905 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<1>	L:S:1905 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<15..8>	L:S:2004:2412	7	500	(200)			167 MHZ
	RAM_DQM_B<1>	L:S:2004 MIL:2412 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<1>	L:S:2004 MIL:2412 MIL	7	500.0000	(200)			167.0 MHz
GROUP 2	MEM_DATA<23..16>	L:S:1435:1500	7	500	(200)			167 MHZ
	MEM_DQM<2>	L:S:1435 MIL:1500 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<2>	L:S:1435 MIL:1500 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<23..16>	L:S:1707:1800	7	500	(200)			167 MHZ
	RAM_DQM_A<2>	L:S:1707 MIL:1800 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<2>	L:S:1707 MIL:1800 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<23..16>	L:S:1900:2000	7	500	(200)			167 MHZ
	RAM_DQM_B<2>	L:S:1900 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<2>	L:S:1900 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
GROUP 3	MEM_DATA<31..24>	L:S:1233:1485	7	500	(200)			167 MHZ
	MEM_DQM<3>	L:S:1233 MIL:1485 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<3>	L:S:1233 MIL:1485 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<31..24>	L:S:1700:2165	7	500	(200)			167 MHZ
	RAM_DQM_A<3>	L:S:1700 MIL:2165 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<3>	L:S:1700 MIL:2165 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<25..24>	L:S:1907:2356	7	500	(200)			167 MHZ
	RAM_DATA_B<26>	L:S:1907 MIL:2356 MIL	7		(200)			167.0 MHz
	RAM_DATA_B<31..27>	L:S:1907:2356	7	500	(200)			167 MHZ
	RAM_DQM_B<3>	L:S:1907 MIL:2356 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<3>	L:S:1907 MIL:2356 MIL	7	500.0000	(200)			167.0 MHz
GROUP 4	MEM_DATA<39..32>	L:S:1915:2000	7	500	(200)			167 MHZ
	MEM_DQM<4>	L:S:1915 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<4>	L:S:1915 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<39..32>	L:S:1205:1387	7	500	(200)			167 MHZ
DDR RAM	RAM_DQM_A<4>	L:S:1205 MIL:1387 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<4>	L:S:1205 MIL:1387 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<39..32>	L:S:1404:1686	7	500	(200)			167 MHZ
	RAM_DQM_B<4>	L:S:1404 MIL:1686 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<4>	L:S:1404 MIL:1686 MIL	7	500.0000	(200)			167.0 MHz
GROUP 5	MEM_DATA<47..40>	L:S:1719:1893	7	500	(200)			167 MHZ
	MEM_DQM<5>	L:S:1719 MIL:1893 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<5>	L:S:1719 MIL:1893 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<47..40>	L:S:1607:1898	7	500	(200)			167 MHZ
	RAM_DQM_A<5>	L:S:1607 MIL:1898 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<5>	L:S:1607 MIL:1898 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<47..40>	L:S:1716:2102	7	500	(200)			167 MHZ
	RAM_DQM_B<5>	L:S:1716 MIL:2102 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<5>	L:S:1716 MIL:2102 MIL	7	500.0000	(200)			167.0 MHz
GROUP 6	MEM_DATA<55..48>	L:S:2101:2170	7	500	(200)			167 MHZ
	MEM_DQM<6>	L:S:2101 MIL:2170 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<6>	L:S:2101 MIL:2170 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<55..48>	L:S:1204:1357	7	500	(200)			167 MHZ
	RAM_DQM_A<6>	L:S:1204 MIL:1357 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<6>	L:S:1204 MIL:1357 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<55..48>	L:S:1400:1546	7	500	(200)			167 MHZ
	RAM_DQM_B<6>	L:S:1400 MIL:1546 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<6>	L:S:1400 MIL:1546 MIL	7	500.0000	(200)			167.0 MHz
GROUP 7	MEM_DATA<63..56>	L:S:1903:2000	7	500	(200)			167 MHZ
	MEM_DQM<7>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<7>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<63..56>	L:S:1611:1696	7	500	(200)			167 MHZ
	RAM_DQM_A<7>	L:S:1611 MIL:1696 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<7>	L:S:1611 MIL:1696 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<63..56>	L:S:1809:1887	7	500	(200)			167 MHZ
	RAM_DQM_B<7>	L:S:1809 MIL:1887 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<7>	L:S:1809 MIL:1887 MIL	7	500.0000	(200)			167.0 MHz
ADDR	MEM_ADDR<12..0>	L:S::500	4					83 MHZ
	RAM_ADDR<12..0>	L:S:2000:3000	10		(200)			
	MEM_BA<1..0>	L:S::500	4					
	RAM_BA<1..0>	L:S:2000:3300	8		(200)			
CONTROL	MEM_CS_L<3..0>	L:S::500	4					
	RAM_CS_L<3..0>	L:S:2500:3200	7		(200)			
	MEM_CKE<3..0>	L:S::500	4					
	RAM_CKE<3..0>	L:S:2500:3200	7		(200)			
	MEM_RAS_L	L:S::500 MIL	4					
	RAM_RAS_L	L:S:2000 MIL:4100 MIL	7		(200)			
	MEM_CAS_L	L:S::500 MIL	4					
	RAM_CAS_L	L:S:2000 MIL:4100 MIL	7		(200)			
	MEM_WE_L	L:S::500 MIL	4					
	RAM_WE_L	L:S:2000 MIL:3100 MIL	8		(200)			
	MEM_MUXSEL_MSB	L:S:1700 MIL:3000 MIL	8					
	MEM_MUXSEL_LSB	L:S:1700 MIL:3000 MIL	7					

TOTAL LENGTH CONTROLLED BY SPREADSHEET

PRIORITY: 2
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9
GOAL: MINIMIZE
EXPOSED ROUTES
MINIMIZE VIAS

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME	PROPAGATION_DELAY	MATCHED_DELAY	MAX VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM
INTREPID CLOCKS	SYSCLK_CPU_UF	L:S::150 MIL					10 MIL SPACING	167.0 MHz
	SYSCLK_CPU	L:S:2650 MIL:2750 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz
	INT_CPUFB_OUT	L:S::150 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_OUT_SHORT	L:S:700 MIL:850 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_OUT_NORM	L:S:500 MIL:600 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_IN_NORM	L:S:500 MIL:600 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_LONG	L:S:1050 MIL:1150 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_IN	L:S:700 MIL:800 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0_UF	L:S:300 MIL:500 MIL	SYSCLK_DDRCLK_A0_UF	SYSCLK_DDRCLK_A0_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0_L_UF	L:S:300 MIL:500 MIL	SYSCLK_DDRCLK_A0_UF	SYSCLK_DDRCLK_A0_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1_UF	L:S:300 MIL:500 MIL	SYSCLK_DDRCLK_A1_UF	SYSCLK_DDRCLK_A1_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1_L_UF	L:S:300 MIL:500 MIL	SYSCLK_DDRCLK_A1_UF	SYSCLK_DDRCLK_A1_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0_UF	L:S:300 MIL:500 MIL	SYSCLK_DDRCLK_B0_UF	SYSCLK_DDRCLK_B0_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0_L_UF	L:S:300 MIL:500 MIL	SYSCLK_DDRCLK_B0_UF	SYSCLK_DDRCLK_B0_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1_UF	L:S:300 MIL:500 MIL	SYSCLK_DDRCLK_B1_UF	SYSCLK_DDRCLK_B1_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1_L_UF	L:S:300 MIL:500 MIL	SYSCLK_DDRCLK_B1_UF	SYSCLK_DDRCLK_B1_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A0	SYSCLK_DDRCLK_A0:G:L:S:0 MIL:25 MIL	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0_L	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A0	SYSCLK_DDRCLK_A0:G:L:S:0 MIL:25 MIL	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A1	SYSCLK_DDRCLK_A1:G:L:S:0 MIL:25 MIL	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1_L	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A1	SYSCLK_DDRCLK_A1:G:L:S:0 MIL:25 MIL	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B0	SYSCLK_DDRCLK_B0:G:L:S:0 MIL:25 MIL	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0_L	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B0	SYSCLK_DDRCLK_B0:G:L:S:0 MIL:25 MIL	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B1	SYSCLK_DDRCLK_B1:G:L:S:0 MIL:25 MIL	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1_L	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B1	SYSCLK_DDRCLK_B1:G:L:S:0 MIL:25 MIL	250.0000	(200)	10 MIL SPACING	167.0 MHz
	INT_REF_CLK_OUT_UF	L:S::400 MIL				(200)	10 MIL SPACING	49.92 MHz
	INT_REF_CLK_OUT	L:S:1000 MIL:1150 MIL		5	250.0000	(200)	10 MIL SPACING	49.92 MHz
	INT_REF_CLK_IN	L:S:1900 MIL:2000 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz
	CLK66M_GPU_AGP_UF	L:S::150 MIL				(200)	10 MIL SPACING	66.00 MHz
	CLK66M_GPU_AGP	L:S:1800 MIL:1900 MIL		6	400.0000	(200)	10 MIL SPACING	66.00 MHz
	INT_AGP_FB_OUT	L:S::150 MIL				(200)	10 MIL SPACING	66.00 MHz
	INT_AGP_FB_IN	L:S:1450 MIL:1550 MIL		6	500.0000	(200)	10 MIL SPACING	66.00 MHz
	CLK33M_CBUS_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz
	CLK33M_CBUS	L:S:5000 MIL:6000 MIL		9	500.0000	(200)	10 MIL SPACING	33.00 MHz
	CLK33M_AIRPORT_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz
	CLK33M_AIRPORT	L:S:9500 MIL:10500 MIL		6	500.0000	(200)	10 MIL SPACING	33.00 MHz
	CLK33M_NEC_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz
	CLK33M_NEC	L:S:4000 MIL:6000 MIL		7	500.0000	(200)	10 MIL SPACING	33.00 MHz
	INT_PCI_FB_OUT	L:S::300 MIL				(200)	10 MIL SPACING	33.00 MHz
	INT_PCI_FB_IN	L:S:6500 MIL:7500 MIL		7	500.0000	(200)	10 MIL SPACING	33.00 MHz
M10 & OSC	ATI_CLK27M_OSC	L:S::400 MIL		5		(200)	10 MIL SPACING	
	ATI_CLK27M_OSC_SS	L:S::400 MIL		5		(200)	10 MIL SPACING	
	ATI_CLK27M_IN	L:S::200 MIL		5		(200)	10 MIL SPACING	
	ATI_SSCLK_UF	L:S::200 MIL		5		(200)	10 MIL SPACING	
	ATI_SSCLK_IN	L:S::1800 MIL		5	500.0000	(200)	10 MIL SPACING	
CRYSTALS	CLK18M_INT_XIN	L:S:1400 MIL:1500 MIL					10 MIL SPACING	
	CLK18M_INT_XOUT	L:S:1250 MIL:1350 MIL					10 MIL SPACING	
	CLK18M_XTAL_IN	L:S::300 MIL					10 MIL SPACING	
	CLK18M_INT_EXT	L:S::400 MIL					10 MIL SPACING	
SOUND	INT_I2S0_SND_MCLK			6	500.0000	(200)	10 MIL SPACING	
ETHERNET	CLKENET_PHY_RX	L:S::300 MIL				(200)		125.0 MHz
	CLKENET_LINK_RX	L:S:8000 MIL:9000 MIL		6	800.0000	(200)	10 MIL SPACING	125.0 MHz
	CLKENET_PHY_GBE_REF	L:S::300 MIL				(200)		125.0 MHz
	CLKENET_LINK_GBE_REF	L:S:8000 MIL:9000 MIL		6	500.0000	(200)	10 MIL SPACING	125.0 MHz
	CLKENET_PHY_TX	L:S::300 MIL				(200)		25.00 MHz
	CLKENET_LINK_TX	L:S:8000 MIL:9000 MIL		6	500.0000	(200)	10 MIL SPACING	25.00 MHz
	CLKENET_LINK_GTX	L:S::300 MIL				(200)		125.0 MHz
	CLKENET_PHY_GTX	L:S:8000 MIL:9000 MIL		6	600.0000	(200)	10 MIL SPACING	125.0 MHz
FIREWIRE	CLKFW_PHY_PCLK	L:S::300 MIL				(200)		49.15 MHz
	CLKFW_LINK_PCLK	L:S:7500 MIL:8000 MIL		5	500.0000	(200)	10 MIL SPACING	49.15 MHz
	CLKFW_PHY_LCLK	L:S:7500 MIL:8000 MIL		5	500.0000	(200)	10 MIL SPACING	49.15 MHz
	CLKFW_LINK_LCLK	L:S::300 MIL				(200)		49.15 MHz
	FW_XI	L:S::500 MIL				(200)	10 MIL SPACING	98.03 MHz
	FW_OSC	L:S::300 MIL				(200)	10 MIL SPACING	98.03 MHz

PRIORITY: 1
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9
GOAL: MINIMIZE EXPOSURE ON LONG NETS

SIGNAL CONSTRAINTS - PAGE 1

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570 B	
SCALE: NONE	SHT 35 OF 44	

DIGITAL SIGNALS

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
MAXBUS	CPU_AACK_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_ADDR<0..31>	L:S:1500:3100	7		(250)		TRUE	83 MHZ
	CPU_ARTRY_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_BG_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_BR_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_CI_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_DATA<0..31>	L:S:1100:2700	7		(250)		TRUE	83 MHZ
	CPU_DATA<32..63>	L:S:1100:2700	8		(250)			83 MHZ
	CPU_DBG_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_DTI<0..2>	L:S:1500:2950	7		(250)			
	CPU_DRDY_L	L:S:1500 MIL:3200 MIL	7		(250)			
	CPU_GBL_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_HIT_L	L:S:1500 MIL:2800 MIL	7		(250)			
	CPU_QACK_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_QREQ_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_TA_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_TBST_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_TEA_L	L:S:1500 MIL:3000 MIL	7		(250)			
	CPU_TS_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_TSIZ<0..2>	L:S:1500:3500	7		(250)			
	CPU_TT<0..4>	L:S:1500:3400	7		(250)			
	CPU_WT_L	L:S:1500 MIL:3100 MIL	7		(250)			

PRIORITY: 4
PRIMARY LAYERS: 9
SECONDARY LAYERS: 4,7
GOAL: MINIMIZE TH VIAS

STUB_LENGTH OF 250 MILS NEEDED WHEN DESIGN SWITCHED TO 14.2

Temporary Area for TMDS/DVO signal constraints

ALL TMDS GROUP SIGNALS ROUTE AT LAYER 4 OR 7 AND HAVE SAME WIDTH SPACING RULE AS OTHER TMDS SIGNALS

GPU_TMDS_CLKN	GPU_CLKTMDS	GPUTMDS:G:L:S:0 MIL:50 MIL		500.0000	100 OHM SPACING 100 OHM SPACING 5	
GPU_TMDS_CLKP	GPU_CLKTMDS	GPUTMDS:G:L:S:0 MIL:50 MIL		500.0000	100 OHM SPACING 100 OHM SPACING 5	
GPU_TMDS_DN<0>	GPU_TMDS_D0			500.0000	100 OHM SPACING 100 OHM SPACING 8	
GPU_TMDS_DP<0>	GPU_TMDS_D0			500.0000	100 OHM SPACING 100 OHM SPACING 8	
GPU_TMDS_DN<1>	GPU_TMDS_D1			600.0000	100 OHM SPACING 100 OHM SPACING 8	
GPU_TMDS_DP<1>	GPU_TMDS_D1			600.0000	100 OHM SPACING 100 OHM SPACING 8	
GPU_TMDS_DN<2>	GPU_TMDS_D2			830.0000	100 OHM SPACING 100 OHM SPACING 8	
GPU_TMDS_DP<2>	GPU_TMDS_D2			830.0000	100 OHM SPACING 100 OHM SPACING 8	

SI_TMDS_CLKN	SI_CLKTMDS	SITMDS:G:L:S:0 MIL:50 MIL			100 OHM SPACING 100 OHM SPACING 5	
SI_TMDS_CLKP	SI_CLKTMDS	SITMDS:G:L:S:0 MIL:50 MIL			100 OHM SPACING 100 OHM SPACING 5	
SI_TMDS_DN<0>	SI_TMDS_D0				100 OHM SPACING 100 OHM SPACING 8	
SI_TMDS_DP<0>	SI_TMDS_D0				100 OHM SPACING 100 OHM SPACING 8	
SI_TMDS_DN<1>	SI_TMDS_D1				100 OHM SPACING 100 OHM SPACING 8	
SI_TMDS_DP<1>	SI_TMDS_D1				100 OHM SPACING 100 OHM SPACING 8	
SI_TMDS_DN<2>	SI_TMDS_D2				100 OHM SPACING 100 OHM SPACING 8	
SI_TMDS_DP<2>	SI_TMDS_D2				100 OHM SPACING 100 OHM SPACING 8	

ALL THE DVOD GROUP SIGNALS ROUTE AT LAYER 4 OR 7 AND ROUTE AS STANDARD 50OHM SIGNALS AT 4 MILS

ATI_DVOD<11..0>	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610		
ATI_DVOD_DE	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610.0000		
ATI_DVO_HSYNC	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610.0000		
ATI_DVO_VSYNC	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610.0000		
ATI_DVO_CLKP	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610.0000	165.0 MHz:::	

GPU_DVOD<11..0>	GPUDVOD:G:L:S:0 MIL:50 MIL	6	700		
GPU_DVOD_DE	GPUDVOD:G:L:S:0 MIL:50 MIL	6	500.0000		
GPU_DVO_HSYNC	GPUDVOD:G:L:S:0 MIL:50 MIL	6	500.0000		
GPU_DVO_VSYNC	GPUDVOD:G:L:S:0 MIL:50 MIL	6	500.0000		
GPU_DVO_CLKP	GPUDVOD:G:L:S:0 MIL:50 MIL	6	500.0000	165.0 MHz:::	

TMDS_CONN_CLKN	CLKCONN_TMDS	TMDS_CONN:G:L:S:0 MIL:50 MIL		500.0000	100 OHM SPACING 100 OHM SPACING 4
TMDS_CONN_CLKP	CLKCONN_TMDS	TMDS_CONN:G:L:S:0 MIL:50 MIL		500.0000	100 OHM SPACING 100 OHM SPACING 4
TMDS_CONN_DN<0>	CONN_TMDS_D0			500.0000	100 OHM SPACING 100 OHM SPACING 4
TMDS_CONN_DP<0>	CONN_TMDS_D0			500.0000	100 OHM SPACING 100 OHM SPACING 4
TMDS_CONN_DN<1>	CONN_TMDS_D1			500.0000	100 OHM SPACING 100 OHM SPACING 4
TMDS_CONN_DP<1>	CONN_TMDS_D1			500.0000	100 OHM SPACING 100 OHM SPACING 4
TMDS_CONN_DN<2>	CONN_TMDS_D2			500.0000	100 OHM SPACING 100 OHM SPACING 4
TMDS_CONN_DP<2>	CONN_TMDS_D2			500.0000	100 OHM SPACING 100 OHM SPACING 4

SIGNAL CONSTRAINTS - PAGE 1

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6570 | REV. B

SCALE NONE | SHT 36 OF 44

Digital Signals (cont'd)

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
AGP	AGP_AD<15..0>	L:S:1050:1450	7					66 MHz
AGP BYTES 0-1	AGP_CBE<1..0>	L:S:1050:1450	7					66 MHz
	AGP_AD_STB<0>	L:S:1050 MIL:1450 MIL			(250)	8 MIL SPACING		133.0 MHz
	AGP_AD_STB_L<0>	L:S:1050 MIL:1450 MIL			(250)	8 MIL SPACING		133.0 MHz
AGP BYTES 2-3	AGP_AD<31..16>	L:S:1050:1450	7					66 MHz
	AGP_CBE<3..2>	L:S:1050:1450	7					66 MHz
	AGP_AD_STB<1>	L:S:1050 MIL:1450 MIL			(250)	8 MIL SPACING		133.0 MHz
	AGP_AD_STB_L<1>	L:S:1050 MIL:1450 MIL			(250)	8 MIL SPACING		133.0 MHz
AGP SIDEBAND	AGP_SBA<7..0>	L:S:1050:1450	7					66 MHz
	AGP_SB_STB	L:S:1050 MIL:1450 MIL			(350)	8 MIL SPACING		66.00 MHz
	AGP_SB_STB_L	L:S:1050 MIL:1450 MIL			(350)	8 MIL SPACING		66.00 MHz
AGP CONTROL	AGP_FRAME_L	L:S:1250 MIL:1950 MIL						66.00 MHz
	AGP_IRDY_L	L:S:1250 MIL:1950 MIL						66.00 MHz
	AGP_TRDY_L	L:S:1250 MIL:1950 MIL						66.00 MHz
	AGP_DEVSEL_L	L:S:1250 MIL:1950 MIL						66.00 MHz
	AGP_STOP_L	L:S:1250 MIL:1950 MIL						66.00 MHz
	AGP_PAR	L:S:1250 MIL:1950 MIL						66.00 MHz
	AGP_REQ_L	L:S:1250 MIL:1950 MIL						66.00 MHz
	AGP_GNT_L	L:S:1250 MIL:1950 MIL						66.00 MHz
	AGP_RBF_L	L:S:1250 MIL:1950 MIL						66.00 MHz
PCI	PCI_AD<31..0>	L:S:6000:12500				MIN_DAISY_CHAIN		33 MHz
	PCI_CBE<3..0>	L:S:6000:12500				MIN_DAISY_CHAIN		33 MHz
	PCI_FRAME_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHz
	PCI_IRDY_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHz
	PCI_TRDY_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHz
	PCI_DEVSEL_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHz
	PCI_STOP_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHz
	PCI_PAR	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHz
ULTRA ATA-100	UIDE_DATA<15..8>	L:S::710			(200)			100 MHZ
	UIDE_DATA<7>	U51_V1:RP19.3::600 MIL			(200)			100.0 MHz
	UIDE_DATA<6..0>	L:S::600			(200)			100 MHZ
	UIDE_ADDR<2..0>	L:S::650			(200)	NEED TO MATCH DELAY TO 250		100 MHZ
	UIDE_RST_L	L:S::400 MIL			(200)			100.0 MHz
	UIDE_DIOW_L	L:S::400 MIL			(200)			100.0 MHz
	UIDE_DIOR_L	L:S::600 MIL		10 MIL SPACING	(200)			100.0 MHz
	UIDE_DMACK_L	L:S::400 MIL			(200)			100.0 MHz
	UIDE_CS0_L	L:S::500 MIL			(200)			100.0 MHz
	UIDE_CS1_L	L:S::500 MIL			(200)			100.0 MHz
	UIDE_DMARQ	L:S::400 MIL			(200)			100.0 MHz
	UIDE_IOCHRDY	L:S::600 MIL		10 MIL SPACING	(200)			100.0 MHz
	UIDE_INTRQ	L:S::400 MIL			(200)			100.0 MHz
	HD_DATA<15..0>	L:S:5000:6500	7		(200)			100 MHZ
	HD_ADDR<2..0>	L:S:5000:6500	7		(200)			100 MHZ
	HD_RESET_L	L:S:4000 MIL:6000 MIL	7		(200)	TOTAL UIDE+HD SKEW <500MIL		100.0 MHz
	HD_DIOW_L	L:S:3000 MIL:5200 MIL	7		(200)			100.0 MHz
	HD_DIOR_L	L:S:6100 MIL:6150 MIL	7	10 MIL SPACING	(200)			100.0 MHz
	HD_DMACK_L	L:S:4500 MIL:6000 MIL	7		(200)			100.0 MHz
	HD_CS0_L	L:S:3000 MIL:6000 MIL	7		(200)			100.0 MHz
	HD_CS1_L	L:S:3000 MIL:6000 MIL	7		(200)			100.0 MHz
	HD_DMARQ	L:S:4500 MIL:6000 MIL	7		(200)			100.0 MHz
	HD_IOCHRDY	L:S:6200 MIL:6300 MIL	7	10 MIL SPACING	(200)			100.0 MHz
	HD_INTRQ	L:S:3000 MIL:5000 MIL	7					100.0 MHz
EIDE INTREPID	EIDE_DATA<15..0>	L:S::850						33 MHZ
	EIDE_ADDR<2..0>	L:S::850						33 MHZ
	EIDE_CS0_L	L:S::850 MIL						33.00 MHz
	EIDE_CS1_L	L:S::850 MIL						33.00 MHz
	EIDE_RD_L	L:S::500 MIL						33.00 MHz
	EIDE_WR_L	L:S::500 MIL						33.00 MHz
	EIDE_IOCHRDY	L:S::500 MIL						33.00 MHz
	EIDE_INT	L:S::500 MIL						33.00 MHz
	EIDE_RST_L	L:S::500 MIL						33.00 MHz
	EIDE_DMACK_L	L:S::500 MIL						33.00 MHz
	EIDE_DMARQ	L:S::500 MIL						33.00 MHz
OPTICAL	EIDE_OPTICAL_DATA<15..0>	L:S:4000:6000						33 MHZ
	EIDE_OPTICAL_ADDR<2..0>	L:S:4000:6000						33 MHZ
	EIDE_OPTICAL_CS0_L	L:S:4500 MIL:6500 MIL						33.00 MHz
	EIDE_OPTICAL_CS1_L	L:S:4500 MIL:6500 MIL						33.00 MHz
	EIDE_OPTICAL_READ_L	L:S:4500 MIL:6500 MIL						33.00 MHz
	EIDE_OPTICAL_WR_L	L:S:4500 MIL:6500 MIL						33.00 MHz
	EIDE_OPTICAL_IOCHRDY	L:S:4500 MIL:6500 MIL						33.00 MHz
	EIDE_OPTICAL_INT	L:S:5000 MIL:7000 MIL						33.00 MHz
	EIDE_OPTICAL_RST_L	L:S:4500 MIL:6500 MIL						33.00 MHz
	EIDE_OPTICAL_DMAACK_L	L:S:4500 MIL:6500 MIL						33.00 MHz
	EIDE_OPTICAL_DMA_RQ	L:S:4500 MIL:6500 MIL						33.00 MHz
ETHERNET MII	ENET_LINK_RXD<7..0>	L:S:8000:9000	7	(400)		(400)		
	ENET_RX_DV	L:S:8000 MIL:9000 MIL						
	ENET_RX_ER	L:S:8000 MIL:9000 MIL						
	ENET_PHY_TXD<7..0>	L:S:8000:9000	7	(400)		(400)		
	ENET_LINK_TXD<7..0>	L:S::600						
	ENET_PHY_TX_ER	L:S:8000 MIL:9000 MIL						
	ENET_LINK_TX_ER	L:S::400 MIL						
	ENET_PHY_TX_EN	L:S:8000 MIL:9000 MIL						
	ENET_LINK_TX_EN	L:S::400 MIL						
	ENET_MDIO	L:S:8000 MIL:9000 MIL						
	ENET_MDC	L:S:8000 MIL:9000 MIL						
	ENET_COL	L:S:8000 MIL:9000 MIL						
	ENET_CRS	L:S:8000 MIL:9000 MIL						
FIREWIRE MII	FW_LINK_DATA<7..0>	L:S:2700:3500	7	(400)		(400)		
	FW_PHY_DATA<7..0>	L:S:4700:5500	7	(400)		(400)		
	FW_LINK_CNTL<1..0>	L:S:9000:10000						
	FW_PHY_CNTL<1..0>	L:S::300						
	FW_LINK_LREQ	L:S::300 MIL						
	FW_PHY_LREQ	L:S:8500 MIL:9500 MIL						
	FW_PINT	L:S:8500 MIL:9500 MIL						

PRIORITY: 4
PRIMARY LAYERS: 9
SECONDARY LAYERS: 4,7
GOAL: MINIMIZE TH VIAS

PRIORITY: 7
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 6
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 8
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 5
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 5
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR	RELATIVE_PROPAGATION_DELAY	MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS
FIREWIRE Zo = 110	FW_TPI0N	FW_TPI0	FW_TPI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPI0P	FW_TPI0	FW_TPI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPO0N	FW_TPO0	FW_TPO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPO0P	FW_TPO0	FW_TPO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPBI0N	FW_TPBI0	FW_TPBI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPBI0P	FW_TPBI0	FW_TPBI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPAO0N	FW_TPAO0	FW_TPAO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPAO0P	FW_TPAO0	FW_TPAO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPA1N	FW_TPA1	FW_TPA1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPA1P	FW_TPA1	FW_TPA1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPB1N	FW_TPB1	FW_TPB1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPB1P	FW_TPB1	FW_TPB1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPI1N	FW_TPI1	FW_TPI1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPI1P	FW_TPI1	FW_TPI1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPO1N	FW_TPO1	FW_TPO1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPO1P	FW_TPO1	FW_TPO1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
ETHERNET Zo = 100	MDI_P<0>	ENET_MDI0	ENET_MDI0:G:U43.29:J23.1:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_M<0>	ENET_MDI0	ENET_MDI0:G:U43.31:J23.2:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_P<1>	ENET_MDI1	ENET_MDI1:G:U43.33:J23.3:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_M<1>	ENET_MDI1	ENET_MDI1:G:U43.34:J23.4:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_P<2>	ENET_MDI2	ENET_MDI2:G:U43.39:J23.7:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_M<2>	ENET_MDI2	ENET_MDI2:G:U43.41:J23.8:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_P<3>	ENET_MDI3	ENET_MDI3:G:U43.42:J23.9:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_M<3>	ENET_MDI3	ENET_MDI3:G:U43.43:J23.10:0 MIL:100 MIL		ENET 11 MIL SPACING	
LVDS Zo = 100 LOWER	CLKLVDS_LN	CLKLVDS_L	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4
	CLKLVDS_LP	CLKLVDS_L	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4
	LVDS_L0N	LVDS_L0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L0P	LVDS_L0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L1N	LVDS_L1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L1P	LVDS_L1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L2N	LVDS_L2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L2P	LVDS_L2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
UPPER	CLKLVDS_UN	CLKLVDS_U	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4
	CLKLVDS_UP	CLKLVDS_U	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4
	LVDS_U0N	LVDS_U0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U0P	LVDS_U0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U1N	LVDS_U1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U1P	LVDS_U1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U2N	LVDS_U2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U2P	LVDS_U2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
TMDS Zo = 100	TMDS_CLKN	CLKTMDS	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	5
	TMDS_CLKP	CLKTMDS	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	5
	TMDS_DN<0>	TMDS_D0		500.0000	100 OHM SPACING	8
	TMDS_DP<0>	TMDS_D0		500.0000	100 OHM SPACING	8
	TMDS_DN<1>	TMDS_D1		500.0000	100 OHM SPACING	8
	TMDS_DP<1>	TMDS_D1		500.0000	100 OHM SPACING	8
	TMDS_DN<2>	TMDS_D2		500.0000	100 OHM SPACING	8
	TMDS_DP<2>	TMDS_D2		500.0000	100 OHM SPACING	8
	ATI_TMDS_CLKN	ATI_CLKTMDS	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	5
	ATI_TMDS_CLKP	ATI_CLKTMDS	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	5
	ATI_TMDS_DN<0>	ATI_TMDS_D0		200.0000	100 OHM SPACING	8
	ATI_TMDS_DP<0>	ATI_TMDS_D0		200.0000	100 OHM SPACING	8
	ATI_TMDS_DN<1>	ATI_TMDS_D1		200.0000	100 OHM SPACING	8
	ATI_TMDS_DP<1>	ATI_TMDS_D1		200.0000	100 OHM SPACING	8
	ATI_TMDS_DN<2>	ATI_TMDS_D2		500.0000	100 OHM SPACING	8
	ATI_TMDS_DP<2>	ATI_TMDS_D2		500.0000	100 OHM SPACING	8
USB 1.1 Zo = 90	USB_DEM	USB_DE	USB_DE:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	USB_DEP	USB_DE	USB_DE:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	USB_DFM	USB_DF	USB_DF:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	USB_DFP	USB_DF	USB_DF:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
USB 2.0 Zo = 90	BT_USB_DM	BT_USB_D	BT_USB:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	BT_USB_DP	BT_USB_D	BT_USB:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	MODEM_USB_DM	MODEM_USB_D	MODEM_USB:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	MODEM_USB_DP	MODEM_USB_D	MODEM_USB:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	NEC_USB_DAM	USB_D1	USB_D1:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	
	NEC_USB_DAP	USB_D1	USB_D1:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	
	NEC_USB_DBM	USB_D2	USB_D2:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	
	NEC_USB_DBP	USB_D2	USB_D2:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	
POWER SUPPLIES	1772_CSSN	1772_CSS	1772_CSS:G:L:S:0 MIL:100 MIL			
	1772_CSSP	1772_CSS	1772_CSS:G:L:S:0 MIL:100 MIL			
	1772_CSIN	1772_CSI	1772_CSI:G:L:S:0 MIL:100 MIL			
	1772_CSIP	1772_CSI	1772_CSI:G:L:S:0 MIL:100 MIL			
	3V_SNSM	3V_SNS	3V_SNS:G:L:S:0 MIL:100 MIL			
	3V_SNSP	3V_SNS	3V_SNS:G:L:S:0 MIL:100 MIL			
	5V_SNSM	5V_SNS	5V_SNS:G:L:S:0 MIL:100 MIL			
	5V_SNSP	5V_SNS	5V_SNS:G:L:S:0 MIL:100 MIL			
THERMOSTAT	THERM1_DM		THERM1:G:L:S:0 MIL:100 MIL			
	THERM1_DP		THERM1:G:L:S:0 MIL:100 MIL			
	THERM2_DM		THERM2:G:L:S:0 MIL:100 MIL			
	THERM2_DP		THERM2:G:L:S:0 MIL:100 MIL			
	THERM1_M_DM	THERM1_MAIN	THERM1_MAIN:G:L:S:0 MIL:100 MIL			
	THERM1_M_DP	THERM1_MAIN	THERM1_MAIN:G:L:S:0 MIL:100 MIL			
	THERM2_M_DM	THERM2_MAIN	THERM2_MAIN:G:L:S:0 MIL:100 MIL			
	THERM2_M_DP	THERM2_MAIN	THERM2_MAIN:G:L:S:0 MIL:100 MIL			
	THERM1_A_DM	THERM1_ALT	THERM1_ALT:G:L:S:0 MIL:100 MIL			
	THERM1_A_DP	THERM1_ALT	THERM1_ALT:G:L:S:0 MIL:100 MIL			
	THERM2_A_DM	THERM2_ALT	THERM2_ALT:G:L:S:0 MIL:100 MIL			
	THERM2_A_DP	THERM2_ALT	THERM2_ALT:G:L:S:0 MIL:100 MIL			

PRIORITY: 3
PRIMARY LAYERS: 4,7 FOR CONTROLLED IMPEDANCE DIFF PAIRS
SECONDARY LAYERS: 2,9 FOR UNCONTROLLED IMPEDANCE DIFF PAIRS

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3MIL (TRACE WIDTH)
S = 11MIL (TRACE SEPERATION)
H = 16.8MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 106.2 OHMS
Zo(single) = 55.4 OHMS

Clear adjacent power plane!
Zo will be lower due to asymmetric stackup.

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3.1MIL (TRACE WIDTH)
S = 4.9MIL (TRACE SEPERATION)
H = 9.6MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 94 OHMS
Zo(single) = 50 OHMS

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3.9MIL (TRACE WIDTH)
S = 5.6MIL (TRACE SEPERATION)
H = 9.6MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 89.8 OHMS
Zo(single) = 46.6 OHMS

LAYERS 2 OR 9

SIGNAL CONSTRAINTS - PAGE 2

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	B
SCALE: NONE	SHT 37 OF 44	

POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
MAIN/SLEEP	+24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+BATT	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23 39
	+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=6	MIN_NECK_WIDTH=6	39
	+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+2_5V_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	39
	+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP_VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30 31 39
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30 38
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30 38
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30 39
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30 39
	1772_DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		30
	1772_LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	30
	1772_LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		30
	1772_DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		30
	1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10		30
PMU	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	+4_85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		29 31
	+4_6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10		31 32
	+4_85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		31
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		31
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		25 29
MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24 32
	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24
TRACKPAD	+5V_TPAD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=10		23 39
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		23 39
VIDEO	+14V_INV	VOLTAGE=14V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	22 39
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
AUDIO	+5V_MAIN_AUD	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 32
	+3V_MAIN_AUD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 32
	AUD_GND	VOLTAGE=0V	MIN_LINE_WIDTH=50		25
FAN	+FAN_PWR	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 39
	FAN1_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	FAN2_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39

I/O AREA	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	IN	
INVERTER	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN	CHGND1
TRACKPAD	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN	CHGND2
LVDS	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN	CHGND3
	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN	CHGND4

ENET_CTAP_CHGND VOLTAGE=0V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=12

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 6 33 39
	CPU_AVDD	VOLTAGE=1.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 6 7 8 15 16 33
	I162 CPU_AVDD_VIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
	I163 CPU_AVDD_VOUT	VOLTAGE=1.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
DDR RAM	DDR_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		11
INTREPID	I148 +2_5V_INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	9 10 15 16
	+3V_INTREPID_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14
PLLS	+1_5V_INTREPID_PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	8 12 14
	+1_5V_INTREPID_PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	8
	+1_5V_INTREPID_PLL8	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
REFERENCE	INT_MEM_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		9
	INT_AGP_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		12 19
	INT_MEM_REF_H	VOLTAGE=0V	MIN_LINE_WIDTH=10		9
	UIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8		13
AIRPORT	+3V_AIRPORT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
CARDBUS	I165 +3V_SLEEP_PCCARD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
ATI M11	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	19 20 39
	+3V_GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 19 20 21
	+3V_GPU_FLT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+2_5V_GPU	VOLTAGE=2.5V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	
	GPU_MEM_IO	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	19 21
	GPU_MEM_IO_FLT	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+2_5V_GPU_MEMCORE	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+1_8V_GPU	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	19 20 21
	+1_5V_AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 15 16 19 20 21
	+2_5V_GPU_PNLIO	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_8V_ATI_PVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20 21
	+1_5V_AGP_GPU	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_5V_GPU_VDD15	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	+1_8V_GPU_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_VDDDI	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	GPU_VCORE_VDDCI	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	+2_5V_GPU_A2VDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_PNLPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_PNLIO	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+2_5V_GPU_MCLK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_AVDDQ	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_MEMPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+3V_ATI_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	+3V_ATI_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	I144 +GPU_VDD15_UF	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	I144 +2_5V_SLEEP_NECK1	VOLTAGE=2.5V	MIN_LINE_WIDTH=10		20
	I144 +3V_SLEEP_NECK	VOLTAGE=3V	MIN_LINE_WIDTH=10		34
	I144 +1_5V_AGP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		20
	I144 +1_8V_PVDD_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		20
	I145 GPU_VCORE_NECK	VOLTAGE=1.2V	MIN_LINE_WIDTH=10		20
	I145 +GPU_VDD15_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		20
	I145 +2_5V_SLEEP_NECK2	VOLTAGE=2.5V	MIN_LINE_WIDTH=10		34
	I145 +1_8V_SLEEP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		34
	I145 +1_5V_SLEEP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		34
	I146 +1_8V_ATI_TPVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	I146 +1_8V_GPU_TP_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
ETHERNET 88E1111 NEC USB2.0	+2_5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+2_5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+1_0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	I141 +3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
	I141 NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	17
FW	I142 LM2594_IN	VOLTAGE=33V	MIN_LINE_WIDTH=40	MIN_NECK_WIDTH=12	27
	I143 +FW_PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	+FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	I144 +FW_AMP_SENSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	
	+FW_PWR_OR	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	27 28
	I141 +FW_PWR1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	+FW_VP0	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28 39
	+FW_VP1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28 39
	+3V_FW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27 28
	+3V_FW_UF	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_PLLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	I141 FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	I145 FW_VDD_ON	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	1625_VSW	VOLTAGE=14V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+PBUS_JUMPER	VOLTAGE=14V	MIN_LINE_WIDTH=10		
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		31
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		31
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		31
	1V20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	30 31
LTC3707 5V SWITCHER	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	32
	5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+5V_MAIN_JUMPER	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
3V SWITCHER	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+3V_MAIN_JUMPER	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		32
MAX1715 2.5V SWITCHER	2_5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	34
	2_5V_LX_F	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	
	2_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	2_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	2_5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	2_5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
1.65V SWITCHER	1_5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8		34
	1_5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	34
	1_5V_LX_F	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	
	1_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	1_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	1_5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	1_5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
CONTROL	1_5V_ILIM		MIN_LINE_WIDTH=8		34
	2_5V_ILIM		MIN_LINE_WIDTH=8		34
	MAX1715_TON		MIN_LINE_WIDTH=8		34
	MAX1715_SKIP		MIN_LINE_WIDTH=8		34
	MAX1715_REF	VOLTAGE=2.0V	MIN_LINE_WIDTH=8		34
	MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
MAX1717	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	33
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=200	MIN_NECK_WIDTH=10	33
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	33
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	33
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	33
	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	33
	VCORE_ILIM		MIN_LINE_WIDTH=8		33
	VCORE_REF		MIN_LINE_WIDTH=8		33
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8		33
	VCORE_CC		MIN_LINE_WIDTH=8		33
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		33 39
	VCORE_TIME		MIN_LINE_WIDTH=8		33
	VCORE_VGATE		MIN_LINE_WIDTH=8		14 33
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30		33
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8		33
	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		33
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8		33
	I131 VCORE_GNDA	VOLTAGE=0V	MIN_LINE_WIDTH=10		33
LTC1778	1778_VIN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1778_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1778_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	20
	1778_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	20
	1778_BST_RC	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	20
	1778_TG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1778_BG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	GPU_VCORE_SW	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	20
	GPU_VCORE_SW_F	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	
	1778_ION		MIN_LINE_WIDTH=8		20
	1778_ITH		MIN_LINE_WIDTH=8		20
	1778_ITH_RC		MIN_LINE_WIDTH=8		20
	1778_VFB		MIN_LINE_WIDTH=8		20 39
	1778_FCB		MIN_LINE_WIDTH=8		20
	1778_VRNG		MIN_LINE_WIDTH=8		20
LTC3411	LTC3411_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	LTC3411_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
	1_8V_SW	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
	1_8V_SW_F	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	
	1_8V_VFB		MIN_LINE_WIDTH=8		34
	LTC3411_ITH_RC		MIN_LINE_WIDTH=8		34
	LTC3411_ITH		MIN_LINE_WIDTH=8		34
	LTC3411_SYNC		MIN_LINE_WIDTH=8		34
	LTC3411_SHDN		MIN_LINE_WIDTH=8		34
LTC1962 INT PLLS	LTC1962_INT_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	14
CY28512D LMU CONN	I136 +3V_MAIN_SSCG	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	I136 +3V_MAIN_LMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23
OPT DRIVER	I136 +5V_SLEEP_OPT	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24

SIGNAL CONSTRAINTS - PAGE 3

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	B
SCALE: NONE	SHT	38 44

FUNCTIONAL TEST POINTS

PROBES ARE ON BOTTOM SIDE. MINIMUM PAD/HOLE SIZE IS 25 MIL.
FUNC TEST IS ONLY PROPERTY USED BY THE TOOLS. FUNC_QTY IS FOR REFERENCE AND LISTS THE NUMBER OF TEST POINTS ON THAT NET AND WITHIN THAT GROUP/CONNECTOR.
FUNC_DIST IS SIMILARLY USED TO DEFINE MAXIMUM DISTANCE FROM A CONNECTOR.

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
SCAN/TEST	J2 JTAG_ASIC_TMS	TRUE			13 26
	J3 JTAG_ASIC_TDI	TRUE			13
	J1 JTAG_ASIC_TDO_TP	TRUE			26
	J4 JTAG_ASIC_TCK	TRUE			13 26
	J6 JTAG_ASIC_TRST_L	TRUE			13 26
	J5 CPU_CHKSTP_OUT_L	TRUE			5
	J7 CPU_SRESET_L	TRUE			5
	J9 CPU_HRESET_L	TRUE			5 6 7
	J8 JTAG_CPU_TMS	TRUE			5 6
	J10 JTAG_CPU_TDI	TRUE			5 6
	J12 JTAG_CPU_TDO_TP	TRUE			5
	J11 JTAG_CPU_TCK	TRUE			5 6
	J13 JTAG_CPU_TRST_L	TRUE			5 6
	J18 INT_JTAG_TEI	TRUE			13
	J20 INT_TST_MONIN_PD	TRUE			13
	J19 INT_TST_MONOUT_TP	TRUE			13
	J21 INT_TST_PLLEN_PD	TRUE			13
INT I2C	J15 INT_I2C_CLK0	TRUE			6 11 13 23
	J14 INT_I2C_DATA0	TRUE			6 11 13 23
	J16 INT_I2C_CLK1	TRUE			13 14 25
	J17 INT_I2C_DATA1	TRUE			13 14 25
PWR/GND	L21 +PBUS	TRUE			38
	L21 +24V_PBUS	TRUE			38
	L25 GPU_VCORE	TRUE			19 20 38
	L24 1778_VFB	TRUE			20 38
	L27 CPU_VCORE_SLEEP	TRUE			5 6 33 38
	L26 VCORE_FB	TRUE			33 38
	L21 +1_8V_MAIN	TRUE			38
	L21 +2_5V_MAIN	TRUE			38
	L21 +5V_MAIN	TRUE	2		38 39
	L22 +5V_SLEEP	TRUE	2		38 39
	L22 +3V_MAIN	TRUE	4		23 38
		TRUE		1000	IN
	L22 +3V_PMU	TRUE			38
CARDBUS	K36 CBUS_DET_1_L	TRUE		2000	18
	K35 CBUS_DET_2_L	TRUE		2000	18
DVI	K37 TMDS_DN<0..2>	TRUE		1000	19 22 37
	K38 TMDS_DP<0..2>	TRUE		1000	19 22 37
	K40 TMDS_CONN_CLKN	TRUE		1000	22 36
	K39 TMDS_CONN_CLKP	TRUE		1000	22 36
	L42 VGA_R	TRUE		1000	22
	L41 VGA_G	TRUE		1000	22
	L44 VGA_B	TRUE		1000	22
	L43 VGA_HSYNC	TRUE		1000	22
	L46 VGA_VSYNC	TRUE		1000	22
	L45 DVI_DDC_CLK_UF	TRUE		1000	22
	L47 DVI_DDC_DATA_UF	TRUE		1000	22
	L48 DVI_HPD_UF	TRUE		1000	22
	L49 +5V_DDC_SLEEP	TRUE		2000	22 38
		TRUE	2	2000	IN
CHGND1		TRUE	6	1000	IN
LVDS	L52 LVDS_L0N	TRUE		1000	20 22 37
	L51 LVDS_L0P	TRUE		1000	20 22 37
	L53 LVDS_L1N	TRUE		1000	20 22 37
	L55 LVDS_L1P	TRUE		1000	20 22 37
	L54 LVDS_L2N	TRUE		1000	20 22 37
	L57 LVDS_L2P	TRUE		1000	20 22 37
	L56 CLKLVDS_LN	TRUE		1000	20 22 37
	L58 CLKLVDS_LP	TRUE		1000	20 22 37
	L59 LVDS_DDC_CLK	TRUE		1000	20 22
	L60 LVDS_DDC_DATA	TRUE		1000	20 22
	L62 +3V_LCD	TRUE	2	2000	22 38
	L22 +3V_SLEEP	TRUE		2000	38 39
		TRUE	2	2000	IN
CHGND4		TRUE	6	1000	IN
INVERTER	L67 +14V_INV	TRUE		2000	22 38
	L66 +5V_INV_SW	TRUE		2000	22 38
	L68 BRIGHT_PWM	TRUE		2000	22
	L24 INV_GND	TRUE		2000	22
		TRUE		1000	IN
S-VIDEO	L70 TV_C	TRUE		2000	22
	L72 TV_Y	TRUE		2000	22
	L71 TV_COMP	TRUE		2000	22
	L73 TV_GND1	TRUE		2000	22 38
	L74 TV_GND2	TRUE		2000	22 38
LIO	L76 INT_I2S0_SND_TO_DAC	TRUE		1000	14 25
	L75 INT_I2S0_SND_LRCLK	TRUE		1000	14 25
	L78 INT_I2S0_SND_MCLK	TRUE		1000	14 25 35
	L83 INT_I2S0_SND_SCLK	TRUE		1000	14 25
	L82 INT_I2S0_SND_FROM_ADC	TRUE		1000	14 25
	L77 SND_HP_MUTE_L	TRUE		1000	14 25
	L79 SND_AMP_MUTE	TRUE		1000	25
	L84 SND_HW_RESET_L	TRUE		1000	14 25
	L85 SND_HP_SENSE_L	TRUE		1000	14 25
	L86 SND_LIN_SENSE_L	TRUE		1000	14 25
	L81 INT_I2C_CLK2	TRUE		1000	14 25
	L80 INT_I2C_DATA2	TRUE		1000	14 25
	L87 ADAPTER_DET	TRUE		1000	25 29
	L88 CHARGE_LED_L	TRUE		1000	25 29
	L89 NEC_LUSB_OCI_UF	TRUE		1000	17 25
	L90 NEC_LUSB_PPON	TRUE		1000	17 25
	L22 +5V_MAIN	TRUE	2	2000	38 39
	L22 +5V_SLEEP	TRUE	2	3000	38 39
	L22 +3V_SLEEP	TRUE		2000	38 39

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
USB	L94 NEC_USB_DAM	TRUE			17 25 37
	L96 NEC_USB_DAP	TRUE			17 25 37
	L95 NEC_USB_DBM	TRUE			17 25 37
	L97 NEC_USB_DBP	TRUE			17 25 37
	L98 BT_USB_DM	TRUE			14 25 37
	L99 BT_USB_DP	TRUE			14 25 37
	L10 MODEM_USB_DM	TRUE			14 25 37
	L10 MODEM_USB_DP	TRUE			14 25 37
RT. USB	L10 NEC_RUSB_PPON	TRUE			17 25
	L10 NEC_RUSB_OCI_UF	TRUE			17 25
WIRELESS	L10 PCI_AD<0..31>	TRUE		1000	9 12 17 18 24 37
	L10 PCI_FRAME_L	TRUE		1000	12 17 18 24 37
	L10 PCI_TRDY_L	TRUE		1000	12 17 18 24 37
	L10 PCI_IRDY_L	TRUE		1000	12 17 18 24 37
	L10 PCI_DEVSEL_L	TRUE		1000	12 17 18 24 37
	L10 PCI_STOP_L	TRUE		1000	12 17 18 24 37
	L11 PCI_PAR	TRUE		1000	12 17 18 24 37
	L11 AIRPORT_PCI_REQ_L	TRUE		1000	12 24
	L11 AIRPORT_PCI_GNT_L	TRUE		1000	12 24
	L11 AIRPORT_PCI_INT_L	TRUE		1000	14 24
	L11 MAIN_RESET_L	TRUE		1000	14 17 18 19 24 29
	L11 CLK33M_AIRPORT	TRUE		1000	12 24 35
	L11 PMU_PME_L	TRUE		1000	14 17 24 29
	L11 ROM_ONBOARD_CS_L	TRUE		1000	9
	L11 ROM_OE_L	TRUE		1000	9 12
	L11 ROM_CS_L	TRUE		1000	9 12
	L11 ROM_RW_L	TRUE		1000	9 12
	L12 RF_DISABLE_L	TRUE		1000	24
	L12 AIRPORT_CLKRUN_L	TRUE		1000	24
	L12 +3V_AIRPORT	TRUE	4	2000	38
		TRUE	6	1000	IN
OPTICAL	L12 EIDE_OPTICAL_DATA<0..15>	TRUE		2000	24 37
	L12 EIDE_OPTICAL_DMA_RQ	TRUE		2000	24 37
	L12 EIDE_OPTICAL_READ_L	TRUE		2000	24 37
	L12 EIDE_OPTICAL_DMAACK_L	TRUE		2000	24 37
	L12 EIDE_OPTICAL_ADDR<0..2>	TRUE		2000	24 37
	L12 EIDE_OPTICAL_CS0_L	TRUE		2000	24 37
	L12 EIDE_OPTICAL_CS1_L	TRUE		2000	24 37
	L13 EIDE_OPTICAL_RST_L	TRUE		2000	24 37
	L13 EIDE_OPTICAL_WR_L	TRUE		2000	24 37
	L13 EIDE_OPTICAL_IOCHRDY	TRUE		2000	24 37
	L13 EIDE_OPTICAL_INT	TRUE		2000	24 37
TRACKPAD	L13 +5V_TPAD_SLEEP	TRUE		3000	23 38
	L13 TPAD_F_TXD	TRUE		3000	23
	L13 TPAD_F_RXD	TRUE		3000	23
	L13 LID_CLOSED_L	TRUE		3000	23
	L13 +3V_HALL_EFFECT	TRUE		3000	23 38
	L13 SOFT_PWR_ON_L	TRUE		3000	22 23 29 33
MODEM/ SERIAL	L14 COMM_RESET_L	TRUE		4000	14 25
	L14 COMM_SHUTDOWN	TRUE		4000	14 25
	L14 COMM_RING_DET_L	TRUE		4000	14 25 29
	L14 COMM_TXD_L	TRUE		4000	14 25
	L14 COMM_TRXC	TRUE		4000	14 25
	L14 COMM_GPIO_L	TRUE		4000	14 25
	L14 COMM_DTR_L	TRUE		4000	14 25
	L14 COMM_RTS_L	TRUE		4000	14 25
	L14 COMM_RXD	TRUE		4000	14 25
KEYBOARD	L14 KBD_ID	TRUE		3000	23 29
	L15 KBD_INTL	TRUE		3000	23
	L15 KBD_JIS	TRUE		3000	23
	L15 KBD_CAPSLOCK_LED	TRUE		3000	23
	L15 KBD_NUMLOCK_LED	TRUE		3000	23
	L15 KBD_FUNCTION_L	TRUE		3000	23 29
	L15 KBD_COMMAND_L	TRUE		3000	23 29
	L15 KBD_OPTION_L	TRUE		3000	23 29
	L15 KBD_CONTROL_L	TRUE		3000	23 29
	L15 KBD_SHIFT_L	TRUE		3000	23 29
	L15 KBD_X<0..9>	TRUE		3000	23 29
	L15 KBD_Y<0..7>	TRUE		3000	23 29
BATTERY	L16 +BATT_POS	TRUE	(100 MIL PROBE PREFERRED)	1000	30 38
	L16 BATT_NEG	TRUE	(100 MIL PROBE PREFERRED)	1000	30 38
	L16 BATT_CLK	TRUE		1000	30
	L16 BATT_DATA	TRUE		1000	30
	L16 PMU_BATT_DET_L	TRUE		1000	29 30
FANS	L16 +FAN_PWR	TRUE		3000	25 38
	L16 FAN1_TACH	TRUE		3000	25
	L16 FAN2_TACH	TRUE		3000	25
	L17 FAN1_GND	TRUE		3000	38
	L17 FAN2_GND	TRUE		3000	38
ETHERNET	L17 MDI_P<0..3>	TRUE		1000	26 37
	L17 MDI_M<0..3>	TRUE		1000	26 37
FIREWIRE	L17 FW_TPO0P	TRUE		1000	27 28 37
	L17 FW_TPO0N	TRUE		1000	27 28 37
	L17 FW_TPO0R	TRUE		1000	28
	L17 FW_TPI0P	TRUE		1000	27 28 37
	L17 FW_TPI0N	TRUE		1000	27 28 37
	L18 +FW_VP0	TRUE		1000	28 38
	L18 FW_VGND	TRUE		1000	39

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
FIREWIRE (CONT.)	L18 FW_TPO1P	TRUE		1000	28 37
	L18 FW_TPO1N	TRUE		1000	28 37
	L18 FW_TPI1P	TRUE		1000	28 37
	L18 FW_TPI1N	TRUE		1000	28 37
	L18 +FW_VP1	TRUE		1000	28 38
	L18 FW_VGND	TRUE		1000	39
DC PWR IN	L18 +ADAPTER	TRUE	3 (100 MIL PROBE PREFERRED)	1000	30 31 38
LMU/ALS	L23 ST7_SLEEP_LED_H	TRUE			23
	L23 PMU_SLEEP_LED	TRUE			23
	L23 PMU_LID_CLOSED_L	TRUE			23 29
	L23 LMU_DETECT	TRUE			23
		TRUE	6	1000	IN
			(100 MIL PROBE PREFERRED)		
MISC.	L19 SLEEP_LED	TRUE			23
	L19 PMU_KB_RESET_L	TRUE			29
	L19 SLEEP	TRUE			23 25 29 32 34
	L19 PMU_CPU_HRESET_L	TRUE			6 29
	L19 BB_RESET_L	TRUE			6
	L24 +3V_PMU_RESET	TRUE			29 33

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6570 | REV. B
SCALE NONE | SHT 39 OF 44

REVISION HISTORY

Proto/EVT Release

10/27/03 - 1. Schematic originated from Q16 MLB

11/10/03 - 1. Replace U56 symbol
2. Connect OVDDSENSE to MAXBUS_SLEEP
3. Modify SRN0, SRN1 and IARTRXD connection
4. Connect VID1(Page 6) to CPU_VCORE_SLEEP(PAGE 5)
5. Connect SENSEVDD to CPU_VCORE_SLEEP
6. Connect SENSEGND to GND
7. Add 4 pcs 0 ohm resistor for AMD BootRom issue (R1,R194,R236,R271)
8. Connect TEMP_ANODE and TEMP_CATHODE to AD17460
9. Modify CPU PLL config
10. Add 0 ohm resistor on CG_FSEL Interpid side(R450)
11. Replace U47 symbol
12. Change R743 from 2m ohm to 1m ohm
13. Change C774,C781,C788,C793,C797,C802 from 220uF to 330uF
14. Change R748 from 410 ohm to 10 Ohm

12/01/03 - 1. Modify CPU_VCORE setting.

12/02/03 - 1. Modify CPU_BTR CPU_VCORE VID setting

12/05/03 - 1. Add CPU_AVDD LDO (Page 5)
2. Change Q45 and Q41 to IRF7805 (376S0035)
3. Change Q47 and Q42 to IRF7811W (376S0104)
4. Change R402 and R409 to 4.7ohm resistors
5. Connect INT_TDO from intrepid to Cypress Chip PD* (U31)

12/12/03 - 1. Add R468 and R601 for MAX1715 2.5V adjust
2. Modify CPU_VCORE setting to Motorola new spec
3. Modify LDO power sequence

12/16/03 - 1. Add 10K pull down for INT_TDO on page 13

12/17/03 - 1. Change LDO Vin from +3V_MAIN to +3V_SLEEP
2. Connect INT_TDO from Intrepid to Marvell 88E1111(U43)
3. Add R755,R756,R758,R759 for power rail

DVT Release (Rev. 02)

01/30/04 - 1. Add Soft Modem(Pin#14) 10K pull-up at J15.7 (Pg 25)
2. Add Bom Table for R97 2.21K ohm VCore offset (Pg 33)

02/04/04 - 1. C811 change to 4.7uF per MOT A7PM requirement (Pg 5)
2. NO STUFF R236,R1,R271&R194 to remove PCI stub (Pg 9)

DVT Release (Rev. 03)

02/12/04 - 1. CPU VCore adjustment for V1.1 A7PM CPU (Pg 33)
2. CPU AVDD adjustment for V1.1 A7PM CPU (Pg 5)
3. AT INT. TMDS termination change to 0 ohm, Qty:8 (Pg 20)
4. AGP I/O VREF voltage divider chagne to both 1K ohm (Pg 12)

DVT Release (Rev. 04)

02/13/04 - 1. INT. TMDS Termination change to 2* 49.9ohm = 100ohm (Pg 20)

PVT Release (Rev. A)

03/11/04 - 1. INT. TMDS Termination change to 2* 75 ohm = 150ohm (except CLK pair) (Pg 20)
2. USB series termination near NEC PHY change to 47 ohm (Pg 17)

PVT Release (Rev. A)

04/02/04 - 1. USB series termination near NEC PHY change to 43.2 ohm (Pg 17)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	B
SCALE: NONE	SHT: 40	44

*** Signal Cross-Reference for the entire design ***

```
+1_0V_MARVELL    26D2< 38B3>
+1_5V_AGP        12B5< 12D1< 12D4< 15D6< 16C8<
               19C6< 19D6< 20A8< 20B4<> 20D5<>
               21B8< 21D6< 38C3>
+1_5V_AGP_GPU    21C5< 38C3>
+1_5V_AGP_NECK   20B4<> 38B3>
+1_5V_GPU_VDD15  20D3< 38C3>
+1_5V_INTREPID_PLL  8D6< 12D4< 12D8< 14D6<> 38D3>
+1_5V_INTREPID_PLL1  14C3< 38D3>
+1_5V_INTREPID_PLL2  14D3< 38D3>
+1_5V_INTREPID_PLL3  14D3< 38D3>
+1_5V_INTREPID_PLL4  14D3< 38D3>
+1_5V_INTREPID_PLL5  12D3< 38D3>
+1_5V_INTREPID_PLL6  12D6< 38D3>
+1_5V_INTREPID_PLL7  8D5< 38D3>
```

```
PMU_AC_IN         29B4<>
PMU_BATT0_DET_L   29B4<>
PMU_BATT1_DET_L_PU  29B4<> 29D2<
PMU_BATT_DET_L    29B3< 29D2< 30A4<> 39A3>
PMU_BYTE          29B6< 29C7<
PMU_CAPSLOCK_LED_L  29C6<>
PMU_CHARGE_V      29C4<> 30B8<>
PMU_CHRG_BATT_G   29C4<> 30A8<>
PMU_CLK           14C2<> 29C4<>
PMU_CNVSS         29B6< 29C7<
PMU_CPU_RESET_L   6A2< 6C3<> 29C4<> 39C1>
PMU_EPM           29C4<> 29D2<
PMU_FROM_IWF      14C2<> 29C4<>
PMU_I2C_CLK       29B4<> 29C2<
PMU_I2C_DATA      29B4<> 29C2<
PMU_INT_L         14B5<> 14B7< 29B6<>
PMU_INT_NMI       14B5<> 14B7< 29D4<>
PMU_KB_RESET_IN1  29A7<>
PMU_KB_RESET_IN2  29A7<>
PMU_KB_RESET_L    29A6> 29B7< 39C1>
PMU_LID_CLOSED_L  23B< 23D6<> 29B2< 29C4<> 39D1>
PMU_SMI_BUTTON_L  29C2< 29C4<>
PMU_SMI_L         29C2< 29C4<>
PMU_SUMLOCK_LED_L  29C6<>
PMU_OOPS          29B2< 29B4<>
PMU_PME_L         14A5<> 17A8< 24D5<> 29B2< 29C4<>
                  39C3>
PMU_POWERUP_OK    29B4<> 29D2<
PMU_POWER_UP_L    28C8<> 29C6<> 29D7< 32B8<
PMU_RSQ_L         14B7< 14C2> 29C4<>
PMU_RESET_BUTTON_L  23A7< 29C4<> 29D2<
PMU_RESET_L       29B6<>
PMU_SLEEP_LED     23C7<> 23D6<> 39D1>
PMU_SLEEP_LED_L   23C8<> 29C4<>
PMU_SMB_CLK       29B4<> 29C2< 30A3<
PMU_SMB_DATA      29B4<> 29C2< 30A2<
PMU_TO_IWF        14C2<> 29C4<>
POWER_UP          28D7<>
POWER_VALID       29B2< 29C4<>
PWR_BUTTON_L      23A7< 23B4<>
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RAM_ADDR<12..0>   35A5>
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RAM_ADDR<2>       9B4< 11B3<> 11B6<>
RAM_ADDR<3>       9B4< 11B5<> 11B8<>
RAM_ADDR<4>       9B4< 11B3<> 11B6<>
RAM_ADDR<5>       9B4< 11B5<> 11B8<>
RAM_ADDR<6>       9B4< 11B3<> 11B6<>
RAM_ADDR<7>       9B4< 11B5<> 11B8<>
RAM_ADDR<8>       9B4< 11B3<> 11B6<>
RAM_ADDR<9>       9A4< 11B5<> 11B8<>
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RAM_ADDR<12>      9A4< 11B5<> 11B8<>
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RAM_BA<1..0>      35A5>
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RAM_CAS_L         9A4< 11B3<> 11B6<> 35A5>
RAM_CKE<0>        9A4< 9C4< 11C6<>
RAM_CKE<3..0>     35A5>
RAM_CKE<1>        9A4< 9C4< 11C8<>
RAM_CKE<2>        9A4< 9C4< 11C3<>
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RAM_CS_L<0>       9C4< 11B8<>
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RAM_CS_L<1>       9C4< 11B6<>
RAM_CS_L<2>       9C4< 11B5<>
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RAM_DATA_A<7..0>  35D5>
RAM_DATA_A<1>     10C8<> 11D8<>
RAM_DATA_A<2>     10C8<> 11D8<>
RAM_DATA_A<3>     10B8<> 11D8<>
RAM_DATA_A<4>     10B8<> 11D6<>
RAM_DATA_A<5>     10B8<> 11D6<>
RAM_DATA_A<6>     10B8<> 11D6<>
RAM_DATA_A<7>     10B8<> 11D6<>
RAM_DATA_A<8>     10B8<> 11D8<>
RAM_DATA_A<15..8>  35C5>
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RAM_DATA_A<10>    10C7<> 11D8<>
RAM_DATA_A<11>    10C7<> 11D8<>
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RAM_DATA_A<13>    10C7<> 11D6<>
RAM_DATA_A<14>    10C7<> 11D6<>
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RAM_DATA_A<23..16>  35C5>
RAM_DATA_A<17>    10C6<> 11C8<>
RAM_DATA_A<18>    10C6<> 11C8<>
RAM_DATA_A<19>    10C6<> 11C6<>
RAM_DATA_A<20>    10C6<> 11D3<>
RAM_DATA_A<21>    10C6<> 11C3<>
RAM_DATA_A<22>    10C6<> 11C3<>
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RAM_DATA_B<24>    10C6<> 11C5<>
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RAM_DATA_B<27>    10C6<> 11C5<>
RAM_DATA_B<31..27>  35C5>
RAM_DATA_B<28>    10C6<> 11C3<>
RAM_DATA_B<29>    10C6<> 11C3<>
RAM_DATA_B<30>    10C6<> 11C3<>
RAM_DATA_B<31>    10C6<> 11C3<>
RAM_DATA_B<32>   10D4<> 11B5<>
RAM_DATA_B<39..32>  35B5>
RAM_DATA_B<33>    10C4<> 11B5<>
RAM_DATA_B<34>    10C4<> 11B5<>
RAM_DATA_B<35>    10C4<> 11B5<>
RAM_DATA_B<36>    10C4<> 11B3<>
RAM_DATA_B<37>    10C4<> 11B3<>
RAM_DATA_B<38>    10C4<> 11B3<>
RAM_DATA_B<39>    10C4<> 11B3<>
RAM_DATA_B<40>    10C4<> 11B5<>
RAM_DATA_B<47..40>  35B5>
RAM_DATA_B<41>    10C4<> 11B5<>
RAM_DATA_B<42>    10C4<> 11B5<>
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RAM_DATA_B<44>    10C4<> 11B3<>
RAM_DATA_B<45>    10C4<> 11B3<>
RAM_DATA_B<46>    10C4<> 11A3<>
RAM_DATA_B<47>    10C4<> 11A3<>
RAM_DATA_B<48>    10D2<> 11A5<>
RAM_DATA_B<55..48>  35B5>
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RAM_DATA_B<63..56>  35A5>
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RAM_DATA_B<62>    10C2<> 11A3<>
RAM_DATA_B<63>    10C2<> 11A3<>
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RAM_DQM_A<1>      10C7<> 11D6<> 35C5>
RAM_DQM_A<2>      10B6<> 11C6<> 35C5>
RAM_DQM_A<3>      10C5<> 11C6<> 35C5>
RAM_DQM_A<4>      10B4<> 11B6<> 35B5>
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RAM_DQM_A<6>      10B2<> 11A6<> 35B5>
RAM_DQM_A<7>      10C1<> 11A6<> 35A5>
RAM_DQM_B<0>      10C8<> 11D3<> 35D5>
RAM_DQM_B<1>      10C8<> 11D3<> 35C5>
RAM_DQM_B<2>      10C6<> 11C3<> 35C5>
RAM_DQM_B<3>      10C6<> 11C3<> 35C5>
RAM_DQM_B<4>      10C4<> 11B3<> 35B5>
RAM_DQM_B<5>      10C4<> 11B3<> 35B5>
RAM_DQM_B<6>      10C2<> 11A3<> 35B5>
RAM_DQM_B<7>      10C2<> 11A3<> 35A5>
RAM_DQS_A<0>      10B8<> 11D8<> 35D5>
RAM_DQS_A<1>      10C7<> 11D8<> 35C5>
RAM_DQS_A<2>      10B6<> 11C8<> 35C5>
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RAM_DQS_B<2>      10C6<> 11C5<> 35C5>
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RAM_WE_L          9A4< 11B5<> 11B8<> 35A5>
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RF_DISABLE_L      24D6<> 39C3>
ROM_CS_L          9B3< 12A4< 39C3>
ROM_CS_TP_L       9C3< 24B6<>
ROM_OE_L          9B3< 12A4< 39C3>
ROM_OE_TP_L       9B3< 24C5<>
ROM_ONBOARD_CS_L  9B3< 39C3>
ROM_ONBOARD_CS_TP_L  9B3< 24C6<>
ROM_RW_L          9B3< 12A4< 39C3>
ROM_RW_TP_L       9B3< 24C6<>
ROM_WP_L          9B3<
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SI_EXT_SWING_SET  19C2<>
SI_HPD            19C4<
SI_I2C_CLK        19D4< 20C5<>
SI_I2S_DATA       19C4< 20C5<>
SI_MSEN           19D2<>
SI_PD_L           19C4<
SI_RST_L          19C4<
SI_TMDS_CLKN      19C2< 19C2<> 36D1>
SI_TMDS_CLKP      19C2<> 19C2< 36D1>
SI_TMDS_CLK_STM   19D1<
SI_TMDS_D0_STM    19D1<
SI_TMDS_D1_STM    19D1<
SI_TMDS_D2_STM    19C1<
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SI_TMDS_DP<1>     19B2< 19C2<> 36C1>
SI_TMDS_DP<2>     19B2< 19C2<> 36C1>
SI_VREF_ICOR_N    19C2< 19C4<
SLEEP             23D7<> 25D7<> 29B6<> 29D7< 32A4<
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SLEEP_LED_DGND    23C3>
SLEEP_LED_I       23D3<
SLEEP_LED_L       23D4<
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SLEEP_LED_UF      23D3<
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SLEEP_L_LS5       18D5< 20A7<> 26A8<> 32A5<> 33C7<>
                  34C8<
SLEEP_L_LS5_EN_L  32A6<>
SLEEP_L_LS5_INV   34A3< 34C2< 34C8<>
SLEEP_L_LS5_NET   32B3<> 34C8<>
SLEEP_NET         32A3<>
SLEEP_NET_INV     32A3<>
SND_AMP_MUTE      25C7<> 25D6<> 39A6>
SND_AMP_MUTE_CTRL  25B5<> 25D6<>
SND_AMP_MUTE_L    14B5<> 25D5<>
SND_HP_MUTE       25C5>
SND_HP_MUTE_L     14C5<> 25C5<> 39A6>
SND_HP_MUTE_LO    25C6<> 25C7<>
SND_HP_SENSE_L    14B5<> 25C8<> 39A6>
SND_HW_RESET_L    14A7< 14B5<> 25D7<> 39A6>
SND_LIN_SENSE_L   14B5<> 25C8<> 39A6>
SOFT_PWR_ON_L     22D1<> 23A3< 29A8< 29C6<> 29D7<
                  33A4<> 39B3>
ST7_SLEEP_LED_H   23C5<> 23C6<> 23D6<> 39D1>
STOP_ASP_L        12D2< 12D4<>
SYSCLK_CPU        5C3< 8A6< 35D1>
SYSCLK_CPU_UF     8A5<> 35D1>
SYSCLK_DDRCLK_A0  9D4< 11D8<> 35D1>
SYSCLK_DDRCLK_A0_L  9D4< 11D8<> 35C1>
SYSCLK_DDRCLK_A0_L_UF  9B6<> 9D5< 35D1>
SYSCLK_DDRCLK_A0_UF  9B6<> 9D5< 35D1>
SYSCLK_DDRCLK_A1  9D4< 11A6<> 35C1>
SYSCLK_DDRCLK_A1_L  9D4< 11A6<> 35C1>
SYSCLK_DDRCLK_A1_L_UF  9B6<> 9D5< 35D1>
SYSCLK_DDRCLK_A1_UF  9B6<> 9D5< 35D1>
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SYSCLK_DDRCLK_B1  9D4< 11A3<> 35C1>
SYSCLK_DDRCLK_B1_L  9D4< 11A3<> 35C1>
SYSCLK_DDRCLK_B1_L_UF  9B6<> 9D5< 35D1>
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SYSCLK_IA_TP      8A5<>
SYSTEM_CLK_EN     14A5< 14B6< 29C4<>
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THERM1_A_DP       25A7< 25A8< 37A2>
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THERM1_DP         25A5< 25A6< 25B5<> 25B6< 37A2>
THERM1_M_DM       25B7< 25B8< 37A2>
THERM1_M_DP       25B7< 25B8< 37A2>
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THERM2_DM         25A5< 25A6< 25B5<> 25B6< 37A2>
THERM2_DP         25A5< 25A6< 25B5<> 25B6< 37A2>
THERM2_M_DM       25B7< 25B8< 37A2>
THERM2_M_DP       25B7< 25B8< 37A2>
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THERM_L_OC        25B1<> 29B4<>
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TMDS_CLKP         19B1< 19C1< 19D2< 22C8<> 37C2>
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TMDS_CONN_CLKP    22C7<> 22C7<> 36C1> 39C6>
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TMDS_CONN_DN<2>   22D6<> 36B1>
TMDS_CONN_DP<0>   22D6<> 36C1>
TMDS_CONN_DP<1>   22D6<> 36B1>
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TMDS_DP<2>        19A1< 19B1< 19C2< 22D5<> 37B2>
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TPAD_F_TXD        23B5<> 39B3>
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TPAD_TXD          23B6< 29B2< 29C4<>
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TV_GND2           22A6<> 38B6> 39A6>
TV_Y              22A6<> 39A6>
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UIDE_DIOW_L       13C7<> 24A4< 37C5>
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UIDE_DMARQ        13C7<> 37C5>
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UIDE_RST_L        13C7<> 24A4< 37C5>
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USB_DCN           14B2<> 14D2<
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USB_DFP           14B2<> 14C2< 37B2>
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USB_OC_EF_L       14B2< 14C7<
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USB_PWREN_EF_L    14B2<> 14C7<
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VCORE_AB_SEL_OPT  33A6<>
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VCORE_BST         33C5<> 38C1>
VCORE_CC          33B6<> 38C1>
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VCORE_D1          33A3<>
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VCORE_DL          33B5<> 38C1>
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VCORE_GND         33B5<> 38B1>
VCORE_GNDA        33B6<> 38B1>
VCORE_GNDDIV      33A5< 33A5< 38B1>
VCORE_GNDDIV_TEST  33A4<>
VCORE_GNDSNS      33A1<> 33A5< 38B1>
VCORE_GNDSNS_TEST  33A4<>
VCORE_ILIM        33C6<> 38C1>
VCORE_LX          33B5<> 38C1>
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VCORE_MUX_SEL     33D5<>
VCORE_OFFSET_DIV  33B6<>
VCORE_REF         33B6<> 38C1>
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VCORE_SHDN_L_3V   5B3<>
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VCORE_TIME        33B4<> 38B1>
VCORE_TON         33B6< 38C1>
VCORE_VCC         33C6< 38C1>
VCORE_VGATE       14B5< 14B7< 33B4> 38B1>
VCORE_VID<0>      33B7<
VCORE_VID<1>      33B7< 33D3< 33D4>
VCORE_VID<2>      33B7< 33D3< 33D4>
VCORE_VID<3>      33B7< 33D3< 33D4>
VCORE_VID<4>      33B7< 33D3< 33D4>
VCORE_VSENSE      33C2<>
VGA_B             22C6<> 22C7< 39B6>
VGA_G             22C5<> 22C7< 39B6>
VGA_HSYNC         22C6<> 22D7< 39B6>
VGA_R             22B7< 22C5<> 39B6>
VGA_VSYNC         22C5<> 22D7< 39B6>
XT10_SPN          4C2<>
XT301_SPN         4C2<>
XT302_SPN         4C2<>
XV_LCDATA20_PU    20C7<>
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6570	B
SCALE: NONE	SHT 42 OF 44	

*** Part Cross-Reference for the entire design ***

C1 CAP 5
C2 CAP 5
C3 CAP 33
C4 CAP 33
C5 CAP 33
C6 CAP 33
C7 CAP 32
C8 CAP 32
C9 CAP 5
C10 CAP 5
C11 CAP 30
C12 CAP 33
C13 CAP 33
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U6	MAX1772	30
U7	MAX1717	33
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U15	PI3B3257	33
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U22	VREG_LP2951	31
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U39	741G32	22
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U43	TRANSCEIVER_88E1111	26
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U50	TRA_SI3447DV	34
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