1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

DRAWING REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
B		397429	PRODUCTION RELEASED	08/30/05?	

SCHEM,MLB,PB15

Fri Aug 26 15:48:02 2005

BOM OPTIONS (IN COMMON PARTS)

STUFF	NO STUFF
1_8V_MAXBUS	1_5V_MAXBUS
NO_SSCG	SSCG
5V_HD_LOGIC	3V_HD_LOGIC
NO_BBANG	BBANG
INT_2_5V_COLD	INT_2_5V_HOT
ATI_MEMIO_HI	ATI_MEMIO_LO
SOFT_MODEM	USB_MODEM
GPU_PWRMSR	EXT_TMDS
GPU_SS	
VGA_BUFFER_RES	
INT_TMDS	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6809	1	SCHEM,MLB,PB15	SCH1	
820-1600	1	PCBF,MLB,PB15	PCB1	
826-4393	1	LABEL,PCB,28MM X 6MM	EEE:SQE	LABEL_BTR
826-4393	1	LABEL,PCB,28MM x 6MM	EEE:SQF	LABEL_BST64
826-4393	1	LABEL,PCB,28MM x 6MM	EEE:SQG	LABEL_BST128

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES °
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER / DESIGN CK /
ENG APPD / MFG APPD /
QA APPD / DESIGNER /
RELEASE / SCALE NONE

MATERIAL/FINISH NOTED AS APPLICABLE

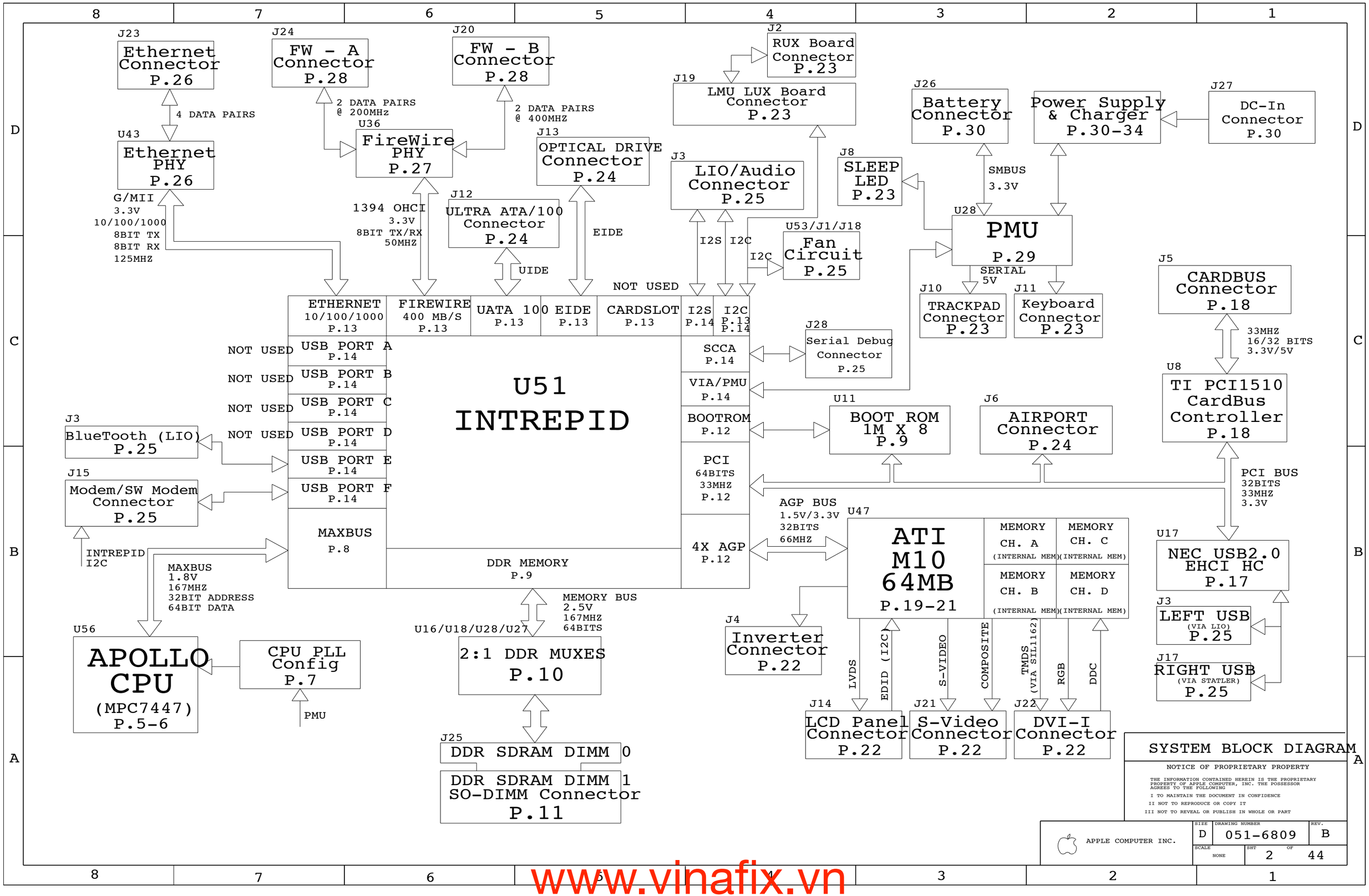
SIZE D

Apple Computer Inc.

TITLE
SCHEM,MLB,PB15

DRAWING NUMBER 051-6809 REV. B

SHT 1 OF 44



SYSTEM BLOCK DIAGRAM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6809	B

SCALE	SHT	OF
NONE	2	44

POWER SYSTEM ARCHITECTURE

AC ADAPTER IN PG 30

INRUSH LIMITER PG 30

+24V_PBUS

1V20_REF
>~13.44V TURNS-ON
<~13.44V SHUTS-OFF
PG 31

RUN/SS
BUCK REGULATOR (LTC1625) PG 31
VCC
AC: 12.8V
NO AC: BATTERY VOLTAGE 1625 NOT RUNNING
SHUTDOWN: RUNNING
SLEEP: RUNNING
RUN: RUNNING

+PBUS

14V_PBUS

+3V_PMU LDO PG 31

+BATT

+5V_MAIN

+3V_PMU

+4_6V_BU

RC AT 1M*0.047UF @ 24V
STARTS 2.0MSEC AFTER DCDC_EN_L BECOMES LOW

RUN/SS - 5V
TURNS ON AT >1V
<100UA ALLOWED
INTERNAL ZENER CLAMP TO 6V

MAIN 3V/5V DC/DC (LTC3707) PG 32
VCC
PGOOD
STBYMD
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING

INTERNAL ZENER CLAMP TO 6V
<100UA ALLOWED
TURNS ON AT >1V
RUN/SS - 3V

+5V_MAIN

3V_5V_OK

HOLDS BOTH RUN/SS AT GND WHEN IT'S CONNECTED TO GND

TURNS CONTROL TO RUN/SS WHEN IT'S OPEN

+3.3V_MAIN

RC AT 1M*0.1UF @ 24V
STARTS ~4.25MSEC AFTER DCDC_EN_L BECOMES LOW

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

+24V_PBUS

DC/DC (LTC3411)
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING
PG 34

+1.8V_MAIN

MAXBUS

BACKUP BATTERY

14V_PBUS

14V CHARGES BACKUP BATTERY

24V IS OUTPUT ONLY FROM BACKUP BATTERY

CHARGER INPUT & BOOST OUTPUT PG 31

BACKUP BATTERY CIRCUIT CHARGES OFF +PBUS
AND PREVENTS +PBUS AND +24V_PBUS FROM DROPPING BELOW 6V
(UNTIL DRAINED)

BATTERY CHARGER (MAX1772) PG 30

+BATT

3S 2P 18650 CELLS

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

BATTERY VOLTAGE FEED-IN PATH PG 30

+PBUS

BACKLIGHT INVERTER

+5V_MAIN

VCC
MAIN 2.5V/1.5V DC/DC (MAX1715) PG 34
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING

TURNS ON OUTPUT @ 2.4V
ON1/ON2

PGOOD

1_5V_2_5V_OK

MAP31 DDR CORE
MAP31 DDR I/O
DDR POWER
+2.5V_MAIN

+1.5V_MAIN
INTREPID CORE
AGP I/O

DCDC_EN_L

AFTER PMU IS UP AND RUNNING
DCDC_EN_L WILL PULL ON1/ON2
LOW IN SHUTDOWN

+PBUS

+5V_MAIN

EXT_VCC
VCC
DC/DC (LTC1778)
SHUTDOWN: STOPPED
SLEEP: D3COLD
RUN: RUNNING
RUN/SS PG 20

TURNS ON AS LOW AS 0.8V/TYP 1.5V
INTERNAL 1.2UA CURRENT SOURCE

GPU_VCORE +1.2V

DCDC_EN
SLEEP
D3_COLD

GPU_VCORE SEQUENCING

1M & 0.1UF @14V, IT TAKES ~5.88MS TO START SWITCHER

1_5V_2_5V_OK

D3_HOT

DCDC_EN_L
D3_HOT

1_5V_2_5V_OK WILL NOT PULL LOW UNTIL +5V_MAIN TURNS ON
HOWEVER, 5V SHOULD TURN ON ~2.23MS AFTER DCDC_EN_L OR PMU_POWERUP_L BECOMES '1'; MUCH LESS THAN THE RC CHARGING AT INT_VCC (5V)

+PBUS

DCDC_EN
SLEEP
MAXBUS SEQUENCING

+5V_MAIN

VCC
SHDN
DC/DC (MAX1717)
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING
PG 33

CPU_VCORE (+1.385V)

SHUT-DOWN RUN SLEEP RUN SHUT-DOWN

SLEEP
SLEEP_L_LS5
DCDC_EN
DCDC_EN_L
+5V_MAIN
+5V_SLEEP
+3V_MAIN
+3V_SLEEP
3V_5V_OK
+2_5V_MAIN
+2_5V_SLEEP
+1_5V_MAIN
+1_5V_SLEEP
1_5V_2_5V_OK (MAX1715 OUTPUT)
1_5V_2_5V_OK (AT LTC1778 RUN/SS)
GPU_VCORE (D3HOT)
GPU_VCORE (D3COLD)

~2.23MS
~7.36MS
2.4V - ??? MS
??? MS
??? MS
~8.2MS

POWER BLOCK DIAGRAM

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6809 | REV. B

SCALE NONE | SHT 3 OF 44

PCB SPECS

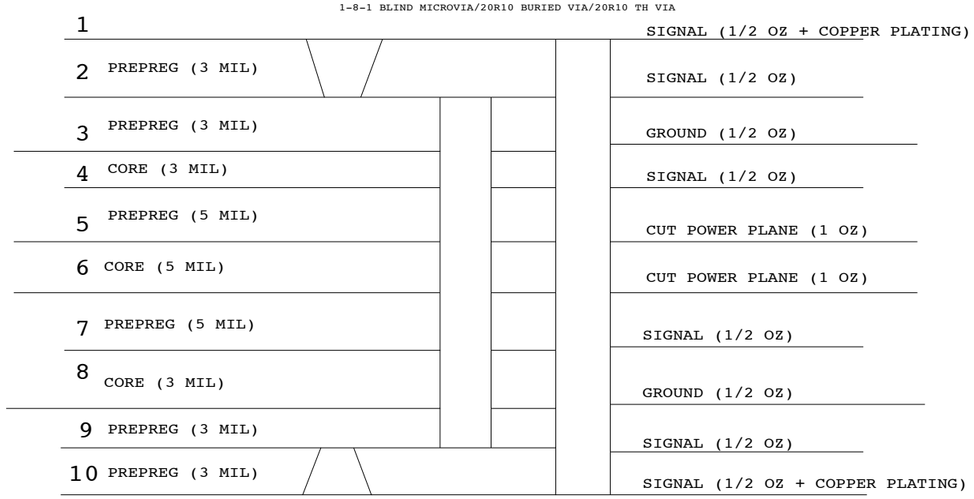
THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 10
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

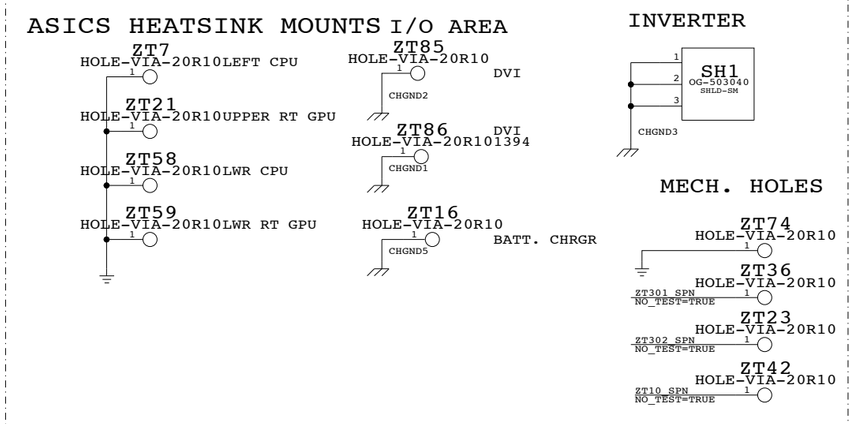
BOARD STACK-UP AND CONSTRUCTION

1-8-1 BLIND MICROVIA/20R10 BURIED VIA/20R10 TH VIA

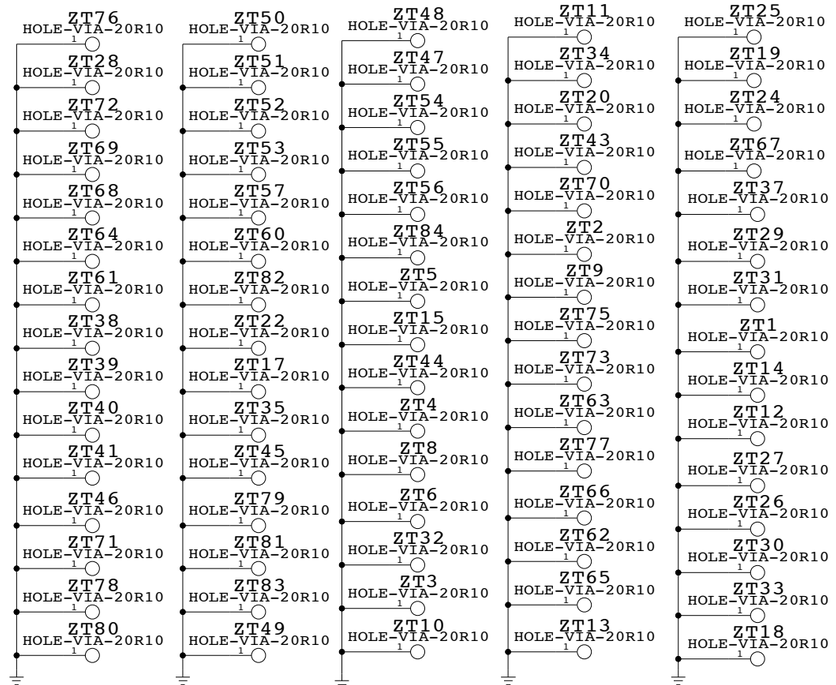


BOARD HOLES

CHASSIS MOUNTS



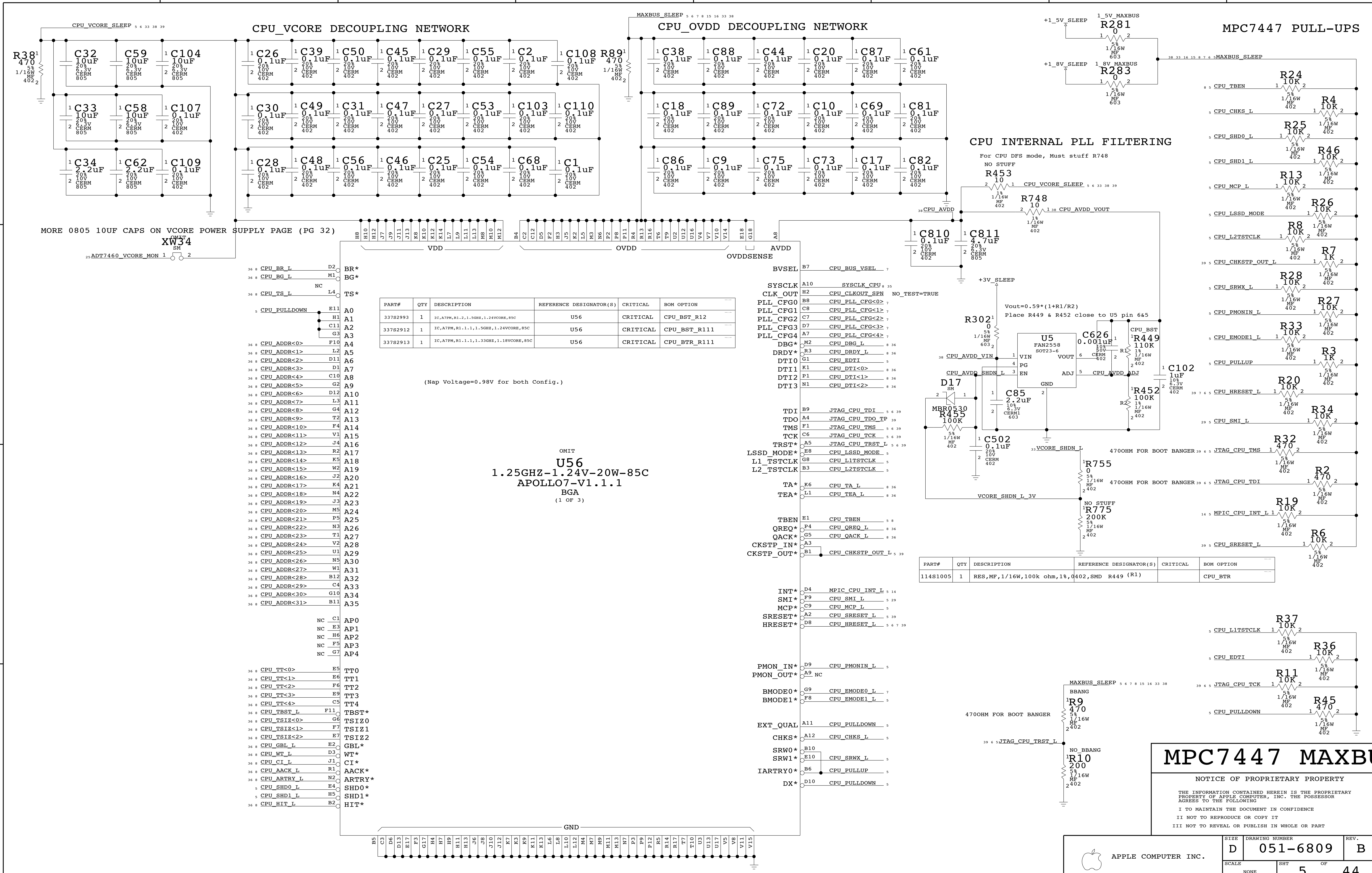
GROUND VIAS



BOARD INFORMATION

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6809	B
SCALE: NONE	SHT 4 OF 44	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S2993	1	IC,A7PM,R1.2,1.5GHZ,1.24VCORE,85C	U56	CRITICAL	CPU_BST_R12
337S2912	1	IC,A7PM,R1.1.1,1.5GHZ,1.24VCORE,85C	U56	CRITICAL	CPU_BST_R111
337S2913	1	IC,A7PM,R1.1.1,1.33GHZ,1.18VCORE,85C	U56	CRITICAL	CPU_BTR_R111

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S1005	1	RES,MF,1/16W,100k ohm,1%,0402,SMD	R449 (R1)		CPU_BTR

MPC7447 MAXBUS

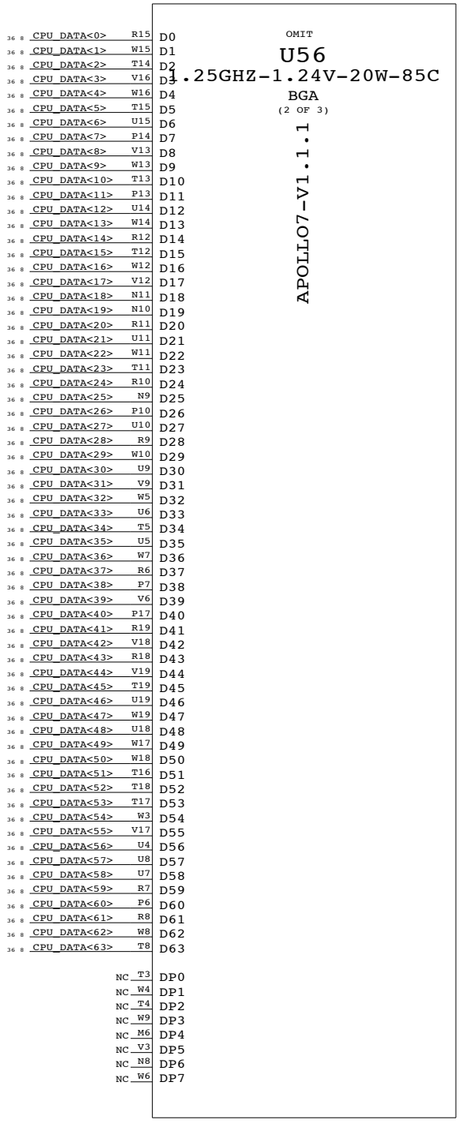
NOTICE OF PROPRIETARY PROPERTY

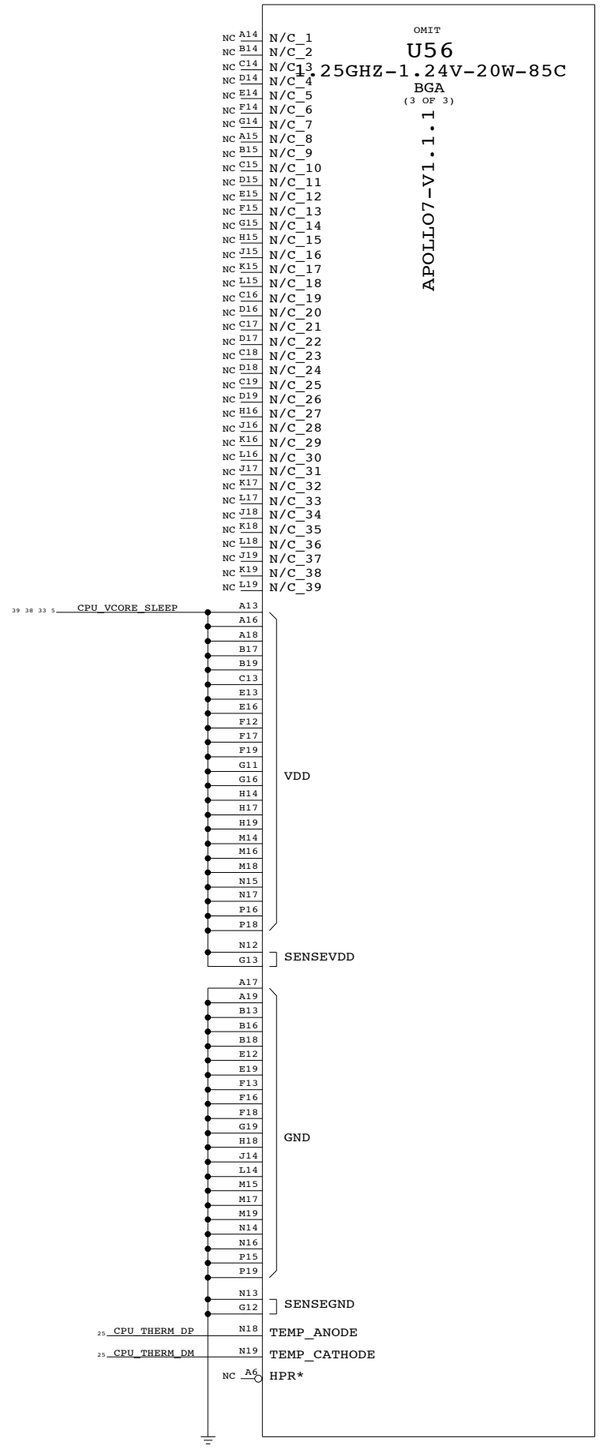
APPLE COMPUTER INC.

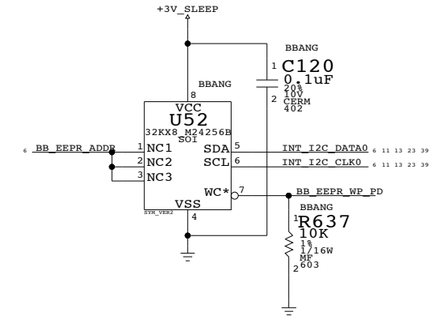
SIZE D | DRAWING NUMBER 051-6809 | REV. B

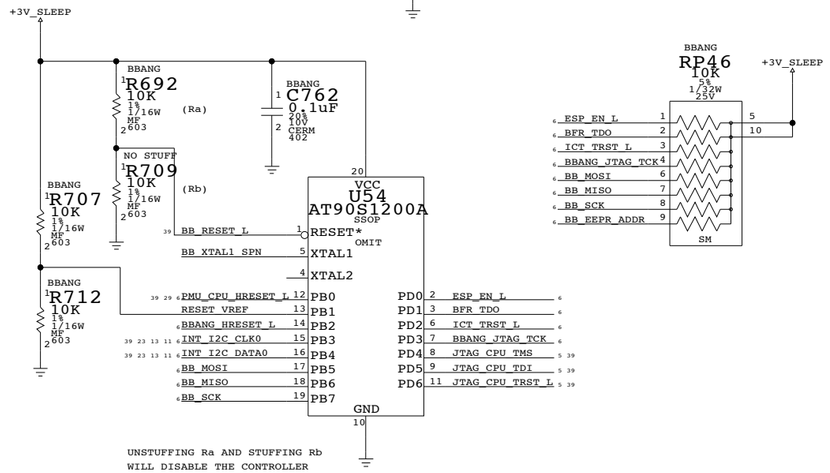
SCALE NONE | SHT 5 OF 44

BOOT BANGER - TWEAK PROCESSOR BITS AFTER POWER-ON

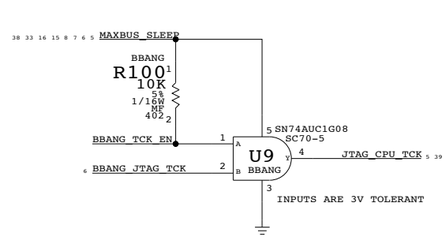


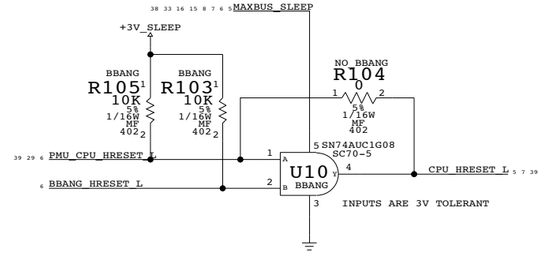






PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1135	1	000-6240-TW-GT4 BBANGER MCU,PROGRAMMED W/ BBANGER	U54	BBANG





MPC7447/BBANG

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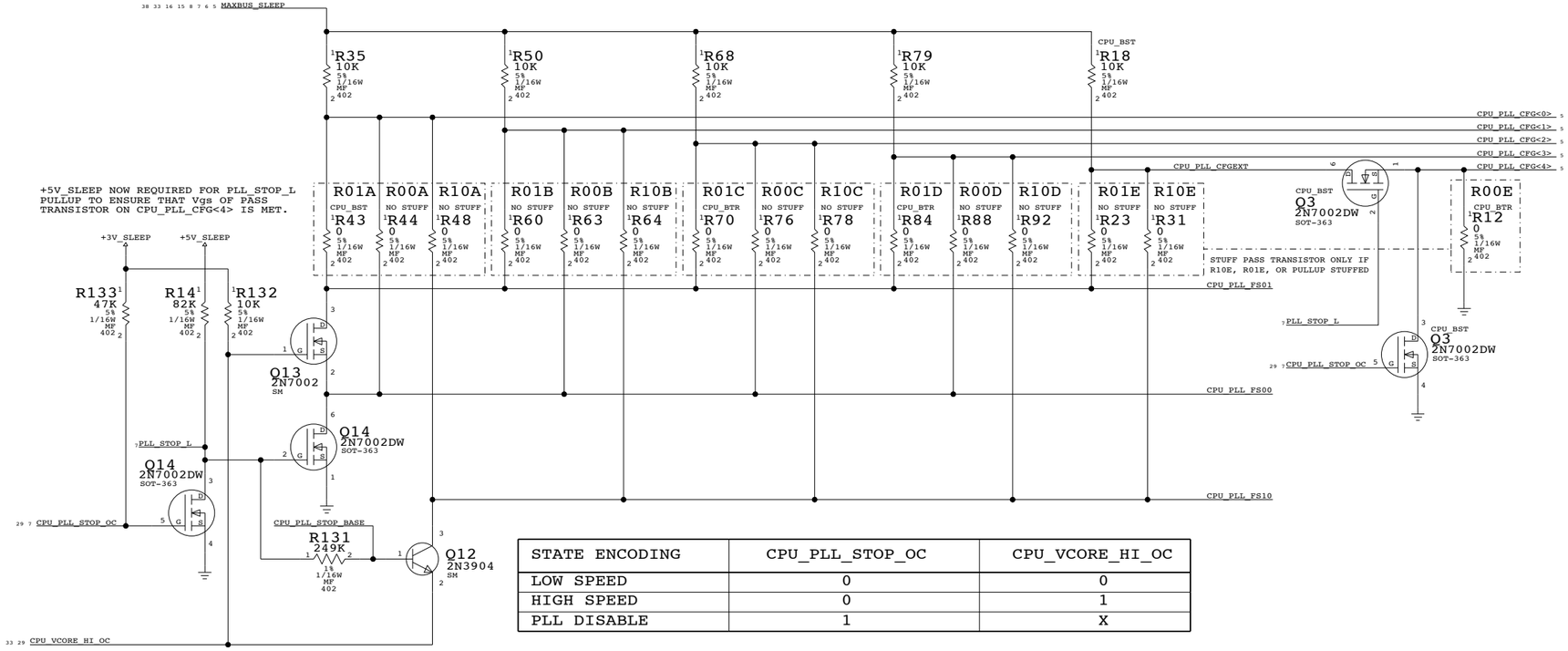
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6809	B

SCALE	SHT	OF
NONE	6	44

CPU PLL CONFIG CIRCUITRY



STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

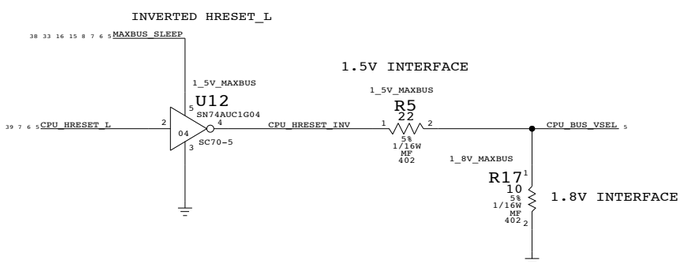
CPU FREQUENCY CONFIGURATION

APOLLO 7

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ (MHZ)	133MHZ (MHZ)	CPU_PLL_CFG 4 E	0123 ABCD	HEX
0.0X	PLL OFF		0	1111	0F
1.0X	PLL BYPASS		0	0011	03
2.0X	333	267	0	0100	04
3.0X	500	400	0	1000	08
4.0X	667	533	0	1010	0A
5.0X	833	667	0	1011	0B
5.5X	917	733	0	1001	09
6.0X	1000	800	0	1101	0D
6.5X	1083	867	0	0101	05
7.0X	1167	933	0	0010	02
7.5X	1250	1000	0	0001	01
8.0X	1333	1067	0	1100	0C
8.5X	1417	1133	0	0110	06
9.0X	1500	1200	1	0111	17
9.5X	1583	1267	0	0111	07
10.0X	1667	1333	1	1010	1A
10.5X	1750	1400	1	1000	18
11.0X	1833	1467	1	1001	19
11.5X	1917	1533	0	0000	00
12.0X	2000	1600	1	1011	1B
12.5X	2083	1667	1	1111	1F
13.0X	2167	1733	1	0101	15
13.5X	2250	1800	0	1110	0E
14.0X	2333	1867	1	1100	1C
15.0X	2500	2000	1	0001	11
16.0X	2667	2133	1	1101	1D
17.0X	2833	2267	1	0000	10
18.0X	3000	2400	1	0010	12
20.0X	3333	2667	1	0011	13
21.0X	3500	2800	1	0100	14
24.0X	4000	3200	1	0110	16
28.0X	4667	3733	1	1110	1E

CPU CONFIGURATION

MAXBUS VSEL



DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L NEED TO CHARACTERIZE

BUSTYPE SELECT

APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

CPU CONFIGURATION

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SIZE	DRAWING NUMBER	REV.
D	051-6809	B
SCALE: NONE	SHT 7 OF 44	

INTREPID BOOT STRAPS

BIT 32 TO 39

MAXBUS_SLEEP

NO STUFF R640	NO STUFF R639	NO STUFF R638	R666				
CPU_DATA<32>	CPU_DATA<33>	CPU_DATA<34>	CPU_DATA<35>	CPU_DATA<36>	CPU_DATA<37>	CPU_DATA<38>	CPU_DATA<39>
R622	R619	R618	NO STUFF R653	R621	R620	R652	R650
DDR TDMOdeEnable_h 1: DDI TDI input (JTAG)			DDR TPDN_Pol 1: Active low	ExtPLLSPwn_Pol 1: Active high			
		Relaxmarclk_En_h 1: Active			Spare	Spare	Spare

BIT 40 TO 47

MAXBUS_SLEEP

NO STUFF R641	SSCG R665	NO STUFF R664	NO_SSCG R693	NO STUFF R694	NO STUFF R699		
CPU_DATA<40>	CPU_DATA<41>	CPU_DATA<42>	CPU_DATA<43>	CPU_DATA<44>	CPU_DATA<45>	CPU_DATA<46>	CPU_DATA<47>
R648	R677	R623	NO_SSCG R651	R649	SSCG R678	R679	R684
Spare	Spare		BIT2	BIT1	BIT0	Internal_SPREADEN 1: Enable	PCI1_Clk_Src 0: PLL2 (no spread) 1: PLL4

PCI0_Clk_Source 0: Clock (no spread) 1: Clock (spread)

PLL4MODESEL_NXT[2:0]
000: 166.4MHz (2.5X)
001: 149.76MHz
010: 133.12MHZ (2.0X)
011: 99.84MHz (1.5X)
100: 83.20MHZ

MODE A (2.5X) IS FOR STATIC OPERATION
MODE C (2.0X) IS FOR CLOCK SLEW OPERATION

BIT 48 TO 55

MAXBUS_SLEEP

SSCG R696	SSCG R695	NO STUFF R667	NO STUFF R668	NO STUFF R643	NO STUFF R642	R698	
CPU_DATA<48>	CPU_DATA<49>	CPU_DATA<50>	CPU_DATA<51>	CPU_DATA<52>	CPU_DATA<53>	CPU_DATA<54>	CPU_DATA<55>
NO_SSCG R681	NO_SSCG R680	NO STUFF R654	R655	R625	R624	NO STUFF R683	R626
BUF_REF_CLK_OUTEnable_h 1: Active		SelPLL4ExtSrc 1: External source					Spare
			OBSOLETE (Should remain high) En_PCI_ROM_P 1: Boot ROM on PCI	TI 1394b workaround 1: TI PHY 1394b workaround		BIT2 BIT1 BIT0	

MaxBus output impedance
111: 28.6 ohm
011: 33.3 ohm
101: 40 ohm
001: 50 ohm
110: 66.6 ohm
010: 100 ohm
100: 200 ohm
000: 200 ohm

R159

+1_5V_INTREPID_PLL — 4.7 5% 1/16W MF 402 — +1_5V_INTREPID_PLL7

C187 0.22uF 20% 6.3V CERM 402

H26 VDD15A_7 (PLL6)

OMIT

U51 INTREPID-REV2.1 BGA

(1 OF 9) CRITCAL

CPU_BR_L	E29	BR INPUT
CPU_BG_L	E26	BG NO BUS KEEPER
CPU_TS_L	B27	TS NO BUS KEEPER
CPU_ADDR<0>	D24	A_0
CPU_ADDR<1>	D25	A_1
CPU_ADDR<2>	A27	A_2
CPU_ADDR<3>	E24	A_3
CPU_ADDR<4>	G23	A_4
CPU_ADDR<5>	B26	A_5
CPU_ADDR<6>	A26	A_6
CPU_ADDR<7>	D23	A_7
CPU_ADDR<8>	A25	A_8
CPU_ADDR<9>	E23	A_9
CPU_ADDR<10>	J22	A_10
CPU_ADDR<11>	B25	A_11
CPU_ADDR<12>	H22	A_12
CPU_ADDR<13>	G22	A_13
CPU_ADDR<14>	D22	A_14
CPU_ADDR<15>	B24	A_15
CPU_ADDR<16>	B23	A_16
CPU_ADDR<17>	E22	A_17
CPU_ADDR<18>	J21	A_18
CPU_ADDR<19>	G21	A_19
CPU_ADDR<20>	E21	A_20
CPU_ADDR<21>	A24	A_21
CPU_ADDR<22>	D21	A_22
CPU_ADDR<23>	A23	A_23
CPU_ADDR<24>	H20	A_24
CPU_ADDR<25>	B22	A_25
CPU_ADDR<26>	H21	A_26
CPU_ADDR<27>	A22	A_27
CPU_ADDR<28>	E20	A_28
CPU_ADDR<29>	B21	A_29
CPU_ADDR<30>	D20	A_30
CPU_ADDR<31>	A21	A_31
CPU_CI_L	G26	CI
CPU_GBL_L	A29	GBL
CPU_TBST_L	A28	TBST
CPU_TSIZ<0>	G24	TSIZ_0
CPU_TSIZ<1>	H24	TSIZ_1
CPU_TSIZ<2>	D26	TSIZ_2
CPU_TT<0>	E25	TT_0
CPU_TT<1>	G25	TT_1
CPU_TT<2>	B28	TT_2
CPU_TT<3>	D27	TT_3
CPU_TT<4>	J25	TT_4
CPU_WT_L	D28	WT
CPU_AACK_L	B29	AACK NO BUS KEEPER - PU
CPU_ARTRY_L	H23	ARTRY NO BUS KEEPER - PU
CPU_HIT_L	B31	HIT INPUT - PU
CPU_QREQ_L	A32	QREQ INPUT - PD
CPU_QACK_L	G27	QACK NO BUS KEEPER - ?
INT_SUSPEND_REQ_L	AK9	SUSPENDREQ
INT_SUSPEND_ACK_L	AM8	SUSPENDACK

Vin = Intrepid Vcore (1.5V)
Vout = MaxBus rail (1.8V)

FB BUFFER HAS 50 OHM OUTPUT IMPEDANCE

INT_CPUFB_IN	J24	CPU_FB_IN
INT_CPUFB_OUT	H16	CPU_FB_OUT
	G8	ANALYZER_CLK
CPU_CLK_EN	AH9	STOPCPUCLK
INTREPID_ACS_REF	H13	ACS_REF
SYSCLK_CPU_UF	J15	CPU_CLK
CPU_TBEN	A31	TBEN NO BUS KEEPER - PU

R169 511 1% 1/16W MF 402 — SYSCLK_LA_TP

R168 0 5% 1/16W MF 402 — SYSCLK_CPU

R161 1K 1% 1/16W MF 402

INTREPID OUTPUTS HIGH BY DEFAULT

VSSA_7 (PLL6) H25

MAXBUS INTERFACE

D_0	D10	CPU_DATA<0>
D_1	G12	CPU_DATA<1>
D_2	E11	CPU_DATA<2>
D_3	H11	CPU_DATA<3>
D_4	B9	CPU_DATA<4>
D_5	B8	CPU_DATA<5>
D_6	A9	CPU_DATA<6>
D_7	A8	CPU_DATA<7>
D_8	E12	CPU_DATA<8>
D_9	D11	CPU_DATA<9>
D_10	B10	CPU_DATA<10>
D_11	J13	CPU_DATA<11>
D_12	A10	CPU_DATA<12>
D_13	D12	CPU_DATA<13>
D_14	E13	CPU_DATA<14>
D_15	G13	CPU_DATA<15>
D_16	B11	CPU_DATA<16>
D_17	D13	CPU_DATA<17>
D_18	A11	CPU_DATA<18>
D_19	G14	CPU_DATA<19>
D_20	H14	CPU_DATA<20>
D_21	E14	CPU_DATA<21>
D_22	B12	CPU_DATA<22>
D_23	G15	CPU_DATA<23>
D_24	B13	CPU_DATA<24>
D_25	H15	CPU_DATA<25>
D_26	D14	CPU_DATA<26>
D_27	B14	CPU_DATA<27>
D_28	A12	CPU_DATA<28>
D_29	G16	CPU_DATA<29>
D_30	E15	CPU_DATA<30>
D_31	J16	CPU_DATA<31>
D_32	D15	CPU_DATA<32>
D_33	A14	CPU_DATA<33>
D_34	A13	CPU_DATA<34>
D_35	D16	CPU_DATA<35>
D_36	E16	CPU_DATA<36>
D_37	G17	CPU_DATA<37>
D_38	B15	CPU_DATA<38>
D_39	H17	CPU_DATA<39>
D_40	A15	CPU_DATA<40>
D_41	B16	CPU_DATA<41>
D_42	E17	CPU_DATA<42>
D_43	A16	CPU_DATA<43>
D_44	J18	CPU_DATA<44>
D_45	H18	CPU_DATA<45>
D_46	D17	CPU_DATA<46>
D_47	G18	CPU_DATA<47>
D_48	A17	CPU_DATA<48>
D_49	B17	CPU_DATA<49>
D_50	E18	CPU_DATA<50>
D_51	B18	CPU_DATA<51>
D_52	D18	CPU_DATA<52>
D_53	A18	CPU_DATA<53>
D_54	A19	CPU_DATA<54>
D_55	H19	CPU_DATA<55>
D_56	B19	CPU_DATA<56>
D_57	J19	CPU_DATA<57>
D_58	A20	CPU_DATA<58>
D_59	D19	CPU_DATA<59>
D_60	E19	CPU_DATA<60>
D_61	G19	CPU_DATA<61>
D_62	B20	CPU_DATA<62>
D_63	G20	CPU_DATA<63>
DBG	A30	CPU_DBG_L
DRDY	G28	CPU_DRDY_L
DTI_0	K25	CPU_DTI<0>
DTI_1	D29	CPU_DTI<1>
DTI_2	B30	CPU_DTI<2>
TA	E27	CPU_TA_L
TEA	E28	CPU_TEA_L

NO BUS KEEPER - ? DTI_0
NO BUS KEEPER - ? DTI_1
NO BUS KEEPER - ? DTI_2
NO BUS KEEPER - PU TA
NO BUS KEEPER - PU TEA

SHORT = 1" SHORTER THAN MATCHED LENGTH
LONG = 1" LONGER THAN MATCHED LENGTH

INT_CPUFB_OUT2	INT_CPUFB_OUT_SHORT	INT_CPUFB_OUT_NORM		INT_CPUFB_LONG
R155 0 5% 1/16W MF 402	R140 0 5% 1/16W MF 402	R128 0 5% 1/16W MF 402		
	NO STUFF R146 0 5% 1/16W MF 402	R141 0 5% 1/16W MF 402	NO STUFF R136 0 5% 1/16W MF 402	
INT_CPUFB_IN	R147 0 5% 1/16W MF 402		INT_CPUFB_IN_NORM	

MAXBUS PULL-UPS

MAXBUS_SLEEP

RP3 10K	RP3 10K	RP3 10K	RP2 10K	R152 10K	RP2 10K	RP2 10K	RP2 10K
CPU_TS_L	CPU_TA_L	CPU_ARTRY_L	CPU_BR_L	CPU_HIT_L	CPU_DRDY_L	CPU_TEA_L	CPU_AACK_L
R150 10K	RP3 10K	R151 10K					
CPU_DBG_L	CPU_BG_L	CPU_QREQ_L					

5% 1/16W MF 402 SM1

INTREPID BOOT STRAPS

BIT 56 TO 63

MAXBUS_SLEEP

NO STUFF R669	NO STUFF R645	NO STUFF R697	NO STUFF R670	R644	NO STUFF R646		
CPU_DATA<56>	CPU_DATA<57>	CPU_DATA<58>	CPU_DATA<59>	CPU_DATA<60>	CPU_DATA<61>	CPU_DATA<62>	CPU_DATA<63>
R656	R685	R657	R628	R682	R658	NO STUFF R627	R629
Spare	Spare	OBSOLETE (Should remain high) 0: 0-15V / Reg PCI 1: 0-15V / 2-3 PCI1	PCI1_REQ0_L / GPIO8	PCI1_REQ1_L / GPIO9	PCI1_GNT0_L / GPIO5	FireWire PHY interface 0: Legacy interface 1: B-Mode interface	PCI0_Clk_Source 0: Bus (G3) 1: 66x Bus (G3)

Intrepid MaxBus

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6809	B
SCALE: NONE	SHT 8 OF 44	

SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

PINS ARE SWAPABLE FOR RPAKS

1MB BOOT ROM

U51 INTREPID-REV2.1 (OMIT) — BGA (2 OF 9) CRITICAL

DDR_DATA_0	AK32	MEM_DATA<0>	35 10
DDR_DATA_1	AK33	MEM_DATA<1>	35 10
DDR_DATA_2	AK31	MEM_DATA<2>	35 10
DDR_DATA_3	AK35	MEM_DATA<3>	35 10
DDR_DATA_4	AK36	MEM_DATA<4>	35 10
DDR_DATA_5	AJ32	MEM_DATA<5>	35 10
DDR_DATA_6	AJ35	MEM_DATA<6>	35 10
DDR_DATA_7	AJ36	MEM_DATA<7>	35 10
DDR_DATA_8	AG33	MEM_DATA<8>	35 10
DDR_DATA_9	AG35	MEM_DATA<9>	35 10
DDR_DATA_10	AH35	MEM_DATA<10>	35 10
DDR_DATA_11	AG36	MEM_DATA<11>	35 10
DDR_DATA_12	AH36	MEM_DATA<12>	35 10
DDR_DATA_13	AH32	MEM_DATA<13>	35 10
DDR_DATA_14	AG32	MEM_DATA<14>	35 10
DDR_DATA_15	AG31	MEM_DATA<15>	35 10
DDR_DATA_16	AE32	MEM_DATA<16>	35 10
DDR_DATA_17	AF35	MEM_DATA<17>	35 10
DDR_DATA_18	AF36	MEM_DATA<18>	35 10
DDR_DATA_19	AE36	MEM_DATA<19>	35 10
DDR_DATA_20	AE35	MEM_DATA<20>	35 10
DDR_DATA_21	AE33	MEM_DATA<21>	35 10
DDR_DATA_22	AD36	MEM_DATA<22>	35 10
DDR_DATA_23	AD35	MEM_DATA<23>	35 10
DDR_DATA_24	AA36	MEM_DATA<24>	35 10
DDR_DATA_25	AA35	MEM_DATA<25>	35 10
DDR_DATA_26	AA33	MEM_DATA<26>	35 10
DDR_DATA_27	AB36	MEM_DATA<27>	35 10
DDR_DATA_28	AB35	MEM_DATA<28>	35 10
DDR_DATA_29	AC36	MEM_DATA<29>	35 10
DDR_DATA_30	AA32	MEM_DATA<30>	35 10
DDR_DATA_31	AB33	MEM_DATA<31>	35 10
DDR_DATA_32	V36	MEM_DATA<32>	35 10
DDR_DATA_33	U33	MEM_DATA<33>	35 10
DDR_DATA_34	U32	MEM_DATA<34>	35 10
DDR_DATA_35	V35	MEM_DATA<35>	35 10
DDR_DATA_36	T36	MEM_DATA<36>	35 10
DDR_DATA_37	U36	MEM_DATA<37>	35 10
DDR_DATA_38	U35	MEM_DATA<38>	35 10
DDR_DATA_39	T36	MEM_DATA<39>	35 10
DDR_DATA_40	P33	MEM_DATA<40>	35 10
DDR_DATA_41	R30	MEM_DATA<41>	35 10
DDR_DATA_42	P35	MEM_DATA<42>	35 10
DDR_DATA_43	P36	MEM_DATA<43>	35 10
DDR_DATA_44	R36	MEM_DATA<44>	35 10
DDR_DATA_45	R35	MEM_DATA<45>	35 10
DDR_DATA_46	R33	MEM_DATA<46>	35 10
DDR_DATA_47	R32	MEM_DATA<47>	35 10
DDR_DATA_48	N35	MEM_DATA<48>	35 10
DDR_DATA_49	M36	MEM_DATA<49>	35 10
DDR_DATA_50	L35	MEM_DATA<50>	35 10
DDR_DATA_51	M35	MEM_DATA<51>	35 10
DDR_DATA_52	M33	MEM_DATA<52>	35 10
DDR_DATA_53	L36	MEM_DATA<53>	35 10
DDR_DATA_54	N33	MEM_DATA<54>	35 10
DDR_DATA_55	M30	MEM_DATA<55>	35 10
DDR_DATA_56	J32	MEM_DATA<56>	35 10
DDR_DATA_57	J33	MEM_DATA<57>	35 10
DDR_DATA_58	J35	MEM_DATA<58>	35 10
DDR_DATA_59	K32	MEM_DATA<59>	35 10
DDR_DATA_60	K33	MEM_DATA<60>	35 10
DDR_DATA_61	J36	MEM_DATA<61>	35 10
DDR_DATA_62	K36	MEM_DATA<62>	35 10
DDR_DATA_63	K35	MEM_DATA<63>	35 10

DDR MEMORY INTERFACE

DDR_A_0	H35	MEM_ADDR<0>	9 35
DDR_A_1	G35	MEM_ADDR<1>	9 35
DDR_A_2	G36	MEM_ADDR<2>	9 35
DDR_A_3	F36	MEM_ADDR<3>	9 35
DDR_A_4	F35	MEM_ADDR<4>	9 35
DDR_A_5	E35	MEM_ADDR<5>	9 35
DDR_A_6	E36	MEM_ADDR<6>	9 35
DDR_A_7	G32	MEM_ADDR<7>	9 35
DDR_A_8	D36	MEM_ADDR<8>	9 35
DDR_A_9	H36	MEM_ADDR<9>	9 35
DDR_A_10	G33	MEM_ADDR<10>	9 35
DDR_A_11	H33	MEM_ADDR<11>	9 35
DDR_A_12	D35	MEM_ADDR<12>	9 35
DDR_BA_0	L30	MEM_BA<0>	9 35
DDR_BA_1	M29	MEM_BA<1>	9 35
DDRCS_0	AN34	MEM_CS_L<0>	9 35
DDRCS_1	AN36	MEM_CS_L<1>	9 35
DDRCS_2	AL35	MEM_CS_L<2>	9 35
DDRCS_3	AL33	MEM_CS_L<3>	9 35
DDR_DQS_0	AJ31	MEM_DQS<0>	10 35
DDR_DQS_1	AH31	MEM_DQS<1>	10 35
DDR_DQS_2	AD32	MEM_DQS<2>	10 35
DDR_DQS_3	AB30	MEM_DQS<3>	10 35
DDR_DQS_4	V30	MEM_DQS<4>	10 35
DDR_DQS_5	P32	MEM_DQS<5>	10 35
DDR_DQS_6	N29	MEM_DQS<6>	10 35
DDR_DQS_7	L32	MEM_DQS<7>	10 35
DDR_DM_0	AJ33	MEM_DQM<0>	10 35
DDR_DM_1	AH33	MEM_DQM<1>	10 35
DDR_DM_2	AD33	MEM_DQM<2>	10 35
DDR_DM_3	AC35	MEM_DQM<3>	10 35
DDR_DM_4	T35	MEM_DQM<4>	10 35
DDR_DM_5	T33	MEM_DQM<5>	10 35
DDR_DM_6	N32	MEM_DQM<6>	10 35
DDR_DM_7	L33	MEM_DQM<7>	10 35
DDRRAS	L29	MEM_RAS_L	9 35
DDRCAS	H32	MEM_CAS_L	9 35
DDRWE	K30	MEM_WE_L	9 35
DDRCKE0	AN35	MEM_CKE<0>	9 35
DDRCKE1	AM35	MEM_CKE<1>	9 35
DDRCKE2	AM36	MEM_CKE<2>	9 35
DDRCKE3	AL36	MEM_CKE<3>	9 35
DDR_SELHI_0	AB32	MEM_MUXSEL_MSB_L_TP	
DDR_SELHI_1	AE29	MEM_MUXSEL_MSB	10 35
DDR_SELLO_0	N30	MEM_MUXSEL_LSB_L_TP	
DDR_SELLO_1	T32	MEM_MUXSEL_LSB	10 35
DDR_MCLK_0_P	Y32	SYSCLK_DDRCLK_A0_UF	9 35
DDR_MCLK_0_N	Y33	SYSCLK_DDRCLK_A0_L_UF	9 35
DDR_MCLK_1_P	Y35	SYSCLK_DDRCLK_A1_UF	9 35
DDR_MCLK_1_N	Y36	SYSCLK_DDRCLK_A1_L_UF	9 35
DDR_MCLK_2_P	Y30	INT_DDRCLK2_P_TP	
DDR_MCLK_2_N	W30	INT_DDRCLK2_N_TP	
DDR_MCLK_3_P	W32	SYSCLK_DDRCLK_B0_UF	9 35
DDR_MCLK_3_N	W33	SYSCLK_DDRCLK_B0_L_UF	9 35
DDR_MCLK_4_P	V33	SYSCLK_DDRCLK_B1_UF	9 35
DDR_MCLK_4_N	V32	SYSCLK_DDRCLK_B1_L_UF	9 35
DDR_MCLK_5_P	W35	INT_DDRCLK5_P_TP	
DDR_MCLK_5_N	W36	INT_DDRCLK5_N_TP	
DDR_REF	AA22	INT_MEM_REF_H	38
DDR_VREF_0	Y22	INT_MEM_VREF	9 38
DDR_VREF_1	T22		

‘0’ & ‘1’ GO TO SLOT A
‘2’ & ‘3’ GO TO SLOT B

‘0’S ARE SAME POLARITY (ACTIVE-LO)
‘1’S ARE SAME POLARITY (ACTIVE-HI)

MEM_VREF

+2_5V_INTREPID — R208 10K 1% 1/16W MF 402 — INT_MEM_VREF — R202 10K 1% 1/16W MF 402 — C249 0.1uF 10% 10V CERM 402

CLOCKS

SYSCLK_DDRCLK_A1_UF	RP20 4	5	SYSCLK_DDRCLK_A1
SYSCLK_DDRCLK_A1_L_UF	RP20 3	6	SYSCLK_DDRCLK_A1_L
SYSCLK_DDRCLK_A0_UF	RP22 1	8	SYSCLK_DDRCLK_A0
SYSCLK_DDRCLK_A0_L_UF	RP22 2	7	SYSCLK_DDRCLK_A0_L
SYSCLK_DDRCLK_B1_UF	RP20 2	7	SYSCLK_DDRCLK_B1
SYSCLK_DDRCLK_B1_L_UF	RP20 1	8	SYSCLK_DDRCLK_B1_L
SYSCLK_DDRCLK_B0_UF	RP22 3	6	SYSCLK_DDRCLK_B0
SYSCLK_DDRCLK_B0_L_UF	RP22 4	5	SYSCLK_DDRCLK_B0_L

CS

MEM_CS_L<0>	RP31 3	6	RAM_CS_L<0>
MEM_CS_L<1>	RP31 2	7	RAM_CS_L<1>
MEM_CS_L<2>	RP29 3	6	RAM_CS_L<2>
MEM_CS_L<3>	RP29 4	5	RAM_CS_L<3>

CKE

MEM_CKE<0>	RP31 1	8	RAM_CKE<0>
MEM_CKE<1>	RP31 4	5	RAM_CKE<1>
MEM_CKE<2>	RP29 1	8	RAM_CKE<2>
MEM_CKE<3>	RP29 2	7	RAM_CKE<3>

ADDR

MEM_ADDR<0>	RP14 3	6	RAM_ADDR<0>
MEM_ADDR<1>	RP12 2	7	RAM_ADDR<1>
MEM_ADDR<2>	RP12 1	8	RAM_ADDR<2>
MEM_ADDR<3>	RP12 4	5	RAM_ADDR<3>
MEM_ADDR<4>	RP12 3	6	RAM_ADDR<4>
MEM_ADDR<5>	RP9 2	7	RAM_ADDR<5>
MEM_ADDR<6>	RP9 1	8	RAM_ADDR<6>
MEM_ADDR<7>	RP14 2	7	RAM_ADDR<7>
MEM_ADDR<8>	RP9 4	5	RAM_ADDR<8>
MEM_ADDR<9>	RP14 4	5	RAM_ADDR<9>
MEM_ADDR<10>	RP14 1	8	RAM_ADDR<10>
MEM_ADDR<11>	RP17 4	5	RAM_ADDR<11>
MEM_ADDR<12>	RP9 3	6	RAM_ADDR<12>

BA

MEM_BA<0>	RP17 2	7	RAM_BA<0>
MEM_BA<1>	RP17 1	8	RAM_BA<1>

CNTL

MEM_WE_L	RP17 3	6	RAM_WE_L
MEM_CAS_L	R162 1	2	RAM_CAS_L
MEM_RAS_L	R176 1	2	RAM_RAS_L

+3V_MAIN — C125 2.2uF 10% 10V CERM 805 — C773 0.1uF 10% 10V CERM 402 — C122 0.1uF 10% 10V CERM 402

U11 1MX8-3.3V TSOP — VPP OMIT VCC (11, 30, 31)

A0	21	DQ0	25
A1	20	DQ1	26
A2	19	DQ2	27
A3	18	DQ3	28
A4	17	DQ4	32
A5	16	DQ5	33
A6	15	DQ6	34
A7	14	DQ7	35
A8	8		
A9	7		
A10	36		
A11	6		
A12	5		
A13	4		
A14	3		
A15	2		
A16	1		
A17	40		
A18	13		
A19	37		
A20	38		
CE	22		
OE	24		
WE	9		
WP	12		
PWD	10		
GND	23, 39		

PCI_AD<0>	39 37 24 18 17 12	PCI_AD<24>	12 17 18 24 37 39
PCI_AD<1>	39 37 24 18 17 12	PCI_AD<25>	12 17 18 24 37 39
PCI_AD<2>	39 37 24 18 17 12	PCI_AD<26>	12 17 18 24 37 39
PCI_AD<3>	39 37 24 18 17 12	PCI_AD<27>	12 17 18 24 37 39
PCI_AD<4>	39 37 24 18 17 12	PCI_AD<28>	12 17 18 24 37 39
PCI_AD<5>	39 37 24 18 17 12	PCI_AD<29>	12 17 18 24 37 39
PCI_AD<6>	39 37 24 18 17 12	PCI_AD<30>	12 17 18 24 37 39
PCI_AD<7>	39 37 24 18 17 12	PCI_AD<31>	12 17 18 24 37 39
PCI_AD<8>	39 37 24 18 17 12		
PCI_AD<9>	39 37 24 18 17 12		
PCI_AD<10>	39 37 24 18 17 12		
PCI_AD<11>	39 37 24 18 17 12		
PCI_AD<12>	39 37 24 18 17 12		
PCI_AD<13>	39 37 24 18 17 12		
PCI_AD<14>	39 37 24 18 17 12		
PCI_AD<15>	39 37 24 18 17 12		
PCI_AD<16>	39 37 24 18 17 12		
PCI_AD<17>	39 37 24 18 17 12		
PCI_AD<18>	39 37 24 18 17 12		
PCI_AD<19>	39 37 24 18 17 12		
PCI_AD<20>	39 37 24 18 17 12		

ROM_CS_TP_L (24) — NO STUFF R236 0 5% 1/16W MF 402 — ROM_CS_L (39 12)

+3V_MAIN — R691 10K 5% 1/16W MF 402 — R112 10K 5% 1/16W MF 402 — R674 1K 5% 1/16W MF 402 — R1 0 NO STUFF 5% 1/16W MF 402 — ROM_ONBOARD_CS_TP_L (24) — R271 0 NO STUFF 5% 1/16W MF 402 — ROM_OE_TP_L (24) — R194 0 NO STUFF 5% 1/16W MF 402 — ROM_RW_TP_L (24)

ROM_ONBOARD_CS_L (39 12)
ROM_OE_L (39 12)
ROM_RW_L (39 12)
ROM_WP_L
INT_RESET_L (29 13)

OVERRIDE ROM MODULE INTERCEPTS ROM CHIP SELECT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1542	1	IC,BootRom Q16A	U11	CRITICAL	?

Weak pulldowns ensure CKEs stay low after 2.5V I/O to Intrepid shuts off.

RAM_CKE<0> (35 11 9)
RAM_CKE<1> (35 11 9)
RAM_CKE<2> (35 11 9)
RAM_CKE<3> (35 11 9)

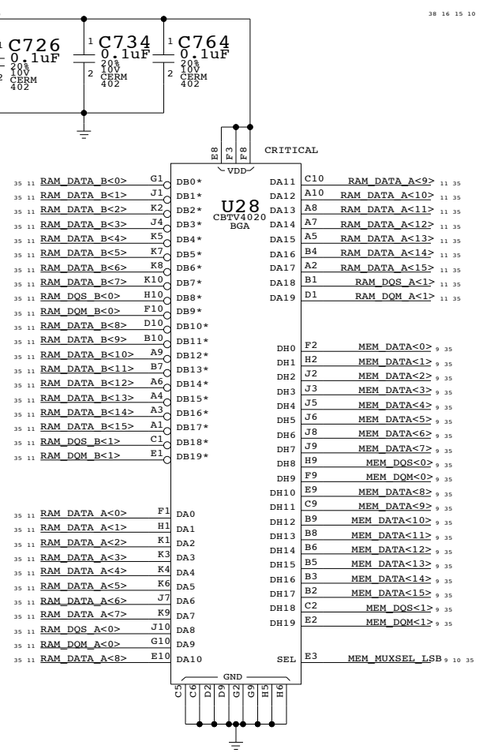
INT_2_5V_COLD	R247 10K 5% 1/16W MF 402	RAM_CKE<0>
INT_2_5V_COLD	R257 10K 5% 1/16W MF 402	RAM_CKE<1>
INT_2_5V_COLD	R260 10K 5% 1/16W MF 402	RAM_CKE<2>
INT_2_5V_COLD	R265 10K 5% 1/16W MF 402	RAM_CKE<3>

INT - DDR/BOOTROM

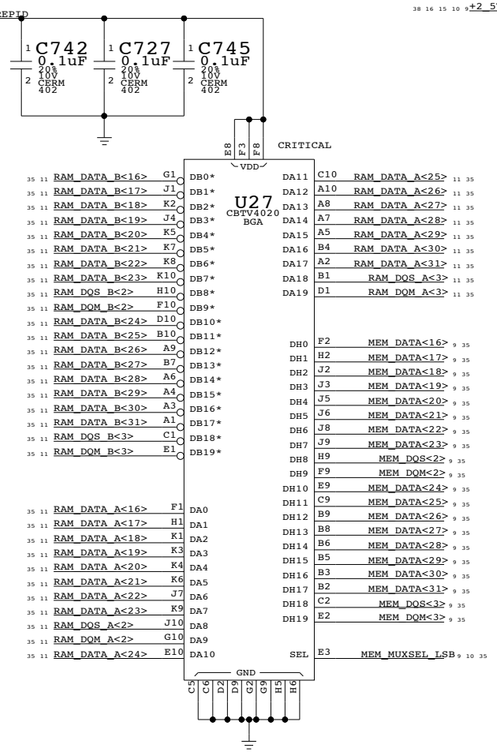
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6809	B
SCALE: NONE	SHT 9 OF 44	

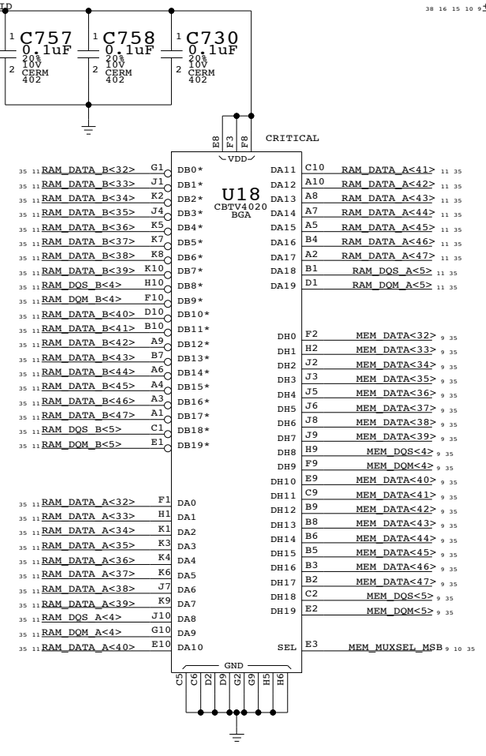
BIT 0..15



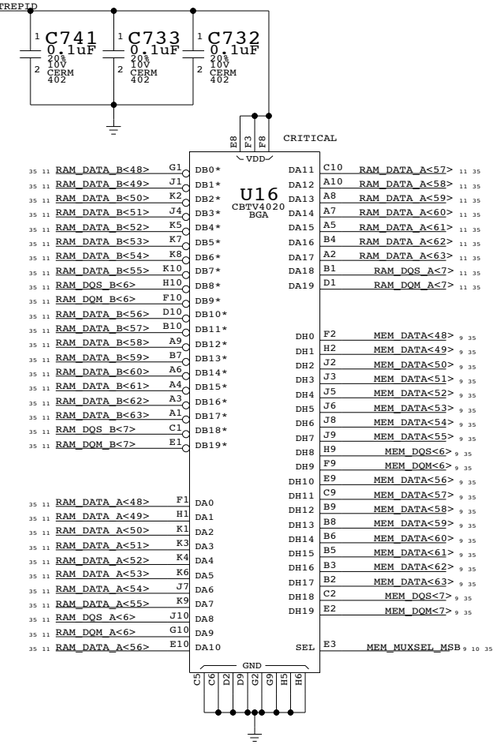
BIT 16..31



BIT 32..47



BIT 48..63

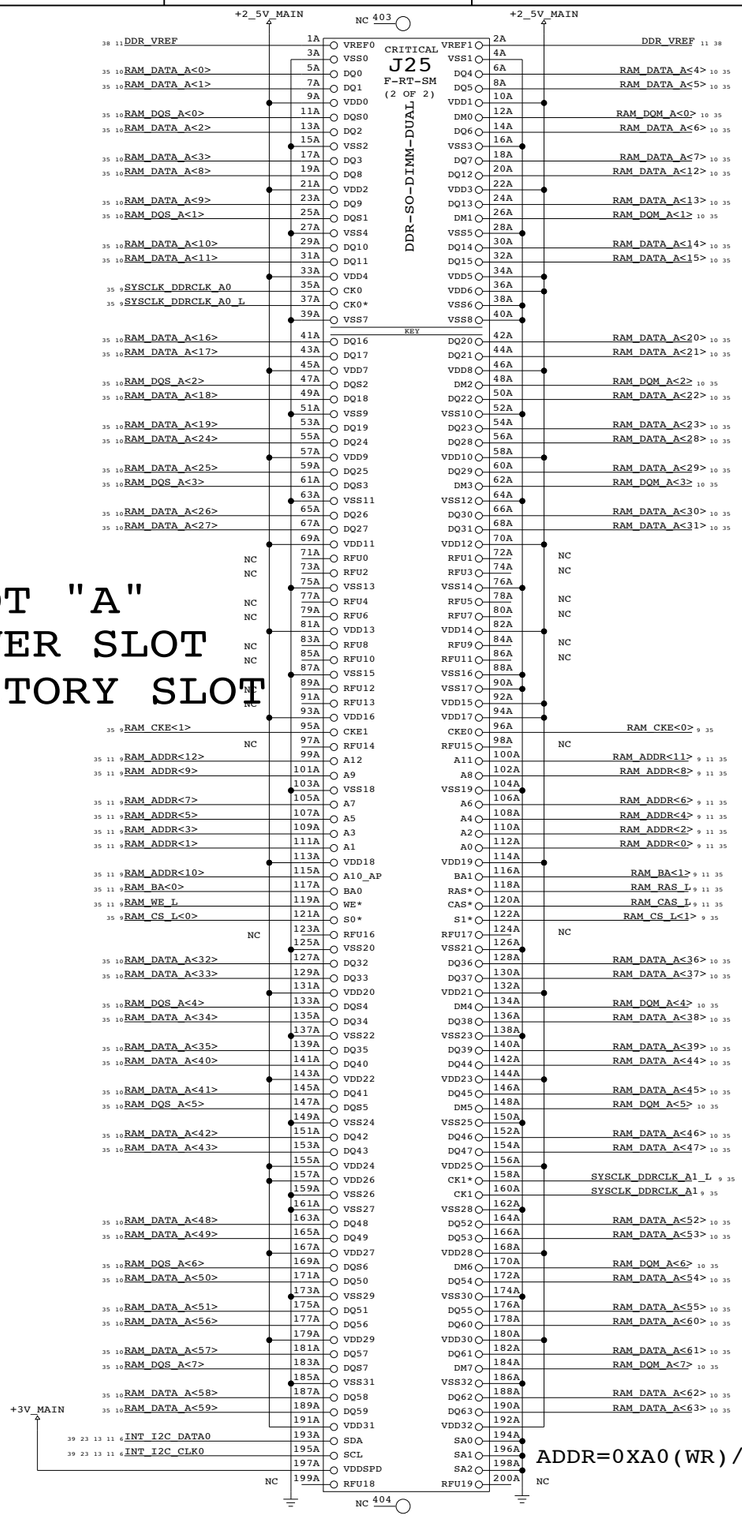


SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND

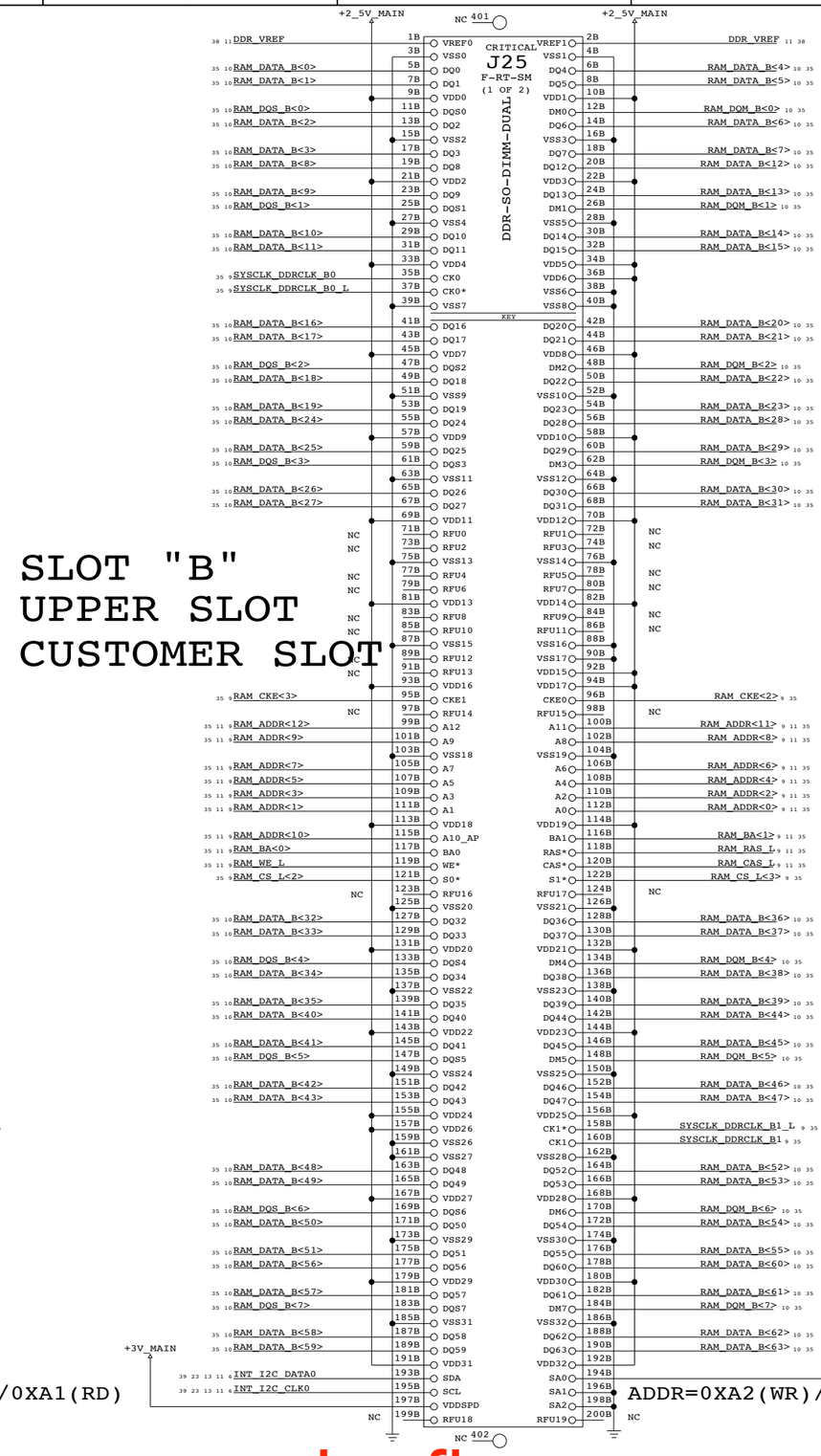
16BIT 2:1 DDR MUXES

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6809	B
SCALE: NONE	SHT 10 OF 44	

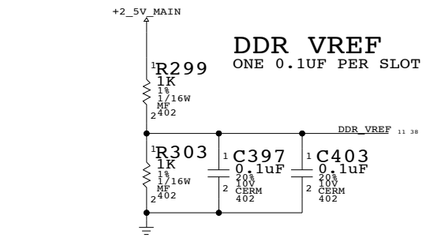


SLOT "A"
LOWER SLOT
FACTORY SLOT

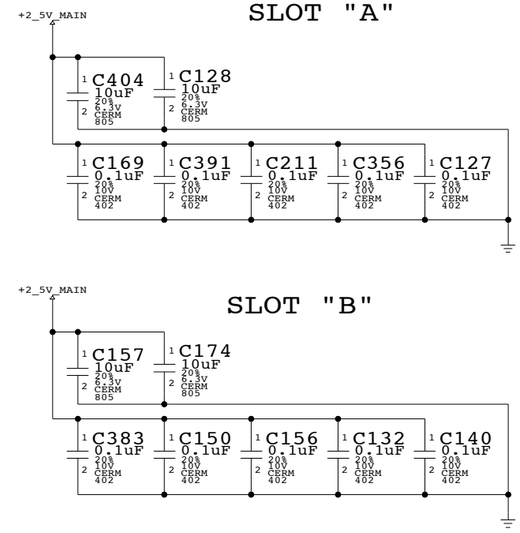


SLOT "B"
UPPER SLOT
CUSTOMER SLOT

NOTE: The SODIMM connector footprint has a through-hole slot on the PCB for additional mounting



DDR VREF
ONE 0.1UF PER SLOT



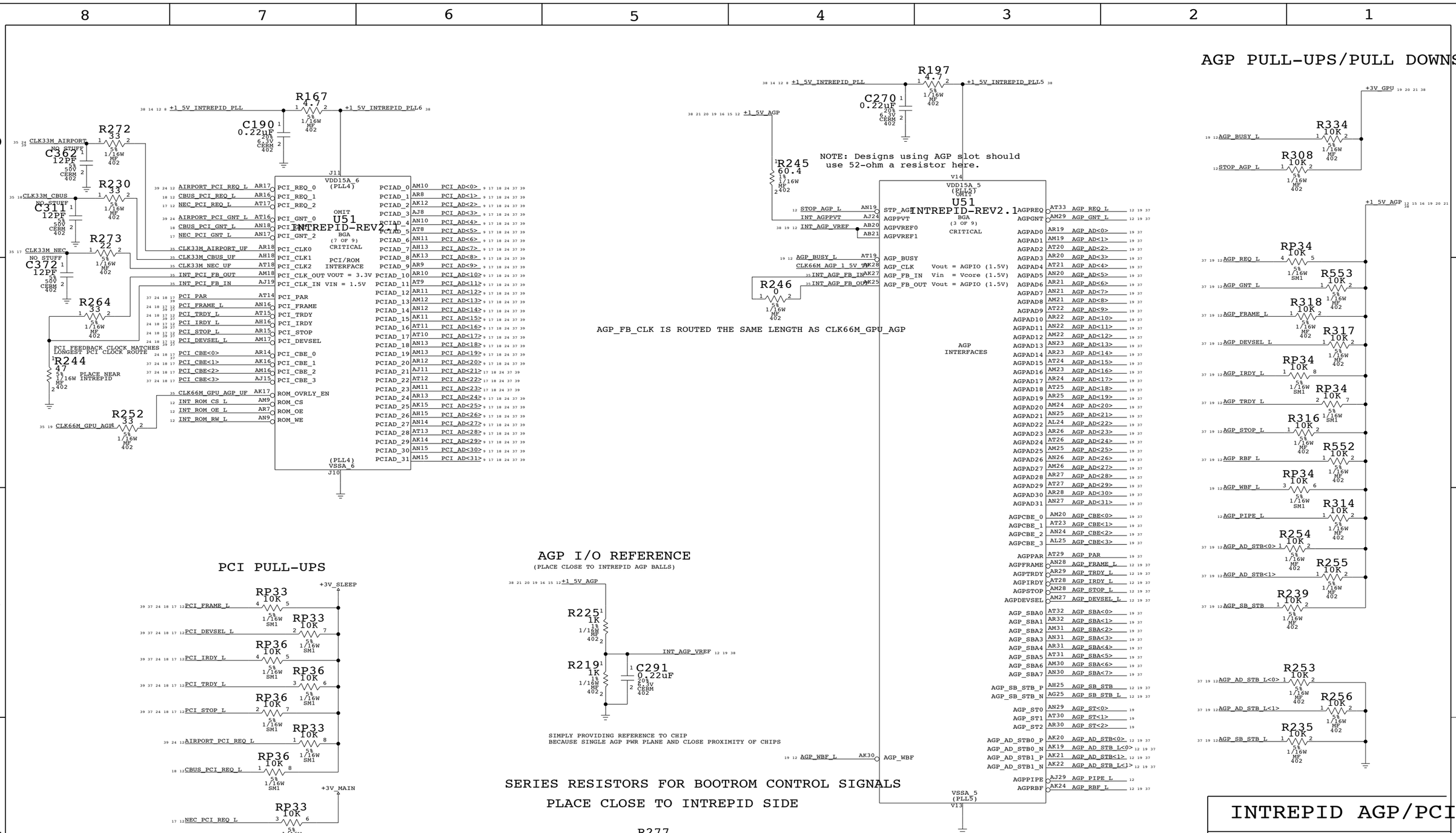
DDR BYPASS
SLOT "A"

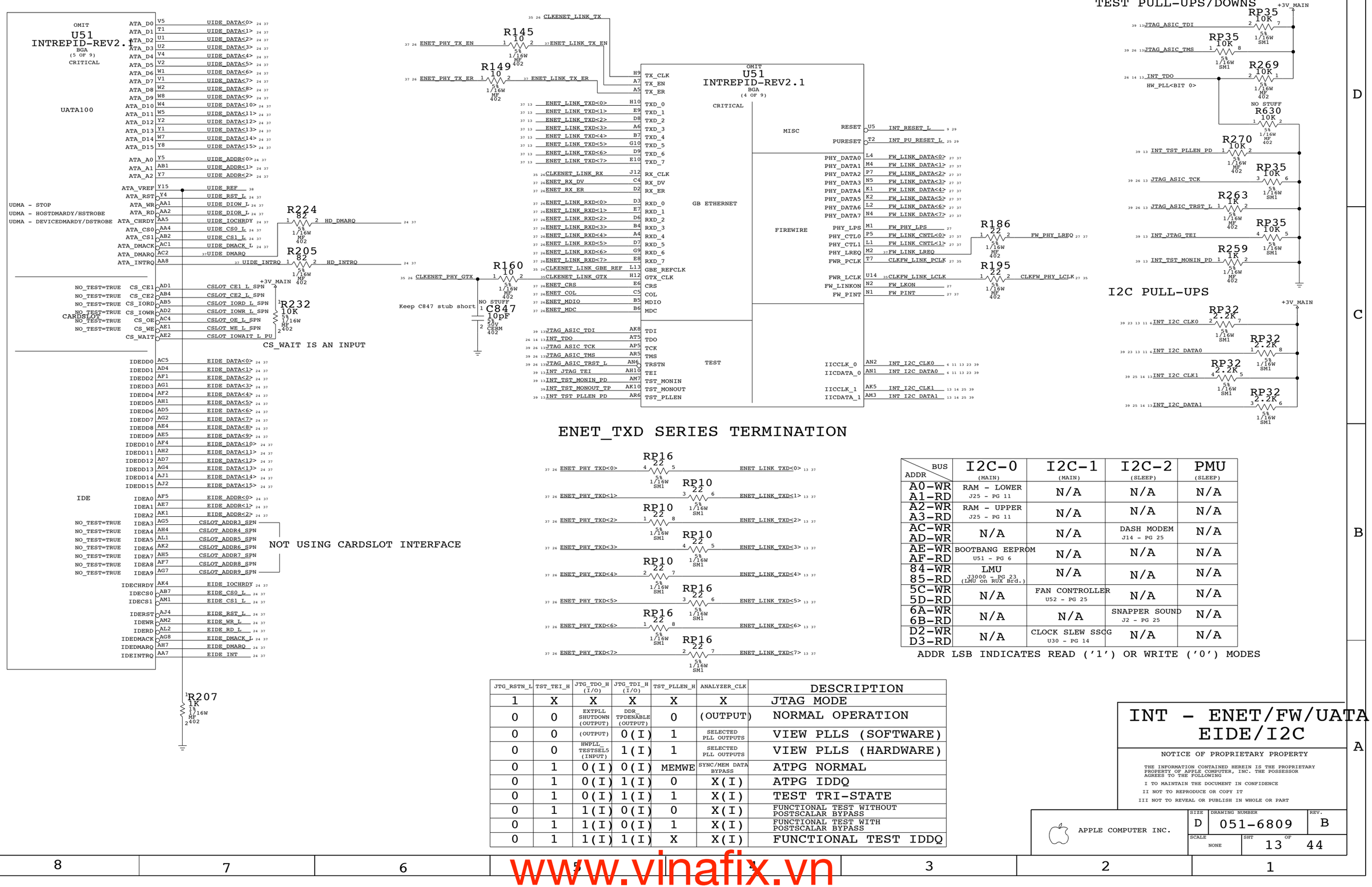
SLOT "B"

DDR SODIMM CONNS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6809	B
SCALE: NONE	SHT 11 OF 44	





USB PORT ASSIGNMENTS

PORT A - PORT D/UNUSED

R181 10K 5% 1/16W MF 402 — USB_DAM
R183 10K 5% 1/16W MF 402 — USB_DAP
R156 10K 5% 1/16W MF 402 — USB_DBM
R157 10K 5% 1/16W MF 402 — USB_DBP
R164 10K 5% 1/16W MF 402 — USB_DCM
R165 10K 5% 1/16W MF 402 — USB_DCP
R182 10K 5% 1/16W MF 402 — USB_DDM
R180 10K 5% 1/16W MF 402 — USB_DDP

PORT E/BLUETOOTH

R174 22 5% 1/16W MF 402 — USB_DEP → BT_USB_DP
R179 22 5% 1/16W MF 402 — USB_DEM → BT_USB_DM
R178 15K 1% 1/16W MF 402
R175 15K 1% 1/16W MF 402

PORT F/MODEM

R192 22 5% 1/16W MF 402 — USB_DFP → MODEM_USB_DP
R188 22 5% 1/16W MF 402 — USB_DFM → MODEM_USB_DM
R189 15K 1% 1/16W MF 402
R193 15K 1% 1/16W MF 402

INT - USB/GPIOS/I2S

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6809	B

SCALE: NONE — SHT 14 OF 44

PCI INTERRUPTS

GPIO/EXTINT PULLUPS

U49 LT1962-ADJ MSOP: IN, NC, NC, SHDN, OUT, ADJ, BYP, GND

U31 CY28512D TSSOP OMIT: CLKIN, FSEL, SCLK, SDATA, ADDRSEL, RESET*, PD*, LOCK, ODSEL; VDD0, VDD1, VDDA, VDDC, VDDQ; VSS0, VSS1, VSSA, VSSC, VSSQ

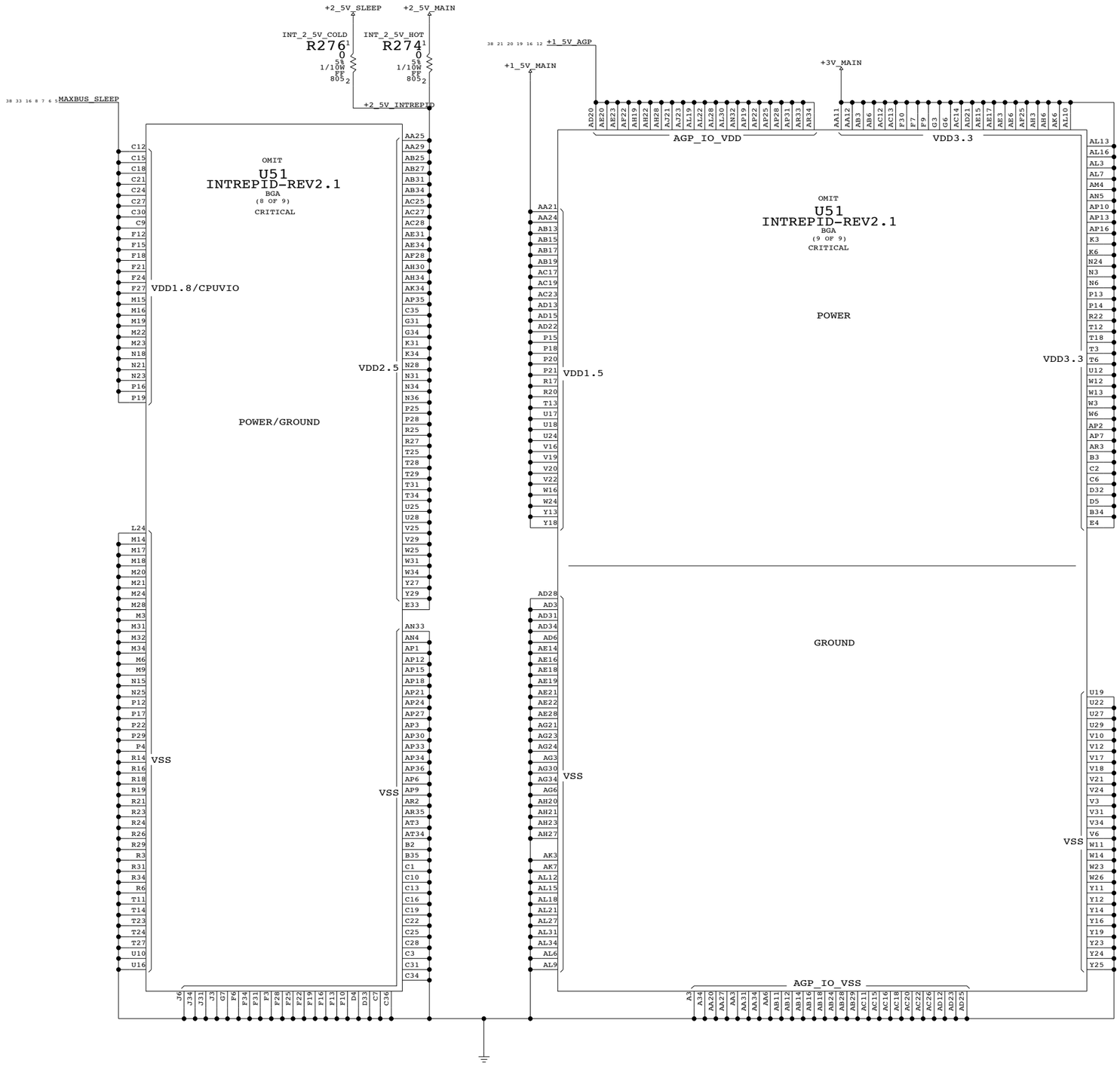
U51 INTREPID-REV2.1 BGA CRITICAL (6 OF 9) OMIT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
359S0086	1	IC,CY28512-2	U31	CRITICAL	SSCG

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0004	197S0035		Y2	Alt. for Siward Part

HWPLL_TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES	RES-0402-V2	RESISTOR	10K		1/16W	5%	R292	NO_SSCG



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0305	1	IC,ASIC,INTREPID,REV2.1,974 BGA,FAST	U51	CRITICAL	?

Intrepid Power

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6809	B
SCALE: NONE	SHT 15 OF 44	

INTREPID MAXBUS DECOUPLING

24 Balls
4 X 10UF (0805)
28 X 0.22UF (0402)

33 15 8 7 6 5 MAXBUS_SLEEP

C148 10uF 20% 6.3V CERM 805 · C142 10uF 20% 6.3V CERM 805 · C182 C178 C141 C145 C214 C163 C164 C225 C160 C159 · C144 10uF 20% 6.3V CERM 805 · C146 10uF 20% 6.3V CERM 805 · C204 C166 C205 C223 C229 C181 C207 C208 C183 C180 · C165 C206 C147 C149 C179 C162 C161 C213

0.22uF 20% 6.3V CERM 402

INTREPID CORE DECOUPLING

30 Balls
4 X 10UF (0805)
29 X 0.22UF (0402)

+1_5V_MAIN

C324 10uF 20% 6.3V CERM 805 · C325 10uF 20% 6.3V CERM 805 · C299 C279 C262 C292 C248 C302 C300 C290 C272 C259 · C201 10uF 20% 6.3V CERM 805 · C200 10uF 20% 6.3V CERM 805 · C301 C278 C226 C238 C250 C263 C224 C222 C261 C227 · C271 C310 C288 C260 C303 C287 C258 C236 C289

0.22uF 20% 6.3V CERM 402

INTREPID AGP I/O DECOUPLING

21 Balls
2 X 10UF (0805)
21 X 0.22UF (0402)

30 21 20 19 15 12 +1_5V_AGP

C381 10uF 20% 6.3V CERM 805 · C380 10uF 20% 6.3V CERM 805 · C367 C319 C330 C363 C366 C332 C361 C320 C328 C364 · C382 10uF 20% 6.3V CERM 805 · C379 10uF 20% 6.3V CERM 805 · C365 C329 C345 C346 C373 C344 C331 C312 C354 C347 · C321

0.22uF 20% 6.3V CERM 402

INTREPID 3.3V DECOUPLING

57 Balls
4 X 10UF (0805)
40 X 0.22UF (0402)

+3V_MAIN

C378 10uF 20% 6.3V CERM 805 · C376 10uF 20% 6.3V CERM 805 · C170 C358 C268 C327 C342 C215 C352 C171 C158 C309 · C377 10uF 20% 6.3V CERM 805 · C375 10uF 20% 6.3V CERM 805 · C175 C357 C351 C350 C286 C176 C189 C167 C371 C359 · C285 C283 C269 C221 C234 C247 C257 C343 C313 C228 · C360 C308 C318 C237 C317 C341 C177 C212 C349 C184

0.22uF 20% 6.3V CERM 402

INTREPID DDR DECOUPLING

44 Balls
4 X 10UF (0805)
46 X 0.22UF (0402)

38 15 10 9 +2_5V_INTREPID

C314 10uF 20% 6.3V CERM 805 · C322 10uF 20% 6.3V CERM 805 · C304 C266 C172 C281 C243 C253 C334 C241 C348 C192 · C191 10uF 20% 6.3V CERM 805 · C202 10uF 20% 6.3V CERM 805 · C306 C252 C275 C297 C240 C218 C274 C369 C368 C168 · C265 C251 C216 C254 C305 C186 C219 C315 C264 C294 · C323 C273 C242 C203 C333 C217 C230 C293 C231 C296 · C239 C316 C185 C282 C295 C280

0.22uF 20% 6.3V CERM 402

INTREPID/MAIN 2.5V DECOUPLING

10 X 0.22UF (0402)

+2_5V_MAIN

C770 C139 C335 C735 C245 C736 C739 C395 C374 C385

0.22uF 20% 6.3V CERM 402

Place these 2.5V Decoupling Caps near the Edge of +2.5V_MAIN and +2.5V_INTREPID split

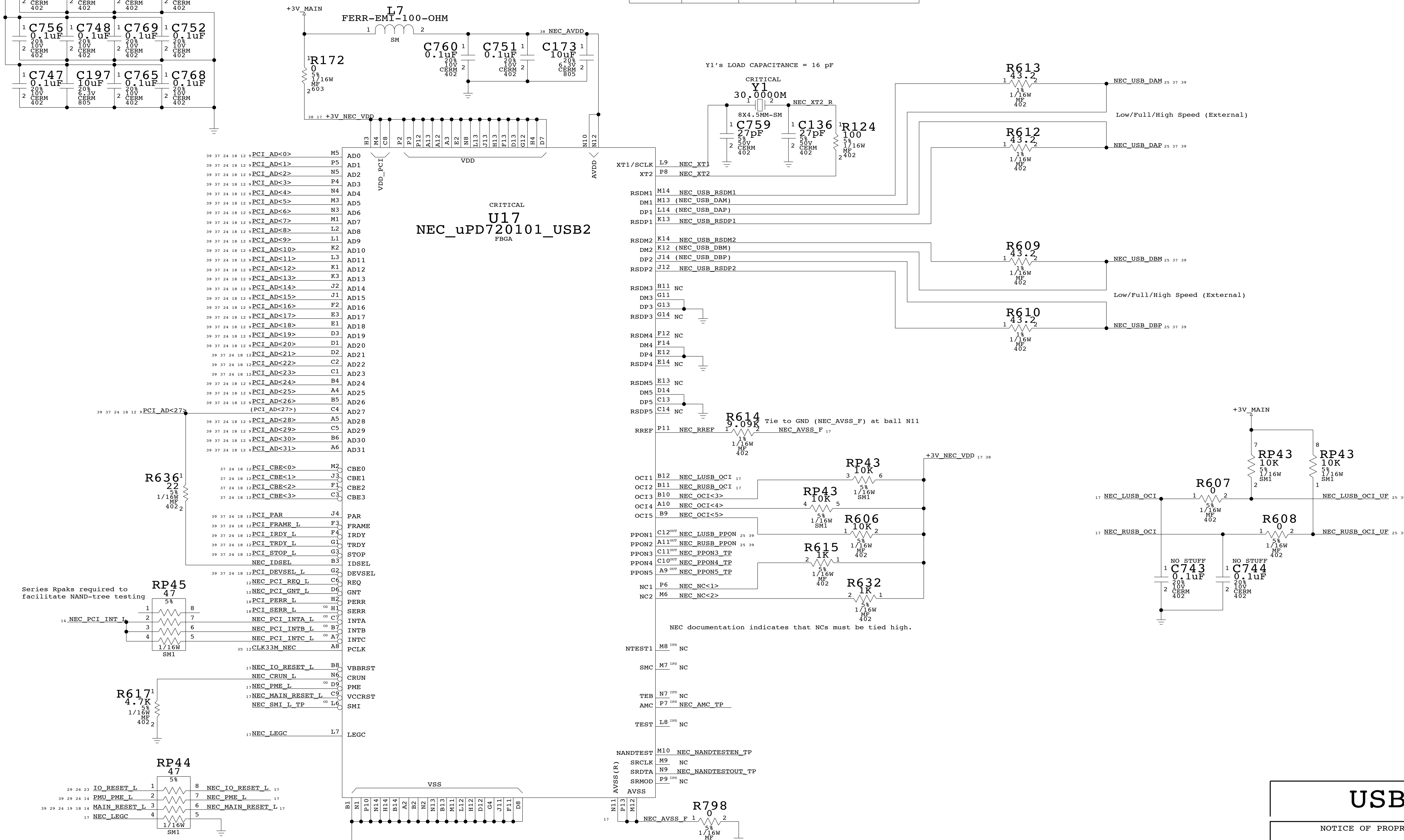
Intrepid Decoupling

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6809	B

SCALE	SHT	OF
NONE	16	44

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0608	197S0038		Y1	Alt. for Siward Part



+3V_NEC_VDD
C749 0.1uF 20% 10V CERM 402
C746 0.1uF 20% 10V CERM 402
C761 0.1uF 20% 10V CERM 402
C750 0.1uF 20% 10V CERM 402
C756 0.1uF
C748 0.1uF
C769 0.1uF
C752 0.1uF
C747 0.1uF
C197 10uF 20% 6.3V CERM 805
C765 0.1uF
C768 0.1uF
+3V_MAIN
L7 FERR-EMI-100-OHM SM
R172 0 5% 1/16W MF 603
C760 0.1uF
C751 0.1uF
C173 10uF 20% 6.3V CERM 805
NEC_AVDD
Y1's LOAD CAPACITANCE = 16 pF
CRITICAL Y1 30.0000M 8X4.5MM-SM
NEC_XT2_R
C759 27pF 5% 50V CERM 402
C136 27pF 5% 50V CERM 402
R124 100 5% 1/16W MF 402
R613 43.2 1% 1/16W MF 402
NEC_USB_DAM
R612 43.2
NEC_USB_DAP
Low/Full/High Speed (External)
R609 43.2
NEC_USB_DBM
R610 43.2
NEC_USB_DBP
Low/Full/High Speed (External)
CRITICAL
U17
NEC_uPD720101_USB2
FBGA
VDD_PCI
VDD
AVDD
XT1/SCLK
XT2
NEC_XT1
NEC_XT2
RSDM1 DM1 DP1 RSDP1
NEC_USB_RSDM1
NEC_USB_RSDP1
RSDM2 DM2 DP2 RSDP2
NEC_USB_RSDM2
NEC_USB_RSDP2
RSDM3 DM3 DP3 RSDP3
RSDM4 DM4 DP4 RSDP4
RSDM5 DM5 DP5 RSDP5
NC
RREF
R614 9.09K 1% 1/16W MF 402
NEC_RREF
Tie to GND (NEC_AVSS_F) at ball N11
NEC_AVSS_F
PCI_AD<0> … PCI_AD<31>
AD0 … AD31
PCI_CBE<0> … PCI_CBE<3>
CBE0 CBE1 CBE2 CBE3
R636 22 5% 1/16W MF 402
PCI_PAR PAR
PCI_FRAME_L FRAME
PCI_IRDY_L IRDY
PCI_TRDY_L TRDY
PCI_STOP_L STOP
NEC_IDSEL IDSEL
PCI_DEVSEL_L DEVSEL
NEC_PCI_REQ_L REQ
NEC_PCI_GNT_L GNT
PCI_PERR_L PERR
PCI_SERR_L SERR
NEC_PCI_INTA_L INTA
NEC_PCI_INTB_L INTB
NEC_PCI_INTC_L INTC
CLK33M_NEC PCLK
Series Rpaks required to facilitate NAND-tree testing
RP45 47 5% 1/16W SM1
NEC_PCI_INT_L
NEC_IO_RESET_L VBBRST
NEC_CRUN_L CRUN
NEC_PME_L PME
NEC_MAIN_RESET_L VCCRST
NEC_SMI_L_TP SMI
NEC_LEGC LEGC
R617 4.7K 5% 1/16W MF 402
RP44 47 5% 1/16W SM1
IO_RESET_L NEC_IO_RESET_L
PMU_PME_L NEC_PME_L
MAIN_RESET_L NEC_MAIN_RESET_L
NEC_LEGC
OCI1 OCI2 OCI3 OCI4 OCI5
NEC_LUSB_OCI
NEC_RUSB_OCI
NEC_OCI<3>
NEC_OCI<4>
NEC_OCI<5>
PPON1 PPON2 PPON3 PPON4 PPON5
NEC_LUSB_PPON
NEC_RUSB_PPON
NEC_PPON3_TP
NEC_PPON4_TP
NEC_PPON5_TP
NC1 NC2
NEC_NC<1>
NEC_NC<2>
+3V_NEC_VDD
RP43 10K 5% 1/16W SM1
R606 10K 5% 1/16W MF 402
R615 1K 5% 1/16W MF 402
R632 1K 5% 1/16W MF 402
NEC documentation indicates that NCs must be tied high.
NTEST1 SMC TEB AMC TEST
NEC_AMC_TP
NANDTEST SRCLK SRDTA SRMOD AVSS
NEC_NANDTESTEN_TP
NEC_NANDTESTOUT_TP
AVSS(R)
VSS
R798 0 5% 1/16W MF 603
+3V_MAIN
RP43 10K 5% 1/16W SM1
R607 0 5% 1/16W MF 402
R608 0 5% 1/16W MF 402
NEC_LUSB_OCI
NEC_LUSB_OCI_UF
NEC_RUSB_OCI
NEC_RUSB_OCI_UF
NO STUFF C743 0.1uF 20% 10V CERM 402
NO STUFF C744 0.1uF 20% 10V CERM 402

USB 2.0

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6809	B
SCALE NONE	SHT 17 OF 44	

PCI1510 PULL-UPS

+3V_SLEEP
R756 0 5% 1/16W MF 603
+3V_SLEEP_PCCARD
C60 10uF 20% 6.3V CERM 805
C776 10uF 20% 6.3V CERM 805
C789 0.22uF 20% 6.3V CERM 402
C791 0.22uF 20% 6.3V CERM 402
C784 0.22uF 20% 6.3V CERM 402
C782 0.22uF 20% 6.3V CERM 402
C783 0.22uF 20% 6.3V CERM 402
C778 0.22uF 20% 6.3V CERM 402
C775 0.22uF 20% 6.3V CERM 402
R721 10K 5% 1/16W MF 402
A7 C13 D5 E1 M1 N7 N11
VCC

+3V_SLEEP_PCCARD
R718 10K 5% 1/16W MF 402 — PCI_PERR_L
R714 10K 5% 1/16W MF 402 — PCI_SERR_L
R722 10K 5% 1/16W MF 402 — CBUS_SUSPEND_PU
+2_5V_SLEEP
C787 4.7uF 20% 6.3V CERM 805
C786 0.22uF 20% 6.3V CERM 402

+3V_MAIN
+5V_MAIN
R726 0 5% 1/16W MF 402
SLEEP_L_LS5
TPS2211_SHTDWN_L

U4
TPS2211
SSOI
NC
V_12 AVPP
V_5_1
V_5_2 AVCC0
V_3_1 AVCC1
V_3_2 AVCC2
VCCD0
VCCD1
VPPD0
VPPD1
SHTDWN
GND
OC
+VPP_CBUS_SW
+VCC_CBUS_SW
C40 0.1uF 20% 10V CERM 402
C37 0.1uF 20% 10V CERM 402

MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES TO MINIMIZE INDUCTANCE!

0.1UF ARE USED TO INCREASE ESD DISCHARGES OF UP TO 10KV

CRITICAL
U8
PCI1510GGU
BGA

CLAMP FOR PC-CARD
CLAMP FOR PCI

NC — CLK_48_RSVD/NC
PCI1510_VR_EN_L — VR_EN*
VR_PORT
VCCCB
VCCP
VCCD0* — CBUS_VCCD0_L
VCCD1* — CBUS_VCCD1_L
VPPD0 — CBUS_VPPD0
VPPD1 — CBUS_VPPD1

AD0 PCI_AD<0>
AD1 PCI_AD<1>
AD2 PCI_AD<2>
AD3 PCI_AD<3>
AD4 PCI_AD<4>
AD5 PCI_AD<5>
AD6 PCI_AD<6>
AD7 PCI_AD<7>
AD8 PCI_AD<8>
AD9 PCI_AD<9>
AD10 PCI_AD<10>
AD11 PCI_AD<11>
AD12 PCI_AD<12>
AD13 PCI_AD<13>
AD14 PCI_AD<14>
AD15 PCI_AD<15>
AD16 PCI_AD<16>
AD17 PCI_AD<17>
AD18 PCI_AD<18>
AD19 (PCI_AD<19>)
AD20 PCI_AD<20>
AD21 PCI_AD<21>
AD22 PCI_AD<22>
AD23 PCI_AD<23>
AD24 PCI_AD<24>
AD25 PCI_AD<25>
AD26 PCI_AD<26>
AD27 PCI_AD<27>
AD28 PCI_AD<28>
AD29 PCI_AD<29>
AD30 PCI_AD<30>
AD31 PCI_AD<31>

C/BE0* PCI_CBE<0>
C/BE1* PCI_CBE<1>
C/BE2* PCI_CBE<2>
C/BE3* PCI_CBE<3>

PAR PCI_PAR
IRDY PCI_IRDY_L
SERR PCI_SERR_L
IDSEL CBUS_PCI_IDSEL
PERR PCI_PERR_L
FRAME PCI_FRAME_L
STOP PCI_STOP_L
TRDY PCI_TRDY_L
DEVSEL PCI_DEVSEL_L
PRST CBUS_PCI_RESET_L
REQ CBUS_PCI_REQ_L
GNT CBUS_PCI_GNT_L
PCLK CLK33M_CBUS

SPKROUT
RI_OUT/PME
SUSPEND CBUS_SUSPEND_PU
MFUNC0 CBUS_INT_L
MFUNC1 CBUS_MFUNC1_PD
MFUNC2 CBUS_MFUNC2_PD
MFUNC3 CBUS_MFUNC3_PD
MFUNC4 CBUS_MFUNC4_PD
MFUNC5 CBUS_MFUNC5_PD
MFUNC6 CBUS_MFUNC6_PD
GRST

R719 22 5% 1/16W MF 402
R723 47 5% 1/16W MF 402 — MAIN_RESET_L
RP1 10K 5% 1/32W 25V SM — CBUS_MFUNC1_PD … CBUS_MFUNC6_PD

CD1*/CCD1* CBUS_DET_1_L
CD2*/CCD2* CBUS_DET_2_L
IORD*/CAD13 CBUS_IORD_L
IOWR*/CAD15 CBUS_IOWR_L
OE*/CAD11 CBUS_OE_L
CE1*/CC/BE0* CBUS_CE1_L
VS1*/CVS1 CBUS_VS1
VS2*/CVS2 CBUS_VS2
WE*/CGNT* CBUS_WE_L
RDY/IREQ*/CINT* CBUS_READY
RESET/CRST* CBUS_RESET_L
REG*/CC/BE3* CBUS_REG_L
BVD1/CSTSCHG/STSCHG*/RI* CBUS_BVD1_L
BVD2/SPKR*/CAUDIO CBUS_BVD2_L
INTEGRATED PULL-UP WP/IOIS16*/CCLKRUN* CBUS_WP_L
CE2/CAD10* CBUS_CE2_L
INPACK/CREQ* CBUS_INPACK_L
WAIT/CSERR* CBUS_WAIT_L

A0/CAD26 CBUS_ADDR<0>
A1/CAD25 CBUS_ADDR<1>
A2/CAD24 CBUS_ADDR<2>
A3/CAD23 CBUS_ADDR<3>
A4/CAD22 CBUS_ADDR<4>
A5/CAD21 CBUS_ADDR<5>
A6/CAD20 CBUS_ADDR<6>
A7/CAD18 CBUS_ADDR<7>
A8/CC/BE1* CBUS_ADDR<8>
A9/CAD14 CBUS_ADDR<9>
A10/CAD9 CBUS_ADDR<10>
A11/CAD12 CBUS_ADDR<11>
A12/CC/BE2* CBUS_ADDR<12>
A13/CPAR CBUS_ADDR<13>
A14/CPERR* CBUS_ADDR<14>
A15/CIRDY* CBUS_ADDR<15>
A16/CCLK CBUS_ADDR_16_UF
A17/CAD16 CBUS_ADDR<17>
A18/RSVD CBUS_ADDR<18>
A19/CBLOCK* CBUS_ADDR<19>
A20/CSTOP* CBUS_ADDR<20>
A21/CDEVSEL* CBUS_ADDR<21>
A22/CTRDY* CBUS_ADDR<22>
A23/CFRAME* CBUS_ADDR<23>
A24/CAD17 CBUS_ADDR<24>
A25/CAD19 CBUS_ADDR<25>

R724 47 5% 1/16W MF 402 — CBUS_ADDR<16>

D0/CAD27 CBUS_DATA<0>
D1/CAD29 CBUS_DATA<1>
D2/RSVD CBUS_DATA<2>
D3/CAD0 CBUS_DATA<3>
D4/CAD1 CBUS_DATA<4>
D5/CAD3 CBUS_DATA<5>
D6/CAD5 CBUS_DATA<6>
D7/CAD7 CBUS_DATA<7>
D8/CAD28 CBUS_DATA<8>
D9/CAD30 CBUS_DATA<9>
D10/CAD31 CBUS_DATA<10>
D11/CAD2 CBUS_DATA<11>
D12/CAD4 CBUS_DATA<12>
D13/CAD6 CBUS_DATA<13>
D14/RSVD CBUS_DATA<14>
D15/CAD8 CBUS_DATA<15>

GND
A2 A11 D1 F13 H4 K8 M13 N2

PC CARD/CARDBUS CONNECTOR

CRITICAL
J5
QT500806-L111
M-ST-SM1

	2	1	CBUS_DATA<3>
CBUS_DET_1_L	4	3	CBUS_DATA<4>
CBUS_DATA<11>	6	5	CBUS_DATA<5>
CBUS_DATA<12>	8	7	CBUS_DATA<6>
CBUS_DATA<13>	10	9	
	12	11	CBUS_DATA<7>
CBUS_DATA<14>	14	13	CBUS_CE1_L
CBUS_DATA<15>	16	15	CBUS_ADDR<10>
CBUS_CE2_L	18	17	CBUS_OE_L
CBUS_VS1	20	19	
	22	21	CBUS_ADDR<11>
CBUS_IORD_L	24	23	CBUS_ADDR<9>
CBUS_IOWR_L	26	25	CBUS_ADDR<8>
CBUS_ADDR<17>	28	27	CBUS_ADDR<13>
CBUS_ADDR<18>	30	29	
	32	31	CBUS_ADDR<14>
CBUS_ADDR<19>	34	33	CBUS_WE_L
CBUS_ADDR<20>	36	35	CBUS_READY
CBUS_ADDR<21>	38	37	+VCC_CBUS_SW
+VCC_CBUS_SW	40	39	
	42	41	+VPP_CBUS_SW
+VPP_CBUS_SW	44	43	CBUS_ADDR<16>
CBUS_ADDR<22>	46	45	CBUS_ADDR<15>
CBUS_ADDR<23>	48	47	CBUS_ADDR<12>
CBUS_ADDR<24>	50	49	
	52	51	CBUS_ADDR<7>
CBUS_ADDR<25>	54	53	CBUS_ADDR<6>
CBUS_VS2	56	55	CBUS_ADDR<5>
CBUS_RESET_L	58	57	CBUS_ADDR<4>
CBUS_WAIT_L	60	59	
	62	61	CBUS_ADDR<3>
CBUS_INPACK_L	64	63	CBUS_ADDR<2>
CBUS_REG_L	66	65	CBUS_ADDR<1>
CBUS_BVD2_L	68	67	CBUS_ADDR<0>
CBUS_BVD1_L	70	69	
	72	71	CBUS_DATA<0>
CBUS_DATA<8>	74	73	CBUS_DATA<1>
CBUS_DATA<9>	76	75	CBUS_DATA<2>
CBUS_DATA<10>	78	77	CBUS_WP_L
CBUS_DET_2_L	80	79	

84 81 83 82

TI REFERENCE SCHEMATIC DID NOT HAVE BULK ON +VCC_CBUS_SW
C796 2.2uF 10% 10V CERM 805
C800 2.2uF 10% 10V CERM 805

CARDBUS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6809	B

SCALE	SHT	OF
NONE	18	44

SIL1162 DVI-Compliant Transmitter

Ext. TMDS source termination

M11 AGP INTERFACE

SPREAD SPECTRUM SUPPORT
S0=1;S1=M => -1.5% DOWN-SPREAD

27M OSC

FOR 2.5 VDDR1
MEMVMODE0=1.8V
MEMVMODE1=GND
FOR 1.8 VDDR1
MEMVMODE0=GND
MEMVMODE1=1.8V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0318	197S0048		G1	Alt. for Siward Part

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6809	B
SCALE: NONE	SHT 19 OF 44	

Int.TMDS Termination

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN
CMF LINE SHOULD BE ROUTED AS 4MIL SURFACE
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS

GPU_TMDS_CLK_CMF
R374 49.9 1% 1/16W MF 402 — GPU_TMDS_CLKP
R377 49.9 1% 1/16W MF 402 — GPU_TMDS_CLKN
C536 470pF 10% 50V CERM 402
C522 470pF 10% 50V CERM 402

GPU_TMDS_D0_CMF
R367 75 1% 1/16W MF 402 — GPU_TMDS_D0P
R369 75 1% 1/16W MF 402 — GPU_TMDS_D0N
C511 470pF 10% 50V CERM 402
C507 470pF 10% 50V CERM 402

GPU_TMDS_D1_CMF
R362 75 1% 1/16W MF 402 — GPU_TMDS_D1P
R355 75 1% 1/16W MF 402 — GPU_TMDS_D1N
C487 470pF 10% 50V CERM 402
C497 470pF 10% 50V CERM 402

GPU_TMDS_D2_CMF
R350 75 1% 1/16W MF 402 — GPU_TMDS_D2P
R340 75 1% 1/16W MF 402 — GPU_TMDS_D2N
C479 470pF 10% 50V CERM 402
C469 470pF 10% 50V CERM 402

R765 0 5% 1/16W MF 402 — GPU_TMDS_DN<0> — ATI_TMDS_DN<0>
R767 0 5% 1/16W MF 402 — GPU_TMDS_DP<0> — ATI_TMDS_DP<0>
R760 0 5% 1/16W MF 402 — GPU_TMDS_DN<1> — ATI_TMDS_DN<1>
R762 0 5% 1/16W MF 402 — GPU_TMDS_DP<1> — ATI_TMDS_DP<1>
R764 0 5% 1/16W MF 402 — GPU_TMDS_DN<2> — ATI_TMDS_DN<2>
R766 0 5% 1/16W MF 402 — GPU_TMDS_DP<2> — ATI_TMDS_DP<2>
R761 0 5% 1/16W MF 402 — GPU_TMDS_CLKN — ATI_TMDS_CLKN
R763 0 5% 1/16W MF 402 — GPU_TMDS_CLKP — ATI_TMDS_CLKP

Place all TMDS 10 ohms close to GPU

+1_8V_GPU
+3V_GPU
R389 10K 5% 1/16W MF 402 — EXT TMDS
R840 10K 5% 1/16W MF 402 — ZV_LCDDATA20_PU
R378 1K 5% 1/16W MF 402
NO STUFF R380 10K 5% 1/16W MF 402 — HPD_PWR_SNS_EN

R351 1K 5% 1/16W MF 402 — ATI_TESTEN

ATI 64MB CRITICAL
U47 RAGE_MOBILITY M11-CSP64 64MB BGA (3_OF_6)

ROMCSB	AE5	NC
R	AK28	GPU_R
G	AK27	GPU_G
B	AK26	GPU_B
VSYNC	AG27	ATI_VSYNC
V2SYNC	AG25	NC
HSYNC	AG26	ATI_HSYNC
H2SYNC	AG24	NC
RSET	AK25	ATI_RSET
R2SET	AJ24	ATI_R2SET
Y_G	AK23	GPU_Y
C_R	AK24	GPU_C
COMP_B	AK22	GPU_COMP
DIGON	AE13	FP_PWR_EN
BLON	AF13	INV_ON_PWM
HPD1	AF11	GPU_HPD
AUXWIN	AJ27	AUXWIN_PU
DDC1DATA	AH28	GPU_DVI_DDC_DATA
DDC1CLK	AH27	GPU_DVI_DDC_CLK
DDC2DATA	AE12	LVDS_DDC_DATA
DDC2CLK	AF12	LVDS_DDC_CLK
DDC3DATA	AH26	SI_I2S_DATA
DDC3CLK	AH25	SI_I2C_CLK
TXOUT_U0N	AH18	LVDS_U0N
TXOUT_U0P	AG18	LVDS_U0P
TXOUT_U1N	AH19	LVDS_U1N
TXOUT_U1P	AG19	LVDS_U1P
TXOUT_U2N	AH20	LVDS_U2N
TXOUT_U2P	AG20	LVDS_U2P
TXOUT_U3N	AH22	LVDS_U3N_TP (NO ICT TEST)
TXOUT_U3P	AG22	LVDS_U3P_TP (NO ICT TEST)
TXCLK_UN	AH21	CLKLVDS_UN
TXCLK_UP	AG21	CLKLVDS_UP
TXOUT_L0N	AK16	LVDS_L0N
TXOUT_L0P	AJ16	LVDS_L0P
TXOUT_L1N	AK17	LVDS_L1N
TXOUT_L1P	AJ17	LVDS_L1P
TXOUT_L2N	AK18	LVDS_L2N
TXOUT_L2P	AJ18	LVDS_L2P
TXOUT_L3N	AK20	LVDS_L3N_TP (NO ICT TEST)
TXOUT_L3P	AJ20	LVDS_L3P_TP (NO ICT TEST)
TXCLK_LN	AK19	CLKLVDS_LN
TXCLK_LP	AJ19	CLKLVDS_LP
SSOUT	AJ25	NC
VSS	A20	
VSS	B21	

ATI_DVOD<0>	AJ5	ZV_LCDDATA0
ATI_DVOD<1>	AK5	ZV_LCDDATA1
ATI_DVOD<2>	AG6	ZV_LCDDATA2
ATI_DVOD<3>	AH6	ZV_LCDDATA3
ATI_DVOD<4>	AJ6	ZV_LCDDATA4
ATI_DVOD<5>	AK6	ZV_LCDDATA5
ATI_DVOD<6>	AG7	ZV_LCDDATA6
ATI_DVOD<7>	AH7	ZV_LCDDATA7
ATI_DVOD<8>	AJ7	ZV_LCDDATA8
ATI_DVOD<9>	AK7	ZV_LCDDATA9
ATI_DVOD<10>	AG8	ZV_LCDDATA10
ATI_DVOD<11>	AH8	ZV_LCDDATA11
NC	AJ8	ZV_LCDDATA12
NC	AK8	ZV_LCDDATA13
NC	AG9	ZV_LCDDATA14
NC	AH9	ZV_LCDDATA15
NC	AJ9	ZV_LCDDATA16
NC	AK9	ZV_LCDDATA17
NC	AG10	ZV_LCDDATA18
NC	AH10	ZV_LCDDATA19
NC	AJ10	ZV_LCDDATA20_PU
NC	AK10	ZV_LCDDATA21
NC	AG11	ZV_LCDDATA22
NC	AH11	ZV_LCDDATA23
ATI_DVO_VSYNC	AJ4	ZV_LCDCNTL0
ATI_DVO_HSYNC	AK4	ZV_LCDCNTL1
ATI_DVOD_DE	AH5	ZV_LCDCNTL2
ATI_DVO_CLKP	AG5	ZV_LCDCNTL3
ATI_AGP_FBSKEW<0>	AJ2	GPIO0
ATI_AGP_FBSKEW<1>	AK2	GPIO1
ATI_X1CLK_SKEW<0>	AK1	GPIO2
ATI_X1CLK_SKEW<1>	AH3	GPIO3
ATI_BUS_CFG<0>	AH2	GPIO4
ATI_BUS_CFG<1>	AJ1	GPIO5
ATI_BUS_CFG<2>	AF4	GPIO6
ATI_GPIO7_SPN	AH1	GPIO7
ATI_GPIO8_PD	AG3	GPIO8
ATI_GPIO9_SPN	AF3	GPIO9
ATI_GPIO10_SPN	AG2	GPIO10
ATI_GPIO11_SPN	AF2	GPIO11
ATI_GPIO12_SPN	AG1	GPIO12
ATI_GPIO13_SPN	AF1	GPIO13
HPD_PWR_SNS_EN	AE2	GPIO14
GPU_VCORE_CNTL_L	AE1	GPIO15
ATI_SSCLK_IN	M1	GPIO16
ATI_TMDS_DN<0>	AJ13	TX0M
ATI_TMDS_DP<0>	AK13	TX0P
ATI_TMDS_DN<1>	AJ14	TX1M
ATI_TMDS_DP<1>	AK14	TX1P
ATI_TMDS_DN<2>	AJ15	TX2M
ATI_TMDS_DP<2>	AK15	TX2P
ATI_TMDS_CLKN	AJ12	TXCM
ATI_TMDS_CLKP	AK12	TXCP
ATI_CLK27M_IN	AJ29	XTALIN
NC	AJ30	XTALOUT
NC	AH24	TESTEN
NC	AJ26	SSIN
	B24	VSS
	B20	VSS
	A24	VSS

+1_5V_AGP
CRITICAL Q23 SI3446DV TSOP
L17 FERR-220-OHM 0805
GPU_CORE_OK
+GPU_VDD15_UF
C407 1000pF 10% 25V X7R 402

R346 75 1% 1/16W MF 402 OMIT
R342 75 1% 1/16W MF 402 OMIT
R341 75 1% 1/16W MF 402 OMIT

R332 715 1% 1/16W MF 402
R333 499 1% 1/16W MF 402
R359 75 1% 1/16W MF 402
R356 75 1% 1/16W MF 402
R360 75 1% 1/16W MF 402

R779 10K 5% 1/16W MF 402 — +3V_GPU
R366 10K 5% 1/16W MF 402
R368 10K 5% 1/16W MF 402

M10 Power Shut down Sequencing

XW11 SM — DP5 BAS16TW SOT-363 — +2_5V_SLEEP_NECK — XW9 SM — +2_5V_SLEEP
XW12 SM — DP5 BAS16TW SOT-363 — +1_5V_AGP_NECK — XW4 — +1_5V_AGP
XW5 SM — DP5 BAS16TW SOT-363 — +GPU_VDD15_UF

+1_8V_ATI_PVDD
+1_8V_PVDD_NECK
GPU_VCORE
GPU_VCORE_NECK
+GPU_VDD15_NECK

+1_5V_GPU_VDD15 (500mA)

C448 0.01uF 20% 16V CERM 402
C443 0.01uF 20% 16V CERM 402
C435 0.01uF 20% 16V CERM 402
C482 0.01uF 20% 16V CERM 402
C411 10uF 20% 6.3V CERM 805
C505 0.01uF 20% 16V CERM 402
C532 0.01uF 20% 16V CERM 402
C529 0.01uF 20% 16V CERM 402
C526 0.01uF 20% 16V CERM 402

GPU VCORE - 1.2V

(PUT ALL CAPs BELOW ATI ASIC)

C484 10uF 20% 6.3V CERM 805
C485 10uF 20% 6.3V CERM 805
C440 0.22uF 20% 6.3V CERM 402
C441 0.22uF 20% 6.3V CERM 402
C445 0.22uF 20% 6.3V CERM 402
C446 0.22uF 20% 6.3V CERM 402
C449 0.22uF 20% 6.3V CERM 402
C434 0.22uF 20% 6.3V CERM 402
C452 0.22uF 20% 6.3V CERM 402
C451 0.22uF 20% 6.3V CERM 402
C494 0.22uF 20% 6.3V CERM 402
C498 0.22uF 20% 6.3V CERM 402
C509 0.22uF 20% 6.3V CERM 402
C510 0.22uF 20% 6.3V CERM 402
C512 0.22uF 20% 6.3V CERM 402
C513 0.22uF 20% 6.3V CERM 402
C524 0.22uF 20% 6.3V CERM 402
C525 0.22uF 20% 6.3V CERM 402
C528 0.22uF 20% 6.3V CERM 402
C531 0.22uF 20% 6.3V CERM 402
C533 0.22uF 20% 6.3V CERM 402
C477 0.22uF 20% 6.3V CERM 402
C486 0.22uF 20% 6.3V CERM 402
C495 0.22uF 20% 6.3V CERM 402

CRITICAL
ATI 64MB U47 RAGE_MOBILITY M11-CSP64 64MB BGA (5_OF_6)

VDD15	F12	
	L6	
	T6	
	AB6	
	F17	
	G25	
	R25	
	AB25	
	AJ3	
	AF25	
	AG4	
	AH4	
	AF5	
	F6	
	G6	
	H6	
	P6	
	AD26	
VDDC	V6	
	W6	
	AC6	
	AD6	
	AE6	
	F7	
	F10	
	AE10	
	F11	
	AE11	
	F13	
	F14	
	AE14	
	AF14	
	W26	
	AF15	
	AE17	
	AC25	
	AE18	
	F23	
	F24	
	AE24	
	F25	
	M25	
	N25	
	W25	
	V25	
VSS	G7	
	G8	
	G9	
	G10	
	G11	
	G12	
	G13	
	G14	
	G15	
	G16	
	G17	
	G18	
	G19	
	G20	
	G21	
	G22	
	G23	
	G24	
	H7	
	H8	
	H23	
	H24	
	J7	
	J24	
	K7	
	K24	
	L7	
	L24	
	M7	
	M24	
	N7	
	N24	
	P7	
	P24	
	R7	
	R24	
	T7	
	T24	
	U7	
	U24	
	V7	
	V24	
	W7	
	W24	
	Y7	
	Y24	
	AA7	
	AA24	
	AB7	
	AB24	
	AC7	
	AC8	
	AC23	
	AC24	
	AD7	
	AD8	
	AD9	
	AD10	
	AD11	
	AD12	
	AD13	
	AD14	
	AD15	
	AD16	
	AD17	
	AD18	
	AD19	
	AD20	
	AD21	
	AD22	
	AD23	

NO STUFF R384 10K 5% 1/16W MF 402
NO STUFF R387 10K 5% 1/16W MF 402
NO STUFF R386 10K 5% 1/16W MF 402
NO STUFF R382 10K 5% 1/16W MF 402
NO STUFF R383 10K 5% 1/16W MF 402
NO STUFF R385 10K 5% 1/16W MF 402
NO STUFF R381 10K 5% 1/16W MF 402

(GPIO0)	ATI_AGP_FBSKEW<0>
(GPIO1)	ATI_AGP_FBSKEW<1>
(GPIO2)	ATI_X1CLK_SKEW<0>
(GPIO3)	ATI_X1CLK_SKEW<1>
(GPIO4)	ATI_BUS_CFG<0>
(GPIO5)	ATI_BUS_CFG<1>
(GPIO6)	ATI_BUS_CFG<2>

NO STUFF R393 10K 5% 1/16W MF 402
NO STUFF R396 10K 5% 1/16W MF 402
NO STUFF R395 10K 5% 1/16W MF 402
NO STUFF R391 10K 5% 1/16W MF 402
NO STUFF R392 10K 5% 1/16W MF 402
NO STUFF R394 10K 5% 1/16W MF 402
NO STUFF R390 10K 5% 1/16W MF 402

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11487501	3	RES,MTL FILM,1/16W,75OHM,0402	R346,R342,R341	?

+PBUS
+5V_MAIN
R559 100K 5% 1/16W MF 402
R556 100K 5% 1/16W MF 402
DP7 BAS16TW SOT-363 — GPU_VCORE_PWR_SEQ
DP7 BAS16TW SOT-363 — SLEEP_L
DP7 BAS16TW SOT-363 — DCDC_EN
R558 10K 5% 1/16W MF 402 — GPU_VCORE_SEQ_L
Q51 2N3904 SM
GPU_VCORE_SEQ_L
Q52 2N3904 SM
R555 33K 5% 1/16W MF 402

R343 0 5% 1/16W MF 402
NO STUFF R352 63.4K 1% 1/16W MF 402
C466 4.7uF 20% 10V CERM 1206 — 1778_GND
R357 100K 5% 1/16W MF 402 — 1778_SHDN_L
R339 20K 1% 1/16W MF 402 — 1778_ITH_RC
C455 470pF 10% 50V CERM 402
C465 220pF 5% 25V CERM 402
NO STUFF R344 0 5% 1/16W MF 402
NO STUFF R353 0 5% 1/16W MF 402
C480 0.1uF 20% 10V CERM 402

R327 1M 5% 1/16W MF 402
R331 2.4K 1% 1/16W MF 603
R326 576K 1% 1/16W MF 402
C431 0.1uF 20% 25V CERM 603

U32 LTC1778 SSOP — EXT_INT_VIN, VCC, VCC
RUN/SS, ITH, VRNG, FCB, PGOOD, SGND, PGND
ION, BOOST, TG, SW, BG, VFB

D12 1N914 SOT23
R358 2.2 5% 1/16W MF 603 — 1778_BST_RC
C481 0.1uF 20% 25V CERM 603
C838 0.001uF 20% 50V CERM 402
OMIT XW6 SM

CRITICAL Q48 SI7860DP SO-8-PWRPK
CRITICAL Q49 IRF7832 SM SO-8
C706 4.7uF 20% 25V CERM 1206
C708 4.7uF 20% 25V CERM 1206
CRITICAL L64 2.1uH-11A SM
D29 MBRS130LT3

CRITICAL C704 22uF 20% 10V CERM 1210
CRITICAL C705 330uF 6.3V SANY CASE-D4
CRITICAL C707 330uF 20% 6.3V SANY CASE-D4
CRITICAL C711 330uF 20% 6.3V SANY CASE-D4
GPU_PWRMSR R549 10K 5% 1/16W MF 402 — GPU_VCORE_CNTL
NO STUFF C712 0.1uF 20% 10V CERM 402

R329 4.99K 1% 1/16W MF 402
GPU_PWRMSR R328 18.2K 1% 1/16W MF 402
GPU_PWRMSR R330 20K 1% 1/16W MF 402
GPU_PWRMSR R361 1.82K 1% 1/16W MF 402
R786 100K 5% 1/16W MF 402
GPU_PWRMSR C846 0.1uF 20% 10V CERM 402
Q25 2N7002DW SOT-363 — GPU_VCORE_CNTL_RC
Q25 2N7002DW SOT-363 — HIGH_VCORE

GPU VCORE SUPPLY

WHEN VCORE_CNTL HIGH => 1.2V
1.2V = 0.8V *(1 + R329 / (R328//R330))
WHEN VCORE_CNTL LOW => 1.0V
1.0V = 0.8V *(1 + R329 / R330)

M11 CORE PWR/LVDS/TMDS

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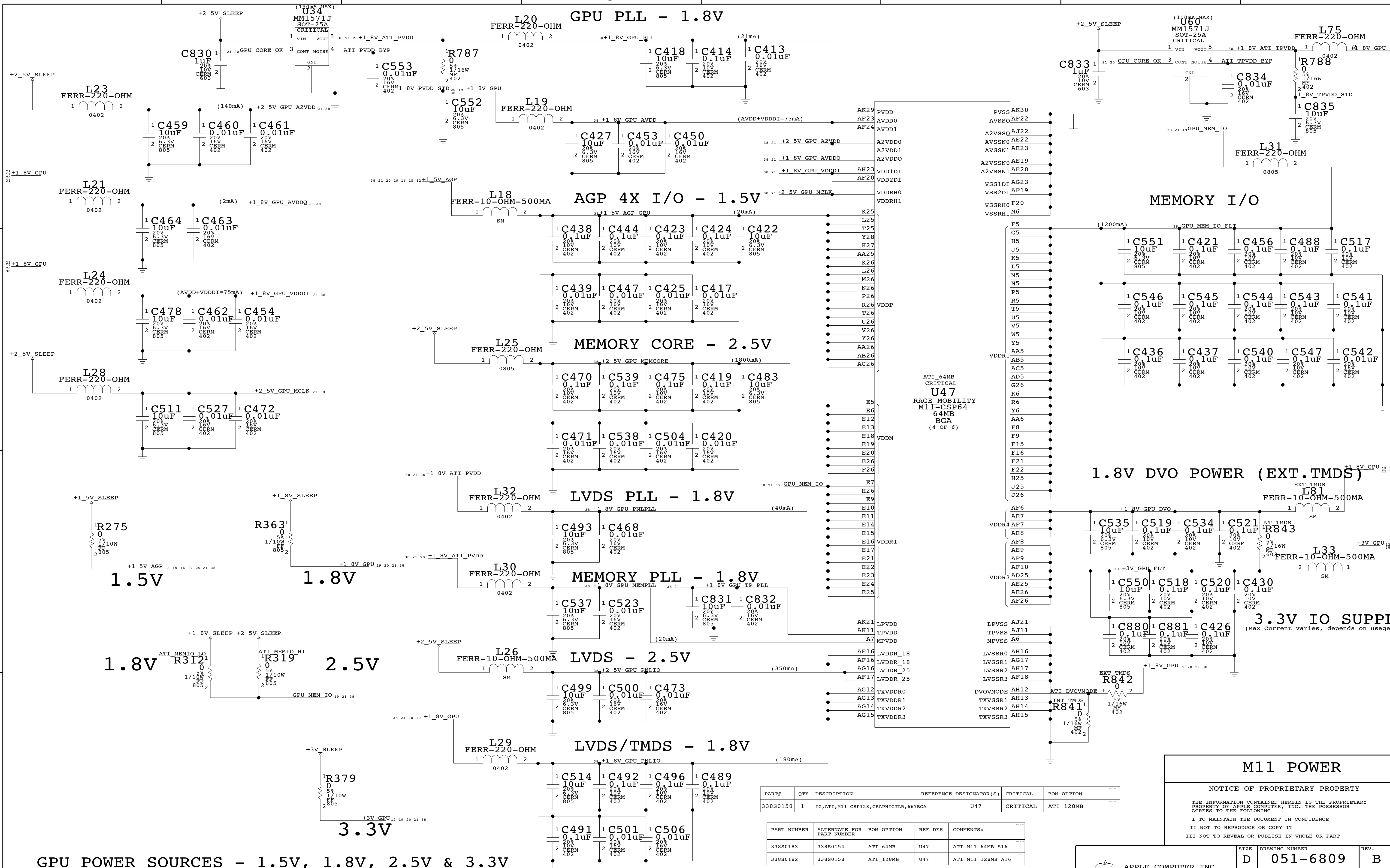
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6809	B
SCALE: NONE	SHT 20 OF 44	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0158	1	IC,ATI,M11-CSP128,GRAPHICTLR,667BGA	U47	CRITICAL	ATI_128MB

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0183	338S0154	ATI_64MB	U47	ATI M11 64MB A16
338S0182	338S0158	ATI_128MB	U47	ATI M11 128MB A16

M11 POWER

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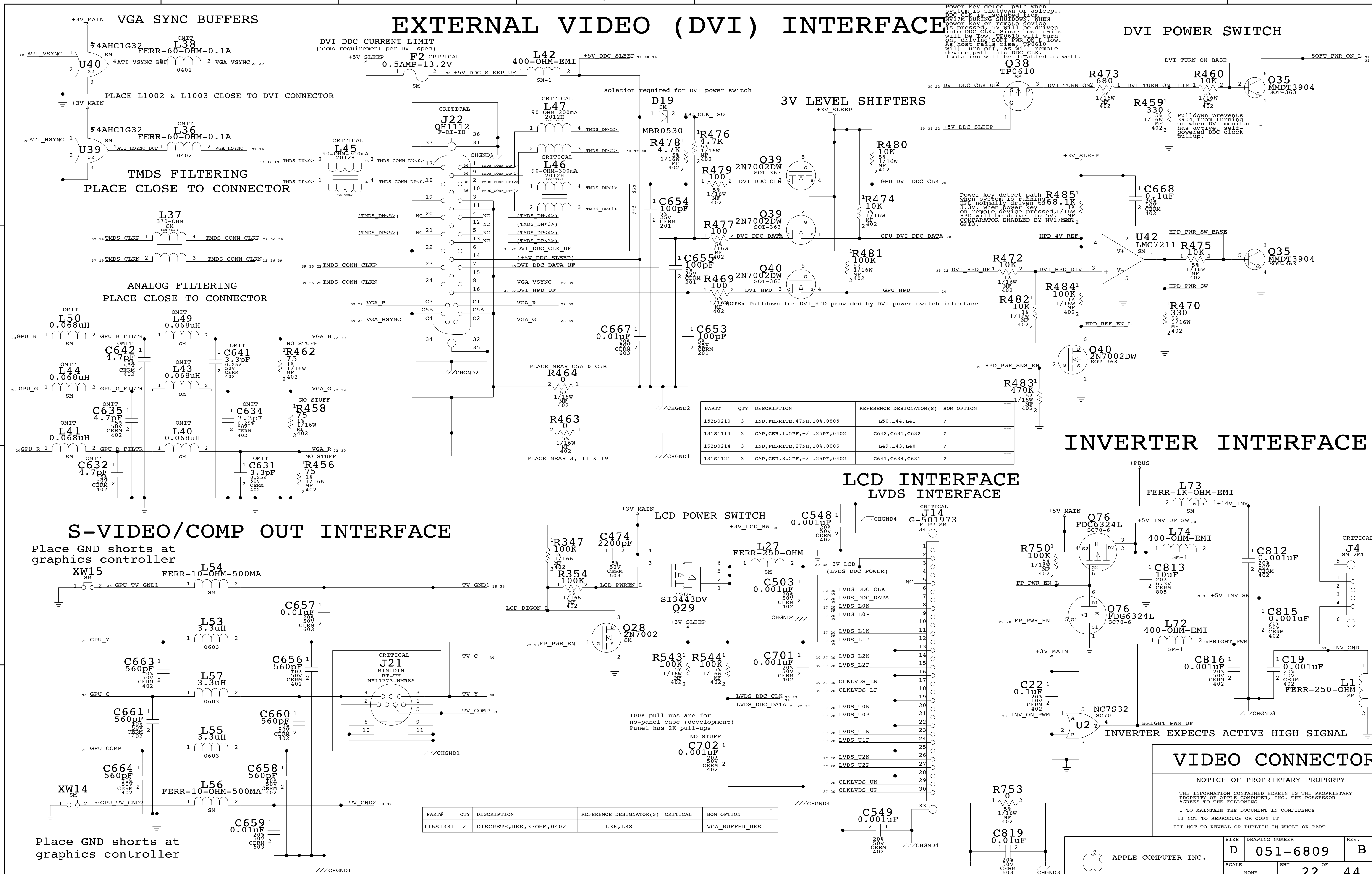
SIZE D | DRAWING NUMBER 051-6809 | REV. B

SCALE NONE | SHT 21 OF 44

EXTERNAL VIDEO (DVI) INTERFACE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
152S0210	3	IND,FERRITE,47NH,10%,0805	L50,L44,L41	?
131S1114	3	CAP,CER,1.5PF,+/-.25PF,0402	C642,C635,C632	?
152S0214	3	IND,FERRITE,27NH,10%,0805	L49,L43,L40	?
131S1121	3	CAP,CER,8.2PF,+/-.25PF,0402	C641,C634,C631	?

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S1331	2	DISCRETE,RES,33OHM,0402	L36,L38		VGA_BUFFER_RES

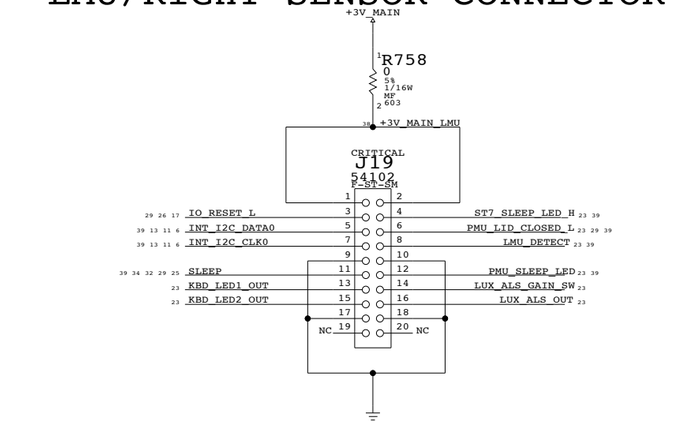
VIDEO CONNECTORS

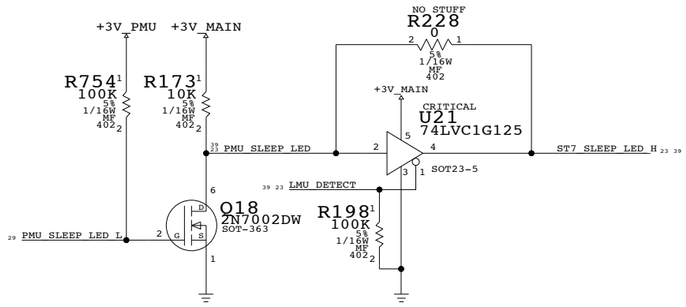
APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6809 | REV. B

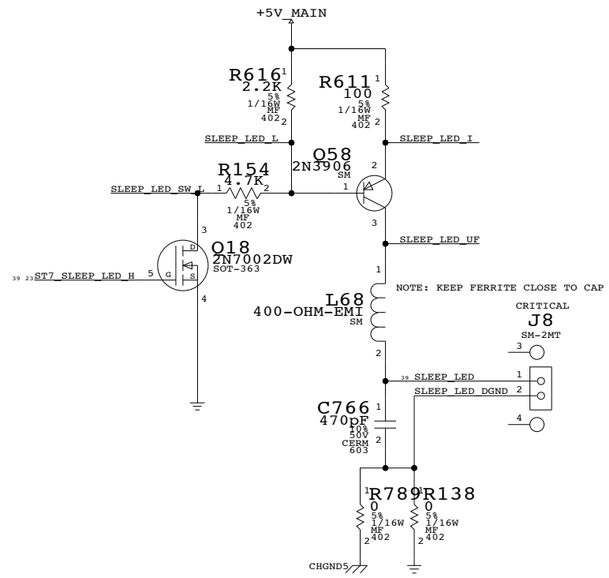
SCALE NONE | SHT 22 OF 44

LMU/RIGHT SENSOR CONNECTOR



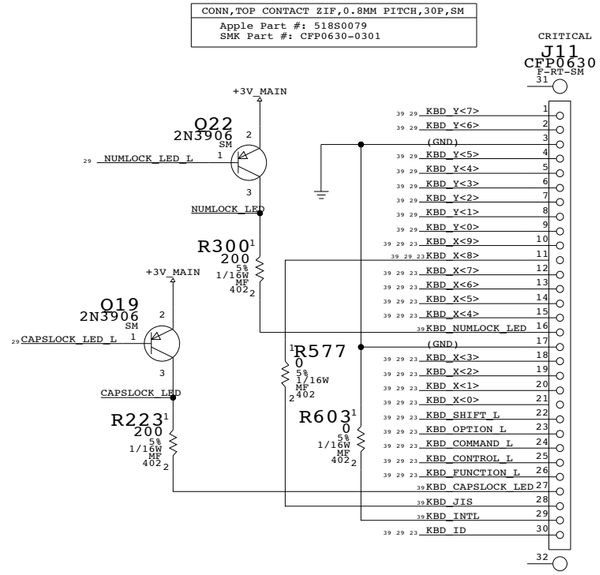


SLEEP LED

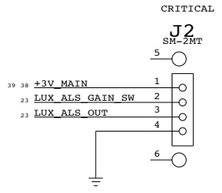


TOP CONTACT ZIF KEYBOARD CONN

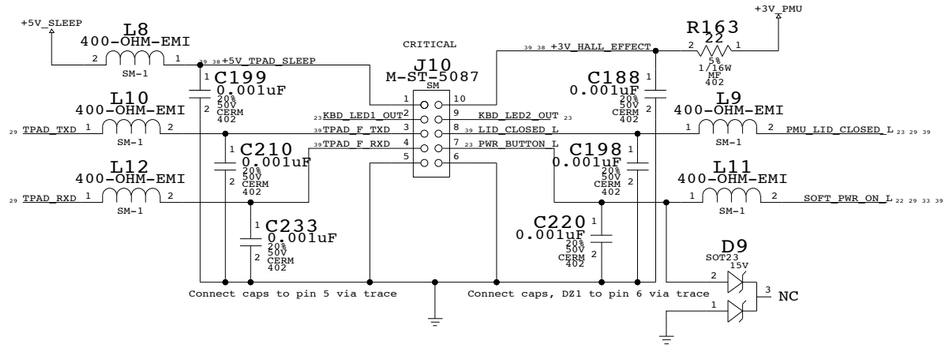
CONN,TOP CONTACT ZIF,0.8MM PITCH,30P,SM
Apple Part #: 518S0079
SMK Part #: CFP0630-0301



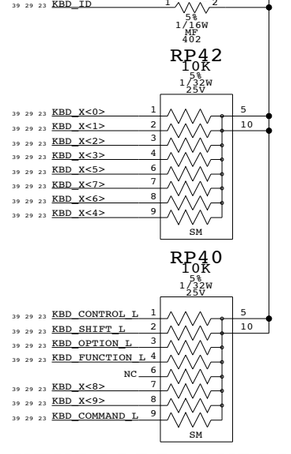
LEFT LIGHT SENSOR CONNECTOR



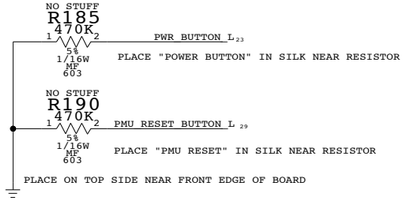
TRACKPAD/PWR BTN CONN



KEYBOARD PULLUPS



DEBUG HELPERS



KEYBOARD/TPAD/SLEEP LED

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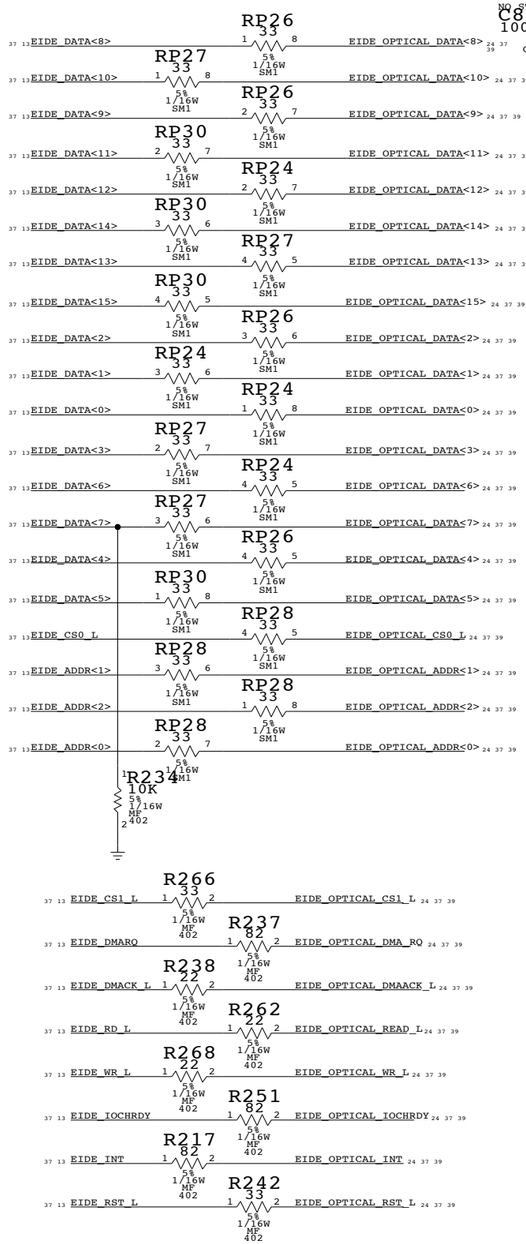
SIZE	DRAWING NUMBER	REV.
D	051-6809	B

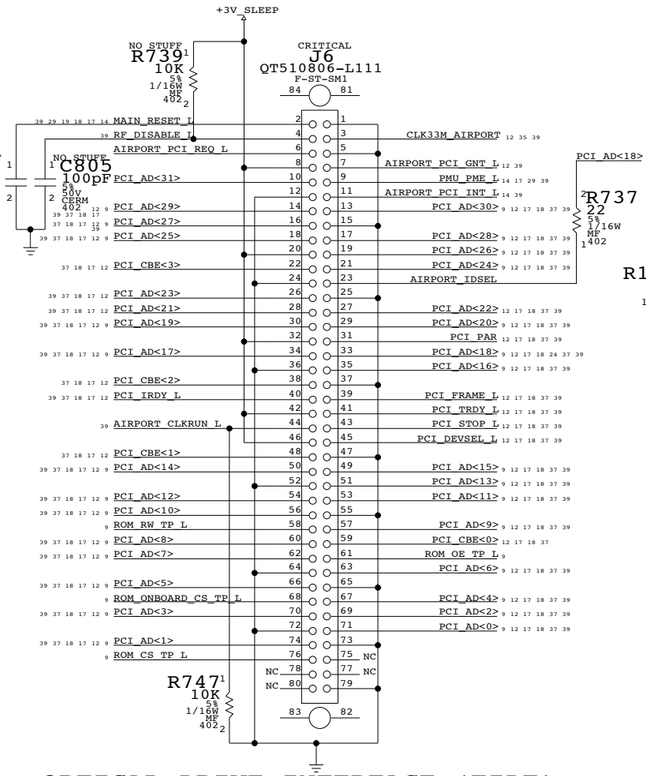
SCALE	SHT	OF
NONE	23	44

WIRELESS INTERFACE

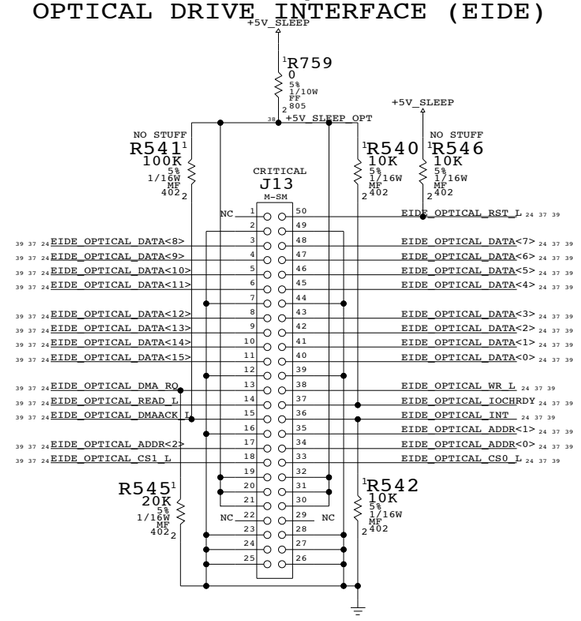
EIDE SERIES TERMINATION

PLACE TERMINATORS NEAR INTREPID



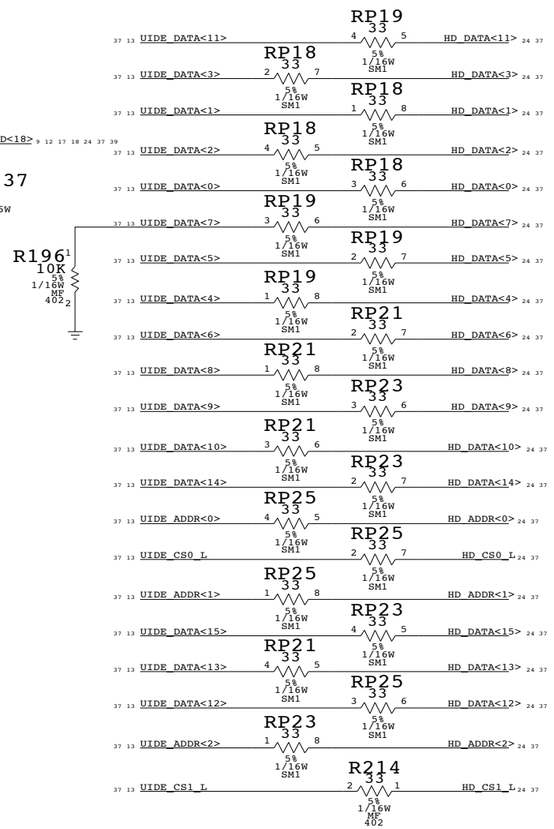


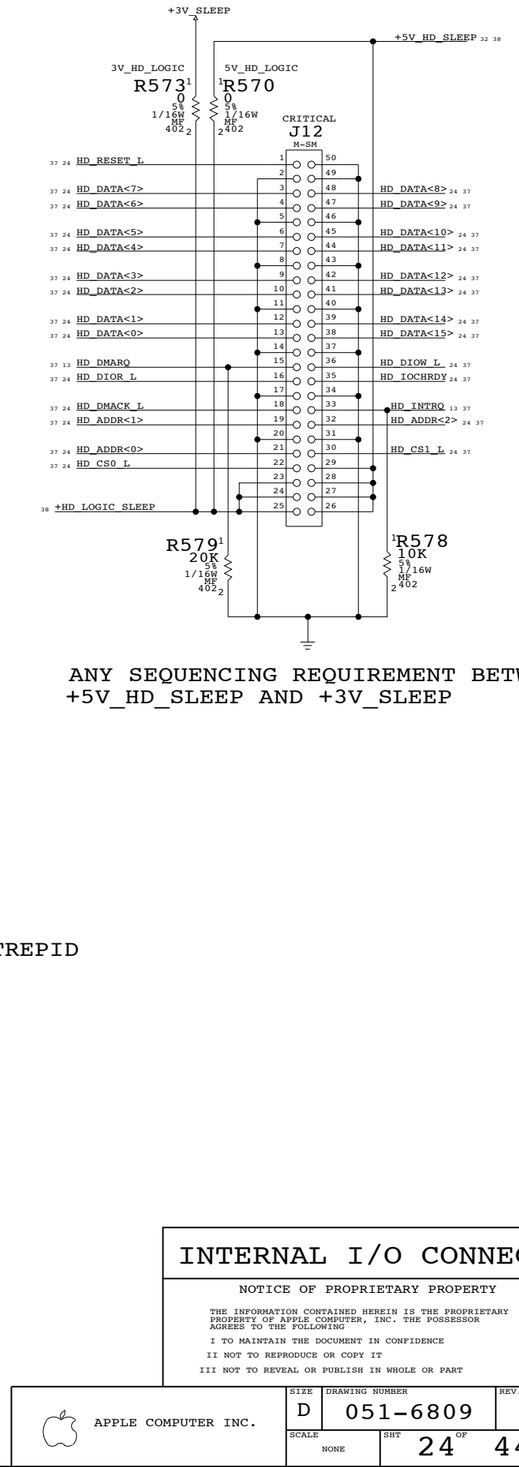
OPTICAL DRIVE INTERFACE (EIDE)



HARD DRIVE INTERFACE (UATA100)

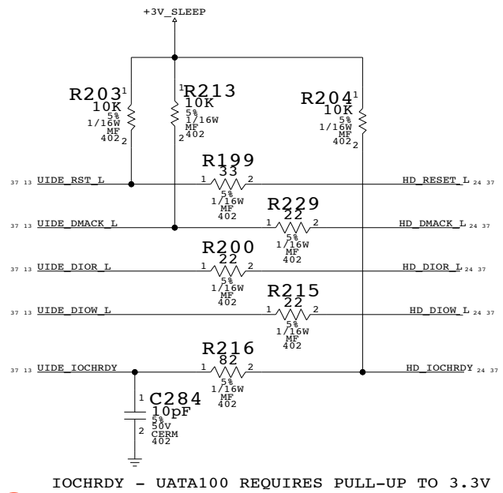
PLACE SERIES R CLOSE TO INTERPID





ANY SEQUENCING REQUIREMENT BETWEEN +5V_HD_SLEEP AND +3V_SLEEP

PLACE PULLUP RESISTORS CLOSE TO INTREPID



IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V

INTERNAL I/O CONNECTORS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6809	B
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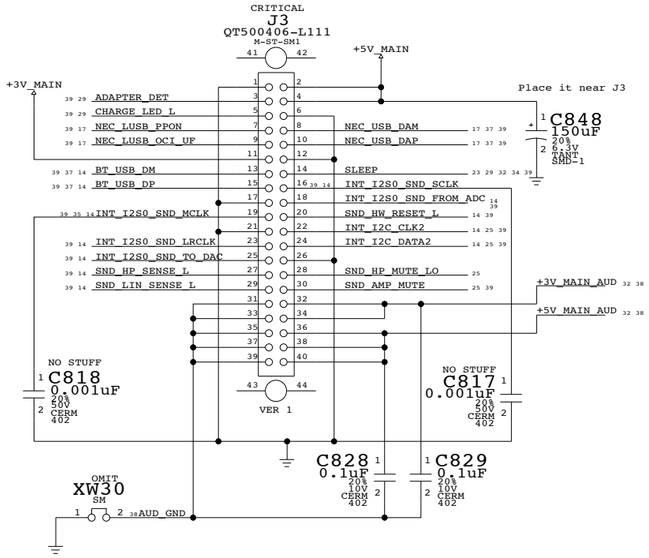
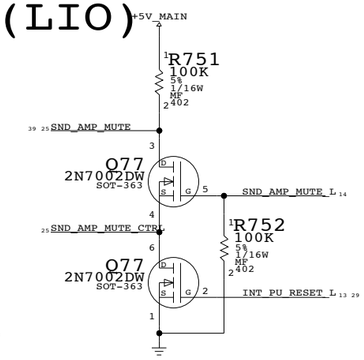
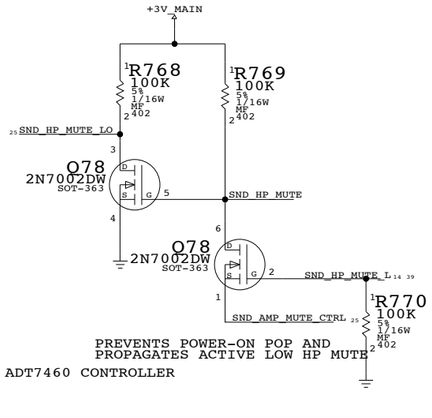
LEFT I/O & AUDIO BOARD (LIO)



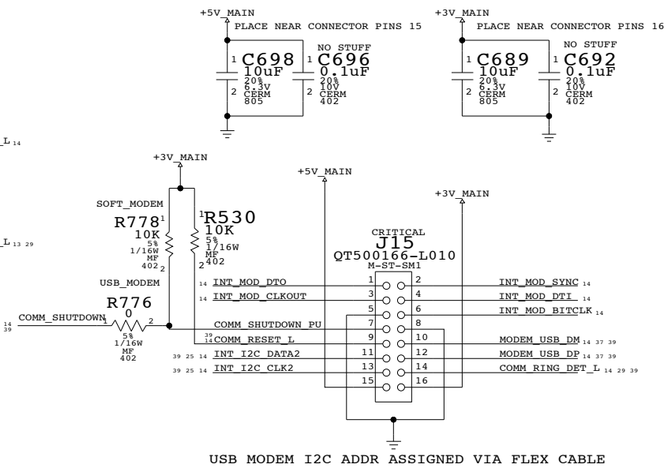


PREVENTS POWER-ON POP AND GENERATES ACTIVE HIGH SPKR MUTE



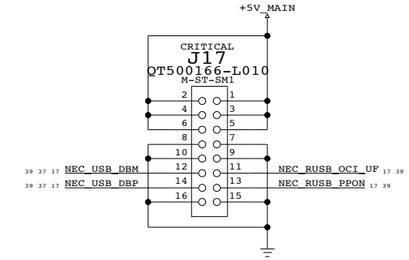
PREVENTS POWER-ON POP AND PROPAGATES ACTIVE LOW HP MUTE

USB MODEM/SOFT MODEM

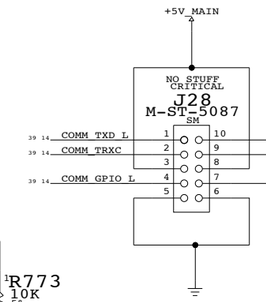


USB MODEM I2C ADDR ASSIGNED VIA FLEX CABLE

RIGHT USB BOARD

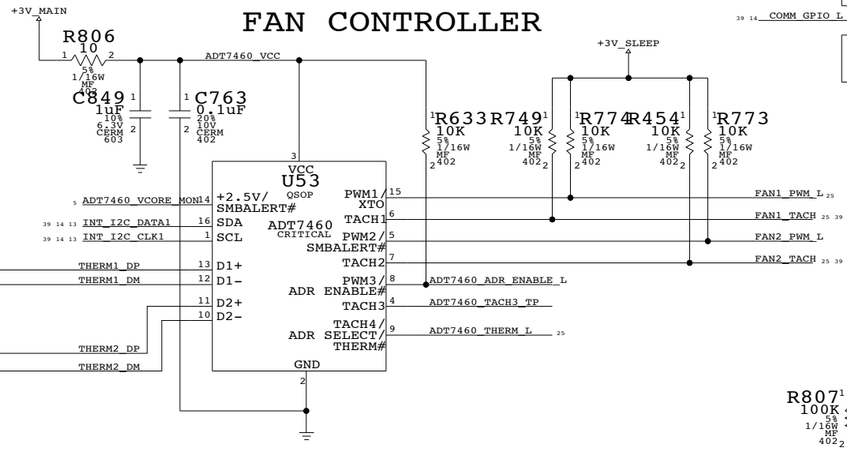


SERIAL DEBUG INTERFACE

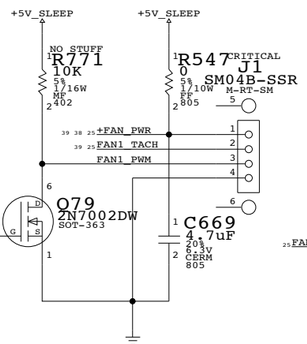


FAN INTERFACE

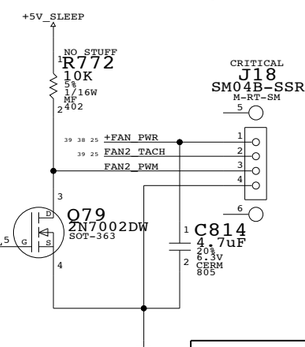
FAN CONTROLLER

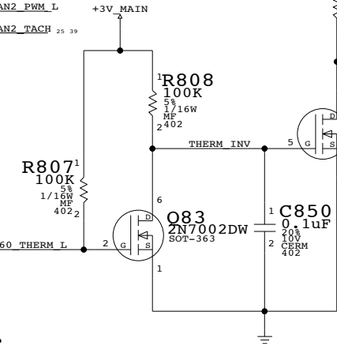


CPU FAN

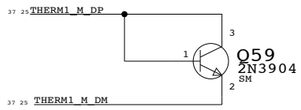


GPU FAN

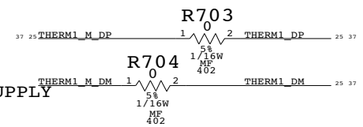




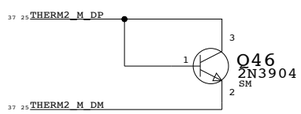
PLACE CLOSE TO CPU
MAIN1

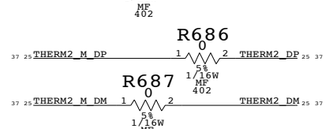


KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

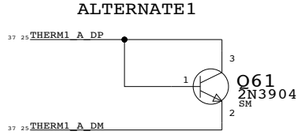


PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY
MAIN2



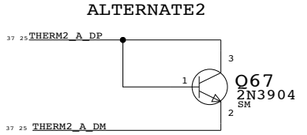


PLACE UNDERNEATH UPPER RAM
ALTERNATE1



KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

PLACE CLOSE TO BATTERY CHARGER/VCORE
ALTERNATE2



FAN/MODEM/SOUND/BACKUP BATT.

APPLE COMPUTER INC.

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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0223	338S0079	?	U43	ALT PART

Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

PLACE ALL SERIES RES CLOSE TO PHY

R423 0 5% 1/16W MF 402 — CLKENET_LINK_TX → CLKENET_PHY_TX
R421 0 5% 1/16W MF 402 — CLKENET_LINK_RX → CLKENET_PHY_RX
R445 0 5% 1/16W MF 402 — CLKENET_LINK_GBE_REF → CLKENET_PHY_GBE_REF

C851 10pF 5% 50V CERM 402 (NO STUFF)
C852 10pF 5% 50V CERM 402
Keep C851 & C852 Stubs short

CRITICAL
U43
88E1111
BCC

TX_CLK	4	
RX_CLK	2	
125CLK	22	
TXD0	11	ENET_PHY_TXD<0>
TXD1	12	ENET_PHY_TXD<1>
TXD2	14	ENET_PHY_TXD<2>
TXD3	16	ENET_PHY_TXD<3>
TXD4	17	ENET_PHY_TXD<4>
TXD5	18	ENET_PHY_TXD<5>
TXD6	19	ENET_PHY_TXD<6>
TXD7	20	ENET_PHY_TXD<7>
TX_EN	9	ENET_PHY_TX_EN
TX_ER	7	ENET_PHY_TX_ER
GTX_CLK	8	CLKENET_PHY_GTX
RXD0	95	ENET_LINK_RXD<0>
RXD1	92	ENET_LINK_RXD<1>
RXD2	93	ENET_LINK_RXD<2>
RXD3	91	ENET_LINK_RXD<3>
RXD4	90	ENET_LINK_RXD<4>
RXD5	89	ENET_LINK_RXD<5>
RXD6	87	ENET_LINK_RXD<6>
RXD7	86	ENET_LINK_RXD<7>
RX_DV	94	ENET_RX_DV
RX_ER	3	ENET_RX_ER
CRS	84	ENET_CRS
COL	83	ENET_COL
MDC	25	ENET_MDC
MDIO	24	ENET_MDIO
INT-/INT+	23	ENET_ENERGY_DET
RESET	28	ENET_RST_L
COMA	27	ENET_COMA
S_IN+	82	NC
S_IN-	81	NC
S_OUT+	77	NC
S_OUT-	75	NC
S_CLK+	79	NC
S_CLK-	80	NC
HSDAC+	37	ENET_HSDACP
HSDAC-	38	ENET_HSDACM
XTAL1	55	CLK25M_ENET_XIN
XTAL2	54	CLK25M_ENET_XOUT
VSSC	53	ENET_VSSC
GND	97	

CTRL10	51	NC
DVDD	1, 6, 10, 15, 57, 62, 67, 71, 85	
VDDO	5, 21, 88, 96	
VDDOH	52, 66, 72	
VDDOX	26, 48	
AVDD	32, 35, 36, 40, 45, 78	
MDI0+	29	MDI_P<0>
MDI0-	31	MDI_M<0>
MDI1+	33	MDI_P<1>
MDI1-	34	MDI_M<1>
MDI2+	39	MDI_P<2>
MDI2-	41	MDI_M<2>
MDI3+	42	MDI_P<3>
MDI3-	43	MDI_M<3>
LED_LINK10	76	LED_LINK10
LED_LINK100	74	LED_LINK100
LED_LINK1000	73 NC	
LED_DUPLEX	70 NC	
LED_RX	69	LED_RX_SPN
LED_TX	68 NC	
CONFIG0	65	(000)
CONFIG1	64	(000)
CONFIG2	63	(111)
CONFIG3	61	(110)
CONFIG4	60	(111)
CONFIG5	59	(101)
CONFIG6	58	(000)
TDI	44	
TDO	50	JTAG_ASIC_TDO_TP
TCK	49	JTAG_ASIC_TCK
TMS	46	JTAG_ASIC_TMS
TRST	47	JTAG_ASIC_TRST_L
RSET	30	ENET_RSET
SEL_OSC	56 NC	
SEL_2.5V	13	

SEE CONFIG TABLES (BELOW)

+3V_MAIN
C680 10uF 20% 6.3V CERM 805
NO STUFF R513 0 5% 1/16W MF 402
3405_MODE
R507 0 5% 1/16W MF 402
U45 LTC3405 SOT23-6: VIN, RUN, MODE, GND, SW, VFB
LTC3405_SW
CRITICAL L60 3.3uH SM1
R506 665K 1% 1/16W MF 402 R2A
C675 22PF 5% 50V CERM 402
R504 49.9K 1% 1/16W MF 402 R2B
3405_VFB
C674 10uF 20% 6.3V CERM 805
+1_0V_MARVELL
R503 182K 1% 1/16W MF 402 R1

VOUT = 0.8V*(1+R2EQV/R1)
R2EQV = R2A||R2B

PLACE CAPS (IN ORDER) ON PINS 1, 6, 10/15, 57/62, 67/71, 85
C594 0.1uF 20% 10V CERM 402
C601 0.01uF 20% 16V CERM 402
C608 0.1uF 20% 10V CERM 402
C619 0.01uF 20% 16V CERM 402
C603 0.1uF 20% 10V CERM 402
C599 0.01uF 20% 16V CERM 402

PLACE CAPS (IN ORDER) ON PINS 5, 21/26, 48/52, 66/72, 88, 96
+2_5V_MARVELL
C597 0.1uF 20% 10V CERM 402
C612 0.01uF 20% 16V CERM 402
C623 0.1uF 20% 10V CERM 402
C600 0.01uF 20% 16V CERM 402
C598 0.1uF 20% 10V CERM 402
C595 10uF 20% 6.3V CERM 805

+2_5V_MARVELL
R442 0 5% 1/16W MF 603
PLACE CAPS AT CONNECTOR PINS 5 & 6
C646 0.1uF 20% 10V CERM 402
C648 0.1uF 20% 10V CERM 402
C645 0.1uF 20% 10V CERM 402
C647 0.1uF 20% 10V CERM 402

+2_5V_MARVELL AVDD
L35 FERR-EMI-600-OHM SM
PLACE CAPS (IN ORDER) ON PINS 32/35, 36/40, 45 & 78
C614 0.1uF 20% 10V CERM 402
C616 0.01uF 20% 16V CERM 402
C618 0.1uF 20% 10V CERM 402
C602 0.01uF 20% 16V CERM 402
C592 10uF 20% 6.3V CERM 805

PLACE RESISTORS CLOSE TO PHY
R433 49.9 1% 1/16W MF 402 MDI0_PD
R435 49.9 1% 1/16W MF 402 MDI1_PD
R437 49.9 1% 1/16W MF 402 MDI2_PD
R439 49.9 1% 1/16W MF 402 MDI3_PD
R434 49.9 1% 1/16W MF 402
R436 49.9 1% 1/16W MF 402
R438 49.9 1% 1/16W MF 402
R440 49.9 1% 1/16W MF 402
C622 0.01uF 20% 16V CERM 402
C613 0.01uF 20% 16V CERM 402
C615 0.01uF 20% 16V CERM 402
C617 0.01uF 20% 16V CERM 402

CRITICAL
J23
MJ-R0016
F-RT-TH

PRIMARY
13
11
5 ENET_CTAP
6 ENET_CTAP
1 MDI_0+
2 MDI_0-
3 MDI_1+
4 MDI_1-
7 MDI_2+
8 MDI_2-
9 MDI_3+
10 MDI_3-
12
14
RJ45 CHIP SIDE
CHGND1

1CT:1CT
75 OHM
SECONDARY
J1 J2 J3 J4 J5 J6 J7 J8
RJ45 CABLE SIDE
SHIELD
1000PF, 2000V

PLACES PHY IN "COMA" MODE WHEN ASLEEP ON BATTERY (SAVES POWER)
Q32 2N7002DW SOT-363
AC_IN
SLEEP_L_LS5
D15 1N914 SOT23
IO_RESET_L
INT_ENET_RST_L1
C611 2.2uF 20% 10V CERM 805

PUT CRYSTAL CIRCUIT CLOSE TO PHY
NO STUFF R425 20K 5% 1/16W MF 402
R441 0 5% 1/16W MF 402
CRITICAL Y5 SM-3 25.0000M
C604 27PF 5% 50V CERM 402
C624 27PF 5% 50V CERM 402
Y6 LOAD CAPACITANCE IS 16PF
NO STUFF R424 49.9 1% 1/16W MF 402
NO STUFF R429 49.9 1% 1/16W MF 402
R428 10K 5% 1/16W MF 402
R427 4.99K 1% 1/16W MF 402
R431 10K 5% 1/16W MF 402
R430 10K 5% 1/16W MF 402
R432 1.5K 5% 1/16W MF 402
R422 1K 5% 1/16W MF 402

CONFIG DEFINITIONS	
PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS			
PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

MARVELL 88E1111

10/100/1000 ETHERNET

APPLE COMPUTER INC.

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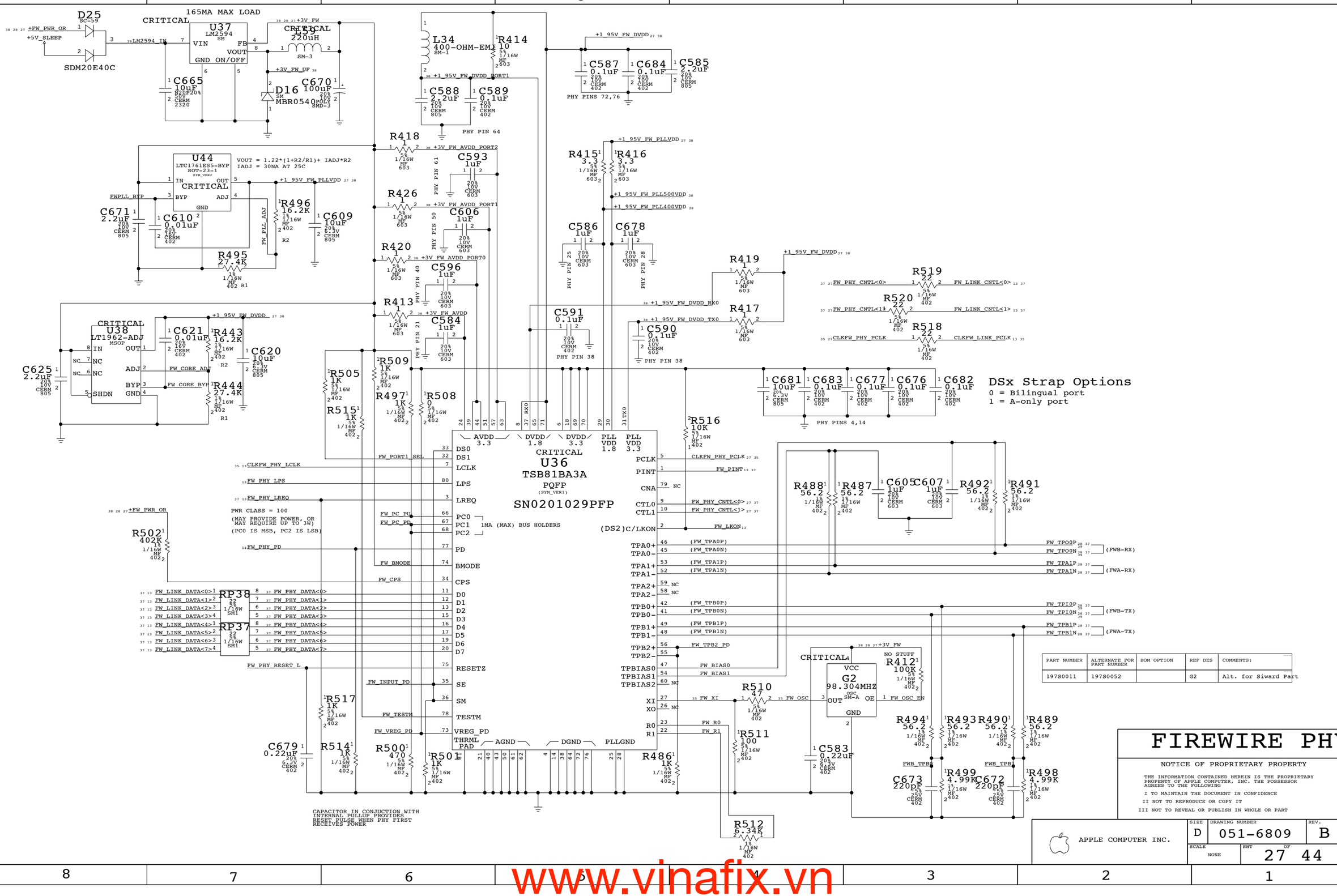
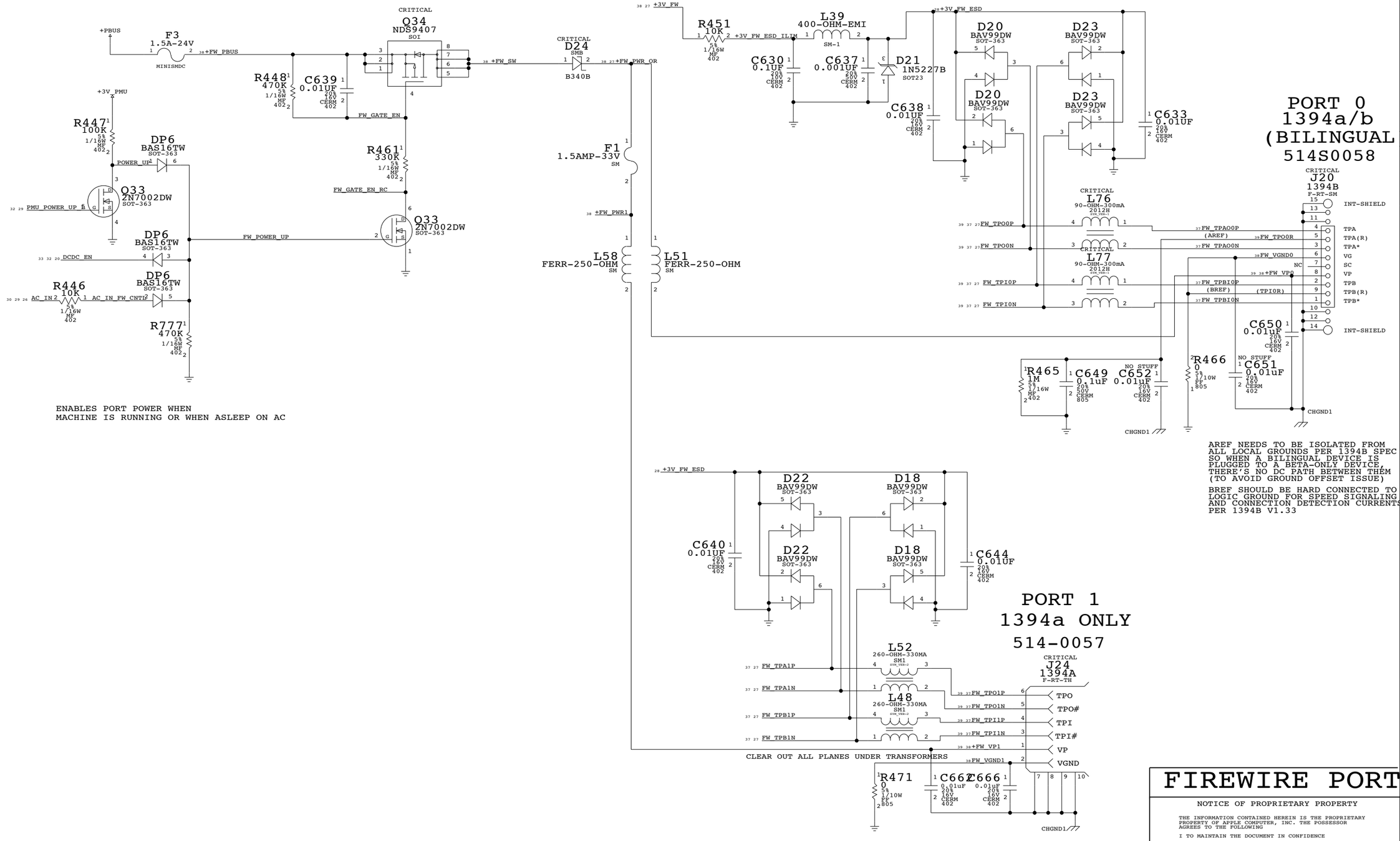


PORT POWER SWITCH



ENABLES PORT POWER WHEN
MACHINE IS RUNNING OR WHEN ASLEEP ON AC

PORT 0
1394a/b
(BILINGUAL)
514S0058

AREF NEEDS TO BE ISOLATED FROM ALL LOCAL GROUNDS PER 1394B SPEC SO WHEN A BILINGUAL DEVICE IS PLUGGED TO A BETA-ONLY DEVICE, THERE'S NO DC PATH BETWEEN THEM (TO AVOID GROUND OFFSET ISSUE)

BREF SHOULD BE HARD CONNECTED TO LOGIC GROUND FOR SPEED SIGNALING AND CONNECTION DETECTION CURRENTS PER 1394B V1.33

PORT 1
1394a ONLY
514-0057

CLEAR OUT ALL PLANES UNDER TRANSFORMERS

FIREWIRE PORTS

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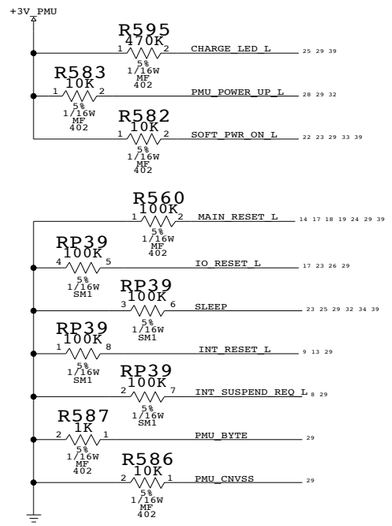
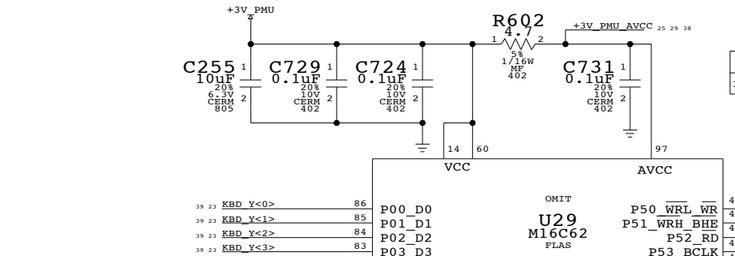
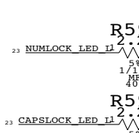
D	051-6809	B
SCALE: NONE	SHT 28 OF 44	





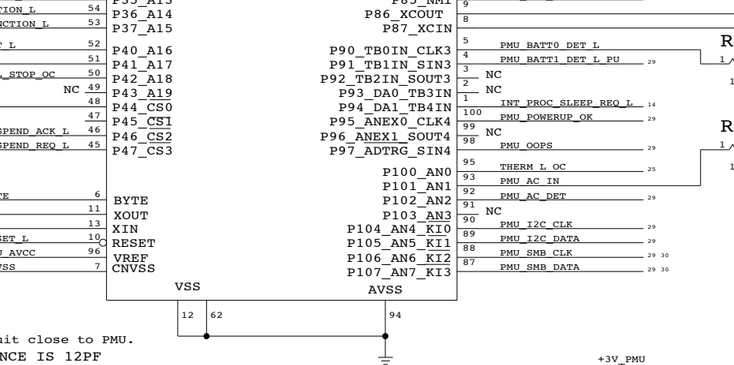


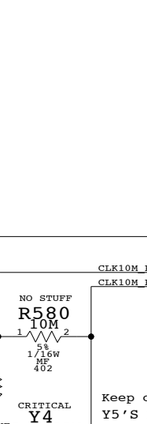
OMIT
U29
M16C62
FLAS

P50_WRL_WR
P51_WRH_BHE
P52_RD
P53_BCLK
P54_HLDA
P55_HOLD
P56_ALE
P57_RDY_CLKOUT
P60_CTS0_RTS0
P61_CLK0
P62_RXD0
P63_TXD0
P64_CTS1_RTS1_CTS0_CLKS1
P65_CLK1
P66_RXD1
P67_TXD1
P70_TXD2_SDA_TA0OUT
P71_RXD2_SCL_TA0IN_TB5IN
P72_CLK2_TA1OUT_V
P73_CTS2_RTS2_TA1IN_V
P74_TA2OUT_W
P75_TA2IN_W
P76_TA3OUT
P77_TA3IN
P80_TA4OUT_U
P81_TA4IN_U
P82_INT0
P83_INT1
P84_INT2
P85_NMI
P86_XCOUT
P87_XCIN
P90_TB0IN_CLK3
P91_TB1IN_SIN3
P92_TB2IN_SOUT3
P93_DA0_TB3IN
P94_DA1_TB4IN
P95_ANEX0_CLK4
P96_ANEX1_SOUT4
P97_ADTRG_SIN4
P100_AN0
P101_AN1
P102_AN2
P103_AN3
P104_AN4_KI0
P105_AN5_KI1
P106_AN6_KI2
P107_AN7_KI3

CPU_VCORE_HI_OC/PMU_AP should have a putldown for coming out of reset. MLB will have a pull-up to +3V_MAIN or +3V_SLEEP, which will act as our putldown since both are off during PMU reset.

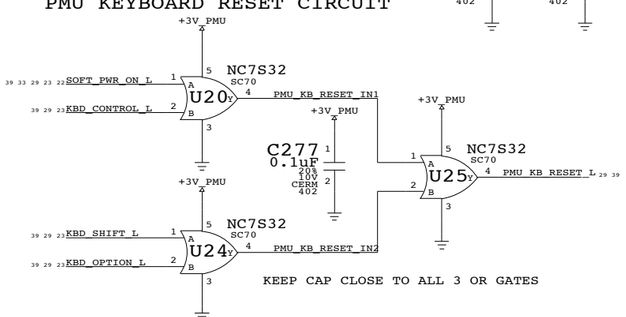
(PMU_AP)
CPU_VCORE_HI_OC
INT_RESET_L
MAIN_RESET_L
NC
PMU_INT_NMI
PMU_EPM
INT_PU_RESET_L
PMU_CPU_HRESET_L
PMU_ACK_L
PMU_CLK
PMU_FROM_INT
PMU_TO_INT
PMU_REQ_L
PMU_LID_CLOSED_L
PMU_RESET_BUTTON_L
PMU_NMI_BUTTON_L
TPAD_RXD
TPAD_TXD
SYSTEM_CLK_EN
CPU_CLK_EN
PMU_CHARGE_V
PMU_CHRG_BATT_0
NC (CHARGE_I)
NC
PMU_SLEEP_LED_L
CPU_SMI_L
POWER_VALID
PMU_PME_L
INT_PEND_PROC_INT
PMU_NMI_L
PMU_BATT0_DET_L
PMU_BATT1_DET_L_PU
NC
NC
INT_PROC_SLEEP_REQ_L
PMU_POWERUP_OK
NC
PMU_OOPS
THERM_L_OC
PMU_AC_IN
PMU_AC_DET
NC
PMU_I2C_CLK
PMU_I2C_DATA
PMU_SMB_CLK
PMU_SMB_DATA



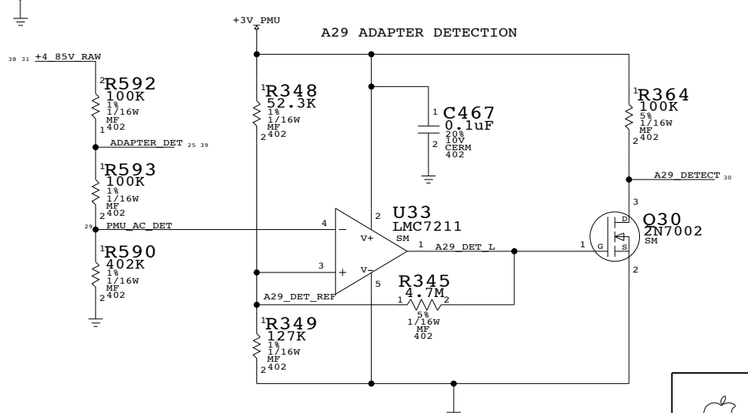


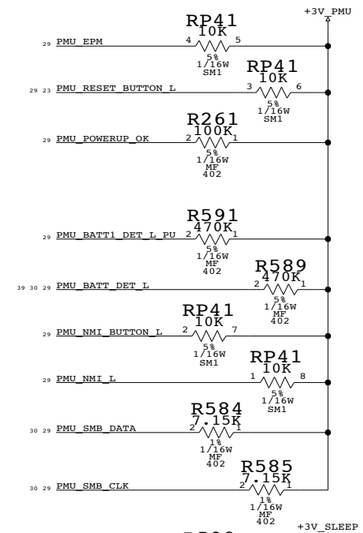
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0604	197S0041		Y4	Alt. for Siward Part

PMU KEYBOARD RESET CIRCUIT



ADAPTER IDs		
ADAPTER	ID RANGE	PIN VOLTAGE
Q11 (65W)	1.65-2.31V	2.007-2.066V
A29 (45W)	2.31-2.97V	2.558-2.661V
AIRLINE	0.33-0.99V	0.589-0.663V





PMU

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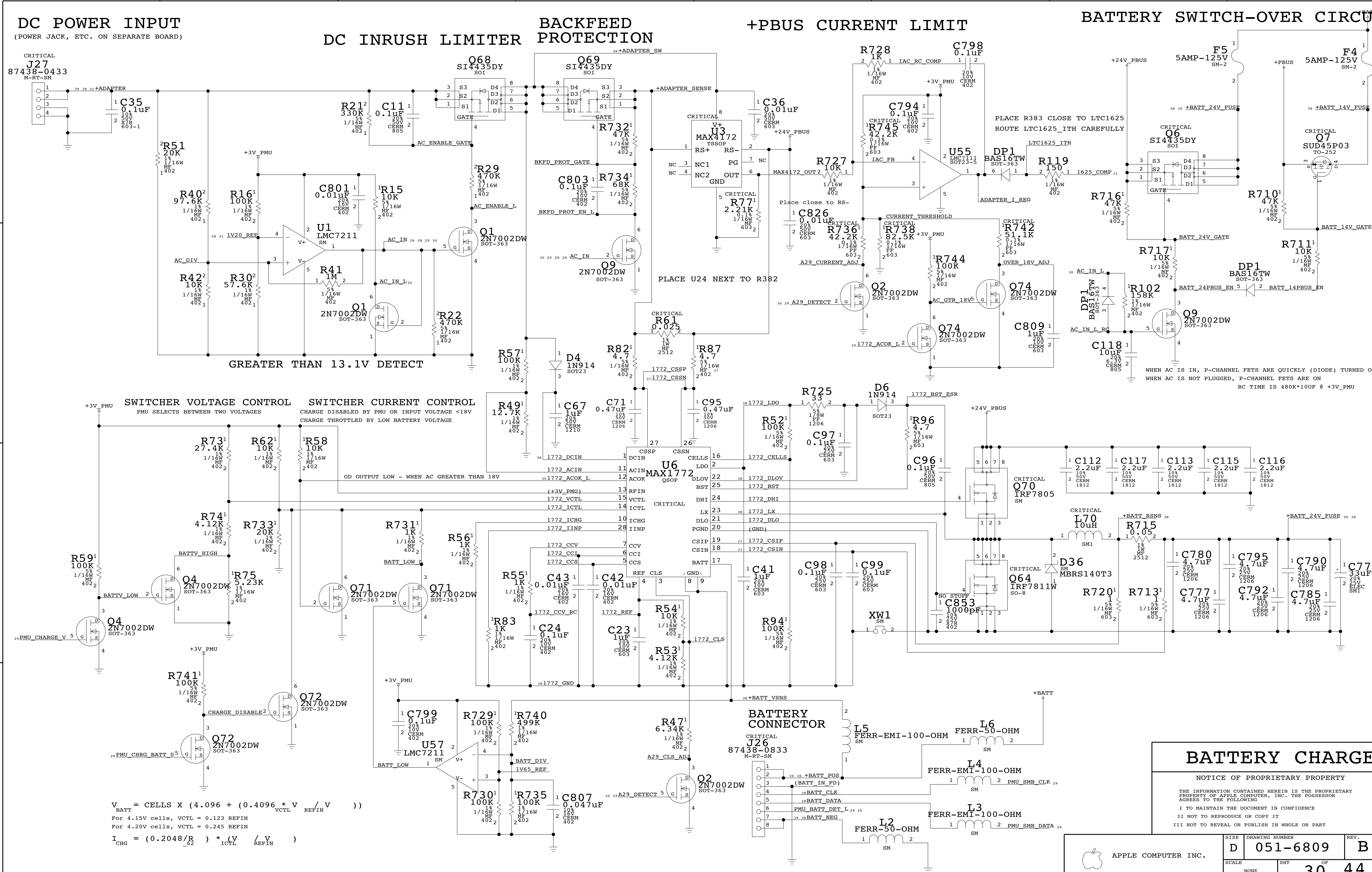
D	051-6809	B
SCALE: NONE	SHT 29 OF 44	



V_{BATT} = CELLS X (4.096 + (0.4096 * V_{VCTL} / V_{REFIN}))

For 4.15V cells, VCTL = 0.123 REFIN

For 4.20V cells, VCTL = 0.245 REFIN

I_{CHG} = (0.2048/R_{62}) * (V_{ICTL} / V_{REFIN})

BATTERY CHARGER

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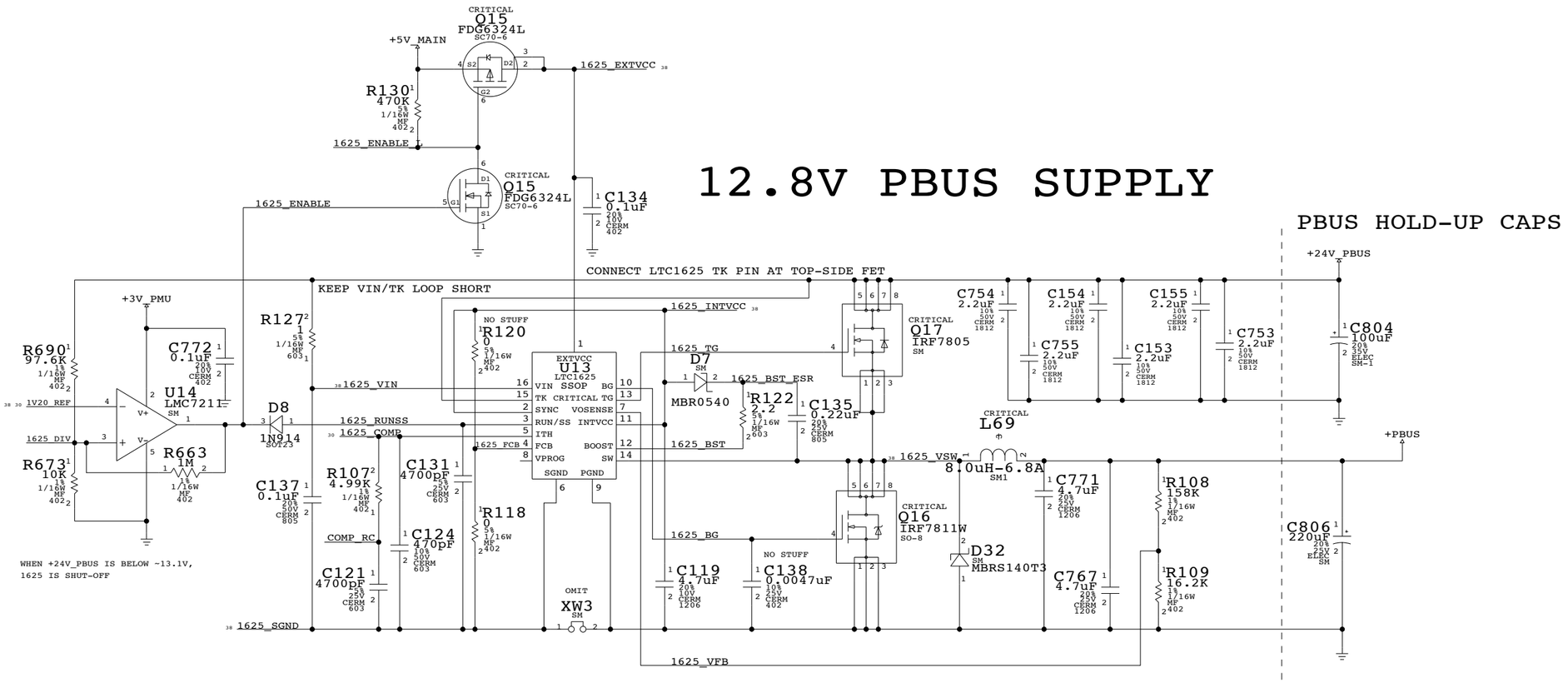
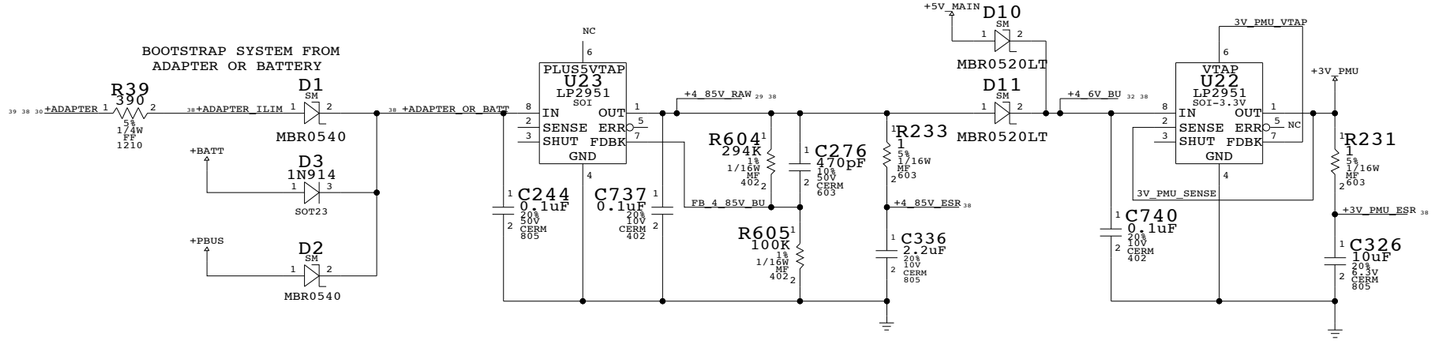
D	051-6809	B
SCALE NONE	SHT 30	OF 44

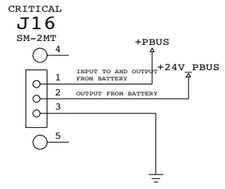
12.8V PBUS SUPPLY



PMU SUPPLY



BACKUP BATTERY



12.8V REGULATOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6809	B
SCALE: NONE	SHT 31 OF 44	

3.3V/5V MAIN SUPPLY

DCDC_EN TRUTH TABLE

PMU_POWER_UP_L	SLEEP	DCDC_EN	DCDC_EN_L	State
0	0	1	0	Run
1 (2.99V)	1	1	0	Sleep
1	0	0	1	Shutdown
+3V_PMU	+3V_PMU	+4_6V_BU	+3V_PMU	VOLTAGE

SLEEP LEVEL SHIFTER (3V -> 5V)

+5V_SLEEP LOADS

1) FAN
2) Headphone amplifier
3) OPTICAL DRIVE
4) DVI
5) TRACKPAD

+3V_SLEEP LOADS

1) CPU PLL CONFIG CONTROL
2) INTREPID - I2C PULLUPS & OSCILLATOR
3) MAP31 - 3V RAIL (IF USING D3COLD)
4) GRAPHIC CHIP SPREAD SPECTRUM CHIP
5) LVDS DDC PULL-UPS
6) DVI LEVEL SHIFTERS & PULLUPS & HPD
7) BOOT BANGER
8) HARD DRIVE (IF USING 3V LOGIC)
9) WIRELESS
10) PMU - I2C PULLUPS

DISTRIBUTE CAPS ALONG TOP EDGE AND FAN CUT-OUT

5V START TO TURN ON ~12.5MS AFTER DCDC_EN_L
3V START TO TURN ON ~25MS AFTER DCDC_EN_L
DIODE WILL ENSURE DCDC_EN_L IS QUICKLY DISCHARGED DURING SHUT-DOWN
POWERDOWN DELAY IS AROUND 4MS-15.6MS

THIS SIGNAL IS OPEN COLLECTOR TO GND WHEN POWER IS NOT GOOD
220PF IS USED TO QUIET NOISE ON PGOOD ONCE INTERNAL OPEN DRAIN IS DISENGAGED

3.3V/5V REGULATOR

APPLE COMPUTER INC.

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VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage
(approx. 7ms delay)

1.250V->0.975V 1.50Ghz
1.200V->0.975V 1.33Ghz
(value without offset)

NOTE: When U15 MUX is removed => NO SW Support,
R794,R795,R796&R797 have to be stuffed

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
126S0036	7	CAP,AL,POLY,8.2uF,20%,16V,V CASE,SMD	C51,C52,C77,C78,C91,C92,C111	CRITICAL	

SEL = 0; Y1=A1
SEL = 1; Y1=B1

Keep trace fat (40-100 mils) and short!!

MAX1717 VID INPUTS ARE 3.3-5V TOLERANT

Note:No stuff R67 to set skip mode of VCore

Connect MAX1717 GND pin 13
to GND at bottom-side FET

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V, HENCE VOFFSET = 2.0V*0.85*(Rb / Ra) AND VCORE = VDAC + VOFFSET.
NOTE: Ra NO STUFFED FOR NO OFFSET CASE

(CPU Vcore value with offset)

1.50Ghz 1.280V->0.990V
1.33Ghz 1.220V->0.990V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S2003	1	RES,MF,1/16W,2K OHM,1%,0402,SMD	R97	?	CPU_BTR
114S5903	1	RES,MF,1/16W,5.9K OHM,1%,0402,SMD	R93	?	CPU_BTR

ROUTE AS DIFFERENTIAL PAIR

OUTPUT VOLTAGE

V_{DAC} D4=0	V_{DAC} D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	A/B_ = Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1
If all pull-ups are >=100K and all
pull-downs are <=1K, A V = B V .

Fmax Test Connections

VCORE SUPPLY

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1.5V/2.5V SWITCHER

M11 Power Shut down Sequencing

+2_5V_SLEEP
XW8 SM
DP4 BAS16TW SOT-363
XW21 SM
+3V_SLEEP
+1_8V_SLEEP
XW10 SM
DP4 BAS16TW SOT-363
+1_5V_SLEEP
XW23 SM
DP4 BAS16TW SOT-363

+1_5V_SLEEP LOADS

1) AGP I/O - IF USING D3COLD
2) MAXBUS I/O - IF 1.5V INTERFACE

+1_5V_MAIN LOADS

1) INTREPID CORE

+2_5V_MAIN LOADS

1) MAP31 - FBCORE/FBIO IF USING D3HOT
2) GIGABIT ETHERNET - AVDDL
3) DDR SODIMMS - CORE/IO
4) DDR MUXES

+2_5V_SLEEP LOADS

1) FBCORE/FBIO IF USING D3COLD

Q53 SI3446DV TSOP
C717 10uF 20% 6.3V CERM 805
C718 1000pF 10% 25V X7R 402
+1_5V_MAIN
+1_5V_SLEEP
1_5V_SLEEP_EN_L
DP3 BAS16TW SOT-363
R117 100K 5% 1/16W MF 402
3V_5V_OK
R177 20 5% 1/16W MF 402
MAX1715_VCC
C195 2.2uF 20% 10V CERM 805
NO STUFF R227 0 5% 1/16W MF 402
NO STUFF R226 0 5% 1/16W MF 402
C194 2.2uF 20% 10V CERM 805
DP3 BAS16TW SOT-363
+5V_MAIN
DP3 BAS16TW SOT-363
R184 330K 1% 1/16W MF 402
DCDC_EN_L
MAX1715_ON_RC
Q10 2N7002 SM
C133 0.01uF 10% 16V CERM 402
DIODE PROVIDE PROVIDE QUICK SHUT-DOWN POWER DOWN DELAY 1.5MS TO 3.5MS
MAX1715_TON
R116 100K 5% 1/16W MF 402
R115 100K 5% 1/16W MF 402
1_5V_SLEEP_EN_L
Q11 2N7002DW SOT-363
SLEEP_L_LS5_INV
SLEEP_L_LS5_NET
R114 100K 5% 1/16W MF 402
Q11 2N7002DW SOT-363
C129 1000pF 10% 25V X7R 402
2_5V_ILIM
1_5V_ILIM
R210 158K 1% 1/16W MF 402
R211 158K 1% 1/16W MF 402
MAX1715_GND
+PBUS
MAX1715_SKIP
U19 MAX1715 QSOP
VCC VDD
ILIM1 ILIM2 ON1 ON2 BST1 DH1 LX1 DL1 TON OUT1 PGOOD REF FB1 AGND
NC_15 NC_23 NC_28 BST2 DH2 LX2 DL2 PGND OUT2 SKIP FB2 THRML
CRITICAL C232 4.7uF 20% 25V CERM 1206
CRITICAL C209 4.7uF 20% 25V CERM 1206
1_5V_BOOST
R171 4.7 5% 1/16W MF 603
2_5V_BST
R170 4.7 5% 1/16W MF 603
2_5V_BOOST
C196 0.1uF 20% 25V CERM 603
CRITICAL C338 4.7uF 20% 25V CERM 1206
CRITICAL C355 4.7uF 20% 25V CERM 1206
C193 0.1uF 20% 25V CERM 603
CRITICAL Q56 IRF7805 SM
CRITICAL Q55 IRF7805 SM
1_5V_DH
2_5V_DH
+1_5V_MAIN
+2_5V_MAIN
MAX1715_GND
MAX1715_REF
1_5V_FB
NO STUFF R221 0 5% 1/16W MF 402
R468 15.4K 1% 1/16W MF 402
R601 10K 1% 1/16W MF 402
C298 1uF 20% 10V CERM 603
R220 0 5% 1/16W MF 402
2_5V_FB
CRITICAL L67 4.7uH SM4
1_5V_LX
2_5V_LX
CRITICAL L65 4.7uH SM4
R212 5.11K 1% 1/16W MF 402
1_5V_FB
R222 10K 1% 1/16W MF 402
D31 MBRS130LT3 SM
CRITICAL Q57 IRF7811W SO-8
NO STUFF C844 0.001uF 20% 50V CERM 402
1_5V_DL
OMIT XW25 SM
2_5V_DL
NO STUFF C845 0.001uF 20% 50V CERM 402
CRITICAL Q54 IRF7811W SO-8
D30 MBRS130LT3 SM
C738 10uF 20% 6.3V CERM 805
C307 150uF 20% 6.3V TANT SMD-1
C267 150uF 20% 6.3V TANT SMD-1
C725 10uF 20% 6.3V CERM 805
C393 150uF 20% 6.3V TANT SMD-1
C405 150uF 20% 6.3V TANT SMD-1
C396 150uF 20% 6.3V TANT SMD-1
U48 SI6467BDQ TSSOP
+2_5V_MAIN
+2_5V_SLEEP
C715 10uF 20% 6.3V CERM 805
C716 1000pF 10% 25V X7R 402
R557 100K 5% 1/16W MF 402
2_5V_SLEEP_PWREN_L
NO STUFF R554 100K 5% 1/16W MF 402
NO STUFF C714 1000pF 10% 25V X7R 402
SLEEP_L_LS5_INV

1.8V SWITCHER

+1_8V_MAIN LOADS

1) INTREPID PLLS

+1_8V_SLEEP LOADS

1) MPC7447 - MAXBUS I/O - IF 1.8V INTERFACE
2) CPU JTAG & MaxBus Pull-ups
3) CPU PLL Config Straps

+3V_MAIN
LTC3411_VCC
C695 10uF 20% 6.3V CERM 805
R398 1M 5% 1/16W MF 402
NO STUFF R526 10K 5% 1/16W MF 402
R527 1M 5% 1/16W MF 402
R531 10 5% 1/16W MF 402
(BURST MODE)
R535 324K 1% 1/16W MF 402
LTC3411_EN_L
LTC3411_SHDN
LTC3411_SYNC
U46 LTC3411 MSOP
SVIN PVIN SHDN/RT SYNC/MODE PGOOD PGND SW VFB ITH SGND
CRITICAL L63 2.2uH SM1
1_8V_SW
+1_8V_MAIN
C693 10pF 5% 50V CERM 402
R529 887K 1% 1/16W MF 402
1_8V_VFB
C697 22uF 20% 10V CERM 1210
R528 698K 1% 1/16W MF 402
LTC3411_ITH
R532 16.2K 1% 1/16W MF 402
LTC3411_ITH_RC
C691 1000pF 5% 25V CERM 603
OMIT XW17 SM
LTC3411_GND
3V_5V_OK
Q31 2N7002 SM
NO STUFF R536 10K 5% 1/16W MF 402
(PULSE MODE)
R525 1M 5% 1/16W MF 402
(CONTINUOUS MODE)
C690 1uF 20% 10V CERM 603
+1_8V_MAIN
+1_8V_SLEEP
R566 100K 5% 1/16W MF 402
SLEEP
C719 10uF 20% 6.3V CERM 805
SI3447DV TSOP U50
C722 1000pF 10% 25V X7R 402
1_8V_SLEEP_PWREN_L
NO STUFF R571 100K 5% 1/16W MF 402
NO STUFF C720 1000pF 10% 25V X7R 402
SLEEP_L_LS5_INV

1.5V/1.8V/2.5V SUPPLIES

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DIGITAL SIGNALS

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
				STUB_LENGTH OF 200 MILS NEEDED WHEN WE CONVERT TO 14.2				
GROUP 0	MEM_DATA<7..0>	L:S:1602:1700	7	500	(200)			167 MHZ
	MEM_DQM<0>	L:S:1602 MIL:1700 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<0>	L:S:1602 MIL:1700 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<7..0>	L:S:1903:2000	7	500	(200)			167 MHZ
	RAM_DQM_A<0>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<0>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<7..0>	L:S:2000:2100	7	500	(200)			167 MHZ
	RAM_DQM_B<0>	L:S:2000 MIL:2100 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<0>	L:S:2000 MIL:2100 MIL	7	500.0000	(200)			167.0 MHz
GROUP 1	MEM_DATA<15..8>	L:S:1344:1660	7	500	(200)			167 MHZ
	MEM_DQM<1>	L:S:1344 MIL:1660 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<1>	L:S:1344 MIL:1660 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<15..8>	L:S:1905:2000	7	500	(200)			167 MHZ
	RAM_DQM_A<1>	L:S:1905 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<1>	L:S:1905 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<15..8>	L:S:2004:2412	7	500	(200)			167 MHZ
	RAM_DQM_B<1>	L:S:2004 MIL:2412 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<1>	L:S:2004 MIL:2412 MIL	7	500.0000	(200)			167.0 MHz
GROUP 2	MEM_DATA<23..16>	L:S:1435:1500	7	500	(200)			167 MHZ
	MEM_DQM<2>	L:S:1435 MIL:1500 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<2>	L:S:1435 MIL:1500 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<23..16>	L:S:1707:1800	7	500	(200)			167 MHZ
	RAM_DQM_A<2>	L:S:1707 MIL:1800 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<2>	L:S:1707 MIL:1800 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<23..16>	L:S:1900:2000	7	500	(200)			167 MHZ
	RAM_DQM_B<2>	L:S:1900 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<2>	L:S:1900 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
GROUP 3	MEM_DATA<31..24>	L:S:1233:1485	7	500	(200)			167 MHZ
	MEM_DQM<3>	L:S:1233 MIL:1485 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<3>	L:S:1233 MIL:1485 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<31..24>	L:S:1700:2165	7	500	(200)			167 MHZ
	RAM_DQM_A<3>	L:S:1700 MIL:2165 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<3>	L:S:1700 MIL:2165 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<25..24>	L:S:1907:2356	7	500	(200)			167 MHZ
	RAM_DATA_B<26>	L:S:1907 MIL:2356 MIL	7		(200)			167.0 MHz
	RAM_DATA_B<31..27>	L:S:1907:2356	7	500	(200)			167 MHZ
	RAM_DQM_B<3>	L:S:1907 MIL:2356 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<3>	L:S:1907 MIL:2356 MIL	7	500.0000	(200)			167.0 MHz
GROUP 4	MEM_DATA<39..32>	L:S:1915:2000	7	500	(200)			167 MHZ
	MEM_DQM<4>	L:S:1915 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<4>	L:S:1915 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<39..32>	L:S:1205:1387	7	500	(200)			167 MHZ
DDR RAM	RAM_DQM_A<4>	L:S:1205 MIL:1387 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<4>	L:S:1205 MIL:1387 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<39..32>	L:S:1404:1686	7	500	(200)			167 MHZ
	RAM_DQM_B<4>	L:S:1404 MIL:1686 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<4>	L:S:1404 MIL:1686 MIL	7	500.0000	(200)			167.0 MHz
GROUP 5	MEM_DATA<47..40>	L:S:1719:1893	7	500	(200)			167 MHZ
	MEM_DQM<5>	L:S:1719 MIL:1893 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<5>	L:S:1719 MIL:1893 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<47..40>	L:S:1607:1898	7	500	(200)			167 MHZ
	RAM_DQM_A<5>	L:S:1607 MIL:1898 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<5>	L:S:1607 MIL:1898 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<47..40>	L:S:1716:2102	7	500	(200)			167 MHZ
	RAM_DQM_B<5>	L:S:1716 MIL:2102 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<5>	L:S:1716 MIL:2102 MIL	7	500.0000	(200)			167.0 MHz
GROUP 6	MEM_DATA<55..48>	L:S:2101:2170	7	500	(200)			167 MHZ
	MEM_DQM<6>	L:S:2101 MIL:2170 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<6>	L:S:2101 MIL:2170 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<55..48>	L:S:1204:1357	7	500	(200)			167 MHZ
	RAM_DQM_A<6>	L:S:1204 MIL:1357 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<6>	L:S:1204 MIL:1357 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<55..48>	L:S:1400:1546	7	500	(200)			167 MHZ
	RAM_DQM_B<6>	L:S:1400 MIL:1546 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<6>	L:S:1400 MIL:1546 MIL	7	500.0000	(200)			167.0 MHz
GROUP 7	MEM_DATA<63..56>	L:S:1903:2000	7	500	(200)			167 MHZ
	MEM_DQM<7>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<7>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<63..56>	L:S:1611:1696	7	500	(200)			167 MHZ
	RAM_DQM_A<7>	L:S:1611 MIL:1696 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<7>	L:S:1611 MIL:1696 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<63..56>	L:S:1809:1887	7	500	(200)			167 MHZ
	RAM_DQM_B<7>	L:S:1809 MIL:1887 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<7>	L:S:1809 MIL:1887 MIL	7	500.0000	(200)			167.0 MHz
ADDR	MEM_ADDR<12..0>	L:S::500	4					83 MHZ
	RAM_ADDR<12..0>	L:S:2000:3000	10		(200)			
	MEM_BA<1..0>	L:S::500	4					
	RAM_BA<1..0>	L:S:2000:3300	8		(200)			
CONTROL	MEM_CS_L<3..0>	L:S::500	4					
	RAM_CS_L<3..0>	L:S:2500:3200	7		(200)			
	MEM_CKE<3..0>	L:S::500	4					
	RAM_CKE<3..0>	L:S:2500:3200	7		(200)			
	MEM_RAS_L	L:S::500 MIL	4					
	RAM_RAS_L	L:S:2000 MIL:4100 MIL	7		(200)			
	MEM_CAS_L	L:S::500 MIL	4					
	RAM_CAS_L	L:S:2000 MIL:4100 MIL	7		(200)			
	MEM_WE_L	L:S::500 MIL	4					
	RAM_WE_L	L:S:2000 MIL:3100 MIL	7		(200)			
	MEM_MUXSEL_MSB	L:S:1700 MIL:3000 MIL	7					
	MEM_MUXSEL_LSB	L:S:1700 MIL:3000 MIL	7					

TOTAL LENGTH CONTROLLED BY SPREADSHEET

PRIORITY: 2
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9
GOAL: MINIMIZE
EXPOSED ROUTES
MINIMIZE VIAS

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME	PROPAGATION_DELAY	MATCHED_DELAY	MAX VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM
INTREPID CLOCKS	SYSCLK_CPU_UF	L:S::150 MIL					10 MIL SPACING	167.0 MHz
	SYSCLK_CPU	L:S:2650 MIL:2750 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz
	INT_CPUFB_OUT	L:S::150 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_OUT_SHORT	L:S:700 MIL:850 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_OUT_NORM	L:S:500 MIL:600 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_IN_NORM	L:S:500 MIL:600 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_LONG	L:S:1050 MIL:1150 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_IN	L:S:700 MIL:800 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0_UF	L:S:300 MIL:500 MIL	SYSCLK_DDRCLK_A0_UF	SYSCLK_DDRCLK_A0_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0_L_UF	L:S:300 MIL:500 MIL	SYSCLK_DDRCLK_A0_UF	SYSCLK_DDRCLK_A0_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1_UF	L:S:300 MIL:500 MIL	SYSCLK_DDRCLK_A1_UF	SYSCLK_DDRCLK_A1_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1_L_UF	L:S:300 MIL:500 MIL	SYSCLK_DDRCLK_A1_UF	SYSCLK_DDRCLK_A1_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0_UF	L:S:300 MIL:500 MIL	SYSCLK_DDRCLK_B0_UF	SYSCLK_DDRCLK_B0_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0_L_UF	L:S:300 MIL:500 MIL	SYSCLK_DDRCLK_B0_UF	SYSCLK_DDRCLK_B0_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1_UF	L:S:300 MIL:500 MIL	SYSCLK_DDRCLK_B1_UF	SYSCLK_DDRCLK_B1_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1_L_UF	L:S:300 MIL:500 MIL	SYSCLK_DDRCLK_B1_UF	SYSCLK_DDRCLK_B1_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A0	SYSCLK_DDRCLK_A0:G:L:S:0 MIL:25 MIL	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0_L	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A0	SYSCLK_DDRCLK_A0:G:L:S:0 MIL:25 MIL	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A1	SYSCLK_DDRCLK_A1:G:L:S:0 MIL:25 MIL	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1_L	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A1	SYSCLK_DDRCLK_A1:G:L:S:0 MIL:25 MIL	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B0	SYSCLK_DDRCLK_B0:G:L:S:0 MIL:25 MIL	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0_L	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B0	SYSCLK_DDRCLK_B0:G:L:S:0 MIL:25 MIL	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B1	SYSCLK_DDRCLK_B1:G:L:S:0 MIL:25 MIL	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1_L	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B1	SYSCLK_DDRCLK_B1:G:L:S:0 MIL:25 MIL	250.0000	(200)	10 MIL SPACING	167.0 MHz
	INT_REF_CLK_OUT_UF	L:S::400 MIL				(200)	10 MIL SPACING	49.92 MHz
	INT_REF_CLK_OUT	L:S:1000 MIL:1150 MIL		5	250.0000	(200)	10 MIL SPACING	49.92 MHz
	INT_REF_CLK_IN	L:S:1900 MIL:2000 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz
	CLK66M_GPU_AGP_UF	L:S::150 MIL				(200)	10 MIL SPACING	66.00 MHz
	CLK66M_GPU_AGP	L:S:1800 MIL:1900 MIL		6	400.0000	(200)	10 MIL SPACING	66.00 MHz
	INT_AGP_FB_OUT	L:S::150 MIL				(200)	10 MIL SPACING	66.00 MHz
	INT_AGP_FB_IN	L:S:1450 MIL:1550 MIL		6	500.0000	(200)	10 MIL SPACING	66.00 MHz
	CLK33M_CBUS_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz
	CLK33M_CBUS	L:S:5000 MIL:6000 MIL		9	500.0000	(200)	10 MIL SPACING	33.00 MHz
	CLK33M_AIRPORT_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz
	CLK33M_AIRPORT	L:S:9500 MIL:10500 MIL		6	500.0000	(200)	10 MIL SPACING	33.00 MHz
	CLK33M_NEC_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz
	CLK33M_NEC	L:S:4000 MIL:6000 MIL		7	500.0000	(200)	10 MIL SPACING	33.00 MHz
	INT_PCI_FB_OUT	L:S::300 MIL				(200)	10 MIL SPACING	33.00 MHz
	INT_PCI_FB_IN	L:S:6500 MIL:7500 MIL		7	500.0000	(200)	10 MIL SPACING	33.00 MHz
M10 & OSC	ATI_CLK27M_OSC	L:S::400 MIL		5		(200)	10 MIL SPACING	
	ATI_CLK27M_OSC_SS	L:S::400 MIL		5		(200)	10 MIL SPACING	
	ATI_CLK27M_IN	L:S::200 MIL		5		(200)	10 MIL SPACING	
	ATI_SSCLK_UF	L:S::200 MIL		5		(200)	10 MIL SPACING	
	ATI_SSCLK_IN	L:S::1800 MIL		5	500.0000	(200)	10 MIL SPACING	
CRYSTALS	CLK18M_INT_XIN	L:S:1400 MIL:1500 MIL					10 MIL SPACING	
	CLK18M_INT_XOUT	L:S:1250 MIL:1350 MIL					10 MIL SPACING	
	CLK18M_XTAL_IN	L:S::300 MIL					10 MIL SPACING	
	CLK18M_INT_EXT	L:S::400 MIL					10 MIL SPACING	
SOUND	INT_I2S0_SND_MCLK			6	500.0000	(200)	10 MIL SPACING	
ETHERNET	CLKENET_PHY_RX	L:S::300 MIL				(200)		125.0 MHz
	CLKENET_LINK_RX	L:S:8000 MIL:9000 MIL		6	800.0000	(200)	10 MIL SPACING	125.0 MHz
	CLKENET_PHY_GBE_REF	L:S::300 MIL				(200)		125.0 MHz
	CLKENET_LINK_GBE_REF	L:S:8000 MIL:9000 MIL		6	500.0000	(200)	10 MIL SPACING	125.0 MHz
	CLKENET_PHY_TX	L:S::300 MIL				(200)		25.00 MHz
	CLKENET_LINK_TX	L:S:8000 MIL:9000 MIL		6	500.0000	(200)	10 MIL SPACING	25.00 MHz
	CLKENET_LINK_GTX	L:S::300 MIL				(200)		125.0 MHz
	CLKENET_PHY_GTX	L:S:8000 MIL:9000 MIL		6	600.0000	(200)	10 MIL SPACING	125.0 MHz
FIREWIRE	CLKFW_PHY_PCLK	L:S::300 MIL				(200)		49.15 MHz
	CLKFW_LINK_PCLK	L:S:7500 MIL:8000 MIL		5	500.0000	(200)	10 MIL SPACING	49.15 MHz
	CLKFW_PHY_LCLK	L:S:7500 MIL:8000 MIL		5	500.0000	(200)	10 MIL SPACING	49.15 MHz
	CLKFW_LINK_LCLK	L:S::300 MIL				(200)		49.15 MHz
	FW_XI	L:S::500 MIL				(200)	10 MIL SPACING	98.03 MHz
	FW_OSC	L:S::300 MIL				(200)	10 MIL SPACING	98.03 MHz

PRIORITY: 1
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9
GOAL: MINIMIZE EXPOSURE ON LONG NETS

SIGNAL CONSTRAINTS - PAGE 1

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6809	B

SCALE	SHT	OF
NONE	35	44

DIGITAL SIGNALS

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
MAXBUS	CPU_AACK_L	L:S:1500 MIL:2700 MIL	7		(250)				5 8
	CPU_ADDR<0..31>	L:S:1500:3100	7		(250)		TRUE	83 MHZ	5 8
	CPU_ARTRY_L	L:S:1500 MIL:2700 MIL	7		(250)				5 8
	CPU_BG_L	L:S:1500 MIL:2700 MIL	7		(250)				5 8
	CPU_BR_L	L:S:1500 MIL:2700 MIL	7		(250)				5 8
	CPU_CI_L	L:S:1500 MIL:2700 MIL	7		(250)				5 8
	CPU_DATA<0..31>	L:S:1100:2700	7		(250)		TRUE	83 MHZ	6 8
	CPU_DATA<32..63>	L:S:1100:2700	8		(250)			83 MHZ	6 8
	CPU_DBG_L	L:S:1500 MIL:2700 MIL	7		(250)				5 8
	CPU_DTI<0..2>	L:S:1500:2950	7		(250)				5 8
	CPU_DRDY_L	L:S:1500 MIL:3200 MIL	7		(250)				5 8
	CPU_GBL_L	L:S:1500 MIL:2700 MIL	7		(250)				5 8
	CPU_HIT_L	L:S:1500 MIL:2800 MIL	7		(250)				5 8
	CPU_QACK_L	L:S:1500 MIL:2700 MIL	7		(250)				5 8
	CPU_QREQ_L	L:S:1500 MIL:2700 MIL	7		(250)				5 8
	CPU_TA_L	L:S:1500 MIL:2700 MIL	7		(250)				5 8
	CPU_TBST_L	L:S:1500 MIL:2700 MIL	7		(250)				5 8
	CPU_TEA_L	L:S:1500 MIL:3000 MIL	7		(250)				5 8
	CPU_TS_L	L:S:1500 MIL:2700 MIL	7		(250)				5 8
	CPU_TSIZ<0..2>	L:S:1500:3500	7		(250)				5 8
	CPU_TT<0..4>	L:S:1500:3400	7		(250)				5 8
	CPU_WT_L	L:S:1500 MIL:3100 MIL	7		(250)				5 8

PRIORITY: 4
PRIMARY LAYERS: 9
SECONDARY LAYERS: 4,7
GOAL: MINIMIZE TH VIAS

STUB_LENGTH OF 250 MILS NEEDED WHEN DESIGN SWITCHED TO 14.2

Temporary Area for TMDS/DVO signal constraints

ALL TMDS GROUP SIGNALS ROUTE AT LAYER 4 OR 7 AND HAVE SAME WIDTH SPACING RULE AS OTHER TMDS SIGNALS

123	GPU_TMDS_CLKN	GPU_CLKTMDS	GPUTMDS:G:L:S:0 MIL:50 MIL		500.0000	100 OHM SPACING	5	19 20
123	GPU_TMDS_CLKP	GPU_CLKTMDS	GPUTMDS:G:L:S:0 MIL:50 MIL		500.0000	100 OHM SPACING	5	19 20
123	GPU_TMDS_DN<0>	GPU_TMDS_D0			500.0000	100 OHM SPACING	8	19 20
123	GPU_TMDS_DP<0>	GPU_TMDS_D0			500.0000	100 OHM SPACING	8	19 20
123	GPU_TMDS_DN<1>	GPU_TMDS_D1			600.0000	100 OHM SPACING	8	19 20
123	GPU_TMDS_DP<1>	GPU_TMDS_D1			600.0000	100 OHM SPACING	8	19 20
123	GPU_TMDS_DN<2>	GPU_TMDS_D2			830.0000	100 OHM SPACING	8	19 20
123	GPU_TMDS_DP<2>	GPU_TMDS_D2			830.0000	100 OHM SPACING	8	19 20
124	SI_TMDS_CLKN	SI_CLKTMDS	SITMDS:G:L:S:0 MIL:50 MIL			100 OHM SPACING	5	19
123	SI_TMDS_CLKP	SI_CLKTMDS	SITMDS:G:L:S:0 MIL:50 MIL			100 OHM SPACING	5	19
124	SI_TMDS_DN<0>	SI_TMDS_D0				100 OHM SPACING	8	19
124	SI_TMDS_DP<0>	SI_TMDS_D0				100 OHM SPACING	8	19
124	SI_TMDS_DN<1>	SI_TMDS_D1				100 OHM SPACING	8	19
124	SI_TMDS_DP<1>	SI_TMDS_D1				100 OHM SPACING	8	19
124	SI_TMDS_DN<2>	SI_TMDS_D2				100 OHM SPACING	8	19
124	SI_TMDS_DP<2>	SI_TMDS_D2				100 OHM SPACING	8	19

ALL THE DVOD GROUP SIGNALS ROUTE AT LAYER 4 OR 7 AND ROUTE AS STANDARD 50OHM SIGNALS AT 4 MILS

126	ATI_DVOD<11..0>	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610			19 20
126	ATI_DVOD_DE	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610.0000			19 20
126	ATI_DVO_HSYNC	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610.0000			19 20
126	ATI_DVO_VSYNC	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610.0000			19 20
126	ATI_DVO_CLKP	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610.0000	165.0 MHz:::		19 20
125	GPU_DVOD<11..0>	GPUDVOD:G:L:S:0 MIL:50 MIL	6	700			19
125	GPU_DVOD_DE	GPUDVOD:G:L:S:0 MIL:50 MIL	6	500.0000			19
126	GPU_DVO_HSYNC	GPUDVOD:G:L:S:0 MIL:50 MIL	6	500.0000			19
126	GPU_DVO_VSYNC	GPUDVOD:G:L:S:0 MIL:50 MIL	6	500.0000			19
126	GPU_DVO_CLKP	GPUDVOD:G:L:S:0 MIL:50 MIL	6	500.0000	165.0 MHz:::		19

126	TMDS_CONN_CLKN	CLKCONN_TMDS	TMDS_CONN:G:L:S:0 MIL:50 MIL		500.0000	100 OHM SPACING	4	22 39
126	TMDS_CONN_CLKP	CLKCONN_TMDS	TMDS_CONN:G:L:S:0 MIL:50 MIL		500.0000	100 OHM SPACING	4	22 39
127	TMDS_CONN_DN<0>	CONN_TMDS_D0			500.0000	100 OHM SPACING	4	22
127	TMDS_CONN_DP<0>	CONN_TMDS_D0			500.0000	100 OHM SPACING	4	22
127	TMDS_CONN_DN<1>	CONN_TMDS_D1			500.0000	100 OHM SPACING	4	22
127	TMDS_CONN_DP<1>	CONN_TMDS_D1			500.0000	100 OHM SPACING	4	22
127	TMDS_CONN_DN<2>	CONN_TMDS_D2			500.0000	100 OHM SPACING	4	22
127	TMDS_CONN_DP<2>	CONN_TMDS_D2			500.0000	100 OHM SPACING	4	22

SIGNAL CONSTRAINTS - PAGE 1

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6809	B

SCALE	SHT	OF
NONE	36	44

Digital Signals (cont'd)

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
AGP	AGP_AD<15..0>	L:S:1050:1450	7					66 MHz
AGP BYTES 0-1	AGP_CBE<1..0>	L:S:1050:1450	7					66 MHz
	AGP_AD_STB<0>	L:S:1050 MIL:1450 MIL			(250)	8 MIL SPACING		133.0 MHz
	AGP_AD_STB_L<0>	L:S:1050 MIL:1450 MIL			(250)	8 MIL SPACING		133.0 MHz
AGP BYTES 2-3	AGP_AD<31..16>	L:S:1050:1450	7					66 MHz
	AGP_CBE<3..2>	L:S:1050:1450	7					66 MHz
	AGP_AD_STB<1>	L:S:1050 MIL:1450 MIL			(250)	8 MIL SPACING		133.0 MHz
	AGP_AD_STB_L<1>	L:S:1050 MIL:1450 MIL			(250)	8 MIL SPACING		133.0 MHz
AGP SIDEBAND	AGP_SBA<7..0>	L:S:1050:1450	7					66 MHz
	AGP_SB_STB	L:S:1050 MIL:1450 MIL			(350)	8 MIL SPACING		66.00 MHz
	AGP_SB_STB_L	L:S:1050 MIL:1450 MIL			(350)	8 MIL SPACING		66.00 MHz
AGP CONTROL	AGP_FRAME_L	L:S:1250 MIL:1950 MIL						66.00 MHz
	AGP_IRDY_L	L:S:1250 MIL:1950 MIL						66.00 MHz
	AGP_TRDY_L	L:S:1250 MIL:1950 MIL						66.00 MHz
	AGP_DEVSEL_L	L:S:1250 MIL:1950 MIL						66.00 MHz
	AGP_STOP_L	L:S:1250 MIL:1950 MIL						66.00 MHz
	AGP_PAR	L:S:1250 MIL:1950 MIL						66.00 MHz
	AGP_REQ_L	L:S:1250 MIL:1950 MIL						66.00 MHz
	AGP_GNT_L	L:S:1250 MIL:1950 MIL						66.00 MHz
	AGP_RBF_L	L:S:1250 MIL:1950 MIL						66.00 MHz
PCI	PCI_AD<31..0>	L:S:6000:12500				MIN_DAISY_CHAIN		33 MHz
	PCI_CBE<3..0>	L:S:6000:12500				MIN_DAISY_CHAIN		33 MHz
	PCI_FRAME_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHz
	PCI_IRDY_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHz
	PCI_TRDY_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHz
	PCI_DEVSEL_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHz
	PCI_STOP_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHz
	PCI_PAR	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHz
ULTRA ATA-100	UIDE_DATA<15..8>	L:S::710			(200)			100 MHZ
	UIDE_DATA<7>	U51_V1:RP19.3::600 MIL			(200)			100.0 MHz
	UIDE_DATA<6..0>	L:S::600			(200)			100 MHZ
	UIDE_ADDR<2..0>	L:S::650			(200)	NEED TO MATCH DELAY TO 250		100 MHZ
	UIDE_RST_L	L:S::400 MIL			(200)			100.0 MHz
	UIDE_DIOW_L	L:S::400 MIL			(200)			100.0 MHz
	UIDE_DIOR_L	L:S::600 MIL		10 MIL SPACING	(200)			100.0 MHz
	UIDE_DMACK_L	L:S::400 MIL			(200)			100.0 MHz
	UIDE_CS0_L	L:S::500 MIL			(200)			100.0 MHz
	UIDE_CS1_L	L:S::500 MIL			(200)			100.0 MHz
	UIDE_DMARQ	L:S::400 MIL			(200)			100.0 MHz
	UIDE_IOCHRDY	L:S::600 MIL		10 MIL SPACING	(200)			100.0 MHz
	UIDE_INTRQ	L:S::400 MIL			(200)			100.0 MHz
	HD_DATA<15..0>	L:S:5000:6500	7		(200)			100 MHZ
	HD_ADDR<2..0>	L:S:5000:6500	7		(200)			100 MHZ
	HD_RESET_L	L:S:4000 MIL:6000 MIL	7		(200)	TOTAL UIDE+HD SKEW <500MIL		100.0 MHz
	HD_DIOW_L	L:S:3000 MIL:5200 MIL	7		(200)			100.0 MHz
	HD_DIOR_L	L:S:6100 MIL:6150 MIL	7	10 MIL SPACING	(200)			100.0 MHz
	HD_DMACK_L	L:S:4500 MIL:6000 MIL	7		(200)			100.0 MHz
	HD_CS0_L	L:S:3000 MIL:6000 MIL	7		(200)			100.0 MHz
	HD_CS1_L	L:S:3000 MIL:6000 MIL	7		(200)			100.0 MHz
	HD_DMARQ	L:S:4500 MIL:6000 MIL	7		(200)			100.0 MHz
	HD_IOCHRDY	L:S:6200 MIL:6300 MIL	7	10 MIL SPACING	(200)			100.0 MHz
	HD_INTRQ	L:S:3000 MIL:5000 MIL	7					100.0 MHz
EIDE INTREPID	EIDE_DATA<15..0>	L:S::850						33 MHZ
	EIDE_ADDR<2..0>	L:S::850						33 MHZ
	EIDE_CS0_L	L:S::850 MIL						33.00 MHz
	EIDE_CS1_L	L:S::850 MIL						33.00 MHz
	EIDE_RD_L	L:S::500 MIL						33.00 MHz
	EIDE_WR_L	L:S::500 MIL						33.00 MHz
	EIDE_IOCHRDY	L:S::500 MIL						33.00 MHz
	EIDE_INT	L:S::500 MIL						33.00 MHz
	EIDE_RST_L	L:S::500 MIL						33.00 MHz
	EIDE_DMACK_L	L:S::500 MIL						33.00 MHz
	EIDE_DMARQ	L:S::500 MIL						33.00 MHz
OPTICAL	EIDE_OPTICAL_DATA<15..0>	L:S:4000:6000						33 MHZ
	EIDE_OPTICAL_ADDR<2..0>	L:S:4000:6000						33 MHZ
	EIDE_OPTICAL_CS0_L	L:S:4500 MIL:6500 MIL						33.00 MHz
	EIDE_OPTICAL_CS1_L	L:S:4500 MIL:6500 MIL						33.00 MHz
	EIDE_OPTICAL_READ_L	L:S:4500 MIL:6500 MIL						33.00 MHz
	EIDE_OPTICAL_WR_L	L:S:4500 MIL:6500 MIL						33.00 MHz
	EIDE_OPTICAL_IOCHRDY	L:S:4500 MIL:6500 MIL						33.00 MHz
	EIDE_OPTICAL_INT	L:S:5000 MIL:7000 MIL						33.00 MHz
	EIDE_OPTICAL_RST_L	L:S:4500 MIL:6500 MIL						33.00 MHz
	EIDE_OPTICAL_DMAACK_L	L:S:4500 MIL:6500 MIL						33.00 MHz
	EIDE_OPTICAL_DMA_RQ	L:S:4500 MIL:6500 MIL						33.00 MHz
ETHERNET MII	ENET_LINK_RXD<7..0>	L:S:8000:9000	7	(400)		(400)		
	ENET_RX_DV	L:S:8000 MIL:9000 MIL						
	ENET_RX_ER	L:S:8000 MIL:9000 MIL						
	ENET_PHY_TXD<7..0>	L:S:8000:9000	7	(400)		(400)		
	ENET_LINK_TXD<7..0>	L:S::600						
	ENET_PHY_TX_ER	L:S:8000 MIL:9000 MIL						
	ENET_LINK_TX_ER	L:S::400 MIL						
	ENET_PHY_TX_EN	L:S:8000 MIL:9000 MIL						
	ENET_LINK_TX_EN	L:S::400 MIL						
	ENET_MDIO	L:S:8000 MIL:9000 MIL						
	ENET_MDC	L:S:8000 MIL:9000 MIL						
	ENET_COL	L:S:8000 MIL:9000 MIL						
	ENET_CRS	L:S:8000 MIL:9000 MIL						
FIREWIRE MII	FW_LINK_DATA<7..0>	L:S:2700:3500	7	(400)		(400)		
	FW_PHY_DATA<7..0>	L:S:4700:5500	7	(400)		(400)		
	FW_LINK_CNTL<1..0>	L:S:9000:10000						
	FW_PHY_CNTL<1..0>	L:S::300						
	FW_LINK_LREQ	L:S::300 MIL						
	FW_PHY_LREQ	L:S:8500 MIL:9500 MIL						
	FW_PINT	L:S:8500 MIL:9500 MIL						

PRIORITY: 4
PRIMARY LAYERS: 9
SECONDARY LAYERS: 4,7
GOAL: MINIMIZE TH VIAS

PRIORITY: 7
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 6
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 8
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 5
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 5
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR	RELATIVE_PROPAGATION_DELAY	MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS
FIREWIRE Zo = 110	FW_TPI0N	FW_TPI0	FW_TPI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPI0P	FW_TPI0	FW_TPI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPO0N	FW_TPO0	FW_TPO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPO0P	FW_TPO0	FW_TPO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPBI0N	FW_TPBI0	FW_TPBI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPBI0P	FW_TPBI0	FW_TPBI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPAO0N	FW_TPAO0	FW_TPAO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPAO0P	FW_TPAO0	FW_TPAO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPA1N	FW_TPA1	FW_TPA1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPA1P	FW_TPA1	FW_TPA1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPB1N	FW_TPB1	FW_TPB1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPB1P	FW_TPB1	FW_TPB1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPI1N	FW_TPI1	FW_TPI1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPI1P	FW_TPI1	FW_TPI1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPO1N	FW_TPO1	FW_TPO1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPO1P	FW_TPO1	FW_TPO1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
ETHERNET Zo = 100	MDI_P<0>	ENET_MDI0	ENET_MDI0:G:U43.29:J23.1:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_M<0>	ENET_MDI0	ENET_MDI0:G:U43.31:J23.2:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_P<1>	ENET_MDI1	ENET_MDI1:G:U43.33:J23.3:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_M<1>	ENET_MDI1	ENET_MDI1:G:U43.34:J23.4:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_P<2>	ENET_MDI2	ENET_MDI2:G:U43.39:J23.7:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_M<2>	ENET_MDI2	ENET_MDI2:G:U43.41:J23.8:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_P<3>	ENET_MDI3	ENET_MDI3:G:U43.42:J23.9:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_M<3>	ENET_MDI3	ENET_MDI3:G:U43.43:J23.10:0 MIL:100 MIL		ENET 11 MIL SPACING	
LVDS Zo = 100 LOWER	CLKLVDS_LN	CLKLVDS_L	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4
	CLKLVDS_LP	CLKLVDS_L	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4
	LVDS_L0N	LVDS_L0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L0P	LVDS_L0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L1N	LVDS_L1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L1P	LVDS_L1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L2N	LVDS_L2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L2P	LVDS_L2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
UPPER	CLKLVDS_UN	CLKLVDS_U	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4
	CLKLVDS_UP	CLKLVDS_U	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4
	LVDS_U0N	LVDS_U0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U0P	LVDS_U0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U1N	LVDS_U1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U1P	LVDS_U1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U2N	LVDS_U2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U2P	LVDS_U2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
TMDS Zo = 100	TMDS_CLKN	CLKTMDS	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	5
	TMDS_CLKP	CLKTMDS	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	5
	TMDS_DN<0>	TMDS_D0		500.0000	100 OHM SPACING	8
	TMDS_DP<0>	TMDS_D0		500.0000	100 OHM SPACING	8
	TMDS_DN<1>	TMDS_D1		500.0000	100 OHM SPACING	8
	TMDS_DP<1>	TMDS_D1		500.0000	100 OHM SPACING	8
	TMDS_DN<2>	TMDS_D2		500.0000	100 OHM SPACING	8
	TMDS_DP<2>	TMDS_D2		500.0000	100 OHM SPACING	8
	ATI_TMDS_CLKN	ATI_CLKTMDS	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	5
	ATI_TMDS_CLKP	ATI_CLKTMDS	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	5
	ATI_TMDS_DN<0>	ATI_TMDS_D0		200.0000	100 OHM SPACING	8
	ATI_TMDS_DP<0>	ATI_TMDS_D0		200.0000	100 OHM SPACING	8
	ATI_TMDS_DN<1>	ATI_TMDS_D1		200.0000	100 OHM SPACING	8
	ATI_TMDS_DP<1>	ATI_TMDS_D1		200.0000	100 OHM SPACING	8
	ATI_TMDS_DN<2>	ATI_TMDS_D2		500.0000	100 OHM SPACING	8
	ATI_TMDS_DP<2>	ATI_TMDS_D2		500.0000	100 OHM SPACING	8
USB 1.1 Zo = 90	USB_DEM	USB_DE	USB_DE:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	USB_DEP	USB_DE	USB_DE:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	USB_DFM	USB_DF	USB_DF:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	USB_DFP	USB_DF	USB_DF:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
USB 2.0 Zo = 90	BT_USB_DM	BT_USB_D	BT_USB:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	BT_USB_DP	BT_USB_D	BT_USB:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	MODEM_USB_DM	MODEM_USB_D	MODEM_USB:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	MODEM_USB_DP	MODEM_USB_D	MODEM_USB:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	NEC_USB_DAM	USB_D1	USB_D1:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	
	NEC_USB_DAP	USB_D1	USB_D1:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	
	NEC_USB_DBM	USB_D2	USB_D2:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	
	NEC_USB_DBP	USB_D2	USB_D2:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	
POWER SUPPLIES	1772_CSSN	1772_CSS	1772_CSS:G:L:S:0 MIL:100 MIL			
	1772_CSSP	1772_CSS	1772_CSS:G:L:S:0 MIL:100 MIL			
	1772_CSIN	1772_CSI	1772_CSI:G:L:S:0 MIL:100 MIL			
	1772_CSIP	1772_CSI	1772_CSI:G:L:S:0 MIL:100 MIL			
	3V_SNSM	3V_SNS	3V_SNS:G:L:S:0 MIL:100 MIL			
	3V_SNSP	3V_SNS	3V_SNS:G:L:S:0 MIL:100 MIL			
	5V_SNSM	5V_SNS	5V_SNS:G:L:S:0 MIL:100 MIL			
	5V_SNSP	5V_SNS	5V_SNS:G:L:S:0 MIL:100 MIL			
THERMOSTAT	THERM1_DM		THERM1:G:L:S:0 MIL:100 MIL			
	THERM1_DP		THERM1:G:L:S:0 MIL:100 MIL			
	THERM2_DM		THERM2:G:L:S:0 MIL:100 MIL			
	THERM2_DP		THERM2:G:L:S:0 MIL:100 MIL			
	THERM1_M_DM	THERM1_MAIN	THERM1_MAIN:G:L:S:0 MIL:100 MIL			
	THERM1_M_DP	THERM1_MAIN	THERM1_MAIN:G:L:S:0 MIL:100 MIL			
	THERM2_M_DM	THERM2_MAIN	THERM2_MAIN:G:L:S:0 MIL:100 MIL			
	THERM2_M_DP	THERM2_MAIN	THERM2_MAIN:G:L:S:0 MIL:100 MIL			
	THERM1_A_DM	THERM1_ALT	THERM1_ALT:G:L:S:0 MIL:100 MIL			
	THERM1_A_DP	THERM1_ALT	THERM1_ALT:G:L:S:0 MIL:100 MIL			
	THERM2_A_DM	THERM2_ALT	THERM2_ALT:G:L:S:0 MIL:100 MIL			
	THERM2_A_DP	THERM2_ALT	THERM2_ALT:G:L:S:0 MIL:100 MIL			

PRIORITY: 3
PRIMARY LAYERS: 4,7 FOR CONTROLLED IMPEDANCE DIFF PAIRS
SECONDARY LAYERS: 2,9 FOR UNCONTROLLED IMPEDANCE DIFF PAIRS

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3MIL (TRACE WIDTH)
S = 11MIL (TRACE SEPERATION)
H = 16.8MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 106.2 OHMS
Zo(single) = 55.4 OHMS

Clear adjacent power plane!
Zo will be lower due to asymmetric stackup.

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3.1MIL (TRACE WIDTH)
S = 4.9MIL (TRACE SEPERATION)
H = 9.6MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 94 OHMS
Zo(single) = 50 OHMS

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3.9MIL (TRACE WIDTH)
S = 5.6MIL (TRACE SEPERATION)
H = 9.6MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 89.8 OHMS
Zo(single) = 46.6 OHMS

LAYERS 2 OR 9

SIGNAL CONSTRAINTS - PAGE 2

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6809 | REV. B

SCALE NONE | SHT 37 OF 44

POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
MAIN/SLEEP	+24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+BATT	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23 39
	+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=6	MIN_NECK_WIDTH=6	39
	+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+2_5V_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	39
	+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP_VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30 31 39
	J30 +ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30 38
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30 38
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30 39
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30 39
	1772_DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		30
	1772_LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	30
	1772_LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		30
	1772_DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		30
	1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10		30
PMU	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	+4_85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		29 31
	+4_6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10		31 32
	+4_85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		31
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		31
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		25 29
MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24 32
	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24
TRACKPAD	+5V_TPAD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=10		23 39
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		23 39
VIDEO	+14V_INV	VOLTAGE=14V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	22 39
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
AUDIO	J38 +5V_MAIN_AUD	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 32
	J38 +3V_MAIN_AUD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 32
	J38 AUD_GND	VOLTAGE=0V	MIN_LINE_WIDTH=50		25
FAN	J40 +FAN_PWR	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 39
	FAN1_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	FAN2_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39

I/O AREA	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	IN	
	CHGND1				
INVERTER	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN	
	CHGND2				
TRACKPAD	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN	
	CHGND3				
LVDS	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN	
	CHGND4				

ENET_CTAP_CHGND VOLTAGE=0V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=12

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 6 33 39
	CPU_AVDD	VOLTAGE=1.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 6 7 8 15 16 33
	J162 CPU_AVDD_VIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
	J163 CPU_AVDD_VOUT	VOLTAGE=1.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
DDR RAM	DDR_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		11
INTREPID	J43 +2_5V_INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	9 10 15 16
	+3V_INTREPID_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14
PLLS	+1_5V_INTREPID_PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	8 12 14
	+1_5V_INTREPID_PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	8
	+1_5V_INTREPID_PLL8	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
REFERENCE	INT_MEM_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		9
	INT_AGP_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		12 19
	INT_MEM_REF_H	VOLTAGE=0V	MIN_LINE_WIDTH=10		9
	UIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8		13
AIRPORT	+3V_AIRPORT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
CARDBUS	J165 +3V_SLEEP_PCCARD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
ATI M11	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	19 20 39
	+3V_GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 19 20 21
	+3V_GPU_FLT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+2_5V_GPU	VOLTAGE=2.5V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	
	GPU_MEM_IO	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	19 21
	GPU_MEM_IO_FLT	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+2_5V_GPU_MEMCORE	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+1_8V_GPU	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	19 20 21
	+1_5V_AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 15 16 19 20 21
	+2_5V_GPU_PNLIO	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_8V_ATI_PVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20 21
	+1_5V_AGP_GPU	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_5V_GPU_VDD15	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	+1_8V_GPU_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_VDDDI	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	GPU_VCORE_VDDCI	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	+2_5V_GPU_A2VDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_PNLPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_PNLIO	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+2_5V_GPU_MCLK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_AVDDQ	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_MEMPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+3V_ATI_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	+3V_ATI_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	+GPU_VDD15_UF	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
ETHERNET 88E1111 NEC USB2.0	J144 +2_5V_SLEEP_NECK1	VOLTAGE=2.5V	MIN_LINE_WIDTH=10		20
	J144 +3V_SLEEP_NECK	VOLTAGE=3V	MIN_LINE_WIDTH=10		34
	J144 +1_5V_AGP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		20
	J156 +1_8V_PVDD_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		20
	J145 GPU_VCORE_NECK	VOLTAGE=1.2V	MIN_LINE_WIDTH=10		20
	J145 +GPU_VDD15_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		20
	J145 +2_5V_SLEEP_NECK2	VOLTAGE=2.5V	MIN_LINE_WIDTH=10		34
	J145 +1_8V_SLEEP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		34
	J145 +1_5V_SLEEP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		34
	J156 +1_8V_ATI_TPVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	J156 +1_8V_GPU_TP_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+2_5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+2_5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+1_0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	J141 +3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
	J141 NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	17
FW	J142 LM2594_IN	VOLTAGE=33V	MIN_LINE_WIDTH=40	MIN_NECK_WIDTH=12	27
	J141 +FW_PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	+FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	J141 +FW_AMP_SENSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	
	+FW_PWR_OR	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	27 28
	J141 +FW_PWR1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	+FW_VP0	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28 39
	+FW_VP1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28 39
	+3V_FW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27 28
	+3V_FW_UF	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_PLLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	J141 FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	J145 FW_VDD_ON	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	1625_VSW	VOLTAGE=14V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+PBUS_JUMPER	VOLTAGE=14V	MIN_LINE_WIDTH=10		
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		31
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		31
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		31
	1V20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	30 31
LTC3707 5V SWITCHER	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	32
	5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+5V_MAIN_JUMPER	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
3V SWITCHER	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+3V_MAIN_JUMPER	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		32
MAX1715 2.5V SWITCHER	2_5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	34
	2_5V_LX_F	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	
	2_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	2_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	2_5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	2_5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
1.65V SWITCHER	1_5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8		34
	1_5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	34
	1_5V_LX_F	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	
	1_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	1_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	1_5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	1_5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
CONTROL	1_5V_ILIM		MIN_LINE_WIDTH=8		34
	2_5V_ILIM		MIN_LINE_WIDTH=8		34
	MAX1715_TON		MIN_LINE_WIDTH=8		34
	MAX1715_SKIP		MIN_LINE_WIDTH=8		34
	MAX1715_REF	VOLTAGE=2.0V	MIN_LINE_WIDTH=8		34
	MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
MAX1717	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	33
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=200	MIN_NECK_WIDTH=10	33
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	33
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	33
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	33
	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	33
	VCORE_ILIM		MIN_LINE_WIDTH=8		33
	VCORE_REF		MIN_LINE_WIDTH=8		33
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8		33
	VCORE_CC		MIN_LINE_WIDTH=8		33
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		33 39
	VCORE_TIME		MIN_LINE_WIDTH=8		33
	VCORE_VGATE		MIN_LINE_WIDTH=8		14 33
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30		33
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8		33
	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		33
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8		33
	J131 VCORE_GNDA	VOLTAGE=0V	MIN_LINE_WIDTH=10		33
LTC1778	1778_VIN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1778_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1778_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	20
	1778_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	20
	1778_BST_RC	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	20
	1778_TG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1778_BG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	GPU_VCORE_SW	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	20
	GPU_VCORE_SW_F	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	
	1778_ION		MIN_LINE_WIDTH=8		20
	1778_ITH		MIN_LINE_WIDTH=8		20
	1778_ITH_RC		MIN_LINE_WIDTH=8		20
	1778_VFB		MIN_LINE_WIDTH=8		20 39
	1778_FCB		MIN_LINE_WIDTH=8		20
	1778_VRNG		MIN_LINE_WIDTH=8		20
LTC3411	LTC3411_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	LTC3411_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
	1_8V_SW	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
	1_8V_SW_F	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	
	1_8V_VFB		MIN_LINE_WIDTH=8		34
	LTC3411_ITH_RC		MIN_LINE_WIDTH=8		34
	LTC3411_ITH		MIN_LINE_WIDTH=8		34
	LTC3411_SYNC		MIN_LINE_WIDTH=8		34
	LTC3411_SHDN		MIN_LINE_WIDTH=8		34
LTC1962 INT PLLS	LTC1962_INT_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	14
CY28512D LMU CONN	J136 +3V_MAIN_SSCG	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	J136 +3V_MAIN_LMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23
OPT DRIVER	J136 +5V_SLEEP_OPT	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24

SIGNAL CONSTRAINTS - PAGE 3

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6809	B
SCALE: NONE	SHT 38 OF 44	

FUNCTIONAL TEST POINTS

PROBES ARE ON BOTTOM SIDE. MINIMUM PAD/HOLE SIZE IS 25 MIL.
FUNC TEST IS ONLY PROPERTY USED BY THE TOOLS. FUNC QTY IS FOR REFERENCE AND LISTS THE NUMBER OF TEST POINTS ON THAT NET AND WITHIN THAT GROUP/CONNECTOR.
FUNC_DIST IS SIMILARLY USED TO DEFINE MAXIMUM DISTANCE FROM A CONNECTOR.

GROUP		SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
SCAN/TEST	J2	JTAG_ASIC_TMS	TRUE			13 26
	J3	JTAG_ASIC_TDI	TRUE			13
	J1	JTAG_ASIC_TDO_TP	TRUE			26
	J4	JTAG_ASIC_TCK	TRUE			13 26
	J6	JTAG_ASIC_TRST_L	TRUE			13 26
	J5	CPU_CHKSTP_OUT_L	TRUE			5
	J7	CPU_SRESET_L	TRUE			5
	J9	CPU_HRESET_L	TRUE			5 6 7
	J8	JTAG_CPU_TMS	TRUE			5 6
	J10	JTAG_CPU_TDI	TRUE			5 6
	J12	JTAG_CPU_TDO_TP	TRUE			5
	J11	JTAG_CPU_TCK	TRUE			5 6
	J13	JTAG_CPU_TRST_L	TRUE			5 6
	J18	INT_JTAG_TEI	TRUE			13
	J20	INT_TST_MONIN_PD	TRUE			13
	J19	INT_TST_MONOUT_TP	TRUE			13
	J21	INT_TST_PLLEN_PD	TRUE			13
INT I2C	J15	INT_I2C_CLK0	TRUE			6 11 13 23
	J14	INT_I2C_DATA0	TRUE			6 11 13 23
	J16	INT_I2C_CLK1	TRUE			13 14 25
	J17	INT_I2C_DATA1	TRUE			13 14 25
PWR/GND	L21	+PBUS	TRUE			38
	L21	+24V_PBUS	TRUE			38
	L25	GPU_VCORE	TRUE			19 20 38
	L24	1778_VFB	TRUE			20 38
	L27	CPU_VCORE_SLEEP	TRUE			5 6 33 38
	L26	VCORE_FB	TRUE			33 38
	L21	+1_8V_MAIN	TRUE			38
	L21	+2_5V_MAIN	TRUE			38
	L21	+5V_MAIN	TRUE	2		38 39
	L22	+5V_SLEEP	TRUE	2		38 39
	L22	+3V_MAIN	TRUE	4		23 38
			TRUE		1000	IN
	L22	+3V_PMU	TRUE			38
CARDBUS	K36	CBUS_DET_1_L	TRUE		2000	18
	K35	CBUS_DET_2_L	TRUE		2000	18
DVI	K37	TMDS_DN<0..2>	TRUE		1000	19 22 37
	K38	TMDS_DP<0..2>	TRUE		1000	19 22 37
	K40	TMDS_CONN_CLKN	TRUE		1000	22 36
	K39	TMDS_CONN_CLKP	TRUE		1000	22 36
	K42	VGA_R	TRUE		1000	22
	K41	VGA_G	TRUE		1000	22
	K44	VGA_B	TRUE		1000	22
	K43	VGA_HSYNC	TRUE		1000	22
	K46	VGA_VSYNC	TRUE		1000	22
	K45	DVI_DDC_CLK_UF	TRUE		1000	22
	K47	DVI_DDC_DATA_UF	TRUE		1000	22
	K48	DVI_HPD_UF	TRUE		1000	22
	K49	+5V_DDC_SLEEP	TRUE		2000	22 38
			TRUE	2	2000	IN
CHGND1			TRUE	6	1000	IN
LVDS	K52	LVDS_L0N	TRUE		1000	20 22 37
	K51	LVDS_L0P	TRUE		1000	20 22 37
	K53	LVDS_L1N	TRUE		1000	20 22 37
	K55	LVDS_L1P	TRUE		1000	20 22 37
	K54	LVDS_L2N	TRUE		1000	20 22 37
	K57	LVDS_L2P	TRUE		1000	20 22 37
	K56	CLKLVDS_LN	TRUE		1000	20 22 37
	K58	CLKLVDS_LP	TRUE		1000	20 22 37
	K59	LVDS_DDC_CLK	TRUE		1000	20 22
	K60	LVDS_DDC_DATA	TRUE		1000	20 22
	K62	+3V_LCD	TRUE	2	2000	22 38
	L22	+3V_SLEEP	TRUE		2000	38 39
			TRUE	2	2000	IN
CHGND4			TRUE	6	1000	IN
INVERTER	K67	+14V_INV	TRUE		2000	22 38
	K66	+5V_INV_SW	TRUE		2000	22 38
	K68	BRIGHT_PWM	TRUE		2000	22
	K24	INV_GND	TRUE		2000	22
			TRUE		1000	IN
S-VIDEO	K70	TV_C	TRUE		2000	22
	K72	TV_Y	TRUE		2000	22
	K71	TV_COMP	TRUE		2000	22
	K73	TV_GND1	TRUE		2000	22 38
	K74	TV_GND2	TRUE		2000	22 38
LIO	K76	INT_I2S0_SND_TO_DAC	TRUE		1000	14 25
	K75	INT_I2S0_SND_LRCLK	TRUE		1000	14 25
	K78	INT_I2S0_SND_MCLK	TRUE		1000	14 25 35
	K83	INT_I2S0_SND_SCLK	TRUE		1000	14 25
	K82	INT_I2S0_SND_FROM_ADC	TRUE		1000	14 25
	K77	SND_HP_MUTE_L	TRUE		1000	14 25
	K79	SND_AMP_MUTE	TRUE		1000	25
	K84	SND_HW_RESET_L	TRUE		1000	14 25
	K85	SND_HP_SENSE_L	TRUE		1000	14 25
	K86	SND_LIN_SENSE_L	TRUE		1000	14 25
	K81	INT_I2C_CLK2	TRUE		1000	14 25
	K80	INT_I2C_DATA2	TRUE		1000	14 25
	K87	ADAPTER_DET	TRUE		1000	25 29
	K88	CHARGE_LED_L	TRUE		1000	25 29
	K89	NEC_LUSB_OCI_UF	TRUE		1000	17 25
	K90	NEC_LUSB_PPON	TRUE		1000	17 25
	L22	+5V_MAIN	TRUE	2	2000	38 39
	L22	+5V_SLEEP	TRUE	2	3000	38 39
	L22	+3V_SLEEP	TRUE		2000	38 39

GROUP		SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
USB	K94	NEC_USB_DAM	TRUE			17 25 37
	K96	NEC_USB_DAP	TRUE			17 25 37
	K95	NEC_USB_DBM	TRUE			17 25 37
	K97	NEC_USB_DBP	TRUE			17 25 37
	K98	BT_USB_DM	TRUE			14 25 37
	K99	BT_USB_DP	TRUE			14 25 37
	K10	MODEM_USB_DM	TRUE			14 25 37
	K10	MODEM_USB_DP	TRUE			14 25 37
RT. USB	K10	NEC_RUSB_PPON	TRUE			17 25
	K10	NEC_RUSB_OCI_UF	TRUE			17 25
WIRELESS	K10	PCI_AD<0..31>	TRUE		1000	9 12 17 18 24 37
	K10	PCI_FRAME_L	TRUE		1000	12 17 18 24 37
	K10	PCI_TRDY_L	TRUE		1000	12 17 18 24 37
	K10	PCI_IRDY_L	TRUE		1000	12 17 18 24 37
	K10	PCI_DEVSEL_L	TRUE		1000	12 17 18 24 37
	K10	PCI_STOP_L	TRUE		1000	12 17 18 24 37
	K11	PCI_PAR	TRUE		1000	12 17 18 24 37
	K11	AIRPORT_PCI_REQ_L	TRUE		1000	12 24
	K11	AIRPORT_PCI_GNT_L	TRUE		1000	12 24
	K11	AIRPORT_PCI_INT_L	TRUE		1000	14 24
	K11	MAIN_RESET_L	TRUE		1000	14 17 18 19 24 29
	K11	CLK33M_AIRPORT	TRUE		1000	12 24 35
	K11	PMU_PME_L	TRUE		1000	14 17 24 29
	K11	ROM_ONBOARD_CS_L	TRUE		1000	9
	K11	ROM_OE_L	TRUE		1000	9 12
	K11	ROM_CS_L	TRUE		1000	9 12
	K11	ROM_RW_L	TRUE		1000	9 12
	K12	RF_DISABLE_L	TRUE		1000	24
	K12	AIRPORT_CLKRUN_L	TRUE		1000	24
	K12	+3V_AIRPORT	TRUE	4	2000	38
			TRUE	6	1000	IN
OPTICAL	K12	EIDE_OPTICAL_DATA<0..15>	TRUE		2000	24 37
	K12	EIDE_OPTICAL_DMA_RQ	TRUE		2000	24 37
	K12	EIDE_OPTICAL_READ_L	TRUE		2000	24 37
	K12	EIDE_OPTICAL_DMAACK_L	TRUE		2000	24 37
	K12	EIDE_OPTICAL_ADDR<0..2>	TRUE		2000	24 37
	K12	EIDE_OPTICAL_CS0_L	TRUE		2000	24 37
	K12	EIDE_OPTICAL_CS1_L	TRUE		2000	24 37
	K13	EIDE_OPTICAL_RST_L	TRUE		2000	24 37
	K13	EIDE_OPTICAL_WR_L	TRUE		2000	24 37
	K13	EIDE_OPTICAL_IOCHRDY	TRUE		2000	24 37
	K13	EIDE_OPTICAL_INT	TRUE		2000	24 37
TRACKPAD	K13	+5V_TPAD_SLEEP	TRUE		3000	23 38
	K13	TPAD_F_TXD	TRUE		3000	23
	K13	TPAD_F_RXD	TRUE		3000	23
	K13	LID_CLOSED_L	TRUE		3000	23
	K13	+3V_HALL_EFFECT	TRUE		3000	23 38
	K13	SOFT_PWR_ON_L	TRUE		3000	22 23 29 33
MODEM/ SERIAL	K14	COMM_RESET_L	TRUE		4000	14 25
	K14	COMM_SHUTDOWN	TRUE		4000	14 25
	K14	COMM_RING_DET_L	TRUE		4000	14 25 29
	K14	COMM_TXD_L	TRUE		4000	14 25
	K14	COMM_TRXC	TRUE		4000	14 25
	K14	COMM_GPIO_L	TRUE		4000	14 25
	K14	COMM_DTR_L	TRUE		4000	14 25
	K14	COMM_RTS_L	TRUE		4000	14 25
	K14	COMM_RXD	TRUE		4000	14 25
KEYBOARD	K14	KBD_ID	TRUE		3000	23 29
	K15	KBD_INTL	TRUE		3000	23
	K15	KBD_JIS	TRUE		3000	23
	K15	KBD_CAPSLOCK_LED	TRUE		3000	23
	K15	KBD_NUMLOCK_LED	TRUE		3000	23
	K15	KBD_FUNCTION_L	TRUE		3000	23 29
	K15	KBD_COMMAND_L	TRUE		3000	23 29
	K15	KBD_OPTION_L	TRUE		3000	23 29
	K15	KBD_CONTROL_L	TRUE		3000	23 29
	K15	KBD_SHIFT_L	TRUE		3000	23 29
	K15	KBD_X<0..9>	TRUE		3000	23 29
	K15	KBD_Y<0..7>	TRUE		3000	23 29
BATTERY	K16	+BATT_POS	TRUE	(100 MIL PROBE PREFERRED)	1000	30 38
	K16	BATT_NEG	TRUE	(100 MIL PROBE PREFERRED)	1000	30 38
	K16	BATT_CLK	TRUE		1000	30
	K16	BATT_DATA	TRUE		1000	30
	K16	PMU_BATT_DET_L	TRUE		1000	29 30
FANS	K16	+FAN_PWR	TRUE		3000	25 38
	K16	FAN1_TACH	TRUE		3000	25
	K16	FAN2_TACH	TRUE		3000	25
	K17	FAN1_GND	TRUE		3000	38
	K17	FAN2_GND	TRUE		3000	38
ETHERNET	K17	MDI_P<0..3>	TRUE		1000	26 37
	K17	MDI_M<0..3>	TRUE		1000	26 37
FIREWIRE	K17	FW_TPO0P	TRUE		1000	27 28 37
	K17	FW_TPO0N	TRUE		1000	27 28 37
	K17	FW_TPO0R	TRUE		1000	28
	K17	FW_TPI0P	TRUE		1000	27 28 37
	K17	FW_TPI0N	TRUE		1000	27 28 37
	K18	+FW_VP0	TRUE		1000	28 38
	K18	FW_VGND	TRUE		1000	39

GROUP		SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
FIREWIRE (CONT.)	K18	FW_TPO1P	TRUE		1000	28 37
	K18	FW_TPO1N	TRUE		1000	28 37
	K18	FW_TPI1P	TRUE		1000	28 37
	K18	FW_TPI1N	TRUE		1000	28 37
	K18	+FW_VP1	TRUE		1000	28 38
	K18	FW_VGND	TRUE		1000	39
DC PWR IN	K18	+ADAPTER	TRUE	3 (100 MIL PROBE PREFERRED)	1000	30 31 38
LMU/ALS	L25	ST7_SLEEP_LED_H	TRUE			23
	L25	PMU_SLEEP_LED	TRUE			23
	L25	PMU_LID_CLOSED_L	TRUE			23 29
	L25	LMU_DETECT	TRUE			23
			TRUE	6	1000	IN
				(100 MIL PROBE PREFERRED)		
MISC.	K19	SLEEP_LED	TRUE			23
	K19	PMU_KB_RESET_L	TRUE			29
	K19	SLEEP	TRUE			23 25 29 32 34
	K19	PMU_CPU_HRESET_L	TRUE			6 29
	K19	BB_RESET_L	TRUE			6
	K24	+3V_PMU_RESET	TRUE			29 33

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6809	B
SCALE: NONE	SHT 39 OF 44	

REVISION HISTORY

Proto/EVT Release

10/27/03 - 1. Schematic originated from Q16 MLB

11/10/03 - 1. Replace U56 symbol
2. Connect OVDDSENSE to MAXBUS_SLEEP
3. Modify SRN0, SRN1 and IARTRXD connection
4. Connect VID1(Page 6) to CPU_VCORE_SLEEP(PAGE 5)
5. Connect SENSEVDD to CPU_VCORE_SLEEP
6. Connect SENSEGND to GND
7. Add 4 pcs 0 ohm resistor for AMD BootRom issue (R1,R194,R236,R271)
8. Connect TEMP_ANODE and TEMP_CATHODE to AD7460
9. Modify CPU PLL config
10. Add 0 ohm resistor on CG_FSEL Interpid side(R450)
11. Replace U47 symbol
12. Change R743 from 2m ohm to 1m ohm
13. Change C774,C781,C788,C793,C797,C802 from 220uF to 330uF
14. Change R748 from 410 ohm to 10 ohm

12/01/03 - 1. Modify CPU_VCORE setting.

12/02/03 - 1. Modify CPU_BTR CPU_VCORE VID setting

12/05/03 - 1. Add CPU_AVDD LDO (Page 5)
2. Change Q45 and Q41 to IRF7805 (376S0035)
3. Change Q47 and Q42 to IRF7811W (376S0104)
4. Change R402 and R409 to 4.7ohm resistors
5. Connect INT_TDO from intrepid to Cypress Chip PD* (U31)

12/12/03 - 1. Add R468 and R601 for MAX1715 2.5V adjust
2. Modify CPU_VCORE setting to Motorola new spec
3. Modify LDO power sequence

12/16/03 - 1. Add 10K pull down for INT_TDO on page 13

12/17/03 - 1. Change LDO Vin from +3V_MAIN to +3V_SLEEP
2. Connect INT_TDO from Intrepid to Marvell 88E1111(U43)
3. Add R755,R756,R758,R759 for power rail

DVT Release (Rev. 02)

01/30/04 - 1. Add Soft Modem(Pin#14) 10K pull-up at J15.7 (Pg 25)
2. Add Bom Table for R97 2.21K ohm VCore offset (Pg 33)

02/04/04 - 1. C811 change to 4.7uF per MOT A7PM requirement (Pg 5)
2. NO STUFF R236,R1,R271&R194 to remove PCI stub (Pg 9)

DVT Release (Rev. 03)

02/12/04 - 1. CPU VCore adjustment for V1.1 A7PM CPU (Pg 33)
2. CPU AVDD adjustment for V1.1 A7PM CPU (Pg 5)
3. ATI INT_TMDS termination change to 0 ohm, Qty:8 (Pg 20)
4. AGP I/O VREF voltage divider chagne to both 1K ohm (Pg 12)

DVT Release (Rev. 04)

02/13/04 - 1. INT. TMDS Termination change to 2* 49.9ohm = 100ohm (Pg 20)

PVT Release (Rev. A)

03/11/04 - 1. INT. TMDS Termination change to 2* 75 ohm = 150ohm (except CLK pair) (Pg 20)
2. USB series termination near NEC PHY change to 47 ohm (Pg 17)

PVT Release (Rev. A - 051-6570)

04/02/04 - 1. USB series termination near NEC PHY change to 43.2 ohm (Pg 17)

Production Release (Rev. A - 051-6653)

04/09/04 - 1. Updated to Apollo 7PM rev 1.1.1 part numbers (Pg 5)
04/09/04 - 2. Updated to production BootROM part number (Pg 9)

Production Release (Rev. B - 051-6653)

04/30/04 - 1. Updated to Fast Intrepid part for 6A ReadMacro Delay value (Pg 8-15)
04/30/04 - 2. Add ATI M11 A16 parts as alternative for A15 parts (Pg 19-21)
04/30/04 - 3. Use new VGA filter to remove ghost image on external VGA display (Pg 22)

Production Release (Rev. C - 051-6653)

05/27/04 - 1. Updated BOM : 113S0006 -> 113S1000
05/27/04 - 2. Updated BOM : 132S0020 -> 132S0100

Production Release (Rev. B - 051-6809)-- mergered with 051-6808

07/07/05 - Added 338S0223 (88E1111 Rev.B1) at U43 and 338S0079 as an alternate
07/08/05 - Added 337S2913 (IC,A7PM,1.33GHZ,1.18VCORE) as an option
07/08/05 - Added label for EEE:SQE
07/08/05 - Replaced 740S0006 with 740S0018 (FUSE,1.5A,24V,SMD,LF) at F3
07/19/05 - Corrected symbols for 337S2838 (MPU),132S0021 (0.47uF,10%) and 138S0511 (2.2uF,10%)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6809	B

SCALE	SHT	OF
NONE	40	44

```
PMU_AC_IN         29B4<>
PMU_BATT0_DET_L   29B4<>
PMU_BATT1_DET_L_PU  29B4<>  29D2<
PMU_BATT_DET_L    29B3<  29D2<  30A4<>  39A3>
PMU_BYTE          29B6<  29C7<
PMU_CAPSLOCK_LED_L  29C6<>
PMU_CHARGE_V      29C4<>  30B8<>
PMU_CHRG_BATT_G   29C4<>  30A8<>
PMU_CLK           14C2<>  29C4<>
PMU_CNVSS         29B6<  29C7<
PMU_CPU_RESET_L   6A2<  6C3<>  29C4<>  39C1>
PMU_EPM           29C4<>  29D2<
PMU_FROM_INT      14C2<>  29C4<>
PMU_I2C_CLK       29B4<>  29C2<
PMU_I2C_DATA      29B4<>  29C2<
PMU_INT_L         14B5<>  14B7<  29B6<>
PMU_INT_NMI       14B5<>  14B7<  29D4<>
PMU_KB_RESET_IN1  29A7<>
PMU_KB_RESET_IN2  29A7<>
PMU_KB_RESET_L    29A6>  29B7<  39C1>
PMU_LID_CLOSED_L  23B3<  23D6<>  29B2<  29C4<>  39D1>
PMU_SMI_BUTTON_L  29C2<  29C4<>
PMU_SMI_L         29C2<  29C4<>
PMU_SUMLOCK_LED_L  29C6<>
PMU_OOPS          29B2<  29B4<>
PMU_PME_L         14A5<>  17A8<  24D5<>  29B2<  29C4<>
                  39C3>
PMU_POWERUP_OK    29B4<>  29D2<
PMU_POWER_UP_L    28C8<>  29C6<>  29D7<  32B8<
PMU_RSQ_L         14B7<  14C2>  29C4<>
PMU_RESET_BUTTON_L  23A7<  29C4<>  29D2<
PMU_RESET_L       29B6<>
PMU_SLEEP_LED     23C7<>  23D6<>  39D1>
PMU_SLEEP_LED_L   23C8<>  29C4<>
PMU_SMB_CLK       29B4<>  29C2<  30A3<
PMU_SMB_DATA      29B4<>  29C2<  30A2<
PMU_TO_INT        14C2<>  29C4<>
POWER_UP          28D7<>
POWER_VALID       29B2<  29C4<>
PWR_BUTTON_L      23A7<  23B4<>
RAM_ADDR<0>       9B4<  11B3<>  11B6<>
RAM_ADDR<12..0>   35A5>
RAM_ADDR<1>       9B4<  11B5<>  11B8<>
RAM_ADDR<2>       9B4<  11B3<>  11B6<>
RAM_ADDR<3>       9B4<  11B5<>  11B8<>
RAM_ADDR<4>       9B4<  11B3<>  11B6<>
RAM_ADDR<5>       9B4<  11B5<>  11B8<>
RAM_ADDR<6>       9B4<  11B3<>  11B6<>
RAM_ADDR<7>       9B4<  11B5<>  11B8<>
RAM_ADDR<8>       9B4<  11B3<>  11B6<>
RAM_ADDR<9>       9A4<  11B5<>  11B8<>
RAM_ADDR<10>      9A4<  11B5<>  11B8<>
RAM_ADDR<11>      9A4<  11B3<>  11B6<>
RAM_ADDR<12>      9A4<  11B5<>  11B8<>
RAM_BA<0>         9A4<  11B5<>  11B8<>
RAM_BA<1..0>      35A5>
RAM_BA<1>         9A4<  11B3<>  11B6<>
RAM_CAS_L         9A4<  11B3<>  11B6<>  35A5>
RAM_CKE<0>        9A4<  9C4<  11C6<>
RAM_CKE<3..0>     35A5>
RAM_CKE<1>        9A4<  9C4<  11CB<>
RAM_CKE<2>        9A4<  9C4<  11C3<>
RAM_CKE<3>        9A4<  9C4<  11C5<>
RAM_CS_L<0>       9C4<  11B8<>
RAM_CS_L<3..0>    35A5>
RAM_CS_L<1>       9C4<  11B6<>
RAM_CS_L<2>       9C4<  11B5<>
RAM_CS_L<3>       9C4<  11B3<>
RAM_DATA_A<0>     10C8<>  11D8<>
RAM_DATA_A<7..0>  35D5>
RAM_DATA_A<1>     10C8<>  11D8<>
RAM_DATA_A<2>     10C8<>  11D8<>
RAM_DATA_A<3>     10B8<>  11D8<>
RAM_DATA_A<4>     10B8<>  11D6<>
RAM_DATA_A<5>     10B8<>  11D6<>
RAM_DATA_A<6>     10B8<>  11D6<>
RAM_DATA_A<7>     10B8<>  11D6<>
RAM_DATA_A<8>     10B8<>  11D8<>
RAM_DATA_A<15..8>  35C5>
RAM_DATA_A<9>     10C7<>  11D8<>
RAM_DATA_A<10>    10C7<>  11D8<>
RAM_DATA_A<11>    10C7<>  11D8<>
RAM_DATA_A<12>    10C7<>  11D6<>
RAM_DATA_A<13>    10C7<>  11D6<>
RAM_DATA_A<14>    10C7<>  11D6<>
RAM_DATA_A<15>    10C7<>  11D6<>
RAM_DATA_A<16>    10C6<>  11D8<>
RAM_DATA_A<23..16>  35C5>
RAM_DATA_A<17>    10C6<>  11C8<>
RAM_DATA_A<18>    10C6<>  11C8<>
RAM_DATA_A<19>    10C6<>  11C8<>
RAM_DATA_A<20>    10C6<>  11D3<>
RAM_DATA_A<21>    10C6<>  11C3<>
RAM_DATA_A<22>    10C6<>  11C3<>
RAM_DATA_A<23>    10C6<>  11C3<>
RAM_DATA_A<24>    10C6<>  11C5<>
```

```
RAM_DATA_B<25..24>  35C5>
RAM_DATA_B<25>    10C6<>  11C5<>
RAM_DATA_B<26>    10C6<>  11C5<>  35C5>
RAM_DATA_B<27>    10C6<>  11C5<>
RAM_DATA_B<31..27>  35C5>
RAM_DATA_B<28>    10C6<>  11C3<>
RAM_DATA_B<29>    10C6<>  11C3<>
RAM_DATA_B<30>    10C6<>  11C3<>
RAM_DATA_B<31>    10C6<>  11C3<>
RAM_DATA_B<32>    10D4<>  11B5<>
RAM_DATA_B<39..32>  35B5>
RAM_DATA_B<33>    10C4<>  11B5<>
RAM_DATA_B<34>    10C4<>  11B5<>
RAM_DATA_B<35>    10C4<>  11B5<>
RAM_DATA_B<36>    10C4<>  11B3<>
RAM_DATA_B<37>    10C4<>  11B3<>
RAM_DATA_B<38>    10C4<>  11B3<>
RAM_DATA_B<39>    10C4<>  11B3<>
RAM_DATA_B<40>    10C4<>  11B5<>
RAM_DATA_B<47..40>  35B5>
RAM_DATA_B<41>    10C4<>  11B5<>
RAM_DATA_B<42>    10C4<>  11A5<>
RAM_DATA_B<43>    10C4<>  11A5<>
RAM_DATA_B<44>    10C4<>  11B3<>
RAM_DATA_B<45>    10C4<>  11B3<>
RAM_DATA_B<46>    10C4<>  11A3<>
RAM_DATA_B<47>    10C4<>  11A3<>
RAM_DATA_B<48>    10D2<>  11A5<>
RAM_DATA_B<55..48>  35B5>
RAM_DATA_B<49>    10C2<>  11A5<>
RAM_DATA_B<50>    10C2<>  11A5<>
RAM_DATA_B<51>    10C2<>  11A5<>
RAM_DATA_B<52>    10C2<>  11A3<>
RAM_DATA_B<53>    10C2<>  11A3<>
RAM_DATA_B<54>    10C2<>  11A3<>
RAM_DATA_B<55>    10C2<>  11A3<>
RAM_DATA_B<56>    10C2<>  11A5<>
RAM_DATA_B<63..56>  35A5>
RAM_DATA_B<57>    10C2<>  11A5<>
RAM_DATA_B<58>    10C2<>  11A5<>
RAM_DATA_B<59>    10C2<>  11A5<>
RAM_DATA_B<60>    10C2<>  11A3<>
RAM_DATA_B<61>    10C2<>  11A3<>
RAM_DATA_B<62>    10C2<>  11A3<>
RAM_DATA_B<63>    10C2<>  11A3<>
RAM_DQM_A<0>      10B8<>  11D6<>  35D5>
RAM_DQM_A<1>      10C7<>  11D6<>  35C5>
RAM_DQM_A<2>      10B6<>  11C6<>  35C5>
RAM_DQM_A<3>      10C5<>  11C6<>  35C5>
RAM_DQM_A<4>      10B4<>  11B6<>  35B5>
RAM_DQM_A<5>      10C3<>  11B6<>  35B5>
RAM_DQM_A<6>      10B2<>  11A6<>  35B5>
RAM_DQM_A<7>      10C1<>  11A6<>  35A5>
RAM_DQM_B<0>      10C8<>  11D3<>  35D5>
RAM_DQM_B<1>      10C8<>  11D3<>  35C5>
RAM_DQM_B<2>      10C6<>  11C3<>  35C5>
RAM_DQM_B<3>      10C6<>  11C3<>  35C5>
RAM_DQM_B<4>      10C4<>  11B3<>  35B5>
RAM_DQM_B<5>      10C4<>  11B3<>  35B5>
RAM_DQM_B<6>      10C2<>  11A3<>  35B5>
RAM_DQM_B<7>      10C2<>  11A3<>  35A5>
RAM_DQS_A<0>      10B8<>  11D8<>  35D5>
RAM_DQS_A<1>      10C7<>  11D8<>  35C5>
RAM_DQS_A<2>      10B6<>  11C8<>  35C5>
RAM_DQS_A<3>      10C5<>  11C8<>  35C5>
RAM_DQS_A<4>      10B4<>  11B8<>  35B5>
RAM_DQS_A<5>      10C3<>  11B8<>  35B5>
RAM_DQS_A<6>      10B2<>  11A8<>  35B5>
RAM_DQS_A<7>      10C1<>  11A8<>  35A5>
RAM_DQS_B<0>      10C8<>  11D5<>  35D5>
RAM_DQS_B<1>      10C8<>  11D5<>  35C5>
RAM_DQS_B<2>      10C6<>  11C5<>  35C5>
RAM_DQS_B<3>      10C6<>  11C5<>  35C5>
RAM_DQS_B<4>      10B4<>  11B5<>  35B5>
RAM_DQS_B<5>      10C4<>  11B5<>  35B5>
RAM_DQS_B<6>      10C2<>  11A5<>  35B5>
RAM_DQS_B<7>      10C2<>  11A5<>  35A5>
RAM_RAS_L         9A4<  11B3<>  11B6<>  35A5>
RAM_WE_L          9A4<  11B5<>  11B8<>  35A5>
RESET_VREF        6C3<>
RF_DISABLE_L      24D6<>  39C3>
ROM_CS_L          9B3<  12A4<  39C3>
ROM_CS_TP_L       9C3<  24B6<>
ROM_OE_L          9B3<  12A4<  39C3>
ROM_OE_TP_L       9B3<  24C5<>
ROM_ONBOARD_CS_L  9B3<  39C3>
ROM_ONBOARD_CS_TP_L  9B3<  24C6<>
ROM_RW_L          9B3<  12A4<  39C3>
ROM_RW_TP_L       9B3<  24C6<>
ROM_WP_L          9B3<
SI_A2             19C4<
SI_EXT_SWING_SET  19C2<>
SI_HPD            19C4<
SI_I2C_CLK        19D4<  20C5<>
SI_I2S_DATA       19C4<  20C5<>
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SI_PD_L           19C4<
SI_RST_L          19C4<
SI_TMDS_CLKN      19C2<  19C2<>  36D1>
SI_TMDS_CLKP      19C2<>  19C2<  36D1>
SI_TMDS_CLK_STM   19D1<
SI_TMDS_D0_STM    19D1<
SI_TMDS_D1_STM    19D1<
SI_TMDS_D2_STM    19C1<
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SI_TMDS_DN<1>     19B2<  19C2<>  36D1>
SI_TMDS_DN<2>     19B2<  19C2<>  36C1>
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SI_TMDS_DP<2>     19B2<  19C2<>  36C1>
SI_VREF_ICOR_N    19C2<  19C4<
SLEEP             23D7<>  25D7<>  29B6<>  29D7<  32A4<
                  32A6<  32B3<  32B8<>  34B3<  34C2<  39C1>
SLEEP_LED         23C3<>  39C1>
SLEEP_LED_DGND    23C3<>
SLEEP_LED_I       23D3<
SLEEP_LED_L       23D4<
SLEEP_LED_SW_L    23D4<>
SLEEP_LED_UF      23D3<
SLEEP_LS5         32A4<>  32A8<
SLEEP_LS5_EN_L    32A5<>
SLEEP_L_LS5       18D5<  20A7<>  26A8<>  32A5<>  33C7<>
                  34C8<
SLEEP_L_LS5_EN_L  32A6<>
SLEEP_L_LS5_INV   34A3<  34C2<  34C8<>
SLEEP_L_LS5_NET   32B3<>  34C8<>
SLEEP_NET         32A3<>
SLEEP_NET_INV     32A3<>
SND_AMP_MUTE      25C7<>  25D6<>  39A6>
SND_AMP_MUTE_CTRL  25B5<>  25D6<>
SND_AMP_MUTE_L    14B5<>  25D5<>
SND_HP_MUTE       25C5<>
SND_HP_MUTE_L     14C5<>  25C5<>  39A6>
SND_HP_MUTE_LO    25C6<>  25C7<>
SND_HP_SENSE_L    14B5<>  25C8<>  39A6>
SND_HW_RESET_L    14A7<  14B5<>  25D7<>  39A6>
SND_LIN_SENSE_L   14B5<>  25C8<>  39A6>
SOFT_PWR_ON_L     22D1<>  23A5<  29A8<  29C6<>  29D7<
                  33A4<>  39B3>
ST7_SLEEP_LED_H   23C5<>  23C6<>  23D6<>  39D1>
STOP_ASP_L        12D2<  12D4<>
SYSCLK_CPU        5C3<  8A6<  35D1>
SYSCLK_CPU_UF     8A5<>  35D1>
SYSCLK_DDRCLK_A0  9D4<  11D8<>  35D1>
SYSCLK_DDRCLK_A0_L  9D4<  11D8<>  35C1>
SYSCLK_DDRCLK_A0_L_UF  9B6<>  9D5<  35D1>
SYSCLK_DDRCLK_A0_UF  9B6<>  9D5<  35D1>
SYSCLK_DDRCLK_A1  9D4<  11A6<>  35C1>
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SYSCLK_DDRCLK_A1_UF  9B6<>  9D5<  35D1>
SYSCLK_DDRCLK_B0  9D4<  11D5<>  35C1>
SYSCLK_DDRCLK_B0_L  9C4<  11D5<>  35C1>
SYSCLK_DDRCLK_B0_L_UF  9B6<>  9C5<  35D1>
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SYSCLK_DDRCLK_B1  9D4<  11A3<>  35C1>
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SYSCLK_DDRCLK_B1_L_UF  9B6<>  9D5<  35D1>
SYSCLK_DDRCLK_B1_UF  9B6<>  9D5<  35D1>
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SYSTEM_CLK_EN     14A5<  14B6<  29C4<>
THERM1_A_DM       25A7<  25A8<  37A2>
THERM1_A_DP       25A7<  25A8<  37A2>
THERM1_DM         25A5<  25A6<  25B5<>  25B6<  37A2>
THERM1_DP         25A6<  25A6<  25B5<>  25B6<  37A2>
THERM1_M_DM       25B7<  25B8<  37A2>
THERM1_M_DP       25B7<  25B8<  37A2>
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THERM2_A_DP       25A7<  25A8<  37A2>
THERM2_DM         25A5<  25A6<  25B5<>  25B6<  37A2>
THERM2_DP         25A5<  25A6<  25B5<>  25B6<  37A2>
THERM2_M_DM       25B7<  25B8<  37A2>
THERM2_M_DP       25B7<  25B8<  37A2>
THERM_INV         25B1<>
THERM_L_OC        25B1<>  29B4<>
TMDS_CLKN         19B1<  19C1<  19D1<  22C8<>  37C2>
TMDS_CLKP         19B1<  19C1<  19D2<  22C8<>  37C2>
TMDS_CONN_CLKN    22C7<>  22C7<>  36C1>  39C6>
TMDS_CONN_CLKP    22C7<>  22C7<>  36C1>  39C6>
TMDS_CONN_DN<0>   22D6<>  36C1>
TMDS_CONN_DN<1>   22D6<>  36B1>
TMDS_CONN_DN<2>   22D6<>  36B1>
TMDS_CONN_DP<0>   22D6<>  36C1>
TMDS_CONN_DP<1>   22D6<>  36B1>
TMDS_CONN_DP<2>   22D6<>  36B1>
TMDS_DN<0>        19B1<  19C1<  19D1<  22D7<>  37C2>
TMDS_DN<0..2>     39C6>
TMDS_DN<1>        19B1<  19B1<  19C1<  22D5<>  37B2>
TMDS_DN<2>        19A1<  19B1<  19C1<  22D5<>  37B2>
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TMDS_DP<0..2>     39C6>
TMDS_DP<1>        19B1<  19B1<  19C2<  22C5<>  37B2>
TMDS_DP<2>        19A1<  19B1<  19C2<  22D5<>  37B2>
TPAD_F_RXD        23B5<>  39B3>
TPAD_F_TXD        23B5<>  39B3>
TPAD_RXD          23A6<  29C2<  29C4<>
TPAD_TXD          23B6<  29B2<  29C4<>
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TV_C              22A6<>  39A6>
TV_COMP           22A6<>  39A6>
TV_GND1           22B6<>  38B6>  39A6>
TV_GND2           22A6<>  38B6>  39A6>
TV_Y              22A6<>  39A6>
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UIDE_ADDR<2..0>   37C5>
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UIDE_CS1_L        13C7<  24B4<  37C5>
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UIDE_DATA<15>     13D7<  24B4<
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UIDE_DIOW_L       13C7<  24A4<  37C5>
UIDE_DMACK_L      13C7<  24A4<  37C5>
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UIDE_IOCHRDY      13C7<  24A4<  37C5>
UIDE_REF          13C7<>  38C3>
UIDE_RST_L        13C7<  24A4<  37C5>
USB_DAN           14B2<>  14D2<
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USB_DBN           14B2<>  14D2<
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USB_DCN           14B2<>  14D2<
USB_DCP           14B2<>  14D2<
USB_DDN           14B2<>  14D2<
USB_DDP           14B2<>  14C2<
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USB_DEP           14B2<>  14C2<  37B2>
USB_DFN           14B2<  14B2<>  37B2>
USB_DFP           14B2<>  14C2<  37B2>
USB_OC_AB_L       14B2<  14C7<
USB_OC_CD_L       14B2<  14C7<
USB_OC_EF_L       14B2<  14C7<
USB_PWREN_AB_L    14B2<>  14C7<
USB_PWREN_CD_L    14B2<>  14C7<
USB_PWREN_EF_L    14B2<>  14C7<
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VCORE_AB_SEL_INV  33A7<>
VCORE_AB_SEL_OPT  33A6<>
VCORE_BOOST       33C4<>  38C1>
VCORE_BST         33C5<>  38C1>
VCORE_CC          33B6<>  38C1>
VCORE_D0          33A3<>
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VCORE_GNDDIV      33A5<  33A5<  38B1>
VCORE_GNDDIV_TEST  33A4<>
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VCORE_GNDSNS_TEST  33A4<>
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VCORE_LX          33B5<>  38C1>
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VCORE_REF         33B6<>  38C1>
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VCORE_TIME        33B4<>  38B1>
VCORE_TON         33B6<  38C1>
VCORE_VCC         33C6<  38C1>
VCORE_VGATE       14B5<  14B7<  33B4>  38B1>
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VCORE_VID<1>      33B7<  33D3<  33D4>
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VCORE_VID<4>      33B7<  33D3<  33D4>
VCORE_VSENSE      33C2<>
VGA_B             22C6<>  22C7<  39B6>
VGA_G             22C5<>  22C7<  39B6>
VGA_HSYNC         22C6<>  22D7<  39B6>
VGA_R             22B7<  22C5<>  39B6>
VGA_VSYNC         22C5<>  22D7<  39B6>
XT10_SPN          4C2<>
XT301_SPN         4C2<>
XT302_SPN         4C2<>
XV_LCDATA20_PU    20C7<>
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6809	B
SCALE: NONE	SHT 42 OF 44	

*** Part Cross-Reference for the entire design ***

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RP3	RPAX4P	8
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RP42	RPAX10P2C	23
RP43	RPAX4P	17
RP44	RPAX4P	17
RP45	RPAX4P	17
RP46	RPAX10P2C	6
RP47	RPAX4P	14
RP49	RPAX4P	19
RP50	RPAX4P	19
RP51	RPAX4P	19
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RP56	RPAX2P	19
RP57	RPAX2P	19
RP58	RPAX2P	19
RP59	RPAX2P	19
RP60	RPAX4P	19
SH1	SHLD_3P_KMI	4
U1	COMPARATOR_LMC7211	30
U2	NC7S32	22
U3	AMP_MAX4172	30
U4	PWR_CNTRL_TPS2211	18
U5	FAN2558	5
U6	MAX1772	30
U7	MAX1717	33
U8	PCI1510GGU	18
U9	SN74AUC1G08	6
U10	SN74AUC1G08	6
U11	FEPR_1MX8	9
U12	SN74AUC1G04	7
U13	LTC1625	31
U14	COMPARATOR_LMC7211	31
U15	PI3B3257	33
U16	CBTV4020	10
U17	UPD720101_FBGA	17
U18	CBTV4020	10
U19	MAX1715	34
U20	NC7S32	29
U21	741125	23
U22	VREG_LP2951	31
U23	VREG_LP2951	31
U24	NC7S32	29
U25	NC7S32	29
U26	MAX6804	29
U27	CBTV4020	10
U28	CBTV4020	10
U29	M16C62	29
U30	CLK_GEN_CY25811	19
U31	CLK_GEN_CY28512	14
U32	LTC1778	20
U33	COMPARATOR_LMC7211	29
U34	VREG_MM1571J	21
U35	LTC3707	32

U36	TSB81BA3A	27
U37	VREG_LM2594	27
U38	VREG_LT1962	27
U39	741G32	22
U40	741G32	22
U42	COMPARATOR_LMC7211	22
U43	TRANSCEIVER_88E1111	26
U44	LTC1761	27
U45	LTC3405	26
U46	LTC3411	34
U47	BAGE_HBLTY_M11_CSP64_667	19 20 21
U48	TRA_SI4467BDQ	34
U49	VREG_LT1962	14
U50	TRA_SI3447DV	34
U51	INTREPID	8 9 12 13 14 15
U52	EEPROM_32KX8_M24256B	6
U53	ADT7460	25
U54	AT90S1200	6
U55	OPAMP_LMC7111	30
U56	APOLLO_MPC7447A_360	5 6
U57	COMPARATOR_LMC7211	30
U58	SIL1162	19
U60	VREG_MM1571J	21
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XW31	SHORT	32
XW32	SHORT	32
XW34	SHORT	5
Y1	CRYSTAL	17
Y2	CRYSTAL	14
Y3	CRYSTAL_4PIN	29
Y4	CRYSTAL	29
Y5	CRYSTAL_4PIN	26
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