

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

DRAWING		CK APPD	ENG APPD
REV	ZONE	ECN	DESCRIPTION OF CHANGE
B		397477	PRODUCTION RELEASED
			DATE
			08/31/05 ?

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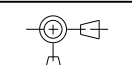
SCHEM, MLB, PB15

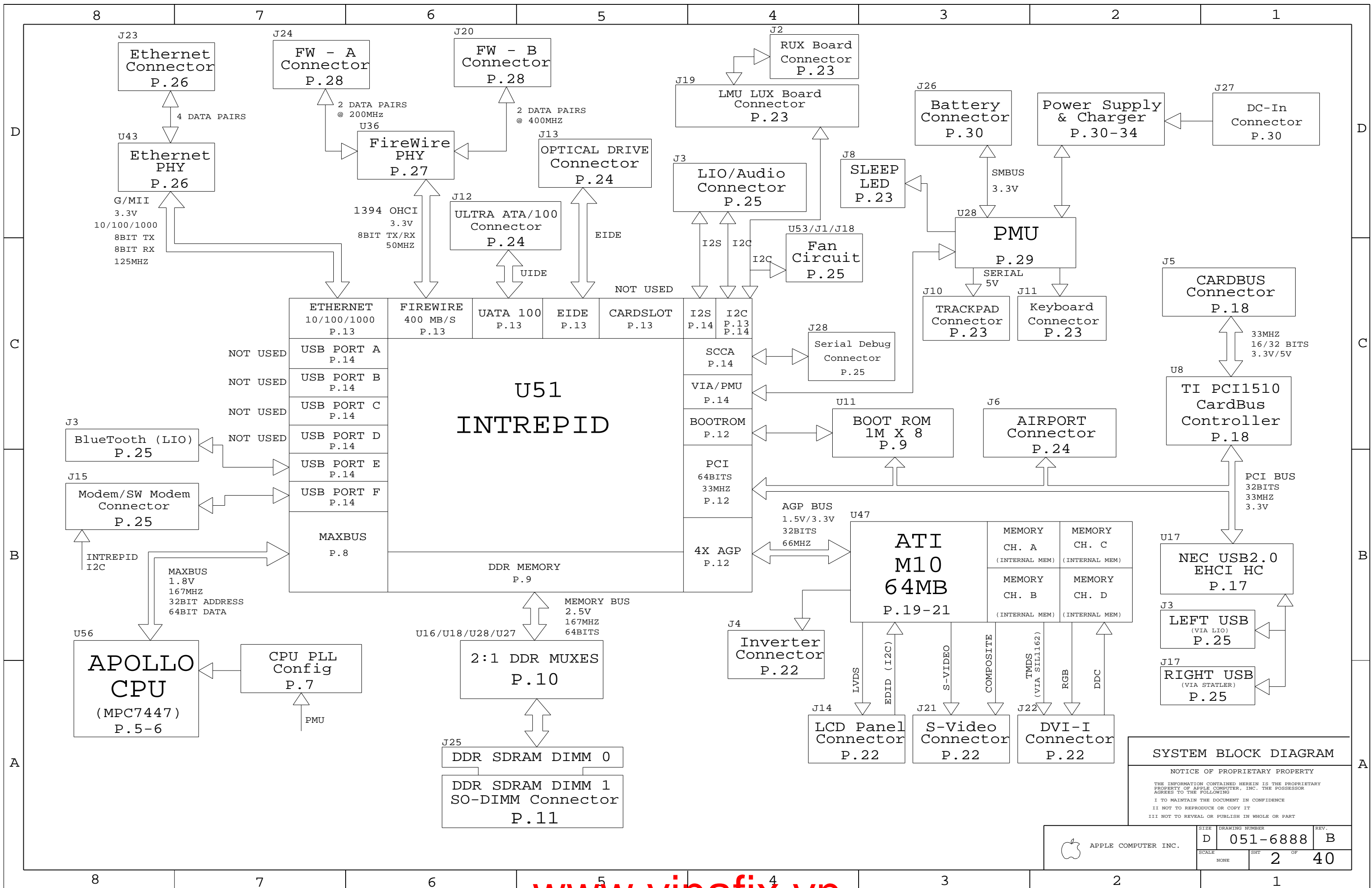
Mon Aug 29 19:19:29 2005

BOM OPTIONS (IN COMMON PARTS)

STUFF	NO STUFF
1_8V_MAXBUS	1_5V_MAXBUS
SSCG	NO_SSCG
5V_HD_LOGIC	3V_HD_LOGIC
NO_BBANG	BBANG
INT_2_5V_COLD	INT_2_5V_HOT
ATI_MEMIO_HI	ATI_MEMIO_LO
USB_MODEM	SOFT_MODEM
GPU_PWRMSR	INT_TMDS
GPU_SS	
VGA_BUFFER_RES	
EXT_TMDS	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6888	1	SCHEM,MLB,PB15	SCH1	
820-1441	1	PCBF,MLB,PB15	PCB1	
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6MM	EEE:T9Q	DMS630-7112
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6MM	EEE:T9R	DMS630-7113

DIMENSIONS ARE IN MILLIMETERS		METRIC		Apple Computer Inc.	
XX :	_____	DRAPTR	DESIGN CK	NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	
X.XX :	_____	ENG APPD	MFG APPD		
X.XXX :	_____	QA APPD	DESIGNER		
ANGLES :	_____	RELEASE	SCALE		
DO NOT SCALE DRAWING		SCALE NONE		TITLE	
 THIRD ANGLE PROJECTION		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE D DRAWING NUMBER 051-6888 REV. B	
				SHT 1 OF 40	

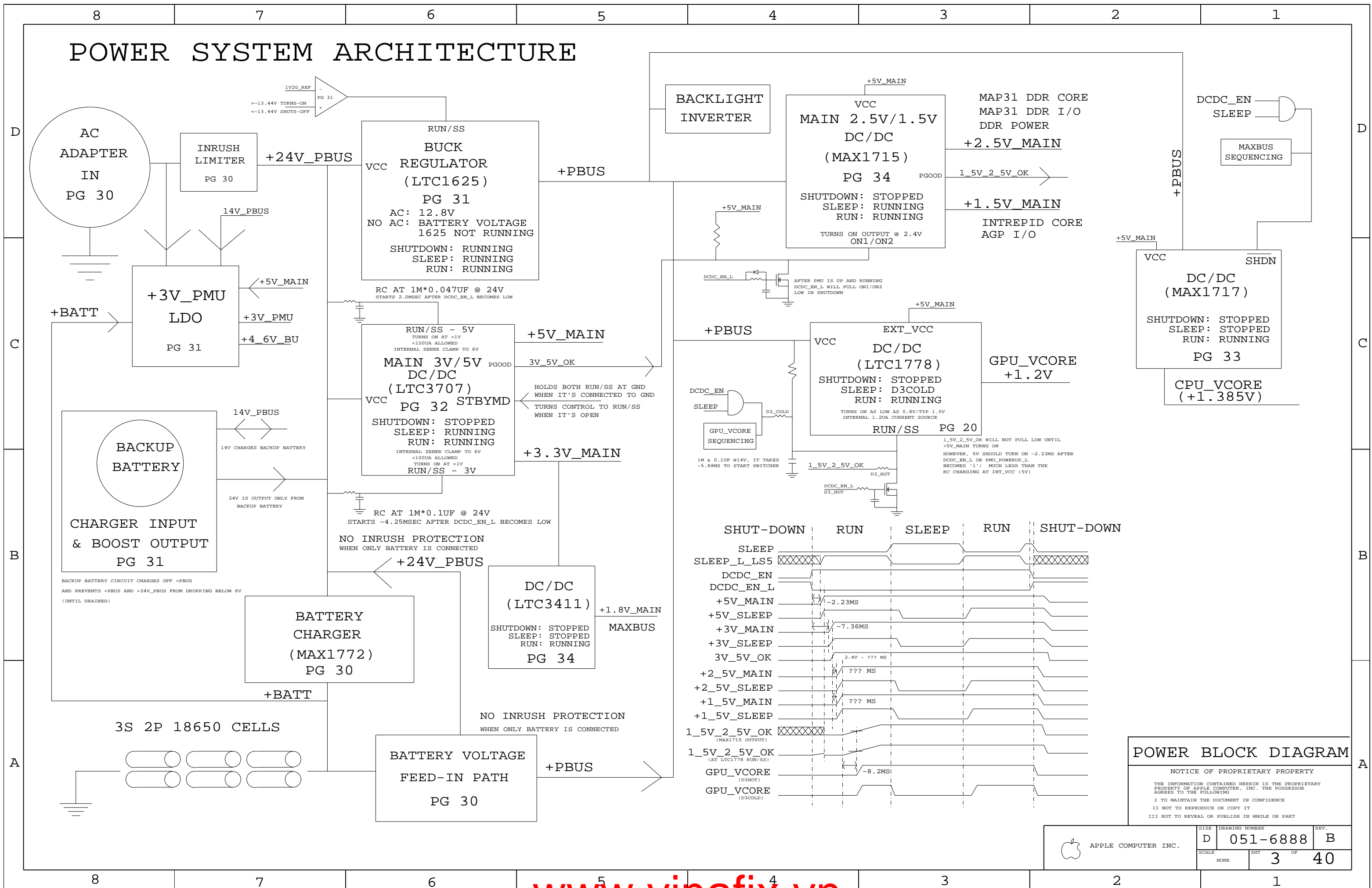


SYSTEM BLOCK DIAGRAM

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	D	051-6888	B
SCALE	NONE	SHT	2 OF 40

POWER SYSTEM ARCHITECTURE



POWER BLOCK DIAGRAM

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	D	051-6888	B
SCALE	SHT 3 OF 40		
NONE			

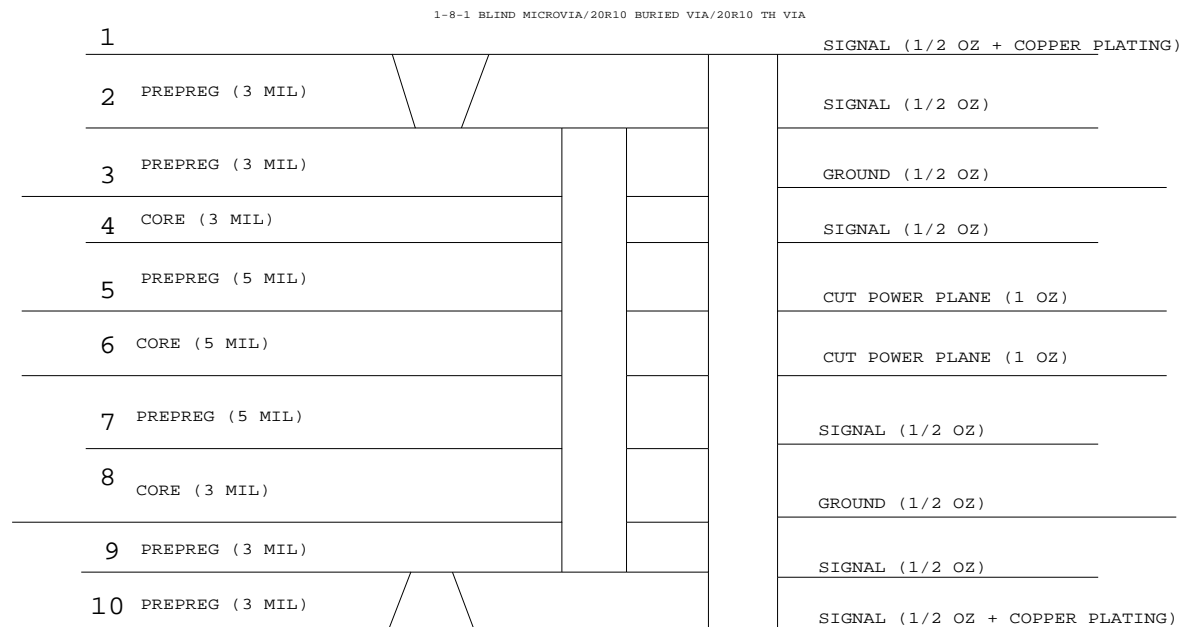
PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
 1/2 OZ CU THICKNESS: 0.7 MILS
 1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
 DIELECTRIC: FR-4
 LAYER COUNT: 10
 SIGNAL TRACE WIDTH: 4 MILS
 SIGNAL TRACE SPACING: 4 MILS
 PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

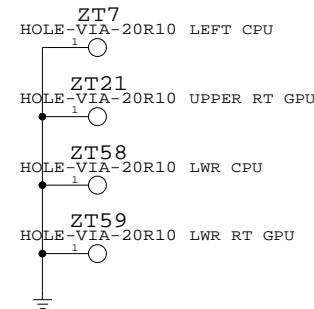
BOARD STACK-UP AND CONSTRUCTION



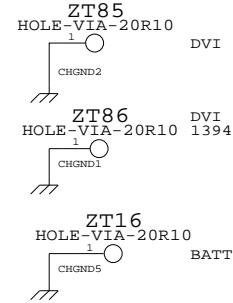
BOARD HOLES

CHASSIS MOUNTS

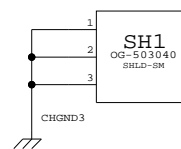
ASICS HEATSINK MOUNTS



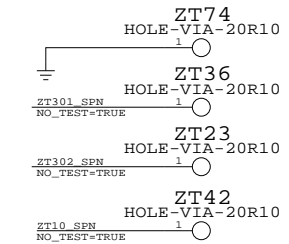
I/O AREA



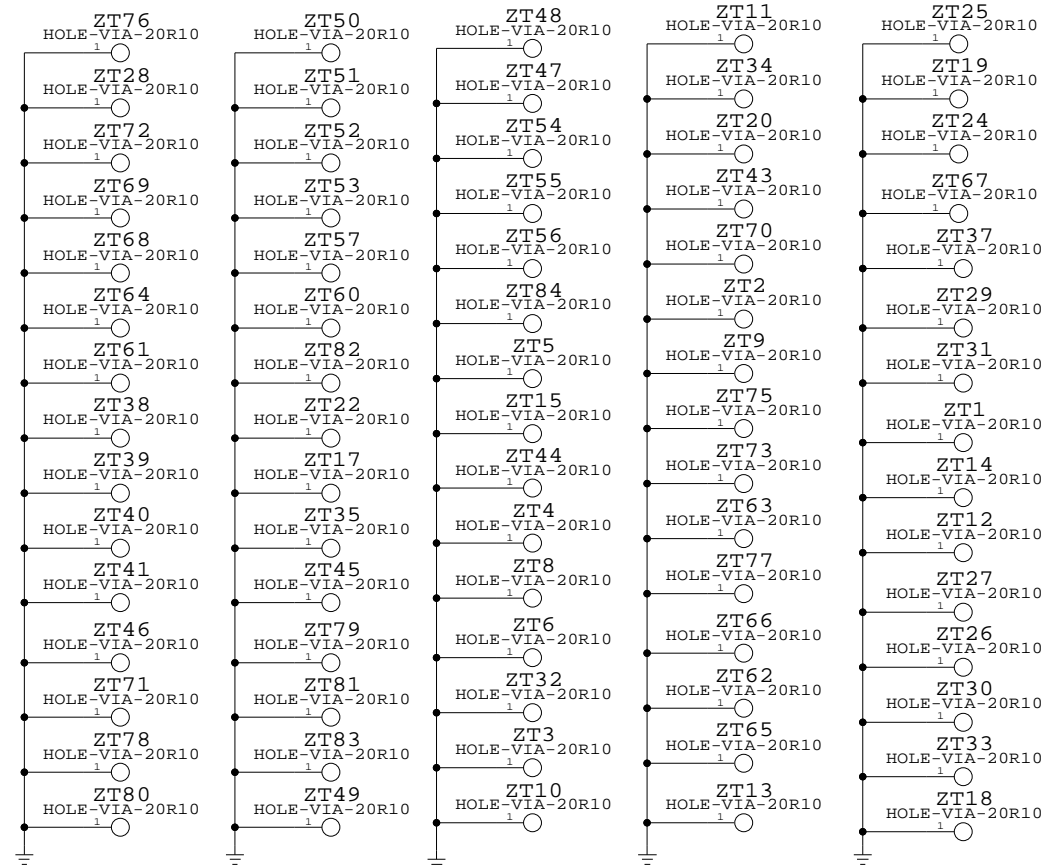
INVERTER



MECH. HOLES



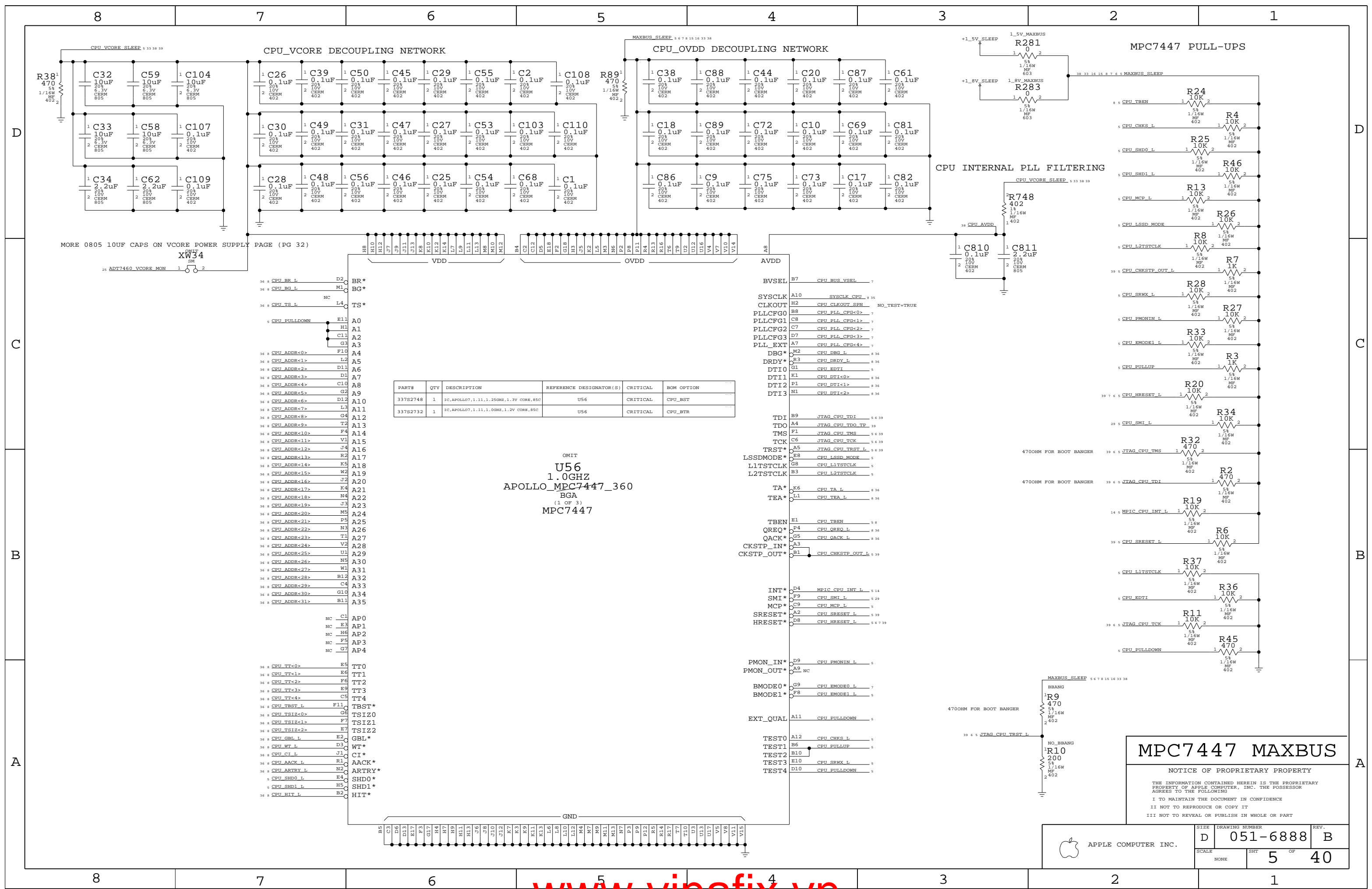
GROUND VIAS



BOARD INFORMATION

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SCALE	SHEET		OF
NONE	4		40



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33782748	1	IC, APOLLO7, 1.11, 1.25GHZ, 1.3V CORE, 85C	U56	CRITICAL	CPU_BST
33782732	1	IC, APOLLO7, 1.11, 1.0GHZ, 1.2V CORE, 85C	U56	CRITICAL	CPU_BTR

OMIT
 U56
 1.0GHZ
 APOLLO_MPC7447_360
 BGA
 (1 OF 3)
 MPC7447

MPC7447 MAXBUS

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	SCALE NONE	SHEET 5 OF 40	

8

7

6

5

4

3

2

1

D

D

C

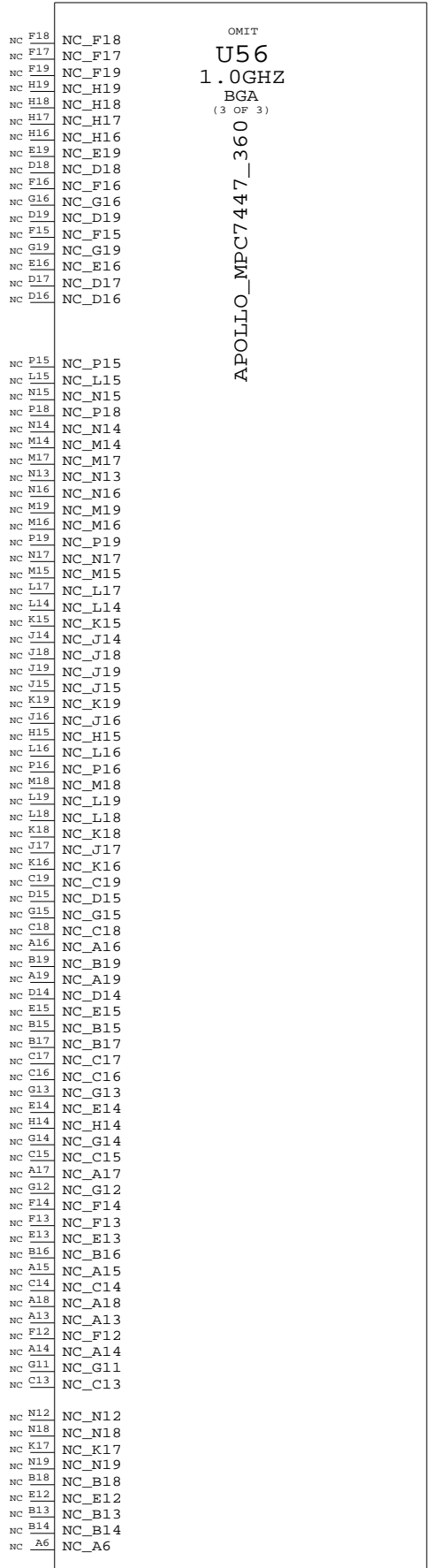
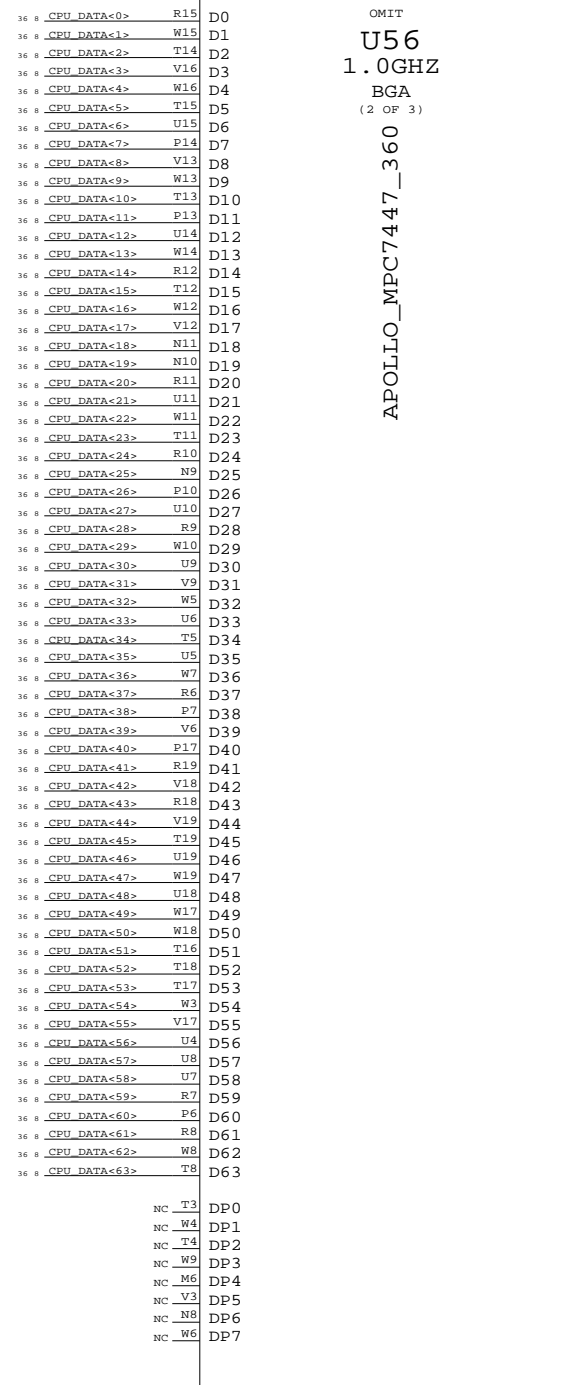
C

B

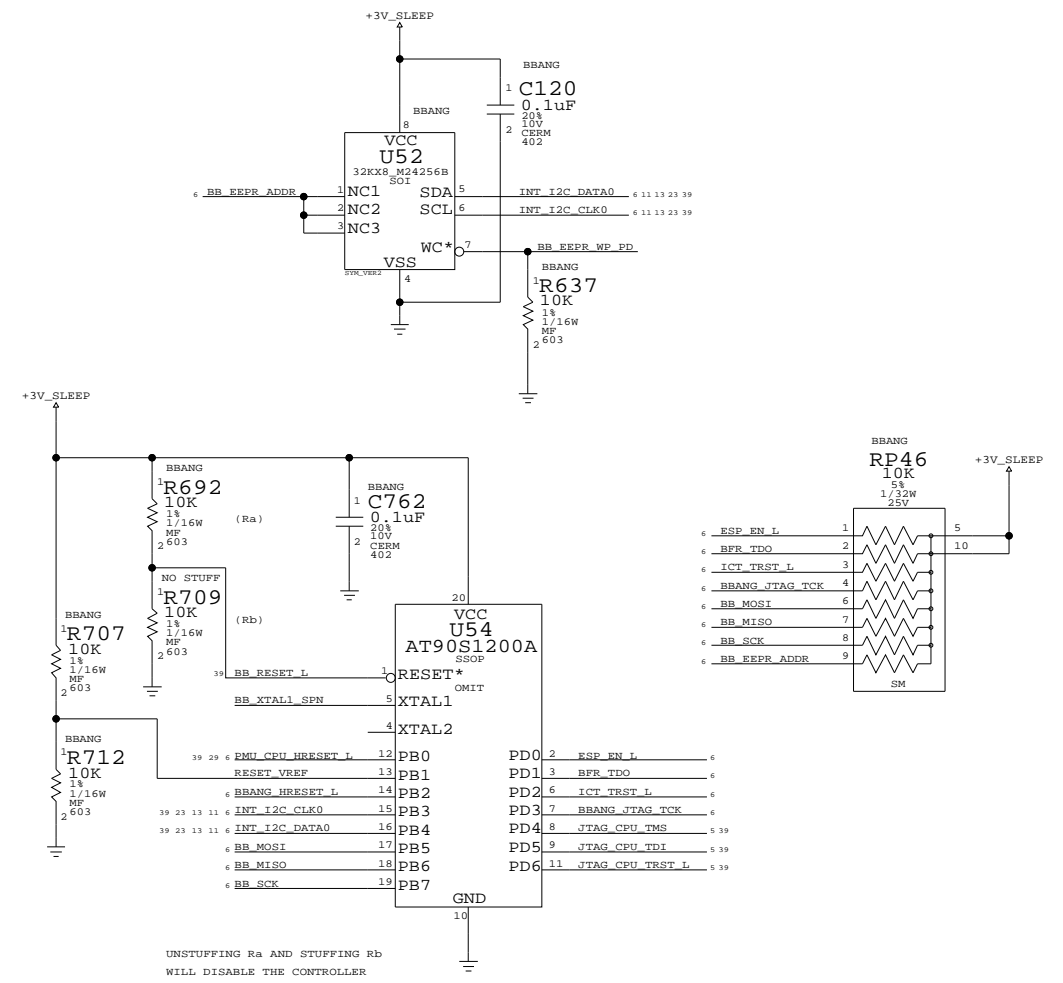
B

A

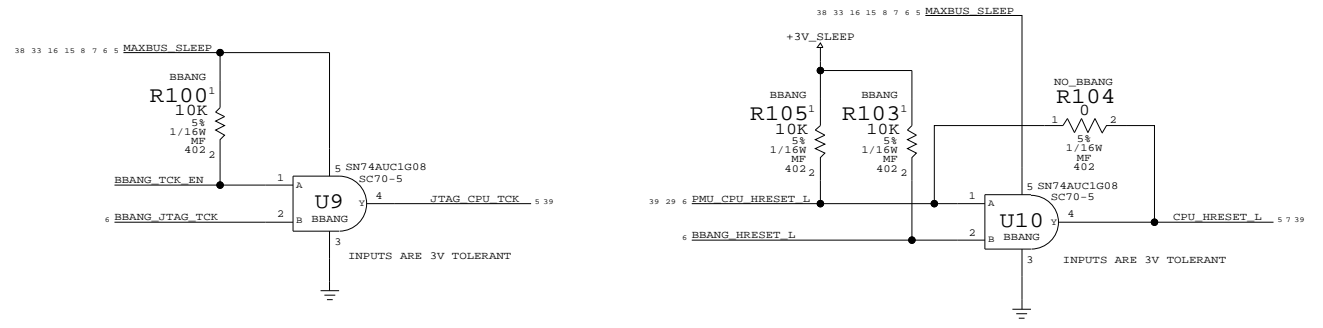
A



BOOT BANGER - TWEAK PROCESSOR BITS AFTER POWER-ON



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1135	1	009-6240 FW GT4 BBANGER MCU, PROGRAMMED W/ BBANGER	U54	BBANG



MPC7447 / BBANG

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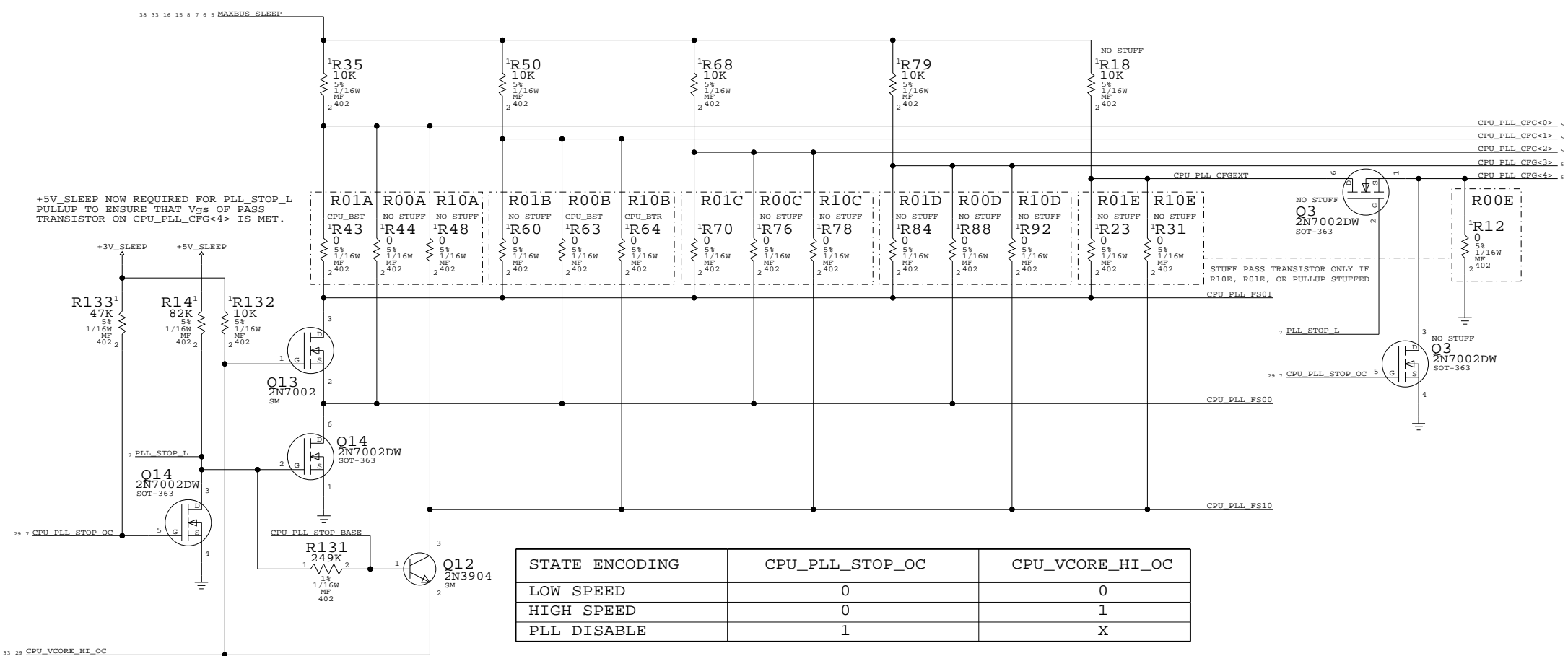
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6888	B
SCALE	NONE	SHT	OF
		6	40

CPU PLL CONFIG CIRCUITRY

CPU FREQUENCY CONFIGURATION

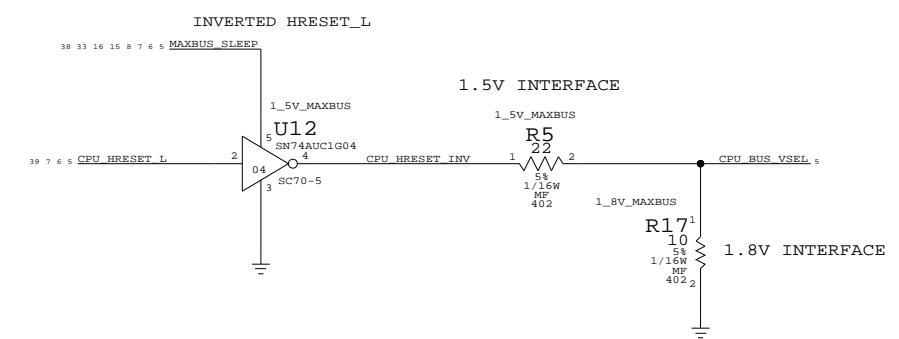
APOLLO 7



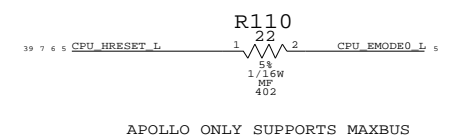
MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY)		CPU_PLL_CFG 4 0123 E ABCD HEX
	167MHZ	133MHZ	
0.0X	PLL OFF		0 1111 0F
1.0X	PLL BYPASS		0 0011 03
2.0X	333	267	0 0100 04
3.0X	500	400	0 1000 08
4.0X	667	533	0 1010 0A
5.0X	833	667	0 1011 0B
5.5X	917	733	0 1001 09
6.0X	1000	800	0 1101 0D
6.5X	1083	867	0 0101 05
7.0X	1167	933	0 0010 02
7.5X	1250	1000	0 0001 01
8.0X	1333	1067	0 1100 0C
8.5X	1417	1133	0 0110 06
9.0X	1500	1200	1 0111 17
9.5X	1583	1267	0 0111 07
10.0X	1667	1333	1 1010 1A
10.5X	1750	1400	1 1000 18
11.0X	1833	1467	1 1001 19
11.5X	1917	1533	0 0000 00
12.0X	2000	1600	1 1011 1B
12.5X	2083	1667	1 1111 1F
13.0X	2167	1733	1 0101 15
13.5X	2250	1800	0 1110 0E
14.0X	2333	1867	1 1100 1C
15.0X	2500	2000	1 0001 11
16.0X	2667	2133	1 1101 1D
17.0X	2833	2267	1 0000 10
18.0X	3000	2400	1 0010 12
20.0X	3333	2667	1 0011 13
21.0X	3500	2800	1 0100 14
24.0X	4000	3200	1 0110 16
28.0X	4667	3733	1 1110 1E

CPU CONFIGURATION

MAXBUS VSEL



BUSTYPE SELECT



APOLLO ONLY SUPPORTS MAXBUS

DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L
NEED TO CHARACTERIZE

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

CPU CONFIGURATION

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	D	051-6888	B
SCALE	SHT 7 OF 40		
NONE			

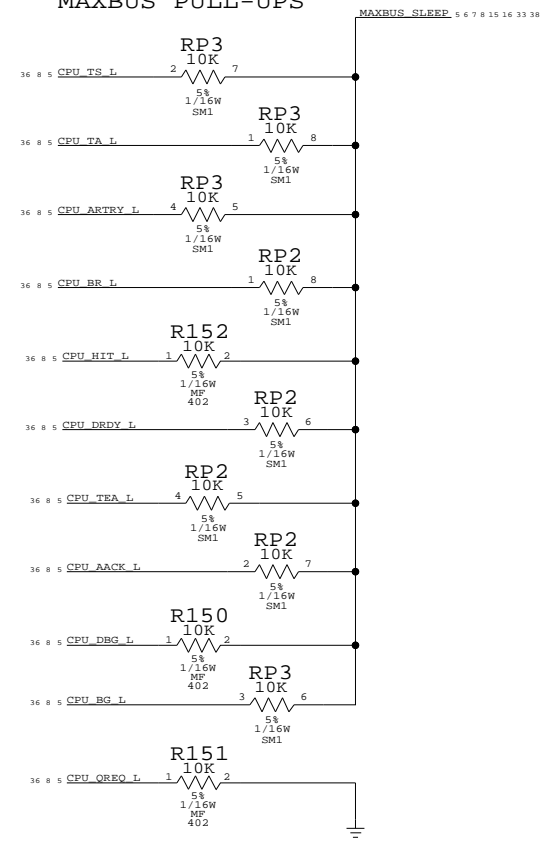
INTREPID BOOT STRAPS

THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:

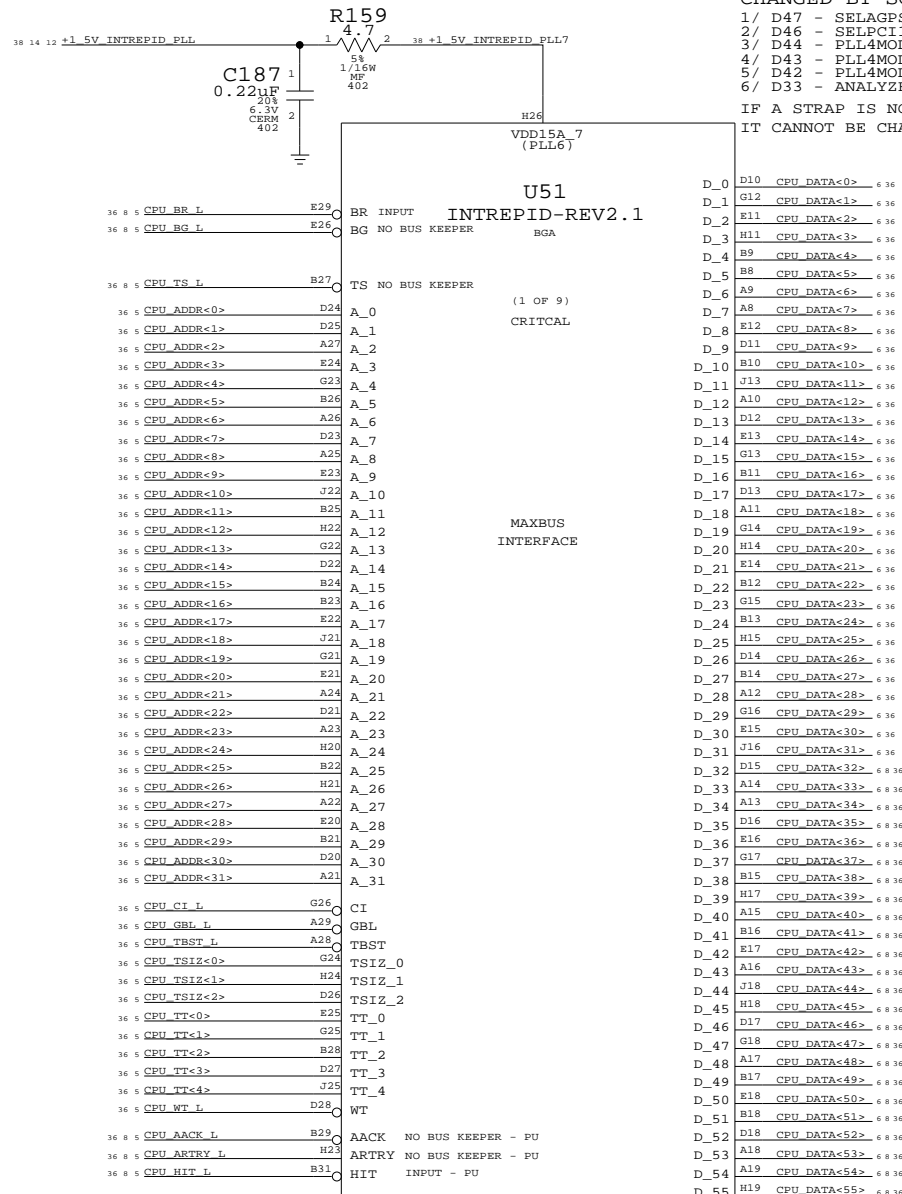
- 1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
- 2/ D46 - SELDPT1SPREADCLK - SLEEP/WAKE CYCLE REQUIRED
- 3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
- 4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
- 5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
- 6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT

IF A STRAP IS NOT LISTED, THEN IT CANNOT BE CHANGED BY SOFTWARE

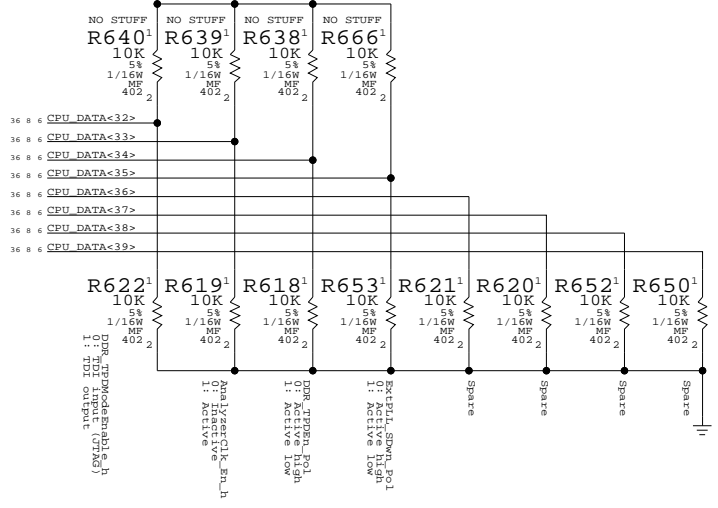
MAXBUS PULL-UPS



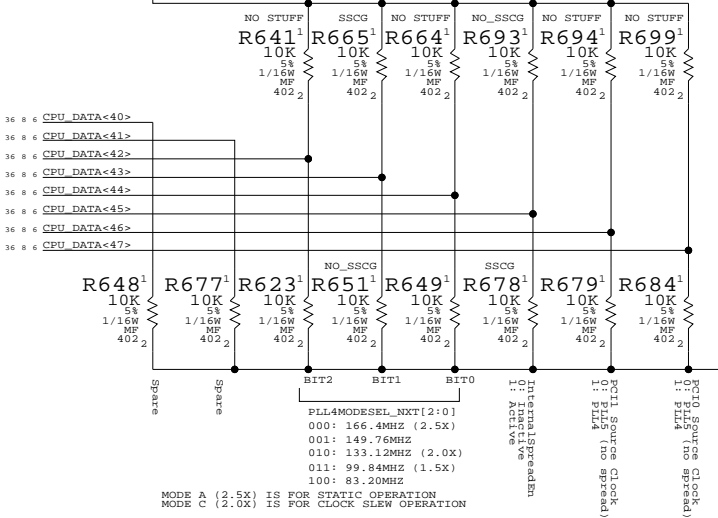
INTREPID BOOT STRAPS



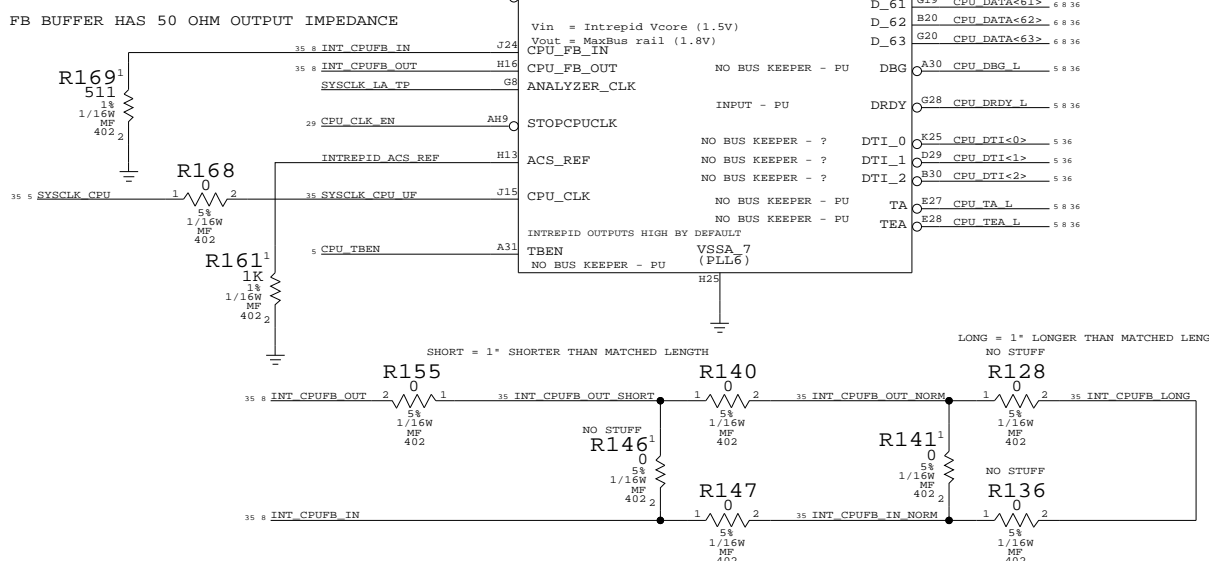
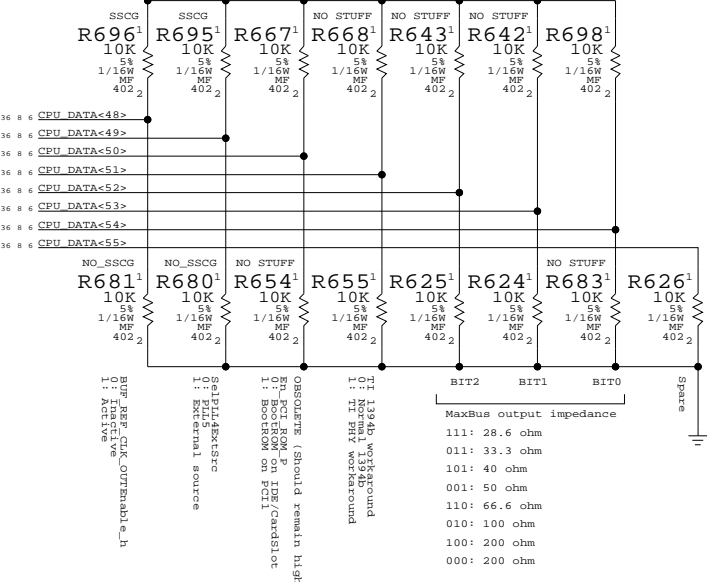
BIT 32 TO 39



BIT 40 TO 47



BIT 48 TO 55



Intrepid MaxBus

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	SCALE: NONE	SHEET: 8	OF: 40

SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

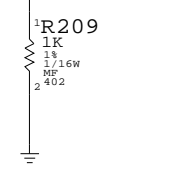
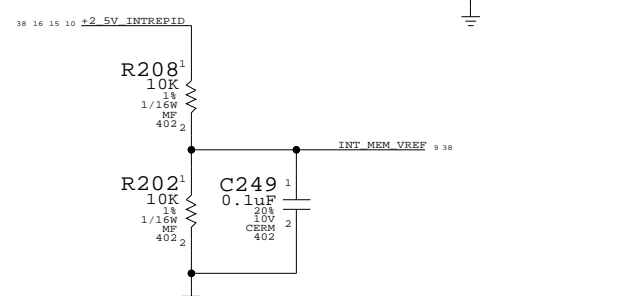
PINS ARE SWAPABLE FOR RPAKS

MEM_DATA<0>	AK32	DDR_DATA_0	DDR_A_0	H35	MEM_ADDR<0>
MEM_DATA<1>	AK33	DDR_DATA_1	DDR_A_1	G35	MEM_ADDR<1>
MEM_DATA<2>	AK31	DDR_DATA_2	DDR_A_2	G36	MEM_ADDR<2>
MEM_DATA<3>	AK35	DDR_DATA_3	DDR_A_3	F35	MEM_ADDR<3>
MEM_DATA<4>	AK36	DDR_DATA_4	DDR_A_4	F35	MEM_ADDR<4>
MEM_DATA<5>	AJ32	DDR_DATA_5	DDR_A_5	E35	MEM_ADDR<5>
MEM_DATA<6>	AJ35	DDR_DATA_6	DDR_A_6	E36	MEM_ADDR<6>
MEM_DATA<7>	AJ36	DDR_DATA_7	DDR_A_7	G32	MEM_ADDR<7>
MEM_DATA<8>	AG33	DDR_DATA_8	DDR_A_8	D36	MEM_ADDR<8>
MEM_DATA<9>	AG35	DDR_DATA_9	DDR_A_9	H36	MEM_ADDR<9>
MEM_DATA<10>	AH35	DDR_DATA_10	DDR_A_10	G33	MEM_ADDR<10>
MEM_DATA<11>	AG36	DDR_DATA_11	DDR_A_11	H33	MEM_ADDR<11>
MEM_DATA<12>	AH36	DDR_DATA_12	DDR_A_12	D35	MEM_ADDR<12>
MEM_DATA<13>	AH32	DDR_DATA_13	DDR_BA_0	L30	MEM_BA<0>
MEM_DATA<14>	AG32	DDR_DATA_14	DDR_BA_1	M29	MEM_BA<1>
MEM_DATA<15>	AG31	DDR_DATA_15	DDRC_S_0	AN34	MEM_CS_L<0>
MEM_DATA<16>	AK32	DDR_DATA_16	DDRC_S_1	AN36	MEM_CS_L<1>
MEM_DATA<17>	AF35	DDR_DATA_17	DDRC_S_2	AL35	MEM_CS_L<2>
MEM_DATA<18>	AF36	DDR_DATA_18	DDRC_S_3	AL33	MEM_CS_L<3>
MEM_DATA<19>	AE36	DDR_DATA_19	DDR_DQS_0	AJ31	MEM_DQS<0>
MEM_DATA<20>	AE35	DDR_DATA_20	DDR_DQS_1	AH31	MEM_DQS<1>
MEM_DATA<21>	AE33	DDR_DATA_21	DDR_DQS_2	AD32	MEM_DQS<2>
MEM_DATA<22>	AD36	DDR_DATA_22	DDR_DQS_3	AB30	MEM_DQS<3>
MEM_DATA<23>	AD35	DDR_DATA_23	DDR_DQS_4	V30	MEM_DQS<4>
MEM_DATA<24>	AA36	DDR_DATA_24	DDR_DQS_5	F32	MEM_DQS<5>
MEM_DATA<25>	AA35	DDR_DATA_25	DDR_DQS_6	W29	MEM_DQS<6>
MEM_DATA<26>	AA33	DDR_DATA_26	DDR_DQS_7	L32	MEM_DQS<7>
MEM_DATA<27>	AB36	DDR_DATA_27	DDR_DM_0	AJ33	MEM_DQM<0>
MEM_DATA<28>	AB35	DDR_DATA_28	DDR_DM_1	AH33	MEM_DQM<1>
MEM_DATA<29>	AC36	DDR_DATA_29	DDR_DM_2	AD33	MEM_DQM<2>
MEM_DATA<30>	AA32	DDR_DATA_30	DDR_DM_3	AC35	MEM_DQM<3>
MEM_DATA<31>	AB33	DDR_DATA_31	DDR_DM_4	F35	MEM_DQM<4>
MEM_DATA<32>	V36	DDR_DATA_32	DDR_DM_5	F33	MEM_DQM<5>
MEM_DATA<33>	U33	DDR_DATA_33	DDR_DM_6	G32	MEM_DQM<6>
MEM_DATA<34>	U32	DDR_DATA_34	DDR_DM_7	L33	MEM_DQM<7>
MEM_DATA<35>	V35	DDR_DATA_35	DDRRAS	L29	MEM_RAS_L
MEM_DATA<36>	T30	DDR_DATA_36	DDRCAS	H32	MEM_CAS_L
MEM_DATA<37>	U36	DDR_DATA_37	DDRWE	K30	MEM_WE_L
MEM_DATA<38>	U35	DDR_DATA_38	DDRCKE0	AN35	MEM_CKE<0>
MEM_DATA<39>	T36	DDR_DATA_39	DDRCKE1	AM35	MEM_CKE<1>
MEM_DATA<40>	F33	DDR_DATA_40	DDRCKE2	AM36	MEM_CKE<2>
MEM_DATA<41>	R30	DDR_DATA_41	DDRCKE3	AL36	MEM_CKE<3>
MEM_DATA<42>	F35	DDR_DATA_42	DDR_SELHI_0	AB32	MEM_MUXSEL_MSB_L_TP
MEM_DATA<43>	F36	DDR_DATA_43	DDR_SELHI_1	AE29	MEM_MUXSEL_MSB
MEM_DATA<44>	R36	DDR_DATA_44	DDR_SELLO_0	N30	MEM_MUXSEL_LSB_L_TP
MEM_DATA<45>	R35	DDR_DATA_45	DDR_SELLO_1	T32	MEM_MUXSEL_LSB
MEM_DATA<46>	R33	DDR_DATA_46	DDR_MCLK_0_P	Y32	SYSCLK_DDRCLK_A0_UF
MEM_DATA<47>	R32	DDR_DATA_47	DDR_MCLK_0_N	Y33	SYSCLK_DDRCLK_A0_L_UF
MEM_DATA<48>	N35	DDR_DATA_48	DDR_MCLK_1_P	Y35	SYSCLK_DDRCLK_A1_UF
MEM_DATA<49>	M36	DDR_DATA_49	DDR_MCLK_1_N	Y36	SYSCLK_DDRCLK_A1_L_UF
MEM_DATA<50>	L35	DDR_DATA_50	DDR_MCLK_2_P	Y30	INT_DDRCLK2_P_TP
MEM_DATA<51>	M35	DDR_DATA_51	DDR_MCLK_2_N	Y30	INT_DDRCLK2_N_TP
MEM_DATA<52>	M33	DDR_DATA_52	DDR_MCLK_3_P	W32	SYSCLK_DDRCLK_B0_UF
MEM_DATA<53>	L36	DDR_DATA_53	DDR_MCLK_3_N	W33	SYSCLK_DDRCLK_B0_L_UF
MEM_DATA<54>	N33	DDR_DATA_54	DDR_MCLK_4_P	Y32	SYSCLK_DDRCLK_B1_UF
MEM_DATA<55>	M30	DDR_DATA_55	DDR_MCLK_4_N	Y32	SYSCLK_DDRCLK_B1_L_UF
MEM_DATA<56>	J32	DDR_DATA_56	DDR_MCLK_5_P	W35	INT_DDRCLK5_P_TP
MEM_DATA<57>	J33	DDR_DATA_57	DDR_MCLK_5_N	W36	INT_DDRCLK5_N_TP
MEM_DATA<58>	J35	DDR_DATA_58	DDR_REF	AA22	INT_MEM_REF_H
MEM_DATA<59>	K32	DDR_DATA_59	DDR_VREF_0	Y22	INT_MEM_VREF
MEM_DATA<60>	K33	DDR_DATA_60	DDR_VREF_1	T22	
MEM_DATA<61>	J36	DDR_DATA_61			
MEM_DATA<62>	K36	DDR_DATA_62			
MEM_DATA<63>	X35	DDR_DATA_63			

U51
INTREPID-REV2.1
(2 OF 9)
CRITICAL

DDR MEMORY INTERFACE

MEM_VREF



CLOCKS

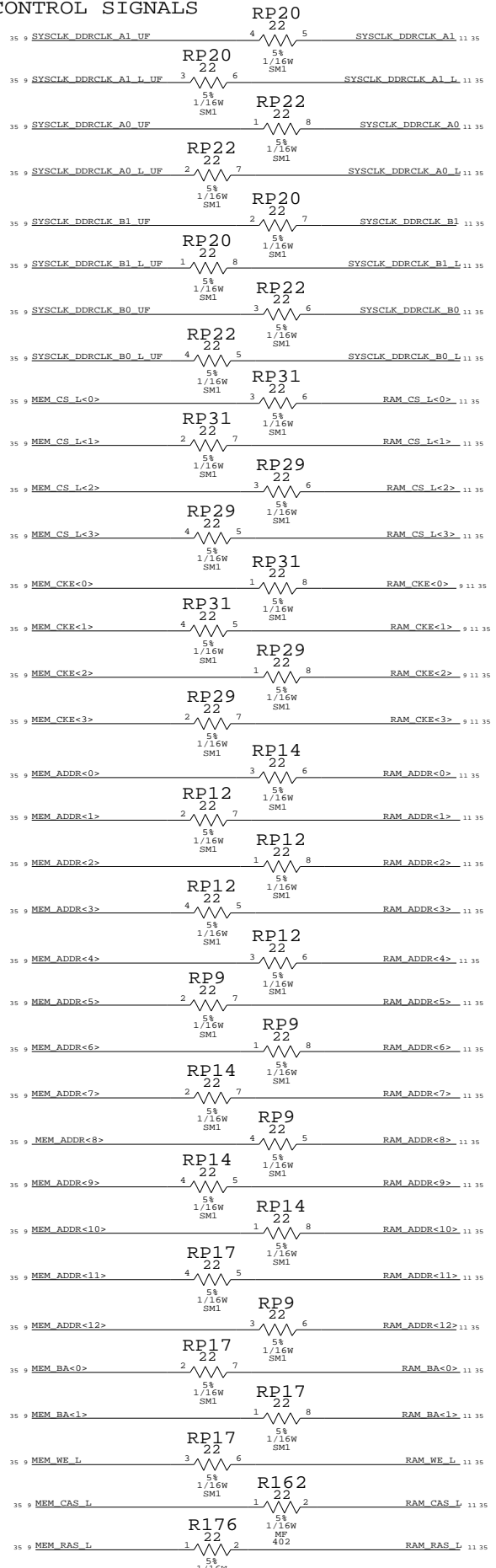
CS

CKE

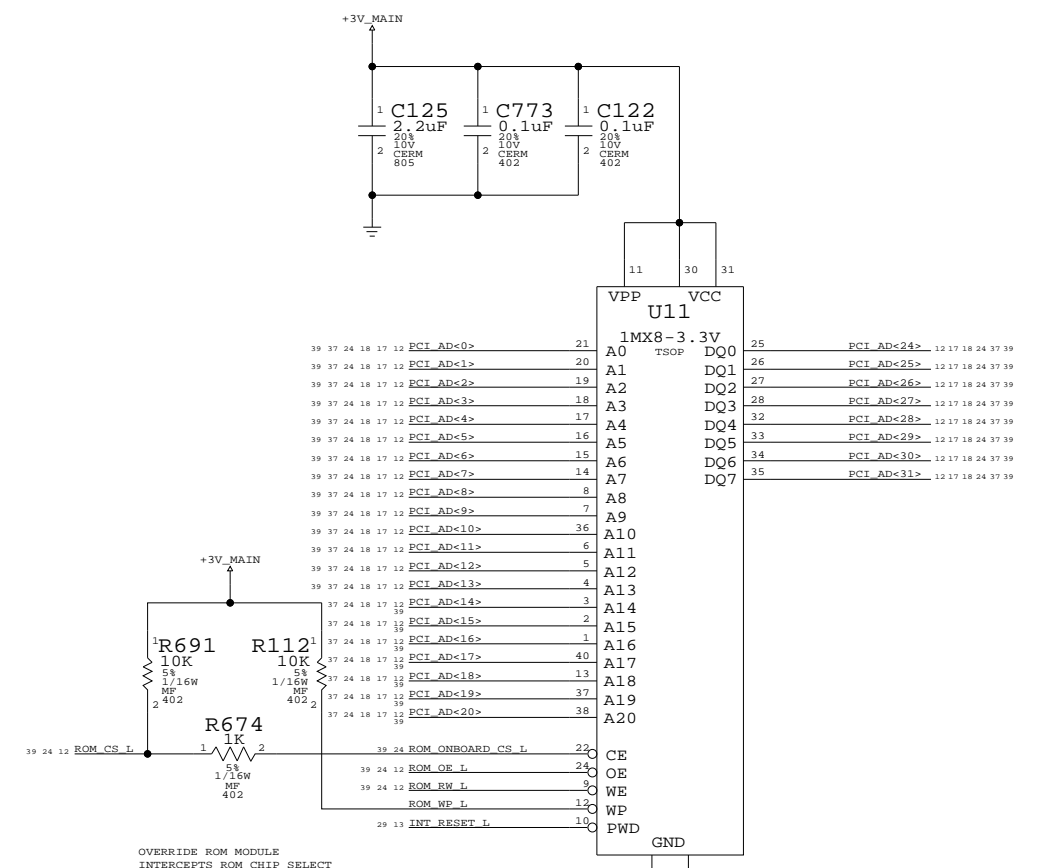
ADDR

BA

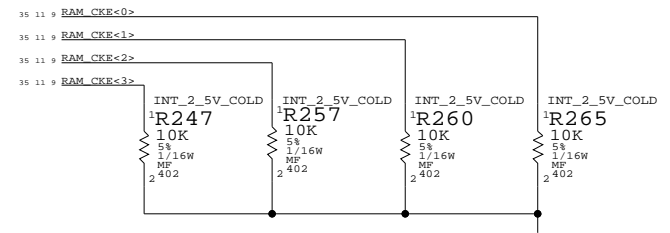
CNTL



1MB BOOT ROM



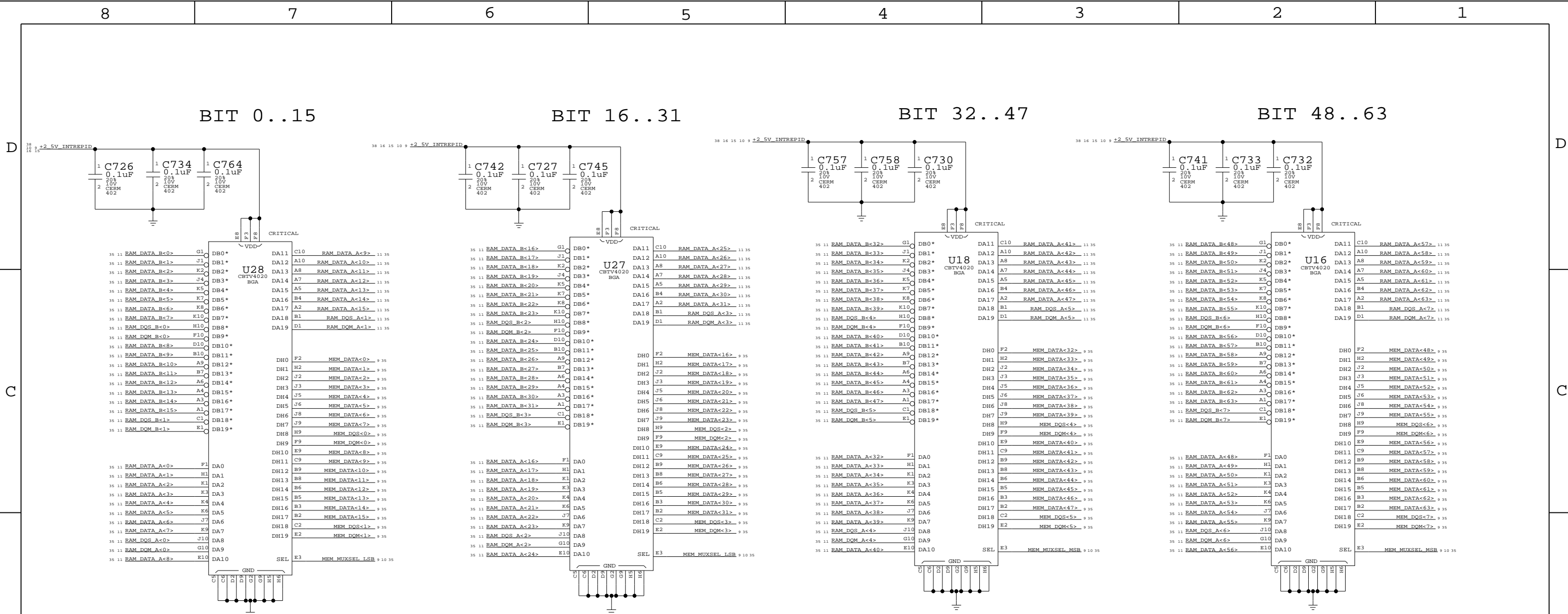
Weak pulldowns ensure CKEs stay low after 2.5V I/O to Intrepid shuts off.



INT - DDR/BOOTROM

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6888	B
SCALE	NONE	SHT	9 OF 40



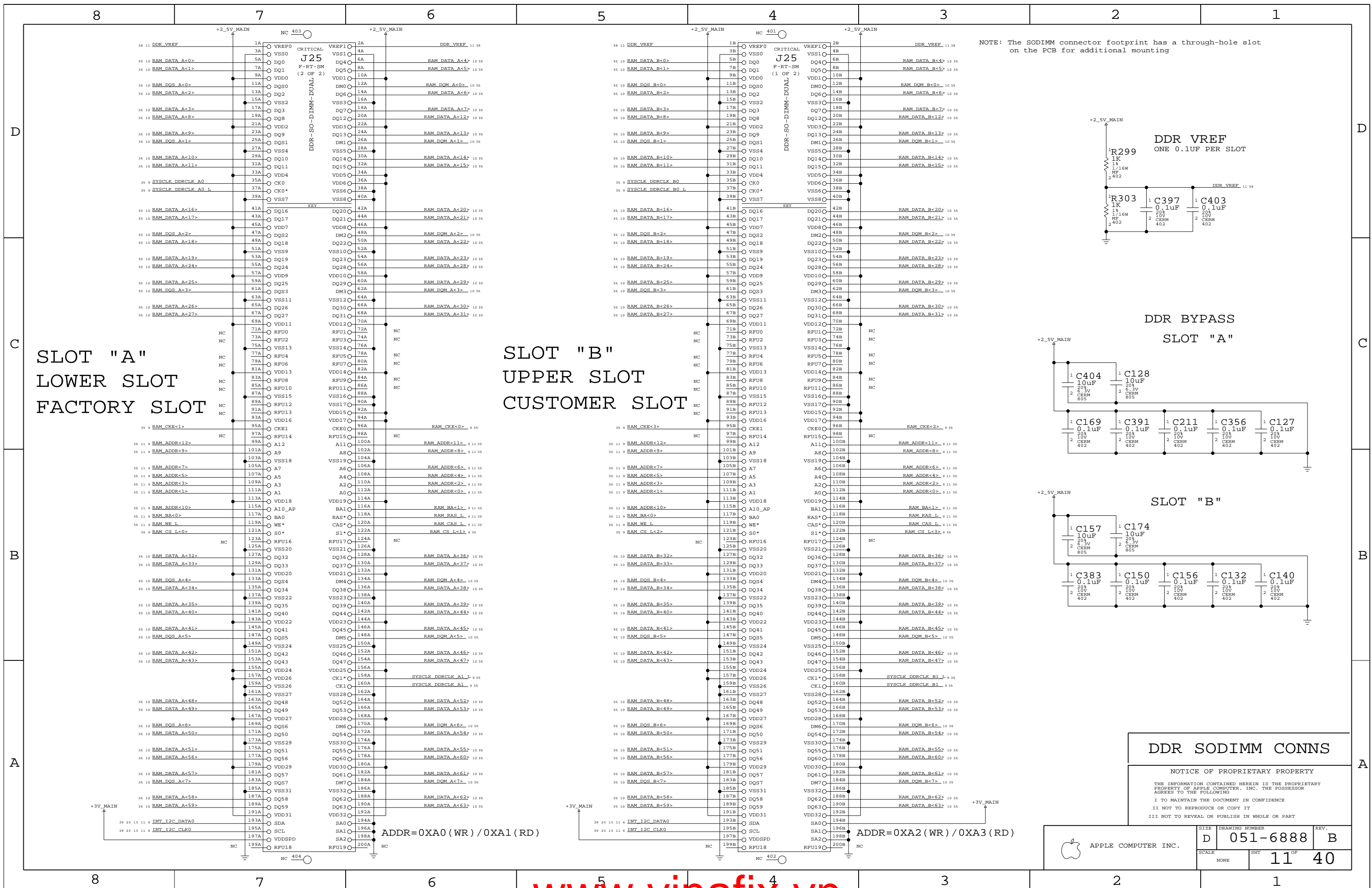
SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
 SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND

16BIT 2:1 DDR MUXES

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6888	B
SCALE	SHT	10 OF 40	
NONE			



NOTE: The SODIMM connector footprint has a through-hole slot on the PCB for additional mounting

SLOT "A"
LOWER SLOT
FACTORY SLOT

SLOT "B"
UPPER SLOT
CUSTOMER SLOT

DDR VREF
ONE 0.1UF PER SLOT

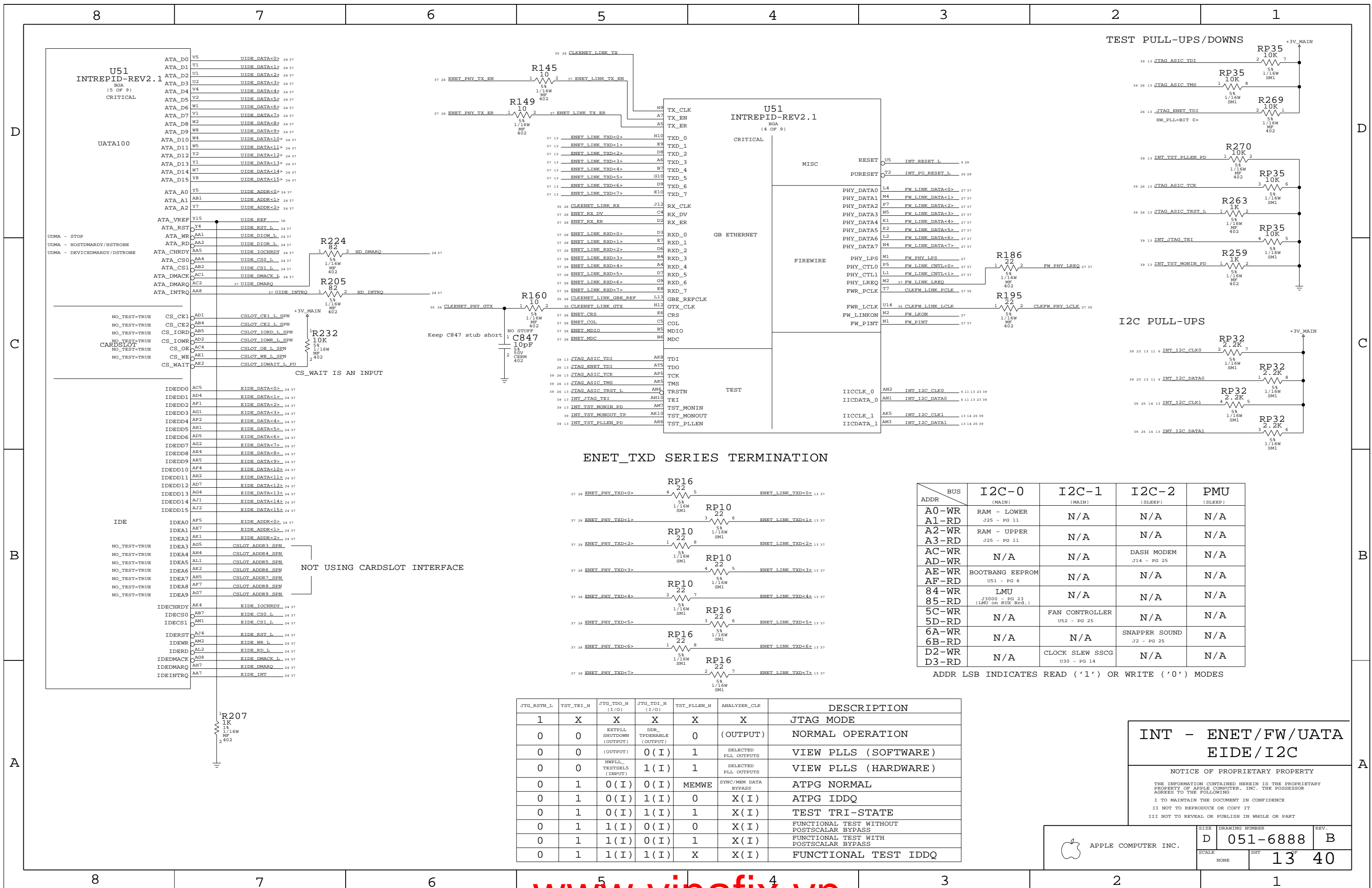
DDR BYPASS
SLOT "A"

SLOT "B"

DDR SODIMM CONNS

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6888	REV. B
	SCALE NONE	SHT 11 OF 40	



U51
INTREPID-REV2.1
BGA
(5 OF 9)
CRITICAL

UATA100

UDMA - STOP
UDMA - HOSTDMARDY/HSTROBE
UDMA - DEVICEMARDY/DSTROBE

CARDSLOT
NO_TEST=TRUE
NO_TEST=TRUE
NO_TEST=TRUE
NO_TEST=TRUE
NO_TEST=TRUE

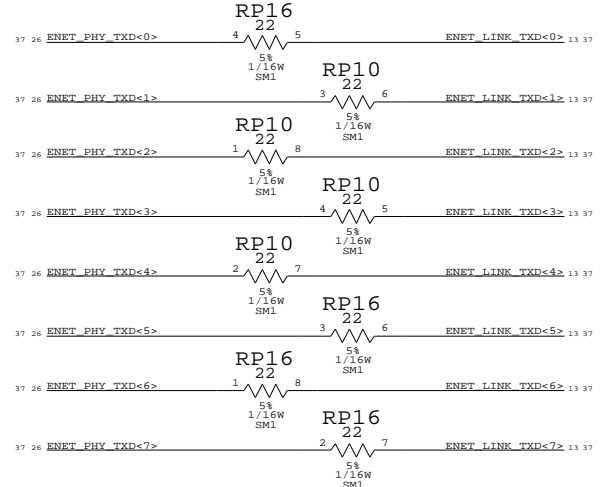
IDE

ATA_D0	V5	UIDE_DATA<0>	24 37
ATA_D1	T1	UIDE_DATA<1>	24 37
ATA_D2	U1	UIDE_DATA<2>	24 37
ATA_D3	U2	UIDE_DATA<3>	24 37
ATA_D4	V4	UIDE_DATA<4>	24 37
ATA_D5	V2	UIDE_DATA<5>	24 37
ATA_D6	M1	UIDE_DATA<6>	24 37
ATA_D7	V1	UIDE_DATA<7>	24 37
ATA_D8	M2	UIDE_DATA<8>	24 37
ATA_D9	M8	UIDE_DATA<9>	24 37
ATA_D10	M4	UIDE_DATA<10>	24 37
ATA_D11	M5	UIDE_DATA<11>	24 37
ATA_D12	V2	UIDE_DATA<12>	24 37
ATA_D13	Y1	UIDE_DATA<13>	24 37
ATA_D14	M7	UIDE_DATA<14>	24 37
ATA_D15	Y8	UIDE_DATA<15>	24 37
ATA_A0	Y5	UIDE_ADDR<0>	24 37
ATA_A1	AB1	UIDE_ADDR<1>	24 37
ATA_A2	Y7	UIDE_ADDR<2>	24 37
ATA_VREF	Y15	UIDE_REF	38
ATA_RST	Y4	UIDE_RST_L	24 37
ATA_WR	AA1	UIDE_DIOW_L	24 37
ATA_RD	AA2	UIDE_DIOR_L	24 37
ATA_CHRDY	AA5	UIDE_IOCHRDY	24 37
ATA_CS0	AA4	UIDE_CS0_L	24 37
ATA_CS1	AB2	UIDE_CS1_L	24 37
ATA_DMACK	AC1	UIDE_DMACK_L	24 37
ATA_DMARQ	AC2	UIDE_DMARQ_L	24 37
ATA_INTRQ	AA8	UIDE_INTRQ	24 37
CS_CEL1	AD1	CSLOT_CEL1_L_SPN	
CS_CEL2	AB4	CSLOT_CEL2_L_SPN	
CS_IORD	AB5	CSLOT_IORD_L_SPN	
CS_IOWR	AD2	CSLOT_IOWR_L_SPN	
CS_OE	AC4	CSLOT_OE_L_SPN	
CS_WE	AE1	CSLOT_WE_L_SPN	
CS_WAIT	AE2	CSLOT_IOWAIT_L_PU	
IDEDD0	AC5	EIDE_DATA<0>	24 37
IDEDD1	AD4	EIDE_DATA<1>	24 37
IDEDD2	AF1	EIDE_DATA<2>	24 37
IDEDD3	AG1	EIDE_DATA<3>	24 37
IDEDD4	AF2	EIDE_DATA<4>	24 37
IDEDD5	AH1	EIDE_DATA<5>	24 37
IDEDD6	AD5	EIDE_DATA<6>	24 37
IDEDD7	AG2	EIDE_DATA<7>	24 37
IDEDD8	AE4	EIDE_DATA<8>	24 37
IDEDD9	AK5	EIDE_DATA<9>	24 37
IDEDD10	AF4	EIDE_DATA<10>	24 37
IDEDD11	AH2	EIDE_DATA<11>	24 37
IDEDD12	AD7	EIDE_DATA<12>	24 37
IDEDD13	AG4	EIDE_DATA<13>	24 37
IDEDD14	AJ1	EIDE_DATA<14>	24 37
IDEDD15	AJ2	EIDE_DATA<15>	24 37
IDEA0	AF5	EIDE_ADDR<0>	24 37
IDEA1	AK7	EIDE_ADDR<1>	24 37
IDEA2	AK1	EIDE_ADDR<2>	24 37
IDEA3	AG5	CSLOT_ADDR3_SPN	
IDEA4	AH4	CSLOT_ADDR4_SPN	
IDEA5	AL1	CSLOT_ADDR5_SPN	
IDEA6	AK2	CSLOT_ADDR6_SPN	
IDEA7	AH5	CSLOT_ADDR7_SPN	
IDEA8	AF7	CSLOT_ADDR8_SPN	
IDEA9	AG7	CSLOT_ADDR9_SPN	
IDECHRDY	AK4	EIDE_IOCHRDY	24 37
IDEC_S0	AB7	EIDE_CS0_L	24 37
IDEC_S1	AM1	EIDE_CS1_L	24 37
IDERST	AJ4	EIDE_RST_L	24 37
IDENR	AM2	EIDE_NR_L	24 37
IDERD	AL2	EIDE_RD_L	24 37
IDEDMACK	AG8	EIDE_DMACK_L	24 37
IDEDMARQ	AH7	EIDE_DMARQ_L	24 37
IDEINTRQ	AA7	EIDE_INT	24 37

NOT USING CARDSLOT INTERFACE

Keep C847 stub short

ENET_TXD SERIES TERMINATION



JTG_RSTN_L	TST_TEI_H	JTG_TDO_H (I/O)	JTG_TDI_H (I/O)	TST_PLEN_H	ANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	EXTPLL SHUTDOWN (OUTPUT)	DDR_TPDENABLE (OUTPUT)	0	(OUTPUT)	NORMAL OPERATION
0	0	(OUTPUT)	0 (I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	HWPLL TRSTSLS (INPUT)	1 (I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0 (I)	0 (I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0 (I)	1 (I)	0	X (I)	ATPG IDDQ
0	1	0 (I)	1 (I)	1	X (I)	TEST TRI-STATE
0	1	1 (I)	0 (I)	0	X (I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1 (I)	0 (I)	1	X (I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1 (I)	1 (I)	X	X (I)	FUNCTIONAL TEST IDDQ

BUS ADDR	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
A0-WR	RAM - LOWER	N/A	N/A	N/A
A1-RD	J25 - PG 11			
A2-WR	RAM - UPPER	N/A	N/A	N/A
A3-RD	J25 - PG 11			
AC-WR			DASH MODEM	N/A
AD-WR			J14 - PG 25	
AE-WR	BOOTBANG EEPROM	N/A	N/A	N/A
AF-RD	U51 - PG 6			
84-WR	LMU	N/A	N/A	N/A
85-RD	J3000 - PG 23 (LMU on RUX Brd.)			
5C-WR		FAN CONTROLLER	N/A	N/A
5D-RD		U52 - PG 25		
6A-WR			SNAPPER SOUND	N/A
6B-RD			J2 - PG 25	
D2-WR		CLOCK SLEW SSCG	N/A	N/A
D3-RD		U30 - PG 14		

ADDR LSB INDICATES READ ('1') OR WRITE ('0') MODES

INT - ENET/FW/UATA EIDE/I2C

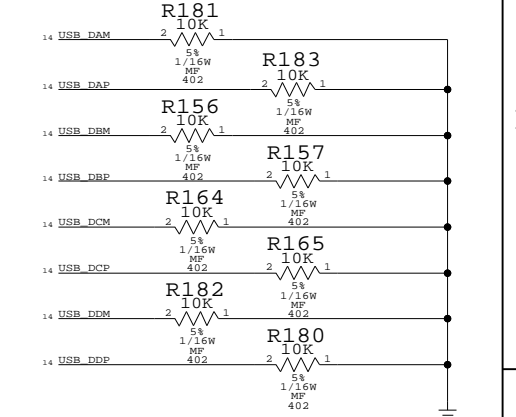
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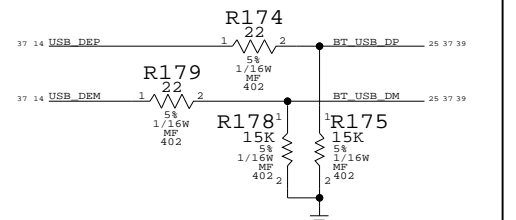
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6888	B
SCALE	SHT	13 40	
NONE			

USB PORT ASSIGNMENTS

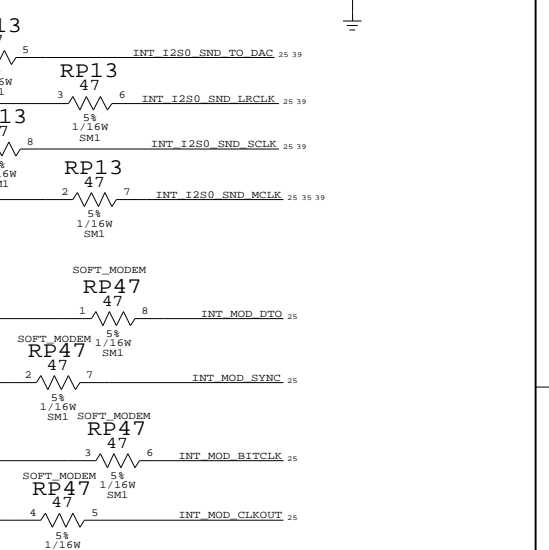
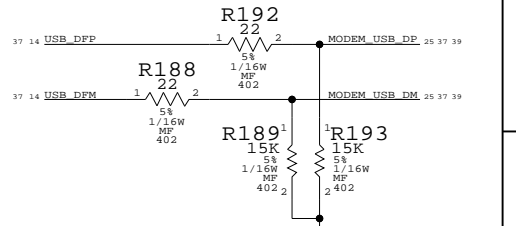
PORT A - PORT D/UNUSED



PORT E/BLUETOOTH



PORT F/MODEM



INT - USB/GPIOS/I2S

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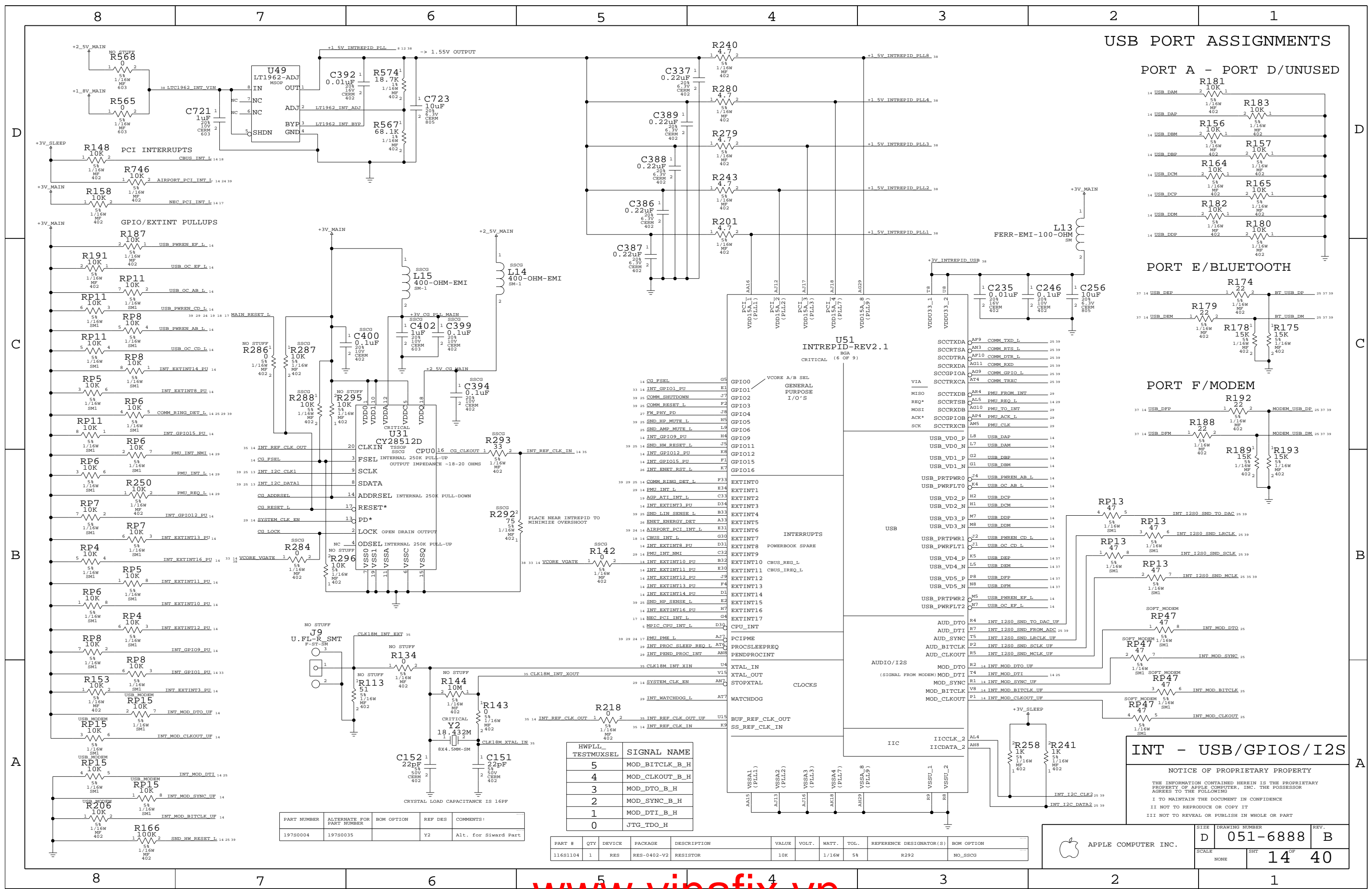
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
19780004	19780035		Y2	Alt. for Sward Part

HWPLL TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES	RES-0402-V2	RESISTOR	10K		1/16W	5%	R292	NO_SSCG



APPLE COMPUTER INC.

SIZE: D

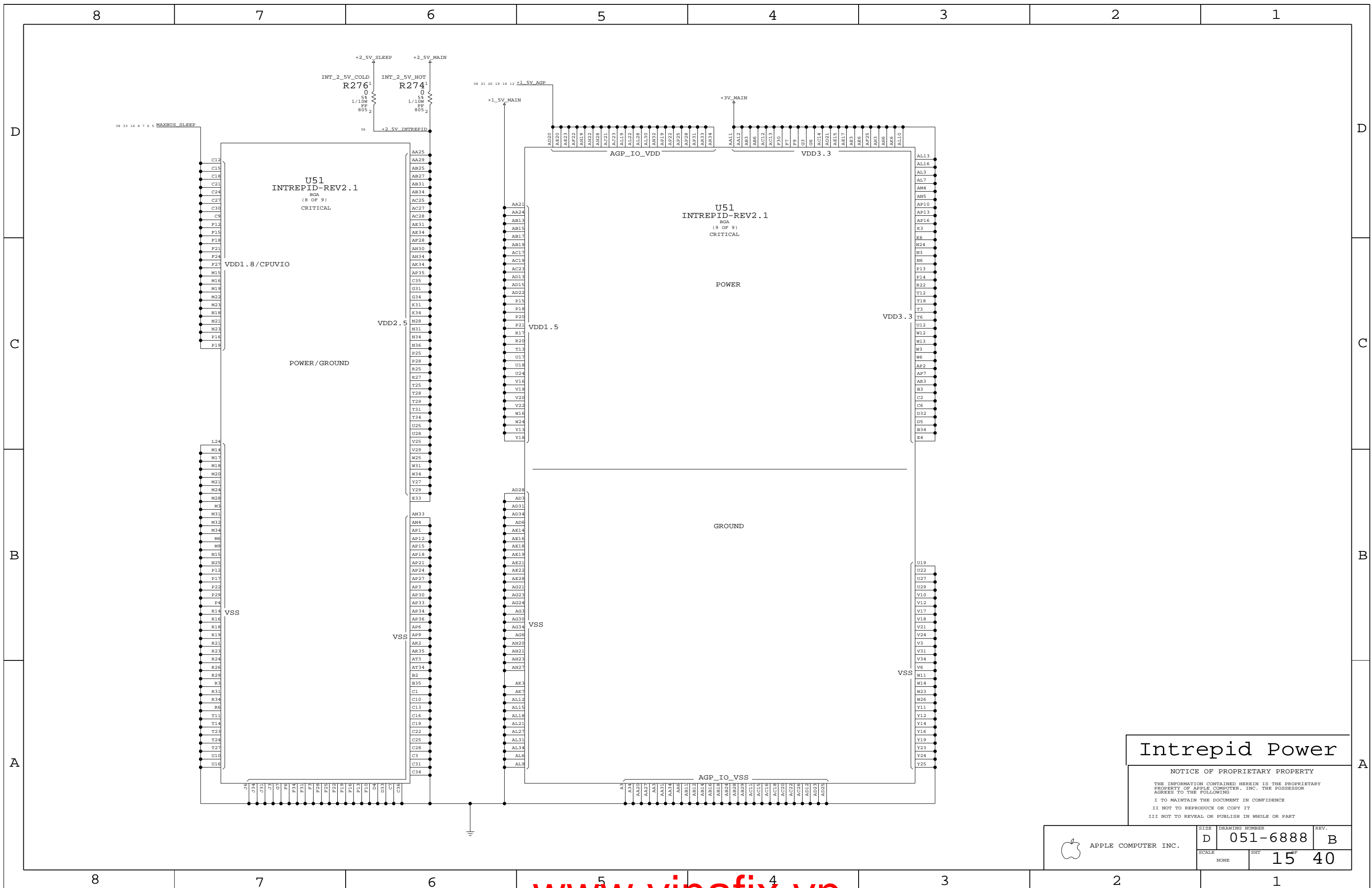
DRAWING NUMBER: 051-6888

REV.: B

SCALE: NONE

SHT: 14

OF: 40

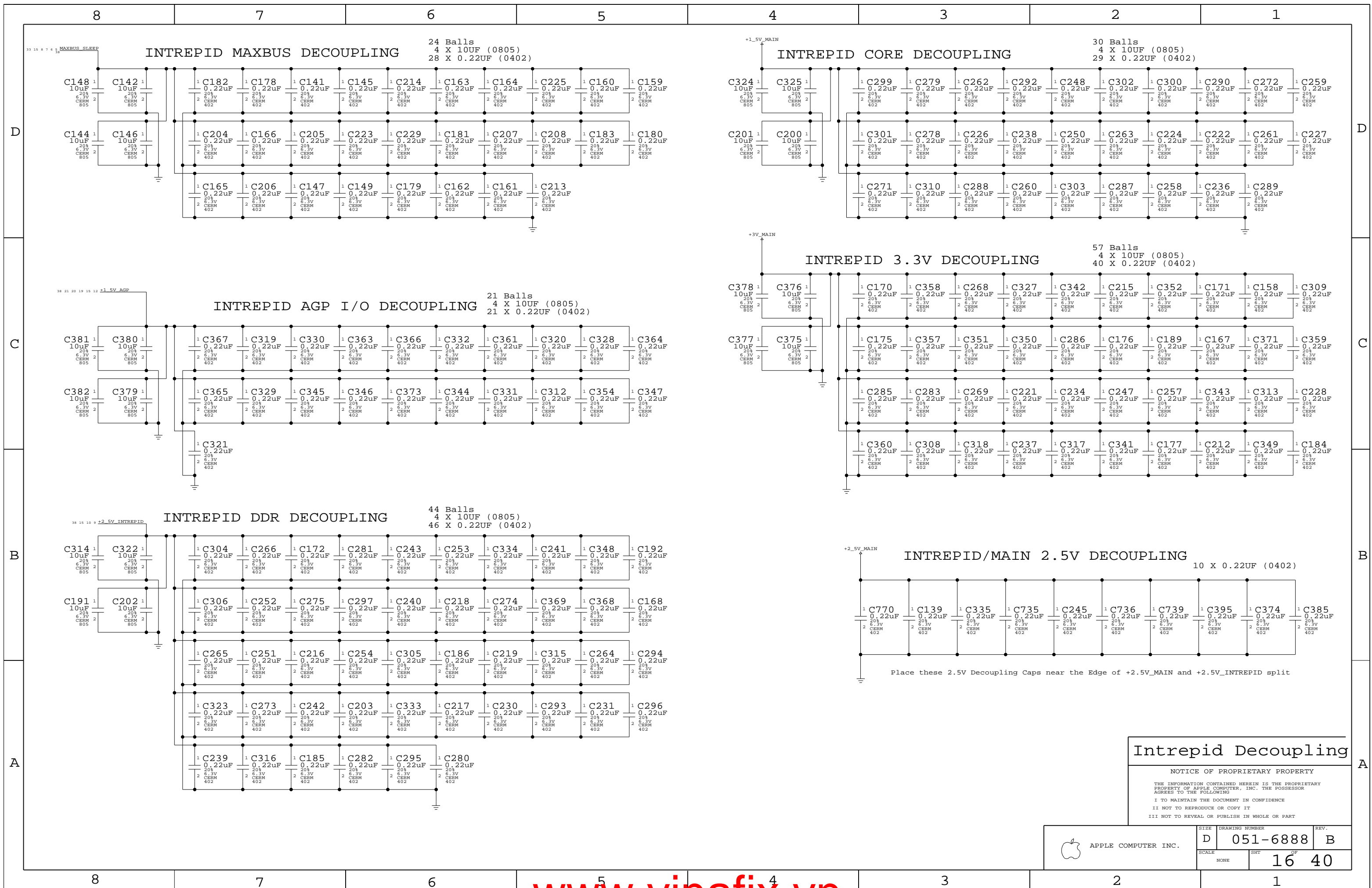


Intrepid Power

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6888	REV. B
	SCALE NONE	SHEETS 15	OF 40

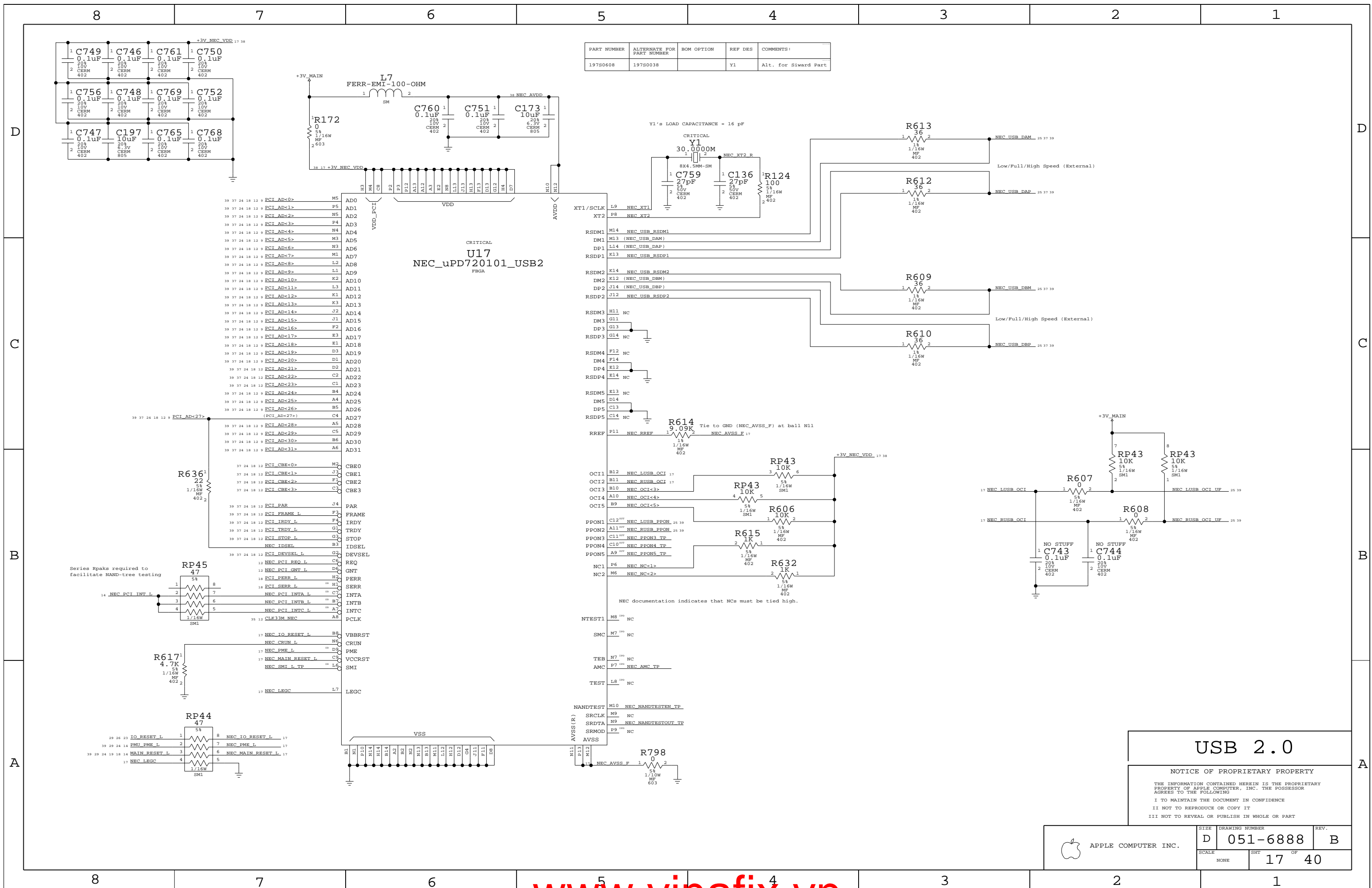


Intrepid Decoupling

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	NONE	051-6888	B
SCALE		SHEET	OF
		16	40



USB 2.0


NOTICE OF PROPRIETARY PROPERTY

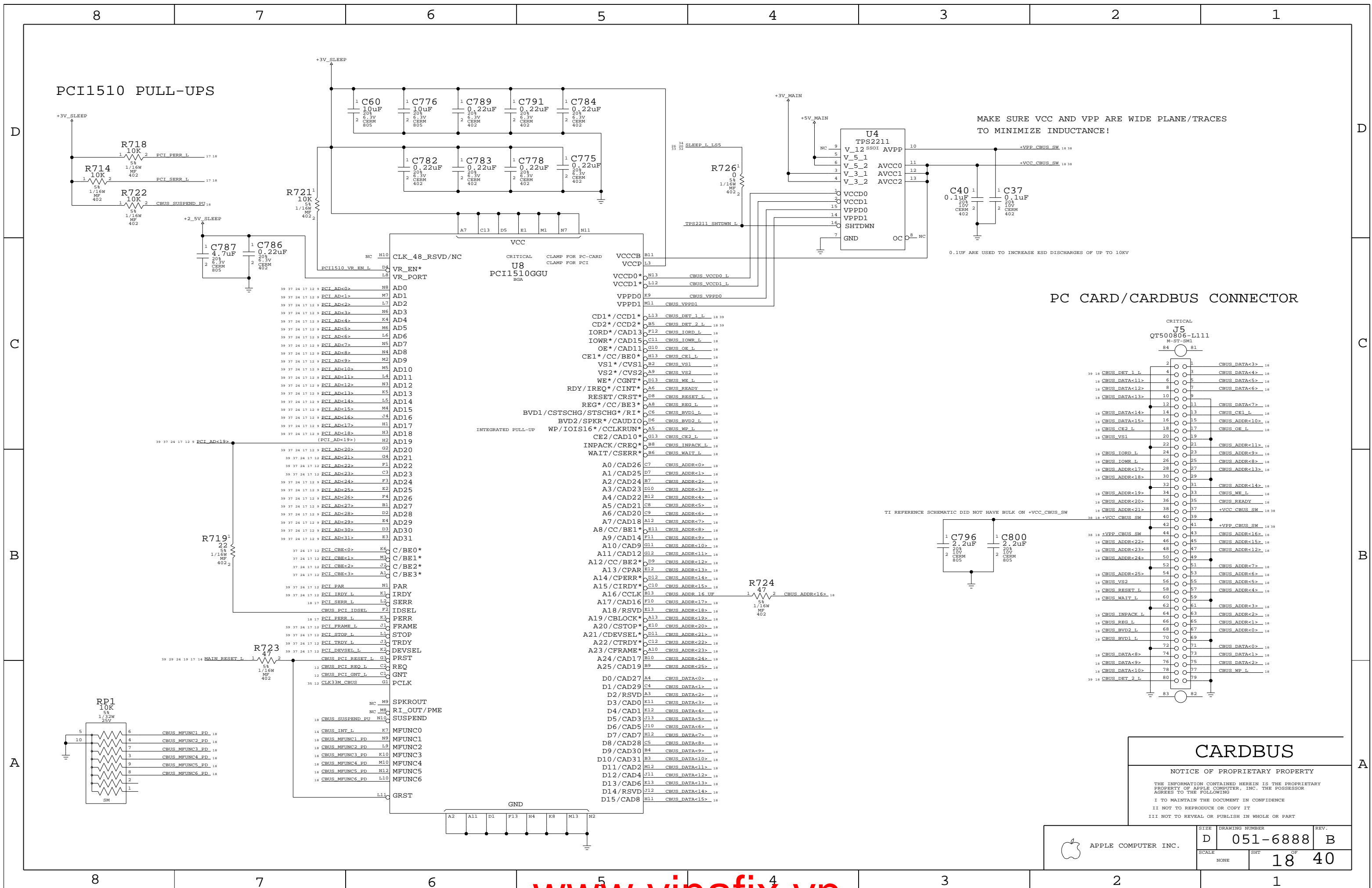
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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6888	B
SCALE	SHT OF		
NONE	17 OF		40



PC CARD/CARDBUS CONNECTOR

CRITICAL

J5
QT500806-L111
M-ST-SM1

84	81
2	1
4	3
6	5
8	7
10	9
12	11
14	13
16	15
18	17
20	19
22	21
24	23
26	25
28	27
30	29
32	31
34	33
36	35
38	37
40	39
42	41
44	43
46	45
48	47
50	49
52	51
54	53
56	55
58	57
60	59
62	61
64	63
66	65
68	67
70	69
72	71
74	73
76	75
78	77
80	79
83	82

CARDBUS

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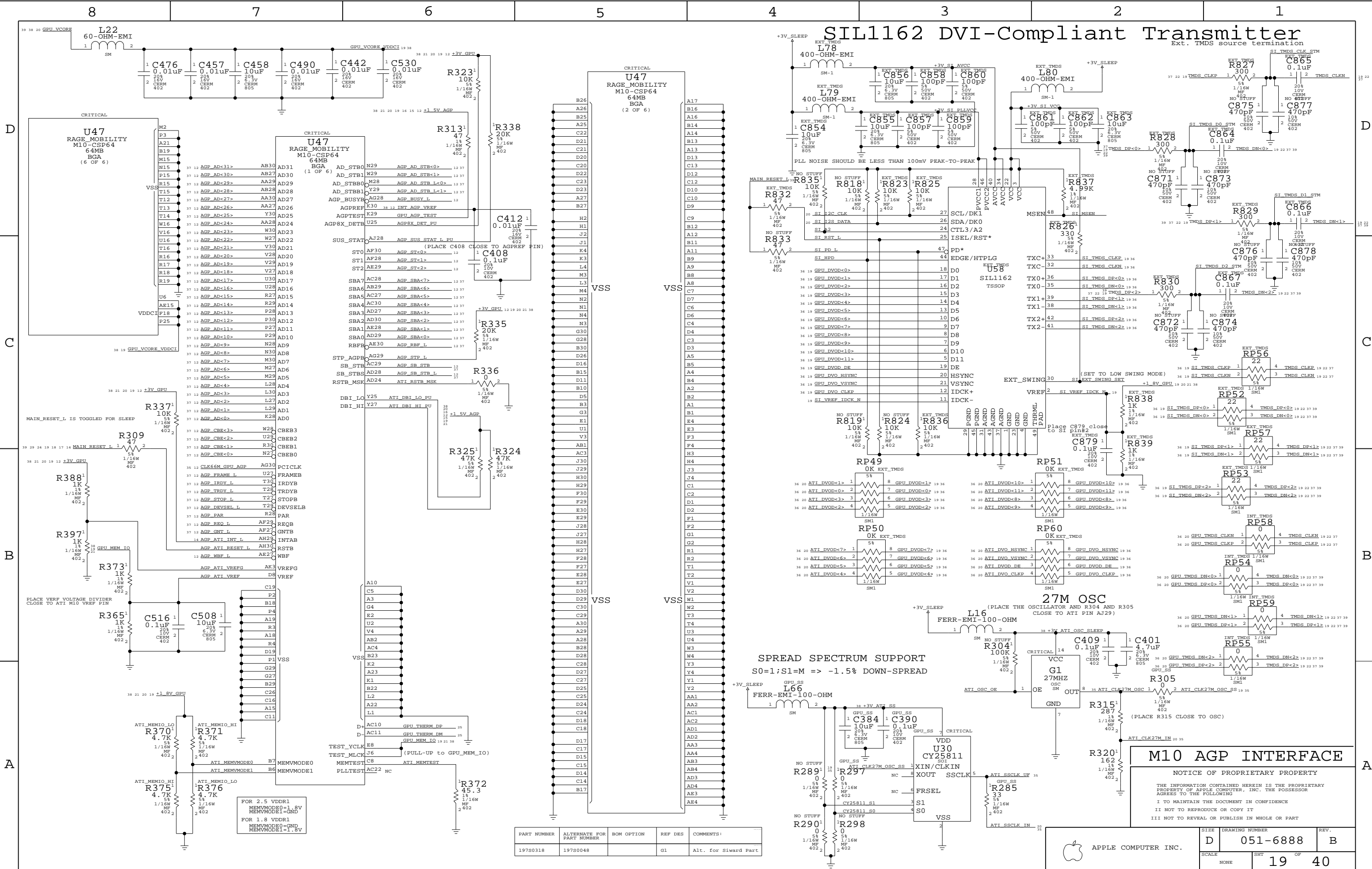
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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6888	B
SCALE	NONE	SHT	OF
		18	40

SIL1162 DVI-Compliant Transmitter

Ext. TMD5 source termination



SPREAD SPECTRUM SUPPORT
 $S0=1;S1=M \Rightarrow -1.5\% \text{ DOWN-SPREAD}$

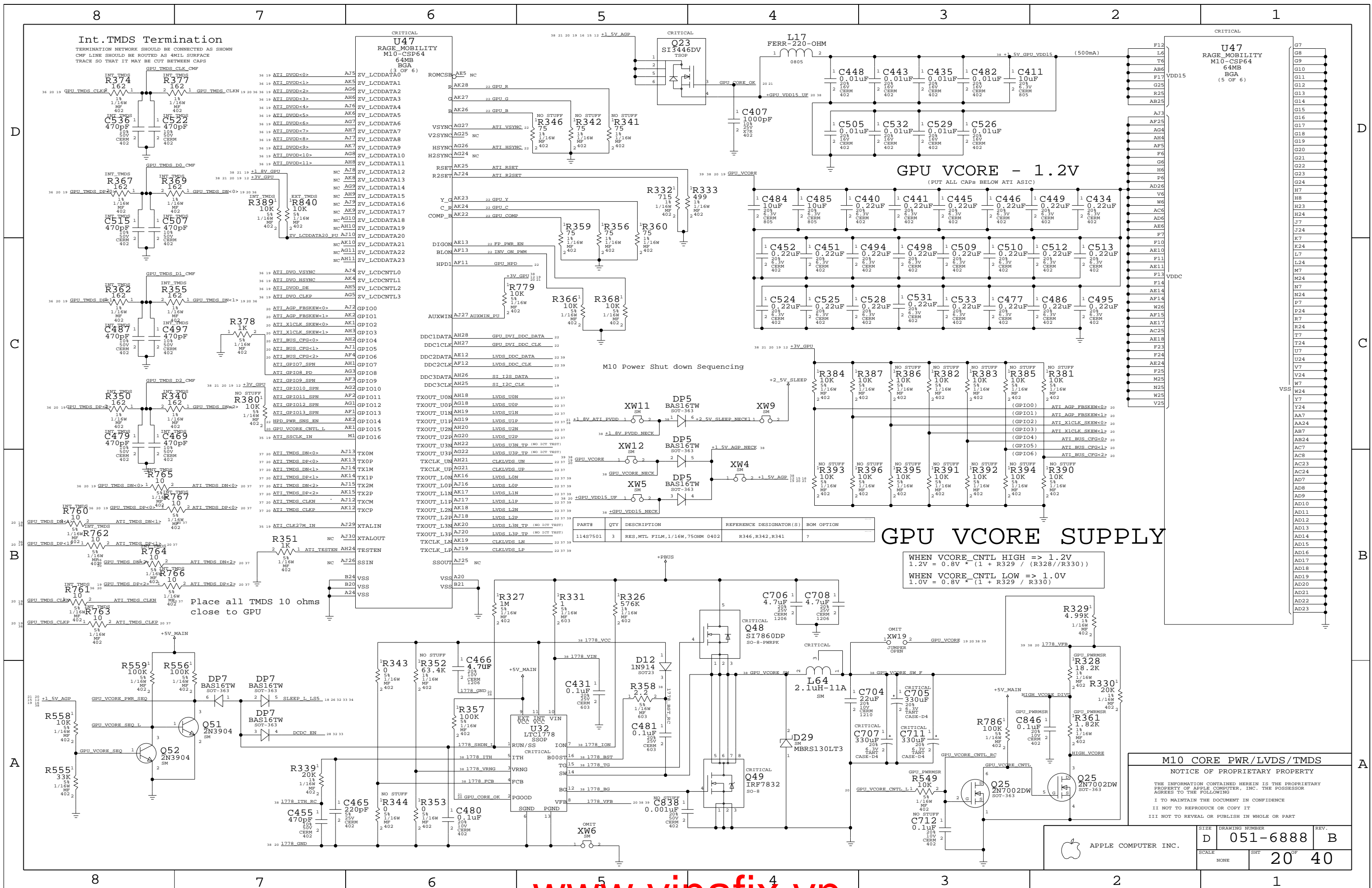
27M OSC
 (PLACE THE OSCILLATOR AND R304 AND R305 CLOSE TO ATI PIN A29)

M10 AGP INTERFACE

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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
19750318	19750048		G1	Alt. for Siward Part

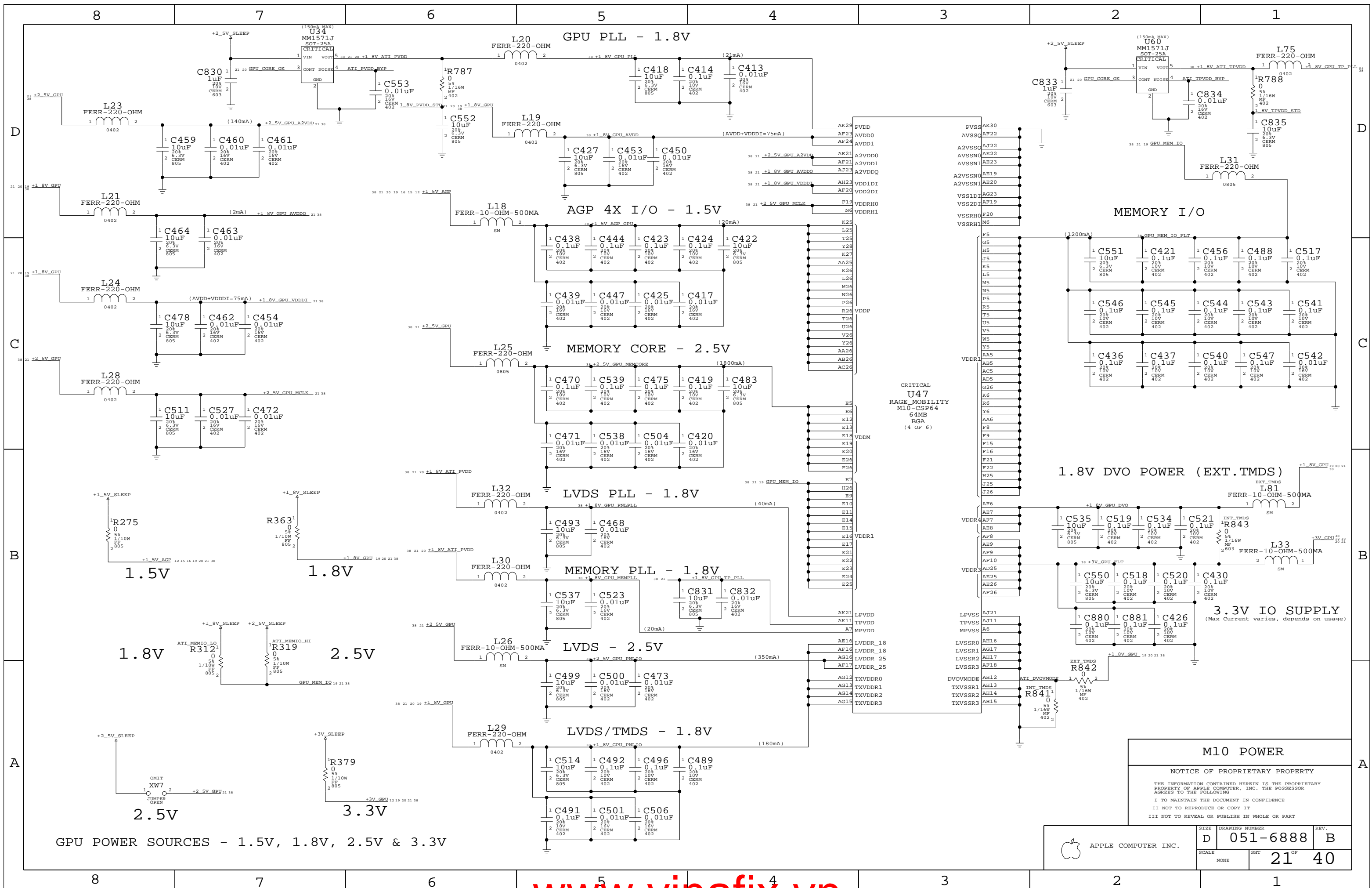
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6888	B
SCALE	NONE	SHEET	19 OF 40



M10 CORE PWR/LVDS/TMDs
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SIZE	DRAWING NUMBER	REV.
D	051-6888	B
SCALE	SHT	20 OF 40
NONE		

APPLE COMPUTER INC.



GPU POWER SOURCES - 1.5V, 1.8V, 2.5V & 3.3V

M10 POWER

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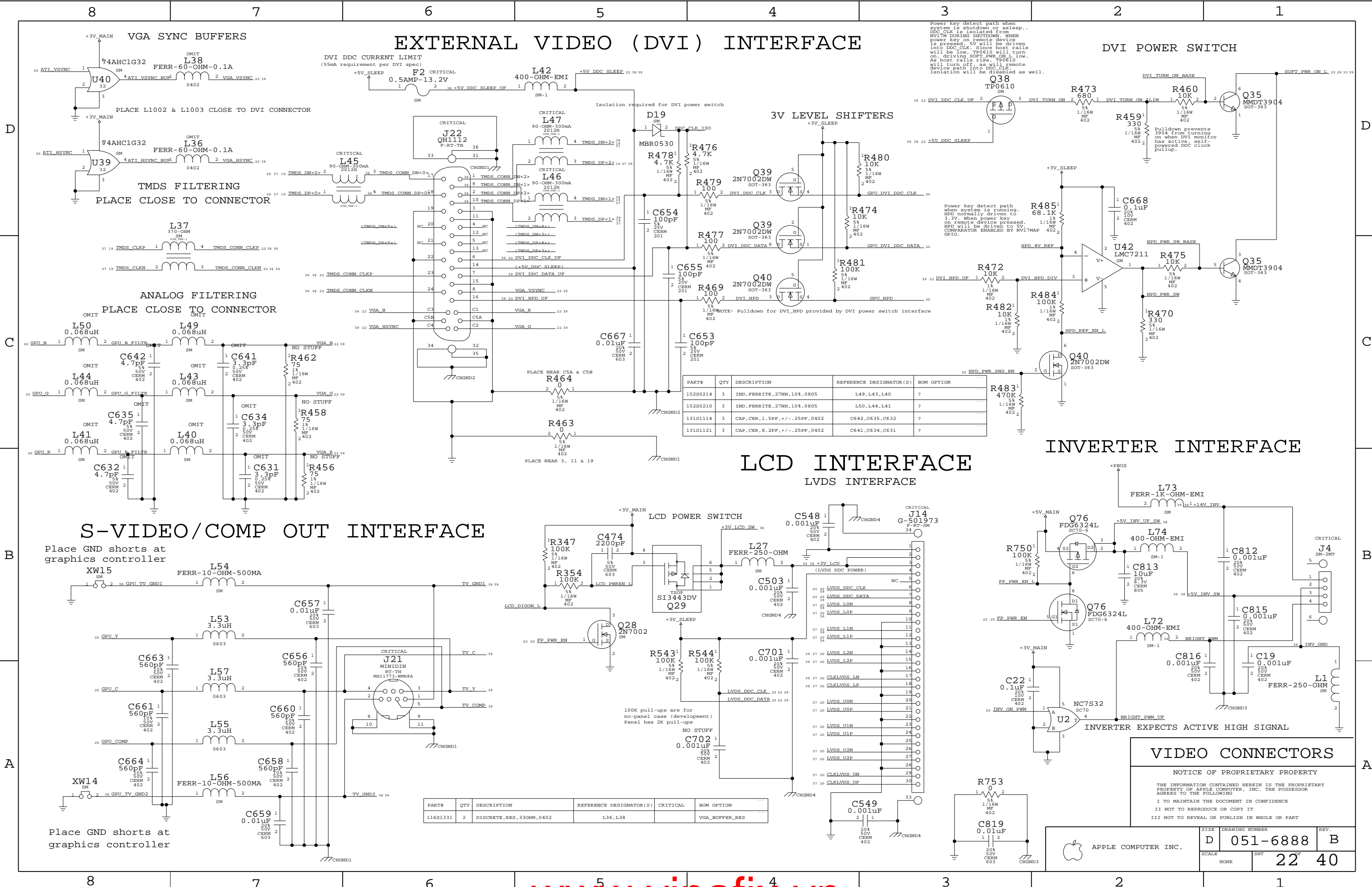
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

SIZE	DRAWING NUMBER	REV.
D	051-6888	B
SCALE	SHT	21 OF 40
NONE		

EXTERNAL VIDEO (DVI) INTERFACE



Power key detect path when system is shutdown or asleep... DDC_CLK is isolated from NV17M during SHUTDOWN. When power key on remote device is pressed, 5V will be driven into DDC_CLK. Since host rails will be low, TP0610 will turn on, driving SOFT_PWR_ON_L low. As host rails rise, TP0610 will turn off, and will remote device path into DDC_CLK. Isolation will be disabled as well.

DVI POWER SWITCH

3V LEVEL SHIFTERS

INVERTER INTERFACE

LCD INTERFACE

LVDS INTERFACE

VIDEO CONNECTORS

NOTICE OF PROPRIETARY PROPERTY

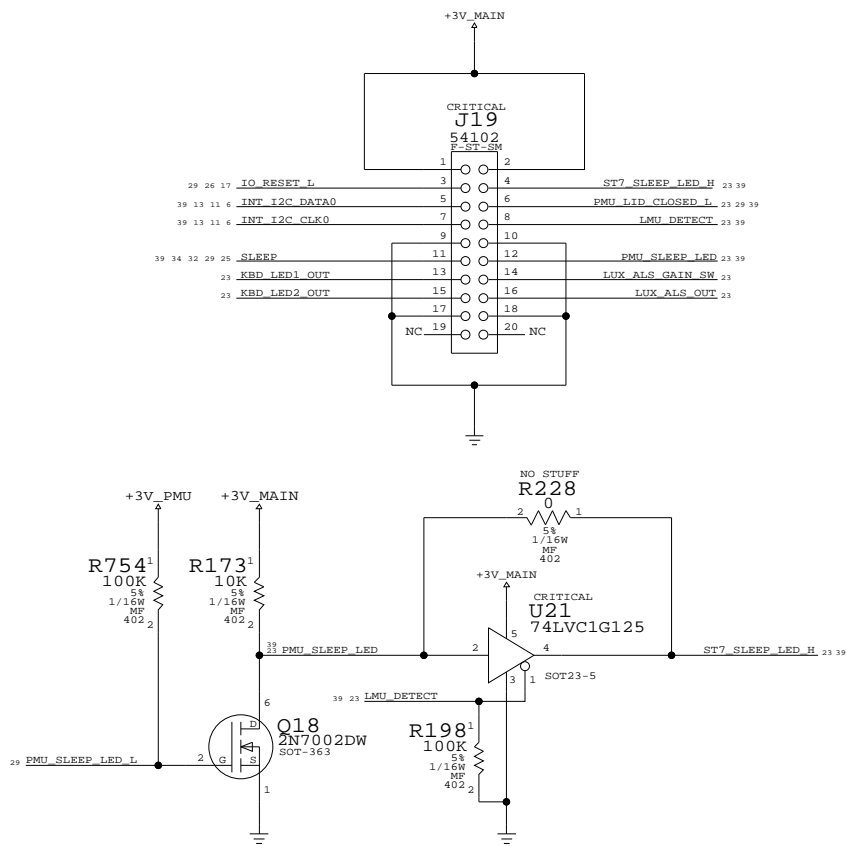
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S1331	2	DISCRETE, RES, 330HM, 0402	L36, L38		VGA_BUFFER_RES

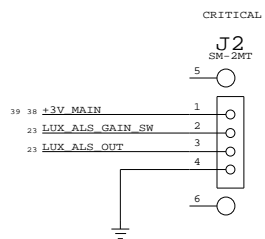
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
152S0214	3	IND, FERRITE, 27NH, 10%, 0805	L49, L43, L40	?
152S0210	3	IND, FERRITE, 27NH, 10%, 0805	L50, L44, L41	?
131S1114	3	CAP, CER, 1.5PF, +/- .25PF, 0402	C642, C635, C632	?
131S1121	3	CAP, CER, 8.2PF, +/- .25PF, 0402	C641, C634, C631	?

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6888	REV. B
	SCALE NONE	SHT 22	OF 40

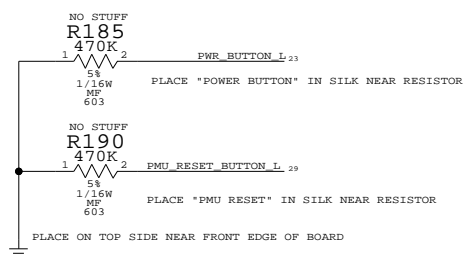
LMU/RIGHT SENSOR CONNECTOR



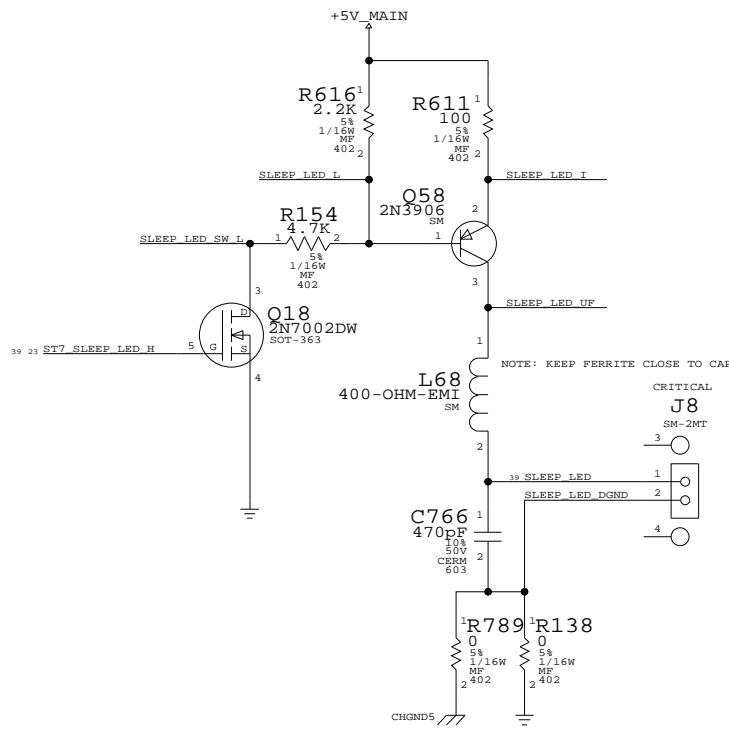
LEFT LIGHT SENSOR CONNECTOR



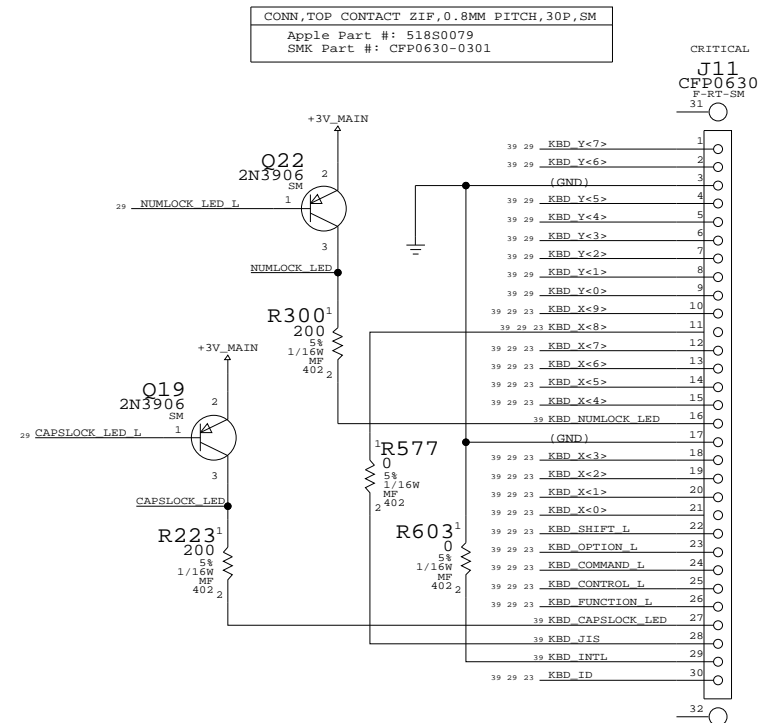
DEBUG HELPERS



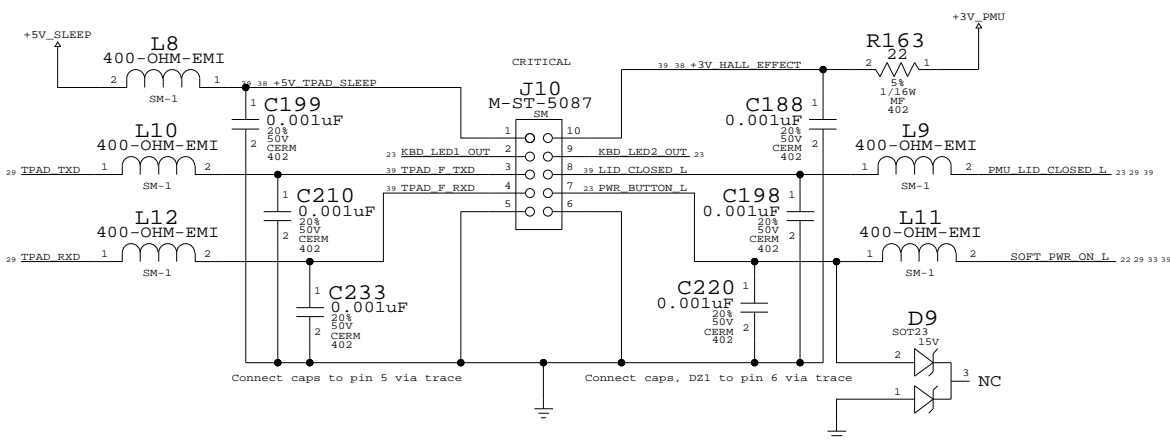
SLEEP LED



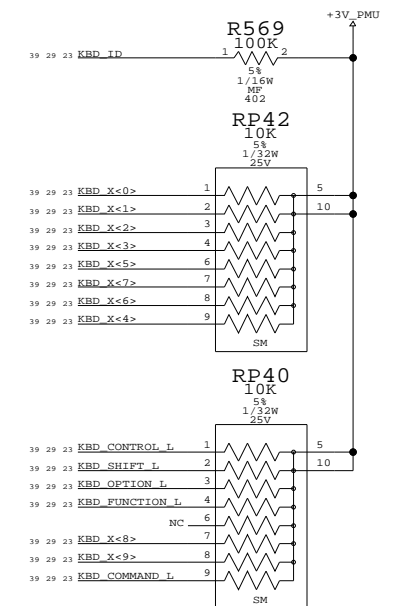
TOP CONTACT ZIF KEYBOARD CONN



TRACKPAD/PWR BTN CONN



KEYBOARD PULLUPS



KEYBOARD/TPAD/SLEEP LED

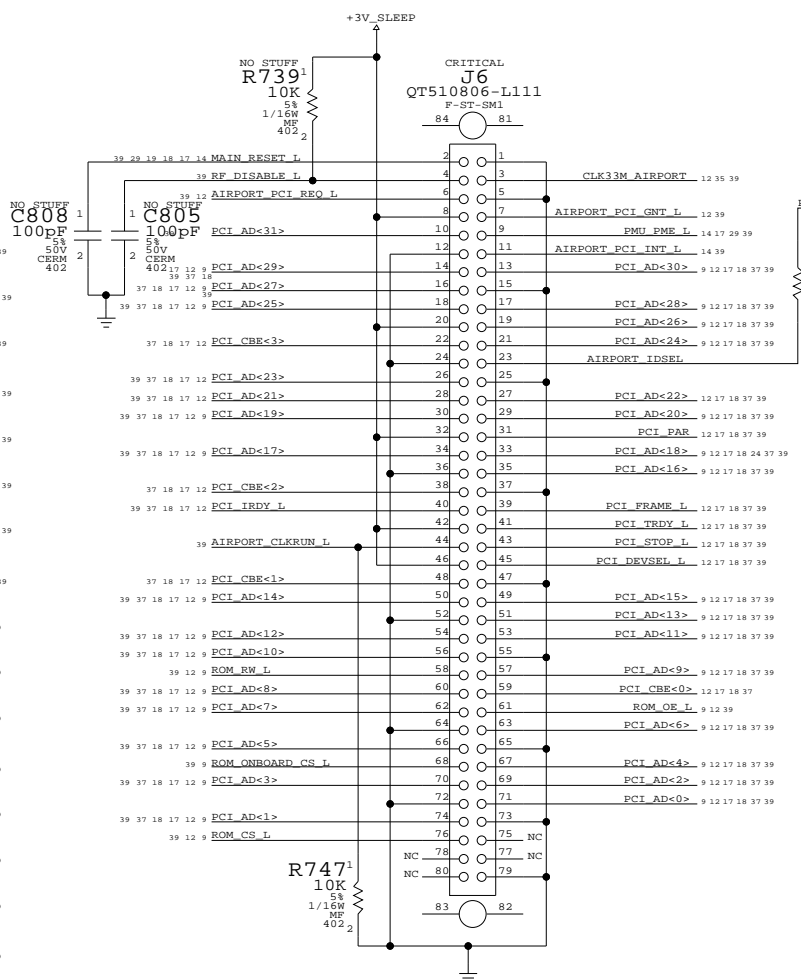
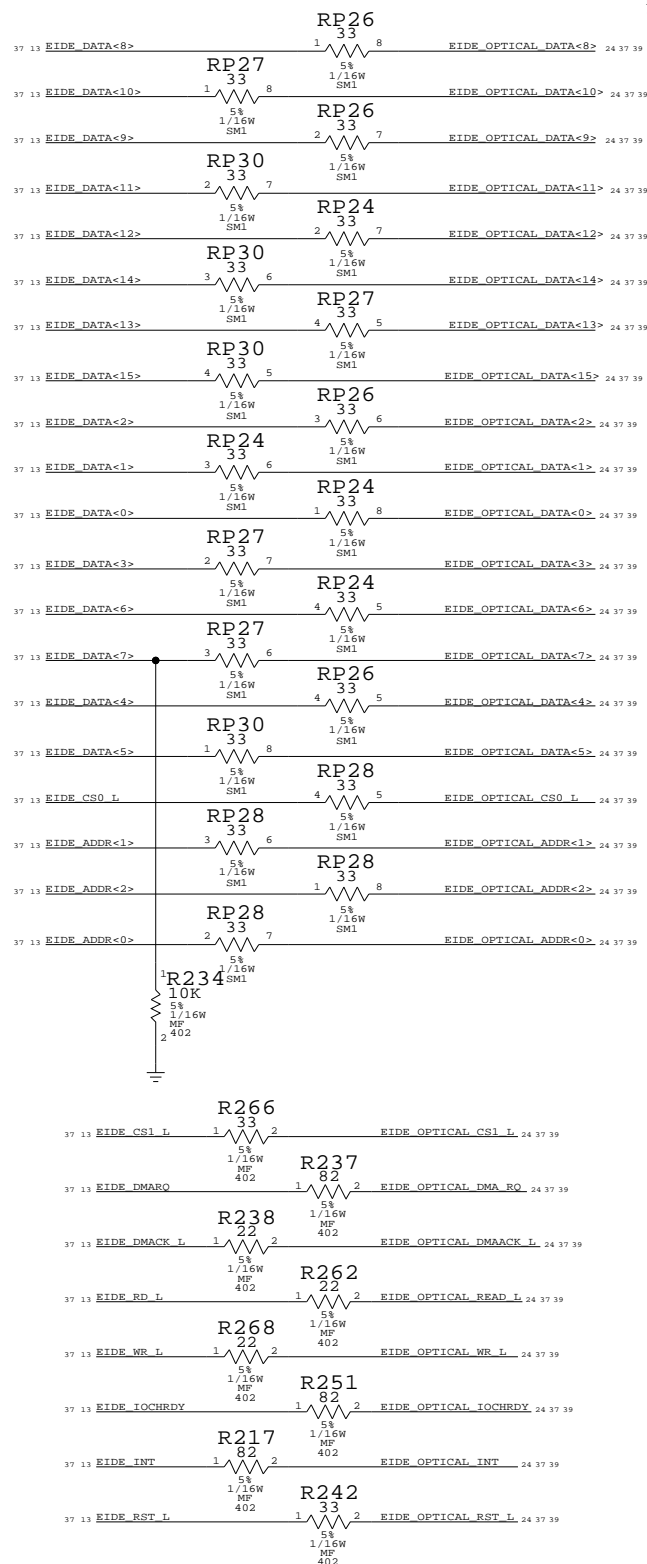
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	NONE	051-6888	B
SCALE		SHT OF	
NONE		23 OF 40	

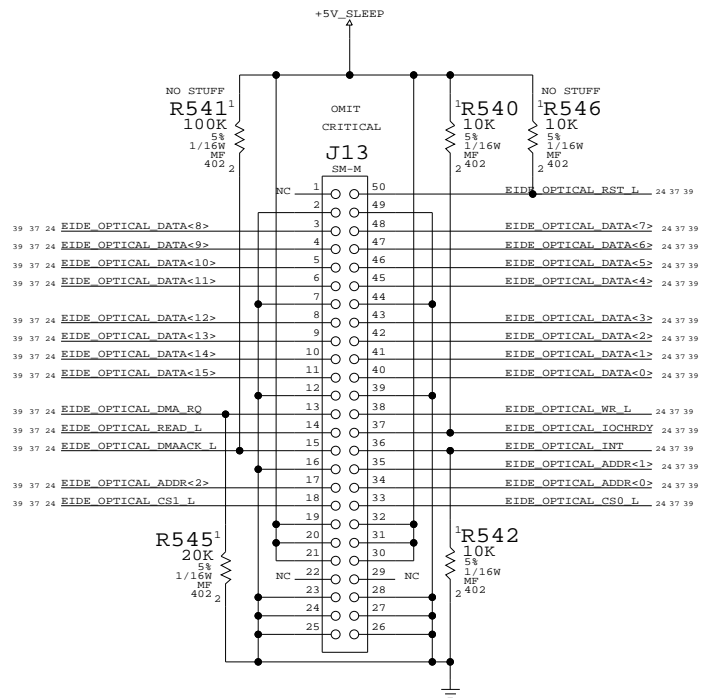
WIRELESS INTERFACE

HARD DRIVE INTERFACE (UATA100)

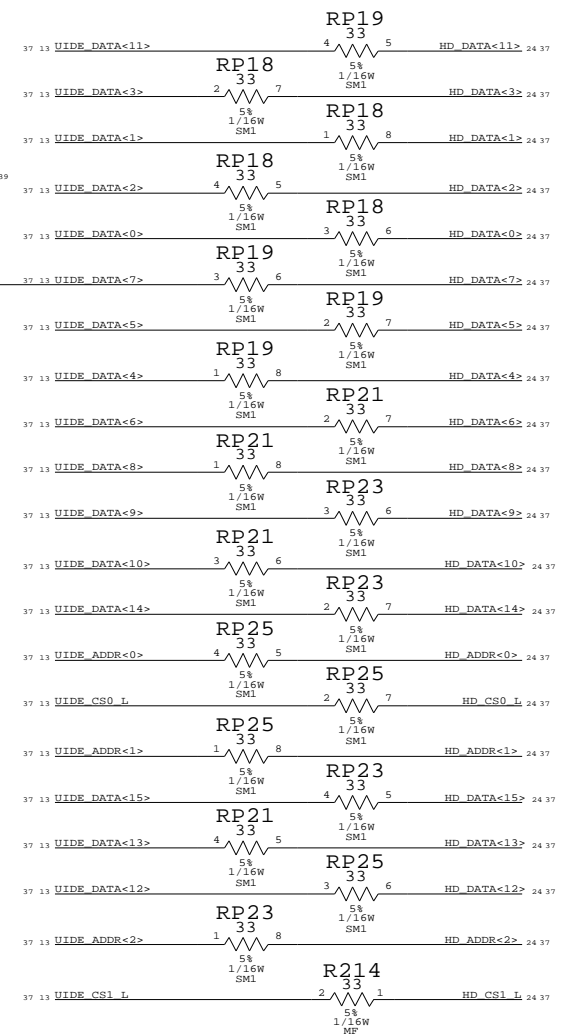
EIDE SERIES TERMINATION
PLACE TERMINATORS NEAR INTREPID



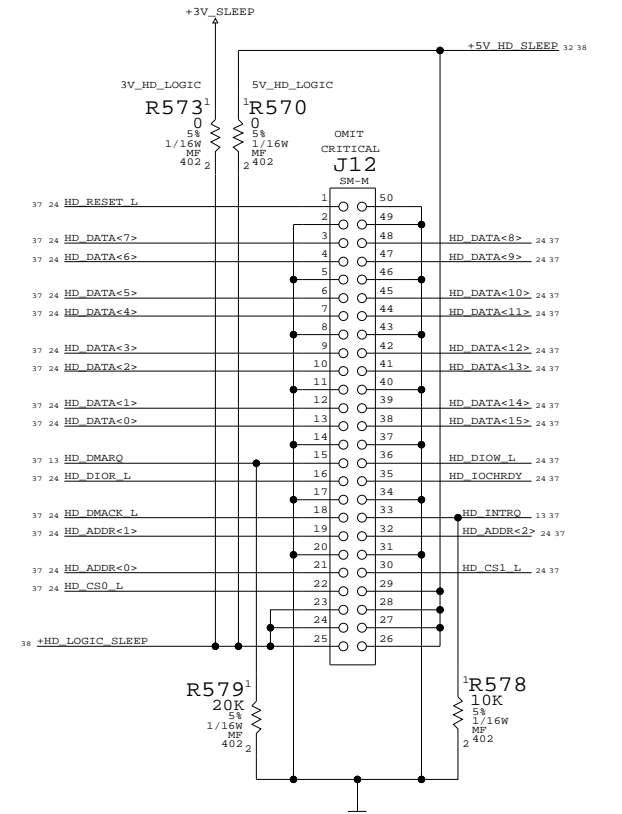
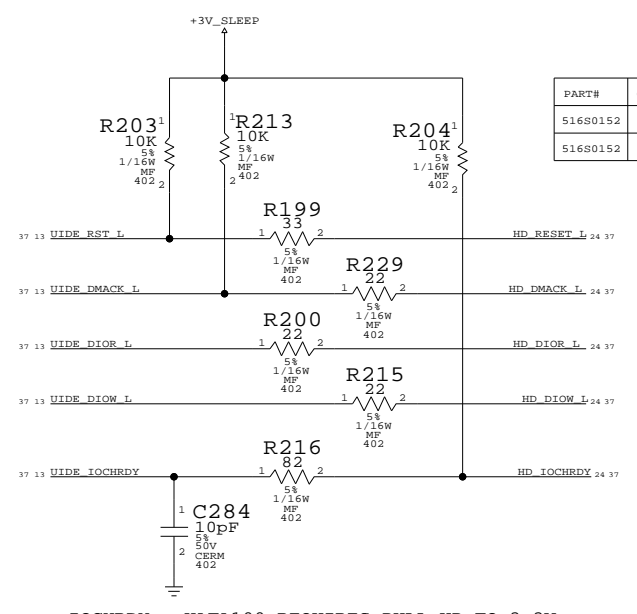
OPTICAL DRIVE INTERFACE (EIDE)



PLACE SERIES R CLOSE TO INTERPID



PLACE PULLUP RESISTORS CLOSE TO INTREPID



ANY SEQUENCING REQUIREMENT BETWEEN
+5V_HD_SLEEP AND +3V_SLEEP

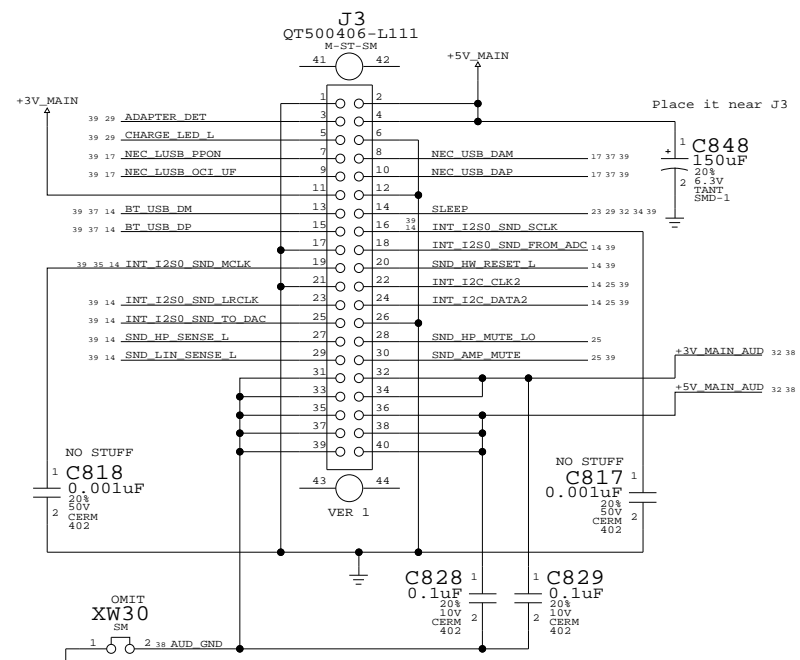
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S0152	1	CONN, PLUG, 0.5MM PITCH, 1.5MM STACK, 50P, GOLD	J12	CRITICAL	?
516S0152	1	CONN, PLUG, 0.5MM PITCH, 1.5MM STACK, 50P, GOLD	J13	CRITICAL	?

INTERNAL I/O CONNECTORS

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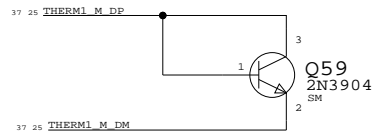
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6888	B
SCALE	SHT	24 OF 40	
NONE			

LEFT I/O & AUDIO BOARD (LIO)

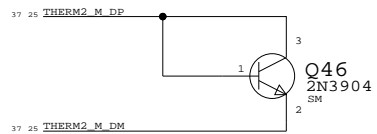


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S0154	1	CONN, PLUG, 0.5MM PITCH, 1.5MM STACK, 40P, GOLD	J3	CRITICAL	?

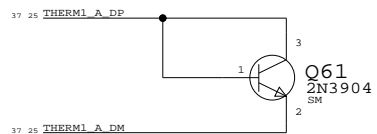
PLACE CLOSE TO CPU MAIN1



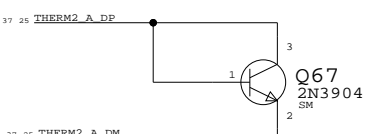
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY MAIN2



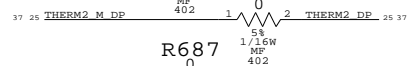
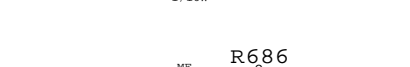
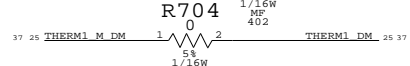
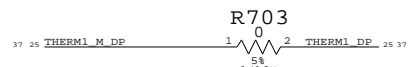
PLACE UNDERNEATH UPPER RAM ALTERNATE1



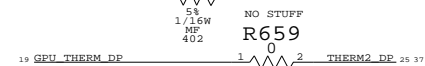
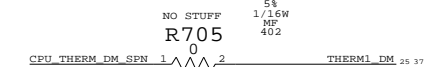
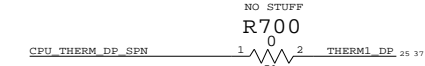
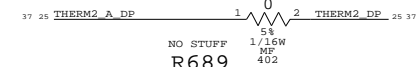
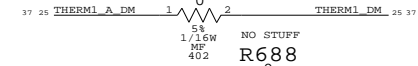
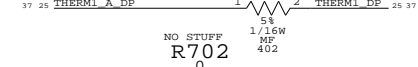
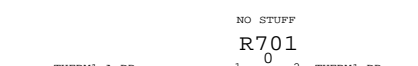
PLACE CLOSE TO BATTERY CHARGER/VCORE ALTERNATE2



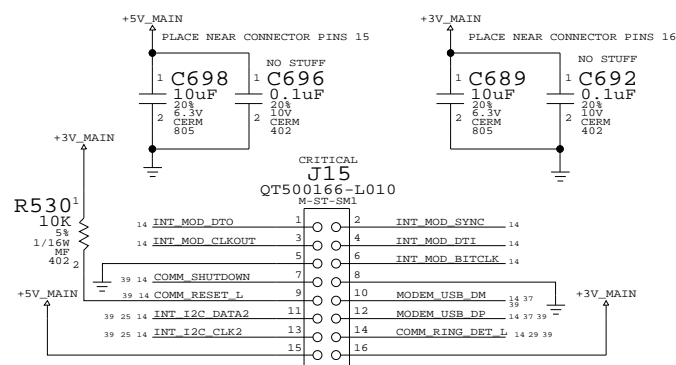
KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER



KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

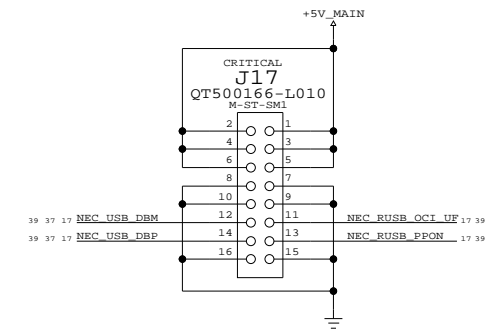


USB MODEM/SOFT MODEM

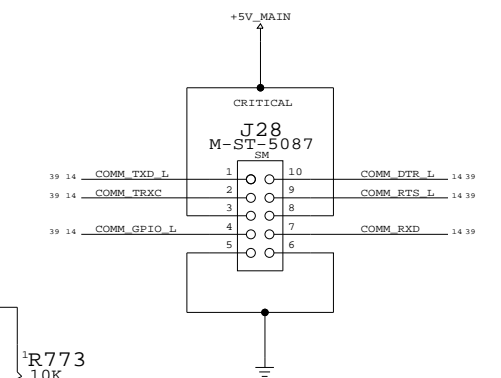


MODEM I2C ADDR ASSIGNED VIA FLEX CABLE

RIGHT USB BOARD

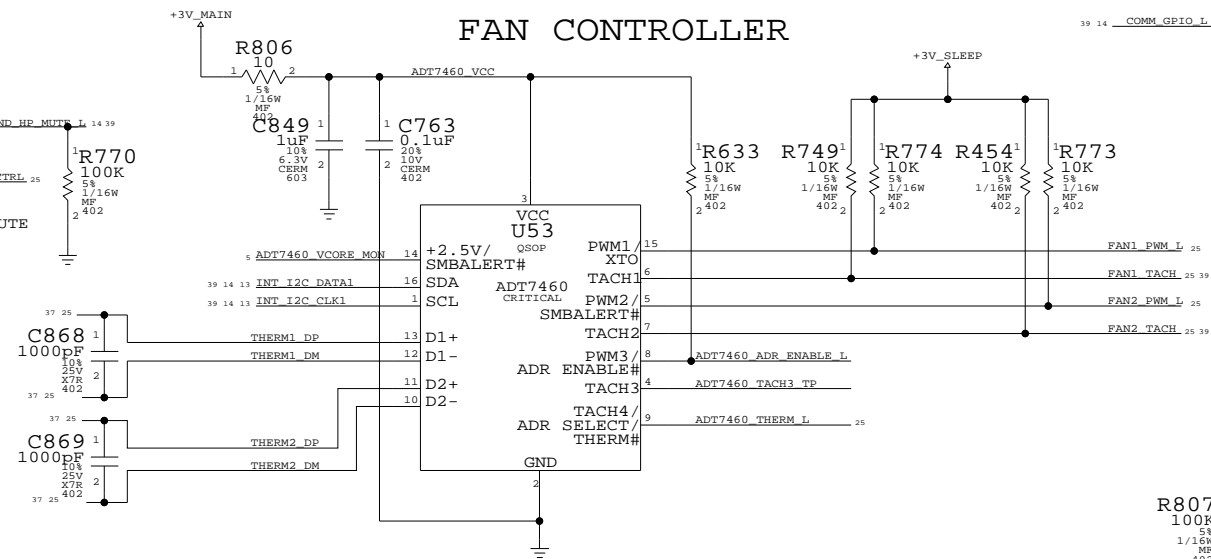


SERIAL DEBUG INTERFACE

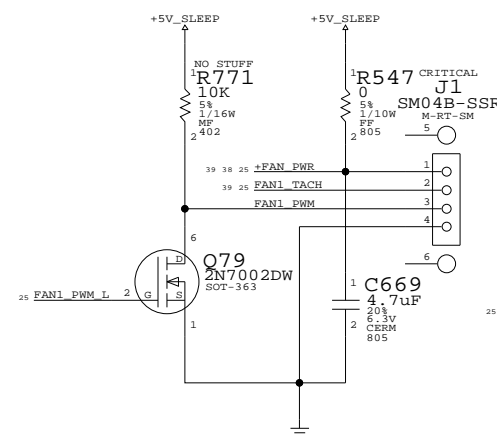


FAN INTERFACE

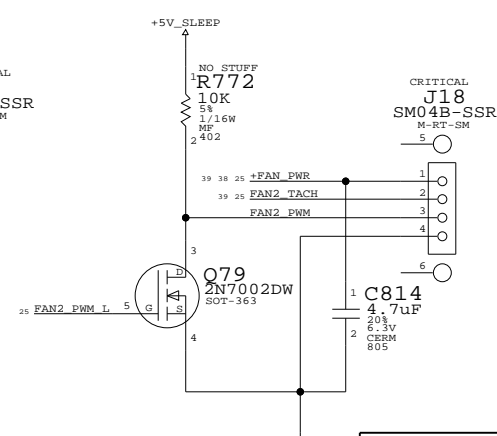
FAN CONTROLLER



CPU FAN



GPU FAN



FAN/MODEM/SOUND/BACKUP BATT.

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	D	051-6888	B
SCALE	NONE	SHT	25 OF 40

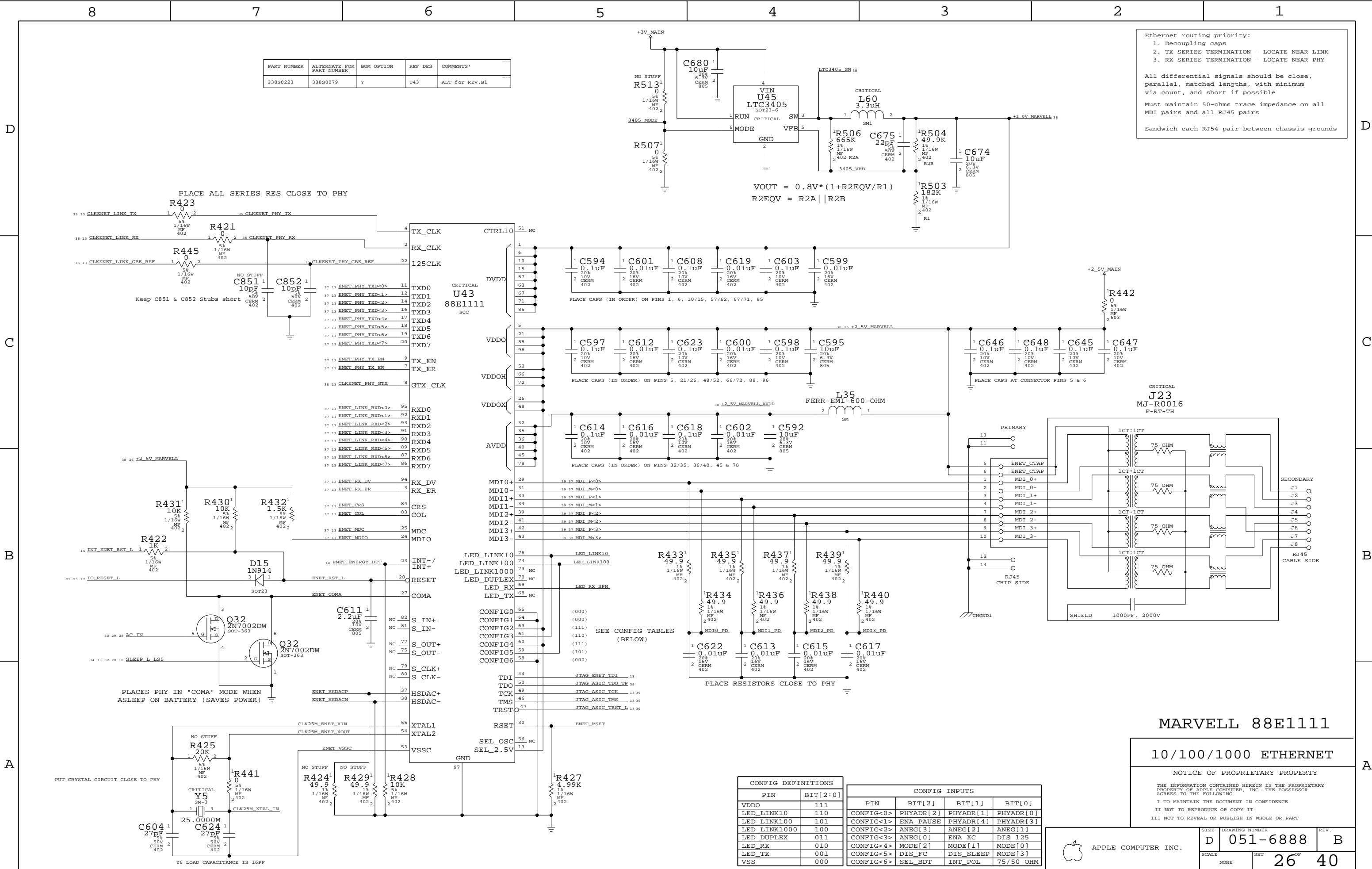
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
338S0223	338S0079	?	U43	ALT for REV.B1

Ethernet routing priority:
 1. Decoupling caps
 2. TX SERIES TERMINATION - LOCATE NEAR LINK
 3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds



PLACE ALL SERIES RES CLOSE TO PHY

NO STUFF
 C851 10pF
 C852 10pF
 Keep C851 & C852 Stubs short

PLACES PHY IN "COMA" MODE WHEN ASLEEP ON BATTERY (SAVES POWER)

$$V_{OUT} = 0.8V * (1 + R2EQV/R1)$$

$$R2EQV = R2A | R2B$$

PLACE CAPS (IN ORDER) ON PINS 1, 6, 10/15, 57/62, 67/71, 85

PLACE CAPS (IN ORDER) ON PINS 5, 21/26, 48/52, 66/72, 88, 96

PLACE CAPS (IN ORDER) ON PINS 32/35, 36/40, 45 & 78

PLACE RESISTORS CLOSE TO PHY

LED_LINK10
 LED_LINK100
 LED_LINK1000
 LED_DUPLEX
 LED_RX
 LED_TX
 LED_RX_SPN

CONFIG0 (000)
 CONFIG1 (000)
 CONFIG2 (111)
 CONFIG3 (110)
 CONFIG4 (111)
 CONFIG5 (101)
 CONFIG6 (000)

SEE CONFIG TABLES (BELOW)

MARVELL 88E1111

10/100/1000 ETHERNET

NOTICE OF PROPRIETARY PROPERTY

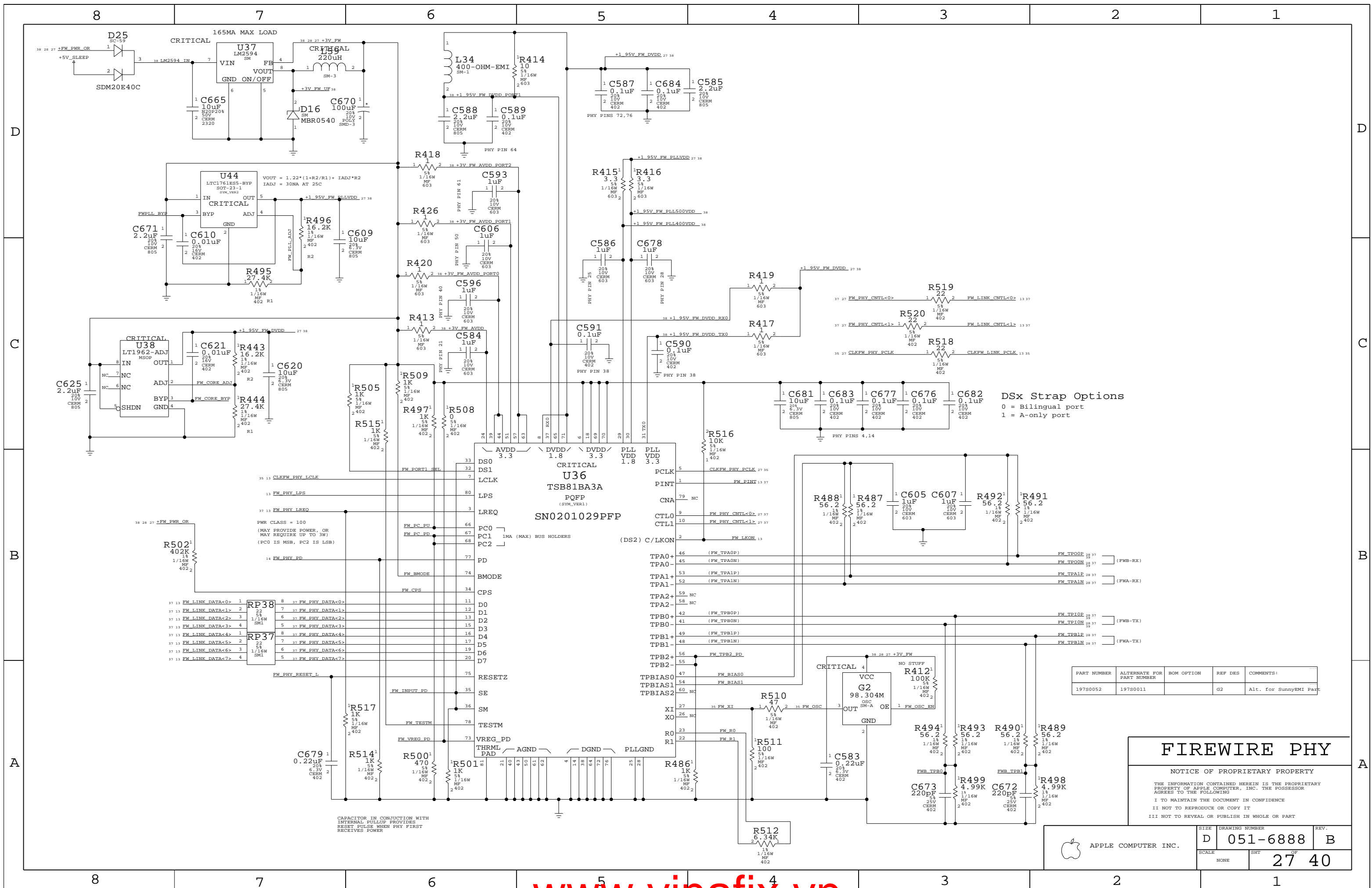
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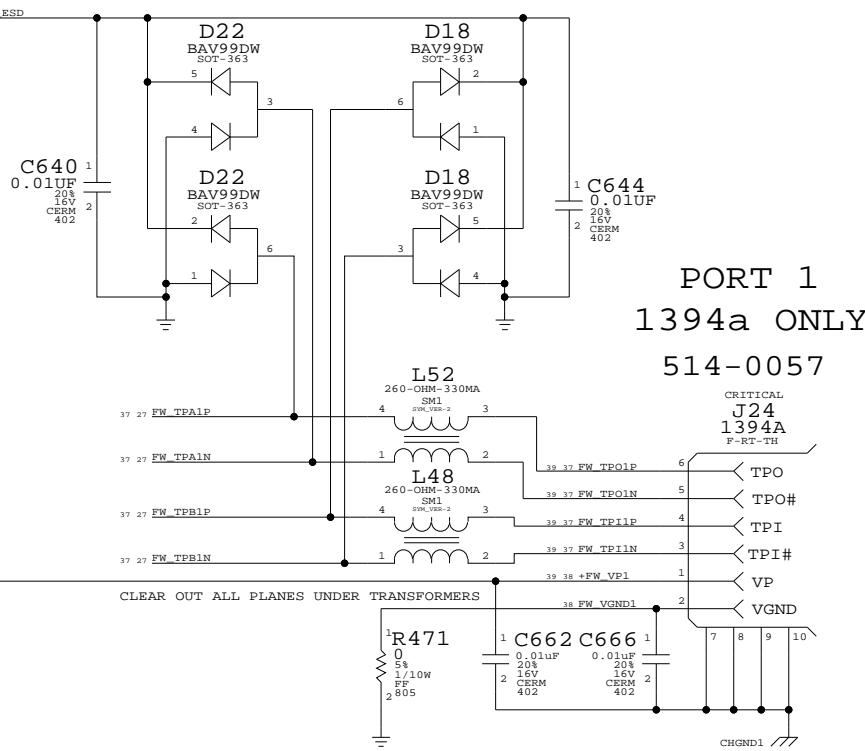
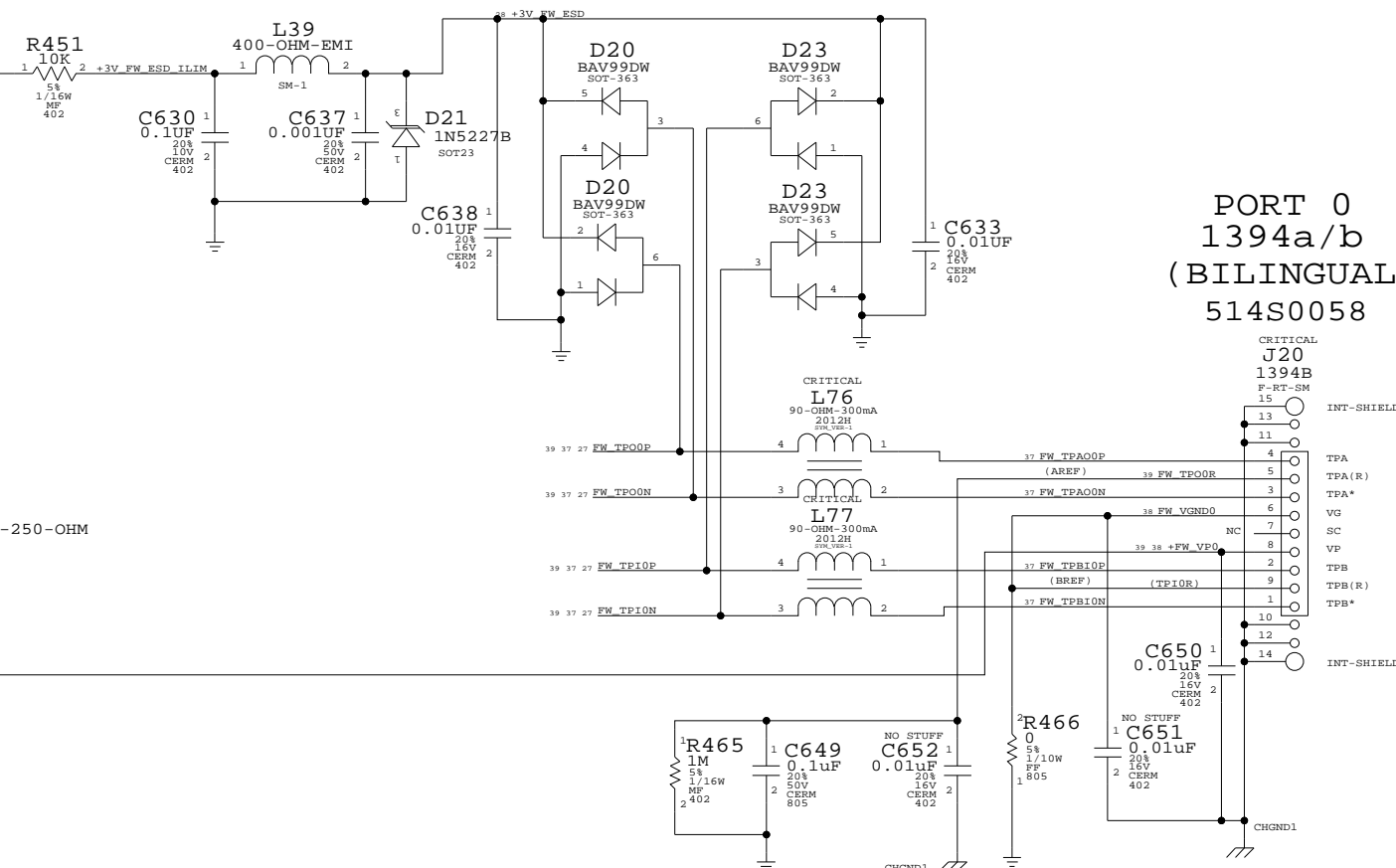
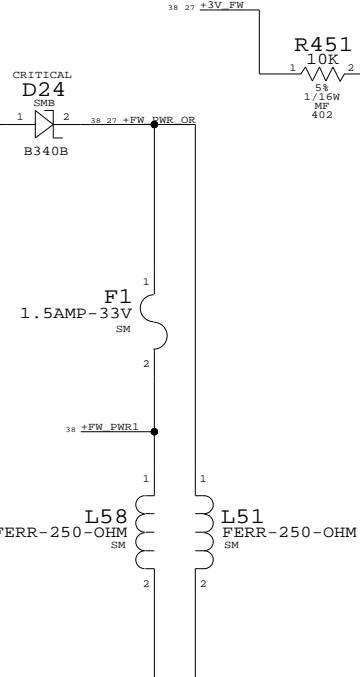
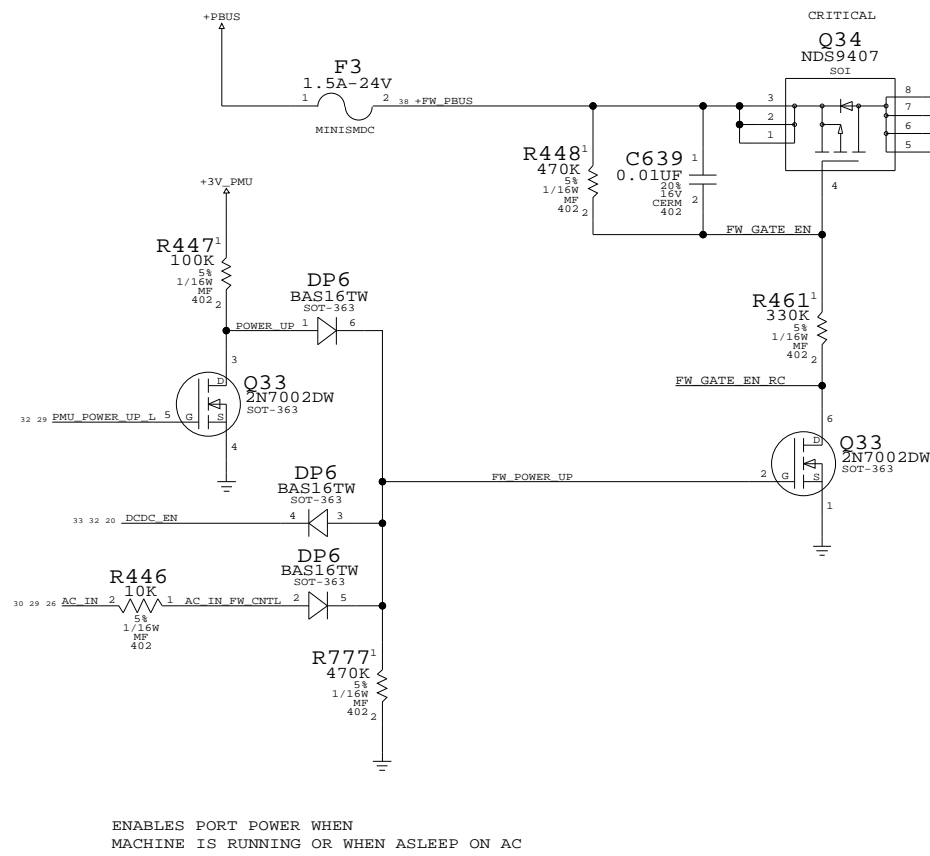
CONFIG DEFINITIONS	
PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS			
PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6888	B
SCALE	SHT	26 OF 40	
NONE			



PORT POWER SWITCH



FIREWIRE PORTS

NOTICE OF PROPRIETARY PROPERTY

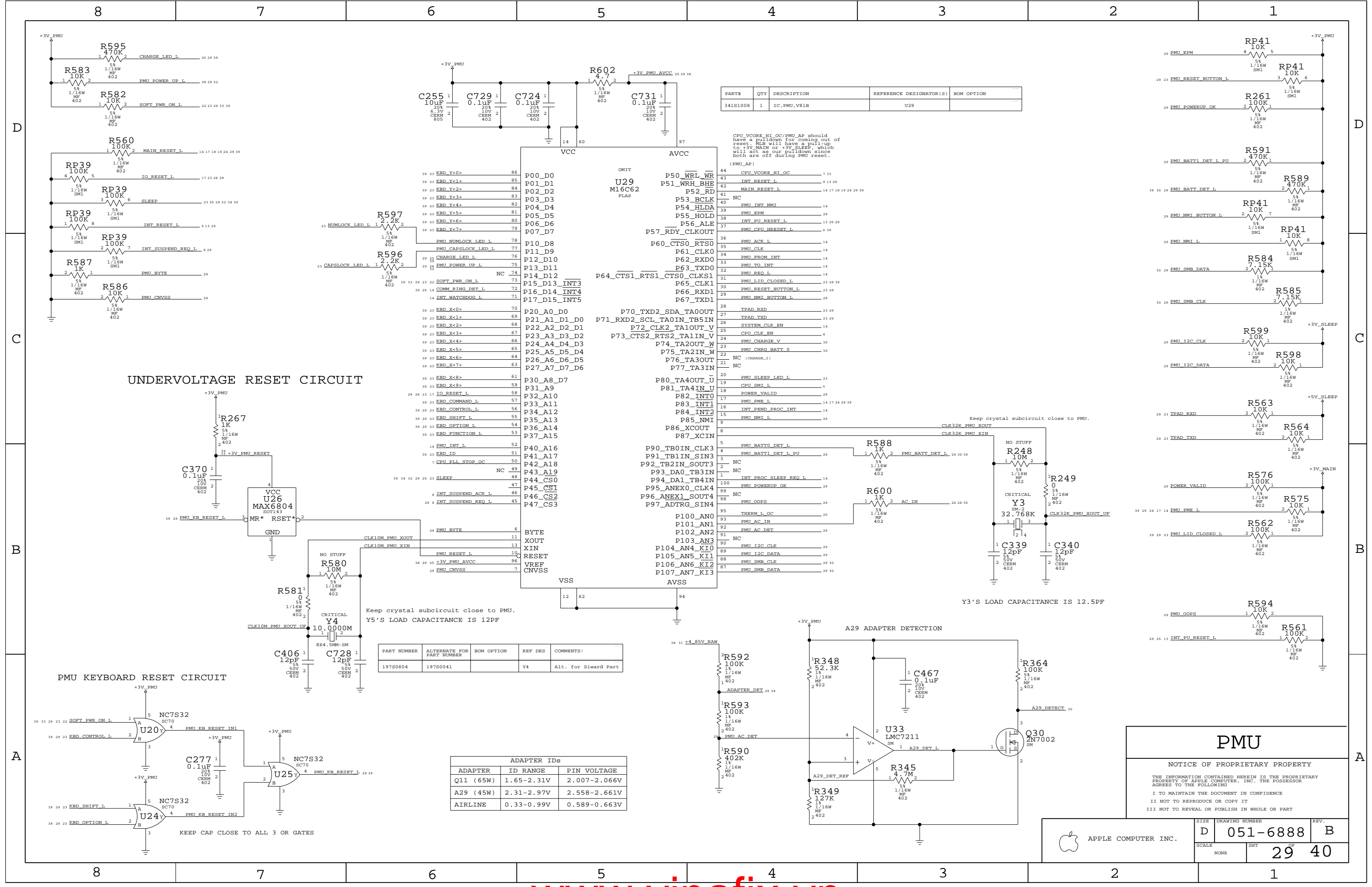
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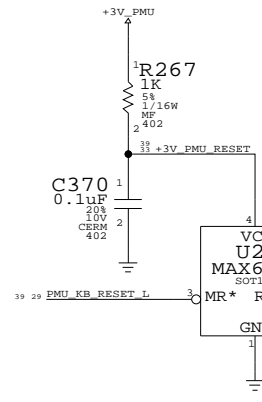
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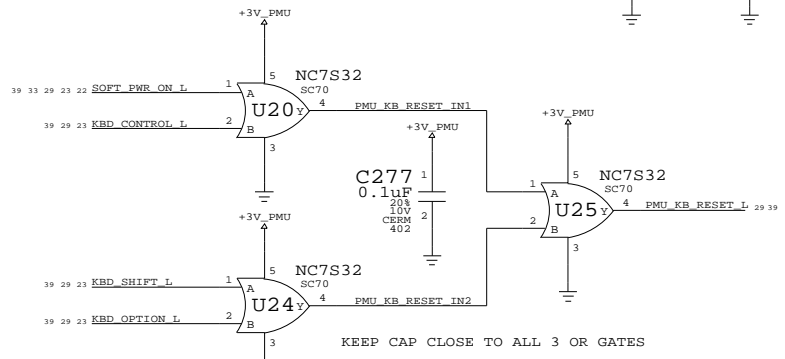
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6888	B
SCALE	NONE	SHT	OF
		28	40



UNDERVOLTAGE RESET CIRCUIT



PMU KEYBOARD RESET CIRCUIT



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
197S0604	197S0041		Y4	Alt. for Sward Part

ADAPTER IDS			
ADAPTER	ID RANGE	PIN VOLTAGE	
Q11 (65W)	1.65-2.31V	2.007-2.066V	
A29 (45W)	2.31-2.97V	2.558-2.661V	
AIRLINE	0.33-0.99V	0.589-0.663V	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1008	1	IC, PMU, V81B	U29	

CPU_VCORE_HI_OC/PMU_AP should have a pullup for coming out of reset. MIB will have a pull-up to +3V_MAIN or +3V_SLEEP which will act as our pulldown since both are off during PMU reset.

(PMU_AP)

PMU

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6888	B
SCALE	SHT	29 OF 40

DC POWER INPUT

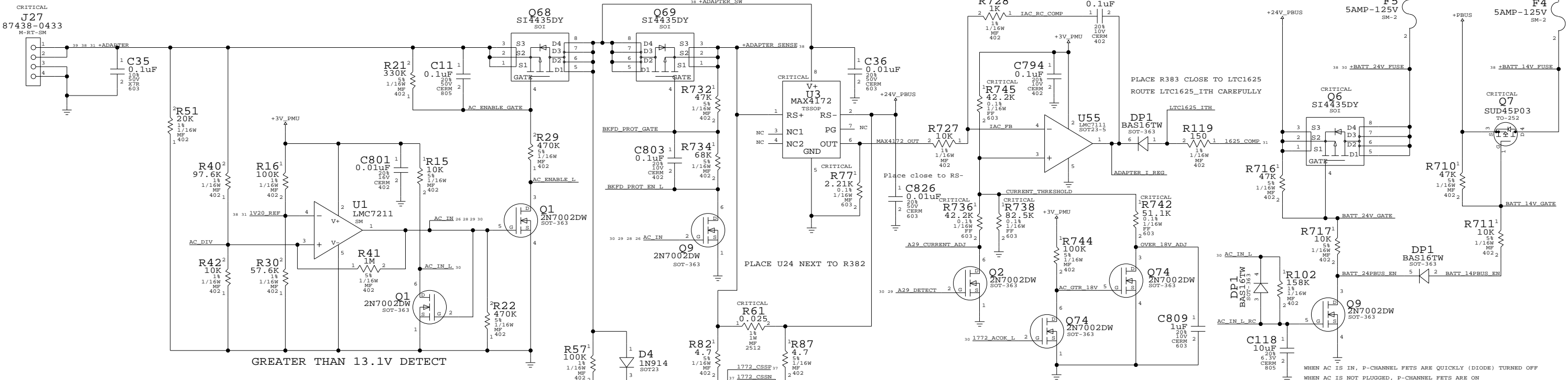
(POWER JACK, ETC. ON SEPARATE BOARD)

DC INRUSH LIMITER

BACKFEED PROTECTION

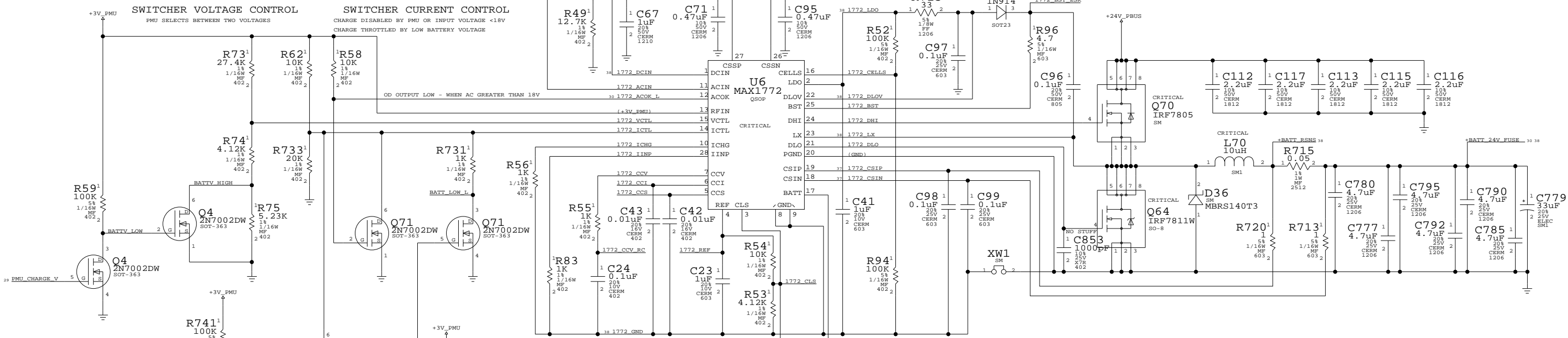
+PBUS CURRENT LIMIT

BATTERY SWITCH-OVER CIRCUIT



SWITCHER VOLTAGE CONTROL

SWITCHER CURRENT CONTROL



$$V_{BATT} = CELLS \times (4.096 + (0.4096 \times V_{VCTL} / V_{REFIN}))$$

$$I_{CHG} = (0.2048 / R_{62}) \times (V_{ICTL} / V_{REFIN})$$

For 4.15V cells, VCTL = 0.123 REFIN
 For 4.20V cells, VCTL = 0.245 REFIN

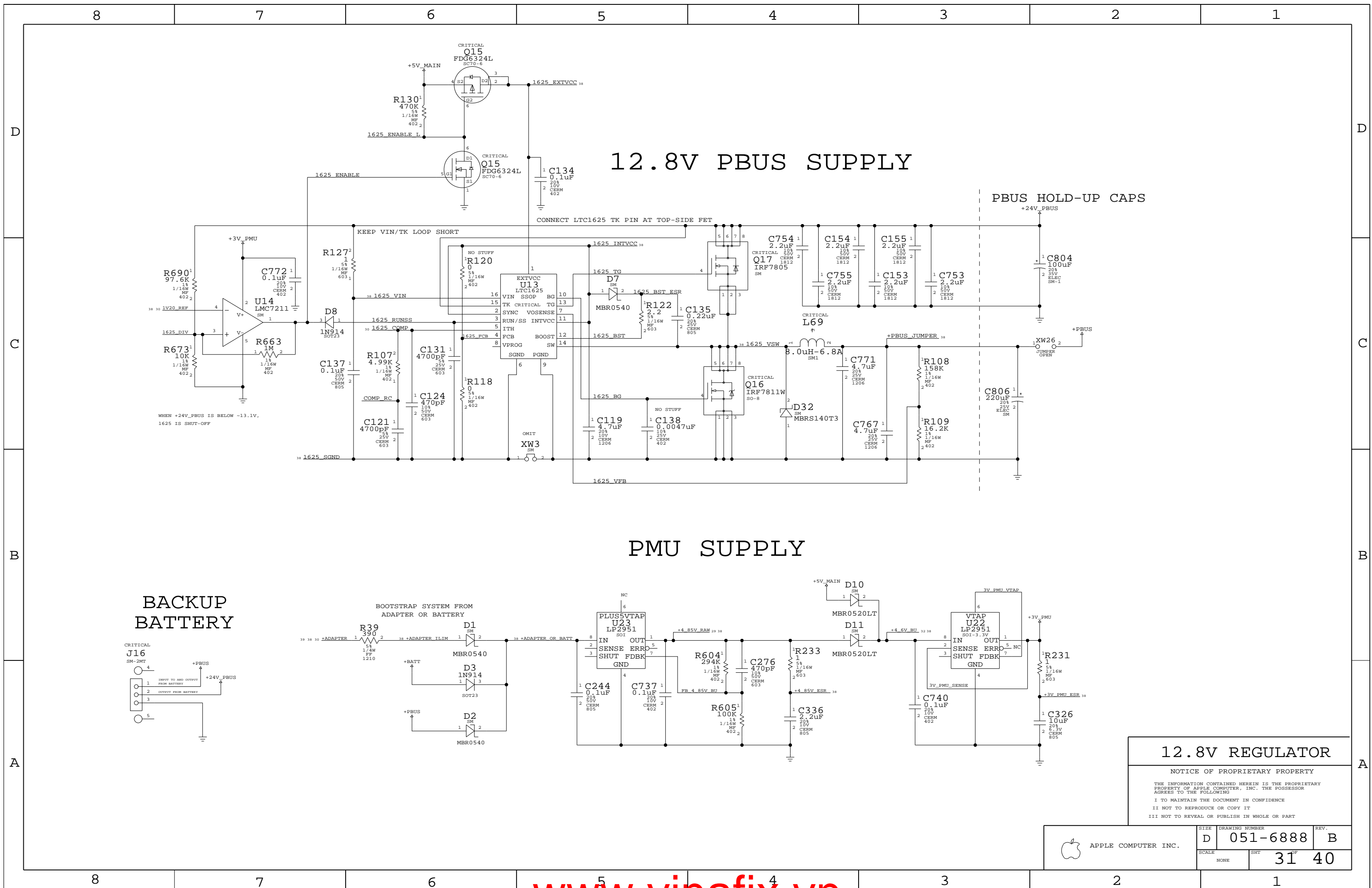
BATTERY CHARGER

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SCALE NONE	SIZE D	DRAWING NUMBER 051-6888	REV. B
	SHEET 30 OF 40		



12.8V PBUS SUPPLY

PBUS HOLD-UP CAPS

PMU SUPPLY

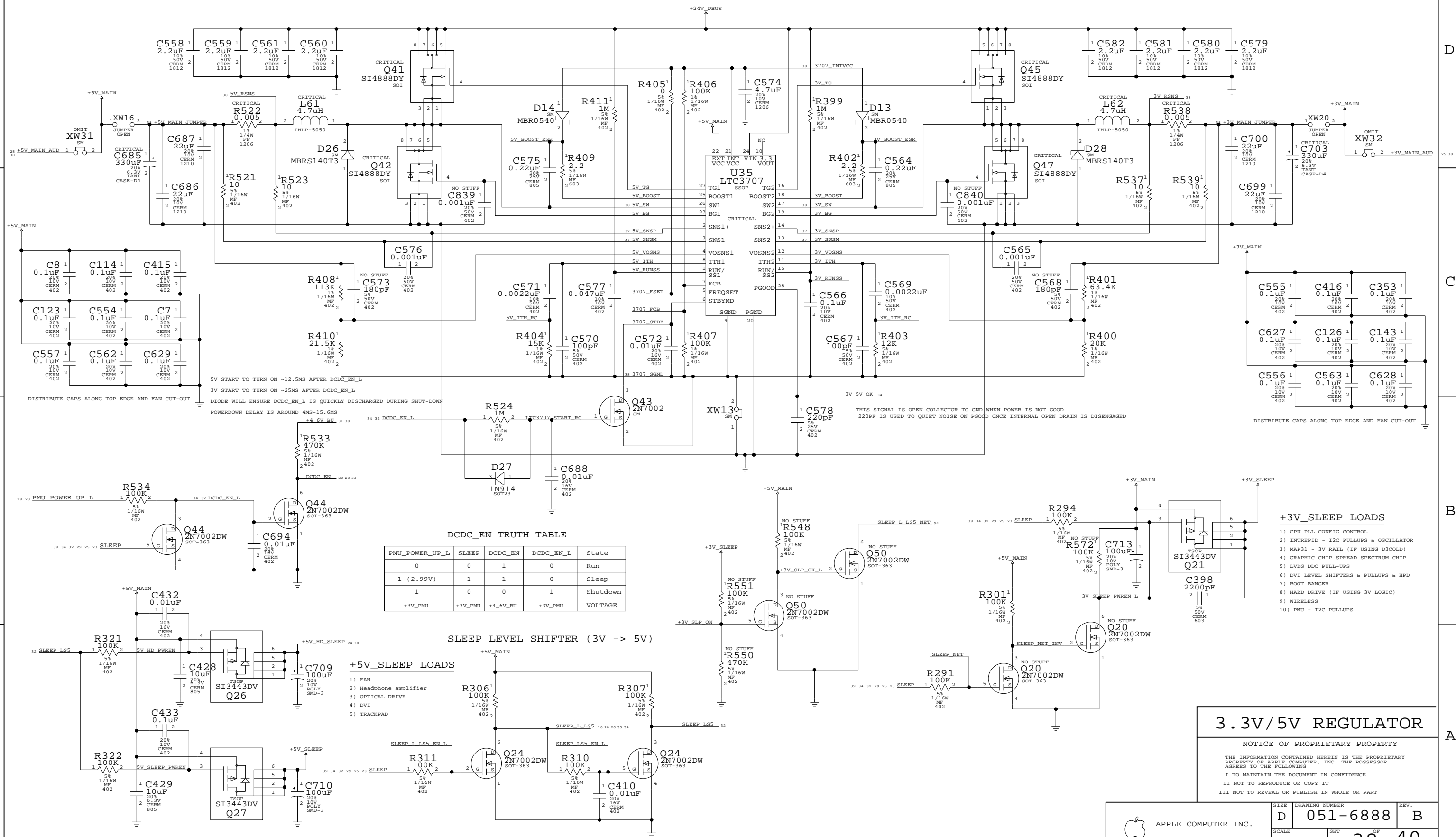
BACKUP BATTERY

12.8V REGULATOR

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	D	051-6888	B
SCALE	SHT		31 40
NONE			

3.3V/5V MAIN SUPPLY

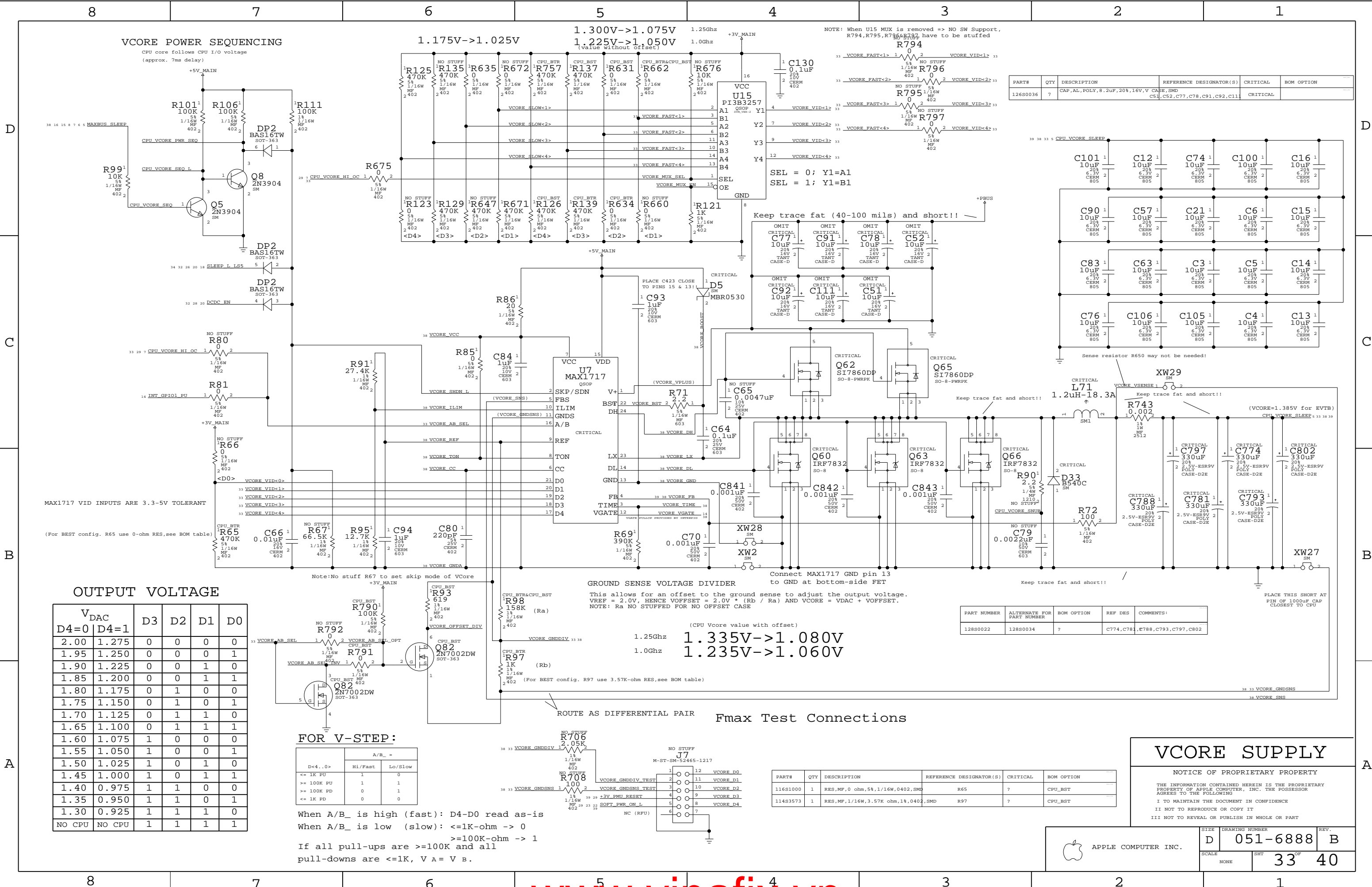


3.3V/5V REGULATOR

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6888	B
SCALE	SHT	OF	
NONE		32 40	



VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage (approx. 7ms delay)

1.175V->1.025V

1.300V->1.075V
1.225V->1.050V
(value without offset)

NOTE: When U15 is removed => NO SW Support, R794, R795, R796, R797 have to be stuffed

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
126S0036	7	CAP,AL,POLY,8.2uF,20%,16V,V	C51,C52,C77,C78,C91,C92,C111	CRITICAL	

OUTPUT VOLTAGE

V _{DAC}		D3	D2	D1	D0
D4=0	D4=1				
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ =	
	Hi/Fast	Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

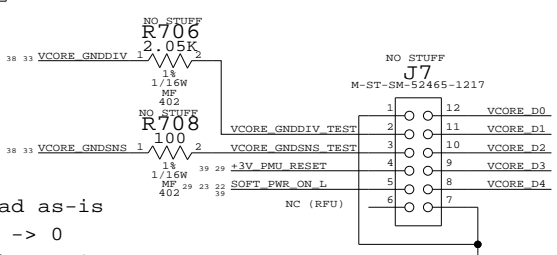
When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1
If all pull-ups are >=100K and all pull-downs are <=1K, V_A = V_B.

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage. VREF = 2.0V, HENCE VOFFSET = 2.0V * (Rb / Ra) AND VCORE = VDVC + VOFFSET. NOTE: Ra NO STUFFED FOR NO OFFSET CASE

	(CPU Vcore value with offset)
1.25Ghz	1.335V->1.080V
1.0Ghz	1.235V->1.060V

Fmax Test Connections



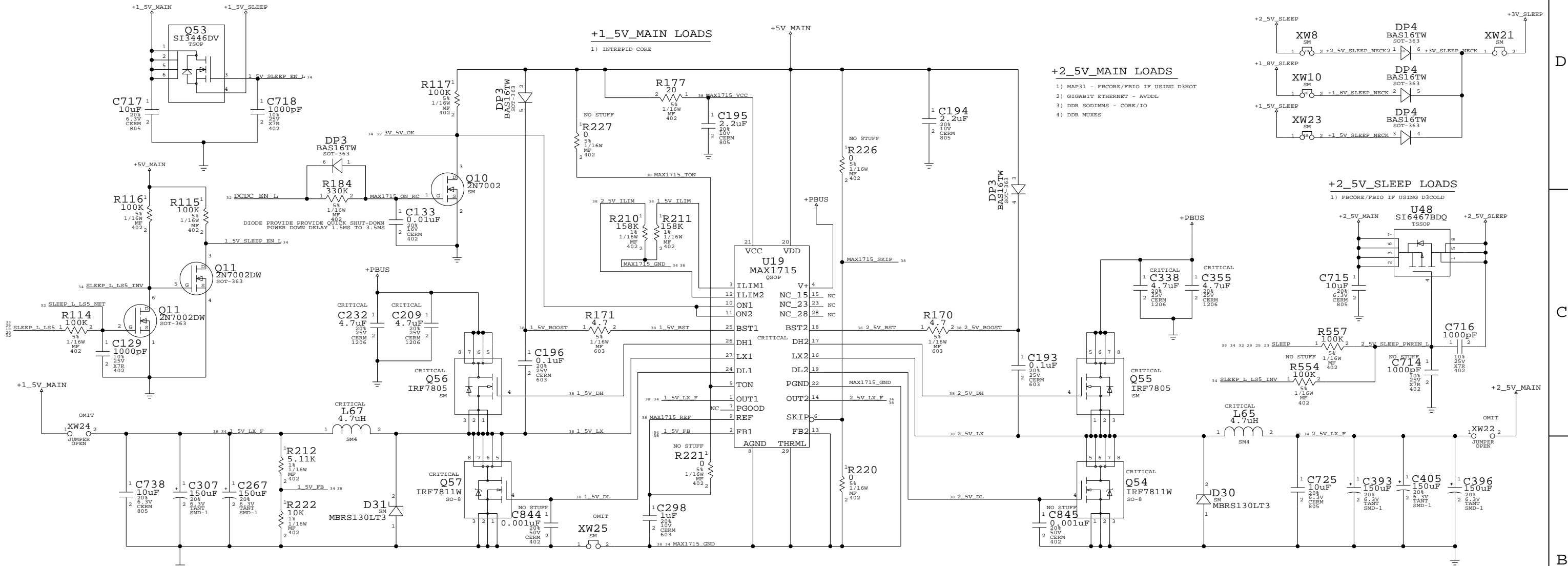
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0022	128S0034	?	C774,C781,C782,C793,C797,C802	

VCORE SUPPLY

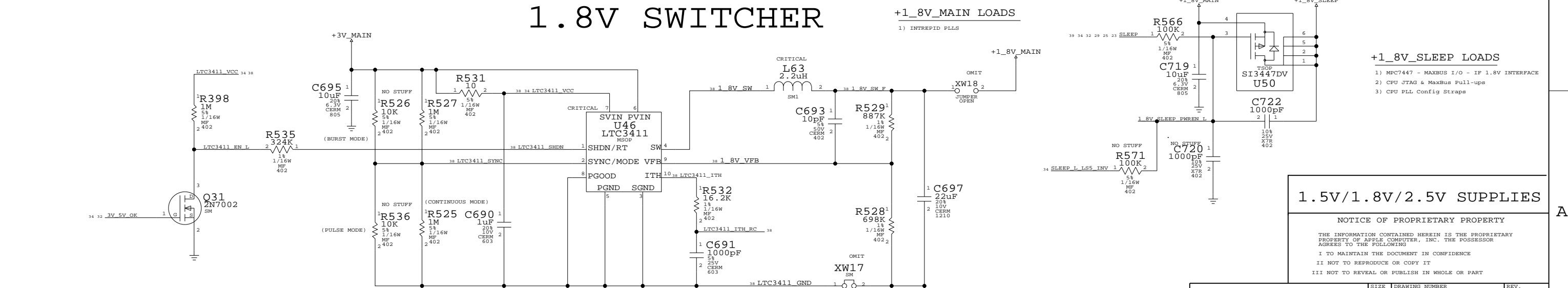
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	D	051-6888	B
SCALE	SHT	33 OF 40	
NONE			

1.5V/2.5V SWITCHER



1.8V SWITCHER



1.5V/1.8V/2.5V SUPPLIES

NOTICE OF PROPRIETARY PROPERTY

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6888	B
SCALE	SHT	34 40	
NONE			

		8		7		6		5		4		3		2		1								
		GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	CLOCK LINE CONSTRAINTS													
											GROUP	SIG_NAME	PROPAGATION_DELAY	MATCHED_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE_PARAM					
DIGITAL SIGNALS	D	GROUP 0	MEM_DATA<7..0>	L:S:1602:1700	7	500	(200)				167 MHZ	INTREPID CLOCKS	SYSCLK_CPU_UP	L:S:1150 MTL					10 MTL SPACING	167.0 MHz	8			
			MEM_DQM<0>	L:S:1602 MTL:1700 MTL	7	500.0000	(200)					167.0 MHz	INTREPID CLOCKS	SYSCLK_CPU	L:S:2650 MTL:2750 MTL		5	250.0000	(200)	10 MTL SPACING	167.0 MHz	8	9	
			MEM_DQS<0>	L:S:1602 MTL:1700 MTL	7	500.0000	(200)					167.0 MHz	INTREPID CLOCKS	INT_CPUFB_OUT	L:S:1150 MTL		5	250.0000		10 MTL SPACING	167.0 MHz	8	9	
			RAM_DATA_A<7..0>	L:S:1903:2000	7	500	(200)					167 MHZ	INTREPID CLOCKS	INT_CPUFB_OUT_SHORT	L:S:700 MTL:850 MTL		5	250.0000		10 MTL SPACING	167.0 MHz	8	9	
			RAM_DQM_A<0>	L:S:1903 MTL:2000 MTL	7	500.0000	(200)					167.0 MHz	INTREPID CLOCKS	INT_CPUFB_OUT_NORM	L:S:500 MTL:600 MTL		5	250.0000		10 MTL SPACING	167.0 MHz	8	9	
			RAM_DQS_A<0>	L:S:1903 MTL:2000 MTL	7	500.0000	(200)					167.0 MHz	INTREPID CLOCKS	INT_CPUFB_IN_NORM	L:S:500 MTL:600 MTL		5	250.0000		10 MTL SPACING	167.0 MHz	8	9	
			RAM_DATA_B<7..0>	L:S:2000:2100	7	500	(200)					167 MHZ	INTREPID CLOCKS	INT_CPUFB_LONG	L:S:1050 MTL:1150 MTL		5	250.0000		10 MTL SPACING	167.0 MHz	8	9	
			RAM_DQM_B<0>	L:S:2000 MTL:2100 MTL	7	500.0000	(200)					167.0 MHz	INTREPID CLOCKS	INT_CPUFB_IN	L:S:700 MTL:800 MTL		5	250.0000	(200)	10 MTL SPACING	167.0 MHz	8	9	
		RAM_DQS_B<0>	L:S:2000 MTL:2100 MTL	7	500.0000	(200)					167.0 MHz	INTREPID CLOCKS												
		GROUP 1	MEM_DATA<15..8>	L:S:1344:1660	7	500	(200)					167 MHZ		SYSCLK_DDRCLK_A0_UP	L:S:300 MTL:360 MTL	SYSCLK_DDRCLK_A0_UP:G:L:S:0 MTL:25 MTL			(200)	10 MTL SPACING	167.0 MHz	9		
			MEM_DQM<1>	L:S:1344 MTL:1660 MTL	7	500.0000	(200)					167.0 MHz		SYSCLK_DDRCLK_A0_L_UP	L:S:300 MTL:360 MTL	SYSCLK_DDRCLK_A0_L_UP:G:L:S:0 MTL:25 MTL			(200)	10 MTL SPACING	167.0 MHz	9		
			MEM_DQS<1>	L:S:1344 MTL:1660 MTL	7	500.0000	(200)					167.0 MHz		SYSCLK_DDRCLK_A1_UP	L:S:300 MTL:360 MTL	SYSCLK_DDRCLK_A1_UP:G:L:S:0 MTL:25 MTL			(200)	10 MTL SPACING	167.0 MHz	9		
			RAM_DATA_A<15..8>	L:S:1905:2000	7	500	(200)					167 MHZ		SYSCLK_DDRCLK_A1_L_UP	L:S:300 MTL:360 MTL	SYSCLK_DDRCLK_A1_L_UP:G:L:S:0 MTL:25 MTL			(200)	10 MTL SPACING	167.0 MHz	9		
			RAM_DQM_A<1>	L:S:1905 MTL:2000 MTL	7	500.0000	(200)					167.0 MHz		SYSCLK_DDRCLK_B0_UP	L:S:300 MTL:360 MTL	SYSCLK_DDRCLK_B0_UP:G:L:S:0 MTL:25 MTL			(200)	10 MTL SPACING	167.0 MHz	9		
			RAM_DQS_A<1>	L:S:1905 MTL:2000 MTL	7	500.0000	(200)					167.0 MHz		SYSCLK_DDRCLK_B0_L_UP	L:S:300 MTL:360 MTL	SYSCLK_DDRCLK_B0_L_UP:G:L:S:0 MTL:25 MTL			(200)	10 MTL SPACING	167.0 MHz	9		
			RAM_DATA_B<15..8>	L:S:2004:2412	7	500	(200)					167 MHZ		SYSCLK_DDRCLK_B1_UP	L:S:300 MTL:360 MTL	SYSCLK_DDRCLK_B1_UP:G:L:S:0 MTL:25 MTL			(200)	10 MTL SPACING	167.0 MHz	9		
			RAM_DQM_B<1>	L:S:2004 MTL:2412 MTL	7	500.0000	(200)					167.0 MHz		SYSCLK_DDRCLK_B1_L_UP	L:S:300 MTL:360 MTL	SYSCLK_DDRCLK_B1_L_UP:G:L:S:0 MTL:25 MTL			(200)	10 MTL SPACING	167.0 MHz	9		
		GROUP 2	MEM_DATA<23..16>	L:S:1435:1500	7	500	(200)					167 MHZ		SYSCLK_DDRCLK_A0_L	L:S:2900 MTL:3000 MTL	SYSCLK_DDRCLK_A0:G:L:S:0 MTL:25 MTL			(200)	10 MTL SPACING	167.0 MHz	9		
			MEM_DQM<2>	L:S:1435 MTL:1500 MTL	7	500.0000	(200)					167.0 MHz		SYSCLK_DDRCLK_A1	L:S:2900 MTL:3000 MTL	SYSCLK_DDRCLK_A1:G:L:S:0 MTL:25 MTL			(200)	10 MTL SPACING	167.0 MHz	9		
			MEM_DQS<2>	L:S:1435 MTL:1500 MTL	7	500.0000	(200)					167.0 MHz		SYSCLK_DDRCLK_A1_L	L:S:2900 MTL:3000 MTL	SYSCLK_DDRCLK_A1:G:L:S:0 MTL:25 MTL			(200)	10 MTL SPACING	167.0 MHz	9		
			RAM_DATA_A<23..16>	L:S:1707:1800	7	500	(200)					167 MHZ		SYSCLK_DDRCLK_B0	L:S:3100 MTL:3200 MTL	SYSCLK_DDRCLK_B0:G:L:S:0 MTL:25 MTL			(200)	10 MTL SPACING	167.0 MHz	9		
			RAM_DQM_A<2>	L:S:1707 MTL:1800 MTL	7	500.0000	(200)					167.0 MHz		SYSCLK_DDRCLK_B0_L	L:S:3100 MTL:3200 MTL	SYSCLK_DDRCLK_B0:G:L:S:0 MTL:25 MTL			(200)	10 MTL SPACING	167.0 MHz	9		
			RAM_DQS_A<2>	L:S:1707 MTL:1800 MTL	7	500.0000	(200)					167.0 MHz		SYSCLK_DDRCLK_B1	L:S:3100 MTL:3200 MTL	SYSCLK_DDRCLK_B1:G:L:S:0 MTL:25 MTL			(200)	10 MTL SPACING	167.0 MHz	9		
			RAM_DATA_B<23..16>	L:S:1900:2000	7	500	(200)					167 MHZ		SYSCLK_DDRCLK_B1_L	L:S:3100 MTL:3200 MTL	SYSCLK_DDRCLK_B1:G:L:S:0 MTL:25 MTL			(200)	10 MTL SPACING	167.0 MHz	9		
RAM_DQM_B<2>	L:S:1900 MTL:2000 MTL		7	500.0000	(200)					167.0 MHz														
GROUP 3	MEM_DATA<31..24>	L:S:1233:1485	7	500	(200)					167 MHZ		INT_REF_CLK_OUT_UP	L:S:400 MTL				(200)	10 MTL SPACING	49.92 MHz	14				
	MEM_DQM<3>	L:S:1233 MTL:1485 MTL	7	500.0000	(200)					167.0 MHz		INT_REF_CLK_OUT	L:S:1000 MTL:1150 MTL		5	250.0000	(200)	10 MTL SPACING	49.92 MHz	14				
	MEM_DQS<3>	L:S:1233 MTL:1485 MTL	7	500.0000	(200)					167.0 MHz		INT_REF_CLK_IN	L:S:1900 MTL:2000 MTL		5	250.0000	(200)	10 MTL SPACING	49.92 MHz	14				
	RAM_DATA_A<31..24>	L:S:1700:2165	7	500	(200)					167 MHZ		CLK66M_GPU_AGP_UP	L:S:1150 MTL				(200)	10 MTL SPACING	66.00 MHz	12				
	RAM_DQM_A<3>	L:S:1700 MTL:2165 MTL	7	500.0000	(200)					167.0 MHz		CLK66M_GPU_AGP	L:S:1800 MTL:1900 MTL		6	400.0000	(200)	10 MTL SPACING	66.00 MHz	12				
	RAM_DQS_A<3>	L:S:1700 MTL:2165 MTL	7	500.0000	(200)					167.0 MHz		INT_AGP_FB_OUT	L:S:1150 MTL				(200)	10 MTL SPACING	66.00 MHz	12				
	RAM_DATA_B<31..24>	L:S:1907:2356	7	500	(200)					167 MHZ		INT_AGP_FB_IN	L:S:1450 MTL:1550 MTL		6	500.0000	(200)	10 MTL SPACING	66.00 MHz	12				
	RAM_DQM_B<3>	L:S:1907 MTL:2356 MTL	7	500.0000	(200)					167.0 MHz		CLK33M_CBUS_UP	L:S:1250 MTL				(200)	10 MTL SPACING	33.00 MHz	12				
GROUP 4	MEM_DATA<39..32>	L:S:1915:2000	7	500	(200)					167 MHZ		CLK33M_CBUS	L:S:1500 MTL:6000 MTL		9	500.0000	(200)	10 MTL SPACING	33.00 MHz	12				
	MEM_DQM<4>	L:S:1915 MTL:2000 MTL	7	500.0000	(200)					167.0 MHz		CLK33M_AIRPORT_UP	L:S:1250 MTL				(200)	10 MTL SPACING	33.00 MHz	12				
	MEM_DQS<4>	L:S:1915 MTL:2000 MTL	7	500.0000	(200)					167.0 MHz		CLK33M_AIRPORT	L:S:9500 MTL:10500 MTL		6	500.0000	(200)	10 MTL SPACING	33.00 MHz	12				
	RAM_DATA_A<39..32>	L:S:1205:1387	7	500	(200)					167 MHZ		CLK33M_NEC_UP	L:S:1250 MTL				(200)	10 MTL SPACING	33.00 MHz	12				
	RAM_DQM_A<4>	L:S:1205 MTL:1387 MTL	7	500.0000	(200)					167.0 MHz		CLK33M_NEC	L:S:4000 MTL:6000 MTL		7	500.0000	(200)	10 MTL SPACING	33.00 MHz	12				
	RAM_DQS_A<4>	L:S:1205 MTL:1387 MTL	7	500.0000	(200)					167.0 MHz		INT_PCI_FB_OUT	L:S:300 MTL				(200)	10 MTL SPACING	33.00 MHz	12				
	RAM_DATA_B<39..32>	L:S:1404:1686	7	500	(200)					167 MHZ		INT_PCI_FB_IN	L:S:6500 MTL:7500 MTL		7	500.0000	(200)	10 MTL SPACING	33.00 MHz	12				
	RAM_DQM_B<4>	L:S:1404 MTL:1686 MTL	7	500.0000	(200)					167.0 MHz														
GROUP 5	MEM_DATA<47..40>	L:S:1719:1893	7	500	(200)					167 MHZ		M10 & OSC	ATI_CLK27M_OSC	L:S:400 MTL			(200)	10 MTL SPACING		19				
	MEM_DQM<5>	L:S:1719 MTL:1893 MTL	7	500.0000	(200)					167.0 MHz		ATI_CLK27M_OSC_SS	L:S:400 MTL				(200)	10 MTL SPACING		19				
	MEM_DQS<5>	L:S:1719 MTL:1893 MTL	7	500.0000	(200)					167.0 MHz		ATI_CLK27M_IN	L:S:1200 MTL				(200)	10 MTL SPACING		19				
	RAM_DATA_A<47..40>	L:S:1607:1898	7	500	(200)					167 MHZ		ATI_SSCLK_UP	L:S:200 MTL				(200)	10 MTL SPACING		19				
	RAM_DQM_A<5>	L:S:1607 MTL:1898 MTL	7	500.0000	(200)					167.0 MHz		ATI_SSCLK_IN	L:S:1800 MTL		5	500.0000	(200)	10 MTL SPACING		19				
	RAM_DQS_A<5>	L:S:1607 MTL:1898 MTL	7	500.0000	(200)					167.0 MHz		CRYSTALS	CLK18M_INT_XIN	L:S:1400 MTL:1500 MTL					10 MTL SPACING		14			
	RAM_DATA_B<47..40>	L:S:1716:2102	7	500	(200)					167 MHZ		CLK18M_INT_XOUT	L:S:1250 MTL:1350 MTL					10 MTL SPACING		14				
	RAM_DQM_B<5>	L:S:1716 MTL:2102 MTL	7	500.0000	(200)					167.0 MHz		CLK18M_XTAL_IN	L:S:300 MTL					10 MTL SPACING		14				
GROUP 6	MEM_DATA<55..48>	L:S:2101:2170	7	500	(200)					167 MHZ		SOUND	INT_I2S0_SND_MCLK		6	500.0000	(200)	10 MTL SPACING		14				
	MEM_DQM<6>	L:S:2101 MTL:2170 MTL	7	500.0000	(200)					167.0 MHz		ETHERNET	CLKENET_PHY_RX	L:S:300 MTL				(200)	125.0 MHz		26			
	MEM_DQS<6>	L:S:2101 MTL:2170 MTL	7	500.0000	(200)					167.0 MHz		CLKENET_LINK_RX	L:S:8000 MTL:9000 MTL		6	800.0000	(200)	10 MTL SPACING	125.0 MHz	13				
	RAM_DATA_A<55..48>	L:S:1204:1357	7	500	(200)					167 MHZ		CLKENET_PHY_GBE_REF	L:S:300 MTL					(200)	125.0 MHz		13			
	RAM_DQM_A<6>	L:S:1204 MTL:1357 MTL	7	500.0000	(200)					167.0 MHz		CLKENET_LINK_GBE_REF	L:S:8000 MTL:9000 MTL		6	500.0000	(200)	10 MTL SPACING	125.0 MHz	13				
	RAM_DQS_A<6>	L:S:1204 MTL:1357 MTL	7	500.0000	(200)					167.0 MHz		CLKENET_PHY_TX	L:S:300 MTL					(200)	10 MTL SPACING	125.0 MHz	13			
	RAM_DATA_B<55..48>	L:S:1400:1546	7	500	(200)					167 MHZ		CLKENET_LINK_TX	L:S:8000 MTL:9000 MTL		6	500.0000	(200)	10 MTL SPACING	125.0 MHz	13				
	RAM_DQM_B<6>	L:S:1400 MTL:1546 MTL	7	500.0000	(200)					167.0 MHz		CLKENET_LINK_GTX	L:S:300 MTL					(200)	10 MTL SPACING	125.0 MHz	13			
GROUP 7	MEM_DATA<63..56>	L:S:1903:2000	7	500	(200)					167 MHZ		ETHERNET	CLKENET_PHY_GTX	L:S:8000 MTL:9000 MTL		6	500.0000	(200)	10 MTL SPACING	125.0 MHz	13			

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1

D

C

B

A

D

C

B

A

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
MAXBUS	CPU_BACK_L	L:S:1500 MTL:2700 MTL 7	7		(250)			
MAXBUS	CPU_ADDR<0..31>	L:S:1500:3100	7		(250)		TRUE	83 MHZ
MAXBUS	CPU_ARTRY_L	L:S:1500 MTL:2700 MTL 7	7		(250)			
MAXBUS	CPU_BG_L	L:S:1500 MTL:2700 MTL 7	7		(250)			
MAXBUS	CPU_BR_L	L:S:1500 MTL:2700 MTL 7	7		(250)			
MAXBUS	CPU_CT_L	L:S:1500 MTL:2700 MTL 7	7		(250)			
MAXBUS	CPU_DATA<0..31>	L:S:1100:2700	7		(250)		TRUE	83 MHZ
MAXBUS	CPU_DATA<32..63>	L:S:1100:2700	8		(250)			83 MHZ
MAXBUS	CPU_DBG_L	L:S:1500 MTL:2700 MTL 7	7		(250)			
MAXBUS	CPU_DTI<0..2>	L:S:1500:2950	7		(250)			
MAXBUS	CPU_DRDY_L	L:S:1500 MTL:3200 MTL 7	7		(250)			
MAXBUS	CPU_GBL_L	L:S:1500 MTL:2700 MTL 7	7		(250)			
MAXBUS	CPU_HIT_L	L:S:1500 MTL:2800 MTL 7	7		(250)			
MAXBUS	CPU_OACK_L	L:S:1500 MTL:2700 MTL 7	7		(250)			
MAXBUS	CPU_QREQ_L	L:S:1500 MTL:2700 MTL 7	7		(250)			
MAXBUS	CPU_TA_L	L:S:1500 MTL:2700 MTL 7	7		(250)			
MAXBUS	CPU_TBST_L	L:S:1500 MTL:2700 MTL 7	7		(250)			
MAXBUS	CPU_TEA_L	L:S:1500 MTL:3000 MTL 7	7		(250)			
MAXBUS	CPU_TS_L	L:S:1500 MTL:2700 MTL 7	7		(250)			
MAXBUS	CPU_TSIZ<0..2>	L:S:1500:3500	7		(250)			
MAXBUS	CPU_TT<0..4>	L:S:1500:3400	7		(250)			
MAXBUS	CPU_WT_L	L:S:1500 MTL:3100 MTL 7	7		(250)			

PRIORITY: 4
 PRIMARY LAYERS: 9
 SECONDARY LAYERS: 4,7
 GOAL: MINIMIZE TH VIAS

STUB_LENGTH OF 250 MILS NEEDED WHEN DESIGN SWITCHED TO 14.2

Temporary Area for TMDS/DVO signal constraints

ALL TMDS GROUP SIGNALS ROUTE AT LAYER 4 OR 7 AND HAVE SAME WIDTH SPACING RULE AS OTHER TMDS SIGNALS

GPU_TMDS_CLKN	GPU_CLKTMDS	GPUTMDS:G:L:S:0 MTL:50 MTL	500.0000	100 OHM SPACING	5	19 20
GPU_TMDS_CLKP	GPU_CLKTMDS	GPUTMDS:G:L:S:0 MTL:50 MTL	500.0000	100 OHM SPACING	5	19 20
GPU_TMDS_DN<0>	GPU_TMDS_D0	GPUTMDS:G:L:S:0 MTL:50 MTL	500.0000	100 OHM SPACING	8	19 20
GPU_TMDS_DP<0>	GPU_TMDS_D0	GPUTMDS:G:L:S:0 MTL:50 MTL	500.0000	100 OHM SPACING	8	19 20
GPU_TMDS_DN<1>	GPU_TMDS_D1	GPUTMDS:G:L:S:0 MTL:50 MTL	500.0000	100 OHM SPACING	8	19 20
GPU_TMDS_DP<1>	GPU_TMDS_D1	GPUTMDS:G:L:S:0 MTL:50 MTL	500.0000	100 OHM SPACING	8	19 20
GPU_TMDS_DN<2>	GPU_TMDS_D2	GPUTMDS:G:L:S:0 MTL:50 MTL	500.0000	100 OHM SPACING	8	19 20
GPU_TMDS_DP<2>	GPU_TMDS_D2	GPUTMDS:G:L:S:0 MTL:50 MTL	500.0000	100 OHM SPACING	8	19 20
SI_TMDS_CLKN	SI_CLKTMDS	SITMDS:G:L:S:0 MTL:50 MTL		100 OHM SPACING	5	19
SI_TMDS_CLKP	SI_CLKTMDS	SITMDS:G:L:S:0 MTL:50 MTL		100 OHM SPACING	5	19
SI_TMDS_DN<0>	SI_TMDS_D0	SITMDS:G:L:S:0 MTL:50 MTL		100 OHM SPACING	8	19
SI_TMDS_DP<0>	SI_TMDS_D0	SITMDS:G:L:S:0 MTL:50 MTL		100 OHM SPACING	8	19
SI_TMDS_DN<1>	SI_TMDS_D1	SITMDS:G:L:S:0 MTL:50 MTL		100 OHM SPACING	8	19
SI_TMDS_DP<1>	SI_TMDS_D1	SITMDS:G:L:S:0 MTL:50 MTL		100 OHM SPACING	8	19
SI_TMDS_DN<2>	SI_TMDS_D2	SITMDS:G:L:S:0 MTL:50 MTL		100 OHM SPACING	8	19
SI_TMDS_DP<2>	SI_TMDS_D2	SITMDS:G:L:S:0 MTL:50 MTL		100 OHM SPACING	8	19

ALL THE DVOD GROUP SIGNALS ROUTE AT LAYER 4 OR 7 AND ROUTE AS STANDARD 50OHM SIGNALS AT 4 MILS

ATI_DVOD<11..0>	ATTIDVOD:G:L:S:0 MTL:50 MTL	6	610			19 20
ATI_DVOD_DE	ATTIDVOD:G:L:S:0 MTL:50 MTL	6	610.0000			19 20
ATI_DVO_HSYNC	ATTIDVOD:G:L:S:0 MTL:50 MTL	6	610.0000			19 20
ATI_DVO_VSYNC	ATTIDVOD:G:L:S:0 MTL:50 MTL	6	610.0000			19 20
ATI_DVO_CLKP	ATTIDVOD:G:L:S:0 MTL:50 MTL	6	610.0000	165.0 MHz:::		19 20
GPU_DVOD<11..0>	GPUDVOD:G:L:S:0 MTL:50 MTL	6	700			19
GPU_DVOD_DE	GPUDVOD:G:L:S:0 MTL:50 MTL	6	500.0000			19
GPU_DVO_HSYNC	GPUDVOD:G:L:S:0 MTL:50 MTL	6	500.0000			19
GPU_DVO_VSYNC	GPUDVOD:G:L:S:0 MTL:50 MTL	6	500.0000			19
GPU_DVO_CLKP	GPUDVOD:G:L:S:0 MTL:50 MTL	6	500.0000	165.0 MHz:::		19
TMDS_CONN_CLKN	CLKCONN_TMDS	TMDS_CONN:G:L:S:0 MTL:50 MTL	500.0000	100 OHM SPACING	4	22 29
TMDS_CONN_CLKP	CLKCONN_TMDS	TMDS_CONN:G:L:S:0 MTL:50 MTL	500.0000	100 OHM SPACING	4	22 29
TMDS_CONN_DN<0>	CONN_TMDS_D0	TMDS_CONN:G:L:S:0 MTL:50 MTL	500.0000	100 OHM SPACING	4	22
TMDS_CONN_DP<0>	CONN_TMDS_D0	TMDS_CONN:G:L:S:0 MTL:50 MTL	500.0000	100 OHM SPACING	4	22
TMDS_CONN_DN<1>	CONN_TMDS_D1	TMDS_CONN:G:L:S:0 MTL:50 MTL	500.0000	100 OHM SPACING	4	22
TMDS_CONN_DP<1>	CONN_TMDS_D1	TMDS_CONN:G:L:S:0 MTL:50 MTL	500.0000	100 OHM SPACING	4	22
TMDS_CONN_DN<2>	CONN_TMDS_D2	TMDS_CONN:G:L:S:0 MTL:50 MTL	500.0000	100 OHM SPACING	4	22
TMDS_CONN_DP<2>	CONN_TMDS_D2	TMDS_CONN:G:L:S:0 MTL:50 MTL	500.0000	100 OHM SPACING	4	22

SIGNAL CONSTRAINTS - PAGE 1

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APPLE COMPUTER INC.	SCALE	DRAWING NUMBER	REV.
	NONE	D 051-6888	B
SHT		36 OF 40	

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Digital Signals (cont'd)

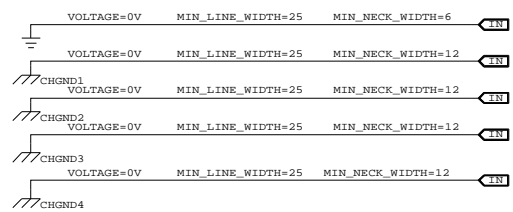
Differential Signals

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
AGP	AGP AD<15..0>	L:S:1050:1450	7					56 MHZ	
	AGP CBE<1..0>	L:S:1050:1450	7					56 MHZ	
	AGP AD_STB<0>	L:S:1050 MTL:1450 MTK			(250)	8 MTL SPACING		133.0 MHZ	
	AGP AD_STB<1>	L:S:1050 MTL:1450 MTK			(250)	8 MTL SPACING		133.0 MHZ	
	AGP AD_STB<2>	L:S:1050 MTL:1450 MTK			(250)	8 MTL SPACING		133.0 MHZ	
	AGP AD_STB<3>	L:S:1050 MTL:1450 MTK			(250)	8 MTL SPACING		133.0 MHZ	
	AGP AD_STB<4>	L:S:1050 MTL:1450 MTK			(250)	8 MTL SPACING		133.0 MHZ	
	AGP AD_STB<5>	L:S:1050 MTL:1450 MTK			(250)	8 MTL SPACING		133.0 MHZ	
	AGP AD_STB<6>	L:S:1050 MTL:1450 MTK			(250)	8 MTL SPACING		133.0 MHZ	
	AGP AD_STB<7>	L:S:1050 MTL:1450 MTK			(250)	8 MTL SPACING		133.0 MHZ	
	AGP AD_STB<8>	L:S:1050 MTL:1450 MTK			(250)	8 MTL SPACING		133.0 MHZ	
	AGP AD_STB<9>	L:S:1050 MTL:1450 MTK			(250)	8 MTL SPACING		133.0 MHZ	
	AGP AD_STB<10>	L:S:1050 MTL:1450 MTK			(250)	8 MTL SPACING		133.0 MHZ	
	AGP AD_STB<11>	L:S:1050 MTL:1450 MTK			(250)	8 MTL SPACING		133.0 MHZ	
	AGP AD_STB<12>	L:S:1050 MTL:1450 MTK			(250)	8 MTL SPACING		133.0 MHZ	
PCI	PCI AD<31..0>	L:S:6000:12500				MIN DAISY CHAIN		33 MHZ	
	PCI CBE<3..0>	L:S:6000:12500				MIN DAISY CHAIN		33 MHZ	
	PCI FRAME L	L:S:6000 MTL:12500 MTL				MIN DAISY CHAIN		33.00 MHZ	
	PCI TRDY L	L:S:6000 MTL:12500 MTL				MIN DAISY CHAIN		33.00 MHZ	
	PCI DEVSSEL L	L:S:6000 MTL:12500 MTL				MIN DAISY CHAIN		33.00 MHZ	
	PCI STOP L	L:S:6000 MTL:12500 MTL				MIN DAISY CHAIN		33.00 MHZ	
	PCI PAR	L:S:6000 MTL:12500 MTL				MIN DAISY CHAIN		33.00 MHZ	
	ULTRA ATA-100	UIDE DATA<15..8>	L:S:1:710			(200)			100 MHZ
		UIDE DATA<7>	H:S:1:RP19 3:..600 MTL			(200)			100 MHZ
		UIDE DATA<6..0>	L:S:1:600			(200)			100 MHZ
		UIDE ADDR<2..0>	L:S:1:650			(200)	NEED TO MATCH DELAY TO 250		100 MHZ
		UIDE RST L	L:S:1:400 MTL			(200)			100.0 MHZ
		UIDE DIOW L	L:S:1:400 MTL			(200)			100.0 MHZ
		UIDE DIOR L	L:S:1:600 MTL		10 MTL SPACING	(200)			100.0 MHZ
		UIDE DMACK L	L:S:1:400 MTL			(200)			100.0 MHZ
UIDE CS0 L		L:S:1:500 MTL			(200)			100.0 MHZ	
UIDE CS1 L		L:S:1:500 MTL			(200)			100.0 MHZ	
UIDE DMARQ		L:S:1:400 MTL			(200)			100.0 MHZ	
UIDE IOCHRDY		L:S:1:600 MTL		10 MTL SPACING	(200)			100.0 MHZ	
UIDE INTRO		L:S:1:400 MTL			(200)			100.0 MHZ	
HD DATA<15..0>		L:S:5000:6500	7		(200)			100 MHZ	
HD ADDR<2..0>		L:S:5000:6500	7		(200)			100 MHZ	
HD RESET L	L:S:4000 MTL:6000 MTL			(200)	TOTAL UIDE+HD SKEW <500MIL		100.0 MHZ		
HD DIOW L	L:S:3000 MTL:5200 MTL			(200)			100.0 MHZ		
HD DIOR L	L:S:6100 MTL:6150 MTL		10 MTL SPACING	(200)			100.0 MHZ		
HD DMACK L	L:S:4500 MTL:6000 MTL			(200)			100.0 MHZ		
HD CS0 L	L:S:3000 MTL:6000 MTL			(200)			100.0 MHZ		
HD CS1 L	L:S:3000 MTL:6000 MTL			(200)			100.0 MHZ		
HD DMARQ	L:S:4500 MTL:6000 MTL			(200)			100.0 MHZ		
HD IOCHRDY	L:S:6200 MTL:6300 MTL		10 MTL SPACING	(200)			100.0 MHZ		
HD INTRO	L:S:3000 MTL:5000 MTL			(200)			100.0 MHZ		
EIDE INTREPID	EIDE DATA<15..0>	L:S:1:850						33 MHZ	
	EIDE ADDR<2..0>	L:S:1:850						33 MHZ	
	EIDE CS0 L	L:S:1:850 MTL						33.00 MHZ	
	EIDE CS1 L	L:S:1:850 MTL						33.00 MHZ	
	EIDE RD L	L:S:1:500 MTL						33.00 MHZ	
	EIDE WR L	L:S:1:500 MTL						33.00 MHZ	
	EIDE IOCHRDY	L:S:1:500 MTL						33.00 MHZ	
	EIDE INT	L:S:1:500 MTL						33.00 MHZ	
	EIDE RST L	L:S:1:500 MTL						33.00 MHZ	
	EIDE DMACK L	L:S:1:500 MTL						33.00 MHZ	
	EIDE DMARQ	L:S:1:500 MTL						33.00 MHZ	
	EIDE OPTICAL DATA<15..0>	L:S:4000:6000						33 MHZ	
	EIDE OPTICAL ADDR<2..0>	L:S:4000:6000						33 MHZ	
	EIDE OPTICAL CS0 L	L:S:4500 MTL:6500 MTL						33.00 MHZ	
	EIDE OPTICAL CS1 L	L:S:4500 MTL:6500 MTL						33.00 MHZ	
EIDE OPTICAL READ L	L:S:4500 MTL:6500 MTL						33.00 MHZ		
EIDE OPTICAL WR L	L:S:4500 MTL:6500 MTL						33.00 MHZ		
EIDE OPTICAL IOCHRDY	L:S:4500 MTL:6500 MTL						33.00 MHZ		
EIDE OPTICAL INT	L:S:5000 MTL:7000 MTL						33.00 MHZ		
EIDE OPTICAL RST L	L:S:4500 MTL:6500 MTL						33.00 MHZ		
EIDE OPTICAL DMAACK L	L:S:4500 MTL:6500 MTL						33.00 MHZ		
EIDE OPTICAL DMA RQ	L:S:4500 MTL:6500 MTL						33.00 MHZ		
ETHERNET MII	ENET LINK RXD<7..0>	L:S:8000:9000	7	(400)				13.26	
	ENET RX DV	L:S:8000 MTL:9000 MTL						13.26	
	ENET RX ER	L:S:8000 MTL:9000 MTL						13.26	
	ENET PHY TXD<7..0>	L:S:8000:9000	7	(400)				13.26	
	ENET LINK TXD<7..0>	L:S:1:600						13	
	ENET PHY TX ER	L:S:8000 MTL:9000 MTL						13.26	
	ENET LINK TX ER	L:S:1:400 MTL						13	
	ENET PHY TX EN	L:S:8000 MTL:9000 MTL						13.26	
	ENET LINK TX EN	L:S:1:400 MTL						13	
	ENET MDIO	L:S:8000 MTL:9000 MTL						13.26	
	ENET MDC	L:S:8000 MTL:9000 MTL						13.26	
	ENET COL	L:S:8000 MTL:9000 MTL						13.26	
	ENET CRS	L:S:8000 MTL:9000 MTL						13.26	
	FW LINK DATA<7..0>	L:S:1:700:3500	7	(400)				13.27	
	FW PHY DATA<7..0>	L:S:1:4700:5500	7	(400)				13.27	
FW LINK CNTL<1..0>	L:S:1:9000:10000						13.27		
FW PHY CNTL<1..0>	L:S:1:100						13.27		
FW LINK LREQ	L:S:1:100 MTL						13		
FW PHY LREQ	L:S:1:8500 MTL:9500 MTL						13.27		
FW PINT	L:S:1:8500 MTL:9500 MTL						13.27		

GROUP	SIG_NAME	DIFFERENTIAL_PAIR	RELATIVE_PROPAGATION_DELAY	MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS
FIREWIRE Zo = 110	FW TP10P	FW TP10	FW_TP10:G:L:S:0 MTL:5 MTL	500.0000	110 OHM SPACING	27.28 39
	FW TP10P	FW TP10	FW_TP10:G:L:S:0 MTL:5 MTL	500.0000	110 OHM SPACING	27.28 39
	FW TP00P	FW TP00	FW_TP00:G:L:S:0 MTL:5 MTL	500.0000	110 OHM SPACING	27.28 39
	FW TP00P	FW TP00	FW_TP00:G:L:S:0 MTL:5 MTL	500.0000	110 OHM SPACING	27.28 39
	FW TP10P	FW TP10	FW_TP10:G:L:S:0 MTL:5 MTL	500.0000	110 OHM SPACING	27.28 39
	FW TP10P	FW TP10	FW_TP10:G:L:S:0 MTL:5 MTL	500.0000	110 OHM SPACING	27.28 39
	FW TP00P	FW TP00	FW_TP00:G:L:S:0 MTL:5 MTL	500.0000	110 OHM SPACING	27.28 39
	FW TP00P	FW TP00	FW_TP00:G:L:S:0 MTL:5 MTL	500.0000	110 OHM SPACING	27.28 39
	FW TP10P	FW TP10	FW_TP10:G:L:S:0 MTL:5 MTL	500.0000	110 OHM SPACING	27.28 39
	FW TP10P	FW TP10	FW_TP10:G:L:S:0 MTL:5 MTL	500.0000	110 OHM SPACING	27.28 39
	FW TP00P	FW TP00	FW_TP00:G:L:S:0 MTL:5 MTL	500.0000	110 OHM SPACING	27.28 39
	FW TP00P	FW TP00	FW_TP00:G:L:S:0 MTL:5 MTL	500.0000	110 OHM SPACING	27.28 39
	FW TP10P	FW TP10	FW_TP10:G:L:S:0 MTL:5 MTL	500.0000	110 OHM SPACING	27.28 39
	FW TP10P	FW TP10	FW_TP10:G:L:S:0 MTL:5 MTL	500.0000	110 OHM SPACING	27.28 39
	FW TP00P	FW TP00	FW_TP00:G:L:S:0 MTL:5 MTL	500.0000	110 OHM SPACING	27.28 39
ETHERNET Zo = 100	MDI P<0>	ENET MDI0	ENET MDI0:G:U43 29:J23 1:0 MTL:100 MTL		ENET 10 MTL SPACING	26.39
	MDI P<0>	ENET MDI0	ENET MDI0:G:U43 31:J23 2:0 MTL:100 MTL		ENET 10 MTL SPACING	26.39
	MDI P<1>	ENET MDI1	ENET MDI1:G:U43 33:J23 3:0 MTL:100 MTL		ENET 10 MTL SPACING	26.39
	MDI P<1>	ENET MDI1	ENET MDI1:G:U43 34:J23 4:0 MTL:100 MTL		ENET 10 MTL SPACING	26.39
	MDI P<2>	ENET MDI2	ENET MDI2:G:U43 39:J23 7:0 MTL:100 MTL		ENET 10 MTL SPACING	26.39
	MDI P<2>	ENET MDI2	ENET MDI2:G:U43 41:J23 8:0 MTL:100 MTL		ENET 10 MTL SPACING	26.39
	MDI P<3>	ENET MDI3	ENET MDI3:G:U43 42:J23 9:0 MTL:100 MTL		ENET 10 MTL SPACING	26.39
	MDI P<3>	ENET MDI3	ENET MDI3:G:U43 43:J23 10:0 MTL:100 MTL		ENET 10 MTL SPACING	26.39
	MDI M<2>	ENET MDI2	ENET MDI2:G:U43 39:J23 7:0 MTL:100 MTL		ENET 10 MTL SPACING	26.39
	MDI M<2>	ENET MDI2	ENET MDI2:G:U43 41:J23 8:0 MTL:100 MTL		ENET 10 MTL SPACING	26.39
	MDI M<3>	ENET MDI3	ENET MDI3:G:U43 42:J23 9:0 MTL:100 MTL		ENET 10 MTL SPACING	26.39
	MDI M<3>	ENET MDI3	ENET MDI3:G:U43 43:J23 10:0 MTL:100 MTL		ENET 10 MTL SPACING	26.39
	CLKLVDS LN	CLKLVDS L	LVDS:G:L:S:0 MTL:110 MTL	500.0000	100 OHM SPACING	20.22 39
	CLKLVDS LP	CLKLVDS L	LVDS:G:L:S:0 MTL:110 MTL	500.0000	100 OHM SPACING	20.22 39
	LVDS L0N	LVDS L0	LVDS:G:L:S:0 MTL:110 MTL	500.0000	100 OHM SPACING	20.22 39
LVDS L0P	LVDS L0	LVDS:G:L:S:0 MTL:110 MTL	500.0000	100 OHM SPACING	20.22 39	
LVDS L1N	LVDS L1	LVDS:G:L:S:0 MTL:110 MTL	500.0000	100 OHM SPACING	20.22 39	
LVDS L1P	LVDS L1	LVDS:G:L:S:0 MTL:110 MTL	500.0000	100 OHM SPACING	20.22 39	
LVDS L2N	LVDS L2	LVDS:G:L:S:0 MTL:110 MTL	500.0000	100 OHM SPACING	20.22 39	
LVDS L2P	LVDS L2	LVDS:G:L:S:0 MTL:110 MTL	500.0000	100 OHM SPACING	20.22 39	
CLKLVDS UN	CLKLVDS U	LVDS:G:L:S:0 MTL:110 MTL	500.0000	100 OHM SPACING	20.22 39	
CLKLVDS UP	CLKLVDS U	LVDS:G:L:S:0 MTL:110 MTL	500.0000	100 OHM SPACING	20.22 39	
LVDS U0N	LVDS U0	LVDS:G:L:S:0 MTL:110 MTL	500.0000	100 OHM SPACING	20.22 39	
LVDS U0P	LVDS U0	LVDS:G:L:S:0 MTL:110 MTL	500.0000	100 OHM SPACING	20.22 39	
LVDS U1N	LVDS U1	LVDS:G:L:S:0 MTL:110 MTL	500.0000	100 OHM SPACING	20.22 39	
LVDS U1P	LVDS U1	LVDS:G:L:S:0 MTL:110 MTL	500.0000	100 OHM SPACING	20.22 39	
LVDS U2N	LVDS U2	LVDS:G:L:S:0 MTL:110 MTL	500.0000	100 OHM SPACING	20.22 39	
LVDS U2P	LVDS U2	LVDS:G:L:S:0 MTL:110 MTL	500.0000	100 OHM SPACING	20.22 39	
TMDS Zo = 100	TMDS CLKN	CLKTMDS	TMDS:G:L:S:0 MTL:50 MTL	500.0000	100 OHM SPACING	19.22
	TMDS CLKP	CLKTMDS	TMDS:G:L:S:0 MTL:50 MTL	500.0000	100 OHM SPACING	19.22
	TMDS DN<0>	TMDS D0	TMDS:G:L:S:0 MTL:50 MTL	500.0000	100 OHM SPACING	19.22 39
	TMDS DP<0>	TMDS D0	TMDS:G:L:S:0 MTL:50 MTL	500.0000	100 OHM SPACING	19.22 39
	TMDS DN<1>	TMDS D1	TMDS:G:L:S:0 MTL:50 MTL	500.0000	100 OHM SPACING	19.22 39
	TMDS DP<1>	TMDS D1	TMDS:G:L:S:0 MTL:50 MTL	500.0000	100 OHM SPACING	19.22 39
	TMDS DN<2>	TMDS D2	TMDS:G:L:S:0 MTL:50 MTL	500.0000	100 OHM SPACING	19.22 39
	TMDS DP<2>	TMDS D2	TMDS:G:L:S:0 MTL:50 MTL	500.0000	100 OHM SPACING	19.22 39
	ATI TMDS CLKN	ATI CLKTMDS	ATI TMDS:G:L:S:0 MTL:50 MTL	200.0000	100 OHM SPACING	5
	ATI TMDS CLKP	ATI CLKTMDS	ATI TMDS:G:L:S:0 MTL:50 MTL	200.0000	100 OHM SPACING	5
	ATI TMDS DN<0>	ATI TMDS D0	ATI TMDS:G:L:S:0 MTL:50 MTL	200.0000	100 OHM SPACING	8

POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
MAIN/SLEEP	+24V PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+BATT	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+5V MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+5V SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	
	+3V PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+2.5V MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+2.5V SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1.8V MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	
	+1.8V SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1.5V MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1.5V SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1.5V LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
+1.5V SLEEP VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10		
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	1772 DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
	1772 LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+BATT_14V FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+BATT_24V FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+BATT_ESNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
	1772 LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
	1772 DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
PMU	1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
	+4.85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
	+4.6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
	+4.85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
	MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
		+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
TRACKPAD	+5V_TPAD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
VIDEO	+14V_INV	VOLTAGE=14V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+5V_INV_UP_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	
	+5V_DDC_SLEEP_UP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10		
AUDIO	+5V_MAIN_AUD	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V_MAIN_AUD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	AUD_GND	VOLTAGE=0V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	
FAN	+FAN_PWR	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	FAN1_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	FAN2_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	



GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	CPU_AVDD	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
DDR RAM	DDR_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10
	INTREPID			
PLL5	+2.5V_INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+3V_INTREPID_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+1.5V_INTREPID_PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10
	+1.5V_INTREPID_PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6
	+1.5V_INTREPID_PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6
	+1.5V_INTREPID_PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6
	+1.5V_INTREPID_PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6
	+1.5V_INTREPID_PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6
	+1.5V_INTREPID_PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6
	+1.5V_INTREPID_PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6
REFERENCE	INT_MEM_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10
	INT_AGP_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10
	INT_MEM_REF_H	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10
AIRPORT	WIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10
	+3V_AIRPORT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
CARDBUS	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	ATI M10			
GPU	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10
	+3V_GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+3V_GPU_FLT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+2.5V_GPU	VOLTAGE=2.5V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10
	GPU_MEM_I0	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	GPU_MEM_I0_FLT	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+2.5V_GPU_MEMCORE	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+1.8V_GPU	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+1.5V_AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+2.5V_GPU_PNLIO	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	+1.8V_ATI_PVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	+1.5V_AGP_GPU	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	+1.5V_GPU_VDDI5	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	+1.8V_GPU_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10
	+1.8V_GPU_VDDI5	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10
	GPU_VCORE_VDDCI	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10
	+2.5V_GPU_A2VDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10
	+1.8V_GPU_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10
	+1.8V_GPU_PNLIO	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10
	+1.8V_GPU_PNLIO	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10
+2.5V_GPU_MCLK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
+1.8V_GPU_AVDDO	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
+1.8V_GPU_MEMPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
+3V_ATI_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
+3V_ATI_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
+GPU_VDDI5_UP	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
+2.5V_SLEEP_NECK1	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
+3V_SLEEP_NECK	VOLTAGE=3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
+1.5V_AGP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
+1.8V_PVDD_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
GPU_VCORE_NECK	VOLTAGE=1.2V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
+GPU_VDDI5_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
+2.5V_SLEEP_NECK2	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
+1.8V_SLEEP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
+1.5V_SLEEP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
+1.8V_ATI_TPVD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
+1.8V_GPU_TP_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	
ETHERNET	+2.5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+2.5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+1.0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10
	LM2594_IN	VOLTAGE=3.3V	MIN_LINE_WIDTH=40	MIN_NECK_WIDTH=12
	+FW_PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12
	+FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12
	+FW_AMP_SENSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12
+FW_PWR_OR	VOLTAGE=3.3V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	
+FW_PWR1	VOLTAGE=3.3V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	
+FW_VP0	VOLTAGE=3.3V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	
+FW_VP1	VOLTAGE=3.3V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	
+3V_FW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
+3V_FW_UP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
+1.95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
+1.95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
+1.95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
+1.95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
+1.95V_FW_PLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
+1.95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
+1.95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	
FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	
FW_VDD_ON	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10
	1625_VSW	VOLTAGE=14V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+PBUS_JUMPER	VOLTAGE=14V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10
	LV20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10
	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10
	5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
LTC3707 5V SWITCHER	+5V_MAIN_JUMPER	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+3V_MAIN_JUMPER	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10
	2.5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10
	2.5V_LX_F	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10
	2.5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10
	2.5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10
	2.5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
3V SWITCHER	2.5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	1.5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10
	1.5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10
	1.5V_LX_F	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10
	1.5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10
	1.5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10
	1.5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	1.5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	1.5V_ILIM		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10
	2.5V_ILIM		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10
MAX1715 2.5V SWITCHER	MAX1715_TON		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10
	MAX1715_SKIP		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10
	MAX1715_REF	VOLTAGE=2.0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10
	MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10
	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=200	MIN_NECK_WIDTH=10
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10
MAX1717	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10
	VCORE_ILIM	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10
	VCORE_REF		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10
	VCORE_CC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10
	VCORE_TIME		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10
	VCORE_VGATE		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10
LTC1778	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=10
	VCORE_GNDA	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10
	1778_VIN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	1778_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	1778_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10
	1778_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10
	1778_BST_RC	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10
	1778_TG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10

FUNCTIONAL TEST POINTS

PROBES ARE ON BOTTOM SIDE. MINIMUM PAD/HOLE SIZE IS 25 MIL.
 FUNC_TEST IS ONLY PROPERTY USED BY THE TOOLS. FUNC_QTY IS FOR REFERENCE AND
 LISTS THE NUMBER OF TEST POINTS ON THAT NET AND WITHIN THAT GROUP/CONNECTOR.
 FUNC_DIST IS SIMILARLY USED TO DEFINE MAXIMUM DISTANCE FROM A CONNECTOR.

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
SCAN/TEST	JTAG ASIC TMS	TRUE		13 26	
	JTAG ASIC TDI	TRUE		13	
	JTAG ASIC TDO TP	TRUE		26	
	JTAG ASIC TCK	TRUE		13 26	
	JTAG ASIC TRST L	TRUE		13 26	
	CPU CHKSTP_OUT_L	TRUE		5	
	CPU SRESET_L	TRUE		5	
	CPU HRESET_L	TRUE		5 4 7	
	JTAG CPU TMS	TRUE		5 4	
	JTAG CPU TDI	TRUE		5 4	
	JTAG CPU TDO TP	TRUE		5	
	JTAG CPU TCK	TRUE		5 4	
	JTAG CPU TRST L	TRUE		5 4	
	INT_JTAG_TEL	TRUE		13	
	INT_TST_MONIN_PD	TRUE		13	
	INT_TST_MONOUT_TP	TRUE		13	
	INT_TST_PLKEN_PD	TRUE		13	
	INT_I2C_CLK0	TRUE		6 11 13 23	
	INT_I2C_DATA0	TRUE		6 11 13 23	
	INT_I2C_CLK1	TRUE		13 14 25	
INT_I2C_DATA1	TRUE		13 14 25		
PWR/GND	+PBUS	TRUE		38	
	+24V_PBUS	TRUE		38	
	GPU_VCORE	TRUE		19 20 38	
	1778_VFB	TRUE		20 38	
	CPU_VCORE_SLEEP	TRUE		5 33 38	
	VCORE_FB	TRUE		33 38	
	+1_8V_MAIN	TRUE		38	
	+2_5V_MAIN	TRUE		38	
	+5V_MAIN	TRUE	2	38 39	
	+5V_SLEEP	TRUE	2	38 39	
	+3V_MAIN	TRUE	4	23 38	
	+3V_PMU	TRUE		38	
	CARDBUS	CBUS_DET_1_L	TRUE		2000
		CBUS_DET_2_L	TRUE		2000
		TMDS_DN<0..2>	TRUE		19 22 37
TMDS_DP<0..2>		TRUE		19 22 37	
TMDS_CONN_CLKN		TRUE		1000	
TMDS_CONN_CLKP		TRUE		1000	
VGA_R		TRUE		1000	
VGA_G		TRUE		1000	
VGA_B		TRUE		1000	
VGA_HSYNC		TRUE		1000	
VGA_VSYNC		TRUE		1000	
DVI_DDC_CLK_UP		TRUE		1000	
DVI_DDC_DATA_UP		TRUE		1000	
DVI_HPD_UP		TRUE		1000	
+5V_DDC_SLEEP		TRUE		2000	
LVDS	LVDS_L0N	TRUE		1000	
	LVDS_L0P	TRUE		1000	
	LVDS_L1N	TRUE		1000	
	LVDS_L1P	TRUE		1000	
	LVDS_L2N	TRUE		1000	
	LVDS_L2P	TRUE		1000	
	CLKLVDS_LN	TRUE		1000	
	CLKLVDS_LP	TRUE		1000	
	LVDS_DDC_CLK	TRUE		1000	
	LVDS_DDC_DATA	TRUE		1000	
	+3V_LCD	TRUE	2	2000	
	+3V_SLEEP	TRUE	2	2000	
	+14V_INV	TRUE		2000	
	+5V_INV_SW	TRUE		2000	
	BRIGHT_PWM	TRUE		2000	
INV_GND	TRUE		2000		
S-VIDEO	TV_C	TRUE		2000	
	TV_Y	TRUE		2000	
	TV_COMP	TRUE		2000	
	TV_GND1	TRUE		2000	
	TV_GND2	TRUE		2000	
	INT_I2S0_SND_TO_DAC	TRUE		1000	
	INT_I2S0_SND_LRCLK	TRUE		1000	
	INT_I2S0_SND_MCLK	TRUE		1000	
	INT_I2S0_SND_SCLK	TRUE		1000	
	INT_I2S0_SND_FROM_ADC	TRUE		1000	
	SND_HP_MUTE_L	TRUE		1000	
	SND_HP_MUTE_R	TRUE		1000	
	SND_HW_RESET_L	TRUE		1000	
	SND_HP_SENSE_L	TRUE		1000	
	SND_LIN_SENSE_L	TRUE		1000	
INT_I2C_CLK2	TRUE		1000		
INT_I2C_DATA2	TRUE		1000		
ADAPTER_DET	TRUE		1000		
CHARGE_LED_L	TRUE		1000		
NEC_LUSB_OCI_UF	TRUE		1000		
NEC_LUSB_PPON	TRUE		1000		
+5V_MAIN	TRUE	2	2000		
+5V_SLEEP	TRUE	2	2000		
+3V_SLEEP	TRUE		2000		

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST
USB	NEC_USB_DAM	TRUE		17 25 37
	NEC_USB_DAP	TRUE		17 25 37
	NEC_USB_DBM	TRUE		17 25 37
	NEC_USB_DBP	TRUE		17 25 37
	BT_USB_DM	TRUE		14 25 37
	BT_USB_DP	TRUE		14 25 37
	MODEM_USB_DM	TRUE		14 25 37
	MODEM_USB_DP	TRUE		14 25 37
	NEC_RUSB_PPON	TRUE		17 25
	NEC_RUSB_OCI_UF	TRUE		17 25
	PCI_AD<0..31>	TRUE	1000	9 12 17 18 24 37
	PCI_FRAME_L	TRUE	1000	12 17 18 24 37
	PCI_TREQ_L	TRUE	1000	12 17 18 24 37
	PCI_IRDY_L	TRUE	1000	12 17 18 24 37
	PCI_DEVSEL_L	TRUE	1000	12 17 18 24 37
RT. USB WIRELESS	PCI_STOP_L	TRUE	1000	12 17 18 24 37
	PCI_PAR	TRUE	1000	12 17 18 24 37
	AIRPORT_PCI_REQ_L	TRUE	1000	12 24
	AIRPORT_PCI_GNT_L	TRUE	1000	12 24
	AIRPORT_PCI_INT_L	TRUE	1000	12 24
	MAIN_RESET_L	TRUE	1000	14 17 18 19 24 29
	CLK33M_AIRPORT	TRUE	1000	12 24 35
	PMU_PME_L	TRUE	1000	14 17 24 29
	ROM_ONBOARD_CS_L	TRUE	1000	9 24
	ROM_OE_L	TRUE	1000	9 12 24
	ROM_CS_L	TRUE	1000	9 12 24
	ROM_RW_L	TRUE	1000	9 12 24
	RF_DISABLE_L	TRUE	1000	24
	AIRPORT_CLKRUN_L	TRUE	1000	24
	+3V_AIRPORT	TRUE	2000	38
OPTICAL	EIDE_OPTICAL_DATA<0..15>	TRUE		2000
	EIDE_OPTICAL_DMA_HQ	TRUE		2000
	EIDE_OPTICAL_READ_L	TRUE		2000
	EIDE_OPTICAL_DMAACK_L	TRUE		2000
	EIDE_OPTICAL_ADDR<0..2>	TRUE		2000
	EIDE_OPTICAL_CS0_L	TRUE		2000
	EIDE_OPTICAL_CS1_L	TRUE		2000
	EIDE_OPTICAL_RST_L	TRUE		2000
	EIDE_OPTICAL_WR_L	TRUE		2000
	EIDE_OPTICAL_IOCHRDY	TRUE		2000
	EIDE_OPTICAL_INT	TRUE		2000
	+5V_TPAD_SLEEP	TRUE		3000
	TPAD_F_TXD	TRUE		3000
	TPAD_F_RXD	TRUE		3000
	LID_CLOSED_L	TRUE		3000
+3V_HALL_EFFECT	TRUE		3000	
SOFT_PWR_ON_L	TRUE		3000	
COMM_RESET_L	TRUE		4000	
COMM_SHUTDOWN	TRUE		4000	
COMM_RING_DET_L	TRUE		4000	
COMM_TXD_L	TRUE		4000	
COMM_TRXC	TRUE		4000	
COMM_GPIO_L	TRUE		4000	
COMM_DTR_L	TRUE		4000	
COMM_RTS_L	TRUE		4000	
COMM_RXD	TRUE		4000	
KEYBOARD	KBD_ID	TRUE		3000
	KBD_INTL	TRUE		3000
	KBD_JIS	TRUE		3000
	KBD_CAPSLOCK_LED	TRUE		3000
	KBD_NUMLOCK_LED	TRUE		3000
	KBD_FUNCTION_L	TRUE		3000
	KBD_COMMAND_L	TRUE		3000
	KBD_OPTION_L	TRUE		3000
	KBD_CONTROL_L	TRUE		3000
	KBD_SHIFT_L	TRUE		3000
	KBD_X<0..9>	TRUE		3000
	KBD_Y<0..7>	TRUE		3000
	+BATT_POS	TRUE	(100 MIL PROBE PREFERRED)	1000
	BATT_NEG	TRUE	(100 MIL PROBE PREFERRED)	1000
	BATT_CLK	TRUE		1000
BATT_DATA	TRUE		1000	
PMU_BATT_DET_L	TRUE		1000	
FANS	+FAN_PWR	TRUE		3000
	FAN1_TACH	TRUE		3000
	FAN2_TACH	TRUE		3000
	FAN1_GND	TRUE		3000
	FAN2_GND	TRUE		3000
ETHERNET	MDI_P<0..3>	TRUE		1000
	MDI_M<0..3>	TRUE		1000
FIREWIRE	FW_TPOOP	TRUE		1000
	FW_TPOGN	TRUE		1000
	FW_TPOOR	TRUE		1000
	FW_TPIOP	TRUE		1000
	FW_TPION	TRUE		1000

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST
FIREWIRE (CONT.)	FW_TPOIP	TRUE		1000
	FW_TPOIN	TRUE		1000
	FW_TPIIP	TRUE		1000
	FW_TPIIN	TRUE		1000
	FW_VGND	TRUE		1000
DC PWR IN	+ADAPTER	TRUE	3 (100 MIL PROBE PREFERRED)	1000
	ST7_SLEEP_LED_H	TRUE		23
LMU/ALS	PMU_SLEEP_LED	TRUE		23
	PMU_LID_CLOSED_L	TRUE		23 29
	LMU_DETECT	TRUE		23
	(100 MIL PROBE PREFERRED)		6	1000
MISC.	SLEEP_LED	TRUE		23
	PMU_KB_RESET_L	TRUE		29
	SLEEP	TRUE		23 25 29 32 34
	PMU_CPU_HRESET_L	TRUE		6 29
	BB_RESET_L	TRUE		6
	+3V_PMU_RESET	TRUE		29 33
	(100 MIL PROBE PREFERRED)			

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APPLE COMPUTER INC. DRAWING NUMBER 051-6888 REV. B
 SCALE NONE SHEET 39 OF 40

REVISION HISTORY

Proto Release

- 7/22/02 - Initial acquisition of schematic (from 051-6278 Rev 01)
Added P59 50-DIMM connector as placeholder (p.12)
Added P59 LVDS connector as placeholder (p.22)
Changed J9 to 10 pin Elco connector for modem (p.25)
Changed PBUS holdup caps to P59 electrolytic cans (p.30)
- 7/23/02 - Removed L3 (p.8)
- 7/24/02 - Replaced CPU Processor with 360 pin Apollo (p.5,6)
- 8/10/02 - Added P58 battery and PBUS rails for airline power (p.29)
Added USB 2.0 (p.18)
- 8/20/02 - Removed spare pullup straps for Intrepid (p.9)
Removed USB overcurrent protection (to be placed on other boards) (p.18)
Changed right USB board connector to 16 pin Hirose connector (p.26)
Changed L10 board connector to 40 pin Molex connector (p.26)
Added 6 bypass caps to MAXBUS_SLEEP and CPU_VCORE_SLEEP (p.5)
- 8/26/02 - Removed 32 bypass caps for +3V MAIN at Intrepid (p.16)
Removed 5 bypass caps for +2.5V MAIN at Intrepid (p.5)
Removed 3 bypass caps for +1.5V_AGP at Intrepid (p.16)
Removed 8 bypass caps for +3V_MAIN at Intrepid (p.16)
- 8/27/02 - Changed main battery connector to BP24067-R1, which is close to final (p.29)
- 8/29/02 - Added dedicated Boot Banger circuit (p.6)
Added 5 bypass caps to each 50-DIMM connector (p.11)
Added quad voltage circuit for bus slewing architecture (p.32)
Changed to low profile 32.768KHz crystal for FMU (p.28)
Changed to Q11 adapter detection scheme (p.28)
- 9/03/02 - Corrected upper LVDS single pin nets (p.20)
Removed unintentional extra pulldown resistor at Intrepid (p.14)
- 9/17/02 - Numerous changes to stay in sync with P84 (all)
- 9/18/02 - Changed battery connector back to P84 part (p.29)
Added LMU circuitry to eliminate extra board (p.23)
Changed to P84 dual channel LVDS connector to reduce I2R cable losses (p.22)
Added L10 adapter detection scheme (p.28)
- 9/19/02 - Removed unnecessary battery ferrite (due to ferrite design) (p.29)
Modified chassis gnds on some components (all)
Removed LMU connector (p.23)
Corrected battery connector [same as P84] (p.29)
Removed P93 support (p.25)
Removed second fuse from FW ports [single fuse provides adequate power] (p.27)
- 9/23/02 - Replaced BCM5421 with Marvell 88E1111 (p.26)
Increased MAX_VIA_COUNT by two on most nets with this constraint for uVia (p.34,35)
- 9/27/02 - Corrected cpu, memory bus constraints to match manhattan lengths (p.34)
Swapped pins on L33, L35 for layout (p.31)
- 9/30/02 - Changed J19 (DC-in) to proper 4-pin connector (p.29)
Corrected holes and chassis gnds (p.4,all)
- 10/01/02 - Removed Intrepid 1.x specific circuitry (p.13)
10/03/02 - Numerous pin-swaps to accommodate board layout (all)
10/08/02 - Added page for functional test points (p.37)
10/09/02 - Changed 16 pin connectors (modem and right USB) to Foxconn parts (p.23)
10/10/02 - Changed HPC MC pins high per documentation (p.17)
Added 10K pullup to CG_ADDRESSL and 10K pulldown to CG_FSEL on CY28512 (p.14)
Added SSO/NO_SSO stuffing options for CY28512 circuit (p.14)
Added CPU_VGATE pullup to 5V to eliminate potential 3V/5V current path (p.32)
Removed Zehra 15/16 support per P84 (p.27)
Added second FW port power fuse (p.27)
Removed INT_CPUFB_IN cap per P84 (p.8)
Replaced INT_F812 ferrite with INT_F811 in battery charger and 14V PBUS switchers (p.29,30)
Renamed optical interface for consistency (p.24,37)
Corrected PLL_CFG4 for Apollo 7 [needs to always be zero] (p.5,7)
Removed temporary P84 constraints and finished up AGP clock changes (p.12,34)
Added stuffing options to power fans off 3V or 5V (p.25)
- 10/11/02 - Replaced DVI EMI caps with 0201 versions (p.22)
- 10/14/02 - Changed J18 to R345 with integrated magnetics (p.26)
10/15/02 - Moved FireWire connectors and port power switch to separate page (p.28)
Changed SBus pullups to 7.15K, 1K as per 1Books/P84 [involved component net swaps] (p.29)
Added 0603 resistors as shunting pads for power up and reset (p.43)
Changed INT_MOD_SYNC, INT_MOD_DTT and INT_MOD_BITCLK to pulldowns per ERS [LA clk not used] (p.14)
Added damping resistor option to LMU circuit (p.23)
Changed INT_RST_FLLDN_PD to pulldown only [LA clk not used] (p.13)
Changed INT_ENET_TDR to pullup [LA clk not used] (p.13)
Removed FW_LKON from Intrepid EXTINT3 [no longer used], pullup added (p.14)
Added HSMC pullup to 3V (p.24)
Changed FW_PC_PD, FW_PC_PU resistors to 5K (p.27)
Added 1K pulldown and net FW_PD2 to FW_PHY (p.27)
- 10/16/02 - Implemented new FW power switch and current limit (p.28)
Renamed +14V_PBUS to +PBUS (p.all)
Added A29 adapter detection circuit (p.29)
Added +PBUS current limiting circuit, removed battery charging current limit circuit (p.30)
Changed FW_PBU1 net to make Port 1 1394a only (p.27)
- 10/21/02 - Updated CY28512 clock chip to Rev B (p.14)
Changed FW_PBU1 net to make Port 1 1394a only (p.27)
- 10/22/02 - Added full support for non-zero CPU_PLL_CFG45 in run state (p.7)
10/23/02 - Changed fan ferrite to S14460V per P84 (p.25)
Changed LMU/sleep LED interface per P84 (p.23)
Mirrored wireless connector for P50 flex (p.24)
Pinned out audio connector (p.25)
Pinned out modem connector (p.25)
Pinned out wireless connector (p.24,38)
Renamed FW low voltage power rails (p.27,37)
Renamed VCore VID nets to be consistent with P84 (p.33)
Removed redundancy in DDR memory constraints (p.35)
Changed FW_DDR_A12 to pullup to shut off port (p.27)
Renamed VCore VID nets to be consistent with P84 (p.33)
Cleaned up CY28512B circuit as per P84 [powered off main, output divider and strap tweaks] (p.14)
Updated PCI clock series B values per P84 (p.23)
Added 0 ohm short and bypass cap for CPU_VDDO_VDD per P84 (p.21,37)
Split FW_VDDO into FW_VDDO1 and FW_VDDO2 (p.37)
Added TP nets to GPU for XOR-tree testing (p.19-21)
Changed fan PWM output pullups to +5V_SLEEP (p.25)
Added FW thermal pad ground hole back in (p.27)
- 10/28/02 - Replaced LMU layout (p.23)
10/30/02 - Changed fan power rails to common net (p.25)
10/31/02 - Removed HLA ALS (p.23)
11/05/02 - Added wireless RF_DISABLE_L pullup and AIRPORT_CLKRUN_L pulldown (p.24)
11/06/02 - Added 6 decoupling caps to CPU_VCORE_SLEEP (p.5)
Broke out quad OR gates to discrete components for better placement (p.22,29)
Changed 10 uF FW current limit output cap to two 4.7 uF caps (p.28)
Added 3 decoupling caps to CPU_VCORE_SLEEP (p.5)
Added 9 decoupling caps to each of +5V_MAIN and +3V_MAIN (p.32)
Removed CW17 jumper for CPU_VCORE_SLEEP (p.33)
Added decoupling cap to PMU reset OR gates (p.29)
11/08/02 - Changed FireWire PHY to Z17 (p.27)
Added bulk caps to fan connectors (p.25)
Added alternate chassis gnd connection for sleep LED (p.23)
- 11/11/02 - Added +3V_MAIN option for P50 card (p.24)
- 11/13/02 - Removed LMU and associated circuitry (p.23)
- 11/15/02 - Implemented D3clock for all PCI devices (p.12,14,18)
- 11/25/02 - Renamed all components (all pages)
- 11/26/02 - Removed chokes from 1394a data pairs (p.27,28)

EVT RELEASE

- 12/13/02 - Added 12 pF caps to source of 33MHz PCI clocks since they can not be buried (p.12)
Replaced AWM1031 with AD7460 12C Address Changes (p.25)
Added AD7460 hooks to CPU thermal diode (p.21,25)
12/16/02 - Added FireWire B ESD protection circuits (p.28)
Removed hole from FireWire ground pad (p.27)
- 12/20/02 - DDR memory connector renamed to J25 (p.11)
Added P10_P20 as placeholders and experiment guides (p.28)
Added diodes to OR +5V_SLEEP into FW PHY power supply (p.27)
- 12/26/02 - Updated CPU p/ns to production p/ns (p.5)
Removed PCI latch filter on CPU_DDRY_L (p.5,36)
Updated PCI source clock and internal spreading straps (p.8)
Changed bootROM PWD signal to INT_RESET_L per P84 (p.9)
Added CR3 pulldowns per P84 (p.9)
Updated ethernet series Rs per P84 [Clocks to 10 ohms, data to 22 ohms] (p.13)
Added SSO/NO_SSO BOM options (p.14)
Renamed line-in and headphone sense lines to reflect active low signals (p.14,25,39)
Added 0 ohm Rs to make 2.5V Intrepid rail hot or cold (p.15,16,38)
NO STUFFED entire 1.5V LDO circuit (p.15)
Stuffed USB OCT RC filters for 0 time constant [due to new port current limiters] (p.17)
Added USB OCT/FPON signals for left/right ports (p.17,39)
Updated GPU VCore to stay in sync with P84 "jitter" improvement (p.20)
Added EMI caps to LVDS_DDC_CLK, INT_I2SD_SND_CLK, INT_I2SD_SND_SCLK per P84 (p.22,25)
Added R800_R801 for eventual thermal diode in CPU (p.25)
Renamed R800 to R789, R801 to R802, R802 to R803 (p.25)
Renamed P10 to P1, P20 to P2 [deleted old P1,P2] (p.28)
Added caps to FW EMI circuit that were missed (p.28)
Changed MAX4172 power source to save current on battery [per P84] (p.30)
Updated 1.5V/2.5V switcher BOM to stay in sync with P84 [PFT change and current limits] (p.34)
Replaced all 132S1961 [1uF,0605,10V,208] with 132S0046 [1uF,0603,10V,208] (p.14,15,27,30,33,34)
Replaced all 138S2511 [1uF,0603,6.3V,104] with 132S0046 [1uF,0603,10V,208] (p.27,30)
12/29/02 - Updated FireWire fuse topology to that of P84 (p.28)
Updated system and power block diagrams (p.2,3)
- 01/02/03 - Corrected +2.5V_INTREPID connections to muxes and reference (p.9,10)
- 01/03/03 - Added NO_TEST nets to pads of DDR connector arms (p.11)
- 01/08/03 - Added ZN002 circuits to ensure speakers are muted during power-up (p.25)
Changed R164 to 511 ohms to avoid low CPU clock amplitude (p.8)
Added required pulldown to output of DVI_HPD sense comparator (p.22)
Swapped R443 and R444 values to ensure Vgs < -4.5V (p.28)
Updated 5-video filter values to those of P84 (p.22)
- 01/10/03 - ZT7, ZT23, ZT61, ZT76, ZT89, ZT87, ZT22, ZT38, ZT60, ZT42 & ZT17 are changed to HOLE-VIA-20R10 (p.4)
- 01/13/03 - Add L53, L54, L55 for TMSD Data+0+2+ Diff Pair (p.22)
- 01/14/03 - Add CR12 - CR21 (total 10 0.22uF caps) for 2.5V Intrepid Decoupling (p.16)
Add CR22 & CR23 at Wireless Card connector MAIN_RESET_L & RF_DISABLE_L_SPN (p.24)
Change MATCHED_DELAY to 50 for all TMSD DIFF PAIR (p.37)
Change MATCHED_DELAY to 50 for all TMSD DIFF PAIR (p.37)
Add R810 & R811 for ALWAYS-ON_FANS in Acrylic Build (p.25)
01/28/03 - Add M10 (p.19-21)
02/07/03 - Add Power Net Constraints (p.38)
Replace Singing PBus Cap C49, C50, C67, C68, C80, C81, C95, C96, C108, C109, C120, C121 with 126S0035 (or alt. 126S0036) (p.33)
02/11/03 - Add FW Power Net Constraints (p.38)
Change signal constraints for AGP signals (p.36)
Add LMU connector and components (p.23)
Edit I2C table for LMU (p.13)
Change R880 to 19.6K (p.22)
Connect Clock Slewing RESET# to MAIN_RESET_L (p.14)
Change Ferrite Bead of ATI power supply to correct values (p.21)
Remove C141 PBUS CAP (p.31)
Change and Rotate Keyboard Connector (p.23)
02/12/03 - Add ATI Power sequencing Circuit for M10 Power-up and Power-down (p.19-22, p.32-35)

EVT RELEASE (continue)

- 02/13/03 - Add CR25 (p.30)
- 02/17/03 - Rename all Reference Designators

EVT ENCLOSURE RELEASE

- 03/13/03 - Change 3-P FAN connectors to 4-P (p.25)
Add PU at PMU_SLEEP_LED_L for LMU (p.23)
Change overcurrent protection (to be placed on other boards) (p.18)
Change ATI M10 GPIO8 to Pull-down (p.20)
Remove Memory MUX 0ohm Resistors (p.10)
- 03/28/03 - Due to MLS outline change at DVI connector, CHGND1 has to be splitted into CHGND1 & CHGND2 (P 4 & 22)
Separate +3V and +5V traces running from 3/5V supply to 40pin LIO connector (P 25 & 32)
R011 change from 100K to 4.7K (P 29)
Change airline detect to 13.1V or greater, R40 and R690 to 97.6K ohm (P 30 & 31)
Add CR26 at U3 RS- pin (P 30)
Change D3 to IN914 PN Junction Diode (P 31)
- 03/31/03 - Change AGPTST Pull-up to 470hm (it was 400hm) (p.20)
Add circuits to prevent start-up Headphone POP (p.25)
Change all 1210 4.7uF to 1206 4.7uF Cap (138S0531) (various pages)
Modify FAN circuit to PWM active low signal (P25)
- 04/08/03 - Add SOFT MODEM support (p.14 & 25)
Add 10-pin ELCO connector for Serial Debug Interface (P 25)
Change Q from S144350Y to SUD45P03-10 (P 30)
Remove U34 R32A8 (P 30)
- 04/11/03 - Change FW Schottky Diode to a 3A part 37180159 (P 28)
Change PBUS L69 and VCORE L71 inductor (P 31 & 33)
Issue to 3S coil for 1206 package part (P 28)
Change all 6 VCORE Caps to 220uF Al Poly Cap 128S0024 (P 33)
Add Mitsumi RM1571J regulator to provide 1.8V TFVDD (P 21)
Change U34 to Mitsumi MM1571J part for ATI PLL 1.8V rail (P 21)
- 04/16/03 - Add FW Port Shutdown/PowerOn Circuit (P 28)
Change the I2C Pull-up for Sound/Modem to 1K ohm (P 14)
- 04/17/03 - Change 3V/5V inductors (152S0137) L61 & L62 (P 32)
- 04/21/03 - Add 12 ICT JTAG TEST PADS (P 39)
- 04/23/03 - Invert ATI GPIO15 signal, no stuff pull-up resistor (P 20)
Combine Q35 and Q36 into a Dual Package Part (P 22)
SWAP the 3V/5V Temperature Sense Part (P 22)
Change FW PHY to production part (P 26)
- 04/24/03 - Remove +3V_CBUS_SLEEP and U5, use +3V_SLEEP directly (P 14,18,24)
Add 040P Res between ATI_PVDD/TPVDD rail and 10uF caps for stability purpose (P 21)
Add 040P Res between mode choke at TMSD data (P 21)
Add Sense Resistor to Vcore power rail, remove one 220uF cap <back to EVTA design> (P 33)
- 04/25/03 - Change CR26 to 0.01uF 50V Cap (P 30)
- 04/30/03 - No stuff R676 to prevent +3V rail leakage (P 33)
- 05/02/03 - L45,L46,L47 is using Common Mode Choke TDK ACM2012D Part, will replace with ACM2012H Part if available (P 22)

DVT RELEASE

- 05/21/03 - Swap +PBUS and +24V_PBUS at Backup Battery Connector - J16 (p.31)
- 05/27/03 - Change Q12 to R22 timing specification (p.13)
Change Q62 & Q65 to S17860DP part (p.33)
Change Q63 & Q66 to INT_F812 part and split C102 into 3 10pF caps (p.33)
Enable VCore Burst(Skip) Mode by no stuffing R67 (p.33)
Enable Q48 to Burst mode by changing R406 & R407 to 100K ohm (p.32)
Change Q49 to INT_F812 part (p.20)
Change Q49 to INT_F812 part by changing R358 to 2.2 ohm, no stuffing R344 and stuffing R343 (p.20)
Reduce audible noise by changing L64 to 152S0139 (p.20)
Add CR38, CR40, CR39, CR44 & CR45 10pF caps near the power switchers FETs (p.20, 32 & 34)
Change PWM L Fan input (both L&R Fans) to +5V_SLEEP pull-up (p.25)
05/30/03 - Change HD DMACLK to digital ground instead of CHGND5 (p.23)
- 06/03/03 - Add CPU Core Voltage offset option circuit (p.33)
- 06/05/03 - Change FW-B connector to S1420058 with internal shield pins (p.28)
- 06/06/03 - Add four 0ohm jumper in case there is no SW support for the multi-stage VCore (p.38)
Change Q14 to P53162 (p.28)
06/12/03 - Change CBUS & USB2 REQ LINE Pullup to +3V_MAIN (p.12)
Add 0 ohm at USB AVSS_GND (p.17)
Change TMSD common mode choke to TDK ACM2012-900H part (p.22)
Add HD DMACLK pullup R215 to 10K (p.24)
Add CR47, CR51 & CR52 at ENET CLK for EMC (p.13 & 26)
Change Q82 pin#4 connection to system digital GND (p.33)
Add CR48 150uF cap at J3 for +5V_MAIN USB2 power (p.25)
Add CR53 1000pF cap at Q64 (p.30)
Add RC at AD7460 power rail for noise isolation (p.25)
Isolate THERM signal at AD7460 by using double inverters for THERM_L_OC (p.25)
Remove redundant pullup R601 for THERM_L_OC (p.29)
Remove SH2 EMI spring at CHGND5 (p.23)
Add additional PWR/GND pins at J17 for R-USB board (p.25)
06/13/03 - New 500DMM connector with 4 through-hole mounting pins (p.11)
Change CPU config stuffing option at R63 and R64 (p.7)
Stuff R288 for Cypress CLK chip (p.14)
Move CBUS_PCI_REQ_L back to +3V_SLEEP rail pull-up (p.12)
Change the TMSD Termination Resistor values to 162ohm (p.20)
Connect CR47 at R160.1 (p.13)
Add 1000pF caps at AD7460 D-plus/minus pairs (p.25)
Add S1152 DVI transmitter to prevent leakage from DVI connector to the system (p.19&20)
- 06/16/03 - Replace C705,C707,C711,C703 & C685 with part 128S0025 (p.20&32)
Remove R771 0ohm resistor (p.34)
Edit Signal Constraints for TMSD routing and ENET routing (p.36&37)

DVT2 RELEASE

- 07/06/03 - Change R97 & R98 to 0402 package (p.33)
No Stuff R835 (p.19)
Change R198 to 100K ohm resistor (p.23)
Add Common Mode Choke L77 & L76 at PWB pairs (p.28)
Removed current monitoring IC for firewire port power (p.28)
Changed RP52,RP53,RP56,RP57 to 22ohm for EMI (p.19)

PRODUCTION RELEASE

- 07/28/03 - Change BOM option for C51,C52,C77,C78,C91,C92,C111 to 8.2uF Panasonic AL cap only (p.34)
- 08/05/03 - Change +3V/5V ITH compensation and No-Stuff Feed Forward Caps (p.32)
- 08/07/03 - Change CPU VCore setting for both BEST and BETTER configurations (p.33)
- 08/07/03 - Change CPU VCore setting for both BEST and BETTER configurations again (p.33)

PRODUCTION RELEASE

- 08/18/03 - Change CPU VCore setting for BEST configuration to: 1.335V(High)->1.080V(Low) (p.33)

PRODUCTION RELEASE (Version B) for 051-6888

- 08/29/05 - Added 138S0223 (88E1111 Rev. B1) as an option
- 08/29/05 - Added 128S0034 as an option
- 08/29/05 - Deleted 740S0006 as BDL


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	D	051-6888	B
SCALE	NONE	SHT	40 OF 40