

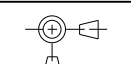
1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
D		412039	PRODUCTION RELEASED	11/29/05	?

PDF	CSA	CONTENTS	SYNC MASTER	DATE
1	1	Table Of Contents	N/A	N/A
2	2	Board Information	N/A	N/A
3	3	System Block Diagram	N/A	N/A
4	4	Power Block Diagram	N/A	N/A
5	5	Revision History	N/A	N/A
6	6	Q16C Pin Swaps	N/A	N/A
7	7	Functional Test Points	N/A	N/A
8	8	I2C Connections	N/A	N/A
9	9	JTAG Connections	N/A	N/A
10	10	Power Synonyms	N/A	N/A
11	11	Signal Synonyms	N/A	N/A
12	12	Power Inputs	N/A	N/A
13	13	Battery Charger	N/A	N/A
14	14	12.8V PBUS/PMU Supplies	N/A	N/A
15	15	5V/3.3V Supplies	N/A	N/A
16	16	1.8V/1.5V Supplies	N/A	N/A
17	17	2.5V Supply	N/A	N/A
18	19	Vesta Power & Misc	N/A	N/A
19	21	I2 Power	N/A	N/A
20	22	I2 Power Supplies	N/A	N/A
21	23	I2 Supplemental	N/A	N/A
22	24	I2 Miscellaneous	N/A	N/A
23	25	PCI Clock Buffer	N/A	N/A
24	26	LEDs/Reset/Debug	N/A	N/A
25	27	Power Management Unit (PMU05)	N/A	N/A
26	29	Power Sequencing	N/A	N/A
27	30	Fan Controller	N/A	N/A
28	31	ALS Support	N/A	N/A
29	32	Sudden Motion Sensor	N/A	N/A
30	33	Q16C Internal I/O I	N/A	N/A
31	34	Q16C Internal I/O II	N/A	N/A
32	35	I2 Processor Interface	N/A	N/A
33	36	A8 MaxBus (CPU0)	MULLET	08/02/2005
34	37	A8 Configuration Straps	MULLET	08/02/2005
35	38	A8 Power (CPU0)	MULLET	08/02/2005
36	39	CPU VCore Supply	N/A	N/A
37	46	CPU AVDD Supply	N/A	N/A
38	47	I2 Memory Interface	N/A	N/A
39	48	Memory Series Termination	N/A	N/A
40	50	DDR2 SO-DIMM Slot A	N/A	N/A

PDF	CSA	CONTENTS	SYNC MASTER	DATE
41	52	DDR2 SO-DIMM Slot B	N/A	N/A
42	55	M11 Frame Buffer Constraints	N/A	N/A
43	56	I2 AGP Interface	N/A	N/A
44	57	GPU (M11) AGP Interface	N/A	N/A
45	58	GPU VCore Supply	N/A	N/A
46	59	GPU (M11) Core Power	N/A	N/A
47	60	GPU (M11) I/O Power	N/A	N/A
48	61	GPU (M11) Frame Buffer I/F	N/A	N/A
49	62	GPU Frame Buffer A	N/A	N/A
50	63	GPU Frame Buffer B	N/A	N/A
51	64	GPU (M11) GPIOs/Straps	N/A	N/A
52	65	GPU (M11) Clocks/Misc	N/A	N/A
53	66	GPU (M11) DVI/DAC Outputs	N/A	N/A
54	67	Lower TMDS Transmitter	N/A	N/A
55	68	Upper TMDS Transmitter	N/A	N/A
56	69	Internal Display Conns	N/A	N/A
57	70	External Display Conns	N/A	N/A
58	71	BootROM	N/A	N/A
59	72	I2 PCI Interface	N/A	N/A
60	73	Q85 Airport/BT Connector	N/A	N/A
61	74	Cardbus	N/A	N/A
62	75	NEC USB2	N/A	N/A
63	81	I2 UATA Interface	N/A	N/A
64	82	HDD/ODD Connectors	N/A	N/A
65	84	I2 Ethernet Interface	N/A	N/A
66	85	Vesta Ethernet PHY	N/A	N/A
67	86	Ethernet Connector	N/A	N/A
68	88	I2 FireWire Interface	N/A	N/A
69	89	Vesta FireWire PHY	N/A	N/A
70	90	FireWire Ports	N/A	N/A
71	91	FireWire Series Term	N/A	N/A
72	92	I2 USB Interface	N/A	N/A
73	93	NEC USB2 Interface	N/A	N/A
74	100	Audio Board Connector	N/A	N/A
75	110	Spacing & Physical Constraints	N/A	N/A
76	111	Spacing & Physical Constraints 2	N/A	N/A
77	112	Cross Reference Page		
78	113	Cross Reference Page		
79	114	Cross Reference Page		
80	115	Cross Reference Page		

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7001	1	SCHEM,MLB,Q16C	SCH1		
820-1940	1	PCBF,MLB,Q16C	PCB1	CRITICAL	
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6MM	[EEE:UEB]	CRITICAL	EEE_UEB
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6MM	[EEE:UEC]	CRITICAL	EEE_UEC
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6MM	[EEE:USK]	CRITICAL	EEE_USK
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6MM	[EEE:USL]	CRITICAL	EEE_USL

DIMENSIONS ARE IN MILLIMETERS		METRIC		Apple Computer Inc.	
XX :	_____	DRAPTER	/	DESIGN CK	/
X.XX :	_____	ENG APPD	/	MFG APPD	/
X.XXX :	_____	QA APPD	/	DESIGNER	/
ANGLES :	_____	RELEASE	/	SCALE	NONE
DO NOT SCALE DRAWING		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE	D
 THIRD ANGLE PROJECTION		DRAWING NUMBER		051-7001	REV. D
SHT 1 OF 115					

Design-Specific Rules

TABLE_SPACING_RULE	STANDARD	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT
TABLE_SPACING_RULE	STANDARD	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT
TABLE_SPACING_RULE	BGA_P1MM	10	0.10 MM	1.25 MM	0.1 MM	12.5 MM
TABLE_SPACING_RULE	BGA_P2MM	20	0.20 MM	1.25 MM	0.1 MM	12.5 MM
TABLE_SPACING_RULE	DEFAULT	*	0.1 MM	2.5 MM	0.15 MM	10.0 MM

"1MM" area defined around BGAs to reduce DRCs caused by fan-out.
 "BGA_P2MM" rule ensures these critical signals do not fan-out routed next to any other signals.

TABLE_PHYSICAL_RULE	STANDARD	DEFAULT	DEFAULT	DEFAULT	DEFAULT
TABLE_PHYSICAL_RULE	STANDARD	*	=DEFAULT	=DEFAULT	=DEFAULT
TABLE_PHYSICAL_RULE	DEFAULT	*	Y	0.100 MM	0.100 mm
TABLE_PHYSICAL_RULE	DEFAULT	*	Y	0.100 mm	1.25 MM

Layer-specific rules for 90-ohm differential impedance

TABLE_SPACING_RULE	TABLE_PHYSICAL_RULE	90_OHM_DIFF	90_OHM_DIFF	90_OHM_DIFF	90_OHM_DIFF	90_OHM_DIFF
TABLE_SPACING_RULE	TABLE_PHYSICAL_RULE	90_OHM_DIFF	90_OHM_DIFF	90_OHM_DIFF	90_OHM_DIFF	90_OHM_DIFF
TABLE_SPACING_RULE	TABLE_PHYSICAL_RULE	90_OHM_DIFF	90_OHM_DIFF	90_OHM_DIFF	90_OHM_DIFF	90_OHM_DIFF

Layer-specific rules for 100-ohm differential impedance

TABLE_SPACING_RULE	TABLE_PHYSICAL_RULE	100_OHM_DIFF	100_OHM_DIFF	100_OHM_DIFF	100_OHM_DIFF	100_OHM_DIFF
TABLE_SPACING_RULE	TABLE_PHYSICAL_RULE	100_OHM_DIFF	100_OHM_DIFF	100_OHM_DIFF	100_OHM_DIFF	100_OHM_DIFF
TABLE_SPACING_RULE	TABLE_PHYSICAL_RULE	100_OHM_DIFF	100_OHM_DIFF	100_OHM_DIFF	100_OHM_DIFF	100_OHM_DIFF

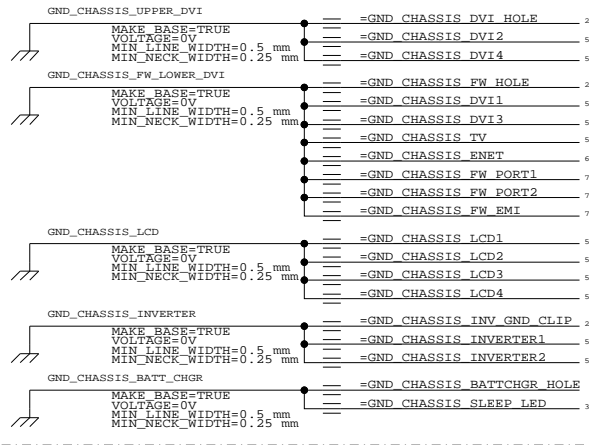
Layer-specific rules for 110-ohm differential impedance

TABLE_SPACING_RULE	TABLE_PHYSICAL_RULE	110_OHM_DIFF	110_OHM_DIFF	110_OHM_DIFF	110_OHM_DIFF	110_OHM_DIFF
TABLE_SPACING_RULE	TABLE_PHYSICAL_RULE	110_OHM_DIFF	110_OHM_DIFF	110_OHM_DIFF	110_OHM_DIFF	110_OHM_DIFF
TABLE_SPACING_RULE	TABLE_PHYSICAL_RULE	110_OHM_DIFF	110_OHM_DIFF	110_OHM_DIFF	110_OHM_DIFF	110_OHM_DIFF

Portable-specific Override Rules

TABLE_SPACING_RULE	TABLE_PHYSICAL_RULE	AGP	AGP_STB	VGA	TV	VGA	TV
TABLE_SPACING_RULE	TABLE_PHYSICAL_RULE	AGP	AGP_STB	VGA	TV	VGA	TV
TABLE_SPACING_RULE	TABLE_PHYSICAL_RULE	AGP	AGP_STB	VGA	TV	VGA	TV

CHASSIS GND CONNECTIONS



Layer-specific rules for 60-ohm single-ended impedance

TABLE_SPACING_RULE	TABLE_PHYSICAL_RULE	60_OHM_SE	60_OHM_SE	60_OHM_SE	60_OHM_SE
TABLE_SPACING_RULE	TABLE_PHYSICAL_RULE	60_OHM_SE	60_OHM_SE	60_OHM_SE	60_OHM_SE
TABLE_SPACING_RULE	TABLE_PHYSICAL_RULE	60_OHM_SE	60_OHM_SE	60_OHM_SE	60_OHM_SE

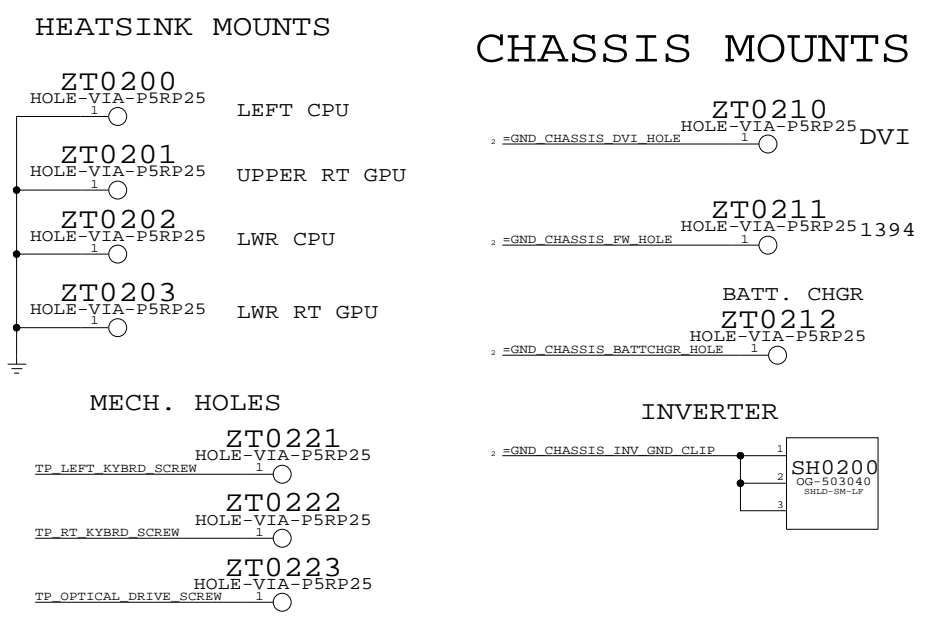
Layer-specific rules for 50-ohm single-ended impedance

TABLE_SPACING_RULE	TABLE_PHYSICAL_RULE	50_OHM_SE	50_OHM_SE	50_OHM_SE	50_OHM_SE
TABLE_SPACING_RULE	TABLE_PHYSICAL_RULE	50_OHM_SE	50_OHM_SE	50_OHM_SE	50_OHM_SE
TABLE_SPACING_RULE	TABLE_PHYSICAL_RULE	50_OHM_SE	50_OHM_SE	50_OHM_SE	50_OHM_SE

NO_TEST Properties

1778_ITH_RC	NO_TEST=TRUE	TP_VESTA_DNC_E9	NO_TEST=TRUE
1778_VRNG	NO_TEST=TRUE	TP_VESTA_F1000	NO_TEST=TRUE
GPU_DVOD_R<18>	NO_TEST=TRUE	TP_VESTA_PHYA<0>	NO_TEST=TRUE
LTC3412_RUNSS	NO_TEST=TRUE	TP_VESTA_REGSEN2	NO_TEST=TRUE
TMDS_CONN_CLKP	NO_TEST=TRUE	TP_VESTA_SPD0	NO_TEST=TRUE
TP_NEC_SMC	NO_TEST=TRUE	USB_NEC_BT_N	NO_TEST=TRUE
TP_NEC_SMI_L	NO_TEST=TRUE	USB_NEC_N<1>	NO_TEST=TRUE
TP_NEC_SRCLK	NO_TEST=TRUE	USB_NEC_N<2>	NO_TEST=TRUE
TP_USB2_PWREN<0>	NO_TEST=TRUE	USB_NEC_N<3>	NO_TEST=TRUE
TP_USB2_PWREN<2>	NO_TEST=TRUE	USB_NEC_P<0>	NO_TEST=TRUE
TP_USB2_PWREN<3>	NO_TEST=TRUE	USB_NEC_P<1>	NO_TEST=TRUE
UATA_DD_R<0>	NO_TEST=TRUE	SI_TMDS_DN<5>	NO_TEST=TRUE
UATA_DD_R<8>	NO_TEST=TRUE	SI_TMDS_DN<4>	NO_TEST=TRUE
UATA_DD_R<10>	NO_TEST=TRUE	SI_TMDS_DP<3>	NO_TEST=TRUE
UATA_DA_R<0>	NO_TEST=TRUE	SI_TMDS_DN<2>	NO_TEST=TRUE
UATA_DA_R<1>	NO_TEST=TRUE	SI_TMDS_DN<1>	NO_TEST=TRUE
		SI_TMDS_DN<0>	NO_TEST=TRUE
		SI_TMDS_CLKP	NO_TEST=TRUE

BOARD HOLES



BOARD STACK-UP AND CONSTRUCTION

SEE BOARD FILE FOR DETAILED INFORMATION
 CONVENTIONAL CONSTRUCTION WITH Pxx TH VIA

Layer	Material	Thickness
1	SIGNAL (1/2 OZ + COPPER PLATING)	
2	PREPREG	
3	GROUND (1/2 OZ)	
4	CORE	
5	SIGNAL (1/2 OZ)	
6	PREPREG	
7	GROUND (1/2 OZ)	
8	CUT POWER PLANE (1 OZ)	
9	CORE	
10	SIGNAL (1/2 OZ)	
11	PREPREG	
12	GROUND (1/2 OZ)	
13	SIGNAL (1/2 OZ + COPPER PLATING)	

BOM OPTIONS

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7338	PCBA, MLB, BESTMHZ, 1.67, VRAM_S, PB15	COMMON, ALTERNATE, gQ16C, gQ16C_BST, EEE_USB, GPU_LF, VRAM_SAMSUNG, gCommon
630-7339	PCBA, MLB, BESTMHZ, 1.67, VRAM_H, PB15	COMMON, ALTERNATE, gQ16C, gQ16C_BST, EEE_USB, GPU_LF, VRAM_HYNIX, gCommon
630-7445	PCBA, MLB, BESTMHZ, GPU_EUT, VRAM_S, PB15	COMMON, ALTERNATE, gQ16C, gQ16C_BST, EEE_USK, GPU_EUTECTIC, VRAM_SAMSUNG, gCommon
630-7446	PCBA, MLB, BESTMHZ, GPU_EUT, VRAM_H, PB15	COMMON, ALTERNATE, gQ16C, gQ16C_BST, EEE_USL, GPU_EUTECTIC, VRAM_HYNIX, gCommon

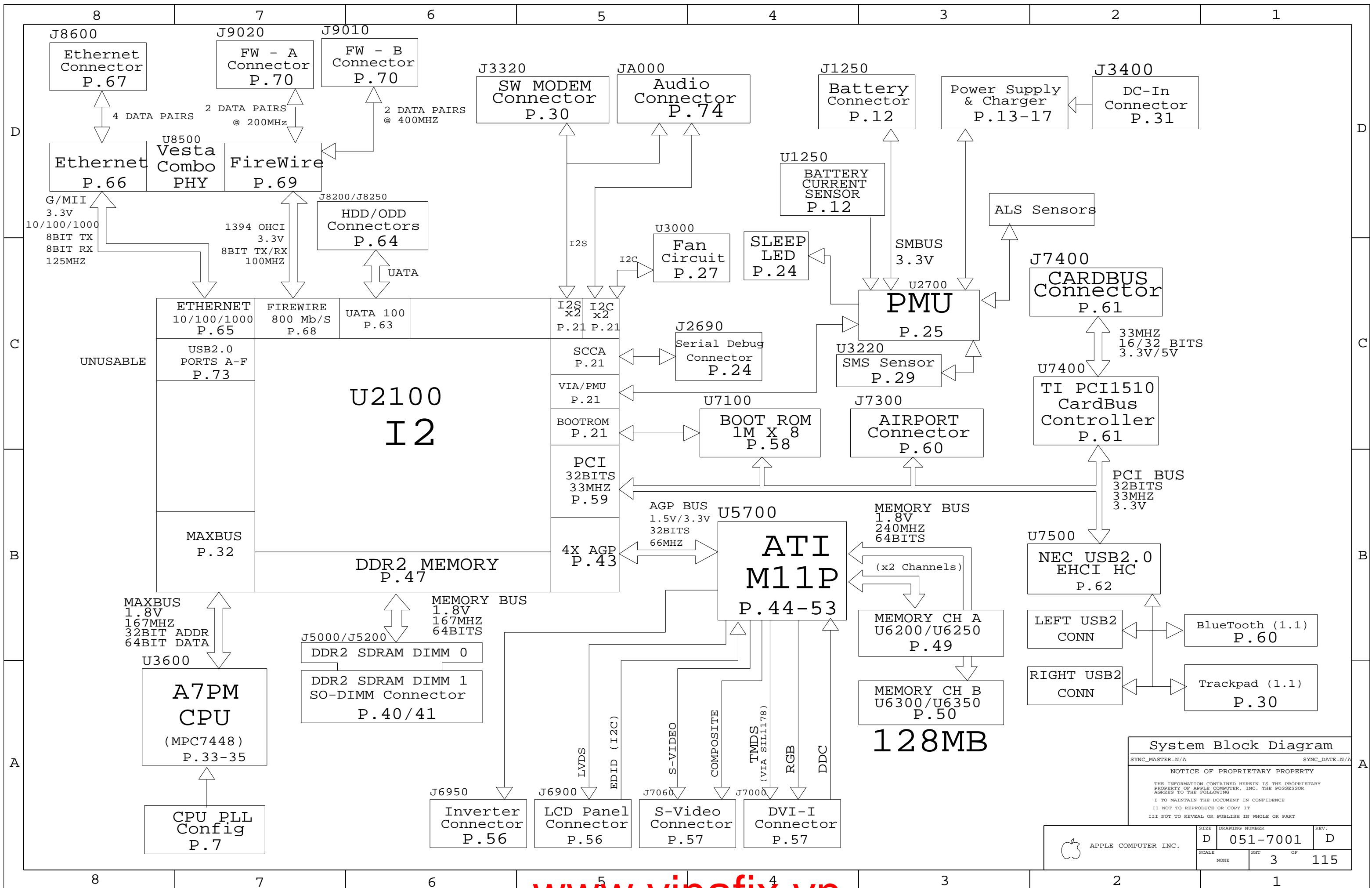
Module Components

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S0383	1	IC, ASIC, I2, REV1.2, NB/SB, 974 BGA	U2100	CRITICAL	
337S3135	1	IC, PMU05, BLANK, QFP	U2700	CRITICAL	PMU_BLANK
341S1772	1	IC, PMU05, V1, QFP	U2700	CRITICAL	PMU_PROG
337S3276	1	IC, A7PM, R1.6, 1.67GHZ, LGA, 1.28V, 23W, 85C	U3600	CRITICAL	A7PM_1P67_LGA
337S3077	1	IC, A8, xxxGHZ	U3600	CRITICAL	CPU_A8
338S0252	1	IC, GPU, M11P	U5700	CRITICAL	GPU_LF
338S0299	1	IC, GPU, M11P, EUTECTIC	U5700	CRITICAL	GPU_EUTECTIC
335S0088	1	BOOTROM, BLANK	U7100	CRITICAL	BOOTROM_BLANK
341S1736	1	IC, BOOTROM, B, Q16C	U7100	CRITICAL	BOOTROM_PROG
343S0356	1	IC, ASIC, VESTA, V1.3, LF	U8500	CRITICAL	
333S0317	4	IC, GDDR SDRAM, 2MX32X4, 300MHZ, LF FBGA144	U6200, U6250, U6300, U6350	CRITICAL	VRAM_SAMSUNG
333S0314	4	IC, GDDR SDRAM, 2MX32X4, 300MHZ, LF FBGA144	U6200, U6250, U6300, U6350	CRITICAL	VRAM_HYNIX

Board Information

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APPLE COMPUTER INC.	D	051-7001	D
SCALE NONE	SHT 2	OF 115	



System Block Diagram

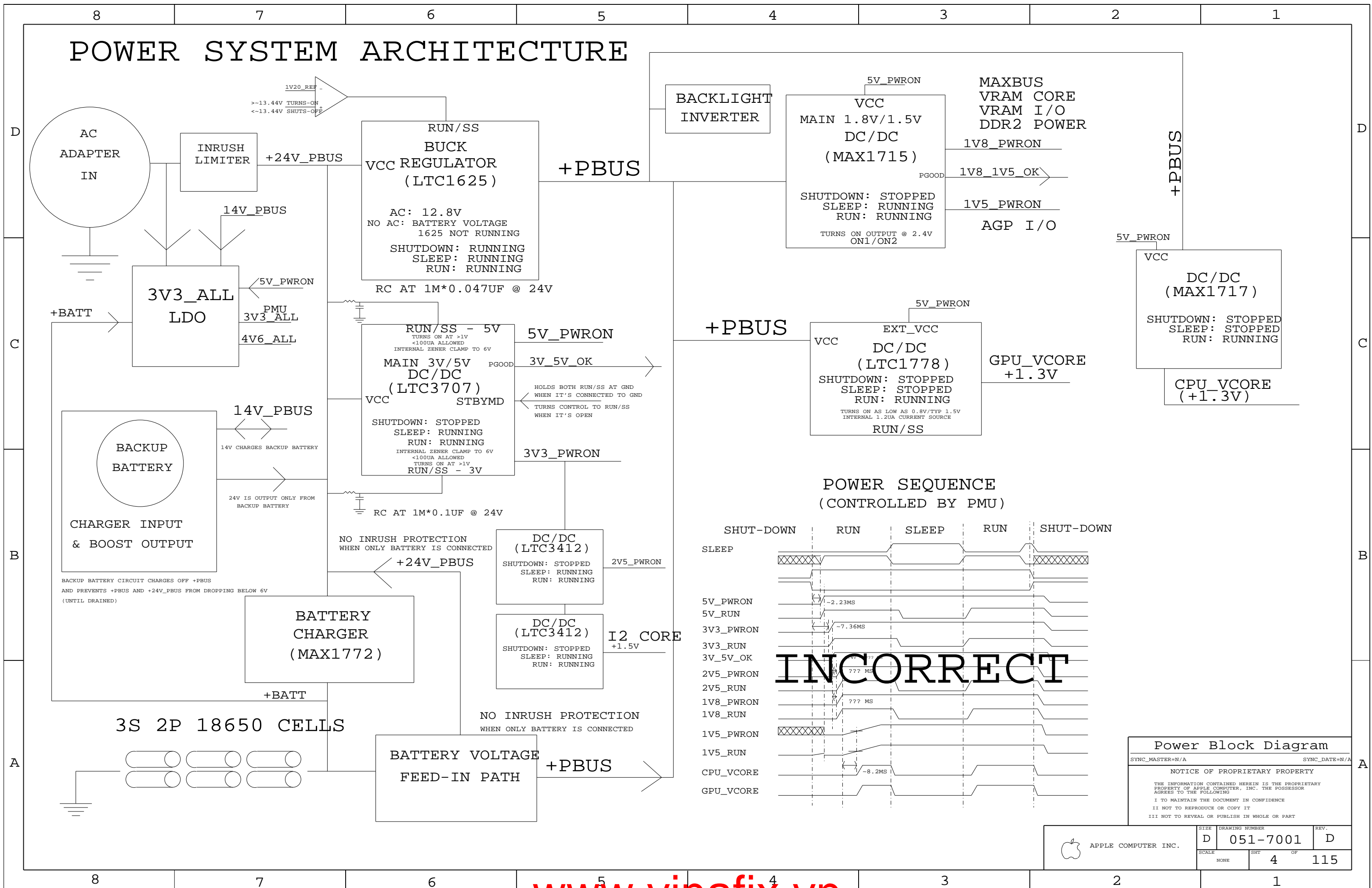
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7001	D
SCALE	SHT		OF
NONE	3		115

POWER SYSTEM ARCHITECTURE



INCORRECT

Power Block Diagram			
SYNC_MASTER=N/A	DRAWING NUMBER		REV.
	D	051-7001	D
SCALE	SHT	OF	REV.
NONE	4	115	

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	NONE	4	115

REVISION HISTORY

EVT

- 04/04/2005 - Beginning revision history
- 04/06/2005 - Made DDR2 and FB pin swaps as requested by CM
- 04/06/2005 - Modem connector moved to non-shared page
- 04/06/2005 - Changed R2941 to level shift/pass FET to correct trackpad power state in sleep
- 04/06/2005 - Made additional FB pin swaps
- 04/11/2005 - Changed DDR2 CS/CKE RPAKs to RPAK2P (added RP4871, RP4876)
- 04/11/2005 - Implemented more DDR2 pin swaps
- 04/11/2005 - Implemented FireWire pin swaps
- 04/11/2005 - Added remaining spacing and physical rule tables
- 04/11/2005 - Added upper LVDS channel to function0 test page
- 04/11/2005 - Changed battery sense resistor to 0.006 ohm (R1250)
- 04/11/2005 - Stuffed R2903 to disable FW port power when off on AC
- 04/12/2005 - Changed audio test to XSR (CA035, CA050, CA051)
- 04/12/2005 - Corrected MIN LINE WIDTH properties on P3V3_PWRON
- 04/12/2005 - Corrected TMS DIFFERENTIAL PAIR properties at DVI connector
- 04/12/2005 - Reduced MIN NECK WIDTH property on GND to 0.2 mm for TMS parts
- 04/12/2005 - Corrected line and neck width properties
- 04/12/2005 - Added high/low swing BOMPTIONS for DVO on SI TMS parts
- 04/13/2005 - Added 1.5V DVO option to GPU
- 04/13/2005 - Removed series R isolating VG from digital ground on FW ports (per design guide)
- 04/15/2005 - Moved FB series R to page 61
- 04/18/2005 - Added remaining VREF inputs and decoupling on GPU
- 04/18/2005 - Corrected system problems on PMU port usage
- 04/19/2005 - Added NO_RST Core properties
- 04/20/2005 - Corrected ENER power rail to PWRON from RUN (for Wake-on-LAN)
- 04/20/2005 - Fixed ENER power rail to PWRON from RUN (for Wake-on-LAN)
- 04/20/2005 - Changed R5880 to 6.34k to take GPU Vcore to 1.3V/1.05V
- 04/21/2005 - Added page 4 and modified pages 11, 35, 81 for design specific pin swaps
- 04/22/2005 - Corrected STOP_AGP_L net name (hooked to I2 now) and removed redundant pullup
- 04/22/2005 - Corrected external pullups to replace missing internal I2 pullups
- 04/22/2005 - Added ADC caps at PMU
- 04/22/2005 - Corrected I2C capacitance for Vesta FireWire crystal (to 18pF)
- 04/22/2005 - Disconnected FW_POWERDOWN from Vesta LPWR_1394 pin
- 04/22/2005 - Corrected pull-down resistor value for 0.006 ohm battery current sense
- 04/22/2005 - Changed 22uF CPU Vcore caps to 330 uF caps
- 04/22/2005 - Changed GPU FB MYREFs into separate dividers
- 04/22/2005 - Rinswapped UTRA I/F, DVO I/F USB pull-downs
- 04/22/2005 - Added extra cap at input to I2 USBVDD
- 05/03/2005 - Added pull-downs to unused HD and debug signals (DTR/RTS)
- 05/03/2005 - Added pull-down to Vesta LPWR_1394
- 05/03/2005 - Added PD/AS signal between HD and ODD connectors
- 05/10/2005 - Various Pb-free component replacements
- 05/13/2005 - Various Pb-free component replacements
- 05/13/2005 - Rinswaps for I2 RPAKs to match up with Q41C style layout
- 05/16/2005 - Various Pb-free component replacements
- 05/19/2005 - Added Synix VRAM option and PCBAs
- 05/19/2005 - Various Pb-free component replacements
- 05/20/2005 - Added EBBN sync circuit
- 05/20/2005 - Various Pb-free component replacements
- 05/21/2005 - Added DSP signal between HD and ODD connectors
- 05/21/2005 - Corrected AGP_INT_L connection between I2 and GPU
- 05/21/2005 - Corrected WKA sync connections at GPU
- 05/23/2005 - Released as REV 01 for Pre-EVT/EVT
- 08/25/2005 - Added USB2 controller
- 08/25/2005 - Added ZDB clock buffer for PCI clocks
- 08/25/2005 - Various Pb-free component replacements
- 08/25/2005 - Removed SMC PIC microcontroller
- 08/25/2005 - Added 2 0.1uF caps to GPU Vcore regulator output
- 08/25/2005 - Corrected USB diff pair and spacing/physical rules on port connections
- 06/01/2005 - Corrected FireWire VP caps to 50V
- 06/01/2005 - Various Pb-free replacements
- 06/02/2005 - Released as REV 02 for EVT
- 06/03/2005 - Changed CPU clock series Rs to 0 ohms
- 06/03/2005 - Released as REV 03 for EVT
- 06/07/2005 - Updated BOM options on CPU Vcore and AVDD for 1.22, 1.30, and 1.33V
- 06/07/2005 - Corrected alternate errors and a leaded table item
- 06/07/2005 - Released as REV 04 for EVT

DVT

- 06/28/2005 - Added 10K pullup to VIA_REQ_L
- 06/28/2005 - Changed R2941 to level shift/pass FET to correct GPU Vcore and CPU Vcore power sequencing
- 06/28/2005 - Moved R2943 to SYS_POWERDOWN_L to correct trackpad power state in sleep
- 06/28/2005 - Moved R2943 to RUN rail to correct pumpup problem in sleep
- 07/06/2005 - Changed to USB1P_NEP_BOMPTION
- 07/06/2005 - Various Pb-free replacements
- 07/06/2005 - Changed TMS drive strength resistors to 301 ohm, which was built at EVT
- 07/06/2005 - Added FET to allow PMU control of trackpad power sequencing
- 07/08/2005 - Added resistor mux for I2's MAXBUS I/O rail (PWRON vs RUN)
- 07/09/2005 - Changed CPU Vcore to 2-states only (no MUX)
- 07/09/2005 - Removed I2's connection to TSEN (leakage path)
- 07/09/2005 - Removed 1.5GHz config
- 07/14/2005 - Changed 32.768kHz crystal to new APN specifying 1uW drive parts
- 07/14/2005 - Added line width constraints to LFC1625 and CPU Vcore gate nodes
- 07/18/2005 - Added external 10K pullups in parallel with all I2 internal pullups
- 07/18/2005 - Changed R2941 series R value to 19.2 ohm
- 07/18/2005 - Added 150 ohm pull-downs to FW_CTL lines at Vesta
- 07/19/2005 - Changed TMS transmitter ferrites to part with higher current rating (1.5A)
- 07/19/2005 - Added BOMPTIONS for and stuffed CPU Vcore at 1.28V and 1.30V
- 07/19/2005 - Added audio mute sequencing FETs
- 07/19/2005 - Moved UATA_DSTROBE cap to other side of series resistor
- 07/22/2005 - Released as REV 06 for DVT
- 07/22/2005 - Changed all external I2 GPIO pullups to 10K
- 07/25/2005 - Stuffed R2942, R2943 to correct I2 2.5V pullup problem
- 07/25/2005 - Replaced 371S0299 with 371S0300
- 07/25/2005 - Swapped I2 MAXBUS 130ohm and I2 MAXBUS 500ohm BOMPTIONS
- 07/26/2005 - Changed to Vesta v1.4 as primary, 08500 Vesta v1.3 as alternate
- 07/26/2005 - Changed PCI ZDB output series term 500 to 2 ohms
- 07/29/2005 - Swapped locations of Vcore and AVDD
- 07/29/2005 - Released as REV 07 for DVT

Pre-PVT

- 08/02/2005 - Added R0985 10K pull down on JTAG_CPU0_TCK
- 08/02/2005 - Added R3773 10K pull down on CPU0_EXT_QUAL on Mullet and sync'd
- 08/05/2005 - Changed R2947 to 2200pF
- 08/05/2005 - Changed C1730 and C2205 to 2200pF
- 08/05/2005 - Changed C1730 to 5.6pF
- 08/05/2005 - Changed C1700 and C1701 and C2215 and C2216 to 47uF
- 08/05/2005 - Changed R1720 and R2205 to 7.5k
- 08/05/2005 - Changed C3940-C3947 to 1206 ceramic caps
- 08/17/2005 - Changed power supply jumpers to shorts
- 08/17/2005 - Added five ceramic caps to Vcore supply
- 08/17/2005 - Changed to 60 schottky to reduce reverse leakage
- 08/18/2005 - Changed R2958 to 10K for improved power sequencing timing
- 08/22/2005 - Added FETs to reduce leakage onto Vesta rails
- 08/24/2005 - Changed C3600-PE801 to 1uF due to insertion of FET
- 08/24/2005 - Changed R5822 to 100K for power sequence improvement
- 08/24/2005 - No stuffed R2949 for power sequence improvement
- 08/24/2005 - Released as REV 08 for Pre-PVT

PVT

- 08/29/2005 - (051-6929) Released as REV A for PVT
- 08/31/2005 - Stuffed R8424 with 10K 5% to ensure MDIO logic levels
- 08/31/2005 - Stuffed R8424 to correct unused GPIO logic level
- 09/02/2005 - Changed ML2 to 820-1940 which corrects tolerance on DIMM conn holes
- 09/09/2005 - Changed C3204-C3206 to 0.05uF for SPS filtering improvements
- 09/09/2005 - (051-7001) Released as REV A for Production

D

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	D	051-7001	D
SCALE	SHT	OF	
NONE	5	115	

	8	7	6	5	4	3	2	1											
D	<h3>I2S Series Rs</h3> <pre> MAKE_BASE=TRUE 22 I2S0_SB_TO_DEV.DTO.R == =RP1150P1 11 11 =RP1150P8 == I2S0_SB_TO_DEV.DTO 7 74 MAKE_BASE=TRUE MAKE_BASE=TRUE 22 I2S0_BITCLK_R == =RP1150P2 11 11 =RP1150P7 == I2S0_BITCLK 7 74 MAKE_BASE=TRUE MAKE_BASE=TRUE 22 I2S0_MCLK_R == =RP1150P3 11 11 =RP1150P6 == I2S0_MCLK 7 74 MAKE_BASE=TRUE MAKE_BASE=TRUE 22 I2S0_SYNC_R == =RP1150P4 11 11 =RP1150P5 == I2S0_SYNC 7 74 MAKE_BASE=TRUE MAKE_BASE=TRUE 22 I2S1_SB_TO_DEV.DTO.R == =RP1151P1 11 11 =RP1151P8 == I2S1_SB_TO_DEV.DTO 30 MAKE_BASE=TRUE MAKE_BASE=TRUE 22 I2S1_SYNC_R == =RP1151P2 11 11 =RP1151P7 == I2S1_SYNC 30 MAKE_BASE=TRUE MAKE_BASE=TRUE 22 I2S1_MCLK_R == =RP1151P3 11 11 =RP1151P6 == I2S1_MCLK 30 MAKE_BASE=TRUE MAKE_BASE=TRUE 22 I2S1_BITCLK_R == =RP1151P4 11 11 =RP1151P5 == I2S1_BITCLK 30 MAKE_BASE=TRUE </pre>				<h3>Lower DVO Series Rs</h3> <pre> MAKE_BASE=TRUE 53 GPU_DVOD_R<16> == =RP6720P1 54 54 =RP6720P8 == GPU_DVOD<16> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<4> == =RP6720P2 54 54 =RP6720P7 == GPU_DVOD<4> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<7> == =RP6720P3 54 54 =RP6720P6 == GPU_DVOD<7> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<6> == =RP6720P4 54 54 =RP6720P5 == GPU_DVOD<6> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<11> == =RP6721P1 54 54 =RP6721P8 == GPU_DVOD<11> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<9> == =RP6721P2 54 54 =RP6721P7 == GPU_DVOD<9> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<10> == =RP6721P3 54 54 =RP6721P6 == GPU_DVOD<10> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVO_HSYNC_R == =RP6721P4 54 54 =RP6721P5 == GPU_DVO_HSYNC 54 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<3> == =RP6722P1 54 54 =RP6722P8 == GPU_DVOD<3> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<5> == =RP6722P2 54 54 =RP6722P7 == GPU_DVOD<5> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<13> == =RP6722P3 54 54 =RP6722P6 == GPU_DVOD<13> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<12> == =RP6722P4 54 54 =RP6722P5 == GPU_DVOD<12> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<2> == =RP6723P1 54 54 =RP6723P8 == GPU_DVOD<2> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<1> == =RP6723P2 54 54 =RP6723P7 == GPU_DVOD<1> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<0> == =RP6723P3 54 54 =RP6723P6 == GPU_DVOD<0> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<14> == =RP6723P4 54 54 =RP6723P5 == GPU_DVOD<14> 55 MAKE_BASE=TRUE </pre>				D										
C	<h3>UATA Series Rs</h3> <pre> MAKE_BASE=TRUE 63 UATA_DD_R<12> == =RP8150P1 63 63 =RP8150P8 == UATA_DD<12> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_CS0_L_R == =RP8150P2 63 63 =RP8150P7 == UATA_CS0_L 7 63 64 MAKE_BASE=TRUE (IDE_CS1FX_L) MAKE_BASE=TRUE 63 UATA_DD_R<14> == =RP8150P3 63 63 =RP8150P6 == UATA_DD<14> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<11> == =RP8150P4 63 63 =RP8150P5 == UATA_DD<11> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<7> == =RP8151P1 63 63 =RP8151P8 == UATA_DD<7> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<2> == =RP8151P2 63 63 =RP8151P7 == UATA_DD<2> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<3> == =RP8151P3 63 63 =RP8151P6 == UATA_DD<3> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<15> == =RP8151P4 63 63 =RP8151P5 == UATA_DD<15> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<9> == =RP8152P1 63 63 =RP8152P8 == UATA_DD<9> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<4> == =RP8152P2 63 63 =RP8152P7 == UATA_DD<4> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<6> == =RP8152P3 63 63 =RP8152P6 == UATA_DD<6> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<5> == =RP8152P4 63 63 =RP8152P5 == UATA_DD<5> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DA_R<2> == =RP8153P1 63 63 =RP8153P8 == UATA_DA<2> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<8> == =RP8153P2 63 63 =RP8153P7 == UATA_DD<8> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<10> == =RP8153P3 63 63 =RP8153P6 == UATA_DD<10> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DA_R<0> == =RP8153P4 63 63 =RP8153P5 == UATA_DA<0> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<13> == =RP8154P1 63 63 =RP8154P8 == UATA_DD<13> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<0> == =RP8154P2 63 63 =RP8154P7 == UATA_DD<0> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<1> == =RP8154P3 63 63 =RP8154P6 == UATA_DD<1> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DA_R<1> == =RP8154P4 63 63 =RP8154P5 == UATA_DA<1> 7 63 64 MAKE_BASE=TRUE </pre>				<h3>Upper DVO Series Rs</h3> <pre> MAKE_BASE=TRUE 53 GPU_DVO_DE_R == =RP6821P1 55 55 =RP6821P8 == GPU_DVO_DE 54 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVO_VSYNC_R == =RP6821P2 55 55 =RP6821P7 == GPU_DVO_VSYNC 54 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVO_CLKP_R == =RP6821P3 55 55 =RP6821P6 == GPU_DVO_CLKP 54 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<8> == =RP6821P4 55 55 =RP6821P5 == GPU_DVOD<8> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<21> == =RP6822P1 55 55 =RP6822P8 == GPU_DVOD<21> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<19> == =RP6822P2 55 55 =RP6822P7 == GPU_DVOD<19> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<17> == =RP6822P3 55 55 =RP6822P6 == GPU_DVOD<17> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<15> == =RP6822P4 55 55 =RP6822P5 == GPU_DVOD<15> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<20> == =RP6823P1 55 55 =RP6823P8 == GPU_DVOD<20> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<22> == =RP6823P2 55 55 =RP6823P7 == GPU_DVOD<22> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<23> == =RP6823P3 55 55 =RP6823P6 == GPU_DVOD<23> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<18> == =RP6823P4 55 55 =RP6823P5 == GPU_DVOD<18> 55 MAKE_BASE=TRUE </pre>				C										
B	<h3>MAXBUS Pullups</h3> <pre> MAKE_BASE=TRUE 33 MAXBUS_TS_L == =RP3510P1 32 MAKE_BASE=TRUE MAKE_BASE=TRUE 32 MAXBUS_CPU1_BG_L == =RP3510P2 32 MAKE_BASE=TRUE MAKE_BASE=TRUE 31 MAXBUS_CPU0_DBG_L == =RP3510P3 32 MAKE_BASE=TRUE MAKE_BASE=TRUE NC_MAXBUS_I2_TBNEN == =RP3510P4 32 NO_TEST=YES MAKE_BASE=TRUE 33 MAXBUS_CPU0_BG_L == =RP3511P1 32 MAKE_BASE=TRUE MAKE_BASE=TRUE 32 MAXBUS_CPU1_HIT_L == =RP3511P2 32 MAKE_BASE=TRUE MAKE_BASE=TRUE 31 MAXBUS_CPU0_HIT_L == =RP3511P3 32 MAKE_BASE=TRUE MAKE_BASE=TRUE 32 MAXBUS_CPU0_BR_L == =RP3511P4 32 MAKE_BASE=TRUE MAKE_BASE=TRUE 32 MAXBUS_CPU1_BR_L == =RP3512P1 32 MAKE_BASE=TRUE MAKE_BASE=TRUE 31 MAXBUS_TA_L == =RP3512P2 32 MAKE_BASE=TRUE MAKE_BASE=TRUE 34 MAXBUS_CPU0_INT_L == =RP3512P3 32 MAKE_BASE=TRUE MAKE_BASE=TRUE 32 MAXBUS_CPU1_INT_L == =RP3512P4 32 MAKE_BASE=TRUE MAKE_BASE=TRUE 33 MAXBUS_CPU0_DRDY_L == =RP3513P2 32 MAKE_BASE=TRUE MAKE_BASE=TRUE 32 MAXBUS_CPU1_DRDY_L == =RP3513P3 32 MAKE_BASE=TRUE MAKE_BASE=TRUE 31 MAXBUS_AACK_L == =RP3513P4 32 MAKE_BASE=TRUE MAKE_BASE=TRUE 33 MAXBUS_ARTRY_L == =RP3514P1 32 MAKE_BASE=TRUE MAKE_BASE=TRUE 32 MAXBUS_CPU1_DBG_L == =RP3514P2 32 MAKE_BASE=TRUE MAKE_BASE=TRUE 33 MAXBUS_TEA_L == =RP3514P3 32 MAKE_BASE=TRUE </pre>		<h3>AGP Pullups</h3> <pre> MAKE_BASE=TRUE 44 AGP_TRDY_L == =RP5610P1 43 MAKE_BASE=TRUE MAKE_BASE=TRUE 44 AGP_IRDY_L == =RP5610P2 43 MAKE_BASE=TRUE MAKE_BASE=TRUE 44 AGP_REQ_L == =RP5610P3 43 MAKE_BASE=TRUE MAKE_BASE=TRUE 44 AGP_RBF_L == =RP5610P4 43 MAKE_BASE=TRUE MAKE_BASE=TRUE 44 AGP_FRAME_L == =RP5611P1 43 MAKE_BASE=TRUE MAKE_BASE=TRUE 44 AGP_DEVSEL_L == =RP5611P2 43 MAKE_BASE=TRUE MAKE_BASE=TRUE 44 AGP_STOP_L == =RP5611P3 43 MAKE_BASE=TRUE MAKE_BASE=TRUE 44 AGP_GNT_L == =RP5611P4 43 MAKE_BASE=TRUE MAKE_BASE=TRUE 11 PCI_AIRPORT_GNT_L == =RP7250P1 59 MAKE_BASE=TRUE MAKE_BASE=TRUE 60 PCI_TRDY_L == =RP7250P2 59 MAKE_BASE=TRUE MAKE_BASE=TRUE 60 PCI_IRDY_L == =RP7250P3 59 MAKE_BASE=TRUE MAKE_BASE=TRUE 60 PCI_STOP_L == =RP7250P4 59 MAKE_BASE=TRUE MAKE_BASE=TRUE 11 PCI_CBUS_REQ_L == =RP7251P1 59 MAKE_BASE=TRUE MAKE_BASE=TRUE 11 PCI_AIRPORT_REQ_L == =RP7251P2 59 MAKE_BASE=TRUE MAKE_BASE=TRUE 11 PCI_CBUS_GNT_L == =RP7251P3 59 MAKE_BASE=TRUE MAKE_BASE=TRUE 60 PCI_FRAME_L == =RP7251P4 59 MAKE_BASE=TRUE </pre>		<h3>USB Pulldowns</h3> <pre> 72 =RP9210P8 == USB_I2_BT_P 11 MAKE_BASE=TRUE 72 =RP9210P7 == USB_I2_BT_N 11 MAKE_BASE=TRUE 72 =RP9210P6 == USB2_I2_RIGHT_PORT_N 11 MAKE_BASE=TRUE 72 =RP9210P5 == USB2_I2_RIGHT_PORT_P 11 MAKE_BASE=TRUE 72 =RP9211P8 == USB2_I2_P<1> 72 MAKE_BASE=TRUE 72 =RP9211P7 == USB2_I2_N<1> 72 MAKE_BASE=TRUE 72 =RP9211P6 == USB2_I2_N<3> 72 MAKE_BASE=TRUE 72 =RP9211P5 == USB2_I2_P<3> 72 MAKE_BASE=TRUE 72 =RP9212P8 == USB_I2_TPAD_N 11 MAKE_BASE=TRUE 72 =RP9212P7 == USB_I2_TPAD_P 11 MAKE_BASE=TRUE 72 =RP9212P6 == USB2_I2_LEFT_PORT_P 11 MAKE_BASE=TRUE 72 =RP9212P5 == USB2_I2_LEFT_PORT_N 11 MAKE_BASE=TRUE 71 =RP9300P8 == USB2_NEC_LEFT_PORT_P 11 MAKE_BASE=TRUE 71 =RP9300P7 == USB2_NEC_LEFT_PORT_N 11 MAKE_BASE=TRUE 71 =RP9300P6 == USB2_NEC_RIGHT_PORT_N 11 MAKE_BASE=TRUE 71 =RP9300P5 == USB2_NEC_RIGHT_PORT_P 11 MAKE_BASE=TRUE 71 =RP9301P8 == USB_NEC_BT_P 11 MAKE_BASE=TRUE 71 =RP9301P7 == USB_NEC_BT_N 2 11 MAKE_BASE=TRUE 71 =RP9301P6 == USB_NEC_TPAD_N 11 MAKE_BASE=TRUE 71 =RP9301P5 == USB_NEC_TPAD_P 11 MAKE_BASE=TRUE </pre>		B												
A	<h3>FW Series Rs</h3> <pre> MAKE_BASE=TRUE 68 FW_D_R<7> == =RP9100P1 71 71 =RP9100P8 == FW_D<7> 9 69 MAKE_BASE=TRUE MAKE_BASE=TRUE 68 FW_D_R<3> == =RP9100P2 71 71 =RP9100P7 == FW_D<3> 9 69 MAKE_BASE=TRUE MAKE_BASE=TRUE 68 FW_D_R<4> == =RP9100P3 71 71 =RP9100P6 == FW_D<4> 9 69 MAKE_BASE=TRUE MAKE_BASE=TRUE 68 FW_D_R<2> == =RP9100P4 71 71 =RP9100P5 == FW_D<2> 9 69 MAKE_BASE=TRUE MAKE_BASE=TRUE 68 FW_D_R<0> == =RP9101P1 71 71 =RP9101P8 == FW_D<0> 9 69 MAKE_BASE=TRUE MAKE_BASE=TRUE 68 FW_D_R<6> == =RP9101P2 71 71 =RP9101P7 == FW_D<6> 9 69 MAKE_BASE=TRUE MAKE_BASE=TRUE 68 FW_D_R<1> == =RP9101P3 71 71 =RP9101P6 == FW_D<1> 9 69 MAKE_BASE=TRUE MAKE_BASE=TRUE 68 FW_D_R<5> == =RP9101P4 71 71 =RP9101P5 == FW_D<5> 9 69 MAKE_BASE=TRUE </pre>				A														
<h3>Q16C Pin Swaps</h3> <p>SYNC_MASTER=N/A SYNC_DATE=N/A</p> <p>NOTICE OF PROPRIETARY PROPERTY</p> <p>THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</p> <p>I TO MAINTAIN THE DOCUMENT IN CONFIDENCE</p> <p>II NOT TO REPRODUCE OR COPY IT</p> <p>III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</p>																			
 <table border="1"> <tr> <td>SIZE</td> <td>DRAWING NUMBER</td> <td>REV.</td> </tr> <tr> <td>D</td> <td>051-7001</td> <td>D</td> </tr> <tr> <td>SCALE</td> <td>SHT</td> <td>OF</td> </tr> <tr> <td>NONE</td> <td>6</td> <td>115</td> </tr> </table>								SIZE	DRAWING NUMBER	REV.	D	051-7001	D	SCALE	SHT	OF	NONE	6	115
SIZE	DRAWING NUMBER	REV.																	
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	8	7	6	5	4	3	2	1											

Enhanced MAC-1 Test Coverage

Functional test points use a P6 pad placed on bottom side.

Category	Test Point	Pin	FUNC_TEST	Notes
POWER	PP24V_ADAPTER	10	FUNC_TEST=YES	Place 2 TPs @ connector.
	PP24V_ALL_PBUSA	10	FUNC_TEST=YES	
	PP12V8_ALL_PBUSB	10	FUNC_TEST=YES	
	PPVCORE_RUN_GPU	10	FUNC_TEST=YES	Place within 50 mm of power supply.
	PPVCORE_RUN_CPU	10	FUNC_TEST=YES	
	PP1V8_PWRON	10	FUNC_TEST=YES	
	PP2V5_PWRON	10	FUNC_TEST=YES	
	PP5V_PWRON	10	FUNC_TEST=YES	
	PP3V3_PWRON	10	FUNC_TEST=YES	Place 5-10 GND TPs.
	PP5V_RUN	10	FUNC_TEST=YES	
PP3V3_ALL	10	FUNC_TEST=YES		
=FTP_GND	7 10	FUNC_TEST=YES		
LVDS	LVDS_U0_P	53 56	FUNC_TEST=YES	Place within 25 mm of LVDS connector.
	LVDS_U0_N	53 56	FUNC_TEST=YES	
	LVDS_U1_P	53 56	FUNC_TEST=YES	
	LVDS_U1_N	53 56	FUNC_TEST=YES	
	LVDS_U2_P	53 56	FUNC_TEST=YES	
	LVDS_U2_N	53 56	FUNC_TEST=YES	
	CLKLVDS_U_P	53 56	FUNC_TEST=YES	
	CLKLVDS_U_N	53 56	FUNC_TEST=YES	
	LVDS_L0_P	53 56	FUNC_TEST=YES	
	LVDS_L0_N	53 56	FUNC_TEST=YES	
	LVDS_L1_P	53 56	FUNC_TEST=YES	
	LVDS_L1_N	53 56	FUNC_TEST=YES	
	LVDS_L2_P	53 56	FUNC_TEST=YES	
	LVDS_L2_N	53 56	FUNC_TEST=YES	
	CLKLVDS_L_P	53 56	FUNC_TEST=YES	
	CLKLVDS_L_N	53 56	FUNC_TEST=YES	
	LVDS_DDC_CLK	51 56	FUNC_TEST=YES	
	LVDS_DDC_DATA	51 56	FUNC_TEST=YES	
=PP3V3_DDC_LCD	10 56	FUNC_TEST=YES		
PP3V3_LCD_CONN	56	FUNC_TEST=YES		
INVERTER	PPBUS_INVERTER	56	FUNC_TEST=YES	Place within 25 mm of inverter connector.
	PP5V_INV_SW	56	FUNC_TEST=YES	
	BRIGHT_PWM	56	FUNC_TEST=YES	
	GND_INVERTER	56	FUNC_TEST=YES	
UATA	=PP5V_RUN_ODD	10 64	FUNC_TEST=YES	Place within 50 mm of ODD/HDD connector.
	=PP5V_RUN_HDD	10 64	FUNC_TEST=YES	
	PP3V3R5V_RUN_HDD_LOGIC	64	FUNC_TEST=YES	
	UATA_DD<15..0>	6 63 64	FUNC_TEST=YES	
	UATA_DMAR0	63 64	FUNC_TEST=YES	
	UATA_DSTROBE	63 64	FUNC_TEST=YES	
	UATA_DMACK_L	63 64	FUNC_TEST=YES	
	UATA_DA<2..0>	6 63 64	FUNC_TEST=YES	
	UATA_CS0_L	6 63 64	FUNC_TEST=YES	
	UATA_CS1_L	63 64	FUNC_TEST=YES	
	UATA_RESET_L	63 64	FUNC_TEST=YES	
	UATA_HSTROBE	63 64	FUNC_TEST=YES	
UATA_STOP	63 64	FUNC_TEST=YES		
UATA_INTRO	63 64	FUNC_TEST=YES		
AUDIO	PP5V_PWRON_AUDIO_PVDD	74	FUNC_TEST=YES	Place within 25 mm of audio connector.
	PP5V_PWRON_AUDIO_AVDD	74	FUNC_TEST=YES	
	PP3V3_PWRON_AUDIO_AVDD	74	FUNC_TEST=YES	
	=PP3V3_RUN_AUDIO	10 74	FUNC_TEST=YES	
	=I2C_AUDIO_SCL	8 74	FUNC_TEST=YES	
	=I2C_AUDIO_SDA	8 74	FUNC_TEST=YES	
	I2S0_MCLK	6 74	FUNC_TEST=YES	
	I2S0_BITCLK	6 74	FUNC_TEST=YES	
	I2S0_SYNC	6 74	FUNC_TEST=YES	
	I2S0_SB_TO_DEV_DTO	6 74	FUNC_TEST=YES	
	I2S0_DEV_TO_SB_DTI	22 74	FUNC_TEST=YES	
	AUDIO_LO_MUTE_L	22 74	FUNC_TEST=YES	
	AUDIO_SPKR_MUTE_L	22 74	FUNC_TEST=YES	
	AUDIO_CODEC_RESET_L	22 74	FUNC_TEST=YES	
	AUDIO_SPDIFRX_RESET_L	22 74	FUNC_TEST=YES	
	AUDIO_LO_DET_L	22 74	FUNC_TEST=YES	
	AUDIO_LI_DET_L	22 74	FUNC_TEST=YES	
	AUDIO_LO_OPTICAL_PLUG_L	22 74	FUNC_TEST=YES	
AUDIO_LI_OPTICAL_PLUG_L	22 74	FUNC_TEST=YES		
AUDIO_I2S_DTIB_SEL	22 74	FUNC_TEST=YES		
AUDIO_EXT_MCLK_SEL	22 74	FUNC_TEST=YES		
AUDIO_GPIO_11	22 74	FUNC_TEST=YES		
GND_AUDIO_AGND	74	FUNC_TEST=YES		
GND_AUDIO_PGND	74	FUNC_TEST=YES		

Category	Test Point	Pin	FUNC_TEST	Notes
SYSTEM	PP5V_TPAD_F	10 30	FUNC_TEST=YES	Place within 25 mm of TPAD connector.
	USB_TPAD_P	11 30	FUNC_TEST=YES	
	USB_TPAD_N	11 30	FUNC_TEST=YES	
	PP3V3_PWRON_DS1775_R	10	FUNC_TEST=YES	
	SYS_OVERTEMP_L	11 25 30	FUNC_TEST=YES	
	PP3V3_ALL_HALL_EFFRCT_R	10	FUNC_TEST=YES	
	SYS_LID_OPEN_F	10	FUNC_TEST=YES	
	SYS_POWER_BUTTON_L_F	10	FUNC_TEST=YES	
	=FTP_SLEEP_LED	10	FUNC_TEST=YES	
	SYS_CHARGE_LED_L	24 74	FUNC_TEST=YES	
	SYS_ADAPTER_ANALOG_AC_DET	12 74	FUNC_TEST=YES	
	KBDLED_ANODE	28 30	FUNC_TEST=YES	
	KBDLED_RETURN	28 30	FUNC_TEST=YES	
=I2C_DS1775_SDA	8 30	FUNC_TEST=YES		
=I2C_DS1775_SCL	8 30	FUNC_TEST=YES		
CPU FAN	=PP5V_FAN1_PWR	10 31	FUNC_TEST=YES	Place within 25 mm of fan connector.
	FAN1_TACH	27 31	FUNC_TEST=YES	
	FAN1_PWM	27 31	FUNC_TEST=YES	
	=FTP_GND	7 10	FUNC_TEST=YES	
GPU FAN	=PP5V_FAN2_PWR	10 31	FUNC_TEST=YES	Place within 25 mm of fan connector.
	FAN2_TACH	27 31	FUNC_TEST=YES	
	FAN2_PWM	27 31	FUNC_TEST=YES	
	=FTP_GND	7 10	FUNC_TEST=YES	
ALS	=PP3V3_PWRON_LEFT_ALS	10 31	FUNC_TEST=YES	Place within 25 mm of ALS connector.
	ALS_0_OUT	25 31	FUNC_TEST=YES	
	ALS_GAIN_BOOST	25 28 31	FUNC_TEST=YES	
SCCA	SCCA_RXD	22 24	FUNC_TEST=YES	Place within 25 mm of debug connector.
	SCCA_TXD_L	22 24	FUNC_TEST=YES	
BACKUP BATT	=PPVIO_BU_BATT	10 31	FUNC_TEST=YES	Place within 25 mm of battery connector.
	=PPVOUT_BU_BATT	10 31	FUNC_TEST=YES	
RT USB	=PP5V_PWRON_RIGHT_USB	10 31	FUNC_TEST=YES	Place within 25 mm of right USB connector.
	USB2_RIGHT_PORT_P	11 31	FUNC_TEST=YES	
	USB2_RIGHT_PORT_N	11 31	FUNC_TEST=YES	
LT USB	=PP5V_PWRON_LEFT_USB	10 74	FUNC_TEST=YES	Place within 25 mm of left USB connector.
	USB2_LEFT_PORT_P	11 74	FUNC_TEST=YES	
	USB2_LEFT_PORT_N	11 74	FUNC_TEST=YES	

Functional Test Points

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NONE	7	115

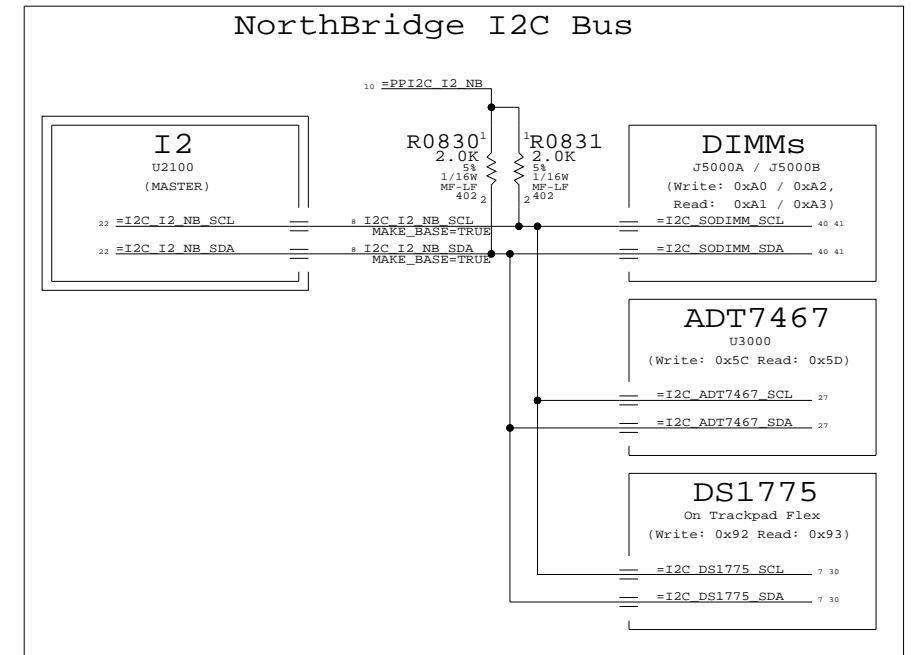
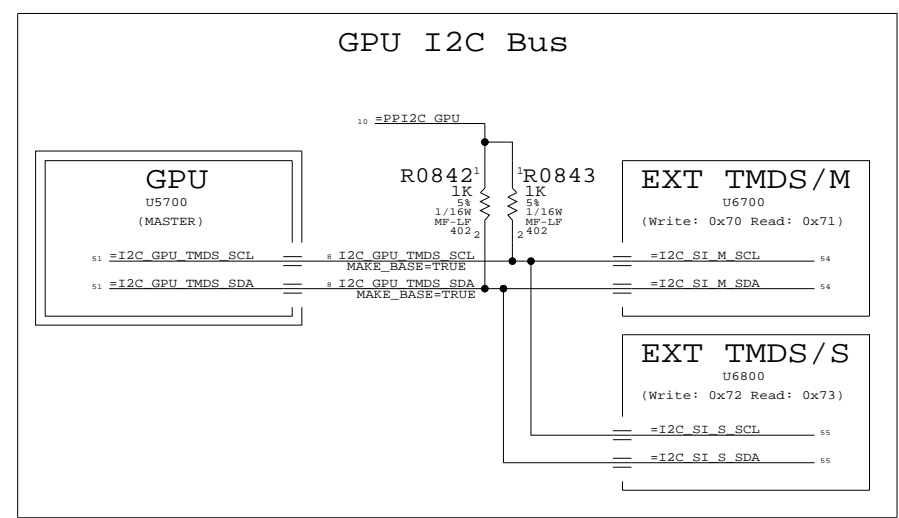
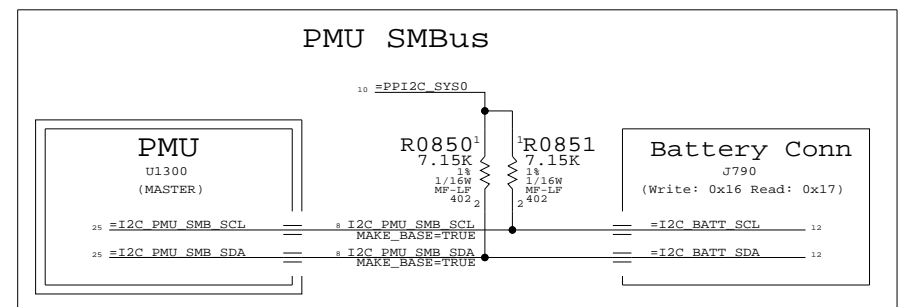
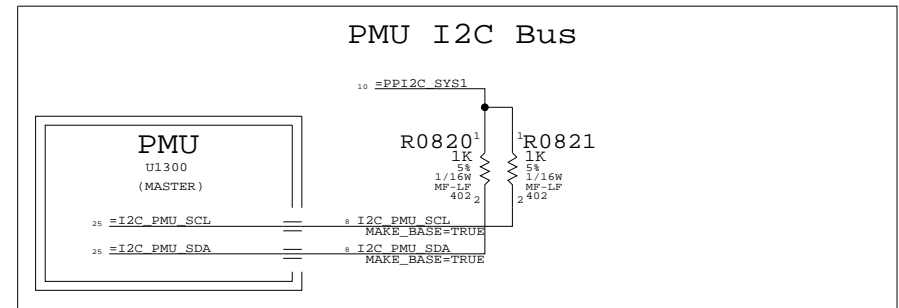
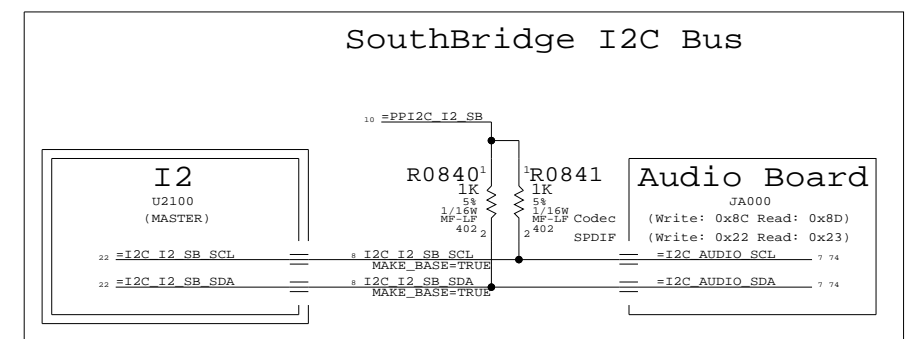
ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
	I2C	I2C		I2C_PMU_SMB_SCL
	I2C	I2C		I2C_PMU_SMB_SDA
	I2C	I2C		I2C_PMU_SCL
	I2C	I2C		I2C_PMU_SDA
I2C_NB	I2C	I2C		I2C_I2_NB_SCL
I2C_NB	I2C	I2C		I2C_I2_NB_SDA
	I2C	I2C		I2C_I2_SB_SCL
	I2C	I2C		I2C_I2_SB_SDA
	I2C	I2C		I2C_GPU_TMDS_SCL
	I2C	I2C		I2C_GPU_TMDS_SDA

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- GOV_I2C / GOV_I2C_BYPASS
Allows bypassing Governor I2C bus.
Most devices are connected directly to PMU instead. One ADT7467 connects to NB I2C bus 1 to resolve address conflict.
- MMM_PWR_ALL / MMM_PWR_PWRON
Selects whether MMM MCU is powered all the time or only when the system is on. ALL moves the MCU to the PMU I2C bus so it can be monitored by in shutdown.
NOTE: Neither option is necessary when MMM_MCU_PMU BOM option is selected.



I2C Connections

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

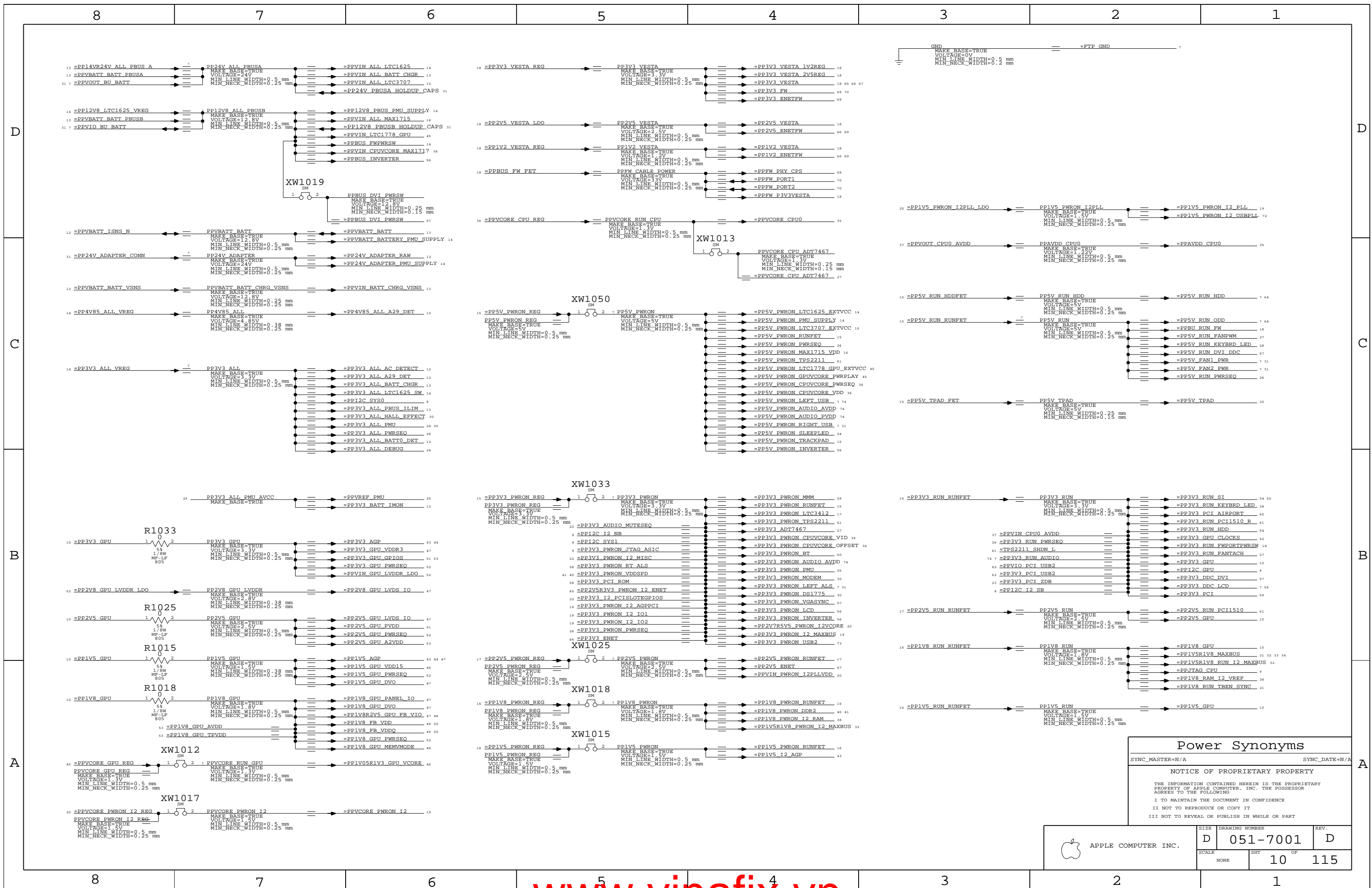
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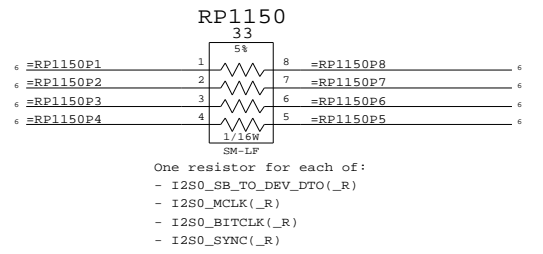
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

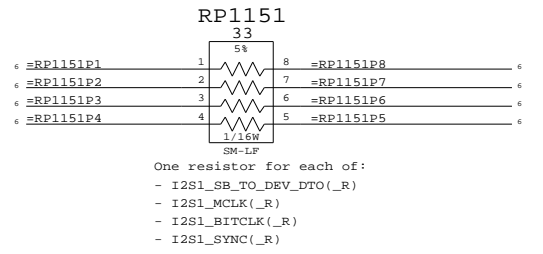
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7001	D
SCALE	NONE	SHT	OF
		8	115



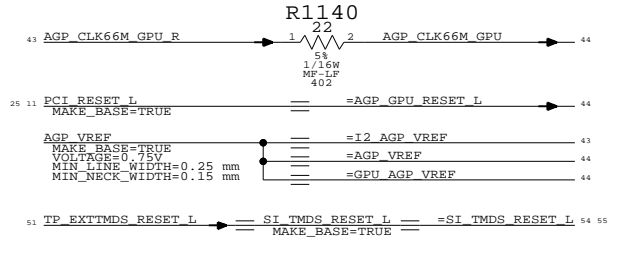
I2S0 Series Rs



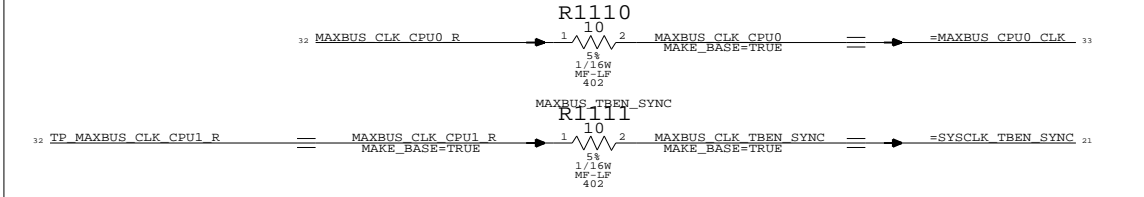
I2S1 Series Rs



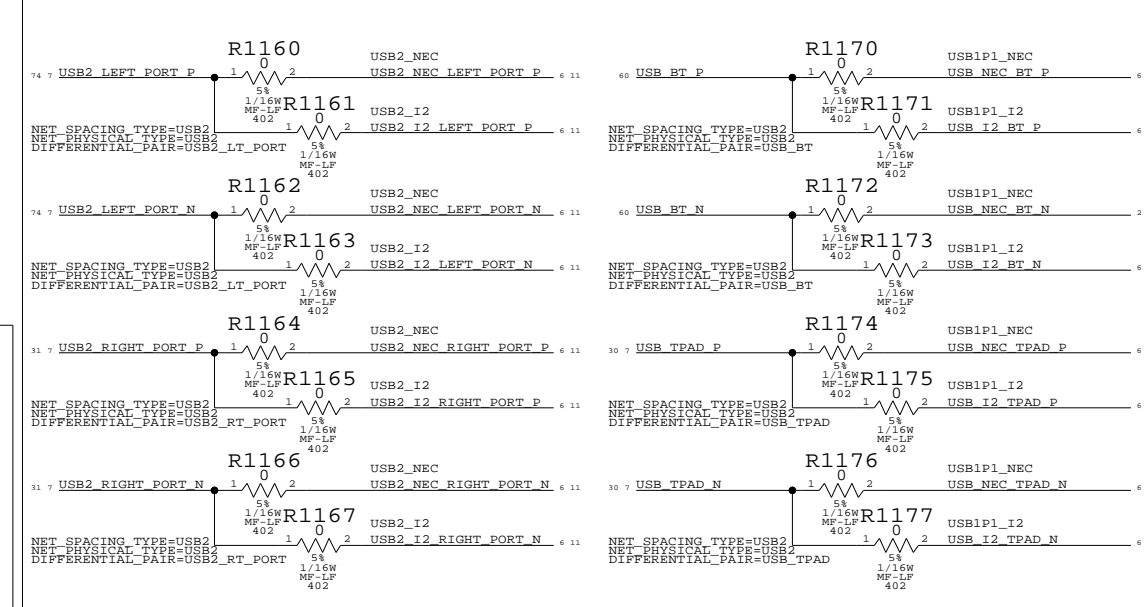
GPU



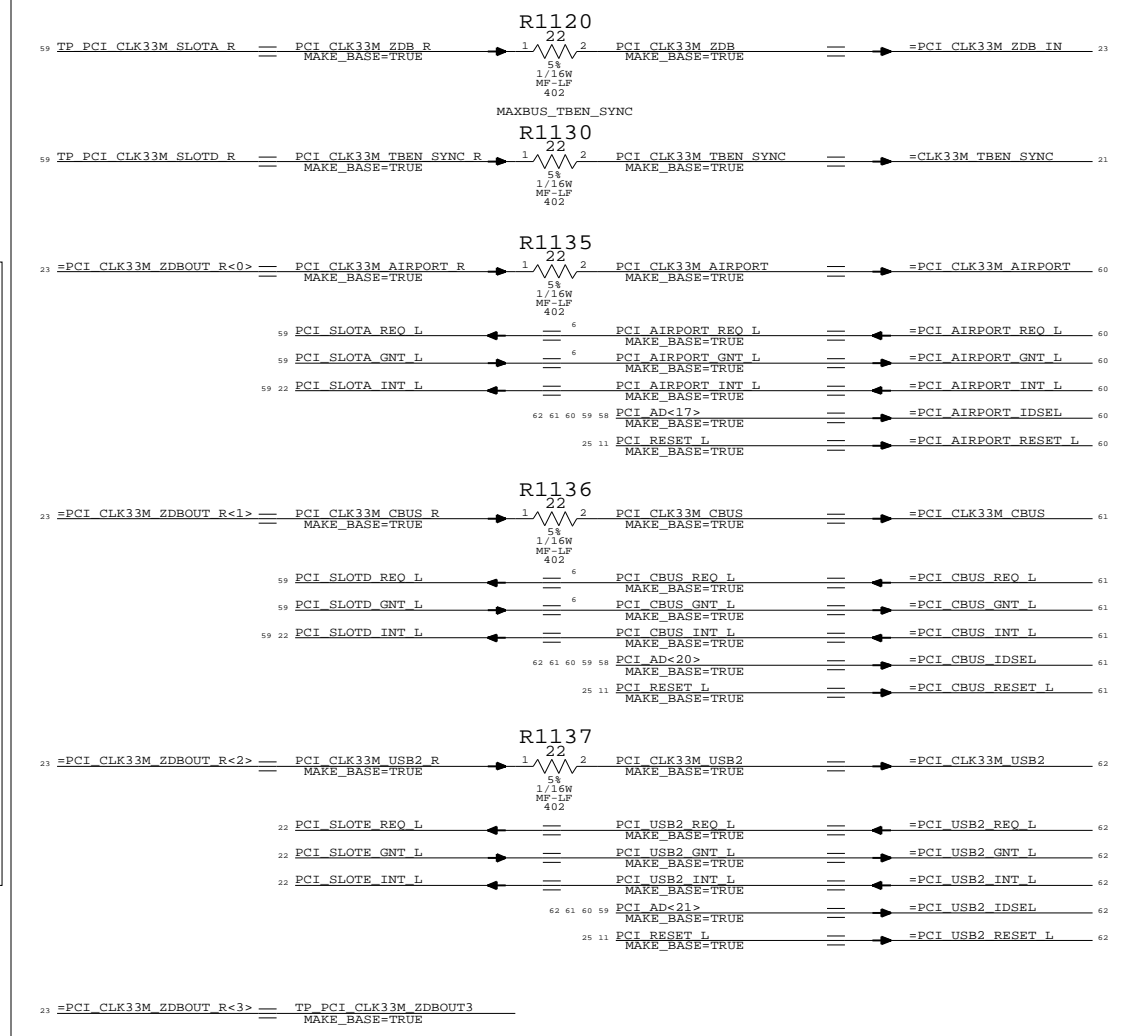
CPU Clocks



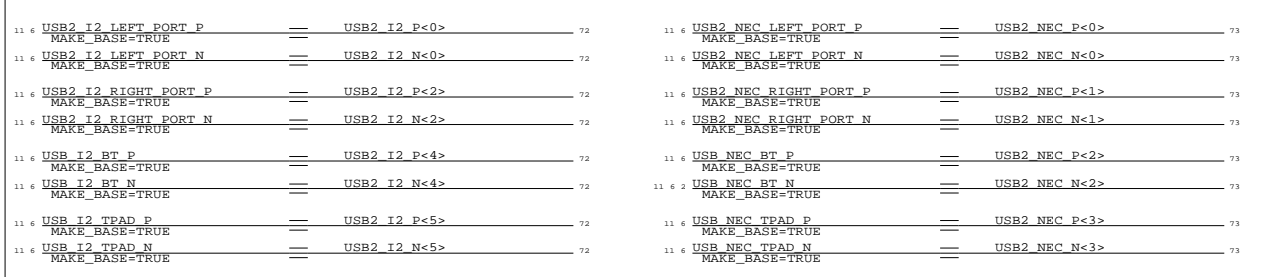
USB Controller Mux



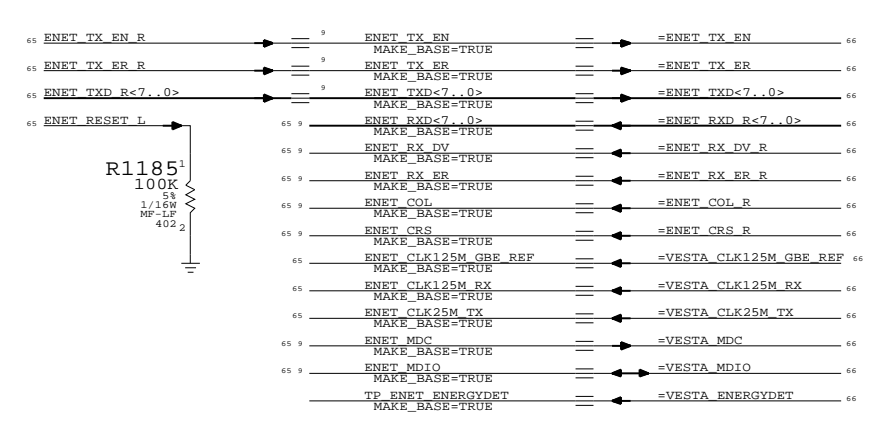
PCI



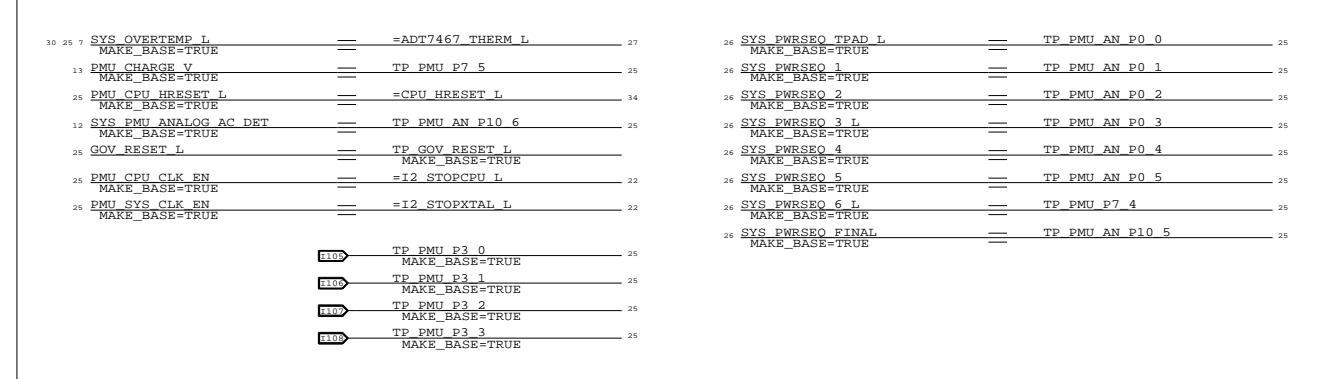
USB Port Assignments



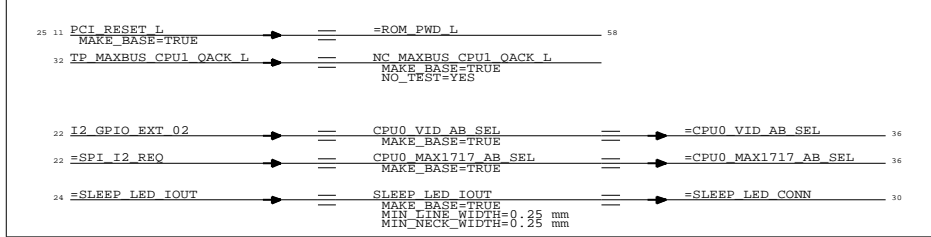
Vesta Ethernet



PMU Connections



MISC



Signal Synonyms

SYNC_MASTER=N/A SYNC_DATE=N/A

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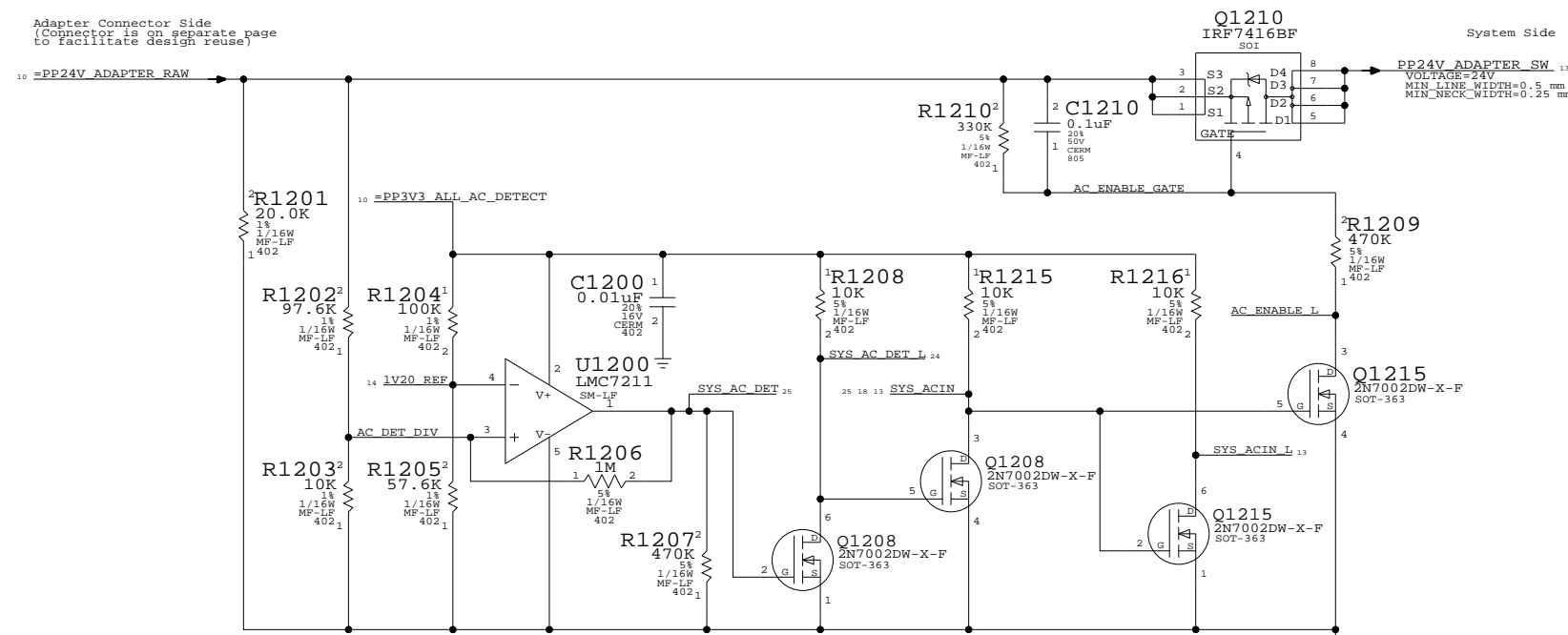
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7001	D
SCALE	SHEET	OF	
NONE	11	115	

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
PP3V	THERM	THERM	BATTERY_ISNS
PP3V	THERM	THERM	BATTERY_ISNS

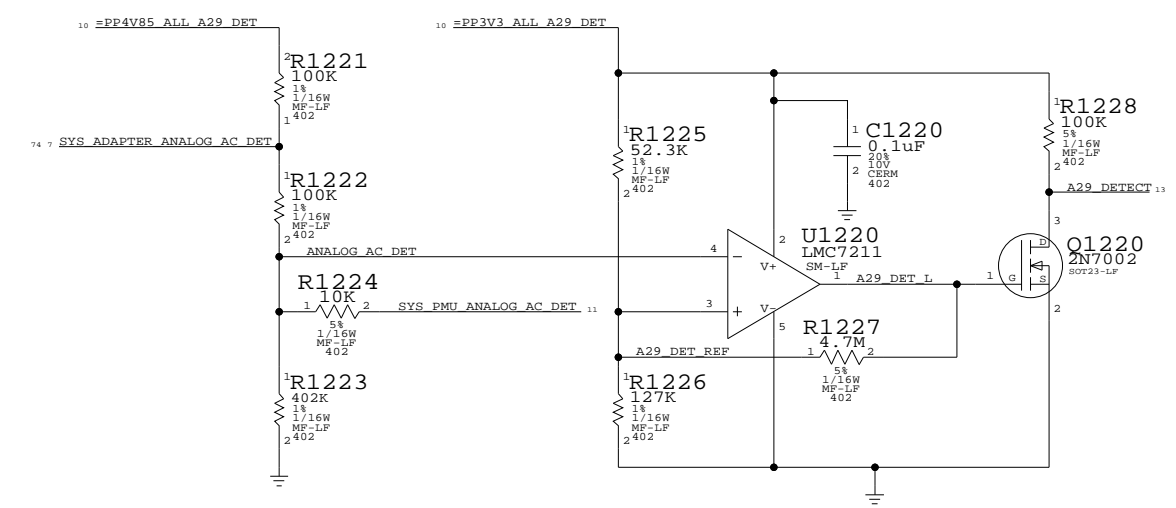
ADAPTER INPUT/INRUSH LIMITER

Adapter Connector Side
(Connector is on separate page to facilitate design reuse)



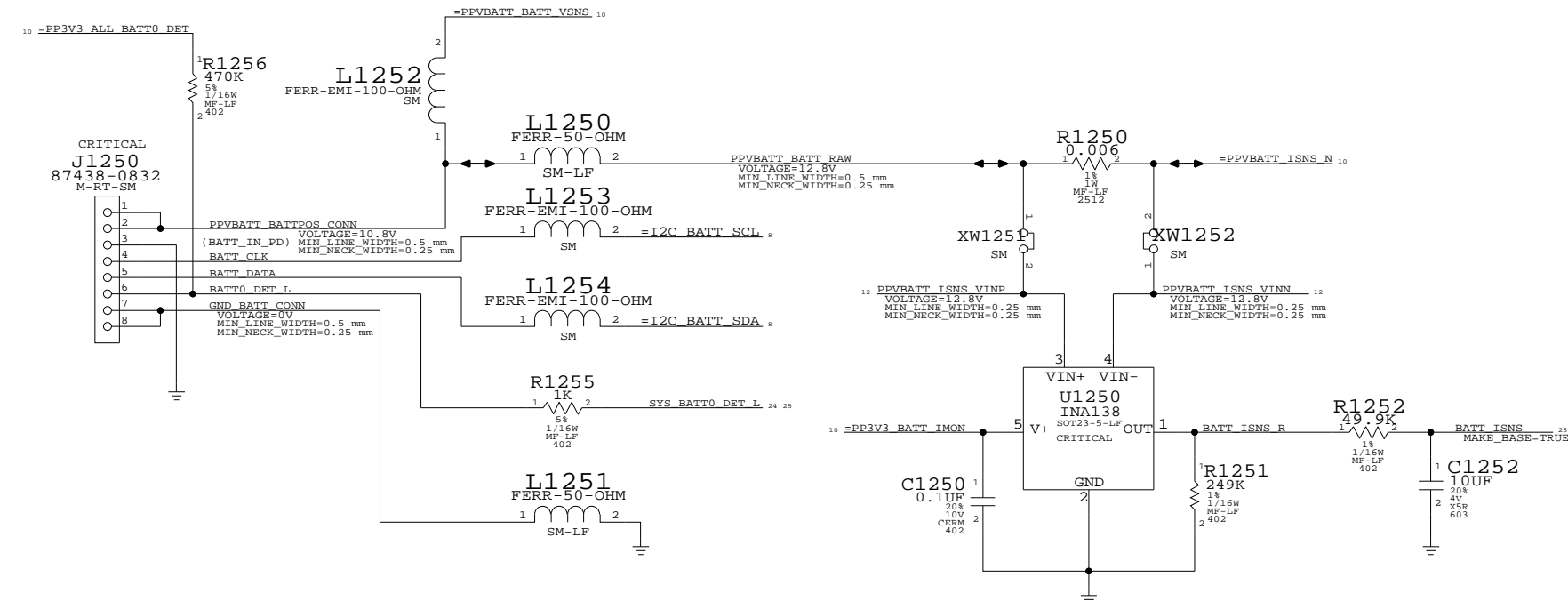
GREATER THAN 13.1V DETECT
SYS AC_DET indicates adapter presence. SYS ACIN is code-controlled signal to enable use of AC in system. Q1208 ensures SYS ACIN goes low as soon as SYS AC_DET goes low. Therefore, hardware immediately disables the AC upon removal but only software can enable AC after detection by the PMU.

A29 ADAPTER DETECTION



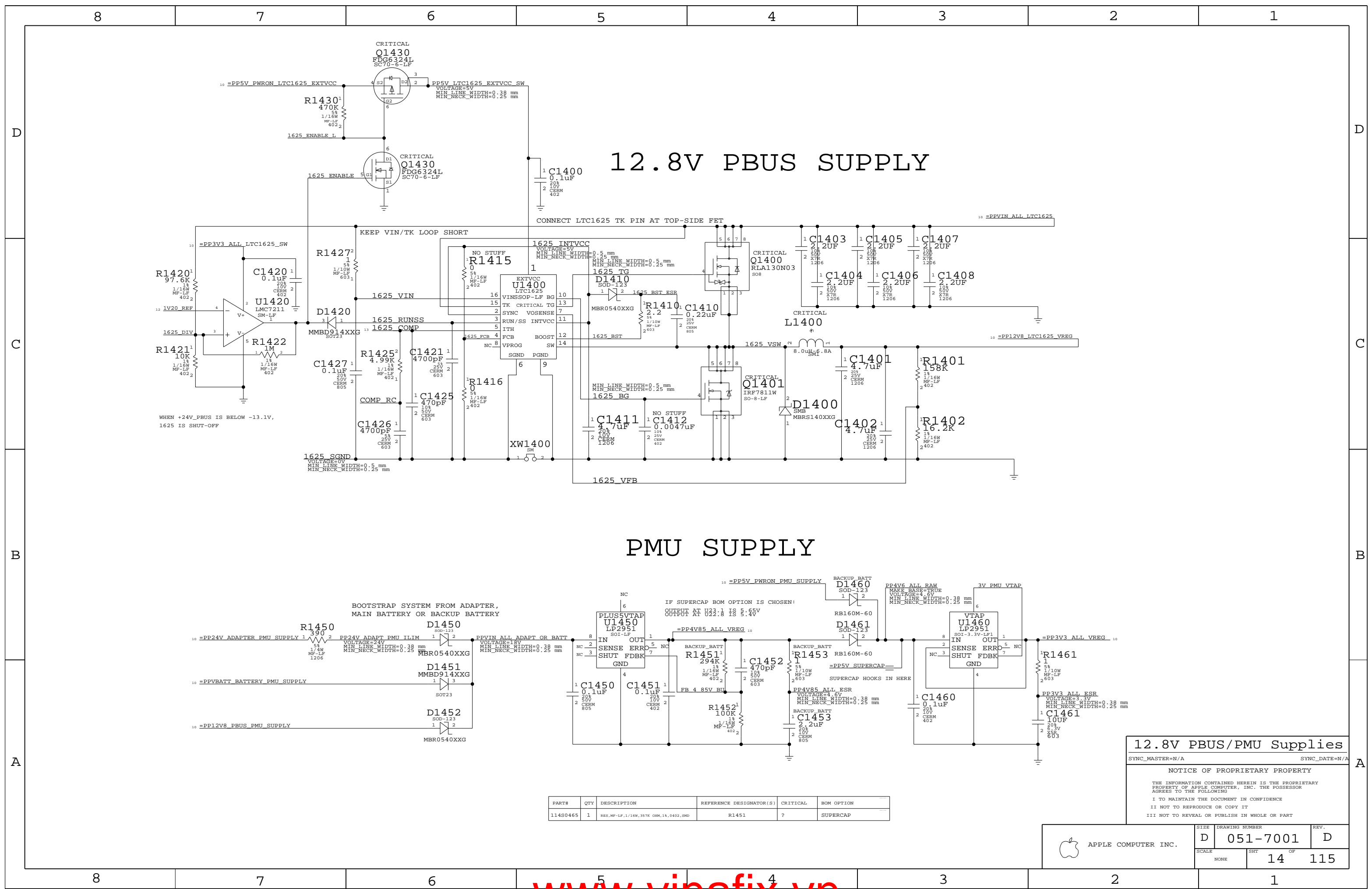
ADAPTER IDS		
ADAPTER	ID RANGE	PIN VOLTAGE
Q11 (65W)	1.65-2.31V	2.007-2.066V
A29 (45W)	2.31-2.97V	2.558-2.661V
AIRLINE	0.33-0.99V	0.589-0.663V

BATTERY INPUT/CURRENT SENSE



Power Inputs
 SYNC_MASTER=N/A SYNC_DATE=N/A
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	D	051-7001	D
SCALE	SHT	OF	REV.
NONE	12	115	



12.8V PBUS SUPPLY

PMU SUPPLY

12.8V PBUS/PMU Supplies

SYNC_MASTER=N/A SYNC_DATE=N/A

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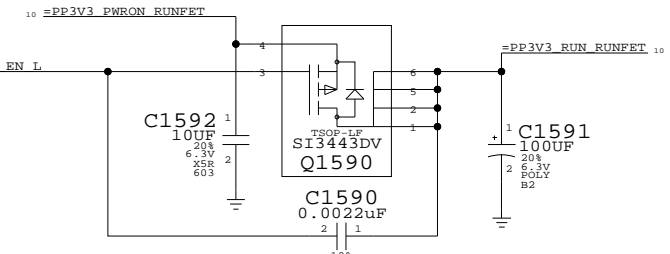
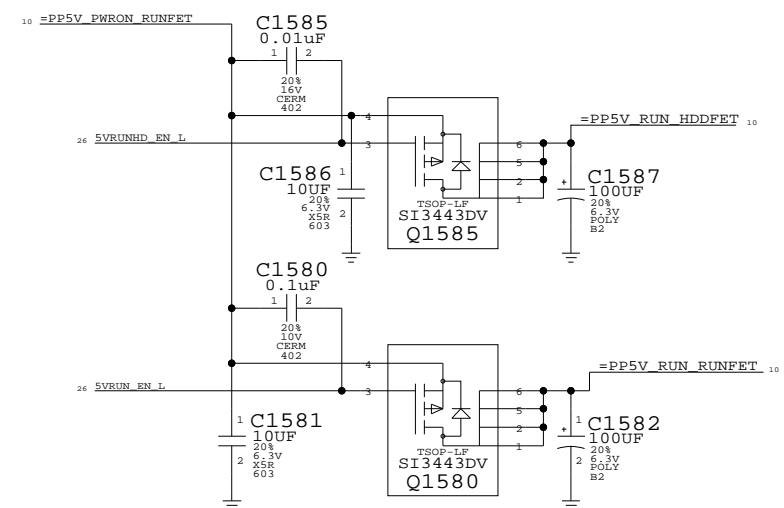
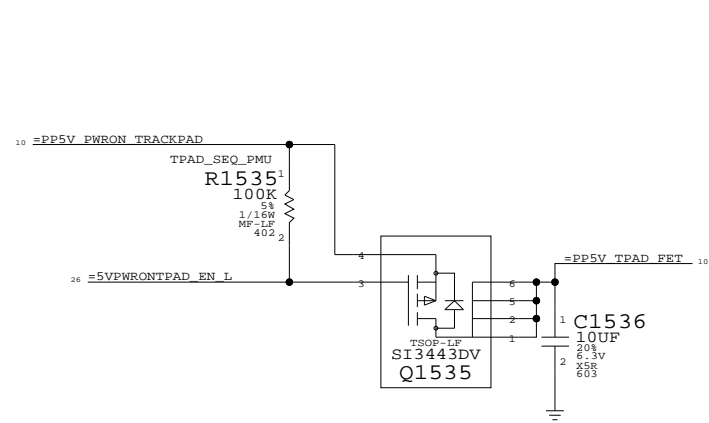
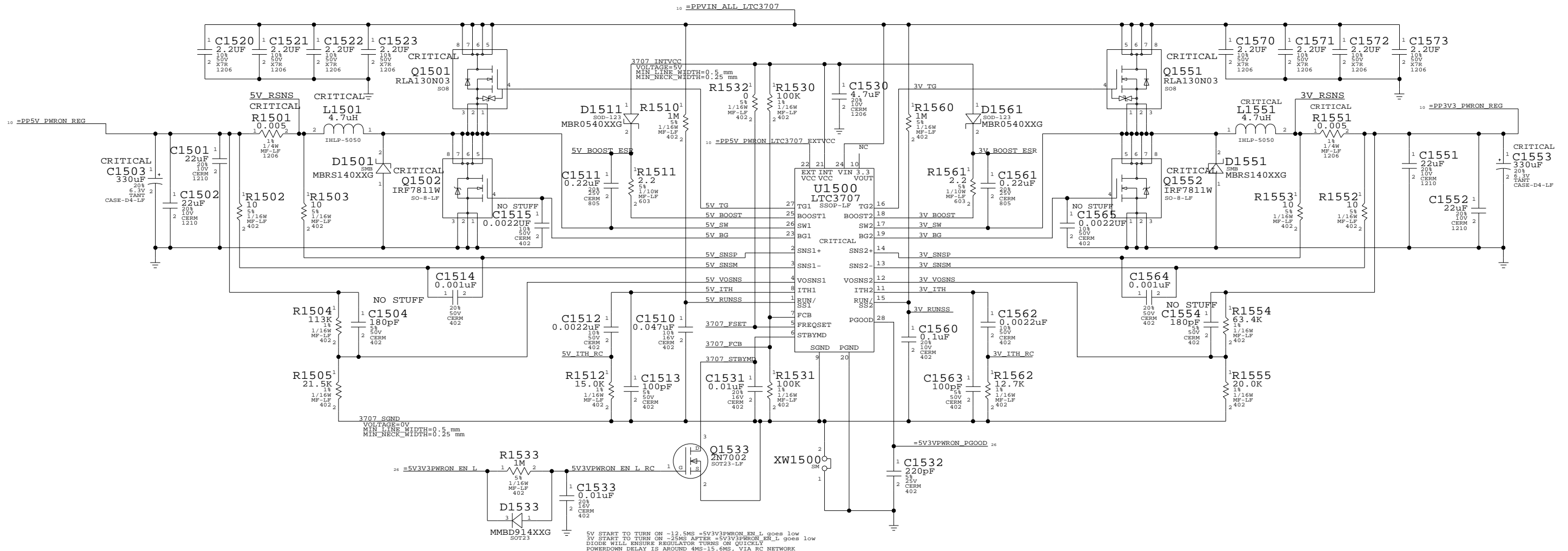
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0465	1	RES,MP-LP,1/16W,357K OHM,1%,0402,SMD	R1451	?	SUPERCAP

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7001	D
SCALE	NONE	SHT OF	14 OF 115

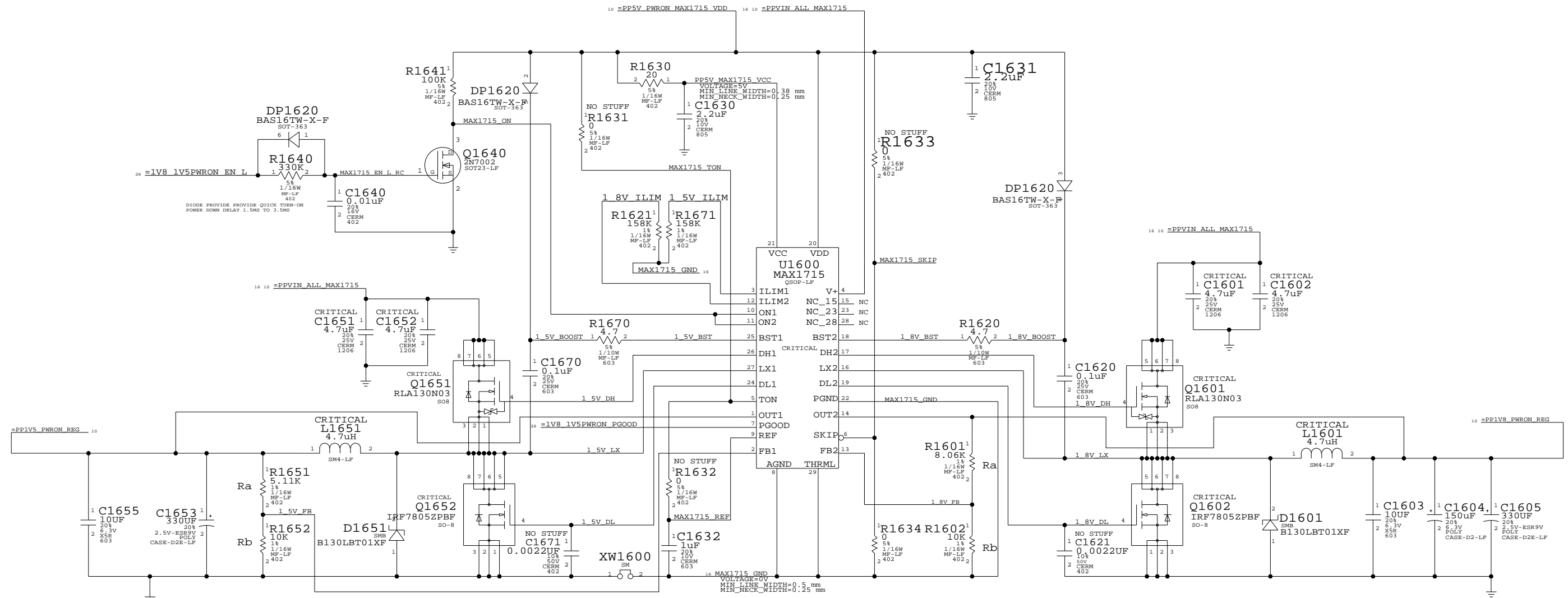
3.3V/5V SWITCHER



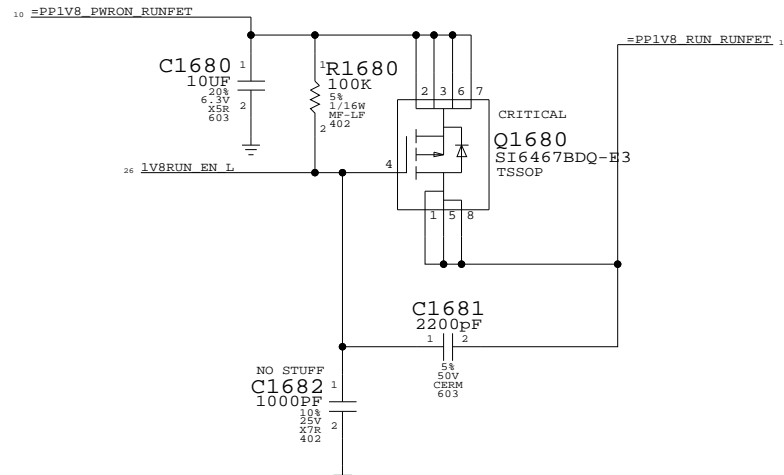
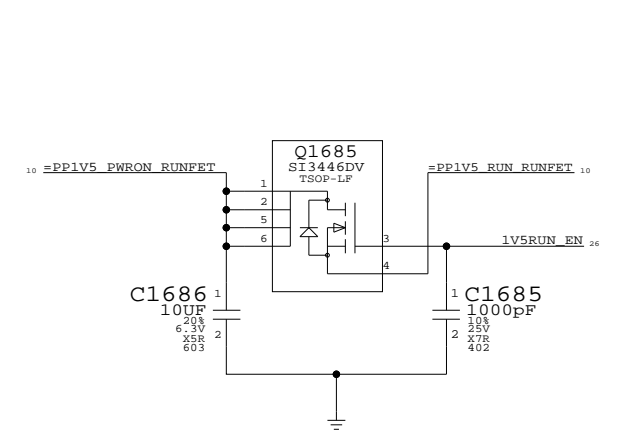
5V/3.3V Supplies
 SYNC_MASTER=N/A SYNC_DATE=N/A
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	D	051-7001	D
SCALE	SHT	OF	REV.
NONE	15	115	

1.5V/1.8V SWITCHER



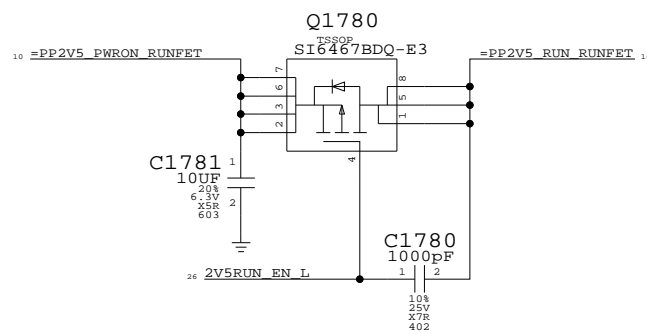
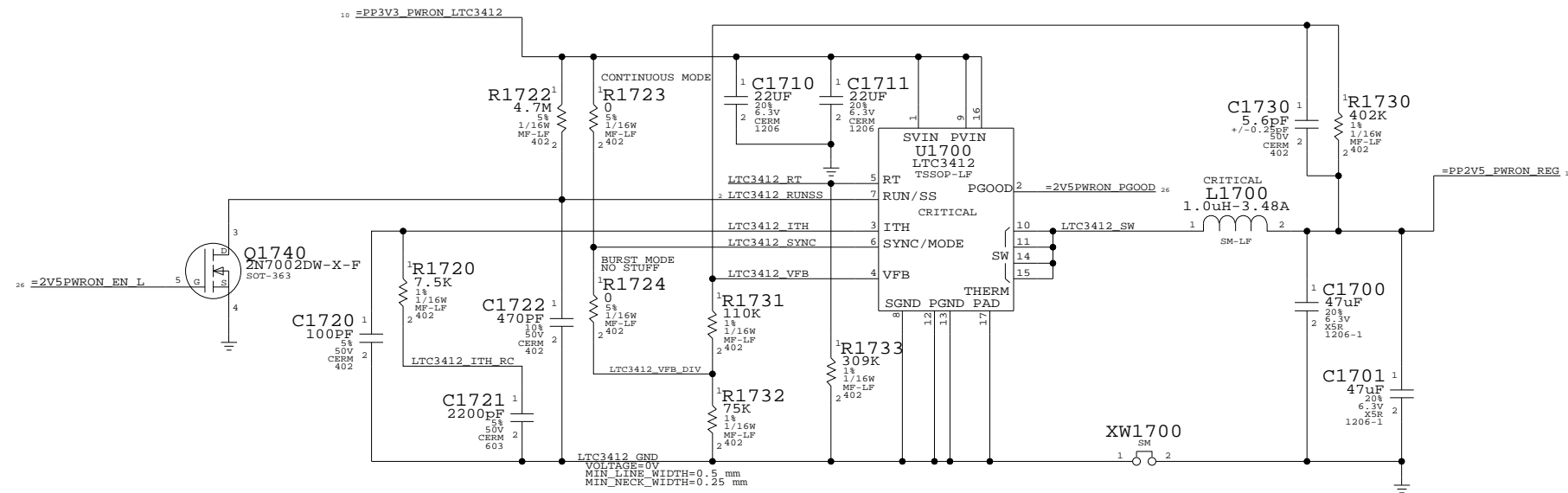
$$V_{out} = 1.0V * (1 + R_a/R_b)$$



1.8V/1.5V Supplies
 SYNC_MASTER=N/A SYNC_DATE=N/A
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7001	D
SCALE	SHT	OF	
NONE	16	115	

2.5V SWITCHER



2.5V Supply

SYNC_MASTER=N/A SYNC_DATE=N/A

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7001	D
SCALE	NONE	SHT OF	17 OF 115

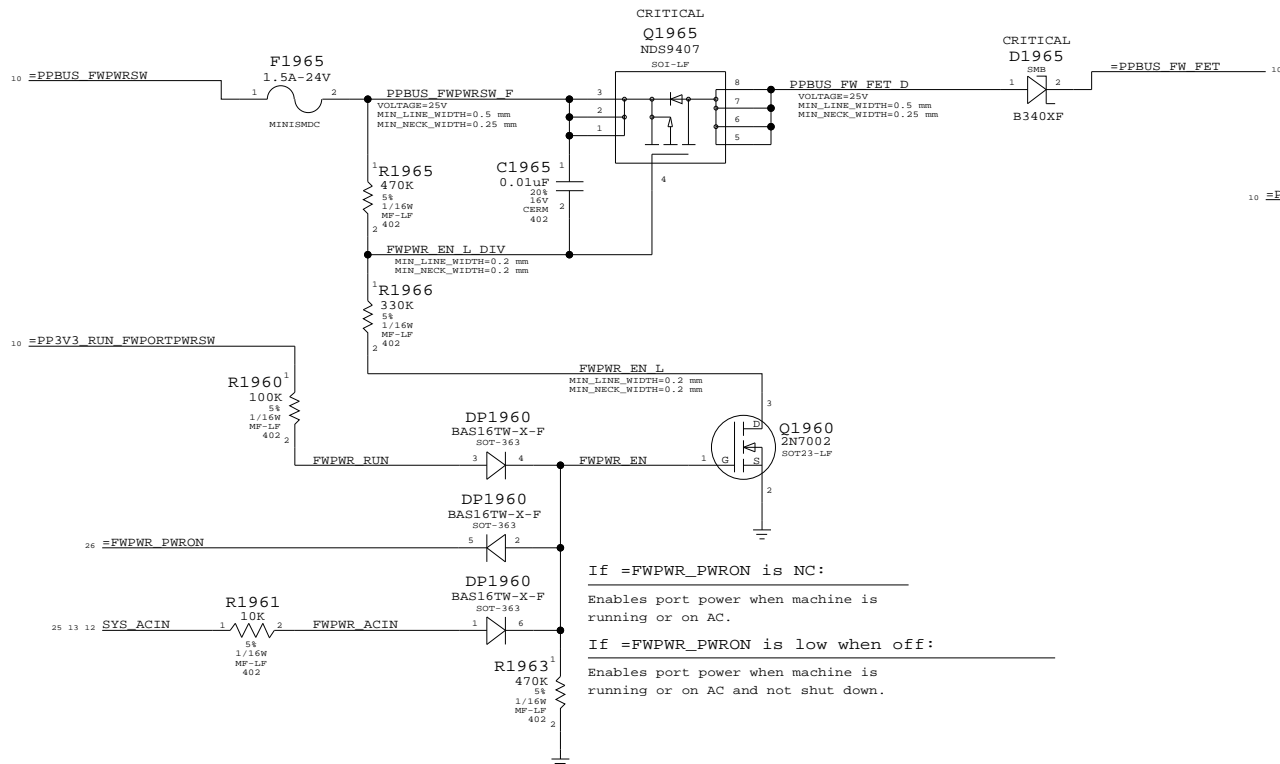
Page Notes

Power aliases required by this page:
 - =PPBUS_FW (system supply for bus power)
 - =PPBUS_RUN_FW (backup PHY power)
 - =PP3V3_RUN_FWPORTFWRWSW

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - VESTALV2_BURST / VESTALV2_PULSE
 Controls operating mode of Vesta 1.2V regulator. If both options are off the regulator will be in continuous mode.

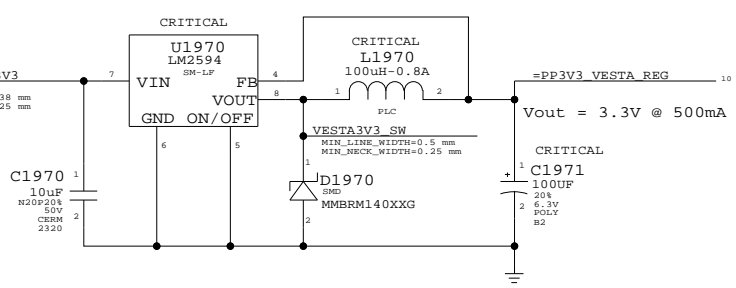
Port Power Switch



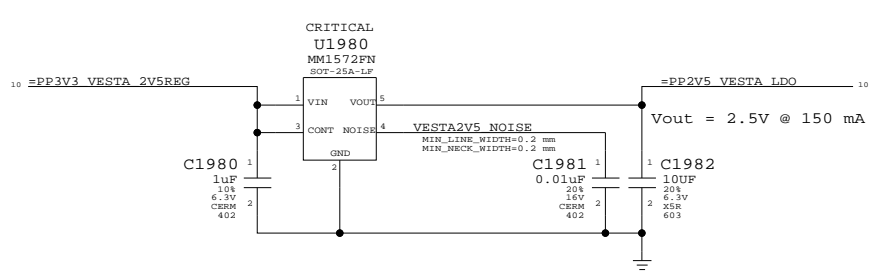
If =FWPWR_PWRON is NC:
 Enables port power when machine is running or on AC.

If =FWPWR_PWRON is low when off:
 Enables port power when machine is running or on AC and not shut down.

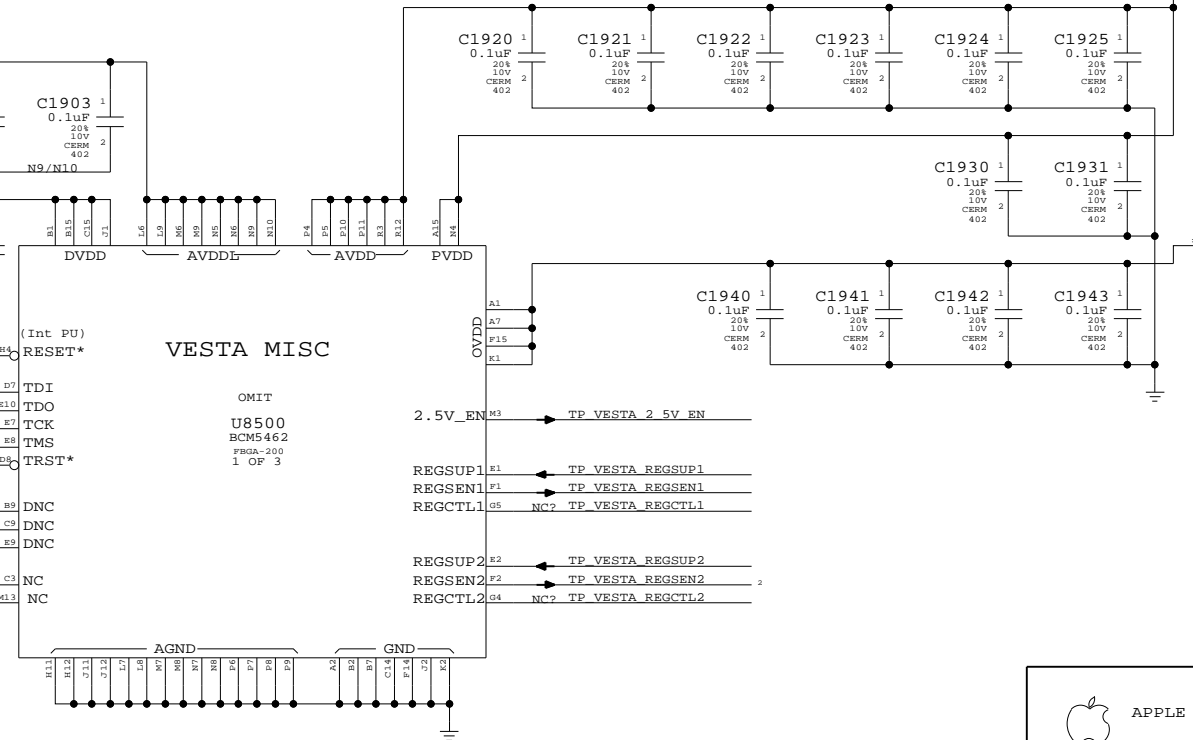
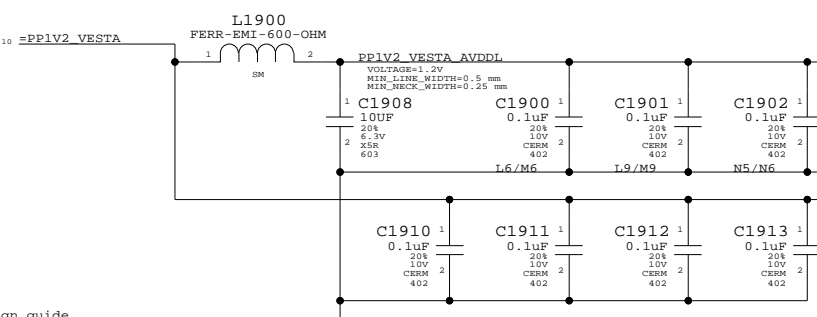
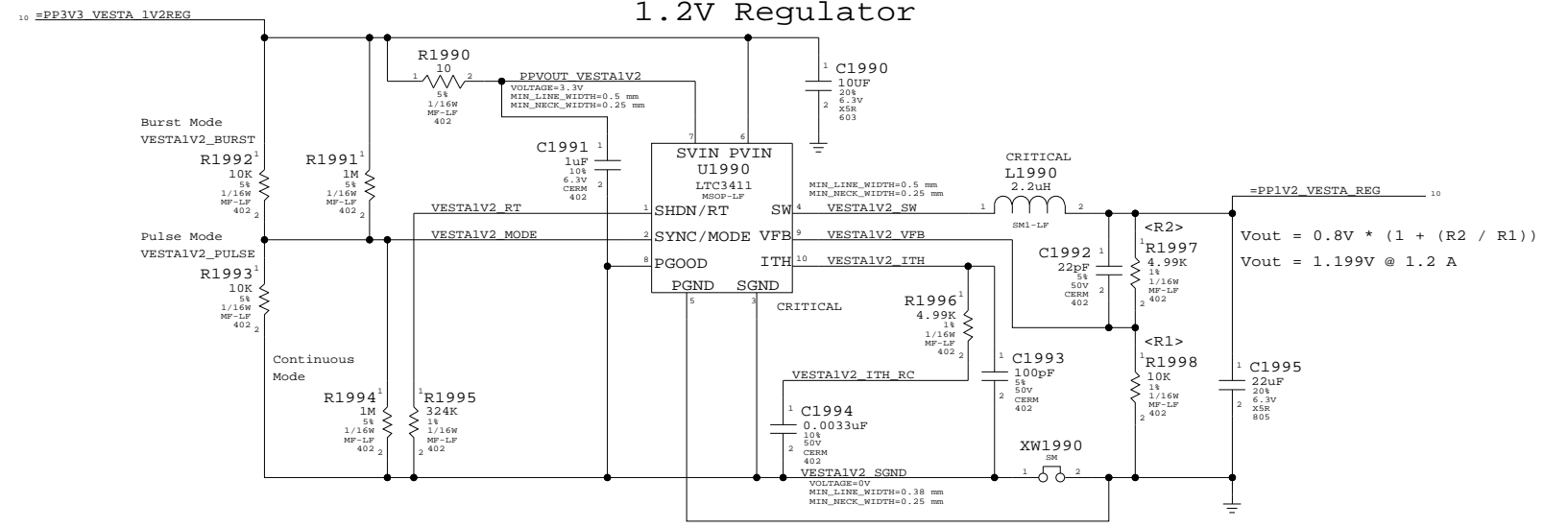
3.3V Regulator



2.5V LDO



1.2V Regulator



Vesta Power & Misc

SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-7001	D
SCALE	SHEET	OF	
NONE	19	115	

Page Notes

Power aliases required by this page:
 - =PPVCORE_PWRON_I2
 - =PP1V5_PWRON_I2_PLL
 - =PP3V3_PWRON_I2_IO1
 - =PP3V3_PWRON_I2_IO2
 - =PP3V3_PWRON_I2_AGPPCI
 - =PP3V3_PWRON_I2_MAXBUS

NOTE: The four 3.3V rails are meant to be aliased together. They are called out separately for test purposes.
 NOTE: When these four rails are not aliased together, make sure there is at least one 10uF cap per rail.

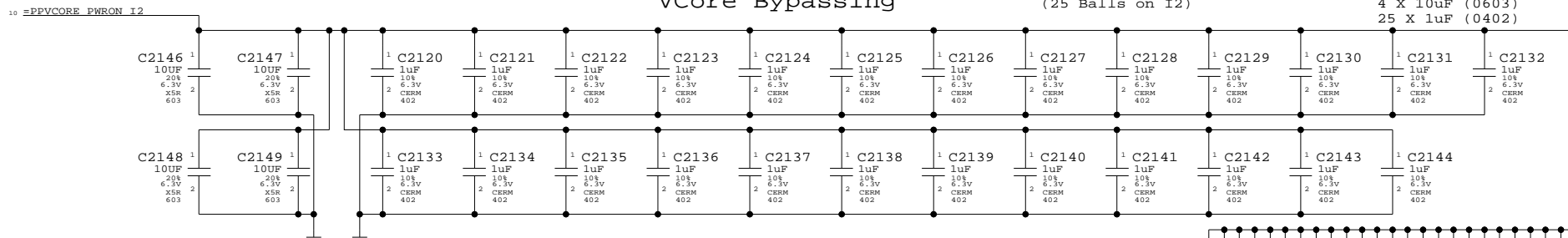
Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

VCore Bypassing

(25 Balls on I2)

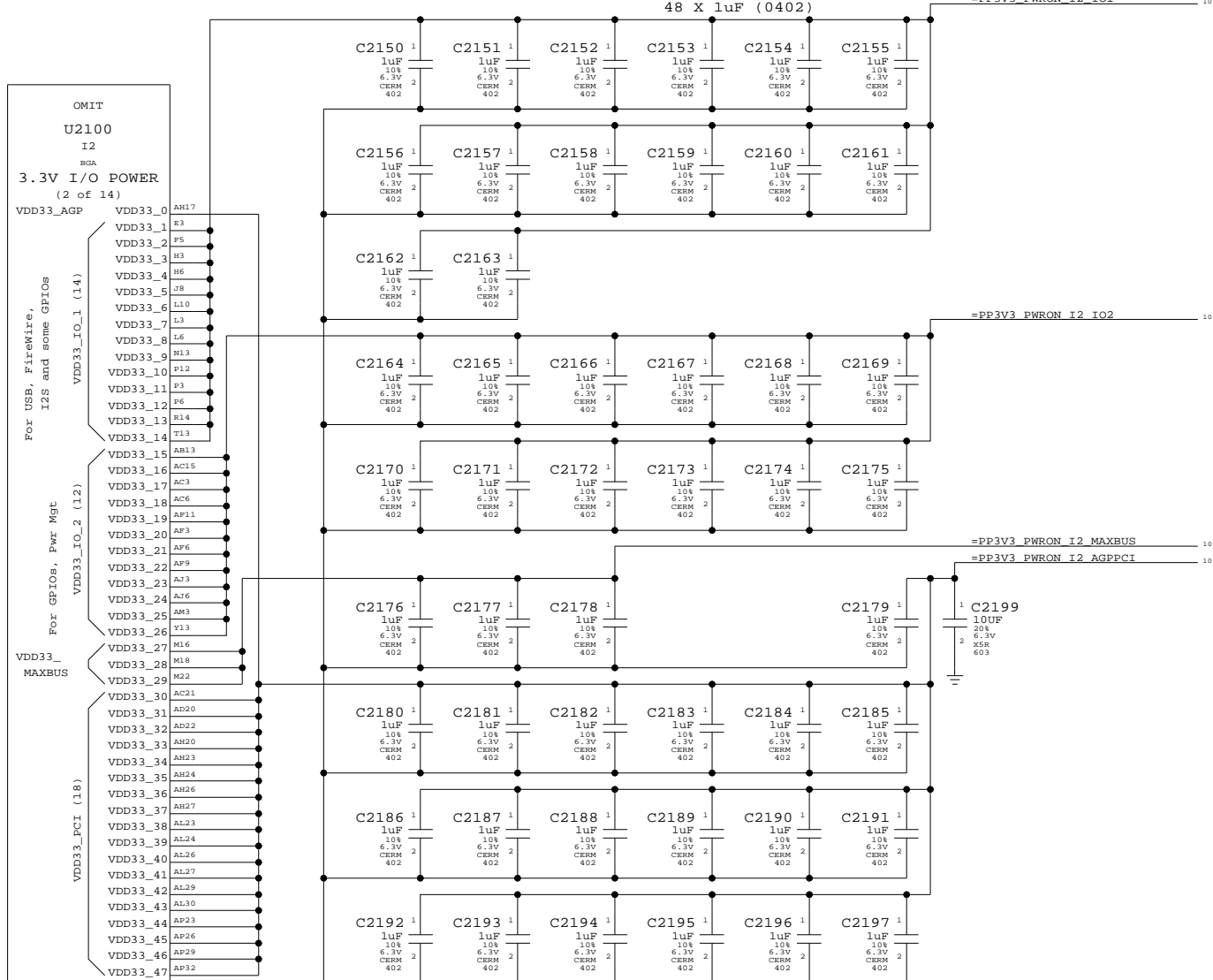
4 X 10uF (0603)
 25 X 1uF (0402)



3.3V I/O DECOUPLING

(48 Balls on I2)

1 X 10uF (0603)
 48 X 1uF (0402)



=PP1V5_PWRON_I2_PLL

=PP3V3_PWRON_I2_IO1

=PP3V3_PWRON_I2_IO2

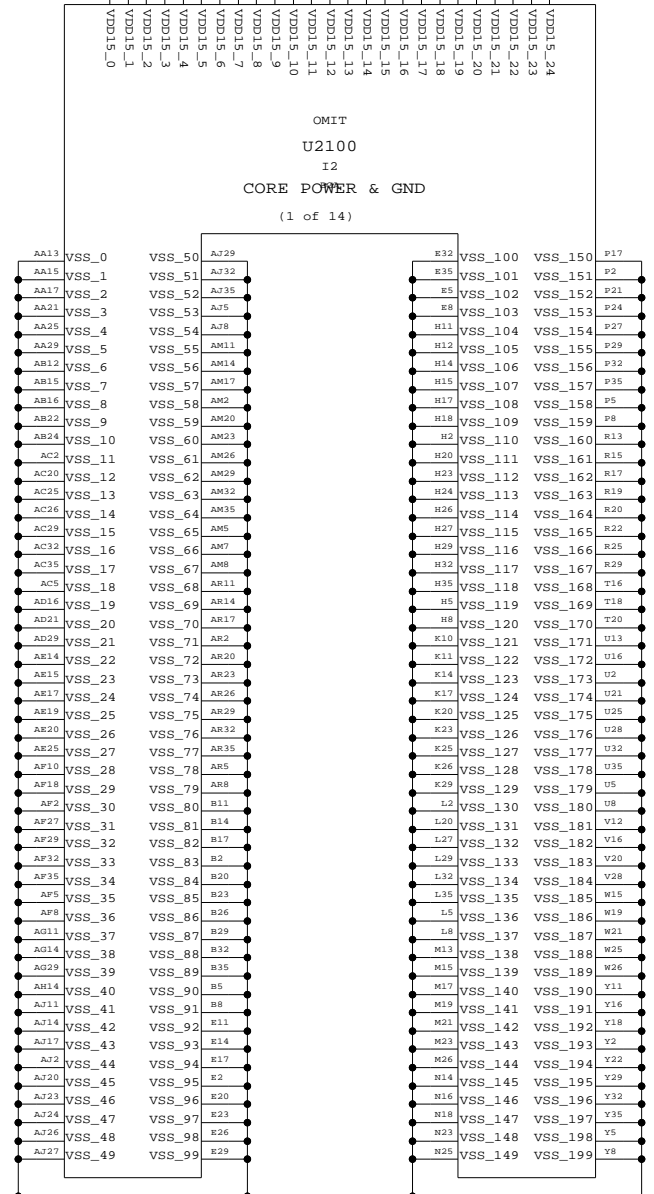
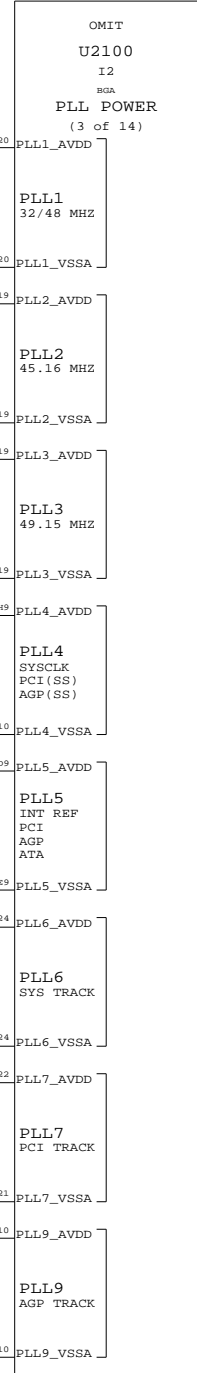
=PP3V3_PWRON_I2_MAXBUS

=PP3V3_PWRON_I2_AGPPCI

=PPVCORE_PWRON_I2

=PP3V3_PWRON_I2_MAXBUS

=PP3V3_PWRON_I2_AGPPCI



I2 Power
 SYNC_MASTER=N/A SYNC_DATE=N/A
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	D	051-7001	D
SCALE	SHEET	OF	
NONE	21	115	

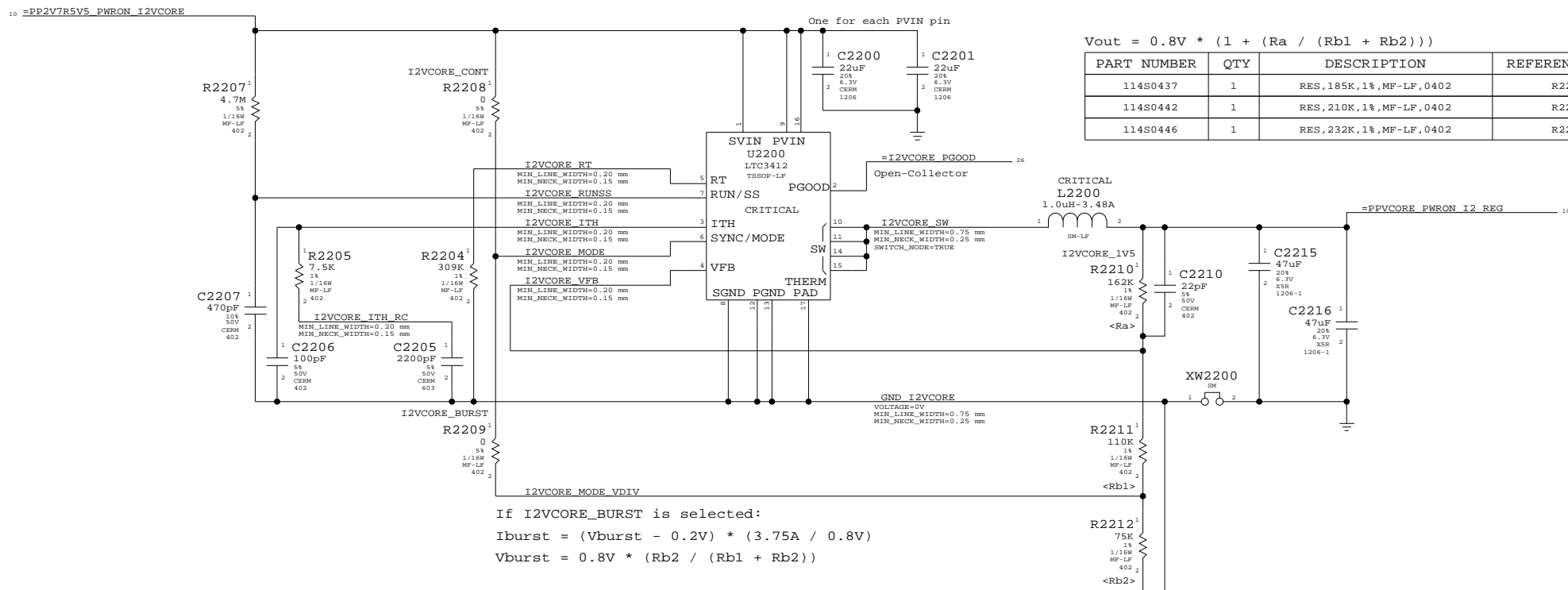
Page Notes

Power aliases required by this page:
 - =PP2V7R5V5_PWRON_I2VCORE
 - =PPVCORE_PWRON_I2_REG
 - =PPVIN_PWRON_I2PLLVD
 - =PP1V5_PWRON_I2PLLVD_LDO

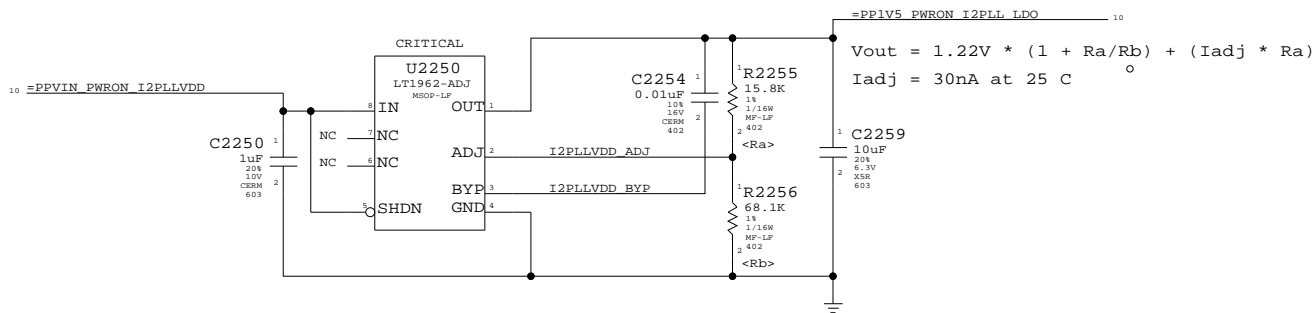
Signal aliases required by this page:
 - =I2VCORE_PGOOD

BOM options provided by this page:
 - I2VCORE_CONT / I2VCORE_BURST
 Selects between forced continuous and burst mode for LTC3412 regulator.
 - I2VCORE_XVX
 Selects appropriate resistor for the indicated LTC3412 output voltage.

I2 VCore Regulator



I2 PLL LDO



I2 Power Supplies

SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-7001	D
SCALE	SHT	OF	REV.
NONE	22	115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
I2S0_DTT	I2S	128	128	I2S0_DEV_TO_SB_DTT
I2S0_DTO	I2S	128	128	I2S0_SB_TO_DEV_DTO_R
I2S0_MCLK	I2S	128	128	I2S0_MCLK_R
I2S0_BITCLK	I2S	128	128	I2S0_BITCLK_R
I2S0_SYNC	I2S	128	128	I2S0_SYNC_R
I2S1_DTT	I2S	128	128	I2S1_DEV_TO_SB_DTT
I2S1_DTO	I2S	128	128	I2S1_SB_TO_DEV_DTO_R
I2S1_MCLK	I2S	128	128	I2S1_MCLK_R
I2S1_BITCLK	I2S	128	128	I2S1_BITCLK_R
I2S1_SYNC	I2S	128	128	I2S1_SYNC_R
I2_CLK18M_XOUT	XTAL	XTAL	XTAL	I2_CLK18M_XOUT
I2_CLK18M_XOUT	XTAL	XTAL	XTAL	I2_CLK18M_XOUT
I2_CLK18M_XIN	XTAL	XTAL	XTAL	I2_CLK18M_XIN

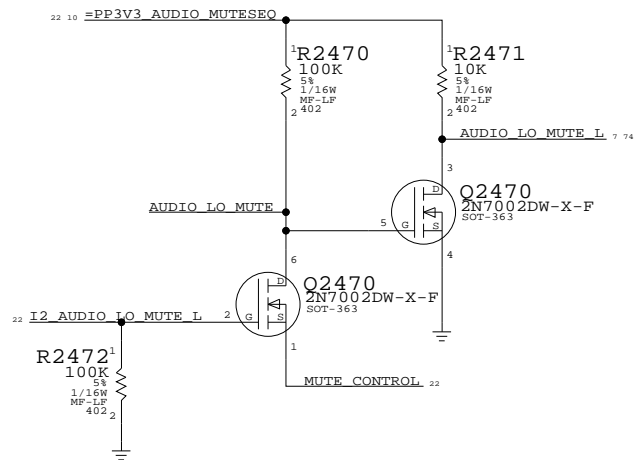
Page Notes

Power aliases required by this page:
 - =PP3V3_PWRON_I2_GPIO
 - =PP3V3_I2_PCISLOTGPIO (PWRON or PCI)
 Should be same as =PP3V3_PCI if slot E is used, or else =PP3V3_PWRON_I2_GPIO.

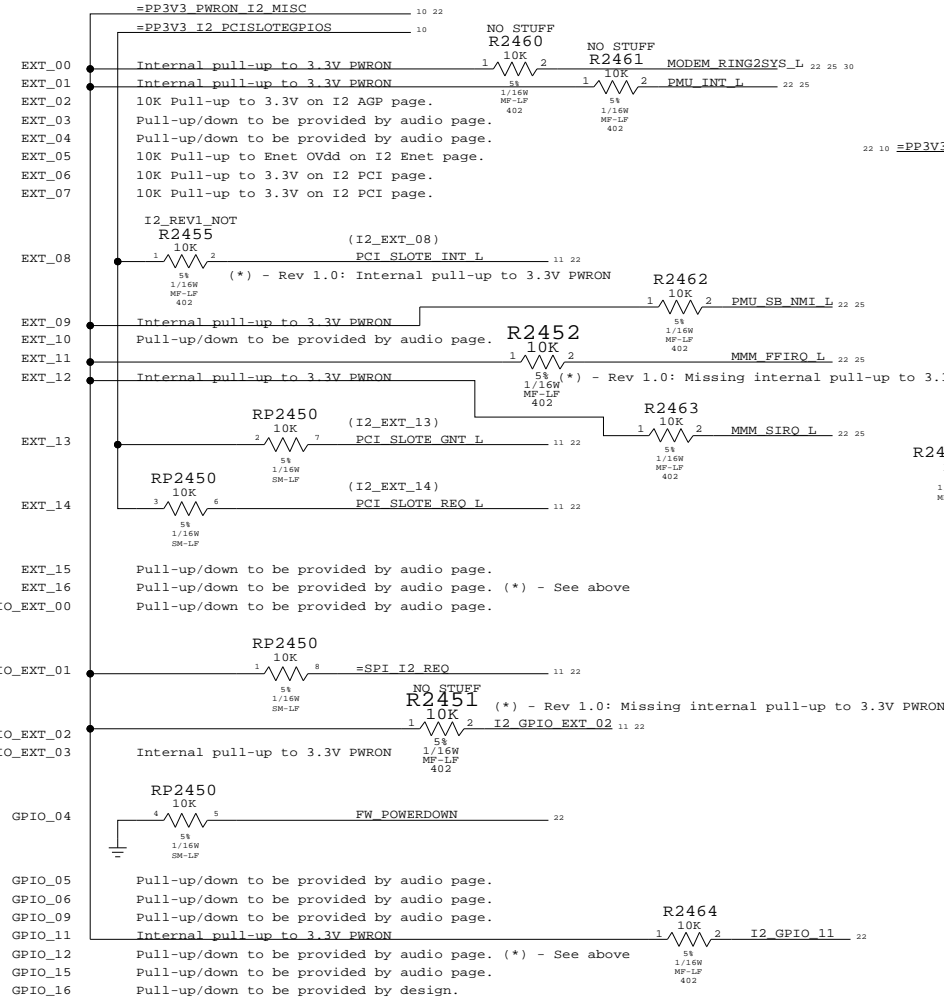
Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - I2_REV1_NOT
 Use for I2 revisions > 1.0

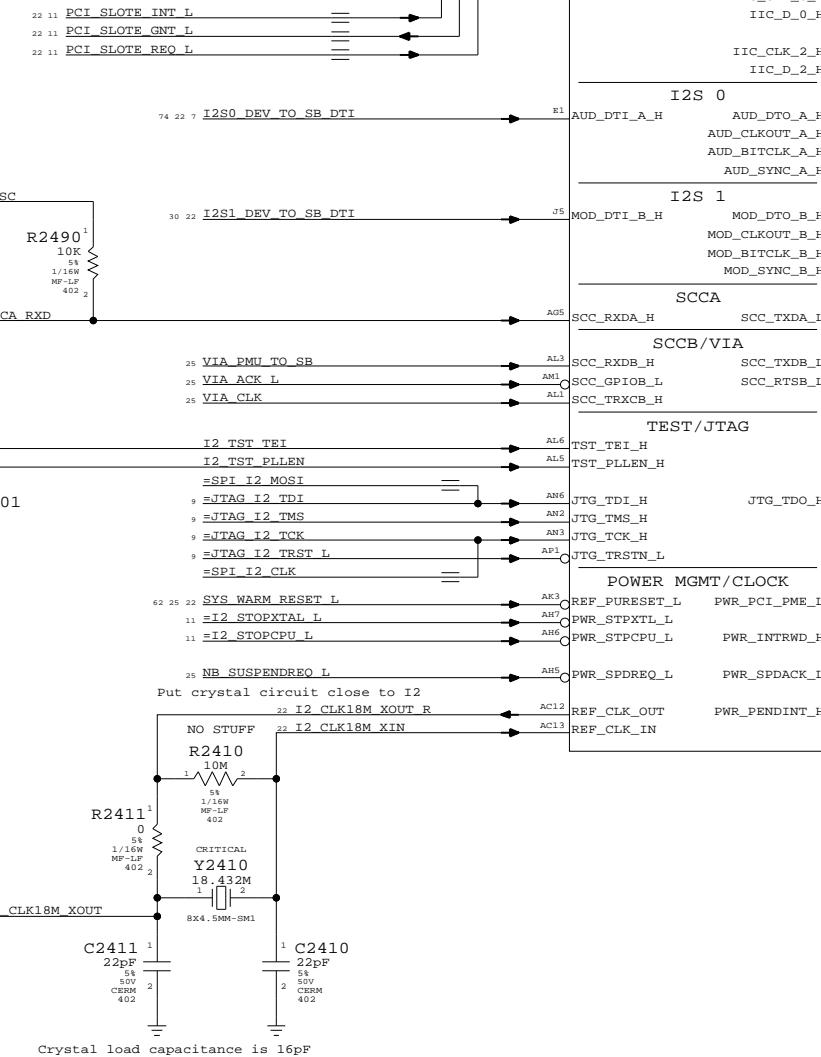
Audio Mute Sequencing
 Prevents mute glitch from reaching audio circuit



GPIO Pull-ups / Pull-downs

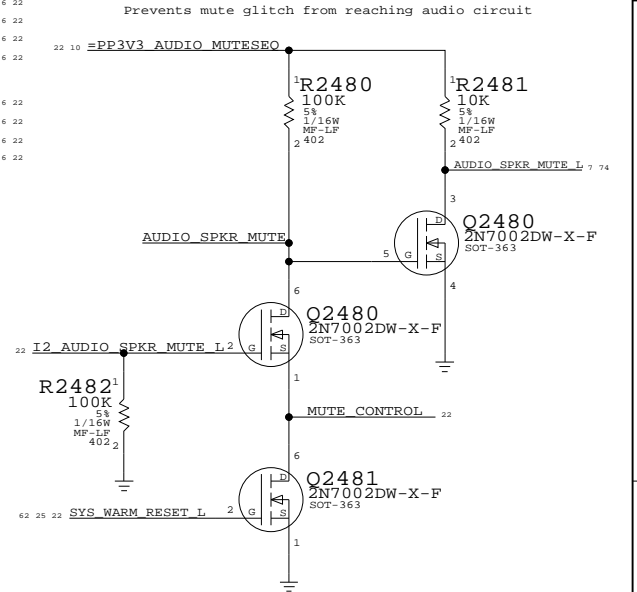


Alternate GPIO Functions
 Use MAKE_BASE to force net name



Pin	Address	MPIC	Int	Int PU?	Alt Func
EXT_00	0x0_0058	46	(0x2E)	Yes	PCI_REQ_2_L
EXT_01	0x0_0059	47	(0x2F)	Yes	
EXT_02	0x0_005A	48	(0x30)	No	
EXT_03	0x0_005B	49	(0x31)	No	
EXT_04	0x0_005C	50	(0x32)	No	
EXT_05	0x0_005D	51	(0x33)	No	
EXT_06	0x0_005E	52	(0x34)	No	
EXT_07	0x0_005F	53	(0x35)	No	
EXT_08	0x0_0060	54	(0x36)	Yes	
EXT_09	0x0_0061	55	(0x37)	Yes	
EXT_10	0x0_0062	56	(0x38)	No	
EXT_11	0x0_0063	57	(0x39)	Yes	
EXT_12	0x0_0064	58	(0x3A)	Yes	
EXT_13	0x0_0065	59	(0x3B)	No	PCI_GNT_2_L
EXT_14	0x0_0066	60	(0x3C)	No	PCI_REQ_2_L
EXT_15	0x0_0067	61	(0x3D)	No	
EXT_16	0x0_0068	62	(0x3F)	Yes	
GPIO_00	0x0_006A	14	(0x0E)	No	
GPIO_01	0x0_006B	15	(0x0F)	No	SPIREQ
GPIO_02	0x0_006C	16	(0x10)	Yes	PCI_GNT_2_L
GPIO_03	0x0_006D	17	(0x11)	Yes	
GPIO_04	0x0_006E	N/A		No	
GPIO_05	0x0_006F	N/A		No	
GPIO_06	0x0_0070	N/A		No	
GPIO_09	0x0_0073	N/A		No	
GPIO_11	0x0_0075	N/A		Yes	
GPIO_12	0x0_0076	N/A		Yes	
GPIO_15	0x0_0079	N/A		No	
GPIO_16	0x0_007A	N/A		No	

Audio Mute Sequencing
 Prevents mute glitch from reaching audio circuit



I2 Miscellaneous

SYNC_MASTER=N/A SYNC_DATE=N/A

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	NONE	D 051-7001	D
	SHEET	OF	
	24	115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		DIFFERENTIAL_PAIR
	SPACING	PHYSICAL	
PCI_ZDBOUT0	CLOCK	CLOCK	
PCI_ZDBOUT1	CLOCK	CLOCK	
PCI_ZDBOUT2	CLOCK	CLOCK	
PCI_ZDBOUT3	CLOCK	CLOCK	

```

=PCI_CLK33M_ZDB_IN 11 23
=PCI_CLK33M_ZDBOUT_R<0> 11 23
=PCI_CLK33M_ZDBOUT_R<1> 11 23
=PCI_CLK33M_ZDBOUT_R<2> 11 23
=PCI_CLK33M_ZDBOUT_R<3> 11 23

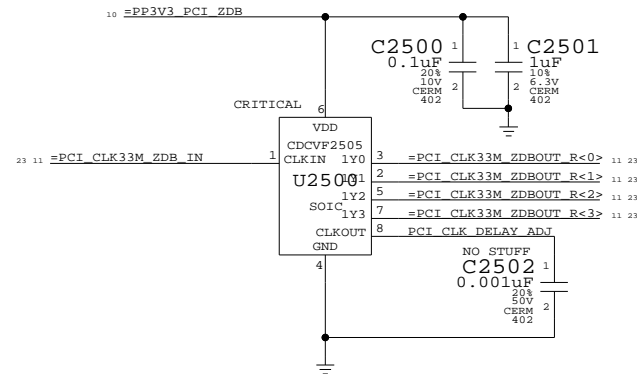
```

Page Notes

Power aliases required by this page:
 - =PP3V3_PWRON_I2_GPIO
 - =PP3V3_I2_PCISLOTGPIO (PWRON or PCI)
 Should be same as =PP3V3_PCI if slot E is used, or else =PP3V3_PWRON_I2_GPIO.

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - I2_REV1_NOT
 Use for I2 revisions > 1.0



PCI Clock Buffer

SYNC_MASTER=N/A SYNC_DATE=N/A

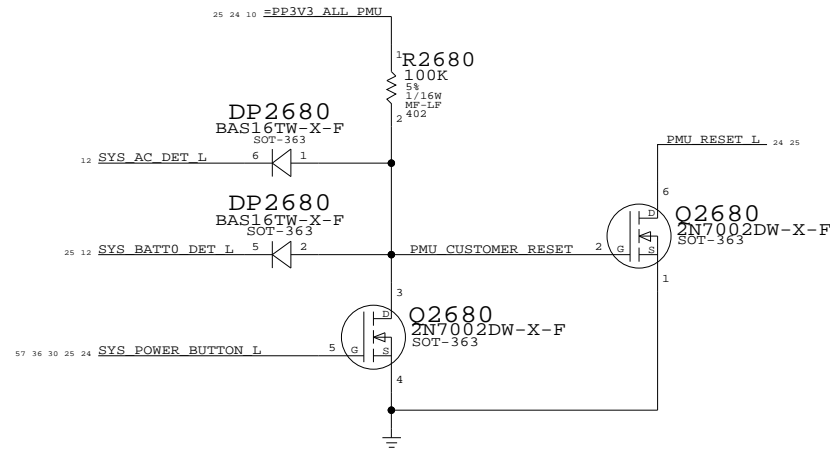
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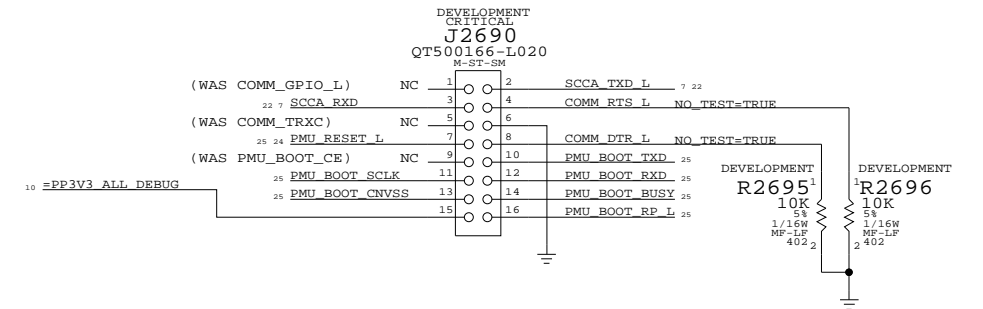
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7001	D
SCALE	SHT	OF	REV.
NONE	25	115	

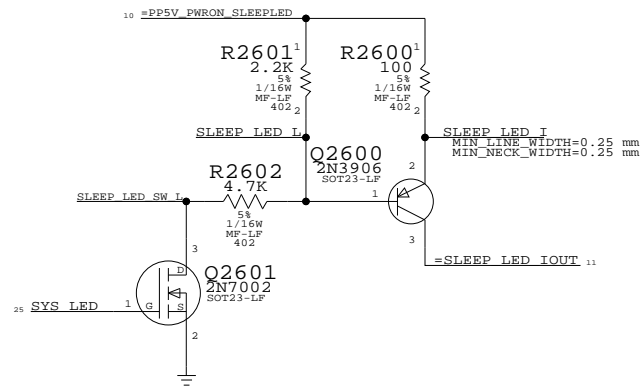
PMU RESET CIRCUIT



SERIAL DEBUG INTERFACE

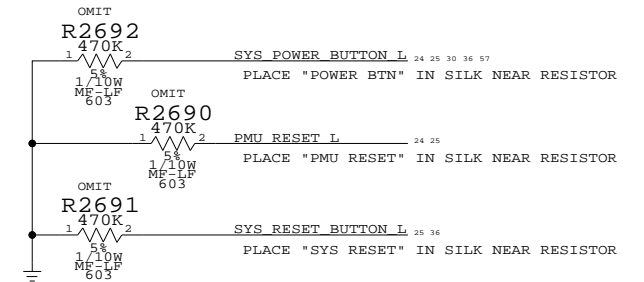


SLEEP LED

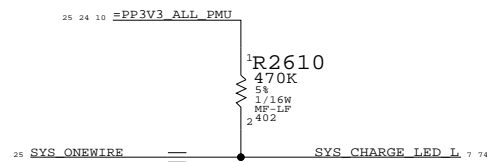


DEBUGGING AIDS

PLACE ON TOP SIDE NEAR FRONT EDGE OF BOARD



CHARGE LED



LEDs/Reset/Debug

SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-7001	D
SCALE	NONE	SHT	OF
		26	115

Power Management Unit

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		DIFFERENTIAL_PAIR	
SPACING	PHYSICAL	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
PP3V3_CLK10M_XTAL	XTAL	XTAL	XTAL		PMU_CLK10M_XIN
PP3V3_CLK10M_XOUT	XTAL	XTAL	XTAL		PMU_CLK10M_XOUT
PP3V3_CLK10M_XOUT_R	XTAL	XTAL	XTAL		PMU_CLK10M_XOUT_R
PP3V3_CLK32K_XTAL	XTAL	XTAL	XTAL		PMU_CLK32K_XIN
PP3V3_CLK32K_XOUT	XTAL	XTAL	XTAL		PMU_CLK32K_XOUT
PP3V3_CLK32K_XOUT_R	XTAL	XTAL	XTAL		PMU_CLK32K_XOUT_R

Page Notes

Power aliases required by this page:

- =PP3V3_ALL_PMU
- =PP3V3_PWRON_PMU
- =PPVREF_PMU (PMU AVCC or 2.5V reference)

Signal aliases required by this page:

- =I2C_PMU_SCL
- =I2C_PMU_SDA
- =I2C_PMU_SMB_SCL
- =I2C_PMU_SMB_SDA
- =JTAG_BBANGER_TCK
- =JTAG_BBANGER_TDI
- =JTAG_BBANGER_TMS
- =JTAG_BBANGER_TRST_L

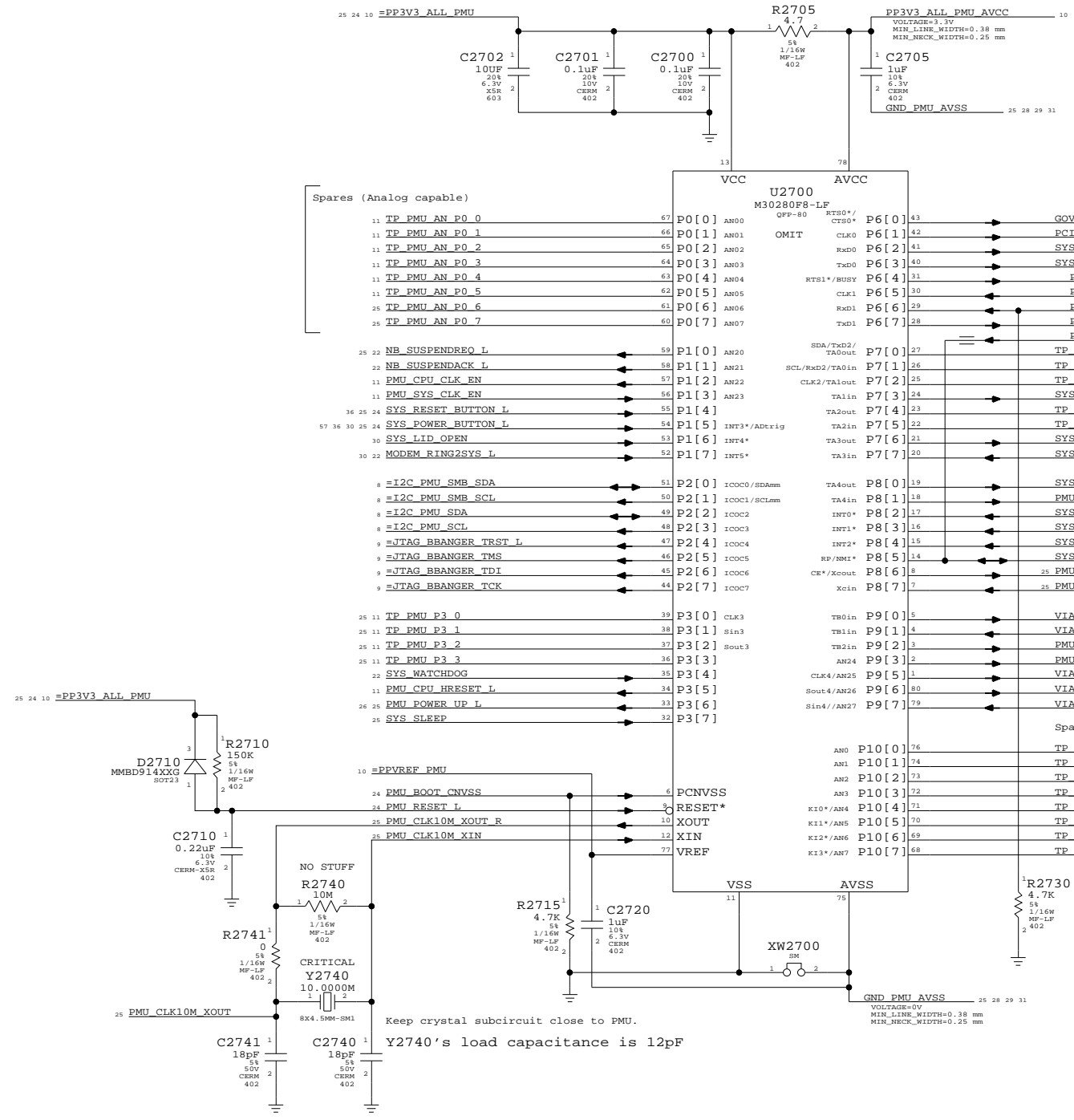
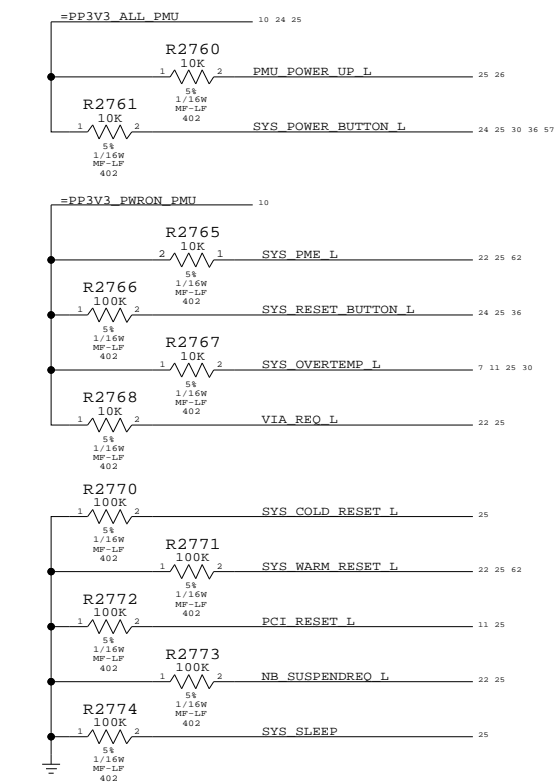
NOTE: Boot-banger pins can be aliased to TP_ or NC_ if not implemented.

BOM options provided by this page: (NONE)

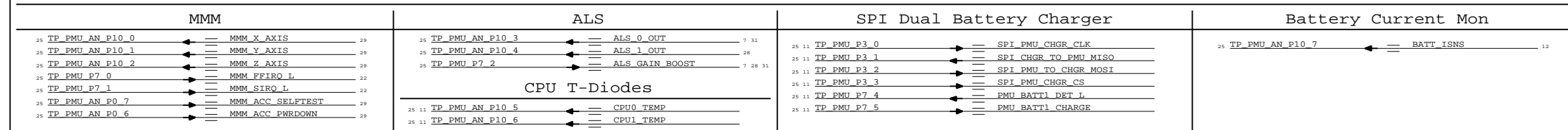
NOTE: TP_PMU_Fx_x signals are general-purpose spares. Some pins are reserved for alternate functions. TP_PMU_AN_Fx_x signals are general-purpose spares that can also be used as analog inputs.

NOTE: All analog inputs to PMU should have a 100pF capacitor to the PMU AVSS signal (GND_PMU_AVSS). None of those capacitors are provided on this page.

PMU Pull-ups / pull-downs



Additional PMU05 "Modules"



Power Management Unit (PMU05)

SYNC_MASTER=N/A SYNC_DATE=N/A

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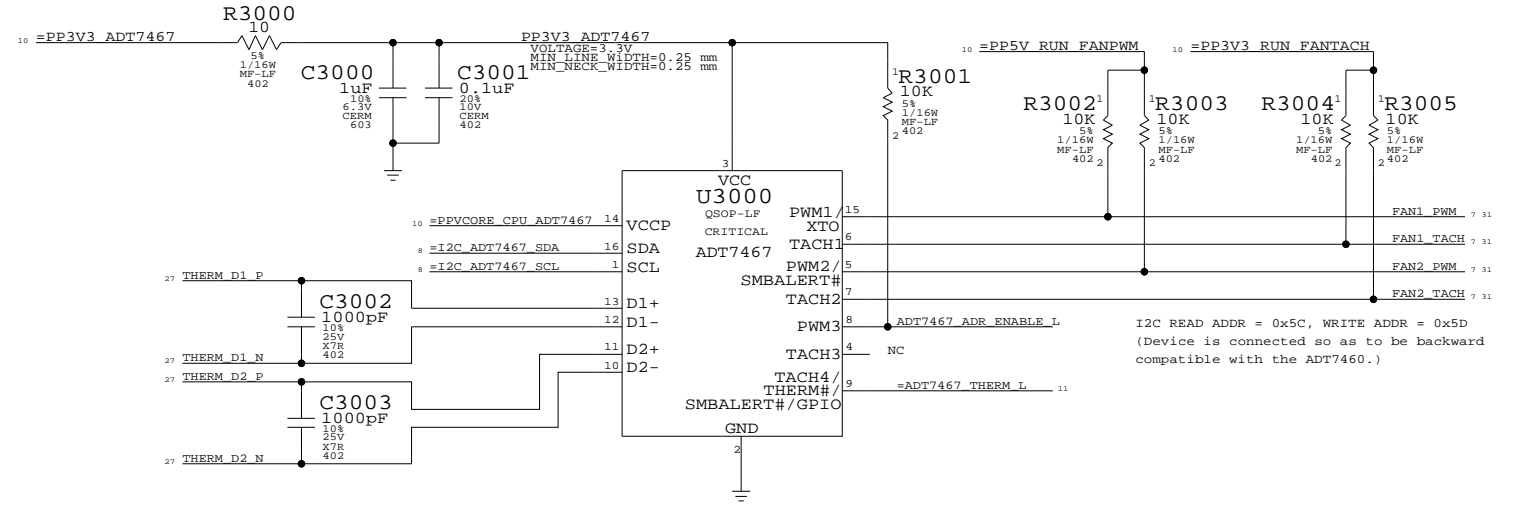
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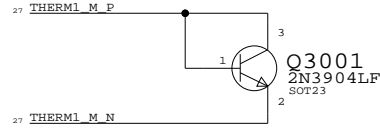
APPLE COMPUTER INC.	SCALE: NONE	DRAWING NUMBER: D 051-7001	REV.: D
		SHEET: 27	OF: 115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
ES2P	THERM	THERM	THERM1_M
ES2N	THERM	THERM	THERM1_N
ES3P	THERM	THERM	THERM2_M
ES3N	THERM	THERM	THERM2_N
ES3A	THERM	THERM	THERM1_A
ES3N	THERM	THERM	THERM1_N
ES3A	THERM	THERM	THERM2_A
ES3N	THERM	THERM	THERM2_N
ES3D	THERM	THERM	THERM_D1
ES3N	THERM	THERM	THERM_D1
ES3D	THERM	THERM	THERM_D2
ES3N	THERM	THERM	THERM_D2

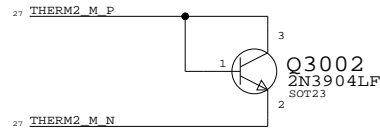
FAN CONTROLLER



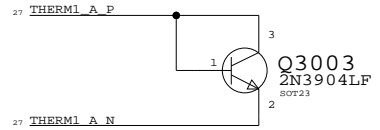
PLACE CLOSE TO CPU MAIN1



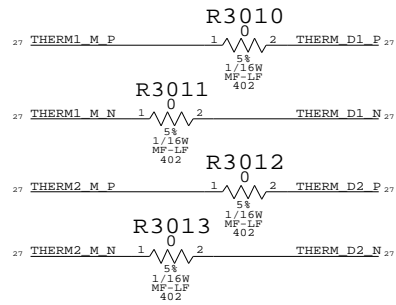
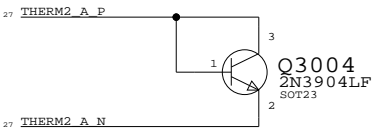
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY MAIN2



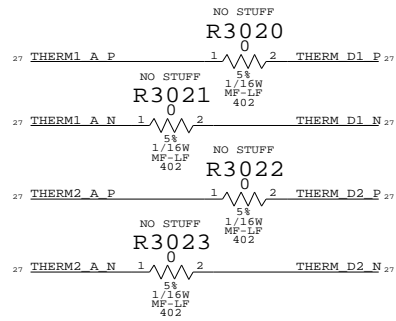
PLACE UNDERNEATH UPPER RAM ALTERNATE1



PLACE CLOSE TO BATTERY CHARGER/VCORE ALTERNATE2

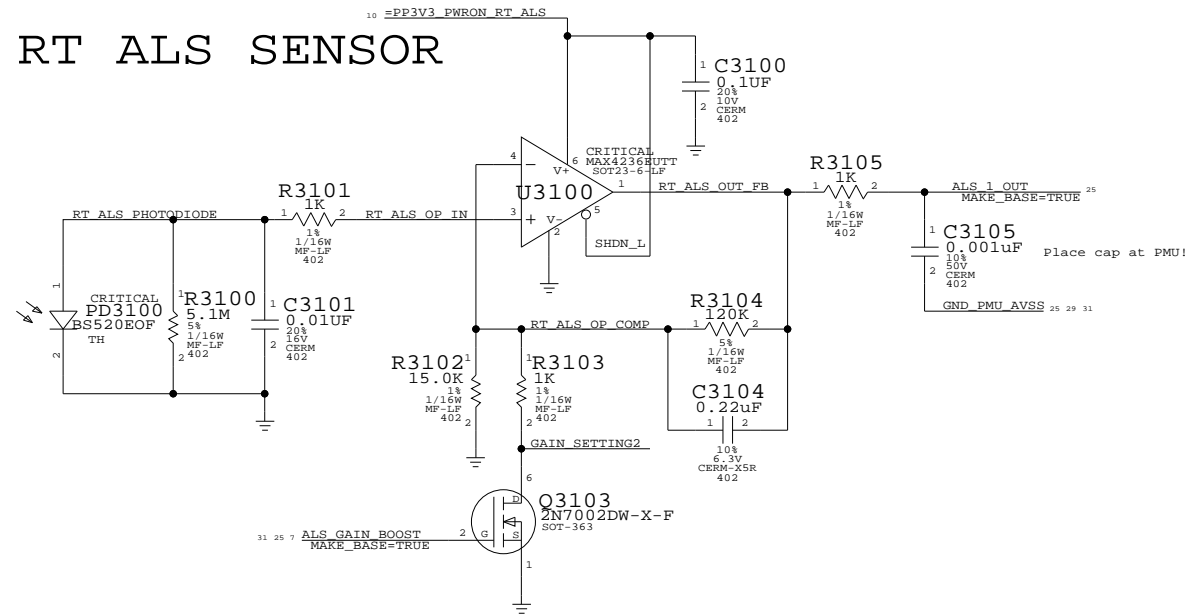


KEEP STUFFING RESISTORS CLOSE TO ADT7467 CONTROLLER



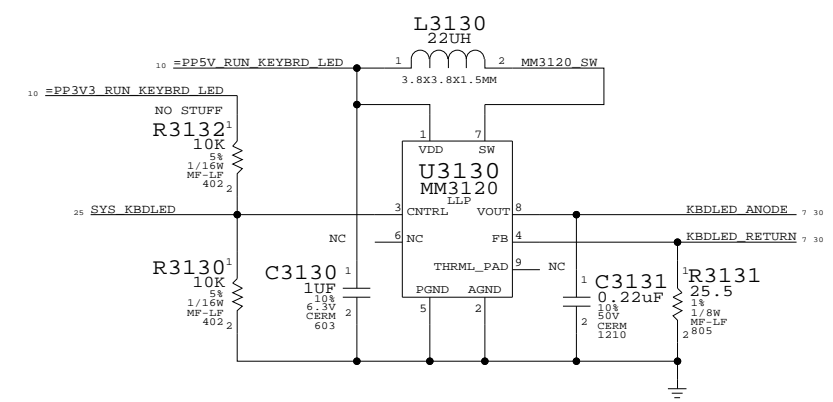
Fan Controller
 SYNC_MASTER=N/A SYNC_DATE=N/A
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	D	051-7001	D
SCALE	SHT	OF	REV.
NONE	30	115	



PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1191	353S1186		U3100	Primary is unity gain stable/als is stable at 0=5

Keyboard LED Driver



ALS Support

SYNC_MASTER=N/A SYNC_DATE=N/A

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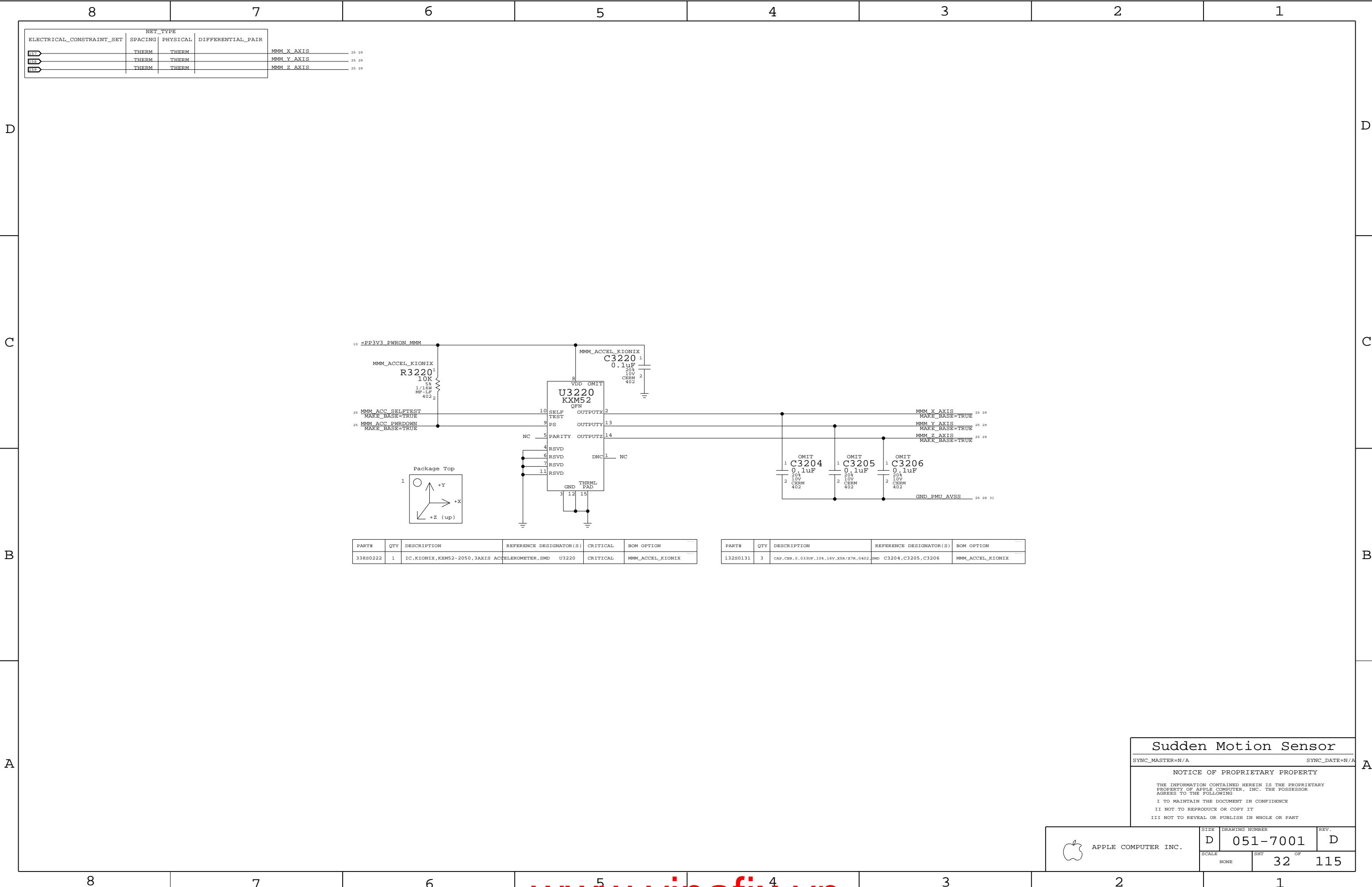
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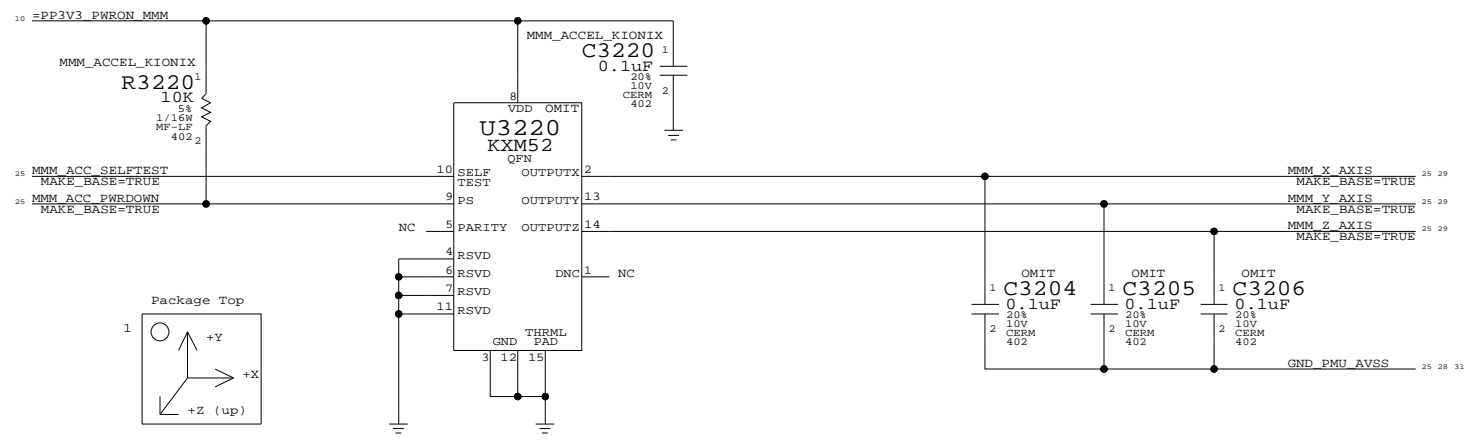
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	D	051-7001	D
SCALE	SHT	OF	
NONE	31	115	



ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
ES7	THERM	THERM	MMM X AXIS
ES8	THERM	THERM	MMM Y AXIS
ES9	THERM	THERM	MMM Z AXIS



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0222	1	IC, KIONIX, KXM52-2050, 3AXIS ACCELEROMETER, SMD	U3220	CRITICAL	MMM_ACCEL_KIONIX

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0131	3	CAP, CER, 0.033UF, 10V, 16V, X5R, X7R, 0402, SMD	C3204, C3205, C3206	MMM_ACCEL_KIONIX

Sudden Motion Sensor

SYNC_MASTER=N/A SYNC_DATE=N/A

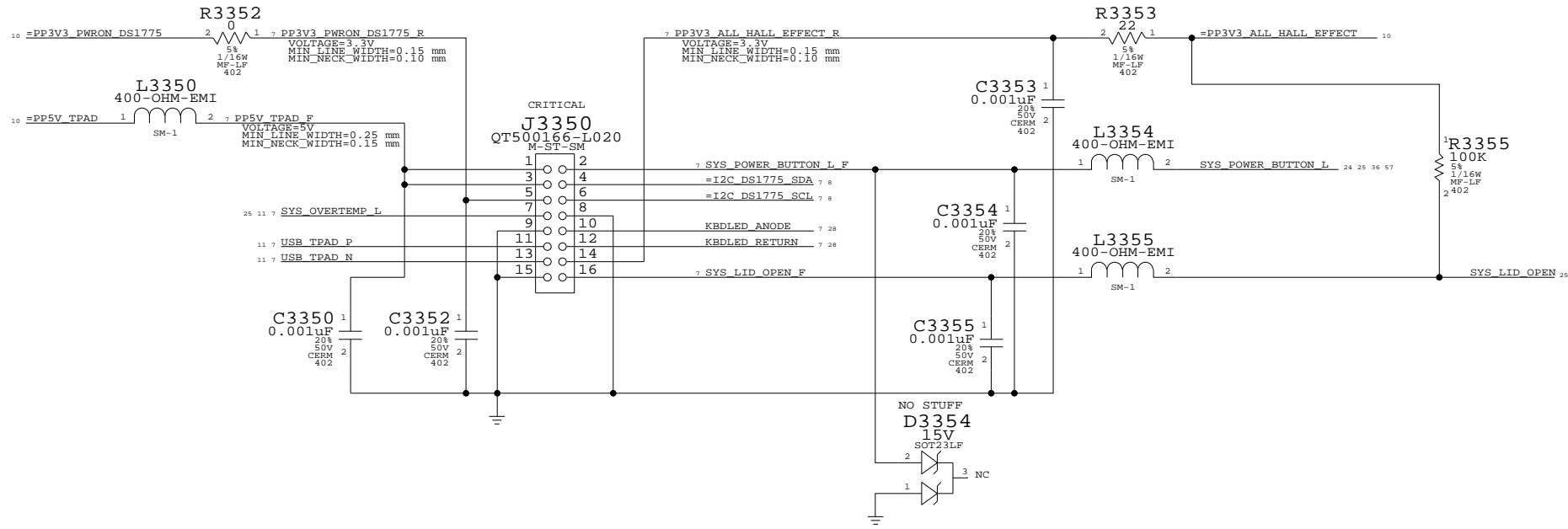
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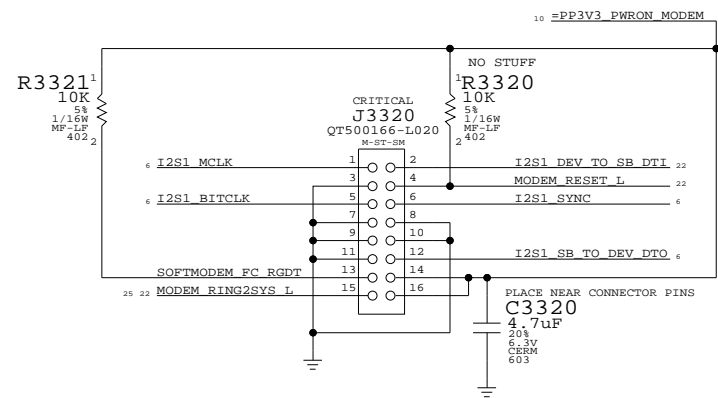
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7001	D
SCALE	SHT OF		
NONE	32 OF		115

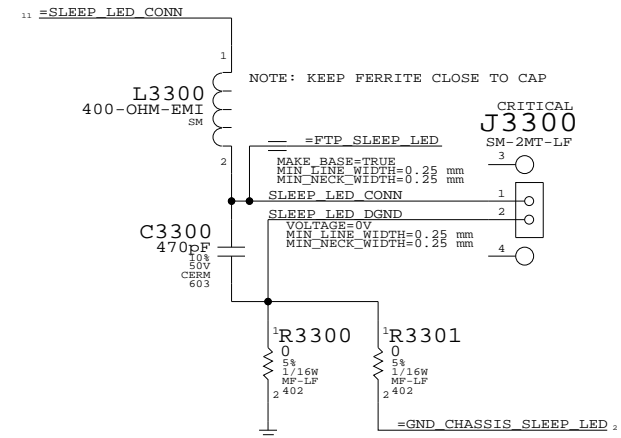
USB Trackpad Connector



SOFT MODEM CONN



SLEEP LED CONNECTOR



Q16C Internal I/O I

SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-7001	D
SCALE	SHT OF		REV.
NONE	33		115

8

7

6

5

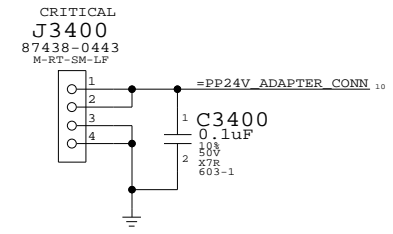
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3

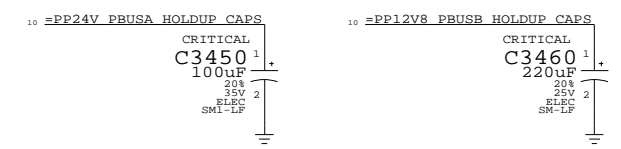
2

1

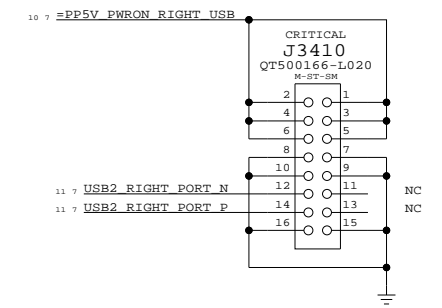
ADAPTER CONNECTOR



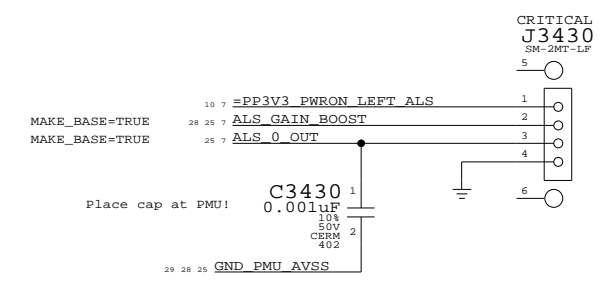
PBUS HOLD-UP CAPS



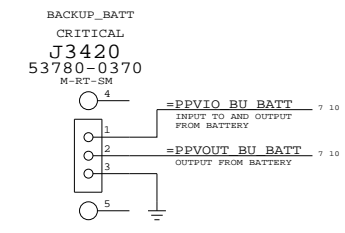
RIGHT USB BOARD



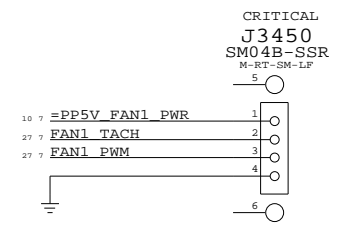
LEFT ALS CONNECTOR



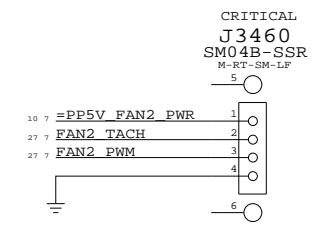
BACKUP BATTERY CONNECTOR



CPU FAN



GPU FAN



Q16C Internal I/O II

SYNC_MASTER=N/A SYNC_DATE=N/A

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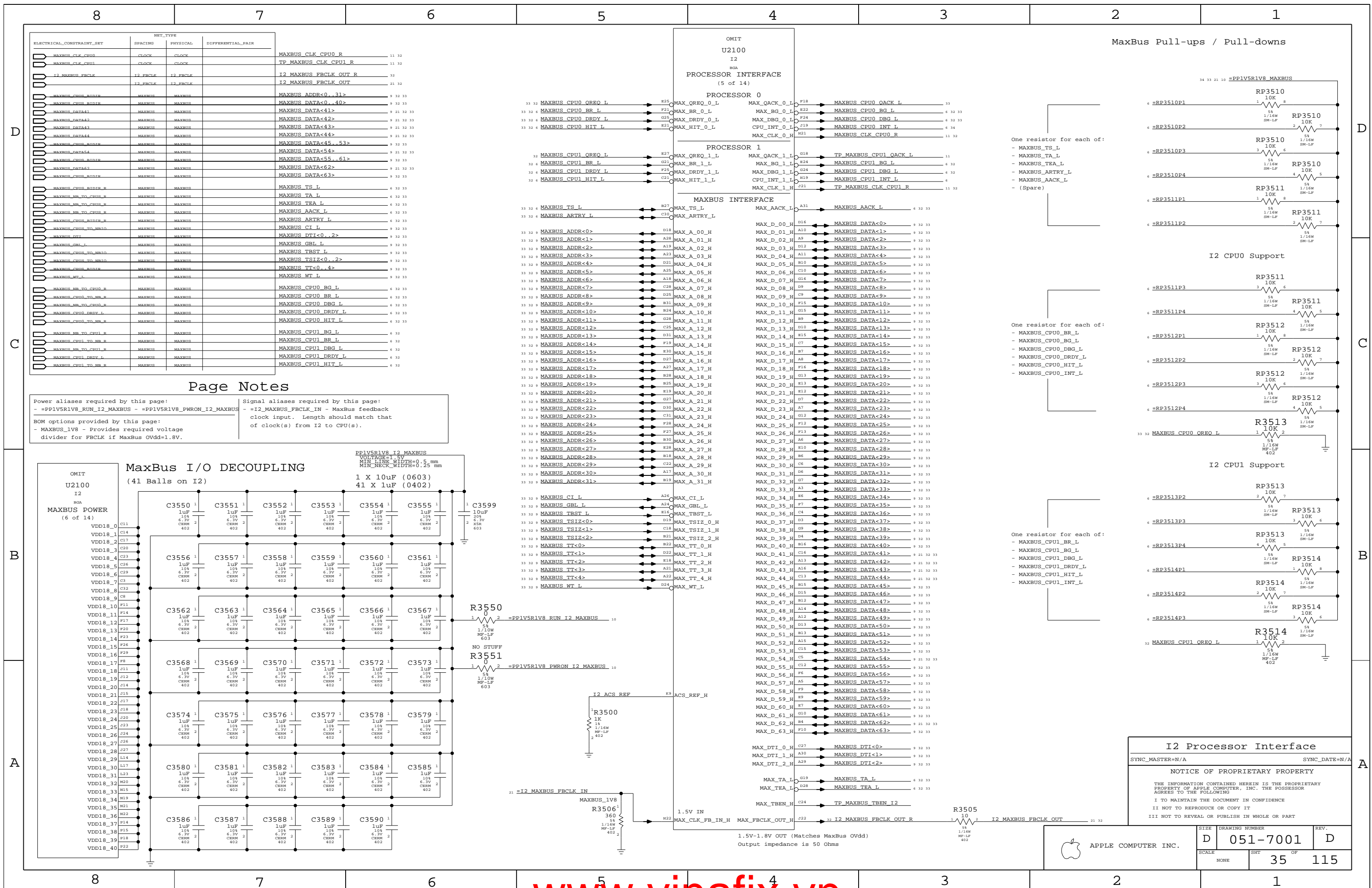
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	D	051-7001	D
SCALE	SHT OF		
NONE	34 OF		115



ELECTRICAL_CONSTRAINT_SET		NET_TYPE		SPACING	PHYSICAL	DIFFERENTIAL_PAIR
MAXBUS_CLK_CPU0	CLOCK	CLOCK				
MAXBUS_CLK_CPU1	CLOCK	CLOCK				
I2_MAXBUS_FBCLK	I2_FBCLK	I2_FBCLK				
MAXBUS_CPU0_BSTR	MAXBUS	MAXBUS				
MAXBUS_CPU1_BSTR	MAXBUS	MAXBUS				
MAXBUS_DATA41	MAXBUS	MAXBUS				
MAXBUS_DATA42	MAXBUS	MAXBUS				
MAXBUS_DATA43	MAXBUS	MAXBUS				
MAXBUS_DATA44	MAXBUS	MAXBUS				
MAXBUS_DATA45	MAXBUS	MAXBUS				
MAXBUS_DATA46	MAXBUS	MAXBUS				
MAXBUS_CPU0_BSTR_R	MAXBUS	MAXBUS				
MAXBUS_CPU1_BSTR_R	MAXBUS	MAXBUS				
MAXBUS_CPU0_DRDY_L	MAXBUS	MAXBUS				
MAXBUS_CPU1_DRDY_L	MAXBUS	MAXBUS				
MAXBUS_CPU0_HIT_L	MAXBUS	MAXBUS				
MAXBUS_CPU1_HIT_L	MAXBUS	MAXBUS				
MAXBUS_TS_L	MAXBUS	MAXBUS				
MAXBUS_TA_L	MAXBUS	MAXBUS				
MAXBUS_TE_A_L	MAXBUS	MAXBUS				
MAXBUS_ARTRY_L	MAXBUS	MAXBUS				
MAXBUS_ARTRY_R	MAXBUS	MAXBUS				
MAXBUS_CI_L	MAXBUS	MAXBUS				
MAXBUS_DTI<0..2>	MAXBUS	MAXBUS				
MAXBUS_GBL_L	MAXBUS	MAXBUS				
MAXBUS_TBST_L	MAXBUS	MAXBUS				
MAXBUS_TSIZ<0..2>	MAXBUS	MAXBUS				
MAXBUS_TT<0..4>	MAXBUS	MAXBUS				
MAXBUS_WT_L	MAXBUS	MAXBUS				
MAXBUS_CPU0_BG_L	MAXBUS	MAXBUS				
MAXBUS_CPU0_DBG_L	MAXBUS	MAXBUS				
MAXBUS_CPU0_DRDY_L	MAXBUS	MAXBUS				
MAXBUS_CPU0_HIT_L	MAXBUS	MAXBUS				
MAXBUS_CPU1_BG_L	MAXBUS	MAXBUS				
MAXBUS_CPU1_DBG_L	MAXBUS	MAXBUS				
MAXBUS_CPU1_DRDY_L	MAXBUS	MAXBUS				
MAXBUS_CPU1_HIT_L	MAXBUS	MAXBUS				

Page Notes

Power aliases required by this page:
 - =PPIV5R1V8_RUN_I2_MAXBUS - =PPIV5R1V8_PWRON_I2_MAXBUS
 Signal aliases required by this page:
 - =I2_MAXBUS_FBCLK_IN - MaxBus feedback clock input. Length should match that of clock(s) from I2 to CPU(s).

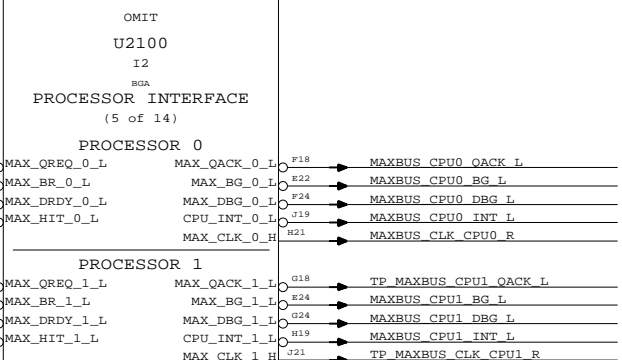
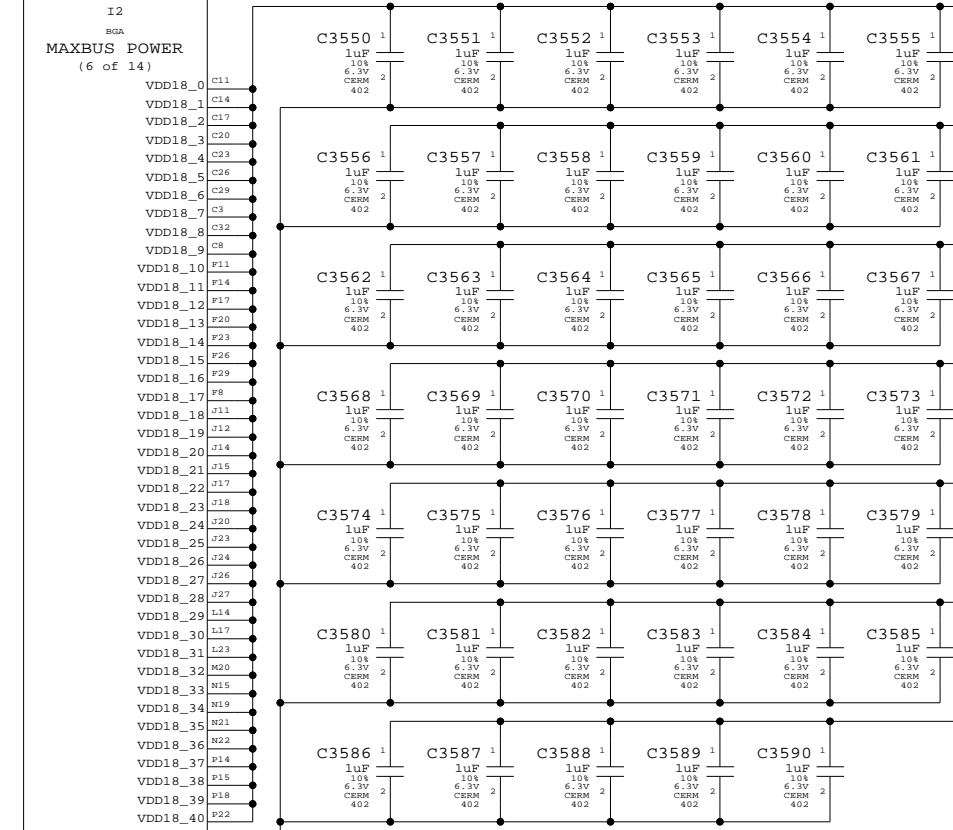
BOM options provided by this page:
 - MAXBUS_LV8 - Provides required voltage divider for FBCLK if MaxBus Ovdd=1.8V.

MaxBus I/O DECOUPLING

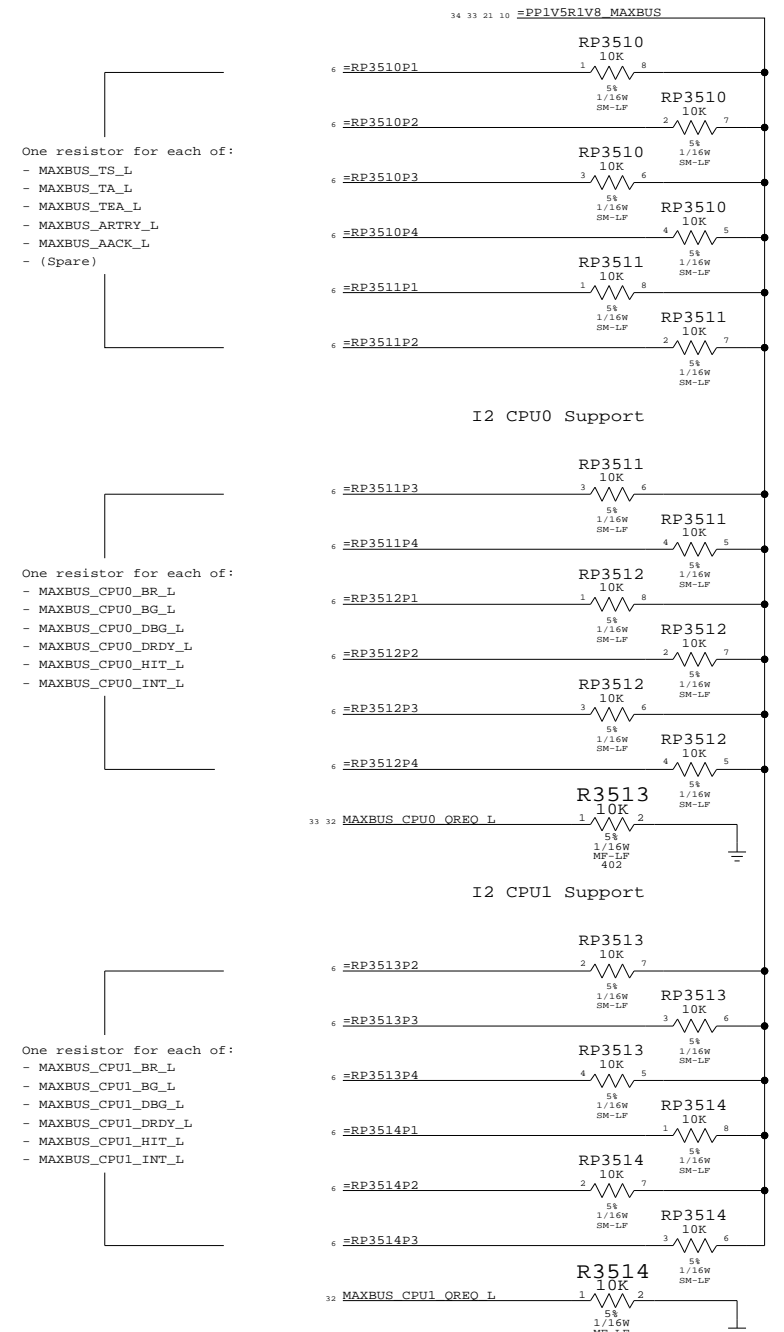
(41 Balls on I2)

PPIV5R1V8 I2_MAXBUS
 VOLTAGE=1.5V
 MIN_LINE_WIDTH=0.5 mm
 MIN_NECK_WIDTH=0.25 mm

1 X 10uF (0603)
 41 X 1uF (0402)



MaxBus Pull-ups / Pull-downs



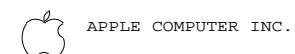
I2 Processor Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

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D	051-7001	D
SCALE	SHEET	OF
NONE	35	115



ELECTRICAL_CONSTRAINT_SET	NET_TYPE	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
MAXBUS	CLOCK	CLOCK	CLOCK	

Page Notes

Power aliases required by this page:
 - =PPIV5R1V8_MAXBUS

Signal aliases required by this page:
 - =MAXBUS_CPU0_CLK

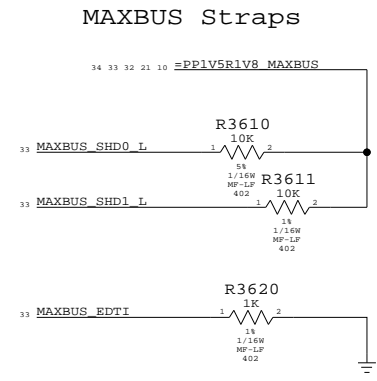
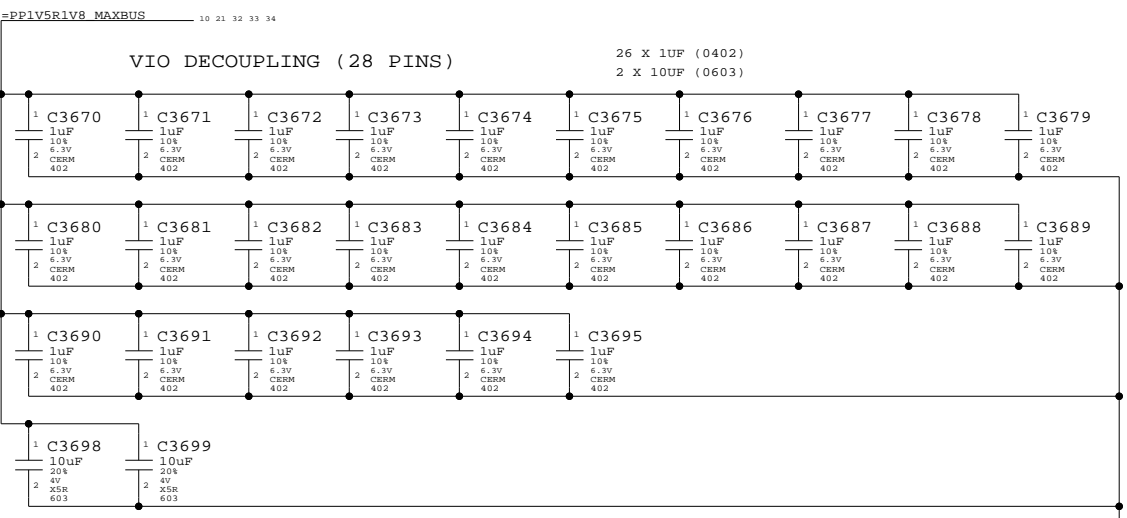
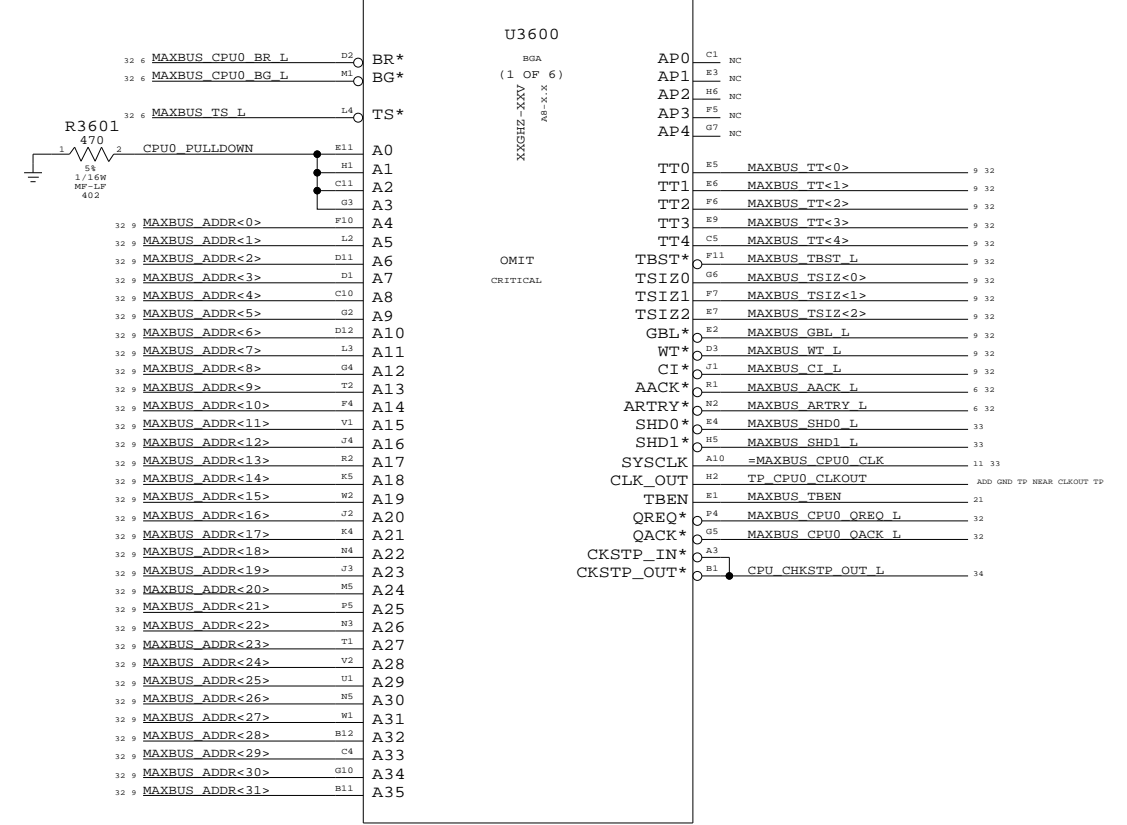
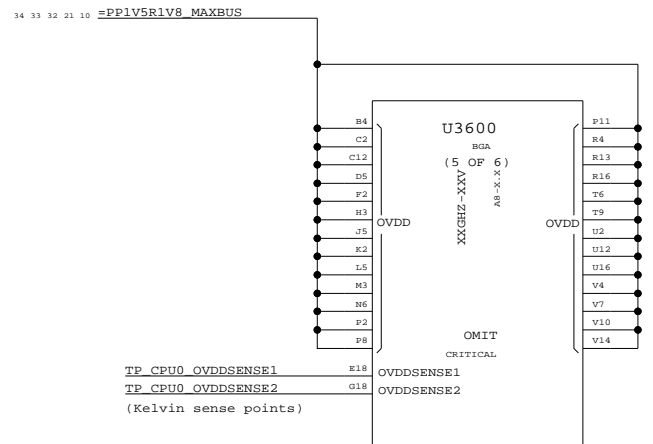
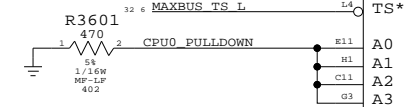
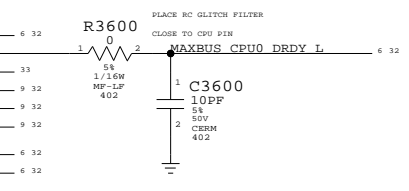
BOM options provided by this page:
 (NONE)

- 32 9 MAXBUS_DATA<0> R15 D0
- 32 9 MAXBUS_DATA<1> M15 D1
- 32 9 MAXBUS_DATA<2> T14 D2
- 32 9 MAXBUS_DATA<3> V16 D3
- 32 9 MAXBUS_DATA<4> W16 D4
- 32 9 MAXBUS_DATA<5> T15 D5
- 32 9 MAXBUS_DATA<6> U15 D6
- 32 9 MAXBUS_DATA<7> P14 D7
- 32 9 MAXBUS_DATA<8> V13 D8
- 32 9 MAXBUS_DATA<9> M13 D9
- 32 9 MAXBUS_DATA<10> T13 D10
- 32 9 MAXBUS_DATA<11> P13 D11
- 32 9 MAXBUS_DATA<12> U14 D12
- 32 9 MAXBUS_DATA<13> M14 D13
- 32 9 MAXBUS_DATA<14> R12 D14
- 32 9 MAXBUS_DATA<15> T12 D15
- 32 9 MAXBUS_DATA<16> M12 D16
- 32 9 MAXBUS_DATA<17> V12 D17
- 32 9 MAXBUS_DATA<18> M11 D18
- 32 9 MAXBUS_DATA<19> M10 D19
- 32 9 MAXBUS_DATA<20> R11 D20
- 32 9 MAXBUS_DATA<21> U11 D21
- 32 9 MAXBUS_DATA<22> M11 D22
- 32 9 MAXBUS_DATA<23> T11 D23
- 32 9 MAXBUS_DATA<24> R10 D24
- 32 9 MAXBUS_DATA<25> M9 D25
- 32 9 MAXBUS_DATA<26> P10 D26
- 32 9 MAXBUS_DATA<27> U10 D27
- 32 9 MAXBUS_DATA<28> R9 D28
- 32 9 MAXBUS_DATA<29> M10 D29
- 32 9 MAXBUS_DATA<30> U9 D30
- 32 9 MAXBUS_DATA<31> V9 D31
- 32 9 MAXBUS_DATA<32> W5 D32
- 32 9 MAXBUS_DATA<33> U6 D33
- 32 9 MAXBUS_DATA<34> T5 D34
- 32 9 MAXBUS_DATA<35> U5 D35
- 32 9 MAXBUS_DATA<36> W7 D36
- 32 9 MAXBUS_DATA<37> R6 D37
- 32 9 MAXBUS_DATA<38> P7 D38
- 32 9 MAXBUS_DATA<39> V6 D39
- 32 9 MAXBUS_DATA<40> P17 D40
- 32 21 MAXBUS_DATA<41> R19 D41
- 32 21 MAXBUS_DATA<42> V18 D42
- 32 21 MAXBUS_DATA<43> R18 D43
- 32 21 MAXBUS_DATA<44> V19 D44
- 32 9 MAXBUS_DATA<45> T19 D45
- 32 9 MAXBUS_DATA<46> U19 D46
- 32 9 MAXBUS_DATA<47> M19 D47
- 32 9 MAXBUS_DATA<48> U18 D48
- 32 9 MAXBUS_DATA<49> M17 D49
- 32 9 MAXBUS_DATA<50> M18 D50
- 32 9 MAXBUS_DATA<51> T18 D51
- 32 9 MAXBUS_DATA<52> T18 D52
- 32 9 MAXBUS_DATA<53> T17 D53
- 32 21 MAXBUS_DATA<54> M3 D54
- 32 9 MAXBUS_DATA<55> V17 D55
- 32 9 MAXBUS_DATA<56> U4 D56
- 32 9 MAXBUS_DATA<57> U8 D57
- 32 9 MAXBUS_DATA<58> U7 D58
- 32 9 MAXBUS_DATA<59> R7 D59
- 32 9 MAXBUS_DATA<60> P6 D60
- 32 9 MAXBUS_DATA<61> R8 D61
- 32 21 MAXBUS_DATA<62> W8 D62
- 32 9 MAXBUS_DATA<63> T8 D63

U3600
 BGA
 (2 OF 6)
 AB-X-X

OMIT
 CRITICAL

- DP0 T3 NC
- DP1 W4 NC
- DP2 T4 NC
- DP3 W5 NC
- DP4 M6 NC
- DP5 V3 NC
- DP6 N8 NC
- DP7 W6 NC
- DBG* M2 MAXBUS_CPU0_DBG_L
- DRDY* R3 MAXBUS_CPU0_DRDY_L_R
- DTIO G1 MAXBUS_EDTI
- DTI1 K1 MAXBUS_DTI<0>
- DTI2 P1 MAXBUS_DTI<1>
- DTI3 N1 MAXBUS_DTI<2>
- TA* K6 MAXBUS_TA_L
- TEA* L1 MAXBUS_TEA_L
- HIT* R2 MAXBUS_CPU0_HIT_L



A8 MaxBus (CPU0)

SYNC_MASTER=MULLET SYNC_DATE=08/02/2005

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SCALE	NONE	SHT	OF
		36	115

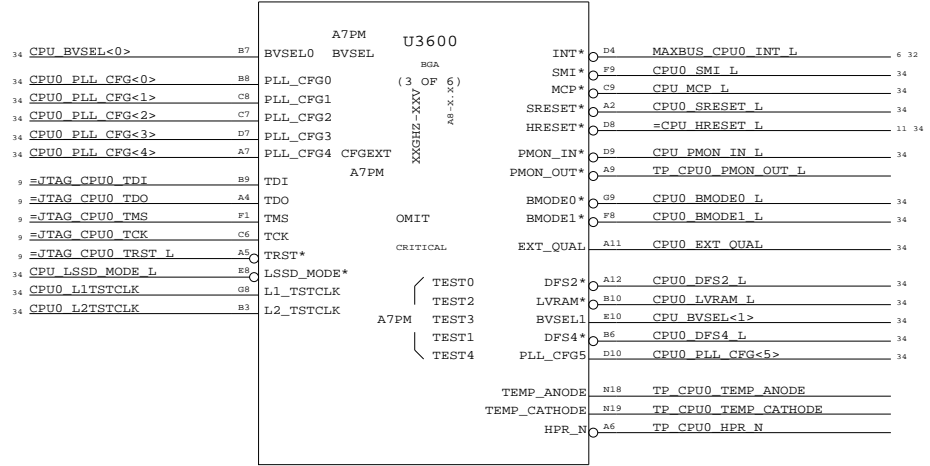
Page Notes

Power aliases required by this page:

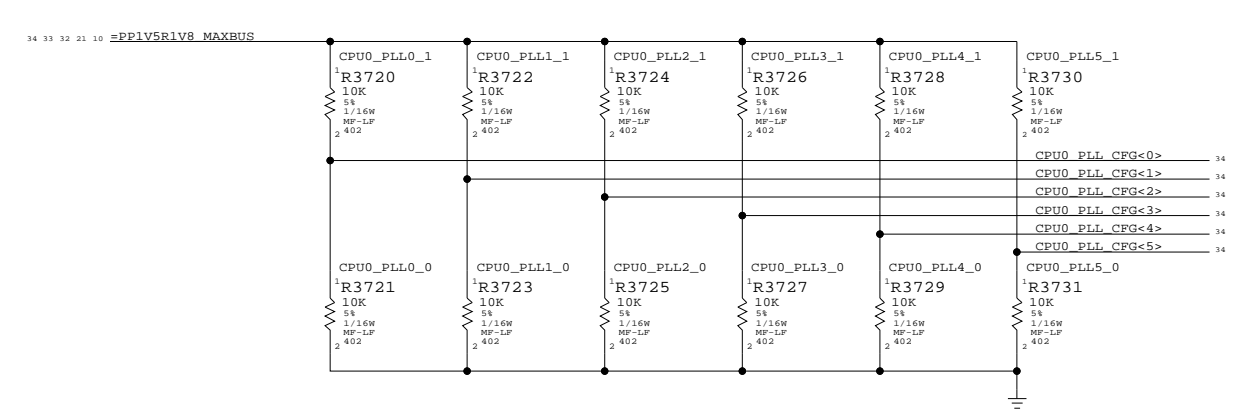
- =PPIV5R1V8_MAXBUS
 - =PP3V3_PWRON_PLLSEL
- Signal aliases required by this page:
- =CPU0_JTAG_TDI
 - =CPU0_JTAG_TDO
 - =CPU0_JTAG_TMS
 - =CPU0_JTAG_TCK
 - =CPU0_JTAG_TRST_L
 - =CPU_HRESET_L (Reset given to all processors)

BOM options provided by this page:

- CPU0_PLL0_0/1
 - CPU0_PLL1_0/1
 - CPU0_PLL2_0/1
 - CPU0_PLL3_0/1
 - CPU0_PLL4_0/1
 - CPU0_PLL5_0/1
- These must be selected to set the CPU core to Maxbus frequency ratio to attain the desired spec
- MAXBUS_1V5 - MAXBUS_1V8
- One of these must be selected to set the Maxbus voltage
- * the MAXBUS_1V5 option does not exist for A7PM
 - CPU_A7PM - CPU_A8
- One of these must be selected to ensure the the above strap is interpreted correctly

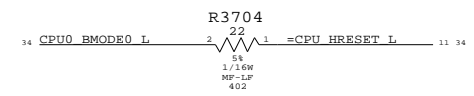


CPU0 PLL CONFIG CIRCUITRY

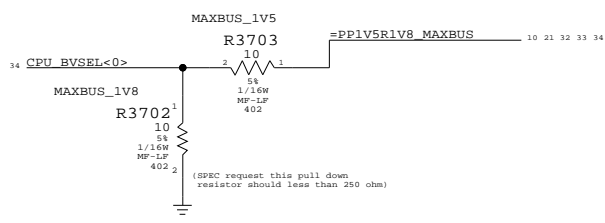


BUS TYPE SELECT

SIGNAL	TIED	MODE
CPU0_BMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE



MAXBUS VSEL



CPU0 FREQUENCY CONFIGURATION

() Indicates DFS setting supported by A8 only

BOM GROUP	DFS SUPPORT	PLL BITS	BOM OPTIONS
CPU0_BUSRATIO_1.0X	-	012345	CPU0_PLL0_0, CPU0_PLL1_0, CPU0_PLL2_1, CPU0_PLL3_1, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_2.0X	-	010000	CPU0_PLL0_0, CPU0_PLL1_1, CPU0_PLL2_0, CPU0_PLL3_0, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_3.0X	-	100000	CPU0_PLL0_1, CPU0_PLL1_0, CPU0_PLL2_0, CPU0_PLL3_0, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_4.0X	2.0X	101000	CPU0_PLL0_1, CPU0_PLL1_0, CPU0_PLL2_1, CPU0_PLL3_0, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_5.0X	2.5X	101100	CPU0_PLL0_1, CPU0_PLL1_0, CPU0_PLL2_1, CPU0_PLL3_1, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_5.5X	(2.75X)	-	CPU0_PLL0_1, CPU0_PLL1_0, CPU0_PLL2_0, CPU0_PLL3_1, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_6.0X	3.0X	110100	CPU0_PLL0_1, CPU0_PLL1_1, CPU0_PLL2_0, CPU0_PLL3_1, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_6.5X	(3.25X)	-	CPU0_PLL0_0, CPU0_PLL1_1, CPU0_PLL2_0, CPU0_PLL3_1, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_7.0X	3.5X	001000	CPU0_PLL0_0, CPU0_PLL1_0, CPU0_PLL2_1, CPU0_PLL3_0, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_7.5X	(3.75X)	-	CPU0_PLL0_0, CPU0_PLL1_0, CPU0_PLL2_0, CPU0_PLL3_1, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_8.0X	4.0X	2.0X	110000
CPU0_BUSRATIO_8.5X	(4.25X)	-	011000
CPU0_BUSRATIO_9.0X	4.5X	(2.25X)	011110
CPU0_BUSRATIO_9.5X	(4.75X)	-	011100
CPU0_BUSRATIO_10.0X	5.0X	2.5X	101010
CPU0_BUSRATIO_10.5X	(5.25X)	-	100010
CPU0_BUSRATIO_11.0X	5.5X	(2.75X)	100110
CPU0_BUSRATIO_11.5X	(5.75X)	-	000000
CPU0_BUSRATIO_12.0X	6.0X	3.0X	101110
CPU0_BUSRATIO_12.5X	(6.25X)	-	111110
CPU0_BUSRATIO_13.0X	6.5X	(3.25X)	010110
CPU0_BUSRATIO_13.5X	(6.75X)	-	111000
CPU0_BUSRATIO_14.0X	7.0X	3.5X	110010
CPU0_BUSRATIO_15.0X	7.5X	(3.75X)	000110
CPU0_BUSRATIO_16.0X	8.0X	4.0X	110110
CPU0_BUSRATIO_17.0X	8.5X	(4.25X)	000010
CPU0_BUSRATIO_18.0X	9.0X	4.5X	001010
CPU0_BUSRATIO_20.0X	10.0X	5.0X	001110
CPU0_BUSRATIO_21.0X	10.5X	(5.25X)	010010
CPU0_BUSRATIO_24.0X	12.0X	6.0X	011010
CPU0_BUSRATIO_28.0X	14.0X	7.0X	111010

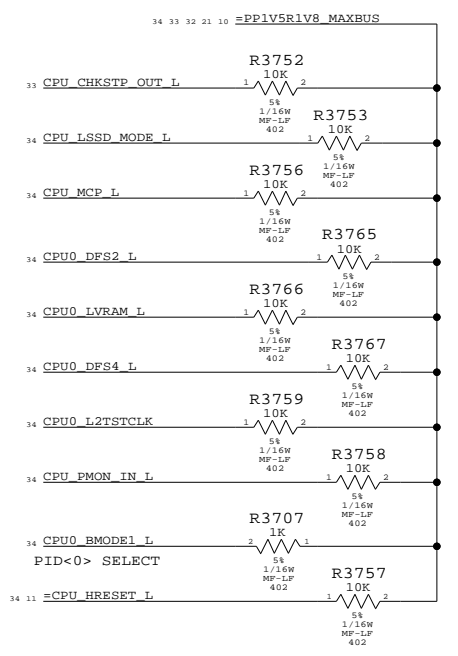
A7PM

OVDD	BVSEL0	BVSEL1
1.8V INTERFACE	GND	OVDD
2.5V INTERFACE	OVDD	OVDD
2.5V INTERFACE	CPU_HRESET_L	OVDD
RESERVED(1.5V)	CPU_HRESET_INV	OVDD

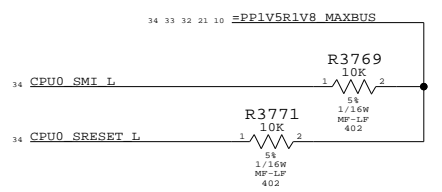
A8

OVDD	BVSEL0	BVSEL1
1.8V INTERFACE	GND	GND
1.5V INTERFACE	OVDD	GND
RESERVED	CPU_HRESET_L	GND
RESERVED	CPU_HRESET_INV	GND
2.5V INTERFACE	GND	OVDD
2.5V INTERFACE	OVDD	OVDD
RESERVED	CPU_HRESET_L	OVDD
RESERVED	CPU_HRESET_INV	OVDD

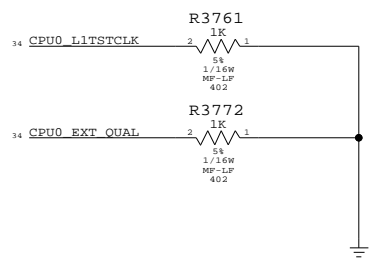
CPU PULLUPS



INTERRUPT PULL-UPS



CPU PULLDOWNS



A8 Configuration Straps

SYNC_MASTER=MULLET SYNC_DATE=08/02/2005

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NONE	37	115	

Page Notes

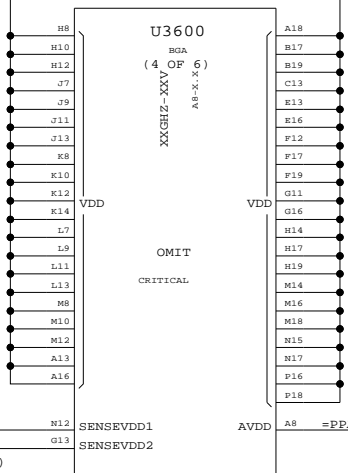
Power aliases required by this page:
 - =PPVCORE_CPU0

Signal aliases required by this page:
 (NONE)

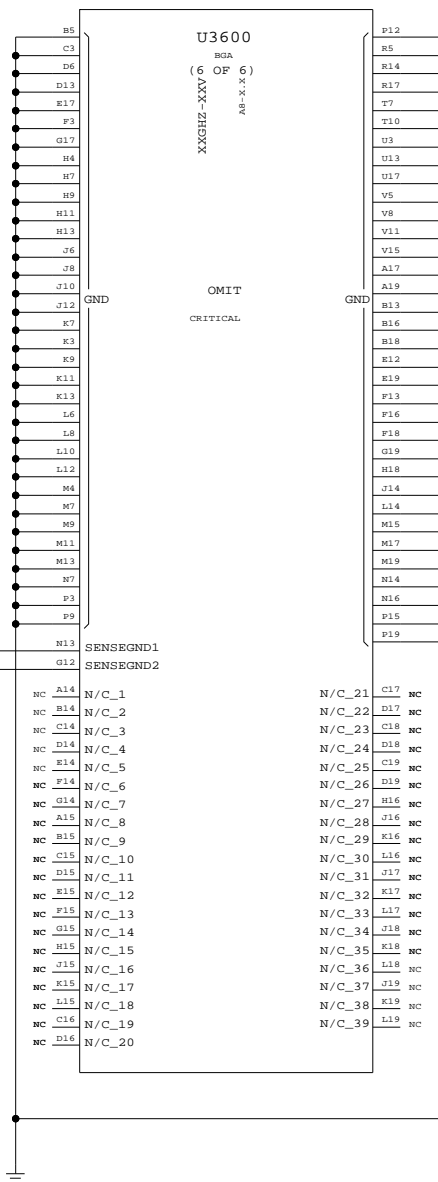
BOM options provided by this page:
 (NONE)

35 10 =PPVCORE_CPU0

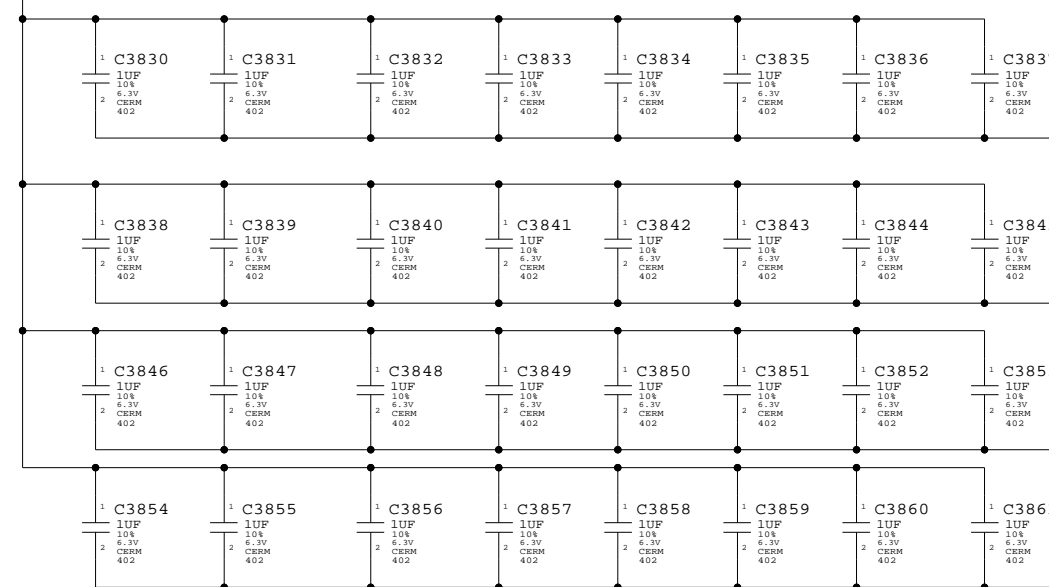
TP_CPU0_SENSEVDD1
 TP_CPU0_SENSEVDD2
 (Kelvin sense points)



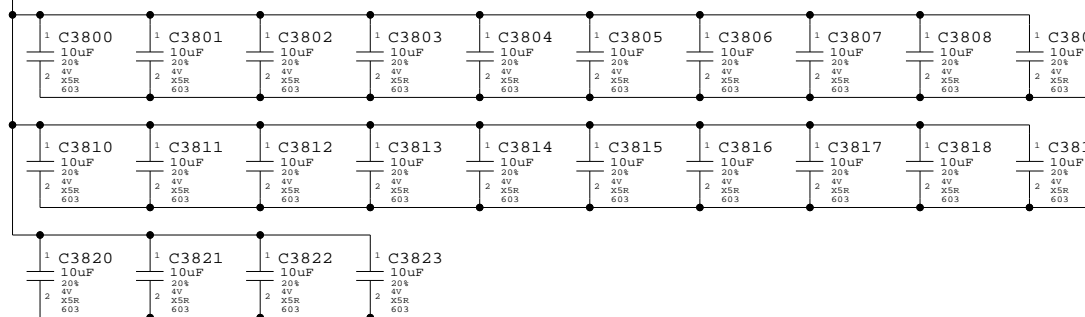
TP_CPU0_SENSEGND1
 TP_CPU0_SENSEGND2
 (Kelvin sense points)



VCORE BULK CAPS
 40 X 1 UF (0402)



24 X 10 UF (0603)



A8 Power (CPU0)

SYNC_MASTER=MULLET SYNC_DATE=08/02/2005

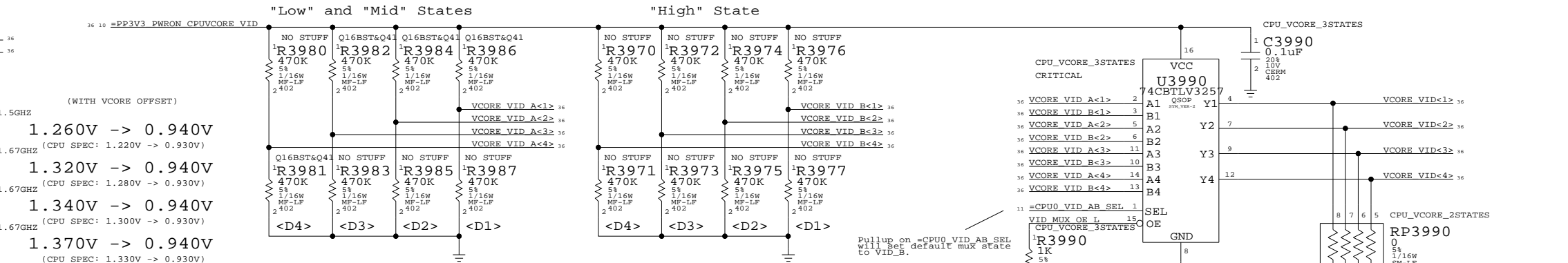
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SCALE	SHT OF		REV.
NONE	38 OF 115		

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
MEM	THERM	THERM	
MEM	THERM	THERM	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0270	1	RES, 3.48K, 1%, 1/16W, MF-LF, 402, SMD	R3946	CPU0_VCORE_IV22
114S0258	1	RES, 2.61K, 1%, 1/16W, MF-LF, 402, SMD	R3944	CPU0_VCORE_IV22
114S0246	1	RES, 2.0K, 1%, 1/16W, MF-LF, 402, SMD	R3946	CPU0_VCORE_IV28
114S0294	1	RES, 6.04K, 1%, 1/16W, MF-LF, 402, SMD	R3944	CPU0_VCORE_IV28
114S0276	1	RES, 4.02K, 1%, 1/16W, MF-LF, 402, SMD	R3946	CPU0_VCORE_IV30
114S0254	1	RES, 2.43K, 1%, 1/16W, MF-LF, 402, SMD	R3944	CPU0_VCORE_IV30
114S0246	1	RES, 2.0K, 1%, 1/16W, MF-LF, 402, SMD	R3946	CPU0_VCORE_IV33
114S0294	1	RES, 6.04K, 1%, 1/16W, MF-LF, 402, SMD	R3944	CPU0_VCORE_IV33



(WITH VCORE OFFSET)

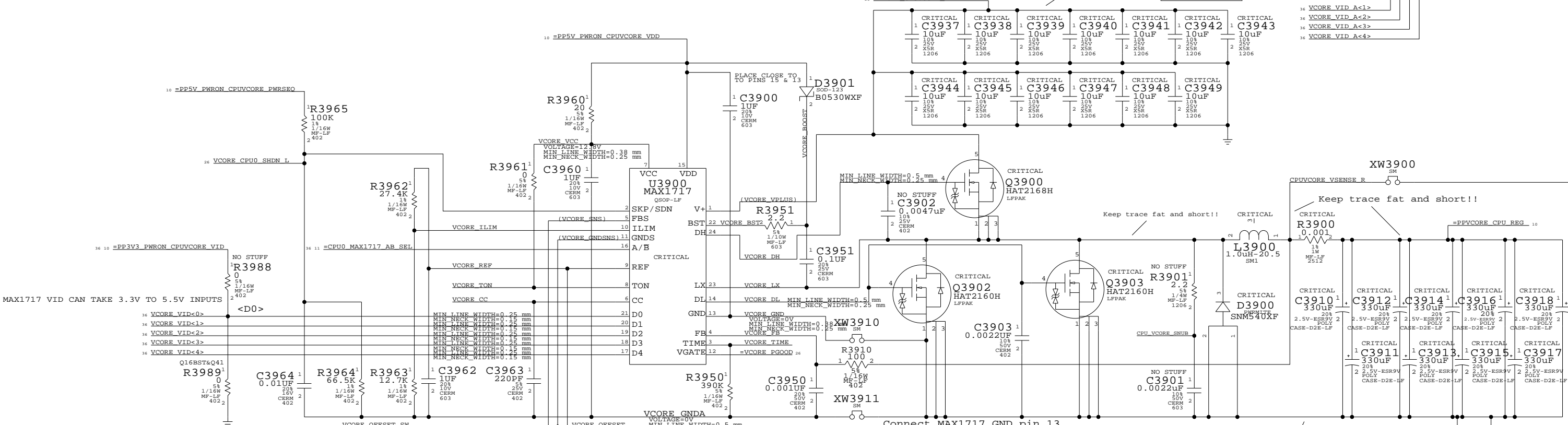
1.5GHZ
1.260V -> 0.940V
(CPU SPEC: 1.220V -> 0.930V)

1.67GHZ
1.320V -> 0.940V
(CPU SPEC: 1.280V -> 0.930V)

1.67GHZ
1.340V -> 0.940V
(CPU SPEC: 1.300V -> 0.930V)

1.67GHZ
1.370V -> 0.940V
(CPU SPEC: 1.330V -> 0.930V)

Keep trace fat (1.00-2.54 mm) and short!!



OUTPUT VOLTAGE

VDAC	D4=0	D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0	0
1.95	1.250	0	0	0	0	1
1.90	1.225	0	0	0	1	0
1.85	1.200	0	0	1	0	1
1.80	1.175	0	1	0	0	0
1.75	1.150	0	1	0	1	1
1.70	1.125	0	1	1	0	0
1.65	1.100	0	1	1	1	1
1.60	1.075	1	0	0	0	0
1.55	1.050	1	0	0	1	1
1.50	1.025	1	0	1	0	0
1.45	1.000	1	0	1	1	1
1.40	0.975	1	1	0	0	0
1.35	0.950	1	1	0	1	1
1.30	0.925	1	1	1	0	0
NO CPU	NO CPU	1	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ =	
	Hi/Fast	Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

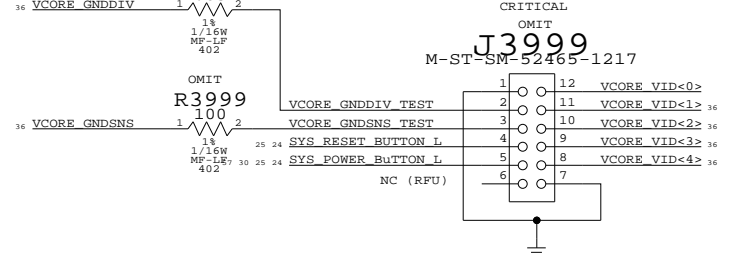
When A/B_ is high (fast): D4-D0 read as-is
 When A/B_ is low (slow): <=1K-ohm -> 0
 >=100K-ohm -> 1
 If all pull-ups are >=100K and all pull-downs are <=1K, V_A = V_B.

GROUND SENSE VOLTAGE DIVIDER
 This allows for an offset to the ground sense to adjust the output voltage.
 $V_{REF} = 2.0V$ WITH A 0.85 SCALE FACTOR, HENCE $V_{OFFSET} = 1.7V * (R1/(R1+R2))$ AND $V_{CORE} = V_{DAC} + V_{OFFSET}$.

NOTE: R3945 (R2) NO STUFFED FOR NO OFFSET CASE

ROUTE AS DIFFERENTIAL PAIR

FMAX CONNECTOR



CPU VCore Supply

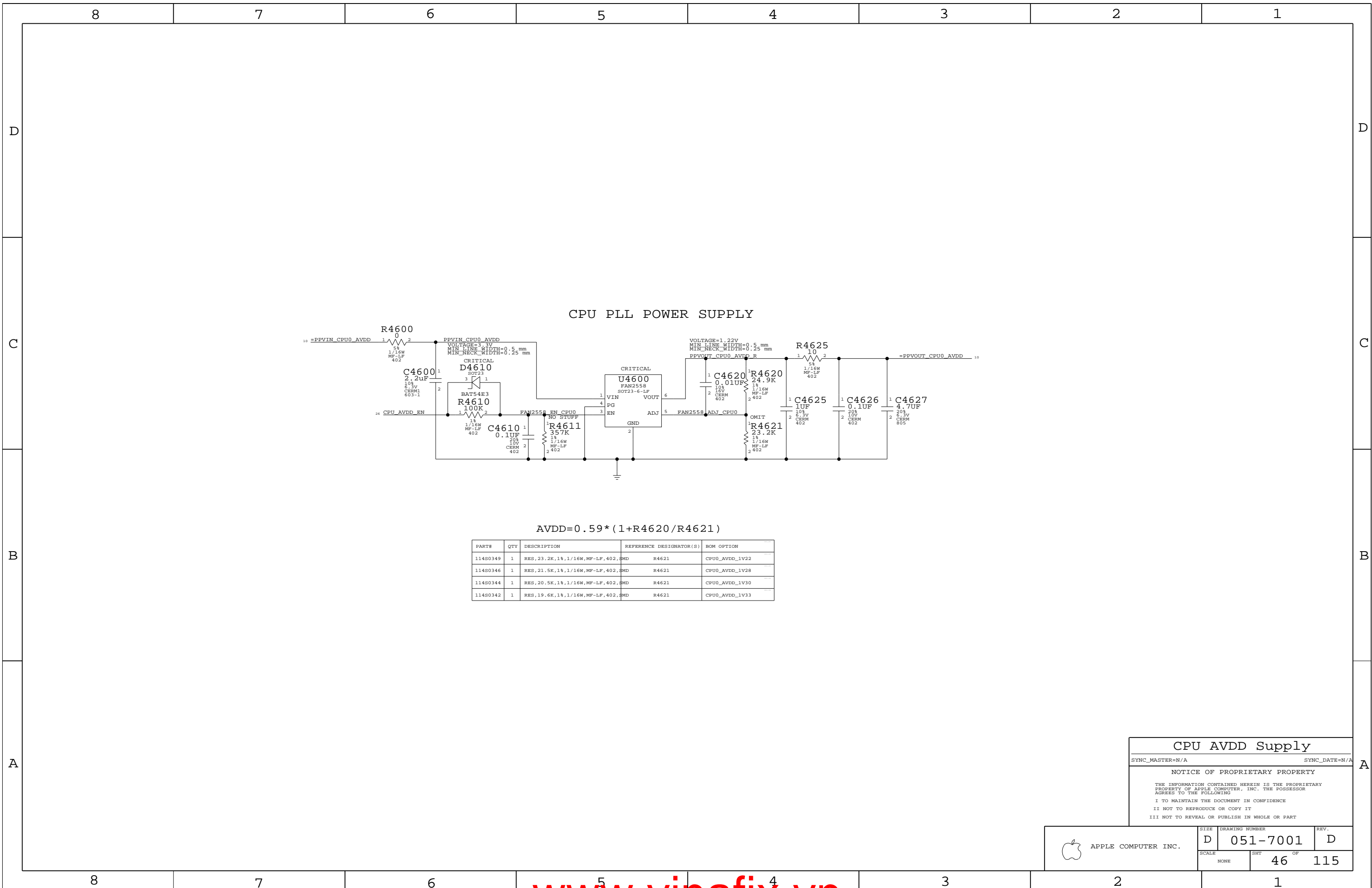
SYNC_MASTER=N/A SYNC_DATE=N/A

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SCALE	SHEET	OF
NONE	39	115



CPU PLL POWER SUPPLY

$$AVDD = 0.59 * (1 + R4620 / R4621)$$

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11480349	1	RES, 23.2K, 1%, 1/16W, MF-LF, 402, SMD	R4621	CPU0_AVDD_1V22
11480346	1	RES, 21.5K, 1%, 1/16W, MF-LF, 402, SMD	R4621	CPU0_AVDD_1V28
11480344	1	RES, 20.5K, 1%, 1/16W, MF-LF, 402, SMD	R4621	CPU0_AVDD_1V30
11480342	1	RES, 19.6K, 1%, 1/16W, MF-LF, 402, SMD	R4621	CPU0_AVDD_1V33

CPU AVDD Supply

SYNC_MASTER=N/A SYNC_DATE=N/A

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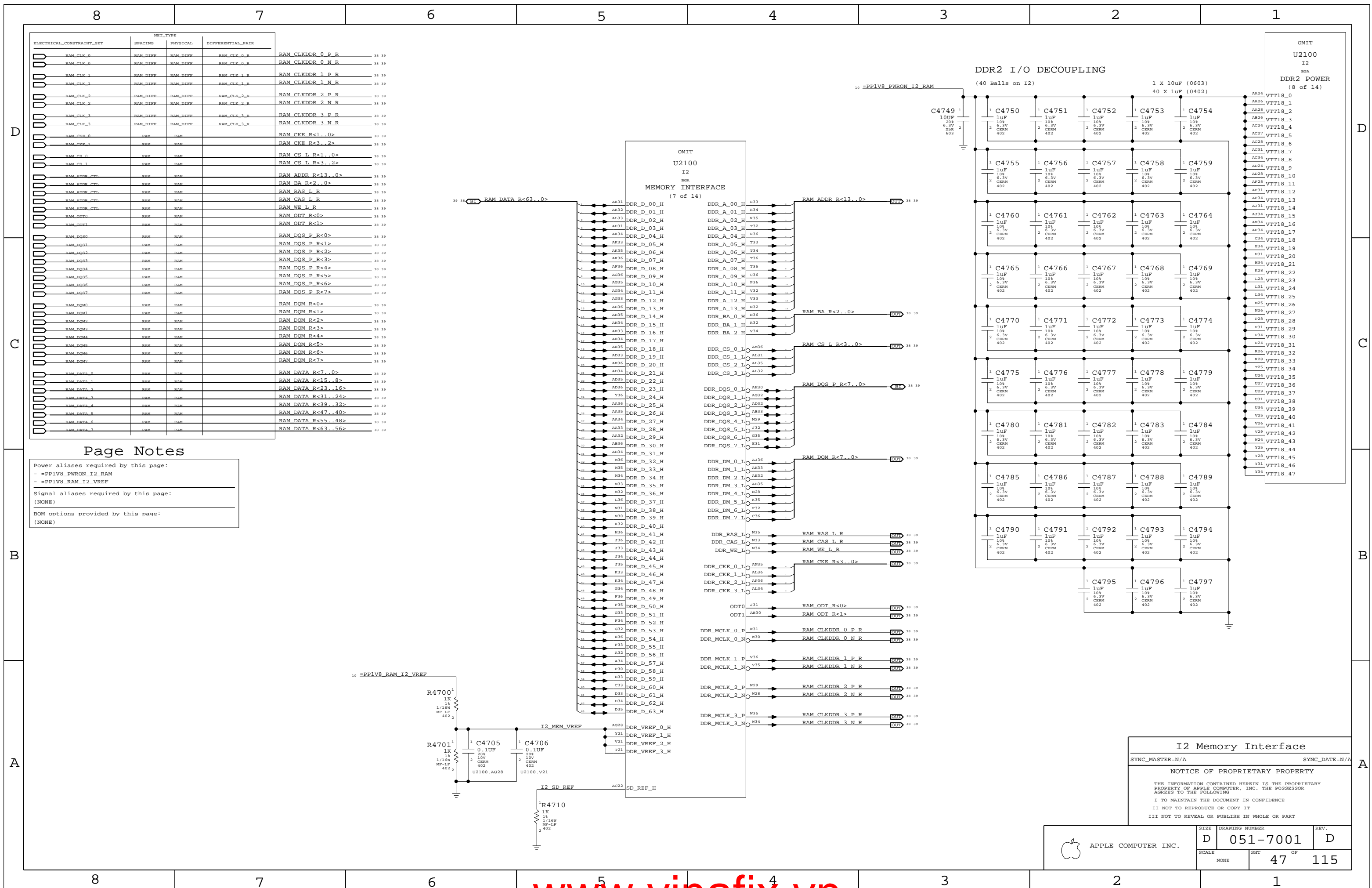
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SCALE	SHT OF		
NONE	46 OF		115



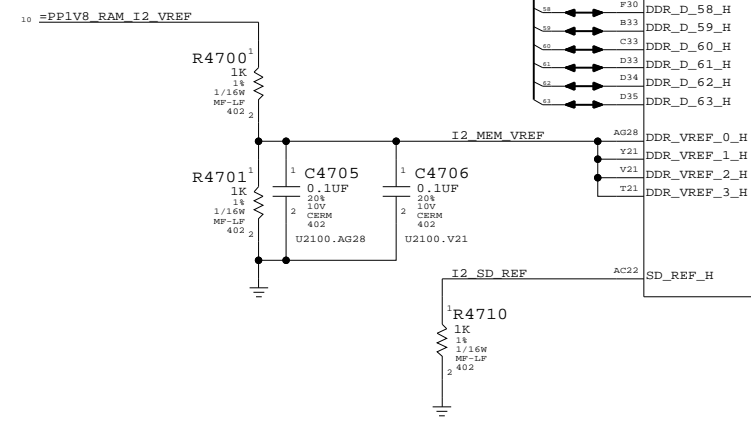
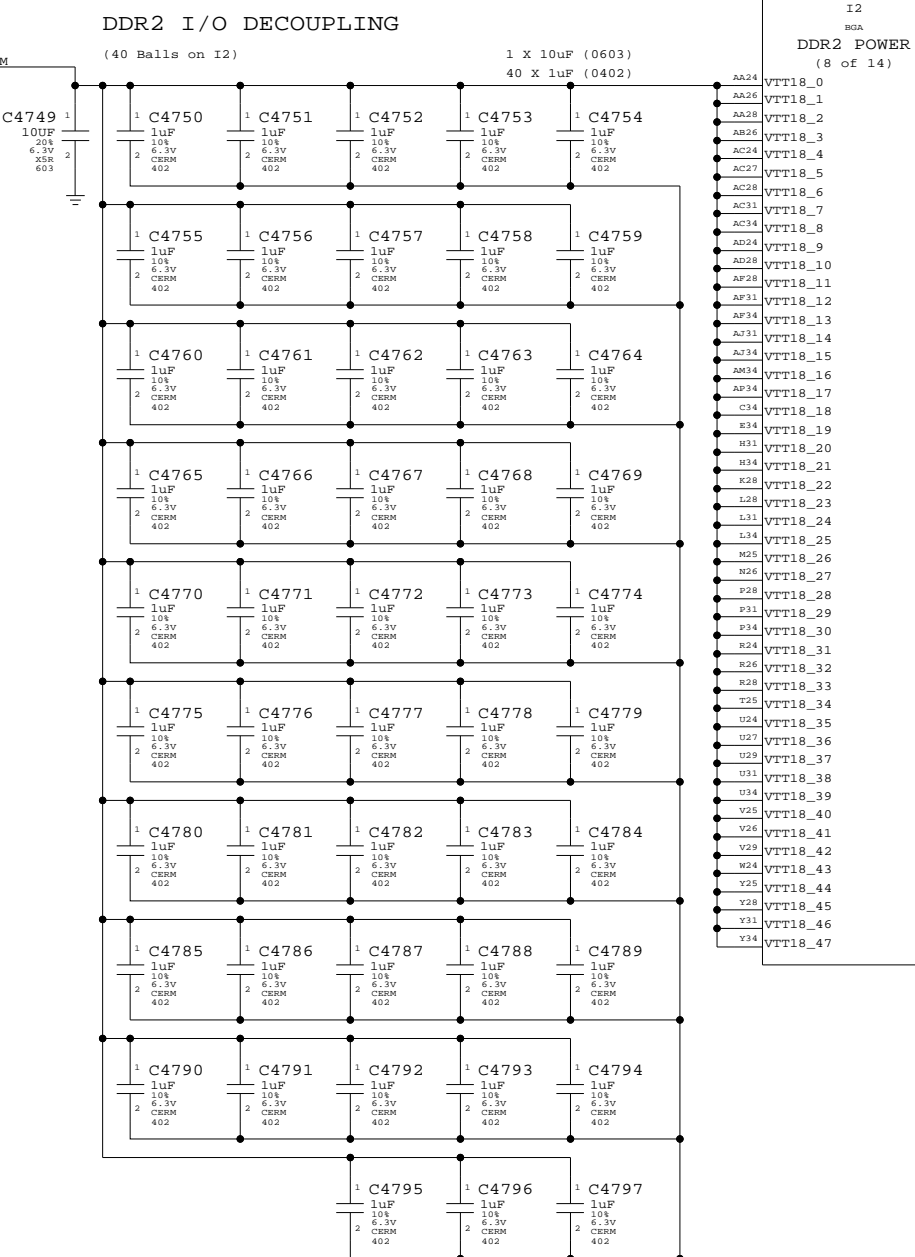
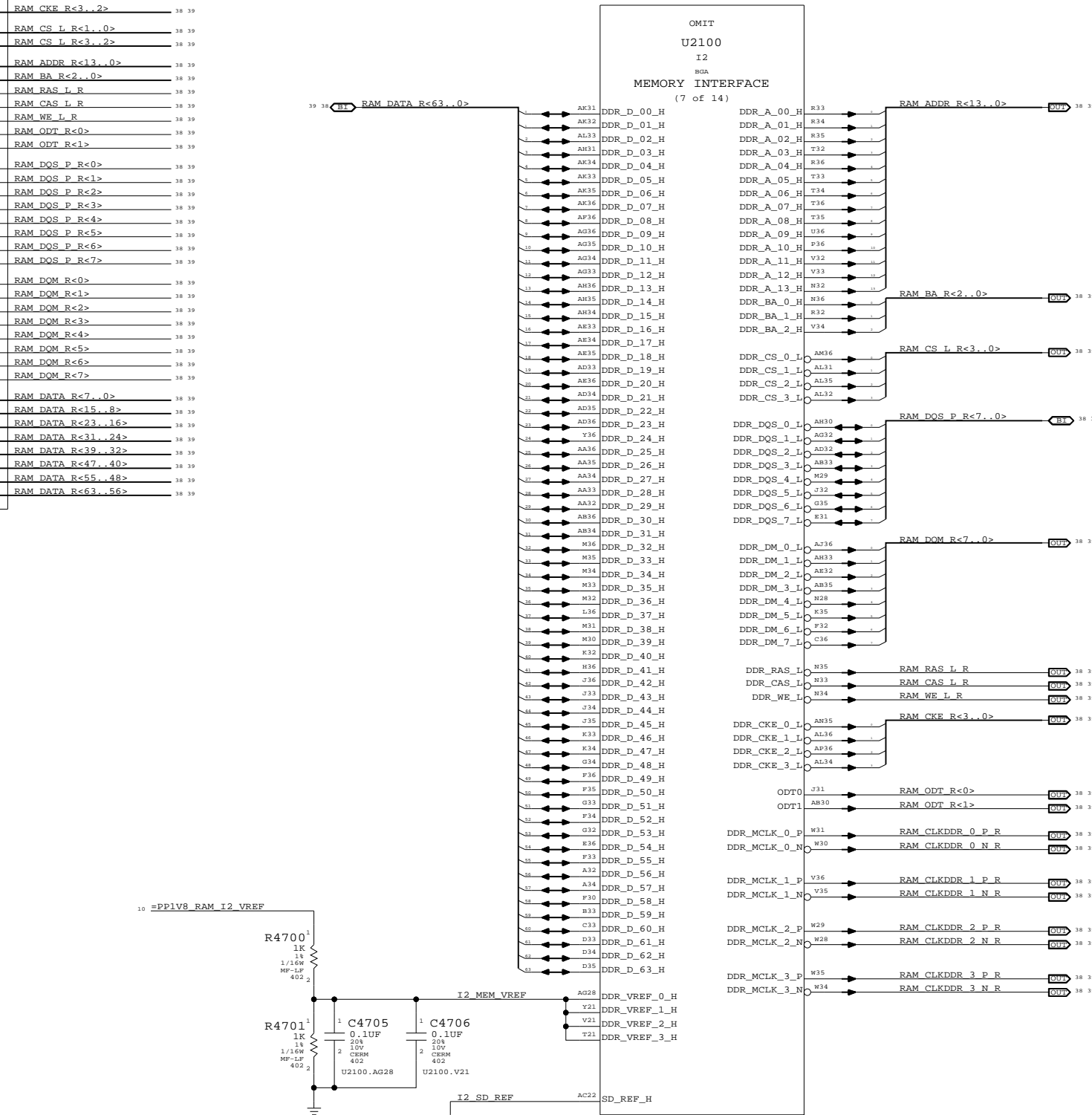
ELECTRICAL_CONSTRAINT_SET	NET_TYPE	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
RAM_CLK_0	RAM_DIFF	RAM_DIFF	RAM_CLK_0_R	RAM_CLKDDR_0_P_R
RAM_CLK_0	RAM_DIFF	RAM_DIFF	RAM_CLK_0_R	RAM_CLKDDR_0_N_R
RAM_CLK_1	RAM_DIFF	RAM_DIFF	RAM_CLK_1_R	RAM_CLKDDR_1_P_R
RAM_CLK_1	RAM_DIFF	RAM_DIFF	RAM_CLK_1_R	RAM_CLKDDR_1_N_R
RAM_CLK_2	RAM_DIFF	RAM_DIFF	RAM_CLK_2_R	RAM_CLKDDR_2_P_R
RAM_CLK_2	RAM_DIFF	RAM_DIFF	RAM_CLK_2_R	RAM_CLKDDR_2_N_R
RAM_CLK_3	RAM_DIFF	RAM_DIFF	RAM_CLK_3_R	RAM_CLKDDR_3_P_R
RAM_CLK_3	RAM_DIFF	RAM_DIFF	RAM_CLK_3_R	RAM_CLKDDR_3_N_R
RAM_CKE_0	RAM	RAM		RAM_CKE_R<1..0>
RAM_CKE_1	RAM	RAM		RAM_CKE_R<3..2>
RAM_CS_0	RAM	RAM		RAM_CS_L_R<1..0>
RAM_CS_1	RAM	RAM		RAM_CS_L_R<3..2>
RAM_ADDR_CTL	RAM	RAM		RAM_ADDR_R<13..0>
RAM_ADDR_CTL	RAM	RAM		RAM_BA_R<2..0>
RAM_ADDR_CTL	RAM	RAM		RAM_RAS_L_R
RAM_ADDR_CTL	RAM	RAM		RAM_CAS_L_R
RAM_ADDR_CTL	RAM	RAM		RAM_WE_L_R
RAM_ODT	RAM	RAM		RAM_ODT_R<0>
RAM_ODT	RAM	RAM		RAM_ODT_R<1>
RAM_DQS	RAM	RAM		RAM_DQS_P_R<0>
RAM_DQS	RAM	RAM		RAM_DQS_P_R<1>
RAM_DQS	RAM	RAM		RAM_DQS_P_R<2>
RAM_DQS	RAM	RAM		RAM_DQS_P_R<3>
RAM_DQS	RAM	RAM		RAM_DQS_P_R<4>
RAM_DQS	RAM	RAM		RAM_DQS_P_R<5>
RAM_DQS	RAM	RAM		RAM_DQS_P_R<6>
RAM_DQS	RAM	RAM		RAM_DQS_P_R<7>
RAM_DQM	RAM	RAM		RAM_DQM_R<0>
RAM_DQM	RAM	RAM		RAM_DQM_R<1>
RAM_DQM	RAM	RAM		RAM_DQM_R<2>
RAM_DQM	RAM	RAM		RAM_DQM_R<3>
RAM_DQM	RAM	RAM		RAM_DQM_R<4>
RAM_DQM	RAM	RAM		RAM_DQM_R<5>
RAM_DQM	RAM	RAM		RAM_DQM_R<6>
RAM_DQM	RAM	RAM		RAM_DQM_R<7>
RAM_DATA_0	RAM	RAM		RAM_DATA_R<7..0>
RAM_DATA_1	RAM	RAM		RAM_DATA_R<15..8>
RAM_DATA_2	RAM	RAM		RAM_DATA_R<23..16>
RAM_DATA_3	RAM	RAM		RAM_DATA_R<31..24>
RAM_DATA_4	RAM	RAM		RAM_DATA_R<39..32>
RAM_DATA_5	RAM	RAM		RAM_DATA_R<47..40>
RAM_DATA_6	RAM	RAM		RAM_DATA_R<55..48>
RAM_DATA_7	RAM	RAM		RAM_DATA_R<63..56>

Page Notes

Power aliases required by this page:
 - =PP1V8_PWRON_I2_RAM
 - =PP1V8_RAM_I2_VREF

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



I2 Memory Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

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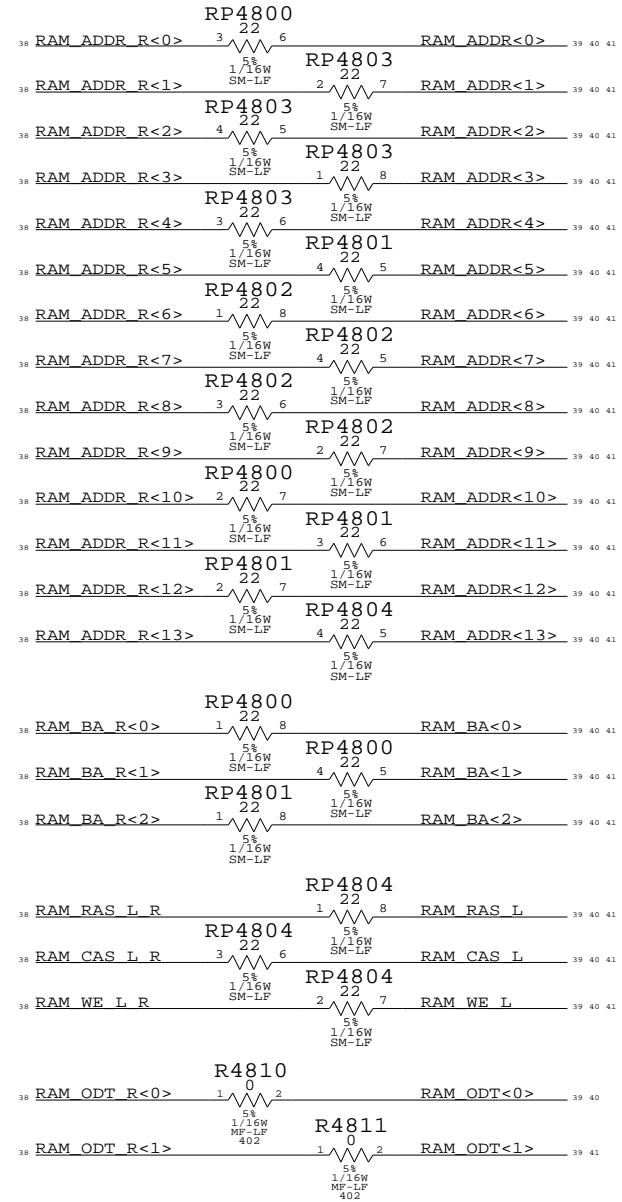
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NONE	47	115	

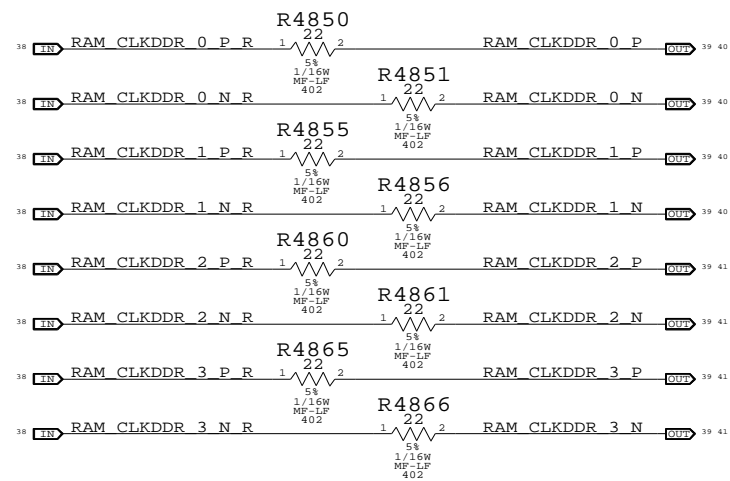
Main Memory Series Termination

SERIES RESISTORS FOR CONTROL SIGNALS

PINS ARE SWAPPABLE FOR RPAKS RP4800-RP4804

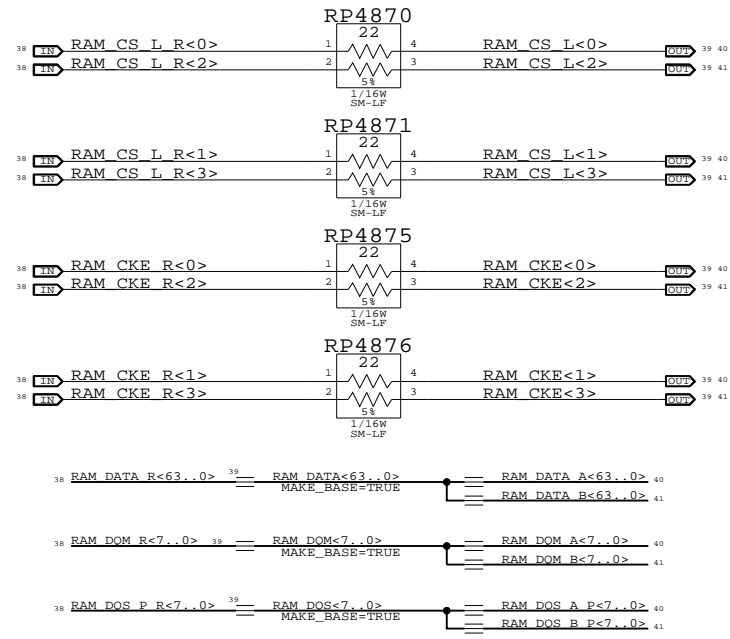


SERIES RESISTORS FOR CLOCKS



SERIES RESISTORS FOR CS / CKE

Do not swap with other RPAKs



ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
DIFF	RAM_DIFF	RAM_DIFF	RAM_CLK_0	RAM_CLKDDR_0_P 39 40
DIFF	RAM_DIFF	RAM_DIFF	RAM_CLK_0	RAM_CLKDDR_0_N 39 40
DIFF	RAM_DIFF	RAM_DIFF	RAM_CLK_1	RAM_CLKDDR_1_P 39 40
DIFF	RAM_DIFF	RAM_DIFF	RAM_CLK_1	RAM_CLKDDR_1_N 39 40
DIFF	RAM_DIFF	RAM_DIFF	RAM_CLK_2	RAM_CLKDDR_2_P 39 41
DIFF	RAM_DIFF	RAM_DIFF	RAM_CLK_2	RAM_CLKDDR_2_N 39 41
DIFF	RAM_DIFF	RAM_DIFF	RAM_CLK_3	RAM_CLKDDR_3_P 39 41
DIFF	RAM_DIFF	RAM_DIFF	RAM_CLK_3	RAM_CLKDDR_3_N 39 41
DIFF	RAM	RAM	RAM_CKE<3..0>	39 40 41
DIFF	RAM	RAM	RAM_CS L<3..0>	39 40 41
DIFF	RAM	RAM	RAM_ADDR<13..0>	39 40 41
DIFF	RAM	RAM	RAM_BA<2..0>	39 40 41
DIFF	RAM	RAM	RAM_RAS L	39 40 41
DIFF	RAM	RAM	RAM_CAS L	39 40 41
DIFF	RAM	RAM	RAM_WE L	39 40 41
DIFF	RAM	RAM	RAM_ODT<1..0>	39 40 41
DIFF	RAM	RAM	RAM_DOS<7..0>	39
DIFF	RAM	RAM	RAM_DOM<7..0>	39
DIFF	RAM	RAM	RAM_DATA<63..0>	39

ECSETS provided by memory controller.

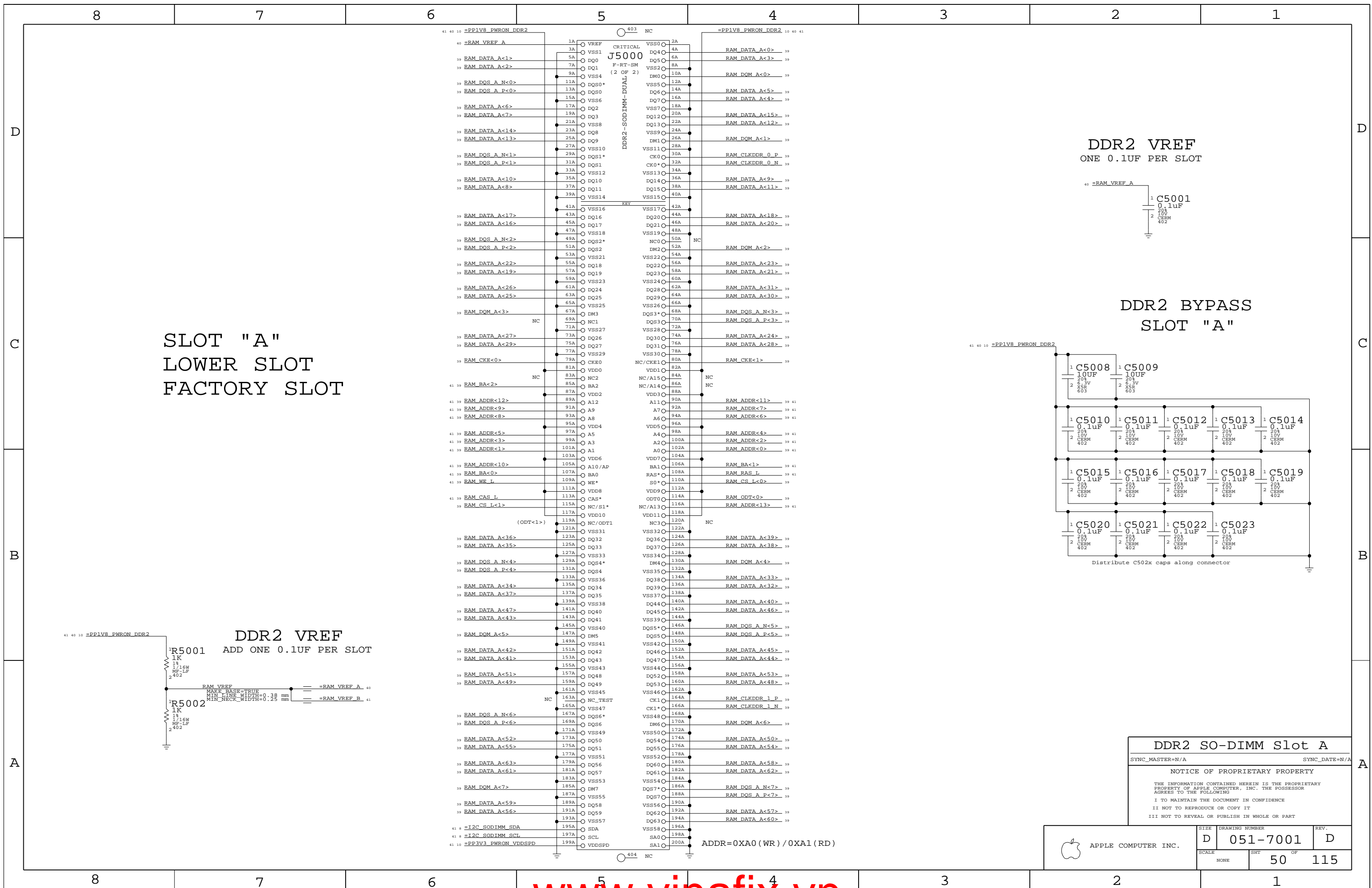
Memory Series Termination

SYNC_MASTER=N/A SYNC_DATE=N/A

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SCALE	NONE	SHT	OF
		48	115



SLOT "A"
LOWER SLOT
FACTORY SLOT

DDR2 VREF
ONE 0.1UF PER SLOT

DDR2 BYPASS
SLOT "A"

DDR2 VREF
ADD ONE 0.1UF PER SLOT

DDR2 SO-DIMM Slot A

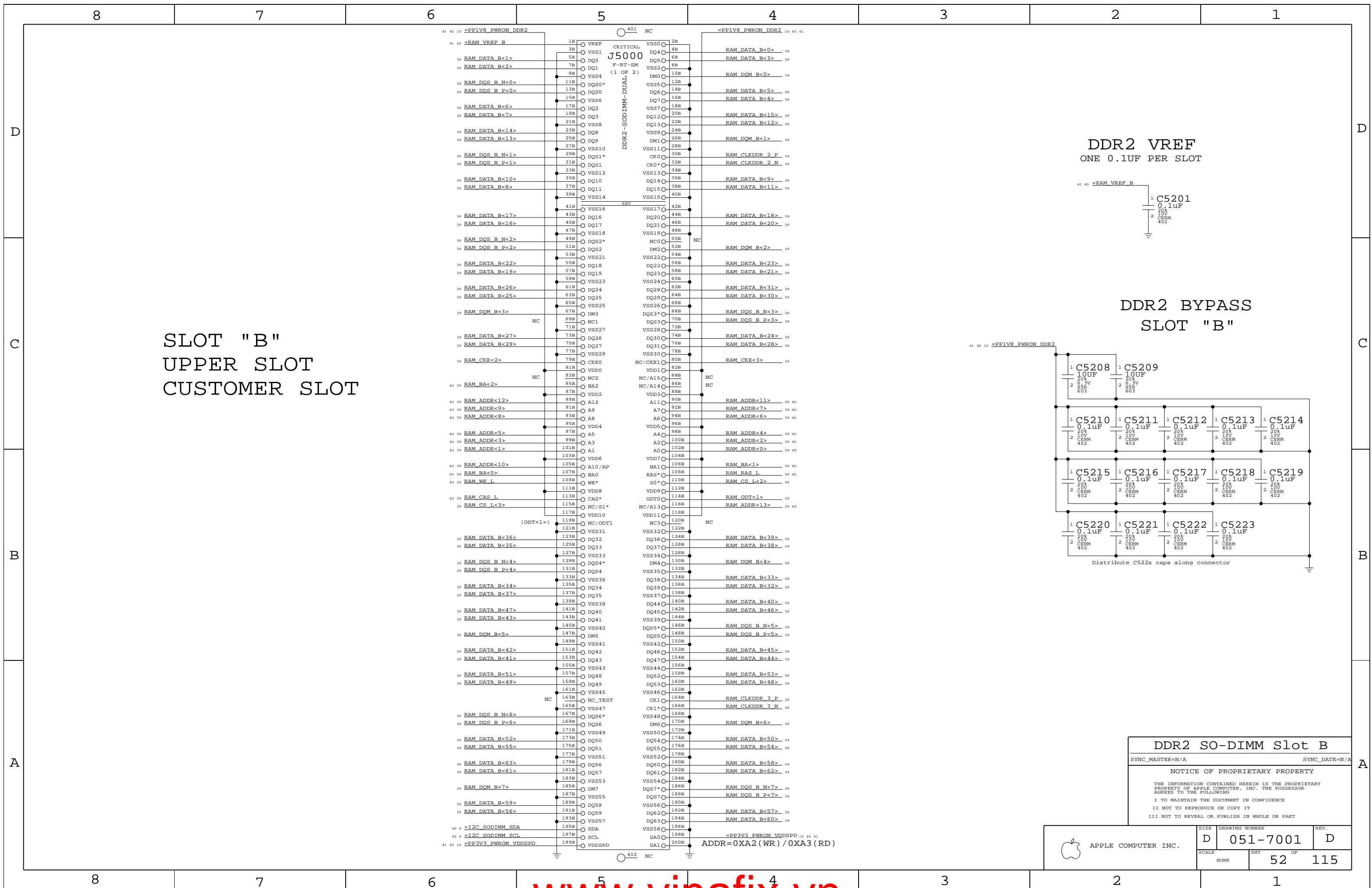
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SCALE	SHT OF		
NONE	50		115



SLOT "B"
UPPER SLOT
CUSTOMER SLOT

DDR2 VREF
ONE 0.1uF PER SLOT

DDR2 BYPASS
SLOT "B"

DDR2 SO-DIMM Slot B

SYNC_MASTER=N/A SYNC_DATE=N/A

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SCALE	NONE	SHT	OF
		52	115

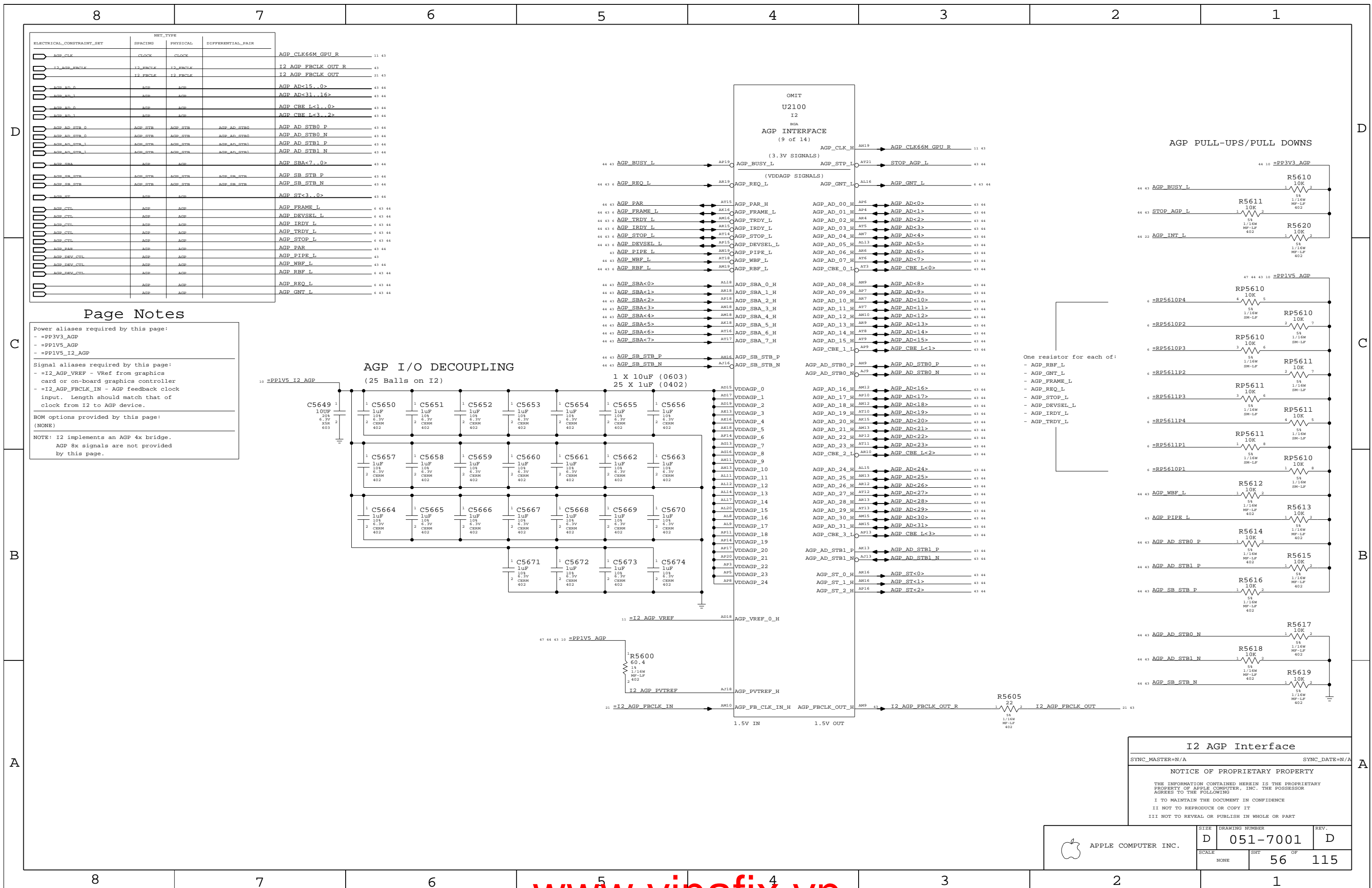


ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
R100	FB_A_CLK_0	SAM_DIFF	SAM_DIFF	FB_A_CLKDDR_0_P_R
R100	(provided above)	SAM_DIFF	SAM_DIFF	FB_A_CLKDDR_0_N_R
R100	FB_A_CLK_1	SAM_DIFF	SAM_DIFF	FB_A_CLKDDR_1_P_R
R100	(provided above)	SAM_DIFF	SAM_DIFF	FB_A_CLKDDR_1_N_R
R100	FB_A_ADDR_CTL	SAM	SAM	FB_A_CKE_R
R100	FB_A_ADDR_CTL	SAM	SAM	FB_A_CS_L_R
R100	FB_A_ADDR_CTL	SAM	SAM	FB_A_ADDR_R<12..0>
R100	FB_A_ADDR_CTL	SAM	SAM	FB_A_BA_R<2..0>
R100	FB_A_ADDR_CTL	SAM	SAM	FB_A_RAS_L_R
R100	FB_A_ADDR_CTL	SAM	SAM	FB_A_CAS_L_R
R100	FB_A_ADDR_CTL	SAM	SAM	FB_A_WE_L_R
R100	FB_A_DQS0	SAM	SAM	FB_A_DQS_R<0>
R100	FB_A_DQS1	SAM	SAM	FB_A_DQS_R<1>
R100	FB_A_DQS2	SAM	SAM	FB_A_DQS_R<2>
R100	FB_A_DQS3	SAM	SAM	FB_A_DQS_R<3>
R100	FB_A_DQS4	SAM	SAM	FB_A_DQS_R<4>
R100	FB_A_DQS5	SAM	SAM	FB_A_DQS_R<5>
R100	FB_A_DQS6	SAM	SAM	FB_A_DQS_R<6>
R100	FB_A_DQS7	SAM	SAM	FB_A_DQS_R<7>
R100	FB_A_DQM0	SAM	SAM	FB_A_DQM_R<0>
R100	FB_A_DQM1	SAM	SAM	FB_A_DQM_R<1>
R100	FB_A_DQM2	SAM	SAM	FB_A_DQM_R<2>
R100	FB_A_DQM3	SAM	SAM	FB_A_DQM_R<3>
R100	FB_A_DQM4	SAM	SAM	FB_A_DQM_R<4>
R100	FB_A_DQM5	SAM	SAM	FB_A_DQM_R<5>
R100	FB_A_DQM6	SAM	SAM	FB_A_DQM_R<6>
R100	FB_A_DQM7	SAM	SAM	FB_A_DQM_R<7>
R100	FB_A_DO0	SAM	SAM	FB_A_DO_R<7..0>
R100	FB_A_DO1	SAM	SAM	FB_A_DO_R<15..8>
R100	FB_A_DO2	SAM	SAM	FB_A_DO_R<23..16>
R100	FB_A_DO3	SAM	SAM	FB_A_DO_R<31..24>
R100	FB_A_DO4	SAM	SAM	FB_A_DO_R<39..32>
R100	FB_A_DO5	SAM	SAM	FB_A_DO_R<47..40>
R100	FB_A_DO6	SAM	SAM	FB_A_DO_R<55..48>
R100	FB_A_DO7	SAM	SAM	FB_A_DO_R<63..56>

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
R110	FB_B_CLK_0	SAM_DIFF	SAM_DIFF	FB_B_CLKDDR_0_P_R
R110	(provided above)	SAM_DIFF	SAM_DIFF	FB_B_CLKDDR_0_N_R
R110	FB_B_CLK_1	SAM_DIFF	SAM_DIFF	FB_B_CLKDDR_1_P_R
R110	(provided above)	SAM_DIFF	SAM_DIFF	FB_B_CLKDDR_1_N_R
R110	FB_B_ADDR_CTL	SAM	SAM	FB_B_CKE_R
R110	FB_B_ADDR_CTL	SAM	SAM	FB_B_CS_L_R
R110	FB_B_ADDR_CTL	SAM	SAM	FB_B_ADDR_R<12..0>
R110	FB_B_ADDR_CTL	SAM	SAM	FB_B_BA_R<2..0>
R110	FB_B_ADDR_CTL	SAM	SAM	FB_B_RAS_L_R
R110	FB_B_ADDR_CTL	SAM	SAM	FB_B_CAS_L_R
R110	FB_B_ADDR_CTL	SAM	SAM	FB_B_WE_L_R
R110	FB_B_DQS0	SAM	SAM	FB_B_DQS_R<0>
R110	FB_B_DQS1	SAM	SAM	FB_B_DQS_R<1>
R110	FB_B_DQS2	SAM	SAM	FB_B_DQS_R<2>
R110	FB_B_DQS3	SAM	SAM	FB_B_DQS_R<3>
R110	FB_B_DQS4	SAM	SAM	FB_B_DQS_R<4>
R110	FB_B_DQS5	SAM	SAM	FB_B_DQS_R<5>
R110	FB_B_DQS6	SAM	SAM	FB_B_DQS_R<6>
R110	FB_B_DQS7	SAM	SAM	FB_B_DQS_R<7>
R110	FB_B_DQM0	SAM	SAM	FB_B_DQM_R<0>
R110	FB_B_DQM1	SAM	SAM	FB_B_DQM_R<1>
R110	FB_B_DQM2	SAM	SAM	FB_B_DQM_R<2>
R110	FB_B_DQM3	SAM	SAM	FB_B_DQM_R<3>
R110	FB_B_DQM4	SAM	SAM	FB_B_DQM_R<4>
R110	FB_B_DQM5	SAM	SAM	FB_B_DQM_R<5>
R110	FB_B_DQM6	SAM	SAM	FB_B_DQM_R<6>
R110	FB_B_DQM7	SAM	SAM	FB_B_DQM_R<7>
R110	FB_B_DO0	SAM	SAM	FB_B_DO_R<7..0>
R110	FB_B_DO1	SAM	SAM	FB_B_DO_R<15..8>
R110	FB_B_DO2	SAM	SAM	FB_B_DO_R<23..16>
R110	FB_B_DO3	SAM	SAM	FB_B_DO_R<31..24>
R110	FB_B_DO4	SAM	SAM	FB_B_DO_R<39..32>
R110	FB_B_DO5	SAM	SAM	FB_B_DO_R<47..40>
R110	FB_B_DO6	SAM	SAM	FB_B_DO_R<55..48>
R110	FB_B_DO7	SAM	SAM	FB_B_DO_R<63..56>

M11 Frame Buffer Constraints
 SYNC_MASTER=N/A SYNC_DATE=N/A
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		SHT	OF
		55	115



ELECTRICAL_CONSTRAINT_SET	NET_TYPE	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
	CLOCK		CLOCK		AGP_CLK66M_GPU_R 11 43
	I2_FBCLK		I2_FBCLK		I2_AGP_FBCLK_OUT_R 43
	I2_FBCLK		I2_FBCLK		I2_AGP_FBCLK_OUT 21 43
	AGP		AGP		AGP_AD<15..0> 43 44
	AGP		AGP		AGP_AD<31..16> 43 44
	AGP		AGP		AGP_CBE_L<1..0> 43 44
	AGP		AGP		AGP_CBE_L<3..2> 43 44
	AGP_STB		AGP_STB		AGP_AD_STB0_P 43 44
	AGP_STB		AGP_STB		AGP_AD_STB0_N 43 44
	AGP_STB		AGP_STB		AGP_AD_STB1_P 43 44
	AGP_STB		AGP_STB		AGP_AD_STB1_N 43 44
	AGP_SBA		AGP_SBA		AGP_SBA<7..0> 43 44
	AGP_SBA		AGP_SBA		AGP_SB_STB_P 43 44
	AGP_SBA		AGP_SBA		AGP_SB_STB_N 43 44
	AGP_ST		AGP_ST		AGP_ST<3..0> 43 44
	AGP		AGP		AGP_FRAME_L 6 43 44
	AGP		AGP		AGP_DEVSEL_L 6 43 44
	AGP		AGP		AGP_TRDY_L 6 43 44
	AGP		AGP		AGP_STOP_L 6 43 44
	AGP		AGP		AGP_DEVSEL_L 6 43 44
	AGP		AGP		AGP_PAR 43 44
	AGP		AGP		AGP_PIPE_L 43
	AGP		AGP		AGP_WBF_L 43 44
	AGP		AGP		AGP_RBF_L 43 44
	AGP		AGP		AGP_REQ_L 6 43 44
	AGP		AGP		AGP_GNT_L 6 43 44

Page Notes

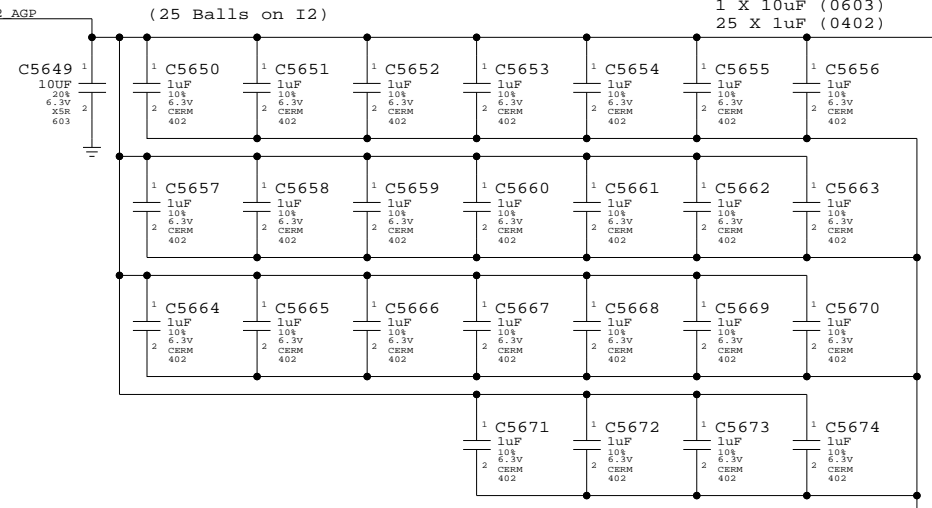
Power aliases required by this page:
 - =PP3V3_AGP
 - =PP1V5_AGP
 - =PP1V5_I2_AGP

Signal aliases required by this page:
 - =I2_AGP_VREF - VRef from graphics card or on-board graphics controller
 - =I2_AGP_FBCLK_IN - AGP feedback clock input. Length should match that of clock from I2 to AGP device.

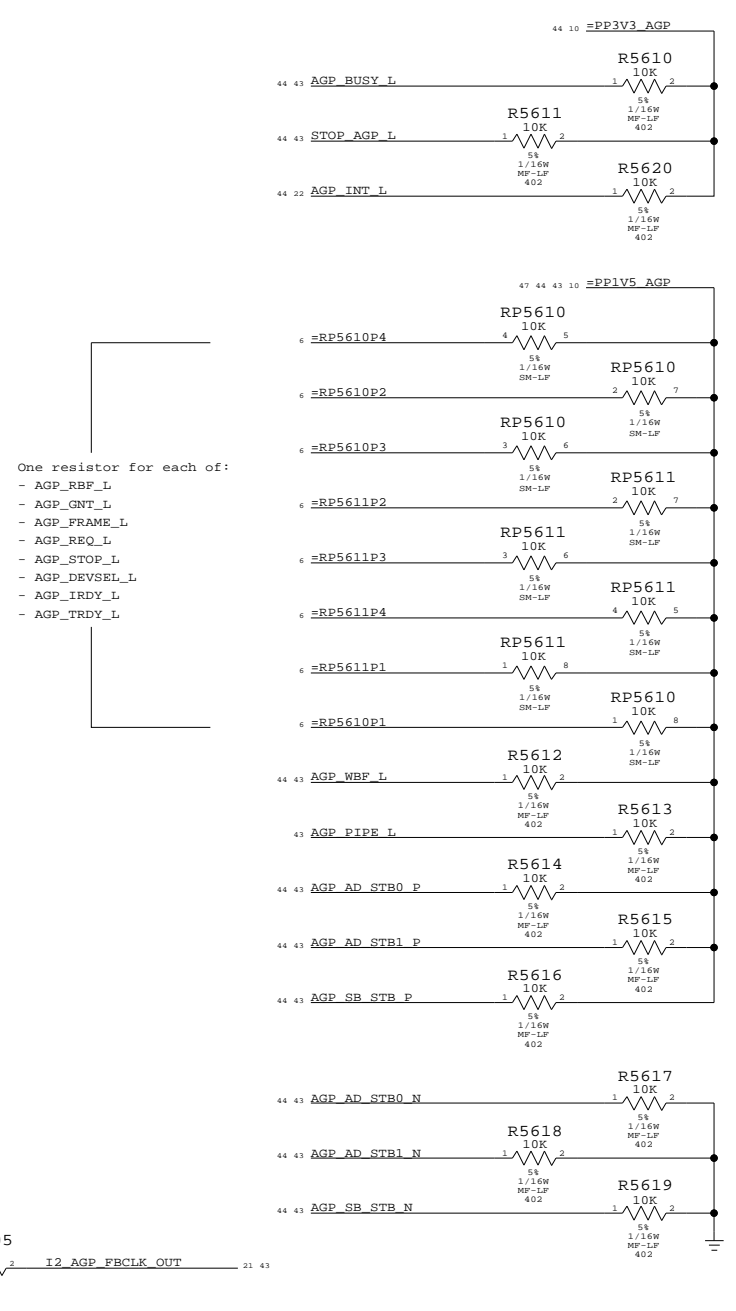
BOM options provided by this page:
 (NONE)

NOTE: I2 implements an AGP 4x bridge. AGP 8x signals are not provided by this page.

AGP I/O DECOUPLING
(25 Balls on I2)



AGP PULL-UPS/PULL DOWNS



One resistor for each of:
 - AGP_RBF_L
 - AGP_GNT_L
 - AGP_FRAME_L
 - AGP_STOP_L
 - AGP_DEVSEL_L
 - AGP_TRDY_L

I2 AGP Interface
 SYNC_MASTER=N/A SYNC_DATE=N/A

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NONE	56	115	

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
770	CLOCK	CLOCK	

AGP_CLK66M_GPU 11 44

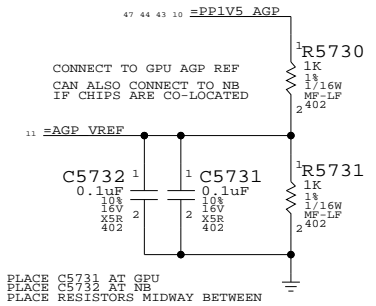
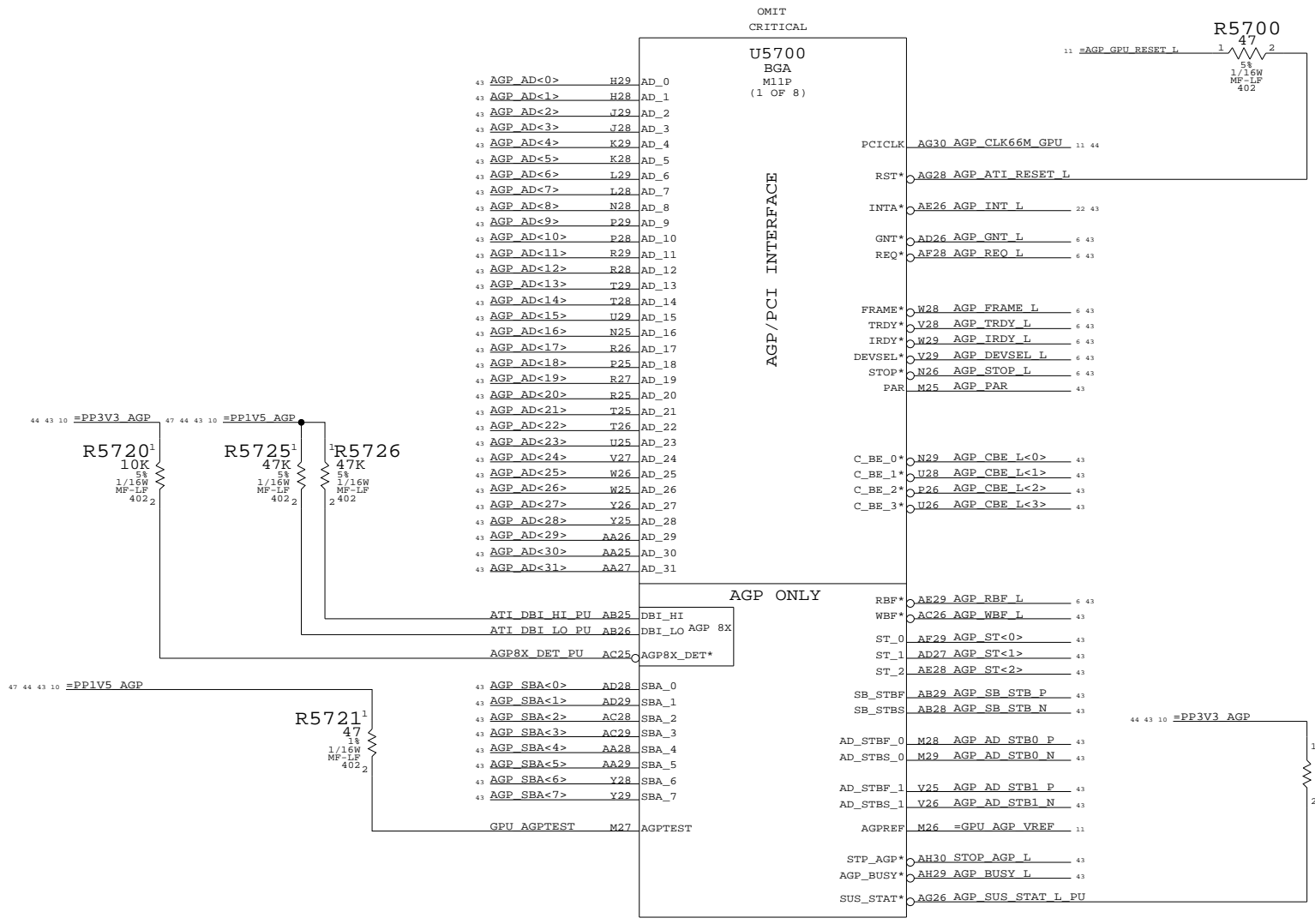
Page Notes

Power aliases required by this page:
 - =PP3V3_AGP
 - =PP1V5_AGP

Signal aliases required by this page:
 - =AGP_VREF - Vref divider output for both GPU and NB
 - =AGP_GPU_RESET_L - Active low reset for GPU

BOM options provided by this page:
 (NONE)

NOTE: AGP 8x signals are not provided by this page.



GPU (M11) AGP Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

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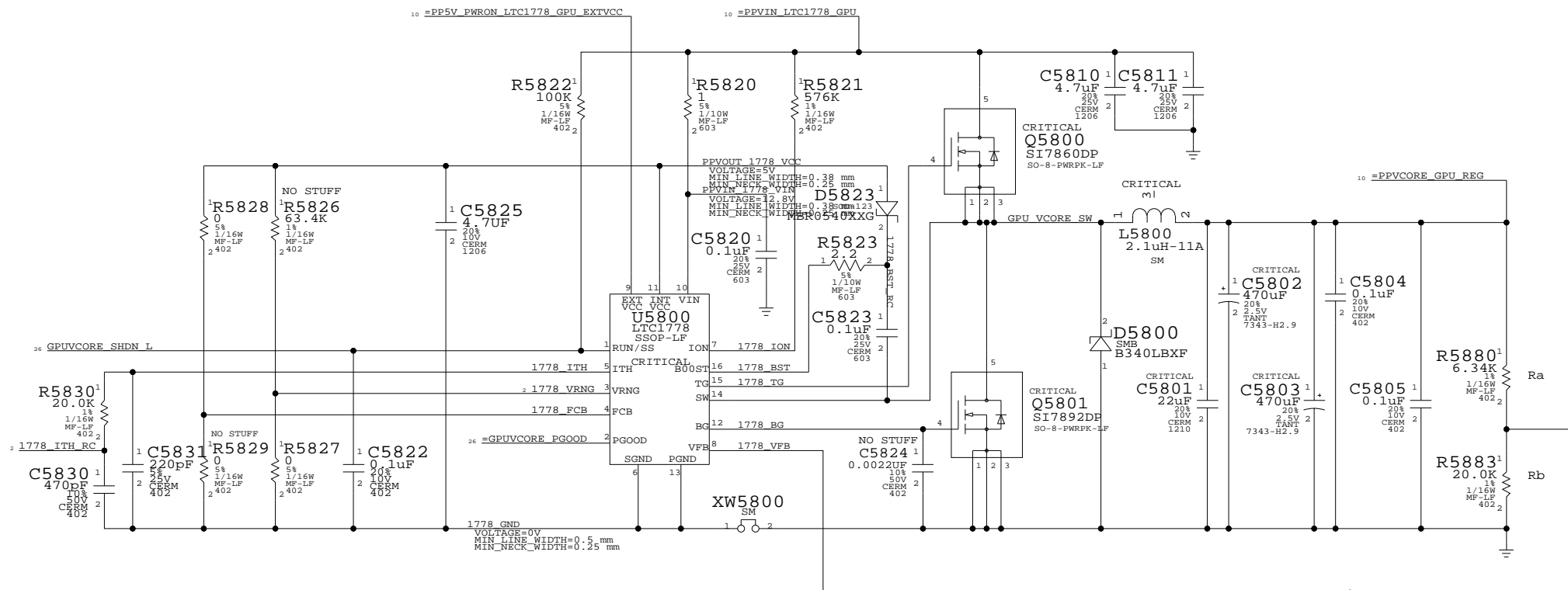
Power aliases required by this page:
 - =PPVIN_LTC1778_GPU
 - =PP5V_PWRON_LTC1778_GPU_EXTVCC
 - =PPVCORE_GPU_REG

Signal aliases required by this page:
 - =GPUVCORE_PGOOD - Active high Power Good signal for power sequencing

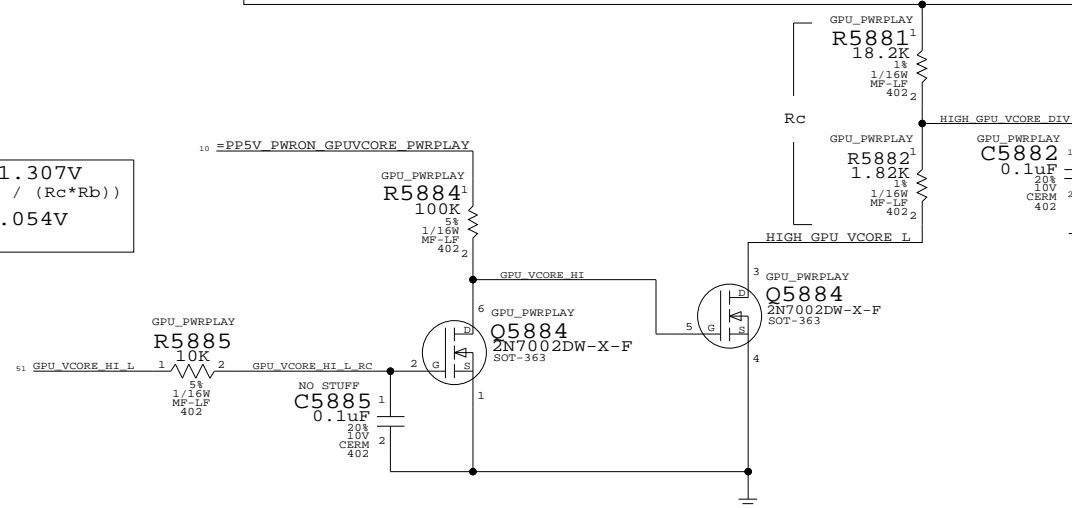
BOM options provided by this page:
 - GPU_PWRPLAY

NOTE: Implements "Power Miser" feature for ATI GPUs

GPU VCore SUPPLY



WHEN VCORE_CNTL HIGH => 1.307V
 $1.307V = 0.8V * (1 + Ra*(Rc+Rb) / (Rc*Rb))$
 WHEN VCORE_CNTL LOW => 1.054V
 $1.054V = 0.8V * (1 + Ra / Rb)$



GPU VCore Supply

SYNC_MASTER=N/A SYNC_DATE=N/A

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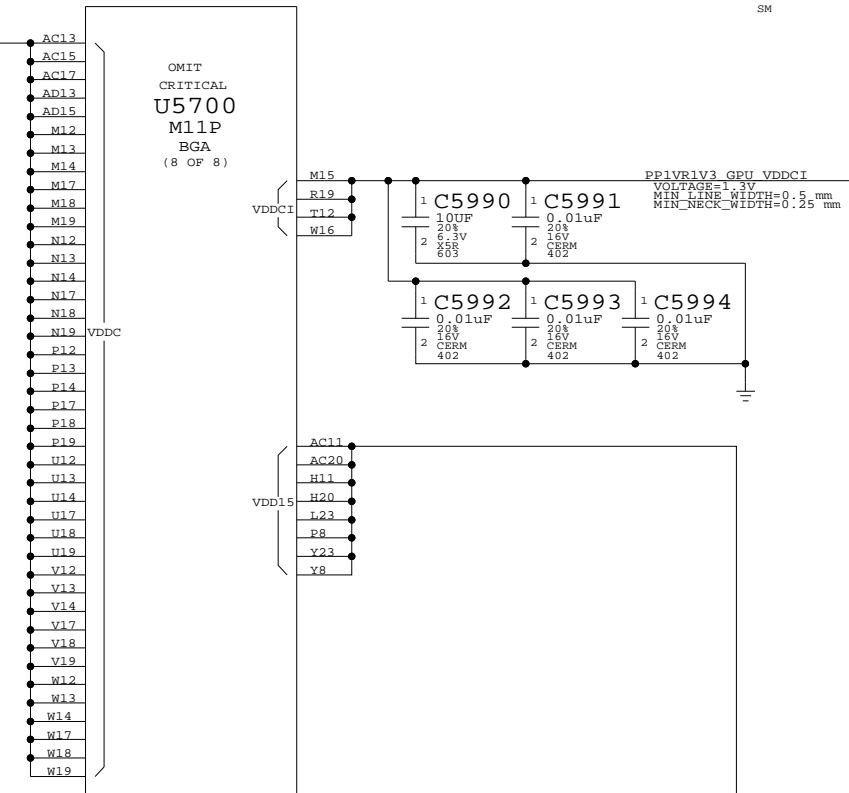
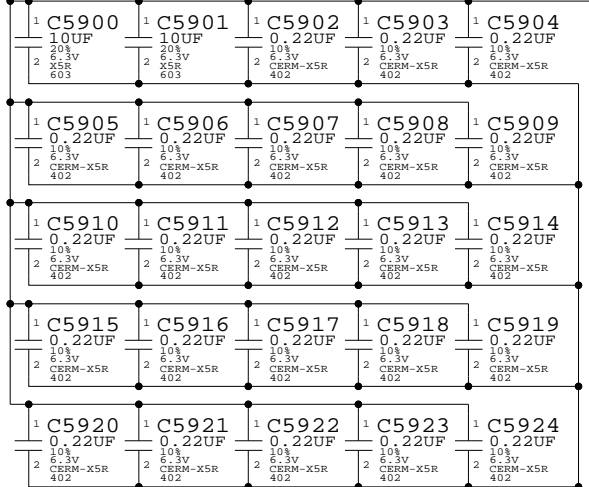
Power aliases required by this page:
 - =PPIV5_GPU_VDD15
 - =PPIV1V3_GPU_VCORE

Signal aliases required by this page:
 (NONE)

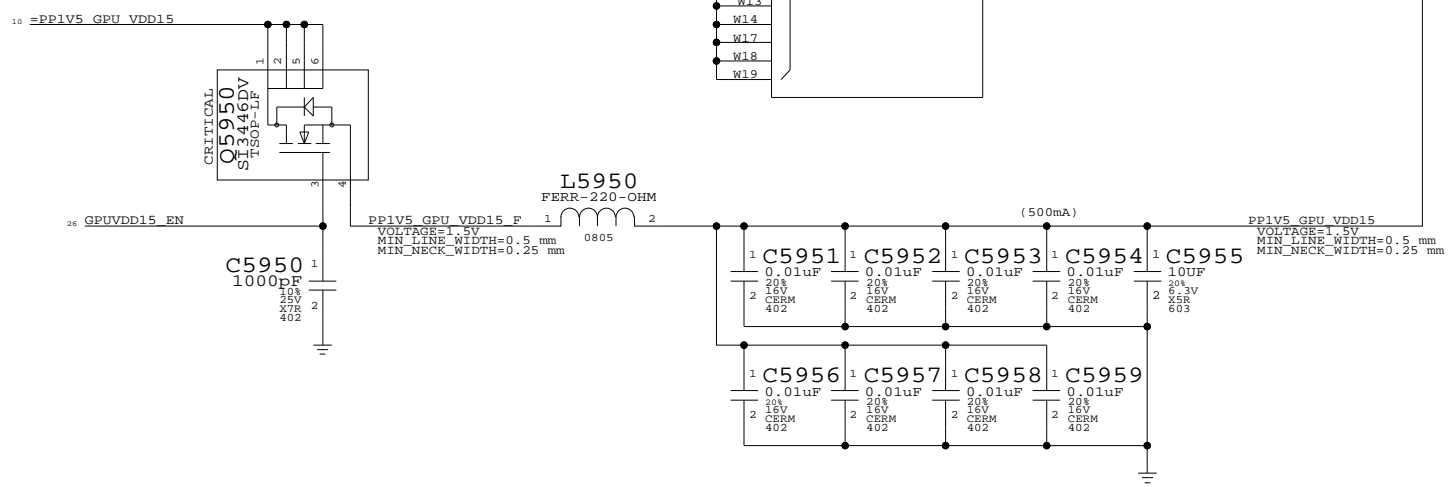
BOM options provided by this page:
 (NONE)

GPU VCORE - 1.3V/1.05V

Internal I/O - 1.3V/1.05V



Internal I/O - 1.5V

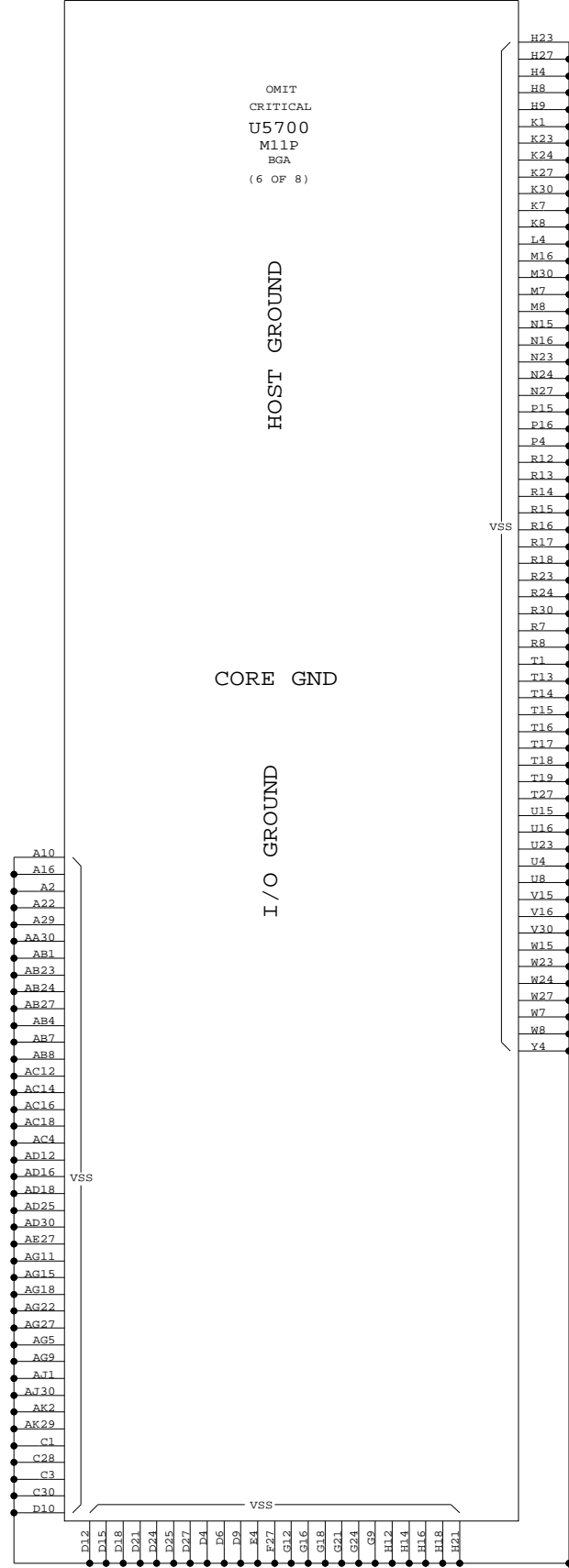


OMIT CRITICAL U5700 M11P BGA (6 OF 8)

HOST GROUND

CORE GND

I/O GROUND



GPU (M11) Core Power

SYNC_MASTER=N/A SYNC_DATE=N/A

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SCALE	NONE	SHT	OF
		59	115

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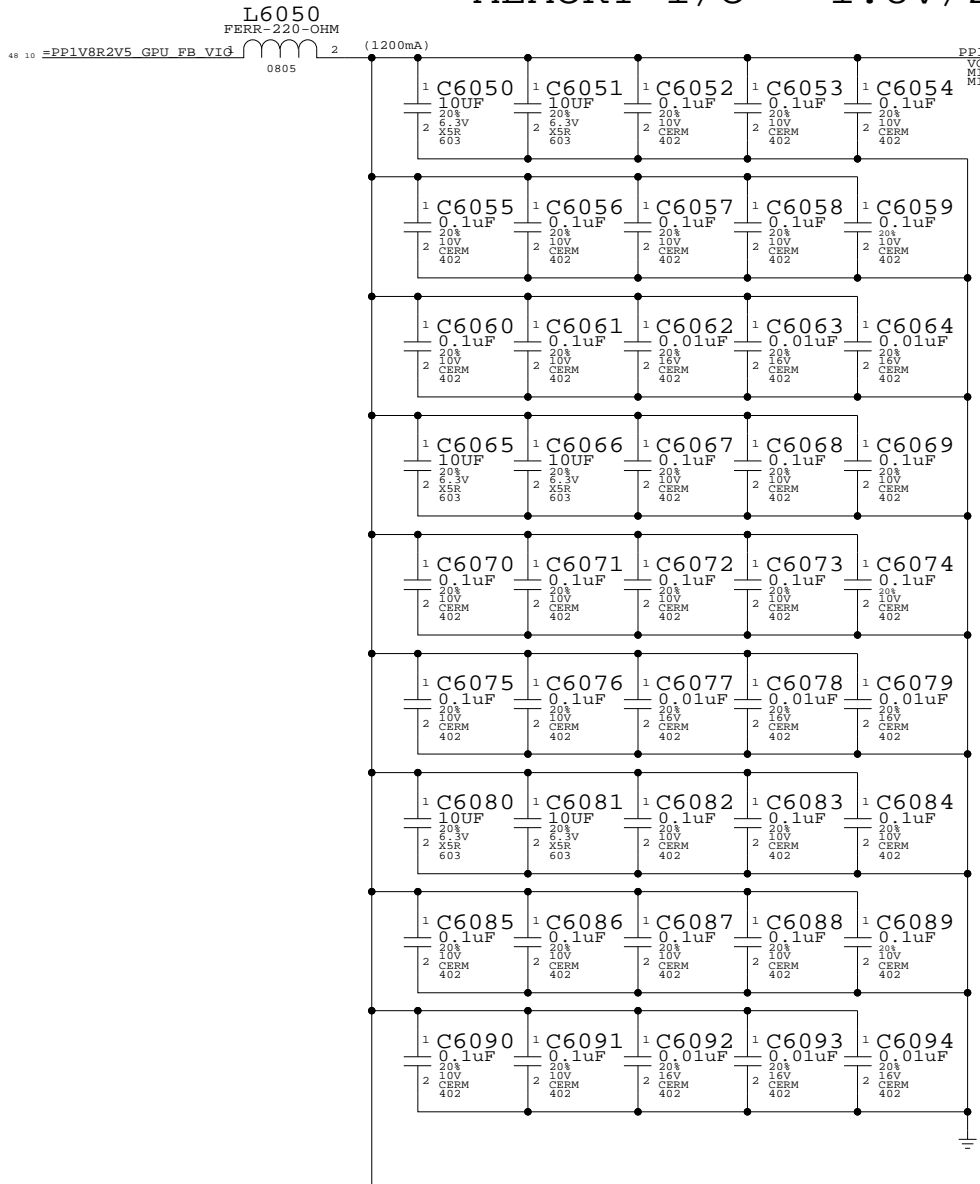
Power aliases required by this page:
 - =PP1V8R2V5_GPU_FB_VIO - =PP1V8_GPU_PANEL_IO
 - =PP3V3_GPU_VDDR3 - =PP1V8_GPU_LVDS_PLL
 - =PP1V5_GPU_DVO - =PP2V5_GPU_LVDS_IO
 - =PP1V8_GPU_DVO - =PP2V5_GPU_LVDS_IO
 - =PP1V5R3V3_DVO_VREF - =PP1V5_AGP

Signal aliases required by this page:
 (NONE)

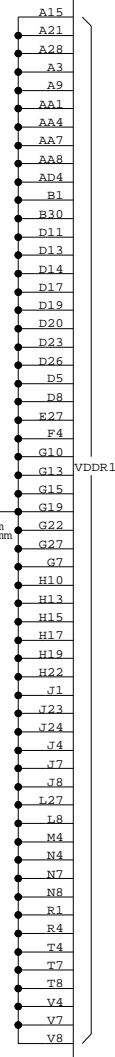
BOM options provided by this page:
 - DVO_1V5 - GPU_LVDDR_2V5
 - DVO_1V8 - GPU_LVDDR_2V8

NOTE: Implements a low-swing DVO bus only

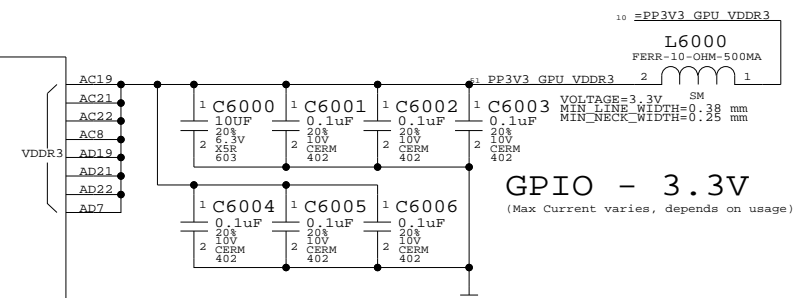
MEMORY I/O - 1.8V/2.5V



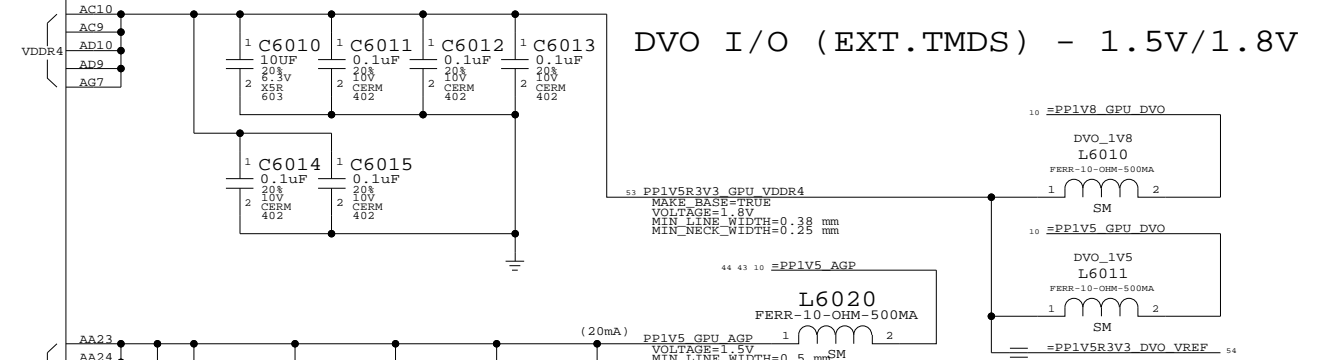
OMIT
 CRITICAL
 U5700
 M11P
 BGA
 (7 OF 8)



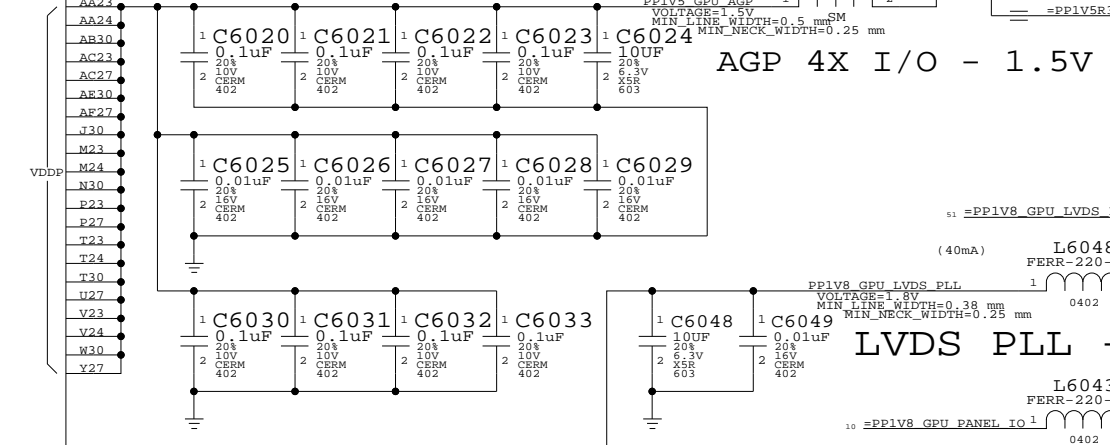
GPIO - 3.3V
 (Max Current varies, depends on usage)



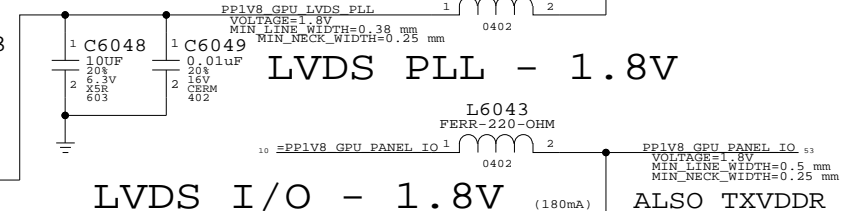
DVO I/O (EXT.TMDS) - 1.5V/1.8V



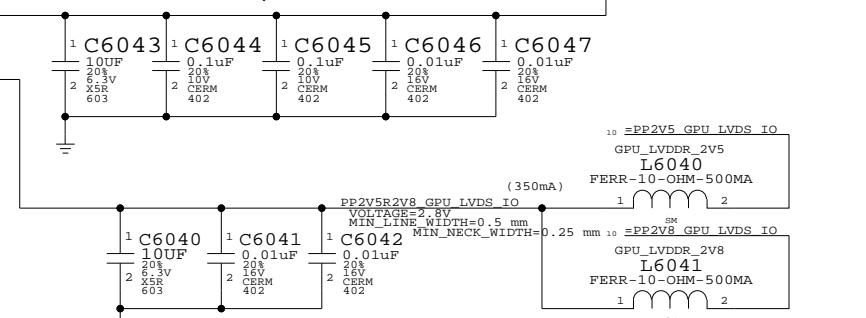
AGP 4X I/O - 1.5V



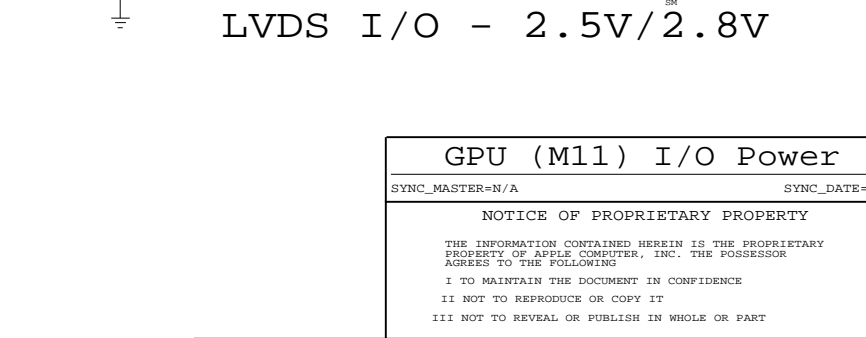
LVDS PLL - 1.8V



LVDS I/O - 1.8V
 (180mA) ALSO TXVDDR



LVDS I/O - 2.5V/2.8V



GPU (M11) I/O Power

SYNC_MASTER=N/A SYNC_DATE=N/A

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SCALE	NONE	SHT OF	60 115

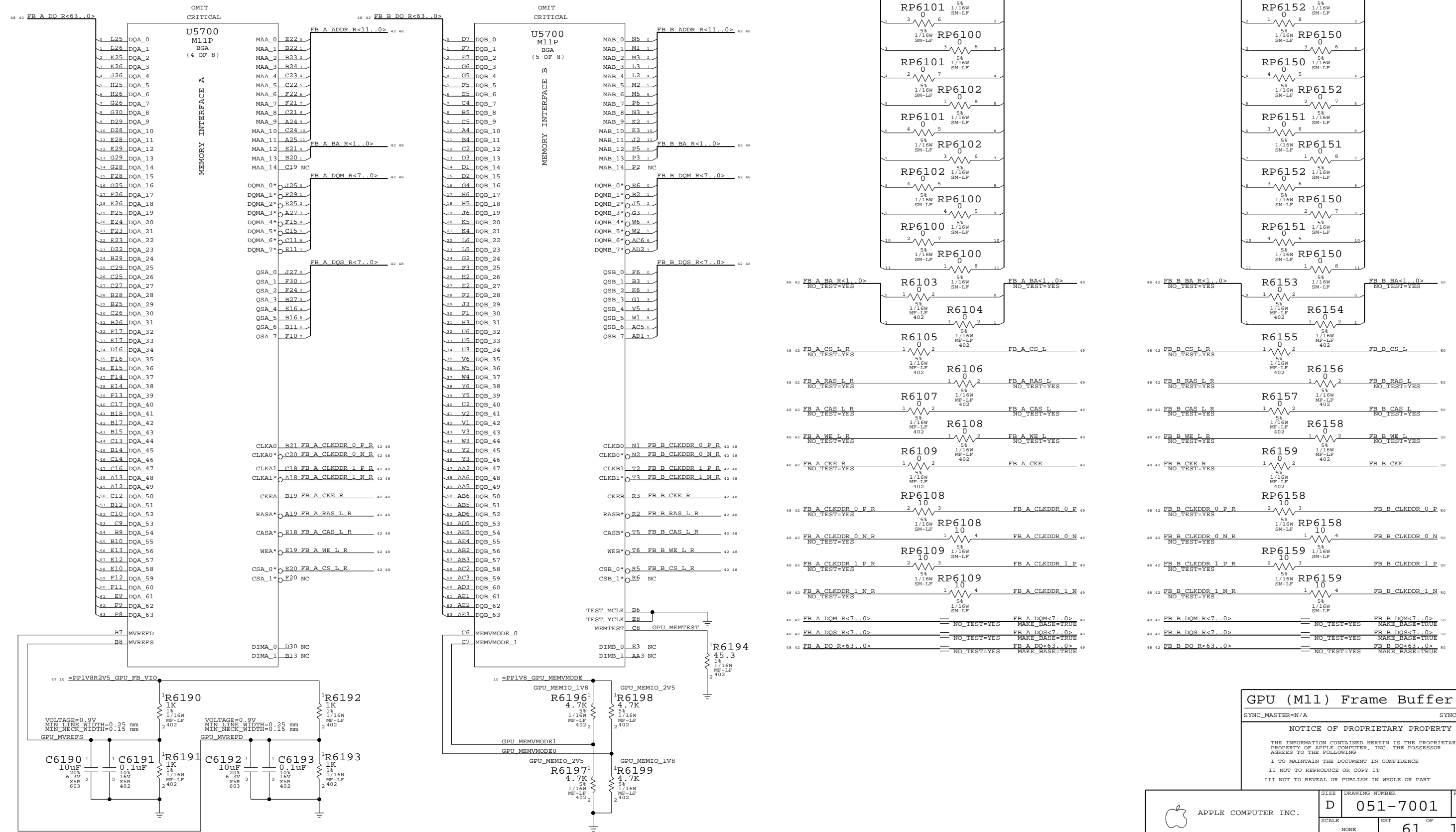
Page Notes

Power aliases required by this page:
 - =PP1V8R2V5_GPU_FB_VIO
 - =PP1V8_GPU_MEMVMODE

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - GPU_MEMIO_1V8
 - GPU_MEMIO_2V5

GPU Frame Buffer Series Term



GPU (M11) Frame Buffer I/F

SYNC_MASTER=N/A SYNC_DATE=N/A

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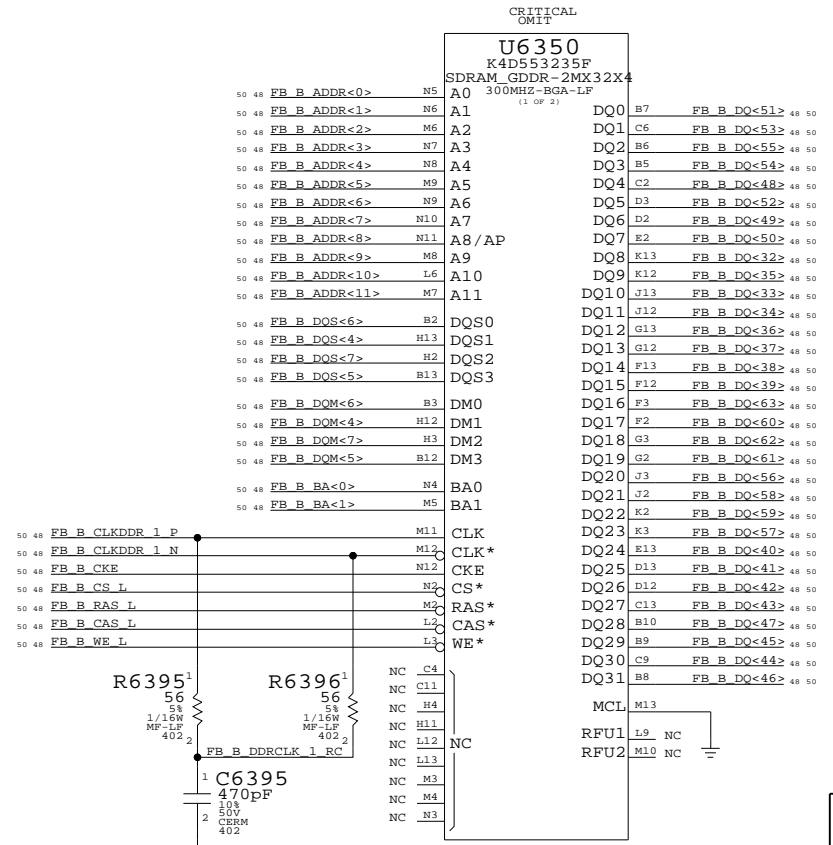
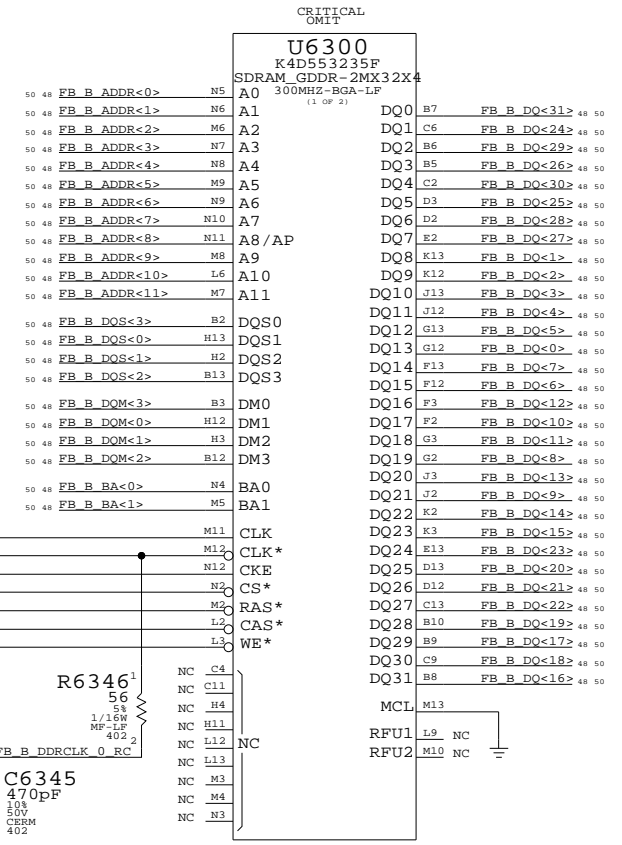
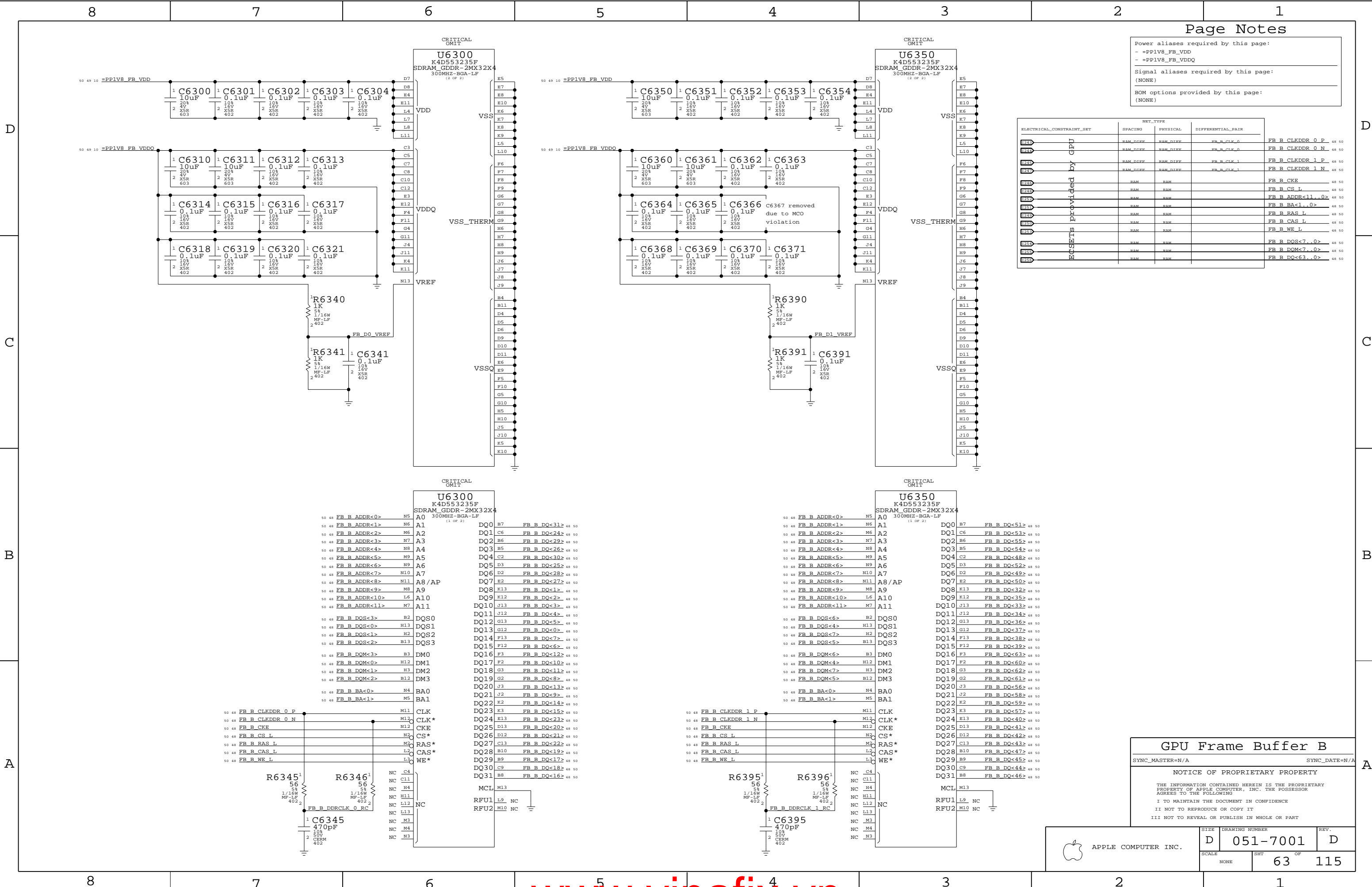
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7001	D
SCALE	NONE	SHT	OF
		61	115

Power aliases required by this page:
- =PPIV8_FB_VDD
- =PPIV8_FB_VDDQ
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)

Table with columns: ELECTRICAL_CONSTRAINT_SET, SPACING, PHYSICAL, DIFFERENTIAL_PAIR. Lists constraints like FB_B_CLK_0_P, FB_B_CLK_0_N, etc.



GPU Frame Buffer B
SYNC_MASTER=N/A SYNC_DATE=N/A
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Table with columns: SIZE, DRAWING NUMBER, REV., SCALE, SHEET OF. Values: D, 051-7001, D, NONE, 63 OF 115.

Page Notes

Power aliases required by this page:
 - =PP3V3_GPU_GPIOS
 - =PP2V5_PVDD
 - =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
 - =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
 - =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
 (NONE)

D

D

C

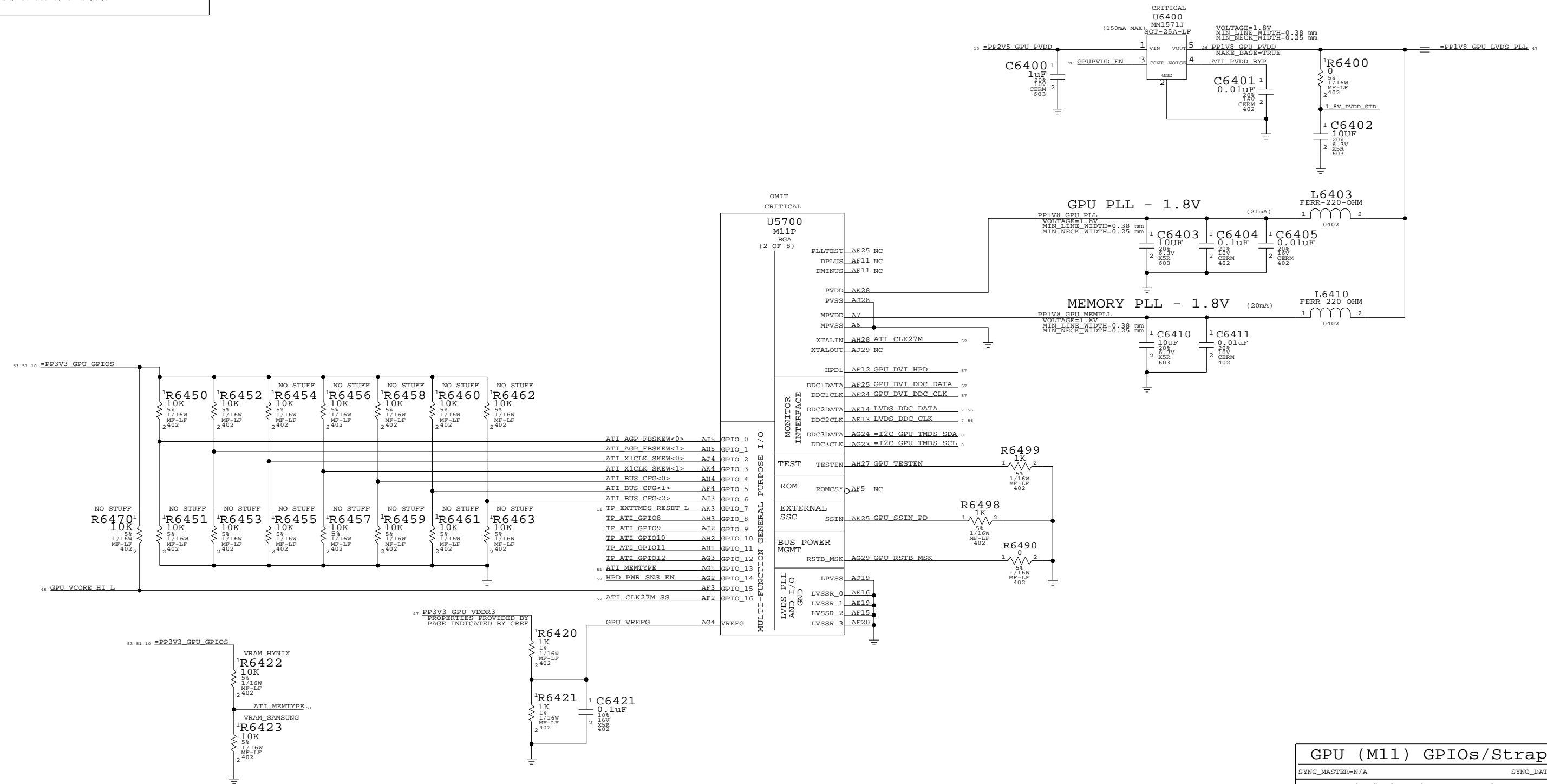
C

B

B

A

A



GPU (M11) GPIOs/Straps

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7001	D
SCALE	SHT	OF	
NONE	64	115	

Page Notes

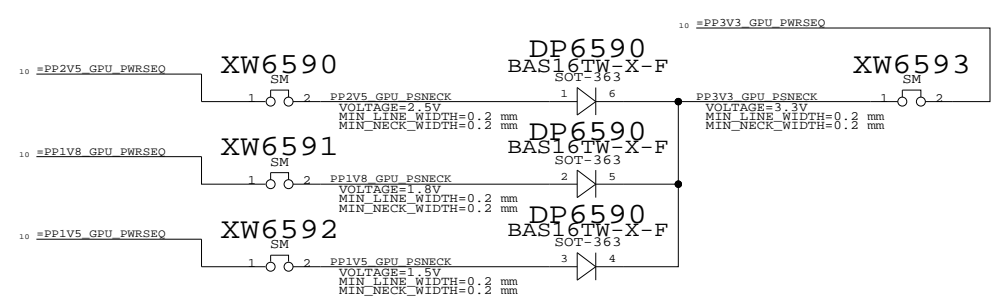
Power aliases required by this page:
 - =PP3V3_GPU_CLOCKS - =PP3V3_GPU_PWRSEQ
 - =PPVIN_GPU_LVDDR_LDO - =PP2V5_GPU_PWRSEQ
 - =PP2V5_GPU_LVDDR_LDO - =PP1V8_GPU_PWRSEQ
 - =PP1V5_GPU_PWRSEQ

Signal aliases required by this page:
 (NONE)

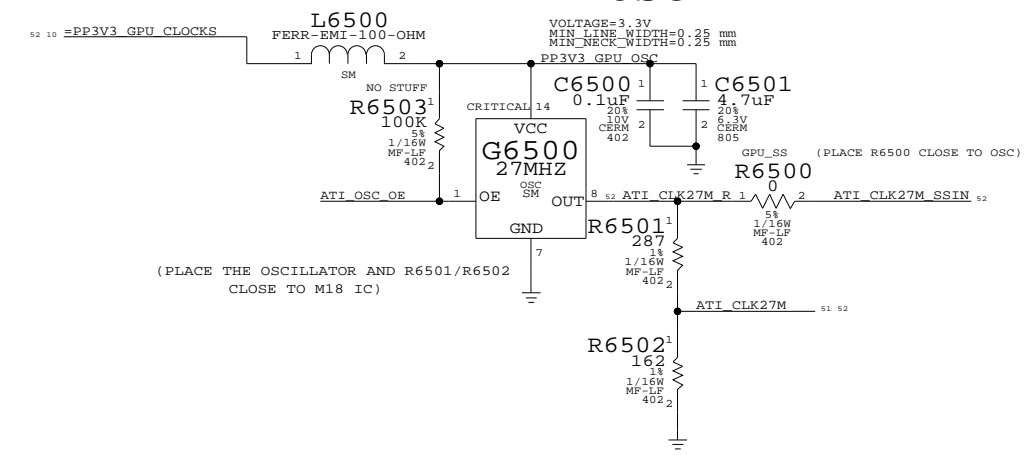
BOM options provided by this page:
 - GPU_SS - GPU_LVDDR_2V8

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
R60	ATI_CLK27M	CLOCK	CLOCK	
R64	ATI_CLK27M	CLOCK	CLOCK	
R65	ATI_CLK27M	CLOCK	CLOCK	
R61	ATI_CLK27M_SS	CLOCK	CLOCK	
R62	ATI_CLK27M_SS	CLOCK	CLOCK	

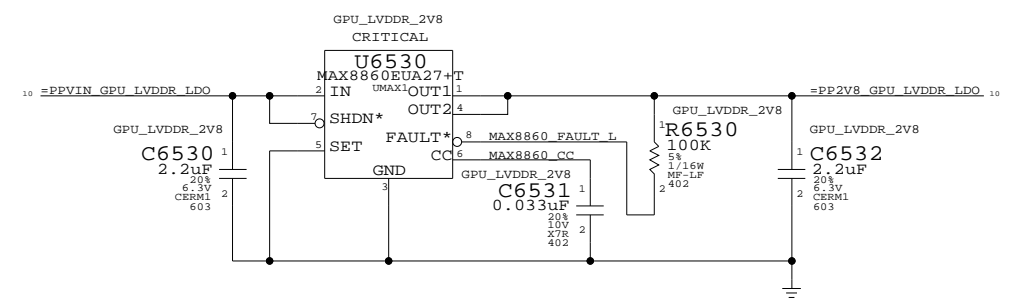
M11 Power Shutdown Sequencing



27M OSC

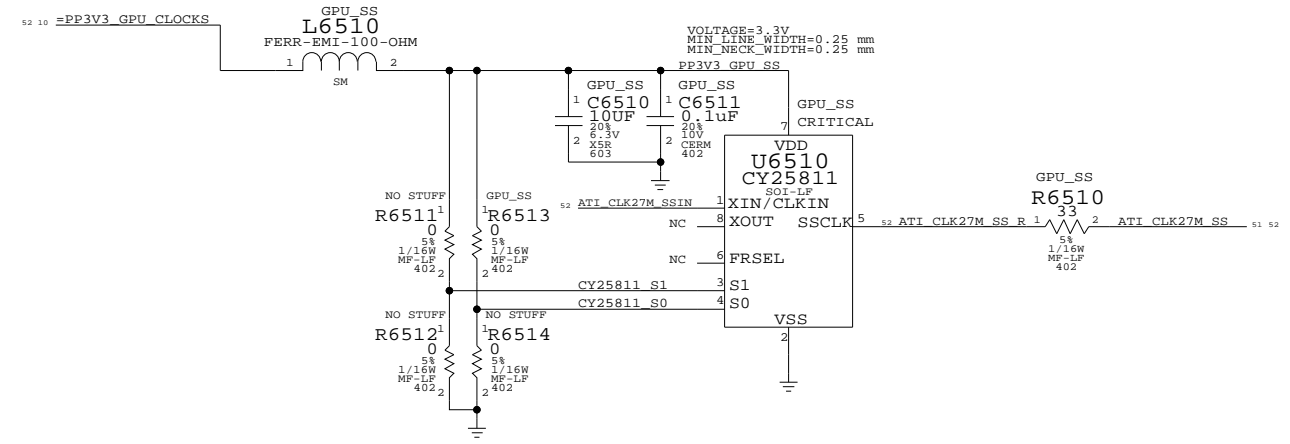


LVDDR 2.8V LDO



PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1188	353S1140	GPU_LVDDR_2V8	U6530	Primary is 2.7V/Alt is 2.8V

SPREAD SPECTRUM SUPPORT
 S0=1;S1=M => -1.5% DOWN-SPREAD



GPU (M11) Clocks/Misc

SYNC_MASTER=N/A SYNC_DATE=N/A

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NONE	65	115	

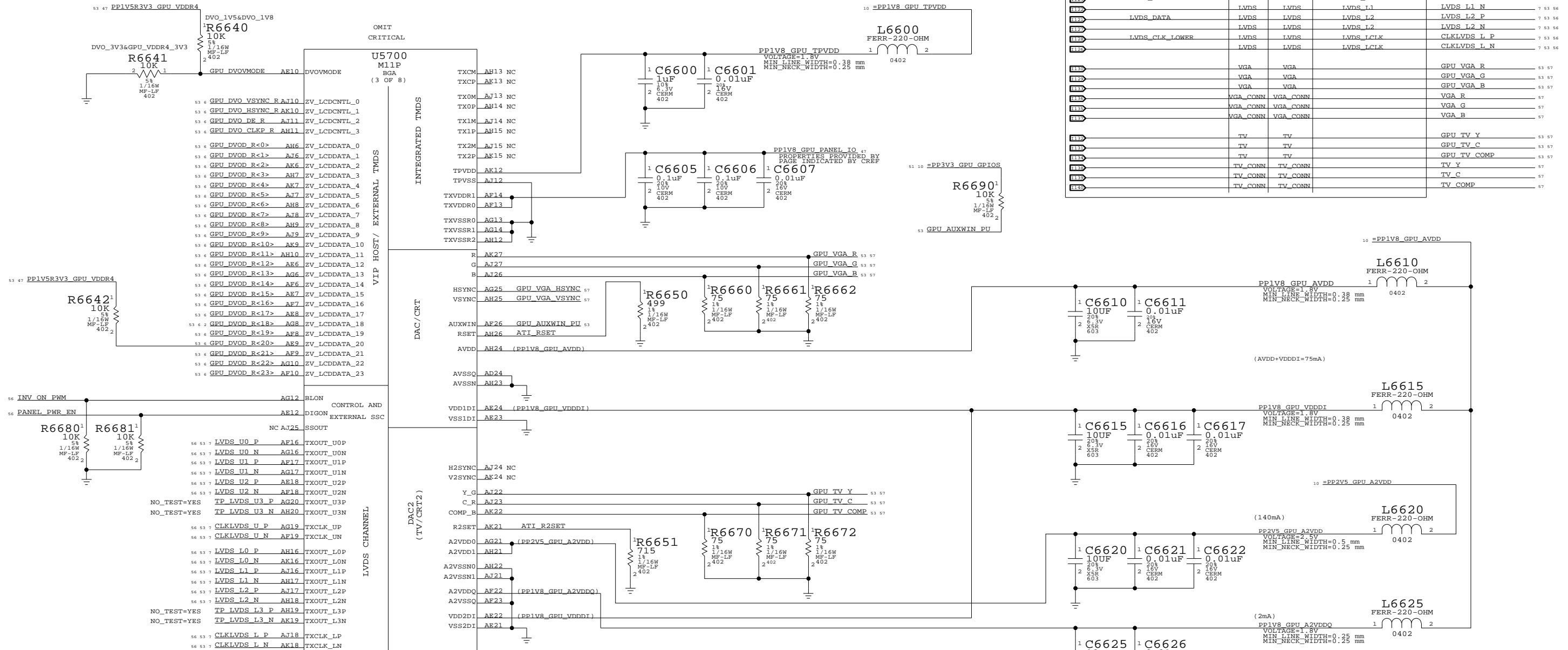
Page Notes

Power aliases required by this page:
 - =PP2V5_GPU_A2VDD - =PP1V8_GPU_AVDD
 - =PP1V8_GPU_TPVDV - =PP3V3_GPU_GPIOS

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - DVO_1V5 - GPU_VDDR4_3V3
 - DVO_1V8 - DVO_3V3

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		DIFFERENTIAL_PAIR	
	SPACING	PHYSICAL		
R6600	DVO	DVO		GPU DVOD R<23..0>
R6601	DVO	DVO		GPU DVO HSYNC R
R6602	DVO	DVO		GPU DVO VSYNC R
R6603	DVO	DVO		GPU DVO DE R
R6604	DVO	DVO		GPU DVO CLKP R
R6605	LVDS_DATA	LVDS	LVDS_U0	LVDS U0_P
R6606	LVDS_DATA	LVDS	LVDS_U0	LVDS U0_N
R6607	LVDS_DATA	LVDS	LVDS_U1	LVDS U1_P
R6608	LVDS_DATA	LVDS	LVDS_U1	LVDS U1_N
R6609	LVDS_DATA	LVDS	LVDS_U2	LVDS U2_P
R6610	LVDS_DATA	LVDS	LVDS_U2	LVDS U2_N
R6611	LVDS_CLK_UPPER	LVDS	LVDS_UCLK	CLKLVDS_U_P
R6612	LVDS_CLK_UPPER	LVDS	LVDS_UCLK	CLKLVDS_U_N
R6613	LVDS_DATA	LVDS	LVDS_L0	LVDS L0_P
R6614	LVDS_DATA	LVDS	LVDS_L0	LVDS L0_N
R6615	LVDS_DATA	LVDS	LVDS_L1	LVDS L1_P
R6616	LVDS_DATA	LVDS	LVDS_L1	LVDS L1_N
R6617	LVDS_DATA	LVDS	LVDS_L2	LVDS L2_P
R6618	LVDS_DATA	LVDS	LVDS_L2	LVDS L2_N
R6619	LVDS_CLK_LOWER	LVDS	LVDS_LCLK	CLKLVDS_L_P
R6620	LVDS_CLK_LOWER	LVDS	LVDS_LCLK	CLKLVDS_L_N
R6621	VGA	VGA		GPU VGA_R
R6622	VGA	VGA		GPU VGA_G
R6623	VGA	VGA		GPU VGA_B
R6624	VGA_CONN	VGA_CONN		VGA_R
R6625	VGA_CONN	VGA_CONN		VGA_G
R6626	VGA_CONN	VGA_CONN		VGA_B
R6627	TV	TV		GPU TV_Y
R6628	TV	TV		GPU TV_C
R6629	TV	TV		GPU TV_COMP
R6630	TV_CONN	TV_CONN		TV_Y
R6631	TV_CONN	TV_CONN		TV_C
R6632	TV_CONN	TV_CONN		TV_COMP



GPU (M11) DVI/DAC Outputs

SYNC_MASTER=N/A SYNC_DATE=N/A

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SCALE	SIZE	DRAWING NUMBER	REV.
	NONE	D 051-7001	D
SCALE		SHT	OF
NONE		66	115

Page Notes

Power aliases required by this page:
 - =PP3V3_RUN_SI - =PP1V5R3V3_DVO_VREF

Signal aliases required by this page:
 - =SI_TMDS_RESET_L - =RP67xxPy (pinswappable series R)
 - =SI_I2C_CLK
 - =SI_I2C_DATA

BOM options provided by this page:
 - TMDS_EXT - DVO_V15 - DVO_V3V3
 - TMDS_DUAL - DVO_V18

Net Spacing Type: TMDS
 Net Physical Type: TMDS

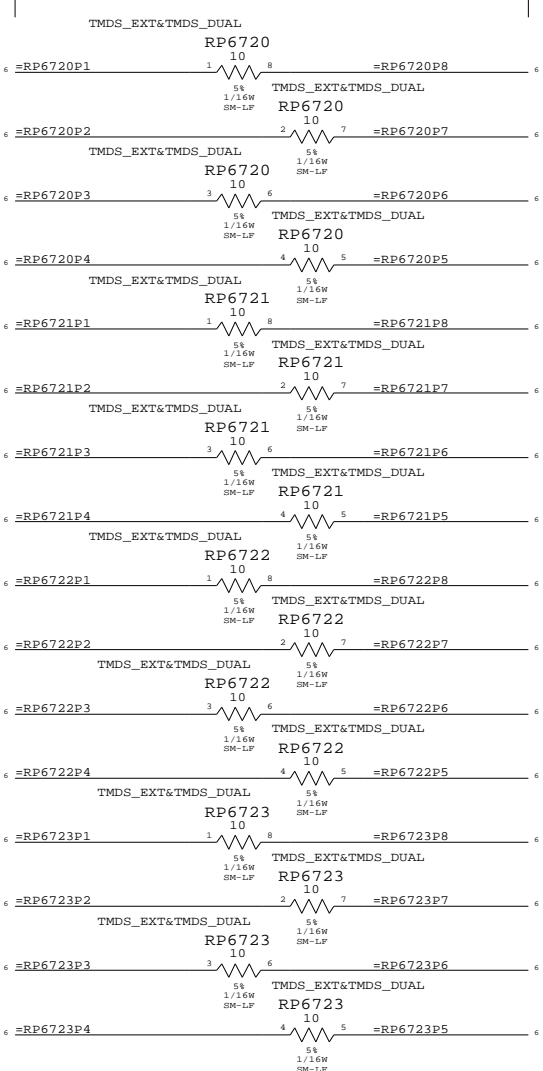
NOTE: Target differential impedance for TMDS data pairs is 100 ohms.

ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
TMDS		DVO	GPU_DVOD<0..11>
TMDS		DVO	GPU_DVO_HSYNC
TMDS		DVO	GPU_DVO_VSYNC
TMDS		DVO	GPU_DVO_DE
TMDS		DVO	GPU_DVO_CLKP
TMDS		TMDS	SI_TMDS_CLK
TMDS		TMDS	SI_TMDS_CLKP
TMDS		TMDS	SI_TMDS_D0
TMDS		TMDS	SI_TMDS_D1
TMDS		TMDS	SI_TMDS_D2
TMDS		TMDS	SI_TMDS_D0
TMDS		TMDS	SI_TMDS_D1
TMDS		TMDS	SI_TMDS_D2

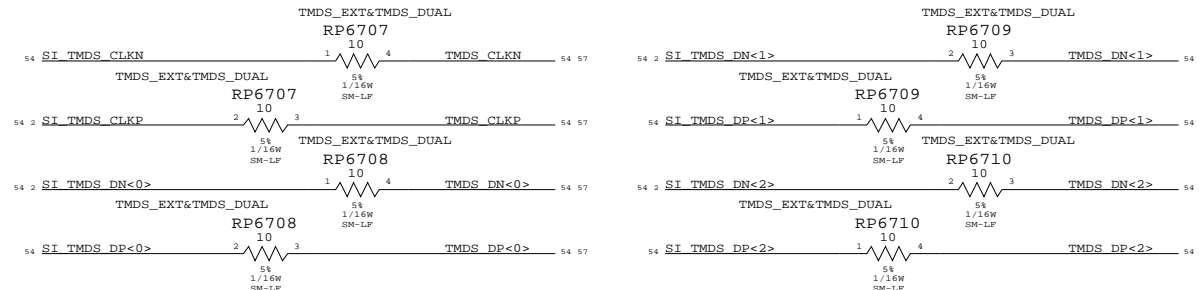
Lower DVO Termination

Place close to GPU

One each for: GPU_DVOD<0..11>
 GPU_DVO_HSYNC
 GPU_DVO_VSYNC
 GPU_DVO_DE
 GPU_DVO_CLKP

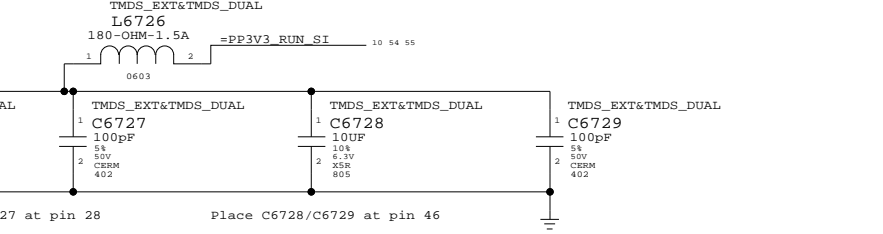
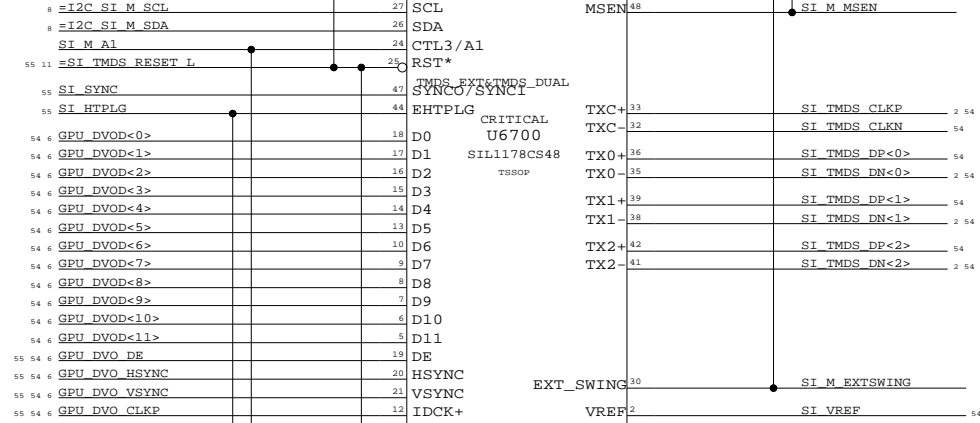
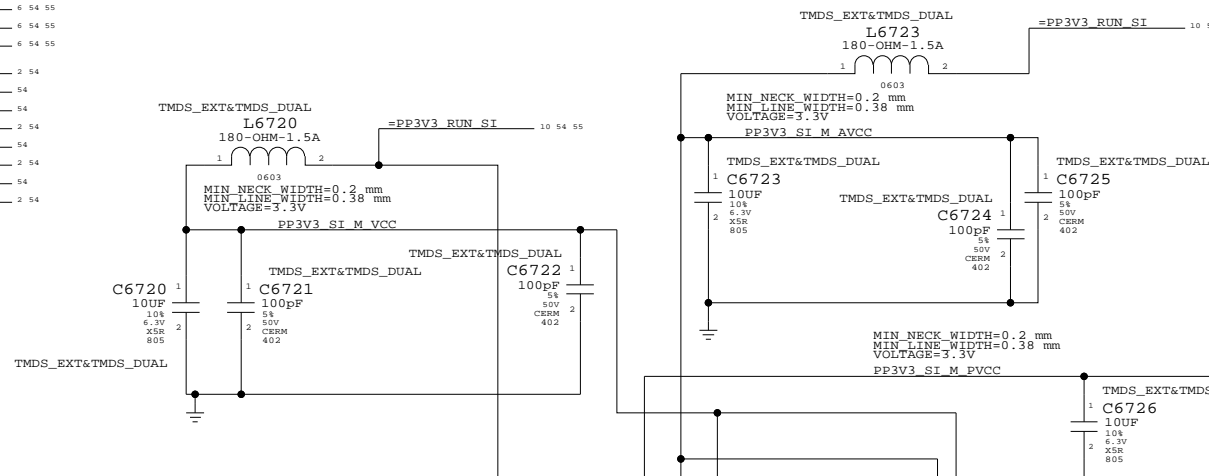
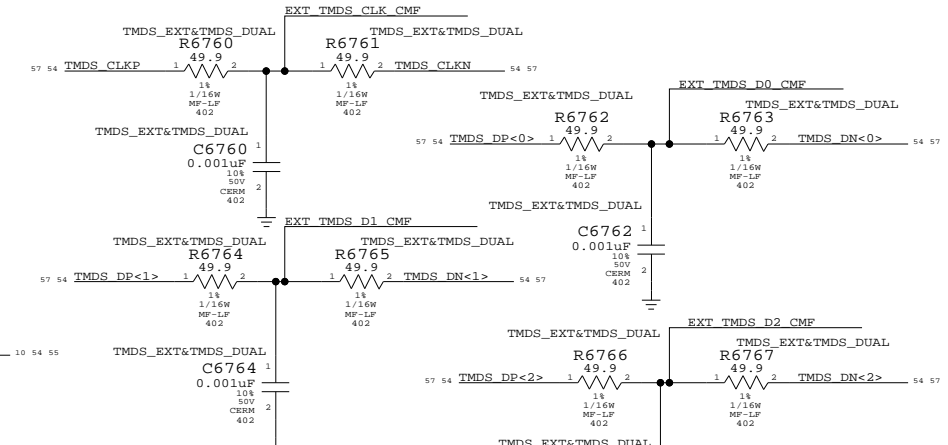


SILICON IMAGE TMDS



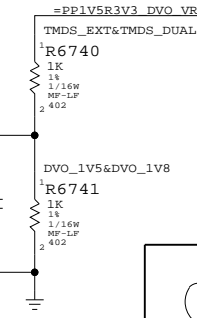
EXTERNAL TMDS TERMINATION

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN



ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
TMDS		TMDS	TMDS_CLK
TMDS		TMDS	TMDS_CLKP
TMDS		TMDS	TMDS_CLKN
TMDS		TMDS	TMDS_D0
TMDS		TMDS	TMDS_D1
TMDS		TMDS	TMDS_D2
TMDS		TMDS	TMDS_DP<0>
TMDS		TMDS	TMDS_DP<1>
TMDS		TMDS	TMDS_DP<2>
TMDS		TMDS	TMDS_DN<0>
TMDS		TMDS	TMDS_DN<1>
TMDS		TMDS	TMDS_DN<2>

The DVO bus can be run with 3.3V or 1.5V/1.8V signaling. The power rail for the reference should be connected to the GPU DVO rail.

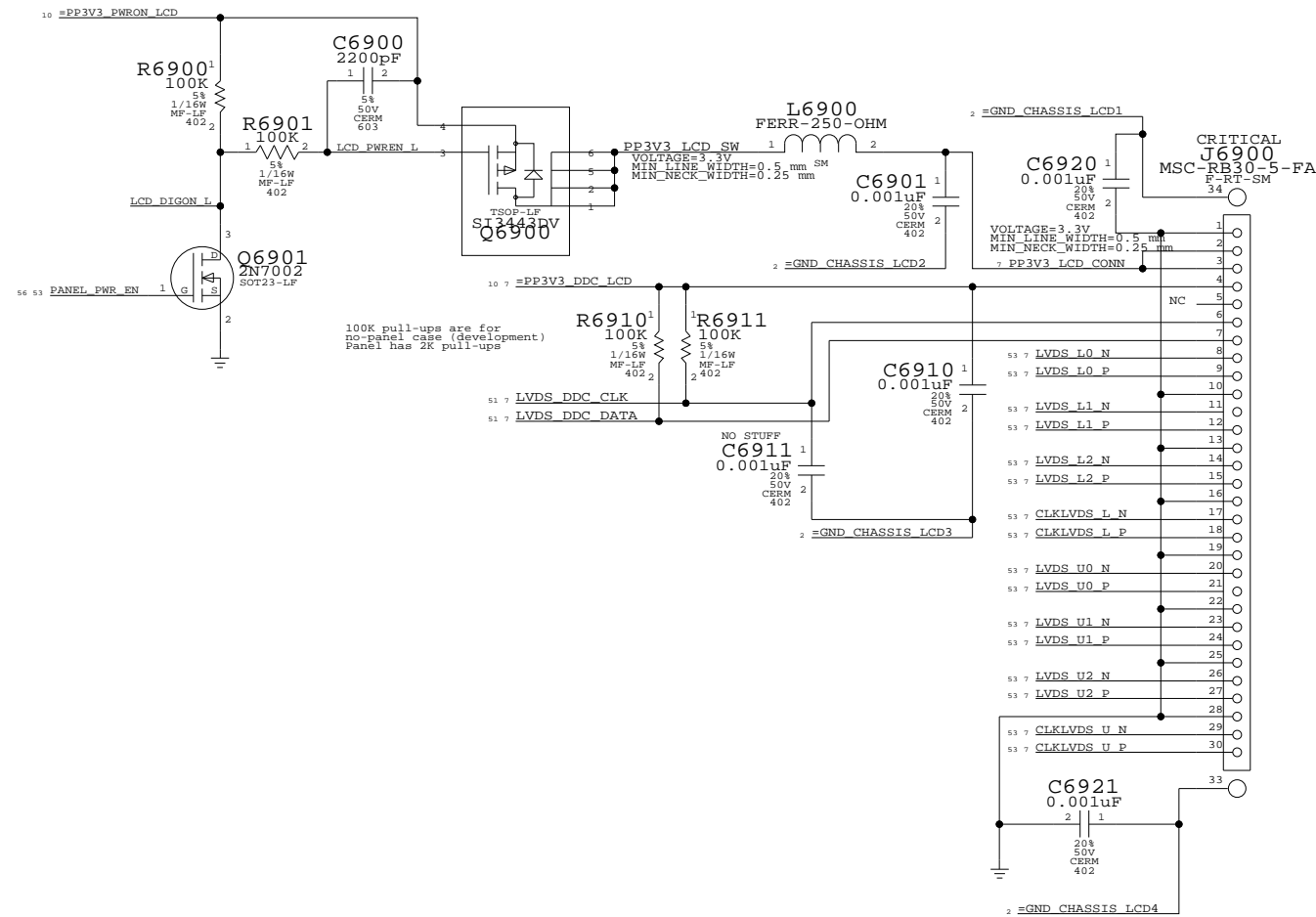


Lower TMDS Transmitter
 SYNC_MASTER=N/A SYNC_DATE=N/A

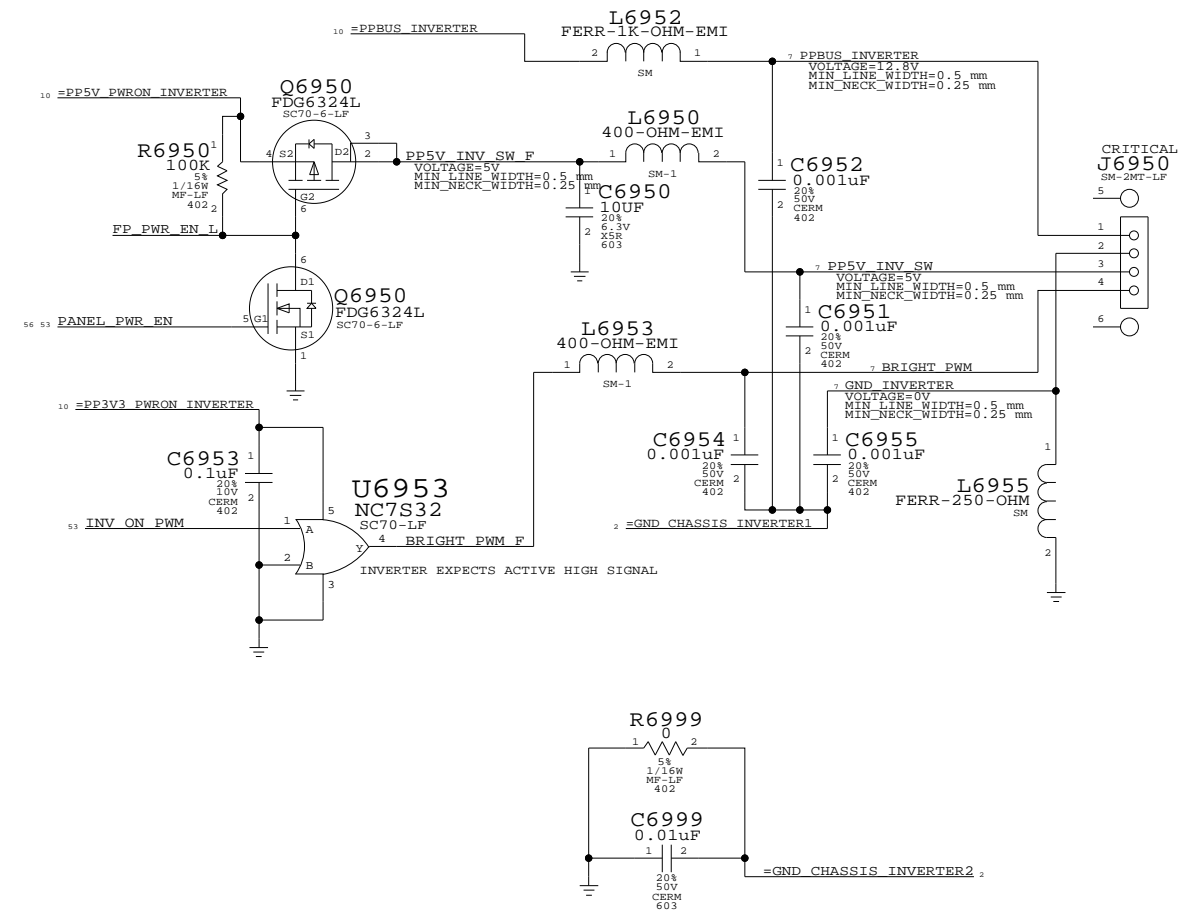
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SCALE	SHT	OF
NONE	67	115

LCD (LVDS) INTERFACE



INVERTER INTERFACE



Internal Display Conns

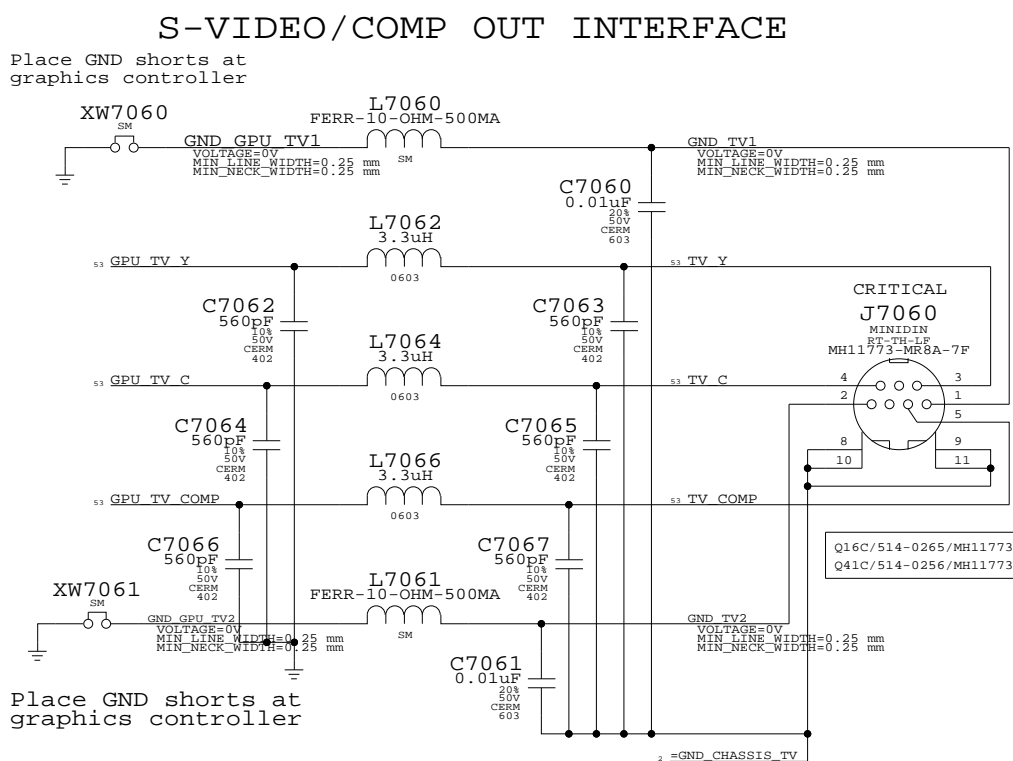
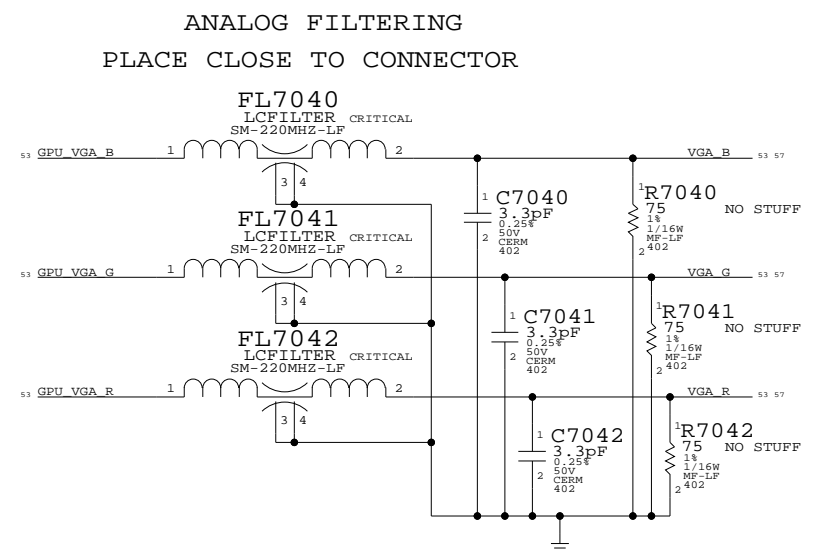
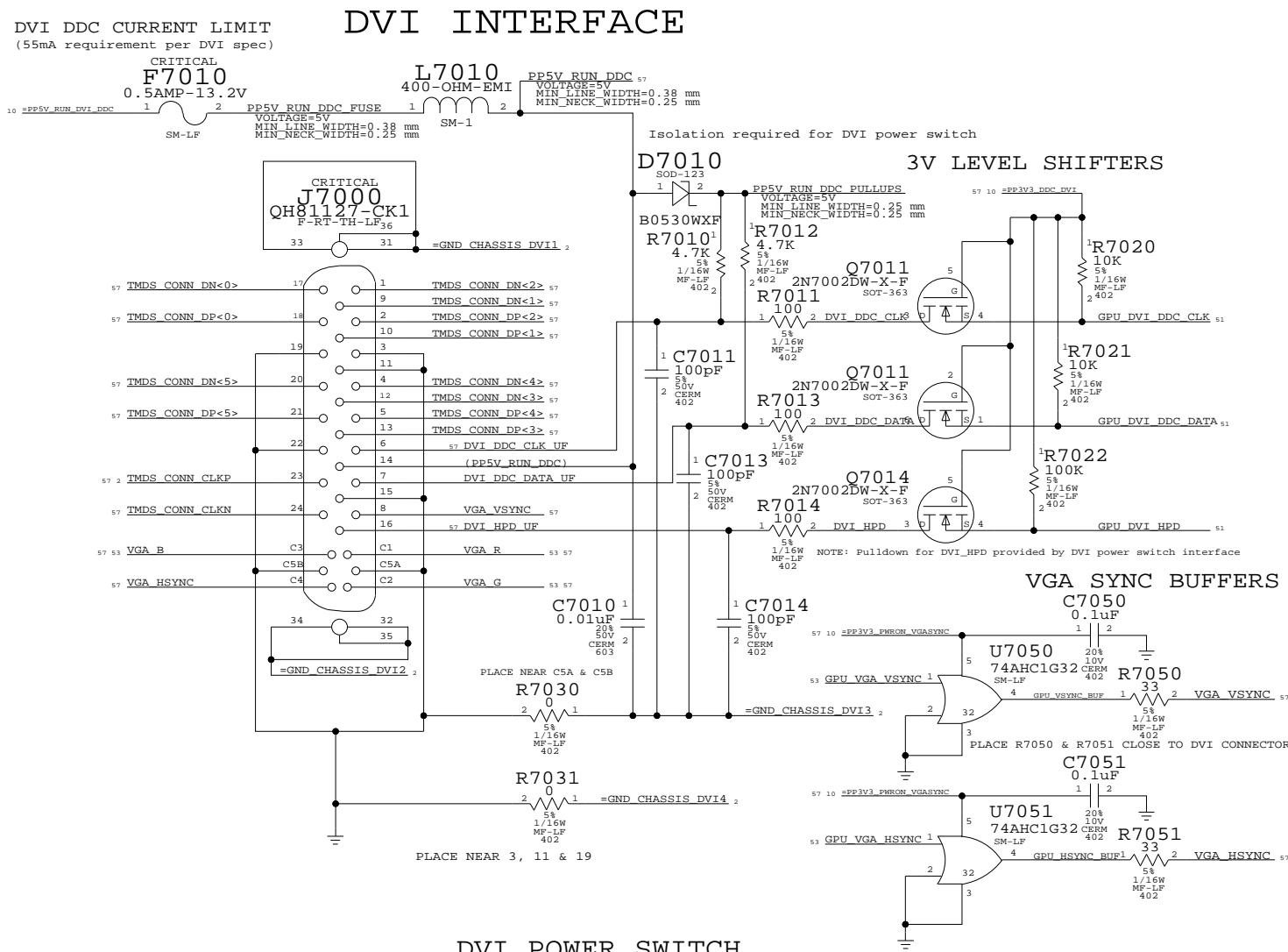
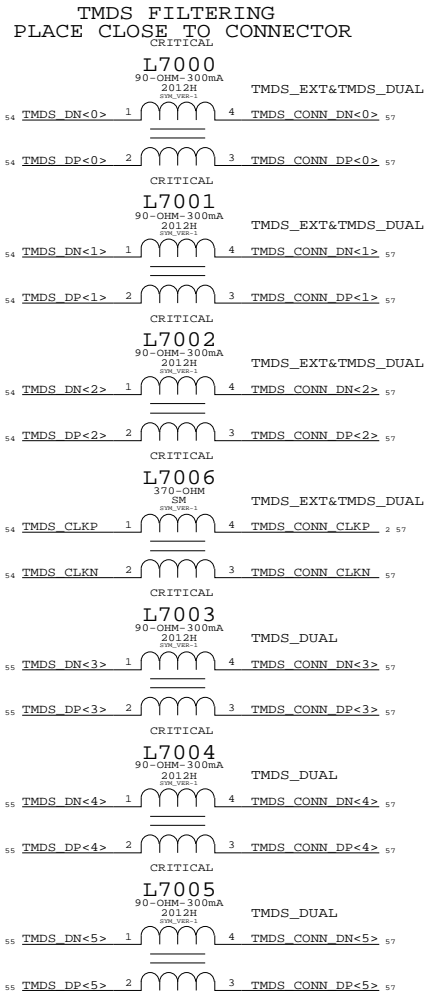
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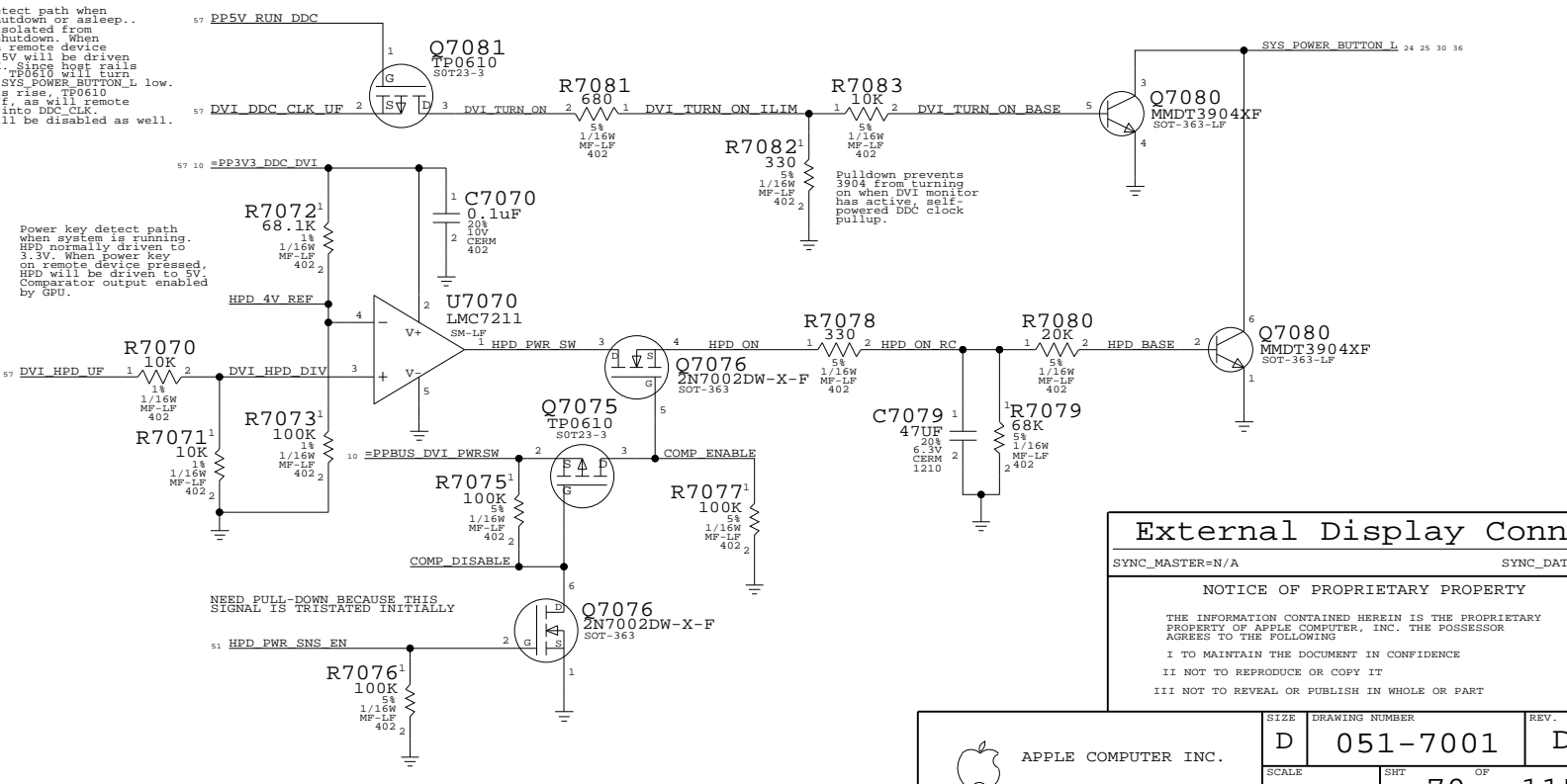
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	D	051-7001	D
SCALE	NONE	SHT OF	69 OF 115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_CLK	TMDS_CONN_CLK
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_CLKN	TMDS_CONN_CLKN
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D0	TMDS_CONN_DP<0>
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D0	TMDS_CONN_DP<0>
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D1	TMDS_CONN_DP<1>
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D1	TMDS_CONN_DP<1>
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D2	TMDS_CONN_DP<2>
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D2	TMDS_CONN_DP<2>
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D3	TMDS_CONN_DP<3>
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D3	TMDS_CONN_DP<3>
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D4	TMDS_CONN_DP<4>
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D4	TMDS_CONN_DP<4>
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D5	TMDS_CONN_DP<5>
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D5	TMDS_CONN_DP<5>



Power key detect path when system is shutdown or asleep... DDC CLK is isolated from GPU during shutdown. When power key on, remote device is pressed, 5V will be driven into DDC CLK. Since hot rails will be low, TP0610 will turn on, driving SYS_POWER_BUTTON_L low. As hot rails rise, TP0610 will turn off, as will remote device path into DDC CLK. Isolation will be disabled as well.



External Display Conns

SYNC_MASTER=N/A SYNC_DATE=N/A

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SCALE	NONE	SHT	OF
		70	115

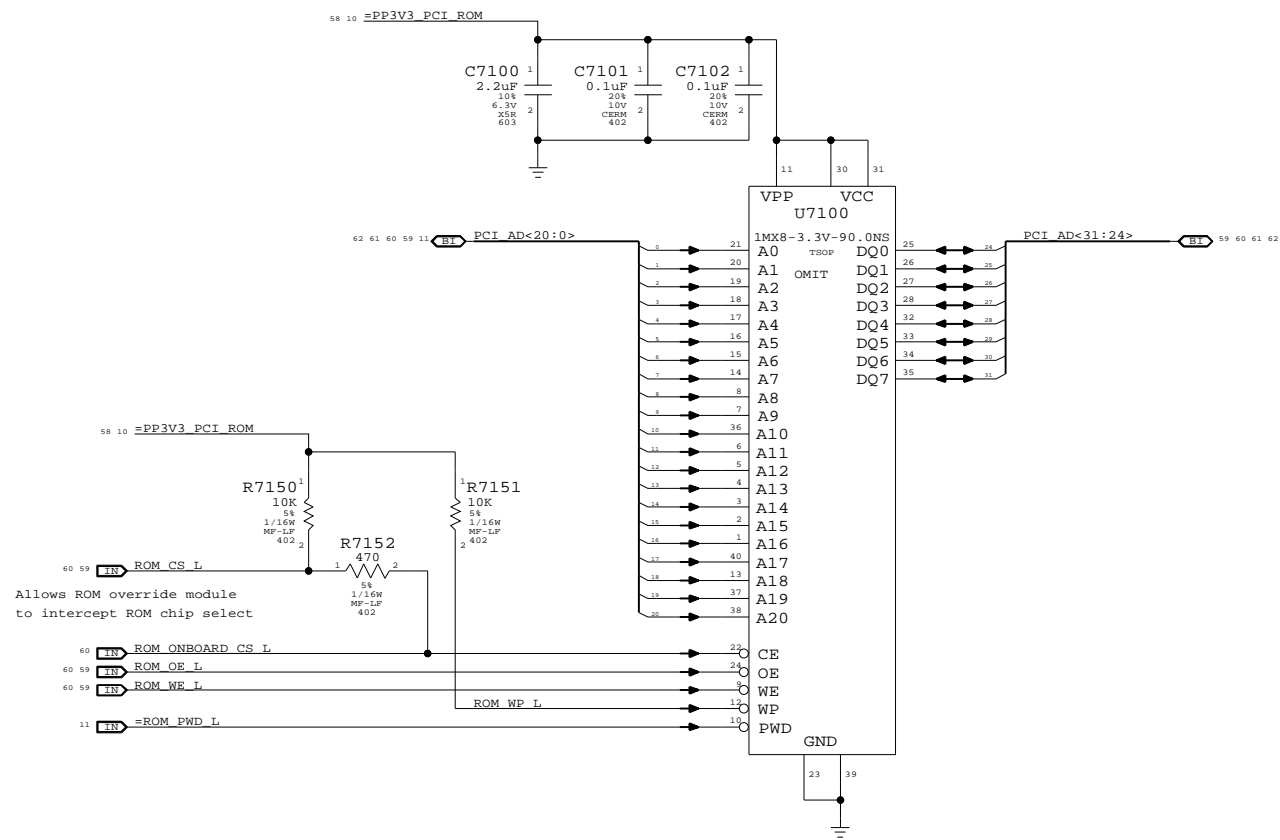
Page Notes

Power aliases required by this page:
 - =PP3V3_PCI_ROM

Signal aliases required by this page:
 - =ROM_PWD_L

BOM options provided by this page:
 (NONE)

NOTE: This page does not specify a BootROM part number. Must use a TABLE_X_ITEM symbol to declare U7100 part number.



BootROM

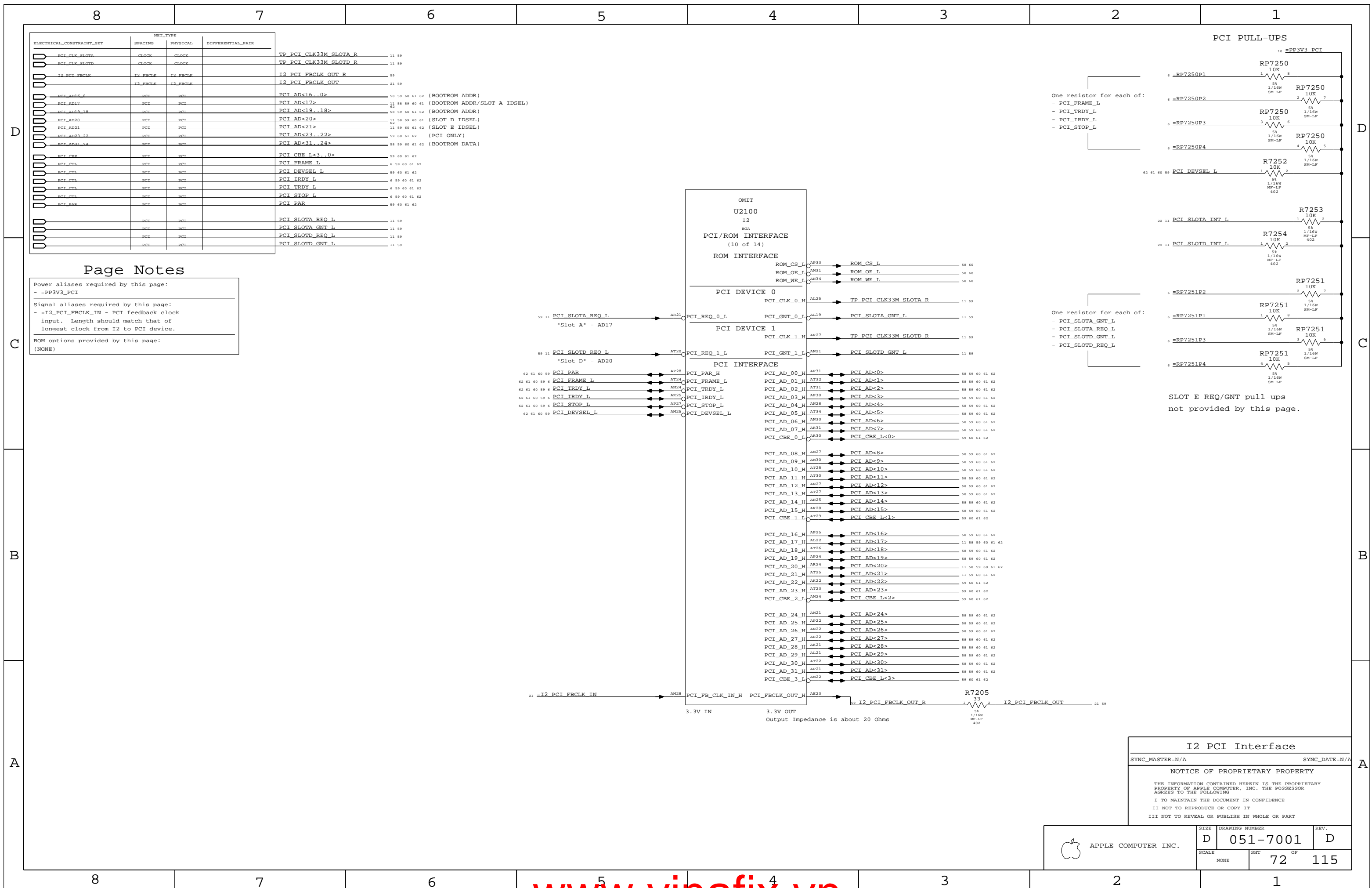
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	D	051-7001	D
SCALE	SHT OF		
NONE	71 OF		115



ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
PCI_CLK_SLOTA	CLOCK	CLOCK	
PCI_CLK_SLOTD	CLOCK	CLOCK	
I2_PCI_FBCLK	I2_FBCLK	I2_FBCLK	
PCI_AD<16..0>	PCI	PCI	
PCI_AD<17>	PCI	PCI	
PCI_AD<19..18>	PCI	PCI	
PCI_AD<20>	PCI	PCI	
PCI_AD<21>	PCI	PCI	
PCI_AD<23..22>	PCI	PCI	
PCI_AD<31..24>	PCI	PCI	
PCI_CBE_L<3..0>	PCI	PCI	
PCI_FRAME_L	PCI	PCI	
PCI_DEVSEL_L	PCI	PCI	
PCI_IRDY_L	PCI	PCI	
PCI_TRDY_L	PCI	PCI	
PCI_STOP_L	PCI	PCI	
PCI_PAR	PCI	PCI	
PCI_SLOTA_REQ_L	PCI	PCI	
PCI_SLOTA_GNT_L	PCI	PCI	
PCI_SLOTD_REQ_L	PCI	PCI	
PCI_SLOTD_GNT_L	PCI	PCI	

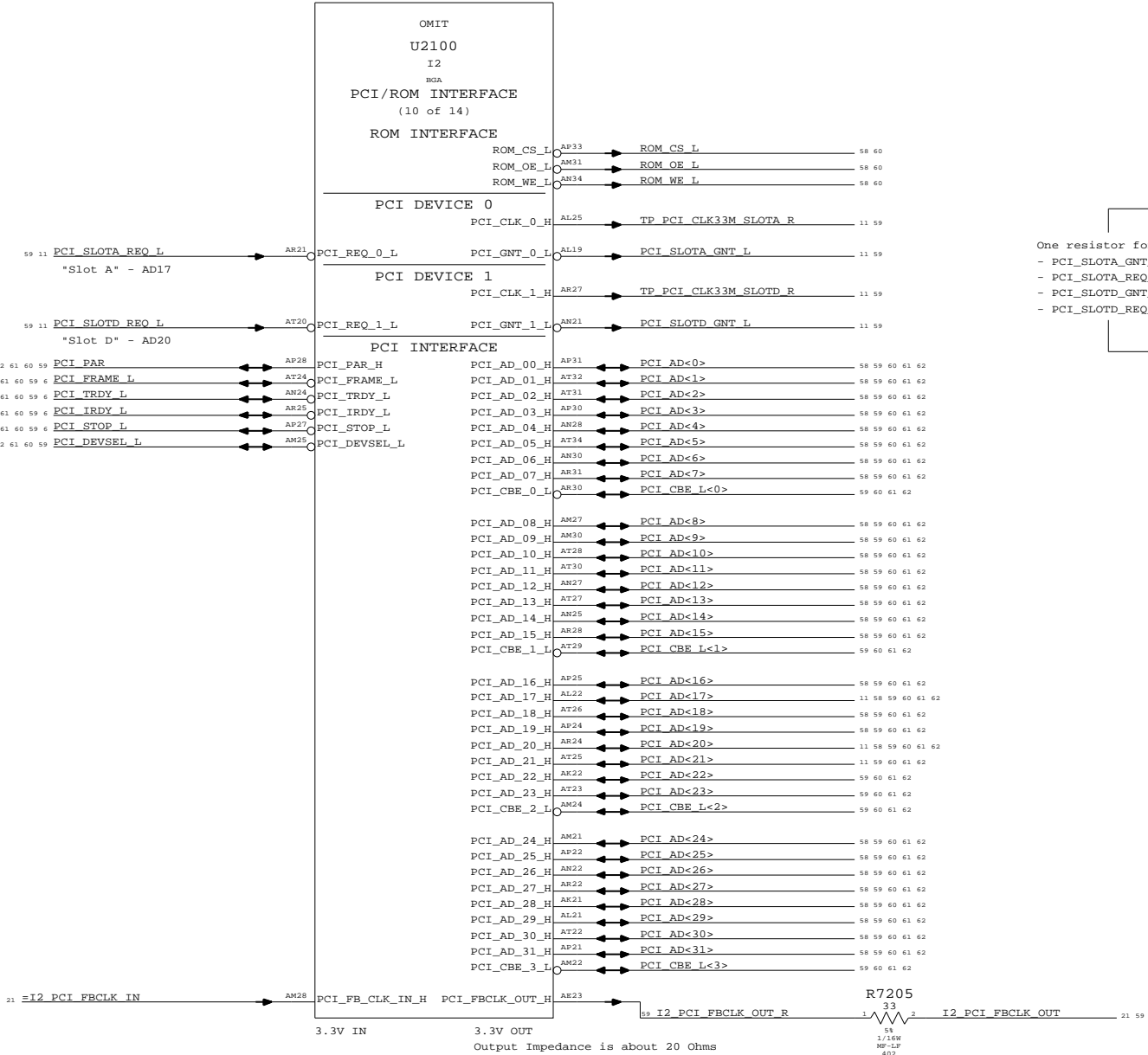
NET_NAME	NET_TYPE	VALUE	DESCRIPTION
TP_PCI_CLK33M_SLOTA_R	CLOCK	11 59	
TP_PCI_CLK33M_SLOTD_R	CLOCK	11 59	
I2_PCI_FBCLK_OUT_R	I2_FBCLK	59	
I2_PCI_FBCLK_OUT	I2_FBCLK	21 59	
PCI_AD<16..0>	PCI	58 59 60 61 62	(BOOTROM ADDR)
PCI_AD<17>	PCI	11 58 59 60 61	(BOOTROM ADDR/SLOT A IDSEL)
PCI_AD<19..18>	PCI	58 59 60 61 62	(BOOTROM ADDR)
PCI_AD<20>	PCI	11 58 59 60 61	(SLOT D IDSEL)
PCI_AD<21>	PCI	11 59 60 61 62	(SLOT E IDSEL)
PCI_AD<23..22>	PCI	59 60 61 62	(PCI ONLY)
PCI_AD<31..24>	PCI	58 59 60 61 62	(BOOTROM DATA)
PCI_CBE_L<3..0>	PCI	59 60 61 62	
PCI_FRAME_L	PCI	6 59 60 61 62	
PCI_DEVSEL_L	PCI	59 60 61 62	
PCI_IRDY_L	PCI	6 59 60 61 62	
PCI_TRDY_L	PCI	6 59 60 61 62	
PCI_STOP_L	PCI	6 59 60 61 62	
PCI_PAR	PCI	59 60 61 62	
PCI_SLOTA_REQ_L	PCI	11 59	
PCI_SLOTA_GNT_L	PCI	11 59	
PCI_SLOTD_REQ_L	PCI	11 59	
PCI_SLOTD_GNT_L	PCI	11 59	

Page Notes

Power aliases required by this page:
 - =PP3V3_PCI

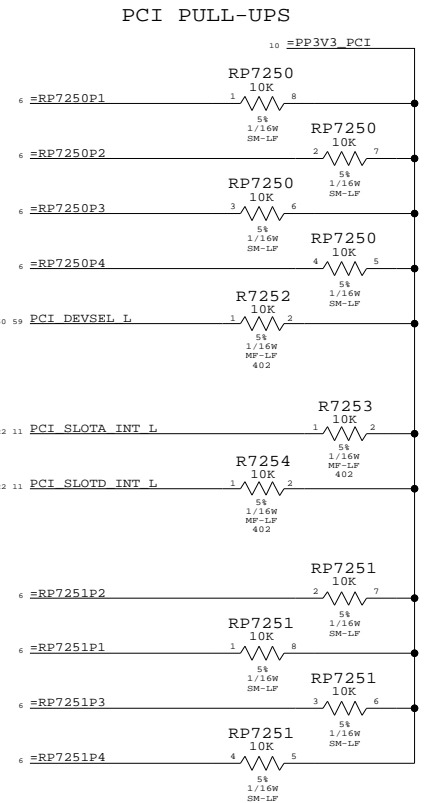
Signal aliases required by this page:
 - =I2_PCI_FBCLK_IN - PCI feedback clock input. Length should match that of longest clock from I2 to PCI device.

BOM options provided by this page:
 (NONE)



One resistor for each of:
 - PCI_FRAME_L
 - PCI_TRDY_L
 - PCI_IRDY_L
 - PCI_STOP_L

One resistor for each of:
 - PCI_SLOTA_GNT_L
 - PCI_SLOTA_REQ_L
 - PCI_SLOTD_GNT_L
 - PCI_SLOTD_REQ_L



SLOT E REQ/GNT pull-ups not provided by this page.

I2 PCI Interface
 SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-7001	D
SCALE	SHT	OF	
NONE	72	115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		DIFFERENTIAL_PAIR
	SPACING	PHYSICAL	
MEM	CLOCK	CLOCK	

=PCI_CLK33M_AIRPORT 11 60

Page Notes

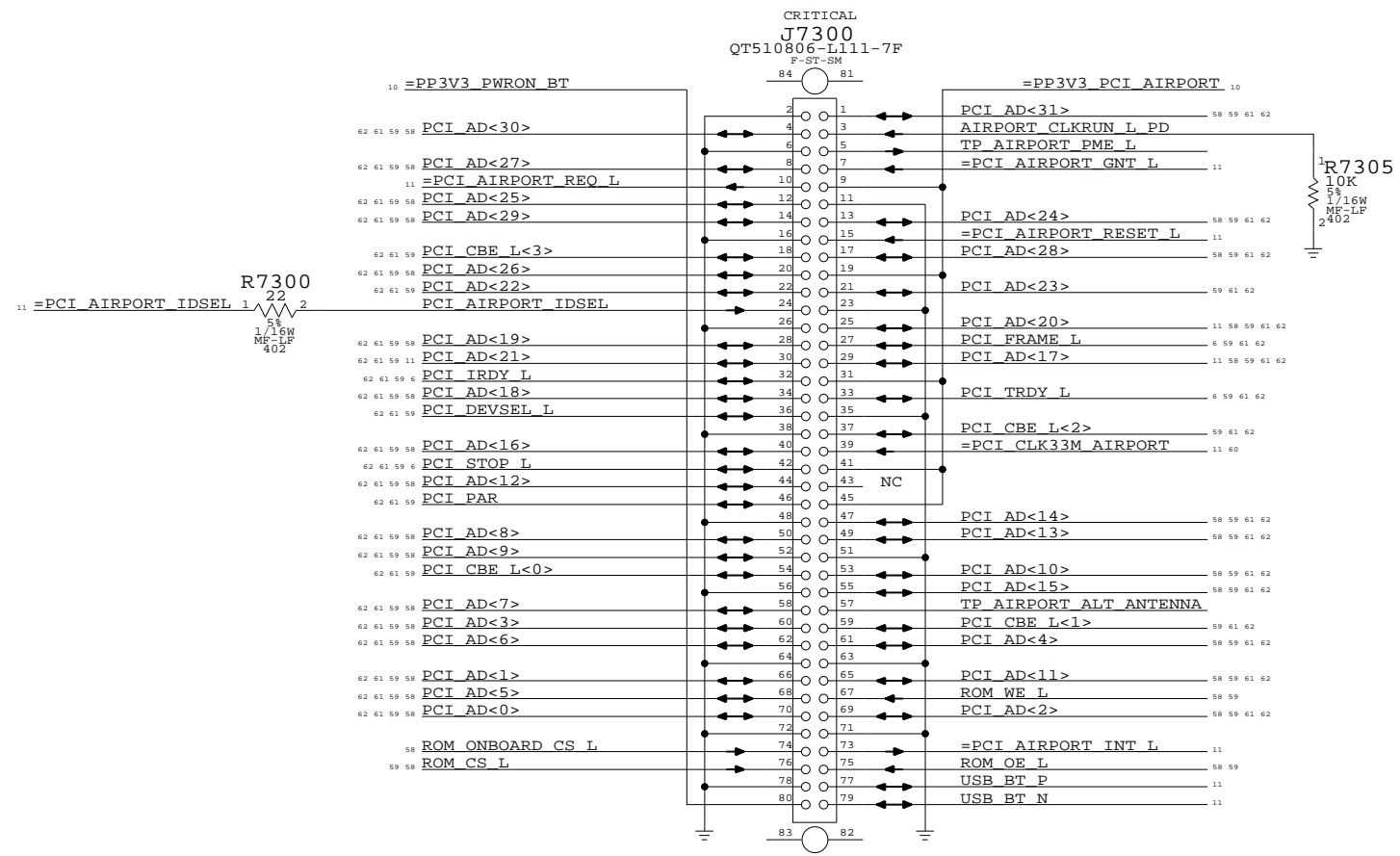
Power aliases required by this page:
 - =PP3V3_PCI (802.11g Power)
 - =PP3V3_PWRON_BT (Bluetooth Power)

Signal aliases required by this page:
 - =PCI_CLK33M_AIRPORT (33MHz PCI clock)
 - =PCI_AIRPORT_RESET_L (PCI Reset)
 - =USB_BT_P (Bluetooth USB D+)
 - =USB_BT_N (Bluetooth USB D-)

BOM options provided by this page:
 (NONE)

PCI Devices implemented on this page:
 ADL7 (Slot "A") - AirPort (0x????/0x????)

NOTE: This AirPort implementation does not support PME#.



Q85 Connector
 Q16C/516S0361/F-ST-SM
 Q41C/516S0352/M-ST-SM-LF

Q85 Airport/BT Connector

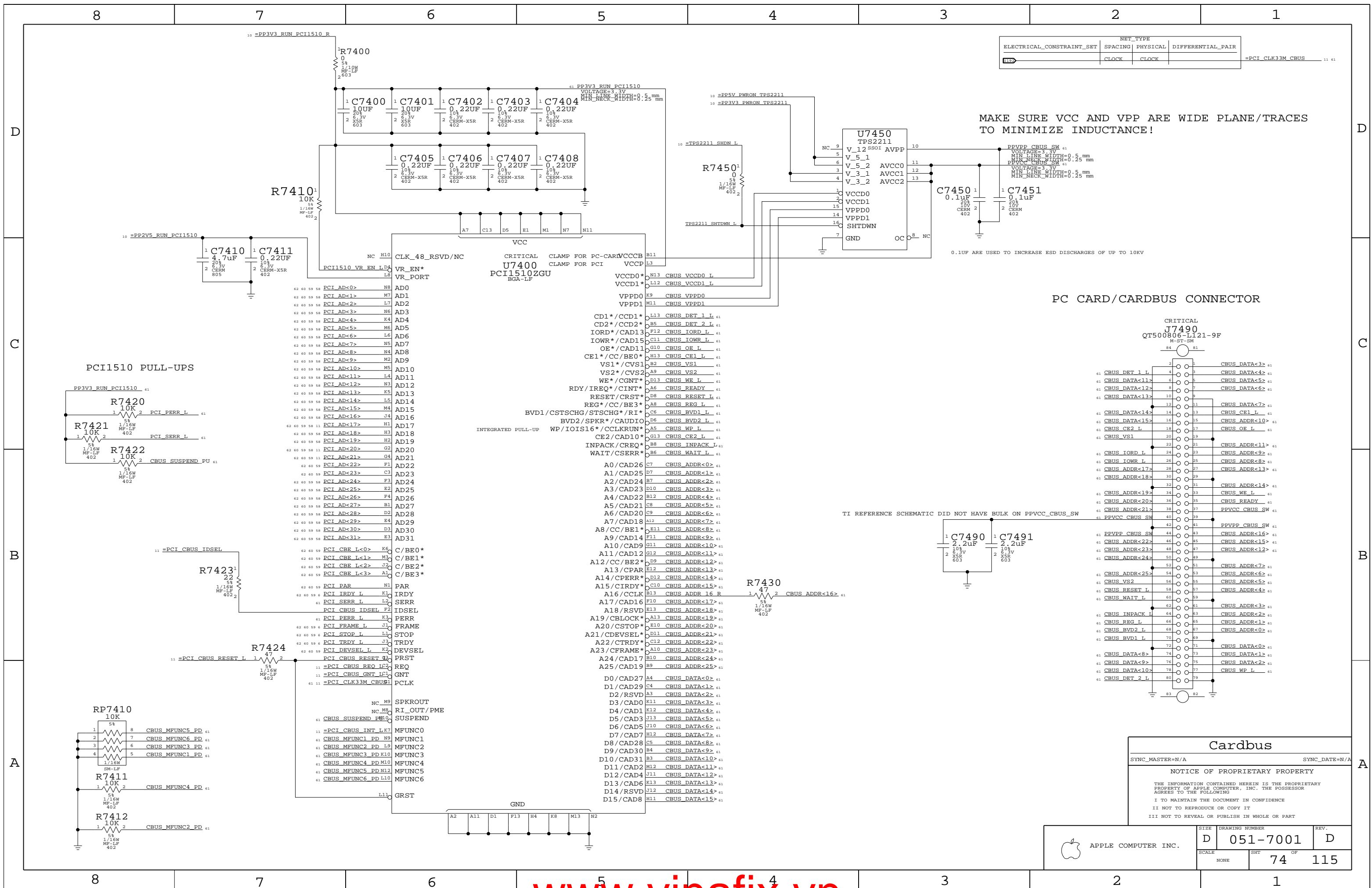
SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-7001	D
SCALE	NONE	SHT OF	73 OF 115



ELECTRICAL_CONSTRAINT_SET	NET_TYPE		DIFFERENTIAL_PAIR
	SPACING	PHYSICAL	
	CLOCK	CLOCK	

=PCI_CLK33M_USB2 11 62

Page Notes

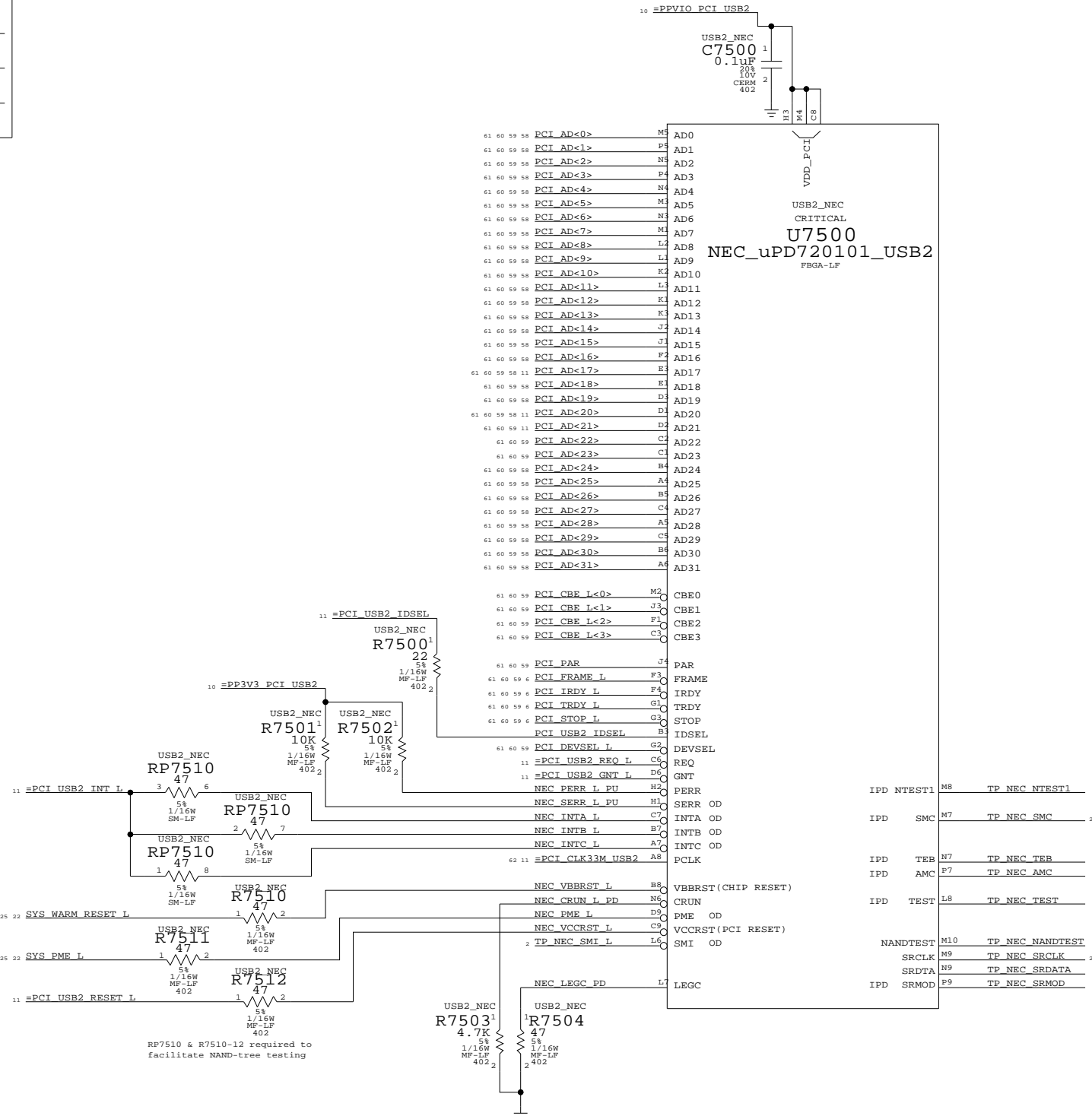
Power aliases required by this page:
 - =PPVIO_PCI (to 3.3V or 5V)
 - =PP3V3_PCI_USB2 (D3cold rail)

Signal aliases required by this page:
 - =PCI_CLK33M_USB2
 - =PCI_USB2_REQ_L - =PCI_USB2_IDSEL
 - =PCI_USB2_GNT_L - =PCI_USB2_RESET_L
 - =PCI_USB2_INT_L

BOM options provided by this page:
 - USB2_NEC

PCI Devices implemented on this page:
 AD27 (Slot "G") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports D3cold.



NEC USB2

SYNC_MASTER=N/A SYNC_DATE=N/A

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SCALE	SHT OF		
NONE	75		115

D

D

C

C

B

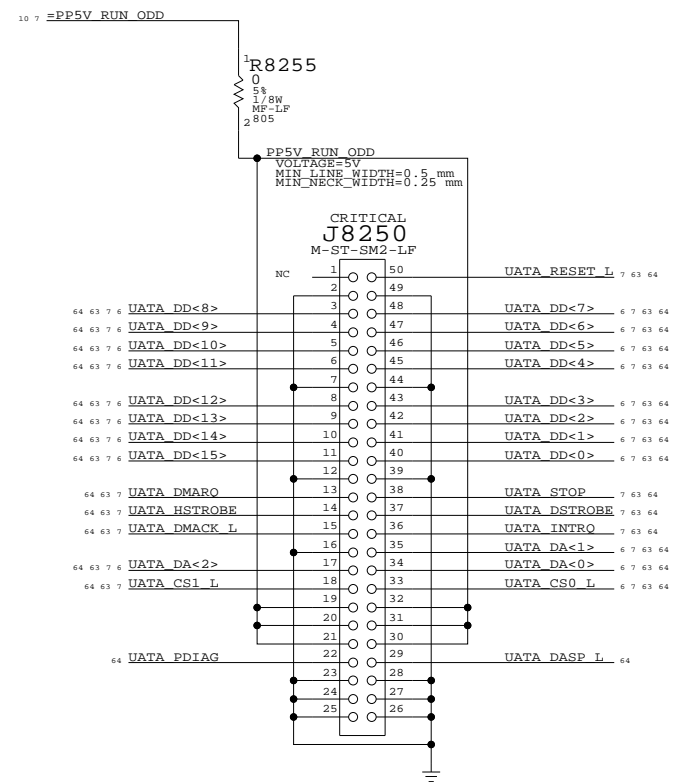
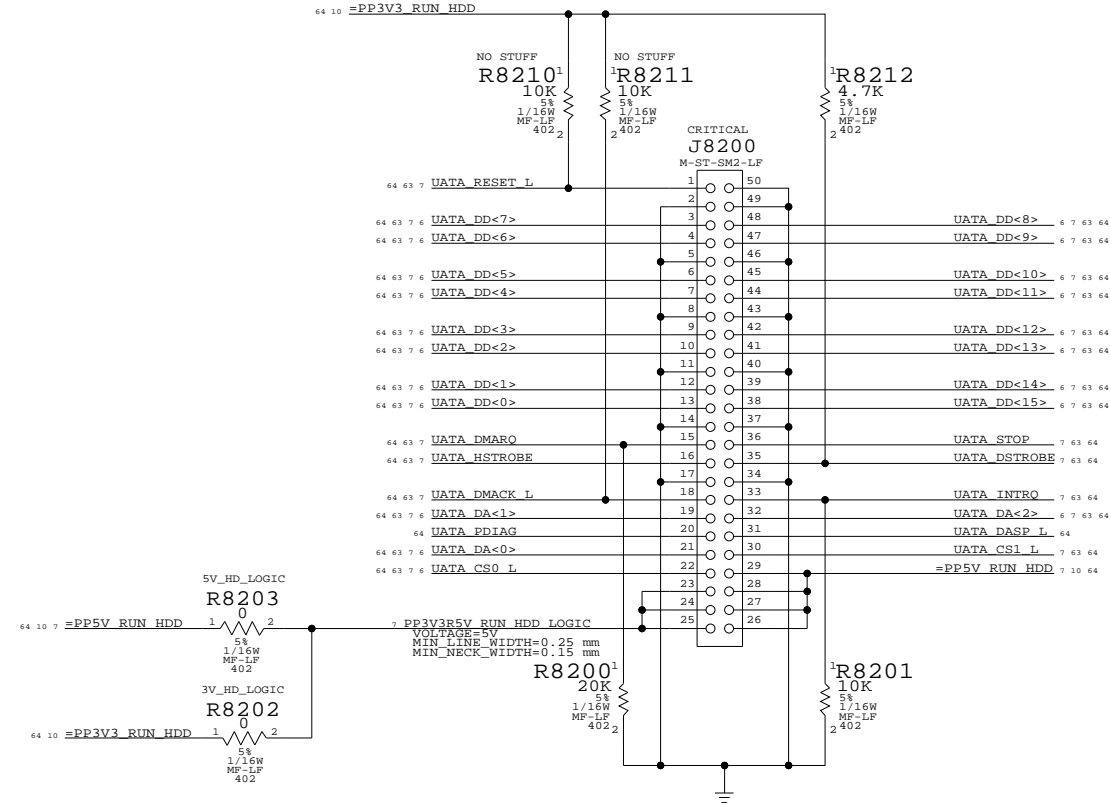
B

A

A

HDD CONNECTOR

ODD CONNECTOR



ATA Connectors
 Q16C/516S0357/M-ST-SM2-LF
 Q41C/516S0335/M-ST-SM1-LF

HDD/ODD Connectors
 SYNC_MASTER=N/A SYNC_DATE=N/A
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	D	051-7001	D
SCALE	SHEET OF		
NONE	82 OF		115

ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	NET_TYPE		
ENET_RX_CLK25M	CLOCK	CLOCK		ENET_CLK25M_TX	11	65
ENET_RX_CLK125M	CLOCK	CLOCK		ENET_CLK125M_RX	11	65
ENET_GBE_REF	CLOCK	CLOCK		ENET_CLK125M_GBE_REF	11	65
ENET_TX_CLK	CLOCK	CLOCK		ENET_CLK125M_GTX_R	65	66
ENET_RXD<0>	ENET	ENET		ENET_RXD<0>	9	11 65
ENET_RXD<1>	ENET	ENET		ENET_RXD<1>	9	11 65
ENET_RXD<2>	ENET	ENET		ENET_RXD<2>	9	11 65
ENET_RXD<3>	ENET	ENET		ENET_RXD<3>	9	11 65
ENET_RXD<4>	ENET	ENET		ENET_RXD<4>	11	65
ENET_RXD<5>	ENET	ENET		ENET_RXD<5>	11	65
ENET_RXD<6>	ENET	ENET		ENET_RXD<6>	11	65
ENET_RXD<7>	ENET	ENET		ENET_RXD<7>	11	65
ENET_RX_DV	ENET	ENET		ENET_RX_DV	9	11 65
ENET_RX_ER	ENET	ENET		ENET_RX_ER	9	11 65
ENET_TXD<0>	ENET	ENET		ENET_TXD<0>	11	65
ENET_TXD<1>	ENET	ENET		ENET_TXD<1>	11	65
ENET_TXD<2>	ENET	ENET		ENET_TXD<2>	11	65
ENET_TXD<3>	ENET	ENET		ENET_TXD<3>	11	65
ENET_TXD<4>	ENET	ENET		ENET_TXD<4>	11	65
ENET_TXD<5>	ENET	ENET		ENET_TXD<5>	11	65
ENET_TXD<6>	ENET	ENET		ENET_TXD<6>	11	65
ENET_TXD<7>	ENET	ENET		ENET_TXD<7>	11	65
ENET_TX_EN_R	ENET	ENET		ENET_TX_EN_R	9	11 65
ENET_TX_ER_R	ENET	ENET		ENET_TX_ER_R	9	11 65
ENET_COL	ENET	ENET		ENET_COL	9	11 65
ENET_CRS	ENET	ENET		ENET_CRS	9	11 65
ENET_MDC	ENET	ENET		ENET_MDC	9	11 65
ENET_MDIO	ENET	ENET		ENET_MDIO	9	11 65
I2_ENET_MDIO	ENET	ENET		I2_ENET_MDIO	65	

Page Notes

Power aliases required by this page:
 - =PP2V5R3V3_PWRON_I2_ENET

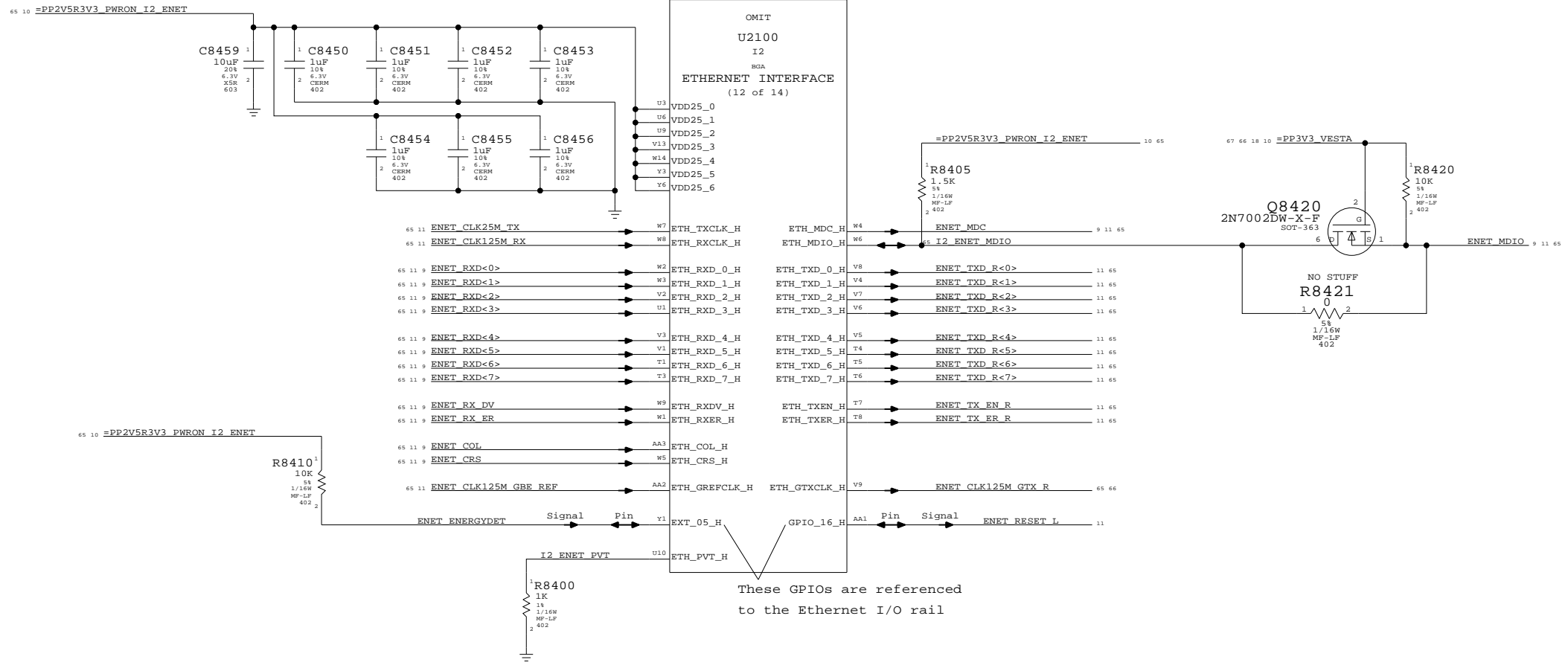
Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

NOTE: This page does not provide any series termination. Any termination, including clock signals, should be provided by the PHY page or a non-shared schematic page.

NOTE: All I2 GPIOs should have a pull-up or pull-down resistor. This page does not provide a resistor for GPIO 16. It must be provided by the PHY page or a non-shared schematic page.

NOTE: ENET_RX_DV has a hold spec violation on I2. May want to lengthen net by ~250ps. Net has a unique ECSet name to allow this.



These GPIOs are referenced to the Ethernet I/O rail

I2 Ethernet Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-7001	D
SCALE	NONE	SHT	OF
		84	115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
[PROVIDED BY LINK PAGE]	CLOCK	CLOCK		
[PROVIDED BY LINK PAGE]	CLOCK	CLOCK		
[PROVIDED BY LINK PAGE]	CLOCK	CLOCK		
ENETCONN	ENETCONN	ENETCONN	ENETCONN_0	
ENETCONN	ENETCONN	ENETCONN	ENETCONN_0	
ENETCONN	ENETCONN	ENETCONN	ENETCONN_1	
ENETCONN	ENETCONN	ENETCONN	ENETCONN_1	
ENETCONN	ENETCONN	ENETCONN	ENETCONN_2	
ENETCONN	ENETCONN	ENETCONN	ENETCONN_2	
ENETCONN	ENETCONN	ENETCONN	ENETCONN_3	
ENETCONN	ENETCONN	ENETCONN	ENETCONN_3	
VESTA_CLK25M_XTAL	XTAL	XTAL		
VESTA_CLK25M_XTALO	XTAL	XTAL		
VESTA_CLK25M_XTALO_R	XTAL	XTAL		

Page Notes

Power aliases required by this page:
 - =PP2V5_ENETFW
 - =PP1V2_ENETFW

Signal aliases required by this page:
 (NONE)

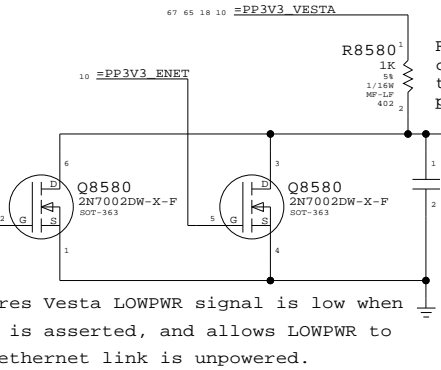
BOM options provided by this page:
 (NONE)

Net Spacing Type: ENET_MDI

Time to Line: 0.38 nms
 Length Tolerance: 50 mils
 Primary Max Sep: 5 mils
 Secondary Max Sep: 100 mils
 Secondary Length: 500 mils

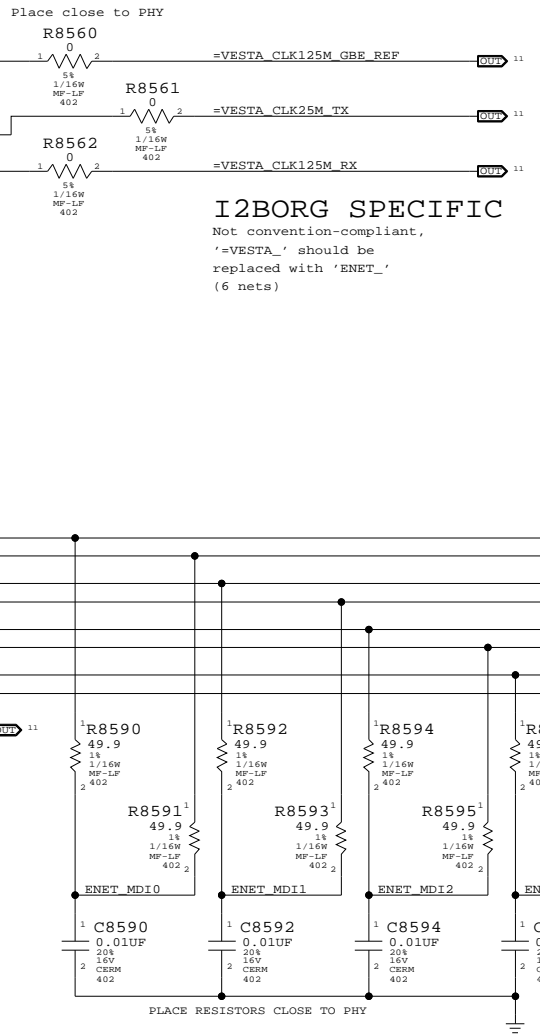
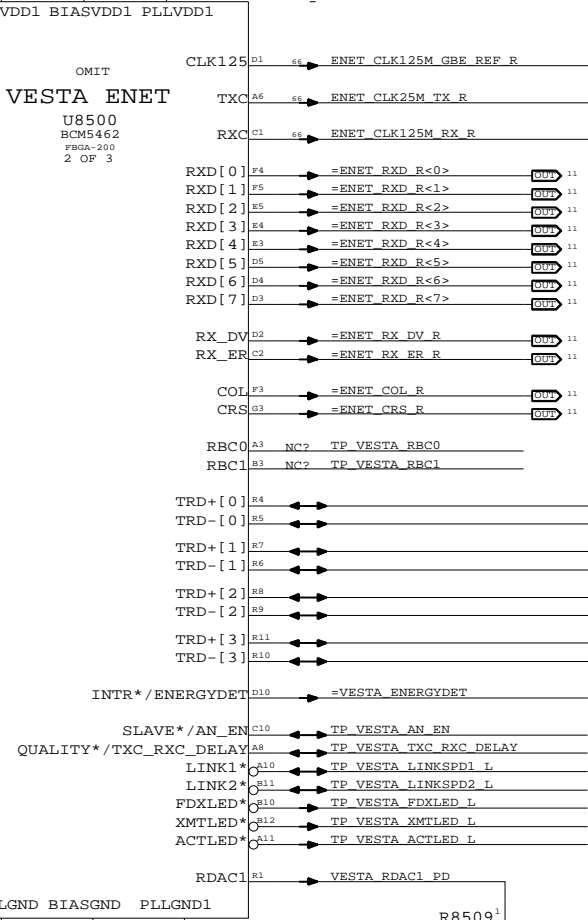
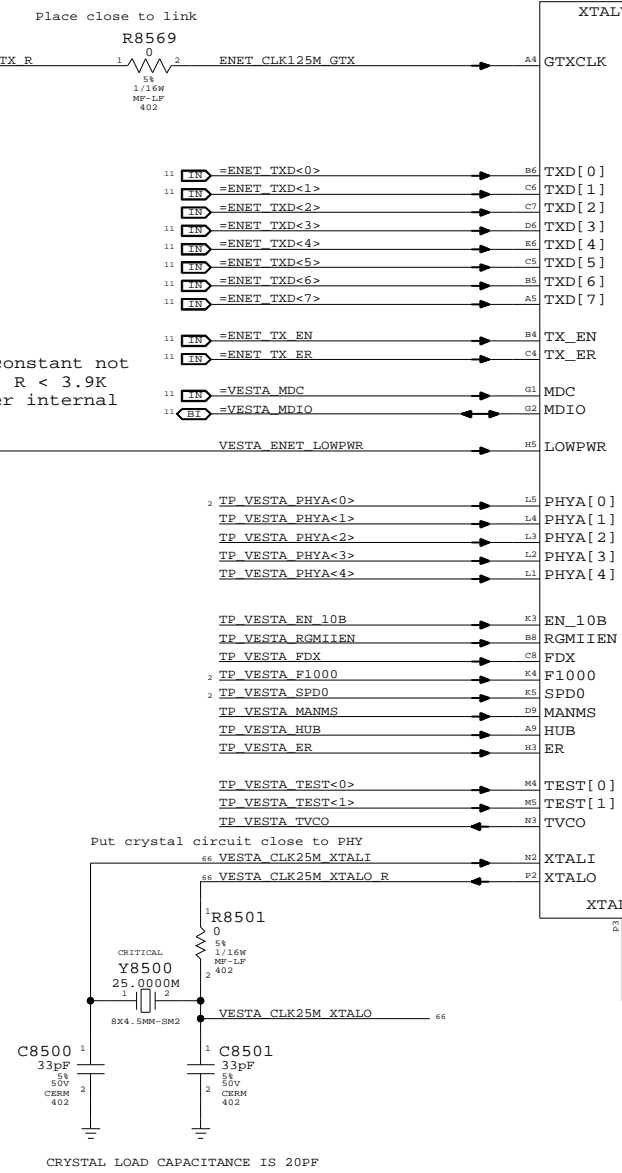
NOTE: Target differential impedance for ENET data pairs is 100 ohms.

Vesta Ethernet LowPwr Disables Vesta Ethernet Circuit



Vesta Config Straps:

PHYA<4..0> - PHY Address Select (Internal Pull-downs)	MANMS - Manual Master/Slave Configuration Select (Internal Pull-downs)
EM_10B - TBI Interface Select (Internal Pull-down)	HUB - Repeater Select (Internal Pull-down)
RGMIEN - RGMII Enable (Internal Pull-down)	ER - Edge Rate Select (Internal Pull-down)
FDX - Full-Duplex Select (Internal Pull-up)	AN_EN - Auto-Negotiation Select (Internal Pull-up)
F1000 - Speed Select (Internal Pull-up)	TXC_RXC_DELAY - TXC/RXC Delay (Internal Pull-up)
SPD0 - Speed Select (Internal Pull-down)	
AN_EN F1000 SPD0 Description	
0 0 0	Force 10BASE-T
0 0 1	Force 100BASE-TX
0 1 X	Force 1000BASE-T (test use only)
1 0 0	Auto-negotiate advertise 10BASE-T
1 0 1	Auto-negotiate advertise 10/100BASE-TX
1 1 0	Auto-negotiate advertise 10/100/1000BASE-T
1 1 1	Auto-negotiate advertise 1000BASE-T



Vesta Ethernet PHY

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

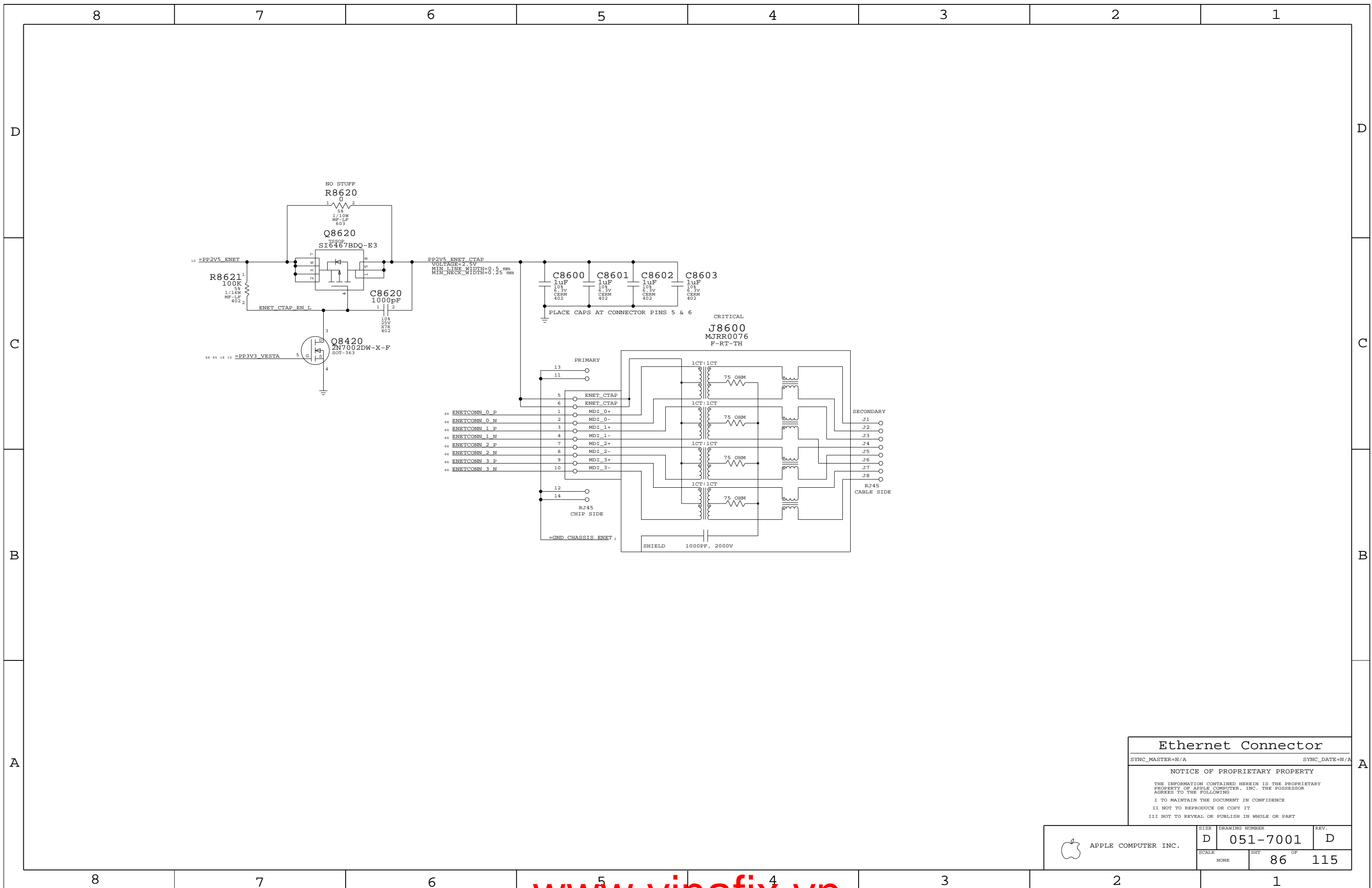
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APPLE COMPUTER INC.	SCALE: NONE	SHEET: 85 OF 115	SIZE: D	DRAWING NUMBER: 051-7001	REV.: D
---------------------	-------------	------------------	---------	--------------------------	---------



Ethernet Connector

SYNC_MASTER=N/A SYNC_DATE=N/A

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	SCALE NONE	SHEET 86	OF 115

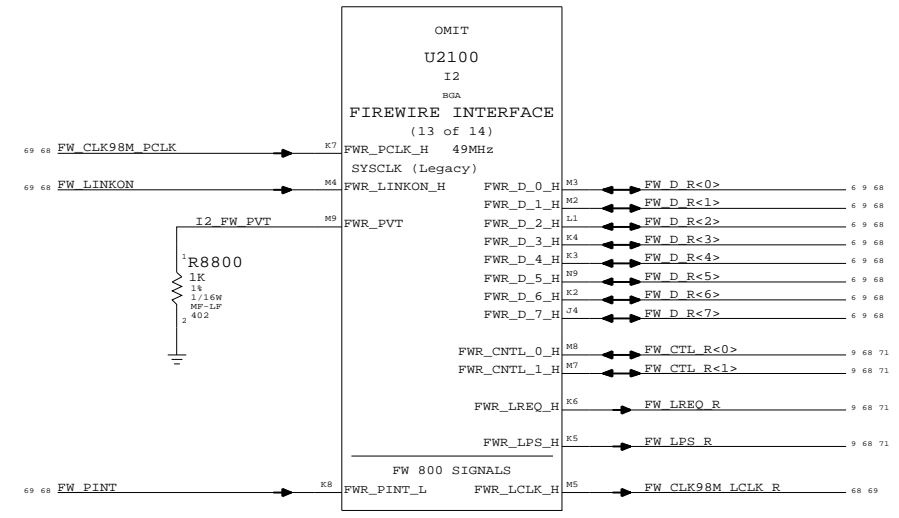
ELECTRICAL_CONSTRAINT_SET	NET_TYPE				
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR		
FW_D	FW	FW		FW D R<7..0>	6 9 68
FW_CTL	FW	FW		FW CTL R<1..0>	9 68 71
FW_LREQ	FW	FW		FW LREQ R	9 68 71
	FW	FW		FW LPS R	9 68 71
	FW	FW		FW LINKON	68 69
FW_PCLK	CLOCK	CLOCK		FW CLK98M_PCLK	68 69
FW_LCLK	CLOCK	CLOCK		FW CLK98M_LCLK R	68 69
FW_PINT	FW	FW		FW PINT	68 69

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



I2 FireWire Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-7001	D
SCALE	SHT OF		
NONE	88 OF		115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
PROVIDED	FW	FW	FW_PORT1_TPA_P_FL
BY	FW	FW	FW_PORT1_TPA_N_FL
	FW	FW	FW_PORT1_TPB_FL
PHY	FW	FW	FW_PORT1_TPB_N_FL
	FW	FW	FW_PORT2_TPA_P_FL
PAGE	FW	FW	FW_PORT2_TPA_N_FL
	FW	FW	FW_PORT2_TPB_P_FL
	FW	FW	FW_PORT2_TPB_N_FL

Page Notes

Power aliases required by this page:
 - _PPFW_PORT1
 - _PPFW_PORT2
 - _PPFW_PORT3
 - _PP3V3_FW
 - _GND_CHASSIS_FW_PORT1
 - _GND_CHASSIS_FW_PORT2
 - _GND_CHASSIS_FW_PORT3

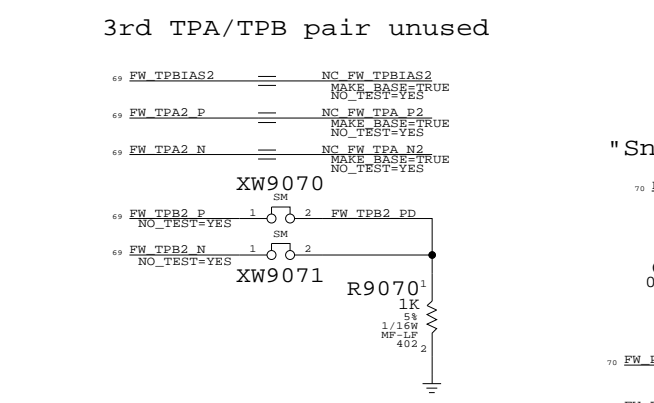
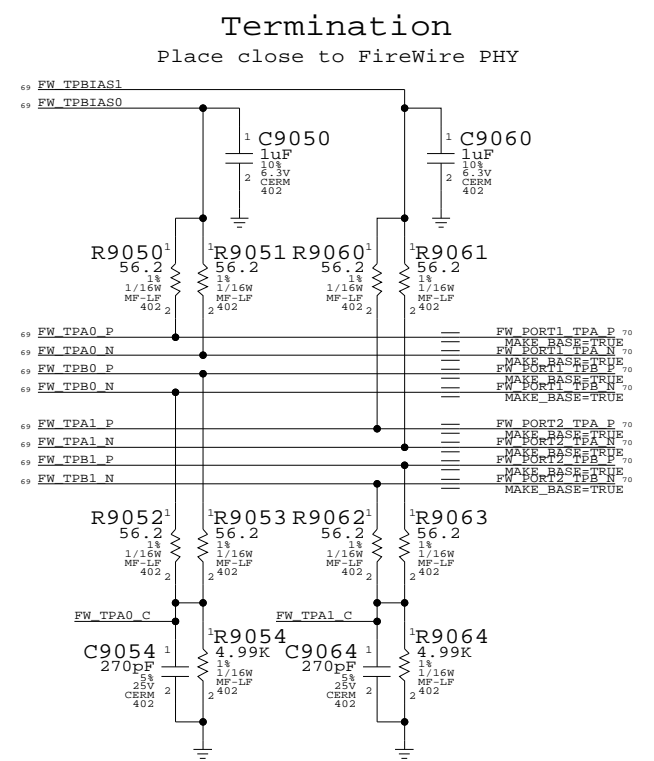
Signal aliases required by this page:
 (NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

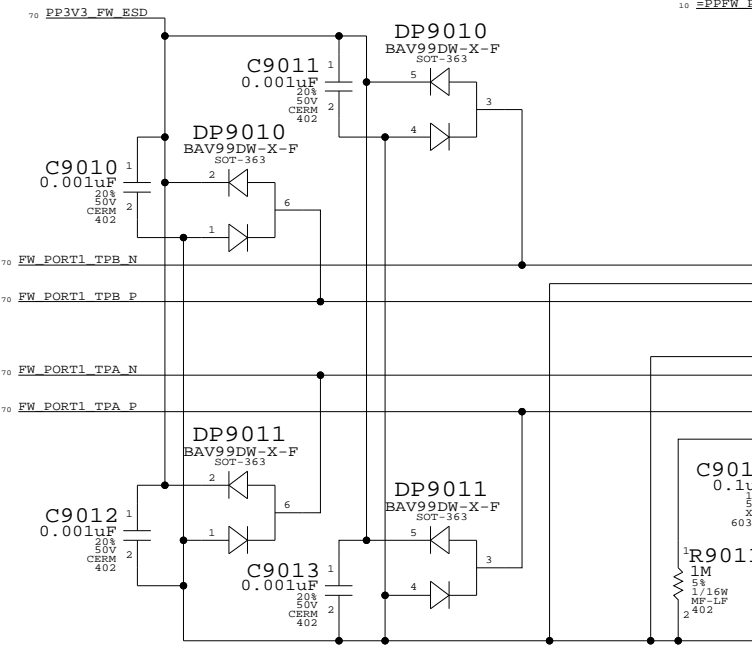
BOM options provided by this page:
 (NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

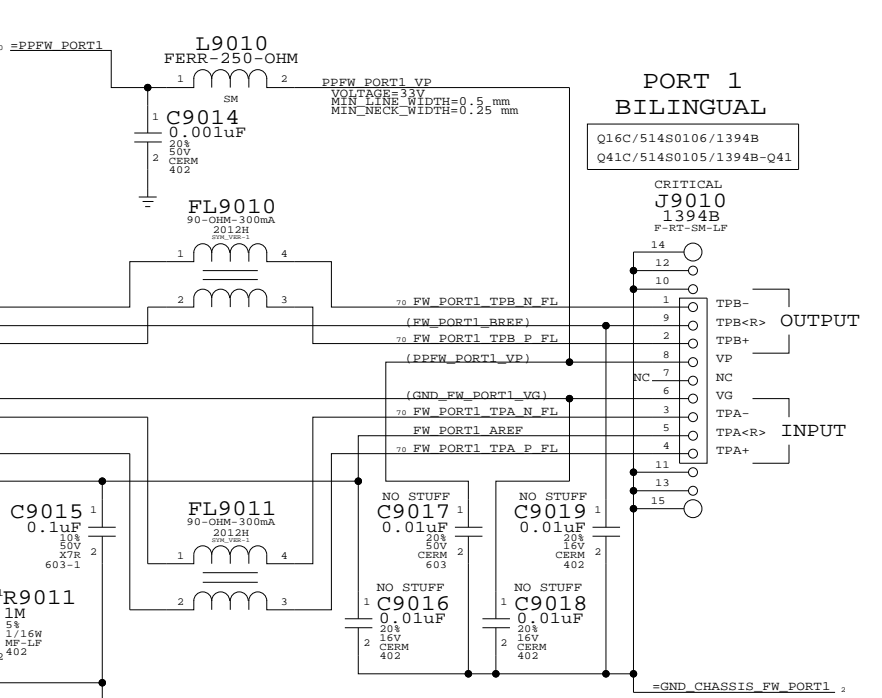
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)



"Snapback" & "Late VG" Protection



Cable Power

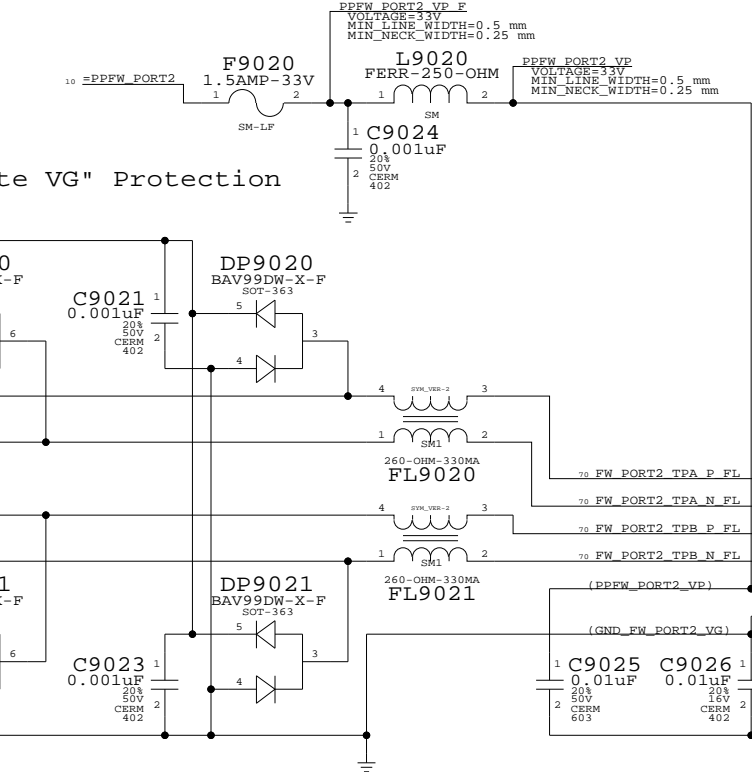


AREF needs to be isolated from all local grounds per 1394b spec

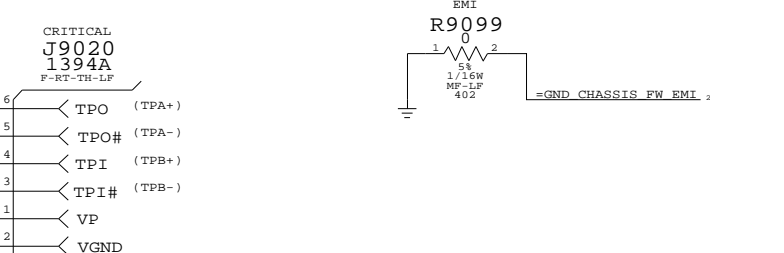
When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

Cable Power



PORT 2 1394A



FireWire Ports

SYNC_MASTER=N/A SYNC_DATE=N/A

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C

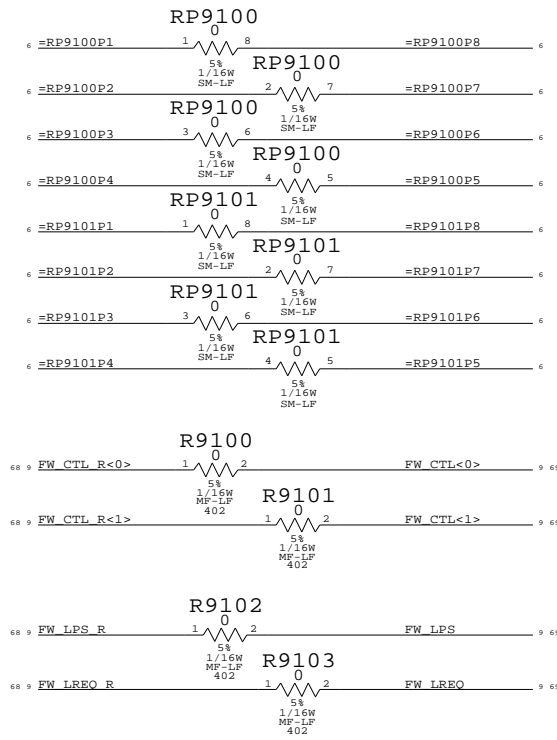
B

B

A

A

Place series terminators approximately halfway between Vesta and NB.
(They should probably be slightly closer to Vesta than the NB.)



FireWire Series Term

SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-7001	D
SCALE	SHT OF		
NONE	91 OF		115

8

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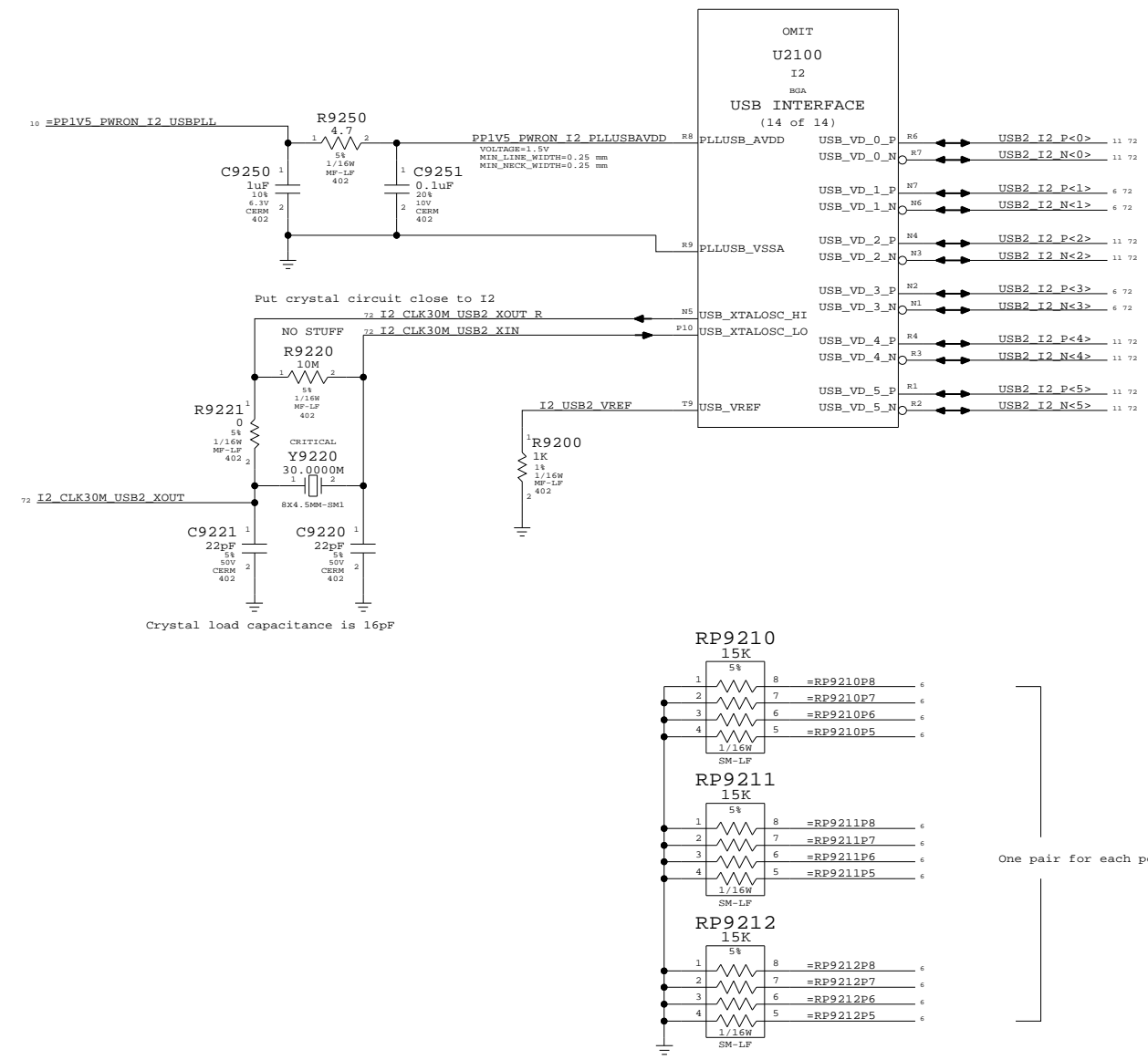
1

ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
USB2_0	USB2	USB2	USB2_I2_0	USB2_I2 P<0>
USB2_0	USB2	USB2	USB2_I2_0	USB2_I2 N<0>
USB2_1	USB2	USB2	USB2_I2_1	USB2_I2 P<1>
USB2_1	USB2	USB2	USB2_I2_1	USB2_I2 N<1>
USB2_2	USB2	USB2	USB2_I2_2	USB2_I2 P<2>
USB2_2	USB2	USB2	USB2_I2_2	USB2_I2 N<2>
USB2_3	USB2	USB2	USB2_I2_3	USB2_I2 P<3>
USB2_3	USB2	USB2	USB2_I2_3	USB2_I2 N<3>
USB2_4	USB2	USB2	USB2_I2_4	USB2_I2 P<4>
USB2_4	USB2	USB2	USB2_I2_4	USB2_I2 N<4>
USB2_5	USB2	USB2	USB2_I2_5	USB2_I2 P<5>
USB2_5	USB2	USB2	USB2_I2_5	USB2_I2 N<5>
USB2_I2_XTAL	XTAL	XTAL		I2_CLK30M_USB2_XOUT_R
(USB2_I2_XTAL)	XTAL	XTAL		I2_CLK30M_USB2_XOUT
(USB2_I2_XTAL)	XTAL	XTAL		I2_CLK30M_USB2_XIN

Page Notes

Power aliases required by this page:
 - =PP1V5_PWRON_USB
 Signal aliases required by this page:
 - =RP92xxPy (pinswappable USB pulldowns)
 BOM options provided by this page:
 (NONE)

Net Spacing Type: USB2
 Line To Line: 19.5 mils
 Length Tolerance: 50 mils
 Primary Max Sep: 7.5 mils
 Secondary Max Sep: 100 mils
 Secondary Length: 500 mils
 NOTE: Target differential impedance for USB2 data pairs is 90 ohms.



One pair for each port USB2_*<0..5>

I2 USB Interface
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ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
E30	USB2	USB2	USB2_NEC_0
E31	USB2	USB2	USB2_NEC_N<0>
E32	USB2	USB2	USB2_NEC_P<1>
E33	USB2	USB2	USB2_NEC_N<1>
E34	USB2	USB2	USB2_NEC_P<2>
E35	USB2	USB2	USB2_NEC_N<2>
E36	USB2	USB2	USB2_NEC_P<3>
E37	USB2	USB2	USB2_NEC_N<3>

E40	USB2_NEC_XTAL	XTAL	XTAL	NEC_CLK30M_XT1
E41		XTAL	XTAL	NEC_CLK30M_XT2
E42		XTAL	XTAL	NEC_CLK30M_XT2_R

Page Notes

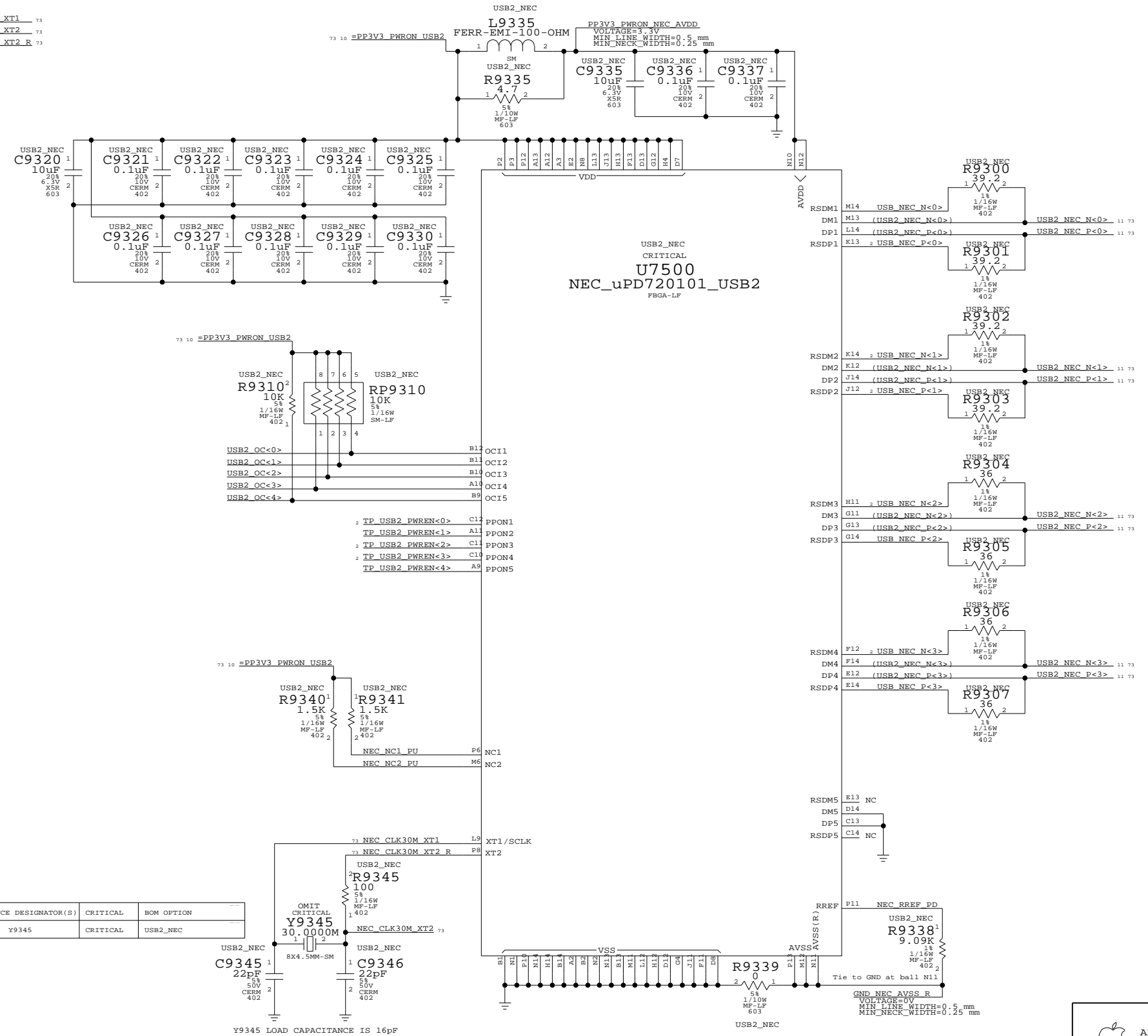
Power aliases required by this page:
 - =PP3V3_PWRON_USB2

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 USB2_NEC

Net Spacing Type: USB2

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
19750087	1	XTAL_CER.30.000MHZ.LW PROF.8X4.5MM.SMD	Y9345	CRITICAL	USB2_NEC

NEC USB2 Interface

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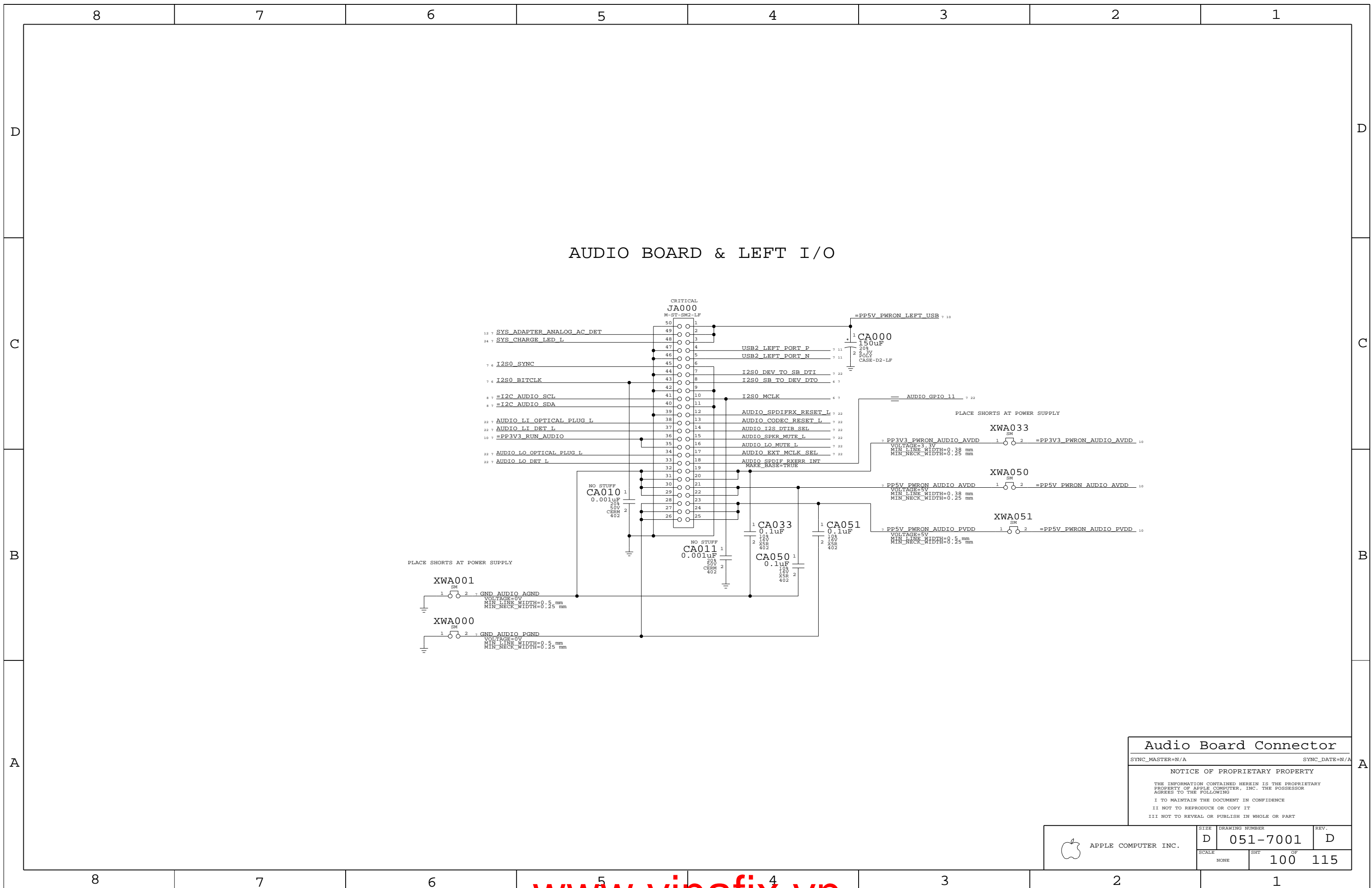
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AUDIO BOARD & LEFT I/O

Audio Board Connector

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NONE	100		115

	8	7	6	5	4	3	2	1					
D	AGP TABLE_SPACING_RULE TABLE_SPACING_RULE AGP 401 * 0.4 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_SPACING_RULE AGP_STB 601 * 0.6 MM 2.5 MM =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE AGP * =STANDARD =60_OHM_SE =60_OHM_SE =60_OHM_SE TABLE_PHYSICAL_RULE AGP_STB * =STANDARD =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF					AUDIO TABLE_SPACING_RULE TABLE_SPACING_RULE AUDIO 251 * 0.25 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE AUDIO * =50_OHM_SE =50_OHM_SE =50_OHM_SE =50_OHM_SE							
	CLOCK TABLE_SPACING_RULE TABLE_SPACING_RULE CLOCK 251 * 0.25 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE CLOCK * =STANDARD =50_OHM_SE =50_OHM_SE =50_OHM_SE					I2S TABLE_SPACING_RULE TABLE_SPACING_RULE I2S 251 * 0.25 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE I2S * =50_OHM_SE =50_OHM_SE =50_OHM_SE =50_OHM_SE							
	ENET (Ethernet Digital) TABLE_SPACING_RULE TABLE_SPACING_RULE ENET_SELF =STANDARD * =STANDARD =STANDARD =STANDARD =STANDARD =STANDARD TABLE_SPACING_RULE ENET 201 * 0.2 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE ENET * =STANDARD =50_OHM_SE =50_OHM_SE =50_OHM_SE					ENETCONN TABLE_SPACING_RULE TABLE_SPACING_RULE ENETCONN 501 * 0.50 MM 3.81 MM =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE ENETCONN * =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF							
	FW (FireWire Digital) TABLE_SPACING_RULE TABLE_SPACING_RULE FW_SELF =STANDARD * =STANDARD =STANDARD =STANDARD =STANDARD =STANDARD TABLE_SPACING_RULE FW 201 * 0.2 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE FW * =STANDARD =50_OHM_SE =50_OHM_SE =50_OHM_SE					FW_TP TABLE_SPACING_RULE TABLE_SPACING_RULE FW_TP 501 * 0.50 MM 3.81 MM =110_OHM_DIFF =110_OHM_DIFF =110_OHM_DIFF TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE FW_TP * =110_OHM_DIFF =110_OHM_DIFF =110_OHM_DIFF =110_OHM_DIFF							
	I2C TABLE_SPACING_RULE TABLE_SPACING_RULE I2C 201 * 0.2 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE I2C * =STANDARD =50_OHM_SE =50_OHM_SE =50_OHM_SE					I2_FBCLK / XTAL TABLE_SPACING_ASSIGNMENT TABLE_SPACING_ASSIGNMENT I2_FBCLK * * CLOCK TABLE_SPACING_ASSIGNMENT XTAL * * CLOCK TABLE_PHYSICAL_ASSIGNMENT TABLE_PHYSICAL_ASSIGNMENT I2_FBCLK * * CLOCK TABLE_PHYSICAL_ASSIGNMENT XTAL * * CLOCK							
	MaxBus TABLE_SPACING_RULE TABLE_SPACING_RULE MAXBUS 151 * 0.15 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE MAXBUS * =STANDARD =50_OHM_SE =50_OHM_SE =50_OHM_SE												
	PCI TABLE_SPACING_RULE TABLE_SPACING_RULE PCI =STANDARD * =STANDARD =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE PCI * =STANDARD =50_OHM_SE =50_OHM_SE =50_OHM_SE												
	RAM TABLE_SPACING_RULE TABLE_SPACING_RULE RAM 201 * 0.2 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_SPACING_RULE RAM_DIFF 251 * 0.25 MM 2.5 MM =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE RAM * =50_OHM_SE =50_OHM_SE =50_OHM_SE =50_OHM_SE TABLE_PHYSICAL_RULE RAM_DIFF * =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF												
	UATA TABLE_SPACING_RULE TABLE_SPACING_RULE UATA 151 * 0.15 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE UATA * =50_OHM_SE =50_OHM_SE =50_OHM_SE =50_OHM_SE												
	USB2 TABLE_SPACING_RULE TABLE_SPACING_RULE USB2 501 * 0.50 MM 3.81 MM =90_OHM_DIFF =90_OHM_DIFF =90_OHM_DIFF TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE USB2 * =90_OHM_DIFF =90_OHM_DIFF =90_OHM_DIFF =90_OHM_DIFF												
	8	7	6	5	4	3	2	1					
C													
B													
A													

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	8	7	6	5	4	3	2	1
D								
C								
B								
A								
	8	7	6	5	4	3	2	1

TABLE_SPACING_RULE								
TABLE_SPACING_RULE	DVO	151	*	0.15 MM	-STANDARD	-STANDARD	-STANDARD	-STANDARD
TABLE_PHYSICAL_RULE	DVO							
TABLE_PHYSICAL_RULE	DVO	*		=STANDARD	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE
TABLE_SPACING_RULE								
TABLE_SPACING_RULE	TV	151	*	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE
TABLE_SPACING_RULE	TV_CONN	151	*	-TV	-TV	-TV	-TV	-TV
TABLE_PHYSICAL_RULE								
TABLE_PHYSICAL_RULE	TV	*		=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE
TABLE_PHYSICAL_RULE	TV_CONN	*		-TV	-TV	-TV	-TV	-TV
TABLE_SPACING_RULE								
TABLE_SPACING_RULE	VGA	151	*	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE
TABLE_SPACING_RULE	VGA_CONN	151	*	-VGA	-VGA	-VGA	-VGA	-VGA
TABLE_PHYSICAL_RULE								
TABLE_PHYSICAL_RULE	VGA	*		=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE
TABLE_PHYSICAL_RULE	VGA_CONN	*		=VGA	=VGA	=VGA	=VGA	=VGA
TABLE_SPACING_RULE								
TABLE_SPACING_RULE	LVDS	151	*		=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TABLE_PHYSICAL_RULE								
TABLE_PHYSICAL_RULE	LVDS	*		=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TABLE_SPACING_RULE								
TABLE_SPACING_RULE	TMDS	251	*	0.25 MM	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TABLE_SPACING_RULE	TMDS_CONN	=TMDS	*	=TMDS	=TMDS	=TMDS	=TMDS	=TMDS
TABLE_PHYSICAL_RULE								
TABLE_PHYSICAL_RULE	TMDS	*		=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TABLE_PHYSICAL_RULE	TMDS_CONN	*		=TMDS	=TMDS	=TMDS	=TMDS	=TMDS
TABLE_SPACING_RULE								
TABLE_SPACING_RULE	THERM	251	*	0.25 MM	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TABLE_PHYSICAL_RULE								
TABLE_PHYSICAL_RULE	THERM	*		Y	0.25 MM	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

DVO

S-VIDEO

VGA

LVDS

TMDS

THERM

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