1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

DRAWING

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
02		248015	ENGINEERING RELEASED	12/05/02	?

SCHEM,MLB,PB15

Thu Aug 7 21:07:05 2003

BOM OPTIONS (IN COMMON PARTS)

STUFF	NO STUFF
1_8V_MAXBUS	1_5V_MAXBUS
SSCG	NO_SSCG
5V_HD_LOGIC	3V_HD_LOGIC
NO_BBANG	BBANG
INT_2_5V_COLD	INT_2_5V_HOT
ATI_MEMIO_HI	ATI_MEMIO_LO
USB_MODEM	SOFT_MODEM
GPU_PWRMSR	INT_TMDS
GPU_SS	
VGA_BUFFER_RES	
EXT_TMDS	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6338	1	SCHEM,MLB,PB15	SCH1	
820-1441	1	PCBF,MLB,PB15	PCB1	
065-3951	1	CMNPRTS,MLB,PB15	DMS1	DMS630-4285&DMS630-4721
065-3952	1	SELPRTS,MLB,PB15,BTR	DMS2	DMS630-4285
065-4479	1	SELPRTS,MLB,PB15,BST	DMS3	DMS630-4721

DIMENSIONS ARE IN MILLIMETERS
XX ± ____
X.XX ± ____
X.XXX ± ____
ANGLES ° ____
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER	/	DESIGN CK	/
ENG APPD	/	MFG APPD	/
QA APPD	/	DESIGNER	/
RELEASE	/	SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer Inc.

TITLE
SCHEM,MLB,PB15"

DRAWING NUMBER 401243 REV. AA

SHT 1 OF 44

U51 INTREPID

J23 Ethernet Connector P.26
4 DATA PAIRS
U43 Ethernet PHY P.26
G/MII
3.3V
10/100/1000
8BIT TX
8BIT RX
125MHZ

J24 FW - A Connector P.28
2 DATA PAIRS @ 200MHz
J20 FW - B Connector P.28
2 DATA PAIRS @ 400MHZ
U36 FireWire PHY P.27
1394 OHCI
3.3V
8BIT TX/RX
50MHZ

J13 OPTICAL DRIVE Connector P.24
EIDE
J12 ULTRA ATA/100 Connector P.24
UIDE

J2 RUX Board Connector P.23
J19 LMU LUX Board Connector P.23
J3 LIO/Audio Connector P.25
I2S
I2C
I2C
U53/J1/J18 Fan Circuit P.25

J26 Battery Connector P.30
Power Supply & Charger P.30-34
J27 DC-In Connector P.30
J8 SLEEP LED P.23
SMBUS
3.3V
U28 PMU P.29
SERIAL
5V
J10 TRACKPAD Connector P.23
J11 Keyboard Connector P.23

J5 CARDBUS Connector P.18
33MHZ
16/32 BITS
3.3V/5V
U8 TI PCI1510 CardBus Controller P.18

NOT USED

ETHERNET 10/100/1000 P.13	FIREWIRE 400 MB/S P.13	UATA 100 P.13	EIDE P.13	CARDSLOT P.13	I2S P.14	I2C P.13 P.14

NOT USED
USB PORT A P.14
NOT USED
USB PORT B P.14
NOT USED
USB PORT C P.14
NOT USED
USB PORT D P.14
USB PORT E P.14
USB PORT F P.14
MAXBUS P.8

SCCA P.14 → J28 Serial Debug Connector P.25
VIA/PMU P.14
BOOTROM P.12 → U11 BOOT ROM 1M X 8 P.9
PCI 64BITS 33MHZ P.12 → J6 AIRPORT Connector P.24
4X AGP P.12

J3 BlueTooth (LIO) P.25
J15 Modem/SW Modem Connector P.25
INTREPID I2C
MAXBUS 1.8V 167MHZ 32BIT ADDRESS 64BIT DATA

PCI BUS 32BITS 33MHZ 3.3V

AGP BUS 1.5V/3.3V 32BITS 66MHZ
U47 ATI M10 64MB P.19-21
MEMORY CH. A (INTERNAL MEM)
MEMORY CH. C (INTERNAL MEM)
MEMORY CH. B (INTERNAL MEM)
MEMORY CH. D (INTERNAL MEM)

U17 NEC USB2.0 EHCI HC P.17
J3 LEFT USB (VIA LIO) P.25
J17 RIGHT USB (VIA STATLER) P.25

U56 APOLLO CPU (MPC7447) P.5-6
CPU PLL Config P.7
PMU

DDR MEMORY P.9
MEMORY BUS 2.5V 167MHZ 64BITS
U16/U18/U28/U27 2:1 DDR MUXES P.10
J25 DDR SDRAM DIMM 0
DDR SDRAM DIMM 1 SO-DIMM Connector P.11

J4 Inverter Connector P.22

LVDS
EDID (I2C)
S-VIDEO
COMPOSITE
TMDS (VIA SIL1162)
RGB
DDC

J14 LCD Panel Connector P.22
J21 S-Video Connector P.22
J22 DVI-I Connector P.22

SYSTEM BLOCK DIAGRAM

APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 401243 | REV. AA
SCALE NONE | SHT 2 OF 44

POWER SYSTEM ARCHITECTURE

AC ADAPTER IN PG 30

INRUSH LIMITER PG 30

+24V_PBUS

1V20_REF
>-13.44V TURNS-ON
<-13.44V SHUTS-OFF
PG 31

RUN/SS
BUCK REGULATOR (LTC1625) PG 31
VCC
AC: 12.8V
NO AC: BATTERY VOLTAGE 1625 NOT RUNNING
SHUTDOWN: RUNNING
SLEEP: RUNNING
RUN: RUNNING

+PBUS

14V_PBUS

+3V_PMU LDO PG 31

+BATT

+5V_MAIN

+3V_PMU

+4_6V_BU

RC AT 1M*0.047UF @ 24V
STARTS 2.0MSEC AFTER DCDC_EN_L BECOMES LOW

RUN/SS - 5V
TURNS ON AT >1V
<100UA ALLOWED
INTERNAL ZENER CLAMP TO 6V

MAIN 3V/5V DC/DC (LTC3707) PG 32
VCC
STBYMD
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING

INTERNAL ZENER CLAMP TO 6V
<100UA ALLOWED
TURNS ON AT >1V
RUN/SS - 3V

+5V_MAIN

3V_5V_OK

HOLDS BOTH RUN/SS AT GND WHEN IT'S CONNECTED TO GND

TURNS CONTROL TO RUN/SS WHEN IT'S OPEN

+3.3V_MAIN

RC AT 1M*0.1UF @ 24V
STARTS ~4.25MSEC AFTER DCDC_EN_L BECOMES LOW

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

+24V_PBUS

BACKUP BATTERY

14V_PBUS

14V CHARGES BACKUP BATTERY

24V IS OUTPUT ONLY FROM BACKUP BATTERY

CHARGER INPUT & BOOST OUTPUT PG 31

BACKUP BATTERY CIRCUIT CHARGES OFF +PBUS AND PREVENTS +PBUS AND +24V_PBUS FROM DROPPING BELOW 6V (UNTIL DRAINED)

BATTERY CHARGER (MAX1772) PG 30

+BATT

3S 2P 18650 CELLS

DC/DC (LTC3411) PG 34
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING

+1.8V_MAIN

MAXBUS

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

BATTERY VOLTAGE FEED-IN PATH PG 30

+PBUS

BACKLIGHT INVERTER

+5V_MAIN

VCC
MAIN 2.5V/1.5V DC/DC (MAX1715) PG 34
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING

PGOOD

TURNS ON OUTPUT @ 2.4V ON1/ON2

MAP31 DDR CORE
MAP31 DDR I/O
DDR POWER
+2.5V_MAIN

1_5V_2_5V_OK

+1.5V_MAIN

INTREPID CORE
AGP I/O

+5V_MAIN

DCDC_EN_L

AFTER PMU IS UP AND RUNNING DCDC_EN_L WILL PULL ON1/ON2 LOW IN SHUTDOWN

+PBUS

+5V_MAIN

VCC
EXT_VCC
DC/DC (LTC1778)
SHUTDOWN: STOPPED
SLEEP: D3COLD
RUN: RUNNING

TURNS ON AS LOW AS 0.8V/TYP 1.5V
INTERNAL 1.2UA CURRENT SOURCE

RUN/SS PG 20

GPU_VCORE +1.2V

DCDC_EN
SLEEP
D3_COLD

GPU_VCORE SEQUENCING

1M & 0.1UF @14V, IT TAKES ~5.88MS TO START SWITCHER

1_5V_2_5V_OK

D3_HOT

DCDC_EN_L
D3_HOT

1_5V_2_5V_OK WILL NOT PULL LOW UNTIL +5V_MAIN TURNS ON

HOWEVER, 5V SHOULD TURN ON ~2.23MS AFTER DCDC_EN_L OR PMU_POWERUP_L BECOMES '1'; MUCH LESS THAN THE RC CHARGING AT INT_VCC (5V)

DCDC_EN
SLEEP

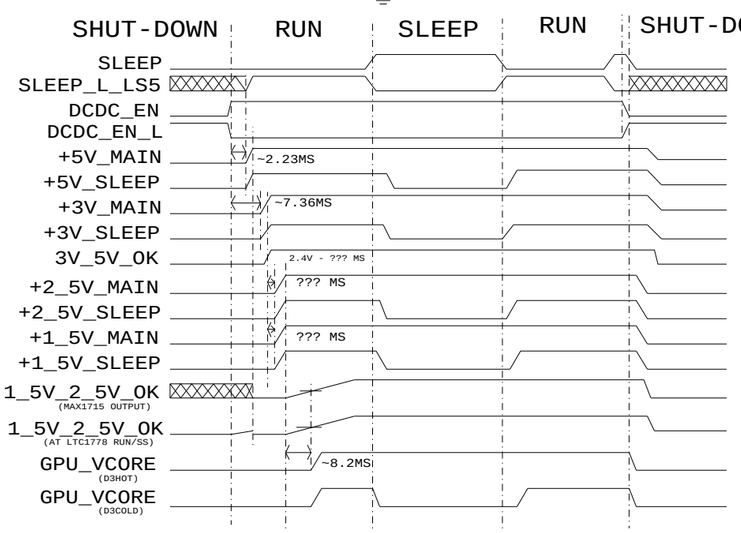
MAXBUS SEQUENCING

+PBUS

+5V_MAIN

VCC
SHDN
DC/DC (MAX1717)
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING
PG 33

CPU_VCORE (+1.385V)



POWER BLOCK DIAGRAM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401243	AA

SCALE: NONE

SHT 3 OF 44

PCB SPECS

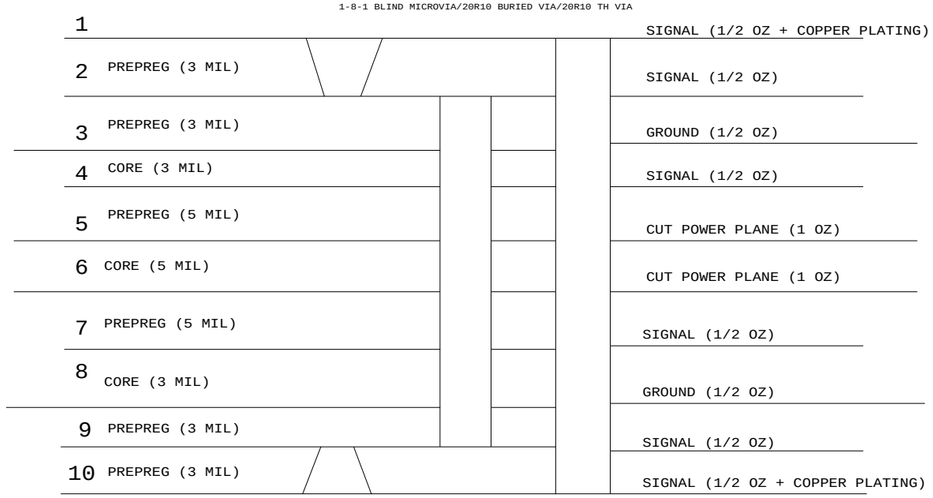
THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 10
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

1-8-1 BLIND MICROVIA/20R10 BURIED VIA/20R10 TH VIA



BOARD HOLES

CHASSIS MOUNTS

ASICS HEATSINK MOUNTS

ZT7 HOLE-VIA-20R10 LEFT CPU
ZT21 HOLE-VIA-20R10 UPPER RT GPU
ZT58 HOLE-VIA-20R10 LWR CPU
ZT59 HOLE-VIA-20R10 LWR RT GPU

I/O AREA

ZT85 HOLE-VIA-20R10 DVI — CHGND2
ZT86 HOLE-VIA-20R10 DVI 1394 — CHGND1
ZT16 HOLE-VIA-20R10 BATT. CHRGR — CHGND5

INVERTER

SH1 OG-503040 SHLD-SM — CHGND3

MECH. HOLES

ZT74 HOLE-VIA-20R10
ZT36 HOLE-VIA-20R10 — ZT301_SPN NO_TEST=TRUE
ZT23 HOLE-VIA-20R10 — ZT302_SPN NO_TEST=TRUE
ZT42 HOLE-VIA-20R10 — ZT10_SPN NO_TEST=TRUE

GROUND VIAS

ZT76, ZT28, ZT72, ZT69, ZT68, ZT64, ZT61, ZT38, ZT39, ZT40, ZT41, ZT46, ZT71, ZT78, ZT80 HOLE-VIA-20R10

ZT50, ZT51, ZT52, ZT53, ZT57, ZT60, ZT82, ZT22, ZT17, ZT35, ZT45, ZT79, ZT81, ZT83, ZT49 HOLE-VIA-20R10

ZT48, ZT47, ZT54, ZT55, ZT56, ZT84, ZT5, ZT15, ZT44, ZT4, ZT8, ZT6, ZT32, ZT3, ZT10 HOLE-VIA-20R10

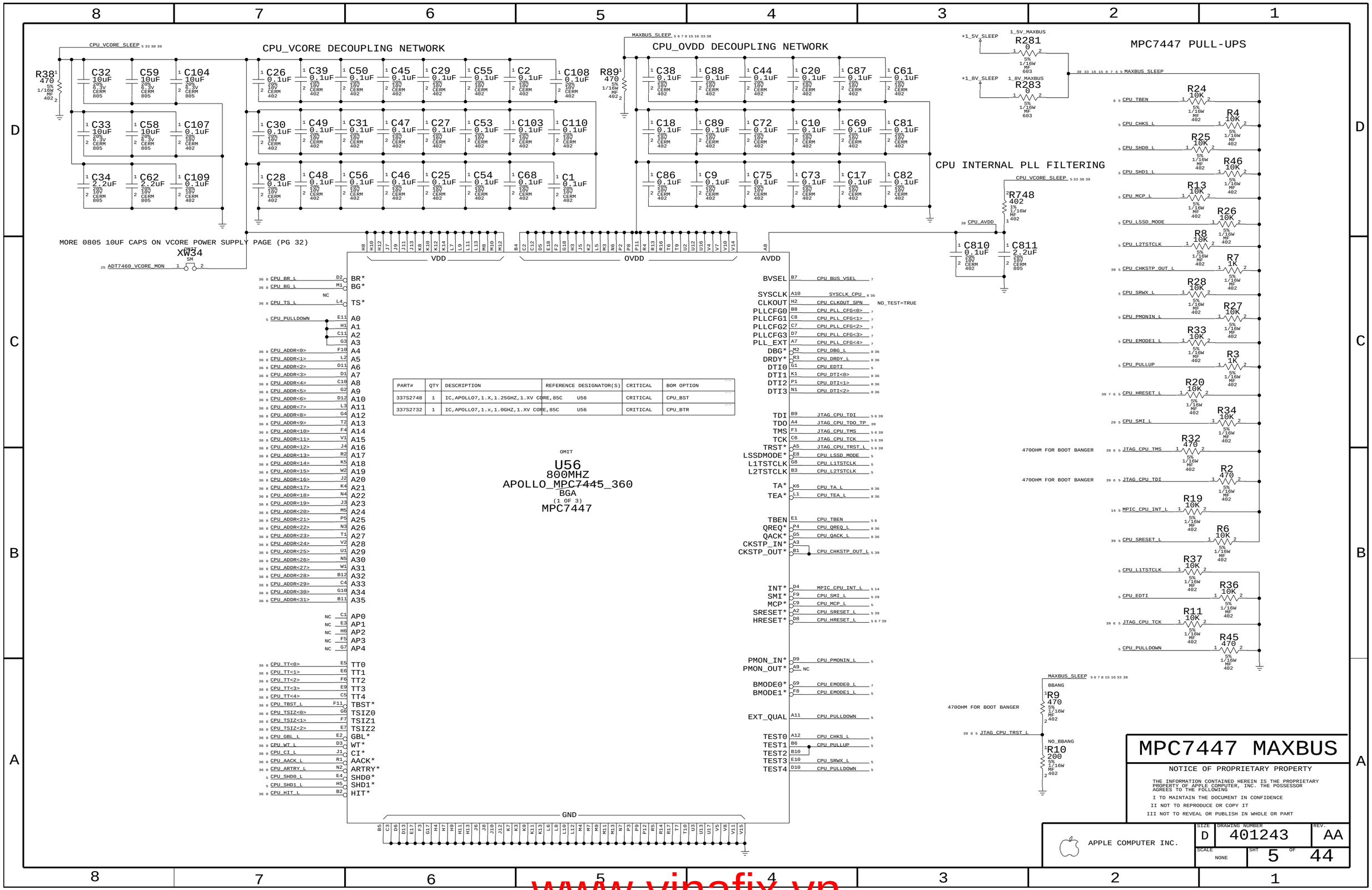
ZT11, ZT34, ZT20, ZT43, ZT70, ZT2, ZT9, ZT75, ZT73, ZT63, ZT77, ZT66, ZT62, ZT65, ZT13 HOLE-VIA-20R10

ZT25, ZT19, ZT24, ZT67, ZT37, ZT29, ZT31, ZT1, ZT14, ZT12, ZT27, ZT26, ZT30, ZT33, ZT18 HOLE-VIA-20R10

BOARD INFORMATION

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401243	AA
SCALE: NONE	SHT 4 OF 44	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S2748	1	IC,APOLLO7,1.X,1.25GHZ,1.XV CORE,85C	U56	CRITICAL	CPU_BST
337S2732	1	IC,APOLLO7,1.X,1.0GHZ,1.XV CORE,85C	U56	CRITICAL	CPU_BTR

MPC7447 MAXBUS

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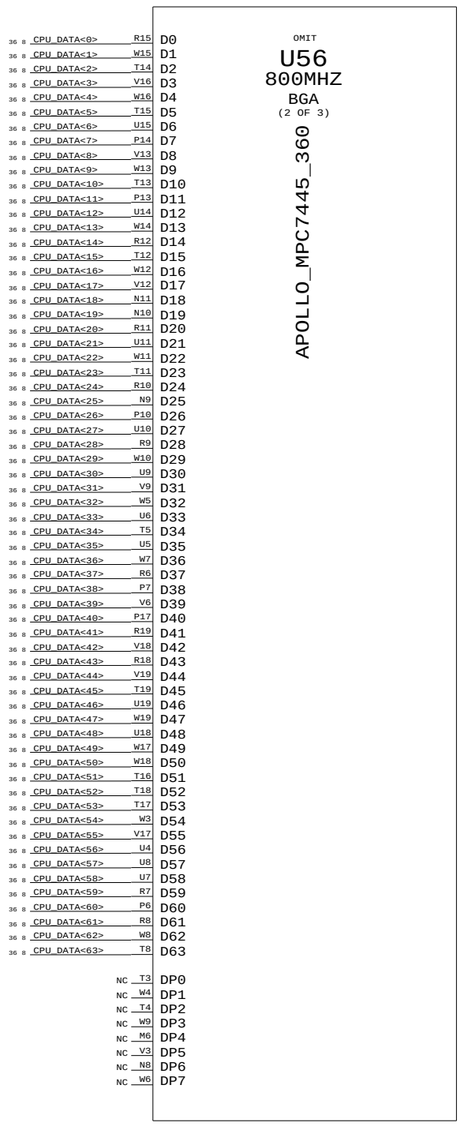
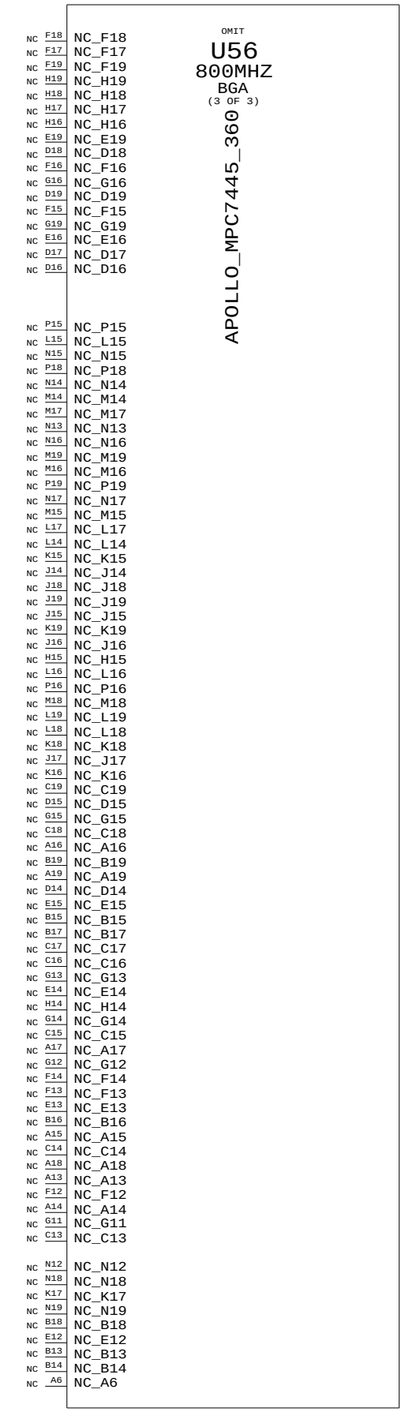
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401243	AA

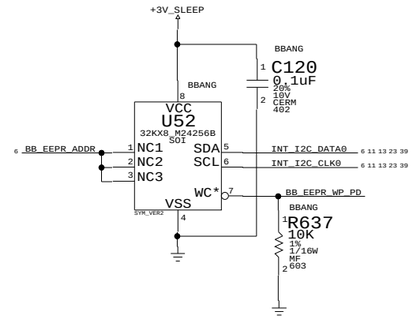
SCALE: NONE

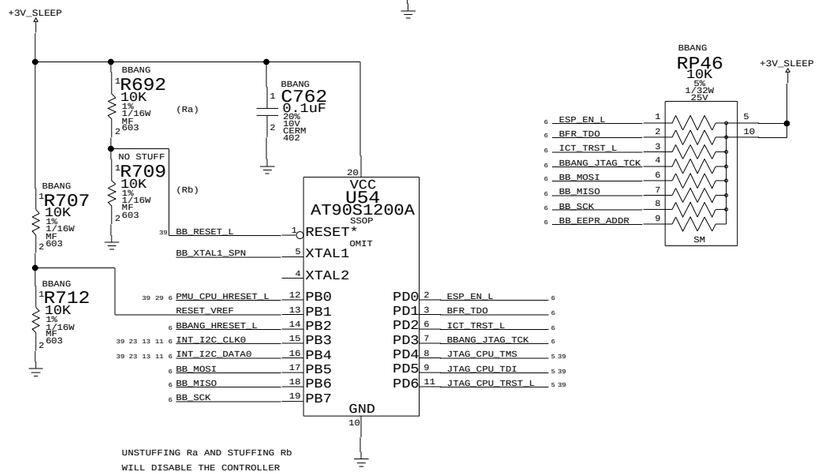
SHT 5 OF 44





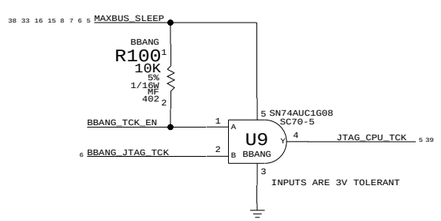
BOOT BANGER - TWEAK PROCESSOR BITS AFTER POWER-ON

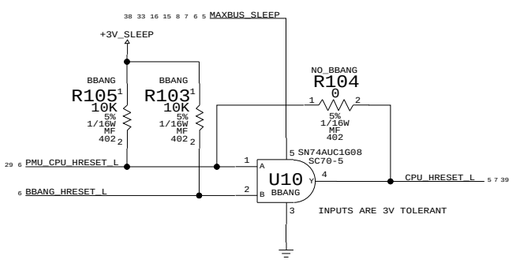




UNSTUFFING Ra AND STUFFING Rb
WILL DISABLE THE CONTROLLER

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1135	1	000-6240 FW GT4 BBANGER MCU,PROGRAMMED W/ BBANGER	U54	BBANG





MPC7447/BBANG

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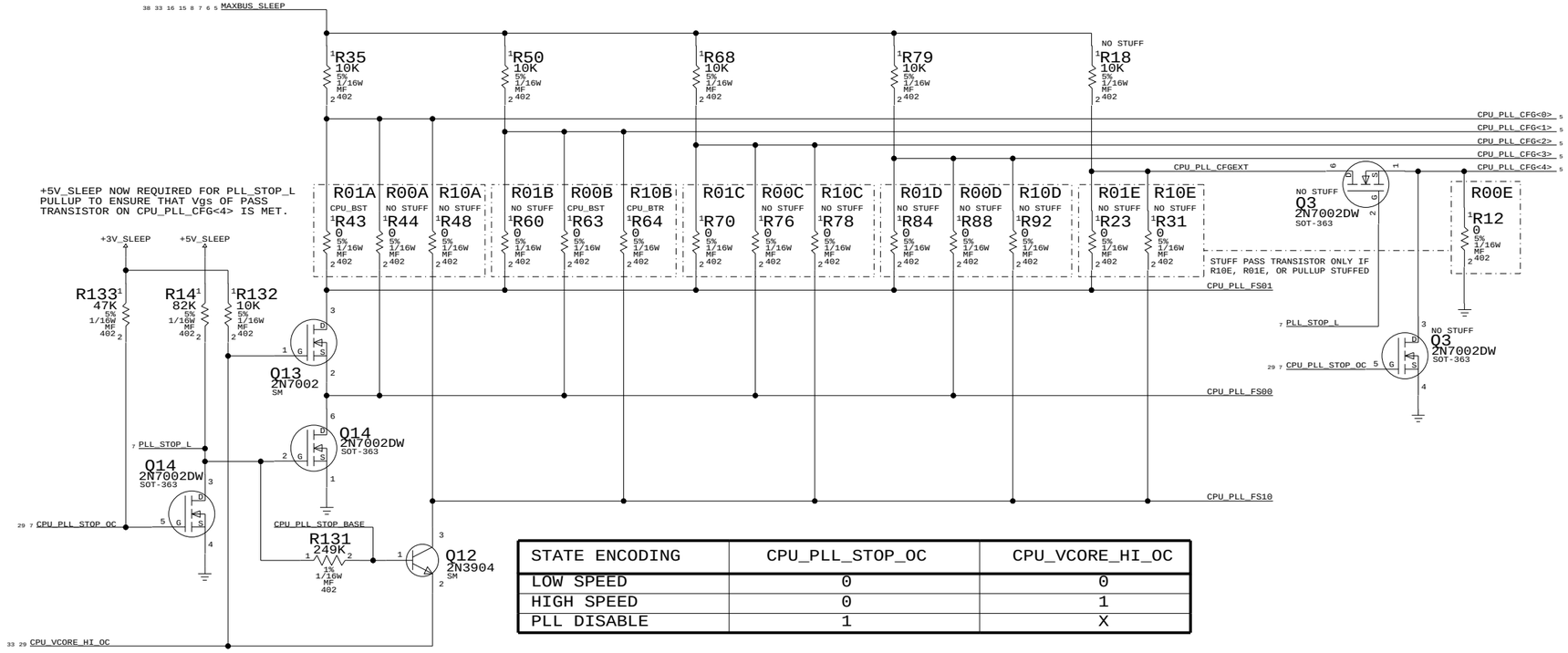
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401243	AA
SCALE: NONE	SHT 6 OF 44	

CPU PLL CONFIG CIRCUITRY



STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

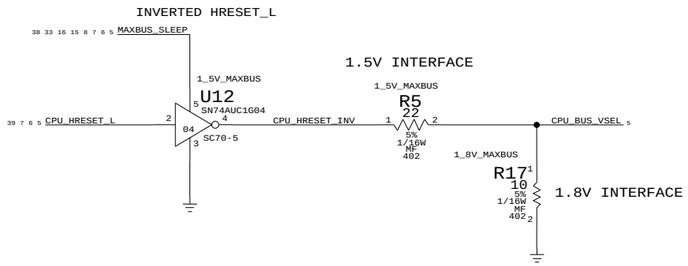
CPU FREQUENCY CONFIGURATION

APOLLO 7

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ (MHZ)	133MHZ (MHZ)	CPU_PLL_CFG 4 0123 E ABCD HEX
0.0X	PLL OFF		0 1111 0F
1.0X	PLL BYPASS		0 0011 03
2.0X	333	267	0 0100 04
3.0X	500	400	0 1000 08
4.0X	667	533	0 1010 0A
5.0X	833	667	0 1011 0B
5.5X	917	733	0 1001 09
6.0X	1000	800	0 1101 0D
6.5X	1083	867	0 0101 05
7.0X	1167	933	0 0010 02
7.5X	1250	1000	0 0001 01
8.0X	1333	1067	0 1100 0C
8.5X	1417	1133	0 0110 06
9.0X	1500	1200	1 0111 17
9.5X	1583	1267	0 0111 07
10.0X	1667	1333	1 1010 1A
10.5X	1750	1400	1 1000 18
11.0X	1833	1467	1 1001 19
11.5X	1917	1533	0 0000 00
12.0X	2000	1600	1 1011 1B
12.5X	2083	1667	1 1111 1F
13.0X	2167	1733	1 0101 15
13.5X	2250	1800	0 1110 0E
14.0X	2333	1867	1 1100 1C
15.0X	2500	2000	1 0001 11
16.0X	2667	2133	1 1101 1D
17.0X	2833	2267	1 0000 10
18.0X	3000	2400	1 0010 12
20.0X	3333	2667	1 0011 13
21.0X	3500	2800	1 0100 14
24.0X	4000	3200	1 0110 16
28.0X	4667	3733	1 1110 1E

CPU CONFIGURATION

MAXBUS VSEL



DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L NEED TO CHARACTERIZE

BUSTYPE SELECT

APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

CPU CONFIGURATION

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 401243 | REV. AA

SCALE NONE | SHT 7 OF 44

INTREPID BOOT STRAPS

BIT 32 TO 39

MAXBUS_SLEEP

NO STUFF R640[1] 10K 5% 1/16W MF 402	NO STUFF R639[1] 10K 5% 1/16W MF 402	NO STUFF R638[1] 10K 5% 1/16W MF 402	NO STUFF R666[1] 10K 5% 1/16W MF 402				
CPU_DATA<32>	CPU_DATA<33>	CPU_DATA<34>	CPU_DATA<35>	CPU_DATA<36>	CPU_DATA<37>	CPU_DATA<38>	CPU_DATA<39>
R622[1] 10K 5% 1/16W MF 402	R619[1] 10K 5% 1/16W MF 402	R618[1] 10K 5% 1/16W MF 402	R653[1] 10K 5% 1/16W MF 402	R621[1] 10K 5% 1/16W MF 402	R620[1] 10K 5% 1/16W MF 402	R652[1] 10K 5% 1/16W MF 402	R650[1] 10K 5% 1/16W MF 402
0: DDR tristate disable 1: TDI output	Analyzerclk_En_h 0: Inactive 1: Active	DDR_tri_en Pol 0: Active high 1: Active low	Bypass_PLL Pol 0: Active high 1: Active low	Spare	Spare	Spare	Spare

BIT 40 TO 47

MAXBUS_SLEEP

NO STUFF R641[1] 10K 5% 1/16W MF 402	SSCG R665[1] 10K 5% 1/16W MF 402	NO STUFF R664[1] 10K 5% 1/16W MF 402	NO_SSCG R693[1] 10K 5% 1/16W MF 402	NO STUFF R694[1] 10K 5% 1/16W MF 402	NO STUFF R699[1] 10K 5% 1/16W MF 402		
CPU_DATA<40>	CPU_DATA<41>	CPU_DATA<42>	CPU_DATA<43>	CPU_DATA<44>	CPU_DATA<45>	CPU_DATA<46>	CPU_DATA<47>
R648[1] 10K 5% 1/16W MF 402	R677[1] 10K 5% 1/16W MF 402	R623[1] 10K 5% 1/16W MF 402	NO_SSCG R651[1] 10K 5% 1/16W MF 402	R649[1] 10K 5% 1/16W MF 402	SSCG R678[1] 10K 5% 1/16W MF 402	R679[1] 10K 5% 1/16W MF 402	R684[1] 10K 5% 1/16W MF 402
Spare	Spare	BIT2	BIT1	BIT0	External Spread En 1: Active	PCI1 Source Clock 1: PLL3 (no spread)	PCI0 Source Clock 1: PLL4 (no spread)

PLL4MODESEL_NXT[2:0]
000: 166.4MHZ (2.5X)
001: 149.76MHZ
010: 133.12MHZ (2.0X)
011: 99.84MHZ (1.5X)
100: 83.20MHZ

MODE A (2.5X) IS FOR STATIC OPERATION
MODE C (2.0X) IS FOR CLOCK SLEW OPERATION

BIT 48 TO 55

MAXBUS_SLEEP

SSCG R696[1] 10K 5% 1/16W MF 402	SSCG R695[1] 10K 5% 1/16W MF 402	NO STUFF R667[1] 10K 5% 1/16W MF 402	NO STUFF R668[1] 10K 5% 1/16W MF 402	NO STUFF R643[1] 10K 5% 1/16W MF 402	NO STUFF R642[1] 10K 5% 1/16W MF 402	R698[1] 10K 5% 1/16W MF 402	
CPU_DATA<48>	CPU_DATA<49>	CPU_DATA<50>	CPU_DATA<51>	CPU_DATA<52>	CPU_DATA<53>	CPU_DATA<54>	CPU_DATA<55>
NO_SSCG R681[1] 10K 5% 1/16W MF 402	NO_SSCG R680[1] 10K 5% 1/16W MF 402	NO STUFF R654[1] 10K 5% 1/16W MF 402	R655[1] 10K 5% 1/16W MF 402	R625[1] 10K 5% 1/16W MF 402	R624[1] 10K 5% 1/16W MF 402	NO STUFF R683[1] 10K 5% 1/16W MF 402	R626[1] 10K 5% 1/16W MF 402
BUF_PREF_CLK_OUTEnable_h 0: Active 1: Inactive	PLL_ExtSrc 0: PLL5 1: External source	OBSOLETE (Should remain high) 0: BOOTROM on IDE/CardSlot 1: BOOTROM on PCI1	0: 1394b WorkAround 1: TI PHY workaround	BIT2	BIT1	BIT0	Spare

MaxBus output impedance
111: 28.6 ohm
011: 33.3 ohm
101: 40 ohm
001: 50 ohm
110: 66.6 ohm
010: 100 ohm
100: 200 ohm
000: 200 ohm

R159 4.7 5% 1/16W MF 402
+1_5V_INTREPID_PLL → +1_5V_INTREPID_PLL7
C187 0.22uF 20% 6.3V CERM 402

U51 INTREPID-REV2.1 BGA (1 OF 9) CRITCAL

CPU_BR_L	E29	BR	INPUT
CPU_BG_L	E26	BG	NO BUS KEEPER
CPU_TS_L	B27	TS	NO BUS KEEPER
CPU_ADDR<0>	D24	A_0	
CPU_ADDR<1>	D25	A_1	
CPU_ADDR<2>	A27	A_2	
CPU_ADDR<3>	E24	A_3	
CPU_ADDR<4>	G23	A_4	
CPU_ADDR<5>	B26	A_5	
CPU_ADDR<6>	A26	A_6	
CPU_ADDR<7>	D23	A_7	
CPU_ADDR<8>	A25	A_8	
CPU_ADDR<9>	E23	A_9	
CPU_ADDR<10>	J22	A_10	
CPU_ADDR<11>	B25	A_11	
CPU_ADDR<12>	H22	A_12	
CPU_ADDR<13>	G22	A_13	
CPU_ADDR<14>	D22	A_14	
CPU_ADDR<15>	B24	A_15	
CPU_ADDR<16>	B23	A_16	
CPU_ADDR<17>	E22	A_17	
CPU_ADDR<18>	J21	A_18	
CPU_ADDR<19>	G21	A_19	
CPU_ADDR<20>	E21	A_20	
CPU_ADDR<21>	A24	A_21	
CPU_ADDR<22>	D21	A_22	
CPU_ADDR<23>	A23	A_23	
CPU_ADDR<24>	H20	A_24	
CPU_ADDR<25>	B22	A_25	
CPU_ADDR<26>	H21	A_26	
CPU_ADDR<27>	A22	A_27	
CPU_ADDR<28>	E20	A_28	
CPU_ADDR<29>	B21	A_29	
CPU_ADDR<30>	D20	A_30	
CPU_ADDR<31>	A21	A_31	
CPU_CI_L	G26	CI	
CPU_GBL_L	A29	GBL	
CPU_TBST_L	A28	TBST	
CPU_TSIZ<0>	G24	TSIZ_0	
CPU_TSIZ<1>	H24	TSIZ_1	
CPU_TSIZ<2>	D26	TSIZ_2	
CPU_TT<0>	E25	TT_0	
CPU_TT<1>	G25	TT_1	
CPU_TT<2>	B28	TT_2	
CPU_TT<3>	D27	TT_3	
CPU_TT<4>	J25	TT_4	
CPU_WT_L	D28	WT	
CPU_AACK_L	B29	AACK	NO BUS KEEPER - PU
CPU_ARTRY_L	H23	ARTRY	NO BUS KEEPER - PU
CPU_HIT_L	B31	HIT	INPUT - PU
CPU_QREQ_L	A32	QREQ	INPUT - PD
CPU_QACK_L	G27	QACK	NO BUS KEEPER - ?
INT_SUSPEND_REQ_L	AK9	SUSPENDREQ	
INT_SUSPEND_ACK_L	AM8	SUSPENDACK	
		Vin = Intrepid Vcore (1.5V) Vout = MaxBus rail (1.8V)	
INT_CPUFB_IN	J24	CPU_FB_IN	
INT_CPUFB_OUT	H16	CPU_FB_OUT	NO BUS KEEPER - PU
SYSCLK_LA_TP	G8	ANALYZER_CLK	INPUT - PU
CPU_CLK_EN	AH9	STOPCPUCLK	NO BUS KEEPER - ?
INTREPID_ACS_REF	H13	ACS_REF	NO BUS KEEPER - ?
			NO BUS KEEPER - ?
SYSCLK_CPU	J15	CPU_CLK	NO BUS KEEPER - PU
			NO BUS KEEPER - PU
CPU_TBEN	A31	TBEN	NO BUS KEEPER - PU
		INTREPID OUTPUTS HIGH BY DEFAULT	

VDD15A_7 (PLL6) H26
VSSA_7 (PLL6) H25

MAXBUS INTERFACE

D_0	D10	CPU_DATA<0>	6 36
D_1	G12	CPU_DATA<1>	6 36
D_2	E11	CPU_DATA<2>	6 36
D_3	H11	CPU_DATA<3>	6 36
D_4	B9	CPU_DATA<4>	6 36
D_5	B8	CPU_DATA<5>	6 36
D_6	A9	CPU_DATA<6>	6 36
D_7	A8	CPU_DATA<7>	6 36
D_8	E12	CPU_DATA<8>	6 36
D_9	D11	CPU_DATA<9>	6 36
D_10	B10	CPU_DATA<10>	6 36
D_11	J13	CPU_DATA<11>	6 36
D_12	A10	CPU_DATA<12>	6 36
D_13	D12	CPU_DATA<13>	6 36
D_14	E13	CPU_DATA<14>	6 36
D_15	G13	CPU_DATA<15>	6 36
D_16	B11	CPU_DATA<16>	6 36
D_17	D13	CPU_DATA<17>	6 36
D_18	A11	CPU_DATA<18>	6 36
D_19	G14	CPU_DATA<19>	6 36
D_20	H14	CPU_DATA<20>	6 36
D_21	E14	CPU_DATA<21>	6 36
D_22	B12	CPU_DATA<22>	6 36
D_23	G15	CPU_DATA<23>	6 36
D_24	B13	CPU_DATA<24>	6 36
D_25	H15	CPU_DATA<25>	6 36
D_26	D14	CPU_DATA<26>	6 36
D_27	B14	CPU_DATA<27>	6 36
D_28	A12	CPU_DATA<28>	6 36
D_29	G16	CPU_DATA<29>	6 36
D_30	E15	CPU_DATA<30>	6 36
D_31	J16	CPU_DATA<31>	6 36
D_32	D15	CPU_DATA<32>	6 8 36
D_33	A14	CPU_DATA<33>	6 8 36
D_34	A13	CPU_DATA<34>	6 8 36
D_35	D16	CPU_DATA<35>	6 8 36
D_36	E16	CPU_DATA<36>	6 8 36
D_37	G17	CPU_DATA<37>	6 8 36
D_38	B15	CPU_DATA<38>	6 8 36
D_39	H17	CPU_DATA<39>	6 8 36
D_40	A15	CPU_DATA<40>	6 8 36
D_41	B16	CPU_DATA<41>	6 8 36
D_42	E17	CPU_DATA<42>	6 8 36
D_43	A16	CPU_DATA<43>	6 8 36
D_44	J18	CPU_DATA<44>	6 8 36
D_45	H18	CPU_DATA<45>	6 8 36
D_46	D17	CPU_DATA<46>	6 8 36
D_47	G18	CPU_DATA<47>	6 8 36
D_48	A17	CPU_DATA<48>	6 8 36
D_49	B17	CPU_DATA<49>	6 8 36
D_50	E18	CPU_DATA<50>	6 8 36
D_51	B18	CPU_DATA<51>	6 8 36
D_52	D18	CPU_DATA<52>	6 8 36
D_53	A18	CPU_DATA<53>	6 8 36
D_54	A19	CPU_DATA<54>	6 8 36
D_55	H19	CPU_DATA<55>	6 8 36
D_56	B19	CPU_DATA<56>	6 8 36
D_57	J19	CPU_DATA<57>	6 8 36
D_58	A20	CPU_DATA<58>	6 8 36
D_59	D19	CPU_DATA<59>	6 8 36
D_60	E19	CPU_DATA<60>	6 8 36
D_61	G19	CPU_DATA<61>	6 8 36
D_62	B20	CPU_DATA<62>	6 8 36
D_63	G20	CPU_DATA<63>	6 8 36
DBG	A30	CPU_DBG_L	5 8 36
DRDY	G28	CPU_DRDY_L	5 8 36
DTI_0	K25	CPU_DTI<0>	5 36
DTI_1	D29	CPU_DTI<1>	5 36
DTI_2	B30	CPU_DTI<2>	5 36
TA	E27	CPU_TA_L	5 8 36
TEA	E28	CPU_TEA_L	5 8 36

FB BUFFER HAS 50 OHM OUTPUT IMPEDANCE

R169 511 1% 1/16W MF 402
R168 0 5% 1/16W MF 402
R161 1K 1% 1/16W MF 402

SHORT = 1" SHORTER THAN MATCHED LENGTH
LONG = 1" LONGER THAN MATCHED LENGTH

R155 0 5% 1/16W MF 402	INT_CPUFB_OUT	INT_CPUFB_OUT_SHORT		
R140 0 5% 1/16W MF 402	INT_CPUFB_OUT_SHORT	INT_CPUFB_OUT_NORM		
NO STUFF R128 0 5% 1/16W MF 402	INT_CPUFB_OUT_NORM	INT_CPUFB_LONG		
NO STUFF R146[1] 0 5% 1/16W MF 402	INT_CPUFB_IN			
R147 0 5% 1/16W MF 402	INT_CPUFB_IN	INT_CPUFB_IN_NORM		
R141[1] 0 5% 1/16W MF 402	INT_CPUFB_IN_NORM			
NO STUFF R136 0 5% 1/16W MF 402	INT_CPUFB_IN_NORM			

THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:
1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
2/ D46 - SELPCI1SPREADCLK - SLEEP/WAKE CYCLE REQUIRED
3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT

IF A STRAP IS NOT LISTED, THEN
IT CANNOT BE CHANGED BY SOFTWARE

MAXBUS PULL-UPS

MAXBUS_SLEEP

RP3 10K 5% 1/16W SM1		RP3 10K 5% 1/16W SM1		RP2 10K 5% 1/16W SM1		R152 10K 5% 1/16W MF 402	RP2 10K 5% 1/16W SM1
CPU_TS_L		CPU_TA_L		CPU_ARTRY_L		CPU_BR_L	CPU_HIT_L
RP2 10K 5% 1/16W SM1		RP2 10K 5% 1/16W SM1		R150 10K 5% 1/16W MF 402	RP3 10K 5% 1/16W SM1	R151 10K 5% 1/16W MF 402	
CPU_DRDY_L		CPU_TEA_L		CPU_AACK_L		CPU_DBG_L	CPU_BG_L	CPU_QREQ_L

INTREPID BOOT STRAPS

MAXBUS_SLEEP

BIT 56 TO 63

NO STUFF R669[1] 10K 5% 1/16W MF 402	NO STUFF R645[1] 10K 5% 1/16W MF 402	NO STUFF R697[1] 10K 5% 1/16W MF 402	NO STUFF R670[1] 10K 5% 1/16W MF 402	R644[1] 10K 5% 1/16W MF 402	NO STUFF R646[1] 10K 5% 1/16W MF 402		
CPU_DATA<56>	CPU_DATA<57>	CPU_DATA<58>	CPU_DATA<59>	CPU_DATA<60>	CPU_DATA<61>	CPU_DATA<62>	CPU_DATA<63>
R656[1] 10K 5% 1/16W MF 402	R685[1] 10K 5% 1/16W MF 402	R657[1] 10K 5% 1/16W MF 402	R628[1] 10K 5% 1/16W MF 402	R682[1] 10K 5% 1/16W MF 402	R658[1] 10K 5% 1/16W MF 402	NO STUFF R627[1] 10K 5% 1/16W MF 402	R629[1] 10K 5% 1/16W MF 402
Spare	Spare	OBSOLETE (Should remain high) ROM Overlay Reg 0: 1 MB IDE 1: 0-1 MB IDE 2 2:3 PCI1	PCI1_REQ2_L / PCI1_GNT2_L 0: REQ/GNT 1: GPIOs	PCI1_REQ1_L / PCI1_GNT1_L 0: REQ/GNT 1: GPIOs	PCI1_REQ0_L / PCI1_GNT0_L 0: REQ/GNT 1: GPIOs	Firewire PHY interface 0: B-Mode interface	Processor Bus Mode 0: 60x Bus (G3) 1: 60x Bus (G4)

Intrepid MaxBus

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401243	AA
SCALE: NONE	SHT 8 OF 44	

SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

PINS ARE SWAPABLE FOR RPAKS

U51
INTREPID-REV2.1
BGA
(2 OF 9)
CRITICAL

DDR MEMORY INTERFACE

DDR_DATA_0	AK32	MEM_DATA<0>	9 10 35
DDR_DATA_1	AK33	MEM_DATA<1>	9 10 35
DDR_DATA_2	AK31	MEM_DATA<2>	9 10 35
DDR_DATA_3	AK35	MEM_DATA<3>	9 10 35
DDR_DATA_4	AK36	MEM_DATA<4>	9 10 35
DDR_DATA_5	AJ32	MEM_DATA<5>	9 10 35
DDR_DATA_6	AJ35	MEM_DATA<6>	9 10 35
DDR_DATA_7	AJ36	MEM_DATA<7>	9 10 35
DDR_DATA_8	AG33	MEM_DATA<8>	9 10 35
DDR_DATA_9	AG35	MEM_DATA<9>	9 10 35
DDR_DATA_10	AH35	MEM_DATA<10>	9 10 35
DDR_DATA_11	AG36	MEM_DATA<11>	9 10 35
DDR_DATA_12	AH36	MEM_DATA<12>	9 10 35
DDR_DATA_13	AH32	MEM_DATA<13>	9 10 35
DDR_DATA_14	AG32	MEM_DATA<14>	9 10 35
DDR_DATA_15	AG31	MEM_DATA<15>	9 10 35
DDR_DATA_16	AE32	MEM_DATA<16>	9 10 35
DDR_DATA_17	AF35	MEM_DATA<17>	9 10 35
DDR_DATA_18	AF36	MEM_DATA<18>	9 10 35
DDR_DATA_19	AE36	MEM_DATA<19>	9 10 35
DDR_DATA_20	AE35	MEM_DATA<20>	9 10 35
DDR_DATA_21	AE33	MEM_DATA<21>	9 10 35
DDR_DATA_22	AD36	MEM_DATA<22>	9 10 35
DDR_DATA_23	AD35	MEM_DATA<23>	9 10 35
DDR_DATA_24	AA36	MEM_DATA<24>	9 10 35
DDR_DATA_25	AA35	MEM_DATA<25>	9 10 35
DDR_DATA_26	AA33	MEM_DATA<26>	9 10 35
DDR_DATA_27	AB36	MEM_DATA<27>	9 10 35
DDR_DATA_28	AB35	MEM_DATA<28>	9 10 35
DDR_DATA_29	AC36	MEM_DATA<29>	9 10 35
DDR_DATA_30	AA32	MEM_DATA<30>	9 10 35
DDR_DATA_31	AB33	MEM_DATA<31>	9 10 35
DDR_DATA_32	V36	MEM_DATA<32>	9 10 35
DDR_DATA_33	U33	MEM_DATA<33>	9 10 35
DDR_DATA_34	U32	MEM_DATA<34>	9 10 35
DDR_DATA_35	V35	MEM_DATA<35>	9 10 35
DDR_DATA_36	T36	MEM_DATA<36>	9 10 35
DDR_DATA_37	U36	MEM_DATA<37>	9 10 35
DDR_DATA_38	U35	MEM_DATA<38>	9 10 35
DDR_DATA_39	T35	MEM_DATA<39>	9 10 35
DDR_DATA_40	P33	MEM_DATA<40>	9 10 35
DDR_DATA_41	R36	MEM_DATA<41>	9 10 35
DDR_DATA_42	P35	MEM_DATA<42>	9 10 35
DDR_DATA_43	P36	MEM_DATA<43>	9 10 35
DDR_DATA_44	R36	MEM_DATA<44>	9 10 35
DDR_DATA_45	R35	MEM_DATA<45>	9 10 35
DDR_DATA_46	R33	MEM_DATA<46>	9 10 35
DDR_DATA_47	R32	MEM_DATA<47>	9 10 35
DDR_DATA_48	N35	MEM_DATA<48>	9 10 35
DDR_DATA_49	M36	MEM_DATA<49>	9 10 35
DDR_DATA_50	L35	MEM_DATA<50>	9 10 35
DDR_DATA_51	M35	MEM_DATA<51>	9 10 35
DDR_DATA_52	M33	MEM_DATA<52>	9 10 35
DDR_DATA_53	L36	MEM_DATA<53>	9 10 35
DDR_DATA_54	N33	MEM_DATA<54>	9 10 35
DDR_DATA_55	M36	MEM_DATA<55>	9 10 35
DDR_DATA_56	J32	MEM_DATA<56>	9 10 35
DDR_DATA_57	J33	MEM_DATA<57>	9 10 35
DDR_DATA_58	J35	MEM_DATA<58>	9 10 35
DDR_DATA_59	K32	MEM_DATA<59>	9 10 35
DDR_DATA_60	K33	MEM_DATA<60>	9 10 35
DDR_DATA_61	J36	MEM_DATA<61>	9 10 35
DDR_DATA_62	K36	MEM_DATA<62>	9 10 35
DDR_DATA_63	K35	MEM_DATA<63>	9 10 35

DDR_A_0	H35	MEM_ADDR<0>	9 35
DDR_A_1	G35	MEM_ADDR<1>	9 35
DDR_A_2	G36	MEM_ADDR<2>	9 35
DDR_A_3	F36	MEM_ADDR<3>	9 35
DDR_A_4	F35	MEM_ADDR<4>	9 35
DDR_A_5	E35	MEM_ADDR<5>	9 35
DDR_A_6	E36	MEM_ADDR<6>	9 35
DDR_A_7	G32	MEM_ADDR<7>	9 35
DDR_A_8	D36	MEM_ADDR<8>	9 35
DDR_A_9	H36	MEM_ADDR<9>	9 35
DDR_A_10	G33	MEM_ADDR<10>	9 35
DDR_A_11	H33	MEM_ADDR<11>	9 35
DDR_A_12	D35	MEM_ADDR<12>	9 35
DDR_BA_0	L30	MEM_BA<0>	9 35
DDR_BA_1	M29	MEM_BA<1>	9 35
DDRCS_0	AN34	MEM_CS_L<0>	9 35
DDRCS_1	AN36	MEM_CS_L<1>	9 35
DDRCS_2	AL35	MEM_CS_L<2>	9 35
DDRCS_3	AL33	MEM_CS_L<3>	9 35
DDR_DQS_0	AJ31	MEM_DQS<0>	10 35
DDR_DQS_1	AH31	MEM_DQS<1>	10 35
DDR_DQS_2	AD32	MEM_DQS<2>	10 35
DDR_DQS_3	AB30	MEM_DQS<3>	10 35
DDR_DQS_4	V30	MEM_DQS<4>	10 35
DDR_DQS_5	P32	MEM_DQS<5>	10 35
DDR_DQS_6	N29	MEM_DQS<6>	10 35
DDR_DQS_7	L32	MEM_DQS<7>	10 35
DDR_DM_0	AJ33	MEM_DQM<0>	10 35
DDR_DM_1	AH33	MEM_DQM<1>	10 35
DDR_DM_2	AD33	MEM_DQM<2>	10 35
DDR_DM_3	AC35	MEM_DQM<3>	10 35
DDR_DM_4	T35	MEM_DQM<4>	10 35
DDR_DM_5	T33	MEM_DQM<5>	10 35
DDR_DM_6	N32	MEM_DQM<6>	10 35
DDR_DM_7	L33	MEM_DQM<7>	10 35
DDRRAS	L29	MEM_RAS_L	9 35
DDRCAS	H32	MEM_CAS_L	9 35
DDRWE	K30	MEM_WE_L	9 35
DDRCKE0	AN35	MEM_CKE<0>	9 35
DDRCKE1	AM35	MEM_CKE<1>	9 35
DDRCKE2	AM36	MEM_CKE<2>	9 35
DDRCKE3	AL36	MEM_CKE<3>	9 35
DDR_SELHI_0	AB32	MEM_MUXSEL_MSB_L_TP	
DDR_SELHI_1	AE29	MEM_MUXSEL_MSB	10 35
DDR_SELLO_0	N30	MEM_MUXSEL_LSB_L_TP	
DDR_SELLO_1	T32	MEM_MUXSEL_LSB	10 35
DDR_MCLK_0_P	Y32	SYSCLK_DDRCLK_A0_UF	9 35
DDR_MCLK_0_N	Y33	SYSCLK_DDRCLK_A0_L_UF	9 35
DDR_MCLK_1_P	Y35	SYSCLK_DDRCLK_A1_UF	9 35
DDR_MCLK_1_N	Y36	SYSCLK_DDRCLK_A1_L_UF	9 35
DDR_MCLK_2_P	Y30	INT_DDRCLK2_P_TP	
DDR_MCLK_2_N	W30	INT_DDRCLK2_N_TP	
DDR_MCLK_3_P	W32	SYSCLK_DDRCLK_B0_UF	9 35
DDR_MCLK_3_N	W33	SYSCLK_DDRCLK_B0_L_UF	9 35
DDR_MCLK_4_P	V33	SYSCLK_DDRCLK_B1_UF	9 35
DDR_MCLK_4_N	V32	SYSCLK_DDRCLK_B1_L_UF	9 35
DDR_MCLK_5_P	W35	INT_DDRCLK5_P_TP	
DDR_MCLK_5_N	W36	INT_DDRCLK5_N_TP	
DDR_REF	AA22	INT_MEM_REF_H	38
DDR_VREF_0	Y22	INT_MEM_VREF	9 38
DDR_VREF_1	T22		

'0' & '1' GO TO SLOT A
'2' & '3' GO TO SLOT B

'0' & '1' GO TO SLOT A
'2' & '3' GO TO SLOT B

'0'S ARE SAME POLARITY (ACTIVE-LO)
'1'S ARE SAME POLARITY (ACTIVE-HI)

R209 1K 1% 1/16W MF 402

MEM_VREF

+2_5V_INTREPID

R208 10K 1% 1/16W MF 402

R202 10K 1% 1/16W MF 402

C249 0.1uF 20% 10V CERM 402

INT_MEM_VREF

CLOCKS

SYSCLK_DDRCLK_A1_UF	RP20	4	5	SYSCLK_DDRCLK_A1	11 35
SYSCLK_DDRCLK_A1_L_UF	RP20	3	6	SYSCLK_DDRCLK_A1_L	11 35
SYSCLK_DDRCLK_A0_UF	RP22	1	8	SYSCLK_DDRCLK_A0	11 35
SYSCLK_DDRCLK_A0_L_UF	RP22	2	7	SYSCLK_DDRCLK_A0_L	11 35
SYSCLK_DDRCLK_B1_UF	RP20	2	7	SYSCLK_DDRCLK_B1	11 35
SYSCLK_DDRCLK_B1_L_UF	RP20	1	8	SYSCLK_DDRCLK_B1_L	11 35
SYSCLK_DDRCLK_B0_UF	RP22	3	6	SYSCLK_DDRCLK_B0	11 35
SYSCLK_DDRCLK_B0_L_UF	RP22	4	5	SYSCLK_DDRCLK_B0_L	11 35

CS

MEM_CS_L<0>	RP31	3	6	RAM_CS_L<0>	11 35
MEM_CS_L<1>	RP31	2	7	RAM_CS_L<1>	11 35
MEM_CS_L<2>	RP29	3	6	RAM_CS_L<2>	11 35
MEM_CS_L<3>	RP29	4	5	RAM_CS_L<3>	11 35

CKE

MEM_CKE<0>	RP31	1	8	RAM_CKE<0>	9 11 35
MEM_CKE<1>	RP31	4	5	RAM_CKE<1>	9 11 35
MEM_CKE<2>	RP29	1	8	RAM_CKE<2>	9 11 35
MEM_CKE<3>	RP29	2	7	RAM_CKE<3>	9 11 35

ADDR

MEM_ADDR<0>	RP14	3	6	RAM_ADDR<0>	11 35
MEM_ADDR<1>	RP12	2	7	RAM_ADDR<1>	11 35
MEM_ADDR<2>	RP12	1	8	RAM_ADDR<2>	11 35
MEM_ADDR<3>	RP12	4	5	RAM_ADDR<3>	11 35
MEM_ADDR<4>	RP9	3	6	RAM_ADDR<4>	11 35
MEM_ADDR<5>	RP9	2	7	RAM_ADDR<5>	11 35
MEM_ADDR<6>	RP14	1	8	RAM_ADDR<6>	11 35
MEM_ADDR<7>	RP14	2	7	RAM_ADDR<7>	11 35
MEM_ADDR<8>	RP9	4	5	RAM_ADDR<8>	11 35
MEM_ADDR<9>	RP14	4	5	RAM_ADDR<9>	11 35
MEM_ADDR<10>	RP14	1	8	RAM_ADDR<10>	11 35
MEM_ADDR<11>	RP17	4	5	RAM_ADDR<11>	11 35
MEM_ADDR<12>	RP9	3	6	RAM_ADDR<12>	11 35

BA

MEM_BA<0>	RP17	2	7	RAM_BA<0>	11 35
MEM_BA<1>	RP17	1	8	RAM_BA<1>	11 35

CNTL

MEM_WE_L	RP17	3	6	RAM_WE_L	11 35
MEM_CAS_L	R162	1	2	RAM_CAS_L	11 35
MEM_RAS_L	R176	1	2	RAM_RAS_L	11 35

1MB BOOT ROM

+3V_MAIN

C125 2.2uF 20% 10V CERM 805

C773 0.1uF 20% 10V CERM 402

C122 0.1uF 20% 10V CERM 402

U11
FEPR-1MX8
1MX8-3.3V
TSOP

VPP = 11, VCC = 30, 31

A0	21	PCI_AD<0>	39 37 24 18 17 12
A1	20	PCI_AD<1>	39 37 24 18 17 12
A2	19	PCI_AD<2>	39 37 24 18 17 12
A3	18	PCI_AD<3>	39 37 24 18 17 12
A4	17	PCI_AD<4>	39 37 24 18 17 12
A5	16	PCI_AD<5>	39 37 24 18 17 12
A6	15	PCI_AD<6>	39 37 24 18 17 12
A7	14	PCI_AD<7>	39 37 24 18 17 12
A8	8	PCI_AD<8>	39 37 24 18 17 12
A9	7	PCI_AD<9>	39 37 24 18 17 12
A10	36	PCI_AD<10>	39 37 24 18 17 12
A11	6	PCI_AD<11>	39 37 24 18 17 12
A12	5	PCI_AD<12>	39 37 24 18 17 12
A13	4	PCI_AD<13>	39 37 24 18 17 12
A14	3	PCI_AD<14>	37 24 18 17 12
A15	2	PCI_AD<15>	37 24 18 17 12
A16	1	PCI_AD<16>	37 24 18 17 12
A17	40	PCI_AD<17>	37 24 18 17 12
A18	13	PCI_AD<18>	37 24 18 17 12
A19	37	PCI_AD<19>	37 24 18 17 12
A20	38	PCI_AD<20>	37 24 18 17 12

DQ0	25	PCI_AD<24>	12 17 18 24 37 39
DQ1	26	PCI_AD<25>	12 17 18 24 37 39
DQ2	27	PCI_AD<26>	12 17 18 24 37 39
DQ3	28	PCI_AD<27>	12 17 18 24 37 39
DQ4	32	PCI_AD<28>	12 17 18 24 37 39
DQ5	33	PCI_AD<29>	12 17 18 24 37 39
DQ6	34	PCI_AD<30>	12 17 18 24 37 39
DQ7	35	PCI_AD<31>	12 17 18 24 37 39

+3V_MAIN

R691 10K 5% 1/16W MF 402

R112 10K 5% 1/16W MF 402

R674 1K 5% 1/16W MF 402

ROM_CS_L (39 24 12)

CE	22	ROM_ONBOARD_CS_L	39 24
OE	24	ROM_OE_L	39 24 12
WE	9	ROM_RW_L	39 24 12
WP	12	ROM_WP_L	
PWD	10	INT_RESET_L	29 13
GND	23, 39		

OVERRIDE ROM MODULE
INTERCEPTS ROM CHIP SELECT

Weak pulldowns ensure CKEs stay low
after 2.5V I/O to Intrepid shuts off.

RAM_CKE<0>	R247 10K 5% 1/16W MF 402	INT_2_5V_COLD
RAM_CKE<1>	R257 10K 5% 1/16W MF 402	INT_2_5V_COLD
RAM_CKE<2>	R260 10K 5% 1/16W MF 402	INT_2_5V_COLD
RAM_CKE<3>	R265 10K 5% 1/16W MF 402	INT_2_5V_COLD

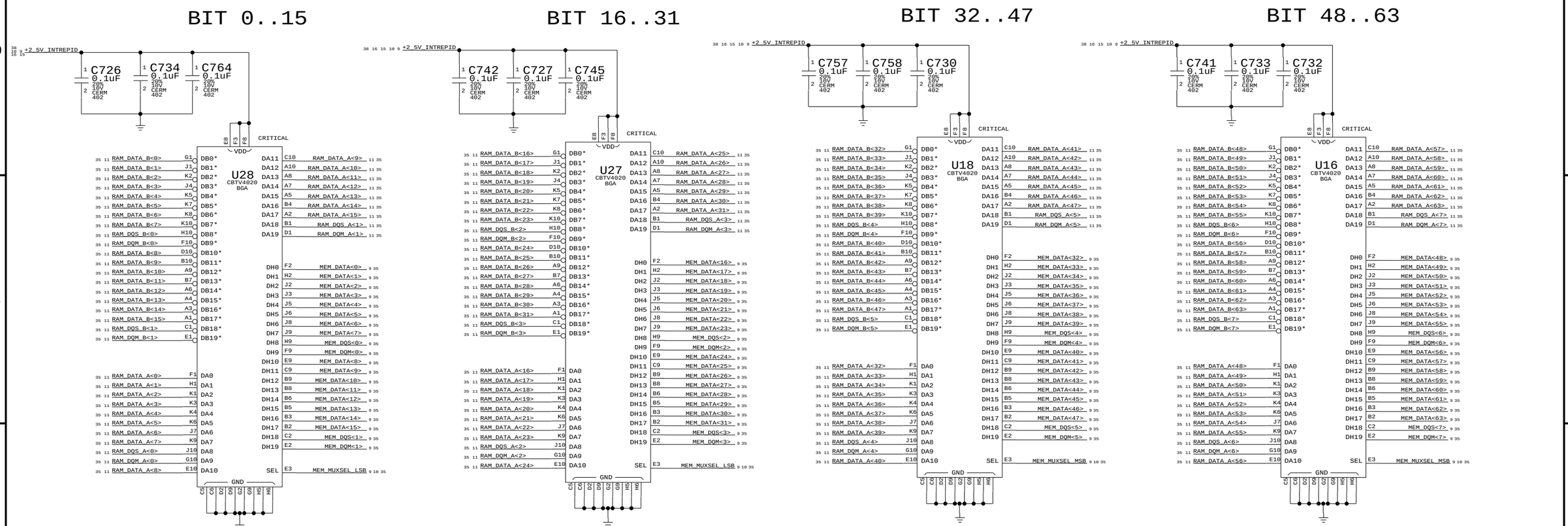
INT - DDR/BOOTROM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401243	AA

SCALE: NONE

SHT 9 OF 44



16BIT 2:1 DDR MUXES	
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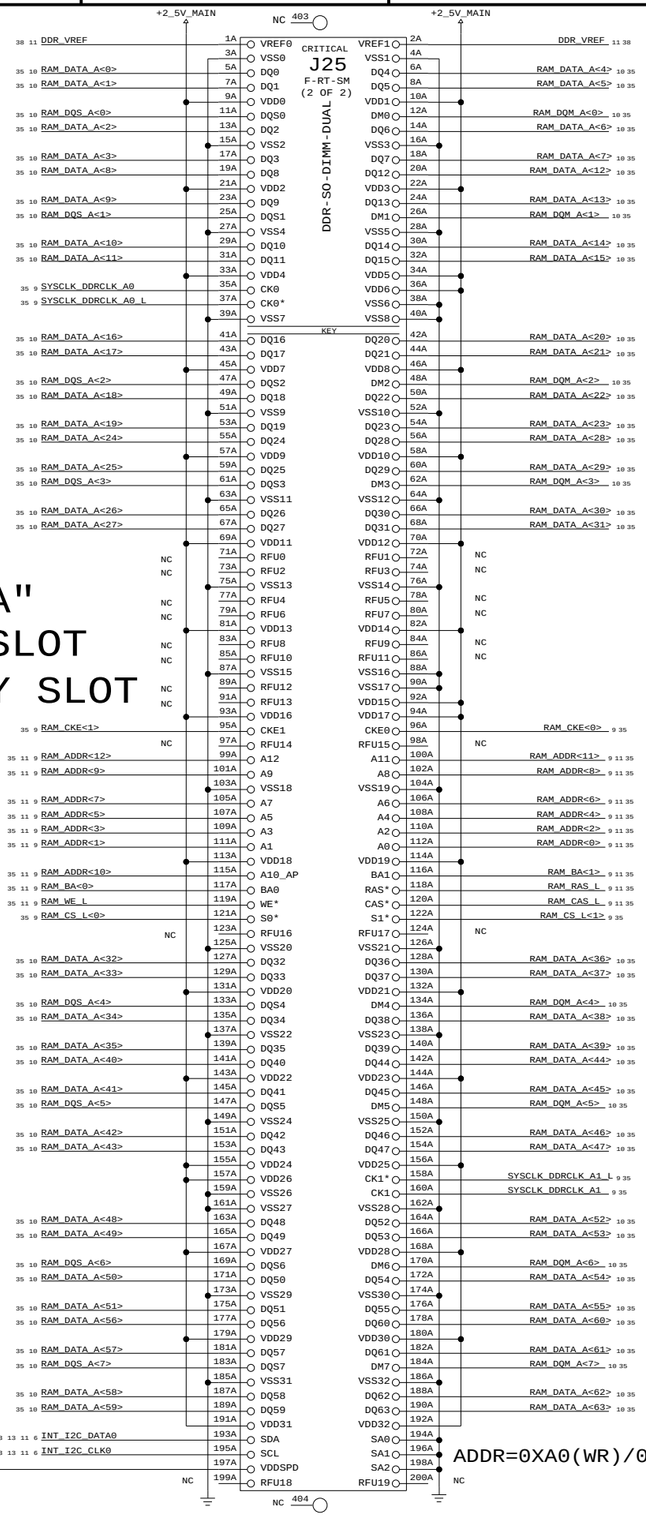
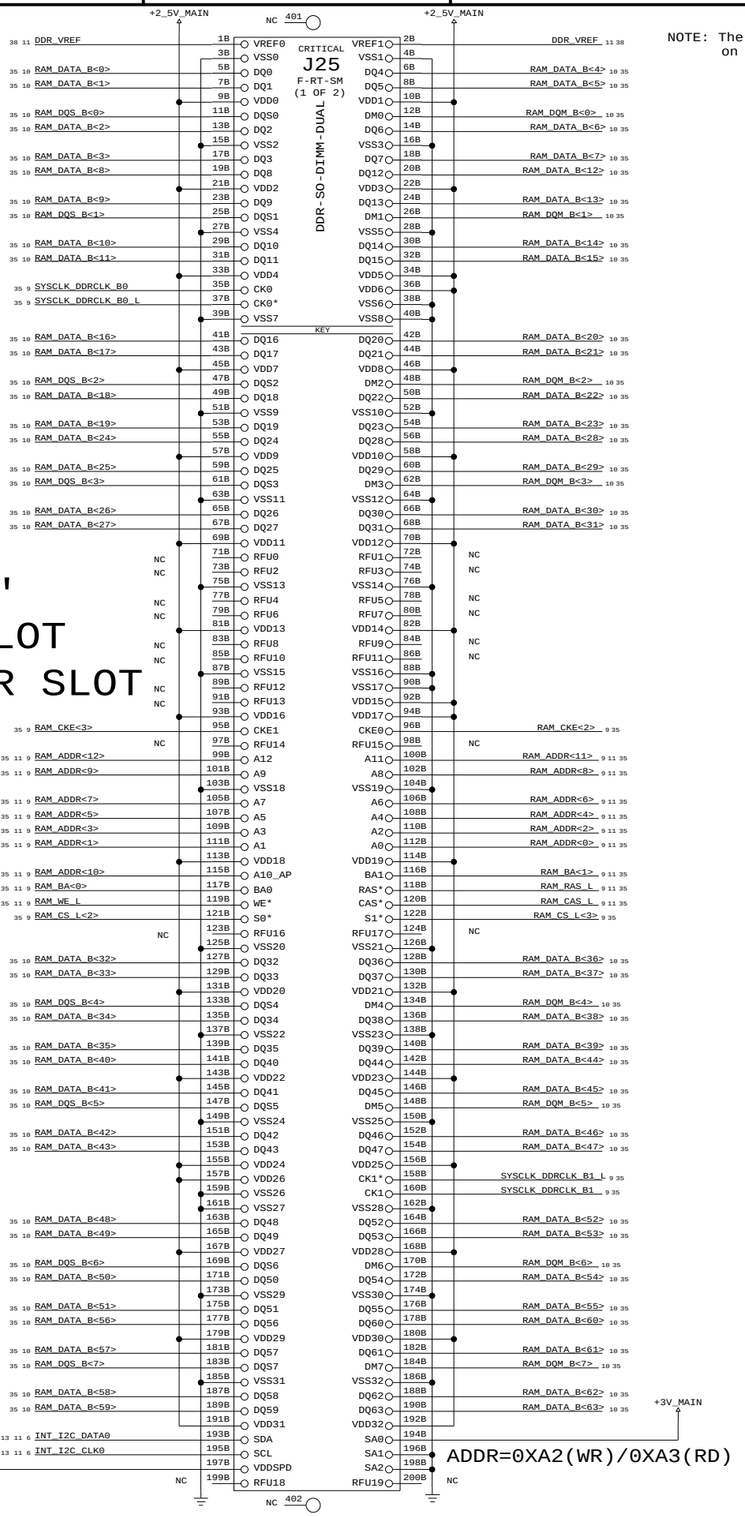
APPLE COMPUTER INC.	SIZE D · DRAWING NUMBER 401243 · REV. AA
	SCALE NONE · SHT 10 OF 44

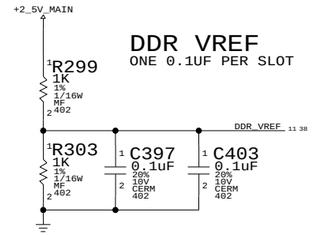


SLOT "A"
LOWER SLOT
FACTORY SLOT



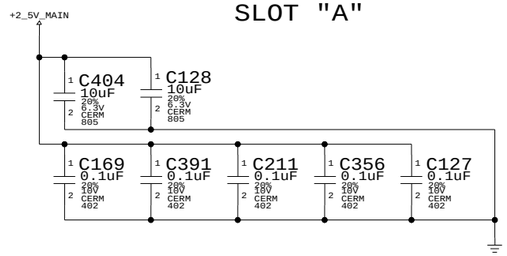
SLOT "B"
UPPER SLOT
CUSTOMER SLOT

NOTE: The SODIMM connector footprint has a through-hole slot on the PCB for additional mounting

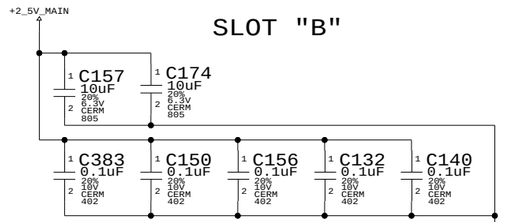


DDR VREF
ONE 0.1UF PER SLOT

DDR BYPASS
SLOT "A"



SLOT "B"



DDR SODIMM CONNS

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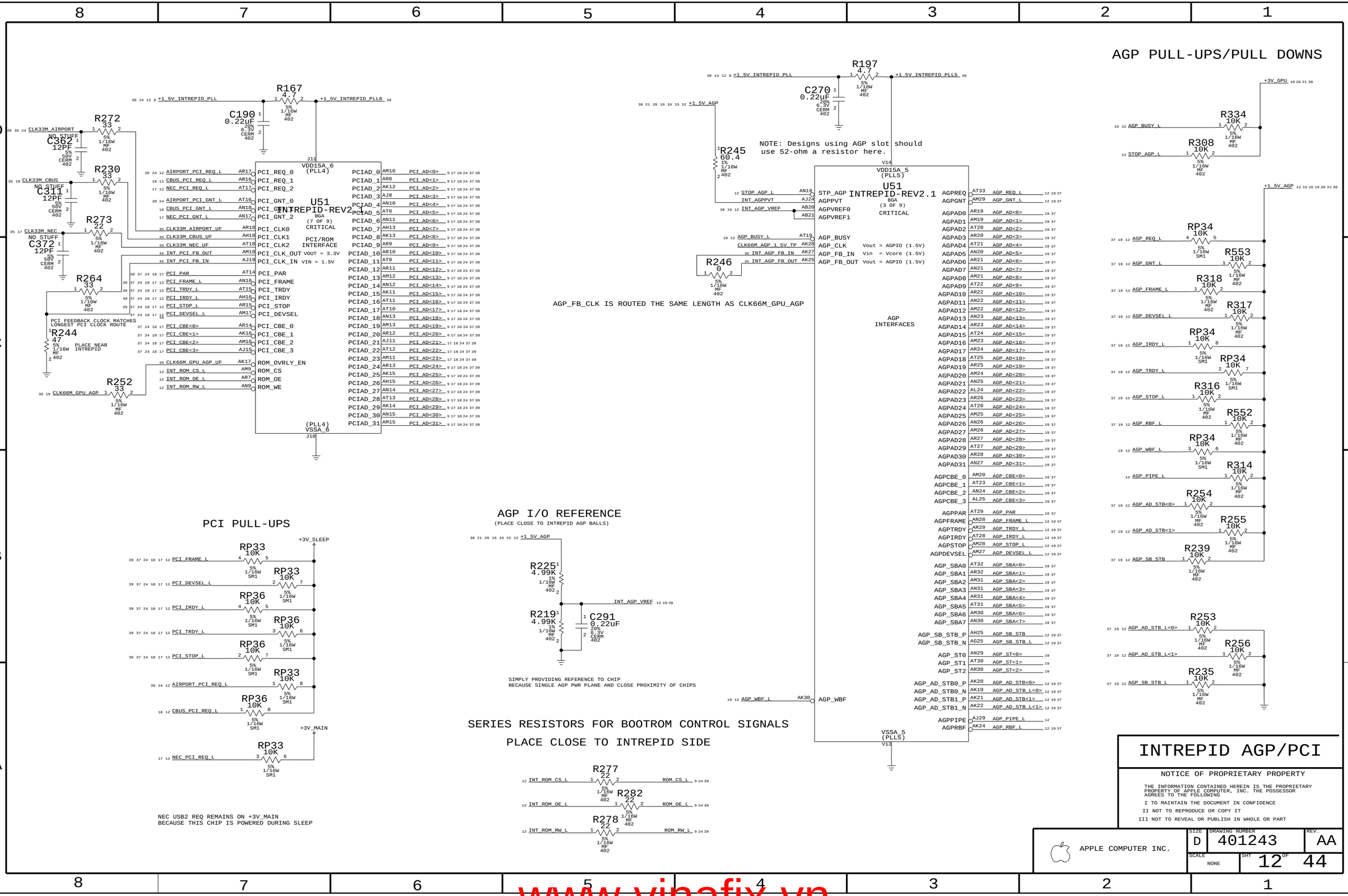
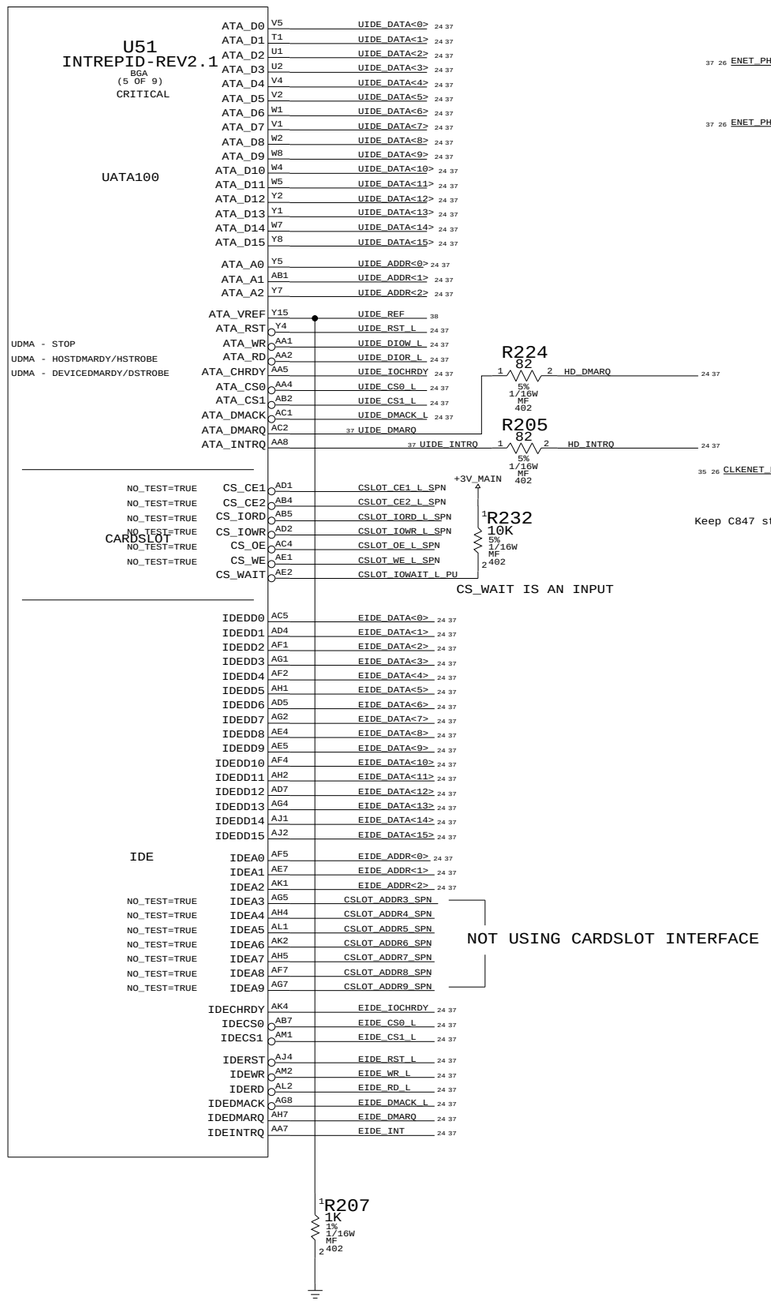
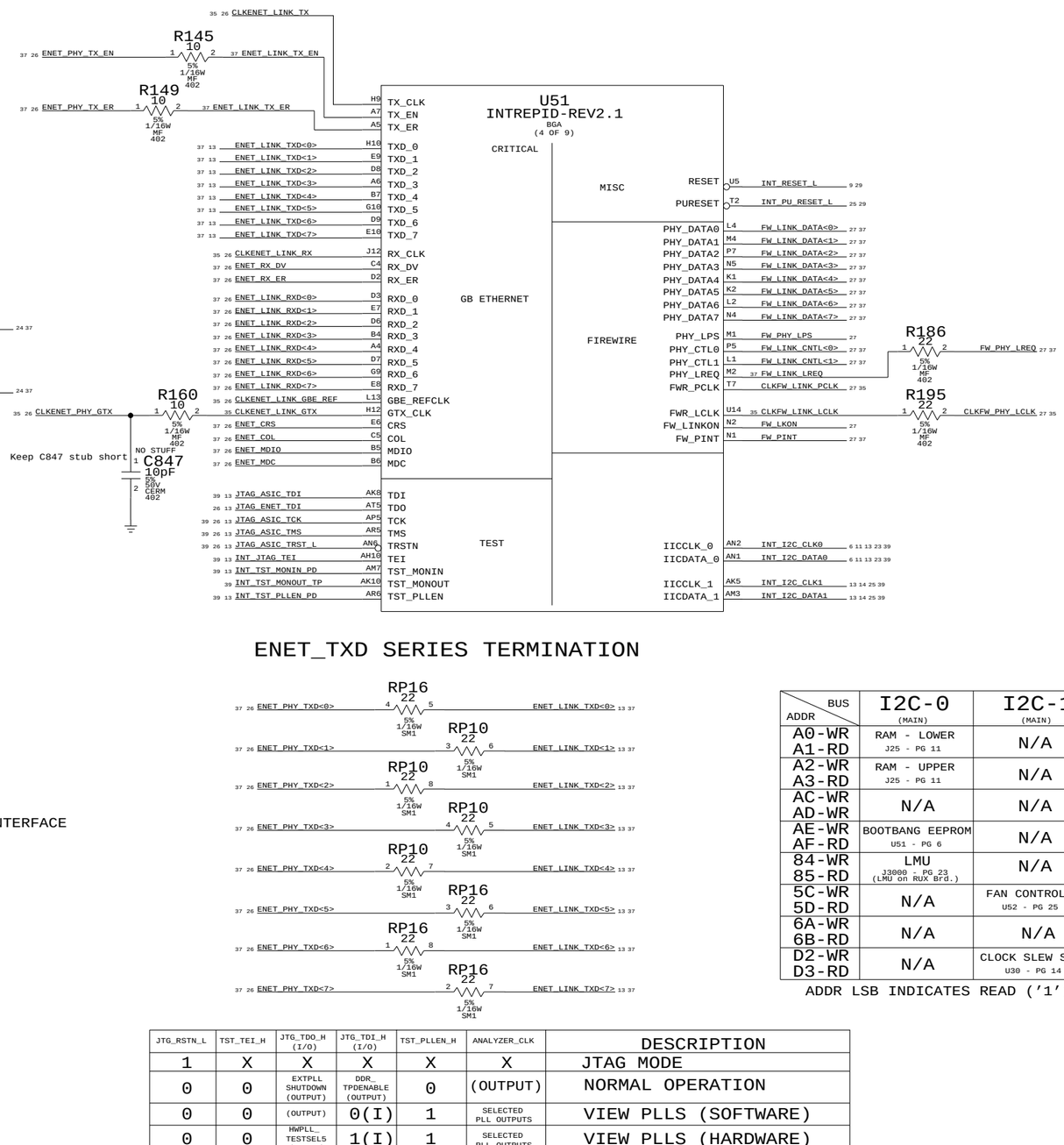
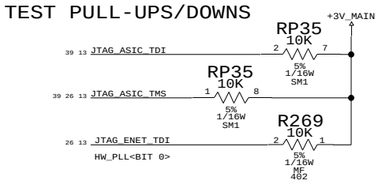
APPLE COMPUTER INC.

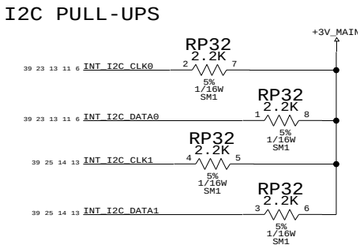
SIZE	DRAWING NUMBER	REV.
D	401243	AA
SCALE: NONE	SHT 11 OF 44	











ENET_TXD SERIES TERMINATION

BUS / ADDR	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
A0-WR A1-RD	RAM - LOWER J25 - PG 11	N/A	N/A	N/A
A2-WR A3-RD	RAM - UPPER J25 - PG 11	N/A	N/A	N/A
AC-WR AD-WR	N/A	N/A	DASH MODEM J14 - PG 25	N/A
AE-WR AF-RD	BOOTBANG EEPROM U51 - PG 6	N/A	N/A	N/A
84-WR 85-RD	LMU J3000 - PG 23 (LMU on RUX Brd.)	N/A	N/A	N/A
5C-WR 5D-RD	N/A	FAN CONTROLLER U52 - PG 25	N/A	N/A
6A-WR 6B-RD	N/A	N/A	SNAPPER SOUND J2 - PG 25	N/A
D2-WR D3-RD	N/A	CLOCK SLEW SSCG U30 - PG 14	N/A	N/A

ADDR LSB INDICATES READ ('1') OR WRITE ('0') MODES

JTG_RSTN_L	TST_TEI_H	JTG_TDO_H (I/O)	JTG_TDI_H (I/O)	TST_PLLEN_H	ANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	EXTPLL SHUTDOWN (OUTPUT)	DDR_ TPDENABLE (OUTPUT)	0	(OUTPUT)	NORMAL OPERATION
0	0	(OUTPUT)	0(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	HWPLL_ TESTSEL5 (INPUT)	1(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0(I)	0(I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0(I)	1(I)	0	X(I)	ATPG IDDQ
0	1	0(I)	1(I)	1	X(I)	TEST TRI-STATE
0	1	1(I)	0(I)	0	X(I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1(I)	0(I)	1	X(I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1(I)	1(I)	X	X(I)	FUNCTIONAL TEST IDDQ

INT - ENET/FW/UATA EIDE/I2C

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 401243 | REV. AA

SCALE NONE | SHT 13 OF 44

USB PORT ASSIGNMENTS

PORT A - PORT D/UNUSED

R181 10K 5% 1/16W MF 402 — 14 USB_DAM
R183 10K 5% 1/16W MF 402 — 14 USB_DAP
R156 10K 5% 1/16W MF 402 — 14 USB_DBM
R157 10K 5% 1/16W MF 402 — 14 USB_DBP
R164 10K 5% 1/16W MF 402 — 14 USB_DCM
R165 10K 5% 1/16W MF 402 — 14 USB_DCP
R182 10K 5% 1/16W MF 402 — 14 USB_DDM
R180 10K 5% 1/16W MF 402 — 14 USB_DDP

PORT E/BLUETOOTH

37 14 USB_DEP — R174 22 5% 1/16W MF 402 — BT_USB_DP 25 37 39
37 14 USB_DEM — R179 22 5% 1/16W MF 402 — BT_USB_DM 25 37 39
R178[1] 15K 5% 1/16W MF 402
R175[1] 15K 5% 1/16W MF 402

PORT F/MODEM

37 14 USB_DFP — R192 22 5% 1/16W MF 402 — MODEM_USB_DP 25 37 39
37 14 USB_DFM — R188 22 5% 1/16W MF 402 — MODEM_USB_DM 25 37 39
R189[1] 15K 5% 1/16W MF 402
R193[1] 15K 5% 1/16W MF 402

+2_5V_MAIN — NO STUFF R568 0 5% 1/16W MF 603
+1_8V_MAIN — R565 0 5% 1/16W MF 603
38 LTC1962_INT_VIN
C721 1uF 20% 10V CERM 603

U49 LT1962-ADJ MSOP
IN, NC, NC, SHDN, OUT, ADJ, BYP, GND
LTC1962_INT_ADJ
LTC1962_INT_BYP

+1_5V_INTREPID_PLL 8 12 38 -> 1.55V OUTPUT
C392 0.01uF 20% 10V CERM 402
R574[1] 18.7K 1% 1/16W MF 402
C723 10uF 20% 6.3V CERM 805
R567[1] 68.1K 1% 1/16W MF 402

+3V_SLEEP
R148 10K 5% 1/16W MF 402 — CBUS_INT_L 14 18
PCI INTERRUPTS
+3V_MAIN
R746 10K 5% 1/16W MF 402 — AIRPORT_PCI_INT_L 14 24 39
R158 10K 5% 1/16W MF 402 — NEC_PCI_INT_L 14 17

+3V_MAIN
GPIO/EXTINT PULLUPS
R187 10K — USB_PWREN_EF_L 14
R191 10K — USB_OC_EF_L 14
RP11 10K — USB_OC_AB_L 14
RP11 10K SM1 — USB_PWREN_CD_L 14
RP8 10K SM1 — USB_PWREN_AB_L 14
RP11 10K SM1 — USB_OC_CD_L 14
RP8 10K SM1 — INT_EXTINT14_PU 14
RP5 10K SM1 — INT_EXTINT8_PU 14
RP6 10K SM1 — COMM_RING_DET_L 14 25 29 39
RP11 10K SM1 — INT_GPIO15_PU 14
RP6 10K SM1 — PMU_INT_NMI 14 29
RP6 10K SM1 — PMU_INT_L 14 29
RP7 10K SM1 — INT_GPIO12_PU 14
RP7 10K SM1 — INT_EXTINT13_PU 14
RP4 10K SM1 — INT_EXTINT16_PU 14
RP5 10K SM1 — INT_EXTINT11_PU 14
RP6 10K SM1 — INT_EXTINT10_PU 14
RP4 10K SM1 — INT_EXTINT12_PU 14
RP8 10K SM1 — INT_GPIO9_PU 14
RP8 10K SM1 — INT_GPIO1_PU 14 33
R153 10K SM1 — INT_EXTINT3_PU 14
USB_MODEM RP15 10K SM1 — INT_MOD_DTO_UF 14
USB_MODEM RP15 10K SM1 — INT_MOD_CLKOUT_UF 14
USB_MODEM RP15 10K SM1 — INT_MOD_DTI 14 25
USB_MODEM RP15 10K SM1 — INT_MOD_SYNC_UF 14
USB_MODEM R206 10K — INT_MOD_BITCLK_UF 14
R166 100K — SND_HW_RESET_L 14 25 39

+3V_MAIN — SSCG L15 400-OHM-EMI SM-1
+2_5V_MAIN — SSCG L14 400-OHM-EMI SM-1
+3V_CG_PLL_MAIN
MAIN_RESET_L
NO STUFF R286[1] 0 — SSCG R287[1] 10K — SSCG C400 0.1uF 10V CERM 402
SSCG C402 1uF 10V CERM 603 — SSCG C399 0.1uF 10V CERM 402
+2_5V_CG_MAIN
SSCG C394 0.1uF 10V CERM 402
NO STUFF R288[1] 10K — NO STUFF R295[2] 10K

U31 CY28512D TSSOP
CRITICAL
CLKIN 20 — 35 14 INT_REF_CLK_OUT
FSEL 3 — 14 CG_FSEL
SCLK 9 — 39 25 13 INT_I2C_CLK1
SDATA 8 — 39 25 13 INT_I2C_DATA1
ADDRSEL 14 — CG_ADDRSEL
RESET* 17 — 29 14 SYSTEM_CLK_EN
PD* 13 — CG_RESET_L
LOCK 2 — CG_LOCK
ODSEL 4 — NC
CPU0 16 — CG_CLKOUT 1
VDDI 1, VDDI 10, VDDA 12, VDDO 5, VDDO 18
VSS0 7, VSS1 19, VSSA 11, VSSC 6, VSSQ 15
INTERNAL 250K PULL-UP
OUTPUT IMPEDANCE ~18-20 OHMS
INTERNAL 250K PULL-UP
OPEN DRAIN OUTPUT
INTERNAL 250K PULL-UP

SSCG R293 33 — INT_REF_CLK_IN 14 35
SSCG R292[2] 75 — PLACE NEAR INTREPID TO MINIMIZE OVERSHOOT
SSCG R284 0 — 33 14 VCORE_VGATE
NO STUFF R296[2] 10K — 38 33 14 VCORE_VGATE
SSCG R142 0 — 38 33 14 VCORE_VGATE

NO STUFF J9 U.FL-R_SMT F-ST-SM — CLK18M_INT_EXT 35
NO STUFF R134 0 — 35 CLK18M_INT_XOUT
NO STUFF R113[1] 51
NO STUFF R144 10M
R143[1] 0
CRITICAL Y2 18.432M 8X4.5MM-SM — CLK18M_XTAL_IN 35
C152 22pF 5% 50V CERM 402
C151 22pF 5% 50V CERM 402
CRYSTAL LOAD CAPACITANCE IS 16PF
R218 0 — 35 14 INT_REF_CLK_OUT — 35 INT_REF_CLK_OUT_UF — 35 14 INT_REF_CLK_IN

HWPLL_ TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0004	197S0035		Y2	Alt. for Siward Part

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES	RES-0402-V2	RESISTOR	10K		1/16W	5%	R292	NO_SSCG

R240 4.7 — +1_5V_INTREPID_PLL8 38
C337 0.22uF 20% 6.3V CERM 402
R280 4.7 — +1_5V_INTREPID_PLL4 38
C389 0.22uF 20% 6.3V CERM 402
R279 4.7 — +1_5V_INTREPID_PLL3 38
C388 0.22uF 20% 6.3V CERM 402
R243 4.7 — +1_5V_INTREPID_PLL2 38
C386 0.22uF 20% 6.3V CERM 402
R201 4.7 — +1_5V_INTREPID_PLL1 38
C387 0.22uF 20% 6.3V CERM 402

+3V_MAIN — L13 FERR-EMI-100-OHM SM
+3V_INTREPID_USB 38
C235 0.01uF 20% 10V CERM 402
C246 0.1uF 20% 10V CERM 402
C256 10uF 20% 6.3V CERM 805

U51 INTREPID-REV2.1 CRITICAL (6 OF 9) BGA

PCI VDD15A_1 (PLL1) AA16 — PCI VDD15A_2 (PLL2) AJ12 — PCI VDD15A_3 (PLL3) AJ17 — PCI VDD15A_4 (PLL7) AJ18 — VDD15A_8 (PLL9) AG29
VDDU33_1 T8 — VDDU33_2 U8

GPIO0 G5 — VCORE A/B SEL
GPIO1 E1
GPIO2 J7
GPIO3 J8
GPIO4 H5
GPIO5 L9
GPIO6 H4
GPIO9 J5
GPIO11 K8
GPIO12 F1
GPIO15 K7
GPIO16
GENERAL PURPOSE I/O'S

14 CG_FSEL
33 14 INT_GPIO1_PU
39 25 COMM_SHUTDOWN
39 25 COMM_RESET_L
27 FW_PHY_PD
39 25 SND_HP_MUTE_L
25 SND_AMP_MUTE_L
14 INT_GPIO9_PU
39 25 14 SND_HW_RESET_L
14 INT_GPIO12_PU
14 INT_GPIO15_PU
26 INT_ENET_RST_L

39 29 25 14 COMM_RING_DET_L — F33
29 14 PMU_INT_L — E34
19 AGP_ATI_INT_L — C33
14 INT_EXTINT3_PU — D34
39 25 SND_LIN_SENSE_L — B33
26 ENET_ENERGY_DET — A33
39 24 14 AIRPORT_PCI_INT_L — E31
18 14 CBUS_INT_L — G30
14 INT_EXTINT8_PU — D31
29 14 PMU_INT_NMI — C32
14 INT_EXTINT10_PU — B32
14 INT_EXTINT11_PU — E30
14 INT_EXTINT12_PU — J9
14 INT_EXTINT13_PU — F4
14 INT_EXTINT14_PU — D1
39 25 SND_HP_SENSE_L — E2
14 INT_EXTINT16_PU — H7
17 14 NEC_PCI_INT_L — G4
5 MPIC_CPU_INT_L — D30
39 29 24 17 PMU_PME_L — AJ7
29 INT_PROC_SLEEP_REQ_L — AT6
29 INT_PEND_PROC_INT — AN8

EXTINT0 EXTINT1 EXTINT2 EXTINT3 EXTINT4 EXTINT5 EXTINT6 EXTINT7 EXTINT8 EXTINT9 EXTINT10 EXTINT11 EXTINT12 EXTINT13 EXTINT14 EXTINT15 EXTINT16 EXTINT17 CPU_INT
INTERRUPTS
POWERBOOK SPARE
CBUS_REG_L
CBUS_IREQ_L

PCIPME
PROCSLEEPREQ
PENDPROCINT

35 CLK18M_INT_XIN — U4
XTAL_IN
XTAL_OUT
29 14 SYSTEM_CLK_EN — AN7
STOPXTAL
29 INT_WATCHDOG_L — AT7
WATCHDOG
CLOCKS
BUF_REF_CLK_OUT — V15
35 INT_REF_CLK_OUT_UF
SS_REF_CLK_IN — K9
35 14 INT_REF_CLK_IN

SCCTXDA AF9 — COMM_TXD_L 25 39
SCCRTSA AN3 — COMM_RTS_L 25 39
SCCDTRA AF10 — COMM_DTR_L 25 39
SCCRXDA AG11 — COMM_RXD 25 39
SCCGPIOA AG9 — COMM_GPIO_L 25 39
VIA SCCTRXCA AT4 — COMM_TRXC 25 39
MISO SCCTXDB AR4 — PMU_FROM_INT 29
REQ* SCCRTSB AL5 — PMU_REQ_L 14 29
MOSI SCCRXDB AG10 — PMU_TO_INT 29
ACK* SCCGPIOB AP4 — PMU_ACK_L 29
SCK SCCTRXCB AM5 — PMU_CLK 29

USB_VD0_P L8 — USB_DAP 14
USB_VD0_N L7 — USB_DAM 14
USB_VD1_P G2 — USB_DBP 14
USB_VD1_N G1 — USB_DBM 14
USB_PRTPWR0 J4 — USB_PWREN_AB_L 14
USB_PWRFLT0 K4 — USB_OC_AB_L 14
USB_VD2_P H2 — USB_DCP 14
USB_VD2_N H1 — USB_DCM 14
USB_VD3_P M7 — USB_DDP 14
USB_VD3_N M8 — USB_DDM 14
USB_PRTPWR1 J2 — USB_PWREN_CD_L 14
USB_PWRFLT1 J1 — USB_OC_CD_L 14
USB_VD4_P K5 — USB_DEP 14 37
USB_VD4_N L5 — USB_DEM 14 37
USB_VD5_P P8 — USB_DFP 14 37
USB_VD5_N N8 — USB_DFM 14 37
USB_PRTPWR2 M5 — USB_PWREN_EF_L 14
USB_PWRFLT2 N7 — USB_OC_EF_L 14
USB

AUD_DTO R4 — INT_I2S0_SND_TO_DAC_UF
AUD_DTI R7 — INT_I2S0_SND_FROM_ADC 25 39
AUD_SYNC T5 — INT_I2S0_SND_LRCLK_UF
AUD_BITCLK P2 — INT_I2S0_SND_SCLK_UF
AUD_CLKOUT R5 — INT_I2S0_SND_MCLK_UF
AUDIO/I2S
MOD_DTO R2 — 14 INT_MOD_DTO_UF
(SIGNAL FROM MODEM) MOD_DTI T4 — INT_MOD_DTI 14 25
MOD_SYNC R1 — 14 INT_MOD_SYNC_UF
MOD_BITCLK V8 — 14 INT_MOD_BITCLK_UF
MOD_CLKOUT P1 — 14 INT_MOD_CLKOUT_UF

IICCLK_2 AL4
IICDATA_2 AH8
IIC

+3V_SLEEP
R258[2] 1K — INT_I2C_CLK2 25 39
R241[2] 1K — INT_I2C_DATA2 25 39

RP13 47 — INT_I2S0_SND_TO_DAC 25 39
RP13 47 — INT_I2S0_SND_LRCLK 25 39
RP13 47 — INT_I2S0_SND_SCLK 25 39
RP13 47 — INT_I2S0_SND_MCLK 25 35 39
SOFT_MODEM RP47 47 — INT_MOD_DTO 25
SOFT_MODEM RP47 47 — INT_MOD_SYNC 25
SOFT_MODEM RP47 47 — INT_MOD_BITCLK 25
SOFT_MODEM RP47 47 — INT_MOD_CLKOUT 25

VSSA1 (PLL1) AA15 — VSSA2 (PLL2) AJ13 — VSSA3 (PLL3) AJ16 — VSSA4 (PLL7) AK18 — VSSA_8 (PLL9) AH29
VSSU_1 R9 — VSSU_2 R8

INT - USB/GPIOS/I2S

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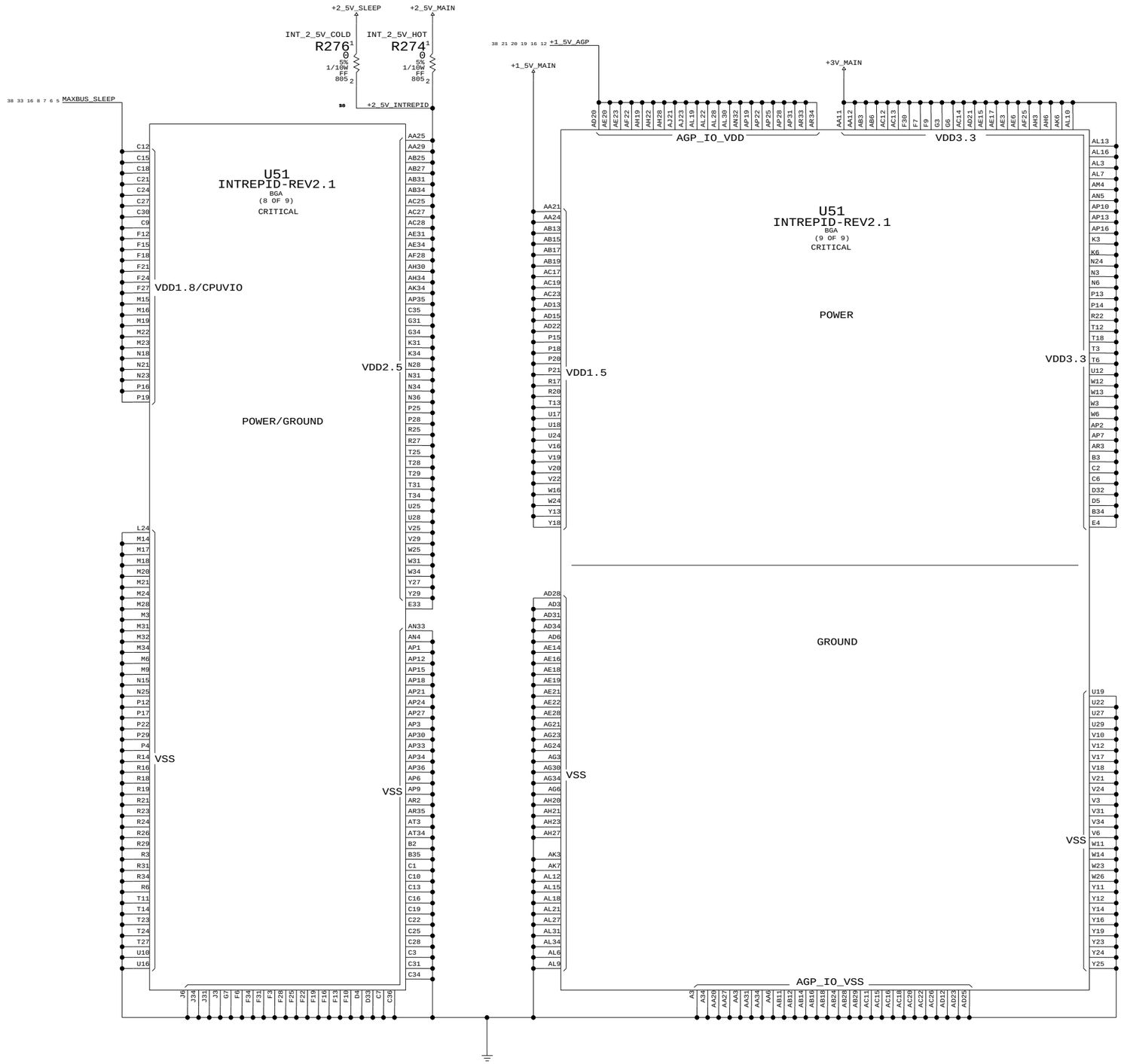
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401243	AA
SCALE: NONE	SHT 14 OF 44	



Intrepid Power

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401243	AA
SCALE: NONE	SHT 15 OF 44	

INTREPID MAXBUS DECOUPLING

24 Balls
4 X 10UF (0805)
28 X 0.22UF (0402)

33 15 8 7 6 5 MAXBUS_SLEEP

C148 10uF 20% 6.3V CERM 805 — C142 10uF 20% 6.3V CERM 805 — C144 10uF 20% 6.3V CERM 805 — C146 10uF 20% 6.3V CERM 805

C182 C178 C141 C145 C214 C163 C164 C225 C160 C159
C204 C166 C205 C223 C229 C181 C207 C208 C183 C180
C165 C206 C147 C149 C179 C162 C161 C213

(0.22uF 20% 6.3V CERM 402)

INTREPID CORE DECOUPLING

30 Balls
4 X 10UF (0805)
29 X 0.22UF (0402)

+1_5V_MAIN

C324 10uF 20% 6.3V CERM 805 — C325 10uF 20% 6.3V CERM 805 — C201 10uF 20% 6.3V CERM 805 — C200 10uF 20% 6.3V CERM 805

C299 C279 C262 C292 C248 C302 C300 C290 C272 C259
C301 C278 C226 C238 C250 C263 C224 C222 C261 C227
C271 C310 C288 C260 C303 C287 C258 C236 C289

(0.22uF 20% 6.3V CERM 402)

INTREPID AGP I/O DECOUPLING

21 Balls
4 X 10UF (0805)
21 X 0.22UF (0402)

38 21 20 19 15 12 +1_5V_AGP

C381 10uF 20% 6.3V CERM 805 — C380 10uF 20% 6.3V CERM 805 — C382 10uF 20% 6.3V CERM 805 — C379 10uF 20% 6.3V CERM 805

C367 C319 C330 C363 C366 C332 C361 C320 C328 C364
C365 C329 C345 C346 C373 C344 C331 C312 C354 C347
C321

(0.22uF 20% 6.3V CERM 402)

INTREPID 3.3V DECOUPLING

57 Balls
4 X 10UF (0805)
40 X 0.22UF (0402)

+3V_MAIN

C378 10uF 20% 6.3V CERM 805 — C376 10uF 20% 6.3V CERM 805 — C377 10uF 20% 6.3V CERM 805 — C375 10uF 20% 6.3V CERM 805

C170 C358 C268 C327 C342 C215 C352 C171 C158 C309
C175 C357 C351 C350 C286 C176 C189 C167 C371 C359
C285 C283 C269 C221 C234 C247 C257 C343 C313 C228
C360 C308 C318 C237 C317 C341 C177 C212 C349 C184

(0.22uF 20% 6.3V CERM 402)

INTREPID DDR DECOUPLING

44 Balls
4 X 10UF (0805)
46 X 0.22UF (0402)

38 15 10 9 +2_5V_INTREPID

C314 10uF 20% 6.3V CERM 805 — C322 10uF 20% 6.3V CERM 805 — C191 10uF 20% 6.3V CERM 805 — C202 10uF 20% 6.3V CERM 805

C304 C266 C172 C281 C243 C253 C334 C241 C348 C192
C306 C252 C275 C297 C240 C218 C274 C369 C368 C168
C265 C251 C216 C254 C305 C186 C219 C315 C264 C294
C323 C273 C242 C203 C333 C217 C230 C293 C231 C296
C239 C316 C185 C282 C295 C280

(0.22uF 20% 6.3V CERM 402)

INTREPID/MAIN 2.5V DECOUPLING

10 X 0.22UF (0402)

+2_5V_MAIN

C770 C139 C335 C735 C245 C736 C739 C395 C374 C385

(0.22uF 20% 6.3V CERM 402)

Place these 2.5V Decoupling Caps near the Edge of +2.5V_MAIN and +2.5V_INTREPID split

Intrepid Decoupling

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401243	AA

SCALE	SHT OF
NONE	16 44

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0608	197S0038		Y1	Alt. for Siward Part

+3V_NEC_VDD 17 38

C749 0.1uF 20% 10V CERM 402
C746 0.1uF 20% 10V CERM 402
C761 0.1uF 20% 10V CERM 402
C750 0.1uF 20% 10V CERM 402
C756 0.1uF 20% 10V CERM 402
C748 0.1uF 20% 10V CERM 402
C769 0.1uF 20% 10V CERM 402
C752 0.1uF 20% 10V CERM 402
C747 0.1uF 20% 10V CERM 402
C197 10uF 20% 6.3V CERM 805
C765 0.1uF 20% 10V CERM 402
C768 0.1uF 20% 10V CERM 402

+3V_MAIN

L7 FERR-EMI-100-OHM SM

R172 0 5% 1/16W MF 603

C760 0.1uF 20% 10V CERM 402
C751 0.1uF 20% 10V CERM 402
C173 10uF 20% 6.3V CERM 805

38 NEC_AVDD

38 17 +3V_NEC_VDD

H3 M4 C8 P2 P3 P12 A13 A12 A3 E2 N8 L13 J13 H13 F13 D13 G12 H4 D7 N10 M12

VDD_PCI — VDD — AVDD

Y1's LOAD CAPACITANCE = 16 pF

CRITICAL
Y1 30.0000M 8X4.5MM-SM

C759 27pF 5% 50V CERM 402
C136 27pF 5% 50V CERM 402
R124 100 5% 1/16W MF 402

NEC_XT2_R

CRITICAL
U17
NEC_uPD720101_USB2
FBGA

39 37 24 18 12 9 PCI_AD<0>	M5	AD0	
39 37 24 18 12 9 PCI_AD<1>	P5	AD1	
39 37 24 18 12 9 PCI_AD<2>	N5	AD2	
39 37 24 18 12 9 PCI_AD<3>	P4	AD3	
39 37 24 18 12 9 PCI_AD<4>	N4	AD4	
39 37 24 18 12 9 PCI_AD<5>	M3	AD5	
39 37 24 18 12 9 PCI_AD<6>	N3	AD6	
39 37 24 18 12 9 PCI_AD<7>	M1	AD7	
39 37 24 18 12 9 PCI_AD<8>	L2	AD8	
39 37 24 18 12 9 PCI_AD<9>	L1	AD9	
39 37 24 18 12 9 PCI_AD<10>	K2	AD10	
39 37 24 18 12 9 PCI_AD<11>	L3	AD11	
39 37 24 18 12 9 PCI_AD<12>	K1	AD12	
39 37 24 18 12 9 PCI_AD<13>	K3	AD13	
39 37 24 18 12 9 PCI_AD<14>	J2	AD14	
39 37 24 18 12 9 PCI_AD<15>	J1	AD15	
39 37 24 18 12 9 PCI_AD<16>	F2	AD16	
39 37 24 18 12 9 PCI_AD<17>	E3	AD17	
39 37 24 18 12 9 PCI_AD<18>	E1	AD18	
39 37 24 18 12 9 PCI_AD<19>	D3	AD19	
39 37 24 18 12 9 PCI_AD<20>	D1	AD20	
39 37 24 18 12 PCI_AD<21>	D2	AD21	
39 37 24 18 12 PCI_AD<22>	C2	AD22	
39 37 24 18 12 PCI_AD<23>	C1	AD23	
39 37 24 18 12 9 PCI_AD<24>	B4	AD24	
39 37 24 18 12 9 PCI_AD<25>	A4	AD25	
39 37 24 18 12 9 PCI_AD<26>	B5	AD26	
(PCI_AD<27>)	C4	AD27	
39 37 24 18 12 9 PCI_AD<28>	A5	AD28	
39 37 24 18 12 9 PCI_AD<29>	C5	AD29	
39 37 24 18 12 9 PCI_AD<30>	B6	AD30	
39 37 24 18 12 9 PCI_AD<31>	A6	AD31	
37 24 18 12 PCI_CBE<0>	M2	CBE0	
37 24 18 12 PCI_CBE<1>	J3	CBE1	
37 24 18 12 PCI_CBE<2>	F1	CBE2	
37 24 18 12 PCI_CBE<3>	C3	CBE3	
39 37 24 18 12 PCI_PAR	J4	PAR	
39 37 24 18 12 PCI_FRAME_L	F3	FRAME	
39 37 24 18 12 PCI_IRDY_L	F4	IRDY	
39 37 24 18 12 PCI_TRDY_L	G1	TRDY	
39 37 24 18 12 PCI_STOP_L	G3	STOP	
NEC_IDSEL	B3	IDSEL	
39 37 24 18 12 PCI_DEVSEL_L	G2	DEVSEL	
12 NEC_PCI_REQ_L	C6	REQ	
12 NEC_PCI_GNT_L	D6	GNT	
18 PCI_PERR_L	H2	PERR	
18 PCI_SERR_L	H1	SERR	
NEC_PCI_INTA_L	C7	INTA	
NEC_PCI_INTB_L	B7	INTB	
NEC_PCI_INTC_L	A7	INTC	
35 12 CLK33M_NEC	A8	PCLK	
17 NEC_IO_RESET_L	B8	VBBRST	
NEC_CRUN_L	N6	CRUN	
17 NEC_PME_L	D9	PME	
17 NEC_MAIN_RESET_L	C9	VCCRST	
NEC_SMI_L_TP	L6	SMI	
17 NEC_LEGC	L7	LEGC	

R636 22 5% 1/16W MF 402

Series Rpaks required to facilitate NAND-tree testing

RP45 47 5% 1/16W SM1

14 NEC_PCI_INT_L

R617 4.7K 5% 1/16W MF 402

RP44 47 5% 1/16W SM1

29 26 23 IO_RESET_L
39 29 24 14 PMU_PME_L
39 29 24 19 18 14 MAIN_RESET_L
17 NEC_LEGC

NEC_IO_RESET_L 17
NEC_PME_L 17
NEC_MAIN_RESET_L 17

VSS

B1 N1 P10 N14 H14 B14 A2 B2 N2 N13 B13 M11 L12 H12 D12 G4 J11 F11 D8

XT1/SCLK	L9	NEC_XT1	
XT2	P8	NEC_XT2	
RSDM1	M14	NEC_USB_RSDM1	
DM1	M13	(NEC_USB_DAM)	
DP1	L14	(NEC_USB_DAP)	
RSDP1	K13	NEC_USB_RSDP1	
RSDM2	K14	NEC_USB_RSDM2	
DM2	K12	(NEC_USB_DBM)	
DP2	J14	(NEC_USB_DBP)	
RSDP2	J12	NEC_USB_RSDP2	
RSDM3	H11	NC	
DM3	G11		
DP3	G13		
RSDP3	G14	NC	
RSDM4	F12	NC	
DM4	F14		
DP4	E12		
RSDP4	E14	NC	
RSDM5	E13	NC	
DM5	D14		
DP5	C13		
RSDP5	C14	NC	
RREF	P11	NEC_RREF	
OCI1	B12	NEC_LUSB_OCI 17	
OCI2	B11	NEC_RUSB_OCI 17	
OCI3	B10	NEC_OCI<3>	
OCI4	A10	NEC_OCI<4>	
OCI5	B9	NEC_OCI<5>	
PPON1	C12 OUT	NEC_LUSB_PPON 25 39	
PPON2	A11 OUT	NEC_RUSB_PPON 25 39	
PPON3	C11 OUT	NEC_PPON3_TP	
PPON4	C10 OUT	NEC_PPON4_TP	
PPON5	A9 OUT	NEC_PPON5_TP	
NC1	P6	NEC_NC<1>	
NC2	M6	NEC_NC<2>	
NTEST1	M8 IPD	NC	
SMC	M7 IPD	NC	
TEB	N7 IPD	NC	
AMC	P7 IPD	NEC_AMC_TP	
TEST	L8 IPD	NC	
NANDTEST	M10	NEC_NANDTESTEN_TP	
SRCLK	M9	NC	
SRDTA	N9	NEC_NANDTESTOUT_TP	
SRMOD	P9 IPD	NC	
AVSS			
AVSS(R)	N11 P13 M12	17 NEC_AVSS_F	

R614 9.09K 1% 1/16W MF 402 — Tie to GND (NEC_AVSS_F) at ball N11

NEC_AVSS_F 17

R798 0 5% 1/10W MF 603

RP43 10K 5% 1/16W SM1
RP43 10K 5% 1/16W SM1
RP43 10K 5% 1/16W SM1
RP43 10K 5% 1/16W SM1
R606 10K 5% 1/16W MF 402
R615 1K 5% 1/16W MF 402
R632 1K 5% 1/16W MF 402

+3V_NEC_VDD 17 38

NEC documentation indicates that NCs must be tied high.

R613 36 1% 1/16W MF 402 — NEC_USB_DAM 25 37 39
R612 36 1% 1/16W MF 402 — NEC_USB_DAP 25 37 39
Low/Full/High Speed (External)
R609 36 1% 1/16W MF 402 — NEC_USB_DBM 25 37 39
R610 36 1% 1/16W MF 402 — NEC_USB_DBP 25 37 39
Low/Full/High Speed (External)

+3V_MAIN

RP43 10K 5% 1/16W SM1
RP43 10K 5% 1/16W SM1
R607 0 5% 1/16W MF 402
R608 0 5% 1/16W MF 402

17 NEC_LUSB_OCI — NEC_LUSB_OCI_UF 25 39
17 NEC_RUSB_OCI — NEC_RUSB_OCI_UF 25 39

NO STUFF C743 0.1UF 20% 10V CERM 402
NO STUFF C744 0.1UF 20% 10V CERM 402

USB 2.0

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II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401243	AA
SCALE: NONE	SHT 17 OF 44	

PCI1510 PULL-UPS

+3V_SLEEP

R718 10K 5% 1/16W MF 402 — PCI_PERR_L (17 18)
R714 10K 5% 1/16W MF 402 — PCI_SERR_L (17 18)
R722 10K 5% 1/16W MF 402 — CBUS_SUSPEND_PU (18)

+2_5V_SLEEP

C787 4.7uF 20% 6.3V CERM 805
C786 0.22uF 20% 6.3V CERM 402

C60 10uF 20% 6.3V CERM 805
C776 10uF 20% 6.3V CERM 805
C789 0.22uF 20% 6.3V CERM 402
C791 0.22uF 20% 6.3V CERM 402
C784 0.22uF 20% 6.3V CERM 402
C782 0.22uF 20% 6.3V CERM 402
C783 0.22uF 20% 6.3V CERM 402
C778 0.22uF 20% 6.3V CERM 402
C775 0.22uF 20% 6.3V CERM 402

R721 10K 5% 1/16W MF 402

A7 C13 D5 E1 M1 N7 N11 — VCC

PCI1510_VR_EN_L (DA)

U8
PCI1510GGU
BGA

NC	H10	CLK_48_RSVD/NC
	DA	VR_EN*
	L8	VR_PORT
	N8	AD0
	M7	AD1
	L7	AD2
	N6	AD3
	K4	AD4
	M6	AD5
	L6	AD6
	N5	AD7
	N4	AD8
	M2	AD9
	M5	AD10
	L4	AD11
	N3	AD12
	K5	AD13
	L5	AD14
	M4	AD15
	J4	AD16
	H1	AD17
	H3	AD18
(PCI_AD<19>)	H2	AD19
	G2	AD20
	G4	AD21
	F1	AD22
	C3	AD23
	F3	AD24
	E2	AD25
	F4	AD26
	B1	AD27
	D2	AD28
	E4	AD29
	D3	AD30
	E3	AD31
	K6	C/BE0*
	M3	C/BE1*
	J2	C/BE2*
	A1	C/BE3*
	N1	PAR
	K1	IRDY
	L2	SERR
CBUS_PCI_IDSEL	F2	IDSEL
	K3	PERR
	J1	FRAME
	L1	STOP
	J3	TRDY
	K2	DEVSEL
CBUS_PCI_RESET_L	G3	PRST
CBUS_PCI_REQ_L	C2	REQ
CBUS_PCI_GNT_L	C1	GNT
CLK33M_CBUS	G1	PCLK
NC	M9	SPKROUT
NC	M8	RI_OUT/PME
CBUS_SUSPEND_PU	N10	SUSPEND
CBUS_INT_L	K7	MFUNC0
CBUS_MFUNC1_PD	N9	MFUNC1
CBUS_MFUNC2_PD	L9	MFUNC2
CBUS_MFUNC3_PD	K10	MFUNC3
CBUS_MFUNC4_PD	M10	MFUNC4
CBUS_MFUNC5_PD	N12	MFUNC5
CBUS_MFUNC6_PD	L10	MFUNC6
	L11	GRST

CRITICAL
CLAMP FOR PC-CARD
CLAMP FOR PCI

	B11	VCCCB
	L3	VCCP
CBUS_VCCD0_L	N13	VCCD0*
CBUS_VCCD1_L	L12	VCCD1*
CBUS_VPPD0	K9	VPPD0
CBUS_VPPD1	M11	VPPD1
CBUS_DET_1_L (18 39)	L13	CD1*/CCD1*
CBUS_DET_2_L (18 39)	B5	CD2*/CCD2*
CBUS_IORD_L (18)	F12	IORD*/CAD13
CBUS_IOWR_L (18)	C11	IOWR*/CAD15
CBUS_OE_L (18)	G10	OE*/CAD11
CBUS_CE1_L (18)	H13	CE1*/CC/BE0*
CBUS_VS1 (18)	B2	VS1*/CVS1
CBUS_VS2 (18)	A9	VS2*/CVS2
CBUS_WE_L (18)	D13	WE*/CGNT*
CBUS_READY (18)	A6	RDY/IREQ*/CINT*
CBUS_RESET_L (18)	D8	RESET/CRST*
CBUS_REG_L (18)	A8	REG*/CC/BE3*
CBUS_BVD1_L (18)	C6	BVD1/CSTSCHG/STSCHG*/RI*
CBUS_BVD2_L (18)	D6	BVD2/SPKR*/CAUDIO
INTEGRATED PULL-UP	A5	WP/IOIS16*/CCLKRUN*
CBUS_CE2_L (18)	G13	CE2/CAD10*
CBUS_INPACK_L (18)	B8	INPACK/CREQ*
CBUS_WAIT_L (18)	B6	WAIT/CSERR*
CBUS_ADDR<0> (18)	C7	A0/CAD26
CBUS_ADDR<1> (18)	D7	A1/CAD25
CBUS_ADDR<2> (18)	B7	A2/CAD24
CBUS_ADDR<3> (18)	D10	A3/CAD23
CBUS_ADDR<4> (18)	B12	A4/CAD22
CBUS_ADDR<5> (18)	C8	A5/CAD21
CBUS_ADDR<6> (18)	C9	A6/CAD20
CBUS_ADDR<7> (18)	A12	A7/CAD18
CBUS_ADDR<8> (18)	E11	A8/CC/BE1*
CBUS_ADDR<9> (18)	F11	A9/CAD14
CBUS_ADDR<10> (18)	G11	A10/CAD9
CBUS_ADDR<11> (18)	G12	A11/CAD12
CBUS_ADDR<12> (18)	D9	A12/CC/BE2*
CBUS_ADDR<13> (18)	E12	A13/CPAR
CBUS_ADDR<14> (18)	D12	A14/CPERR*
CBUS_ADDR<15> (18)	C10	A15/CIRDY*
CBUS_ADDR_16_UF	B13	A16/CCLK
CBUS_ADDR<17> (18)	F10	A17/CAD16
CBUS_ADDR<18> (18)	E13	A18/RSVD
CBUS_ADDR<19> (18)	A13	A19/CBLOCK*
CBUS_ADDR<20> (18)	E10	A20/CSTOP*
CBUS_ADDR<21> (18)	D11	A21/CDEVSEL*
CBUS_ADDR<22> (18)	C12	A22/CTRDY*
CBUS_ADDR<23> (18)	A10	A23/CFRAME*
CBUS_ADDR<24> (18)	B10	A24/CAD17
CBUS_ADDR<25> (18)	B9	A25/CAD19
CBUS_DATA<0> (18)	A4	D0/CAD27
CBUS_DATA<1> (18)	C4	D1/CAD29
CBUS_DATA<2> (18)	A3	D2/RSVD
CBUS_DATA<3> (18)	K11	D3/CAD0
CBUS_DATA<4> (18)	K12	D4/CAD1
CBUS_DATA<5> (18)	J13	D5/CAD3
CBUS_DATA<6> (18)	J10	D6/CAD5
CBUS_DATA<7> (18)	H12	D7/CAD7
CBUS_DATA<8> (18)	C5	D8/CAD28
CBUS_DATA<9> (18)	B4	D9/CAD30
CBUS_DATA<10> (18)	B3	D10/CAD31
CBUS_DATA<11> (18)	M12	D11/CAD2
CBUS_DATA<12> (18)	J11	D12/CAD4
CBUS_DATA<13> (18)	K13	D13/CAD6
CBUS_DATA<14> (18)	J12	D14/RSVD
CBUS_DATA<15> (18)	H11	D15/CAD8

R724 47 5% 1/16W MF 402 — CBUS_ADDR<16> (18)

R719 22 5% 1/16W MF 402

MAIN_RESET_L (39 29 24 19 17 14) — R723 47 5% 1/16W MF 402

RP1 10K 5% 1/32W 25V SM

CBUS_MFUNC1_PD (18)	6
CBUS_MFUNC2_PD (18)	4
CBUS_MFUNC3_PD (18)	7
CBUS_MFUNC4_PD (18)	3
CBUS_MFUNC5_PD (18)	9
CBUS_MFUNC6_PD (18)	8
	2
	1
	5
	10

GND — A2 A11 D1 F13 H4 K8 M13 N2

+3V_MAIN
+5V_MAIN

U4
TPS2211
SSOI

NC	9	
	5	V_12
	6	V_5_1
	3	V_5_2
	4	V_3_1
		V_3_2
	1	VCCD0
	2	VCCD1
	15	VPPD0
	14	VPPD1
TPS2211_SHTDWN_L	16	SHTDWN
	7	GND
	10	AVPP
	11	AVCC0
	12	AVCC1
	13	AVCC2
	8	OC

SLEEP_L_LS5 (26 34 28 33 32)

R726 0 5% 1/16W MF 402

+VPP_CBUS_SW (18 38)
+VCC_CBUS_SW (18 38)

C40 0.1uF 20% 10V CERM 402
C37 0.1uF 20% 10V CERM 402

MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES TO MINIMIZE INDUCTANCE!

0.1UF ARE USED TO INCREASE ESD DISCHARGES OF UP TO 10KV

TI REFERENCE SCHEMATIC DID NOT HAVE BULK ON +VCC_CBUS_SW

C796 2.2uF 20% 10V CERM 805
C800 2.2uF 20% 10V CERM 805

PC CARD/CARDBUS CONNECTOR

CRITICAL
J5
QT500806-L111
M-ST-SM1

CBUS_DET_1_L (18 39)	4	3	CBUS_DATA<4> (18)
CBUS_DATA<11> (18)	6	5	CBUS_DATA<5> (18)
CBUS_DATA<12> (18)	8	7	CBUS_DATA<6> (18)
CBUS_DATA<13> (18)	10	9	
	12	11	CBUS_DATA<7> (18)
CBUS_DATA<14> (18)	14	13	CBUS_CE1_L (18)
CBUS_DATA<15> (18)	16	15	CBUS_ADDR<10> (18)
CBUS_CE2_L (18)	18	17	CBUS_OE_L (18)
CBUS_VS1 (18)	20	19	
	22	21	CBUS_ADDR<11> (18)
CBUS_IORD_L (18)	24	23	CBUS_ADDR<9> (18)
CBUS_IOWR_L (18)	26	25	CBUS_ADDR<8> (18)
CBUS_ADDR<17> (18)	28	27	CBUS_ADDR<13> (18)
CBUS_ADDR<18> (18)	30	29	
	32	31	CBUS_ADDR<14> (18)
CBUS_ADDR<19> (18)	34	33	CBUS_WE_L (18)
CBUS_ADDR<20> (18)	36	35	CBUS_READY (18)
CBUS_ADDR<21> (18)	38	37	+VCC_CBUS_SW (18 38)
+VCC_CBUS_SW (18 38)	40	39	
	42	41	+VPP_CBUS_SW (18 38)
+VPP_CBUS_SW (18 38)	44	43	CBUS_ADDR<16> (18)
CBUS_ADDR<22> (18)	46	45	CBUS_ADDR<15> (18)
CBUS_ADDR<23> (18)	48	47	CBUS_ADDR<12> (18)
CBUS_ADDR<24> (18)	50	49	
	52	51	CBUS_ADDR<7> (18)
CBUS_ADDR<25> (18)	54	53	CBUS_ADDR<6> (18)
CBUS_VS2 (18)	56	55	CBUS_ADDR<5> (18)
CBUS_RESET_L (18)	58	57	CBUS_ADDR<4> (18)
CBUS_WAIT_L (18)	60	59	
	62	61	CBUS_ADDR<3> (18)
CBUS_INPACK_L (18)	64	63	CBUS_ADDR<2> (18)
CBUS_REG_L (18)	66	65	CBUS_ADDR<1> (18)
CBUS_BVD2_L (18)	68	67	CBUS_ADDR<0> (18)
CBUS_BVD1_L (18)	70	69	
	72	71	CBUS_DATA<0> (18)
CBUS_DATA<8> (18)	74	73	CBUS_DATA<1> (18)
CBUS_DATA<9> (18)	76	75	CBUS_DATA<2> (18)
CBUS_DATA<10> (18)	78	77	CBUS_WP_L (18)
CBUS_DET_2_L (39 18)	80	79	

84 81 83 82

CARDBUS

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401243	AA
SCALE: NONE	SHT 18 OF 44	

SIL1162 DVI-Compliant Transmitter

Ext. TMDS source termination

L22 60-OHM-EMI (SM) — GPU_VCORE

C476 0.01uF 20% 16V CERM 402
C457 0.01uF 20% 16V CERM 402
C458 10uF 20% 6.3V CERM 805
C490 0.01uF 20% 16V CERM 402
C442 0.01uF 20% 16V CERM 402
C530 0.01uF 20% 16V CERM 402

GPU_VCORE_VDDCI

+3V_GPU

R323 10K 5% 1/16W MF 402

+1.5V AGP

R313 47 1% 1/16W MF 402

R338 20K 5% 1/16W MF 402

C412 0.01uF 20% 16V CERM 402

C408 0.1uF 20% 10V CERM 402 (PLACE C408 CLOSE TO AGPREF PIN)

R335 20K 5% 1/16W MF 402

R336 0 5% 1/16W MF 402

R325 47K 5% 1/16W MF 402

R324 47K 5% 1/16W MF 402

R372 45.3 1% 1/16W MF 402

U47 RAGE_MOBILITY M10-CSP64 64MB BGA (6 OF 6)

CRITICAL

M2	
P3	
A21	
B19	
M15	
N15	
P15	VSS
R15	
T15	
T12	
T13	
T14	
W16	
V16	
U16	
T16	
R16	
R17	
R18	
R19	
U6	
AE15	
F18	VDDCI
P25	

U47 RAGE_MOBILITY M10-CSP64 64MB BGA (1 OF 6)

CRITICAL

AB30	AD31	AGP_AD<31>	
AB27	AD30	AGP_AD<30>	
AA29	AD29	AGP_AD<29>	
AB28	AD28	AGP_AD<28>	
AA30	AD27	AGP_AD<27>	
AA27	AD26	AGP_AD<26>	
Y30	AD25	AGP_AD<25>	
AA28	AD24	AGP_AD<24>	
W30	AD23	AGP_AD<23>	
W27	AD22	AGP_AD<22>	
V30	AD21	AGP_AD<21>	
V28	AD20	AGP_AD<20>	
V29	AD19	AGP_AD<19>	
V27	AD18	AGP_AD<18>	
U30	AD17	AGP_AD<17>	
U28	AD16	AGP_AD<16>	
R27	AD15	AGP_AD<15>	
R29	AD14	AGP_AD<14>	
P28	AD13	AGP_AD<13>	
P30	AD12	AGP_AD<12>	
P27	AD11	AGP_AD<11>	
P29	AD10	AGP_AD<10>	
N28	AD9	AGP_AD<9>	
N30	AD8	AGP_AD<8>	
M30	AD7	AGP_AD<7>	
M27	AD6	AGP_AD<6>	
M29	AD5	AGP_AD<5>	
L28	AD4	AGP_AD<4>	
L30	AD3	AGP_AD<3>	
L27	AD2	AGP_AD<2>	
L29	AD1	AGP_AD<1>	
K28	AD0	AGP_AD<0>	
W28	CBEB3	AGP_CBE<3>	
U29	CBEB2	AGP_CBE<2>	
R30	CBEB1	AGP_CBE<1>	
N27	CBEB0	AGP_CBE<0>	
AG30	PCICLK	CLK66M_GPU_AGP	
U27	FRAMEB	AGP_FRAME_L	
T30	IRDYB	AGP_IRDY_L	
T28	TRDYB	AGP_TRDY_L	
T27	STOPB	AGP_STOP_L	
T29	DEVSELB	AGP_DEVSEL_L	
R28	PAR	AGP_PAR	
AF29	REQB	AGP_REQ_L	
AF27	GNTB	AGP_GNT_L	
AH29	INTAB	AGP_ATI_INT_L	
AH30	RSTB	AGP_ATI_RESET_L	
AE27	WBF	AGP_WBF_L	
AK3	VREFG	AGP_ATI_VREFG	
D8	VREF	AGP_ATI_VREF	

N29	AD_STB0	AGP_AD_STB<0>	
W29	AD_STB1	AGP_AD_STB<1>	
M28	AD_STBB0	AGP_AD_STB_L<0>	
Y29	AD_STBB1	AGP_AD_STB_L<1>	
AG28	AGP_BUSYB	AGP_BUSY_L	
K30	AGPREF	INT_AGP_VREF	
K29	AGPTEST	GPU_AGP_TEST	
U25	AGP8X_DETB	AGP8X_DET_PU	
AJ28	SUS_STAT	AGP_SUS_STAT_L_PU	
AF30	ST0	AGP_ST<0>	
AF28	ST1	AGP_ST<1>	
AE29	ST2	AGP_ST<2>	
AC28	SBA7	AGP_SBA<7>	
AB29	SBA6	AGP_SBA<6>	
AC27	SBA5	AGP_SBA<5>	
AC30	SBA4	AGP_SBA<4>	
AD27	SBA3	AGP_SBA<3>	
AD30	SBA2	AGP_SBA<2>	
AE28	SBA1	AGP_SBA<1>	
AD29	SBA0	AGP_SBA<0>	
AE30	RBFB	AGP_RBF_L	
AG29	STP_AGPB	AGP_STP_L	
AC29	SB_STB	AGP_SB_STB	
AD28	SB_STBS	AGP_SB_STB_L	
AD24	RSTB_MSK	ATI_RSTB_MSK	
Y25	DBI_LO	ATI_DBI_LO_PU	
Y27	DBI_HI	ATI_DBI_HI_PU	

U47 RAGE_MOBILITY M10-CSP64 64MB BGA (2 OF 6)

CRITICAL

B26	A17		
A26	B16		
B25	A16		
A25	B14		
C22	A14		
D21	B13		
C21	A13		
D20	D13		
C20	C13		
D22	D12		
C23	C12		
D23	D10		
A27	C10		
B27	D9		
H2	C9		
H1	B12		
J2	A12		
J1	B11		
K4	A11		
K3	B9		
L4	A9		
M3	B8		
L3	A8	VSS	VSS
M4	C7		
N2	D7		
N1	C6		
N4	D6		
N3	C4		
G30	D4		
G28	C3		
B30	D3		
D26	A5		
D16	B5		
B15	A4		
D11	B4		
B10	A2		
D5	B2		
B3	A1		
G3	B1		
E1	E4		
U1	E3		
V3	F3		
AB1	F4		
AC3	H3		
J30	H4		
J29	J3		
H30	J4		
H29	C1		
F30	C2		
F29	D1		
E30	D2		
E29	F1		
J28	F2		
J27	G1		
H28	G2		
H27	R1		
F28	R2		
F27	T1		
E28	T2		
E27	V1		
D30	V2		
D29	W1	VSS	VSS
C30	W2		
C29	T3		
A30	T4		
A29	U3		
A28	U4		
B28	W3		
D28	W4		
C28	Y3		
D27	Y4		
C27	Y1		
D25	Y2		
C25	AA1		
D24	AA2		
C24	AC1		
D18	AC2		
C18	AD1		
D17	AD2		
C17	AA3		
D15	AA4		
C15	AB3		
D14	AB4		
C14	AD3		
B17	AD4		
	AE3		
	AE4		

A10			
C5			
A3			
G4			
E2			
U2			
V4			
AB2			
AC4			
B23			
K2	VSS		
A23			
K1			
B22			
L2			
A22			
L1			

AC10	D+	GPU_THERM_DP	25
AC11	D-	GPU_THERM_DM	25
E8	TEST_YCLK	GPU_MEM_IO	19 21 38
J6	TEST_MLCK	(PULL-UP to GPU_MEM_IO)	
C8	MEMTEST	ATI_MEMTEST	
AC22	PLLTEST	NC	

MAIN_RESET_L IS TOGGLED FOR SLEEP

R337 10K 5% 1/16W MF 402 — +3V_GPU

R309 47 5% 1/16W MF 402 — MAIN_RESET_L

R388 1K 1% 1/16W MF 402 — +3V_GPU

R397 1K 1% 1/16W MF 402 — GPU_MEM_IO

R373 1K 1% 1/16W MF 402 — AGP_ATI_VREFG

PLACE VERF VOLTAGE DIVIDER CLOSE TO ATI M10 VREF PIN

R365 1K 1% 1/16W MF 402

C516 0.1uF 20% 10V CERM 402

C508 10uF 20% 6.3V CERM 805

+1.8V GPU

R370 4.7K 5% 1/16W MF 402 — ATI_MEMIO_LO

R371 4.7K 5% 1/16W MF 402 — ATI_MEMIO_HI

ATI_MEMVMODE0 — MEMVMODE0

ATI_MEMVMODE1 — MEMVMODE1

R375 4.7K 5% 1/16W MF 402 — ATI_MEMIO_HI

R376 4.7K 5% 1/16W MF 402 — ATI_MEMIO_LO

FOR 2.5 VDDR1
MEMVMODE0=1.8V
MEMVMODE1=GND

FOR 1.8 VDDR1
MEMVMODE0=GND
MEMVMODE1=1.8V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0318	197S0048		G1	Alt. for Siward Part

+3V_SLEEP

L78 400-OHM-EMI (SM-1) — EXT_TMDS

C856 10uF 20% 6.3V CERM 805
C858 100pF 5% 50V CERM 402
C860 100pF 5% 50V CERM 402 — +3V_SI_AVCC

L79 400-OHM-EMI (SM-1) — EXT_TMDS

C854 10uF 20% 6.3V CERM 805
C855 10uF 20% 6.3V CERM 805
C857 100pF 5% 50V CERM 402
C859 100pF 5% 50V CERM 402 — +3V_SI_PLLVCC

PLL NOISE SHOULD BE LESS THAN 100mV PEAK-TO-PEAK

L80 400-OHM-EMI (SM-1) — EXT_TMDS — +3V_SLEEP

C861 100pF 5% 50V CERM 402
C862 100pF 5% 50V CERM 402
C863 10uF 20% 6.3V CERM 805 — +3V_SI_VCC

MAIN_RESET_L

R832 47 5% 1/16W MF 402 — EXT_TMDS
R833 47 5% 1/16W MF 402 — NO STUFF

R835 10K 5% 1/16W MF 402
R818 10K 5% 1/16W MF 402 — NO STUFF
R823 10K 5% 1/16W MF 402 — EXT_TMDS
R825 10K 5% 1/16W MF 402 — EXT_TMDS

R837 4.99K 1% 1/16W MF 402 — EXT_TMDS

R826 330 5% 1/16W MF 402 — EXT_TMDS

SI_I2C_CLK	27	SCL/DK1
SI_I2S_DATA	26	SDA/DK0
SI_I2	24	CTL3/A2
SI_RST_L	25	ISEL/RST*
SI_PD_L	47	PD*
SI_HPD	44	EDGE/HTPLG

U58 SIL1162 TSSOP

GPU_DVOD<0>	18	D0
GPU_DVOD<1>	17	D1
GPU_DVOD<2>	16	D2
GPU_DVOD<3>	15	D3
GPU_DVOD<4>	14	D4
GPU_DVOD<5>	13	D5
GPU_DVOD<6>	10	D6
GPU_DVOD<7>	9	D7
GPU_DVOD<8>	8	D8
GPU_DVOD<9>	7	D9
GPU_DVOD<10>	6	D10
GPU_DVOD<11>	5	D11
GPU_DVOD_DE	19	DE
GPU_DVO_HSYNC	20	HSYNC
GPU_DVO_VSYNC	21	VSYNC
GPU_DVO_CLKP	12	IDCK+
SI_VREF_IDCK_N	11	IDCK-

	28	PVCC1
	46	PVCC2
	40	AVCC
	34	AVCC
	22	VCC
	3	VCC
	45	PGND
	42	PGND
	31	AGND
	43	AGND
	37	AGND
	1	GND
	23	GND
	4	GND
	49	THRMPAD

SI_MSEN	48	MSEN
SI_TMDS_CLKP	33	TXC+
SI_TMDS_CLKN	32	TXC-
SI_TMDS_DP<0>	36	TX0+
SI_TMDS_DN<0>	35	TX0-
SI_TMDS_DP<1>	39	TX1+
SI_TMDS_DN<1>	38	TX1-
SI_TMDS_DP<2>	42	TX2+
SI_TMDS_DN<2>	41	TX2-
SI_EXT_SWING_SET	30	EXT_SWING
SI_VREF_IDCK_N	2	VREF

(SET TO LOW SWING MODE)

+1.8V GPU

R838 1K 1% 1/16W MF 402 — EXT_TMDS
R839 1K 1% 1/16W MF 402 — EXT_TMDS

Place C879 close to SI pin#2

C879 0.1uF 20% 10V CERM 402

RP49 0K EXT_TMDS
RP51 0K EXT_TMDS
RP50 0K EXT_TMDS
RP60 0K EXT_TMDS

ATI_DVOD<1>	GPU_DVOD<1>	
ATI_DVOD<0>	GPU_DVOD<0>	
ATI_DVOD<3>	GPU_DVOD<3>	
ATI_DVOD<2>	GPU_DVOD<2>	
ATI_DVOD<10>	GPU_DVOD<10>	
ATI_DVOD<11>	GPU_DVOD<11>	
ATI_DVOD<8>	GPU_DVOD<8>	
ATI_DVOD<9>	GPU_DVOD<9>	
ATI_DVOD<7>	GPU_DVOD<7>	
ATI_DVOD<6>	GPU_DVOD<6>	
ATI_DVOD<5>	GPU_DVOD<5>	
ATI_DVOD<4>	GPU_DVOD<4>	
ATI_DVO_HSYNC	GPU_DVO_HSYNC	
ATI_DVO_VSYNC	GPU_DVO_VSYNC	
ATI_DVOD_DE	GPU_DVOD_DE	
ATI_DVO_CLKP	GPU_DVO_CLKP	

27M OSC

(PLACE THE OSCILLATOR AND R304 AND R305 CLOSE TO ATI PIN AJ29)

+3V_SLEEP — L16 FERR-EMI-100-OHM (SM)

R304 100K 5% 1/16W MF 402 — NO STUFF

G1 27MHZ OSC SM — CRITICAL — VCC / OE / OUT / GND — ATI_OSC_OE — +3V_ATI_OSC_SLEEP

C409 0.1uF 20% 10V CERM 402
C401 4.7uF 20% 6.3V CERM 805

R305 0 5% 1/16W MF 402 — ATI_CLK27M_OSC_SS

R315 287 1% 1/16W MF 402 — ATI_CLK27M_IN — (PLACE R315 CLOSE TO OSC)

R320 162 1% 1/16W MF 402

SPREAD SPECTRUM SUPPORT

S0=1;S1=M => -1.5% DOWN-SPREAD

+3V_SLEEP — L66 FERR-EMI-100-OHM (SM) — GPU_SS

C384 10uF 20% 6.3V CERM 805
C390 0.1uF 20% 10V CERM 402 — +3V_ATI_SS

R289 0 5% 1/16W MF 402 — NO STUFF
R297 0 5% 1/16W MF 402 — ATI_CLK27M_OSC_SS

R290 0 5% 1/16W MF 402 — NO STUFF
R298 0 5% 1/16W MF 402

VDD U30 CY25811 SOIC — CRITICAL — GPU_SS

XIN/CLKIN	1	
XOUT	8	
NC		
NC	6	
FRSEL		
S1	3	CY25811_S1
S0	4	CY25811_S0
SSCLK	5	ATI_SSCLK_UF
VSS	2	

R285 33 5% 1/16W MF 402 — ATI_SSCLK_IN

M10 AGP INTERFACE

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SIZE	DRAWING NUMBER	REV.
D	401243	AA
SCALE: NONE	SHT 19 OF 44	

Int.TMDS Termination

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN
CMF LINE SHOULD BE ROUTED AS 4MIL SURFACE
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS

GPU_TMDS_CLK_CMF
R374 162 1% 1/16W MF 402 — GPU_TMDS_CLK#
R377 162 1% 1/16W MF 402 — GPU_TMDS_CLK
C536 470pF 10% 50V CERM 402
C522 470pF 10% 50V CERM 402

GPU_TMDS_D0_CMF
R367 162 1% 1/16W MF 402 — GPU_TMDS_D0#
R369 162 1% 1/16W MF 402 — GPU_TMDS_D0
C515 470pF 10% 50V CERM 402
C507 470pF 10% 50V CERM 402

GPU_TMDS_D1_CMF
R362 162 1% 1/16W MF 402 — GPU_TMDS_D1#
R355 162 1% 1/16W MF 402 — GPU_TMDS_D1
C487 470pF 10% 50V CERM 402
C497 470pF 10% 50V CERM 402

GPU_TMDS_D2_CMF
R350 162 1% 1/16W MF 402 — GPU_TMDS_D2#
R340 162 1% 1/16W MF 402 — GPU_TMDS_D2
C479 470pF 10% 50V CERM 402
C469 470pF 10% 50V CERM 402

R765 10 5% 1/16W MF 402 — GPU_TMDS_CLK#
R760 10 5% 1/16W MF 402 — GPU_TMDS_D0#
R762 10 5% 1/16W MF 402 — GPU_TMDS_D1#
R764 10 5% 1/16W MF 402 — GPU_TMDS_D2#
R766 10 5% 1/16W MF 402 — GPU_TMDS_CLK
R761 10 5% 1/16W MF 402 — GPU_TMDS_D0
R763 10 5% 1/16W MF 402 — GPU_TMDS_D1
R767 10 5% 1/16W MF 402 — GPU_TMDS_D2

Place all TMDS 10 ohms close to GPU

R389 10K 5% 1/16W MF 402 — +1_8V_GPU
R840 10K 5% 1/16W MF 402 — +3V_GPU
R378 1K 5% 1/16W MF 402
R380 10K 5% 1/16W MF 402 — NO STUFF
R351 1K 5% 1/16W MF 402 — ATI_TESTEN

U47 RAGE_MOBILITY M10-CSP64 64MB BGA (3 OF 6)

ROMCSB	AE5	NC
R	AK28	GPU_R
G	AK27	GPU_G
B	AK26	GPU_B
VSYNC	AG27	ATI_VSYNC
V2SYNC	AG25	NC
HSYNC	AG26	ATI_HSYNC
H2SYNC	AG24	NC
RSET	AK25	ATI_RSET
R2SET	AJ24	ATI_R2SET
Y_G	AK23	GPU_Y
C_R	AK24	GPU_C
COMP_B	AK22	GPU_COMP
DIGON	AE13	FP_PWR_EN
BLON	AF13	INV_ON_PWM
HPD1	AF11	GPU_HPD
AUXWIN	AJ27	AUXWIN_PU
DDC1DATA	AH28	GPU_DVI_DDC_DATA
DDC1CLK	AH27	GPU_DVI_DDC_CLK
DDC2DATA	AE12	LVDS_DDC_DATA
DDC2CLK	AF12	LVDS_DDC_CLK
DDC3DATA	AH26	SI_I2S_DATA
DDC3CLK	AH25	SI_I2C_CLK
TXOUT_U0N	AH18	LVDS_U0N
TXOUT_U0P	AG18	LVDS_U0P
TXOUT_U1N	AH19	LVDS_U1N
TXOUT_U1P	AG19	LVDS_U1P
TXOUT_U2N	AH20	LVDS_U2N
TXOUT_U2P	AG20	LVDS_U2P
TXOUT_U3N	AH22	LVDS_U3N_TP (NO ICT TEST)
TXOUT_U3P	AG22	LVDS_U3P_TP (NO ICT TEST)
TXCLK_UN	AH21	CLKLVDS_UN
TXCLK_UP	AG21	CLKLVDS_UP
TXOUT_L0N	AK16	LVDS_L0N
TXOUT_L0P	AJ16	LVDS_L0P
TXOUT_L1N	AK17	LVDS_L1N
TXOUT_L1P	AJ17	LVDS_L1P
TXOUT_L2N	AK18	LVDS_L2N
TXOUT_L2P	AJ18	LVDS_L2P
TXOUT_L3N	AK20	LVDS_L3N_TP (NO ICT TEST)
TXOUT_L3P	AJ20	LVDS_L3P_TP (NO ICT TEST)
TXCLK_LN	AK19	CLKLVDS_LN
TXCLK_LP	AJ19	CLKLVDS_LP
SSOUT	AJ25	NC
VSS	A20	
VSS	B21	

ATI_DVOD<0>	AJ5	ZV_LCDDATA0
ATI_DVOD<1>	AK5	ZV_LCDDATA1
ATI_DVOD<2>	AG6	ZV_LCDDATA2
ATI_DVOD<3>	AH6	ZV_LCDDATA3
ATI_DVOD<4>	AJ6	ZV_LCDDATA4
ATI_DVOD<5>	AK6	ZV_LCDDATA5
ATI_DVOD<6>	AG7	ZV_LCDDATA6
ATI_DVOD<7>	AH7	ZV_LCDDATA7
ATI_DVOD<8>	AJ7	ZV_LCDDATA8
ATI_DVOD<9>	AK7	ZV_LCDDATA9
ATI_DVOD<10>	AG8	ZV_LCDDATA10
ATI_DVOD<11>	AH8	ZV_LCDDATA11
NC	AJ8	ZV_LCDDATA12
NC	AK8	ZV_LCDDATA13
NC	AG9	ZV_LCDDATA14
NC	AH9	ZV_LCDDATA15
NC	AJ9	ZV_LCDDATA16
NC	AK9	ZV_LCDDATA17
NC	AG10	ZV_LCDDATA18
NC	AH10	ZV_LCDDATA19
ZV_LCDDATA20_PU	AJ10	ZV_LCDDATA20
NC	AK10	ZV_LCDDATA21
NC	AG11	ZV_LCDDATA22
NC	AH11	ZV_LCDDATA23
ATI_DVO_VSYNC	AJ4	ZV_LCDCNTL0
ATI_DVO_HSYNC	AK4	ZV_LCDCNTL1
ATI_DVOD_DE	AH5	ZV_LCDCNTL2
ATI_DVO_CLKP	AG5	ZV_LCDCNTL3
ATI_AGP_FBSKEW<0>	AJ2	GPIO0
ATI_AGP_FBSKEW<1>	AK2	GPIO1
ATI_X1CLK_SKEW<0>	AK1	GPIO2
ATI_X1CLK_SKEW<1>	AH3	GPIO3
ATI_BUS_CFG<0>	AH2	GPIO4
ATI_BUS_CFG<1>	AJ1	GPIO5
ATI_BUS_CFG<2>	AF4	GPIO6
ATI_GPIO7_SPN	AH1	GPIO7
ATI_GPIO8_PD	AG3	GPIO8
ATI_GPIO9_SPN	AF3	GPIO9
ATI_GPIO10_SPN	AG2	GPIO10
ATI_GPIO11_SPN	AF2	GPIO11
ATI_GPIO12_SPN	AG1	GPIO12
ATI_GPIO13_SPN	AF1	GPIO13
HPD_PWR_SNS_EN	AE2	GPIO14
GPU_VCORE_CNTL_L	AE1	GPIO15
ATI_SSCLK_IN	M1	GPIO16
ATI_TMDS_DN<0>	AJ13	TX0M
ATI_TMDS_DP<0>	AK13	TX0P
ATI_TMDS_DN<1>	AJ14	TX1M
ATI_TMDS_DP<1>	AK14	TX1P
ATI_TMDS_DN<2>	AJ15	TX2M
ATI_TMDS_DP<2>	AK15	TX2P
ATI_TMDS_CLKN	AJ12	TXCM
ATI_TMDS_CLKP	AK12	TXCP
ATI_CLK27M_IN	AJ29	XTALIN
NC	AJ30	XTALOUT
ATI_TESTEN	AH24	TESTEN
NC	AJ26	SSIN
	B24	VSS
	B20	VSS
	A24	VSS

Q23 SI3446DV TSOP

+1_5V_AGP → pin 1; pin 3 → GPU_CORE_OK; pin 4 → +GPU_VDD15_UF

L17 FERR-220-OHM 0805 (500mA)

+1_5V_GPU_VDD15 → +GPU_VDD15_UF

C407 1000pF 10% 25V X7R 402

U47 RAGE_MOBILITY M10-CSP64 64MB BGA (5 OF 6)

VDD15	F12	G7
	L6	G8
	T6	G9
	AB6	G10
	F17	G11
	G25	G12
	R25	G13
	AB25	G14
	AJ3	G15
	AF25	G16
	AG4	G17
	AH4	G18
	AF5	G19
	F6	G20
	G6	G21
	H6	G22
	P6	G23
	AD26	G24
	V6	H7
	W6	H8
	AC6	H23
	AD6	H24
	AE6	J7
	F7	J24
VDDC	F10	K7
	AE10	K24
	F11	L7
	AE11	L24
	F13	M7
	F14	M24
	AE14	N7
	AF14	N24
	W26	P7
	AF15	P24
	AE17	R7
	AC25	R24
	AE18	T7
	F23	T24
	F24	U7
	AE24	U24
	F25	V7
	M25	V24
	N25	W7
VSS	W25	W24
	V25	Y7
		Y24
		AA7
		AA24
		AB7
		AB24
		AC7
		AC8
		AC23
		AC24
		AD7
		AD8
		AD9
		AD10
		AD11
		AD12
		AD13
		AD14
		AD15
		AD16
		AD17
		AD18
		AD19
		AD20
		AD21
		AD22
		AD23

GPU VCORE - 1.2V

(PUT ALL CAPs BELOW ATI ASIC)

C448 C443 C435 C482 C411 0.01uF 20% 16V CERM 402; C411 10uF 20% 6.3V CERM 805
C505 C532 C529 C526 0.01uF 20% 16V CERM 402
C484 C485 10uF 20% 6.3V CERM 805
C440 C441 C445 C446 C449 C434 0.22uF 20% 6.3V CERM 402
C452 C451 C494 C498 C509 C510 C512 C513 0.22uF 20% 6.3V CERM 402
C524 C525 C528 C531 C533 C477 C486 C495 0.22uF 20% 6.3V CERM 402

R332 715 1% 1/16W MF 402 — GPU_VCORE
R333 499 1% 1/16W MF 402
R359 R356 R360 75 1% 1/16W MF 402

M10 Power Shut down Sequencing

XW11 SM — +1_8V_ATI_PVDD → DP5 BAS16TW SOT-363 → +2_5V_SLEEP_NECK1 → XW9 SM → +2_5V_SLEEP
XW12 SM — GPU_VCORE → DP5 BAS16TW SOT-363 → +1_5V_AGP_NECK → XW4 SM → +1_5V_AGP
XW5 SM — +GPU_VDD15_UF → DP5 BAS16TW SOT-363 → +GPU_VDD15_NECK

R384 R387 10K 5% 1/16W MF 402
R386 R382 R383 R385 R381 10K 5% 1/16W MF 402 — NO STUFF
R393 R396 R395 R391 R392 R394 R390 10K 5% 1/16W MF 402 — NO STUFF

(GPIO0) ATI_AGP_FBSKEW<0>
(GPIO1) ATI_AGP_FBSKEW<1>
(GPIO2) ATI_X1CLK_SKEW<0>
(GPIO3) ATI_X1CLK_SKEW<1>
(GPIO4) ATI_BUS_CFG<0>
(GPIO5) ATI_BUS_CFG<1>
(GPIO6) ATI_BUS_CFG<2>

GPU VCORE SUPPLY

WHEN VCORE_CNTL HIGH => 1.2V
1.2V = 0.8V * (1 + R329 / (R328//R330))

WHEN VCORE_CNTL LOW => 1.0V
1.0V = 0.8V * (1 + R329 / R330)

+PBUS
C706 C708 4.7uF 20% 25V CERM 1206
R327 1M 5% 1/16W MF 402
R331 1 5% 1/16W MF 603
R326 576K 1% 1/16W MF 402
Q48 SI7860DP SO-8-PWRPK
L64 2.1uH-11A SM
D12 1N914 SOT23
R358 2.2 5% 1/16W MF 603
C481 0.1uF 20% 25V CERM 603
D29 SM MBRS130LT3
Q49 IRF7832 SO-8
C704 22uF 20% 10V CERM 1210
C705 C711 330uF 20% 6.3V TANT CASE-D4
C707 330uF 20% 6.3V TANT CASE-D4
R329 4.99K 1% 1/16W MF 402
R328 18.2K 1% 1/16W MF 402
R330 20K 1% 1/16W MF 402
R361 1.82K 1% 1/16W MF 402
R786 100K 5% 1/16W MF 402
C846 0.1uF 20% 10V CERM 402
Q25 2N7002DW SOT-363
R549 10K 5% 1/16W MF 402
C712 0.1uF 20% 10V CERM 402
R343 0 5% 1/16W MF 402
R352 63.4K 1% 1/16W MF 402 — NO STUFF
C466 4.7uF 20% 10V CERM 1206
R357 100K 5% 1/16W MF 402
R344 R353 0 5% 1/16W MF 402 — NO STUFF
C465 220pF 5% 25V CERM 402
C455 470pF 10% 50V CERM 402
C480 0.1uF 20% 10V CERM 402
C838 0.001uF 20% 50V CERM 402 — NO STUFF
C431 0.1uF 20% 25V CERM 603
R339 20K 1% 1/16W MF 402
XW6 SM — OMIT
XW19 JUMPER OPEN — OMIT

U32 LTC1778 SSOP — CRITICAL
EXT VIN VCC VCC
RUN/SS ITH VRNG FCB PGOND SGND PGND
ION BOOST TG SW BG VFB

R559 R556 100K 5% 1/16W MF 402
DP7 BAS16TW SOT-363
R558 10K 5% 1/16W MF 402
R555 33K 5% 1/16W MF 402
Q51 2N3904 SM
Q52 2N3904 SM

GPU_VCORE_PWR_SEQ
GPU_VCORE_SEQ_L
GPU_VCORE_SEQ
SLEEP_L_LS5
DCDC_EN

1778_GND
1778_SHDN_L
1778_ITH_RC
1778_VCC
1778_VIN
1778_ION
1778_BST
1778_TG
1778_BG
1778_VFB
1778_ITH
1778_VRNG
1778_FCB
GPU_CORE_OK
1778_BST_RC
GPU_VCORE_SW
GPU_VCORE_SW_F
GPU_VCORE_CNTL_L
GPU_VCORE_CNTL_RC
GPU_VCORE_CNTL
HIGH_VCORE_DIV
HIGH_VCORE

M10 CORE PWR/LVDS/TMDS

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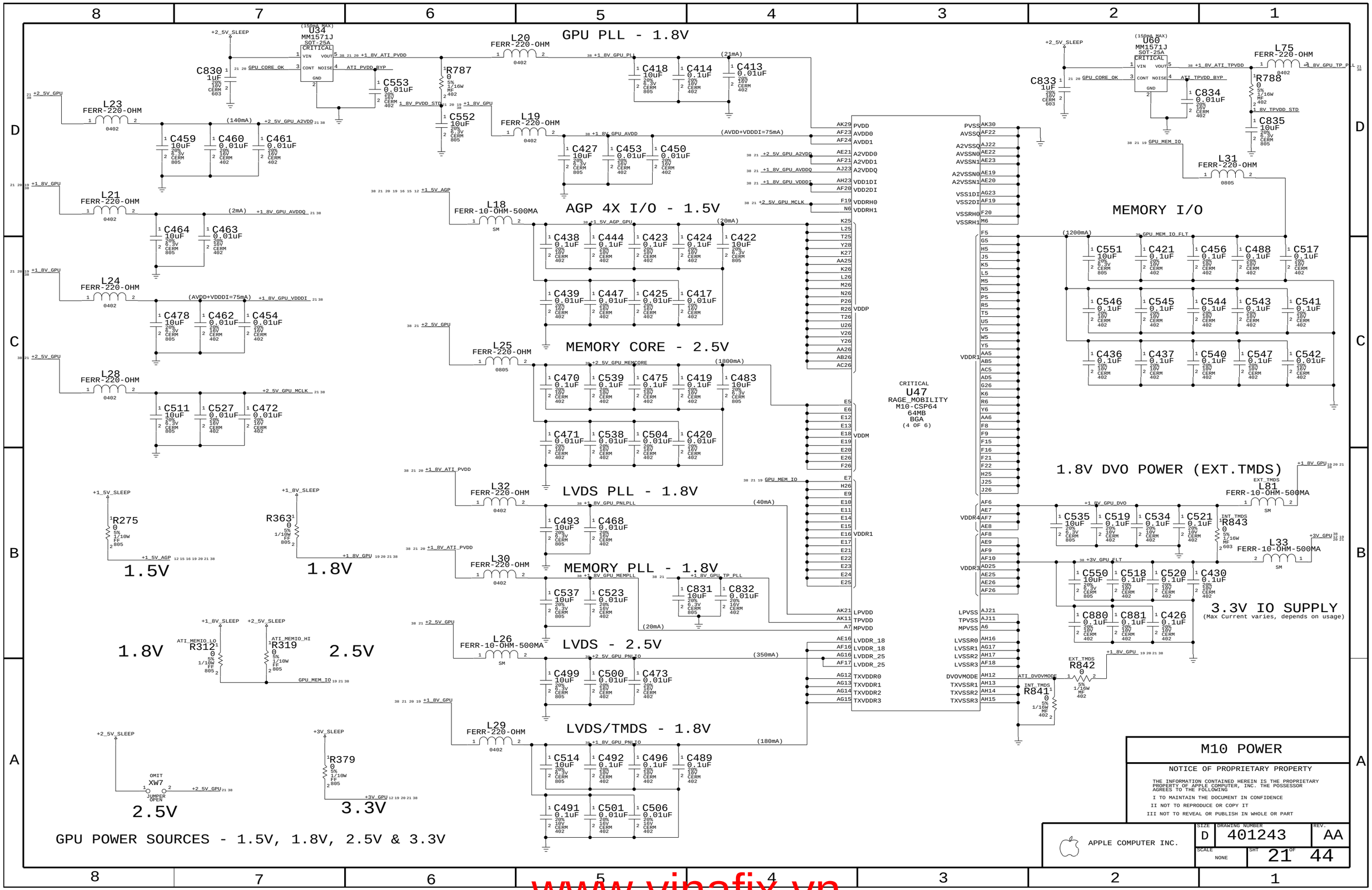
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401243	AA
SCALE: NONE	SHT 20 OF 44	



EXTERNAL VIDEO (DVI) INTERFACE

VGA SYNC BUFFERS

+3V_MAIN

U40 74AHC1G32 SM

ATI_VSYNC → ATI_VSYNC_BUF → L38 OMIT FERR-60-OHM-0.1A 0402 → VGA_VSYNC 22 39

U39 74AHC1G32 SM

ATI_HSYNC → ATI_HSYNC_BUF → L36 OMIT FERR-60-OHM-0.1A 0402 → VGA_HSYNC 22 39

PLACE L1002 & L1003 CLOSE TO DVI CONNECTOR

TMDS FILTERING
PLACE CLOSE TO CONNECTOR

L45 CRITICAL 90-OHM-200MA SM
L46 CRITICAL 90-OHM-200MA SM SYM_VER-1
L47 CRITICAL 90-OHM-200MA SM SYM_VER-1

TMDS_DN<0> → TMDS_CONN_DN<0>
TMDS_DP<0> → TMDS_CONN_DP<0>
TMDS_DN<1> → TMDS_CONN_DN<1>
TMDS_DP<1> → TMDS_CONN_DP<1>
TMDS_DN<2> → TMDS_CONN_DN<2>
TMDS_DP<2> → TMDS_CONN_DP<2>

(TMDS_DN<5>) NC
(TMDS_DP<5>) NC
(TMDS_DN<4>)
(TMDS_DP<4>)
(TMDS_DN<3>)
(TMDS_DP<3>)

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

L37 370-OHM SM SYM_VER-1

TMDS_CLKP → TMDS_CONN_CLKP
TMDS_CLKN → TMDS_CONN_CLKN

L50 0.068uH SM — GPU_B → GPU_B_FILTR → VGA_B 22 39
L49 0.068uH SM
C642 4.7pF 5% 50V CERM 402
C641 3.3pF 0.25% 50V CERM 402
R462 75 1% 1/16W MF 402

L44 0.068uH SM — GPU_G → GPU_G_FILTR → VGA_G 22 39
L43 0.068uH SM
C635 4.7pF 5% 50V CERM 402
C634 3.3pF 0.25% 50V CERM 402
R458 75 1% 1/16W MF 402

L41 0.068uH SM — GPU_R → GPU_R_FILTR → VGA_R 22 39
L40 0.068uH SM
C632 4.7pF 5% 50V CERM 402
C631 3.3pF 0.25% 50V CERM 402
R456 75 1% 1/16W MF 402

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)

+5V_SLEEP → F2 CRITICAL 0.5AMP-13.2V SM → +5V_DDC_SLEEP_UF 38 → L42 400-OHM-EMI SM-1 → +5V_DDC_SLEEP 22 38 39

Isolation required for DVI power switch

D19 SM MBR0530 — DDC_CLK_ISO
R476 4.7K 5% 1/16W MF 402
R478 4.7K 5% 1/16W MF 402

J22 CRITICAL QH112 F-RT-TH — CHGND1

R479 100 5% 1/16W MF 402 — DVI_DDC_CLK
R477 100 5% 1/16W MF 402 — DVI_DDC_DATA
R469 100 5% 1/16W MF 402 — DVI_HPD

C654 100pF 5% 25V CERM 201
C655 100pF 5% 25V CERM 201
C667 0.01uF 20% 50V CERM 603
C653 100pF 5% 25V CERM 201

DVI_DDC_CLK_UF 39 22
(+5V_DDC_SLEEP)
DVI_DDC_DATA_UF 39
DVI_HPD_UF 39 22
VGA_VSYNC 22 39
VGA_R 22 39
VGA_G 22 39

PLACE NEAR C5A & C5B
R464 0 5% 1/16W MF 402

R463 0 5% 1/16W MF 402
PLACE NEAR 3, 11 & 19

CHGND1 CHGND2

3V LEVEL SHIFTERS

+3V_SLEEP

Q39 2N7002DW SOT-363
Q39 2N7002DW SOT-363
Q40 2N7002DW SOT-363

R480 10K 5% 1/16W MF 402 — GPU_DVI_DDC_CLK
R474 10K 5% 1/16W MF 402 — GPU_DVI_DDC_DATA
R481 100K 5% 1/16W MF 402 — GPU_HPD

NOTE: Pulldown for DVI_HPD provided by DVI power switch interface

DVI POWER SWITCH

Power key detect path when system is shutdown or asleep.. DDC_CLK is isolated from NV17M DURING SHUTDOWN. WHEN power key on remote device is pressed, 5V will be driven into DDC_CLK. Since host rails will be low, TP0610 will turn on, driving SOFT_PWR_ON_L low. As host rails rise, TP0610 will turn off, as will remote device path into DDC_CLK. Isolation will be disabled as well.

Q38 TP0610 SM
DVI_DDC_CLK_UF → DVI_TURN_ON
+5V_DDC_SLEEP

R473 680 5% 1/16W MF 402 — DVI_TURN_ON_ILIM
R459 330 5% 1/16W MF 402 — Pulldown prevents 3904 from turning on when DVI monitor has active, self-powered DDC clock pullup.
R460 10K 5% 1/16W MF 402
DVI_TURN_ON_BASE
Q35 MMDT3904 SOT-363 — SOFT_PWR_ON_L 23 29 33 39

Power key detect path when system is running. HPD normally driven to 3.3V. When power key on remote device pressed, HPD will be driven to 5V. COMPARATOR ENABLED BY NV17MAP GPIO.

+3V_SLEEP
R485 68.1K 1% 1/16W MF 402
C668 0.1uF 20% 10V CERM 402
U42 LMC7211 SM
HPD_4V_REF
HPD_PWR_SW_BASE
R475 10K 5% 1/16W MF 402
Q35 MMDT3904 SOT-363
DVI_HPD_UF 39 22 → R472 10K 1% 1/16W MF 402 → DVI_HPD_DIV
R484 100K 1% 1/16W MF 402
R482 10K 1% 1/16W MF 402
HPD_PWR_SW
R470 330 5% 1/16W MF 402
HPD_REF_EN_L
Q40 2N7002DW SOT-363
HPD_PWR_SNS_EN 20 → R483 470K 5% 1/16W MF 402

INVERTER INTERFACE

+PBUS
L73 FERR-1K-OHM-EMI SM — +14V_INV
+5V_MAIN
Q76 FDG6324L SC70-6
+5V_INV_UF_SW 38
L74 400-OHM-EMI SM-1
R750 100K 5% 1/16W MF 402 — FP_PWR_EN_L
C812 0.001uF 20% 50V CERM 402
C813 10uF 20% 6.3V CERM 805
+5V_INV_SW 39 38
J4 SM-2MT CRITICAL
Q76 FDG6324L SC70-6
FP_PWR_EN 22 20
L72 400-OHM-EMI SM-1 — BRIGHT_PWM 39 38
C815 0.001uF 20% 50V CERM 402
+3V_MAIN
C816 0.001uF 20% 50V CERM 402
C19 0.001uF 20% 50V CERM 402
INV_GND 39
L1 FERR-250-OHM SM
C22 0.1uF 20% 10V CERM 402
INV_ON_PWM 20 → U2 NC7S32 SC70 → BRIGHT_PWM_UF
INVERTER EXPECTS ACTIVE HIGH SIGNAL
CHGND3

S-VIDEO/COMP OUT INTERFACE

Place GND shorts at graphics controller

XW15 SM — GPU_TV_GND1 38 → L54 FERR-10-OHM-500MA SM → TV_GND1 38 39

L53 3.3uH 0603 — GPU_Y 20 → TV_Y 39
C657 0.01uF 20% 50V CERM 603
C663 560pF 10% 50V CERM 402
C656 560pF 10% 50V CERM 402

L57 3.3uH 0603 — GPU_C 20 → TV_C 39
C661 560pF 10% 50V CERM 402
C660 560pF 10% 50V CERM 402

L55 3.3uH 0603 — GPU_COMP 20 → TV_COMP 39
C664 560pF 10% 50V CERM 402
C658 560pF 10% 50V CERM 402

J21 CRITICAL MINIDIN RT-TH MH11773-WMR8A — CHGND1

XW14 SM — GPU_TV_GND2 38 → L56 FERR-10-OHM-500MA SM → TV_GND2 38 39
C659 0.01uF 20% 50V CERM 603 — CHGND1

Place GND shorts at graphics controller

LCD INTERFACE

LVDS INTERFACE

LCD POWER SWITCH

+3V_MAIN
R347 100K 5% 1/16W MF 402
C474 2200pF 5% 50V CERM 603
R354 100K 5% 1/16W MF 402 — LCD_PWREN_L
+3V_LCD_SW 38
L27 FERR-250-OHM SM — +3V_LCD (LVDS DDC POWER) 39 38
C503 0.001uF 20% 50V CERM 402 — CHGND4
TSOP SI3443DV Q29
LCD_DIGON_L
Q28 2N7002 SM — FP_PWR_EN 22 20
+3V_SLEEP
R543 100K 5% 1/16W MF 402
R544 100K 5% 1/16W MF 402
C701 0.001uF 20% 50V CERM 402

100K pull-ups are for no-panel case (development) Panel has 2K pull-ups

NO STUFF
C702 0.001uF 20% 50V CERM 402

C548 0.001uF 20% 50V CERM 402 — CHGND4

J14 CRITICAL G-501973 F-RT-SM — CHGND4

LVDS_DDC_CLK	22 28 39
LVDS_DDC_DATA	22 28 39
LVDS_L0N	37 28 39
LVDS_L0P	37 28 39
LVDS_L1N	37 28 39
LVDS_L1P	37 28 39
LVDS_L2N	39 37 28
LVDS_L2P	39 37 28
CLKLVDS_LN	39 37 28
CLKLVDS_LP	39 37 28
LVDS_U0N	37 28 39
LVDS_U0P	37 28 39
LVDS_U1N	37 28 39
LVDS_U1P	37 28 39
LVDS_U2N	37 28 39
LVDS_U2P	37 28 39
CLKLVDS_UN	37 28 39
CLKLVDS_UP	37 28 39

LCD_DDC_CLK 20 22 39
LCD_DDC_DATA 20 22 39

C549 0.001uF 20% 50V CERM 402 — CHGND4

R753 0 5% 1/16W MF 402
C819 0.01uF 20% 50V CERM 603 — CHGND3

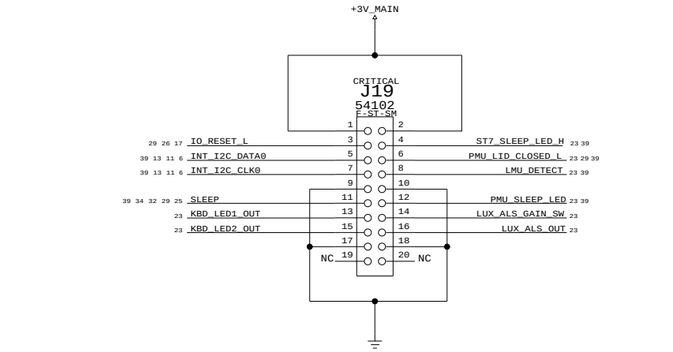
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S1331	2	DISCRETE,RES,33OHM,0402	L36,L38		VGA_BUFFER_RES

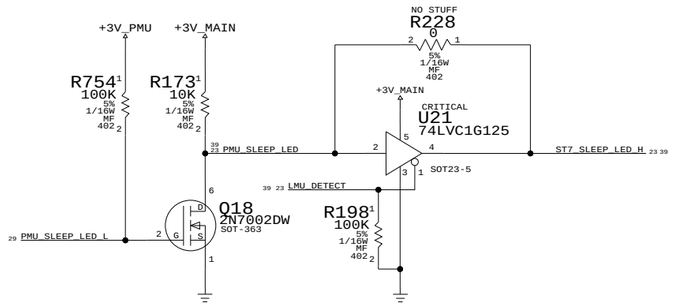
VIDEO CONNECTORS

APPLE COMPUTER INC.

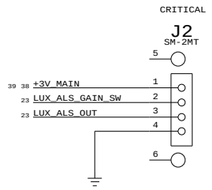
SIZE	DRAWING NUMBER	REV.
D	401243	AA
SCALE: NONE	SHT 22 OF 44	

LMU/RIGHT SENSOR CONNECTOR

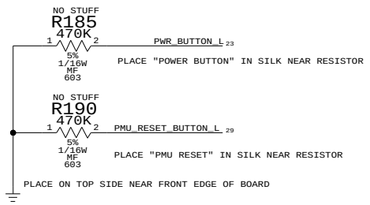




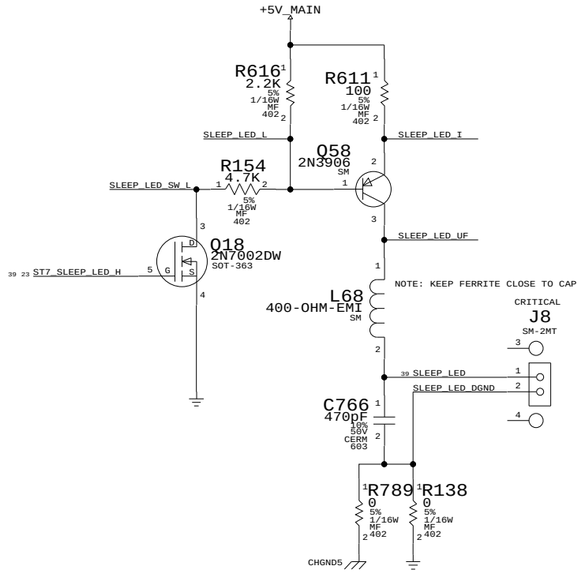
LEFT LIGHT SENSOR CONNECTOR



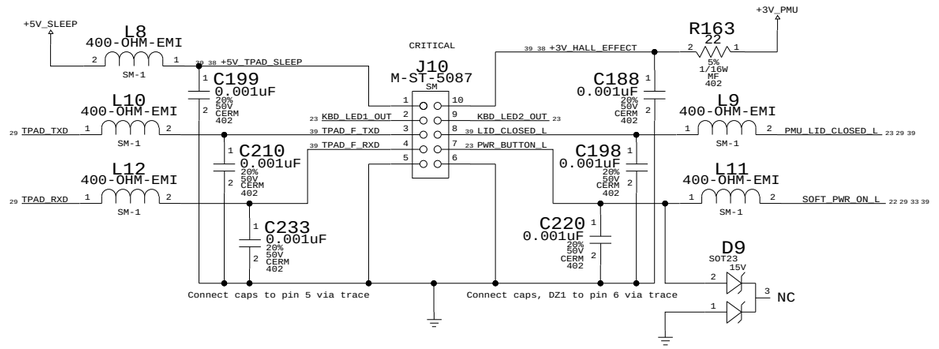
DEBUG HELPERS



SLEEP LED

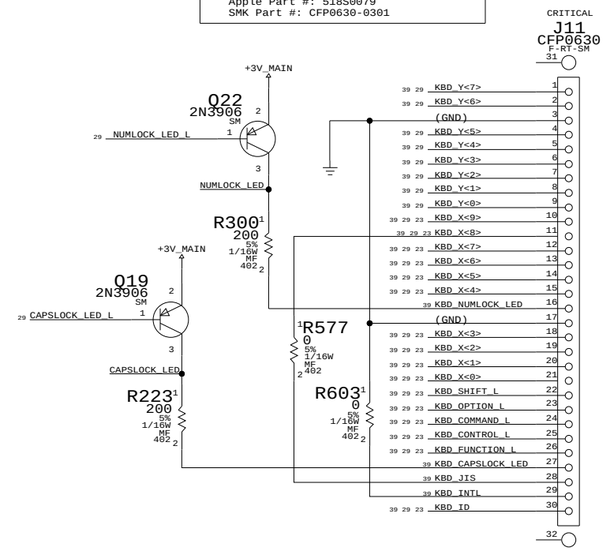


TRACKPAD/PWR BTN CONN

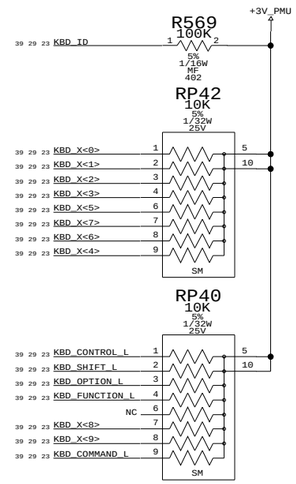


TOP CONTACT ZIF KEYBOARD CONN

CONN,TOP CONTACT ZIF,0.8MM PITCH,30P,SM
Apple Part #: 518S0079
SMK Part #: CFP0630-0301



KEYBOARD PULLUPS



KEYBOARD/TPAD/SLEEP LED

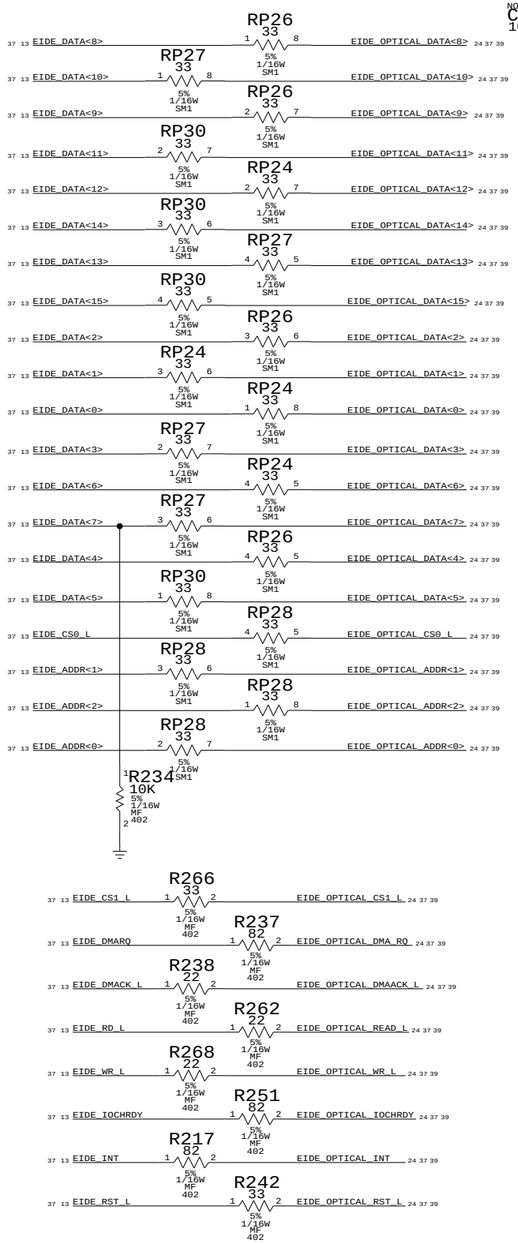
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401243	AA

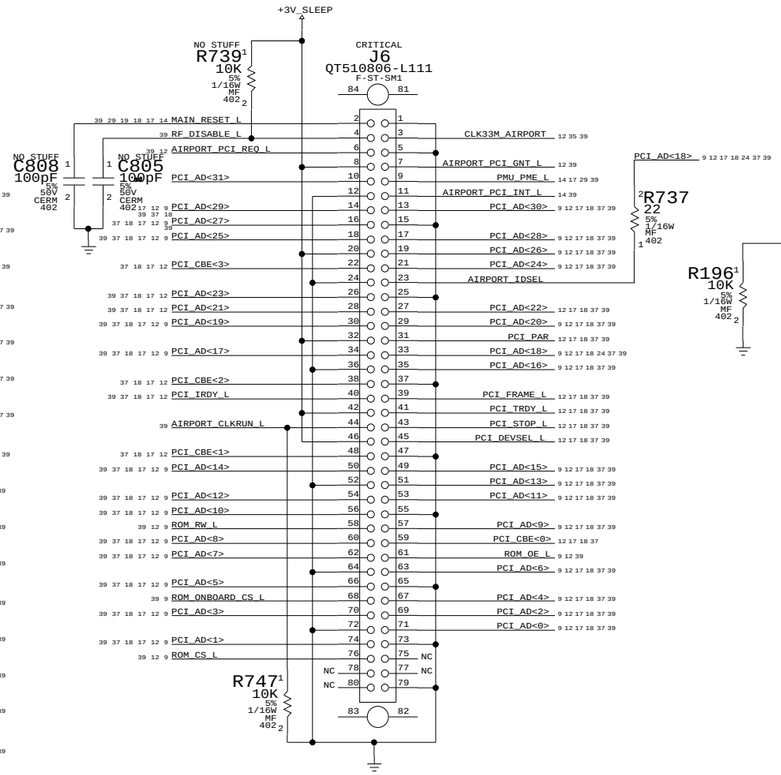
SCALE	SHT	OF
NONE	23	44

EIDE SERIES TERMINATION

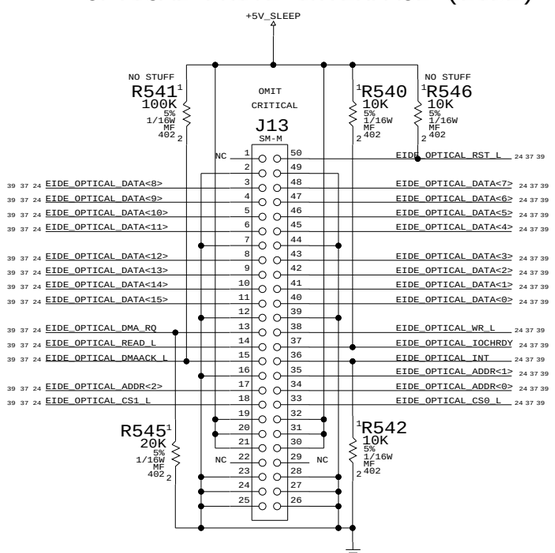
PLACE TERMINATORS NEAR INTREPID



WIRELESS INTERFACE

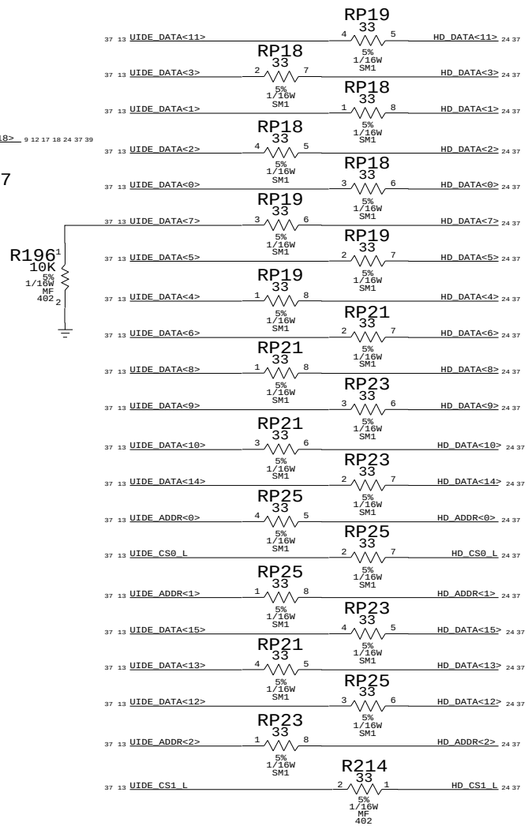


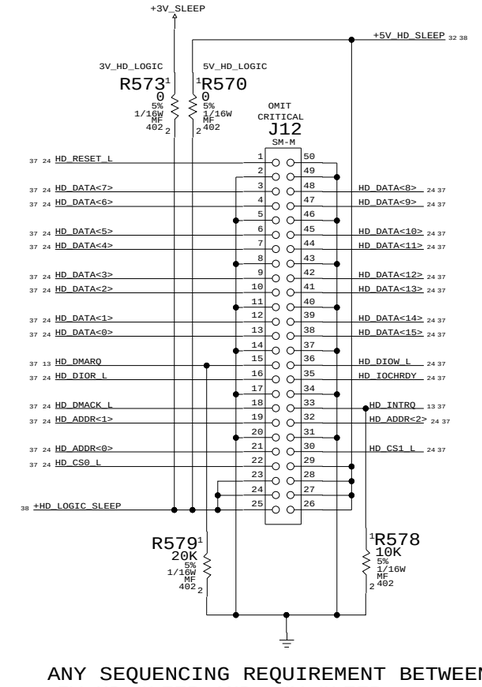
OPTICAL DRIVE INTERFACE (EIDE)



HARD DRIVE INTERFACE (UATA100)

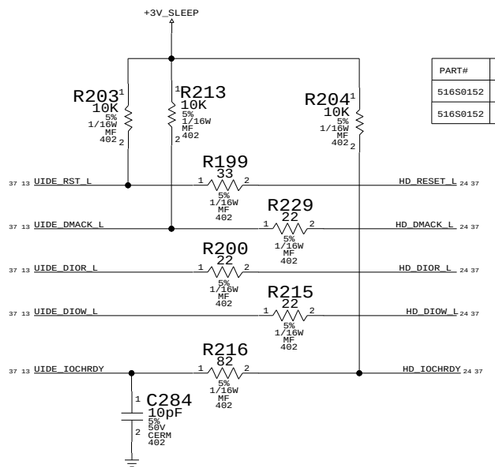
PLACE SERIES R CLOSE TO INTERPID





ANY SEQUENCING REQUIREMENT BETWEEN +5V_HD_SLEEP AND +3V_SLEEP

PLACE PULLUP RESISTORS CLOSE TO INTREPID



IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S0152	1	CONN,PLUG,0.5MM PITCH,1.5MM STACK,50P,GOLD	J12	CRITICAL	?
516S0152	1	CONN,PLUG,0.5MM PITCH,1.5MM STACK,50P,GOLD	J13	CRITICAL	?

INTERNAL I/O CONNECTORS

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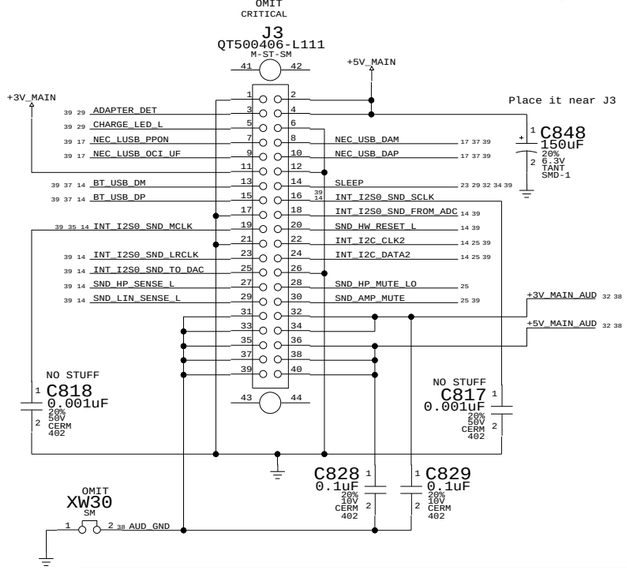
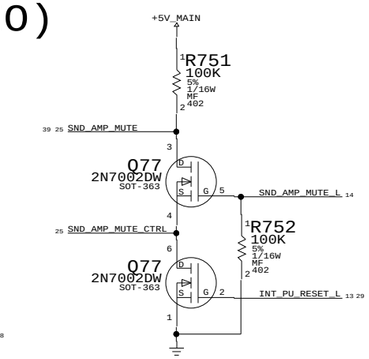
D	401243	AA
SCALE: NONE	SHT 24 OF 44	

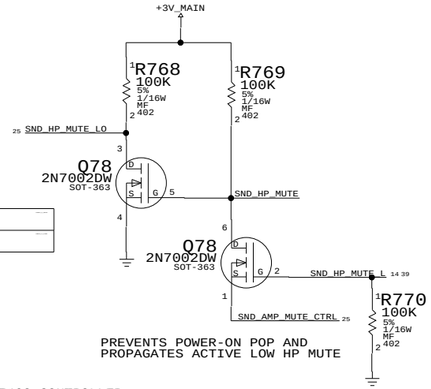
LEFT I/O & AUDIO BOARD (LIO)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S0154	1	CONN,PLUG,0.5MM PITCH,1.5MM STACK,40P,GOLD	J3	CRITICAL	?

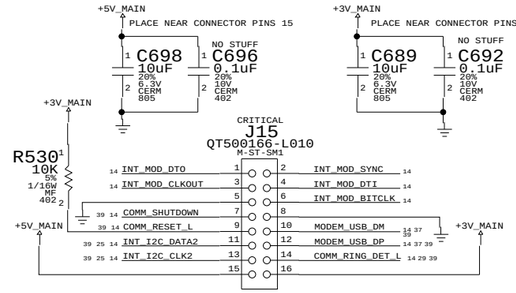


PREVENTS POWER-ON POP AND
GENERATES ACTIVE HIGH SPKR MUTE



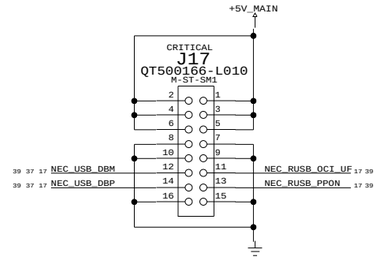
PREVENTS POWER-ON POP AND
PROPAGATES ACTIVE LOW HP MUTE

USB MODEM/SOFT MODEM

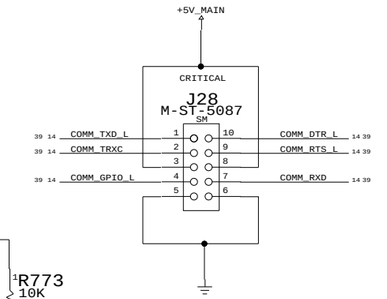


MODEM I2C ADDR ASSIGNED VIA FLEX CABLE

RIGHT USB BOARD

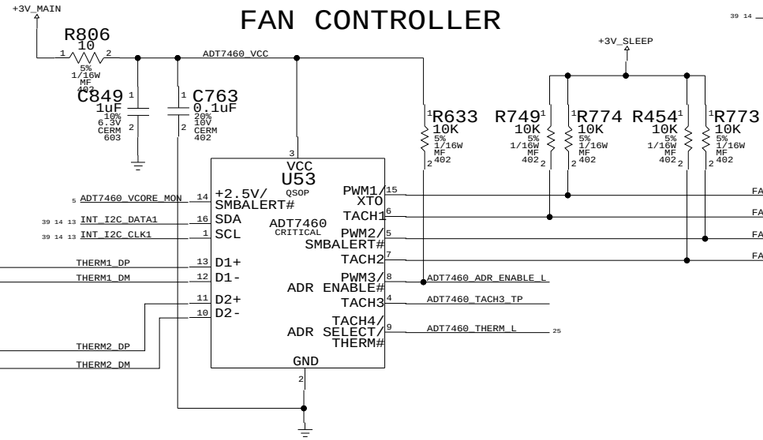


SERIAL DEBUG INTERFACE

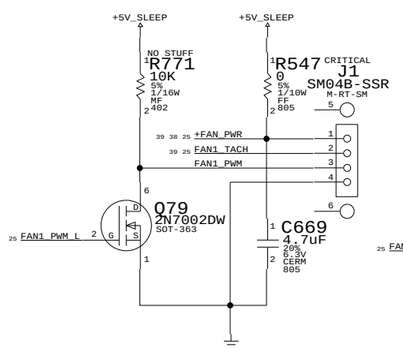


FAN INTERFACE

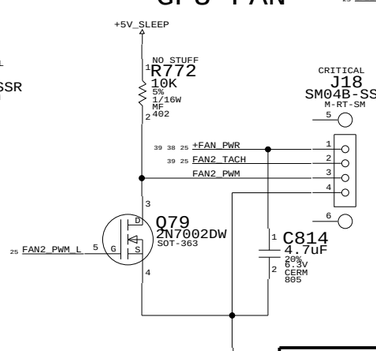
FAN CONTROLLER



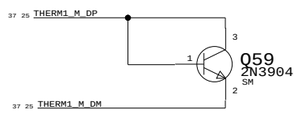
CPU FAN



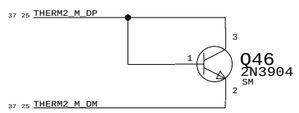
GPU FAN



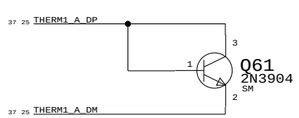
PLACE CLOSE TO CPU MAIN1



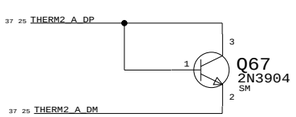
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY MAIN2



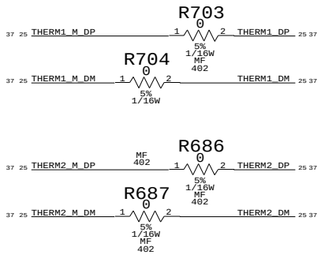
PLACE UNDERNEATH UPPER RAM ALTERNATE1



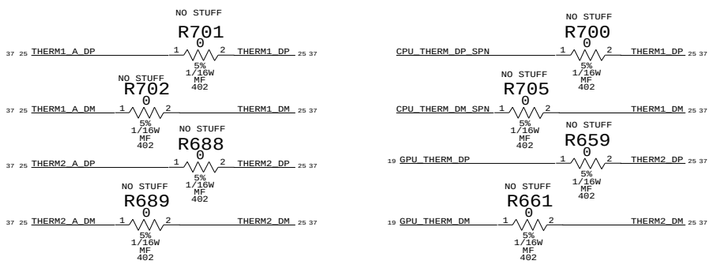
PLACE CLOSE TO BATTERY CHARGER/VCORE ALTERNATE2

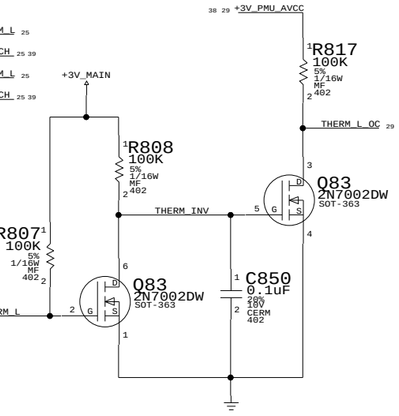


KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER



KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER





FAN/MODEM/SOUND/BACKUP BATT.

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401243	AA
SCALE: NONE	SHT 25 OF 44	

Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

+3V_MAIN

C680 10uF 20% 6.3V CERM 805

NO STUFF R513 0 5% 1/16W MF 402

3405_MODE

U45 LTC3405 SOT23-6 CRITICAL
VIN, RUN, MODE, GND, SW, VFB

LTC3405_SW

CRITICAL L60 3.3uH SM1

R507 0 5% 1/16W MF 402

R506 665K 1% 1/16W MF 402 R2A

C675 22pF 5% 50V CERM 402

R504 49.9K 1% 1/16W MF 402 R2B

3405_VFB

C674 10uF 20% 6.3V CERM 805

+1_0V_MARVELL

R503 182K 1% 1/16W MF 402 R1

VOUT = 0.8V*(1+R2EQV/R1)
R2EQV = R2A||R2B

PLACE ALL SERIES RES CLOSE TO PHY

R423 0 5% 1/16W MF 402 — CLKENET_LINK_TX → CLKENET_PHY_TX
R421 0 5% 1/16W MF 402 — CLKENET_LINK_RX → CLKENET_PHY_RX
R445 0 5% 1/16W MF 402 — CLKENET_LINK_GBE_REF → CLKENET_PHY_GBE_REF

NO STUFF C851 10pF 5% 50V CERM 402
C852 10pF 5% 50V CERM 402
Keep C851 & C852 Stubs short

CRITICAL U43 88E1111 BCC

TX_CLK	4	
RX_CLK	2	
125CLK	22	
TXD0	11	ENET_PHY_TXD<0>
TXD1	12	ENET_PHY_TXD<1>
TXD2	14	ENET_PHY_TXD<2>
TXD3	16	ENET_PHY_TXD<3>
TXD4	17	ENET_PHY_TXD<4>
TXD5	18	ENET_PHY_TXD<5>
TXD6	19	ENET_PHY_TXD<6>
TXD7	20	ENET_PHY_TXD<7>
TX_EN	9	ENET_PHY_TX_EN
TX_ER	7	ENET_PHY_TX_ER
GTX_CLK	8	CLKENET_PHY_GTX
RXD0	95	ENET_LINK_RXD<0>
RXD1	92	ENET_LINK_RXD<1>
RXD2	93	ENET_LINK_RXD<2>
RXD3	91	ENET_LINK_RXD<3>
RXD4	90	ENET_LINK_RXD<4>
RXD5	89	ENET_LINK_RXD<5>
RXD6	87	ENET_LINK_RXD<6>
RXD7	86	ENET_LINK_RXD<7>
RX_DV	94	ENET_RX_DV
RX_ER	3	ENET_RX_ER
CRS	84	ENET_CRS
COL	83	ENET_COL
MDC	25	ENET_MDC
MDIO	24	ENET_MDIO
INT-/INT+	23	ENET_ENERGY_DET
RESET	28	ENET_RST_L
COMA	27	ENET_COMA
S_IN+	82	NC
S_IN-	81	NC
S_OUT+	77	NC
S_OUT-	75	NC
S_CLK+	79	NC
S_CLK-	80	NC
HSDAC+	37	ENET_HSDACP
HSDAC-	38	ENET_HSDACM
XTAL1	55	CLK25M_ENET_XIN
XTAL2	54	CLK25M_ENET_XOUT
VSSC	53	ENET_VSSC
CTRL10	51	NC
DVDD	1, 6, 10, 15, 57, 62, 67, 71, 85	
VDDO	5, 21, 88, 96	
VDDOH	52, 66, 72	
VDDOX	26, 48	
AVDD	32, 35, 36, 40, 45, 78	
MDI0+	29	MDI_P<0>
MDI0-	31	MDI_M<0>
MDI1+	33	MDI_P<1>
MDI1-	34	MDI_M<1>
MDI2+	39	MDI_P<2>
MDI2-	41	MDI_M<2>
MDI3+	42	MDI_P<3>
MDI3-	43	MDI_M<3>
LED_LINK10	76	LED_LINK10
LED_LINK100	74	LED_LINK100
LED_LINK1000	73	NC
LED_DUPLEX	70	NC
LED_RX	69	LED_RX_SPN
LED_TX	68	NC
CONFIG0	65	(000)
CONFIG1	64	(000)
CONFIG2	63	(111)
CONFIG3	61	(110)
CONFIG4	60	(111)
CONFIG5	59	(101)
CONFIG6	58	(000)
TDI	44	JTAG_ENET_TDI
TDO	50	JTAG_ASIC_TDO_TP
TCK	49	JTAG_ASIC_TCK
TMS	46	JTAG_ASIC_TMS
TRST	47	JTAG_ASIC_TRST_L
RSET	30	ENET_RSET
SEL_OSC	56	NC
SEL_2.5V	13	
GND	97	

SEE CONFIG TABLES (BELOW)

C594 0.1uF 20% 16V CERM 402
C601 0.01uF 20% 16V CERM 402
C608 0.1uF 20% 16V CERM 402
C619 0.01uF 20% 16V CERM 402
C603 0.1uF 20% 16V CERM 402
C599 0.01uF 20% 16V CERM 402
PLACE CAPS (IN ORDER) ON PINS 1, 6, 10/15, 57/62, 67/71, 85

+2_5V_MAIN
R442 0 5% 1/16W MF 603

+2_5V_MARVELL

C597 0.1uF 20% 16V CERM 402
C612 0.01uF 20% 16V CERM 402
C623 0.1uF 20% 16V CERM 402
C600 0.01uF 20% 16V CERM 402
C598 0.1uF 20% 16V CERM 402
C595 10uF 20% 6.3V CERM 805
PLACE CAPS (IN ORDER) ON PINS 5, 21/26, 48/52, 66/72, 88, 96

C646 0.1uF 20% 16V CERM 402
C648 0.1uF 20% 16V CERM 402
C645 0.1uF 20% 16V CERM 402
C647 0.1uF 20% 16V CERM 402
PLACE CAPS AT CONNECTOR PINS 5 & 6

+2_5V_MARVELL_AVDD
L35 FERR-EMI-600-OHM SM

C614 0.1uF 20% 16V CERM 402
C616 0.01uF 20% 16V CERM 402
C618 0.1uF 20% 16V CERM 402
C602 0.01uF 20% 16V CERM 402
C592 10uF 20% 6.3V CERM 805
PLACE CAPS (IN ORDER) ON PINS 32/35, 36/40, 45 & 78

R433 49.9 1% 1/16W MF 402 — MDI0_PD
R435 49.9 1% 1/16W MF 402 — MDI1_PD
R437 49.9 1% 1/16W MF 402 — MDI2_PD
R439 49.9 1% 1/16W MF 402 — MDI3_PD
R434 49.9 1% 1/16W MF 402
R436 49.9 1% 1/16W MF 402
R438 49.9 1% 1/16W MF 402
R440 49.9 1% 1/16W MF 402

C622 0.01uF 20% 16V CERM 402
C613 0.01uF 20% 16V CERM 402
C615 0.01uF 20% 16V CERM 402
C617 0.01uF 20% 16V CERM 402
PLACE RESISTORS CLOSE TO PHY

CRITICAL J23 MJ-R0016 F-RT-TH

PRIMARY
13
11
5 ENET_CTAP
6 ENET_CTAP
1 MDI_0+
2 MDI_0-
3 MDI_1+
4 MDI_1-
7 MDI_2+
8 MDI_2-
9 MDI_3+
10 MDI_3-
12
14
RJ45 CHIP SIDE
CHGND1

1CT:1CT
75 OHM
1CT:1CT
75 OHM
1CT:1CT
75 OHM
1CT:1CT
75 OHM

SECONDARY
J1
J2
J3
J4
J5
J6
J7
J8
RJ45 CABLE SIDE

SHIELD
1000PF, 2000V

+2_5V_MARVELL

R431 10K 5% 1/16W MF 402
R430 10K 5% 1/16W MF 402
R432 1.5K 5% 1/16W MF 402
R422 1K 5% 1/16W MF 402 — INT_ENET_RST_L

D15 1N914 SOT23 — IO_RESET_L → ENET_RST_L

Q32 2N7002DW SOT-363 — AC_IN
Q32 2N7002DW SOT-363 — SLEEP_L_LS5

C611 2.2uF 20% 10V CERM 805

PLACES PHY IN "COMA" MODE WHEN ASLEEP ON BATTERY (SAVES POWER)

NO STUFF R425 20K 5% 1/16W MF 402
R441 0 5% 1/16W MF 402
PUT CRYSTAL CIRCUIT CLOSE TO PHY

CRITICAL Y5 SM-3
25.0000M
CLK25M_XTAL_IN
C604 27pF 5% 50V CERM 402
C624 27pF 5% 50V CERM 402
Y6 LOAD CAPACITANCE IS 16PF

NO STUFF R424 49.9 1% 1/16W MF 402
NO STUFF R429 49.9 1% 1/16W MF 402
R428 10K 5% 1/16W MF 402
R427 4.99K 1% 1/16W MF 402

CONFIG DEFINITIONS	
PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

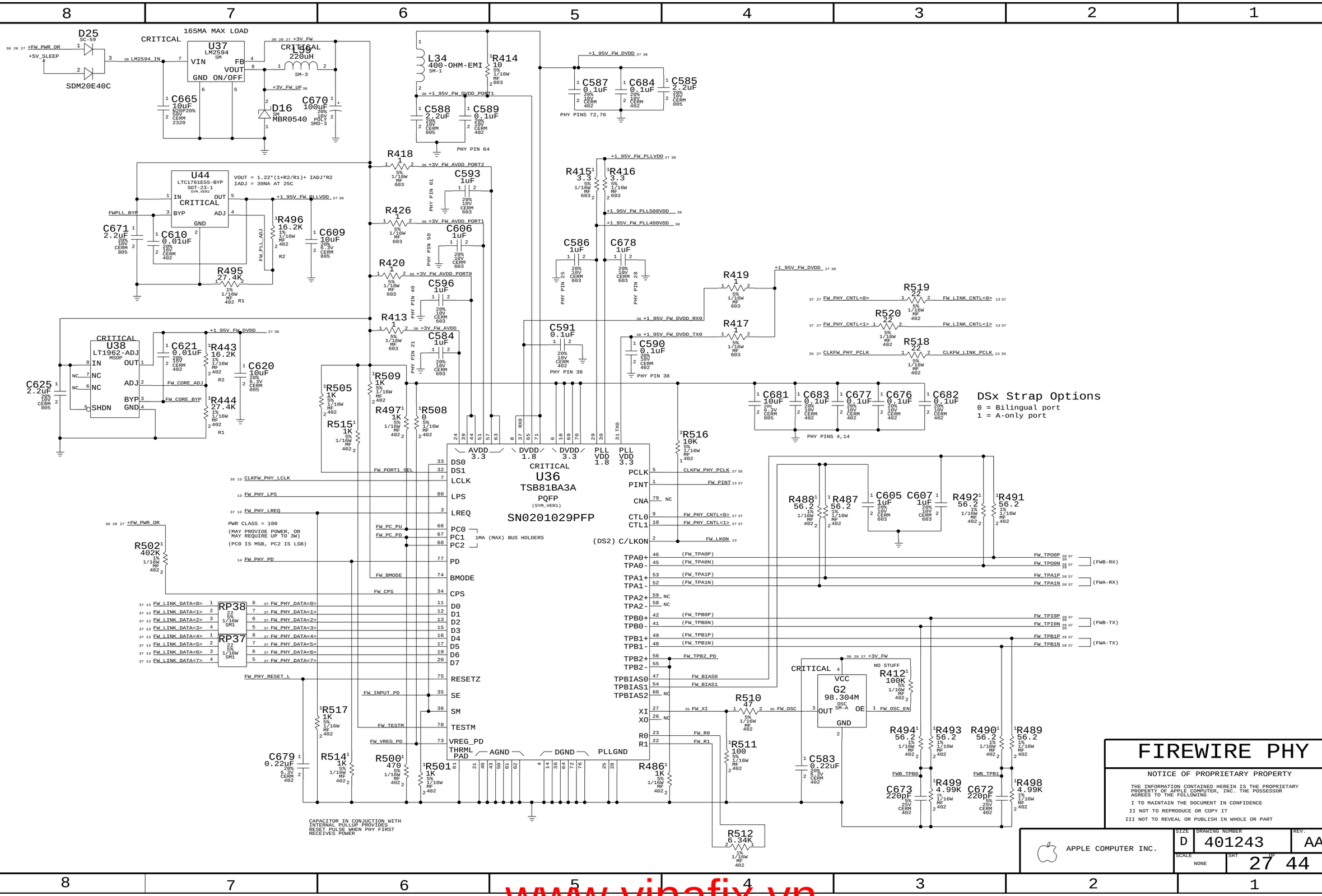
CONFIG INPUTS			
PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

MARVELL 88E1111

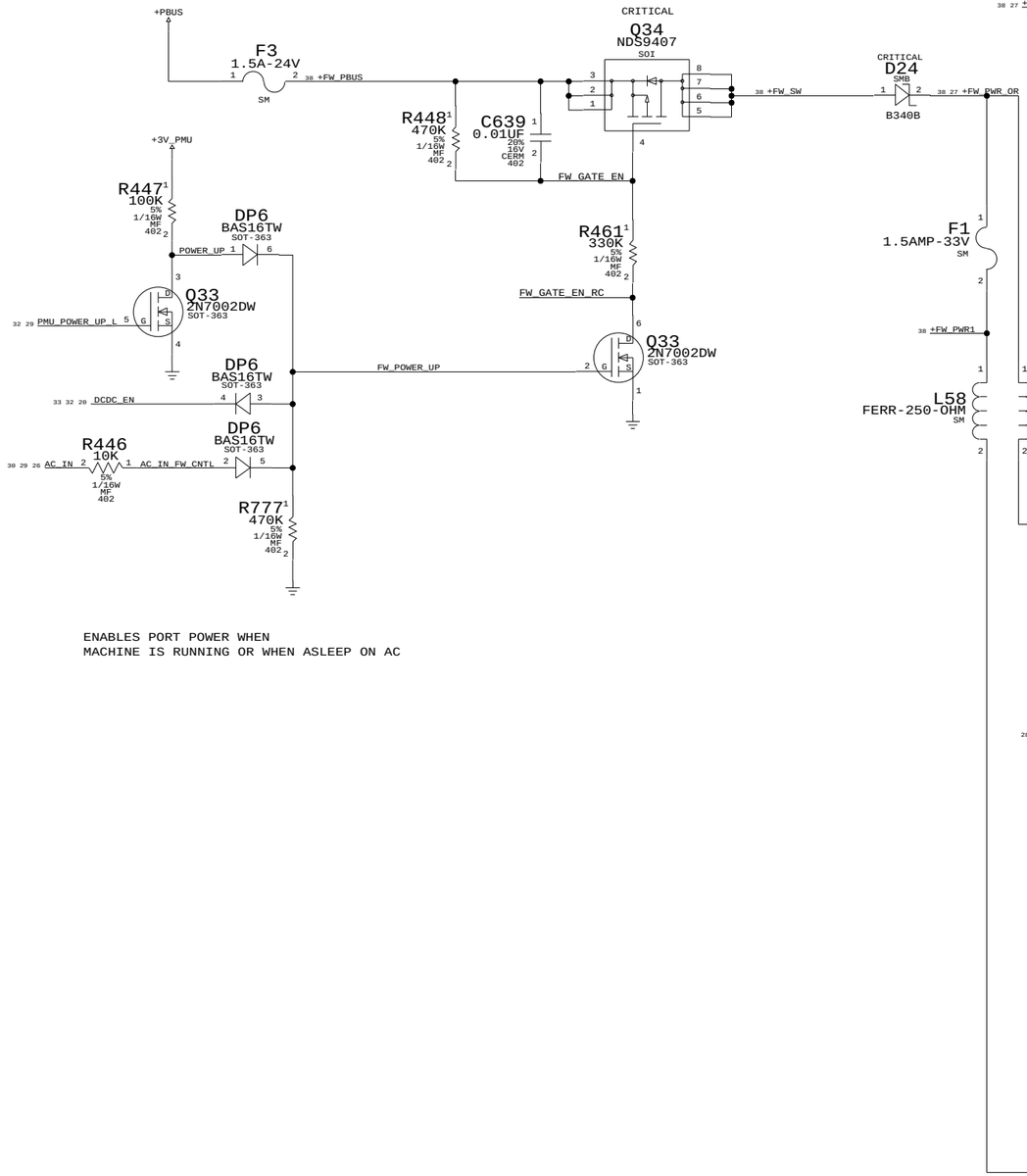
10/100/1000 ETHERNET

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401243	AA
SCALE: NONE	SHT 26 OF 44	



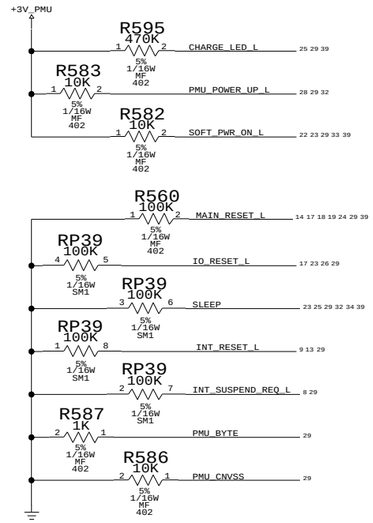
PORT POWER SWITCH

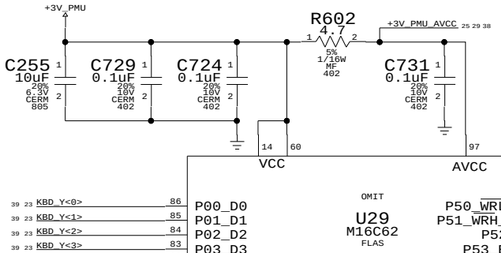


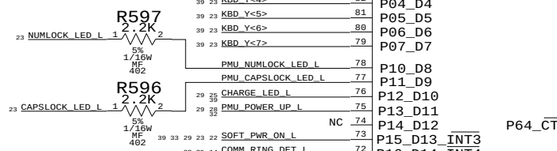
APPLE COMPUTER INC.

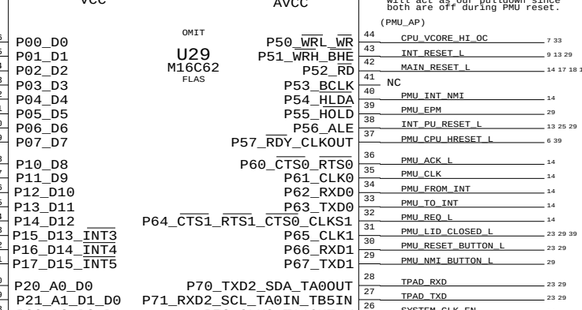
SIZE D | DRAWING NUMBER 401243 | REV. AA

SCALE NONE | SHT 28 OF 44





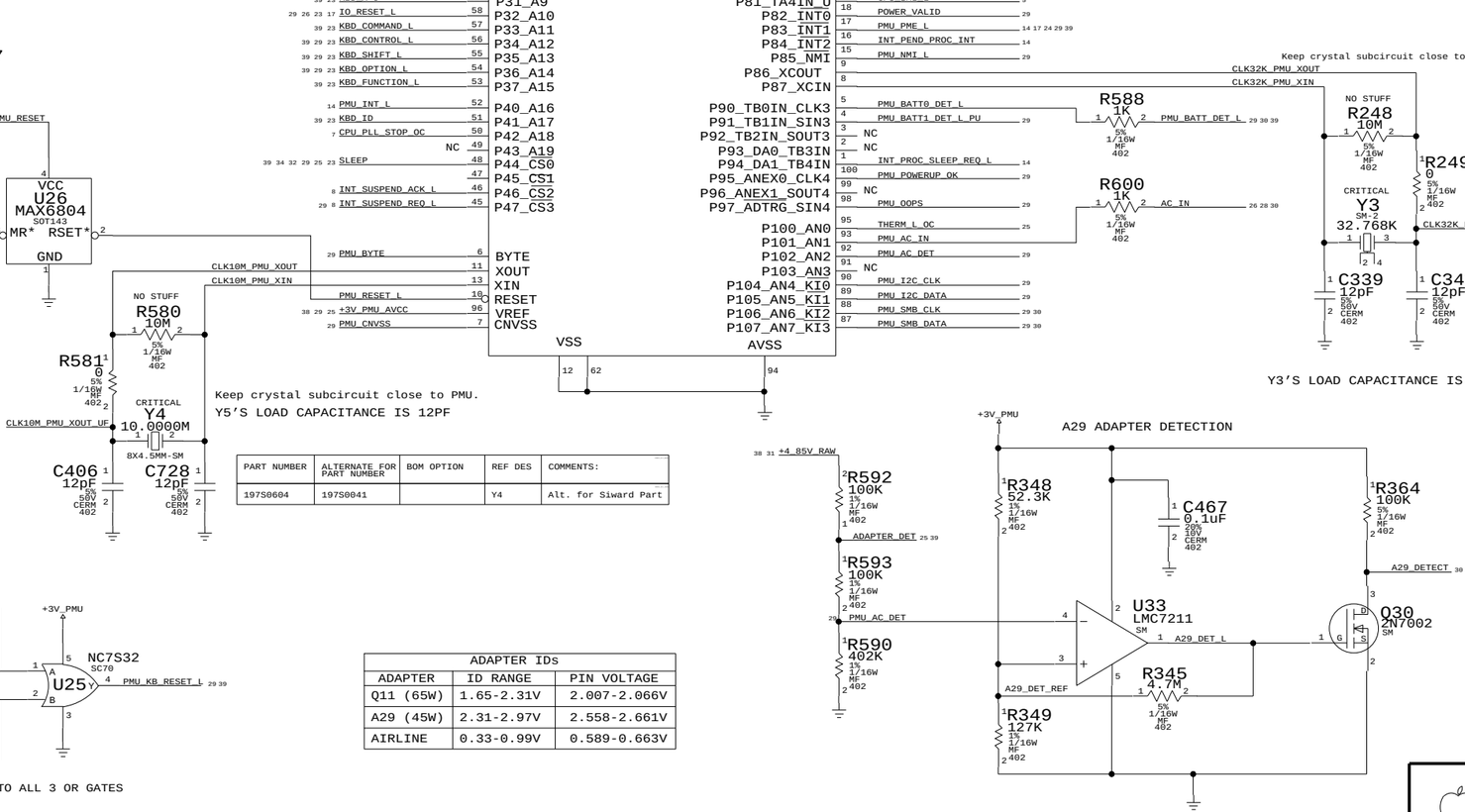


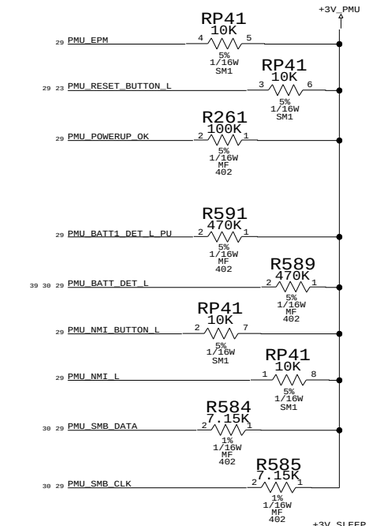


CPU_VCORE_HI_OC/PMU_AP should have a pulldown for coming out of reset. MLB will have a pull-up to +3V_MAIN or +3V_SLEEP, which will act as our pulldown since both are off during PMU reset.

(PMU_AP)

CPU_VCORE_HI_OC 7 33
INT_RESET_L 9 13 29
MAIN_RESET_L 14 17 18 19 24 29 39
NC
PMU_INT_NMI 14
PMU_EPM 29
INT_PU_RESET_L 13 25 29
PMU_CPU_HRESET_L 6 39
PMU_ACK_L 14
PMU_CLK 14
PMU_FROM_INT 14
PMU_TO_INT 14
PMU_REQ_L 14
PMU_LID_CLOSED_L 23 29 39
PMU_RESET_BUTTON_L 23 29
PMU_NMI_BUTTON_L 29
TPAD_RXD 23 29
TPAD_TXD 23 29
SYSTEM_CLK_EN 14
CPU_CLK_EN 8
PMU_CHARGE_V 30
PMU_CHRG_BATT_0 30
NC (CHARGE_I)
NC
PMU_SLEEP_LED_L 23
CPU_SMI_L 5
POWER_VALID 29
PMU_PME_L 14 17 24 29 39
INT_PEND_PROC_INT 14
PMU_NMI_L 29





UNDERVOLTAGE RESET CIRCUIT

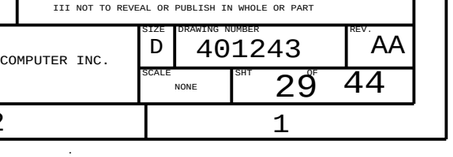
Keep crystal subcircuit close to PMU.
Y5'S LOAD CAPACITANCE IS 12PF

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0604	197S0041		Y4	Alt. for Siward Part

PMU KEYBOARD RESET CIRCUIT

KEEP CAP CLOSE TO ALL 3 OR GATES

ADAPTER IDs		
ADAPTER	ID RANGE	PIN VOLTAGE
Q11 (65W)	1.65-2.31V	2.007-2.066V
A29 (45W)	2.31-2.97V	2.558-2.661V
AIRLINE	0.33-0.99V	0.589-0.663V



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1008	1	IC,PMU,V81B	U29	

DC POWER INPUT

(POWER JACK, ETC. ON SEPARATE BOARD)

CRITICAL
J27
87438-0433
M-RT-SM

+ADAPTER

C35 0.1uF 10% 50V X7R 603

R51 20K 1% 1/16W MF 402

DC INRUSH LIMITER

Q68 SI4435DY SOI

R21 330K 5% 1/16W MF 402

C11 0.1uF 20% 50V CERM 805

AC_ENABLE_GATE

R29 470K 5% 1/16W MF 402

AC_ENABLE_L

+3V_PMU

R40 97.6K 1% 1/16W MF 402

R16 100K 1% 1/16W MF 402

C801 0.01uF 20% 16V CERM 402

R15 10K 5% 1/16W MF 402

38 31 1V20_REF

U1 LMC7211 SM

AC_DIV

R42 10K 1% 1/16W MF 402

R30 57.6K 1% 1/16W MF 402

R41 1M 5% 1/16W MF 402

AC_IN 26 28 29 30

AC_IN_L 30

Q1 2N7002DW SOT-363

R22 470K 5% 1/16W MF 402

Q1 2N7002DW SOT-363

GREATER THAN 13.1V DETECT

BACKFEED PROTECTION

Q69 SI4435DY SOI

38 +ADAPTER_SW

+ADAPTER_SENSE 38

BKFD_PROT_GATE

R732 47K 5% 1/16W MF 402

C803 0.1uF 20% 16V CERM 402

R734 68K 5% 1/16W MF 402

BKFD_PROT_EN_L

30 29 28 26 AC_IN

Q9 2N7002DW SOT-363

CRITICAL
U3 MAX4172 TSSOP

RS+ RS- PG OUT GND V+ NC NC1 NC2

+24V_PBUS

MAX4172_OUT

CRITICAL
R77 2.21K 0.1% 1/16W MF 603

C36 0.01uF 20% 50V CERM 603

Place close to RS-

C826 0.01uF 20% 50V CERM 603

PLACE U24 NEXT TO R382

CRITICAL
R61 0.025 1% 1W MF 2512

1772_CSSP 37

1772_CSSN 37

CSSP CSSN

R57 100K 1% 1/16W MF 402

D4 1N914 SOT23

C67 1uF 20% 50V CERM 1210

R82 4.7 5% 1/16W MF 402

R87 4.7 5% 1/16W MF 402

C71 0.47uF 20% 50V CERM 1206

C95 0.47uF 20% 50V CERM 1206

38 1772_DCIN

1772_ACIN

30 1772_ACOK_L

(+3V_PMU)

1772_VCTL

1772_ICTL

1772_ICHG

1772_IINP

1772_CCV

1772_CCI

1772_CCS

DCIN ACIN ACOK RFIN VCTL ICTL ICHG IINP CCV CCI CCS

U6 MAX1772 QSOP

CELLS LDO DLOV BST DHI LX DLO PGND CSIP CSIN BATT

CRITICAL

1772_CELLS

1772_DLOV

1772_BST

1772_DHI

1772_LX

1772_DLO

(GND)

37 1772_CSIP

37 1772_CSIN

REF CLS GND

1772_REF

1772_CLS

38 1772_GND

R56 1K 1% 1/16W MF 402

R55 1K 1% 1/16W MF 402

C43 0.01uF 20% 16V CERM 402

C42 0.01uF 20% 16V CERM 402

1772_CCV_RC

C24 0.1uF 20% 10V CERM 402

C23 1uF 20% 10V CERM 603

R54 10K 1% 1/16W MF 402

R53 4.12K 1% 1/16W MF 402

R83 1K 1% 1/16W MF 402

C41 1uF 20% 10V CERM 603

R94 100K 5% 1/16W MF 402

+PBUS CURRENT LIMIT

R728 1K 1% 1/16W MF 402

IAC_RC_COMP

C798 0.1uF 20% 10V CERM 402

+3V_PMU

C794 0.1uF 20% 10V CERM 402

CRITICAL
R745 42.2K 0.1% 1/16W FF 603

IAC_FB

U55 LMC7111 SOT23-5

PLACE R383 CLOSE TO LTC1625

ROUTE LTC1625_ITH CAREFULLY

LTC1625_ITH

DP1 BAS16TW SOT-363

R119 150 1% 1/16W MF 402

1625_COMP 31

ADAPTER_I_REG

R727 10K 1% 1/16W MF 402

CURRENT_THRESHOLD

CRITICAL
R736 42.2K 0.1% 1/16W FF 603

CRITICAL
R738 8.55K 0.1% 1/16W FF 603

CRITICAL
R742 51.1K 0.1% 1/16W FF 603

A29_CURRENT_ADJ

OVER_18V_ADJ

Q2 2N7002DW SOT-363

R744 100K 5% 1/16W MF 402

Q74 2N7002DW SOT-363

30 29 A29_DETECT

AC_GTR_18V

Q74 2N7002DW SOT-363

30 1772_ACOK_L

C809 1uF 20% 16V CERM 603

BATTERY SWITCH-OVER CIRCUIT

+BATT

F5 5AMP-125V SM-2

F4 5AMP-125V SM-2

+24V_PBUS

+PBUS

38 +BATT_24V_FUSE

30 +BATT_14V_FUSE

CRITICAL
Q6 SI4435DY SOI

CRITICAL
Q7 SUD45P03 TO-252

R716 47K 5% 1/16W MF 402

R710 47K 5% 1/16W MF 402

BATT_24V_GATE

BATT_14V_GATE

R717 10K 5% 1/16W MF 402

R711 10K 5% 1/16W MF 402

DP1 BAS16TW SOT-363

BATT_24PBUS_EN

BATT_14PBUS_EN

30 AC_IN_L

DP1 BAS16TW SOT-363

R102 158K 1% 1/16W MF 402

Q9 2N7002DW SOT-363

AC_IN_L_RC

C118 10uF 20% 6.3V CERM 805

WHEN AC IS IN, P-CHANNEL FETS ARE QUICKLY (DIODE) TURNED OFF

WHEN AC IS NOT PLUGGED, P-CHANNEL FETS ARE ON

RC TIME IS 480K*10UF @ +3V_PMU

SWITCHER VOLTAGE CONTROL

PMU SELECTS BETWEEN TWO VOLTAGES

SWITCHER CURRENT CONTROL

CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V

CHARGE THROTTLED BY LOW BATTERY VOLTAGE

OD OUTPUT LOW - WHEN AC GREATER THAN 18V

+3V_PMU

R73 27.4K 1% 1/16W MF 402

R62 10K 1% 1/16W MF 402

R58 10K 1% 1/16W MF 402

R74 4.12K 1% 1/16W MF 402

R733 20K 1% 1/16W MF 402

R731 1K 1% 1/16W MF 402

BATTV_HIGH

BATT_LOW_L

R59 100K 5% 1/16W MF 402

Q4 2N7002DW SOT-363

BATTV_LOW

R75 5.23K 1% 1/16W MF 402

Q71 2N7002DW SOT-363

Q71 2N7002DW SOT-363

29 PMU_CHARGE_V

Q4 2N7002DW SOT-363

+3V_PMU

R741 100K 5% 1/16W MF 402

Q72 2N7002DW SOT-363

CHARGE_DISABLE

29 PMU_CHRG_BATT_0

Q72 2N7002DW SOT-363

$V_{BATT} = CELLS \times (4.096 + (0.4096 * V_{VCTL} / V_{REFIN}))$

For 4.15V cells, VCTL = 0.123 REFIN

For 4.20V cells, VCTL = 0.245 REFIN

$I_{CHG} = (0.2048/R_{62}) * (V_{ICTL} / V_{REFIN})$

+3V_PMU

C799 0.1uF 20% 16V CERM 402

U57 LMC7211 SM

BATT_LOW

R729 100K 1% 1/16W MF 402

R740 499K 1% 1/16W MF 402

BATT_DIV

1V65_REF

R730 100K 1% 1/16W MF 402

R735 100K 1% 1/16W MF 402

C807 0.047uF 10% 16V CERM 402

R47 6.34K 1% 1/16W MF 402

A29_CLS_ADJ

30 29 A29_DETECT

Q2 2N7002DW SOT-363

38 +BATT_VSNS

BATTERY CONNECTOR

CRITICAL
J26
87438-0833
M-RT-SM

39 38 +BATT_POS

(BATT_IN_PD)

39 BATT_CLK

39 BATT_DATA

PMU_BATT_DET_L 29 39

38 39 BATT_NEG

L5 FERR-EMI-100-OHM SM

L6 FERR-50-OHM SM

L4 FERR-EMI-100-OHM SM

PMU_SMB_CLK 29

L3 FERR-EMI-100-OHM SM

PMU_SMB_DATA 29

L2 FERR-50-OHM SM

+BATT

R725 33 5% 1/8W FF 1206

D6 1N914 SOT23

1772_BST_ESR

R52 100K 5% 1/16W MF 402

C97 0.1uF 20% 25V CERM 603

R96 4.7 5% 1/16W MF 603

+24V_PBUS

C96 0.1uF 20% 50V CERM 805

CRITICAL
Q70 IRF7805 SM

C112 2.2uF 20% 50V CERM 1812

C117 2.2uF 20% 50V CERM 1812

C113 2.2uF 20% 50V CERM 1812

C115 2.2uF 20% 50V CERM 1812

C116 2.2uF 20% 50V CERM 1812

CRITICAL
L70 10uH SM1

+BATT_RSNS 38

R715 0.05 1% 1W MF 2512

+BATT_24V_FUSE 30 38

C98 0.1uF 20% 25V CERM 603

C99 0.1uF 20% 25V CERM 603

CRITICAL
Q64 IRF7811W SO-8

D36 SM MBRS140T3

C780 4.7uF 20% 25V CERM 1206

C795 4.7uF 20% 25V CERM 1206

C790 4.7uF 20% 25V CERM 1206

C779 33uF 20% 20VDC SM1

NO STUFF

C853 1000pF 10% 50V X7R 402

XW1 SM

R720 1 5% 1/16W MF 603

R713 1 5% 1/16W MF 603

C777 4.7uF 20% 25V CERM 1206

C792 4.7uF 20% 25V CERM 1206

C785 4.7uF 20% 25V CERM 1206

BATTERY CHARGER

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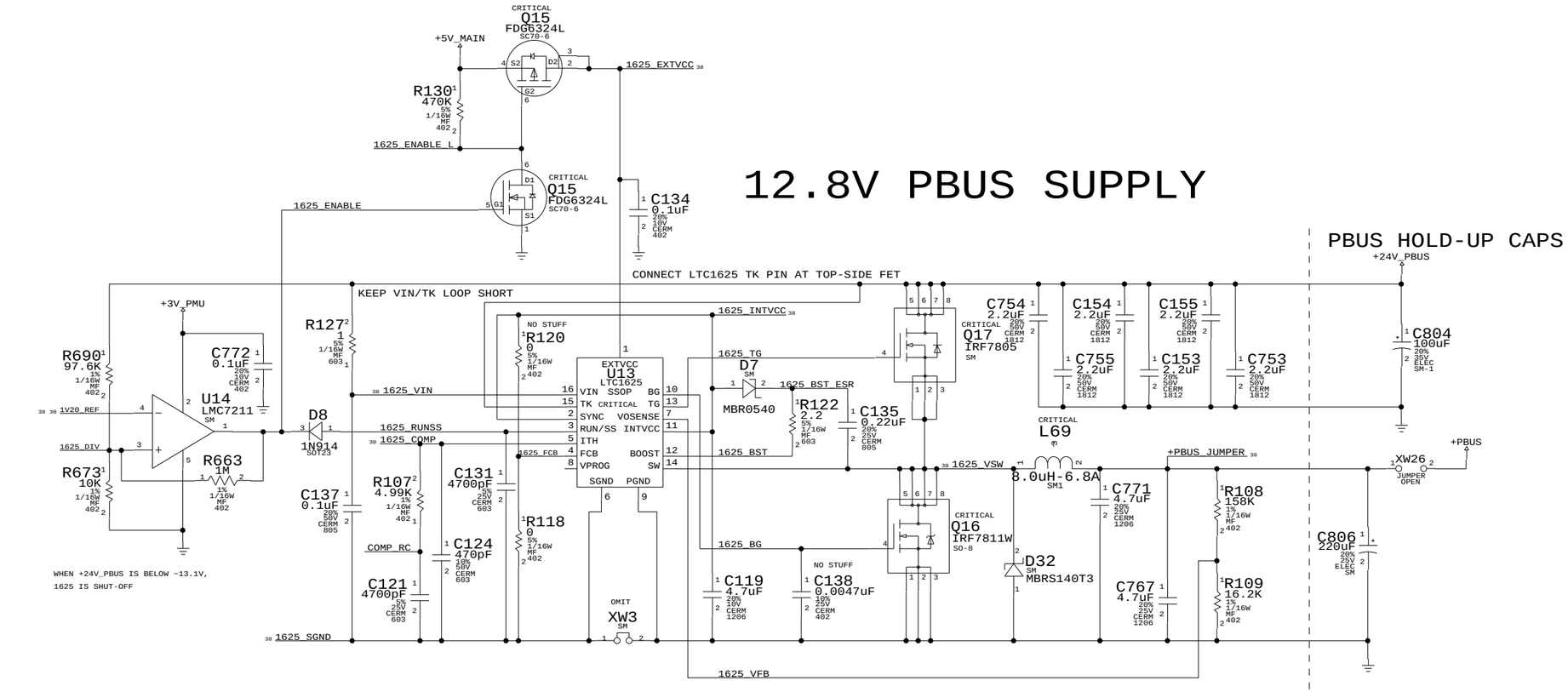
APPLE COMPUTER INC.

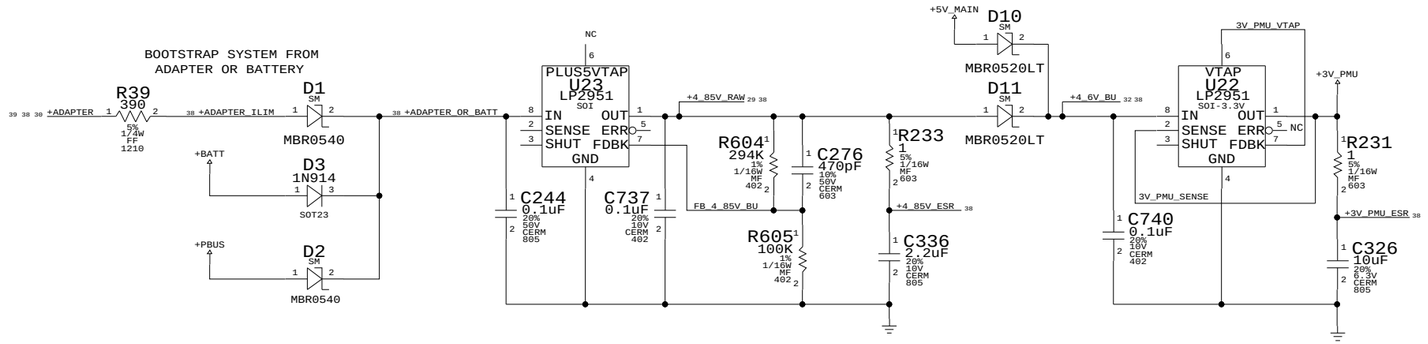
SIZE	DRAWING NUMBER	REV.
D	401243	AA

SCALE	SHT OF
NONE	30 44

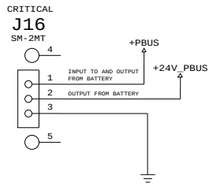
12.8V PBUS SUPPLY



PMU SUPPLY



BACKUP BATTERY



12.8V REGULATOR

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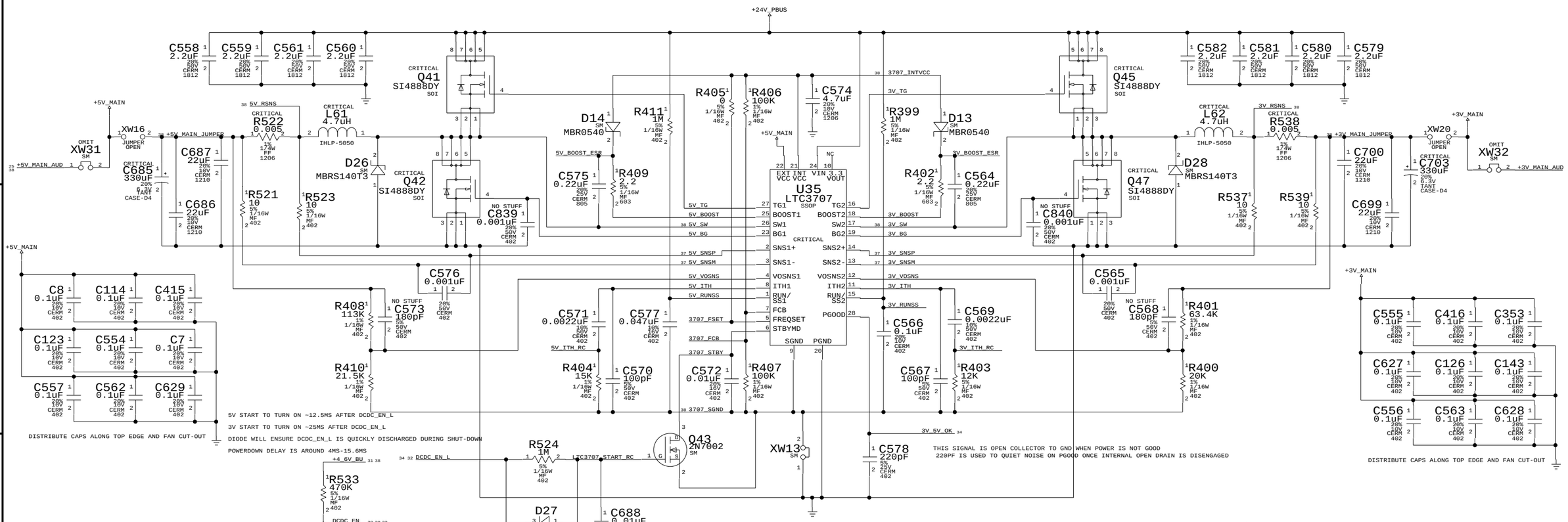
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401243	AA
SCALE: NONE	SHT 31 OF 44	

3.3V/5V MAIN SUPPLY



3.3V/5V REGULATOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401243	AA
SCALE: NONE	SHT 32 OF 44	

VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage
(approx. 7ms delay)

1.175V->1.025V

1.350V->1.075V
1.225V->1.050V
(value without offset)

1.25Ghz
1.0Ghz

NOTE: When U15 MUX is removed => NO SW Support,
R794,R795,R796&R797 have to be stuffed

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
126S0036	7	CAP,AL,POLY,8.2uF,20%,16V,V CASE,SMD	C51,C52,C77,C78,C91,C92,C111	CRITICAL	

SEL = 0; Y1=A1
SEL = 1; Y1=B1

Keep trace fat (40-100 mils) and short!!

Sense resistor R650 may not be needed!

Keep trace fat and short!!

(VCORE=1.385V for EVTB)

MAX1717 VID INPUTS ARE 3.3-5V TOLERANT

Note:No stuff R67 to set skip mode of VCore

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V, HENCE VOFFSET = 2.0V * (Rb / Ra) AND VCORE = VDAC + VOFFSET.
NOTE: Ra NO STUFFED FOR NO OFFSET CASE

Connect MAX1717 GND pin 13
to GND at bottom-side FET

Keep trace fat and short!!

PLACE THIS SHORT AT
PIN OF 1000uF CAP
CLOSEST TO CPU

ROUTE AS DIFFERENTIAL PAIR

(CPU Vcore value with offset)

1.25Ghz 1.360V->1.080V
1.0Ghz 1.235V->1.060V

OUTPUT VOLTAGE

V_{DAC} D4=0	V_{DAC} D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	A/B_ = Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1
If all pull-ups are >=100K and all
pull-downs are <=1K, $V_A = V_B$.

Fmax Test Connections

VCORE SUPPLY

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401243	AA
SCALE: NONE	SHT 33 OF 44	

1.5V/2.5V SWITCHER

+1_5V_SLEEP LOADS

1) AGP I/O - IF USING D3COLD
2) MAXBUS I/O - IF 1.5V INTERFACE

+1_5V_MAIN LOADS

1) INTREPID CORE

+2_5V_MAIN LOADS

1) MAP31 - FBCORE/FBIO IF USING D3HOT
2) GIGABIT ETHERNET - AVDDL
3) DDR SODIMMS - CORE/IO
4) DDR MUXES

M10 Power Shut down Sequencing

+2_5V_SLEEP LOADS

1) FBCORE/FBIO IF USING D3COLD

1.8V SWITCHER

+1_8V_MAIN LOADS

1) INTREPID PLLS

+1_8V_SLEEP LOADS

1) MPC7447 - MAXBUS I/O - IF 1.8V INTERFACE
2) CPU JTAG & MaxBus Pull-ups
3) CPU PLL Config Straps

1.5V/1.8V/2.5V SUPPLIES

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401243	AA
SCALE: NONE	SHT 34 OF 44	

DIGITAL SIGNALS

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
				STUB_LENGTH OF 200 MILS NEEDED WHEN WE CONVERT TO 14.2				
GROUP 0	MEM_DATA<7..0>	L:S:1602:1700	7	500	(200)			167 MHZ
	MEM_DQM<0>	L:S:1602 MIL:1700 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<0>	L:S:1602 MIL:1700 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<7..0>	L:S:1903:2000	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<0>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<0>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<7..0>	L:S:2000:2100	7	500	(200)			167 MHZ
	RAM_DQM_B<0>	L:S:2000 MIL:2100 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<0>	L:S:2000 MIL:2100 MIL	7	500.0000	(200)			167.0 MHz
GROUP 1	MEM_DATA<15..8>	L:S:1344:1660	7	500	(200)			167 MHZ
	MEM_DQM<1>	L:S:1344 MIL:1660 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<1>	L:S:1344 MIL:1660 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<15..8>	L:S:1905:2000	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<1>	L:S:1905 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<1>	L:S:1905 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<15..8>	L:S:2004:2412	7	500	(200)			167 MHZ
	RAM_DQM_B<1>	L:S:2004 MIL:2412 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<1>	L:S:2004 MIL:2412 MIL	7	500.0000	(200)			167.0 MHz
GROUP 2	MEM_DATA<23..16>	L:S:1435:1500	7	500	(200)			167 MHZ
	MEM_DQM<2>	L:S:1435 MIL:1500 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<2>	L:S:1435 MIL:1500 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<23..16>	L:S:1707:1800	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<2>	L:S:1707 MIL:1800 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<2>	L:S:1707 MIL:1800 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<23..16>	L:S:1900:2000	7	500	(200)			167 MHZ
	RAM_DQM_B<2>	L:S:1900 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<2>	L:S:1900 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
GROUP 3	MEM_DATA<31..24>	L:S:1233:1485	7	500	(200)			167 MHZ
	MEM_DQM<3>	L:S:1233 MIL:1485 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<3>	L:S:1233 MIL:1485 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<31..24>	L:S:1700:2165	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<3>	L:S:1700 MIL:2165 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<3>	L:S:1700 MIL:2165 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<25..24>	L:S:1907:2356	7	500	(200)			167 MHZ
	RAM_DATA_B<26>	L:S:1907 MIL:2356 MIL	7		(200)			167.0 MHz
	RAM_DATA_B<31..27>	L:S:1907:2356	7	500	(200)			167 MHZ
	RAM_DQM_B<3>	L:S:1907 MIL:2356 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<3>	L:S:1907 MIL:2356 MIL	7	500.0000	(200)			167.0 MHz
GROUP 4	MEM_DATA<39..32>	L:S:1915:2000	7	500	(200)			167 MHZ
	MEM_DQM<4>	L:S:1915 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<4>	L:S:1915 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<39..32>	L:S:1205:1387	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<4>	L:S:1205 MIL:1387 MIL	7	500.0000	(200)			167.0 MHz
DDR RAM	RAM_DQS_A<4>	L:S:1205 MIL:1387 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<39..32>	L:S:1404:1686	7	500	(200)			167 MHZ
	RAM_DQM_B<4>	L:S:1404 MIL:1686 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<4>	L:S:1404 MIL:1686 MIL	7	500.0000	(200)			167.0 MHz
GROUP 5	MEM_DATA<47..40>	L:S:1719:1893	7	500	(200)			167 MHZ
	MEM_DQM<5>	L:S:1719 MIL:1893 MIL	7	500.0000	**(200)**			167.0 MHz
	MEM_DQS<5>	L:S:1719 MIL:1893 MIL	7	500.0000	**(200)**			167.0 MHz
	RAM_DATA_A<47..40>	L:S:1607:1898	7	500	**(200)**	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<5>	L:S:1607 MIL:1898 MIL	7	500.0000	**(200)**			167.0 MHz
	RAM_DQS_A<5>	L:S:1607 MIL:1898 MIL	7	500.0000	**(200)**			167.0 MHz
	RAM_DATA_B<47..40>	L:S:1716:2102	7	500	**(200)**			167 MHZ
	RAM_DQM_B<5>	L:S:1716 MIL:2102 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<5>	L:S:1716 MIL:2102 MIL	7	500.0000	(200)			167.0 MHz
GROUP 6	MEM_DATA<55..48>	L:S:2101:2170	7	500	(200)			167 MHZ
	MEM_DQM<6>	L:S:2101 MIL:2170 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<6>	L:S:2101 MIL:2170 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<55..48>	L:S:1204:1357	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<6>	L:S:1204 MIL:1357 MIL	7	500.0000	**(200)**			167.0 MHz
	RAM_DQS_A<6>	L:S:1204 MIL:1357 MIL	7	500.0000	**(200)**			167.0 MHz
	RAM_DATA_B<55..48>	L:S:1400:1546	7	500	**(200)**			167 MHZ
	RAM_DQM_B<6>	L:S:1400 MIL:1546 MIL	7	500.0000	**(200)**			167.0 MHz
	RAM_DQS_B<6>	L:S:1400 MIL:1546 MIL	7	500.0000	**(200)**			167.0 MHz
GROUP 7	MEM_DATA<63..56>	L:S:1903:2000	7	500	**(200)**			167 MHZ
	MEM_DQM<7>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<7>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<63..56>	L:S:1611:1696	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<7>	L:S:1611 MIL:1696 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<7>	L:S:1611 MIL:1696 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<63..56>	L:S:1809:1887	7	500	(200)			167 MHZ
	RAM_DQM_B<7>	L:S:1809 MIL:1887 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<7>	L:S:1809 MIL:1887 MIL	7	500.0000	(200)			167.0 MHz
ADDR	MEM_ADDR<12..0>	L:S:500	4					83 MHZ
	RAM_ADDR<12..0>	L:S:2000:3000	10		(200)			
	MEM_BA<1..0>	L:S:500	4					
	RAM_BA<1..0>	L:S:2000:3300	8		(200)			
CONTROL	MEM_CS_L<3..0>	L:S:500	4					
	RAM_CS_L<3..0>	L:S:2500:3200	7		(200)			
	MEM_CKE<3..0>	L:S:500	4					
	RAM_CKE<3..0>	L:S:2500:3200	7		(200)			
	MEM_RAS_L	L:S:500 MIL	4					
	RAM_RAS_L	L:S:2000 MIL:4100 MIL	7		(200)			
	MEM_CAS_L	L:S:500 MIL	4					
	RAM_CAS_L	L:S:2000 MIL:4100 MIL	7		(200)			
	MEM_WE_L	L:S:500 MIL	4					
	RAM_WE_L	L:S:2000 MIL:3100 MIL	8		(200)			
	MEM_MUXSEL_MSB	L:S:1700 MIL:3000 MIL	8					
	MEM_MUXSEL_LSB	L:S:1700 MIL:3000 MIL	7					

PRIORITY: 2
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9
GOAL: MINIMIZE
EXPOSED ROUTES
MINIMIZE VIAS

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME	PROPAGATION_DELAY	MATCHED_DELAY	MAX VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM
INTREPID CLOCKS	SYSCLK_CPU_UF	L:S::150 MIL					10 MIL SPACING	167.0 MHz:::
	SYSCLK_CPU	L:S:2650 MIL:2750 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz:::
	INT_CPUFB_OUT	L:S::150 MIL		5	250.0000		10 MIL SPACING	167.0 MHz:::
	INT_CPUFB_OUT_SHORT	L:S:700 MIL:850 MIL		5	250.0000		10 MIL SPACING	167.0 MHz:::
	INT_CPUFB_OUT_NORM	L:S:500 MIL:600 MIL		5	250.0000		10 MIL SPACING	167.0 MHz:::
	INT_CPUFB_IN_NORM	L:S:500 MIL:600 MIL		5	250.0000		10 MIL SPACING	167.0 MHz:::
	INT_CPUFB_LONG	L:S:1050 MIL:1150 MIL		5	250.0000		10 MIL SPACING	167.0 MHz:::
	INT_CPUFB_IN	L:S:700 MIL:800 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz:::
	SYSCLK_DDRCLK_A0_UF	L:S:300 MIL:3000 MIL	SYSCLK_DDRCLK_A0_UF	SYSCLK_DDRCLK_A0_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz:::
	SYSCLK_DDRCLK_A0_L_UF	L:S:300 MIL:3000 MIL	SYSCLK_DDRCLK_A0_UF	SYSCLK_DDRCLK_A0_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz:::
	SYSCLK_DDRCLK_A1_UF	L:S:300 MIL:3000 MIL	SYSCLK_DDRCLK_A1_UF	SYSCLK_DDRCLK_A1_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz:::
	SYSCLK_DDRCLK_A1_L_UF	L:S:300 MIL:3000 MIL	SYSCLK_DDRCLK_A1_UF	SYSCLK_DDRCLK_A1_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz:::
	SYSCLK_DDRCLK_B0_UF	L:S:300 MIL:3000 MIL	SYSCLK_DDRCLK_B0_UF	SYSCLK_DDRCLK_B0_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz:::
	SYSCLK_DDRCLK_B0_L_UF	L:S:300 MIL:3000 MIL	SYSCLK_DDRCLK_B0_UF	SYSCLK_DDRCLK_B0_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz:::
	SYSCLK_DDRCLK_B1_UF	L:S:300 MIL:3000 MIL	SYSCLK_DDRCLK_B1_UF	SYSCLK_DDRCLK_B1_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz:::
	SYSCLK_DDRCLK_B1_L_UF	L:S:300 MIL:3000 MIL	SYSCLK_DDRCLK_B1_UF	SYSCLK_DDRCLK_B1_UF:G:L:S:0 MIL:25 MIL		(200)	10 MIL SPACING	167.0 MHz:::
	SYSCLK_DDRCLK_A0	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A0	SYSCLK_DDRCLK_A0:G:L:S:0 MIL:25 MIL7	250.0000	(200)	10 MIL SPACING	167.0 MHz:::
	SYSCLK_DDRCLK_A0_L	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A0	SYSCLK_DDRCLK_A0:G:L:S:0 MIL:25 MIL7	250.0000	(200)	10 MIL SPACING	167.0 MHz:::
	SYSCLK_DDRCLK_A1	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A1	SYSCLK_DDRCLK_A1:G:L:S:0 MIL:25 MIL7	250.0000	(200)	10 MIL SPACING	167.0 MHz:::
	SYSCLK_DDRCLK_A1_L	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A1	SYSCLK_DDRCLK_A1:G:L:S:0 MIL:25 MIL7	250.0000	(200)	10 MIL SPACING	167.0 MHz:::
	SYSCLK_DDRCLK_B0	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B0	SYSCLK_DDRCLK_B0:G:L:S:0 MIL:25 MIL7	250.0000	(200)	10 MIL SPACING	167.0 MHz:::
	SYSCLK_DDRCLK_B0_L	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B0	SYSCLK_DDRCLK_B0:G:L:S:0 MIL:25 MIL7	250.0000	(200)	10 MIL SPACING	167.0 MHz:::
	SYSCLK_DDRCLK_B1	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B1	SYSCLK_DDRCLK_B1:G:L:S:0 MIL:25 MIL7	250.0000	(200)	10 MIL SPACING	167.0 MHz:::
	SYSCLK_DDRCLK_B1_L	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B1	SYSCLK_DDRCLK_B1:G:L:S:0 MIL:25 MIL7	250.0000	(200)	10 MIL SPACING	167.0 MHz:::
	INT_REF_CLK_OUT_UF	L:S::400 MIL				(200)	10 MIL SPACING	49.92 MHz:::
	INT_REF_CLK_OUT	L:S:1000 MIL:1150 MIL		5	250.0000	(200)	10 MIL SPACING	49.92 MHz:::
	INT_REF_CLK_IN	L:S:1900 MIL:2000 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz:::
	CLK66M_GPU_AGP_UF	L:S::150 MIL				(200)	10 MIL SPACING	66.00 MHz:::
	CLK66M_GPU_AGP	L:S:1800 MIL:1900 MIL		6	400.0000	(200)	10 MIL SPACING	66.00 MHz:::
	INT_AGP_FB_OUT	L:S::150 MIL				(200)	10 MIL SPACING	66.00 MHz:::
	INT_AGP_FB_IN	L:S:1450 MIL:1550 MIL		6	500.0000	(200)	10 MIL SPACING	66.00 MHz:::
	CLK33M_CBUS_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz:::
	CLK33M_CBUS	L:S:5000 MIL:6000 MIL		9	500.0000	(200)	10 MIL SPACING	33.00 MHz:::
	CLK33M_AIRPORT_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz:::
	CLK33M_AIRPORT	L:S:9500 MIL:10500 MIL		6	500.0000	(200)	10 MIL SPACING	33.00 MHz:::
	CLK33M_NEC_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz:::
	CLK33M_NEC	L:S:4000 MIL:6000 MIL		7	500.0000	(200)	10 MIL SPACING	33.00 MHz:::
	INT_PCI_FB_OUT	L:S::300 MIL				(200)	10 MIL SPACING	33.00 MHz:::
	INT_PCI_FB_IN	L:S:6500 MIL:7500 MIL		7	500.0000	(200)	10 MIL SPACING	33.00 MHz:::
M10 & OSC	ATI_CLK27M_OSC	L:S::400 MIL		5		(200)	10 MIL SPACING	
	ATI_CLK27M_OSC_SS	L:S::400 MIL		5		(200)	10 MIL SPACING	
	ATI_CLK27M_IN	L:S::200 MIL		5		(200)	10 MIL SPACING	
	ATI_SSCLK_UF	L:S::200 MIL		5		(200)	10 MIL SPACING	
	ATI_SSCLK_IN	L:S::1800 MIL		5	500.0000	(200)	10 MIL SPACING	
CRYSTALS	CLK18M_INT_XIN	L:S:1400 MIL:1500 MIL					10 MIL SPACING	
	CLK18M_INT_XOUT	L:S:1250 MIL:1350 MIL					10 MIL SPACING	
	CLK18M_XTAL_IN	L:S::300 MIL					10 MIL SPACING	
	CLK18M_INT_EXT	L:S::400 MIL					10 MIL SPACING	
SOUND	INT_I2S0_SND_MCLK			6	500.0000	(200)	10 MIL SPACING	
ETHERNET	CLKENET_PHY_RX	L:S::300 MIL				(200)		125.0 MHz:::
	CLKENET_LINK_RX	L:S:8000 MIL:9000 MIL		6	800.0000	(200)	10 MIL SPACING	125.0 MHz:::
	CLKENET_PHY_GBE_REF	L:S::300 MIL				(200)		125.0 MHz:::
	CLKENET_LINK_GBE_REF	L:S:8000 MIL:9000 MIL		6	500.0000	(200)	10 MIL SPACING	125.0 MHz:::
	CLKENET_PHY_TX	L:S::300 MIL				(200)		25.00 MHz:::
	CLKENET_LINK_TX	L:S:8000 MIL:9000 MIL		6	500.0000	(200)	10 MIL SPACING	25.00 MHz:::
	CLKENET_LINK_GTX	L:S::300 MIL				(200)		125.0 MHz:::
	CLKENET_PHY_GTX	L:S:8000 MIL:9000 MIL		6	600.0000	(200)	10 MIL SPACING	125.0 MHz:::
FIREWIRE	CLKFW_PHY_PCLK	L:S::300 MIL				(200)		49.15 MHz:::
	CLKFW_LINK_PCLK	L:S:7500 MIL:8000 MIL		5	500.0000	(200)	10 MIL SPACING	49.15 MHz:::
	CLKFW_PHY_LCLK	L:S:7500 MIL:8000 MIL		5	500.0000	(200)	10 MIL SPACING	49.15 MHz:::
	CLKFW_LINK_LCLK	L:S::300 MIL				(200)		49.15 MHz:::
	FW_XI	L:S::500 MIL				(200)	10 MIL SPACING	98.03 MHz:::
	FW_OSC	L:S::300 MIL				(200)	10 MIL SPACING	98.03 MHz:::

PRIORITY: 1
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9
GOAL: MINIMIZE EXPOSURE ON LONG NETS

SIGNAL CONSTRAINTS - PAGE 1

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401243	AA
SCALE: NONE	SHT 35 OF 44	

DIGITAL SIGNALS

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
MAXBUS	CPU_AACK_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_ADDR<0..31>	L:S:1500:3100	7		(250)		TRUE	83 MHZ
	CPU_ARTRY_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_BG_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_BR_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_CI_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_DATA<0..31>	L:S:1100:2700	7		(250)		TRUE	83 MHZ
	CPU_DATA<32..63>	L:S:1100:2700	8		(250)			83 MHZ
	CPU_DBG_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_DTI<0..2>	L:S:1500:2950	7		(250)			
	CPU_DRDY_L	L:S:1500 MIL:3200 MIL	7		(250)			
	CPU_GBL_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_HIT_L	L:S:1500 MIL:2800 MIL	7		(250)			
	CPU_QACK_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_QREQ_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_TA_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_TBST_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_TEA_L	L:S:1500 MIL:3000 MIL	7		(250)			
	CPU_TS_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_TSIZ<0..2>	L:S:1500:3500	7		(250)			
	CPU_TT<0..4>	L:S:1500:3400	7		(250)			
	CPU_WT_L	L:S:1500 MIL:3100 MIL	7		(250)			

PRIORITY: 4
PRIMARY LAYERS: 9
SECONDARY LAYERS: 4,7
GOAL: MINIMIZE TH VIAS

STUB_LENGTH OF 250 MILS NEEDED WHEN DESIGN SWITCHED TO 14.2

Temporary Area for TMDS/DVO signal constraints

ALL TMDS GROUP SIGNALS ROUTE AT LAYER 4 OR 7 AND HAVE SAME WIDTH SPACING RULE AS OTHER TMDS SIGNALES

T231	GPU_TMDS_CLKN	GPU_CLKTMDS	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	5	19 20
T233	GPU_TMDS_CLKP	GPU_CLKTMDS	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	5	19 20
T232	GPU_TMDS_DN<0>	GPU_TMDS_D0	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19 20
T234	GPU_TMDS_DP<0>	GPU_TMDS_D0	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19 20
T235	GPU_TMDS_DN<1>	GPU_TMDS_D1	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19 20
T236	GPU_TMDS_DP<1>	GPU_TMDS_D1	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19 20
T238	GPU_TMDS_DN<2>	GPU_TMDS_D2	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19 20
T237	GPU_TMDS_DP<2>	GPU_TMDS_D2	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19 20

T240	SI_TMDS_CLKN	SI_CLKTMDS	SITMDS:G:L:S:0 MIL:50 MIL		100 OHM SPACING	5	19
T239	SI_TMDS_CLKP	SI_CLKTMDS	SITMDS:G:L:S:0 MIL:50 MIL		100 OHM SPACING	5	19
T242	SI_TMDS_DN<0>	SI_TMDS_D0	SITMDS:G:L:S:0 MIL:50 MIL		100 OHM SPACING	8	19
T241	SI_TMDS_DP<0>	SI_TMDS_D0	SITMDS:G:L:S:0 MIL:50 MIL		100 OHM SPACING	8	19
T243	SI_TMDS_DN<1>	SI_TMDS_D1	SITMDS:G:L:S:0 MIL:50 MIL		100 OHM SPACING	8	19
T245	SI_TMDS_DP<1>	SI_TMDS_D1	SITMDS:G:L:S:0 MIL:50 MIL		100 OHM SPACING	8	19
T244	SI_TMDS_DN<2>	SI_TMDS_D2	SITMDS:G:L:S:0 MIL:50 MIL		100 OHM SPACING	8	19
T246	SI_TMDS_DP<2>	SI_TMDS_D2	SITMDS:G:L:S:0 MIL:50 MIL		100 OHM SPACING	8	19

ALL THE DVOD GROUP SIGNALS ROUTE AT LAYER 4 OR 7 AND ROUTE AS STANDARD 50OHM SIGNALS AT 4 MILS

T263	ATI_DVOD<11..0>	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610			19 20
T265	ATI_DVOD_DE	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610.0000			19 20
T264	ATI_DVO_HSYNC	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610.0000			19 20
T267	ATI_DVO_VSYNC	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610.0000			19 20
T266	ATI_DVO_CLKP	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610.0000	165.0 MHz:::		19 20

T255	GPU_DVOD<11..0>	GPUDVOD:G:L:S:0 MIL:50 MIL	6	700			19
T256	GPU_DVOD_DE	GPUDVOD:G:L:S:0 MIL:50 MIL	6	500.0000			19
T260	GPU_DVO_HSYNC	GPUDVOD:G:L:S:0 MIL:50 MIL	6	500.0000			19
T261	GPU_DVO_VSYNC	GPUDVOD:G:L:S:0 MIL:50 MIL	6	500.0000			19
T262	GPU_DVO_CLKP	GPUDVOD:G:L:S:0 MIL:50 MIL	6	500.0000	165.0 MHz:::		19

T268	TMDS_CONN_CLKN	CLKCONN_TMDS	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	4	22 39
T269	TMDS_CONN_CLKP	CLKCONN_TMDS	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	4	22 39
T271	TMDS_CONN_DN<0>	CONN_TMDS_D0	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	4	22
T270	TMDS_CONN_DP<0>	CONN_TMDS_D0	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	4	22
T272	TMDS_CONN_DN<1>	CONN_TMDS_D1	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	4	22
T273	TMDS_CONN_DP<1>	CONN_TMDS_D1	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	4	22
T274	TMDS_CONN_DN<2>	CONN_TMDS_D2	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	4	22
T276	TMDS_CONN_DP<2>	CONN_TMDS_D2	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	4	22

SIGNAL CONSTRAINTS - PAGE 1

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401243	AA

SCALE: NONE

SHT 36 OF 44

Digital Signals (cont'd)

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
AGP	AGP_AD<15..0>	L:S:1050:1450	7					66 MHZ	12 19
AGP BYTES 0-1	AGP_CBE<1..0>	L:S:1050:1450	7					66 MHZ	12 19
	AGP_AD_STB<0>	L:S:1050 MIL:1450 MIL	6		(250)	8 MIL SPACING		133.0 MHZ	12 19
	AGP_AD_STB_L<0>	L:S:1050 MIL:1450 MIL	6		(250)	8 MIL SPACING		133.0 MHZ	12 19
AGP BYTES 2-3	AGP_AD<31..16>	L:S:1050:1450	7					66 MHZ	12 19
	AGP_CBE<3..2>	L:S:1050:1450	7					66 MHZ	12 19
	AGP_AD_STB<1>	L:S:1050 MIL:1450 MIL	6		(250)	8 MIL SPACING		133.0 MHZ	12 19
	AGP_AD_STB_L<1>	L:S:1050 MIL:1450 MIL	6		(250)	8 MIL SPACING		133.0 MHZ	12 19
AGP SIDEBAND	AGP_SBA<7..0>	L:S:1050:1450	7					66 MHZ	12 19
	AGP_SB_STB	L:S:1050 MIL:1450 MIL	6		(350)	8 MIL SPACING		66.00 MHZ	12 19
	AGP_SB_STB_L	L:S:1050 MIL:1450 MIL	6		(350)	8 MIL SPACING		66.00 MHZ	12 19
AGP CONTROL	AGP_FRAME_L	L:S:1250 MIL:1950 MIL	6					66.00 MHZ	12 19
	AGP_IRDY_L	L:S:1250 MIL:1950 MIL	6					66.00 MHZ	12 19
	AGP_TRDY_L	L:S:1250 MIL:1950 MIL	6					66.00 MHZ	12 19
	AGP_DEVSEL_L	L:S:1250 MIL:1950 MIL	7					66.00 MHZ	12 19
	AGP_STOP_L	L:S:1250 MIL:1950 MIL	6					66.00 MHZ	12 19
	AGP_PAR	L:S:1250 MIL:1950 MIL	6					66.00 MHZ	12 19
	AGP_REQ_L	L:S:1250 MIL:1950 MIL	6					66.00 MHZ	12 19
	AGP_GNT_L	L:S:1250 MIL:1950 MIL	6					66.00 MHZ	12 19
	AGP_RBF_L	L:S:1250 MIL:1950 MIL	6					66.00 MHZ	12 19
PCI	PCI_AD<31..0>	L:S:6000:12500				MIN_DAISY_CHAIN		33 MHZ	9 12 17 18 24 39
	PCI_CBE<3..0>	L:S:6000:12500				MIN_DAISY_CHAIN		33 MHZ	12 17 18 24
	PCI_FRAME_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ	12 17 18 24 39
	PCI_IRDY_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ	12 17 18 24 39
	PCI_TRDY_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ	12 17 18 24 39
	PCI_DEVSEL_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ	12 17 18 24 39
	PCI_STOP_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ	12 17 18 24 39
	PCI_PAR	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ	12 17 18 24 39
ULTRA ATA-100	UIDE_DATA<15..8>	L:S::710			(200)			100 MHZ	13 24
	UIDE_DATA<7>	U51_V1:RP19.3::600 MIL			(200)			100.0 MHZ	13 24
	UIDE_DATA<6..0>	L:S::600			(200)			100 MHZ	13 24
	UIDE_ADDR<2..0>	L:S::650			(200)			100 MHZ	13 24
	UIDE_RST_L	L:S::400 MIL			(200)			100.0 MHZ	13 24
	UIDE_DIOW_L	L:S::400 MIL			(200)			100.0 MHZ	13 24
	UIDE_DIOR_L	L:S::600 MIL		10 MIL SPACING	(200)			100.0 MHZ	13 24
	UIDE_DMACK_L	L:S::400 MIL			(200)			100.0 MHZ	13 24
	UIDE_CS0_L	L:S::500 MIL			(200)			100.0 MHZ	13 24
	UIDE_CS1_L	L:S::500 MIL			(200)			100.0 MHZ	13 24
	UIDE_DMARQ	L:S::400 MIL			(200)			100.0 MHZ	13
	UIDE_IOCHRDY	L:S::600 MIL		10 MIL SPACING	(200)			100.0 MHZ	13 24
	UIDE_INTRQ	L:S::400 MIL			(200)			100.0 MHZ	13
	HD_DATA<15..0>	L:S:5000:6500	7		(200)			100 MHZ	24
	HD_ADDR<2..0>	L:S:5000:6500	7		(200)			100 MHZ	24
	HD_RESET_L	L:S:4000 MIL:6000 MIL			(200)			100.0 MHZ	24
	HD_DIOW_L	L:S:3000 MIL:5200 MIL			(200)			100.0 MHZ	24
	HD_DIOR_L	L:S:6100 MIL:6150 MIL		10 MIL SPACING	(200)			100.0 MHZ	24
	HD_DMACK_L	L:S:4500 MIL:6000 MIL			(200)			100.0 MHZ	24
	HD_CS0_L	L:S:3000 MIL:6000 MIL			(200)			100.0 MHZ	24
	HD_CS1_L	L:S:3000 MIL:6000 MIL			(200)			100.0 MHZ	24
	HD_DMARQ	L:S:4500 MIL:6000 MIL			(200)			100.0 MHZ	13 24
	HD_IOCHRDY	L:S:6200 MIL:6300 MIL		10 MIL SPACING	(200)			100.0 MHZ	24
	HD_INTRQ	L:S:3000 MIL:5000 MIL						100.0 MHZ	13 24
EIDE INTREPID	EIDE_DATA<15..0>	L:S::850						33 MHZ	13 24
	EIDE_ADDR<2..0>	L:S::850						33 MHZ	13 24
	EIDE_CS0_L	L:S::850 MIL						33.00 MHZ	13 24
	EIDE_CS1_L	L:S::850 MIL						33.00 MHZ	13 24
	EIDE_RD_L	L:S::500 MIL						33.00 MHZ	13 24
	EIDE_WR_L	L:S::500 MIL						33.00 MHZ	13 24
	EIDE_IOCHRDY	L:S::500 MIL						33.00 MHZ	13 24
	EIDE_INT	L:S::500 MIL						33.00 MHZ	13 24
	EIDE_RST_L	L:S::500 MIL						33.00 MHZ	13 24
	EIDE_DMACK_L	L:S::500 MIL						33.00 MHZ	13 24
	EIDE_DMARQ	L:S::500 MIL						33.00 MHZ	13 24
OPTICAL	EIDE_OPTICAL_DATA<15..0>	L:S:4000:6000						33 MHZ	24 39
	EIDE_OPTICAL_ADDR<2..0>	L:S:4000:6000						33 MHZ	24 39
	EIDE_OPTICAL_CS0_L	L:S:4500 MIL:6500 MIL						33.00 MHZ	24 39
	EIDE_OPTICAL_CS1_L	L:S:4500 MIL:6500 MIL						33.00 MHZ	24 39
	EIDE_OPTICAL_READ_L	L:S:4500 MIL:6500 MIL						33.00 MHZ	24 39
	EIDE_OPTICAL_WR_L	L:S:4500 MIL:6500 MIL						33.00 MHZ	24 39
	EIDE_OPTICAL_IOCHRDY	L:S:4500 MIL:6500 MIL						33.00 MHZ	24 39
	EIDE_OPTICAL_INT	L:S:5000 MIL:7000 MIL						33.00 MHZ	24 39
	EIDE_OPTICAL_RST_L	L:S:4500 MIL:6500 MIL						33.00 MHZ	24 39
	EIDE_OPTICAL_DMAACK_L	L:S:4500 MIL:6500 MIL						33.00 MHZ	24 39
	EIDE_OPTICAL_DMA_RQ	L:S:4500 MIL:6500 MIL						33.00 MHZ	24 39
ETHERNET MII	ENET_LINK_RXD<7..0>	L:S:8000:9000	7	(400)		(400)			13 26
	ENET_RX_DV	L:S:8000 MIL:9000 MIL							13 26
	ENET_RX_ER	L:S:8000 MIL:9000 MIL							13 26
	ENET_PHY_TXD<7..0>	L:S:8000:9000	7	(400)		(400)			13 26
	ENET_LINK_TXD<7..0>	L:S::600							13
	ENET_PHY_TX_ER	L:S:8000 MIL:9000 MIL							13 26
	ENET_LINK_TX_ER	L:S::400 MIL							13
	ENET_PHY_TX_EN	L:S:8000 MIL:9000 MIL							13 26
	ENET_LINK_TX_EN	L:S::400 MIL							13
	ENET_MDIO	L:S:8000 MIL:9000 MIL							13 26
	ENET_MDC	L:S:8000 MIL:9000 MIL							13 26
	ENET_COL	L:S:8000 MIL:9000 MIL							13 26
	ENET_CRS	L:S:8000 MIL:9000 MIL							13 26
FIREWIRE MII	FW_LINK_DATA<7..0>	L:S:2700:3500	7	(400)		(400)			13 27
	FW_PHY_DATA<7..0>	L:S:4700:5500	7	(400)		(400)			27
	FW_LINK_CNTL<1..0>	L:S:9000:10000							13 27
	FW_PHY_CNTL<1..0>	L:S::300							27
	FW_LINK_LREQ	L:S::300 MIL							13
	FW_PHY_LREQ	L:S:8500 MIL:9500 MIL							13 27
	FW_PINT	L:S:8500 MIL:9500 MIL							13 27

NEED TO MATCH DELAY TO 250

TOTAL UIDE+HD SKEW <500MIL

PRIORITY: 4
PRIMARY LAYERS: 9
SECONDARY LAYERS: 4,7
GOAL: MINIMIZE TH VIAS

PRIORITY: 7
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 6
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 8
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 5
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 5
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR	RELATIVE_PROPAGATION_DELAY	MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS	
FIREWIRE Zo = 110	FW_TPI0N	FW_TPI0	FW_TPI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING		27 28 39
	FW_TPI0P	FW_TPI0	FW_TPI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING		27 28 39
	FW_TPO0N	FW_TPO0	FW_TPO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING		27 28 39
	FW_TPO0P	FW_TPO0	FW_TPO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING		27 28 39
	FW_TPBI0N	FW_TPBI0	FW_TPBI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING		28
	FW_TPBI0P	FW_TPBI0	FW_TPBI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING		28
	FW_TPAO0N	FW_TPAO0	FW_TPAO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING		28
	FW_TPAO0P	FW_TPAO0	FW_TPAO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING		28
	FW_TPA1N	FW_TPA1	FW_TPA1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING		27 28
	FW_TPA1P	FW_TPA1	FW_TPA1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING		27 28
	FW_TPB1N	FW_TPB1	FW_TPB1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING		27 28
	FW_TPB1P	FW_TPB1	FW_TPB1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING		27 28
	FW_TPI1N	FW_TPI1	FW_TPI1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING		28 39
	FW_TPI1P	FW_TPI1	FW_TPI1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING		28 39
	FW_TPO1N	FW_TPO1	FW_TPO1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING		28 39
	FW_TPO1P	FW_TPO1	FW_TPO1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING		28 39
ETHERNET Zo = 100	MDI_P<0>	ENET_MDI0	ENET_MDI0:G:U43.29:J23.1:0 MIL:100 MIL		ENET 10 MIL SPACING		26 39
	MDI_M<0>	ENET_MDI0	ENET_MDI0:G:U43.31:J23.2:0 MIL:100 MIL		ENET 10 MIL SPACING		26 39
	MDI_P<1>	ENET_MDI1	ENET_MDI1:G:U43.33:J23.3:0 MIL:100 MIL		ENET 10 MIL SPACING		26 39
	MDI_M<1>	ENET_MDI1	ENET_MDI1:G:U43.34:J23.4:0 MIL:100 MIL		ENET 10 MIL SPACING		26 39
	MDI_P<2>	ENET_MDI2	ENET_MDI2:G:U43.39:J23.7:0 MIL:100 MIL		ENET 10 MIL SPACING		26 39
	MDI_M<2>	ENET_MDI2	ENET_MDI2:G:U43.41:J23.8:0 MIL:100 MIL		ENET 10 MIL SPACING		26 39
	MDI_P<3>	ENET_MDI3	ENET_MDI3:G:U43.42:J23.9:0 MIL:100 MIL		ENET 10 MIL SPACING		26 39
	MDI_M<3>	ENET_MDI3	ENET_MDI3:G:U43.43:J23.10:0 MIL:100 MIL		ENET 10 MIL SPACING		26 39
LVDS Zo = 100 LOWER	CLKLVDS_LN	CLKLVDS_L	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4	20 22 39
	CLKLVDS_LP	CLKLVDS_L	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4	20 22 39
	LVDS_L0N	LVDS_L0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22 39
	LVDS_L0P	LVDS_L0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22 39
	LVDS_L1N	LVDS_L1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22 39
	LVDS_L1P	LVDS_L1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22 39
	LVDS_L2N	LVDS_L2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22 39
	LVDS_L2P	LVDS_L2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22 39
UPPER	CLKLVDS_UN	CLKLVDS_U	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4	20 22
	CLKLVDS_UP	CLKLVDS_U	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4	20 22
	LVDS_U0N	LVDS_U0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22
	LVDS_U0P	LVDS_U0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22
	LVDS_U1N	LVDS_U1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22
	LVDS_U1P	LVDS_U1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22
	LVDS_U2N	LVDS_U2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22
	LVDS_U2P	LVDS_U2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22
TMDS Zo = 100	TMDS_CLKN	CLKTMDS	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	5	19 22
	TMDS_CLKP	CLKTMDS	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	5	19 22
	TMDS_DN<0>	TMDS_D0	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19 22 39
	TMDS_DP<0>	TMDS_D0	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19 22 39
	TMDS_DN<1>	TMDS_D1	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19 22 39
	TMDS_DP<1>	TMDS_D1	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19 22 39
	TMDS_DN<2>	TMDS_D2	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19 22 39
	TMDS_DP<2>	TMDS_D2	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19 22 39
	ATI_TMDS_CLKN	ATI_CLKTMDS	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	5	20
	ATI_TMDS_CLKP	ATI_CLKTMDS	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	5	20
	ATI_TMDS_DN<0>	ATI_TMDS_D0	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	8	20
	ATI_TMDS_DP<0>	ATI_TMDS_D0	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	8	20
	ATI_TMDS_DN<1>	ATI_TMDS_D1	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	8	20
	ATI_TMDS_DP<1>	ATI_TMDS_D1	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	8	20
	ATI_TMDS_DN<2>	ATI_TMDS_D2	ATITMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	20
USB 1.1 Zo = 90	ATI_TMDS_DP<2>	ATI_TMDS_D2	ATITMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	20
	USB_DEM	USB_DE	USB_DE:G:L:S:0 MIL:200 MIL		10 MIL SPACING		14
	USB_DEP	USB_DE	USB_DE:G:L:S:0 MIL:200 MIL		10 MIL SPACING		14
	USB_DFM	USB_DF	USB_DF:G:L:S:0 MIL:200 MIL		10 MIL SPACING		14
	USB_DFP	USB_DF	USB_DF:G:L:S:0 MIL:200 MIL		10 MIL SPACING		14
USB 2.0 Zo = 90	BT_USB_DM	BT_USB_D	BT_USB:G:L:S:0 MIL:200 MIL		10 MIL SPACING		14 25 39
	BT_USB_DP	BT_USB_D	BT_USB:G:L:S:0 MIL:200 MIL		10 MIL SPACING		14 25 39
	MODEM_USB_DM	MODEM_USB_D	MODEM_USB:G:L:S:0 MIL:200 MIL		10 MIL SPACING		14 25 39
	MODEM_USB_DP	MODEM_USB_D	MODEM_USB:G:L:S:0 MIL:200 MIL		10 MIL SPACING		14 25 39
	NEC_USB_DAM	USB_D1	USB_D1:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING		17 25 39
	NEC_USB_DAP	USB_D1	USB_D1:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING		17 25 39
	NEC_USB_DBM	USB_D2	USB_D2:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING		17 25 39
	NEC_USB_DBP	USB_D2	USB_D2:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING		17 25 39
POWER SUPPLIES	1772_CSSN	1772_CSS	1772_CSS:G:L:S:0 MIL:100 MIL				30
	1772_CSSP	1772_CSS	1772_CSS:G:L:S:0 MIL:100 MIL				30
	1772_CSIN	1772_CSI	1772_CSI:G:L:S:0 MIL:100 MIL				30
	1772_CSIP	1772_CSI	1772_CSI:G:L:S:0 MIL:100 MIL				30
	3V_SNSM	3V_SNS	3V_SNS:G:L:S:0 MIL:100 MIL				32
	3V_SNSP	3V_SNS	3V_SNS:G:L:S:0 MIL:100 MIL				32
	5V_SNSM	5V_SNS	5V_SNS:G:L:S:0 MIL:100 MIL				32
	5V_SNSP	5V_SNS	5V_SNS:G:L:S:0 MIL:100 MIL				32
THERMOSTAT	THERM1_DM		THERM1:G:L:S:0 MIL:100 MIL				25
	THERM1_DP		THERM1:G:L:S:0 MIL:100 MIL				25
	THERM2_DM		THERM2:G:L:S:0 MIL:100 MIL				25
	THERM2_DP		THERM2:G:L:S:0 MIL:100 MIL				25
	THERM1_M_DM	THERM1_MAIN	THERM1_MAIN:G:L:S:0 MIL:100 MIL				25
	THERM1_M_DP	THERM1_MAIN	THERM1_MAIN:G:L:S:0 MIL:100 MIL				25
	THERM2_M_DM	THERM2_MAIN	THERM2_MAIN:G:L:S:0 MIL:100 MIL				25
	THERM2_M_DP	THERM2_MAIN	THERM2_MAIN:G:L:S:0 MIL:100 MIL				25
	THERM1_A_DM	THERM1_ALT	THERM1_ALT:G:L:S:0 MIL:100 MIL				25
	THERM1_A_DP	THERM1_ALT	THERM1_ALT:G:L:S:0 MIL:100 MIL				25
	THERM2_A_DM	THERM2_ALT	THERM2_ALT:G:L:S:0 MIL:100 MIL				25
	THERM2_A_DP	THERM2_ALT	THERM2_ALT:G:L:S:0 MIL:100 MIL				25

PRIORITY: 3
PRIMARY LAYERS: 4,7 FOR CONTROLLED IMPEDANCE DIFF PAIRS
SECONDARY LAYERS: 2,9 FOR UNCONTROLLED IMPEDANCE DIFF PAIRS

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3MIL (TRACE WIDTH)
S = 11MIL (TRACE SEPERATION)
H = 16.8MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 106.2 OHMS
Zo(single) = 55.4 OHMS

Clear adjacent power plane!
Zo will be lower due to asymmetric stackup.

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3.1MIL (TRACE WIDTH)
S = 4.9MIL (TRACE SEPERATION)
H = 9.6MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 94 OHMS
Zo(single) = 50 OHMS

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3.6MIL (TRACE WIDTH)
S = 7MIL (TRACE SEPERATION)
H = 9.6MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 89.8 OHMS
Zo(single) = 46.6 OHMS

LAYERS 2 OR 9

SIGNAL CONSTRAINTS - PAGE 2

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401243	AA
SCALE: NONE	SHT 37 OF 44	

POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
MAIN/SLEEP	+24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+BATT	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23 39
	+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	39
	+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+2_5V_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	39
	+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP_VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30 31 39
	1634 +ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30 38
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30 38
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30 39
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30 39
	1772_DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		30
	1772_LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	30
	1772_LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		30
	1772_DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		30
	1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10		30
PMU	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	+4_85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		29 31
	+4_6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10		31 32
	+4_85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		31
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		31
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		25 29
MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24 32
	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24
TRACKPAD	+5V_TPAD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=10		23 39
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		23 39
VIDEO	+14V_INV	VOLTAGE=14V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	22 39
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
AUDIO	1357 +5V_MAIN_AUD	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 32
	1356 +3V_MAIN_AUD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 32
	1358 AUD_GND	VOLTAGE=0V	MIN_LINE_WIDTH=50		25
FAN	1400 +FAN_PWR	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 39
	FAN1_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	FAN2_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39

I/O AREA
INVERTER
TRACKPAD
LVDS

CHGND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	IN
CHGND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN
CHGND3	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN
CHGND4	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN

ENET_CTAP_CHGND VOLTAGE=0V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=12

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 33 39
	CPU_AVDD	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 6 7 8 15 16 33
DDR RAM	DDR_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		11
INTREPID	1335 +2_5V_INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	9 10 15 16
	+3V_INTREPID_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14
PLLS	+1_5V_INTREPID_PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	8 12 14
	+1_5V_INTREPID_PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	8
	+1_5V_INTREPID_PLL8	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
REFERENCE	INT_MEM_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		9
	INT_AGP_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		12 19
	INT_MEM_REF_H	VOLTAGE=0V	MIN_LINE_WIDTH=10		9
	VIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8		13
AIRPORT	+3V_AIRPORT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
CARDBUS	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
ATI M10	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	19 20 39
	+3V_GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 19 20 21
	+3V_GPU_FLT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+2_5V_GPU	VOLTAGE=2.5V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	21
	GPU_MEM_IO	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	19 21
	GPU_MEM_IO_FLT	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+2_5V_GPU_MEMCORE	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+1_8V_GPU	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	19 20 21
	+1_5V_AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 15 16 19 20 21
	+2_5V_GPU_PNLIO	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_8V_ATI_PVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20 21
	+1_5V_AGP_GPU	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_5V_GPU_VDD15	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	+1_8V_GPU_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_VDDDI	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	GPU_VCORE_VDDCI	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	+2_5V_GPU_A2VDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_PNLPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_PNLIO	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+2_5V_GPU_MCLK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_AVDDQ	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_MEMPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+3V_ATI_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	+3V_ATI_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	1346 +GPU_VDD15_UF	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1347 +2_5V_SLEEP_NECK1	VOLTAGE=2.5V	MIN_LINE_WIDTH=10		20
	1348 +3V_SLEEP_NECK	VOLTAGE=3V	MIN_LINE_WIDTH=10		34
	1349 +1_5V_AGP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		20
	1350 +1_8V_PVDD_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		20
	1351 GPU_VCORE_NECK	VOLTAGE=1.2V	MIN_LINE_WIDTH=10		20
	1352 +GPU_VDD15_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		20
	1353 +2_5V_SLEEP_NECK2	VOLTAGE=2.5V	MIN_LINE_WIDTH=10		34
	1354 +1_8V_SLEEP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		34
	1355 +1_5V_SLEEP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		34
	1360 +1_8V_ATI_TPVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	1361 +1_8V_GPU_TP_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
ETHERNET 88E1111 NEC USB2.0	+2_5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+2_5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+1_0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	1616 +3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
	1617 NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	17
FW	1602 LM2594_IN	VOLTAGE=33V	MIN_LINE_WIDTH=40	MIN_NECK_WIDTH=12	27
	1611 +FW_PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	+FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	1645 +FW_AMP_SENSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	
	+FW_PWR_OR	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	27 28
	1610 +FW_PWR1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	+FW_VP0	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28 39
	+FW_VP1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28 39
	+3V_FW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27 28
	+3V_FW_UF	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_PLLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	1615 FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	1650 FW_VDD_ON	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	1625_VSW	VOLTAGE=14V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+PBUS_JUMPER	VOLTAGE=14V	MIN_LINE_WIDTH=10		31
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		31
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		31
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		31
	1V20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	30 31
LTC3707 5V SWITCHER	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	32
	5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+5V_MAIN_JUMPER	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
3V SWITCHER	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+3V_MAIN_JUMPER	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		32
MAX1715 2.5V SWITCHER	2_5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	34
	2_5V_LX_F	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	34
	2_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	2_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	2_5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	2_5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
1.65V SWITCHER	1_5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8		34
	1_5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	34
	1_5V_LX_F	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	34
	1_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	1_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	1_5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	1_5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
CONTROL	1_5V_ILIM		MIN_LINE_WIDTH=8		34
	2_5V_ILIM		MIN_LINE_WIDTH=8		34
	MAX1715_TON		MIN_LINE_WIDTH=8		34
	MAX1715_SKIP		MIN_LINE_WIDTH=8		34
	MAX1715_REF	VOLTAGE=2.0V	MIN_LINE_WIDTH=8		34
	MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
MAX1717	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	33
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=200	MIN_NECK_WIDTH=10	33
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	33
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	33
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	33
	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	33
	VCORE_ILIM		MIN_LINE_WIDTH=8		33
	VCORE_REF		MIN_LINE_WIDTH=8		33
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8		33
	VCORE_CC		MIN_LINE_WIDTH=8		33
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		33 39
	VCORE_TIME		MIN_LINE_WIDTH=8		33
	VCORE_VGATE		MIN_LINE_WIDTH=8		14 33
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30		33
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8		33
	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		33
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8		33
	1315 VCORE_GNDA	VOLTAGE=0V	MIN_LINE_WIDTH=10		33
LTC1778	1778_VIN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1778_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1778_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	20
	1778_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	20
	1778_BST_RC	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	20
	1778_TG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1778_BG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	GPU_VCORE_SW	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	20
	GPU_VCORE_SW_F	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	20
	1778_ION		MIN_LINE_WIDTH=8		20
	1778_ITH		MIN_LINE_WIDTH=8		20
	1778_ITH_RC		MIN_LINE_WIDTH=8		20
	1778_VFB		MIN_LINE_WIDTH=8		20 39
	1778_FCB		MIN_LINE_WIDTH=8		20
	1778_VRNG		MIN_LINE_WIDTH=8		20
LTC3411	LTC3411_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	LTC3411_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
	1_8V_SW	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
	1_8V_SW_F	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
	1_8V_VFB		MIN_LINE_WIDTH=8		34
	LTC3411_ITH_RC		MIN_LINE_WIDTH=8		34
	LTC3411_ITH		MIN_LINE_WIDTH=8		34
	LTC3411_SYNC		MIN_LINE_WIDTH=8		34
LTC1962 INT PLLS	LTC3411_SHDN		MIN_LINE_WIDTH=8		34
	LTC1962_INT_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	14

SIGNAL CONSTRAINTS - PAGE 3

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401243	AA
SCALE: NONE	SHT 38 OF 44	

FUNCTIONAL TEST POINTS

PROBES ARE ON BOTTOM SIDE. MINIMUM PAD/HOLE SIZE IS 25 MIL.

FUNC_TEST IS ONLY PROPERTY USED BY THE TOOLS. FUNC_QTY IS FOR REFERENCE AND LISTS THE NUMBER OF TEST POINTS ON THAT NET AND WITHIN THAT GROUP/CONNECTOR. FUNC_DIST IS SIMILARLY USED TO DEFINE MAXIMUM DISTANCE FROM A CONNECTOR.

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
SCAN/TEST	JTAG_ASIC_TMS	TRUE			13 26
	JTAG_ASIC_TDI	TRUE			13
	JTAG_ASIC_TDO_TP	TRUE			26
	JTAG_ASIC_TCK	TRUE			13 26
	JTAG_ASIC_TRST_L	TRUE			13 26
	CPU_CHKSTP_OUT_L	TRUE			5
	CPU_SRESET_L	TRUE			5
	CPU_HRESET_L	TRUE			5 6 7
	JTAG_CPU_TMS	TRUE			5 6
	JTAG_CPU_TDI	TRUE			5 6
	JTAG_CPU_TDO_TP	TRUE			5
	JTAG_CPU_TCK	TRUE			5 6
	JTAG_CPU_TRST_L	TRUE			5 6
	INT_JTAG_TEI	TRUE			13
	INT_TST_MONIN_PD	TRUE			13
	INT_TST_MONOUT_TP	TRUE			13
	INT_TST_PLLEN_PD	TRUE			13
INT I2C	INT_I2C_CLK0	TRUE			6 11 13 23
	INT_I2C_DATA0	TRUE			6 11 13 23
	INT_I2C_CLK1	TRUE			13 14 25
	INT_I2C_DATA1	TRUE			13 14 25
PWR/GND	+PBUS	TRUE			38
	+24V_PBUS	TRUE			38
	GPU_VCORE	TRUE			19 20 38
	1778_VFB	TRUE			20 38
	CPU_VCORE_SLEEP	TRUE			5 33 38
	VCORE_FB	TRUE			33 38
	+1_8V_MAIN	TRUE			38
	+2_5V_MAIN	TRUE			38
	+5V_MAIN	TRUE	2		38 39
	+5V_SLEEP	TRUE	2		38 39
	+3V_MAIN	TRUE	4		23 38
		TRUE		1000	IN
	+3V_PMU	TRUE			38
CARDBUS	CBUS_DET_1_L	TRUE		2000	18
DVI	CBUS_DET_2_L	TRUE		2000	18
	TMDS_DN<0..2>	TRUE		1000	19 22 37
	TMDS_DP<0..2>	TRUE		1000	19 22 37
	TMDS_CONN_CLKN	TRUE		1000	22 36
	TMDS_CONN_CLKP	TRUE		1000	22 36
	VGA_R	TRUE		1000	22
	VGA_G	TRUE		1000	22
	VGA_B	TRUE		1000	22
	VGA_HSYNC	TRUE		1000	22
	VGA_VSYNC	TRUE		1000	22
	DVI_DDC_CLK_UF	TRUE		1000	22
	DVI_DDC_DATA_UF	TRUE		1000	22
	DVI_HPD_UF	TRUE		1000	22
	+5V_DDC_SLEEP	TRUE		2000	22 38
		TRUE	2	2000	IN
CHGND1		TRUE	6	1000	IN
LVDS	LVDS_L0N	TRUE		1000	20 22 37
	LVDS_L0P	TRUE		1000	20 22 37
	LVDS_L1N	TRUE		1000	20 22 37
	LVDS_L1P	TRUE		1000	20 22 37
	LVDS_L2N	TRUE		1000	20 22 37
	LVDS_L2P	TRUE		1000	20 22 37
	CLKLVDS_LN	TRUE		1000	20 22 37
	CLKLVDS_LP	TRUE		1000	20 22 37
	LVDS_DDC_CLK	TRUE		1000	20 22
	LVDS_DDC_DATA	TRUE		1000	20 22
	+3V_LCD	TRUE	2	2000	22 38
	+3V_SLEEP	TRUE		2000	38 39
		TRUE	2	2000	IN
CHGND4		TRUE	6	1000	IN
INVERTER	+14V_INV	TRUE		2000	22 38
	+5V_INV_SW	TRUE		2000	22 38
	BRIGHT_PWM	TRUE		2000	22
	INV_GND	TRUE		2000	22
		TRUE		1000	IN
S-VIDEO	TV_C	TRUE		2000	22
	TV_Y	TRUE		2000	22
	TV_COMP	TRUE		2000	22
	TV_GND1	TRUE		2000	22 38
	TV_GND2	TRUE		2000	22 38
LIO	INT_I2S0_SND_TO_DAC	TRUE		1000	14 25
	INT_I2S0_SND_LRCLK	TRUE		1000	14 25
	INT_I2S0_SND_MCLK	TRUE		1000	14 25 35
	INT_I2S0_SND_SCLK	TRUE		1000	14 25
	INT_I2S0_SND_FROM_ADC	TRUE		1000	14 25
	SND_HP_MUTE_L	TRUE		1000	14 25
	SND_AMP_MUTE	TRUE		1000	25
	SND_HW_RESET_L	TRUE		1000	14 25
	SND_HP_SENSE_L	TRUE		1000	14 25
	SND_LIN_SENSE_L	TRUE		1000	14 25
	INT_I2C_CLK2	TRUE		1000	14 25
	INT_I2C_DATA2	TRUE		1000	14 25
	ADAPTER_DET	TRUE		1000	25 29
	CHARGE_LED_L	TRUE		1000	25 29
	NEC_LUSB_OCI_UF	TRUE		1000	17 25
	NEC_LUSB_PPON	TRUE		1000	17 25
	+5V_MAIN	TRUE	2	2000	38 39
	+5V_SLEEP	TRUE	2	3000	38 39
	+3V_SLEEP	TRUE		2000	38 39

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
USB	NEC_USB_DAM	TRUE			17 25 37
	NEC_USB_DAP	TRUE			17 25 37
	NEC_USB_DBM	TRUE			17 25 37
	NEC_USB_DBP	TRUE			17 25 37
	BT_USB_DM	TRUE			14 25 37
	BT_USB_DP	TRUE			14 25 37
	MODEM_USB_DM	TRUE			14 25 37
	MODEM_USB_DP	TRUE			14 25 37
RT. USB	NEC_RUSB_PPON	TRUE			17 25
	NEC_RUSB_OCI_UF	TRUE			17 25
WIRELESS	PCI_AD<0..31>	TRUE		1000	9 12 17 18 24 37
	PCI_FRAME_L	TRUE		1000	12 17 18 24 37
	PCI_TRDY_L	TRUE		1000	12 17 18 24 37
	PCI_IRDY_L	TRUE		1000	12 17 18 24 37
	PCI_DEVSEL_L	TRUE		1000	12 17 18 24 37
	PCI_STOP_L	TRUE		1000	12 17 18 24 37
	PCI_PAR	TRUE		1000	12 17 18 24 37
	AIRPORT_PCI_REQ_L	TRUE		1000	12 24
	AIRPORT_PCI_GNT_L	TRUE		1000	12 24
	AIRPORT_PCI_INT_L	TRUE		1000	14 24
	MAIN_RESET_L	TRUE		1000	14 17 18 19 24 29
	CLK33M_AIRPORT	TRUE		1000	12 24 35
	PMU_PME_L	TRUE		1000	14 17 24 29
	ROM_ONBOARD_CS_L	TRUE		1000	9 24
	ROM_OE_L	TRUE		1000	9 12 24
	ROM_CS_L	TRUE		1000	9 12 24
	ROM_RW_L	TRUE		1000	9 12 24
	RF_DISABLE_L	TRUE		1000	24
	AIRPORT_CLKRUN_L	TRUE		1000	24
	+3V_AIRPORT	TRUE	4	2000	38
		TRUE	6	1000	IN
OPTICAL	EIDE_OPTICAL_DATA<0..15>	TRUE		2000	24 37
	EIDE_OPTICAL_DMA_RQ	TRUE		2000	24 37
	EIDE_OPTICAL_READ_L	TRUE		2000	24 37
	EIDE_OPTICAL_DMAACK_L	TRUE		2000	24 37
	EIDE_OPTICAL_ADDR<0..2>	TRUE		2000	24 37
	EIDE_OPTICAL_CS0_L	TRUE		2000	24 37
	EIDE_OPTICAL_CS1_L	TRUE		2000	24 37
	EIDE_OPTICAL_RST_L	TRUE		2000	24 37
	EIDE_OPTICAL_WR_L	TRUE		2000	24 37
	EIDE_OPTICAL_IOCHRDY	TRUE		2000	24 37
	EIDE_OPTICAL_INT	TRUE		2000	24 37
TRACKPAD	+5V_TPAD_SLEEP	TRUE		3000	23 38
	TPAD_F_TXD	TRUE		3000	23
	TPAD_F_RXD	TRUE		3000	23
	LID_CLOSED_L	TRUE		3000	23
	+3V_HALL_EFFECT	TRUE		3000	23 38
	SOFT_PWR_ON_L	TRUE		3000	22 23 29 33
MODEM/ SERIAL	COMM_RESET_L	TRUE		4000	14 25
	COMM_SHUTDOWN	TRUE		4000	14 25
	COMM_RING_DET_L	TRUE		4000	14 25 29
	COMM_TXD_L	TRUE		4000	14 25
	COMM_TRXC	TRUE		4000	14 25
	COMM_GPIO_L	TRUE		4000	14 25
	COMM_DTR_L	TRUE		4000	14 25
	COMM_RTS_L	TRUE		4000	14 25
	COMM_RXD	TRUE		4000	14 25
KEYBOARD	KBD_ID	TRUE		3000	23 29
	KBD_INTL	TRUE		3000	23
	KBD_JIS	TRUE		3000	23
	KBD_CAPSLOCK_LED	TRUE		3000	23
	KBD_NUMLOCK_LED	TRUE		3000	23
	KBD_FUNCTION_L	TRUE		3000	23 29
	KBD_COMMAND_L	TRUE		3000	23 29
	KBD_OPTION_L	TRUE		3000	23 29
	KBD_CONTROL_L	TRUE		3000	23 29
	KBD_SHIFT_L	TRUE		3000	23 29
	KBD_X<0..9>	TRUE		3000	23 29
	KBD_Y<0..7>	TRUE		3000	23 29
BATTERY	+BATT_POS	TRUE	(100 MIL PROBE PREFERRED)	1000	30 38
	BATT_NEG	TRUE	(100 MIL PROBE PREFERRED)	1000	30 38
	BATT_CLK	TRUE		1000	30
	BATT_DATA	TRUE		1000	30
	PMU_BATT_DET_L	TRUE		1000	29 30
FANS	+FAN_PWR	TRUE		3000	25 38
	FAN1_TACH	TRUE		3000	25
	FAN2_TACH	TRUE		3000	25
	FAN1_GND	TRUE		3000	38
	FAN2_GND	TRUE		3000	38
ETHERNET	MDI_P<0..3>	TRUE		1000	26 37
	MDI_M<0..3>	TRUE		1000	26 37
FIREWIRE	FW_TPO0P	TRUE		1000	27 28 37
	FW_TPO0N	TRUE		1000	27 28 37
	FW_TPO0R	TRUE		1000	28
	FW_TPI0P	TRUE		1000	27 28 37
	FW_TPI0N	TRUE		1000	27 28 37
	+FW_VP0	TRUE		1000	28 38
	FW_VGND	TRUE		1000	39

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
FIREWIRE (CONT.)	FW_TPO1P	TRUE		1000	28 37
	FW_TPO1N	TRUE		1000	28 37
	FW_TPI1P	TRUE		1000	28 37
	FW_TPI1N	TRUE		1000	28 37
	+FW_VP1	TRUE		1000	28 38
	FW_VGND	TRUE		1000	39
DC PWR IN	+ADAPTER	TRUE	3 (100 MIL PROBE PREFERRED)	1000	30 31 38
LMU/ALS	ST7_SLEEP_LED_H	TRUE			23
	PMU_SLEEP_LED	TRUE			23
	PMU_LID_CLOSED_L	TRUE			23 29
	LMU_DETECT	TRUE			23
		TRUE	6	1000	IN
MISC.	SLEEP_LED	TRUE	(100 MIL PROBE PREFERRED)		23
	PMU_KB_RESET_L	TRUE			29
	SLEEP	TRUE			23 25 29 32 34
	PMU_CPU_HRESET_L	TRUE			6 29
	BB_RESET_L	TRUE			6
	+3V_PMU_RESET	TRUE			29 33

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401243	AA
SCALE: NONE	SHT 39 OF 44	

REVISION HISTORY

Proto Release

7/22/02 - Initial acquisition of schematic (from 051-6278 Rev 01)
Added P59 SO-DIMM connector as placeholder (p.12)
Added P59 LVDS connector as placeholder (p.22)
Changed J9 to 10 pin Elco connector for modem (p.25)
Changed PBUS holdup caps to P59 electrolytic cans (p.30)
7/23/02 - Removed L3 (p.8)
Replaced processor with 360 pin Apollo (p.5,6)
7/24/02 - Added FETs between battery and PBUS rails for airline power (p.29)
8/10/02 - Added USB 2.0 (p.18)
8/20/02 - Removed spare pullup straps for Intrepid (p.9)
Removed USB overcurrent protection [to be placed on other boards] (p.18)
Changed right USB board connector to 16 pin Hirose connector (p.26)
Changed LIO board connector to 40 pin Molex connector (p.26)
Added 6 bypass caps to MAXBUS_SLEEP and CPU_VCORE_SLEEP (p.5)
8/26/02 - Removed 32 bypass caps for +3V_MAIN at Intrepid (p.16)
Removed 5 bypass caps for +2.5V_MAIN at Intrepid (p.16)
Removed 3 bypass caps for +1.5V_AGP at Intrepid (p.16)
Removed 4 bypass caps for MAXBUS_MAIN at Intrepid (p.16)
8/27/02 - Changed main battery connector to BP24067-R1, which is close to final (p.29)
8/29/02 - Added dedicated Boot Banger circuit (p.6)
Added 5 bypass caps to each SO-DIMM connector (p.11)
Added quad voltage circuit for bus slewing architecture (p.32)
8/30/02 - Changed to low profile 32.768kHz crystal for PMU (p.28)
Changed to Q11 adpater detection scheme (p.28)
9/03/02 - Corrected upper LVDS single pin nets (p.20)
Removed unintentional extra pulldown resistor at Intrepid (p.14)
9/17/02 - Numerous changes to stay in sync with P84 (all)
9/18/02 - Changed battery connector back to P84 part (p.29)
Added LMU circuitry to eliminate extra board (p.23)
Changed to P84 dual channel LVDS connector to reduce I2R cable losses(p.22)
9/19/02 - Removed unnecessary battery FETs [due to 3S only design] (p.29)
Modified chassis gnds on some components (all)
Removed LMU connector (p.23)
Corrected battery connector [same as P84] (p.29)
Removed P93 support (p.25)
Removed second fuse from FW ports [single fuse provides adequate power] (p.27)
9/23/02 - Replaced BCM5421 with Marvell 88E1111 (p.26)
Increased MAX_VIA_COUNT by two on most nets with this constraint for uVia (p.34,35)
9/27/02 - Corrected cpu, memory bus constraints to match manhattan lengths (p.34)
Swapped pins on L33, L35 for layout (p.31)
Changed Y6 to smaller form-factor crystal (p.26)
9/30/02 - Changed J19 (DC-in) to proper 4-pin connector (p.29)
Corrected holes and chassis gnds (p.4,all)
10/01/02 - Removed Intrepid 1.x specific circuitry (p.13)
10/03/02 - Numerous pin-swaps to accomodate board layout (all)
10/08/02 - Added page for functional test points (p.37)
10/09/02 - Changed 16 pin connectors (modem and right USB) to Foxconn parts (p.23)
10/10/02 - Clamped NEC NC pins high per documentation (p.17)
Added 10K pullup to CG_ADDRSEL and 10K pulldown to CG_FSEL on CY28512 (p.14)
Added R5CG/NO_S5CG stuffing options for CY28512 circuit (p.14)
Removed CPU_VGATE pullup to 5V to eliminate potential 3V/5V current path (p.32)
Removed Zebra 15/18 support per P84 (p.27)
Added second FW port power fuse (p.27)
Removed INT_CPUFB_IN cap per P84 (p.8)
Replaced IRF7822 FETs with IRF7811W in battery charger and 14V PBUS switchers (p.29,30)
Renamed optical interface for consistency (p.24,37)
Corrected PLL_CFG<4> for Apollo 7 (needs to always be zero) (p.5,7)
Removed temporary P84 constraints and finished up AGP clock changes (p.12,34)
Added stuffing options to power fans off 3V or 5V (p.25)
10/11/02 - Replaced DVI EMI caps with 0201 versions (p.22)
10/14/02 - Changed J18 to RJ45 with integrated magnetics (p.26)
10/15/02 - Moved Firewire connectors and port power switch to separate page (p.28)
Changed SMBus pullups to 7.15K, 1% as per iBooks/P84 [involved component net swaps] (p.29)
Added 0603 resistors as shorting pads for power up and reset (p.23)
Changed INT_MOD_SYNC, INT_MOD_DTI and INT_MOD_BITCLK to pulldowns per ERS [LA clk not used] (p.14)
Added damping resistor option to LMU crystal (p.23)
Changed INT_TST_PLLEN PD to pulldown only [LA_clk not used] (p.13)
Changed JTAG_ENET_TDI to pullup [LA_clk not used] (p.13)
Removed FW_LKON from Intrepid EXTINT3 [no longer used], pullup added (p.14)
Changed BBANG_HRESET_L pullup to 3V_SLEEP (p.6)
Changed FW_PC_PD, FW_PC_PU resistors to 5% (p.27)
Added 1K pulldown and net FW_PD2 to FW_PHY (p.27)
10/16/02 - Implemented new FW power switch and current limit (p.28)
Renamed +14V_PBUS to +PBUS (p.all)
Added A29 adapter detection circuit (p.29)
Added +PBUS current limiting circuit, removed battery charging current limit circuit (p.30)
Changed FW_PHY_PWR_DS1 to pull3 to make Port 1 1394a only (p.27)
10/21/02 - Updated CY28512 clock chip to Rev B (p.14)
Changed keyboard ZIF to large SMK connector (p.23)
Added full support for non-zero CPU_PLL_CFG<4> in run state (p.7)
10/22/02 - Mirrored wireless connector for P50 flex (p.24)
10/23/02 - Changed LMU/sleep LED interface per p84 (p.23)
Changed LMU JTAG/I2C pinout/pullup/pulldown strategy per P84 (p.23)
Changed fan FETs to SI3446DV per P84 (p.25)
Pinned out audio connector (p.25)
Pinned out right USB connector (p.25)
Pinned out modem connector (p.25)
Added 2 functional test points to wireless connector (p.24,38)
Renamed FW low voltage power rails (p.27,37)
Renamed Vcore VID nets to be consistent with P84 (p.33)
Removed redundancy in DDR memory constraints (p.35)
10/24/02 - Changed FW_DS2 strap to pull3 [Port 2 (p.27)
Cleaned up CY28512B circuit as per P84 (powered off main, output divider and strap tweaks] (p.14)
Updated PCI clock series R values per P84 (p.12)
Changed power rail for ALS to +3V_MAIN per P84 (p.23)
Added 8 ohm short and bypass cap for GPU VDDQ10 per P84 (p.21,37)
Split FW_VDN0 into FW_VGND0 and FW_VGND1 (p.28,37)
Added TP nets to GPU for XOR-tree testing (p.19-21)
Changed fan PWM output pullups to +3V_SLEEP to prevent pump-up (p.25)
10/28/02 - Added FW thermal pad ground hole back in (p.27)
Repinned LMU pulldown for layout (p.23)
10/30/02 - Changed fan power rails to common net (p.25)
10/31/02 - Removed MLB ALS (p.23)
Added wireless RF_DISABLE_L pullup and AIRPORT_CLKRUN_L pulldown (p.24)
11/05/02 - Added 6 decoupling caps to CPU_VCORE_SLEEP (p.5)
Broke out quad OR-gate to discrete components for better placement (p.22,29)
11/06/02 - Changed 10 uF FW current limit output cap to two 4.7 uF caps (p.28)
Added 3 decoupling caps to CPU_VCORE_SLEEP (p.5)
Added 9 decoupling caps to each of +5V_MAIN and +3V_MAIN (p.32)
Removed XW1 jumper for CPU_VCORE_SLEEP (p.33)
Added decoupling cap to PMU reset OR gates (p.29)
11/08/02 - Changed Firewire PHY to Z17 (p.27)
Added bulk caps to fan connectors (p.25)
Added alternate chassis gnd connection for sleep LED (p.23)
11/11/02 - Removed +3V_MAIN option for P50 card (p.24)
11/13/02 - Removed LMU and associated circuitry (p.23)
11/21/02 - Implemented D3cold for all PCI devices (p.12,14,18)
11/25/02 - Renamed all components (all pages)
11/26/02 - Removed chokes from 1394b data pairs (p.27,28)

EVT RELEASE

12/13/02 - Added 12 pF caps to source of 33MHz PCI clocks since they can not be buried (p.12)
Replaced ADM1031 with ADT7460 [I2C Address Change!] (p.25)
Added ADT7460 hookups to GPU thermal diode (p.21,25)
Added Firewire 8 ESD protection circuits (p.28)
12/16/02 - Removed hole from Firewire ground pad (p.27)
DDR memory connector renamed to J25 (p.11)
12/20/02 - Removed LT4210 from Firewire port power (p.28)
Added F10,F29 as placeholders and experiment guides (p.28)
Added diodes to OR +5V_SLEEP into FW_PHY power supply (p.27)
12/26/02 - Updated CPU p/ns to production p/ns (p.5)
Removed RC glitch filter on CPU_DRDY_L (p.5,36)
Updated PCI source clock and internal spreading straps (p.8)
Changed BootROM PWD signal to INT_RESET_L per P84 (p.9)
Added CKE pulldowns per P84 (p.9)
Updated Ethernet series Rs per P84 [Clocks to 10 ohms, data to 22 ohms] (p.13)
Updated SSCG/NO_SSCG BOM options (p.14)
Renamed line-in and headphone sense lines to reflect active low signals (p.14,25.39)
Added 0 ohm Rs to make 5V_Intrepid rail hot or cold (p.15.16,38)
NO STUFFed enable for 1.5V LDO circuit (p.15)
Stuffed USB OC1/PPON filters for 8 time constant due to new port current limiters] (p.17)
Renamed USB OC1/PPON signals for left/right ports (p.17,39)
Updated GPU VCore to stay in sync with P84 [Jitter improvement] (p.20)
Added EMI caps to LVDS_DDC_CLK, INT_I2S0_SND_MCLK, INT_I2S0_SND_SCLK per P84 (p.22,25)
Added R800,R801 for eventual thermal diode in CPU (p.25)
Renamed R2009 to R799, R2001 to R802, R2002 to R803 (p.25)
Renamed F10 to F1, F20 to F2 [deleted old F1,F2] (p.28)
Added caps to FW ESD circuit that were missed (p.28)
Changed MAX4172 power source to save current on battery [per P84] (p.30)
Updated 1.5V/2.5V switcher BOM to stay in sync with P84 [FET change and current limits] (p.34)
Replaced all 1325i061 [1uF,0805,10V,20%] with 1325P046 [1uF,0603,10V,20%] (p.14,15,27,30,33,34)
Replaced all 1385B351 [1uF,0603,6.3V,10%] with 1325P046 [1uF,0603,10V,20%] (p.27,30)
01/02/03 - Updated Firewire fuse topology to that of P84 (p.28)
Updated system and power block diagrams (p.2,3)
01/03/03 - Corrected +2.5V_INTREPID connections to muxes and reference (p.9,10)
01/07/03 - Added NO_TEST nets to pads of DDR connector arms (p.11)
01/08/03 - Added 2N7002 circuits to ensure speakers are muted during power-up (p.25)
Changed R164 to 511 ohms to avoid low CPU clock amplitude (p.8)
01/09/03 - Added required pulldown to output of DVI HPD sense comparator (p.22)
Swapped R443 and R444 values to ensure Vgs < -4.5V (p.28)
Updated S-video filter values to those of P84 (p.22)
01/10/03 - Z77,Z723,Z761,Z776,Z789,Z787,Z722,Z738,Z760,Z742 & Z717 are changed to HOLE-VIA-20R10 (p.4)
01/13/03 - Add L53, L54, L55 for TMDS Data<0:2> Diff Pair (p.22)
01/14/03 - Add C812 - C821 (Totol 10 0.22uF caps) for 2.5V Intrepid Decoupling (p.16)
Add C822 & C823 at Wireless Card connector MAIN_RESET_L & RF_DISABLE_L_SPN (p.24)
Change MATCHED_DELAY to 50 for all TMDS DIFF PAIR (p.37)
Change MATCHED_DELAY to 50 for all TMDS DIFF PAIR (p.37)
Add R810 & R811 for ALWAYS-ON FANs in Acrylic Build (p.25)
01/28/03 - Remove NV31/17 components (p.19-21)
Add M10 (p.19-21)
02/07/03 - Add Power Net Constraints for M10 (p.38)
Replace Singing PBus Cap C49,C50,C67,C68,C80,C81,C95,C96,C108,C109,C120,C121 with 12G30035 (or alt. 12G50036) (p.33)
02/11/03 - Add FW Power Net Constraints (p.36)
Change signal constraints for AGP signals (p.36)
Add LMU connector and components (p.23)
Edit I2C table for LMU (p.13)
Change R500 to 19.6K (p.14)
Connect Clock Slewing RESET# to MAIN_RESET_L (p.14)
Change Ferrite Bean of ATI power supply to correct values (p.21)
Remove C141 PBUS CAP (p.31)
02/12/03 - Change and Rotate Keyboard Connector (p.23)
Add ATI Power sequencing Circuit for M10 Power-up and Power-down (p.19-22, p.32-35)

EVT RELEASE (continue)

02/13/03 - Add C825 (p.30)
02/17/03 - Rename all Reference Designators

EVT ENCLOSURE RELEASE

03/13/03 - Change 3-P FAN connectors to 4-P (p.25)
Add PU at PMU_SLEEP_LED_L for LMU (p.23)
Change stuffing option for clock slewing & PLL5 (p.14)
Change ATI M10 GPIO8 to Pull-down (p.20)
Remove Memory MUX 0ohm Resistors (p.10)
03/28/03 - Due to MLB outline change at DVI connector, CHGND1 has to be splitted into CHGND1 & CHGND2 (P 4 & 22)
Separate +3V and +5V traces running from 3/5V supply to 40Pin LIO connector (P 25 & 32)
R603 change from 100K to 4.7K (P 29)
Change airline detect to 13.1V or greater, R40 and R690 to 97.6K ohm (P 30 & 31)
Add C826 at U3 RS- pin (P 30)
Change D3 to 1N914 PN Junction Diode(P 31)
03/31/03 - Change AGPTEST Pull-up to 47ohm (it was 40ohm) (P 20)
Add circuits to prevent start-up Headphone POP (P 25)
Change all 1210 4.7uF to 1206 4.7uF Cap (13850931) (various pages)
Modify FAN circuit to PWM active low signal (P25)
04/08/03 - Add SOFT_MODEM_support (P 14 & 25)
Add 10-Pin ELCO connector for Serial Debug Interface (P 25)
Change Q7 from SI4435DY to SUD45P03-10 (P 30)
Remove D34 RS3AB (P 30)
04/11/03 - Change FW Schottky Diode to a 3A part 371S0159 (P 28)
Change PBUS L69 and VCORE L71 Inductor (P 31 & 33)
Change C643 10uF Cap to 1206 package part (P 28)
Change all 6 VCORE Caps to 220uF Al Poly Cap 128S0024 (P 33)
Add Mitsumi MM1571J regulator to provide 1.8V TPVDD (P 21)
Change U34 to Mitsumi MM1571J part for ATI PLL 1.8V rail(P 21)
04/16/03 - Add FW Port ShutDown/PowerOn Circuit (P 28)
Change the I2C Pull-up for Sound/Modem to 1K ohm (P 14)
04/17/03 - Change 3V/5V inductors (152S0137) L61 & L62 (P 32)
04/21/03 - Add 12 ICT JTAG TEST PADs (P 39)
04/23/03 - Invert ATI GPIO15 signal, no stuff pull-up resistor (P 20)
Combine Q35 and Q36 into a Dual Package Part (P 22)
SWAP the ADT7460 Temperature Sense pair (P 25)
Change FW PHY to production part (P 26)
04/24/03 - Remove +3V_CBUS_SLEEP and US, use +3V_SLEEP directly (P 14,18,24)
Add 0402 Res between ATI PVDD/TPVDD rail and 10uF caps for stability purpose (P 21)
Add 90ohm common mode choke at TMDS data <0..2> pairs (P 22)
Add Sense Resistor to Vcore power rail, remove one 220uF cap <back to EVTA design> (P 33)
04/25/03 - Change C826 to 0.01uF 50V Cap (P 30)
04/30/03 - No stuff R676 to prevent +3V rail leakage (P 33)
05/02/03 - L45,L46,L47 is using Common Mode Choke TDK ACM2012D Part, will replace with ACM2012H Part if available (P 22)

DVT RELEASE

05/21/03 - Swap +PBUS and +24V_PBUS at Backup Battery Connector - J16 (P.31)
05/27/03 - Change R931 to 4.7K for I2C timing specification (P.13)
Change Q62 & Q65 to SI7308DP part (P.33)
Change Q60, Q63 & Q66 to IRF7832 part and split C102 into 3 10pF caps (P.33)
Enable Vcore Burst(Skip) Mode by no stuffing R67 (P.33)
Enable 3V/5V Burst Mode by changing R406 & R407 to 100K ohm (P.32)
Change Q48 to SI7090DP part (P.20)
Change Q49 to IRF7832 part (P.20)
Enable GPUcore Burst Mode by changing R358 to 2.2 ohm, no stuffing R344 and stuffing R343 (P.20)
Reduce audible noise by changing L64 to 152S0139 (P.20)
Add C838, C840, C839, C844 & C845 10pF caps near the power switchers FETs (P.20, 32 & 34)
Change PWM_L_Fan input (both L&R Fans) to +5V_SLEEP pull-up (P.25)
05/30/03 - Connect SLEEP_LED_DGND to digital ground instead of CHGNDS (P.23)
06/03/03 - Add CPU Core Voltage offset option circuit (P.33)
GPU Vcore on/off timing (P.20)
06/05/03 - Change FW-B connector to 614S0058 with internal shield pins (P.28)
06/06/03 - Add four 0ohm jumper, in case there is no sw support for the multi-stage VCore (P.38)
Change the +2.5V_Sleep FET to reduce Voltage drop on the rail (P.34)
06/12/03 - Change CBUS & USB2_REQ_LINE Pullup to +3V_MAIN (P.12)
Add 0 ohm at USB AVSS_GND (P.17)
Change TMDS common mode choke to TDK ACM2012-900H part (P.22)
Change HD_DMACK_L pullup R213 to 10K (P.24)
Add C847, C851 & C852 at ENET CLK for EMC (P.13 & 26)
Change Q34 to FDS3672 (P.28)
Change Q82 pin#4 connection to system digital GND (P.33)
Add C848 150uF cap at J3 for +5V_MAIN USB2 power (P.25)
Add C853 1000pF cap at Q64 (P.30)
Add RC at ADT7460 power rail for noise isolation (P.25)
Isolate THERM# signal at ADT7460 by using double inverters for THERM_L_OC (P.25)
Remove redundant pullup R601 for THERM_L_OC (P.29)
Remove SH2 EMI spring at CHGNDS (P.23)
Add additional PWR/GND pins at J17 for R-USB board (P.25)
06/13/03 - New SODIMM connector with 4 through-hole mounting pins (P.11)
Change CPU config stuffing option at R63 and R64 (P.7)
Stuff R288 for Cypress clk chip (P.14)
Move CBUS_PCI_REQ_L back to +3V_SLEEP rail pull-up (P.12)
Change the TMDS Termination Resistor values to 162ohm (P.20)
Connect C847 at R160.1 (P.13)
Add 1000pF caps at ADT7460 D_plus/minus pairs (P.25)
Add SiI162 DVI transmitter to prevent leakage from DVI connector to the system (P.19&20)
06/16/03 - Replace C705,C707,C711,C703 & C685 with part 128S0025 (P.20&32)
Remove R771 0ohm resistor (P.34)
Edit Signal Constraints for TMDS routing and ENET routing (P.36&37)

DVT2 RELEASE

07/06/03 - Change R97 & R98 to 0402 package (P.33)
No Stuff R835 (P.19)
Change R198 to 100K ohm resistor (P.23)
Add Common Mode Choke L77 & L76 at FW8 pairs (P.28)
Removed current monitoring IC for firewire port power (P.28)
Changed RP52,RP53,RP56,RP57 to 22ohm for EMI (P.19)

PRODUCTION RELEASE

07/28/03 - Change BOM option for C51,C52,C77,C78,C91,C92,C111 to 8.2uF Panasonic AL cap only (p. 34)
08/05/03 - Change +3V/5V ITH compensation and No-Stuff Feed Forward Caps (P. 32)
Change CPU VCORE setting for both BEST and BETTER configurations (p. 33)
08/07/03 - Change CPU VCORE setting for both BEST and BETTER configurations again (p. 33)

8	7	6	5	4	3	2	1

D

C

B

A

*** Signal Cross-Reference for the entire design ***

[illegible]

8	7	6	5	4	3	2	1

```
PMU_EPM          29C4<> 29D2<
PMU_FROM_INT     14C2<> 29C4<>
PMU_I2C_CLK      29B4<> 29C2<
PMU_I2C_DATA     29B4<> 29C2<
PMU_INT_L        14B5<> 14B7< 29B6<>
PMU_INT_NMI      14B5<> 14B7< 29D4<>
PMU_KB_RESET_IN1  29A7<>
PMU_KB_RESET_IN2  29A7<>
PMU_KB_RESET_L   29A6> 29B7< 39C1>
PMU_LID_CLOSED_L  23B3< 23D6<> 29B2< 29C4<> 39D1>
PMU_NMI_BUTTON_L  29C2< 29C4<>
PMU_NMI_L        29C2< 29C4<>
PMU_NUMLOCK_LED_L  29C6<>
PMU_OOPS         29B2< 29B4<>
PMU_PME_L        14A5<> 17A8< 24D5<> 29B2< 29C4<>
                 39C3>
PMU_POWERUP_OK   29B4<> 29D2<
PMU_POWER_UP_L   28C8> 29C6<> 29D7< 32B8<
PMU_REQ_L        14B7< 14C2> 29C4<>
PMU_RESET_BUTTON_L  23A7> 29C4<> 29D2<
PMU_RESET_L      29B6<>
PMU_SLEEP_LED    23C7<> 23D6<> 39D1>
PMU_SLEEP_LED_L  23C8<> 29C4<>
PMU_SMB_CLK      29B4<> 29C2< 30A3<
PMU_SMB_DATA     29B4<> 29C2< 30A2<
PMU_TO_INT       14C2<> 29C4<>
POWER_UP         28D7<>
POWER_VALID      29B2< 29C4<>
PWR_BUTTON_L     23A7< 23B4<>
RAM_ADDR<0>      9B4< 11B3<> 11B6<>
RAM_ADDR<12..0>  35A5>
RAM_ADDR<1>      9B4< 11B5<> 11B8<>
RAM_ADDR<2>      9B4< 11B3<> 11B6<>
RAM_ADDR<3>      9B4< 11B5<> 11B8<>
RAM_ADDR<4>      9B4< 11B3<> 11B6<>
RAM_ADDR<5>      9B4< 11B5<> 11B8<>
RAM_ADDR<6>      9B4< 11B3<> 11B6<>
RAM_ADDR<7>      9B4< 11B5<> 11B8<>
RAM_ADDR<8>      9B4< 11B3<> 11B6<>
RAM_ADDR<9>      9A4< 11B5<> 11B8<>
RAM_ADDR<10>     9A4< 11B5<> 11B8<>
RAM_ADDR<11>     9A4< 11B3<> 11B6<>
RAM_ADDR<12>     9A4< 11B5<> 11B8<>
RAM_BA<0>        9A4< 11B5<> 11B8<>
RAM_BA<1..0>     35A5>
RAM_BA<1>        9A4< 11B3<> 11B6<>
RAM_CAS_L        9A4< 11B3<> 11B6<> 35A5>
RAM_CKE<0>       9A4< 9C4< 11C6<>
RAM_CKE<3..0>    35A5>
RAM_CKE<1>       9A4< 9C4< 11C8<>
RAM_CKE<2>       9A4< 9C4< 11C3<>
RAM_CKE<3>       9A4< 9C4< 11C5<>
RAM_CS_L<0>      9C4< 11B8<>
RAM_CS_L<3..0>   35A5>
RAM_CS_L<1>      9C4< 11B6<>
RAM_CS_L<2>      9C4< 11B5<>
RAM_CS_L<3>      9C4< 11B3<>
RAM_DATA_A<0>   10C8<> 11D8<>
RAM_DATA_A<7..0>  35D5>
RAM_DATA_A<1>   10C8<> 11D8<>
RAM_DATA_A<2>   10C8<> 11D8<>
RAM_DATA_A<3>   10B8<> 11D8<>
RAM_DATA_A<4>   10B8<> 11D6<>
RAM_DATA_A<5>   10B8<> 11D6<>
RAM_DATA_A<6>   10B8<> 11D6<>
RAM_DATA_A<7>   10B8<> 11D6<>
RAM_DATA_A<8>   10B8<> 11D8<>
RAM_DATA_A<15..8>  35C5>
RAM_DATA_A<9>   10C7<> 11D8<>
RAM_DATA_A<10>  10C7<> 11D8<>
RAM_DATA_A<11>  10C7<> 11D8<>
RAM_DATA_A<12>  10C7<> 11D6<>
RAM_DATA_A<13>  10C7<> 11D6<>
RAM_DATA_A<14>  10C7<> 11D6<>
RAM_DATA_A<15>  10C7<> 11D6<>
RAM_DATA_A<16>  10C6<> 11D8<>
RAM_DATA_A<23..16>  35C5>
RAM_DATA_A<17>  10C6<> 11C8<>
RAM_DATA_A<18>  10C6<> 11C8<>
RAM_DATA_A<19>  10B6<> 11C8<>
RAM_DATA_A<20>  10B6<> 11D6<>
RAM_DATA_A<21>  10B6<> 11C6<>
RAM_DATA_A<22>  10B6<> 11C6<>
RAM_DATA_A<23>  10B6<> 11C6<>
RAM_DATA_A<24>  10B6<> 11C8<>
RAM_DATA_A<31..24>  35C5>
RAM_DATA_A<25>  10C5<> 11C8<>
RAM_DATA_A<26>  10C5<> 11C8<>
RAM_DATA_A<27>  10C5<> 11C8<>
RAM_DATA_A<28>  10C5<> 11C6<>
RAM_DATA_A<29>  10C5<> 11C6<>
RAM_DATA_A<30>  10C5<> 11C6<>
RAM_DATA_A<31>  10C5<> 11C6<>
RAM_DATA_A<32>  10C4<> 11B8<>
RAM_DATA_A<39..32>  35B5>
RAM_DATA_A<33>  10C4<> 11B6<>
RAM_DATA_A<34>  10C4<> 11B6<>
RAM_DATA_A<35>  10C4<> 11B6<>
RAM_DATA_A<36>  10C4<> 11B3<>
RAM_DATA_A<37>  10C4<> 11B3<>
RAM_DATA_A<38>  10C4<> 11B3<>
RAM_DATA_A<39>  10C4<> 11B3<>
RAM_DATA_A<40>  10C4<> 11B5<>
RAM_DATA_A<47..40>  35B5>
RAM_DATA_A<41>  10C4<> 11B5<>
RAM_DATA_A<42>  10C4<> 11A5<>
RAM_DATA_A<43>  10C4<> 11A5<>
RAM_DATA_A<44>  10C4<> 11B3<>
RAM_DATA_A<45>  10C4<> 11B3<>
RAM_DATA_A<46>  10C4<> 11A3<>
RAM_DATA_A<47>  10C4<> 11A3<>
RAM_DATA_A<48>  10D2<> 11A5<>
RAM_DATA_A<55..48>  35B5>
RAM_DATA_A<49>  10C2<> 11A5<>
RAM_DATA_A<50>  10C2<> 11A5<>
RAM_DATA_A<51>  10C2<> 11A5<>
RAM_DATA_A<52>  10C2<> 11A3<>
RAM_DATA_A<53>  10C2<> 11A3<>
RAM_DATA_A<54>  10C2<> 11A3<>
RAM_DATA_A<55>  10C2<> 11A3<>
RAM_DATA_A<56>  10B2<> 11A5<>
RAM_DATA_A<63..56>  35A5>
RAM_DATA_A<57>  10D1<> 11A8<>
RAM_DATA_A<58>  10C1<> 11A8<>
RAM_DATA_A<59>  10C1<> 11A8<>
RAM_DATA_A<60>  10C1<> 11A6<>
RAM_DATA_A<61>  10C1<> 11A6<>
RAM_DATA_A<62>  10C1<> 11A6<>
RAM_DATA_A<63>  10C1<> 11A6<>
RAM_DATA_B<0>   10C8<> 11D5<>
RAM_DATA_B<7..0>  35D5>
RAM_DATA_B<1>   10C8<> 11D5<>
RAM_DATA_B<2>   10C8<> 11D5<>
RAM_DATA_B<3>   10C8<> 11D5<>
RAM_DATA_B<4>   10C8<> 11D3<>
RAM_DATA_B<5>   10C8<> 11D3<>
RAM_DATA_B<6>   10C8<> 11D3<>
RAM_DATA_B<7>   10C8<> 11D3<>
RAM_DATA_B<8>   10C8<> 11D5<>
RAM_DATA_B<15..8>  35C5>
RAM_DATA_B<9>   10C8<> 11D5<>
RAM_DATA_B<10>  10C8<> 11D5<>
RAM_DATA_B<11>  10C8<> 11D5<>
RAM_DATA_B<12>  10C8<> 11D3<>
RAM_DATA_B<13>  10C8<> 11D3<>
RAM_DATA_B<14>  10C8<> 11D3<>
RAM_DATA_B<15>  10C8<> 11D3<>
RAM_DATA_B<16>  10C6<> 11D5<>
RAM_DATA_B<23..16>  35C5>
RAM_DATA_B<17>  10C6<> 11C5<>
RAM_DATA_B<18>  10C6<> 11C5<>
RAM_DATA_B<19>  10C6<> 11C5<>
RAM_DATA_B<20>  10C6<> 11D3<>
RAM_DATA_B<21>  10C6<> 11C3<>
RAM_DATA_B<22>  10C6<> 11C3<>
RAM_DATA_B<23>  10C6<> 11C3<>
RAM_DATA_B<24>  10C6<> 11C5<>
RAM_DATA_B<25..24>  35C5>
RAM_DATA_B<25>  10C6<> 11C5<>
RAM_DATA_B<26>  10C6<> 11C5<> 35C5>
RAM_DATA_B<27>  10C6<> 11C5<>
RAM_DATA_B<31..27>  35C5>
RAM_DATA_B<28>  10C6<> 11C3<>
RAM_DATA_B<29>  10C6<> 11C3<>
RAM_DATA_B<30>  10C6<> 11C3<>
RAM_DATA_B<31>  10C6<> 11C3<>
RAM_DATA_B<32>  10D4<> 11B5<>
RAM_DATA_B<39..32>  35B5>
RAM_DATA_B<33>  10C4<> 11B5<>
RAM_DATA_B<34>  10C4<> 11B5<>
RAM_DATA_B<35>  10C4<> 11B5<>
RAM_DATA_B<36>  10C4<> 11B3<>
RAM_DATA_B<37>  10C4<> 11B3<>
RAM_DATA_B<38>  10C4<> 11B3<>
RAM_DATA_B<39>  10C4<> 11B3<>
RAM_DATA_B<40>  10C4<> 11B5<>
RAM_DATA_B<47..40>  35B5>
RAM_DATA_B<41>  10C4<> 11B5<>
RAM_DATA_B<42>  10C4<> 11A5<>
RAM_DATA_B<43>  10C4<> 11A5<>
RAM_DATA_B<44>  10C4<> 11B3<>
RAM_DATA_B<45>  10C4<> 11B3<>
RAM_DATA_B<46>  10C4<> 11A3<>
RAM_DATA_B<47>  10C4<> 11A3<>
RAM_DATA_B<48>  10D2<> 11A5<>
RAM_DATA_B<55..48>  35B5>
RAM_DATA_B<49>  10C2<> 11A5<>
RAM_DATA_B<50>  10C2<> 11A5<>
RAM_DATA_B<51>  10C2<> 11A5<>
RAM_DATA_B<52>  10C2<> 11A3<>
RAM_DATA_B<53>  10C2<> 11A3<>
RAM_DATA_B<54>  10C2<> 11A3<>
RAM_DATA_B<55>  10C2<> 11A3<>
RAM_DATA_B<56>  10C2<> 11A5<>
RAM_DATA_B<63..56>  35A5>
RAM_DATA_B<57>  10C2<> 11A5<>
RAM_DATA_B<58>  10C2<> 11A5<>
RAM_DATA_B<59>  10C2<> 11A5<>
RAM_DATA_B<60>  10C2<> 11A3<>
RAM_DATA_B<61>  10C2<> 11A3<>
RAM_DATA_B<62>  10C2<> 11A3<>
RAM_DATA_B<63>  10C2<> 11A3<>
RAM_DQM_A<0>    10B8<> 11D6<> 35D5>
RAM_DQM_A<1>    10C7<> 11D6<> 35C5>
RAM_DQM_A<2>    10B8<> 11C6<> 35C5>
RAM_DQM_A<3>    10C5<> 11C6<> 35C5>
RAM_DQM_A<4>    10B4<> 11B6<> 35B5>
RAM_DQM_A<5>    10C3<> 11B6<> 35B5>
RAM_DQM_A<6>    10B2<> 11A6<> 35B5>
RAM_DQM_A<7>    10C1<> 11A6<> 35A5>
RAM_DQM_B<0>    10C8<> 11D3<> 35D5>
RAM_DQM_B<1>    10C8<> 11D3<> 35C5>
RAM_DQM_B<2>    10C6<> 11C3<> 35C5>
RAM_DQM_B<3>    10C6<> 11C3<> 35C5>
RAM_DQM_B<4>    10C4<> 11B3<> 35B5>
RAM_DQM_B<5>    10C4<> 11B3<> 35B5>
RAM_DQM_B<6>    10C2<> 11A3<> 35B5>
RAM_DQM_B<7>    10C2<> 11A3<> 35A5>
RAM_DQS_A<0>    10B8<> 11D8<> 35D5>
RAM_DQS_A<1>    10C7<> 11D8<> 35C5>
RAM_DQS_A<2>    10B6<> 11C8<> 35C5>
RAM_DQS_A<3>    10C5<> 11C8<> 35C5>
RAM_DQS_A<4>    10B4<> 11B8<> 35B5>
RAM_DQS_A<5>    10C3<> 11B8<> 35B5>
RAM_DQS_A<6>    10B2<> 11A8<> 35B5>
RAM_DQS_A<7>    10C1<> 11A8<> 35A5>
RAM_DQS_B<0>    10C8<> 11D5<> 35D5>
RAM_DQS_B<1>    10C8<> 11D5<> 35C5>
RAM_DQS_B<2>    10C6<> 11C5<> 35C5>
RAM_DQS_B<3>    10C6<> 11C5<> 35C5>
RAM_DQS_B<4>    10C4<> 11B5<> 35B5>
RAM_DQS_B<5>    10C4<> 11B5<> 35B5>
RAM_DQS_B<6>    10C2<> 11A5<> 35B5>
RAM_DQS_B<7>    10C2<> 11A5<> 35A5>
RAM_RAS_L        9A4< 11B3<> 11B6<> 35A5>
RAM_WE_L         9A4< 11B5<> 11B8<> 35A5>
RESET_VREF       6C3<>
RF_DISABLE_L     24D6<> 39C3>
ROM_CS_L         9B3< 12A4< 24B6<> 39C3>
ROM_OE_L         9B3< 12A4< 24C5<> 39C3>
ROM_ONBOARD_CS_L  9B3< 24C6<> 39C3>
ROM_RW_L         9B3< 12A4< 24C6<> 39C3>
ROM_WP_L         9B3<
SI_A2            19C4<
SI_EXT_SWING_SET  19C2<>
SI_HPD           19C4<
SI_I2C_CLK       19D4< 20C5<>
SI_I2S_DATA      19C4< 20C5<>
SI_MSEN          19D2<>
SI_PD_L          19C4<
SI_RST_L         19C4<
SI_TMDS_CLKN     19C2<> 19C2< 36D1>
SI_TMDS_CLKP     19C2< 19C2<> 36D1>
SI_TMDS_CLK_STM  19D1<
SI_TMDS_D0_STM   19D1<
SI_TMDS_D1_STM   19D1<
SI_TMDS_D2_STM   19C1<
SI_TMDS_DN<0>    19C2<> 19C2< 36D1>
SI_TMDS_DN<1>    19B2< 19C2<> 36D1>
SI_TMDS_DN<2>    19B2< 19C2<> 36C1>
SI_TMDS_DP<0>    19C2<> 19C2< 36D1>
SI_TMDS_DP<1>    19B2< 19C2<> 36C1>
SI_TMDS_DP<2>    19B2< 19C2<> 36C1>
SI_VREF_IDCK_N   19C2< 19C4<
SLEEP            23D7<> 25D7<> 29B6<> 29D7< 32A4<
                 32A6< 32B3< 32B8<> 34B3< 34C2< 39C1>
SLEEP_LED        23C3<> 39C1>
SLEEP_LED_DGND   23C3<>
SLEEP_LED_I      23D3<
SLEEP_LED_L      23D4<
SLEEP_LED_SW_L   23D4<>
SLEEP_LED_UF     23D3<
SLEEP_LS5        32A4<> 32A8<
SLEEP_LS5_EN_L   32A5<>
SLEEP_L_LS5      18D5< 20A7<> 26A8<> 32A5<> 33C7<>
                 34C8<
SLEEP_L_LS5_EN_L  32A6<>
SLEEP_L_LS5_INV  34A3< 34C2< 34C8<>
SLEEP_L_LS5_NET  32B3<> 34C8<>
SLEEP_NET        32A3<>
SLEEP_NET_INV    32A3<>
SND_AMP_MUTE     25C7<> 25D6<> 39A6>
SND_AMP_MUTE_CTRL  25B5> 25D6<>
SND_AMP_MUTE_L   14B5<> 25D5<>
SND_HP_MUTE      25C5<>
SND_HP_MUTE_L    14C5<> 25C5<> 39A6>
SND_HP_MUTE_LO   25C6<> 25C7<>
SND_HP_SENSE_L   14B5<> 25C8<> 39A6>
SND_HW_RESET_L   14A7< 14B5<> 25D7<> 39A6>
SND_LIN_SENSE_L  14B5<> 25C8<> 39A6>
SOFT_PWR_ON_L    22D1<> 23A3< 29A8< 29C6<> 29D7<
                 33A4<> 39B3>
ST7_SLEEP_LED_H  23C5<> 23C6<> 23D6<> 39D1>
STOP_AGP_L       12D2< 12D4<>
SYSCLK_CPU       5C3< 8A6< 35D1>
SYSCLK_CPU_UF    8A5<> 35D1>
SYSCLK_DDRCLK_A0  9D4< 11D8<> 35D1>
SYSCLK_DDRCLK_A0_L  9D4< 11D8<> 35C1>
SYSCLK_DDRCLK_A0_L_UF  9B6<> 9D5< 35D1>
SYSCLK_DDRCLK_A0_UF  9B6<> 9D5< 35D1>
SYSCLK_DDRCLK_A1  9D4< 11A6<> 35C1>
SYSCLK_DDRCLK_A1_L  9D4< 11A6<> 35C1>
SYSCLK_DDRCLK_A1_L_UF  9B6<> 9D5< 35D1>
SYSCLK_DDRCLK_A1_UF  9B6<> 9D5< 35D1>
SYSCLK_DDRCLK_B0  9D4< 11D5<> 35C1>
SYSCLK_DDRCLK_B0_L  9C4< 11D5<> 35C1>
SYSCLK_DDRCLK_B0_L_UF  9B6<> 9C5< 35D1>
SYSCLK_DDRCLK_B0_UF  9B6<> 9D5< 35D1>
SYSCLK_DDRCLK_B1  9D4< 11A3<> 35C1>
SYSCLK_DDRCLK_B1_L  9D4< 11A3<> 35C1>
SYSCLK_DDRCLK_B1_L_UF  9B6<> 9D5< 35D1>
SYSCLK_DDRCLK_B1_UF  9B6<> 9D5< 35D1>
SYSCLK_LA_TP     8A5<>
SYSTEM_CLK_EN    14A5< 14B7< 29C4<>
THERM1_A_DM      25A7< 25AB< 37A2>
THERM1_A_DP      25A7< 25AB< 37A2>
THERM1_DM        25A5< 25A6< 25B5<> 25B6< 37A2>
THERM1_DP        25A5< 25A6< 25B5<> 25B6< 37A2>
THERM1_M_DM      25B7< 25B8< 37A2>
THERM1_M_DP      25B7< 25B8< 37A2>
THERM2_A_DM      25A7< 25AB< 37A2>
THERM2_A_DP      25A7< 25AB< 37A2>
THERM2_DM        25A5< 25A6< 25B5<> 25B6< 37A2>
THERM2_DP        25A5< 25A6< 25B5<> 25B6< 37A2>
THERM2_M_DM      25B7< 25B8< 37A2>
THERM2_M_DP      25B7< 25B8< 37A2>
THERM_INV        25B1<>
THERM_L_OC       25B1<> 29B4<>
TMDS_CLKN        19B1< 19C1< 19D1< 22C8<> 37C2>
TMDS_CLKP        19B1< 19C1< 19D2< 22C6<> 37C2>
TMDS_CONN_CLKN   22C7<> 22C7<> 36C1> 39C6>
TMDS_CONN_CLKP   22C7<> 22C7<> 36C1> 39C6>
TMDS_CONN_DN<0>  22D6<> 36C1>
TMDS_CONN_DN<1>  22D6<> 36B1>
TMDS_CONN_DN<2>  22D6<> 36B1>
TMDS_CONN_DP<0>  22D6<> 36C1>
TMDS_CONN_DP<1>  22D6<> 36B1>
TMDS_CONN_DP<2>  22D6<> 36B1>
TMDS_DN<0>       19B1< 19C1< 19D1< 22D7<> 37C2>
TMDS_DN<0..2>    39C6>
TMDS_DN<1>       19B1< 19B1< 19C1< 22D5<> 37B2>
TMDS_DN<2>       19A1< 19B1< 19C1< 22D5<> 37B2>
TMDS_DP<0>       19B1< 19C1< 19D2< 22D7<> 37B2>
TMDS_DP<0..2>    39C6>
TMDS_DP<1>       19B1< 19B1< 19C2< 22C5<> 37B2>
TMDS_DP<2>       19A1< 19B1< 19C2< 22D5<> 37B2>
TPAD_F_RXD       23B5<> 39B3>
TPAD_F_TXD       23B5<> 39B3>
TPAD_RXD         23A5< 29C2< 29C4<>
TPAD_TXD         23B5< 29B2< 29C4<>
TPS2211_SHTDWN_L  18C5<
TV_C             22A6<> 39A6>
TV_COMP          22A6<> 39A6>
TV_GND1          22B6<> 38B6> 39A6>
TV_GND2          22A6<> 38B6> 39A6>
TV_Y             22A6<> 39A6>
UIDE_ADDR<0>     13D7<> 24C4<
UIDE_ADDR<2..0>  37C5>
UIDE_ADDR<1>     13D7<> 24C4<
UIDE_ADDR<2>     13D7<> 24B4<
UIDE_CS0_L       13C7<> 24C4< 37C5>
UIDE_CS1_L       13C7<> 24B4< 37C5>
UIDE_DATA<0>     13D7<> 24D4<
UIDE_DATA<6..0>  37C5>
UIDE_DATA<1>     13D7<> 24D4<
UIDE_DATA<2>     13D7<> 24D4<
UIDE_DATA<3>     13D7<> 24D4<
UIDE_DATA<4>     13D7<> 24C4<
UIDE_DATA<5>     13D7<> 24C4<
UIDE_DATA<6>     13D7<> 24C4<
UIDE_DATA<7>     13D7<> 24C4< 37C5>
UIDE_DATA<8>     13D7<> 24C4<
UIDE_DATA<15..8>  37C5>
UIDE_DATA<9>     13D7<> 24C4<
UIDE_DATA<10>    13D7<> 24C4<
UIDE_DATA<11>    13D7<> 24D4<
UIDE_DATA<12>    13D7<> 24B4<
UIDE_DATA<13>    13D7<> 24B4<
UIDE_DATA<14>    13D7<> 24C4<
UIDE_DATA<15>    13D7<> 24B4<
UIDE_DIOR_L      13C7<> 24A4< 37C5>
UIDE_DIOW_L      13C7<> 24A4< 37C5>
UIDE_DMACK_L     13C7<> 24A4< 37C5>
UIDE_DMARQ       13C7<> 37C5>
UIDE_INTRQ       13C7< 37C5>
UIDE_IOCHRDY     13C7< 24A4< 37C5>
UIDE_REF         13C7<> 38C3>
UIDE_RST_L       13C7<> 24A4< 37C5>
USB_DAM          14B2<> 14D2<
USB_DAP          14B2<> 14D2<
USB_DBM          14B2<> 14D2<
USB_DBP          14B2<> 14D2<
USB_DCM          14B2<> 14D2<
USB_DCP          14B2<> 14D2<
USB_DDM          14B2<> 14D2<
USB_DDP          14B2<> 14C2<
USB_DEM          14B2<> 14C2< 37B2>
USB_DEP          14B2<> 14C2< 37B2>
USB_DFM          14B2< 14B2<> 37B2>
USB_DFP          14B2<> 14C2< 37B2>
USB_OC_AB_L      14B2< 14C7<
USB_OC_CD_L      14B2< 14C7<
USB_OC_EF_L      14B2< 14C7<
USB_PWREN_AB_L   14B2<> 14C7<
USB_PWREN_CD_L   14B2<> 14C7<
USB_PWREN_EF_L   14B2<> 14C7<
VCORE_AB_SEL     33A7<> 33C6<
VCORE_AB_SEL_INV  33A7<>
VCORE_AB_SEL_OPT  33A6<>
VCORE_BOOST      33C4<> 38C1>
VCORE_BST        33C5<> 38C1>
VCORE_CC         33B6<> 38C1>
VCORE_D0         33A3<>
VCORE_D1         33A3<>
VCORE_D2         33A3<>
VCORE_D3         33A3<>
VCORE_D4         33A3<>
VCORE_DH         33B5<> 38C1>
VCORE_DL         33B5<> 38C1>
VCORE_FAST<1>    33D4< 33D5<
VCORE_FAST<2>    33D4< 33D5<
VCORE_FAST<3>    33D4< 33D5<
VCORE_FAST<4>    33D4< 33D5<
VCORE_FB         33B5< 38B1> 39C6>
VCORE_GND        33B5<> 38B1>
VCORE_GNDA       33B6<> 38B1>
VCORE_GNDDIV     33A5< 33A5< 38B1>
VCORE_GNDDIV_TEST  33A4<>
VCORE_GNDSNS     33A1<> 33A5< 38B1>
VCORE_GNDSNS_TEST  33A4<>
VCORE_ILIM       33C6<> 38C1>
VCORE_LX         33B5<> 38C1>
VCORE_MUX_EN     33D5<>
VCORE_MUX_SEL    33D5<>
VCORE_OFFSET_DIV  33B6<>
VCORE_REF        33B6<> 38C1>
VCORE_SHDN_L     33C6<>
VCORE_SLOW<1>    33D6<
VCORE_SLOW<2>    33D6<
VCORE_SLOW<3>    33D6<
VCORE_SLOW<4>    33D6<
VCORE_SNS        33A1<> 38B1>
VCORE_TIME       33B4<> 38B1>
VCORE_TON        33B6< 38C1>
VCORE_VCC        33C6< 38C1>
VCORE_VGATE      14B5< 14B7< 33B4> 38B1>
VCORE_VID<0>     33B7<
VCORE_VID<1>     33B7< 33D3< 33D4>
VCORE_VID<2>     33B7< 33D3< 33D4>
VCORE_VID<3>     33B7< 33D3< 33D4>
VCORE_VID<4>     33B7< 33D3< 33D4>
VCORE_VSENSE     33C2<>
VGA_B            22C6<> 22C7< 39B6>
VGA_G            22C5<> 22C7< 39B6>
VGA_HSYNC        22C6<> 22D7< 39B6>
VGA_R            22B7< 22C5<> 39B6>
VGA_VSYNC        22C5<> 22D7< 39B6>
ZT10_SPN         4C2<>
ZT301_SPN        4C2<>
ZT302_SPN        4C2<>
ZV_LCDDATA20_PU  29C7<>
```


APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	4	

SCALE	SHT	OF
NONE	?x2	?

8 7 6 5 4 3 2 1

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*** Part Cross-Reference for the entire design ***

C1 CAP 5
C2 CAP 5
C3 CAP 33
C4 CAP 33
C5 CAP 33
C6 CAP 33
C7 CAP 32
C8 CAP 32
C9 CAP 5
C10 CAP 5
C11 CAP 30
C12 CAP 33
C13 CAP 33
C14 CAP 33
C15 CAP 33
C16 CAP 33
C17 CAP 5
C18 CAP 5
C19 CAP 22
C20 CAP 5
C21 CAP 33
C22 CAP 22
C23 CAP 30
C24 CAP 30
C25 CAP 5
C26 CAP 5
C27 CAP 5
C28 CAP 5
C29 CAP 5
C30 CAP 5
C31 CAP 5
C32 CAP 5
C33 CAP 5
C34 CAP 5
C35 CAP 30
C36 CAP 30
C37 CAP 18
C38 CAP 5
C39 CAP 5
C40 CAP 18
C41 CAP 30
C42 CAP 30
C43 CAP 30
C44 CAP 5
C45 CAP 5
C46 CAP 5
C47 CAP 5
C48 CAP 5
C49 CAP 5
C50 CAP 5
C51 CAP_P 33
C52 CAP_P 33
C53 CAP 5
C54 CAP 5
C55 CAP 5
C56 CAP 5
C57 CAP 33
C58 CAP 5
C59 CAP 5
C60 CAP 18
C61 CAP 5
C62 CAP 5
C63 CAP 33
C64 CAP 33
C65 CAP 33
C66 CAP 33
C67 CAP 30
C68 CAP 5
C69 CAP 5
C70 CAP 33
C71 CAP 30
C72 CAP 5
C73 CAP 5
C74 CAP 33
C75 CAP 5
C76 CAP 33
C77 CAP_P 33
C78 CAP_P 33
C79 CAP 33
C80 CAP 33
C81 CAP 5
C82 CAP 5
C83 CAP 33
C84 CAP 33
C85 CAP 5
C86 CAP 5
C87 CAP 5
C88 CAP 5
C89 CAP 5
C90 CAP 33
C91 CAP_P 33
C92 CAP_P 33
C93 CAP 33
C94 CAP 33
C95 CAP 30
C96 CAP 30
C97 CAP 30
C98 CAP 30
C99 CAP 30
C100 CAP 33
C101 CAP 33
C102 CAP 5
C103 CAP 5
C104 CAP 5
C105 CAP 33
C106 CAP 33
C107 CAP 5
C108 CAP 5
C109 CAP 5
C110 CAP 5
C111 CAP_P 33
C112 CAP 30
C113 CAP 30
C114 CAP 32
C115 CAP 30
C116 CAP 30
C117 CAP 30
C118 CAP 30
C119 CAP 31
C120 CAP 6
C121 CAP 31
C122 CAP 9
C123 CAP 32
C124 CAP 31
C125 CAP 9
C126 CAP 32
C127 CAP 11
C128 CAP 11
C129 CAP 34
C130 CAP 33
C131 CAP 31
C132 CAP 11
C133 CAP 34
C134 CAP 31
C135 CAP 31
C136 CAP 17
C137 CAP 31
C138 CAP 31
C139 CAP 16
C140 CAP 11
C141 CAP 16
C142 CAP 16
C143 CAP 32
C144 CAP 16
C145 CAP 16
C146 CAP 16
C147 CAP 16
C148 CAP 16
C149 CAP 16
C150 CAP 11
C151 CAP 14
C152 CAP 14
C153 CAP 31
C154 CAP 31
C155 CAP 16
C156 CAP 11
C157 CAP 11
C158 CAP 16
C159 CAP 16
C160 CAP 16
C161 CAP 16
C162 CAP 16
C163 CAP 16
C164 CAP 16
C165 CAP 16
C166 CAP 16
C167 CAP 16
C168 CAP 16
C169 CAP 11
C170 CAP 16
C171 CAP 16
C172 CAP 16
C173 CAP 17
C174 CAP 11
C175 CAP 16
C176 CAP 16
C177 CAP 16
C178 CAP 16
C179 CAP 16
C180 CAP 16
C181 CAP 16
C182 CAP 29
C183 CAP 16
C184 CAP 16
C185 CAP 16
C186 CAP 16
C187 CAP 8
C188 CAP 23
C189 CAP 16
C190 CAP 13
C191 CAP 16
C192 CAP 16
C193 CAP 34
C194 CAP 34
C195 CAP 34
C196 CAP 34
C197 CAP 17
C198 CAP 23
C199 CAP 23
C200 CAP 16
C201 CAP 16
C202 CAP 16
C203 CAP 16
C204 CAP 16
C205 CAP 16
C206 CAP 16
C207 CAP 16
C208 CAP 16
C209 CAP 34
C210 CAP 23
C211 CAP 11
C212 CAP 16
C213 CAP 16
C214 CAP 16
C215 CAP 16
C216 CAP 16
C217 CAP 16
C218 CAP 16
C219 CAP 16
C220 CAP 23
C221 CAP 16
C222 CAP 16
C223 CAP 16
C224 CAP 16
C225 CAP 16
C226 CAP 16
C227 CAP 16
C228 CAP 16
C229 CAP 16
C230 CAP 16
C231 CAP 16
C232 CAP 19
C233 CAP 23
C234 CAP 16
C235 CAP 14
C236 CAP 16
C237 CAP 16
C238 CAP 16
C239 CAP 16
C240 CAP 32
C241 CAP 16
C242 CAP 16
C243 CAP 16
C244 CAP 31
C245 CAP 16
C246 CAP 14
C247 CAP 16
C248 CAP 16
C249 CAP 9
C250 CAP 16
C251 CAP 16
C252 CAP 16
C253 CAP 16
C254 CAP 16
C255 CAP 29
C256 CAP 14
C257 CAP 16
C258 CAP 16
C259 CAP 16
C260 CAP 16
C261 CAP 16
C262 CAP 16
C263 CAP 16
C264 CAP 16
C265 CAP 16
C266 CAP 34
C267 CAP_P 34
C268 CAP 16
C269 CAP 16
C270 CAP 12
C271 CAP 16
C272 CAP 16
C273 CAP 16
C274 CAP 16
C275 CAP 16
C276 CAP 31
C277 CAP 29
C278 CAP 16
C279 CAP 16
C280 CAP 16
C281 CAP 16
C282 CAP 16
C283 CAP 16
C284 CAP 19
C285 CAP 16
C286 CAP 16
C287 CAP 16
C288 CAP 16
C289 CAP 16
C290 CAP 16
C291 CAP 12
C292 CAP 16
C293 CAP 16
C294 CAP 16
C295 CAP 16
C296 CAP 16
C297 CAP 16
C298 CAP 34
C299 CAP 16
C300 CAP 16
C301 CAP 16
C302 CAP 16
C303 CAP 16
C304 CAP 16
C305 CAP 16
C306 CAP 16
C307 CAP_P 34
C308 CAP 16
C309 CAP 16
C310 CAP 16
C311 CAP 12
C312 CAP 16
C313 CAP 16
C314 CAP 16
C315 CAP 16
C316 CAP 16
C317 CAP 16
C318 CAP 16
C319 CAP 16
C320 CAP 16
C321 CAP 16
C322 CAP 16
C323 CAP 16
C324 CAP 16
C325 CAP 16
C326 CAP 31
C327 CAP 16
C328 CAP 16
C329 CAP 16
C330 CAP 16
C331 CAP 16
C332 CAP 16
C333 CAP 16
C334 CAP 16
C335 CAP 16
C336 CAP 31
C337 CAP 14
C338 CAP 34
C339 CAP 29
C340 CAP 29
C341 CAP 16
C342 CAP 16
C343 CAP 16
C344 CAP 16
C345 CAP 16
C346 CAP 16
C347 CAP 16
C348 CAP 16
C349 CAP 16
C350 CAP 16
C351 CAP 16
C352 CAP 16
C353 CAP 32
C354 CAP 16
C355 CAP 34
C356 CAP 11
C357 CAP 16
C358 CAP 16
C359 CAP 16
C360 CAP 16
C361 CAP 16
C362 CAP 12
C363 CAP 16
C364 CAP 16
C365 CAP 16
C366 CAP 16
C367 CAP 16
C368 CAP 16
C369 CAP 16
C370 CAP 29
C371 CAP 16
C372 CAP 12
C373 CAP 16
C374 CAP 16
C375 CAP 16
C376 CAP 16
C377 CAP 16
C378 CAP 16
C379 CAP 16
C380 CAP 16
C381 CAP 16
C382 CAP 16
C383 CAP 11
C384 CAP 19
C385 CAP 16
C386 CAP 14
C387 CAP 14
C388 CAP 14
C389 CAP 14
C390 CAP 19
C391 CAP 11
C392 CAP 14
C393 CAP_P 34
C394 CAP 14
C395 CAP 16
C396 CAP_P 34
C397 CAP 11
C398 CAP 32
C399 CAP 14
C400 CAP 14
C401 CAP 19
C402 CAP 14
C403 CAP 11
C404 CAP 11
C405 CAP_P 34
C406 CAP 29
C407 CAP 20
C408 CAP 19
C409 CAP 19
C410 CAP 32
C411 CAP 20
C412 CAP 19
C413 CAP 21
C414 CAP 21
C415 CAP 32
C416 CAP 32
C417 CAP 21
C418 CAP 21
C419 CAP 21
C420 CAP 21
C421 CAP 21
C422 CAP 21
C423 CAP 21
C424 CAP 21
C425 CAP 21
C426 CAP 21
C427 CAP 21
C428 CAP 32
C429 CAP 32
C430 CAP 21
C431 CAP 20
C432 CAP 32
C433 CAP 32
C434 CAP 20
C435 CAP 20
C436 CAP 21
C437 CAP 21
C438 CAP 21
C439 CAP 21
C440 CAP 20
C441 CAP 20
C442 CAP 19
C443 CAP 20
C444 CAP 21
C445 CAP 20
C446 CAP 20
C447 CAP 21
C448 CAP 20
C449 CAP 20
C450 CAP 21
C451 CAP 20
C452 CAP 20
C453 CAP 21
C454 CAP 21
C455 CAP 20
C456 CAP 21
C457 CAP 19
C458 CAP 19
C459 CAP 21
C460 CAP 21
C461 CAP 21
C462 CAP 21
C463 CAP 21
C464 CAP 21
C465 CAP 20
C466 CAP 20
C467 CAP 29
C468 CAP 21
C469 CAP 20
C470 CAP 21
C471 CAP 21
C472 CAP 21
C473 CAP 21
C474 CAP 22
C475 CAP 21
C476 CAP 19
C477 CAP 20
C478 CAP 21
C479 CAP 20
C480 CAP 20
C481 CAP 20
C482 CAP 20
C483 CAP 21
C484 CAP 21
C485 CAP 20
C486 CAP 20
C487 CAP 20
C488 CAP 21
C489 CAP 21
C490 CAP 19
C491 CAP 21
C492 CAP 21
C493 CAP 21
C494 CAP 20
C495 CAP 20
C496 CAP 21
C497 CAP 20
C498 CAP 20
C499 CAP 21
C500 CAP 21
C501 CAP 21
C503 CAP 22
C504 CAP 21
C505 CAP 20
C506 CAP 21
C507 CAP 20
C508 CAP 19
C509 CAP 20
C510 CAP 20
C511 CAP 21
C512 CAP 20
C513 CAP 20
C514 CAP 21
C515 CAP 20
C516 CAP 19
C517 CAP 21
C518 CAP 21
C519 CAP 21
C520 CAP 21
C521 CAP 21
C522 CAP 20
C523 CAP 21
C524 CAP 20
C525 CAP 20
C526 CAP 20
C527 CAP 21
C528 CAP 20
C529 CAP 20
C530 CAP 19
C531 CAP 20
C532 CAP 20
C533 CAP 20
C534 CAP 21
C535 CAP 21
C536 CAP 20
C537 CAP 21
C538 CAP 21
C539 CAP 21
C540 CAP 21
C541 CAP 21
C542 CAP 21
C543 CAP 21
C544 CAP 21
C545 CAP 21
C546 CAP 21
C547 CAP 21
C548 CAP 22
C549 CAP 22
C550 CAP 21
C551 CAP 21
C552 CAP 21
C553 CAP 21
C554 CAP 32
C555 CAP 32
C556 CAP 32
C557 CAP 32
C558 CAP 32
C559 CAP 32
C560 CAP 32
C561 CAP 32
C562 CAP 32
C563 CAP 32
C564 CAP 32
C565 CAP 32
C566 CAP 32
C567 CAP 32
C568 CAP 32
C569 CAP 32
C570 CAP 32
C571 CAP 32
C572 CAP 32
C573 CAP 32
C574 CAP 32
C575 CAP 32
C576 CAP 32
C577 CAP 32
C578 CAP 32
C579 CAP 32
C580 CAP 32
C581 CAP 32
C582 CAP 32
C583 CAP 27
C584 CAP 27
C585 CAP 27
C586 CAP 27
C587 CAP 27
C588 CAP 27
C589 CAP 27
C590 CAP 27
C591 CAP 27
C592 CAP 26
C593 CAP 27
C594 CAP 26
C595 CAP 26
C596 CAP 27
C597 CAP 26
C598 CAP 26
C599 CAP 26
C600 CAP 26
C601 CAP 26
C602 CAP 26
C603 CAP 26
C604 CAP 26
C605 CAP 27
C606 CAP 27
C607 CAP 27
C608 CAP 26
C609 CAP 27
C610 CAP 27
C611 CAP 26
C612 CAP 26
C613 CAP 26
C614 CAP 26
C615 CAP 26
C616 CAP 26
C617 CAP 26
C618 CAP 26
C619 CAP 26
C620 CAP 27
C621 CAP 27
C622 CAP 26
C623 CAP 26
C624 CAP 26
C625 CAP 27
C627 CAP 32
C628 CAP 32
C629 CAP 32
C630 CAP 28
C631 CAP 22
C632 CAP 22
C633 CAP 28
C634 CAP 22
C635 CAP 22
C636 CAP 28
C637 CAP 28
C638 CAP 28
C639 CAP 28
C640 CAP 28
C641 CAP 22
C642 CAP 22
C644 CAP 28
C645 CAP 26
C646 CAP 26
C647 CAP 26
C648 CAP 26
C649 CAP 28
C650 CAP 28
C651 CAP 28
C652 CAP 28
C653 CAP 22
C654 CAP 22
C655 CAP 22
C656 CAP 22
C657 CAP 22
C658 CAP 22
C659 CAP 22
C660 CAP 22
C661 CAP 22
C662 CAP 28
C663 CAP 22
C664 CAP 22
C665 CAP 27
C666 CAP 28
C667 CAP 22
C668 CAP 22
C669 CAP 25
C670 CAP_P 27
C671 CAP 27
C672 CAP 27
C673 CAP 27
C674 CAP 26
C675 CAP 26
C676 CAP 27
C677 CAP 27
C678 CAP 27
C679 CAP 27
C680 CAP 26
C681 CAP 27
C682 CAP 27
C683 CAP 27
C684 CAP 27
C685 CAP_P 32
C686 CAP 32
C687 CAP 32
C688 CAP 32
C689 CAP 25
C690 CAP 34
C691 CAP 34
C692 CAP 25
C693 CAP 34
C694 CAP 32
C695 CAP 34
C696 CAP 25
C697 CAP 34
C698 CAP 25
C699 CAP 32
C700 CAP 32
C701 CAP 22
C702 CAP 22
C703 CAP_P 32
C704 CAP 20
C705 CAP_P 20
C706 CAP 20
C707 CAP_P 20
C708 CAP 20
C709 CAP_P 32
C710 CAP_P 32
C711 CAP_P 20
C712 CAP 20
C713 CAP_P 32
C714 CAP 34
C715 CAP 34
C716 CAP 34
C717 CAP 34
C718 CAP 34
C719 CAP 34
C720 CAP 34
C721 CAP 14
C722 CAP 34
C723 CAP 14
C724 CAP 29
C725 CAP 34
C726 CAP 10
C727 CAP 10
C728 CAP 29
C729 CAP 29
C730 CAP 10
C731 CAP 29
C732 CAP 10
C733 CAP 10
C734 CAP 10
C735 CAP 16
C736 CAP 16
C737 CAP 31
C738 CAP 34
C739 CAP 16
C740 CAP 31
C741 CAP 10
C742 CAP 10
C743 CAP 17
C744 CAP 17
C745 CAP 10
C746 CAP 17
C747 CAP 17
C748 CAP 17
C749 CAP 17
C750 CAP 27
C751 CAP 17
C752 CAP 17
C753 CAP 31
C754 CAP 31
C755 CAP 31
C756 CAP 17
C757 CAP 10
C758 CAP 10
C759 CAP 17
C760 CAP 17
C761 CAP 17
C762 CAP 6
C763 CAP 25
C764 CAP 10
C765 CAP 17
C766 CAP 23
C767 CAP 31
C768 CAP 17
C769 CAP 17
C770 CAP 16
C771 CAP 31
C772 CAP 31
C773 CAP 9
C774 CAP_P 33
C775 CAP 18
C776 CAP 18
C777 CAP 30
C778 CAP 18
C779 CAP_P 30
C780 CAP 30
C781 CAP_P 33
C782 CAP 18
C783 CAP 18
C784 CAP 18
C785 CAP 30
C786 CAP 18
C787 CAP 18
C788 CAP_P 33
C789 CAP 18
C790 CAP 30
C791 CAP 18
C792 CAP 30
C793 CAP_P 33
C794 CAP 30
C795 CAP 30
C796 CAP 18
C797 CAP_P 33
C798 CAP 30
C799 CAP 30
C800 CAP 18
C801 CAP 30
C802 CAP_P 33
C803 CAP 30
C804 CAP_P 31
C805 CAP 24
C806 CAP_P 31
C807 CAP 30
C808 CAP 24
C809 CAP 30
C810 CAP 5
C811 CAP 5
C812 CAP 22
C813 CAP 22
C814 CAP 25
C815 CAP 22
C816 CAP 22
C817 CAP 25
C818 CAP 25
C819 CAP 22
C826 CAP 30
C828 CAP 25
C829 CAP 25
C830 CAP 21
C831 CAP 21
C832 CAP 21
C833 CAP 21
C834 CAP 21
C835 CAP 21
C838 CAP 20
C839 CAP 32
C840 CAP 32
C841 CAP 33
C842 CAP 33
C843 CAP 34
C844 CAP 34
C845 CAP 34
C846 CAP 20
C847 CAP 13
C848 CAP_P 25
C849 CAP 25
C850 CAP 25
C851 CAP 26
C852 CAP 26
C853 CAP 30
C854 CAP 19
C855 CAP 19
C856 CAP 19
C857 CAP 19
C858 CAP 19
C859 CAP 19
C860 CAP 19
C861 CAP 19
C862 CAP 19
C863 CAP 19
C864 CAP 19
C865 CAP 19
C866 CAP 19
C867 CAP 19
C868 CAP 25
C869 CAP 25
C871 CAP 19
C872 CAP 19
C873 CAP 19
C874 CAP 19
C875 CAP 19
C876 CAP 19
C877 CAP 19
C878 CAP 19
C879 CAP 19
C880 CAP 21
C881 CAP 21
D1 DIODE_SCHOT 31
D2 DIODE_SCHOT 31
D3 DIODE 31
D4 DIODE 30
D5 DIODE_SCHOT 33
D6 DIODE 30
D7 DIODE_SCHOT 31
D8 DIODE 31
D9 ZENER_MMBZ15VDLT1 23
D10 DIODE_SCHOT 31
D11 DIODE_SCHOT 31
D12 DIODE 20
D13 DIODE_SCHOT 32
D14 DIODE_SCHOT 32
D15 DIODE 26
D16 DIODE_SCHOT 27
D18 DIODE_DUAL_6P 28
D19 DIODE_SCHOT 22
D20 DIODE_DUAL_6P 28
D21 ZENER 28
D22 DIODE_DUAL_6P 28
D23 DIODE_DUAL_6P 28
D24 DIODE_SCHOT 28
D25 DIODE_SCHOT_3P2 27
D26 DIODE_SCHOT 32
D27 DIODE 32
D28 DIODE_SCHOT 32
D29 DIODE_SCHOT 20
D30 DIODE_SCHOT 34
D31 DIODE_SCHOT 34
D32 DIODE_SCHOT 31
D33 DIODE 33
D36 DIODE_SCHOT 30
DP1 DPAK3P 30
DP2 DPAK3P 33
DP3 DPAK3P 34
DP4 DPAK3P 34
DP5 DPAK3P 20
DP6 DPAK3P 28
DP7 DPAK3P 20
F1 FUSE 28
F2 FUSE 22
F3 FUSE 28
F4 FUSE 30
F5 FUSE 30
G1 OSC 19
G2 OSC 27
J1 CON_M4RT_S2MT_SM 25
J2 CON_4RT_WRIB 23
J3 CON_M40ST_D4MT_SM 25
J4 CON_4RT_WRIB 22
J5 CON_M06ST_D4MT_SM 18
J6 CON_F80ST_D4MT_SM 24
J7 CON_12 33
J8 CON_2RTSM_12S 23
J9 CON_F1ST_S2MT_SM 14
J10 CON_10STSM_S08T 23
J11 CON_F30RT_S2MT_SM1 23
J12 CON_M50SM_5MM 24
J13 CON_M50SM_5MM 24
J14 CON_F30RT_S2MT_SM 22
J15 CON_M16ST_D_SMA 25
J16 CON_3RTSM_12S 31
J17 CON_M16ST_D_SMA 25
J18 CON_M4RT_S2MT_SM 25
J19 CON_F20ST_D_SM 23
J20 CON_F9RT_1394B_S6MT_SMA 28
J21 CON_F5RT_MINIDIN_TH 22
J22 CON_F30RT_T6MT_TH1 22
J23 CON_R14S_10RT_S4MT_TH1 26
J24 CON_F6RT_S4MT_TH1 28
J25 CON_F400RT_DDRDIMM_SM3 11
J26 CON_M8RT_S_SM 30
J27 CON_M4RT_S_SM 30
J28 CON_10STSM_S08T 25
L1 IND 22
L2 IND 30
L3 IND 30
L4 IND 30
L5 IND 30
L6 IND 30
L7 IND 17
L8 IND 23
L9 IND 23
L10 IND 23
L11 IND 23
L12 IND 23
L13 IND 14
L14 IND 14
L15 IND 14
L16 IND 19
L17 IND 20
L18 IND 21
L19 IND 21
L20 IND 21
L21 IND 21
L22 IND 19
L23 IND 21
L24 IND 33
L25 IND 21
L26 IND 21
L27 IND 22
L28 IND 21
L29 IND 21
L30 IND 21
L31 IND 21
L32 IND 21
L33 IND 21
L34 IND 27
L35 IND 26
L36 IND 22
L37 FILTER_4P 22
L38 IND 22
L39 IND 28
L40 IND 22
L41 IND 22
L42 IND 22
L43 IND 22
L44 IND 22
L45 FILTER_4P 22
L46 FILTER_4P 22
L47 FILTER_4P 22
L48 FILTER_4P 28
L49 IND 22
L50 IND 22
L51 IND 28
L52 FILTER_4P 28
L53 IND 22
L54 IND 22
L55 IND 22
L56 IND 22
L57 IND 22
L58 IND 28
L59 IND 27
L60 IND 26
L61 IND 32
L62 IND 32
L63 IND 34
L64 IND_3P 20
L65 IND 34
L66 IND 19
L67 IND 34
L68 IND 23
L69 IND_3P 31
L70 IND 30
L71 IND_3P 33
L72 IND 22
L73 IND 22
L74 IND 22
L75 IND 21
L76 FILTER_4P 28
L77 FILTER_4P 28
L78 IND 19
L79 IND 19
L80 IND 19
L81 IND 21
Q1 TRA_2N7002DW 30
Q2 TRA_2N7002DW 30
Q3 TRA_2N7002DW 7
Q4 TRA_2N7002DW 30
Q5 TRA_2N3904 33
Q6 TRA_SI4435DY 30
Q7 TRA_SUD45P03 30
Q8 TRA_2N3904 33
Q9 TRA_2N7002DW 30
Q10 TRA_2N7002 34
Q11 TRA_2N7002DW 34
Q12 TRA_2N3904 7
Q13 TRA_2N7002 7
Q14 TRA_2N7002DW 7
Q15 TRA_FDG6324L 31
Q16 TRA_IRF7811W 31
Q17 TRA_IRF7805 31
Q18 TRA_2N7002DW 23
Q19 TRA_2N3906 23
Q20 TRA_2N7002DW 32
Q21 TRA_SI3443DV 32
Q22 TRA_2N3906 23
Q23 TRA_SI3446DV 20
Q24 TRA_2N7002DW 32
Q25 TRA_2N7002DW 20
Q26 TRA_SI3443DV 32
Q27 TRA_SI3443DV 32
Q28 TRA_2N7002 22
Q29 TRA_SI3443DV 22
Q30 TRA_2N7002 29
Q31 TRA_2N7002 34
Q32 TRA_2N7002DW 26
Q33 TRA_2N7002DW 28
Q34 TRA_NDS9407 28
Q35 TRA_DUAL_MMDT3904 22
Q38 TRA_TPS610 22
Q39 TRA_2N7002DW 22
Q40 TRA_2N7002DW 22
Q41 TRA_SI4888DY 32
Q42 TRA_SI4888DY 32
Q43 TRA_2N7002 32
Q44 TRA_2N7002DW 32
Q45 TRA_SI4888DY 32
Q46 TRA_2N3904 25
Q47 TRA_SI4888DY 32
Q48 TRA_SI7860DP 20
Q49 TRA_IRF7832 20
Q50 TRA_2N7002DW 32
Q51 TRA_2N3904 20
Q52 TRA_2N3904 20
Q53 TRA_SI3446DV 34
Q54 TRA_IRF7811W 34
Q55 TRA_IRF7805 34
Q56 TRA_IRF7805 34
Q57 TRA_IRF7811W 34
Q58 TRA_2N3906 23
Q59 TRA_2N3904 25
Q60 TRA_IRF7832 33
Q61 TRA_2N3904 25
Q62 TRA_SI7860DP 33
Q63 TRA_IRF7832 33
Q64 TRA_IRF7811W 30
Q65 TRA_SI7860DP 33
Q66 TRA_IRF7832 33
Q67 TRA_2N3904 25
Q68 TRA_SI4435DY 30
Q69 TRA_SI4435DY 30
Q70 TRA_IRF7805 30
Q71 TRA_2N7002DW 30
Q72 TRA_2N7002DW 30
Q74 TRA_2N7002DW 30
Q76 TRA_FDG6324L 22
Q77 TRA_2N7002DW 25
Q78 TRA_2N7002DW 25
Q79 TRA_2N7002DW 25
Q82 TRA_2N7002DW 33
Q83 TRA_2N7002DW 21
R2 RES 5
R3 RES 5
R4 RES 5
R5 RES 7
R6 RES 5
R7 RES 5
R8 RES 5
R9 RES 5
R10 RES 5
R11 RES 5
R12 RES 7
R13 RES 5
R14 RES 7
R15 RES 30
R16 RES 30
R17 RES 7
R18 RES 7
R19 RES 5
R20 RES 5
R21 RES 30
R22 RES 30
R23 RES 7
R24 RES 5
R25 RES 5
R26 RES 5
R27 RES 5
R28 RES 5
R29 RES 30
R30 RES 30
R31 RES 7
R32 RES 5
R33 RES 5
R34 RES 5
R35 RES 7
R36 RES 5
R37 RES 5
R38 RES 5
R39 RES 31
R40 RES 30
R41 RES 30
R42 RES 30
R43 RES 7
R44 RES 7
R45 RES 5
R46 RES 5
R47 RES 30
R48 RES 7
R49 RES 30
R50 RES 7
R51 RES 30
R52 RES 30
R53 RES 30
R54 RES 30
R55 RES 30
R56 RES 30
R57 RES 30
R58 RES 30
R59 RES 30
R60 RES 7
R61 RES 30
R62 RES 30
R63 RES 7
R64 RES 7
R65 RES 33
R66 RES 33
R67 RES 33
R68 RES 7
R69 RES 33
R70 RES 7
R71 RES 33
R72 RES 33
R73 RES 30
R74 RES 30
R75 RES 30
R76 RES 7
R77 RES 30
R78 RES 7
R79 RES 7
R80 RES 33
R81 RES 33
R82 RES 30
R83 RES 30
R84 RES 7
R85 RES 33
R86 RES 33
R87 RES 30
R88 RES 7
R89 RES 5
R90 RES 33
R91 RES 33
R92 RES 7
R93 RES 33
R94 RES 30
R95 RES 33
R96 RES 30
R97 RES 33
R98 RES 33
R99 RES 33
R100 RES 6
R101 RES 33
R102 RES 30
R103 RES 6
R104 RES 6
R105 RES 6
R106 RES 33
R107 RES 31
R108 RES 31
R109 RES 33
R110 RES 7
R111 RES 33
R112 RES 9
R113 RES 14
R114 RES 34
R115 RES 34
R116 RES 34
R117 RES 34
R118 RES 31
R119 RES 30
R120 RES 31
R121 RES 33
R122 RES 31
R123 RES 33
R124 RES 17
R125 RES 33
R126 RES 33
R127 RES 31
R128 RES 8
R129 RES 33
R130 RES 33
R131 RES 7
R132 RES 7
R133 RES 7
R134 RES 14
R135 RES 33
R136 RES 8
R137 RES 33
R138 RES 23
R139 RES 33
R140 RES 8
R141 RES 8
R142 RES 14
R143 RES 14
R144 RES 14
R145 RES 13
R146 RES 8
R147 RES 8
R148 RES 14
R149 RES 13
R150 RES 8
R151 RES 8
R152 RES 8
R153 RES 14
R154 RES 23
R155 RES 8
R156 RES 14
R157 RES 14
R158 RES 14
R159 RES 8
R160 RES 13
R161 RES 8
R162 RES 9
R163 RES 23
R164 RES 14
R165 RES 14
R166 RES 14
R167 RES 12
R168 RES 8
R169 RES 8
R170 RES 34
R171 RES 34
R172 RES 17
R173 RES 23
R174 RES 14
R175 RES 14
R176 RES 9
R177 RES 34
R178 RES 14
R179 RES 14
R180 RES 14
R181 RES 14
R182 RES 14
R183 RES 14
R184 RES 34
R185 RES 23
R186 RES 13
R187 RES 14
R188 RES 14
R189 RES 14
R190 RES 23
R191 RES 14
R192 RES 14
R193 RES 14
R195 RES 13
R196 RES 24
R197 RES 12
R198 RES 23
R199 RES 24
R200 RES 24
R201 RES 14
R202 RES 9
R203 RES 24
R204 RES 24
R205 RES 13
R206 RES 14
R207 RES 13
R208 RES 9
R209 RES 9
R210 RES 34
R211 RES 34
R212 RES 34
R213 RES 24
R214 RES 24
R215 RES 24
R216 RES 24
R217 RES 24
R218 RES 14
R219 RES 12
R220 RES 34
R221 RES 34
R222 RES 34
R223 RES 23
R224 RES 13
R225 RES 12
R226 RES 34
R227 RES 34
R228 RES 23
R229 RES 24
R230 RES 12
R231 RES 31
R232 RES 13
R233 RES 31
R234 RES 24
R235 RES 12
R236 RES 24
R238 RES 24
R239 RES 12
R240 RES 14
R241 RES 14
R242 RES 24
R243 RES 14
R244 RES 12
R245 RES 12
R246 RES 12
R247 RES 9
R248 RES 29
R249 RES 29
R250 RES 14
R251 RES 24
R252 RES 12
R253 RES 12
R254 RES 12
R255 RES 12
R256 RES 12
R257 RES 9
R258 RES 14
R259 RES 13
R260 RES 9
R261 RES 29
R262 RES 24
R263 RES 13
R264 RES 12
R265 RES 9
R266 RES 24
R267 RES 29
R268 RES 24
R269 RES 13
R270 RES 13
R272 RES 12
R273 RES 12
R274 RES 15
R275 RES 21
R276 RES 15
R277 RES 12
R278 RES 12
R279 RES 14
R280 RES 14
R281 RES 5
R282 RES 12
R283 RES 5
R284 RES 14
R285 RES 19
R286 RES 14
R287 RES 14
R288 RES 14
R289 RES 19
R290 RES 19
R291 RES 32
R292 RES 14
R293 RES 14
R294 RES 32
R295 RES 14
R296 RES 14
R297 RES 19
R298 RES 19
R299 RES 11
R300 RES 23
R301 RES 32
R303 RES 11
R304 RES 19
R305 RES 19
R306 RES 32
R307 RES 32
R308 RES 12
R309 RES 19
R310 RES 32
R311 RES 32
R312 RES 21
R313 RES 19
R314 RES 12
R315 RES 19
R316 RES 12
R317 RES 12
R318 RES 12
R319 RES 21
R320 RES 19
R321 RES 32
R322 RES 32
R323 RES 19
R324 RES 19
R325 RES 19
R326 RES 20
R327 RES 20
R328 RES 20
R329 RES 20
R330 RES 20
R331 RES 20
R332 RES 20
R333 RES 20
R334 RES 12
R335 RES 19
R336 RES 19
R337 RES 19
R338 RES 19
R339 RES 20
R340 RES 20
R341 RES 20
R342 RES 20
R343 RES 20
R344 RES 20
R345 RES 29
R346 RES 20
R347 RES 22
R348 RES 29
R349 RES 29
R350 RES 20
R351 RES 20
R352 RES 20
R353 RES 20
R354 RES 22
R355 RES 20
R356 RES 20
R357 RES 20
R358 RES 20
R359 RES 20
R360 RES 20
R361 RES 20
R362 RES 20
R363 RES 21
R364 RES 29
R365 RES 19
R366 RES 20
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R392 RES 20
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R394 RES 20
R395 RES 20
R396 RES 20
R397 RES 19
R398 RES 34
R399 RES 32
R400 RES 32
R401 RES 32
R402 RES 32
R403 RES 32
R404 RES 32
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R409 RES 32
R410 RES 32
R411 RES 32
R412 RES 27
R413 RES 27
R414 RES 27
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R418	RES	27
R419	RES	27
R420	RES	27
R421	RES	26
R422	RES	26
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R424	RES	26
R425	RES	26
R426	RES	27
R427	RES	26
R428	RES	26
R429	RES	26
R430	RES	26
R431	RES	26
R432	RES	26
R433	RES	26
R434	RES	26
R435	RES	26
R436	RES	26
R437	RES	26
R438	RES	26
R439	RES	26
R440	RES	26
R441	RES	26
R442	RES	26
R443	RES	27
R444	RES	27
R445	RES	26
R446	RES	28
R447	RES	28
R448	RES	28
R451	RES	28
R454	RES	25
R456	RES	22
R458	RES	22
R459	RES	22
R460	RES	22
R461	RES	28
R462	RES	22
R463	RES	22
R464	RES	22
R465	RES	28
R466	RES	28
R469	RES	22
R470	RES	22
R471	RES	28
R472	RES	22
R473	RES	22
R474	RES	22
R475	RES	22
R476	RES	22
R477	RES	22
R478	RES	22
R479	RES	22
R480	RES	22
R481	RES	22
R482	RES	22
R483	RES	22
R484	RES	22
R485	RES	22
R486	RES	27
R487	RES	27
R488	RES	27
R489	RES	27
R490	RES	27
R491	RES	27
R492	RES	27
R493	RES	27
R494	RES	27
R495	RES	27
R496	RES	27
R497	RES	27
R498	RES	27
R499	RES	27
R500	RES	27
R501	RES	27
R502	RES	27
R503	RES	26
R504	RES	26
R505	RES	27
R506	RES	26
R507	RES	26
R508	RES	27
R509	RES	27
R510	RES	27
R511	RES	27
R512	RES	27
R513	RES	26
R514	RES	27
R515	RES	27
R516	RES	27
R517	RES	27
R518	RES	27
R519	RES	27
R520	RES	27
R521	RES	32
R522	RES	32
R523	RES	32
R524	RES	32
R525	RES	34
R526	RES	34
R527	RES	34
R528	RES	34
R529	RES	34
R530	RES	25
R531	RES	34
R532	RES	34
R533	RES	32
R534	RES	32
R535	RES	34
R536	RES	34
R537	RES	32
R538	RES	32
R539	RES	32
R540	RES	24
R541	RES	24
R542	RES	24
R543	RES	22
R544	RES	22
R545	RES	24
R546	RES	24
R547	RES	25
R548	RES	32
R549	RES	20
R550	RES	32
R551	RES	32
R552	RES	12
R553	RES	12
R554	RES	34
R555	RES	20
R556	RES	20
R557	RES	34
R558	RES	20
R559	RES	20
R560	RES	29
R561	RES	29
R562	RES	29
R563	RES	29
R564	RES	29
R565	RES	14
R566	RES	34
R567	RES	14
R568	RES	14
R569	RES	23
R570	RES	24
R571	RES	34
R572	RES	32
R573	RES	24
R574	RES	14
R575	RES	29
R576	RES	29
R577	RES	23
R578	RES	24
R579	RES	24
R580	RES	29
R581	RES	29
R582	RES	29
R583	RES	29
R584	RES	29
R585	RES	29
R586	RES	29
R587	RES	29
R588	RES	29
R589	RES	29
R590	RES	29
R591	RES	29
R592	RES	29
R593	RES	29

R594	RES	29
R595	RES	29
R596	RES	29
R597	RES	29
R598	RES	29
R599	RES	29
R600	RES	29
R602	RES	29
R603	RES	23
R604	RES	31
R605	RES	31
R606	RES	17
R607	RES	17
R608	RES	17
R609	RES	17
R610	RES	17
R611	RES	23
R612	RES	17
R613	RES	17
R614	RES	17
R615	RES	17
R616	RES	23
R617	RES	17
R618	RES	8
R619	RES	8
R620	RES	8
R621	RES	8
R622	RES	8
R623	RES	8
R624	RES	8
R625	RES	8
R626	RES	8
R627	RES	8
R628	RES	8
R629	RES	8
R631	RES	33
R632	RES	17
R633	RES	25
R634	RES	33
R635	RES	33
R636	RES	17
R637	RES	6
R638	RES	8
R639	RES	8
R640	RES	8
R641	RES	8
R642	RES	8
R643	RES	8
R644	RES	8
R645	RES	8
R646	RES	8
R647	RES	33
R648	RES	8
R649	RES	8
R650	RES	8
R651	RES	8
R652	RES	8
R653	RES	8
R654	RES	8
R655	RES	8
R656	RES	8
R657	RES	8
R658	RES	8
R659	RES	25
R660	RES	33
R661	RES	25
R662	RES	33
R663	RES	31
R664	RES	8
R665	RES	8
R666	RES	8
R667	RES	8
R668	RES	8
R669	RES	8
R670	RES	8
R671	RES	33
R672	RES	33
R673	RES	31
R674	RES	9
R675	RES	33
R676	RES	33
R677	RES	8
R678	RES	8
R679	RES	8
R680	RES	8
R681	RES	8
R682	RES	8
R683	RES	8
R684	RES	8
R685	RES	8
R686	RES	25
R687	RES	25
R688	RES	25
R689	RES	25
R690	RES	31
R691	RES	9
R692	RES	6
R693	RES	8
R694	RES	8
R695	RES	8
R696	RES	8
R697	RES	8
R698	RES	8
R699	RES	8
R700	RES	25
R701	RES	25
R702	RES	25
R703	RES	25
R704	RES	25
R705	RES	25
R706	RES	33
R707	RES	6
R708	RES	33
R709	RES	6
R710	RES	30
R711	RES	30
R712	RES	6
R713	RES	30
R714	RES	18
R715	RES	30
R716	RES	30
R717	RES	30
R718	RES	18
R719	RES	18
R720	RES	30
R721	RES	18
R722	RES	18
R723	RES	18
R724	RES	18
R725	RES	30
R726	RES	18
R727	RES	30
R728	RES	30
R729	RES	30
R730	RES	30
R731	RES	30
R732	RES	30
R733	RES	30
R734	RES	30
R735	RES	30
R736	RES	30
R737	RES	24
R738	RES	30
R739	RES	24
R740	RES	30
R741	RES	30
R742	RES	30
R743	RES	33
R744	RES	30
R745	RES	30
R746	RES	14
R747	RES	24
R748	RES	5
R749	RES	25
R750	RES	22
R751	RES	25
R752	RES	25
R753	RES	22
R754	RES	23
R757	RES	33
R760	RES	20
R761	RES	20
R762	RES	20
R763	RES	20
R764	RES	20
R765	RES	20
R766	RES	20
R767	RES	20

R768	RES	25
R769	RES	25
R770	RES	25
R771	RES	25
R772	RES	25
R773	RES	25
R774	RES	25
R777	RES	28
R779	RES	20
R786	RES	20
R787	RES	21
R788	RES	21
R789	RES	23
R790	RES	33
R791	RES	33
R792	RES	33
R794	RES	33
R795	RES	33
R796	RES	33
R797	RES	33
R798	RES	17
R806	RES	25
R807	RES	25
R808	RES	25
R817	RES	25
R818	RES	19
R819	RES	19
R823	RES	19
R824	RES	19
R825	RES	19
R826	RES	19
R827	RES	19
R828	RES	19
R829	RES	19
R830	RES	19
R832	RES	19
R833	RES	19
R835	RES	19
R836	RES	19
R837	RES	19
R838	RES	19
R839	RES	19
R840	RES	20
R841	RES	21
R842	RES	21
R843	RES	21
RP1	RPAK10P2C	18
RP2	RPAK4P	8
RP3	RPAK4P	8
RP4	RPAK4P	14
RP5	RPAK4P	14
RP6	RPAK4P	14
RP7	RPAK4P	14
RP8	RPAK4P	14
RP9	RPAK4P	9
RP10	RPAK4P	13
RP11	RPAK4P	14
RP12	RPAK4P	9
RP13	RPAK4P	14
RP14	RPAK4P	9
RP15	RPAK4P	14
RP16	RPAK4P	13
RP17	RPAK4P	9
RP18	RPAK4P	24
RP19	RPAK4P	24
RP20	RPAK4P	9
RP21	RPAK4P	24
RP22	RPAK4P	9
RP23	RPAK4P	24
RP24	RPAK4P	24
RP25	RPAK4P	24
RP26	RPAK4P	24
RP27	RPAK4P	24
RP28	RPAK4P	24
RP29	RPAK4P	9
RP30	RPAK4P	24
RP31	RPAK4P	9
RP32	RPAK4P	13
RP33	RPAK4P	12
RP34	RPAK4P	12
RP35	RPAK4P	13
RP36	RPAK4P	12
RP37	RPAK4P	27
RP38	RPAK4P	27
RP39	RPAK4P	29
RP40	RPAK10P2C	23
RP41	RPAK4P	29
RP42	RPAK10P2C	23
RP43	RPAK4P	17
RP44	RPAK4P	17
RP45	RPAK4P	17
RP46	RPAK10P2C	6
RP47	RPAK4P	14
RP49	RPAK4P	19
RP50	RPAK4P	19
RP51	RPAK4P	19
RP52	RPAK4P	19
RP53	RPAK2P	19
RP54	RPAK2P	19
RP55	RPAK2P	19
RP56	RPAK2P	19
RP57	RPAK2P	19
RP58	RPAK2P	19
RP59	RPAK2P	19
RP60	RPAK4P	19
SH1	SHLD_3P_EMI	4
U1	COMPARATOR_LMC7211	30
U2	NC7S32	22
U3	AMP_MAX4172	30
U4	PWR_CNTRL_TPS2211	18
U6	MAX1772	30
U7	MAX1717	33
U8	PCI5100GU	18
U9	SN74AUC1G08	6
U10	SN74AUC1G08	6
U11	FEPR_1MX8	9
U12	SN74AUC1G04	7
U13	LTC1625	31
U14	COMPARATOR_LMC7211	31
U15	P13B3257	33
U16	CBTV4020	10
U17	UPD72010_FBGA	17
U18	CBTV4020	10
U19	MAX1715	34
U20	NC7S32	29
U21	741125	23
U22	VREG_LP2951	31
U23	VREG_LP2951	31
U24	NC7S32	29
U25	NC7S32	29
U26	MAX6804	29
U27	CBTV4020	10
U28	CBTV4020	10
U29	M16C62	29
U30	CLK_GEN_CY25811	19
U31	CLK_GEN_CY28512	14
U32	LTC1778	20
U33	COMPARATOR_LMC7211	29
U34	VREG_MM1571	21
U35	LTC3707	32
U36	TSB81BA3A	27
U37	VREG_LM2594	27
U38	VREG_LT1962	27
U39	741G32	22
U40	741G32	22
U42	COMPARATOR_LMC7211	22
U43	TRANSCEIVER_88E1111	26
U44	LTC1761	27
U45	LTC3405	26
U46	LTC3411	34
U47	RAGE_MBLTY_M10_CSP64_667	19 20 21
U48	TRA_SI6467BDQ	34
U49	VREG_LT1962	14
U50	TRA_SI3447DV	34
U51	INTREPID 8 9 12 13 14 15	
U52	EEPROM_32KX8_M24256B	6
U53	ADT7460	25
U54	AT90S1200	6
U55	OPAMP_LMC7111	30
U56	APOLLO_MPC744S_360	5 6
U57	COMPARATOR_LMC7211	30
U58	SIL1162	19
U60	VREG_MM1571	21
XW1	SHORT	30
XW2	SHORT	33
XW3	SHORT	31
XW4	SHORT	20
XW5	SHORT	20

XW6	SHORT	20
XW7	JUMPER	21
XW8	SHORT	34
XW9	SHORT	20
XW10	SHORT	34
XW11	SHORT	20
XW12	SHORT	20
XW13	SHORT	32
XW14	SHORT	22
XW15	SHORT	22
XW16	JUMPER	32
XW17	SHORT	34
XW18	JUMPER	34
XW19	JUMPER	20
XW20	JUMPER	32
XW21	SHORT	34
XW22	JUMPER	34
XW23	SHORT	34
XW24	JUMPER	34
XW25	SHORT	34
XW26	JUMPER	31
XW27	SHORT	33
XW28	SHORT	33
XW29	SHORT	33
XW30	SHORT	25
XW31	SHORT	32
XW32	SHORT	32
XW34	SHORT	5
Y1	CRYSTAL	17
Y2	CRYSTAL	14
Y3	CRYSTAL_4PIN	29
Y4	CRYSTAL	29
Y5	CRYSTAL_4PIN	26
ZT1	HOLE_VIA	4
ZT2	HOLE_VIA	4
ZT3	HOLE_VIA	4
ZT4	HOLE_VIA	4
ZT5	HOLE_VIA	4
ZT6	HOLE_VIA	4
ZT7	HOLE_VIA	4
ZT8	HOLE_VIA	4
ZT9	HOLE_VIA	4
ZT10	HOLE_VIA	4
ZT11	HOLE_VIA	4
ZT12	HOLE_VIA	4
ZT13	HOLE_VIA	4
ZT14	HOLE_VIA	4
ZT15	HOLE_VIA	4
ZT16	HOLE_VIA	4
ZT17	HOLE_VIA	4
ZT18	HOLE_VIA	4
ZT19	HOLE_VIA	4
ZT20	HOLE_VIA	4
ZT21	HOLE_VIA	4
ZT22	HOLE_VIA	4
ZT23	HOLE_VIA	4
ZT24	HOLE_VIA	4
ZT25	HOLE_VIA	4
ZT26	HOLE_VIA	4
ZT27	HOLE_VIA	4
ZT28	HOLE_VIA	4
ZT29	HOLE_VIA	4
ZT30	HOLE_VIA	4
ZT31	HOLE_VIA	4
ZT32	HOLE_VIA	4
ZT33	HOLE_VIA	4
ZT34	HOLE_VIA	4
ZT35	HOLE_VIA	4
ZT36	HOLE_VIA	4
ZT37	HOLE_VIA	4
ZT38	HOLE_VIA	4
ZT39	HOLE_VIA	4
ZT40	HOLE_VIA	4
ZT41	HOLE_VIA	4
ZT42	HOLE_VIA	4
ZT43	HOLE_VIA	4
ZT44	HOLE_VIA	4
ZT45	HOLE_VIA	4
ZT46	HOLE_VIA	4
ZT47	HOLE_VIA	4
ZT48	HOLE_VIA	4
ZT49	HOLE_VIA	4
ZT50	HOLE_VIA	4
ZT51	HOLE_VIA	4
ZT52	HOLE_VIA	4
ZT53	HOLE_VIA	4
ZT54	HOLE_VIA	4
ZT55	HOLE_VIA	4
ZT56	HOLE_VIA	4
ZT57	HOLE_VIA	4
ZT58	HOLE_VIA	4
ZT59	HOLE_VIA	4
ZT60	HOLE_VIA	4
ZT61	HOLE_VIA	4
ZT62	HOLE_VIA	4
ZT63	HOLE_VIA	4
ZT64	HOLE_VIA	4
ZT65	HOLE_VIA	4
ZT66	HOLE_VIA	4
ZT67	HOLE_VIA	4
ZT68	HOLE_VIA	4
ZT69	HOLE_VIA	4
ZT70	HOLE_VIA	4
ZT71	HOLE_VIA	4
ZT72	HOLE_VIA	4
ZT73	HOLE_VIA	4
ZT74	HOLE_VIA	4
ZT75	HOLE_VIA	4
ZT76	HOLE_VIA	4
ZT77	HOLE_VIA	4
ZT78	HOLE_VIA	4
ZT79	HOLE_VIA	4
ZT80	HOLE_VIA	4
ZT81	HOLE_VIA	4
ZT82	HOLE_VIA	4
ZT83	HOLE_VIA	4
ZT84	HOLE_VIA	4
ZT85	HOLE_VIA	4
ZT86	HOLE_VIA	4