1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
A		285476	PRODUCTION RELEASED	07/28/03	?

SCHEM,MLB,PB17"

07/28/2003

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2	SYSTEM BLOCK DIAGRAM
3	POWER BLOCK DIAGRAM
4	PCB NOTES AND HOLES
5	MPC7450 MAXBUS INTERFACE
6	MPC7450 DATA
7	CPU PLL AND CONFIGURATION STRAPS
8	INTREPID MAXBUS AND BOOT STRAPS
9	INTREPID MEMORY INTERFACE / BOOT ROM
10	DDR MEMORY MUXES
11	200PIN DDR MEMORY SODIMM CONNECTORS
12	INTREPID AGP 4X/PCI
13	INTREPID ENET/FW/UATA/EIDE INTERFACES
14	INTREPID GPIOS/SERIAL/USB INTERFACES/SSCG
15	INTREPID POWER RAILS
16	INTREPID DECOUPLING
17	CARDBUS CONTROLLER (PCI1510)
18	M10 AGP & CLOCKS
19	M10 LVDS/TMDS/VGA/GPIO & GPU VCORE
20	M10 ANALOG, POWER, GND
21	VIDEO CONNECTORS - INVERTER, DVI, S-VIDEO DUAL-CHANNEL LVDS

PAGE	CONTENTS
22	LMU, LIGHT SENSOR, BOOTBANGER, SLEEP LED SPIDEY - KBD,TPAD,HALL EFFECT,PWR BUTTON
23	INTERNAL CONNECTORS - DVD, CARDSLOT, HARD DRIVE, LEFT USB/BLUETOOTH
24	FAN CONTROLLER, MODEM, SOUND SERIAL DEBUG (JOLLY ROGER, PWR/NMI/RESET)
25	USB 2.0
26	MARVELL GIGABIT ETHERNET PHY
27	FIREWIRE A/B PHY
28	FIREWIRE A/B CONNECTORS, PORT POWER LIMITER
29	PMU (POWER MANAGEMENT UNIT)
30	BATTERY CHARGER AND CONNECTOR
31	12.8V SYSTEM POWER SUPPLY / PMU POWER SUPPLY
32	3.3V / 5V SYSTEM POWER SUPPLIES
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35	SIGNAL CONSTRAINTS (1 OF 3) - DIGITAL/CLK
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40-41	SIGNAL NAMES
42-43	COMPONENT LOCATIONS

BOM OPTIONS	STUFF	NO STUFF
D3_HOT		✓
D3_COLD	✓	
GPU_SS	✓	
GPU_SWITCH	✓	
SERIAL_DEBUG	✓	
VCORE_OFFSET	✓	
1_8V_MAXBUS	✓	
1_5V_MAXBUS		✓
NEC_USB	✓	
INTREPID_USB		✓
BBANG		✓
NO_BBANG	✓	
ATI_MEMIO_HI	✓	
ATI_MEMIO_LO		✓
SSCG		✓
NO_SSCG	✓	
5V_HD_LOGIC	✓	
3V_HD_LOGIC		✓
EXT_TMDS	✓	
INT_TMDS		✓

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6459	1	SCHEM,MLB,PB17 INCH	SCH1	
820-1524	1	PCBF,MLB,PB17 INCH	PCB1	

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES °
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

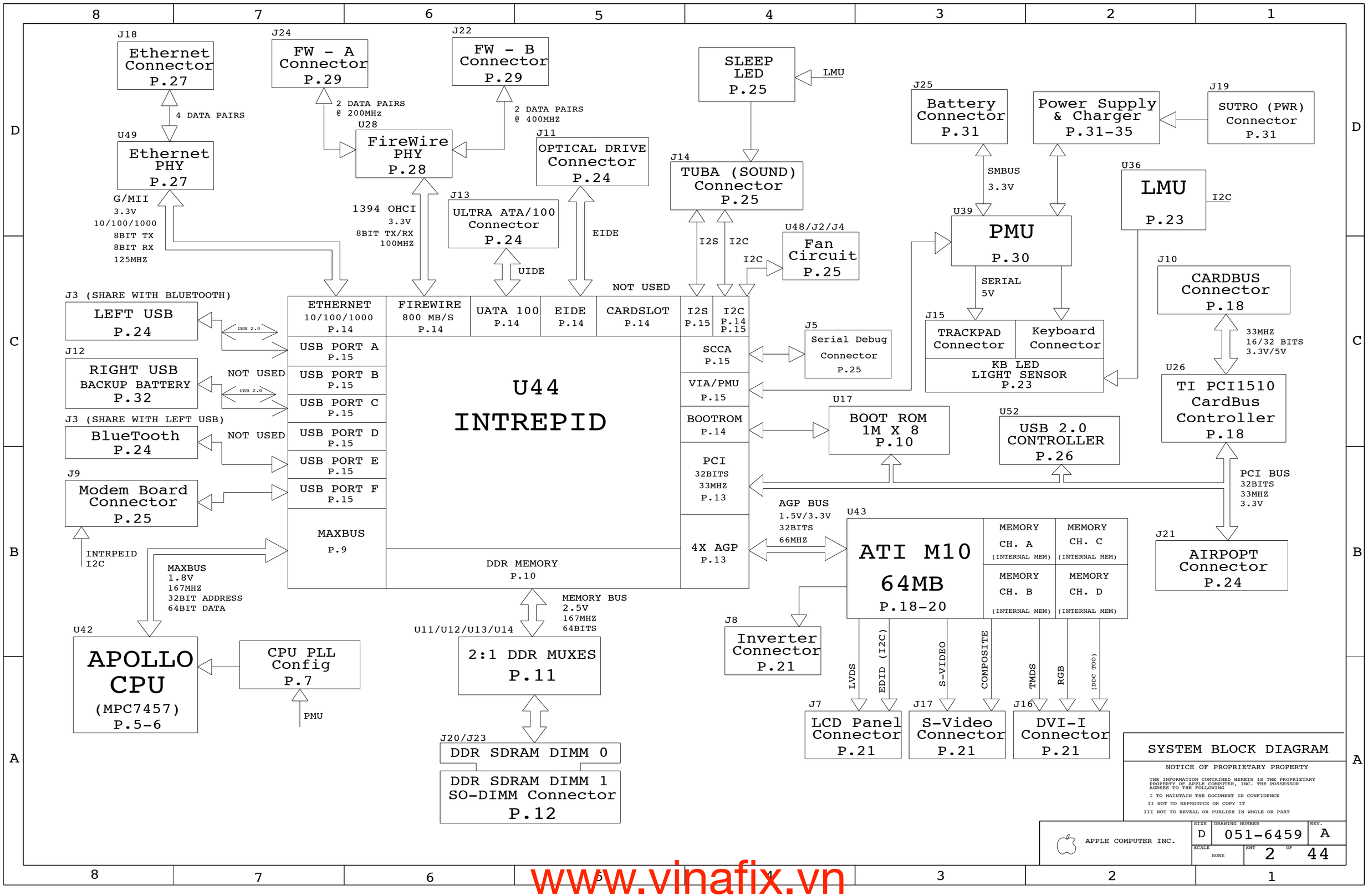
METRIC

DRAFTER | DESIGN CK
ENG APPD | MFG APPD
QA APPD | DESIGNER
RELEASE | SCALE NONE
MATERIAL/FINISH NOTED AS APPLICABLE
SIZE D

Apple Computer Inc.

TITLE
SCHEM,MLB,PB17 INCH

DRAWING NUMBER 051-6459 REV. A
SHT 1 OF 44



POWER SYSTEM ARCHITECTURE

AC ADAPTER IN PG 31

INRUSH LIMITER PG 30

+24V_PBUS

1V20_REF
U21 PG 31
>-13.44V TURNS-ON
<-13.44V SHUTS-OFF

RUN/SS
BUCK REGULATOR (LTC1625) PG 32
VCC
AC: 12.8V
NO AC: BATTERY VOLTAGE
1625 NOT RUNNING
SHUTDOWN: RUNNING
SLEEP: RUNNING
RUN: RUNNING

+PBUS (12.8V)

BACKLIGHT INVERTER

+5V_MAIN
VCC
MAIN 2.5V/1.5V DC/DC (MAX1715) PG 35
PGOOD
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING
TURNS ON OUTPUT @ 2.4V ON1/ON2

MAP31 DDR I/O
MAP31 DDR CORE
DDR POWER
+2.5V_MAIN
1_5V_2_5V_OK
+1.5V_MAIN
INTREPID CORE
AGP I/O

+PBUS

DCDC_EN
SLEEP
MAXBUS SEQUENCING

+5V_MAIN
VCC
SHDN
DC/DC (MAX1717) PG 34
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING
CPU_VCORE (+1.4V/+1.5V)

14V_PBUS

+3V_PMU LDO PG 32
+BATT
+5V_MAIN
+3V_PMU
+4_6V_BU

RC AT 1M*0.047UF @ 24V
STARTS 2.0MSEC AFTER DCDC_EN_L BECOMES LOW

RUN/SS - 5V
TURNS ON AT >1V
<100UA ALLOWED
INTERNAL ZENER CLAMP TO 6V
MAIN 3V/5V DC/DC (LTC3707) PG 33
VCC
PGOOD
STBYMD
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING
INTERNAL ZENER CLAMP TO 6V
<100UA ALLOWED
TURNS ON AT >1V
RUN/SS - 3V

+5V_MAIN
3V_5V_OK
HOLDS BOTH RUN/SS AT GND WHEN IT'S CONNECTED TO GND
TURNS CONTROL TO RUN/SS WHEN IT'S OPEN
+3.3V_MAIN

DCDC_EN_L
AFTER PMU IS UP AND RUNNING
DCDC_EN_L WILL PULL ON1/ON2 LOW IN SHUTDOWN

+5V_MAIN
+PBUS (12.8V)
VCC
EXT_VCC
DC/DC (LTC1778) PG 20
SHUTDOWN: STOPPED
SLEEP: D3HOT/D3COLD
RUN: RUNNING
TURNS ON AS LOW AS 0.8V/TYP 1.5V
INTERNAL 1.2UA CURRENT SOURCE
RUN/SS
GPU_VCORE +1.2V/+1.0V

DCDC_EN
SLEEP
D3_COLD
GPU_VCORE SEQUENCING
1M & 0.1UF @14V, IT TAKES ~5.88MS TO START SWITCHER
1_5V_2_5V_OK
D3_HOT
DCDC_EN_L
D3_HOT
1_5V_2_5V_OK WILL NOT PULL LOW UNTIL +5V_MAIN TURNS ON
HOWEVER, 5V SHOULD TURN ON ~2.23MS AFTER DCDC_EN_L OR PMU_POWERUP_L BECOMES '1'; MUCH LESS THAN THE RC CHARGING AT INT_VCC (5V)

+PBUS
BACKUP BATTERY
12.8V CHARGES BACKUP BATTERY
24V IS OUTPUT ONLY FROM BACKUP BATTERY
CHARGER INPUT & BOOST OUTPUT PG 32
BACKUP BATTERY CIRCUIT CHARGES OFF +PBUS AND PREVENTS +PBUS AND +24V_PBUS FROM DROPPING BELOW 6V (UNTIL DRAINED)

RC AT 1M*0.1UF @ 24V
STARTS ~4.25MSEC AFTER DCDC_EN_L BECOMES LOW
NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED
+24V_PBUS

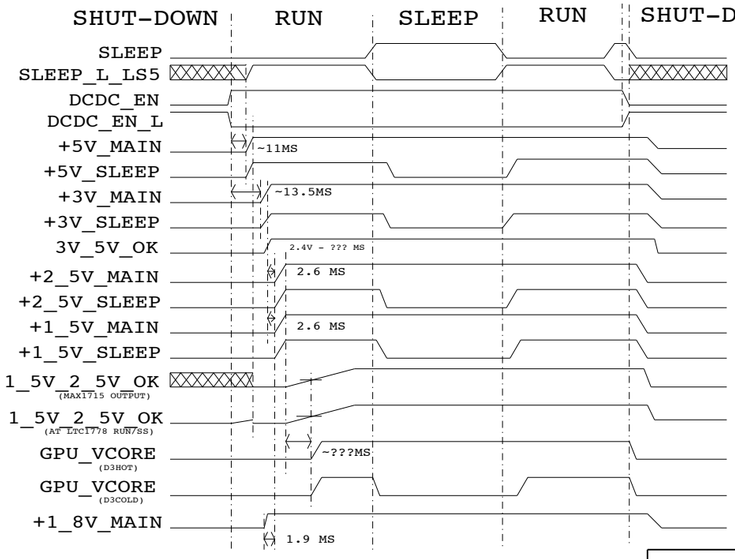
DC/DC (LTC3411) PG 35
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING
+1.8V_MAIN
MAXBUS BROADCOM

BATTERY CHARGER (MAX1772) PG 31
+BATT

3S 3P PRISMATIC CELLS

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED
BATTERY VOLTAGE FEED-IN PATH PG 31
+PBUS

SHUT-DOWN | RUN | SLEEP | RUN | SHUT-DOWN



POWER BLOCK DIAGRAM

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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6459	A
SCALE: NONE	SHT 3 OF 44	

PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 12
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

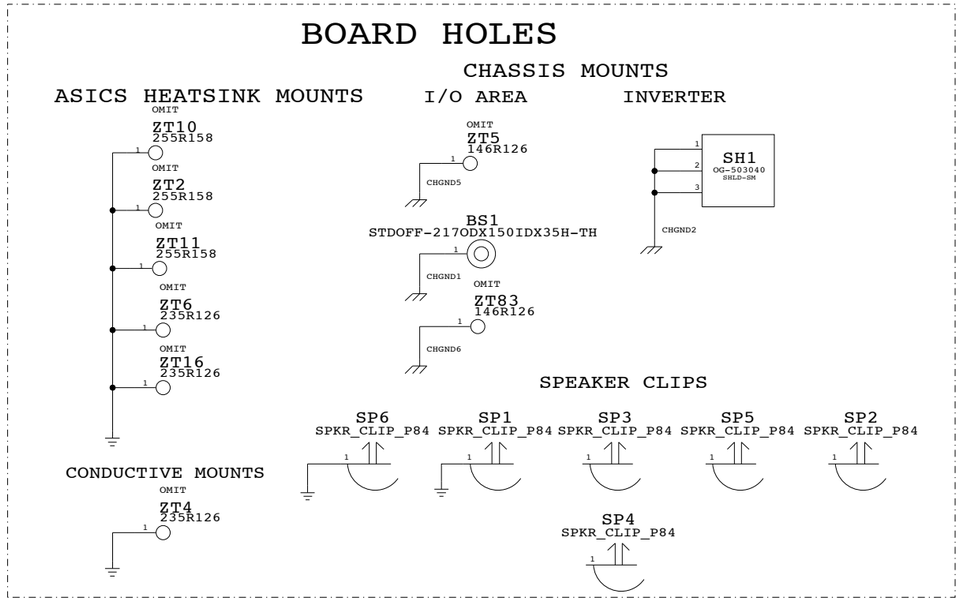
SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

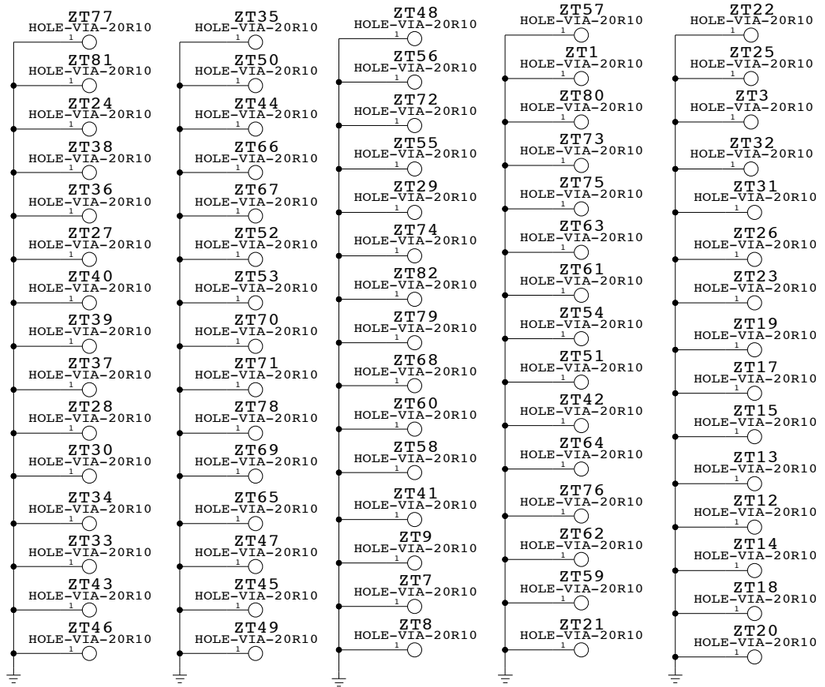
20R10 TH VIA OR VIA IN PAD

1		SIGNAL (1/3 OZ + COPPER PLATING)
2	PREPREG (3MIL)	GROUND (1/2 OZ)
3	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
4	PREPREG (3MIL)	SIGNAL (1/2 OZ)
5	LAMINATE (4MIL)	GROUND (1/2 OZ)
6	PREPREG (2MIL)	CUT POWER PLANE(1 OZ)
7	LAMINATE (3MIL)	CUT POWER PLANE(1 OZ)
8	PREPREG (2MIL)	GROUND (1/2 OZ)
9	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
10	PREPREG (3MIL)	SIGNAL (1/2 OZ)
11	LAMINATE (4MIL)	GROUND (1/2 OZ)
12	PREPREG (3MIL)	SIGNAL (1/3 OZ + COPPER PLATING)

BOARD HOLES



GROUND VIAS

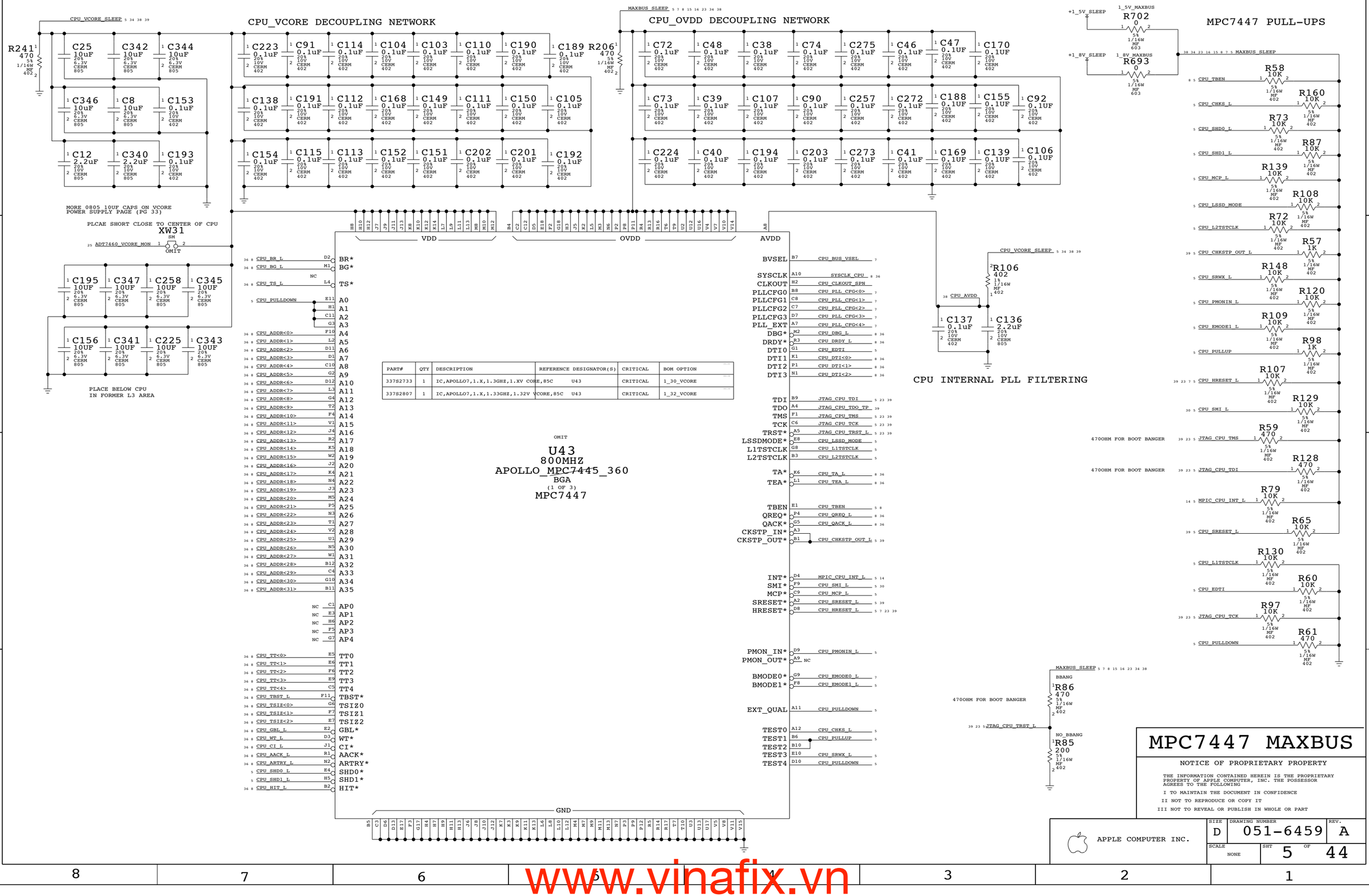


BOARD INFORMATION

APPLE COMPUTER INC.

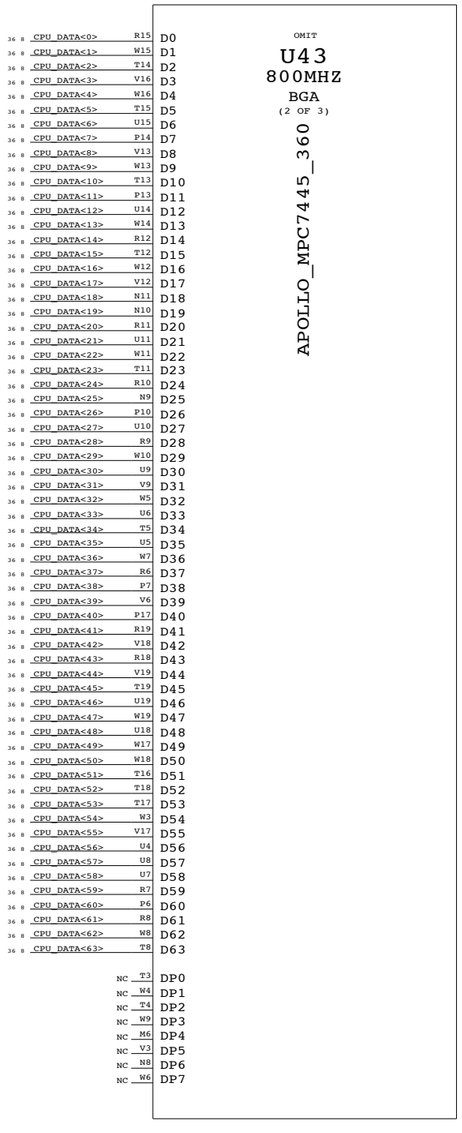
SIZE	DRAWING NUMBER	REV.
D	051-6459	A

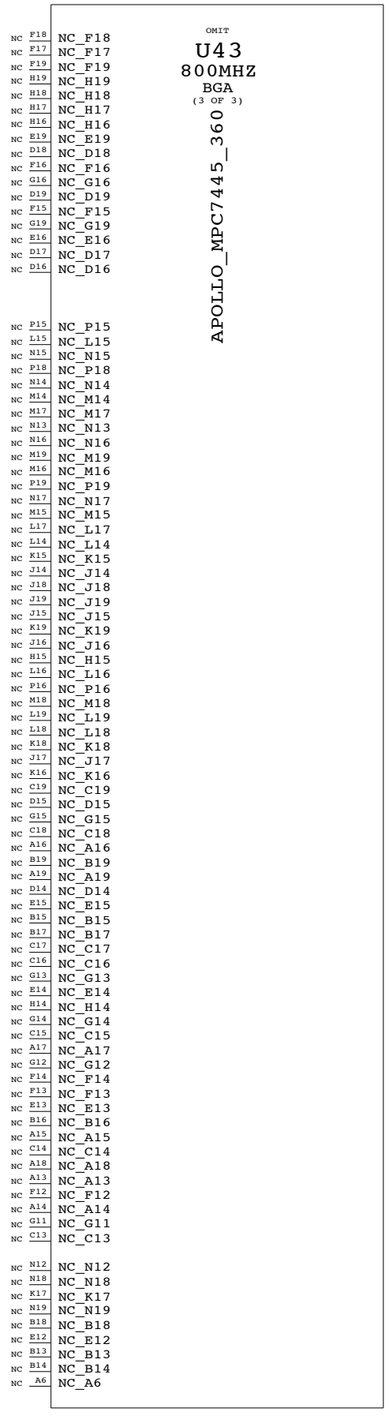
SCALE	SHT	OF
NONE	4	44



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33782733	1	IC,APOLLO7,1.X,1.3GHZ,1.XV CORE,85C	U43	CRITICAL	1_30_VCORE
33782807	1	IC,APOLLO7,1.X,1.33GHZ,1.32V VCORE,85C	U43	CRITICAL	1_32_VCORE

BOOT BANGER - LMU PERORMS THIS FUNCTION IF NEEDED
SEE PAGE 22





MPC7447/BBANG

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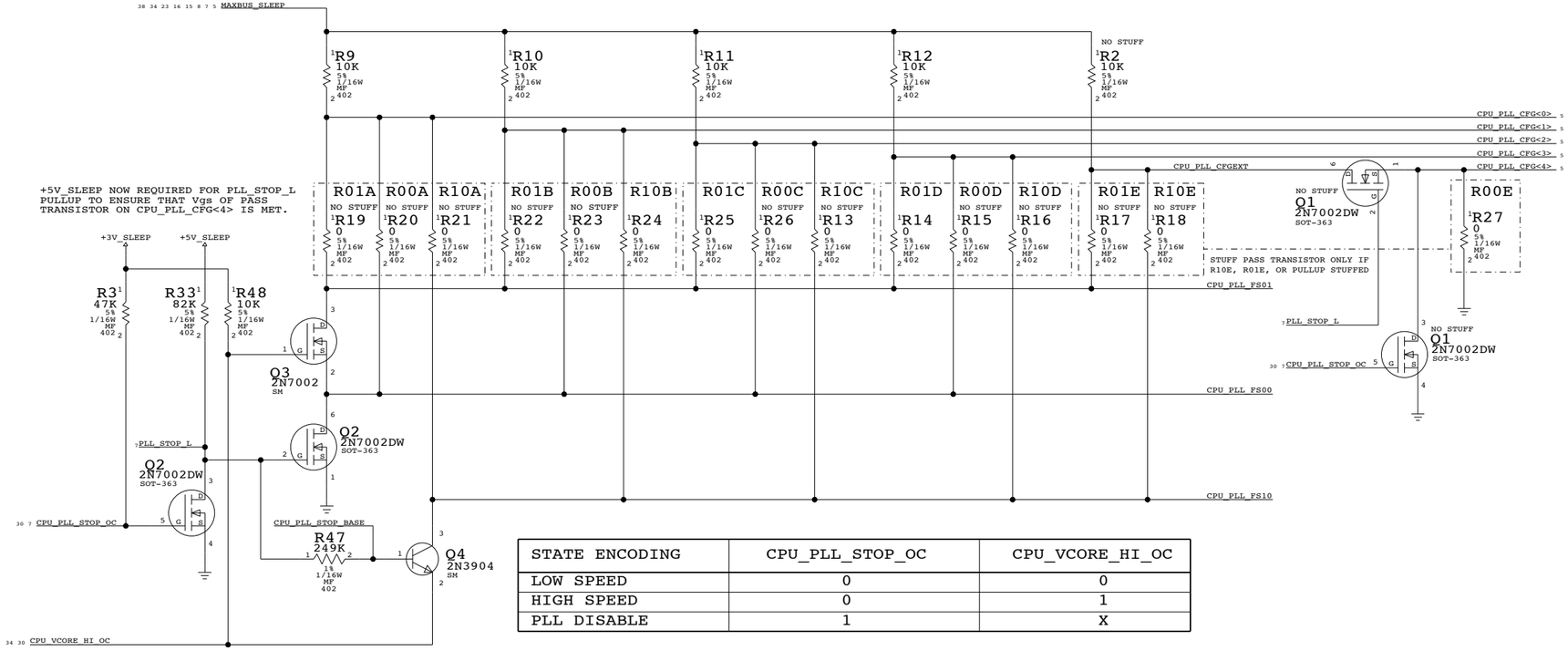
SIZE	DRAWING NUMBER	REV.
D	051-6459	A
SCALE: NONE	SHT 6 OF 44	

CPU PLL CONFIG CIRCUITRY



STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

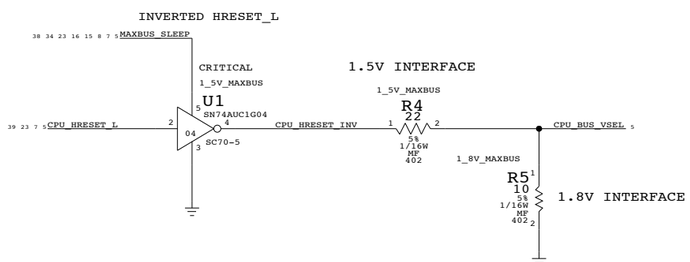
CPU FREQUENCY CONFIGURATION

APOLLO 7

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ (MHZ)	133MHZ (MHZ)	CPU_PLL_CFG 4 E	0123 ABCD	HEX
0.0X	PLL OFF		0	1111	0F
1.0X	PLL BYPASS		0	0011	03
2.0X	333	267	0	0100	04
3.0X	500	400	0	1000	08
4.0X	667	533	0	1010	0A
5.0X	833	667	0	1011	0B
5.5X	917	733	0	1001	09
6.0X	1000	800	0	1101	0D
6.5X	1083	867	0	0101	05
7.0X	1167	933	0	0010	02
7.5X	1250	1000	0	0001	01
8.0X	1333	1067	0	1100	0C
8.5X	1417	1133	0	0110	06
9.0X	1500	1200	1	0111	17
9.5X	1583	1267	0	0111	07
10.0X	1667	1333	1	1010	1A
10.5X	1750	1400	1	1000	18
11.0X	1833	1467	1	1001	19
11.5X	1917	1533	0	0000	00
12.0X	2000	1600	1	1011	1B
12.5X	2083	1667	1	1111	1F
13.0X	2167	1733	1	0101	15
13.5X	2250	1800	0	1110	0E
14.0X	2333	1867	1	1100	1C
15.0X	2500	2000	1	0001	11
16.0X	2667	2133	1	1101	1D
17.0X	2833	2267	1	0000	10
18.0X	3000	2400	1	0010	12
20.0X	3333	2667	1	0011	13
21.0X	3500	2800	1	0100	14
24.0X	4000	3200	1	0110	16
28.0X	4667	3733	1	1110	1E

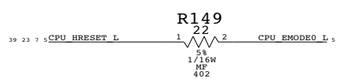
CPU CONFIGURATION

MAXBUS VSEL



DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L NEED TO CHARACTERIZE

BUSTYPE SELECT



APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

CPU CONFIGURATION

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6459 | REV. A

SCALE NONE | SHT 7 OF 44

INTREPID BOOT STRAPS

BIT 32 TO 39

MAXBUS_SLEEP

R642	R135	R123	R153	R166	R179	R651	R178
NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF
CPU_DATA<32>	CPU_DATA<33>	CPU_DATA<34>	CPU_DATA<35>	CPU_DATA<36>	CPU_DATA<37>	CPU_DATA<38>	CPU_DATA<39>

R136	R643	R639	R657	R664	R673	R143	R674
0: PCIE_CLK_REQ_L input (GND) 1: TRI state output	Reserved 0: normal 1: active	Reserved 0: normal 1: active	Reserved 0: normal 1: active	spare	spare	spare	spare

BIT 40 TO 47

MAXBUS_SLEEP

R122	R142	R164	R134	R184	R177	R152	R165
NO STUFF	NO STUFF	NO STUFF	SSCG	NO STUFF	NO_SSCG	NO_SSCG	NO_SSCG
CPU_DATA<40>	CPU_DATA<41>	CPU_DATA<42>	CPU_DATA<43>	CPU_DATA<44>	CPU_DATA<45>	CPU_DATA<46>	CPU_DATA<47>

R640	R652	R665	R644	R683	R675	R658	R666
Spare	Spare	Spare	NO_SSCG	Spare	SSCG	SSCG	SSCG

BIT2 BIT1 BIT0

PLL4MODESEL_NXT[2:0]
000: 166.4MHZ (2.5X)
001: 149.76MHZ
010: 133.12MHZ (2.0X)
011: 99.84MHZ (1.5X)
100: 83.20MHZ

MODE A (2.5X) IS FOR STATIC OPERATION
MODE C (2.0X) IS FOR CLOCK SLEW OPERATION

InternalSpreadEn 0: PLL1 (NO SPREAD) 1: Active

PCIE_Source Clock 0: PLL1 (NO SPREAD) 1: PLL3 (NO SPREAD)

BIT 48 TO 55

MAXBUS_SLEEP

R133	R121	R163	R151	R162	R141	R183	R176
SSCG	SSCG	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF
CPU_DATA<48>	CPU_DATA<49>	CPU_DATA<50>	CPU_DATA<51>	CPU_DATA<52>	CPU_DATA<53>	CPU_DATA<54>	CPU_DATA<55>

R645	R641	R668	R659	R667	R653	R684	R676
NO_SSCG	NO_SSCG	NO STUFF	Spare	Spare	Spare	NO STUFF	Spare

BUF_REF_CLK_OUTEnable_h 0: Disabled 1: Active

SelPll4ExtSrc 0: Internal source 1: External source

TRI 134b workaround 0: Normal 1: TRI PHY workaround

BIT2 BIT1 BIT0

MaxBus output impedance
111: 28.6 ohm
011: 33.3 ohm
101: 40 ohm
001: 50 ohm
110: 66.6 ohm
010: 100 ohm
100: 200 ohm
000: 200 ohm

R227 4.7 5% 1/16W MF 402

C308 0.22UF 20% 6.3V CERM 402

+1_5V_INTREPID_PLL → +1_5V_INTREPID_PLL7

THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:
1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
2/ D46 - SELPCI1SPREADCLK - SLEEP/WAKE CYCLE REQUIRED
3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT

IF A STRAP IS NOT LISTED, THEN
IT CANNOT BE CHANGED BY SOFTWARE

VDD15A_7 (PLL6) H26
CRITICAL

U45
INTREPID-REV2.1
BGA
(1 OF 9)

CPU_BR_L	E29	BR	INPUT
CPU_BG_L	E26	BG	NO BUS KEEPER
CPU_TS_L	B27	TS	NO BUS KEEPER
CPU_ADDR<0>	D24	A_0	
CPU_ADDR<1>	D25	A_1	
CPU_ADDR<2>	A27	A_2	
CPU_ADDR<3>	E24	A_3	
CPU_ADDR<4>	G23	A_4	
CPU_ADDR<5>	B26	A_5	
CPU_ADDR<6>	A26	A_6	
CPU_ADDR<7>	D23	A_7	
CPU_ADDR<8>	A25	A_8	
CPU_ADDR<9>	E23	A_9	
CPU_ADDR<10>	J22	A_10	
CPU_ADDR<11>	B25	A_11	
CPU_ADDR<12>	H22	A_12	
CPU_ADDR<13>	G22	A_13	
CPU_ADDR<14>	D22	A_14	
CPU_ADDR<15>	B24	A_15	
CPU_ADDR<16>	B23	A_16	
CPU_ADDR<17>	E22	A_17	
CPU_ADDR<18>	J21	A_18	
CPU_ADDR<19>	G21	A_19	
CPU_ADDR<20>	E21	A_20	
CPU_ADDR<21>	A24	A_21	
CPU_ADDR<22>	D21	A_22	
CPU_ADDR<23>	A23	A_23	
CPU_ADDR<24>	H20	A_24	
CPU_ADDR<25>	B22	A_25	
CPU_ADDR<26>	H21	A_26	
CPU_ADDR<27>	A22	A_27	
CPU_ADDR<28>	E20	A_28	
CPU_ADDR<29>	B21	A_29	
CPU_ADDR<30>	D20	A_30	
CPU_ADDR<31>	A21	A_31	
CPU_CI_L	G26	CI	
CPU_GBL_L	A29	GBL	
CPU_TBST_L	A28	TBST	
CPU_TSIZ<0>	G24	TSIZ_0	
CPU_TSIZ<1>	H24	TSIZ_1	
CPU_TSIZ<2>	D26	TSIZ_2	
CPU_TT<0>	E25	TT_0	
CPU_TT<1>	G25	TT_1	
CPU_TT<2>	B28	TT_2	
CPU_TT<3>	D27	TT_3	
CPU_TT<4>	J25	TT_4	
CPU_WT_L	D28	WT	
CPU_AACK_L	B29	AACK	NO BUS KEEPER - PU
CPU_ARTRY_L	H23	ARTRY	NO BUS KEEPER - PU
CPU_HIT_L	B31	HIT	INPUT - PU
CPU_QREQ_L	A32	QREQ	INPUT - PD
CPU_QACK_L	G27	QACK	NO BUS KEEPER - ?
INT_SUSPEND_REQ_L	AK9	SUSPENDREQ	
INT_SUSPEND_ACK_L	AM8	SUSPENDACK	

MAXBUS INTERFACE

D_0	D10	CPU_DATA<0>	6 36
D_1	G12	CPU_DATA<1>	6 36
D_2	E11	CPU_DATA<2>	6 36
D_3	H11	CPU_DATA<3>	6 36
D_4	B9	CPU_DATA<4>	6 36
D_5	B8	CPU_DATA<5>	6 36
D_6	A9	CPU_DATA<6>	6 36
D_7	A8	CPU_DATA<7>	6 36
D_8	E12	CPU_DATA<8>	6 36
D_9	D11	CPU_DATA<9>	6 36
D_10	B10	CPU_DATA<10>	6 36
D_11	J13	CPU_DATA<11>	6 36
D_12	A10	CPU_DATA<12>	6 36
D_13	D12	CPU_DATA<13>	6 36
D_14	E13	CPU_DATA<14>	6 36
D_15	G13	CPU_DATA<15>	6 36
D_16	B11	CPU_DATA<16>	6 36
D_17	D13	CPU_DATA<17>	6 36
D_18	A11	CPU_DATA<18>	6 36
D_19	G14	CPU_DATA<19>	6 36
D_20	H14	CPU_DATA<20>	6 36
D_21	E14	CPU_DATA<21>	6 36
D_22	B12	CPU_DATA<22>	6 36
D_23	G15	CPU_DATA<23>	6 36
D_24	B13	CPU_DATA<24>	6 36
D_25	H15	CPU_DATA<25>	6 36
D_26	D14	CPU_DATA<26>	6 36
D_27	B14	CPU_DATA<27>	6 36
D_28	A12	CPU_DATA<28>	6 36
D_29	G16	CPU_DATA<29>	6 36
D_30	E15	CPU_DATA<30>	6 36
D_31	J16	CPU_DATA<31>	6 36
D_32	D15	CPU_DATA<32>	6 8 36
D_33	A14	CPU_DATA<33>	6 8 36
D_34	A13	CPU_DATA<34>	6 8 36
D_35	D16	CPU_DATA<35>	6 8 36
D_36	E16	CPU_DATA<36>	6 8 36
D_37	G17	CPU_DATA<37>	6 8 36
D_38	B15	CPU_DATA<38>	6 8 36
D_39	H17	CPU_DATA<39>	6 8 36
D_40	A15	CPU_DATA<40>	6 8 36
D_41	B16	CPU_DATA<41>	6 8 36
D_42	E17	CPU_DATA<42>	6 8 36
D_43	A16	CPU_DATA<43>	6 8 36
D_44	J18	CPU_DATA<44>	6 8 36
D_45	H18	CPU_DATA<45>	6 8 36
D_46	D17	CPU_DATA<46>	6 8 36
D_47	G18	CPU_DATA<47>	6 8 36
D_48	A17	CPU_DATA<48>	6 8 36
D_49	B17	CPU_DATA<49>	6 8 36
D_50	E18	CPU_DATA<50>	6 8 36
D_51	B18	CPU_DATA<51>	6 8 36
D_52	D18	CPU_DATA<52>	6 8 36
D_53	A18	CPU_DATA<53>	6 8 36
D_54	A19	CPU_DATA<54>	6 8 36
D_55	H19	CPU_DATA<55>	6 8 36
D_56	B19	CPU_DATA<56>	6 8 36
D_57	J19	CPU_DATA<57>	6 8 36
D_58	A20	CPU_DATA<58>	6 8 36
D_59	D19	CPU_DATA<59>	6 8 36
D_60	E19	CPU_DATA<60>	6 8 36
D_61	G19	CPU_DATA<61>	6 8 36
D_62	B20	CPU_DATA<62>	6 8 36
D_63	G20	CPU_DATA<63>	6 8 36
DBG	A30	CPU_DBG_L	5 8 36
DRDY	G28	CPU_DRDY_L	5 8 36
DTI_0	K25	CPU_DTI<0>	5 36
DTI_1	D29	CPU_DTI<1>	5 36
DTI_2	B30	CPU_DTI<2>	5 36
TA	E27	CPU_TA_L	5 8 36
TEA	E28	CPU_TEA_L	5 8 36

SYSCLK_LA_TP	G8		
CPU_CLK_EN	AH9	STOPCPUCLK	INPUT - PU
INTREPID_ACS_REF	H13	ACS_REF	NO BUS KEEPER - ?
			NO BUS KEEPER - ?
			NO BUS KEEPER - ?
SYSCLK_CPU_UF	J15	CPU_CLK	NO BUS KEEPER - PU
			NO BUS KEEPER - PU
CPU_TBEN	A31	TBEN	NO BUS KEEPER - PU

INTREPID OUTPUTS HIGH BY DEFAULT

VSSA_7 (PLL6) H25

Vin = Intrepid Vcore (1.5V)
Vout = MaxBus rail (1.8V)

FB BUFFER HAS 50 OHM OUTPUT IMPEDANCE

R197 511 1% 1/16W MF 402
R144 0 5% 1/16W MF 402
R137 1K 1% 1/16W MF 402

SHORT = 1" SHORTER THAN MATCHED LENGTH
LONG = 1" LONGER THAN MATCHED LENGTH

R167 0 5% 1/16W MF 402 — INT_CPUFB_OUT → INT_CPUFB_OUT_SHORT
R215 0 5% 1/16W MF 402 — INT_CPUFB_OUT_SHORT → INT_CPUFB_OUT_NORM
R207 0 5% 1/16W MF 402 — INT_CPUFB_OUT_NORM → INT_CPUFB_LONG
NO STUFF R225 0 5% 1/16W MF 402 — INT_CPUFB_OUT_SHORT → INT_CPUFB_IN
R208 0 5% 1/16W MF 402 — INT_CPUFB_OUT_NORM → INT_CPUFB_IN_NORM
R226 0 5% 1/16W MF 402 — INT_CPUFB_IN
NO STUFF R196 0 5% 1/16W MF 402 — INT_CPUFB_IN_NORM

MAXBUS PULL-UPS

MAXBUS_SLEEP

CPU_TS_L	RP21 10K	2 7
CPU_TA_L	RP21 10K	1 8
CPU_ARTRY_L	RP21 10K	4 5
CPU_BR_L	RP23 10K	1 8
CPU_HIT_L	RP24 10K	3 6
CPU_DRDY_L	RP23 10K	3 6
CPU_TEA_L	RP23 10K	4 5
CPU_AACK_L	RP23 10K	2 7
CPU_DBG_L	RP24 10K	4 5
CPU_BG_L	RP21 10K	3 6
CPU_QREQ_L	RP24 10K	2 7

All: 5% 1/16W SM1

INTREPID BOOT STRAPS

BIT 56 TO 63

MAXBUS_SLEEP

R140	R161	R175	R132	R131	R150	R174	R182
NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF
CPU_DATA<56>	CPU_DATA<57>	CPU_DATA<58>	CPU_DATA<59>	CPU_DATA<60>	CPU_DATA<61>	CPU_DATA<62>	CPU_DATA<63>

R654	R669	R677	R646	R647	R660	R678	R685
Spare	Spare	Spare	PCI1_RST2_L / PCI1_GNT2_L 0: GPIO 1: PCI1_GNT2_L	PCI1_RST1_L / PCI1_GNT1_L 0: GPIO 1: PCI1_GNT1_L	PCI1_RST0_L / PCI1_GNT0_L 0: GPIO 1: PCI1_GNT0_L	NO STUFF	PCIE_CLK_REQ_L 0: Legacy interface 1: B-mode interface

Disable PHY interface 0: Enable 1: Disable

Processor Bus Mode 0: 60X Bus (GS) 1: MPX Bus

Intrepid MaxBus

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6459	A
SCALE: NONE	SHT 8 OF 44	

SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

PINS ARE SWAPABLE FOR RPAKS

U45
INTREPID-REV2.1
BGA
(2 OF 9)
CRITICAL

DDR_DATA_0 … DDR_DATA_63

DDR MEMORY INTERFACE

DDR_A_0	H35	MEM_ADDR<0>
DDR_A_1	G35	MEM_ADDR<1>
DDR_A_2	G36	MEM_ADDR<2>
DDR_A_3	F36	MEM_ADDR<3>
DDR_A_4	F35	MEM_ADDR<4>
DDR_A_5	E35	MEM_ADDR<5>
DDR_A_6	E36	MEM_ADDR<6>
DDR_A_7	G32	MEM_ADDR<7>
DDR_A_8	D36	MEM_ADDR<8>
DDR_A_9	H36	MEM_ADDR<9>
DDR_A_10	G33	MEM_ADDR<10>
DDR_A_11	H33	MEM_ADDR<11>
DDR_A_12	D35	MEM_ADDR<12>
DDR_BA_0	L30	MEM_BA<0>
DDR_BA_1	M29	MEM_BA<1>
DDRCS_0	AN34	MEM_CS_L<0>
DDRCS_1	AN36	MEM_CS_L<1>
DDRCS_2	AL35	MEM_CS_L<2>
DDRCS_3	AL33	MEM_CS_L<3>
DDR_DQS_0	AJ31	MEM_DQS<0>
DDR_DQS_1	AH31	MEM_DQS<1>
DDR_DQS_2	AD32	MEM_DQS<2>
DDR_DQS_3	AB30	MEM_DQS<3>
DDR_DQS_4	V30	MEM_DQS<4>
DDR_DQS_5	P32	MEM_DQS<5>
DDR_DQS_6	N29	MEM_DQS<6>
DDR_DQS_7	L32	MEM_DQS<7>
DDR_DM_0	AJ33	MEM_DQM<0>
DDR_DM_1	AH33	MEM_DQM<1>
DDR_DM_2	AD33	MEM_DQM<2>
DDR_DM_3	AC35	MEM_DQM<3>
DDR_DM_4	T35	MEM_DQM<4>
DDR_DM_5	T33	MEM_DQM<5>
DDR_DM_6	N32	MEM_DQM<6>
DDR_DM_7	L33	MEM_DQM<7>
DDRRAS	L29	MEM_RAS_L
DDRCAS	H32	MEM_CAS_L
DDRWE	E30	MEM_WE_L
DDRCKE0	AM35	MEM_CKE<0>
DDRCKE1	AM35	MEM_CKE<1>
DDRCKE2	AM36	MEM_CKE<2>
DDRCKE3	AL36	MEM_CKE<3>
DDR_SELHI_0	AB32	MEM_MUXSEL_H<0>
DDR_SELHI_1	AE29	MEM_MUXSEL_H<1>
DDR_SELLO_0	N30	MEM_MUXSEL_L<0>
DDR_SELLO_1	T32	MEM_MUXSEL_L<1>
DDR_MCLK_0_P	Y32	SYSCLK_DDRCLK_A0_UF
DDR_MCLK_0_N	Y33	SYSCLK_DDRCLK_A0_L_UF
DDR_MCLK_1_P	Y35	SYSCLK_DDRCLK_A1_UF
DDR_MCLK_1_N	Y36	SYSCLK_DDRCLK_A1_L_UF
DDR_MCLK_2_P	Y30	INT_DDRCLK2_P_TP
DDR_MCLK_2_N	W30	INT_DDRCLK2_N_TP
DDR_MCLK_3_P	W32	SYSCLK_DDRCLK_B0_UF
DDR_MCLK_3_N	W33	SYSCLK_DDRCLK_B0_L_UF
DDR_MCLK_4_P	V33	SYSCLK_DDRCLK_B1_UF
DDR_MCLK_4_N	V32	SYSCLK_DDRCLK_B1_L_UF
DDR_MCLK_5_P	W35	INT_DDRCLK5_P_TP
DDR_MCLK_5_N	W36	INT_DDRCLK5_N_TP
DDR_REF	AA22	INT_MEM_REF_H
DDR_VREF_0	Y22	INT_MEM_VREF
DDR_VREF_1	T22	

'0' & '1' GO TO SLOT A
'2' & '3' GO TO SLOT B

'0' & '1' GO TO SLOT A
'2' & '3' GO TO SLOT B

'0'S ARE SAME POLARITY (ACTIVE-LO)
'1'S ARE SAME POLARITY (ACTIVE-HI)

R199 1K 1% 1/16W MF 402

MEM_VREF

+2_5V_INTREPID

R198 10K 1% 1/16W MF 402
R191 10K 1% 1/16W MF 402
C245 0.1UF 20% 10V CERM 402
INT_MEM_VREF

CLOCKS

SYSCLK_DDRCLK_A1_UF	RP33 22	SYSCLK_DDRCLK_A1	11 36
SYSCLK_DDRCLK_A1_L_UF	RP33 22	SYSCLK_DDRCLK_A1_L	11 36
SYSCLK_DDRCLK_A0_UF	RP34 22	SYSCLK_DDRCLK_A0	11 36
SYSCLK_DDRCLK_A0_L_UF	RP34 22	SYSCLK_DDRCLK_A0_L	11 36
SYSCLK_DDRCLK_B1_UF	RP33 22	SYSCLK_DDRCLK_B1	11 36
SYSCLK_DDRCLK_B1_L_UF	RP33 22	SYSCLK_DDRCLK_B1_L	11 36
SYSCLK_DDRCLK_B0_UF	RP34 22	SYSCLK_DDRCLK_B0	11 36
SYSCLK_DDRCLK_B0_L_UF	RP34 22	SYSCLK_DDRCLK_B0_L	11 36

CS

MEM_CS_L<0>	RP36 22	RAM_CS_L<0>	11 36
MEM_CS_L<1>	RP36 22	RAM_CS_L<1>	11 36
MEM_CS_L<2>	RP35 22	RAM_CS_L<2>	11 36
MEM_CS_L<3>	RP35 22	RAM_CS_L<3>	11 36

CKE

MEM_CKE<0>	RP36 22	RAM_CKE<0>	9 11 36
MEM_CKE<1>	RP36 22	RAM_CKE<1>	9 11 36
MEM_CKE<2>	RP35 22	RAM_CKE<2>	9 11 36
MEM_CKE<3>	RP35 22	RAM_CKE<3>	9 11 36

ADDR

MEM_ADDR<0>	RP31 22	RAM_ADDR<0>	11 36
MEM_ADDR<1>	RP25 22	RAM_ADDR<1>	11 36
MEM_ADDR<2>	RP25 22	RAM_ADDR<2>	11 36
MEM_ADDR<3>	RP25 22	RAM_ADDR<3>	11 36
MEM_ADDR<4>	RP30 22	RAM_ADDR<4>	11 36
MEM_ADDR<5>	RP30 22	RAM_ADDR<5>	11 36
MEM_ADDR<6>	RP31 22	RAM_ADDR<6>	11 36
MEM_ADDR<7>	RP30 22	RAM_ADDR<7>	11 36
MEM_ADDR<8>	RP31 22	RAM_ADDR<8>	11 36
MEM_ADDR<9>	RP31 22	RAM_ADDR<9>	11 36
MEM_ADDR<10>	RP26 22	RAM_ADDR<10>	11 36
MEM_ADDR<11>	RP30 22	RAM_ADDR<11>	11 36
MEM_ADDR<12>	RP26 22	RAM_ADDR<12>	11 36

BA

MEM_BA<0>	RP26 22	RAM_BA<0>	11 36
MEM_BA<1>	RP26 22	RAM_BA<1>	11 36

CNTL

MEM_WE_L	RP26 22	RAM_WE_L	11 36
MEM_CAS_L	R250 22	RAM_CAS_L	11 36
MEM_RAS_L	R238 22	RAM_RAS_L	11 36

1MB BOOT ROM

+3V_MAIN

C460 2.2UF 20% 10V CERM 805
C470 0.1UF 20% 10V CERM 402
C479 0.1UF 20% 10V CERM 402

U17
FEPR-1MX8
3.3V
TSOP
OMIT

A0	21	DQ0	25
A1	20	DQ1	26
A2	19	DQ2	27
A3	18	DQ3	28
A4	17	DQ4	32
A5	16	DQ5	33
A6	15	DQ6	34
A7	14	DQ7	35
A8	8		
A9	7		
A10	36		
A11	6		
A12	5		
A13	4		
A14	3		
A15	2		
A16	1		
A17	40		
A18	13		
A19	37		
A20	38		
CE	22		
OE	24		
WE	9		
WP	12		
PWD	10		
VPP	11		
VCC	30		
GND	23, 39		

PCI_AD<0> … PCI_AD<31>
ROM_ONBOARD_CS_L
ROM_OE_L
ROM_RW_L
ROM_WP_L
INT_RESET_L

+3V_MAIN

R338 10K 5% 1/16W MF 402
R386 10K 5% 1/16W MF 402
R357 1K 5% 1/16W MF 402
ROM_CS_L

OVERRIDE ROM MODULE
INTERCEPTS ROM CHIP SELECT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1255	1	BOOTROM,P84	U17	CRITICAL	?

PULL-DOWN RESISTORS TO ENSURE
CKE STAYS LOW AFTER INTREPID
2.5V I/O SHUTS OFF

RAM_CKE<0>
RAM_CKE<1>
RAM_CKE<2>
RAM_CKE<3>

R500 10K 5% 1/16W MF 402
R439 10K 5% 1/16W MF 402
R409 10K 5% 1/16W MF 402
R387 10K 5% 1/16W MF 402

INT - DDR/BOOTROM

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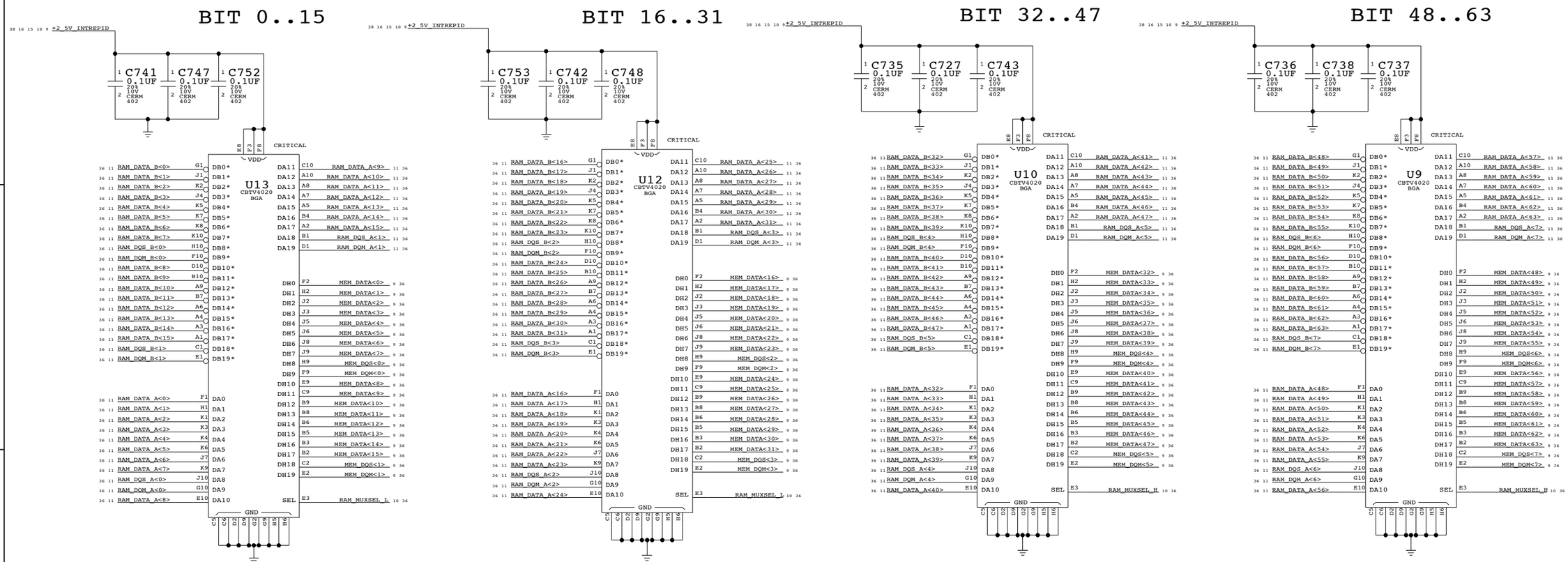
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6459	A
SCALE: NONE	SHT 9 OF 44	



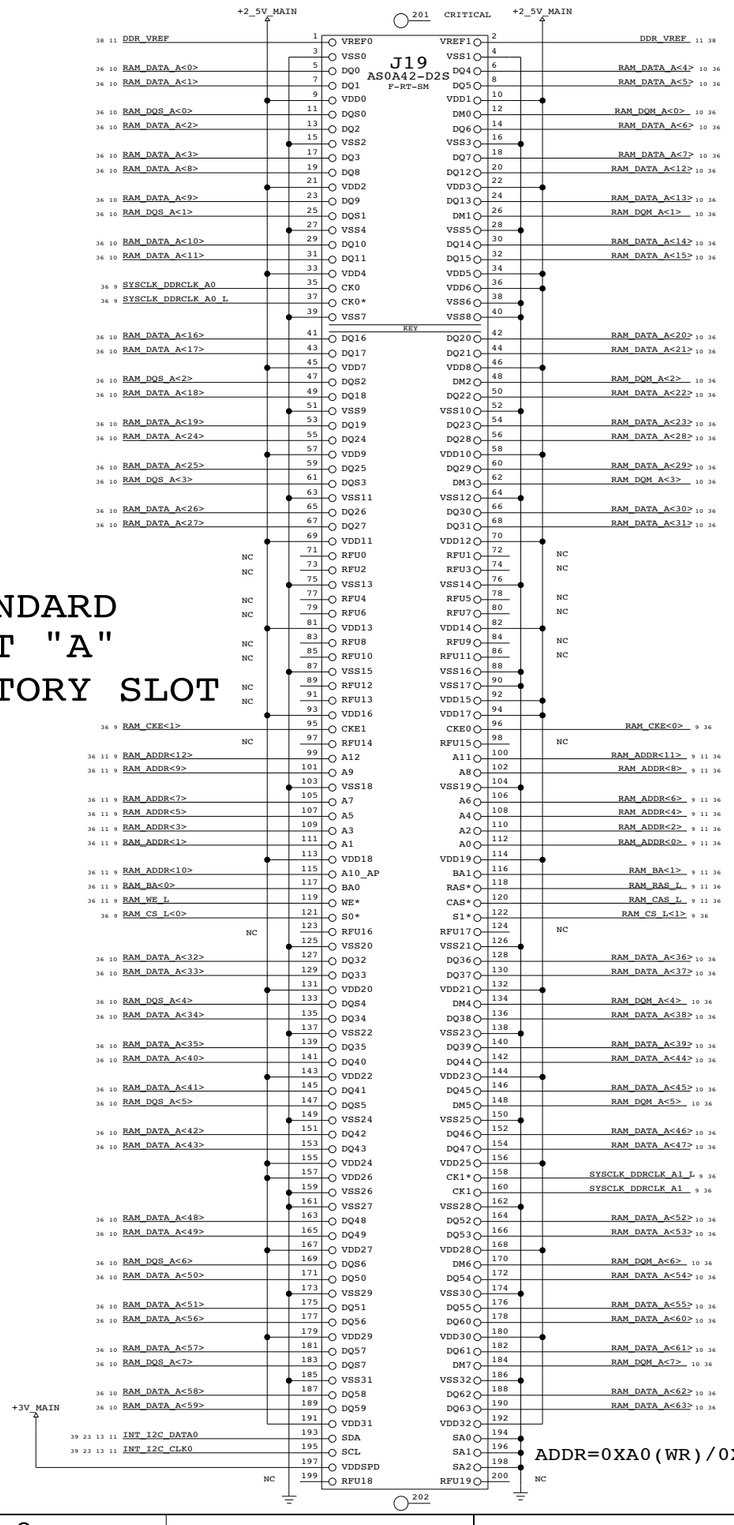
SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND
MEM_MUXSEL_H<0> AND MEM_MUXSEL_L<0> ARE ACTIVE LOW
MEM_MUXSEL_H<1> AND MEM_MUXSEL_L<1> ARE ACTIVE HIGH

ADDED 0 OHM RESISTORS IN CASE POLARITY IS WRONG

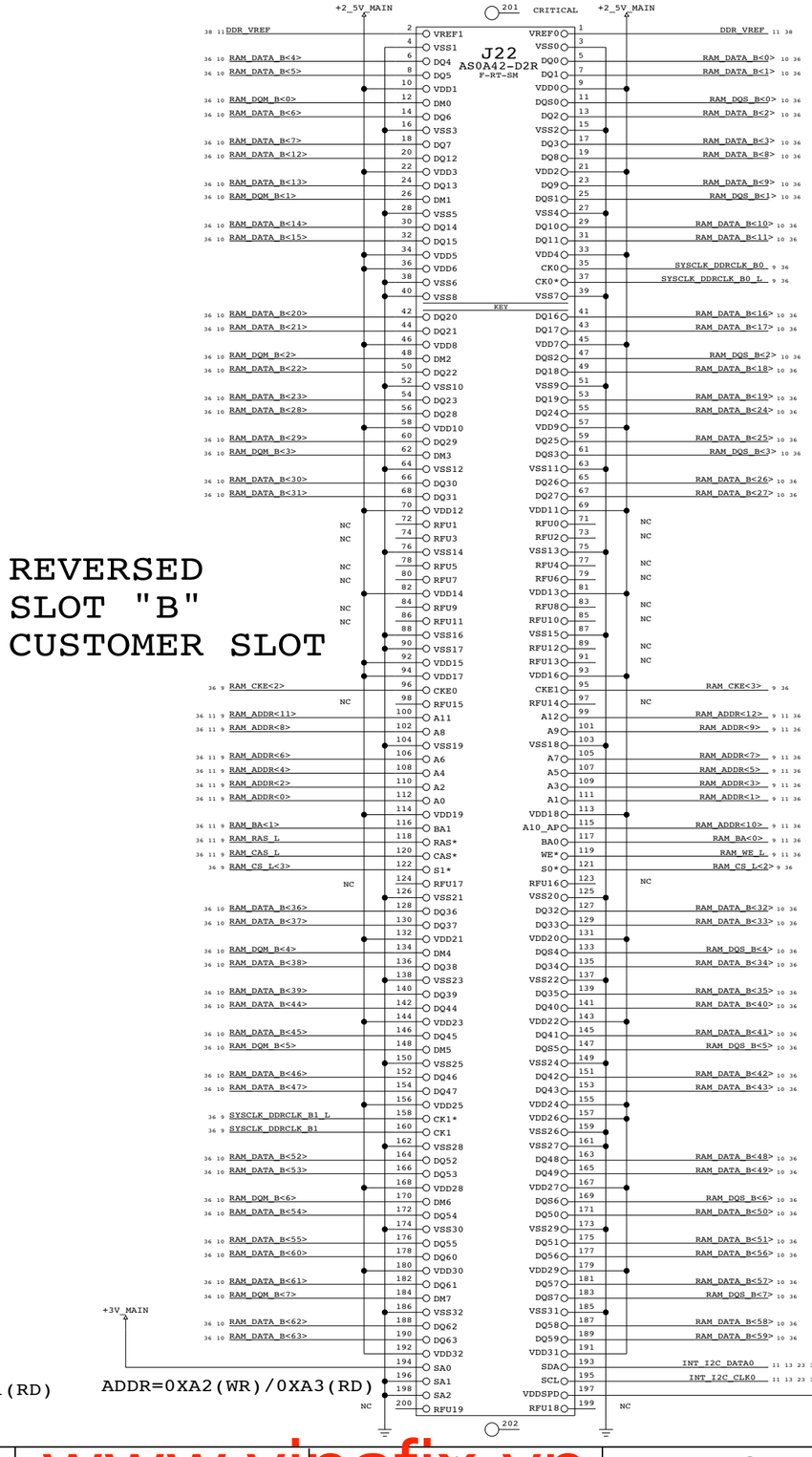
16BIT 2:1 DDR MUXES

APPLE COMPUTER INC.

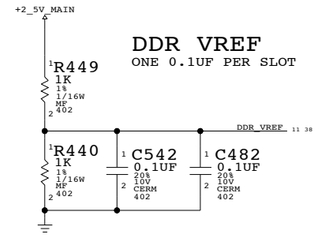
SIZE	DRAWING NUMBER	REV.
D	051-6459	A
SCALE: NONE	SHT 10 OF 44	

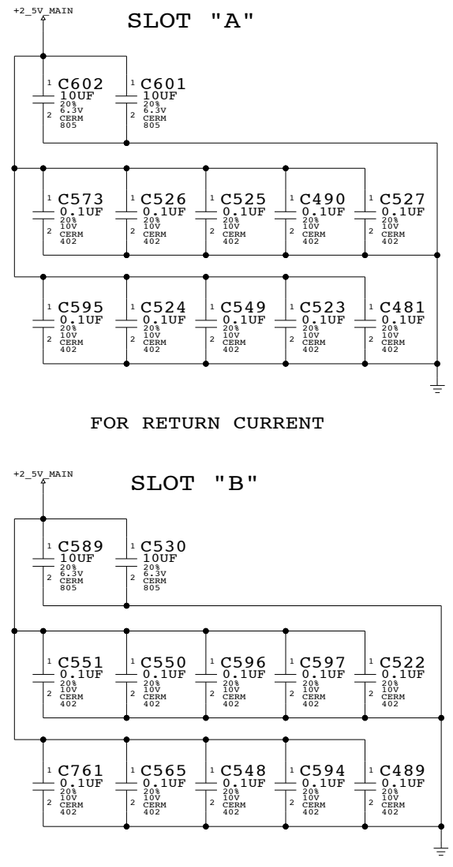


STANDARD
SLOT "A"
FACTORY SLOT



REVERSED
SLOT "B"
CUSTOMER SLOT





DDR SODIMM CONNS

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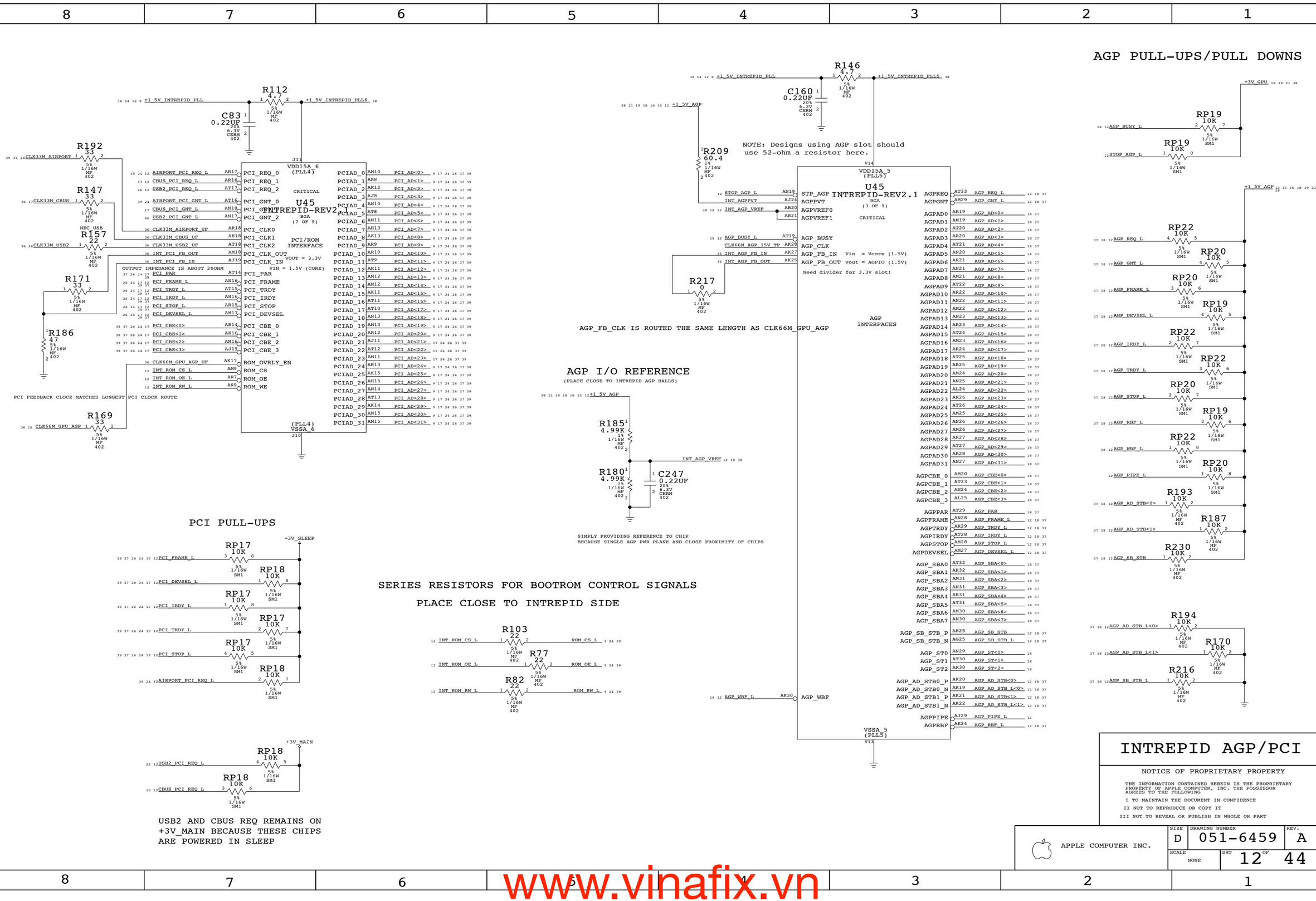
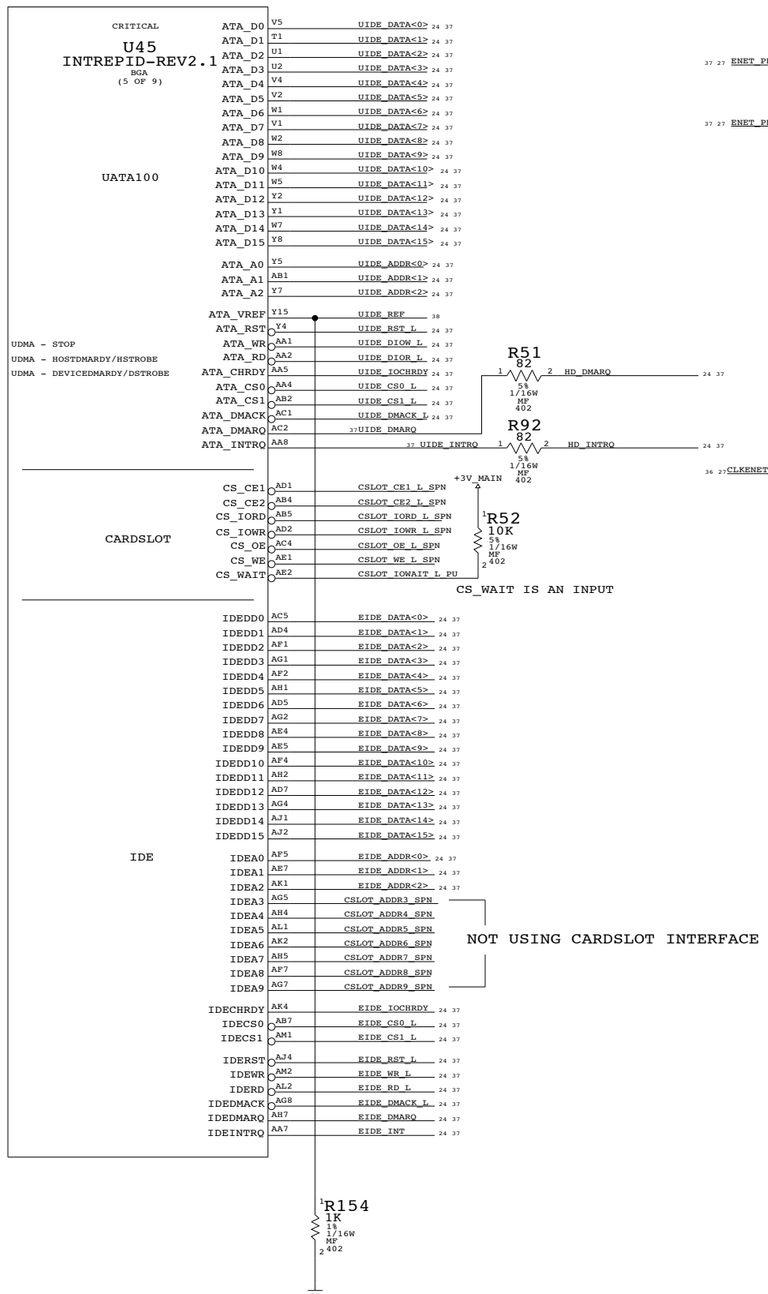
APPLE COMPUTER INC.

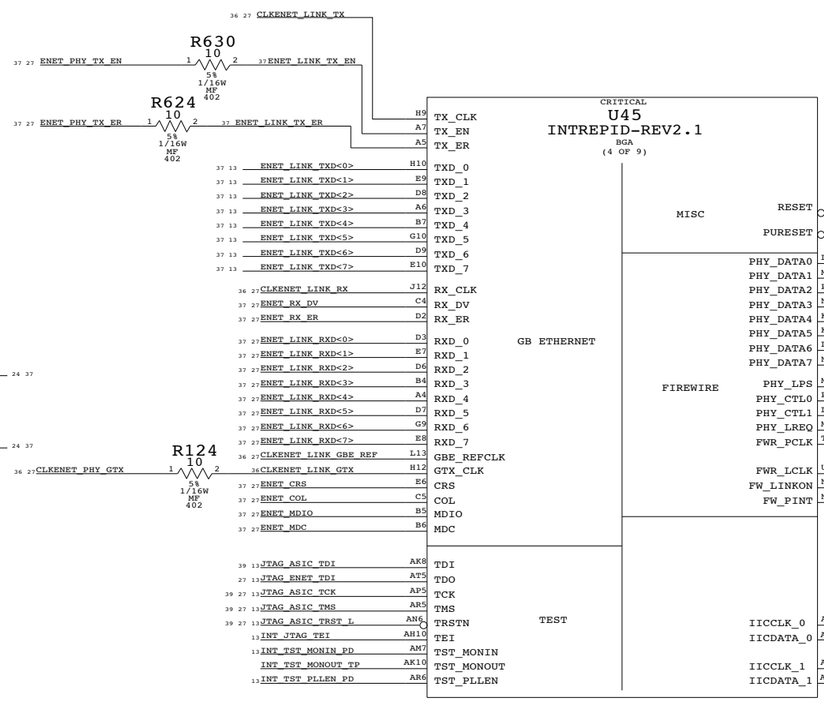
SIZE	DRAWING NUMBER	REV.
D	051-6459	A

SCALE NONE

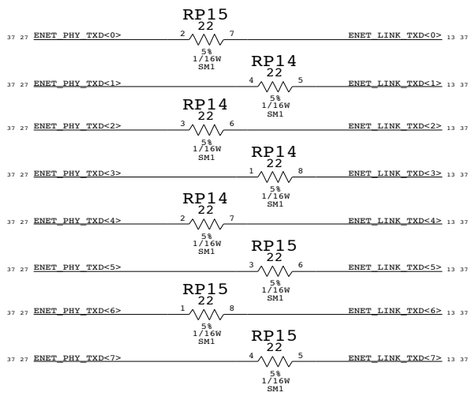
SHT 11 OF 44





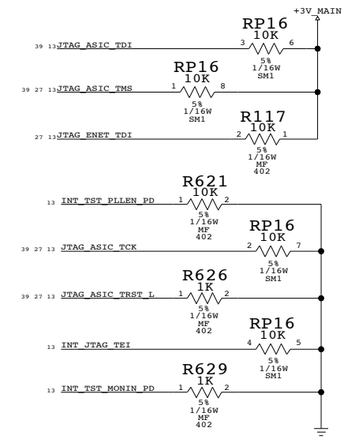


ENET_TXD SERIES TERMINATION

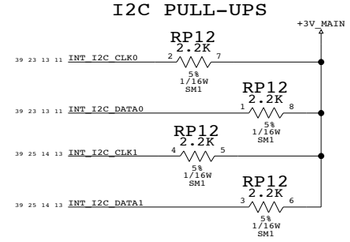


JTG_RSTN_L	TST_TEI_H	JTG_TDO_H (I/O)	JTG_TDI_H (I/O)	TST_PLLEN_H	ANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	EXTPLL SHUTDOWN (OUTPUT)	DDR_ TPDENABLE (OUTPUT)	0	(OUTPUT)	NORMAL OPERATION
0	0	(OUTPUT)	0(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	HWPLL_ TESTSEL5 (INPUT)	1(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0(I)	0(I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0(I)	1(I)	0	X(I)	ATPG IDDQ
0	1	0(I)	1(I)	1	X(I)	TEST TRI-STATE
0	1	1(I)	0(I)	0	X(I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1(I)	0(I)	1	X(I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1(I)	1(I)	X	X(I)	FUNCTIONAL TEST IDDQ

TEST PULL-UPS/DOWNS



I2C PULL-UPS

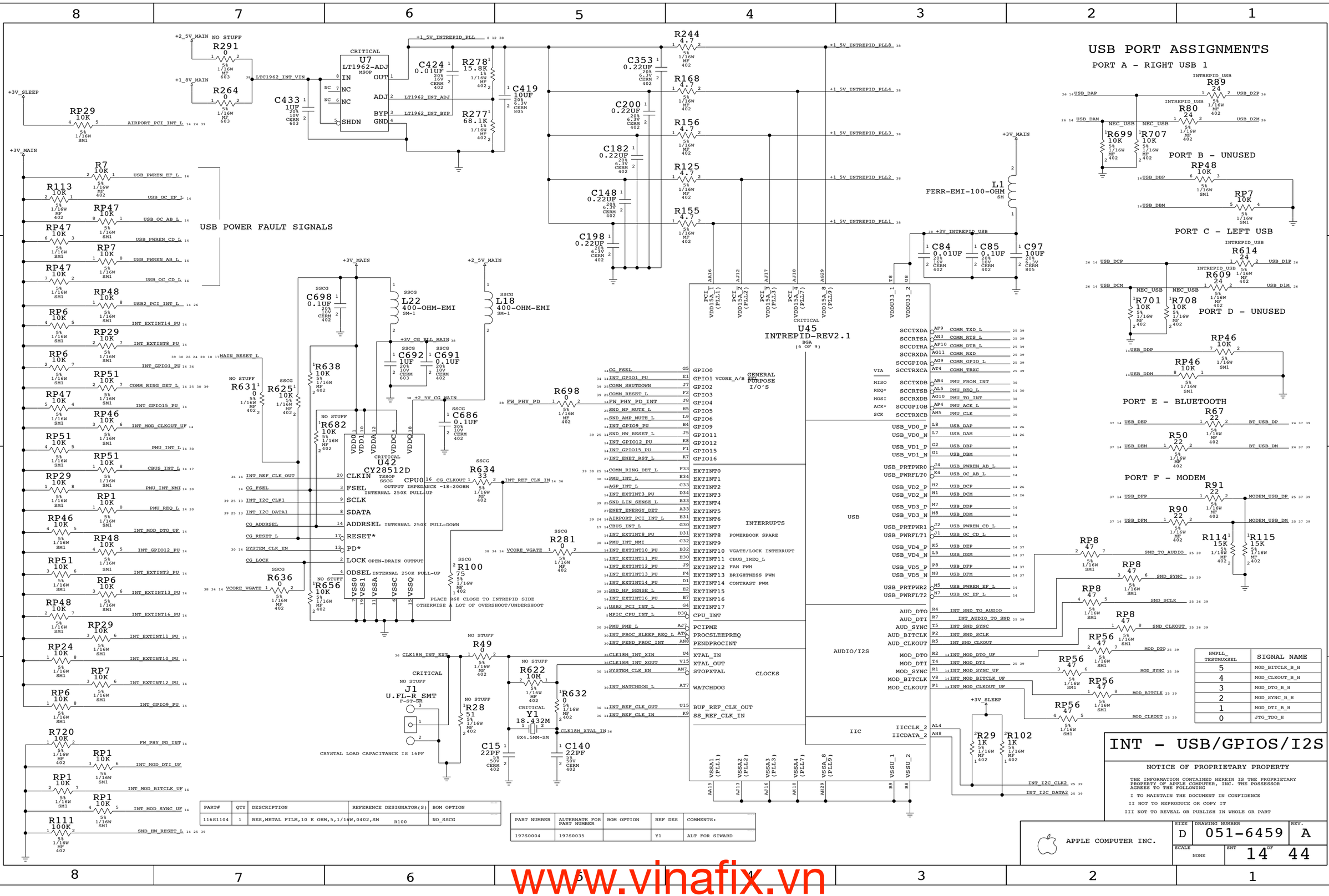


BUS / ADDR	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
A0-WR A1-RD	RAM - STANDARD J20 - PG 12	N/A	N/A	N/A
A2-WR A3-RD	RAM - REVERSED J23 - PG 12	N/A	N/A	N/A
AC-WR AD-RD	N/A	N/A	DASH MODEM J9 - PG 25	N/A
AE-WR AF-RD	BOOTBANG E2PROM U37 - PG 23	N/A	N/A	N/A
84-WR 85-RD	LMU U36 - PG 23	N/A	N/A	N/A
58-WR 59-RD	N/A	FAN CONTROLLER U3 - PG 24	N/A	N/A
6A-WR 6B-RD	N/A	N/A	SNAPPER SOUND J12 - PG 24	N/A
D0-WR D1-RD	N/A	CLOCK SLEW SSCG U56 - PG 15	N/A	N/A

ADDR LSB INDICATES READ ('1') OR WRITE ('0') MODES

INT - ENET/FW/UATA EIDE/I2C

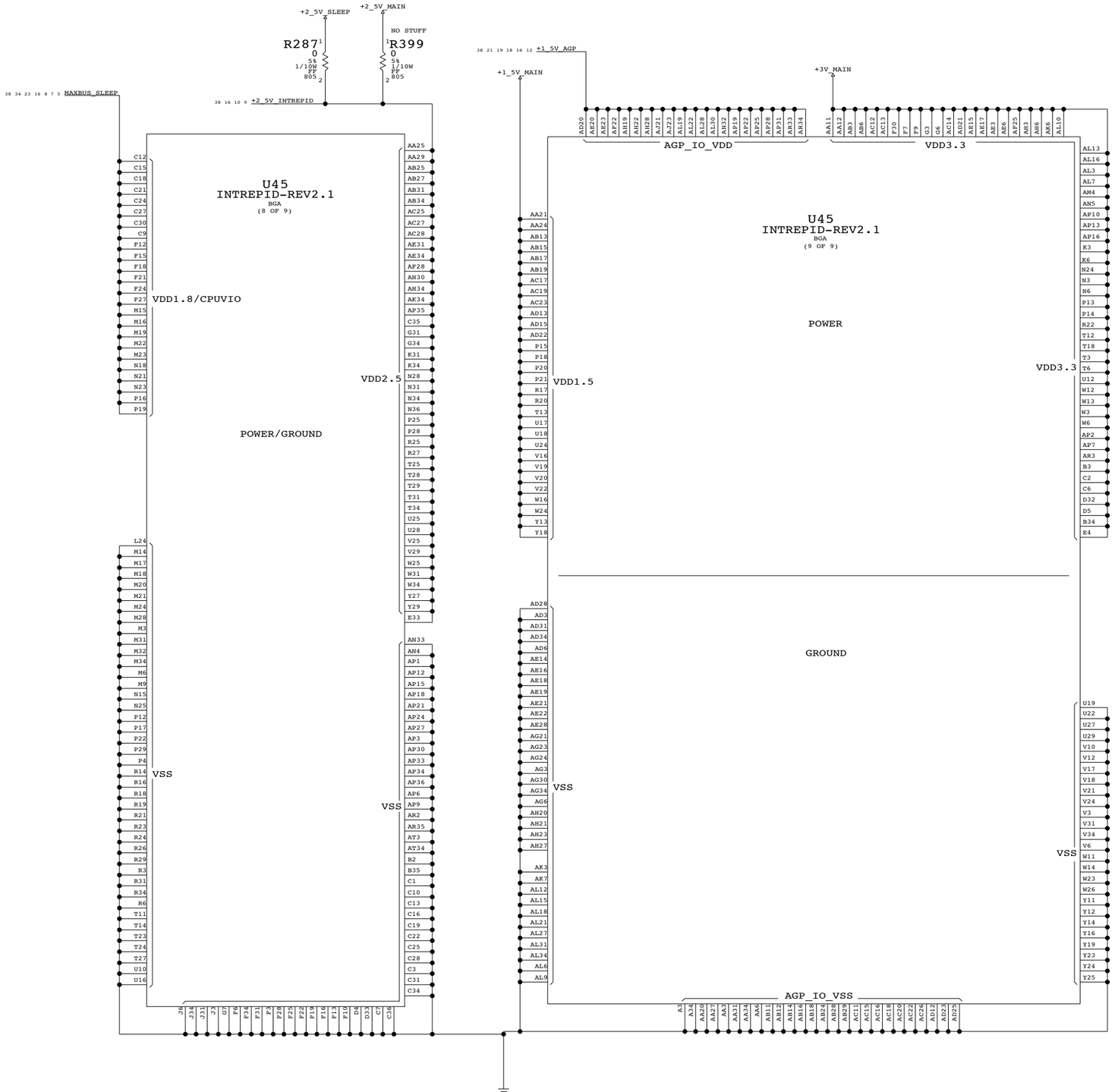
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6459
REV. A
SCALE NONE
SHT 13 OF 44



HWPLL_TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES,METAL FILM,10 K OHM,5,1/16W,0402,SM	R100	NO_SSCG

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0004	197S0035		Y1	ALT FOR SIWARD



Intrepid Power

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6459	A
SCALE: NONE	SHT 15 OF 44	

INTREPID MAXBUS DECOUPLING

38 34 23 15 8 7 5 MAXBUS_SLEEP

24 Balls
4 X 10UF (0805)
32 X 0.22UF (0402)

C204 10uF 20% 6.3V CERM 805 · C348 10uF 20% 6.3V CERM 805 · C236 10uF 20% 6.3V CERM 805 · C196 10uF 20% 6.3V CERM 805

C239 C240 C350 C312 C176 C288 C313 C94 C286 C158 — 0.22uF 20% 6.3V CERM 402

C174 C206 C259 C237 C238 C95 C117 C241 C260 C314 — 0.22uF 20% 6.3V CERM 402

C173 C171 C175 C226 C172 C207 C118 C287 C119 C349 — 0.22uF 20% 6.3V CERM 402

C205 C209 — 0.22uF 20% 6.3V CERM 402

INTREPID AGP I/O DECOUPLING

38 21 19 18 15 12 +1_5V_AGP

21 Balls
4 X 10UF (0805)
24 X 0.22UF (0402)

C371 10uF 20% 6.3V CERM 805 · C231 10uF 20% 6.3V CERM 805 · C281 10uF 20% 6.3V CERM 805 · C394 10uF 20% 6.3V CERM 805

C356 C297 C268 C217 C355 C267 C250 C298 C377 C216 — 0.22uF 20% 6.3V CERM 402

C228 C230 C265 C378 C357 C229 C325 C393 C324 C323 — 0.22uF 20% 6.3V CERM 402

C251 C266 C249 — 0.22uF 20% 6.3V CERM 402

INTREPID DDR DECOUPLING

38 15 10 9 +2_5V_INTREPID

44 Balls
4 X 10UF (0805)
51 X 0.22UF (0402)

C422 10uF 20% 6.3V CERM 805 · C417 10uF 20% 6.3V CERM 805 · C418 10uF 20% 6.3V CERM 805 · C423 10uF 20% 6.3V CERM 805

C407 C391 C310 C317 C480 C390 C370 C320 C365 C366 — 0.22uF 20% 6.3V CERM 402

C367 C292 C295 C403 C291 C352 C322 C392 C385 C376 — 0.22uF 20% 6.3V CERM 402

C321 C318 C399 C410 C335 C369 C384 C294 C406 C405 — 0.22uF 20% 6.3V CERM 402

C404 C400 C386 C289 C387 C401 C354 C389 C309 C398 — 0.22uF 20% 6.3V CERM 402

C337 C290 C402 C397 C368 C334 C388 C293 C319 C336 — 0.22uF 20% 6.3V CERM 402

C316 — 0.22uF 20% 6.3V CERM 402

INTREPID CORE DECOUPLING

+1_5V_MAIN

30 Balls
4 X 10UF (0805)
29 X 0.22UF (0402)

C128 10uF 20% 6.3V CERM 805 · C101 10uF 20% 6.3V CERM 805 · C157 10uF 20% 6.3V CERM 805 · C315 10uF 20% 6.3V CERM 805

C147 C243 C262 C242 C227 C181 C142 C215 C278 C264 — 0.22uF 20% 6.3V CERM 402

C244 C212 C178 C179 C177 C159 C161 C162 C280 C279 — 0.22uF 20% 6.3V CERM 402

C144 C246 C211 C263 C180 C213 C197 C208 C214 — 0.22uF 20% 6.3V CERM 402

INTREPID 3.3V DECOUPLING

+3V_MAIN

57 Balls
4 X 10UF (0805)
72 X 0.22UF (0402)

C164 10uF 20% 6.3V CERM 805 · C395 10uF 20% 6.3V CERM 805 · C10 10uF 20% 6.3V CERM 805 · C9 10uF 20% 6.3V CERM 805

C375 C351 C53 C42 C21 C185 C31 C143 C123 C121 — 0.22uF 20% 6.3V CERM 402

C33 C184 C43 C35 C261 C60 C52 C199 C57 C19 — 0.22uF 20% 6.3V CERM 402

C16 C108 C55 C32 C125 C45 C76 C277 C28 C26 — 0.22uF 20% 6.3V CERM 402

C34 C23 C120 C146 C141 C30 C145 C96 C54 C50 — 0.22uF 20% 6.3V CERM 402

C75 C122 C51 C59 C163 C126 C98 C109 C56 C27 — 0.22uF 20% 6.3V CERM 402

C296 C248 C210 C58 C22 C20 C61 C44 C29 C24 — 0.22uF 20% 6.3V CERM 402

C183 C18 C49 C36 C17 C99 C396 C124 C127 C100 — 0.22uF 20% 6.3V CERM 402

Intrepid Decoupling

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6459	A

SCALE	SHT	OF
NONE	16	44

PCI1510 PULL-UPS

+3V_MAIN

R757 10K 5% 1/16W MF 402 — CBUS_PCI_PERR_L 17

R756 10K 5% 1/16W MF 402 — CBUS_PCI_SERR_L 17

R753 10K 5% 1/16W MF 402 — CBUS_SUSPEND_PU 17

+3V_MAIN

C813 10UF 20% 6.3V CERM 805
C795 0.22UF 20% 6.3V CERM 402
C798 0.22UF 20% 6.3V CERM 402
C790 0.22UF 20% 6.3V CERM 402
C796 0.22UF 20% 6.3V CERM 402
C797 0.22UF 20% 6.3V CERM 402
C791 0.22UF 20% 6.3V CERM 402

R762 10K 5% 1/16W MF 402

+2_5V_MAIN

C789 0.22UF 20% 6.3V CERM 402

A7 C13 D5 E1 M1 N7 N11 — VCC

39 30 26 24 20 18 17 14 MAIN_RESET_L

THIS PROPERLY SHUTS DOWN
CARDBUS POWER FOR PSUEDO-D3COLD

R348 47 5% 1/16W MF 402

+3V_MAIN

+5V_MAIN

NO STUFF
R373 10K 5% 1/16W MF 402

U19
TPS2211 SSOI

NC	9		
V_12	5	AVPP	10
V_5_1	6		
V_5_2	3	AVCC0	11
V_3_1	4	AVCC1	12
V_3_2		AVCC2	13
VCCD0	1		
VCCD1	2		
VPPD0	15	CRITICAL	
VPPD1	14		
SHTDWN	16		
GND	7	OC	8 NC

TPS2211_SHDN_L_PU

+VPP_CBUS_SW 17 38

+VCC_CBUS_SW 17 38

C773 0.1UF 20% 10V CERM 402
C467 0.1UF 20% 10V CERM 402

MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES
TO MINIMIZE INDUCTANCE!

0.1UF ARE USED TO INCREASE ESD DISCHARGES OF UP TO 10KV

CRITICAL
U26
PCI1510GGU
BGA

CLAMP FOR PC-CARD
CLAMP FOR PCI

NC	H10	CLK_48_RSVD/NC	
PCI1510_VR_EN_L	D4	VR_EN*	
	L8	VR_PORT	
PCI_AD<0>	N8	AD0	
PCI_AD<1>	M7	AD1	
PCI_AD<2>	L7	AD2	
PCI_AD<3>	N6	AD3	
PCI_AD<4>	K4	AD4	
PCI_AD<5>	M6	AD5	
PCI_AD<6>	L6	AD6	
PCI_AD<7>	N5	AD7	
PCI_AD<8>	N4	AD8	
PCI_AD<9>	M2	AD9	
PCI_AD<10>	M5	AD10	
PCI_AD<11>	L4	AD11	
PCI_AD<12>	N3	AD12	
PCI_AD<13>	K5	AD13	
PCI_AD<14>	L5	AD14	
PCI_AD<15>	M4	AD15	
PCI_AD<16>	J4	AD16	
PCI_AD<17>	H1	AD17	
	H3	AD18	
PCI_AD<19>	H2	AD19	
PCI_AD<20>	G2	AD20	
PCI_AD<21>	G4	AD21	
PCI_AD<22>	F1	AD22	
PCI_AD<23>	C3	AD23	
PCI_AD<24>	F3	AD24	
PCI_AD<25>	E2	AD25	
PCI_AD<26>	F4	AD26	
PCI_AD<27>	B1	AD27	
PCI_AD<28>	D2	AD28	
PCI_AD<29>	E4	AD29	
PCI_AD<30>	D3	AD30	
PCI_AD<31>	E3	AD31	
PCI_CBE<0>	K6	C/BE0*	
PCI_CBE<1>	M3	C/BE1*	
PCI_CBE<2>	J2	C/BE2*	
PCI_CBE<3>	A1	C/BE3*	
PCI_PAR	N1	PAR	
PCI_IRDY_L	K1	IRDY	
CBUS_PCI_SERR_L	L2	SERR	
CBUS_PCI_IDSEL	F2	IDSEL	
CBUS_PCI_PERR_L	K3	PERR	
PCI_FRAME_L	J1	FRAME	
PCI_STOP_L	L1	STOP	
PCI_TRDY_L	J3	TRDY	
PCI_DEVSEL_L	K2	DEVSEL	
IO_RESET_L	G3	PRST	
CBUS_PCI_REQ_L	C2	REQ	
CBUS_PCI_GNT_L	C1	GNT	
CLK33M_CBUS	G1	PCLK	
	M9	SPKROUT	
	M8	RI_OUT/PME	
CBUS_SUSPEND_PU	N10	SUSPEND	
CBUS_INT_L	K7	MFUNC0	
CBUS_MFUNC1_PD	N9	MFUNC1	
CBUS_MFUNC2_PD	L9	MFUNC2	
CBUS_MFUNC3_PD	K10	MFUNC3	
CBUS_MFUNC4_PD	M10	MFUNC4	
CBUS_MFUNC5_PD	N12	MFUNC5	
CBUS_MFUNC6_PD	L10	MFUNC6	
	L11	GRST	
	B11	VCCCB	
	L3	VCCP	
CBUS_VCCD0_L	N13	VCCD0*	
CBUS_VCCD1_L	L12	VCCD1*	
CBUS_VPPD0	K9	VPPD0	
CBUS_VPPD1	M11	VPPD1	
CBUS_DET_1_L	L13	CD1*/CCD1*	
CBUS_DET_2_L	B5	CD2*/CCD2*	
CBUS_IORD_L	F12	IORD*/CAD13	
CBUS_IOWR_L	C11	IOWR*/CAD15	
CBUS_OE_L	G10	OE*/CAD11	
CBUS_CE1_L	H13	CE1*/CC/BE0*	
CBUS_VS1	B2	VS1*/CVS1	
CBUS_VS2	A9	VS2*/CVS2	
CBUS_WE_L	D13	WE*/CGNT*	
CBUS_READY	A6	RDY/IREQ*/CINT*	
CBUS_RESET_L	D8	RESET/CRST*	
CBUS_REG_L	A8	REG*/CC/BE3*	
CBUS_BVD1_L	C6	BVD1/CSTSCHG/STSCHG*/RI*	
CBUS_BVD2_L	D6	BVD2/SPKR*/CAUDIO	
CBUS_WP_L	A5	WP/IOIS16*/CCLKRUN*	
CBUS_CE2_L	G13	CE2/CAD10*	
CBUS_INPACK_L	B8	INPACK/CREQ*	
CBUS_WAIT_L	B6	WAIT/CSERR*	
CBUS_ADDR<0>	C7	A0/CAD26	
CBUS_ADDR<1>	D7	A1/CAD25	
CBUS_ADDR<2>	B7	A2/CAD24	
CBUS_ADDR<3>	D10	A3/CAD23	
CBUS_ADDR<4>	B12	A4/CAD22	
CBUS_ADDR<5>	C8	A5/CAD21	
CBUS_ADDR<6>	C9	A6/CAD20	
CBUS_ADDR<7>	A12	A7/CAD18	
CBUS_ADDR<8>	E11	A8/CC/BE1*	
CBUS_ADDR<9>	F11	A9/CAD14	
CBUS_ADDR<10>	G11	A10/CAD9	
CBUS_ADDR<11>	G12	A11/CAD12	
CBUS_ADDR<12>	D9	A12/CC/BE2*	
CBUS_ADDR<13>	E12	A13/CPAR	
CBUS_ADDR<14>	D12	A14/CPERR*	
CBUS_ADDR<15>	C10	A15/CIRDY*	
CBUS_ADDR_16_UF	B13	A16/CCLK	
CBUS_ADDR<17>	F10	A17/CAD16	
CBUS_ADDR<18>	E13	A18/RSVD	
CBUS_ADDR<19>	A13	A19/CBLOCK*	
CBUS_ADDR<20>	E10	A20/CSTOP*	
CBUS_ADDR<21>	D11	A21/CDEVSEL*	
CBUS_ADDR<22>	C12	A22/CTRDY*	
CBUS_ADDR<23>	A10	A23/CFRAME*	
CBUS_ADDR<24>	B10	A24/CAD17	
CBUS_ADDR<25>	B9	A25/CAD19	
CBUS_DATA<0>	A4	D0/CAD27	
CBUS_DATA<1>	C4	D1/CAD29	
CBUS_DATA<2>	A3	D2/RSVD	
CBUS_DATA<3>	K11	D3/CAD0	
CBUS_DATA<4>	K12	D4/CAD1	
CBUS_DATA<5>	J13	D5/CAD3	
CBUS_DATA<6>	J10	D6/CAD5	
CBUS_DATA<7>	H12	D7/CAD7	
CBUS_DATA<8>	C5	D8/CAD28	
CBUS_DATA<9>	B4	D9/CAD30	
CBUS_DATA<10>	B3	D10/CAD31	
CBUS_DATA<11>	M12	D11/CAD2	
CBUS_DATA<12>	J11	D12/CAD4	
CBUS_DATA<13>	K13	D13/CAD6	
CBUS_DATA<14>	J12	D14/RSVD	
CBUS_DATA<15>	H11	D15/CAD8	

INTEGRATED PULL-UP

R767 22 5% 1/16W MF 402

NO STUFF
R764 47 5% 1/16W MF 402

R766 47 5% 1/16W MF 402

39 30 26 24 20 18 17 14 MAIN_RESET_L

RP39 10K 5% 1/32W 25V SM

CBUS_MFUNC1_PD 17
CBUS_MFUNC2_PD 17
CBUS_MFUNC3_PD 17
CBUS_MFUNC4_PD 17
CBUS_MFUNC5_PD 17
CBUS_MFUNC6_PD 17

GND

A2 A11 D1 F13 H4 K8 M13 N2

R750 47 5% 1/16W MF 402 — CBUS_ADDR<16> 17

TI REFERENCE SCHEMATIC DID NOT HAVE BULK ON +VCC_CBUS_SW

C783 2.2UF 20% 10V CERM 805
C776 2.2UF 20% 10V CERM 805

38 17 +VCC_CBUS_SW

PC CARD/CARDBUS CONNECTOR

CRITICAL
J9
QT500806-L111
M-ST-SM1

		84	81		
		2	1	CBUS_DATA<3>	17
39 17 CBUS_DET_1_L		4	3	CBUS_DATA<4>	17
17 CBUS_DATA<11>		6	5	CBUS_DATA<5>	17
17 CBUS_DATA<12>		8	7	CBUS_DATA<6>	17
17 CBUS_DATA<13>		10	9		
		12	11	CBUS_DATA<7>	17
17 CBUS_DATA<14>		14	13	CBUS_CE1_L	17
17 CBUS_DATA<15>		16	15	CBUS_ADDR<10>	17
17 CBUS_CE2_L		18	17	CBUS_OE_L	17
17 CBUS_VS1		20	19		
		22	21	CBUS_ADDR<11>	17
17 CBUS_IORD_L		24	23	CBUS_ADDR<9>	17
17 CBUS_IOWR_L		26	25	CBUS_ADDR<8>	17
17 CBUS_ADDR<17>		28	27	CBUS_ADDR<13>	17
17 CBUS_ADDR<18>		30	29		
		32	31	CBUS_ADDR<14>	17
17 CBUS_ADDR<19>		34	33	CBUS_WE_L	17
17 CBUS_ADDR<20>		36	35	CBUS_READY	17
17 CBUS_ADDR<21>		38	37	+VCC_CBUS_SW	17 38
38 17 +VCC_CBUS_SW		40	39		
		42	41	+VPP_CBUS_SW	17 38
38 17 +VPP_CBUS_SW		44	43	CBUS_ADDR<16>	17
17 CBUS_ADDR<22>		46	45	CBUS_ADDR<15>	17
17 CBUS_ADDR<23>		48	47	CBUS_ADDR<12>	17
17 CBUS_ADDR<24>		50	49		
		52	51	CBUS_ADDR<7>	17
17 CBUS_ADDR<25>		54	53	CBUS_ADDR<6>	17
17 CBUS_VS2		56	55	CBUS_ADDR<5>	17
17 CBUS_RESET_L		58	57	CBUS_ADDR<4>	17
17 CBUS_WAIT_L		60	59		
		62	61	CBUS_ADDR<3>	17
17 CBUS_INPACK_L		64	63	CBUS_ADDR<2>	17
17 CBUS_REG_L		66	65	CBUS_ADDR<1>	17
17 CBUS_BVD2_L		68	67	CBUS_ADDR<0>	17
17 CBUS_BVD1_L		70	69		
		72	71	CBUS_DATA<0>	17
17 CBUS_DATA<8>		74	73	CBUS_DATA<1>	17
17 CBUS_DATA<9>		76	75	CBUS_DATA<2>	17
17 CBUS_DATA<10>		78	77	CBUS_WP_L	17
39 17 CBUS_DET_2_L		80	79		
		83	82		

CARDBUS

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6459	A
SCALE: NONE	SHT 17 OF 44	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0133	1	IC,ATI,M10,NO HEATSPREADER	U44	CRITICAL	?

OMIT
CRITICAL

U44
RAGE MOBILITY
M10-CSP64
64MB
BGA
(1 OF 6)

AD_STB0 N29 AGP_AD_STB<0>
AD_STB1 W29 AGP_AD_STB<1>
AD_STBB0 M28 AGP_AD_STB_L<0>
AD_STBB1 Y29 AGP_AD_STB_L<1>
AGP_BUSYB AG28 AGP_BUSY_L
AGPREF K30
AGPTEST K29 GPU_AGP_TEST
AGP8X_DETB U25 AGP8X_DET_PU
SUS_STAT AJ28 AGP_SUS_STAT_L_PU
ST0 AF30 AGP_ST<0>
ST1 AF28 AGP_ST<1>
ST2 AE29 AGP_ST<2>
SBA7 AC28 AGP_SBA<7>
SBA6 AB29 AGP_SBA<6>
SBA5 AC27 AGP_SBA<5>
SBA4 AC30 AGP_SBA<4>
SBA3 AD27 AGP_SBA<3>
SBA2 AD30 AGP_SBA<2>
SBA1 AE28 AGP_SBA<1>
SBA0 AD29 AGP_SBA<0>
RBFB AE30 AGP_RBF_L
STP_AGPB AG29 AGP_STP_L
SB_STB AC29 AGP_SB_STB
SB_STBS AD28 AGP_SB_STB_L
RSTB_MSK AD24 ATI_RSTB_MSK
DBI_LO Y25 ATI_DBI_LO_PU
DBI_HI Y27 ATI_DBI_HI_PU

AD31 AB30 AGP_AD<31>
AD30 AB27 AGP_AD<30>
AD29 AA29 AGP_AD<29>
AD28 AB25 AGP_AD<28>
AD27 AA30 AGP_AD<27>
AD26 AA27 AGP_AD<26>
AD25 Y30 AGP_AD<25>
AD24 AA28 AGP_AD<24>
AD23 W30 AGP_AD<23>
AD22 W27 AGP_AD<22>
AD21 V30 AGP_AD<21>
AD20 V28 AGP_AD<20>
AD19 V29 AGP_AD<19>
AD18 V27 AGP_AD<18>
AD17 U30 AGP_AD<17>
AD16 U28 AGP_AD<16>
AD15 R27 AGP_AD<15>
AD14 R29 AGP_AD<14>
AD13 P28 AGP_AD<13>
AD12 P30 AGP_AD<12>
AD11 P27 AGP_AD<11>
AD10 P29 AGP_AD<10>
AD9 N28 AGP_AD<9>
AD8 N30 AGP_AD<8>
AD7 M30 AGP_AD<7>
AD6 M27 AGP_AD<6>
AD5 M29 AGP_AD<5>
AD4 L28 AGP_AD<4>
AD3 L30 AGP_AD<3>
AD2 L27 AGP_AD<2>
AD1 L29 AGP_AD<1>
AD0 K28 AGP_AD<0>

CBEB3 W28 AGP_CBE<3>
CBEB2 U29 AGP_CBE<2>
CBEB1 R30 AGP_CBE<1>
CBEB0 N27 AGP_CBE<0>
PCICLK AG30 CLK66M_GPU_AGP
FRAMEB U27 AGP_FRAME_L
IRDYB T30 AGP_IRDY_L
TRDYB T28 AGP_TRDY_L
STOPB T27 AGP_STOP_L
DEVSELB T29 AGP_DEVSEL_L
PAR R28 AGP_PAR
REQB AF29 AGP_REQ_L
GNTB AF27 AGP_GNT_L
INTAB AH29 AGP_INT_L
RSTB AH30 AGP_ATI_RESET_L
WBF AE27 AGP_WBF_L
VREFG AK3 AGP_ATI_VREFG
VREF D8 AGP_ATI_VREF

C19 P2 B18 P4 A19 R3 A18 R4 D19 P1 G29 G27 B29 C26 C16 A15 C11 → VSS

A10 C5 A3 G4 E2 U2 V4 AB2 AC4 VSS B23 K2 A23 K1 B22 L2 A22 L1 → VSS

D+ AC10 GPU_THERM_DP
D- AC11 GPU_THERM_DM
TEST_YCLK E8 +GPU_MEM
TEST_MLCK J6 (PULL-UP to GPU_MEM_IO)
MEMTEST C8 ATI_MEMTEST
PLLTEST AC22 NC

MEMVMODE0 B7
MEMVMODE1 B6

38 21 19 18 12 +3V_GPU
38 21 19 18 16 15 12 +1_5V_AGP
38 21 19 18 12 +3V_GPU
38 21 19 20 +1_8V_GPU
39 38 19 GPU_VCORE

R119 47 5% 1/16W MF 402
R127 10K 5% 1/16W MF 402
R159 20K 5% 1/16W MF 402
R172 20K 5% 1/16W MF 402
R158 0 5% 1/16W MF 402
R126 47K 5% 1/16W MF 402
R138 47K 5% 1/16W MF 402
R118 45.3 1% 1/16W MF 402

C62 0.1uF 20% 10V CERM 402
C63 0.01uF 20% 16V CERM 402
(PLACE C1002 CLOSE TO AGPREF PIN)

MAIN_RESET_L IS TOGGLED FOR SLEEP
24 20 17 14 39 30 26 MAIN_RESET_L
R53 47 5% 1/16W MF 402
R54 10K 5% 1/16W MF 402

R43 1K 1% 1/16W MF 402
R44 1K 1% 1/16W MF 402
38 21 18 +GPU_MEM
R45 1K 1% 1/16W MF 402
R46 1K 1% 1/16W MF 402
C11 0.1uF 20% 10V CERM 402
C37 10uF 20% 6.3V CERM 805
PLACE VERF VOLTAGE DIVIDER CLOSE TO ATI M10 VREF PIN

FOR 2.5 VDDR1
MEMVMODE0=1.8V
MEMVMODE1=GND
FOR 1.8 VDDR1
MEMVMODE0=GND
MEMVMODE1=1.8V

ATI_MEMIO_LO R55 4.7K 5% 1/16W MF 402
ATI_MEMIO_HI R104 4.7K 5% 1/16W MF 402
ATI_MEMIO_HI R70 4.7K 5% 1/16W MF 402
ATI_MEMIO_LO R105 4.7K 5% 1/16W MF 402

OMIT

U44
RAGE MOBILITY
M10-CSP64
64MB
BGA
(6 OF 6)

M2 P3 A21 B19 M15 N15 P15 R15 VSS T15 T12 T13 T14 W16 V16 U16 T16 R16 R17 R18 R19
U6 AE15 VDDCI F18 P25

L2
60-OHM-EMI
SM
GPU_VCORE → +GPU_VCORE_VDDCI

C64 0.01uF 20% 16V CERM 402
C67 10uF 20% 6.3V CERM 805
C65 0.01uF 20% 16V CERM 402
C68 0.01uF 20% 16V CERM 402
C66 0.01uF 20% 16V CERM 402
C69 0.01uF 20% 16V CERM 402

U44
RAGE MOBILITY
M10-CSP64
64MB
BGA
(2 OF 6)

B26 A26 B25 A25 C22 D21 C21 D20 C20 D22 C23 D23 A27 B27 → VSS
H2 H1 J2 J1 K4 K3 L4 M3 L3 M4 N2 N1 N4 N3 G30 G28 B30 D26 D16 B15 D11 B10 D5 B3 G3 E1 U1 V3 AB1 AC3 J30 J29 H30 H29 F30 F29 E30 E29 J28 J27 H28 H27 F28 F27 E28 E27 D30 D29 C30 C29 A30 A29 A28 B28 D28 C28 D27 C27 D25 C25 D24 C24 D18 C18 D17 C17 D15 C15 D14 C14 B17 → VSS

OMIT

A17 B16 A16 B14 A14 B13 A13 D13 C13 D12 C12 D10 C10 D9 C9 B12 A12 B11 A11 B9 A9 B8 A8 C7 D7 C6 D6 C4 D4 C3 D3 A5 B5 A4 B4 A2 B2 A1 B1 E4 E3 F3 F4 H3 H4 J3 J4 C1 C2 D1 D2 F1 F2 G1 G2 R1 R2 T1 T2 V1 V2 W1 W2 T3 T4 U3 U4 W3 W4 Y3 Y4 V1 Y2 AA1 AA2 AC1 AC2 AD1 AD2 AA3 AA4 AB3 AB4 AD3 AD4 AE3 AE4 → VSS

27M OSC

(PLACE THE OSCILLATOR AND R1015 AND R1077 CLOSE TO ATI PIN AJ29)

+3V_SLEEP
L4 FERR-EMI-100-OHM SM
38 +3V_ATI_OSC_SLEEP
C77 0.1uF 20% 10V CERM 402
C78 4.7uF 20% 6.3V CERM 805
NO STUFF R188 100K 5% 1/16W MF 402
CRITICAL
VCC
G2 27.0000M OSC SM-1
OE
OUT
GND
ATI_OSC_OE
ATI_CLK27M_OSC
(PLACE R1085 CLOSE TO OSC)
GPU_SS R200 0 1% 1/16W MF 402
ATI_CLK27M_OSC_SS 18
R189 287 1% 1/16W MF 402
ATI_CLK27M_IN 19
R195 162 1% 1/16W MF 402

S0=1;S1=M => -1.5% DOWN-SPREAD
SPREAD SPECTRUM SUPPORT

+3V_SLEEP
GPU_SS L3 FERR-EMI-100-OHM SM
38 +3V_ATI_SS
GPU_SS C70 10uF 20% 6.3V CERM 805
GPU_SS C71 0.1uF 20% 10V CERM 402
NO STUFF R173 0 5% 1/16W MF 402
GPU_SS R181 0 5% 1/16W MF 402
GPU_SS CRITICAL
VDD
U47 CY25811 SOI
18 ATI_CLK27M_OSC_SS XIN/CLKIN
NC XOUT SSCLK 5 ATI_SSCLK_UF
NC FRSEL
CY25811_S1 S1
CY25811_S0 S0
VSS
GPU_SS R201 33 5% 1/16W MF 402
ATI_SSCLK_IN 19
NO STUFF R37 0 5% 1/16W MF 402
NO STUFF R38 0 5% 1/16W MF 402

M10 AGP INTERFACE

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D	051-6459	A
SCALE: NONE	SHT 18 OF 44	

TMDS TERMINATION

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN
CMF LINE SHOULD BE ROUTED AS 4MIL SURFACE
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS

U44
RAGE_MOBILITY
M10-CSP64
64MB
BGA
(3 OF 6)

EXT_TMDS R228 10K 5% 1/16W MF 402
INT_TMDS R234 10K 5% 1/16W MF 402
R223 NO STUFF 10K 5% 1/16W MF 402
R221 1K 5% 1/16W MF 402
R229 1K 5% 1/16W MF 402

Q77 SI3446DV TSOP
L24 FERR-220-OHM 0805 (500mA)
C166 1000pF 10% 25V X7R 402

GPU_VCORE = 1.2V
(PUT ALL CAPs BELOW ATI ASIC)

C222 C256 C299 C305 0.01uF 20% 16V CERM 402
C328 10uF 20% 6.3V CERM 805
C232 C269 C300 C306 0.01uF 20% 16V CERM 402
C167 C219 10uF 20% 6.3V CERM 805
C252 C270 C301 C307 C329 C332 0.22uF 20% 6.3V CERM 402
C186 C220 C253 C271 C302 C311 C330 C333 0.22uF 20% 6.3V CERM 402
C187 C221 C254 C282 C303 C326 C331 C338 0.22uF 20% 6.3V CERM 402

U44
RAGE_MOBILITY
M10-CSP64
64MB
BGA
(5 OF 6)

VDD15
VDDC
VSS
OMIT

M10 Power Shut down Sequencing

XW21 XW24 XW20 XW23 XW22 SM
DP6 BAS16TW SOT-363

R258 R260 R262 R265 R269 R271 R273 10K 5% 1/16W MF 402 (NO STUFF)
R259 R261 R263 R266 R270 R272 R274 10K 5% 1/16W MF 402 (NO STUFF)

GPU VCORE SUPPLY

U16 LTC1778 SSOP (CRITICAL)
R389 1M 5% 1/16W MF 402
R430 1 5% 1/16W MF 603
R339 576K 1% 1/16W MF 402
R388 0 5% 1/16W MF 402 (NO STUFF)
R341 63.4K 1% 1/16W MF 402
R236 100K 5% 1/16W MF 402
R390 0 5% 1/16W MF 402
R340 20K 1% 1/16W MF 402
R311 0 5% 1/16W MF 402
R332 0 5% 1/16W MF 402
C473 4.7UF 20% 10V CERM 1206
C494 0.1uF 20% 25V CERM 603
C514 0.1uF 20% 25V CERM 603
C451 220pF 5% 25V CERM 402
C448 470pF 10% 50V CERM 402
C483 0.1uF 20% 10V CERM 402
C882 0.0022UF 10% 50V CERM 402 (NO STUFF)
D5 MBR0540 SM
R416 2.2 5% 1/16W MF 603
Q51 SI7860DP SO-8-PWRPK (CRITICAL)
Q48 SI7892DP SO-8-PWRPK (CRITICAL)
L30 2.1UH-11A SM (CRITICAL)
D24 B340LB SMB
C762 C766 4.7UF 20% 25V CERM 1206
C708 22uF 20% 10V CERM 1210
C719 C720 330UF 20% 6.3V POLY SMD
C721 330UF 20% 6.3V POLY SMD
R352 4.99K 1% 1/16W MF 402
R451 18.2K 1% 1/16W MF 402
R804 1.82K 1% 1/16W MF 402
R351 20K 1% 1/16W MF 402
R307 100K 5% 1/16W MF 402
C902 0.1UF 20% 10V CERM 402
R410 10K 5% 1/16W MF 402
C515 0.1uF 20% 10V CERM 402
Q80 2N7002DW SOT-363

WHEN VCORE_CNTL HIGH => 1.2V
1.2V = 0.8V * (1 + R332 / (R331//R333))

WHEN VCORE_CNTL LOW => 1.0V
1.0V = 0.8V * (1 + R332 / R333)

R306 R316 100K 5% 1/16W MF 402
R294 10K 5% 1/16W MF 402
R203 33K 5% 1/16W MF 402
DP1 BAS16TW SOT-363
Q6 2N3904 SM
Q5 2N3904 SM

M10 CORE PWR/LVDS/TMDS
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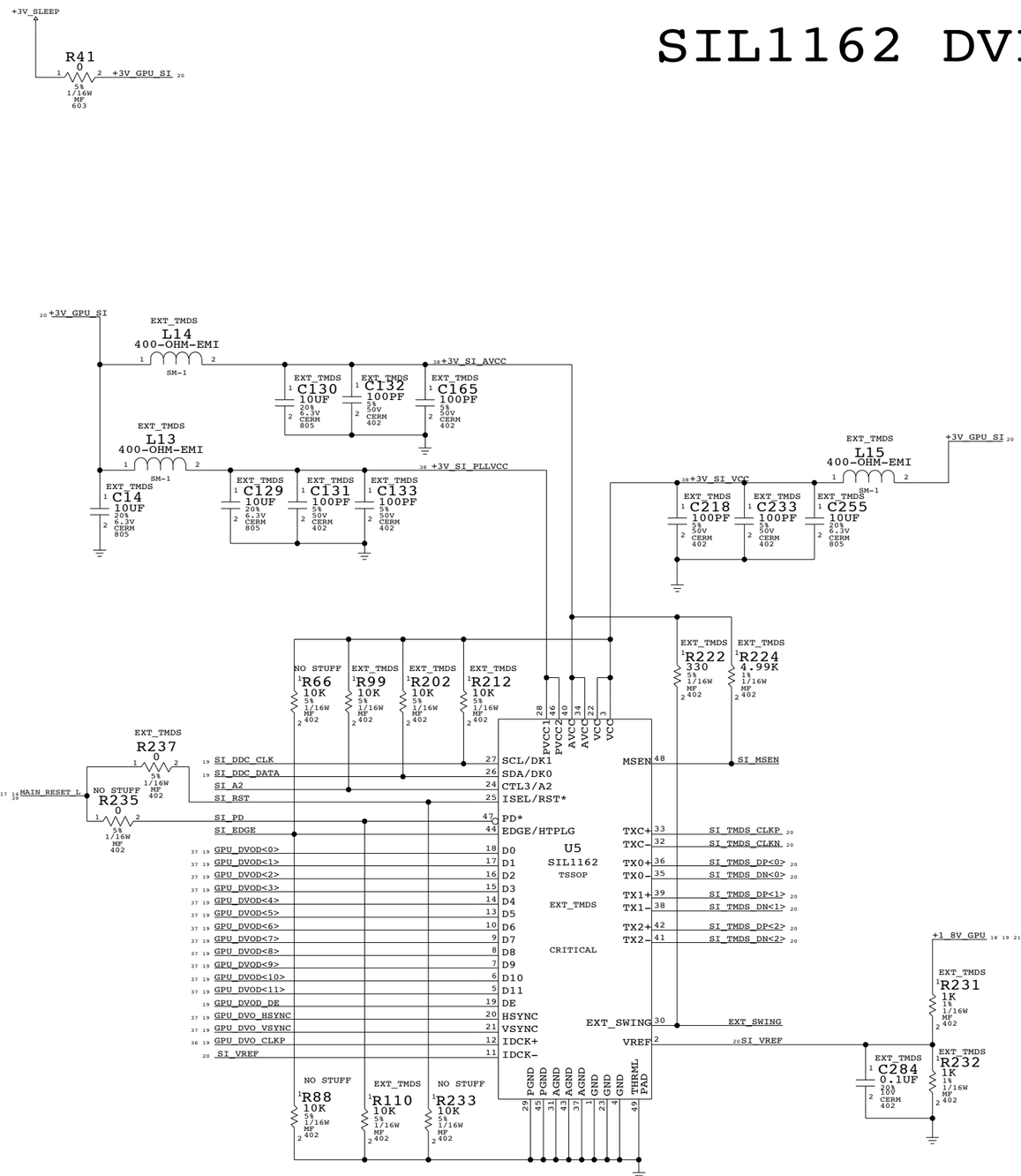
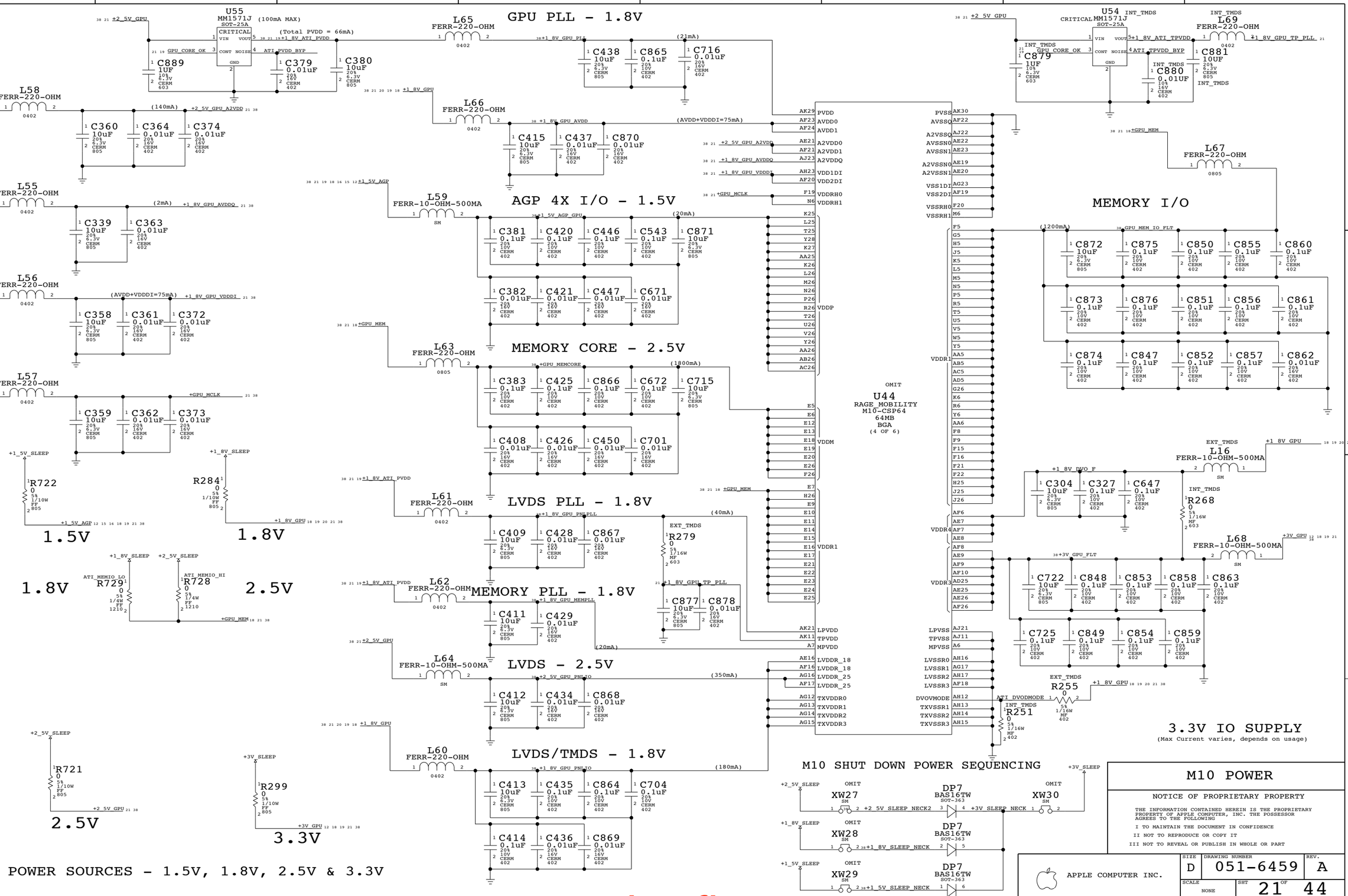
SIZE D | DRAWING NUMBER 051-6459 | REV. A
SCALE NONE | SHT 19 OF 44

SIL1162 DVI TRANSMITTER



APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6459	A
SCALE: NONE	SHT 20 OF 44	



EXTERNAL VIDEO (DVI) INTERFACE

ANALOG FILTERING PLACE CLOSE TO CONNECTOR

FL2 CRITICAL LCFILTER SM-220MHZ
FL1 CRITICAL LCFILTER SM-220MHZ
FL3 CRITICAL LCFILTER SM-220MHZ
GPU_B, GPU_G, GPU_R → VGA_B, VGA_G, VGA_R
C685 3.3PF 0.25% 50V CERM 402
C676 3.3PF 0.25% 50V CERM 402
C684 3.3PF 0.25% 50V CERM 402

VGA VSYNC BUFFERS

+3V_MAIN
U56 CRITICAL 74AHC1G32 SM
U57 CRITICAL 74AHC1G32 SM
ATI_HSYNC → R718 33 5% 1/16W MF 402 → VGA_HSYNC
ATI_VSYNC → R714 33 5% 1/16W MF 402 → VGA_VSYNC

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)

+5V_SLEEP → F1 0.5AMP-13.2V SM → +5V_DDC_SLEEP_UF → L23 400-OHM-EMI SM-1 → +5V_DDC_SLEEP

Isolation required for DVI power switch

D21 SM MBR0530 → DDC_CLK_ISO
R655 4.7K 5% 1/16W MF 402
R661 4.7K 5% 1/16W MF 402

J14 CRITICAL QH1112 F-RT-TH

TMDS_CONN_DN<0>	17	1	TMDS_CONN_DN<2>
TMDS_CONN_DP<0>	18	9	TMDS_CONN_DN<1>
(TMDS_DN<5>)	19	2	TMDS_CONN_DP<2>
(TMDS_DP<5>)	20	10	TMDS_CONN_DP<1>
NC	21	3	NC
TMDS_CONN_CLKP	22	11	(TMDS_DN<4>)
TMDS_CONN_CLKN	23	4	NC
DVI_DDC_CLK_UF	24	12	(TMDS_DP<4>)
(+5V_DDC_SLEEP)	25	5	NC
DVI_DDC_DATA_UF	26	13	(TMDS_DP<3>)
VGA_VSYNC	27	6	NC
DVI_HPD_UF	28	14	NC
VGA_R	29	7	NC
VGA_G	30	15	NC
VGA_B	31	8	NC
VGA_HSYNC	32	16	NC
	33	34	35

R670 100 5% 1/16W MF 402
R649 100 5% 1/16W MF 402
R650 100 5% 1/16W MF 402
C706 100pF 5% 50V CERM 402
C669 100pF 5% 50V CERM 402
C1 100pF 5% 50V CERM 402
C710 0.01UF 20% 50V CERM 603
R706 0 5% 1/16W MF 402 — PLACE NEAR 3, 11 & 19
R1 0 5% 1/16W MF 402 — PLACE NEAR C5A & C5B
CHGND1, CHGND5

3V LEVEL SHIFTERS

+3V_SLEEP
Q38 2N7002DW SOT-363 (DVI_DDC_CLK → GPU_DVI_DDC_CLK)
Q38 2N7002DW SOT-363 (DVI_DDC_DATA → GPU_DVI_DDC_DATA)
Q35 2N7002DW SOT-363 (DVI_HPD → GPU_HPD)
R662 10K 5% 1/16W MF 402
R671 10K 5% 1/16W MF 402
R694 100K 5% 1/16W MF 402

NOTE: Pulldown for DVI_HPD provided by DVI power switch interface
NOTE: DVI_HPD SHARES Q68 WITH ALS BECAUSE OF BOARD REAL ESTATE

DVI POWER SWITCH

Power key detect path when system is shutdown or asleep.. DDC_CLK is isolated from NV17M DURING SHUTDOWN. WHEN power key on remote device is pressed, 5V will be driven into DDC_CLK. Since host rails will be low, TP0610 will turn on, driving SOFT_PWR_ON_L low. As host rails rise, TP0610 will turn off, as will remote device path into DDC_CLK. Isolation will be disabled as well.

Q40 TP0610 SM
R690 680 5% 1/16W MF 402
R691 10K 5% 1/16W MF 402
R688 330 5% 1/16W MF 402 — Pulldown prevents 3904 from turning on when DVI monitor has active, self-powered DDC clock pullup.
Q42 2N3904 SM
DVI_DDC_CLK_UF, DVI_TURN_ON, DVI_TRUN_ON_ILIM, DVI_TURN_ON_BASE, +5V_DDC_SLEEP, SOFT_PWR_ON_L

Power key detect path when system is running. HPD normally driven to 3.3V. When power key on remote device pressed, HPD will be driven to 5V. COMPARATOR ENABLED BY NV17MAP GPIO.

+3V_SLEEP
R680 68.1K 1% 1/16W MF 402
C696 0.1UF 20% 10V CERM 402
U46 CRITICAL LMC7211 SM
R663 10K 1% 1/16W MF 402 ← DVI_HPD_UF, DVI_HPD_DIV
R686 10K 1% 1/16W MF 402
R681 100K 1% 1/16W MF 402
HPD_4V_REF, HPD_PWR_SW, HPD_ON
Q41 2N7002DW SOT-363
+PBUS
Q45 TP0610 SM
R696 100K 5% 1/16W MF 402
R704 100K 5% 1/16W MF 402
COMP_ENABLE, COMP_DISABLE, HPD_ON_RC
R703 330 5% 1/16W MF 402
R700 20K 5% 1/16W MF 402
Q44 2N3904 SM
HPD_BASE
C703 47UF 20% 6.3V CERM 1210
R705 68K 5% 1/16W MF 402
NEED PULL-DOWN BECAUSE THIS SIGNAL IS TRISTATED INITIALLY
Q41 2N7002DW SOT-363
HPD_PWR_SNS_EN
R213 100K 5% 1/16W MF 402

TMDS FILTERING PLACE CLOSE TO CONNECTOR

L72 CRITICAL 90-OHM-200MA SM
L21 CRITICAL 165-OHM SM
L73 90-OHM-200MA SM
L74 90-OHM-200MA SM
TMDS_DN<0>, TMDS_DP<0>, TMDS_CLKP, TMDS_CLKN, TMDS_DN<1>, TMDS_DP<1>, TMDS_DN<2>, TMDS_DP<2> → TMDS_CONN_*

LCD INTERFACE

LVDS INTERFACE

100K pull-ups are for no-panel case (development) Panel has 2K pull-ups

C416 0.001uF 20% 50V CERM 402 → CHGND4
+3V_SLEEP
R342 100K 5% 1/16W MF 402
R320 100K 5% 1/16W MF 402
LVDS_DDC_CLK, LVDS_DDC_DATA
NO STUFF
C449 0.001uF 20% 50V CERM 402
C452 0.001uF 20% 50V CERM 402 → CHGND4
+3V_LCD (LVDS DDC POWER)
CRITICAL J6 G-501973 F-RT-SM
LVDS_L0N, LVDS_L0P, LVDS_L1N, LVDS_L1P, LVDS_L2N, LVDS_L2P, CLKLVDS_LN, CLKLVDS_LP, LVDS_U0N, LVDS_U0P, LVDS_U1N, LVDS_U1P, LVDS_U2N, LVDS_U2P, CLKLVDS_UN, CLKLVDS_UP
C500 0.001uF 20% 50V CERM 402 → CHGND4

INVERTER INTERFACE

+PBUS
L33 FERR-1K-OHM-EMI SM → +12_8V_INV
+5V_MAIN
Q7 FDG6324L SC70-6
+5V_INV_UF_SW
L32 400-OHM-EMI SM-1
R317 100K 5% 1/16W MF 402
FP_PWR_EN_L
C440 10UF 20% 6.3V CERM 805
+5V_INV_SW
C746 0.001UF 20% 50V CERM 402
CRITICAL J7 SM-2MT
Q7 FDG6324L SC70-6
FP_PWR_EN
C749 0.001UF 20% 50V CERM 402
L31 400-OHM-EMI SM-1
BRIGHT_PWM
C739 0.001UF 20% 50V CERM 402
+3V_PMU
C552 0.1UF 20% 10V CERM 402
INV_ON_PWM
74LVC32 TSSOP U24
BRIGHT_PWM_UF
INVERTER EXPECTS ACTIVE HIGH SIGNAL
SHARES LOGIC WITH KB RESET SIGNALS (PG 28)
R724 0 5% 1/16W MF 402
C744 0.01uF 20% 50V CERM 603 → CHGND2

S-VIDEO/COMP OUT INTERFACE

Place GND shorts at graphics controller

XW12 SM — GPU_TV_GND1
XW13 SM — GPU_TV_GND2
L26 FERR-10-OHM-500MA SM → TV_GND1
L28 FERR-10-OHM-500MA SM → TV_GND2
L25 3.3UH 0603 — GPU_Y
L29 3.3UH 0603 — GPU_C
L27 3.3UH 0603 — GPU_COMP
C712 0.01UF 20% 50V CERM 603
C702 560PF 10% 50V CERM 402
C707 560PF 10% 50V CERM 402
C718 560PF 10% 50V CERM 402
C724 560PF 10% 50V CERM 402
C714 560PF 10% 50V CERM 402
C713 560PF 10% 50V CERM 402
C717 0.01UF 20% 50V CERM 603
CRITICAL J15 MINIDIN RT-TH MH1177 → TV_C, TV_Y, TV_COMP
CHGND1

Place GND shorts at graphics controller

LCD POWER SWITCHES

+3V_MAIN
R400 100K 5% 1/16W MF 402
C484 2200pF 5% 50V CERM 603
R391 100K 5% 1/16W MF 402
LCD_PWREN_L
Q11 TSOP SI3443DV
+3V_LCD_SW
L6 FERR-250-OHM SM
C474 0.001uF 20% 50V CERM 402 → CHGND4
LCD_DIGON_L
Q8 2N7002 SM
FP_PWR_EN

VIDEO CONNECTORS

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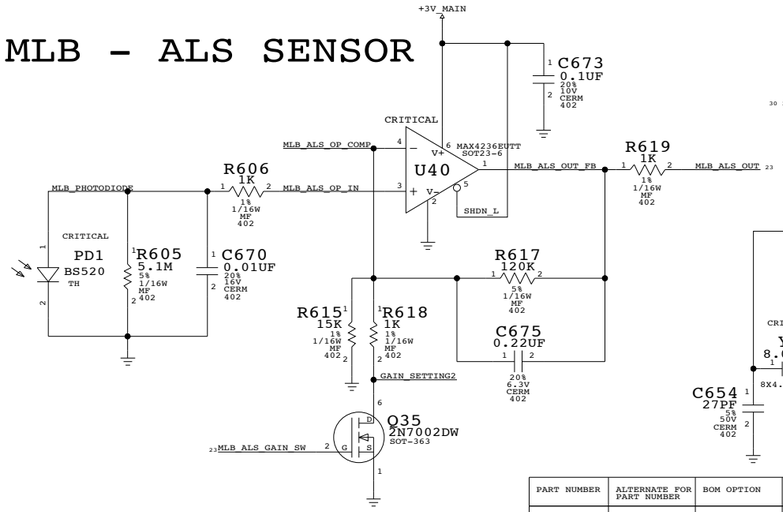
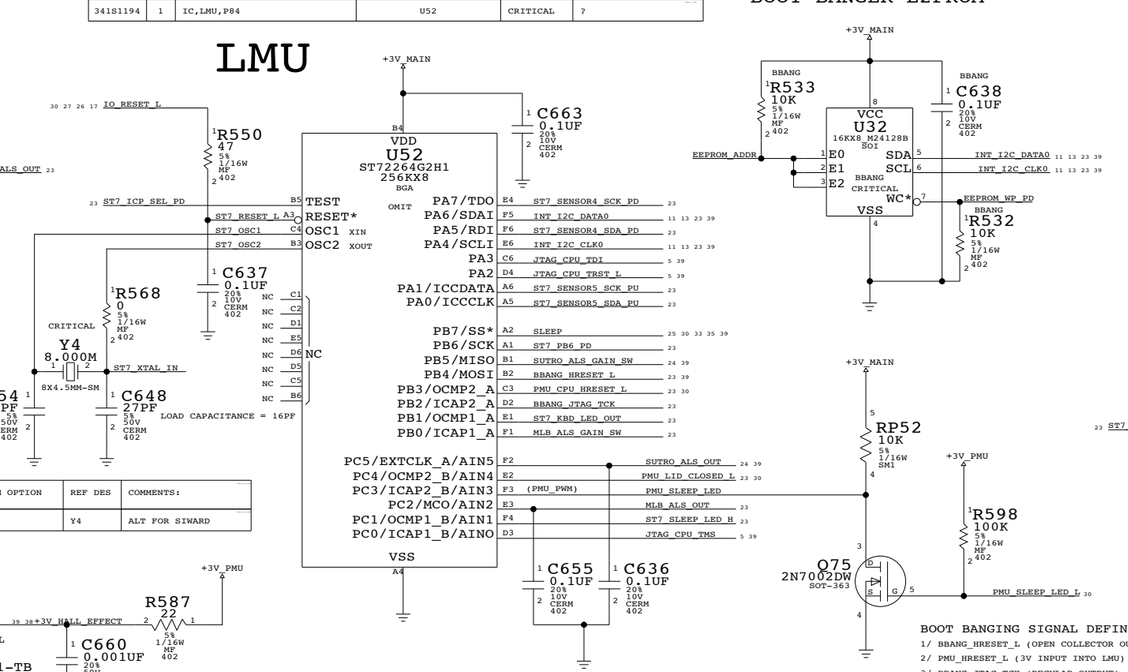
D	051-6459	A
SCALE: NONE	SHT 22 OF 44	

MLB - ALS SENSOR



LMU

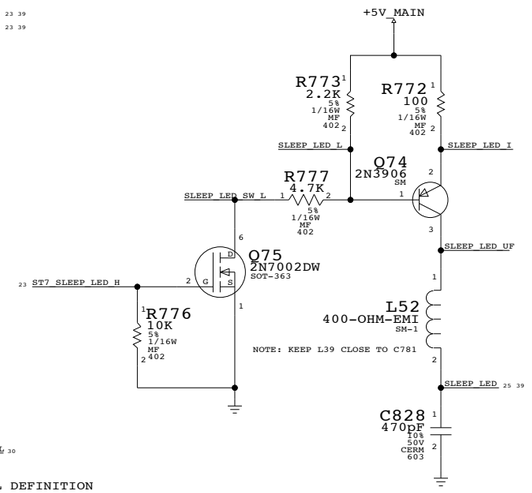


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0008	197S0040		Y4	ALT FOR SIWARD

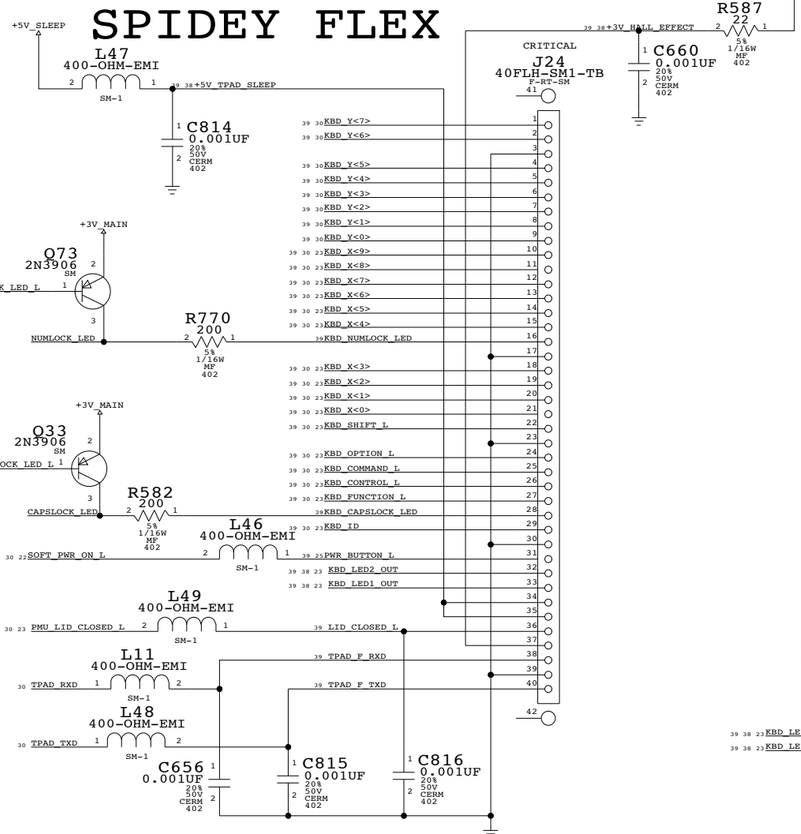
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1194	1	IC,LMU,P84	U52	CRITICAL	?

BOOT BANGER E2PROM

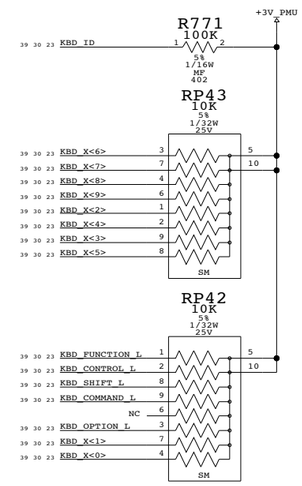
SLEEP LED



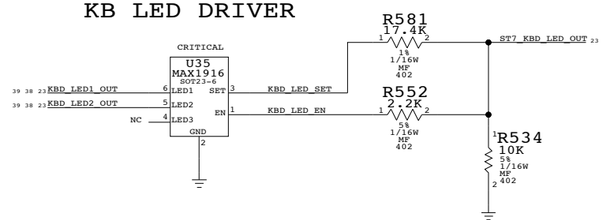
SPIDEY FLEX



KEYBOARD PULLUPS

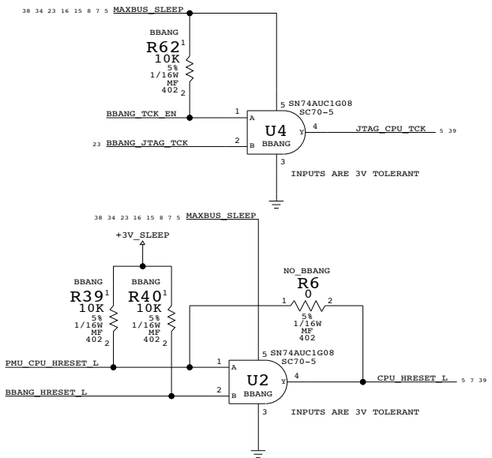


KB LED DRIVER

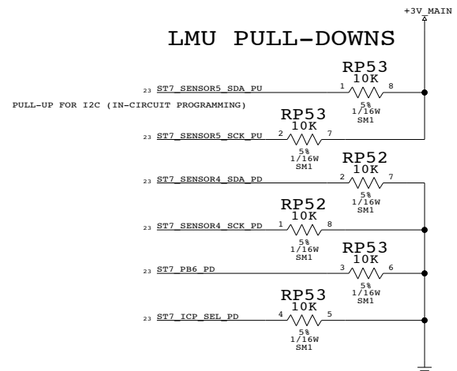


BOOT BANGING SIGNAL DEFINITION

1/ BBANG_HRESET_L (OPEN COLLECTOR OUTPUT - 10K PULLUP ON MLB)
2/ PMU_HRESET_L (3V INPUT INTO LMU)
3/ BBANG_JTAG_TCK (REGULAR OUTPUT)
4/ JTAG_CPU_TMS (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
5/ JTAG_CPU_TDI (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
6/ JTAG_CPU_TRST_L (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)



LMU PULL-DOWNS



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LMU/BOOTBANGER/SPIDEY

APPLE COMPUTER INC.

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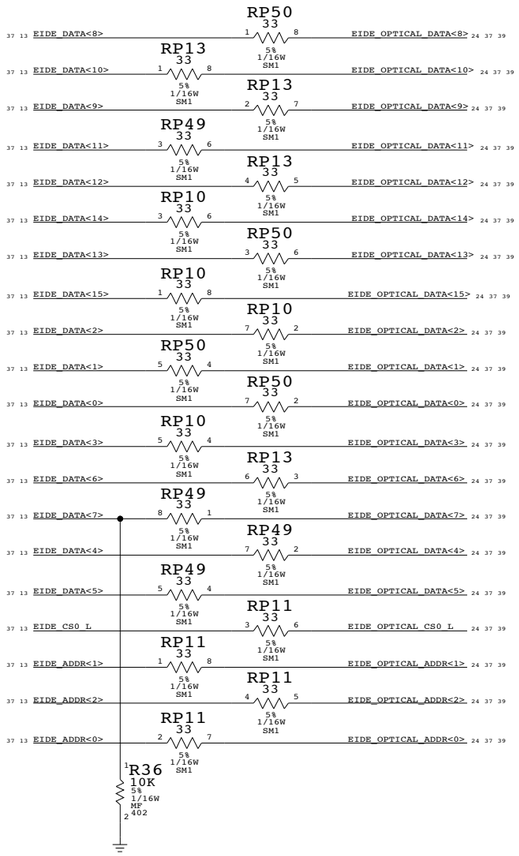
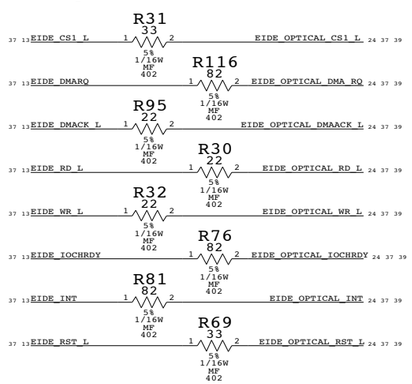
HARD DRIVE INTERFACE (UATA100)

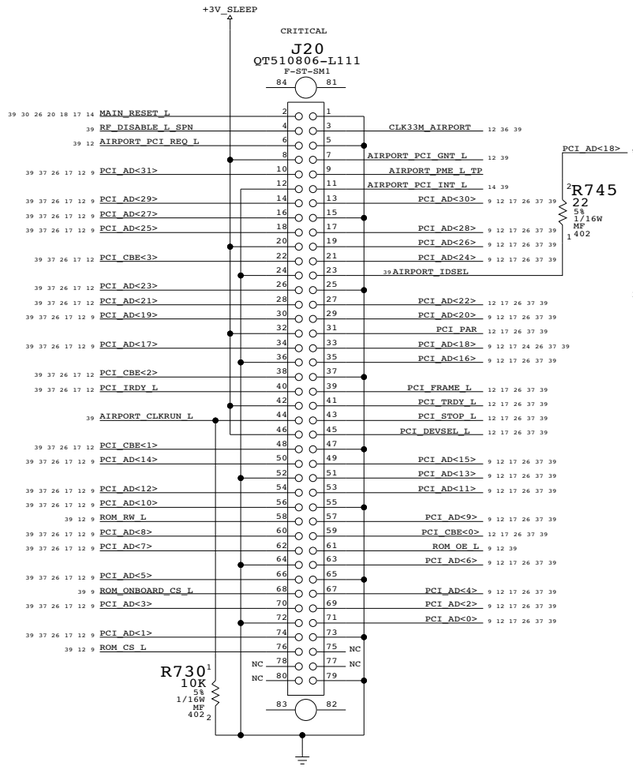
EIDE SERIES TERMINATION

PLACE TERMINATORS NEAR INTREPID

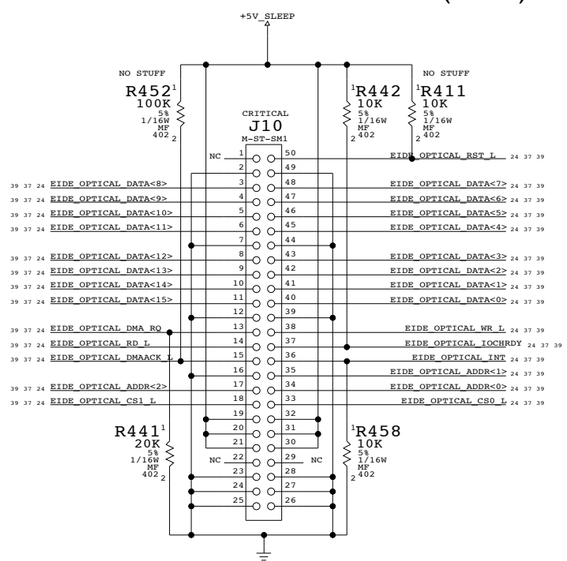




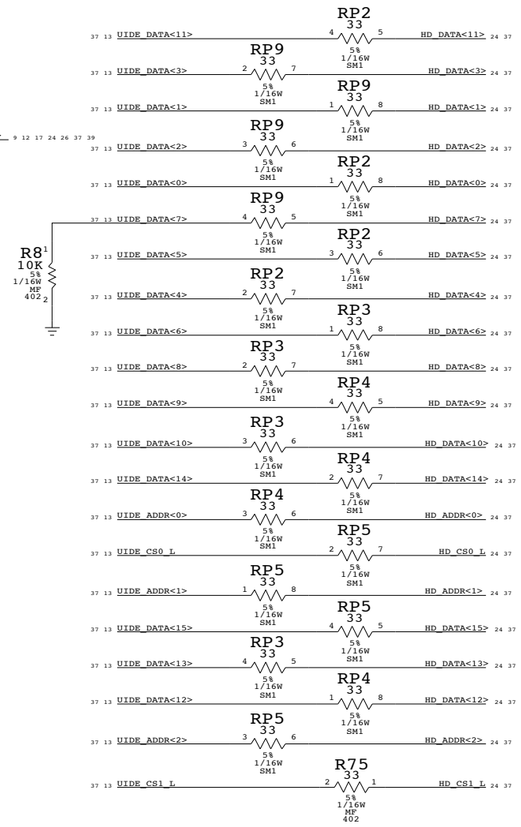
WIRELESS INTERFACE



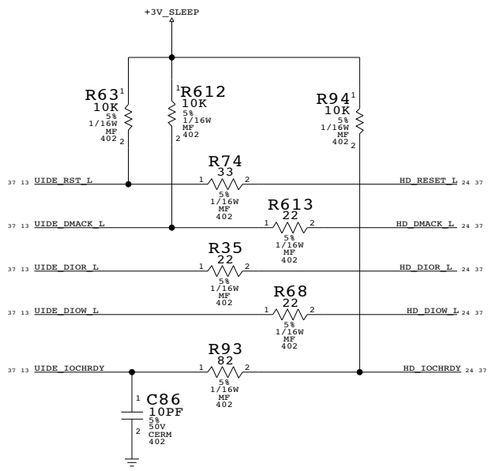
OPTICAL DRIVE INTERFACE (EIDE)



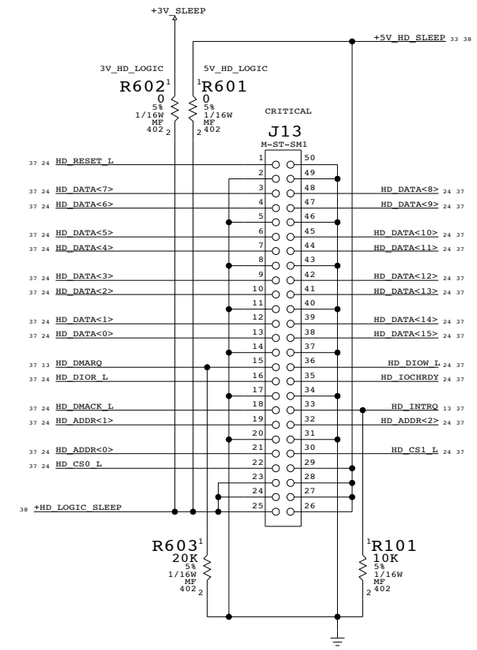
PLACE SERIES R CLOSE TO INTERPID



PLACE PULLUP RESISTORS CLOSE TO INTREPID

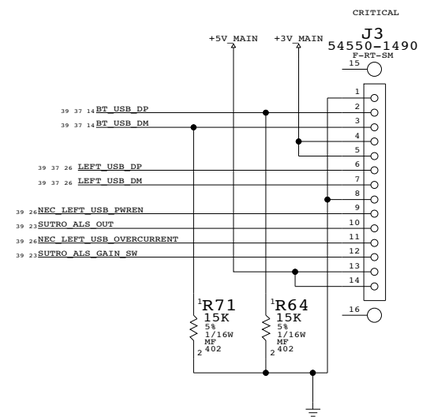


IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V



ANY SEQUENCING REQUIREMENT BETWEEN +5V_HD_SLEEP AND +3V_SLEEP?

BLUETOOTH/LEFT-SIDE USB



INTERNAL I/O CONNECTORS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6459	A
SCALE: NONE	SHT 24 OF 44	

SOUND BOARD (SOUSAPHONE)

AUDIO - SNAPPER
SND - INTREPID

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1000	7	RES	RES-402-V2	RESISTOR	0		1/16W	5%	L77,L80,L81,L82,L76,L78,L79	

PLACE XW9 CLOSE TO 5V SWITCHER (U27)
PLACE CAPS AS CLOSE TO THERMISTORS AS POSSIBLE
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY

CAPS FOR EMI EXPERIMENTATION ONLY

FAN INTERFACE

KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

MODEM

SUPPORTS BOTH THE LAST DASH AND Q52 SOFT MODEM

FAN CONTROLLER

THERM ISOLATION

SERIAL DEBUG INTERFACE

DEBUG POWER BUTTON

DEBUG JUMPERS

RIGHT FAN (GPU)

LEFT FAN (CPU)

FAN/MODEM/SOUND/SLEEP LED/DEBUG

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6459	A
SCALE: NONE	SHT 25 OF 44	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0608	197S0038	NEC_USB	Y5	ALT FOR SIWARD

Y7 LOAD CAPACITANCE IS 16PF

SERR_L AND PERR_L
HAS DEDICATED PULL-UP
FOR BOTH CBUS AND USB2

Series Rpaks required to facilitate NAND-tree testing

INTREPID USB CONSTRAINTS

NEED PULL-UP RESISTORS IN CASE USB 1.0 IS USED FOR PORT POWER

PLACE NEAR J3

SUTRO CONNECTOR

PLACE NEAR J12

BUBBA CONNECTOR

USB 2.0

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6459	A
SCALE: NONE	SHT 26 OF 44	

Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

+3V_MAIN

C442 10uF 20% 6.3V CERM 805

NO STUFF R333 0 5% 1/16W MF 402

3405_MODE

R319 0 5% 1/16W MF 402

U14 LTC3405 SOT23-6 — VIN, RUN, MODE, GND, SW, VFB

LTC3405_SW

CRITICAL L5 3.3uH SM1

R334 665K 1% 1/16W MF 402 R2A

C471 22pF 5% 50V CERM 402

R361 49.9K 1% 1/16W MF 402 R2B

3405_VFB

R362 182K 1% 1/16W MF 402 R1

+1_0V_MARVELL

C486 10uF 20% 6.3V CERM 805

VOUT = 0.8V*(1+R2EQV/R1)

R2EQV = R2A||R2B

PLACE ALL SERIES RES CLOSE TO PHY

R370 0 5% 1/16W MF 402 — CLKENET_LINK_TX / CLKENET_PHY_TX

R353 0 5% 1/16W MF 402 — CLKENET_LINK_RX / CLKENET_PHY_RX

R344 0 5% 1/16W MF 402 — CLKENET_LINK_GBE_REF / CLKENET_PHY_GBE_REF

CRITICAL U49 88E1111 BCC

TX_CLK, RX_CLK, 125CLK

TXD0–TXD7, TX_EN, TX_ER, GTX_CLK

RXD0–RXD7, RX_DV, RX_ER, CRS, COL, MDC, MDIO

INT-/INT+, RESET, COMA

S_IN+, S_IN-, S_OUT+, S_OUT-, S_CLK+, S_CLK-

HSDAC+, HSDAC-

XTAL1, XTAL2, VSSC

CTRL10 — NC

DVDD: C492 0.1UF, C511 0.01UF, C517 0.1UF, C502 0.01UF, C465 0.1UF, C475 0.01UF

PLACE CAPS (IN ORDER) ON PINS 1, 6, 10/15, 57/62, 67/71, 85

VDDO: C464 0.1UF, C472 0.01UF, C453 0.1UF, C503 0.01UF, C501 0.1UF, C496 10uF 6.3V CERM 805

PLACE CAPS (IN ORDER) ON PINS 5, 21/26, 48/52, 66/72, 88, 96

+2_5V_MARVELL

VDDOH

VDDOX

L34 FERR-EMI-600-OHM SM

+2_5V_MARVELL_AVDD

AVDD: C497 0.1UF, C504 0.1UF, C487 0.01UF, C476 0.1UF, C754 10uF 6.3V CERM 805

PLACE CAPS (IN ORDER) ON PINS 32/35, 36/40, 45 & 78

GND

+2_5V_MAIN

R465 0 5% 1/16W MF 603

C488 0.1UF, C466 0.1UF, C506 0.1UF, C520 0.1UF

PLACE CAPS AT TRANSFORMER PINS 1, 4, 7 & 10

PLACE CLOSE TO ETHERNET CONNECTOR

NO STUFF R438 0 5% 1/10W MF 805 — CHGND1

CRITICAL J17 RJ45 RT-TH

RJ45_DP<0>, RJ45_C0_PD, RJ45_DN<0>, RJ45_DP<1>, RJ45_C1_PD, RJ45_DN<1>, RJ45_DP<2>, RJ45_C2_PD, RJ45_DN<2>, RJ45_DP<3>, RJ45_C3_PD, RJ45_DN<3>

Short shielded RJ-45 — CHGND1

CRITICAL T1 XFR-ENET-1000BT SM

MDI0+, MDI0-, MDI1+, MDI1-, MDI2+, MDI2-, MDI3+, MDI3-

R346 49.9 1% 1/16W MF 402 — MDI0_PD

R372 49.9 1% 1/16W MF 402 — MDI1_PD

R404 49.9 1% 1/16W MF 402 — MDI2_PD

R413 49.9 1% 1/16W MF 402 — MDI3_PD

C454 0.01UF, C477 0.01UF, C493 0.01UF, C505 0.01UF

PLACE RESISTORS CLOSE TO PHY

R735 75 5% 1/16W MF 402, R733 75 5% 1/16W MF 402, R382 75 5% 1/16W MF 402, R347 75 5% 1/16W MF 402 — ENET_CTAP_CHGND

C457 100pF 10% 3KV CERM 1808 — CHGND1

LED_LINK10, LED_LINK100, LED_LINK1000 (NC), LED_DUPLEX (NC), LED_RX, LED_TX (NC)

CONFIG0 (000), CONFIG1 (000), CONFIG2 (111), CONFIG3 (110), CONFIG4 (111), CONFIG5 (101), CONFIG6 (000)

SEE CONFIG TABLES (BELOW)

TDI, TDO, TCK, TMS, TRST — JTAG_ENET_TDI, JTAG_ASIC_TDO_TP, JTAG_ASIC_TCK, JTAG_ASIC_TMS, JTAG_ASIC_TRST_L

RSET — ENET_RSET

SEL_OSC, SEL_2.5V (NC)

R380 4.99K 1% 1/16W MF 402

R371 10K 5% 1/16W MF 402

R345 10K 5% 1/16W MF 402

R354 1.5K 1% 1/16W MF 402

R343 1K 5% 1/16W MF 402 — INT_ENET_RST_L

D1 1N914 SOT23 — ENET_ENERGY_DET, ENET_RST_L, IO_RESET_L

Q15 2N7002DW SOT-363 — AC_IN

Q15 2N7002DW SOT-363 — SLEEP_L_LS5

PLACES PHY IN "COMA" MODE WHEN ASLEEP ON BATTERY (SAVES POWER)

C755 2.2uF 20% 10V CERM 805 — ENET_COMA

ENET_HSDACP, ENET_HSDACM

ENET_VSSC

+2_5V_MARVELL

NO STUFF R435 20K 5% 1/16W MF 402

PUT CRYSTAL CIRCUIT CLOSE TO PHY

R427 0 5% 1/16W MF 402

CRITICAL Y3 25.0000M 8X4.5MM-SM — CLK25M_XTAL_IN

C555 33pF 5% 50V CERM 402, C491 33pF 5% 50V CERM 402

Y3'S LOAD CAPACITANCE IS 20PF

NO STUFF R393 49.9 1% 1/16W MF 402

NO STUFF R403 49.9 1% 1/16W MF 402

R335 10K 5% 1/16W MF 402

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0703	197S0037	ALTERNATE	Y3	
197S0603	197S0037	ALTERNATE	Y3	ALT FOR SIWARD

CONFIG DEFINITIONS

PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS

PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

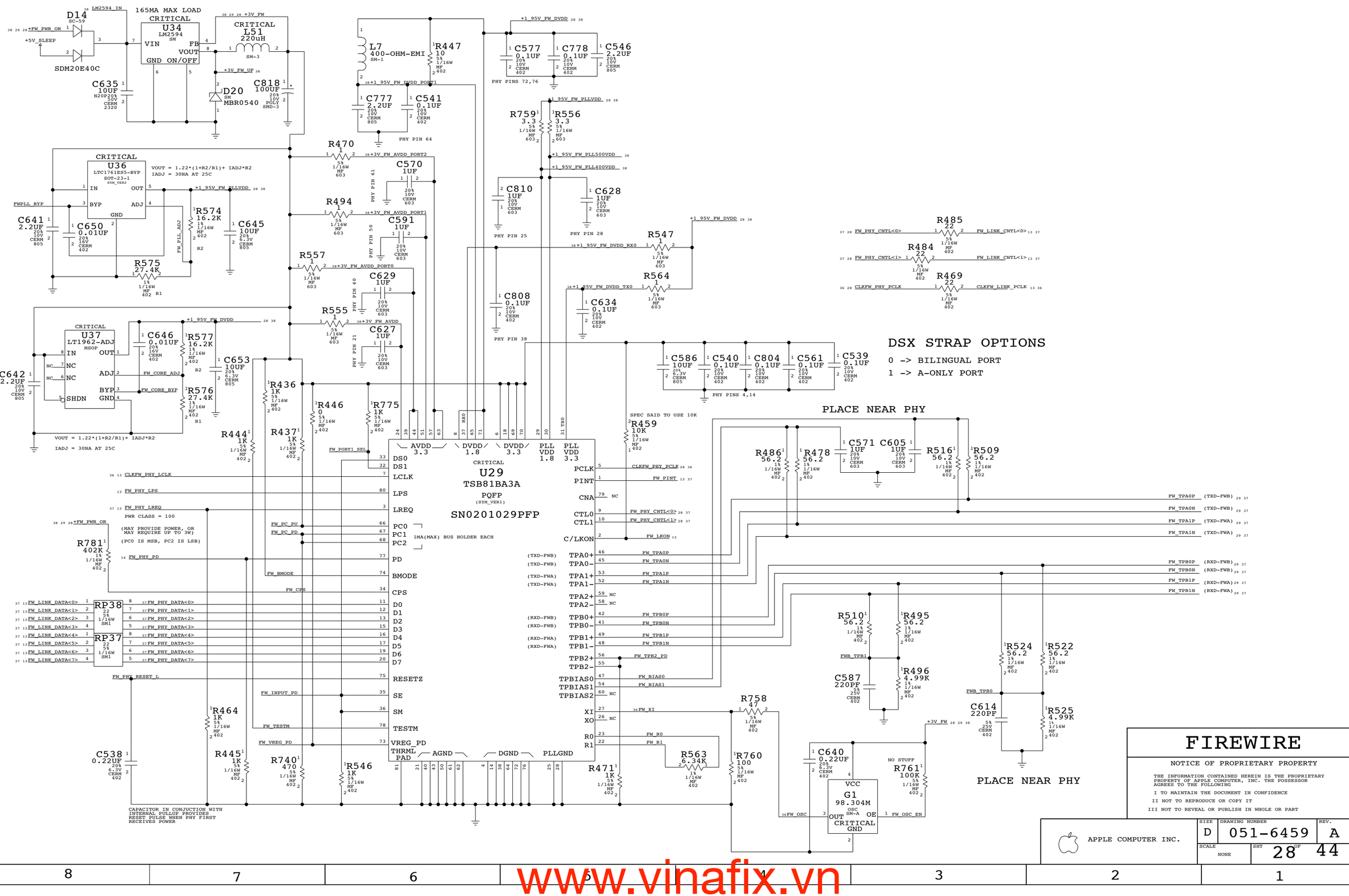
MARVELL 88E1111

10/100/1000 ETHERNET

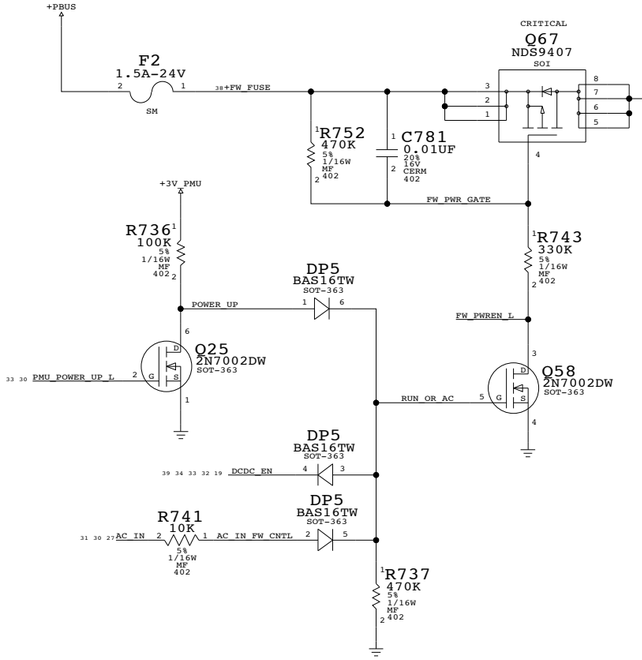
APPLE COMPUTER INC.

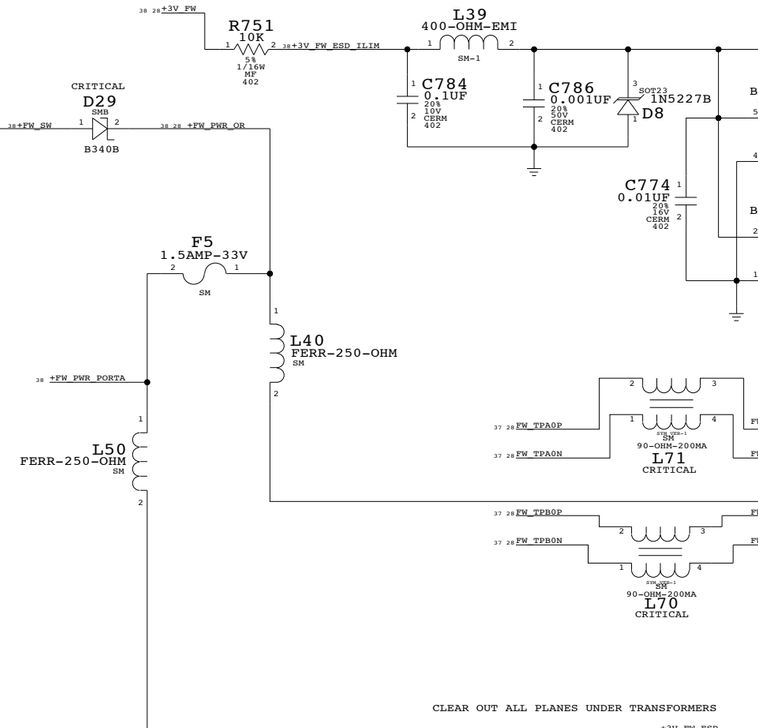
SIZE D | DRAWING NUMBER 051-6459 | REV. A

SCALE NONE | SHT 27 OF 44



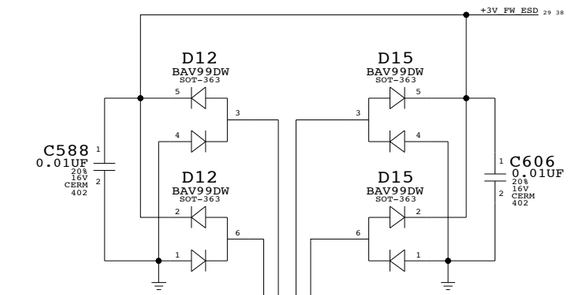
PORT POWER SWITCH



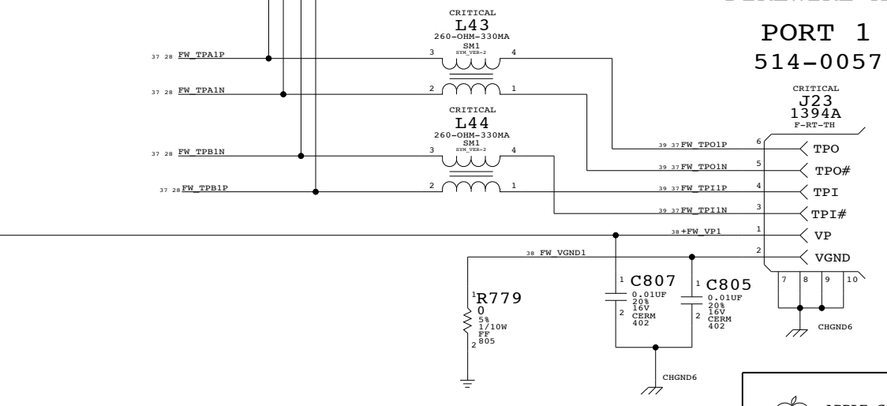


PORT 0
514S0059
FIREWIRE B - BILINGUAL

CLEAR OUT ALL PLANES UNDER TRANSFORMERS



CLEAR OUT ALL PLANES UNDER TRANSFORMERS



FIREWIRE A

PORT 1
514-0057

AREF NEEDS TO BE ISOLATED FROM ALL LOCAL GROUNDS PER 1394B SPEC

SO WHEN A BILINGUAL DEVICE IS PLUGGED TO BETA-ONLY DEVICE, THERE'S NO DC PATH BETWEEN THEM (TO AVOID GROUND OFFSET ISSUE)

BREF SHOULD BE HARD CONNECTED TO LOGIC GROUND FOR SPEED SIGNALING AND CONNECTION DETECTION CURRENTS PER 1394B V1.33

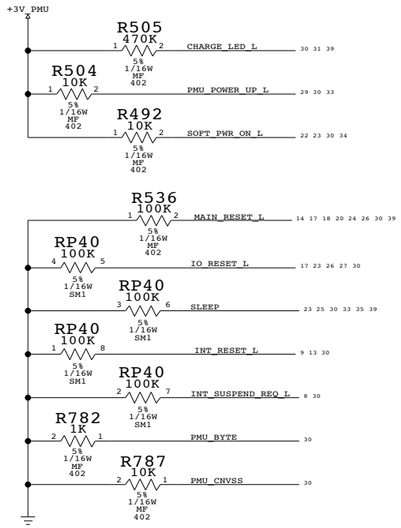
ENABLES PORT POWER WHEN MACHINE IS RUNNING OR WHEN ASLEEP ON AC

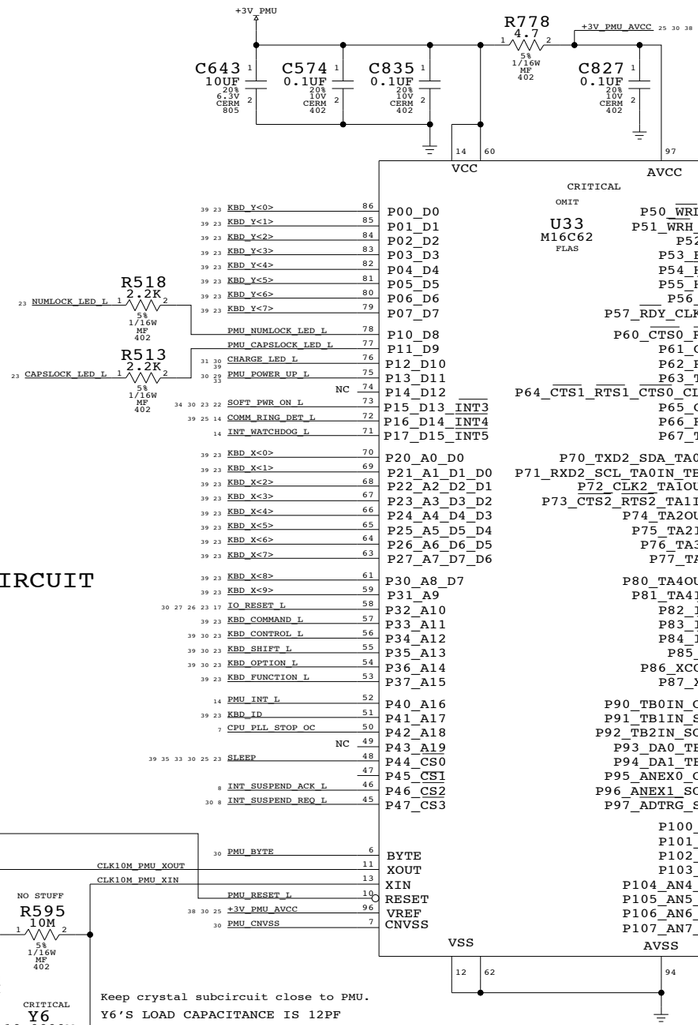
STATE	PMU_POWER_UP_L	POWER_UP	DCDC_EN	AC_IN	LTC4210_ON
SHUTDOWN (AC)	1	0	0	1	OFF
SLEEP (AC)	1	0	1	1	ON
RUN (AC)	0	1	1	1	ON
SHUTDOWN (BATT)	1	0	0	0	OFF
SLEEP (BATT)	1	0	1	0	OFF (PULL-DOWN RESISTOR)
RUN (BATT)	0	1	1	0	ON
	2.99V	+3V_PMU	+4_6V_BU	+3V_PMU	

FIREWIRE PORTS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6459	A
SCALE: NONE	SHT 29 OF 44	





CPU VCORE_HI_OC/PMU_AP should have a pulldown for coming out of reset. MLB will have a pull-up to +3V_MAIN or +3V_SLEEP, which will act as our pulldown since both are off during PMU reset.

(PMU_AP)

44	CPU_VCORE_HI_OC	7 34
43	INT_RESET_L	9 13 30
42	MAIN_RESET_L	14 17 18 20 24 26 30 39
41	NC	
40	PMU_INT_NMI	14
39	PMU_EPM	30
38	INT_PU_RESET_L	13 25 30
37	PMU_CPU_HRESET_L	23
36	PMU_ACK_L	14
35	PMU_CLK	14
34	PMU_FROM_INT	14
33	PMU_TO_INT	14
32	PMU_REQ_L	14
31	PMU_LID_CLOSED_L	23 30
30	PMU_RESET_BUTTON_L	25 30
29	PMU_NMI_BUTTON_L	25 30
28	TPAD_RXD	23 30
27	TPAD_TXD	23 30
26	SYSTEM_CLK_EN	14
25	CPU_CLK_EN	8
24	PMU_CHARGE_V	31
23	PMU_CHRG_BATT_0	31
22	NC (CHARGE_I)	
21	NC	
20	PMU_SLEEP_LED_L	23
19	CPU_SMI_L	5
18	POWER_VALID	30
17	PMU_PME_L	14 26 30
16	INT_PEND_PROC_INT	14
15	PMU_NMI_L	30
9		
8		
5	PMU_BATT0_DET_L	
4	PMU_BATT1_DET_L_PU	30
3	NC	
2	NC	
1	INT_PROC_SLEEP_REQ_L	14
100	PMU_POWERUP_OK	30
99	NC	
98	PMU_OOPS	30
95	THERM_L_OC	25
93	PMU_AC_IN	
92	PMU_AC_DET	30
91	NC	
90	PMU_I2C_CLK	30
89	PMU_I2C_DATA	30
88	PMU_SMB_CLK	30 31
87	PMU_SMB_DATA	30 31

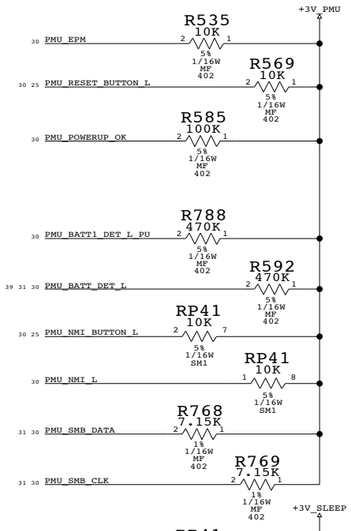
Keep crystal subcircuit close to PMU.

CLK32K_PMU_XOUT
CLK32K_PMU_XIN

R593 1K 5% 1/16W MF 402 PMU_BATT_DET_L 30 31 39
R572 1K 5% 1/16W MF 402 AC_IN 27 29 31

NO STUFF R786 10M 5% 1/16W MF 402
R785 0 5% 1/16W MF 402
CRITICAL Y7 SM-1 32.768K
C832 12PF 5% 50V CERM 402
C831 12PF 5% 50V CERM 402
CLK32K_PMU_XOUT_UF

Y7'S LOAD CAPACITANCE IS 12.5PF

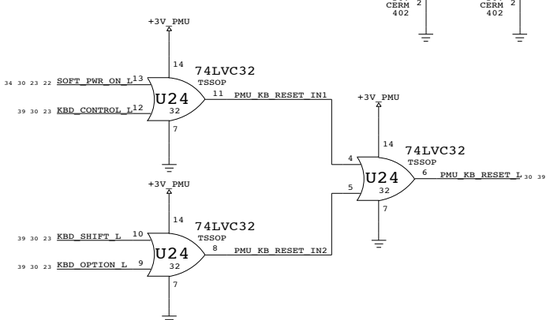


UNDERVOLTAGE RESET CIRCUIT

Keep crystal subcircuit close to PMU.
Y6'S LOAD CAPACITANCE IS 12PF

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0704	197S0041		Y6	ALT CRYSTAL SIZE
197S0604	197S0041		Y6	ALT FOR SIWARD

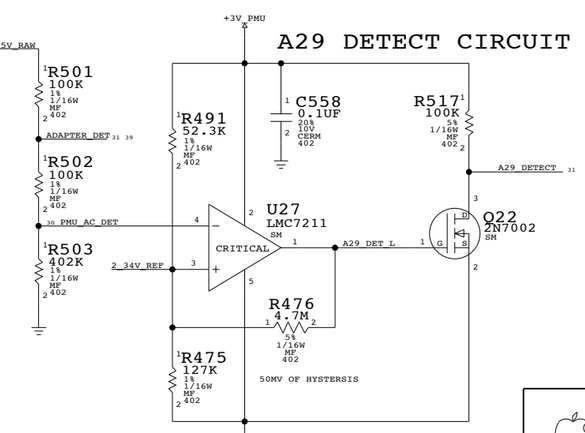
PMU KEYBOARD RESET CIRCUIT



Q11 ADAPTER DETECTION SCHEME

CASE	ADAPTER	PIN VOLT	ID VOLT RANGE	SYSTEM STATUS
1	Q11 (65W)	2.007V- 2.066V	1.65V- 2.31V	RECOGNIZES AS Q11 FULL FUNCTIONS
2	A29 (45W)	2.558V- 2.661V	2.31V- 2.97V	RECOGNIZES AS A29 LIMITED FUNCTIONS
3	AIRLINE	0.589V- 0.663V	0.33V- 0.99V	FULL FUNCTIONS NO BATTERY CHARGING
4	HOOPER	3.19V- 3.28V	2.97V- 3.30V	RECOGNIZES AS HOOPER LIMITED FUNCTIONS

A29 DETECT CIRCUIT



PMU

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6459	A
SCALE: NONE	SHT 30 OF 44	

DC POWER INPUT

(POWER JACK, ETC. ON SEPARATE BOARD)

CRITICAL

J18
87438-0833
M-RT-SM

CHARGE_LED_L
+ADAPTER
ADAPTER_DET

NO STUFF
C757 0.1UF 20% 50V CERM 805

PLACE CLOSE TO DC INPUT

R396 20K 1% 1/16W MF 402

DC INRUSH LIMITER

+ADAPTER_SW
+ADAPTER_SENSE

Q13 SI4435DY SOI
Q16 SI4435DY SOI

R414 330K 5% 1/16W MF 402
C458 0.1UF 20% 50V CERM 805

AC_ENABLE_GATE
AC_ENABLE_L

R374 470K 5% 1/16W MF 402

BCKFD_PROT_GATE
BCKFD_PROT_EN_L

R474 47K 5% 1/16W MF 402
C592 0.1UF 20% 50V CERM 805
R499 68K 5% 1/16W MF 402

Q10 2N7002DW SOT-363
Q21 2N7002DW SOT-363

+3V_PMU

R395 102K 1% 1/16W MF 402
R364 102K 1% 1/16W MF 402
C468 0.01UF 20% 16V CERM 402
R363 10K 5% 1/16W MF 402

1V20_REF
U15 LMC7211 SM
CRITICAL
AC_IN
AC_DIV

R394 1M 5% 1/16W MF 402
AC_IN_L

R375 10K 1% 1/16W MF 402
R365 57.6K 1% 1/16W MF 402

Q10 2N7002DW SOT-363

R383 470K 5% 1/16W MF 402

GREATER THAN 13.5V DETECT

PLACE U23 NEXT TO R460

U23 SENSE VOLTAGE DROP ACROSS R460

C572 0.01UF 20% 50V CERM 603

U23 MAX4172 TSSOP
CRITICAL
RS+ RS- PG NC1 NC2 OUT GND

+24V_PBUS
MAX4172_OUT

R454 2.21K 0.1% 1/16W MF 603
C883 0.1UF 10% 50V X7R 603

R460 0.025 1% 1W MF 2512

IF A29 ADAPTER USED, ADJUST CURRENT SETTING

R488 4.7 5% 1/16W MF 402
R498 4.7 5% 1/16W MF 402

1772_CSSP
1772_CSSN

C578 0.47UF 20% 50V CERM 1206
C579 0.47UF 20% 50V CERM 1206

1MSEC INTEGRATION TIME

R742 1K 1% 1/16W MF 402
C771 0.1UF 20% 10V CERM 402

IAC_RC_COMP

+3V_PMU

R747 42.2K 0.1% 1/16W FF 603
C772 0.1UF 20% 10V CERM 402

PLACE R358 CLOSE TO LTC1625
ROUTE LTC1625_ITH CAREFULLY

U50 LMC7111 SOT23-5
CRITICAL

IAC_FB
LTC1625_ITH

DP4 BAS16TW SOT-363
R358 150 1% 1/16W MF 402
1625_COMP

R466 10K 1% 1/16W MF 402

ADAPTER_I_REG
CURRENT_THRESHOLD

R738 42.2K 0.1% 1/16W FF 603
R734 82.5K 0.1% 1/16W FF 603

A29_CURRENT_ADJ

R739 51.1K 0.1% 1/16W FF 603
IF ADAPTER IS OVER 18V, ADJUST CURRENT SETTING

R748 100K 5% 1/16W MF 402

OVER_18V_ADJ

Q20 2N7002DW SOT-363
Q20 2N7002DW SOT-363
C775 1UF 20% 10V CERM 603

A29_DETECT
AC_GTR_18V

Q65 2N7002DW SOT-363
1772_ACOK_L

BATTERY SWITCH-OVER CIRCUIT

+BATT

F4 5AMP-125V SM-2
F3 5AMP-125V SM-2

+24V_PBUS
+PBUS
+BATT_24V_FUSE
+BATT_14V_FUSE

CRITICAL
Q24 SI4435DY SOI
Q76 SUD45P03 TO-252

R490 47K 5% 1/16W MF 402
R746 47K 5% 1/16W MF 402

BATT_24V_GATE
BATT_14V_GATE

R512 10K 5% 1/16W MF 402
R744 10K 5% 1/16W MF 402

DP4 BAS16TW SOT-363
BATT_24PBUS_EN
BATT_14PBUS_EN

Q21 2N7002DW SOT-363

AC_IN_L
DP4 BAS16TW SOT-363
R489 158K 1% 1/16W MF 402
AC_IN_L_RC
C593 10UF 20% 6.3V CERM 805

WHEN AC IS IN, P-CHANNEL FETS ARE QUICKLY (DIODE) TURNED OFF
WHEN AC IS NOT PLUGGED, P-CHANNEL FETS ARE ON
RC TIME IS 480K*10UF @ +3V_PMU

SWITCHER VOLTAGE CONTROL

PMU SELECTS BETWEEN TWO VOLTAGES

+3V_PMU

R567 27.4K 1% 1/16W MF 402
R558 10K 1% 1/16W MF 402
R548 10K 1% 1/16W MF 402
R560 4.12K 1% 1/16W MF 402
R565 48.7K 1% 1/16W MF 402

BATTV_HIGH
BATTV_LOW

R561 100K 5% 1/16W MF 402
Q27 2N7002DW SOT-363
R580 5.23K 1% 1/16W MF 402
Q27 2N7002DW SOT-363
PMU_CHARGE_V

SWITCHER CURRENT CONTROL

CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V
CHARGE THROTTLED BY LOW BATTERY VOLTAGE

OD OUTPUT LOW - WHEN AC GREATER THAN 18V

R566 1K 1% 1/16W MF 402
R542 1K 1% 1/16W MF 402

BATT_LOW_L

Q29 2N7002DW SOT-363
Q29 2N7002DW SOT-363

R526 1K 1% 1/16W MF 402
C622 0.01UF 20% 16V CERM 402
C616 0.01UF 20% 16V CERM 402

1772_CCV_RC

R497 1K 1% 1/16W MF 402
C621 0.1UF 20% 10V CERM 402

1772_REF

C630 1UF 20% 10V CERM 603

R487 10K 1% 1/16W MF 402
R473 4.12K 1% 1/16W MF 402

1772_CLS

U31 MAX1772 QSOP
CRITICAL

CSSP CSSN DCIN CELLS ACIN LDO ACOK DLOV RFIN BST VCTL DHI ICTL LX ICHG DLO IINP PGND CCV CSIP CCI CSIN CCS BATT
REF = 4.096V
REF CLS GND

1772_DCIN
1772_ACIN
1772_ACOK_L
(+3V_PMU)
1772_VCTL
1772_ICTL
1772_ICHG
1772_IINP
1772_CCV
1772_CCI
1772_CCS
1772_CELLS
1772_DLOV
1772_BST
1772_DHI
1772_LX
1772_DLO
(GND)
1772_CSIP
1772_CSIN

C652 1UF 20% 10V CERM 603
C817 0.1UF 20% 25V CERM 603
C802 0.1UF 20% 25V CERM 603

R559 100K 5% 1/16W MF 402

NO STUFF
C906 0.0022UF 10% 50V CERM 402

XW19 SM

R571 33 5% 1/8W FF 1206
D10 1N914 SOT23
1772_BST_ESR

R549 100K 5% 1/16W MF 402
C624 0.1UF 20% 25V CERM 603

R774 4.7 5% 1/16W MF 603
C608 0.1UF 20% 50V CERM 805

+24V_PBUS

CRITICAL
Q63 IRF7805 SM

C547 2.2UF 20% 50V CERM 1812
C562 2.2UF 20% 50V CERM 1812
C563 2.2UF 20% 50V CERM 1812
C557 2.2UF 20% 50V CERM 1812
C564 2.2UF 20% 50V CERM 1812

CRITICAL
Q64 IRF7811W SO-8

L42 10uH SM1
D30 MBRS140T3 SM

+BATT_RSNS
R763 0.05 1% 1W MF 2512

+BATT_24V_FUSE

C619 4.7UF 20% 25V CERM 1206
C632 4.7UF 20% 25V CERM 1206
C617 4.7UF 20% 25V CERM 1206
C824 33UF 20% 25V ELEC SM1

R543 1 5% 1/16W MF 603
R511 1 5% 1/16W MF 603

C631 4.7UF 20% 25V CERM 1206
C633 4.7UF 20% 25V CERM 1206
C618 4.7UF 20% 25V CERM 1206

R754 100K 1% 1/16W MF 402
D9 1N914 SOT23
C600 1UF 20% 50V CERM1 1210
R755 12.7K 1% 1/16W MF 402

R578 100K 5% 1/16W MF 402
CHARGE_DISABLE
Q30 2N7002DW SOT-363
Q30 2N7002DW SOT-363
PMU_CHRG_BATT_0

+3V_PMU

C615 0.1UF 20% 10V CERM 402

U38 LMC7211 SM
CRITICAL
BATT_LOW

R588 100K 1% 1/16W MF 402
R579 499K 1% 1/16W MF 402

BATT_DIV
1V65_REF

R599 100K 1% 1/16W MF 402
R570 100K 1% 1/16W MF 402
C658 0.047uF 10% 16V CERM 402

R749 6.34K 1% 1/16W MF 402

A29_CLS_ADJ

Q65 2N7002DW SOT-363
A29_DETECT

$V_{BATT} = CELLS \times (4.096 + (0.4096 * V_{VCTL} / V_{REFIN}))$

For 4.15V cells, VCTL = 0.123 REFIN

For 4.20V cells, VCTL = 0.245 REFIN

$I_{CHG} = (0.2048/R_{62}) * (V_{ICTL} / V_{REFIN})$

+BATT_VSNS

BATTERY CONNECTOR

CRITICAL
J25
87438-0833
M-RT-SM

+BATT_POS
(BATT_IN_PD)
BATT_CLK
BATT_DATA
PMU_BATT_DET_L
BATT_NEG

L9 FERR-EMI-100-OHM SM
L53 FERR-50-OHM SM
L10 FERR-EMI-100-OHM SM
L8 FERR-EMI-100-OHM SM
L12 FERR-50-OHM SM

PMU_SMB_CLK
PMU_SMB_DATA

BATTERY CHARGER

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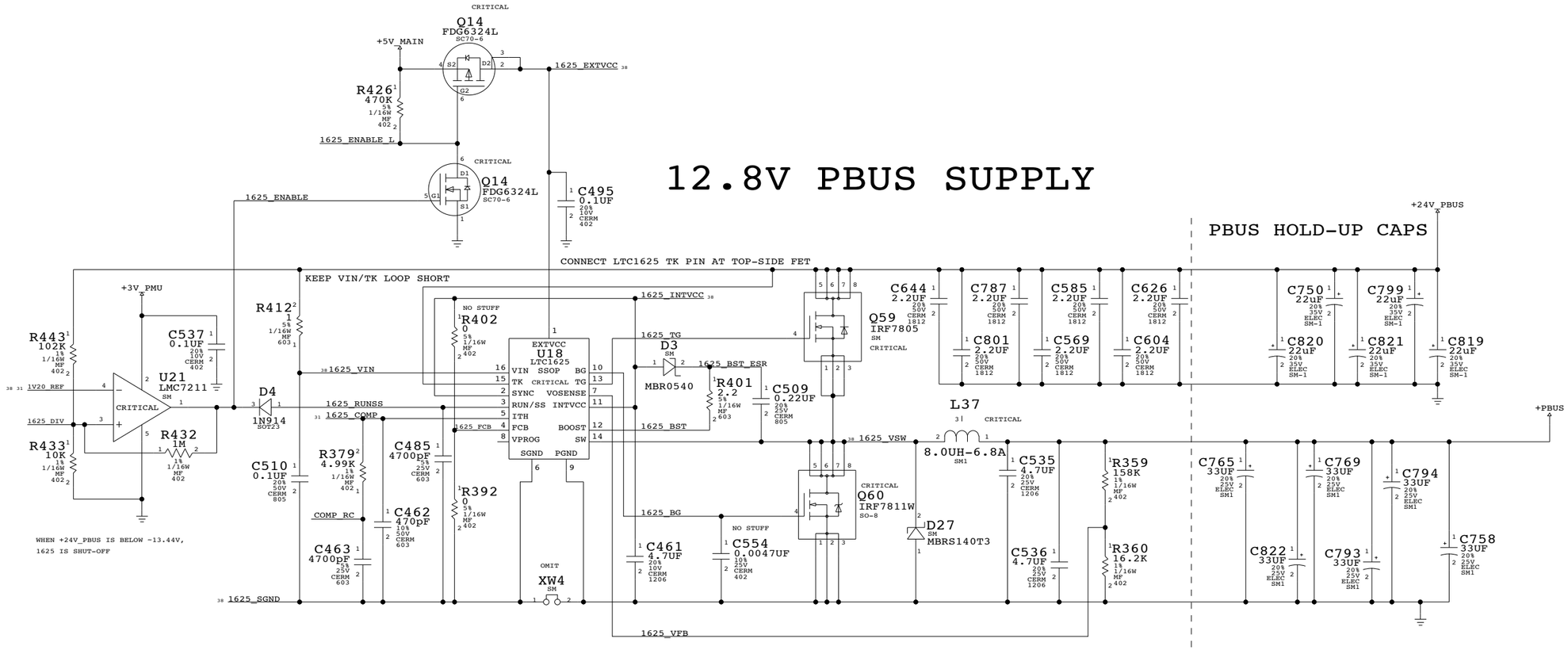
APPLE COMPUTER INC.

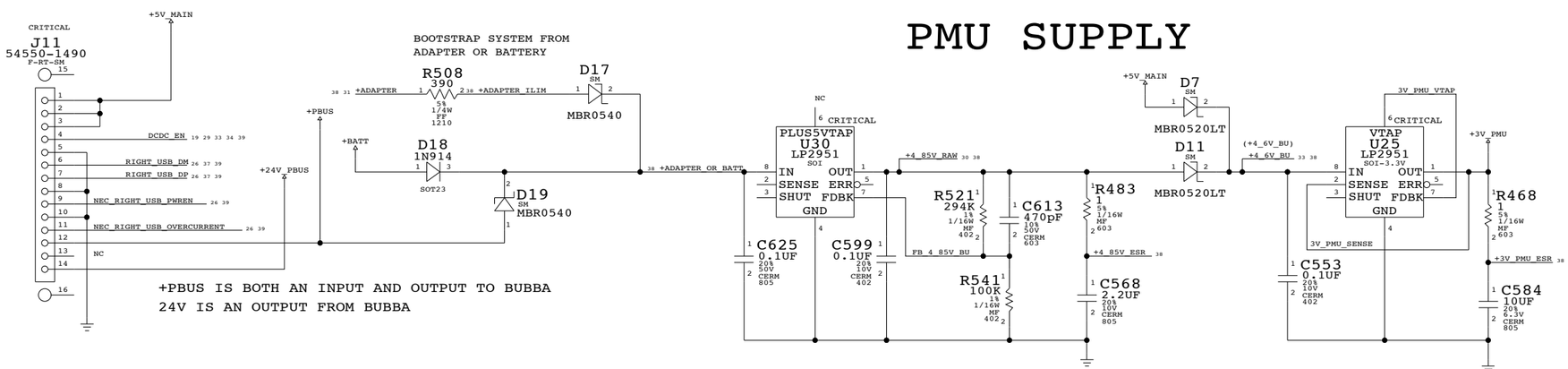
SIZE	DRAWING NUMBER	REV.
D	051-6459	A
SCALE: NONE	SHT 31 OF 44	

12.8V PBUS SUPPLY



BACKUP BATTERY / USB CONNECTOR

PMU SUPPLY

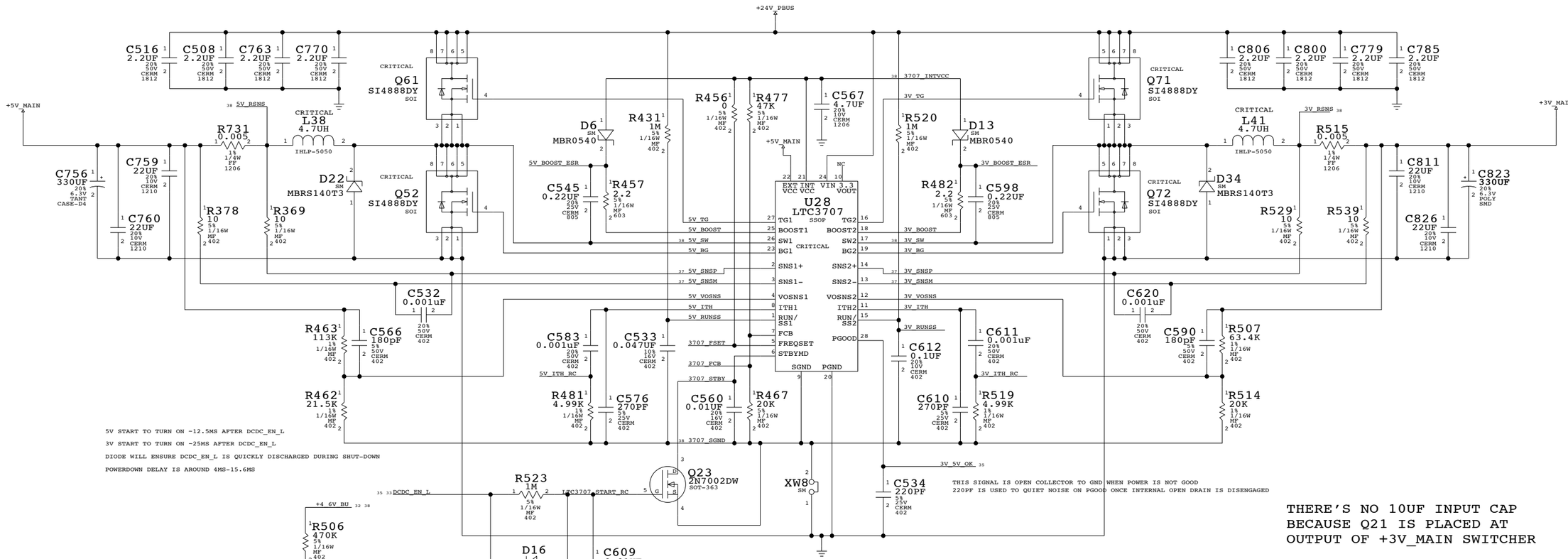


12.8V REGULATOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6459	A
SCALE: NONE	SHT 32 OF 44	

3.3V/5V MAIN SUPPLY



3.3V/5V REGULATOR

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D	051-6459	A
SCALE: NONE	SHT 33 OF 44	

VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage
(approx. 7ms delay)

1.175V -> 1.025V 1.30V -> 1.10V

SEL = 0; Y1=A1
SEL = 1; Y1=B1

Keep trace fat (40-100 mils) and short!!

MAX1717 VID CAN TAKE 3.3V TO 5.5V INPUTS

Connect MAX1717 GND pin 13 to GND at bottom-side FET

Keep trace fat and short!!

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V, HENCE VOFFSET = 2.0V * (R1/(R1+R2)) AND VCORE = VDAC + VOFFSET.

NOTE: R310 (R2) NO STUFFED FOR NO OFFSET CASE

ROUTE AS DIFFERENTIAL PAIR

PLACE THIS SHORT AT PIN OF 1000uF CAP CLOSEST TO CPU

OUTPUT VOLTAGE

V_{DAC} D4=0	V_{DAC} D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	A/B_ = Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1

If all pull-ups are >=100K and all pull-downs are <=1K, $V_A = V_B$.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S3013	1	RESISTOR	R321	?	1_30_VCORE
114S4993	1	RESISTOR	R321	?	1_32_VCORE

FMAX CONNECTOR

CRITICAL
NO STUFF
J5
M-ST-SM-52465-1217

NC (RFU)

VCORE SUPPLY

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SCALE: NONE	SHT 34 OF 44	

1.5V/2.5V SWITCHER

+1_5V_SLEEP LOADS

1) AGP I/O - IF USING D3COLD
2) MAXBUS I/O - IF 1.5V INTERFACE

+1_5V_MAIN LOADS

1) INTREPID CORE
2) AGP I/O IF USING D3HOT

+2_5V_MAIN LOADS

1) MAP31 - FBCORE/FBIO IF USING D3HOT
2) GIGABIT ETHERNET - AVDDL
3) DDR SODIMMS - CORE/IO
4) DDR MUXES
5) CLOCK SLEWING I/O
6) PCI1510 CORE

+2_5V_SLEEP LOADS

1) FBCORE/FBIO IF USING D3COLD
2) INTREPID MEMORY I/O

THERE'S 100K PULL-UP ON PG 31 ALREADY

DIODE PROVIDE PROVIDE QUICK SHUT-DOWN
POWER DOWN DELAY 1.5MS TO 3.5MS

CHANGE R424 BACK TO 10K, 1%, AND STUFF 5.11K FOR 1.5V OPERATION
CONNECTING 1_5V_FB TO GND, FORCES 1.8V OUTPUT

1.8V SWITCHER

+1_8V_MAIN LOADS

1) INTREPID PLLS

+1_8V_SLEEP LOADS

1) MPC7450 - MAXBUS I/O - IF 1.8V INTERFACE
2) CPU JTAG & MaxBus Pull-ups
3) CPU PLL Config Straps
4) OPTIONAL VIDEO MEMORY (M10 PRO ONLY)

1.5V/1.8V/2.5V SUPPLIES

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6459	A
SCALE: NONE	SHT 35 OF 44	

DIGITAL SIGNALS

GROUP	SIG_NAME		MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
MAXBUS	CPU_AACK_L				250.0000	10_MIL_SPACING			5 8
	CPU_ADDR<0..31>		5		250			83_MHZ	5 8
	CPU_ARTRY_L				250.0000	10_MIL_SPACING			5 8
	CPU_BG_L				250.0000	10_MIL_SPACING			5 8
	CPU_BR_L				250.0000	10_MIL_SPACING			5 8
	CPU_CI_L		5		250.0000				5 8
	CPU_DATA<0..31>		5		250			83_MHZ	6 8
	CPU_DATA<32..63>		5		250			83_MHZ	6 8
	CPU_DBG_L		5		250.0000	10_MIL_SPACING			5 8
	CPU_DTI<0..2>		5		250				5 8
	CPU_DRDY_L_UF					10_MIL_SPACING			
	CPU_DRDY_L				250.0000	10_MIL_SPACING			5 8
	CPU_GBL_L		5		250.0000				5 8
	CPU_HIT_L				250.0000	10_MIL_SPACING			5 8
	CPU_QACK_L		5		250.0000	10_MIL_SPACING			5 8
	CPU_QREQ_L				250.0000	10_MIL_SPACING			5 8
	CPU_TA_L				250.0000	10_MIL_SPACING			5 8
	CPU_TBST_L		5		250.0000	10_MIL_SPACING			5 8
	CPU_TEA_L				250.0000				5 8
	CPU_TS_L				250.0000	10_MIL_SPACING			5 8
	CPU_TSIZ<0..2>		5		250				5 8
	CPU_TT<0...4>		5		250				5 8
	CPU_WT_L		5		250.0000				5 8
GROUP 0	MEM_DATA<7..0>		4		200			167_MHZ	9 10
	RAM_DATA_A<7..0>		4		200			167_MHZ	10 11
	RAM_DATA_B<7..0>		4		200			167_MHZ	10 11
	MEM_DQS<0>	TOTAL LENGTH CONTROLLED BY SPREADSHEET			200				9 10
	RAM_DQS_A<0>		4		200				10 11
	RAM_DQS_B<0>		4		200				10 11
	MEM_DQM<0>		4		200				9 10
	RAM_DQM_A<0>		4		200				10 11
	RAM_DQM_B<0>		4		200				10 11
GROUP 1	MEM_DATA<15..8>		4		200			167_MHZ	9 10
	RAM_DATA_A<15..8>		4		200			167_MHZ	10 11
	RAM_DATA_B<15..8>		4		200			167_MHZ	10 11
	MEM_DQS<1>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200				9 10
	RAM_DQS_A<1>		4		200				10 11
	RAM_DQS_B<1>		4		200				10 11
	MEM_DQM<1>				200				9 10
	RAM_DQM_A<1>		4		200				10 11
	RAM_DQM_B<1>		4		200				10 11
GROUP 2/3	MEM_DATA<31..16>		4		200			167_MHZ	9 10
	RAM_DATA_A<31..16>		4		200			167_MHZ	10 11
	RAM_DATA_B<31..16>		4		200			167_MHZ	10 11
	MEM_DQS<3..2>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200			167_MHZ	9 10
DDR RAM	RAM_DQS_A<3..2>		4		200			167_MHZ	10 11
	RAM_DQS_B<3..2>		4		200			167_MHZ	10 11
	MEM_DQM<3..2>		4		200			167_MHZ	9 10
	RAM_DQM_A<3..2>		4		200			167_MHZ	10 11
	RAM_DQM_B<3..2>		4		200			167_MHZ	10 11
GROUP 4/5	MEM_DATA<47..32>		4		200			167_MHZ	9 10
	RAM_DATA_A<47..32>		4		200			167_MHZ	10 11
	RAM_DATA_B<47..32>		4		200			167_MHZ	10 11
	MEM_DQS<5..4>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200			167_MHZ	9 10
	RAM_DQS_A<5..4>		4		200			167_MHZ	10 11
	RAM_DQS_B<5..4>		4		200			167_MHZ	10 11
	MEM_DQM<5..4>		4		200			167_MHZ	9 10
	RAM_DQM_A<5..4>		4		200			167_MHZ	10 11
	RAM_DQM_B<5..4>		4		200			167_MHZ	10 11
GROUP 6	MEM_DATA<55..48>		4		200			167_MHZ	9 10
	RAM_DATA_A<55..48>		4		200			167_MHZ	10 11
	RAM_DATA_B<55..48>		4		200			167_MHZ	10 11
	MEM_DQS<6>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200				9 10
	RAM_DQS_A<6>				200				10 11
	RAM_DQS_B<6>		4		200				10 11
	MEM_DQM<6>				200				9 10
	RAM_DQM_A<6>		4		200				10 11
	RAM_DQM_B<6>		4		200				10 11
GROUP 7	MEM_DATA<63..56>		4		200			167_MHZ	9 10
	RAM_DATA_A<63..56>		4		200			167_MHZ	10 11
	RAM_DATA_B<63..56>		4		200			167_MHZ	10 11
	MEM_DQS<7>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200				9 10
	RAM_DQS_A<7>				200				10 11
	RAM_DQS_B<7>				200				10 11
	MEM_DQM<7>		4		200				9 10
	RAM_DQM_A<7>		4		200				10 11
	RAM_DQM_B<7>		4		200				10 11
ADDR	MEM_ADDR<12..0>		4					83_MHZ	9
	RAM_ADDR<12..0>		6		200				9 11
CONTROL	MEM_BA<1..0>		4						9
	RAM_BA<1..0>		6		200				9 11
	MEM_CS_L<3..0>		4						9
	RAM_CS_L<3..0>		6		200				9 11
	MEM_CKE<3..0>		4						9
	RAM_CKE<3..0>		6		200				9 11
	MEM_RAS_L		4						9
	RAM_RAS_L				200.0000				9 11
	MEM_CAS_L		4						9
	RAM_CAS_L				200.0000				9 11
	MEM_WE_L		4						9
	RAM_WE_L				200.0000				9 11
	MEM_MUXSEL_H<1..0>		3						9 10
	MEM_MUXSEL_L<1..0>		3						9 10
	RAM_MUXSEL_H		5						10
	RAM_MUXSEL_L		5						10

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME			MAX VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM	
INTREPID CLOCKS	SYSCLK_CPU_UF						10_MIL_SPACING		8
	SYSCLK_CPU			4		200.0000	10_MIL_SPACING		5 8
	INT_CPUFB_OUT			3			10_MIL_SPACING		8
	INT_CPUFB_OUT_SHORT			3			10_MIL_SPACING		8
	INT_CPUFB_OUT_NORM			3			10_MIL_SPACING		8
	INT_CPUFB_IN_NORM			3			10_MIL_SPACING		8
	INT_CPUFB_LONG			3			10_MIL_SPACING		8
	INT_CPUFB_IN					200.0000	10_MIL_SPACING		8
	SYSCLK_DDRCLK_A0_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_A0_L_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_A1_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_A1_L_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_B0_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_B0_L_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_B1_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_B1_L_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_A0	DDRCLK_A0		3		200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_A0_L	DDRCLK_A0				200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_A1	DDRCLK_A1		3		200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_A1_L	DDRCLK_A1				200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_B0	DDRCLK_B0		3		200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_B0_L	DDRCLK_B0		3		200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_B1	DDRCLK_B1		3		200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_B1_L	DDRCLK_B1		3		200.0000	10_MIL_SPACING		9 11
	INT_REF_CLK_OUT			3		200.0000	10_MIL_SPACING		14
	INT_REF_CLK_IN					200.0000	10_MIL_SPACING		14
	CLK66M_GPU_AGP_UF					200.0000	10_MIL_SPACING		12
	CLK66M_GPU_AGP			4		200.0000	10_MIL_SPACING		12 18
	INT_AGP_FB_OUT					200.0000	10_MIL_SPACING		12
	INT_AGP_FB_IN			4		200.0000	10_MIL_SPACING		12
	CLK33M_CBUS_UF					200.0000	10_MIL_SPACING		12
	CLK33M_CBUS	SHOULD BE AT MOST 4 VIAS FOR CLK		6		200.0000	10_MIL_SPACING		12 17
	CLK33M_AIRPORT_UF					200.0000	10_MIL_SPACING		12
	CLK33M_AIRPORT	SHOULD BE AT MOST 4 VIAS FOR CLK		6		200.0000	10_MIL_SPACING		12 24 39
	CLK33M_USB2_UF					200.0000	10_MIL_SPACING		12
	CLK33M_USB2	SHOULD BE AT MOST 4 VIAS FOR CLK		6		200.0000	10_MIL_SPACING		12 26
	INT_PCI_FB_OUT					200.0000	10_MIL_SPACING		12
	INT_PCI_FB_IN			3		200.0000	10_MIL_SPACING		12
MAP31	GPU_CLK27M_OUT						10_MIL_SPACING		
	GPU_CLK27M_UF						10_MIL_SPACING		
	GPU_SSCLK_UF						10_MIL_SPACING		
	GPU_SSCLK_IN						10_MIL_SPACING		
	GPU_FBCLK0						10_MIL_SPACING		
	GPU_FBCLK0_L						10_MIL_SPACING		
	GPU_FBCLK1						10_MIL_SPACING		
	GPU_FBCLK1_L						10_MIL_SPACING		
	GPU_DVO_CLKP						10_MIL_SPACING		19 20
CRYSTALS	CLK27M_GPU_XOUT						10_MIL_SPACING		
	CLK27M_XTAL_IN						10_MIL_SPACING		
	CLK27M_GPU_XIN						10_MIL_SPACING		
	CLK18M_INT_XIN						10_MIL_SPACING		14
	CLK18M_INT_XOUT						10_MIL_SPACING		14
	CLK18M_XTAL_IN						10_MIL_SPACING		14
	CLK18M_INT_EXT						10_MIL_SPACING		14
	CLK25M_ENET_XIN						10_MIL_SPACING		27
	CLK25M_ENET_XOUT						10_MIL_SPACING		27
	NEC_XT1						10_MIL_SPACING		26
	NEC_XT2	THERE'S ANOTHER 280MIL LEG					10_MIL_SPACING		26
SOUND	SND_SCLK			7		200.0000	10_MIL_SPACING		14 25 39
	SND_CLKOUT					200.0000	10_MIL_SPACING		14 25 39
ETHERNET MARVELL	CLKENET_PHY_RX					200.0000			27
	CLKENET_LINK_RX			3		200.0000	10_MIL_SPACING		13 27
	CLKENET_PHY_GBE_REF					200.0000			27
	CLKENET_LINK_GBE_REF			3		200.0000	10_MIL_SPACING		13 27
	CLKENET_PHY_TX					200.0000			27
	CLKENET_LINK_TX			5		200.0000	10_MIL_SPACING		13 27
	CLKENET_LINK_GTX					200.0000			13
	CLKENET_PHY_GTX			3		200.0000	10_MIL_SPACING		13 27
FIREWIRE	CLKFW_PHY_PCLK					200.0000			28
	CLKFW_LINK_PCLK			3		200.0000	10_MIL_SPACING		13 28
	CLKFW_PHY_LCLK			3		200.0000	10_MIL_SPACING		13 28
	CLKFW_LINK_LCLK					200.0000			13
	FW_XI					200.0000	10_MIL_SPACING		28
	FW_OSC					200.0000	10_MIL_SPACING		28

SIGNAL CONSTRAINTS - PAGE 1

APPLE COMPUTER INC.

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D	051-6459	A
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Digital Signals (cont'd)

GROUP	SIG_NAME	DELAY_RULE	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
AGP	AGP_AD<15..0>		5	100				66 MHz	12 18
AGP BYTES 0-1	AGP_CBE<1..0>		5	100				66 MHz	12 18
	AGP_AD_STB<0>		4	100		8 MIL SPACING			12 18
	AGP_AD_STB_L<0>		4	100		8 MIL SPACING			12 18
AGP BYTES 2-3	AGP_AD<31..16>		5	100				66 MHz	12 18
	AGP_CBE<3..2>		5	100				66 MHz	12 18
	AGP_AD_STB<1>		4	100		8 MIL SPACING			12 18
	AGP_AD_STB_L<1>			100		8 MIL SPACING			12 18
AGP SIDEBAND	AGP_SBA<7..0>		5	100				66 MHz	12 18
	AGP_SB_STB			100.0000		8 MIL SPACING			12 18
	AGP_SB_STB_L		4	100.0000		8 MIL SPACING			12 18
AGP CONTROL	AGP_FRAME_L			250.0000					12 18
	AGP_IRDY_L			250.0000					12 18
	AGP_TRDY_L		6	250.0000					12 18
	AGP_DEVSEL_L			250.0000					12 18
	AGP_STOP_L		6	250.0000					12 18
	AGP_PAR		6	250.0000					12 18
	AGP_REQ_L			285.0000					12 18
	AGP_GNT_L			250.0000					12 18
	AGP_RBF_L			250.0000					12 18
DVO	GPU_DVOD<0..11>		5	250					19 20
	GPU_DVO_HSYNC								19 20
	GPU_DVO_VSYNC								19 20
PCI	PCI_AD<31..0>					MIN_DAISY_CHAIN		33 MHz	9 12 17 24 26 39
	PCI_CBE<3..0>					MIN_DAISY_CHAIN		33 MHz	12 17 24 26 39
	PCI_FRAME_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_IRDY_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_TRDY_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_DEVSEL_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_STOP_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_PAR					MIN_DAISY_CHAIN			12 17 24 26 39
ULTRA ATA-100	UIDE_DATA<15..8>			NEED TO MATCH DELAY TO 250	200			100 MHz	13 24
	UIDE_DATA<7>				200				13 24
	UIDE_DATA<6..0>				200			100 MHz	13 24
	UIDE_ADDR<2..0>				200			100 MHz	13 24
	UIDE_RST_L				200.0000				13 24
	UIDE_DIOW_L				200.0000				13 24
	UIDE_DIOR_L			10 MIL SPACING	200.0000				13 24
	UIDE_DMACK_L				200.0000				13 24
	UIDE_CS0_L				200.0000				13 24
	UIDE_CS1_L				200.0000				13 24
	UIDE_DMARQ				200.0000				13
	UIDE_IOCHRDY			10 MIL SPACING	200.0000				13 24
	UIDE_INTRQ				200.0000				13
	HD_DATA<15..0>		5	TOTAL UIDE+HD SKEW <500MIL	200			100 MHz	24
	HD_ADDR<2..0>		5		200			100 MHz	24
	HD_RESET_L		5		200.0000				24
	HD_DIOW_L		5		200.0000				24
	HD_DIOR_L		5	10 MIL SPACING	200.0000				24
	HD_DMACK_L		5		200.0000				24
	HD_CS0_L		5		200.0000				24
	HD_CS1_L		5		200.0000				24
	HD_DMARQ				200.0000				13 24
	HD_IOCHRDY		5	10 MIL SPACING	200.0000				24
	HD_INTRQ		5						13 24
EIDE INTREPID	EIDE_DATA<15..0>							33 MHZ	13 24
	EIDE_ADDR<2..0>							33 MHZ	13 24
	EIDE_CS0_L								13 24
	EIDE_CS1_L								13 24
	EIDE_RD_L								13 24
	EIDE_WR_L								13 24
	EIDE_IOCHRDY								13 24
	EIDE_INT								13 24
	EIDE_RST_L								13 24
	EIDE_DMACK_L								13 24
	EIDE_DMARQ								13 24
OPTICAL	EIDE_OPTICAL_DATA<15..0>							33 MHZ	24 39
	EIDE_OPTICAL_ADDR<2..0>							33 MHZ	24 39
	EIDE_OPTICAL_CS0_L								24 39
	EIDE_OPTICAL_CS1_L								24 39
	EIDE_OPTICAL_RD_L								24 39
	EIDE_OPTICAL_WR_L								24 39
	EIDE_OPTICAL_IOCHRDY								24 39
	EIDE_OPTICAL_INT								24 39
	EIDE_OPTICAL_RST_L								24 39
	EIDE_OPTICAL_DMAACK_L								24 39
	EIDE_OPTICAL_DMA_RQ								24 39
ETHERNET MII	ENET_LINK_RXD<7..0>		5						13 27
	ENET_RX_DV								13 27
	ENET_RX_ER								13 27
	ENET_PHY_TXD<7..0>		5						13 27
	ENET_LINK_TXD<7..0>								13
	ENET_PHY_TX_ER		5						13 27
	ENET_LINK_TX_ER								13
	ENET_PHY_TX_EN		5						13 27
	ENET_LINK_TX_EN								13
	ENET_MDIO								13 27
	ENET_MDC								13 27
	ENET_COL								13 27
	ENET_CRS								13 27
FIREWIRE MII	FW_LINK_DATA<7..0>		5						13 28
	FW_PHY_DATA<7..0>		5						28
	FW_LINK_CNTL<1..0>								13 28
	FW_PHY_CNTL<1..0>								28
	FW_LINK_LREQ								13
	FW_PHY_LREQ								13 28
	FW_PINT								13 28

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR		MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS	
ETHERNET	MDI_M<0>	ENET_MDI0					27
	MDI_P<0>	ENET_MDI0					27
	MDI_M<1>	ENET_MDI1		SPACING DELETED BECAUSE			27
	MDI_P<1>	ENET_MDI1		OF PHYSICAL CONSTRAINTS			27
	MDI_M<2>	ENET_MDI2		AROUND MARVELL PHY			27
	MDI_P<2>	ENET_MDI2					27
	MDI_M<3>	ENET_MDI3					27
	MDI_P<3>	ENET_MDI3					27
	RJ45_DN<0>	RJ45_DP0			10 MIL SPACING		27 39
	RJ45_DP<0>	RJ45_DP0			10 MIL SPACING		27 39
	RJ45_DN<1>	RJ45_DP1			10 MIL SPACING		27 39
	RJ45_DP<1>	RJ45_DP1			10 MIL SPACING		27 39
	RJ45_DN<2>	RJ45_DP2			10 MIL SPACING		27 39
	RJ45_DP<2>	RJ45_DP2			10 MIL SPACING		27 39
	RJ45_DN<3>	RJ45_DP3			10 MIL SPACING		27 39
	RJ45_DP<3>	RJ45_DP3			10 MIL SPACING		27 39
FIREWIRE	FW_TPA0N	FW_TPA0			MIN LINE WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPA0P	FW_TPA0			MIN LINE WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB0N	FW_TPB0			MIN LINE WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB0P	FW_TPB0			MIN LINE WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPI0N	FW_TPI0			MIN LINE WIDTH=3.4 10 MIL SPACING		
	FW_TPI0P	FW_TPI0			MIN LINE WIDTH=3.4 10 MIL SPACING		
	FW_TPO0N	FW_TPO0			MIN LINE WIDTH=3.4 10 MIL SPACING		
	FW_TPO0P	FW_TPO0			MIN LINE WIDTH=3.4 10 MIL SPACING		
	FW_TPA1N	FW_TPA1		500.0000	MIN LINE WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPA1P	FW_TPA1		500.0000	MIN LINE WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB1N	FW_TPB1		500.0000	MIN LINE WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB1P	FW_TPB1		500.0000	MIN LINE WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPI1N	FW_TPI1			MIN LINE WIDTH=3.4 10 MIL SPACING		29 39
	FW_TPI1P	FW_TPI1			MIN LINE WIDTH=3.4 10 MIL SPACING		29 39
	FW_TPO1N	FW_TPO1			MIN LINE WIDTH=3.4 10 MIL SPACING		29 39
	FW_TPO1P	FW_TPO1			MIN LINE WIDTH=3.4 10 MIL SPACING		29 39
LVDS LOWER	CLKLVDS_LN	CLKLVDS_L			10 MIL SPACING	4	19 22 39
	CLKLVDS_LP	CLKLVDS_L			10 MIL SPACING	4	19 22 39
	LVDS_L0N	LVDS_L0			10 MIL SPACING		19 22 39
	LVDS_L0P	LVDS_L0			10 MIL SPACING		19 22 39
	LVDS_L1N	LVDS_L1			10 MIL SPACING		19 22 39
	LVDS_L1P	LVDS_L1			10 MIL SPACING		19 22 39
	LVDS_L2N	LVDS_L2			10 MIL SPACING		19 22 39
	LVDS_L2P	LVDS_L2			10 MIL SPACING		19 22 39
UPPER	CLKLVDS_UN	CLKLVDS_U			10 MIL SPACING	4	19 22 39
	CLKLVDS_UP	CLKLVDS_U			10 MIL SPACING	4	19 22 39
	LVDS_U0N	LVDS_U0			10 MIL SPACING		19 22 39
	LVDS_U0P	LVDS_U0			10 MIL SPACING		19 22 39
	LVDS_U1N	LVDS_U1			10 MIL SPACING		19 22 39
	LVDS_U1P	LVDS_U1			10 MIL SPACING		19 22 39
	LVDS_U2N	LVDS_U2			10 MIL SPACING		19 22 39
	LVDS_U2P	LVDS_U2			10 MIL SPACING		19 22 39
TMDS	TMDS_CONN_CLKN	CLKCONN_TMDS			10 MIL SPACING	4	22 39
	TMDS_CONN_CLKP	CLKCONN_TMDS			10 MIL SPACING	4	22 39
	TMDS_CLKN	CLKTMDS			10 MIL SPACING	4	20 22
	TMDS_CLKP	CLKTMDS			10 MIL SPACING	4	20 22
	TMDS_DN<0>	TMDS_D0			10 MIL SPACING		20 22 39
	TMDS_DP<0>	TMDS_D0			10 MIL SPACING		20 22 39
	TMDS_DN<1>	TMDS_D1			10 MIL SPACING		20 22 39
	TMDS_DP<1>	TMDS_D1			10 MIL SPACING		20 22 39
	TMDS_DN<2>	TMDS_D2			10 MIL SPACING		20 22 39
	TMDS_DP<2>	TMDS_D2			10 MIL SPACING		20 22 39
USB	NEC_USB_DAM	NEC_USB_DA		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_DAP	NEC_USB_DA		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	USB_DEM	USB_DE			5 MIL SPACING		14
	USB_DEP	USB_DE			5 MIL SPACING		14
	NEC_USB_DBM	NEC_USB_DB		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_DBP	NEC_USB_DB		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	USB_DFM	USB_DF			5 MIL SPACING		14
	USB_DFP	USB_DF			5 MIL SPACING		14
	BT_USB_DM	BT_USB_D			5 MIL SPACING		14 24 39
	BT_USB_DP	BT_USB_D			5 MIL SPACING		14 24 39
	NEC_USB_RSDM1	NEC_USB_RSD1		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_RSDP1	NEC_USB_RSD1		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_RSDM2	NEC_USB_RSD2		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_RSDP2	NEC_USB_RSD2		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	MODEM_USB_DM	MODEM_USB_D			5 MIL SPACING		14 25 39
	MODEM_USB_DP	MODEM_USB_D			5 MIL SPACING		14 25 39
	LEFT_USB_DM	LEFT_USB		MIN_LINE_WIDTH=5	10 MIL SPACING		24 26 39
	LEFT_USB_DP	LEFT_USB		MIN_LINE_WIDTH=5	10 MIL SPACING		24 26 39
	RIGHT_USB_DM	RIGHT_USB		MIN_LINE_WIDTH=5	10 MIL SPACING		26 32 39
	RIGHT_USB_DP	RIGHT_USB		MIN_LINE_WIDTH=5	10 MIL SPACING		26 32 39
POWER SUPPLIES	1772_CSSN	1772_CSS					31
	1772_CSSP	1772_CSS					31
	1772_CSIN	1772_CSI					31
	1772_CSIP	1772_CSI					31
	3V_SNSM	3V_SNS					33
	3V_SNSP	3V_SNS					33
	5V_SNSM	5V_SNS					33
	5V_SNSP	5V_SNS					33
THERMOSTAT	THERM1_DM	THERM1					25
	THERM1_DP	THERM1					25
	THERM2_DM	THERM2					25
	THERM2_DP	THERM2					25
	THERM1_M_DM	THERM1_MATN					
	THERM1_M_DP	THERM1_MATN					
	THERM2_M_DM	THERM2_MATN					
	THERM2_M_DP	THERM2_MATN					
	THERM1_A_DM	THERM1_ALT					25
	THERM1_A_DP	THERM1_ALT					25
	THERM2_A_DM	THERM2_ALT					25
	THERM2_A_DP	THERM2_ALT					25

INTERNAL LAYER

ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.57OHM
ZDIFF = 99.80HM

FOR FIREWIRE

ER = 4.3 (DIELECTRIC CONSTANT)
W = 3.4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 53.37OHM
ZDIFF = 107.17OHM

INTERNAL LAYER (USB1.1/USB 2.0)

ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL(USB 1.1)/ 5MIL(USB 2.0) (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 5MIL (USB 1.1) (SEPERATION OF DIFF TRACES)
S = 10MIL (USB 2.0) (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.5OHM (USB 1.1)/ 46.2OHM (USB 2.0)
ZDIFF = 89.3OHM (USB 1.1)/ 89.4OHM (USB 2.0)

SIGNAL CONSTRAINTS - PAGE 2

APPLE COMPUTER INC.

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POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
MAIN/SLEEP	+24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+BATT	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	
	+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+2_5V_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	39
	+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	35
	+1_5V_SLEEP_VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	35
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31 32
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31 39
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31 39
	1772_DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	1772_LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	31
	1772_LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		31
	1772_DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		31
	1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10		31
PMU	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	+4_85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		30 32
	+4_6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10		32 33
	+4_85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		32
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		32
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		25 30
MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24 33
	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24
TRACKPAD	+5V_TPAD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=10		23 39
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		23 39
VIDEO	+12_8V_INV	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	22
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
KB LED	KBD_LED1_OUT	VOLTAGE=0V	MIN_LINE_WIDTH=10		23 39
	KBD_LED2_OUT	VOLTAGE=0V	MIN_LINE_WIDTH=10		23 39
FAN GND	FANL_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 39
	FANR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 39
SOUND	+5V_SOUND_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	SND_AGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=15	25

	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	GND	
I/O AREA	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND1	
	CHGND1				
INVERTER	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND2	
	CHGND2				
TRACKPAD	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND3	
	CHGND3				
LVDS	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND4	39
	CHGND4				
I/O AREA	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND5	
	CHGND5				
I/O AREA	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND6	
	CHGND6				
ENET_CTAP_CHGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12		27

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 34 39
	CPU_AVDD	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
DDR RAM	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 7 8 15 16 23 34
INTREPID PLLS	DDR_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		11
	+2_5V_INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	9 10 15 16
	+3V_INTREPID_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14
	+1_5V_INTREPID_PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	8 12 14
	+1_5V_INTREPID_PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5	14
	+1_5V_INTREPID_PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5	12
	+1_5V_INTREPID_PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	8
	+1_5V_INTREPID_PLL8	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
REFERENCE	INT_MEM_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		9
	INT_AGP_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		12 18
	INT_MEM_REF_H	VOLTAGE=0V	MIN_LINE_WIDTH=10		9
	UIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8		13
CARDBUS	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
ATI M10	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	18 19 39
	+GPU_MEM	VOLTAGE=2.5V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	18 21
	+3V_GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 18 19 21
	+3V_GPU_FLT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	21
	+1_5V_AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 15 16 18 19 21
	GPU_MEM_IO	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	GPU_MEM_IO_FLT	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+GPU_MEMCORE	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+1_8V_GPU	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18 19 20 21
	+2_5V_GPU_PNLIO	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_8V_ATI_PVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19 21
	+1_5V_AGP_GPU	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_5V_GPU_VDD15	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	+1_8V_GPU_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1331	+1_8V_GPU_VDDDI	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1332	GPU_VCORE_VDDCI	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	18
1333	+2_5V_GPU_A2VDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1334	+1_8V_GPU_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1335	+1_8V_GPU_PNLPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1336	+1_8V_GPU_PNLIO	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1337	+GPU_MCLK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1338	+1_8V_GPU_AVDDQ	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1341	+1_8V_GPU_MEMPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1340	+3V_ATI_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	18
1339	+3V_ATI_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	18
1342	+GPU_VDD15_UF	VOLTAGE=1.5V	MIN_LINE_WIDTH=20		19
1343	+2_5V_SLEEP_NECK1	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		19
1344	+3V_SLEEP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		21
1345	+1_5V_AGP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		19
1346	+1_8V_PVDD_NECK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10		19
1347	GPU_VCORE_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		19
1348	+GPU_VDD15_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		19
1351	+2_5V_SLEEP_NECK2	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		21
1349	+1_8V_SLEEP_NECK	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		21
1350	+1_5V_SLEEP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		21
1352	+2_5V_GPU	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
SILICON IMIAGE	+3V_SI_PLLVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	20
	+3V_SI_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	20
	+3V_SI_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	20
88E1111	+2_5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+2_5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
	+1_0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
	LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
	LM2594_IN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
FW	+3V_FW_ESD_ILIM	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+3V_FW_ESD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+FW_FUSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_PWR_OR	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28 29
	+FW_VP0	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_PWR_PORTA	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_VP1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+3V_FW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28 29
	+3V_FW_UF	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	28
	+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	FW_TPO0R	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29 39
USB 2.0	NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
INTREPID SSCG	+3V_CG_PLL_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	14
	+2_5V_CG_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	14

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	1625_VSW	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		32
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		32
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		32
	1V20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	31 32
LTC3707 5V SWITCHER	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	33
	5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
3V SWITCHER	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		33
MAX1715 2.5V SWITCHER	2_5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	35
	2_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	2_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	2_5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	2_5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
1.5V SWITCHER	1_5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8		35
	1_5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	35
	1_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	1_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	1_5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	1_5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
CONTROL	1_5V_ILIM		MIN_LINE_WIDTH=8		35
	2_5V_ILIM		MIN_LINE_WIDTH=8		35
	MAX1715_TON		MIN_LINE_WIDTH=8		35
	MAX1715_SKIP		MIN_LINE_WIDTH=8		35
	MAX1715_REF	VOLTAGE=2.0V	MIN_LINE_WIDTH=8		35
	MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	35
MAX1717	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=200	MIN_NECK_WIDTH=10	34
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	VCORE_ILIM		MIN_LINE_WIDTH=8		34
	VCORE_REF		MIN_LINE_WIDTH=8		34
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8		34
	VCORE_CC		MIN_LINE_WIDTH=8		34
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		34 39
	VCORE_TIME		MIN_LINE_WIDTH=8		34
	VCORE_VGATE		MIN_LINE_WIDTH=8		14 34
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30		34
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8		34
	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		34
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8		34
LTC1778	1778_VIN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	19
	1778_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	1778_BST_RC	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	1778_TG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_BG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	GPU_VCORE_SW	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	19
	1778_ION		MIN_LINE_WIDTH=8		19
	1778_ITH		MIN_LINE_WIDTH=8		19
	1778_ITH_RC		MIN_LINE_WIDTH=8		19
	1_5V_2_5V_OK		MIN_LINE_WIDTH=8		35
	1778_VFB		MIN_LINE_WIDTH=8		19 39
	1778_FCB		MIN_LINE_WIDTH=8		19
	1778_VRNG		MIN_LINE_WIDTH=8		19
LTC3411	LTC3411_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC3411_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	
	1_8V_SW	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	35
	1_8V_VFB		MIN_LINE_WIDTH=8		
	LTC3411_ITH_RC		MIN_LINE_WIDTH=8		
	LTC3411_ITH		MIN_LINE_WIDTH=8		
	LTC3411_SYNC		MIN_LINE_WIDTH=8		
	LTC3411_SHDN		MIN_LINE_WIDTH=8		
LTC1962 INT PLLS	LTC1962_INT_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	14
	LTC1962_L3_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_L3_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_1V5_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_1V5_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	

MIN_NECK_WIDTH REDUCED FOR TESTPOINTS

SIGNAL CONSTRAINTS - PAGE 3

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6459	A
SCALE: NONE	SHT 38 OF 44	

FUNCTIONAL TEST POINTS

FUNC_TEST=YES JTAG_ASIC_TMS 13 27
FUNC_TEST=YES JTAG_ASIC_TDI 13
FUNC_TEST=YES JTAG_ASIC_TDO_TP 27
FUNC_TEST=YES JTAG_ASIC_TCK 13 27
FUNC_TEST=YES JTAG_ASIC_TRST_L 13 27
FUNC_TEST=YES CPU_CHKSTP_OUT_L 5
FUNC_TEST=YES CPU_SRESET_L 5
FUNC_TEST=YES CPU_HRESET_L 5 7 23
FUNC_TEST=YES JTAG_CPU_TMS 5 23
FUNC_TEST=YES JTAG_CPU_TDI 5 23
FUNC_TEST=YES JTAG_CPU_TDO_TP 5
FUNC_TEST=YES JTAG_CPU_TCK 5 23
FUNC_TEST=YES JTAG_CPU_TRST_L 5 23 39

FUNC_TEST=YES INT_I2C_CLK0 11 13 23
FUNC_TEST=YES INT_I2C_DATA0 11 13 23
FUNC_TEST=YES INT_I2C_CLK1 13 14 25
FUNC_TEST=YES INT_I2C_DATA1 13 14 25
FUNC_TEST=YES CBUS_DET_1_L 17
FUNC_TEST=YES CBUS_DET_2_L 17
FUNC_TEST=YES TMDS_DN<0> 20 22 37
FUNC_TEST=YES TMDS_DP<0> 20 22 37
FUNC_TEST=YES TMDS_DN<1> 20 22 37
FUNC_TEST=YES TMDS_DP<1> 20 22 37
FUNC_TEST=YES TMDS_DN<2> 20 22 37
FUNC_TEST=YES TMDS_DP<2> 20 22 37
FUNC_TEST=YES TMDS_CONN_CLKN 22 37

FUNC_TEST=YES TMDS_CONN_CLKP 22 37
FUNC_TEST=YES VGA_R 22
FUNC_TEST=YES VGA_G 22
FUNC_TEST=YES VGA_B 22
FUNC_TEST=YES VGA_VSYNC 22
FUNC_TEST=YES VGA_HSYNC 22
FUNC_TEST=YES DVI_DDC_CLK_UF 22
FUNC_TEST=YES DVI_DDC_DATA_UF 22
FUNC_TEST=YES DVI_HPD_UF 22
FUNC_TEST=YES LVDS_L0N 19 22 37
FUNC_TEST=YES LVDS_L0P 19 22 37
FUNC_TEST=YES LVDS_L1N 19 22 37
FUNC_TEST=YES LVDS_L1P 19 22 37
FUNC_TEST=YES LVDS_L2N 19 22 37
FUNC_TEST=YES LVDS_L2P 19 22 37
FUNC_TEST=YES CLKLVDS_LN 19 22 37
FUNC_TEST=YES CLKLVDS_LP 19 22 37
FUNC_TEST=YES LVDS_U0N 19 22 37
FUNC_TEST=YES LVDS_U0P 19 22 37
FUNC_TEST=YES LVDS_U1N 19 22 37
FUNC_TEST=YES LVDS_U1P 19 22 37
FUNC_TEST=YES LVDS_U2N 19 22 37
FUNC_TEST=YES LVDS_U2P 19 22 37
FUNC_TEST=YES CLKLVDS_UN 19 22 37
FUNC_TEST=YES CLKLVDS_UP 19 22 37
FUNC_TEST=YES LVDS_DDC_CLK 19 22
FUNC_TEST=YES LVDS_DDC_DATA 19 22
FUNC_TEST=YES BRIGHT_PWM 22
FUNC_TEST=YES TV_GND1 22 38
FUNC_TEST=YES TV_GND2 22 38

FUNC_TEST=YES TV_C 22
FUNC_TEST=YES TV_Y 22
FUNC_TEST=YES TV_COMP 22
FUNC_TEST=YES SND_TO_AUDIO 14 25
FUNC_TEST=YES SND_SYNC 14 25
FUNC_TEST=YES SND_CLKOUT 14 25 36

FUNC_TEST=YES INT_AUDIO_TO_SND 14 25
FUNC_TEST=YES SND_SCLK 14 25 36
FUNC_TEST=YES SND_HW_RESET_L 14 25
FUNC_TEST=YES SND_HP_SENSE_L 14 25
FUNC_TEST=YES SND_LIN_SENSE_L 14 25
FUNC_TEST=YES INT_I2C_DATA2 14 25
FUNC_TEST=YES INT_I2C_CLK2 14 25
FUNC_TEST=YES CHGND4 38
FUNC_TEST=YES SLEEP_LED 23 25

FUNC_TEST=YES BT_USB_DM 14 24 37
FUNC_TEST=YES BT_USB_DP 14 24 37
FUNC_TEST=YES MODEM_USB_DM 14 25 37
FUNC_TEST=YES MODEM_USB_DP 14 25 37
FUNC_TEST=YES PCI_AD<0> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<1> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<2> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<3> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<4> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<5> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<6> 9 12 17 24 26 37

FUNC_TEST=YES PCI_AD<7> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<8> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<9> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<10> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<11> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<12> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<13> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<14> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<15> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<16> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<17> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<18> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<19> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<20> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<21> 12 17 24 26 37
FUNC_TEST=YES PCI_AD<22> 12 17 24 26 37
FUNC_TEST=YES PCI_AD<23> 12 17 24 26 37
FUNC_TEST=YES PCI_AD<24> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<25> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<26> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<27> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<28> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<29> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<30> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<31> 9 12 17 24 26 37
FUNC_TEST=YES PCI_FRAME_L 12 17 24 26 37
FUNC_TEST=YES PCI_TRDY_L 12 17 24 26 37
FUNC_TEST=YES PCI_IRDY_L 12 17 24 26 37
FUNC_TEST=YES PCI_DEVSEL_L 12 17 24 26 37
FUNC_TEST=YES PCI_STOP_L 12 17 24 26 37

FUNC_TEST=YES PCI_PAR 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<0> 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<1> 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<2> 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<3> 12 17 24 26 37
FUNC_TEST=YES AIRPORT_PCI_REQ_L 12 24
FUNC_TEST=YES AIRPORT_PCI_GNT_L 12 24
FUNC_TEST=YES AIRPORT_PCI_INT_L 14 24
FUNC_TEST=YES EIDE_OPTICAL_DATA<0> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<1> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<2> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<3> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<4> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<5> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<6> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<7> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<8> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<9> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<10> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<11> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<12> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<13> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<14> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<15> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DMA_RQ 24 37
FUNC_TEST=YES EIDE_OPTICAL_RD_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_DMAACK_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_ADDR<0> 24 37
FUNC_TEST=YES EIDE_OPTICAL_ADDR<1> 24 37
FUNC_TEST=YES EIDE_OPTICAL_ADDR<2> 24 37
FUNC_TEST=YES SND_AMP_MUTE 25
FUNC_TEST=YES SND_HP_MUTE_INV 25

FUNC_TEST=YES EIDE_OPTICAL_CS0_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_CS1_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_RST_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_WR_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_IOCHRDY 24 37
FUNC_TEST=YES EIDE_OPTICAL_INT 24 37
FUNC_TEST=YES TPAD_F_TXD 23
FUNC_TEST=YES TPAD_F_RXD 23
FUNC_TEST=YES LID_CLOSED_L 23
FUNC_TEST=YES COMM_RESET_L 14 25
FUNC_TEST=YES COMM_SHUTDOWN 14 25
FUNC_TEST=YES COMM_RING_DET_L 14 25 30
FUNC_TEST=YES KBD_ID 23 30
FUNC_TEST=YES +5V_TPAD_SLEEP 23 38
FUNC_TEST=YES +3V_HALL_EFFECT 23 38
FUNC_TEST=YES KBD_CAPSLOCK_LED 23
FUNC_TEST=YES KBD_FUNCTION_L 23 30
FUNC_TEST=YES KBD_CONTROL_L 23 30
FUNC_TEST=YES KBD_COMMAND_L 23 30
FUNC_TEST=YES KBD_OPTION_L 23 30
FUNC_TEST=YES KBD_SHIFT_L 23 30
FUNC_TEST=YES KBD_X<0> 23 30
FUNC_TEST=YES KBD_X<1> 23 30
FUNC_TEST=YES KBD_X<2> 23 30
FUNC_TEST=YES KBD_X<3> 23 30
FUNC_TEST=YES KBD_X<4> 23 30
FUNC_TEST=YES KBD_X<5> 23 30
FUNC_TEST=YES KBD_X<6> 23 30
FUNC_TEST=YES KBD_X<7> 23 30
FUNC_TEST=YES KBD_X<8> 23 30
FUNC_TEST=YES SRCLK_TP 26
FUNC_TEST=YES SRMOD_TP 26
FUNC_TEST=YES TEB_TP 26
FUNC_TEST=YES TEST_TP 26

FUNC_TEST=YES KBD_X<9> 23 30
FUNC_TEST=YES KBD_Y<0> 23 30
FUNC_TEST=YES KBD_Y<1> 23 30
FUNC_TEST=YES KBD_Y<2> 23 30
FUNC_TEST=YES KBD_Y<3> 23 30
FUNC_TEST=YES KBD_Y<4> 23 30
FUNC_TEST=YES KBD_Y<5> 23 30
FUNC_TEST=YES KBD_Y<6> 23 30
FUNC_TEST=YES KBD_Y<7> 23 30
FUNC_TEST=YES KBD_NUMLOCK_LED 23
FUNC_TEST=YES +BATT_POS 31 38
FUNC_TEST=YES BATT_CLK 31
FUNC_TEST=YES BATT_DATA 31
FUNC_TEST=YES BATT_NEG 31 38
FUNC_TEST=YES PMU_BATT_DET_L 30 31
FUNC_TEST=YES FANR_GND 25 38
FUNC_TEST=YES FANL_GND 25 38
FUNC_TEST=YES FANL_TACH 25
T271 FUNC_TEST=YES FANR_PWM 25
T272 FUNC_TEST=YES FANL_PWM 25
FUNC_TEST=YES RJ45_DP<0> 27 37
FUNC_TEST=YES RJ45_DN<0> 27 37
FUNC_TEST=YES RJ45_DP<1> 27 37
FUNC_TEST=YES RJ45_DN<1> 27 37
FUNC_TEST=YES RJ45_DP<2> 27 37
FUNC_TEST=YES RJ45_DN<2> 27 37
FUNC_TEST=YES RJ45_DP<3> 27 37
FUNC_TEST=YES RJ45_DN<3> 27 37
FUNC_TEST=YES FW_TPOOR 29 38
T281 FUNC_TEST=YES VCORE_VID0
T282 FUNC_TEST=YES VCORE_VID1
T283 FUNC_TEST=YES VCORE_VID2
T284 FUNC_TEST=YES VCORE_VID3
T285 FUNC_TEST=YES VCORE_VID4

FUNC_TEST=YES FW_TPO1P 29 37
FUNC_TEST=YES FW_TPO1N 29 37
FUNC_TEST=YES FW_TPI1P 29 37
FUNC_TEST=YES FW_TPI1N 29 37
FUNC_TEST=YES CHARGE_LED_L 30 31
FUNC_TEST=YES ADAPTER_DET 30 31
FUNC_TEST=YES SUTRO_ALS_GAIN_SW 23 24
FUNC_TEST=YES SUTRO_ALS_OUT 23 24
FUNC_TEST=YES KBD_LED1_OUT 23 38
FUNC_TEST=YES KBD_LED2_OUT 23 38
FUNC_TEST=YES COMM_TXD_L 14 25
FUNC_TEST=YES COMM_TRXC 14 25
FUNC_TEST=YES COMM_GPIO_L 14 25
FUNC_TEST=YES COMM_DTR_L 14 25
FUNC_TEST=YES COMM_RTS_L 14 25
FUNC_TEST=YES COMM_RXD 14 25
FUNC_TEST=YES PMU_KB_RESET_L 30
FUNC_TEST=YES PWR_BUTTON_L 23 25
FUNC_TEST=YES +PBUS 38
FUNC_TEST=YES +24V_PBUS 38
FUNC_TEST=YES GPU_VCORE 18 19 38
FUNC_TEST=YES CPU_VCORE_SLEEP 5 34 38
FUNC_TEST=YES VCORE_FB 34 38
FUNC_TEST=YES +1_8V_MAIN 38
FUNC_TEST=YES +3V_PMU 38
FUNC_TEST=YES +5V_DDC_SLEEP 22 38
FUNC_TEST=YES +12_8V_INV 22 38
T286 FUNC_TEST=YES VCORE_MUX_EN 34

FUNC_TEST=YES +5V_INV_SW 22 38
FUNC_TEST=YES LEFT_USB_DM 24 26 37
FUNC_TEST=YES LEFT_USB_DP 24 26 37
FUNC_TEST=YES RIGHT_USB_DM 26 32 37
FUNC_TEST=YES RIGHT_USB_DP 26 32 37
FUNC_TEST=YES NEC_LEFT_USB_PWREN 24 26
FUNC_TEST=YES NEC_LEFT_USB_OVERCURRENT 24 26
FUNC_TEST=YES NEC_RIGHT_USB_PWREN 26 32
FUNC_TEST=YES NEC_RIGHT_USB_OVERCURRENT 26 32
FUNC_TEST=YES DCDC_EN 19 29 32 33 34
FUNC_TEST=YES BBANG_HRESET_L 23
FUNC_TEST=YES MAIN_RESET_L 14 17 18 20 24 26 30
FUNC_TEST=YES RF_DISABLE_L_SPN 24
FUNC_TEST=YES AIRPORT_CLKRUN_L 24
FUNC_TEST=YES ROM_RW_L 9 12 24
FUNC_TEST=YES ROM_ONBOARD_CS_L 9 24
FUNC_TEST=YES ROM_CS_L 9 12 24
FUNC_TEST=YES CLK33M_AIRPORT 12 24 36
FUNC_TEST=YES AIRPORT_IDSEL 24
FUNC_TEST=YES ROM_OE_L 9 12 24
T273 FUNC_TEST=YES INT_MOD_DTI 14 25
T274 FUNC_TEST=YES JTAG_CPU_TRST_L 5 23 39
T275 FUNC_TEST=YES MOD_BITCLK 14 25
T276 FUNC_TEST=YES MOD_CLKOUT 14 25
T277 FUNC_TEST=YES MOD_DTO 14 25
T278 FUNC_TEST=YES MOD_SYNC 14 25
T279 FUNC_TEST=YES SLEEP 23 25 30 33 35
T280 FUNC_TEST=YES 1778_VFB 19 38

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6459	A
SCALE: NONE	SHT 39 OF 44	

REVISION HISTORY

REV 0.01 - 03/06/2003

3/3
1) Initial check-in of Enterprise schematic after conversion to Concept 14.2

3/10
2) added 8 new 10uF vcore caps
3) added jumpers at 1.5V, 1.8V, 2.5V, 3.3V, 5V, and PBUS supply outputs
4) added 8 more 0.1uF vcore byapass caps

3/11
5) removed dedicated boot banger circuit (U5400,U5200,RP46,U9,U1000)
6) updated firewire to phy to rev A prt number
7) changed cpu PLL config to 1083/833
8) changed reset to U56 (clock slewing chip) to MAIN_RESET_L
9) changed C550 to 138S0536 to limit AVL
10) changed Vcore stuffing options to 1.4V/1.025V using analog mux to support slewing
11) changed stuffing to set Vcore offset to 0mV by default
12) changed comments to eliminate references to L3 in power supply section

3/18
13) changed stuffing options for GPU PCI ID to 0x319
14) changed R164 (DAC1RSET) to 107 ohm pulldown
15) added 10K pulldown to U43 pin A21
16) changed fan controller to ADT7460

3/19
17) added pads for 0.1uF cap from +Adapter to digital gnd for EMC
18) added pads for 0 ohm between chassis and digital gnd near ENET connector for EMC
19) corrected path to correct for last checkin
20) removed BOM table for MAP31
21) REMOVED ALL RELATIVE_PROPAGATION_DELAY AND PROPAGATION_DELAY PROPERTIES TO PRERPARE_FOR_CONSTRAINT_BACK_ANNOTATION
22) changed CHGND on R616 to CHGND1
23) ***BOARD RENUMBERED***

3/28
24) integrated M10 pages from Q16 schematic and renumbered them

4/10
25) updated physical constraints for M10 power nets
26) added DP7 for M10 power sequencing
27) added RP27,RP28,RP32, and RP57 for TMDS series termination
28) update PLL CFG high 0010 1.25GHz
low 1011 833MHz
29) update sscg/nosscg stuffing option on intrepid boot straps
30) removed D31 between +Batt and 24V_Pbus
31) add Vcore DAC resistors (R288,R289,R290,R292) for no mux case
32) change intrepid PLL LDO stuffing back to 1.8V main
33) change C640 and C646 to 0.01uF (Apple # 132S1047) for FW check config
34) change I2C pullups (R29 and R102) to 1K
35) changed bootrom part number to 341S1255

4/18
36) changed C756 to 128S0025 (Sanyo only 6.3V 330uF)
37) add pads for 90 ohm chokes to FWB path close to connector (route through the pads)
38) changed Vcore inductor (L36) to molded core part (152S0125)
39) changed Pbus inductor (L37) to molded core part (152S0126)
40) added seperate 1_8V_GPU_TPVDD filter and LDO (U54)

4/21
41) replace disctrete LCL with single chip LCL filters (155S0154) for VGA (L ,L , and L)
42) add 165 ohm chokes on TMDS data pairs at connector (L ,L , and L)
43) move BS1 to bottom side
44) move CPU thermal sensor (Q39) to input 1 on fan controller and power supply sensor (Q66) to input 2
45) added trace from Vcore to fan controller ADC input
46) added FET inverters (Q78) to PWM outputs of fan controller (U3) to prevent spinup at boot
47) added FET (Q79) for +3V_Sleep for M10 power sequencing

4/27
48) changed TMDS data chokes to 90 ohm (155S0128)
49) changed C762 and C766 to 4.7uF 1206 caps
50) changed TMDS data chokes to 90 ohms (155S0128)
51) changed C762 and C766 to 4.7uF 1206
52) changed Q51 to Si7860DP (376S0119)
53) changed Q48 to Si7892DP (376S0120)
54) changed D24 to B340LB (371S0132)
55) changed L30 to 2.2uH Tokin inductor (152S0139)
56) added Q58, R307, and C515 for GPU Vcore control inverter
57) changed R416 to 2.2ohms
58) changed R364 to 102K
59) added 0.1uF 50V C883 to RS- of Max4172 (NO stuff)
60) changed D18 to 1N914
61) changed L38 and L41 to 4.7uH (152S0137)
62) added Q81, R308, R309, and R310 for power sequencing (no stuff)
63) changed Q49 and Q50 to Si7860DP (376S0119)
64) changed L36 to 1.2uH 18.3A (152S0125)
65) added R331 1mohm sense resistor to CPU Vcore
66) added C885 and C884 , 1000uF CPU Vcore outpur caps
67) added Q82, R607, R455, R417, and C886 for 1.5V sleep sequencing
68) added Q83 and 100K R608 for 1.8V sequencing
69) added 15.4K R616 and 10K R672 for 2.5V switcher feedback divider
70) changed pinout of sound connector for sousaphone
71) removed Q44 (5V sound sleep fet)
72) changed Q31 to invert headphone Mute to sousaphone

4/28
73) changed CPU_VCORE_SLEEP location back to across bypass caps to correct after adding reference resistor
74) changed D5 to schottky diode (MBR0540)
75) fixed unnamed net (LTC3411_SHDN_SEQ)
76) changed drain/source polarity of Q76 (FET from +BATT to Pbus)

4/28
77) moved XW15 to connect to CPU_VCORE_SLEEP_UF (before positioning resistor)
78) changed Fan control nets to FanL and FanR from Fan1 and Fan2
79) SWAPPED CONNECTIONS SO THAT OUTPUT 1 FROM FAN CONTROLLER CONNECTS TO LEFT FAN (CPU) AND FAN 2 CONNECTS TO THE RIGHT FAN (GPU)
80) updated power constraints with new fan net names

4/28
81) change Q58 on pg19 to Q80 to consolidate parts
82) CHANGED U55 TO MM1571J FOR COST SAVINGS
83) changed L72,L73,L74 to 90 ohm ferrites
84) added 10K pullup to +5V_MAIN to SND_HP_MUTE
85) repinout Sousaphone connector
86) remore redundant pullups on FANL_TACH and FANR_TACH
87) added TP to all NC on NEC USB2 part for NAND tree testing
88) added NEC_USB bomoption to 0 ohm resistor on NEC_AVSS_F

4/30
89) repinout Sousaphone connector (J12)
90) no stuff R322 to eliminate 3V_sleep pump up
91) updated various text notes with correct reference designators

5/1
92) change L30 to 152S0139 (Tokin CPI-1050-2R2) 11A
93) remove FANR_TACH functional test point
94) add CHGND4 and SLEEP_LED functional test points
95) swap INT_AUDIO_TO_SND and SND_TO_AUDIO on Sousaphone connector (J12)

*** rev 01 released for EVT ***

5/6
96) remove NO STUFF on R477 (set 5V and 3.3V switcher in pulse skipping mode)
97) change R337 to 470K and remove No Stuff and no stuff R336 to change Vcore DAC to 1.35V/1.15V
98) change R321 to 499ohm to set 5mV Vcore offset
99) change L72,L73,L74 to 155S0165 (D part for EVT only)

*** rev 02 released for EVT ***

5/7
100) no stuff Q79 to disable 3V_SLEEP sequencing to work around wake from sleep bug with M10
101) added BOM table to define correct part number for M10 without heatspreader (338S0133)

*** rev 03 released for EVT ***

5/22
102) fixed NO STUFF BOM option for R291
103) add NO STUFF to R223 to correct startup level of GPU_VCORE_CNTL
104) add NO STUFF to R300 to complete 3V sequecing on wake from sleep fix
105) changed R376 to 158K and R321 to 2.74K to set CPU_VCORE offset to 35mV

*** rev 04 released for EVT ***

5/19/03
106) changed both AGP_NV_INT_L and AGP_ATI_INT_L to AGP_INT_L
107) removed redundant 3V_GPU pullup R687 (Intrepid side AGP_INT_L pullup)
108) added R699,R701,R707,R708 as 10k pulldowns to Intrepid USB ports A and C when NEC_USB is stuffed
109) changed SND_HP_MUTE_INV gate/inversion FETS to pullup to +3V_MAIN
110) added R711 as pullup to +3V_GPU on AUXWIN signal from M10 (U44)
111) added R698 as 0 ohm jumper between FW_PHY_PD and Intrepid
112) added U56, U57, R718,R714 for VGA Hsync and VGA Vsync buffering
113) changed L72,L73,L74 to 155S0164 (new high speed part)
114) added NO STUFF BOM option to R223 to correct for sense of GPU_VCORE_CNTL
115) added NO STUFF BOM option to R300 to avoid sleep wake problem

6/3/03
116) Intgrated new 1.8V switcher (LTC3412)(U58)(353S0650) and inductor (L75- 152S0142)
117) changed 2.5V_SLEEP FET (U48) and 1.8V_SLEEP FET (U6) to higher current part (Si6467BDQ - 376S0161)
118) added 10K pulldown (R720) on FW_PHY_PD_INT for when R698 is removed
119) changed R728 and R729 to 1210 0ohm resistors to support switching the entire memory bus between 1.8V and 2.5V
120) added R721 as jumper between +2_5V_SLEEP and +2_5V_GPU

6/4/03
121) NO STUFF R631 to remove MAIN_RESET_L from clock slewing chip
122) changed FWB connector to new part with extra ground tabs (514S0059)

6/5/03
123) changed I2C 0 and 1 pullups (RP12) to 2.2K to improve rise/fall times (sensor check config errors)
124) added CRITICAL flag to new 1.8V switcher (U58), inductor (L75), 1.8V sleep FET (U6), and 2.5V sleep FET (48)
125) removed gnd caps (C651 and C647) on I2S clock at sound connector (J12)
126) added LC filter on SND_CLKOUT for EMI (L77 and C895)
127) added LC filter on SND_CLKOUT for EMI (80 and C899)
128) added LC filter on INT_AUDIO_TO_SND for EMI (L81 and C896)
129) added LC filter on SND_TO_AUDIO for EMI (L82 and C897)
130) added LC filter on SND_AMP_MUTE for EMI (L76 and C898)
131) added LC filter on SND_HW_RESET_L for EMI (L78 and C900)
132) added LC filter on SND_SCLK for EMI (L79 and C901)
133) added C902 and R804 to prevent latch-up condition in GPU Vcore circuit when using powermiser
134) removed R331 (CPU Vcore positioning resistor)
135) changed C728,C729,C730,C731,C732,C733,C734,C884,C885 to 220uF Rubycon caps (128S0024)
136) add Vcore offset change circuit to modify offset in low (Q86,R805,R806,R807,R808,R809)
137) changed Q83 into dual (2N7002DW) and added R810 to invert 3V_5V_ON before switching RUN/SS

6/6/03
138) rotated J26 (FW B connector)
139) changed D29 to B340B (3A part - 371S0159)

6/9/03
140) modified Vcore offset select circuit with Takashi's changes - changed Gnd reference to VCORE_GND_SNS
141) added double inverter to buffer THERM_L_OC (added Q87,R811,R812)
142) removed redundant pullup on THERM_L_OC (R780)

6/9/03
143) added cap on gate of the second FET in Q87 for possible turn on delay (C903)
144) changed inner shield of FWB connector J26 to connect to chassis gnd
145) changed R336 and R325 to 0 ohm to set Vcore VID to 1.3V/1.15V
146) changed R321 to 2.49K to set Vcore offset to +25mV
147) added 10 ohm resistor (R814) and 1uF cap (C904) to filter power to ADT7460 (Gary Leo)

6/10/03
148) changed R612 to 10K to prevent UIDE DMACK from floating
149) changed C80,C88,C81,C89,C82,C102,C79,C87 to NO STUFF (TMDS common-mode termination)
150) changed R205,R218,R211,R219,R210,R220,R204,R214 to 162 ohm 1% (TMDS common-mode termination)
151) changed RP27,RP32,RP28,RP57 to 10ohm (TMDS series termination)

*** released for EVT2 6/10/03 ***

6/13/03
152) fixed NO STUFF on R291
153) removed NO STUFF from C80,C88,C81,C89,C82,C102,C79,C87 (TMDS common-mode termination)
154) removed NO STUFF from R638 (pullup on slewing chip FSEL)
155) removed NO STUFF from C903 (cap on input to second part of THERM_OC_L buffer)
156) CHANGED R321 TO 1K FOR VCORE OFFSET OF 12MV (VCORE = 1.30V -30MV/+100MV)

*** released for EVT2 6/13/03 ***

6/18/03
157) changed R228 to pullup to 1.8V for DVO interface conpatibility
158) added R234 and INT_TMDS option to maintain internal TMDS capability
159) changed L30 to 3 pin symbol
160) added U5 to use as external TMDS transmitter (DVI)
161) added R41 to create +3V_GPU_SI power for SIL1162 (U5)
162) added L14, C130, C132, and C165 for 3V AVCC filtering for SIL1162 (U5)
163) added L13, C14, C129, C131, C133 for 3V PVCC filtering for SIL1162 (U5)
164) added L15, C255, C233, C218 for 3V Vcc filtering for SIL1162 (U5)
165) added R235 and R237 as options for MAIN_RESET_L to U5
166) added R231. R232, and C284 for Vref for U5
167) added R66, R99, R202, R212, R222, R224, R88, R110, R223 as straps for U5
168) added RP58, RP59, RP60, RP61 for series termination of SIL1162 TMDS output
169) added L16, C304, C327, C647 for filtering GPU VDDR4
170) added R255 and R251 to strap GPU_DVODMODE correctly for 1.8V DVO
171) added R268 to connect L16 to +3V_GPU_FLT when not using SIL1162
172) added C681, C668, C678, C651 to filter the thermal sensor diff pairs

6/19/03
173) changed GPU_MEM_IO to +GPU_MEM to connect ATI Vref to correct memory voltage
174) swapped TMDS_CLKN and CLKP on RP57 and RP58 for layout
175) swapped DN<0> and DP<0> on RP27 for layout
176) corrected un-named nets in TMDS common-mode filters
177) added physical constriants for new Silicon Image power rails
178) CHANGED C728,C731,C734,C733,C730,C732,C729,C885,C885 TO 128S0022
(124S0024 WILL BE DELETED AS A DUPLICATE IN THE LIBRARY)

6/23/03
179) NO STUFF'ed C895,C899,C896,C897,C898,C900, and C901 to fix no sound problem
180) changed C890 to 100pF for improved transient response (Takashi)
181) Removed bypass traces on FWB chokes and stuffed L70 and L71
182) CHANGED R491 TO 52.3K 1%, R475 TO 127K 1%, AND R476 TO 4.7M 5% IN A29 ADAPTER DETECT CIRCUIT DIVIDERS TO REDUCE SHUTDOWN CURRENT
183) added R331 as CPU Vcore sense resistor (1 mohm 1% 2512)
184) No STUFF'ed C651 and C678
185) added C688,C690,C846,C905 for thermal pair filtering at fan controller
186) added C906 to prevent shoot-thru on Q64 (currently NO STUFF'ed)
187) added C907 to prevent shoot-thru on Q68 (currently NO STUFF'ed)
188) changed R517 to 100K
189) changed GND reference for input side of Q86 to digital GND (the other FET in Q856 remains on VCORE_GNDSNS

6/24/03
190) added C908 to prevent gate shoot-thru on Q56
191) added R279 to power TMDS PLL from LVDS filter when using external TMDS transmitter
192) changed R325 to 470K to set the low Vcore to 1.10V
193) stuffed Vcore offset switch (R807,R805,R809,Q86)
194) changed R809 to 1.5K 1% to set low Vcore offset to 10mV
195) changed R321 to 3.01K 1% to set high Vcore offset to 30mV

6/25/03
196) rotated L70 and L71 for layout (PCB symbol problem)
197) changed Q53,Q54,Q55 to IRF7832 (376S0148) for better thermal performance
198) NO STUFF'ed C908 (Q56 gate shoot-thru cap)

*** released for DVT 6/26/03 ***

7/2/03
199) CHANGED J9 (CARDBUS) TO 516S0141 (NEW PIN PLATING SPEC)
200) CHANGED J20 (AIRPORT) TO 516S0142 (NEW PIN PLATING SPEC)
201) CHANGED J10 (OPTICAL DRIVE) TO 516S0140 (NEW PIN PLATING SPEC)
202) CHANGED J13 (HARD DRIVE) TO 516S0140 (NEW PIN PLATING SPEC)
203) CHANGED J12 (SOUND) TO 516S0144 (NEW PIN PLATING SPEC)
204) CHANGED J8 (MODEM) TO 516S0143 (NEW PIN PLATING SPEC)
205) ADDED BOM TABLE TO PUT 0 OHM 402 ON L77,L80,L81,L82,L76,L78,L79

7/9/03
207) CORRECTED C889 TO CONNECT TO INPUT (PIN 1) OF U55
208) REMOVED POWER JUMPERS XW25,XW17,XW16,XW10,XW14,XW18
209) CHANGED 197S0035 TO PRIMARY AND 197S0004 AS ALTERNATE FOR Y1 (INTREPID)
210) CHANGED 197S0037 TO PRIMARY AND 197S0603 AS ALTERNATE FOR Y3 (ETHERNET)
211) CHANGED 197S0038 TO PRIMARY AND 197S0608 AS ALTERNATE FOR Y5 (NEC USB2)
212) CHANGED 197S0040 TO PRIMARY AND 197S0008 AS ALTERNATE FOR Y4 (LMU)
213) CHANGED 197S0041 TO PRIMARY AND 197S0604 AS ALTERNATE FOR Y6 (PMU)

7/22/03
214) ADDED 1_32V_VCORE AND 1_30V_VCORE BOM OPTIONS FOR 2 DIFFERENT CPU VCORE SPECS
215) UPDATED CAP_MATERIAL TYPES
216) CHANGED FROM 715 PIN TO 667 PIN SYMBOL FOR U44 (M10)

7/28/03
217) CHANGED TMDS TERMINATION FROM 2X 162 TO 2X 49.9 OHMS PER PAIR
218) CHANGED 126S0036 FROM ALT TO PRIMARY, REPLACING 126S0035 FOR CPU VCORE INPUT CAPS

*** RELEASED FOR PRODUCTION 7/28/03 ***

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6459	A

SCALE NONE

SHT 40 OF 44

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*** Signal Cross-Reference for the entire design ***

+1_0V_MARVELL       27D2< 38B3>
+1_5V_AGP           12C5< 12D1< 12D4< 15D6< 16C8<
                  18C6< 18D6< 19A8< 19B4<> 19D5<>
                  21B8< 21D6< 38C3>
+1_5V_AGP_GPU       21C5< 38C3>
+1_5V_AGP_NECK      19B4<> 38B3>
+1_5V_GPU_VDD15     19D3< 38C3>
+1_5V_INTREPID_PLL  8D6< 12D4< 12D8< 14D6<> 38D3>
+1_5V_INTREPID_PLL1  14C3< 38D3>
+1_5V_INTREPID_PLL2  14D3< 38D3>
+1_5V_INTREPID_PLL3  14D3< 38D3>
+1_5V_INTREPID_PLL4  14D3< 38D3>
+1_5V_INTREPID_PLL5  12D3< 38D3>
+1_5V_INTREPID_PLL6  12D6< 38D3>
+1_5V_INTREPID_PLL7  8D5< 38D3>
+1_5V_INTREPID_PLL8  14D3< 38D3>
+1_5V_LDO           35D8< 38D6>
+1_5V_MAIN          38D6>
+1_5V_SLEEP         38D6>
+1_5V_SLEEP_NECK    21A3<> 38B3>
+1_5V_SLEEP_VIN     35D8<> 38D6>
+1_8V_ATI_PVDD      19C5<> 21B6< 21B6< 21D6<> 38C3>
+1_8V_ATI_TPVDD     21D2<>
+1_8V_DVO_F         21B2<
+1_8V_GPU           18A7< 19D8< 20A5< 21A2< 21A6<
                  21B1< 21B6< 21C8< 21D6< 21D8< 38C3>
+1_8V_GPU_AVDD      21D5< 38C3>
+1_8V_GPU_AVDDQ     21D4< 21D7< 38C3>
+1_8V_GPU_MEMPLL    21B5< 38C3>
+1_8V_GPU_PLL       21D5< 38C3>
+1_8V_GPU_PNLIO     21A5< 38C3>
+1_8V_GPU_PNLPLL    21B5< 38C3>
+1_8V_GPU_TP_PLL    21B4< 21D1<
+1_8V_GPU_VDDDI     21C7< 21D4< 38C3>
+1_8V_MAIN          38D6> 39A2>
+1_8V_MAIN_LX_F     35A4<>
+1_8V_PVDD_NECK     19B5<> 38B3>
+1_8V_SLEEP         38D6>
+1_8V_SLEEP_NECK    21A3<> 38B3>
+1_95V_FW_DVDD      28C4< 28C7<> 28D5< 38A3>
+1_95V_FW_DVDD_PORT1  28D6< 38A3>
+1_95V_FW_DVDD_RX0  28C5< 38A3>
+1_95V_FW_DVDD_TX0  28C5< 38A3>
+1_95V_FW_PLL400VDD  28D5< 38A3>
+1_95V_FW_PLL500VDD  28D5< 38A3>
+1_95V_FW_PLLVDD    28D5< 28D7<> 38A3>
+2_5V_CG_MAIN       14C6< 38A3>
+2_5V_GPU           21A7< 21B6< 21D3< 21D7< 21D8<
                  38B3>
+2_5V_GPU_A2VDD     21D4< 21D7< 38C3>
+2_5V_GPU_PNLIO     21A5< 38C3>
+2_5V_INTREPID      9A8< 10D3< 10D5< 10D7< 10D8< 15D7<
                  16B8< 38D3>
+2_5V_MAIN          38D6>
+2_5V_MARVELL       27B8< 27C4<> 38B3>
+2_5V_MARVELL_AVDD  27C4< 38B3>
+2_5V_SLEEP         38D6>
+2_5V_SLEEP_NECK1   19C4<> 38B3>
+2_5V_SLEEP_NECK2   21A3<> 38B3>
+3V_ATI_OSC_SLEEP   18D2< 38C3>
+3V_ATI_SS          18B2< 38C3>
+3V_CG_PLL_MAIN     14C6< 38A3>
+3V_FW              28A3< 28D7<> 29D5< 38A3>
+3V_FW_AVDD         28C6< 38A3>
+3V_FW_AVDD_PORT0   28C6< 38A3>
+3V_FW_AVDD_PORT1   28C6< 38A3>
+3V_FW_AVDD_PORT2   28D6< 38A3>
+3V_FW_ESD          29B3<> 29D2<> 38B3>
+3V_FW_ESD_ILIM     29D4< 38B3>
+3V_FW_UF           28D7<> 38A3>
+3V_GPU             12D1< 18B8< 18C5< 18C7< 18D6<
                  19C4< 19C5< 19C7< 19D7< 21A6< 21B1<
                  38C3>
+3V_GPU_FLT         21B2< 38C3>
+3V_GPU_SI          20C4< 20C8< 20D8<
+3V_HALL_EFFECT     23C6<> 38B6> 39C4>
+3V_INTREPID_USB    14C3< 38D3>
+3V_LCD             22B4<> 38B6>
+3V_LCD_SW          22A4<> 38B6>
+3V_MAIN            38D6>
+3V_NEC_VDD         26D7< 26D7< 38A3>
+3V_PMU             38D6> 39A2>
+3V_PMU_AVCC        25A4< 30B6< 30D5<> 38C6>
+3V_PMU_ESR         32A2< 38C6>
+3V_PMU_RESET       30B7< 34A3<>
+3V_SI_AVCC         20C7< 38B3>
+3V_SI_PLLVCC       20C7< 38B3>
+3V_SI_VCC          20C6< 38B3>
+3V_SLEEP           38D6>
+3V_SLEEP_NECK      21A3<> 38B3>
+3V_SLP_OK_L        33B4<>
+3V_SLP_ON          33A5<>
+4_6V_BU            32A3<> 33B6< 38C6>
+4_85V_ESR          32A4< 38C6>
+4_85V_RAW          30B4< 32A4<> 38C6>
+5V_DDC_SLEEP       22D3<> 22D5<> 38B6> 39A2>
+5V_DDC_SLEEP_UF    22D6< 38B6>
+5V_HD_SLEEP        24D1<> 33A7<> 38C6>
+5V_INV_SW          22B2<> 38B6> 39D1>
+5V_INV_UF_SW       22B2<> 38B6>
+5V_MAIN            38D6>
+5V_SLEEP           38D6>
+5V_SOUND_SLEEP     38B6>
+5V_TPAD_SLEEP      23C7<> 38B6> 39C4>
+12_8V_INV          22B1<> 38B6> 39A2>
+24V_PBUS           38D6> 39B2>
+ADAPTER            31D8<> 32B7< 38D6>
+ADAPTER_ILIM       32B6< 38C6>
+ADAPTER_OR_BATT    32A5<> 38C6>
+ADAPTER_SENSE      31D5<> 38C6>
+ADAPTER_SW         31D6<> 38C6>
+BATT               38D6>
+BATT_14V_FUSE      31D1<> 38C6>
+BATT_24V_FUSE      31B1< 31D2<> 38C6>
+BATT_POS           31A4<> 38C6> 39C3>
+BATT_RSNS          31B2< 38C6>
+BATT_VSNS          31A4< 38C6>
+FW_FUSE            29D7<> 38A3>
+FW_PWR_OR          28B8< 28D8<> 29D5<> 38A3>
+FW_PWR_PORTA       29C5< 38A3>
+FW_SW              29D5<> 38A3>
+FW_VP0             29C2<> 38A3>
+FW_VP1             29A3<> 38A3>
+GPU_MCLK           21C7< 21D4< 38C3>
+GPU_MEM            18A6<> 18B8< 21B4< 21B7< 21C6<
                  21C8< 21D2< 38C3>
+GPU_MEMCORE        21C5< 38C3>
+GPU_VDD15_NECK     19B5<> 38B3>
+GPU_VDD15_UF       19B5<> 19D4<> 38C3>
+HD_LOGIC_SLEEP     24C2<> 38C6>
+PBUS               38D6> 39B2>
+VCC_CBUS_SW        17B1<> 17B2<> 17D2<> 38D3>
+VPP_CBUS_SW        17B1<> 17B2<> 17D2<> 38C3>
1V20_REF            31C7< 32C8< 38D1>
1V65_REF            31A5<
1_5V_2_5V_OK        35C5> 38B1>
1_5V_BOOST          35C6<> 38C1>
1_5V_BST            35C5<> 38C1>
1_5V_DH             35C5<> 38C1>
1_5V_DL             35B5<> 38C1>
1_5V_FB             35B5< 35B7< 38C1>
1_5V_ILIM           35C5<> 38C1>
1_5V_LX             35B5<> 38C1>
1_5V_SLEEP_EN_L     35C7<> 35D7<>
1_8V_SLEEP_PWREN_L  35A3<>
1_8V_SW             35A5<> 38A1>
1_8V_VFB            38A1>
2_5V_BOOST          35C4<> 38D1>
2_5V_BST            35C4<> 38D1>
2_5V_DH             35C4<> 38D1>
2_5V_DL             35B4<> 38D1>
2_5V_ILIM           35C5<> 38C1>
2_5V_LX             35B4<> 38D1>
2_5V_SLEEP_PWREN_L  35C2<>
2_34V_REF           30A4<
3V_5V_OK            33B4<> 35A8<> 35D6<
3V_5V_OK_INV        35A8<>
3V_BG               33C4<>
3V_BOOST            33C4<>
3V_BOOST_ESR        33D3<>
3V_ITH              33C4<>
3V_ITH_RC           33C3<
3V_PMU_VTAP         32B3<
3V_RSNS             33D2< 38D1>
3V_RUNSS            33C4<
3V_SLEEP_PWREN_L    33A3<>

3V_SNSM             33C4< 37A2>
3V_SNSP             33C4< 37A2>
3V_SW               33C4<> 38D1>
3V_TG               33D4<>
3V_VOSNS            33C4<>
5V_BG               33C5<>
5V_BOOST            33C5<>
5V_BOOST_ESR        33D6<>
5V_HD_PWREN         33A8<>
5V_ITH              33C5<>
5V_ITH_RC           33C6<
5V_RSNS             33D7< 38D1>
5V_RUNSS            33C5<
5V_SLEEP_PWREN      33A8<>
5V_SNSM             33C5< 37A2>
5V_SNSP             33C5< 37A2>
5V_SW               33C5<> 38D1>
5V_TG               33C5<>
5V_VOSNS            33C5<>
1625_BG             32C5<>
1625_BST            32C5<
1625_BST_ESR        32C5<>
1625_COMP           31D2< 32C6<
1625_DIV            32C8<
1625_ENABLE         32D7<>
1625_ENABLE_L       32D6<>
1625_EXTVCC         32D5<> 38D1>
1625_FCB            32C6<
1625_INTVCC         32C5<> 38D1>
1625_RUNSS          32C6<
1625_SGND           32B7<> 38D1>
1625_TG             32C5<>
1625_VFB            32B5<>
1625_VIN            32C6< 38D1>
1625_VSW            32C4<> 38D1>
1772_ACIN           31B5<
1772_ACOK_L         31B5<> 31C4<>
1772_BST            31B4<>
1772_BST_ESR        31C3<
1772_CCI            31B5<>
1772_CCS            31B5<
1772_CCV            31B5<>
1772_CCV_RC         31B5<
1772_CELLS          31B4<
1772_CLS            31A4<
1772_CSIN           31B4<> 37A2>
1772_CSIP           31B4<> 37A2>
1772_CSSN           31C5< 37A2>
1772_CSSP           31C5< 37A2>
1772_DCIN           31B5< 38C6>
1772_DHI            31B4<>
1772_DLO            31B4<>
1772_DLOV           31B4<> 38C6>
1772_GND            31A5<> 38C6>
1772_ICHG           31B5<>
1772_ICTL           31B5<>
1772_IINP           31B5<
1772_LDO            31C4<> 38C6>
1772_LX             31B4<> 38C6>
1772_REF            31B5<>
1772_VCTL           31B5<
1778_BG             19A5<> 38B1>
1778_BST            19A5<> 38B1>
1778_BST_RC         19A4<> 38B1>
1778_FCB            19A5< 38B1>
1778_GND            19A5< 19A7<> 38B1>
1778_ION            19A5< 38B1>
1778_ITH            19A5<> 38B1>
1778_ITH_RC         19A7< 38B1>
1778_SHDN_L         19A6<
1778_SHDN_L_D3COLD  19A7<>
1778_TG             19A5<> 38B1>
1778_VCC            19A5<> 38B1>
1778_VFB            19A2< 19A5< 38B1> 39A1>
1778_VIN            19A5< 38B1>
1778_VRNG           19A5< 38B1>
3405_MODE           27D5<
3405_VFB            27D4<>
3707_FCB            33C5<
3707_FSET           33C5<
3707_INTVCC         33D4<> 38D1>
3707_SGND           33B5<> 38D1>
3707_STBY           33C5<>
A29_CLS_ADJ         31A5<>
A29_CURRENT_ADJ     31C4<>
A29_DETECT          30A2< 31A5<> 31C4<>
A29_DET_L           30A3<
AB_SEL_LOW          34A6<>
AC_DIV              31C8<
AC_ENABLE_GATE      31D6<>
AC_ENABLE_L         31C6<>
AC_GTR_18V          31C4<>
AC_IN               27B8<> 29C7< 30B3< 31C5<> 31C7<>
AC_IN_FW_CNTL       29C7<>
AC_IN_L             31C2<> 31C6<>
AC_IN_L_RC          31C2<>
ADAPTER_DET         30A4< 31D8<> 39C2>
ADAPTER_I_REG       31D3<>
ADT7460_ADR_EN_L    25B3<>
ADT7460_FAN1_PWM    25B3<>
ADT7460_FAN2_PWM    25B3<>
ADT7460_THERM       25A5<> 25B3<>
ADT7460_VCC         25C4<
ADT7460_VCORE_MON   5C8<> 25B4<>
AGP8X_DET_PU        18C6<>
AGP_AD<0>           12D2<> 18C7<>
AGP_AD<15..0>       37D5>
AGP_AD<1>           12C2<> 18C7<>
AGP_AD<2>           12C2<> 18C7<>
AGP_AD<3>           12C2<> 18C7<>
AGP_AD<4>           12C2<> 18C7<>
AGP_AD<5>           12C2<> 18C7<>
AGP_AD<6>           12C2<> 18C7<>
AGP_AD<7>           12C2<> 18C7<>
AGP_AD<8>           12C2<> 18C7<>
AGP_AD<9>           12C2<> 18C7<>
AGP_AD<10>          12C2<> 18C7<>
AGP_AD<11>          12C2<> 18C7<>
AGP_AD<12>          12C2<> 18C7<>
AGP_AD<13>          12C2<> 18C7<>
AGP_AD<14>          12C2<> 18C7<>
AGP_AD<15>          12C2<> 18C7<>
AGP_AD<16>          12C2<> 18C7<>
AGP_AD<31..16>      37D5>
AGP_AD<17>          12C2<> 18C7<>
AGP_AD<18>          12C2<> 18C7<>
AGP_AD<19>          12C2<> 18C7<>
AGP_AD<20>          12C2<> 18C7<>
AGP_AD<21>          12C2<> 18C7<>
AGP_AD<22>          12C2<> 18C7<>
AGP_AD<23>          12C2<> 18C7<>
AGP_AD<24>          12C2<> 18C7<>
AGP_AD<25>          12C2<> 18D7<>
AGP_AD<26>          12C2<> 18D7<>
AGP_AD<27>          12B2<> 18D7<>
AGP_AD<28>          12B2<> 18D7<>
AGP_AD<29>          12B2<> 18D7<>
AGP_AD<30>          12B2<> 18D7<>
AGP_AD<31>          12B2<> 18D7<>
AGP_AD_STB<0>       12A2<> 12B2< 18D6<> 37D5>
AGP_AD_STB<1>       12A2<> 12B2< 18D6<> 37D5>
AGP_AD_STB_L<0>     12A2<> 12B2< 18D6<> 37D5>
AGP_AD_STB_L<1>     12A2< 12A2<> 18D6<> 37D5>
AGP_ATI_RESET_L     18B7<
AGP_ATI_VREF        18B7<
AGP_ATI_VREFG       18B7<
AGP_BUSY_L          12C4<> 12D2< 18D6>
AGP_CBE<0>          12B2<> 18B7<>
AGP_CBE<1..0>       37D5>
AGP_CBE<1>          12B2<> 18B7<>
AGP_CBE<2>          12B2<> 18B7<>
AGP_CBE<3..2>       37D5>
AGP_CBE<3>          12B2<> 18C7<>
AGP_DEVSEL_L        12B2<> 12C2< 18B7<> 37D5>
AGP_FRAME_L         12B2<> 12C2< 18B7<> 37D5>
AGP_GNT_L           12C2< 12D2<> 18B7< 37D5>
AGP_INT_L           14B5<> 18B7<>
AGP_IRDY_L          12B2<> 12C2< 18B7<> 37D5>
AGP_PAR             12B2<> 18B7> 37D5>
AGP_PIPE_L          12A2<> 12B2<
AGP_RBF_L           12A2<> 12C2< 18C6> 37D5>
AGP_REQ_L           12C2< 12D2<> 18B7<> 37D5>
AGP_SBA<0>          12B2< 18C6>
AGP_SBA<7..0>       37D5>
AGP_SBA<1>          12B2<> 18C6>
AGP_SBA<2>          12B2<> 18C6>
AGP_SBA<3>          12B2<> 18C6>
AGP_SBA<4>          12B2<> 18C6>

AGP_SBA<5>          12B2<> 18C6>
AGP_SBA<6>          12B2<> 18C6>
AGP_SBA<7>          12B2<> 18C6<>
AGP_SB_STB          12B2< 12B2<> 18C6<> 37D5>
AGP_SB_STB_L        12A2< 12A2<> 18C6<> 37D5>
AGP_ST<0>           12A2<> 18C6<
AGP_ST<1>           12A2<> 18C6<
AGP_ST<2>           12A2<> 18C6<
AGP_STOP_L          12B2<> 12C2< 18B7<> 37D5>
AGP_STP_L           18C6<
AGP_SUS_STAT_L_PU   18C6<
AGP_TRDY_L          12B2<> 12C2< 18B7<> 37D5>
AGP_WBF_L           12A4<> 12B2< 18B7>
AIRPORT_CLKRUN_L    24C6<> 39C1>
AIRPORT_IDSEL       24C5<> 39B1>
AIRPORT_PCI_GNT_L   12D7<> 24D5<> 39C4>
AIRPORT_PCI_INT_L   14B5<> 14D7< 24D5<> 39C4>
AIRPORT_PCI_REQ_L   12A7< 12D7<> 24D6<> 39D4>
AIRPORT_PME_L_TP    24D5<>
AMP_CONTROL         25C5<> 25D5<>
ATI_AGP_FBSKEW<0>   19C2< 19C7<>
ATI_AGP_FBSKEW<1>   19C2< 19C7<>
ATI_BUS_CFG<0>      19B2< 19C7<>
ATI_BUS_CFG<1>      19B2< 19C7<>
ATI_BUS_CFG<2>      19B2< 19C7<>
ATI_CLK27M_IN       18C1< 19B7<
ATI_CLK27M_OSC      18D2<
ATI_CLK27M_OSC_SS   18B2< 18D1<
ATI_DBI_HI_PU       18C6<>
ATI_DBI_LO_PU       18C6<>
ATI_DVODMODE        21A3<
ATI_GPIO7_SPN       19C7<>
ATI_GPIO8_PD        19C7<>
ATI_GPIO9_SPN       19C7<>
ATI_GPIO10_SPN      19C7<>
ATI_GPIO11_SPN      19C7<>
ATI_GPIO12_SPN      19C7<>
ATI_GPIO13_SPN      19C7<>
ATI_HSYNC           19D5<> 22C8<
ATI_MEMTEST         18A6<>
ATI_MEMVMODE0       18A7<
ATI_MEMVMODE1       18A7<
ATI_OSC_OE          18D3<
ATI_PVDD_BYP        21D6<>
ATI_R2SET           19D6<>
ATI_RSET            19D6<>
ATI_RSTB_MSK        18C6<>
ATI_SSCLK_IN        18B1< 19B7<>
ATI_SSCLK_UF        18B1<>
ATI_TESTEN          19B7<
ATI_TMDS_CLKN       19B7> 20B4<
ATI_TMDS_CLKP       19B7> 20B4<
ATI_TMDS_DN<0>      19B7> 20B4<
ATI_TMDS_DN<1>      19B7> 20A4<
ATI_TMDS_DN<2>      19B7> 20A4<
ATI_TMDS_DP<0>      19B7> 20B4<
ATI_TMDS_DP<1>      19B7> 20A4<
ATI_TMDS_DP<2>      19B7> 20A4<
ATI_TPVDD_BYP       21D1<>
ATI_VSYNC           19D5<> 22C8<
ATI_X1CLK_SKEW<0>   19C2< 19C7<>
ATI_X1CLK_SKEW<1>   19B2< 19C7<>
BATTV_HIGH          31B7<>
BATTV_LOW           31B8<>
BATT_14PBUS_EN      31C1<>
BATT_14V_GATE       31C1<>
BATT_24PBUS_EN      31C2<>
BATT_24V_GATE       31C1<>
BATT_CLK            31A4<> 39C3>
BATT_DATA           31A4<> 39C3>
BATT_DIV            31A5<
BATT_LOW            31A6<>
BATT_LOW_L          31B6<>
BATT_NEG            31A4<> 38C6> 39C3>
BBANG_HRESET_L      23A4< 23C4<> 39C1>
BBANG_JTAG_TCK      23B3< 23C4<>
BBANG_TCK_EN        23B3<
BCKFD_PROT_EN_L     31C6<>
BCKFD_PROT_GATE     31D6<>
BRIGHT_PWM          22A1<> 39A7>
BRIGHT_PWM_UF       22A2<>
BT_USB_DM           14B1< 24B2<> 37B2> 39B6>
BT_USB_DP           14C1< 24B2<> 37B2> 39B6>
CAPSLOCK_LED        23A8<
CAPSLOCK_LED_L      23B8< 30C7<
CBUS_ADDR<0>        17B1<> 17B4>
CBUS_ADDR<1>        17B1<> 17B4>
CBUS_ADDR<2>        17B1<> 17B4>
CBUS_ADDR<3>        17B1<> 17B4>
CBUS_ADDR<4>        17B1<> 17B4>
CBUS_ADDR<5>        17B1<> 17B4>
CBUS_ADDR<6>        17B1<> 17B4>
CBUS_ADDR<7>        17B1<> 17B4>
CBUS_ADDR<8>        17B1<> 17B4>
CBUS_ADDR<9>        17B1<> 17B4>
CBUS_ADDR<10>       17B4> 17C1<>
CBUS_ADDR<11>       17B1<> 17B4>
CBUS_ADDR<12>       17B1<> 17B4>
CBUS_ADDR<13>       17B1<> 17B4>
CBUS_ADDR<14>       17B1<> 17B4>
CBUS_ADDR<15>       17B1<> 17B4>
CBUS_ADDR<16>       17B1<> 17B4<
CBUS_ADDR<17>       17B2<> 17B4>
CBUS_ADDR<18>       17B2<> 17B4>
CBUS_ADDR<19>       17B2<> 17B4>
CBUS_ADDR<20>       17B2<> 17B4>
CBUS_ADDR<21>       17B2<> 17B4>
CBUS_ADDR<22>       17A4> 17B2<>
CBUS_ADDR<23>       17A4> 17B2<>
CBUS_ADDR<24>       17A4> 17B2<>
CBUS_ADDR<25>       17A4> 17B2<>
CBUS_ADDR_16_UF     17B5<>
CBUS_BVD1_L         17B2<> 17C4<
CBUS_BVD2_L         17B2<> 17C4<
CBUS_CE1_L          17C1<> 17C4>
CBUS_CE2_L          17B4> 17C2<>
CBUS_DATA<0>        17A1<> 17A4<>
CBUS_DATA<1>        17A1<> 17A4<>
CBUS_DATA<2>        17A1<> 17A4<>
CBUS_DATA<3>        17A4<> 17C1<>
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CBUS_DATA<8>        17A2<> 17A4<>
CBUS_DATA<9>        17A2<> 17A4<>
CBUS_DATA<10>       17A2<> 17A4<>
CBUS_DATA<11>       17A4<> 17C2<>
CBUS_DATA<12>       17A4<> 17C2<>
CBUS_DATA<13>       17A4<> 17C2<>
CBUS_DATA<14>       17A4<> 17C2<>
CBUS_DATA<15>       17A4<> 17C2<>
CBUS_DET_1_L        17C2<> 17C4< 39B8>
CBUS_DET_2_L        17A2<> 17C4< 39B8>
CBUS_INPACK_L       17B2<> 17B4<
CBUS_INT_L          14B5<> 14B7< 17A7<>
CBUS_IORD_L         17B2<> 17C4>
CBUS_IOWR_L         17B2<> 17C4>
CBUS_MFUNC1_PD      17A7<> 17A7<
CBUS_MFUNC2_PD      17A7<> 17A7<
CBUS_MFUNC3_PD      17A7<> 17A7<
CBUS_MFUNC4_PD      17A7<> 17A7<
CBUS_MFUNC5_PD      17A7<> 17A7<
CBUS_MFUNC6_PD      17A7< 17A7<>
CBUS_OE_L           17C1<> 17C4>
CBUS_PCI_GNT_L      12D7<> 17A7<
CBUS_PCI_IDSEL      17B7<
CBUS_PCI_PERR_L     17B7<> 17D7<
CBUS_PCI_REQ_L      12A7< 12D7<> 17A7>
CBUS_PCI_RESET_L    17A7<
CBUS_PCI_SERR_L     17B7> 17D7<
CBUS_READY          17B1<> 17C4<
CBUS_REG_L          17B2<> 17C4>
CBUS_RESET_L        17B2<> 17C4>
CBUS_SUSPEND_PU     17A7< 17D7<
CBUS_VCCD0_L        17C4<>
CBUS_VCCD1_L        17C4<>
CBUS_VPPD0          17C4<>
CBUS_VPPD1          17C5<>
CBUS_VS1            17B2<> 17C4<>
CBUS_VS2            17B2<> 17C4<>
CBUS_WAIT_L         17B2<> 17B4<
CBUS_WE_L           17B1<> 17C4>
CBUS_WP_L           17A1<> 17B4<
CG_ADDRSEL          14B7<
CG_CLKOUT           14B6<>
CG_FSEL             14B7< 14C5<>
CG_LOCK             14B7<>

CG_RESET_L          14B7<
CHARGE_DISABLE      31A7<>
CHARGE_LED_L        30C6<> 30D7< 31D8<> 39D2>
CHGND1              38A6>
CHGND2              38A6>
CHGND3              38A6>
CHGND4              38A6> 39B6>
CHGND5              38A6>
CHGND6              38A6>
CLK10M_PMU_XIN      30B6<
CLK10M_PMU_XOUT     30B6<
CLK10M_PMU_XOUT_UF  30B7<
CLK18M_INT_EXT      14A6<> 36B1>
CLK18M_INT_XIN      14A5< 36B1>
CLK18M_INT_XOUT     14A5<> 36B1>
CLK18M_XTAL_IN      14A5<> 36B1>
CLK25M_ENET_XIN     27A7< 36B1>
CLK25M_ENET_XOUT    27A7<> 36B1>
CLK25M_XTAL_IN      27A7<
CLK27M_GPU_XIN      36B1>
CLK27M_GPU_XOUT     36B1>
CLK27M_XTAL_IN      36B1>
CLK32K_PMU_XIN      30B3<>
CLK32K_PMU_XOUT     30B3<>
CLK32K_PMU_XOUT_UF  30B2<>
CLK33M_AIRPORT      12D8< 24D5<> 36C1> 39B1>
CLK33M_AIRPORT_UF   12C7<> 36C1>
CLK33M_CBUS         12D8< 17A7< 36C1>
CLK33M_CBUS_UF      12C7<> 36C1>
CLK33M_USB2         12C8< 26B7< 36C1>
CLK33M_USB2_UF      12C7<> 36C1>
CLK66M_AGP_15V_TP   12C4>
CLK66M_GPU_AGP      12C8< 18B7< 36C1>
CLK66M_GPU_AGP_UF   12C7<> 36C1>
CLKENET_LINK_GBE_REF  13C5< 27C8< 36B1>
CLKENET_LINK_GTX    13C5<> 36A1>
CLKENET_LINK_RX     13D5< 27C8< 36B1>
CLKENET_LINK_TX     13D5< 27D8< 36A1>
CLKENET_PHY_GBE_REF  27C7<> 36B1>
CLKENET_PHY_GTX     13C6< 27C7< 36A1>
CLKENET_PHY_RX      27C7<> 36B1>
CLKENET_PHY_TX      27D7<> 36B1>
CLKFW_LINK_LCLK     13C3<> 36A1>
CLKFW_LINK_PCLK     13C3<> 28C3< 36A1>
CLKFW_PHY_LCLK      13C2< 28B8< 36A1>
CLKFW_PHY_PCLK      28B4> 28C3< 36A1>
CLKLVDS_LN          19B5> 22A4<> 37C2> 39B7>
CLKLVDS_LP          19B5> 22A4<> 37C2> 39B7>
CLKLVDS_UN          19B5> 22A4<> 37C2> 39B7>
CLKLVDS_UP          19B5> 22A4<> 37C2> 39A7>
COMM_DTR_L          14C2> 25D1<> 39B2>
COMM_GPIO_L         14C2<> 25D2<> 39C2>
COMM_RESET_L        14C5<> 25C4<> 39C4>
COMM_RING_DET_L     14B5<> 14C7< 25C3<> 30C6<> 39C4>
COMM_RTS_L          14C2> 25D1<> 39B2>
COMM_RXD            14C2<> 25D1<> 39B2>
COMM_SHUTDOWN       14C5<> 25C4<> 39C4>
COMM_TRXC           14C2<> 25D2<> 39C2>
COMM_TXD_L          14C2<> 25D2<> 39C2>
COMP_DISABLE        22C2<>
COMP_ENABLE         22C1<>
COMP_RC             32C6<
CPU_AACK_L          5A7< 8B6<> 8C2< 36D5>
CPU_ADDR<0>         5C7<> 8D6<>
CPU_ADDR<0..31>     36D5>
CPU_ADDR<1>         5C7<> 8D6<>
CPU_ADDR<2>         5C7<> 8D6<>
CPU_ADDR<3>         5C7<> 8D6<>
CPU_ADDR<4>         5C7<> 8D6<>
CPU_ADDR<5>         5C7<> 8C6<>
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CPU_ADDR<10>        5B7<> 8C6<>
CPU_ADDR<11>        5B7<> 8C6<>
CPU_ADDR<12>        5B7<> 8C6<>
CPU_ADDR<13>        5B7<> 8C6<>
CPU_ADDR<14>        5B7<> 8C6<>
CPU_ADDR<15>        5B7<> 8C6<>
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CPU_ADDR<17>        5B7<> 8C6<>
CPU_ADDR<18>        5B7<> 8C6<>
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CPU_ADDR<28>        5B7<> 8C6<>
CPU_ADDR<29>        5B7<> 8C6<>
CPU_ADDR<30>        5B7<> 8C6<>
CPU_ADDR<31>        5B7<> 8B6<>
CPU_ARTRY_L         5A7<> 8B6<> 8D2< 36D5>
CPU_AVDD            5C3< 38D3>
CPU_BG_L            5C7< 8C2< 8D6<> 36D5>
CPU_BR_L            5C7> 8D2< 8D6< 36D5>
CPU_BUS_VSEL        5C3< 7A6<
CPU_CHKSTP_OUT_L    5B3<> 5C2< 39D8>
CPU_CHKS_L          5A3< 5D2<
CPU_CI_L            5A7> 8B6<> 36D5>
CPU_CLKOUT_SPN      5C3>
CPU_CLK_EN          8A6< 30C4<>
CPU_DATA<0>         6D8<> 8D4<>
CPU_DATA<0..31>     36D5>
CPU_DATA<1>         6D8<> 8D4<>
CPU_DATA<2>         6D8<> 8D4<>
CPU_DATA<3>         6D8<> 8D4<>
CPU_DATA<4>         6D8<> 8D4<>
CPU_DATA<5>         6D8<> 8D4<>
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CPU_DATA<8>         6D8<> 8D4<>
CPU_DATA<9>         6C8<> 8D4<>
CPU_DATA<10>        6C8<> 8D4<>
CPU_DATA<11>        6C8<> 8D4<>
CPU_DATA<12>        6C8<> 8C4<>
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CPU_DATA<30>        6C8<> 8C4<>
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CPU_DATA<32>        6C8<> 8C4<> 8D8<
CPU_DATA<32..63>    36D5>
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CPU_DATA<34>        6C8<> 8C4<> 8D8<
CPU_DATA<35>        6C8<> 8C4<> 8D8<
CPU_DATA<36>        6B8<> 8C4<> 8D8<
CPU_DATA<37>        6B8<> 8C4<> 8D8<
CPU_DATA<38>        6B8<> 8B4<> 8D8<
CPU_DATA<39>        6B8<> 8B4<> 8D8<
CPU_DATA<40>        6B8<> 8B4<> 8C8<
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CPU_DATA<42>        6B8<> 8B4<> 8C8<
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CPU_DATA<44>        6B8<> 8B4<> 8C8<
CPU_DATA<45>        6B8<> 8B4<> 8B8<
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CPU_DATA<47>        6B8<> 8B4<> 8B8<
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CPU_DATA<49>        6B8<> 8A8< 8B4<>
CPU_DATA<50>        6B8<> 8A8< 8B4<>
CPU_DATA<51>        6B8<> 8A8< 8B4<>
CPU_DATA<52>        6B8<> 8A8< 8B4<>
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CPU_DATA<58>        6B8<> 8B3< 8B4<>
CPU_DATA<59>        6B8<> 8B3< 8B4<>

CPU_DATA<60>        6B8<> 8B3< 8B4<>
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CPU_DATA<62>        6A8<> 8B3< 8B4<>
CPU_DATA<63>        6A8<> 8B3< 8B4<>
CPU_DBG_L           5C3< 8A4<> 8C2< 36D5>
CPU_DRDY_L          5C3> 8A4<> 8C2< 36D5>
CPU_DRDY_L_UF       36D5>
CPU_DTI<0>          5C3< 8A4<>
CPU_DTI<0..2>       36D5>
CPU_DTI<1>          5C3< 8A4<>
CPU_DTI<2>          5C3< 8A4<>
CPU_EDTI            5B2< 5C3<
CPU_EMODE0_L        5A3< 7A4<
CPU_EMODE1_L        5A3< 5C2<
CPU_GBL_L           5A7<> 8B6<> 36D5>
CPU_HIT_L           5A7> 8B6<> 8D2< 36D5>
CPU_HRESET_INV      7A7<>
CPU_HRESET_L        5B3< 5C2< 7A5< 7A8< 23A2<> 39C8>
CPU_L1TSTCLK        5B2< 5B3<
CPU_L2TSTCLK        5B3< 5C2<
CPU_LSSD_MODE       5B3< 5C2<
CPU_MCP_L           5B3< 5D2<
CPU_M_DM            25A8< 25B6<
CPU_M_DP            25B6< 25B8<
CPU_PLL_CFG<0>      5C3< 7D3<
CPU_PLL_CFG<1>      5C3< 7D3<
CPU_PLL_CFG<2>      5C3< 7D3<
CPU_PLL_CFG<3>      5C3< 7D3<
CPU_PLL_CFG<4>      5C3< 7D3<>
CPU_PLL_CFGEXT      7D4<>
CPU_PLL_FS00        7C4<>
CPU_PLL_FS01        7C4<
CPU_PLL_FS10        7C4<
CPU_PLL_STOP_BASE   7C7<
CPU_PLL_STOP_OC     7C4<> 7C8<> 30B6<>
CPU_PMONIN_L        5A3< 5C2<
CPU_PULLDOWN        5A2< 5A3< 5A3< 5C7<>
CPU_PULLUP          5A3< 5C2<
CPU_QACK_L          5B3< 8B6<> 36D5>
CPU_QREQ_L          5B3> 8B6< 8C2< 36D5>
CPU_SHD0_L          5A7<> 5D2<
CPU_SHD1_L          5A7<> 5D2<
CPU_SMI_L           5B3< 5C2< 30C4<>
CPU_SRESET_L        5B2< 5B3< 39C8>
CPU_SRWX_L          5A3< 5C2<
CPU_TA_L            5B3< 8A4<> 8D2< 36D5>
CPU_TBEN            5B3< 5D2< 8A6<>
CPU_TBST_L          5A7> 8B6<> 36D5>
CPU_TEA_L           5B3< 8A4<> 8C2< 36D5>
CPU_TSIZ<0>         5A7> 8B6<>
CPU_TSIZ<0..2>      36D5>
CPU_TSIZ<1>         5A7> 8B6<>
CPU_TSIZ<2>         5A7> 8B6<>
CPU_TS_L            5C7<> 8D2< 8D6<> 36D5>
CPU_TT<0>           5A7<> 8B6<>
CPU_TT<0..4>        36C5>
CPU_TT<1>           5A7<> 8B6<>
CPU_TT<2>           5A7<> 8B6<>
CPU_TT<3>           5A7<> 8B6<>
CPU_TT<4>           5A7<> 8B6<>
CPU_VCORE_HI_OC     7B8<> 30D4<> 34C8< 34D7<
CPU_VCORE_PWR_SEQ   34D8<>
CPU_VCORE_SEQ       34D8<
CPU_VCORE_SEQ_L     34D8<
CPU_VCORE_SLEEP     5C2< 5D8<> 34C1< 34D2< 38D3> 39B2>

CPU_VCORE_SLEEP_F   34C2<>
CPU_VCORE_SNUB      34B3<
CPU_WT_L            5A7> 8B6<> 36C5>
CSLOT_ADDR3_SPN     13B7>
CSLOT_ADDR4_SPN     13B7>
CSLOT_ADDR5_SPN     13B7>
CSLOT_ADDR6_SPN     13B7>
CSLOT_ADDR7_SPN     13B7>
CSLOT_ADDR8_SPN     13B7>
CSLOT_ADDR9_SPN     13B7>
CSLOT_CE1_L_SPN     13C7>
CSLOT_CE2_L_SPN     13C7>
CSLOT_IORD_L_SPN    13C7>
CSLOT_IOWAIT_L_PU   13C7<
CSLOT_IOWR_L_SPN    13C7>
CSLOT_OE_L_SPN      13C7>
CSLOT_WE_L_SPN      13C7>
CURRENT_THRESHOLD   31C4<
CY25811_S0          18B2<
CY25811_S1          18B2<
DCDC_EN             19A7<> 29C7<> 32B7<> 33B6<> 34C8<>
                  39C1>
DCDC_EN_L           33B6< 33B7<> 35C7<>
DDC_CLK_ISO         22D4<>
DDR_VREF            11D1< 11D3<> 11D5<> 11D6<> 11D8<>
                  38D3>
DVI_DDC_CLK         22D4<>
DVI_DDC_CLK_UF      22C5<> 22D3<> 39C7>
DVI_DDC_DATA        22C4<>
DVI_DDC_DATA_UF     22C5<> 39C7>
DVI_HPD             22C4<>
DVI_HPD_DIV         22C3<
DVI_HPD_UF          22C3< 22C5<> 39C7>
DVI_TRUN_ON_ILIM    22D2<
DVI_TURN_ON         22D3<>
DVI_TURN_ON_BASE    22D2<
EEPROM_ADDR         23D4<
EEPROM_WP_PD        23D3<>
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EIDE_ADDR<2..0>     37B5>
EIDE_ADDR<1>        13B7> 24B8<
EIDE_ADDR<2>        13B7> 24B8<
EIDE_CS0_L          13B7> 24B8< 37B5>
EIDE_CS1_L          13B7> 24B8< 37B5>
EIDE_DATA<0>        13C7<> 24C8<
EIDE_DATA<15..0>    37B5>
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EIDE_DATA<5>        13B7<> 24B8<
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EIDE_DATA<8>        13B7<> 24D8<
EIDE_DATA<9>        13B7<> 24D8<
EIDE_DATA<10>       13B7<> 24D8<
EIDE_DATA<11>       13B7<> 24D8<
EIDE_DATA<12>       13B7<> 24D8<
EIDE_DATA<13>       13B7<> 24C8<
EIDE_DATA<14>       13B7<> 24C8<
EIDE_DATA<15>       13B7<> 24C8<
EIDE_DMACK_L        13A7<> 24A8< 37B5>
EIDE_DMARQ          13A7< 24B8< 37B5>
EIDE_INT            13A7< 24A8< 37B5>
EIDE_IOCHRDY        13B7< 24A8< 37B5>
EIDE_OPTICAL_ADDR<0>  24A5<> 24B7< 39A4>
EIDE_OPTICAL_ADDR<2..0>  37B5>
EIDE_OPTICAL_ADDR<1>  24A5<> 24B7< 39A4>
EIDE_OPTICAL_ADDR<2>  24A6<> 24B7< 39A4>
EIDE_OPTICAL_CS0_L  24A5<> 24B7< 37B5> 39D4>
EIDE_OPTICAL_CS1_L  24A6<> 24B7< 37B5> 39D4>
EIDE_OPTICAL_DATA<0>  24A5<> 24C7< 39C4>
EIDE_OPTICAL_DATA<15..0>  37B5>
EIDE_OPTICAL_DATA<1>  24A5<> 24C7< 39C4>
EIDE_OPTICAL_DATA<2>  24A5<> 24C7< 39C4>
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EIDE_OPTICAL_DATA<9>  24A6<> 24D7< 39B4>
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EIDE_OPTICAL_DATA<11>  24A6<> 24D7< 39B4>
EIDE_OPTICAL_DATA<12>  24A6<> 24D7< 39B4>
EIDE_OPTICAL_DATA<13>  24A6<> 24C7< 39B4>
EIDE_OPTICAL_DATA<14>  24A6<> 24C7< 39B4>
EIDE_OPTICAL_DATA<15>  24A6<> 24C7< 39B4>
EIDE_OPTICAL_DMAACK_L  24A6<> 24A7< 37A5> 39A4>
EIDE_OPTICAL_DMA_RQ  24A6<> 24B7< 37A5> 39A4>
EIDE_OPTICAL_INT    24A5<> 24A7< 37A5> 39D4>
EIDE_OPTICAL_IOCHRDY  24A5<> 24A7< 37A5> 39D4>
EIDE_OPTICAL_RD_L   24A6<> 24A7< 37B5> 39A4>
EIDE_OPTICAL_RST_L  24A7< 24B5<> 37A5> 39D4>
EIDE_OPTICAL_WR_L   24A5<> 24A7< 37A5> 39D4>
EIDE_RD_L           13A7> 24A8< 37B5>
EIDE_RST_L          13B7> 24A8< 37B5>
EIDE_WR_L           13A7> 24A8< 37B5>
ENET_COL            13C5< 27B7> 37A5>
ENET_COMA           27B7<>
ENET_CRS            13C5< 27B7> 37A5>
ENET_CTAP_CHGND     27A1< 38A6>

ENET_ENERGY_DET     14B5<> 27B7<>
ENET_HSDACM         27A7<>
ENET_HSDACP         27A7<>
ENET_LINK_RXD<0>    13C5< 27C7>
ENET_LINK_RXD<7..0>  37A5>
ENET_LINK_RXD<1>    13C5< 27C7>
ENET_LINK_RXD<2>    13C5< 27C7>
ENET_LINK_RXD<3>    13C5< 27B7>
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ENET_LINK_RXD<7>    13C5< 27B7>
ENET_LINK_TXD<0>    13B4< 13D5>
ENET_LINK_TXD<7..0>  37A5>
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ENET_LINK_TXD<2>    13B4< 13D5>
ENET_LINK_TXD<3>    13B4< 13D5>
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ENET_LINK_TXD<5>    13B4< 13D5>
ENET_LINK_TXD<6>    13A4< 13D5>
ENET_LINK_TXD<7>    13A4< 13D5>
ENET_LINK_TX_EN     13D5<> 37A5>
ENET_LINK_TX_ER     13D5<> 37A5>
ENET_MDC            13C5> 27B7< 37A5>
ENET_MDIO           13C5<> 27B7<> 37A5>
ENET_PHY_TXD<0>     13B5> 27C7<
ENET_PHY_TXD<7..0>  37A5>
ENET_PHY_TXD<1>     13B5> 27C7<
ENET_PHY_TXD<2>     13B5> 27C7<
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ENET_PHY_TXD<5>     13B5> 27C7<
ENET_PHY_TXD<6>     13A5> 27C7<
ENET_PHY_TXD<7>     13A5> 27C7<
ENET_PHY_TX_EN      13D6> 27C7< 37A5>
ENET_PHY_TX_ER      13D6> 27C7< 37A5>
ENET_RSET           27A5<
ENET_RST_L          27B7<
ENET_RX_DV          13D5< 27B7> 37A5>
ENET_RX_ER          13C5< 27B7> 37A5>
ENET_VSSC           27A7<>
EXT_SWING           20A5<>
FANL_GND            25A3<> 38B6> 39B3>
FANL_PWM            25A3<> 25B2<> 39B3>
FANL_TACH           25A3<> 25B2< 39B3>
FANR_GND            25B2<> 38B6> 39B3>
FANR_PWM            25A2<> 25B1<> 39B3>
FANR_TACH           25B2< 25B2<>
FB_4_85V_BU         32A5<
FP_PWR_EN           19C6<> 22A6< 22B3<>
FP_PWR_EN_L         22B3<>
FWB_TPB0            28A3<
FWB_TPB1            28A4<
FWPLL_BYP           28C8<>
FW_BIAS0            28A5<>
FW_BIAS1            28A5<>
FW_BMODE            28B7<
FW_CORE_ADJ         28C8<
FW_CORE_BYP         28C7<>
FW_CPS              28B7<
FW_INPUT_PD         28A7<
FW_LINK_CNTL<0>     13C3<> 28C3<
FW_LINK_CNTL<1..0>  37A5>
FW_LINK_CNTL<1>     13C3<> 28C3<
FW_LINK_DATA<0>     13D3<> 28B8<
FW_LINK_DATA<7..0>  37A5>
FW_LINK_DATA<1>     13D3<> 28B8<
FW_LINK_DATA<2>     13D3<> 28B8<
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FW_LINK_DATA<4>     13C3<> 28A8<
FW_LINK_DATA<5>     13C3<> 28A8<
FW_LINK_DATA<6>     13C3<> 28A8<
FW_LINK_DATA<7>     13C3<> 28A8<
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FW_LKON             13C3<> 28B5<>
FW_OSC              28A4<> 36A1>
FW_OSC_EN           28A3<
FW_PC_PD            28B7<
FW_PC_PU            28B7<
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FW_PHY_CNTL<1..0>   37A5>
FW_PHY_CNTL<1>      28B4<> 28C3<
FW_PHY_DATA<0>      28B8<>
FW_PHY_DATA<7..0>   37A5>
FW_PHY_DATA<1>      28B8<>
FW_PHY_DATA<2>      28B8<>
FW_PHY_DATA<3>      28A8<>
FW_PHY_DATA<4>      28A8<>
FW_PHY_DATA<5>      28A8<>
FW_PHY_DATA<6>      28A8<>
FW_PHY_DATA<7>      28A8<>
FW_PHY_LPS          13C3<> 28B8<
FW_PHY_LREQ         13C2< 28B8< 37A5>
FW_PHY_PD           14C5< 28B8<
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FW_R1               28A5<>
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FW_TPA0P            28B1<> 29C4<> 37D2>
FW_TPA0P_CONN       29C3<>
FW_TPA1N            28B1<> 29A4<> 37C2>
FW_TPA1P            28B1<> 29A4<> 37C2>
FW_TPB0N            28B1<> 29C4<> 37D2>
FW_TPB0N_CONN       29C3<>
FW_TPB0P            28B1<> 29C4<> 37D2>
FW_TPB0P_CONN       29C3<>
FW_TPB1N            28B1<> 29A4<> 37C2>
FW_TPB1P            28B1<> 29A4<> 37C2>
FW_TPB2_PD          28A5<>
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FW_TPI0P            37C2>
FW_TPI1N            29A3<> 37C2> 39D2>
FW_TPI1P            29A3<> 37C2> 39D2>
FW_TPO0N            37C2>
FW_TPO0P            37C2>
FW_TPO0R            29C2<> 38A3> 39A3>
FW_TPO1N            29A3<> 37C2> 39D2>
FW_TPO1P            29A3<> 37C2> 39D2>
FW_VGND0            29C2<> 38A3>
FW_VGND1            29A3<> 38A3>
FW_VREG_PD          28A7<
FW_XI               28A5<> 36A1>
GAIN_SETTING2       23C7<>
GPU_AGP_TEST        18D6<
GPU_AUXWIN          19C5<>
GPU_B               19D6<> 22D8<
GPU_C               19D6<> 22A8<
GPU_CLK27M_OUT      36C1>
GPU_CLK27M_UF       36C1>
GPU_COMP            19D6<> 22A8<
GPU_CORE_OK         19A6<> 19D4<> 21D2<> 21D7<>
GPU_DVI_DDC_CLK     19C5<> 22D3<>
GPU_DVI_DDC_DATA    19C5<> 22C3<>
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GPU_DVOD<0..11>     37D5>
GPU_DVOD<1>         19D7<> 20B7<
GPU_DVOD<2>         19D7<> 20B7<
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GPU_DVOD<9>         19D7<> 20A7<
GPU_DVOD<10>        19D7<> 20A7<
GPU_DVOD<11>        19D7<> 20A7<
GPU_DVOD_DE         19C7<> 20A7<
GPU_DVO_CLKP        19C7<> 20A7< 36B1>
GPU_DVO_HSYNC       19C7<> 20A7< 37C5>
GPU_DVO_VSYNC       19C7<> 20A7< 37C5>
GPU_FBCLK0          36B1>
GPU_FBCLK0_L        36B1>
GPU_FBCLK1          36B1>
GPU_FBCLK1_L        36B1>
GPU_G               19D6<> 22D8<
GPU_HPD             19C5<> 22C3<>
GPU_MEM_IO          38C3>
GPU_MEM_IO_FLT      21C2< 38C3>
GPU_R               19D6<> 22D8<
GPU_SSCLK_IN        36B1>

GPU_SSCLK_UF        36C1>
GPU_THERM_DM        18A6<>
GPU_THERM_DP        18A6<>
GPU_TV_GND1         22B8<> 38B6>
GPU_TV_GND2         22A8<> 38B6>
GPU_VCORE           18A6<> 19A3<> 19B5<> 19D4< 38C3>
                  39B2>
GPU_VCORE_CNTL      19A3<>
GPU_VCORE_CNTL_L    19A4< 19B7<>
GPU_VCORE_NECK      19B5<> 38B3>
GPU_VCORE_PWR_SEQ   19A8<>
GPU_VCORE_SEQ       19A8<
GPU_VCORE_SEQ_L     19A8<
GPU_VCORE_SW        19A4<> 38B1>
GPU_VCORE_VDDCI     18A5< 38C3>
GPU_Y               19D6<> 22B8<
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HD_ADDR<2..0>       37C5>
HD_ADDR<1>          24C2<> 24C3<
HD_ADDR<2>          24B3< 24C1<>
HD_CS0_L            24C2<> 24C3< 37B5>
HD_CS1_L            24B3< 24C1<> 37B5>
HD_DATA<0>          24C2<> 24D3<
HD_DATA<15..0>      37C5>
HD_DATA<1>          24C2<> 24D3<
HD_DATA<2>          24D2<> 24D3<
HD_DATA<3>          24D2<> 24D3<
HD_DATA<4>          24C3< 24D2<>
HD_DATA<5>          24C3< 24D2<>
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HD_DATA<7>          24C3< 24D2<>
HD_DATA<8>          24C3< 24D1<>
HD_DATA<9>          24C3< 24D1<>
HD_DATA<10>         24C3< 24D1<>
HD_DATA<11>         24D1<> 24D3<
HD_DATA<12>         24B3< 24D1<>
HD_DATA<13>         24B3< 24D1<>
HD_DATA<14>         24C1<> 24C3<
HD_DATA<15>         24B3< 24C1<>
HD_DIOR_L           24A3< 24C2<> 37B5>
HD_DIOW_L           24A3< 24C1<> 37B5>
HD_DMACK_L          24A3< 24C2<> 37B5>
HD_DMARQ            13C6< 24C2<> 37B5>
HD_INTRQ            13C6< 24C1<> 37B5>
HD_IOCHRDY          24A3< 24C1<> 37B5>
HD_RESET_L          24A3< 24D2<> 37B5>
HIGH_VCORE          19A2<>
HIGH_VCORE_DIV      19A3<
HPD_4V_REF          22C3<
HPD_BASE            22C1<
HPD_ON              22C2<>
HPD_ON_RC           22C2<
HPD_PWR_SNS_EN      19C7<> 22C3<>
HPD_PWR_SW          22C2<>
IAC_FB              31D4<
IAC_RC_COMP         31D4<
INTREPID_ACS_REF    8A6<
INT_AGPPVT          12D4<>
INT_AGP_FB_IN       12C4< 36C1>
INT_AGP_FB_OUT      12C4<> 36C1>
INT_AGP_VREF        12B4< 12D4<> 18D5< 38D3>
INT_AUDIO_TO_SND    14B2< 25D8< 39C6>
INT_AUDIO_TO_SND_F  25D7<> 25D7<
INT_CPUFB_IN        8A6< 8B6< 36D1>
INT_CPUFB_IN_NORM   8A4< 36D1>
INT_CPUFB_LONG      8A4< 36D1>
INT_CPUFB_OUT       8A6< 8A6<> 36D1>
INT_CPUFB_OUT_NORM  8A4< 36D1>
INT_CPUFB_OUT_SHORT  8A5< 36D1>
INT_DDRCLK2_N_TP    9B6<>
INT_DDRCLK2_P_TP    9B6<>
INT_DDRCLK5_N_TP    9B6<>
INT_DDRCLK5_P_TP    9B6<>
INT_ENET_RST_L      14B5<> 27B8<
INT_EXTINT3_PU      14B5<> 14B7<
INT_EXTINT8_PU      14B5<> 14C7<
INT_EXTINT10_PU     14A7< 14B5<>
INT_EXTINT11_PU     14A7< 14B5<>
INT_EXTINT12_PU     14A7< 14B5<>
INT_EXTINT13_PU     14B5<> 14B7<
INT_EXTINT14_PU     14B5<> 14C7<
INT_EXTINT16_PU     14B5<> 14B7<
INT_GPIO1_PU        14C5<> 14C7< 34C8<
INT_GPIO9_PU        14A7< 14B5<>
INT_GPIO12_PU       14B5<> 14B7<
INT_GPIO15_PU       14B5<> 14C7<
INT_I2C_CLK0        11A3<> 11A8<> 13C2< 13C3<> 23D2<
                  23D4<> 39B8>
INT_I2C_CLK1        13C2< 13C3<> 14B7< 25B4< 39B8>
INT_I2C_CLK2        14A2<> 25C4<> 25D7<> 39C6>
INT_I2C_DATA0       11A3<> 11A8<> 13C2< 13C3<> 23D2<>
                  23D4<> 39B8>
INT_I2C_DATA1       13B2< 13C3<> 14B7< 25B4<> 39B8>
INT_I2C_DATA2       14A2<> 25C4<> 25C7<> 39C6>
INT_JTAG_TEI        13C2< 13C5<
INT_MEM_REF_H       9B6< 38D3>
INT_MEM_VREF        9A7< 9B6<> 38D3>
INT_MOD_BITCLK_UF   14A3<> 14A7<
INT_MOD_CLKOUT_UF   14A3<> 14B7<
INT_MOD_DTI         14A2< 25C3<> 39B1>
INT_MOD_DTI_UF      14A7<
INT_MOD_DTO_UF      14A3<> 14B7<
INT_MOD_SYNC_UF     14A3<> 14A7<
INT_PCI_FB_IN       12C7< 36C1>
INT_PCI_FB_OUT      12C7<> 36C1>
INT_PEND_PROC_INT   14A5> 30C4<>
INT_PROC_SLEEP_REQ_L  14A5< 30B4<>
INT_PU_RESET_L      13D3< 25D4<> 30A2< 30C4<>
INT_REF_CLK_IN      14A5< 14B5< 36C1>
INT_REF_CLK_OUT     14A5> 14B7< 36C1>
INT_RESET_L         9B3< 13D3< 30C7< 30D4<>
INT_ROM_CS_L        12A6< 12C7>
INT_ROM_OE_L        12A6< 12C7>
INT_ROM_RW_L        12A6< 12C7>
INT_SND_CLKOUT      14A3<>
INT_SND_SCLK        14A3<>
INT_SND_SYNC        14B3<>
INT_SND_TO_AUDIO    14B3<>
INT_SUSPEND_ACK_L   8B6> 30B6<>
INT_SUSPEND_REQ_L   8B6< 30B6<> 30C7<
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INT_TST_MONOUT_TP   13C5>
INT_TST_PLLEN_PD    13C5< 13D2<
INT_WATCHDOG_L      14A5> 30C6<>
INV_ON_PWM          19C6<> 22A3<
IO_RESET_L          17A7< 23D6< 26B8< 27B8< 30C6<>
                  30D7<
JTAG_ASIC_TCK       13C5< 13D2< 27A5< 39D8>
JTAG_ASIC_TDI       13C5< 13D2< 39D8>
JTAG_ASIC_TDO_TP    27A5> 39D8>
JTAG_ASIC_TMS       13C5< 13D2< 27A5< 39D8>
JTAG_ASIC_TRST_L    13C2< 13C5< 27A5< 39D8>
JTAG_CPU_TCK        5B2< 5B3< 23B2> 39C8>
JTAG_CPU_TDI        5B2< 5C3< 23D4<> 39C8>
JTAG_CPU_TDO_TP     5C3> 39C8>
JTAG_CPU_TMS        5B2< 5B3< 23C4<> 39C8>
JTAG_CPU_TRST_L     5A3< 5B3< 23D4<> 39B1> 39C8>
JTAG_ENET_TDI       13C5> 13D2< 27A5<
KBD_CAPSLOCK_LED    23A7<> 39B4>
KBD_COMMAND_L       23A5< 23A7<> 30C6<> 39B4>
KBD_CONTROL_L       23A5< 23A7<> 30A8< 30C6<> 39B4>
KBD_FUNCTION_L      23A5< 23A7<> 30B6<> 39B4>
KBD_ID              23A7<> 23B5< 30B6<> 39C4>
KBD_LED1_OUT        23A5<> 23A7<> 38B6> 39C2>
KBD_LED2_OUT        23A5<> 23A7<> 38B6> 39C2>
KBD_LED_EN          23A5<>
KBD_LED_SET         23A5<
KBD_NUMLOCK_LED     23B7<> 39C3>
KBD_OPTION_L        23A5< 23B7<> 30A8< 30B6<> 39B4>
KBD_SHIFT_L         23A5< 23B7<> 30A8< 30C6<> 39B4>
KBD_X<0>            23A5< 23B7<> 30C6<> 39B4>
KBD_X<1>            23A5< 23B7<> 30C6<> 39B4>
KBD_X<2>            23B5< 23B7<> 30C6<> 39B4>
KBD_X<3>            23B5< 23B7<> 30C6<> 39A4>
KBD_X<4>            23B5< 23B7<> 30C6<> 39A4>
KBD_X<5>            23B5< 23B7<> 30C6<> 39A4>
KBD_X<6>            23B5< 23B7<> 30C6<> 39A4>
KBD_X<7>            23B5< 23B7<> 30C6<> 39A4>
KBD_X<8>            23B5< 23B7<> 30C6<> 39A4>
KBD_X<9>            23B5< 23B7<> 30C6<> 39D3>
KBD_Y<0>            23B7<> 30D6<> 39D3>
KBD_Y<1>            23B7<> 30D6<> 39D3>
KBD_Y<2>            23B7<> 30D6<> 39D3>
KBD_Y<3>            23B7<> 30D6<> 39D3>
KBD_Y<4>            23B7<> 30D6<> 39D3>
KBD_Y<5>            23B7<> 30D6<> 39D3>
KBD_Y<6>            23B7<> 30C6<> 39C3>
KBD_Y<7>            23B7<> 30C6<> 39C3>

LCD_DIGON_L         22A6<
LCD_PWREN_L         22A5<>
LED_LINK10          27B5<>
LED_LINK100         27B5<>
LED_RX_SPN          27B5>
LEFT_USB_DM         24B2<> 26B3< 37A2> 39D1>
LEFT_USB_DP         24B2<> 26A3< 37A2> 39D1>
LID_CLOSED_L        23A7<> 39C4>
LM2594_IN           28D8<> 38B3>
LT1962_INT_ADJ      14D6<
LT1962_INT_BYP      14D6<>
LTC1625_ITH         31D3<>
LTC1962_1V5_VIN     38A1>
LTC1962_1V5_VOUT    38A1>
LTC1962_INT_VIN     14D7<> 38A1>
LTC1962_L3_VIN      38A1>
LTC1962_L3_VOUT     38A1>
LTC3405_SW          27D4<> 38B3>
LTC3411_GND         38A1>
LTC3411_ITH         38A1>
LTC3411_ITH_RC      38A1>
LTC3411_SHDN        38A1>
LTC3411_SYNC        38A1>
LTC3411_VCC         38B1>
LTC3412_GND         35A6<>
LTC3412_ITH         35A6<>
LTC3412_ITH_RC      35A6<
LTC3412_PGOOD       35A4<>
LTC3412_RT          35A6<
LTC3412_RUNSS       35A6<>
LTC3412_SYNC        35A6<>
LTC3412_VFB         35A6<>
LTC3412_VFB_DIV     35A6<
LTC3707_START_RC    33B6<>
LVDS_DDC_CLK        19C5<> 22B5<> 39A7>
LVDS_DDC_DATA       19C5<> 22B5<> 39A7>
LVDS_L0N            19B5> 22B4<> 37C2> 39C7>
LVDS_L0P            19B5> 22B4<> 37C2> 39C7>
LVDS_L1N            19B5> 22B4<> 37C2> 39C7>
LVDS_L1P            19B5> 22B4<> 37C2> 39C7>
LVDS_L2N            19B5> 22B4<> 37C2> 39C7>
LVDS_L2P            19B5> 22B4<> 37C2> 39C7>
LVDS_L3N_TP         19B5>
LVDS_L3P_TP         19B5>
LVDS_U0N            19C5> 22A4<> 37C2> 39B7>
LVDS_U0P            19C5> 22A4<> 37C2> 39B7>
LVDS_U1N            19C5> 22A4<> 37C2> 39B7>
LVDS_U1P            19C5> 22A4<> 37C2> 39B7>
LVDS_U2N            19B5> 22A4<> 37B2> 39B7>
LVDS_U2P            19B5> 22A4<> 37B2> 39B7>
LVDS_U3N_TP         19B5>
LVDS_U3P_TP         19B5>
MAIN_RESET_L        14C7< 17A7< 17D5< 18C8< 20B8<
                  24D6<> 26B8< 30D4<> 30D7< 39C1>
MAX1715_FB2         35B1< 35B4<
MAX1715_GND         35B5<> 35C5< 38C1>
MAX1715_ON_RC       35C7<>
MAX1715_REF         35B5<> 38C1>
MAX1715_SKIP        35C4< 38C1>
MAX1715_TON         35C5< 38C1>
MAX1715_VCC         35D5< 38C1>
MAX1717_AB_SEL      34A7< 34C6<
MAX4172_OUT         31D4<>
MAXBUS_SLEEP        5A2< 5D1< 5D5< 7B7< 7D8< 8B8< 8C3<
                  8C8< 8D1< 8D8< 15D8< 16D8< 23B3<
                  23B3< 34D8< 38D3>
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MDI1_PD             27B4<
MDI2_PD             27B4<
MDI3_PD             27B3<
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MDI_P<2>            27B5<> 37D2>
MDI_P<3>            27B5<> 37D2>
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MEM_ADDR<12..0>     36A5>
MEM_ADDR<1>         9B5< 9D6<>
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MEM_ADDR<3>         9B5< 9D6<>
MEM_ADDR<4>         9B5< 9D6<>
MEM_ADDR<5>         9B5< 9D6<>
MEM_ADDR<6>         9B5< 9D6<>
MEM_ADDR<7>         9B5< 9D6<>
MEM_ADDR<8>         9B5< 9D6<>
MEM_ADDR<9>         9A5< 9D6<>
MEM_ADDR<10>        9A5< 9D6<>
MEM_ADDR<11>        9A5< 9D6<>
MEM_ADDR<12>        9A5< 9D6<>
MEM_BA<0>           9A5< 9D6<>
MEM_BA<1..0>        36A5>
MEM_BA<1>           9A5< 9C6<>
MEM_CAS_L           9A5< 9C6<> 36A5>
MEM_CKE<0>          9B6<> 9C5<
MEM_CKE<3..0>       36A5>
MEM_CKE<1>          9B6<> 9C5<
MEM_CKE<2>          9B6<> 9C5<
MEM_CKE<3>          9B6<> 9C5<
MEM_CS_L<0>         9C5< 9C6<>
MEM_CS_L<3..0>      36A5>
MEM_CS_L<1>         9C5< 9C6<>
MEM_CS_L<2>         9C5< 9C6<>
MEM_CS_L<3>         9C5< 9C6<>
MEM_DATA<0>         9D8<> 10C7<>
MEM_DATA<7..0>      36C5>
MEM_DATA<1>         9D8<> 10C7<>
MEM_DATA<2>         9D8<> 10C7<>
MEM_DATA<3>         9D8<> 10C7<>
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MEM_DATA<5>         9D8<> 10C7<>
MEM_DATA<6>         9D8<> 10C7<>
MEM_DATA<7>         9D8<> 10C7<>
MEM_DATA<8>         9D8<> 10C7<>
MEM_DATA<15..8>     36C5>
MEM_DATA<9>         9D8<> 10C7<>
MEM_DATA<10>        9D8<> 10C7<>
MEM_DATA<11>        9D8<> 10C7<>
MEM_DATA<12>        9D8<> 10B7<>
MEM_DATA<13>        9C8<> 10B7<>
MEM_DATA<14>        9C8<> 10B7<>
MEM_DATA<15>        9C8<> 10B7<>
MEM_DATA<16>        9C8<> 10C5<>
MEM_DATA<31..16>    36C5>
MEM_DATA<17>        9C8<> 10C5<>
MEM_DATA<18>        9C8<> 10C5<>
MEM_DATA<19>        9C8<> 10C5<>
MEM_DATA<20>        9C8<> 10C5<>
MEM_DATA<21>        9C8<> 10C5<>
MEM_DATA<22>        9C8<> 10C5<>
MEM_DATA<23>        9C8<> 10C5<>
MEM_DATA<24>        9C8<> 10C5<>
MEM_DATA<25>        9C8<> 10C5<>
MEM_DATA<26>        9C8<> 10C5<>
MEM_DATA<27>        9C8<> 10C5<>
MEM_DATA<28>        9C8<> 10C5<>
MEM_DATA<29>        9C8<> 10B5<>
MEM_DATA<30>        9C8<> 10B5<>
MEM_DATA<31>        9C8<> 10B5<>
MEM_DATA<32>        9C8<> 10C3<>
MEM_DATA<47..32>    36B5>
MEM_DATA<33>        9C8<> 10C3<>
MEM_DATA<34>        9C8<> 10C3<>
MEM_DATA<35>        9C8<> 10C3<>
MEM_DATA<36>        9C8<> 10C3<>
MEM_DATA<37>        9C8<> 10C3<>
MEM_DATA<38>        9C8<> 10C3<>
MEM_DATA<39>        9B8<> 10C3<>
MEM_DATA<40>        9B8<> 10C3<>
MEM_DATA<41>        9B8<> 10C3<>
MEM_DATA<42>        9B8<> 10C3<>
MEM_DATA<43>        9B8<> 10C3<>
MEM_DATA<44>        9B8<> 10C3<>
MEM_DATA<45>        9B8<> 10B3<>
MEM_DATA<46>        9B8<> 10B3<>
MEM_DATA<47>        9B8<> 10B3<>
MEM_DATA<48>        9B8<> 10C1<>
MEM_DATA<55..48>    36B5>
MEM_DATA<49>        9B8<> 10C1<>
MEM_DATA<50>        9B8<> 10C1<>
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MEM_DATA<52>        9B8<> 10C1<>
MEM_DATA<53>        9B8<> 10C1<>
MEM_DATA<54>        9B8<> 10C1<>
MEM_DATA<55>        9B8<> 10C1<>
MEM_DATA<56>        9B8<> 10C1<>

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MEM_DATA<58>        9B8<> 10C1<>
MEM_DATA<59>        9B8<> 10C1<>
MEM_DATA<60>        9B8<> 10C1<>
MEM_DATA<61>        9B8<> 10B1<>
MEM_DATA<62>        9B8<> 10B1<>
MEM_DATA<63>        9B8<> 10B1<>
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MEM_DQM<1>          9C6<> 10B7<> 36C5>
MEM_DQM<2>          9C6<> 10C5<>
MEM_DQM<3..2>       36B5>
MEM_DQM<3>          9C6<> 10B5<>
MEM_DQM<4>          9C6<> 10C3<>
MEM_DQM<5..4>       36B5>
MEM_DQM<5>          9C6<> 10B3<>
MEM_DQM<6>          9C6<> 10C1<> 36B5>
MEM_DQM<7>          9C6<> 10B1<> 36A5>
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MEM_DQS<1>          9C6<> 10B7<> 36C5>
MEM_DQS<2>          9C6<> 10C5<>
MEM_DQS<3..2>       36B5>
MEM_DQS<3>          9C6<> 10B5<>
MEM_DQS<4>          9C6<> 10C3<>
MEM_DQS<5..4>       36B5>
MEM_DQS<5>          9C6<> 10B3<>
MEM_DQS<6>          9C6<> 10C1<> 36B5>
MEM_DQS<7>          9C6<> 10B1<> 36A5>
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MEM_MUXSEL_H<1>     9B6<> 10A4<
MEM_MUXSEL_L<0>     9B6<> 10A6<
MEM_MUXSEL_L<1..0>  36A5>
MEM_MUXSEL_L<1>     9B6<> 10A4<
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MEM_WE_L            9A5< 9C6<> 36A5>
MLB_ALS_GAIN_SW     23C4<> 23C8<>
MLB_ALS_OP_COMP     23D7<
MLB_ALS_OP_IN       23D7<
MLB_ALS_OUT         23C4<> 23D6<
MLB_ALS_OUT_FB      23D7<>
MLB_PHOTODIODE      23D8<>
MODEM_USB_DM        14B1< 25C3<> 37A2> 39B6>
MODEM_USB_DP        14B1< 25C3<> 37A2> 39B6>
MOD_BITCLK          14A2< 25C3<> 39B1>
MOD_CLKOUT          14A2< 25C4<> 39A1>
MOD_DTO             14A2< 25C4<> 39A1>
MOD_SYNC            14A2< 25C3<> 39A1>
MPIC_CPU_INT_L      5B2< 5B3< 14B5>
NEC_AMC_TP          26A5<
NEC_AVDD            26D6< 38A3>
NEC_AVSS_F          26A5< 26B4<
NEC_CRUN_L          26A7<>
NEC_IDSEL           26B7<
NEC_IO_RESET_L      26B7< 26B7<
NEC_LEFT_USB_OVERCURRENT  24B2<> 26C1< 39D1>
NEC_LEFT_USB_PWREN  24B2<> 26B5<> 39D1>
NEC_LEGC            26A7<
NEC_MAIN_RESET_L    26A7< 26B7<
NEC_NANDTESTEN_TP   26A5<
NEC_NANDTESTOUT_TP  26A4<>
NEC_NC1_TP          26B5<>
NEC_NC2_TP          26B5<>
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NEC_PCI_INTA_L      26A7< 26B7>
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NEC_PCI_PERR_L      26B7<> 26C8<
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NEC_PME_L           26A7> 26B7<
NEC_PPON3_TP        26B5>
NEC_PPON4_TP        26B5>
NEC_PPON5_TP        26B5>
NEC_RIGHT_USB_OVERCURRENT  26C1< 32A7<> 39C1>
NEC_RIGHT_USB_PWREN  26B5<> 32A7<> 39C1>
NEC_RREF            26B5<>
NEC_SMI_L_TP        26A7>
NEC_USB_DAM         26B4< 26C3<> 37B2>
NEC_USB_DAP         26A4< 26C3<> 37B2>
NEC_USB_DBM         26A4< 26C3<> 37B2>
NEC_USB_DBP         26A4< 26C3<> 37B2>
NEC_USB_RSDM1       26C5<> 37B2>
NEC_USB_RSDM2       26C5<> 37B2>
NEC_USB_RSDP1       26C5<> 37B2>
NEC_USB_RSDP2       26C5<> 37B2>
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NEC_XT2             26D5<> 36B1>
NEC_XT2_R           26D4<
NTEST1_TP           26B5<
NUMLOCK_LED         23B8<
NUMLOCK_LED_L       23B8< 30C7<
OVER_18V_ADJ        31C3<>
PCI1510_VR_EN_L     17C7<
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                  39B6>
PCI_AD<31..0>       37C5>
PCI_AD<1>           9C3< 12D6<> 17C7<> 24B6<> 26D7<>
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PCI_AD<2>           9C3< 12D6<> 17C7<> 24C5<> 26D7<>
                  39A6>
PCI_AD<3>           9C3< 12D6<> 17C7<> 24C6<> 26C7<>
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PCI_AD<4>           9C3< 12D6<> 17C7<> 24C5<> 26C7<>
                  39A6>
PCI_AD<5>           9C3< 12D6<> 17C7<> 24C6<> 26C7<>
                  39A6>
PCI_AD<6>           9C3< 12C6<> 17C7<> 24C5<> 26C7<>
                  39A6>
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PCI_AD<10>          9C3< 12C6<> 17C7<> 24C6<> 26C7<>
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PCI_AD<19>          9C3< 12C6<> 17B7<> 24C6<> 26C7<>
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PCI_AD<20>          9B3< 12C6<> 17B7<> 24C5<> 26C7<>
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PCI_AD<21>          12C6<> 17B7<> 24C6<> 26C7<> 39C5>
PCI_AD<22>          12C6<> 17B7<> 24C5<> 26C7<> 39B5>
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PCI_AD<24>          9C1<> 12C6<> 17B7<> 24C5<> 26C7<>
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PCI_AD<25>          9C1<> 12C6<> 17B7<> 24C6<> 26C7<>
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PCI_AD<26>          9C1<> 12C6<> 17B7<> 24C5<> 26C7<>
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PCI_AD<27>          9C1<> 12C6<> 17B7<> 24D6<> 26C8<>
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PCI_AD<28>          9C1<> 12C6<> 17B7<> 24C5<> 26C7<>
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PCI_AD<29>          9C1<> 12C6<> 17B7<> 24D6<> 26B7<>
                  39B5>
PCI_AD<30>          9C1<> 12C6<> 17B7<> 24D5<> 26B7<>
                  39B5>
PCI_AD<31>          9C1<> 12C6<> 17B7<> 24D6<> 26B7<>
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PCI_CBE<0>          12C7<> 17B7<> 24C5<> 26B7<> 39D4>
PCI_CBE<3..0>       37C5>
PCI_CBE<1>          12C7<> 17B7<> 24C6<> 26B7<> 39D4>
PCI_CBE<2>          12C7<> 17B7<> 24C6<> 26B7<> 39D4>
PCI_CBE<3>          12C7<> 17B7<> 24C6<> 26B7<> 39D4>
PCI_DEVSEL_L        12B7< 12C7<> 17A7<> 24C5<> 26B7<>
                  37C5> 39A5>
PCI_FRAME_L         12B7< 12C7<> 17B7<> 24C5<> 26B7<>
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                  39D4>
PCI_STOP_L        12A7< 12C7<> 17B7<> 24C5<> 26B7<>
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PCI_TRDY_L        12B7< 12C7<> 17A7<> 24C5<> 26B7<>
                  37C5> 39A5>
PLL_STOP_L        7C4<> 7C8<>
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PMU_AC_DET        30A4< 30B4<>
PMU_AC_IN         30B4<>
PMU_BATT0_DET_L   30B4<>
PMU_BATT1_DET_L_PU  30B4<> 30D2<
PMU_BATT_DET_L    30B3> 30D2< 31A4<> 39C3>
PMU_BYTE          30B6< 30C7<>
PMU_CAPSLOCK_LED_L  30C6<>
PMU_CHARGE_V      30C4<> 31B8<>
PMU_CHRG_BATT_0   30C6<> 31A8<>
PMU_CLK           14C2<> 30C4<>
PMU_CNVSS         30B6< 30C7<>
PMU_CPU_RESET_L   23A4< 23C4<> 30C4<>
PMU_EPM           30D2< 30D4<>
PMU_FROM_IWP      14C2<> 30C4<>
PMU_I2C_CLK       30B4<> 30C2<>
PMU_I2C_DATA      30B4<> 30C2<
PMU_IWP_L         14B5<> 14B7< 30B6<>
PMU_IWP_NMI       14B5<> 14B7< 30D4<>
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PMU_KB_RESET_IN2  30A7<>
PMU_KB_RESET_L    30A6> 30B7< 39B2>
PMU_LID_CLOSED_L  23A8< 23C4<> 30B2< 30C4<>
PMU_NMI_BUTTON_L  25C1< 30C2< 30C4<>
PMU_NMI_L         30C2< 30C4<>
PMU_NUMLOCK_LED_L  30C4<>
PMU_OOPS          30B2< 30B4<>
PMU_PME_L         14B5<> 26B8< 30B2< 30C4<>
PMU_POWERUP_OK    30B4<> 30D2<
PMU_POWER_UP_L    29C7<> 30C6<> 30D7< 33B8<
PMU_RSQ_L         14B7< 14C2> 30C4<>
PMU_RESET_BUTTON_L  25B1< 30C4<> 30D2<
PMU_RESET_L       30B6<>
PMU_SLEEP_LED     23C4<>
PMU_SLEEP_LED_L   23C2<> 30C4<>
PMU_SMB_CLK       30B4<> 30C2< 31A3<
PMU_SMB_DATA      30B4<> 30C2< 31A2<
PMU_TO_INT        14C2<> 30C4<>
POWER_UP          29C7<>
POWER_VALID       30B2< 30C4<>
PWR_BUTTON_L      23A7<> 25C2< 39B2>
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RAM_ADDR<12..0>   36A5>
RAM_ADDR<1>       9B4< 11B3<> 11B8<>
RAM_ADDR<2>       9B4< 11B5<> 11B6<>
RAM_ADDR<3>       9B4< 11B3<> 11B8<>
RAM_ADDR<4>       9B4< 11B5<> 11B6<>
RAM_ADDR<5>       9B4< 11B3<> 11B8<>
RAM_ADDR<6>       9B4< 11B5<> 11B6<>
RAM_ADDR<7>       9B4< 11B3<> 11B8<>
RAM_ADDR<8>       9B4< 11B5<> 11B6<>
RAM_ADDR<9>       9A4< 11B3<> 11B8<>
RAM_ADDR<10>      9A4< 11B3<> 11B8<>
RAM_ADDR<11>      9A4< 11B5<> 11B6<>
RAM_ADDR<12>      9A4< 11B3<> 11B8<>
RAM_BA<0>         9A4< 11B3<> 11B8<>
RAM_BA<1..0>      36A5>
RAM_BA<1>         9A4< 11B5<> 11B6<>
RAM_CAS_L         9A4< 11B5<> 11B6<> 36A5>
RAM_CKE<0>        9A3< 9C4< 11B6<>
RAM_CKE<3..0>     36A5>
RAM_CKE<1>        9A3< 9C4< 11B8<>
RAM_CKE<2>        9A3< 9C4< 11C5<>
RAM_CKE<3>        9A3< 9C4< 11C3<>
RAM_CS_L<0>       9C4< 11B8<>
RAM_CS_L<3..0>    36A5>
RAM_CS_L<1>       9C4< 11B6<>
RAM_CS_L<2>       9C4< 11B3<>
RAM_CS_L<3>       9C4< 11B5<>
RAM_DATA_A<0>     10C6<> 11D8<>
RAM_DATA_A<7..0>  36C5>
RAM_DATA_A<1>     10C8<> 11D8<>
RAM_DATA_A<2>     10C8<> 11D8<>
RAM_DATA_A<3>     10B8<> 11D8<>
RAM_DATA_A<4>     10B8<> 11D6<>
RAM_DATA_A<5>     10B8<> 11D6<>
RAM_DATA_A<6>     10B8<> 11D6<>
RAM_DATA_A<7>     10B8<> 11D6<>
RAM_DATA_A<8>     10B8<> 11D8<>
RAM_DATA_A<15..8>  36C5>
RAM_DATA_A<9>     10C7<> 11D8<>
RAM_DATA_A<10>    10C7<> 11D8<>
RAM_DATA_A<11>    10C7<> 11D8<>
RAM_DATA_A<12>    10C7<> 11D6<>
RAM_DATA_A<13>    10C7<> 11D6<>
RAM_DATA_A<14>    10C7<> 11D6<>
RAM_DATA_A<15>    10C7<> 11D6<>
RAM_DATA_A<16>    10C6<> 11D8<>
RAM_DATA_A<31..16>  36B5>
RAM_DATA_A<17>    10C8<> 11D3<>
RAM_DATA_A<18>    10C6<> 11D3<>
RAM_DATA_A<19>    10C6<> 11D3<>
RAM_DATA_A<20>    10C6<> 11D5<>
RAM_DATA_A<21>    10C6<> 11C5<>
RAM_DATA_A<22>    10C6<> 11C5<>
RAM_DATA_A<23>    10C6<> 11C5<>
RAM_DATA_A<24>    10C6<> 11C3<>
RAM_DATA_A<25>    10C6<> 11C3<>
RAM_DATA_A<26>    10C6<> 11C3<>
RAM_DATA_A<27>    10C6<> 11C5<>
RAM_DATA_A<28>    10C6<> 11C5<>
RAM_DATA_A<29>    10C6<> 11B3<>
RAM_DATA_A<30>    10C6<> 11B3<>
RAM_DATA_A<31>    10C5<> 11B3<>
RAM_DATA_A<32>    10C4<> 11B8<>
RAM_DATA_A<47..32>  36B5>
RAM_DATA_A<33>    10C4<> 11B6<>
RAM_DATA_A<34>    10C4<> 11B6<>
RAM_DATA_A<35>    10C4<> 11B6<>
RAM_DATA_A<36>    10B4<> 11B6<>
RAM_DATA_A<37>    10B4<> 11B6<>
RAM_DATA_A<38>    10B4<> 11B6<>
RAM_DATA_A<39>    10B4<> 11B6<>
RAM_DATA_A<40>    10B4<> 11B8<>
RAM_DATA_A<41>    10D3<> 11B8<>
RAM_DATA_A<42>    10C3<> 11A8<>
RAM_DATA_A<43>    10C3<> 11A8<>
RAM_DATA_A<44>    10C3<> 11B6<>
RAM_DATA_A<45>    10C3<> 11B6<>
RAM_DATA_A<46>    10C3<> 11A6<>
RAM_DATA_A<47>    10C3<> 11A6<>
RAM_DATA_A<48>    10C2<> 11A8<>
RAM_DATA_A<63..48>  36B5>
RAM_DATA_A<49>    10C2<> 11A8<>
RAM_DATA_A<50>    10C2<> 11A8<>
RAM_DATA_A<51>    10C2<> 11A8<>
RAM_DATA_A<52>    10B2<> 11A6<>
RAM_DATA_A<53>    10B2<> 11A6<>
RAM_DATA_A<54>    10B2<> 11A6<>
RAM_DATA_A<55>    10B2<> 11A6<>
RAM_DATA_A<56>    10B2<> 11A8<>
RAM_DATA_A<63..56>  36A5>
RAM_DATA_A<57>    10D1<> 11A8<>
RAM_DATA_A<58>    10C1<> 11A8<>
RAM_DATA_A<59>    10C1<> 11A8<>
RAM_DATA_A<60>    10C1<> 11A6<>
RAM_DATA_A<61>    10C1<> 11A6<>
RAM_DATA_A<62>    10C1<> 11A6<>
RAM_DATA_A<63>    10C1<> 11A6<>
RAM_DATA_B<0>     10C8<> 11D3<>
RAM_DATA_B<7..0>  36C5>
RAM_DATA_B<1>     10C8<> 11D3<>
RAM_DATA_B<2>     10C8<> 11D3<>
RAM_DATA_B<3>     10C8<> 11D3<>
RAM_DATA_B<4>     10C8<> 11D5<>
RAM_DATA_B<5>     10C8<> 11D5<>
RAM_DATA_B<6>     10C8<> 11D5<>
RAM_DATA_B<7>     10C8<> 11D5<>
RAM_DATA_B<8>     10C8<> 11D3<>
RAM_DATA_B<15..8>  36C5>
RAM_DATA_B<9>     10C8<> 11D3<>
RAM_DATA_B<10>    10C8<> 11D3<>
RAM_DATA_B<11>    10C8<> 11D3<>
RAM_DATA_B<12>    10C8<> 11D5<>
RAM_DATA_B<13>    10C8<> 11D5<>
RAM_DATA_B<14>    10C8<> 11D5<>
RAM_DATA_B<15>    10C8<> 11D5<>
RAM_DATA_B<16>    10C6<> 11D3<>
RAM_DATA_B<31..16>  36B5>
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RAM_DATA_B<18>    10C6<> 11C3<>
RAM_DATA_B<19>    10C6<> 11C3<>
RAM_DATA_B<20>    10C6<> 11D5<>
RAM_DATA_B<21>    10C6<> 11C5<>
RAM_DATA_B<22>    10C6<> 11C5<>
RAM_DATA_B<23>    10C6<> 11C5<>
RAM_DATA_B<24>    10C6<> 11C3<>
RAM_DATA_B<25>    10C6<> 11C3<>
RAM_DATA_B<26>    10C6<> 11C3<>
RAM_DATA_B<27>    10C6<> 11C3<>
RAM_DATA_B<28>    10C6<> 11C5<>
RAM_DATA_B<29>    10C6<> 11C5<>
RAM_DATA_B<30>    10C6<> 11C5<>
RAM_DATA_B<31>    10C6<> 11C5<>
RAM_DATA_B<32>    10C4<> 11B3<>
RAM_DATA_B<47..32>  36B5>
RAM_DATA_B<33>    10C4<> 11B3<>
RAM_DATA_B<34>    10C4<> 11B3<>
RAM_DATA_B<35>    10C4<> 11B3<>
RAM_DATA_B<36>    10C4<> 11B5<>
RAM_DATA_B<37>    10C4<> 11B5<>
RAM_DATA_B<38>    10C4<> 11B5<>
RAM_DATA_B<39>    10C4<> 11B5<>
RAM_DATA_B<40>    10C4<> 11B3<>
RAM_DATA_B<41>    10C4<> 11B3<>
RAM_DATA_B<42>    10C4<> 11A3<>
RAM_DATA_B<43>    10C4<> 11A3<>
RAM_DATA_B<44>    10C4<> 11B5<>
RAM_DATA_B<45>    10C4<> 11B5<>
RAM_DATA_B<46>    10C4<> 11A5<>
RAM_DATA_B<47>    10C4<> 11A5<>
RAM_DATA_B<48>    10D2<> 11A3<>
RAM_DATA_B<55..48>  36B5>
RAM_DATA_B<49>    10C2<> 11A3<>
RAM_DATA_B<50>    10C2<> 11A3<>
RAM_DATA_B<51>    10C2<> 11A3<>
RAM_DATA_B<52>    10C2<> 11A5<>
RAM_DATA_B<53>    10C2<> 11A5<>
RAM_DATA_B<54>    10C2<> 11A5<>
RAM_DATA_B<55>    10C2<> 11A5<>
RAM_DATA_B<56>    10C2<> 11A3<>
RAM_DATA_B<63..56>  36A5>
RAM_DATA_B<57>    10C2<> 11A3<>
RAM_DATA_B<58>    10C2<> 11A3<>
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RAM_DATA_B<61>    10C2<> 11A5<>
RAM_DATA_B<62>    10C2<> 11A5<>
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RAM_DQM_A<1>      10C7<> 11D6<> 36C5>
RAM_DQM_A<2>      10B8<> 11C6<>
RAM_DQM_A<3..2>   36B5>
RAM_DQM_A<3>      10C5<> 11C6<>
RAM_DQM_A<1>      10B4<> 11B6<>
RAM_DQM_A<5..4>   36B5>
RAM_DQM_A<5>      10C3<> 11A6<>
RAM_DQM_A<4>      10B2<> 11A6<> 36B5>
RAM_DQM_A<7>      10C1<> 11A6<> 36A5>
RAM_DQM_A<6>      10C8<> 11D5<> 36C5>
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RAM_DQS_B<7>      10C2<> 11A3<> 36A5>
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RAM_MUXSEL_L      10A3< 10A5< 10B5<> 10B7<> 36A5>
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RAM_WE_L          9A4< 11B3<> 11B8<> 36A5>
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SRMOD_TP          26A5< 39A4>
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ST7_SENSOR5_SCK_PU  23B2< 23D4<>
ST7_SENSOR5_SDA_PU  23B2< 23B4< 23D4<>
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6459	A
SCALE: NONE	SHT 42 OF 44	

*** Part Cross-Reference for the entire design ***

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D12	DIODE_DUAL_6P	29
D13	DIODE_SCHOT	33
D14	DIODE_SCHOT_3P2	28
D15	DIODE_DUAL_6P	29
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FL3	FILTER_LC	22
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G2	OSC	18
J1	CON_F1ST_S2MT_SM	14
J2	CON_3RTSM_125	25
J3	CON_F14RT_S2MT_SM	24
J4	CON_3RTSM_125	25
J5	CON_12	34
J6	CON_F30RT_S2MT_SM	22
J7	CON_4RT_WRIB	22
J8	CON_F16ST_D_SMA	25
J9	CON_M80ST_D4MT_SM	17
J10	CON_M50SM_5MM	24
J11	CON_F14RT_S2MT_SM	32
J12	CON_F30ST_D_SM	25
J13	CON_M50SM_5MM	24
J14	CON_F30RT_T6MT_TH1	22
J15	CON_F5RT_MINIDIN_TH	22
J16	CON_10STSM_5087	25
J17	CON_RJ45_SHORT_4MT_TH	27
J18	CON_M8RT_S_SM	31
J19	CON_F200RT_DDRDIMM_SM1	11
J20	CON_F80ST_D4MT_SM	24
J22	CON_F200RT_DDRDIMM_SM2	11
J23	CON_F6RT_S4MT_TH1	29
J24	CON_F40RT_S2MT_SM	23
J25	CON_M8RT_S_SM	31
J26	CON_F9RT_1394B_S6MT_SMA	29
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Q33	TRA_2N3906	23
Q35	TRA_2N7002DW	22 23
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XW29	SHORT	21
XW30	SHORT	21
XW31	SHORT	5
Y1	CRYSTAL	14
Y3	CRYSTAL	27
Y4	CRYSTAL	23
Y5	CRYSTAL	26
Y6	CRYSTAL	30
Y7	CRYSTAL_4PIN	30
ET1	HOLE_VIA	4
ET2	MTGHOLE	4
ET3	HOLE_VIA	4
ET4	MTGHOLE	4
ET5	MTGHOLE	4
ET6	MTGHOLE	4
ET7	HOLE_VIA	4
ET8	HOLE_VIA	4
ET9	HOLE_VIA	4
ET10	MTGHOLE	4
ET11	MTGHOLE	4
ET12	HOLE_VIA	4
ET13	HOLE_VIA	4
ET14	HOLE_VIA	4
ET15	HOLE_VIA	4
ET16	MTGHOLE	4
ET17	HOLE_VIA	4
ET18	HOLE_VIA	4
ET19	HOLE_VIA	4
ET20	HOLE_VIA	4
ET21	HOLE_VIA	4
ET22	HOLE_VIA	4
ET23	HOLE_VIA	4
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ET25	HOLE_VIA	4
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ET31	HOLE_VIA	4
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ET69	HOLE_VIA	4
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ET76	HOLE_VIA	4
ET77	HOLE_VIA	4
ET78	HOLE_VIA	4
ET79	HOLE_VIA	4
ET80	HOLE_VIA	4
ET81	HOLE_VIA	4
ET82	HOLE_VIA	4
ET83	MTGHOLE	4