1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
C		480849	PRODUCTION RELEASED	01/10/07	?

SCHEM,MLB,PB17"
01/04/2007

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7	CPU PLL AND CONFIGURATION STRAPS
8	INTREPID MAXBUS AND BOOT STRAPS
9	INTREPID MEMORY INTERFACE / BOOT ROM
10	DDR MEMORY MUXES
11	200PIN DDR MEMORY SODIMM CONNECTORS
12	INTREPID AGP 4X/PCI
13	INTREPID ENET/FW/UATA/EIDE INTERFACES
14	INTREPID GPIOS/SERIAL/USB INTERFACES/SSCG
15	INTREPID POWER RAILS
16	INTREPID DECOUPLING
17	CARDBUS CONTROLLER (PCI1510)
18	M10 AGP & CLOCKS
19	M10 LVDS/TMDS/VGA/GPIO & GPU VCORE
20	SIL1162 TMDS TRANSMITTER
21	M10 ANALOG, POWER, GND

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22	VIDEO CONNECTORS - INVERTER, DVI, S-VIDEO DUAL-CHANNEL LVDS
23	LMU, LIGHT SENSOR, BOOTBANGER, SLEEP LED SPIDEY - KBD,TPAD,HALL EFFECT,PWR BUTTON
24	INTERNAL CONNECTORS - DVD, CARDSLOT, HARD DRIVE, LEFT USB/BLUETOOTH
25	FAN CONTROLLER, MODEM, SOUND SERIAL DEBUG (JOLLY ROGER, PWR/NMI/RESET)
26	USB 2.0
27	MARVELL GIGABIT ETHERNET PHY
28	FIREWIRE A/B PHY
29	FIREWIRE A/B CONNECTORS, PORT POWER LIMITER
30	PMU (POWER MANAGEMENT UNIT)
31	BATTERY CHARGER AND CONNECTOR
32	12.8V SYSTEM POWER SUPPLY / PMU POWER SUPPLY
33	3.3V / 5V SYSTEM POWER SUPPLIES
34	CPU CORE VOLTAGE POWER SUPPLY
35	1.5V/ 1.8V / 2.5V SYSTEM POWER SUPPLIES
36	SIGNAL CONSTRAINTS (1 OF 3) - DIGITAL/CLK
37	SIGNAL CONSTRAINTS (2 OF 3) - DIGITAL/DIFF
38	SIGNAL CONSTRAINTS (3 OF 3) - POWER NETS
39	FUNCTIONAL TEST POINTS
40	REVISION HISTORY (1 OF 1)
41-42	SIGNAL NAMES
43-44	COMPONENT LOCATIONS

BOM OPTIONS	STUFF	NO STUFF
D3_HOT		✓
D3_COLD	✓	
GPU_SS	✓	
GPU_SWITCH	✓	
SERIAL_DEBUG		✓
VCORE_OFFSET	✓	
1_8V_MAXBUS	✓	
1_5V_MAXBUS		✓
NEC_USB	✓	
INTREPID_USB		✓
BBANG		✓
NO_BBANG	✓	
ATI_MEMIO_HI	✓	
ATI_MEMIO_LO		✓
SSCG		✓
NO_SSCG	✓	
5V_HD_LOGIC	✓	
3V_HD_LOGIC		✓
EXT_TMDS	✓	
INT_TMDS		✓
NO_4XVCORE	✓	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6582	1	SCHEM,MLB,PB17 INCH	SCH1	
820-1524	1	PCBF,MLB,PB17 INCH	PCB1	

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE
SIZE D

Apple Computer Inc.

TITLE
SCHEM,MLB,PB17 INCH

DRAWING NUMBER 051-6582 REV. C
SHT 1 OF 44

U44 INTREPID

J18 Ethernet Connector P.28
4 DATA PAIRS
U49 Ethernet PHY P.28
G/MII
3.3V
10/100/1000
8BIT TX
8BIT RX
125MHZ

J24 FW - A Connector P.30
2 DATA PAIRS @ 200MHz
J22 FW - B Connector P.30
2 DATA PAIRS @ 400MHz
U28 FireWire PHY P.29
1394 OHCI
3.3V
8BIT TX/RX
100MHZ

J11 OPTICAL DRIVE Connector P.25
EIDE
J13 ULTRA ATA/100 Connector P.25
UIDE

SLEEP LED P.26
LMU
J14 TUBA (SOUND) Connector P.26
I2S
I2C
I2C
U48/J2/J4 Fan Circuit P.26

J25 Battery Connector P.32
SMBUS
3.3V
Power Supply & Charger P.32-36
J19 SUTRO (PWR) Connector P.32

U36 LMU P.24
I2C
U39 PMU P.31
SERIAL
5V

J10 CARDBUS Connector P.18
33MHZ
16/32 BITS
3.3V/5V
U26 TI PCI1510 CardBus Controller P.18

J3 (SHARE WITH BLUETOOTH)
LEFT USB P.25
USB 2.0
J12 RIGHT USB BACKUP BATTERY P.33
NOT USED
USB 2.0
J3 (SHARE WITH LEFT USB)
BlueTooth P.25
NOT USED
J9 Modem Board Connector P.26
INTRPEID
I2C

ETHERNET 10/100/1000 P.14	FIREWIRE 800 MB/S P.14	UATA 100 P.14	EIDE P.14	CARDSLOT P.14	I2S P.15	I2C P.14 P.15

NOT USED

USB PORT A P.15
USB PORT B P.15
USB PORT C P.15
USB PORT D P.15
USB PORT E P.15
USB PORT F P.15
MAXBUS P.9

SCCA P.15 → J5 Serial Debug Connector P.26
VIA/PMU P.15
BOOTROM P.14 → U17 BOOT ROM 1M X 8 P.10
PCI 32BITS 33MHZ P.13
4X AGP P.13

J15 TRACKPAD Connector | Keyboard Connector
KB LED LIGHT SENSOR P.24

U52 USB 2.0 CONTROLLER P.27
PCI BUS
32BITS
33MHZ
3.3V

AGP BUS
1.5V/3.3V
32BITS
66MHZ
U43 ATI M10 64MB P.18-21
MEMORY CH. A (INTERNAL MEM)
MEMORY CH. C (INTERNAL MEM)
MEMORY CH. B (INTERNAL MEM)
MEMORY CH. D (INTERNAL MEM)
J21 AIRPOPT Connector P.25

J8 Inverter Connector P.22

LVDS
EDID (I2C)
S-VIDEO
COMPOSITE
TMDS
RGB
(DDC TOO)

J7 LCD Panel Connector P.22
J17 S-Video Connector P.22
J16 DVI-I Connector P.22

DDR MEMORY P.10
MEMORY BUS
2.5V
167MHZ
64BITS
U11/U12/U13/U14 2:1 DDR MUXES P.11
J20/J23 DDR SDRAM DIMM 0
DDR SDRAM DIMM 1 SO-DIMM Connector P.12

MAXBUS
1.8V
167MHZ
32BIT ADDRESS
64BIT DATA
U42 APOLLO CPU (MPC7457) P.5-6
CPU PLL Config P.7
PMU

SYSTEM BLOCK DIAGRAM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C

SCALE NONE | SHT 2 OF 44

POWER SYSTEM ARCHITECTURE

AC ADAPTER IN PG 31

INRUSH LIMITER PG 30

+24V_PBUS

1V20_REF
U21 PG 31
>-13.44V TURNS-ON
<-13.44V SHUTS-OFF

RUN/SS
BUCK REGULATOR (LTC1625) PG 32
VCC
AC: 12.8V
NO AC: BATTERY VOLTAGE
1625 NOT RUNNING
SHUTDOWN: RUNNING
SLEEP: RUNNING
RUN: RUNNING

+PBUS (12.8V)

BACKLIGHT INVERTER

+5V_MAIN
VCC
MAIN 2.5V/1.5V DC/DC (MAX1715) PG 35
PGOOD
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING
TURNS ON OUTPUT @ 2.4V ON1/ON2

MAP31 DDR I/O
MAP31 DDR CORE
DDR POWER
+2.5V_MAIN
1_5V_2_5V_OK
+1.5V_MAIN
INTREPID CORE
AGP I/O

+PBUS

DCDC_EN
SLEEP
MAXBUS SEQUENCING

+5V_MAIN
VCC
SHDN
DC/DC (MAX1717) PG 34
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING
CPU_VCORE (+1.4V/+1.5V)

14V_PBUS

+3V_PMU LDO PG 32
+BATT
+5V_MAIN
+3V_PMU
+4_6V_BU

RC AT 1M*0.047UF @ 24V
STARTS 2.0MSEC AFTER DCDC_EN_L BECOMES LOW

RUN/SS - 5V
TURNS ON AT >1V
<100UA ALLOWED
INTERNAL ZENER CLAMP TO 6V
MAIN 3V/5V DC/DC (LTC3707) PG 33
VCC
PGOOD
STBYMD
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING
INTERNAL ZENER CLAMP TO 6V
<100UA ALLOWED
TURNS ON AT >1V
RUN/SS - 3V

+5V_MAIN
3V_5V_OK
HOLDS BOTH RUN/SS AT GND WHEN IT'S CONNECTED TO GND
TURNS CONTROL TO RUN/SS WHEN IT'S OPEN
+3.3V_MAIN

DCDC_EN_L
AFTER PMU IS UP AND RUNNING DCDC_EN_L WILL PULL ON1/ON2 LOW IN SHUTDOWN

+5V_MAIN
+PBUS (12.8V)
VCC
EXT_VCC
DC/DC (LTC1778) PG 20
SHUTDOWN: STOPPED
SLEEP: D3HOT/D3COLD
RUN: RUNNING
TURNS ON AS LOW AS 0.8V/TYP 1.5V
INTERNAL 1.2UA CURRENT SOURCE
RUN/SS
GPU_VCORE +1.2V/+1.0V

DCDC_EN
SLEEP
D3_COLD
GPU_VCORE SEQUENCING
1M & 0.1UF @14V, IT TAKES ~5.88MS TO START SWITCHER
1_5V_2_5V_OK
D3_HOT
DCDC_EN_L
D3_HOT
1_5V_2_5V_OK WILL NOT PULL LOW UNTIL +5V_MAIN TURNS ON
HOWEVER, 5V SHOULD TURN ON ~2.23MS AFTER DCDC_EN_L OR PMU_POWERUP_L BECOMES '1'; MUCH LESS THAN THE RC CHARGING AT INT_VCC (5V)

+PBUS
BACKUP BATTERY
12.8V CHARGES BACKUP BATTERY
24V IS OUTPUT ONLY FROM BACKUP BATTERY
CHARGER INPUT & BOOST OUTPUT PG 32
BACKUP BATTERY CIRCUIT CHARGES OFF +PBUS AND PREVENTS +PBUS AND +24V_PBUS FROM DROPPING BELOW 6V (UNTIL DRAINED)

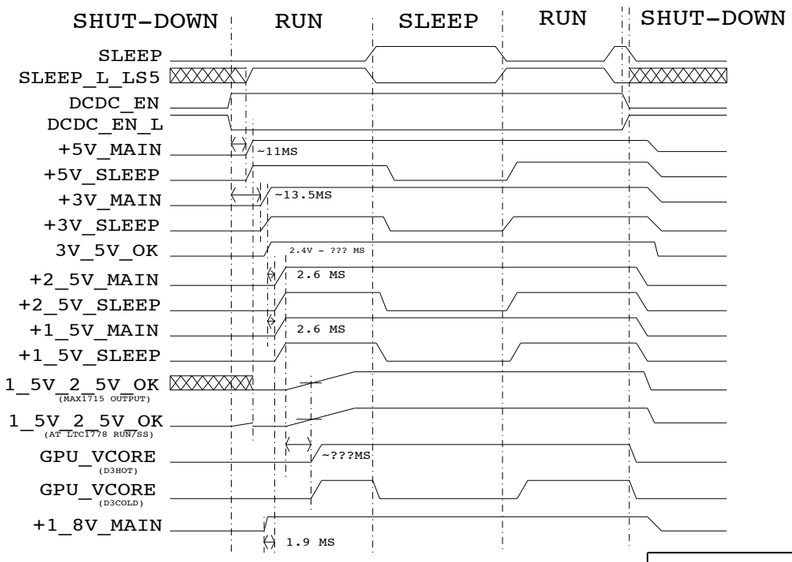
RC AT 1M*0.1UF @ 24V
STARTS ~4.25MSEC AFTER DCDC_EN_L BECOMES LOW
NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED
+24V_PBUS

DC/DC (LTC3411) PG 35
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING
+1.8V_MAIN
MAXBUS BROADCOM

BATTERY CHARGER (MAX1772) PG 31
+BATT

3S 3P PRISMATIC CELLS

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED
BATTERY VOLTAGE FEED-IN PATH PG 31
+PBUS



POWER BLOCK DIAGRAM

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 3 OF 44	

PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 12
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

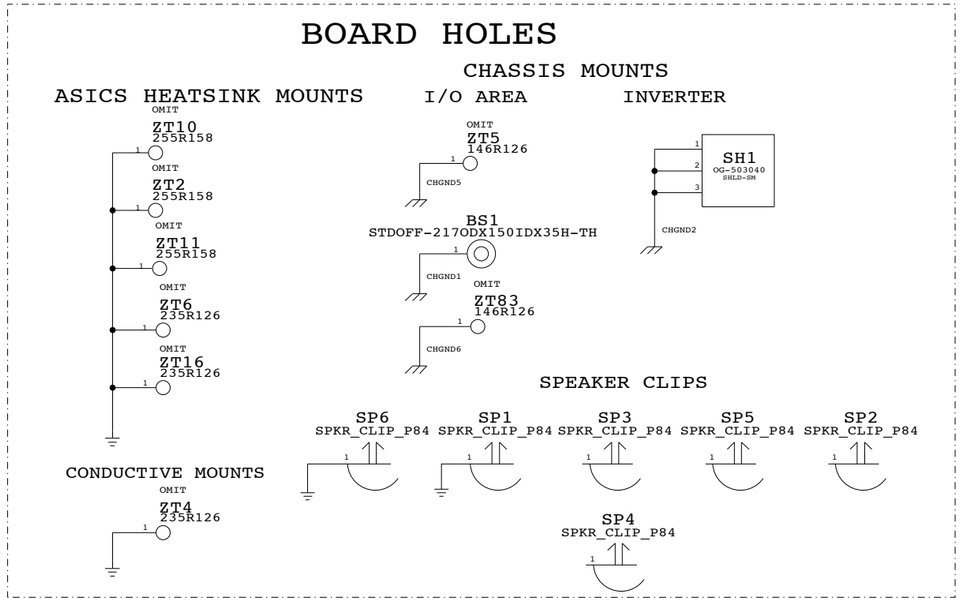
SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

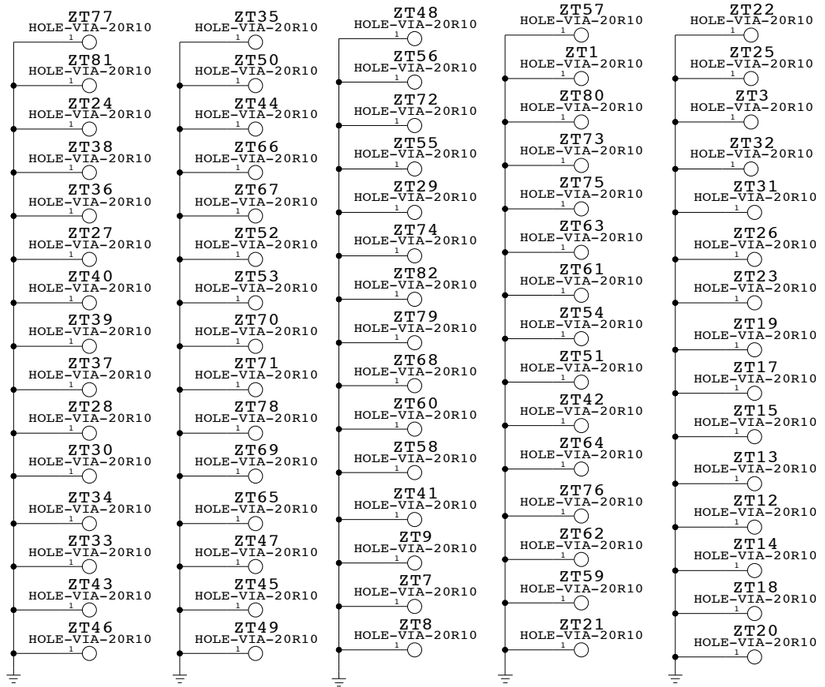
20R10 TH VIA OR VIA IN PAD

1		SIGNAL (1/3 OZ + COPPER PLATING)
2	PREPREG (3MIL)	GROUND (1/2 OZ)
3	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
4	PREPREG (3MIL)	SIGNAL (1/2 OZ)
5	LAMINATE (4MIL)	GROUND (1/2 OZ)
6	PREPREG (2MIL)	CUT POWER PLANE(1 OZ)
7	LAMINATE (3MIL)	CUT POWER PLANE(1 OZ)
8	PREPREG (2MIL)	GROUND (1/2 OZ)
9	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
10	PREPREG (3MIL)	SIGNAL (1/2 OZ)
11	LAMINATE (4MIL)	GROUND (1/2 OZ)
12	PREPREG (3MIL)	SIGNAL (1/3 OZ + COPPER PLATING)

BOARD HOLES



GROUND VIAS



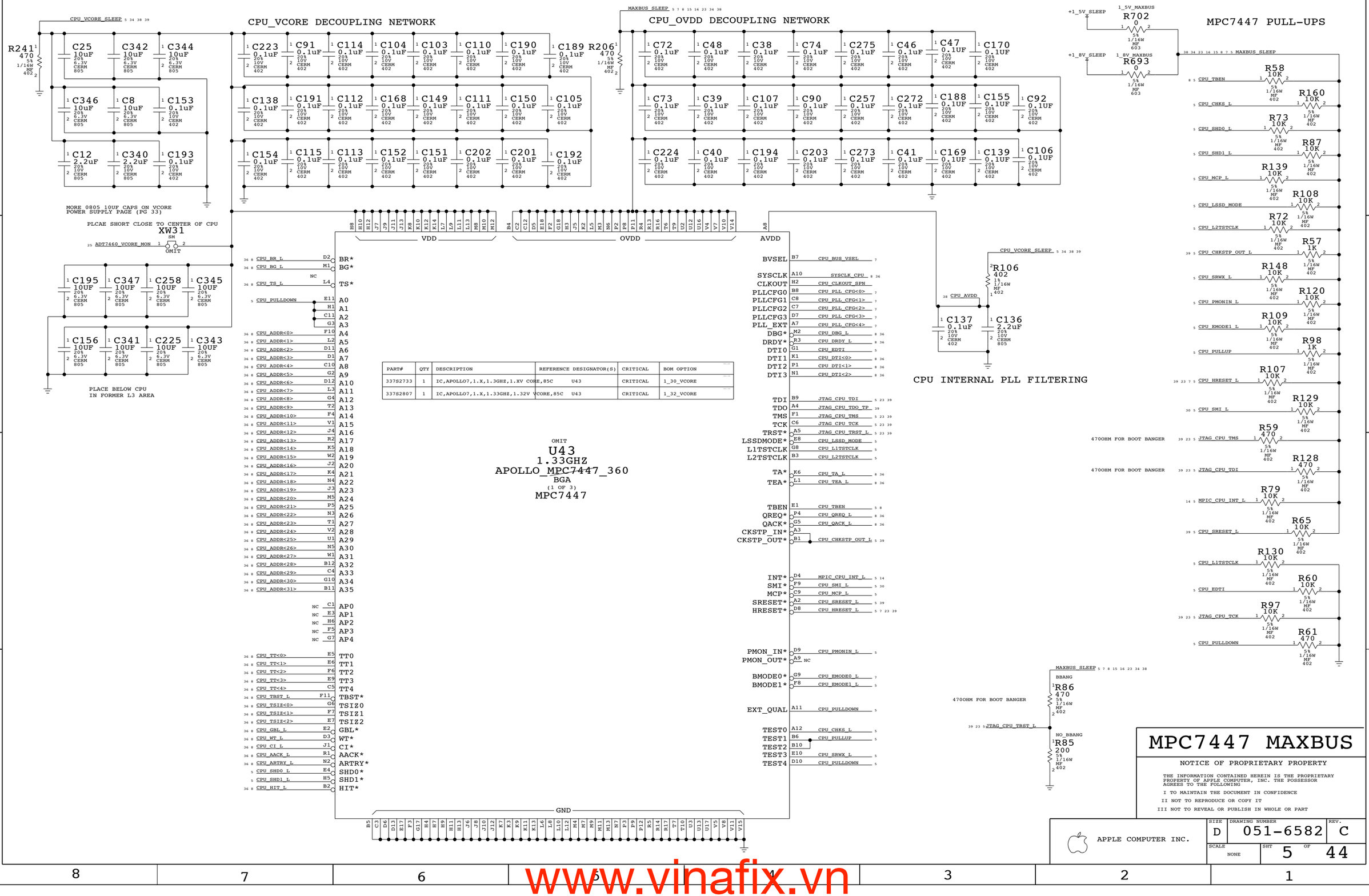
BOARD INFORMATION

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C

SCALE: NONE

SHT 4 OF 44



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33782733	1	IC,APOLLO7,1.X,1.3GHZ,1.XV CORE,85C	U43	CRITICAL	1_30_VCORE
33782807	1	IC,APOLLO7,1.X,1.33GHZ,1.32V VCORE,85C	U43	CRITICAL	1_32_VCORE

BOOT BANGER - LMU PERORMS THIS FUNCTION IF NEEDED
SEE PAGE 22

OMIT
U43
1.33GHZ
BGA
(2 OF 3)
APOLLO_MPC7447_360

36	CPU_DATA<0>	R15	D0
36	CPU_DATA<1>	W15	D1
36	CPU_DATA<2>	T14	D2
36	CPU_DATA<3>	V16	D3
36	CPU_DATA<4>	W16	D4
36	CPU_DATA<5>	T15	D5
36	CPU_DATA<6>	U15	D6
36	CPU_DATA<7>	P14	D7
36	CPU_DATA<8>	V13	D8
36	CPU_DATA<9>	W13	D9
36	CPU_DATA<10>	T13	D10
36	CPU_DATA<11>	P13	D11
36	CPU_DATA<12>	U14	D12
36	CPU_DATA<13>	W14	D13
36	CPU_DATA<14>	R12	D14
36	CPU_DATA<15>	T12	D15
36	CPU_DATA<16>	W12	D16
36	CPU_DATA<17>	V12	D17
36	CPU_DATA<18>	N11	D18
36	CPU_DATA<19>	N10	D19
36	CPU_DATA<20>	R11	D20
36	CPU_DATA<21>	U11	D21
36	CPU_DATA<22>	W11	D22
36	CPU_DATA<23>	T11	D23
36	CPU_DATA<24>	R10	D24
36	CPU_DATA<25>	N9	D25
36	CPU_DATA<26>	P10	D26
36	CPU_DATA<27>	U10	D27
36	CPU_DATA<28>	R9	D28
36	CPU_DATA<29>	W10	D29
36	CPU_DATA<30>	U9	D30
36	CPU_DATA<31>	V9	D31
36	CPU_DATA<32>	W5	D32
36	CPU_DATA<33>	U6	D33
36	CPU_DATA<34>	T5	D34
36	CPU_DATA<35>	U5	D35
36	CPU_DATA<36>	W7	D36
36	CPU_DATA<37>	R6	D37
36	CPU_DATA<38>	P7	D38
36	CPU_DATA<39>	V6	D39
36	CPU_DATA<40>	P17	D40
36	CPU_DATA<41>	R19	D41
36	CPU_DATA<42>	V18	D42
36	CPU_DATA<43>	R18	D43
36	CPU_DATA<44>	V19	D44
36	CPU_DATA<45>	T19	D45
36	CPU_DATA<46>	U19	D46
36	CPU_DATA<47>	W19	D47
36	CPU_DATA<48>	U18	D48
36	CPU_DATA<49>	W17	D49
36	CPU_DATA<50>	W18	D50
36	CPU_DATA<51>	T16	D51
36	CPU_DATA<52>	T18	D52
36	CPU_DATA<53>	T17	D53
36	CPU_DATA<54>	W3	D54
36	CPU_DATA<55>	V17	D55
36	CPU_DATA<56>	U4	D56
36	CPU_DATA<57>	U8	D57
36	CPU_DATA<58>	U7	D58
36	CPU_DATA<59>	R7	D59
36	CPU_DATA<60>	P6	D60
36	CPU_DATA<61>	R8	D61
36	CPU_DATA<62>	W8	D62
36	CPU_DATA<63>	T8	D63
NC	T3		DP0
NC	W4		DP1
NC	T4		DP2
NC	W9		DP3
NC	M6		DP4
NC	V3		DP5
NC	N8		DP6
NC	W6		DP7

OMIT
U43
1.33GHZ
BGA
(3 OF 3)
APOLLO_MPC7447_360

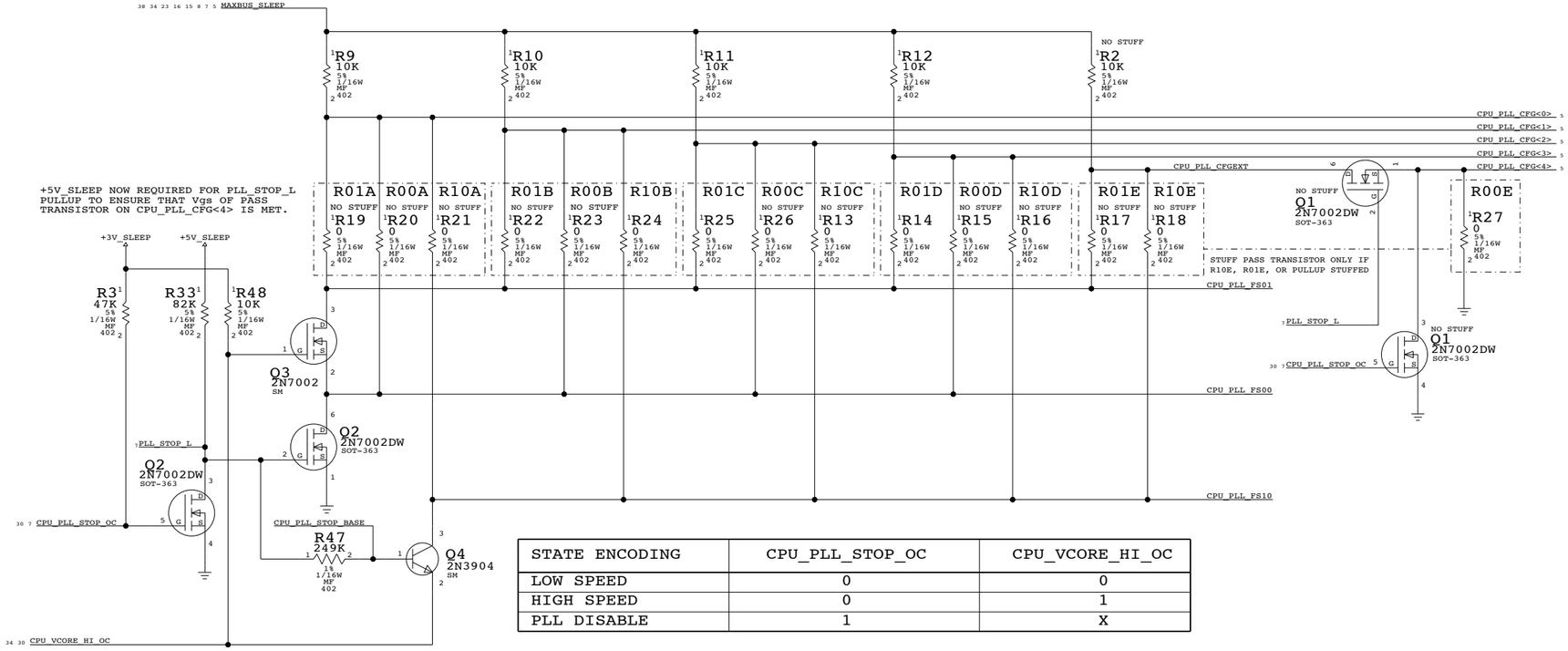
NC	F18	NC_F18
NC		NC_F17
NC		NC_F19
NC	H19	NC_H19
NC		NC_H18
NC	H17	NC_H17
NC		NC_H16
NC		NC_E19
NC		NC_D18
NC		NC_F16
NC		NC_G16
NC		NC_D19
NC		NC_F15
NC		NC_G19
NC		NC_E16
NC		NC_D17
NC		NC_D16
NC		NC_P15
NC		NC_L15
NC		NC_N15
NC		NC_P18
NC		NC_N14
NC		NC_M14
NC		NC_M17
NC		NC_N13
NC		NC_N16
NC		NC_M19
NC		NC_M16
NC		NC_P19
NC		NC_N17
NC		NC_M15
NC		NC_L17
NC		NC_L14
NC		NC_K15
NC		NC_J14
NC		NC_J18
NC		NC_J19
NC		NC_J15
NC		NC_K19
NC	J16	NC_J16
NC		NC_H15
NC		NC_L16
NC		NC_P16
NC		NC_M18
NC		NC_L19
NC	L18	NC_L18
NC		NC_K18
NC		NC_J17
NC		NC_K16
NC		NC_C19
NC		NC_D15
NC		NC_G15
NC		NC_C18
NC		NC_A16
NC		NC_B19
NC		NC_A19
NC		NC_D14
NC		NC_E15
NC		NC_B15
NC		NC_B17
NC		NC_C17
NC	C16	NC_C16
NC		NC_G13
NC	E14	NC_E14
NC	H14	NC_H14
NC	G14	NC_G14
NC	C15	NC_C15
NC	A17	NC_A17
NC	G12	NC_G12
NC	F14	NC_F14
NC	F13	NC_F13
NC	E13	NC_E13
NC	B16	NC_B16
NC	A15	NC_A15
NC	C14	NC_C14
NC	A18	NC_A18
NC	A13	NC_A13
NC	F12	NC_F12
NC	A14	NC_A14
NC	G11	NC_G11
NC	C13	NC_C13
NC	N12	NC_N12
NC	N18	NC_N18
NC	K17	NC_K17
NC	N19	NC_N19
NC	B18	NC_B18
NC	E12	NC_E12
NC	B13	NC_B13
NC	B14	NC_B14
NC	A6	NC_A6

MPC7447/BBANG

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 6 OF 44	

CPU PLL CONFIG CIRCUITRY



STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

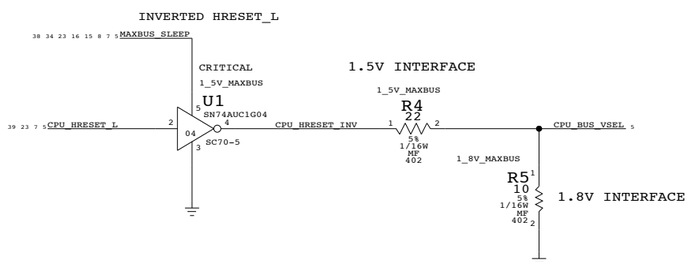
CPU FREQUENCY CONFIGURATION

APOLLO 7

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ (MHZ)	133MHZ (MHZ)	CPU_PLL_CFG 4 E	0123 ABCD	HEX
0.0X	PLL OFF		0	1111	0F
1.0X	PLL BYPASS		0	0011	03
2.0X	333	267	0	0100	04
3.0X	500	400	0	1000	08
4.0X	667	533	0	1010	0A
5.0X	833	667	0	1011	0B
5.5X	917	733	0	1001	09
6.0X	1000	800	0	1101	0D
6.5X	1083	867	0	0101	05
7.0X	1167	933	0	0010	02
7.5X	1250	1000	0	0001	01
8.0X	1333	1067	0	1100	0C
8.5X	1417	1133	0	0110	06
9.0X	1500	1200	1	0111	17
9.5X	1583	1267	0	0111	07
10.0X	1667	1333	1	1010	1A
10.5X	1750	1400	1	1000	18
11.0X	1833	1467	1	1001	19
11.5X	1917	1533	0	0000	00
12.0X	2000	1600	1	1011	1B
12.5X	2083	1667	1	1111	1F
13.0X	2167	1733	1	0101	15
13.5X	2250	1800	0	1110	0E
14.0X	2333	1867	1	1100	1C
15.0X	2500	2000	1	0001	11
16.0X	2667	2133	1	1101	1D
17.0X	2833	2267	1	0000	10
18.0X	3000	2400	1	0010	12
20.0X	3333	2667	1	0011	13
21.0X	3500	2800	1	0100	14
24.0X	4000	3200	1	0110	16
28.0X	4667	3733	1	1110	1E

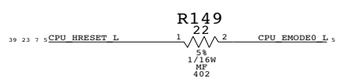
CPU CONFIGURATION

MAXBUS VSEL



DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L NEED TO CHARACTERIZE

BUSTYPE SELECT



APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

CPU CONFIGURATION

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 7 OF 44	

INTREPID BOOT STRAPS

BIT 32 TO 39

MAXBUS_SLEEP

R642	R135	R123	R153	R166	R179	R651	R178
NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF
CPU_DATA<32>	CPU_DATA<33>	CPU_DATA<34>	CPU_DATA<35>	CPU_DATA<36>	CPU_DATA<37>	CPU_DATA<38>	CPU_DATA<39>

R136	R643	R639	R657	R664	R673	R143	R674
10K 5% 1/16W MF 402							
0: FSB 1.05V (CPU input voltage) 1: FSB 1.5V	0: Disable Intel Thermal Diode 1: Activate	0: Disable Intel Thermal Diode 1: Activate	0: Disable Extra FSB Strength 1: Activate Extra FSB Strength	spare	spare	spare	spare

BIT 40 TO 47

MAXBUS_SLEEP

R122	R142	R164	R134	R184	R177	R152	R165
NO STUFF	NO STUFF	NO STUFF	SSCG	NO STUFF	NO_SSCG	NO_SSCG	NO_SSCG
CPU_DATA<40>	CPU_DATA<41>	CPU_DATA<42>	CPU_DATA<43>	CPU_DATA<44>	CPU_DATA<45>	CPU_DATA<46>	CPU_DATA<47>

R640	R652	R665	R644	R683	R675	R658	R666
10K 5% 1/16W MF 402			NO_SSCG		SSCG	SSCG	SSCG

Spare | Spare | BIT2 | BIT1 | BIT0

PLL4MODESEL_NXT[2:0]
000: 166.4MHZ (2.5X)
001: 149.76MHZ
010: 133.12MHZ (2.0X)
011: 99.84MHZ (1.5X)
100: 83.20MHZ

MODE A (2.5X) IS FOR STATIC OPERATION
MODE C (2.0X) IS FOR CLOCK SLEW OPERATION

InternalSpreadEn 0: PLL1 (NO SPREAD) 1: Active

PCI1_Source Clock 0: PLL1 (NO SPREAD) 1: PLL2 (NO SPREAD)

PCI0_Source Clock 0: PLL1 (NO SPREAD) 1: PLL2 (NO SPREAD)

BIT 48 TO 55

MAXBUS_SLEEP

R133	R121	R163	R151	R162	R141	R183	R176
SSCG	SSCG	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF
CPU_DATA<48>	CPU_DATA<49>	CPU_DATA<50>	CPU_DATA<51>	CPU_DATA<52>	CPU_DATA<53>	CPU_DATA<54>	CPU_DATA<55>

R645	R641	R668	R659	R667	R653	R684	R676
NO_SSCG	NO_SSCG	NO STUFF				NO STUFF	
10K 5% 1/16W MF 402							

BUF_REF_CLK_OUTEnable_h 0: Disable 1: Active

SelPll4ExtSrc 0: Internal source 1: External source

Spare

TT1 1.34v workaround 0: Disable 1: TT1 1.34v workaround

BIT2 | BIT1 | BIT0

MaxBus output impedance
111: 28.6 ohm
011: 33.3 ohm
101: 40 ohm
001: 50 ohm
110: 66.6 ohm
010: 100 ohm
100: 200 ohm
000: 200 ohm

Spare

R227 4.7 5% 1/16W MF 402

+1_5V_INTREPID_PLL — +1_5V_INTREPID_PLL7

C308 0.22UF 20% 6.3V CERM 402

THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:
1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
2/ D46 - SELPCI1SPREADCLK - SLEEP/WAKE CYCLE REQUIRED
3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT

IF A STRAP IS NOT LISTED, THEN
IT CANNOT BE CHANGED BY SOFTWARE

VDD15A_7 (PLL6) H26
CRITICAL

U45
INTREPID-REV2.1
BGA
(1 OF 9)

CPU_BR_L	E29	BR	INPUT
CPU_BG_L	E26	BG	NO BUS KEEPER
CPU_TS_L	B27	TS	NO BUS KEEPER
CPU_ADDR<0>	D24	A_0	
CPU_ADDR<1>	D25	A_1	
CPU_ADDR<2>	A27	A_2	
CPU_ADDR<3>	E24	A_3	
CPU_ADDR<4>	G23	A_4	
CPU_ADDR<5>	B26	A_5	
CPU_ADDR<6>	A26	A_6	
CPU_ADDR<7>	D23	A_7	
CPU_ADDR<8>	A25	A_8	
CPU_ADDR<9>	E23	A_9	
CPU_ADDR<10>	J22	A_10	
CPU_ADDR<11>	B25	A_11	
CPU_ADDR<12>	H22	A_12	
CPU_ADDR<13>	G22	A_13	
CPU_ADDR<14>	D22	A_14	
CPU_ADDR<15>	B24	A_15	
CPU_ADDR<16>	B23	A_16	
CPU_ADDR<17>	E22	A_17	
CPU_ADDR<18>	J21	A_18	
CPU_ADDR<19>	G21	A_19	
CPU_ADDR<20>	E21	A_20	
CPU_ADDR<21>	A24	A_21	
CPU_ADDR<22>	D21	A_22	
CPU_ADDR<23>	A23	A_23	
CPU_ADDR<24>	H20	A_24	
CPU_ADDR<25>	B22	A_25	
CPU_ADDR<26>	H21	A_26	
CPU_ADDR<27>	A22	A_27	
CPU_ADDR<28>	E20	A_28	
CPU_ADDR<29>	B21	A_29	
CPU_ADDR<30>	D20	A_30	
CPU_ADDR<31>	A21	A_31	
CPU_CI_L	G26	CI	
CPU_GBL_L	A29	GBL	
CPU_TBST_L	A28	TBST	
CPU_TSIZ<0>	G24	TSIZ_0	
CPU_TSIZ<1>	H24	TSIZ_1	
CPU_TSIZ<2>	D26	TSIZ_2	
CPU_TT<0>	E25	TT_0	
CPU_TT<1>	G25	TT_1	
CPU_TT<2>	B28	TT_2	
CPU_TT<3>	D27	TT_3	
CPU_TT<4>	J25	TT_4	
CPU_WT_L	D28	WT	
CPU_AACK_L	B29	AACK	NO BUS KEEPER - PU
CPU_ARTRY_L	H23	ARTRY	NO BUS KEEPER - PU
CPU_HIT_L	B31	HIT	INPUT - PU
CPU_QREQ_L	A32	QREQ	INPUT - PD
CPU_QACK_L	G27	QACK	NO BUS KEEPER - ?
INT_SUSPEND_REQ_L	AK9	SUSPENDREQ	
INT_SUSPEND_ACK_L	AM8	SUSPENDACK	
INT_CPUFB_IN	J24	CPU_FB_IN	
INT_CPUFB_OUT	H16	CPU_FB_OUT	NO BUS KEEPER - PU
SYSCLK_LA_TP	G8	ANALYZER_CLK	
CPU_CLK_EN	AH9	STOPCPUCLK	INPUT - PU
INTREPID_ACS_REF	H13	ACS_REF	NO BUS KEEPER - ?
			NO BUS KEEPER - ?
			NO BUS KEEPER - ?
SYSCLK_CPU_UF	J15	CPU_CLK	NO BUS KEEPER - PU
			NO BUS KEEPER - PU
CPU_TBEN	A31	TBEN	NO BUS KEEPER - PU

Vin = Intrepid Vcore (1.5V)
Vout = MaxBus rail (1.8V)

INTREPID OUTPUTS HIGH BY DEFAULT

VSSA_7 (PLL6) H25

MAXBUS INTERFACE

DBG	A30	CPU_DBG_L	
DRDY	G28	CPU_DRDY_L	
DTI_0	K25	CPU_DTI<0>	
DTI_1	D29	CPU_DTI<1>	
DTI_2	B30	CPU_DTI<2>	
TA	E27	CPU_TA_L	
TEA	E28	CPU_TEA_L	

D_0	D10	CPU_DATA<0>	
D_1	G12	CPU_DATA<1>	
D_2	E11	CPU_DATA<2>	
D_3	H11	CPU_DATA<3>	
D_4	B9	CPU_DATA<4>	
D_5	B8	CPU_DATA<5>	
D_6	A9	CPU_DATA<6>	
D_7	A8	CPU_DATA<7>	
D_8	E12	CPU_DATA<8>	
D_9	D11	CPU_DATA<9>	
D_10	B10	CPU_DATA<10>	
D_11	J13	CPU_DATA<11>	
D_12	A10	CPU_DATA<12>	
D_13	D12	CPU_DATA<13>	
D_14	E13	CPU_DATA<14>	
D_15	G13	CPU_DATA<15>	
D_16	B11	CPU_DATA<16>	
D_17	D13	CPU_DATA<17>	
D_18	A11	CPU_DATA<18>	
D_19	G14	CPU_DATA<19>	
D_20	H14	CPU_DATA<20>	
D_21	E14	CPU_DATA<21>	
D_22	B12	CPU_DATA<22>	
D_23	G15	CPU_DATA<23>	
D_24	B13	CPU_DATA<24>	
D_25	H15	CPU_DATA<25>	
D_26	D14	CPU_DATA<26>	
D_27	B14	CPU_DATA<27>	
D_28	A12	CPU_DATA<28>	
D_29	G16	CPU_DATA<29>	
D_30	E15	CPU_DATA<30>	
D_31	J16	CPU_DATA<31>	
D_32	D15	CPU_DATA<32>	
D_33	A14	CPU_DATA<33>	
D_34	A13	CPU_DATA<34>	
D_35	D16	CPU_DATA<35>	
D_36	E16	CPU_DATA<36>	
D_37	G17	CPU_DATA<37>	
D_38	B15	CPU_DATA<38>	
D_39	H17	CPU_DATA<39>	
D_40	A15	CPU_DATA<40>	
D_41	B16	CPU_DATA<41>	
D_42	E17	CPU_DATA<42>	
D_43	A16	CPU_DATA<43>	
D_44	J18	CPU_DATA<44>	
D_45	H18	CPU_DATA<45>	
D_46	D17	CPU_DATA<46>	
D_47	G18	CPU_DATA<47>	
D_48	A17	CPU_DATA<48>	
D_49	B17	CPU_DATA<49>	
D_50	E18	CPU_DATA<50>	
D_51	B18	CPU_DATA<51>	
D_52	D18	CPU_DATA<52>	
D_53	A18	CPU_DATA<53>	
D_54	A19	CPU_DATA<54>	
D_55	H19	CPU_DATA<55>	
D_56	B19	CPU_DATA<56>	
D_57	J19	CPU_DATA<57>	
D_58	A20	CPU_DATA<58>	
D_59	D19	CPU_DATA<59>	
D_60	E19	CPU_DATA<60>	
D_61	G19	CPU_DATA<61>	
D_62	B20	CPU_DATA<62>	
D_63	G20	CPU_DATA<63>	

FB BUFFER HAS 50 OHM OUTPUT IMPEDANCE

R197 511 1% 1/16W MF 402

R144 0 5% 1/16W MF 402

R137 1K 1% 1/16W MF 402

SHORT = 1" SHORTER THAN MATCHED LENGTH
LONG = 1" LONGER THAN MATCHED LENGTH

R167 0 5% 1/16W MF 402	INT_CPUFB_OUT	INT_CPUFB_OUT_SHORT	R215 0 5% 1/16W MF 402	INT_CPUFB_OUT_NORM	R207 0 5% 1/16W MF 402 NO STUFF
R225 0 5% 1/16W MF 402 NO STUFF				R208 0 5% 1/16W MF 402 NO STUFF	
	INT_CPUFB_IN		R226 0 5% 1/16W MF 402	INT_CPUFB_IN_NORM	R196 0 5% 1/16W MF 402 NO STUFF

INT_CPUFB_LONG

MAXBUS PULL-UPS

MAXBUS_SLEEP

CPU_TS_L	RP21 10K 5% 1/16W SM1	CPU_TA_L	RP21 10K 5% 1/16W SM1
CPU_ARTRY_L	RP21 10K 5% 1/16W SM1	CPU_BR_L	RP23 10K 5% 1/16W SM1
CPU_HIT_L	RP24 10K 5% 1/16W SM1	CPU_DRDY_L	RP23 10K 5% 1/16W SM1
CPU_TEA_L	RP23 10K 5% 1/16W SM1	CPU_AACK_L	RP23 10K 5% 1/16W SM1
CPU_DBG_L	RP24 10K 5% 1/16W SM1	CPU_BG_L	RP21 10K 5% 1/16W SM1
CPU_QREQ_L	RP24 10K 5% 1/16W SM1		

INTREPID BOOT STRAPS

BIT 56 TO 63

MAXBUS_SLEEP

R140	R161	R175	R132	R131	R150	R174	R182
NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF
CPU_DATA<56>	CPU_DATA<57>	CPU_DATA<58>	CPU_DATA<59>	CPU_DATA<60>	CPU_DATA<61>	CPU_DATA<62>	CPU_DATA<63>

R654	R669	R677	R646	R647	R660	R678	R685
10K 5% 1/16W MF 402						NO STUFF	

Spare | Spare | Spare | 0: FSB 1.05V (CPU input voltage) 1: FSB 1.5V | 0: FSB 1.05V (CPU input voltage) 1: FSB 1.5V | 0: Disable PHY interface 1: Enable PHY interface | 0: Legacy interface 1: B-mode interface | Processor Bus Mode 0: 60X Bus (G3) 1: 6XX Bus (G4)

PCI1_RST2_L / PCI1_GNT2_L 0: GPIO[0] 1: GPIO[0]

PCI1_RST1_L / PCI1_GNT1_L 0: GPIO[1] 1: GPIO[1]

PCI1_RST0_L / PCI1_GNT0_L 0: GPIO[2] 1: GPIO[2]

Intrepid MaxBus

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 8 OF 44	

SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

PINS ARE SWAPABLE FOR RPAKS

U45
INTREPID-REV2.1
BGA
(2 OF 9)
CRITICAL

DDR MEMORY INTERFACE

DDR_DATA_0	AK32	H35	MEM_ADDR<0>
DDR_DATA_1	AK33	G35	MEM_ADDR<1>
DDR_DATA_2	AK31	G36	MEM_ADDR<2>
DDR_DATA_3	AK35	F36	MEM_ADDR<3>
DDR_DATA_4	AK36	F35	MEM_ADDR<4>
DDR_DATA_5	AJ32	E35	MEM_ADDR<5>
DDR_DATA_6	AJ35	E36	MEM_ADDR<6>
DDR_DATA_7	AJ36	G32	MEM_ADDR<7>
DDR_DATA_8	AG33	D36	MEM_ADDR<8>
DDR_DATA_9	AG35	H36	MEM_ADDR<9>
DDR_DATA_10	AH35	G33	MEM_ADDR<10>
DDR_DATA_11	AG36	H33	MEM_ADDR<11>
DDR_DATA_12	AH36	D35	MEM_ADDR<12>
DDR_DATA_13	AH32	L30	MEM_BA<0>
DDR_DATA_14	AG32	M29	MEM_BA<1>
DDR_DATA_15	AG31	AN34	MEM_CS_L<0>
DDR_DATA_16	AE32	AN36	MEM_CS_L<1>
DDR_DATA_17	AF35	AL35	MEM_CS_L<2>
DDR_DATA_18	AF36	AL33	MEM_CS_L<3>
DDR_DATA_19	AE36	AJ31	MEM_DQS<0>
DDR_DATA_20	AE35	AH31	MEM_DQS<1>
DDR_DATA_21	AE33	AD32	MEM_DQS<2>
DDR_DATA_22	AD36	AB30	MEM_DQS<3>
DDR_DATA_23	AD35	V30	MEM_DQS<4>
DDR_DATA_24	AA36	P32	MEM_DQS<5>
DDR_DATA_25	AA35	N29	MEM_DQS<6>
DDR_DATA_26	AA33	L32	MEM_DQS<7>
DDR_DATA_27	AB36	AJ33	MEM_DQM<0>
DDR_DATA_28	AB35	AH33	MEM_DQM<1>
DDR_DATA_29	AC36	AD33	MEM_DQM<2>
DDR_DATA_30	AA32	AC35	MEM_DQM<3>
DDR_DATA_31	AB33	T35	MEM_DQM<4>
DDR_DATA_32	V36	T33	MEM_DQM<5>
DDR_DATA_33	U33	N32	MEM_DQM<6>
DDR_DATA_34	U32	L33	MEM_DQM<7>
DDR_DATA_35	V35	L29	MEM_RAS_L
DDR_DATA_36	T30	H32	MEM_CAS_L
DDR_DATA_37	U36	K30	MEM_WE_L
DDR_DATA_38	U35	AM35	MEM_CKE<0>
DDR_DATA_39	T36	AM35	MEM_CKE<1>
DDR_DATA_40	P33	AM36	MEM_CKE<2>
DDR_DATA_41	R30	AL36	MEM_CKE<3>
DDR_DATA_42	P35	AB32	MEM_MUXSEL_H<0>
DDR_DATA_43	P36	AE29	MEM_MUXSEL_H<1>
DDR_DATA_44	R36	N30	MEM_MUXSEL_L<0>
DDR_DATA_45	R35	T32	MEM_MUXSEL_L<1>
DDR_DATA_46	R33	Y32	SYSCLK_DDRCLK_A0_UF
DDR_DATA_47	R32	Y33	SYSCLK_DDRCLK_A0_L_UF
DDR_DATA_48	N35	Y35	SYSCLK_DDRCLK_A1_UF
DDR_DATA_49	M36	Y36	SYSCLK_DDRCLK_A1_L_UF
DDR_DATA_50	L35	Y30	INT_DDRCLK2_P_TP
DDR_DATA_51	M35	W30	INT_DDRCLK2_N_TP
DDR_DATA_52	M33	W32	SYSCLK_DDRCLK_B0_UF
DDR_DATA_53	L36	W33	SYSCLK_DDRCLK_B0_L_UF
DDR_DATA_54	N33	V33	SYSCLK_DDRCLK_B1_UF
DDR_DATA_55	M30	V32	SYSCLK_DDRCLK_B1_L_UF
DDR_DATA_56	J32	W35	INT_DDRCLK5_P_TP
DDR_DATA_57	J33	W36	INT_DDRCLK5_N_TP
DDR_DATA_58	J35	AA22	INT_MEM_REF_H
DDR_DATA_59	K32	Y22	INT_MEM_VREF
DDR_DATA_60	K33	T22	
DDR_DATA_61	J36		
DDR_DATA_62	K36		
DDR_DATA_63	K35		

DDRCS_0 … DDRCS_3: ‘0’ & ‘1’ GO TO SLOT A; ‘2’ & ‘3’ GO TO SLOT B

DDRCKE0 … DDRCKE3: ‘0’ & ‘1’ GO TO SLOT A; ‘2’ & ‘3’ GO TO SLOT B

DDR_SELHI_0, DDR_SELHI_1, DDR_SELLO_0, DDR_SELLO_1: ‘0’S ARE SAME POLARITY (ACTIVE-LO); ‘1’S ARE SAME POLARITY (ACTIVE-HI)

DDR_MCLK_0_P … DDR_MCLK_5_N

DDR_VREF_0, DDR_VREF_1

R199 1K 1% 1/16W MF 402

MEM_VREF

+2_5V_INTREPID

R198 10K 1% 1/16W MF 402

R191 10K 1% 1/16W MF 402

C245 0.1UF 20% 10V CERM 402

INT_MEM_VREF

CLOCKS

SYSCLK_DDRCLK_A1_UF	RP33 22	4	SYSCLK_DDRCLK_A1
SYSCLK_DDRCLK_A1_L_UF	RP33 22	3	SYSCLK_DDRCLK_A1_L
SYSCLK_DDRCLK_A0_UF	RP34 22	1	SYSCLK_DDRCLK_A0
SYSCLK_DDRCLK_A0_L_UF	RP34 22	2	SYSCLK_DDRCLK_A0_L
SYSCLK_DDRCLK_B1_UF	RP33 22	2	SYSCLK_DDRCLK_B1
SYSCLK_DDRCLK_B1_L_UF	RP33 22	1	SYSCLK_DDRCLK_B1_L
SYSCLK_DDRCLK_B0_UF	RP34 22	3	SYSCLK_DDRCLK_B0
SYSCLK_DDRCLK_B0_L_UF	RP34 22	4	SYSCLK_DDRCLK_B0_L

CS

MEM_CS_L<0>	RP36 22	1	RAM_CS_L<0>
MEM_CS_L<1>	RP36 22	3	RAM_CS_L<1>
MEM_CS_L<2>	RP35 22	4	RAM_CS_L<2>
MEM_CS_L<3>	RP35 22	2	RAM_CS_L<3>

CKE

MEM_CKE<0>	RP36 22	2	RAM_CKE<0>
MEM_CKE<1>	RP36 22	4	RAM_CKE<1>
MEM_CKE<2>	RP35 22	1	RAM_CKE<2>
MEM_CKE<3>	RP35 22	3	RAM_CKE<3>

ADDR

MEM_ADDR<0>	RP31 22	1	RAM_ADDR<0>
MEM_ADDR<1>	RP25 22	1	RAM_ADDR<1>
MEM_ADDR<2>	RP25 22	2	RAM_ADDR<2>
MEM_ADDR<3>	RP25 22	4	RAM_ADDR<3>
MEM_ADDR<4>	RP25 22	3	RAM_ADDR<4>
MEM_ADDR<5>	RP30 22	1	RAM_ADDR<5>
MEM_ADDR<6>	RP30 22	2	RAM_ADDR<6>
MEM_ADDR<7>	RP31 22	3	RAM_ADDR<7>
MEM_ADDR<8>	RP30 22	4	RAM_ADDR<8>
MEM_ADDR<9>	RP31 22	2	RAM_ADDR<9>
MEM_ADDR<10>	RP31 22	4	RAM_ADDR<10>
MEM_ADDR<11>	RP26 22	4	RAM_ADDR<11>
MEM_ADDR<12>	RP30 22	3	RAM_ADDR<12>

BA

MEM_BA<0>	RP26 22	2	RAM_BA<0>
MEM_BA<1>	RP26 22	1	RAM_BA<1>

CNTL

MEM_WE_L	RP26 22	3	RAM_WE_L
MEM_CAS_L	R250 22	1	RAM_CAS_L
MEM_RAS_L	R238 22	1	RAM_RAS_L

All: 5% 1/16W SM1

1MB BOOT ROM

+3V_MAIN

C460 2.2UF 20% 10V CERM 805

C470 0.1UF 20% 10V CERM 402

C479 0.1UF 20% 10V CERM 402

U17
3.3V
TSOP
OMIT

PCI_AD<0>	A0	DQ0	PCI_AD<24>
PCI_AD<1>	A1	DQ1	PCI_AD<25>
PCI_AD<2>	A2	DQ2	PCI_AD<26>
PCI_AD<3>	A3	DQ3	PCI_AD<27>
PCI_AD<4>	A4	DQ4	PCI_AD<28>
PCI_AD<5>	A5	DQ5	PCI_AD<29>
PCI_AD<6>	A6	DQ6	PCI_AD<30>
PCI_AD<7>	A7	DQ7	PCI_AD<31>
PCI_AD<8>	A8		
PCI_AD<9>	A9		
PCI_AD<10>	A10		
PCI_AD<11>	A11		
PCI_AD<12>	A12		
PCI_AD<13>	A13		
PCI_AD<14>	A14		
PCI_AD<15>	A15		
PCI_AD<16>	A16		
PCI_AD<17>	A17		
PCI_AD<18>	A18		
PCI_AD<19>	A19		
PCI_AD<20>	A20		
ROM_ONBOARD_CS_L	CE		
ROM_OE_L	OE		
ROM_RW_L	WE		
ROM_WP_L	WP		
INT_RESET_L	PWD		
	GND		

VPP = 11, VCC = 30, GND = 23, 39, 31

+3V_MAIN

R338 10K 5% 1/16W MF 402

R386 10K 5% 1/16W MF 402

R357 1K 5% 1/16W MF 402

ROM_CS_L

OVERRIDE ROM MODULE
INTERCEPTS ROM CHIP SELECT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S2103	1	IC, BOOTROM,Q16, SERVICE_BOM	U17	CRITICAL	?

PULL-DOWN RESISTORS TO ENSURE
CKE STAYS LOW AFTER INTREPID
2.5V I/O SHUTS OFF

RAM_CKE<0>, RAM_CKE<1>, RAM_CKE<2>, RAM_CKE<3>

R500 10K 5% 1/16W MF 402

R439 10K 5% 1/16W MF 402

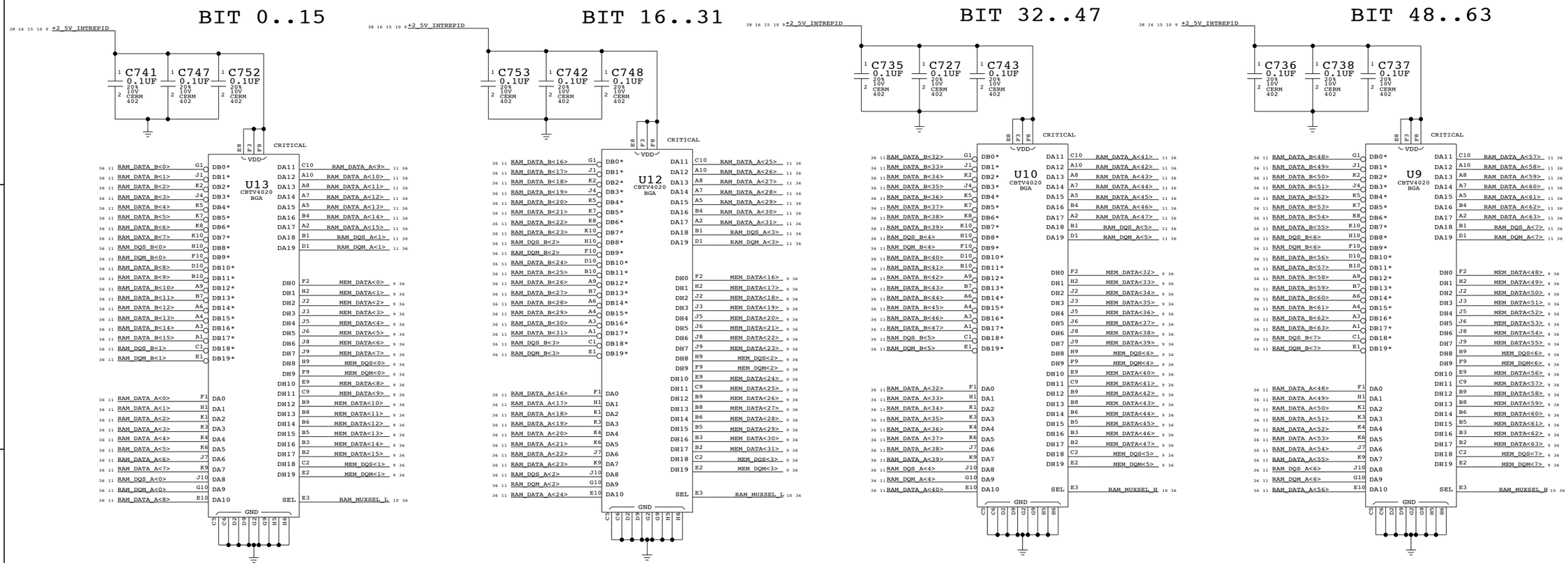
R409 10K 5% 1/16W MF 402

R387 10K 5% 1/16W MF 402

INT - DDR/BOOTROM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 9 OF 44	



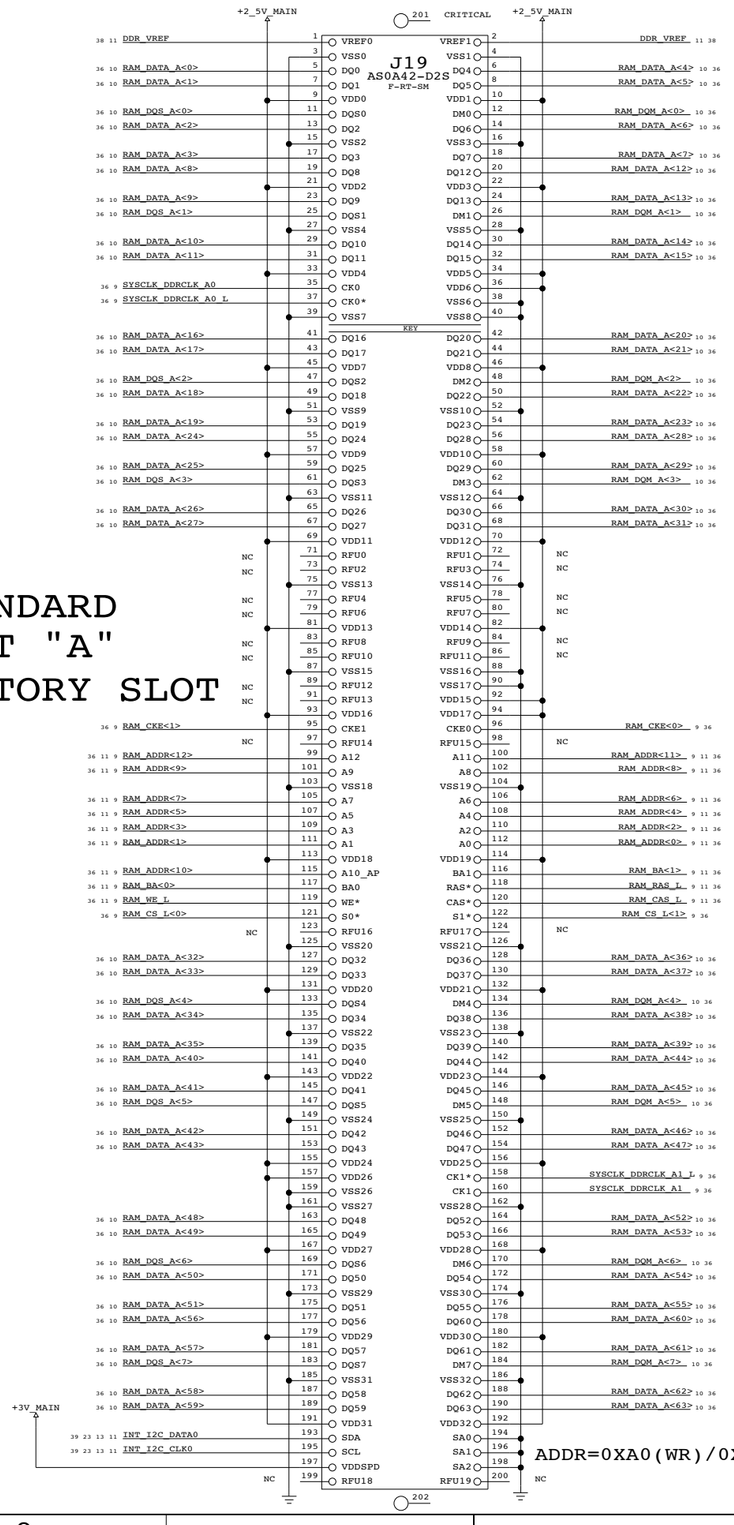
SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND
MEM_MUXSEL_H<0> AND MEM_MUXSEL_L<0> ARE ACTIVE LOW
MEM_MUXSEL_H<1> AND MEM_MUXSEL_L<1> ARE ACTIVE HIGH

ADDED 0 OHM RESISTORS IN CASE POLARITY IS WRONG

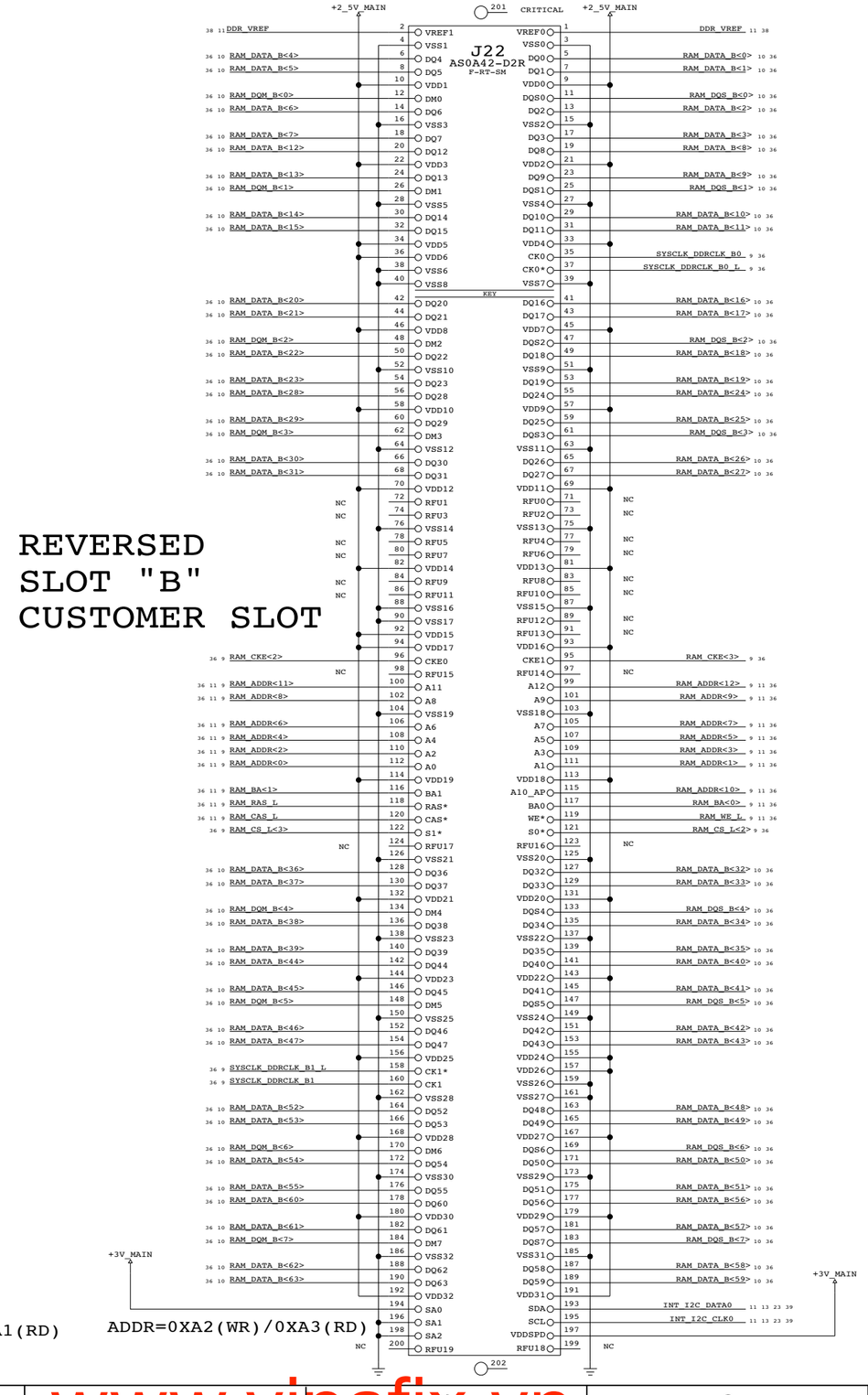
16BIT 2:1 DDR MUXES

APPLE COMPUTER INC.

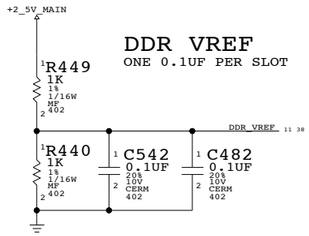
SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 10 OF 44	

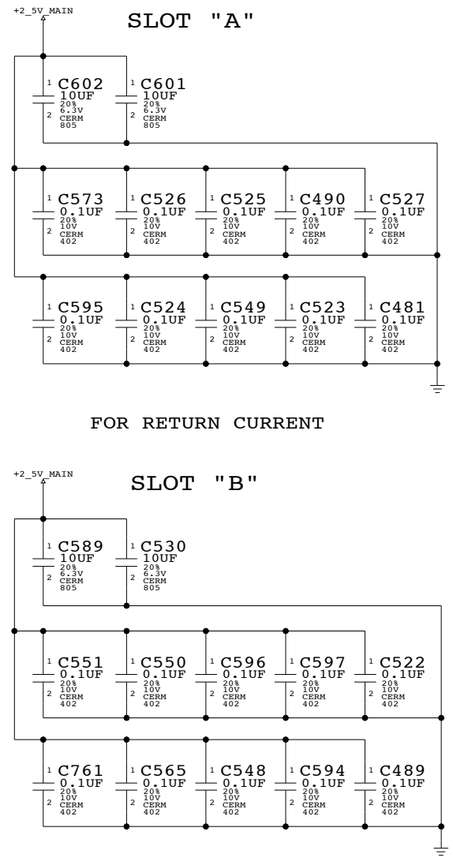


STANDARD
SLOT "A"
FACTORY SLOT



REVERSED
SLOT "B"
CUSTOMER SLOT





DDR SODIMM CONNS

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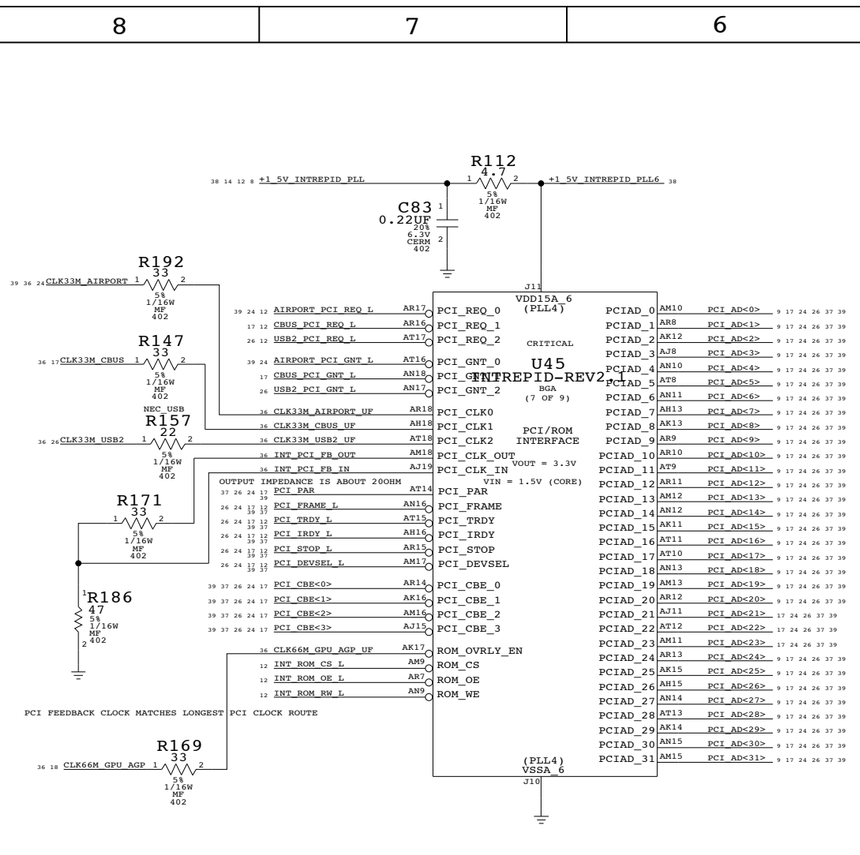
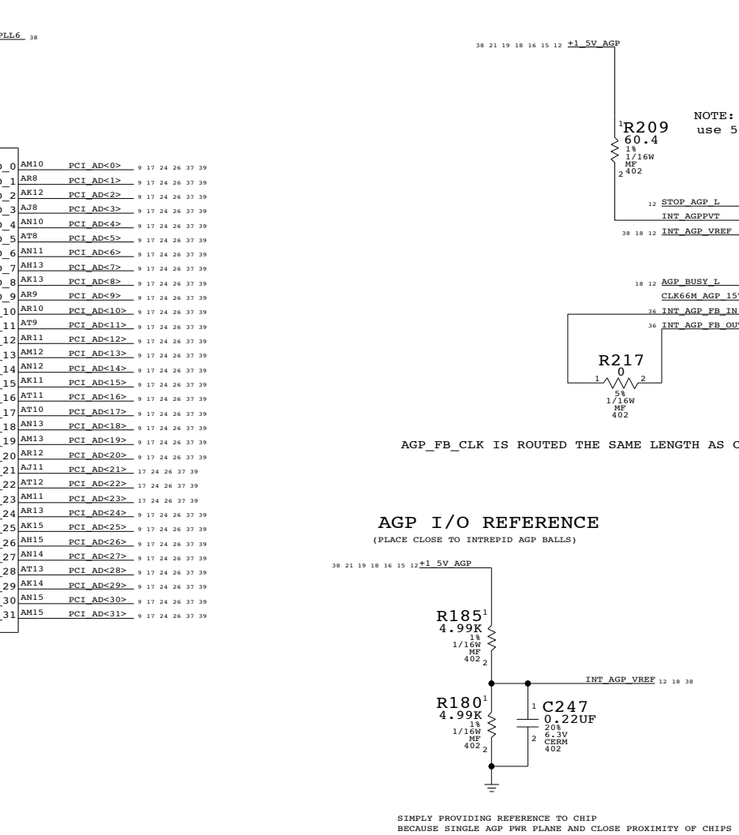
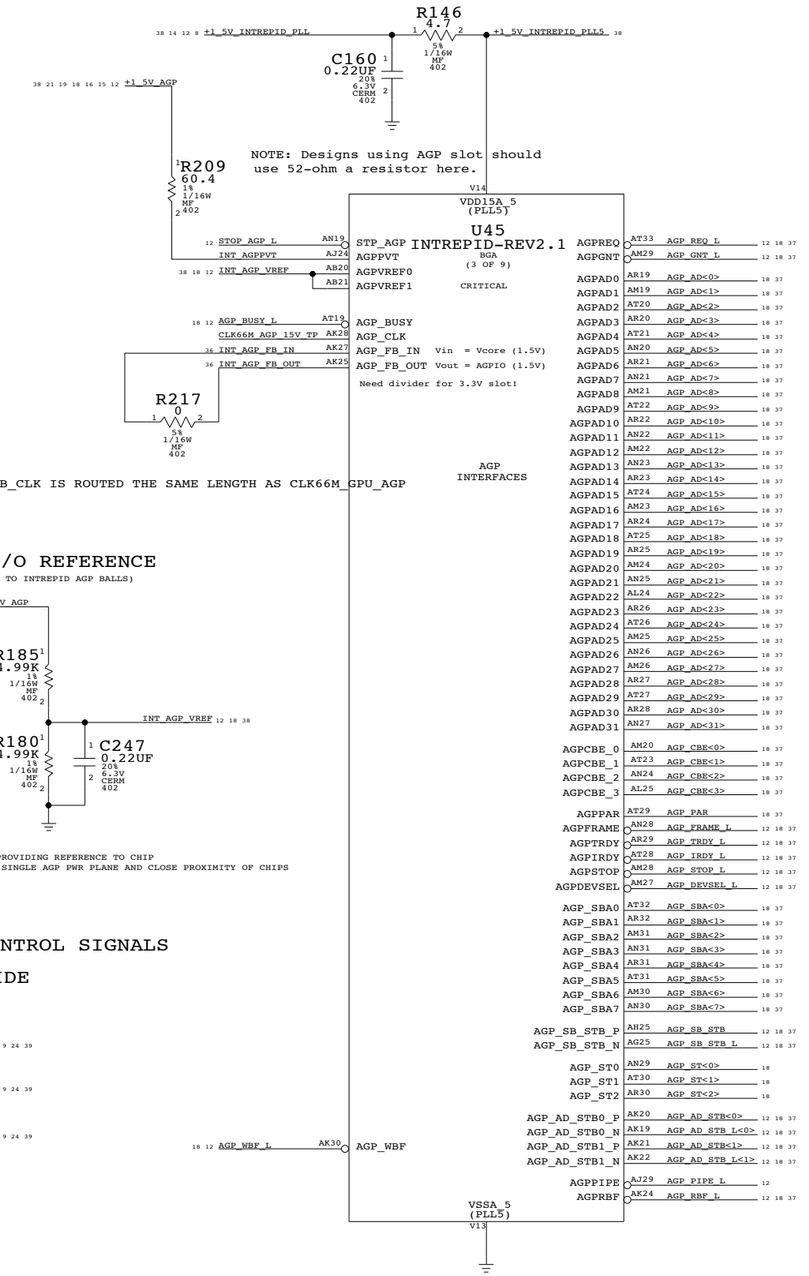
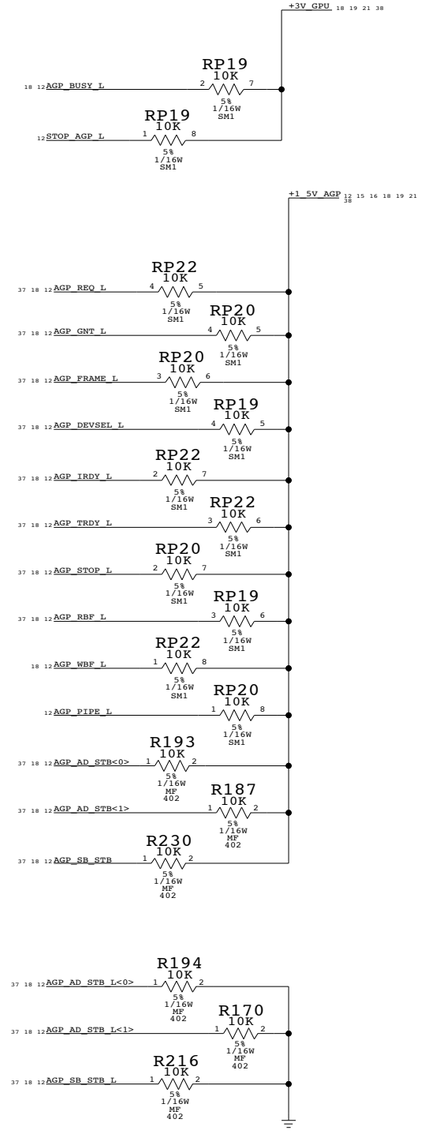
SIZE	DRAWING NUMBER	REV.
D	051-6582	C

SCALE NONE | SHT 11 OF 44









INTREPID AGP/PCI

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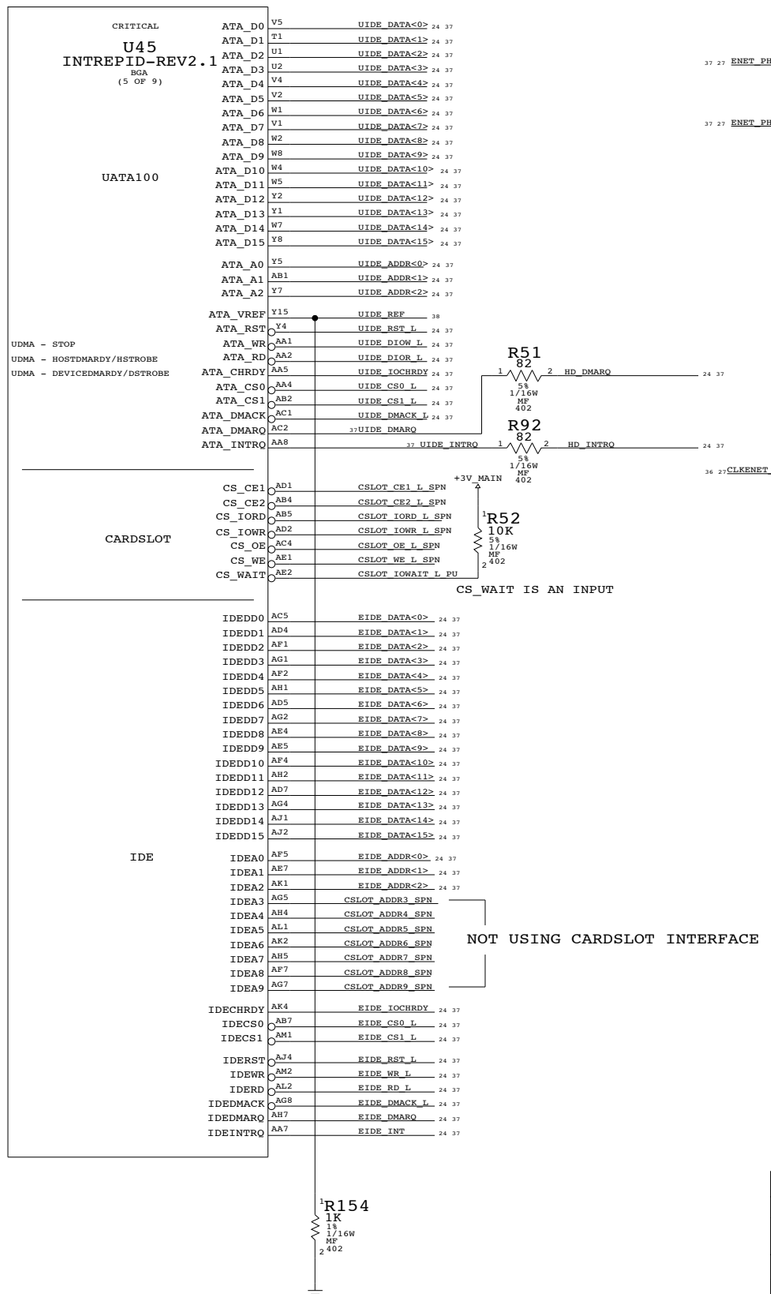
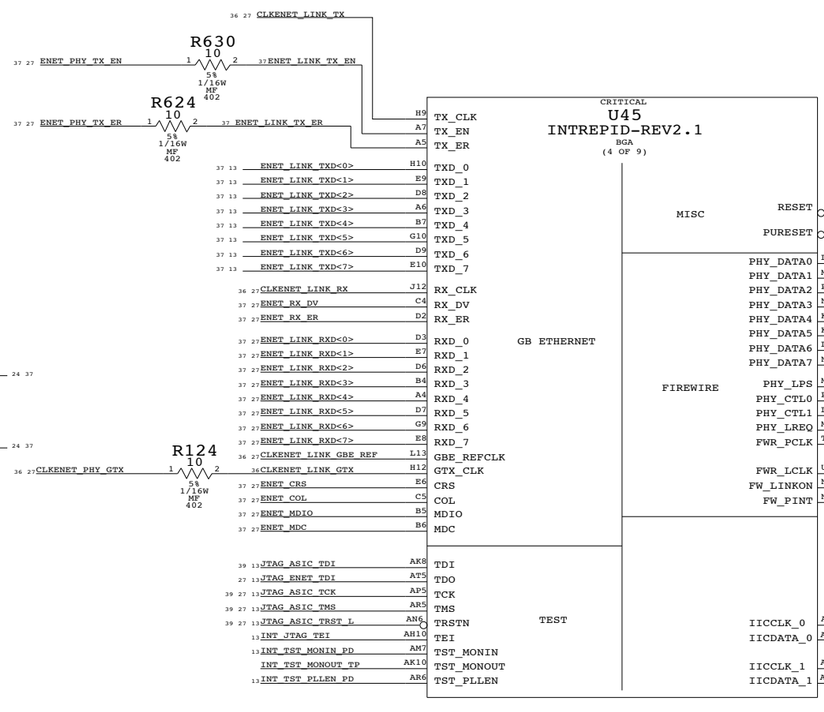
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C

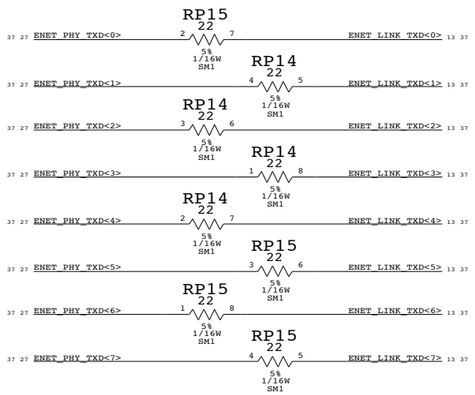
SCALE: NONE

SHT 12 OF 44



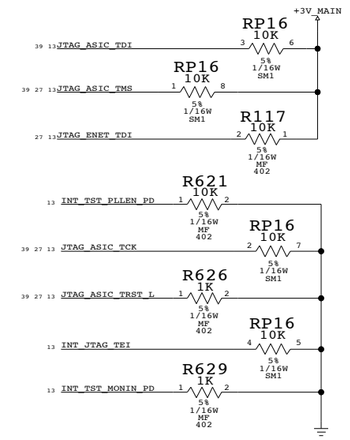


ENET_TXD SERIES TERMINATION

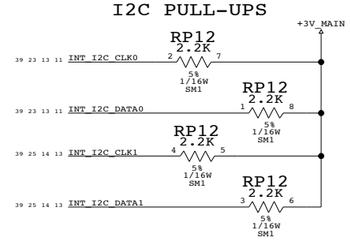


JTG_RSTN_L	TST_TEI_H	JTG_TDO_H (I/O)	JTG_TDI_H (I/O)	TST_PLLEN_H	ANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	EXTPLL SHUTDOWN (OUTPUT)	DDR_ TPDENABLE (OUTPUT)	0	(OUTPUT)	NORMAL OPERATION
0	0	(OUTPUT)	0(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	HWPLL_ TESTSEL5 (INPUT)	1(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0(I)	0(I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0(I)	1(I)	0	X(I)	ATPG IDDQ
0	1	0(I)	1(I)	1	X(I)	TEST TRI-STATE
0	1	1(I)	0(I)	0	X(I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1(I)	0(I)	1	X(I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1(I)	1(I)	X	X(I)	FUNCTIONAL TEST IDDQ

TEST PULL-UPS/DOWNS



I2C PULL-UPS



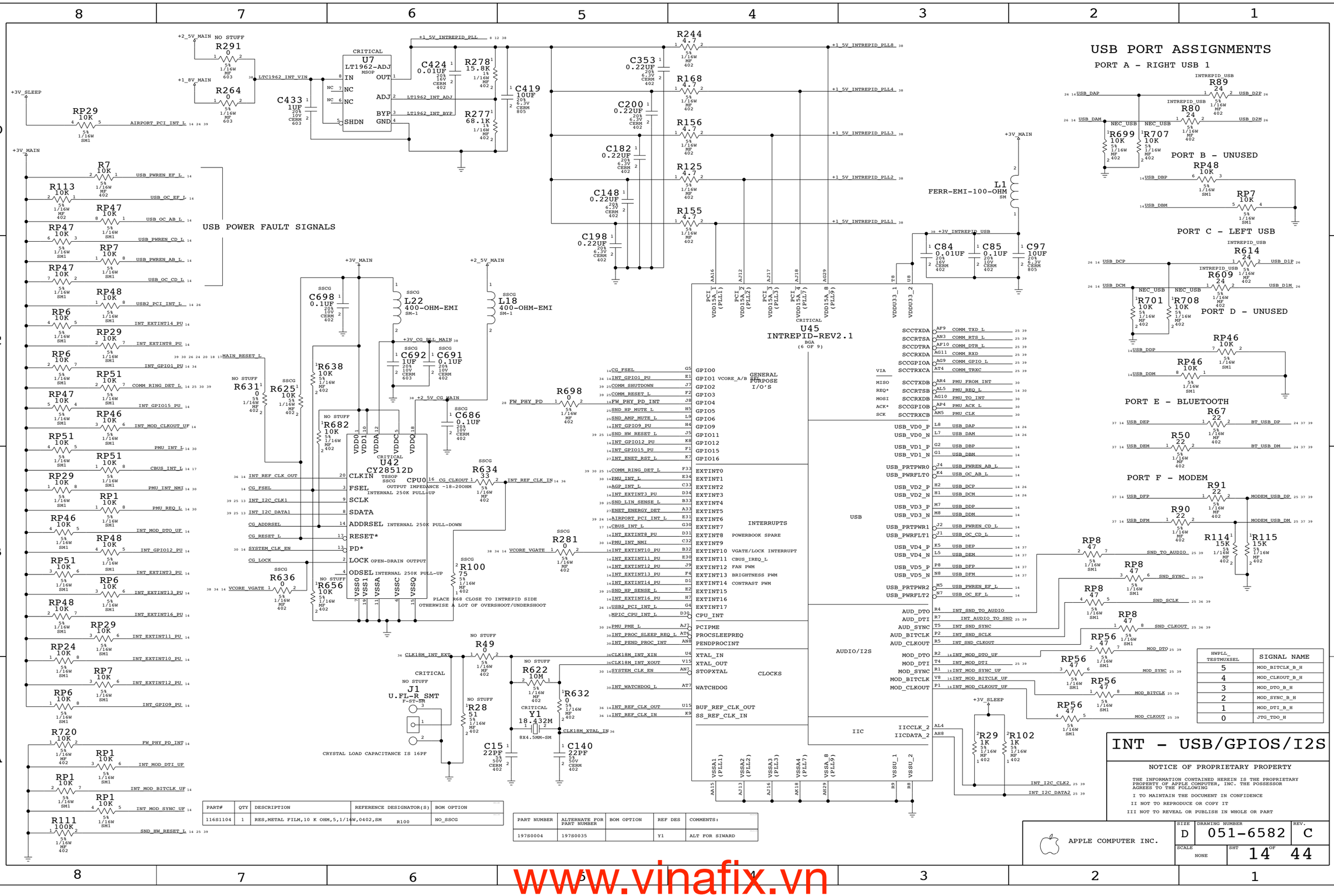
BUS / ADDR	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
A0-WR A1-RD	RAM - STANDARD J20 - PG 12	N/A	N/A	N/A
A2-WR A3-RD	RAM - REVERSED J23 - PG 12	N/A	N/A	N/A
AC-WR AD-RD	N/A	N/A	DASH MODEM J9 - PG 25	N/A
AE-WR AF-RD	BOOTBANG E2PROM U37 - PG 23	N/A	N/A	N/A
84-WR 85-RD	LMU U36 - PG 23	N/A	N/A	N/A
58-WR 59-RD	N/A	FAN CONTROLLER U3 - PG 24	N/A	N/A
6A-WR 6B-RD	N/A	N/A	SNAPPER SOUND J12 - PG 24	N/A
D0-WR D1-RD	N/A	CLOCK SLEW SSCG U56 - PG 15	N/A	N/A

ADDR LSB INDICATES READ ('1') OR WRITE ('0') MODES

INT - ENET/FW/UATA EIDE/I2C

APPLE COMPUTER INC.

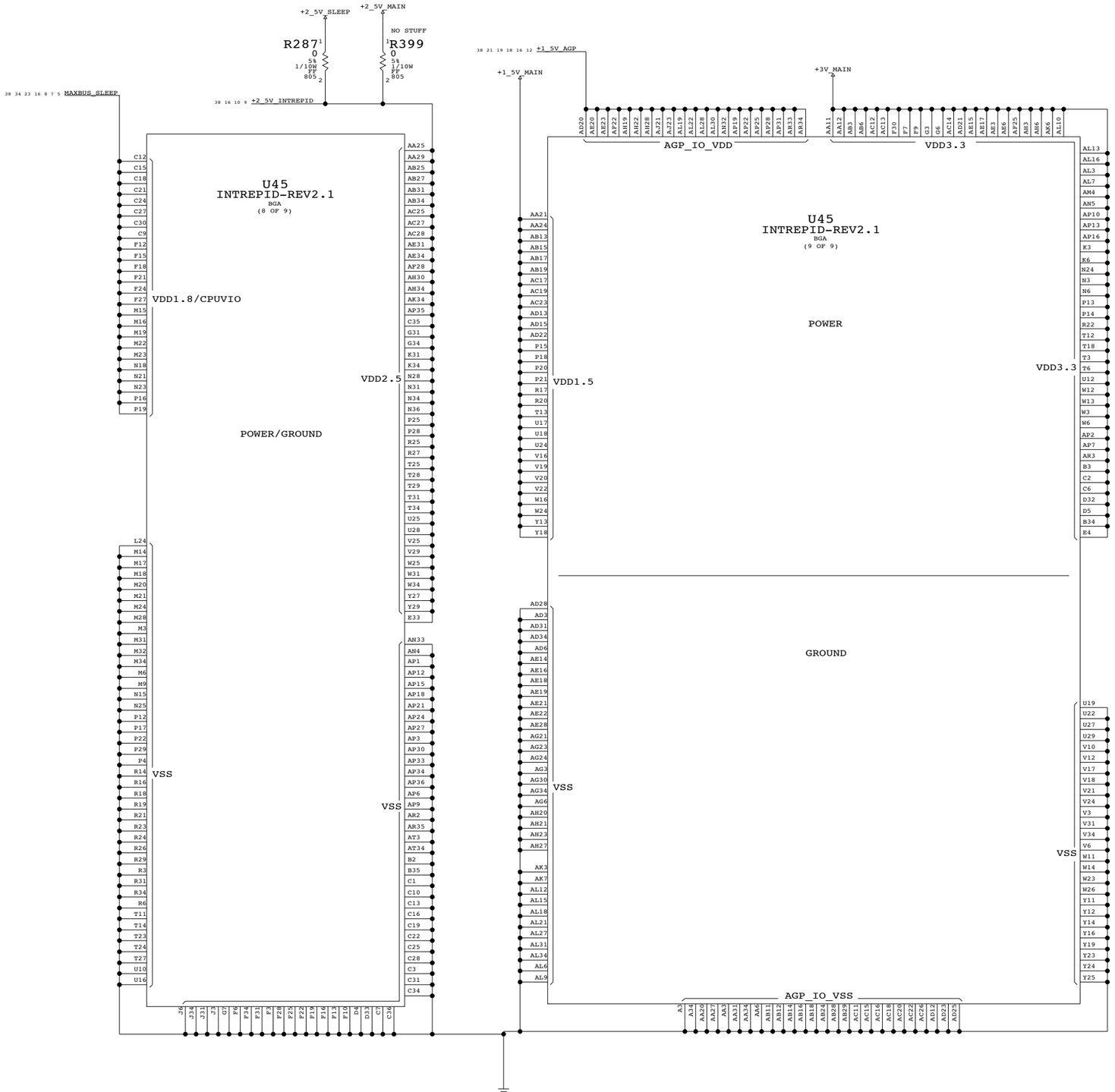
SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 13 OF 44	



HWPLL_TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES,METAL FILM,10 K OHM,5,1/16W,0402,SM	R100	NO_SSCG

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0004	197S0035		Y1	ALT FOR SIWARD



Intrepid Power

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SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 15 OF 44	

INTREPID MAXBUS DECOUPLING

24 Balls
4 X 10UF (0805)
32 X 0.22UF (0402)

38 34 23 15 8 7 5 MAXBUS_SLEEP

C204 10uF 20% 6.3V CERM 805 1 2
C348 10uF 20% 6.3V CERM 805 1 2
C236 10uF 20% 6.3V CERM 805 1 2
C196 10uF 20% 6.3V CERM 805 1 2

C239 0.22uF 20% 6.3V CERM 402 1 2
C240 0.22uF 20% 6.3V CERM 402 1 2
C350 0.22uF 20% 6.3V CERM 402 1 2
C312 0.22uF 20% 6.3V CERM 402 1 2
C176 0.22uF 20% 6.3V CERM 402 1 2
C288 0.22uF 20% 6.3V CERM 402 1 2
C313 0.22uF 20% 6.3V CERM 402 1 2
C94 0.22uF 20% 6.3V CERM 402 1 2
C286 0.22uF 20% 6.3V CERM 402 1 2
C158 0.22uF 20% 6.3V CERM 402 1 2

C174 0.22uF 20% 6.3V CERM 402 1 2
C206 0.22uF 20% 6.3V CERM 402 1 2
C259 0.22uF 20% 6.3V CERM 402 1 2
C237 0.22uF 20% 6.3V CERM 402 1 2
C238 0.22uF 20% 6.3V CERM 402 1 2
C95 0.22uF 20% 6.3V CERM 402 1 2
C117 0.22uF 20% 6.3V CERM 402 1 2
C241 0.22uF 20% 6.3V CERM 402 1 2
C260 0.22uF 20% 6.3V CERM 402 1 2
C314 0.22uF 20% 6.3V CERM 402 1 2

C173 0.22uF 20% 6.3V CERM 402 1 2
C171 0.22uF 20% 6.3V CERM 402 1 2
C175 0.22uF 20% 6.3V CERM 402 1 2
C226 0.22uF 20% 6.3V CERM 402 1 2
C172 0.22uF 20% 6.3V CERM 402 1 2
C207 0.22uF 20% 6.3V CERM 402 1 2
C118 0.22uF 20% 6.3V CERM 402 1 2
C287 0.22uF 20% 6.3V CERM 402 1 2
C119 0.22uF 20% 6.3V CERM 402 1 2
C349 0.22uF 20% 6.3V CERM 402 1 2

C205 0.22uF 20% 6.3V CERM 402 1 2
C209 0.22uF 20% 6.3V CERM 402 1 2

INTREPID AGP I/O DECOUPLING

21 Balls
4 X 10UF (0805)
24 X 0.22UF (0402)

38 21 19 18 15 12 +1_5V_AGP

C371 10uF 20% 6.3V CERM 805 1 2
C231 10uF 20% 6.3V CERM 805 1 2
C281 10uF 20% 6.3V CERM 805 1 2
C394 10uF 20% 6.3V CERM 805 1 2

C356 0.22uF 20% 6.3V CERM 402 1 2
C297 0.22uF 20% 6.3V CERM 402 1 2
C268 0.22uF 20% 6.3V CERM 402 1 2
C217 0.22uF 20% 6.3V CERM 402 1 2
C355 0.22uF 20% 6.3V CERM 402 1 2
C267 0.22uF 20% 6.3V CERM 402 1 2
C250 0.22uF 20% 6.3V CERM 402 1 2
C298 0.22uF 20% 6.3V CERM 402 1 2
C377 0.22uF 20% 6.3V CERM 402 1 2
C216 0.22uF 20% 6.3V CERM 402 1 2

C228 0.22uF 20% 6.3V CERM 402 1 2
C230 0.22uF 20% 6.3V CERM 402 1 2
C265 0.22uF 20% 6.3V CERM 402 1 2
C378 0.22uF 20% 6.3V CERM 402 1 2
C357 0.22uF 20% 6.3V CERM 402 1 2
C229 0.22uF 20% 6.3V CERM 402 1 2
C325 0.22uF 20% 6.3V CERM 402 1 2
C393 0.22uF 20% 6.3V CERM 402 1 2
C324 0.22uF 20% 6.3V CERM 402 1 2
C323 0.22uF 20% 6.3V CERM 402 1 2

C251 0.22uF 20% 6.3V CERM 402 1 2
C266 0.22uF 20% 6.3V CERM 402 1 2
C249 0.22uF 20% 6.3V CERM 402 1 2

INTREPID DDR DECOUPLING

44 Balls
4 X 10UF (0805)
51 X 0.22UF (0402)

38 15 10 9 +2_5V_INTREPID

C422 10uF 20% 6.3V CERM 805 1 2
C417 10uF 20% 6.3V CERM 805 1 2
C418 10uF 20% 6.3V CERM 805 1 2
C423 10uF 20% 6.3V CERM 805 1 2

C407 0.22uF 20% 6.3V CERM 402 1 2
C391 0.22uF 20% 6.3V CERM 402 1 2
C310 0.22uF 20% 6.3V CERM 402 1 2
C317 0.22uF 20% 6.3V CERM 402 1 2
C480 0.22uF 20% 6.3V CERM 402 1 2
C390 0.22uF 20% 6.3V CERM 402 1 2
C370 0.22uF 20% 6.3V CERM 402 1 2
C320 0.22uF 20% 6.3V CERM 402 1 2
C365 0.22uF 20% 6.3V CERM 402 1 2
C366 0.22uF 20% 6.3V CERM 402 1 2

C367 0.22uF 20% 6.3V CERM 402 1 2
C292 0.22uF 20% 6.3V CERM 402 1 2
C295 0.22uF 20% 6.3V CERM 402 1 2
C403 0.22uF 20% 6.3V CERM 402 1 2
C291 0.22uF 20% 6.3V CERM 402 1 2
C352 0.22uF 20% 6.3V CERM 402 1 2
C322 0.22uF 20% 6.3V CERM 402 1 2
C392 0.22uF 20% 6.3V CERM 402 1 2
C385 0.22uF 20% 6.3V CERM 402 1 2
C376 0.22uF 20% 6.3V CERM 402 1 2

C321 0.22uF 20% 6.3V CERM 402 1 2
C318 0.22uF 20% 6.3V CERM 402 1 2
C399 0.22uF 20% 6.3V CERM 402 1 2
C410 0.22uF 20% 6.3V CERM 402 1 2
C335 0.22uF 20% 6.3V CERM 402 1 2
C369 0.22uF 20% 6.3V CERM 402 1 2
C384 0.22uF 20% 6.3V CERM 402 1 2
C294 0.22uF 20% 6.3V CERM 402 1 2
C406 0.22uF 20% 6.3V CERM 402 1 2
C405 0.22uF 20% 6.3V CERM 402 1 2

C404 0.22uF 20% 6.3V CERM 402 1 2
C400 0.22uF 20% 6.3V CERM 402 1 2
C386 0.22uF 20% 6.3V CERM 402 1 2
C289 0.22uF 20% 6.3V CERM 402 1 2
C387 0.22uF 20% 6.3V CERM 402 1 2
C401 0.22uF 20% 6.3V CERM 402 1 2
C354 0.22uF 20% 6.3V CERM 402 1 2
C389 0.22uF 20% 6.3V CERM 402 1 2
C309 0.22uF 20% 6.3V CERM 402 1 2
C398 0.22uF 20% 6.3V CERM 402 1 2

C337 0.22uF 20% 6.3V CERM 402 1 2
C290 0.22uF 20% 6.3V CERM 402 1 2
C402 0.22uF 20% 6.3V CERM 402 1 2
C397 0.22uF 20% 6.3V CERM 402 1 2
C368 0.22uF 20% 6.3V CERM 402 1 2
C334 0.22uF 20% 6.3V CERM 402 1 2
C388 0.22uF 20% 6.3V CERM 402 1 2
C293 0.22uF 20% 6.3V CERM 402 1 2
C319 0.22uF 20% 6.3V CERM 402 1 2
C336 0.22uF 20% 6.3V CERM 402 1 2

C316 0.22uF 20% 6.3V CERM 402 1 2

INTREPID CORE DECOUPLING

30 Balls
4 X 10UF (0805)
29 X 0.22UF (0402)

+1_5V_MAIN

C128 10uF 20% 6.3V CERM 805 1 2
C101 10uF 20% 6.3V CERM 805 1 2
C157 10uF 20% 6.3V CERM 805 1 2
C315 10uF 20% 6.3V CERM 805 1 2

C147 0.22uF 20% 6.3V CERM 402 1 2
C243 0.22uF 20% 6.3V CERM 402 1 2
C262 0.22uF 20% 6.3V CERM 402 1 2
C242 0.22uF 20% 6.3V CERM 402 1 2
C227 0.22uF 20% 6.3V CERM 402 1 2
C181 0.22uF 20% 6.3V CERM 402 1 2
C142 0.22uF 20% 6.3V CERM 402 1 2
C215 0.22uF 20% 6.3V CERM 402 1 2
C278 0.22uF 20% 6.3V CERM 402 1 2
C264 0.22uF 20% 6.3V CERM 402 1 2

C244 0.22uF 20% 6.3V CERM 402 1 2
C212 0.22uF 20% 6.3V CERM 402 1 2
C178 0.22uF 20% 6.3V CERM 402 1 2
C179 0.22uF 20% 6.3V CERM 402 1 2
C177 0.22uF 20% 6.3V CERM 402 1 2
C159 0.22uF 20% 6.3V CERM 402 1 2
C161 0.22uF 20% 6.3V CERM 402 1 2
C162 0.22uF 20% 6.3V CERM 402 1 2
C280 0.22uF 20% 6.3V CERM 402 1 2
C279 0.22uF 20% 6.3V CERM 402 1 2

C144 0.22uF 20% 6.3V CERM 402 1 2
C246 0.22uF 20% 6.3V CERM 402 1 2
C211 0.22uF 20% 6.3V CERM 402 1 2
C263 0.22uF 20% 6.3V CERM 402 1 2
C180 0.22uF 20% 6.3V CERM 402 1 2
C213 0.22uF 20% 6.3V CERM 402 1 2
C197 0.22uF 20% 6.3V CERM 402 1 2
C208 0.22uF 20% 6.3V CERM 402 1 2
C214 0.22uF 20% 6.3V CERM 402 1 2

INTREPID 3.3V DECOUPLING

57 Balls
4 X 10UF (0805)
72 X 0.22UF (0402)

+3V_MAIN

C164 10uF 20% 6.3V CERM 805 1 2
C395 10uF 20% 6.3V CERM 805 1 2
C10 10uF 20% 6.3V CERM 805 1 2
C9 10uF 20% 6.3V CERM 805 1 2

C375 0.22uF 20% 6.3V CERM 402 1 2
C351 0.22uF 20% 6.3V CERM 402 1 2
C53 0.22uF 20% 6.3V CERM 402 1 2
C42 0.22uF 20% 6.3V CERM 402 1 2
C21 0.22uF 20% 6.3V CERM 402 1 2
C185 0.22uF 20% 6.3V CERM 402 1 2
C31 0.22uF 20% 6.3V CERM 402 1 2
C143 0.22uF 20% 6.3V CERM 402 1 2
C123 0.22uF 20% 6.3V CERM 402 1 2
C121 0.22uF 20% 6.3V CERM 402 1 2

C33 0.22uF 20% 6.3V CERM 402 1 2
C184 0.22uF 20% 6.3V CERM 402 1 2
C43 0.22uF 20% 6.3V CERM 402 1 2
C35 0.22uF 20% 6.3V CERM 402 1 2
C261 0.22uF 20% 6.3V CERM 402 1 2
C60 0.22uF 20% 6.3V CERM 402 1 2
C52 0.22uF 20% 6.3V CERM 402 1 2
C199 0.22uF 20% 6.3V CERM 402 1 2
C57 0.22uF 20% 6.3V CERM 402 1 2
C19 0.22uF 20% 6.3V CERM 402 1 2

C16 0.22uF 20% 6.3V CERM 402 1 2
C108 0.22uF 20% 6.3V CERM 402 1 2
C55 0.22uF 20% 6.3V CERM 402 1 2
C32 0.22uF 20% 6.3V CERM 402 1 2
C125 0.22uF 20% 6.3V CERM 402 1 2
C45 0.22uF 20% 6.3V CERM 402 1 2
C76 0.22uF 20% 6.3V CERM 402 1 2
C277 0.22uF 20% 6.3V CERM 402 1 2
C28 0.22uF 20% 6.3V CERM 402 1 2
C26 0.22uF 20% 6.3V CERM 402 1 2

C34 0.22uF 20% 6.3V CERM 402 1 2
C23 0.22uF 20% 6.3V CERM 402 1 2
C120 0.22uF 20% 6.3V CERM 402 1 2
C146 0.22uF 20% 6.3V CERM 402 1 2
C141 0.22uF 20% 6.3V CERM 402 1 2
C30 0.22uF 20% 6.3V CERM 402 1 2
C145 0.22uF 20% 6.3V CERM 402 1 2
C96 0.22uF 20% 6.3V CERM 402 1 2
C54 0.22uF 20% 6.3V CERM 402 1 2
C50 0.22uF 20% 6.3V CERM 402 1 2

C75 0.22uF 20% 6.3V CERM 402 1 2
C122 0.22uF 20% 6.3V CERM 402 1 2
C51 0.22uF 20% 6.3V CERM 402 1 2
C59 0.22uF 20% 6.3V CERM 402 1 2
C163 0.22uF 20% 6.3V CERM 402 1 2
C126 0.22uF 20% 6.3V CERM 402 1 2
C98 0.22uF 20% 6.3V CERM 402 1 2
C109 0.22uF 20% 6.3V CERM 402 1 2
C56 0.22uF 20% 6.3V CERM 402 1 2
C27 0.22uF 20% 6.3V CERM 402 1 2

C296 0.22uF 20% 6.3V CERM 402 1 2
C248 0.22uF 20% 6.3V CERM 402 1 2
C210 0.22uF 20% 6.3V CERM 402 1 2
C58 0.22uF 20% 6.3V CERM 402 1 2
C22 0.22uF 20% 6.3V CERM 402 1 2
C20 0.22uF 20% 6.3V CERM 402 1 2
C61 0.22uF 20% 6.3V CERM 402 1 2
C44 0.22uF 20% 6.3V CERM 402 1 2
C29 0.22uF 20% 6.3V CERM 402 1 2
C24 0.22uF 20% 6.3V CERM 402 1 2

C183 0.22uF 20% 6.3V CERM 402 1 2
C18 0.22uF 20% 6.3V CERM 402 1 2
C49 0.22uF 20% 6.3V CERM 402 1 2
C36 0.22uF 20% 6.3V CERM 402 1 2
C17 0.22uF 20% 6.3V CERM 402 1 2
C99 0.22uF 20% 6.3V CERM 402 1 2
C396 0.22uF 20% 6.3V CERM 402 1 2
C124 0.22uF 20% 6.3V CERM 402 1 2
C127 0.22uF 20% 6.3V CERM 402 1 2
C100 0.22uF 20% 6.3V CERM 402 1 2

Intrepid Decoupling

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C

SCALE	SHT OF
NONE	16 44

PCI1510 PULL-UPS

+3V_MAIN

R757 10K 5% 1/16W MF 402 — CBUS_PCI_PERR_L 17

R756 10K 5% 1/16W MF 402 — CBUS_PCI_SERR_L 17

R753 10K 5% 1/16W MF 402 — CBUS_SUSPEND_PU 17

+3V_MAIN

C813 10UF 20% 6.3V CERM 805

C795 0.22UF 20% 6.3V CERM 402

C798 0.22UF 20% 6.3V CERM 402

C790 0.22UF 20% 6.3V CERM 402

C796 0.22UF 20% 6.3V CERM 402

C797 0.22UF 20% 6.3V CERM 402

C791 0.22UF 20% 6.3V CERM 402

R762 10K 5% 1/16W MF 402

+2_5V_MAIN

C789 0.22UF 20% 6.3V CERM 402

A7 C13 D5 E1 M1 N7 N11 — VCC

39 30 26 24 20 18 17 14 MAIN_RESET_L

THIS PROPERLY SHUTS DOWN
CARDBUS POWER FOR PSUEDO-D3COLD

R348 47 5% 1/16W MF 402

+3V_MAIN

+5V_MAIN

NO STUFF
R373 10K 5% 1/16W MF 402

MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES
TO MINIMIZE INDUCTANCE!

U19
TPS2211

NC	9	V_12 SSOI AVPP	10
	5	V_5_1	
	6	V_5_2 AVCC0	11
	3	V_3_1 AVCC1	12
	4	V_3_2 AVCC2	13
	1	VCCD0	
	2	VCCD1	
CRITICAL	15	VPPD0	
	14	VPPD1	
TPS2211_SHDN_L_PU	16	SHTDWN	
	7	GND	OC 8 NC

+VPP_CBUS_SW 17 38

+VCC_CBUS_SW 17 38

C773 0.1UF 20% 10V CERM 402

C467 0.1UF 20% 10V CERM 402

0.1UF ARE USED TO INCREASE ESD DISCHARGES OF UP TO 10KV

CRITICAL
U26
PCI1510GGU
BGA

CLAMP FOR PC-CARD
CLAMP FOR PCI

NC	H10	CLK_48_RSVD/NC	
PCI1510_VR_EN_L	D4	VR_EN*	
	L8	VR_PORT	
39 37 26 24 12 9 PCI_AD<0>	N8	AD0	
39 37 26 24 12 9 PCI_AD<1>	M7	AD1	
39 37 26 24 12 9 PCI_AD<2>	L7	AD2	
39 37 26 24 12 9 PCI_AD<3>	N6	AD3	
39 37 26 24 12 9 PCI_AD<4>	K4	AD4	
39 37 26 24 12 9 PCI_AD<5>	M6	AD5	
39 37 26 24 12 9 PCI_AD<6>	L6	AD6	
39 37 26 24 12 9 PCI_AD<7>	N5	AD7	
39 37 26 24 12 9 PCI_AD<8>	N4	AD8	
39 37 26 24 12 9 PCI_AD<9>	M2	AD9	
39 37 26 24 12 9 PCI_AD<10>	M5	AD10	
39 37 26 24 12 9 PCI_AD<11>	L4	AD11	
39 37 26 24 12 9 PCI_AD<12>	N3	AD12	
39 37 26 24 12 9 PCI_AD<13>	K5	AD13	
39 37 26 24 12 9 PCI_AD<14>	L5	AD14	
39 37 26 24 12 9 PCI_AD<15>	M4	AD15	
39 37 26 24 12 9 PCI_AD<16>	J4	AD16	
39 37 26 24 12 9 PCI_AD<17>	H1	AD17	
39 37 26 24 12 9 PCI_AD<18>	H3	AD18	
PCI_AD<19>	H2	AD19	
39 37 26 24 12 9 PCI_AD<20>	G2	AD20	
39 37 26 24 12 9 PCI_AD<21>	G4	AD21	
39 37 26 24 12 9 PCI_AD<22>	F1	AD22	
39 37 26 24 12 9 PCI_AD<23>	C3	AD23	
39 37 26 24 12 9 PCI_AD<24>	F3	AD24	
39 37 26 24 12 9 PCI_AD<25>	E2	AD25	
39 37 26 24 12 9 PCI_AD<26>	F4	AD26	
39 37 26 24 12 9 PCI_AD<27>	B1	AD27	
39 37 26 24 12 9 PCI_AD<28>	D2	AD28	
39 37 26 24 12 9 PCI_AD<29>	E4	AD29	
39 37 26 24 12 9 PCI_AD<30>	D3	AD30	
39 37 26 24 12 9 PCI_AD<31>	E3	AD31	
39 37 26 24 12 9 PCI_CBE<0>	K6	C/BE0*	
39 37 26 24 12 9 PCI_CBE<1>	M3	C/BE1*	
39 37 26 24 12 9 PCI_CBE<2>	J2	C/BE2*	
39 37 26 24 12 9 PCI_CBE<3>	A1	C/BE3*	
39 37 26 24 12 9 PCI_PAR	N1	PAR	
39 37 26 24 12 9 PCI_IRDY_L	K1	IRDY	
17 CBUS_PCI_SERR_L	L2	SERR	
CBUS_PCI_IDSEL	F2	IDSEL	
17 CBUS_PCI_PERR_L	K3	PERR	
39 37 26 24 12 PCI_FRAME_L	J1	FRAME	
39 37 26 24 12 PCI_STOP_L	L1	STOP	
39 37 26 24 12 PCI_TRDY_L	J3	TRDY	
39 37 26 24 12 PCI_DEVSEL_L	K2	DEVSEL	
CBUS_PCI_RESET_L	G3	PRST	
12 CBUS_PCI_REQ_L	C2	REQ	
12 CBUS_PCI_GNT_L	C1	GNT	
36 12 CLK33M_CBUS	G1	PCLK	
NC	M9	SPKROUT	
NC	M8	RI_OUT/PME	
17 CBUS_SUSPEND_PU	N10	SUSPEND	
14 CBUS_INT_L	K7	MFUNC0	
17 CBUS_MFUNC1_PD	N9	MFUNC1	
17 CBUS_MFUNC2_PD	L9	MFUNC2	
17 CBUS_MFUNC3_PD	K10	MFUNC3	
17 CBUS_MFUNC4_PD	M10	MFUNC4	
17 CBUS_MFUNC5_PD	N12	MFUNC5	
17 CBUS_MFUNC6_PD	L10	MFUNC6	
	L11	GRST	
	B11	VCCCB	
	L3	VCCP	
	N13	VCCD0*	CBUS_VCCD0_L
	L12	VCCD1*	CBUS_VCCD1_L
	K9	VPPD0	CBUS_VPPD0
	M11	VPPD1	CBUS_VPPD1
	L13	CD1*/CCD1*	CBUS_DET_1_L 17 39
	B5	CD2*/CCD2*	CBUS_DET_2_L 17 39
	F12	IORD*/CAD13	CBUS_IORD_L 17
	C11	IOWR*/CAD15	CBUS_IOWR_L 17
	G10	OE*/CAD11	CBUS_OE_L 17
	H13	CE1*/CC/BE0*	CBUS_CE1_L 17
	B2	VS1*/CVS1	CBUS_VS1 17
	A9	VS2*/CVS2	CBUS_VS2 17
	D13	WE*/CGNT*	CBUS_WE_L 17
	A6	RDY/IREQ*/CINT*	CBUS_READY 17
	D8	RESET/CRST*	CBUS_RESET_L 17
	A8	REG*/CC/BE3*	CBUS_REG_L 17
	C6	BVD1/CSTSCHG/STSCHG*/RI*	CBUS_BVD1_L 17
	D6	BVD2/SPKR*/CAUDIO	CBUS_BVD2_L 17
INTEGRATED PULL-UP	A5	WP/IOIS16*/CCLKRUN*	CBUS_WP_L 17
	G13	CE2/CAD10*	CBUS_CE2_L 17
	B8	INPACK/CREQ*	CBUS_INPACK_L 17
	B6	WAIT/CSERR*	CBUS_WAIT_L 17
	C7	A0/CAD26	CBUS_ADDR<0> 17
	D7	A1/CAD25	CBUS_ADDR<1> 17
	B7	A2/CAD24	CBUS_ADDR<2> 17
	D10	A3/CAD23	CBUS_ADDR<3> 17
	B12	A4/CAD22	CBUS_ADDR<4> 17
	C8	A5/CAD21	CBUS_ADDR<5> 17
	C9	A6/CAD20	CBUS_ADDR<6> 17
	A12	A7/CAD18	CBUS_ADDR<7> 17
	E11	A8/CC/BE1*	CBUS_ADDR<8> 17
	F11	A9/CAD14	CBUS_ADDR<9> 17
	G11	A10/CAD9	CBUS_ADDR<10> 17
	G12	A11/CAD12	CBUS_ADDR<11> 17
	D9	A12/CC/BE2*	CBUS_ADDR<12> 17
	E12	A13/CPAR	CBUS_ADDR<13> 17
	D12	A14/CPERR*	CBUS_ADDR<14> 17
	C10	A15/CIRDY*	CBUS_ADDR<15> 17
	B13	A16/CCLK	CBUS_ADDR_16_UF 17
	F10	A17/CAD16	CBUS_ADDR<17> 17
	E13	A18/RSVD	CBUS_ADDR<18> 17
	A13	A19/CBLOCK*	CBUS_ADDR<19> 17
	E10	A20/CSTOP*	CBUS_ADDR<20> 17
	D11	A21/CDEVSEL*	CBUS_ADDR<21> 17
	C12	A22/CTRDY*	CBUS_ADDR<22> 17
	A10	A23/CFRAME*	CBUS_ADDR<23> 17
	B10	A24/CAD17	CBUS_ADDR<24> 17
	B9	A25/CAD19	CBUS_ADDR<25> 17
	A4	D0/CAD27	CBUS_DATA<0> 17
	C4	D1/CAD29	CBUS_DATA<1> 17
	A3	D2/RSVD	CBUS_DATA<2> 17
	K11	D3/CAD0	CBUS_DATA<3> 17
	K12	D4/CAD1	CBUS_DATA<4> 17
	J13	D5/CAD3	CBUS_DATA<5> 17
	J10	D6/CAD5	CBUS_DATA<6> 17
	H12	D7/CAD7	CBUS_DATA<7> 17
	C5	D8/CAD28	CBUS_DATA<8> 17
	B4	D9/CAD30	CBUS_DATA<9> 17
	B3	D10/CAD31	CBUS_DATA<10> 17
	M12	D11/CAD2	CBUS_DATA<11> 17
	J11	D12/CAD4	CBUS_DATA<12> 17
	K13	D13/CAD6	CBUS_DATA<13> 17
	J12	D14/RSVD	CBUS_DATA<14> 17
	H11	D15/CAD8	CBUS_DATA<15> 17

R750 47 5% 1/16W MF 402 — CBUS_ADDR<16> 17

R767 22 5% 1/16W MF 402

NO STUFF
R764 47 5% 1/16W MF 402 — IO_RESET_L 30 27 26 23

R766 47 5% 1/16W MF 402 — MAIN_RESET_L 39 30 26 24 20 18 17 14

RP39 10K 5% 1/32W 25V SM

5	
10	
6	CBUS_MFUNC1_PD 17
4	CBUS_MFUNC2_PD 17
7	CBUS_MFUNC3_PD 17
3	CBUS_MFUNC4_PD 17
9	CBUS_MFUNC5_PD 17
8	CBUS_MFUNC6_PD 17
2	
1	

GND

A2 A11 D1 F13 H4 K8 M13 N2

TI REFERENCE SCHEMATIC DID NOT HAVE BULK ON +VCC_CBUS_SW

C783 2.2UF 20% 10V CERM 805

C776 2.2UF 20% 10V CERM 805

38 17 +VCC_CBUS_SW

PC CARD/CARDBUS CONNECTOR

CRITICAL
J9
QT500806-L111
M-ST-SM1

84 81

	2	1	CBUS_DATA<3> 17
39 17 CBUS_DET_1_L	4	3	CBUS_DATA<4> 17
17 CBUS_DATA<11>	6	5	CBUS_DATA<5> 17
17 CBUS_DATA<12>	8	7	CBUS_DATA<6> 17
17 CBUS_DATA<13>	10	9	
	12	11	CBUS_DATA<7> 17
17 CBUS_DATA<14>	14	13	CBUS_CE1_L 17
17 CBUS_DATA<15>	16	15	CBUS_ADDR<10> 17
17 CBUS_CE2_L	18	17	CBUS_OE_L 17
17 CBUS_VS1	20	19	
	22	21	CBUS_ADDR<11> 17
17 CBUS_IORD_L	24	23	CBUS_ADDR<9> 17
17 CBUS_IOWR_L	26	25	CBUS_ADDR<8> 17
17 CBUS_ADDR<17>	28	27	CBUS_ADDR<13> 17
17 CBUS_ADDR<18>	30	29	
	32	31	CBUS_ADDR<14> 17
17 CBUS_ADDR<19>	34	33	CBUS_WE_L 17
17 CBUS_ADDR<20>	36	35	CBUS_READY 17
17 CBUS_ADDR<21>	38	37	+VCC_CBUS_SW 17 38
38 17 +VCC_CBUS_SW	40	39	
	42	41	+VPP_CBUS_SW 17 38
38 17 +VPP_CBUS_SW	44	43	CBUS_ADDR<16> 17
17 CBUS_ADDR<22>	46	45	CBUS_ADDR<15> 17
17 CBUS_ADDR<23>	48	47	CBUS_ADDR<12> 17
17 CBUS_ADDR<24>	50	49	
	52	51	CBUS_ADDR<7> 17
17 CBUS_ADDR<25>	54	53	CBUS_ADDR<6> 17
17 CBUS_VS2	56	55	CBUS_ADDR<5> 17
17 CBUS_RESET_L	58	57	CBUS_ADDR<4> 17
17 CBUS_WAIT_L	60	59	
	62	61	CBUS_ADDR<3> 17
17 CBUS_INPACK_L	64	63	CBUS_ADDR<2> 17
17 CBUS_REG_L	66	65	CBUS_ADDR<1> 17
17 CBUS_BVD2_L	68	67	CBUS_ADDR<0> 17
17 CBUS_BVD1_L	70	69	
	72	71	CBUS_DATA<0> 17
17 CBUS_DATA<8>	74	73	CBUS_DATA<1> 17
17 CBUS_DATA<9>	76	75	CBUS_DATA<2> 17
17 CBUS_DATA<10>	78	77	CBUS_WP_L 17
39 17 CBUS_DET_2_L	80	79	

83 82

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6582 | REV. C

SCALE NONE | SHT 17 OF 44

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0168	1	IC,ATI,M10,NO HEATSPREADER	U44	CRITICAL	?

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0336	338S0168	?	U44	ALT FOR 338S0168 EOL

OMIT
CRITICAL

U44
RAGE_MOBILITY
M10-CSP64
64MB
BGA
(1 OF 6)

AD31 AD30 AD29 AD28 AD27 AD26 AD25 AD24 AD23 AD22 AD21 AD20 AD19 AD18 AD17 AD16 AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0

CBEB3 CBEB2 CBEB1 CBEB0 PCICLK FRAMEB IRDYB TRDYB STOPB DEVSELB PAR REQB GNTB INTAB RSTB WBF VREFG VREF

AD_STB0 AD_STB1 AD_STBB0 AD_STBB1 AGP_BUSYB AGPREF AGPTEST AGP8X_DETB SUS_STAT ST0 ST1 ST2 SBA7 SBA6 SBA5 SBA4 SBA3 SBA2 SBA1 SBA0 RBFB STP_AGPB SB_STB SB_STBS RSTB_MSK DBI_LO DBI_HI TEST_YCLK TEST_MLCK MEMTEST PLLTEST MEMVMODE0 MEMVMODE1 D+ D- GPU_THERM_DP GPU_THERM_DM

VSS

R119 47 5% 1/16W MF 402
R127 10K 5% 1/16W MF 402
R159 20K 5% 1/16W MF 402
R172 20K 5% 1/16W MF 402
R158 0 5% 1/16W MF 402
R126 47K 5% 1/16W MF 402
R138 47K 5% 1/16W MF 402
R118 45.3 1% 1/16W MF 402

C62 0.1uF 20% 10V CERM 402
C63 0.01uF 20% 16V CERM 402
(PLACE C1002 CLOSE TO AGPREF PIN)

+3V_GPU
+1_5V_AGP
INT_AGP_VREF

OMIT

U44
RAGE_MOBILITY
M10-CSP64
64MB
BGA
(6 OF 6)

VSS VDDCI

L2
60-OHM-EMI
SM
GPU_VCORE
+GPU_VCORE_VDDCI

C64 0.01uF 20% 16V CERM 402
C67 10uF 20% 6.3V CERM 805
C65 0.01uF 20% 16V CERM 402
C68 0.01uF 20% 16V CERM 402
C66 0.01uF 20% 16V CERM 402
C69 0.01uF 20% 16V CERM 402

MAIN_RESET_L IS TOGGLED FOR SLEEP
MAIN_RESET_L
R54 10K 5% 1/16W MF 402
R53 47 5% 1/16W MF 402

R43 1K 1% 1/16W MF 402
R44 1K 1% 1/16W MF 402
+GPU_MEM
R45 1K 1% 1/16W MF 402
R46 1K 1% 1/16W MF 402
C11 0.1uF 20% 10V CERM 402
C37 10uF 20% 6.3V CERM 805
PLACE VERF VOLTAGE DIVIDER CLOSE TO ATI M10 VREF PIN

+1_8V_GPU
ATI_MEMIO_LO R55 4.7K 5% 1/16W MF 402
ATI_MEMIO_HI R104 4.7K 5% 1/16W MF 402
ATI_MEMIO_HI R70 4.7K 5% 1/16W MF 402
ATI_MEMIO_LO R105 4.7K 5% 1/16W MF 402
ATI_MEMVMODE0
ATI_MEMVMODE1

FOR 2.5 VDDR1
MEMVMODE0=1.8V
MEMVMODE1=GND
FOR 1.8 VDDR1
MEMVMODE0=GND
MEMVMODE1=1.8V

(PULL-UP to GPU_MEM_IO)
ATI_MEMTEST
+GPU_MEM

U44
RAGE_MOBILITY
M10-CSP64
64MB
BGA
(2 OF 6)

VSS VSS VSS VSS

OMIT

27M OSC

(PLACE THE OSCILLATOR AND R189 AND R195
CLOSE TO ATI PIN AJ29)

+3V_SLEEP
L4
FERR-EMI-100-OHM
SM
+3V_ATI_OSC_SLEEP
C77 0.1uF 20% 10V CERM 402
C78 4.7uF 20% 6.3V CERM 805
NO STUFF
R188 100K 5% 1/16W MF 402
CRITICAL
VCC
G2
27.0000M
OSC SM-1
OE
OUT
GND
ATI_OSC_OE
ATI_CLK27M_OSC
ATI_CLK27M_OSC_SS
(PLACE R200 CLOSE TO OSC)
GPU_SS
R200 0 1% 1/16W MF 402
R189 287 1% 1/16W MF 402
R195 162 1% 1/16W MF 402
ATI_CLK27M_IN

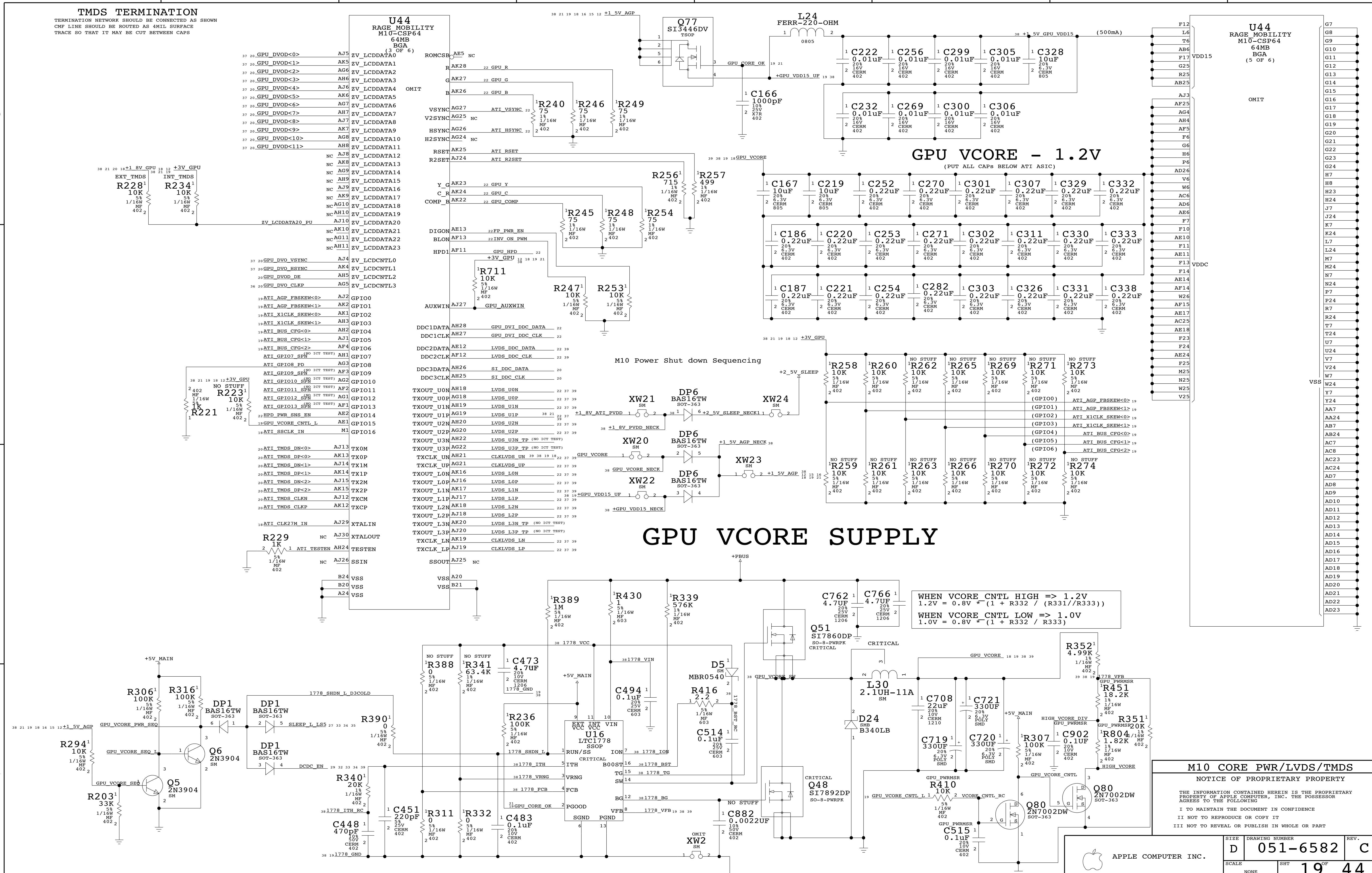
S0=1;S1=M => -1.5% DOWN-SPREAD
SPREAD SPECTRUM SUPPORT

+3V_SLEEP
GPU_SS
L3
FERR-EMI-100-OHM
SM
+3V_ATI_SS
GPU_SS C70 10uF 20% 6.3V CERM 805
GPU_SS C71 0.1uF 20% 10V CERM 402
NO STUFF
R173 0 5% 1/16W MF 402
GPU_SS
R181 0 5% 1/16W MF 402
CRITICAL
VDD
U47
CY25811
SOI
XIN/CLKIN
XOUT
SSCLK
FRSEL
S1
S0
VSS
ATI_CLK27M_OSC_SS
ATI_SSCLK_UF
ATI_SSCLK_IN
CY25811_S1
CY25811_S0
GPU_SS
R201 33 5% 1/16W MF 402
NO STUFF
R37 0 5% 1/16W MF 402
NO STUFF
R38 0 5% 1/16W MF 402

M10 AGP INTERFACE

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 18 OF 44	



M10 CORE PWR/LVDS/TMDS

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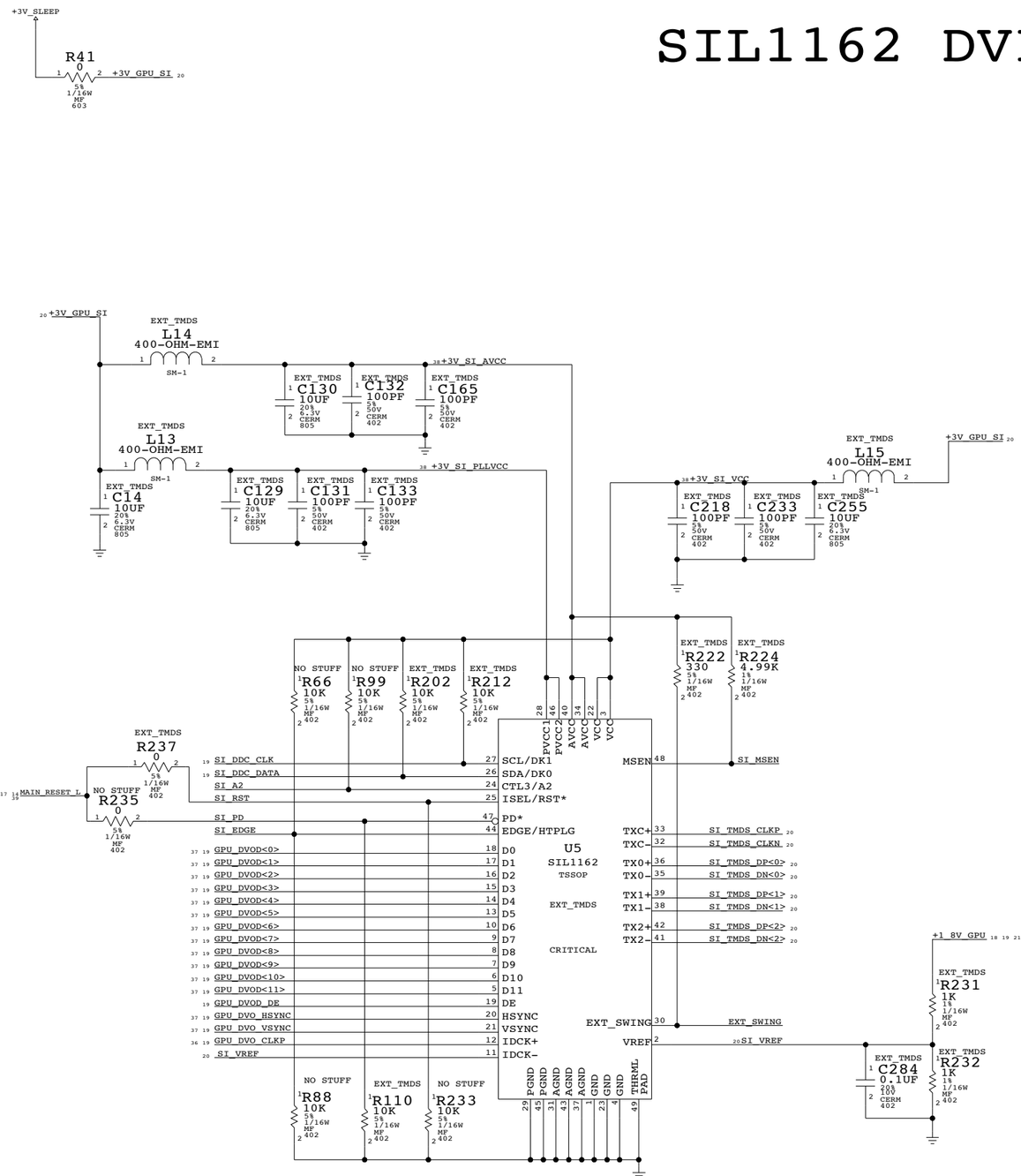
APPLE COMPUTER INC.

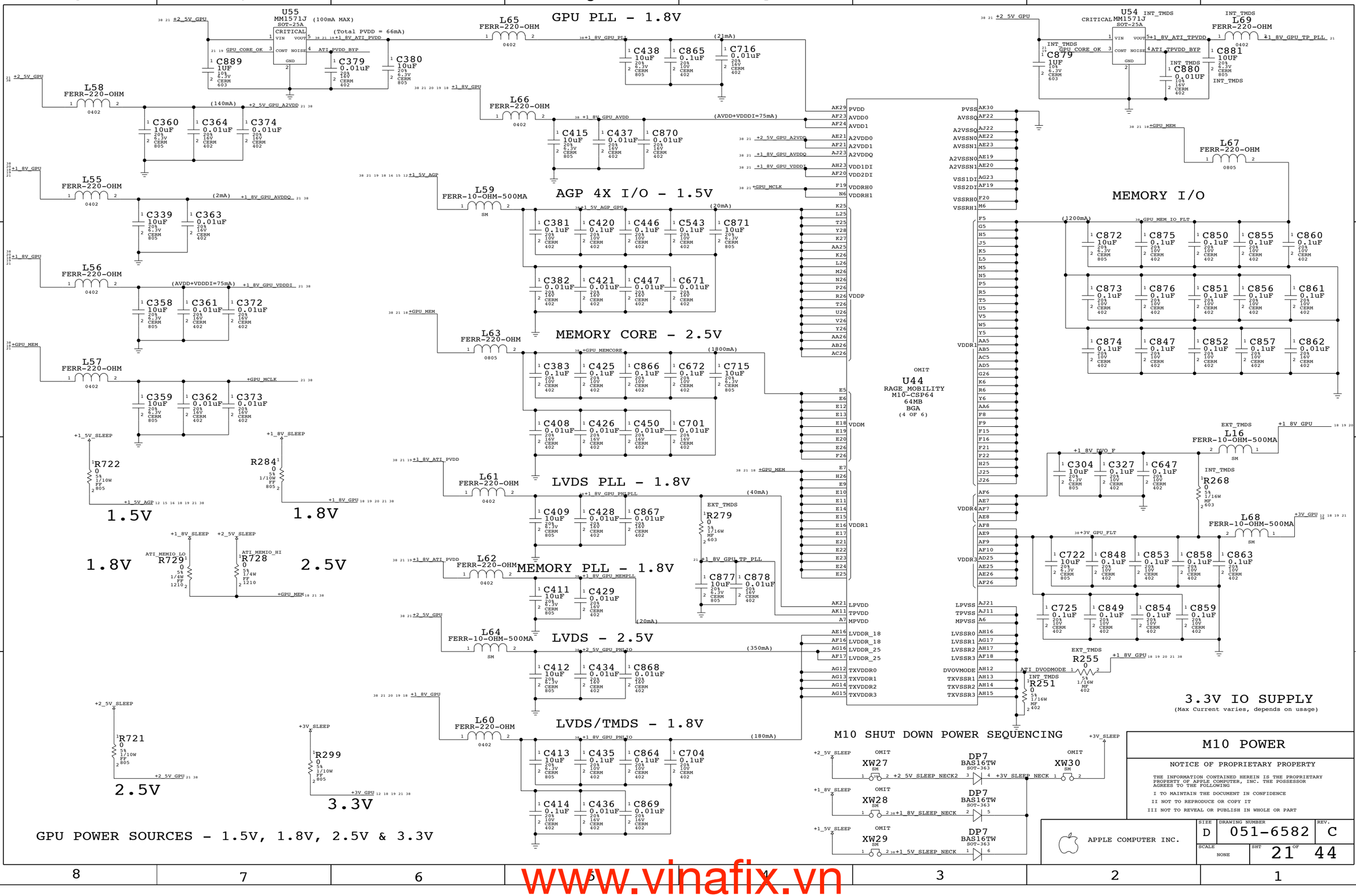
SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE NONE	SHT 19 OF 44	

SIL1162 DVI TRANSMITTER



APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 20 OF 44	



EXTERNAL VIDEO (DVI) INTERFACE

ANALOG FILTERING PLACE CLOSE TO CONNECTOR

FL2 CRITICAL LCFILTER SM-220MHZ
FL1 CRITICAL LCFILTER SM-220MHZ
FL3 CRITICAL LCFILTER SM-220MHZ
GPU_B, GPU_G, GPU_R → VGA_B, VGA_G, VGA_R
C685 3.3PF, C676 3.3PF, C684 3.3PF (0.25% 50V CERM 402)

VGA VSYNC BUFFERS

+3V_MAIN
U56 CRITICAL 74AHC1G32 SM
U57 CRITICAL 74AHC1G32 SM
ATI_HSYNC → R718 33 (5% 1/16W MF 402) → VGA_HSYNC
ATI_VSYNC → R714 33 (5% 1/16W MF 402) → VGA_VSYNC

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)

+5V_SLEEP → F1 0.5AMP-13.2V SM → +5V_DDC_SLEEP_UF → L23 400-OHM-EMI SM-1 → +5V_DDC_SLEEP
Isolation required for DVI power switch

D21 SM MBR0530
DDC_CLK_ISO
R661 4.7K, R655 4.7K (5% 1/16W MF 402)
R670 100, R649 100, R650 100 (5% 1/16W MF 402)
C706 100pF, C669 100pF, C1 100pF (5% 50V CERM 402)
C710 0.01UF (20% 50V CERM 603)
R706 0 (5% 1/16W MF 402) PLACE NEAR 3, 11 & 19
R1 0 (5% 1/16W MF 402) PLACE NEAR C5A & C5B
CHGND1, CHGND5

J14 CRITICAL QH1112 F-RT-TH
TMDS_CONN_DN<0>, DP<0>, DN<1>, DP<1>, DN<2>, DP<2>
TMDS_CONN_CLKP, TMDS_CONN_CLKN
VGA_B, VGA_G, VGA_R, VGA_HSYNC, VGA_VSYNC
DVI_DDC_CLK_UF, DVI_DDC_DATA_UF, DVI_HPD_UF, (+5V_DDC_SLEEP)

NOTE: Pulldown for DVI_HPD provided by DVI power switch interface
NOTE: DVI_HPD SHARES Q68 WITH ALS BECAUSE OF BOARD REAL ESTATE

3V LEVEL SHIFTERS

+3V_SLEEP
Q38 2N7002DW SOT-363 (DVI_DDC_CLK → GPU_DVI_DDC_CLK)
Q38 2N7002DW SOT-363 (DVI_DDC_DATA → GPU_DVI_DDC_DATA)
Q35 2N7002DW SOT-363 (DVI_HPD → GPU_HPD)
R662 10K, R671 10K, R694 100K (5% 1/16W MF 402)

Power key detect path when system is shutdown or asleep.. DDC_CLK is isolated from NV17M DURING SHUTDOWN. WHEN power key on remote device is pressed, 5V will be driven into DDC_CLK. Since host rails will be low, TP0610 will turn on, driving SOFT_PWR_ON_L low. As host rails rise, TP0610 will turn off, as will remote device path into DDC CLK. Isolation will be disabled as well.

DVI POWER SWITCH

Q40 TP0610 SM
R690 680 (5% 1/16W MF 402)
R691 10K (5% 1/16W MF 402)
Q42 2N3904 SM
R688 330 (5% 1/16W MF 402) Pulldown prevents 3904 from turning on when DVI monitor has active, self-powered DDC clock pullup.
DVI_TURN_ON_BASE, DVI_TURN_ON, DVI_TRUN_ON_ILIM, SOFT_PWR_ON_L

Power key detect path when system is running. HPD normally driven to 3.3V. When power key on remote device pressed, HPD will be driven to 5V. COMPARATOR ENABLED BY NV17MAP GPIO.

+3V_SLEEP
R680 68.1K, C696 0.1UF (20% 10V CERM 402)
HPD_4V_REF
U46 LMC7211 SM CRITICAL
R663 10K (1% 1/16W MF 402) ← DVI_HPD_UF, DVI_HPD_DIV
R686 10K, R681 100K (1% 1/16W MF 402)
HPD_PWR_SW, HPD_ON
Q41 2N7002DW SOT-363
R703 330 (5% 1/16W MF 402)
+PBUS
Q45 TP0610 SM
COMP_ENABLE, COMP_DISABLE
R696 100K, R704 100K (5% 1/16W MF 402)
HPD_ON_RC
R700 20K (5% 1/16W MF 402)
HPD_BASE
Q44 2N3904 SM
C703 47UF (20% 6.3V CERM 1210)
R705 68K (5% 1/16W MF 402)
NEED PULL-DOWN BECAUSE THIS SIGNAL IS TRISTATED INITIALLY
HPD_PWR_SNS_EN
Q41 2N7002DW SOT-363
R213 100K (5% 1/16W MF 402)

LCD INTERFACE

LVDS INTERFACE

100K pull-ups are for no-panel case (development) Panel has 2K pull-ups

C416 0.001uF (20% 50V CERM 402) CHGND4
CRITICAL J6 G-501973 F-RT-SM
+3V_SLEEP
R342 100K, R320 100K (5% 1/16W MF 402)
+3V_LCD (LVDS DDC POWER)
LVDS_DDC_CLK, LVDS_DDC_DATA
NO STUFF
C449 0.001uF, C452 0.001uF (20% 50V CERM 402) CHGND4
LVDS_L0N, L0P, L1N, L1P, L2N, L2P, CLKLVDS_LN, LP, LVDS_U0N, U0P, U1N, U1P, U2N, U2P, CLKLVDS_UN, UP
C500 0.001uF (20% 50V CERM 402) CHGND4

LCD POWER SWITCHES

+3V_MAIN
R400 100K (5% 1/16W MF 402)
C484 2200pF (5% 50V CERM 603)
+3V_LCD_SW
L6 FERR-250-OHM SM
R391 100K (5% 1/16W MF 402) LCD_PWREN_L
C474 0.001uF (20% 50V CERM 402) CHGND4
LCD_DIGON_L
Q11 TSOP SI3443DV
Q8 2N7002 SM
FP_PWR_EN

INVERTER INTERFACE

+PBUS
L33 FERR-1K-OHM-EMI SM +12_8V_INV
+5V_MAIN
Q7 FDG6324L SC70-6
+5V_INV_UF_SW
L32 400-OHM-EMI SM-1
R317 100K (5% 1/16W MF 402)
C440 10UF (20% 6.3V CERM 805)
FP_PWR_EN_L
Q7 FDG6324L SC70-6
FP_PWR_EN
+5V_INV_SW
C746 0.001UF (20% 50V CERM 402)
CRITICAL J7 SM-2MT
C749 0.001UF (20% 50V CERM 402)
L31 400-OHM-EMI SM-1 BRIGHT_PWM
C739 0.001UF (20% 50V CERM 402)
CHGND2
+3V_PMU
C552 0.1UF (20% 10V CERM 402)
INV_ON_PWM
U24 74LVC32 TSSOP
BRIGHT_PWM_UF
INVERTER EXPECTS ACTIVE HIGH SIGNAL
SHARES LOGIC WITH KB RESET SIGNALS (PG 28)
R724 0 (5% 1/16W MF 402)
C744 0.01uF (20% 50V CERM 603) CHGND2

TMDS FILTERING PLACE CLOSE TO CONNECTOR

CRITICAL L72 90-OHM-300MA 2012H
TMDS_DN<0>, TMDS_DP<0> → TMDS_CONN_DN<0>, TMDS_CONN_DP<0>
CRITICAL L21 165-OHM SM
TMDS_CLKP → TMDS_CONN_CLKP
TMDS_CLKN → TMDS_CONN_CLKN
CRITICAL L73 90-OHM-300MA 2012H
TMDS_DN<1>, TMDS_DP<1> → TMDS_CONN_DN<1>, TMDS_CONN_DP<1>
L74 90-OHM-300MA 2012H
TMDS_DN<2>, TMDS_DP<2> → TMDS_CONN_DN<2>, TMDS_CONN_DP<2>

S-VIDEO/COMP OUT INTERFACE

Place GND shorts at graphics controller

XW12 SM GPU_TV_GND1
L26 FERR-10-OHM-500MA SM → TV_GND1
L25 3.3UH 0603 GPU_Y → TV_C
L29 3.3UH 0603 GPU_C → TV_Y
L27 3.3UH 0603 GPU_COMP → TV_COMP
C712 0.01UF, C702 560PF, C707 560PF, C718 560PF, C724 560PF, C714 560PF, C713 560PF (10% 50V CERM 402)
CRITICAL J15 MINIDIN RT-TH MH1177
XW13 SM GPU_TV_GND2
L28 FERR-10-OHM-500MA SM → TV_GND2
C717 0.01UF (20% 50V CERM 603)
CHGND1

Place GND shorts at graphics controller

VIDEO CONNECTORS

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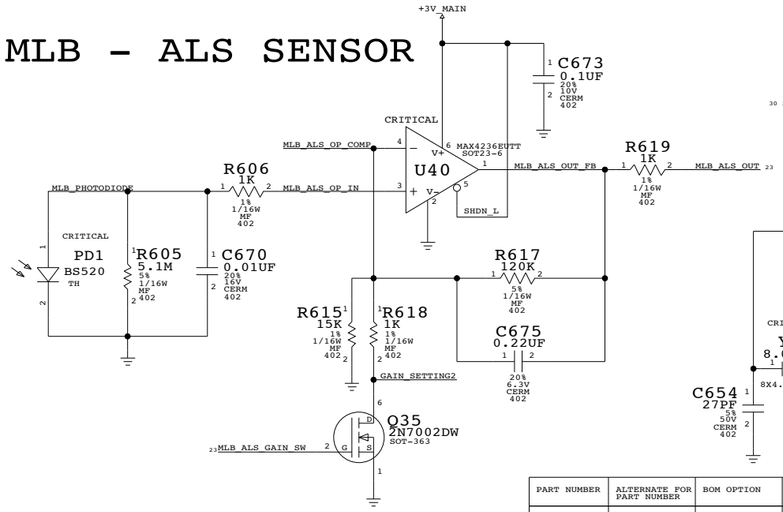
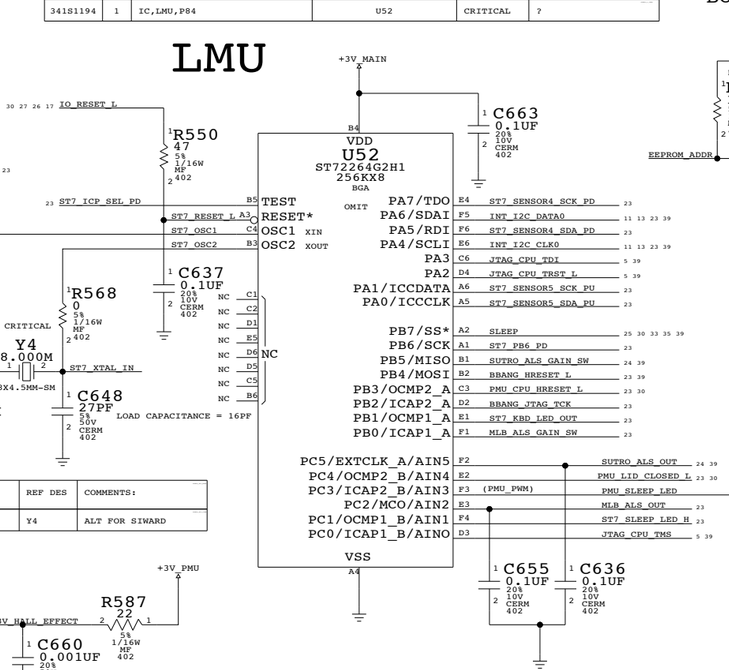
MLB - ALS SENSOR



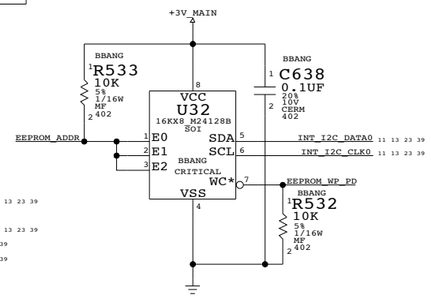
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1194	1	IC,LMU,P84	U52	CRITICAL	?

LMU

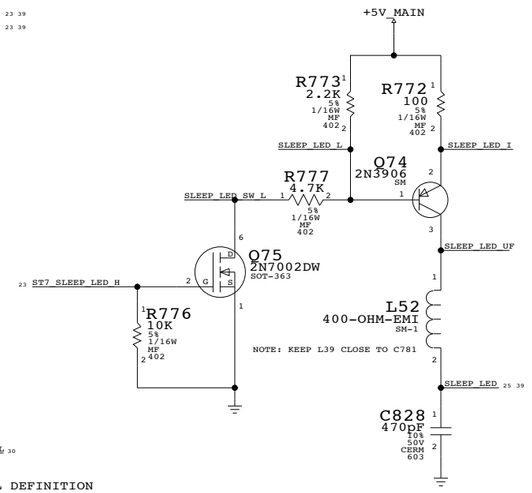


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0008	197S0040		Y4	ALT FOR SIWARD

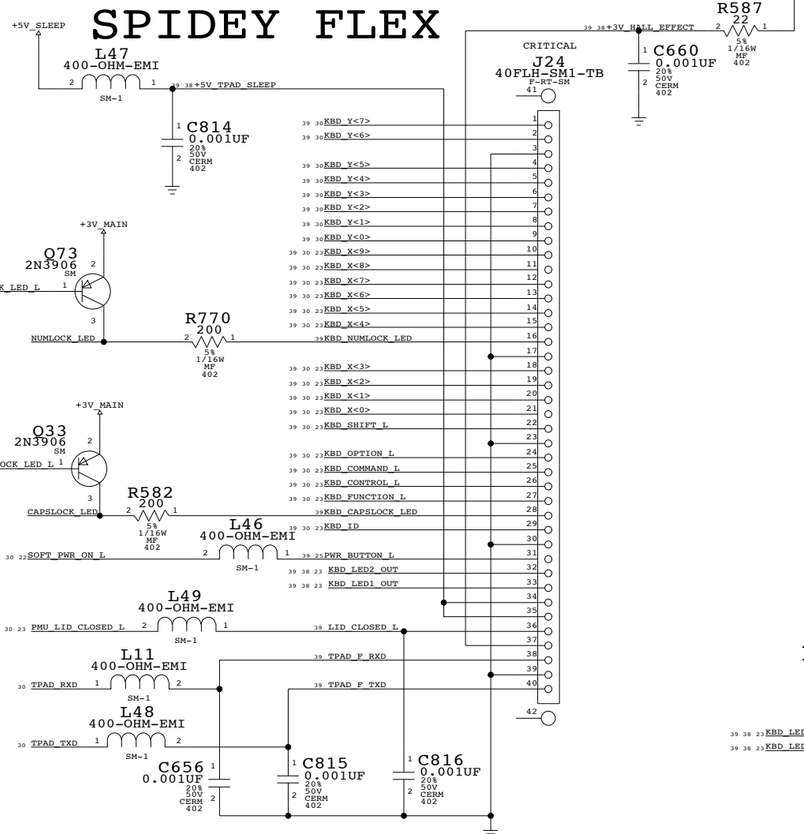
BOOT BANGER E2PROM



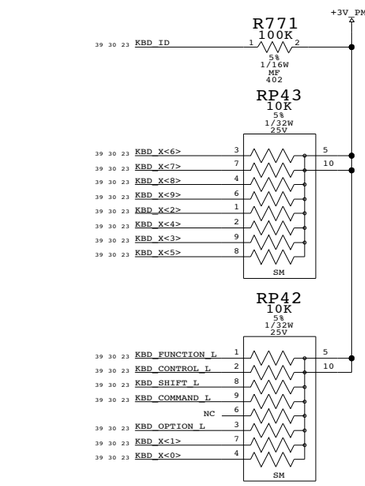
SLEEP LED



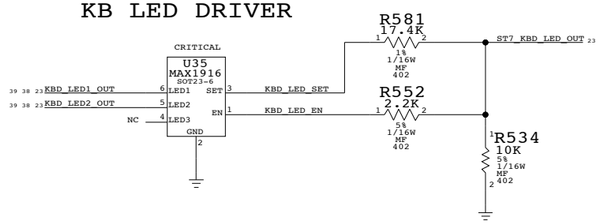
SPIDEY FLEX



KEYBOARD PULLUPS

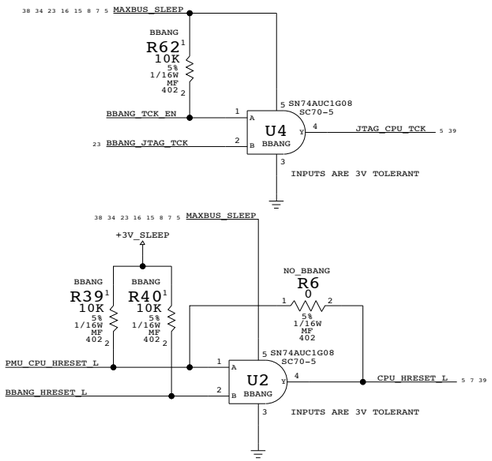


KB LED DRIVER

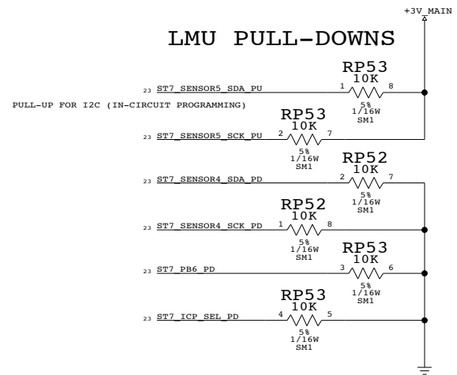


BOOT BANGING SIGNAL DEFINITION

1/ BBANG_HRESET_L (OPEN COLLECTOR OUTPUT - 10K PULLUP ON MLB)
2/ PMU_HRESET_L (3V INPUT INTO LMU)
3/ BBANG_JTAG_TCK (REGULAR OUTPUT)
4/ JTAG_CPU_TMS (OPEN COLLECTOR OUTPUT - 4700HM PULLUP ON MLB)
5/ JTAG_CPU_TDI (OPEN COLLECTOR OUTPUT - 4700HM PULLUP ON MLB)
6/ JTAG_CPU_TRST_L (OPEN COLLECTOR OUTPUT - 4700HM PULLUP ON MLB)



LMU PULL-DOWNS



LMU/BOOTBANGER/SPIDEY

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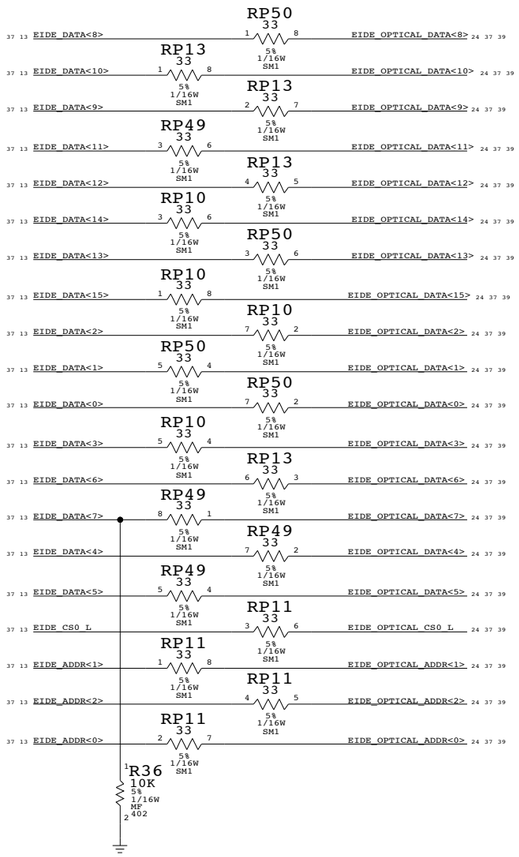
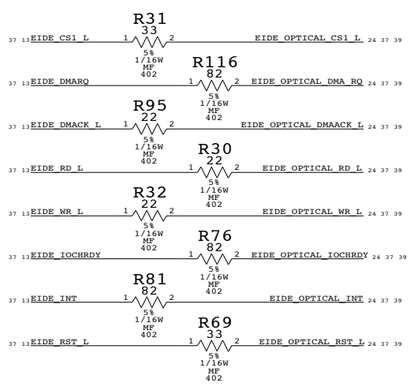
HARD DRIVE INTERFACE (UATA100)

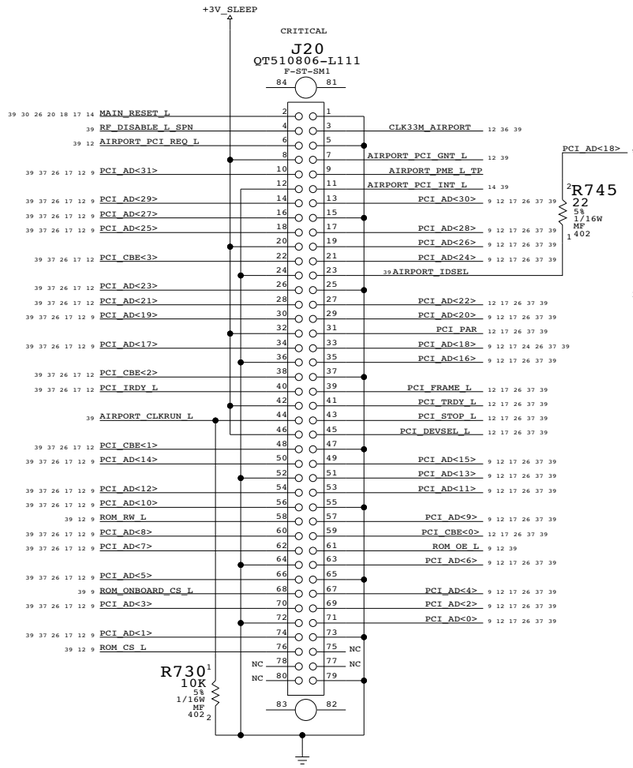
EIDE SERIES TERMINATION

PLACE TERMINATORS NEAR INTREPID

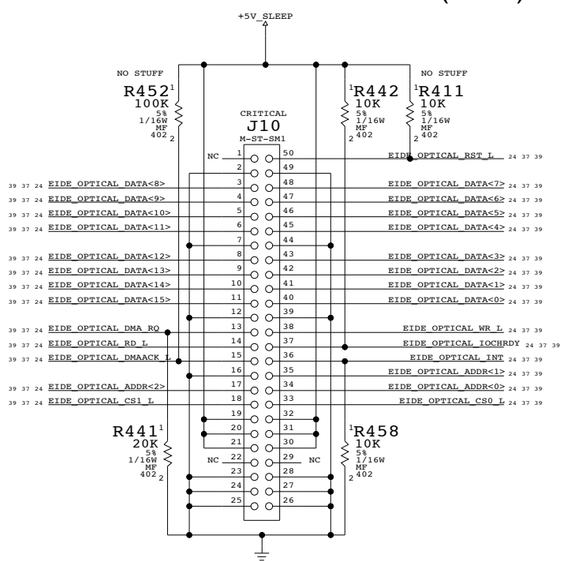




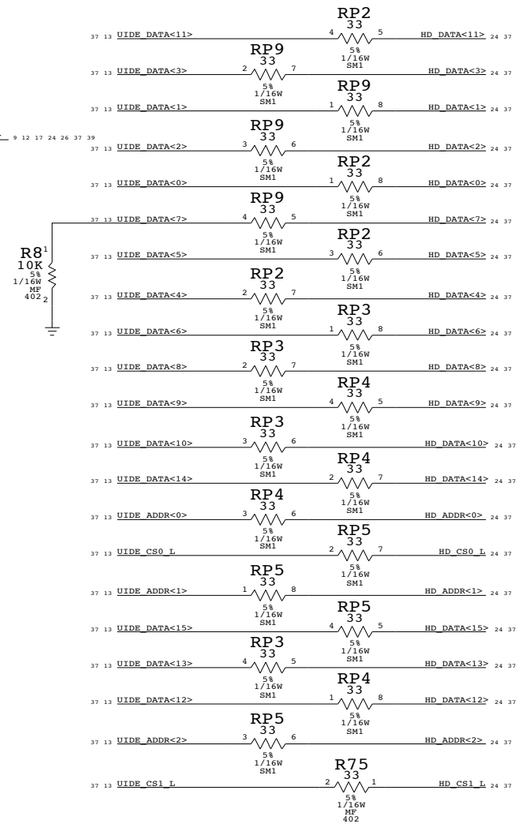
WIRELESS INTERFACE



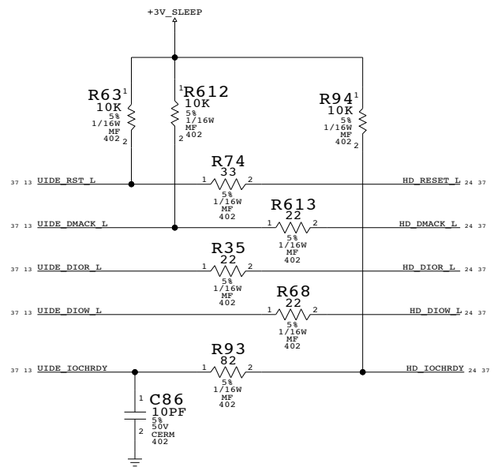
OPTICAL DRIVE INTERFACE (EIDE)



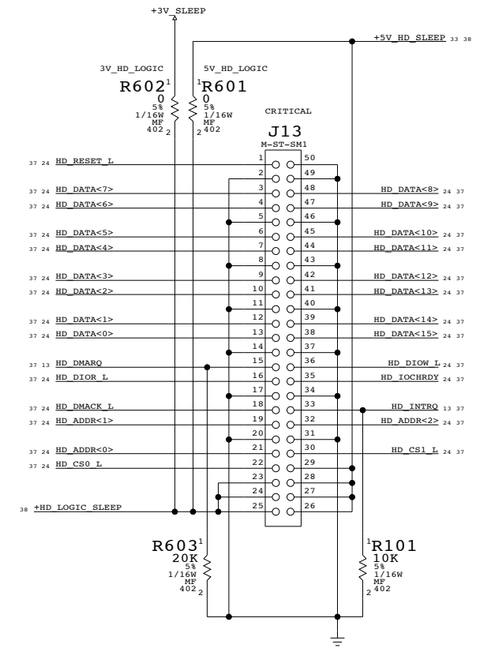
PLACE SERIES R CLOSE TO INTERPID



PLACE PULLUP RESISTORS CLOSE TO INTREPID

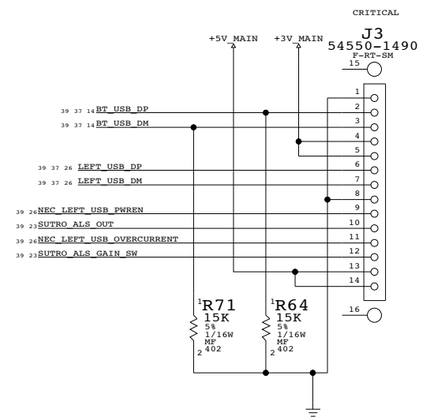


IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V



ANY SEQUENCING REQUIREMENT BETWEEN +5V_HD_SLEEP AND +3V_SLEEP?

BLUETOOTH/LEFT-SIDE USB



INTERNAL I/O CONNECTORS

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SOUND BOARD (SOUSAPHONE)

AUDIO - SNAPPER
SND - INTREPID

L77 FERR-220-OHM 0402
L80 FERR-220-OHM 0402
L81 FERR-220-OHM 0402
L82 FERR-220-OHM 0402
L76 FERR-220-OHM 0402
L78 FERR-220-OHM 0402
L79 FERR-220-OHM 0402

SND_SYNC → SND_SYNC_F
SND_CLKOUT → SND_CLKOUT_F
INT_AUDIO_TO_SND → INT_AUDIO_TO_SND_F
SND_TO_AUDIO → SND_TO_AUDIO_F
SND_AMP_MUTE → SND_AMP_MUTE_F
SND_HW_RESET_L → SND_HW_RESET_L_F
SND_SCLK → SND_SCLK_F

C895 0.01UF 20% 16V CERM 402 NO STUFF
C899 0.01UF 20% 16V CERM 402 NO STUFF
C896 0.01UF 20% 16V CERM 402 NO STUFF
C897 0.01UF 20% 16V CERM 402 NO STUFF
C898 0.01UF 20% 16V CERM 402 NO STUFF
C900 0.01UF 20% 16V CERM 402 NO STUFF
C901 0.01UF 20% 16V CERM 402 NO STUFF

+3V_MAIN
+5V_MAIN

CRITICAL
J12
QT510306-L111
F-ST-SM1

INT_AUDIO_TO_SND_F
INT_I2C_CLK2
SND_SCLK_F
SND_CLKOUT_F
SND_SYNC_F
INT_I2C_DATA2
SLEEP_LED
SND_TO_AUDIO_F
SND_HP_SENSE_L
SND_LIN_SENSE_L
SND_AMP_MUTE_F
SLEEP
SND_HW_RESET_L_F
SND_HP_MUTE_INV

XW9 SM SND_AGND

+5V_MAIN
RP44 100K 5% 1/16W SM1
SND_AMP_MUTE
Q26 2N7002DW SOT-363
SND_AMP_MUTE_L
AMP_CONTROL
RP44 100K 5% 1/16W SM1
Q26 2N7002DW SOT-363
INT_PU_RESET_L

+3V_MAIN
RP44 100K 5% 1/16W SM1
R689 100K 5% 1/16W MF 402
SND_HP_MUTE_INV
Q31 2N7002DW SOT-363
SND_HP_MUTE
Q31 2N7002DW SOT-363
SND_HP_MUTE_L
AMP_CONTROL
RP44 100K 5% 1/16W SM1

PLACE XW9 CLOSE TO 5V SWITCHER (U27)
PLACE CAPS AS CLOSE TO THERMISTORS AS POSSIBLE
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY

CAPS FOR EMI EXPERIMENTATION ONLY

FAN INTERFACE

MAIN1
SUPPLY_M_DP
C681 0.0001UF 20% 50V CERM 402
Q66 2N3904 SM
SUPPLY_M_DM

PLACE CLOSE TO CPU
MAIN2
CPU_M_DP
C668 0.001UF 20% 50V CERM 402
Q39 2N3904 SM
CPU_M_DM

PLACE UNDERNEATH UPPER RAM
ALTERNATE1
THERM1_A_DP
C678 0.001UF 20% 50V CERM 402 NO STUFF
Q47 2N3904 SM NO STUFF
THERM1_A_DM

PLACE CLOSE TO BATTERY CHARGER/VCORE
ALTERNATE2
THERM2_A_DP
C651 0.001UF 20% 50V CERM 402 NO STUFF
Q62 2N3904 SM NO STUFF
THERM2_A_DM

KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

CPU_M_DP → R719 0 5% 1/16W MF 402 → THERM1_DP
CPU_M_DM → R725 0 5% 1/16W MF 402 → THERM1_DM
SUPPLY_M_DP → R713 0 5% 1/16W MF 402 → THERM2_DP
SUPPLY_M_DM → R716 0 5% 1/16W MF 402 → THERM2_DM

KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

THERM1_A_DP → R723 0 5% 1/16W MF 402 NO STUFF → THERM1_DP
THERM1_A_DM → R726 0 5% 1/16W MF 402 NO STUFF → THERM1_DM
THERM2_A_DP → R710 0 5% 1/16W MF 402 NO STUFF → THERM2_DP
THERM2_A_DM → R717 0 5% 1/16W MF 402 NO STUFF → THERM2_DM

MODEM

SUPPORTS BOTH THE LAST DASH AND Q52 SOFT MODEM

+5V_MAIN
C767 10UF 20% 6.3V CERM 805 NO STUFF
C513 0.1UF 20% 10V CERM 402
R405 10K 5% 1/16W MF 402
+3V_MAIN
C478 0.1UF 20% 10V CERM 402 NO STUFF
C469 10UF 20% 6.3V CERM 805

CRITICAL
J8
QT51066-L010
F-ST-SM1

MOD_DTO
MOD_CLKOUT
COMM_RESET_L
COMM_SHUTDOWN
INT_I2C_CLK2
INT_I2C_DATA2
MOD_SYNC
INT_MOD_DTI
MOD_BITCLK
MODEM_USB_DM
MODEM_USB_DP
COMM_RING_DET_L

FAN CONTROLLER

+3V_MAIN
R814 10 5% 1/16W MF 402
ADT7460_VCC
C904 1UF 20% 10V CERM 603
C711 0.1UF 20% 10V CERM 402

VCC
U3
+2.5V/QSOP SMBALERT# SDA SCL
ADT7460
CRITICAL
D1+ D1- D2+ D2-
ADR ENABLE# TACH3 TACH4/ADR SELECT/THERM#
GND
PWM1/XTO TACH1 PWM2/SMBALERT# TACH2 PWM3/TACH3 NC

ADT7460_VCORE_MON
INT_I2C_DATA1
INT_I2C_CLK1
THERM1_DP
THERM1_DM
THERM2_DP
THERM2_DM
ADT7460_FAN1_PWM
FANL_TACH
ADT7460_FAN2_PWM
FANR_TACH
ADT7460_ADR_EN_L
ADT7460_THERM

C688 0.001UF 20% 50V CERM 402 NO STUFF
C690 0.001UF 20% 50V CERM 402 NO STUFF
C846 0.001UF 20% 50V CERM 402 NO STUFF
C905 0.001UF 20% 50V CERM 402 NO STUFF

R42 10K 5% 1/16W MF 402
+5V_SLEEP
R692 10K 5% 1/16W MF 402
R695 10K 5% 1/16W MF 402
Q78 2N7002DW SOT-363
Q78 2N7002DW SOT-363

THERM ISOLATION

+3V_MAIN
R811 100K 5% 1/16W MF 402
+3V_PMU_AVCC
R812 100K 5% 1/16W MF 402
THERM_L_OC
R813 100K 5% 1/16W MF 402
THERM_INV
Q87 2N7002DW SOT-363
Q87 2N7002DW SOT-363
C903 0.1UF 20% 10V CERM 402
ADT7460_THERM

LEFT FAN (CPU)

+5V_SLEEP
R679 10K 5% 1/16W MF 402
FANL_TACH
FANL_GND
Q37 SI3446DV TSOP
CRITICAL
J4
SM-2MT
PLACE CLOSE TO CONNECTOR
C134 4.7UF 20% 10V CERM 1206
FANL_PWM

SERIAL DEBUG INTERFACE

+5V_MAIN
SERIAL_DEBUG
CRITICAL
J16
M-ST-5087
SM
COMM_TXD_L
COMM_TRXC
COMM_GPIO_L
COMM_DTR_L
COMM_RTS_L
COMM_RXD

DEBUG POWER BUTTON

NO STUFF
R527 0 5% 1/16W MF 603
PWR_BUTTON_L

DEBUG JUMPERS

+5V_SLEEP
R293 10K 5% 1/16W MF 402
R295 10K 5% 1/16W MF 402
FANL_PWM
FANR_PWM
Q78 2N7002DW SOT-363
Q78 2N7002DW SOT-363

NO STUFF
R537 0 5% 1/16W MF 603
PMU_NMI_BUTTON_L
NO STUFF
R553 0 5% 1/16W MF 603
PMU_RESET_BUTTON_L

RIGHT FAN (GPU)

+5V_SLEEP
R623 10K 5% 1/16W MF 402
CRITICAL
J2
SM-2MT
FANR_GND
FANR_TACH
Q36 SI3446DV TSOP
PLACE CLOSE TO CONNECTOR
C135 4.7UF 20% 10V CERM 1206
FANR_PWM

FAN/MODEM/SOUND/SLEEP LED/DEBUG

APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-6582 | REV. C
SCALE NONE | SHT 25 OF 44

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0608	197S0038	NEC_USB	Y5	ALT FOR SIWARD

Y7 LOAD CAPACITANCE IS 16PF

SERR_L AND PERR_L
HAS DEDICATED PULL-UP
FOR BOTH CBUS AND USB2

Series Rpaks required to facilitate NAND-tree testing

Low/Full/High Speed (External)

Low/Full/High Speed (External)

INTREPID USB CONSTRAINTS

NEED PULL-UP RESISTORS IN CASE USB 1.0 IS USED FOR PORT POWER

PLACE NEAR J3

SUTRO CONNECTOR

PLACE NEAR J12

BUBBA CONNECTOR

USB 2.0

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 26 OF 44	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0223	338S0079	7	U49	ALT FOR B1

Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

+3V_MAIN

C442 10uF 20% 6.3V CERM 805

NO STUFF R333 0 5% 1/16W MF 402

3405_MODE

R319 0 5% 1/16W MF 402

U14 LTC3405 SOT23-6 — VIN, RUN, MODE, GND, SW, VFB

LTC3405_SW

CRITICAL L5 3.3uH SM1

+1.0V_MARVELL

R334 665K 1% 1/16W MF 402 R2A

C471 22pF 5% 50V CERM 402

R361 49.9K 1% 1/16W MF 402 R2B

C486 10uF 20% 6.3V CERM 805

3405_VFB

R362 182K 1% 1/16W MF 402 R1

VOUT = 0.8V*(1+R2EQV/R1)

R2EQV = R2A||R2B

PLACE ALL SERIES RES CLOSE TO PHY

R370 0 5% 1/16W MF 402 — CLKENET_LINK_TX / CLKENET_PHY_TX

R353 0 5% 1/16W MF 402 — CLKENET_LINK_RX / CLKENET_PHY_RX

R344 0 5% 1/16W MF 402 — CLKENET_LINK_GBE_REF / CLKENET_PHY_GBE_REF

CRITICAL U49 88E1111 BCC

TX_CLK, RX_CLK, 125CLK

TXD0–TXD7, TX_EN, TX_ER, GTX_CLK

RXD0–RXD7, RX_DV, RX_ER, CRS, COL, MDC, MDIO

INT-/INT+, RESET, COMA, S_IN+, S_IN-, S_OUT+, S_OUT-, S_CLK+, S_CLK-, HSDAC+, HSDAC-, XTAL1, XTAL2, VSSC

CTRL10, DVDD, VDDO, VDDOH, VDDOX, AVDD, GND

MDI0+, MDI0-, MDI1+, MDI1-, MDI2+, MDI2-, MDI3+, MDI3-

LED_LINK10, LED_LINK100, LED_LINK1000, LED_DUPLEX, LED_RX, LED_TX

CONFIG0–CONFIG6

TDI, TDO, TCK, TMS, TRST, RSET, SEL_OSC, SEL_2.5V

C492 C511 C517 C502 C465 C475 0.1UF/0.01UF 20% 10V/16V CERM 402

PLACE CAPS (IN ORDER) ON PINS 1, 6, 10/15, 57/62, 67/71, 85

C464 C472 C453 C503 C501 C496 0.1UF/10uF 20% 10V/6.3V CERM 402/805

PLACE CAPS (IN ORDER) ON PINS 5, 21/26, 48/52, 66/72, 88, 96

L34 FERR-EMI-600-OHM SM

+2_5V_MARVELL_AVDD

C497 C504 C487 C476 0.1UF/0.01UF 20% 10V/16V CERM 402

C754 10uF 20% 6.3V CERM 805

PLACE CAPS (IN ORDER) ON PINS 32/35, 36/40, 45 & 78

+2_5V_MAIN

R465 0 5% 1/16W MF 603

PLACE CLOSE TO ETHERNET CONNECTOR

NO STUFF R438 0 5% 1/10W MF 805 — CHGND1

C488 C466 C506 C520 0.1UF 20% 10V CERM 402

PLACE CAPS AT TRANSFORMER PINS 1, 4, 7 & 10

CRITICAL J17 RJ45 RT-TH

RJ45_DP<0>, RJ45_C0_PD, RJ45_DN<0>, RJ45_DP<1>, RJ45_C1_PD, RJ45_DN<1>, RJ45_DP<2>, RJ45_C2_PD, RJ45_DN<2>, RJ45_DP<3>, RJ45_C3_PD, RJ45_DN<3>

Short shielded RJ-45 — CHGND1

SM XFR-ENET-1000BT T1 CRITICAL

R735 R733 R382 R347 75 5% 1/16W MF 402 — ENET_CTAP_CHGND

C457 100pF 10% 3KV CERM 1808 — CHGND1

+2_5V_MARVELL

R371 10K 5% 1/16W MF 402

R345 10K 5% 1/16W MF 402

R354 1.5K 1% 1/16W MF 402

R343 1K 5% 1/16W MF 402 — INT_ENET_RST_L

D1 1N914 SOT23 — IO_RESET_L / ENET_RST_L

ENET_ENERGY_DET

Q15 2N7002DW SOT-363 — AC_IN

Q15 2N7002DW SOT-363 — SLEEP_L_LS5

C755 2.2uF 20% 10V CERM 805

PLACES PHY IN "COMA" MODE WHEN ASLEEP ON BATTERY (SAVES POWER)

ENET_HSDACP, ENET_HSDACM

SEE CONFIG TABLES (BELOW)

JTAG_ENET_TDI, JTAG_ASIC_TDO_TP, JTAG_ASIC_TCK, JTAG_ASIC_TMS, JTAG_ASIC_TRST_L

ENET_RSET

R346 R372 R404 R413 49.9 1% 1/16W MF 402

R355 R381 R406 R428 49.9 1% 1/16W MF 402

MDI0_PD, MDI1_PD, MDI2_PD, MDI3_PD

C454 C477 C493 C505 0.01UF 20% 16V CERM 402

PLACE RESISTORS CLOSE TO PHY

NO STUFF R435 20K 5% 1/16W MF 402

PUT CRYSTAL CIRCUIT CLOSE TO PHY

R427 0 5% 1/16W MF 402

CRITICAL Y3 25.0000M 8X4.5MM-SM — CLK25M_XTAL_IN

C555 C491 33pF 5% 50V CERM 402

Y3'S LOAD CAPACITANCE IS 20PF

NO STUFF R393 R403 49.9 1% 1/16W MF 402

R335 10K 5% 1/16W MF 402

R380 4.99K 1% 1/16W MF 402

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0703	197S0037	ALTERNATE	Y3	
197S0603	197S0037	ALTERNATE	Y3	ALT FOR SIWARD

CONFIG DEFINITIONS	
PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS			
PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

MARVELL 88E1111

10/100/1000 ETHERNET

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6582 | REV. C

SCALE NONE | SHT 27 OF 44

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0052	197S0011	?	G1	SIWARD ALT FOR FW OSC

DSX STRAP OPTIONS

0 -> BILINGUAL PORT

1 -> A-ONLY PORT

PLACE NEAR PHY

PLACE NEAR PHY

CAPACITOR IN CONJUCTION WITH INTERNAL PULLUP PROVIDES RESET PULSE WHEN PHY FIRST RECEIVES POWER

VOUT = 1.22*(1+R2/R1)+ IADJ*R2

IADJ = 30NA AT 25C

PWR CLASS = 100

(MAY PROVIDE POWER, OR MAY REQUIRE UP TO 3W)

(PC0 IS MSB, PC2 IS LSB)

1MA(MAX) BUS HOLDER EACH

FIREWIRE

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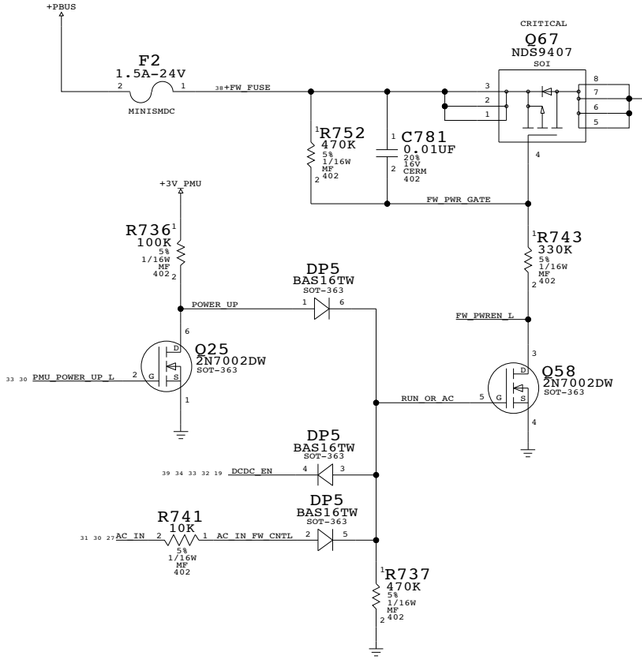
APPLE COMPUTER INC.

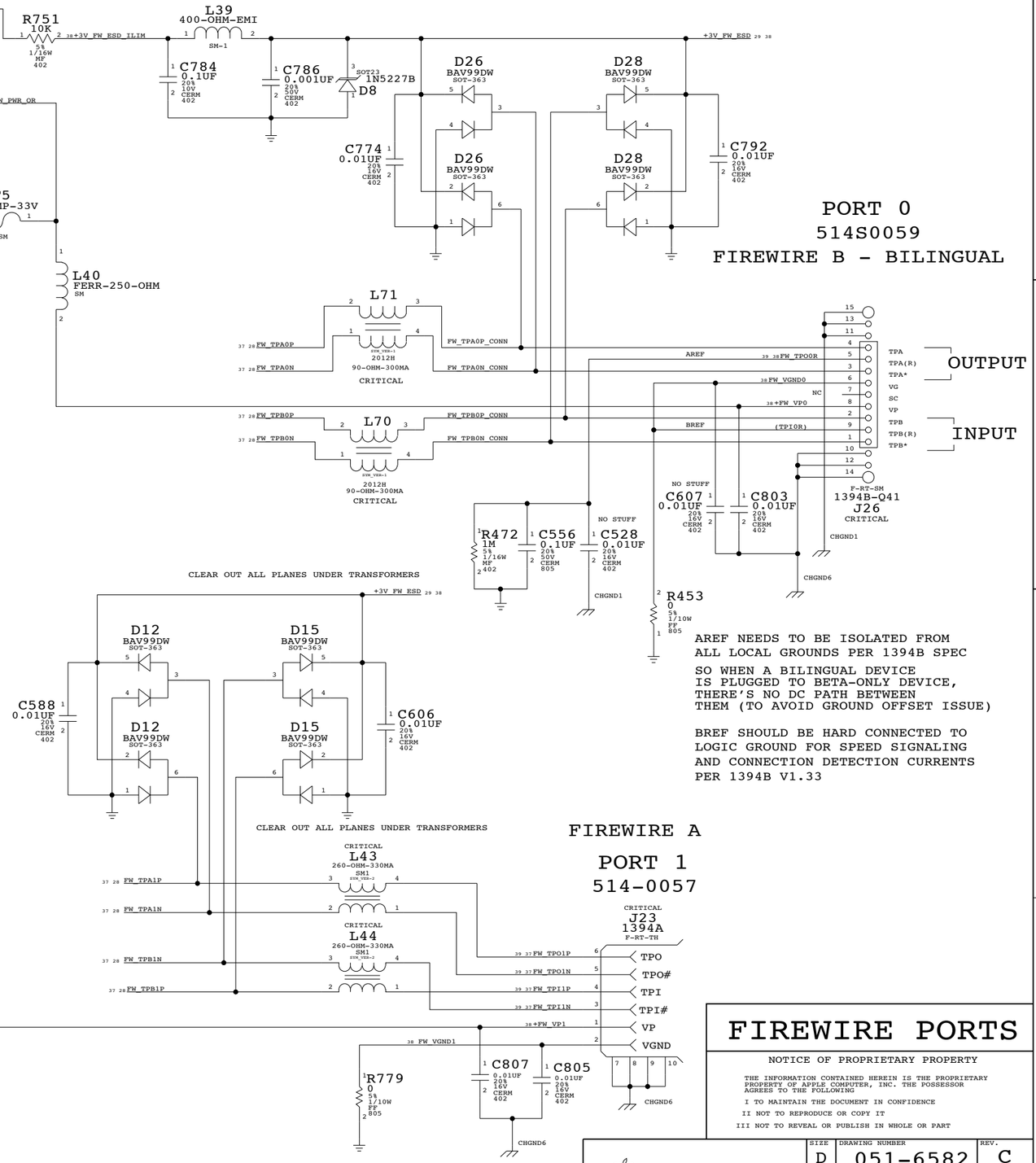
SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 28 OF 44	

PORT POWER SWITCH



ENABLES PORT POWER WHEN MACHINE IS RUNNING OR WHEN ASLEEP ON AC

STATE	PMU_POWER_UP_L	POWER_UP	DCDC_EN	AC_IN	LTC4210_ON
SHUTDOWN (AC)	1	0	0	1	OFF
SLEEP (AC)	1	0	1	1	ON
RUN (AC)	0	1	1	1	ON
SHUTDOWN (BATT)	1	0	0	0	OFF
SLEEP (BATT)	1	0	1	0	OFF (PULL-DOWN RESISTOR)
RUN (BATT)	0	1	1	0	ON
	2.99V	+3V_PMU	+4_6V_BU	+3V_PMU	



PORT 0
514S0059
FIREWIRE B - BILINGUAL

AREF NEEDS TO BE ISOLATED FROM ALL LOCAL GROUNDS PER 1394B SPEC

SO WHEN A BILINGUAL DEVICE IS PLUGGED TO BETA-ONLY DEVICE, THERE'S NO DC PATH BETWEEN THEM (TO AVOID GROUND OFFSET ISSUE)

BREF SHOULD BE HARD CONNECTED TO LOGIC GROUND FOR SPEED SIGNALING AND CONNECTION DETECTION CURRENTS PER 1394B V1.33

FIREWIRE A

PORT 1
514-0057

FIREWIRE PORTS

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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SCALE: NONE	SHT 29 OF 44	

+3V_PMU

R505 470K 5% 1/16W MF 402 — CHARGE_LED_L 30 31 39
R504 10K 5% 1/16W MF 402 — PMU_POWER_UP_L 29 30 33
R492 10K 5% 1/16W MF 402 — SOFT_PWR_ON_L 22 23 30 34
R536 100K 5% 1/16W MF 402 — MAIN_RESET_L 14 17 18 20 24 26 30 39
RP40 100K 5% 1/16W SM1 — IO_RESET_L 17 23 26 27 30
RP40 100K 5% 1/16W SM1 — SLEEP 23 25 30 33 35 39
RP40 100K 5% 1/16W SM1 — INT_RESET_L 9 13 30
RP40 100K 5% 1/16W SM1 — INT_SUSPEND_REQ_L 8 30
R782 1K 5% 1/16W MF 402 — PMU_BYTE 30
R787 10K 5% 1/16W MF 402 — PMU_CNVSS 30

+3V_PMU

C643 10UF 20% 6.3V CERM 805
C574 0.1UF 20% 10V CERM 402
C835 0.1UF 20% 10V CERM 402
R778 4.7 5% 1/16W MF 402 — +3V_PMU_AVCC 25 30 38
C827 0.1UF 20% 10V CERM 402

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1008	1	IC,PMU,V81B	U33	

CPU_VCORE_HI_OC/PMU_AP should have a pulldown for coming out of reset. MLB will have a pull-up to +3V_MAIN or +3V_SLEEP, which will act as our pulldown since both are off during PMU reset.

U33 M16C62 FLAS — CRITICAL — OMIT — VCC 14 60 — AVCC 97 — VSS 12 62 — 94

39 23 KBD_Y<0>	86	P00_D0	P50_WRL_WR
39 23 KBD_Y<1>	85	P01_D1	P51_WRH_BHE
39 23 KBD_Y<2>	84	P02_D2	P52_RD
39 23 KBD_Y<3>	83	P03_D3	P53_BCLK
39 23 KBD_Y<4>	82	P04_D4	P54_HLDA
39 23 KBD_Y<5>	81	P05_D5	P55_HOLD
39 23 KBD_Y<6>	80	P06_D6	P56_ALE
39 23 KBD_Y<7>	79	P07_D7	P57_RDY_CLKOUT
PMU_NUMLOCK_LED_L	78	P10_D8	P60_CTS0_RTS0
PMU_CAPSLOCK_LED_L	77	P11_D9	P61_CLK0
31 30 39 CHARGE_LED_L	76	P12_D10	P62_RXD0
30 23 33 PMU_POWER_UP_L	75	P13_D11	P63_TXD0
NC	74	P14_D12	P64_CTS1_RTS1_CTS0_CLKS1
34 30 23 22 SOFT_PWR_ON_L	73	P15_D13_INT3	P65_CLK1
39 25 14 COMM_RING_DET_L	72	P16_D14_INT4	P66_RXD1
14 INT_WATCHDOG_L	71	P17_D15_INT5	P67_TXD1
39 23 KBD_X<0>	70	P20_A0_D0	P70_TXD2_SDA_TA0OUT
39 23 KBD_X<1>	69	P21_A1_D1_D0	P71_RXD2_SCL_TA0IN_TB5IN
39 23 KBD_X<2>	68	P22_A2_D2_D1	P72_CLK2_TA1OUT_V
39 23 KBD_X<3>	67	P23_A3_D3_D2	P73_CTS2_RTS2_TA1IN_V
39 23 KBD_X<4>	66	P24_A4_D4_D3	P74_TA2OUT_W
39 23 KBD_X<5>	65	P25_A5_D5_D4	P75_TA2IN_W
39 23 KBD_X<6>	64	P26_A6_D6_D5	P76_TA3OUT
39 23 KBD_X<7>	63	P27_A7_D7_D6	P77_TA3IN
39 23 KBD_X<8>	61	P30_A8_D7	P80_TA4OUT_U
39 23 KBD_X<9>	59	P31_A9	P81_TA4IN_U
30 27 26 23 17 IO_RESET_L	58	P32_A10	P82_INT0
39 23 KBD_COMMAND_L	57	P33_A11	P83_INT1
39 30 23 KBD_CONTROL_L	56	P34_A12	P84_INT2
39 30 23 KBD_SHIFT_L	55	P35_A13	P85_NMI
39 30 23 KBD_OPTION_L	54	P36_A14	P86_XCOUT
39 23 KBD_FUNCTION_L	53	P37_A15	P87_XCIN
14 PMU_INT_L	52	P40_A16	P90_TB0IN_CLK3
39 23 KBD_ID	51	P41_A17	P91_TB1IN_SIN3
7 CPU_PLL_STOP_OC	50	P42_A18	P92_TB2IN_SOUT3
NC	49	P43_A19	P93_DA0_TB3IN
39 35 33 30 25 23 SLEEP	48	P44_CS0	P94_DA1_TB4IN
	47	P45_CS1	P95_ANEX0_CLK4
8 INT_SUSPEND_ACK_L	46	P46_CS2	P96_ANEX1_SOUT4
30 8 INT_SUSPEND_REQ_L	45	P47_CS3	P97_ADTRG_SIN4
30 PMU_BYTE	6	BYTE	P100_AN0
	11	XOUT	P101_AN1
	13	XIN	P102_AN2
PMU_RESET_L	10	RESET	P103_AN3
38 30 25 +3V_PMU_AVCC	96	VREF	P104_AN4_KI0
30 PMU_CNVSS	7	CNVSS	P105_AN5_KI1
			P106_AN6_KI2
			P107_AN7_KI3

(PMU_AP)			
44	CPU_VCORE_HI_OC	7 34	
43	INT_RESET_L	9 13 30	
42	MAIN_RESET_L	14 17 18 20 24 26 30 39	
41	NC		
40	PMU_INT_NMI	14	
39	PMU_EPM	30	
38	INT_PU_RESET_L	13 25 30	
37	PMU_CPU_HRESET_L	23	
36	PMU_ACK_L	14	
35	PMU_CLK	14	
34	PMU_FROM_INT	14	
33	PMU_TO_INT	14	
32	PMU_REQ_L	14	
31	PMU_LID_CLOSED_L	23 30	
30	PMU_RESET_BUTTON_L	25 30	
29	PMU_NMI_BUTTON_L	25 30	
28	TPAD_RXD	23 30	
27	TPAD_TXD	23 30	
26	SYSTEM_CLK_EN	14	
25	CPU_CLK_EN	8	
24	PMU_CHARGE_V	31	
23	PMU_CHRG_BATT_0	31	
22	NC (CHARGE_I)		
21	NC		
20	PMU_SLEEP_LED_L	23	
19	CPU_SMI_L	5	
18	POWER_VALID	30	
17	PMU_PME_L	14 26 30	
16	INT_PEND_PROC_INT	14	
15	PMU_NMI_L	30	
9			
8			
5	PMU_BATT0_DET_L		
4	PMU_BATT1_DET_L_PU	30	
3	NC		
2	NC		
1	INT_PROC_SLEEP_REQ_L	14	
100	PMU_POWERUP_OK	30	
99	NC		
98	PMU_OOPS	30	
95	THERM_L_OC	25	
93	PMU_AC_IN		
92	PMU_AC_DET	30	
91	NC		
90	PMU_I2C_CLK	30	
89	PMU_I2C_DATA	30	
88	PMU_SMB_CLK	30 31	
87	PMU_SMB_DATA	30 31	

R518 2.2K 5% 1/16W MF 402 — 23 NUMLOCK_LED_L
R513 2.2K 5% 1/16W MF 402 — 23 CAPSLOCK_LED_L

Keep crystal subcircuit close to PMU.

CLK32K_PMU_XOUT
CLK32K_PMU_XIN
R593 1K 5% 1/16W MF 402 — PMU_BATT_DET_L 30 31 39
R572 1K 5% 1/16W MF 402 — AC_IN 27 29 31
NO STUFF R786 10M 5% 1/16W MF 402
R785 0 5% 1/16W MF 402
CRITICAL Y7 SM-1 32.768K
C832 12PF 5% 50V CERM 402
C831 12PF 5% 50V CERM 402
CLK32K_PMU_XOUT_UF

Y7'S LOAD CAPACITANCE IS 12.5PF

R535 10K 5% 1/16W MF 402 — 30 PMU_EPM
R569 10K 5% 1/16W MF 402 — 30 25 PMU_RESET_BUTTON_L
R585 100K 5% 1/16W MF 402 — 30 PMU_POWERUP_OK
R788 470K 5% 1/16W MF 402 — 30 PMU_BATT1_DET_L_PU
R592 470K 5% 1/16W MF 402 — 39 31 30 PMU_BATT_DET_L
RP41 10K 5% 1/16W SM1 — 30 25 PMU_NMI_BUTTON_L
RP41 10K 5% 1/16W SM1 — 30 PMU_NMI_L
R768 7.15K 1% 1/16W MF 402 — 31 30 PMU_SMB_DATA
R769 7.15K 1% 1/16W MF 402 — 31 30 PMU_SMB_CLK
+3V_SLEEP
RP41 10K 5% 1/16W SM1 — 30 PMU_I2C_DATA
RP41 10K 5% 1/16W SM1 — 30 PMU_I2C_CLK
+5V_SLEEP
R573 10K 5% 1/16W MF 402 — 30 23 TPAD_RXD
R584 10K 5% 1/16W MF 402 — 30 23 TPAD_TXD
+3V_MAIN
R597 100K 5% 1/16W MF 402 — 30 POWER_VALID
R596 10K 5% 1/16W MF 402 — 30 26 14 PMU_PME_L
R562 100K 5% 1/16W MF 402 — 30 23 PMU_LID_CLOSED_L
R583 10K 5% 1/16W MF 402 — 30 PMU_OOPS
R544 100K 5% 1/16W MF 402 — 30 25 13 INT_PU_RESET_L

UNDERVOLTAGE RESET CIRCUIT

+3V_PMU
R765 1K 5% 1/16W MF 402
14 +3V_PMU_RESET
C812 0.1UF 10% 10V CERM 402
CRITICAL
U51 MAX6804 SOT143 — VCC MR* RSET* GND
39 30 PMU_KB_RESET_L
CLK10M_PMU_XOUT
CLK10M_PMU_XIN
PMU_RESET_L
38 30 25 +3V_PMU_AVCC
30 PMU_CNVSS
NO STUFF R595 10M 5% 1/16W MF 402
R594 0 5% 1/16W MF 402 2
CRITICAL Y6 10.0000M 8X4.5MM-SM
CLK10M_PMU_XOUT_UF
C666 12PF 5% 50V CERM 402
C664 12PF 5% 50V CERM 402

Keep crystal subcircuit close to PMU.
Y6'S LOAD CAPACITANCE IS 12PF

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0704	197S0041		Y6	ALT CRYSTAL SIZE
197S0604	197S0041		Y6	ALT FOR SIWARD

PMU KEYBOARD RESET CIRCUIT

+3V_PMU
74LVC32 TSSOP U24
34 30 23 22 SOFT_PWR_ON_L
39 30 23 KBD_CONTROL_L
11 PMU_KB_RESET_IN1
+3V_PMU
74LVC32 TSSOP U24
4 5 6 PMU_KB_RESET_L 30 39
+3V_PMU
74LVC32 TSSOP U24
39 30 23 KBD_SHIFT_L
39 30 23 KBD_OPTION_L
8 PMU_KB_RESET_IN2

Q11 ADAPTER DETECTION SCHEME

CASE	ADAPTER	PIN VOLT	ID VOLT RANGE	SYSTEM STATUS
1	Q11 (65W)	2.007V- 2.066V	1.65V- 2.31V	RECOGNIZES AS Q11 FULL FUNCTIONS
2	A29 (45W)	2.558V- 2.661V	2.31V- 2.97V	RECOGNIZES AS A29 LIMITED FUNCTIONS
3	AIRLINE	0.589V- 0.663V	0.33V- 0.99V	FULL FUNCTIONS NO BATTERY CHARGING
4	HOOPER	3.19V- 3.28V	2.97V- 3.30V	RECOGNIZES AS HOOPER LIMITED FUNCTIONS

A29 DETECT CIRCUIT

+3V_PMU
38 32 +4.85V_RAW
R501 100K 1% 1/16W MF 402
ADAPTER_DET 31 39
R502 100K 1% 1/16W MF 402
30 PMU_AC_DET
R503 402K 1% 1/16W MF 402
2.34V_REF
R491 52.3K 1% 1/16W MF 402
C558 0.1UF 20% 10V CERM 402
R517 100K 5% 1/16W MF 402
A29_DETECT 31
U27 LMC7211 SM CRITICAL
A29_DET_L
Q22 2N7002 SM
R476 4.7M 5% 1/16W MF 402
R475 127K 1% 1/16W MF 402
50MV OF HYSTERSIS

PMU

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SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 30 OF 44	

DC POWER INPUT

(POWER JACK, ETC. ON SEPARATE BOARD)

CRITICAL

J18
87438-0833
M-RT-SM

CHARGE_LED_L
+ADAPTER
ADAPTER_DET

NO STUFF
C757 0.1UF 20% 50V CERM 805

PLACE CLOSE TO DC INPUT

R396 20K 1% 1/16W MF 402

DC INRUSH LIMITER

+ADAPTER_SW
+ADAPTER_SENSE

Q13 SI4435DY SOI
Q16 SI4435DY SOI

R414 330K 5% 1/16W MF 402
C458 0.1UF 20% 50V CERM 805

AC_ENABLE_GATE
AC_ENABLE_L

R374 470K 5% 1/16W MF 402

Q10 2N7002DW SOT-363

+3V_PMU

R395 102K 1% 1/16W MF 402
R364 102K 1% 1/16W MF 402
C468 0.01UF 20% 16V CERM 402
R363 10K 5% 1/16W MF 402

U15 LMC7211 SM
CRITICAL

1V20_REF
AC_IN
AC_DIV

R375 10K 1% 1/16W MF 402
R365 57.6K 1% 1/16W MF 402
R394 1M 5% 1/16W MF 402

AC_IN_L

Q10 2N7002DW SOT-363

R383 470K 5% 1/16W MF 402

GREATER THAN 13.5V DETECT

BCKFD_PROT_GATE
BCKFD_PROT_EN_L

C592 0.1UF 20% 50V CERM 805
R499 68K 5% 1/16W MF 402
R474 47K 5% 1/16W MF 402

Q21 2N7002DW SOT-363

PLACE U23 NEXT TO R460

U23 SENSE VOLTAGE DROP ACROSS R460

C572 0.01UF 20% 50V CERM 603

U23 MAX4172 TSSOP
RS+ RS- PG NC1 NC2 OUT GND
CRITICAL

+24V_PBUS
MAX4172_OUT

R454 2.21K 0.1% 1/16W MF 603
C883 0.1UF 10% 50V X7R 603-1

A29_CURRENT_ADJ

R460 0.025 1% 1W MF 2512

IF A29 ADAPTER USED, ADJUST CURRENT SETTING

R488 4.7 5% 1/16W MF 402
R498 4.7 5% 1/16W MF 402

1772_CSSP
1772_CSSN

C578 0.47UF 10% 50V CERM 1206
C579 0.47UF 10% 50V CERM 1206

R754 100K 1% 1/16W MF 402
D9 1N914 SOT23
R755 12.7K 1% 1/16W MF 402
C600 1UF 20% 50V CERM1 1210

1772_DCIN
1772_ACIN
1772_ACOK_L
(+3V_PMU)
1772_VCTL
1772_ICTL
1772_ICHG
1772_IINP

U31 MAX1772 QSOP
CRITICAL

CSSP CSSN DCIN CELLS ACIN LDO ACOK DLOV RFIN BST VCTL DHI ICTL LX ICHG DLO IINP PGND CCV CSIP CCI CSIN CCS BATT REF = 4.096V REF_CLS GND

1772_CELLS
1772_DLOV
1772_BST
1772_DHI
1772_LX
1772_DLO
(GND)
1772_CSIP
1772_CSIN

OD OUTPUT LOW - WHEN AC GREATER THAN 18V

R542 1K 1% 1/16W MF 402
R566 1K 1% 1/16W MF 402
R565 48.7K 1% 1/16W MF 402
R560 4.12K 1% 1/16W MF 402
R567 27.4K 1% 1/16W MF 402
R558 10K 1% 1/16W MF 402
R548 10K 1% 1/16W MF 402

R526 1K 1% 1/16W MF 402
C622 0.01UF 20% 16V CERM 402
C616 0.01UF 20% 16V CERM 402
C652 1UF 20% 10V CERM 603
C817 0.1UF 20% 25V CERM 603
C802 0.1UF 20% 25V CERM 603

1772_CCV_RC
1772_REF
1772_CLS

R497 1K 1% 1/16W MF 402
C621 0.1UF 20% 10V CERM 402
C630 1UF 20% 10V CERM 603
R487 10K 1% 1/16W MF 402
R473 4.12K 1% 1/16W MF 402

R559 100K 5% 1/16W MF 402

1772_GND

BATT_LOW_L

Q29 2N7002DW SOT-363

BATTV_HIGH
BATTV_LOW

R561 100K 5% 1/16W MF 402
R580 5.23K 1% 1/16W MF 402

Q27 2N7002DW SOT-363

PMU_CHARGE_V

SWITCHER VOLTAGE CONTROL

PMU SELECTS BETWEEN TWO VOLTAGES

SWITCHER CURRENT CONTROL

CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V
CHARGE THROTTLED BY LOW BATTERY VOLTAGE

R578 100K 5% 1/16W MF 402

CHARGE_DISABLE

Q30 2N7002DW SOT-363

PMU_CHRG_BATT_0

C615 0.1UF 20% 10V CERM 402

U38 LMC7211 SM
CRITICAL

BATT_LOW

R588 100K 1% 1/16W MF 402
R579 499K 1% 1/16W MF 402
R599 100K 1% 1/16W MF 402
R570 100K 1% 1/16W MF 402
C658 0.047uF 10% 16V CERM 402

BATT_DIV
1V65_REF

R749 6.34K 1% 1/16W MF 402

A29_CLS_ADJ
A29_DETECT

Q65 2N7002DW SOT-363

$V_{BATT} = CELLS \times (4.096 + (0.4096 * V_{VCTL} / V_{REFIN}))$

For 4.15V cells, VCTL = 0.123 REFIN

For 4.20V cells, VCTL = 0.245 REFIN

$I_{CHG} = (0.2048/R_{62}) * (V_{ICTL} / V_{REFIN})$

1MSEC INTEGRATION TIME

R742 1K 1% 1/16W MF 402
C771 0.1UF 20% 10V CERM 402

IAC_RC_COMP

+3V_PMU

R747 42.2K 0.1% 1/16W FF 603
C772 0.1UF 20% 10V CERM 402

U50 LMC7111 SOT23-5
CRITICAL

IAC_FB

PLACE R358 CLOSE TO LTC1625
ROUTE LTC1625_ITH CAREFULLY

LTC1625_ITH

DP4 BAS16TW SOT-363

R358 150 1% 1/16W MF 402

1625_COMP

ADAPTER_I_REG

R466 10K 1% 1/16W MF 402

CURRENT_THRESHOLD

R738 42.2K 0.1% 1/16W FF 603
R734 82.5K 0.1% 1/16W FF 603

Q20 2N7002DW SOT-363

A29_DETECT

R739 51.1K 0.1% 1/16W FF 603

IF ADAPTER IS OVER 18V, ADJUST CURRENT SETTING

OVER_18V_ADJ

R748 100K 5% 1/16W MF 402

Q20 2N7002DW SOT-363

AC_GTR_18V

C775 1UF 20% 10V CERM 603

Q65 2N7002DW SOT-363

1772_ACOK_L

BATTERY SWITCH-OVER CIRCUIT

+BATT

F4 5AMP-125V SM-2
F3 5AMP-125V SM-2

+24V_PBUS
+PBUS

+BATT_24V_FUSE
+BATT_14V_FUSE

CRITICAL

Q24 SI4435DY SOI

Q76 SUD45P03 TO-252

R490 47K 5% 1/16W MF 402
R746 47K 5% 1/16W MF 402

BATT_24V_GATE
BATT_14V_GATE

R512 10K 5% 1/16W MF 402
R744 10K 5% 1/16W MF 402

DP4 BAS16TW SOT-363

BATT_24PBUS_EN
BATT_14PBUS_EN

Q21 2N7002DW SOT-363

AC_IN_L
AC_IN_L_RC

DP4 BAS16TW SOT-363

R489 158K 1% 1/16W MF 402
C593 10UF 20% 6.3V CERM 805

WHEN AC IS IN, P-CHANNEL FETS ARE QUICKLY (DIODE) TURNED OFF
WHEN AC IS NOT PLUGGED, P-CHANNEL FETS ARE ON
RC TIME IS 480K*10UF @ +3V_PMU

R549 100K 5% 1/16W MF 402
C624 0.1UF 20% 25V CERM 603

R571 33 5% 1/8W FF 1206
D10 1N914 SOT23
1772_LDO
1772_BST_ESR
R774 4.7 5% 1/16W MF 603

C608 0.1UF 20% 50V CERM 805

Q63 IRF7805 SM
CRITICAL

C547 2.2UF 10% 25V CERM 1812
C562 2.2UF 10% 25V CERM 1812
C563 2.2UF 10% 25V CERM 1812
C557 2.2UF 10% 25V CERM 1812
C564 2.2UF 10% 25V CERM 1812

L42 10uH SM1
CRITICAL

+BATT_RSNS
R763 0.05 1% 1W MF 2512

D30 MBRS140T3 SM

+BATT_24V_FUSE

C619 4.7UF 20% 25V CERM 1206
C632 4.7UF 20% 25V CERM 1206
C617 4.7UF 20% 25V CERM 1206
C824 33UF 20% 25V ELEC SM1

Q64 IRF7811W SO-8
CRITICAL

NO STUFF
C906 0.0022UF 10% 50V CERM 402

XW19 SM

R543 1 5% 1/16W MF 603
R511 1 5% 1/16W MF 603

C631 4.7UF 20% 25V CERM 1206
C633 4.7UF 20% 25V CERM 1206
C618 4.7UF 20% 25V CERM 1206

+BATT_VSNS

BATTERY CONNECTOR

CRITICAL
J25
87438-0833
M-RT-SM

+BATT_POS
(BATT_IN_PD)
BATT_CLK
BATT_DATA
PMU_BATT_DET_L
BATT_NEG

L9 FERR-EMI-100-OHM SM
L53 FERR-50-OHM SM
L10 FERR-EMI-100-OHM SM
L8 FERR-EMI-100-OHM SM
L12 FERR-50-OHM SM

PMU_SMB_CLK
PMU_SMB_DATA

BATTERY CHARGER

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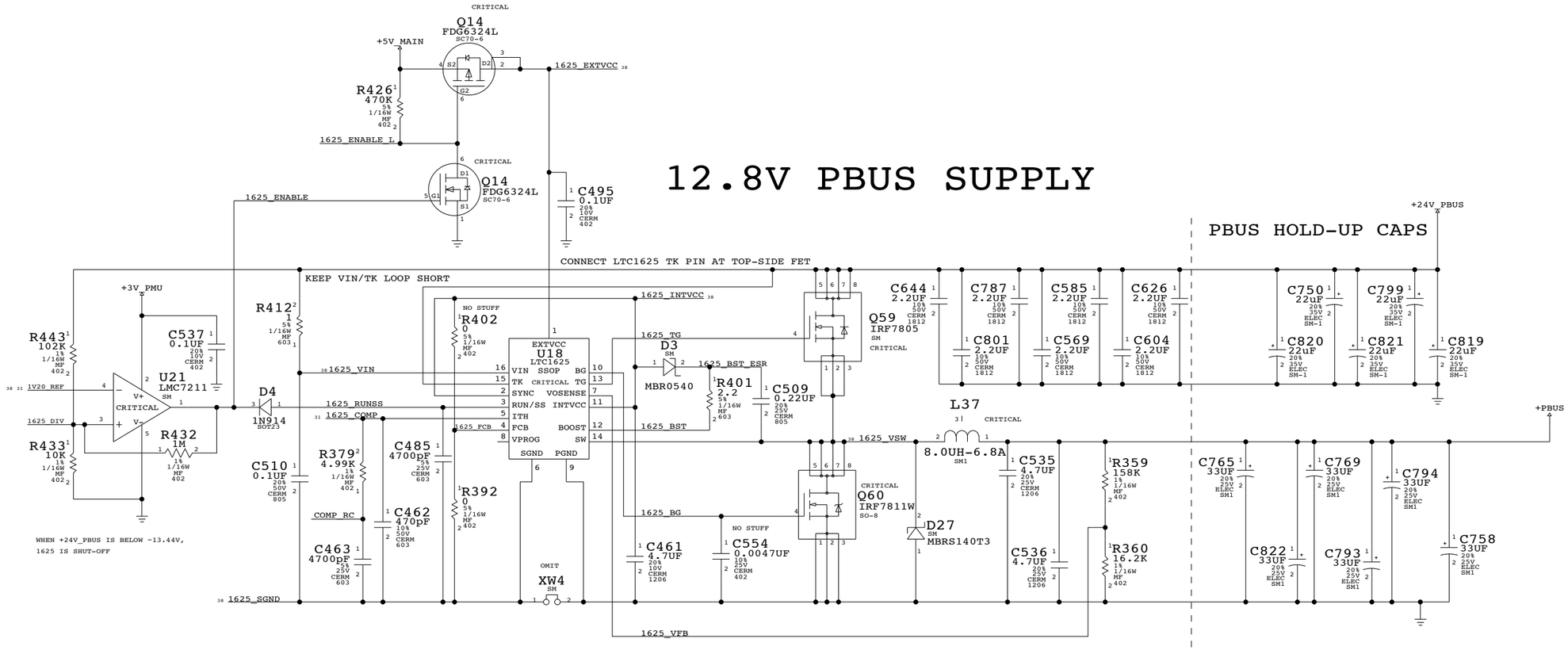
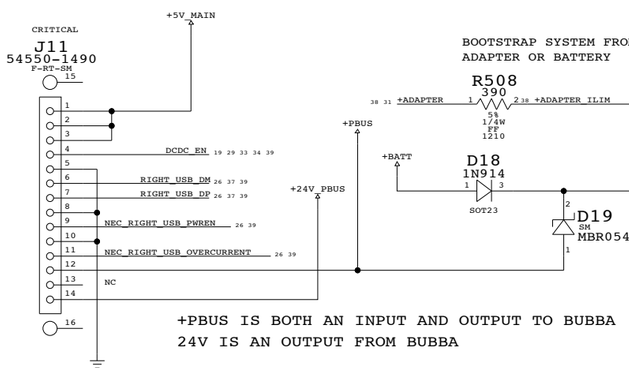
SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 31 OF 44	

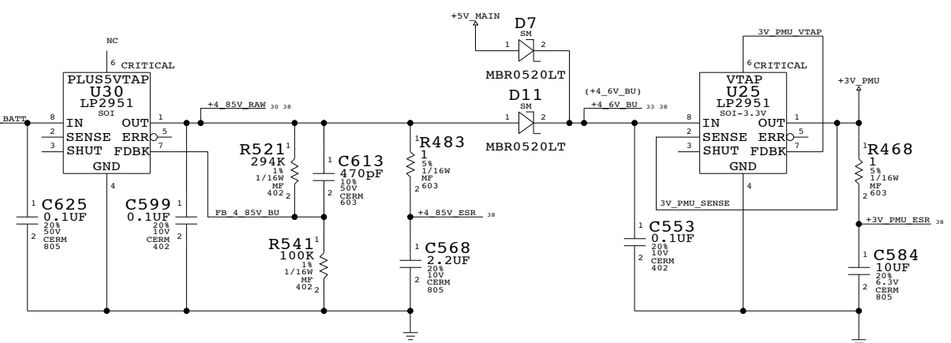
12.8V PBUS SUPPLY



BACKUP BATTERY / USB CONNECTOR



PMU SUPPLY



12.8V REGULATOR

APPLE COMPUTER INC.

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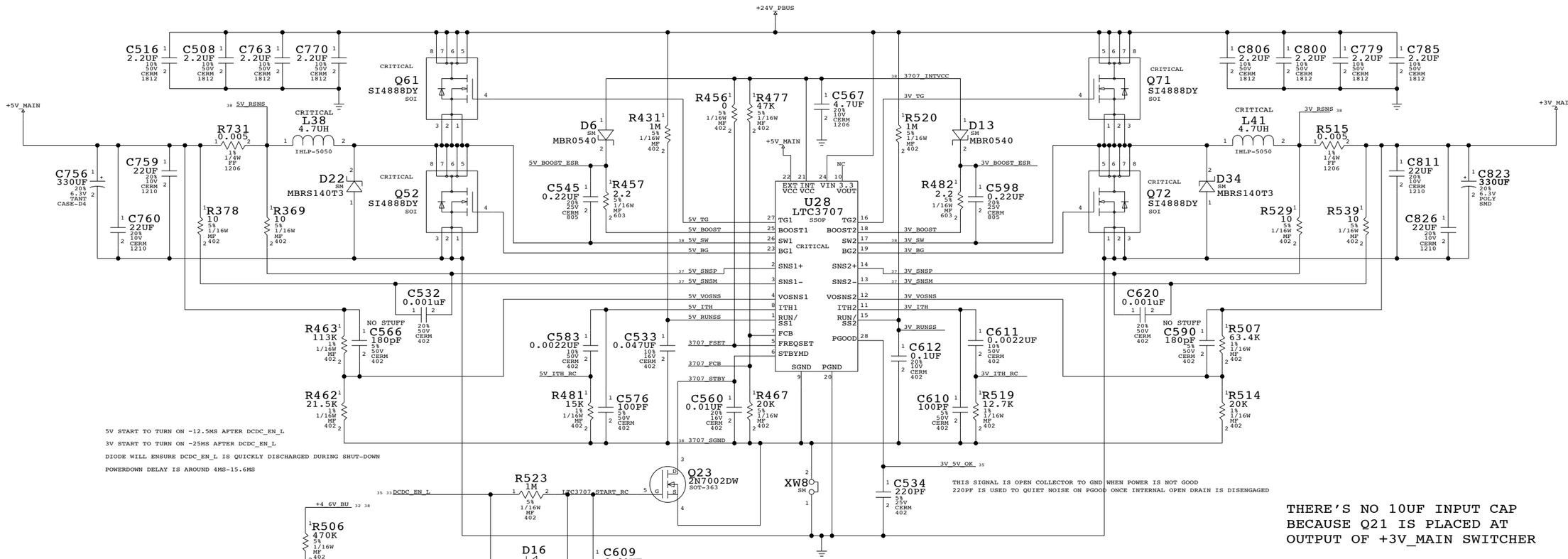
D	051-6582	C

SCALE: NONE

SHT 32 OF 44

3.3V/5V MAIN SUPPLY



5V START TO TURN ON ~12.5MS AFTER DCDC_EN_L
3V START TO TURN ON ~25MS AFTER DCDC_EN_L
DIODE WILL ENSURE DCDC_EN_L IS QUICKLY DISCHARGED DURING SHUT-DOWN
POWERDOWN DELAY IS AROUND 4MS-15.6MS

THERE'S NO 10UF INPUT CAP
BECAUSE Q21 IS PLACED AT
OUTPUT OF +3V_MAIN SWITCHER

3.3V/5V REGULATOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 33 OF 44	

VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage
(approx. 7ms delay)

1.175V -> 1.025V 1.30V -> 1.10V

SEL = 0; Y1=A1
SEL = 1; Y1=B1

Keep trace fat (40-100 mils) and short!!

MAX1717 VID CAN TAKE 3.3V TO 5.5V INPUTS

Connect MAX1717 GND pin 13 to GND at bottom-side FET

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V, HENCE VOFFSET = 2.0V * (R1/(R1+R2)) AND VCORE = VDAC + VOFFSET.

NOTE: R310 (R2) NO STUFFED FOR NO OFFSET CASE

ROUTE AS DIFFERENTIAL PAIR

Keep trace fat and short!!

PLACE THIS SHORT AT PIN OF 1000uF CAP CLOSEST TO CPU

PLACE C423 CLOSE TO PINS 15 & 13!!

OUTPUT VOLTAGE

V_{DAC} D4=0	V_{DAC} D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	A/B_ = Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1

If all pull-ups are >=100K and all pull-downs are <=1K, $V_A = V_B$.

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0022	128S0034	?	C728,C729,C730,C731,C732,C733,C734,C884,C885	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S4023	1	RESISTOR	R321	?	1_30_VCORE
114S6343	1	RESISTOR	R321	?	1_32_VCORE

FMAX CONNECTOR

CRITICAL
NO STUFF
J5
M-ST-SM-52465-1217

NC (RFU)

VCORE SUPPLY

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SCALE: NONE	SHT 34 OF 44	

1.5V/2.5V SWITCHER

+1_5V_SLEEP LOADS

1) AGP I/O - IF USING D3COLD
2) MAXBUS I/O - IF 1.5V INTERFACE

+1_5V_MAIN LOADS

1) INTREPID CORE
2) AGP I/O IF USING D3HOT

+2_5V_MAIN LOADS

1) MAP31 - FBCORE/FBIO IF USING D3HOT
2) GIGABIT ETHERNET - AVDDL
3) DDR SODIMMS - CORE/IO
4) DDR MUXES
5) CLOCK SLEWING I/O
6) PCI1510 CORE

+2_5V_SLEEP LOADS

1) FBCORE/FBIO IF USING D3COLD
2) INTREPID MEMORY I/O

THERE'S 100K PULL-UP ON PG 31 ALREADY

DIODE PROVIDE PROVIDE QUICK SHUT-DOWN
POWER DOWN DELAY 1.5MS TO 3.5MS

CHANGE R424 BACK TO 10K, 1%, AND STUFF 5.11K FOR 1.5V OPERATION
CONNECTING 1_5V_FB TO GND, FORCES 1.8V OUTPUT

1.8V SWITCHER

+1_8V_MAIN LOADS

1) INTREPID PLLS

+1_8V_SLEEP LOADS

1) MPC7450 - MAXBUS I/O - IF 1.8V INTERFACE
2) CPU JTAG & MaxBus Pull-ups
3) CPU PLL Config Straps
4) OPTIONAL VIDEO MEMORY (M10 PRO ONLY)

1.5V/1.8V/2.5V SUPPLIES

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SCALE: NONE	SHT 35 OF 44	

DIGITAL SIGNALS

GROUP	SIG_NAME		MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
MAXBUS	CPU_AACK_L				250.0000	10_MIL_SPACING			5 8
	CPU_ADDR<0..31>		5		250			83_MHZ	5 8
	CPU_ARTRY_L				250.0000	10_MIL_SPACING			5 8
	CPU_BG_L				250.0000	10_MIL_SPACING			5 8
	CPU_BR_L				250.0000	10_MIL_SPACING			5 8
	CPU_CI_L		5		250.0000				5 8
	CPU_DATA<0..31>		5		250			83_MHZ	6 8
	CPU_DATA<32..63>		5		250			83_MHZ	6 8
	CPU_DBG_L		5		250.0000	10_MIL_SPACING			5 8
	CPU_DTI<0..2>		5		250				5 8
	CPU_DRDY_L_UF					10_MIL_SPACING			
	CPU_DRDY_L				250.0000	10_MIL_SPACING			5 8
	CPU_GBL_L		5		250.0000				5 8
	CPU_HIT_L				250.0000	10_MIL_SPACING			5 8
	CPU_QACK_L		5		250.0000	10_MIL_SPACING			5 8
	CPU_QREQ_L				250.0000	10_MIL_SPACING			5 8
	CPU_TA_L				250.0000	10_MIL_SPACING			5 8
	CPU_TBST_L		5		250.0000	10_MIL_SPACING			5 8
	CPU_TEA_L				250.0000				5 8
	CPU_TS_L				250.0000	10_MIL_SPACING			5 8
	CPU_TSIZ<0..2>		5		250				5 8
	CPU_TT<0...4>		5		250				5 8
	CPU_WT_L		5		250.0000				5 8
GROUP 0	MEM_DATA<7..0>		4		200			167_MHZ	9 10
	RAM_DATA_A<7..0>		4		200			167_MHZ	10 11
	RAM_DATA_B<7..0>		4		200			167_MHZ	10 11
	MEM_DQS<0>	TOTAL LENGTH CONTROLLED BY SPREADSHEET			200				9 10
	RAM_DQS_A<0>		4		200				10 11
	RAM_DQS_B<0>		4		200				10 11
	MEM_DQM<0>		4		200				9 10
	RAM_DQM_A<0>		4		200				10 11
	RAM_DQM_B<0>		4		200				10 11
GROUP 1	MEM_DATA<15..8>		4		200			167_MHZ	9 10
	RAM_DATA_A<15..8>		4		200			167_MHZ	10 11
	RAM_DATA_B<15..8>		4		200			167_MHZ	10 11
	MEM_DQS<1>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200				9 10
	RAM_DQS_A<1>		4		200				10 11
	RAM_DQS_B<1>		4		200				10 11
	MEM_DQM<1>				200				9 10
	RAM_DQM_A<1>		4		200				10 11
	RAM_DQM_B<1>		4		200				10 11
GROUP 2/3	MEM_DATA<31..16>		4		200			167_MHZ	9 10
	RAM_DATA_A<31..16>		4		200			167_MHZ	10 11
	RAM_DATA_B<31..16>		4		200			167_MHZ	10 11
	MEM_DQS<3..2>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200			167_MHZ	9 10
DDR RAM	RAM_DQS_A<3..2>		4		200			167_MHZ	10 11
	RAM_DQS_B<3..2>		4		200			167_MHZ	10 11
	MEM_DQM<3..2>		4		200			167_MHZ	9 10
	RAM_DQM_A<3..2>		4		200			167_MHZ	10 11
	RAM_DQM_B<3..2>		4		200			167_MHZ	10 11
GROUP 4/5	MEM_DATA<47..32>		4		200			167_MHZ	9 10
	RAM_DATA_A<47..32>		4		200			167_MHZ	10 11
	RAM_DATA_B<47..32>		4		200			167_MHZ	10 11
	MEM_DQS<5..4>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200			167_MHZ	9 10
	RAM_DQS_A<5..4>		4		200			167_MHZ	10 11
	RAM_DQS_B<5..4>		4		200			167_MHZ	10 11
	MEM_DQM<5..4>		4		200			167_MHZ	9 10
	RAM_DQM_A<5..4>		4		200			167_MHZ	10 11
	RAM_DQM_B<5..4>		4		200			167_MHZ	10 11
GROUP 6	MEM_DATA<55..48>		4		200			167_MHZ	9 10
	RAM_DATA_A<55..48>		4		200			167_MHZ	10 11
	RAM_DATA_B<55..48>		4		200			167_MHZ	10 11
	MEM_DQS<6>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200				9 10
	RAM_DQS_A<6>				200				10 11
	RAM_DQS_B<6>		4		200				10 11
	MEM_DQM<6>				200				9 10
	RAM_DQM_A<6>		4		200				10 11
	RAM_DQM_B<6>		4		200				10 11
GROUP 7	MEM_DATA<63..56>		4		200			167_MHZ	9 10
	RAM_DATA_A<63..56>		4		200			167_MHZ	10 11
	RAM_DATA_B<63..56>		4		200			167_MHZ	10 11
	MEM_DQS<7>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200				9 10
	RAM_DQS_A<7>				200				10 11
	RAM_DQS_B<7>				200				10 11
	MEM_DQM<7>		4		200				9 10
	RAM_DQM_A<7>		4		200				10 11
	RAM_DQM_B<7>		4		200				10 11
ADDR	MEM_ADDR<12..0>		4					83_MHZ	9
	RAM_ADDR<12..0>		6		200				9 11
CONTROL	MEM_BA<1..0>		4						9
	RAM_BA<1..0>		6		200				9 11
	MEM_CS_L<3..0>		4						9
	RAM_CS_L<3..0>		6		200				9 11
	MEM_CKE<3..0>		4						9
	RAM_CKE<3..0>		6		200				9 11
	MEM_RAS_L		4						9
	RAM_RAS_L				200.0000				9 11
	MEM_CAS_L		4						9
	RAM_CAS_L				200.0000				9 11
	MEM_WE_L		4						9
	RAM_WE_L				200.0000				9 11
	MEM_MUXSEL_H<1..0>		3						9 10
	MEM_MUXSEL_L<1..0>		3						9 10
	RAM_MUXSEL_H		5						10
	RAM_MUXSEL_L		5						10

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME			MAX_VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM	
INTREPID CLOCKS	SYSCLK_CPU_UF						10_MIL_SPACING		8
	SYSCLK_CPU			4		200.0000	10_MIL_SPACING		5 8
	INT_CPUFB_OUT			3			10_MIL_SPACING		8
	INT_CPUFB_OUT_SHORT			3			10_MIL_SPACING		8
	INT_CPUFB_OUT_NORM			3			10_MIL_SPACING		8
	INT_CPUFB_IN_NORM			3			10_MIL_SPACING		8
	INT_CPUFB_LONG			3			10_MIL_SPACING		8
	INT_CPUFB_IN					200.0000	10_MIL_SPACING		8
	SYSCLK_DDRCLK_A0_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_A0_L_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_A1_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_A1_L_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_B0_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_B0_L_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_B1_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_B1_L_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_A0	DDRCLK_A0		3		200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_A0_L	DDRCLK_A0				200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_A1	DDRCLK_A1		3		200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_A1_L	DDRCLK_A1				200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_B0	DDRCLK_B0		3		200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_B0_L	DDRCLK_B0		3		200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_B1	DDRCLK_B1		3		200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_B1_L	DDRCLK_B1		3		200.0000	10_MIL_SPACING		9 11
	INT_REF_CLK_OUT			3		200.0000	10_MIL_SPACING		14
	INT_REF_CLK_IN					200.0000	10_MIL_SPACING		14
	CLK66M_GPU_AGP_UF					200.0000	10_MIL_SPACING		12
	CLK66M_GPU_AGP			4		200.0000	10_MIL_SPACING		12 18
	INT_AGP_FB_OUT					200.0000	10_MIL_SPACING		12
	INT_AGP_FB_IN			4		200.0000	10_MIL_SPACING		12
	CLK33M_CBUS_UF					200.0000	10_MIL_SPACING		12
	CLK33M_CBUS		SHOULD BE AT MOST 4 VIAS FOR CLK	6		200.0000	10_MIL_SPACING		12 17
	CLK33M_AIRPORT_UF					200.0000	10_MIL_SPACING		12
	CLK33M_AIRPORT		SHOULD BE AT MOST 4 VIAS FOR CLK	6		200.0000	10_MIL_SPACING		12 24 39
	CLK33M_USB2_UF					200.0000	10_MIL_SPACING		12
	CLK33M_USB2		SHOULD BE AT MOST 4 VIAS FOR CLK	6		200.0000	10_MIL_SPACING		12 26
	INT_PCI_FB_OUT					200.0000	10_MIL_SPACING		12
	INT_PCI_FB_IN			3		200.0000	10_MIL_SPACING		12
MAP31	GPU_CLK27M_OUT						10_MIL_SPACING		
	GPU_CLK27M_UF						10_MIL_SPACING		
	GPU_SSCLK_UF						10_MIL_SPACING		
	GPU_SSCLK_IN						10_MIL_SPACING		
	GPU_FBCLK0						10_MIL_SPACING		
	GPU_FBCLK0_L						10_MIL_SPACING		
	GPU_FBCLK1						10_MIL_SPACING		
	GPU_FBCLK1_L						10_MIL_SPACING		
	GPU_DVO_CLKP						10_MIL_SPACING		19 20
CRYSTALS	CLK27M_GPU_XOUT						10_MIL_SPACING		
	CLK27M_XTAL_IN						10_MIL_SPACING		
	CLK27M_GPU_XIN						10_MIL_SPACING		
	CLK18M_INT_XIN						10_MIL_SPACING		14
	CLK18M_INT_XOUT						10_MIL_SPACING		14
	CLK18M_XTAL_IN						10_MIL_SPACING		14
	CLK18M_INT_EXT						10_MIL_SPACING		14
	CLK25M_ENET_XIN						10_MIL_SPACING		27
	CLK25M_ENET_XOUT						10_MIL_SPACING		27
	NEC_XT1						10_MIL_SPACING		26
	NEC_XT2		THERE'S ANOTHER 280MIL LEG				10_MIL_SPACING		26
SOUND	SND_SCLK			7		200.0000	10_MIL_SPACING		14 25 39
	SND_CLKOUT					200.0000	10_MIL_SPACING		14 25 39
ETHERNET MARVELL	CLKENET_PHY_RX					200.0000			27
	CLKENET_LINK_RX			3		200.0000	10_MIL_SPACING		13 27
	CLKENET_PHY_GBE_REF					200.0000			27
	CLKENET_LINK_GBE_REF			3		200.0000	10_MIL_SPACING		13 27
	CLKENET_PHY_TX					200.0000			27
	CLKENET_LINK_TX			5		200.0000	10_MIL_SPACING		13 27
	CLKENET_LINK_GTX					200.0000			13
	CLKENET_PHY_GTX			3		200.0000	10_MIL_SPACING		13 27
FIREWIRE	CLKFW_PHY_PCLK					200.0000			28
	CLKFW_LINK_PCLK			3		200.0000	10_MIL_SPACING		13 28
	CLKFW_PHY_LCLK			3		200.0000	10_MIL_SPACING		13 28
	CLKFW_LINK_LCLK					200.0000			13
	FW_XI					200.0000	10_MIL_SPACING		28
	FW_OSC					200.0000	10_MIL_SPACING		28

SIGNAL CONSTRAINTS - PAGE 1

APPLE COMPUTER INC.

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Digital Signals (cont'd)

GROUP	SIG_NAME	DELAY_RULE	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
AGP	AGP_AD<15..0>		5	100				66 MHz	12 18
AGP BYTES 0-1	AGP_CBE<1..0>		5	100				66 MHz	12 18
	AGP_AD_STB<0>		4	100		8 MIL SPACING			12 18
	AGP_AD_STB_L<0>		4	100		8 MIL SPACING			12 18
AGP BYTES 2-3	AGP_AD<31..16>		5	100				66 MHz	12 18
	AGP_CBE<3..2>		5	100				66 MHz	12 18
	AGP_AD_STB<1>		4	100		8 MIL SPACING			12 18
	AGP_AD_STB_L<1>			100		8 MIL SPACING			12 18
AGP SIDEBAND	AGP_SBA<7..0>		5	100				66 MHz	12 18
	AGP_SB_STB			100.0000		8 MIL SPACING			12 18
	AGP_SB_STB_L		4	100.0000		8 MIL SPACING			12 18
AGP CONTROL	AGP_FRAME_L			250.0000					12 18
	AGP_IRDY_L			250.0000					12 18
	AGP_TRDY_L		6	250.0000					12 18
	AGP_DEVSEL_L			250.0000					12 18
	AGP_STOP_L		6	250.0000					12 18
	AGP_PAR		6	250.0000					12 18
	AGP_REQ_L			285.0000					12 18
	AGP_GNT_L			250.0000					12 18
	AGP_RBF_L			250.0000					12 18
DVO	GPU_DVOD<0..11>		5	250					19 20
	GPU_DVO_HSYNC								19 20
	GPU_DVO_VSYNC								19 20
PCI	PCI_AD<31..0>					MIN_DAISY_CHAIN		33 MHz	9 12 17 24 26 39
	PCI_CBE<3..0>					MIN_DAISY_CHAIN		33 MHz	12 17 24 26 39
	PCI_FRAME_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_IRDY_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_TRDY_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_DEVSEL_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_STOP_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_PAR					MIN_DAISY_CHAIN			12 17 24 26 39
ULTRA ATA-100	UIDE_DATA<15..8>			NEED TO MATCH DELAY TO 250	200			100 MHz	13 24
	UIDE_DATA<7>				200				13 24
	UIDE_DATA<6..0>				200			100 MHz	13 24
	UIDE_ADDR<2..0>				200			100 MHz	13 24
	UIDE_RST_L				200.0000				13 24
	UIDE_DIOW_L				200.0000				13 24
	UIDE_DIOR_L			10 MIL SPACING	200.0000				13 24
	UIDE_DMACK_L				200.0000				13 24
	UIDE_CS0_L				200.0000				13 24
	UIDE_CS1_L				200.0000				13 24
	UIDE_DMARQ				200.0000				13
	UIDE_IOCHRDY			10 MIL SPACING	200.0000				13 24
	UIDE_INTRQ				200.0000				13
	HD_DATA<15..0>		5	TOTAL UIDE+HD SKEW <500MIL	200			100 MHz	24
	HD_ADDR<2..0>		5		200			100 MHz	24
	HD_RESET_L		5		200.0000				24
	HD_DIOW_L		5		200.0000				24
	HD_DIOR_L		5	10 MIL SPACING	200.0000				24
	HD_DMACK_L		5		200.0000				24
	HD_CS0_L		5		200.0000				24
	HD_CS1_L		5		200.0000				24
	HD_DMARQ				200.0000				13 24
	HD_IOCHRDY		5	10 MIL SPACING	200.0000				24
	HD_INTRQ		5						13 24
EIDE INTREPID	EIDE_DATA<15..0>							33 MHZ	13 24
	EIDE_ADDR<2..0>							33 MHZ	13 24
	EIDE_CS0_L								13 24
	EIDE_CS1_L								13 24
	EIDE_RD_L								13 24
	EIDE_WR_L								13 24
	EIDE_IOCHRDY								13 24
	EIDE_INT								13 24
	EIDE_RST_L								13 24
	EIDE_DMACK_L								13 24
	EIDE_DMARQ								13 24
OPTICAL	EIDE_OPTICAL_DATA<15..0>							33 MHZ	24 39
	EIDE_OPTICAL_ADDR<2..0>							33 MHZ	24 39
	EIDE_OPTICAL_CS0_L								24 39
	EIDE_OPTICAL_CS1_L								24 39
	EIDE_OPTICAL_RD_L								24 39
	EIDE_OPTICAL_WR_L								24 39
	EIDE_OPTICAL_IOCHRDY								24 39
	EIDE_OPTICAL_INT								24 39
	EIDE_OPTICAL_RST_L								24 39
	EIDE_OPTICAL_DMAACK_L								24 39
	EIDE_OPTICAL_DMA_RQ								24 39
ETHERNET MII	ENET_LINK_RXD<7..0>		5						13 27
	ENET_RX_DV								13 27
	ENET_RX_ER								13 27
	ENET_PHY_TXD<7..0>		5						13 27
	ENET_LINK_TXD<7..0>								13
	ENET_PHY_TX_ER		5						13 27
	ENET_LINK_TX_ER								13
	ENET_PHY_TX_EN		5						13 27
	ENET_LINK_TX_EN								13
	ENET_MDIO								13 27
	ENET_MDC								13 27
	ENET_COL								13 27
	ENET_CRS								13 27
FIREWIRE MII	FW_LINK_DATA<7..0>		5						13 28
	FW_PHY_DATA<7..0>		5						28
	FW_LINK_CNTL<1..0>								13 28
	FW_PHY_CNTL<1..0>								28
	FW_LINK_LREQ								13
	FW_PHY_LREQ								13 28
	FW_PINT								13 28

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR	MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS	
ETHERNET	MDI_M<0>	ENET_MDI0				27
	MDI_P<0>	ENET_MDI0				27
	MDI_M<1>	ENET_MDI1	SPACING DELETED BECAUSE			27
	MDI_P<1>	ENET_MDI1	OF PHYSICAL CONSTRAINTS			27
	MDI_M<2>	ENET_MDI2	AROUND MARVELL PHY			27
	MDI_P<2>	ENET_MDI2				27
	MDI_M<3>	ENET_MDI3				27
	MDI_P<3>	ENET_MDI3				27
	RJ45_DN<0>	RJ45_DP0		10 MIL SPACING		27 39
	RJ45_DP<0>	RJ45_DP0		10 MIL SPACING		27 39
	RJ45_DN<1>	RJ45_DP1		10 MIL SPACING		27 39
	RJ45_DP<1>	RJ45_DP1		10 MIL SPACING		27 39
	RJ45_DN<2>	RJ45_DP2		10 MIL SPACING		27 39
	RJ45_DP<2>	RJ45_DP2		10 MIL SPACING		27 39
	RJ45_DN<3>	RJ45_DP3		10 MIL SPACING		27 39
	RJ45_DP<3>	RJ45_DP3		10 MIL SPACING		27 39
FIREWIRE	FW_TPA0N	FW_TPA0		MIN LINE WIDTH=3.4		
	FW_TPA0P	FW_TPA0		10 MIL SPACING MIN LINE WIDTH=3.4		28 29
	FW_TPB0N	FW_TPB0		10 MIL SPACING MIN LINE WIDTH=3.4		28 29
	FW_TPB0P	FW_TPB0		10 MIL SPACING MIN LINE WIDTH=3.4		28 29
	FW_TPI0N	FW_TPI0		10 MIL SPACING MIN LINE WIDTH=3.4		
	FW_TPI0P	FW_TPI0		10 MIL SPACING MIN LINE WIDTH=3.4		
	FW_TPO0N	FW_TPO0		10 MIL SPACING MIN LINE WIDTH=3.4		
	FW_TPO0P	FW_TPO0		10 MIL SPACING MIN LINE WIDTH=3.4		
	FW_TPA1N	FW_TPA1	500.0000	10 MIL SPACING MIN LINE WIDTH=3.4		28 29
	FW_TPA1P	FW_TPA1	500.0000	10 MIL SPACING MIN LINE WIDTH=3.4		28 29
	FW_TPB1N	FW_TPB1	500.0000	10 MIL SPACING MIN LINE WIDTH=3.4		28 29
	FW_TPB1P	FW_TPB1	500.0000	10 MIL SPACING MIN LINE WIDTH=3.4		28 29
	FW_TPI1N	FW_TPI1		10 MIL SPACING MIN LINE WIDTH=3.4		29 39
	FW_TPI1P	FW_TPI1		10 MIL SPACING MIN LINE WIDTH=3.4		29 39
	FW_TPO1N	FW_TPO1		10 MIL SPACING MIN LINE WIDTH=3.4		29 39
	FW_TPO1P	FW_TPO1		10 MIL SPACING		29 39
LVDS LOWER	CLKLVDS_LN	CLKLVDS_L		10 MIL SPACING	4	19 22 39
	CLKLVDS_LP	CLKLVDS_L		10 MIL SPACING	4	19 22 39
	LVDS_L0N	LVDS_L0		10 MIL SPACING		19 22 39
	LVDS_L0P	LVDS_L0		10 MIL SPACING		19 22 39
	LVDS_L1N	LVDS_L1		10 MIL SPACING		19 22 39
	LVDS_L1P	LVDS_L1		10 MIL SPACING		19 22 39
	LVDS_L2N	LVDS_L2		10 MIL SPACING		19 22 39
	LVDS_L2P	LVDS_L2		10 MIL SPACING		19 22 39
UPPER	CLKLVDS_UN	CLKLVDS_U		10 MIL SPACING	4	19 22 39
	CLKLVDS_UP	CLKLVDS_U		10 MIL SPACING	4	19 22 39
	LVDS_U0N	LVDS_U0		10 MIL SPACING		19 22 39
	LVDS_U0P	LVDS_U0		10 MIL SPACING		19 22 39
	LVDS_U1N	LVDS_U1		10 MIL SPACING		19 22 39
	LVDS_U1P	LVDS_U1		10 MIL SPACING		19 22 39
	LVDS_U2N	LVDS_U2		10 MIL SPACING		19 22 39
	LVDS_U2P	LVDS_U2		10 MIL SPACING		19 22 39
TMDS	TMDS_CONN_CLKN	CLKCONN_TMDS		10 MIL SPACING	4	22 39
	TMDS_CONN_CLKP	CLKCONN_TMDS		10 MIL SPACING	4	22 39
	TMDS_CLKN	CLKTMDS		10 MIL SPACING	4	20 22
	TMDS_CLKP	CLKTMDS		10 MIL SPACING	4	20 22
	TMDS_DN<0>	TMDS_D0		10 MIL SPACING		20 22 39
	TMDS_DP<0>	TMDS_D0		10 MIL SPACING		20 22 39
	TMDS_DN<1>	TMDS_D1		10 MIL SPACING		20 22 39
	TMDS_DP<1>	TMDS_D1		10 MIL SPACING		20 22 39
	TMDS_DN<2>	TMDS_D2		10 MIL SPACING		20 22 39
	TMDS_DP<2>	TMDS_D2		10 MIL SPACING		20 22 39
USB	NEC_USB_DAM	NEC_USB_DA	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_DAP	NEC_USB_DA	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	USB_DEM	USB_DE		5 MIL SPACING		14
	USB_DEP	USB_DE		5 MIL SPACING		14
	NEC_USB_DBM	NEC_USB_DB	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_DBP	NEC_USB_DB	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	USB_DFM	USB_DF		5 MIL SPACING		14
	USB_DFP	USB_DF		5 MIL SPACING		14
	BT_USB_DM	BT_USB_D		5 MIL SPACING		14 24 39
	BT_USB_DP	BT_USB_D		5 MIL SPACING		14 24 39
	NEC_USB_RSDM1	NEC_USB_RSD1	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_RSDP1	NEC_USB_RSD1	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_RSDM2	NEC_USB_RSD2	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_RSDP2	NEC_USB_RSD2	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	MODEM_USB_DM	MODEM_USB_D		5 MIL SPACING		14 25 39
	MODEM_USB_DP	MODEM_USB_D		5 MIL SPACING		14 25 39
	LEFT_USB_DM	LEFT_USB	MIN_LINE_WIDTH=5	10 MIL SPACING		24 26 39
	LEFT_USB_DP	LEFT_USB	MIN_LINE_WIDTH=5	10 MIL SPACING		24 26 39
	RIGHT_USB_DM	RIGHT_USB	MIN_LINE_WIDTH=5	10 MIL SPACING		26 32 39
	RIGHT_USB_DP	RIGHT_USB	MIN_LINE_WIDTH=5	10 MIL SPACING		26 32 39
POWER SUPPLIES	1772_CSSN	1772_CSS				31
	1772_CSSP	1772_CSS				31
	1772_CSIN	1772_CSI				31
	1772_CSIP	1772_CSI				31
	3V_SNSM	3V_SNS				33
	3V_SNSP	3V_SNS				33
	5V_SNSM	5V_SNS				33
	5V_SNSP	5V_SNS				33
THERMOSTAT	THERM1_DM	THERM1				25
	THERM1_DP	THERM1				25
	THERM2_DM	THERM2				25
	THERM2_DP	THERM2				25
	THERM1_M_DM	THERM1_MAIN				
	THERM1_M_DP	THERM1_MAIN				
	THERM2_M_DM	THERM2_MAIN				
	THERM2_M_DP	THERM2_MAIN				
	THERM1_A_DM	THERM1_ALT				25
	THERM1_A_DP	THERM1_ALT				25
	THERM2_A_DM	THERM2_ALT				25
	THERM2_A_DP	THERM2_ALT				25

INTERNAL LAYER

ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.57OHM
ZDIFF = 99.80HM

FOR FIREWIRE

ER = 4.3 (DIELECTRIC CONSTANT)
W = 3.4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 53.37OHM
ZDIFF = 107.17OHM

INTERNAL LAYER (USB1.1/USB 2.0)

ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL(USB 1.1)/ 5MIL(USB 2.0) (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 5MIL (USB 1.1) (SEPERATION OF DIFF TRACES)
S = 10MIL (USB 2.0) (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.5OHM (USB 1.1)/ 46.2OHM (USB 2.0)
ZDIFF = 89.3OHM (USB 1.1)/ 89.4OHM (USB 2.0)

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POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
MAIN/SLEEP	+24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+BATT	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	
	+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+2_5V_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	39
	+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	35
	+1_5V_SLEEP_VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	35
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31 32
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31 39
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31 39
	1772_DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	1772_LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	31
	1772_LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		31
	1772_DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		31
	1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10		31
PMU	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	+4_85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		30 32
	+4_6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10		32 33
	+4_85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		32
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		32
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		25 30
MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24 33
	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24
TRACKPAD	+5V_TPAD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=10		23 39
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		23 39
VIDEO	+12_8V_INV	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	22
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
KB LED	KBD_LED1_OUT	VOLTAGE=0V	MIN_LINE_WIDTH=10		23 39
	KBD_LED2_OUT	VOLTAGE=0V	MIN_LINE_WIDTH=10		23 39
FAN GND	FANL_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 39
	FANR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 39
SOUND	+5V_SOUND_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	SND_AGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=15	25

		VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	GND
I/O AREA		VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND1
	CHGND1				
INVERTER		VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND2
	CHGND2				
TRACKPAD		VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND3
	CHGND3				
LVDS		VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND4 39
	CHGND4				
I/O AREA		VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND5
	CHGND5				
I/O AREA		VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND6
	CHGND6				
ENET_CTAP_CHGND		VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	27

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 34 39
	CPU_AVDD	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
DDR RAM	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 7 8 15 16 23 34
	DDR_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		11
INTREPID	+2_5V_INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	9 10 15 16
	+3V_INTREPID_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14
PLLS	+1_5V_INTREPID_PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	8 12 14
	+1_5V_INTREPID_PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5	14
	+1_5V_INTREPID_PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5	12
	+1_5V_INTREPID_PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	8
	+1_5V_INTREPID_PLL8	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
REFERENCE	INT_MEM_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		9
	INT_AGP_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		12 18
	INT_MEM_REF_H	VOLTAGE=0V	MIN_LINE_WIDTH=10		9
	UIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8		13
CARDBUS	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	MIN_NECK_WIDTH REDUCED FOR TESTPOINTS 17
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
ATI M10	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	18 19 39
	+GPU_MEM	VOLTAGE=2.5V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	18 21
	+3V_GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 18 19 21
	+3V_GPU_FLT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	21
	+1_5V_AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 15 16 18 19 21
	GPU_MEM_IO	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	GPU_MEM_IO_FLT	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+GPU_MEMCORE	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+1_8V_GPU	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18 19 20 21
	+2_5V_GPU_PNLIO	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_8V_ATI_PVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19 21
	+1_5V_AGP_GPU	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_5V_GPU_VDD15	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	+1_8V_GPU_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1331	+1_8V_GPU_VDDDI	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1332	GPU_VCORE_VDDCI	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	18
1333	+2_5V_GPU_A2VDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1334	+1_8V_GPU_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1335	+1_8V_GPU_PNLPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1336	+1_8V_GPU_PNLIO	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1337	+GPU_MCLK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1338	+1_8V_GPU_AVDDQ	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1341	+1_8V_GPU_MEMPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1342	+3V_ATI_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	18
1339	+3V_ATI_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	18
1340	+GPU_VDD15_UF	VOLTAGE=1.5V	MIN_LINE_WIDTH=20		19
1343	+2_5V_SLEEP_NECK1	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		19
1344	+3V_SLEEP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		21
1345	+1_5V_AGP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		19
1346	+1_8V_PVDD_NECK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10		19
1347	GPU_VCORE_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		19
1348	+GPU_VDD15_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		19
1351	+2_5V_SLEEP_NECK2	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		21
1349	+1_8V_SLEEP_NECK	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		21
1350	+1_5V_SLEEP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		21
1352	+2_5V_GPU	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
SILICON IMIAGE	+3V_SI_PLLVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	20
	+3V_SI_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	20
	+3V_SI_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	20
88E1111	+2_5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+2_5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
	+1_0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
	LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
	LM2594_IN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
FW	+3V_FW_ESD_ILIM	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+3V_FW_ESD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+FW_FUSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_PWR_OR	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28 29
	+FW_VP0	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_PWR_PORTA	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_VP1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+3V_FW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28 29
	+3V_FW_UF	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	28
	+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	FW_TPO0R	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29 39
USB 2.0	NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
INTREPID SSCG	+3V_CG_PLL_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	14
	+2_5V_CG_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	14

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	1625_VSW	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		32
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		32
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		32
	1V20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	31 32
LTC3707 5V SWITCHER	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	33
	5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
3V SWITCHER	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		33
MAX1715 2.5V SWITCHER	2_5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	35
	2_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	2_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	2_5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	2_5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
1.5V SWITCHER	1_5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8		35
	1_5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	35
	1_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	1_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	1_5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	1_5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
CONTROL	1_5V_ILIM		MIN_LINE_WIDTH=8		35
	2_5V_ILIM		MIN_LINE_WIDTH=8		35
	MAX1715_TON		MIN_LINE_WIDTH=8		35
	MAX1715_SKIP		MIN_LINE_WIDTH=8		35
	MAX1715_REF	VOLTAGE=2.0V	MIN_LINE_WIDTH=8		35
	MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	35
MAX1717	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=200	MIN_NECK_WIDTH=10	34
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	VCORE_ILIM		MIN_LINE_WIDTH=8		34
	VCORE_REF		MIN_LINE_WIDTH=8		34
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8		34
	VCORE_CC		MIN_LINE_WIDTH=8		34
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		34 39
	VCORE_TIME		MIN_LINE_WIDTH=8		34
	VCORE_VGATE		MIN_LINE_WIDTH=8		14 34
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30		34
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8		34
	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		34
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8		34
LTC1778	1778_VIN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	19
	1778_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	1778_BST_RC	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	1778_TG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_BG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	GPU_VCORE_SW	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	19
	1778_ION		MIN_LINE_WIDTH=8		19
	1778_ITH		MIN_LINE_WIDTH=8		19
	1778_ITH_RC		MIN_LINE_WIDTH=8		19
	1_5V_2_5V_OK		MIN_LINE_WIDTH=8		35
	1778_VFB		MIN_LINE_WIDTH=8		19 39
	1778_FCB		MIN_LINE_WIDTH=8		19
	1778_VRNG		MIN_LINE_WIDTH=8		19
LTC3411	LTC3411_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC3411_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	
	1_8V_SW	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	35
	1_8V_VFB		MIN_LINE_WIDTH=8		
	LTC3411_ITH_RC		MIN_LINE_WIDTH=8		
	LTC3411_ITH		MIN_LINE_WIDTH=8		
	LTC3411_SYNC		MIN_LINE_WIDTH=8		
	LTC3411_SHDN		MIN_LINE_WIDTH=8		
LTC1962 INT PLLS	LTC1962_INT_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	14
	LTC1962_L3_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_L3_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_1V5_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_1V5_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	

SIGNAL CONSTRAINTS - PAGE 3

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 38 OF 44	

FUNCTIONAL TEST POINTS

FUNC_TEST=YES JTAG_ASIC_TMS 13 27
FUNC_TEST=YES JTAG_ASIC_TDI 13
FUNC_TEST=YES JTAG_ASIC_TDO_TP 27
FUNC_TEST=YES JTAG_ASIC_TCK 13 27
FUNC_TEST=YES JTAG_ASIC_TRST_L 13 27
FUNC_TEST=YES CPU_CHKSTP_OUT_L 5
FUNC_TEST=YES CPU_SRESET_L 5
FUNC_TEST=YES CPU_HRESET_L 5 7 23
FUNC_TEST=YES JTAG_CPU_TMS 5 23
FUNC_TEST=YES JTAG_CPU_TDI 5 23
FUNC_TEST=YES JTAG_CPU_TDO_TP 5
FUNC_TEST=YES JTAG_CPU_TCK 5 23
FUNC_TEST=YES JTAG_CPU_TRST_L 5 23 39

FUNC_TEST=YES INT_I2C_CLK0 11 13 23
FUNC_TEST=YES INT_I2C_DATA0 11 13 23
FUNC_TEST=YES INT_I2C_CLK1 13 14 25
FUNC_TEST=YES INT_I2C_DATA1 13 14 25
FUNC_TEST=YES CBUS_DET_1_L 17
FUNC_TEST=YES CBUS_DET_2_L 17
FUNC_TEST=YES TMDS_DN<0> 20 22 37
FUNC_TEST=YES TMDS_DP<0> 20 22 37
FUNC_TEST=YES TMDS_DN<1> 20 22 37
FUNC_TEST=YES TMDS_DP<1> 20 22 37
FUNC_TEST=YES TMDS_DN<2> 20 22 37
FUNC_TEST=YES TMDS_DP<2> 20 22 37
FUNC_TEST=YES TMDS_CONN_CLKN 22 37

FUNC_TEST=YES TMDS_CONN_CLKP 22 37
FUNC_TEST=YES VGA_R 22
FUNC_TEST=YES VGA_G 22
FUNC_TEST=YES VGA_B 22
FUNC_TEST=YES VGA_VSYNC 22
FUNC_TEST=YES VGA_HSYNC 22
FUNC_TEST=YES DVI_DDC_CLK_UF 22
FUNC_TEST=YES DVI_DDC_DATA_UF 22
FUNC_TEST=YES DVI_HPD_UF 22
FUNC_TEST=YES LVDS_L0N 19 22 37
FUNC_TEST=YES LVDS_L0P 19 22 37
FUNC_TEST=YES LVDS_L1N 19 22 37
FUNC_TEST=YES LVDS_L1P 19 22 37
FUNC_TEST=YES LVDS_L2N 19 22 37
FUNC_TEST=YES LVDS_L2P 19 22 37
FUNC_TEST=YES CLKLVDS_LN 19 22 37
FUNC_TEST=YES CLKLVDS_LP 19 22 37
FUNC_TEST=YES LVDS_U0N 19 22 37
FUNC_TEST=YES LVDS_U0P 19 22 37
FUNC_TEST=YES LVDS_U1N 19 22 37
FUNC_TEST=YES LVDS_U1P 19 22 37
FUNC_TEST=YES LVDS_U2N 19 22 37
FUNC_TEST=YES LVDS_U2P 19 22 37
FUNC_TEST=YES CLKLVDS_UN 19 22 37
FUNC_TEST=YES CLKLVDS_UP 19 22 37
FUNC_TEST=YES LVDS_DDC_CLK 19 22
FUNC_TEST=YES LVDS_DDC_DATA 19 22
FUNC_TEST=YES BRIGHT_PWM 22
FUNC_TEST=YES TV_GND1 22 38
FUNC_TEST=YES TV_GND2 22 38

FUNC_TEST=YES TV_C 22
FUNC_TEST=YES TV_Y 22
FUNC_TEST=YES TV_COMP 22
FUNC_TEST=YES SND_TO_AUDIO 14 25
FUNC_TEST=YES SND_SYNC 14 25
FUNC_TEST=YES SND_CLKOUT 14 25 36

FUNC_TEST=YES INT_AUDIO_TO_SND 14 25
FUNC_TEST=YES SND_SCLK 14 25 36
FUNC_TEST=YES SND_HW_RESET_L 14 25
FUNC_TEST=YES SND_HP_SENSE_L 14 25
FUNC_TEST=YES SND_LIN_SENSE_L 14 25
FUNC_TEST=YES INT_I2C_DATA2 14 25
FUNC_TEST=YES INT_I2C_CLK2 14 25
FUNC_TEST=YES CHGND4 38
FUNC_TEST=YES SLEEP_LED 23 25

FUNC_TEST=YES BT_USB_DM 14 24 37
FUNC_TEST=YES BT_USB_DP 14 24 37
FUNC_TEST=YES MODEM_USB_DM 14 25 37
FUNC_TEST=YES MODEM_USB_DP 14 25 37
FUNC_TEST=YES PCI_AD<0> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<1> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<2> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<3> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<4> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<5> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<6> 9 12 17 24 26 37

FUNC_TEST=YES PCI_AD<7> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<8> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<9> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<10> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<11> 9 12 17 24 26 37
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FUNC_TEST=YES PCI_AD<20> 9 12 17 24 26 37
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FUNC_TEST=YES PCI_AD<23> 12 17 24 26 37
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FUNC_TEST=YES PCI_AD<25> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<26> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<27> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<28> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<29> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<30> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<31> 9 12 17 24 26 37
FUNC_TEST=YES PCI_FRAME_L 12 17 24 26 37
FUNC_TEST=YES PCI_TRDY_L 12 17 24 26 37
FUNC_TEST=YES PCI_IRDY_L 12 17 24 26 37
FUNC_TEST=YES PCI_DEVSEL_L 12 17 24 26 37
FUNC_TEST=YES PCI_STOP_L 12 17 24 26 37

FUNC_TEST=YES PCI_PAR 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<0> 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<1> 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<2> 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<3> 12 17 24 26 37
FUNC_TEST=YES AIRPORT_PCI_REQ_L 12 24
FUNC_TEST=YES AIRPORT_PCI_GNT_L 12 24
FUNC_TEST=YES AIRPORT_PCI_INT_L 14 24
FUNC_TEST=YES EIDE_OPTICAL_DATA<0> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<1> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<2> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<3> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<4> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<5> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<6> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<7> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<8> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<9> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<10> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<11> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<12> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<13> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<14> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<15> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DMA_RQ 24 37
FUNC_TEST=YES EIDE_OPTICAL_RD_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_DMAACK_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_ADDR<0> 24 37
FUNC_TEST=YES EIDE_OPTICAL_ADDR<1> 24 37
FUNC_TEST=YES EIDE_OPTICAL_ADDR<2> 24 37
FUNC_TEST=YES SND_AMP_MUTE 25
FUNC_TEST=YES SND_HP_MUTE_INV 25

FUNC_TEST=YES EIDE_OPTICAL_CS0_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_CS1_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_RST_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_WR_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_IOCHRDY 24 37
FUNC_TEST=YES EIDE_OPTICAL_INT 24 37
FUNC_TEST=YES TPAD_F_TXD 23
FUNC_TEST=YES TPAD_F_RXD 23
FUNC_TEST=YES LID_CLOSED_L 23
FUNC_TEST=YES COMM_RESET_L 14 25
FUNC_TEST=YES COMM_SHUTDOWN 14 25
FUNC_TEST=YES COMM_RING_DET_L 14 25 30
FUNC_TEST=YES KBD_ID 23 30
FUNC_TEST=YES +5V_TPAD_SLEEP 23 38
FUNC_TEST=YES +3V_HALL_EFFECT 23 38
FUNC_TEST=YES KBD_CAPSLOCK_LED 23
FUNC_TEST=YES KBD_FUNCTION_L 23 30
FUNC_TEST=YES KBD_CONTROL_L 23 30
FUNC_TEST=YES KBD_COMMAND_L 23 30
FUNC_TEST=YES KBD_OPTION_L 23 30
FUNC_TEST=YES KBD_SHIFT_L 23 30
FUNC_TEST=YES KBD_X<0> 23 30
FUNC_TEST=YES KBD_X<1> 23 30
FUNC_TEST=YES KBD_X<2> 23 30
FUNC_TEST=YES KBD_X<3> 23 30
FUNC_TEST=YES KBD_X<4> 23 30
FUNC_TEST=YES KBD_X<5> 23 30
FUNC_TEST=YES KBD_X<6> 23 30
FUNC_TEST=YES KBD_X<7> 23 30
FUNC_TEST=YES KBD_X<8> 23 30
FUNC_TEST=YES SRCLK_TP 26
FUNC_TEST=YES SRMOD_TP 26
FUNC_TEST=YES TEB_TP 26
FUNC_TEST=YES TEST_TP 26

FUNC_TEST=YES KBD_X<9> 23 30
FUNC_TEST=YES KBD_Y<0> 23 30
FUNC_TEST=YES KBD_Y<1> 23 30
FUNC_TEST=YES KBD_Y<2> 23 30
FUNC_TEST=YES KBD_Y<3> 23 30
FUNC_TEST=YES KBD_Y<4> 23 30
FUNC_TEST=YES KBD_Y<5> 23 30
FUNC_TEST=YES KBD_Y<6> 23 30
FUNC_TEST=YES KBD_Y<7> 23 30
FUNC_TEST=YES KBD_NUMLOCK_LED 23
FUNC_TEST=YES +BATT_POS 31 38
FUNC_TEST=YES BATT_CLK 31
FUNC_TEST=YES BATT_DATA 31
FUNC_TEST=YES BATT_NEG 31 38
FUNC_TEST=YES PMU_BATT_DET_L 30 31
FUNC_TEST=YES FANR_GND 25 38
FUNC_TEST=YES FANL_GND 25 38
FUNC_TEST=YES FANL_TACH 25
FUNC_TEST=YES FANR_PWM 25
FUNC_TEST=YES FANL_PWM 25
FUNC_TEST=YES RJ45_DP<0> 27 37
FUNC_TEST=YES RJ45_DN<0> 27 37
FUNC_TEST=YES RJ45_DP<1> 27 37
FUNC_TEST=YES RJ45_DN<1> 27 37
FUNC_TEST=YES RJ45_DP<2> 27 37
FUNC_TEST=YES RJ45_DN<2> 27 37
FUNC_TEST=YES RJ45_DP<3> 27 37
FUNC_TEST=YES RJ45_DN<3> 27 37
FUNC_TEST=YES FW_TPOOR 29 38
FUNC_TEST=YES VCORE_VID0
FUNC_TEST=YES VCORE_VID1
FUNC_TEST=YES VCORE_VID2
FUNC_TEST=YES VCORE_VID3
FUNC_TEST=YES VCORE_VID4

FUNC_TEST=YES FW_TPO1P 29 37
FUNC_TEST=YES FW_TPO1N 29 37
FUNC_TEST=YES FW_TPI1P 29 37
FUNC_TEST=YES FW_TPI1N 29 37
FUNC_TEST=YES CHARGE_LED_L 30 31
FUNC_TEST=YES ADAPTER_DET 30 31
FUNC_TEST=YES SUTRO_ALS_GAIN_SW 23 24
FUNC_TEST=YES SUTRO_ALS_OUT 23 24
FUNC_TEST=YES KBD_LED1_OUT 23 38
FUNC_TEST=YES KBD_LED2_OUT 23 38
FUNC_TEST=YES COMM_TXD_L 14 25
FUNC_TEST=YES COMM_TRXC 14 25
FUNC_TEST=YES COMM_GPIO_L 14 25
FUNC_TEST=YES COMM_DTR_L 14 25
FUNC_TEST=YES COMM_RTS_L 14 25
FUNC_TEST=YES COMM_RXD 14 25
FUNC_TEST=YES PMU_KB_RESET_L 30
FUNC_TEST=YES PWR_BUTTON_L 23 25
FUNC_TEST=YES +PBUS 38
FUNC_TEST=YES +24V_PBUS 38
FUNC_TEST=YES GPU_VCORE 18 19 38
FUNC_TEST=YES CPU_VCORE_SLEEP 5 34 38
FUNC_TEST=YES VCORE_FB 34 38
FUNC_TEST=YES +1_8V_MAIN 38
FUNC_TEST=YES +3V_PMU 38
FUNC_TEST=YES +5V_DDC_SLEEP 22 38
FUNC_TEST=YES +12_8V_INV 22 38
FUNC_TEST=YES VCORE_MUX_EN 34

FUNC_TEST=YES +5V_INV_SW 22 38
FUNC_TEST=YES LEFT_USB_DM 24 26 37
FUNC_TEST=YES LEFT_USB_DP 24 26 37
FUNC_TEST=YES RIGHT_USB_DM 26 32 37
FUNC_TEST=YES RIGHT_USB_DP 26 32 37
FUNC_TEST=YES NEC_LEFT_USB_PWREN 24 26
FUNC_TEST=YES NEC_LEFT_USB_OVERCURRENT 24 26
FUNC_TEST=YES NEC_RIGHT_USB_PWREN 26 32
FUNC_TEST=YES NEC_RIGHT_USB_OVERCURRENT 26 32
FUNC_TEST=YES DCDC_EN 19 29 32 33 34
FUNC_TEST=YES BBANG_HRESET_L 23
FUNC_TEST=YES MAIN_RESET_L 14 17 18 20 24 26 30
FUNC_TEST=YES RF_DISABLE_L_SPN 24
FUNC_TEST=YES AIRPORT_CLKRUN_L 24
FUNC_TEST=YES ROM_RW_L 9 12 24
FUNC_TEST=YES ROM_ONBOARD_CS_L 9 24
FUNC_TEST=YES ROM_CS_L 9 12 24
FUNC_TEST=YES CLK33M_AIRPORT 12 24 36
FUNC_TEST=YES AIRPORT_IDSEL 24
FUNC_TEST=YES ROM_OE_L 9 12 24
FUNC_TEST=YES INT_MOD_DTI 14 25
FUNC_TEST=YES JTAG_CPU_TRST_L 5 23 39
FUNC_TEST=YES MOD_BITCLK 14 25
FUNC_TEST=YES MOD_CLKOUT 14 25
FUNC_TEST=YES MOD_DTO 14 25
FUNC_TEST=YES MOD_SYNC 14 25
FUNC_TEST=YES SLEEP 23 25 30 33 35
FUNC_TEST=YES 1778_VFB 19 38

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 39 OF 44	

REVISION HISTORY

REV 0.01 - 03/06/2003

3/3
1) Initial check-in of Enterprise schematic after conversion to Concept 14.2

3/10
2) added 8 new 10uF vcore caps
3) added jumpers at 1.5V, 1.8V, 2.5V, 3.3V, 5V, and PBUS supply outputs
4) added 8 more 0.1uF vcore byapass caps

3/11
5) removed dedicated boot banger circuit (U5400,U5200,RP46,U9,U1000)
6) updated firewire to phy to rev A prt number
7) changed cpu PLL config to 1083/833
8) changed reset to U56 (clock slewing chip) to MAIN_RESET_L
9) changed C550 to 138S0536 to limit AVL
10) changed Vcore stuffing options to 1.4V/1.025V using analog mux to support slewing
11) changed stuffing to set Vcore offset to 0mV by default
12) changed comments to eliminate references to L3 in power supply section

3/18
13) changed stuffing options for GPU PCI ID to 0x319
14) changed R164 (DAC1RSET) to 107 ohm pulldown
15) added 10K pulldown to U43 pin A21
16) changed fan controller to ADT7460

3/19
17) added pads for 0.1uF cap from +Adapter to digital gnd for EMC
18) added pads for 0 ohm between chassis and digital gnd near ENET connector for EMC
19) corrected path to correct for last checkin
20) removed BOM table for MAP31
21) REMOVED ALL RELATIVE_PROPAGATION_DELAY AND PROPAGATION_DELAY PROPERTIES TO PRERPARE FOR CONSTRAINT BACK ANNOTATION
22) changed CHGND on R616 to CHGND1
23) ***BOARD RENUMBERED***

3/28
24) integrated M10 pages from Q16 schematic and renumbered them

4/10
25) updated physical constraints for M10 power nets
26) added DP7 for M10 power sequencing
27) added RP27,RP28,RP32, and RP57 for TMDS series termination
28) update PLL CFG high 0010 1.25GHz
low 1011 833MHz
29) update sscg/nosscg stuffing option on intrepid boot straps
30) removed D31 between +Batt and 24V_Pbus
31) add Vcore DAC resistors (R288,R289,R290,R292) for no mux case
32) change intrepid PLL LDO stuffing back to 1.8V main
33) change C640 and C646 to 0.01uF (Apple # 132S1047) for FW check config
34) change I2C pullups (R29 and R102) to 1K
35) changed bootrom part number to 341S1255

4/18
36) changed C756 to 128S0025 (Sanyo only 6.3V 330uF)
37) add pads for 90 ohm chokes to FWB path close to connector (route through the pads)
38) changed Vcore inductor (L36) to molded core part (152S0125)
39) changed Pbus inductor (L37) to molded core part (152S0126)
40) added seperate 1_8V_GPU_TPVDD filter and LDO (U54)

4/21
41) replace disctrete LCL with single chip LCL filters (155S0154) for VGA (L ,L , and L)
42) add 165 ohm chokes on TMDS data pairs at connector (L ,L , and L)
43) move BS1 to bottom side
44) move CPU thermal sensor (Q39) to input 1 on fan controller and power supply sensor (Q66) to input 2
45) added trace from Vcore to fan controller ADC input
46) added FET inverters (Q78) to PWM outputs of fan controller (U3) to prevent spinup at boot
47) added FET (Q79) for +3V_Sleep for M10 power sequencing

4/27
48) changed TMDS data chokes to 90 ohm (155S0128)
49) changed C762 and C766 to 4.7uF 1206 caps
50) changed TMDS data chokes to 90 ohms (155S0128)
51) changed C762 and C766 to 4.7uF 1206
52) changed Q51 to Si7860DP (376S0119)
53) changed Q48 to Si7892DP (376S0120)
54) changed D24 to B340LB (371S0132)
55) changed L30 to 2.2uH Tokin inductor (152S0139)
56) added Q58, R307, and C515 for GPU Vcore control inverter
57) changed R416 to 2.2ohms
58) changed R364 to 102K
59) added 0.1uF 50V C883 to RS- of Max4172 (NO stuff)
60) changed D18 to 1N914
61) changed L38 and L41 to 4.7uH (152S0137)
62) added Q81, R308, R309, and R310 for power sequencing (no stuff)
63) changed Q49 and Q50 to Si7860DP (376S0119)
64) changed L36 to 1.2uH 18.3A (152S0125)
65) added R331 1mohm sense resistor to CPU Vcore
66) added C885 and C884 , 1000uF CPU Vcore outpur caps
67) added Q82, R607, R455, R417, and C886 for 1.5V sleep sequencing
68) added Q83 and 100K R608 for 1.8V sequencing
69) added 15.4K R616 and 10K R672 for 2.5V switcher feedback divider
70) changed pinout of sound connector for sousaphone
71) removed Q44 (5V sound sleep fet)
72) changed Q31 to invert headphone Mute to sousaphone

4/28
73) changed CPU_VCORE_SLEEP location back to across bypass caps to correct after adding reference resistor
74) changed D5 to schottky diode (MBR0540)
75) fixed unnamed net (LTC3411_SHDN_SEQ)
76) changed drain/source polarity of Q76 (FET from +BATT to Pbus)

4/28
77) moved XW15 to connect to CPU_VCORE_SLEEP_UF (before positioning resistor)
78) changed Fan control nets to FanL and FanR from Fan1 and Fan2
79) SWAPPED CONNECTIONS SO THAT OUTPUT 1 FROM FAN CONTROLLER CONNECTS TO LEFT FAN (CPU) AND FAN 2 CONNECTS TO THE RIGHT FAN (GPU)
80) updated power constraints with new fan net names

4/28
81) change Q58 on pg19 to Q80 to consolidate parts
82) CHANGED U55 TO MM1571J FOR COST SAVINGS
83) changed L72,L73,L74 to 90 ohm ferrites
84) added 10K pullup to +5V_MAIN to SND_HP_MUTE
85) repinout Sousaphone connector
86) remore redundant pullups on FANL_TACH and FANR_TACH
87) added TP to all NC on NEC USB2 part for NAND tree testing
88) added NEC_USB bomoption to 0 ohm resistor on NEC_AVSS_F

4/30
89) repinout Sousaphone connector (J12)
90) no stuff R322 to eliminate 3V_sleep pump up
91) updated various text notes with correct reference designators

5/1
92) change L30 to 152S0139 (Tokin CPI-1050-2R2) 11A
93) remove FANR_TACH functional test point
94) add CHGND4 and SLEEP_LED functional test points
95) swap INT_AUDIO_TO_SND and SND_TO_AUDIO on Sousaphone connector (J12)

*** rev 01 released for EVT ***

5/6
96) remove NO STUFF on R477 (set 5V and 3.3V switcher in pulse skipping mode)
97) change R337 to 470K and remove No Stuff and no stuff R336 to change Vcore DAC to 1.35V/1.15V
98) change R321 to 499ohm to set 5mV Vcore offset
99) change L72,L73,L74 to 155S0165 (D part for EVT only)

*** rev 02 released for EVT ***

5/7
100) no stuff Q79 to disable 3V_SLEEP sequencing to work around wake from sleep bug with M10
101) added BOM table to define correct part number for M10 without heatspreader (338S0133)

*** rev 03 released for EVT ***

5/22
102) fixed NO STUFF BOM option for R291
103) add NO STUFF to R223 to correct startup level of GPU_VCORE_CNTL
104) add NO STUFF to R300 to complete 3V sequecing on wake from sleep fix
105) changed R376 to 158K and R321 to 2.74K to set CPU_VCORE offset to 35mV

*** rev 04 released for EVT ***

5/19/03
106) changed both AGP_NV_INT_L and AGP_ATI_INT_L to AGP_INT_L
107) removed redundant 3V_GPU pullup R687 (Intrepid side AGP_INT_L pullup)
108) added R699,R701,R707,R708 as 10k pulldowns to Intrepid USB ports A and C when NEC_USB is stuffed
109) changed SND_HP_MUTE_INV gate/inversion FETS to pullup to +3V_MAIN
110) added R711 as pullup to +3V_GPU on AUXWIN signal from M10 (U44)
111) added R698 as 0 ohm jumper between FW_PHY_PD and Intrepid
112) added U56, U57, R718,R714 for VGA Hsync and VGA Vsync buffering
113) changed L72,L73,L74 to 155S0164 (new high speed part)
114) added NO STUFF BOM option to R223 to correct for sense of GPU_VCORE_CNTL
115) added NO STUFF BOM option to R300 to avoid sleep wake problem

6/3/03
116) Intgrated new 1.8V switcher (LTC3412)(U58)(353S0650) and inductor (L75- 152S0142)
117) changed 2.5V_SLEEP FET (U48) and 1.8V_SLEEP FET (U6) to higher current part (Si6467BDQ - 376S0161)
118) added 10K pulldown (R720) on FW_PHY_PD_INT for when R698 is removed
119) changed R728 and R729 to 1210 0ohm resistors to support switching the entire memory bus between 1.8V and 2.5V
120) added R721 as jumper between +2_5V_SLEEP and +2_5V_GPU

6/4/03
121) NO STUFF R631 to remove MAIN_RESET_L from clock slewing chip
122) changed FWB connector to new part with extra ground tabs (514S0059)

6/5/03
123) changed I2C 0 and 1 pullups (RP12) to 2.2K to improve rise/fall times (sensor check config errors)
124) added CRITICAL flag to new 1.8V switcher (U58), inductor (L75), 1.8V sleep FET (U6), and 2.5V sleep FET (48)
125) removed gnd caps (C651 and C647) on I2S clock at sound connector (J12)
126) added LC filter on SND_SYNC for EMI (L77 and C895)
127) added LC filter on SND_CLKOUT for EMI (80 and C899)
128) added LC filter on INT_AUDIO_TO_SND for EMI (L81 and C896)
129) added LC filter on SND_TO_AUDIO for EMI (L82 and C897)
130) added LC filter on SND_AMP_MUTE for EMI (L76 and C898)
131) added LC filter on SND_HW_RESET_L for EMI (L78 and C900)
132) added LC filter on SND_SCLK for EMI (L79 and C901)
133) added C902 and R804 to prevent latch-up condition in GPU Vcore circuit when using powermiser
134) removed R331 (CPU Vcore positioning resistor)
135) changed C728,C729,C730,C731,C732,C733,C734,C884,C885 to 220uF Rubycon caps (128S0024)
136) add Vcore offset change circuit to modify offset in low (Q86,R805,R806,R807,R808,R809)
137) changed Q83 into dual (2N7002DW) and added R810 to invert 3V_5V_ON before switching RUN/SS

6/6/03
138) rotated J26 (FW B connector)
139) changed D29 to B340B (3A part - 371S0159)

6/9/03
140) modified Vcore offset select circuit with Takashi's changes - changed Gnd reference to VCORE_GND_SNS
141) added double inverter to buffer THERM_L_OC (added Q87,R811,R812)
142) removed redundant pullup on THERM_L_OC (R780)

6/9/03
143) added cap on gate of the second FET in Q87 for possible turn on delay (C903)
144) changed inner shield of FWB connector J26 to connect to chassis gnd
145) changed R336 and R325 to 0 ohm to set Vcore VID to 1.3V/1.15V
146) changed R321 to 2.49K to set Vcore offset to +25mV
147) added 10 ohm resistor (R814) and 1uF cap (C904) to filter power to ADT7460 (Gary Leo)

6/10/03
148) changed R612 to 10K to prevent UIDE DMACK from floating
149) changed C80,C88,C81,C89,C82,C102,C79,C87 to NO STUFF (TMDS common-mode termination)
150) changed R205,R218,R211,R219,R210,R220,R204,R214 to 162 ohm 1% (TMDS common-mode termination)
151) changed RP27,RP32,RP28,RP57 to 10ohm (TMDS series termination)

*** released for EVT2 6/10/03 ***

6/13/03
152) fixed NO STUFF on R291
153) removed NO STUFF from C80,C88,C81,C89,C82,C102,C79,C87 (TMDS common-mode termination)
154) removed NO STUFF from R638 (pullup on slewing chip FSEL)
155) removed NO STUFF from C903 (cap on input to second part of THERM_OC_L buffer)
156) CHANGED R321 TO 1K FOR VCORE OFFSET OF 12MV (VCORE = 1.30V -30MV/+100MV)

*** released for EVT2 6/13/03 ***

6/18/03
157) changed R228 to pullup to 1.8V for DVO interface conpatibility
158) added R234 and INT_TMDS option to maintain internal TMDS capability
159) changed L30 to 3 pin symbol
160) added U5 to use as external TMDS transmitter (DVI)
161) added R41 to create +3V_GPU_SI power for SIL1162 (U5)
162) added L14, C130, C132, and C165 for 3V AVCC filtering for SIL1162 (U5)
163) added L13, C14, C129, C131, C133 for 3V PVCC filtering for SIL1162 (U5)
164) added L15, C255, C233, C218 for 3V Vcc filtering for SIL1162 (U5)
165) added R235 and R237 as options for MAIN_RESET_L to U5
166) added R231. R232, and C284 for Vref for U5
167) added R66, R99, R202, R212, R222, R224, R88, R110, R223 as straps for U5
168) added RP58, RP59, RP60, RP61 for series termination of SIL1162 TMDS output
169) added L16, C304, C327, C647 for filtering GPU VDDR4
170) added R255 and R251 to strap GPU_DVODMODE correctly for 1.8V DVO
171) added R268 to connect L16 to +3V_GPU_FLT when not using SIL1162
172) added C681, C668, C678, C651 to filter the thermal sensor diff pairs

6/19/03
173) changed GPU_MEM_IO to +GPU_MEM to connect ATI Vref to correct memory voltage
174) swapped TMDS CLKN and CLKP on RP57 and RP58 for layout
175) swapped DN<0> and DP<0> on RP27 for layout
176) corrected un-named nets in TMDS common-mode filters
177) added physical constriants for new Silicon Image power rails
178) CHANGED C728,C731,C734,C733,C730,C732,C729,C885,C885 TO 128S0022 (124S0024 WILL BE DELETED AS A DUPLICATE IN THE LIBRARY)

6/23/03
179) NO STUFF'ed C895,C899,C896,C897,C898,C900, and C901 to fix no sound problem
180) changed C890 to 100pF for improved transient response (Takashi)
181) Removed bypass traces on FWB chokes and stuffed L70 and L71
182) CHANGED R491 TO 52.3K 1%, R475 TO 127K 1%, AND R476 TO 4.7M 5% IN A29 ADAPTER DETECT CIRCUIT DIVIDERS TO REDUCE SHUTDOWN CURRENT
183) added R331 as CPU Vcore sense resistor (1 mohm 1% 2512)
184) No STUFF'ed C651 and C678
185) added C688,C690,C846,C905 for thermal pair filtering at fan controller
186) added C906 to prevent shoot-thru on Q64 (currently NO STUFF'ed)
187) added C907 to prevent shoot-thru on Q68 (currently NO STUFF'ed)
188) changed R517 to 100K
189) changed GND reference for input side of Q86 to digital GND (the other FET in Q856 remains on VCORE_GNDSNS

6/24/03
190) added C908 to prevent gate shoot-thru on Q56
191) added R279 to power TMDS PLL from LVDS filter when using external TMDS transmitter
192) changed R325 to 470K to set the low Vcore to 1.10V
193) stuffed Vcore offset switch (R807,R805,R809,Q86)
194) changed R809 to 1.5K 1% to set low Vcore offset to 10mV
195) changed R321 to 3.01K 1% to set high Vcore offset to 30mV

6/25/03
196) rotated L70 and L71 for layout (PCB symbol problem)
197) changed Q53,Q54,Q55 to IRF7832 (376S0148) for better thermal performance
198) NO STUFF'ed C908 (Q56 gate shoot-thru cap)

*** released for DVT 6/26/03 ***

7/2/03
199) CHANGED J9 (CARDBUS) TO 516S0141 (NEW PIN PLATING SPEC)
200) CHANGED J20 (AIRPORT) TO 516S0142 (NEW PIN PLATING SPEC)
201) CHANGED J10 (OPTICAL DRIVE) TO 516S0140 (NEW PIN PLATING SPEC)
202) CHANGED J13 (HARD DRIVE) TO 516S0140 (NEW PIN PLATING SPEC)
203) CHANGED J12 (SOUND) TO 516S0144 (NEW PIN PLATING SPEC)
204) CHANGED J8 (MODEM) TO 516S0143 (NEW PIN PLATING SPEC)
205) ADDED BOM TABLE TO PUT 0 OHM 402 ON L77,L80,L81,L82,L76,L78,L79

7/9/03
207) CORRECTED C889 TO CONNECT TO INPUT (PIN 1) OF U55
208) REMOVED POWER JUMPERS XW25,XW17,XW16,XW10,XW14,XW18
209) CHANGED 197S0035 TO PRIMARY AND 197S0004 AS ALTERNATE FOR Y1 (INTREPID)
210) CHANGED 197S0037 TO PRIMARY AND 197S0603 AS ALTERNATE FOR Y3 (ETHERNET)
211) CHANGED 197S0038 TO PRIMARY AND 197S0608 AS ALTERNATE FOR Y5 (NEC USB2)
212) CHANGED 197S0040 TO PRIMARY AND 197S0008 AS ALTERNATE FOR Y4 (LMU)
213) CHANGED 197S0041 TO PRIMARY AND 197S0604 AS ALTERNATE FOR Y6 (PMU)

7/22/03
214) ADDED 1_32V_VCORE AND 1_30V_VCORE BOM OPTIONS FOR 2 DIFFERENT CPU VCORE SPECS
215) UPDATED CAP MATERIAL TYPES
216) CHANGED FROM 715 PIN TO 667 PIN SYMBOL FOR U44 (M10)

7/28/03
217) CHANGED TMDS TERMINATION FROM 2X 162 TO 2X 49.9 OHMS PER PAIR
218) CHANGED 126S0036 FROM ALT TO PRIMARY, REPLACING 126S0035 FOR CPU VCORE INPUT CAPS

*** RELEASED FOR PRODUCTION 7/28/03 ***

8/4/03
219) CHANGED R99 TO NO STUFF TO FIX I2C ADDRESS OF SIL1162 TMDS TRANSMITTER
220) CHANGED R321 TO 4.02K 1% FOR 1_30_VCORE (40MV OFFSET) AND TO 6.34K 1% FOR 1_32_VCORE (60MV OFFSET)
221) CHANGED R304 TO 470K AND R329 AND R325 TO 0 OHM TO CHANGE LOW VID TO 1.05V ON VCORE
222) CHANGED C611 TO 2200PF, C610 TO 100PF, AND R519 TO 12.7K 1% TO INCREASE IMMUNITY TO 3.3V PGOOD SIGNAL DROPOUT
223) NO STUFF C590 TO INCREASE IMMUNITY TO 3.3V PGOOD SIGNAL DROPOUT
224) CHANGED C583 TO 2200PF, C576 TO 100PF, AND R481 TO 15.0K 1% TO INCREASE IMMUNITY TO 3.3V PGOOD SIGNAL DROPOUT
225) NO STUFF C566 TO INCREASE IMMUNITY TO 3.3V PGOOD SIGNAL DROPOUT

9/4/03
228) ADDED 197S0052 AS ALTERNATE FOR G1 (98 MHZ FW OSCILLATOR)
229) CHANGED C728-C734,C884,C885 TO 128S0022 TO REMOVE DUPLICATE PART NUMBER
230) CHANGED C883 TO 132S0100 TO CORRECT FOR USE OF OEM PART NUMBER

8/29/05
1) ADDED 338S0223 (88E1111, B1) AS OPTION
2) ADDED 128S0034 AS OPTION
3) REPLACED 740S0006 WITH 740S0018

*** PRODUCTION RELEASE FOR 051-6582-B ***

01/04/07
1) PER RADAR #4312710, ADD 338S0336 AS ALTERNATE OF 338S0168.
2) PER RADAR #4312710, REPLACE 341S1336 WITH 341S2103, DUE TO 335SXXXX EOL, WHICH REPORT TO 341S1336.

*** SERVICE BON UPDATE FOR 051-6582-C ***

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 40 OF 44	

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*** Signal Cross-Reference for the entire design ***

+1_0V_MARVELL      27D2< 38B3>
+1_5V_AGP          12C5< 12D1< 12D4< 15D6< 16C8<
                   18C6< 18D6< 19A8< 19B4<> 19D5<>
                   21B8< 21D6< 38C3>
+1_5V_AGP_GPU      21C5< 38C3>
+1_5V_AGP_NECK     19B4<> 38B3>
+1_5V_GPU_VDD15    19D3< 38C3>
+1_5V_INTREPID_PLL  8D6< 12D4< 12D8< 14D6<> 38D3>
+1_5V_INTREPID_PLL1  14C3< 38D3>
+1_5V_INTREPID_PLL2  14D3< 38D3>
+1_5V_INTREPID_PLL3  14D3< 38D3>
+1_5V_INTREPID_PLL4  14D3< 38D3>
+1_5V_INTREPID_PLL5  12D3< 38D3>
+1_5V_INTREPID_PLL6  12D6< 38D3>
+1_5V_INTREPID_PLL7  8D5< 38D3>
+1_5V_INTREPID_PLL8  14D3< 38D3>
+1_5V_LDO          35D8< 38D6>
+1_5V_MAIN         38D6>
+1_5V_SLEEP        38D6>
+1_5V_SLEEP_NECK   21A3<> 38B3>
+1_5V_SLEEP_VIN    35D8<> 38D6>
+1_8V_ATI_PVDD     19C5<> 21B6< 21B6< 21D6<> 38C3>
+1_8V_ATI_TPVDD    21D2<>
+1_8V_DVO_F        21B2<
+1_8V_GPU          18A7< 19D8< 20A5< 21A2< 21A6<
                   21B1< 21B6< 21C8< 21D6< 21D8< 38C3>
+1_8V_GPU_AVDD     21D5< 38C3>
+1_8V_GPU_AVDDQ    21D4< 21D7< 38C3>
+1_8V_GPU_MEMPLL   21B5< 38C3>
+1_8V_GPU_PLL      21D5< 38C3>
+1_8V_GPU_PNLIO    21A5< 38C3>
+1_8V_GPU_PNLPLL   21B5< 38C3>
+1_8V_GPU_TP_PLL   21B4< 21D1<
+1_8V_GPU_VDDDI    21C7< 21D4< 38C3>
+1_8V_MAIN         38D6> 39A2>
+1_8V_MAIN_LX_F    35A4<>
+1_8V_PVDD_NECK    19B5<> 38B3>
+1_8V_SLEEP        38D6>
+1_8V_SLEEP_NECK   21A3<> 38B3>
+1_95V_FW_DVDD     28C4< 28C7<> 28D5< 38A3>
+1_95V_FW_DVDD_PORT1  28D6< 38A3>
+1_95V_FW_DVDD_RX0  28C5< 38A3>
+1_95V_FW_DVDD_TX0  28C5< 38A3>
+1_95V_FW_PLL400VDD  28D5< 38A3>
+1_95V_FW_PLL500VDD  28D5< 38A3>
+1_95V_FW_PLLVDD   28D5< 28D7<> 38A3>
+2_5V_CG_MAIN      14C6< 38A3>
+2_5V_GPU          21A7< 21B6< 21D3< 21D7< 21D8<
                   38B3>
+2_5V_GPU_A2VDD    21D4< 21D7< 38C3>
+2_5V_GPU_PNLIO    21A5< 38C3>
+2_5V_INTREPID     9A8< 10D3< 10D5< 10D7< 10D8< 15D7<
                   16B8< 38D3>
+2_5V_MAIN         38D6>
+2_5V_MARVELL      27B8< 27C4<> 38B3>
+2_5V_MARVELL_AVDD  27C4< 38B3>
+2_5V_SLEEP        38D6>
+2_5V_SLEEP_NECK1  19C4<> 38B3>
+2_5V_SLEEP_NECK2  21A3<> 38B3>
+3V_ATI_OSC_SLEEP  18D2< 38C3>
+3V_ATI_SS         18B2< 38C3>
+3V_CG_PLL_MAIN    14C6< 38A3>
+3V_FW             28A3< 28D7<> 29D5< 38A3>
+3V_FW_AVDD        28C6< 38A3>
+3V_FW_AVDD_PORT0  28C6< 38A3>
+3V_FW_AVDD_PORT1  28C6< 38A3>
+3V_FW_AVDD_PORT2  28D6< 38A3>
+3V_FW_ESD         29B3<> 29D2<> 38B3>
+3V_FW_ESD_ILIM    29D4< 38B3>
+3V_FW_UF          28D7<> 38A3>
+3V_GPU            12D1< 18B8< 18C5< 18C7< 18D6<
                   19C4< 19C5< 19C7< 19D7< 21A6< 21B1<
                   38C3>
+3V_GPU_FLT        21B2< 38C3>
+3V_GPU_SI         20C4< 20C8< 20D8<
+3V_HALL_EFFECT    23C6<> 38B6> 39C4>
+3V_INTREPID_USB   14C3< 38D3>
+3V_LCD            22B4<> 38B6>
+3V_LCD_SW         22A4<> 38B6>
+3V_MAIN           38D6>
+3V_NEC_VDD        26D7< 26D7< 38A3>
+3V_PMU            38D6> 39A2>
+3V_PMU_AVCC       25A4< 30B6< 30D5<> 38C6>
+3V_PMU_ESR        32A2< 38C6>
+3V_PMU_RESET      30B7< 34A3<>
+3V_SI_AVCC        20C7< 38B3>
+3V_SI_PLLVCC      20C7< 38B3>
+3V_SI_VCC         20C6< 38B3>
+3V_SLEEP          38D6>
+3V_SLEEP_NECK     21A3<> 38B3>
+3V_SLP_OK_L       33B4<>
+3V_SLP_ON         33A5<>
+4_6V_BU           32A3<> 33B6< 38C6>
+4_85V_ESR         32A4< 38C6>
+4_85V_RAW         30B4< 32A4<> 38C6>
+5V_DDC_SLEEP      22D3<> 22D5<> 38B6> 39A2>
+5V_DDC_SLEEP_UF   22D6< 38B6>
+5V_HD_SLEEP       24D1<> 33A7<> 38C6>
+5V_INV_SW         22B2<> 38B6> 39D1>
+5V_INV_UF_SW      22B2<> 38B6>
+5V_MAIN           38D6>
+5V_SLEEP          38D6>
+5V_SOUND_SLEEP    38B6>
+5V_TPAD_SLEEP     23C7<> 38B6> 39C4>
+12_8V_INV         22B1<> 38B6> 39A2>
+24V_PBUS          38D6> 39B2>
+ADAPTER           31D8<> 32B7< 38D6>
+ADAPTER_ILIM      32B6<> 38C6>
+ADAPTER_OR_BATT   32A5<> 38C6>
+ADAPTER_SENSE     31D5<> 38C6>
+ADAPTER_SW        31D6<> 38C6>
+BATT              38D6>
+BATT_14V_FUSE     31D1<> 38C6>
+BATT_24V_FUSE     31B1< 31D2<> 38C6>
+BATT_POS          31A4<> 38C6> 39C3>
+BATT_RSNS         31B2< 38C6>
+BATT_VSNS         31A4< 38C6>
+FW_FUSE           29D7<> 38A3>
+FW_PWR_OR         28B8< 28D8<> 29D5<> 38A3>
+FW_PWR_PORTA      29C5< 38A3>
+FW_SW             29D5<> 38A3>
+FW_VP0            29C2<> 38A3>
+FW_VP1            29A3<> 38A3>
+GPU_MCLK          21C7< 21D4< 38C3>
+GPU_MEM           18A6<> 18B8< 21B4< 21B7< 21C6<
                   21C8< 21D2< 38C3>
+GPU_MEMCORE       21C5< 38C3>
+GPU_VDD15_NECK    19B5<> 38B3>
+GPU_VDD15_UF      19B5<> 19D4<> 38C3>
+HD_LOGIC_SLEEP    24C2<> 38C6>
+PBUS              38D6> 39B2>
+VCC_CBUS_SW       17B1<> 17B2<> 17D2<> 38D3>
+VPP_CBUS_SW       17B1<> 17B2<> 17D2<> 38C3>
1V20_REF           31C7< 32C8< 38D1>
1V65_REF           31A5<
1_5V_2_5V_OK       35C5> 38B1>
1_5V_BOOST         35C6<> 38C1>
1_5V_BST           35C5<> 38C1>
1_5V_DH            35C5<> 38C1>
1_5V_DL            35B5<> 38C1>
1_5V_FB            35B5< 35B7< 38C1>
1_5V_ILIM          35C5<> 38C1>
1_5V_LX            35B5<> 38C1>
1_5V_SLEEP_EN_L    35C7<> 35D7<>
1_8V_SLEEP_PWREN_L  35A3<>
1_8V_SW            35A5<> 38A1>
1_8V_VFB           38A1>
2_5V_BOOST         35C4<> 38D1>
2_5V_BST           35C4<> 38D1>
2_5V_DH            35C4<> 38D1>
2_5V_DL            35B4<> 38D1>
2_5V_ILIM          35C5<> 38C1>
2_5V_LX            35B4<> 38D1>
2_5V_SLEEP_PWREN_L  35C2<>
2_34V_REF          30A4<
3V_5V_OK           33B4<> 35A8<> 35D6<
3V_5V_OK_INV       35A8<>
3V_BG              33C4<>
3V_BOOST           33C4<>
3V_BOOST_ESR       33D3<>
3V_ITH             33C4<>
3V_ITH_RC          33C3<
3V_PMU_VTAP        32B3<
3V_RSNS            33D2< 38D1>
3V_RUNSS           33C4<
3V_SLEEP_PWREN_L   33A3<>

3V_SNSM            33C4< 37A2>
3V_SNSP            33C4< 37A2>
3V_SW              33C4<> 38D1>
3V_TG              33D4<>
3V_VOSNS           33C4<>
5V_BG              33C5<>
5V_BOOST           33C5<>
5V_BOOST_ESR       33D6<>
5V_HD_PWREN        33A8<>
5V_ITH             33C5<>
5V_ITH_RC          33C6<
5V_RSNS            33D7< 38D1>
5V_RUNSS           33C5<
5V_SLEEP_PWREN     33A8<>
5V_SNSM            33C5< 37A2>
5V_SNSP            33C5< 37A2>
5V_SW              33C5<> 38D1>
5V_TG              33C5<>
5V_VOSNS           33C5<>
1625_BG            32C5<>
1625_BST           32C5<
1625_BST_ESR       32C5<>
1625_COMP          31D2< 32C6<
1625_DIV           32C8<
1625_ENABLE        32D7<>
1625_ENABLE_L      32D6<>
1625_EXTVCC        32D5<> 38D1>
1625_FCB           32C6<
1625_INTVCC        32C5<> 38D1>
1625_RUNSS         32C6<
1625_SGND          32B7<> 38D1>
1625_TG            32C5<>
1625_VFB           32B5<>
1625_VIN           32C6< 38D1>
1625_VSW           32C4<> 38D1>
1772_ACIN          31B5<
1772_ACOK_L        31B5<> 31C4<>
1772_BST           31B4<>
1772_BST_ESR       31C3<
1772_CCI           31B5<>
1772_CCS           31B5<
1772_CCV           31B5<>
1772_CCV_RC        31B5<
1772_CELLS         31B4<
1772_CLS           31A4<
1772_CSIN          31B4<> 37A2>
1772_CSIP          31B4<> 37A2>
1772_CSSN          31C5< 37A2>
1772_CSSP          31C5< 37A2>
1772_DCIN          31B5< 38C6>
1772_DHI           31B4<>
1772_DLO           31B4<>
1772_DLOV          31B4<> 38C6>
1772_GND           31A5<> 38C6>
1772_ICHG          31B5<>
1772_ICTL          31B5<>
1772_IINP          31B5<
1772_LDO           31C4<> 38C6>
1772_LX            31B4<> 38C6>
1772_REF           31B5<>
1772_VCTL          31B5<
1778_BG            19A5<> 38B1>
1778_BST           19A5<> 38B1>
1778_BST_RC        19A4<> 38B1>
1778_FCB           19A5< 38B1>
1778_GND           19A5< 19A7<> 38B1>
1778_ION           19A5< 38B1>
1778_ITH           19A5<> 38B1>
1778_ITH_RC        19A7< 38B1>
1778_SHDN_L        19A6<
1778_SHDN_L_D3COLD  19A7<>
1778_TG            19A5<> 38B1>
1778_VCC           19A5<> 38B1>
1778_VFB           19A2< 19A5< 38B1> 39A1>
1778_VIN           19A5< 38B1>
1778_VRNG          19A5< 38B1>
3405_MODE          27D5<
3405_VFB           27D4<>
3707_FCB           33C5<
3707_FSET          33C5<
3707_INTVCC        33D4<> 38D1>
3707_SGND          33B5<> 38D1>
3707_STBY          33C5<>
A29_CLS_ADJ        31A5<>
A29_CURRENT_ADJ    31C4<>
A29_DETECT         30A2< 31A5<> 31C4<>
A29_DET_L          30A3<
AB_SEL_LOW         34A6<>
AC_DIV             31C8<
AC_ENABLE_GATE     31D6<>
AC_ENABLE_L        31C6<>
AC_GTR_18V         31C4<>
AC_IN              27B8<> 29C7< 30B3< 31C5<> 31C7<>
AC_IN_FW_CNTL      29C7<>
AC_IN_L            31C2<> 31C6<>
AC_IN_L_RC         31C2<>
ADAPTER_DET        30A4< 31D8<> 39C2>
ADAPTER_I_REG      31D3<>
ADT7460_ADR_EN_L   25B3<>
ADT7460_FAN1_PWM   25B3<>
ADT7460_FAN2_PWM   25B3<>
ADT7460_THERM      25A5<> 25B3<>
ADT7460_VCC        25C4<
ADT7460_VCORE_MON  5C8<> 25B4<>
AGP8X_DET_PU       18C6<>
AGP_AD<0>          12D2<> 18C7<>
AGP_AD<15..0>      37D5>
AGP_AD<1>          12C2<> 18C7<>
AGP_AD<2>          12C2<> 18C7<>
AGP_AD<3>          12C2<> 18C7<>
AGP_AD<4>          12C2<> 18C7<>
AGP_AD<5>          12C2<> 18C7<>
AGP_AD<6>          12C2<> 18C7<>
AGP_AD<7>          12C2<> 18C7<>
AGP_AD<8>          12C2<> 18C7<>
AGP_AD<9>          12C2<> 18C7<>
AGP_AD<10>         12C2<> 18C7<>
AGP_AD<11>         12C2<> 18C7<>
AGP_AD<12>         12C2<> 18C7<>
AGP_AD<13>         12C2<> 18C7<>
AGP_AD<14>         12C2<> 18C7<>
AGP_AD<15>         12C2<> 18C7<>
AGP_AD<16>         12C2<> 18C7<>
AGP_AD<31..16>     37D5>
AGP_AD<17>         12C2<> 18C7<>
AGP_AD<18>         12C2<> 18C7<>
AGP_AD<19>         12C2<> 18C7<>
AGP_AD<20>         12C2<> 18C7<>
AGP_AD<21>         12C2<> 18C7<>
AGP_AD<22>         12C2<> 18C7<>
AGP_AD<23>         12C2<> 18C7<>
AGP_AD<24>         12C2<> 18C7<>
AGP_AD<25>         12C2<> 18D7<>
AGP_AD<26>         12C2<> 18D7<>
AGP_AD<27>         12B2<> 18D7<>
AGP_AD<28>         12B2<> 18D7<>
AGP_AD<29>         12B2<> 18D7<>
AGP_AD<30>         12B2<> 18D7<>
AGP_AD<31>         12B2<> 18D7<>
AGP_AD_STB<0>      12A2<> 12B2< 18D6<> 37D5>
AGP_AD_STB<1>      12A2<> 12B2< 18D6<> 37D5>
AGP_AD_STB_L<0>    12A2<> 12B2< 18D6<> 37D5>
AGP_AD_STB_L<1>    12A2<> 12A2< 18D6<> 37D5>
AGP_ATI_RESET_L    18B7<
AGP_ATI_VREF       18B7<
AGP_ATI_VREFG      18B7<
AGP_BUSY_L         12C4<> 12D2< 18D6>
AGP_CBE<0>         12B2<> 18B7<>
AGP_CBE<1..0>      37D5>
AGP_CBE<1>         12B2<> 18B7<>
AGP_CBE<2>         12B2<> 18B7<>
AGP_CBE<3..2>      37D5>
AGP_CBE<3>         12B2<> 18C7<>
AGP_DEVSEL_L       12B2<> 12C2< 18B7<> 37D5>
AGP_FRAME_L        12B2<> 12C2< 18B7<> 37D5>
AGP_GNT_L          12C2< 12D2<> 18B7< 37D5>
AGP_INT_L          14B5<> 18B7<>
AGP_IRDY_L         12B2<> 12C2< 18B7<> 37D5>
AGP_PAR            12B2<> 18B7> 37D5>
AGP_PIPE_L         12A2<> 12B2<
AGP_RBF_L          12A2<> 12C2< 18C6> 37D5>
AGP_REQ_L          12C2< 12D2<> 18B7<> 37D5>
AGP_SBA<0>         12B2< 18C6>
AGP_SBA<7..0>      37D5>
AGP_SBA<1>         12B2<> 18C6>
AGP_SBA<2>         12B2<> 18C6>
AGP_SBA<3>         12B2<> 18C6>
AGP_SBA<4>         12B2<> 18C6>

AGP_SBA<5>         12B2<> 18C6>
AGP_SBA<6>         12B2<> 18C6>
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AGP_SB_STB_L       12A2<> 12A2< 18C6<> 37D5>
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AGP_SUS_STAT_L_PU  18C6<
AGP_TRDY_L         12B2<> 12C2< 18B7<> 37D5>
AGP_WBF_L          12A4<> 12B2< 18B7>
AIRPORT_CLKRUN_L   24C6<> 39C1>
AIRPORT_IDSEL      24C5<> 39B1>
AIRPORT_PCI_GNT_L  12D7<> 24D5<> 39C4>
AIRPORT_PCI_INT_L  14B5<> 14D7< 24D5<> 39C4>
AIRPORT_PCI_REQ_L  12A7< 12D7<> 24D6<> 39D4>
AIRPORT_PME_L_TP   24D5<>
AMP_CONTROL        25C5<> 25D5<>
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ATI_AGP_FBSKEW<1>  19C2< 19C7<>
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ATI_CLK27M_IN      18C1< 19B7<
ATI_CLK27M_OSC     18D2<
ATI_CLK27M_OSC_SS  18B2< 18D1<
ATI_DBI_HI_PU      18C6<>
ATI_DBI_LO_PU      18C6<>
ATI_DVODMODE       21A3<
ATI_GPIO7_SPN      19C7<>
ATI_GPIO8_PD       19C7<>
ATI_GPIO9_SPN      19C7<>
ATI_GPIO10_SPN     19C7<>
ATI_GPIO11_SPN     19C7<>
ATI_GPIO12_SPN     19C7<>
ATI_GPIO13_SPN     19C7<>
ATI_HSYNC          19D5<> 22C8<
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ATI_MEMVMODE0      18A7<
ATI_MEMVMODE1      18A7<
ATI_OSC_OE         18D3<
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ATI_R2SET          19D6<>
ATI_RSET           19D6<>
ATI_RSTB_MSK       18C6<>
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BATTV_HIGH         31B7<>
BATTV_LOW          31B8<>
BATT_14PBUS_EN     31C1<>
BATT_14V_GATE      31C1<>
BATT_24PBUS_EN     31C2<>
BATT_24V_GATE      31C1<>
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BATT_DATA          31A4<> 39C3>
BATT_DIV           31A5<
BATT_LOW           31A6<>
BATT_LOW_L         31B6<>
BATT_NEG           31A4<> 38C6> 39C3>
BBANG_HRESET_L     23A4< 23C4<> 39C1>
BBANG_JTAG_TCK     23B3< 23C4<>
BBANG_TCK_EN       23B3<
BCKFD_PROT_EN_L    31C6<>
BCKFD_PROT_GATE    31D6<>
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BRIGHT_PWM_UF      22A2<>
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BT_USB_DP          14C1< 24B2<> 37B2> 39B6>
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CAPSLOCK_LED_L     23B8< 30C7<
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CBUS_DATA<13>      17A4<> 17C2<>
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CBUS_DET_2_L       17A2<> 17C4< 39B8>
CBUS_INPACK_L      17B2<> 17B4<
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CBUS_IORD_L        17B2<> 17C4>
CBUS_IOWR_L        17B2<> 17C4>
CBUS_MFUNC1_PD     17A7< 17A7<>
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CBUS_PCI_PERR_L    17B7<> 17D7<
CBUS_PCI_REQ_L     12A7< 12D7<> 17A7>
CBUS_PCI_RESET_L   17A7<
CBUS_PCI_SERR_L    17B7> 17D7<
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CBUS_RESET_L       17B2<> 17C4>
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CBUS_VCCD0_L       17C4<>
CBUS_VCCD1_L       17C4<>
CBUS_VPPD0         17C4<>
CBUS_VPPD1         17C5<>
CBUS_VS1           17B2<> 17C4<>
CBUS_VS2           17B2<> 17C4<>
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CBUS_WE_L          17B1<> 17C4>
CBUS_WP_L          17A1<> 17B4<
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CG_CLKOUT          14B6<>
CG_FSEL            14B7< 14C5<>
CG_LOCK            14B7<>

CG_RESET_L         14B7<
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CHARGE_LED_L       30C6<> 30D7< 31D8<> 39D2>
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CHGND2             38A6>
CHGND3             38A6>
CHGND4             38A6> 39B6>
CHGND5             38A6>
CHGND6             38A6>
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CLK10M_PMU_XOUT    30B6<
CLK10M_PMU_XOUT_UF  30B7<
CLK18M_INT_EXT     14A6<> 36B1>
CLK18M_INT_XIN     14A5< 36B1>
CLK18M_INT_XOUT    14A5<> 36B1>
CLK18M_XTAL_IN     14A5< 36B1>
CLK25M_ENET_XIN    27A7< 36B1>
CLK25M_ENET_XOUT   27A7<> 36B1>
CLK25M_XTAL_IN     27A7<
CLK27M_GPU_XIN     36B1>
CLK27M_GPU_XOUT    36B1>
CLK27M_XTAL_IN     36B1>
CLK32K_PMU_XIN     30B3<>
CLK32K_PMU_XOUT    30B3<>
CLK32K_PMU_XOUT_UF  30B2<>
CLK33M_AIRPORT     12D8< 24D5<> 36C1> 39B1>
CLK33M_AIRPORT_UF  12C7<> 36C1>
CLK33M_CBUS        12D8< 17A7< 36C1>
CLK33M_CBUS_UF     12C7<> 36C1>
CLK33M_USB2        12C8< 26B7< 36C1>
CLK33M_USB2_UF     12C7<> 36C1>
CLK66M_AGP_15V_TP  12C4>
CLK66M_GPU_AGP     12C8< 18B7< 36C1>
CLK66M_GPU_AGP_UF  12C7<> 36C1>
CLKENET_LINK_GBE_REF  13C5< 27C8< 36B1>
CLKENET_LINK_GTX   13C5<> 36A1>
CLKENET_LINK_RX    13D5< 27C8< 36B1>
CLKENET_LINK_TX    13D5< 27D8< 36A1>
CLKENET_PHY_GBE_REF  27C7<> 36B1>
CLKENET_PHY_GTX    13C6< 27C7< 36A1>
CLKENET_PHY_RX     27C7<> 36B1>
CLKENET_PHY_TX     27D7<> 36B1>
CLKFW_LINK_LCLK    13C3<> 36A1>
CLKFW_LINK_PCLK    13C3<> 28C3< 36A1>
CLKFW_PHY_LCLK     13C2< 28B8< 36A1>
CLKFW_PHY_PCLK     28B4> 28C3< 36A1>
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CLKLVDS_LP         19B5> 22A4<> 37C2> 39B7>
CLKLVDS_UN         19B5> 22A4<> 37C2> 39B7>
CLKLVDS_UP         19B5> 22A4<> 37C2> 39A7>
COMM_DTR_L         14C2> 25D1<> 39B2>
COMM_GPIO_L        14C2<> 25D2<> 39C2>
COMM_RESET_L       14C5<> 25C4<> 39C4>
COMM_RING_DET_L    14B5<> 14C7< 25C3<> 30C6<> 39C4>
COMM_RTS_L         14C2> 25D1<> 39B2>
COMM_RXD           14C2<> 25D1<> 39B2>
COMM_SHUTDOWN      14C5<> 25C4<> 39C4>
COMM_TRXC          14C2<> 25D2<> 39C2>
COMM_TXD_L         14C2<> 25D2<> 39C2>
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COMP_ENABLE        22C1<>
COMP_RC            32C6<
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CPU_ADDR<30>       5B7<> 8C6<>
CPU_ADDR<31>       5B7<> 8B6<>
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CPU_AVDD           5C3< 38D3>
CPU_BG_L           5C7< 8C2< 8D6<> 36D5>
CPU_BR_L           5C7> 8D2< 8D6< 36D5>
CPU_BUS_VSEL       5C3< 7A6<
CPU_CHKSTP_OUT_L   5B3<> 5C2< 39D8>
CPU_CHKS_L         5A3< 5D2<
CPU_CI_L           5A7> 8B6<> 36D5>
CPU_CLKOUT_SPN     5C3>
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PCI_PAR           12C7<> 17B7<> 24C5<> 26B7<> 37C5>
                  39D4>
PCI_STOP_L        12A7< 12C7<> 17B7<> 24C5<> 26B7<>
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PCI_TRDY_L        12B7< 12C7<> 17A7<> 24C5<> 26B7<>
                  37C5> 39A5>
PLL_STOP_L        7C4<> 7C8<>
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PMU_AC_DET        30A4< 30B4<>
PMU_AC_IN         30B4<>
PMU_BATT0_DET_L   30B4<>
PMU_BATT1_DET_L_PU  30B4<> 30D2<>
PMU_BATT_DET_L    30B3> 30D2< 31A4<> 39C3>
PMU_BYTE          30B6< 30C7<>
PMU_CAPSLOCK_LED_L  30C6<>
PMU_CHARGE_V      30C4<> 31B8<>
PMU_CHRG_BATT_G   30C6<> 31A8<>
PMU_CLK           14C2<> 30C4<>
PMU_CNVSS         30B6< 30C7<>
PMU_CPU_RESET_L   23A4< 23C4<> 30C4<>
PMU_EPM           30D2< 30D4<>
PMU_FROM_IWP      14C2<> 30C4<>
PMU_I2C_CLK       30B4<> 30C2<>
PMU_I2C_DATA      30B4<> 30C2<>
PMU_IWP_L         14B5<> 14B7< 30B6<>
PMU_IWP_NMI       14B5<> 14B7< 30D4<>
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PMU_KB_RESET_IN2  30A7<>
PMU_KB_RESET_L    30A6> 30B7< 39B2>
PMU_LID_CLOSED_L  23A8< 23C4<> 30B2< 30C4<>
PMU_NMI_BUTTON_L  25C1< 30C2< 30C4<>
PMU_NMI_L         30C2< 30C4<>
PMU_NUMLOCK_LED_L  30C4<>
PMU_OOPS          30B2< 30B4<>
PMU_PME_L         14B5<> 26B8< 30B2< 30C4<>
PMU_POWERUP_OK    30B4<> 30D2<>
PMU_POWER_UP_L    29C7<> 30C6<> 30D7< 33B8<
PMU_RSQ_L         14B7< 14C2> 30C4<>
PMU_RESET_BUTTON_L  25B1< 30C4<> 30D2<
PMU_RESET_L       30B6<>
PMU_SLEEP_LED     23C4<>
PMU_SLEEP_LED_L   23C2<> 30C4<>
PMU_SMB_CLK       30B4<> 30C2< 31A3<
PMU_SMB_DATA      30B4<> 30C2< 31A2<
PMU_TO_INT        14C2<> 30C4<>
POWER_UP          29C7<>
POWER_VALID       30B2< 30C4<>
PWR_BUTTON_L      23A7<> 25C2< 39B2>
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RAM_ADDR<12..0>   36A5>
RAM_ADDR<1>       9B4< 11B3<> 11B8<>
RAM_ADDR<2>       9B4< 11B5<> 11B6<>
RAM_ADDR<3>       9B4< 11B3<> 11B8<>
RAM_ADDR<4>       9B4< 11B5<> 11B6<>
RAM_ADDR<5>       9B4< 11B3<> 11B8<>
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RAM_ADDR<11>      9A4< 11B5<> 11B6<>
RAM_ADDR<12>      9A4< 11B3<> 11B8<>
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RAM_BA<1>         9A4< 11B5<> 11B6<>
RAM_CAS_L         9A4< 11B5<> 11B6<> 36A5>
RAM_CKE<0>        9A3< 9C4< 11B6<>
RAM_CKE<3..0>     36A5>
RAM_CKE<1>        9A3< 9C4< 11B8<>
RAM_CKE<2>        9A3< 9C4< 11C5<>
RAM_CKE<3>        9A3< 9C4< 11C3<>
RAM_CS_L<0>       9C4< 11B8<>
RAM_CS_L<3..0>    36A5>
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RAM_CS_L<2>       9C4< 11B3<>
RAM_CS_L<3>       9C4< 11B5<>
RAM_DATA_A<0>     10C6<> 11D8<>
RAM_DATA_A<7..0>  36C5>
RAM_DATA_A<1>     10C8<> 11D8<>
RAM_DATA_A<2>     10C8<> 11D8<>
RAM_DATA_A<3>     10B8<> 11D8<>
RAM_DATA_A<4>     10B8<> 11D6<>
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RAM_DATA_A<7>     10B8<> 11D6<>
RAM_DATA_A<8>     10B8<> 11D8<>
RAM_DATA_A<15..8>  36C5>
RAM_DATA_A<9>     10C7<> 11D8<>
RAM_DATA_A<10>    10C7<> 11D8<>
RAM_DATA_A<11>    10C7<> 11D8<>
RAM_DATA_A<12>    10C7<> 11D6<>
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RAM_DATA_A<17>    10C4<> 11B3<>
RAM_DATA_A<18>    10C4<> 11B5<>
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RAM_DQM_A<3>      10C5<> 11C6<>
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RAM_DQM_A<7>      10C1<> 11A6<> 36A5>
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RAM_DQM_B<3..2>   36B5>
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RAM_DQM_B<5..4>   36B5>
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RAM_DQS_A<2>      10B6<> 11C8<>
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RAM_DQS_B<7>      10C2<> 11A3<> 36A5>
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RAM_MUXSEL_L      10A3< 10A5< 10B5<> 10B7<> 36A5>
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RAM_WE_L          9A4< 11B3<> 11B8<> 36A5>
RF_DISABLE_L_EPM  24D6<> 39C1>
RIGHT_USB_DM      26A3< 32A7<> 37A2> 39D1>
RIGHT_USB_DP      26A3< 32A7<> 37A2> 39D1>
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RJ45_C1_PD        27B2<>
RJ45_C2_PD        27B2<>
RJ45_C3_PD        27B2<>
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RJ45_DN<2>        27B2<> 37D2> 39A3>
RJ45_DN<3>        27B2<> 37D2> 39A3>
RJ45_DP<0>        27B2<> 37D2> 39B3>
RJ45_DP<1>        27B2<> 37D2> 39B3>
RJ45_DP<2>        27B2<> 37D2> 39A3>
RJ45_DP<3>        27B2<> 37D2> 39A3>
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ROM_OE_L          9B3< 12A5< 24C5<> 39B1>
ROM_ONBOARD_CS_L  9B3< 24C6<> 39B1>
ROM_RW_L          9B3< 12A5< 24C6<> 39B1>
ROM_WP_L          9B3<
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RSDM5_TP          26C5>
RSDP3_TP          26C5>
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RSDP5_TP          26C5>
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SI_DDC_DATA       19C5<> 20B7<
SI_EDGE           20B7<
SI_MSEN           20B5<>
SI_PD             20B7<
SI_RST            20B7<
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SI_TMDS_CLKP      20B5<> 20C4<
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SI_TMDS_DP<2>     20A5<> 20B4<
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SLEEP_LED_L       23D2<
SLEEP_LED_SW_L    23C2<>
SLEEP_LED_UF      23C1<
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SLEEP_NET_INV     33A3<>
SMC_TP            26B5<
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SND_AMP_MUTE      25C8< 25D6<> 39A4>
SND_AMP_MUTE_F    25C7< 25D6<>
SND_AMP_MUTE_L    14C5<> 25D5<>
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SND_CLKOUT_F      25C7<> 25D7<
SND_HP_MUTE       25C5<>
SND_HP_MUTE_INV   25C5<> 25C6<> 39A4>
SND_HP_MUTE_L     14C5<> 25C4<>
SND_HP_SENSE_L    14B5<> 25D6<> 39C6>
SND_HW_RESET_L    14A7< 14B5<> 25C8< 39C6>
SND_HW_RESET_L_F  25C6<> 25C7<
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SND_SCLK_F        25C7< 25D7<>
SND_SYNC          14B1< 25D8< 39D6>
SND_SYNC_F        25C7<> 25D7<
SND_TO_AUDIO      14B1< 25D8< 39D6>
SND_TO_AUDIO_F    25D6<> 25D7<
SOFT_PWR_ON_L     22D1< 23A8< 30A8< 30C6<> 30D7<
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SRCLK_TP          26A5> 39A4>
SRNOD_TP          26A5< 39A4>
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ST7_KBD_LED_OUT   23A4< 23C4<>
ST7_OSC1          23D5<
ST7_OSC2          23D5<>
ST7_PB6_PD        23B2< 23C4<>
ST7_RESET_L       23D5<>
ST7_SENSOR4_SCK_PD  23B2< 23D4<>
ST7_SENSOR4_SDA_PD  23B2< 23D4<>
ST7_SENSOR5_SCK_PU  23B2< 23D4<>
ST7_SENSOR5_SDA_PU  23B2< 23B4<>
ST7_SLEEP_LED_H   23C2<> 23C4<>
ST7_XTAL_IN       23C5<
STOP_ACK_L        12D2< 12D4<>
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SUPPLY_M_DP       25B6< 25B8<
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SUTRO_ALS_OUT     23C4<> 24B2<> 39C2>
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SYSCLK_CPU_UF     8A6<> 36D1>
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SYSCLK_DDRCLK_A0_L  9D4< 11D8<> 36D1>
SYSCLK_DDRCLK_A0_L_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_A0_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_A1  9D4< 11A6<> 36D1>
SYSCLK_DDRCLK_A1_L  9D4< 11A6<> 36D1>
SYSCLK_DDRCLK_A1_L_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_A1_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_B0  9D4< 11D3<> 36D1>
SYSCLK_DDRCLK_B0_L  9C4< 11D3<> 36C1>
SYSCLK_DDRCLK_B0_L_UF  9B6<> 9C5< 36D1>
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SYSCLK_DDRCLK_B1  9D4< 11A5<> 36C1>
SYSCLK_DDRCLK_B1_L  9D4< 11A5<> 36C1>
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TEST_TP           26A5< 39A4>
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THERM1_A_DP       25A6< 25A8< 37A2>
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THERM1_DP         25A5< 25B5< 25B5<> 37A2>
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THERM1_M_DP       37A2>
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THERM2_A_DP       25A6< 25A8< 37A2>
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THERM2_DP         25A5< 25B5< 25B5<> 37A2>
THERM2_M_DM       37A2>
THERM2_M_DP       37A2>
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TMDS_CLKP         20B3< 20C2< 20C3< 22C7<> 37B2>
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TMDS_CONN_CLKP    22C6<> 22C7<> 37B2> 39D7>
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TPAD_F_TXD        23A7<> 39C4>
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TPS2211_SHDN_L_PU  17C4<
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TV_GND2           22A6<> 38B6> 39A7>
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UIDE_DATA<15>     13D7<> 24B4<
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UIDE_DIOW_L       13C7<> 24A4< 37C5>
UIDE_DMACK_L      13C7<> 24A4< 37C5>
UIDE_DMARQ        13C7<> 37C5>
UIDE_INTRQ        13C7< 37C5>
UIDE_IOCHRDY      13C7< 24A4< 37C5>
UIDE_REF          13C7<> 38D3>
UIDE_RST_L        13C7<> 24A4< 37C5>
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USB2_PCI_INT_L    14B5<> 14C7< 26A8<
USB2_PCI_REQ_L    12A7< 12D7<> 26B7>
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USB_D1P           14C1< 26A4< 26A5>
USB_D2N           14D1< 26A4< 26A5>
USB_D2P           14D1< 26A5< 26A5>
USB_DAN           14B2<> 14D2< 26A5>
USB_DAP           14B2<> 14D2< 26A5>
USB_DBN           14B2<> 14D2<
USB_DBP           14B2<> 14D2<
USB_DCN           14B2<> 14C2< 26A5>
USB_DCP           14B2<> 14C2< 26A5>
USB_DDN           14B2<> 14C2<
USB_DDP           14B2<> 14C2<
USB_DEN           14B2< 14B2<> 37B2>
USB_DEP           14B2<> 14C2< 37B2>
USB_DFN           14B2< 14B2<> 37B2>
USB_DFP           14B2< 14B2<> 37B2>
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USB_OC_CD_L       14B2< 14C7<
USB_OC_EF_L       14B2< 14D7<
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USB_PWREN_CD_L    14B2<> 14C7<
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VCORE_BST         34C5<> 38C1>
VCORE_CC          34B6<> 38B1>
VCORE_CNTL_RC     19A3<>
VCORE_DH          34B5<> 38C1>
VCORE_DL          34B5<> 38C1>
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VCORE_FAST<2>     34D3< 34D5<
VCORE_FAST<3>     34D3< 34D5<
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VCORE_FB          34B5< 38B1> 39A2>
VCORE_GND         34B5<> 38B1>
VCORE_GNDA        34B6<>
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VCORE_GNDDIV_TEST  34A3<>
VCORE_GNDSNS      34A2<> 34A4< 38B1>
VCORE_GNDSNS_TEST  34A3<>
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VCORE_LX          34B5<> 38C1>
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VCORE_MUX_SEL     34D5<>
VCORE_REF         34B6<> 38C1>
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VCORE_SEL_ON      34B6<>
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VCORE_TIME        34B4<> 38B1>
VCORE_TON         34B6< 38C1>
VCORE_VCC         34C6< 38C1>
VCORE_VGATE       14B5< 14B7< 34B4> 38B1>
VCORE_VID0        39A3>
VCORE_VID1        39A3>
VCORE_VID2        39A3>
VCORE_VID3        39A3>
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 42 OF 44	

*** Part Cross-Reference for the entire design ***

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D7	DIODE_SCHOT	32
D8	ZENER	29
D9	DIODE	31
D10	DIODE	31
D11	DIODE_SCHOT	32
D12	DIODE_DUAL_6P	29
D13	DIODE_SCHOT	33
D14	DIODE_SCHOT_3P2	28
D15	DIODE_DUAL_6P	29
D16	DIODE	33
D17	DIODE_SCHOT	32
D18	DIODE	32
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D27	DIODE_SCHOT	32
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J3	CON_F14RT_S2MT_SM	24
J4	CON_3RTSM_125	25
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J6	CON_F30RT_S2MT_SM	22
J7	CON_4RT_WRIB	22
J8	CON_F16ST_D_SMA	25
J9	CON_M80ST_D4MT_SM	17
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J11	CON_F14RT_S2MT_SM	32
J12	CON_F30ST_D_SM	25
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J14	CON_F30RT_T6MT_TH1	22
J15	CON_F5RT_MINIDIN_TH	22
J16	CON_10STSM_5087	25
J17	CON_RJ45_SHORT_4MT_TH	27
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J20	CON_F80ST_D4MT_SM	24
J22	CON_F200RT_DDRDIMM_SM2	11
J23	CON_F6RT_S4MT_TH1	29
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R742	RES	31
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R784	RES	26
R785	RES	30
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R811	RES	25
R812	RES	25
R813	RES	25
R814	RES	25
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RP9	RPAK4P	24
RP10	RPAK4P	24
RP11	RPAK4P	24
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RP13	RPAK4P	24
RP14	RPAK4P	13
RP15	RPAK4P	13
RP16	RPAK4P	13
RP17	RPAK4P	12
RP18	RPAK4P	12
RP19	RPAK4P	12
RP20	RPAK4P	12
RP21	RPAK4P	8
RP22	RPAK4P	12
RP23	RPAK4P	8
RP24	RPAK4P	8 14
RP25	RPAK4P	9
RP26	RPAK4P	9
RP27	RPAK22P	20
RP28	RPAK22P	20
RP29	RPAK4P	14
RP30	RPAK4P	9
RP31	RPAK4P	9
RP32	RPAK22P	20
RP33	RPAK4P	9
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RP35	RPAK4P	9
RP36	RPAK4P	9
RP37	RPAK4P	28
RP38	RPAK4P	28
RP39	RPAK10P2C	17
RP40	RPAK4P	30
RP41	RPAK4P	30
RP42	RPAK10P2C	23
RP43	RPAK10P2C	23
RP44	RPAK4P	25
RP45	RPAK4P	26
RP46	RPAK4P	14
RP47	RPAK4P	14
RP48	RPAK4P	14
RP49	RPAK4P	24
RP50	RPAK4P	24
RP51	RPAK4P	14
RP52	RPAK4P	23 26
RP53	RPAK4P	23
RP54	RPAK4P	26
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RP56	RPAK4P	14
RP57	RPAK22P	20
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RP59	RPAK22P	20
RP60	RPAK22P	20
RP61	RPAK22P	20
SH1	SHLD_3P_EMI	4
SP1	SPKR_CLIP_P84	4
SP2	SPKR_CLIP_P84	4
SP3	SPKR_CLIP_P84	4
SP4	SPKR_CLIP_P84	4
SP5	SPKR_CLIP_P84	4
SP6	SPKR_CLIP_P84	4
T1	XFR_ENET_1000BT	27
U1	SN74AUC1G04	7
U2	SN74AUC1G08	23
U3	ADT7460	25
U4	SN74AUC1G08	23
U5	SIL1162	20
U7	VREG_LT1962	14
U9	CBTV4020	10
U10	CBTV4020	10
U11	PI3B3257	34
U12	CBTV4020	10
U13	CBTV4020	10
U14	LTC3405	27
U15	COMPARATOR_LMC7211	31
U16	LTC1778	19
U17	FEPR_1MX8	9
U18	LTC1625	32
U19	PWR_CNTRL_TPS2211	17
U20	MAX1717	34
U21	COMPARATOR_LMC7211	32
U22	MAX1715	35
U23	AMP_MAX4172	31
U24	7432	22 30
U25	VREG_LP2951	32
U26	PC11510GGU	17
U27	COMPARATOR_LMC7211	30
U28	LTC3707	33
U29	TSB81BA3A	28
U30	VREG_LP2951	32
U31	MAX1772	31
U32	EEPROM_16KX8_M2412RB	23
U33	M14C62	30
U34	VREG_LM2594	28
U35	MAX1916	23
U36	LTC1761	28
U37	VREG_LT1962	28
U38	COMPARATOR_LMC7211	31
U39	UPD720101_FBGA	26
U40	OPAMP_MAX4236EUTT	23
U42	CLK_GEN_CY28512	14
U43	APOLLO_MPC7445_360	5 6
U44	BAGE_HBLTY_M10_CSP64_667	18 19 21
U45	INTREPID	8 9 12 13 14 15
U46	COMPARATOR_LMC7211	22
U47	CLK_GEN_CY25811	18
U49	TRANSCEIVER_88E1111	27
U50	OPAMP_LMC7111	31
U51	MAX6804	30
U52	FEPR_256KX8_ST72264_BGA	23
U54	VREG_NM157LJ	21
U55	VREG_NM157LJ	21
U56	741G32	22
U57	741G32	22
U58	LTC3412	35
XW1	SHORT	35
XW2	SHORT	19
XW3	SHORT	34
XW4	SHORT	32
XW5	SHORT	34
XW6	SHORT	35
XW7	SHORT	34
XW8	SHORT	33
XW9	SHORT	25
XW11	JUMPER	35
XW12	SHORT	22
XW13	SHORT	22
XW15	SHORT	34
XW19	SHORT	31
XW20	SHORT	19
XW21	SHORT	19
XW22	SHORT	19
XW23	SHORT	19
XW24	SHORT	19
XW27	SHORT	21
XW28	SHORT	21
XW29	SHORT	21
XW30	SHORT	21
XW31	SHORT	5
Y1	CRYSTAL	14
Y3	CRYSTAL	27
Y4	CRYSTAL	23
Y5	CRYSTAL	26
Y6	CRYSTAL	30
Y7	CRYSTAL_4PIN	30
ET1	HOLE_VIA	4
ET2	MTGHOLE	4
ET3	HOLE_VIA	4
ET4	MTGHOLE	4
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ET6	MTGHOLE	4
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ET13	HOLE_VIA	4
ET14	HOLE_VIA	4
ET15	HOLE_VIA	4
ET16	MTGHOLE	4
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ET79	HOLE_VIA	4
ET80	HOLE_VIA	4
ET81	HOLE_VIA	4
ET82	HOLE_VIA	4
ET83	MTGHOLE	4