1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
A		285476	PRODUCTION RELEASED	07/28/03	?

SCHEM,MLB,PB17"

08/05/2003

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1	TITLE PAGE AND CONTENTS
2	SYSTEM BLOCK DIAGRAM
3	POWER BLOCK DIAGRAM
4	PCB NOTES AND HOLES
5	MPC7450 MAXBUS INTERFACE
6	MPC7450 DATA
7	CPU PLL AND CONFIGURATION STRAPS
8	INTREPID MAXBUS AND BOOT STRAPS
9	INTREPID MEMORY INTERFACE / BOOT ROM
10	DDR MEMORY MUXES
11	200PIN DDR MEMORY SODIMM CONNECTORS
12	INTREPID AGP 4X/PCI
13	INTREPID ENET/FW/UATA/EIDE INTERFACES
14	INTREPID GPIOS/SERIAL/USB INTERFACES/SSCG
15	INTREPID POWER RAILS
16	INTREPID DECOUPLING
17	CARDBUS CONTROLLER (PCI1510)
18	M10 AGP & CLOCKS
19	M10 LVDS/TMDS/VGA/GPIO & GPU VCORE
20	SIL1162 TMDS TRANSMITTER
21	M10 ANALOG, POWER, GND

PAGE	CONTENTS
22	VIDEO CONNECTORS - INVERTER, DVI, S-VIDEO DUAL-CHANNEL LVDS
23	LMU, LIGHT SENSOR, BOOTBANGER, SLEEP LED SPIDEY - KBD,TPAD,HALL EFFECT,PWR BUTTON
24	INTERNAL CONNECTORS - DVD, CARDSLOT, HARD DRIVE, LEFT USB/BLUETOOTH
25	FAN CONTROLLER, MODEM, SOUND SERIAL DEBUG (JOLLY ROGER, PWR/NMI/RESET)
26	USB 2.0
27	MARVELL GIGABIT ETHERNET PHY
28	FIREWIRE A/B PHY
29	FIREWIRE A/B CONNECTORS, PORT POWER LIMITER
30	PMU (POWER MANAGEMENT UNIT)
31	BATTERY CHARGER AND CONNECTOR
32	12.8V SYSTEM POWER SUPPLY / PMU POWER SUPPLY
33	3.3V / 5V SYSTEM POWER SUPPLIES
34	CPU CORE VOLTAGE POWER SUPPLY
35	1.5V/ 1.8V / 2.5V SYSTEM POWER SUPPLIES
36	SIGNAL CONSTRAINTS (1 OF 3) - DIGITAL/CLK
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39	FUNCTIONAL TEST POINTS
40	REVISION HISTORY (1 OF 1)
41-42	SIGNAL NAMES
43-44	COMPONENT LOCATIONS

BOM OPTIONS	STUFF	NO STUFF
D3_HOT		✓
D3_COLD	✓	
GPU_SS	✓	
GPU_SWITCH	✓	
SERIAL_DEBUG		✓
VCORE_OFFSET	✓	
1_8V_MAXBUS	✓	
1_5V_MAXBUS		✓
NEC_USB	✓	
INTREPID_USB		✓
BBANG		✓
NO_BBANG	✓	
ATI_MEMIO_HI	✓	
ATI_MEMIO_LO		✓
SSCG		✓
NO_SSCG	✓	
5V_HD_LOGIC	✓	
3V_HD_LOGIC		✓
EXT_TMDS	✓	
INT_TMDS		✓
NO_4XVCORE	✓	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6459	1	SCHEM,MLB,PB17 INCH	SCH1	
820-1524	1	PCBF,MLB,PB17 INCH	PCB1	

DIMENSIONS ARE IN MILLIMETERS
XX ± _____
X.XX ± _____
X.XXX ± _____
ANGLES ± _____
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

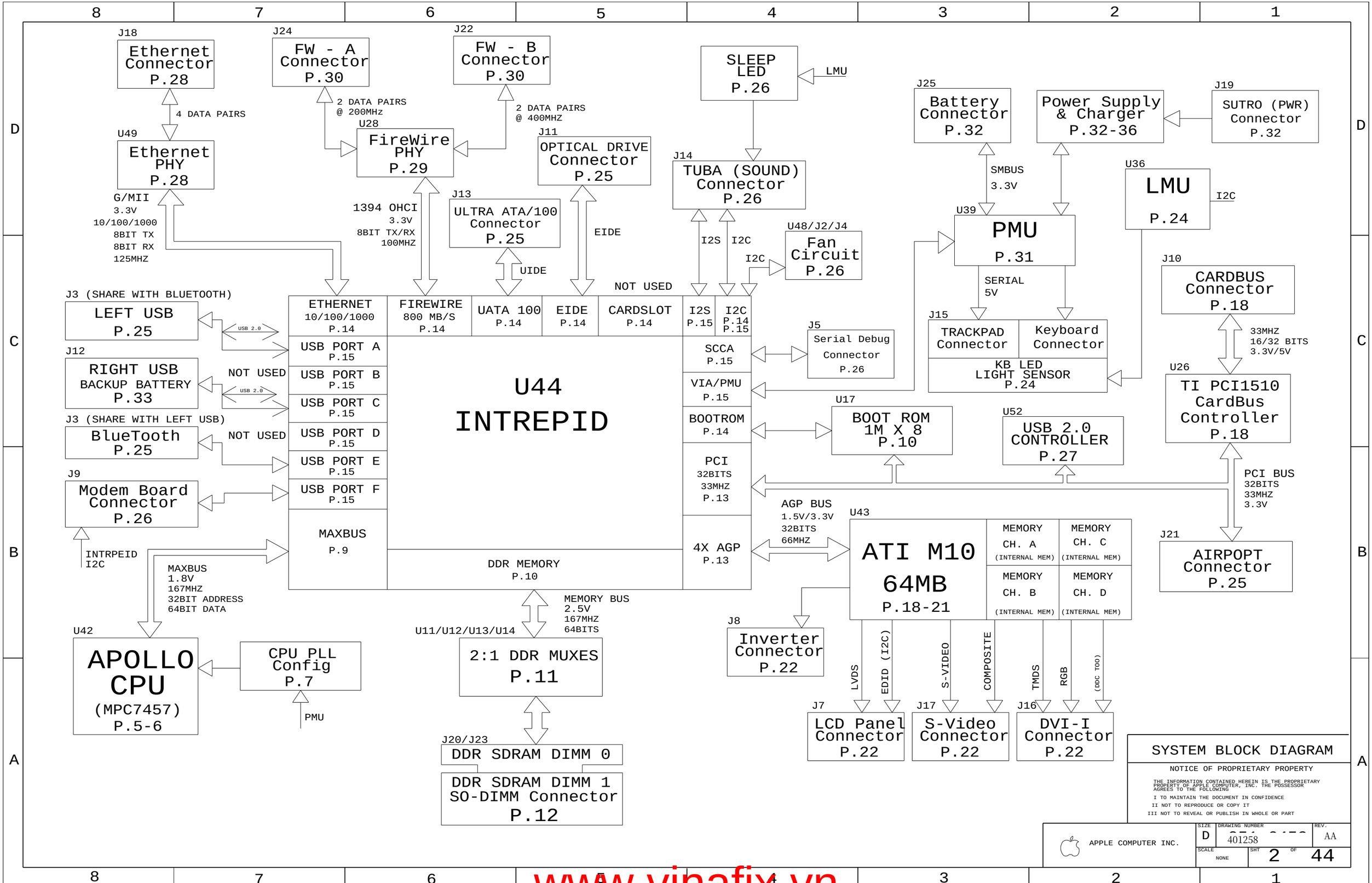
MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer Inc.

TITLE
SCHEM,MLB,PB17 INCH

DRAWING NUMBER 401258
REV. AA
SHT 1 OF 44



POWER SYSTEM ARCHITECTURE

AC ADAPTER IN PG 31

INRUSH LIMITER PG 30

+24V_PBUS

1V20_REF

U21 PG 31

>~13.44V TURNS-ON
<~13.44V SHUTS-OFF

RUN/SS

BUCK REGULATOR (LTC1625) PG 32

VCC

AC: 12.8V
NO AC: BATTERY VOLTAGE 1625 NOT RUNNING

SHUTDOWN: RUNNING
SLEEP: RUNNING
RUN: RUNNING

+PBUS (12.8V)

14V_PBUS

+3V_PMU LDO PG 32

+BATT

+5V_MAIN

+3V_PMU

+4_6V_BU

RC AT 1M*0.047UF @ 24V
STARTS 2.0MSEC AFTER DCDC_EN_L BECOMES LOW

RUN/SS - 5V
TURNS ON AT >1V
<100UA ALLOWED
INTERNAL ZENER CLAMP TO 6V

MAIN 3V/5V DC/DC (LTC3707) PG 33

VCC

STBYMD

PGOOD

SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING

INTERNAL ZENER CLAMP TO 6V
<100UA ALLOWED
TURNS ON AT >1V
RUN/SS - 3V

+5V_MAIN

3V_5V_OK

HOLDS BOTH RUN/SS AT GND WHEN IT'S CONNECTED TO GND

TURNS CONTROL TO RUN/SS WHEN IT'S OPEN

+3.3V_MAIN

RC AT 1M*0.1UF @ 24V
STARTS ~4.25MSEC AFTER DCDC_EN_L BECOMES LOW

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

+24V_PBUS

BACKUP BATTERY

+PBUS

12.8V CHARGES BACKUP BATTERY

24V IS OUTPUT ONLY FROM BACKUP BATTERY

CHARGER INPUT & BOOST OUTPUT PG 32

BACKUP BATTERY CIRCUIT CHARGES OFF +PBUS
AND PREVENTS +PBUS AND +24V_PBUS FROM DROPPING BELOW 6V
(UNTIL DRAINED)

BATTERY CHARGER (MAX1772) PG 31

+BATT

3S 3P PRISMATIC CELLS

DC/DC (LTC3411) PG 35

+1.8V_MAIN

MAXBUS BROADCOM

SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

BATTERY VOLTAGE FEED-IN PATH PG 31

+PBUS

BACKLIGHT INVERTER

+5V_MAIN

VCC

MAIN 2.5V/1.5V DC/DC (MAX1715) PG 35

PGOOD

SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING

TURNS ON OUTPUT @ 2.4V
ON1/ON2

MAP31 DDR I/O
MAP31 DDR CORE
DDR POWER

+2.5V_MAIN

1_5V_2_5V_OK

+1.5V_MAIN

INTREPID CORE
AGP I/O

DCDC_EN_L

AFTER PMU IS UP AND RUNNING
DCDC_EN_L WILL PULL ON1/ON2
LOW IN SHUTDOWN

+PBUS (12.8V)

+5V_MAIN

EXT_VCC

VCC

DC/DC (LTC1778) PG 20

SHUTDOWN: STOPPED
SLEEP: D3HOT/D3COLD
RUN: RUNNING

TURNS ON AS LOW AS 0.8V/TYP 1.5V
INTERNAL 1.2UA CURRENT SOURCE

RUN/SS

GPU_VCORE +1.2V/+1.0V

DCDC_EN

SLEEP

D3_COLD

GPU_VCORE SEQUENCING

1M & 0.1UF @14V, IT TAKES ~5.88MS TO START SWITCHER

1_5V_2_5V_OK

D3_HOT

DCDC_EN_L

D3_HOT

1_5V_2_5V_OK WILL NOT PULL LOW UNTIL +5V_MAIN TURNS ON

HOWEVER, 5V SHOULD TURN ON ~2.23MS AFTER DCDC_EN_L OR PMU_POWERUP_L BECOMES '1'; MUCH LESS THAN THE RC CHARGING AT INT_VCC (5V)

+PBUS

DCDC_EN

SLEEP

MAXBUS SEQUENCING

+5V_MAIN

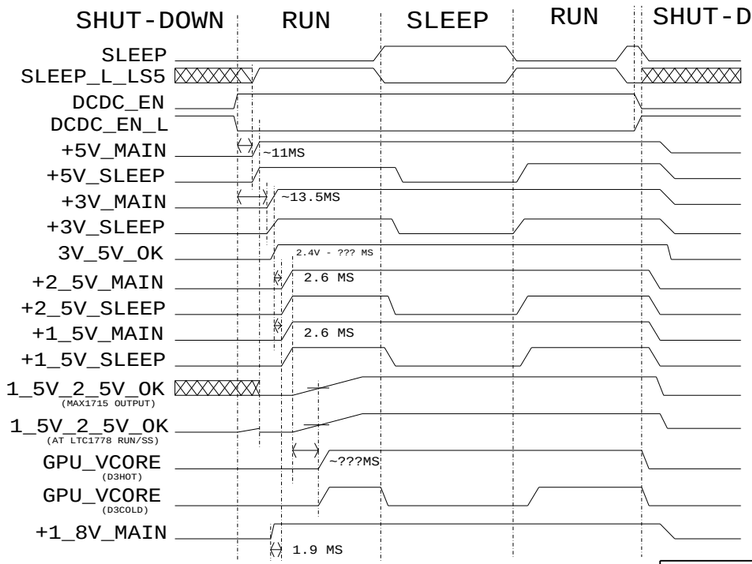
VCC

SHDN

DC/DC (MAX1717) PG 34

SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING

CPU_VCORE (+1.4V/+1.5V)



POWER BLOCK DIAGRAM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401258	AA

SCALE: NONE

SHT 3 OF 44

PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 12
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

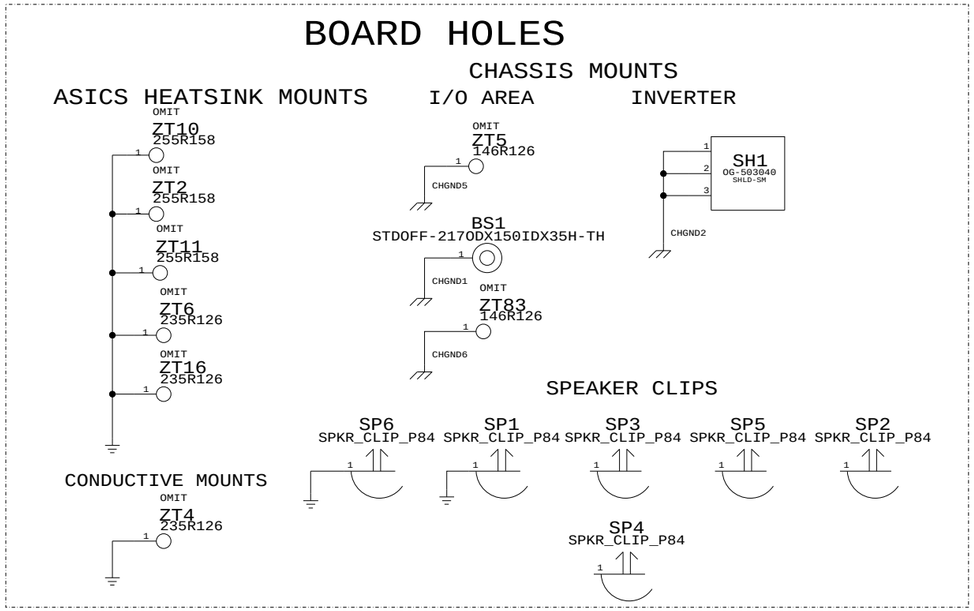
SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

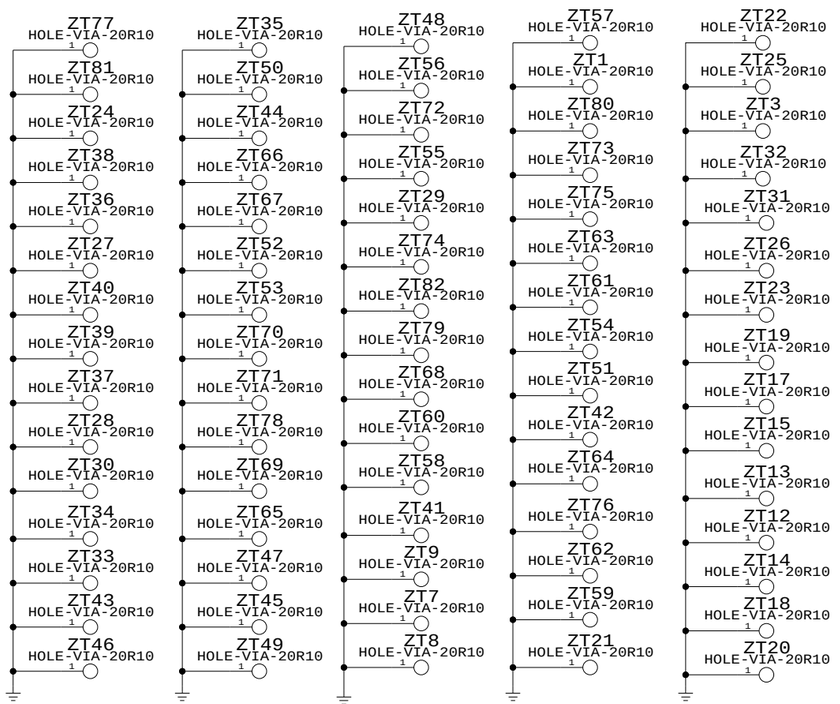
20R10 TH VIA OR VIA IN PAD

1		SIGNAL (1/3 OZ + COPPER PLATING)
2	PREPREG (3MIL)	GROUND (1/2 OZ)
3	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
4	PREPREG (3MIL)	SIGNAL (1/2 OZ)
5	LAMINATE (4MIL)	GROUND (1/2 OZ)
6	PREPREG (2MIL)	CUT POWER PLANE(1 OZ)
7	LAMINATE (3MIL)	CUT POWER PLANE(1 OZ)
8	PREPREG (2MIL)	GROUND (1/2 OZ)
9	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
10	PREPREG (3MIL)	SIGNAL (1/2 OZ)
11	LAMINATE (4MIL)	GROUND (1/2 OZ)
12	PREPREG (3MIL)	SIGNAL (1/3 OZ + COPPER PLATING)

BOARD HOLES



GROUND VIAS



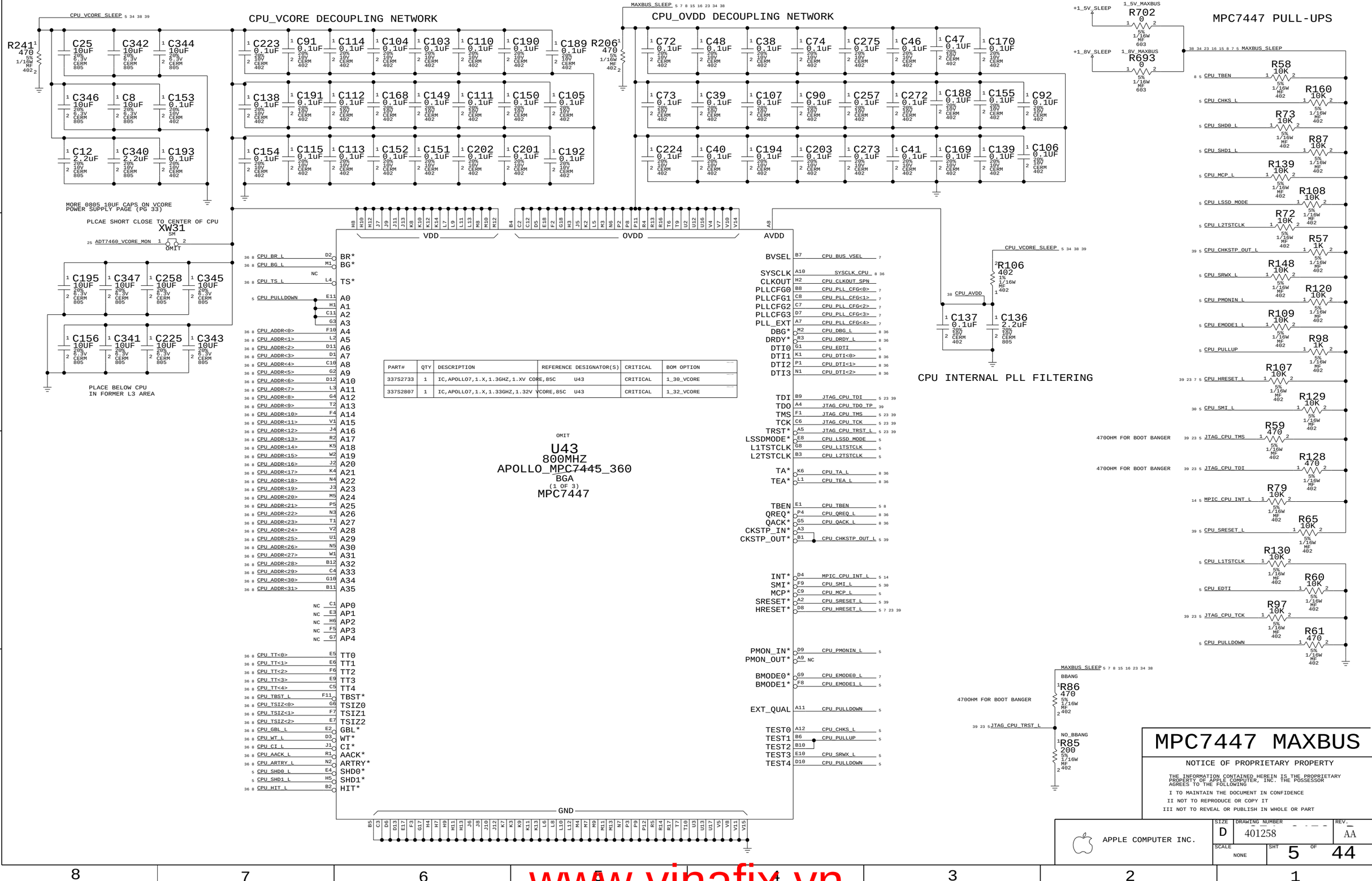
BOARD INFORMATION

APPLE COMPUTER INC.

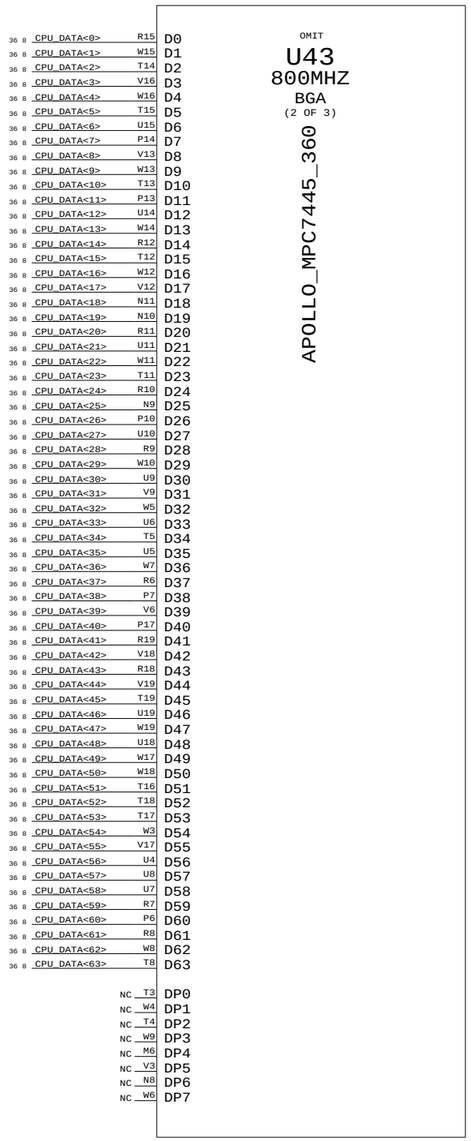
SIZE	DRAWING NUMBER	REV.
D	401258	AA

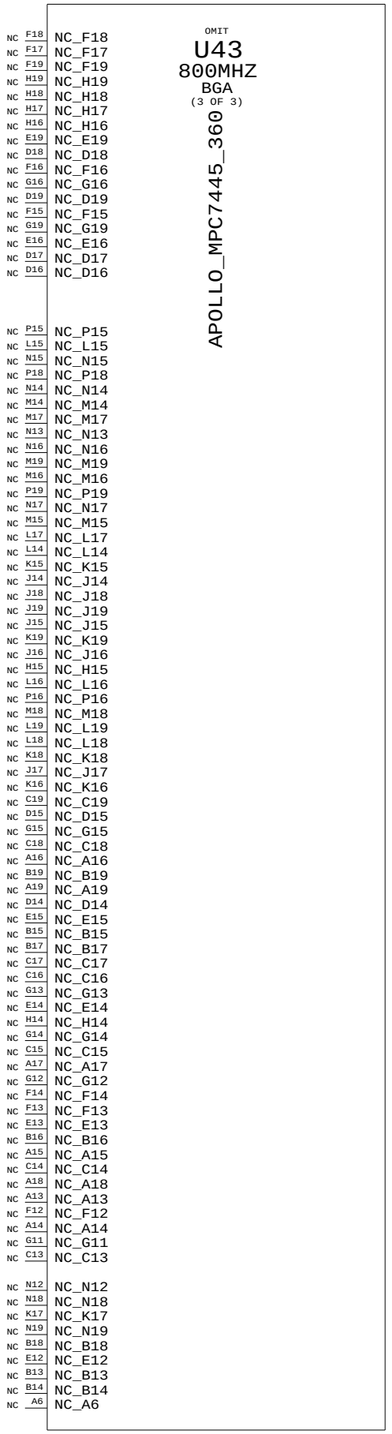
SCALE: NONE

SHT 4 OF 44



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S2733	1	IC,APOLLO7,1.X,1.3GHZ,1.XV CORE,85C	U43	CRITICAL	1_30_VCORE
337S2807	1	IC,APOLLO7,1.X,1.33GHZ,1.32V VCORE,85C	U43	CRITICAL	1_32_VCORE





BOOT BANGER - LMU PERORMS THIS FUNCTION IF NEEDED
SEE PAGE 22

MPC7447/BBANG

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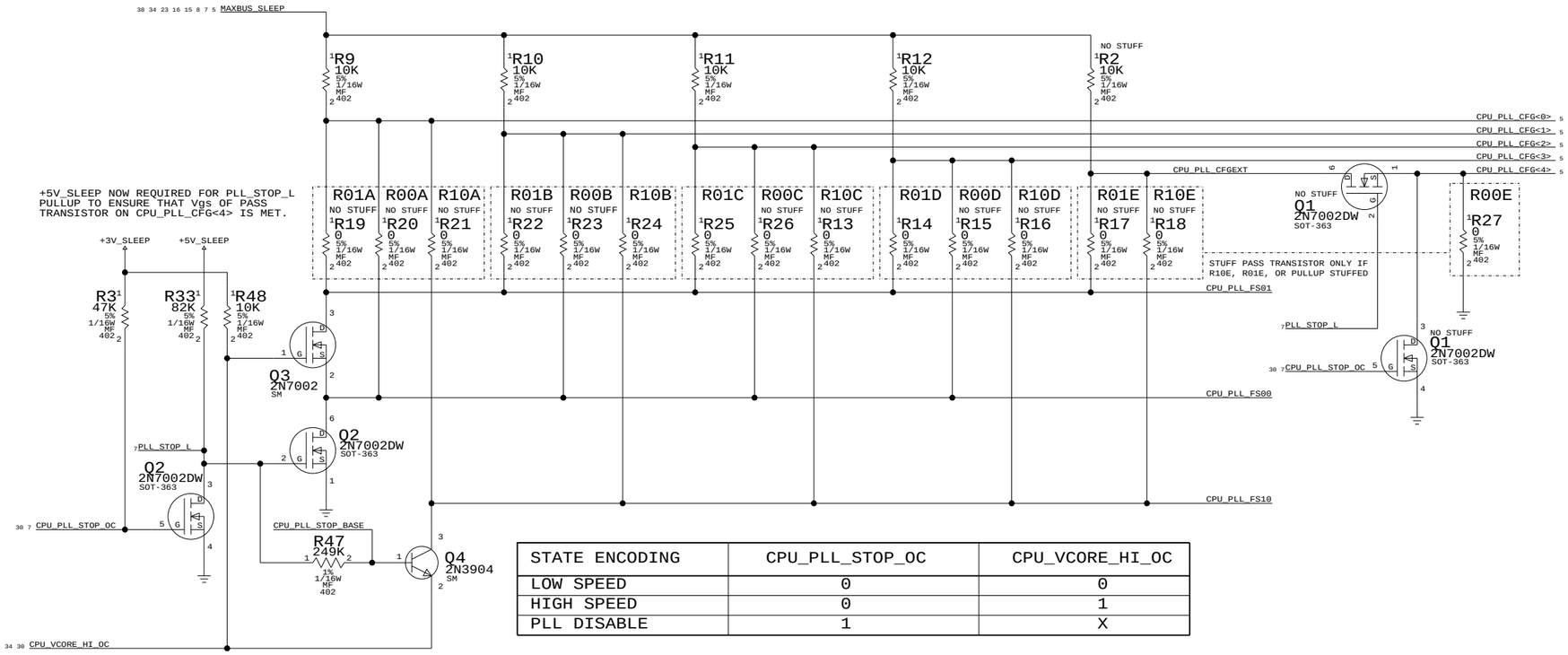
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401258	AA

SCALE	SHT	OF
NONE	6	44

CPU PLL CONFIG CIRCUITRY



STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

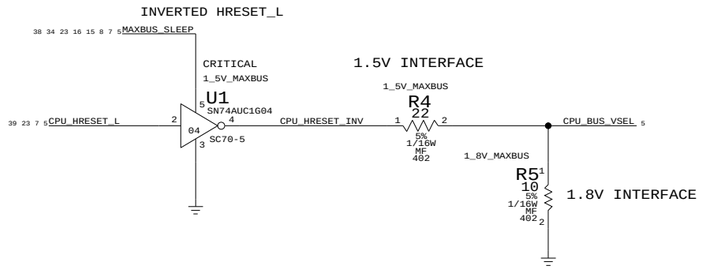
CPU FREQUENCY CONFIGURATION

APOLLO 7

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ (MHZ)	133MHZ (MHZ)	CPU_PLL_CFG 4 (HEX)	0123 ABCD (HEX)
0.0X	PLL OFF		0	1111 0F
1.0X	PLL BYPASS		0	0011 03
2.0X	333	267	0	0100 04
3.0X	500	400	0	1000 08
4.0X	667	533	0	1010 0A
5.0X	833	667	0	1011 0B
5.5X	917	733	0	1001 09
6.0X	1000	800	0	1101 0D
6.5X	1083	867	0	0101 05
7.0X	1167	933	0	0010 02
7.5X	1250	1000	0	0001 01
8.0X	1333	1067	0	1100 0C
8.5X	1417	1133	0	0110 06
9.0X	1500	1200	1	0111 17
9.5X	1583	1267	0	0111 07
10.0X	1667	1333	1	1010 1A
10.5X	1750	1400	1	1000 18
11.0X	1833	1467	1	1001 19
11.5X	1917	1533	0	0000 00
12.0X	2000	1600	1	1011 1B
12.5X	2083	1667	1	1111 1F
13.0X	2167	1733	1	0101 15
13.5X	2250	1800	0	1110 0E
14.0X	2333	1867	1	1100 1C
15.0X	2500	2000	1	0001 11
16.0X	2667	2133	1	1101 1D
17.0X	2833	2267	1	0000 10
18.0X	3000	2400	1	0010 12
20.0X	3333	2667	1	0011 13
21.0X	3500	2800	1	0100 14
24.0X	4000	3200	1	0110 16
28.0X	4667	3733	1	1110 1E

CPU CONFIGURATION

MAXBUS VSEL



DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L NEED TO CHARACTERIZE

BUSTYPE SELECT

APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

CPU CONFIGURATION

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 401258 | REV. AA | SCALE NONE | SHT 7 OF 44

INTREPID BOOT STRAPS

BIT 32 TO 39

38 34 23 16 15 8 7 5 MAXBUS_SLEEP

NO STUFF R642[1] 10K 5% 1/16W MF 402	NO STUFF R135[1] 10K	NO STUFF R123[1] 10K	NO STUFF R153[1] 10K	NO STUFF R166[1] 10K	NO STUFF R179[1] 10K	NO STUFF R651[1] 10K	NO STUFF R178[1] 10K
36 8 6 CPU_DATA<32>	36 8 6 CPU_DATA<33>	36 8 6 CPU_DATA<34>	36 8 6 CPU_DATA<35>	36 8 6 CPU_DATA<36>	36 8 6 CPU_DATA<37>	36 8 6 CPU_DATA<38>	36 8 6 CPU_DATA<39>
R136[1] 10K	R643[1] 10K	R639[1] 10K	R657[1] 10K	R664[1] 10K	R673[1] 10K	R143[1] 10K	R674[1] 10K
0: TDI, TDO monitor(JTAG) 1: TDI, TDO output	0: Analyzerclk_En_h Active 1: Inactive	0: DDR_ref_pol Active high 1: Active low	0: ExtPLL_SDwn_Pol Active high 1: Active low	Spare	Spare	Spare	Spare

BIT 40 TO 47

38 34 23 16 15 8 7 5 MAXBUS_SLEEP

NO STUFF R122[1] 10K	NO STUFF R142[1] 10K	NO STUFF R164[1] 10K	SSCG R134[1] 10K	NO STUFF R184[1] 10K	NO_SSCG R177[1] 10K	NO_SSCG R152[1] 10K	NO_SSCG R165[1] 10K
36 8 6 CPU_DATA<40>	36 8 6 CPU_DATA<41>	36 8 6 CPU_DATA<42>	36 8 6 CPU_DATA<43>	36 8 6 CPU_DATA<44>	36 8 6 CPU_DATA<45>	36 8 6 CPU_DATA<46>	36 8 6 CPU_DATA<47>
R640[1] 10K	R652[1] 10K	R665[1] 10K	NO_SSCG R644[1] 10K	R683[1] 10K	SSCG R675[1] 10K	SSCG R658[1] 10K	SSCG R666[1] 10K
Spare	Spare	BIT2	BIT1	BIT0	0: Internal Spread En Active 1: Inactive	0: PCI1 Source Clock PLL4 (NO SPREAD)	0: PCI0 Source Clock PLL5 (NO SPREAD)

PLL4MODESEL_NXT[2:0]
000: 166.4MHZ (2.5X)
001: 149.76MHZ
010: 133.12MHZ (2.0X)
011: 99.84MHZ (1.5X)
100: 83.20MHZ

MODE A (2.5X) IS FOR STATIC OPERATION
MODE C (2.0X) IS FOR CLOCK SLEW OPERATION

BIT 48 TO 55

38 34 23 16 15 8 7 5 MAXBUS_SLEEP

SSCG R133[1] 10K	SSCG R121[1] 10K	NO STUFF R163[1] 10K	NO STUFF R151[1] 10K	NO STUFF R162[1] 10K	NO STUFF R141[1] 10K	NO STUFF R183[1] 10K	NO STUFF R176[1] 10K
36 8 6 CPU_DATA<48>	36 8 6 CPU_DATA<49>	36 8 6 CPU_DATA<50>	36 8 6 CPU_DATA<51>	36 8 6 CPU_DATA<52>	36 8 6 CPU_DATA<53>	36 8 6 CPU_DATA<54>	36 8 6 CPU_DATA<55>
NO_SSCG R645[1] 10K	NO_SSCG R641[1] 10K	NO STUFF R668[1] 10K	R659[1] 10K	R667[1] 10K	R653[1] 10K	NO STUFF R684[1] 10K	R676[1] 10K
0: BUF_REF_CLK_OUTEnable_h Inactive 1: Active	0: SelPLLdefaultSrc Internal source 1: External source	Spare	0: TI 1394b workaround 1: TI PHY workaround	Spare	BIT2	BIT1	BIT0

MaxBus output impedance
111: 28.6 ohm
011: 33.3 ohm
101: 40 ohm
001: 50 ohm
110: 66.6 ohm
010: 100 ohm
100: 200 ohm
000: 200 ohm

38 14 12 +1_5V_INTREPID_PLL — R227 4.7 5% 1/16W MF 402 — 38 +1_5V_INTREPID_PLL7

C308 0.22UF 20% 6.3V CERM 402

H26 VDD15A_7 (PLL6) CRITICAL

U45 INTREPID-REV2.1 BGA

(1 OF 9)

36 8 5 CPU_BR_L	E29	BR	INPUT
36 8 5 CPU_BG_L	E26	BG	NO BUS KEEPER
36 8 5 CPU_TS_L	B27	TS	NO BUS KEEPER

MAXBUS INTERFACE

36 5 CPU_ADDR<0>	D24	A_0	
36 5 CPU_ADDR<1>	D25	A_1	
36 5 CPU_ADDR<2>	A27	A_2	
36 5 CPU_ADDR<3>	E24	A_3	
36 5 CPU_ADDR<4>	G23	A_4	
36 5 CPU_ADDR<5>	B26	A_5	
36 5 CPU_ADDR<6>	A26	A_6	
36 5 CPU_ADDR<7>	D23	A_7	
36 5 CPU_ADDR<8>	A25	A_8	
36 5 CPU_ADDR<9>	E23	A_9	
36 5 CPU_ADDR<10>	J22	A_10	
36 5 CPU_ADDR<11>	B25	A_11	
36 5 CPU_ADDR<12>	H22	A_12	
36 5 CPU_ADDR<13>	G22	A_13	
36 5 CPU_ADDR<14>	D22	A_14	
36 5 CPU_ADDR<15>	B24	A_15	
36 5 CPU_ADDR<16>	B23	A_16	
36 5 CPU_ADDR<17>	E22	A_17	
36 5 CPU_ADDR<18>	J21	A_18	
36 5 CPU_ADDR<19>	G21	A_19	
36 5 CPU_ADDR<20>	E21	A_20	
36 5 CPU_ADDR<21>	A24	A_21	
36 5 CPU_ADDR<22>	D21	A_22	
36 5 CPU_ADDR<23>	A23	A_23	
36 5 CPU_ADDR<24>	H20	A_24	
36 5 CPU_ADDR<25>	B22	A_25	
36 5 CPU_ADDR<26>	H21	A_26	
36 5 CPU_ADDR<27>	A22	A_27	
36 5 CPU_ADDR<28>	E20	A_28	
36 5 CPU_ADDR<29>	B21	A_29	
36 5 CPU_ADDR<30>	D20	A_30	
36 5 CPU_ADDR<31>	A21	A_31	

36 5 CPU_CI_L	G26	CI	
36 5 CPU_GBL_L	A29	GBL	
36 5 CPU_TBST_L	A28	TBST	
36 5 CPU_TSIZ<0>	G24	TSIZ_0	
36 5 CPU_TSIZ<1>	H24	TSIZ_1	
36 5 CPU_TSIZ<2>	D26	TSIZ_2	
36 5 CPU_TT<0>	E25	TT_0	
36 5 CPU_TT<1>	G25	TT_1	
36 5 CPU_TT<2>	B28	TT_2	
36 5 CPU_TT<3>	D27	TT_3	
36 5 CPU_TT<4>	J25	TT_4	
36 5 CPU_WT_L	D28	WT	
36 8 5 CPU_AACK_L	B29	AACK	NO BUS KEEPER - PU
36 8 5 CPU_ARTRY_L	H23	ARTRY	NO BUS KEEPER - PU
36 8 5 CPU_HIT_L	B31	HIT	INPUT - PU
36 8 5 CPU_QREQ_L	A32	QREQ	INPUT - PD
36 5 CPU_QACK_L	G27	QACK	NO BUS KEEPER - ?
39 INT_SUSPEND_REQ_L	AK9	SUSPENDREQ	
39 INT_SUSPEND_ACK_L	AM8	SUSPENDACK	

Vin = Intrepid Vcore (1.5V)
Vout = MaxBus rail (1.8V)

FB BUFFER HAS 50 OHM OUTPUT IMPEDANCE

36 8 INT_CPUFB_IN	J24	CPU_FB_IN	
36 8 INT_CPUFB_OUT	H16	CPU_FB_OUT	NO BUS KEEPER - PU
SYSCLK_LA_TP	G8	ANALYZER_CLK	
36 CPU_CLK_EN	AH9	STOPCPUCLK	INPUT - PU
INTREPID_ACS_REF	H13	ACS_REF	NO BUS KEEPER - ?
36 SYSCLK_CPU_UF	J15	CPU_CLK	NO BUS KEEPER - ?
5 CPU_TBEN	A31	TBEN	NO BUS KEEPER - PU

INTREPID OUTPUTS HIGH BY DEFAULT

DBG	A30	CPU_DBG_L	5 8 36
DRDY	G28	CPU_DRDY_L	5 8 36
DTI_0	K25	CPU_DTI<0>	5 36
DTI_1	D29	CPU_DTI<1>	5 36
DTI_2	B30	CPU_DTI<2>	5 36
TA	E27	CPU_TA_L	5 8 36
TEA	E28	CPU_TEA_L	5 8 36

VSSA_7 (PLL6) H25

R197[1] 511 1% 1/16W MF 402

R144 0 5% 1/16W MF 402

R137[1] 1K 1% 1/16W MF 402

SHORT = 1" SHORTER THAN MATCHED LENGTH
LONG = 1" LONGER THAN MATCHED LENGTH

36 8 INT_CPUFB_OUT — R167 0 5% 1/16W MF 402 — 36 INT_CPUFB_OUT_SHORT — R215 0 5% 1/16W MF 402 — 36 INT_CPUFB_OUT_NORM — R207 NO STUFF 0 5% 1/16W MF 402 — 36 INT_CPUFB_LONG

R225[1] NO STUFF 0 5% 1/16W MF 402

R208[1] 0 5% 1/16W MF 402

R226 0 5% 1/16W MF 402

R196 NO STUFF 0 5% 1/16W MF 402

36 8 INT_CPUFB_IN — 36 INT_CPUFB_IN_NORM

THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:

1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
2/ D46 - SELPCI1SPREADCLK - SLEEP/WAKE CYCLE REQUIRED
3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT

IF A STRAP IS NOT LISTED, THEN
IT CANNOT BE CHANGED BY SOFTWARE

D_0	D10	CPU_DATA<0>	6 36
D_1	G12	CPU_DATA<1>	6 36
D_2	E11	CPU_DATA<2>	6 36
D_3	H11	CPU_DATA<3>	6 36
D_4	B9	CPU_DATA<4>	6 36
D_5	B8	CPU_DATA<5>	6 36
D_6	A9	CPU_DATA<6>	6 36
D_7	A8	CPU_DATA<7>	6 36
D_8	E12	CPU_DATA<8>	6 36
D_9	D11	CPU_DATA<9>	6 36
D_10	B10	CPU_DATA<10>	6 36
D_11	J13	CPU_DATA<11>	6 36
D_12	A10	CPU_DATA<12>	6 36
D_13	D12	CPU_DATA<13>	6 36
D_14	E13	CPU_DATA<14>	6 36
D_15	G13	CPU_DATA<15>	6 36
D_16	B11	CPU_DATA<16>	6 36
D_17	D13	CPU_DATA<17>	6 36
D_18	A11	CPU_DATA<18>	6 36
D_19	G14	CPU_DATA<19>	6 36
D_20	H14	CPU_DATA<20>	6 36
D_21	E14	CPU_DATA<21>	6 36
D_22	B12	CPU_DATA<22>	6 36
D_23	G15	CPU_DATA<23>	6 36
D_24	B13	CPU_DATA<24>	6 36
D_25	H15	CPU_DATA<25>	6 36
D_26	D14	CPU_DATA<26>	6 36
D_27	B14	CPU_DATA<27>	6 36
D_28	A12	CPU_DATA<28>	6 36
D_29	G16	CPU_DATA<29>	6 36
D_30	E15	CPU_DATA<30>	6 36
D_31	J16	CPU_DATA<31>	6 36
D_32	D15	CPU_DATA<32>	6 8 36
D_33	A14	CPU_DATA<33>	6 8 36
D_34	A13	CPU_DATA<34>	6 8 36
D_35	D16	CPU_DATA<35>	6 8 36
D_36	E16	CPU_DATA<36>	6 8 36
D_37	G17	CPU_DATA<37>	6 8 36
D_38	B15	CPU_DATA<38>	6 8 36
D_39	H17	CPU_DATA<39>	6 8 36
D_40	A15	CPU_DATA<40>	6 8 36
D_41	B16	CPU_DATA<41>	6 8 36
D_42	E17	CPU_DATA<42>	6 8 36
D_43	A16	CPU_DATA<43>	6 8 36
D_44	J18	CPU_DATA<44>	6 8 36
D_45	H18	CPU_DATA<45>	6 8 36
D_46	D17	CPU_DATA<46>	6 8 36
D_47	G18	CPU_DATA<47>	6 8 36
D_48	A17	CPU_DATA<48>	6 8 36
D_49	B17	CPU_DATA<49>	6 8 36
D_50	E18	CPU_DATA<50>	6 8 36
D_51	B18	CPU_DATA<51>	6 8 36
D_52	D18	CPU_DATA<52>	6 8 36
D_53	A18	CPU_DATA<53>	6 8 36
D_54	A19	CPU_DATA<54>	6 8 36
D_55	H19	CPU_DATA<55>	6 8 36
D_56	B19	CPU_DATA<56>	6 8 36
D_57	J19	CPU_DATA<57>	6 8 36
D_58	A20	CPU_DATA<58>	6 8 36
D_59	D19	CPU_DATA<59>	6 8 36
D_60	E19	CPU_DATA<60>	6 8 36
D_61	G19	CPU_DATA<61>	6 8 36
D_62	B20	CPU_DATA<62>	6 8 36
D_63	G20	CPU_DATA<63>	6 8 36

MAXBUS PULL-UPS

MAXBUS_SLEEP 5 7 8 15 16 23 34 38

36 8 5 CPU_TS_L	RP21 10K 2 7	36 8 5 CPU_TA_L	RP21 10K 1 8	36 8 5 CPU_ARTRY_L	RP21 10K 4 5	36 8 5 CPU_BR_L	RP23 10K 1 8
36 8 5 CPU_HIT_L	RP24 10K 3 6	36 8 5 CPU_DRDY_L	RP23 10K 3 6	36 8 5 CPU_TEA_L	RP23 10K 4 5	36 8 5 CPU_AACK_L	RP23 10K 2 7
36 8 5 CPU_DBG_L	RP24 10K 4 5	36 8 5 CPU_BG_L	RP21 10K 3 6	36 8 5 CPU_QREQ_L	RP24 10K 2 7		

All: 5% 1/16W SM1

INTREPID BOOT STRAPS

BIT 56 TO 63

38 34 23 16 15 8 7 5 MAXBUS_SLEEP

NO STUFF R140[1] 10K 5% 1/16W MF 402	NO STUFF R161[1] 10K	NO STUFF R175[1] 10K	NO STUFF R132[1] 10K	NO STUFF R131[1] 10K	NO STUFF R150[1] 10K	R174[1] 10K	NO STUFF R182[1] 10K
36 8 6 CPU_DATA<56>	36 8 6 CPU_DATA<57>	36 8 6 CPU_DATA<58>	36 8 6 CPU_DATA<59>	36 8 6 CPU_DATA<60>	36 8 6 CPU_DATA<61>	36 8 6 CPU_DATA<62>	36 8 6 CPU_DATA<63>
R654[1] 10K	R669[1] 10K	R677[1] 10K	R646[1] 10K	R647[1] 10K	R660[1] 10K	NO STUFF R678[1] 10K	R685[1] 10K
Spare	Spare	Spare	0: PCI1_REQ1_L / PCI1_GNT1_L 1: GPIO1	0: PCI1_REQ0_L / PCI1_GNT0_L 1: GPIO0	0: PCI1_REQ2_L / PCI1_GNT2_L 1: GPIO2	0: FirmWare PHY interface 1: Legacy interface	0: Host Bus Mode 1: 60x bus (G3)

Intrepid MaxBus

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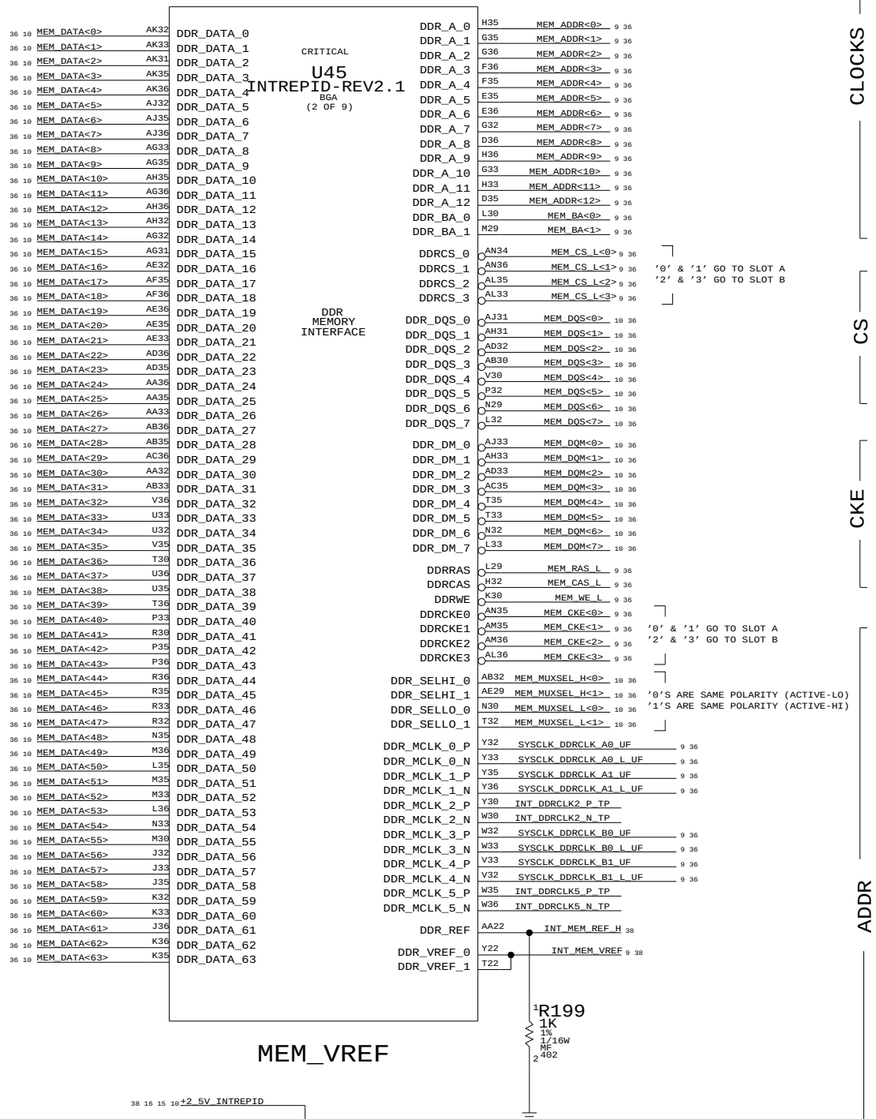
APPLE COMPUTER INC.

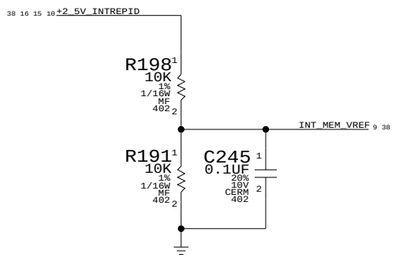
SIZE	DRAWING NUMBER	REV.
D	401258	AA
SCALE: NONE	SHT 8 OF 44	

SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

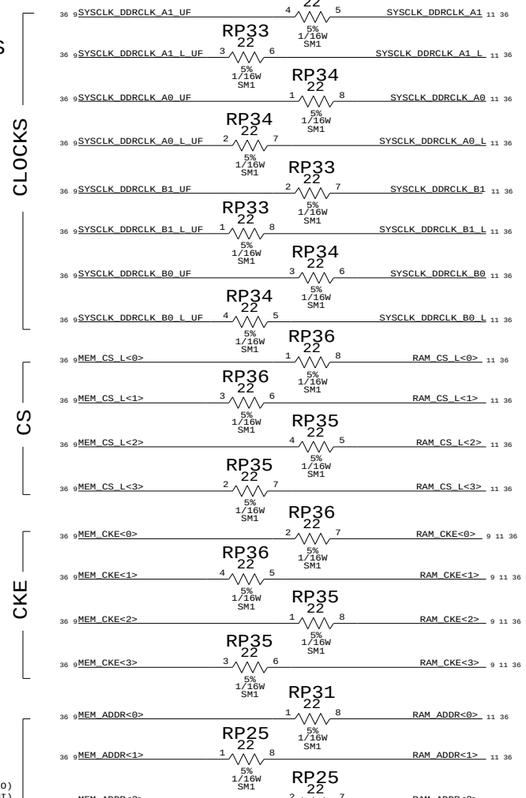
PINS ARE SWAPABLE FOR RPAKS



MEM_VREF



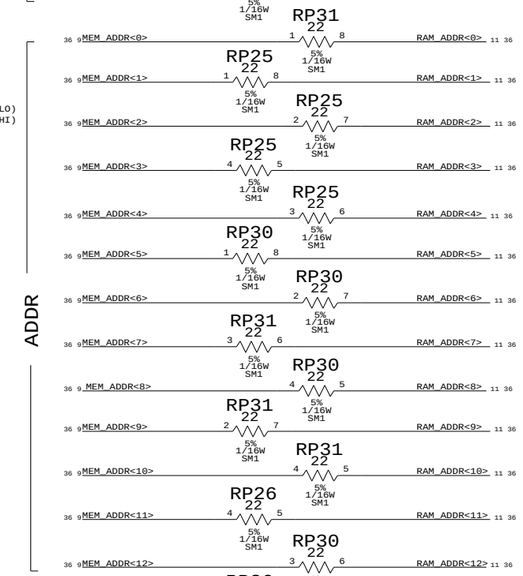
CLOCKS



CS

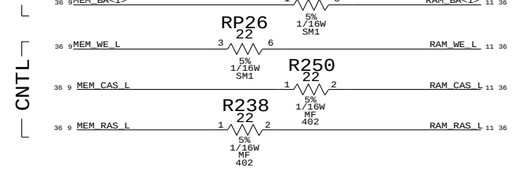
CKE

ADDR

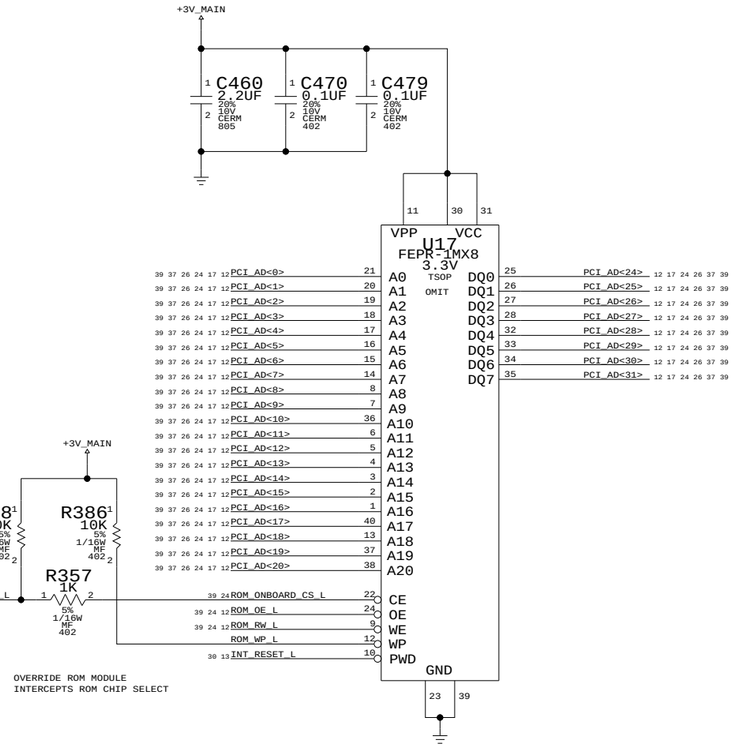


BA

CNTL



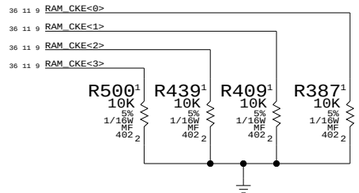
1MB BOOT ROM



OVERRIDE ROM MODULE
INTERCEPTS ROM CHIP SELECT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1255	1	BOOTROM,P84	U17	CRITICAL	?

PULL-DOWN RESISTORS TO ENSURE
CKE STAYS LOW AFTER INTREPID
2.5V I/O SHUTS OFF



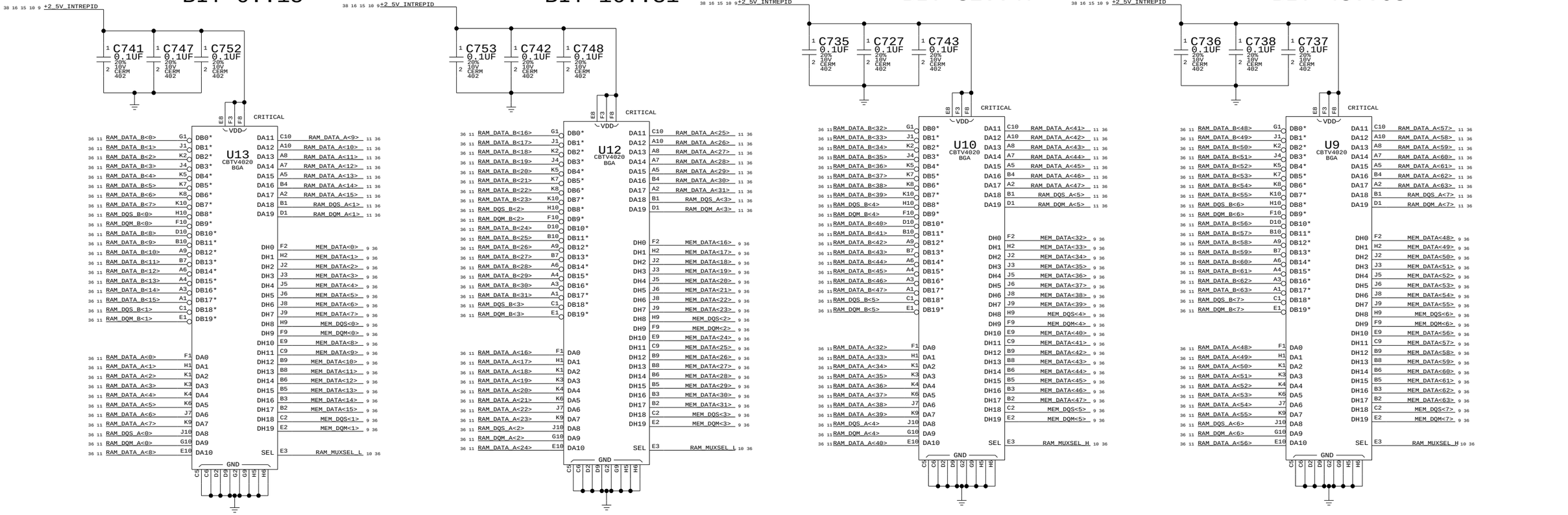
INT - DDR/BOOTROM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401258	AA

SCALE: NONE

SHT 9 OF 44



SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND
MEM_MUXSEL_H<0> AND MEM_MUXSEL_L<0> ARE ACTIVE LOW
MEM_MUXSEL_H<1> AND MEM_MUXSEL_L<1> ARE ACTIVE HIGH

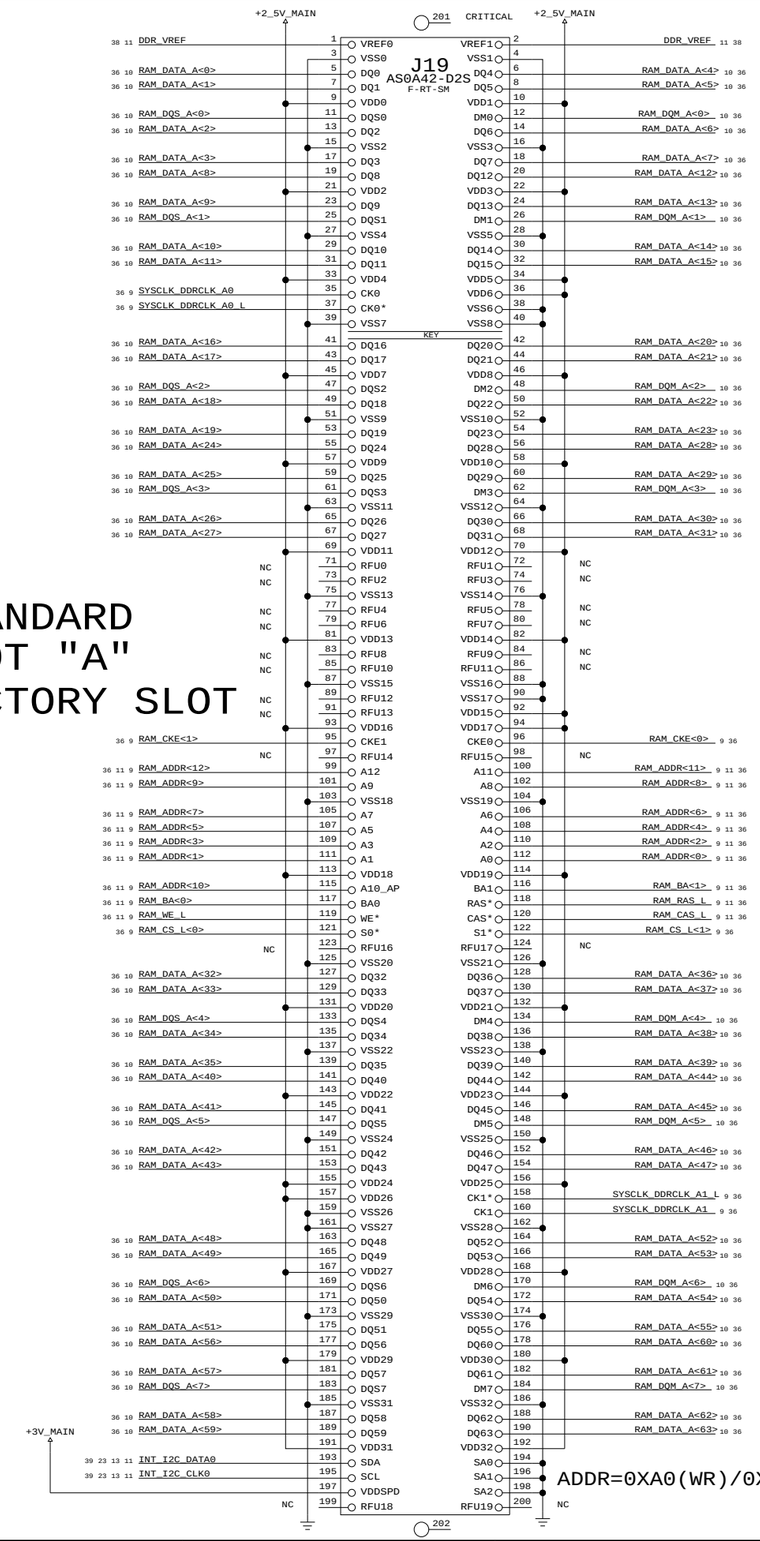
ADDED 0 OHM RESISTORS IN CASE POLARITY IS WRONG

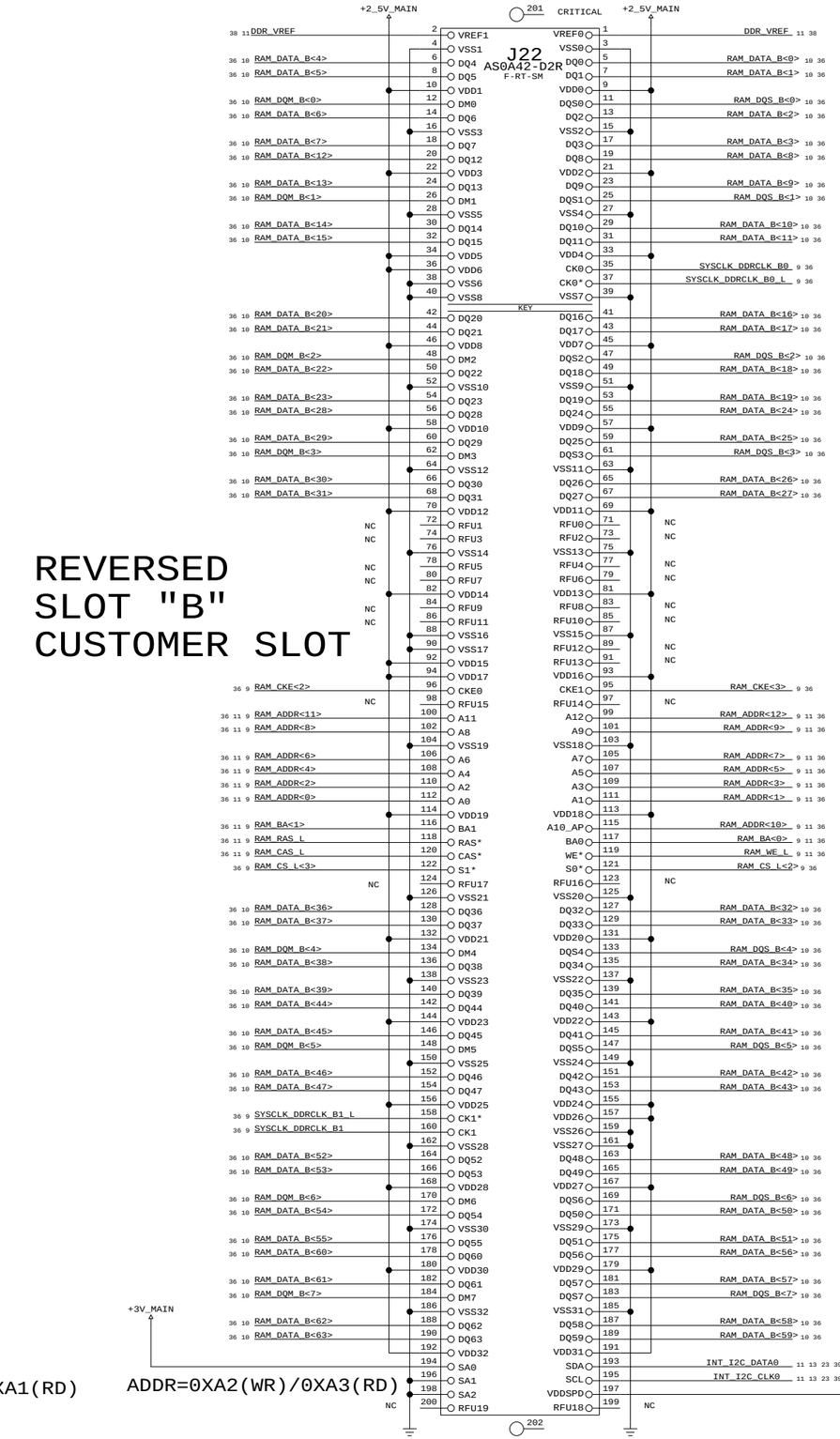
16BIT 2:1 DDR MUXES

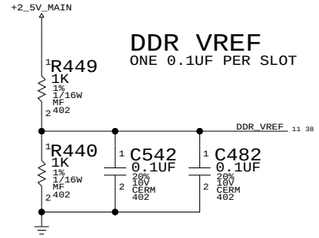
APPLE COMPUTER INC.

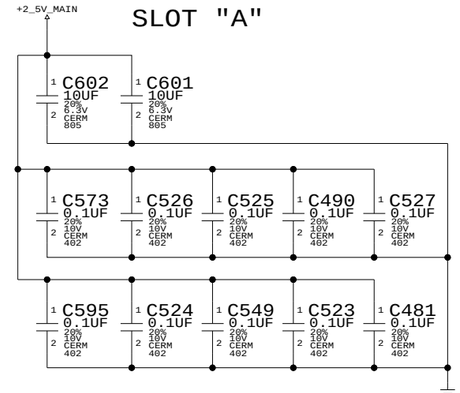
SIZE	DRAWING NUMBER	REV.
D	401258	AA

SCALE	SHT	OF
NONE	10	44

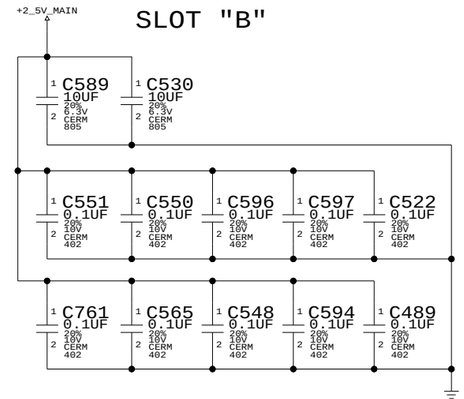








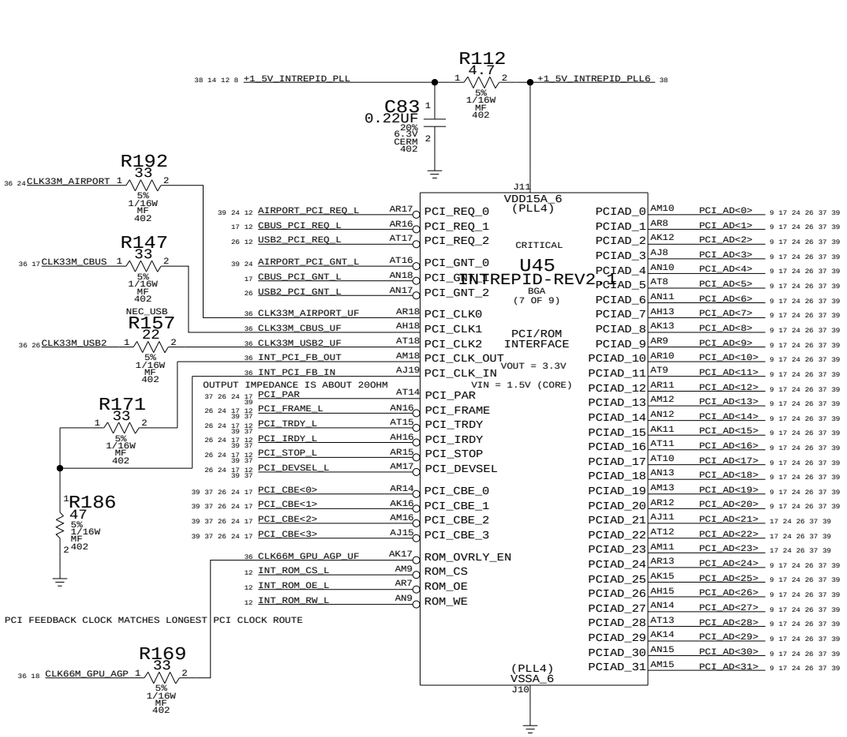
FOR RETURN CURRENT

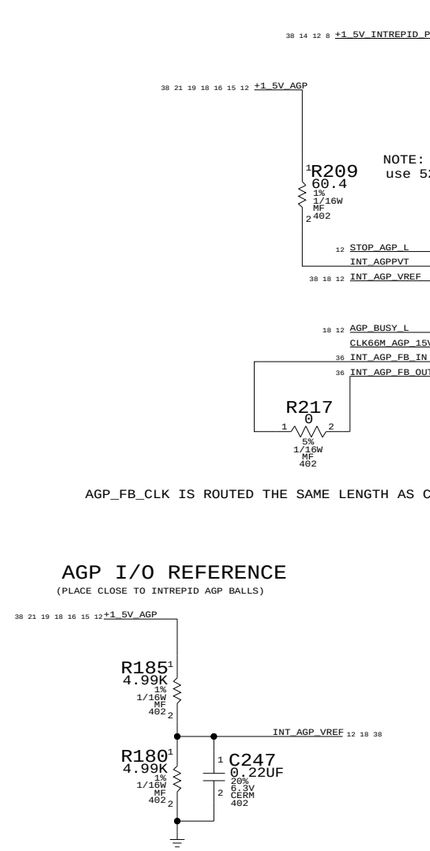


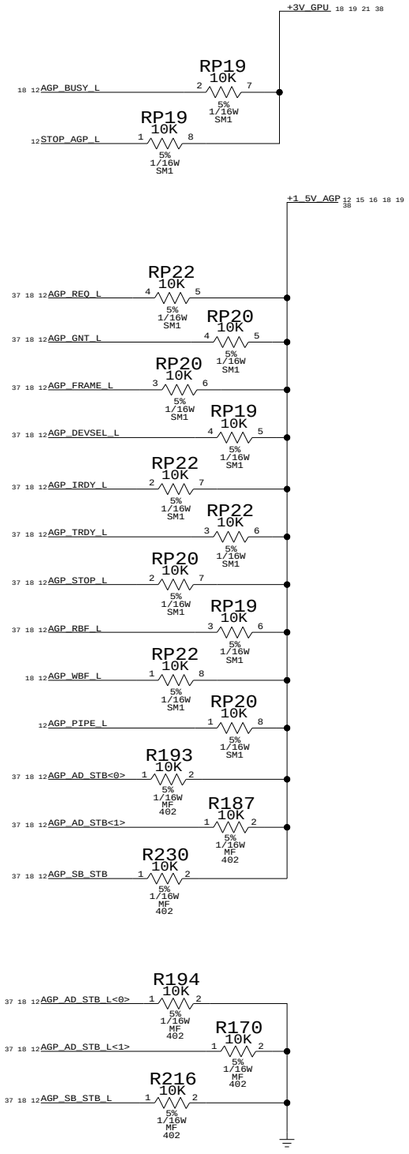
DDR SODIMM CONNS

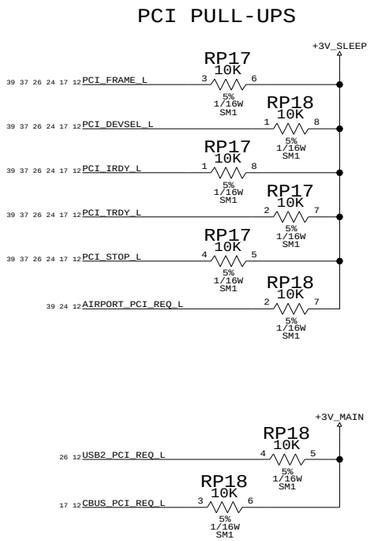
NOTICE OF PROPRIETARY PROPERTY

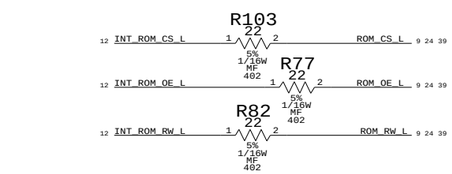
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 401258	REV. AA
	SCALE NONE	SHT 11 OF 44	











INTREPID AGP/PCI

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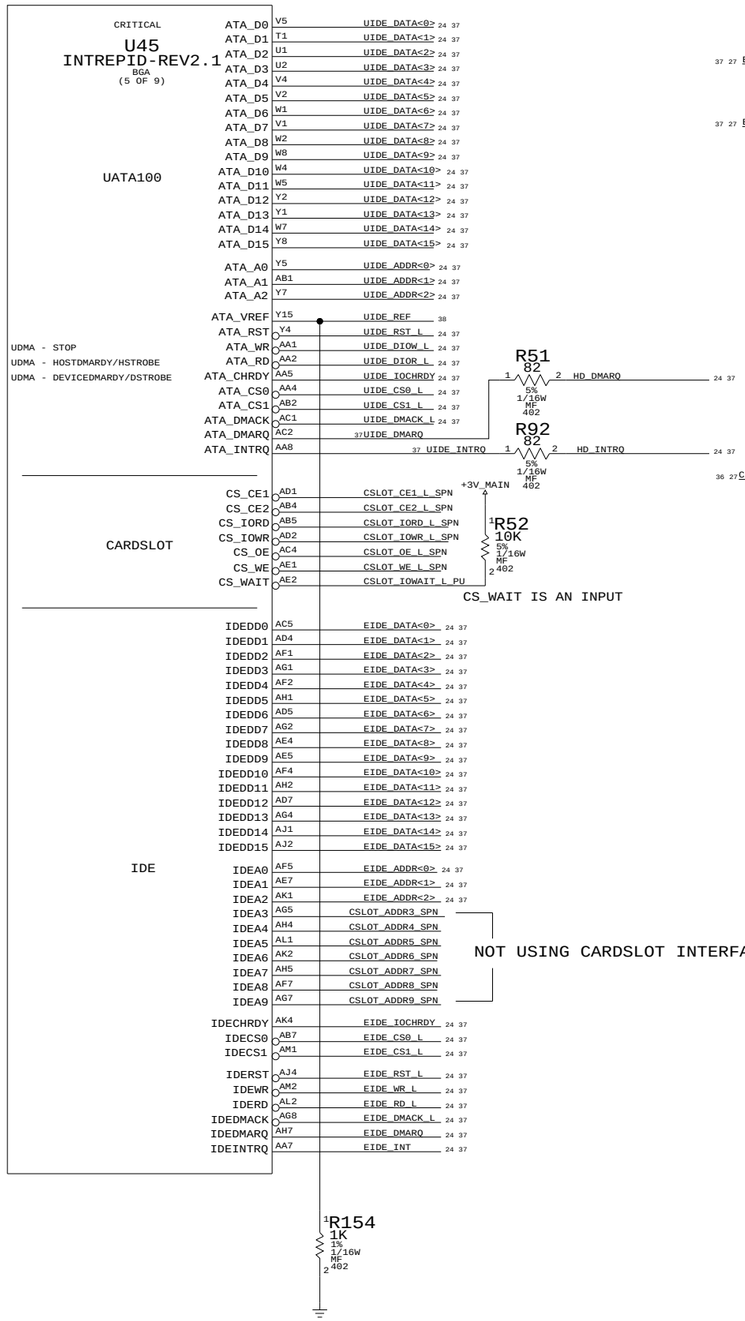
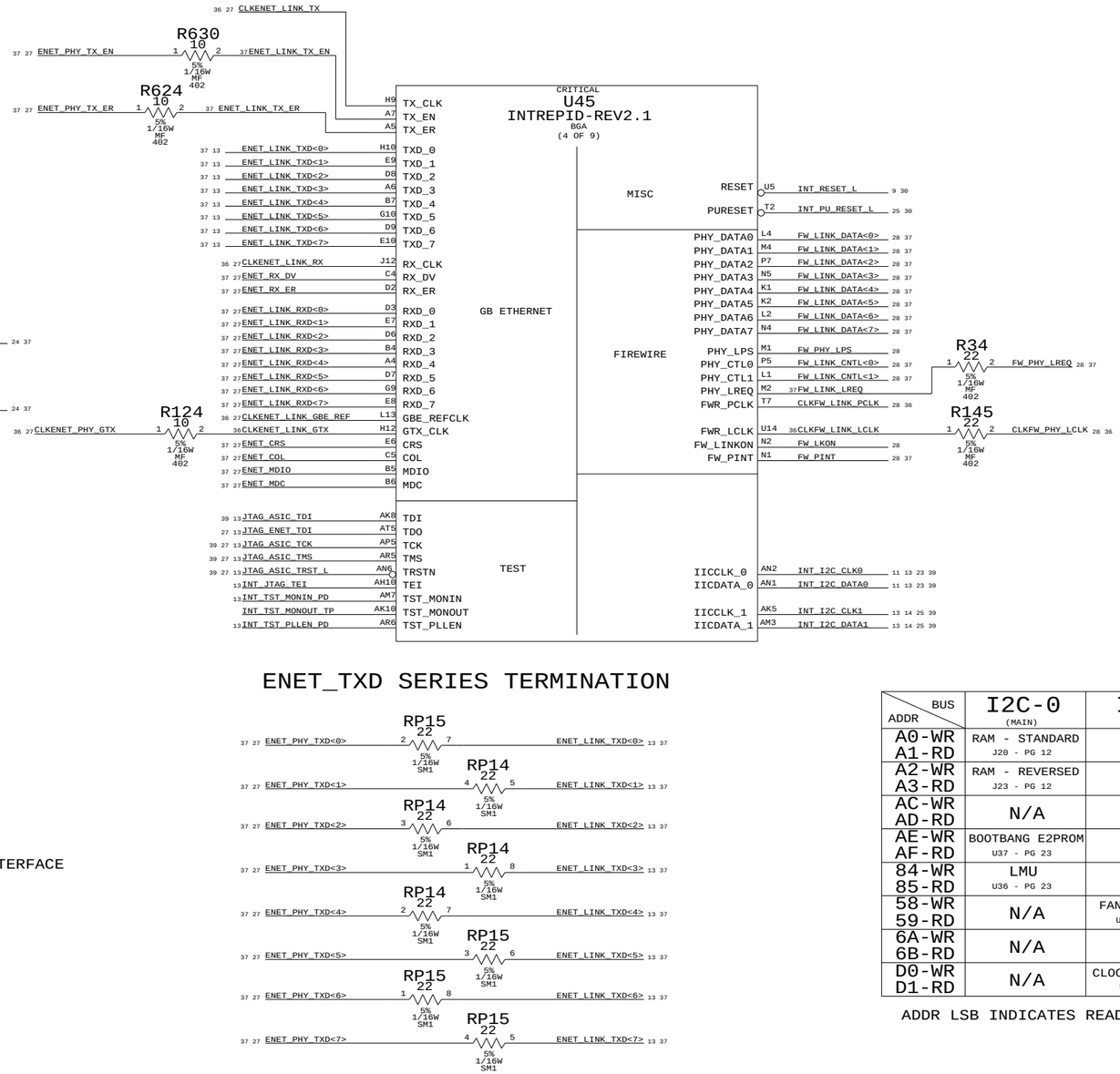
APPLE COMPUTER INC.

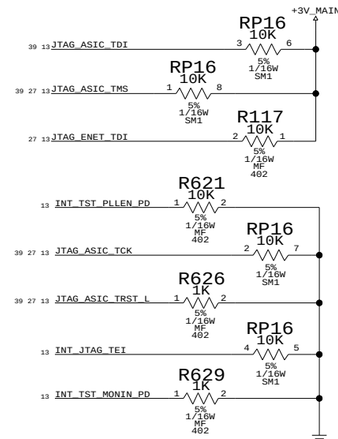
SIZE	DRAWING NUMBER	REV.
D	401258	AA

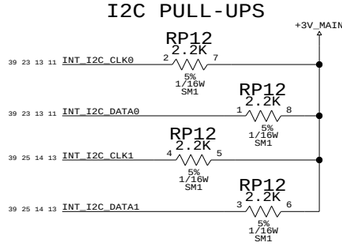
SCALE: NONE

SHT 12 OF 44









ENET_TXD SERIES TERMINATION

JTG_RSTN_L	TST_TEI_H	JTG_TDO_H (I/O)	JTG_TDI_H (I/O)	TST_PLLEN_H	ANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	EXTPLL SHUTDOWN (OUTPUT)	DDR_ TPDENABLE (OUTPUT)	0	(OUTPUT)	NORMAL OPERATION
0	0	(OUTPUT)	0(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	HWPLL_ TESTSEL5 (INPUT)	1(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0(I)	0(I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0(I)	1(I)	0	X(I)	ATPG IDDQ
0	1	0(I)	1(I)	1	X(I)	TEST TRI-STATE
0	1	1(I)	0(I)	0	X(I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1(I)	0(I)	1	X(I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1(I)	1(I)	X	X(I)	FUNCTIONAL TEST IDDQ

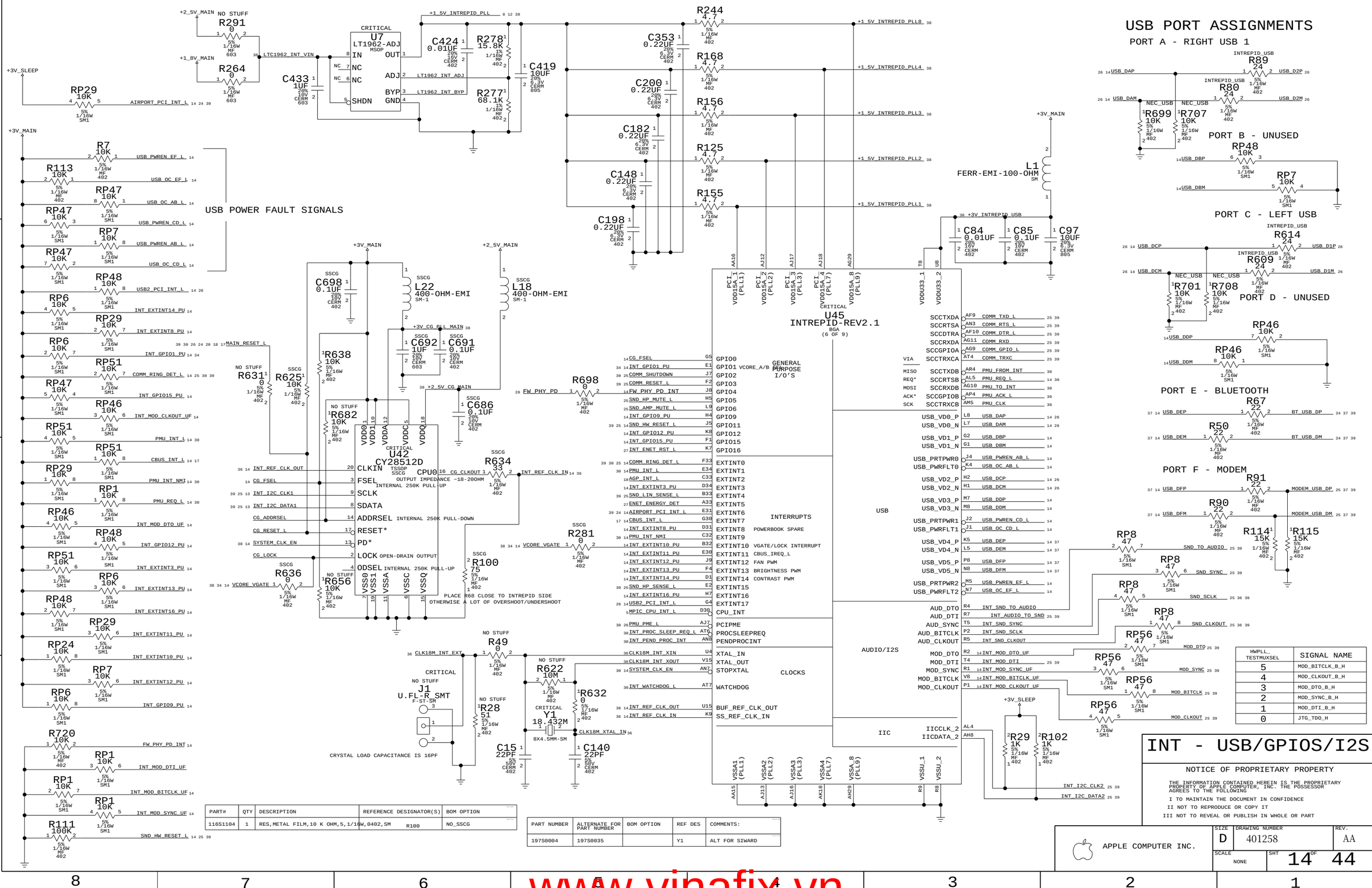
BUS / ADDR	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
A0-WR A1-RD	RAM - STANDARD J20 - PG 12	N/A	N/A	N/A
A2-WR A3-RD	RAM - REVERSED J23 - PG 12	N/A	N/A	N/A
AC-WR AD-RD	N/A	N/A	DASH MODEM J9 - PG 25	N/A
AE-WR AF-RD	BOOTBANG E2PROM U37 - PG 23	N/A	N/A	N/A
84-WR 85-RD	LMU U36 - PG 23	N/A	N/A	N/A
58-WR 59-RD	N/A	FAN CONTROLLER U3 - PG 24	N/A	N/A
6A-WR 6B-RD	N/A	N/A	SNAPPER SOUND J12 - PG 24	N/A
D0-WR D1-RD	N/A	CLOCK SLEW SSCG U56 - PG 15	N/A	N/A

ADDR LSB INDICATES READ ('1') OR WRITE ('0') MODES

INT - ENET/FW/UATA EIDE/I2C

APPLE COMPUTER INC.

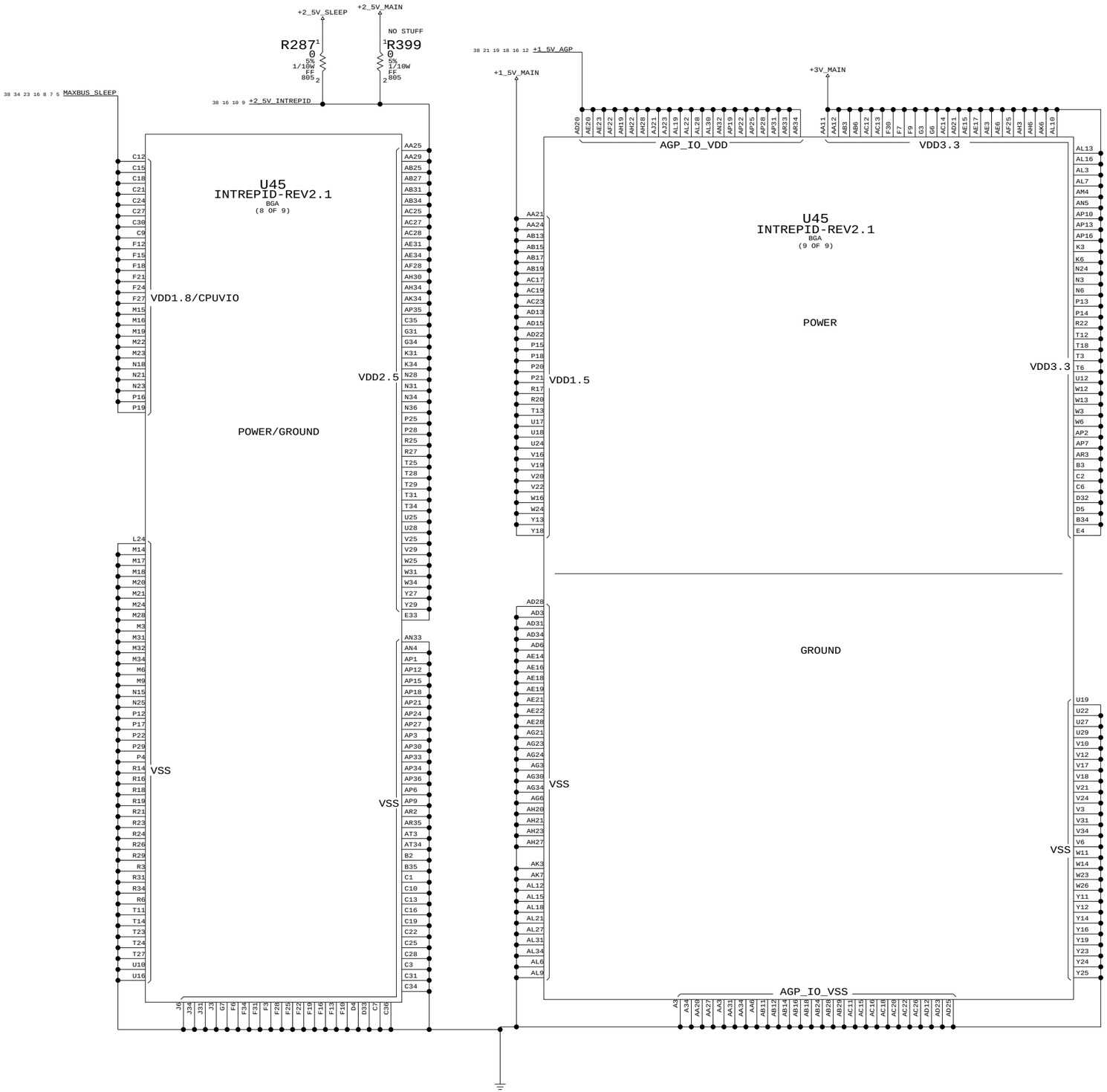
SIZE	DRAWING NUMBER	REV.
D	401258	AA
SCALE: NONE	SHT 13 OF 44	



HWPLL_TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES,METAL FILM,10 K OHM,5,1/16W,0402,SM	R100	NO_SSCG

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0004	197S0035		Y1	ALT FOR SIWARD



Intrepid Power

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401258	AA

SCALE	SHT	OF
NONE	15	44

INTREPID MAXBUS DECOUPLING

24 Balls
4 X 10UF (0805)
32 X 0.22UF (0402)

38 34 23 15 8 7 5 MAXBUS_SLEEP

C204 10uF 20% 6.3V CERM 805 (1 2)
C348 10uF 20% 6.3V CERM 805 (1 2)
C236 10uF 20% 6.3V CERM 805 (1 2)
C196 10uF 20% 6.3V CERM 805 (1 2)

C239 C240 C350 C312 C176 C288 C313 C94 C286 C158
C174 C206 C259 C237 C238 C95 C117 C241 C260 C314
C173 C171 C175 C226 C172 C207 C118 C287 C119 C349
C205 C209

(0.22uF 20% 6.3V CERM 402)

INTREPID AGP I/O DECOUPLING

21 Balls
4 X 10UF (0805)
24 X 0.22UF (0402)

38 21 19 18 15 12 +1_5V_AGP

C371 10uF 20% 6.3V CERM 805 (1 2)
C231 10uF 20% 6.3V CERM 805 (1 2)
C281 10uF 20% 6.3V CERM 805 (1 2)
C394 10uF 20% 6.3V CERM 805 (1 2)

C356 C297 C268 C217 C355 C267 C250 C298 C377 C216
C228 C230 C265 C378 C357 C229 C325 C393 C324 C323
C251 C266 C249

(0.22uF 20% 6.3V CERM 402)

INTREPID DDR DECOUPLING

44 Balls
4 X 10UF (0805)
51 X 0.22UF (0402)

38 15 10 9 +2_5V_INTREPID

C422 10uF 20% 6.3V CERM 805 (1 2)
C417 10uF 20% 6.3V CERM 805 (1 2)
C418 10uF 20% 6.3V CERM 805 (1 2)
C423 10uF 20% 6.3V CERM 805 (1 2)

C407 C391 C310 C317 C480 C390 C370 C320 C365 C366
C367 C292 C295 C403 C291 C352 C322 C392 C385 C376
C321 C318 C399 C410 C335 C369 C384 C294 C406 C405
C404 C400 C386 C289 C387 C401 C354 C389 C309 C398
C337 C290 C402 C397 C368 C334 C388 C293 C319 C336
C316

(0.22uF 20% 6.3V CERM 402)

INTREPID CORE DECOUPLING

30 Balls
4 X 10UF (0805)
29 X 0.22UF (0402)

+1_5V_MAIN

C128 10uF 20% 6.3V CERM 805 (1 2)
C101 10uF 20% 6.3V CERM 805 (1 2)
C157 10uF 20% 6.3V CERM 805 (1 2)
C315 10uF 20% 6.3V CERM 805 (1 2)

C147 C243 C262 C242 C227 C181 C142 C215 C278 C264
C244 C212 C178 C179 C177 C159 C161 C162 C280 C279
C144 C246 C211 C263 C180 C213 C197 C208 C214

(0.22uF 20% 6.3V CERM 402)

INTREPID 3.3V DECOUPLING

57 Balls
4 X 10UF (0805)
72 X 0.22UF (0402)

+3V_MAIN

C164 10uF 20% 6.3V CERM 805 (1 2)
C395 10uF 20% 6.3V CERM 805 (1 2)
C10 10uF 20% 6.3V CERM 805 (1 2)
C9 10uF 20% 6.3V CERM 805 (1 2)

C375 C351 C53 C42 C21 C185 C31 C143 C123 C121
C33 C184 C43 C35 C261 C60 C52 C199 C57 C19
C16 C108 C55 C32 C125 C45 C76 C277 C28 C26
C34 C23 C120 C146 C141 C30 C145 C96 C54 C50
C75 C122 C51 C59 C163 C126 C98 C109 C56 C27
C296 C248 C210 C58 C22 C20 C61 C44 C29 C24
C183 C18 C49 C36 C17 C99 C396 C124 C127 C100

(0.22uF 20% 6.3V CERM 402)

Intrepid Decoupling

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401258	AA

SCALE	SHT	OF
NONE	16	44

PCI1510 PULL-UPS

R757 10K 5% 1/16W MF 402 — CBUS_PCI_PERR_L 17
R756 10K 5% 1/16W MF 402 — CBUS_PCI_SERR_L 17
R753 10K 5% 1/16W MF 402 — CBUS_SUSPEND_PU 17

+3V_MAIN

C813 10UF 20% 6.3V CERM 805
C795 0.22UF 20% 6.3V CERM 402
C798 0.22UF 20% 6.3V CERM 402
C790 0.22UF 20% 6.3V CERM 402
C796 0.22UF 20% 6.3V CERM 402
C797 0.22UF 20% 6.3V CERM 402
C791 0.22UF 20% 6.3V CERM 402

R762 10K 5% 1/16W MF 402

+2_5V_MAIN

C789 0.22UF 20% 6.3V CERM 402

VCC: A7 C13 D5 E1 M1 N7 N11

39 30 26 24 20 18 17 14 MAIN_RESET_L

THIS PROPERLY SHUTS DOWN
CARDBUS POWER FOR PSUEDO-D3COLD

R348 47 5% 1/16W MF 402

+3V_MAIN
+5V_MAIN

NO STUFF
R373 10K 5% 1/16W MF 402

U19
TPS2211
SSOP

NC	9		
V_12	5	AVPP	10
V_5_1	6		
V_5_2	3	AVCC0	11
V_3_1	4	AVCC1	12
V_3_2		AVCC2	13
VCCD0	1		
VCCD1	2	CRITICAL	
VPPD0	15		
VPPD1	14		
SHTDWN	16		
GND	7	OC	8 NC

TPS2211_SHDN_L_PU

+VPP_CBUS_SW 17 38
+VCC_CBUS_SW 17 38

C773 0.1UF 20% 10V CERM 402
C467 0.1UF 20% 10V CERM 402

MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES
TO MINIMIZE INDUCTANCE!

0.1UF ARE USED TO INCREASE ESD DISCHARGES OF UP TO 10KV

CRITICAL
U26
PCI1510GGU
BGA

CLAMP FOR PC-CARD
CLAMP FOR PCI

NC	H10	CLK_48_RSVD/NC
PCI1510_VR_EN_L	D4	VR_EN*
	L8	VR_PORT
PCI_AD<0>	N8	AD0
PCI_AD<1>	M7	AD1
PCI_AD<2>	L7	AD2
PCI_AD<3>	N6	AD3
PCI_AD<4>	K4	AD4
PCI_AD<5>	M6	AD5
PCI_AD<6>	L6	AD6
PCI_AD<7>	N5	AD7
PCI_AD<8>	N4	AD8
PCI_AD<9>	M2	AD9
PCI_AD<10>	M5	AD10
PCI_AD<11>	L4	AD11
PCI_AD<12>	N3	AD12
PCI_AD<13>	K5	AD13
PCI_AD<14>	L5	AD14
PCI_AD<15>	M4	AD15
PCI_AD<16>	J4	AD16
PCI_AD<17>	H1	AD17
PCI_AD<18>	H3	AD18
PCI_AD<19>	H2	AD19
PCI_AD<20>	G2	AD20
PCI_AD<21>	G4	AD21
PCI_AD<22>	F1	AD22
PCI_AD<23>	C3	AD23
PCI_AD<24>	F3	AD24
PCI_AD<25>	E2	AD25
PCI_AD<26>	F4	AD26
PCI_AD<27>	B1	AD27
PCI_AD<28>	D2	AD28
PCI_AD<29>	E4	AD29
PCI_AD<30>	D3	AD30
PCI_AD<31>	E3	AD31
PCI_CBE<0>	K6	C/BE0*
PCI_CBE<1>	M3	C/BE1*
PCI_CBE<2>	J2	C/BE2*
PCI_CBE<3>	A1	C/BE3*
PCI_PAR	N1	PAR
PCI_IRDY_L	K1	TRDY
CBUS_PCI_SERR_L	L2	SERR
CBUS_PCI_IDSEL	F2	IDSEL
CBUS_PCI_PERR_L	K3	PERR
PCI_FRAME_L	J1	FRAME
PCI_STOP_L	L1	STOP
PCI_TRDY_L	J3	TRDY
PCI_DEVSEL_L	K2	DEVSEL
CBUS_PCI_RESET_L	G3	PRST
CBUS_PCI_REQ_L	C2	REQ
CBUS_PCI_GNT_L	C1	GNT
CLK33M_CBUS	G1	PCLK
NC	M9	SPKROUT
NC	M8	RI_OUT/PME
CBUS_SUSPEND_PU	N10	SUSPEND
CBUS_INT_L	K7	MFUNC0
CBUS_MFUNC1_PD	N9	MFUNC1
CBUS_MFUNC2_PD	L9	MFUNC2
CBUS_MFUNC3_PD	K10	MFUNC3
CBUS_MFUNC4_PD	M10	MFUNC4
CBUS_MFUNC5_PD	N12	MFUNC5
CBUS_MFUNC6_PD	L10	MFUNC6
	L11	GRST

	VCCCB	B11
	VCCP	L3
	VCCD0*	N13 CBUS_VCCD0_L
	VCCD1*	L12 CBUS_VCCD1_L
	VPPD0	K9 CBUS_VPPD0
	VPPD1	M11 CBUS_VPPD1
	CD1*/CCD1*	L13 CBUS_DET_1_L 17 39
	CD2*/CCD2*	B5 CBUS_DET_2_L 17 39
	IORD*/CAD13	F12 CBUS_IORD_L 17
	IOWR*/CAD15	C11 CBUS_IOWR_L 17
	OE*/CAD11	G10 CBUS_OE_L 17
	CE1*/CC/BE0*	H13 CBUS_CE1_L 17
	VS1*/CVS1	B2 CBUS_VS1 17
	VS2*/CVS2	A9 CBUS_VS2 17
	WE*/CGNT*	D13 CBUS_WE_L 17
	RDY/IREQ*/CINT*	A6 CBUS_READY 17
	RESET/CRST*	D8 CBUS_RESET_L 17
	REG*/CC/BE3*	A8 CBUS_REG_L 17
	BVD1/CSTSCHG/STSCHG*/RI*	C6 CBUS_BVD1_L 17
	BVD2/SPKR*/CAUDIO	D6 CBUS_BVD2_L 17
INTEGRATED PULL-UP	WP/IOIS16*/CCLKRUN*	A5 CBUS_WP_L 17
	CE2/CAD10*	G13 CBUS_CE2_L 17
	INPACK/CREQ*	B8 CBUS_INPACK_L 17
	WAIT/CSERR*	B6 CBUS_WAIT_L 17
	A0/CAD26	C7 CBUS_ADDR<0> 17
	A1/CAD25	D7 CBUS_ADDR<1> 17
	A2/CAD24	B7 CBUS_ADDR<2> 17
	A3/CAD23	D10 CBUS_ADDR<3> 17
	A4/CAD22	B12 CBUS_ADDR<4> 17
	A5/CAD21	C8 CBUS_ADDR<5> 17
	A6/CAD20	C9 CBUS_ADDR<6> 17
	A7/CAD18	A12 CBUS_ADDR<7> 17
	A8/CC/BE1*	E11 CBUS_ADDR<8> 17
	A9/CAD14	F11 CBUS_ADDR<9> 17
	A10/CAD9	G11 CBUS_ADDR<10> 17
	A11/CAD12	G12 CBUS_ADDR<11> 17
	A12/CC/BE2*	D9 CBUS_ADDR<12> 17
	A13/CPAR	E12 CBUS_ADDR<13> 17
	A14/CPERR*	D12 CBUS_ADDR<14> 17
	A15/CIRDY*	C10 CBUS_ADDR<15> 17
	A16/CCLK	B13 CBUS_ADDR_16_UF
	A17/CAD16	F10 CBUS_ADDR<17> 17
	A18/RSVD	E13 CBUS_ADDR<18> 17
	A19/CBLOCK*	A13 CBUS_ADDR<19> 17
	A20/CSTOP*	E10 CBUS_ADDR<20> 17
	A21/CDEVSEL*	D11 CBUS_ADDR<21> 17
	A22/CTRDY*	C12 CBUS_ADDR<22> 17
	A23/CFRAME*	A10 CBUS_ADDR<23> 17
	A24/CAD17	B10 CBUS_ADDR<24> 17
	A25/CAD19	B9 CBUS_ADDR<25> 17
	D0/CAD27	A4 CBUS_DATA<0> 17
	D1/CAD29	C4 CBUS_DATA<1> 17
	D2/RSVD	A3 CBUS_DATA<2> 17
	D3/CAD0	K11 CBUS_DATA<3> 17
	D4/CAD1	K12 CBUS_DATA<4> 17
	D5/CAD3	J13 CBUS_DATA<5> 17
	D6/CAD5	J10 CBUS_DATA<6> 17
	D7/CAD7	H12 CBUS_DATA<7> 17
	D8/CAD28	C5 CBUS_DATA<8> 17
	D9/CAD30	B4 CBUS_DATA<9> 17
	D10/CAD31	B3 CBUS_DATA<10> 17
	D11/CAD2	M12 CBUS_DATA<11> 17
	D12/CAD4	J11 CBUS_DATA<12> 17
	D13/CAD6	K13 CBUS_DATA<13> 17
	D14/RSVD	J12 CBUS_DATA<14> 17
	D15/CAD8	H11 CBUS_DATA<15> 17

R750 47 5% 1/16W MF 402 — CBUS_ADDR<16> 17

R767 22 5% 1/16W MF 402

NO STUFF
R764 47 5% 1/16W MF 402 — 30 27 26 23 IO_RESET_L

R766 47 5% 1/16W MF 402 — 39 30 26 24 20 18 17 14 MAIN_RESET_L

RP39 10K 5% 1/32W 25V SM
5 10 — 6 4 7 3 9 8 2 1
CBUS_MFUNC1_PD 17
CBUS_MFUNC2_PD 17
CBUS_MFUNC3_PD 17
CBUS_MFUNC4_PD 17
CBUS_MFUNC5_PD 17
CBUS_MFUNC6_PD 17

GND: A2 A11 D1 F13 H4 K8 M13 N2

TI REFERENCE SCHEMATIC DID NOT HAVE BULK ON +VCC_CBUS_SW

C783 2.2UF 20% 10V CERM 805
C776 2.2UF 20% 10V CERM 805

PC CARD/CARDBUS CONNECTOR

CRITICAL
J9
QT500806-L111
M-ST-SM1

	2	1	CBUS_DATA<3> 17
39 17 CBUS_DET_1_L	4	3	CBUS_DATA<4> 17
17 CBUS_DATA<11>	6	5	CBUS_DATA<5> 17
17 CBUS_DATA<12>	8	7	CBUS_DATA<6> 17
17 CBUS_DATA<13>	10	9	
	12	11	CBUS_DATA<7> 17
17 CBUS_DATA<14>	14	13	CBUS_CE1_L 17
17 CBUS_DATA<15>	16	15	CBUS_ADDR<10> 17
17 CBUS_CE2_L	18	17	CBUS_OE_L 17
17 CBUS_VS1	20	19	
	22	21	CBUS_ADDR<11> 17
17 CBUS_IORD_L	24	23	CBUS_ADDR<9> 17
17 CBUS_IOWR_L	26	25	CBUS_ADDR<8> 17
17 CBUS_ADDR<17>	28	27	CBUS_ADDR<13> 17
17 CBUS_ADDR<18>	30	29	
	32	31	CBUS_ADDR<14> 17
17 CBUS_ADDR<19>	34	33	CBUS_WE_L 17
17 CBUS_ADDR<20>	36	35	CBUS_READY 17
17 CBUS_ADDR<21>	38	37	+VCC_CBUS_SW 17 38
38 17 +VCC_CBUS_SW	40	39	
	42	41	+VPP_CBUS_SW 17 38
38 17 +VPP_CBUS_SW	44	43	CBUS_ADDR<16> 17
17 CBUS_ADDR<22>	46	45	CBUS_ADDR<15> 17
17 CBUS_ADDR<23>	48	47	CBUS_ADDR<12> 17
17 CBUS_ADDR<24>	50	49	
	52	51	CBUS_ADDR<7> 17
17 CBUS_ADDR<25>	54	53	CBUS_ADDR<6> 17
17 CBUS_VS2	56	55	CBUS_ADDR<5> 17
17 CBUS_RESET_L	58	57	CBUS_ADDR<4> 17
17 CBUS_WAIT_L	60	59	
	62	61	CBUS_ADDR<3> 17
17 CBUS_INPACK_L	64	63	CBUS_ADDR<2> 17
17 CBUS_REG_L	66	65	CBUS_ADDR<1> 17
17 CBUS_BVD2_L	68	67	CBUS_ADDR<0> 17
17 CBUS_BVD1_L	70	69	
	72	71	CBUS_DATA<0> 17
17 CBUS_DATA<8>	74	73	CBUS_DATA<1> 17
17 CBUS_DATA<9>	76	75	CBUS_DATA<2> 17
17 CBUS_DATA<10>	78	77	CBUS_WP_L 17
39 17 CBUS_DET_2_L	80	79	

83 82

CARDBUS

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401258	AA
SCALE: NONE	SHT 17 OF 44	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0133	1	IC,ATI,M10,NO HEATSPREADER	U44	CRITICAL	?

27M OSC

(PLACE THE OSCILLATOR AND R189 AND R195 CLOSE TO ATI PIN AJ29)

+3V_SLEEP — L4 FERR-EMI-100-OHM (SM) — +3V_ATI_OSC_SLEEP

C77 0.1uF 20% 16V CERM 402

C78 4.7uF 20% 6.3V CERM 805

NO STUFF R188 100K 5% 1/16W MF 402

CRITICAL — U44 VCC — G2 27.0000M OSC SM-1 — OE / GND / OUT

ATI_OSC_OE

(PLACE R200 CLOSE TO OSC)

GPU_SS R200 0 5% 1/16W MF 402

ATI_CLK27M_OSC — ATI_CLK27M_OSC_SS

R189 287 1% 1/16W MF 402

ATI_CLK27M_IN

R195 162 1% 1/16W MF 402

S0=1;S1=M => -1.5% DOWN-SPREAD

SPREAD SPECTRUM SUPPORT

+3V_SLEEP — GPU_SS L3 FERR-EMI-100-OHM (SM) — +3V_ATI_SS

GPU_SS C70 10uF 20% 6.3V CERM 805

GPU_SS C71 0.1uF 20% 16V CERM 402

NO STUFF R173 0 5% 1/16W MF 402

GPU_SS R181 0 5% 1/16W MF 402

GPU_SS — CRITICAL — VDD U47 CY25811 SOI

ATI_CLK27M_OSC_SS — XIN/CLKIN

XOUT — SSCLK — ATI_SSCLK_UF

NC — FRSEL

CY25811_S1 — S1

CY25811_S0 — S0

VSS

GPU_SS R201 33 5% 1/16W MF 402 — ATI_SSCLK_IN

NO STUFF R37 0 5% 1/16W MF 402

NO STUFF R38 0 5% 1/16W MF 402

OMIT CRITICAL — U44 RAGE_MOBILITY M10-CSP64 64MB BGA (1 OF 6)

AD31 AD30 AD29 AD28 AD27 AD26 AD25 AD24 AD23 AD22 AD21 AD20 AD19 AD18 AD17 AD16 AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0

CBEB3 CBEB2 CBEB1 CBEB0 PCICLK FRAMEB IRDYB TRDYB STOPB DEVSELB PAR REQB GNTB INTAB RSTB WBF VREFG VREF

AD_STB0 AD_STB1 AD_STBB0 AD_STBB1 AGP_BUSYB AGPREF AGPTEST AGP8X_DETB SUS_STAT ST0 ST1 ST2 SBA7 SBA6 SBA5 SBA4 SBA3 SBA2 SBA1 SBA0 RBFB STP_AGPB SB_STB SB_STBS RSTB_MSK DBI_LO DBI_HI

R119 47 5% 1/16W MF 402 — R127 10K 5% 1/16W MF 402 — R159 20K 5% 1/16W MF 402

INT_AGP_VREF — C62 0.1uF 20% 16V CERM 402 — C63 0.01uF 20% 16V CERM 402 — (PLACE C1002 CLOSE TO AGPREF PIN)

R172 20K 5% 1/16W MF 402

R158 0 5% 1/16W MF 402

R126 47K 5% 1/16W MF 402 — R138 47K 5% 1/16W MF 402

R118 45.3 1% 1/16W MF 402

OMIT — U44 RAGE_MOBILITY M10-CSP64 64MB BGA (6 OF 6)

VSS — VDDCI

L2 60-OHM-EMI (SM) — GPU_VCORE — GPU_VCORE_VDDCI

C64 0.01uF 20% 16V CERM 402 — C67 10uF 20% 6.3V CERM 805

C65 0.01uF 20% 16V CERM 402 — C68 0.01uF 20% 16V CERM 402

C66 0.01uF 20% 16V CERM 402 — C69 0.01uF 20% 16V CERM 402

U44 RAGE_MOBILITY M10-CSP64 64MB BGA (2 OF 6) — OMIT

VSS — VSS

MAIN_RESET_L IS TOGGLED FOR SLEEP

R54 10K 5% 1/16W MF 402 — R53 47 5% 1/16W MF 402 — MAIN_RESET_L

R43 1K 1% 1/16W MF 402

R44 1K 1% 1/16W MF 402 — +GPU_MEM

R45 1K 1% 1/16W MF 402

R46 1K 1% 1/16W MF 402

C11 0.1uF 20% 16V CERM 402 — C37 10uF 20% 6.3V CERM 805

PLACE VERF VOLTAGE DIVIDER CLOSE TO ATI M10 VREF PIN

R55 4.7K 5% 1/16W MF 402 — R104 4.7K 5% 1/16W MF 402

R70 4.7K 5% 1/16W MF 402 — R105 4.7K 5% 1/16W MF 402

ATI_MEMIO_LO — ATI_MEMIO_HI

ATI_MEMVMODE0 — MEMVMODE0

ATI_MEMVMODE1 — MEMVMODE1

FOR 2.5 VDDR1
MEMVMODE0=1.8V
MEMVMODE1=GND

FOR 1.8 VDDR1
MEMVMODE0=GND
MEMVMODE1=1.8V

TEST_YCLK TEST_MLCK MEMTEST PLLTEST — ATI_MEMTEST — NC

GPU_THERM_DP GPU_THERM_DM +GPU_MEM (PULL-UP to GPU_MEM_IO)

M10 AGP INTERFACE

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401258	AA

SCALE: NONE — SHT 18 OF 44

TMDS TERMINATION

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN
CMF LINE SHOULD BE ROUTED AS 4MIL SURFACE
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS

U44
RAGE_MOBILITY
M10-CSP64
64MB
BGA
(3 OF 6)

GPU_DVOD<0> AJ5 ZV_LCDDATA0
GPU_DVOD<1> AK5 ZV_LCDDATA1
GPU_DVOD<2> AG6 ZV_LCDDATA2
GPU_DVOD<3> AH6 ZV_LCDDATA3
GPU_DVOD<4> AJ6 ZV_LCDDATA4
GPU_DVOD<5> AK6 ZV_LCDDATA5
GPU_DVOD<6> AG7 ZV_LCDDATA6
GPU_DVOD<7> AH7 ZV_LCDDATA7
GPU_DVOD<8> AJ7 ZV_LCDDATA8
GPU_DVOD<9> AK7 ZV_LCDDATA9
GPU_DVOD<10> AG8 ZV_LCDDATA10
GPU_DVOD<11> AH8 ZV_LCDDATA11
NC AJ8 ZV_LCDDATA12
NC AK8 ZV_LCDDATA13
NC AG9 ZV_LCDDATA14
NC AH9 ZV_LCDDATA15
NC AJ9 ZV_LCDDATA16
NC AK9 ZV_LCDDATA17
NC AG10 ZV_LCDDATA18
NC AH10 ZV_LCDDATA19
ZV_LCDDATA20_PU AJ10 ZV_LCDDATA20
NC AK10 ZV_LCDDATA21
NC AG11 ZV_LCDDATA22
NC AH11 ZV_LCDDATA23

GPU_DVO_VSYNC AJ4 ZV_LCDCNTL0
GPU_DVO_HSYNC AK4 ZV_LCDCNTL1
GPU_DVOD_DE AH5 ZV_LCDCNTL2
GPU_DVO_CLKP AG5 ZV_LCDCNTL3

ATI_AGP_FBSKEW<0> AJ2 GPIO0
ATI_AGP_FBSKEW<1> AK2 GPIO1
ATI_X1CLK_SKEW<0> AK1 GPIO2
ATI_X1CLK_SKEW<1> AH3 GPIO3
ATI_BUS_CFG<0> AH2 GPIO4
ATI_BUS_CFG<1> AJ1 GPIO5
ATI_BUS_CFG<2> AF4 GPIO6
ATI_GPIO7_SPN AH1 GPIO7 (NO ICT TEST)
ATI_GPIO8_PD AG3 GPIO8
ATI_GPIO9_SPN AF3 GPIO9 (NO ICT TEST)
ATI_GPIO10_SPN AG2 GPIO10 (NO ICT TEST)
ATI_GPIO11_SPN AF2 GPIO11 (NO ICT TEST)
ATI_GPIO12_SPN AG1 GPIO12 (NO ICT TEST)
ATI_GPIO13_SPN AF1 GPIO13 (NO ICT TEST)
HPD_PWR_SNS_EN AE2 GPIO14
GPU_VCORE_CNTL_L AE1 GPIO15
ATI_SSCLK_IN M1 GPIO16

ATI_TMDS_DN<0> AJ13 TX0M
ATI_TMDS_DP<0> AK13 TX0P
ATI_TMDS_DN<1> AJ14 TX1M
ATI_TMDS_DP<1> AK14 TX1P
ATI_TMDS_DP<2> AJ15 TX2M
ATI_TMDS_DP<2> AK15 TX2P
ATI_TMDS_CLKN AJ12 TXCM
ATI_TMDS_CLKP AK12 TXCP

ATI_CLK27M_IN AJ29 XTALIN
NC AJ30 XTALOUT
ATI_TESTEN AH24 TESTEN
NC AJ26 SSIN

B24 VSS
B20 VSS
A24 VSS

ROMCSB AE5 NC
R AK28 GPU_R
G AK27 GPU_G
B AK26 GPU_B
VSYNC AG27 ATI_VSYNC
V2SYNC AG25 NC
HSYNC AG26 ATI_HSYNC
H2SYNC AG24 NC
RSET AK25 ATI_RSET
R2SET AJ24 ATI_R2SET
Y_G AK23 GPU_Y
C_R AK24 GPU_C
COMP_B AK22 GPU_COMP
DIGON AE13 FP_PWR_EN
BLON AF13 INV_ON_PWM
HPD1 AF11 GPU_HPD
AUXWIN AJ27 GPU_AUXWIN
DDC1DATA AH28 GPU_DVI_DDC_DATA
DDC1CLK AH27 GPU_DVI_DDC_CLK
DDC2DATA AE12 LVDS_DDC_DATA
DDC2CLK AF12 LVDS_DDC_CLK
DDC3DATA AH26 SI_DDC_DATA
DDC3CLK AH25 SI_DDC_CLK
TXOUT_U0N AH18 LVDS_U0N
TXOUT_U0P AG18 LVDS_U0P
TXOUT_U1N AH19 LVDS_U1N
TXOUT_U1P AG19 LVDS_U1P
TXOUT_U2N AH20 LVDS_U2N
TXOUT_U2P AG20 LVDS_U2P
TXOUT_U3N AH22 LVDS_U3N_TP (NO ICT TEST)
TXOUT_U3P AG22 LVDS_U3P_TP (NO ICT TEST)
TXCLK_UN AH21 CLKLVDS_UN
TXCLK_UP AG21 CLKLVDS_UP
TXOUT_L0N AK16 LVDS_L0N
TXOUT_L0P AJ16 LVDS_L0P
TXOUT_L1N AK17 LVDS_L1N
TXOUT_L1P AJ17 LVDS_L1P
TXOUT_L2N AK18 LVDS_L2N
TXOUT_L2P AJ18 LVDS_L2P
TXOUT_L3N AK20 LVDS_L3N_TP (NO ICT TEST)
TXOUT_L3P AJ20 LVDS_L3P_TP (NO ICT TEST)
TXCLK_LN AK19 CLKLVDS_LN
TXCLK_LP AJ19 CLKLVDS_LP
SSOUT AJ25 NC

VSS A20
VSS B21

OMIT

R229 1K 5% 1/16W MF 402

+1_8V_GPU +3V_GPU
EXT_TMDS R228 10K 5% 1/16W MF 402
INT_TMDS R234 10K 5% 1/16W MF 402

R240 75 1% 1/16W MF 402
R246 75 1% 1/16W MF 402
R249 75 1% 1/16W MF 402
R256 715 1% 1/16W MF 402
R257 499 1% 1/16W MF 402
R245 75 1% 1/16W MF 402
R248 75 1% 1/16W MF 402
R254 75 1% 1/16W MF 402
R711 10K 5% 1/16W MF 402
R247 10K 5% 1/16W MF 402
R253 10K 5% 1/16W MF 402

+1_5V_AGP
Q77 SI3446DV TSOP
GPU_CORE_OK
+GPU_VDD15_UF
C166 1000pF 10% 25V X7R 402

L24 FERR-220-OHM 0805
+1_5V_GPU_VDD15 (500mA)

C222 0.01uF 20% 16V CERM 402
C256 0.01uF 20% 16V CERM 402
C299 0.01uF 20% 16V CERM 402
C305 0.01uF 20% 16V CERM 402
C328 10uF 20% 6.3V CERM 805
C232 0.01uF 20% 16V CERM 402
C269 0.01uF 20% 16V CERM 402
C300 0.01uF 20% 16V CERM 402
C306 0.01uF 20% 16V CERM 402

U44
RAGE_MOBILITY
M10-CSP64
64MB
BGA
(5 OF 6)

F12 L6 T6 AB6 F17 G25 R25 AB25 VDD15
AJ3 AF25 AG4 AH4 AF5 F6 G6 H6 P6 AD26 V6 W6 AC6 AD6 AE6 F7 F10 AE10 F11 AE11 F13 F14 AE14 AF14 W26 AF15 AE17 AC25 AE18 F23 F24 AE24 F25 M25 N25 W25 V25 VDDC
OMIT
G7 G8 G9 G10 G11 G12 G13 G14 G15 G16 G17 G18 G19 G20 G21 G22 G23 G24 H7 H8 H23 H24 J7 J24 K7 K24 L7 L24 M7 M24 N7 N24 P7 P24 R7 R24 T7 T24 U7 U24 V7 V24 W7 W24 Y7 Y24 AA7 AA24 AB7 AB24 AC7 AC8 AC23 AC24 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 VSS

GPU_VCORE

GPU VCORE - 1.2V

(PUT ALL CAPS BELOW ATI ASIC)

C167 10uF 20% 6.3V CERM 805
C219 10uF 20% 6.3V CERM 805
C252 0.22uF 20% 6.3V CERM 402
C270 0.22uF 20% 6.3V CERM 402
C301 0.22uF 20% 6.3V CERM 402
C307 0.22uF 20% 6.3V CERM 402
C329 0.22uF 20% 6.3V CERM 402
C332 0.22uF 20% 6.3V CERM 402
C186 0.22uF 20% 6.3V CERM 402
C220 0.22uF 20% 6.3V CERM 402
C253 0.22uF 20% 6.3V CERM 402
C271 0.22uF 20% 6.3V CERM 402
C302 0.22uF 20% 6.3V CERM 402
C311 0.22uF 20% 6.3V CERM 402
C330 0.22uF 20% 6.3V CERM 402
C333 0.22uF 20% 6.3V CERM 402
C187 0.22uF 20% 6.3V CERM 402
C221 0.22uF 20% 6.3V CERM 402
C254 0.22uF 20% 6.3V CERM 402
C282 0.22uF 20% 6.3V CERM 402
C303 0.22uF 20% 6.3V CERM 402
C326 0.22uF 20% 6.3V CERM 402
C331 0.22uF 20% 6.3V CERM 402
C338 0.22uF 20% 6.3V CERM 402

M10 Power Shut down Sequencing

+2_5V_SLEEP
XW21 SM
DP6 BAS16TW SOT-363
+1_8V_ATI_PVDD
+2_5V_SLEEP_NECK
XW24 SM
+1_8V_PVDD_NECK
XW20 SM
DP6 BAS16TW SOT-363
+1_5V_AGP_NECK
XW23 SM
GPU_VCORE
GPU_VCORE_NECK
XW22 SM
DP6 BAS16TW SOT-363
+GPU_VDD15_UF
+GPU_VDD15_NECK

R258 10K 5% 1/16W MF 402
R260 10K 5% 1/16W MF 402
R262 10K 5% 1/16W MF 402 NO STUFF
R265 10K 5% 1/16W MF 402 NO STUFF
R269 10K 5% 1/16W MF 402 NO STUFF
R271 10K 5% 1/16W MF 402 NO STUFF
R273 10K 5% 1/16W MF 402 NO STUFF
R259 10K 5% 1/16W MF 402 NO STUFF
R261 10K 5% 1/16W MF 402 NO STUFF
R263 10K 5% 1/16W MF 402 NO STUFF
R266 10K 5% 1/16W MF 402 NO STUFF
R270 10K 5% 1/16W MF 402 NO STUFF
R272 10K 5% 1/16W MF 402 NO STUFF
R274 10K 5% 1/16W MF 402 NO STUFF

(GPIO0) ATI_AGP_FBSKEW<0>
(GPIO1) ATI_AGP_FBSKEW<1>
(GPIO2) ATI_X1CLK_SKEW<0>
(GPIO3) ATI_X1CLK_SKEW<1>
(GPIO4) ATI_BUS_CFG<0>
(GPIO5) ATI_BUS_CFG<1>
(GPIO6) ATI_BUS_CFG<2>

GPU VCORE SUPPLY

WHEN VCORE_CNTL HIGH => 1.2V
1.2V = 0.8V * (1 + R332 / (R331//R333))

WHEN VCORE_CNTL LOW => 1.0V
1.0V = 0.8V * (1 + R332 / R333)

+PBUS
+5V_MAIN
+3V_GPU

R389 1M 5% 1/16W MF 402
R430 1 5% 1/16W MF 603
R339 576K 1% 1/16W MF 402
C762 4.7UF 20% 25V CERM 1206
C766 4.7UF 20% 25V CERM 1206
Q51 SI7860DP SO-8-PWRPK CRITICAL
L30 2.1UH-11A SM
D24 SMB B340LB
D5 SM MBR0540
R416 2.2 5% 1/16W MF 603
C514 0.1uF 20% 25V CERM 603
C494 0.1uF 20% 25V CERM 603
R388 0 5% 1/16W MF 402 NO STUFF
R341 63.4K 1% 1/16W MF 402 NO STUFF
C473 4.7UF 20% 10V CERM 1206
R236 100K 5% 1/16W MF 402
R306 100K 5% 1/16W MF 402
R316 100K 5% 1/16W MF 402
DP1 BAS16TW SOT-363
R390 0 5% 1/16W MF 402
R294 10K 5% 1/16W MF 402
Q6 2N3904 SM
Q5 2N3904 SM
R203 33K 5% 1/16W MF 402
R340 20K 1% 1/16W MF 402
C451 220pF 5% 25V CERM 402
C448 470pF 10% 50V CERM 402
R311 0 5% 1/16W MF 402
R332 0 5% 1/16W MF 402
C483 0.1uF 20% 10V CERM 402
C882 0.0022UF 10% 50V CERM 402 NO STUFF
OMIT XW2 SM

U16
LTC1778
SSOP
EXT_VCC_VIN
RUN/SS
ITH
VRNG
FCB
PGOOD
SGND
PGND
BOOST
TG
SW
BG
VFB

C708 22UF 20% 10V CERM 1210
C721 330UF 20% 6.3V POLY SMD
C719 330UF 20% 6.3V POLY SMD
C720 330UF 20% 6.3V POLY SMD
R307 100K 5% 1/16W MF 402
C902 0.1UF 20% 10V CERM 402
R410 10K 5% 1/16W MF 402
C515 0.1uF 20% 10V CERM 402
Q80 2N7002DW SOT-363
R352 4.99K 1% 1/16W MF 402
R451 18.2K 1% 1/16W MF 402
R351 20K 1% 1/16W MF 402
R804 1.82K 1% 1/16W MF 402

HIGH_VCORE_DIV
GPU_PWRMSR
HIGH_VCORE
GPU_VCORE_CNTL
VCORE_CNTL_RC

CRITICAL
NO STUFF

M10 CORE PWR/LVDS/TMDS

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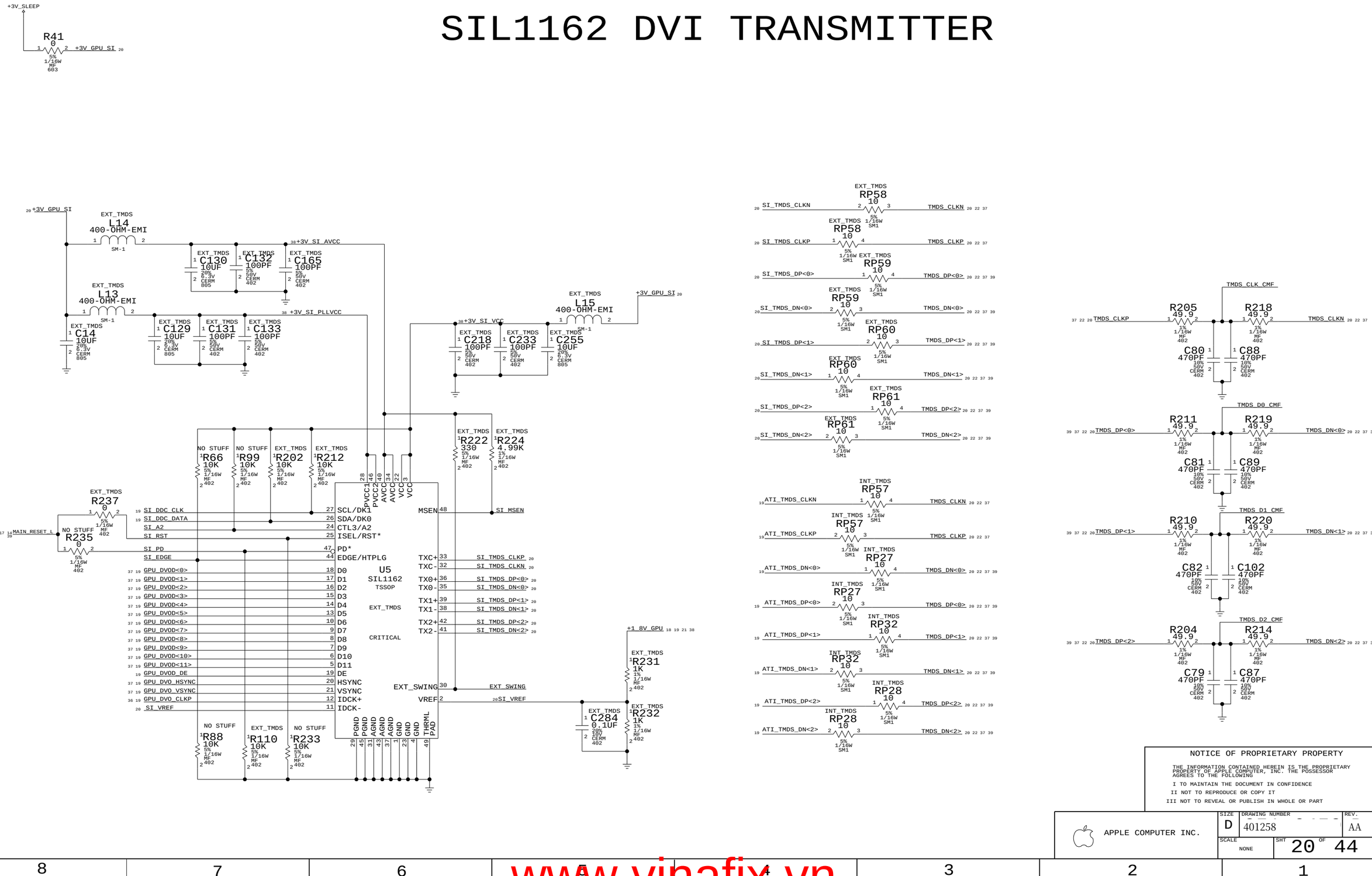
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401258	AA
SCALE: NONE	SHT 19 OF 44	

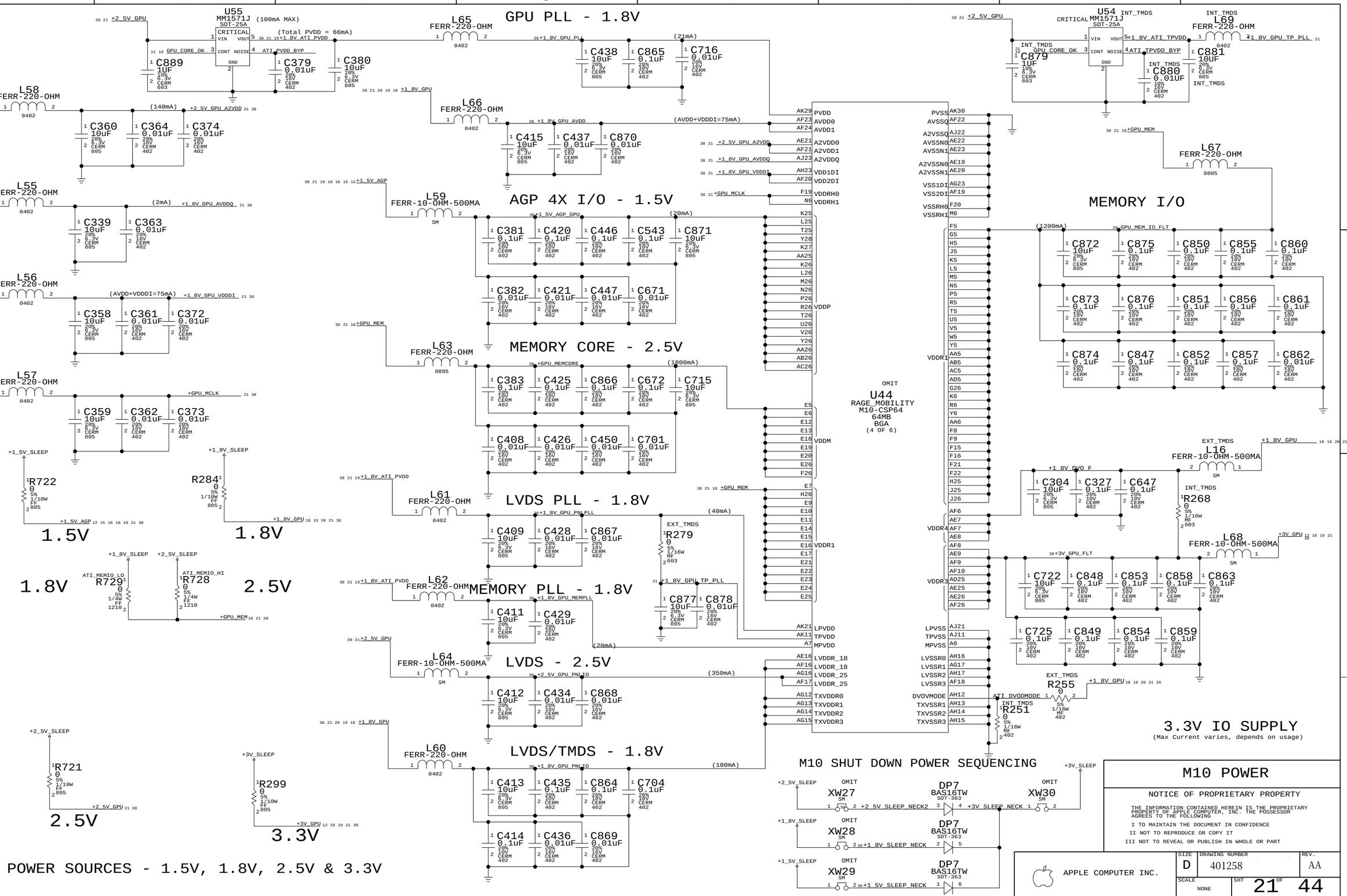
SIL1162 DVI TRANSMITTER



APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401258	AA

SCALE	SHT	OF
NONE	20	44



EXTERNAL VIDEO (DVI) INTERFACE

ANALOG FILTERING PLACE CLOSE TO CONNECTOR

FL2 CRITICAL LCFILTER SM-220MHZ — GPU_B → VGA_B
FL1 CRITICAL LCFILTER SM-220MHZ — GPU_G → VGA_G
FL3 CRITICAL LCFILTER SM-220MHZ — GPU_R → VGA_R
C685 3.3PF 0.25% 50V CERM 402
C676 3.3PF 0.25% 50V CERM 402
C684 3.3PF 0.25% 50V CERM 402

VGA VSYNC BUFFERS

+3V_MAIN
U56 CRITICAL 74AHC1G32 SM — ATI_HSYNC → VGA_HSYNC_BUF
R718 33 5% 1/16W MF 402 — VGA_HSYNC_BUF → VGA_HSYNC
U57 CRITICAL 74AHC1G32 SM — ATI_VSYNC → VGA_VSYNC_BUF
R714 33 5% 1/16W MF 402 — VGA_VSYNC_BUF → VGA_VSYNC

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)

+5V_SLEEP → F1 0.5AMP-13.2V SM → +5V_DDC_SLEEP_UF → L23 400-OHM-EMI SM-1 → +5V_DDC_SLEEP
Isolation required for DVI power switch

D21 SM MBR0530 — DDC_CLK_ISO

J14 CRITICAL QH1112 F-RT-TH

TMDS_CONN_DN<0>	17	1	TMDS_CONN_DN<2>
TMDS_CONN_DP<0>	18	2	TMDS_CONN_DP<2>
	19	3	TMDS_CONN_DP<1>
(TMDS_DN<5>)	20	4	(TMDS_DN<4>)
(TMDS_DP<5>)	21	5	(TMDS_DN<3>)
	22	6	(TMDS_DP<4>)
TMDS_CONN_CLKP	23	7	(TMDS_DP<3>)
TMDS_CONN_CLKN	24	8	VGA_VSYNC
		16	DVI_HPD_UF
		14	(+5V_DDC_SLEEP)
		15	DVI_DDC_DATA_UF
VGA_B	C3	C1	VGA_R
VGA_HSYNC	C4	C2	VGA_G

R655 4.7K 5% 1/16W MF 402 — DDC_CLK_ISO
R661 4.7K 5% 1/16W MF 402
R670 100 5% 1/16W MF 402 — DVI_DDC_CLK
R649 100 5% 1/16W MF 402 — DVI_DDC_DATA
R650 100 5% 1/16W MF 402 — DVI_HPD
C706 100pF 5% 50V CERM 402
C669 100pF 5% 50V CERM 402
C710 0.01UF 20% 50V CERM 603
C1 100pF 5% 50V CERM 402
R706 0 5% 1/16W MF 402 — PLACE NEAR 3, 11 & 19
R1 0 5% 1/16W MF 402 — PLACE NEAR C5A & C5B
CHGND1 / CHGND5

3V LEVEL SHIFTERS

+3V_SLEEP
Q038 2N7002DW SOT-363 — DVI_DDC_CLK → GPU_DVI_DDC_CLK
Q038 2N7002DW SOT-363 — DVI_DDC_DATA → GPU_DVI_DDC_DATA
Q035 2N7002DW SOT-363 — DVI_HPD → GPU_HPD
R662 10K 5% 1/16W MF 402
R671 10K 5% 1/16W MF 402
R694 100K 5% 1/16W MF 402

NOTE: Pulldown for DVI_HPD provided by DVI power switch interface
NOTE: DVI_HPD SHARES Q68 WITH ALS BECAUSE OF BOARD REAL ESTATE

DVI POWER SWITCH

Power key detect path when system is shutdown or asleep.. DDC_CLK is isolated from NV17M DURING SHUTDOWN. WHEN power key on remote device is pressed, 5V will be driven into DDC_CLK. Since host rails will be low, TP0610 will turn on, driving SOFT_PWR_ON_L low. As host rails rise, TP0610 will turn off, as will remote device path into DDC_CLK. Isolation will be disabled as well.

Q40 TP0610 SM — DVI_DDC_CLK_UF → DVI_TURN_ON
R690 680 5% 1/16W MF 402
R691 10K 5% 1/16W MF 402 — DVI_TRUN_ON_ILIM
Q042 2N3904 SM — DVI_TURN_ON_BASE
SOFT_PWR_ON_L
R688 330 5% 1/16W MF 402 — Pulldown prevents 3904 from turning on when DVI monitor has active, self-powered DDC clock pullup.
+5V_DDC_SLEEP

Power key detect path when system is running. HPD normally driven to 3.3V. When power key on remote device pressed, HPD will be driven to 5V. COMPARATOR ENABLED BY NV17MAP GPIO.

+3V_SLEEP
R680 68.1K 1% 1/16W MF 402
C696 0.1UF 20% 10V CERM 402
U46 CRITICAL LMC7211 SM — HPD_4V_REF
HPD_PWR_SW
R663 10K 1% 1/16W MF 402 — DVI_HPD_UF → DVI_HPD_DIV
R686 10K 1% 1/16W MF 402
R681 100K 1% 1/16W MF 402
Q041 2N7002DW SOT-363 — HPD_ON
R703 330 5% 1/16W MF 402
+PBUS
Q045 TP0610 SM — COMP_ENABLE
R696 100K 5% 1/16W MF 402
R704 100K 5% 1/16W MF 402
COMP_DISABLE
HPD_ON_RC
R700 20K 5% 1/16W MF 402
HPD_BASE
Q044 2N3904 SM
NEED PULL-DOWN BECAUSE THIS SIGNAL IS TRISTATED INITIALLY
HPD_PWR_SNS_EN
Q041 2N7002DW SOT-363
R213 100K 5% 1/16W MF 402
C703 47UF 20% 6.3V CERM 1210
R705 68K 5% 1/16W MF 402

TMDS FILTERING PLACE CLOSE TO CONNECTOR

L72 CRITICAL 90-OHM-200MA SM — TMDS_DN<0> → TMDS_CONN_DN<0>; TMDS_DP<0> → TMDS_CONN_DP<0>
L21 CRITICAL 165-OHM SM — TMDS_CLKP → TMDS_CONN_CLKP; TMDS_CLKN → TMDS_CONN_CLKN
L73 CRITICAL 90-OHM-200MA SM — TMDS_DN<1> → TMDS_CONN_DN<1>; TMDS_DP<1> → TMDS_CONN_DP<1>
L74 CRITICAL 90-OHM-200MA SM — TMDS_DN<2> → TMDS_CONN_DN<2>; TMDS_DP<2> → TMDS_CONN_DP<2>

LCD INTERFACE

LVDS INTERFACE

100K pull-ups are for no-panel case (development) Panel has 2K pull-ups

+3V_SLEEP
R342 100K 5% 1/16W MF 402 — LVDS_DDC_CLK
R320 100K 5% 1/16W MF 402 — LVDS_DDC_DATA
C449 0.001uF 20% 50V CERM 402 — NO STUFF
C452 0.001uF 20% 50V CERM 402
C416 0.001uF 20% 50V CERM 402
CHGND4

J6 CRITICAL G-501973 F-RT-SM

+3V_LCD	1	(LVDS DDC POWER)
	2	
	3	
	4	NC
	5	
	6	
	7	
LVDS_L0N	8	
LVDS_L0P	9	
	10	
LVDS_L1N	11	
LVDS_L1P	12	
	13	
LVDS_L2N	14	
LVDS_L2P	15	
	16	
CLKLVDS_LN	17	
CLKLVDS_LP	18	
	19	
LVDS_U0N	20	
LVDS_U0P	21	
	22	
LVDS_U1N	23	
LVDS_U1P	24	
	25	
LVDS_U2N	26	
LVDS_U2P	27	
	28	
CLKLVDS_UN	29	
CLKLVDS_UP	30	
	33	

C500 0.001uF 20% 50V CERM 402 — CHGND4

LCD POWER SWITCHES

+3V_MAIN
R400 100K 5% 1/16W MF 402
C484 2200pF 5% 50V CERM 603 — LCD_PWREN_L
R391 100K 5% 1/16W MF 402 — LCD_DIGON_L
Q11 TSOP SI3443DV — +3V_LCD_SW
L6 FERR-250-OHM SM
C474 0.001uF 20% 50V CERM 402
Q8 2N7002 SM — FP_PWR_EN

INVERTER INTERFACE

+PBUS
L33 FERR-1K-OHM-EMI SM — +12_8V_INV
+5V_MAIN
Q7 FDG6324L SC70-6 — +5V_INV_UF_SW → +5V_INV_SW
R317 100K 5% 1/16W MF 402 — FP_PWR_EN_L
L32 400-OHM-EMI SM-1
C440 10UF 20% 6.3V CERM 805
C746 0.001UF 20% 50V CERM 402
J7 CRITICAL SM-2MT
Q7 FDG6324L SC70-6 — FP_PWR_EN
L31 400-OHM-EMI SM-1 — BRIGHT_PWM
C749 0.001UF 20% 50V CERM 402
C739 0.001UF 20% 50V CERM 402
+3V_PMU
C552 0.1UF 20% 10V CERM 402
U24 74LVC32 TSSOP — INV_ON_PWM; BRIGHT_PWM_UF
INVERTER EXPECTS ACTIVE HIGH SIGNAL
SHARES LOGIC WITH KB RESET SIGNALS (PG 28)
R724 0 5% 1/16W MF 402
C744 0.01uF 20% 50V CERM 603
CHGND2

S-VIDEO/COMP OUT INTERFACE

Place GND shorts at graphics controller

XW12 SM — GPU_TV_GND1 → TV_GND1
L26 FERR-10-OHM-500MA SM
C712 0.01UF 20% 50V CERM 603
L25 3.3UH 0603 — GPU_Y → TV_Y
C702 560PF 10% 50V CERM 402
C707 560PF 10% 50V CERM 402
J15 CRITICAL MINIDIN RT-TH MH1177 — TV_C; TV_Y; TV_COMP
L29 3.3UH 0603 — GPU_C
C718 560PF 10% 50V CERM 402
C724 560PF 10% 50V CERM 402
L27 3.3UH 0603 — GPU_COMP
C714 560PF 10% 50V CERM 402
C713 560PF 10% 50V CERM 402
XW13 SM — GPU_TV_GND2 → TV_GND2
L28 FERR-10-OHM-500MA SM
C717 0.01UF 20% 50V CERM 603
CHGND1

Place GND shorts at graphics controller

VIDEO CONNECTORS

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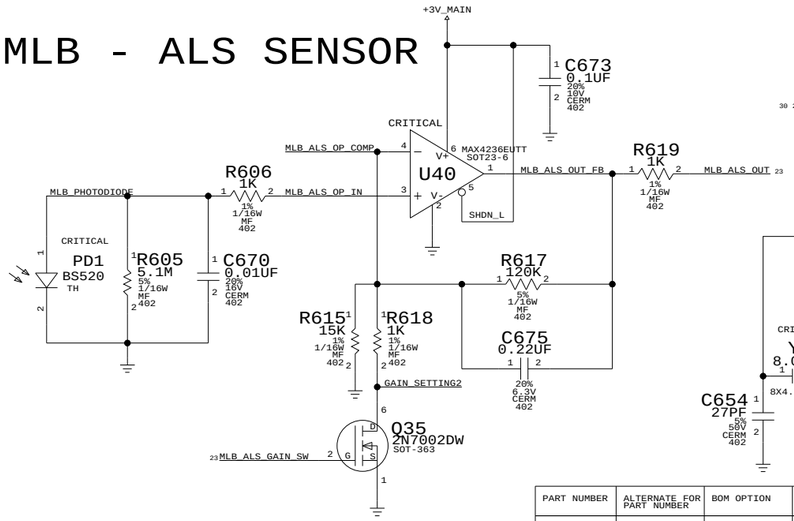
SIZE	DRAWING NUMBER	REV.
D	401258	AA
SCALE: NONE	SHT 22 OF 44	

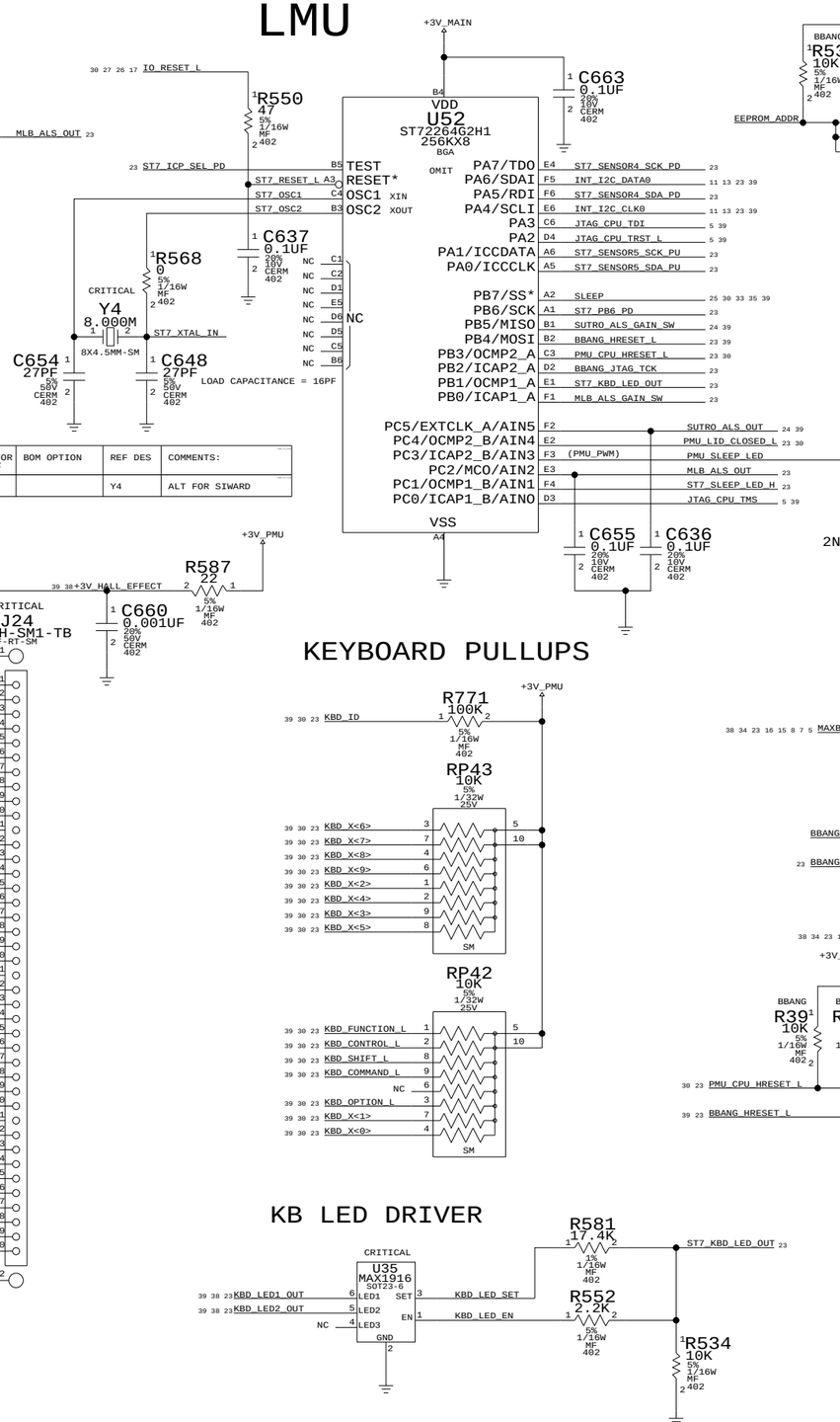
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1194	1	IC,LMU,P84	U52	CRITICAL	?

MLB - ALS SENSOR

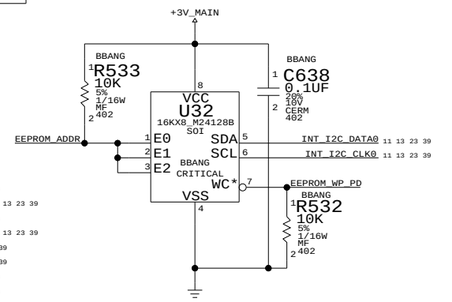


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0008	197S0040		Y4	ALT FOR SIWARD

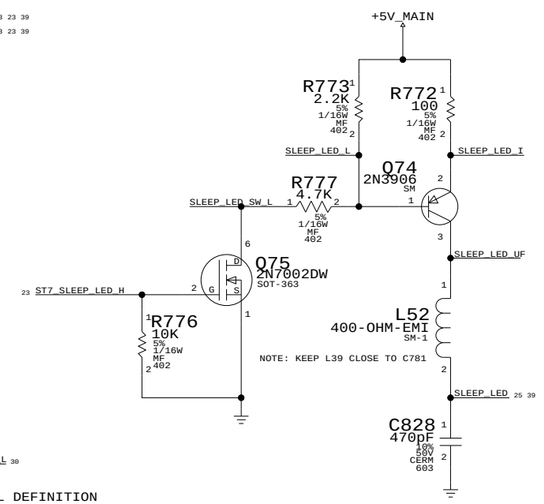
LMU



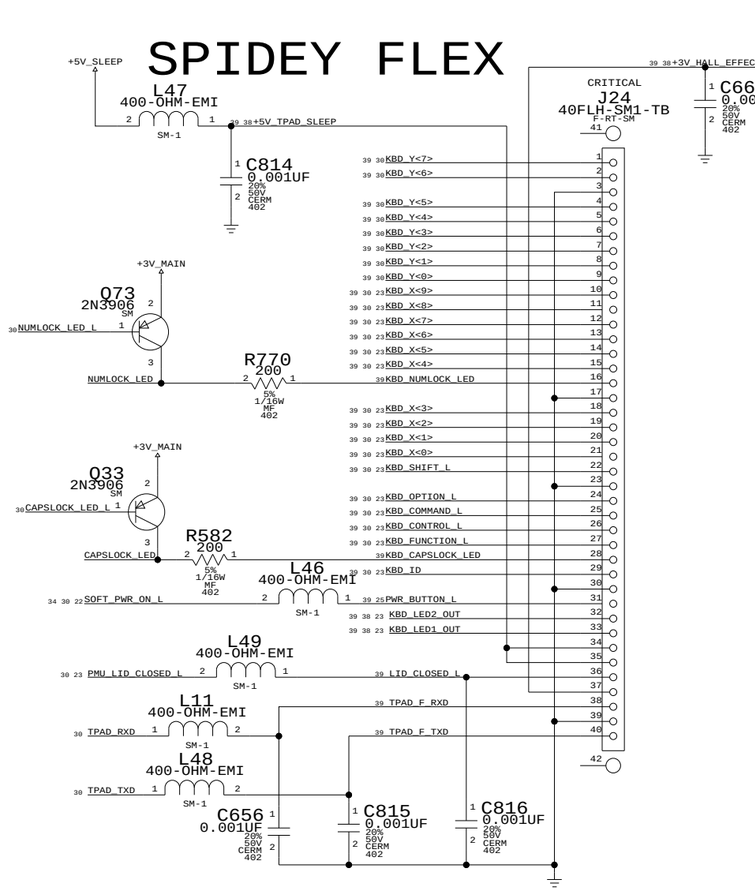
BOOT BANGER E2PROM



SLEEP LED



SPIDEY FLEX

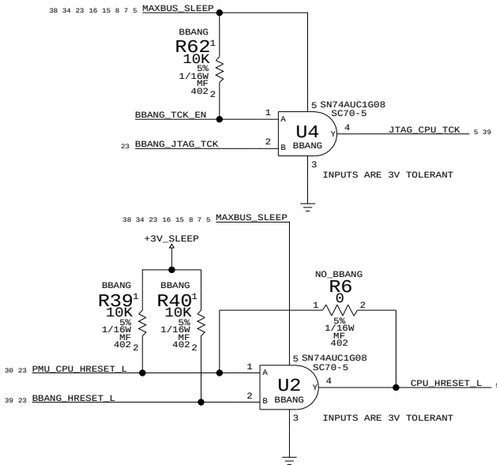


KEYBOARD PULLUPS

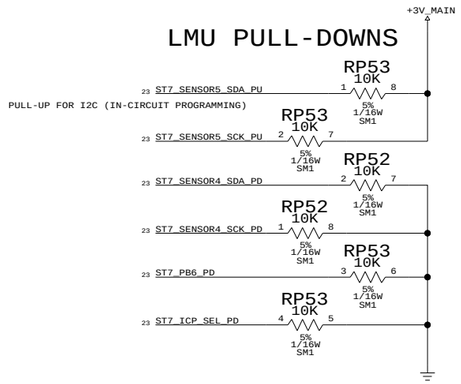
KB LED DRIVER

BOOT BANGING SIGNAL DEFINITION

1/ BBANG_HRESET_L (OPEN COLLECTOR OUTPUT - 10K PULLUP ON MLB)
2/ PMU_HRESET_L (3V INPUT INTO LMU)
3/ BBANG_JTAG_TCK (REGULAR OUTPUT)
4/ JTAG_CPU_TMS (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
5/ JTAG_CPU_TDI (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
6/ JTAG_CPU_TRST_L (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)



LMU PULL-DOWNS



LMU/BOOTBANGER/SPIDEY

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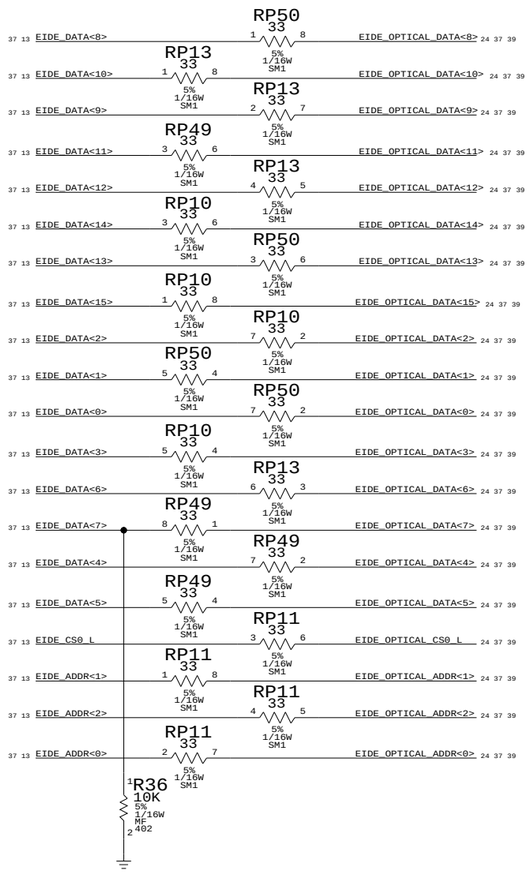
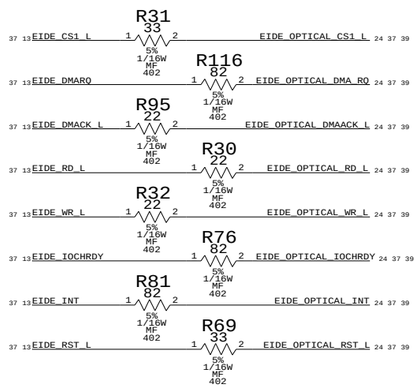
SCALE: NONE	SHT 23 OF 44	

HARD DRIVE INTERFACE (UATA100)

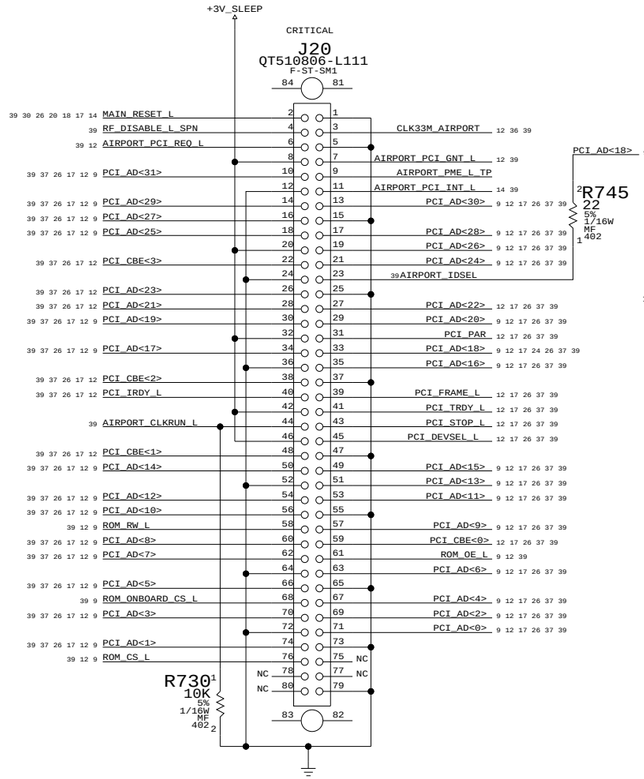
EIDE SERIES TERMINATION

PLACE TERMINATORS NEAR INTREPID

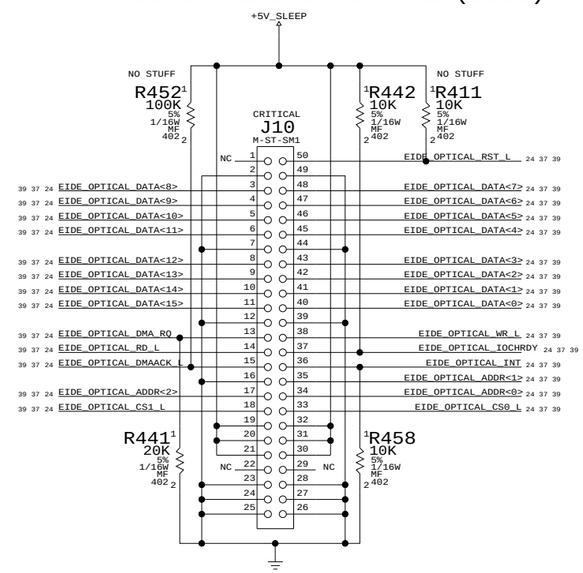




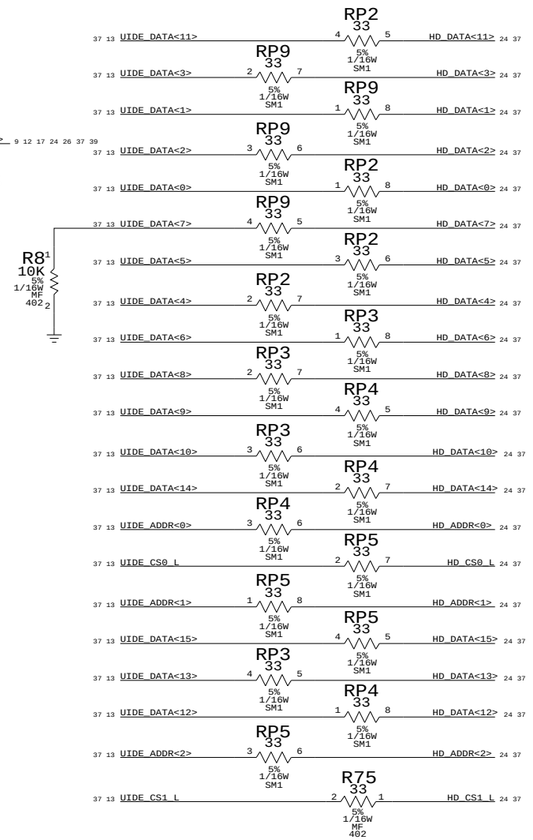
WIRELESS INTERFACE



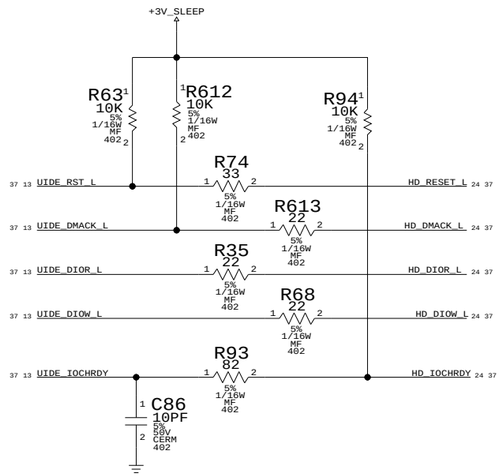
OPTICAL DRIVE INTERFACE (EIDE)



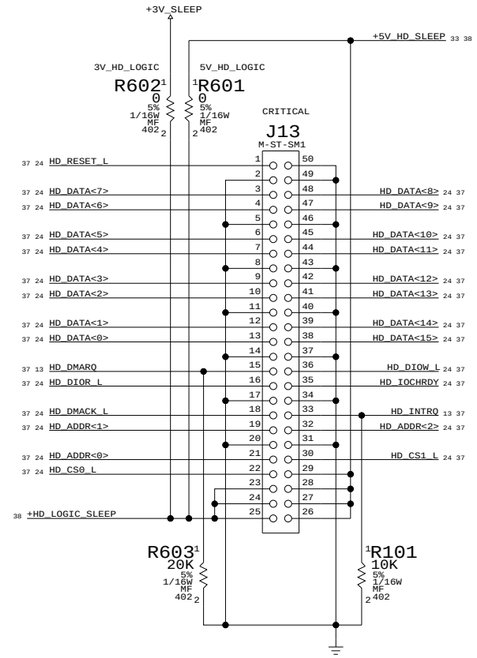
PLACE SERIES R CLOSE TO INTERPID



PLACE PULLUP RESISTORS CLOSE TO INTREPID

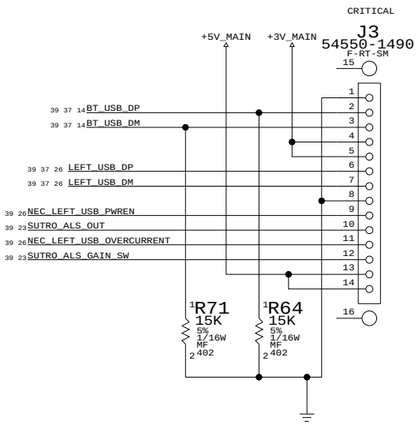


IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V



ANY SEQUENCING REQUIREMENT BETWEEN +5V_HD_SLEEP AND +3V_SLEEP?

BLUETOOTH/LEFT-SIDE USB



INTERNAL I/O CONNECTORS

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	401258	AA
	SCALE: NONE	SHT 24 OF 44	

SOUND BOARD (SOUSAPHONE)

AUDIO - SNAPPER
SND - INTREPID

L77 FERR-220-OHM 0402 — SND_SYNC → SND_SYNC_F
C895 NO STUFF 0.01UF 20% 16V CERM 402
L80 FERR-220-OHM 0402 — SND_CLKOUT → SND_CLKOUT_F
C899 NO STUFF 0.01UF 20% 16V CERM 402
L81 FERR-220-OHM 0402 — INT_AUDIO_TO_SND → INT_AUDIO_TO_SND_F
C896 NO STUFF 0.01UF 20% 16V CERM 402
L82 FERR-220-OHM 0402 — SND_TO_AUDIO → SND_TO_AUDIO_F
C897 NO STUFF 0.01UF 20% 16V CERM 402
L76 FERR-220-OHM 0402 — SND_AMP_MUTE → SND_AMP_MUTE_F
C898 NO STUFF 0.01UF 20% 16V CERM 402
L78 FERR-220-OHM 0402 — SND_HW_RESET_L → SND_HW_RESET_L_F
C900 NO STUFF 0.01UF 20% 16V CERM 402
L79 FERR-220-OHM 0402 — SND_SCLK → SND_SCLK_F
C901 NO STUFF 0.01UF 20% 16V CERM 402

+3V_MAIN, +5V_MAIN

CRITICAL
J12 QT510306-L111 F-ST-SM1

INT_AUDIO_TO_SND_F	1	2	SND_TO_AUDIO_F
	3	4	SND_HP_SENSE_L
INT_I2C_CLK2	5	6	SND_LIN_SENSE_L
SND_SCLK_F	7	8	
	9	10	SND_AMP_MUTE_F
SND_CLKOUT_F	11	12	SLEEP
SND_SYNC_F	13	14	
INT_I2C_DATA2	15	16	SND_HW_RESET_L_F
SLEEP_LED	17	18	
	19	20	
	21	22	SND_HP_MUTE_INV
	23	24	
	25	26	
	27	28	
	29	30	

XW9 SM — SND_AGND

RP44 100K 5% 1/16W SM1 — SND_AMP_MUTE
Q26 2N7002DW SOT-363 — SND_AMP_MUTE_L, AMP_CONTROL
RP44 100K 5% 1/16W SM1 — AMP_CONTROL → INT_PU_RESET_L
Q26 2N7002DW SOT-363

RP44 100K 5% 1/16W SM1 — SND_HP_MUTE_INV
R689 100K 5% 1/16W MF 402
Q31 2N7002DW SOT-363 — SND_HP_MUTE
Q31 2N7002DW SOT-363 — SND_HP_MUTE_L
RP44 100K 5% 1/16W SM1 — AMP_CONTROL

MODEM

SUPPORTS BOTH THE LAST DASH AND Q52 SOFT MODEM

C767 10UF 20% 6.3V CERM 805
NO STUFF C513 0.1UF 20% 10V CERM 402
R405 10K 5% 1/16W MF 402
NO STUFF C478 0.1UF 20% 10V CERM 402
C469 10UF 20% 6.3V CERM 805

CRITICAL
J8 QT510166-L010 F-ST-SM1

MOD_DTO	1	2	MOD_SYNC
MOD_CLKOUT	3	4	INT_MOD_DTI
	5	6	MOD_BITCLK
COMM_RESET_L	7	8	
COMM_SHUTDOWN	9	10	MODEM_USB_DM
INT_I2C_CLK2	11	12	MODEM_USB_DP
INT_I2C_DATA2	13	14	COMM_RING_DET_L
	15	16	

SERIAL DEBUG INTERFACE

SERIAL_DEBUG CRITICAL J16 M-ST-5087 SM

COMM_TXD_L	1	10	COMM_DTR_L
COMM_TRXC	2	9	COMM_RTS_L
	3	8	
COMM_GPIO_L	4	7	COMM_RXD
	5	6	

DEBUG POWER BUTTON

NO STUFF R527 0 5% 1/16W MF 603 — PWR_BUTTON_L

DEBUG JUMPERS

R293 10K 5% 1/16W MF 402 — FANL_PWM
R295 10K 5% 1/16W MF 402 — FANR_PWM
NO STUFF R537 0 5% 1/16W MF 603 — PMU_NMI_BUTTON_L
NO STUFF R553 0 5% 1/16W MF 603 — PMU_RESET_BUTTON_L

FAN CONTROLLER

R814 10 5% 1/16W MF 402
C904 1UF 20% 10V CERM 603
C711 0.1UF 20% 10V CERM 402
R42 10K 5% 1/16W MF 402
R692 10K 5% 1/16W MF 402
R695 10K 5% 1/16W MF 402
Q78 2N7002DW SOT-363
Q78 2N7002DW SOT-363

U3 ADT7460 QSOP

ADT7460_VCORE_MON	14	15	ADT7460_FAN1_PWM
INT_I2C_DATA1	16	16	FANL_TACH
INT_I2C_CLK1	1	5	ADT7460_FAN2_PWM
		7	FANR_TACH
		8	ADT7460_ADR_EN_L
		4	NC
		9	ADT7460_THERM
THERM1_DP	13		
THERM1_DM	12		
THERM2_DP	11		
THERM2_DM	10		
	2		GND

NO STUFF C690 0.001UF 20% 50V CERM 402
NO STUFF C688 0.001UF 20% 50V CERM 402
NO STUFF C846 0.001UF 20% 50V CERM 402
NO STUFF C905 0.001UF 20% 50V CERM 402

RIGHT FAN (GPU)

CRITICAL J2 SM-2MT

FANR_GND	4	1	
FANR_TACH		2	
		3	
		5	

Q36 SI3446DV TSOP — PLACE CLOSE TO CONNECTOR C135 4.7UF 20% 16V CERM 1206

LEFT FAN (CPU)

R679 10K 5% 1/16W MF 402

CRITICAL J4 SM-2MT

FANL_TACH	4	1	
FANL_GND		2	
		3	
		5	

Q37 SI3446DV TSOP — PLACE CLOSE TO CONNECTOR C134 4.7UF 20% 16V CERM 1206

PLACE XW9 CLOSE TO 5V SWITCHER (U27)
PLACE CAPS AS CLOSE TO THERMISTORS AS POSSIBLE
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY

CAPS FOR EMI EXPERIMENTATION ONLY

FAN INTERFACE

MAIN1
C681 0.001UF 20% 50V CERM 402 — Q66 2N3904 SM — SUPPLY_M_DP, SUPPLY_M_DM

PLACE CLOSE TO CPU
MAIN2
C668 0.001UF 20% 50V CERM 402 — Q39 2N3904 SM — CPU_M_DP, CPU_M_DM

PLACE UNDERNEATH UPPER RAM
ALTERNATE1
C678 NO STUFF 0.001UF 20% 50V CERM 402 — Q47 2N3904 SM — THERM1_A_DP, THERM1_A_DM

PLACE CLOSE TO BATTERY CHARGER/VCORE
ALTERNATE2
C651 NO STUFF 0.001UF 20% 50V CERM 402 — Q62 2N3904 SM — THERM2_A_DP, THERM2_A_DM

KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

R719 0 5% 1/16W MF 402 — CPU_M_DP → THERM1_DP
R725 0 5% 1/16W MF 402 — CPU_M_DM → THERM1_DM
R713 0 5% 1/16W MF 402 — SUPPLY_M_DP → THERM2_DP
R716 0 5% 1/16W MF 402 — SUPPLY_M_DM → THERM2_DM

KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

NO STUFF R723 0 5% 1/16W MF 402 — THERM1_A_DP → THERM1_DP
NO STUFF R726 0 5% 1/16W MF 402 — THERM1_A_DM → THERM1_DM
NO STUFF R710 0 5% 1/16W MF 402 — THERM2_A_DP → THERM2_DP
NO STUFF R717 0 5% 1/16W MF 402 — THERM2_A_DM → THERM2_DM

THERM ISOLATION

R811 100K 5% 1/16W MF 402 — +3V_MAIN
R812 100K 5% 1/16W MF 402 — +3V_PMU_AVCC, THERM_L_OC
R813 100K 5% 1/16W MF 402 — THERM_INV
Q87 2N7002DW SOT-363 — ADT7460_THERM, THERM_INV
Q87 2N7002DW SOT-363 — THERM_L_OC
C903 0.1UF 20% 10V CERM 402

FAN/MODEM/SOUND/SLEEP LED/DEBUG

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401258	AA
SCALE: NONE	SHT 25 OF 44	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0608	197S0038	NEC_USB	Y5	ALT FOR SIWARD

Y7 LOAD CAPACITANCE IS 16PF

SERR_L AND PERR_L
HAS DEDICATED PULL-UP
FOR BOTH CBUS AND USB2

Series Rpaks required to facilitate NAND-tree testing

Low/Full/High Speed (External)

Low/Full/High Speed (External)

Tie to GND at ball N11

NEED PULL-UP RESISTORS IN CASE USB 1.0 IS USED FOR PORT POWER

PLACE NEAR J3

SUTRO CONNECTOR

PLACE NEAR J12

BUBBA CONNECTOR

INTREPID USB CONSTRAINTS

USB 2.0

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401258	AA
SCALE: NONE	SHT 26 OF 44	

Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

+3V_MAIN

C442 10uF 20% 6.3V CERM 805

NO STUFF R333 0 5% 1/16W MF 402

3405_MODE

R319 0 5% 1/16W MF 402

U14 LTC3405 SOT23-6 CRITICAL — VIN, RUN, MODE, SW, VFB, GND

LTC3405_SW 38

CRITICAL L5 3.3uH SM1

R334 665K 1% 1/16W MF 402 R2A

C471 22pF 5% 50V CERM 402

R361 49.9K 1% 1/16W MF 402 R2B

R362 182K 1% 1/16W MF 402 R1

C486 10uF 20% 6.3V CERM 805

3405_VFB

+1_0V_MARVELL 38

VOUT = 0.8V*(1+R2EQV/R1)
R2EQV = R2A||R2B

PLACE ALL SERIES RES CLOSE TO PHY

R370 0 5% 1/16W MF 402 — 36 13 CLKENET_LINK_TX — 36 CLKENET_PHY_TX

R353 0 5% 1/16W MF 402 — 36 13 CLKENET_LINK_RX — 36 CLKENET_PHY_RX

R344 0 5% 1/16W MF 402 — 36 13 CLKENET_LINK_GBE_REF — 36 CLKENET_PHY_GBE_REF

CRITICAL U49 88E1111 BCC

TX_CLK	4	
RX_CLK	2	
125CLK	22	
TXD0	11	37 13 ENET_PHY_TXD<0>
TXD1	12	37 13 ENET_PHY_TXD<1>
TXD2	14	37 13 ENET_PHY_TXD<2>
TXD3	16	37 13 ENET_PHY_TXD<3>
TXD4	17	37 13 ENET_PHY_TXD<4>
TXD5	18	37 13 ENET_PHY_TXD<5>
TXD6	19	37 13 ENET_PHY_TXD<6>
TXD7	20	37 13 ENET_PHY_TXD<7>
TX_EN	9	37 13 ENET_PHY_TX_EN
TX_ER	7	37 13 ENET_PHY_TX_ER
GTX_CLK	8	36 13 CLKENET_PHY_GTX
RXD0	95	37 13 ENET_LINK_RXD<0>
RXD1	92	37 13 ENET_LINK_RXD<1>
RXD2	93	37 13 ENET_LINK_RXD<2>
RXD3	91	37 13 ENET_LINK_RXD<3>
RXD4	90	37 13 ENET_LINK_RXD<4>
RXD5	89	37 13 ENET_LINK_RXD<5>
RXD6	87	37 13 ENET_LINK_RXD<6>
RXD7	86	37 13 ENET_LINK_RXD<7>
RX_DV	94	37 13 ENET_RX_DV
RX_ER	3	37 13 ENET_RX_ER
CRS	84	37 13 ENET_CRS
COL	83	37 13 ENET_COL
MDC	25	37 13 ENET_MDC
MDIO	24	37 13 ENET_MDIO
INT-/	23	14 ENET_ENERGY_DET
INT+		
RESET	28	ENET_RST_L
COMA	27	ENET_COMA
S_IN+	NC 82	
S_IN-	NC 81	
S_OUT+	NC 77	
S_OUT-	NC 75	
S_CLK+	NC 79	
S_CLK-	NC 80	
HSDAC+	37	ENET_HSDACP
HSDAC-	38	ENET_HSDACM
XTAL1	55	36 CLK25M_ENET_XIN
XTAL2	54	36 CLK25M_ENET_XOUT
VSSC	53	ENET_VSSC
CTRL10	51 NC	
DVDD	1, 6, 10, 15, 57, 62, 67, 71, 85	
VDDO	5, 21, 88, 96	
VDDOH	52, 66, 72	
VDDOX	26, 48	
AVDD	32, 35, 36, 40, 45, 78	
MDI0+	29	37 MDI_P<0>
MDI0-	31	37 MDI_M<0>
MDI1+	33	37 MDI_P<1>
MDI1-	34	37 MDI_M<1>
MDI2+	39	37 MDI_P<2>
MDI2-	41	37 MDI_M<2>
MDI3+	42	37 MDI_P<3>
MDI3-	43	37 MDI_M<3>
LED_LINK10	76	LED_LINK10
LED_LINK100	74	LED_LINK100
LED_LINK1000	73 NC	
LED_DUPLEX	70 NC	
LED_RX	69	LED_RX_SPN
LED_TX	68 NC	
CONFIG0	65	(000)
CONFIG1	64	(000)
CONFIG2	63	(111)
CONFIG3	61	(110)
CONFIG4	60	(111)
CONFIG5	59	(101)
CONFIG6	58	(000)
TDI	44	JTAG_ENET_TDI 13
TDO	50	JTAG_ASIC_TDO_TP 39
TCK	49	JTAG_ASIC_TCK 13 39
TMS	46	JTAG_ASIC_TMS 13 39
TRST	47	JTAG_ASIC_TRST_L 13 39
RSET	30	ENET_RSET
SEL_OSC	56 NC	
SEL_2.5V	13	
GND	97	

SEE CONFIG TABLES (BELOW)

C492 0.1UF 20% 10V CERM 402
C511 0.01UF 20% 10V CERM 402
C517 0.1UF 20% 10V CERM 402
C502 0.01UF 20% 10V CERM 402
C465 0.1UF 20% 10V CERM 402
C475 0.01UF 20% 10V CERM 402
PLACE CAPS (IN ORDER) ON PINS 1, 6, 10/15, 57/62, 67/71, 85

C464 0.1UF 20% 10V CERM 402
C472 0.01UF 20% 10V CERM 402
C453 0.1UF 20% 10V CERM 402
C503 0.01UF 20% 10V CERM 402
C501 0.1UF 20% 10V CERM 402
C496 10uF 20% 6.3V CERM 805
38 27 +2_5V_MARVELL
PLACE CAPS (IN ORDER) ON PINS 5, 21/26, 48/52, 66/72, 88, 96

C497 0.1UF 20% 10V CERM 402
C504 0.01UF 20% 10V CERM 402
C487 0.1UF 20% 10V CERM 402
C476 0.01UF 20% 10V CERM 402
C754 10uF 20% 6.3V CERM 805
38 +2_5V_MARVELL_AVDD
PLACE CAPS (IN ORDER) ON PINS 32/35, 36/40, 45 & 78

L34 FERR-EMI-600-OHM SM

+2_5V_MAIN

R465 0 5% 1/16W MF 603

C488 0.1UF 20% 10V CERM 402
C466 0.1UF 20% 10V CERM 402
C506 0.1UF 20% 10V CERM 402
C520 0.1UF 20% 10V CERM 402
PLACE CAPS AT TRANSFORMER PINS 1, 4, 7 & 10

PLACE CLOSE TO ETHERNET CONNECTOR

NO STUFF R438 0 5% 1/10W MF 805 — CHGND1

CRITICAL J17 RJ45 RT-TH

12	39 37 13	RJ45_DP<0>
10	15	RJ45_C0_PD
11	39 37 14	RJ45_DN<0>
9	39 37 16	RJ45_DP<1>
7	18	RJ45_C1_PD
8	39 37 17	RJ45_DN<1>
6	39 37 19	RJ45_DP<2>
4	21	RJ45_C2_PD
5	39 37 20	RJ45_DN<2>
3	39 37 22	RJ45_DP<3>
1	24	RJ45_C3_PD
2	39 37 23	RJ45_DN<3>

XFR-ENET-1000BT T1 SM CRITICAL

Short shielded RJ-45 — CHGND1

R735 75 5% 1/16W MF 402
R733 75 5% 1/16W MF 402
R382 75 5% 1/16W MF 402
R347 75 5% 1/16W MF 402
ENET_CTAP_CHGND 38

C457 100pF 10% 3KV CERM 1808 — CHGND1

R346 49.9 1% 1/16W MF 402 — R355 49.9 1% 1/16W MF 402 — MDI0_PD — C454 0.01UF 20% 10V CERM 402
R372 49.9 1% 1/16W MF 402 — R381 49.9 1% 1/16W MF 402 — MDI1_PD — C477 0.01UF 20% 10V CERM 402
R404 49.9 1% 1/16W MF 402 — R406 49.9 1% 1/16W MF 402 — MDI2_PD — C493 0.01UF 20% 10V CERM 402
R413 49.9 1% 1/16W MF 402 — R428 49.9 1% 1/16W MF 402 — MDI3_PD — C505 0.01UF 20% 10V CERM 402
PLACE RESISTORS CLOSE TO PHY

+2_5V_MARVELL

R371 10K 5% 1/16W MF 402
R345 10K 5% 1/16W MF 402
R354 1.5K 5% 1/16W MF 402
R343 1K 5% 1/16W MF 402 — 14 INT_ENET_RST_L

D1 1N914 SOT23 — 30 26 23 17 IO_RESET_L

Q15 2N7002DW SOT-363 — 31 30 29 AC_IN
Q15 2N7002DW SOT-363 — 35 34 33 19 SLEEP_L_LS5

C755 2.2uF 10% 10V CERM 805

PLACES PHY IN "COMA" MODE WHEN ASLEEP ON BATTERY (SAVES POWER)

PUT CRYSTAL CIRCUIT CLOSE TO PHY

NO STUFF R435 20K 5% 1/16W MF 402

CRITICAL Y3 25.0000M 8X4.5MM-SM

C555 33pF 5% 50V CERM 402
C491 33pF 5% 50V CERM 402
CLK25M_XTAL_IN

Y3'S LOAD CAPACITANCE IS 20PF

R427 0 5% 1/16W MF 402

NO STUFF R393 49.9 1% 1/16W MF 402
NO STUFF R403 49.9 1% 1/16W MF 402
R335 10K 5% 1/16W MF 402

R380 4.99K 1% 1/16W MF 402

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0703	197S0037	ALTERNATE	Y3	
197S0603	197S0037	ALTERNATE	Y3	ALT FOR SIWARD

CONFIG DEFINITIONS

PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS

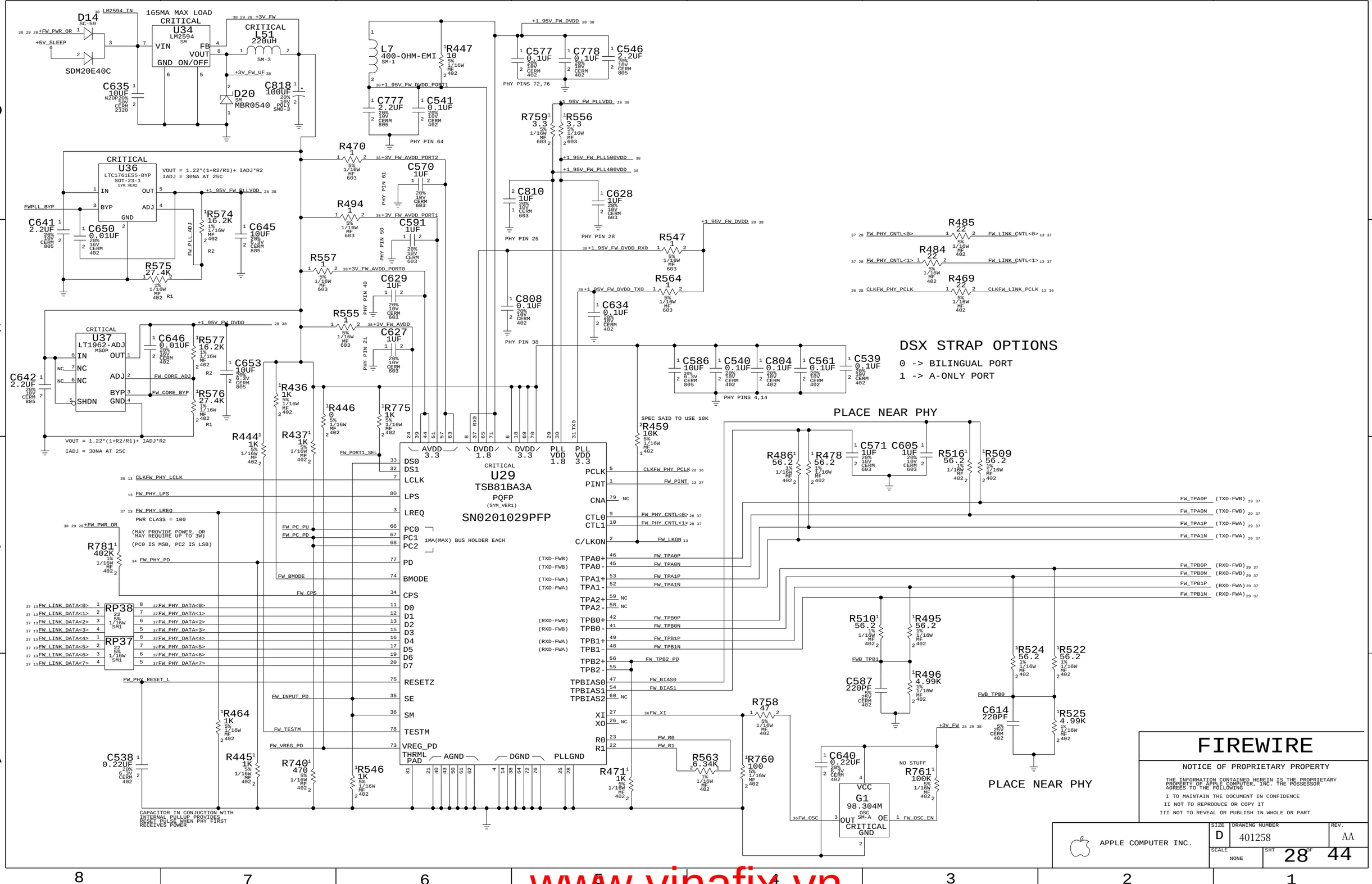
PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

MARVELL 88E1111

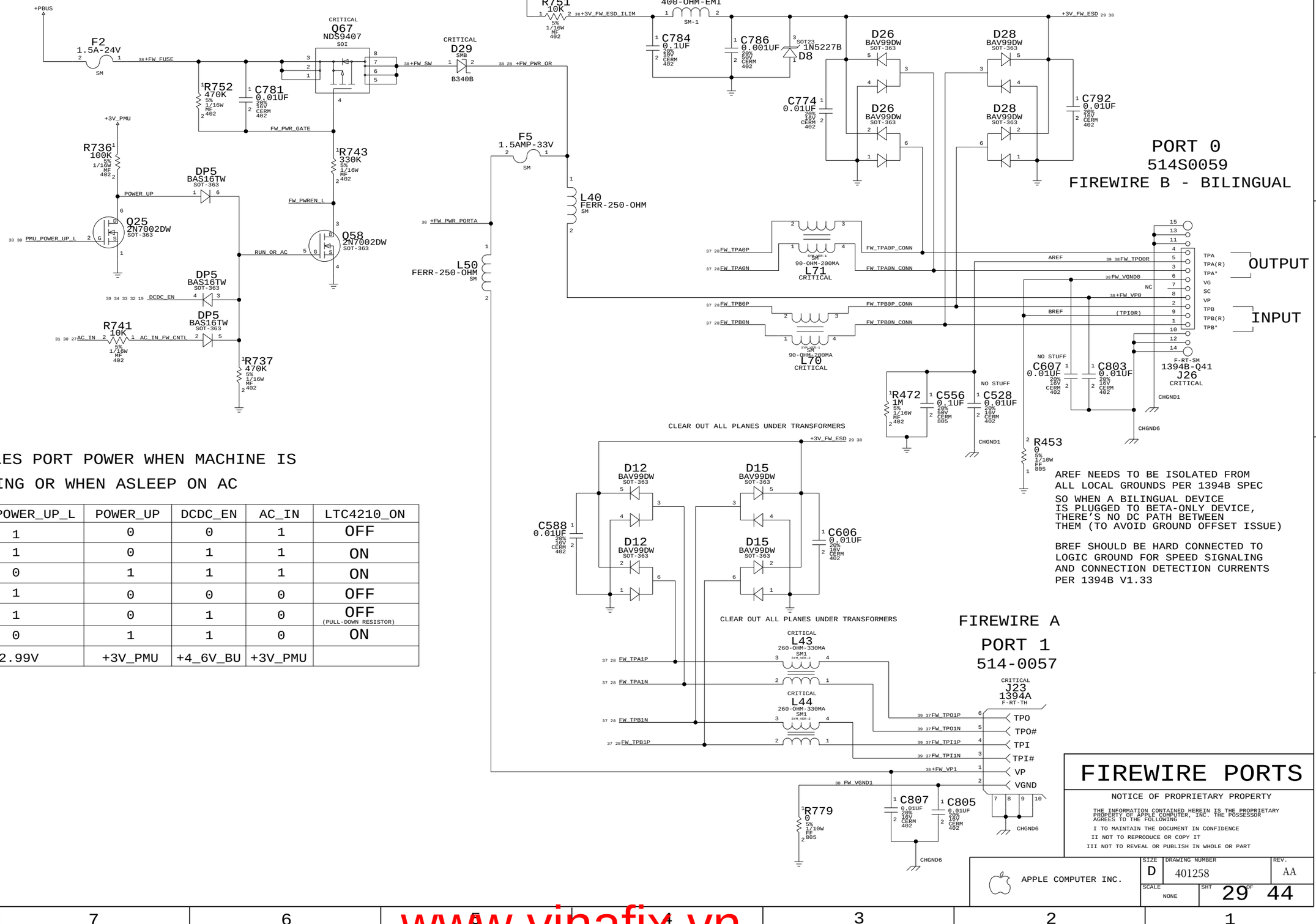
10/100/1000 ETHERNET

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401258	AA
SCALE: NONE	SHT 27 OF 44	



PORT POWER SWITCH



PORT 0
514S0059
FIREWIRE B - BILINGUAL

ENABLES PORT POWER WHEN MACHINE IS RUNNING OR WHEN ASLEEP ON AC

STATE	PMU_POWER_UP_L	POWER_UP	DCDC_EN	AC_IN	LTC4210_ON
SHUTDOWN (AC)	1	0	0	1	OFF
SLEEP (AC)	1	0	1	1	ON
RUN (AC)	0	1	1	1	ON
SHUTDOWN (BATT)	1	0	0	0	OFF
SLEEP (BATT)	1	0	1	0	OFF (PULL-DOWN RESISTOR)
RUN (BATT)	0	1	1	0	ON
	2.99V	+3V_PMU	+4_6V_BU	+3V_PMU	

AREF NEEDS TO BE ISOLATED FROM ALL LOCAL GROUNDS PER 1394B SPEC

SO WHEN A BILINGUAL DEVICE IS PLUGGED TO BETA-ONLY DEVICE, THERE'S NO DC PATH BETWEEN THEM (TO AVOID GROUND OFFSET ISSUE)

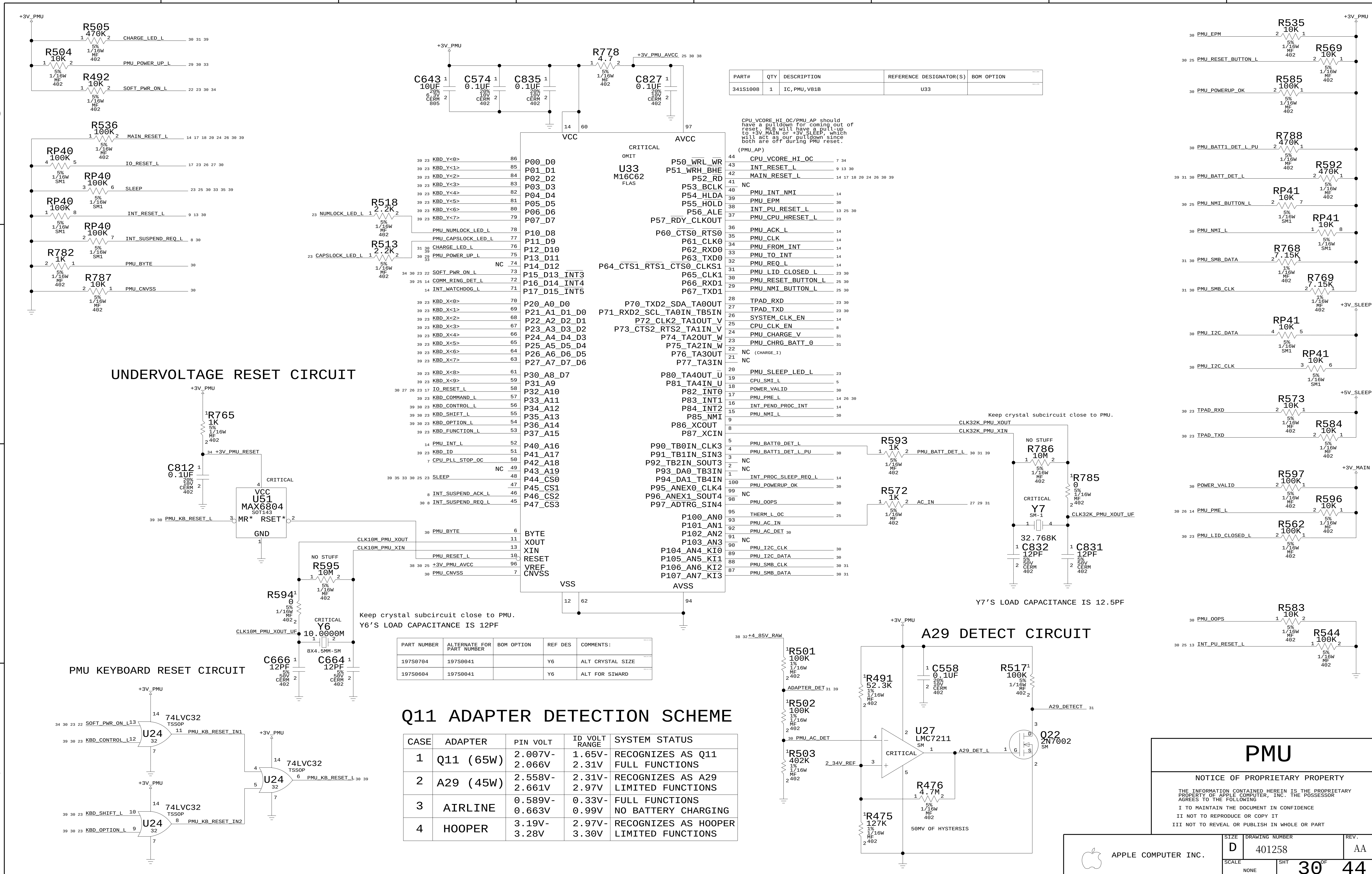
BREF SHOULD BE HARD CONNECTED TO LOGIC GROUND FOR SPEED SIGNALING AND CONNECTION DETECTION CURRENTS PER 1394B V1.33

FIREWIRE A
PORT 1
514-0057

FIREWIRE PORTS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401258	AA
SCALE: NONE	SHT 29 OF 44	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1008	1	IC,PMU,V81B	U33	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0704	197S0041		Y6	ALT CRYSTAL SIZE
197S0604	197S0041		Y6	ALT FOR SIWARD

Q11 ADAPTER DETECTION SCHEME

CASE	ADAPTER	PIN VOLT	ID VOLT RANGE	SYSTEM STATUS
1	Q11 (65W)	2.007V-2.066V	1.65V-2.31V	RECOGNIZES AS Q11 FULL FUNCTIONS
2	A29 (45W)	2.558V-2.661V	2.31V-2.97V	RECOGNIZES AS A29 LIMITED FUNCTIONS
3	AIRLINE	0.589V-0.663V	0.33V-0.99V	FULL FUNCTIONS NO BATTERY CHARGING
4	HOOPER	3.19V-3.28V	2.97V-3.30V	RECOGNIZES AS HOOPER LIMITED FUNCTIONS

PMU

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401258	AA
SCALE NONE	SHT 30 OF 44	

DC POWER INPUT

(POWER JACK, ETC. ON SEPARATE BOARD)

CRITICAL

J18
87438-0833
M-RT-SM

1 CHARGE_LED_L 30 39
2
3
4
5
6
7
8 ADAPTER_DET 30 39

38 32 +ADAPTER

NO STUFF
C757 0.1UF 20% 50V CERM 805

PLACE CLOSE TO DC INPUT

R396 20K 1% 1/16W MF 402

R395 102K 1% 1/16W MF 402
R364 102K 1% 1/16W MF 402
R375 10K 1% 1/16W MF 402
R365 57.6K 1% 1/16W MF 402

+3V_PMU

C468 0.01UF 20% 16V CERM 402
R363 10K 1% 1/16W MF 402

U15 LMC7211 SM
CRITICAL

38 32 1V20_REF
AC_DIV
AC_IN
AC_IN_L 31

R394 1M 5% 1/16W MF 402

Q10 2N7002DW SOT-363

R383 470K 5% 1/16W MF 402

GREATER THAN 13.5V DETECT

DC INRUSH LIMITER

Q13 SI4435DY SOI
Q16 SI4435DY SOI

S3 S2 S1 D4 D3 D2 D1 GATE

38 +ADAPTER_SW
38 +ADAPTER_SENSE

R414 330K 5% 1/16W MF 402
C458 0.1UF 20% 50V CERM 805

AC_ENABLE_GATE
R374 470K 5% 1/16W MF 402
AC_ENABLE_L
Q10 2N7002DW SOT-363

BCKFD_PROT_GATE
R474 47K 5% 1/16W MF 402
C592 0.1UF 20% 50V CERM 805
R499 68K 5% 1/16W MF 402
BCKFD_PROT_EN_L
Q21 2N7002DW SOT-363
31 30 29 27 AC_IN

C572 0.01UF 20% 50V CERM 603

PLACE U23 NEXT TO R460
U23 SENSE VOLTAGE DROP ACROSS R460

U23 MAX4172 TSSOP
CRITICAL
RS+ RS- PG NC1 NC2 OUT GND
NC NC MAX4172_OUT

R466 10K 1% 1/16W MF 402
R454 2.21K 0.1% 1/16W MF 603
C883 0.1UF 10% 50V X7R 603

+24V_PBUS

1MSEC INTEGRATION TIME

R742 1K 1% 1/16W MF 402
C771 0.1UF 20% 10V CERM 402
IAC_RC_COMP

+3V_PMU

R747 42.2K 0.1% 1/16W FF 603
C772 0.1UF 20% 10V CERM 402

U50 LMC7111 SOT23-5
CRITICAL
IAC_FB

PLACE R358 CLOSE TO LTC1625
ROUTE LTC1625_ITH CAREFULLY

DP4 BAS16TW SOT-363
LTC1625_ITH
R358 150 1% 1/16W MF 402
1625_COMP 32

ADAPTER_I_REG

CURRENT_THRESHOLD
R738 42.2K 0.1% 1/16W FF 603
R734 82.5K 0.1% 1/16W FF 603
R739 51.1K 0.1% 1/16W FF 603
IF ADAPTER IS OVER 18V, ADJUST CURRENT SETTING

A29_CURRENT_ADJ
R748 100K 1% 1/16W MF 402
OVER_18V_ADJ
Q20 2N7002DW SOT-363
AC_GTR_18V
C775 1UF 20% 10V CERM 603
Q65 2N7002DW SOT-363
31 1772_ACOK_L

31 30 A29_DETECT 5
IF A29 ADAPTER USED, ADJUST CURRENT SETTING

R460 0.025 1% 1W MF 2512

R488 4.7 5% 1/16W MF 402
R498 4.7 5% 1/16W MF 402
1772_CSSP 37
1772_CSSN 37

C578 0.47UF 20% 50V CERM 1206
C579 0.47UF 20% 50V CERM 1206

R754 100K 1% 1/16W MF 402
D9 1N914 SOT23
R755 12.7K 1% 1/16W MF 402
C600 1UF 20% 50V CERM1 1210

38 1772_LDO
R571 33 5% 1/8W FF 1206
D10 1N914 SOT23
1772_BST_ESR
R549 100K 5% 1/16W MF 402
C624 0.1UF 20% 25V CERM 603
R774 4.7 5% 1/16W MF 603
C608 0.1UF 20% 25V CERM 805

+24V_PBUS

CRITICAL
Q63 IRF7805 SM

C547 2.2UF 20% 25V CERM 1812
C562 2.2UF 20% 25V CERM 1812
C563 2.2UF 20% 25V CERM 1812
C557 2.2UF 20% 25V CERM 1812
C564 2.2UF 20% 25V CERM 1812

CRITICAL
L42 10uH SM1
+BATT_RSNS 38
R763 0.05 1% 1W MF 2512
D30 SM MBRS140T3
C619 4.7UF 20% 25V CERM 1206
C632 4.7UF 20% 25V CERM 1206
C617 4.7UF 20% 25V CERM 1206
C824 33UF 20% 25V ELEC SM1
+BATT_24V_FUSE 31 38

CRITICAL
Q64 IRF7811W SO-8
NO STUFF
C906 0.0022UF 10% 50V CERM 402
XW19 SM
R543 1 5% 1/16W MF 603
R511 1 5% 1/16W MF 603
C631 4.7UF 20% 25V CERM 1206
C633 4.7UF 20% 25V CERM 1206
C618 4.7UF 20% 25V CERM 1206

BATTERY SWITCH-OVER CIRCUIT

+BATT
F4 5AMP-125V SM-2
F3 5AMP-125V SM-2
+PBUS
+BATT_24V_FUSE 38
+BATT_14V_FUSE 38

CRITICAL
Q24 SI4435DY SOI
GATE
R490 47K 5% 1/16W MF 402
BATT_24V_GATE
R512 10K 5% 1/16W MF 402
BATT_24PBUS_EN
DP4 BAS16TW SOT-363

CRITICAL
Q76 SUD45P03 TO-252
R746 47K 5% 1/16W MF 402
BATT_14V_GATE
R744 10K 5% 1/16W MF 402
BATT_14PBUS_EN

31 AC_IN_L
DP4 BAS16TW SOT-363
R489 158K 1% 1/16W MF 402
AC_IN_L_RC
C593 10UF 20% 6.3V CERM 805
Q21 2N7002DW SOT-363

WHEN AC IS IN, P-CHANNEL FETS ARE QUICKLY (DIODE) TURNED OFF
WHEN AC IS NOT PLUGGED, P-CHANNEL FETS ARE ON
RC TIME IS 480K*10UF @ +3V_PMU

SWITCHER VOLTAGE CONTROL

PMU SELECTS BETWEEN TWO VOLTAGES

+3V_PMU

R567 27.4K 1% 1/16W MF 402
R558 10K 1% 1/16W MF 402
R548 10K 1% 1/16W MF 402
OD OUTPUT LOW - WHEN AC GREATER THAN 18V
R560 4.12K 1% 1/16W MF 402
R565 48.7K 1% 1/16W MF 402
R566 1K 1% 1/16W MF 402
BATT_LOW_L
R561 100K 5% 1/16W MF 402
BATTV_HIGH
Q27 2N7002DW SOT-363
R580 5.23K 1% 1/16W MF 402
BATTV_LOW
Q27 2N7002DW SOT-363
30 PMU_CHARGE_V
Q29 2N7002DW SOT-363
Q29 2N7002DW SOT-363

SWITCHER CURRENT CONTROL

CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V
CHARGE THROTTLED BY LOW BATTERY VOLTAGE

+3V_PMU
R578 100K 5% 1/16W MF 402
CHARGE_DISABLE
Q30 2N7002DW SOT-363
30 PMU_CHRG_BATT_0
Q30 2N7002DW SOT-363

$V_{BATT} = CELLS \times (4.096 + (0.4096 * V_{VCTL} / V_{REFIN}))$

For 4.15V cells, VCTL = 0.123 REFIN

For 4.20V cells, VCTL = 0.245 REFIN

$I_{CHG} = (0.2048/R_{62}) * (V_{ICTL} / V_{REFIN})$

U31 MAX1772 QSOP
CRITICAL

CSSP CSSN DCIN ACIN ACOK RFIN VCTL ICTL ICHG IINP CCV CCI CCS REF LDO DLOV BST DHI LX DLO PGND CSIP CSIN BATT CELLS GND

38 1772_DCIN
1772_ACIN
31 1772_ACOK_L
(+3V_PMU)
1772_VCTL
1772_ICTL
1772_ICHG
1772_IINP
1772_CCV
1772_CCI
1772_CCS
REF = 4.096V
REF_CLS
38 1772_CELLS
38 1772_DLOV
1772_BST
1772_DHI
38 1772_LX
1772_DLO
(GND)
37 1772_CSIP
37 1772_CSIN

R542 1K 1% 1/16W MF 402
R526 1K 1% 1/16W MF 402
C622 0.01UF 20% 16V CERM 402
C616 0.01UF 20% 16V CERM 402
R497 1K 1% 1/16W MF 402
1772_CCV_RC
C621 0.1UF 20% 16V CERM 402
38 1772_GND
1772_REF
C630 1UF 20% 16V CERM 603
R487 10K 1% 1/16W MF 402
R473 4.12K 1% 1/16W MF 402
1772_CLS

C652 1UF 20% 25V CERM 603
C817 0.1UF 20% 25V CERM 603
C802 0.1UF 20% 25V CERM 603
R559 100K 5% 1/16W MF 402

+3V_PMU
C615 0.1UF 20% 16V CERM 402
R588 100K 1% 1/16W MF 402
R579 499K 1% 1/16W MF 402
BATT_DIV
1V65_REF
R599 100K 1% 1/16W MF 402
R570 100K 1% 1/16W MF 402
C658 0.047UF 10% 16V CERM 402
BATT_LOW

R749 6.34K 1% 1/16W MF 402
A29_CLS_ADJ
31 30 A29_DETECT 5
Q65 2N7002DW SOT-363

38 +BATT_VSNS

BATTERY CONNECTOR

CRITICAL
J25
87438-0833
M-RT-SM

39 38 +BATT_POS (BATT_IN_PD)
39 BATT_CLK
39 BATT_DATA
PMU_BATT_DET_L 30 39
39 38 BATT_NEG

L9 FERR-EMI-100-OHM SM
L53 FERR-50-OHM SM
L10 FERR-EMI-100-OHM SM
PMU_SMB_CLK 30
L8 FERR-EMI-100-OHM SM
PMU_SMB_DATA 30
L12 FERR-50-OHM SM

+BATT

BATTERY CHARGER

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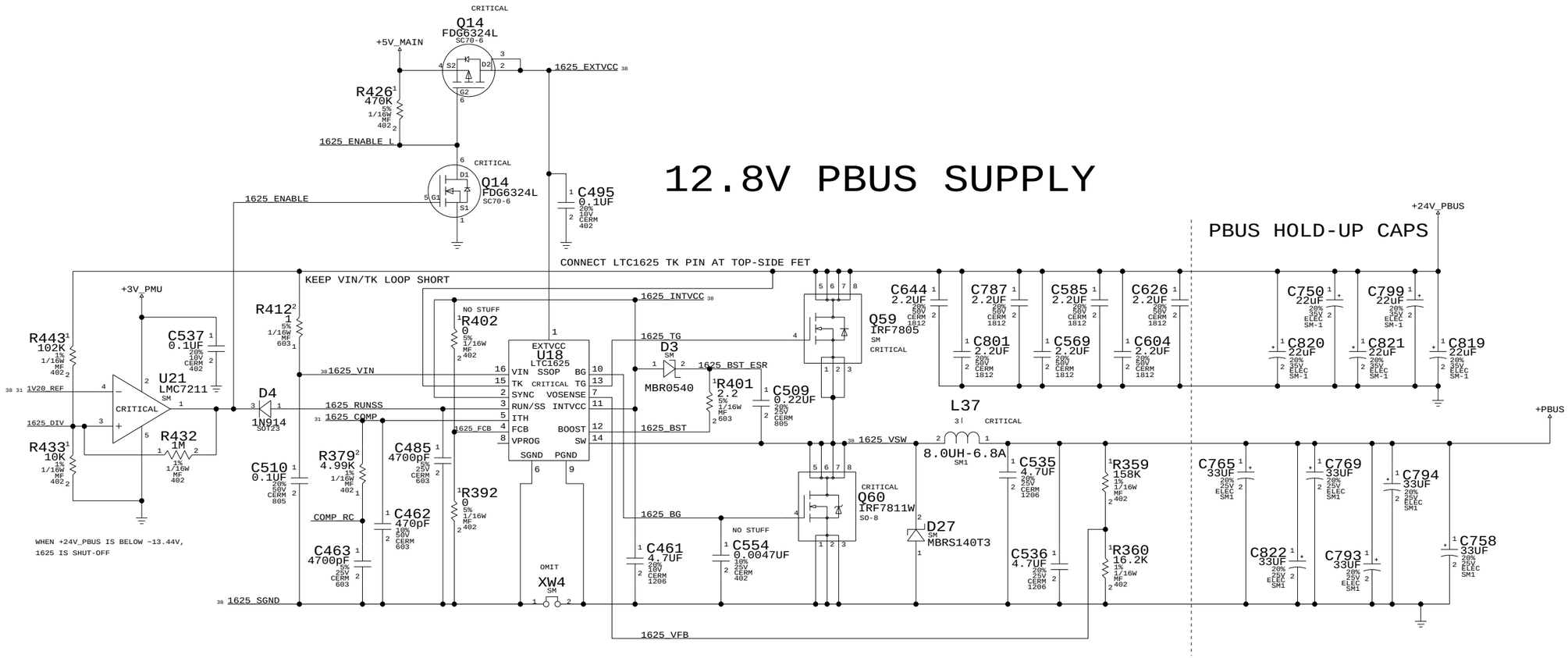
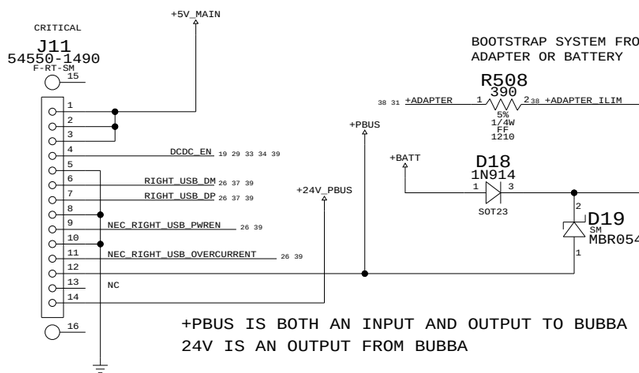
APPLE COMPUTER INC.

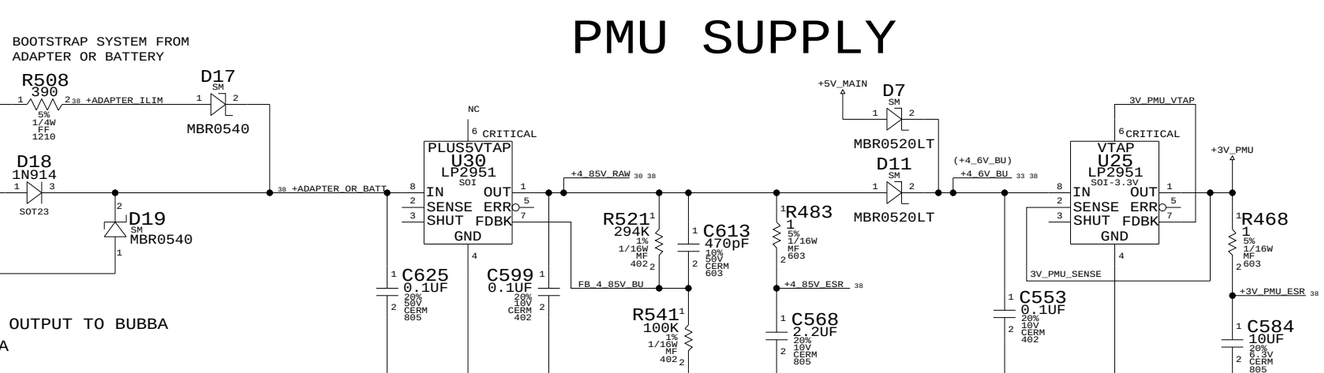
SIZE	DRAWING NUMBER	REV.
D	401258	AA
SCALE: NONE	SHT 31 OF 44	

12.8V PBUS SUPPLY



BACKUP BATTERY / USB CONNECTOR





PMU SUPPLY

12.8V REGULATOR

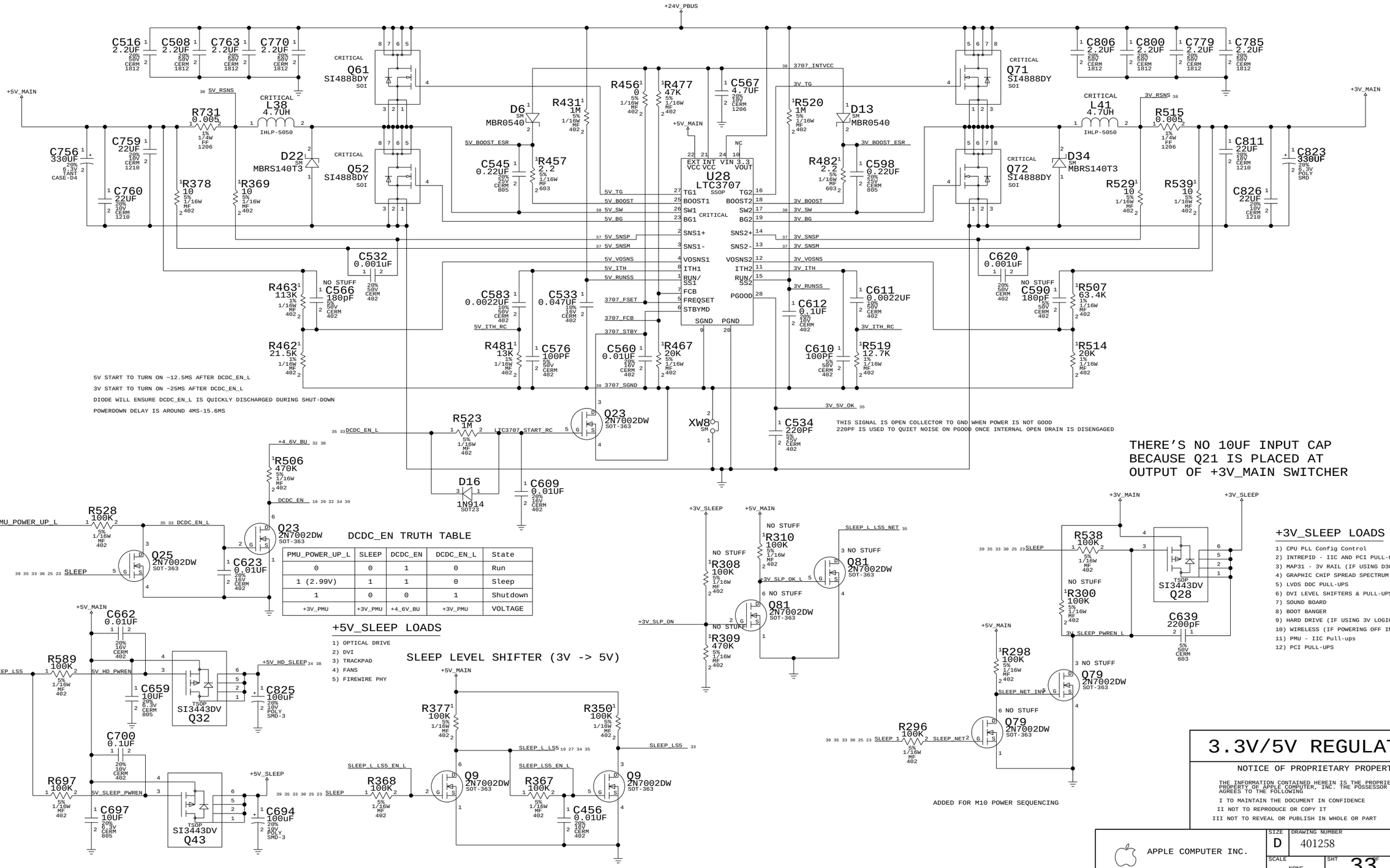
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401258	AA

SCALE: NONE

SHT 32 OF 44

3.3V/5V MAIN SUPPLY



5V START TO TURN ON ~12.5MS AFTER DCDC_EN_L
3V START TO TURN ON ~25MS AFTER DCDC_EN_L
DIODE WILL ENSURE DCDC_EN_L IS QUICKLY DISCHARGED DURING SHUT-DOWN
POWERDOWN DELAY IS AROUND 4MS-15.6MS

THIS SIGNAL IS OPEN COLLECTOR TO GND WHEN POWER IS NOT GOOD
220PF IS USED TO QUIET NOISE ON PGOOD ONCE INTERNAL OPEN DRAIN IS DISENGAGED

THERE'S NO 10UF INPUT CAP
BECAUSE Q21 IS PLACED AT
OUTPUT OF +3V_MAIN SWITCHER

DCDC_EN TRUTH TABLE

PMU_POWER_UP_L	SLEEP	DCDC_EN	DCDC_EN_L	State
0	0	1	0	Run
1 (2.99V)	1	1	0	Sleep
1	0	0	1	Shutdown
+3V_PMU	+3V_PMU	+4_6V_BU	+3V_PMU	VOLTAGE

+5V_SLEEP LOADS

1) OPTICAL DRIVE
2) DVI
3) TRACKPAD
4) FANS
5) FIREWIRE PHY

SLEEP LEVEL SHIFTER (3V -> 5V)

+3V_SLEEP LOADS

1) CPU PLL Config Control
2) INTREPID - IIC AND PCI PULL-UPS
3) MAP31 - 3V RAIL (IF USING D3COLD)
4) GRAPHIC CHIP SPREAD SPECTRUM CHIP
5) LVDS DDC PULL-UPS
6) DVI LEVEL SHIFTERS & PULL-UPS & HPD
7) SOUND BOARD
8) BOOT BANGER
9) HARD DRIVE (IF USING 3V LOGIC)
10) WIRELESS (IF POWERING OFF IN SLEEP)
11) PMU - IIC Pull-ups
12) PCI PULL-UPS

ADDED FOR M10 POWER SEQUENCING

3.3V/5V REGULATOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401258	AA
SCALE: NONE	SHT 33 OF 44	

VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage
(approx. 7ms delay)

1.175V -> 1.025V 1.30V -> 1.10V

SEL = 0; Y1=A1
SEL = 1; Y1=B1

Keep trace fat (40-100 mils) and short!!

Keep trace fat and short!!

Keep trace fat and short!!

Connect MAX1717 GND pin 13
to GND at bottom-side FET

OUTPUT VOLTAGE

V_{DAC} D4=0	V_{DAC} D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

MAX1717 VID CAN TAKE 3.3V TO 5.5V INPUTS

FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	A/B_ = Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1

If all pull-ups are >=100K and all
pull-downs are <=1K, $V_A = V_B$.

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V, HENCE VOFFSET = 2.0V * (R1/(R1+R2)) AND VCORE = VDAC + VOFFSET.

NOTE: R310 (R2) NO STUFFED FOR NO OFFSET CASE

ROUTE AS DIFFERENTIAL PAIR

PLACE THIS SHORT AT
PIN OF 1000uF CAP
CLOSEST TO CPU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S4023	1	RESISTOR	R321	?	1_30_VCORE
114S6343	1	RESISTOR	R321	?	1_32_VCORE

FMAX CONNECTOR

J5
M-ST-SM-52465-1217

NC (RFU)

VCORE SUPPLY

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SCALE: NONE	SHT 34 OF 44	

1.5V/2.5V SWITCHER

+1_5V_SLEEP LOADS

1) AGP I/O - IF USING D3COLD
2) MAXBUS I/O - IF 1.5V INTERFACE

+1_5V_MAIN LOADS

1) INTREPID CORE
2) AGP I/O IF USING D3HOT

+2_5V_MAIN LOADS

1) MAP31 - FBCORE/FBIO IF USING D3HOT
2) GIGABIT ETHERNET - AVDDL
3) DDR SODIMMS - CORE/IO
4) DDR MUXES
5) CLOCK SLEWING I/O
6) PCI1510 CORE

+2_5V_SLEEP LOADS

1) FBCORE/FBIO IF USING D3COLD
2) INTREPID MEMORY I/O

THERE'S 100K PULL-UP ON PG 31 ALREADY

DIODE PROVIDE PROVIDE QUICK SHUT-DOWN
POWER DOWN DELAY 1.5MS TO 3.5MS

CHANGE R424 BACK TO 10K, 1%, AND STUFF 5.11K FOR 1.5V OPERATION
CONNECTING 1_5V_FB TO GND, FORCES 1.8V OUTPUT

1.8V SWITCHER

+1_8V_MAIN LOADS

1) INTREPID PLLS

+1_8V_SLEEP LOADS

1) MPC7450 - MAXBUS I/O - IF 1.8V INTERFACE
2) CPU JTAG & MaxBus Pull-ups
3) CPU PLL Config Straps
4) OPTIONAL VIDEO MEMORY (M10 PRO ONLY)

CONTINUOUS MODE

BURST MODE
NO STUFF

1.5V/1.8V/2.5V SUPPLIES

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SCALE: NONE	SHT 35 OF 44	

DIGITAL SIGNALS

GROUP	SIG_NAME		MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
MAXBUS	CPU_AACK_L				250.0000	10 MIL SPACING			5 8
	CPU_ADDR<0..31>		5		250			83 MHZ	5 8
	CPU_ARTRY_L				250.0000	10 MIL SPACING			5 8
	CPU_BG_L				250.0000	10 MIL SPACING			5 8
	CPU_BR_L				250.0000	10 MIL SPACING			5 8
	CPU_CI_L		5		250.0000				5 8
	CPU_DATA<0..31>		5		250			83 MHZ	6 8
	CPU_DATA<32..63>		5		250			83 MHZ	6 8
	CPU_DBG_L		5		250.0000	10 MIL SPACING			5 8
	CPU_DTI<0..2>		5		250				5 8
	CPU_DRDY_L_UF					10 MIL SPACING			
	CPU_DRDY_L				250.0000	10 MIL SPACING			5 8
	CPU_GBL_L		5		250.0000				5 8
	CPU_HIT_L				250.0000	10 MIL SPACING			5 8
	CPU_QACK_L		5		250.0000	10 MIL SPACING			5 8
	CPU_QREQ_L				250.0000	10 MIL SPACING			5 8
	CPU_TA_L				250.0000	10 MIL SPACING			5 8
	CPU_TBST_L		5		250.0000	10 MIL SPACING			5 8
	CPU_TEA_L				250.0000				5 8
	CPU_TS_L				250.0000	10 MIL SPACING			5 8
	CPU_TSIZ<0..2>		5		250				5 8
	CPU_TT<0..4>		5		250				5 8
	CPU_WT_L		5		250.0000				5 8
GROUP 0	MEM_DATA<7..0>		4		200			167 MHZ	9 10
	RAM_DATA_A<7..0>		4		200			167 MHZ	10 11
	RAM_DATA_B<7..0>		4		200			167 MHZ	10 11
	MEM_DQS<0>	TOTAL LENGTH CONTROLLED BY SPREADSHEET			200				9 10
	RAM_DQS_A<0>		4		200				10 11
	RAM_DQS_B<0>		4		200				10 11
	MEM_DQM<0>		4		200				9 10
	RAM_DQM_A<0>		4		200				10 11
	RAM_DQM_B<0>		4		200				10 11
GROUP 1	MEM_DATA<15..8>		4		200			167 MHZ	9 10
	RAM_DATA_A<15..8>		4		200			167 MHZ	10 11
	RAM_DATA_B<15..8>		4		200			167 MHZ	10 11
	MEM_DQS<1>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200				9 10
	RAM_DQS_A<1>		4		200				10 11
	RAM_DQS_B<1>		4		200				10 11
	MEM_DQM<1>				200				9 10
	RAM_DQM_A<1>		4		200				10 11
	RAM_DQM_B<1>		4		200				10 11
GROUP 2/3	MEM_DATA<31..16>		4		200			167 MHZ	9 10
	RAM_DATA_A<31..16>		4		200			167 MHZ	10 11
	RAM_DATA_B<31..16>		4		200			167 MHZ	10 11
	MEM_DQS<3..2>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200			167 MHZ	9 10
DDR RAM	RAM_DQS_A<3..2>		4		200			167 MHZ	10 11
	RAM_DQS_B<3..2>		4		200			167 MHZ	10 11
	MEM_DQM<3..2>		4		200			167 MHZ	9 10
	RAM_DQM_A<3..2>		4		200			167 MHZ	10 11
	RAM_DQM_B<3..2>		4		200			167 MHZ	10 11
GROUP 4/5	MEM_DATA<47..32>		4		200			167 MHZ	9 10
	RAM_DATA_A<47..32>		4		200			167 MHZ	10 11
	RAM_DATA_B<47..32>		4		200			167 MHZ	10 11
	MEM_DQS<5..4>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200			167 MHZ	9 10
	RAM_DQS_A<5..4>		4		200			167 MHZ	10 11
	RAM_DQS_B<5..4>		4		200			167 MHZ	10 11
	MEM_DQM<5..4>		4		200			167 MHZ	9 10
	RAM_DQM_A<5..4>		4		200			167 MHZ	10 11
	RAM_DQM_B<5..4>		4		200			167 MHZ	10 11
GROUP 6	MEM_DATA<55..48>		4		200			167 MHZ	9 10
	RAM_DATA_A<55..48>		4		200			167 MHZ	10 11
	RAM_DATA_B<55..48>		4		200			167 MHZ	10 11
	MEM_DQS<6>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200				9 10
	RAM_DQS_A<6>				200				10 11
	RAM_DQS_B<6>		4		200				10 11
	MEM_DQM<6>				200				9 10
	RAM_DQM_A<6>		4		200				10 11
	RAM_DQM_B<6>		4		200				10 11
GROUP 7	MEM_DATA<63..56>		4		200			167 MHZ	9 10
	RAM_DATA_A<63..56>		4		200			167 MHZ	10 11
	RAM_DATA_B<63..56>		4		200			167 MHZ	10 11
	MEM_DQS<7>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200				9 10
	RAM_DQS_A<7>				200				10 11
	RAM_DQS_B<7>				200				10 11
	MEM_DQM<7>		4		200				9 10
	RAM_DQM_A<7>		4		200				10 11
	RAM_DQM_B<7>		4		200				10 11
ADDR	MEM_ADDR<12..0>		4					83 MHZ	9
	RAM_ADDR<12..0>		6		200				9 11
CONTROL	MEM_BA<1..0>		4						9
	RAM_BA<1..0>		6		200				9 11
	MEM_CS_L<3..0>		4						9
	RAM_CS_L<3..0>		6		200				9 11
	MEM_CKE<3..0>		4						9
	RAM_CKE<3..0>		6		200				9 11
	MEM_RAS_L		4						9
	RAM_RAS_L				200.0000				9 11
	MEM_CAS_L		4						9
	RAM_CAS_L				200.0000				9 11
	MEM_WE_L		4						9
	RAM_WE_L				200.0000				9 11
	MEM_MUXSEL_H<1..0>		3						9 10
	MEM_MUXSEL_L<1..0>		3						9 10
	RAM_MUXSEL_H		5						10
	RAM_MUXSEL_L		5						10

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME			MAX VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM	
INTREPID CLOCKS	SYSCLK_CPU_UF						10 MIL SPACING		8
	SYSCLK_CPU			4		200.0000	10 MIL SPACING		5 8
	INT_CPUFB_OUT			3			10 MIL SPACING		8
	INT_CPUFB_OUT_SHORT			3			10 MIL SPACING		8
	INT_CPUFB_OUT_NORM			3			10 MIL SPACING		8
	INT_CPUFB_IN_NORM			3			10 MIL SPACING		8
	INT_CPUFB_LONG			3			10 MIL SPACING		8
	INT_CPUFB_IN					200.0000	10 MIL SPACING		8
	SYSCLK_DDRCLK_A0_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A0_L_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A1_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A1_L_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B0_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B0_L_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B1_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B1_L_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A0	DDRCLK_A0		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_A0_L	DDRCLK_A0				200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_A1	DDRCLK_A1		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_A1_L	DDRCLK_A1				200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B0	DDRCLK_B0		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B0_L	DDRCLK_B0		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B1	DDRCLK_B1		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B1_L	DDRCLK_B1		3		200.0000	10 MIL SPACING		9 11
	INT_REF_CLK_OUT			3		200.0000	10 MIL SPACING		14
	INT_REF_CLK_IN					200.0000	10 MIL SPACING		14
	CLK66M_GPU_AGP_UF					200.0000	10 MIL SPACING		12
	CLK66M_GPU_AGP			4		200.0000	10 MIL SPACING		12 18
	INT_AGP_FB_OUT					200.0000	10 MIL SPACING		12
	INT_AGP_FB_IN			4		200.0000	10 MIL SPACING		12
	CLK33M_CBUS_UF					200.0000	10 MIL SPACING		12
	CLK33M_CBUS		SHOULD BE AT MOST 4 VIAS FOR CLK	6		200.0000	10 MIL SPACING		12 17
	CLK33M_AIRPORT_UF					200.0000	10 MIL SPACING		12
	CLK33M_AIRPORT		SHOULD BE AT MOST 4 VIAS FOR CLK	6		200.0000	10 MIL SPACING		12 24 39
	CLK33M_USB2_UF					200.0000	10 MIL SPACING		12
	CLK33M_USB2		SHOULD BE AT MOST 4 VIAS FOR CLK	6		200.0000	10 MIL SPACING		12 26
	INT_PCI_FB_OUT					200.0000	10 MIL SPACING		12
	INT_PCI_FB_IN			3		200.0000	10 MIL SPACING		12
MAP31	GPU_CLK27M_OUT						10 MIL SPACING		
	GPU_CLK27M_UF						10 MIL SPACING		
	GPU_SSCLK_UF						10 MIL SPACING		
	GPU_SSCLK_IN						10 MIL SPACING		
	GPU_FBCLK0						10 MIL SPACING		
	GPU_FBCLK0_L						10 MIL SPACING		
	GPU_FBCLK1						10 MIL SPACING		
	GPU_FBCLK1_L						10 MIL SPACING		
	GPU_DVO_CLKP						10 MIL SPACING		19 20
CRYSTALS	CLK27M_GPU_XOUT						10 MIL SPACING		
	CLK27M_XTAL_IN						10 MIL SPACING		
	CLK27M_GPU_XIN						10 MIL SPACING		
	CLK18M_INT_XIN						10 MIL SPACING		14
	CLK18M_INT_XOUT						10 MIL SPACING		14
	CLK18M_XTAL_IN						10 MIL SPACING		14
	CLK18M_INT_EXT						10 MIL SPACING		14
	CLK25M_ENET_XIN						10 MIL SPACING		27
	CLK25M_ENET_XOUT						10 MIL SPACING		27
	NEC_XT1						10 MIL SPACING		26
	NEC_XT2		THERE'S ANOTHER 280MIL LEG				10 MIL SPACING		26
SOUND	SND_SCLK			7		200.0000	10 MIL SPACING		14 25 39
	SND_CLKOUT					200.0000	10 MIL SPACING		14 25 39
ETHERNET MARVELL	CLKENET_PHY_RX					200.0000			27
	CLKENET_LINK_RX			3		200.0000	10 MIL SPACING		13 27
	CLKENET_PHY_GBE_REF					200.0000			27
	CLKENET_LINK_GBE_REF			3		200.0000	10 MIL SPACING		13 27
	CLKENET_PHY_TX					200.0000			27
	CLKENET_LINK_TX			5		200.0000	10 MIL SPACING		13 27
	CLKENET_LINK_GTX					200.0000			13
	CLKENET_PHY_GTX			3		200.0000	10 MIL SPACING		13 27
FIREWIRE	CLKFW_PHY_PCLK					200.0000			28
	CLKFW_LINK_PCLK			3		200.0000	10 MIL SPACING		13 28
	CLKFW_PHY_LCLK			3		200.0000	10 MIL SPACING		13 28
	CLKFW_LINK_LCLK					200.0000			13
	FW_XI					200.0000	10 MIL SPACING		28
	FW_OSC					200.0000	10 MIL SPACING		28

SIGNAL CONSTRAINTS - PAGE 1

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401258	AA

SCALE: NONE

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Digital Signals (cont'd)

GROUP	SIG_NAME	DELAY_RULE	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
AGP	AGP_AD<15..0>		5	100				66 MHz	12 18
AGP BYTES 0-1	AGP_CBE<1..0>		5	100				66 MHz	12 18
	AGP_AD_STB<0>		4	100		8 MIL SPACING			12 18
	AGP_AD_STB_L<0>		4	100		8 MIL SPACING			12 18
AGP BYTES 2-3	AGP_AD<31..16>		5	100				66 MHz	12 18
	AGP_CBE<3..2>		5	100				66 MHz	12 18
	AGP_AD_STB<1>		4	100		8 MIL SPACING			12 18
	AGP_AD_STB_L<1>			100		8 MIL SPACING			12 18
AGP SIDEBAND	AGP_SBA<7..0>		5	100				66 MHz	12 18
	AGP_SB_STB			100.0000		8 MIL SPACING			12 18
	AGP_SB_STB_L		4	100.0000		8 MIL SPACING			12 18
AGP CONTROL	AGP_FRAME_L			250.0000					12 18
	AGP_IRDY_L			250.0000					12 18
	AGP_TRDY_L		6	250.0000					12 18
	AGP_DEVSEL_L			250.0000					12 18
	AGP_STOP_L		6	250.0000					12 18
	AGP_PAR		6	250.0000					12 18
	AGP_REQ_L			285.0000					12 18
	AGP_GNT_L			250.0000					12 18
	AGP_RBF_L			250.0000					12 18
DVO	GPU_DVOD<0..11>		5	250					19 20
	GPU_DVO_HSYNC								19 20
	GPU_DVO_VSYNC								19 20
PCI	PCI_AD<31..0>					MIN_DAISY_CHAIN		33 MHz	9 12 17 24 26 39
	PCI_CBE<3..0>					MIN_DAISY_CHAIN		33 MHz	12 17 24 26 39
	PCI_FRAME_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_IRDY_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_TRDY_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_DEVSEL_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_STOP_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_PAR					MIN_DAISY_CHAIN			12 17 24 26 39
ULTRA ATA-100	UIDE_DATA<15..8>			NEED TO MATCH DELAY TO 250	200			100 MHZ	13 24
	UIDE_DATA<7>				200				13 24
	UIDE_DATA<6..0>				200			100 MHZ	13 24
	UIDE_ADDR<2..0>				200			100 MHZ	13 24
	UIDE_RST_L				200.0000				13 24
	UIDE_DIOW_L				200.0000				13 24
	UIDE_DIOR_L			10 MIL SPACING	200.0000				13 24
	UIDE_DMACK_L				200.0000				13 24
	UIDE_CS0_L				200.0000				13 24
	UIDE_CS1_L				200.0000				13 24
	UIDE_DMARQ				200.0000				13
	UIDE_IOCHRDY			10 MIL SPACING	200.0000				13 24
	UIDE_INTRQ				200.0000				13
	HD_DATA<15..0>		5	TOTAL UIDE+HD SKEW <500MIL	200			100 MHZ	24
	HD_ADDR<2..0>		5		200			100 MHZ	24
	HD_RESET_L		5		200.0000				24
	HD_DIOW_L		5		200.0000				24
	HD_DIOR_L		5	10 MIL SPACING	200.0000				24
	HD_DMACK_L		5		200.0000				24
	HD_CS0_L		5		200.0000				24
	HD_CS1_L		5		200.0000				24
	HD_DMARQ				200.0000				13 24
	HD_IOCHRDY		5	10 MIL SPACING	200.0000				24
	HD_INTRQ		5						13 24
EIDE INTREPID	EIDE_DATA<15..0>							33 MHZ	13 24
	EIDE_ADDR<2..0>							33 MHZ	13 24
	EIDE_CS0_L								13 24
	EIDE_CS1_L								13 24
	EIDE_RD_L								13 24
	EIDE_WR_L								13 24
	EIDE_IOCHRDY								13 24
	EIDE_INT								13 24
	EIDE_RST_L								13 24
	EIDE_DMACK_L								13 24
	EIDE_DMARQ								13 24
OPTICAL	EIDE_OPTICAL_DATA<15..0>							33 MHZ	24 39
	EIDE_OPTICAL_ADDR<2..0>							33 MHZ	24 39
	EIDE_OPTICAL_CS0_L								24 39
	EIDE_OPTICAL_CS1_L								24 39
	EIDE_OPTICAL_RD_L								24 39
	EIDE_OPTICAL_WR_L								24 39
	EIDE_OPTICAL_IOCHRDY								24 39
	EIDE_OPTICAL_INT								24 39
	EIDE_OPTICAL_RST_L								24 39
	EIDE_OPTICAL_DMAACK_L								24 39
	EIDE_OPTICAL_DMA_RQ								24 39
ETHERNET MII	ENET_LINK_RXD<7..0>		5						13 27
	ENET_RX_DV								13 27
	ENET_RX_ER								13 27
	ENET_PHY_TXD<7..0>		5						13 27
	ENET_LINK_TXD<7..0>								13
	ENET_PHY_TX_ER		5						13 27
	ENET_LINK_TX_ER								13
	ENET_PHY_TX_EN		5						13 27
	ENET_LINK_TX_EN								13
	ENET_MDIO								13 27
	ENET_MDC								13 27
	ENET_COL								13 27
	ENET_CRS								13 27
FIREWIRE MII	FW_LINK_DATA<7..0>		5						13 28
	FW_PHY_DATA<7..0>		5						28
	FW_LINK_CNTL<1..0>								13 28
	FW_PHY_CNTL<1..0>								28
	FW_LINK_LREQ								13
	FW_PHY_LREQ								13 28
	FW_PINT								13 28

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR	MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS	
ETHERNET	MDI_M<0>	ENET_MDI0				27
	MDI_P<0>	ENET_MDI0				27
	MDI_M<1>	ENET_MDI1	SPACING DELETED BECAUSE			27
	MDI_P<1>	ENET_MDI1	OF PHYSICAL CONSTRAINTS			27
	MDI_M<2>	ENET_MDI2	AROUND MARVELL PHY			27
	MDI_P<2>	ENET_MDI2				27
	MDI_M<3>	ENET_MDI3				27
	MDI_P<3>	ENET_MDI3				27
	RJ45_DN<0>	RJ45_DP0		10 MIL SPACING		27 39
	RJ45_DP<0>	RJ45_DP0		10 MIL SPACING		27 39
	RJ45_DN<1>	RJ45_DP1		10 MIL SPACING		27 39
	RJ45_DP<1>	RJ45_DP1		10 MIL SPACING		27 39
	RJ45_DN<2>	RJ45_DP2		10 MIL SPACING		27 39
	RJ45_DP<2>	RJ45_DP2		10 MIL SPACING		27 39
	RJ45_DN<3>	RJ45_DP3		10 MIL SPACING		27 39
	RJ45_DP<3>	RJ45_DP3		10 MIL SPACING		27 39
FIREWIRE	FW_TPA0N	FW_TPA0		MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPA0P	FW_TPA0		MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB0N	FW_TPB0		MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB0P	FW_TPB0		MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPI0N	FW_TPI0		MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPI0P	FW_TPI0		MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPO0N	FW_TPO0		MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPO0P	FW_TPO0		MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPA1N	FW_TPA1	500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPA1P	FW_TPA1	500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB1N	FW_TPB1	500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB1P	FW_TPB1	500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPI1N	FW_TPI1		MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 39
	FW_TPI1P	FW_TPI1		MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 39
	FW_TPO1N	FW_TPO1		MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 39
	FW_TPO1P	FW_TPO1		MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 39
LVDS LOWER	CLKLVDS_LN	CLKLVDS_L		10 MIL SPACING	4	19 22 39
	CLKLVDS_LP	CLKLVDS_L		10 MIL SPACING	4	19 22 39
	LVDS_L0N	LVDS_L0		10 MIL SPACING		19 22 39
	LVDS_L0P	LVDS_L0		10 MIL SPACING		19 22 39
	LVDS_L1N	LVDS_L1		10 MIL SPACING		19 22 39
	LVDS_L1P	LVDS_L1		10 MIL SPACING		19 22 39
	LVDS_L2N	LVDS_L2		10 MIL SPACING		19 22 39
	LVDS_L2P	LVDS_L2		10 MIL SPACING		19 22 39
UPPER	CLKLVDS_UN	CLKLVDS_U		10 MIL SPACING	4	19 22 39
	CLKLVDS_UP	CLKLVDS_U		10 MIL SPACING	4	19 22 39
	LVDS_U0N	LVDS_U0		10 MIL SPACING		19 22 39
	LVDS_U0P	LVDS_U0		10 MIL SPACING		19 22 39
	LVDS_U1N	LVDS_U1		10 MIL SPACING		19 22 39
	LVDS_U1P	LVDS_U1		10 MIL SPACING		19 22 39
	LVDS_U2N	LVDS_U2		10 MIL SPACING		19 22 39
	LVDS_U2P	LVDS_U2		10 MIL SPACING		19 22 39
TMDS	TMDS_CONN_CLKN	CLKCONN_TMDS		10 MIL SPACING	4	22 39
	TMDS_CONN_CLKP	CLKCONN_TMDS		10 MIL SPACING	4	22 39
	TMDS_CLKN	CLKTMDS		10 MIL SPACING	4	20 22
	TMDS_CLKP	CLKTMDS		10 MIL SPACING	4	20 22
	TMDS_DN<0>	TMDS_D0		10 MIL SPACING		20 22 39
	TMDS_DP<0>	TMDS_D0		10 MIL SPACING		20 22 39
	TMDS_DN<1>	TMDS_D1		10 MIL SPACING		20 22 39
	TMDS_DP<1>	TMDS_D1		10 MIL SPACING		20 22 39
	TMDS_DN<2>	TMDS_D2		10 MIL SPACING		20 22 39
	TMDS_DP<2>	TMDS_D2		10 MIL SPACING		20 22 39
USB	NEC_USB_DAM	NEC_USB_DA	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_DAP	NEC_USB_DA	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	USB_DEM	USB_DE		5 MIL SPACING		14
	USB_DEP	USB_DE		5 MIL SPACING		14
	NEC_USB_DBM	NEC_USB_DB	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_DBP	NEC_USB_DB	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	USB_DFM	USB_DF		5 MIL SPACING		14
	USB_DFP	USB_DF		5 MIL SPACING		14
	BT_USB_DM	BT_USB_D		5 MIL SPACING		14 24 39
	BT_USB_DP	BT_USB_D		5 MIL SPACING		14 24 39
	NEC_USB_RSDM1	NEC_USB_RSD1	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_RSDP1	NEC_USB_RSD1	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_RSDM2	NEC_USB_RSD2	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_RSDP2	NEC_USB_RSD2	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	MODEM_USB_DM	MODEM_USB_D		5 MIL SPACING		14 25 39
	MODEM_USB_DP	MODEM_USB_D		5 MIL SPACING		14 25 39
	LEFT_USB_DM	LEFT_USB	MIN_LINE_WIDTH=5	10 MIL SPACING		24 26 39
	LEFT_USB_DP	LEFT_USB	MIN_LINE_WIDTH=5	10 MIL SPACING		24 26 39
	RIGHT_USB_DM	RIGHT_USB	MIN_LINE_WIDTH=5	10 MIL SPACING		26 32 39
	RIGHT_USB_DP	RIGHT_USB	MIN_LINE_WIDTH=5	10 MIL SPACING		26 32 39
POWER SUPPLIES	1772_CSSN	1772_CSS				31
	1772_CSSP	1772_CSS				31
	1772_CSIN	1772_CSI				31
	1772_CSIP	1772_CSI				31
	3V_SNSM	3V_SNS				33
	3V_SNSP	3V_SNS				33
	5V_SNSM	5V_SNS				33
	5V_SNSP	5V_SNS				33
THERMOSTAT	THERM1_DM	THERM1				25
	THERM1_DP	THERM1				25
	THERM2_DM	THERM2				25
	THERM2_DP	THERM2				25
	THERM1_M_DM	THERM1_MAIN				
	THERM1_M_DP	THERM1_MAIN				
	THERM2_M_DM	THERM2_MAIN				
	THERM2_M_DP	THERM2_MAIN				
	THERM1_A_DM	THERM1_ALT				25
	THERM1_A_DP	THERM1_ALT				25
	THERM2_A_DM	THERM2_ALT				25
	THERM2_A_DP	THERM2_ALT				25

INTERNAL LAYER
ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.57OHM
ZDIFF = 99.8OHM

FOR FIREWIRE
ER = 4.3 (DIELECTRIC CONSTANT)
W = 3.4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 53.37OHM
ZDIFF = 107.17OHM

INTERNAL LAYER (USB1.1/USB 2.0)
ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL(USB 1.1)/ 5MIL(USB 2.0) (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 5MIL (USB 1.1) (SEPERATION OF DIFF TRACES)
S = 10MIL (USB 2.0) (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.5OHM (USB 1.1)/ 46.2OHM (USB 2.0)
ZDIFF = 89.3OHM (USB 1.1)/ 89.4OHM (USB 2.0)

SIGNAL CONSTRAINTS - PAGE 2

APPLE COMPUTER INC.
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SCALE NONE | SHT 37 OF 44

POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
MAIN/SLEEP	+24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+BATT	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	
	+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+2_5V_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	39
	+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	35
	+1_5V_SLEEP_VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	35
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31 32
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31 39
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31 39
	1772_DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	1772_LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	31
	1772_LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		31
	1772_DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		31
	1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10		31
PMU	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	+4_85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		30 32
	+4_6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10		32 33
	+4_85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		32
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		32
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		25 30
MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24 33
	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24
TRACKPAD	+5V_TPAD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=10		23 39
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		23 39
VIDEO	+12_8V_INV	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	22
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
KB LED	KBD_LED1_OUT	VOLTAGE=0V	MIN_LINE_WIDTH=10		23 39
	KBD_LED2_OUT	VOLTAGE=0V	MIN_LINE_WIDTH=10		23 39
FAN GND	FANL_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 39
	FANR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 39
SOUND	+5V_SOUND_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	SND_AGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=15	25

	GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	
I/O AREA	CHGND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND1
INVERTER	CHGND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND2
TRACKPAD	CHGND3	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND3
LVDS	CHGND4	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND4 39
I/O AREA	CHGND5	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND5
I/O AREA	CHGND6	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND6
	ENET_CTAP_CHGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	27

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 34 39
	CPU_AVDD	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
DDR RAM INTREPID PLLS	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 7 8 15 16 23 34
	DDR_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		11
	+2_5V_INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	9 10 15 16
	+3V_INTREPID_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14
	+1_5V_INTREPID_PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	8 12 14
	+1_5V_INTREPID_PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5	14
	+1_5V_INTREPID_PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5	12
	+1_5V_INTREPID_PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	8
	+1_5V_INTREPID_PLL8	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
REFERENCE	INT_MEM_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		9
	INT_AGP_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		12 18
	INT_MEM_REF_H	VOLTAGE=0V	MIN_LINE_WIDTH=10		9
	UIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8		13
CARDBUS	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
ATI M10	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	18 19 39
	+GPU_MEM	VOLTAGE=2.5V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	18 21
	+3V_GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 18 19 21
	+3V_GPU_FLT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	21
	+1_5V_AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 15 16 18 19 21
	GPU_MEM_IO	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	GPU_MEM_IO_FLT	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+GPU_MEMCORE	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+1_8V_GPU	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18 19 20 21
	+2_5V_GPU_PNLIO	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_8V_ATI_PVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19 21
	+1_5V_AGP_GPU	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_5V_GPU_VDD15	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	+1_8V_GPU_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1331	+1_8V_GPU_VDDDI	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1332	GPU_VCORE_VDDCI	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	18
1333	+2_5V_GPU_A2VDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1334	+1_8V_GPU_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1335	+1_8V_GPU_PNLPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1336	+1_8V_GPU_PNLIO	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1337	+GPU_MCLK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1338	+1_8V_GPU_AVDDQ	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1341	+1_8V_GPU_MEMPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1340	+3V_ATI_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	18
1339	+3V_ATI_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	18
1342	+GPU_VDD15_UF	VOLTAGE=1.5V	MIN_LINE_WIDTH=20		19
1343	+2_5V_SLEEP_NECK1	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		19
1347	+3V_SLEEP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		21
1345	+1_5V_AGP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		19
1346	+1_8V_PVDD_NECK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10		19
1344	GPU_VCORE_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		19
1348	+GPU_VDD15_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		19
1350	+2_5V_SLEEP_NECK2	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		21
1349	+1_8V_SLEEP_NECK	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		21
1351	+1_5V_SLEEP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		21
1352	+2_5V_GPU	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
SILICON IMIAGE	+3V_SI_PLLVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	20
	+3V_SI_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	20
	+3V_SI_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	20
88E1111	+2_5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+2_5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
	+1_0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
	LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
	LM2594_IN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
FW	+3V_FW_ESD_ILIM	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+3V_FW_ESD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+FW_FUSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_PWR_OR	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28 29
	+FW_VP0	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_PWR_PORTA	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_VP1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+3V_FW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28 29
	+3V_FW_UF	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	28
	+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
USB 2.0	FW_TPO0R	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29 39
INTREPID SSCG	NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+3V_CG_PLL_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	14
	+2_5V_CG_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	14

MIN_NECK_WIDTH REDUCED FOR TESTPOINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	1625_VSW	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		32
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		32
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		32
	1V20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	31 32
LTC3707 5V SWITCHER	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	33
	5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
3V SWITCHER	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		33
MAX1715 2.5V SWITCHER	2_5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	35
	2_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	2_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	2_5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	2_5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
1.5V SWITCHER	1_5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8		35
	1_5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	35
	1_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	1_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	1_5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	1_5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
CONTROL	1_5V_ILIM		MIN_LINE_WIDTH=8		35
	2_5V_ILIM		MIN_LINE_WIDTH=8		35
	MAX1715_TON		MIN_LINE_WIDTH=8		35
	MAX1715_SKIP		MIN_LINE_WIDTH=8		35
	MAX1715_REF	VOLTAGE=2.0V	MIN_LINE_WIDTH=8		35
	MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	35
MAX1717	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=200	MIN_NECK_WIDTH=10	34
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	VCORE_ILIM		MIN_LINE_WIDTH=8		34
	VCORE_REF		MIN_LINE_WIDTH=8		34
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8		34
	VCORE_CC		MIN_LINE_WIDTH=8		34
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		34 39
	VCORE_TIME		MIN_LINE_WIDTH=8		34
	VCORE_VGATE		MIN_LINE_WIDTH=8		14 34
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30		34
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8		34
	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		34
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8		34
LTC1778	1778_VIN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	19
	1778_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	1778_BST_RC	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	1778_TG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_BG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	GPU_VCORE_SW	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	19
	1778_ION		MIN_LINE_WIDTH=8		19
	1778_ITH		MIN_LINE_WIDTH=8		19
	1778_ITH_RC		MIN_LINE_WIDTH=8		19
	1_5V_2_5V_OK		MIN_LINE_WIDTH=8		35
	1778_VFB		MIN_LINE_WIDTH=8		19 39
	1778_FCB		MIN_LINE_WIDTH=8		19
	1778_VRNG		MIN_LINE_WIDTH=8		19
LTC3411	LTC3411_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC3411_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	
	1_8V_SW	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	35
	1_8V_VFB		MIN_LINE_WIDTH=8		
	LTC3411_ITH_RC		MIN_LINE_WIDTH=8		
	LTC3411_ITH		MIN_LINE_WIDTH=8		
	LTC3411_SYNC		MIN_LINE_WIDTH=8		
	LTC3411_SHDN		MIN_LINE_WIDTH=8		
LTC1962 INT PLLS	LTC1962_INT_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	14
	LTC1962_L3_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_L3_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_1V5_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_1V5_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	

SIGNAL CONSTRAINTS - PAGE 3

APPLE COMPUTER INC.

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D	401258	AA
SCALE: NONE	SHT 38 OF 44	

FUNCTIONAL TEST POINTS

FUNC_TEST=YES JTAG_ASIC_TMS 13 27
FUNC_TEST=YES JTAG_ASIC_TDI 13
FUNC_TEST=YES JTAG_ASIC_TDO_TP 27
FUNC_TEST=YES JTAG_ASIC_TCK 13 27
FUNC_TEST=YES JTAG_ASIC_TRST_L 13 27
FUNC_TEST=YES CPU_CHKSTP_OUT_L 5
FUNC_TEST=YES CPU_SRESET_L 5
FUNC_TEST=YES CPU_HRESET_L 5 7 23
FUNC_TEST=YES JTAG_CPU_TMS 5 23
FUNC_TEST=YES JTAG_CPU_TDI 5 23
FUNC_TEST=YES JTAG_CPU_TDO_TP 5
FUNC_TEST=YES JTAG_CPU_TCK 5 23
FUNC_TEST=YES JTAG_CPU_TRST_L 5 23 39

FUNC_TEST=YES INT_I2C_CLK0 11 13 23
FUNC_TEST=YES INT_I2C_DATA0 11 13 23
FUNC_TEST=YES INT_I2C_CLK1 13 14 25
FUNC_TEST=YES INT_I2C_DATA1 13 14 25
FUNC_TEST=YES CBUS_DET_1_L 17
FUNC_TEST=YES CBUS_DET_2_L 17
FUNC_TEST=YES TMDS_DN<0> 20 22 37
FUNC_TEST=YES TMDS_DP<0> 20 22 37
FUNC_TEST=YES TMDS_DN<1> 20 22 37
FUNC_TEST=YES TMDS_DP<1> 20 22 37
FUNC_TEST=YES TMDS_DN<2> 20 22 37
FUNC_TEST=YES TMDS_DP<2> 20 22 37
FUNC_TEST=YES TMDS_CONN_CLKN 22 37

FUNC_TEST=YES TMDS_CONN_CLKP 22 37
FUNC_TEST=YES VGA_R 22
FUNC_TEST=YES VGA_G 22
FUNC_TEST=YES VGA_B 22
FUNC_TEST=YES VGA_VSYNC 22
FUNC_TEST=YES VGA_HSYNC 22
FUNC_TEST=YES DVI_DDC_CLK_UF 22
FUNC_TEST=YES DVI_DDC_DATA_UF 22
FUNC_TEST=YES DVI_HPD_UF 22
FUNC_TEST=YES LVDS_L0N 19 22 37
FUNC_TEST=YES LVDS_L0P 19 22 37
FUNC_TEST=YES LVDS_L1N 19 22 37
FUNC_TEST=YES LVDS_L1P 19 22 37
FUNC_TEST=YES LVDS_L2N 19 22 37
FUNC_TEST=YES LVDS_L2P 19 22 37
FUNC_TEST=YES CLKLVDS_LN 19 22 37
FUNC_TEST=YES CLKLVDS_LP 19 22 37
FUNC_TEST=YES LVDS_U0N 19 22 37
FUNC_TEST=YES LVDS_U0P 19 22 37
FUNC_TEST=YES LVDS_U1N 19 22 37
FUNC_TEST=YES LVDS_U1P 19 22 37
FUNC_TEST=YES LVDS_U2N 19 22 37
FUNC_TEST=YES LVDS_U2P 19 22 37
FUNC_TEST=YES CLKLVDS_UN 19 22 37
FUNC_TEST=YES CLKLVDS_UP 19 22 37
FUNC_TEST=YES LVDS_DDC_CLK 19 22
FUNC_TEST=YES LVDS_DDC_DATA 19 22
FUNC_TEST=YES BRIGHT_PWM 22
FUNC_TEST=YES TV_GND1 22 38
FUNC_TEST=YES TV_GND2 22 38

FUNC_TEST=YES TV_C 22
FUNC_TEST=YES TV_Y 22
FUNC_TEST=YES TV_COMP 22
FUNC_TEST=YES SND_TO_AUDIO 14 25
FUNC_TEST=YES SND_SYNC 14 25
FUNC_TEST=YES SND_CLKOUT 14 25 36

FUNC_TEST=YES INT_AUDIO_TO_SND 14 25
FUNC_TEST=YES SND_SCLK 14 25 36
FUNC_TEST=YES SND_HW_RESET_L 14 25
FUNC_TEST=YES SND_HP_SENSE_L 14 25
FUNC_TEST=YES SND_LIN_SENSE_L 14 25
FUNC_TEST=YES INT_I2C_DATA2 14 25
FUNC_TEST=YES INT_I2C_CLK2 14 25
1294 FUNC_TEST=YES CHGND4 38
1294 FUNC_TEST=YES SLEEP_LED 23 25

FUNC_TEST=YES BT_USB_DM 14 24 37
FUNC_TEST=YES BT_USB_DP 14 24 37
FUNC_TEST=YES MODEM_USB_DM 14 25 37
FUNC_TEST=YES MODEM_USB_DP 14 25 37
FUNC_TEST=YES PCI_AD<0> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<1> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<2> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<3> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<4> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<5> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<6> 9 12 17 24 26 37

FUNC_TEST=YES PCI_AD<7> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<8> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<9> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<10> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<11> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<12> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<13> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<14> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<15> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<16> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<17> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<18> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<19> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<20> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<21> 12 17 24 26 37
FUNC_TEST=YES PCI_AD<22> 12 17 24 26 37
FUNC_TEST=YES PCI_AD<23> 12 17 24 26 37
FUNC_TEST=YES PCI_AD<24> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<25> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<26> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<27> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<28> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<29> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<30> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<31> 9 12 17 24 26 37
FUNC_TEST=YES PCI_FRAME_L 12 17 24 26 37
FUNC_TEST=YES PCI_TRDY_L 12 17 24 26 37
FUNC_TEST=YES PCI_IRDY_L 12 17 24 26 37
FUNC_TEST=YES PCI_DEVSEL_L 12 17 24 26 37
FUNC_TEST=YES PCI_STOP_L 12 17 24 26 37

FUNC_TEST=YES PCI_PAR 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<0> 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<1> 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<2> 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<3> 12 17 24 26 37
FUNC_TEST=YES AIRPORT_PCI_REQ_L 12 24
FUNC_TEST=YES AIRPORT_PCI_GNT_L 12 24
FUNC_TEST=YES AIRPORT_PCI_INT_L 14 24
FUNC_TEST=YES EIDE_OPTICAL_DATA<0> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<1> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<2> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<3> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<4> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<5> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<6> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<7> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<8> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<9> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<10> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<11> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<12> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<13> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<14> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<15> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DMA_RQ 24 37
FUNC_TEST=YES EIDE_OPTICAL_RD_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_DMAACK_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_ADDR<0> 24 37
FUNC_TEST=YES EIDE_OPTICAL_ADDR<1> 24 37
FUNC_TEST=YES EIDE_OPTICAL_ADDR<2> 24 37
1291 FUNC_TEST=YES SND_AMP_MUTE 25
1292 FUNC_TEST=YES SND_HP_MUTE_INV 25

FUNC_TEST=YES EIDE_OPTICAL_CS0_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_CS1_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_RST_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_WR_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_IOCHRDY 24 37
FUNC_TEST=YES EIDE_OPTICAL_INT 24 37
FUNC_TEST=YES TPAD_F_TXD 23
FUNC_TEST=YES TPAD_F_RXD 23
FUNC_TEST=YES LID_CLOSED_L 23
FUNC_TEST=YES COMM_RESET_L 14 25
FUNC_TEST=YES COMM_SHUTDOWN 14 25
FUNC_TEST=YES COMM_RING_DET_L 14 25 30
FUNC_TEST=YES KBD_ID 23 30
FUNC_TEST=YES +5V_TPAD_SLEEP 23 38
FUNC_TEST=YES +3V_HALL_EFFECT 23 38
FUNC_TEST=YES KBD_CAPSLOCK_LED 23
FUNC_TEST=YES KBD_FUNCTION_L 23 30
FUNC_TEST=YES KBD_CONTROL_L 23 30
FUNC_TEST=YES KBD_COMMAND_L 23 30
FUNC_TEST=YES KBD_OPTION_L 23 30
FUNC_TEST=YES KBD_SHIFT_L 23 30
FUNC_TEST=YES KBD_X<0> 23 30
FUNC_TEST=YES KBD_X<1> 23 30
FUNC_TEST=YES KBD_X<2> 23 30
FUNC_TEST=YES KBD_X<3> 23 30
FUNC_TEST=YES KBD_X<4> 23 30
FUNC_TEST=YES KBD_X<5> 23 30
FUNC_TEST=YES KBD_X<6> 23 30
FUNC_TEST=YES KBD_X<7> 23 30
FUNC_TEST=YES KBD_X<8> 23 30
1287 FUNC_TEST=YES SRCLK_TP 26
1288 FUNC_TEST=YES SRMOD_TP 26
1289 FUNC_TEST=YES TEB_TP 26
1290 FUNC_TEST=YES TEST_TP 26

FUNC_TEST=YES KBD_X<9> 23 30
FUNC_TEST=YES KBD_Y<0> 23 30
FUNC_TEST=YES KBD_Y<1> 23 30
FUNC_TEST=YES KBD_Y<2> 23 30
FUNC_TEST=YES KBD_Y<3> 23 30
FUNC_TEST=YES KBD_Y<4> 23 30
FUNC_TEST=YES KBD_Y<5> 23 30
FUNC_TEST=YES KBD_Y<6> 23 30
FUNC_TEST=YES KBD_Y<7> 23 30
FUNC_TEST=YES KBD_NUMLOCK_LED 23
FUNC_TEST=YES +BATT_POS 31 38
FUNC_TEST=YES BATT_CLK 31
FUNC_TEST=YES BATT_DATA 31
FUNC_TEST=YES BATT_NEG 31 38
FUNC_TEST=YES PMU_BATT_DET_L 30 31
FUNC_TEST=YES FANR_GND 25 38

FUNC_TEST=YES FANL_GND 25 38
FUNC_TEST=YES FANL_TACH 25
1277 FUNC_TEST=YES FANR_PWM 25
1272 FUNC_TEST=YES FANL_PWM 25
FUNC_TEST=YES RJ45_DP<0> 27 37
FUNC_TEST=YES RJ45_DN<0> 27 37
FUNC_TEST=YES RJ45_DP<1> 27 37
FUNC_TEST=YES RJ45_DN<1> 27 37
FUNC_TEST=YES RJ45_DP<2> 27 37
FUNC_TEST=YES RJ45_DN<2> 27 37
FUNC_TEST=YES RJ45_DP<3> 27 37
FUNC_TEST=YES RJ45_DN<3> 27 37
FUNC_TEST=YES FW_TPO0R 29 38
FUNC_TEST=YES VCORE_VID0 1281
FUNC_TEST=YES VCORE_VID1 1282
FUNC_TEST=YES VCORE_VID2 1283
FUNC_TEST=YES VCORE_VID3 1284
FUNC_TEST=YES VCORE_VID4 1285

FUNC_TEST=YES FW_TPO1P 29 37
FUNC_TEST=YES FW_TPO1N 29 37
FUNC_TEST=YES FW_TPI1P 29 37
FUNC_TEST=YES FW_TPI1N 29 37
FUNC_TEST=YES CHARGE_LED_L 30 31
FUNC_TEST=YES ADAPTER_DET 30 31
FUNC_TEST=YES SUTRO_ALS_GAIN_SW 23 24
FUNC_TEST=YES SUTRO_ALS_OUT 23 24
FUNC_TEST=YES KBD_LED1_OUT 23 38
FUNC_TEST=YES KBD_LED2_OUT 23 38
FUNC_TEST=YES COMM_TXD_L 14 25
FUNC_TEST=YES COMM_TRXC 14 25
FUNC_TEST=YES COMM_GPIO_L 14 25
FUNC_TEST=YES COMM_DTR_L 14 25
FUNC_TEST=YES COMM_RTS_L 14 25
FUNC_TEST=YES COMM_RXD 14 25
FUNC_TEST=YES PMU_KB_RESET_L 30
FUNC_TEST=YES PWR_BUTTON_L 23 25
FUNC_TEST=YES +PBUS 38
FUNC_TEST=YES +24V_PBUS 38
FUNC_TEST=YES GPU_VCORE 18 19 38
FUNC_TEST=YES CPU_VCORE_SLEEP 5 34 38
FUNC_TEST=YES VCORE_FB 34 38
FUNC_TEST=YES +1_8V_MAIN 38
FUNC_TEST=YES +3V_PMU 38
FUNC_TEST=YES +5V_DDC_SLEEP 22 38
FUNC_TEST=YES +12_8V_INV 22 38
1286 FUNC_TEST=YES VCORE_MUX_EN 34

FUNC_TEST=YES +5V_INV_SW 22 38
FUNC_TEST=YES LEFT_USB_DM 24 26 37
FUNC_TEST=YES LEFT_USB_DP 24 26 37
FUNC_TEST=YES RIGHT_USB_DM 26 32 37
FUNC_TEST=YES RIGHT_USB_DP 26 32 37
FUNC_TEST=YES NEC_LEFT_USB_PWREN 24 26
FUNC_TEST=YES NEC_LEFT_USB_OVERCURRENT 24 26
FUNC_TEST=YES NEC_RIGHT_USB_PWREN 26 32
FUNC_TEST=YES NEC_RIGHT_USB_OVERCURRENT 26 32
FUNC_TEST=YES DCDC_EN 19 29 32 33 34
FUNC_TEST=YES BBANG_HRESET_L 23

FUNC_TEST=YES MAIN_RESET_L 14 17 18 20 24 26 30
FUNC_TEST=YES RF_DISABLE_L_SPN 24
FUNC_TEST=YES AIRPORT_CLKRUN_L 24
FUNC_TEST=YES ROM_RW_L 9 12 24
FUNC_TEST=YES ROM_ONBOARD_CS_L 9 24
FUNC_TEST=YES ROM_CS_L 9 12 24
FUNC_TEST=YES CLK33M_AIRPORT 12 24 36
FUNC_TEST=YES AIRPORT_IDSEL 24
FUNC_TEST=YES ROM_OE_L 9 12 24
FUNC_TEST=YES INT_MOD_DTI 1273 14 25
FUNC_TEST=YES JTAG_CPU_TRST_L 1274 5 23 39
FUNC_TEST=YES MOD_BITCLK 1275 14 25
FUNC_TEST=YES MOD_CLKOUT 1276 14 25
FUNC_TEST=YES MOD_DTO 1277 14 25
FUNC_TEST=YES MOD_SYNC 1278 14 25
FUNC_TEST=YES SLEEP 1279 23 25 30 33 35
FUNC_TEST=YES 1778_VER 1280 19 38

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401258	AA

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REVISION HISTORY

REV 0.01 - 03/06/2003

3/3
1) Initial check-in of Enterprise schematic after conversion to Concept 14.2

3/10
2) added 8 new 10uF vcore caps
3) added jumpers at 1.5V, 1.8V, 2.5V, 3.3V, 5V, and PBUS supply outputs
4) added 8 more 0.1uF vcore byapass caps

3/11
5) removed dedicated boot banger circuit (U5400,U5200,RP46,U9,U1000)
6) updated firewire to phy to rev A prt number
7) changed cpu PLL config to 1083/833
8) changed reset to U56 (clock slewing chip) to MAIN_RESET_L
9) changed C550 to 138S0536 to limit AVL
10) changed Vcore stuffing options to 1.4V/1.025V using analog mux to support slewing
11) changed stuffing to set Vcore offset to 0mV by default
12) changed comments to eliminate references to L3 in power supply section

3/18
13) changed stuffing options for GPU PCI ID to 0x319
14) changed R164 (DAC1RSET) to 107 ohm pulldown
15) added 10K pulldown to U43 pin A21
16) changed fan controller to ADT7460

3/19
17) added pads for 0.1uF cap from +Adapter to digital gnd for EMC
18) added pads for 0 ohm between chassis and digital gnd near ENET connector for EMC
19) corrected path to correct for last checkin
20) removed BOM table for MAP31
21) REMOVED ALL RELATIVE_PROPAGATION_DELAY AND PROPAGATION_DELAY PROPERTIES TO PREPARE_FOR_CONSTRAINT_BACK_ANNOTATION
22) changed CHGND on R616 to CHGND1
23) ***BOARD RENUMBERED***

3/28
24) integrated M10 pages from Q16 schematic and renumbered them

4/10
25) updated physical constraints for M10 power nets
26) added DP7 for M10 power sequencing
27) added RP27,RP28,RP32, and RP57 for TMDS series termination
28) update PLL CFG high 0010 1.25GHz
low 1011 833MHz
29) update sscg/nosscg stuffing option on intrepid boot straps
30) removed D31 between +Batt and 24V_Pbus
31) add Vcore DAC resistors (R288,R289,R290,R292) for no mux case
32) change intrepid PLL LDO stuffing back to 1.8V main
33) change C640 and C646 to 0.01uF (Apple # 132S1047) for FW check config
34) change I2C pullups (R29 and R102) to 1K
35) changed bootrom part number to 341S1255

4/18
36) changed C756 to 128S0025 (Sanyo only 6.3V 330uF)
37) add pads for 90 ohm chokes to FWB path close to connector (route through the pads)
38) changed Vcore inductor (L36) to molded core part (152S0125)
39) changed Pbus inductor (L37) to molded core part (152S0126)
40) added seperate 1_8V_GPU_TPVDD filter and LDO (U54)

4/21
41) replace disctrete LCL with single chip LCL filters (155S0154) for VGA (L ,L , and L)
42) add 165 ohm chokes on TMDS data pairs at connector (L ,L , and L)
43) move BS1 to bottom side
44) move CPU thermal sensor (Q39) to input 1 on fan controller and power supply sensor (Q66) to input 2
45) added trace from Vcore to fan controller ADC input
46) added FET inverters (Q78) to PWM outputs of fan controller (U3) to prevent spinup at boot
47) added FET (Q79) for +3V_Sleep for M10 power sequencing

4/27
48) changed TMDS data chokes to 90 ohm (155S0128)
49) changed C762 and C766 to 4.7uF 1206 caps
50) changed TMDS data chokes to 90 ohms (155S0128)
51) changed C762 and C766 to 4.7uF 1206
52) changed Q51 to Si7860DP (376S0119)
53) changed Q48 to Si7892DP (376S0120)
54) changed D24 to B340LB (371S0132)
55) changed L30 to 2.2uH Tokin inductor (152S0139)
56) added Q58, R307, and C515 for GPU Vcore control inverter
57) changed R416 to 2.2ohms
58) changed R364 to 102K
59) added 0.1uF 50V C883 to RS- of Max4172 (NO stuff)
60) changed D18 to 1N914
61) changed L38 and L41 to 4.7uH (152S0137)
62) added Q81, R308, R309, and R310 for power sequencing (no stuff)
63) changed Q49 and Q50 to Si7860DP (376S0119)
64) changed L36 to 1.2uH 18.3A (152S0125)
65) added R331 1mohm sense resistor to CPU Vcore
66) added C885 and C884 , 1000uF CPU Vcore outpur caps
67) added Q82, R607, R455, R417, and C886 for 1.5V sleep sequencing
68) added Q83 and 100K R608 for 1.8V sequencing
69) added 15.4K R616 and 10K R672 for 2.5V switcher feedback divider
70) changed pinout of sound connector for sousaphone
71) removed Q44 (5V sound sleep fet)
72) changed Q31 to invert headphone Mute to sousaphone

4/28
73) changed CPU_VCORE_SLEEP location back to across bypass caps to correct after adding reference resistor
74) changed D5 to schottky diode (MBR0540)
75) fixed unnamed net (LTC3411_SHDN_SEQ)
76) changed drain/source polarity of Q76 (FET from +BATT to Pbus)

4/28
77) moved XW15 to connect to CPU_VCORE_SLEEP_UF (before positioning resistor)
78) changed Fan control nets to FanL and FanR from Fan1 and Fan2
79) SWAPPED CONNECTIONS SO THAT OUTPUT 1 FROM FAN CONTROLLER CONNECTS TO LEFT FAN (CPU) AND FAN 2 CONNECTS TO THE RIGHT FAN (GPU)
80) updated power constraints with new fan net names

4/28
81) change Q58 on pg19 to Q80 to consolidate parts
82) CHANGED U55 TO MM1571J FOR COST SAVINGS
83) changed L72,L73,L74 to 90 ohm ferrites
84) added 10K pullup to +5V_MAIN to SND_HP_MUTE
85) repinout Sousaphone connector
86) remore redundant pullups on FANL_TACH and FANR_TACH
87) added TP to all NC on NEC USB2 part for NAND tree testing
88) added NEC_USB bomoption to 0 ohm resistor on NEC_AVSS_F

4/30
89) repinout Sousaphone connector (J12)
90) no stuff R322 to eliminate 3V_sleep pump up
91) updated various text notes with correct reference designators

5/1
92) change L30 to 152S0139 (Tokin CPI-1050-2R2) 11A
93) remove FANR_TACH functional test point
94) add CHGND4 and SLEEP_LED functional test points
95) swap INT_AUDIO_TO_SND and SND_TO_AUDIO on Sousaphone connector (J12)

*** rev 01 released for EVT ***

5/6
96) remove NO STUFF on R477 (set 5V and 3.3V switcher in pulse skipping mode)
97) change R337 to 470K and remove No Stuff and no stuff R336 to change Vcore DAC to 1.35V/1.15V
98) change R321 to 499ohm to set 5mV Vcore offset
99) change L72,L73,L74 to 155S0165 (D part for EVT only)

*** rev 02 released for EVT ***

5/7
100) no stuff Q79 to disable 3V_SLEEP sequencing to work around wake from sleep bug with M10
101) added BOM table to define correct part number for M10 without heatspreader (338S0133)

*** rev 03 released for EVT ***

5/22
102) fixed NO STUFF BOM option for R291
103) add NO STUFF to R223 to correct startup level of GPU_VCORE_CNTL
104) add NO STUFF to R300 to complete 3V sequecing on wake from sleep fix
105) changed R376 to 158K and R321 to 2.74K to set CPU_VCORE offset to 35mV

*** rev 04 released for EVT ***

5/19/03
106) changed both AGP_NV_INT_L and AGP_ATI_INT_L to AGP_INT_L
107) removed redundant 3V_GPU pullup R687 (Intrepid side AGP_INT_L pullup)
108) added R699,R701,R707,R708 as 10k pulldowns to Intrepid USB ports A and C when NEC_USB is stuffed
109) changed SND_HP_MUTE_INV gate/inversion FETS to pullup to +3V_MAIN
110) added R711 as pullup to +3V_GPU on AUXWIN signal from M10 (U44)
111) added R698 as 0 ohm jumper between FW_PHY_PD and Intrepid
112) added U56, U57, R718,R714 for VGA Hsync and VGA Vsync buffering
113) changed L72,L73,L74 to 155S0164 (new high speed part)
114) added NO STUFF BOM option to R223 to correct for sense of GPU_VCORE_CNTL
115) added NO STUFF BOM option to R300 to avoid sleep wake problem

6/3/03
116) Intgrated new 1.8V switcher (LTC3412)(U58)(353S0650) and inductor (L75- 152S0142)
117) changed 2.5V_SLEEP FET (U48) and 1.8V_SLEEP FET (U6) to higher current part (Si6467BDQ - 376S0161)
118) added 10K pulldown (R720) on FW_PHY_PD_INT for when R698 is removed
119) changed R728 and R729 to 1210 0ohm resistors to support switching the entire memory bus between 1.8V and 2.5V
120) added R721 as jumper between +2_5V_SLEEP and +2_5V_GPU

6/4/03
121) NO STUFF R631 to remove MAIN_RESET_L from clock slewing chip
122) changed FWB connector to new part with extra ground tabs (514S0059)

6/5/03
123) changed I2C 0 and 1 pullups (RP12) to 2.2K to improve rise/fall times (sensor check config errors)
124) added CRITICAL flag to new 1.8V switcher (U58), inductor (L75), 1.8V sleep FET (U6), and 2.5V sleep FET (48)
125) removed gnd caps (C651 and C647) on I2S clock at sound connector (J12)
126) added LC filter on SND_SYNC for EMI (L77 and C895)
127) added LC filter on SND_CLKOUT for EMI (80 and C899)
128) added LC filter on INT_AUDIO_TO_SND for EMI (L81 and C896)
129) added LC filter on SND_TO_AUDIO for EMI (L82 and C897)
130) added LC filter on SND_AMP_MUTE for EMI (L76 and C898)
131) added LC filter on SND_HW_RESET_L for EMI (L78 and C900)
132) added LC filter on SND_SCLK for EMI (L79 and C901)
133) added C902 and R804 to prevent latch-up condition in GPU Vcore circuit when using powermiser
134) removed R331 (CPU Vcore positioning resistor)
135) changed C728,C729,C730,C731,C732,C733,C734,C884,C885 to 220uF Rubycon caps (128S0024)
136) add Vcore offset change circuit to modify offset in low (Q86,R805,R806,R807,R808,R809)
137) changed Q83 into dual (2N7002DW) and added R810 to invert 3V_5V_ON before switching RUN/SS

6/6/03
138) rotated J26 (FW B connector)
139) changed D29 to B340B (3A part - 371S0159)

6/9/03
140) modified Vcore offset select circuit with Takashi's changes - changed Gnd reference to VCORE_GND_SNS
141) added double inverter to buffer THERM _L_OC (added Q87,R811,R812)
142) removed redundant pullup on THERM_L_OC (R780)

6/9/03
143) added cap on gate of the second FET in Q87 for possible turn on delay (C903)
144) changed inner shield of FWB connector J26 to connect to chassis gnd
145) changed R336 and R325 to 0 ohm to set Vcore VID to 1.3V/1.15V
146) changed R321 to 2.49K to set Vcore offset to +25mV
147) added 10 ohm resistor (R814) and 1uF cap (C904) to filter power to ADT7460 (Gary Leo)

6/10/03
148) changed R612 to 10K to prevent UIDE DMACK from floating
149) changed C80,C88,C81,C89,C82,C102,C79,C87 to NO STUFF (TMDS common-mode termination)
150) changed R205,R218,R211,R219,R210,R220,R204,R214 to 162 ohm 1% (TMDS common-mode termination)
151) changed RP27,RP32,RP28,RP57 to 10ohm (TMDS series termination)

*** released for EVT2 6/10/03 ***

6/13/03
152) fixed NO STUFF on R291
153) removed NO STUFF from C80,C88,C81,C89,C82,C102,C79,C87 (TMDS common-mode termination)
154) removed NO STUFF from R638 (pullup on slewing chip FSEL)
155) removed NO STUFF from C903 (cap on input to second part of THERM_OC_L buffer)
156) CHANGED R321 TO 1K FOR VCORE OFFSET OF 12MV (VCORE = 1.30V -30MV/+100MV)

*** released for EVT2 6/13/03 ***

6/18/03
157) changed R228 to pullup to 1.8V for DVO interface conpatibility
158) added R234 and INT_TMDS option to maintain internal TMDS capability
159) changed L30 to 3 pin symbol
160) added U5 to use as external TMDS transmitter (DVI)
161) added R41 to create +3V_GPU_SI power for SIL1162 (U5)
162) added L14, C130, C132, and C165 for 3V AVCC filtering for SIL1162 (U5)
163) added L13, C14, C129, C131, C133 for 3V PVCC filtering for SIL1162 (U5)
164) added L15, C255, C233, C218 for 3V Vcc filtering for SIL1162 (U5)
165) added R235 and R237 as options for MAIN_RESET_L to U5
166) added R231. R232, and C284 for Vref for U5
167) added R66, R99, R202, R212, R222, R224, R88, R110, R223 as straps for U5
168) added RP58, RP59, RP60, RP61 for series termination of SIL1162 TMDS output
169) added L16, C304, C327, C647 for filtering GPU VDDR4
170) added R255 and R251 to strap GPU_DVODMODE correctly for 1.8V DVO
171) added R268 to connect L16 to +3V_GPU_FLT when not using SIL1162
172) added C681, C668, C678, C651 to filter the thermal sensor diff pairs

6/19/03
173) changed GPU_MEM_IO to +GPU_MEM to connect ATI Vref to correct memory voltage
174) swapped TMDS CLKN and CLKP on RP57 and RP58 for layout
175) swapped DN<0> and DP<0> on RP27 for layout
176) corrected un-named nets in TMDS common-mode filters
177) added physical constraints for new Silicon Image power rails
178) CHANGED C728,C731,C734,C733,C730,C732,C729,C885,C885 TO 128S0022 (124S0024 WILL BE DELETED AS A DUPLICATE IN THE LIBRARY)

6/23/03
179) NO STUFF'ed C895,C899,C896,C897,C898,C900, and C901 to fix no sound problem
180) changed C890 to 100pF for improved transient response (Takashi)
181) Removed bypass traces on FWB chokes and stuffed L70 and L71
182) CHANGED R491 TO 52.3K 1%, R475 TO 127K 1%, AND R476 TO 4.7M 5% IN A29 ADAPTER DETECT CIRCUIT DIVIDERS TO REDUCE SHUTDOWN CURRENT
183) added R331 as CPU Vcore sense resistor (1 mohm 1% 2512)
184) No STUFF'ed C651 and C678
185) added C688,C690,C846,C905 for thermal pair filtering at fan controller
186) added C906 to prevent shoot-thru on Q64 (currently NO STUFF'ed)
187) added C907 to prevent shoot-thru on Q68 (currently NO STUFF'ed)
188) changed R517 to 100K
189) changed GND reference for input side of Q86 to digital GND (the other FET in Q856 remains on VCORE_GNDSNS

6/24/03
190) added C908 to prevent gate shoot-thru on Q56
191) added R279 to power TMDS PLL from LVDS filter when using external TMDS transmitter
192) changed R325 to 470K to set the low Vcore to 1.10V
193) stuffed Vcore offset switch (R807,R805,R809,Q86)
194) changed R809 to 1.5K 1% to set low Vcore offset to 10mV
195) changed R321 to 3.01K 1% to set high Vcore offset to 30mV

6/25/03
196) rotated L70 and L71 for layout (PCB symbol problem)
197) changed Q53,Q54,Q55 to IRF7832 (376S0148) for better thermal performance
198) NO STUFF'ed C908 (Q56 gate shoot-thru cap)

*** released for DVT 6/26/03 ***

7/2/03
199) CHANGED J9 (CARDBUS) TO 516S0141 (NEW PIN PLATING SPEC)
200) CHANGED J20 (AIRPORT) TO 516S0142 (NEW PIN PLATING SPEC)
201) CHANGED J10 (OPTICAL DRIVE) TO 516S0140 (NEW PIN PLATING SPEC)
202) CHANGED J13 (HARD DRIVE) TO 516S0140 (NEW PIN PLATING SPEC)
203) CHANGED J12 (SOUND) TO 516S0144 (NEW PIN PLATING SPEC)
204) CHANGED J8 (MODEM) TO 516S0143 (NEW PIN PLATING SPEC)
205) ADDED BOM TABLE TO PUT 0 OHM 402 ON L77,L80,L81,L82,L76,L78,L79

7/9/03
207) CORRECTED C889 TO CONNECT TO INPUT (PIN 1) OF U55
208) REMOVED POWER JUMPERS XW25,XW17,XW16,XW10,XW14,XW18
209) CHANGED 197S0035 TO PRIMARY AND 197S0004 AS ALTERNATE FOR Y1 (INTREPID)
210) CHANGED 197S0037 TO PRIMARY AND 197S0603 AS ALTERNATE FOR Y3 (ETHERNET)
211) CHANGED 197S0038 TO PRIMARY AND 197S0608 AS ALTERNATE FOR Y5 (NEC USB2)
212) CHANGED 197S0040 TO PRIMARY AND 197S0008 AS ALTERNATE FOR Y4 (LMU)
213) CHANGED 197S0041 TO PRIMARY AND 197S0604 AS ALTERNATE FOR Y6 (PMU)

7/22/03
214) ADDED 1_32V_VCORE AND 1_30V_VCORE BOM OPTIONS FOR 2 DIFFERENT CPU VCORE SPECS
215) UPDATED CAP MATERIAL TYPES
216) CHANGED FROM 715 PIN TO 667 PIN SYMBOL FOR U44 (M10)

7/28/03
217) CHANGED TMDS TERMINATION FROM 2X 162 TO 2X 49.9 OHMS PER PAIR
218) CHANGED 126S0036 FROM ALT TO PRIMARY, REPLACING 126S0035 FOR CPU VCORE INPUT CAPS

*** RELEASED FOR PRODUCTION 7/28/03 ***

8/4/03
219) CHANGED R99 TO NO STUFF TO FIX I2C ADDRESS OF SIL1162 TMDS TRANSMITTER
220) CHANGED R321 TO 4.02K 1% FOR 1_30_VCORE (40MV OFFSET) AND TO 6.34K 1% FOR 1_32_VCORE (60MV OFFSET)
221) CHANGED R304 TO 470K AND R329 AND R325 TO 0 OHM TO CHANGE LOW VID TO 1.05V ON VCORE
222) CHANGED C611 TO 2200PF, C610 TO 100PF, AND R519 TO 12.7K 1% TO INCREASE IMMUNITY TO 3.3V PGOOD SIGNAL DROPOUT
223) NO STUFF C590 TO INCREASE IMMUNITY TO 3.3V PGOOD SIGNAL DROPOUT
224) CHANGED C583 TO 2200PF, C576 TO 100PF, AND R481 TO 15.0K 1% TO INCREASE IMMUNITY TO 3.3V PGOOD SIGNAL DROPOUT
225) NO STUFF C566 TO INCREASE IMMUNITY TO 3.3V PGOOD SIGNAL DROPOUT

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401258	AA

SCALE: NONE

SHT 40 OF 44

*** Signal Cross-Reference for the entire design ***

```
+1_0V_MARVELL    27D2< 38B3>
+1_5V_AGP        12C5< 12D1< 12D4< 15D6< 16C8<
               18C6< 18D6< 19A8< 19B4<> 19D5<>
               21B8< 21D6< 38C3>
+1_5V_AGP_GPU    21C5< 38C3>
+1_5V_AGP_NECK   19B4<> 38B3>
+1_5V_GPU_VDD15  19D3< 38C3>
+1_5V_INTREPID_PLL  8D6< 12D4< 12D8< 14D6<> 38D3>
+1_5V_INTREPID_PLL1  14C3< 38D3>
+1_5V_INTREPID_PLL2  14D3< 38D3>
+1_5V_INTREPID_PLL3  14D3< 38D3>
+1_5V_INTREPID_PLL4  14D3< 38D3>
+1_5V_INTREPID_PLL5  12D3< 38D3>
+1_5V_INTREPID_PLL6  12D6< 38D3>
+1_5V_INTREPID_PLL7  8D5< 38D3>
+1_5V_INTREPID_PLL8  14D3< 38D3>
+1_5V_LDO        35D8< 38D6>
+1_5V_MAIN       38D6>
+1_5V_SLEEP      38D6>
+1_5V_SLEEP_NECK  21A3<> 38B3>
+1_5V_SLEEP_VIN  35D8<> 38D6>
```

```
PCI_IRDY_L       12B7< 12C7<> 17B7<> 24C6<> 26B7<>
                 17C5> 39A5>
PCI_PAR          12C7<> 17B7<> 24C5<> 26B7<> 37C5>
                 39D4>
PCI_STOP_L       12A7< 12C7<> 17B7<> 24C5<> 26B7<>
                 37C5> 39A5>
PCI_TRDY_L       12B7< 12C7<> 17A7<> 24C5<> 26B7<>
                 37C5> 39A5>
PLL_STOP_L       7C4<> 7C8<>
PMU_ACK_L        14C2< 30C4<>
PMU_AC_DET       30A4< 30B4<>
PMU_AC_IN        30B4<>
PMU_BATT0_DET_L  30B4<>
PMU_BATT1_DET_L_PU  30B4<> 30D2<
PMU_BATT_DET_L   30B3< 30D2< 31A4<> 39C3>
PMU_BYTE         30B6< 30C7<
PMU_CAPSLOCK_LED_L  30C6<>
PMU_CHARGE_V     30C4<> 31B8<>
PMU_CHRG_BATT_0  30C4<> 31A8<>
PMU_CLK          14C2<> 30C4<>
PMU_CNVSS        30B6< 30C7<
PMU_CPU_HRESET_L  23A4< 23C4<> 30C4<>
PMU_EPM          30D2< 30D4<>
PMU_FROM_INT     14C2<> 30C4<>
PMU_I2C_CLK      30B4<> 30C2<
PMU_I2C_DATA     30B4<> 30C2<
PMU_INT_L        14B5<> 14B7< 30B6<>
PMU_INT_NMI      14B5<> 14B7< 30D4<>
PMU_KB_RESET_IN1  30A7<>
PMU_KB_RESET_IN2  30A7<>
PMU_KB_RESET_L   30A6> 30B7< 39B2>
PMU_LID_CLOSED_L  23A8< 23C4<> 30B2< 30C4<>
PMU_NMI_BUTTON_L  25C1< 30C2< 30C4<>
PMU_NMI_L        30C2< 30C4<>
PMU_NUMLOCK_LED_L  30C6<>
PMU_OOPS         30B2< 30B4<>
PMU_PME_L        14B5<> 26B8< 30B2< 30C4<>
PMU_POWERUP_OK   30B4<> 30D2<
PMU_POWER_UP_L   29C7<> 30C6<> 30D7< 33B8<
PMU_REQ_L        14B7< 14C2> 30C4<>
PMU_RESET_BUTTON_L  25B1< 30C4<> 30D2<
PMU_RESET_L      30B6<>
PMU_SLEEP_LED    23C4<>
PMU_SLEEP_LED_L  23C2<> 30C4<>
PMU_SMB_CLK      30B4<> 30C2< 31A3<
PMU_SMB_DATA     30B4<> 30C2< 31A2<
PMU_TO_INT       14C2<> 30C4<>
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POWER_VALID      30B2< 30C4<>
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RAM_DQM_A<7>     10C1<> 11A6<> 36A5>
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RAM_DQS_A<2>     10B6<> 11C8<>
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RAM_DQS_A<3>     10C5<> 11C8<>
RAM_DQS_A<4>     10B4<> 11B8<>
RAM_DQS_A<5..4>  36B5>
RAM_DQS_A<5>     10C3<> 11A8<>
RAM_DQS_A<6>     10B2<> 11A8<> 36B5>
RAM_DQS_A<7>     10C1<> 11A8<> 36A5>
RAM_DQS_B<0>     10B8<> 11D3<> 36C5>
RAM_DQS_B<1>     10C8<> 11D3<> 36C5>
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RAM_DQS_B<3..2>  36B5>
RAM_DQS_B<3>     10C6<> 11C3<>
RAM_DQS_B<4>     10C4<> 11B3<>
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RAM_DQS_B<6>     10C2<> 11A3<> 36B5>
RAM_DQS_B<7>     10C2<> 11A3<> 36A5>
RAM_MUXSEL_H     10A3< 10A5< 10B1<> 10B3<> 36A5>
RAM_MUXSEL_L     10A3< 10A5< 10B5<> 10B7<> 36A5>
RAM_RAS_L        9A4< 11B5<> 11B6<> 36A5>
RAM_WE_L         9A4< 11B3<> 11B8<> 36A5>
RF_DISABLE_L_SPN  24D6<> 39C1>
RIGHT_USB_DM     26A3< 32A7<> 37A2> 39D1>
RIGHT_USB_DP     26A3< 32A7<> 37A2> 39D1>
RJ45_C0_PD       27B2<>
RJ45_C1_PD       27B2<>
RJ45_C2_PD       27B2<>
RJ45_C3_PD       27B2<>
RJ45_DM<0>       27B2<> 37D2> 39B3>
RJ45_DM<1>       27B2<> 37D2> 39B3>
RJ45_DM<2>       27B2<> 37D2> 39A3>
RJ45_DM<3>       27B2<> 37D2> 39A3>
RJ45_DP<0>       27B2<> 37D2> 39B3>
RJ45_DP<1>       27B2<> 37D2> 39B3>
RJ45_DP<2>       27B2<> 37D2> 39A3>
RJ45_DP<3>       27B2<> 37D2> 39A3>
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ROM_OE_L         9B3< 12A5< 24C5<> 39B1>
ROM_ONBOARD_CS_L  9B3< 24C6<> 39B1>
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RSDP5_TP         26C5>
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SI_PD            20B7<
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SLEEP_L_LS5_INV  35A3< 35C2< 35C8<>
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SND_HP_MUTE_L    14C5<> 25C4<>
SND_HP_SENSE_L   14B5<> 25D6<> 39C6>
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SND_HW_RESET_L_F  25C6<> 25C7<
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SND_SCLK         14B1< 25C8< 36B1> 39C6>
SND_SCLK_F       25C7< 25D7<>
SND_SYNC         14B1< 25D8< 39D6>
SND_SYNC_F       25C7<> 25D7<
SND_TO_AUDIO     14B1< 25D8< 39D6>
SND_TO_AUDIO_F   25D6<> 25D7<
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ST7_SENSOR4_SDA_PD  23B2< 23D4<>
ST7_SENSOR5_SCK_PU  23B2< 23D4<>
ST7_SENSOR5_SDA_PU  23B2< 23D4<>
ST7_SLEEP_LED_H  23C2<> 23C4<>
ST7_XTAL_IN      23C5<
STOP_AGP_L       12D2< 12D4<>
SUPPLY_M_DM      25B6< 25B8<
SUPPLY_M_DP      25B6< 25B8<
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SUTRO_ALS_OUT    23C4<> 24B2<> 39C2>
SYSCLK_CPU       5C3< 8A6< 36D1>
SYSCLK_CPU_UF    8A6<> 36D1>
SYSCLK_DDRCLK_A0  9D4< 11D8<> 36D1>
SYSCLK_DDRCLK_A0_L  9D4< 11D8<> 36D1>
SYSCLK_DDRCLK_A0_L_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_A0_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_A1  9D4< 11A6<> 36D1>
SYSCLK_DDRCLK_A1_L  9D4< 11A6<> 36D1>
SYSCLK_DDRCLK_A1_L_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_A1_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_B0  9D4< 11D3<> 36D1>
SYSCLK_DDRCLK_B0_L  9C4< 11D3<> 36C1>
SYSCLK_DDRCLK_B0_L_UF  9B6<> 9C5< 36D1>
SYSCLK_DDRCLK_B0_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_B1  9D4< 11A5<> 36C1>
SYSCLK_DDRCLK_B1_L  9D4< 11A5<> 36C1>
SYSCLK_DDRCLK_B1_L_UF  9B6<> 9D5< 36D1>
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THERM1_M_DP      37A2>
THERM2_A_DM      25A6< 25A8< 37A2>
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THERM2_DP        25A5< 25B5<> 25B5< 37A2>
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THERM2_M_DP      37A2>
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TMDS_CLKP        20B3< 20C2< 20C3< 22C7<> 37B2>
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TMDS_CONN_CLKP   22C6<> 22C7<> 37B2> 39D7>
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TMDS_DN<1>       20A3< 20B1< 20C3< 22B8<> 37B2>
                 39AB>
TMDS_DN<2>       20A1< 20A3< 20B3< 22B7<> 37B2>
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TMDS_DP<0>       20B2< 20B3< 20C3< 22B8<> 37B2>
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TMDS_DP<1>       20A3< 20B2< 20C3< 22B8<> 37B2>
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TMDS_DP<2>       20A2< 20A3< 20B3< 22B7<> 37B2>
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TPAD_F_RXD       23A7<> 39C4>
TPAD_F_TXD       23A7<> 39C4>
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TPAD_TXD         23A8< 30B2< 30C4<>
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TV_GND2          22A6<> 38B6> 39A7>
TV_Y             22A6<> 39D6>
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UIDE_DMACK_L     13C7<> 24A4< 37C5>
UIDE_DMARQ       13C7<> 37C5>
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UIDE_IOCHRDY     13C7< 24A4< 37C5>
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USB2_PCI_GNT_L   12C7<> 26B7<
USB2_PCI_INT_L   14B5<> 14C7< 26A8<
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USB_DEP          14B2<> 14C2< 37B2>
USB_DFM          14B2<> 14B2< 37B2>
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USB_PWREN_EF_L   14B2<> 14D7<
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VCORE_BST        34C5<> 38C1>
VCORE_CC         34B6<> 38B1>
VCORE_CNTL_RC    19A3<>
VCORE_DH         34B5<> 38C1>
VCORE_DL         34B5<> 38C1>
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VCORE_GNDA       34B6<>
VCORE_GNDDIV     34A4< 34B5< 38B1>
VCORE_GNDDIV_TEST  34A3<>
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VCORE_GNDSNS_TEST  34A3<>
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VCORE_LX         34B5<> 38C1>
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VCORE_MUX_SEL    34D5<>
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VCORE_TIME       34B4<> 38B1>
VCORE_TON        34B6< 38C1>
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VCORE_VGATE      14B5< 14B7< 34B4> 38B1>
VCORE_VID0       39A3>
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VGA_B            22C6<> 22D7< 39D7>
VGA_G            22C5<> 22D7< 39D7>
VGA_HSYNC        22C6<> 22C7< 39D7>
VGA_HSYNC_BUF    22C8<>
VGA_R            22C5<> 22D7< 39D7>
VGA_VSYNC        22C5<> 22C7< 39D7>
VGA_VSYNC_BUF    22C8<>
ZV_LCDDATA20_PU  19C7<>
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*** Part Cross-Reference for the entire design ***

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J10 CON_M50SR_5MM 24
J11 CON_F14RT_S2MT_SM 32
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U19	PWR_CNTRL_TPS2211	17
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