

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
B		293301	PRODUCTION RELEASED		
				DATE	DATE
				09/11/03	?

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2	SYSTEM BLOCK DIAGRAM
3	POWER BLOCK DIAGRAM
4	PCB NOTES AND HOLES
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6	MPC7450 DATA
7	CPU PLL AND CONFIGURATION STRAPS
8	INTREPID MAXBUS AND BOOT STRAPS
9	INTREPID MEMORY INTERFACE / BOOT ROM
10	DDR MEMORY MUXES
11	200PIN DDR MEMORY SODIMM CONNECTORS
12	INTREPID AGP 4X/PCI
13	INTREPID ENET/FW/UATA/EIDE INTERFACES
14	INTREPID GPIO/SERIAL/USB INTERFACES/SSCG
15	INTREPID POWER RAILS
16	INTREPID DECOUPLING
17	CARDBUS CONTROLLER (PCI1510)
18	M10 AGP & CLOCKS
19	M10 LVDS/TMDS/VGA/GPIO & GPU VCORE
20	SIL1162 TMDS TRANSMITTER
21	M10 ANALOG, POWER, GND

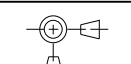
PAGE	CONTENTS
22	VIDEO CONNECTORS - INVERTER, DVI, S-VIDEO DUAL-CHANNEL LVDS
23	LMU, LIGHT SENSOR, BOOTBANGER, SLEEP LED SPIDEY - KBD,TPAD,HALL EFFECT,PWR BUTTON
24	INTERNAL CONNECTORS - DVD, CARDSLOT, HARD DRIVE, LEFT USB/BLUETOOTH
25	FAN CONTROLLER, MODEM, SOUND SERIAL DEBUG (JOLLY ROGER, PWR/NMI/RESET)
26	USB 2.0
27	MARVELL GIGABIT ETHERNET PHY
28	FIREWIRE A/B PHY
29	FIREWIRE A/B CONNECTORS, PORT POWER LIMITER
30	PMU (POWER MANAGEMENT UNIT)
31	BATTERY CHARGER AND CONNECTOR
32	12.8V SYSTEM POWER SUPPLY / PMU POWER SUPPLY
33	3.3V / 5V SYSTEM POWER SUPPLIES
34	CPU CORE VOLTAGE POWER SUPPLY
35	1.5V/ 1.8V / 2.5V SYSTEM POWER SUPPLIES
36	SIGNAL CONSTRAINTS (1 OF 3) - DIGITAL/CLK
37	SIGNAL CONSTRAINTS (2 OF 3) - DIGITAL/DIFF
38	SIGNAL CONSTRAINTS (3 OF 3) - POWER NETS
39	FUNCTIONAL TEST POINTS
40	REVISION HISTORY (1 OF 1)
41-42	SIGNAL NAMES
43-44	COMPONENT LOCATIONS

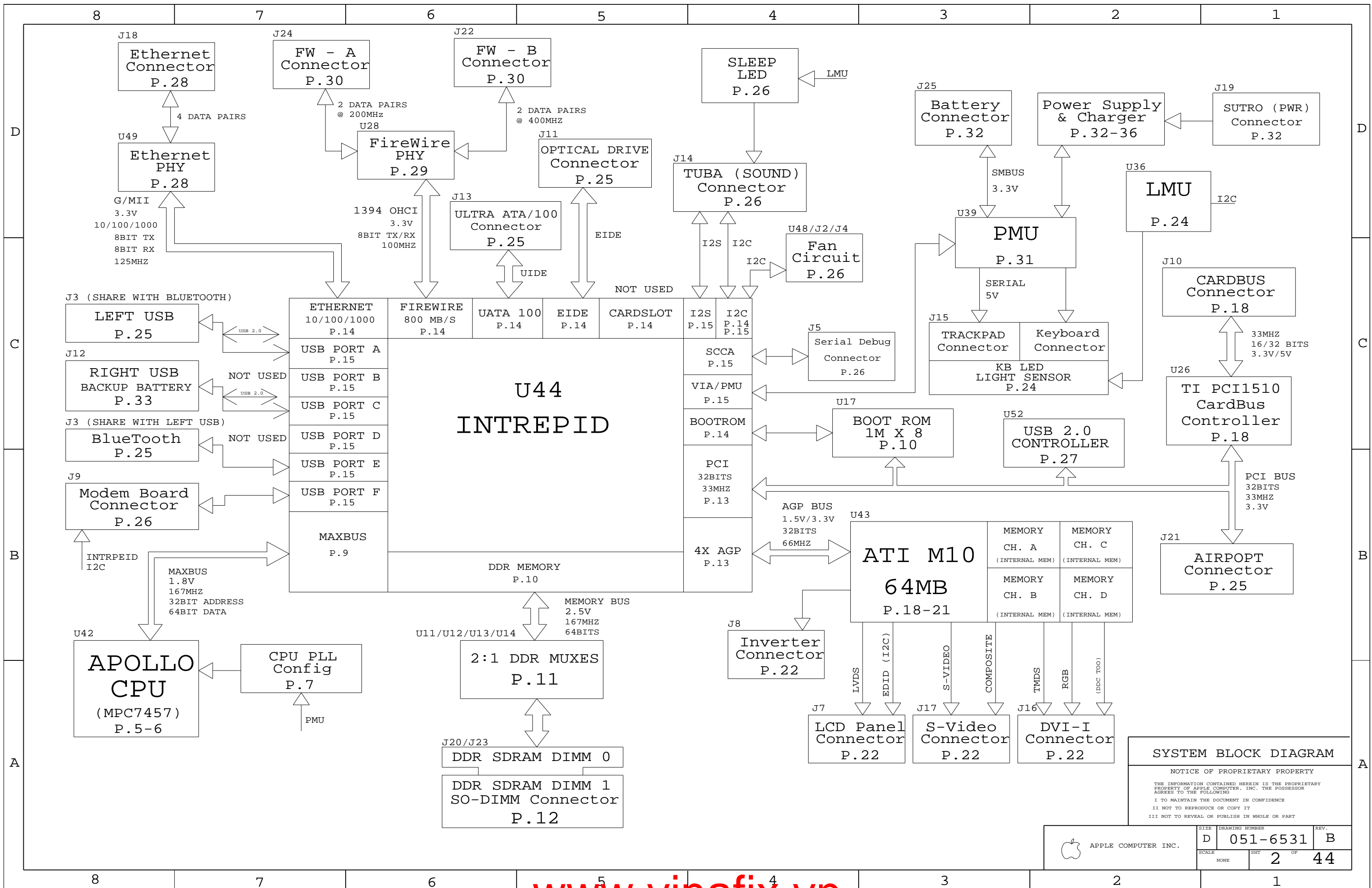
SCHEM, MLB, PB17 "

09/04/2003

BOM OPTIONS	STUFF	NO STUFF
D3_HOT		✓
D3_COLD	✓	
GPU_SS	✓	
GPU_SWITCH	✓	
SERIAL_DEBUG		✓
VCORE_OFFSET	✓	
1_8V_MAXBUS	✓	
1_5V_MAXBUS		✓
NEC_USB	✓	
INTREPID_USB		✓
BBANG		✓
NO_BBANG	✓	
ATI_MEMIO_HI	✓	
ATI_MEMIO_LO		✓
SSCG		✓
NO_SSCG	✓	
5V_HD_LOGIC	✓	
3V_HD_LOGIC		✓
EXT_TMDS	✓	
INT_TMDS		✓
NO_4XVCORE	✓	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6531	1	SCHEM,MLB,PB17 INCH	SCH1	
820-1524	1	PCBF,MLB,PB17 INCH	PCB1	

DIMENSIONS ARE IN MILLIMETERS		METRIC		Apple Computer Inc.	
xx : _____		DRAPTER	DESIGN CK	NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	
x.xx : _____		ENG APPD	MFG APPD		
x.xxx : _____		QA APPD	DESIGNER		
ANGLES : _____		RELEASE	SCALE		
DO NOT SCALE DRAWING		NONE		TITLE	
 THIRD ANGLE PROJECTION		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE D	DRAWING NUMBER
				051-6531	REV. B
				SHT 1 OF 44	

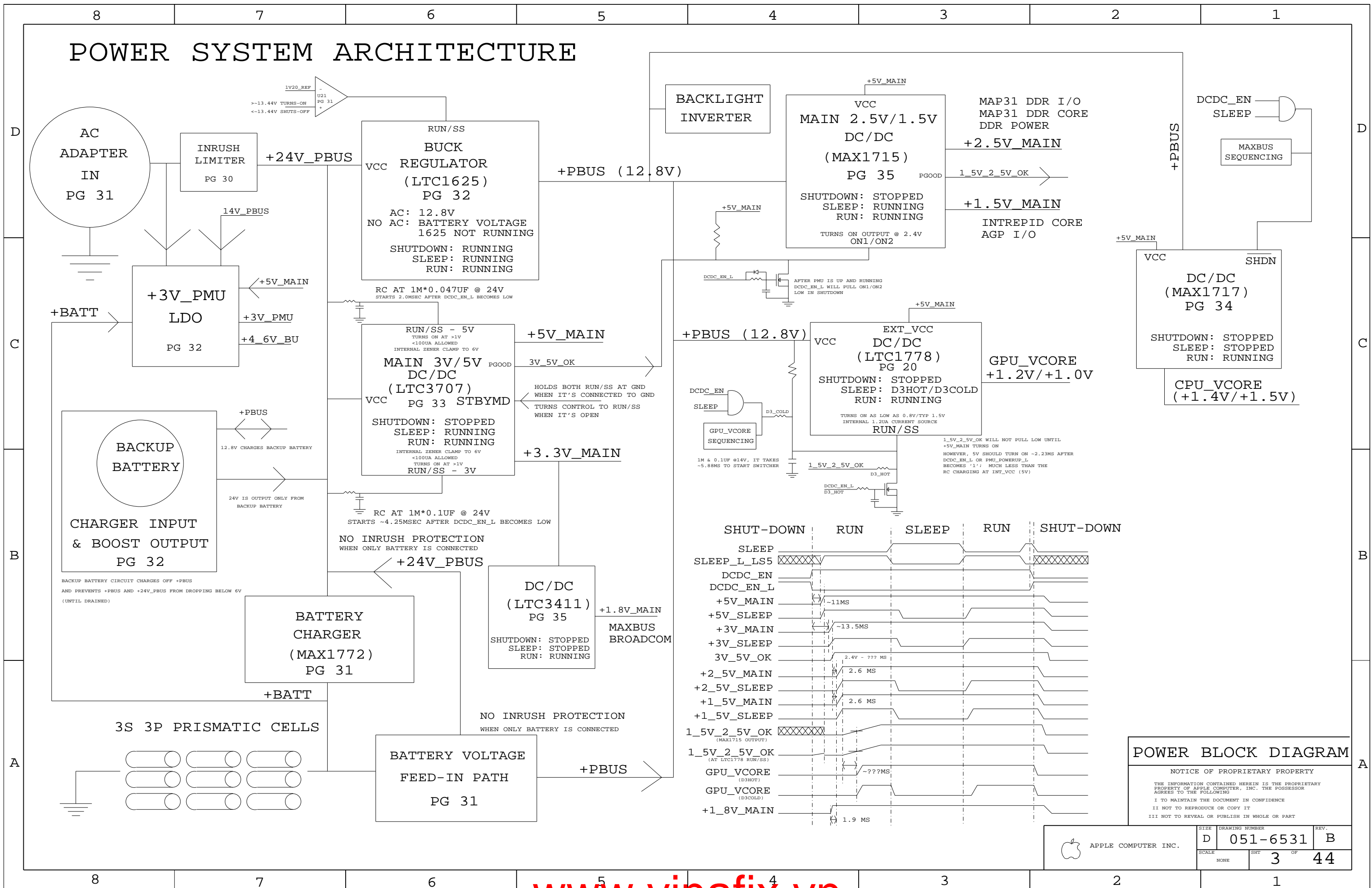


SYSTEM BLOCK DIAGRAM

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	NONE	051-6531	B
SCALE		SHT	OF
NONE		2	44

POWER SYSTEM ARCHITECTURE



POWER BLOCK DIAGRAM

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	D	051-6531	B
SCALE	NONE	SHT	3 OF 44

PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
 1/2 OZ CU THICKNESS: 0.7 MILS
 1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
 DIELECTRIC: FR-4
 LAYER COUNT: 12
 SIGNAL TRACE WIDTH: 4 MILS
 SIGNAL TRACE SPACING: 4 MILS
 PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

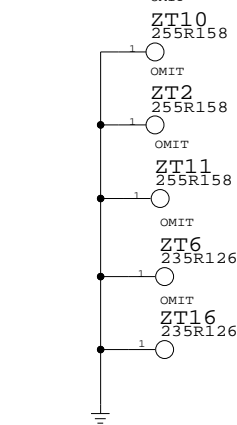
BOARD STACK-UP AND CONSTRUCTION

20R10 TH VIA OR VIA IN PAD

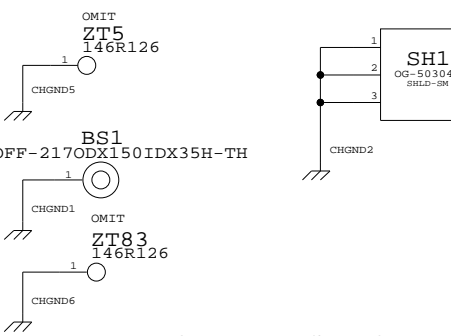
1	SIGNAL (1/3 OZ + COPPER PLATING)
2	PREPREG (3MIL) GROUND (1/2 OZ)
3	LAMINATE (4MIL) SIGNAL (1/2 OZ)
4	PREPREG (3MIL) SIGNAL (1/2 OZ)
5	LAMINATE (4MIL) GROUND (1/2 OZ)
6	PREPREG (2MIL) CUT POWER PLANE(1 OZ)
7	LAMINATE (3MIL) CUT POWER PLANE(1 OZ)
8	PREPREG (2MIL) GROUND (1/2 OZ)
9	LAMINATE (4MIL) SIGNAL (1/2 OZ)
10	PREPREG (3MIL) SIGNAL (1/2 OZ)
11	LAMINATE (4MIL) GROUND (1/2 OZ)
12	PREPREG (3MIL) SIGNAL (1/3 OZ + COPPER PLATING)

BOARD HOLES

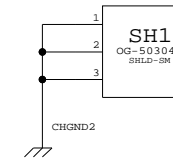
ASICS HEATSINK MOUNTS



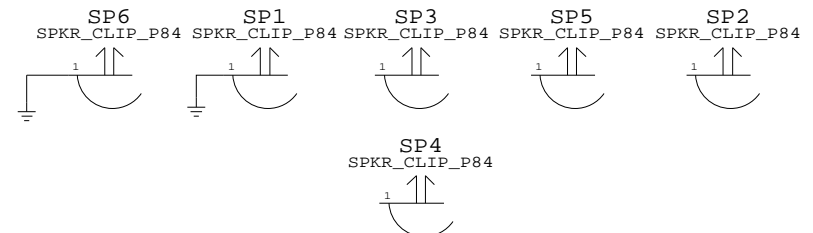
CHASSIS MOUNTS



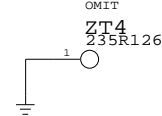
INVERTER



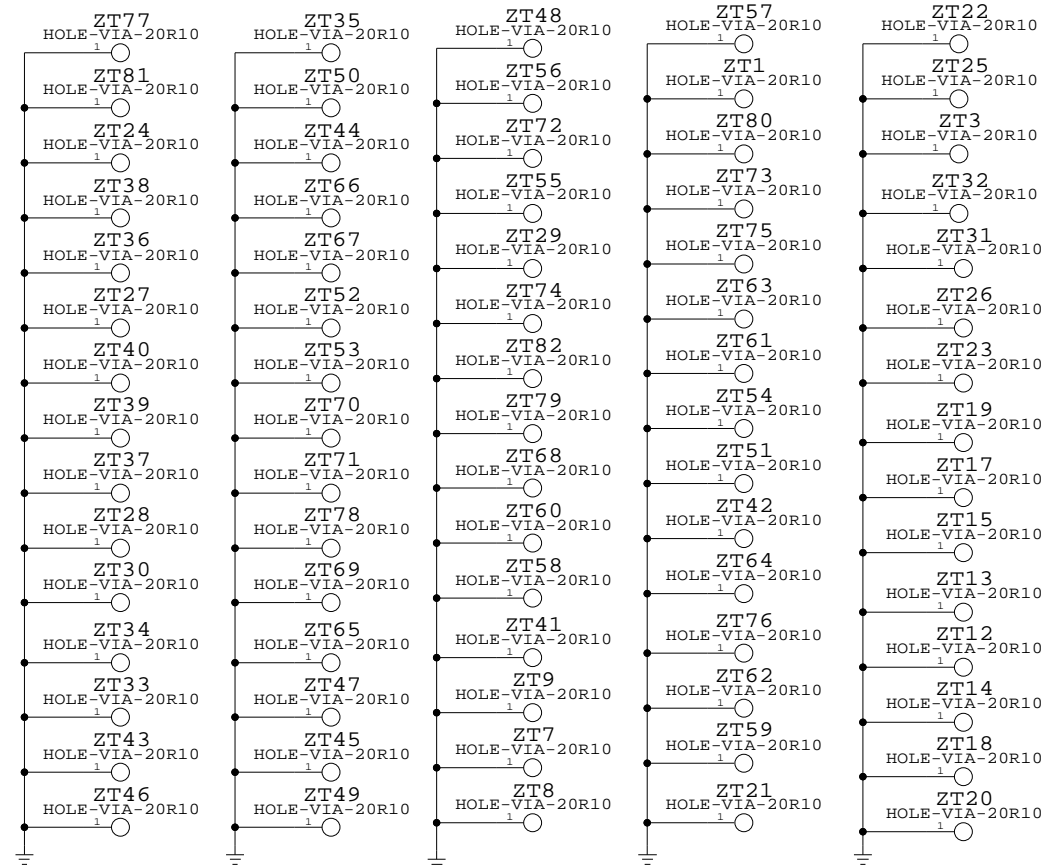
SPEAKER CLIPS



CONDUCTIVE MOUNTS



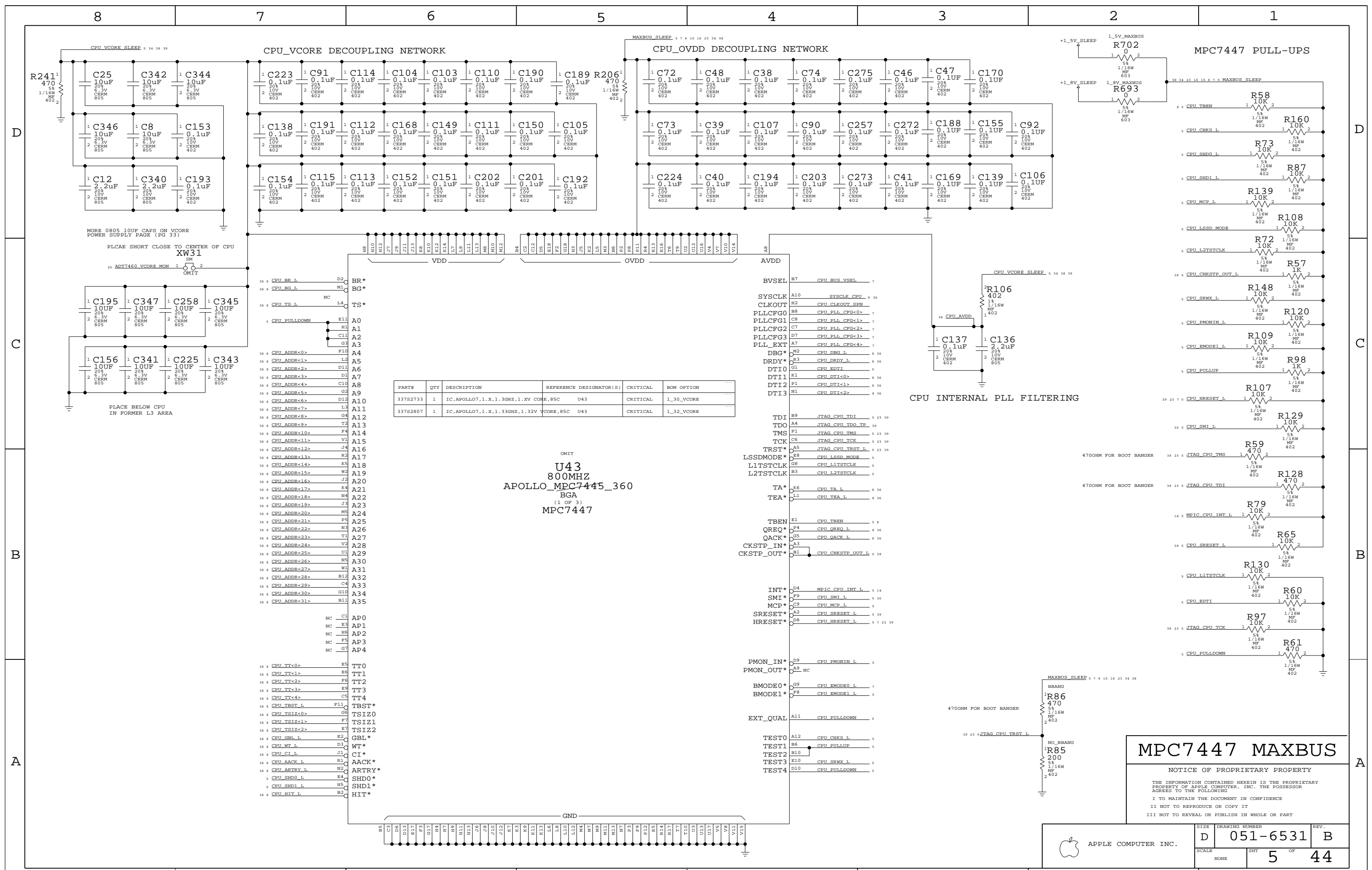
GROUND VIAS



BOARD INFORMATION

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	D	051-6531	B
SCALE	NONE	SHT	4 OF 44



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33782733	1	IC, APOLLO7, 1. X, 1.3GHZ, 1.1XV CORE, 85C	U43	CRITICAL	1_30_VCORE
33782807	1	IC, APOLLO7, 1. X, 1.3GHZ, 1.32V VCORE, 85C	U43	CRITICAL	1_32_VCORE

OMIT
U43
800MHZ
APOLLO_MPC7445_360
BGA
 (1 OF 3)
MPC7447

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33782733	1	IC, APOLLO7, 1. X, 1.3GHZ, 1.1XV CORE, 85C	U43	CRITICAL	1_30_VCORE
33782807	1	IC, APOLLO7, 1. X, 1.3GHZ, 1.32V VCORE, 85C	U43	CRITICAL	1_32_VCORE

MPC7447 MAXBUS

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	SCALE NONE	SHEET 5	OF 44

8

7

6

5

4

3

2

1

BOOT BANGER - LMU PERORMS THIS FUNCTION IF NEEDED
SEE PAGE 22

```

36 CPU_DATA<0> R15 D0
36 CPU_DATA<1> W15 D1
36 CPU_DATA<2> T14 D2
36 CPU_DATA<3> V16 D3
36 CPU_DATA<4> W16 D4
36 CPU_DATA<5> T15 D5
36 CPU_DATA<6> U15 D6
36 CPU_DATA<7> P14 D7
36 CPU_DATA<8> V13 D8
36 CPU_DATA<9> W13 D9
36 CPU_DATA<10> T13 D10
36 CPU_DATA<11> P13 D11
36 CPU_DATA<12> U14 D12
36 CPU_DATA<13> W14 D13
36 CPU_DATA<14> R12 D14
36 CPU_DATA<15> T12 D15
36 CPU_DATA<16> W12 D16
36 CPU_DATA<17> V12 D17
36 CPU_DATA<18> N11 D18
36 CPU_DATA<19> N10 D19
36 CPU_DATA<20> R11 D20
36 CPU_DATA<21> U11 D21
36 CPU_DATA<22> W11 D22
36 CPU_DATA<23> T11 D23
36 CPU_DATA<24> R10 D24
36 CPU_DATA<25> N9 D25
36 CPU_DATA<26> P10 D26
36 CPU_DATA<27> U10 D27
36 CPU_DATA<28> R9 D28
36 CPU_DATA<29> W10 D29
36 CPU_DATA<30> U9 D30
36 CPU_DATA<31> V9 D31
36 CPU_DATA<32> W5 D32
36 CPU_DATA<33> U6 D33
36 CPU_DATA<34> T5 D34
36 CPU_DATA<35> U5 D35
36 CPU_DATA<36> W7 D36
36 CPU_DATA<37> R6 D37
36 CPU_DATA<38> P7 D38
36 CPU_DATA<39> V6 D39
36 CPU_DATA<40> P17 D40
36 CPU_DATA<41> R19 D41
36 CPU_DATA<42> V18 D42
36 CPU_DATA<43> R18 D43
36 CPU_DATA<44> V19 D44
36 CPU_DATA<45> T19 D45
36 CPU_DATA<46> U19 D46
36 CPU_DATA<47> W19 D47
36 CPU_DATA<48> U18 D48
36 CPU_DATA<49> W17 D49
36 CPU_DATA<50> W18 D50
36 CPU_DATA<51> T16 D51
36 CPU_DATA<52> T18 D52
36 CPU_DATA<53> T17 D53
36 CPU_DATA<54> W3 D54
36 CPU_DATA<55> V17 D55
36 CPU_DATA<56> U4 D56
36 CPU_DATA<57> U8 D57
36 CPU_DATA<58> U7 D58
36 CPU_DATA<59> R7 D59
36 CPU_DATA<60> P6 D60
36 CPU_DATA<61> R8 D61
36 CPU_DATA<62> W8 D62
36 CPU_DATA<63> T8 D63

```

OMIT
U43
800MHZ
BGA
(2 OF 3)

APOLLO_MPC7445_360

```

NC_T3 DP0
NC_W4 DP1
NC_T4 DP2
NC_W9 DP3
NC_M6 DP4
NC_V3 DP5
NC_N8 DP6
NC_W6 DP7

```

```

NC_F18 NC_F18
NC_F17 NC_F17
NC_F19 NC_F19
NC_H19 NC_H19
NC_H18 NC_H18
NC_H17 NC_H17
NC_H16 NC_H16
NC_E19 NC_E19
NC_D18 NC_D18
NC_F16 NC_F16
NC_G16 NC_G16
NC_D19 NC_D19
NC_F15 NC_F15
NC_G19 NC_G19
NC_E16 NC_E16
NC_D17 NC_D17
NC_D16 NC_D16

```

OMIT
U43
800MHZ
BGA
(3 OF 3)

APOLLO_MPC7445_360

```

NC_P15 NC_P15
NC_L15 NC_L15
NC_N15 NC_N15
NC_P18 NC_P18
NC_N14 NC_N14
NC_M14 NC_M14
NC_M17 NC_M17
NC_N13 NC_N13
NC_N16 NC_N16
NC_M19 NC_M19
NC_M16 NC_M16
NC_P19 NC_P19
NC_N17 NC_N17
NC_M15 NC_M15
NC_L17 NC_L17
NC_L14 NC_L14
NC_K15 NC_K15
NC_J14 NC_J14
NC_J18 NC_J18
NC_J19 NC_J19
NC_J15 NC_J15
NC_K19 NC_K19
NC_J16 NC_J16
NC_H15 NC_H15
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NC_P16 NC_P16
NC_M18 NC_M18
NC_L19 NC_L19
NC_L18 NC_L18
NC_K18 NC_K18
NC_J17 NC_J17
NC_K16 NC_K16
NC_C19 NC_C19
NC_D15 NC_D15
NC_G15 NC_G15
NC_C18 NC_C18
NC_A16 NC_A16
NC_B19 NC_B19
NC_A19 NC_A19
NC_D14 NC_D14
NC_E15 NC_E15
NC_B15 NC_B15
NC_B17 NC_B17
NC_C17 NC_C17
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NC_E14 NC_E14
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NC_C15 NC_C15
NC_A17 NC_A17
NC_G12 NC_G12
NC_F14 NC_F14
NC_F13 NC_F13
NC_E13 NC_E13
NC_B16 NC_B16
NC_A15 NC_A15
NC_C14 NC_C14
NC_A18 NC_A18
NC_A13 NC_A13
NC_F12 NC_F12
NC_A14 NC_A14
NC_G11 NC_G11
NC_C13 NC_C13

```

```

NC_N12 NC_N12
NC_N18 NC_N18
NC_K17 NC_K17
NC_N19 NC_N19
NC_B18 NC_B18
NC_E12 NC_E12
NC_B13 NC_B13
NC_B14 NC_B14
NC_A6 NC_A6

```

MPC7447 / BBANG

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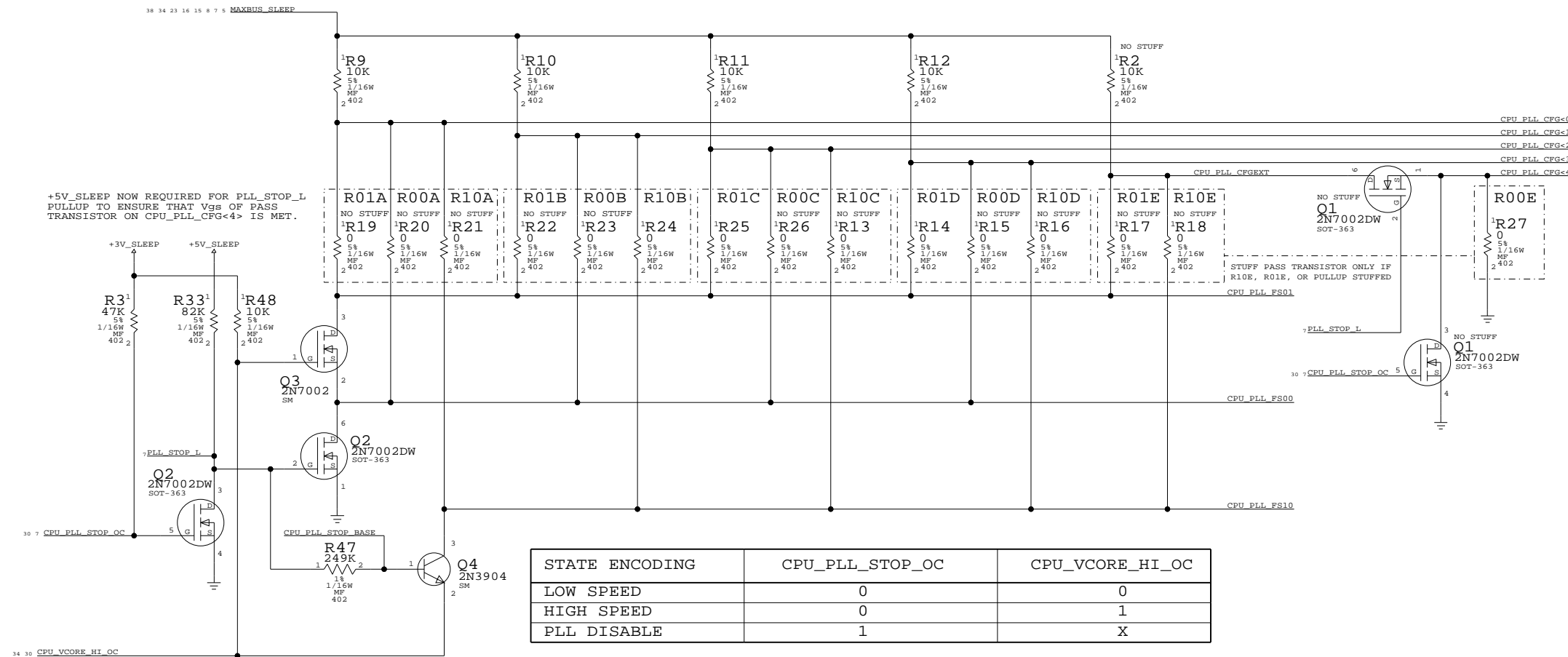
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	D	051-6531	B
SCALE	NONE	SHT	OF
		6	44

CPU PLL CONFIG CIRCUITRY



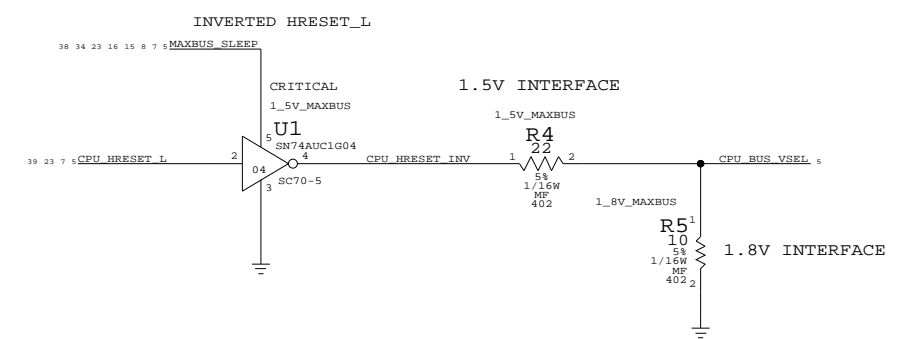
CPU FREQUENCY CONFIGURATION

APOLLO 7

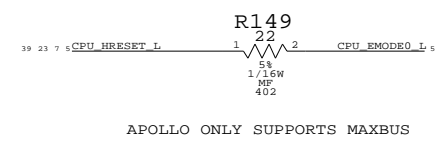
MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY)		CPU_PLL_CFG E ABCD HEX
	167MHZ	133MHZ	
0.0X	PLL OFF		0 1111 0F
1.0X	PLL BYPASS		0 0011 03
2.0X	333	267	0 0100 04
3.0X	500	400	0 1000 08
4.0X	667	533	0 1010 0A
5.0X	833	667	0 1011 0B
5.5X	917	733	0 1001 09
6.0X	1000	800	0 1101 0D
6.5X	1083	867	0 0101 05
7.0X	1167	933	0 0010 02
7.5X	1250	1000	0 0001 01
8.0X	1333	1067	0 1100 0C
8.5X	1417	1133	0 0110 06
9.0X	1500	1200	1 0111 17
9.5X	1583	1267	0 0111 07
10.0X	1667	1333	1 1010 1A
10.5X	1750	1400	1 1000 18
11.0X	1833	1467	1 1001 19
11.5X	1917	1533	0 0000 00
12.0X	2000	1600	1 1011 1B
12.5X	2083	1667	1 1111 1F
13.0X	2167	1733	1 0101 15
13.5X	2250	1800	0 1110 0E
14.0X	2333	1867	1 1100 1C
15.0X	2500	2000	1 0001 11
16.0X	2667	2133	1 1101 1D
17.0X	2833	2267	1 0000 10
18.0X	3000	2400	1 0010 12
20.0X	3333	2667	1 0011 13
21.0X	3500	2800	1 0100 14
24.0X	4000	3200	1 0110 16
28.0X	4667	3733	1 1110 1E

CPU CONFIGURATION

MAXBUS VSEL



BUSTYPE SELECT



DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L
NEED TO CHARACTERIZE

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

CPU CONFIGURATION

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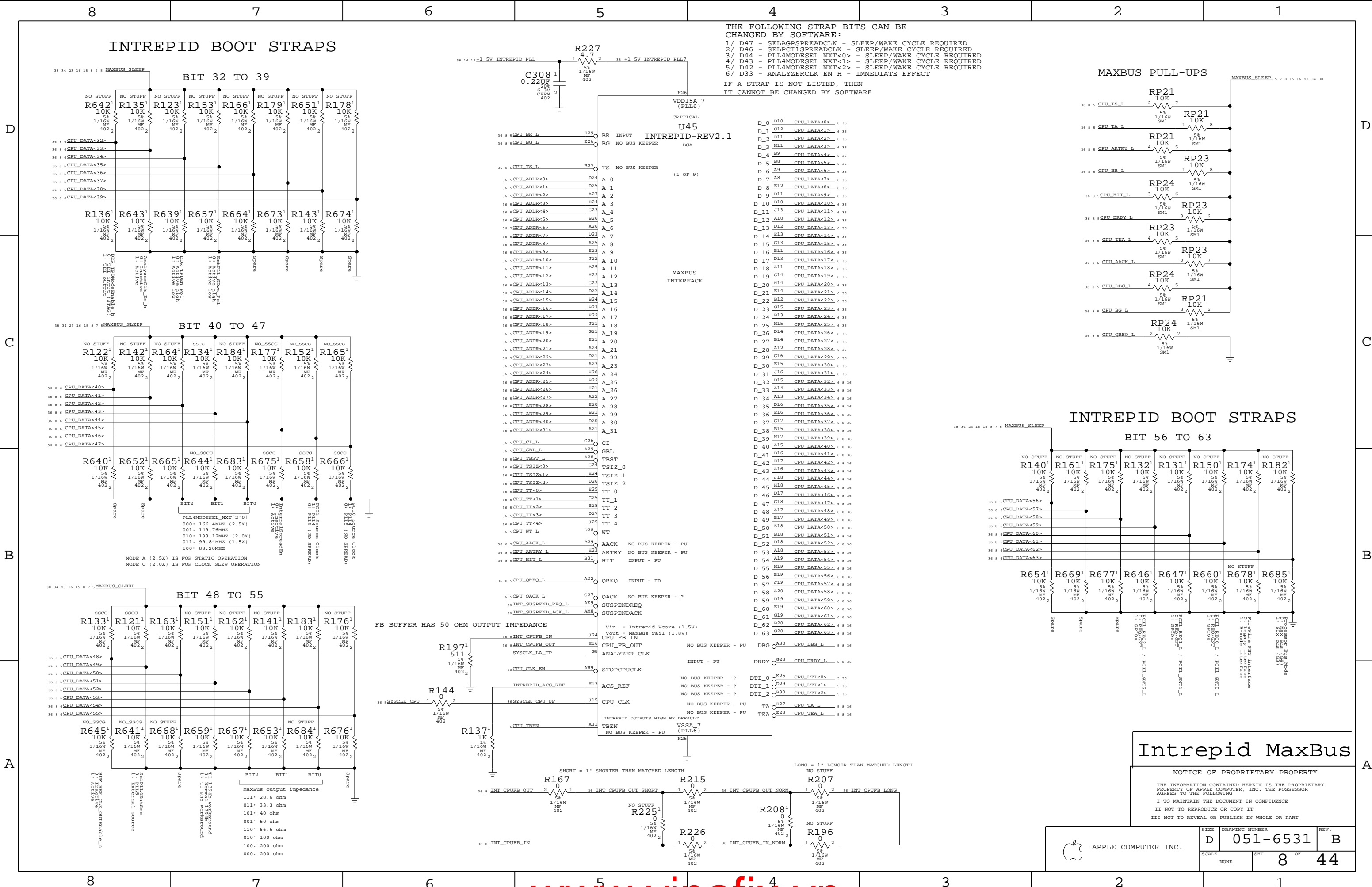
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6531	B
SCALE	NONE	SHT	7 OF 44

INTREPID BOOT STRAPS

THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:

- 1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
- 2/ D46 - SELPCILSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
- 3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
- 4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
- 5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
- 6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT

IF A STRAP IS NOT LISTED, THEN IT CANNOT BE CHANGED BY SOFTWARE



INTREPID BOOT STRAPS

Intrepid MaxBus

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SCALE NONE	SHEET 8	DRAWING NUMBER 051-6531	REV. B

SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

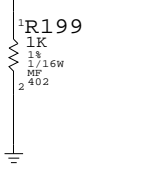
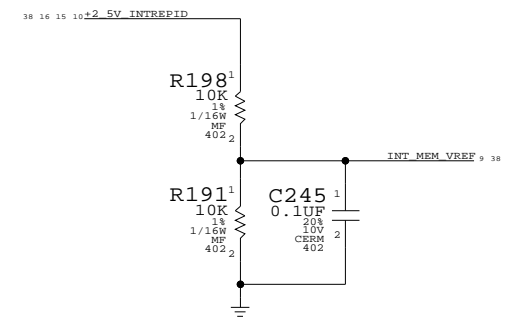
PINS ARE SWAPABLE FOR RPAKS

MEM_DATA<0>	AK32	DDR_DATA_0	DDR_A_0	H35	MEM_ADDR<0>
MEM_DATA<1>	AK33	DDR_DATA_1	DDR_A_1	G35	MEM_ADDR<1>
MEM_DATA<2>	AK31	DDR_DATA_2	DDR_A_2	G36	MEM_ADDR<2>
MEM_DATA<3>	AK35	DDR_DATA_3	DDR_A_3	F35	MEM_ADDR<3>
MEM_DATA<4>	AK36	DDR_DATA_4	DDR_A_4	F35	MEM_ADDR<4>
MEM_DATA<5>	AJ32	DDR_DATA_5	DDR_A_5	E35	MEM_ADDR<5>
MEM_DATA<6>	AJ35	DDR_DATA_6	DDR_A_6	E36	MEM_ADDR<6>
MEM_DATA<7>	AJ36	DDR_DATA_7	DDR_A_7	G32	MEM_ADDR<7>
MEM_DATA<8>	AG33	DDR_DATA_8	DDR_A_8	D36	MEM_ADDR<8>
MEM_DATA<9>	AG35	DDR_DATA_9	DDR_A_9	H36	MEM_ADDR<9>
MEM_DATA<10>	AH35	DDR_DATA_10	DDR_A_10	G33	MEM_ADDR<10>
MEM_DATA<11>	AG36	DDR_DATA_11	DDR_A_11	H33	MEM_ADDR<11>
MEM_DATA<12>	AH36	DDR_DATA_12	DDR_A_12	D35	MEM_ADDR<12>
MEM_DATA<13>	AH32	DDR_DATA_13	DDR_BA_0	L30	MEM_BA<0>
MEM_DATA<14>	AG32	DDR_DATA_14	DDR_BA_1	M29	MEM_BA<1>
MEM_DATA<15>	AG31	DDR_DATA_15	DDRCS_0	AN34	MEM_CS_L<0>
MEM_DATA<16>	AE32	DDR_DATA_16	DDRCS_1	AN36	MEM_CS_L<1>
MEM_DATA<17>	AF35	DDR_DATA_17	DDRCS_2	AL35	MEM_CS_L<2>
MEM_DATA<18>	AF36	DDR_DATA_18	DDRCS_3	AL33	MEM_CS_L<3>
MEM_DATA<19>	AE36	DDR_DATA_19	DDR_DQS_0	AJ31	MEM_DQS<0>
MEM_DATA<20>	AE35	DDR_DATA_20	DDR_DQS_1	AH31	MEM_DQS<1>
MEM_DATA<21>	AE33	DDR_DATA_21	DDR_DQS_2	AD32	MEM_DQS<2>
MEM_DATA<22>	AD36	DDR_DATA_22	DDR_DQS_3	AB30	MEM_DQS<3>
MEM_DATA<23>	AD35	DDR_DATA_23	DDR_DQS_4	V30	MEM_DQS<4>
MEM_DATA<24>	AA36	DDR_DATA_24	DDR_DQS_5	F32	MEM_DQS<5>
MEM_DATA<25>	AA35	DDR_DATA_25	DDR_DQS_6	M29	MEM_DQS<6>
MEM_DATA<26>	AA33	DDR_DATA_26	DDR_DQS_7	L32	MEM_DQS<7>
MEM_DATA<27>	AB36	DDR_DATA_27	DDR_DM_0	AJ33	MEM_DQM<0>
MEM_DATA<28>	AB35	DDR_DATA_28	DDR_DM_1	AH33	MEM_DQM<1>
MEM_DATA<29>	AC36	DDR_DATA_29	DDR_DM_2	AD33	MEM_DQM<2>
MEM_DATA<30>	AA32	DDR_DATA_30	DDR_DM_3	AC35	MEM_DQM<3>
MEM_DATA<31>	AB33	DDR_DATA_31	DDR_DM_4	F35	MEM_DQM<4>
MEM_DATA<32>	V36	DDR_DATA_32	DDR_DM_5	F33	MEM_DQM<5>
MEM_DATA<33>	U33	DDR_DATA_33	DDR_DM_6	F32	MEM_DQM<6>
MEM_DATA<34>	U32	DDR_DATA_34	DDR_DM_7	L33	MEM_DQM<7>
MEM_DATA<35>	V35	DDR_DATA_35	DDRRAS	L29	MEM_RAS_L
MEM_DATA<36>	T30	DDR_DATA_36	DDRCAS	H32	MEM_CAS_L
MEM_DATA<37>	U36	DDR_DATA_37	DDRWE	K30	MEM_WE_L
MEM_DATA<38>	U35	DDR_DATA_38	DDRCKE0	AN35	MEM_CKE<0>
MEM_DATA<39>	T36	DDR_DATA_39	DDRCKE1	AM35	MEM_CKE<1>
MEM_DATA<40>	F33	DDR_DATA_40	DDRCKE2	AM36	MEM_CKE<2>
MEM_DATA<41>	R30	DDR_DATA_41	DDRCKE3	AL36	MEM_CKE<3>
MEM_DATA<42>	F35	DDR_DATA_42	DDR_SELHI_0	AB32	MEM_MUXSEL_H<0>
MEM_DATA<43>	F36	DDR_DATA_43	DDR_SELHI_1	AE29	MEM_MUXSEL_H<1>
MEM_DATA<44>	R36	DDR_DATA_44	DDR_SELLO_0	N30	MEM_MUXSEL_L<0>
MEM_DATA<45>	R35	DDR_DATA_45	DDR_SELLO_1	T32	MEM_MUXSEL_L<1>
MEM_DATA<46>	R33	DDR_DATA_46	DDR_MCLK_0_P	Y32	SYSLCK_DDRCLK_A0_UF
MEM_DATA<47>	R32	DDR_DATA_47	DDR_MCLK_0_N	Y33	SYSLCK_DDRCLK_A0_L_UF
MEM_DATA<48>	N35	DDR_DATA_48	DDR_MCLK_1_P	Y35	SYSLCK_DDRCLK_A1_UF
MEM_DATA<49>	M36	DDR_DATA_49	DDR_MCLK_1_N	Y36	SYSLCK_DDRCLK_A1_L_UF
MEM_DATA<50>	L35	DDR_DATA_50	DDR_MCLK_2_P	Y30	INT_DDRCLK2_P_TP
MEM_DATA<51>	M35	DDR_DATA_51	DDR_MCLK_2_N	Y30	INT_DDRCLK2_N_TP
MEM_DATA<52>	M33	DDR_DATA_52	DDR_MCLK_3_P	W32	SYSLCK_DDRCLK_B0_UF
MEM_DATA<53>	L36	DDR_DATA_53	DDR_MCLK_3_N	W33	SYSLCK_DDRCLK_B0_L_UF
MEM_DATA<54>	N33	DDR_DATA_54	DDR_MCLK_4_P	Y32	SYSLCK_DDRCLK_B1_UF
MEM_DATA<55>	M30	DDR_DATA_55	DDR_MCLK_4_N	Y35	SYSLCK_DDRCLK_B1_L_UF
MEM_DATA<56>	J32	DDR_DATA_56	DDR_MCLK_5_P	W35	INT_DDRCLK5_P_TP
MEM_DATA<57>	J33	DDR_DATA_57	DDR_MCLK_5_N	W36	INT_DDRCLK5_N_TP
MEM_DATA<58>	J35	DDR_DATA_58	DDR_REF	AA22	INT_MEM_REF_H
MEM_DATA<59>	K32	DDR_DATA_59	DDR_VREF_0	Y22	INT_MEM_VREF
MEM_DATA<60>	K33	DDR_DATA_60	DDR_VREF_1	T22	
MEM_DATA<61>	J36	DDR_DATA_61			
MEM_DATA<62>	K36	DDR_DATA_62			
MEM_DATA<63>	K35	DDR_DATA_63			

CRITICAL
U45
INTREPID-REV2.1
BSA
(2 OF 9)

DDR MEMORY INTERFACE

MEM_VREF



CLOCKS

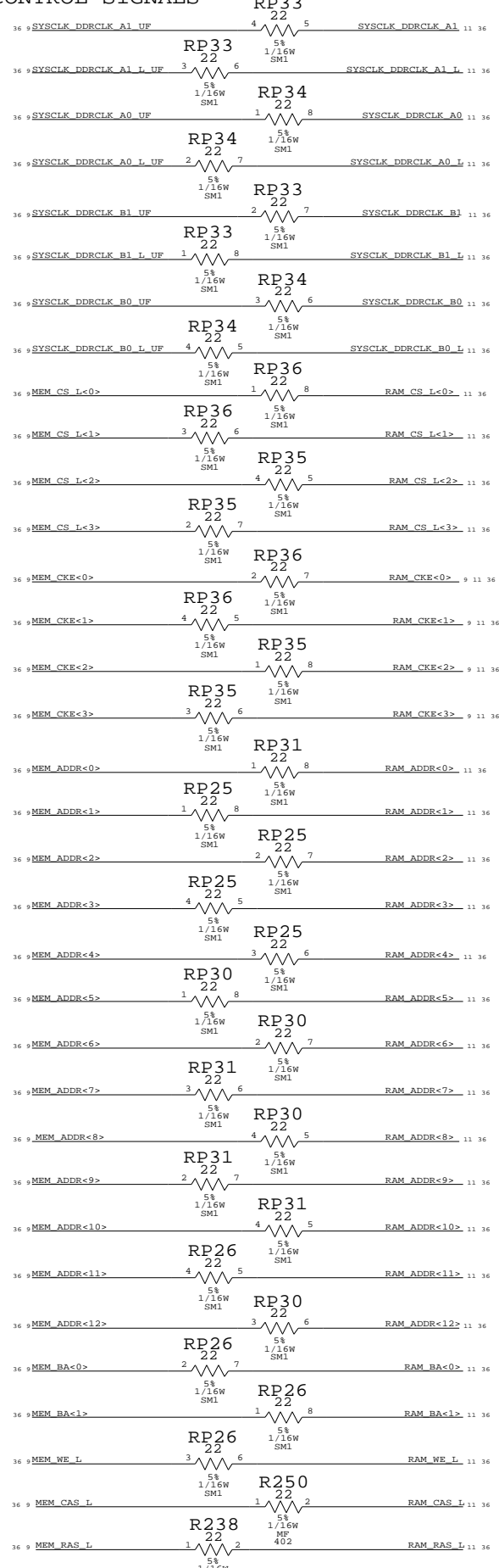
CS

CKE

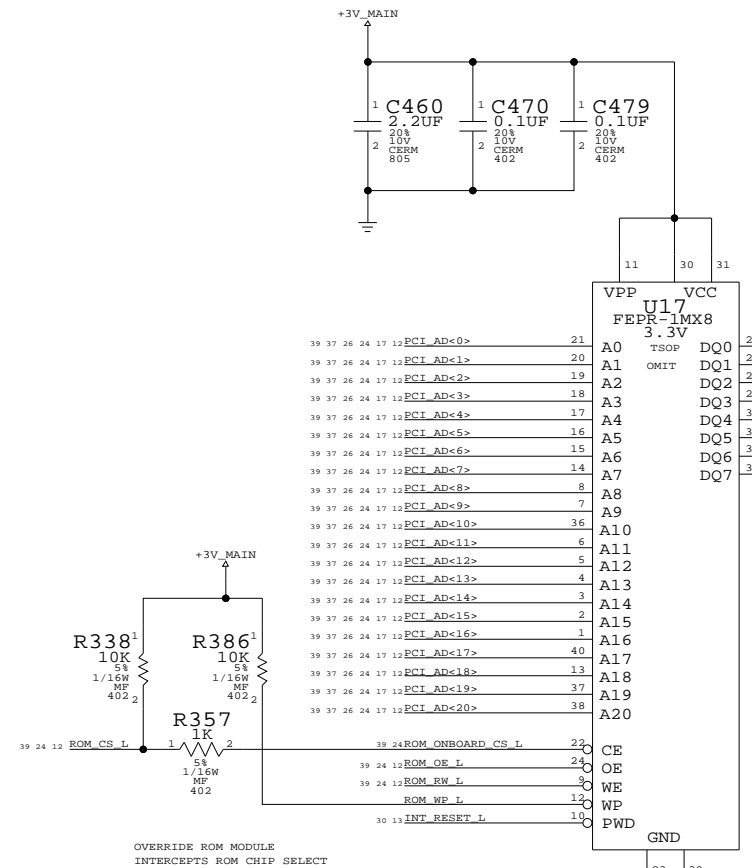
ADDR

BA

CNTL



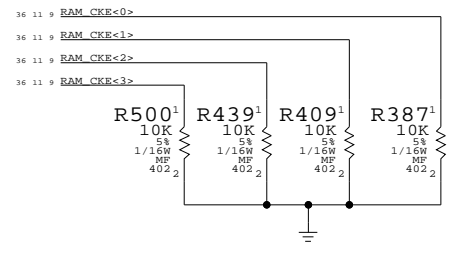
1MB BOOT ROM



OVERVERRIDE ROM MODULE INTERCEPTS ROM CHIP SELECT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1336	1	BOOTROM,P84	U17	CRITICAL	?

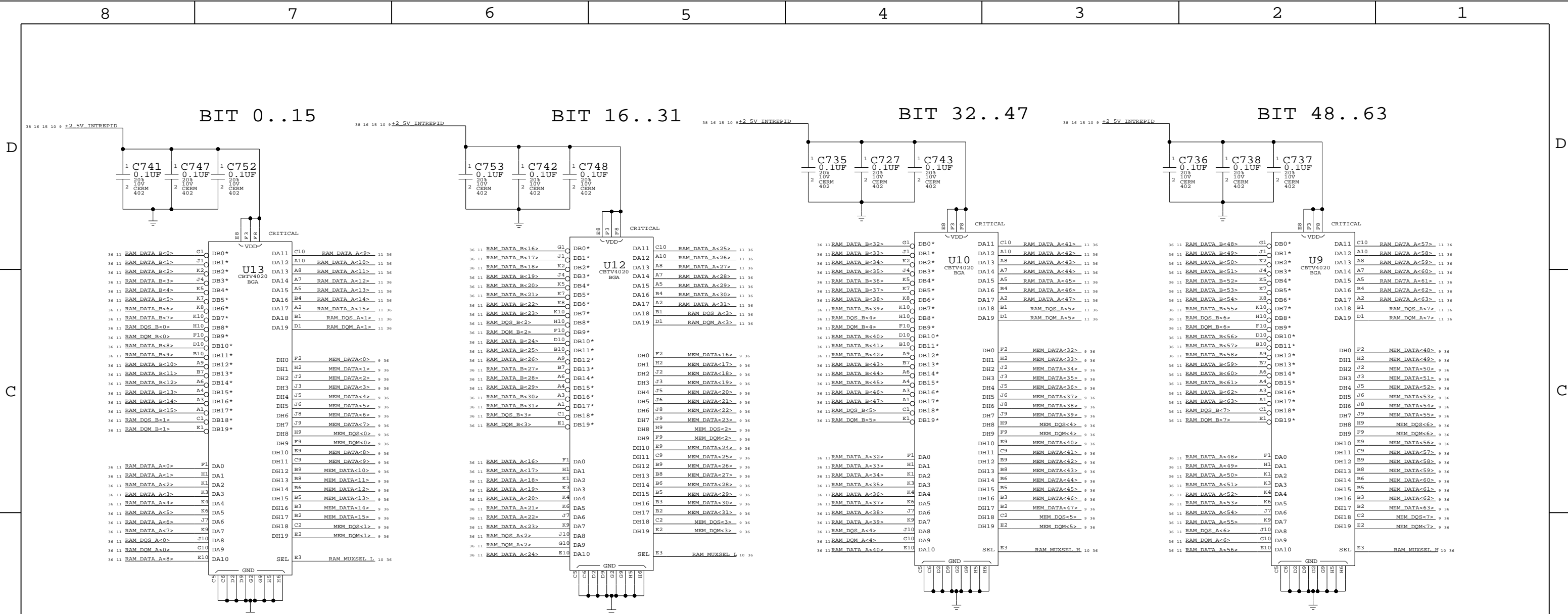
PULL-DOWN RESISTORS TO ENSURE CKE STAYS LOW AFTER INTREPID 2.5V I/O SHUTS OFF



INT - DDR/BOOTROM

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APPLE COMPUTER INC.	SCALE	DRAWING NUMBER	REV.
	NONE	D 051-6531	B
		SHEET	OF
		9	44



SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
 SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND
 MEM_MUXSEL_H<0> AND MEM_MUXSEL_L<0> ARE ACTIVE LOW
 MEM_MUXSEL_H<1> AND MEM_MUXSEL_L<1> ARE ACTIVE HIGH

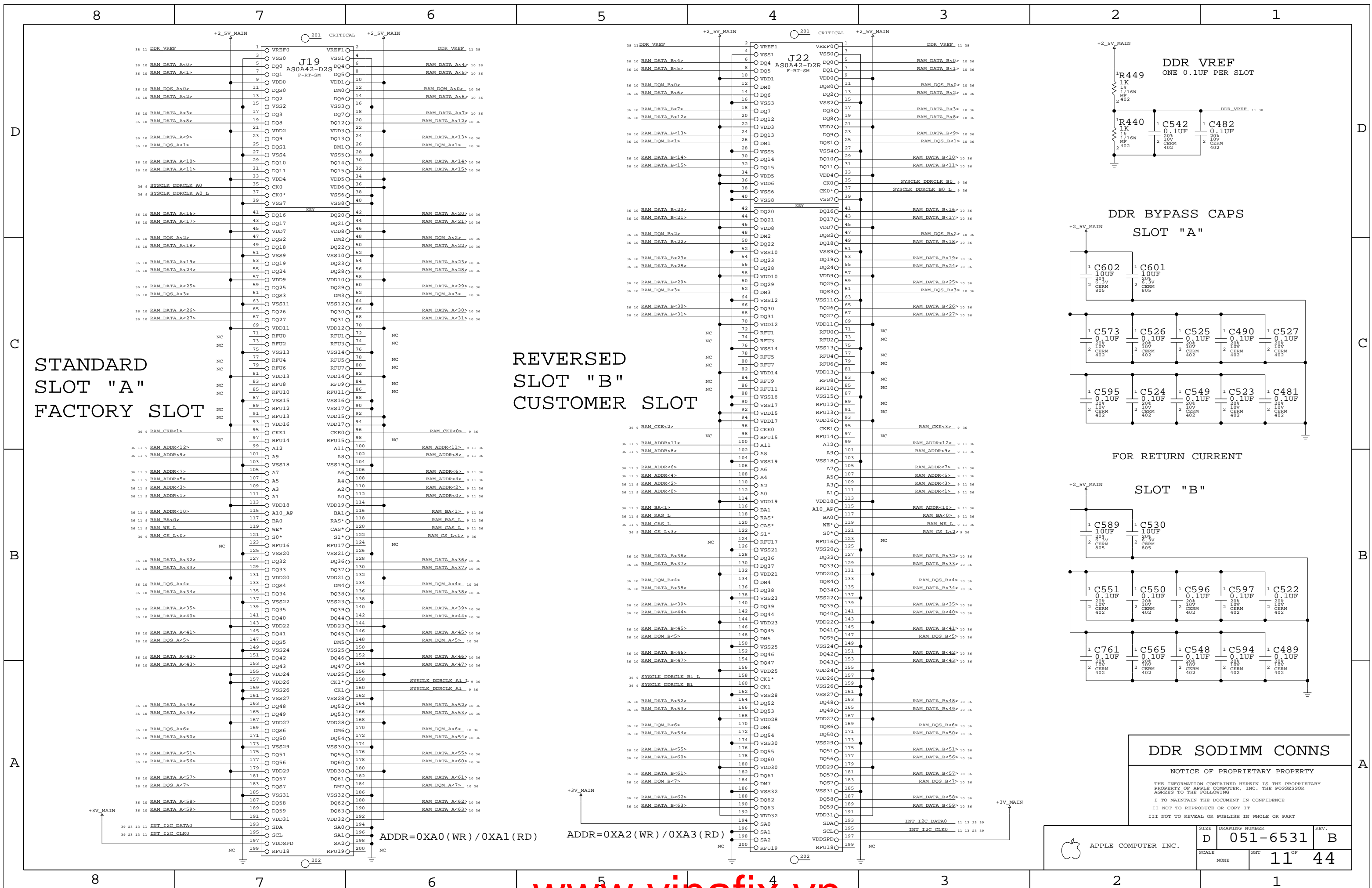
ADDED 0 OHM RESISTORS IN CASE POLARITY IS WRONG



16BIT 2:1 DDR MUXES

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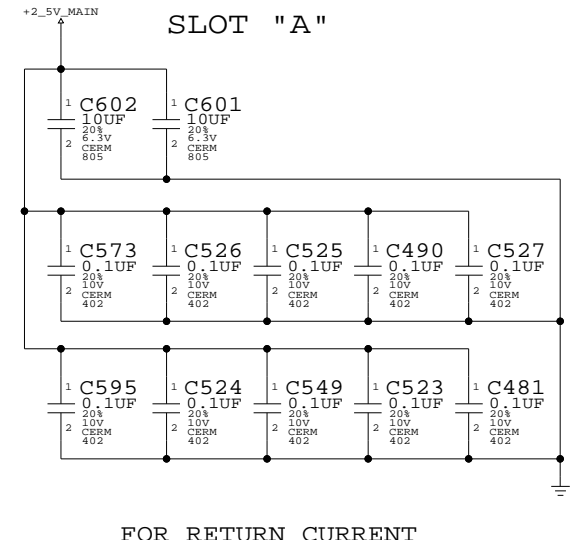
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6531	B
SCALE	SHT	10 ^{OF} 44	
NONE			



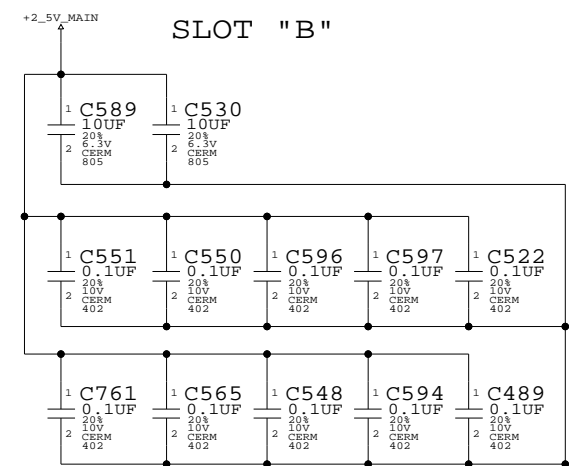
STANDARD
SLOT "A"
FACTORY SLOT

REVERSED
SLOT "B"
CUSTOMER SLOT

DDR BYPASS CAPS
SLOT "A"



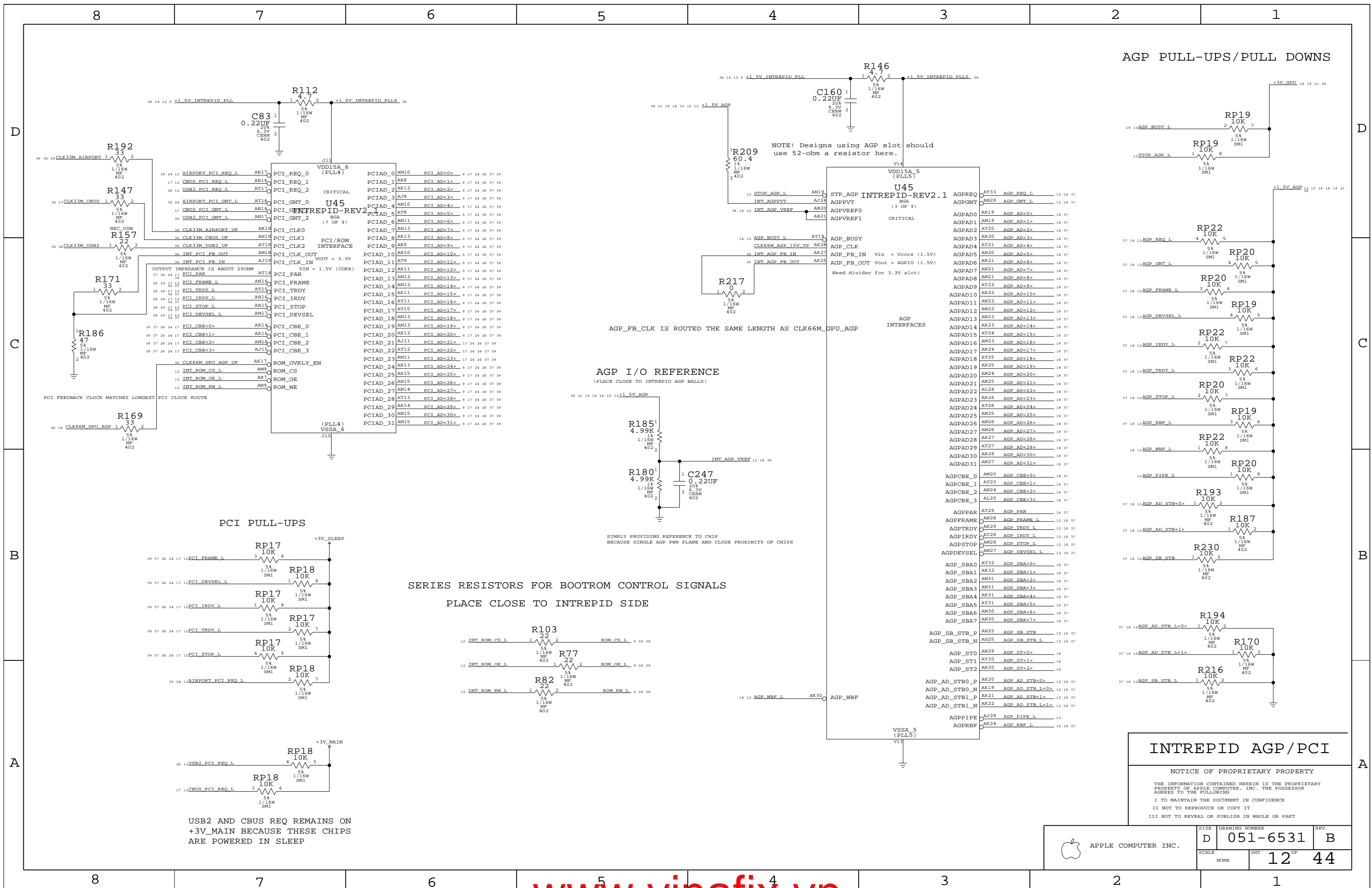
FOR RETURN CURRENT



DDR SODIMM CONNS

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6531	B
SCALE	SHT	11 OF 44	
NONE			



AGP PULL-UPS/PULL DOWNS

PCI PULL-UPS

AGP I/O REFERENCE
(PLACE CLOSE TO INTREPID AGP BALLS)

SERIES RESISTORS FOR BOOTROM CONTROL SIGNALS
PLACE CLOSE TO INTREPID SIDE

INTREPID AGP/PCI

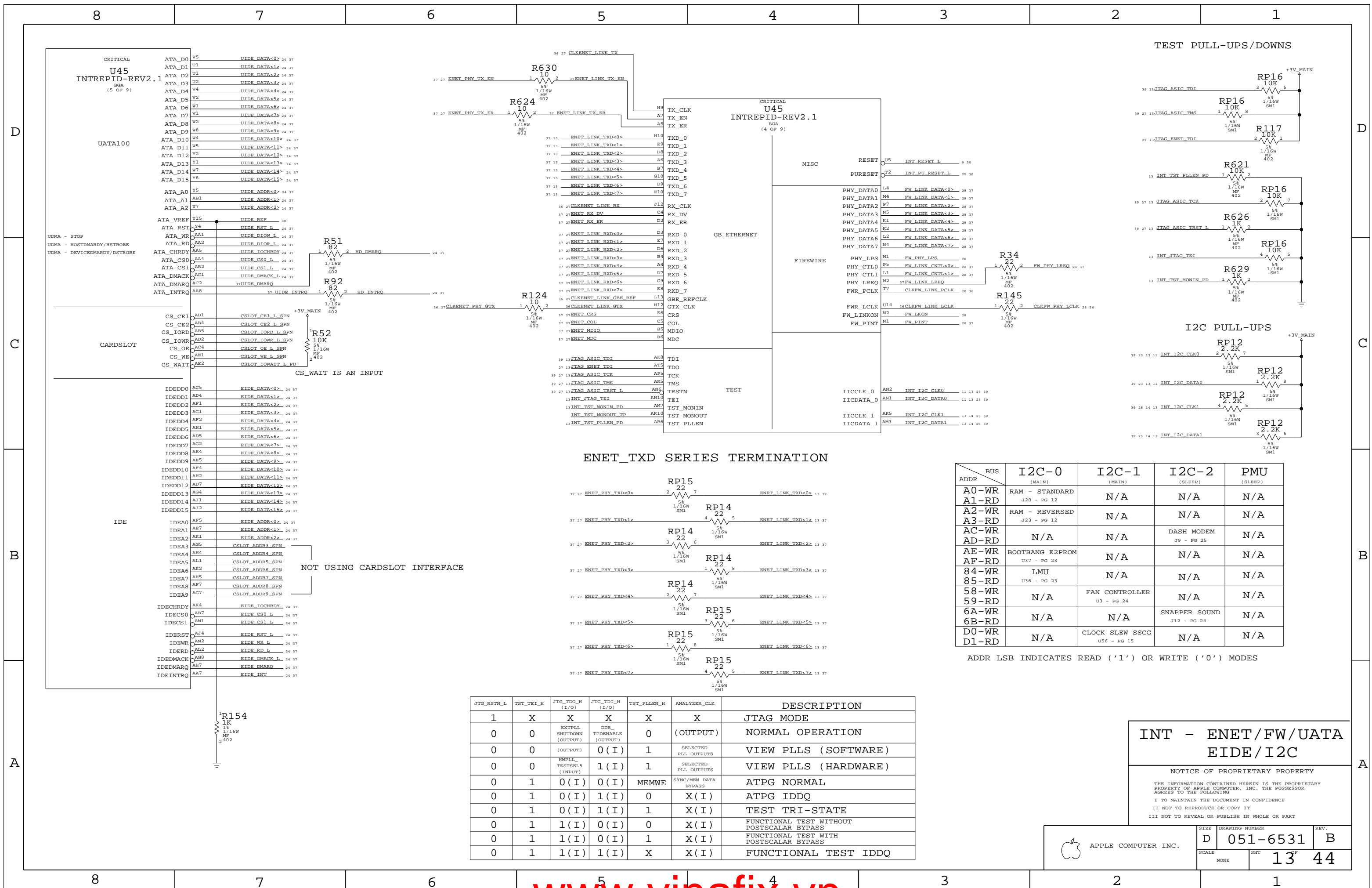
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USB2 AND CBUS REQ REMAINS ON +3V_MAIN BECAUSE THESE CHIPS ARE POWERED IN SLEEP

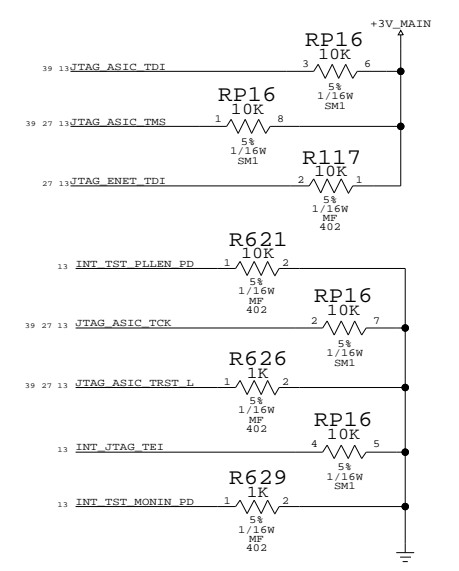
NOTE: Designs using AGP slot should use 52-ohm a resistor here.

SIMPLY PROVIDING REFERENCE TO CHIP BECAUSE SINGLE AGP PWR PLANE AND CLOSE PROXIMITY OF CHIPS

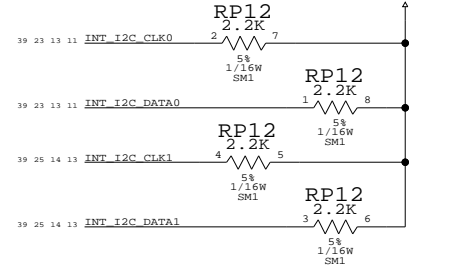
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6531	B
SCALE	NONE	SHT	12 OF 44



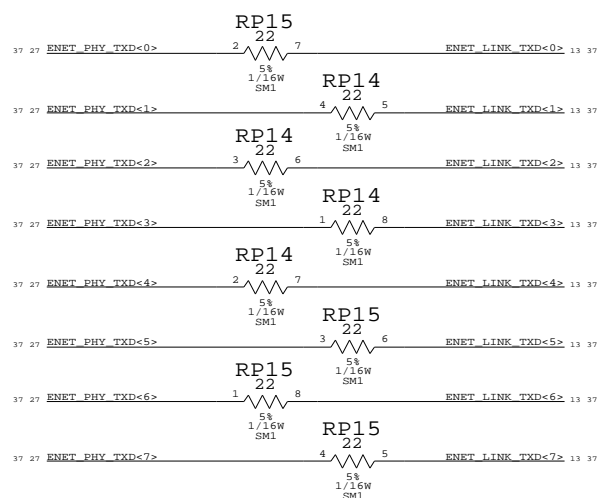
TEST PULL-UPS/DOWNS



I2C PULL-UPS



ENET_TXD SERIES TERMINATION



NOT USING CARDSLOT INTERFACE

BUS	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
A0-WR	RAM - STANDARD J20 - PG 12	N/A	N/A	N/A
A1-RD				
A2-WR	RAM - REVERSED J23 - PG 12	N/A	N/A	N/A
A3-RD				
AC-WR			DASH MODEM J9 - PG 25	N/A
AD-RD	N/A	N/A		
AE-WR	BOOTBANG E2PROM U37 - PG 23	N/A	N/A	N/A
AF-RD				
84-WR	LMU U36 - PG 23	N/A	N/A	N/A
85-RD				
58-WR	N/A	FAN CONTROLLER U3 - PG 24	N/A	N/A
59-RD				
6A-WR	N/A	N/A	SNAPPER SOUND J12 - PG 24	N/A
6B-RD				
D0-WR	N/A	CLOCK SLEW SSCG U56 - PG 15	N/A	N/A
D1-RD				

ADDR LSB INDICATES READ ('1') OR WRITE ('0') MODES

JTG_RSTN_L	TST_TEI_H	JTG_TDO_H (I/O)	JTG_TDI_H (I/O)	TST_PLLN_H	ANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	EXTPLL SHUTDOWN (OUTPUT)	DDR_TPDENABLE (OUTPUT)	0	(OUTPUT)	NORMAL OPERATION
0	0	(OUTPUT)	0(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	HWPLL_TESTSEL5 (INPUT)	1(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0(I)	0(I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0(I)	1(I)	0	X(I)	ATPG IDDQ
0	1	0(I)	1(I)	1	X(I)	TEST TRI-STATE
0	1	1(I)	0(I)	0	X(I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1(I)	0(I)	1	X(I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1(I)	1(I)	X	X(I)	FUNCTIONAL TEST IDDQ

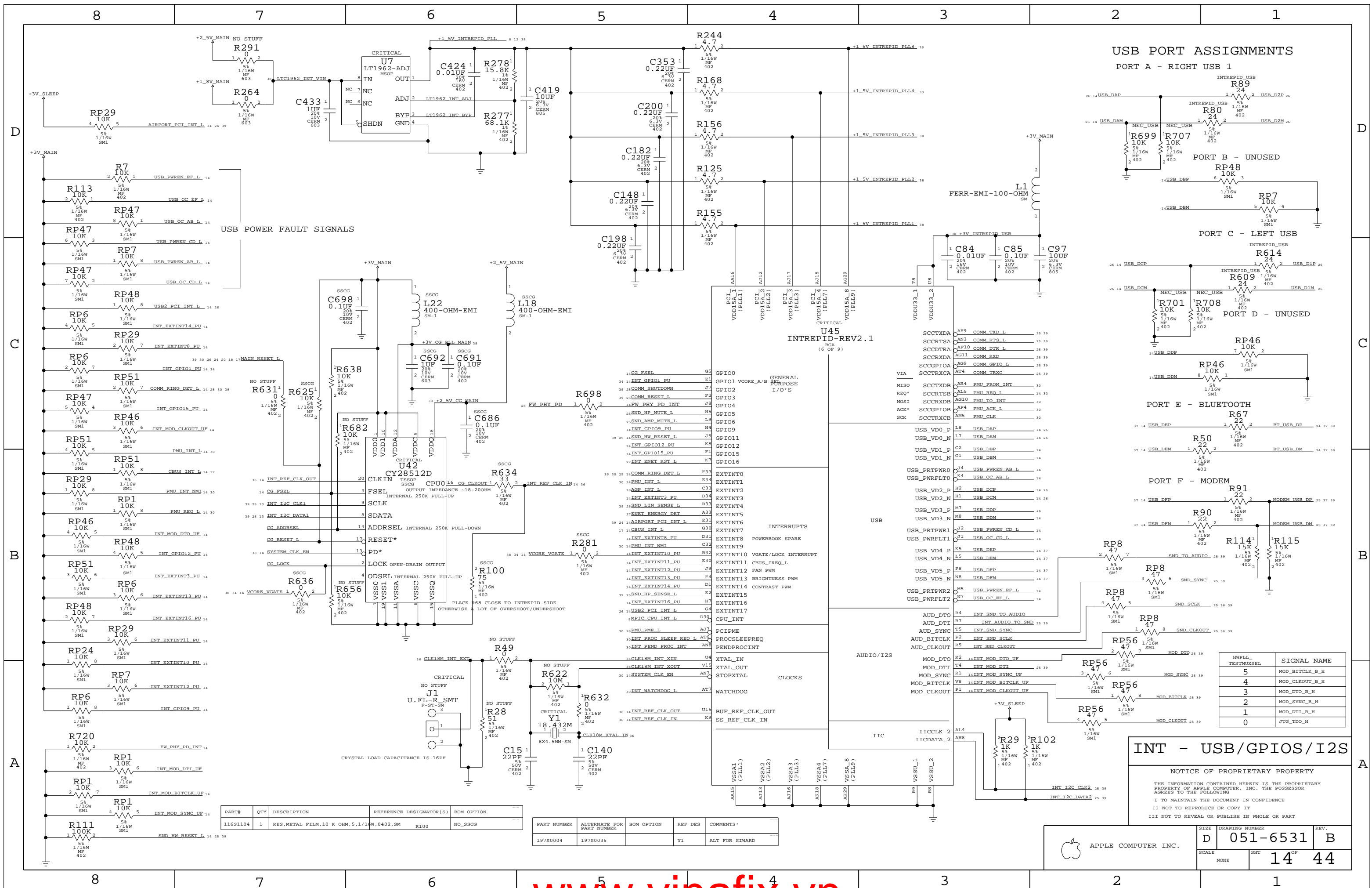
INT - ENET/FW/UATA EIDE/I2C

NOTICE OF PROPRIETARY PROPERTY

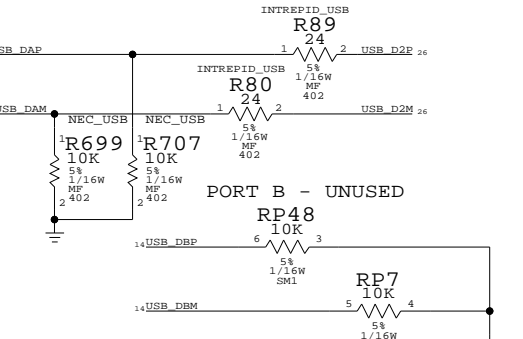
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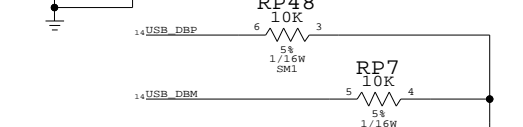
SIZE	D	DRAWING NUMBER	051-6531	REV.	B
SCALE	NONE	SHT	13		44



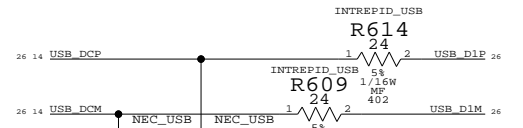
USB PORT ASSIGNMENTS
PORT A - RIGHT USB 1



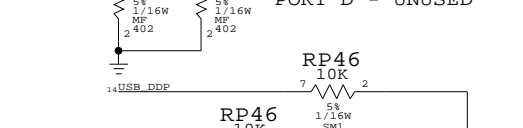
PORT B - UNUSED



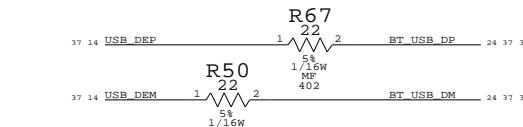
PORT C - LEFT USB



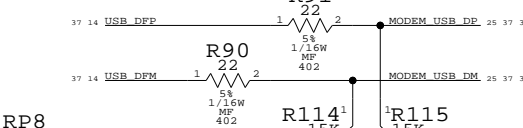
PORT D - UNUSED



PORT E - BLUETOOTH



PORT F - MODEM

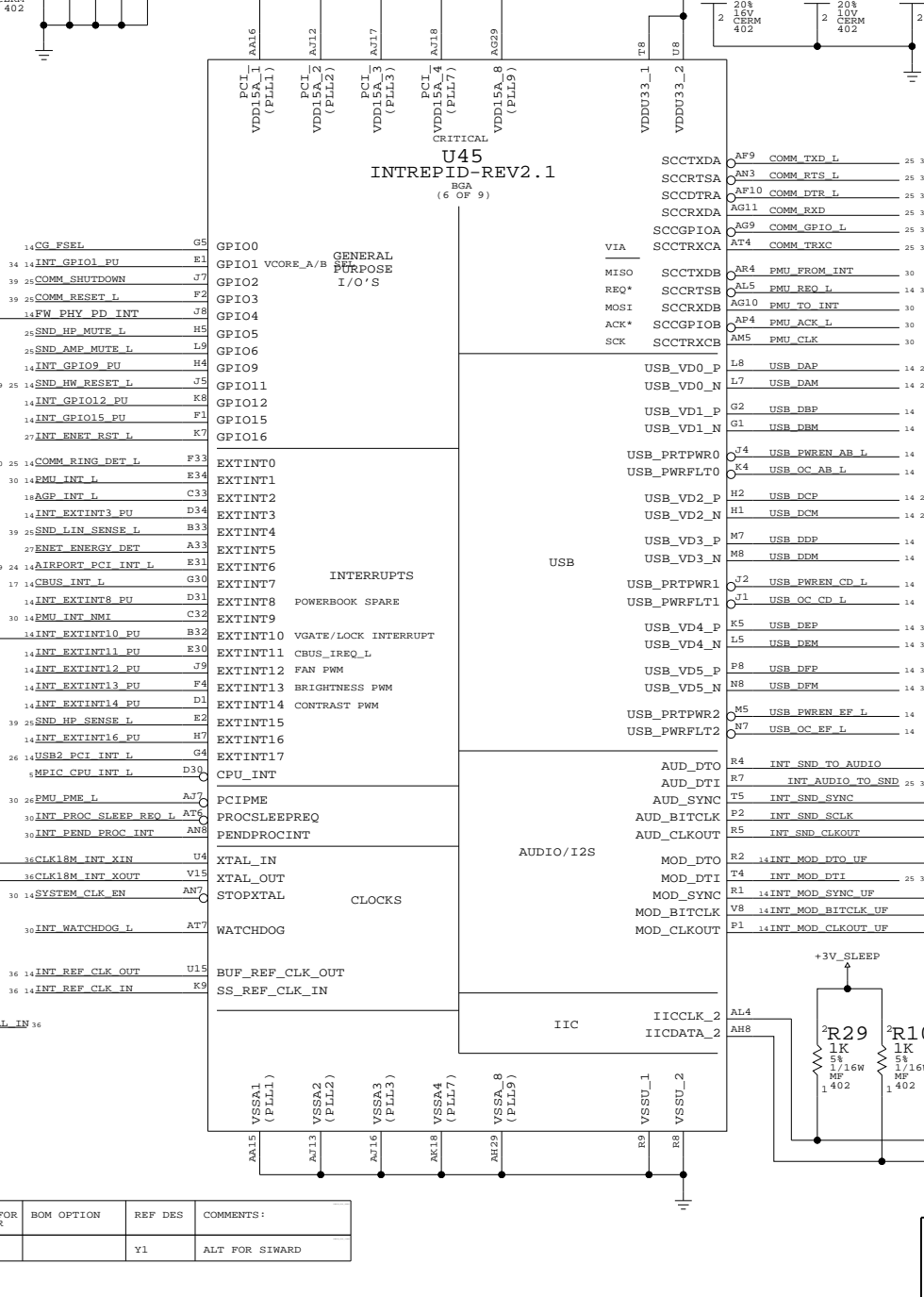
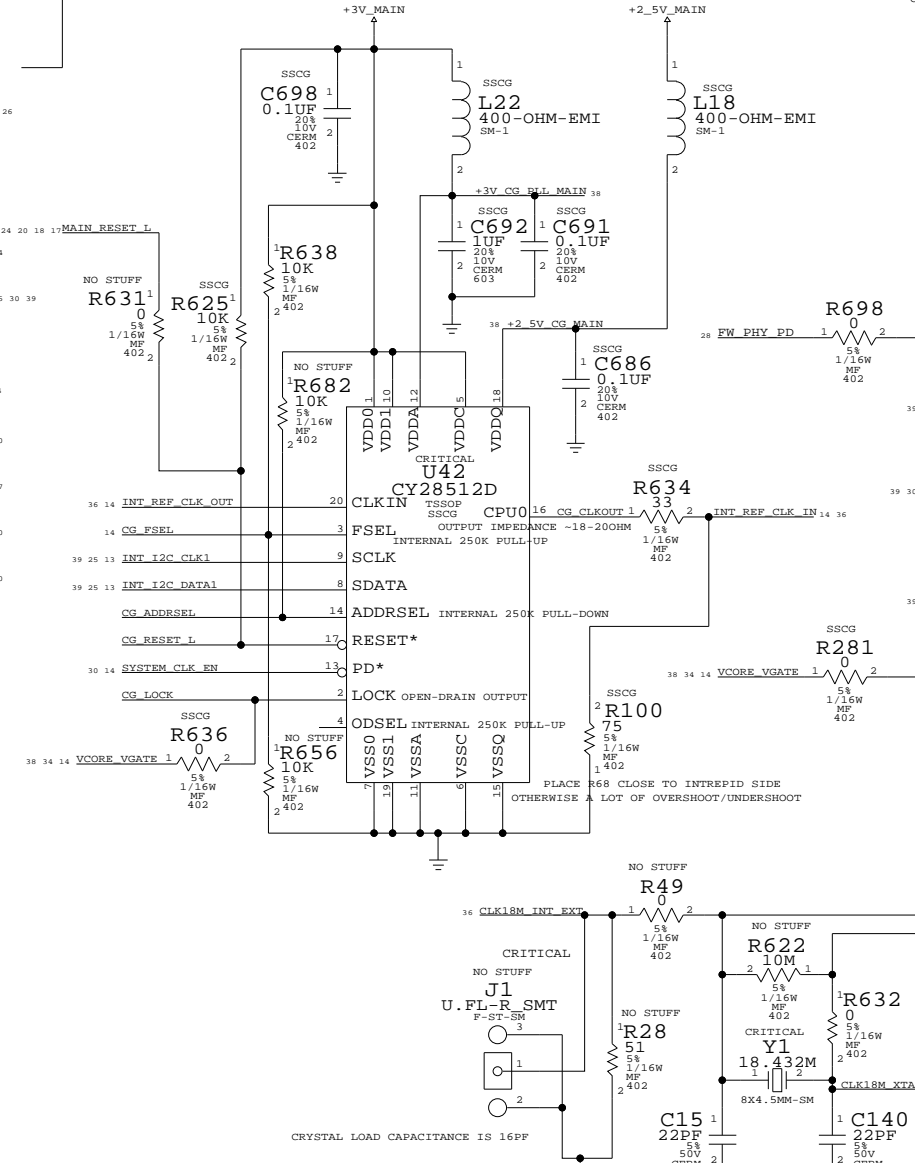
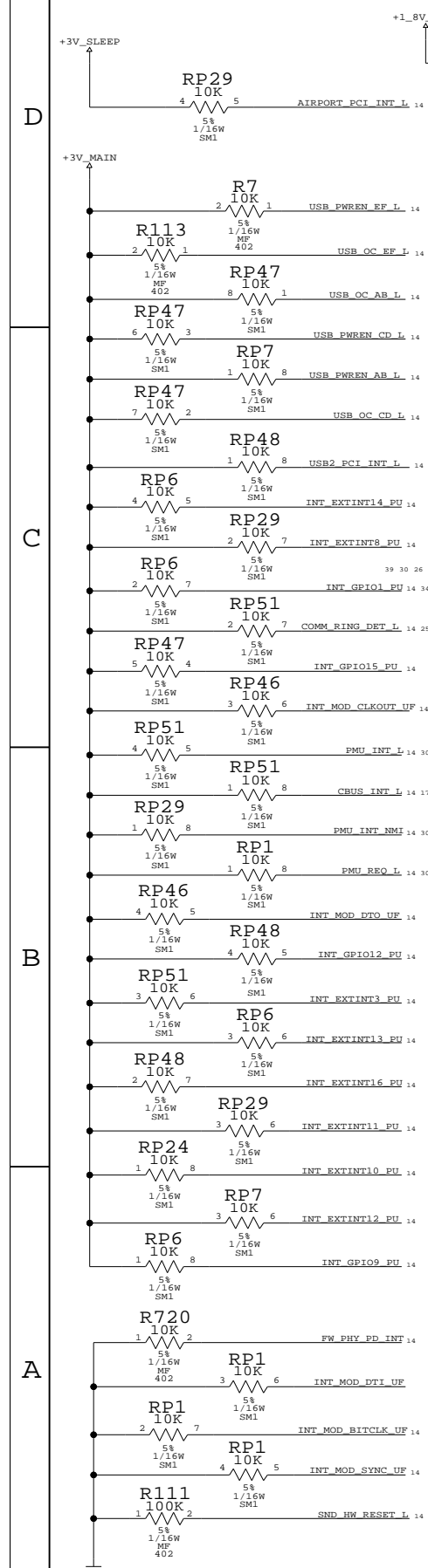


HWPLL TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

INT - USB/GPIOS/I2S

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USB POWER FAULT SIGNALS

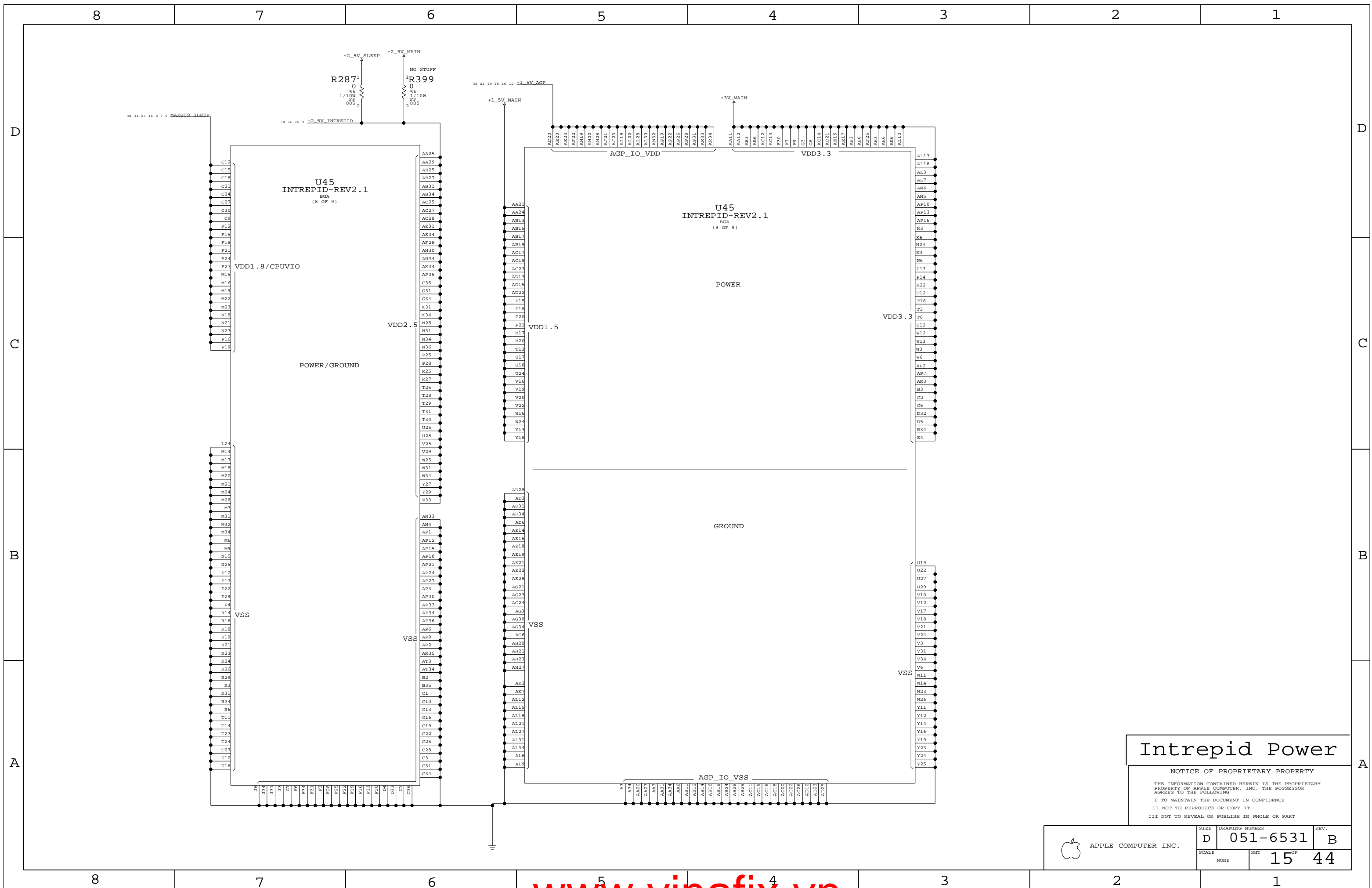


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES, METAL FILM, 10 K OHM, 5, 1/16W, 0402, SM	R100	NO_SSCG

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0004	197S0035		Y1	ALT FOR SIWARD

APPLE COMPUTER INC.

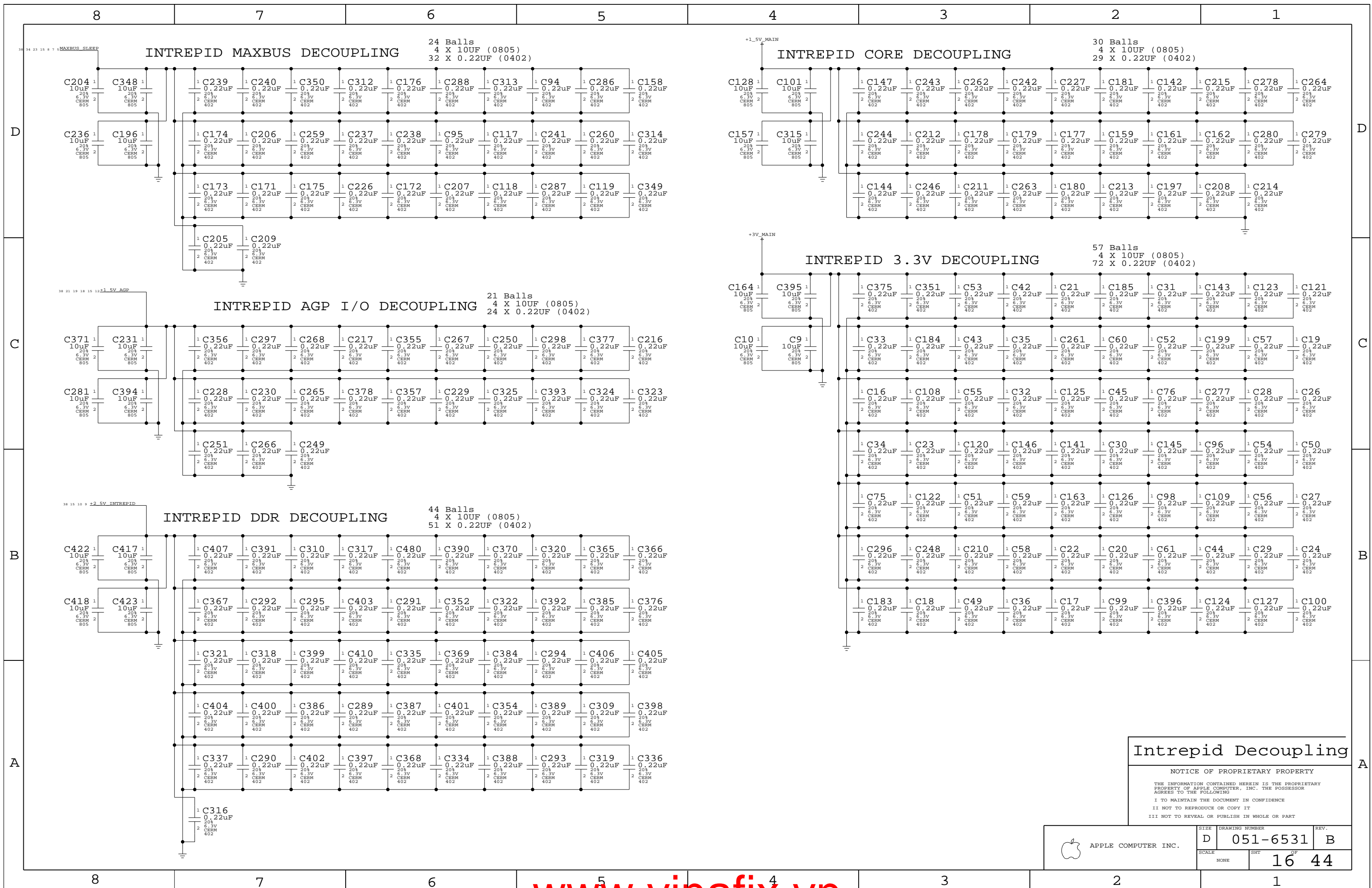
SIZE	D	DRAWING NUMBER	051-6531	REV.	B
SCALE	NONE	SHT	14	OF	44



Intrepid Power

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	NONE	15 OF 44	B



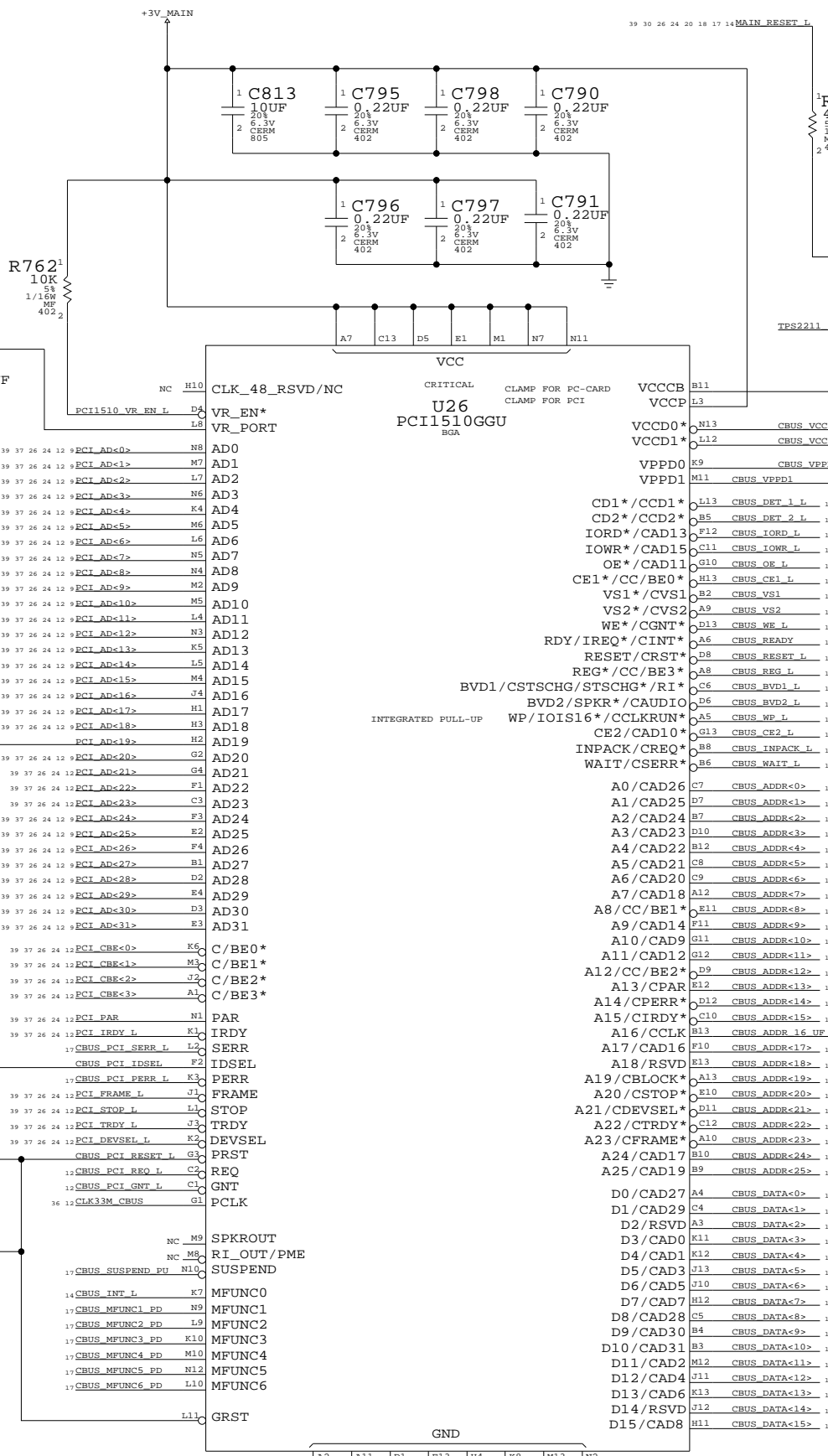
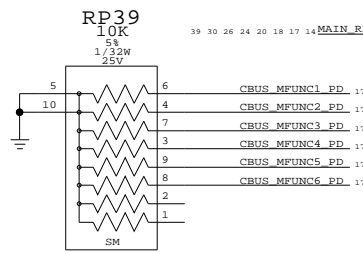
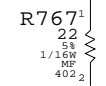
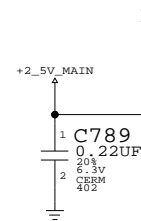
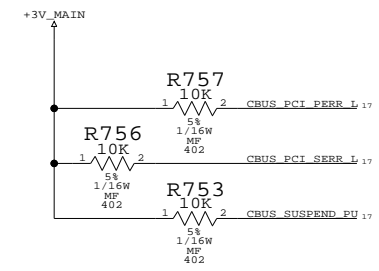
Intrepid Decoupling

NOTICE OF PROPRIETARY PROPERTY

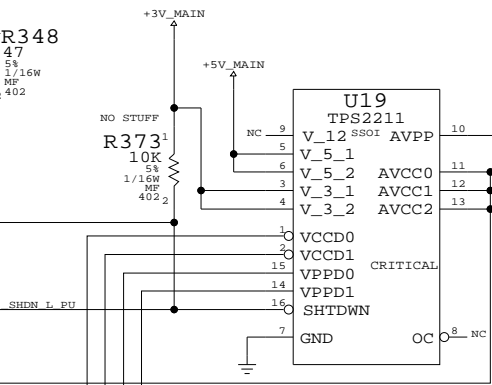
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6531	B
SCALE	NONE	SHT	OF
		16	44

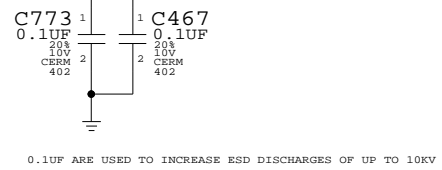
PCI1510 PULL-UPS



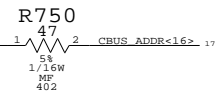
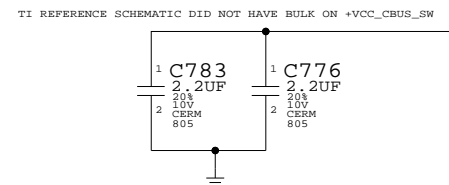
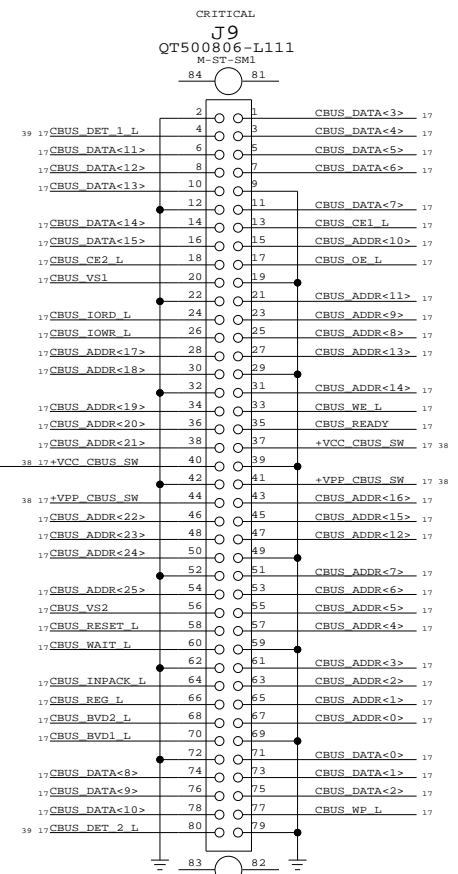
THIS PROPERLY SHUTS DOWN CARDBUS POWER FOR PSUEDO-D3COLD



MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES TO MINIMIZE INDUCTANCE!



PC CARD/CARDBUS CONNECTOR



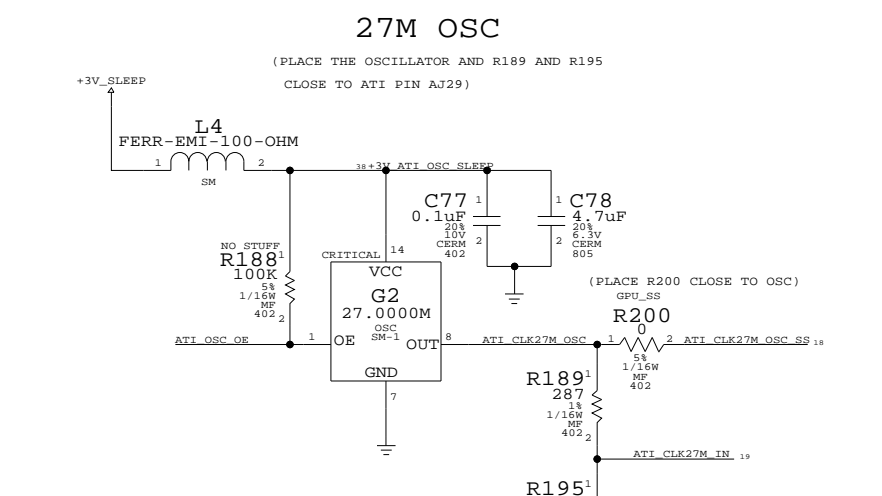
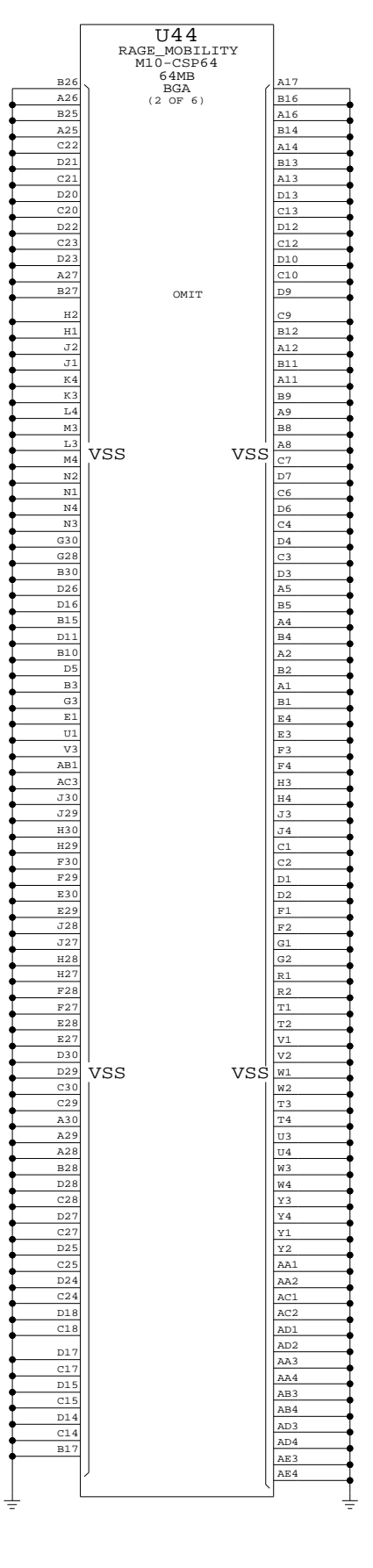
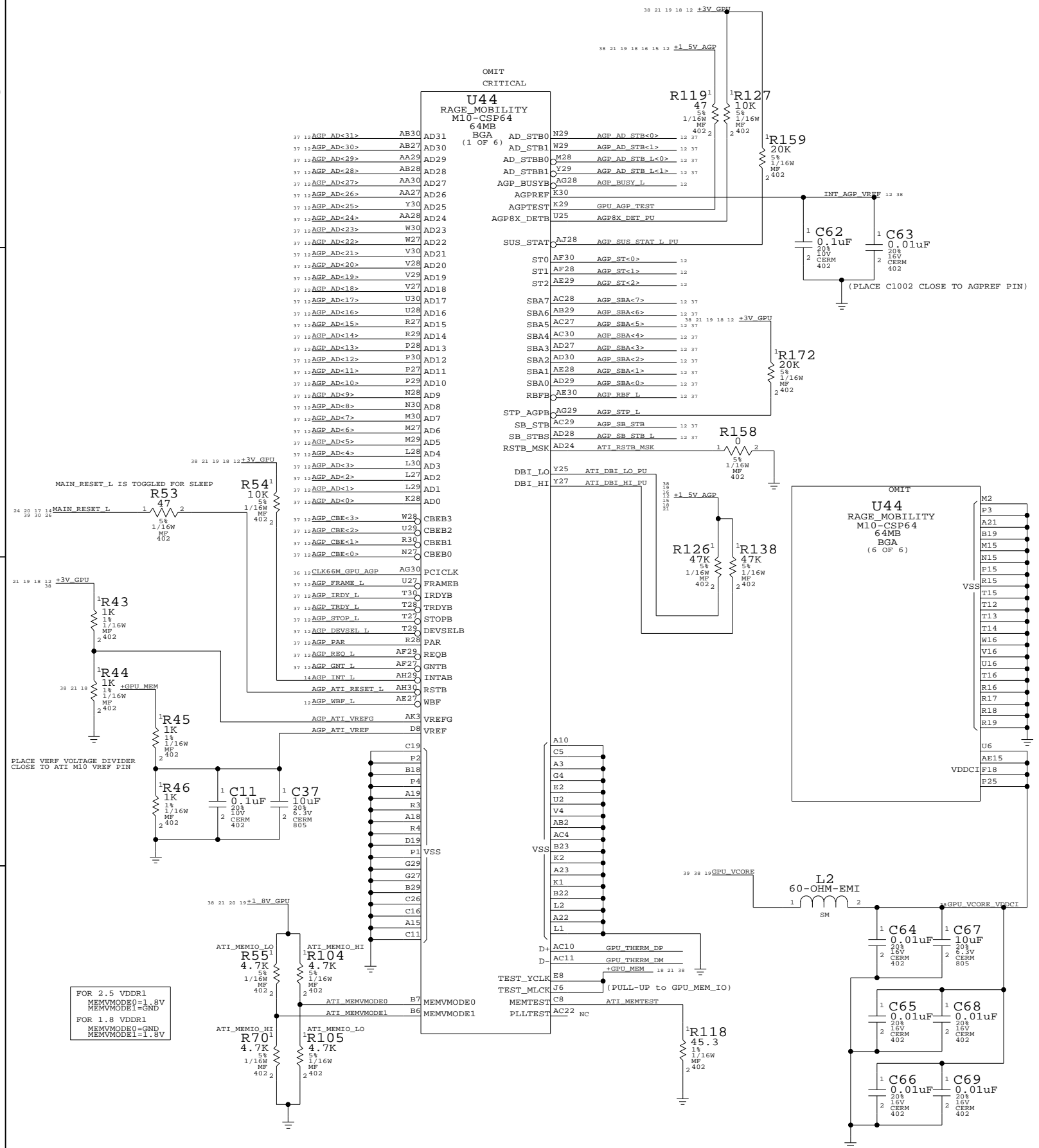
CARDBUS
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6531	B
SCALE	NONE	SHT	17 44

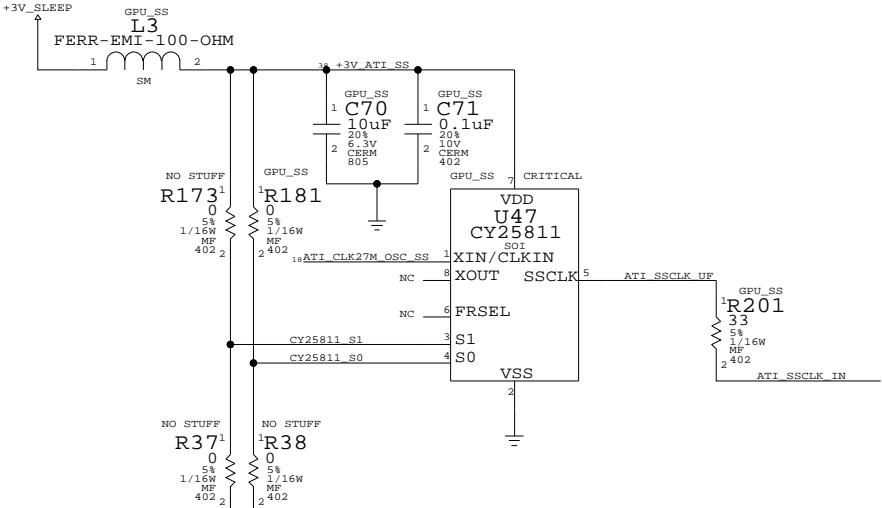
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0133	1	IC,ATI,M10,NO HEATSPREADER	U44	CRITICAL	7

D
C
B
A

D
C
B
A



S0=S1=M => -1.5% DOWN-SPREAD
SPREAD SPECTRUM SUPPORT



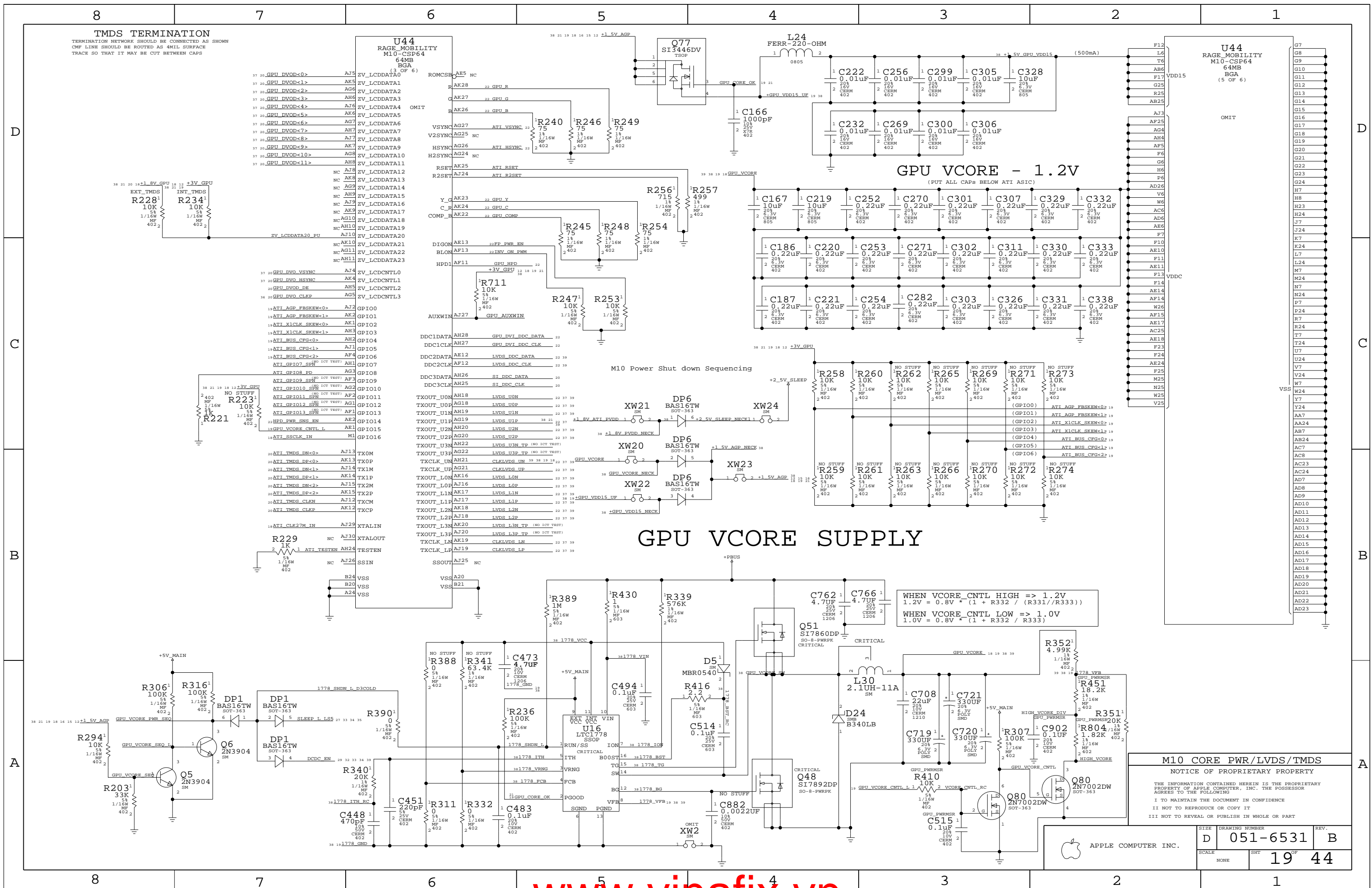
M10 AGP INTERFACE

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6531	B
SCALE	SHT	18 OF 44	
NONE			



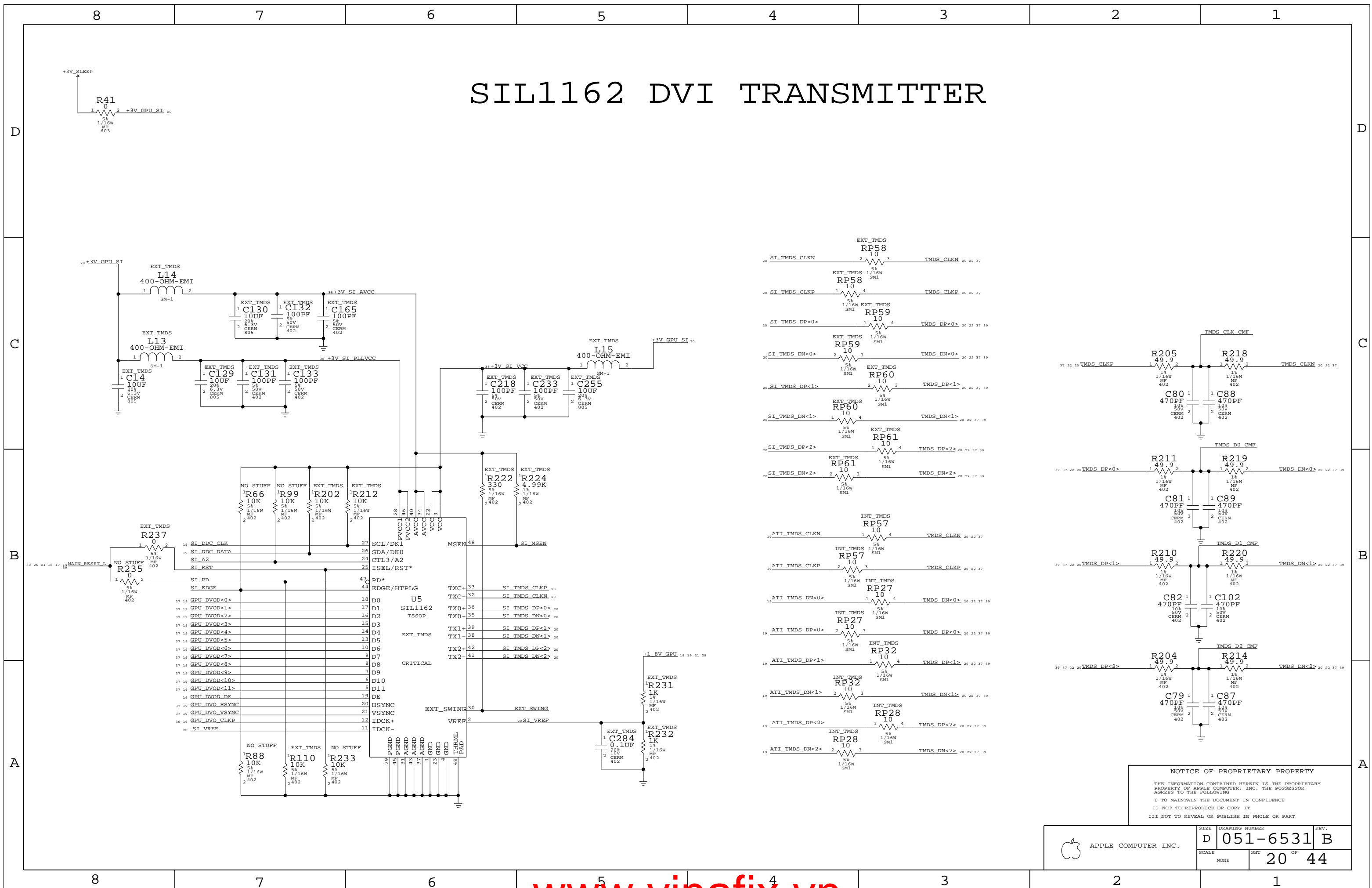
M10 CORE PWR/LVDS/TMDS
 NOTICE OF PROPRIETARY PROPERTY
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SIZE	DRAWING NUMBER	REV.
D	051-6531	B
SCALE	SHT	19 OF 44
NONE		



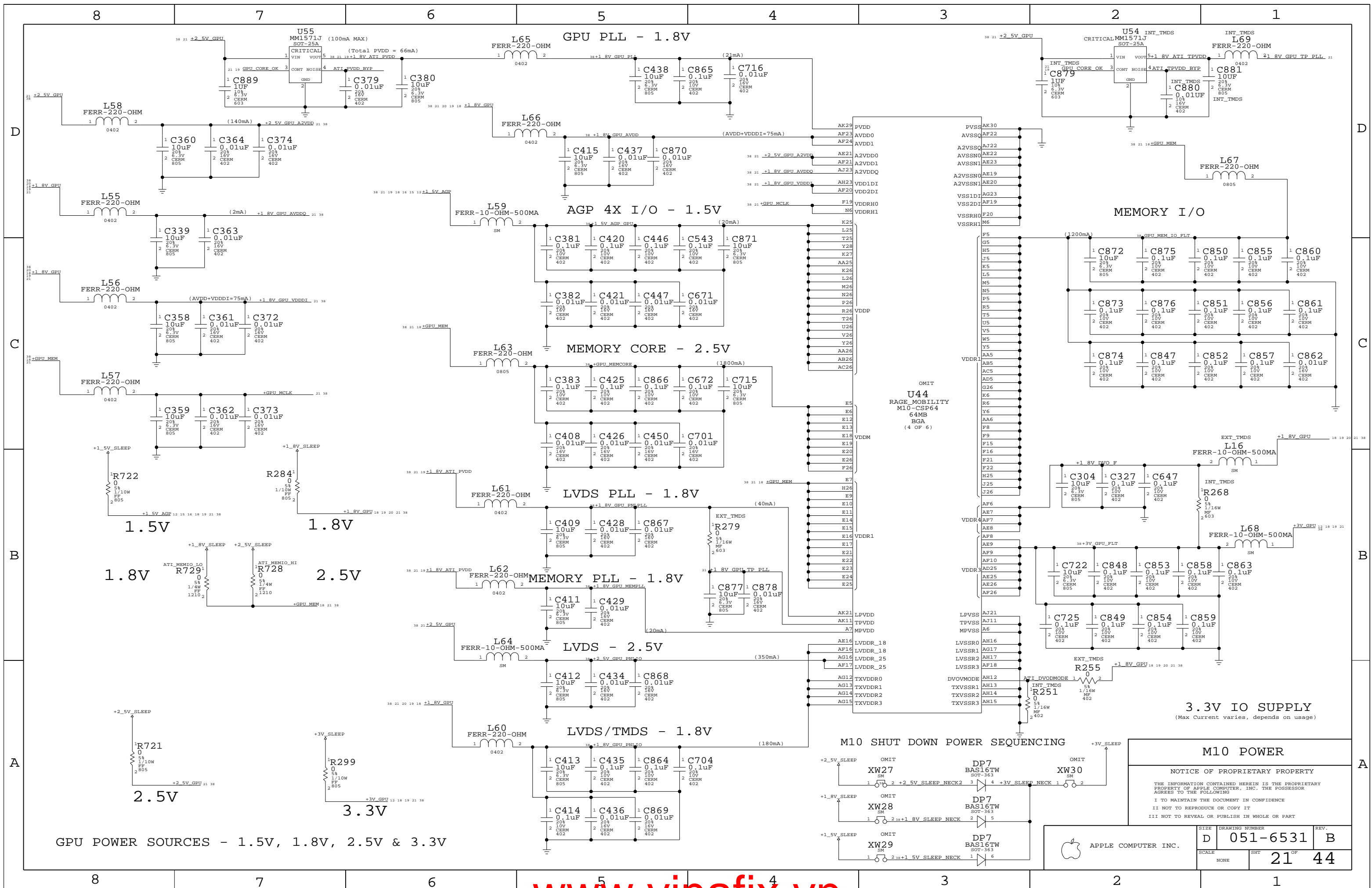
APPLE COMPUTER INC.

SIL1162 DVI TRANSMITTER



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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	NONE	051-6531	B
SCALE		SHT 20 OF 44	



GPU POWER SOURCES - 1.5V, 1.8V, 2.5V & 3.3V

3.3V IO SUPPLY
(Max Current varies, depends on usage)

M10 POWER

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SIZE	DRAWING NUMBER	REV.
D	051-6531	B
SCALE	SHT	21 OF 44
NONE		

ANALOG FILTERING PLACE CLOSE TO CONNECTOR

EXTERNAL VIDEO (DVI) INTERFACE

Power key detect path when system is shutdown or asleep... DDC_CLK is isolated from NV17M during SHUTDOWN. WHEN power key on remote device is pressed, 5V will be driven into DDC_CLK. Since host rails will be low, TP0610 will turn on, driving SOFT_PWR_ON low. As host rails rise, TP0610 will turn off, as will remote device path into DDC_CLK. Isolation will be disabled as well.

DVI POWER SWITCH

D

D

C

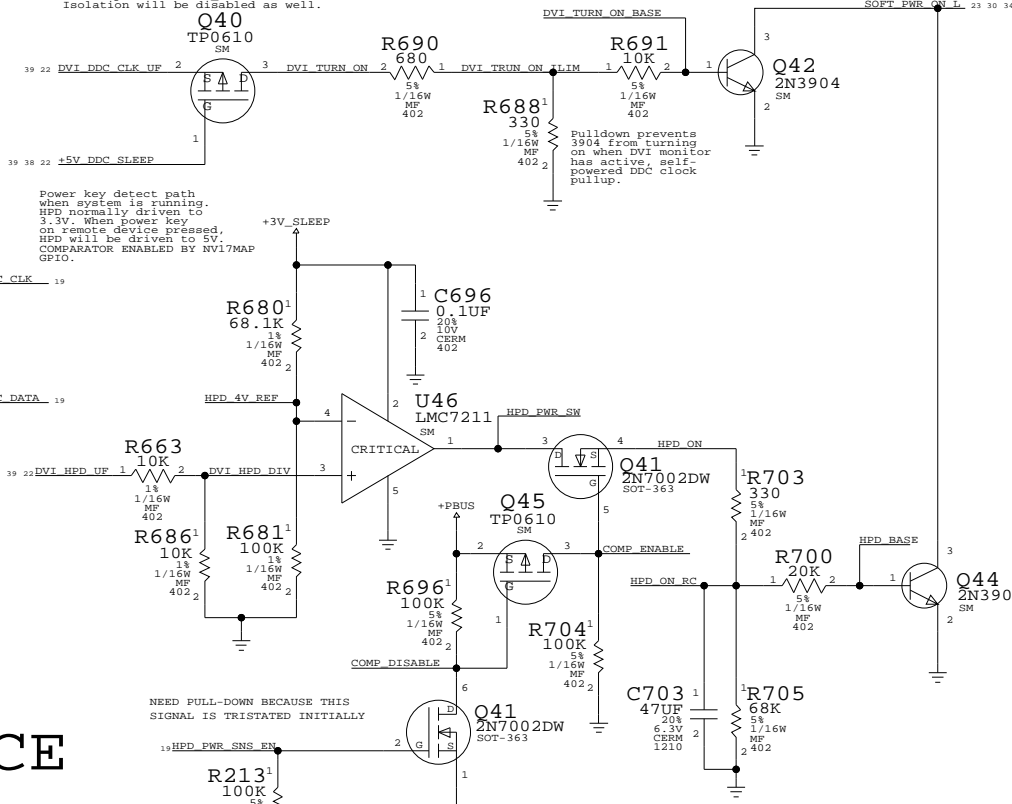
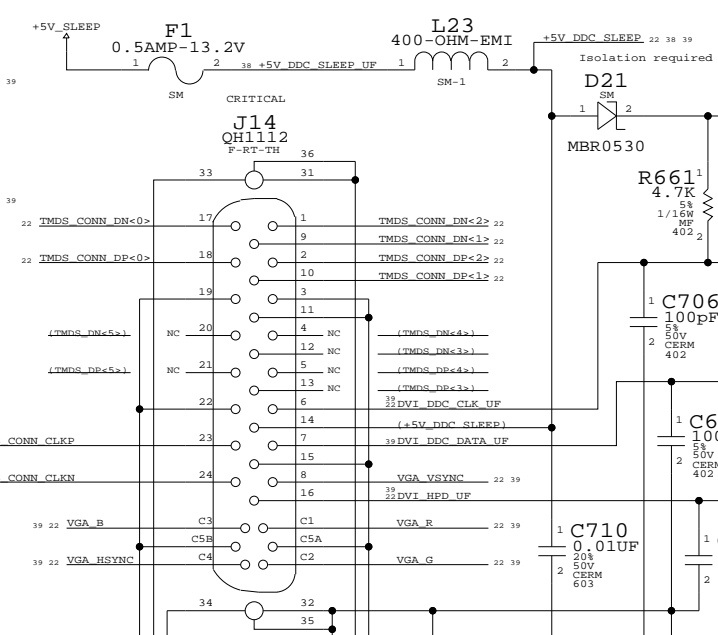
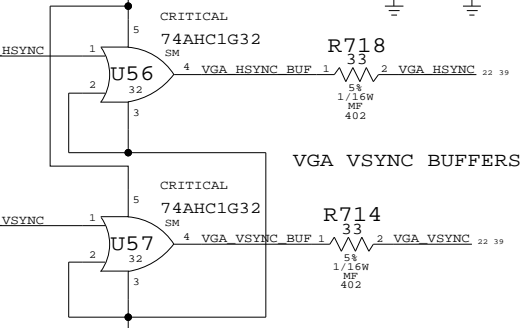
C

B

B

A

A

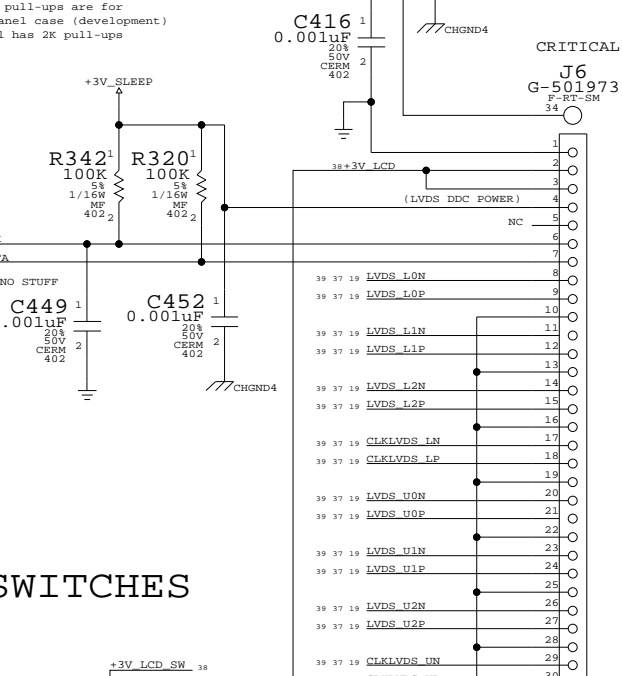


TMSD FILTERING PLACE CLOSE TO CONNECTOR

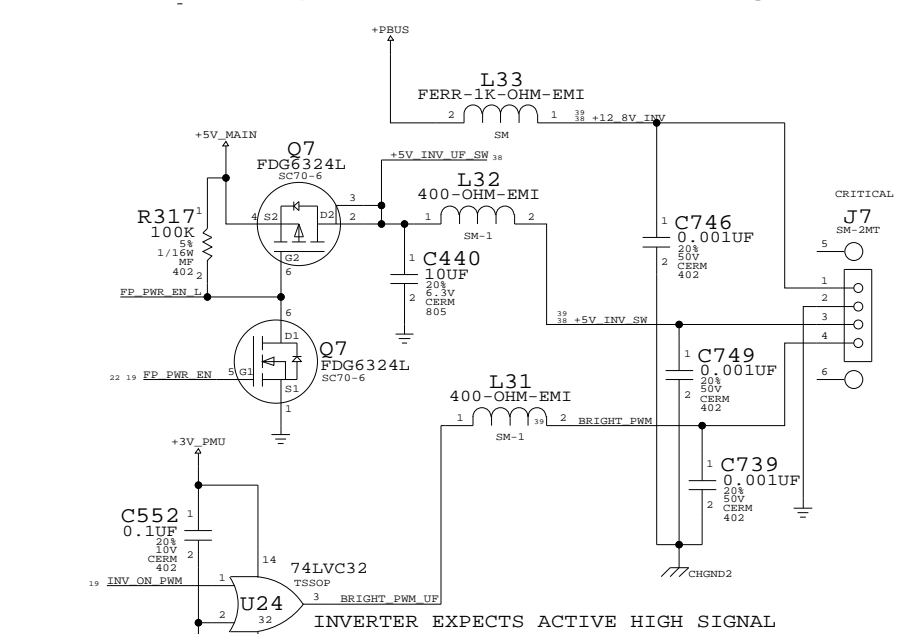


LCD INTERFACE

LVDS INTERFACE

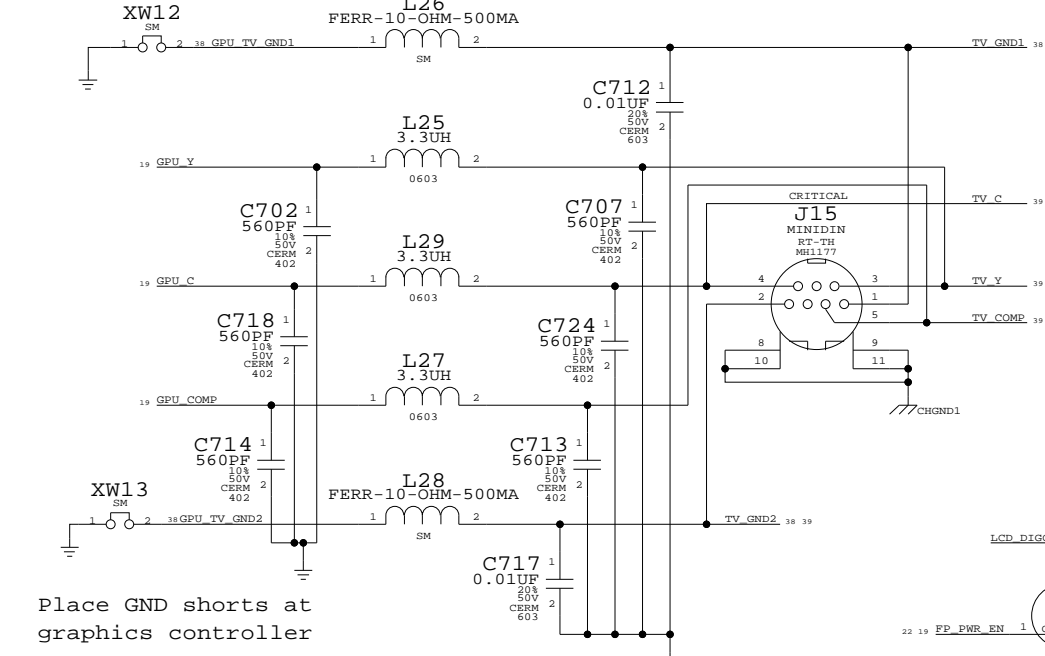


INVERTER INTERFACE



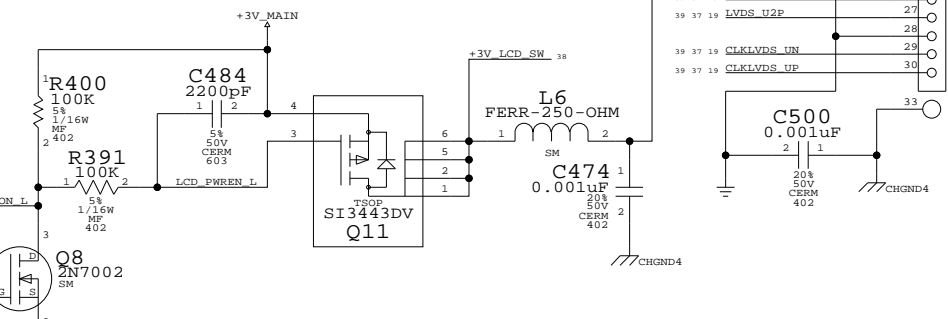
S-VIDEO/COMP OUT INTERFACE

Place GND shorts at graphics controller



Place GND shorts at graphics controller

LCD POWER SWITCHES



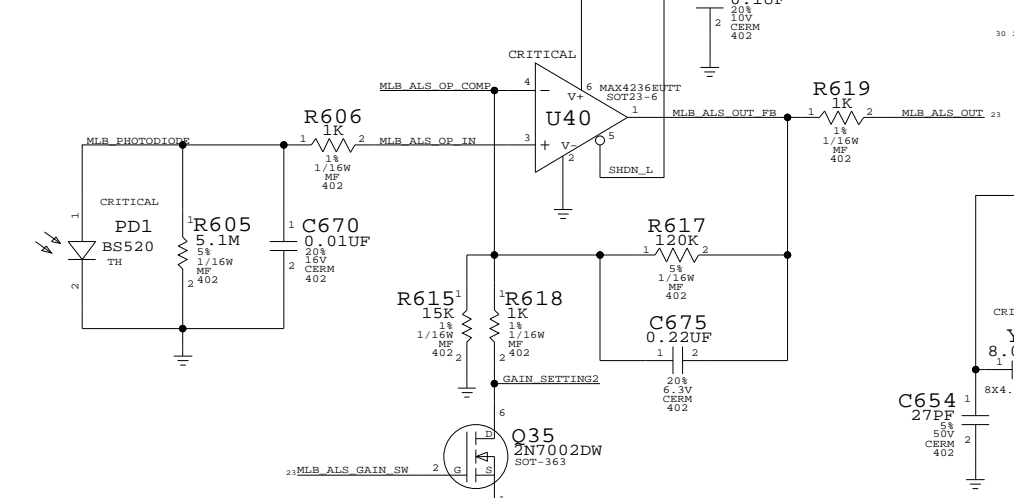
VIDEO CONNECTORS

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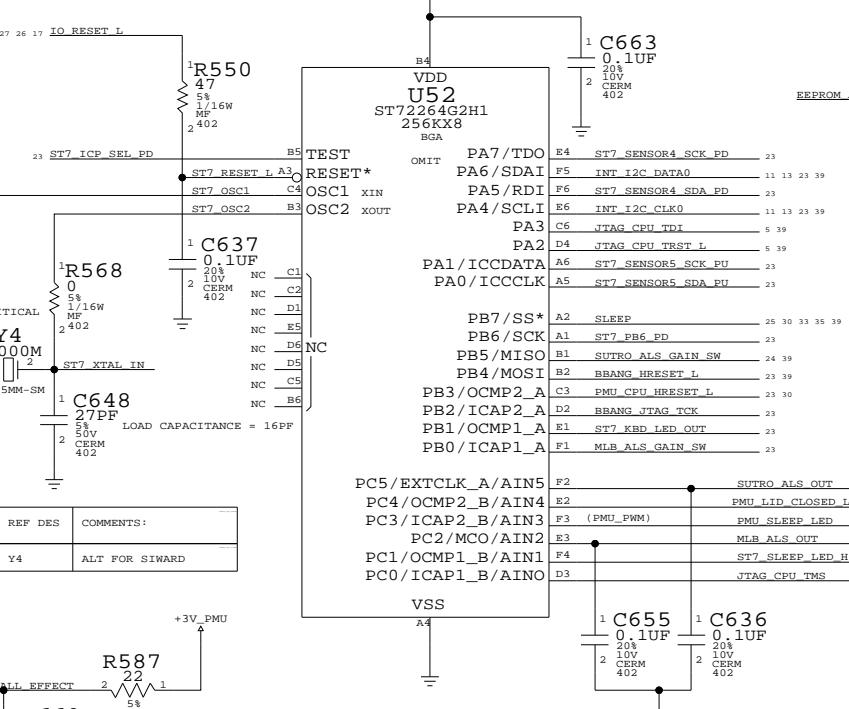
Table with drawing information: APPLE COMPUTER INC., DRAWING NUMBER D 051-6531, REV. B, SCALE NONE, SHEET 22 OF 44.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1194	1	IC,LMU,P84	U52	CRITICAL	?

MLB - ALS SENSOR

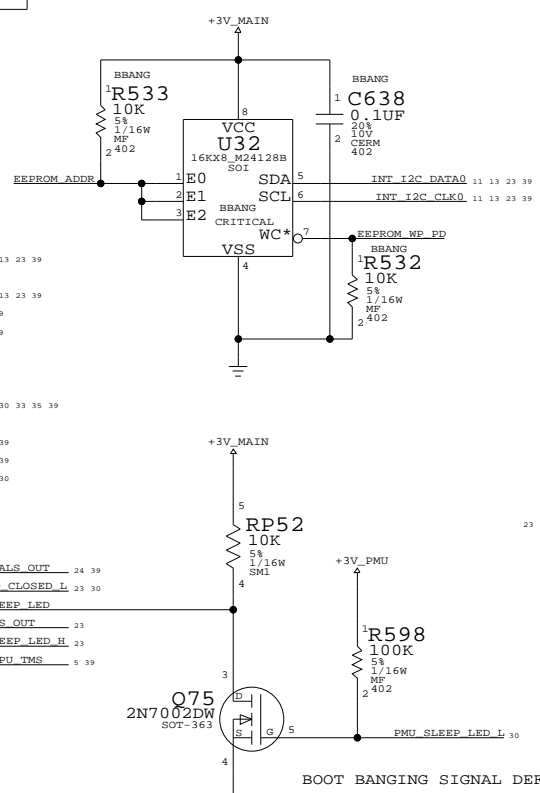


LMU



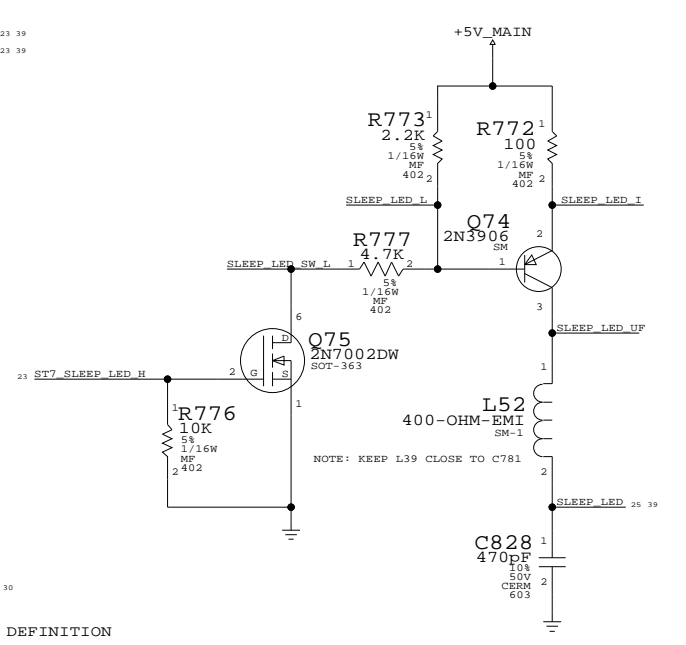
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0008	197S0040		Y4	ALT FOR SIMARD

BOOT BANGER E2PROM

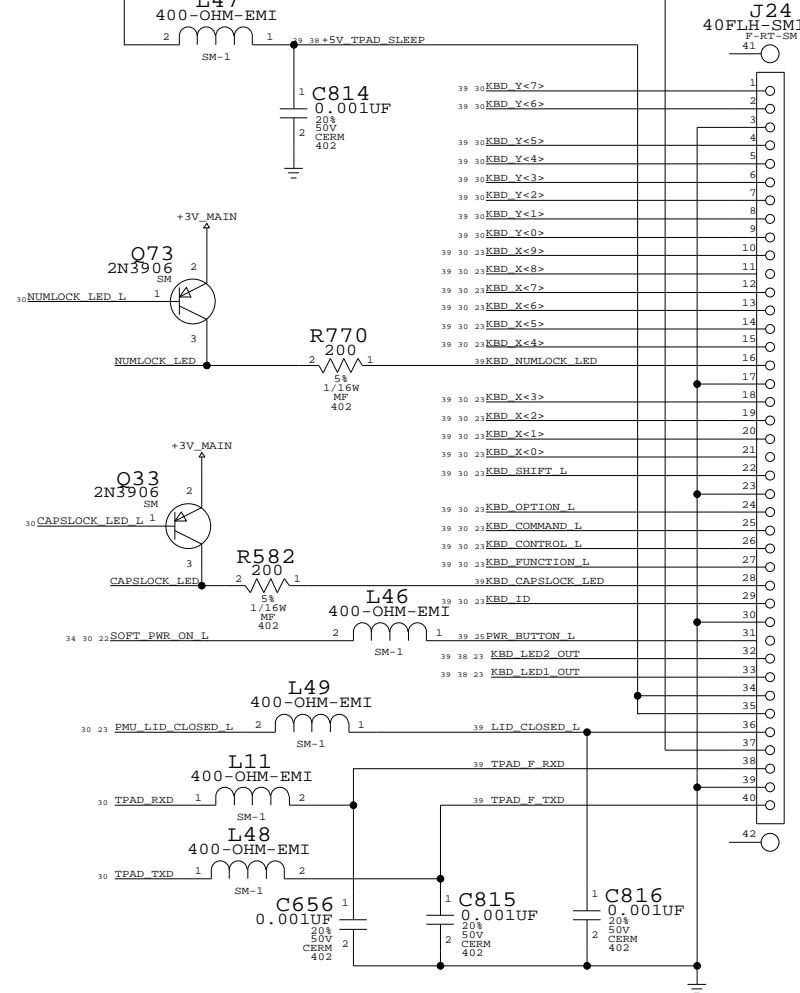


- BOOT BANGING SIGNAL DEFINITION**
- 1/ B Bang_HRESET_L (OPEN COLLECTOR OUTPUT - 10K PULLUP ON MLB)
 - 2/ PMU_HRESET_L (3V INPUT INTO LMU)
 - 3/ B Bang_JTAG_TCK (REGULAR OUTPUT)
 - 4/ JTAG_CPU_TMS (OPEN COLLECTOR OUTPUT - 4700HM PULLUP ON MLB)
 - 5/ JTAG_CPU_TDI (OPEN COLLECTOR OUTPUT - 4700HM PULLUP ON MLB)
 - 6/ JTAG_CPU_TRST_L (OPEN COLLECTOR OUTPUT - 4700HM PULLUP ON MLB)

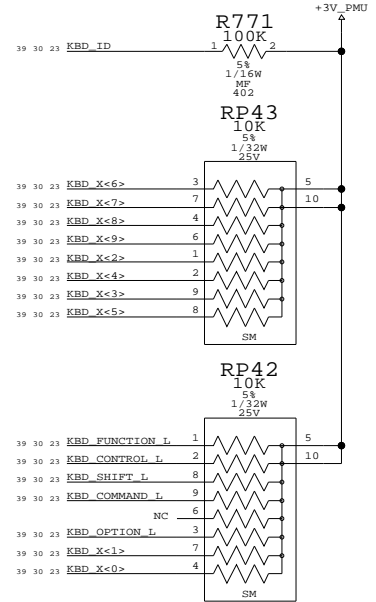
SLEEP LED



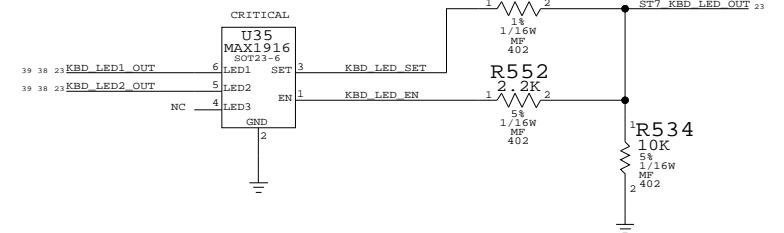
SPIDEY FLEX



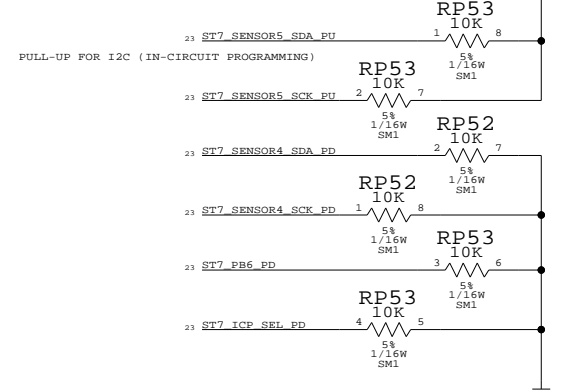
KEYBOARD PULLUPS



KB LED DRIVER



LMU PULL-DOWNS



LMU/BOOTBANGER/SPIDEY

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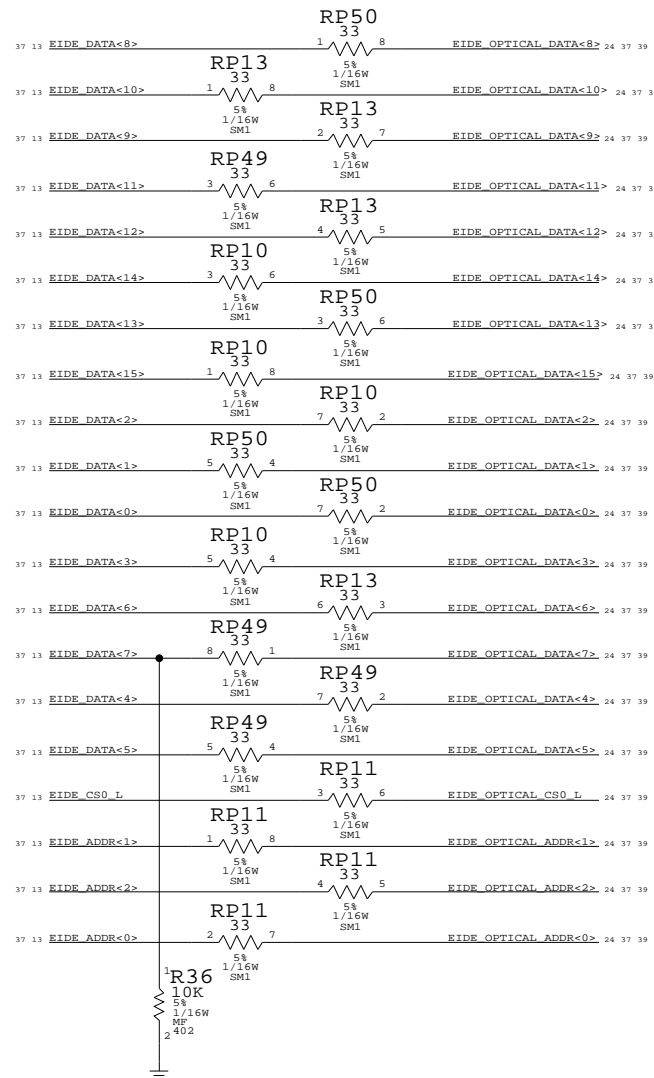
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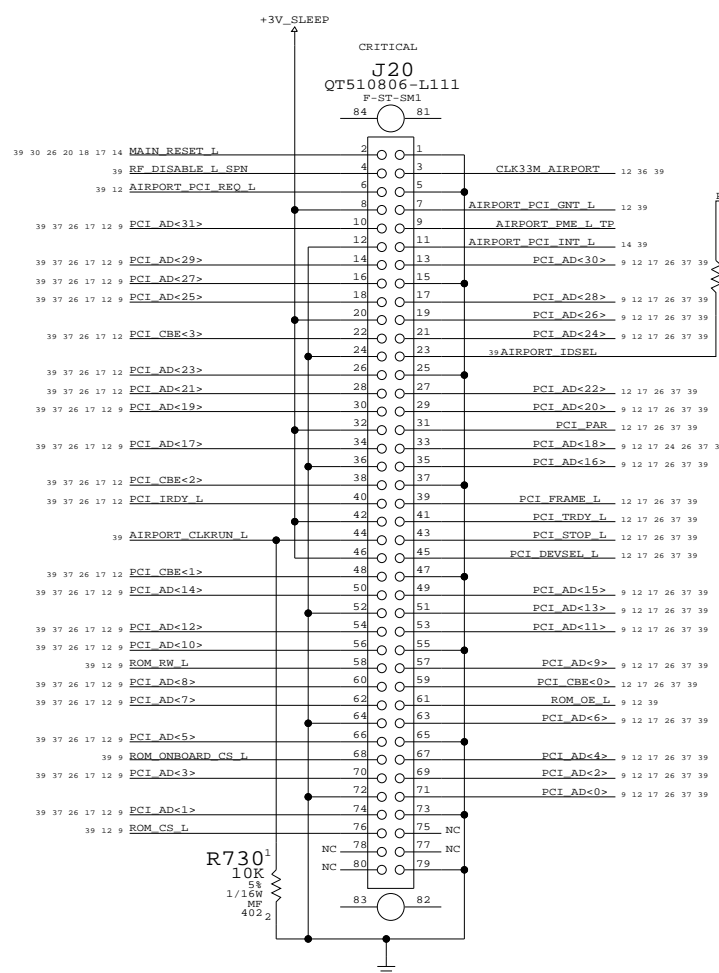
APPLE COMPUTER INC.	SCALE	SHT	REV.
	NONE	23	B
DRAWING NUMBER		REV.	
D 051-6531		B	
SHEET		OF	
NONE		23 44	

HARD DRIVE INTERFACE (UATA100)

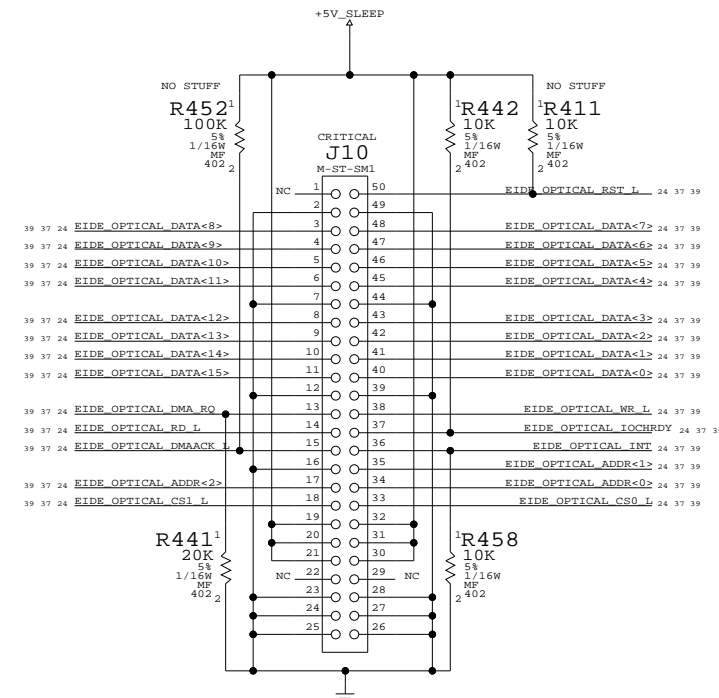
EIDE SERIES TERMINATION PLACE TERMINATORS NEAR INTREPID



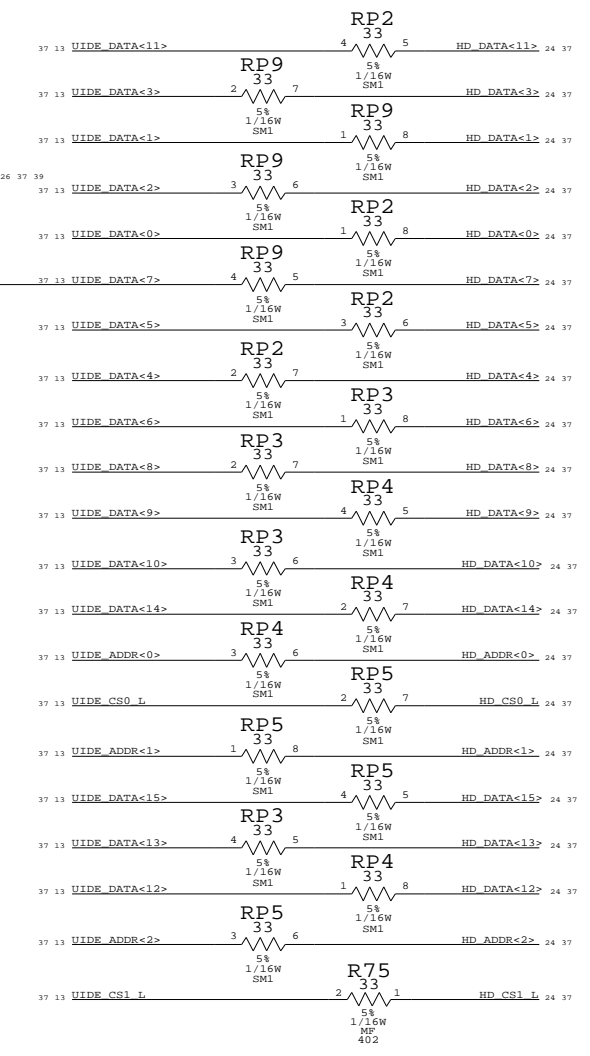
WIRELESS INTERFACE



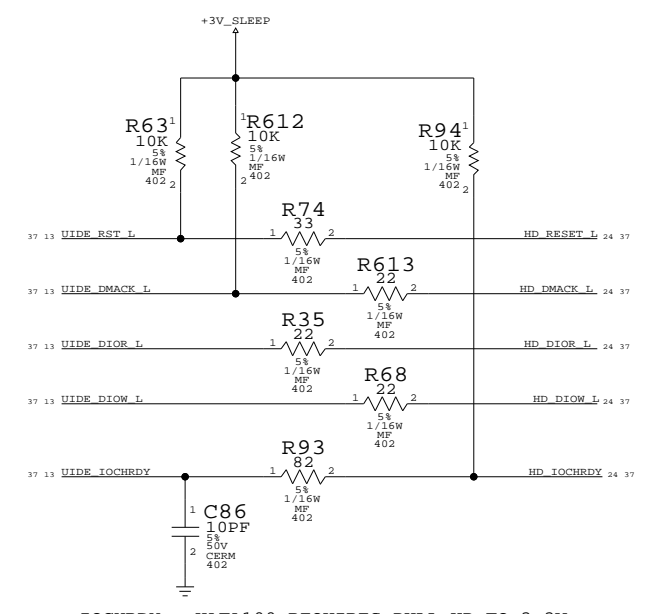
OPTICAL DRIVE INTERFACE (EIDE)



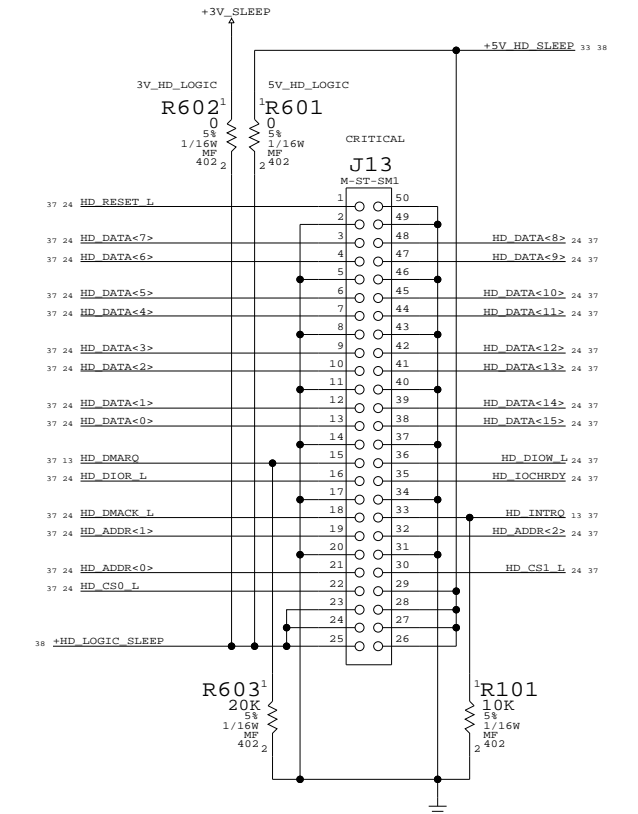
PLACE SERIES R CLOSE TO INTERPID



PLACE PULLUP RESISTORS CLOSE TO INTREPID

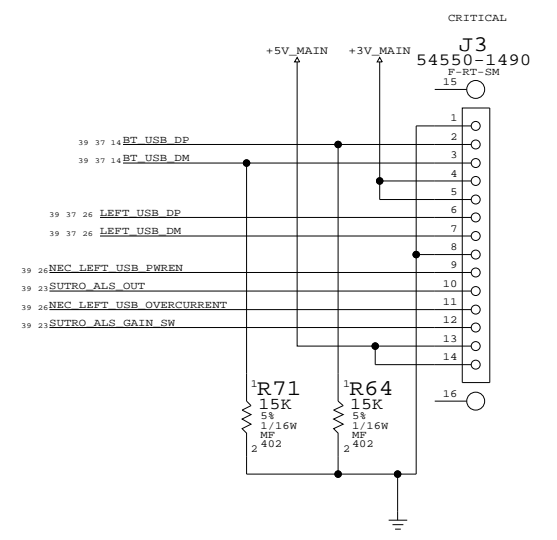


IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V



ANY SEQUENCING REQUIREMENT BETWEEN +5V_HD_SLEEP AND +3V_SLEEP?

BLUETOOTH/LEFT-SIDE USB

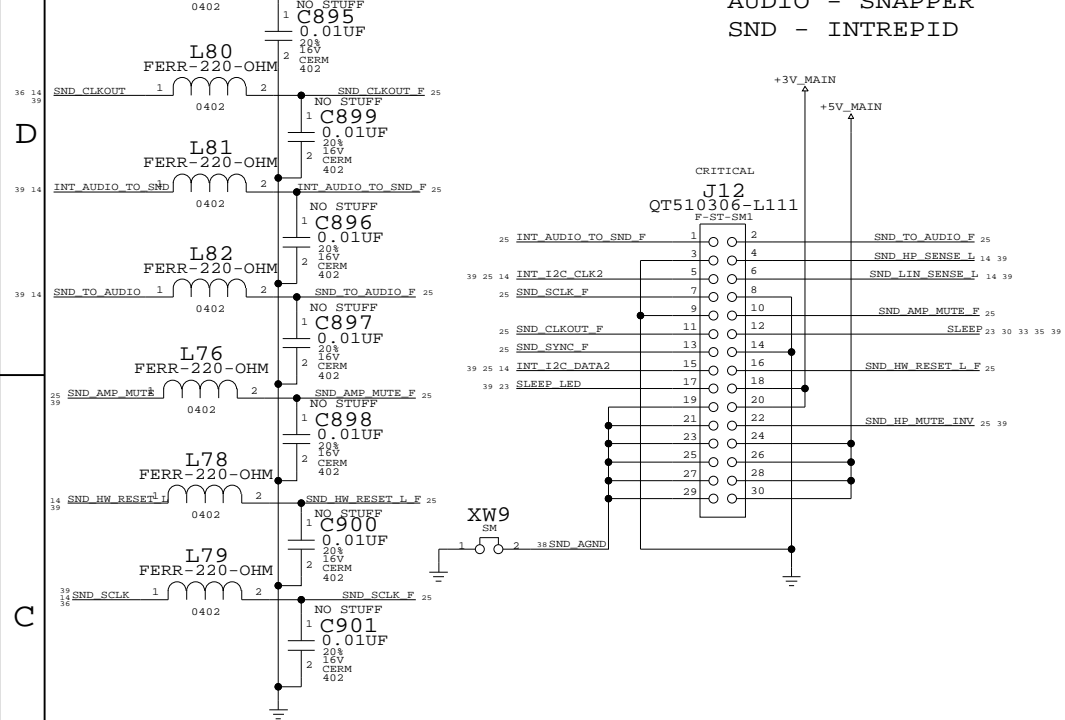


INTERNAL I/O CONNECTORS

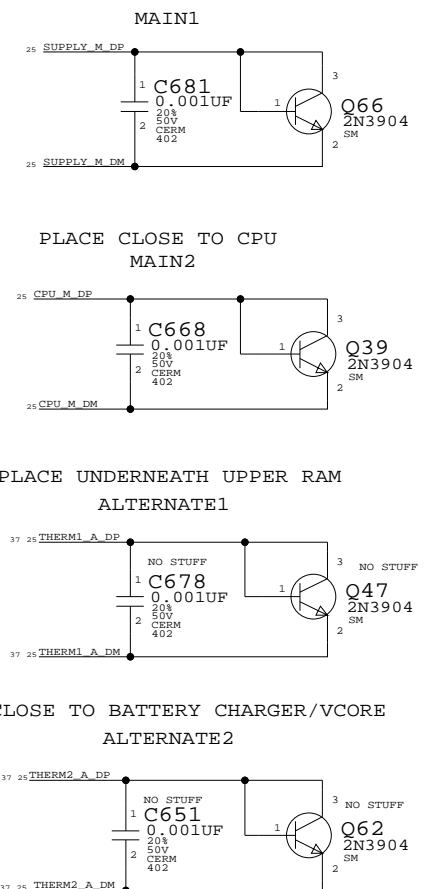
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	D	051-6531	B
SCALE	NONE	SHT	24 OF 44

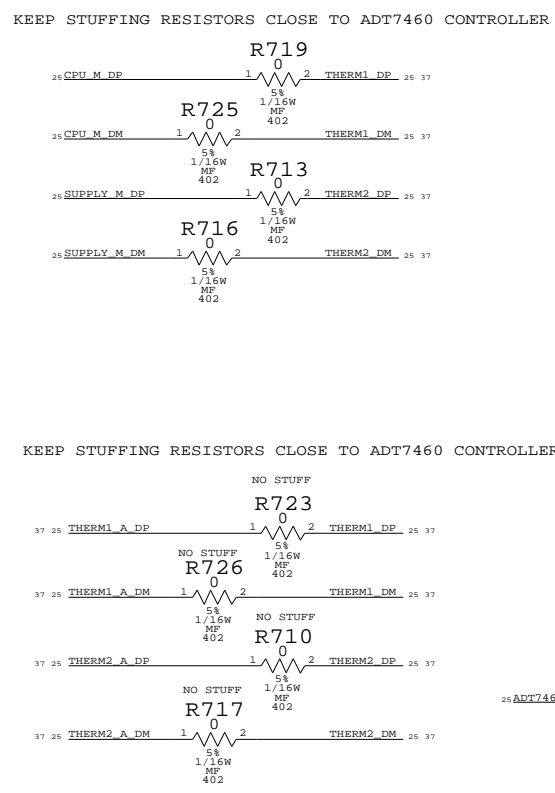
SOUND BOARD (SOUSAPHONE)



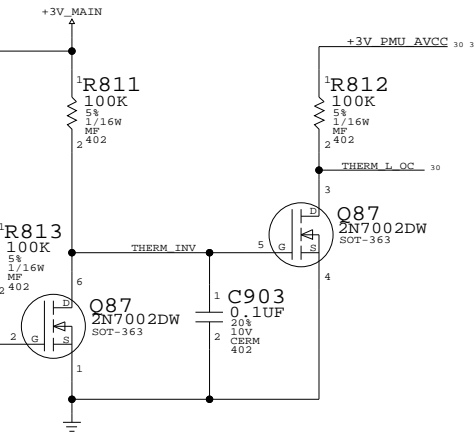
PLACE XW9 CLOSE TO 5V SWITCHER (U27)
PLACE CAPS AS CLOSE TO THERMISTORS AS POSSIBLE
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY



FAN INTERFACE

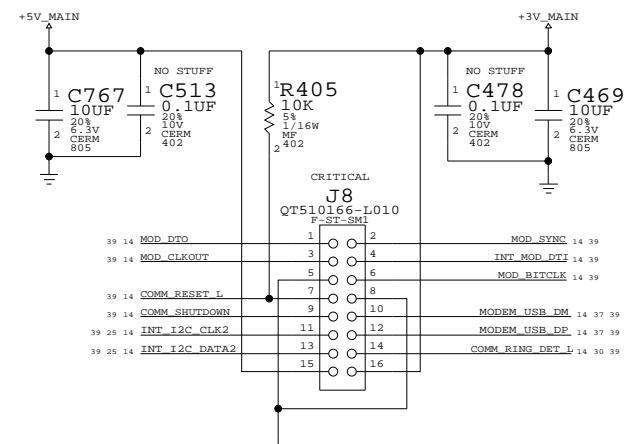


THERM ISOLATION

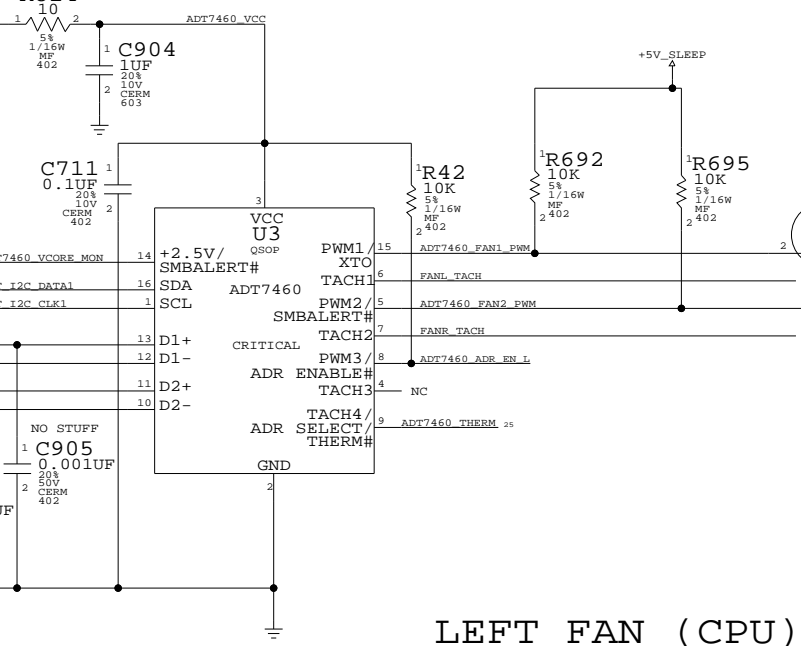


MODEM

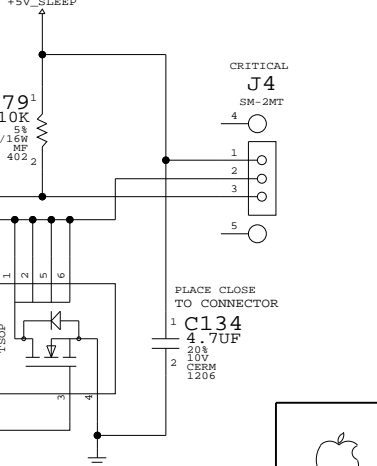
SUPPORTS BOTH THE LAST DASH AND Q52 SOFT MODEM



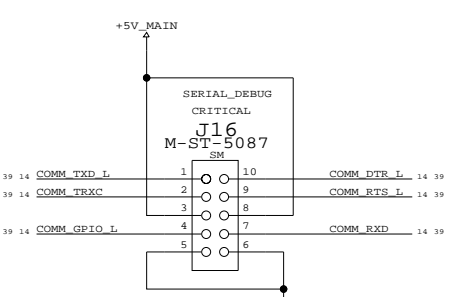
FAN CONTROLLER



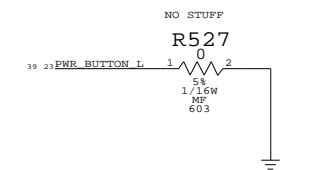
LEFT FAN (CPU)



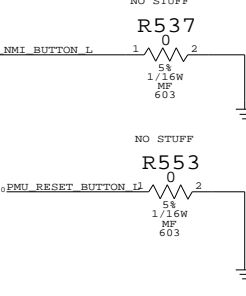
SERIAL DEBUG INTERFACE



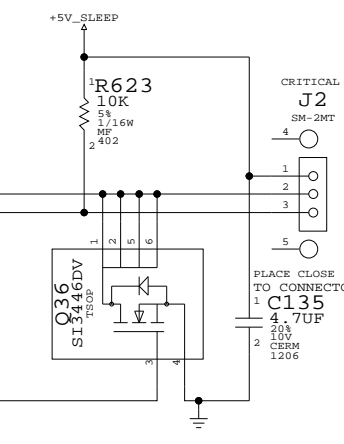
DEBUG POWER BUTTON



DEBUG JUMPERS



RIGHT FAN (GPU)



FAN/MODEM/SOUND/SLEEP LED/DEBUG

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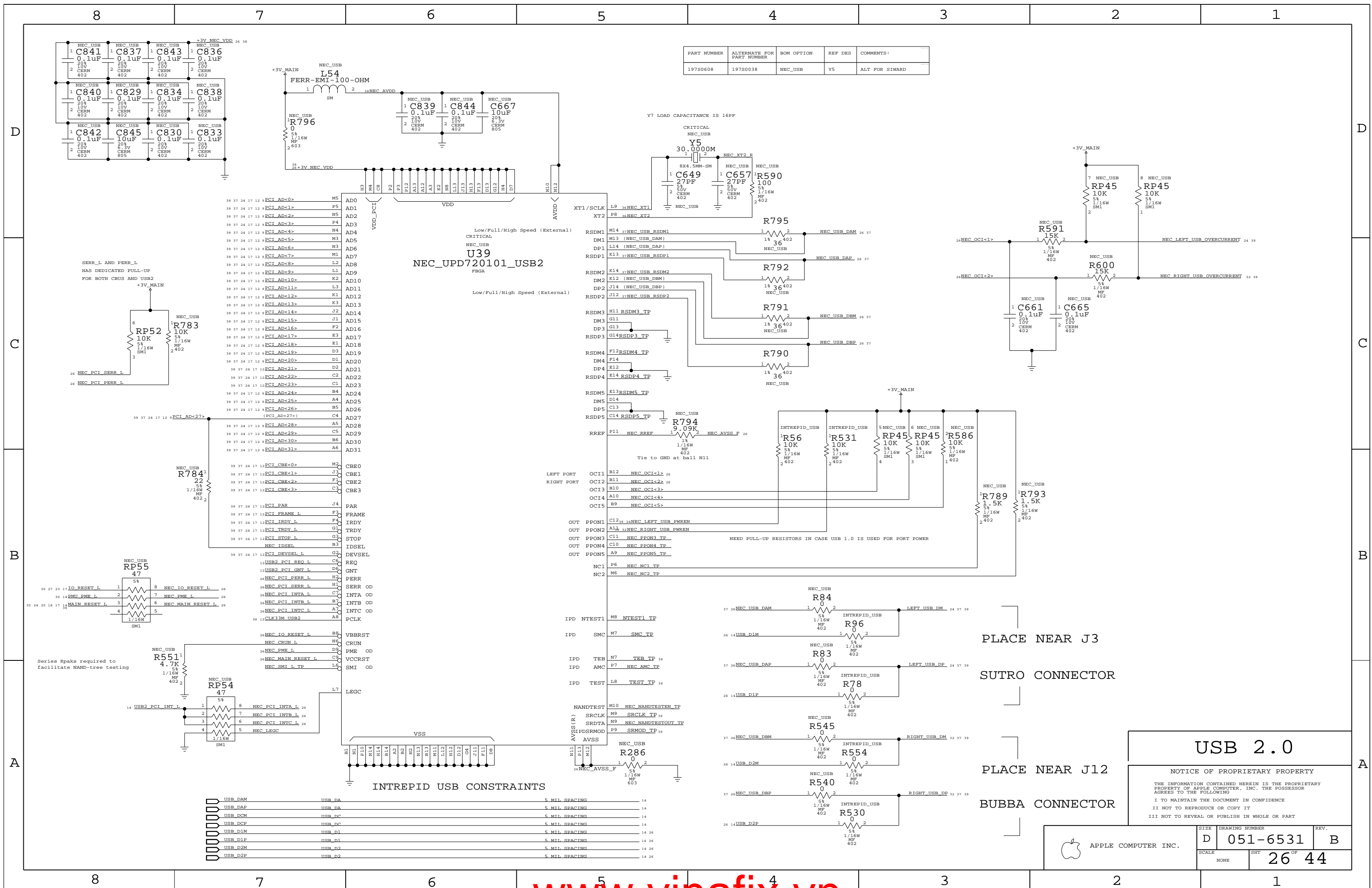
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	D	051-6531	B
SCALE	SHT	25 OF 44	
NONE			



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0608	197S0038	NEC_USB	Y5	ALT FOR SIWARD

Y7 LOAD CAPACITANCE IS 16PF

CRITICAL NEC_USB

Y5 30.0000M

8X4.5MM-SM

NEC_USB

NEC_USB

NEC_USB

NEC_USB

NEC_USB

NEC_USB

NEC_USB

NEC_USB

NEC_USB

NEC_USB

NEC_USB

NEC_USB

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NEC_USB

NEC_USB

NEC_USB

NEC UPD720101_USB2

FBGA

Low/Full/High Speed (External)

CRITICAL

NEC_USB

Low/Full/High Speed (External)

39 37 24 17 12	PCI_Ad<0>	M5	AD0
39 37 24 17 12	PCI_Ad<1>	P5	AD1
39 37 24 17 12	PCI_Ad<2>	N5	AD2
39 37 24 17 12	PCI_Ad<3>	P4	AD3
39 37 24 17 12	PCI_Ad<4>	N4	AD4
39 37 24 17 12	PCI_Ad<5>	M3	AD5
39 37 24 17 12	PCI_Ad<6>	N3	AD6
39 37 24 17 12	PCI_Ad<7>	M1	AD7
39 37 24 17 12	PCI_Ad<8>	L2	AD8
39 37 24 17 12	PCI_Ad<9>	L1	AD9
39 37 24 17 12	PCI_Ad<10>	K2	AD10
39 37 24 17 12	PCI_Ad<11>	L3	AD11
39 37 24 17 12	PCI_Ad<12>	K1	AD12
39 37 24 17 12	PCI_Ad<13>	K3	AD13
39 37 24 17 12	PCI_Ad<14>	J2	AD14
39 37 24 17 12	PCI_Ad<15>	F2	AD15
39 37 24 17 12	PCI_Ad<16>	E3	AD16
39 37 24 17 12	PCI_Ad<17>	E1	AD17
39 37 24 17 12	PCI_Ad<18>	D3	AD18
39 37 24 17 12	PCI_Ad<19>	D1	AD19
39 37 24 17 12	PCI_Ad<20>	D2	AD20
39 37 24 17 12	PCI_Ad<21>	C2	AD21
39 37 24 17 12	PCI_Ad<22>	C1	AD22
39 37 24 17 12	PCI_Ad<23>	B4	AD23
39 37 24 17 12	PCI_Ad<24>	B4	AD24
39 37 24 17 12	PCI_Ad<25>	A4	AD25
39 37 24 17 12	PCI_Ad<26>	B5	AD26
39 37 24 17 12	PCI_Ad<27>	C4	AD27
39 37 24 17 12	PCI_Ad<28>	A5	AD28
39 37 24 17 12	PCI_Ad<29>	C5	AD29
39 37 24 17 12	PCI_Ad<30>	B6	AD30
39 37 24 17 12	PCI_Ad<31>	A6	AD31
39 37 24 17 12	PCI_CBE<0>	M2	CBE0
39 37 24 17 12	PCI_CBE<1>	J3	CBE1
39 37 24 17 12	PCI_CBE<2>	F1	CBE2
39 37 24 17 12	PCI_CBE<3>	C3	CBE3
39 37 24 17 12	PCI_PAR	J4	PAR
39 37 24 17 12	PCI_FRAME_L	F3	FRAME
39 37 24 17 12	PCI_IRDY_L	F4	IRDY
39 37 24 17 12	PCI_TRDY_L	G1	TRDY
39 37 24 17 12	PCI_STOP_L	G3	STOP
39 37 24 17 12	PCI_IDSEL	B3	IDSEL
39 37 24 17 12	PCI_DEVSEL_L	G2	DEVSEL
39 37 24 17 12	USB2_PCI_REQ_L	C6	REQ
39 37 24 17 12	USB2_PCI_GNT_L	D6	GNT
39 37 24 17 12	NEC_PCI_PERR_L	H1	PERR
39 37 24 17 12	NEC_PCI_SERR_L	H1	SERR OD
39 37 24 17 12	NEC_PCI_INTA_L	C7	INTA OD
39 37 24 17 12	NEC_PCI_INTB_L	B7	INTB OD
39 37 24 17 12	NEC_PCI_INTC_L	A7	INTC OD
39 37 24 17 12	CLK33M USB2	A8	PCLK
39 37 24 17 12	NEC_IO_RESET_L	B8	VBRST
39 37 24 17 12	NEC_CRUN_L	N6	CRUN
39 37 24 17 12	NEC_EME_L	D9	PME OD
39 37 24 17 12	NEC_MAIN_RESET_L	C9	VCCRST
39 37 24 17 12	NEC_SMI_L_TP	L6	SMI OD
39 37 24 17 12		L7	LEGC
39 37 24 17 12			VSS

INTREPID USB CONSTRAINTS

USB_DAM	USB_DA	5 MIL SEACING	14
USB_DAP	USB_DA	5 MIL SEACING	14
USB_DCM	USB_DC	5 MIL SEACING	14
USB_DCP	USB_DC	5 MIL SEACING	14
USB_DIM	USB_D1	5 MIL SEACING	14 26
USB_DIP	USB_D1	5 MIL SEACING	14 26
USB_D2M	USB_D2	5 MIL SEACING	14 26
USB_D2P	USB_D2	5 MIL SEACING	14 26

USB 2.0

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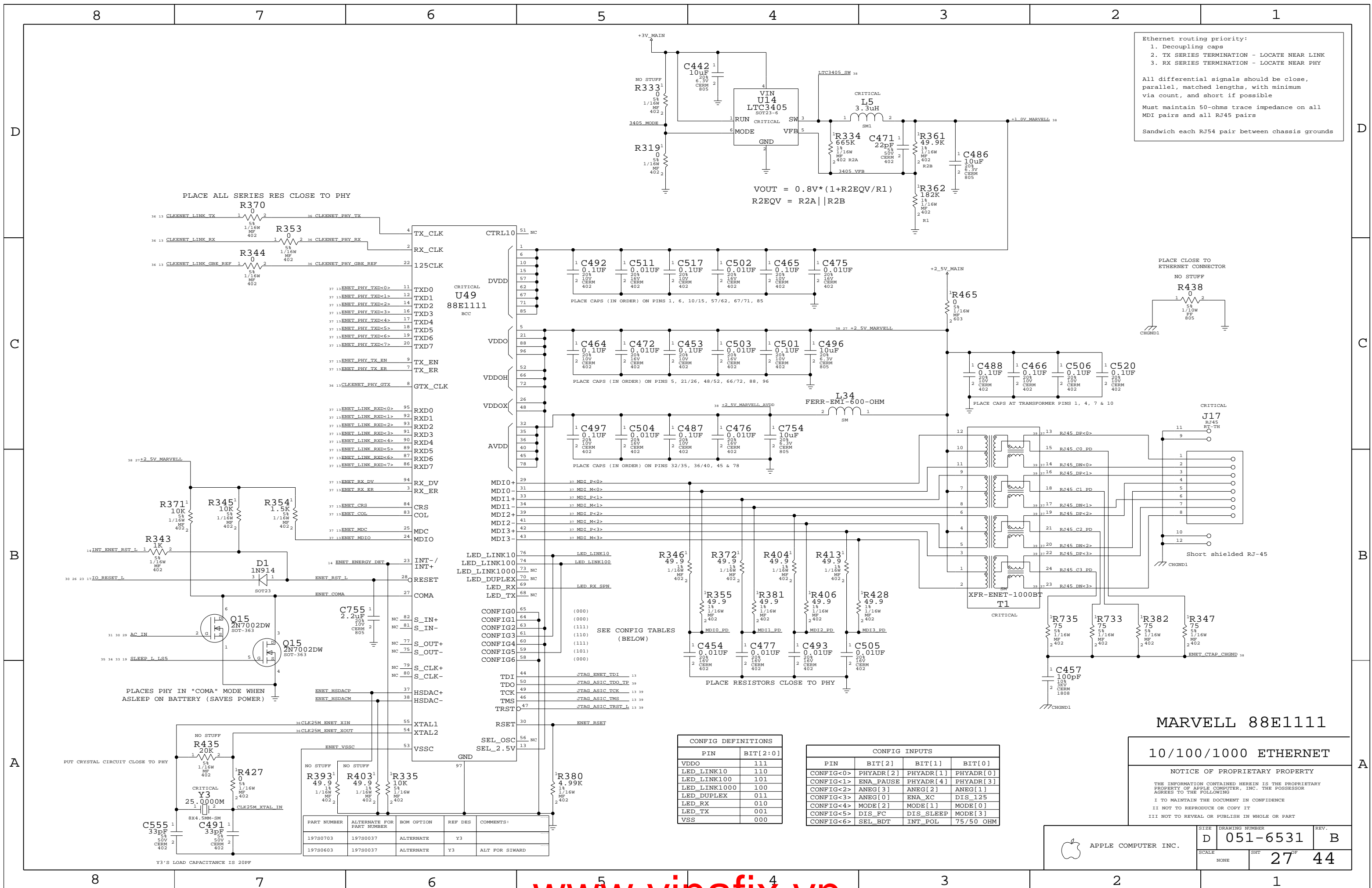
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	NONE	26 OF 44	B



Ethernet routing priority:
 1. Decoupling caps
 2. TX SERIES TERMINATION - LOCATE NEAR LINK
 3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

PLACE ALL SERIES RES CLOSE TO PHY

PLACE CAPS (IN ORDER) ON PINS 1, 6, 10/15, 57/62, 67/71, 85

PLACE CAPS (IN ORDER) ON PINS 5, 21/26, 48/52, 66/72, 88, 96

PLACE CAPS (IN ORDER) ON PINS 32/35, 36/40, 45 & 78

PLACE RESISTORS CLOSE TO PHY

PLACE CLOSE TO ETHERNET CONNECTOR

Short shielded RJ-45

PLACES PHY IN "COMA" MODE WHEN ASLEEP ON BATTERY (SAVES POWER)

CRITICAL
 U49
 88E1111
 BCC

CRITICAL
 J17
 RJ45
 RT-TH

MARVELL 88E1111

10/100/1000 ETHERNET

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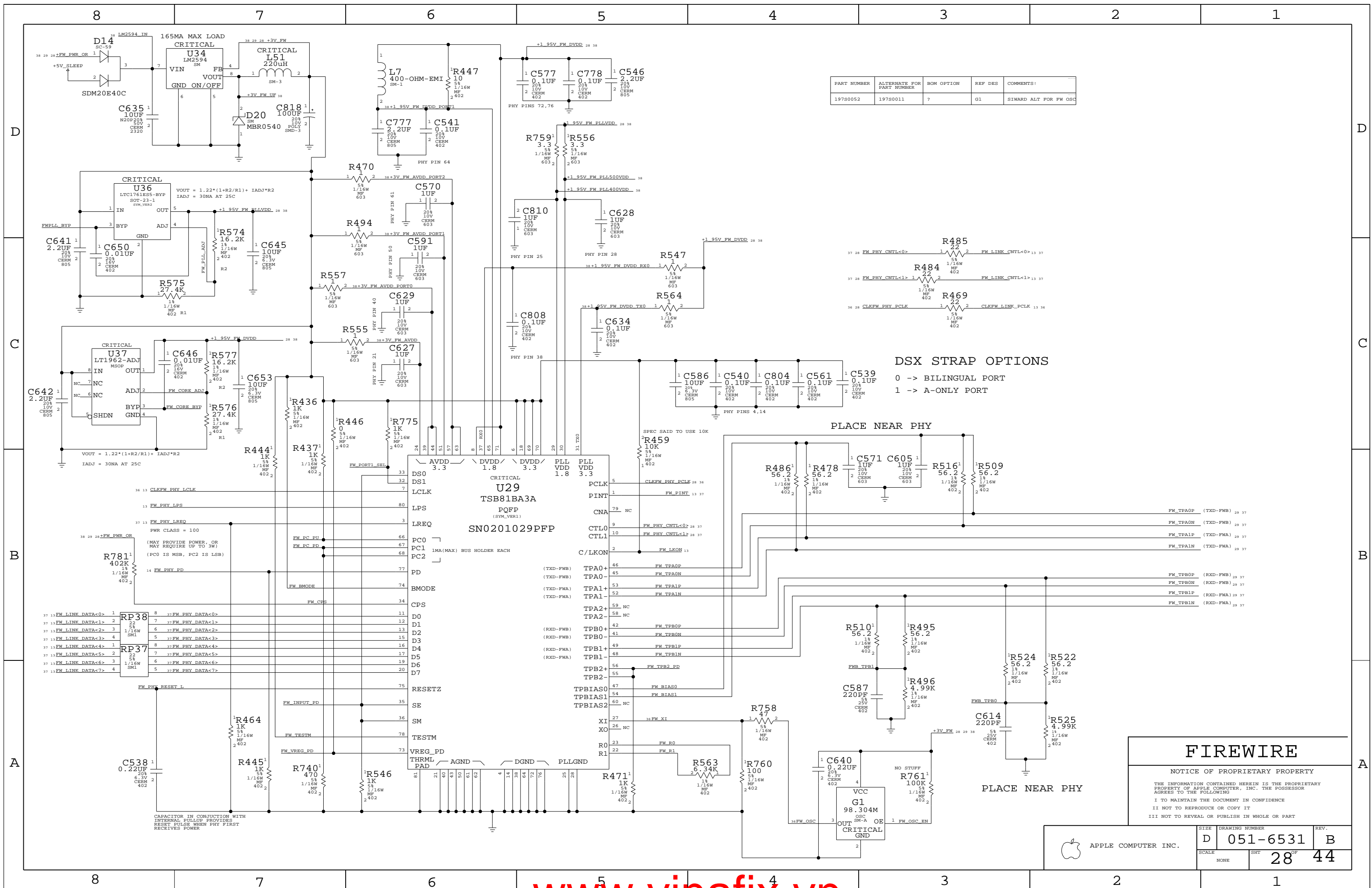
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

CONFIG DEFINITIONS	
PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS			
PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
197S0703	197S0037	ALTERNATE	Y3	
197S0603	197S0037	ALTERNATE	Y3	ALT FOR SIWARD

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6531	REV. B
	SCALE NONE	SHT 27	44



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
197S0052	197S0011	?	G1	SIWARD ALT FOR FW OSC

DSX STRAP OPTIONS
 0 -> BILINGUAL PORT
 1 -> A-ONLY PORT

FIREWIRE

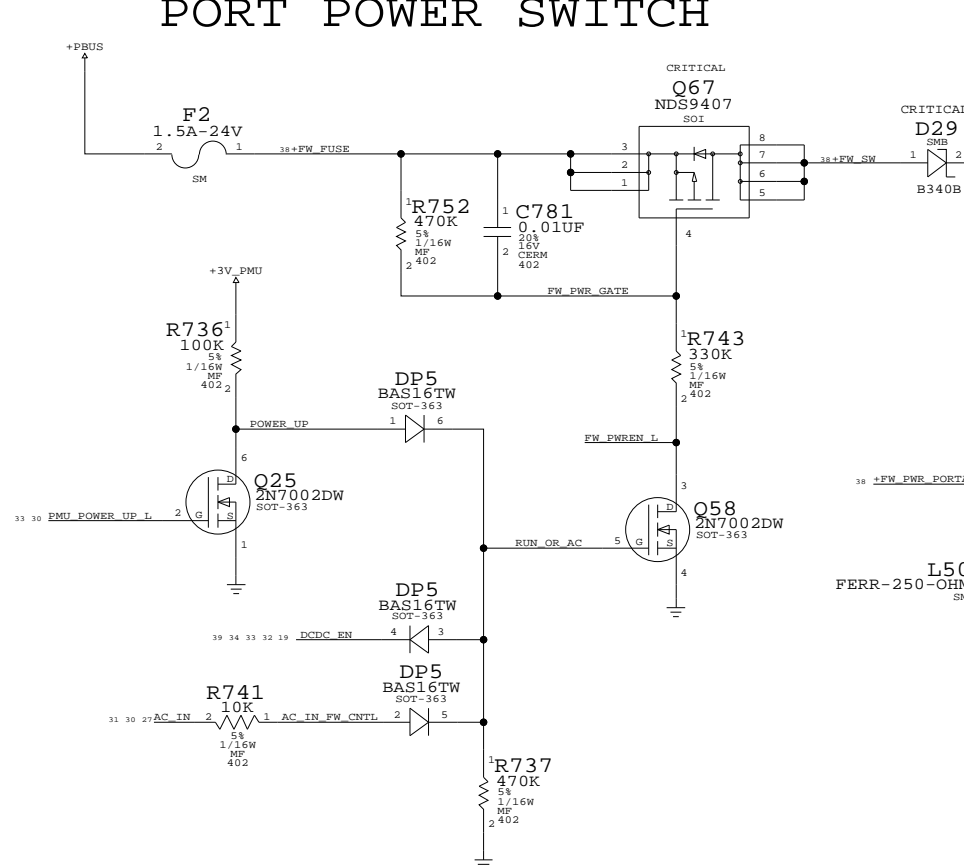
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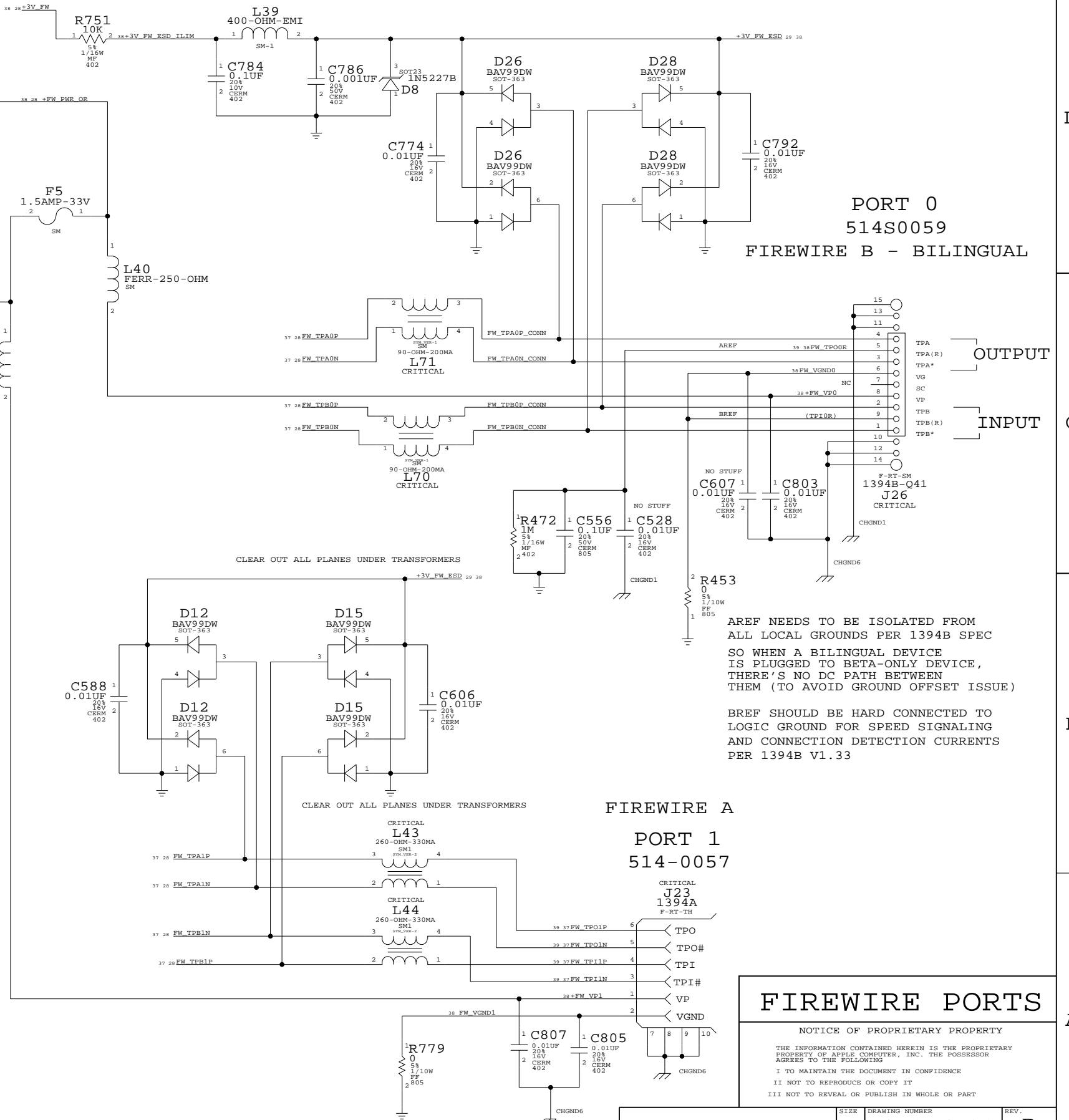
SCALE NONE	SHT 28	REV. B	SIZE	DRAWING NUMBER	REV.
			D	051-6531	B

PORT POWER SWITCH



ENABLES PORT POWER WHEN MACHINE IS RUNNING OR WHEN ASLEEP ON AC

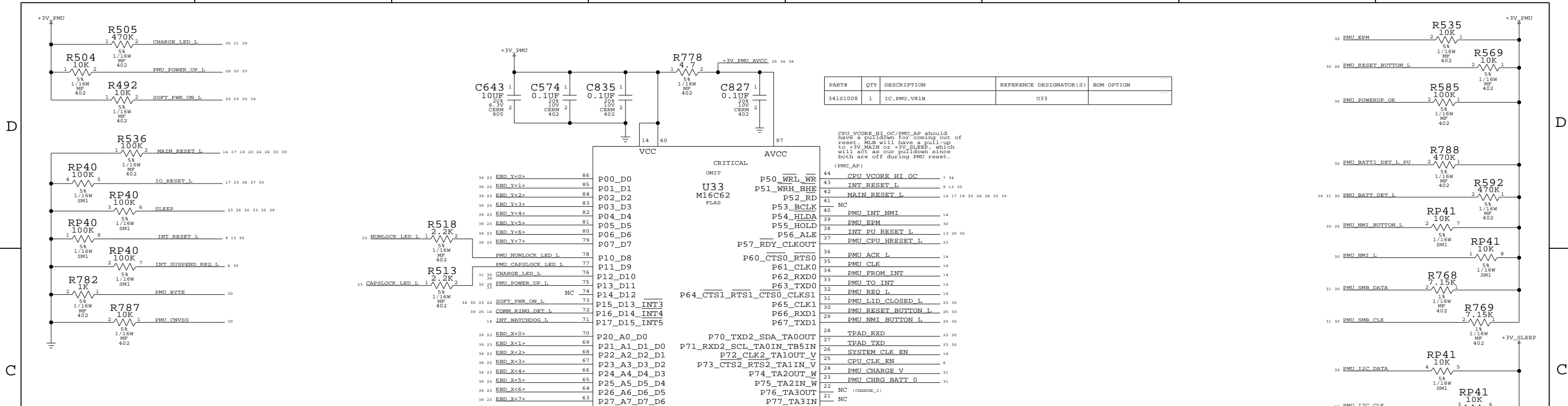
STATE	PMU_POWER_UP_L	POWER_UP	DCDC_EN	AC_IN	LTC4210_ON
SHUTDOWN (AC)	1	0	0	1	OFF
SLEEP (AC)	1	0	1	1	ON
RUN (AC)	0	1	1	1	ON
SHUTDOWN (BATT)	1	0	0	0	OFF
SLEEP (BATT)	1	0	1	0	OFF (PULL-DOWN RESISTOR)
RUN (BATT)	0	1	1	0	ON
	2.99V	+3V_PMU	+4_6V_BU	+3V_PMU	



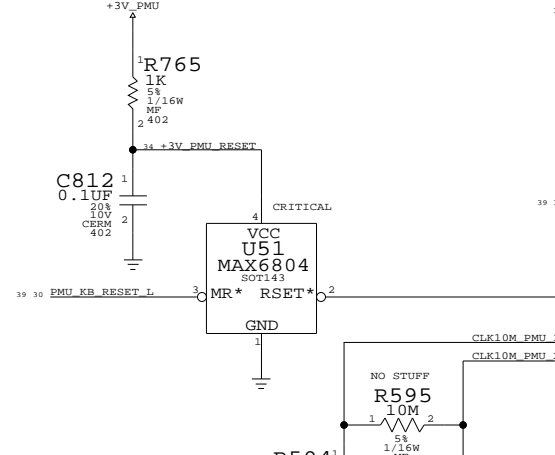
FIREWIRE PORTS

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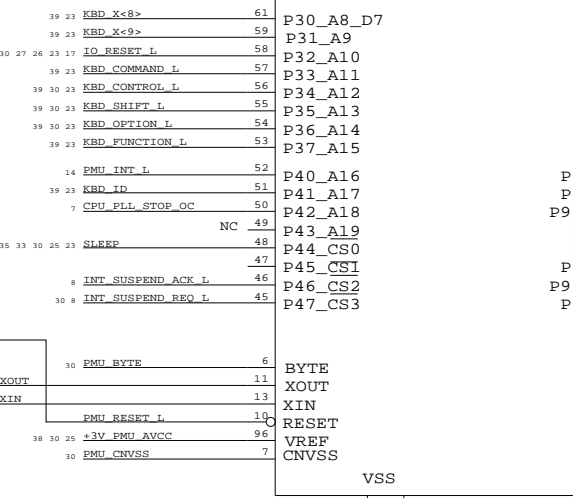
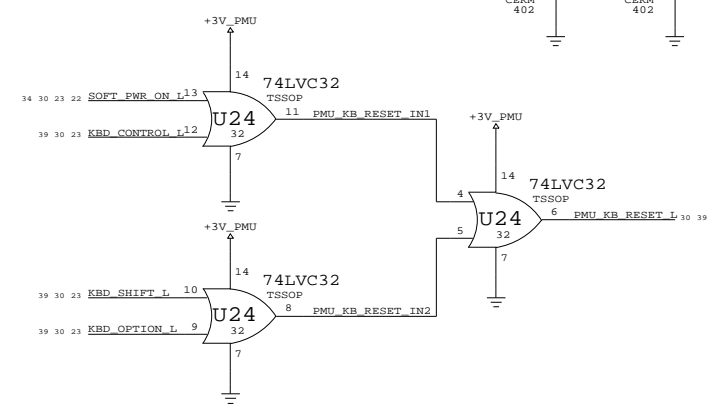
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6531	B
SCALE	NONE	SHT	29 OF 44



UNDERVOLTAGE RESET CIRCUIT



PMU KEYBOARD RESET CIRCUIT

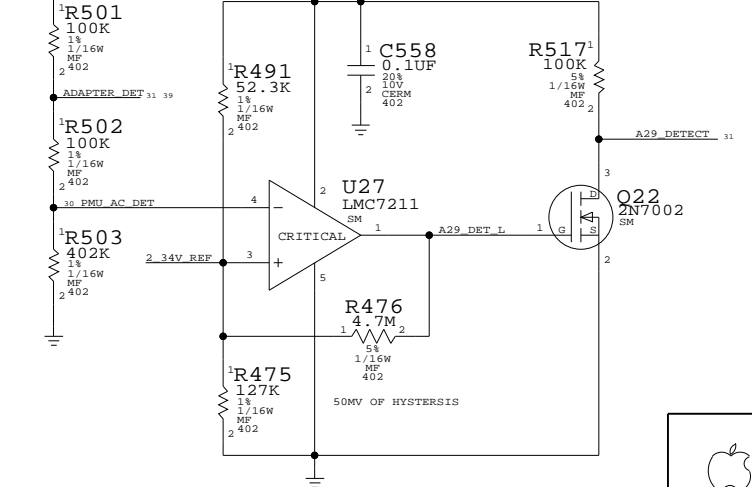


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0704	197S0041		Y6	ALT CRYSTAL SIZE
197S0604	197S0041		Y6	ALT FOR SIWARD

Q11 ADAPTER DETECTION SCHEME

CASE	ADAPTER	PIN VOLT	ID VOLT RANGE	SYSTEM STATUS
1	Q11 (65W)	2.007V-2.066V	1.65V-2.31V	RECOGNIZES AS Q11 FULL FUNCTIONS
2	A29 (45W)	2.558V-2.661V	2.31V-2.97V	RECOGNIZES AS A29 LIMITED FUNCTIONS
3	AIRLINE	0.589V-0.663V	0.33V-0.99V	FULL FUNCTIONS NO BATTERY CHARGING
4	HOOPER	3.19V-3.28V	2.97V-3.30V	RECOGNIZES AS HOOPER LIMITED FUNCTIONS

A29 DETECT CIRCUIT



PMU

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6531	B
SCALE	SHT	
NONE	30	44

DC POWER INPUT

(POWER JACK, ETC. ON SEPARATE BOARD)

CRITICAL

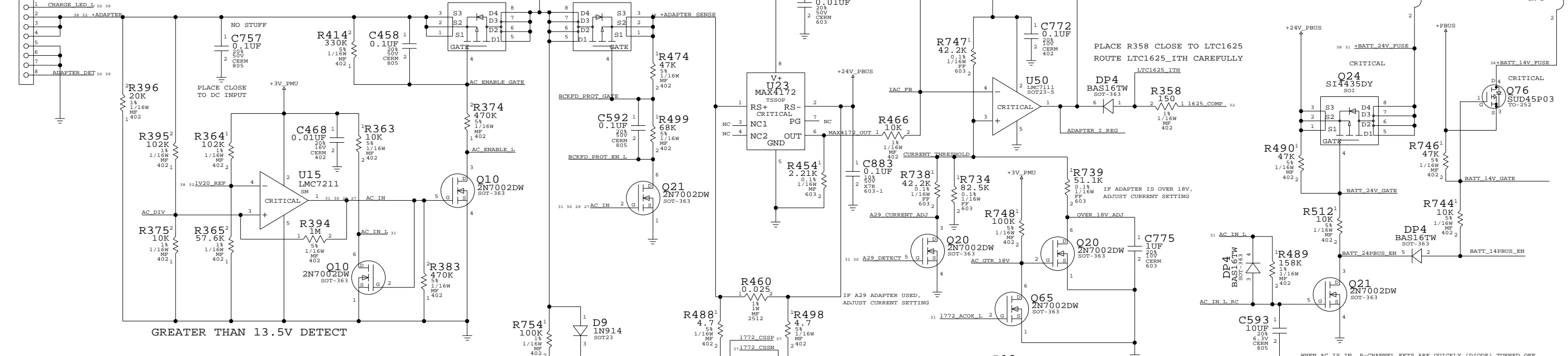
J18
87438-0833
M-RT-SM

DC INRUSH LIMITER

PLACE U23 NEXT TO R460
U23 SENSE VOLTAGE DROP ACROSS R460

1MSEC INTEGRATION TIME

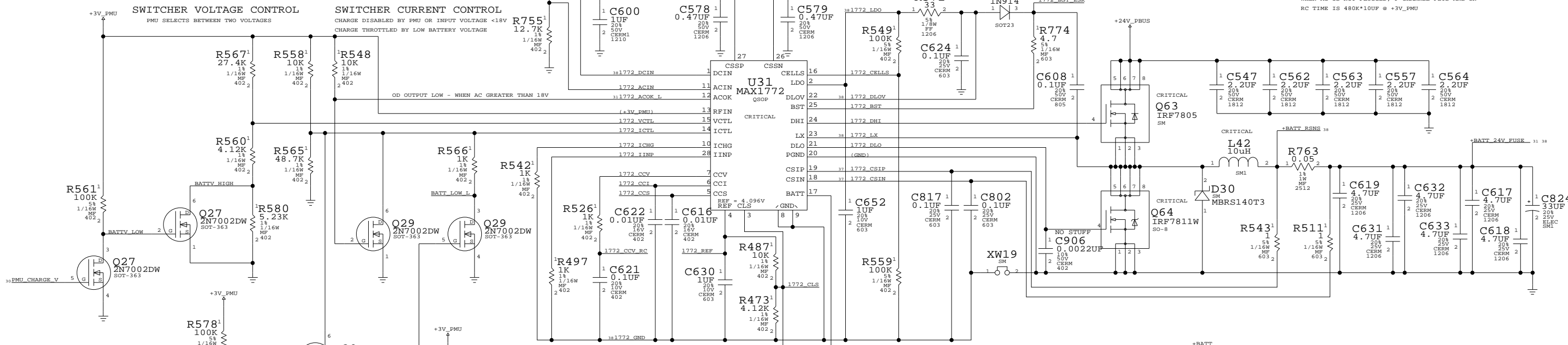
BATTERY SWITCH-OVER CIRCUIT



GREATER THAN 13.5V DETECT

SWITCHER VOLTAGE CONTROL
PMU SELECTS BETWEEN TWO VOLTAGES

SWITCHER CURRENT CONTROL
CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V
CHARGE THROTTLED BY LOW BATTERY VOLTAGE



$V_{BATT} = CELLS \times (4.096 + (0.4096 \times V_{VCTL} / V_{REFIN}))$
 For 4.15V cells, $V_{VCTL} = 0.123 \times V_{REFIN}$
 For 4.20V cells, $V_{VCTL} = 0.245 \times V_{REFIN}$
 $I_{CHG} = (0.2048 / R_{62}) \times (V_{ICTL} / V_{REFIN})$

BATTERY CONNECTOR

J25
87438-0833
M-RT-SM

BATTERY CHARGER

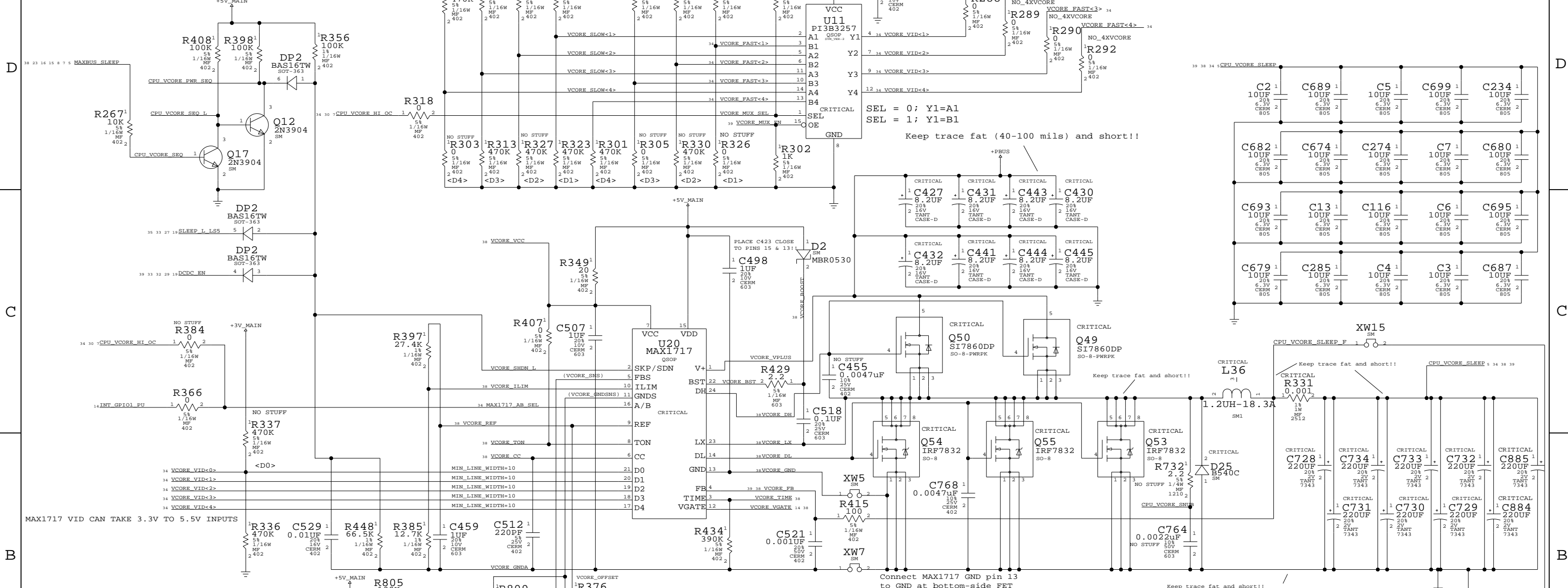
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APPLE COMPUTER INC.	SCALE	DRAWING NUMBER	REV.
	NONE	051-6531	B
		SHT	31 OF 44

VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage (approx. 7ms delay)

1.175V -> 1.025V 1.30V -> 1.10V



OUTPUT VOLTAGE

V _{DAC}		D3	D2	D1	D0
D4=0	D4=1				
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ =	
	Hs/Fast	Lo/Slow
<= 1K PU	1	0
>= 100K PD	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
 When A/B_ is low (slow): <=1K-ohm -> 0
 >=100K-ohm -> 1
 If all pull-ups are >=100K and all pull-downs are <=1K, V_A = V_B.

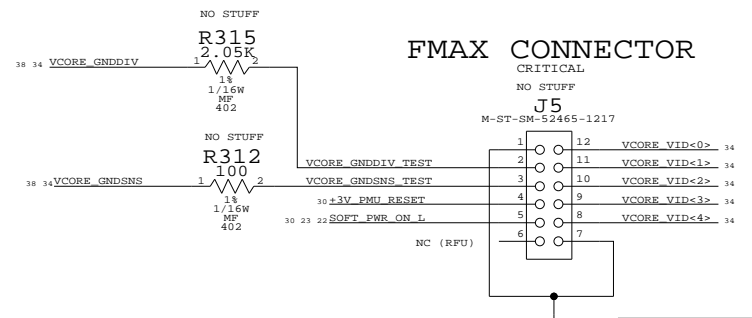
GROUND SENSE VOLTAGE DIVIDER
 This allows for an offset to the ground sense to adjust the output voltage.
 V_{REF} = 2.0V, HENCE V_{OFFSET} = 2.0V * (R1/(R1+R2)) AND V_{CORE} = V_{DAC} + V_{OFFSET}.

NOTE: R310 (R2) NO STUFFED FOR NO OFFSET CASE

ROUTE AS DIFFERENTIAL PAIR

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
11484023	1	RESISTOR	R321	?	1_30_VCORE
11486343	1	RESISTOR	R321	?	1_32_VCORE

FMAX CONNECTOR

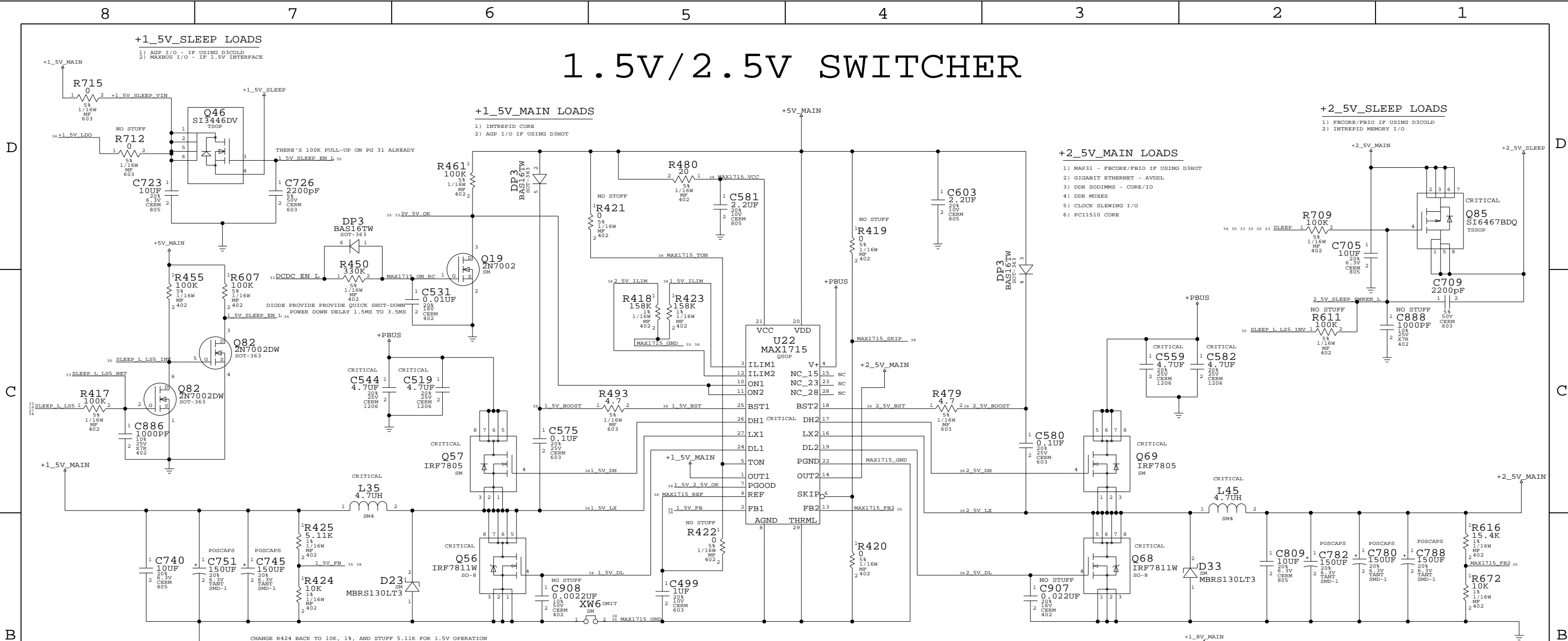


VCORE SUPPLY

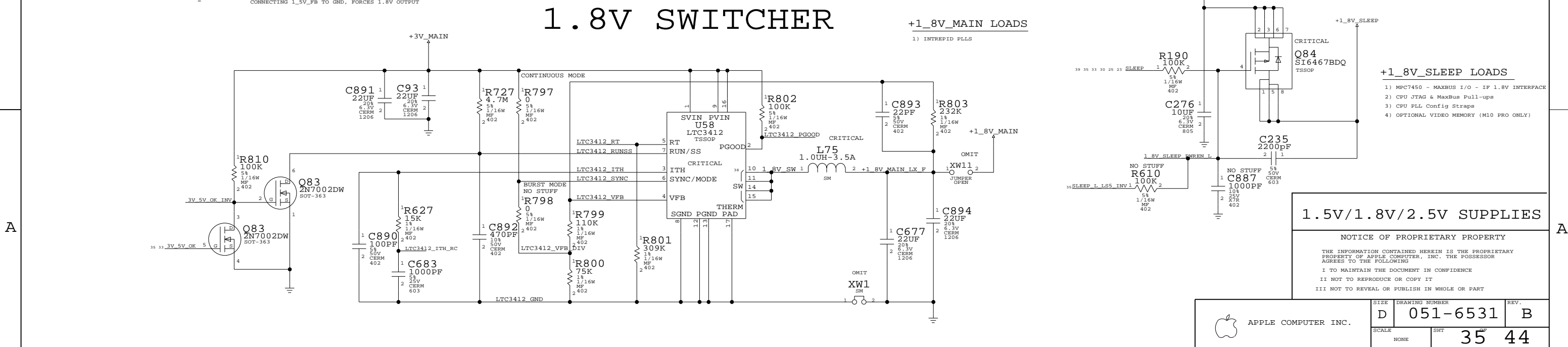
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SCALE NONE	SHT 34	REV. B	SIZE	DRAWING NUMBER	REV.
			D	051-6531	B
SCALE		SHT		REV.	
NONE		34		44	

1.5V/2.5V SWITCHER



1.8V SWITCHER



APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6531	B
SCALE	SHT	35 44	
NONE			

	8	7	6	5	4	3	2	1			
DIGITAL SIGNALS	MAXBUS	SIG_NAME	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM			
		CPU_BACK_L			250.0000	10 MIL SPACING			83 MHZ	5 8	
		CPU_ADDR<0..31>	5		250					5 8	
		CPU_ARTRY_L			250.0000	10 MIL SPACING				5 8	
		CPU_BG_L			250.0000	10 MIL SPACING				5 8	
		CPU_BK_L			250.0000	10 MIL SPACING				5 8	
		CPU_CT_L	5		250.0000					5 8	
		CPU_DATA<0..31>	5		250				83 MHZ	6 8	
		CPU_DATA<32..63>	5		250				83 MHZ	6 8	
		CPU_DBG_L	5		250.0000	10 MIL SPACING				5 8	
		CPU_DTI<0..2>	5		250					5 8	
		CPU_DRDY_L_UF					10 MIL SPACING			5 8	
		CPU_DRDY_L			250.0000	10 MIL SPACING				5 8	
		CPU_GBL_L	5		250.0000					5 8	
		CPU_HIT_L			250.0000	10 MIL SPACING				5 8	
		CPU_OACK_L	5		250.0000	10 MIL SPACING				5 8	
		CPU_QREQ_L			250.0000	10 MIL SPACING				5 8	
		CPU_TA_L			250.0000	10 MIL SPACING				5 8	
		CPU_TRST_L	5		250.0000	10 MIL SPACING				5 8	
		CPU_TEA_L			250.0000					5 8	
		CPU_TS_L			250.0000	10 MIL SPACING				5 8	
		CPU_TSIZ<0..2>	5		250					5 8	
		CPU_TT<0..4>	5		250					5 8	
		CPU_WT_L	5		250.0000					5 8	
		GROUP 0	MEM_DATA<7..0>	4		200				167 MHZ	9 10
	RAM_DATA_A<7..0>		4		200				167 MHZ	10 11	
	RAM_DATA_B<7..0>		4		200				167 MHZ	10 11	
	MEM_DQS<0>		4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200					9 10	
	RAM_DQS_A<0>		4		200					10 11	
	RAM_DQS_B<0>		4		200					10 11	
	MEM_DQM<0>		4		200					9 10	
	RAM_DQM_A<0>		4		200					10 11	
	RAM_DQM_B<0>		4		200					10 11	
	MEM_DATA<15..8>		4		200				167 MHZ	9 10	
	RAM_DATA_A<15..8>		4		200				167 MHZ	10 11	
	RAM_DATA_B<15..8>		4		200				167 MHZ	10 11	
	MEM_DQS<1>		4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200					9 10	
	RAM_DQS_A<1>		4		200					10 11	
	RAM_DQS_B<1>		4		200					10 11	
	MEM_DQM<1>		4		200					9 10	
	RAM_DQM_A<1>		4		200					10 11	
	RAM_DQM_B<1>		4		200					10 11	
	MEM_DATA<31..16>		4		200				167 MHZ	9 10	
	RAM_DATA_A<31..16>		4		200				167 MHZ	10 11	
	RAM_DATA_B<31..16>		4		200				167 MHZ	10 11	
	MEM_DQS<3..2>		4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200					9 10	
	RAM_DQS_A<3..2>		4		200				167 MHZ	10 11	
	RAM_DQS_B<3..2>		4		200				167 MHZ	10 11	
	MEM_DQM<3..2>		4		200					9 10	
	RAM_DQM_A<3..2>	4		200				167 MHZ	10 11		
	RAM_DQM_B<3..2>	4		200				167 MHZ	10 11		
	MEM_DATA<47..32>	4		200				167 MHZ	9 10		
	RAM_DATA_A<47..32>	4		200				167 MHZ	10 11		
	RAM_DATA_B<47..32>	4		200				167 MHZ	10 11		
	MEM_DQS<5..4>	4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200					9 10		
	RAM_DQS_A<5..4>	4		200				167 MHZ	10 11		
	RAM_DQS_B<5..4>	4		200				167 MHZ	10 11		
	MEM_DQM<5..4>	4		200					9 10		
	RAM_DQM_A<5..4>	4		200				167 MHZ	10 11		
	RAM_DQM_B<5..4>	4		200				167 MHZ	10 11		
	MEM_DATA<55..48>	4		200				167 MHZ	9 10		
	RAM_DATA_A<55..48>	4		200				167 MHZ	10 11		
	RAM_DATA_B<55..48>	4		200				167 MHZ	10 11		
	MEM_DQS<6>	4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200					9 10		
	RAM_DQS_A<6>	4		200					10 11		
	RAM_DQS_B<6>	4		200					10 11		
	MEM_DQM<6>	4		200					9 10		
	RAM_DQM_A<6>	4		200					10 11		
	RAM_DQM_B<6>	4		200					10 11		
	MEM_DATA<63..56>	4		200				167 MHZ	9 10		
	RAM_DATA_A<63..56>	4		200				167 MHZ	10 11		
	RAM_DATA_B<63..56>	4		200				167 MHZ	10 11		
	MEM_DQS<7>	4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200					9 10		
	RAM_DQS_A<7>	4		200					10 11		
	RAM_DQS_B<7>	4		200					10 11		
	MEM_DQM<7>	4		200					9 10		
	RAM_DQM_A<7>	4		200					10 11		
	RAM_DQM_B<7>	4		200					10 11		
	MEM_ADDR<12..0>	4						83 MHZ	9		
	RAM_ADDR<12..0>	6		200					9 11		
	MEM_BA<1..0>	4							9		
	RAM_BA<1..0>	6		200					9 11		
	MEM_CS_L<3..0>	4							9		
	RAM_CS_L<3..0>	6		200					9 11		
	MEM_CKE<3..0>	4							9		
	RAM_CKE<3..0>	6		200					9 11		
	MEM_RAS_L	4							9		
	RAM_RAS_L	4		200.0000					9 11		
	MEM_CAS_L	4							9		
	RAM_CAS_L	4		200.0000					9 11		
	MEM_WE_L	4							9		
	RAM_WE_L	4		200.0000					9 11		
	MEM_MUXSEL_H<1..0>	3							9 10		
	RAM_MUXSEL_L<1..0>	3							9 10		
	MEM_MUXSEL_H	5							10		
	RAM_MUXSEL_L	5							10		
	CLOCK LINE CONSTRAINTS	INTREPID CLOCKS	SIG_NAME	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM		
			SYSCLK_CPU_UF							10 MIL SPACING	8
			SYSCLK_CPU	4							8
			INT_CPUFB_OUT	3		200.0000		10 MIL SPACING			8
INT_CPUFB_OUT_SHORT			3				10 MIL SPACING			8	
INT_CPUFB_OUT_NORM			3				10 MIL SPACING			8	
INT_CPUFB_IN_NORM			3				10 MIL SPACING			8	
INT_CPUFB_LONG			3				10 MIL SPACING			8	
INT_CPUFB_IN			3				10 MIL SPACING			8	
INT_CPUFB_IN_2			3		200.0000		10 MIL SPACING			8	
SYSCLK_DDRCLK_A0_L_UF			3		200.0000		10 MIL SPACING			8	
SYSCLK_DDRCLK_A0_L			3		200.0000		10 MIL SPACING			8	
SYSCLK_DDRCLK_A1_UF			3		200.0000		10 MIL SPACING			8	
SYSCLK_DDRCLK_A1_L			3		200.0000		10 MIL SPACING			8	
SYSCLK_DDRCLK_B0_UF			3		200.0000		10 MIL SPACING			8	
SYSCLK_DDRCLK_B0_L			3		200.0000		10 MIL SPACING			8	
SYSCLK_DDRCLK_B1_UF			3		200.0000		10 MIL SPACING			8	
SYSCLK_DDRCLK_B1_L			3		200.0000		10 MIL SPACING			8	
SYSCLK_DDRCLK_A0			3		200.0000		10 MIL SPACING			9 11	
SYSCLK_DDRCLK_A0_L			3		200.0000		10 MIL SPACING			9 11	
SYSCLK_DDRCLK_A1			3		200.0000		10 MIL SPACING			9 11	
SYSCLK_DDRCLK_A1_L			3		200.0000		10 MIL SPACING			9 11	
SYSCLK_DDRCLK_B0			3		200.0000		10 MIL SPACING			9 11	
SYSCLK_DDRCLK_B0_L			3		200.0000		10 MIL SPACING			9 11	
SYSCLK_DDRCLK_B1			3		200.0000		10 MIL SPACING			9 11	
SYSCLK_DDRCLK_B1_L		3		200.0000		10 MIL SPACING			9 11		
INT_REF_CLK_OUT		3		200.0000		10 MIL SPACING			14		
INT_REF_CLK_IN		3		200.0000		10 MIL SPACING			14		
CLK66M_GPU_AGP_UF		4		200.0000		10 MIL SPACING			12		
CLK66M_GPU_AGP		4		200.0000		10 MIL SPACING			12 18		
INT_AGP_FB_OUT		4		200.0000		10 MIL SPACING			12		
INT_AGP_FB_IN		4		200.0000		10 MIL SPACING			12		
CLK33M_CBUS_UF		4		200.0000		10 MIL SPACING			12		
CLK33M_CBUS		4	SHOULD BE AT MOST 4 VIAS FOR CLK	200.0000		10 MIL SPACING			12 17		
CLK33M_AIRPORT_UF		4		200.0000		10 MIL SPACING			12		
CLK33M_AIRPORT		4	SHOULD BE AT MOST 4 VIAS FOR CLK	200.0000		10 MIL SPACING			12 24 39		
CLK33M_USB2_UF		4		200.0000		10 MIL SPACING			12		
CLK33M_USB2		4	SHOULD BE AT MOST 4 VIAS FOR CLK	200.0000		10 MIL SPACING			12 26		
INT_PCI_FB_OUT		3		200.0000		10 MIL SPACING			12		
INT_PCI_FB_IN		3		200.0000		10 MIL SPACING			12		
MAP31		GPU_CLK27M_OUT					10 MIL SPACING				
		GPU_CLK27M_UF					10 MIL SPACING				
		GPU_SSCLK_UF					10 MIL SPACING				
		GPU_SSCLK_IN					10 MIL SPACING				
		GPU_FBCLK0					10 MIL SPACING				
		GPU_FBCLK0_L					10 MIL SPACING				
		GPU_FBCLK1					10 MIL SPACING				
		GPU_FBCLK1_L					10 MIL SPACING				
		GPU_DVO_CLKP					10 MIL SPACING			19 20	
		CRYSTALS	CLK27M_GPU_XOUT					10 MIL SPACING			
CLK27M_XTAL_IN							10 MIL SPACING				
CLK27M_GPU_XIN							10 MIL SPACING				
CLK18M_INT_XIN							10 MIL SPACING			14	
CLK18M_INT_XOUT							10 MIL SPACING			14	
CLK18M_XTAL_IN							10 MIL SPACING			14	
CLK18M_INT_EXT							10 MIL SPACING			14	
CLK25M_ENET_XIN							10 MIL SPACING			27	
CLK25M_ENET_XOUT							10 MIL SPACING			27	
NEC_XT1							10 MIL SPACING			26	
NEC_XT2			THERE'S ANOTHER 280MIL LEG			10 MIL SPACING			26		
SOUND		SND_SCLK	7				10 MIL SPACING			14 25 39	
		SND_CLKOUT					10 MIL SPACING			14 25 39	
ETHERNET MARVELL		CLKENET_PHY_RX					10 MIL SPACING			27	
		CLKENET_LINK_RX	3				10 MIL SPACING			13 27	
		CLKENET_PHY_GBE_REF					10 MIL SPACING			27	
		CLKENET_LINK_GBE_REF	3				10 MIL SPACING			13 27	
		CLKENET_PHY_TX									

FUNCTIONAL TEST POINTS

8	7	6	5	4	3	2	1
FUNC_TEST=YES JTAG ASIC TMS 13 27	FUNC_TEST=YES TMS_CONN_CLKP 22 37	FUNC_TEST=YES TV_C 22	FUNC_TEST=YES PCI_AD<7> 9 12 17 24 26 37	FUNC_TEST=YES PCI_PAR 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_CS0_L 24 37	FUNC_TEST=YES KBD_X<9> 23 30	FUNC_TEST=YES +5V_INV_SW 22 38
FUNC_TEST=YES JTAG ASIC TDI 13	FUNC_TEST=YES VGA_R 22	FUNC_TEST=YES TV_Y 22	FUNC_TEST=YES PCI_AD<8> 9 12 17 24 26 37	FUNC_TEST=YES PCI_CBE<0> 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_CS1_L 24 37	FUNC_TEST=YES KBD_Y<0> 23 30	FUNC_TEST=YES LEFT_USB_DM 24 26 37
FUNC_TEST=YES JTAG ASIC TDO_TP 27	FUNC_TEST=YES VGA_G 22	FUNC_TEST=YES TV_COMP 22	FUNC_TEST=YES PCI_AD<9> 9 12 17 24 26 37	FUNC_TEST=YES PCI_CBE<1> 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_RST_L 24 37	FUNC_TEST=YES KBD_Y<1> 23 30	FUNC_TEST=YES LEFT_USB_DP 24 26 37
FUNC_TEST=YES JTAG ASIC TCK 13 27	FUNC_TEST=YES VGA_B 22	FUNC_TEST=YES SND_TO_AUDIO 14 25	FUNC_TEST=YES PCI_AD<10> 9 12 17 24 26 37	FUNC_TEST=YES PCI_CBE<2> 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_WR_L 24 37	FUNC_TEST=YES KBD_Y<2> 23 30	FUNC_TEST=YES RIGHT_USB_DM 26 32 37
FUNC_TEST=YES JTAG ASIC TRST_L 13 27	FUNC_TEST=YES VGA_VSYNC 22	FUNC_TEST=YES SND_SYNC 14 25	FUNC_TEST=YES PCI_AD<11> 9 12 17 24 26 37	FUNC_TEST=YES PCI_CBE<3> 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_LOCHRDY 24 37	FUNC_TEST=YES KBD_Y<3> 23 30	FUNC_TEST=YES RIGHT_USB_DP 26 32 37
FUNC_TEST=YES CPU_CHKSTP_OUT_L 5	FUNC_TEST=YES VGA_HSYNC 22	FUNC_TEST=YES SND_CLKOUT 14 25 36	FUNC_TEST=YES PCI_AD<12> 9 12 17 24 26 37	FUNC_TEST=YES AIRPORT_PCI_REQ_L 12 24	FUNC_TEST=YES EIDE_OPTICAL_INT 24 37	FUNC_TEST=YES KBD_Y<4> 23 30	FUNC_TEST=YES NEC_LEFT_USB_PWREN 24 26
FUNC_TEST=YES CPU_SRESET_L 5	FUNC_TEST=YES DVI_DDC_CLK_UP 22		FUNC_TEST=YES PCI_AD<13> 9 12 17 24 26 37	FUNC_TEST=YES AIRPORT_PCI_GNT_L 12 24	FUNC_TEST=YES TPAD_F_TXD 23	FUNC_TEST=YES KBD_Y<5> 23 30	FUNC_TEST=YES NEC_LEFT_USB_OVERCURRENT 24 26
FUNC_TEST=YES CPU_HRESET_L 5 7 23	FUNC_TEST=YES DVI_DDC_DATA_UP 22		FUNC_TEST=YES PCI_AD<14> 9 12 17 24 26 37	FUNC_TEST=YES AIRPORT_PCI_INT_L 14 24	FUNC_TEST=YES TPAD_F_RXD 23	FUNC_TEST=YES KBD_Y<6> 23 30	FUNC_TEST=YES NEC_RIGHT_USB_PWREN 26 32
FUNC_TEST=YES JTAG_CPU_TMS 5 23	FUNC_TEST=YES DVI_HPD_UP 22	FUNC_TEST=YES INT_AUDIO_TO_SND 14 25	FUNC_TEST=YES PCI_AD<15> 9 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DATA<0> 24 37	FUNC_TEST=YES LID_CLOSED_L 23	FUNC_TEST=YES KBD_Y<7> 23 30	FUNC_TEST=YES NEC_RIGHT_USB_OVERCURRENT 26 32
FUNC_TEST=YES JTAG_CPU_TDI 5 23	FUNC_TEST=YES LVDS_L0N 19 22 37	FUNC_TEST=YES SND_SCLK 14 25 36	FUNC_TEST=YES PCI_AD<16> 9 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DATA<1> 24 37	FUNC_TEST=YES COMM_RESET_L 14 25	FUNC_TEST=YES KBD_NUMLOCK_LED 23	FUNC_TEST=YES DCDC_EN 19 29 32 33 34
FUNC_TEST=YES JTAG_CPU_TDO_TP 5	FUNC_TEST=YES LVDS_L0P 19 22 37	FUNC_TEST=YES SND_HW_RESET_L 14 25	FUNC_TEST=YES PCI_AD<17> 9 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DATA<2> 24 37	FUNC_TEST=YES COMM_SHUTDOWN 14 25	FUNC_TEST=YES +BATT_POS 31 38	FUNC_TEST=YES BRANG_HRESET_L 23
FUNC_TEST=YES JTAG_CPU_TCK 5 23	FUNC_TEST=YES LVDS_L1N 19 22 37	FUNC_TEST=YES SND_HP_SENSE_L 14 25	FUNC_TEST=YES PCI_AD<18> 9 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DATA<3> 24 37	FUNC_TEST=YES COMM_RING_DET_L 14 25 30	FUNC_TEST=YES BATT_CLK 31	FUNC_TEST=YES KBD_LED2_OUT 23 38
FUNC_TEST=YES JTAG_CPU_TEST_L 5 23 39	FUNC_TEST=YES LVDS_L1P 19 22 37	FUNC_TEST=YES SND_LIN_SENSE_L 14 25	FUNC_TEST=YES PCI_AD<19> 9 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DATA<4> 24 37	FUNC_TEST=YES KBD_ID 23 30	FUNC_TEST=YES BATT_DATA 31	FUNC_TEST=YES MAIN_RESET_L 14 17 18 20 24 26 30
	FUNC_TEST=YES LVDS_L2N 19 22 37	FUNC_TEST=YES INT_I2C_DATA2 14 25	FUNC_TEST=YES PCI_AD<20> 9 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DATA<5> 24 37	FUNC_TEST=YES +SV_TPAD_SLEEP 23 38	FUNC_TEST=YES BATT_NEG 31 38	FUNC_TEST=YES RF_DISABLE_L_SPN 24
	FUNC_TEST=YES LVDS_L2P 19 22 37	FUNC_TEST=YES INT_I2C_CLK2 14 25	FUNC_TEST=YES PCI_AD<21> 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DATA<6> 24 37	FUNC_TEST=YES +3V_HALL_EFFECT 23 38	FUNC_TEST=YES PMU_BATT_DET_L 30 31	FUNC_TEST=YES AIRPORT_CLKRUN_L 24
	FUNC_TEST=YES CLKLVDS_IN 19 22 37	FUNC_TEST=YES CHGNDA 38	FUNC_TEST=YES PCI_AD<22> 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DATA<7> 24 37	FUNC_TEST=YES KBD_CAPSLOCK_LED 23	FUNC_TEST=YES FANR_GND 25 38	FUNC_TEST=YES ROM_RW_L 9 12 24
	FUNC_TEST=YES CLKLVDS_LP 19 22 37	FUNC_TEST=YES SLEEP_LED 23 25	FUNC_TEST=YES PCI_AD<23> 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DATA<8> 24 37	FUNC_TEST=YES KBD_FUNCTION_L 23 30	FUNC_TEST=YES COMM_RTS_L 14 25	FUNC_TEST=YES ROM_ONBOARD_CS_L 9 24
FUNC_TEST=YES INT_I2C_CLK0 11 13 23	FUNC_TEST=YES LVDS_U0N 19 22 37		FUNC_TEST=YES PCI_AD<24> 9 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DATA<9> 24 37	FUNC_TEST=YES KBD_CONTROL_L 23 30	FUNC_TEST=YES FANL_GND 25 38	FUNC_TEST=YES ROM_CS_L 9 12 24
FUNC_TEST=YES INT_I2C_DATA0 11 13 23	FUNC_TEST=YES LVDS_U0P 19 22 37		FUNC_TEST=YES PCI_AD<25> 9 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DATA<10> 24 37	FUNC_TEST=YES KBD_COMMAND_L 23 30	FUNC_TEST=YES FANL_TACH 25	FUNC_TEST=YES CLK33M_AIRPORT 12 24 36
FUNC_TEST=YES INT_I2C_CLK1 13 14 25	FUNC_TEST=YES LVDS_U1N 19 22 37	FUNC_TEST=YES BT_USB_DM 14 24 37	FUNC_TEST=YES PCI_AD<26> 9 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DATA<11> 24 37	FUNC_TEST=YES KBD_OPTION_L 23 30	FUNC_TEST=YES FANR_PWM 25	FUNC_TEST=YES AIRPORT_IDSEL 24
FUNC_TEST=YES INT_I2C_DATA1 13 14 25	FUNC_TEST=YES LVDS_U1P 19 22 37	FUNC_TEST=YES BT_USB_DP 14 24 37	FUNC_TEST=YES PCI_AD<27> 9 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DATA<12> 24 37	FUNC_TEST=YES KBD_SHIFT_L 23 30	FUNC_TEST=YES FANL_PWM 25	FUNC_TEST=YES ROM_OE_L 9 12 24
FUNC_TEST=YES CBUS_DET_1_L 17	FUNC_TEST=YES LVDS_U2N 19 22 37	FUNC_TEST=YES MODEM_USB_DM 14 25 37	FUNC_TEST=YES PCI_AD<28> 9 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DATA<13> 24 37	FUNC_TEST=YES KBD_X<0> 23 30	FUNC_TEST=YES RJ45_DP<0> 27 37	FUNC_TEST=YES INT_MOD_DTI 14 25
FUNC_TEST=YES CBUS_DET_2_L 17	FUNC_TEST=YES LVDS_U2P 19 22 37	FUNC_TEST=YES MODEM_USB_DP 14 25 37	FUNC_TEST=YES PCI_AD<29> 9 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DATA<14> 24 37	FUNC_TEST=YES KBD_X<1> 23 30	FUNC_TEST=YES RJ45_DP<1> 27 37	FUNC_TEST=YES +24V_PBUS 38
FUNC_TEST=YES TMS_DN<0> 20 22 37	FUNC_TEST=YES CLKLVDS_UN 19 22 37	FUNC_TEST=YES PCI_AD<0> 9 12 17 24 26 37	FUNC_TEST=YES PCI_AD<30> 9 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DATA<15> 24 37	FUNC_TEST=YES KBD_X<2> 23 30	FUNC_TEST=YES RJ45_DP<2> 27 37	FUNC_TEST=YES GPU_VCORE 18 19 38
FUNC_TEST=YES TMS_DP<0> 20 22 37	FUNC_TEST=YES CLKLVDS_UP 19 22 37	FUNC_TEST=YES PCI_AD<1> 9 12 17 24 26 37	FUNC_TEST=YES PCI_AD<31> 9 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DMA_RQ 24 37	FUNC_TEST=YES KBD_X<3> 23 30	FUNC_TEST=YES RJ45_DP<3> 27 37	FUNC_TEST=YES MOD_BITCLK 14 25
FUNC_TEST=YES TMS_DN<1> 20 22 37	FUNC_TEST=YES LVDS_DDC_CLK 19 22	FUNC_TEST=YES PCI_AD<2> 9 12 17 24 26 37	FUNC_TEST=YES PCI_FRAME_L 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_RD_L 24 37	FUNC_TEST=YES KBD_X<4> 23 30	FUNC_TEST=YES RJ45_DP<4> 27 37	FUNC_TEST=YES MOD_CLKOUT 14 25
FUNC_TEST=YES TMS_DP<1> 20 22 37	FUNC_TEST=YES LVDS_DDC_DATA 19 22	FUNC_TEST=YES PCI_AD<3> 9 12 17 24 26 37	FUNC_TEST=YES PCI_TRDY_L 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_DMAACK_L 24 37	FUNC_TEST=YES KBD_X<5> 23 30	FUNC_TEST=YES RJ45_DP<5> 27 37	FUNC_TEST=YES VCORE_FB 34 38
FUNC_TEST=YES TMS_DN<2> 20 22 37	FUNC_TEST=YES BRIGHT_PWM 22	FUNC_TEST=YES PCI_AD<4> 9 12 17 24 26 37	FUNC_TEST=YES PCI_IRDY_L 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_ADDR<0> 24 37	FUNC_TEST=YES KBD_X<6> 23 30	FUNC_TEST=YES RJ45_DP<6> 27 37	FUNC_TEST=YES MOD_DTD 14 25
FUNC_TEST=YES TMS_DP<2> 20 22 37	FUNC_TEST=YES TV_GND1 22 38	FUNC_TEST=YES PCI_AD<5> 9 12 17 24 26 37	FUNC_TEST=YES PCI_DEVSEL_L 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_ADDR<1> 24 37	FUNC_TEST=YES KBD_X<7> 23 30	FUNC_TEST=YES RJ45_DP<7> 27 37	FUNC_TEST=YES +1.8V_MAIN 38
FUNC_TEST=YES TMS_CONN_CLKN 22 37	FUNC_TEST=YES TV_GND2 22 38	FUNC_TEST=YES PCI_AD<6> 9 12 17 24 26 37	FUNC_TEST=YES PCI_STOP_L 12 17 24 26 37	FUNC_TEST=YES EIDE_OPTICAL_ADDR<2> 24 37	FUNC_TEST=YES KBD_X<8> 23 30	FUNC_TEST=YES RJ45_DP<8> 27 37	FUNC_TEST=YES +3V_PMU 38
				FUNC_TEST=YES SND_AMP_MUTE 25	FUNC_TEST=YES SRCLK_TP 26	FUNC_TEST=YES RJ45_DP<9> 27 37	FUNC_TEST=YES SLEEP 23 25 30 33 35
				FUNC_TEST=YES SND_HP_MUTE_INV 25	FUNC_TEST=YES SRMOD_TP 26	FUNC_TEST=YES RJ45_DP<10> 27 37	FUNC_TEST=YES +5V_DDC_SLEEP 22 38
					FUNC_TEST=YES TEB_TP 26	FUNC_TEST=YES RJ45_DP<11> 27 37	FUNC_TEST=YES 1778_VFB 19 38
					FUNC_TEST=YES TEST_TP 26	FUNC_TEST=YES VCORE_VID0	FUNC_TEST=YES FW_TPODR 29 38
						FUNC_TEST=YES VCORE_VID1	FUNC_TEST=YES VCORE_VID0
						FUNC_TEST=YES VCORE_VID2	FUNC_TEST=YES VCORE_MUX_EN 34
						FUNC_TEST=YES VCORE_VID3	
						FUNC_TEST=YES VCORE_VID4	

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REVISION HISTORY

REV 0.01 - 03/06/2003

3/3
1) Initial check-in of Enterprise schematic after conversion to Concept 1.2
3/10
2) added 8 new 10uF vcore caps
3) added jumpers at 1.5V, 1.8V, 2.5V, 3.3V, 5V, and PBUS supply outputs
4) added 8 more 0.1uF vcore bypass caps
3/11
5) removed dedicated boot banger circuit (U5400,U5200,RP46,U9,U1000)
6) updated firmware to phy to rev A prt number
7) changed gpu PLL config to 1083/833
8) changed reset to U56 (clock slewing chip) to MAIN_RESET_L
9) changed C550 to 138S0536 to limit AVL
10) changed Vcore stuffing options to 1.4V/1.025V using analog mux to support slewing
11) changed stuffing to set Vcore offset to 0mV by default
12) changed comments to eliminate references to L3 in power supply section
3/18
13) changed stuffing options for GPU PCI ID to 0x319
14) changed R164 (DAC1RSET) to 107 ohm pulldown
15) added 10K pulldown to U43 pin A21
16) changed fan controller to AD77460
3/19
17) added pads for 0.1uF cap from +Adapter to digital gnd for EMC
18) added pads for 0 ohm between chassis and digital gnd near ENET connector for EMC
19) corrected path to correct for last checkin
20) removed BOM table for MAP31
21) REMOVED ALL RELATIVE_PROPAGATION_DELAY AND PROPAGATION_DELAY PROPERTIES TO PREPARE FOR CONSTRAINT_BACK_ANNOTATION
22) CHANGED CHRN ON R6 TO CHRN2
23) ***BOARD RENUMBERED***
3/28
24) integrated M10 pages from Q16 schematic and renumbered them
4/10
25) updated physical constraints for M10 power nets
26) added DP7 for M10 power sequencing
27) added RP27,RP28,RP32, and RP57 for TMDs series termination
28) update PLL CFG high 0010 1.25GHz low 1011 833MHz
29) update sscg/nosscg stuffing option on intrepid boot straps
30) removed D31 between +Batt and 24V_Pbus
31) add Vcore DAC resistors (R288,R289,R290,R292) for no mux case
32) change intrepid PLL LDO stuffing back to 1.8V main
33) change C640 and C646 to 0.01uF (Apple # 132S1047) for FW check config
34) change I2C pullups (R29 and R102) to 1K
35) changed bootrom part number to 341S1255
4/18
36) changed C756 to 128S0025 (Sanyo only 6.3V 330uF)
37) add pads for 90 ohm chokes to FNB path close to connector (route through the pads)
38) changed Vcore inductor (L36) to molded core part (152S0125)
39) changed Pbus inductor (L37) to molded core part (152S0126)
40) added separate 1.8V_GPU_TPVDV filter and LDO (U54)
4/21
41) replace discrete LCL with single chip LCL filters (155S0154) for VGA (L , L , and L)
42) add 165 ohm chokes on TMDs data pairs at connector (L , L , and L)
43) move BSI to bottom side
44) move CPU thermal sensor (Q39) to input 1 on fan controller and power supply sensor (Q66) to input 2
45) added trace from Vcore to fan controller ADC input
46) added FET inverters (Q78) to PWM outputs of fan controller (U3) to prevent spinup at boot
47) added FET (Q79) for +3V_Sleep for M10 power sequencing
4/27
48) changed TMDs data chokes to 90 ohm (155S0128)
49) changed C762 and C766 to 4.7uF 1206 caps
50) changed TMDs data chokes to 90 ohms (155S0128)
51) changed C762 and C766 to 4.7uF 1206
52) changed Q51 to SI7860DP (376S0119)
53) changed Q48 to SI7892DP (376S0120)
54) changed D24 to B340LB (371S0132)
55) changed L30 to 2.2uH Tokin inductor (152S0139)
56) added Q58, R307, and C515 for GPU Vcore control inverter
57) changed R416 to 2.2ohms
58) changed R364 to 102K
59) added 0.1uF 50V C883 to RS- of Max4172 (no stuff)
60) changed D18 to 1N914
61) changed L38 and L41 to 4.7uH (152S0137)
62) added Q81, R308, R309, and R310 for power sequencing (no stuff)
63) changed Q49 and Q50 to SI7860DP (376S0119)
64) changed L36 to 1.2uH 18.3K (152S0125)
65) added R331 1mohm sense resistor to CPU Vcore
66) added C885 and C884 , 1000uF CPU Vcore output caps
67) added Q82, R607, R455, R417, and C886 for 1.5V sleep sequencing
68) added Q83 and 100K R608 for 1.8V sequencing
69) added 15.4K R616 and 10K R672 for 2.5V switcher feedback divider
70) changed pinout of sound connector for sousaphone
71) removed Q44 (5V sound sleep fet)
72) changed Q31 to invert headphone Mute to sousaphone
4/28
73) changed CPU_VCORE_SLEEP location back to across bypass caps to correct after adding reference resistor
74) changed D5 to schottky diode (MBR0540)
75) fixed unnamed net (LTC3411_SHDN_SEQ)
76) changed drain/source polarity of Q76 (FET from +BATT to Pbus)
4/28
77) moved XW15 to connect to CPU_VCORE_SLEEP_UP (before positioning resistor)
78) changed fan control nets to FanL and FanR from Fan1 and Fan2
79) SWAPPED CONNECTIONS SO THAT OUTPUT 1 FROM FAN CONTROLLER CONNECTS TO LEFT FAN (CPU) AND FAN 2 CONNECTS TO THE RIGHT FAN (GPU)
80) updated power constraints with new fan net names
4/28
81) change Q58 on pg19 to Q80 to consolidate parts
82) CHANGED U55 TO MM1571J FOR COST SAVINGS
83) changed L72,L73,L74 to 90 ohm ferrites
84) added 10K pulldown to +5V_MAIN to SND_HP_MUTE
85) repinout Sousaphone connector
86) remove redundant pullups on FANL_TACH and FANR_TACH
87) added TP to all NC on NEC USB2 part for NAND tree testing
88) added NEC_USB_bomoption to 0 ohm resistor on NEC_AVSS_F
4/30
89) repinout Sousaphone connector (J12)
90) no stuff R322 to eliminate 3V_sleep pump up
91) updated various text notes with correct reference designators
5/1
92) change L30 to 152S0139 (Tokin CPI-1050-2R2) 11A
93) remove FANR_TACH functional test point
94) add CHGNDA and SLEEP_LED functional test points
95) swap INT_AUDIO_TO_SND and SND_TO_AUDIO on Sousaphone connector (J12)
*** rev 01 released for EVT ***
5/6
96) remove NO STUFF on R477 (set 5V and 3.3V switcher in pulse skipping mode)
97) change R337 to 470K and remove NO Stuff and no stuff R336 to change Vcore DAC to 1.35V/1.15V
98) change R321 to 499ohm to set 5mV Vcore offset
99) change L72,L73,L74 to 155S0165 (D part for EVT only)
*** rev 02 released for EVT ***
5/7
100) no stuff Q79 to disable 3V_SLEEP sequencing to work around wake from sleep bug with M10
101) added BOM table to define correct part number for M10 without heatspreader (338S0133)
*** rev 03 released for EVT ***

5/22
102) fixed NO STUFF BOM option for R291
103) add NO STUFF to R223 to correct startup level of GPU_VCORE_CNTL
104) add NO STUFF to R300 to complete 3V sequencing on wake from sleep fix
105) changed R376 to 158K and R321 to 2.74K to set CPU_VCORE offset to 35mV
*** rev 04 released for EVT ***
5/19/03
106) changed both AGP_NV_INT_L and AGP_ATI_INT_L to AGP_INT_L
107) removed redundant 3V_GPU pullup R687 (Intrepid side AGP_INT_L pullup)
108) added R699,R701,R707,R708 as 10K pulldowns to Intrepid USB ports A and C when NEC_USB is stuffed
109) changed SND_HP_MUTE_INV gate/inversion FETS to pullup to +3V_MAIN
110) added R711 as pullup to +3V_GPU on AUXWIN signal from M10 (U44)
111) added R698 as 0 ohm jumper between FW_PHY_PD and Intrepid
112) added U56, U57, R718,R714 for VGA Hsync and VGA Vsync buffering
113) changed L72,L73,L74 to 155S0164 (new high speed part)
114) added NO STUFF BOM option to R223 to correct for sense of GPU_VCORE_CNTL
115) added NO STUFF BOM option to R300 to avoid sleep wake problem
6/3/03
116) Integrated new 1.8V switcher (LTC3412)(U58)(353S0650) and inductor (L75- 152S0142)
117) changed 2.5V_SLEEP FET (U48) and 1.8V_SLEEP FET (U6) to higher current part (S16467BDQ - 376S0161)
118) added 10K pulldown (R720) on FW_PHY_PD_INT for when R698 is removed
119) changed R728 and R729 to 1210 Ohm resistors to support switching the entire memory bus between 1.8V and 2.5V
120) added R721 as jumper between +2.5V_SLEEP and +2.5V_GPU
6/4/03
121) NO STUFF R631 to remove MAIN_RESET_L from clock slewing chip
122) changed FNB connector to new part with extra ground tabs (514S0059)
6/5/03
123) changed I2C 0 and 1 pullups (RP12) to 2.2K to improve rise/fall times (sensor check config errors)
124) added CRITICAL files to new 1.8V switcher (U58), inductor (L75), 1.8V sleep FET (U6), and 2.5V sleep FET (48)
125) removed gnd caps (C651 and C647) on I2S clock at sound connector (J12)
126) added LC filter on SND_SYNC for EMI (L77 and C895)
127) added LC filter on SND_CLKOUT for EMI (80 and C899)
128) added LC filter on INT_AUDIO_TO_SND for EMI (L81 and C896)
129) added LC filter on SND_TO_AUDIO for EMI (L82 and C897)
130) added LC filter on SND_HP_MUTE for EMI (L78 and C898)
131) added LC filter on SND_HW_RESET_L for EMI (L78 and C900)
132) added LC filter on SND_SCLK for EMI (L79 and C901)
133) added C902 and R804 to prevent latch-up condition in GPU Vcore circuit when using powermiser
134) removed R331 (CPU Vcore positioning resistor)
135) changed C728,C729,C730,C731,C732,C733,C734,C884,C885 to 220uF Rubycon caps (128S0024)
136) add Vcore offset change circuit to modify offset in low (Q86,R805,R806,R807,R808,R809)
137) changed Q83 into dual (2N7002DW) and added R810 to invert 3V_5V_ON before switching RUN/SS
6/6/03
138) rotated J26 (FW B connector)
139) changed D29 to B340B (3A part - 371S0159)
6/9/03
140) modified Vcore offset select circuit with Takashi's changes - changed Gnd reference to VCORE_GND_SNS
141) added double inverter to buffer THERM_L_OC (added Q87,R811,R812)
142) removed redundant pullup on THERM_L_OC (R780)
6/9/03
143) added cap on gate of the second FET in Q87 for possible turn on delay (C903)
144) changed inner shield of FNB connector J26 to connect to chassis gnd
145) changed R326 and R325 to 0 ohm to set Vcore VID to 1.3V/1.15V
146) changed R321 to 2.49K to set Vcore offset to +25mV
147) added 10 ohm resistor (R814) and uF cap (C904) to filter power to ADT7460 (Gary Leo)
6/10/03
148) changed R612 to 10K to prevent UIDE_DMACK from floating
149) changed C80,C88,C81,C89,C82,C102,C79,C87 to NO STUFF (TMDs common-mode termination)
150) changed R205,R218,R211,R219,R210,R210,R220,R204,R214 to 162 ohm 1% (TMDs common-mode termination)
151) changed RP27,RP32,RP28,RP57 to 10ohm (TMDs series termination)
*** released for EVT2 6/10/03 ***
6/13/03
152) fixed NO STUFF on R291
153) removed NO STUFF from C80,C88,C81,C89,C82,C102,C79,C87 (TMDs common-mode termination)
154) removed NO STUFF from R638 (pullup on slewing chip FSEL)
155) removed NO STUFF from C903 (cap on input to second part of THERM_OC_L buffer)
156) CHANGED R321 TO 1K FOR VCORE OFFSET OF 12MV (VCORE = 1.30V -30MV/+100MV)
*** released for EVT2 6/13/03 ***
6/18/03
157) changed R228 to pullup to 1.8V for DVO interface compatibility
158) added R234 and INT_TMDs option to maintain internal TMDs capability
159) changed L30 to 3 pin symbol
160) added U5 to use as external TMDs transmitter (DVI)
161) added R41 to create +3V_GPU_SI power for SILL162 (U5)
162) added L14, C130, C132, and C165 for 3V AVCC filtering for SILL162 (U5)
163) added L13, C14, C129, C131, C133 for 3V PVCC filtering for SILL162 (U5)
164) added L15, C255, C233, C218 for 3V Vcc filtering for SILL162 (U5)
165) added R235 and R237 as options for MAIN_RESET_L to U5
166) added R231, R232, and C284 for Vref for U5
167) added R676, R99, R202, R212, R224, R88, R110, R223 as straps for U5
168) added RP58, RP59, RP60, RP61 for series termination of SILL162 TMDs output
169) added L16, C304, C327, C647 for filtering GPU_VDDR4
170) added R255 and R251 to strap GPU_DVDDMODE correctly for 1.8V DVO
171) added R268 to connect L16 to +3V_GPU_FLT when not using SILL162
172) added C681, C668, C678, C651 to filter the thermal sensor diff pairs
6/19/03
173) changed GPU_MEM_IO to +GPU_MEM to connect ATI Vref to correct memory voltage
174) swapped TMDs CLK and CLKP on RP57 and RP58 for layout
175) swapped DN<0> and DP<0> on RP27 for layout
176) corrected un-named nets in TMDs common-mode filters
177) added physical constraints for new Silicon Image power rails
178) CHANGED C728,C731,C734,C733,C730,C732,C729,C885,C885 TO 128S0022 (124S0024 WILL BE DELETED AS A DUPLICATE IN THE LIBRARY)
6/23/03
179) NO STUFF'ed C895,C899,C896,C897,C898,C900, and C901 to fix no sound problem
180) changed C890 to 100pF for improved transient response (Takashi)
181) Removed bypass traces on FNB chokes and stuffed L70 and L71
182) CHANGED R491 TO 52.3K 1%, R475 TO 127K 1%, AND R476 TO 4.7M 5% IN A29 ADAPTER DETECT CIRCUIT DIVIDERS TO REDUCE SHUTDOWN CURRENT
183) added R331 as CPU Vcore sense resistor (1 mohm 1% 2512)
184) NO STUFF'ed C651 and C678
185) added C688,C690,C846,C905 for thermal pair filtering at fan controller
186) added C906 to prevent shoot-thru on Q64 (currently NO STUFF'ed)
187) added C907 to prevent shoot-thru on Q68 (currently NO STUFF'ed)
188) changed R517 to 100K
189) changed GND reference for input side of Q86 to digital GND (the other FET in Q856 remains on VCORE_GNDSNS)
6/24/03
190) added C908 to prevent gate shoot-thru on Q56
191) added R279 to power TMDs PLL from LVDS filter when using external TMDs transmitter
192) changed R325 to 470K to set the low Vcore to 1.10V
193) stuffed Vcore offset switch (R807,R805,R809,Q86)
194) changed R809 to 1.5K 1% to set low Vcore offset to 10mV
195) changed R321 to 3.01K 1% to set high Vcore offset to 30mV
6/25/03
196) rotated L70 and L71 for layout (PCB symbol problem)
197) changed Q53,Q54,Q55 to IRF7832 (376S0148) for better thermal performance
198) NO STUFF'ed C908 (Q56 gate shoot-thru cap)
*** released for DVT 6/26/03 ***

7/2/03
199) CHANGED J9 (CARDBUS) TO 516S0141 (NEW PIN PLATING SPEC)
200) CHANGED J20 (AIRPORT) TO 516S0142 (NEW PIN PLATING SPEC)
201) CHANGED J10 (OPTICAL DRIVE) TO 516S0140 (NEW PIN PLATING SPEC)
202) CHANGED J13 (HARD DRIVE) TO 516S0140 (NEW PIN PLATING SPEC)
203) CHANGED J12 (SOUND) TO 516S0144 (NEW PIN PLATING SPEC)
204) CHANGED J8 (MODEM) TO 516S0143 (NEW PIN PLATING SPEC)
205) ADDED BOM TABLE TO PUT 0 OHM 402 ON L77,L80,L81,L82,L76,L78,L79
7/9/03
207) CORRECTED C889 TO CONNECT TO INPUT (PIN 1) OF U55
208) REMOVED POWER JUMPERS XW25,XW17,XW16,XW10,XW14,XW18
209) CHANGED 197S0035 TO PRIMARY AND 197S0004 AS ALTERNATE FOR Y1 (INTREPID)
210) CHANGED 197S0037 TO PRIMARY AND 197S0603 AS ALTERNATE FOR Y3 (ETHERNET)
211) CHANGED 197S0038 TO PRIMARY AND 197S0608 AS ALTERNATE FOR Y5 (NEC USB2)
212) CHANGED 197S0040 TO PRIMARY AND 197S0008 AS ALTERNATE FOR Y4 (LMU)
213) CHANGED 197S0041 TO PRIMARY AND 197S0604 AS ALTERNATE FOR Y6 (PMU)
7/22/03
214) ADDED 1_32V_VCORE AND 1_30V_VCORE BOM OPTIONS FOR 2 DIFFERENT CPU VCORE SPECS
215) UPDATED CAP MATERIAL TYPES
216) CHANGED FROM 715 PIN TO 667 PIN SYMBOL FOR U44 (M10)
7/28/03
217) CHANGED TMDs TERMINATION FROM 2X 162 TO 2X 49.9 OHMS PER PAIR
218) CHANGED 126S0036 FROM ALT TO PRIMARY, REPLACING 126S0035 FOR CPU VCORE INPUT CAPS
*** RELEASED FOR PRODUCTION 7/28/03 ***
8/4/03
219) CHANGED R99 TO NO STUFF TO FIX I2C ADDRESS OF SILL162 TMDs TRANSMITTER
220) CHANGED R321 TO 4.02K 1% FOR 1_30_VCORE (40MV OFFSET) AND TO 6.34K 1% FOR 1_32_VCORE (60MV OFFSET)
221) CHANGED R304 TO 470K AND R329 AND R325 TO 0 OHM TO CHANGE LOW VID TO 1.05V ON VCORE
222) CHANGED C611 TO 2200PF, C610 TO 100PF, AND R519 TO 12.7K 1% TO INCREASE IMMUNITY TO 3.3V PGOOD SIGNAL DROPOUT
223) NO STUFF C590 TO INCREASE IMMUNITY TO 3.3V PGOOD SIGNAL DROPOUT
224) CHANGED C583 TO 2200PF, C576 TO 100PF, AND R481 TO 15.0K 1% TO INCREASE IMMUNITY TO 3.3V PGOOD SIGNAL DROPOUT
225) NO STUFF C566 TO INCREASE IMMUNITY TO 3.3V PGOOD SIGNAL DROPOUT
9/4/03
228) ADDED 197S0052 AS ALTERNATE FOR G1 (98 MHZ FW OSCILLATOR)
229) CHANGED C728-C734,C884,C885 TO 128S0022 TO REMOVE DUPLICATE PART NUMBER
230) CHANGED C883 TO 132S0100 TO CORRECT FOR USE OF OEM PART NUMBER

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6531	B
SCALE	NONE	SHT	40 44

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D	<p>R371 RES 27</p> <p>R372 RES 26</p> <p>R373 RES 17</p> <p>R374 RES 31</p> <p>R375 RES 31</p> <p>R376 RES 14</p> <p>R377 RES 33</p> <p>R378 RES 33</p> <p>R379 RES 32</p> <p>R380 RES 27</p> <p>R381 RES 27</p> <p>R382 RES 27</p> <p>R383 RES 31</p> <p>R384 RES 34</p> <p>R385 RES 34</p> <p>R386 RES 9</p> <p>R387 RES 9</p> <p>R388 RES 19</p> <p>R389 RES 19</p> <p>R390 RES 19</p> <p>R391 RES 22</p> <p>R392 RES 32</p> <p>R393 RES 27</p> <p>R394 RES 31</p> <p>R395 RES 31</p> <p>R396 RES 31</p> <p>R397 RES 34</p> <p>R398 RES 14</p> <p>R399 RES 15</p> <p>R400 RES 22</p> <p>R401 RES 32</p> <p>R402 RES 32</p> <p>R403 RES 27</p> <p>R404 RES 27</p> <p>R405 RES 25</p> <p>R406 RES 27</p> <p>R407 RES 34</p> <p>R408 RES 34</p> <p>R409 RES 9</p> <p>R410 RES 19</p> <p>R411 RES 24</p> <p>R412 RES 27</p> <p>R413 RES 27</p> <p>R414 RES 31</p> <p>R415 RES 14</p> <p>R416 RES 19</p> <p>R417 RES 35</p> <p>R418 RES 35</p> <p>R419 RES 35</p> <p>R420 RES 35</p> <p>R421 RES 35</p> <p>R422 RES 35</p> <p>R423 RES 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<p>R689 RES 25</p> <p>R690 RES 22</p> <p>R691 RES 33</p> <p>R692 RES 25</p> <p>R693 RES 5</p> <p>R694 RES 23</p> <p>R695 RES 25</p> <p>R696 RES 23</p> <p>R697 RES 33</p> <p>R698 RES 14</p> <p>R699 RES 14</p> <p>R700 RES 33</p> <p>R701 RES 14</p> <p>R702 RES 8</p> <p>R703 RES 22</p> <p>R704 RES 22</p> <p>R705 RES 22</p> <p>R706 RES 33</p> <p>R707 RES 14</p> <p>R708 RES 14</p> <p>R709 RES 35</p> <p>R710 RES 25</p> <p>R711 RES 19</p> <p>R712 RES 35</p> <p>R713 RES 25</p> <p>R714 RES 25</p> <p>R715 RES 35</p>	<p>R716 RES 25</p> <p>R717 RES 25</p> <p>R718 RES 22</p> <p>R719 RES 26</p> <p>R720 RES 14</p> <p>R721 RES 31</p> <p>R722 RES 21</p> <p>R723 RES 25</p> <p>R724 RES 22</p> <p>R725 RES 26</p> <p>R726 RES 25</p> <p>R727 RES 35</p> <p>R728 RES 21</p> <p>R729 RES 21</p> <p>R730 RES 24</p> <p>R731 RES 33</p> <p>R732 RES 34</p> <p>R733 RES 27</p> <p>R734 RES 31</p> <p>R735 RES 27</p> <p>R736 RES 29</p> <p>R737 RES 29</p> <p>R738 RES 31</p> <p>R739 RES 31</p> <p>R740 RES 28</p> <p>R741 RES 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HPAK10PC2 23</p> <p>R843 HPAK10PC2 23</p> <p>R844 HPAK4D 25</p> <p>R845 HPAK4D 26</p> <p>R846 HPAK4D 14</p> <p>R847 HPAK4D 14</p> <p>R848 HPAK4D 14</p> <p>R849 HPAK4D 24</p> <p>R850 HPAK4D 24</p> <p>R851 HPAK4D 14</p> <p>R852 HPAK4D 23</p> <p>R853 HPAK4D 23</p> <p>R854 HPAK4D 26</p> <p>R855 HPAK4D 26</p> <p>R856 HPAK4D 14</p> <p>R857 HPAK4D 14</p> <p>R858 HPAK4D 20</p> <p>R859 HPAK4D 20</p> <p>R860 HPAK4D 20</p> <p>R861 HPAK4D 20</p> <p>R862 HPAK4D 20</p> <p>R863 HPAK4D 20</p> <p>R864 HPAK4D 20</p> <p>R865 HPAK4D 20</p> <p>R866 HPAK4D 20</p> <p>R867 HPAK4D 20</p> <p>R868 HPAK4D 20</p> <p>R869 HPAK4D 20</p> <p>R870 HPAK4D 20</p> <p>R871 HPAK4D 20</p> <p>R872 HPAK4D 20</p> <p>R873 HPAK4D 20</p> <p>R874 HPAK4D 20</p> <p>R875 HPAK4D 20</p> <p>R876 HPAK4D 20</p> <p>R877 HPAK4D 20</p> <p>R878 HPAK4D 20</p> <p>R879 HPAK4D 20</p> <p>R880 HPAK4D 20</p> <p>R881 HPAK4D 20</p> <p>R882 HPAK4D 20</p> <p>R883 HPAK4D 20</p> <p>R884 HPAK4D 20</p> <p>R885 HPAK4D 20</p> <p>R886 HPAK4D 20</p> <p>R887 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