1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
C		358886	PRODUCTION RELEASED	01/07/05	?

SCHEM,MLB,PB17"

01/07/2005

BOM OPTIONS	STUFF	NO STUFF
D3_HOT		✓
D3_COLD	✓	
GPU_SS	✓	
GPU_SWITCH	✓	
SERIAL_DEBUG		✓
VCORE_OFFSET	✓	
1_8V_MAXBUS	✓	
1_5V_MAXBUS		✓
NEC_USB	✓	
INTREPID_USB		✓
BBANG		✓
NO_BBANG		✓
ATI_MEMIO_HI	✓	
ATI_MEMIO_LO		✓
SSCG		✓
NO_SSCG	✓	
5V_HD_LOGIC	✓	
3V_HD_LOGIC		✓
EXT_TMDS	✓	
INT_TMDS		✓
MMM	✓	
INT_CLK	✓	
EXT_CLK		✓

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6694	1	SCHEM,MLB,PB17	SCH1	
820-1688	1	PCBF,MLB,PB17	PCB1	

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES °
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

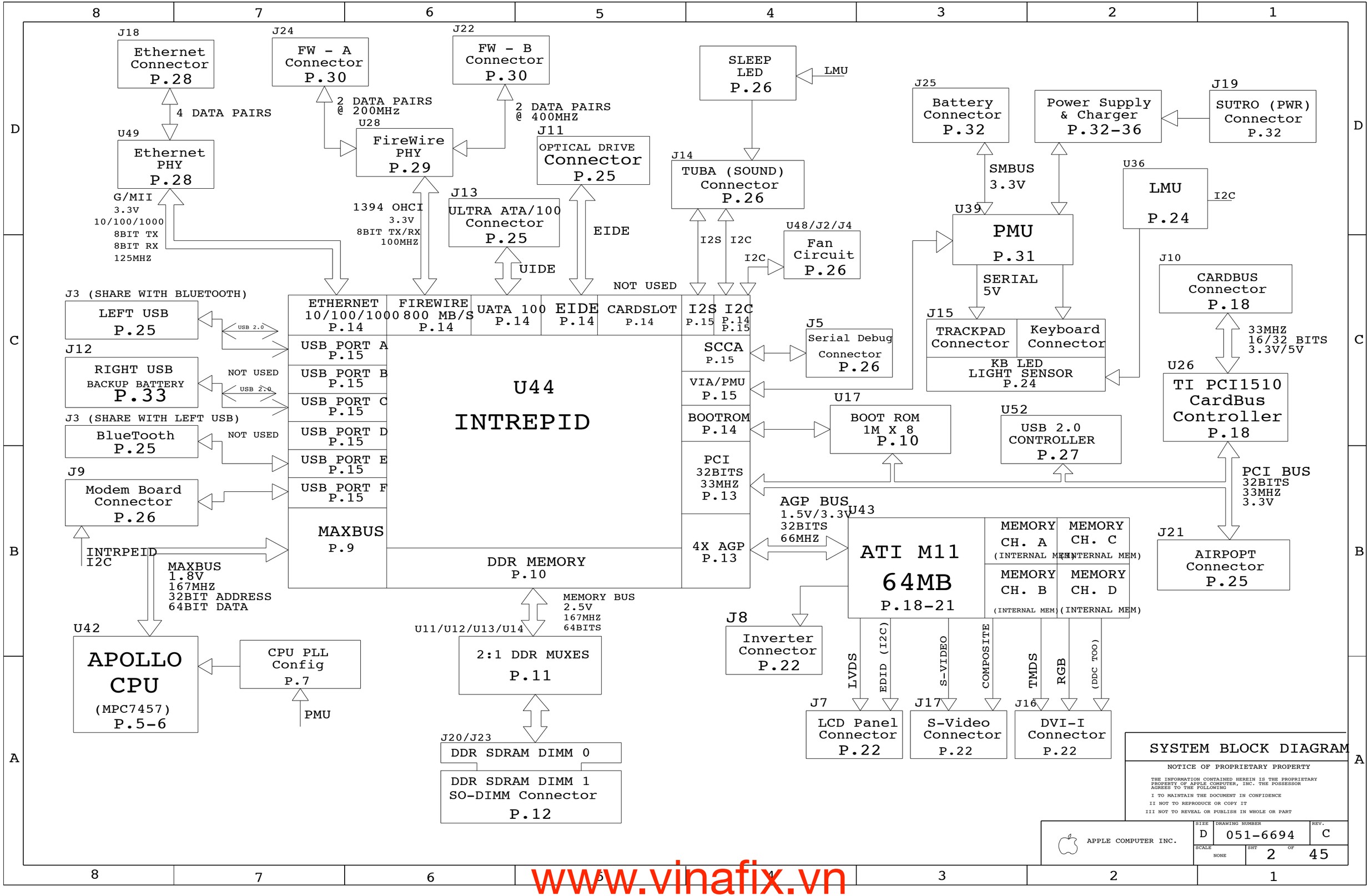
DRAFTER / DESIGN CK / ENG APPD / MFG APPD / QA APPD / DESIGNER / RELEASE / SCALE NONE
MATERIAL/FINISH NOTED AS APPLICABLE
SIZE D

Apple Computer Inc.

TITLE
SCHEM,MLB,PB17"

DRAWING NUMBER 051-6694 REV. C

SHT 1 OF 45



POWER SYSTEM ARCHITECTURE

AC ADAPTER IN PG 31

INRUSH LIMITER PG 30

+24V_PBUS

1V20_REF

>-13.44V TURNS-ON
<-13.44V SHUTS-OFF

U21 PG 31

RUN/SS

BUCK VCC REGULATOR (LTC1625) PG 32

AC: 12.8V
NO AC: BATTERY VOLTAGE
1625 NOT RUNNING

SHUTDOWN: RUNNING
SLEEP: RUNNING
RUN: RUNNING

+PBUS (12.8V)

BACKLIGHT INVERTER

+5V_MAIN

VCC MAIN 2.5V/1.5V DC/DC (MAX1715) PG 35

SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING

TURNS ON OUTPUT @ 2.4V
ON1/ON2

PGOOD 1_5V_2_5V_OK

MAP31 DDR I/O
MAP31 DDR CORE
DDR POWER

+2.5V_MAIN

+1.5V_MAIN

INTREPID CORE
AGP I/O

+PBUS

DCDC_EN
SLEEP

MAXBUS SEQUENCING

+5V_MAIN

VCC SHDN

DC/DC (MAX1717) PG 34

SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING

CPU_VCORE (+1.4V/+1.5V)

14V_PBUS

+3V_PMU LDO PG 32

+5V_MAIN
+3V_PMU
+4_6V_BU

+BATT

DCDC_EN_L

AFTER PMU IS UP AND RUNNING
DCDC_EN_L WILL PULL ON1/ON2
LOW IN SHUTDOWN

RC AT 1M*0.047UF @ 24V
STARTS 2.0MSEC AFTER DCDC_EN_L BECOMES LOW

RUN/SS - 5V
TURNS ON AT >1V
<100UA ALLOWED
INTERNAL ZENER CLAMP TO 6V

MAIN 3V/5V DC/DC (LTC3707) PG 33

VCC STBYMD

SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING

INTERNAL ZENER CLAMP TO 6V
<100UA ALLOWED
TURNS ON AT >1V
RUN/SS - 3V

+5V_MAIN

PGOOD 3V_5V_OK

HOLDS BOTH RUN/SS AT GND
WHEN IT'S CONNECTED TO GND

TURNS CONTROL TO RUN/SS
WHEN IT'S OPEN

+3.3V_MAIN

+PBUS (12.8V)

+5V_MAIN

VCC EXT_VCC DC/DC (LTC1778) PG 20

SHUTDOWN: STOPPED
SLEEP: D3HOT/D3COLD
RUN: RUNNING

TURNS ON AS LOW AS 0.8V/TYP 1.5V
INTERNAL 1.2UA CURRENT SOURCE

RUN/SS

GPU_VCORE +1.2V/+1.0V

DCDC_EN
SLEEP

D3_COLD

GPU_VCORE SEQUENCING

1M & 0.1UF @14V, IT TAKES
~5.88MS TO START SWITCHER

1_5V_2_5V_OK

D3_HOT

DCDC_EN_L
D3_HOT

1_5V_2_5V_OK WILL NOT PULL LOW UNTIL
+5V_MAIN TURNS ON

HOWEVER, 5V SHOULD TURN ON ~2.23MS AFTER
DCDC_EN_L OR PMU_POWERUP_L
BECOMES '1'; MUCH LESS THAN THE
RC CHARGING AT INT_VCC (5V)

+PBUS

BACKUP BATTERY

CHARGER INPUT & BOOST OUTPUT PG 32

12.8V CHARGES BACKUP BATTERY

24V IS OUTPUT ONLY FROM BACKUP BATTERY

BACKUP BATTERY CIRCUIT CHARGES OFF +PBUS
AND PREVENTS +PBUS AND +24V_PBUS FROM DROPPING BELOW 6V
(UNTIL DRAINED)

RC AT 1M*0.1UF @ 24V
STARTS ~4.25MSEC AFTER DCDC_EN_L BECOMES LOW

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

+24V_PBUS

DC/DC (LTC3411) PG 35

+1.8V_MAIN

MAXBUS BROADCOM

SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING

BATTERY CHARGER (MAX1772) PG 31

+BATT

3S 3P PRISMATIC CELLS

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

BATTERY VOLTAGE FEED-IN PATH PG 31

+PBUS

SHUT-DOWN RUN SLEEP RUN SHUT-DOWN

SLEEP
SLEEP_L_LS5
DCDC_EN
DCDC_EN_L
+5V_MAIN ~11MS
+5V_SLEEP
+3V_MAIN ~13.5MS
+3V_SLEEP
3V_5V_OK 2.4V - ??? MS
+2_5V_MAIN 2.6 MS
+2_5V_SLEEP
+1_5V_MAIN 2.6 MS
+1_5V_SLEEP
1_5V_2_5V_OK (MAX1715 OUTPUT)
1_5V_2_5V_OK (AT LTC1778 RUN/SS)
GPU_VCORE (D3HOT) ~???MS
GPU_VCORE (D3COLD)
+1_8V_MAIN 1.9 MS

POWER BLOCK DIAGRAM

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	C
SCALE: NONE	SHT 3 OF 45	

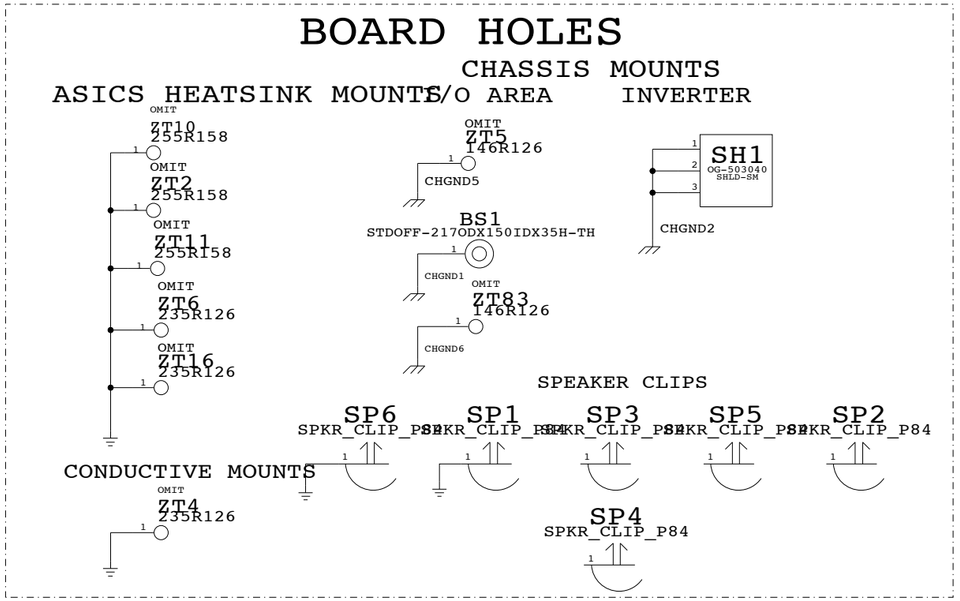
PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 12
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD HOLES

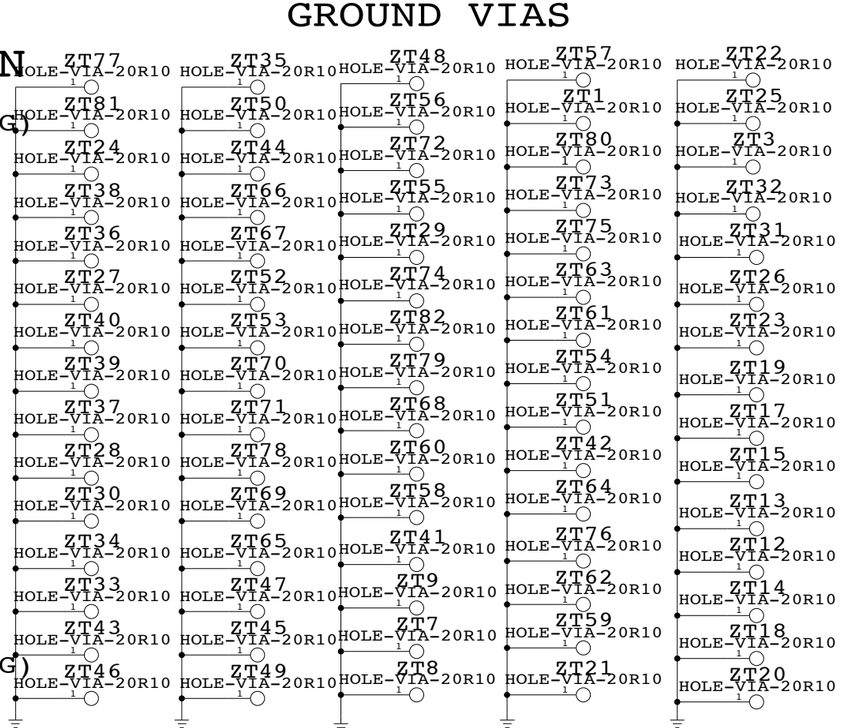


BOARD STACK-UP AND CONSTRUCTION

20R10 TH VIA OR VIA IN PAD

1		SIGNAL (1/3 OZ + COPPER PLATING)
2	PREPREG (3MIL)	GROUND (1/2 OZ)
3	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
4	PREPREG (3MIL)	SIGNAL (1/2 OZ)
5	LAMINATE (4MIL)	GROUND (1/2 OZ)
6	PREPREG (2MIL)	CUT POWER PLANE(1 OZ)
7	LAMINATE (3MIL)	CUT POWER PLANE(1 OZ)
8	PREPREG (2MIL)	GROUND (1/2 OZ)
9	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
10	PREPREG (3MIL)	SIGNAL (1/2 OZ)
11	LAMINATE (4MIL)	GROUND (1/2 OZ)
12	PREPREG (3MIL)	SIGNAL (1/3 OZ + COPPER PLATING)

GROUND VIAS

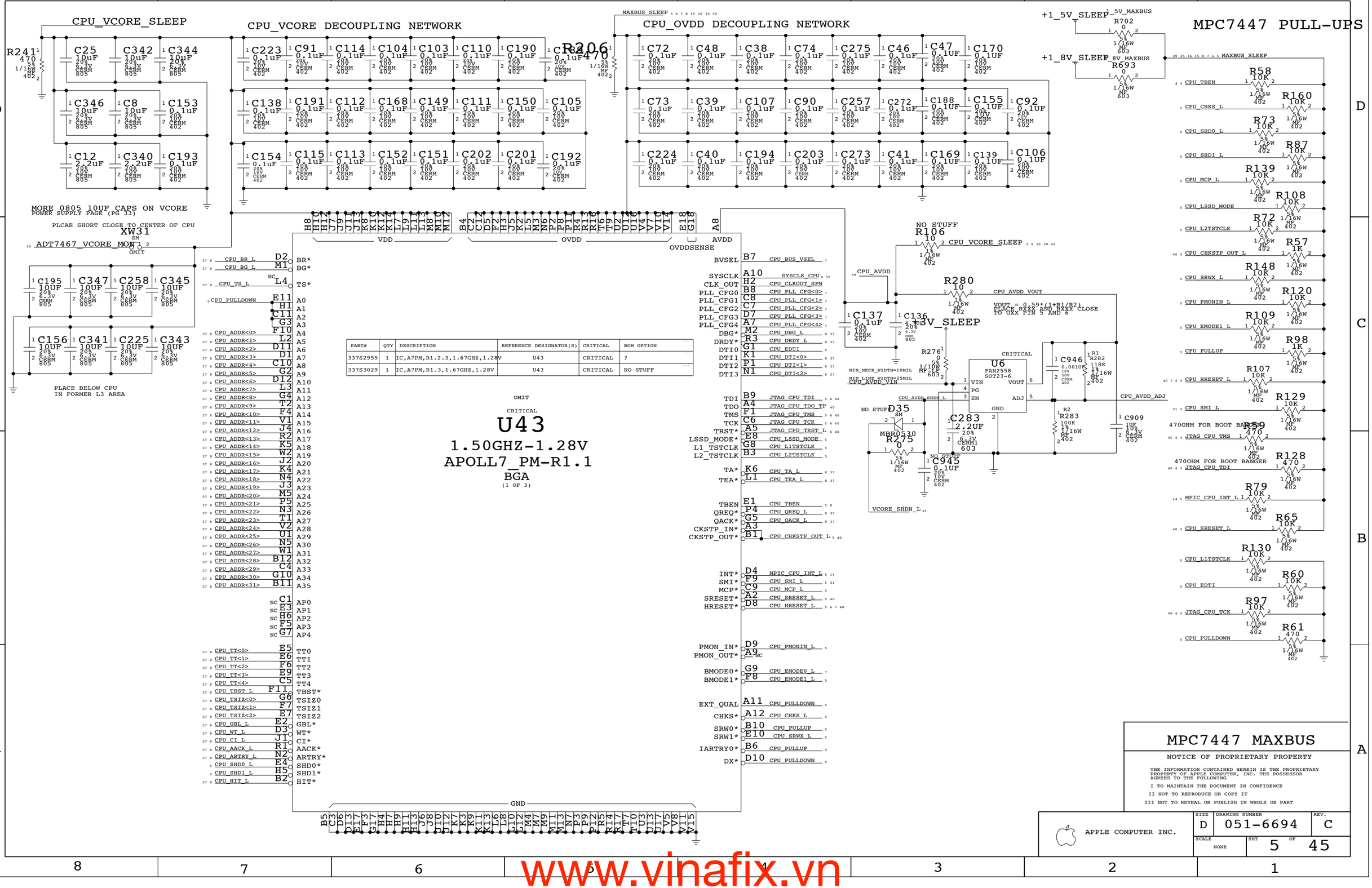


BOARD INFORMATION

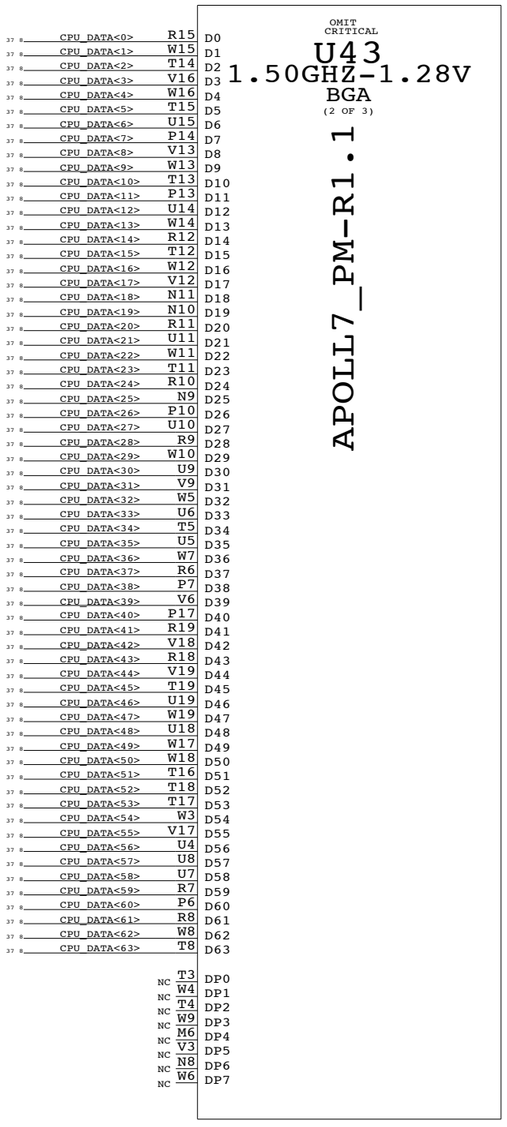
APPLE COMPUTER INC.

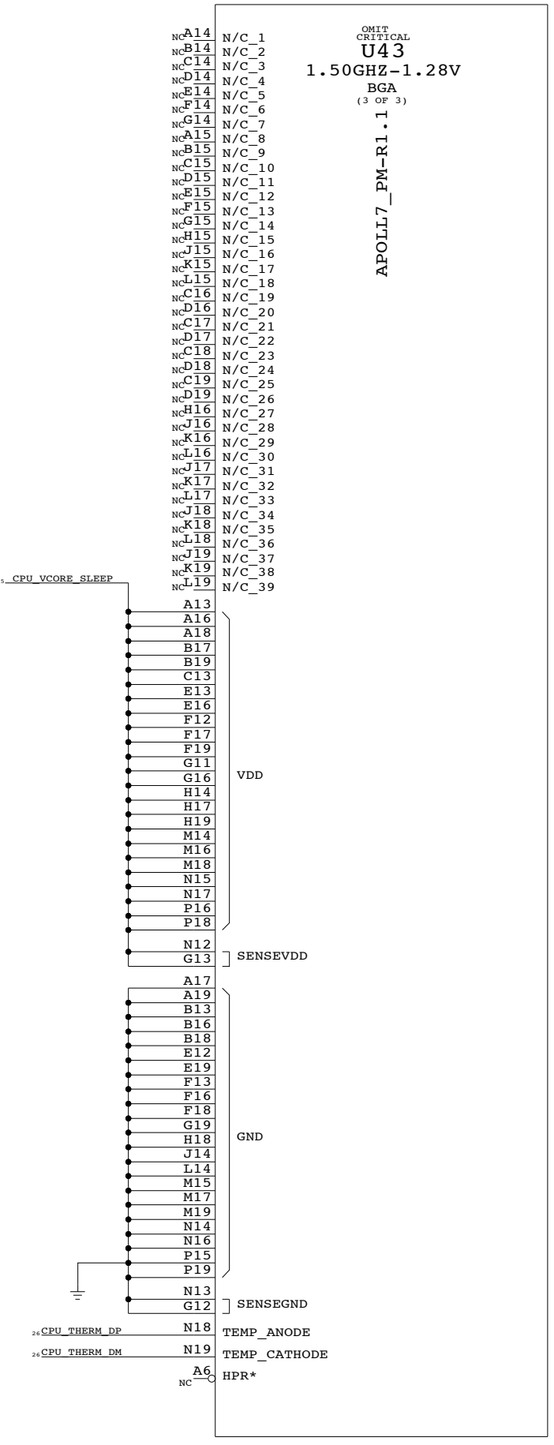
SIZE	DRAWING NUMBER	REV.
D	051-6694	C

SCALE: NONE | SHT 4 OF 45

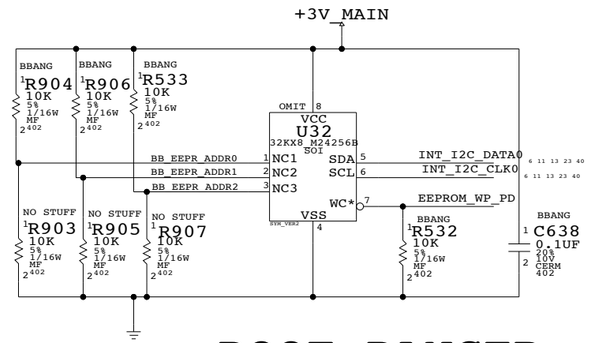


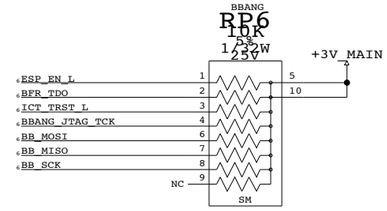
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S2955	1	IC,A7PM,R1.2.3,1.67GHZ,1.28V	U43	CRITICAL	?
337S3029	1	IC,A7PM,R1.3,1.67GHZ,1.28V	U43	CRITICAL	NO STUFF



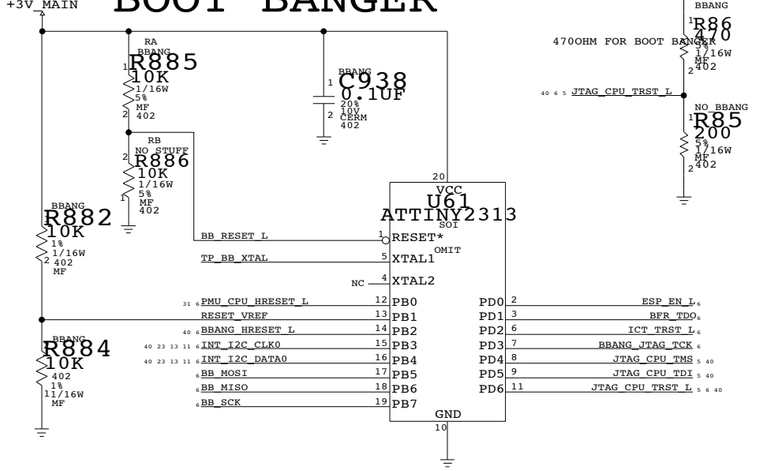


BOOT BANGER E2PROM



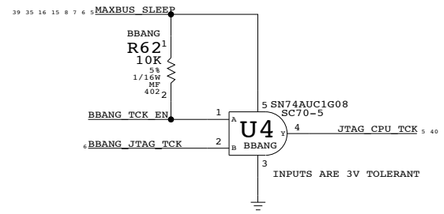


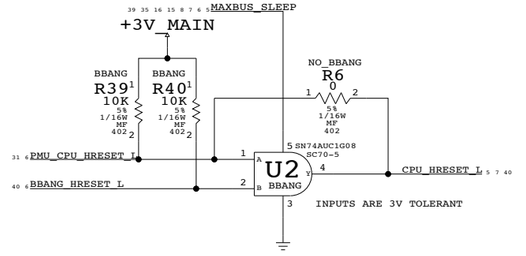
BOOT BANGER



UNSTUFFING RA AND STUFFING RB
WILL DISABLE THE CONTROLLER

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1660	1	MCU,PROGRAMMED W/ BANGER	U61	BBANG
341S1661	1	I2C EEPROM,PROGRAMMED W/ BANGER	U32	BBANG





BOOT BANGING SIGNAL DEFINITION

1/ BBANG_HRESET_L (OPEN COLLECTOR OUTPUT - 10K PULLUP ON MLB)
2/ PMU_HRESET_L (3V INPUT INTO LMU)
3/ BBANG_JTAG_TCK (REGULAR OUTPUT)
4/ JTAG_CPU_TMS (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
5/ JTAG_CPU_TDI (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
6/ JTAG_CPU_TRST_L (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)

MPC7447/BBANG

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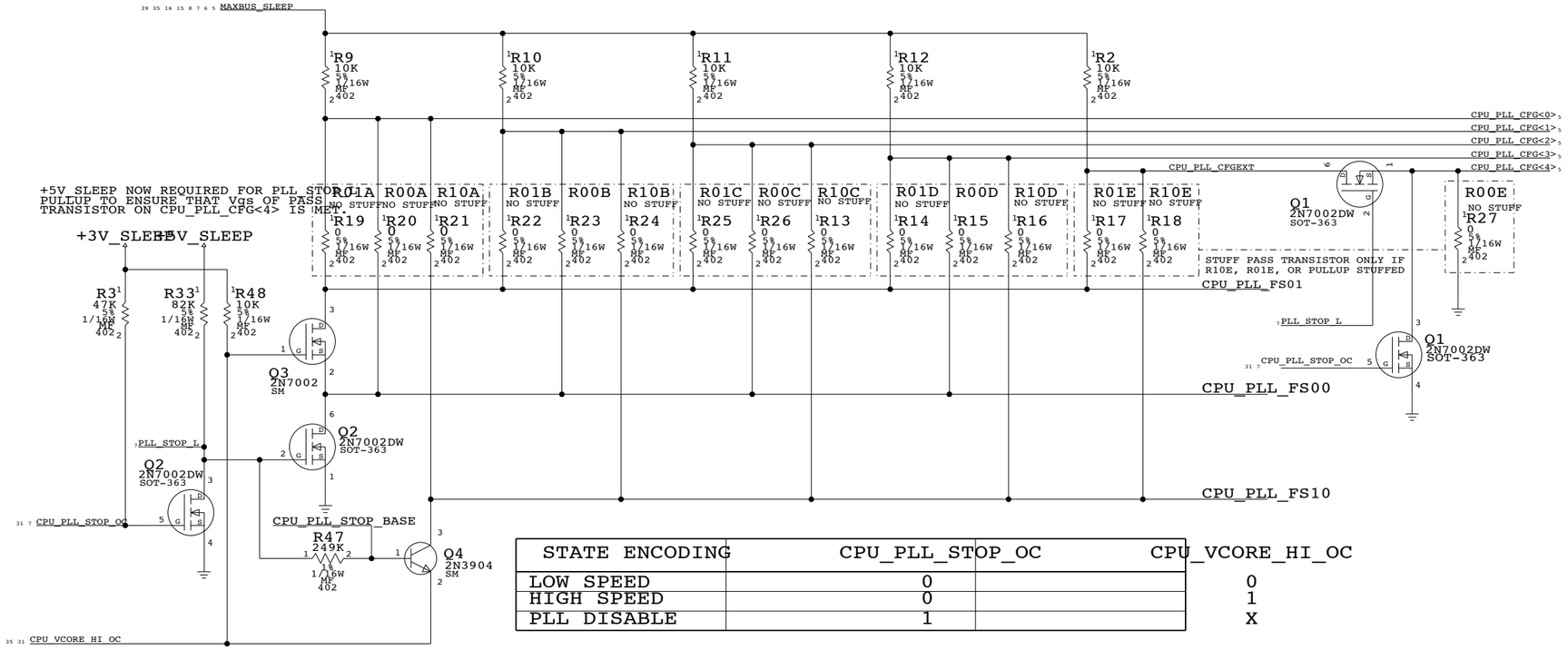
D	051-6694	C
SCALE: NONE	SHT 6 OF 45	

CPU PLL CONFIG CIRCUITRY



STATE ENCODING	CPU_PLL_STOP_OC		CPU_VCORE_HI_OC
LOW SPEED	0		0
HIGH SPEED	0		1
PLL DISABLE	1		X

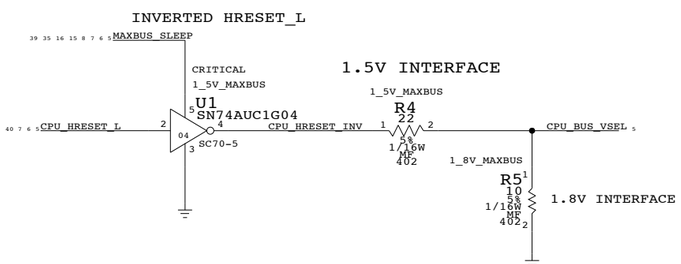
CPU FREQUENCY CONFIGURATION

APOLLO 7

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ (MHZ)	133MHZ	CPU_PLL_CFG 4 0123 E ABCD HEX
0.0X	PLL OFF		0 1111 0F
1.0X	PLL BYPASS		0 0011 03
2.0X	333	267	0 0100 04
3.0X	500	400	0 1000 08
4.0X	667	533	0 1010 0A
5.0X	833	667	0 1011 0B
5.5X	917	733	0 1001 09
6.0X	1000	800	0 1101 0D
6.5X	1083	867	0 0101 05
7.0X	1167	933	0 0010 02
7.5X	1250	1000	0 0001 01
8.0X	1333	1067	0 1100 0C
8.5X	1417	1133	0 0110 06
9.0X	1500	1200	1 0111 17
9.5X	1583	1267	0 0111 07
10.0X	1667	1333	1 1010 1A
10.5X	1750	1400	1 1000 18
11.0X	1833	1467	1 1001 19
11.5X	1917	1533	0 0000 00
12.0X	2000	1600	1 1011 1B
12.5X	2083	1667	1 1111 1F
13.0X	2167	1733	1 0101 15
13.5X	2250	1800	0 1110 0E
14.0X	2333	1867	1 1100 1C
15.0X	2500	2000	1 0001 11
16.0X	2667	2133	1 1101 1D
17.0X	2833	2267	1 0000 10
18.0X	3000	2400	1 0010 12
20.0X	3333	2667	1 0011 13
21.0X	3500	2800	1 0100 14
24.0X	4000	3200	1 0110 16
28.0X	4667	3733	1 1110 1E

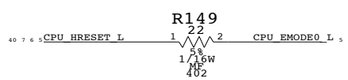
CPU CONFIGURATION

MAXBUS VSEL



DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L NEED TO CHARACTERIZE

BUSTYPE SELECT



APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	C
SCALE: NONE	SHT 7 OF 45	

INTREPID BOOT STRAPS

BIT 32 TO 39

MAXBUS_SLEEP

R642	R135	R123	R153	R166	R179	R651	R178
NO STUFF	NO STUFF	NO STUFF		NO STUFF	NO STUFF	NO STUFF	NO STUFF
CPU_DATA<32>	CPU_DATA<33>	CPU_DATA<34>	CPU_DATA<35>	CPU_DATA<36>	CPU_DATA<37>	CPU_DATA<38>	CPU_DATA<39>

R136	R643	R639	R657	R664	R673	R143	R674
			NO STUFF				
Output Mode 0: Tri-State 1: Active	Output Slew Rate 0: Fast 1: Reduced	Output Drive Strength 0: Full 1: Reduced	Spare	Spare	Spare	Spare	Spare

BIT 40 TO 47

MAXBUS_SLEEP

R122	R142	R164	R134	R184	R177	R152	R165
NO STUFF	NO STUFF	NO STUFF	EXT_CLK	NO STUFF	INT_CLK	INT_CLK	INT_CLK
CPU_DATA<40>	CPU_DATA<41>	CPU_DATA<42>	CPU_DATA<43>	CPU_DATA<44>	CPU_DATA<45>	CPU_DATA<46>	CPU_DATA<47>

R640	R652	R665	R644	R683	R675	R658	R666
			INT_CLK		EXT_CLK	EXT_CLK	EXT_CLK
Spare	Spare	BIT2	BIT1	BIT0	Input Clock Frequency 0: 100MHz 1: 133MHz	PCI1 Source Clock 0: PLL5 (NO SPREAD) 1: PLL5 (NO SPREAD)	PCI0 Source Clock 0: PLL5 (NO SPREAD) 1: PLL5 (NO SPREAD)

PLL4MODESEL_NXT[2:0]
000: 166.4MHZ (2.5X)
001: 149.76MHZ
010: 133.12MHZ (2.0X)
011: 99.84MHZ (1.5X)
100: 83.20MHZ

MODE A (2.5X) IS FOR STATIC OPERATION
MODE C (2.0X) IS FOR CLOCK SLEEP OPERATION

BIT 48 TO 55

MAXBUS_SLEEP

R133	R121	R163	R151	R162	R141	R183	R176
EXT_CLK	EXT_CLK		NO STUFF	NO STUFF	NO STUFF		NO STUFF
CPU_DATA<48>	CPU_DATA<49>	CPU_DATA<50>	CPU_DATA<51>	CPU_DATA<52>	CPU_DATA<53>	CPU_DATA<54>	CPU_DATA<55>

R645	R641	R668	R659	R667	R653	R684	R676
INT_CLK	INT_CLK	NO STUFF				NO STUFF	
Buf Ref Clk Output Enable_h 1: Active	Select 14.31818MHz Ext Source 1: External source	Spare	BIT2	BIT1	BIT0	Spare	

1394b workaround 1: 1394b workaround

MaxBus output impedance
111: 28.6 ohm
011: 33.3 ohm
101: 40 ohm
001: 50 ohm
110: 66.6 ohm
010: 100 ohm
100: 200 ohm
000: 200 ohm

THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:
1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
2/ D46 - SELPCI1SPREADCLK - SLEEP/WAKE CYCLE REQUIRED
3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT

IF A STRAP IS NOT LISTED, THEN
IT CANNOT BE CHANGED BY SOFTWARE

+1_5V_INTREPID_PLL — R227 4.7 5% 1/16W MF 402 — +1_5V_INTREPID_PLL7
C308 0.22UF 20% 6.3V CERM 2 402

H26

U45 INTREPID-REV2.1 BGA (1 OF 9)

CPU_BR_L	E29	BR	INPUT
CPU_BG_L	E26	BG	NO BUS KEEPER
CPU_TS_L	B27	TS	NO BUS KEEPER
CPU_ADDR<0>	D24	A_0	
CPU_ADDR<1>	D25	A_1	
CPU_ADDR<2>	A27	A_2	
CPU_ADDR<3>	E24	A_3	
CPU_ADDR<4>	G23	A_4	
CPU_ADDR<5>	B26	A_5	
CPU_ADDR<6>	A26	A_6	
CPU_ADDR<7>	D23	A_7	
CPU_ADDR<8>	A25	A_8	
CPU_ADDR<9>	E23	A_9	
CPU_ADDR<10>	J22	A_10	
CPU_ADDR<11>	B25	A_11	
CPU_ADDR<12>	H22	A_12	
CPU_ADDR<13>	G22	A_13	
CPU_ADDR<14>	D22	A_14	
CPU_ADDR<15>	B24	A_15	
CPU_ADDR<16>	B23	A_16	
CPU_ADDR<17>	E22	A_17	
CPU_ADDR<18>	J21	A_18	
CPU_ADDR<19>	G21	A_19	
CPU_ADDR<20>	E21	A_20	
CPU_ADDR<21>	A24	A_21	
CPU_ADDR<22>	D21	A_22	
CPU_ADDR<23>	A23	A_23	
CPU_ADDR<24>	H20	A_24	
CPU_ADDR<25>	B22	A_25	
CPU_ADDR<26>	H21	A_26	
CPU_ADDR<27>	A22	A_27	
CPU_ADDR<28>	E20	A_28	
CPU_ADDR<29>	B21	A_29	
CPU_ADDR<30>	D20	A_30	
CPU_ADDR<31>	A21	A_31	
CPU_CI_L	G26	CI	
CPU_GBL_L	A29	GBL	
CPU_TBST_L	A28	TBST	
CPU_TSIZ<0>	G24	TSIZ_0	
CPU_TSIZ<1>	H24	TSIZ_1	
CPU_TSIZ<2>	D26	TSIZ_2	
CPU_TT<0>	E25	TT_0	
CPU_TT<1>	G25	TT_1	
CPU_TT<2>	B28	TT_2	
CPU_TT<3>	D27	TT_3	
CPU_TT<4>	J25	TT_4	
CPU_WT_L	D28	WT	
CPU_AACK_L	B29	AACK	NO BUS KEEPER - PU
CPU_ARTRY_L	H23	ARTRY	NO BUS KEEPER - PU
CPU_HIT_L	B31	HIT	INPUT - PU
CPU_QREQ_L	A32	QREQ	INPUT - PD
CPU_QACK_L	G27	QACK	NO BUS KEEPER - ?
INT_SUSPEND_REQ_L	AK9	SUSPENDREQ	
INT_SUSPEND_ACK_L	AM8	SUSPENDACK	
INT_CPUFB_IN	J24	CPU_FB_IN	
INT_CPUFB_OUT	H16	CPU_FB_OUT	
SYSCLK_LA_TP	G8	ANALYZER_CLK	
CPU_CLK_EN	AH9	STOPCPUCLK	INPUT - PU
INTREPID_ACS_REF	H13	ACS_REF	NO BUS KEEPER - PU
SYSCLK_CPU_UF	J15	CPU_CLK	NO BUS KEEPER - PU
CPU_TBEN	A31	TBEN	NO BUS KEEPER - PU

CPU_DATA<0>	D10	D_0	
CPU_DATA<1>	G12	D_1	
CPU_DATA<2>	E11	D_2	
CPU_DATA<3>	H11	D_3	
CPU_DATA<4>	B9	D_4	
CPU_DATA<5>	B8	D_5	
CPU_DATA<6>	A9	D_6	
CPU_DATA<7>	A8	D_7	
CPU_DATA<8>	E12	D_8	
CPU_DATA<9>	D11	D_9	
CPU_DATA<10>	B10	D_10	
CPU_DATA<11>	J13	D_11	
CPU_DATA<12>	A10	D_12	
CPU_DATA<13>	D12	D_13	
CPU_DATA<14>	E13	D_14	
CPU_DATA<15>	G13	D_15	
CPU_DATA<16>	B11	D_16	
CPU_DATA<17>	D13	D_17	
CPU_DATA<18>	A11	D_18	
CPU_DATA<19>	G14	D_19	
CPU_DATA<20>	H14	D_20	
CPU_DATA<21>	E14	D_21	
CPU_DATA<22>	B12	D_22	
CPU_DATA<23>	G15	D_23	
CPU_DATA<24>	B13	D_24	
CPU_DATA<25>	H15	D_25	
CPU_DATA<26>	D14	D_26	
CPU_DATA<27>	B14	D_27	
CPU_DATA<28>	A12	D_28	
CPU_DATA<29>	G16	D_29	
CPU_DATA<30>	E15	D_30	
CPU_DATA<31>	J16	D_31	
CPU_DATA<32>	D15	D_32	
CPU_DATA<33>	A14	D_33	
CPU_DATA<34>	A13	D_34	
CPU_DATA<35>	D16	D_35	
CPU_DATA<36>	E16	D_36	
CPU_DATA<37>	G17	D_37	
CPU_DATA<38>	B15	D_38	
CPU_DATA<39>	H17	D_39	
CPU_DATA<40>	A15	D_40	
CPU_DATA<41>	B16	D_41	
CPU_DATA<42>	E17	D_42	
CPU_DATA<43>	A16	D_43	
CPU_DATA<44>	J18	D_44	
CPU_DATA<45>	H18	D_45	
CPU_DATA<46>	D17	D_46	
CPU_DATA<47>	G18	D_47	
CPU_DATA<48>	A17	D_48	
CPU_DATA<49>	B17	D_49	
CPU_DATA<50>	E18	D_50	
CPU_DATA<51>	B18	D_51	
CPU_DATA<52>	D18	D_52	
CPU_DATA<53>	A18	D_53	
CPU_DATA<54>	A19	D_54	
CPU_DATA<55>	H19	D_55	
CPU_DATA<56>	B19	D_56	
CPU_DATA<57>	J19	D_57	
CPU_DATA<58>	A20	D_58	
CPU_DATA<59>	D19	D_59	
CPU_DATA<60>	E19	D_60	
CPU_DATA<61>	G19	D_61	
CPU_DATA<62>	B20	D_62	
CPU_DATA<63>	G20	D_63	
CPU_DBG_L	A30	DBG	
CPU_DRDY_L	G28	DRDY	
CPU_DTI<0>	K25	DTI_0	
CPU_DTI<1>	D29	DTI_1	
CPU_DTI<2>	B30	DTI_2	
CPU_TA_L	E27	TA	
CPU_TEA_L	E28	TEA	

MAXBUS INTERFACE

INTREPID OUTPUTS HIGH BY DEFAULT

VDD15A_7 (PLL6) OMIT CRITICAL
H25

FB BUFFER HAS 50 OHM OUTPUT IMPEDANCE

R197 511 1% 1/16W MF 402 — R144 0 5% 1/16W MF 402 — SYSCLK_CPU1 — R137 1K 1% 1/16W MF 402

Vin = Intrepid Vcore (1.5V)
Vout = MaxBus rail (1.8V)

SHORT = 1" SHORTER THAN MATCHED LENGTH
LONG = 1" LONGER THAN MATCHED LENGTH

INT_CPUFB_OUT — R167 0 5% 1/16W MF 402 — INT_CPUFB_OUT_SHORT — R215 0 5% 1/16W MF 402 — INT_CPUFB_OUT_NORM — R207 NO STUFF 0 5% 1/16W MF 402 — INT_CPUFB_LONG

R225 NO STUFF 0 5% 1/16W MF 402 — R208 0 5% 1/16W MF 402 — NO STUFF

INT_CPUFB_IN — R226 0 5% 1/16W MF 402 — INT_CPUFB_IN_NORM — R196 0 5% 1/16W MF 402

MAXBUS PULL-UPS

MAXBUS_SLEEP

CPU_TS_L	RP21 10K 5% 1/16W SM1	2 7
CPU_TA_L	RP21 10K 5% 1/16W SM1	1 8
CPU_ARTRY_L	RP21 10K 5% 1/16W SM1	4 5
CPU_BR_L	RP23 10K 5% 1/16W SM1	1 8
CPU_HIT_L	RP24 10K 5% 1/16W SM1	3 6
CPU_DRDY_L	RP23 10K 5% 1/16W SM1	3 6
CPU_TEA_L	RP23 10K 5% 1/16W SM1	4 5
CPU_AACK_L	RP23 10K 5% 1/16W SM1	2 7
CPU_DBG_L	RP24 10K 5% 1/16W SM1	4 5
CPU_BG_L	RP21 10K 5% 1/16W SM1	3 6
CPU_QREQ_L	RP24 10K 5% 1/16W SM1	2 7

INTREPID BOOT STRAPS

BIT 56 TO 63

MAXBUS_SLEEP

R140	R161	R175	R132	R131	R150	R174	R182
NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF		NO STUFF
CPU_DATA<56>	CPU_DATA<57>	CPU_DATA<58>	CPU_DATA<59>	CPU_DATA<60>	CPU_DATA<61>	CPU_DATA<62>	CPU_DATA<63>

R654	R669	R677	R646	R647	R660	R678	R685
						NO STUFF	
Spare	Spare	Spare	PCI1_REQ2_L / PCI1_GNT2_L 0: GPIO5 1: GPIO5	PCI1_REQ1_L / PCI1_GNT1_L 0: GPIO4 1: GPIO4	PCI1_REQ0_L / PCI1_GNT0_L 0: GPIO3 1: GPIO3	Disable PHY interface 0: B mode interface	Processor Bus Mode 1: 60X Bus {63}

Intrepid MaxBus

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	C
SCALE: NONE	SHT 8 OF 45	

SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

PINS ARE SWAPABLE FOR RPAKS

U45
INTREPID-REV2.1
BGA
(2 OF 9)
OMIT
CRITICAL

MEM_DATA<0>	AK32	DDR_DATA_0	H35	MEM_ADDR<0>	DDR_A_0
MEM_DATA<1>	AK33	DDR_DATA_1	G35	MEM_ADDR<1>	DDR_A_1
MEM_DATA<2>	AK31	DDR_DATA_2	G36	MEM_ADDR<2>	DDR_A_2
MEM_DATA<3>	AK35	DDR_DATA_3	F36	MEM_ADDR<3>	DDR_A_3
MEM_DATA<4>	AK36	DDR_DATA_4	F35	MEM_ADDR<4>	DDR_A_4
MEM_DATA<5>	AJ32	DDR_DATA_5	E35	MEM_ADDR<5>	DDR_A_5
MEM_DATA<6>	AJ35	DDR_DATA_6	E36	MEM_ADDR<6>	DDR_A_6
MEM_DATA<7>	AJ36	DDR_DATA_7	G32	MEM_ADDR<7>	DDR_A_7
MEM_DATA<8>	AG33	DDR_DATA_8	D36	MEM_ADDR<8>	DDR_A_8
MEM_DATA<9>	AG35	DDR_DATA_9	H36	MEM_ADDR<9>	DDR_A_9
MEM_DATA<10>	AH35	DDR_DATA_10	G33	MEM_ADDR<10>	DDR_A_10
MEM_DATA<11>	AG36	DDR_DATA_11	H33	MEM_ADDR<11>	DDR_A_11
MEM_DATA<12>	AH36	DDR_DATA_12	D35	MEM_ADDR<12>	DDR_A_12
MEM_DATA<13>	AH32	DDR_DATA_13	L30	MEM_BA<0>	DDR_BA_0
MEM_DATA<14>	AG32	DDR_DATA_14	M29	MEM_BA<1>	DDR_BA_1
MEM_DATA<15>	AG31	DDR_DATA_15			
MEM_DATA<16>	AE32	DDR_DATA_16	AN34	MEM_CS_L<0>	DDRCS_0
MEM_DATA<17>	AF35	DDR_DATA_17	AN36	MEM_CS_L<1>	DDRCS_1
MEM_DATA<18>	AF36	DDR_DATA_18	AL35	MEM_CS_L<2>	DDRCS_2
MEM_DATA<19>	AE36	DDR_DATA_19	AL33	MEM_CS_L<3>	DDRCS_3
MEM_DATA<20>	AE35	DDR_DATA_20			
MEM_DATA<21>	AE33	DDR_DATA_21	AJ31	MEM_DQS<0>	DDR_DQS_0
MEM_DATA<22>	AD36	DDR_DATA_22	AH31	MEM_DQS<1>	DDR_DQS_1
MEM_DATA<23>	AD35	DDR_DATA_23	AD32	MEM_DQS<2>	DDR_DQS_2
MEM_DATA<24>	AA36	DDR_DATA_24	AB30	MEM_DQS<3>	DDR_DQS_3
MEM_DATA<25>	AA35	DDR_DATA_25	V30	MEM_DQS<4>	DDR_DQS_4
MEM_DATA<26>	AA33	DDR_DATA_26	P32	MEM_DQS<5>	DDR_DQS_5
MEM_DATA<27>	AB36	DDR_DATA_27	N29	MEM_DQS<6>	DDR_DQS_6
MEM_DATA<28>	AB35	DDR_DATA_28	L32	MEM_DQS<7>	DDR_DQS_7
MEM_DATA<29>	AC36	DDR_DATA_29			
MEM_DATA<30>	AA32	DDR_DATA_30	AJ33	MEM_DQM<0>	DDR_DM_0
MEM_DATA<31>	AB33	DDR_DATA_31	AH33	MEM_DQM<1>	DDR_DM_1
MEM_DATA<32>	V36	DDR_DATA_32	AD33	MEM_DQM<2>	DDR_DM_2
MEM_DATA<33>	U33	DDR_DATA_33	AC35	MEM_DQM<3>	DDR_DM_3
MEM_DATA<34>	U32	DDR_DATA_34	T35	MEM_DQM<4>	DDR_DM_4
MEM_DATA<35>	V35	DDR_DATA_35	T33	MEM_DQM<5>	DDR_DM_5
MEM_DATA<36>	T30	DDR_DATA_36	N32	MEM_DQM<6>	DDR_DM_6
MEM_DATA<37>	U36	DDR_DATA_37	L33	MEM_DQM<7>	DDR_DM_7
MEM_DATA<38>	U35	DDR_DATA_38			
MEM_DATA<39>	T36	DDR_DATA_39	L29	MEM_RAS_L	DDRRAS
MEM_DATA<40>	P33	DDR_DATA_40	H32	MEM_CAS_L	DDRCAS
MEM_DATA<41>	R30	DDR_DATA_41	K30	MEM_WE_L	DDRWE
MEM_DATA<42>	P35	DDR_DATA_42	AN35	MEM_CKE<0>	DDRCKE0
MEM_DATA<43>	P36	DDR_DATA_43	AM35	MEM_CKE<1>	DDRCKE1
MEM_DATA<44>	R36	DDR_DATA_44	AM36	MEM_CKE<2>	DDRCKE2
MEM_DATA<45>	R35	DDR_DATA_45	AL36	MEM_CKE<3>	DDRCKE3
MEM_DATA<46>	R33	DDR_DATA_46			
MEM_DATA<47>	R32	DDR_DATA_47	AB32	MEM_MUXSEL_H<0>	DDR_SELHI_0
MEM_DATA<48>	N35	DDR_DATA_48	AE29	MEM_MUXSEL_H<1>	DDR_SELHI_1
MEM_DATA<49>	M36	DDR_DATA_49	N30	MEM_MUXSEL_L<0>	DDR_SELLO_0
MEM_DATA<50>	L35	DDR_DATA_50	T32	MEM_MUXSEL_L<1>	DDR_SELLO_1
MEM_DATA<51>	M35	DDR_DATA_51			
MEM_DATA<52>	M33	DDR_DATA_52	Y32	SYSCLK_DDRCLK_A0_UF	DDR_MCLK_0_P
MEM_DATA<53>	L36	DDR_DATA_53	Y33	SYSCLK_DDRCLK_A0_L_UF	DDR_MCLK_0_N
MEM_DATA<54>	N33	DDR_DATA_54	Y35	SYSCLK_DDRCLK_A1_UF	DDR_MCLK_1_P
MEM_DATA<55>	M30	DDR_DATA_55	Y36	SYSCLK_DDRCLK_A1_L_UF	DDR_MCLK_1_N
MEM_DATA<56>	J32	DDR_DATA_56	Y30	INT_DDRCLK2_P_TP	DDR_MCLK_2_P
MEM_DATA<57>	J33	DDR_DATA_57	W30	INT_DDRCLK2_N_TP	DDR_MCLK_2_N
MEM_DATA<58>	J35	DDR_DATA_58	W32	SYSCLK_DDRCLK_B0_UF	DDR_MCLK_3_P
MEM_DATA<59>	K32	DDR_DATA_59	W33	SYSCLK_DDRCLK_B0_L_UF	DDR_MCLK_3_N
MEM_DATA<60>	K33	DDR_DATA_60	V33	SYSCLK_DDRCLK_B1_UF	DDR_MCLK_4_P
MEM_DATA<61>	J36	DDR_DATA_61	V32	SYSCLK_DDRCLK_B1_L_UF	DDR_MCLK_4_N
MEM_DATA<62>	K36	DDR_DATA_62	W35	INT_DDRCLK5_P_TP	DDR_MCLK_5_P
MEM_DATA<63>	K35	DDR_DATA_63	W36	INT_DDRCLK5_N_TP	DDR_MCLK_5_N
			AA22	INT_MEM_REF_H	DDR_REF
			Y22	INT_MEM_VREF	DDR_VREF_0
			T22		DDR_VREF_1

DDR MEMORY INTERFACE

'0' & '1' GO TO SLOT A
'2' & '3' GO TO SLOT B

'0'S ARE SAME POLARITY (ACTIVE-LO)
'1'S ARE SAME POLARITY (ACTIVE-HI)

MEM_VREF

R199 1K 1% 1/16W MF 402

+2_5V_INTREPID

R198 10K 1% 1/16W MF 402

R191 10K 1% 1/16W MF 402

C245 0.1UF 20% 10V CERM 402

INT_MEM_VREF

CLOCKS

SYSCLK_DDRCLK_A1_UF	RP33 22	4 5	SYSCLK_DDRCLK_A1
SYSCLK_DDRCLK_A1_L_UF	RP33 22	3 6	SYSCLK_DDRCLK_A1_L
SYSCLK_DDRCLK_A0_UF	RP34 22	1 8	SYSCLK_DDRCLK_A0
SYSCLK_DDRCLK_A0_L_UF	RP34 22	2 7	SYSCLK_DDRCLK_A0_L
SYSCLK_DDRCLK_B1_UF	RP33 22	2 7	SYSCLK_DDRCLK_B1
SYSCLK_DDRCLK_B1_L_UF	RP33 22	1 8	SYSCLK_DDRCLK_B1_L
SYSCLK_DDRCLK_B0_UF	RP34 22	3 6	SYSCLK_DDRCLK_B0
SYSCLK_DDRCLK_B0_L_UF	RP34 22	4 5	SYSCLK_DDRCLK_B0_L

CS

MEM_CS_L<0>	RP36 22	1 8	RAM_CS_L<0>
MEM_CS_L<1>	RP36 22	3 6	RAM_CS_L<1>
MEM_CS_L<2>	RP35 22	4 5	RAM_CS_L<2>
MEM_CS_L<3>	RP35 22	2 7	RAM_CS_L<3>

CKE

MEM_CKE<0>	RP36 22	2 7	RAM_CKE<0>
MEM_CKE<1>	RP36 22	4 5	RAM_CKE<1>
MEM_CKE<2>	RP35 22	1 8	RAM_CKE<2>
MEM_CKE<3>	RP35 22	3 6	RAM_CKE<3>

ADDR

MEM_ADDR<0>	RP31 22	1 8	RAM_ADDR<0>
MEM_ADDR<1>	RP25 22	1 8	RAM_ADDR<1>
MEM_ADDR<2>	RP25 22	2 7	RAM_ADDR<2>
MEM_ADDR<3>	RP25 22	4 5	RAM_ADDR<3>
MEM_ADDR<4>	RP25 22	3 6	RAM_ADDR<4>
MEM_ADDR<5>	RP30 22	1 8	RAM_ADDR<5>
MEM_ADDR<6>	RP30 22	2 7	RAM_ADDR<6>
MEM_ADDR<7>	RP31 22	3 6	RAM_ADDR<7>
MEM_ADDR<8>	RP30 22	4 5	RAM_ADDR<8>
MEM_ADDR<9>	RP31 22	2 7	RAM_ADDR<9>
MEM_ADDR<10>	RP31 22	4 5	RAM_ADDR<10>
MEM_ADDR<11>	RP26 22	4 5	RAM_ADDR<11>
MEM_ADDR<12>	RP30 22	3 6	RAM_ADDR<12>

BA

MEM_BA<0>	RP26 22	2 7	RAM_BA<0>
MEM_BA<1>	RP26 22	1 8	RAM_BA<1>

CNTL

MEM_WE_L	RP26 22	3 6	RAM_WE_L
MEM_CAS_L	R250 22	1 2	RAM_CAS_L
MEM_RAS_L	R238 22	1 2	RAM_RAS_L

1MB BOOT ROM

+3V_MAIN

C460 2.2UF 20% 10V CERM 805

C470 0.1UF 20% 10V CERM 402

C479 0.1UF 20% 10V CERM 402

U17
FEPR-1MX8
3.3V
TSOP
OMIT

A0	21	DQ0	25
A1	20	DQ1	26
A2	19	DQ2	27
A3	18	DQ3	28
A4	17	DQ4	32
A5	16	DQ5	33
A6	15	DQ6	34
A7	14	DQ7	35
A8	8		
A9	7		
A10	36		
A11	6		
A12	5		
A13	4		
A14	3		
A15	2		
A16	1		
A17	40		
A18	13		
A19	37		
A20	38		
CE	22		
OE	24		
WE	9		
WP	12		
PWD	10		

VPP 11, VCC 30, 31, GND 23, 39

PCI_AD<0> … PCI_AD<31>

ROM_ONBOARD_CS_L
ROM_OE_L
ROM_RW_L
ROM_WP_L
INT_RESET_L

+3V_MAIN

R338 10K 5% 1/16W MF 402

R386 10K 5% 1/16W MF 402

R357 1K 5% 1/16W MF 402

ROM_CS_L

OVERRIDE ROM MODULE
INTERCEPTS ROM CHIP SELECT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1556	1	IC,BOOTROM,Q41B	U17	CRITICAL	?

PULL-DOWN RESISTORS TO ENSURE
CKE STAYS LOW AFTER INTREPID
2.5V I/O SHUTS OFF

RAM_CKE<0>
RAM_CKE<1>
RAM_CKE<2>
RAM_CKE<3>

R500 10K 5% 1/16W MF 402

R439 10K 5% 1/16W MF 402

R409 10K 5% 1/16W MF 402

R387 10K 5% 1/16W MF 402

INT - DDR/BOOTROM

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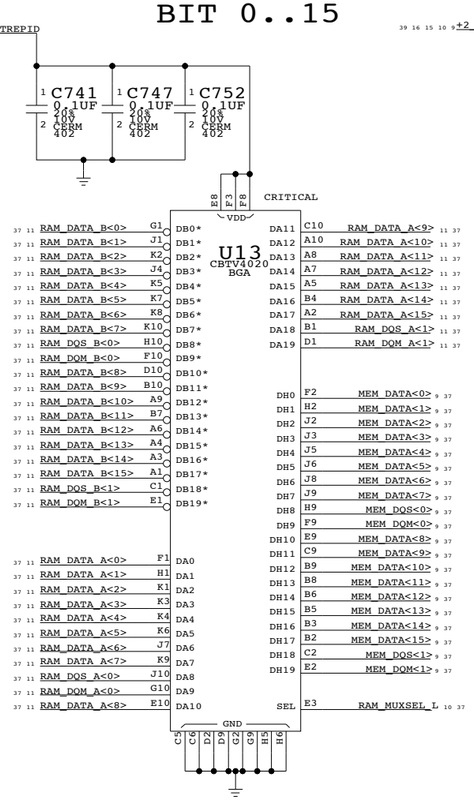
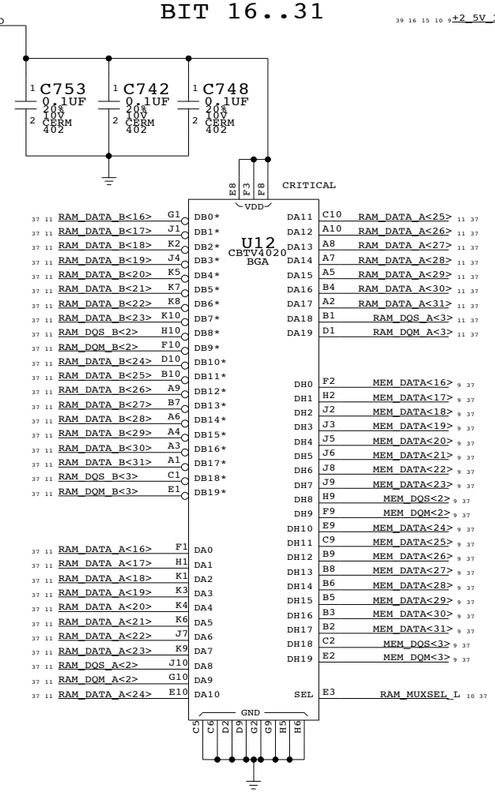
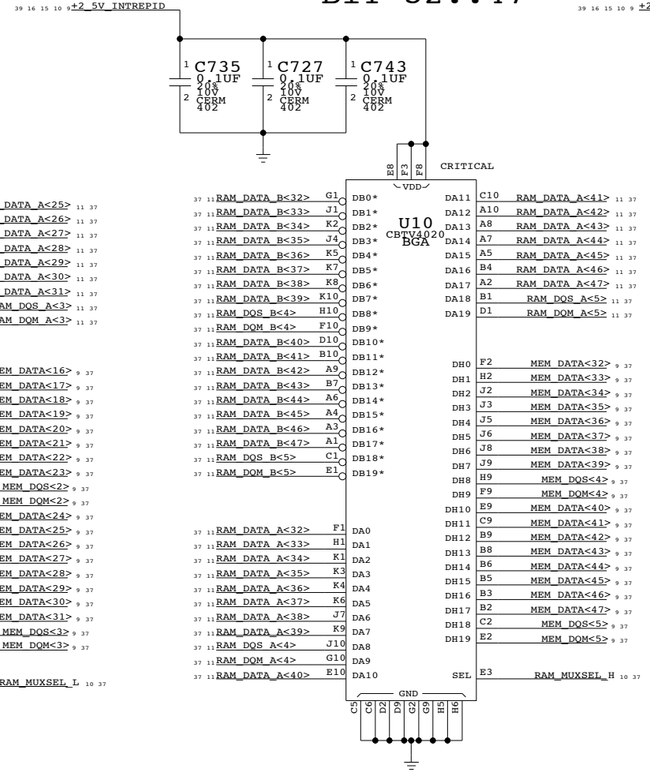
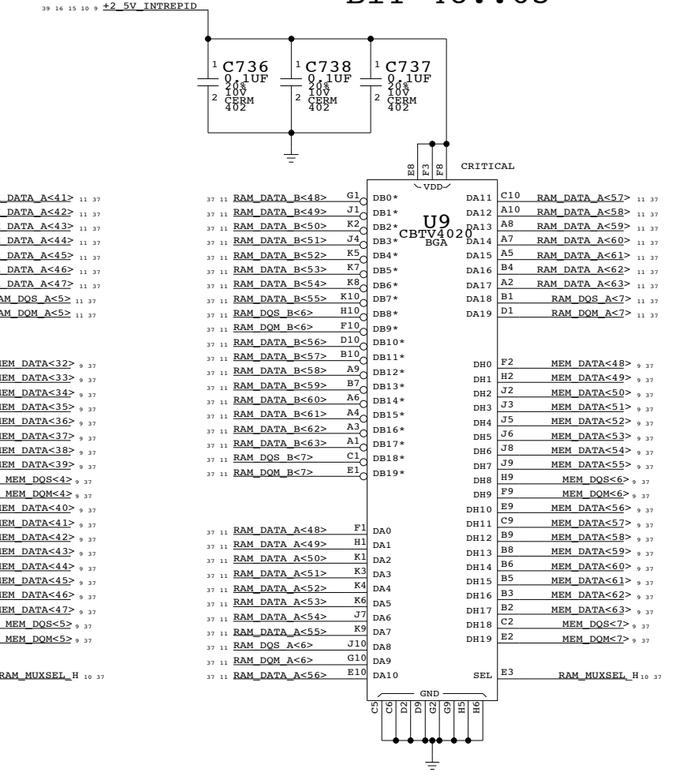
SIZE	DRAWING NUMBER	REV.
D	051-6694	C
SCALE: NONE	SHT 9 OF 45	



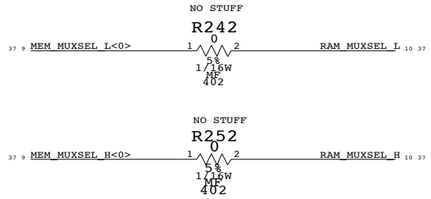


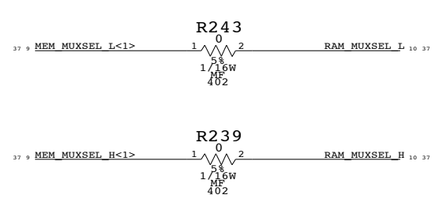




SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND
MEM_MUXSEL_H<0> AND MEM_MUXSEL_L<0> ARE ACTIVE LOW
MEM_MUXSEL_H<1> AND MEM_MUXSEL_L<1> ARE ACTIVE HIGH

ADDED 0 OHM RESISTORS IN CASE POLARITY IS WRONG





16BIT 2:1 DDR MUXES

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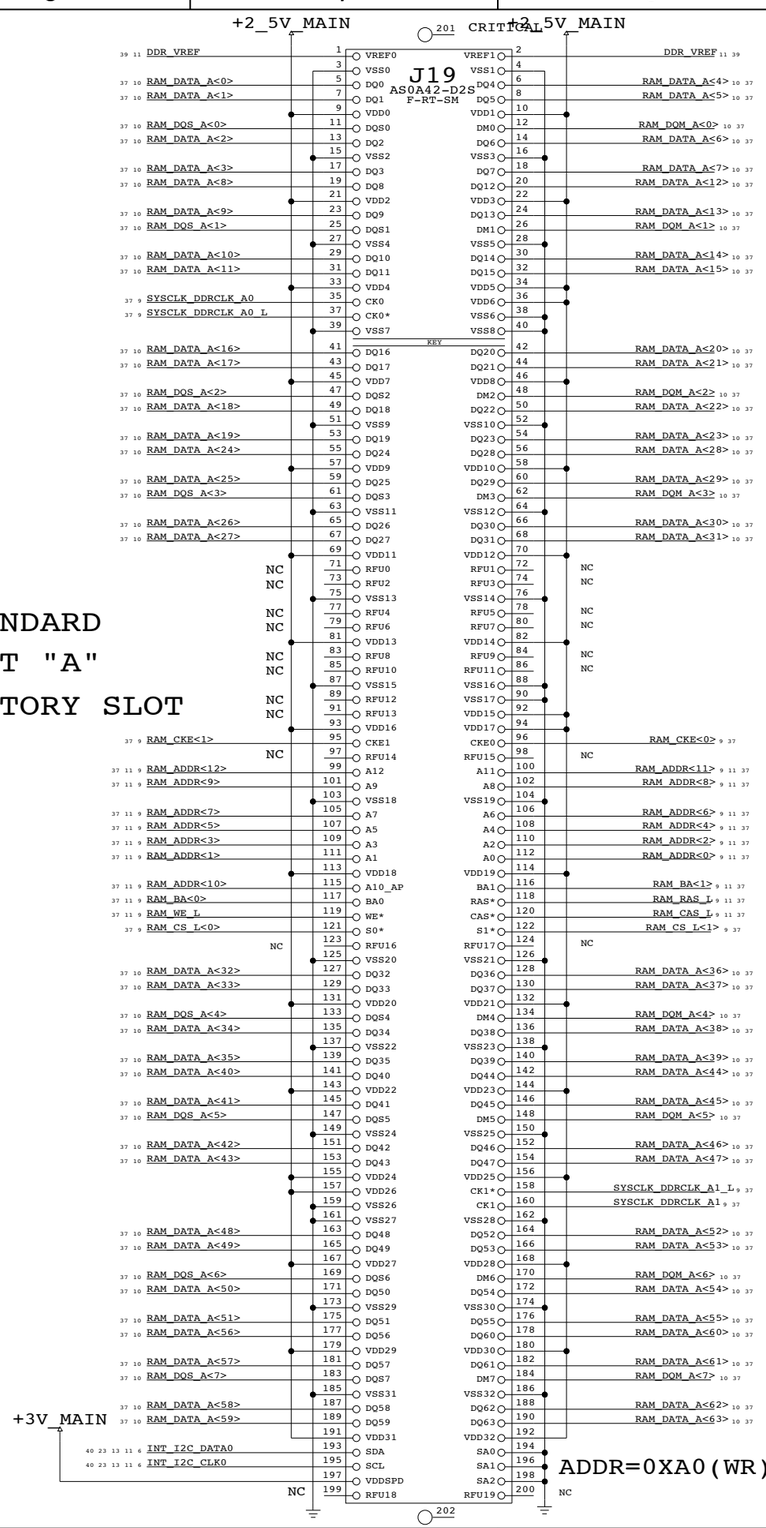
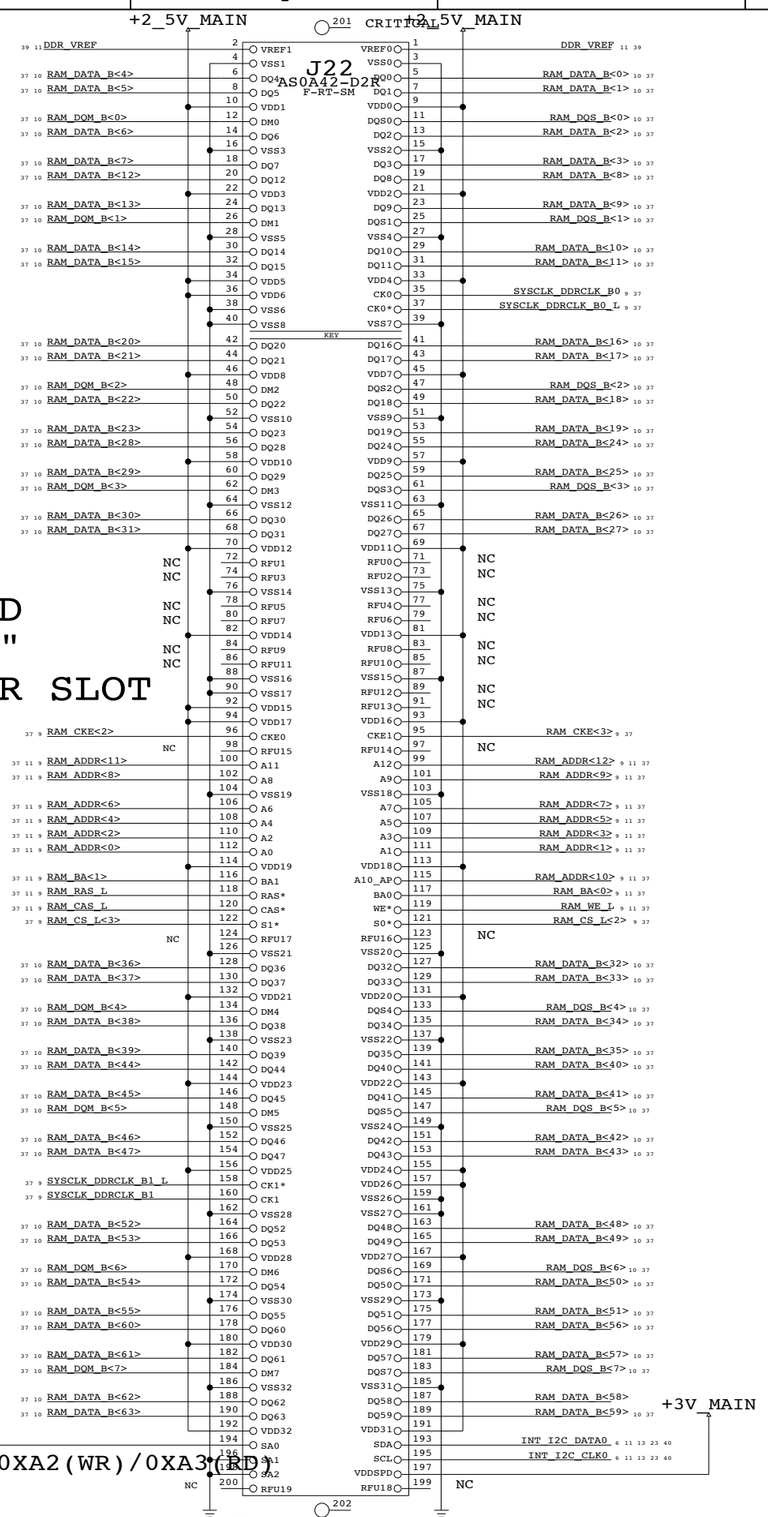
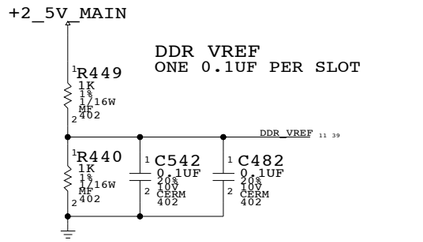
SIZE	DRAWING NUMBER	REV.
D	051-6694	C

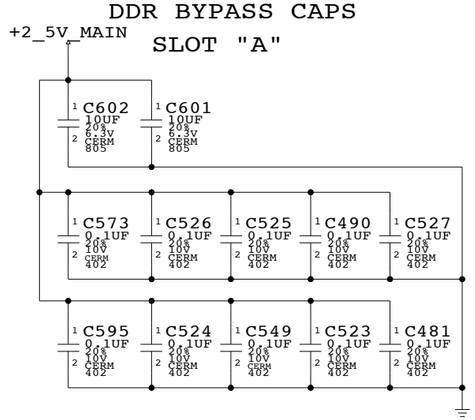
SCALE: NONE

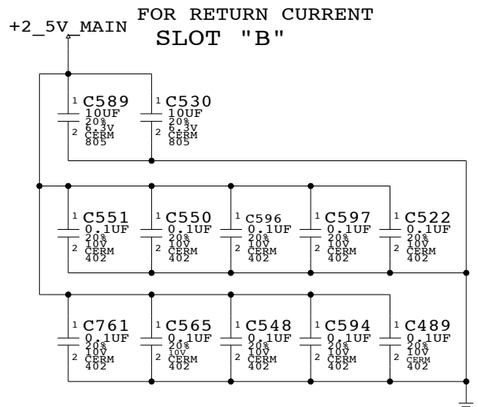
SHT 10 OF 45











DDR SODIMM CONNS

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APPLE COMPUTER INC.

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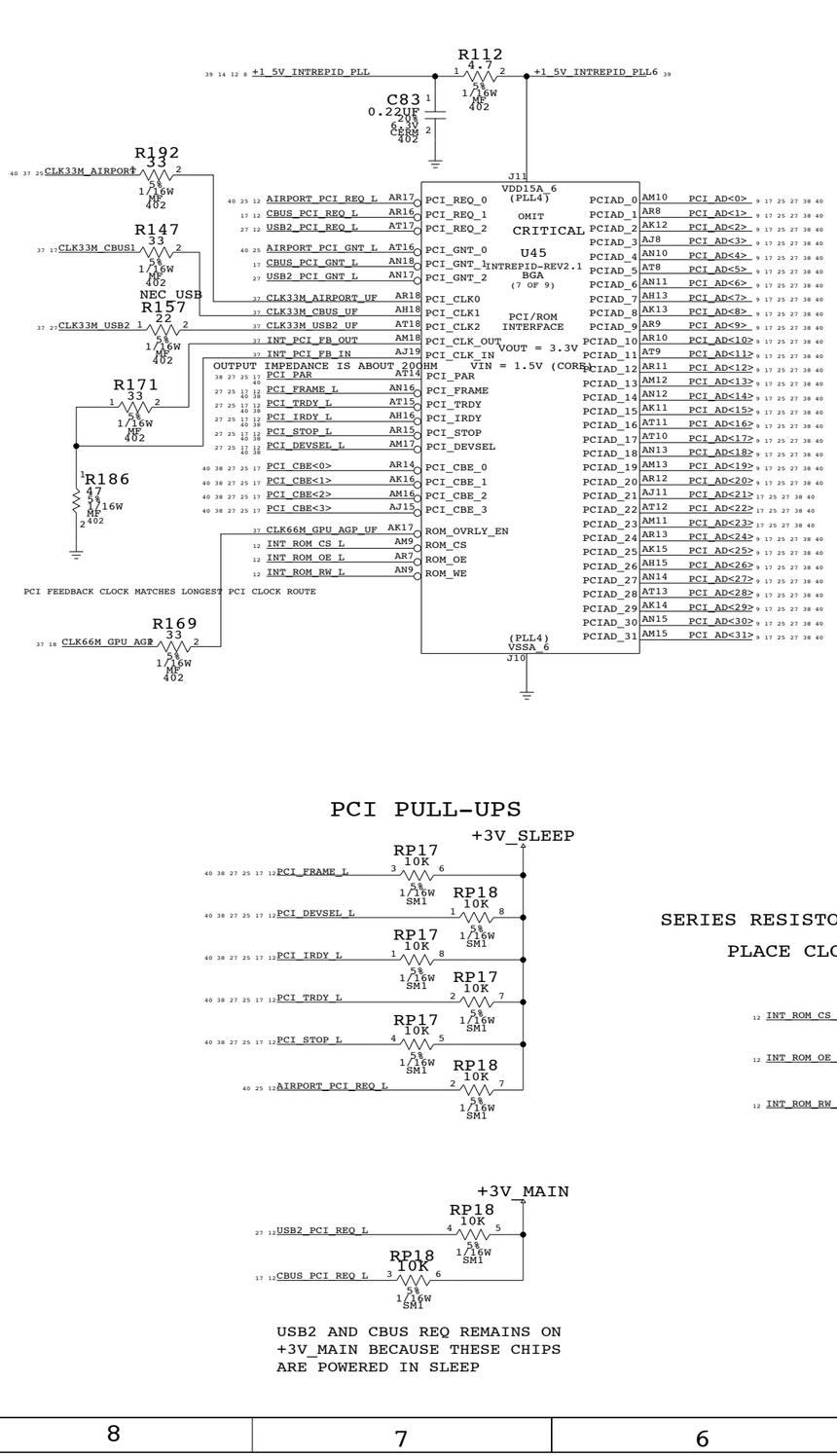
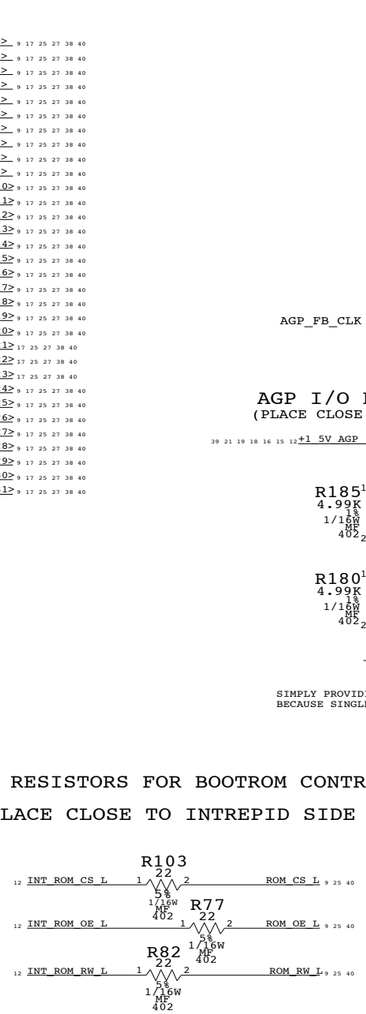
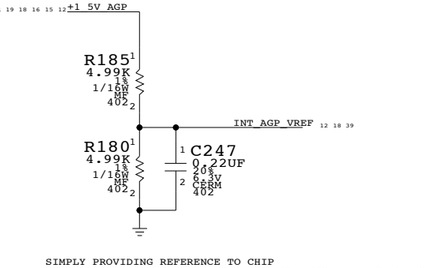
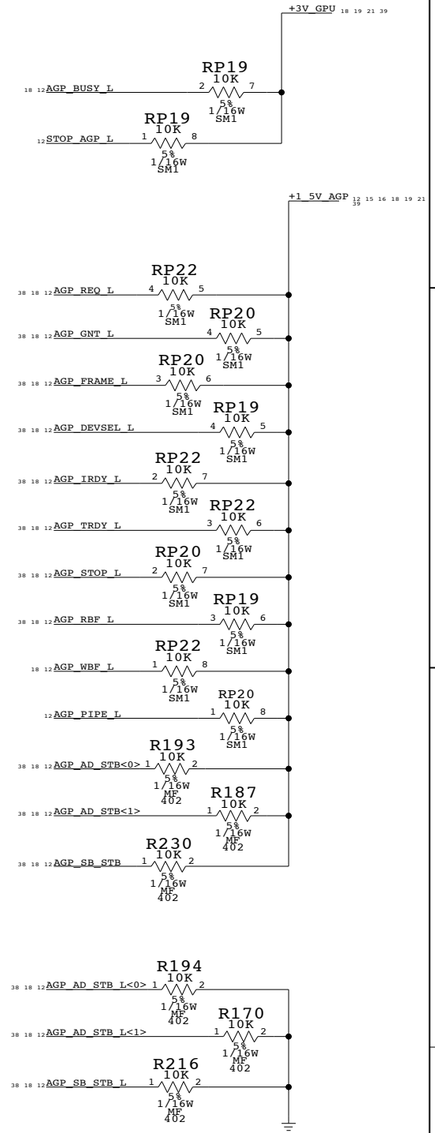
D	051-6694	C

SCALE	SHT
NONE	11 OF 45









INTREPID AGP/PCI

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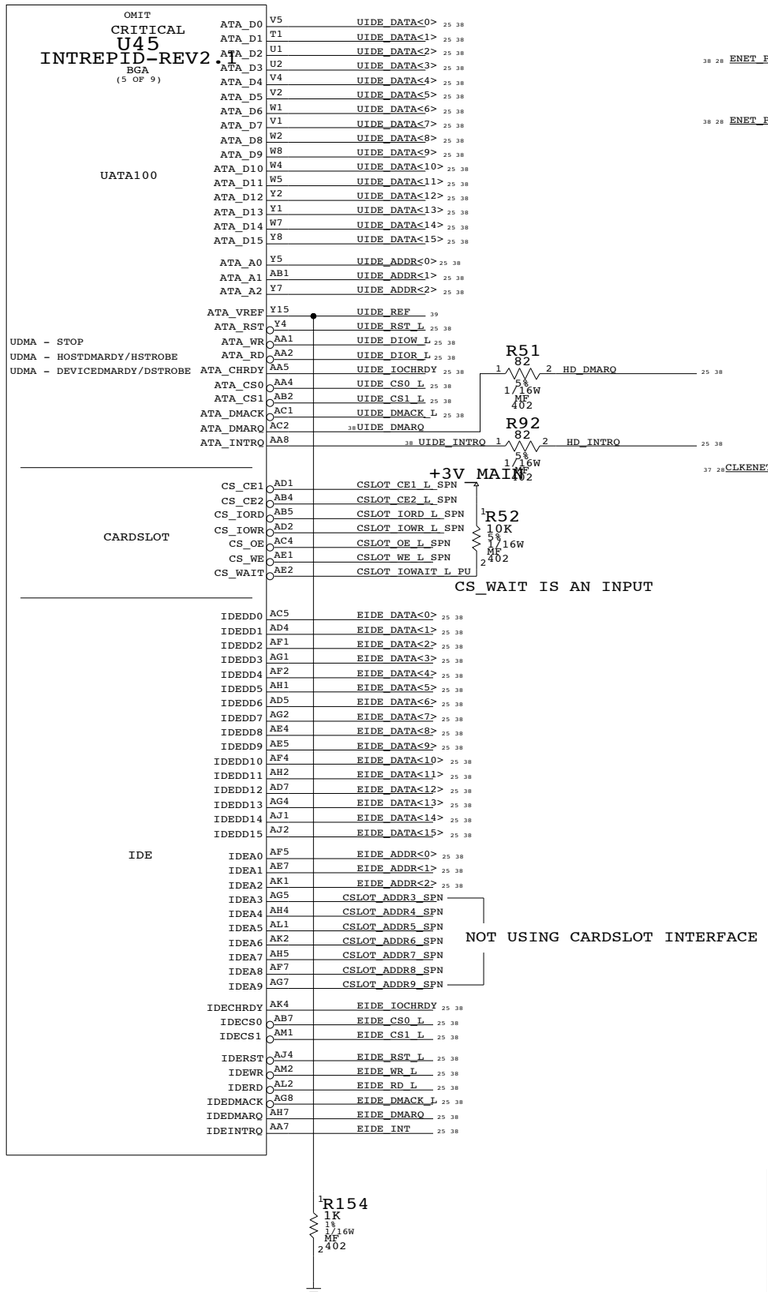
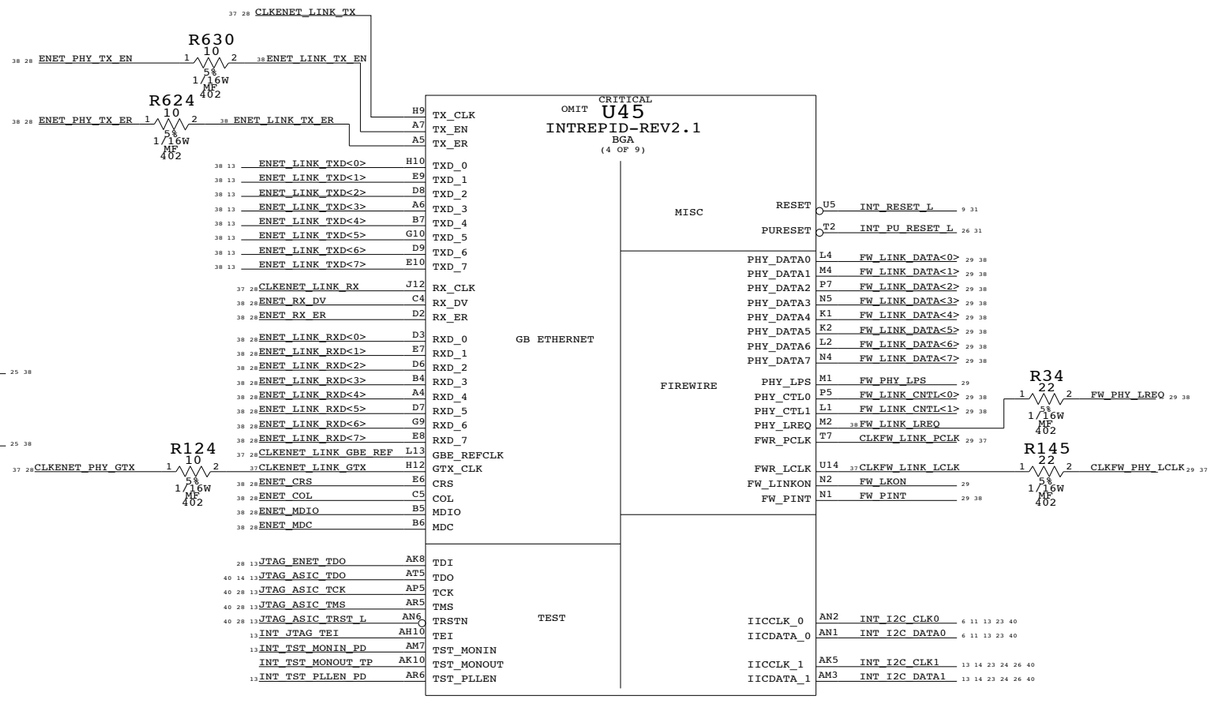
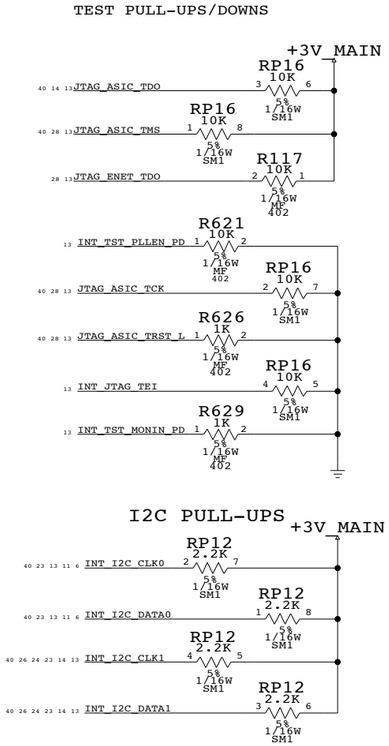
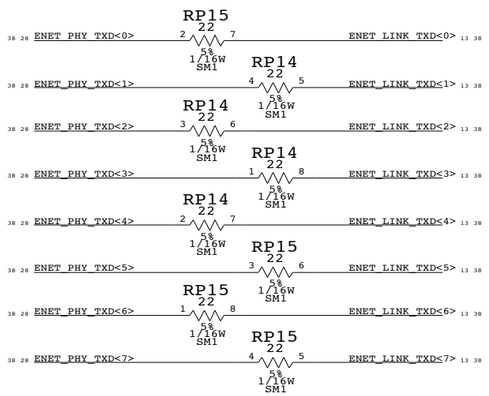
SHT 12 OF 45







ENET_TXD SERIES TERMINATION



JTG_RSTN_H	TST_TEI_H	JTG_TDO_H (I/O)	JTG_TDI_H (I/O)	TST_PLLEN_H	ANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	EXTPLL SHUTDOWN (OUTPUT)	DDR_TPDENABLE (OUTPUT)	0	(OUTPUT)	NORMAL OPERATION
0	0	(OUTPUT)	0(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	HWPLL_TESTSEL5 (INPUT)	1(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0(I)	0(I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0(I)	1(I)	0	X(I)	ATPG IDDQ
0	1	0(I)	1(I)	1	X(I)	TEST TRI-STATE
0	1	1(I)	0(I)	0	X(I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1(I)	0(I)	1	X(I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1(I)	1(I)	X	X(I)	FUNCTIONAL TEST IDDQ

BUS / ADDR	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
A0-WR A1-RD	RAM - STANDARD J20 - PG 12	N/A	N/A	N/A
A2-WR A3-RD	RAM - REVERSED J23 - PG 12	N/A	N/A	N/A
AC-WR AD-RD	N/A	N/A	DASH MODEM J9 - PG 25	N/A
AE-WR AF-RD	BOOTBANG E2PROM U37 - PG 23	N/A	N/A	N/A
84-WR 85-RD	LMU U36 - PG 23	N/A	N/A	N/A
58-WR 59-RD	N/A	FAN CONTROLLER U3 - PG 24	N/A	N/A
6A-WR 6B-RD	N/A	N/A	SNAPPER SOUND J12 - PG 24	N/A
D0-WR D1-RD	N/A	CLOCK SLEW SSCG U56 - PG 15	N/A	N/A
B0-WR B1-RD	N/A	MMM	N/A	N/A

ADDR LSB INDICATES READ ('1') OR WRITE ('0') MODES

INT - ENET/FW/UATA EIDE/I2C

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USB POWER FAULT SIGNALS

USB PORT ASSIGNMENTS

PORT A - RIGHT USB 1

PORT B - UNUSE

PORT C - LEFT USB

PORT D - MODEM

PORT E - BLUETOOTH

PORT F - TPAD

R89,R80 NEED PLACE NEAR TPAD CONNECTOR

PLACE R68 CLOSE TO INTREPID SIDE
OTHERWISE A LOT OF OVERSHOOT/UNDERSHOOT

CRYSTAL LOAD CAPACITANCE IS 16PF

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
359S0074	359S0086	?	U42	ALT FOR NEW SCREEN

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0090	1	XTAL,CER,LOW PROF,18,432MHZ,8X4.5MM,SMD	Y1	CRITICAL	?

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES,METAL FILM,10 K OHM,5,1/16W,0402,SM	R100	NO_SSCG

HWPLL TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

INT - USB/GPIOS/I2S

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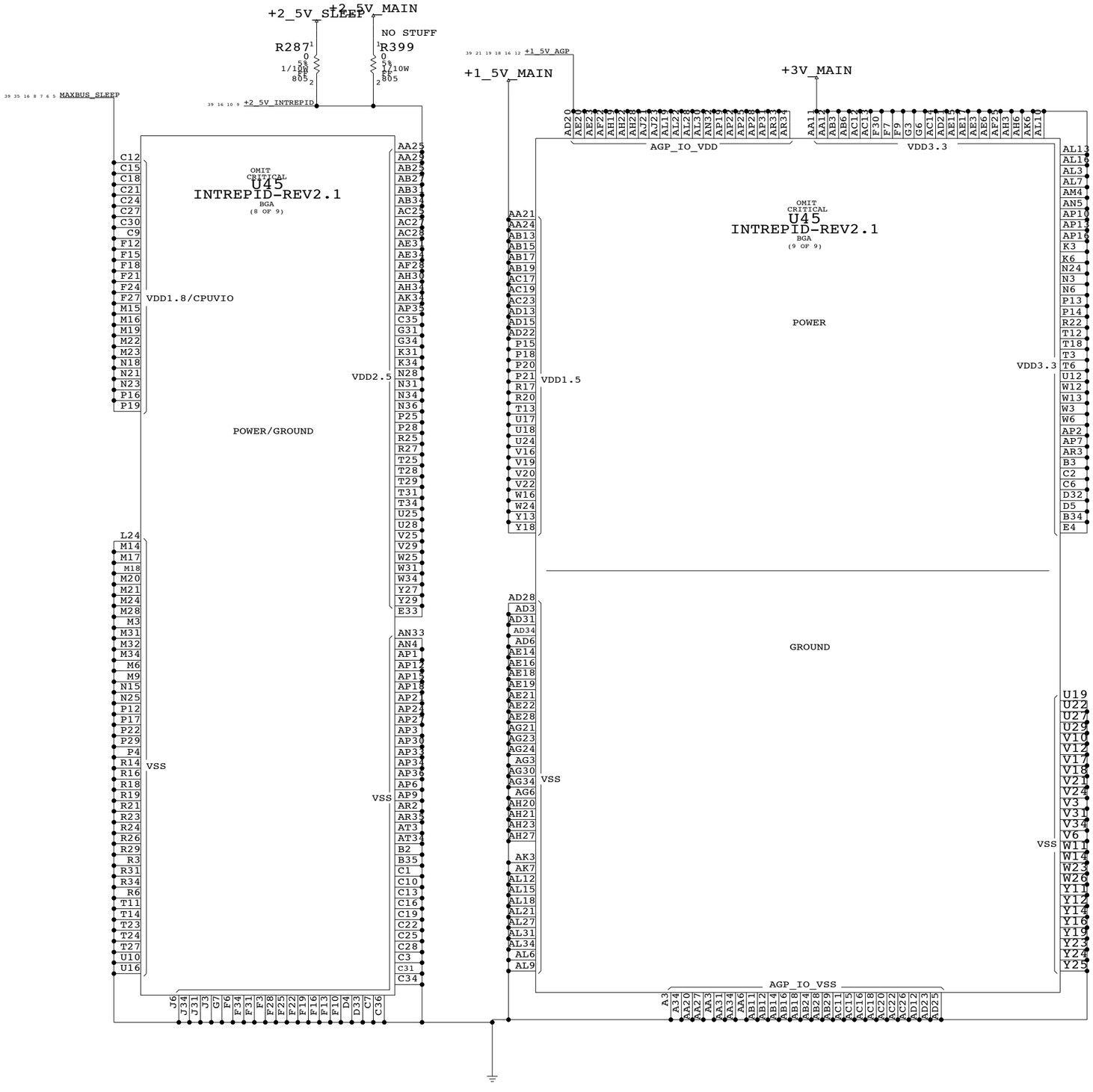

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0305	1	IC,ASIC,INTREPID,REV2.1,974BGA,FAST	U45	CRITICAL	?

Intrepid Power

APPLE COMPUTER INC.

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D	051-6694	C

SCALE	SHT	OF
NONE	15	45

INTREPID MAXBUS DECOUPLING

MAXBUS_SLEEP

24 Balls
4 X 10UF (0805)
32 X 0.22UF (0402)

C204 10uF 20% 6.3V CERM 805 | C348 10uF 20% 6.3V CERM 805 | C236 10uF 20% 6.3V CERM 805 | C196 10uF 20% 6.3V CERM 805

C239 C240 C350 C312 C176 C288 C313 C94 C286 C158 — 0.22uF 20% 6.3V CERM 402

C174 C206 C259 C237 C238 C95 C117 C241 C260 C314 — 0.22uF 20% 6.3V CERM 402

C173 C171 C175 C226 C172 C207 C118 C287 C119 C349 — 0.22uF 20% 6.3V CERM 402

C205 C209 — 0.22uF 20% 6.3V CERM 402

INTREPID AGP I/O DECOUPLING

+1_5V_AGP

21 Balls
4 X 10UF (0805)
24 X 0.22UF (0402)

C371 10uF 20% 6.3V CERM 805 | C231 10uF 20% 6.3V CERM 805 | C281 10uF 20% 6.3V CERM 805 | C394 10uF 20% 6.3V CERM 805

C356 C297 C268 C217 C355 C267 C250 C298 C377 C216 — 0.22uF 20% 6.3V CERM 402

C228 C230 C265 C378 C357 C229 C325 C393 C324 C323 — 0.22uF 20% 6.3V CERM 402

C251 C266 C249 — 0.22uF 20% 6.3V CERM 402

INTREPID DDR DECOUPLING

+2_5V_INTREPID

44 Balls
4 X 10UF (0805)
51 X 0.22UF (0402)

C422 10uF 20% 6.3V CERM 805 | C417 10uF 20% 6.3V CERM 805 | C418 10uF 20% 6.3V CERM 805 | C423 10uF 20% 6.3V CERM 805

C407 C391 C310 C317 C480 C390 C370 C320 C365 C366 — 0.22uF 20% 6.3V CERM 402

C367 C292 C295 C403 C291 C352 C322 C392 C385 C376 — 0.22uF 20% 6.3V CERM 402

C321 C318 C399 C410 C335 C369 C384 C294 C406 C405 — 0.22uF 20% 6.3V CERM 402

C404 C400 C386 C289 C387 C401 C354 C389 C309 C398 — 0.22uF 20% 6.3V CERM 402

C337 C290 C402 C397 C368 C334 C388 C293 C319 C336 — 0.22uF 20% 6.3V CERM 402

C316 0.22uF 20% 6.3V CERM 402

INTREPID CORE DECOUPLING

+1_5V_MAIN

30 Balls
4 X 10UF (0805)
29 X 0.22UF (0402)

C128 10uF 20% 6.3V CERM 805 | C101 10uF 20% 6.3V CERM 805 | C157 10uF 20% 6.3V CERM 805 | C315 10uF 20% 6.3V CERM 805

C147 C243 C262 C242 C227 C181 C142 C215 C278 C264 — 0.22uF 20% 6.3V CERM 402

C244 C212 C178 C179 C177 C159 C161 C162 0.22uF C280 C279 — 0.22uF 20% 6.3V CERM 402

C144 C246 C211 C263 C180 C213 C197 C208 C214 — 0.22uF 20% 6.3V CERM 402

INTREPID 3.3V DECOUPLING

+3V_MAIN

57 Balls
4 X 10UF (0805)
72 X 0.22UF (0402)

C164 10uF 20% 6.3V CERM 805 | C395 10uF 20% 6.3V CERM 805 | C10 10uF 20% 6.3V CERM 805 | C9 10uF 20% 6.3V CERM 805

C375 C351 C53 C42 C21 C185 C31 C143 C123 C121 — 0.22uF 20% 6.3V CERM 402

C33 C184 C43 C35 C261 C60 C52 0.22uF C199 C57 C19 — 0.22uF 20% 6.3V CERM 402

C16 C108 C55 C32 C125 C45 C76 C277 C28 C26 0.22uF — 0.22uF 20% 6.3V CERM 402

C34 C23 C120 C146 C141 C30 0.22uF C145 C96 C54 C50 — 0.22uF 20% 6.3V CERM 402

C75 C122 C51 C59 C163 C126 C98 C109 C56 C27 — 0.22uF 20% 6.3V CERM 402

C296 C248 C210 C58 C22 C20 0.22uF C61 C44 C29 C24 — 0.22uF 20% 6.3V CERM 402

C183 C18 C49 C36 C17 C99 C396 C124 C127 C100 — 0.22uF 20% 6.3V CERM 402

Intrepid Decoupling

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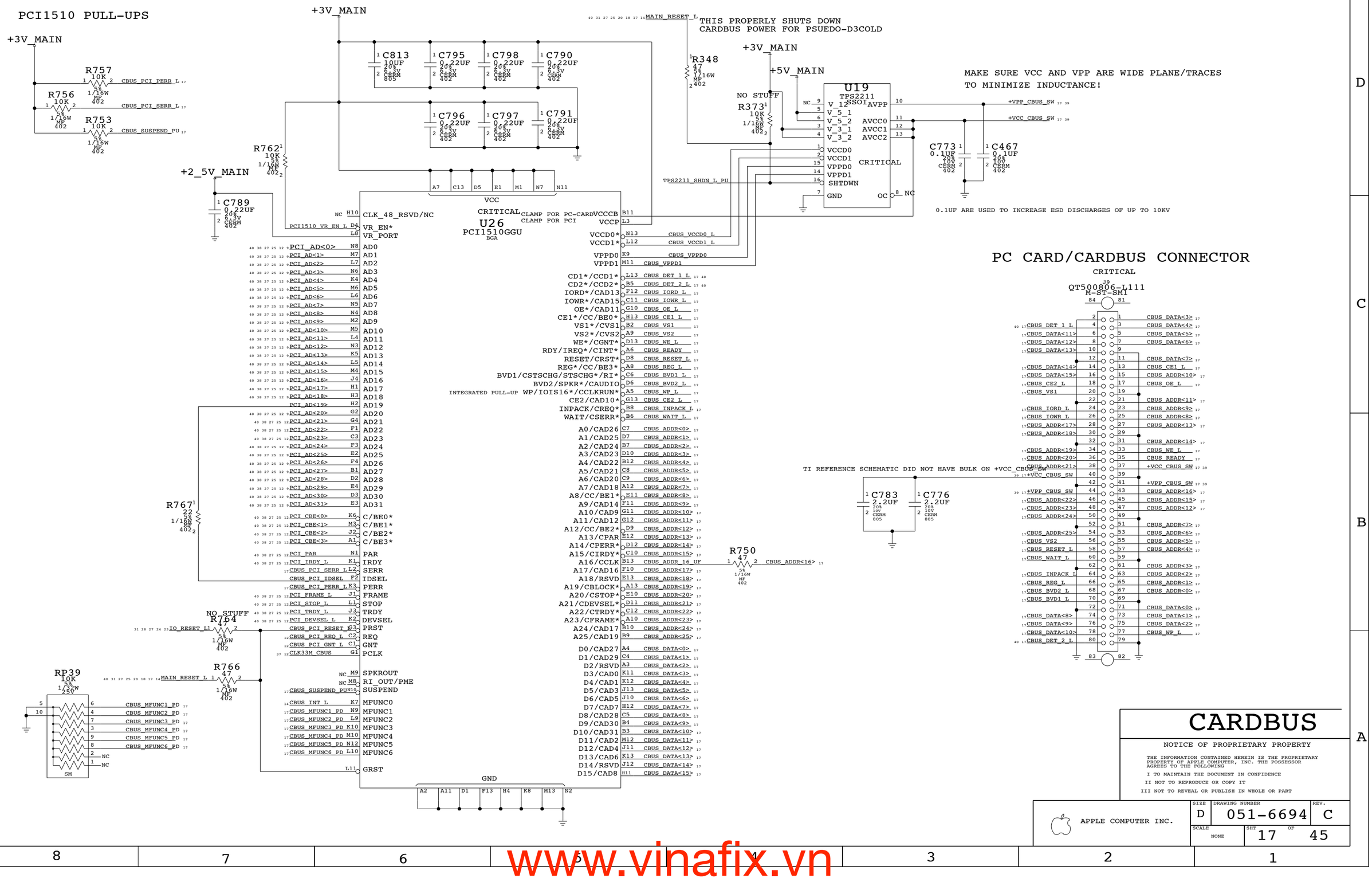
NONE	16	45



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0214	1	IC,ATI,M11-CSP128,GRPHCTLR,667BGA,HYNIX U44		CRITICAL	M11_CSP128

27M OSC

(PLACE THE OSCILLATOR AND R189 AND R195 CLOSE TO ATI PIN AJ29)

+3V_SLEEP
L4 FERR-EMI-100-OHM SM
+3V ATI OSC SLEEP
C77 0.1uF 20% 10V CERM 402
C78 4.7uF 20% 6.3V CERM 805
NO STUFF R188 100K 5% 1/16W MF 402
CRITICAL
VCC
G2 27.0000M OSC SM-1
ATI OSC OE
OE
OUT
GND
ATI CLK27M OSC
(PLACE R200 CLOSE TO OSC)
GPU_SS
R200 0 5% 1/16W MF 402
ATI CLK27M OSC SS
R189 287 1% 1/16W MF 402
ATI CLK27M IN
R195 162 1% 1/16W MF 402

S0=1;S1=M => -1.5% DOWN-SPREAD
SPREAD SPECTRUM SUPPORT

+3V_SLEEP
GPU_SS
L3 FERR-EMI-100-OHM SM
+3V ATI SS
GPU_SS C70 10uF 20% 6.3V CERM 805
GPU_SS C71 0.1uF 20% 10V CERM 402
NO STUFF R173 0 5% 1/16W MF 402
GPU_SS R181 0 5% 1/16W MF 402
GPU_SS CRITICAL
U47 CY25811 SOI
ATI CLK27M OSC SS
XIN/CLKIN
XOUT
SSCLK
ATI SSCLK UF
NC
FRSEL
CY25811 S1
CY25811 S0
S1
S0
VSS
GPU_SS R201 33 5% 1/16W MF 402
ATI SSCLK IN
NO STUFF R37 0 5% 1/16W MF 402
NO STUFF R38 0 5% 1/16W MF 402

U44
RAGE MOBILITY M11-CSP64 64MB BGA
(1 OF 6)

+3V_GPU
+1_5V_AGP
R119 47 5% 1/16W MF 402
R127 10K 5% 1/16W MF 402
R159 20K 5% 1/16W MF 402
INT_AGP_VREF
C62 0.1uF 20% 10V CERM 402
C63 0.01uF 20% 16V CERM 402
(PLACE C1002 CLOSE TO AGPREF PIN)
R172 20K 5% 1/16W MF 402
R158 0 5% 1/16W MF 402
R126 47K 5% 1/16W MF 402
R138 47K 5% 1/16W MF 402
R118 45.3 1% 1/16W MF 402

AGP_AD<31:0> AB30 AB27 AA29 AB28 AA30 AA27 Y30 AA28 W30 W27 V30 V28 V29 V27 U30 U28 R27 R29 P28 P30 P27 P29 N28 N30 M30 M27 M29 L28 L30 L27 L29 K28
AD31 AD30 AD29 AD28 AD27 AD26 AD25 AD24 AD23 AD22 AD21 AD20 AD19 AD18 AD17 AD16 AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0

AGP_CBE<3:0> W28 U29 R30 N27
CBEB3 CBEB2 CBEB1 CBEB0

CLK66M_GPU_AGP AG30 PCICLK
AGP_FRAME_L U27 FRAMEB
AGP_IRDY_L T30 IRDYB
AGP_TRDY_L T28 TRDYB
AGP_STOP_L T27 STOPB
AGP_DEVSEL_L T29 DEVSELB
AGP_PAR R28 PAR
AGP_REQ_L AF29 REQB
AGP_GNT_L AF27 GNTB
AGP_INT_L AH29 INTAB
AGP_ATI_RESET_L AH30 RSTB
AGP_WBF_L AE27 WBF
AGP_ATI_VREFG AK3 VREFG
AGP_ATI_VREF D8 MVREF

AD_STB0 N29 AGP_AD_STB<0>
AD_STB1 W29 AGP_AD_STB<1>
AD_STBB0 M28 AGP_AD_STB_L<0>
AD_STBB1 Y29 AGP_AD_STB_L<1>
AGP_BUSYB AG28 AGP_BUSY_L
AGPREF K30
AGPTEST K29 GPU_AGP_TEST
AGP8X_DETB U25 AGP8X_DET_PU
SUS_STAT AJ28 AGP_SUS_STAT_L_PU
ST0 AF30 AGP_ST<0>
ST1 AF28 AGP_ST<1>
ST2 AE29 AGP_ST<2>
SBA7 AC28 AGP_SBA<7>
SBA6 AB29 AGP_SBA<6>
SBA5 AC27 AGP_SBA<5>
SBA4 AC30 AGP_SBA<4>
SBA3 AD27 AGP_SBA<3>
SBA2 AD30 AGP_SBA<2>
SBA1 AE28 AGP_SBA<1>
SBA0 AD29 AGP_SBA<0>
RBFB AE30 AGP_RBF_L
STP_AGPB AG29 AGP_STP_L
SB_STB AC29 AGP_SB_STB
SB_STBS AD28 AGP_SB_STB_L
RSTB_MSK AD24 ATI_RSTB_MSK
DBI_LO Y25 ATI_DBI_LO_PU
DBI_HI Y27 ATI_DBI_HI_PU

OMIT

U44
RAGE MOBILITY M11-CSP64 64MB BGA
(6 OF 6)

M2 P3 A21 B19 M15 N15 P15 R15 T15 T12 T13 T14 W16 V16 U16 T16 R16 R17 R18 R19
U6 AE15 F18 P25
VDDCI

U44
RAGE MOBILITY M11-CSP64 64MB BGA
(2 OF 6)

B26 A26 B25 A25 C22 D21 C21 D20 C20 D22 C23 D23 A27 B27
H2 H1 J2 J1 K4 K3 L4 M3 L3 M4 N2 N1 N4 N3 G30 G28 B30 D26 D16 B15 D11 B10 D5 B3 G3 E1 U1 V3 AB1 AC3 J30 J29 H30 H29 F30 F29 E30 E29 J28 J27 H28 H27 F28 F27 E28 E27 D30 D29 C30 C29 A30 A29 A28 B28 B28 C28 D27 C27 D25 C25 D24 C24 D18 C18 D17 C17 D15 C15 D14 C14 B17
VSS
OMIT

A17 B16 B14 A14 B13 A13 D13 C13 D12 C12 D10 C10 D9
C9 B12 A12 B11 A11 B9 A9 B8 A8 C7 D7 C6 D6 C4 D4 C3 D3 A5 B5 A4 B4 A2 B2 A1 B1 E4 E3 F3 F4 H3 H4 J3 J4 C1 C2 D1 D2 F1 F2 G1 G2 R1 R2 T1 T2 V1 V2 W1 W2 T3 T4 U3 U4 W3 W4 Y3 Y4 Y1 Y2 AA1 AA2 AC1 AC2 AD1 AD2 AA3 AA4 AB3 AB4 AD3 AD4 AE3 AE4
VSS
OMIT

A10 C5 A3 G4 E2 U2 V4 AB2 AC4 B23 K2 A23 K1 B22 L2 A22 L1
VSS

AC10 GPU_THERM_DP_TP
AC11 GPU_THERM_DM_TP
+GPU_MEM
E8
J6 (PULL-UP to GPU_MEM_IO)
C8 ATI_MEMTEST
AC22 NC
TEST_YCLK
TEST_MLCK
MEMTEST
PLLTEST

GPU_VCORE
L2 60-OHM-EMI SM
+GPU_VCORE_VDDCI
C64 0.01uF 20% 16V CERM 402
C67 10uF 20% 6.3V CERM 805
C65 0.01uF 20% 16V CERM 402
C68 0.01uF 20% 16V CERM 402
C66 0.01uF 20% 16V CERM 402
C69 0.01uF 20% 16V CERM 402

+3V_GPU
MAIN_RESET_L IS TOGGLED FOR SLEEP
MAIN_RESET_L
R53 47 5% 1/16W MF 402
R54 10K 5% 1/16W MF 402
R43 1K 1% 1/16W MF 402
R44 1K 1% 1/16W MF 402
+GPU_MEM
R45 1K 1% 1/16W MF 402
PLACE VERF VOLTAGE DIVIDER CLOSE TO ATI M10 VREF PIN
R46 1K 1% 1/16W MF 402
C11 0.1uF 20% 10V CERM 402
C37 10uF 20% 6.3V CERM 805

+1_8V_GPU
ATI_MEMIO_LO
ATI_MEMIO_HI
R55 4.7K 5% 1/16W MF 402
R104 4.7K 5% 1/16W MF 402
R70 4.7K 5% 1/16W MF 402
R105 4.7K 5% 1/16W MF 402
ATI_MEMVMODE0
ATI_MEMVMODE1
MEMVMODE0
MEMVMODE1

FOR 2.5 VDDR1
MEMVMODE0=1.8V
MEMVMODE1=GND
FOR 1.8 VDDR1
MEMVMODE0=GND
MEMVMODE1=1.8V

M11 AGP INTERFACE

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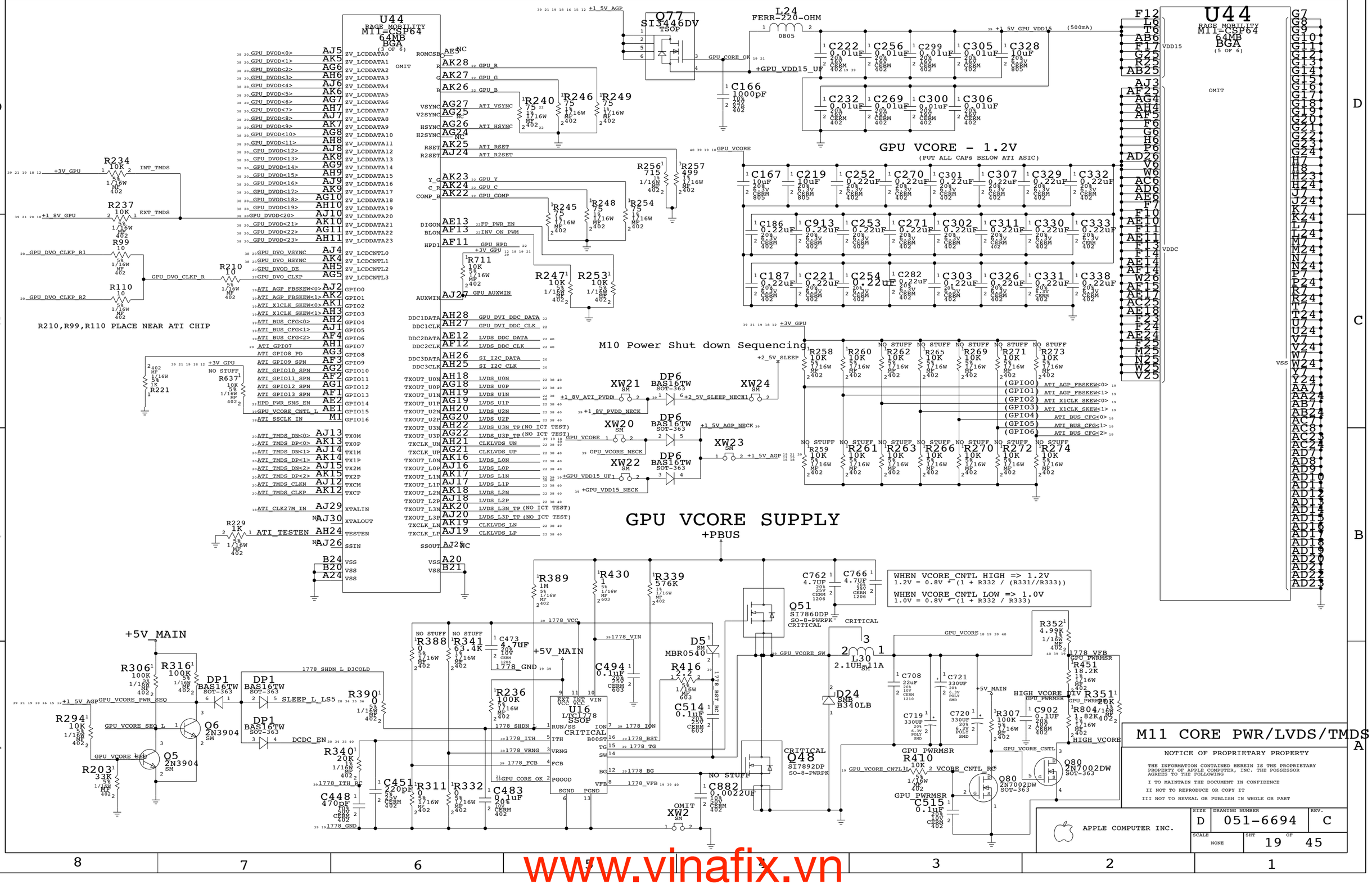

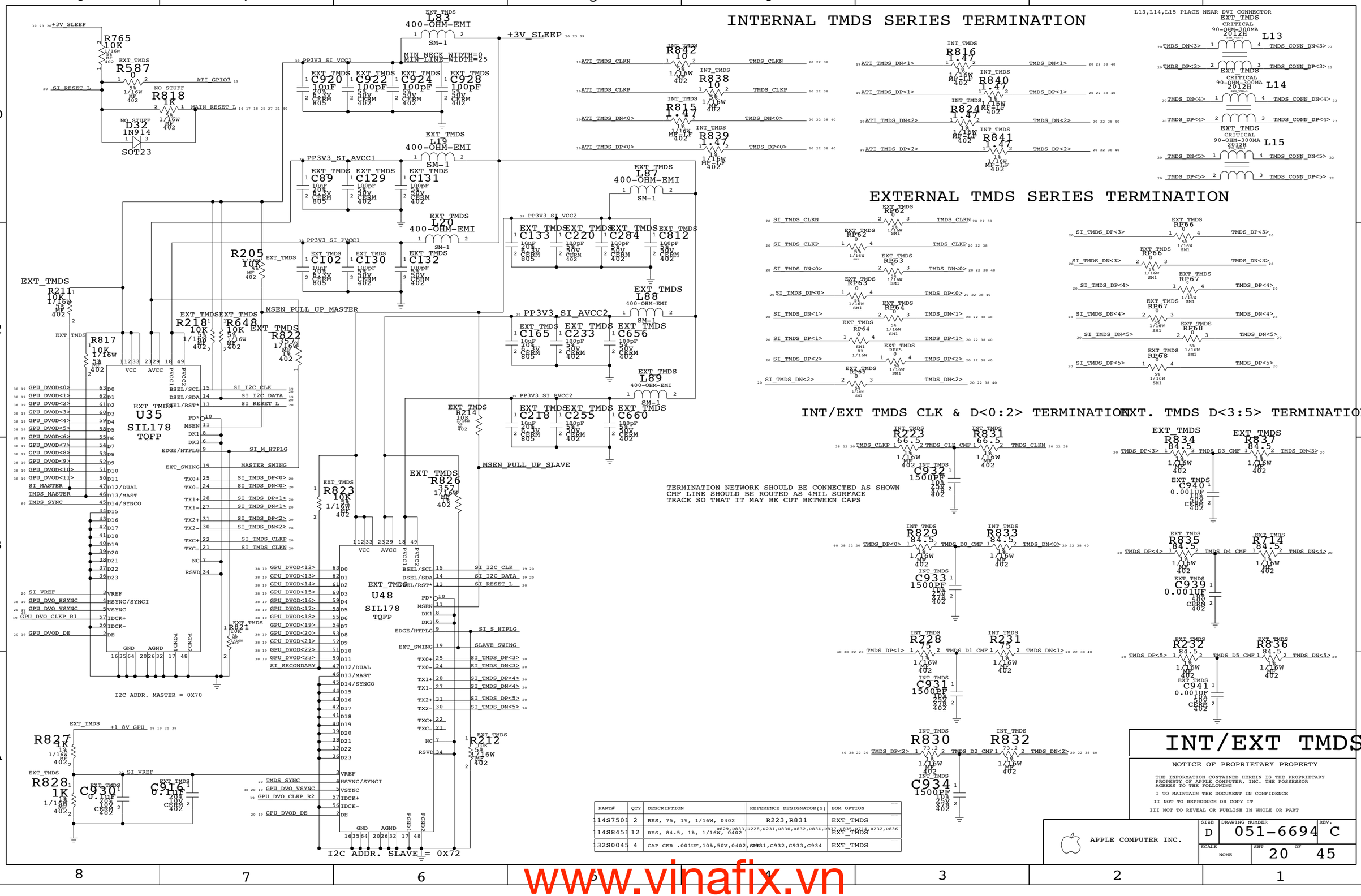

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S7501	2	RES, 75, 1%, 1/16W, 0402	R223,R831	EXT_TMDS
114S8451	12	RES, 84.5, 1%, 1/16W, 0402	R829,R833,R228,R231,R830,R832,R834,R837,R835,R714,R232,R836	EXT_TMDS
132S0045	4	CAP CER .001UF,10%,50V,0402,X7R	C931,C932,C933,C934	EXT_TMDS

GPU PLL - 1.8V

+2_5V_GPU → L58 FERR-220-OHM 0402 (140mA) → +2_5V_GPU_A2VDD
C360 10uF 20% 6.3V CERM 805; C364 0.01uF 20% 16V CERM 402; C374 0.01uF 20% 16V CERM 402

+1_8V_GPU → L55 FERR-220-OHM 0402 (2mA) → +1_8V_GPU_AVDDQ
C339 10uF 20% 6.3V CERM 805; C363 0.01uF 20% 16V CERM 402

+1_8V_GPU → L56 FERR-220-OHM 0402 (AVDD+VDDDI=75mA) → +1_8V_GPU_VDDDI
C358 10uF 20% 6.3V CERM 805; C361 0.01uF 20% 16V CERM 402; C372 0.01uF 20% 16V CERM 402

+GPU_MEM → L57 FERR-220-OHM 0402 → +GPU_MCLK
C359 10uF 20% 6.3V CERM 805; C362 0.01uF 20% 16V CERM 402; C373 0.01uF 20% 16V CERM 402

+2_5V_GPU → U55 MM1571J (100mA MAX) SOT-25A (Total PVDD = 66mA) → +1_8V_ATI_PVDD
CRITICAL; VIN; VOUT; CONT; NOISE; GND; GPU_CORE_OK; ATI_PVDD_BYP
C889 1UF 10% 6.3V CERM 603; C379 0.01uF 20% 16V CERM 402; C380 10uF 20% 6.3V CERM 805

+1_8V_GPU → L65 FERR-220-OHM 0402 → +1_8V_GPU_PLL
C438 10uF 20% 6.3V CERM 805; C865 0.1uF 20% 10V CERM 402; C716 0.01uF 20% 16V CERM 402 (21mA)

+1_8V_GPU → L66 FERR-220-OHM 0402 → +1_8V_GPU_AVDD
C415 10uF 20% 6.3V CERM 805; C437 0.01uF 20% 16V CERM 402; C870 0.01uF 20% 16V CERM 402 (AVDD+VDDDI=75mA)

+2_5V_GPU_A2VDD → AE21 A2VDD0; AF21 A2VDD1; AJ23 A2VDDQ
+1_8V_GPU_AVDDQ → AH23 VDD1DI
+1_8V_GPU_VDDDI → AF20 VDD2DI
+GPU_MCLK → F19 VDDRH0; N6 VDDRH1
AK29 PVDD; AF23 AVDD0; AF24 AVDD1

AGP 4X I/O - 1.5V

+1_5V_AGP → L59 FERR-10-OHM-500MA SM → +1_5V_AGP_GPU (20mA)
C381 0.1uF 20% 10V CERM 402; C420 0.1uF 20% 10V CERM 402; C446 0.1uF 20% 10V CERM 402; C543 0.1uF 20% 10V CERM 402; C871 10uF 20% 6.3V CERM 805
C382 0.01uF 20% 16V CERM 402; C421 0.01uF 20% 16V CERM 402; C447 0.01uF 20% 16V CERM 402; C671 0.01uF 20% 16V CERM 402

K25 L25 T25 Y28 K27 AA25 K26 L26 M26 N26 P26 R26 T26 U26 V26 Y26 AA26 AB26 AC26 → VDDP

MEMORY CORE - 2.5V

+GPU_MEM → L63 FERR-220-OHM 0805 → +GPU_MEMCORE (1800mA)
C383 0.1uF 20% 10V CERM 402; C425 0.1uF 20% 10V CERM 402; C866 0.1uF 20% 10V CERM 402; C672 0.1uF 20% 10V CERM 402; C715 10uF 20% 6.3V CERM 805
C408 0.01uF 20% 16V CERM 402; C426 0.01uF 20% 16V CERM 402; C450 0.01uF 20% 16V CERM 402; C701 0.01uF 20% 16V CERM 402

E5 E6 E12 E13 E18 E19 E20 E26 F26 → VDDM

LVDS PLL - 1.8V

+1_8V_GPU → L61 FERR-220-OHM 0402 → +1_8V_GPU_ENLPLL (40mA)
C409 10uF 20% 6.3V CERM 805; C428 0.01uF 20% 16V CERM 402; C867 0.01uF 20% 16V CERM 402
EXT_TMDS R279 0 5% 1/16W MF 603 → +1_8V_GPU_TP_PLL
C877 10uF 20% 6.3V CERM 805; C878 0.01uF 20% 16V CERM 402

E7 H26 E9 E10 E11 E14 E15 E16 E17 E27 E22 E23 E24 E25 → VDDR1

MEMORY PLL - 1.8V

+1_8V_ATI_PVDD → L62 FERR-220-OHM 0402 → +1_8V_GPU_MEMPLL
C411 10uF 20% 6.3V CERM 805; C429 0.01uF 20% 16V CERM 402

AK21 LPVDD; AK11 TPVDD; A7 MPVDD (20mA)

LVDS - 2.5V

+2_5V_GPU → L64 FERR-10-OHM-500MA SM (NO STUFF)
+2_8V_GPU_LVDS_LDO → L17 FERR-10-OHM-500MA SM → +2_5V_GPU_PNLIO (350mA)
C412 10uF 20% 6.3V CERM 805; C434 0.01uF 20% 16V CERM 402; C868 0.01uF 20% 16V CERM 402

AE16 LVDDR_18; AF16 LVDDR_18; AG16 LVDDR_25; AF17 LVDDR_25
AG12 TXVDDR0; AG13 TXVDDR1; AG14 TXVDDR2; AG15 TXVDDR3

LVDS/TMDS - 1.8V

+1_8V_GPU → L60 FERR-220-OHM 0402 → +1_8V_GPU_PNLIO (180mA)
C413 10uF 20% 6.3V CERM 805; C435 0.1uF 20% 10V CERM 402; C864 0.1uF 20% 10V CERM 402; C704 0.1uF 20% 10V CERM 402
C414 0.1uF 20% 10V CERM 402; C436 0.01uF 20% 16V CERM 402; C869 0.01uF 20% 16V CERM 402

GPU POWER SOURCES - 1.5V, 1.8V, 2.5V & 3.3V

+1_5V_SLEEP → R722 0 5% 1/10W MF 805 → +1_5V_AGP — 1.5V
+1_8V_SLEEP → R284 0 5% 1/10W MF 805 → +1_8V_GPU — 1.8V
+1_8V_SLEEP, +2_5V_SLEEP → ATI_MEMIO_LO R729 0 5% 1/4W MF 1210; ATI_MEMIO_HI R728 0 5% 1/4W MF 1210 → +GPU_MEM — 2.5V / 1.8V
+2_5V_SLEEP → R721 0 5% 1/10W MF 805 → +2_5V_GPU — 2.5V
+3V_SLEEP → R299 0 5% 1/10W MF 805 → +3V_GPU — 3.3V

+3V_GPU → U8 MAX8860 (OMIT) UMAX
IN; SHDN*; SET; GND; OUT1; OUT2; FAULT*; CC
C910 2.2UF 20% 6.3V CERM1 603; C911 0.033UF 20% 10V X7R 402; C912 2.2UF 20% 6.3V CERM1 603
R635 100K 5% 1/16W MF 402 → MAX8860_FAULT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S0828	1	IC,MAX8860,LDO,2.77V	U8	?

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0647	353S0828	?	U8	ALT FOR 2.82V PART

GPU I/O

U44 RAGE_MOBILITY M11-CSP64 64MB BGA (4 OF 6) (OMIT)

PVSS AK30; A2VSSQ AF22; A2VSSQ AJ22; A2VSSN0 AE22; AVSSN1 AE23; A2VSSN0 AE19; A2VSSN1 AE20; VSS1DI AG23; VSS2DI AF19; VSSRH0 F20; VSSRH1 M6
F5 G5 H5 J5 K5 L5 M5 N5 P5 R5 T5 U5 V5 W5 Y5 AA5 AB5 AC5 AD5 G26 K6 R6 Y6 AA6 F8 F9 F15 F16 F21 F22 H25 J25 J26 → VDDR1
AF6 AE7 AF7 AE8 AF8 AE9 AF9 AF10 AD25 AE25 AE26 AF26 → VDDR3
LVSS AJ21; TPVSS AJ11; MPVSS A6
LVSSR0 AH16; LVSSR1 AG17; LVSSR2 AH17; LVSSR3 AF18
DVOVMODE AH12; TXVSSR1 AH13; TXVSSR2 AH14; TXVSSR3 AH15

MEMORY I/O

+GPU_MEM → L67 FERR-220-OHM 0805 (1200mA) → GPU_MEM_IO_FLT
C872 10uF 20% 6.3V CERM 805; C875 0.1uF 20% 10V CERM 402; C850 0.1uF 20% 10V CERM 402; C855 0.1uF 20% 10V CERM 402; C860 0.1uF 20% 10V CERM 402
C873 0.1uF 20% 10V CERM 402; C876 0.1uF 20% 10V CERM 402; C851 0.1uF 20% 10V CERM 402; C856 0.1uF 20% 10V CERM 402; C861 0.1uF 20% 10V CERM 402
C874 0.1uF 20% 10V CERM 402; C847 0.1uF 20% 10V CERM 402; C852 0.1uF 20% 10V CERM 402; C857 0.1uF 20% 10V CERM 402; C862 0.01uF 20% 16V CERM 402

3.3V IO SUPPLY (Max Current varies, depends on usage)

+2_5V_GPU → U54 INT_TMDS MM1571J SOT-25A → +1_8V_ATI_TPVDD
CRITICAL; VIN; VOUT; CONT; NOISE; GND; GPU_CORE_OK; ATI_TPVDD_BYP
C879 1UF 10% 6.3V CERM 603; C880 0.01UF 10% 16V CERM 402; C881 10UF 20% 6.3V CERM 805
L69 FERR-220-OHM 0402 → +1_8V_GPU_TP_PLL

+1_8V_GPU → L16 FERR-10-OHM-500MA SM → EXT_TMDS
+1_8V_DVO_F
C304 10uF 20% 6.3V CERM 805; C327 0.1uF 20% 10V CERM 402; C647 0.1uF 20% 10V CERM 402
R268 0 5% 1/16W MF 603 → INT_TMDS

+3V_GPU → L68 FERR-10-OHM-500MA SM → +3V_GPU_FLT
C722 10uF 20% 6.3V CERM 805; C848 0.1uF 20% 10V CERM 402; C853 0.1uF 20% 10V CERM 402; C858 0.1uF 20% 10V CERM 402; C863 0.1uF 20% 10V CERM 402
C725 0.1uF 20% 10V CERM 402; C849 0.1uF 20% 10V CERM 402; C854 0.1uF 20% 10V CERM 402; C859 0.1uF 20% 10V CERM 402

EXT_TMDS R255 0 5% 1/16W MF 402 → +1_8V_GPU
ATI_DVOVMODE
INT_TMDS R251 0 5% 1/16W MF 402

M11 SHUT DOWN POWER SEQUENCING

+2_5V_SLEEP (OMIT) XW27 SM → DP7 BAS16TW SOT-363 → +2_5V_SLEEP_NECK2
+3V_SLEEP_NECK → (OMIT) XW30 SM
+1_8V_SLEEP (OMIT) XW28 SM → DP7 BAS16TW SOT-363 → +1_8V_SLEEP_NECK
+1_5V_SLEEP (OMIT) XW29 SM → DP7 BAS16TW SOT-363 → +1_5V_SLEEP_NECK

M11 POWER

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EXTERNAL VIDEO (DVI) INTERFACE

ANALOG FILTERING PLACE CLOSE TO CONNECTOR

FL2 CRITICAL LCFILTER SM-220MHZ — GPU_B → VGA_B
FL1 CRITICAL LCFILTER SM-220MHZ — GPU_G → VGA_G
FL3 CRITICAL LCFILTER SM-220MHZ — GPU_R → VGA_R
C685 3.3PF 0.25% 50V CERM 402
C676 3.3PF 0.25% 50V CERM 402
C684 3.3PF 0.25% 50V CERM 402

+3V_MAIN

CRITICAL 74AHC1G32 SM U56 — ATI_HSYNC → R718 33 5% 1/16W MF 402 → VGA_HSYNC_BUF → VGA_HSYNC
CRITICAL 74AHC1G32 SM U57 — ATI_VSYNC → R687 33 5% 1/16W MF 402 → VGA_VSYNC_BUF → VGA_VSYNC

VGA VSYNC BUFFERS

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)

+5V_SLEEP F1 0.5AMP-13.2V SM — +5V_DDC_SLEEP_UF → L23 400-OHM-EMI SM-1 → +5V_DDC_SLEEP

Isolation required for DVI power switch

D21 SM MBR0530 — DDC_CLK_ISO

CRITICAL J14 QH1112 F-RT-TH

TMDS_CONN_DN<0>	17	19	TMDS_CONN_DN<2>
TMDS_CONN_DP<0>	18	20	TMDS_CONN_DP<2>
TMDS_CONN_DN<5>	20	21	TMDS_CONN_DN<4>
TMDS_CONN_DP<5>	21	22	TMDS_CONN_DP<4>
	22	23	TMDS_CONN_DN<3>
	23	24	TMDS_CONN_DP<3>
TMDS_CONN_CLKP	24	25	DVI_DDC_CLK_UF
TMDS_CONN_CLKN	33	31	(+5V_DDC_SLEEP)
	34	32	DVI_DDC_DATA_UF
	C3	C1	VGA_VSYNC
VGA_B	C5B	C5A	DVI_HPD_UF
VGA_HSYNC	C4	C2	VGA_R
	35	36	VGA_G

R655 4.7K 5% 1/16W MF 402 — DDC_CLK_ISO
R661 4.7K 5% 1/16W MF 402 — DVI_DDC_CLK
R670 100 5% 1/16W MF 402
R649 100 5% 1/16W MF 402 — DVI_DDC_DATA
R650 100 5% 1/16W MF 402 — DVI_HPD
C706 100pF 5% 50V CERM 402
C669 100pF 5% 50V CERM 402
C1 100pF 5% 50V CERM 402
C710 0.01UF 20% 50V CERM 603
R706 0 5% 1/16W MF 402
R1 0 5% 1/16W MF 402 — PLACE NEAR C5A & C5B
PLACE NEAR 3, 11 & 19
CHGND5
CHGND1

3V LEVEL SHIFTERS

+3V_SLEEP

Q38 2N7002DW SOT-363 — DVI_DDC_CLK
Q38 2N7002DW SOT-363 — DVI_DDC_DATA
Q35 2N7002DW SOT-363 — DVI_HPD

R662 10K 5% 1/16W MF 402 — GPU_DVI_DDC_CLK
R671 10K 5% 1/16W MF 402 — GPU_DVI_DDC_DATA
R694 100K 5% 1/16W MF 402 — GPU_HPD

NOTE: Pulldown for DVI_HPD provided by DVI power switch interface
NOTE: DVI_HPD SHARES Q68 WITH ALS BECAUSE OF BOARD REAL ESTATE

DVI POWER SWITCH

Power key detect path when system is shutdown or asleep.. DDC CLK is isolated from NV17M DURING SHUTDOWN. WHEN power key on remote device is pressed, 5V will be driven into DDC CLK. since both rails will be low, TP0610 will turn on, driving SOFT_PWR_ON_L low. As both rails rise, TP0610 will turn off, as will remote device path into DDC CLK. Isolation will be disabled as well.

Q40 TP0610 SM — DVI_DDC_CLK_UP → DVI_TURN_ON
R690 680 5% 1/16W MF 402 — DVI_TURN_ON → DVI_TURN_ON_ILIM
R688 330 5% 1/16W MF 402 — Pulldown prevents 3904 from turning on when DVI monitor has active self-powered DDC clock pullup.
R691 10K 5% 1/16W MF 402
Q42 2N3904 SM — DVI_TURN_ON_BASE → SOFT_PWR_ON_L

Power key detect path when system is running. 3.3V when power key +3V_SLEEP on remote device pressed. HPD will be driven to 5V. COMPARATOR ENABLED BY NV17MAP GPIO.

R680 68.1 1% 1/16W MF 402
C696 0.1UF 20% 10V CERM 402
U46 LMC7211 SM CRITICAL — HPD_4V_REF
R663 10K 1% 1/16W MF 402 — DVI_HPD_UP1 → DVI_HPD_DN
R686 10K 1% 1/16W MF 402
R681 100K 1% 1/16W MF 402
HPD_PWR_SW
Q41 2N7002DW SOT-363 — HPD_ON
+PBUS
Q45 TP0610 SM
R696 100K 5% 1/16W MF 402
R704 100K 5% 1/16W MF 402
COMP_ENABLE
COMP_DISABLE
HPD_ON_RC
R703 330 5% 1/16W MF 402
R700 20K 5% 1/16W MF 402
HPD_BASE
Q44 2N3904 SM
C703 47UF 20% 6.3V CERM 1210
R705 68K 5% 1/16W MF 402

NEED PULL-DOWN BECAUSE THIS SIGNAL IS TRISTATED INITIALLY

HPD_PWR_SNS_EN
R213 100K 1% 1/16W MF 402
Q41 2N7002DW SOT-363

LCD INTERFACE

LVDS INTERFACE

100K pull-ups are for no-panel case (development) Panel has 2K pull-ups

+3V_SLEEP
R342 100K 5% 1/16W MF 402
R320 100K 5% 1/16W MF 402 — +3V_LCD
(LVDS DDC POWER)
LVDS_DDC_CLK
LVDS_DDC_DATA
NO STUFF
C449 0.001uF 20% 50V CERM 402
C452 0.001uF 20% 50V CERM 402
CHGND4
C416 0.001uF 20% 50V CERM 402

CRITICAL J6 G-501973 F-RT-SM

	1	2	
	3	4	(LVDS DDC POWER)
	5	6	NC
	7	8	LVDS_L0N
	9	10	LVDS_L0P
LVDS_L1N	11	12	LVDS_L1P
LVDS_L2N	13	14	LVDS_L2P
CLKLVDS_LN	15	16	
CLKLVDS_LP	17	18	
LVDS_U0N	19	20	LVDS_U0P
LVDS_U1N	21	22	LVDS_U1P
LVDS_U2N	23	24	LVDS_U2P
CLKLVDS_UN	25	26	
CLKLVDS_UP	27	28	
	29	30	
	31	32	
	33	34	

C500 0.001uF 20% 50V CERM 402

TMDS FILTERING PLACE CLOSE TO CONNECTOR

L72 CRITICAL 90-OHM-300MA 2012H — TMDS_DN<0> → TMDS_CONN_DN<0>
L73 CRITICAL 90-OHM-300MA 2012H — TMDS_DP<0> → TMDS_CONN_DP<0>
L21 CRITICAL 165-OHM SM — TMDS_CLKP → TMDS_CONN_CLKP; TMDS_CLKN → TMDS_CONN_CLKN
L74 CRITICAL 90-OHM-300MA 2012H — TMDS_DN<2> → TMDS_CONN_DN<2>
L74 CRITICAL 90-OHM-300MA 2012H — TMDS_DP<2> → TMDS_CONN_DP<2>
L74 CRITICAL 90-OHM-300MA 2012H — TMDS_DN<1> → TMDS_CONN_DN<1>
L74 CRITICAL 90-OHM-300MA 2012H — TMDS_DP<1> → TMDS_CONN_DP<1>

S-VIDEO/COMP OUT INTERFACE

Place GND shorts at graphics controller

XW12 SM — GPU_TV_GND1 → L26 FERR-10-OHM-500MA SM → TV_GND1
XW13 SM — GPU_TV_GND2 → L28 FERR-10-OHM-500MA SM → TV_GND2
L25 3.3UH 0603 — GPU_Y → TV_Y
L29 3.3UH 0603 — GPU_C → TV_C
L27 3.3UH 0603 — GPU_COMP → TV_COMP
C712 0.01UF 20% 50V CERM 603
C702 560PF 10% 50V CERM 402
C707 560PF 10% 50V CERM 402
C718 560PF 10% 50V CERM 402
C724 560PF 10% 50V CERM 402
C714 560PF 10% 50V CERM 402
C713 560PF 10% 50V CERM 402
C717 0.01UF 20% 50V CERM 603
CRITICAL J15 MINIDIN RT-TH MH177
CHGND1

Place GND shorts at graphics controller

LCD POWER SWITCHES

+3V_MAIN
R400 100K 5% 1/16W MF 402
C484 2200pF 5% 50V CERM 603
R391 100K 5% 1/16W MF 402 — LCD_DIGON_L → LCD_PWREN
Q11 SI3443DV TSOP — +3V_LCD_SW
Q8 2N7002 SM — FP_PWR_EN
L6 FERR-250-OHM SM
C474 0.001uF 20% 50V CERM 402
CHGND4

SHARES LOGIC WITH KB RESET SIGNALS (PG 28)
R724 0 5% 1/16W MF 402
C744 0.01uF 20% 50V CERM 603
CHGND2

INVERTER INTERFACE

+PBUS
L33 FERR-1K-OHM-EMI SM — +12_8V_INV
+5V_MAIN
Q7 FDG6324L SC70-6
R317 100K 5% 1/16W MF 402 — FP_PWR_EN
+5V_INV_UF_SW
L32 400-OHM-EMI SM-1 — +5V_INV_SW
C440 10UF 20% 6.3V CERM 805
C746 0.001UF 20% 50V CERM 402
CRITICAL J7 SM-2MT
C749 0.001UF 20% 50V CERM 402
C739 0.001UF 20% 50V CERM 402
L31 400-OHM-EMI SM-1 — BRIGHT_PWM
+3V_PMU
C552 0.1UF 20% 10V CERM 402
U24 74LVC32 TSSOP — INV_ON_PWM1 → BRIGHT_PWM_UF
INVERTER EXPECTS ACTIVE HIGH SIGNAL
CHGND2

VIDEO CONNECTORS

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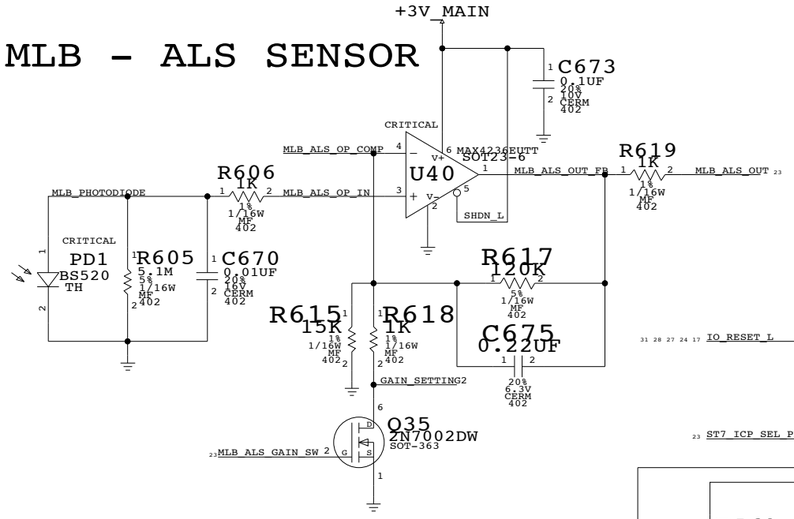
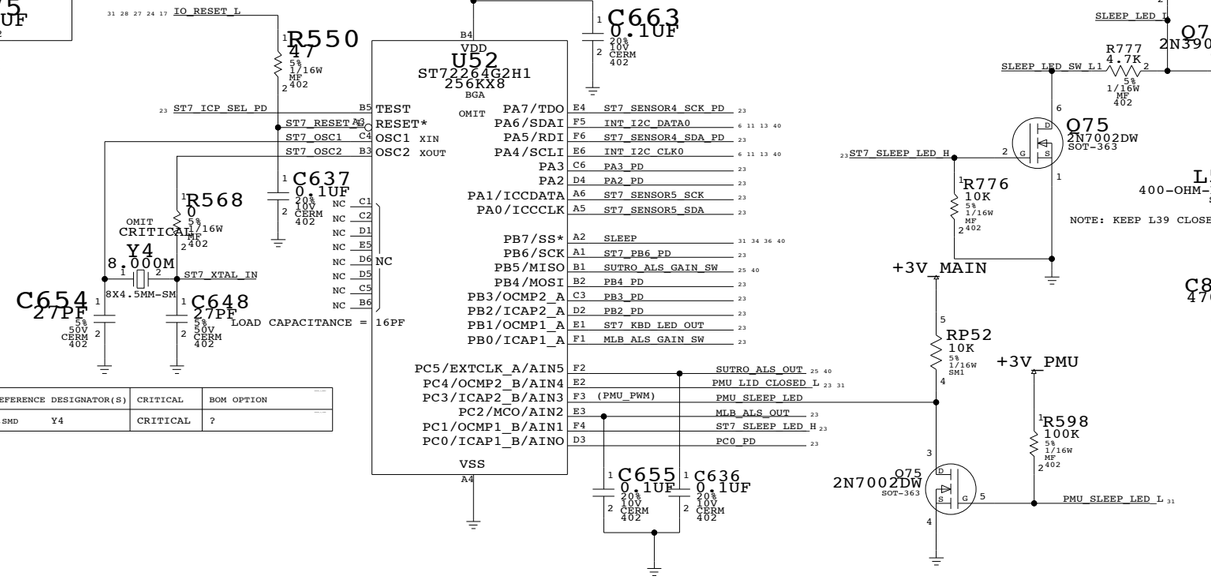
MLB - ALS SENSOR



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0856	353S0504	?	U40	ALT FOR SUPPLY PROBLEM

LMU

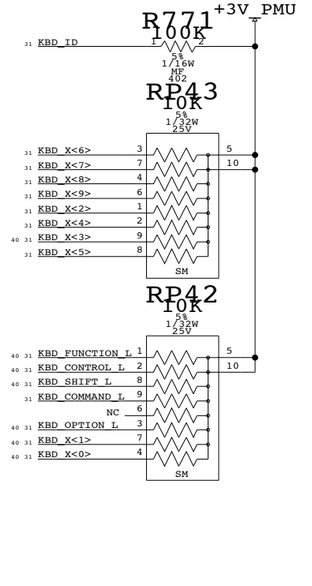
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1194	1	IC,LMU,P84	U52	CRITICAL	?



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0091	1	XTAL,CER,LOW PROF,8.000MHZ,8X4.5MM,SMD	Y4	CRITICAL	?

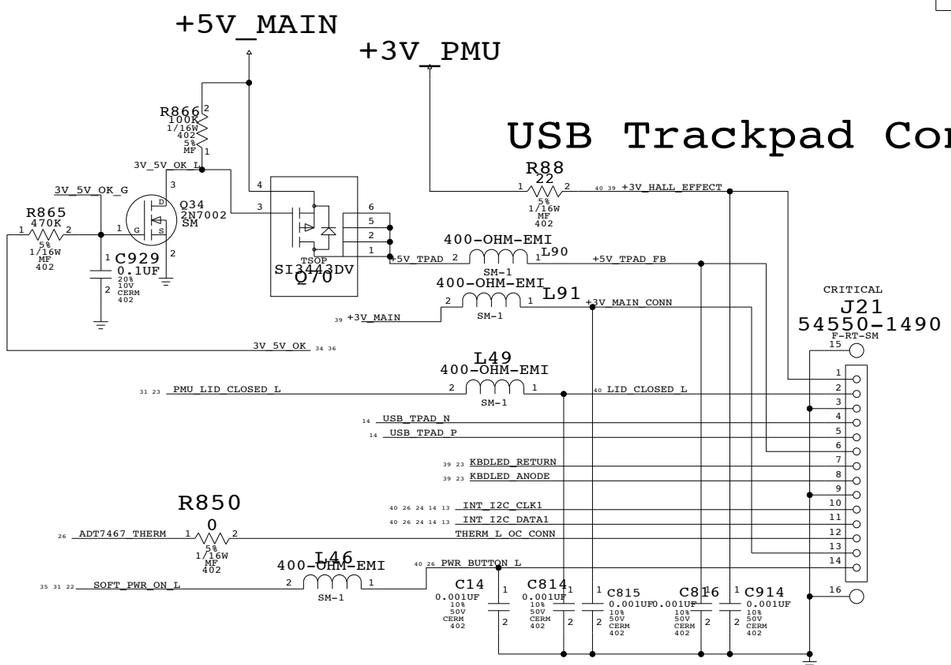
SLEEP LED

KEYBOARD PULLUPS

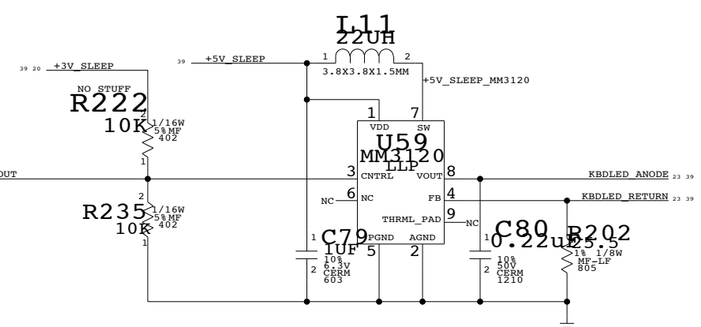


LMU PULL-DOWNS

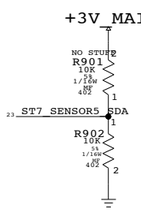
USB Trackpad Connector



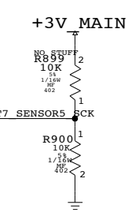
Keyboard LED Driver



+3V_MAIN



+3V_MAIN



LMU/BOOTBANGER/SPIDEY

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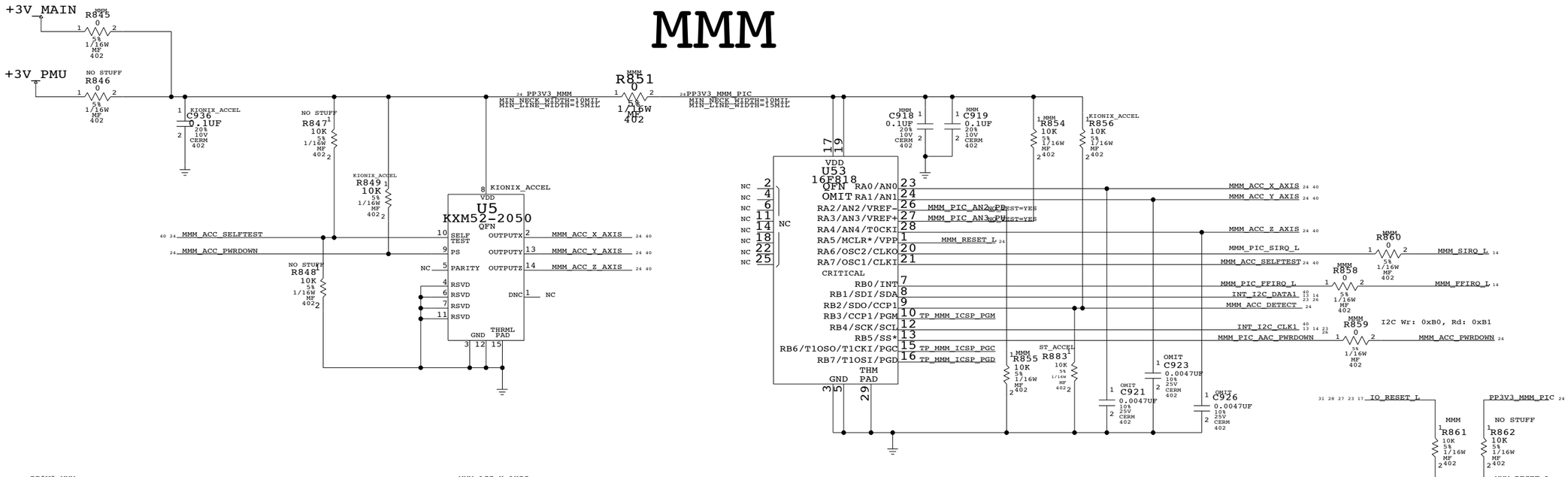
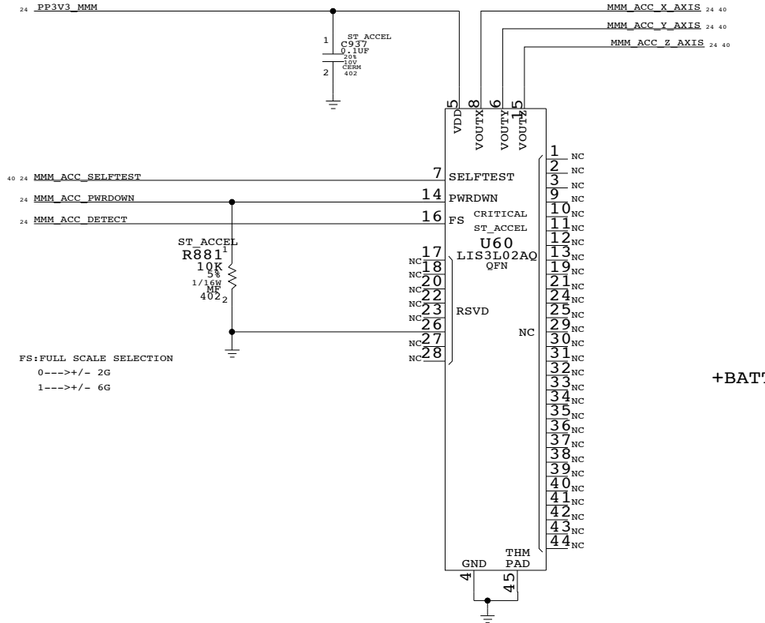
MMM

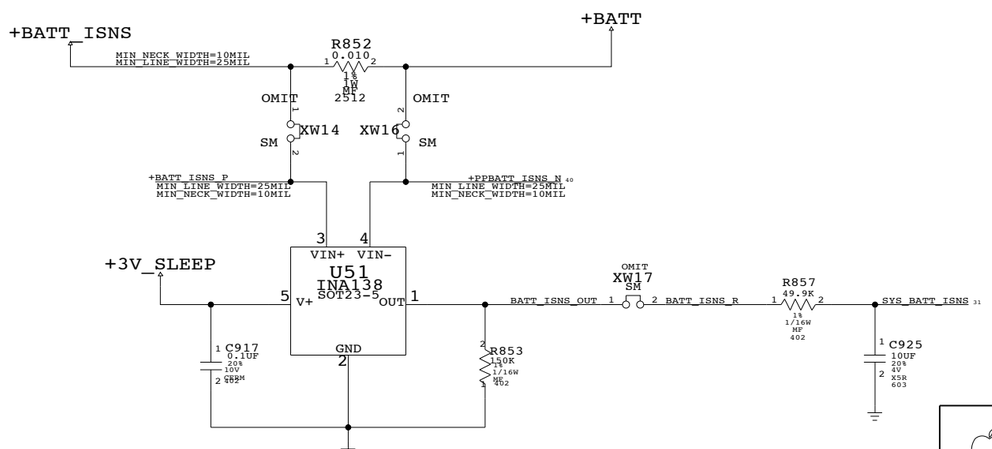




PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
1325I0131	3	CAP CER .033UF,10%,16V,X7R/X5R,0402,SMD	C921,C923,C926	KIONIX_ACCEL
1325I0072	3	CAP CER .0015UF,10%,25V,X7R,0402,SMD	C921,C923,C926	ST_ACCEL
341S1630	1	IC,UCTLR,MMM,PIC16F818,SMD,W/PROGRAM	U53	MMM

BOM TABLE USED TO COMPENSATE DIFFERENT OUTPUT RESISTANCE

BATTERY CURRENT SENSE



MMM, BATTERY CURRENT SENSE

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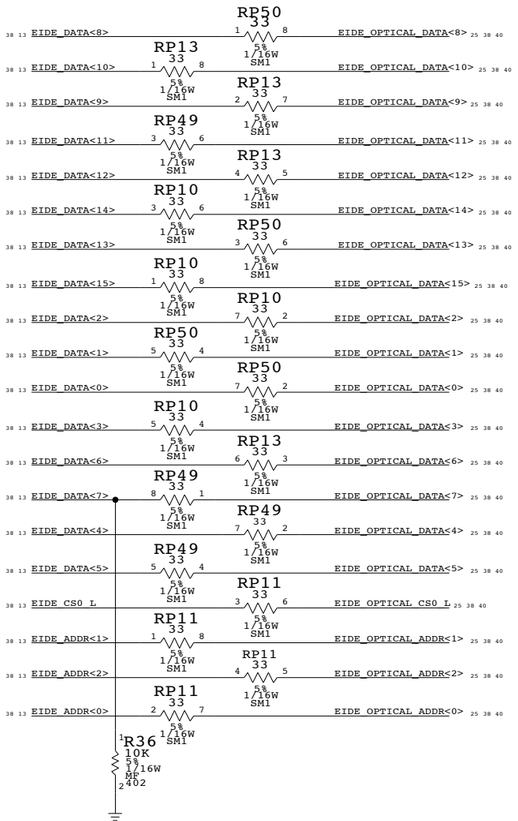
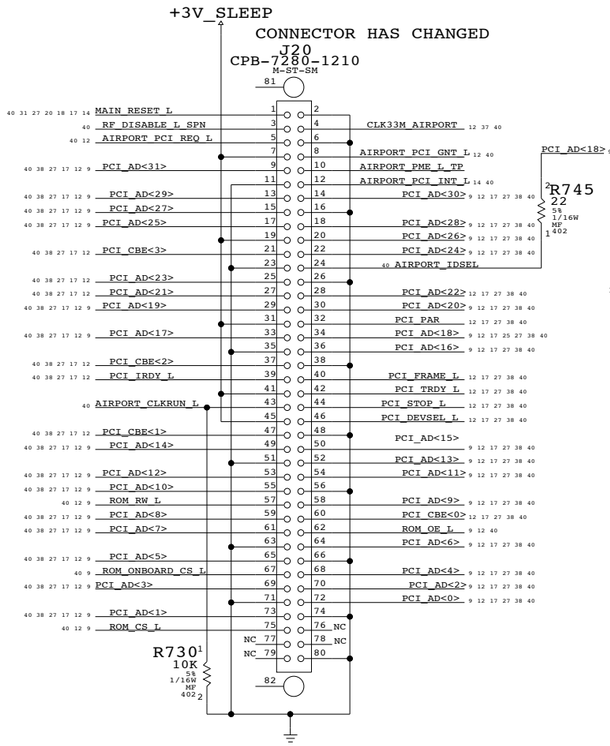
SIZE	DRAWING NUMBER	REV.
D	051-6694	C
SCALE: NONE	SHT 24 OF 45	

EIDE SERIES TERMINATION

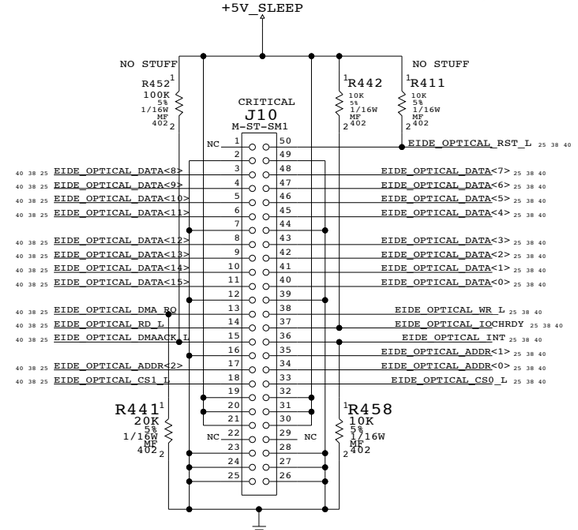
PLACE TERMINATORS NEAR INTREPID



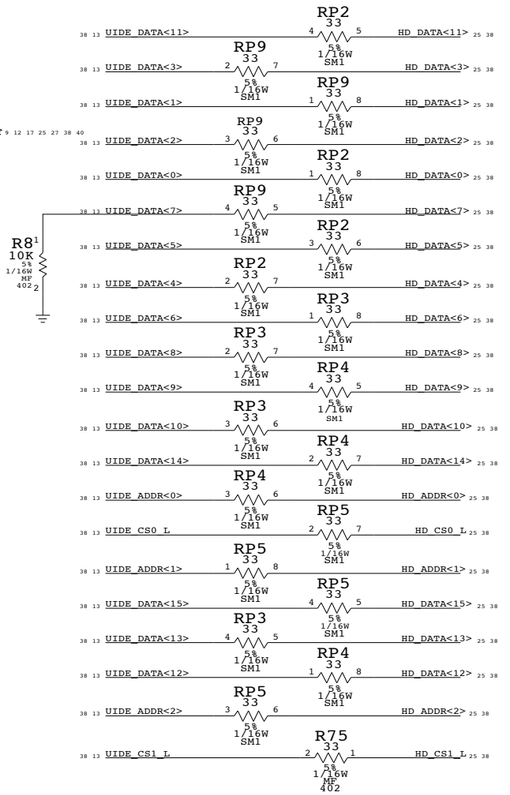
WIRELESS INTERFACE



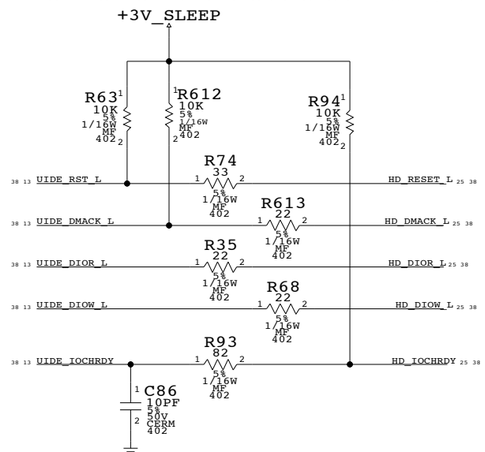
OPTICAL DRIVE INTERFACE (EIDE)



PLACE SERIES R CLOSE TO INTERPID

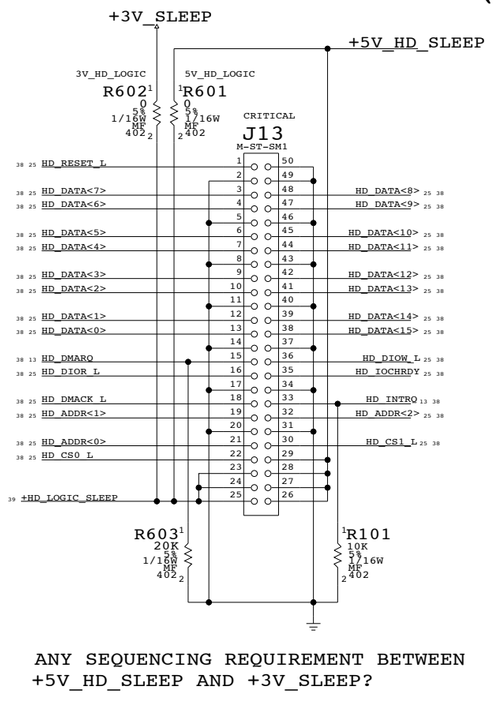


PLACE PULLUP RESISTORS CLOSE TO INTREPID



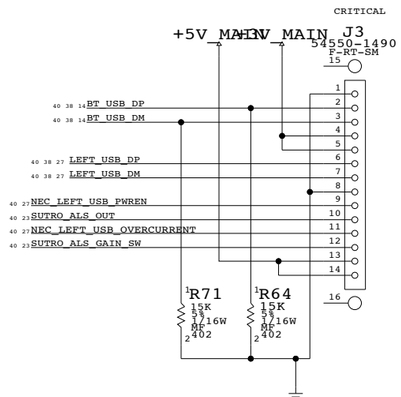
IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V

HARD DRIVE INTERFACE (UATA100)



ANY SEQUENCING REQUIREMENT BETWEEN +5V_HD_SLEEP AND +3V_SLEEP?

BLUETOOTH/LEFT-SIDE USB



INTERNAL I/O CONNECTORS

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SCALE: NONE	SHT 25 OF 45	

SOUND BOARD (SOUSAPHONE)

AUDIO - CRYSTAL SND - INTREPID

Sound Board Connector

Place shorts at 3.3V and 5V regulators

+5V_MAIN

XW9 SM — This is an internal board short. PLACE XW9 CLOSE TO 5V SWITCHER (U27)

XW10 SM +3V_SLEEP — This is an internal board short

CRITICAL J12 QT500406-L111 M-ST-SM1

R534 0 5% 1/16W MF 402 — SOUND_SPDIF_GPO0 — SPDIF_GPO0

R581 0 5% 1/16W MF 402 — AUDIO_MCLK_SEL — AUDIO_EXT_MCLK_SEL

R552 0 5% 1/16W MF 402 — AUDIO_LO_SPDIF_PLUG — AUDIO_LO_OPTICAL_PLUG_L

R582 0 5% 1/16W MF 402 — AUDIO_LI_SPDIF_PLUG — AUDIO_LI_OPTICAL_PLUG_L

R918 0 5% 1/16W MF 402 — +5V_MAIN_AUDIO — +5V_MAIN_AUDIO_0

R917 NO STUFF 0 5% 1/16W MF 402

SPDIF_GPO0	13	14	AUDIO_LO_DET_L
+3V_SLEEP_AUDIO	15	16	AUDIO_LO_OPTICAL_PLUG_L
AUDIO_EXT_MCLK_SEL	17	18	AUDIO_LI_DET_L
AUDIO_LO_MUTE_L	19	20	AUDIO_LI_OPTICAL_PLUG_L
	21	22	AUDIO_SPKR_MUTE_F
I2S0_MCLK_F	23	24	
I2S0_BITCLK_F	25	26	I2S0_RESET_L_F
I2S0_SYNC_F	27	28	I2S1_RESET_L_F
I2S0_SB_TO_DEV_DTO_F	29	30	
I2S0_DEV_TO_SB_DTI_F	31	32	INT_I2C_DATA2
	33	34	INT_I2C_CLK2
I2S1_BITCLK_F	35	36	
I2S1_SYNC_F	37	38	SLEEP_ANODE
I2S1_DEV_TO_SB_DTI_F	39	40	(SLEEP_LED_GND)
	43	44	

VER_1 516S0154

XW11 SM — SND_AGND — This is an internal board short

L77 FERR-220-OHM 0402 — SND_SYNC — I2S0_SYNC_F
C895 NO STUFF 0.01UF 20% 16V CERM 402

L80 FERR-220-OHM 0402 — SND_CLKOUT — I2S0_MCLK_F
C899 NO STUFF 0.01UF 20% 16V CERM 402

L81 FERR-220-OHM 0402 — INT_AUDIO_TO_SND — I2S0_DEV_TO_SB_DTI_F
C896 NO STUFF 0.01UF 20% 16V CERM 402

L82 FERR-220-OHM 0402 — SND_TO_AUDIO — I2S0_SB_TO_DEV_DTO_F
C897 NO STUFF 0.01UF 20% 16V CERM 402

L76 FERR-220-OHM 0402 — SND_AMP_MUTE_INV — AUDIO_SPKR_MUTE_F
C898 NO STUFF 0.01UF 20% 16V CERM 402

L78 FERR-220-OHM 0402 — SND_HW_RESET_L — I2S0_RESET_L_F
C900 NO STUFF 0.01UF 20% 16V CERM 402

L79 FERR-220-OHM 0402 — SND_SCLK — I2S0_BITCLK_F
C901 NO STUFF 0.01UF 20% 16V CERM 402

L84 FERR-220-OHM 0402 — MOD_SYNC — I2S1_SYNC_F
C81 NO STUFF 0.01UF 20% 16V CERM 402

L48 FERR-220-OHM 0402 — MOD_BITCLK — I2S1_BITCLK_F
C82 NO STUFF 0.01UF 20% 16V CERM 402

L85 FERR-220-OHM 0402 — INT_MOD_DTI — I2S1_DEV_TO_SB_DTI_F
C87 NO STUFF 0.01UF 20% 16V CERM 402

L86 FERR-220-OHM 0402 — AUDIO_SPDIF_RESET — I2S1_RESET_L_F
C88 NO STUFF 0.01UF 20% 16V CERM 402

CAPS FOR EMI EXPERIMENTATION ONLY

KEEP STUFFING RESISTORS CLOSE TO ADT7467 CONTROLLER

R719 0 5% 1/16W MF 402 — CPU_M_DP — THERM1_DP
R725 0 5% 1/16W MF 402 — CPU_M_DM — THERM1_DM
R713 0 5% 1/16W MF 402 — SUPPLY_M_DP — THERM2_DP
R716 0 5% 1/16W MF 402 — SUPPLY_M_DM — THERM2_DM

KEEP STUFFING RESISTORS CLOSE TO ADT7467 CONTROLLER

PLACE CAPS AS CLOSE TO THERMISTORS AS POSSIBLE

PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY

PLACE CLOSE TO CPU

MAIN1

SUPPLY_M_DP — C681 0.001UF 20% 50V CERM 402 — Q66 2N3904 SM — SUPPLY_M_DM

MAIN2

CPU_M_DP — C668 0.001UF 20% 50V CERM 402 — Q39 2N3904 SM — CPU_M_DM

PLACE UNDERNEATH UPPER RAM

ALTERNATE1

THERM1_A_DP — C678 NO STUFF 0.001UF 20% 50V CERM 402 — Q47 NO STUFF 2N3904 SM — THERM1_A_DM

PLACE CLOSE TO BATTERY CHARGER/VCORE

ALTERNATE2

THERM2_A_DP — C651 NO STUFF 0.001UF 20% 50V CERM 402 — Q62 NO STUFF 2N3904 SM — THERM2_A_DM

R628 NO STUFF 0 5% 1/16W MF 402 — CPU_THERM_DP — THERM1_DP
R620 0 5% 1/16W MF 402 — CPU_THERM_DM1 — THERM1_DM
R723 NO STUFF 0 5% 1/16W MF 402 — THERM1_A_DP — THERM1_DM
R726 NO STUFF 0 5% 1/16W MF 402 — THERM1_A_DM — THERM2_DM
R710 NO STUFF 0 5% 1/16W MF 402 — THERM2_A_DP — THERM2_DP
R717 0 5% 1/16W MF 402 — THERM2_A_DM — THERM2_DM

MODEM

SUPPORTS BOTH THE LAST DASH AND Q52 SOFT MODEM

+5V_MAIN

R874 100K 5% 1/16W MF 402 — SND_AMP_MUTE

R224 NO STUFF 10K 5% 1/16W MF 402 — SND_AMP_MUTE_INV

Q33 NO STUFF 2N7002 SM

R915 0 5% 1/16W MF 402

Q26 2N7002DW SOT-363 — SND_AMP_MUTE_L

AMP_CONTROL — R875 100K 5% 1/16W MF 402 — INT_PU_RESET_L

Q26 2N7002DW SOT-363 — SND_AMP_MUTE

+3V_MAIN

C767 10UF 20% 6.3V CERM 805 — NO STUFF C513 0.1UF 20% 10V CERM 402

R405 10K 5% 1/16W MF 402 — NO STUFF C478 0.1UF 20% 10V CERM 402 — C469 10UF 20% 6.3V CERM 805

CRITICAL J8 QT510166-L010 F-ST-SM1

MOD_DTO	1	2	MOD_SYNC
MOD_CLKOUT	3	4	INT_MOD_DTI
	5	6	MOD_BITCLK
COMM_RESET_L	7	8	
COMM_SHUTDOWN	9	10	MODEM_USB_DM
INT_I2C_CLK2	11	12	MODEM_USB_DP
INT_I2C_DATA2	13	15	COMM_RING_DET_L
	15	16	

+5V_MAIN

SERIAL_DEBUG CRITICAL J16 M-ST-5087 SM

COMM_TXD_L	1	10	COMM_DTR_L
COMM_TRXC	2	9	COMM_RTS_L
	3	8	
COMM_GPIO_L	4	7	COMM_RXD
	5	6	

SERIAL DEBUG INTERFACE

DEBUG POWER BUTTON

R527 NO STUFF 0 5% 1/16W MF 603 — PWR_BUTTON_L

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S0608	1	IC,ADT7460,FAN,CTLR,16P,QSOP	U3	ADT7460

+3V_MAIN

R872 10K 5% 1/16W MF 402 — AUDIO_LO_MUTE_L

R689 100K 5% 1/16W MF 402

Q31 2N7002DW SOT-363 — SND_HP_MUTE

Q31 2N7002DW SOT-363 — SND_HP_MUTE_L

R873 100K 5% 1/16W MF 402 — AMP_CONTROL

FAN INTERFACE

+3V_MAIN

R814 10 5% 1/16W MF 402 — ADT7467_VCC

C904 1UF 20% 10V CERM 603

C711 0.1UF 20% 10V CERM 402

U3 ADT7467 QSOP

ADT7467_VCORE_MON	5	14	VCCP
INT_I2C_DATA1	16		SDA
INT_I2C_CLK1	1		SCL
THERM1_DP	13		D1+
THERM1_DM	12		D1-
THERM2_DP	11		D2+
THERM2_DM	10		D2-
	2		GND
FAN1_PWM_L	15		PWM1
	6		XTO
FAN1_TACH	16		TACH1
FAN2_PWM_L	5		PWM2/ SMBALERT#
FAN2_TACH	7		TACH2
ADT7467_ADR_EN_L	8		PWM3
ADT7460_TACH3_TP	4		TACH3
ADT7467_THERM	9		TACH4/ THERM#/ SMBALERT#/GPIO

NO STUFF C690 0.001UF 20% 50V CERM 402 — NO STUFF C846 0.001UF 20% 50V CERM 402 — C688 0.001UF 20% 50V CERM 402 — NO STUFF C905 0.001UF 20% 50V CERM 402

FAN CONTROLLER

+3V_SLEEP

ADT7460 R692 10K 5% 1/16W MF 402 — R293 10K 5% 1/16W MF 402

ADT7460 R695 10K 5% 1/16W MF 402 — R295 10K 5% 1/16W MF 402

R42 10K 5% 1/16W MF 402

ADT7460_ADR_EN_L

ADT7460_TACH3_TP

ADT7467_THERM

FAN1_PWM_L — FAN1_TACH — FAN2_PWM_L — FAN2_TACH

THERM ISOLATION

+3V_MAIN

R813 100K 5% 1/16W MF 402 — R811 100K 5% 1/16W MF 402 — R812 100K 5% 1/16W MF 402

+3V_PMU_AVCC

THERM_L_OC

THERM_INV

Q87 2N7002DW SOT-363

Q87 2N7002DW SOT-363 — C903 0.1UF 20% 10V CERM 402

ADT7467_THERM

DEBUG JUMPERS

PMU_NMI_BUTTON_L — R537 NO STUFF 0 5% 1/16W MF 603

PMU_RESET_BUTTON_L — R553 NO STUFF 0 5% 1/16W MF 603

LEFT FAN (CPU)

+5V_SLEEP

R679 10K 5% 1/16W MF 402 — R910 NO STUFF 10K 5% 1/16W MF 402 — R908 0 5% 1/16W MF 603

J4 CRITICAL SM-2MT

ADT7467 R878 0 5% 1/16W MF 402

+FAN1_PWR — FAN1_TACH — FAN1_PWM

FAN1_PWM_L

ADT7460 Q78 2N7002DW SOT-363

C134 4.7UF 20% 10V CERM 1206 PLACE CLOSE TO CONNECTOR

RIGHT FAN (GPU)

+5V_SLEEP

R623 10K 5% 1/16W MF 402 — R911 NO STUFF 10K 5% 1/16W MF 402 — R909 0 5% 1/16W MF 603

J2 CRITICAL SM-2MT

ADT7467 R879 0 5% 1/16W MF 402

+FAN2_PWR — FAN2_TACH — FAN2_PWM

FAN2_PWM

ADT7460 Q78 2N7002DW SOT-363

C135 4.7UF 20% 10V CERM 1206 PLACE CLOSE TO CONNECTOR

FAN/MODEM/SOUND/SLEEP LED/DEBUG

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SIZE	DRAWING NUMBER	REV.
D	051-6694	C
SCALE: NONE	SHT 26 OF 45	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0087	1	XTAL,CER,LW PROF,30.0000MHZ,8X4.5MM,SMD	Y5	CRITICAL	NEC_USB

Y7 LOAD CAPACITANCE IS 16PF

Low/Full/High Speed (External)

Low/Full/High Speed (Extenpall)

SERR_L AND PERR_L
HAS DEDICATED PULL-UP
FOR BOTH CBUS AND USB2

Series Rpaks required to facilitate NAND-tree testing

INTREPID USB CONSTRAINTS

USB_DAM	USB_DA	5 MIL SPACING
USB_DAP	USB_DA	5 MIL SPACING
USB_DCM	USB_DC	5 MIL SPACING
USB_DCP	USB_DC	5 MIL SPACING
USB_D1M	USB_D1	5 MIL SPACING
USB_D1P	USB_D1	5 MIL SPACING
USB_D2M	USB_D2	5 MIL SPACING
USB_D2P	USB_D2	5 MIL SPACING

NEED PULL-UP RESISTORS IN CASE USB 1.0 IS USED FOR PORT POWER

PLACE NEAR J3

SUTRO CONNECTOR

PLACE NEAR J12

BUBBA CONNECTOR

USB 2.0

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SCALE: NONE	SHT 27 OF 45	

Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0223	338S0079		U49	88EE1111 B1

+3V_MAIN

R633 10K 5% 1/16W MF 402

JTAG_ASIC_TDI 28 40

+3V_MAIN

NO STUFF R333 0 5% 1/16W MF 402

3405_MODE

R319 0 5% 1/16W MF 402

C442 10uF 20% 6.3V CERM 805

U14 LTC3405 SOT23-6

VIN, RUN, MODE, GND, CRITICAL SW, VFB

LTC3405_SW 39

CRITICAL L5 3.3uH SM1

R334 665K 1% 1/16W MF 402R2A

C471 22PF 5% 50V CERM 402

R361 49.9K 1% 1/16W MF 402 R2B

C486 10uF 20% 6.3V CERM 805

+1_0V_MARVELL

3405_VFB

R362 162K 1% 1/16W MF 402 R1

VOUT = 0.8V*(1+R2EQV/R1)

R2EQV = R2A||R2B

PLACE ALL SERIES RES CLOSE TO PHY

R370 0 5% 1/16W MF 402

R353 0 5% 1/16W MF 402

R344 0 5% 1/16W MF 402

37 13 CLKENET_LINK_TX — 37 CLKENET_PHY_TX

37 13 CLKENET_LINK_RX — 37 CLKENET_PHY_RX

37 13 CLKENET_LINK_GBE_REF — 37 CLKENET_PHY_GBE_REF

CRITICAL U49 88E1111 BCC

TX_CLK, RX_CLK, 125CLK

38 13 ENET_PHY_TXD<0> TXD0
38 13 ENET_PHY_TXD<1> TXD1
38 13 ENET_PHY_TXD<2> TXD2
38 13 ENET_PHY_TXD<3> TXD3
38 13 ENET_PHY_TXD<4> TXD4
38 13 ENET_PHY_TXD<5> TXD5
38 13 ENET_PHY_TXD<6> TXD6
38 13 ENET_PHY_TXD<7> TXD7

38 13 ENET_PHY_TX_EN TX_EN
38 13 ENET_PHY_TX_ER TX_ER
37 13 CLKENET_PHY_GTX GTX_CLK

38 13 ENET_LINK_RXD<0> RXD0
38 13 ENET_LINK_RXD<1> RXD1
38 13 ENET_LINK_RXD<2> RXD2
38 13 ENET_LINK_RXD<3> RXD3
38 13 ENET_LINK_RXD<4> RXD4
38 13 ENET_LINK_RXD<5> RXD5
38 13 ENET_LINK_RXD<6> RXD6
38 13 ENET_LINK_RXD<7> RXD7

38 13 ENET_RX_DV RX_DV
38 13 ENET_RX_ER RX_ER

38 13 ENET_CRS CRS
38 13 ENET_COL COL

38 13 ENET_MDC MDC
38 13 ENET_MDIO MDIO

14 ENET_ENERGY_DET — INT-/INT+

ENET_RST_L RESET

ENET_COMA COMA

CTRL10 NC

DVDD: C492 0.1UF, C511 0.01UF, C517 0.1UF, C502 0.01UF, C465 0.1UF, C475 0.01UF

PLACE CAPS (IN ORDER) ON PINS 1, 6, 10/15, 57/62, 67/71, 85

VDDO: C464 0.1UF, C472 0.01UF, C453 0.1UF, C503 0.01UF, C501 0.1UF, C496 10uF 20% 6.3V CERM 805

39 28 +2_5V_MARVELL

PLACE CAPS (IN ORDER) ON PINS 5, 21/26, 48/52, 66/72, 88, 96

VDDOH

VDDOX

+2_5V_MARVELL_AVDD — L34 FERR-EMI-600-OHM SM

AVDD: C497 0.1UF, C504 0.01UF, C487 0.1UF, C476 0.01UF, C754 10uF 20% 6.3V CERM 805

PLACE CAPS (IN ORDER) ON PINS 32/35, 36/40, 45 & 78

GND 97

MDI0+ MDI_P<0>
MDI0- MDI_M<0>
MDI1+ MDI_P<1>
MDI1- MDI_M<1>
MDI2+ MDI_P<2>
MDI2- MDI_M<2>
MDI3+ MDI_P<3>
MDI3- MDI_M<3>

LED_LINK10 — LED_LINK10
LED_LINK100 — LED_LINK100
LED_LINK1000 NC
LED_DUPLEX NC
LED_RX — LED_RX_SPN
LED_TX NC

CONFIG0 (000)
CONFIG1 (000)
CONFIG2 (111)
CONFIG3 (110)
CONFIG4 (111)
CONFIG5 (101)
CONFIG6 (000)

SEE CONFIG TABLES (BELOW)

TDI — JTAG_ASIC_TDI 28 40
TDO — JTAG_ENET_TDO 13
TCK — JTAG_ASIC_TCK 13 40
TMS — JTAG_ASIC_TMS 13 40
TRST — JTAG_ASIC_TRST_L 13 40

RSET — ENET_RSET

SEL_OSC NC
SEL_2.5V 13

R346 49.9 1% 1/16W MF 402 — MDI0_PD
R372 49.9 1% 1/16W MF 402 — MDI1_PD
R404 49.9 1% 1/16W MF 402 — MDI2_PD
R413 49.9 1% 1/16W MF 402 — MDI3_PD

R355 49.9 1% 1/16W MF 402
R381 49.9 1% 1/16W MF 402
R406 49.9 1% 1/16W MF 402
R428 49.9 1% 1/16W MF 402

C454 0.01UF 20% 16V CERM 402
C477 0.01UF 20% 16V CERM 402
C493 0.01UF 20% 16V CERM 402
C505 0.01UF 20% 16V CERM 402

PLACE RESISTORS CLOSE TO PHY

+2_5V_MAIN

R465 5V 5% 1/10W MF 805

PLACE CLOSE TO ETHERNET CONNECTOR

NO STUFF R438 0 5% 1/10W MF 805

CHGND1

C488 0.1UF 20% 10V CERM 402
C466 0.1UF 20% 10V CERM 402
C506 0.1UF 20% 10V CERM 402
C520 0.1UF 20% 10V CERM 402

PLACE CAPS AT TRANSFORMER PINS 1, 4, 7 & 10

CRITICAL SIT RJ45 RT-TH

40 38 RJ45_DP<0> 13
RJ45_C0_PD 15
40 38 RJ45_DN<0> 14
40 38 RJ45_DP<1> 16
RJ45_C1_PD 18
40 38 RJ45_DN<1> 17
40 38 RJ45_DP<2> 19
RJ45_C2_PD 21
40 38 RJ45_DN<2> 20
40 38 RJ45_DP<3> 22
RJ45_C3_PD 24
40 38 RJ45_DN<3> 23

SM XFR-ENET-1000BT T1 CRITICAL

Short shielded RJ-45

CHGND1

R735 75 5% 1/16W MF 402
R733 75 5% 1/16W MF 402
R382 75 5% 1/16W MF 402
R347 75 5% 1/16W MF 402

ENET_CTAP_CHGND 39

C457 100pF 10% 3KV CERM 1808

CHGND1

39 28 +2_5V_MARVELL

R371 10K 5% 1/16W MF 402
R345 10K 5% 1/16W MF 402
R354 1.5K 1% 1/16W MF 402

R343 1K 5% 1/16W MF 402

14 INT_ENET_RST_L

D1 1N914 SOT23

31 27 24 23 17 IO_RESET_L

Q15 2N7002DW SOT-363

32 31 30 AC_IN

Q15 2N7002DW SOT-363

36 35 34 19 SLEEP_L_LS5

C755 2.2uF 10% 10V CERM 805

PLACES PHY IN "COMA" MODE WHEN ASLEEP ON BATTERY (SAVES POWER)

ENET_HSDACP HSDAC+
ENET_HSDACM HSDAC-

37 CLK25M_ENET_XIN XTAL1
37 CLK25M_ENET_XOUT XTAL2

ENET_VSSC VSSC

NO STUFF R435 20K 5% 1/16W MF 402

PUT CRYSTAL CIRCUIT CLOSE TO PHY

OMIT CRITICAL Y3 25.0000M 8X4.5MM-SM

CLK25M_XTAL_IN

C555 33PF 5% 50V CERM 402

C491 33PF 5% 50V CERM 402

Y3'S LOAD CAPACITANCE IS 20PF

R427 0 5% 1/16W MF 402

NO STUFF R393 49.9 1% 1/16W MF 402

NO STUFF R403 49.9 1% 1/16W MF 402

R335 10K 5% 1/16W MF 402

R380 4.99K 1% 1/16W MF 402

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0086	1	XTAL,CER,25MHZ,.005%,20PF,8X4.5MM,SMD	Y3	CRITICAL	?

CONFIG DEFINITIONS

PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS

PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

MARVELL 88E1111
10/100/1000 ETHERNET

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D	051-6694	C
SCALE: NONE	SHT 28 OF 45	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0011	197S0052	?	G1	SIWARD ALT FOR FW OSC

DSX STRAP OPTIONS

0 -> BILINGUAL PORT

1 -> A-ONLY PORT

PLACE NEAR PHY

PLACE NEAR PHY

CAPACITOR IN CONJUCTION WITH INTERNAL PULLUP PROVIDES RESET PULSE WHEN PHY FIRST RECEIVES POWER

SPEC SAID TO USE 10K

1MA(MAX) BUS HOLDER EACH

PWR CLASS = 100

(MAY PROVIDE POWER, OR MAY REQUIRE UP TO 3W)

(PC0 IS MSB, PC2 IS LSB)

VOUT = 1.22*(1+R2/R1)+ IADJ*R2

IADJ = 30NA AT 25C

165MA MAX LOAD

FIREWIRE

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APPLE COMPUTER INC.

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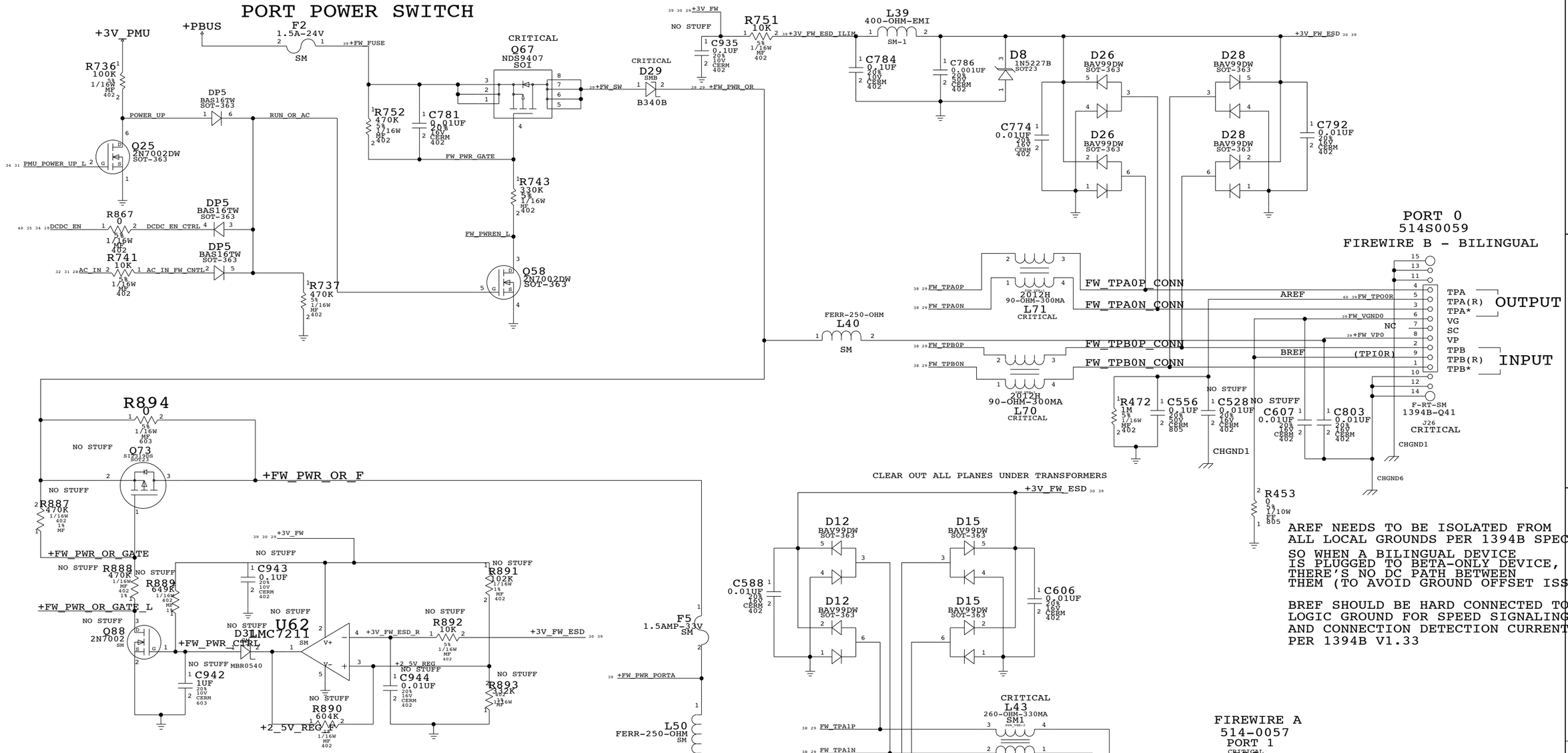
SCALE: NONE	SHT 29 OF 45	

PORT POWER SWITCH



ENABLES PORT POWER WHEN MACHINE IS RUNNING, SHUTDOEN OR WHEN ASLEEP ON AC

STATE	PMU_POWER_UP_L	POWER_UP	DCDC_EN	AC_IN	STUFF R867	NO STUFF R867
SHUTDOWN (AC)	1	0	0	1	OFF	ON
SLEEP (AC)	1	0	1	1	ON	ON
RUN (AC)	0	1	1	1	ON	ON
SHUTDOWN (BATT)	1	0	0	0	OFF	OFF
SLEEP (BATT)	1	0	1	0	OFF (PULL-DOWN RESISTOR)	OFF (PULL-DOWN RESISTOR)
RUN (BATT)	0	1	1	0	ON	ON
	2.99V	+3V_PMU	+4_6V_BU	+3V_PMU		

FIREWIRE PORTS

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SIZE	DRAWING NUMBER	REV.
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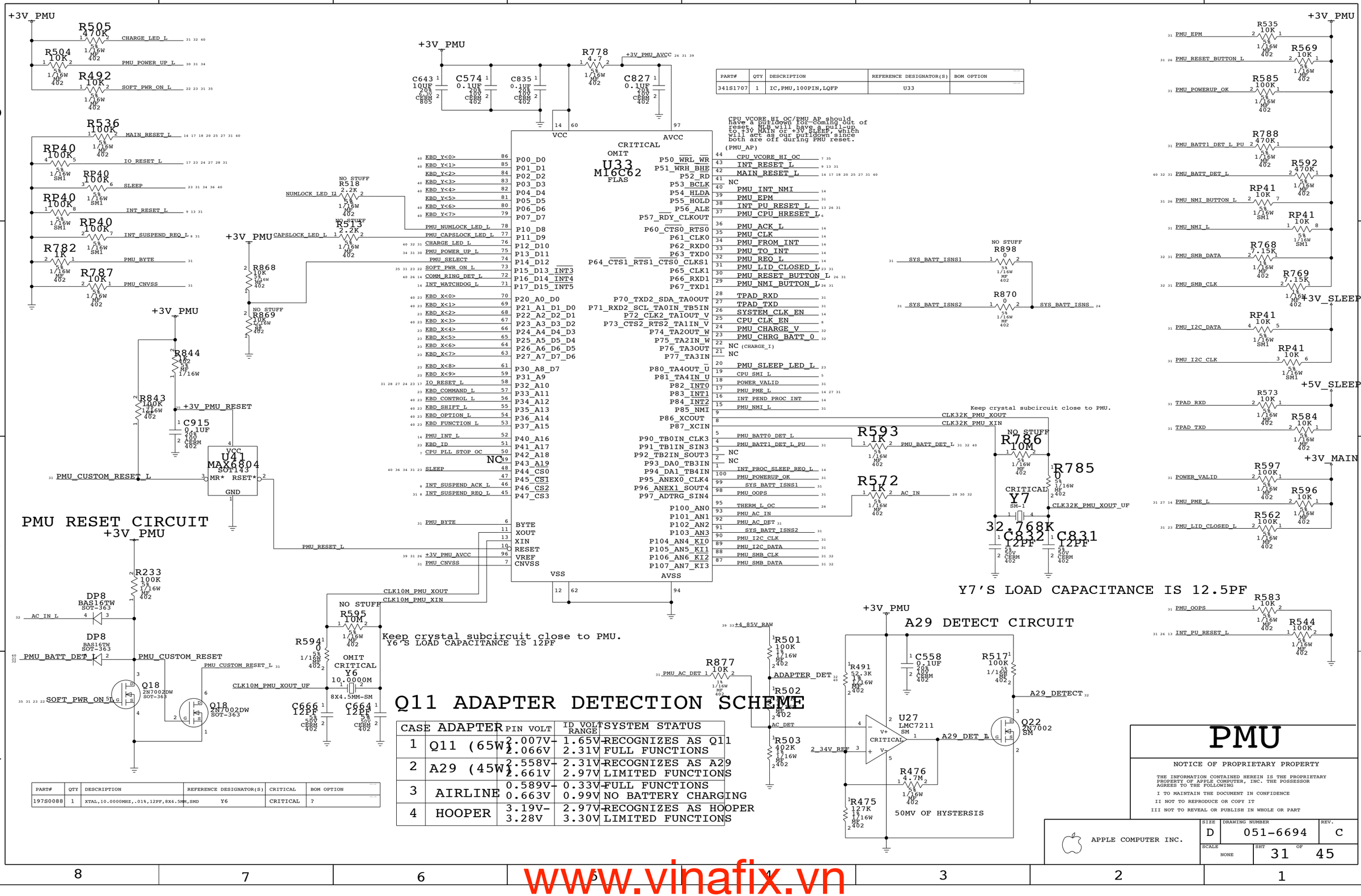

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1707	1	IC,PMU,100PIN,LQFP	U33	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0088	1	XTAL,10.0000MHZ,.01%,12PF,8X4.5MM,SMD	Y6	CRITICAL	?

DC POWER INPUT

(POWER JACK, ETC. ON SEPARATE BOARD)
CRITICAL

J18
87438-0833
M-RT-SM

CHARGE_LED_L
+ADAPTER
ADAPTER_DET

NO STUFF
C757 0.1UF 20% 50V CERM 805
PLACE CLOSE TO DC INPUT

R396 20K 1% 1/16W MF 402
R395 102K 1% 1/16W MF 402
R364 102K 1% 1/16W MF 402
R375 10K 1% 1/16W MF 402
R365 57.6K 1% 1/16W MF 402
R394 1M 5% 1/16W MF 402

+3V_PMU
C468 0.01UF 20% 16V CERM 402
R363 10K 5% 1/16W MF 402
U15 LMC7211 SM CRITICAL
1V20_REF
AC_DIV
AC_IN
AC_IN_L
Q10 2N7002DW SOT-363

R383 470K 5% 1/16W MF 402
GREATER THAN 13.5V DETECT

DC INRUSH LIMITER

Q13 SI4435DY SOI
Q16 SI4435DY SOI
+ADAPTER_SW
+ADAPTER_SENSE
GATE
R414 330K 1% 1/16W MF 402
C458 0.1UF 20% 25V CERM 805
AC_ENABLE_GATE
R374 470K 5% 1/16W MF 402
AC_ENABLE_L
BCKFD_PROT_GATE
C592 0.01UF 20% 25V CERM 402
R499 68K 5% 1/16W MF 402
BCKFD_PROT_EN_L
Q21 2N7002DW SOT-363

R754 100K 1% 1/16W MF 402
D9 1N914 SOT23
R755 7.87K 1% 1/16W MF 402
C600 1UF 20% 50V CERM 1210

PLACE U23 NEXT TO R460

U23 SENSE VOLTAGE DROP ACROSS R460

C572 0.010UF 20% 50V CERM 603
U23 MAX4172 TSSOP
RS+ RS- PG NC1 NC2 OUT GND
CRITICAL
MAX4172_OUT
+24V_PBUS
R454 2.21K 1% 1/16W MF 603
C883 0.1UF 10% 50V X7R 603-1
R460 0.025 1% 1W MF 2512
IF A29 ADAPTER USED, ADJUST CURRENT SETTING
R488 4.7 5% 1/16W MF 402
R498 4.7 5% 1/16W MF 402
1772_CSSP
1772_CSSN

1MSEC INTEGRATION TIME

R742 1K 1% 1/16W MF 402
C771 0.1UF 20% 10V CERM 402
IAC_RC_COMP
+3V_PMU
C772 0.1UF 20% 10V CERM 402
R747 42.2K 1% 1/16W MF 603
U50 LMC7111 SOT23-5 CRITICAL
IAC_FB
R466 10K 1% 1/16W MF 402
CURRENT_THRESHOLD
R738 42.2K 1% 1/16W MF 603
R734 82.5K 1% 1/16W MF 603
A29_CURRENT_ADJ
Q20 2N7002DW SOT-363
A29_DETECT_G
+3V_PMU
R739 51.1K 1% 1/16W MF 603
IF ADAPTER IS OVER 18V, ADJUST CURRENT SETTING
OVER_18V_ADJ
R748 100K 5% 1/16W MF 402
Q20 2N7002DW SOT-363
C775 1UF 20% 16V CERM 603
AC_GTR_18V
Q65 2N7002DW SOT-363
1772_ACOK_L

BATTERY SWITCH-OVER CIRCUIT

+BATT
F4 5AMP-125V SM-2
F3 5AMP-125V SM-2
+24V_PBUS
+PBUS
PLACE R358 CLOSE TO LTC1625
ROUTE LTC1625_ITH CAREFULLY
+BATT_24V_FUSE
CRITICAL
Q24 SI4435DY SOI
+BATT_14V_FUSE
Q76 SUD45P03 TO-252
LTC1625_ITH
DP4 BAS16TW SOT-363
R358 150 1% 1/16W MF 402
1625_COMP
ADAPTER_I_REG
R490 47K 5% 1/16W MF 402
R746 47K 5% 1/16W MF 402
BATT_14V_GATE
BATT_24V_GATE
R512 10K 5% 1/16W MF 402
R744 10K 5% 1/16W MF 402
DP4 BAS16TW SOT-363
BATT_24PBUS_EN
BATT_14PBUS_EN
AC_IN_L
R489 158K 1% 1/16W MF 402
Q21 2N7002DW SOT-363
AC_IN_L_RC
C593 10UF 20% 6.3V CERM 805
WHEN AC IS IN, P-CHANNEL FETS ARE QUICKLY (DIODE) TURNED OFF
WHEN AC IS NOT PLUGGED, P-CHANNEL FETS ARE ON
RC TIME IS 480K*10UF @ +3V_PMU

SWITCHER VOLTAGE CONTROL

PMU SELECTS BETWEEN TWO VOLTAGES

SWITCHER CURRENT CONTROL

CHARGE DISABLED BY PMU OR INPUT VOLTAGE
CHARGE THROTTLED BY LOW BATTERY VOLTAGE

+3V_PMU
R567 27.4K 1% 1/16W MF 402
R558 10K 1% 1/16W MF 402
R548 10K 1% 1/16W MF 402
R560 4.12K 1% 1/16W MF 402
R565 48.7K 1% 1/16W MF 402
R566 1K 1% 1/16W MF 402
R542 1K 1% 1/16W MF 402
BATTV_HIGH
BATT_LOW_L
R561 100K 5% 1/16W MF 402
Q27 2N7002DW SOT-363
R580 5.23K 1% 1/16W MF 402
BATTV_LOW
Q29 2N7002DW SOT-363
Q29 2N7002DW SOT-363
PMU_CHARGE_V
Q27 2N7002DW SOT-363

OD OUTPUT LOW - WHEN AC GREATER THAN 13.7V

U31 MAX1772 QSOP CRITICAL
CSSP DCIN ACIN ACOK RFIN VCTL ICTL ICHG IINP CCV CCI CCS REF CSSN CELLS LDO DLOV BST DHI LX DLO PGND CSIP CSIN BATT GND
REF = 4.096V
REF_CLS
1772_DCIN
1772_ACIN
1772_ACOK_L
(+3V_PMU)
1772_VCTL
1772_ICTL
1772_ICHG
1772_IINP
1772_CCV
1772_CCI
1772_CCS
1772_CELLS
1772_DLOV
1772_BST
1772_DHI
1772_LX
1772_DLO
(GND)
1772_CSIP
1772_CSIN

R526 1K 1% 1/16W MF 402
C622 0.01UF 20% 16V CERM 402
C616 0.01UF 20% 16V CERM 402
R497 1K 1% 1/16W MF 402
C621 0.1UF 20% 10V CERM 402
1772_CCV_RC
1772_REF
C630 1UF 20% 10V CERM 603
R487 10K 1% 1/16W MF 402
R473 4.12K 1% 1/16W MF 402
1772_CLS
1772_GND
C652 1UF 20% 10V CERM 603
C817 0.1UF 20% 25V CERM 603
C802 0.1UF 20% 25V CERM 603
R559 100K 1% 1/16W MF 402
NO STUFF
C906 0.0022UF 10% 50V CERM 402
XW19 SM

+3V_PMU
C615 0.1UF 20% 10V CERM 402
R588 100K 1% 1/16W MF 402
R579 499K 1% 1/16W MF 402
U38 LMC7211 SM CRITICAL
BATT_LOW
BATT_DIV
1V65_REF
R599 100K 1% 1/16W MF 402
R570 100K 1% 1/16W MF 402
C658 0.047UF 10% 16V CERM 402

R749 6.34K 1% 1/16W MF 402
A29_CLS_ADJ
A29_DETECT
Q65 2N7002DW SOT-363

+BATT_VSNS
BATTERY CONNECTOR CRITICAL
J25 87438-0833 M-RT-SM
+BATT_POS
(BATT_IN_PD)
BATT_CLK
BATT_DATA
PMU_BATT_DET_L
BATT_NEG

+BATT_ISNS
L9 FERR-EMI-100-OHM SM
L53 FERR-50-OHM SM
L10 FERR-EMI-100-OHM SM
PMU_SMB_CLK
L8 FERR-EMI-100-OHM SM
PMU_SMB_DATA
L12 FERR-50-OHM SM

D10 1N914 SOT23
1772_BST_ESR
R571 33 1% 1/8W MF 1206
R549 100K 5% 1/16W MF 402
C624 0.1UF 20% 25V CERM 402
R774 4.7 5% 1/16W MF 603
C608 0.1UF 20% 50V CERM 805
+24V_PBUS
Q63 IRF7805 SM CRITICAL
Q64 IRF7811W SO-8 CRITICAL
C547 2.2UF 10% 50V CERM 1812
C562 2.2UF 10% 50V CERM 1812
C563 2.2UF 10% 50V CERM 1812
C557 2.2UF 10% 50V CERM 1812
C564 2.2UF 10% 50V CERM 1812
L42 10UH SM CRITICAL
D30 MBRS140T3 SM CRITICAL
+BATT_RSNS
R763 0.05 1% 1W MF 2512
+BATT_24V_FUSE
R543 1 5% 1/16W MF 603
R511 1 5% 1/16W MF 603
C619 4.7UF 20% 25V CERM 1206
C632 4.7UF 20% 25V CERM 1206
C617 4.7UF 20% 25V CERM 1206
C824 33UF 20% 25V ELEC SM
C631 4.7UF 20% 25V CERM 1206
C633 4.7UF 20% 25V CERM 1206
C618 4.7UF 20% 25V CERM 1206

$V_{BATT} = CELLS \times (4.096 + (0.4096 \times V_{VCTL} / V_{REFIN}))$

For 4.15V cells, VCTL = 0.123 REFIN
For 4.20V cells, VCTL = 0.245 REFIN

$I_{CHG} = (0.2048/R_{62}) * ICTL (V_{REFIN} / V)$

BATTERY CHARGER

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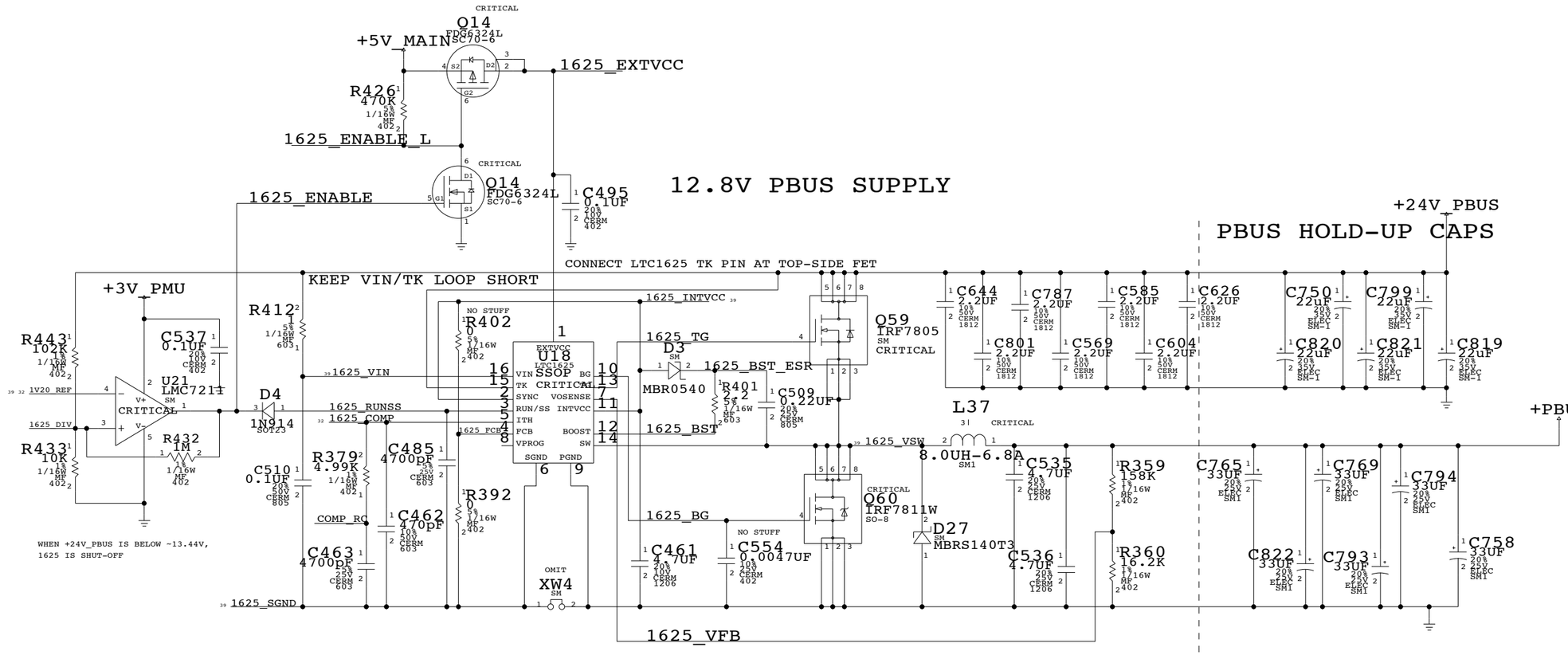
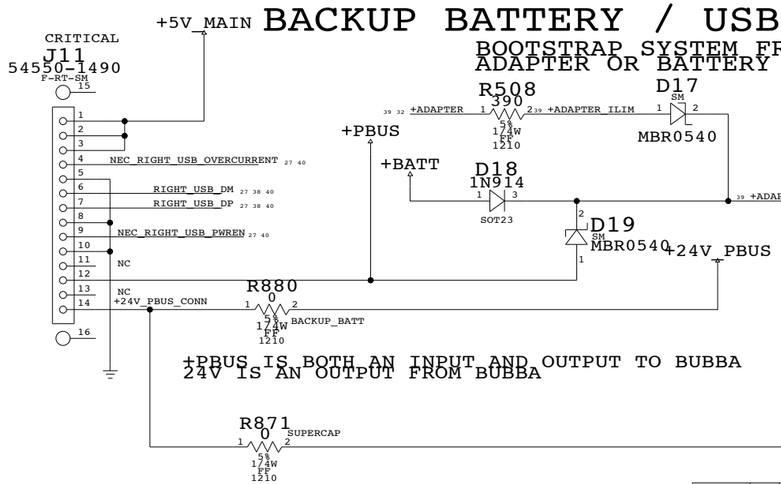
12.8V PBUS SUPPLY

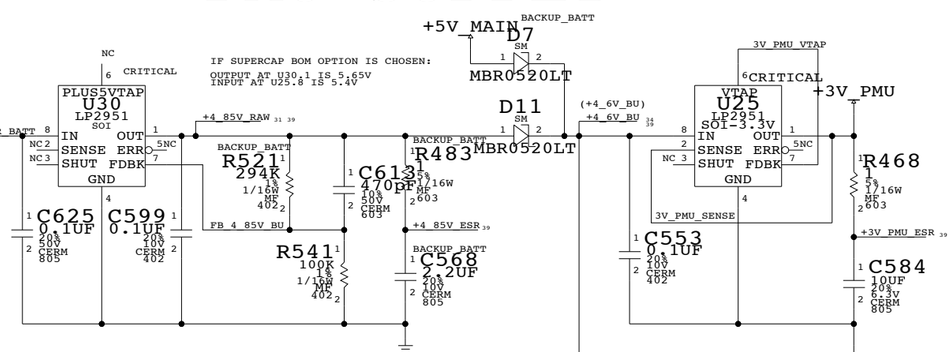


BACKUP BATTERY / USB CONNECTOR



BOOTSTRAP SYSTEM FROM ADAPTER OR BATTERY

PMU SUPPLY



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S3575	1	RES,MF,1/16W/357K OHM,1%,0402,SMD	R521	?	SUPERCAP

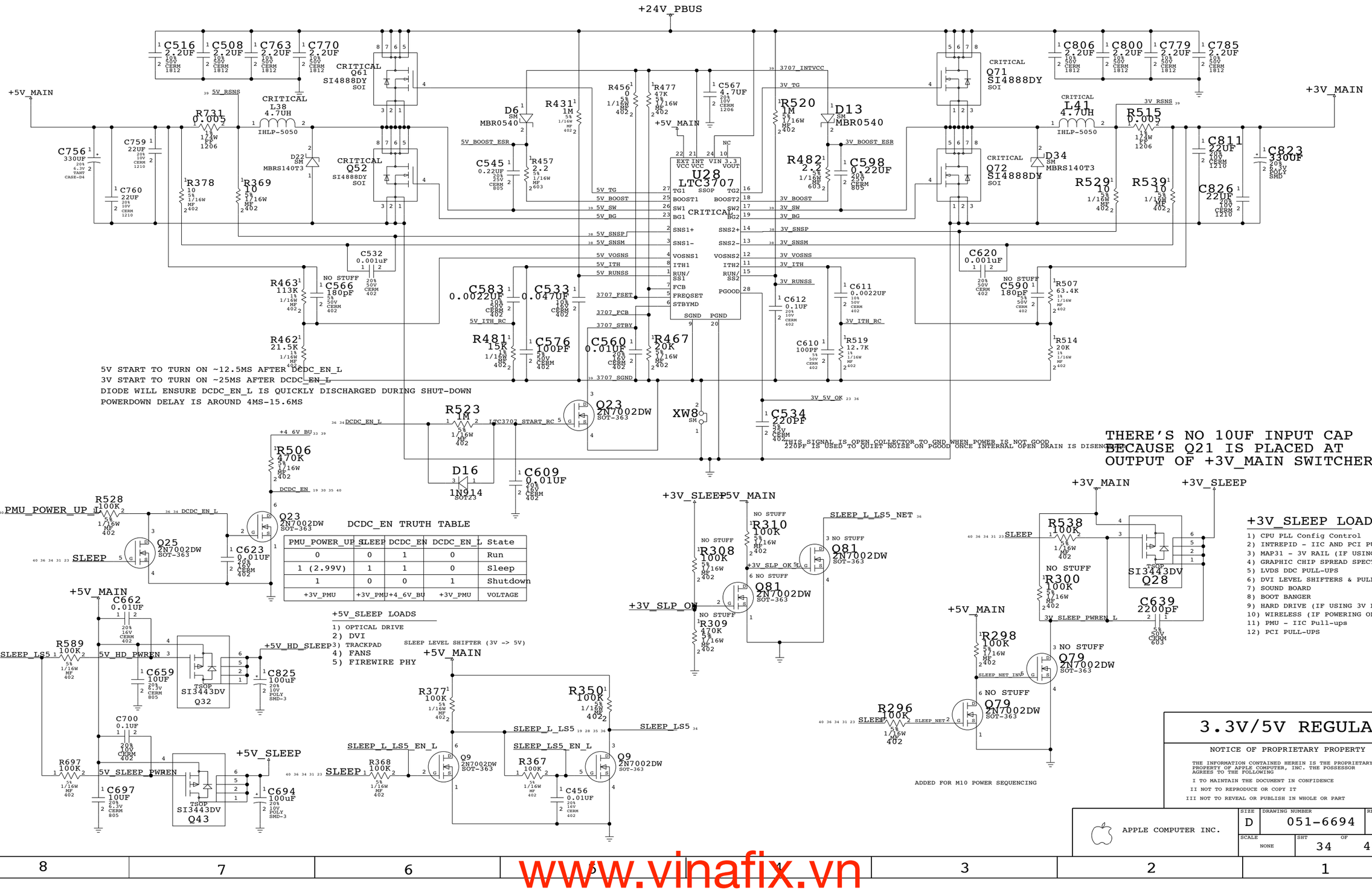
12.8V REGULATOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	C

SCALE	SHT	OF
NONE	33	45

3.3V/5V MAIN SUPPLY



3.3V/5V REGULATOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	C
SCALE: NONE	SHT 34 OF 45	

VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage
(approx. 7ms delay)

+5V_MAIN

R408 100K 5% 1/16W MF 402
R398 100K 5% 1/16W MF 402
R356 100K 1% 1/16W MF 402
DP2 BAS16TW SOT-363
MAXBUS_SLEEP
CPU_VCORE_PWR_SEQ
R267 10K 5% 1/16W MF 402
CPU_VCORE_SEQ_L
Q12 2N3904 SM
CPU_VCORE_SEQ
Q17 2N3904 SM
DP2 BAS16TW SOT-363
SLEEP_L
DP2 BAS16TW SOT-363
DCDC_EN

NO STUFF R384 0 5% 1/16W MF 402
CPU_VCORE_HI_OC
R366 0 5% 1/16W MF 402
INT_GPIO1_PU
NO STUFF R337 470K 5% 1/16W MF 402 <D0>
R336 0 1% 1/16W MF 402
C529 0.01UF 20% 16V CERM 402
R448 66.5K 1% 1/16W MF 402
R385 12.7K 1% 1/16W MF 402
C459 1UF 20% 10V CERM 603
C512 220PF 5% 25V CERM 402

VCORE_VID<0>
VCORE_VID<1>
VCORE_VID<2>
VCORE_VID<3>
VCORE_VID<4>

MAX1717 VID CAN TAKE 3.3V TO 5.5V INPUTS

1.67GHZ (WITHOUT VCORE OFFSET) 1.300V -> 0.975V

NO STUFF R297 470K 5% 1/16W MF 402 <D4>
NO STUFF R314 470K 5% 1/16W MF 402 <D3>
NO STUFF R328 0 5% 1/16W MF 402 <D2>
NO STUFF R324 0 5% 1/16W MF 402 <D1>
NO STUFF R876 470K 5% 1/16W MF 402 <D4>
R304 470K 5% 1/16W MF 402 <D3>
R329 470K 5% 1/16W MF 402 <D2>
R325 0 5% 1/16W MF 402 <D1>
NO STUFF R322 10K 5% 1/16W MF 402
NO STUFF R303 0 5% 1/16W MF 402 <D4>
NO STUFF R313 470K 5% 1/16W MF 402 <D3>
NO STUFF R327 470K 5% 1/16W MF 402 <D2>
NO STUFF R323 470K 5% 1/16W MF 402 <D1>
R301 470K 5% 1/16W MF 402 <D4>
R305 0 5% 1/16W MF 402 <D3>
NO STUFF R330 470K 5% 1/16W MF 402 <D2>
NO STUFF R326 0 5% 1/16W MF 402 <D1>
NO STUFF R302 1K 5% 1/16W MF 402

VCORE_SLOW<1>
VCORE_SLOW<2>
VCORE_SLOW<3>
VCORE_SLOW<4>
VCORE_FAST<1>
VCORE_FAST<2>
VCORE_FAST<3>
VCORE_FAST<4>
VCORE_MUX_SEL
VCORE_MUX_EN

NO STUFF R318 0 5% 1/16W MF 402
CPU_VCORE_HI_OC

U11 VCC NO STUFF PT3B3257 QSOP (EEM_VER=2) CRITICAL
A1 B1 A2 B2 A3 B3 A4 B4 SEL OE GND Y1 Y2 Y3 Y4

NO STUFF C439 0.1UF 20% 10V CERM 402

NO_4XVCORE R288 0 5% 1/16W MF 402
NO_4XVCORE R289 0 5% 1/16W MF 402
NO_4XVCORE R290 0 5% 1/16W MF 402
NO_4XVCORE R292 0 5% 1/16W MF 402

VCORE_VID<1>
VCORE_VID<2>
VCORE_VID<3>
VCORE_VID<4>

SEL = 0; Y1=A1
SEL = 1; Y1=B1

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S0242	1	IND,PWR,1.0UH,20,20.5A,SMD	L36	CRITICAL	

CPU_VCORE_SLEEP

C2 10UF 20% 6.3V CERM 805
C689 10UF 20% 6.3V CERM 805
C5 10UF 20% 6.3V CERM 805
C699 10UF 20% 6.3V CERM 805
C234 10UF 20% 6.3V CERM 805
C682 10UF 20% 6.3V CERM 805
C674 10UF 20% 6.3V CERM 805
C274 10UF 20% 6.3V CERM 805
C7 10UF 20% 6.3V CERM 805
C680 10UF 20% 6.3V CERM 805
C693 10UF 20% 6.3V CERM 805
C13 10UF 20% 6.3V CERM 805
C116 10UF 20% 6.3V CERM 805
C6 10UF 20% 6.3V CERM 805
C695 10UF 20% 6.3V CERM 805
C679 10UF 20% 6.3V CERM 805
C285 10UF 20% 6.3V CERM 805
C4 10UF 20% 6.3V CERM 805
C3 10UF 20% 6.3V CERM 805
C687 10UF 20% 6.3V CERM 805

Keep trace fat (40-100 mils) and short!!

+PBUS

CRITICAL C427 8.2UF 20% 16V TANT CASE-D
CRITICAL C431 8.2UF 20% 16V TANT CASE-D
CRITICAL C443 8.2UF 20% 16V TANT CASE-D
CRITICAL C430 8.2UF 20% 16V TANT CASE-D
CRITICAL C432 8.2UF 20% 16V TANT CASE-D
CRITICAL C441 8.2UF 20% 16V TANT CASE-D
CRITICAL C444 8.2UF 20% 16V TANT CASE-D
CRITICAL C445 8.2UF 20% 16V TANT CASE-D

+5V_MAIN

R349 20 5% 1/16W MF 402
PLACE C423 CLOSE TO PINS 15 & 1311
C498 1UF 20% 10V CERM 603
D2 SM MBR0530
VCORE_BOOST
VCORE_VCC

R407 0 5% 1/16W MF 402
C507 1UF 20% 10V CERM 603
R397 27.4K 1% 1/16W MF 402

U20 MAX1717 QSOP
VCC VDD SKP/SDN FBS ILIM GNDS A/B REF TON CC D0 D1 D2 D3 D4 V+ BST DH LX DL GND FB TIME VGATE CRITICAL

VCORE_SHDN_L
(VCORE_SNS)
VCORE_ILIM
(VCORE_GNDSNS)
MAX1717_AB_SEL
VCORE_REF
VCORE_TON
VCORE_CC
VCORE_VPLUS
VCORE_BST
VCORE_DH
VCORE_LX
VCORE_DL
VCORE_GND
VCORE_FB
VCORE_TIME
VCORE_VGATE

NO STUFF C455 0.0047uF 10% 25V CERM 402
R429 2.2 5% 1/16W MF 603
C518 0.1UF 20% 25V CERM 603
C768 0.0047uF 10% 25V CERM 402
R415 100 5% 1/16W MF 402
R434 390K 5% 1/16W MF 402
C521 0.001UF 20% 50V CERM 402
XW5 SM
XW7 SM

CRITICAL Q50 SI7860DP SO-8-PWRPK
CRITICAL Q49 SI7860DP SO-8-PWRPK
CRITICAL Q54 IRF7832 SO-8
CRITICAL Q55 IRF7832 SO-8
CRITICAL Q53 IRF7832 SO-8

Keep trace fat and short!!

OMIT CRITICAL L36 1.2UH-18.3A SM1
CRITICAL R331 0.001 1% 1W MF 2512
CRITICAL D25 B540C SM
R732 2.2 5% 1/4W MF 1210
NO STUFF C764 0.0022UF 10% 50V CERM 603
CPU_VCORE_SNUB

CRITICAL C728 220UF 20% 2V TANT 7343
CRITICAL C734 220UF 20% 2V TANT 7343
CRITICAL C733 220UF 20% 2V TANT 7343
CRITICAL C732 220UF 20% 2V TANT 7343
CRITICAL C885 220UF 20% 2V TANT 7343
CRITICAL C731 220UF 20% 2V TANT 7343
CRITICAL C730 220UF 20% 2V TANT 7343
CRITICAL C729 220UF 20% 2V TANT 7343
CRITICAL C884 220UF 20% 2V TANT 7343

CPU_VCORE_SLEEP_F
XW15 SM
Keep trace fat and short!!
CPU_VCORE_SLEEP

Connect MAX1717 GND pin 13 to GND at bottom-side FET

Keep trace fat and short!!

VCORE_GNDSNS
PLACE THIS SHORT AT PIN OF 1000uF CAP CLOSEST TO CPU
XW3 SM
VCORE_SNS

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V WITH A 0.85 SCALE FACTOR, HENCE VOFFSET = 1.7V * (R1/(R1+R2)) AND VCORE = VDAC + VOFFSET.

NOTE: R310 (R2) NO STUFFED FOR NO OFFSET CASE

ROUTE AS DIFFERENTIAL PAIR

+5V_MAIN
VCORE_OFFSET_SW
R805 100K 1% 1/16W MF 402
VCORE_SEL_OFF_ON
R809 6.04K 1% 1/16W MF 402
VCORE_OFFSET
R376 162K 1% 1/16W MF 603 R2
VCORE_GNDDIV
R321 2K 1% 1/16W MF 402 R1
NO STUFF R806 0 5% 1/16W MF 402
VCORE_SEL_ON
Q86 2N7002DW SOT-363
MAX1717_AB_SEL_OFFSET_SW
R807 0 5% 1/16W MF 402
AB_SEL_LOW
Q86 2N7002DW SOT-363
NO STUFF R808 100K 5% 1/16W MF 402

1.67GHZ (WITH VCORE OFFSET) 1.320V -> 0.990V
(CPU SPEC: 1.280V -> 0.980V)

OUTPUT VOLTAGE

V_{DAC} D4=0	V_{DAC} D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	A/B_ = Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1

If all pull-ups are >=100K and all pull-downs are <=1K, VB = V .

FMAX CONNECTOR

NO STUFF R315 2.05K 1% 1/16W MF 402
VCORE_GNDDIV
NO STUFF R312 100 1% 1/16W MF 402
VCORE_GNDSNS
VCORE_GNDDIV_TEST
VCORE_GNDSNS_TEST
+3V_PMU_RESET
SOFT_PWR_ON_L
NC (RFU)

CRITICAL NO STUFF J5 M-ST-SM-52465-1217
VCORE_VID<0>
VCORE_VID<1>
VCORE_VID<2>
VCORE_VID<3>
VCORE_VID<4>

VCORE SUPPLY

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1.5V/2.5V SWITCHER

+1_5V_SLEEP LOADS
1) AGP I/O - IF USING D3COLD
2) MAXBUS I/O - IF 1.5V INTERFACE

+1_5V_MAIN LOADS
1) INTREPID CORE
2) AGP I/O IF USING D3HOT

+2_5V_MAIN LOADS
1) MAP31 - FBCORE/FBIO IF USING D3HOT
2) GIGABIT ETHERNET - AVDDL
3) DDR SODIMMS - CORE/IO
4) DDR MUXES
5) CLOCK SLEWING I/O
6) PCI1510 CORE

+2_5V_SLEEP LOADS
1) FBCORE/FBIO IF USING D3COLD
2) INTREPID MEMORY I/O

THERE'S 100K PULL-UP ON PG 31 ALREADY

DIODE PROVIDE PROVIDE QUICK SHUT DOWN
POWER DOWN DELAY 1.5MS TO 3.3MS

CHANGE R424 BACK TO 10K, 1%, AND STUFF 5.11K FOR 1.5V OPERATION
CONNECTING 1_5V_FB TO GND, FORCES 1.8V OUTPUT

1.8V SWITCHER

+1_8V_MAIN LOADS
1) INTREPID PLLS

+1_8V_SLEEP LOADS
1) MPC7450 - MAXBUS I/O - IF 1.8V INTERFACE
2) CPU JTAG & MaxBus Pull-ups
3) CPU PLL Config Straps
4) OPTIONAL VIDEO MEMORY (M10 PRO ONLY)

1.5V/1.8V/2.5V SUPPLIES

APPLE COMPUTER INC.

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DIGITAL SIGNALS

GROUP	SIG_NAME		MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
MAXBUS	CPU_AACK_L				250.0000	10 MIL SPACING			5 8
	CPU_ADDR<0..31>		5		250			83 MHZ	5 8
	CPU_ARTRY_L				250.0000	10 MIL SPACING			5 8
	CPU_BG_L				250.0000	10 MIL SPACING			5 8
	CPU_BR_L				250.0000	10 MIL SPACING			5 8
	CPU_CI_L		5		250.0000				5 8
	CPU_DATA<0..31>		5		250			83 MHZ	6 8
	CPU_DATA<32..63>		5		250			83 MHZ	6 8
	CPU_DBG_L		5		250.0000	10 MIL SPACING			5 8
	CPU_DTI<0..2>		5		250				5 8
	CPU_DRDY_L_UF					10 MIL SPACING			
	CPU_DRDY_L				250.0000	10 MIL SPACING			5 8
	CPU_GBL_L		5		250.0000				5 8
	CPU_HIT_L				250.0000	10 MIL SPACING			5 8
	CPU_QACK_L		5		250.0000	10 MIL SPACING			5 8
	CPU_QREQ_L				250.0000	10 MIL SPACING			5 8
	CPU_TA_L				250.0000	10 MIL SPACING			5 8
	CPU_TBST_L		5		250.0000	10 MIL SPACING			5 8
	CPU_TEA_L				250.0000				5 8
	CPU_TS_L				250.0000	10 MIL SPACING			5 8
	CPU_TSIZ<0..2>		5		250				5 8
	CPU_TT<0..4>		5		250				5 8
	CPU_WT_L		5		250.0000				5 8
GROUP 0	MEM_DATA<7..0>		4		200			167 MHZ	9 10
	RAM_DATA_A<7..0>		4		200			167 MHZ	10 11
	RAM_DATA_B<7..0>		4		200			167 MHZ	10 11
	MEM_DQS<0>	TOTAL LENGTH CONTROLLED BY SPREADSHEET			200				9 10
	RAM_DQS_A<0>		4		200				10 11
	RAM_DQS_B<0>		4		200				10 11
	MEM_DQM<0>		4		200				9 10
	RAM_DQM_A<0>		4		200				10 11
	RAM_DQM_B<0>		4		200				10 11
GROUP 1	MEM_DATA<15..8>		4		200			167 MHZ	9 10
	RAM_DATA_A<15..8>		4		200			167 MHZ	10 11
	RAM_DATA_B<15..8>		4		200			167 MHZ	10 11
	MEM_DQS<1>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200				9 10
	RAM_DQS_A<1>		4		200				10 11
	RAM_DQS_B<1>		4		200				10 11
	MEM_DQM<1>				200				9 10
	RAM_DQM_A<1>		4		200				10 11
	RAM_DQM_B<1>		4		200				10 11
GROUP 2/3	MEM_DATA<31..16>		4		200			167 MHZ	9 10
	RAM_DATA_A<31..16>		4		200			167 MHZ	10 11
	RAM_DATA_B<31..16>		4		200			167 MHZ	10 11
	MEM_DQS<3..2>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200			167 MHZ	9 10
DDR RAM	RAM_DQS_A<3..2>		4		200			167 MHZ	10 11
	RAM_DQS_B<3..2>		4		200			167 MHZ	10 11
	MEM_DQM<3..2>		4		200			167 MHZ	9 10
	RAM_DQM_A<3..2>		4		200			167 MHZ	10 11
	RAM_DQM_B<3..2>		4		200			167 MHZ	10 11
GROUP 4/5	MEM_DATA<47..32>		4		200			167 MHZ	9 10
	RAM_DATA_A<47..32>		4		200			167 MHZ	10 11
	RAM_DATA_B<47..32>		4		200			167 MHZ	10 11
	MEM_DQS<5..4>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200			167 MHZ	9 10
	RAM_DQS_A<5..4>		4		200			167 MHZ	10 11
	RAM_DQS_B<5..4>		4		200			167 MHZ	10 11
	MEM_DQM<5..4>		4		200			167 MHZ	9 10
	RAM_DQM_A<5..4>		4		200			167 MHZ	10 11
	RAM_DQM_B<5..4>		4		200			167 MHZ	10 11
GROUP 6	MEM_DATA<55..48>		4		200			167 MHZ	9 10
	RAM_DATA_A<55..48>		4		200			167 MHZ	10 11
	RAM_DATA_B<55..48>		4		200			167 MHZ	10 11
	MEM_DQS<6>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200				9 10
	RAM_DQS_A<6>				200				10 11
	RAM_DQS_B<6>		4		200				10 11
	MEM_DQM<6>				200				9 10
	RAM_DQM_A<6>		4		200				10 11
	RAM_DQM_B<6>		4		200				10 11
GROUP 7	MEM_DATA<63..56>		4		200			167 MHZ	9 10
	RAM_DATA_A<63..56>		4		200			167 MHZ	10 11
	RAM_DATA_B<63..56>		4		200			167 MHZ	10 11
	MEM_DQS<7>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200				9 10
	RAM_DQS_A<7>				200				10 11
	RAM_DQS_B<7>				200				10 11
	MEM_DQM<7>		4		200				9 10
	RAM_DQM_A<7>		4		200				10 11
	RAM_DQM_B<7>		4		200				10 11
ADDR	MEM_ADDR<12..0>		4					83 MHZ	9
	RAM_ADDR<12..0>		6		200				9 11
	MEM_BA<1..0>		4						9
	RAM_BA<1..0>		6		200				9 11
CONTROL	MEM_CS_L<3..0>		4						9
	RAM_CS_L<3..0>		6		200				9 11
	MEM_CKE<3..0>		4						9
	RAM_CKE<3..0>		6		200				9 11
	MEM_RAS_L		4						9
	RAM_RAS_L				200.0000				9 11
	MEM_CAS_L		4						9
	RAM_CAS_L				200.0000				9 11
	MEM_WE_L		4						9
	RAM_WE_L				200.0000				9 11
	MEM_MUXSEL_H<1..0>		3						9 10
	MEM_MUXSEL_L<1..0>		3						9 10
	RAM_MUXSEL_H		5						10
	RAM_MUXSEL_L		5						10

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME		MAX VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM	
INTREPID CLOCKS	SYSCLK_CPU_UF					10 MIL SPACING		8
	SYSCLK_CPU		4		200.0000	10 MIL SPACING		5 8
	INT_CPUFB_OUT		3			10 MIL SPACING		8
	INT_CPUFB_OUT_SHORT		3			10 MIL SPACING		8
	INT_CPUFB_OUT_NORM		3			10 MIL SPACING		8
	INT_CPUFB_IN_NORM		3			10 MIL SPACING		8
	INT_CPUFB_LONG		3			10 MIL SPACING		8
	INT_CPUFB_IN				200.0000	10 MIL SPACING		8
	SYSCLK_DDRCLK_A0_UF		3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A0_L_UF		3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A1_UF		3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A1_L_UF		3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B0_UF		3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B0_L_UF		3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B1_UF		3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B1_L_UF		3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A0	DDRCLK_A0	3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_A0_L	DDRCLK_A0			200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_A1	DDRCLK_A1	3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_A1_L	DDRCLK_A1			200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B0	DDRCLK_B0	3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B0_L	DDRCLK_B0	3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B1	DDRCLK_B1	3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B1_L	DDRCLK_B1	3		200.0000	10 MIL SPACING		9 11
	INT_REF_CLK_OUT		3		200.0000	10 MIL SPACING		14
	INT_REF_CLK_IN				200.0000	10 MIL SPACING		14
	CLK66M_GPU_AGP_UF				200.0000	10 MIL SPACING		12
	CLK66M_GPU_AGP		4		200.0000	10 MIL SPACING		12 18
	INT_AGP_FB_OUT				200.0000	10 MIL SPACING		12
	INT_AGP_FB_IN		4		200.0000	10 MIL SPACING		12
	CLK33M_CBUS_UF				200.0000	10 MIL SPACING		12
	CLK33M_CBUS	SHOULD BE AT MOST 4 VIAS FOR CLK	6		200.0000	10 MIL SPACING		12 17
	CLK33M_AIRPORT_UF				200.0000	10 MIL SPACING		12
	CLK33M_AIRPORT	SHOULD BE AT MOST 4 VIAS FOR CLK	6		200.0000	10 MIL SPACING		12 25 40
	CLK33M_USB2_UF				200.0000	10 MIL SPACING		12
	CLK33M_USB2	SHOULD BE AT MOST 4 VIAS FOR CLK	6		200.0000	10 MIL SPACING		12 27
	INT_PCI_FB_OUT				200.0000	10 MIL SPACING		12
	INT_PCI_FB_IN		3		200.0000	10 MIL SPACING		12
MAP31	GPU_CLK27M_OUT					10 MIL SPACING		
	GPU_CLK27M_UF					10 MIL SPACING		
	GPU_SSCLK_UF					10 MIL SPACING		
	GPU_SSCLK_IN					10 MIL SPACING		
	GPU_FBCLK0					10 MIL SPACING		
	GPU_FBCLK0_L					10 MIL SPACING		
	GPU_FBCLK1					10 MIL SPACING		
	GPU_FBCLK1_L					10 MIL SPACING		
	GPU_DVO_CLKP					10 MIL SPACING		19
CRYSTALS	CLK27M_GPU_XOUT					10 MIL SPACING		
	CLK27M_XTAL_IN					10 MIL SPACING		
	CLK27M_GPU_XIN					10 MIL SPACING		
	CLK18M_INT_XIN					10 MIL SPACING		14
	CLK18M_INT_XOUT					10 MIL SPACING		14
	CLK18M_XTAL_IN					10 MIL SPACING		14
	CLK18M_INT_EXT					10 MIL SPACING		14
	CLK25M_ENET_XIN					10 MIL SPACING		28
	CLK25M_ENET_XOUT					10 MIL SPACING		28
	NEC_XT1					10 MIL SPACING		27
	NEC_XT2	THERE'S ANOTHER 280MIL LEG				10 MIL SPACING		27
SOUND	SND_SCLK		7		200.0000	10 MIL SPACING		14 26 40
	SND_CLKOUT				200.0000	10 MIL SPACING		14 26 40
ETHERNET MARVELL	CLKENET_PHY_RX				200.0000			28
	CLKENET_LINK_RX		3		200.0000	10 MIL SPACING		13 28
	CLKENET_PHY_GBE_REF				200.0000			28
	CLKENET_LINK_GBE_REF		3		200.0000	10 MIL SPACING		13 28
	CLKENET_PHY_TX				200.0000			28
	CLKENET_LINK_TX		5		200.0000	10 MIL SPACING		13 28
	CLKENET_LINK_GTX				200.0000			13
	CLKENET_PHY_GTX		3		200.0000	10 MIL SPACING		13 28
FIREWIRE	CLKFW_PHY_PCLK				200.0000			29
	CLKFW_LINK_PCLK		3		200.0000	10 MIL SPACING		13 29
	CLKFW_PHY_LCLK		3		200.0000	10 MIL SPACING		13 29
	CLKFW_LINK_LCLK				200.0000			13
	FW_XI				200.0000	10 MIL SPACING		29
	FW_OSC				200.0000	10 MIL SPACING		29

SIGNAL CONSTRAINTS - PAGE 1

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Digital Signals (cont'd)

GROUP	SIG_NAME	DELAY_RULE	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
AGP	AGP_AD<15..0>		5	100				66 MHz	12 18
AGP BYTES 0-1	AGP_CBE<1..0>		5	100				66 MHz	12 18
	AGP_AD_STB<0>		5	100		8 MIL SPACING			12 18
	AGP_AD_STB_L<0>		5	100		8 MIL SPACING			12 18
AGP BYTES 2-3	AGP_AD<31..16>		5	100				66 MHz	12 18
	AGP_CBE<3..2>		5	100				66 MHz	12 18
	AGP_AD_STB<1>		5	100		8 MIL SPACING			12 18
	AGP_AD_STB_L<1>			100		8 MIL SPACING			12 18
AGP SIDEBAND	AGP_SBA<7..0>		5	100				66 MHz	12 18
	AGP_SB_STB			100.0000		8 MIL SPACING			12 18
	AGP_SB_STB_L		5	100.0000		8 MIL SPACING			12 18
AGP CONTROL	AGP_FRAME_L			250.0000					12 18
	AGP_IRDY_L			250.0000					12 18
	AGP_TRDY_L		6	250.0000					12 18
	AGP_DEVSEL_L			250.0000					12 18
	AGP_STOP_L		6	250.0000					12 18
	AGP_PAR		6	250.0000					12 18
	AGP_REQ_L			285.0000					12 18
	AGP_GNT_L			250.0000					12 18
	AGP_RBF_L			250.0000					12 18
DVO	GPU_DVOD<0..23>		5	250					19 20
	GPU_DVO_HSYNC								19 20
	GPU_DVO_VSYNC								19 20
PCI	PCI_AD<31..0>					MIN_DAISY_CHAIN		33 MHz	9 12 17 25 27 40
	PCI_CBE<3..0>					MIN_DAISY_CHAIN		33 MHz	12 17 25 27 40
	PCI_FRAME_L					MIN_DAISY_CHAIN			12 17 25 27 40
	PCI_IRDY_L					MIN_DAISY_CHAIN			12 17 25 27 40
	PCI_TRDY_L					MIN_DAISY_CHAIN			12 17 25 27 40
	PCI_DEVSEL_L					MIN_DAISY_CHAIN			12 17 25 27 40
	PCI_STOP_L					MIN_DAISY_CHAIN			12 17 25 27 40
	PCI_PAR					MIN_DAISY_CHAIN			12 17 25 27 40
ULTRA ATA-100	UIDE_DATA<15..8>				200			100 MHZ	13 25
	UIDE_DATA<7>			NEED TO MATCH DELAY TO 250	200				13 25
	UIDE_DATA<6..0>				200			100 MHZ	13 25
	UIDE_ADDR<2..0>				200			100 MHZ	13 25
	UIDE_RST_L				200.0000				13 25
	UIDE_DIOW_L				200.0000				13 25
	UIDE_DIOR_L			10 MIL SPACING	200.0000				13 25
	UIDE_DMACK_L				200.0000				13 25
	UIDE_CS0_L				200.0000				13 25
	UIDE_CS1_L				200.0000				13 25
	UIDE_DMARQ				200.0000				13
	UIDE_IOCHRDY			10 MIL SPACING	200.0000				13 25
	UIDE_INTRQ				200.0000				13
	HD_DATA<15..0>		5		200			100 MHZ	25
	HD_ADDR<2..0>		5	TOTAL UIDE+HD SKEW <500MIL	200			100 MHZ	25
	HD_RESET_L		5		200.0000				25
	HD_DIOW_L		5		200.0000				25
	HD_DIOR_L		5	10 MIL SPACING	200.0000				25
	HD_DMACK_L		5		200.0000				25
	HD_CS0_L		5		200.0000				25
	HD_CS1_L		5		200.0000				25
	HD_DMARQ				200.0000				13 25
	HD_IOCHRDY		5	10 MIL SPACING	200.0000				25
	HD_INTRQ		5						13 25
EIDE INTREPID	EIDE_DATA<15..0>							33 MHZ	13 25
	EIDE_ADDR<2..0>							33 MHZ	13 25
	EIDE_CS0_L								13 25
	EIDE_CS1_L								13 25
	EIDE_RD_L								13 25
	EIDE_WR_L								13 25
	EIDE_IOCHRDY								13 25
	EIDE_INT								13 25
	EIDE_RST_L								13 25
	EIDE_DMACK_L								13 25
	EIDE_DMARQ								13 25
OPTICAL	EIDE_OPTICAL_DATA<15..0>							33 MHZ	25 40
	EIDE_OPTICAL_ADDR<2..0>							33 MHZ	25 40
	EIDE_OPTICAL_CS0_L								25 40
	EIDE_OPTICAL_CS1_L								25 40
	EIDE_OPTICAL_RD_L								25 40
	EIDE_OPTICAL_WR_L								25 40
	EIDE_OPTICAL_IOCHRDY								25 40
	EIDE_OPTICAL_INT								25 40
	EIDE_OPTICAL_RST_L								25 40
	EIDE_OPTICAL_DMAACK_L								25 40
	EIDE_OPTICAL_DMA_RQ								25 40
ETHERNET MII	ENET_LINK_RXD<7..0>		5						13 28
	ENET_RX_DV								13 28
	ENET_RX_ER								13 28
	ENET_PHY_TXD<7..0>		5						13 28
	ENET_LINK_TXD<7..0>								13
	ENET_PHY_TX_ER		5						13 28
	ENET_LINK_TX_ER								13
	ENET_PHY_TX_EN		5						13 28
	ENET_LINK_TX_EN								13
	ENET_MDIO								13 28
	ENET_MDC								13 28
	ENET_COL								13 28
	ENET_CRS								13 28
FIREWIRE MII	FW_LINK_DATA<7..0>		5						13 29
	FW_PHY_DATA<7..0>		5						29
	FW_LINK_CNTL<1..0>								13 29
	FW_PHY_CNTL<1..0>								29
	FW_LINK_LREQ								13
	FW_PHY_LREQ								13 29
	FW_PINT								13 29

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR	MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS	
ETHERNET	MDI_M<0>	ENET_MDI0				28
	MDI_P<0>	ENET_MDI0				28
	MDI_M<1>	ENET_MDI1	SPACING DELETED BECAUSE			28
	MDI_P<1>	ENET_MDI1	OF PHYSICAL CONSTRAINTS			28
	MDI_M<2>	ENET_MDI2	AROUND MARVELL PHY			28
	MDI_P<2>	ENET_MDI2				28
	MDI_M<3>	ENET_MDI3				28
	MDI_P<3>	ENET_MDI3				28
	RJ45_DN<0>	RJ45_DP0		10 MIL SPACING		28 40
	RJ45_DP<0>	RJ45_DP0		10 MIL SPACING		28 40
	RJ45_DN<1>	RJ45_DP1		10 MIL SPACING		28 40
	RJ45_DP<1>	RJ45_DP1		10 MIL SPACING		28 40
	RJ45_DN<2>	RJ45_DP2		10 MIL SPACING		28 40
	RJ45_DP<2>	RJ45_DP2		10 MIL SPACING		28 40
	RJ45_DN<3>	RJ45_DP3		10 MIL SPACING		28 40
	RJ45_DP<3>	RJ45_DP3		10 MIL SPACING		28 40
FIREWIRE	FW_TPA0N	FW_TPA0		MIN_LINE_WIDTH=3.4		
	FW_TPA0P	FW_TPA0		10 MIL SPACING		29 30
	FW_TPB0N	FW_TPB0		MIN_LINE_WIDTH=3.4		
	FW_TPB0P	FW_TPB0		10 MIL SPACING		29 30
	FW_TPI0N	FW_TPI0		MIN_LINE_WIDTH=3.4		
	FW_TPI0P	FW_TPI0		10 MIL SPACING		29 30
	FW_TPO0N	FW_TPO0		MIN_LINE_WIDTH=3.4		
	FW_TPO0P	FW_TPO0		10 MIL SPACING		30 40
	FW_TPA1N	FW_TPA1	500.0000	MIN_LINE_WIDTH=3.4		
	FW_TPA1P	FW_TPA1	500.0000	10 MIL SPACING		29 30
	FW_TPB1N	FW_TPB1	500.0000	MIN_LINE_WIDTH=3.4		
	FW_TPB1P	FW_TPB1	500.0000	10 MIL SPACING		29 30
	FW_TPI1N	FW_TPI1		MIN_LINE_WIDTH=3.4		
	FW_TPI1P	FW_TPI1		10 MIL SPACING		29 30
	FW_TPO1N	FW_TPO1		MIN_LINE_WIDTH=3.4		
	FW_TPO1P	FW_TPO1		10 MIL SPACING		30 40
LVDS LOWER	CLKLVDS_LN	CLKLVDS_L		10 MIL SPACING	4	30 40
	CLKLVDS_LP	CLKLVDS_L		10 MIL SPACING	4	19 22 40
	LVDS_L0N	LVDS_L0		10 MIL SPACING		19 22 40
	LVDS_L0P	LVDS_L0		10 MIL SPACING		19 22 40
	LVDS_L1N	LVDS_L1		10 MIL SPACING		19 22 40
	LVDS_L1P	LVDS_L1		10 MIL SPACING		19 22 40
	LVDS_L2N	LVDS_L2		10 MIL SPACING		19 22 40
	LVDS_L2P	LVDS_L2		10 MIL SPACING		19 22 40
UPPER	CLKLVDS_UN	CLKLVDS_U		10 MIL SPACING	4	19 22 40
	CLKLVDS_UP	CLKLVDS_U		10 MIL SPACING	4	19 22 40
	LVDS_U0N	LVDS_U0		10 MIL SPACING		19 22 40
	LVDS_U0P	LVDS_U0		10 MIL SPACING		19 22 40
	LVDS_U1N	LVDS_U1		10 MIL SPACING		19 22 40
	LVDS_U1P	LVDS_U1		10 MIL SPACING		19 22 40
	LVDS_U2N	LVDS_U2		10 MIL SPACING		19 22 40
	LVDS_U2P	LVDS_U2		10 MIL SPACING		19 22 40
TMDS	TMDS_CONN_CLKN	CLKCONN_TMDS		10 MIL SPACING	4	22 40
	TMDS_CONN_CLKP	CLKCONN_TMDS		10 MIL SPACING	4	22 40
	TMDS_CLKN	CLKTMDS		10 MIL SPACING	4	20 22
	TMDS_CLKP	CLKTMDS		10 MIL SPACING	4	20 22
	TMDS_DN<0>	TMDS_D0		10 MIL SPACING		20 22 40
	TMDS_DP<0>	TMDS_D0		10 MIL SPACING		20 22 40
	TMDS_DN<1>	TMDS_D1		10 MIL SPACING		20 22 40
	TMDS_DP<1>	TMDS_D1		10 MIL SPACING		20 22 40
	TMDS_DN<2>	TMDS_D2		10 MIL SPACING		20 22 40
	TMDS_DP<2>	TMDS_D2		10 MIL SPACING		20 22 40
USB	NEC_USB_DAM	NEC_USB_DA	MIN_LINE_WIDTH=5	10 MIL SPACING		27
	NEC_USB_DAP	NEC_USB_DA	MIN_LINE_WIDTH=5	10 MIL SPACING		27
	USB_DEM	USB_DE		5 MIL SPACING		14
	USB_DEP	USB_DE		5 MIL SPACING		14
	NEC_USB_DBM	NEC_USB_DB	MIN_LINE_WIDTH=5	10 MIL SPACING		27
	NEC_USB_DBP	NEC_USB_DB	MIN_LINE_WIDTH=5	10 MIL SPACING		27
	USB_DFM	USB_DF		5 MIL SPACING		14
	USB_DFP	USB_DF		5 MIL SPACING		14
	BT_USB_DM	BT_USB_D		5 MIL SPACING		14 25 40
	BT_USB_DP	BT_USB_D		5 MIL SPACING		14 25 40
	NEC_USB_RSDM1	NEC_USB_RSD1	MIN_LINE_WIDTH=5	10 MIL SPACING		27
	NEC_USB_RSDP1	NEC_USB_RSD1	MIN_LINE_WIDTH=5	10 MIL SPACING		27
	NEC_USB_RSDM2	NEC_USB_RSD2	MIN_LINE_WIDTH=5	10 MIL SPACING		27
	NEC_USB_RSDP2	NEC_USB_RSD2	MIN_LINE_WIDTH=5	10 MIL SPACING		27
	MODEM_USB_DM	MODEM_USB_D		5 MIL SPACING		14 26 40
	MODEM_USB_DP	MODEM_USB_D		5 MIL SPACING		14 26 40
	LEFT_USB_DM	LEFT_USB	MIN_LINE_WIDTH=5	10 MIL SPACING		25 27 40
	LEFT_USB_DP	LEFT_USB	MIN_LINE_WIDTH=5	10 MIL SPACING		25 27 40
	RIGHT_USB_DM	RIGHT_USB	MIN_LINE_WIDTH=5	10 MIL SPACING		27 33 40
	RIGHT_USB_DP	RIGHT_USB	MIN_LINE_WIDTH=5	10 MIL SPACING		27 33 40
POWER SUPPLIES	1772_CSSN	1772_CSS		DIFF		32
	1772_CSSP	1772_CSS		DIFF		32
	1772_CSIN	1772_CSI		DIFF		32
	1772_CSIP	1772_CSI		DIFF		32
	3V_SNSM	3V_SNS		DIFF		34
	3V_SNSP	3V_SNS		DIFF		34
	5V_SNSM	5V_SNS		DIFF		34
	5V_SNSP	5V_SNS		DIFF		34
THERMOSTAT	THERM1_DM	THERM1		DIFF		26
	THERM1_DP	THERM1		DIFF		26
	THERM2_DM	THERM2		DIFF		26
	THERM2_DP	THERM2		DIFF		26
	THERM1_M_DM	THERM1_MAIN		DIFF		
	THERM1_M_DP	THERM1_MAIN		DIFF		
	THERM2_M_DM	THERM2_MAIN		DIFF		
	THERM2_M_DP	THERM2_MAIN		DIFF		
	THERM1_A_DM	THERM1_ALT		DIFF		26
	THERM1_A_DP	THERM1_ALT		DIFF		26
	THERM2_A_DM	THERM2_ALT		DIFF		26
	THERM2_A_DP	THERM2_ALT		DIFF		26

INTERNAL LAYER

ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.57OHM
ZDIFF = 99.8OHM

FOR FIREWIRE
ER = 4.3 (DIELECTRIC CONSTANT)
W = 3.4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 53.37OHM
ZDIFF = 107.17OHM

INTERNAL LAYER (USB1.1/USB 2.0)

ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL(USB 1.1)/ 5MIL(USB 2.0) (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 5MIL (USB 1.1) (SEPERATION OF DIFF TRACES)
S = 10MIL (USB 2.0) (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.5OHM (USB 1.1)/ 46.2OHM (USB 2.0)
ZDIFF = 89.3OHM (USB 1.1)/ 89.4OHM (USB 2.0)

SIGNAL CONSTRAINTS - PAGE 2

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	C
SCALE: NONE	SHT 38 OF 45	

POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH
MAIN/SLEEP	+24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 40
	+BATT	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 40
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 23
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 23
	+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6 20 23
	+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 40
	+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+2_5V_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6 40
	+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+1_5V_SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+1_5V_LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 36
	+1_5V_SLEEP_VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 36
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 32 33
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 32
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 32
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 32 40
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 32 40
	1772_DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10	32
	1772_LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 32
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 32
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 32
	+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 32
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 32
	1772_LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 32
	1772_DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 32
	1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 32
PMU	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 33
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 33
	+4_85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 31 33
	+4_6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 33 34
	+4_85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 33
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 33
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 26 31
MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 25 34
	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 25
TRACKPAD	+5V_MAIN_CONN	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 23 40
VIDEO	+12_8V_INV	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 22 40
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 22
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 22 40
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 22 40
	+5V_DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 22
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10 22
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 22
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 22
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 22
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 22 40
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 22 40
KB LED	KBDLED_ANODE	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 23
	KBDLED_RETURN	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 23
FAN GND	FANL_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 40
	FANR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 40
SOUND	+5V_SOUND_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	SND_AGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=15 26

I/O AREA	GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6
	CHGND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12 CHGND1
INVERTER	CHGND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12 CHGND2
TRACKPAD	CHGND3	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12 CHGND3
LVDS	CHGND4	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12 CHGND4 40
I/O AREA	CHGND5	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12 CHGND5
I/O AREA	CHGND6	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12 CHGND6
	ENET_CTAP_CHGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12 28

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 5 6 35 40
	CPU_AVDD	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 5
	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 5 6 7 8 15 16 35
DDR RAM	DDR_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 11
INTREPID	+2_5V_INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 9 10 15 16
	+3V_INTREPID_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 14
PLLS	+1_5V_INTREPID_PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 8 12 14
	+1_5V_INTREPID_PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6 14
	+1_5V_INTREPID_PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6 14
	+1_5V_INTREPID_PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6 14
	+1_5V_INTREPID_PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5 14
	+1_5V_INTREPID_PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5 12
	+1_5V_INTREPID_PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6 12
	+1_5V_INTREPID_PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6 8
	+1_5V_INTREPID_PLL8	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6 14
REFERENCE	INT_MEM_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 9
	INT_AGP_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 12 18
	INT_MEM_REF_H	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 9
	UIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 13
CARDBUS	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 17
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 17
ATI M11	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10 18 19 40
	+GPU_MEM	VOLTAGE=2.5V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10 18 21
	+3V_GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 12 18 19 21
	+3V_GPU_FLT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8 21
	+1_5V_AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 12 15 16 18 19 21
	GPU_MEM_IO	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	GPU_MEM_IO_FLT	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 21
	+GPU_MEMCORE	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 21
	+1_8V_GPU	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 18 19 20 21
	+2_5V_GPU_PNLIO	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 21
	+1_8V_ATI_PVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 19 21
	+1_5V_AGP_GPU	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 21
	+1_5V_GPU_VDD15	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 19
	+1_8V_GPU_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 21
134	+1_8V_GPU_VDDDI	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 21
135	GPU_VCORE_VDDCI	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 18
136	+2_5V_GPU_A2VDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 21
137	+1_8V_GPU_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 21
138	+1_8V_GPU_PNLPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 21
139	+1_8V_GPU_PNLIO	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 21
140	GPU_MCLK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 21
141	+1_8V_GPU_AVDDQ	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 21
142	+1_8V_GPU_MEMPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 21
143	+3V_ATI_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 18
144	+3V_ATI_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 18
145	+GPU_VDD15_UF	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 19
146	+2_5V_SLEEP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 19
147	+3V_SLEEP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 21
148	+1_5V_AGP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 19
149	+1_8V_PVDD_NECK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 19
150	GPU_VCORE_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 19
151	+GPU_VDD15_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 19
152	+2_5V_SLEEP_NECK2	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 21
153	+1_8V_SLEEP_NECK	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 21
154	+1_5V_SLEEP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 21
155	+2_5V_GPU	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 21
SILICON IMIAGE	PP3V3_SI_PVCC1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0 20
	PP3V3_SI_AVCC1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0 20
	PP3V3_SI_VCC1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0 20
	PP3V3_SI_PVCC2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0 20
	PP3V3_SI_AVCC2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0 20
	PP3V3_SI_VCC2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0 20
88E1111	+2_5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 28
	+2_5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8 28
	+1_0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8 28
	LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8 28
	LM2594_IN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
FW	+3V_FW_ESD_ILIM	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 30
	+3V_FW_ESD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 30
	+FW_FUSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30
	+FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30
	+FW_PWR_OR	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 29 30
	+FW_VP0	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30
	+FW_PWR_PORTA	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30
	+FW_VP1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30
	+3V_FW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29 30
	+3V_FW_UF	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6 29
	+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_PLLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30
	FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30
	FW_TPO0R	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 30 40
	NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 27
USB 2.0	+3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 27
INTREPID	+3V_CG_PLL_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8 14
SSCG	+2_5V_CG_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8 14

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 33
	1625_VSW	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 33
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 33
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 33
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 33
	1V20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 2 33
LTC3707 5V SWITCHER	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 4
	5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 4
	5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 4
3V SWITCHER	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 4
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 4
	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 34
MAX1715 2.5V SWITCHER	2_5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 6
	2_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 6
	2_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 6
	2_5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 6
	2_5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 6
1.5V SWITCHER	1_5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 36
	1_5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 6
	1_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 6
	1_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 6
	1_5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 6
	1_5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 6
CONTROL	1_5V_ILIM		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 36
	2_5V_ILIM		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 36
	MAX1715_TON		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 36
	MAX1715_SKIP		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 36
	MAX1715_REF	VOLTAGE=2.0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 36
	MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 6
	MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10 6
MAX1717	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 5
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 5
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 5
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 5
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 5
	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 5
	VCORE_ILIM		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 35
	VCORE_REF		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 35
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 35
	VCORE_CC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 35
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 35 40
	VCORE_TIME		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 35
	VCORE_VGATE		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 14 35
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=15 5
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 35
	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 35
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 35
LTC1778	1778_VIN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 9
	1778_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 9
	1778_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10 9
	1778_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 9
	1778_BST_RC	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 9
	1778_TG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 9
	1778_BG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 9
	GPU_VCORE_SW	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 9
	1778_ION		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 19
	1778_ITH		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 19
	1778_ITH_RC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 19
	1_5V_2_5V_OK		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 36
	1778_VFB		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 19 40
	1778_FCB		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 19
	1778_VRNG		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 19
LTC3411	LTC3411_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	LTC3411_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10
	1_8V_SW	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10 6
	1_8V_VFB		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6
	LTC3411_ITH_RC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6
	LTC3411_ITH		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6
	LTC3411_SYNC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6
	LTC3411_SHDN		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6
LTC1962 INT PLLS	LTC1962_INT_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 4
	LTC1962_L3_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	LTC1962_L3_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	LTC1962_1V5_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	LTC1962_1V5_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10

SIGNAL CONSTRAINTS - PAGE 3

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	C
SCALE: NONE	SHT 39 OF 45	

FUNCTIONAL TEST POINTS

FUNC_TEST=YES JTAG_ASIC_TMS 13 28
FUNC_TEST=YES JTAG_ASIC_TDI 28
FUNC_TEST=YES JTAG_ASIC_TDO 13 14
FUNC_TEST=YES JTAG_ASIC_TCK 13 28
FUNC_TEST=YES JTAG_ASIC_TRST_L 13 28
FUNC_TEST=YES CPU_CHKSTP_OUT_L 5
FUNC_TEST=YES CPU_SRESET_L 5
FUNC_TEST=YES CPU_HRESET_L 5 6 7
FUNC_TEST=YES JTAG_CPU_TMS 5 6
FUNC_TEST=YES JTAG_CPU_TDI 5 6
FUNC_TEST=YES JTAG_CPU_TDO_TP 5
FUNC_TEST=YES JTAG_CPU_TCK 5 6
FUNC_TEST=YES JTAG_CPU_TRST_L 5 6 40

FUNC_TEST=YES TMDS_CONN_CLKP 22 38
FUNC_TEST=YES VGA_R 22
FUNC_TEST=YES VGA_G 22
FUNC_TEST=YES VGA_B 22
FUNC_TEST=YES VGA_VSYNC 22
FUNC_TEST=YES VGA_HSYNC 22
FUNC_TEST=YES DVI_DDC_CLK_UF 22
FUNC_TEST=YES DVI_DDC_DATA_UF 22
FUNC_TEST=YES DVI_HPD_UF 22
FUNC_TEST=YES LVDS_L0N 19 22 38
FUNC_TEST=YES LVDS_L0P 19 22 38
FUNC_TEST=YES LVDS_L1N 19 22 38
FUNC_TEST=YES LVDS_L1P 19 22 38
FUNC_TEST=YES LVDS_L2N 19 22 38
FUNC_TEST=YES LVDS_L2P 19 22 38
FUNC_TEST=YES CLKLVDS_LN 19 22 38
FUNC_TEST=YES CLKLVDS_LP 19 22 38
FUNC_TEST=YES LVDS_U0N 19 22 38
FUNC_TEST=YES LVDS_U0P 19 22 38
FUNC_TEST=YES LVDS_U1N 19 22 38
FUNC_TEST=YES LVDS_U1P 19 22 38
FUNC_TEST=YES LVDS_U2N 19 22 38
FUNC_TEST=YES LVDS_U2P 19 22 38
FUNC_TEST=YES CLKLVDS_UN 19 22 38
FUNC_TEST=YES CLKLVDS_UP 19 22 38
FUNC_TEST=YES LVDS_DDC_CLK 19 22
FUNC_TEST=YES LVDS_DDC_DATA 19 22
FUNC_TEST=YES BRIGHT_PWM 22
FUNC_TEST=YES TV_GND1 22 39
FUNC_TEST=YES TV_GND2 22 39

FUNC_TEST=YES TV_C 22
FUNC_TEST=YES TV_Y 22
FUNC_TEST=YES TV_COMP 22
FUNC_TEST=YES SND_TO_AUDIO 14 26
FUNC_TEST=YES SND_SYNC 14 26
FUNC_TEST=YES SND_CLKOUT 14 26 37
FUNC_TEST=YES INT_AUDIO_TO_SND 14 26
FUNC_TEST=YES SND_SCLK 14 26 37
FUNC_TEST=YES SND_HW_RESET_L 14 26
FUNC_TEST=YES SND_HP_SENSE_L
FUNC_TEST=YES SND_LIN_SENSE_L
FUNC_TEST=YES INT_I2C_DATA2 14 26
FUNC_TEST=YES INT_I2C_CLK2 14 26
FUNC_TEST=YES T393 CHGND4 39
FUNC_TEST=YES T394 SLEEP_LED

FUNC_TEST=YES INT_I2C_CLK0 6 11 13 23
FUNC_TEST=YES INT_I2C_DATA0 6 11 13 23
FUNC_TEST=YES INT_I2C_CLK1 13 14 23 24 26
FUNC_TEST=YES INT_I2C_DATA1 13 14 23 24 26
FUNC_TEST=YES CBUS_DET_1_L 17
FUNC_TEST=YES CBUS_DET_2_L 17
FUNC_TEST=YES TMDS_DN<0> 20 22 38
FUNC_TEST=YES TMDS_DP<0> 20 22 38
FUNC_TEST=YES TMDS_DN<1> 20 22 38
FUNC_TEST=YES TMDS_DP<1> 20 22 38
FUNC_TEST=YES TMDS_DN<2> 20 22 38
FUNC_TEST=YES TMDS_DP<2> 20 22 38
FUNC_TEST=YES TMDS_CONN_CLKN 22 38

FUNC_TEST=YES BT_USB_DM 14 25 38
FUNC_TEST=YES BT_USB_DP 14 25 38
FUNC_TEST=YES MODEM_USB_DM 14 26 38
FUNC_TEST=YES MODEM_USB_DP 14 26 38
FUNC_TEST=YES PCI_AD<0> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<1> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<2> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<3> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<4> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<5> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<6> 9 12 17 25 27 38

FUNC_TEST=YES PCI_AD<7> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<8> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<9> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<10> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<11> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<12> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<13> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<14> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<15> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<16> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<17> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<18> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<19> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<20> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<21> 12 17 25 27 38
FUNC_TEST=YES PCI_AD<22> 12 17 25 27 38
FUNC_TEST=YES PCI_AD<23> 12 17 25 27 38
FUNC_TEST=YES PCI_AD<24> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<25> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<26> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<27> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<28> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<29> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<30> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<31> 9 12 17 25 27 38
FUNC_TEST=YES PCI_FRAME_L 12 17 25 27 38
FUNC_TEST=YES PCI_TRDY_L 12 17 25 27 38
FUNC_TEST=YES PCI_IRDY_L 12 17 25 27 38
FUNC_TEST=YES PCI_DEVSEL_L 12 17 25 27 38
FUNC_TEST=YES PCI_STOP_L 12 17 25 27 38

FUNC_TEST=YES PCI_PAR 12 17 25 27 38
FUNC_TEST=YES PCI_CBE<0> 12 17 25 27 38
FUNC_TEST=YES PCI_CBE<1> 12 17 25 27 38
FUNC_TEST=YES PCI_CBE<2> 12 17 25 27 38
FUNC_TEST=YES PCI_CBE<3> 12 17 25 27 38
FUNC_TEST=YES AIRPORT_PCI_REQ_L 12 25
FUNC_TEST=YES AIRPORT_PCI_GNT_L 12 25
FUNC_TEST=YES AIRPORT_PCI_INT_L 14 25
FUNC_TEST=YES EIDE_OPTICAL_DATA<0> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<1> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<2> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<3> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<4> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<5> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<6> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<7> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<8> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<9> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<10> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<11> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<12> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<13> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<14> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<15> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DMA_RQ 25 38
FUNC_TEST=YES EIDE_OPTICAL_RD_L 25 38
FUNC_TEST=YES EIDE_OPTICAL_DMAACK_L 25 38
FUNC_TEST=YES EIDE_OPTICAL_ADDR<0> 25 38
FUNC_TEST=YES EIDE_OPTICAL_ADDR<1> 25 38
FUNC_TEST=YES EIDE_OPTICAL_ADDR<2> 25 38
FUNC_TEST=YES SND_AMP_MUTE 26
FUNC_TEST=YES SND_HP_MUTE_INV

FUNC_TEST=YES EIDE_OPTICAL_CS0_L 25 38
FUNC_TEST=YES EIDE_OPTICAL_CS1_L 25 38
FUNC_TEST=YES EIDE_OPTICAL_RST_L 25 38
FUNC_TEST=YES EIDE_OPTICAL_WR_L 25 38
FUNC_TEST=YES EIDE_OPTICAL_IOCHRDY 25 38
FUNC_TEST=YES EIDE_OPTICAL_INT 25 38
FUNC_TEST=YES TPAD_F_TXD
FUNC_TEST=YES TPAD_F_RXD
FUNC_TEST=YES LID_CLOSED_L 23
FUNC_TEST=YES COMM_RESET_L 14 26
FUNC_TEST=YES COMM_SHUTDOWN 14 26
FUNC_TEST=YES COMM_RING_DET_L 14 26 31
FUNC_TEST=YES +5V_TPAD_SLEEP
FUNC_TEST=YES +3V_HALL_EFFECT 23 39
FUNC_TEST=YES KBD_CAPSLOCK_LED
FUNC_TEST=YES KBD_FUNCTION_L 23 31
FUNC_TEST=YES KBD_CONTROL_L 23 31
FUNC_TEST=YES +PPBATT_ISNS_N 24
FUNC_TEST=YES KBD_OPTION_L 23 31
FUNC_TEST=YES KBD_SHIFT_L 23 31
FUNC_TEST=YES KBD_X<0> 23 31
FUNC_TEST=YES KBD_X<1> 23 31
FUNC_TEST=YES KBD_X<3> 23 31
FUNC_TEST=YES MMM_ACC_SELFTEST 24
FUNC_TEST=YES MMM_ACC_X_AXIS 24
FUNC_TEST=YES MMM_ACC_Y_AXIS 24
FUNC_TEST=YES MMM_ACC_Z_AXIS 24
FUNC_TEST=YES SRCLK_TP 27
FUNC_TEST=YES SRMOD_TP 27
FUNC_TEST=YES TEB_TP 27
FUNC_TEST=YES TEST_TP 27

FUNC_TEST=YES KBD_Y<0> 31
FUNC_TEST=YES KBD_Y<1> 31
FUNC_TEST=YES KBD_Y<3> 31
FUNC_TEST=YES KBD_Y<4> 31
FUNC_TEST=YES KBD_Y<6> 31
FUNC_TEST=YES KBD_Y<7> 31
FUNC_TEST=YES KBD_NUMLOCK_LED
FUNC_TEST=YES +BATT_POS 32 39
FUNC_TEST=YES BATT_CLK 32
FUNC_TEST=YES BATT_DATA 32
FUNC_TEST=YES BATT_NEG 32 39
FUNC_TEST=YES PMU_BATT_DET_L 31 32
FUNC_TEST=YES FANR_GND 39
FUNC_TEST=YES FANL_GND 39
FUNC_TEST=YES FANL_TACH
FUNC_TEST=YES FANR_PWM
FUNC_TEST=YES FANL_PWM
FUNC_TEST=YES RJ45_DP<0> 28 38
FUNC_TEST=YES RJ45_DN<0> 28 38
FUNC_TEST=YES RJ45_DP<1> 28 38
FUNC_TEST=YES RJ45_DN<1> 28 38
FUNC_TEST=YES RJ45_DP<2> 28 38
FUNC_TEST=YES RJ45_DN<2> 28 38
FUNC_TEST=YES RJ45_DP<3> 28 38
FUNC_TEST=YES RJ45_DN<3> 28 38
FUNC_TEST=YES FW_TPO0R 30 39
FUNC_TEST=YES VCORE_VID0
FUNC_TEST=YES VCORE_VID1
FUNC_TEST=YES VCORE_VID2
FUNC_TEST=YES VCORE_VID3
FUNC_TEST=YES VCORE_VID4

FUNC_TEST=YES FW_TPO1P 30 38
FUNC_TEST=YES FW_TPO1N 30 38
FUNC_TEST=YES FW_TPI1P 30 38
FUNC_TEST=YES FW_TPI1N 30 38
FUNC_TEST=YES CHARGE_LED_L 31 32
FUNC_TEST=YES ADAPTER_DET 31 32
FUNC_TEST=YES SUTRO_ALS_GAIN_SW 23 25
FUNC_TEST=YES SUTRO_ALS_OUT 23 25
FUNC_TEST=YES KBD_LED1_OUT
FUNC_TEST=YES KBD_LED2_OUT
FUNC_TEST=YES COMM_TXD_L 14 26
FUNC_TEST=YES COMM_TRXC 14 26
FUNC_TEST=YES COMM_GPIO_L 14 26
FUNC_TEST=YES COMM_DTR_L 14 26
FUNC_TEST=YES COMM_RTS_L 14 26
FUNC_TEST=YES COMM_RXD 14 26
FUNC_TEST=YES PMU_KB_RESET_L
FUNC_TEST=YES PWR_BUTTON_L 23 26
FUNC_TEST=YES +PBUS 39
FUNC_TEST=YES +24V_PBUS 39
FUNC_TEST=YES GPU_VCORE 18 19 39
FUNC_TEST=YES CPU_VCORE_SLEEP 5 6 35 39
FUNC_TEST=YES VCORE_FB 35 39
FUNC_TEST=YES +1_8V_MAIN 39
FUNC_TEST=YES +3V_PMU 39
FUNC_TEST=YES +5V_DDC_SLEEP 22 39
FUNC_TEST=YES +12_8V_INV 22 39
FUNC_TEST=YES VCORE_MUX_EN 35

FUNC_TEST=YES +5V_INV_SW 22 39
FUNC_TEST=YES LEFT_USB_DM 25 27 38
FUNC_TEST=YES LEFT_USB_DP 25 27 38
FUNC_TEST=YES RIGHT_USB_DM 27 33 38
FUNC_TEST=YES RIGHT_USB_DP 27 33 38
FUNC_TEST=YES NEC_LEFT_USB_PWREN 25 27
FUNC_TEST=YES NEC_LEFT_USB_OVERCURRENT 25 27
FUNC_TEST=YES NEC_RIGHT_USB_PWREN 27 33
FUNC_TEST=YES NEC_RIGHT_USB_OVERCURRENT 27 33
FUNC_TEST=YES DCDC_EN 19 30 34 35
FUNC_TEST=YES BBANG_HRESET_L 6
FUNC_TEST=YES MAIN_RESET_L 14 17 18 20 25 27 31
FUNC_TEST=YES RF_DISABLE_L_SPN 25
FUNC_TEST=YES AIRPORT_CLKRUN_L 25
FUNC_TEST=YES ROM_RW_L 9 12 25
FUNC_TEST=YES ROM_ONBOARD_CS_L 9 25
FUNC_TEST=YES ROM_CS_L 9 12 25
FUNC_TEST=YES CLK33M_AIRPORT 12 25 37
FUNC_TEST=YES AIRPORT_IDSEL 25
FUNC_TEST=YES ROM_OE_L 9 12 25
FUNC_TEST=YES INT_MOD_DTI 14 26
FUNC_TEST=YES JTAG_CPU_TRST_L 5 6 40
FUNC_TEST=YES MOD_BITCLK 14 26
FUNC_TEST=YES MOD_CLKOUT 14 26
FUNC_TEST=YES MOD_DTO 14 26
FUNC_TEST=YES MOD_SYNC 14 26
FUNC_TEST=YES SLEEP 23 31 34 36
FUNC_TEST=YES 1778_VFB 19 39

FUNCTIONAL TEST POINTS

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	C
SCALE: NONE	SHT 40 OF 45	

REVISION HISTORY

12/11/03

1) IMPORTED Q41 PRODUCTION RELEASE SCHEMATIC
2) CHANGED CPU (U43) TO A7PM
3) CHANGED PLL CONFIG STUFFING FOR NEW CPU
4) CHANGED U44 TO M1Y-PSP64 SYMBOL
5) ADDED CPU AVDD LDO (U6)
6) ADDED R284 AND R604 TO ADD OPTION FOR PD_I OF U42 (CLOCK CHIP) TO BE DRIVEN BY JTAG_ASIC_TDO FROM INTREPID
7) ADDED R608 TO DISCONNECT INT_GPIO0 FROM CS_FSEL
8) CHANGED JTAG_ASIC_TDO_TP TO JTAG_ASIC_TDO AND MOVED IT TO INTREPID'S TDO
9) CHANGED JTAG_ASIC_TDI TO CONNECT TO ETHERNET PHY'S TDI

12/15/03

10) CHANGED PIN 4 (DCDC_EN) ON J11 TO NEC_RIGHT_USBOVERCURRENT
11) CHANGED PIN 11 OF J11 TO NC

12/16/03

12) ADDED R633 AS PULLUP ON JTAG_ASIC_TDI
13) CHANGED CPU_TEMP_DM TO CPU_THERM_DM
14) CHANGED CPU_TEMP_DP TO CPU_THERM_DP
15) CHANGED GPU_THERM_DP TO GPU_THERM_DP_TP
16) CHANGED GPU_THERM_DM TO GPU_THERM_DM_TP
17) FIXED MISSED CONNECTION WITH MAXBUS_SLEEP TO CPU

12/17/03

18) CHANGED R657 (EXTPLL_SDWN_POL_BOOT_STRAP) TO NO_STUFF AND REMOVED NO_STUFF FROM R153
19) UPDATE DIFF_NET_SPACING_TYPE PROPERTY ON POWER_SUPPLY_SENSE AND THERMAL_DIODE_DIFF_PAIRS
20) CHANGED FIREWIRE OSCILLATOR (G1) TO NEW PREFERRED SUNNY PART

12/18/03

21) CHANGED MAX_VIA_COUNT ON ALL AGP_STB NETS TO 5 TO CLEAR DRCS

** RELEASED FOR EVT **

2/10/04

22) REMOVED XW11 - JUMPER ON 1.8V SWITCHER OUTPUT
23) CHANGED R657 TO STUFFE AND R153 TO NO STUFF
24) CHANGED CPU PLL CONFIG TO 9X HIGH AND 5X LOW

** RELEASED FOR DVT **

3/24/04

25) REMOVED ALTERNATE BOM OPTION FROM ALTERNATE ETHERNET CRYSTALS

3/29/04

26) ADDED ALTERNATE FOR Q41A REV 1.1.1 CPU (U43)
27) ADDED ALTERNATES FOR 128MB AND 64MB A16_M11_S
28) CHANGED TMDS SERIES RPAKS TO 0 OHMS (RP57,RP27,RP32,RP28)
29) ADDED ALTERNATE FOR ALS OP-AMP (U40)

** RELEASED TO REV A **

30) CHANGED TMDS TERMINATION R,C AND LS TO PRODUCTION VALUES

** RELEASED TO REV A UNDER NEW PART NUMBER **

09/17/2004

1) GPU_DVOD<0..12> NETNAME CHANGE TO GPU_DVOD<0..23>
2) D8 FROM 1N5227B CHANGE TO BZX84C2V7LT1
3) R751 VALUE FROM 10K OHM CHANGE TO 604 OHM
4) ADD C935 (0.1UF)
5) ADD R867 (0 OHM) FOR IPOD ACTION
6) PMU PIN74 NETNAME FROM NC TO PMU_SELECT
7) ADD R868 (10K OHM; NO_STUFF) PULL UP TO +3V_PMU
8) ADD R869 (10K OHM) PULL DOWN TO GND
9) PMU PIN 91 NETNAME FROM NC TO SYS_BATT_ISNS2
10) ADD R870 (0 OHM) SYS_BATT_ISNS2 LINK TO SYS_BATT_ISNS
11) ADD U51 (INA138)
12) ADD R852 (0.010 OHM),R853 (150K OHM) AND R857(49.9 OHM)
13) ADD C917 (0.1UF) AND C925 (10UF)
14) ADD DESCRIPTION FOR MMM I2C BUS
15) MMM I2C BUS LINK TO INTREPID :INT_I2C_CLK1 AND INT_I2C_DATA1
16) CHANGE NETNAME FROM INT_EXTINT11_PU TO MMM_FFIRQ_L
17) CHANGE NETNAME FROM INT_EXTINT12_PU TO MMM_SIRQ_L
18) ADD R863 (10K OHM) AND R864 (10K OHM) FOR MMM_FFIRQ_L&MMM_SIRQ_L PULL UP TO +3V_MAIN
19) ADD U53 (16F818) AND U5 (KXM52)
20) ADD R845 (0 OHM),R846 (0 OHM;NO_STUFF),R847 (10K OHM;NO_STUFF),R848 (10K OHM;NO_STUFF)
21) ADD R849 (10K OHM),R850 (10K OHM;NO_STUFF),R851(0 OHM),R854 (10K OHM),R856 (10K OHM),
22) ADD R860 (0 OHM),R858 (0 OHM),R859 (0 OHM),R855 (10K OHM),R861 (10K OHM),R862(10K OHM;NO_STUFF)
23) ADD C936(0.1UF),C918(0.1UF),C919(0.1UF),C921(0.0047UF),C923(0.0047UF),C926(0.0047UF),C927(0.1UF)
24) DEL RP44 (100K OHM) AND ADD R874 (100K OHM), R875 (100K OHM) AND R873 (100K OHM)
25) ADD R872 (10K OHM) FOR AUDIO_LO_MUTE_L
26) ADD R871 (100 OHM) AND SUPERCAP C937 (N20P80;5.5V;ELEC;0.33F)
27) J21 PIN12 NETNAME FROM NC CHANGE TO THERM_L_OC
28) J21 PIN10 NETNAME FROM NC CHANGE TO INT_I2C_DATA1
29) J21 PIN11 NETNAME FROM NC CHANGE TO INT_I2C_CLK1
30) C592 VALUE FROM 0.001UF CHANGE TO 0.01UF (20%,50V,0603)
31) U59 FROM MP1518DJ CHANGE TO MM3120
32) L11 CHANGE TO 152S0235 (22UH;3.8*3.8*1.5MM)
33) DEL D31
34) R202 VALUE FROM 5.23 OHM CHANGE TO 25.5 OHM
35) C79 VALUE FROM 2.2UF CHANGE TO 1UF
36) ADD Q70 (SI3443), Q34 (2N7002)
37) ADD R866 (100K OHM),R865 (4.7 OHM),C929 (0.022UF)

09/20/2004

1) ADD R877 (10K OHM)
2) ADD R876 (470K OHM;NO_STUFF)

09/21/2004

1) ADD R878 AND R879 (0 OHM;NO_STUFF)[ADD A 0-OHM RESISTOR TO BY-PASS THE N-FET ON EACH FAN]

09/22/2004

1) R822 (680 OHM CHANGE TO 510 OHM) AND R826 (680 OHM CHANGE TO 510 OHM)

09/23/2004

1) ADD NC NETNAME AT U59 PIN6 AND PIN9
2) CHANGE R465 CAP SIZE FROM 0603 TO 0805
3) BOM OPTION FROM NO STUFF CHANGE TO SUPERCAP

09/24/2004

1) CHANGE R465 FROM MF 1/16W TO FF 1/10W
2) ADD R880 AND R871 (0 OHM;BOM_OPTIOM;FOR SUPERCAP AND BACKUP BATTERY SWITCH)
3) ADD U60 (LIS3L02AQ;ST SENSOR)
4) ADD R881 (10K OHM) ,R882 (10K OHM), R883 (10K OHM)
5) ADD C937 (0.1UF,10V,20%,0402)
6) ADD BOM_OPTION (KIONIX_ACCEL AND ST_ACCEL)

10/04/2004

1) CHANGE TEST POINT FUNC_TEST=NO FOR FUNC_TP_WRONG_SIDE.LOG
2) ADD NO_TEST=YES FOR NOTP.LOG(MMM_PIC_AN2_PD,MMM_PIC_AN3_PU)

10/05/2004

1) ADD R850 (0 OHM)

10/15/2004

1) REPLACE BOOT BANGER EEPROM U32 WITH 32KX M24256B FUNC_TP_WRONG_SIDE.LOG

12/16/2004

1) SCHEMATIC RELEASE FOR PRODUCTION

REVISION HISTORY(1 OF 1)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	C
SCALE: NONE	SHT 41 OF 45	

*** Signal Cross-Reference for the entire design ***

```
+1_0V_MARVELL        28D2< 39B3>
+1_5V_AGP            12C5< 12D1< 12D4< 15D6< 16C8<
                     18C6< 18D6< 19A8< 19B4<> 19D5<>
                     21B8< 21D6< 39C3>
+1_5V_AGP_GPU        21C5< 39C3>
+1_5V_AGP_NECK       19B4<> 39B3>
+1_5V_GPU_VDD15      19D3< 39C3>
+1_5V_INTREPID_PLL   8D6< 12D4< 12D8< 14D6<> 39D3>
+1_5V_INTREPID_PLL1  14C3< 39D3>
+1_5V_INTREPID_PLL2  14D3< 39D3>
+1_5V_INTREPID_PLL3  14D3< 39D3>
+1_5V_INTREPID_PLL4  14D3< 39D3>
+1_5V_INTREPID_PLL5  12D3< 39D3>
+1_5V_INTREPID_PLL6  12D6< 39D3>
+1_5V_INTREPID_PLL7  8D5< 39D3>
+1_5V_INTREPID_PLL8  14D3< 39D3>
+1_5V_LDO            36D8< 39D6>
+1_5V_MAIN           39D6>
+1_5V_SLEEP          39D6>
+1_5V_SLEEP_NECK     21A3<> 39B3>
+1_5V_SLEEP_VIN      36D8<> 39D6>
+1_8V_ATI_PVDD       19C5<> 21B6< 21B6< 21D6<> 39C3>
+1_8V_ATI_TPVDD      21D2<>
+1_8V_DVO_F          21B2<
+1_8V_GPU            18A7< 19C8< 20A8< 21A2< 21A6<
                     21B1< 21B6< 21C8< 21D6< 21D8< 39C3>
+1_8V_GPU_AVDD       21D5< 39C3>
+1_8V_GPU_AVDDQ      21D4< 21D7< 39C3>
+1_8V_GPU_MEMPLL     21B5< 39C3>
+1_8V_GPU_PLL        21D5< 39C3>
+1_8V_GPU_PNLIO      21A5< 39C3>
+1_8V_GPU_PNLPLL     21B5< 39C3>
+1_8V_GPU_TP_PLL     21B4< 21D1<
+1_8V_GPU_VDDDI      21C7< 21D4< 39C3>
+1_8V_MAIN           39D6> 40A2>
+1_8V_PVDD_NECK      19B5<> 39B3>
+1_8V_SLEEP          39D6>
+1_8V_SLEEP_NECK     21A3<> 39B3>
+1_95V_FW_DVDD       29C4< 29C7<> 29D5< 39A3>
+1_95V_FW_DVDD_PORT1 29D6< 39A3>
+1_95V_FW_DVDD_RX0   29C5< 39A3>
+1_95V_FW_DVDD_TX0   29C5< 39A3>
+1_95V_FW_PLL400VDD  29D5< 39A3>
+1_95V_FW_PLL500VDD  29D5< 39A3>
+1_95V_FW_PLLVDD     29D5< 29D7<> 39A3>
+2_5V_CG_MAIN        14C6< 39A3>
+2_5V_GPU            21A8< 21B6< 21D3< 21D7< 21D8<
                     39B3>
+2_5V_GPU_A2VDD      21D4< 21D7< 39C3>
+2_5V_GPU_PNLIO      21A5< 39C3>
+2_5V_INTREPID       9A8< 10D3< 10D5< 10D7< 10D8< 15D7<
                     16B8< 39D3>
+2_5V_MAIN           39D6>
+2_5V_MARVELL        28B8< 28C4<> 39B3>
+2_5V_MARVELL_AVDD   28C4< 39B3>
+2_5V_REG            30B6<
+2_5V_REG_F          30A7<>
+2_5V_SLEEP          39D6>
+2_5V_SLEEP_NECK1    19C4<> 39B3>
+2_5V_SLEEP_NECK2    21A3<> 39B3>
+2_8V_GPU_LVDS_LDO   21A6<>
+3V_ATI_OSC_SLEEP    18D2< 39C3>
+3V_ATI_SS           18B2< 39C3>
+3V_CG_PLL_MAIN      14C6< 39A3>
+3V_FW               29A3< 29D7<> 30B7<> 30D5< 39A3>
+3V_FW_AVDD          29C6< 39A3>
+3V_FW_AVDD_PORT0    29C6< 39A3>
+3V_FW_AVDD_PORT1    29C6< 39A3>
+3V_FW_AVDD_PORT2    29D6< 39A3>
+3V_FW_ESD           30B3<> 30B5< 30D2<> 39B3>
+3V_FW_ESD_ILIM      30D4< 39B3>
+3V_FW_ESD_R         30B6<
+3V_FW_UF            29D7<> 39A3>
+3V_GPU              12D1< 18B8< 18C5< 18C7< 18D6<
                     19C4< 19C5< 19C7< 19D8< 21A7< 21B1<
                     21B8< 39C3>
+3V_GPU_FLT          21B2< 39C3>
+3V_HALL_EFFECT      23B6<> 39B6> 40C4>
+3V_INTREPID_USB     14C3< 39D3>
+3V_LCD              22B4<> 39B6>
+3V_LCD_SW           22A4<> 39B6>
+3V_MAIN             23A7< 39D6>
+3V_MAIN_CONN        23A6<>
+3V_NEC_VDD          27D7< 27D7< 39A3>
+3V_PMU              39D6> 40A2>
+3V_PMU_AVCC         26B1< 31B6< 31D5<> 39C6>
+3V_PMU_ESR          33A2< 39C6>
+3V_PMU_RESET        31C7< 35A3<>
+3V_SLEEP            20D5< 20D8< 23A5< 39D6>
+3V_SLEEP_AUDIO      26D6<> 26D7<>
+3V_SLEEP_NECK       21A3<> 39B3>
+3V_SLP_OK_L         34B4<>
+3V_SLP_ON           34A5<>
+4_6V_BU             33A3<> 34B6< 39C6>
+4_85V_ESR           33A4< 39C6>
+4_85V_RAW           31B4< 33A4<> 39C6>
+5V_DDC_SLEEP        22D3<> 22D5<> 39B6> 40A2>
+5V_DDC_SLEEP_UF     22D6< 39B6>
+5V_HD_SLEEP         25D1<> 34A7<> 39C6>
+5V_INV_SW           22B2<> 39B6> 40D1>
+5V_INV_UF_SW        22B2<> 39B6>
+5V_MAIN             39D6>
+5V_MAIN_AUDIO       26D7<>
+5V_MAIN_AUDIO_0     26D7<>
+5V_MAIN_CONN        39B6>
+5V_SLEEP            23A4< 39D6>
+5V_SLEEP_MM3120     23A4<>
+5V_SOUND_SLEEP      39B6>
+5V_TPAD             23B7<>
+5V_TPAD_FB          23B6<>
+5V_TPAD_SLEEP       40C4>
+12_8V_INV           22B1<> 39B6> 40A2>
+24V_PBUS            39D6> 40B2>
+24V_PBUS_CONN       33A8<>
+ADAPTER             32D8<> 33B7< 39D6>
+ADAPTER_ILIM        33B6<> 39C6>
+ADAPTER_OR_BATT     33A5<> 39C6>
+ADAPTER_SENSE       32D5<> 39C6>
+ADAPTER_SW          32D6<> 39C6>
+BATT                39D6>
+BATT_14V_FUSE       32D1<> 39C6>
+BATT_24V_FUSE       32B1< 32D2<> 39C6>
+BATT_ISNS_P         24A5<>
+BATT_POS            32A4<> 39C6> 40C3>
+BATT_RSNS           32B2< 39C6>
+BATT_VSNS           32A4< 39C6>
+FAN1_PWR            26A4<>
+FAN2_PWR            26A3<>
+FW_FUSE             30D7<> 39A3>
+FW_PWR_CTRL         30B7<>
+FW_PWR_OR           29B8< 29D8<> 30D5<> 39A3>
+FW_PWR_OR_F         30B7<>
+FW_PWR_OR_GATE      30B8<>
+FW_PWR_OR_GATE_L    30B8<
+FW_PWR_PORTA        30B5< 39A3>
+FW_SW               30D5<> 39A3>
+FW_VP0              30C2<> 39A3>
+FW_VP1              30A3<> 39A3>
+GPU_MCLK            21C7< 21D4< 39C3>
+GPU_MEM             18A6<> 18B8< 21B4< 21B7< 21C6<
                     21C8< 21D2< 39C3>
+GPU_MEMCORE         21C5< 39C3>
+GPU_VDD15_NECK      19B5<> 39B3>
+GPU_VDD15_UF        19B5<> 19D4<> 39C3>
+HD_LOGIC_SLEEP      25C2<> 39C6>
+PBUS                39D6> 40B2>
+PPBATT_ISNS_N       24A4<> 40B4>
+VCC_CBUS_SW         17B1< 17B2< 17D2<> 39D3>
+VPP_CBUS_SW         17B1< 17B2< 17D2<> 39C3>
1V20_REF             32C7< 33C8< 39D1>
1V65_REF             32A5<
1_5V_2_5V_OK         36C5> 39B1>
1_5V_BOOST           36C6<> 39C1>
1_5V_BST             36C5<> 39C1>
1_5V_DH              36C5<> 39C1>
1_5V_DL              36B5<> 39C1>
1_5V_FB              36B5< 36B7< 39C1>
1_5V_ILIM            36C5<> 39C1>
1_5V_LX              36B5<> 39C1>
1_5V_SLEEP_EN_L      36C7<> 36D7<>
1_8V_SLEEP_PWREN_L   36A3<>
1_8V_SW              36A5<> 39A1>
1_8V_VFB             39A1>
2_5V_BOOST           36C4<> 39D1>
2_5V_BST             36C4<> 39D1>
2_5V_DH              36C4<> 39D1>
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```
2_5V_DL              36B4<> 39D1>
2_5V_ILIM            36C5<> 39C1>
2_5V_LX              36B4<> 39D1>
2_5V_SLEEP_PWREN_L   36C2<>
2_34V_REF            31A4<
3V_5V_OK             23A7<> 34B4<> 36A8<> 36D6<
3V_5V_OK_G           23B8<
3V_5V_OK_INV         36A8<>
3V_5V_OK_L           23B8<>
3V_BG                34C4<>
3V_BOOST             34C4<>
3V_BOOST_ESR         34D3<>
3V_ITH               34C4<>
3V_ITH_RC            34C3<
3V_PMU_VTAP          33B3<
3V_RSNS              34D2< 39D1>
3V_RUNSS             34C4<
3V_SLEEP_PWREN_L     34A3<>
3V_SNSM              34C4< 38A2>
3V_SNSP              34C4< 38A2>
3V_SW                34C4<> 39D1>
3V_TG                34D4<>
3V_VOSNS             34C4<>
5V_BG                34C5<>
5V_BOOST             34C5<>
5V_BOOST_ESR         34D6<>
5V_HD_PWREN          34A8<>
5V_ITH               34C5<>
5V_ITH_RC            34C6<
5V_RSNS              34D7< 39D1>
5V_RUNSS             34C5<
5V_SLEEP_PWREN       34A8<>
5V_SNSM              34C5< 38A2>
5V_SNSP              34C5< 38A2>
5V_SW                34C5<> 39D1>
5V_TG                34C5<>
5V_VOSNS             34C5<>
1625_BG              33C5<>
1625_BST             33C5<
1625_BST_ESR         33C5<>
1625_COMP            32D2< 33C6<
1625_DIV             33C8<
1625_ENABLE          33D7<>
1625_ENABLE_L        33D7<>
1625_EXTVCC          33D5<> 39D1>
1625_FCB             33C6<
1625_INTVCC          33C5<> 39D1>
1625_RUNSS           33C6<
1625_SGND            33B7<> 39D1>
1625_TG              33C5<>
1625_VFB             33B5<>
1625_VIN             33C6< 39D1>
1625_VSW             33C4<> 39D1>
1772_ACIN            32B5<
1772_ACOK_L          32B5<> 32C4<>
1772_BST             32B4<>
1772_BST_ESR         32C3<
1772_CCI             32B5<
1772_CCS             32B5<
1772_CCV             32B5<>
1772_CCV_RC          32B5<
1772_CELLS           32B4<
1772_CLS             32A4<
1772_CSIN            32B4<> 38A2>
1772_CSIP            32B4<> 38A2>
1772_CSSN            32C5< 38A2>
1772_CSSP            32C5< 38A2>
1772_DCIN            32B5<> 39C6>
1772_DHI             32B4<>
1772_DLO             32B4<>
1772_DLOV            32B4<> 39C6>
1772_GND             32A5<> 39C6>
1772_ICHG            32B5<>
1772_ICTL            32B5<>
1772_IINP            32B5<
1772_LDO             32C4<> 39C6>
1772_LX              32B4<> 39C6>
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NEC_USB_RSDP1     27C5<> 38B2>
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PMU_AC_IN      31B4<>
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PMU_BATT1_DET_L_PU  31B4<> 31D2<
PMU_BATT_DET_L   31A8<> 31B3< 31D2< 32A4<> 40C3>
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PMU_CHARGE_V     31C4<> 32B8<>
PMU_CHRG_BATT_S  31C4<> 32A8<>
PMU_CLK          14C2<> 31C4<>
PMU_CNVSS        31B6< 31C7<
PMU_CPU_RESET_L  4A2< 6C3<> 31C4<>
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PMU_CUSTOM_RESET_L  31A7<> 31B8<
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PMU_FROM_INT     14C2<> 31C4<>
PMU_I2C_CLK      31B4<> 31C2<
PMU_I2C_DATA     31B4<> 31C2<
PMU_INT_L        14B5<> 14B7< 31B6<>
PMU_INT_NMI      14B5<> 14B7< 31D4<>
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PMU_NMI_L        31C2< 31C4<>
PMU_NUMLOCK_LED_L  31C6<>
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PMU_PME_L        14B5<> 27B8< 31B2< 31C4<>
PMU_POWERUP_OK   31B4<> 31D2<
PMU_POWER_UP_L   30D8<> 31C6<> 31D7< 34B8<
PMU_RSQ_L        14B7< 14C2> 31C4<>
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PMU_SELECT       31C6<>
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PMU_SLEEP_LED_L  23B3<> 31C4<>
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PP3V3_SI_PVCC1   20C7< 39B3>
PP3V3_SI_PVCC2   20C5< 39B3>
PP3V3_SI_VCC1    20D7< 39B3>
PP3V3_SI_VCC2    20C5< 39B3>
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RAM_DQM_B<7>     10C2<> 11A3<> 37A5>
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RAM_MUXSEL_L     10A3< 10A5< 10B5<> 10B7<> 37A5>
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RAM_WE_L         9A4< 11B3<> 11B8<> 37A5>
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	C
SCALE: NONE	SHT 43 OF 45	

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*** Part Cross-Reference for the entire design ***

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D11   DIODE_SCHOT 33
D12   DIODE_DGAL_6P 30
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D14   DIODE_SCHOT_3P2 29
D15   DIODE_DGAL_6P 30
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D17   DIODE_SCHOT 33
D18   DIODE    33
D19   DIODE_SCHOT 33
D20   DIODE_SCHOT 29
D21   DIODE_SCHOT 22
D22   DIODE_SCHOT 34
D23   DIODE_SCHOT 36
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D34   DIODE_SCHOT 34
D35   DIODE_SCHOT 5
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DP8   DPAK3P   31
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FL2   FILTER_LC 22
FL3   FILTER_LC 22
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G2    OSC      18
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J2    CON_4RT_WR1B 26
J3    CON_F14RT_S2MT_SM 25
J4    CON_4RT_WR1B 26
J5    CON_12   35
J6    CON_F30RT_S2MT_SM 22
J7    CON_4RT_WR1B 22
J8    CON_F16ST_S_SMA 26
J9    CON_M80ST_D4MT_SM 17
J10   CON_M5OSH_5MM 25
J11   CON_F14RT_S2MT_SM 33
J12   CON_M40ST_D4MT_SM 26
J13   CON_M5OSH_5MM 25
J14   CON_F30RT_T4MT_TH1 22
J15   CON_F5MT_MINIDIN_TH 22
J16   CON_10STSM_5087 26
J17   CON_RJ45_SHORT_4MT_TH 28
J18   CON_M8RT_S_SH 32
J19   CON_F20SMT_DDRDIMM_SM1 11
J20   CON_M80ST_D2MT_SM3 25
J21   CON_F14RT_S2MT_SM 23
J22   CON_F20SMT_DDRDIMM_SM2 11
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J26   CON_F9MT_13948_S6MT_SMA 30
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XW14	SHORT	24
XW15	SHORT	35
XW16	SHORT	24
XW17	SHORT	24
XW18	SHORT	24
XW19	SHORT	32
XW20	SHORT	19
XW21	SHORT	19
XW22	SHORT	19
XW23	SHORT	19
XW24	SHORT	19
XW27	SHORT	21
XW28	SHORT	21
XW29	SHORT	21
XW30	SHORT	21
XW31	SHORT	5
Y1	CRYSTAL	14
Y3	CRYSTAL	28
Y4	CRYSTAL	23
Y5	CRYSTAL	27
Y6	CRYSTAL	31
Y7	CRYSTAL_4PIN	31
ZT1	HOLE_VIA	4
ZT2	MTGHOLE	4
ZT3	HOLE_VIA	4
ZT4	MTGHOLE	4
ZT5	MTGHOLE	4
ZT6	MTGHOLE	4
ZT7	HOLE_VIA	4
ZT8	HOLE_VIA	4
ZT9	HOLE_VIA	4
ZT10	MTGHOLE	4
ZT11	MTGHOLE	4
ZT12	HOLE_VIA	4
ZT13	HOLE_VIA	4
ZT14	HOLE_VIA	4
ZT15	HOLE_VIA	4
ZT16	MTGHOLE	4
ZT17	HOLE_VIA	4
ZT18	HOLE_VIA	4
ZT19	HOLE_VIA	4
ZT20	HOLE_VIA	4
ZT21	HOLE_VIA	4
ZT22	HOLE_VIA	4
ZT23	HOLE_VIA	4
ZT24	HOLE_VIA	4
ZT25	HOLE_VIA	4
ZT26	HOLE_VIA	4
ZT27	HOLE_VIA	4
ZT28	HOLE_VIA	4
ZT29	HOLE_VIA	4
ZT30	HOLE_VIA	4
ZT31	HOLE_VIA	4
ZT32	HOLE_VIA	4
ZT33	HOLE_VIA	4
ZT34	HOLE_VIA	4
ZT35	HOLE_VIA	4
ZT36	HOLE_VIA	4
ZT37	HOLE_VIA	4
ZT38	HOLE_VIA	4
ZT39	HOLE_VIA	4
ZT40	HOLE_VIA	4
ZT41	HOLE_VIA	4
ZT42	HOLE_VIA	4
ZT43	HOLE_VIA	4
ZT44	HOLE_VIA	4
ZT45	HOLE_VIA	4
ZT46	HOLE_VIA	4
ZT47	HOLE_VIA	4
ZT48	HOLE_VIA	4
ZT49	HOLE_VIA	4
ZT50	HOLE_VIA	4
ZT51	HOLE_VIA	4
ZT52	HOLE_VIA	4
ZT53	HOLE_VIA	4
ZT54	HOLE_VIA	4
ZT55	HOLE_VIA	4
ZT56	HOLE_VIA	4
ZT57	HOLE_VIA	4
ZT58	HOLE_VIA	4
ZT59	HOLE_VIA	4
ZT60	HOLE_VIA	4
ZT61	HOLE_VIA	4
ZT62	HOLE_VIA	4
ZT63	HOLE_VIA	4
ZT64	HOLE_VIA	4
ZT65	HOLE_VIA	4
ZT66	HOLE_VIA	4
ZT67	HOLE_VIA	4
ZT68	HOLE_VIA	4
ZT69	HOLE_VIA	4
ZT70	HOLE_VIA	4
ZT71	HOLE_VIA	4
ZT72	HOLE_VIA	4
ZT73	HOLE_VIA	4
ZT74	HOLE_VIA	4
ZT75	HOLE_VIA	4
ZT76	HOLE_VIA	4
ZT77	HOLE_VIA	4
ZT78	HOLE_VIA	4
ZT79	HOLE_VIA	4
ZT80	HOLE_VIA	4
ZT81	HOLE_VIA	4
ZT82	HOLE_VIA	4
ZT83	MYOHOLE	4