

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
B		357142	PRODUCTION RELEASED	12/21/04	?

PAGE	CONTENTS
1	TITLE PAGE AND CONTENTS
2	SYSTEM BLOCK DIAGRAM
3	POWER BLOCK DIAGRAM
4	PCB NOTES AND HOLES
5	MPC7450 MAXBUS INTERFACE
6	MPC7450 DATA
7	CPU PLL AND CONFIGURATION STRAPS
8	INTREPID MAXBUS AND BOOT STRAPS
9	INTREPID MEMORY INTERFACE / BOOT ROM
10	DDR MEMORY MUXES
11	200PIN DDR MEMORY SODIMM CONNECTORS
12	INTREPID AGP 4X/PCI
13	INTREPID ENET/FW/UATA/EIDE INTERFACES
14	INTREPID GPIO/SERIAL/USB INTERFACES/SSCG
15	INTREPID POWER RAILS
16	INTREPID DECOUPLING
17	CARDBUS CONTROLLER (PCI1510)
18	M11 AGP & CLOCKS
19	M11 LVDS/TMDS/VGA/GPIO & GPU VCORE
20	SIL178 DUAL TMDS TRANSMITTER
21	M11 ANALOG, POWER, GND

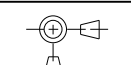

PAGE	CONTENTS
22	VIDEO CONNECTORS - INVERTER, DVI, S-VIDEO DUAL-CHANNEL LVDS
23	LMU, LIGHT SENSOR, BOOTBANGER, SLEEP LED SPIDEY - KBD,TPAD,HALL EFFECT,PWR BUTTON
24	MMM, BATTERY CURRENT SENSE
25	INTERNAL CONNECTORS - DVD, CARDSLOT, HARD DRIVE, LEFT USB/BLUETOOTH
26	FAN CONTROLLER, MODEM, SOUND SERIAL DEBUG (JOLLY ROGER, PWR/NMI/RESET)
27	USB 2.0
28	MARVELL GIGABIT ETHERNET PHY
29	FIREWIRE A/B PHY
30	FIREWIRE A/B CONNECTORS, PORT POWER LIMITER
31	PMU (POWER MANAGEMENT UNIT)
32	BATTERY CHARGER AND CONNECTOR
33	12.8V SYSTEM POWER SUPPLY / PMU POWER SUPPLY
34	3.3V / 5V SYSTEM POWER SUPPLIES
35	CPU CORE VOLTAGE POWER SUPPLY
36	1.5V/ 1.8V / 2.5V SYSTEM POWER SUPPLIES
37	SIGNAL CONSTRAINTS (1 OF 3) - DIGITAL/CLK
38	SIGNAL CONSTRAINTS (2 OF 3) - DIGITAL/DIFF
39	SIGNAL CONSTRAINTS (3 OF 3) - POWER NETS
40	FUNCTIONAL TEST POINTS
41	REVISION HISTORY (1 OF 1)
42-45	SCHEMATIC CREF AND NETLIST REPORTS

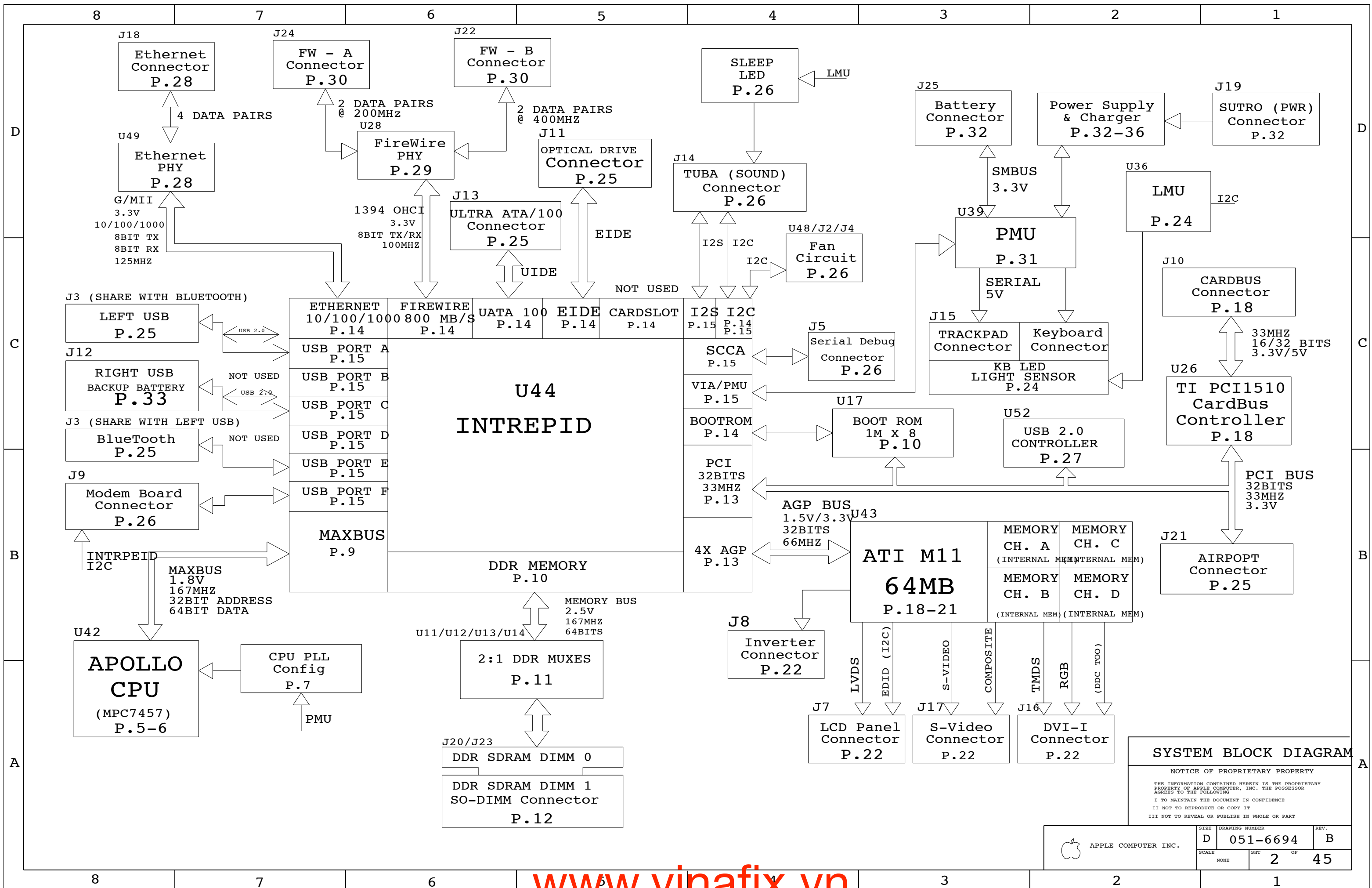
SCHEM, MLB, PB17 "

12/21/2004

BOM OPTIONS	STUFF	NO STUFF
D3_HOT		✓
D3_COLD	✓	
GPU_SS	✓	
GPU_SWITCH	✓	
SERIAL_DEBUG		✓
VCORE_OFFSET	✓	
1_8V_MAXBUS	✓	
1_5V_MAXBUS		✓
NEC_USB	✓	
INTREPID_USB		✓
BBANG		✓
NO_BBANG		✓
ATI_MEMIO_HI	✓	
ATI_MEMIO_LO		✓
SSCG		✓
NO_SSCG	✓	
5V_HD_LOGIC	✓	
3V_HD_LOGIC		✓
EXT_TMDS	✓	
INT_TMDS		✓
MMM	✓	
INT_CLK	✓	
EXT_CLK		✓

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6694	1	SCHEM,MLB,PB17	SCH1	
820-1688	1	PCBF,MLB,PB17	PCB1	

<p style="text-align: center;">DIMENSIONS ARE IN MILLIMETERS</p> <p>XX : _____</p> <p>X.XX : _____</p> <p>X.XXX : _____</p> <p>ANGLES : _____</p> <p style="text-align: center;">DO NOT SCALE DRAWING</p> <p style="text-align: center;">  THIRD ANGLE PROJECTION </p>	METRIC	<p style="text-align: center;">  Apple Computer Inc. </p> <p style="text-align: center;">NOTICE OF PROPRIETARY PROPERTY</p> <p style="text-align: center;"> <small>THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</small> <small>I TO MAINTAIN THE DOCUMENT IN CONFIDENCE</small> <small>II NOT TO REPRODUCE OR COPY IT</small> <small>III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</small> </p> <p style="text-align: center; font-size: 1.2em;">SCHEM, MLB, PB17 "</p> <p style="text-align: center;">DRAWING NUMBER 051-6694 REV. B</p> <p style="text-align: right; font-size: 0.8em;">SHT 1 OF 45</p>
DRAFTER _____ ENG APPD _____ QA APPD _____ RELEASE _____	DESIGN CK _____ MFG APPD _____ DESIGNER _____ SCALE NONE	MATERIAL/FINISH NOTED AS APPLICABLE SIZE D

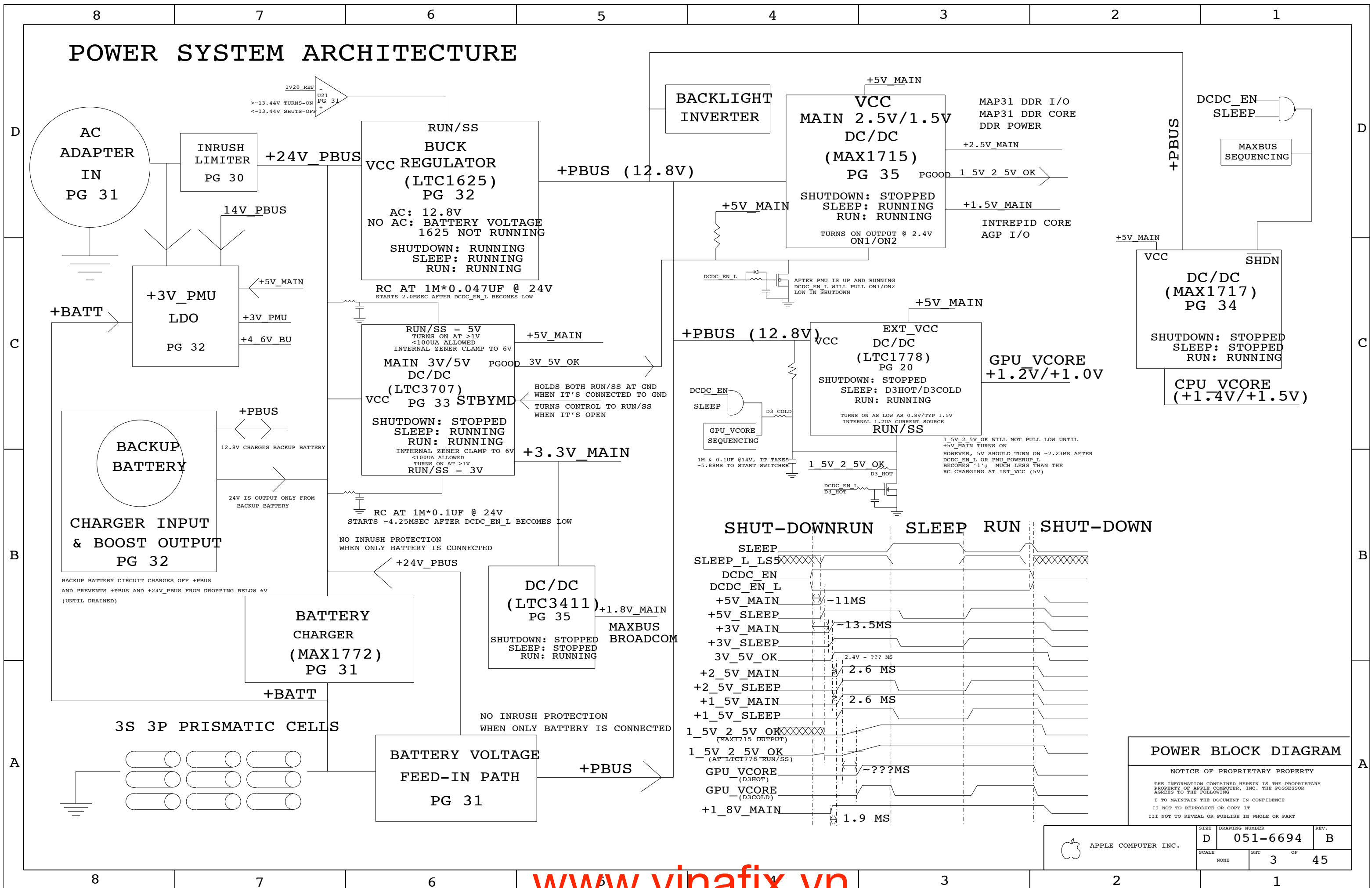


SYSTEM BLOCK DIAGRAM

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	D	051-6694	B
SCALE	NONE	SHT	2 OF 45

POWER SYSTEM ARCHITECTURE



POWER BLOCK DIAGRAM

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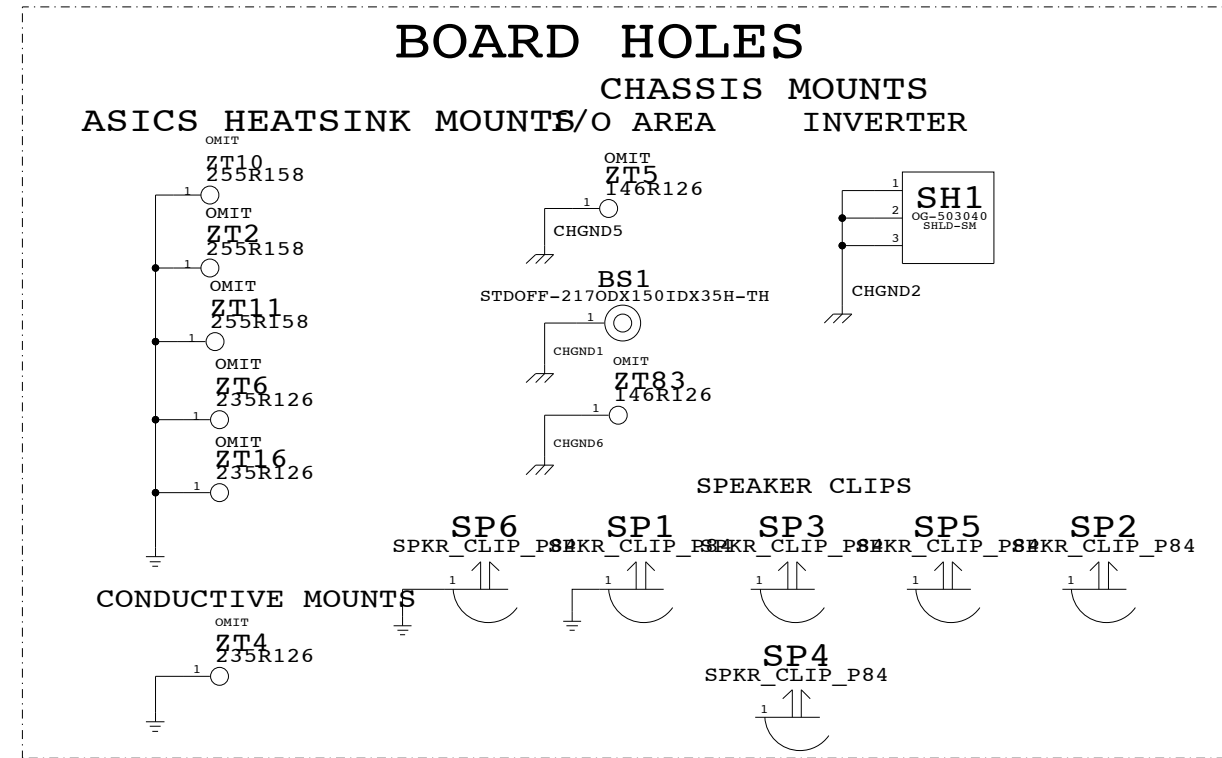
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6694	B
SCALE	SHT	OF	
NONE	3	45	

PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
 1/2 OZ CU THICKNESS: 0.7 MILS
 1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
 DIELECTRIC: FR-4
 LAYER COUNT: 12
 SIGNAL TRACE WIDTH: 4 MILS
 SIGNAL TRACE SPACING: 4 MILS
 PREPREG THICKNESS: 2-3 MILS

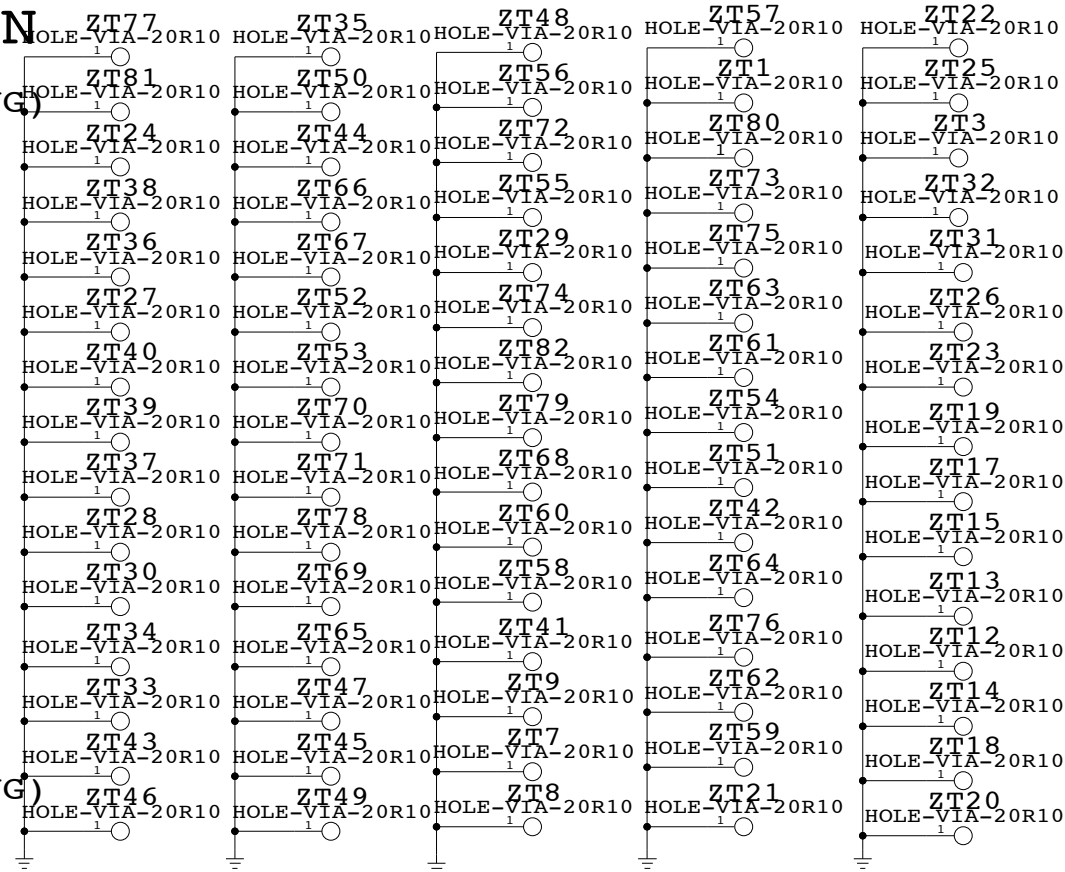
SEE PCB CAD FILES FOR MORE SPECIFIC INFO.



BOARD STACK-UP AND CONSTRUCTION

Layer	Material	Thickness	Notes
1	SIGNAL	1/3 OZ + COPPER PLATING	20R10 TH VIA OR VIA IN PAD
2	PREPREG	3MIL	GROUND (1/2 OZ)
3	LAMINATE	4MIL	SIGNAL (1/2 OZ)
4	PREPREG	3MIL	SIGNAL (1/2 OZ)
5	LAMINATE	4MIL	GROUND (1/2 OZ)
6	PREPREG	2MIL	CUT POWER PLANE (1 OZ)
7	LAMINATE	3MIL	CUT POWER PLANE (1 OZ)
8	PREPREG	2MIL	GROUND (1/2 OZ)
9	LAMINATE	4MIL	SIGNAL (1/2 OZ)
10	PREPREG	3MIL	SIGNAL (1/2 OZ)
11	LAMINATE	4MIL	GROUND (1/2 OZ)
12	PREPREG	3MIL	SIGNAL (1/3 OZ + COPPER PLATING)

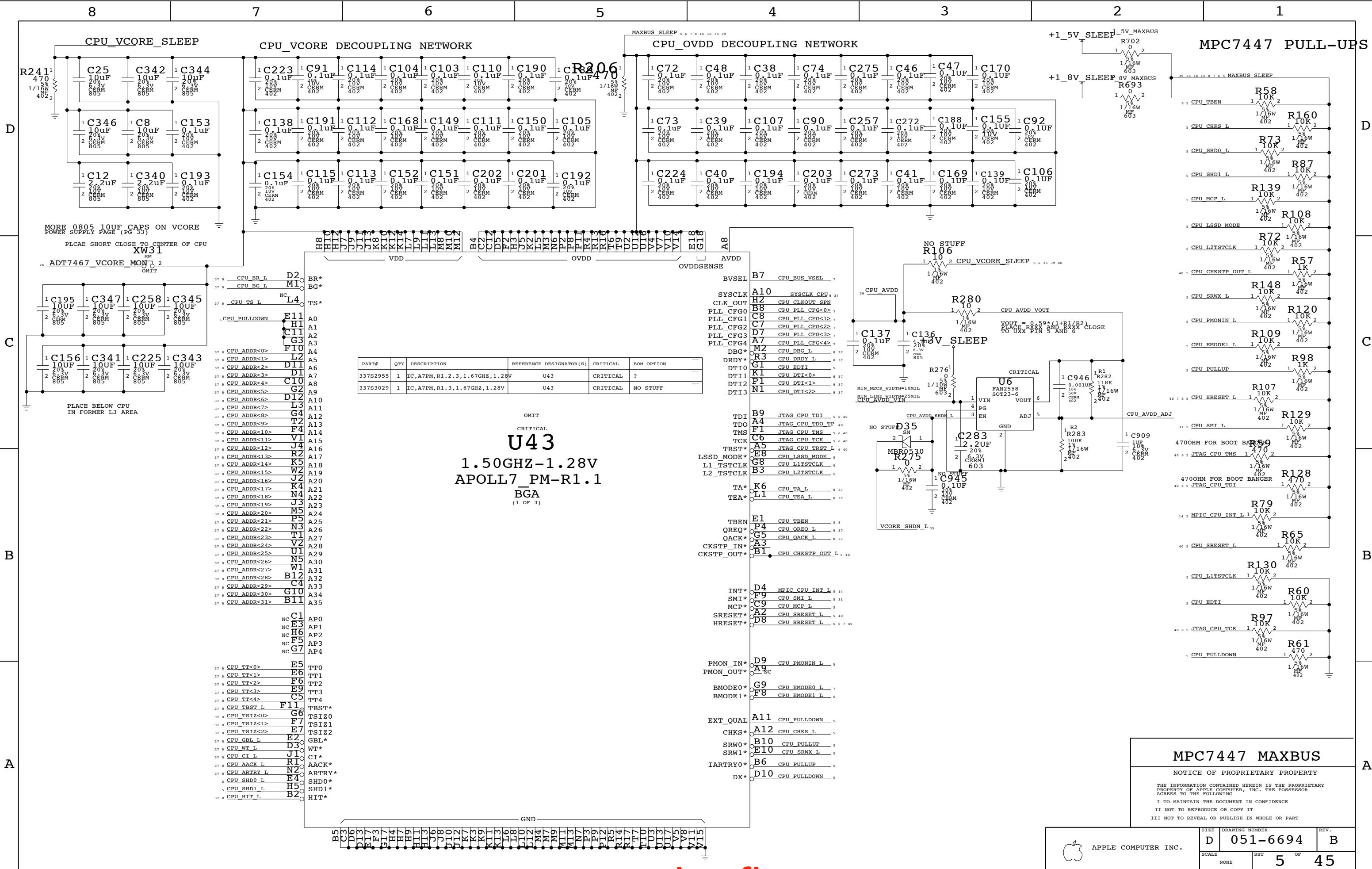
GROUND VIAS



BOARD INFORMATION

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	SCALE	NONE	SHT	4	OF	45



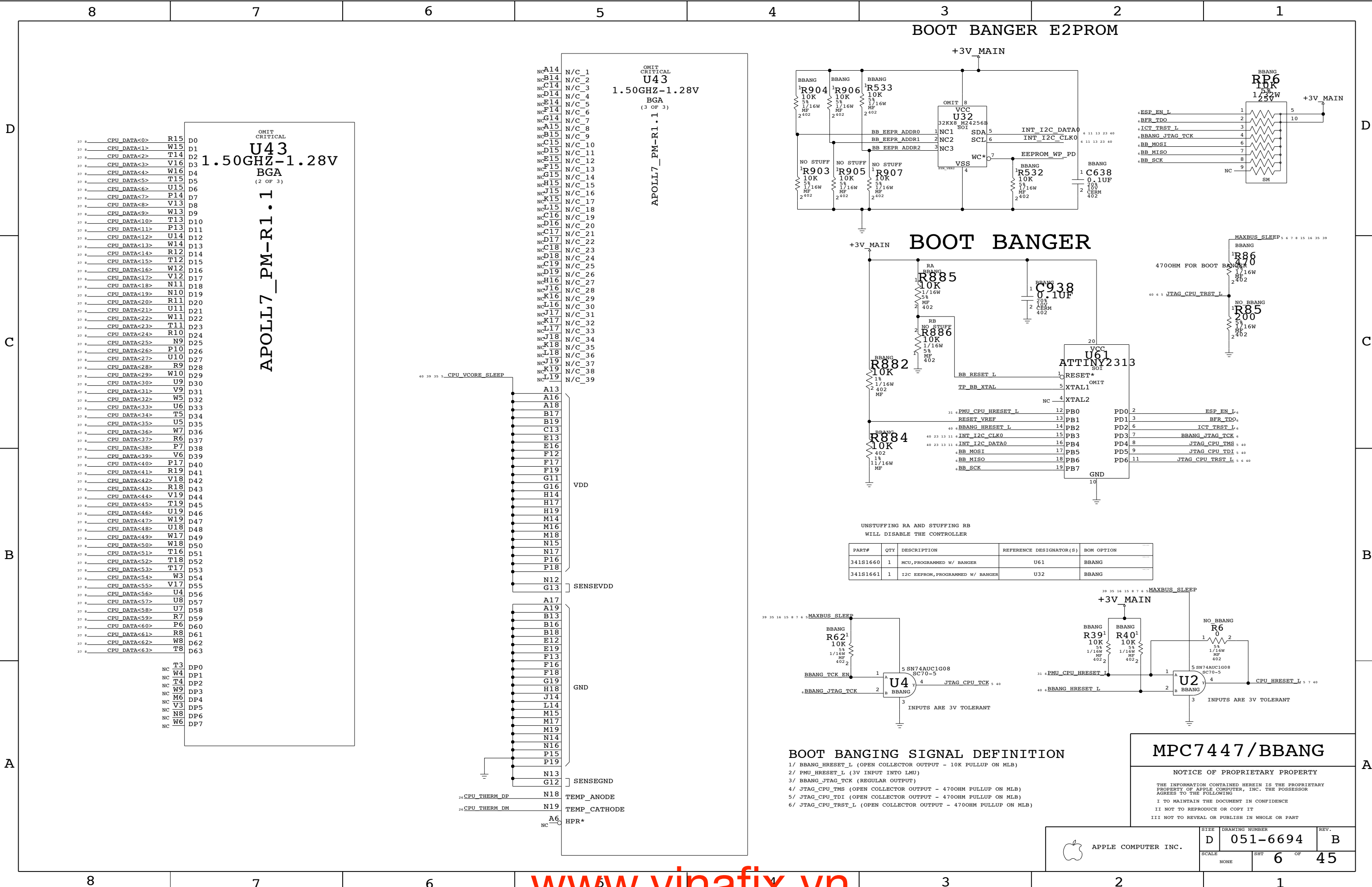
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S2955	1	IC, A7PM, R1.2.3, 1.67GHZ, 1.28V	U43	CRITICAL	?
337S3029	1	IC, A7PM, R1.3, 1.67GHZ, 1.28V	U43	CRITICAL	NO STUFF

OMIT
U43
 1.50GHZ-1.28V
 APOLL7_PM-R1.1
 BGA
 (1 OF 3)

- 37 CPU_BR_L D2 BR*
- 37 CPU_BG_L M1 BG*
- 37 CPU_TS_L L4 TS*
- 37 CPU_PULLDOWN E11 HI*
- 37 CPU_ADDR<0> F10 A0
- 37 CPU_ADDR<1> L2 A1
- 37 CPU_ADDR<2> D11 A2
- 37 CPU_ADDR<3> D1 A3
- 37 CPU_ADDR<4> C10 A4
- 37 CPU_ADDR<5> G2 A5
- 37 CPU_ADDR<6> D12 A6
- 37 CPU_ADDR<7> L3 A7
- 37 CPU_ADDR<8> G4 A8
- 37 CPU_ADDR<9> T2 A9
- 37 CPU_ADDR<10> F4 A10
- 37 CPU_ADDR<11> V1 A11
- 37 CPU_ADDR<12> J4 A12
- 37 CPU_ADDR<13> R2 A13
- 37 CPU_ADDR<14> K5 A14
- 37 CPU_ADDR<15> W2 A15
- 37 CPU_ADDR<16> J2 A16
- 37 CPU_ADDR<17> K4 A17
- 37 CPU_ADDR<18> N4 A18
- 37 CPU_ADDR<19> J3 A19
- 37 CPU_ADDR<20> M5 A20
- 37 CPU_ADDR<21> P5 A21
- 37 CPU_ADDR<22> N3 A22
- 37 CPU_ADDR<23> T1 A23
- 37 CPU_ADDR<24> V2 A24
- 37 CPU_ADDR<25> U1 A25
- 37 CPU_ADDR<26> N5 A26
- 37 CPU_ADDR<27> W1 A27
- 37 CPU_ADDR<28> B12 A28
- 37 CPU_ADDR<29> C4 A29
- 37 CPU_ADDR<30> G10 A30
- 37 CPU_ADDR<31> B11 A31
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- 37 CPU_ADDR<96> A96
- 37 CPU_ADDR<97> A97
- 37 CPU_ADDR<98> A98
- 37 CPU_ADDR<99> A99
- 37 CPU_ADDR<100> A100

MPC7447 MAXBUS
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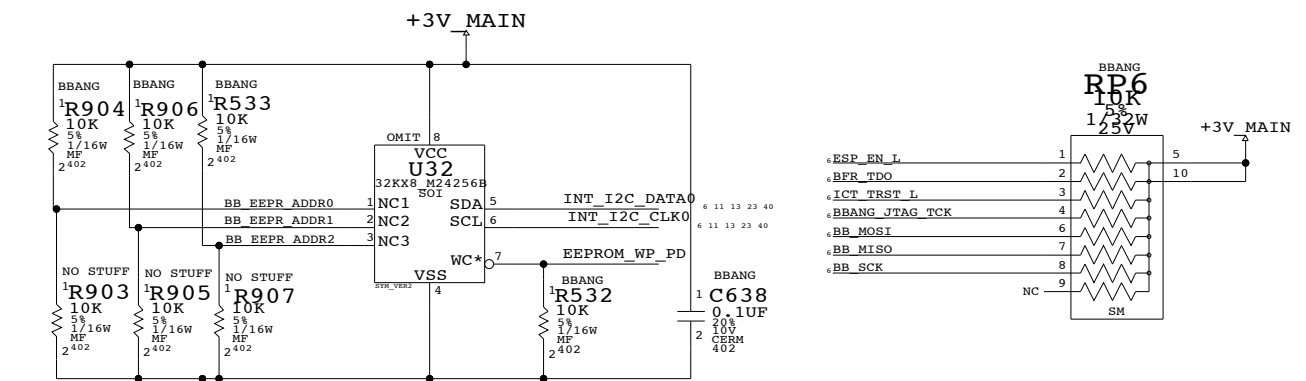
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6694	REV. B
	SCALE NONE	SHEET 5	OF 45



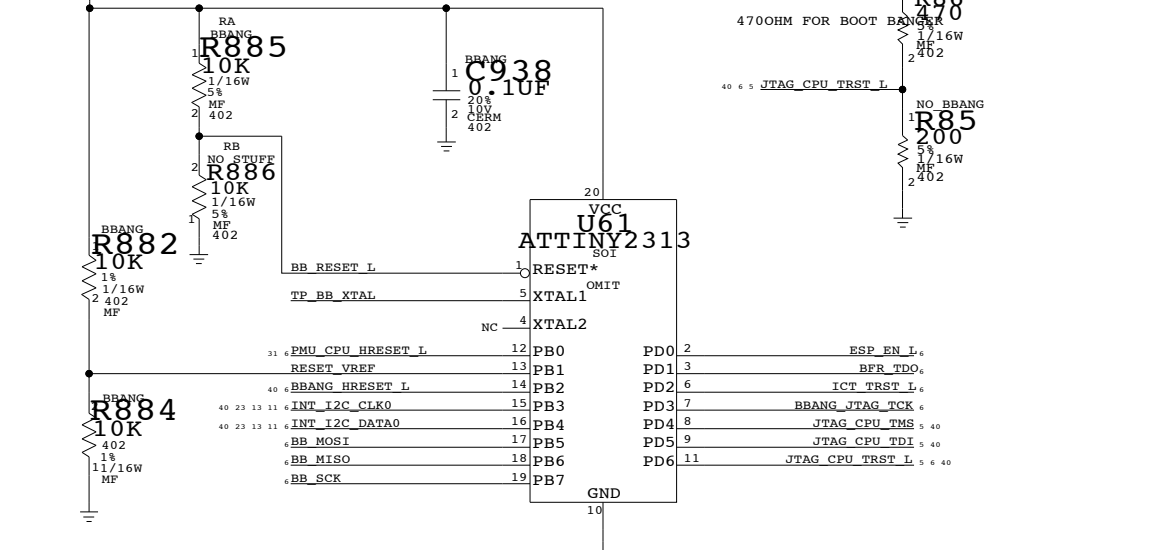
OMIT CRITICAL
U43
 1.50GHZ-1.28V
 BGA
 (2 OF 3)
APOLL7_PM-R1.1

OMIT CRITICAL
U43
 1.50GHZ-1.28V
 BGA
 (3 OF 3)
APOLL7_PM-R1.1

BOOT BANGER E2PROM

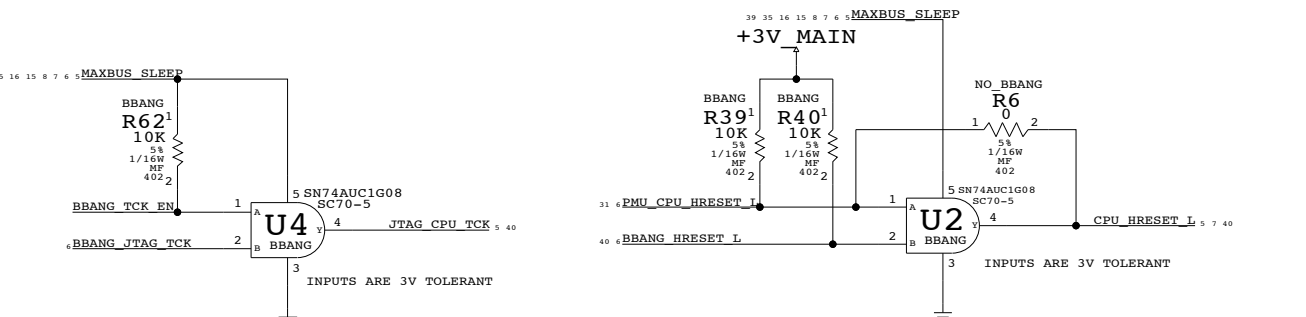


BOOT BANGER



UNSTUFFING RA AND STUFFING RB
 WILL DISABLE THE CONTROLLER

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1660	1	MCU, PROGRAMMED W/ BANGER	U61	BBANG
341S1661	1	I2C EEPROM, PROGRAMMED W/ BANGER	U32	BBANG



BOOT BANGING SIGNAL DEFINITION

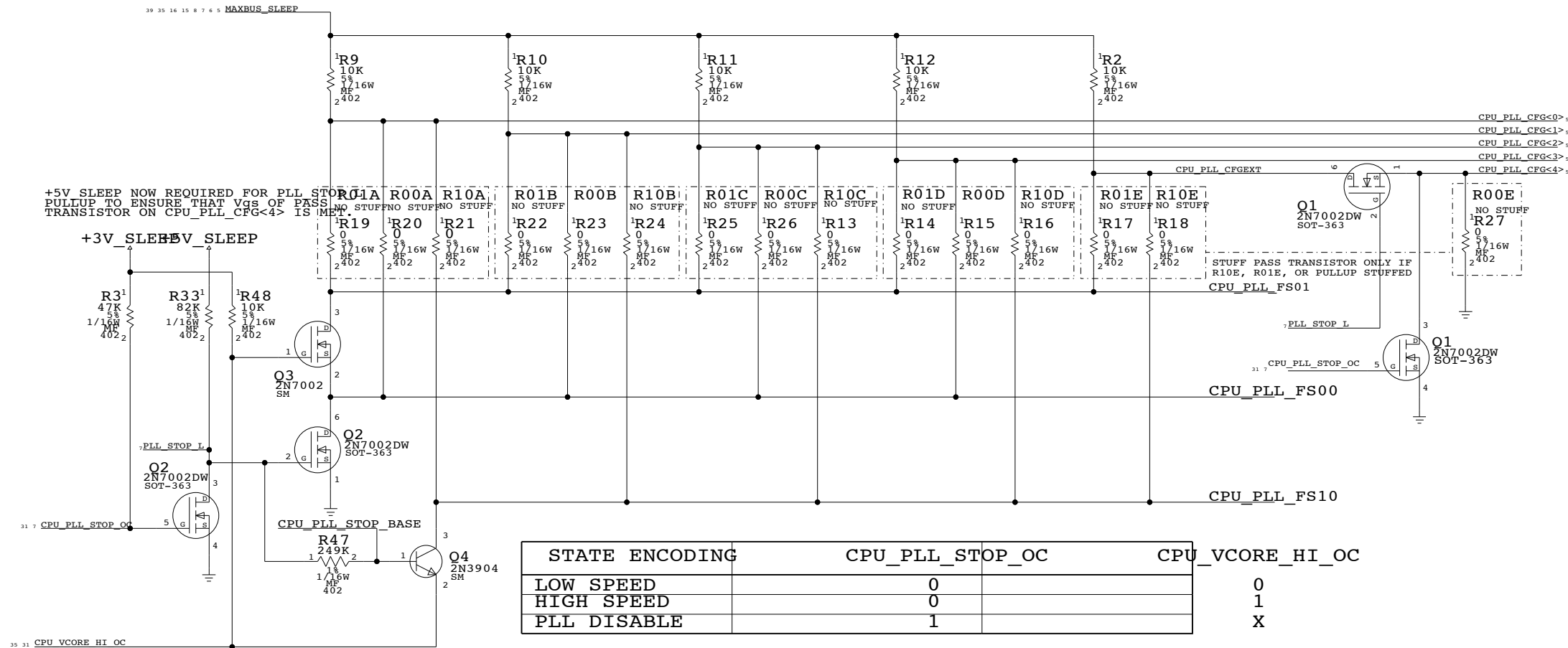
- 1/ BBANG_HRESET_L (OPEN COLLECTOR OUTPUT - 10K PULLUP ON MLB)
- 2/ PMU_HRESET_L (3V INPUT INTO LMU)
- 3/ BBANG_JTAG_TCK (REGULAR OUTPUT)
- 4/ JTAG_CPU_TMS (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
- 5/ JTAG_CPU_TDI (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
- 6/ JTAG_CPU_TRST_L (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)

MPC7447/BBANG

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	D	051-6694	B
SCALE	NONE	SHT	6 OF 45

CPU PLL CONFIG CIRCUITRY



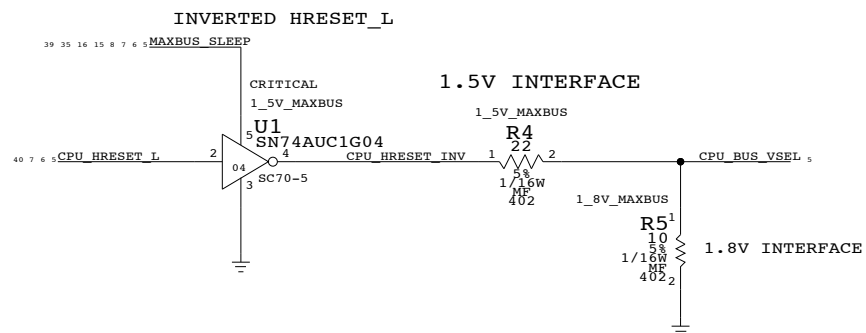
CPU FREQUENCY CONFIGURATION

APOLLO 7

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY)		CPU_PLL_CFG			
	167MHZ	133MHZ	4	0123	HEX	
0.0X	PLL OFF		0	1111	0F	
1.0X	PLL BYPASS		0	0011	03	
2.0X	333	267	0	0100	04	
3.0X	500	400	0	1000	08	
4.0X	667	533	0	1010	0A	
5.0X	833	667	0	1011	0B	
5.5X	917	733	0	1001	09	
6.0X	1000	800	0	1101	0D	
6.5X	1083	867	0	0101	05	
7.0X	1167	933	0	0010	02	
7.5X	1250	1000	0	0001	01	
8.0X	1333	1067	0	1100	0C	
8.5X	1417	1133	0	0110	06	
9.0X	1500	1200	1	0111	17	
9.5X	1583	1267	0	0111	07	
10.0X	1667	1333	1	1010	1A	
10.5X	1750	1400	1	1000	18	
11.0X	1833	1467	1	1001	19	
11.5X	1917	1533	0	0000	00	
12.0X	2000	1600	1	1011	1B	
12.5X	2083	1667	1	1111	1F	
13.0X	2167	1733	1	0101	15	
13.5X	2250	1800	0	1110	0E	
14.0X	2333	1867	1	1100	1C	
15.0X	2500	2000	1	0001	11	
16.0X	2667	2133	1	1101	1D	
17.0X	2833	2267	1	0000	10	
18.0X	3000	2400	1	0010	12	
20.0X	3333	2667	1	0011	13	
21.0X	3500	2800	1	0100	14	
24.0X	4000	3200	1	0110	16	
28.0X	4667	3733	1	1110	1E	

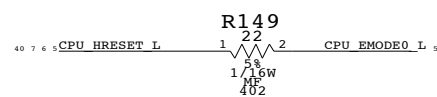
CPU CONFIGURATION

MAXBUS VSEL



DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L
NEED TO CHARACTERIZE

BUSTYPE SELECT



APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
	CPU_HRESET_L	2.5V INTERFACE
CPU_BUS_VSEL (PROCESSOR)	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

CPU CONFIGURATION

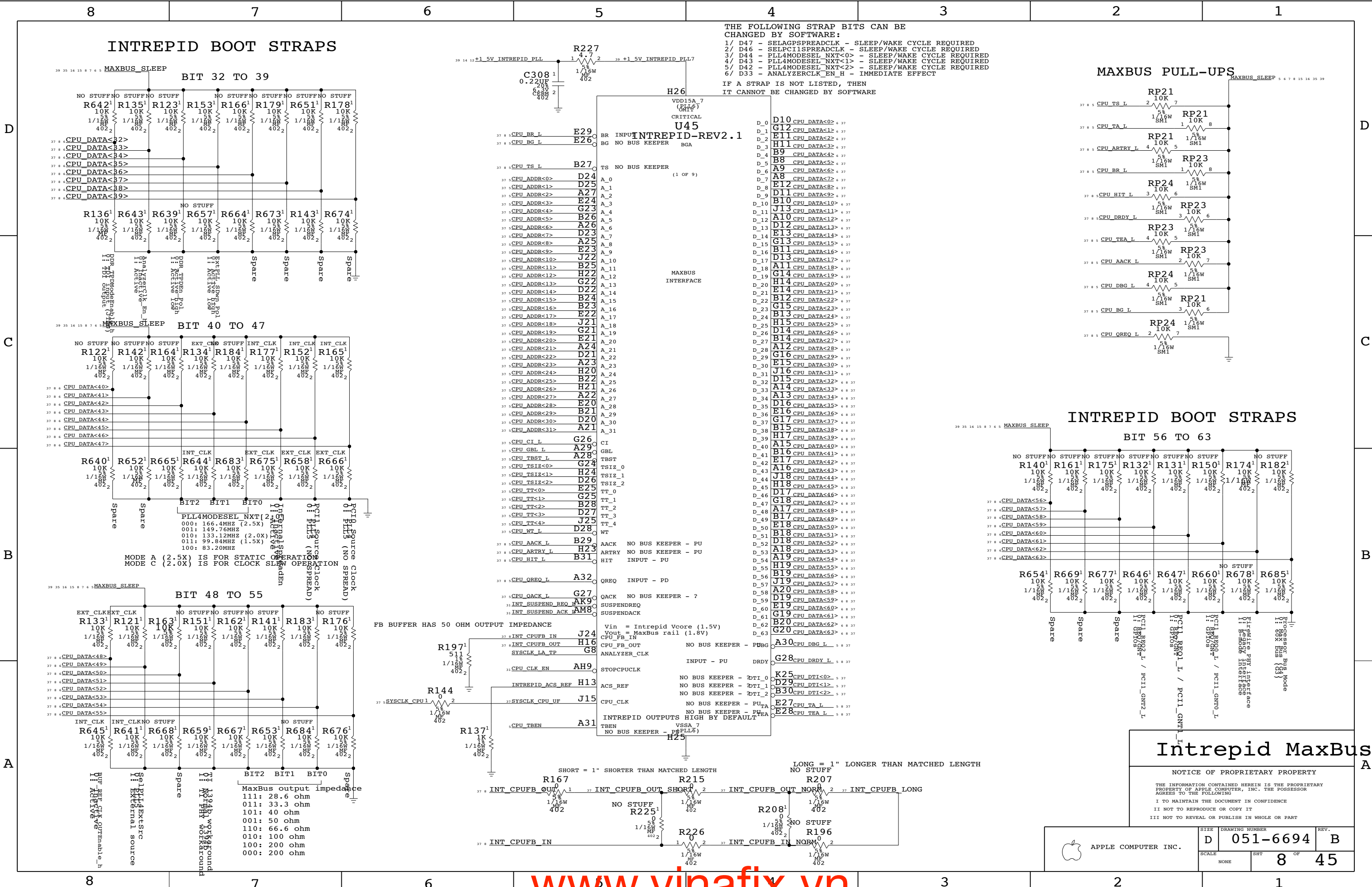
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SCALE	NONE	SHT	7 OF 45

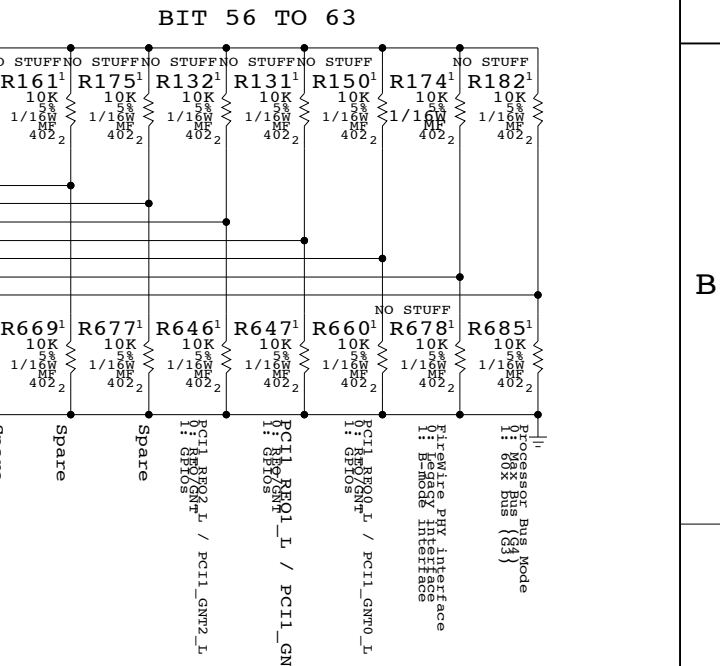
INTREPID BOOT STRAPS

THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:
1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
2/ D46 - SELPCI1SPREADCLK - SLEEP/WAKE CYCLE REQUIRED
3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT
IF A STRAP IS NOT LISTED, THEN IT CANNOT BE CHANGED BY SOFTWARE

MAXBUS PULL-UPS

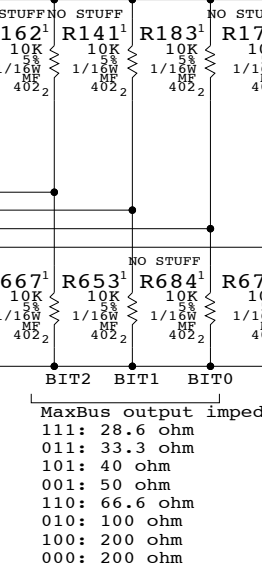


INTREPID BOOT STRAPS

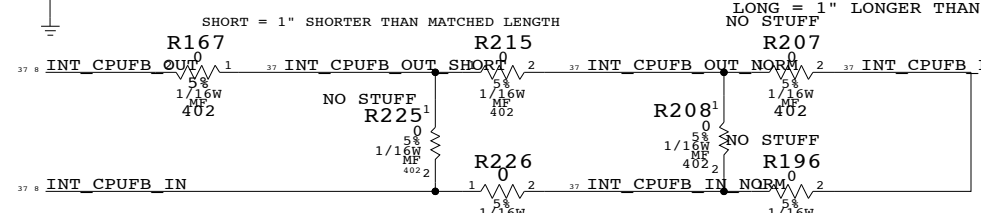


MODE A (2.5X) IS FOR STATIC OPERATION
MODE B (2.0X) IS FOR CLOCK SLEW OPERATION

BIT 48 TO 55



MaxBus output impedance
111: 28.6 ohm
011: 33.3 ohm
101: 40 ohm
001: 50 ohm
110: 66.6 ohm
010: 100 ohm
100: 200 ohm
000: 200 ohm



Intrepid MaxBus

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SIZE	D	DRAWING NUMBER	051-6694	REV.	B
SCALE	NONE	SHT	8	OF	45

SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

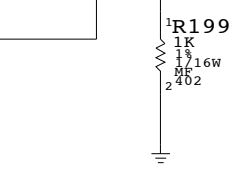
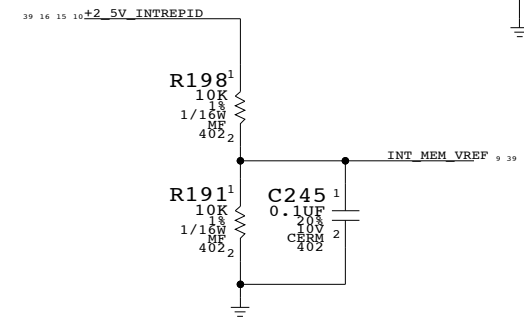
PINS ARE SWAPABLE FOR RPAKS

MEM_DATA<0>	AK32	DDR_DATA_0	DDR_A_0	H35	MEM_ADDR<0>
MEM_DATA<1>	AK33	DDR_DATA_1	DDR_A_1	G35	MEM_ADDR<1>
MEM_DATA<2>	AK31	DDR_DATA_2	DDR_A_2	G36	MEM_ADDR<2>
MEM_DATA<3>	AK35	DDR_DATA_3	DDR_A_3	F36	MEM_ADDR<3>
MEM_DATA<4>	AK36	DDR_DATA_4	DDR_A_4	F35	MEM_ADDR<4>
MEM_DATA<5>	AJ32	DDR_DATA_5	DDR_A_5	E35	MEM_ADDR<5>
MEM_DATA<6>	AJ36	DDR_DATA_6	DDR_A_6	E36	MEM_ADDR<6>
MEM_DATA<7>	AJ36	DDR_DATA_7	DDR_A_7	G32	MEM_ADDR<7>
MEM_DATA<8>	AG33	DDR_DATA_8	DDR_A_8	D36	MEM_ADDR<8>
MEM_DATA<9>	AG35	DDR_DATA_9	DDR_A_9	H36	MEM_ADDR<9>
MEM_DATA<10>	AH35	DDR_DATA_10	DDR_A_10	G33	MEM_ADDR<10>
MEM_DATA<11>	AH36	DDR_DATA_11	DDR_A_11	H33	MEM_ADDR<11>
MEM_DATA<12>	AH36	DDR_DATA_12	DDR_A_12	D35	MEM_ADDR<12>
MEM_DATA<13>	AH32	DDR_DATA_13	DDR_BA_0	L30	MEM_BA<0>
MEM_DATA<14>	AG32	DDR_DATA_14	DDR_BA_1	M29	MEM_BA<1>
MEM_DATA<15>	AG31	DDR_DATA_15	DDRC_S_0	AN34	MEM_CS_L<0>
MEM_DATA<16>	AE32	DDR_DATA_16	DDRC_S_1	AN36	MEM_CS_L<1>
MEM_DATA<17>	AF35	DDR_DATA_17	DDRC_S_2	AL35	MEM_CS_L<2>
MEM_DATA<18>	AF36	DDR_DATA_18	DDRC_S_3	AL33	MEM_CS_L<3>
MEM_DATA<19>	AE36	DDR_DATA_19	DDR_DQS_0	AJ31	MEM_DQS<0>
MEM_DATA<20>	AE35	DDR_DATA_20	DDR_DQS_1	AH31	MEM_DQS<1>
MEM_DATA<21>	AE33	DDR_DATA_21	DDR_DQS_2	AD32	MEM_DQS<2>
MEM_DATA<22>	AD36	DDR_DATA_22	DDR_DQS_3	AB30	MEM_DQS<3>
MEM_DATA<23>	AD35	DDR_DATA_23	DDR_DQS_4	V30	MEM_DQS<4>
MEM_DATA<24>	AA36	DDR_DATA_24	DDR_DQS_5	P32	MEM_DQS<5>
MEM_DATA<25>	AA35	DDR_DATA_25	DDR_DQS_6	N29	MEM_DQS<6>
MEM_DATA<26>	AA33	DDR_DATA_26	DDR_DQS_7	L32	MEM_DQS<7>
MEM_DATA<27>	AB36	DDR_DATA_27	DDR_DM_0	AJ33	MEM_DQM<0>
MEM_DATA<28>	AB35	DDR_DATA_28	DDR_DM_1	AH33	MEM_DQM<1>
MEM_DATA<29>	AC36	DDR_DATA_29	DDR_DM_2	AD33	MEM_DQM<2>
MEM_DATA<30>	AA32	DDR_DATA_30	DDR_DM_3	AC35	MEM_DQM<3>
MEM_DATA<31>	AB33	DDR_DATA_31	DDR_DM_4	T35	MEM_DQM<4>
MEM_DATA<32>	V36	DDR_DATA_32	DDR_DM_5	T33	MEM_DQM<5>
MEM_DATA<33>	U33	DDR_DATA_33	DDR_DM_6	N32	MEM_DQM<6>
MEM_DATA<34>	U32	DDR_DATA_34	DDR_DM_7	L33	MEM_DQM<7>
MEM_DATA<35>	V35	DDR_DATA_35	DDRRAS	L29	MEM_RAS_L
MEM_DATA<36>	T30	DDR_DATA_36	DDRCAS	H32	MEM_CAS_L
MEM_DATA<37>	U36	DDR_DATA_37	DDRWE	K30	MEM_WE_L
MEM_DATA<38>	U35	DDR_DATA_38	DDRC_E0	AN35	MEM_CKE<0>
MEM_DATA<39>	T36	DDR_DATA_39	DDRC_E1	AM35	MEM_CKE<1>
MEM_DATA<40>	P33	DDR_DATA_40	DDRC_E2	AM36	MEM_CKE<2>
MEM_DATA<41>	R30	DDR_DATA_41	DDRC_E3	AL36	MEM_CKE<3>
MEM_DATA<42>	P35	DDR_DATA_42	DDR_SELHI_0	AB32	MEM_MUXSEL_H<0>
MEM_DATA<43>	P36	DDR_DATA_43	DDR_SELHI_1	AE29	MEM_MUXSEL_H<1>
MEM_DATA<44>	R36	DDR_DATA_44	DDR_SELLO_0	N30	MEM_MUXSEL_L<0>
MEM_DATA<45>	R35	DDR_DATA_45	DDR_SELLO_1	T32	MEM_MUXSEL_L<1>
MEM_DATA<46>	R33	DDR_DATA_46	DDR_MCLK_0_P	Y32	SYCLK_DDRCLK_A0_UF
MEM_DATA<47>	R32	DDR_DATA_47	DDR_MCLK_0_N	Y33	SYCLK_DDRCLK_A0_L_UF
MEM_DATA<48>	N35	DDR_DATA_48	DDR_MCLK_1_P	Y35	SYCLK_DDRCLK_A1_UF
MEM_DATA<49>	M36	DDR_DATA_49	DDR_MCLK_1_N	Y36	SYCLK_DDRCLK_A1_L_UF
MEM_DATA<50>	L35	DDR_DATA_50	DDR_MCLK_2_P	Y30	INT_DDRCLK2_P_TP
MEM_DATA<51>	M35	DDR_DATA_51	DDR_MCLK_2_N	W30	INT_DDRCLK2_N_TP
MEM_DATA<52>	M33	DDR_DATA_52	DDR_MCLK_3_P	W32	SYCLK_DDRCLK_B0_UF
MEM_DATA<53>	L36	DDR_DATA_53	DDR_MCLK_3_N	W33	SYCLK_DDRCLK_B0_L_UF
MEM_DATA<54>	N33	DDR_DATA_54	DDR_MCLK_4_P	V32	SYCLK_DDRCLK_B1_UF
MEM_DATA<55>	M30	DDR_DATA_55	DDR_MCLK_4_N	V32	SYCLK_DDRCLK_B1_L_UF
MEM_DATA<56>	J32	DDR_DATA_56	DDR_MCLK_5_P	W35	INT_DDRCLK5_P_TP
MEM_DATA<57>	J33	DDR_DATA_57	DDR_MCLK_5_N	W36	INT_DDRCLK5_N_TP
MEM_DATA<58>	J35	DDR_DATA_58	DDR_REF	AA22	INT_MEM_REF_H
MEM_DATA<59>	K32	DDR_DATA_59	DDR_VREF_0	Y22	INT_MEM_VREF
MEM_DATA<60>	K33	DDR_DATA_60	DDR_VREF_1	T22	
MEM_DATA<61>	J36	DDR_DATA_61			
MEM_DATA<62>	K36	DDR_DATA_62			
MEM_DATA<63>	K35	DDR_DATA_63			

U45
INTREPID-REV2.1
(2 OF 9)

DDR MEMORY INTERFACE

MEM_VREF



CLOCKS

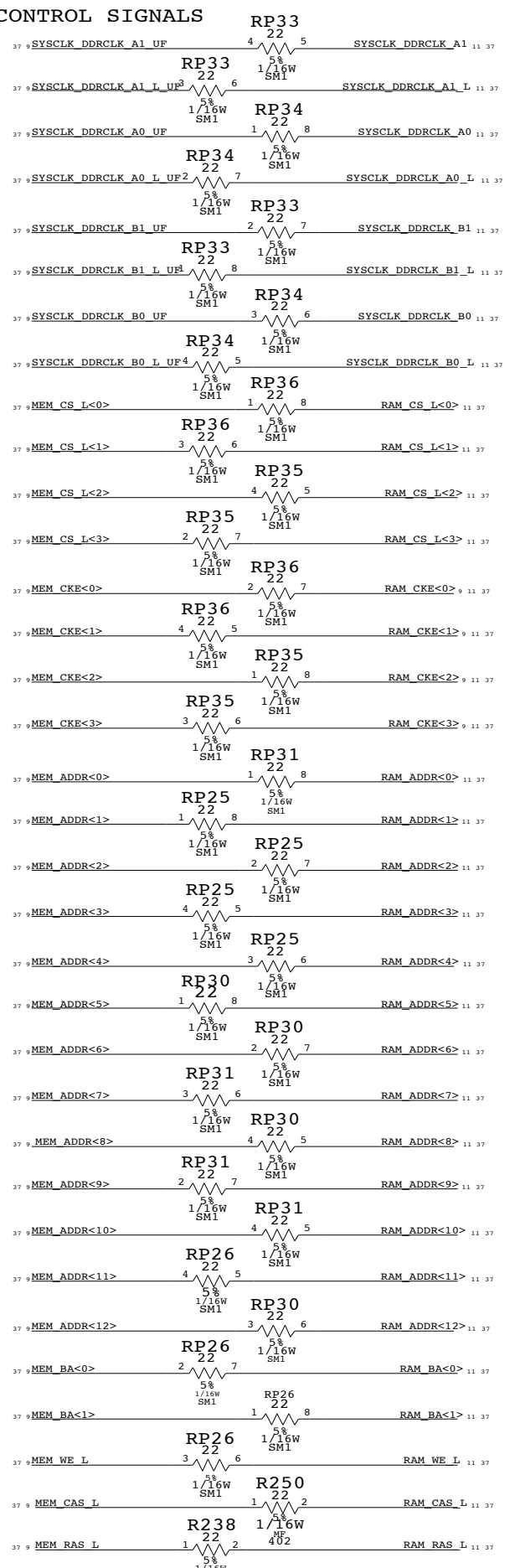
CS

CKE

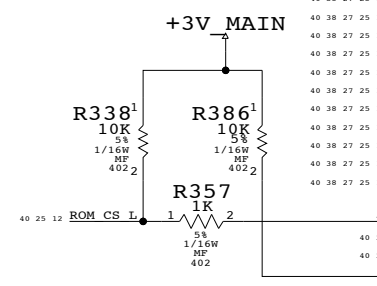
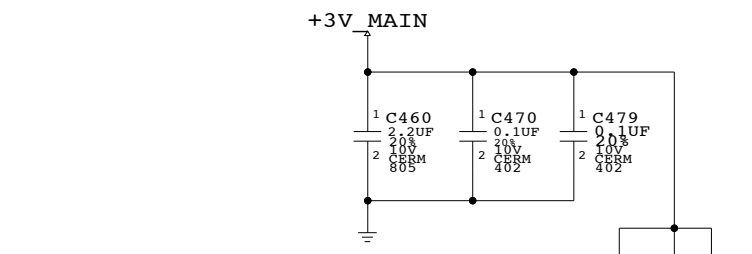
ADDR

BA

CNTL



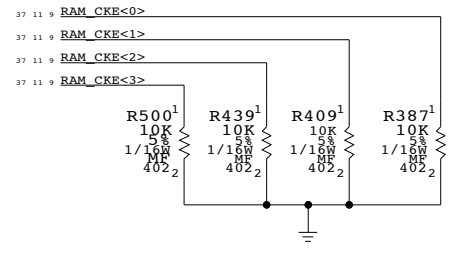
1MB BOOT ROM



Override ROM module intercepts ROM chip select

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1556	1	IC, BOOTROM, Q41B	U17	CRITICAL	?

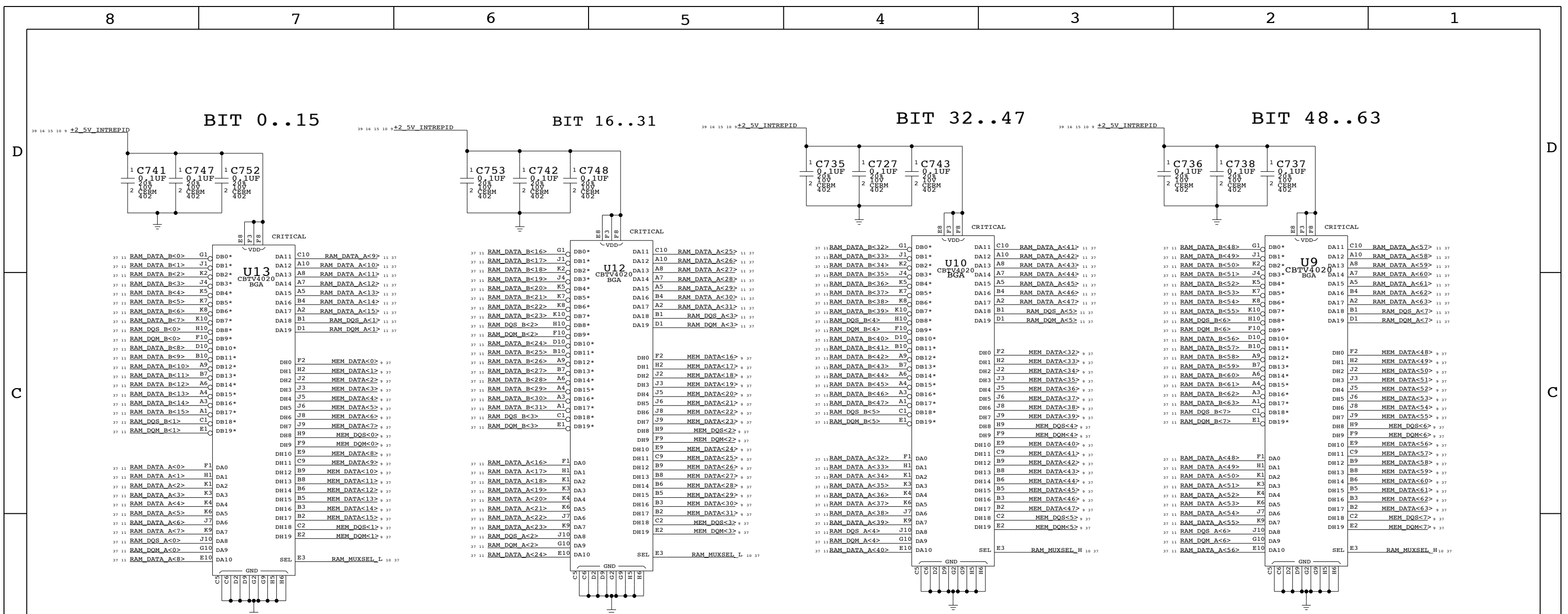
PULL-DOWN RESISTORS TO ENSURE CKE STAYS LOW AFTER INTREPID 2.5V I/O SHUTS OFF



INT - DDR/BOOTROM

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	NONE	D 051-6694	B
		SHT	OF
		9	45



SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
 SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND
 MEM_MUXSEL_H<0> AND MEM_MUXSEL_L<0> ARE ACTIVE LOW
 MEM_MUXSEL_H<1> AND MEM_MUXSEL_L<1> ARE ACTIVE HIGH

ADDED 0 OHM RESISTORS IN CASE POLARITY IS WRONG



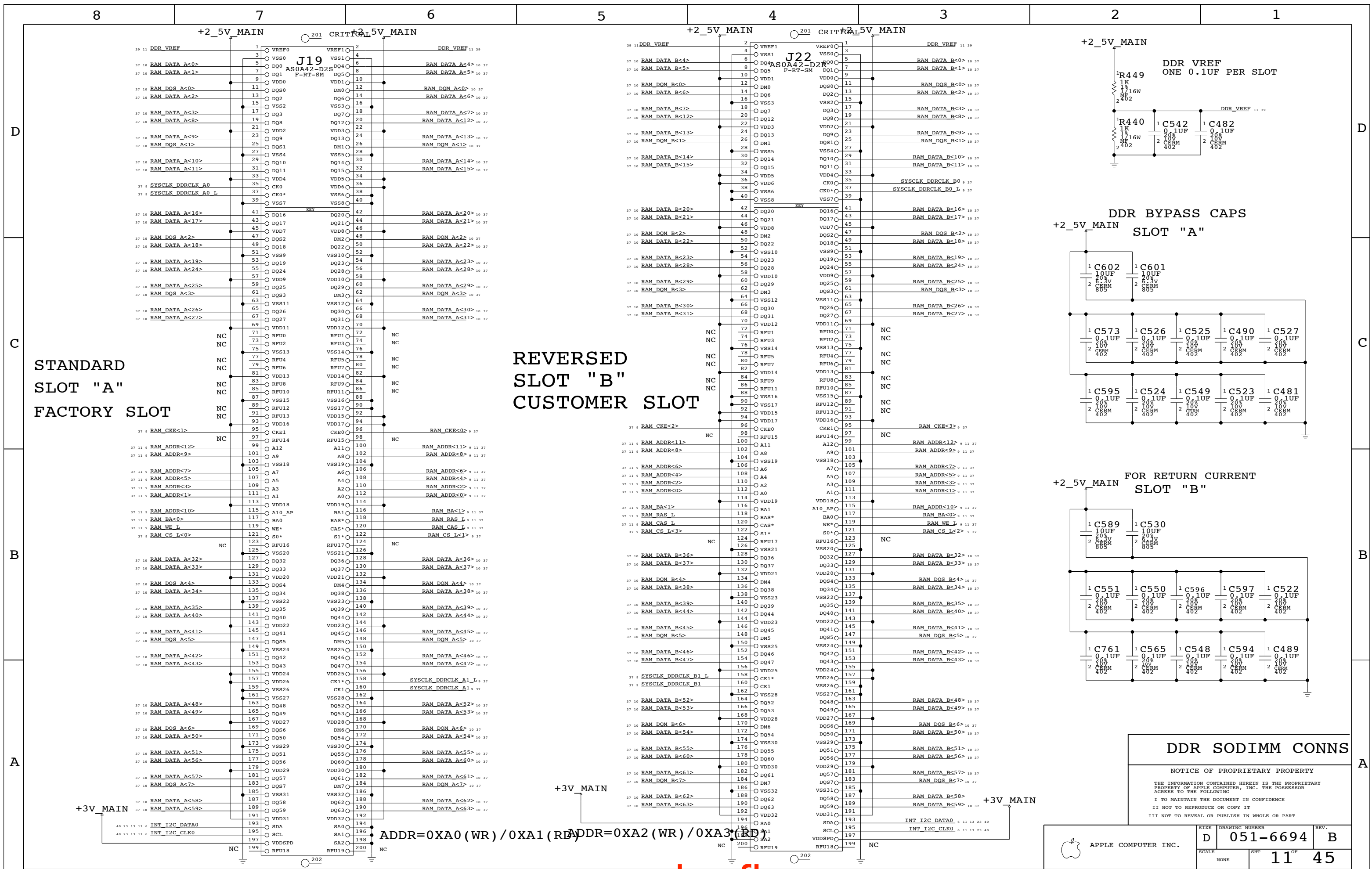
16BIT 2:1 DDR MUXES

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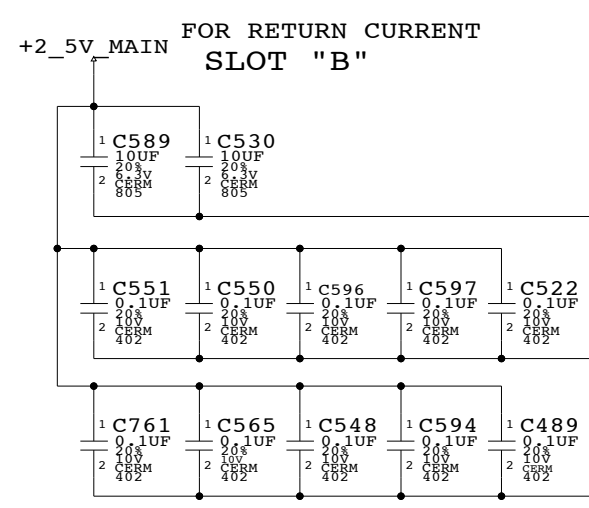
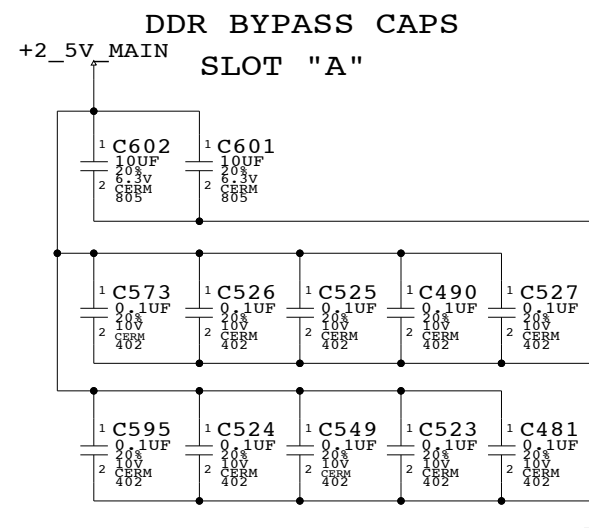
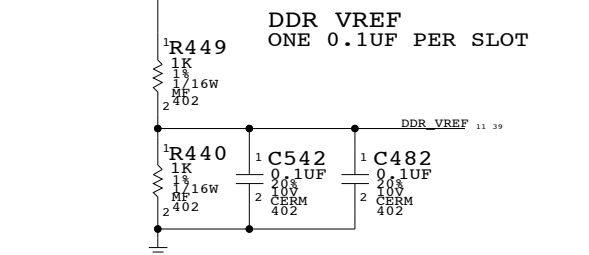
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	D	051-6694	B
SCALE	SHT	OF	
NONE	10	45	



REVERSED
SLOT "B"
CUSTOMER SLOT

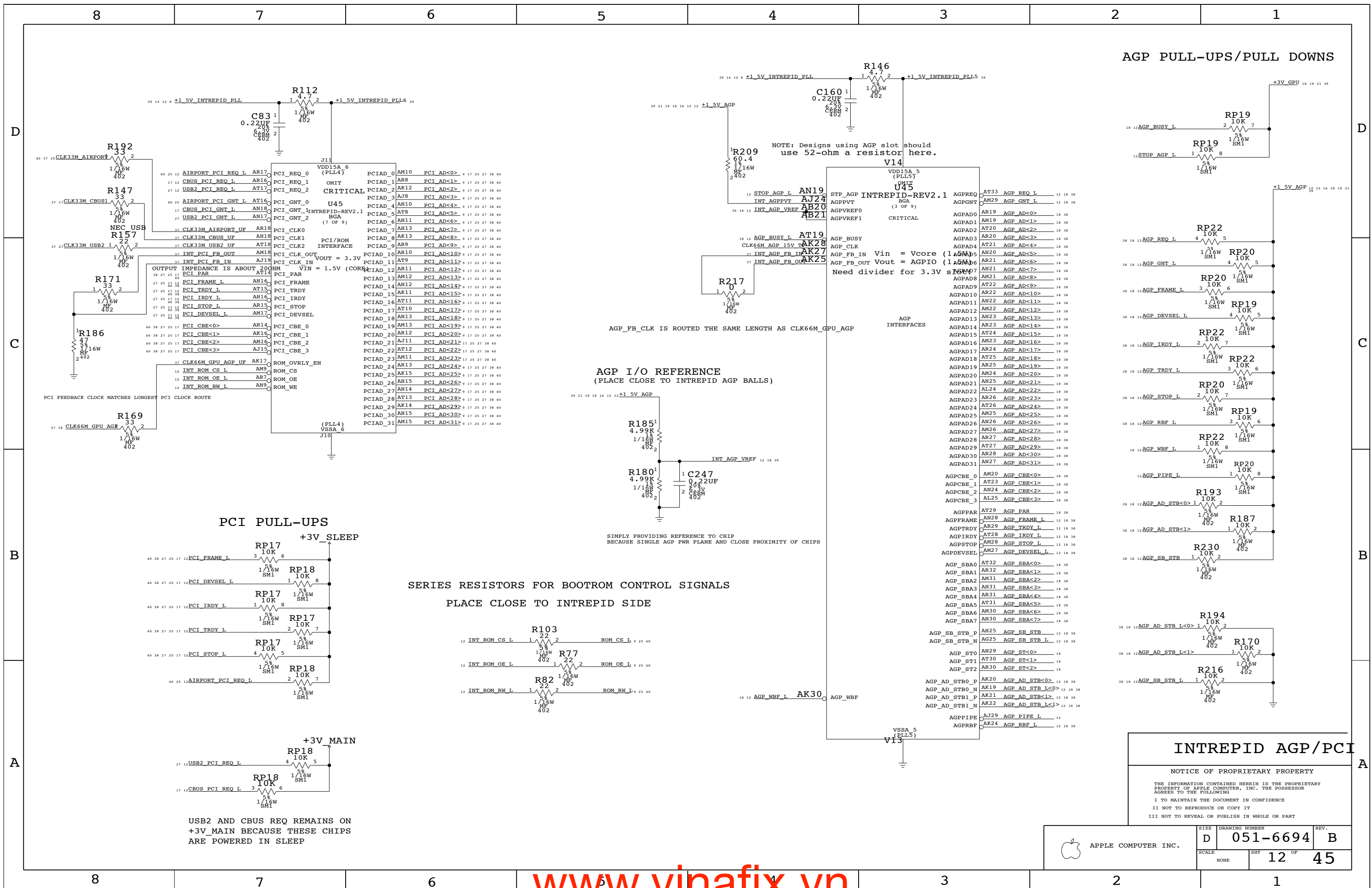
STANDARD
SLOT "A"
FACTORY SLOT

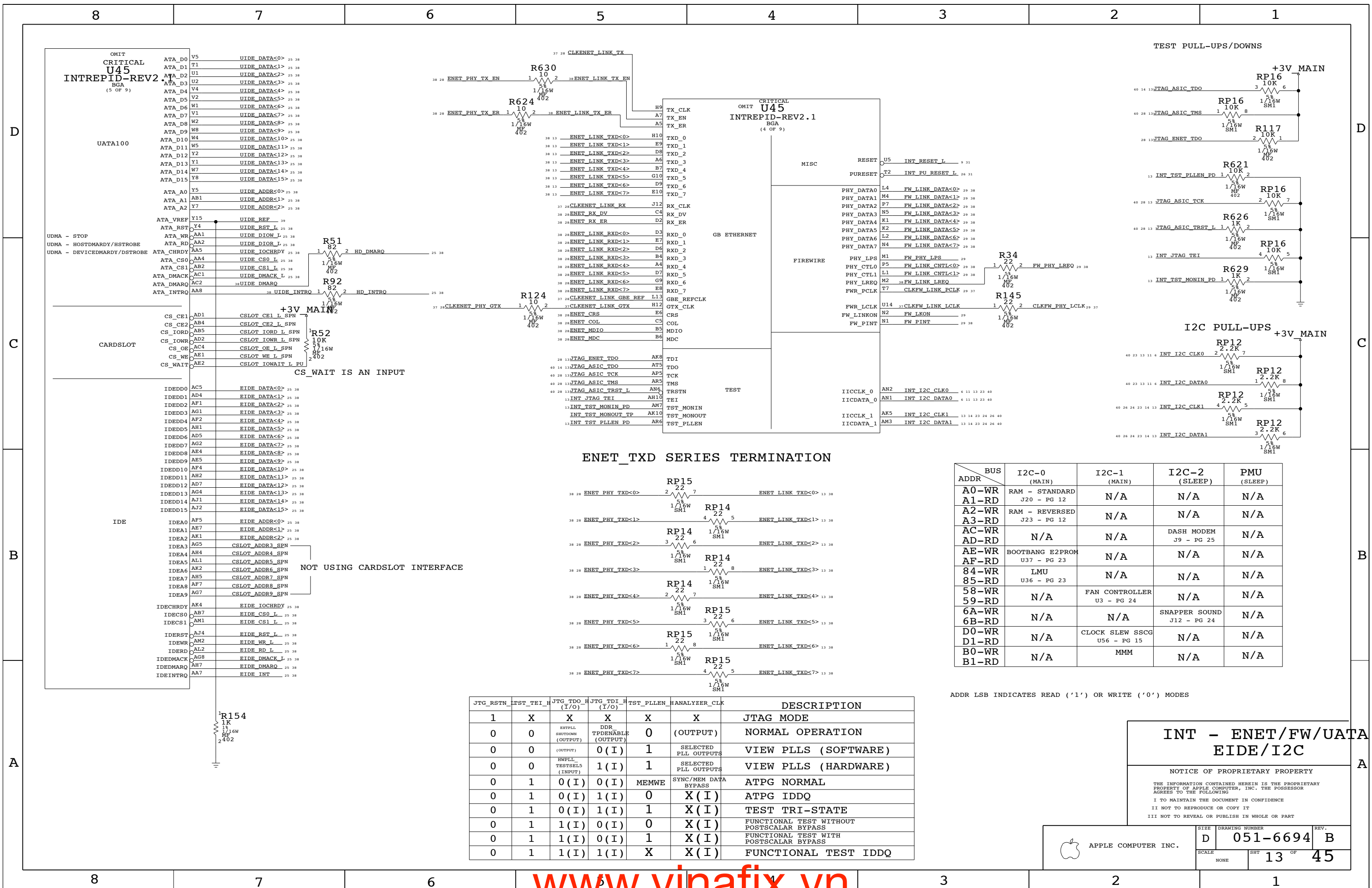


DDR SODIMM CONNS

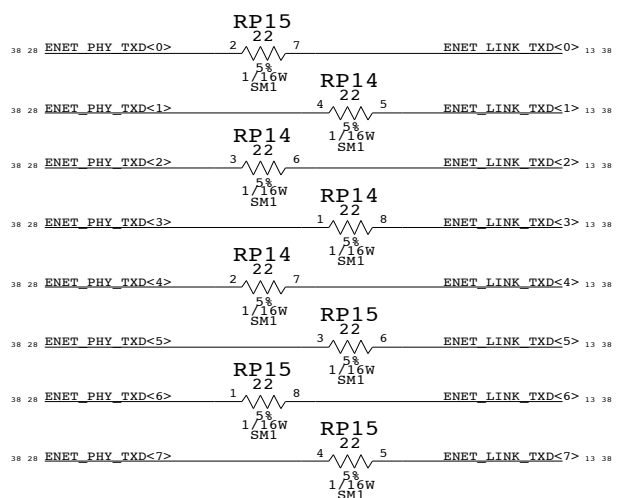
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	D	051-6694	B
SCALE	SHT	11 OF 45	
NONE			





ENET_TXD SERIES TERMINATION



BUS ADDR	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
A0-WR	RAM - STANDARD	N/A	N/A	N/A
A1-RD	J20 - PG 12	N/A	N/A	N/A
A2-WR	RAM - REVERSED	N/A	N/A	N/A
A3-RD	J23 - PG 12	N/A	N/A	N/A
AC-WR	N/A	N/A	DASH MODEM	N/A
AD-RD	N/A	N/A	J9 - PG 25	N/A
AE-WR	BOOTBANG E2PROM	N/A	N/A	N/A
AF-RD	U37 - PG 23	N/A	N/A	N/A
84-WR	LMU	N/A	N/A	N/A
85-RD	U36 - PG 23	N/A	N/A	N/A
58-WR	N/A	FAN CONTROLLER	N/A	N/A
59-RD	N/A	U3 - PG 24	N/A	N/A
6A-WR	N/A	N/A	SNAPPER SOUND	N/A
6B-RD	N/A	N/A	J12 - PG 24	N/A
D0-WR	N/A	CLOCK SLEW SSCG	N/A	N/A
D1-RD	N/A	U56 - PG 15	N/A	N/A
B0-WR	N/A	MMM	N/A	N/A
B1-RD	N/A	N/A	N/A	N/A

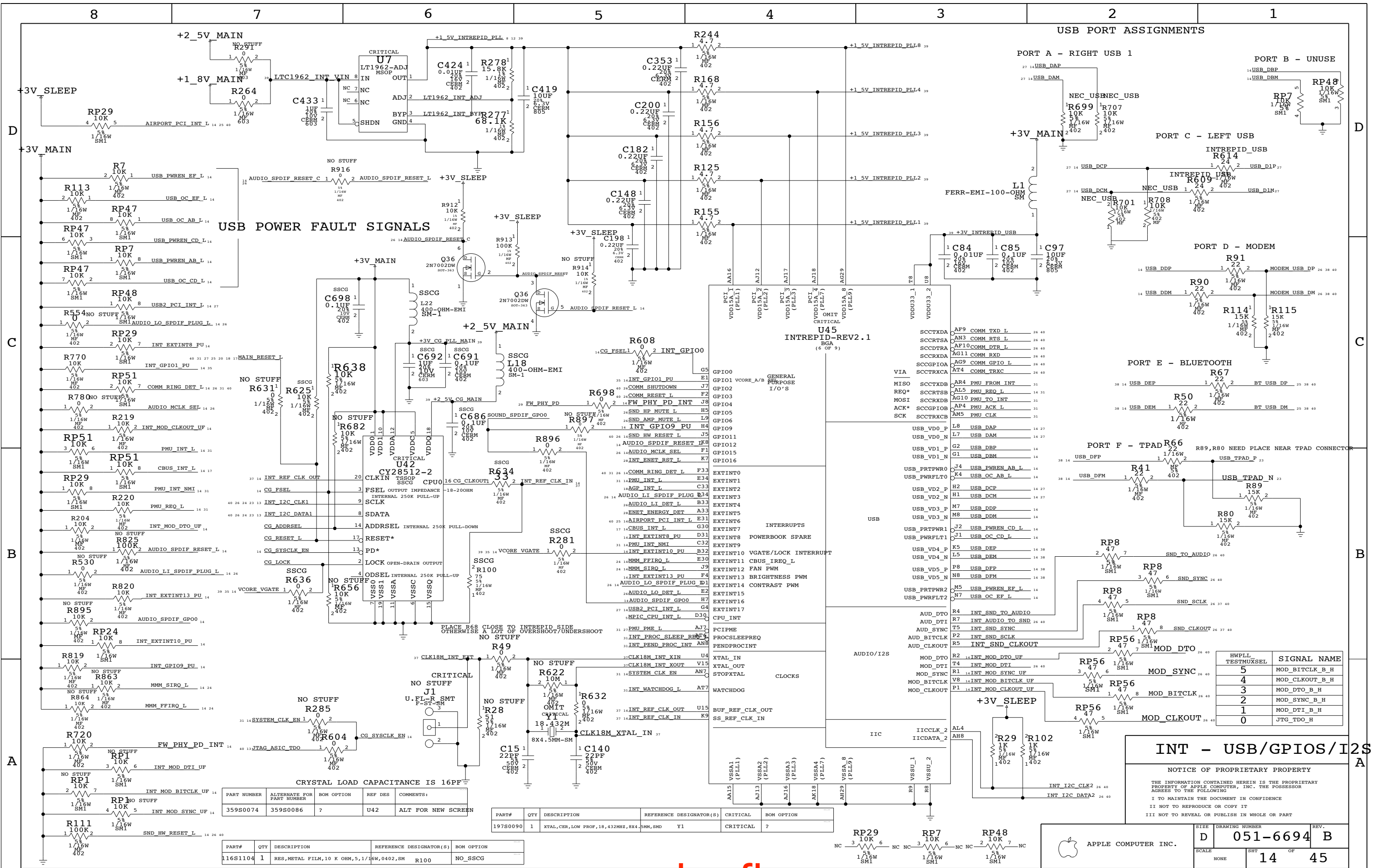
ADDR LSB INDICATES READ ('1') OR WRITE ('0') MODES

JTG_RSTN	TST_TEI	JTG_TDO (I/O)	JTG_TDI (I/O)	TST_PLEN	HANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	EXTPLL SHUTDOWN (OUTPUT)	TPDENABLE (OUTPUT)	0	(OUTPUT)	NORMAL OPERATION
0	0	(OUTPUT)	0 (I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	HWPLL TESTSEL5 (INPUT)	1 (I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0 (I)	0 (I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0 (I)	1 (I)	0	X (I)	ATPG IDDQ
0	1	0 (I)	1 (I)	1	X (I)	TEST TRI-STATE
0	1	1 (I)	0 (I)	0	X (I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1 (I)	0 (I)	1	X (I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1 (I)	1 (I)	X	X (I)	FUNCTIONAL TEST IDDQ

INT - ENET/FW/UATA EIDE/I2C

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SCALE	SHT	OF	
NONE	13	45	



USB POWER FAULT SIGNALS

USB PORT ASSIGNMENTS

INT - USB/GPIOS/I2S

CRYSTAL LOAD CAPACITANCE IS 16PF

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
359S0074	359S0086	?	U42	ALT FOR NEW SCREEN

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0090	1	XTAL,CER,LOW PROF,18,432MHz,8X4.5MM,SMD	Y1	CRITICAL	?

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES,METAL FILM,10 K OHM,5,1/16W,0402,SM	R100	NO_SSCG

HWPLL TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

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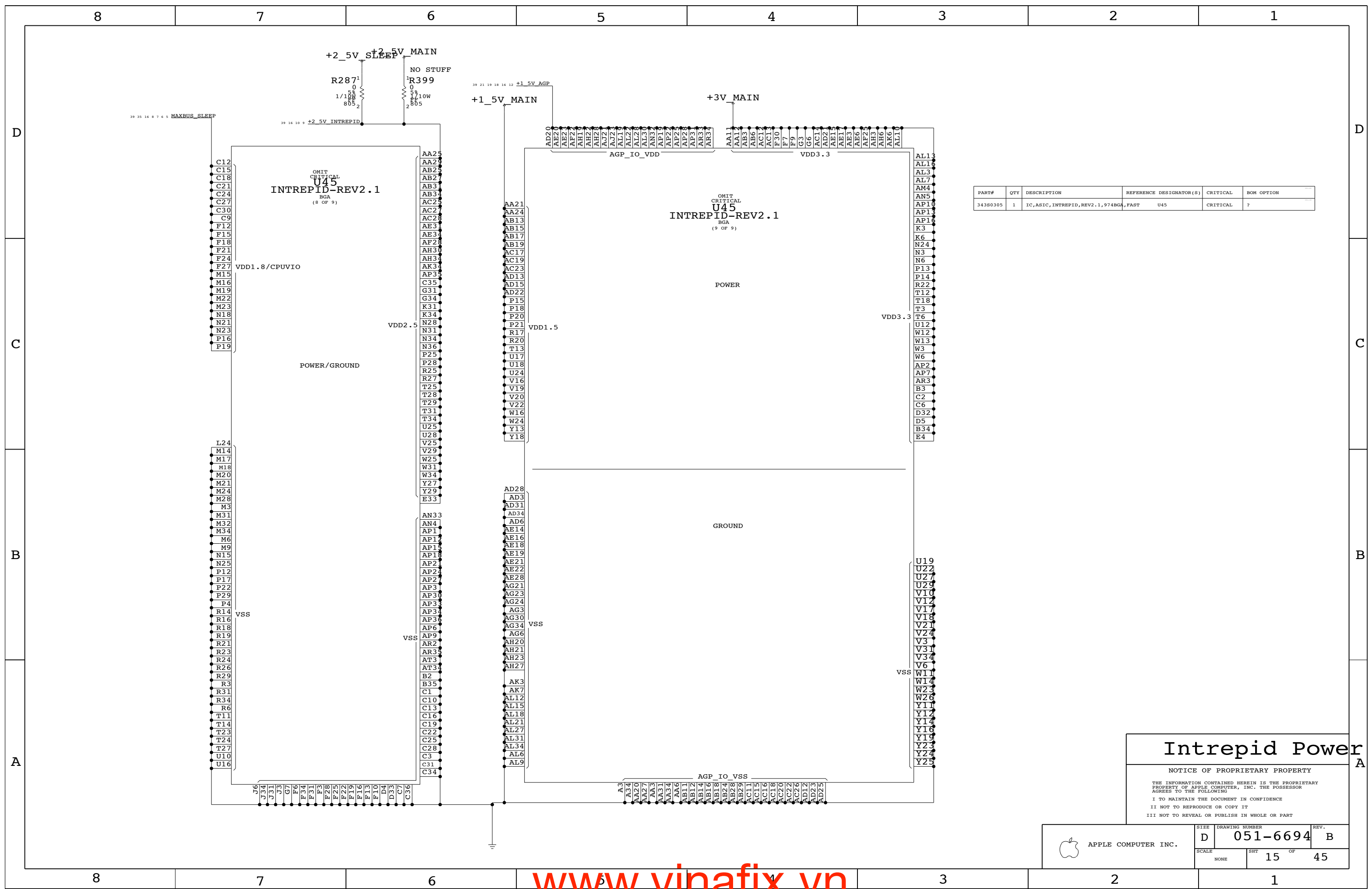
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APPLE COMPUTER INC.

SIZE	D	DRAWING NUMBER	051-6694	REV.	B
SCALE	NONE	SHT	14	OF	45



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
34380305	1	IC,ASIC,INTREPID,REV2.1,974BGA,FAST	U45	CRITICAL	?

Intrepid Power

NOTICE OF PROPRIETARY PROPERTY

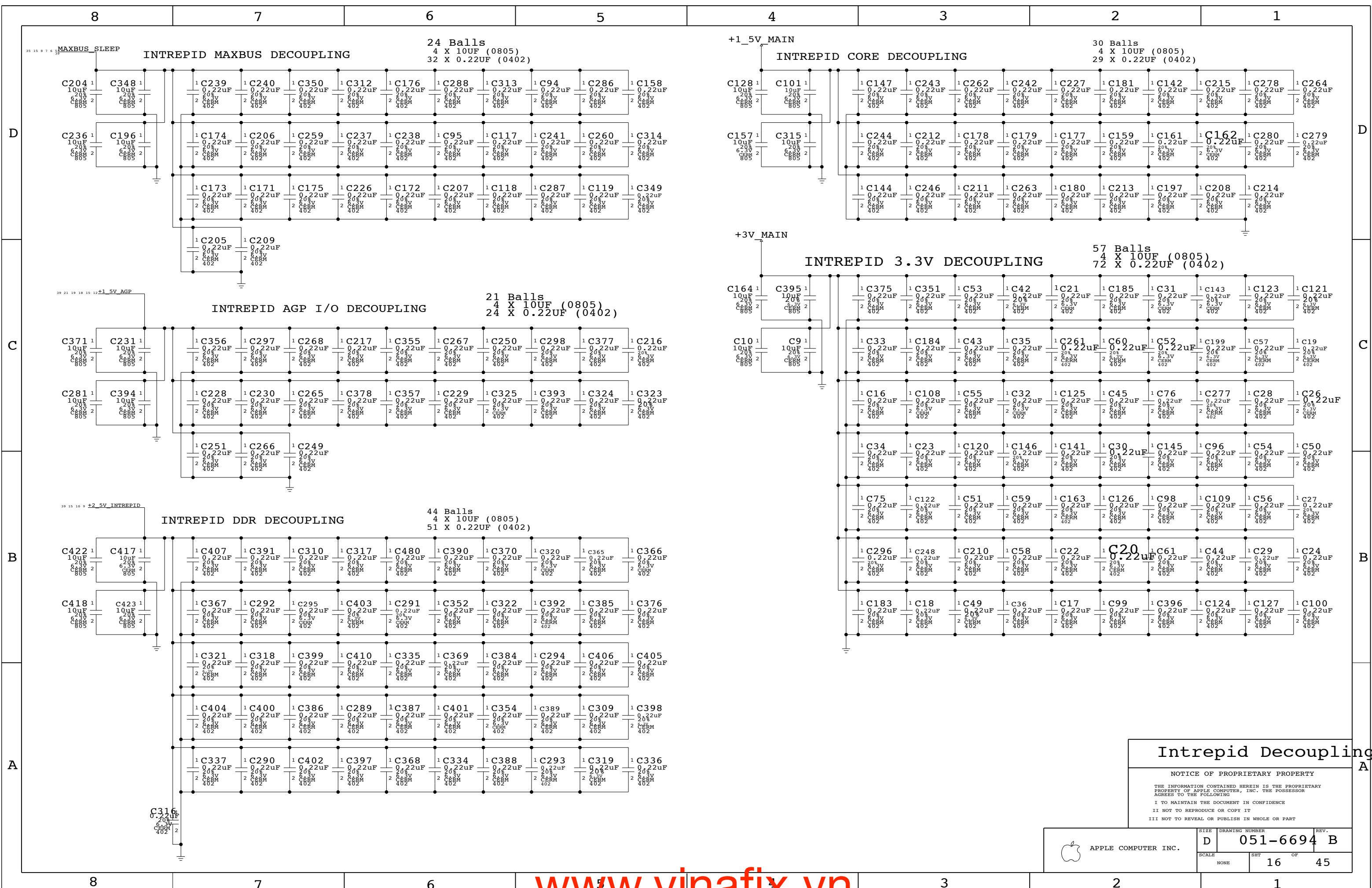
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SCALE	SHT	OF	
NONE	15	45	



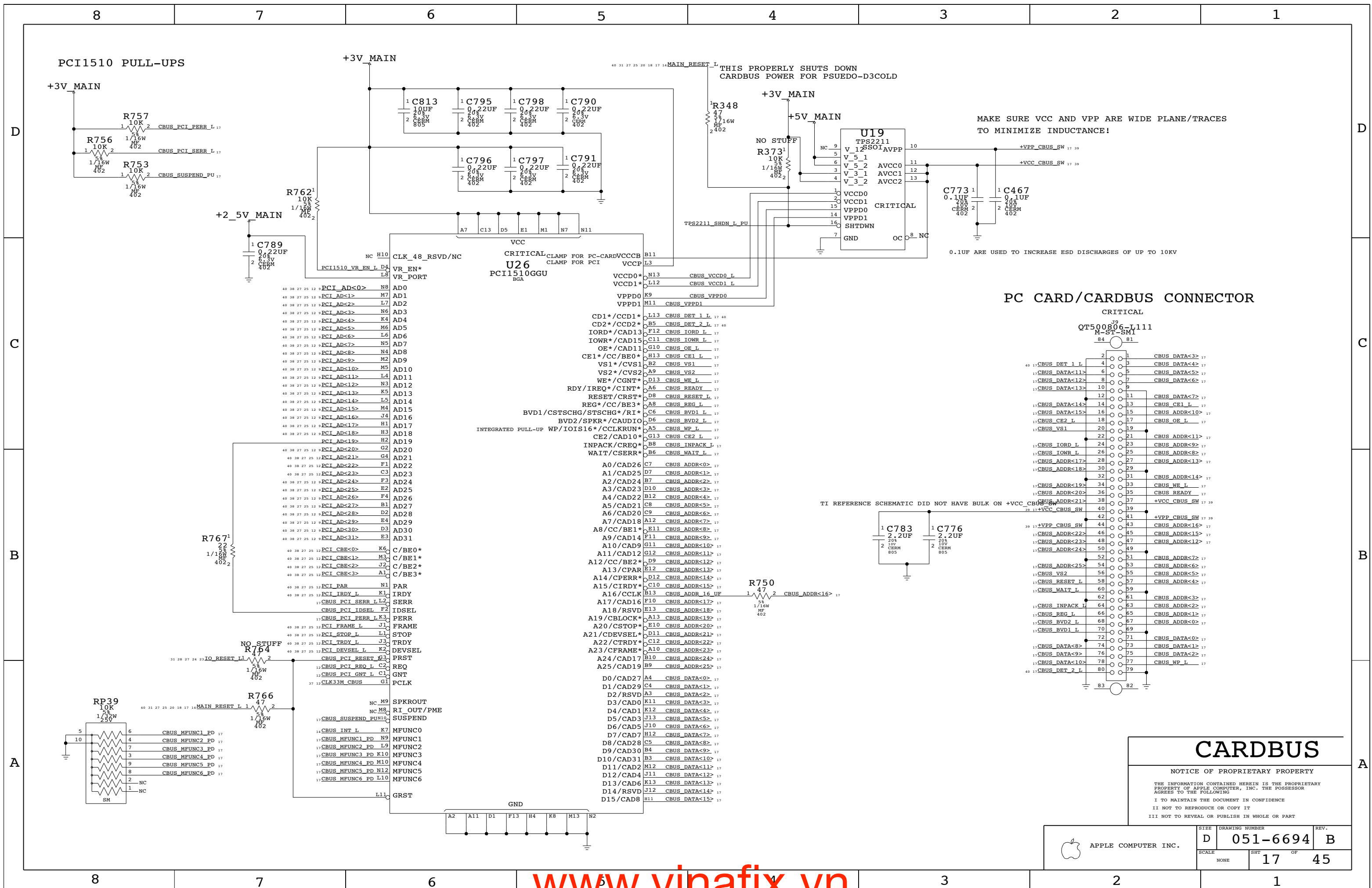
Intrepid Decoupling

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SCALE	SHT	OF	
NONE	16	45	



PC CARD/CARDBUS CONNECTOR

CRITICAL

QT500806-I111
M-ST-SMI

17	CBUS_DET_1_L	2	1	CBUS_DATA<3>	17
17	CBUS_DATA<11>	6	5	CBUS_DATA<42>	17
17	CBUS_DATA<12>	8	7	CBUS_DATA<52>	17
17	CBUS_DATA<13>	10	9	CBUS_DATA<62>	17
17	CBUS_DATA<14>	12	11	CBUS_DATA<72>	17
17	CBUS_DATA<15>	14	13	CBUS_CE1_L	17
17	CBUS_CE2_L	18	17	CBUS_ADDR<10>	17
17	CBUS_VS1	20	19	CBUS_ADDR<11>	17
17	CBUS_IORD_L	24	23	CBUS_ADDR<92>	17
17	CBUS_IOWR_L	26	25	CBUS_ADDR<82>	17
17	CBUS_ADDR<17>	28	27	CBUS_ADDR<13>	17
17	CBUS_ADDR<18>	30	29	CBUS_ADDR<14>	17
17	CBUS_ADDR<19>	34	33	CBUS_WE_L	17
17	CBUS_ADDR<20>	36	35	CBUS_READY	17
17	CBUS_ADDR<21>	38	37	+VCC_CBUS_SW	17
17	CBUS_ADDR<22>	40	39	+VCC_CBUS_SW	17
17	CBUS_ADDR<23>	42	41	+VPP_CBUS_SW	17
17	CBUS_ADDR<24>	44	43	CBUS_ADDR<16>	17
17	CBUS_ADDR<25>	46	45	CBUS_ADDR<15>	17
17	CBUS_VS2	56	55	CBUS_ADDR<12>	17
17	CBUS_RESET_L	58	57	CBUS_ADDR<72>	17
17	CBUS_WAIT_L	60	59	CBUS_ADDR<62>	17
17	CBUS_INPACK_L	64	63	CBUS_ADDR<52>	17
17	CBUS_REG_L	66	65	CBUS_ADDR<12>	17
17	CBUS_BVD2_L	68	67	CBUS_ADDR<02>	17
17	CBUS_BVD1_L	70	69	CBUS_DATA<02>	17
17	CBUS_DATA<8>	74	73	CBUS_DATA<12>	17
17	CBUS_DATA<9>	76	75	CBUS_DATA<22>	17
17	CBUS_DATA<10>	78	77	CBUS_DATA<12>	17
40	CBUS_DET_2_L	80	79	CBUS_WP_L	17

CARDBUS

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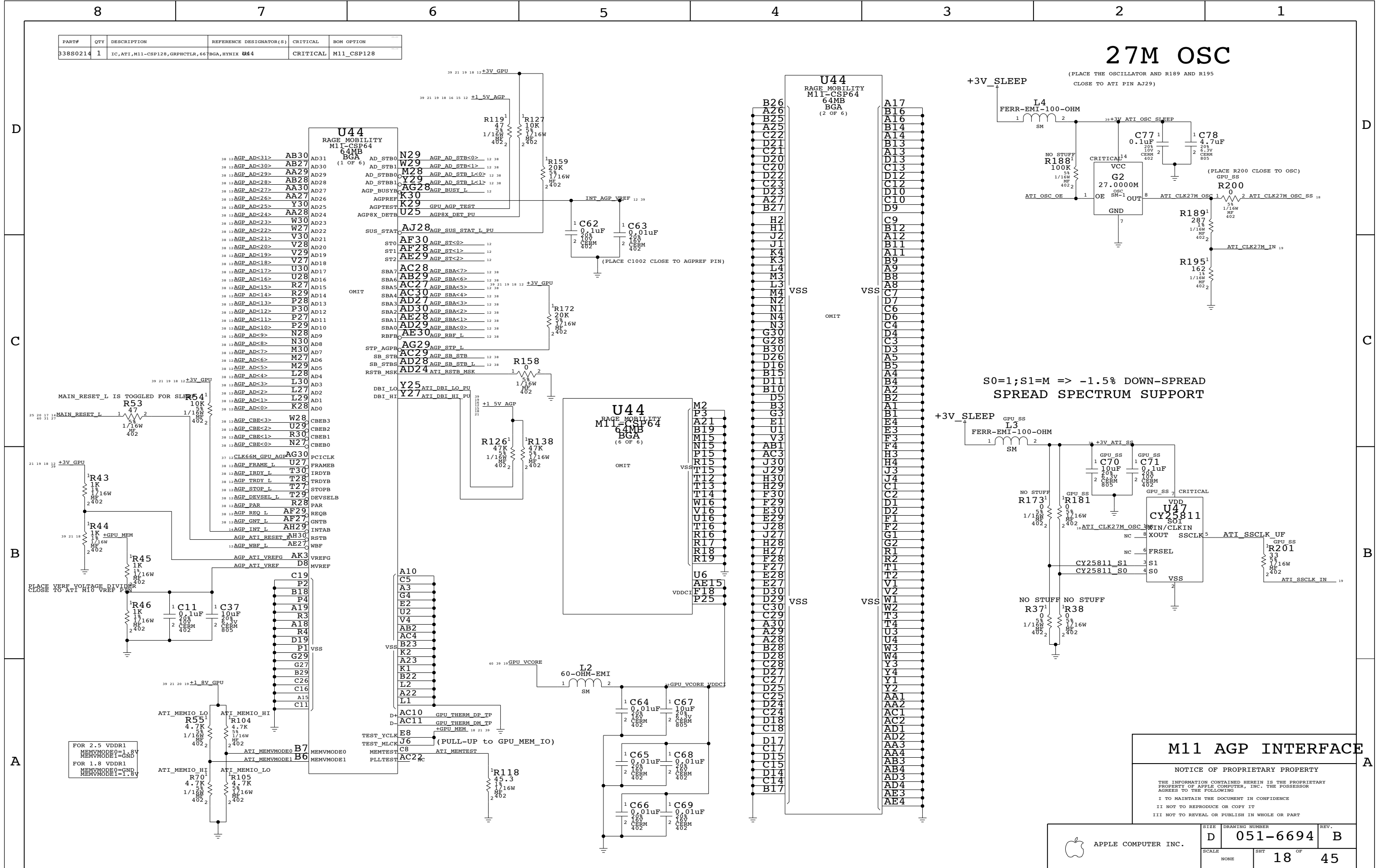
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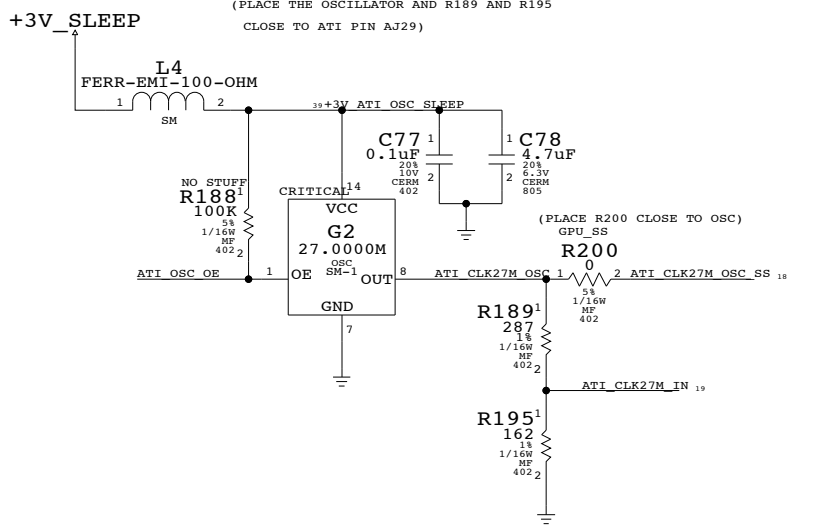
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6694	B
SCALE	NONE	SHT	17 OF 45

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0214	1	IC, ATI, M11-CSP128, GRPCHTLR, 66	BGA, HYNIX U44	CRITICAL	M11_CSP128

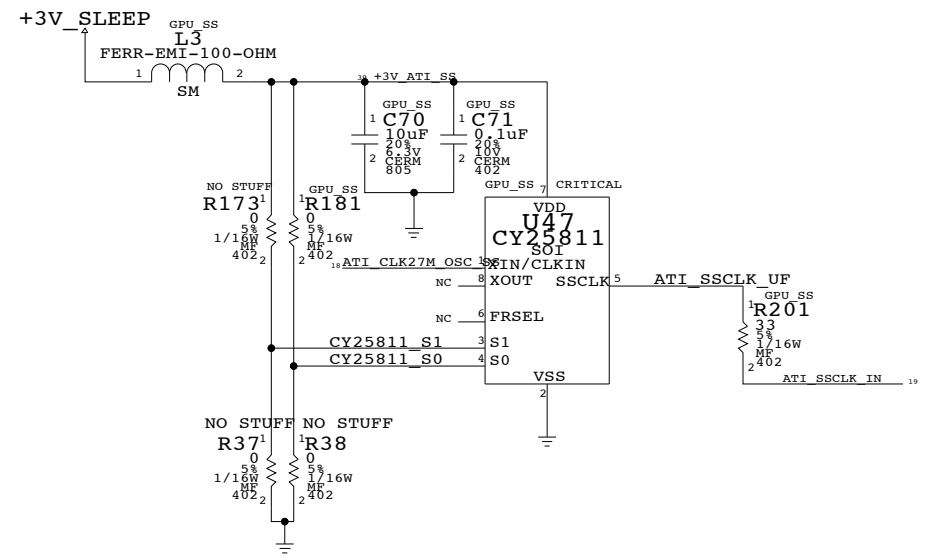


27M OSC

(PLACE THE OSCILLATOR AND R189 AND R195 CLOSE TO ATI PIN AJ29)



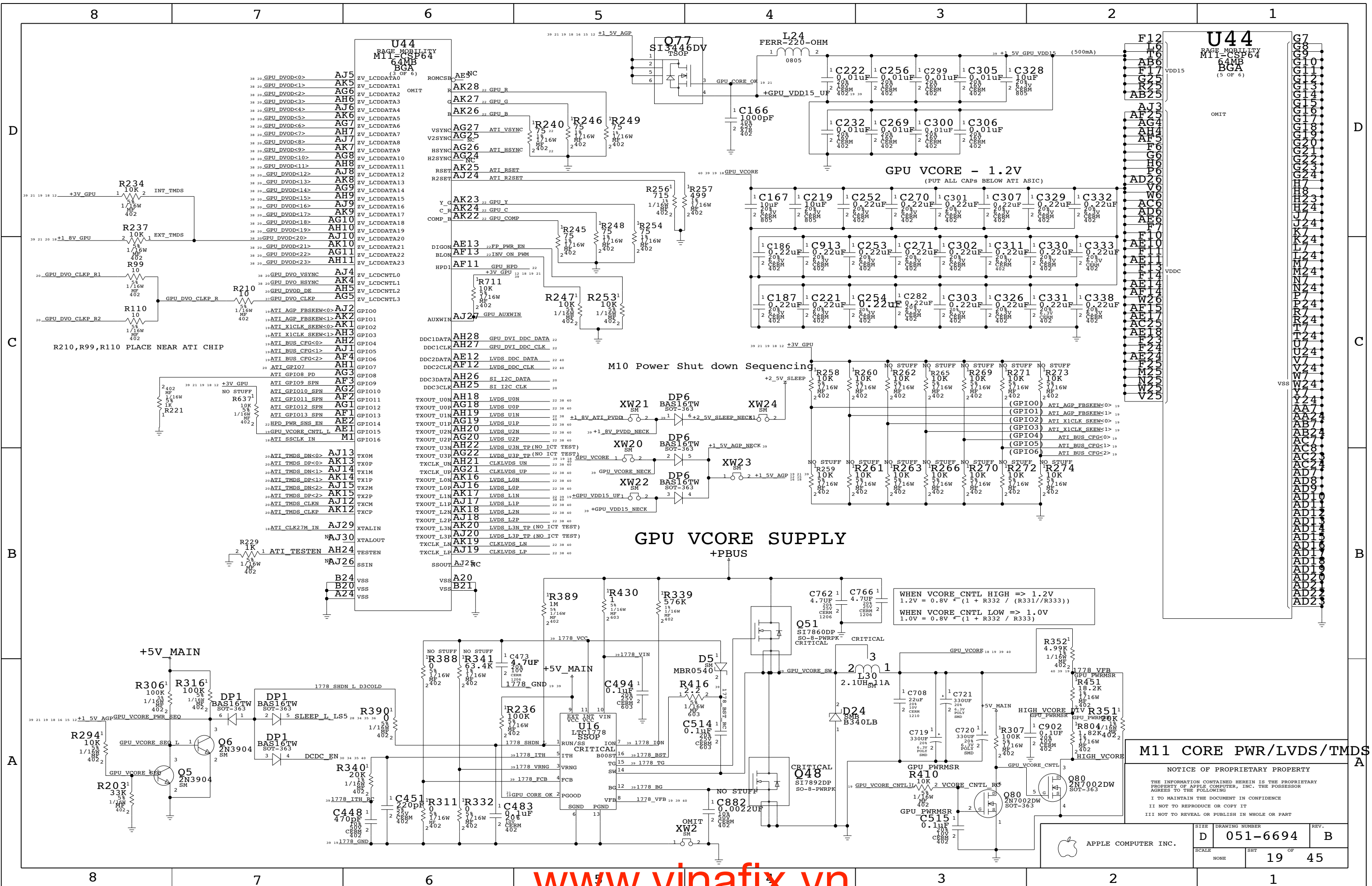
S0=1;S1=M => -1.5% DOWN-SPREAD
SPREAD SPECTRUM SUPPORT



M11 AGP INTERFACE

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SCALE	NONE	SHT	18 OF 45



U44 M11-CSP64 BGA (3 OF 6)

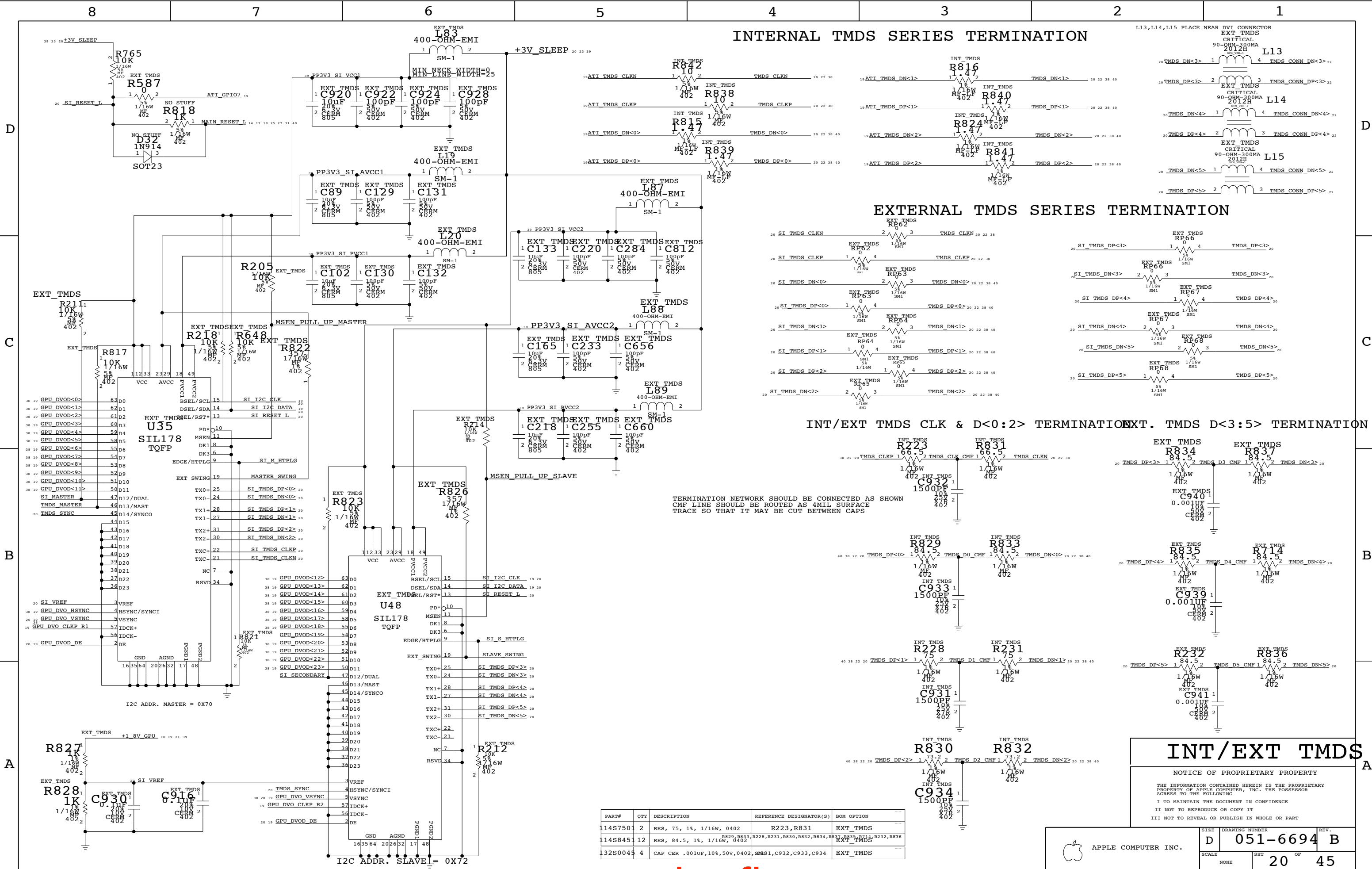
20 GPU DVOD<0>	AJ5	ZV_LCDDATA0	ROMCSB0	AE5C
20 GPU DVOD<1>	AK5	ZV_LCDDATA1	OMIT	AK28
20 GPU DVOD<2>	AG6	ZV_LCDDATA2		AK27
20 GPU DVOD<3>	AH6	ZV_LCDDATA3		AK26
20 GPU DVOD<4>	AJ6	ZV_LCDDATA4		AG27
20 GPU DVOD<5>	AK6	ZV_LCDDATA5		AG25
20 GPU DVOD<6>	AG7	ZV_LCDDATA6		AK26
20 GPU DVOD<7>	AH7	ZV_LCDDATA7		AG27
20 GPU DVOD<8>	AJ7	ZV_LCDDATA8		AG26
20 GPU DVOD<9>	AK7	ZV_LCDDATA9		AG24
20 GPU DVOD<10>	AH8	ZV_LCDDATA10		AK25
20 GPU DVOD<11>	AJ8	ZV_LCDDATA11		AK25
20 GPU DVOD<12>	AK8	ZV_LCDDATA12		AJ24
20 GPU DVOD<13>	AG9	ZV_LCDDATA13		AK23
20 GPU DVOD<14>	AH9	ZV_LCDDATA14		AK24
20 GPU DVOD<15>	AJ9	ZV_LCDDATA15		AK22
20 GPU DVOD<16>	AK9	ZV_LCDDATA16		AE13
20 GPU DVOD<17>	AG10	ZV_LCDDATA17		AF13
20 GPU DVOD<18>	AH10	ZV_LCDDATA18		AF11
20 GPU DVOD<19>	AJ10	ZV_LCDDATA19		AE13
20 GPU DVOD<20>	AK10	ZV_LCDDATA20		AF13
20 GPU DVOD<21>	AH11	ZV_LCDDATA21		AF11
20 GPU DVOD<22>	AJ11	ZV_LCDDATA22		AE13
20 GPU DVOD<23>	AK11	ZV_LCDDATA23		AF13
20 GPU DVO_VSYNC	AJ4	ZV_LCDCNTL0	GPI00	AH28
20 GPU DVO_HSYNC	AK4	ZV_LCDCNTL1	GPI01	AH27
20 GPU DVOD_DE	AH5	ZV_LCDCNTL2	GPI02	AE12
20 GPU DVOD_DE	AG5	ZV_LCDCNTL3	GPI03	AF12
20 GPU DVO_CLKP_R1	AJ2	GPI04	GPI04	AH26
20 GPU DVO_CLKP_R2	AK2	GPI05	GPI05	AH25
20 GPU DVO_CLKP_R2	AH3	GPI06	GPI06	AH18
20 GPU DVO_CLKP_R2	AJ3	GPI07	GPI07	AG18
20 GPU DVO_CLKP_R2	AK3	GPI08	GPI08	AH19
20 GPU DVO_CLKP_R2	AH4	GPI09	GPI09	AG19
20 GPU DVO_CLKP_R2	AG4	GPI10	GPI10	AH20
20 GPU DVO_CLKP_R2	AJ4	GPI11	GPI11	AG20
20 GPU DVO_CLKP_R2	AK4	GPI12	GPI12	AH22
20 GPU DVO_CLKP_R2	AH5	GPI13	GPI13	AG22
20 GPU DVO_CLKP_R2	AG5	GPI14	GPI14	AH21
20 GPU DVO_CLKP_R2	AJ5	GPI15	GPI15	AG21
20 GPU DVO_CLKP_R2	AK5	GPI16	GPI16	AK16
20 GPU DVO_CLKP_R2	AH6	GPI17	GPI17	AJ16
20 GPU DVO_CLKP_R2	AG6	GPI18	GPI18	AK17
20 GPU DVO_CLKP_R2	AJ6	GPI19	GPI19	AJ17
20 GPU DVO_CLKP_R2	AK6	GPI20	GPI20	AK18
20 GPU DVO_CLKP_R2	AH7	GPI21	GPI21	AJ18
20 GPU DVO_CLKP_R2	AJ7	GPI22	GPI22	AK20
20 GPU DVO_CLKP_R2	AK7	GPI23	GPI23	AJ20
20 GPU DVO_CLKP_R2	AG7	GPI24	GPI24	AK19
20 GPU DVO_CLKP_R2	AH8	GPI25	GPI25	AJ19
20 GPU DVO_CLKP_R2	AJ8	GPI26	GPI26	AJ26
20 GPU DVO_CLKP_R2	AK8	GPI27	GPI27	B24
20 GPU DVO_CLKP_R2	AG8	GPI28	GPI28	B20
20 GPU DVO_CLKP_R2	AH9	GPI29	GPI29	A24
20 GPU DVO_CLKP_R2	AJ9	GPI30	GPI30	
20 GPU DVO_CLKP_R2	AK9	GPI31	GPI31	
20 GPU DVO_CLKP_R2	AH10	GPI32	GPI32	
20 GPU DVO_CLKP_R2	AJ10	GPI33	GPI33	
20 GPU DVO_CLKP_R2	AK10	GPI34	GPI34	
20 GPU DVO_CLKP_R2	AH11	GPI35	GPI35	
20 GPU DVO_CLKP_R2	AJ11	GPI36	GPI36	
20 GPU DVO_CLKP_R2	AK11	GPI37	GPI37	
20 GPU DVO_CLKP_R2	AH12	GPI38	GPI38	
20 GPU DVO_CLKP_R2	AJ12	GPI39	GPI39	
20 GPU DVO_CLKP_R2	AK12	GPI40	GPI40	
20 GPU DVO_CLKP_R2	AH13	GPI41	GPI41	
20 GPU DVO_CLKP_R2	AJ13	GPI42	GPI42	
20 GPU DVO_CLKP_R2	AK13	GPI43	GPI43	
20 GPU DVO_CLKP_R2	AH14	GPI44	GPI44	
20 GPU DVO_CLKP_R2	AJ14	GPI45	GPI45	
20 GPU DVO_CLKP_R2	AK14	GPI46	GPI46	
20 GPU DVO_CLKP_R2	AH15	GPI47	GPI47	
20 GPU DVO_CLKP_R2	AJ15	GPI48	GPI48	
20 GPU DVO_CLKP_R2	AK15	GPI49	GPI49	
20 GPU DVO_CLKP_R2	AH16	GPI50	GPI50	
20 GPU DVO_CLKP_R2	AJ16	GPI51	GPI51	
20 GPU DVO_CLKP_R2	AK16	GPI52	GPI52	
20 GPU DVO_CLKP_R2	AH17	GPI53	GPI53	
20 GPU DVO_CLKP_R2	AJ17	GPI54	GPI54	
20 GPU DVO_CLKP_R2	AK17	GPI55	GPI55	
20 GPU DVO_CLKP_R2	AH18	GPI56	GPI56	
20 GPU DVO_CLKP_R2	AJ18	GPI57	GPI57	
20 GPU DVO_CLKP_R2	AK18	GPI58	GPI58	
20 GPU DVO_CLKP_R2	AH19	GPI59	GPI59	
20 GPU DVO_CLKP_R2	AJ19	GPI60	GPI60	
20 GPU DVO_CLKP_R2	AK19	GPI61	GPI61	
20 GPU DVO_CLKP_R2	AH20	GPI62	GPI62	
20 GPU DVO_CLKP_R2	AJ20	GPI63	GPI63	
20 GPU DVO_CLKP_R2	AK20	GPI64	GPI64	
20 GPU DVO_CLKP_R2	AH21	GPI65	GPI65	
20 GPU DVO_CLKP_R2	AJ21	GPI66	GPI66	
20 GPU DVO_CLKP_R2	AK21	GPI67	GPI67	
20 GPU DVO_CLKP_R2	AH22	GPI68	GPI68	
20 GPU DVO_CLKP_R2	AJ22	GPI69	GPI69	
20 GPU DVO_CLKP_R2	AK22	GPI70	GPI70	
20 GPU DVO_CLKP_R2	AH23	GPI71	GPI71	
20 GPU DVO_CLKP_R2	AJ23	GPI72	GPI72	
20 GPU DVO_CLKP_R2	AK23	GPI73	GPI73	
20 GPU DVO_CLKP_R2	AH24	GPI74	GPI74	
20 GPU DVO_CLKP_R2	AJ24	GPI75	GPI75	
20 GPU DVO_CLKP_R2	AK24	GPI76	GPI76	
20 GPU DVO_CLKP_R2	AH25	GPI77	GPI77	
20 GPU DVO_CLKP_R2	AJ25	GPI78	GPI78	
20 GPU DVO_CLKP_R2	AK25	GPI79	GPI79	
20 GPU DVO_CLKP_R2	AH26	GPI80	GPI80	
20 GPU DVO_CLKP_R2	AJ26	GPI81	GPI81	
20 GPU DVO_CLKP_R2	AK26	GPI82	GPI82	
20 GPU DVO_CLKP_R2	AH27	GPI83	GPI83	
20 GPU DVO_CLKP_R2	AJ27	GPI84	GPI84	
20 GPU DVO_CLKP_R2	AK27	GPI85	GPI85	
20 GPU DVO_CLKP_R2	AH28	GPI86	GPI86	
20 GPU DVO_CLKP_R2	AJ28	GPI87	GPI87	
20 GPU DVO_CLKP_R2	AK28	GPI88	GPI88	
20 GPU DVO_CLKP_R2	AH29	GPI89	GPI89	
20 GPU DVO_CLKP_R2	AJ29	GPI90	GPI90	
20 GPU DVO_CLKP_R2	AK29	GPI91	GPI91	
20 GPU DVO_CLKP_R2	AH30	GPI92	GPI92	
20 GPU DVO_CLKP_R2	AJ30	GPI93	GPI93	
20 GPU DVO_CLKP_R2	AK30	GPI94	GPI94	
20 GPU DVO_CLKP_R2	AH31	GPI95	GPI95	
20 GPU DVO_CLKP_R2	AJ31	GPI96	GPI96	
20 GPU DVO_CLKP_R2	AK31	GPI97	GPI97	
20 GPU DVO_CLKP_R2	AH32	GPI98	GPI98	
20 GPU DVO_CLKP_R2	AJ32	GPI99	GPI99	
20 GPU DVO_CLKP_R2	AK32	GPI100	GPI100	

M11 CORE PWR/LVDS/TMDS

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SCALE	SHT	OF
NONE	19	45

APPLE COMPUTER INC.



INTERNAL TMSD SERIES TERMINATION

EXTERNAL TMSD SERIES TERMINATION

INT/EXT TMSD CLK & D<0:2> TERMINATION EXT. TMSD D<3:5> TERMINATION

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN
 CMF LINE SHOULD BE ROUTED AS 4MIL SURFACE
 TRACE SO THAT IT MAY BE CUT BETWEEN CAPS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S7501	2	RES, 75, 1%, 1/16W, 0402	R223, R831	EXT_TMSD
114S8451	12	RES, 84.5, 1%, 1/16W, 0402	R228, R231, R830, R832, R834, R835, R836, R837, R838, R839, R840, R841, R845, R846, R847, R848, R849, R850, R851, R852, R853, R854, R855, R856, R857, R858, R859, R860, R861, R862, R863, R864, R865, R866, R867, R868, R869, R870, R871, R872, R873, R874, R875, R876, R877, R878, R879, R880, R881, R882, R883, R884, R885, R886, R887, R888, R889, R890, R891, R892, R893, R894, R895, R896, R897, R898, R899, R900	EXT_TMSD
132S0044	4	CAP CER .001UF, 10%, 50V, 0402	C931, C932, C933, C934	EXT_TMSD

INT/EXT TMSD

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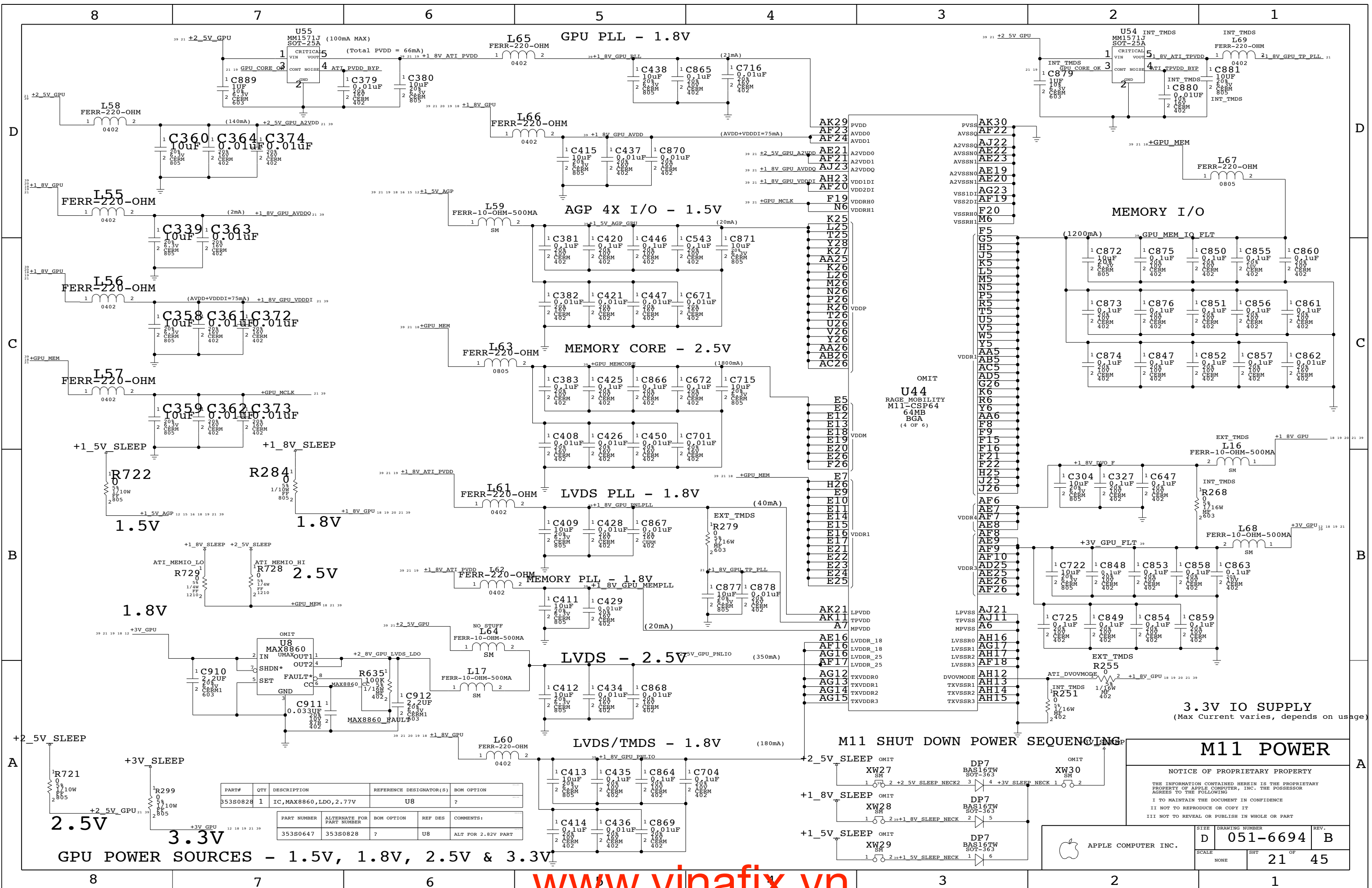
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APPLE COMPUTER INC.

SIZE: D DRAWING NUMBER: 051-6694 B REV. 1

SCALE: NONE SHEET: 20 OF 45



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S0828	1	IC, MAX8860, LDO, 2.77V	U8	?
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0647	353S0828	?	U8	ALT FOR 2.82V PART

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	NONE	051-6694	B
SCALE		SHT	OF
NONE		21	45

ANALOG FILTERING PLACE CLOSE TO CONNECTOR

EXTERNAL VIDEO (DVI) INTERFACE

Power key detect path when system is shutdown or asleep...
DVI HPD will be driven low when power key is pressed...
As host falls rise of remote device isolation will be disabled as well.

DVI POWER SWITCH

D

D

C

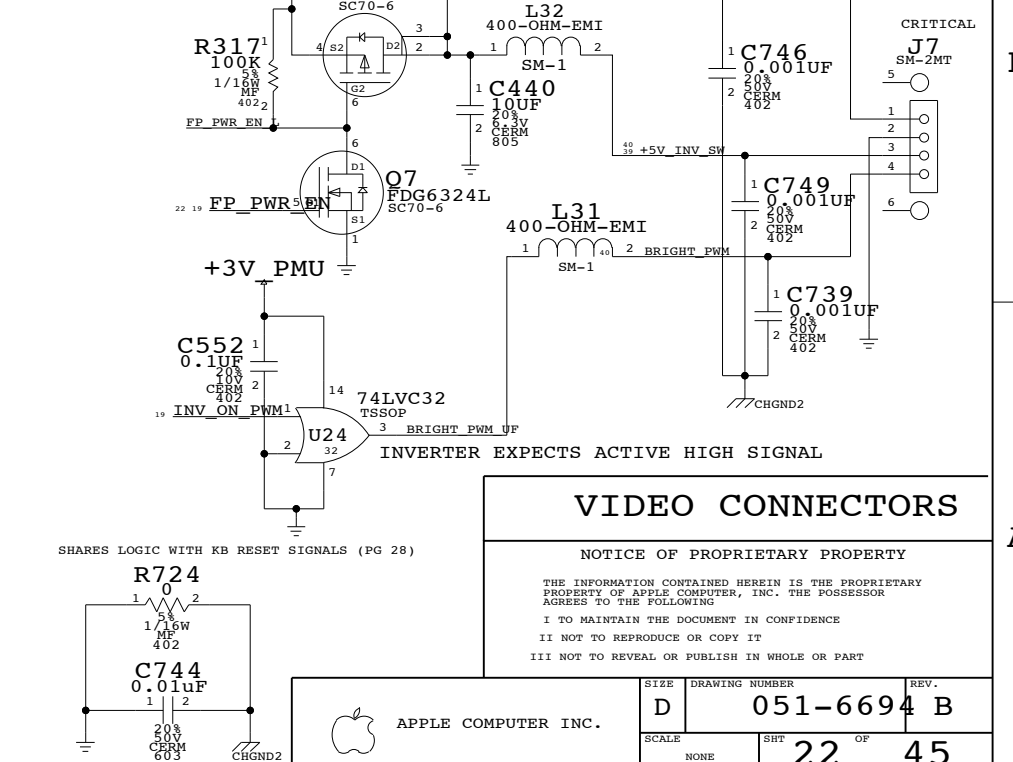
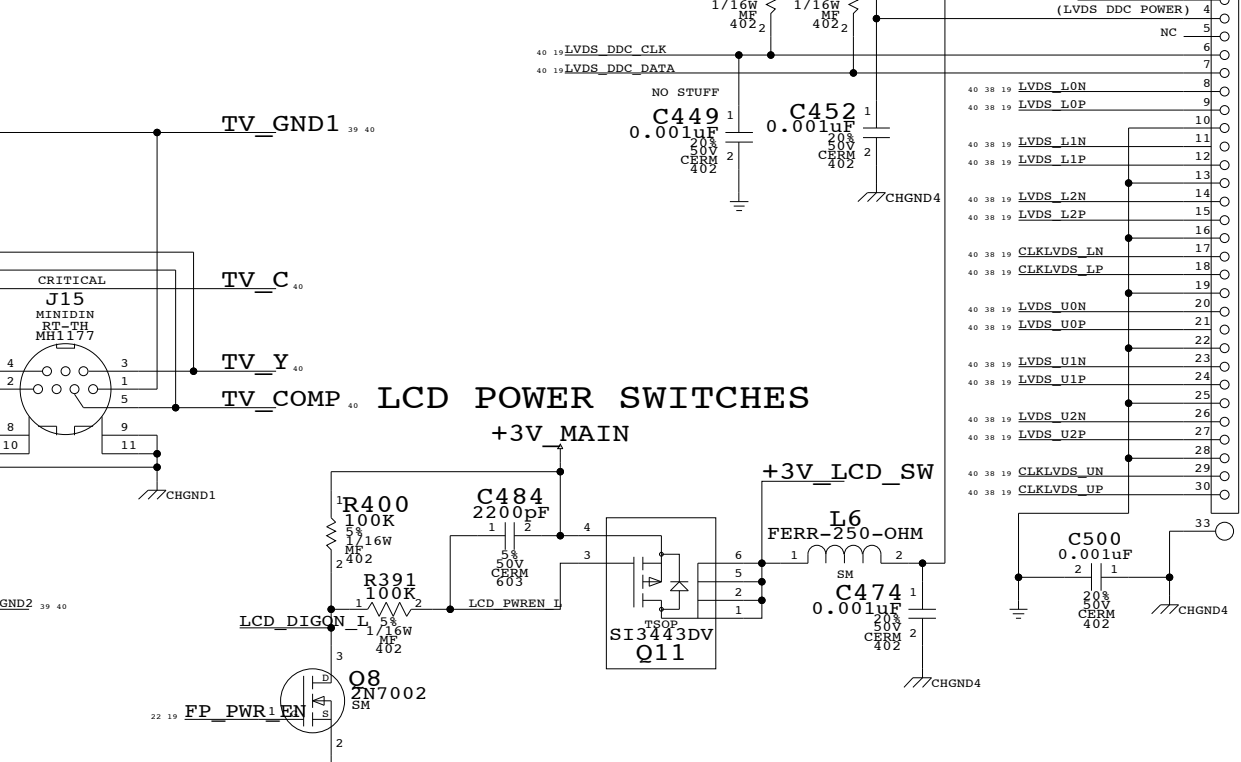
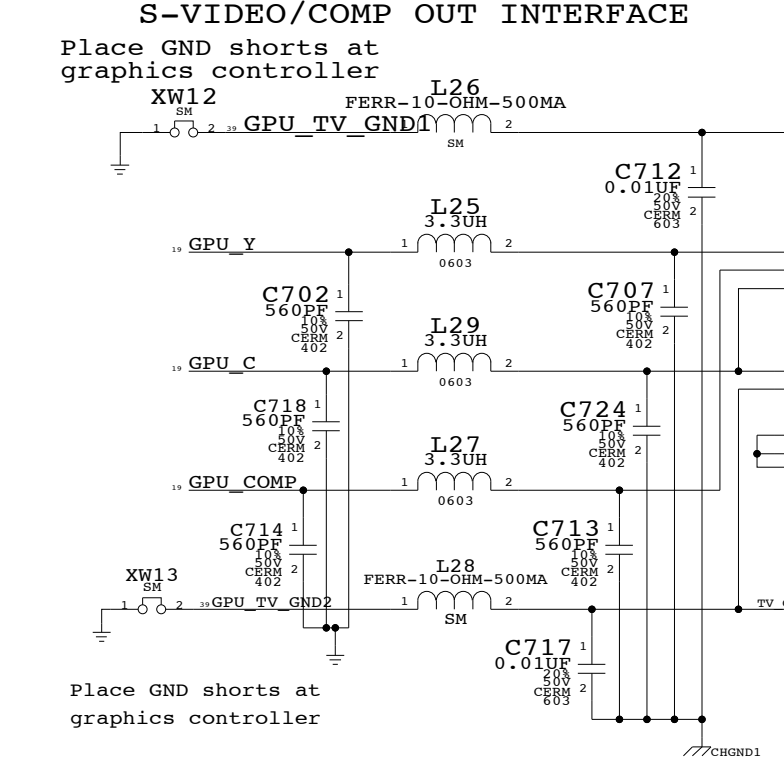
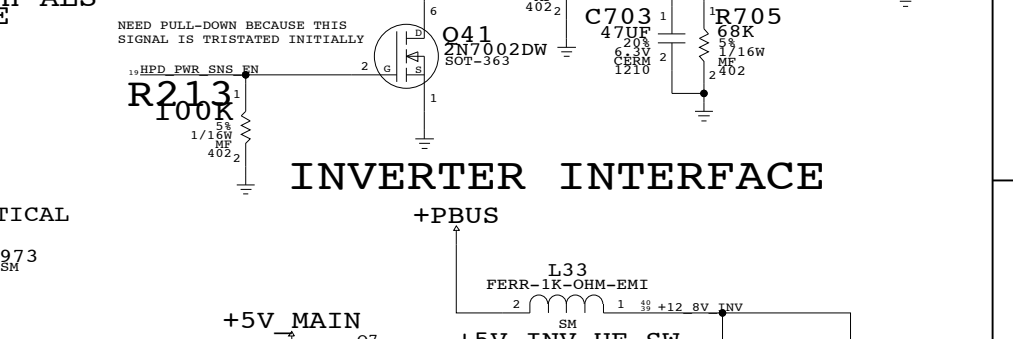
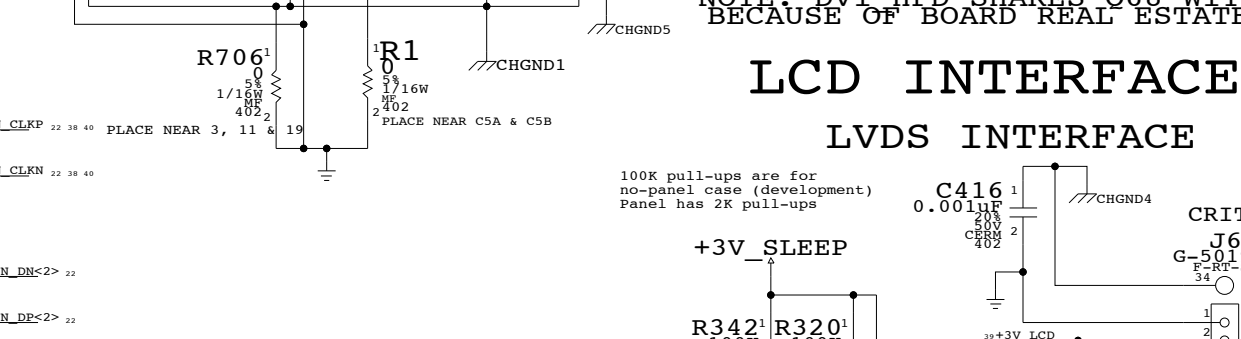
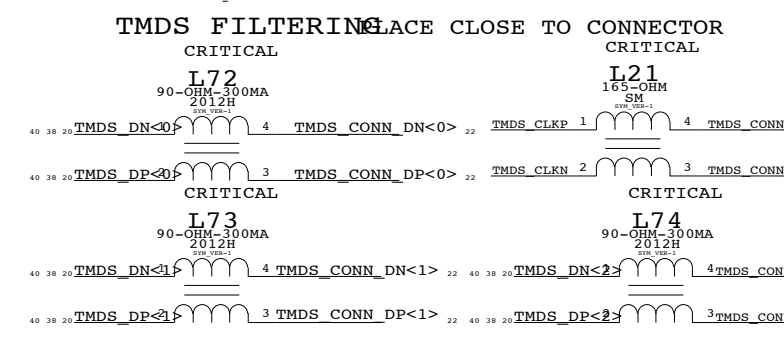
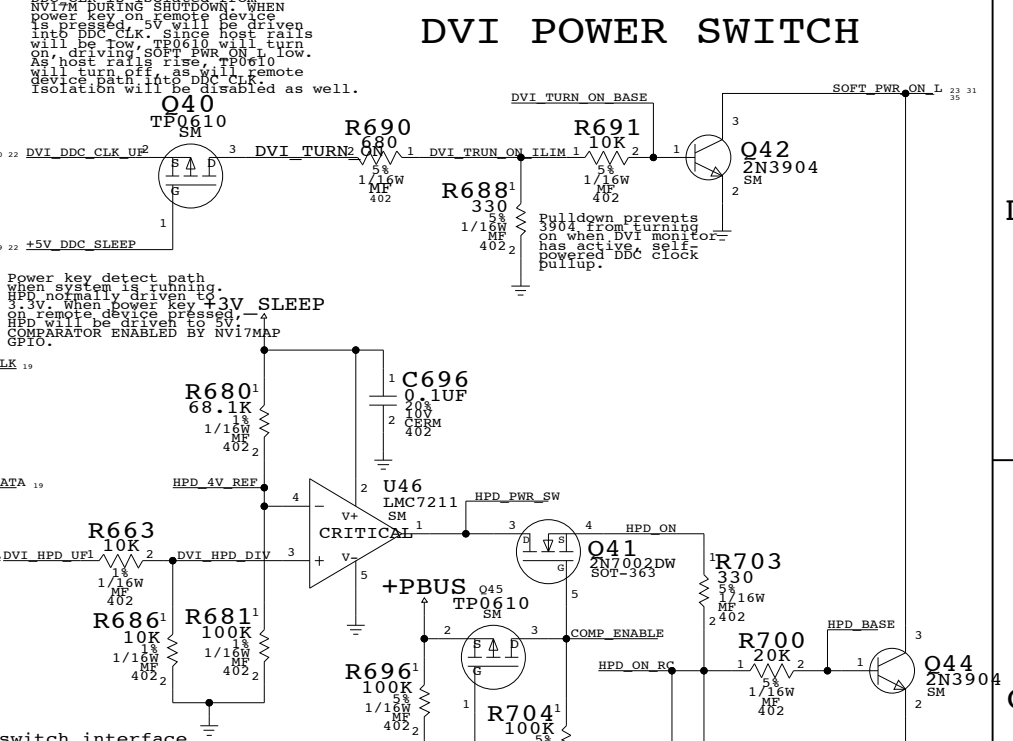
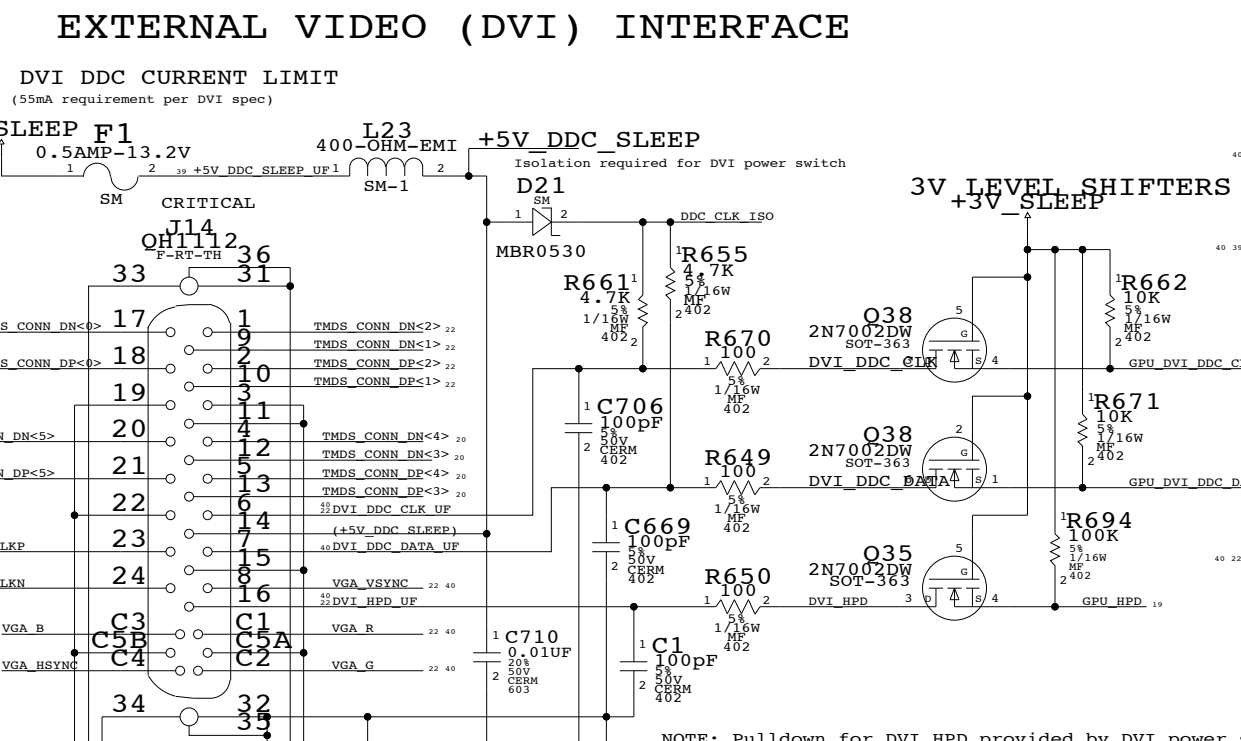
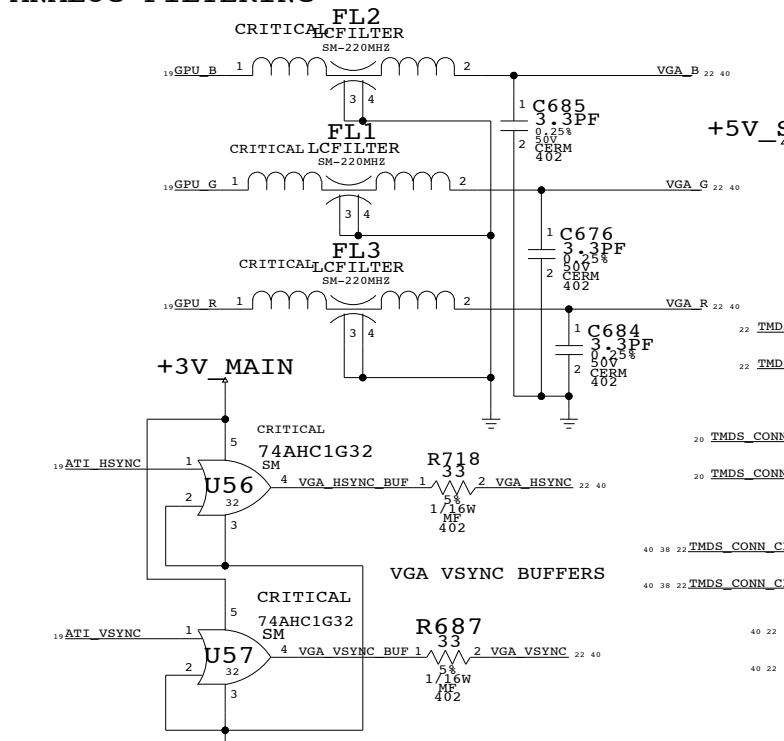
C

B

B

A

A



NOTE: Pull-down for DVI HPD provided by DVI power switch interface
NOTE: DVI HPD SHARES O68 WITH ALS BECAUSE OF BOARD REAL ESTATE

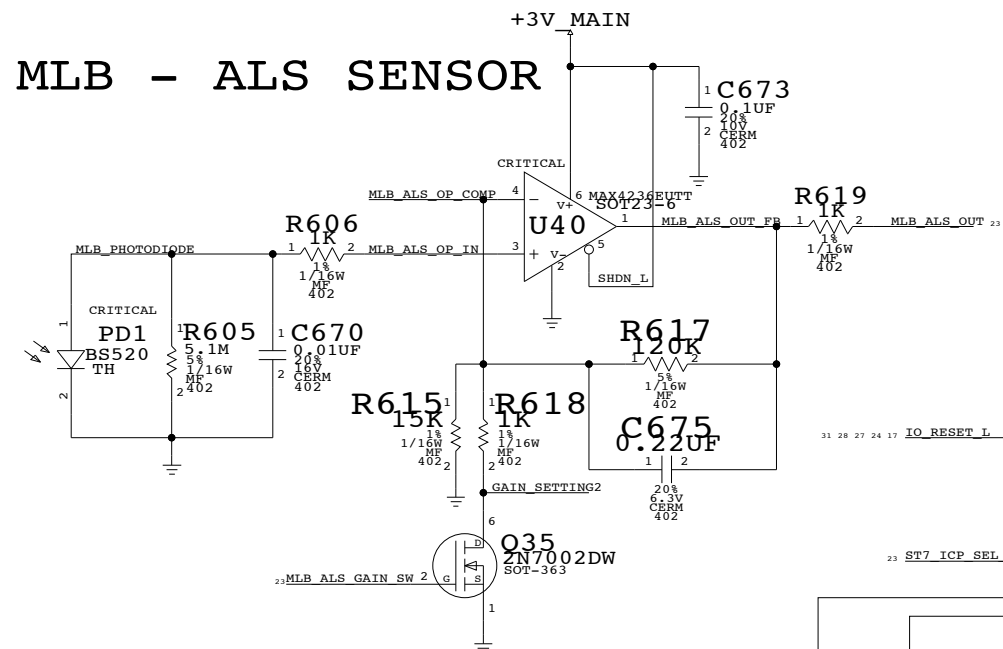
Place GND shorts at graphics controller

Place GND shorts at graphics controller

VIDEO CONNECTORS
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SIZE	D	DRAWING NUMBER	051-6694 B	REV.	
SCALE	NONE	SHT	22	OF	45

MLB - ALS SENSOR

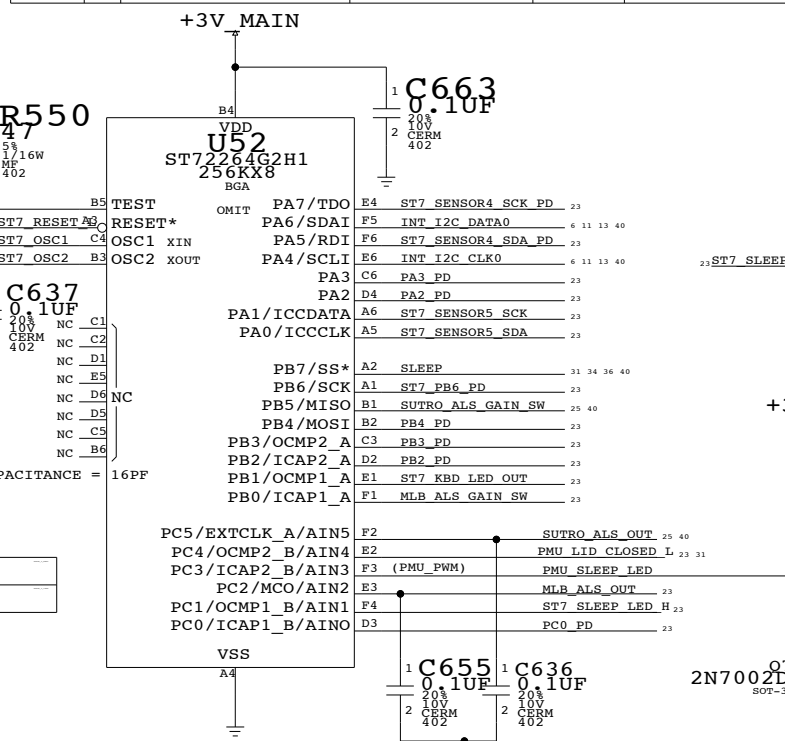


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0856	353S0504	?	U40	ALT FOR SUPPLY PROBLEM

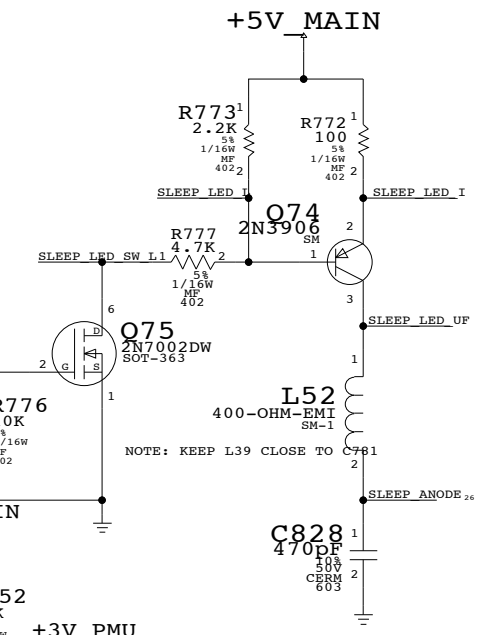
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0091	1	XTAL,CER,LOW PROF,8.000MHZ,8X4.5MM,SMD	Y4	CRITICAL	?

LMU

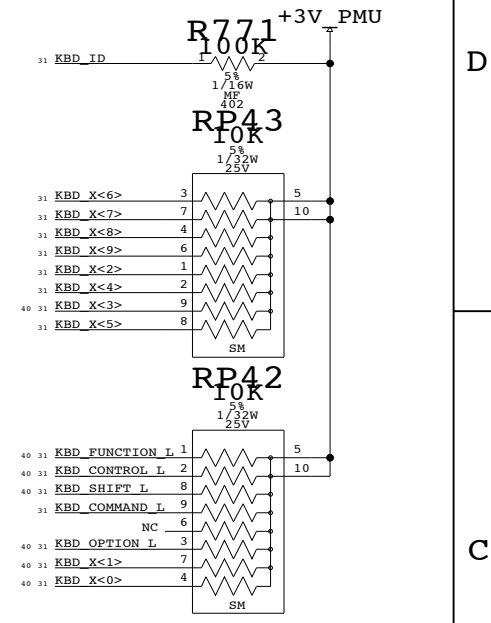
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1194	1	IC,LMU,P84	U52	CRITICAL	?



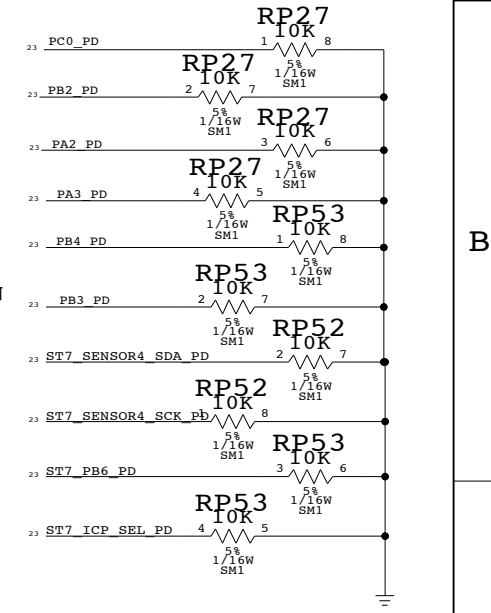
SLEEP LED



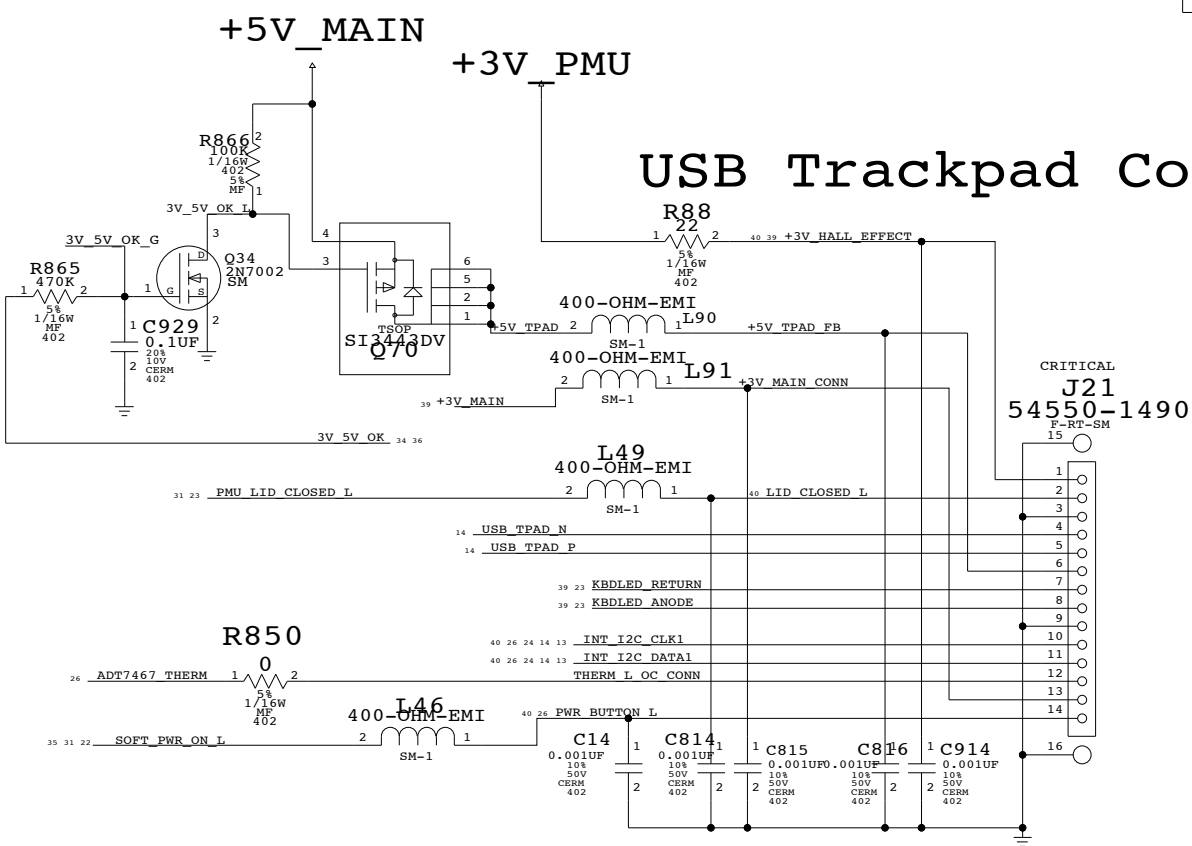
KEYBOARD PULLUPS



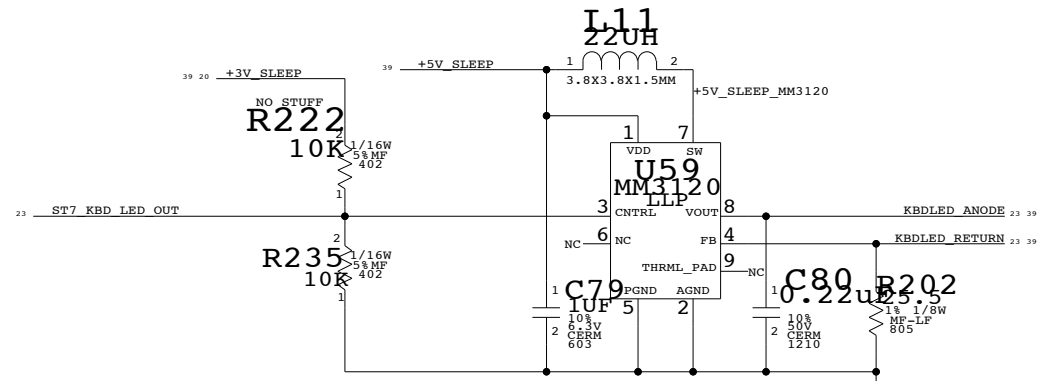
LMU PULL-DOWNS



USB Trackpad Connector



Keyboard LED Driver

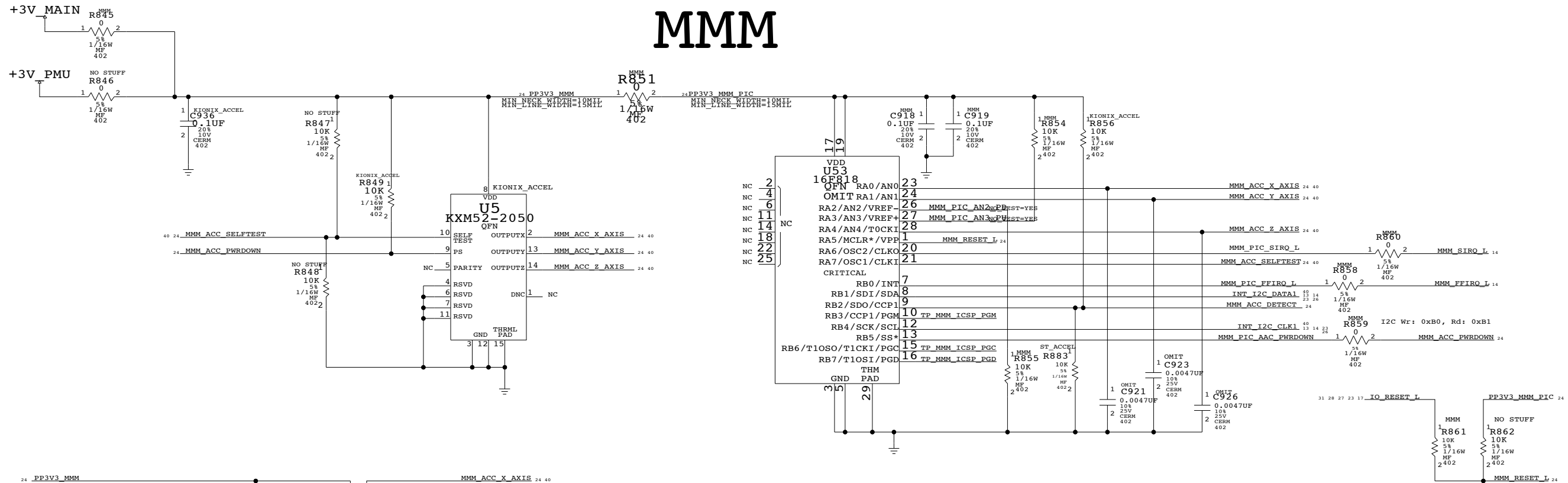


LMU/BOOTBANGER/SPIDEY

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SCALE	SHT	OF	
NONE	23	45	

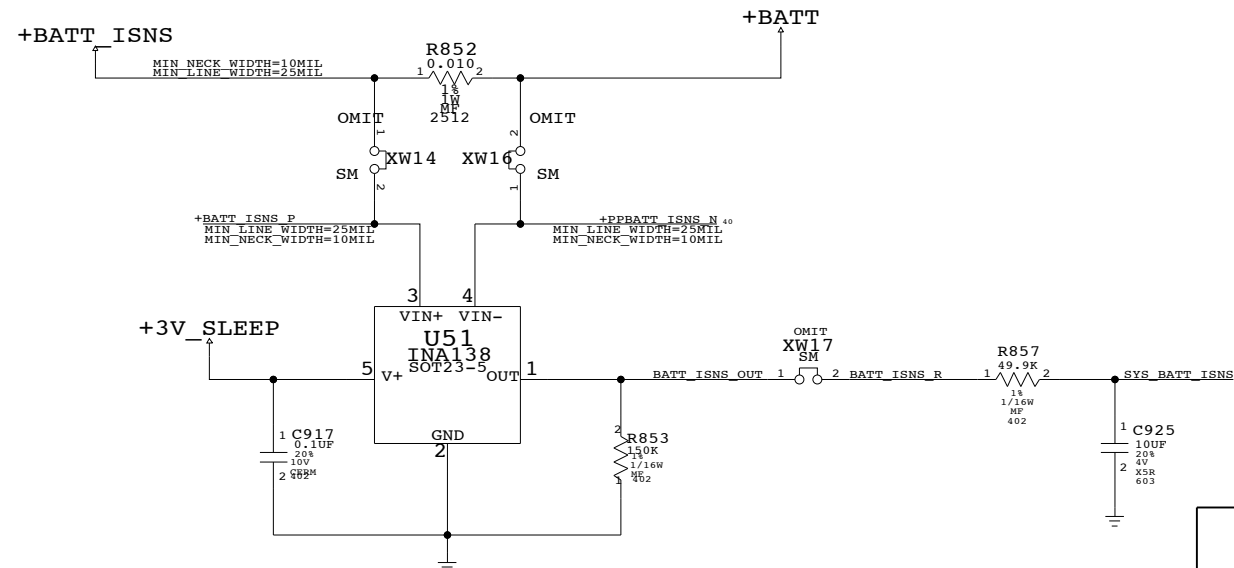
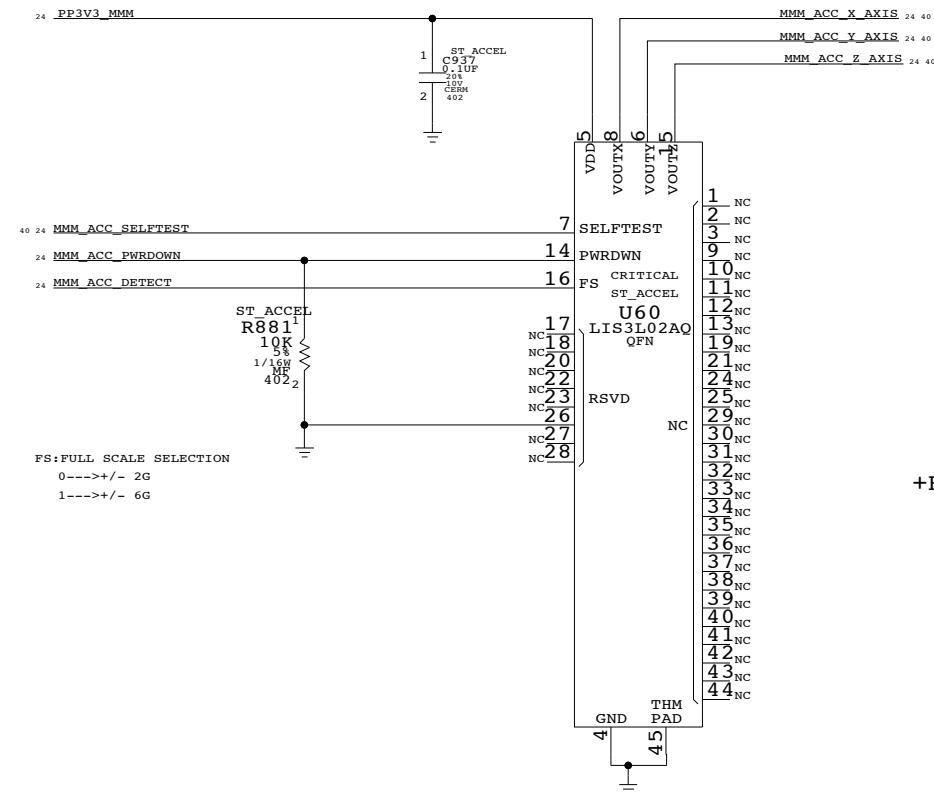
MMM



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S4733	3	CAP CER .0047UF,10%,25V,X7R,0402,SMD	C921,C923,C926	KIONIX_ACCEL
132S0072	3	CAP CER .0015UF,10%,25V,X7R,0402,SMD	C921,C923,C926	ST_ACCEL
341S1630	1	IC,UCTLR,MMM,PIC16F818,SMD,W/PROGRAM	U53	MMM

BOM TABLE USED TO COMPENSATE DIFFERENT OUTPUT RESISTANCE

BATTERY CURRENT SENSE



MMM, BATTERY CURRENT SENSE

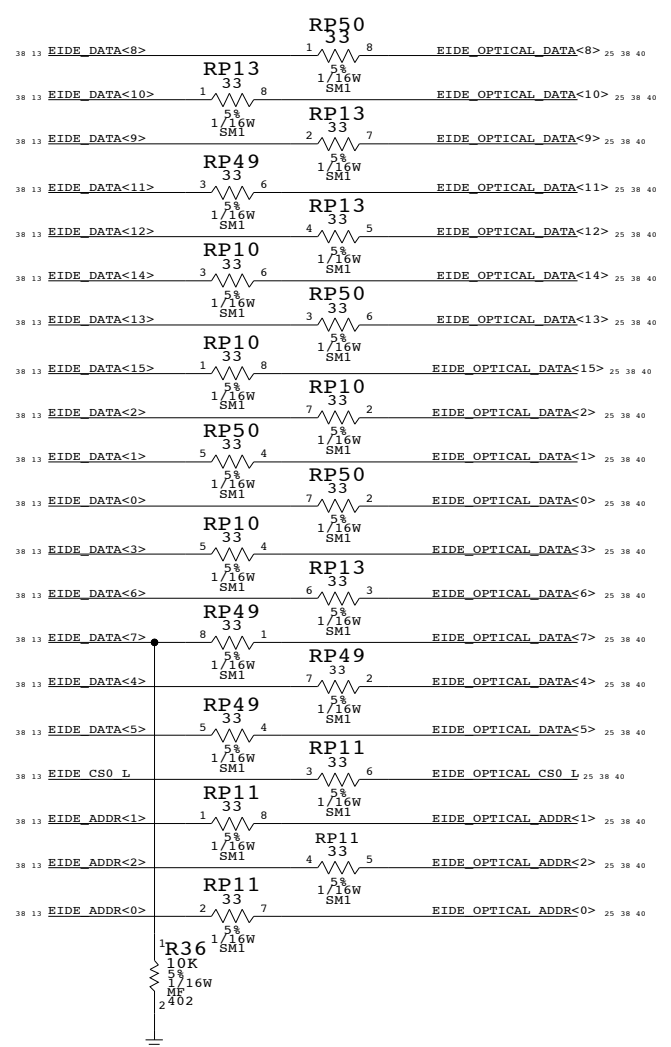
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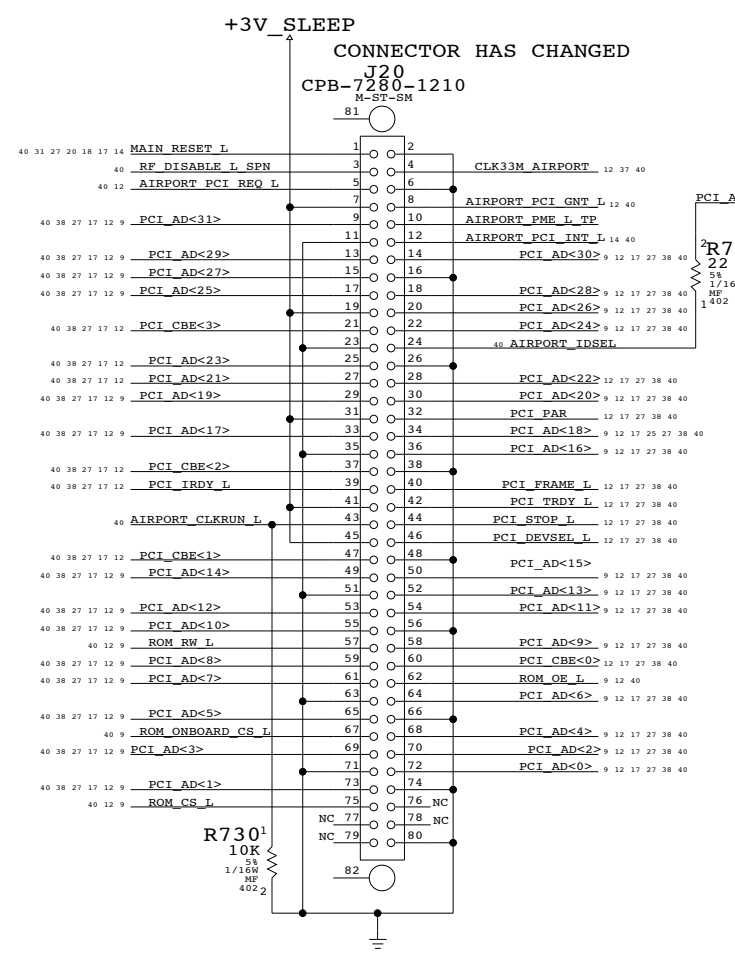
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6694	B
SCALE	SHT	OF	
NONE	24	45	

HARD DRIVE INTERFACE (UATA100)

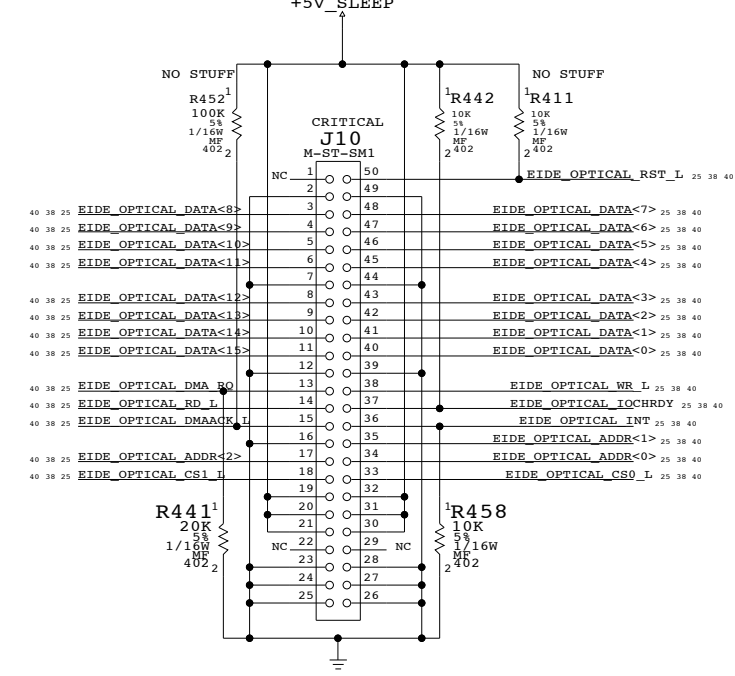
EIDE SERIES TERMINATION PLACE TERMINATORS NEAR INTREPID



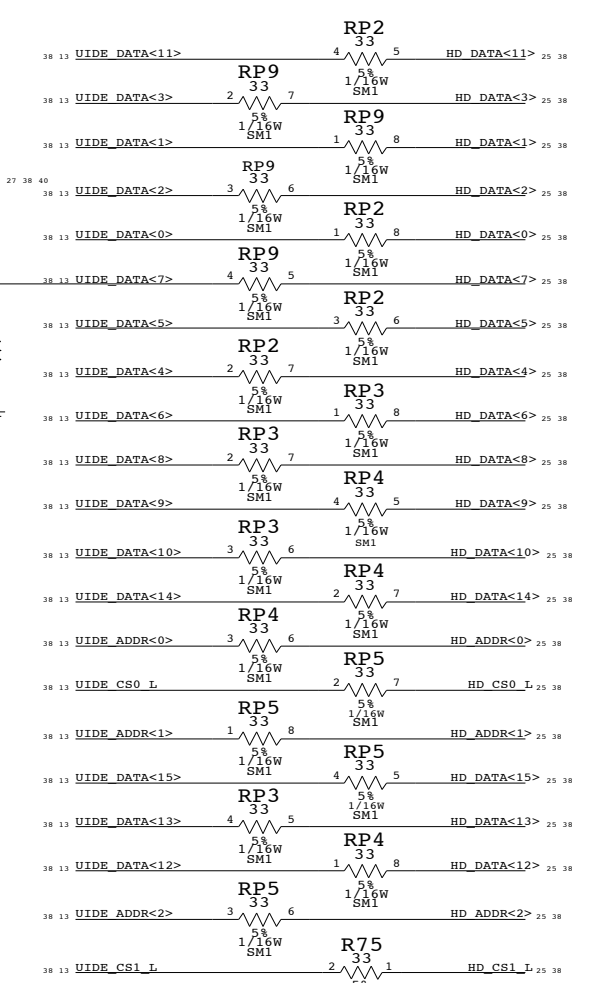
WIRELESS INTERFACE



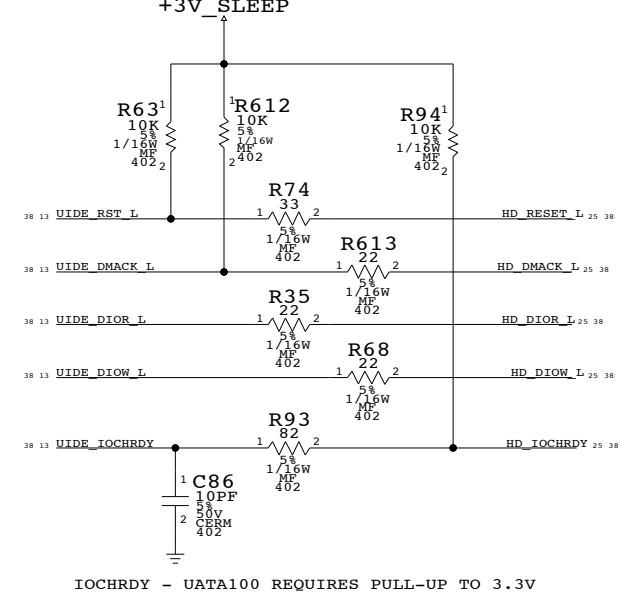
OPTICAL DRIVE INTERFACE (EIDE)



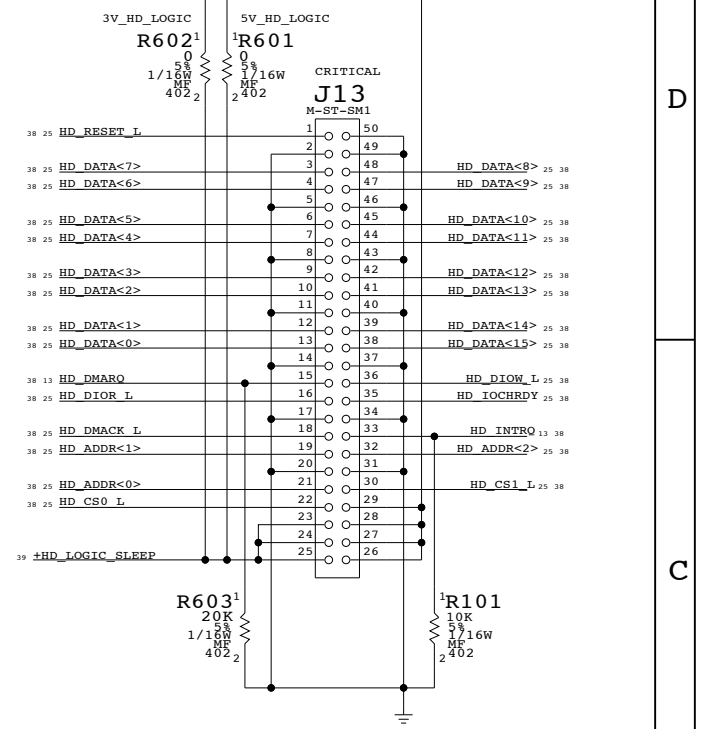
PLACE SERIES R CLOSE TO INTERPID



PLACE PULLUP RESISTORS CLOSE TO INTREPID

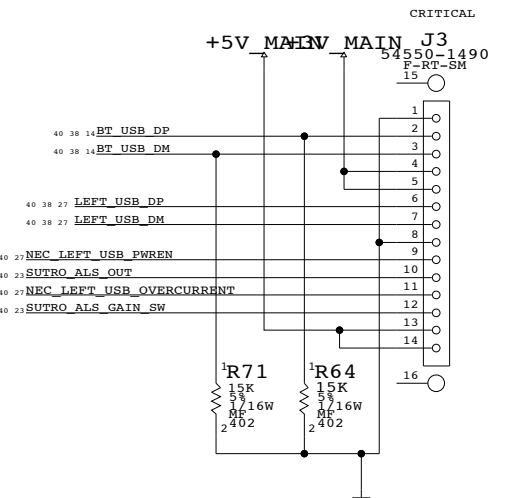


+3V_SLEEP +5V_HD_SLEEP



ANY SEQUENCING REQUIREMENT BETWEEN +5V_HD_SLEEP AND +3V_SLEEP?

BLUETOOTH/LEFT-SIDE USB

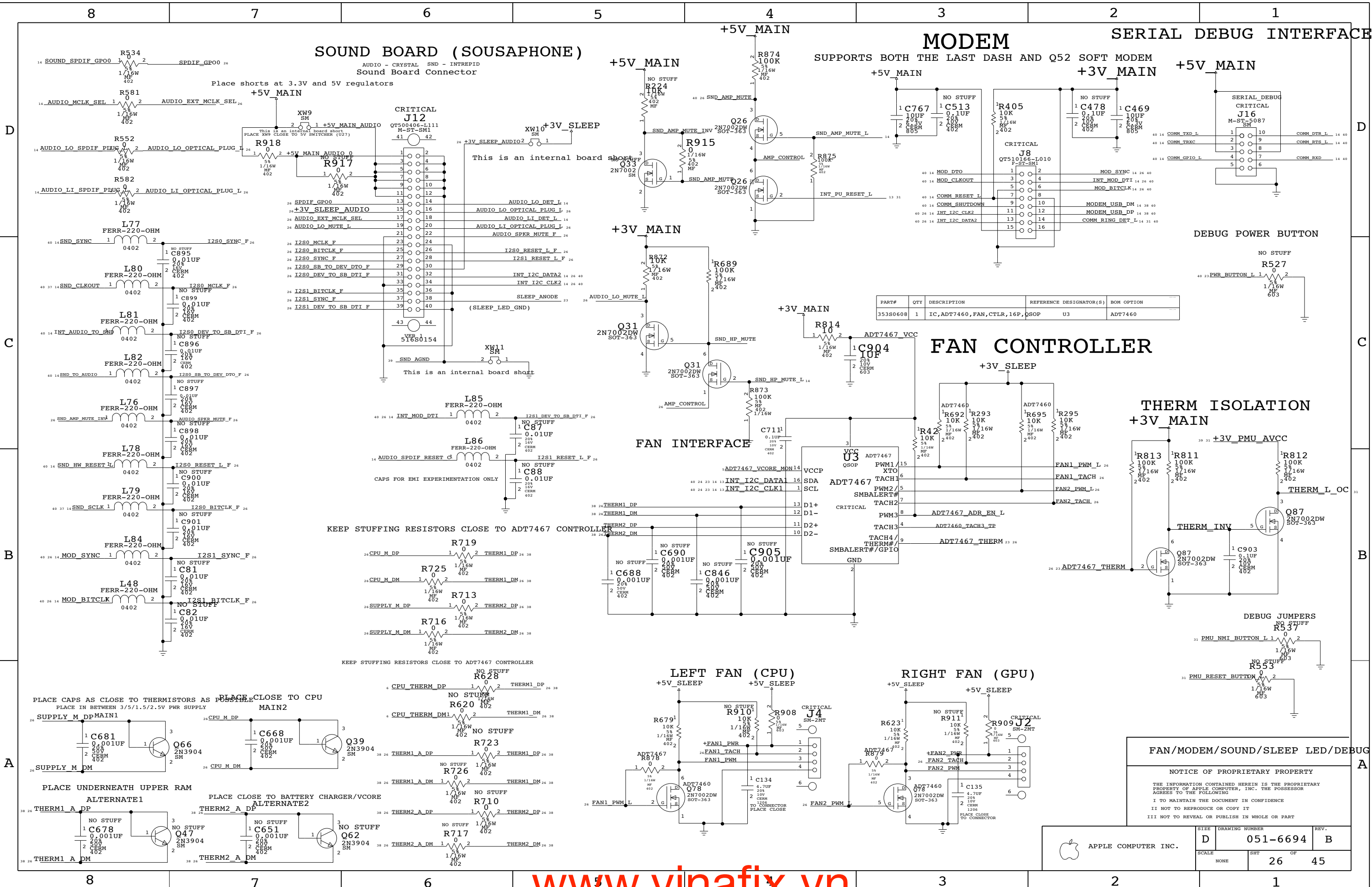


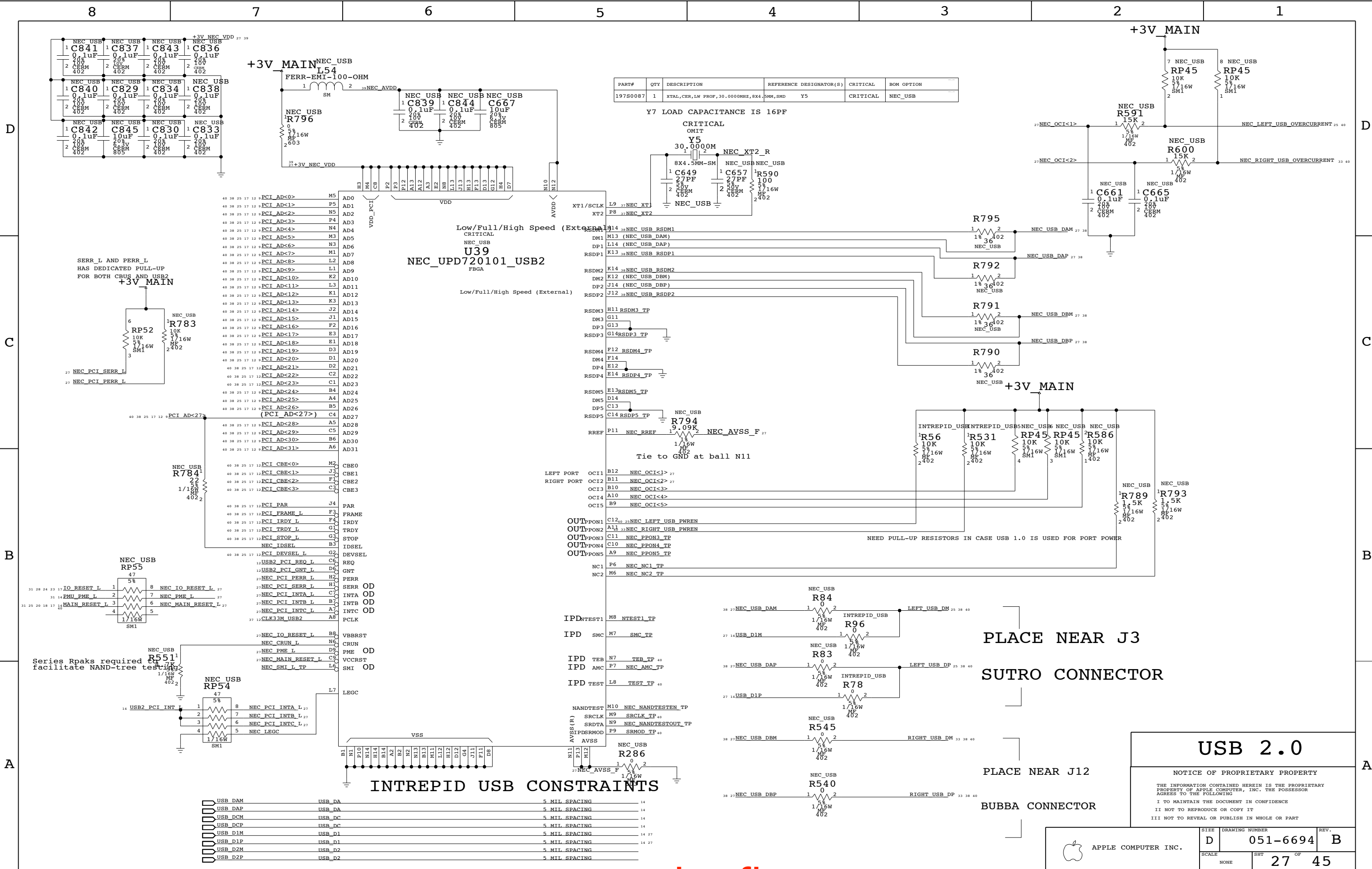
INTERNAL I/O CONNECTORS

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SCALE	SHEET	OF	
NONE	25	45	

IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V





40 38 25 17 12	PCI_AD<0>	M5	AD0
40 38 25 17 12	PCI_AD<1>	P5	AD1
40 38 25 17 12	PCI_AD<2>	N5	AD2
40 38 25 17 12	PCI_AD<3>	P4	AD3
40 38 25 17 12	PCI_AD<4>	N4	AD4
40 38 25 17 12	PCI_AD<5>	M3	AD5
40 38 25 17 12	PCI_AD<6>	N3	AD6
40 38 25 17 12	PCI_AD<7>	M1	AD7
40 38 25 17 12	PCI_AD<8>	L1	AD8
40 38 25 17 12	PCI_AD<9>	K2	AD9
40 38 25 17 12	PCI_AD<10>	L3	AD10
40 38 25 17 12	PCI_AD<11>	K1	AD11
40 38 25 17 12	PCI_AD<12>	K1	AD12
40 38 25 17 12	PCI_AD<13>	K3	AD13
40 38 25 17 12	PCI_AD<14>	J2	AD14
40 38 25 17 12	PCI_AD<15>	J1	AD15
40 38 25 17 12	PCI_AD<16>	F2	AD16
40 38 25 17 12	PCI_AD<17>	E3	AD17
40 38 25 17 12	PCI_AD<18>	D1	AD18
40 38 25 17 12	PCI_AD<19>	D3	AD19
40 38 25 17 12	PCI_AD<20>	D1	AD20
40 38 25 17 12	PCI_AD<21>	D2	AD21
40 38 25 17 12	PCI_AD<22>	C2	AD22
40 38 25 17 12	PCI_AD<23>	C1	AD23
40 38 25 17 12	PCI_AD<24>	B4	AD24
40 38 25 17 12	PCI_AD<25>	A4	AD25
40 38 25 17 12	PCI_AD<26>	B5	AD26
40 38 25 17 12	PCI_AD<27>	C4	AD27
40 38 25 17 12	PCI_AD<28>	A5	AD28
40 38 25 17 12	PCI_AD<29>	C5	AD29
40 38 25 17 12	PCI_AD<30>	B6	AD30
40 38 25 17 12	PCI_AD<31>	A6	AD31
40 38 25 17 12	PCI_CBE<0>	M2	CBE0
40 38 25 17 12	PCI_CBE<1>	J3	CBE1
40 38 25 17 12	PCI_CBE<2>	F1	CBE2
40 38 25 17 12	PCI_CBE<3>	C3	CBE3
40 38 25 17 12	PCI_PAR	J4	PAR
40 38 25 17 12	PCI_FRAME L	F3	FRAME
40 38 25 17 12	PCI_TRDY L	F4	TRDY
40 38 25 17 12	PCI_TRDY L	G1	TRDY
40 38 25 17 12	PCI_STOP L	G3	STOP
40 38 25 17 12	NEC_IDSEL	B3	IDSEL
40 38 25 17 12	PCI_DEVSEL L	G2	DEVSEL
40 38 25 17 12	USB2_PCI_REQ L	C6	REQ
40 38 25 17 12	USB2_PCI_GNT L	D6	GNT
40 38 25 17 12	NEC_PCI_PERR L	H2	PERR
40 38 25 17 12	NEC_PCI_SERR L	H1	SERR
40 38 25 17 12	NEC_PCI_INTA L	C7	INTA
40 38 25 17 12	NEC_PCI_INTB L	B7	INTB
40 38 25 17 12	NEC_PCI_INTC L	A7	INTC
40 38 25 17 12	CLK33M USB2	A8	CLK
40 38 25 17 12	NEC_IO_RESET L	B8	VBRST
40 38 25 17 12	NEC_CRUN L	N6	CRUN
40 38 25 17 12	NEC_PME L	D9	PME
40 38 25 17 12	NEC_MAIN_RESET L	C9	VCCRST
40 38 25 17 12	NEC_SMI L TP	L6	SMI
40 38 25 17 12		L7	LEGC

INTREPID USB CONSTRAINTS

USB DAM	USB_DA	5 MIL SPACING	14
USB DAP	USB_DA	5 MIL SPACING	14
USB DCM	USB_DC	5 MIL SPACING	14
USB DCP	USB_DC	5 MIL SPACING	14
USB D1M	USB_D1	5 MIL SPACING	14 27
USB D1P	USB_D1	5 MIL SPACING	14 27
USB D2M	USB_D2	5 MIL SPACING	14
USB D2P	USB_D2	5 MIL SPACING	14

USB 2.0

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SIZE	D	DRAWING NUMBER	051-6694	REV.	B
SCALE	NONE	SHT	27	OF	45

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
338S0223	338S0079		U49	88EE1111 B1

Ethernet routing priority:
 1. Decoupling caps
 2. TX SERIES TERMINATION - LOCATE NEAR LINK
 3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

PLACE ALL SERIES RES CLOSE TO PHY

$$V_{OUT} = 0.8V * (1 + R2EQV / R1)$$

$$R2EQV = R2A || R2B$$

PLACE CLOSE TO ETHERNET CONNECTOR

Short shielded RJ-45

CONFIG DEFINITIONS

PIN	BIT[2:0]
VDDO	111
LED LINK10	110
LED LINK100	101
LED LINK1000	100
LED DUPLEX	011
LED RX	010
LED TX	001
VSS	000

CONFIG INPUTS

PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>PHYADR[2]	PHYADR[1]	PHYADR[0]	
CONFIG<1>ENA PAUSE	PHYADR[4]	PHYADR[3]	
CONFIG<2>ANEG[3]	ANEG[2]	ANEG[1]	
CONFIG<3>ANEG[0]	ENA XC	DIS 125	
CONFIG<4>MODE[2]	MODE[1]	MODE[0]	
CONFIG<5>DIS FC	DIS SLEEP	MODE[3]	
CONFIG<6>SEL BDT	INT POL	75/50 OHM	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0086	1	XTAL, CER, 25MHZ, .005%, 20PF, 8X4.5MM, SMD	Y3	CRITICAL	?

MARVELL 88E1111
10/100/1000 ETHERNET

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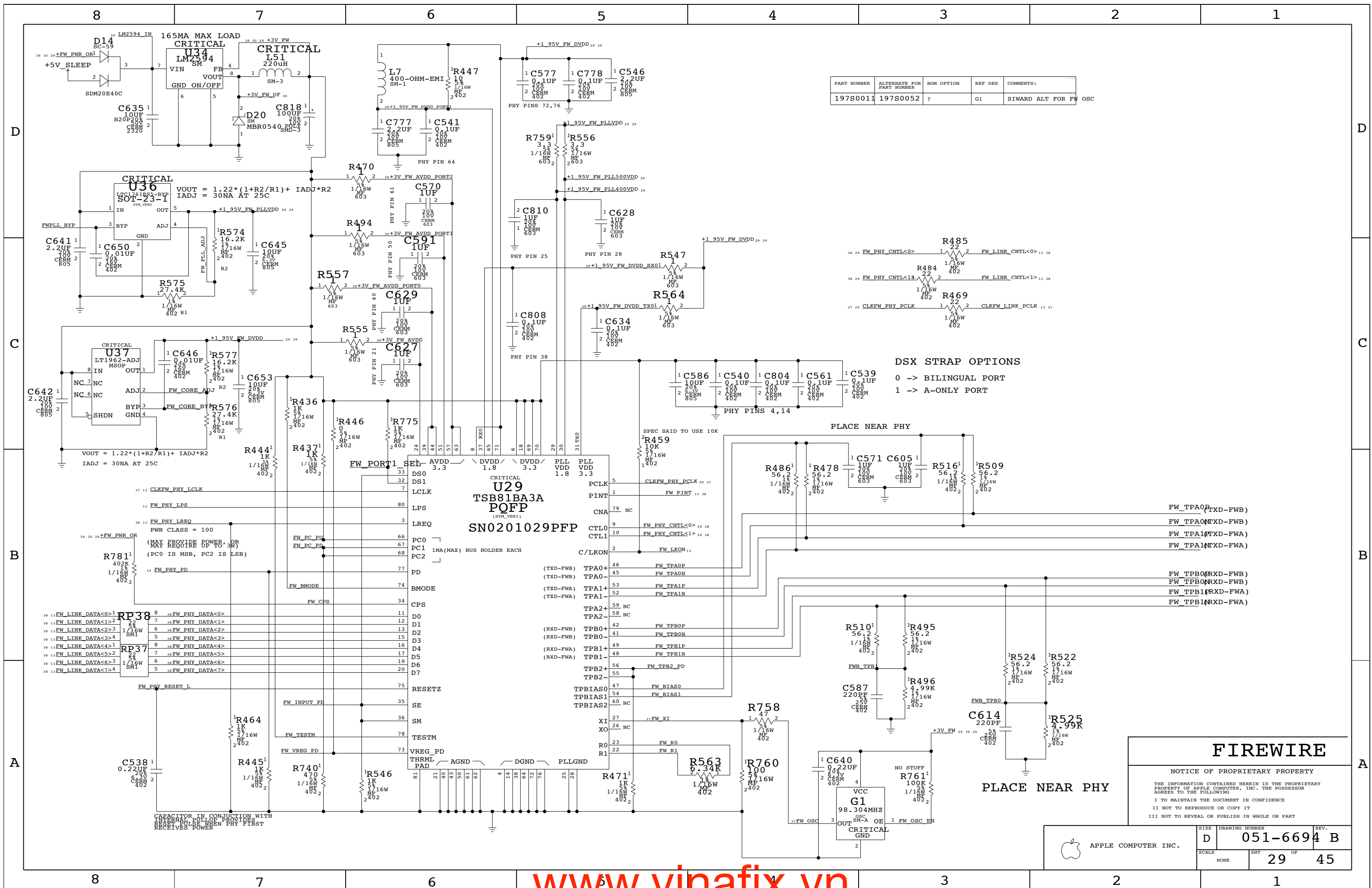
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6694	B
SCALE	NONE	SHT	28 OF 45



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
197S0011	197S0052	?	G1	SIWARD ALT FOR FW OSC

DSX STRAP OPTIONS
 0 -> BILINGUAL PORT
 1 -> A-ONLY PORT

FIREWIRE

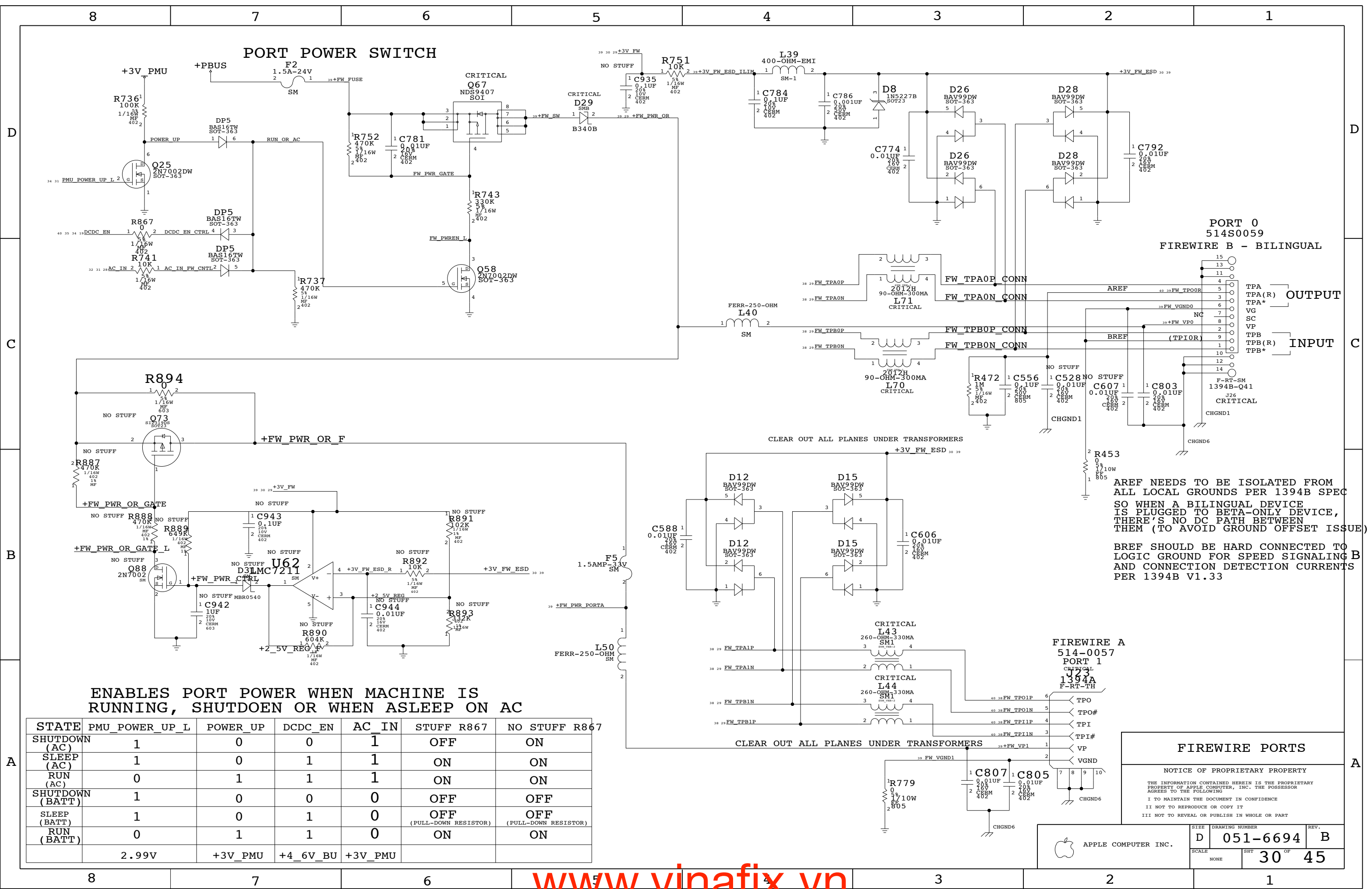
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6694	B
SCALE	SHT	OF	
NONE	29	45	

PORT POWER SWITCH



ENABLES PORT POWER WHEN MACHINE IS RUNNING, SHUTDOWN OR WHEN ASLEEP ON AC

STATE	PMU_POWER_UP_L	POWER_UP	DCDC_EN	AC_IN	STUFF R867	NO STUFF R867
SHUTDOWN (AC)	1	0	0	1	OFF	ON
SLEEP (AC)	1	0	1	1	ON	ON
RUN (AC)	0	1	1	1	ON	ON
SHUTDOWN (BATT)	1	0	0	0	OFF	OFF
SLEEP (BATT)	1	0	1	0	OFF	OFF
RUN (BATT)	0	1	1	0	ON	ON
	2.99V	+3V_PMU	+4_6V_BU	+3V_PMU	(PULL-DOWN RESISTOR)	(PULL-DOWN RESISTOR)

AREF NEEDS TO BE ISOLATED FROM ALL LOCAL GROUNDS PER 1394B SPEC SO WHEN A BILINGUAL DEVICE IS PLUGGED TO BETA-ONLY DEVICE, THERE'S NO DC PATH BETWEEN THEM (TO AVOID GROUND OFFSET ISSUE)

BREF SHOULD BE HARD CONNECTED TO LOGIC GROUND FOR SPEED SIGNALING B AND CONNECTION DETECTION CURRENTS PER 1394B V1.33

FIREWIRE PORTS

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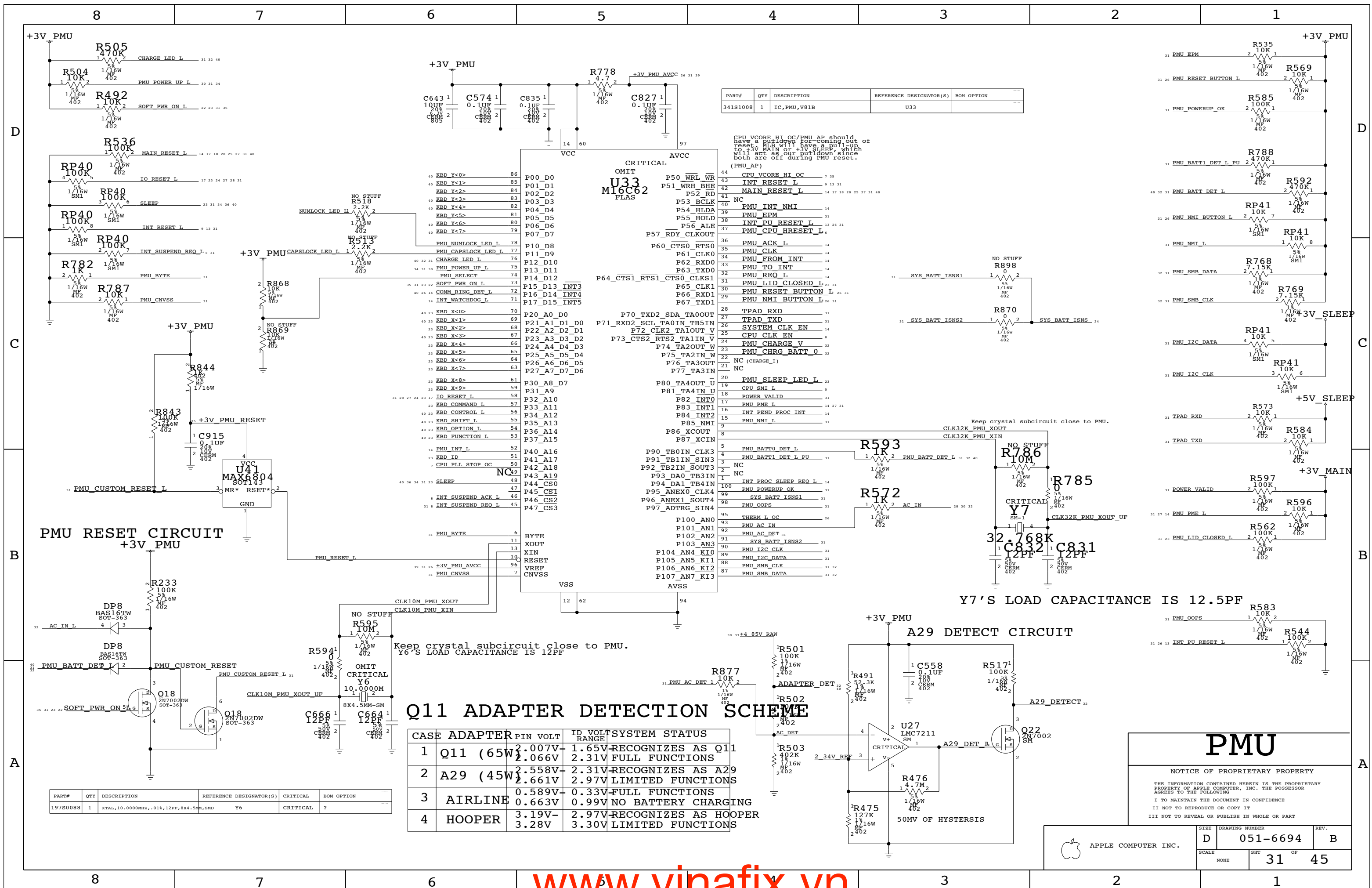
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APPLE COMPUTER INC.

SIZE: D, DRAWING NUMBER: 051-6694, REV. B

SCALE: NONE, SHT: 30 OF 45

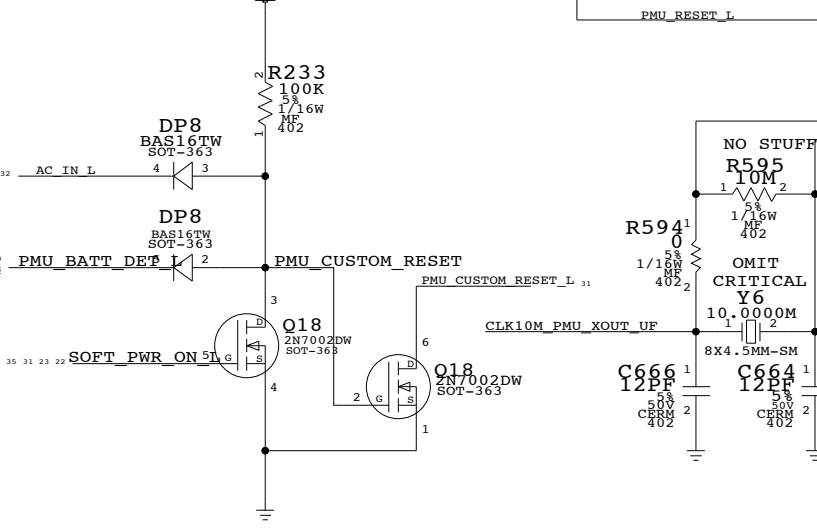


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1008	1	IC,PMU,V81B	U33	

CPU VCORE HI_OC/PMU AP should have a pull-up resistor coming out of reset. MIB will have a pull-up to +5V MAIN or +3V SLEEP, which will act as our pull-down since both are off during PMU reset.

Pin	Signal	Pin	Signal
86	P00_D0	7	CPU_VCORE_HI_OC
85	P01_D1	9	INT_RESET_L
84	P02_D2	14	MAIN_RESET_L
83	P03_D3	41	NC
82	P04_D4	40	PMU_INT_NMI
81	P05_D5	39	PMU_EP
80	P06_D6	38	INT_PU_RESET_L
79	P07_D7	37	PMU_CPU_HRESET_L
78	PMU_NUMLOCK_LED_L	36	PMU_ACK_L
77	PMU_CAPSLOCK_LED_L	35	PMU_CLK
76	CHARGE_LED_L	34	PMU_FROM_INT
75	PMU_POWER_UP_L	33	PMU_TO_INT
74	PMU_SELECT	32	PMU_REQ_L
73	SOFT_PWR_ON_L	31	PMU_LID_CLOSED_L
72	COMM_RING_DET_L	30	PMU_RESET_BUTTON_L
71	INT_WATCHDOG_L	29	PMU_NMI_BUTTON_L
70	KBD_X<0>	28	TPAD_RXD
69	KBD_X<1>	27	TPAD_TXD
68	KBD_X<2>	26	SYSTEM_CLK_EN
67	KBD_X<3>	25	CPU_CLK_EN
66	KBD_X<4>	24	PMU_CHRG_V
65	KBD_X<5>	23	PMU_CHRG_BATT_0
64	KBD_X<6>	22	NC (CHARGE_I)
63	KBD_X<7>	21	NC
61	KBD_X<8>	20	PMU_SLEEP_LED_L
59	KBD_X<9>	19	CPU_SMI_L
58	IO_RESET_L	18	POWER_VALID
57	KBD_COMMAND_L	17	PMU_PME_L
56	KBD_CONTROL_L	16	INT_PEND_PROC_INT
55	KBD_SHIFT_L	15	PMU_NMI_L
54	KBD_OPTION_L	9	PMU_NMI_L
53	KBD_FUNCTION_L	8	P86_XCOUT
52	P40_A16	8	P87_XCIN
51	KBD_ID	5	PMU_BATT0_DET_L
50	CPU_PIL_STOP_OC	4	PMU_BATT1_DET_L_PU
49	NC	3	NC
48	SLEEP	2	NC
47	P44_CS0	1	INT_PROC_SLEEP_REQ_L
46	P45_CSI	100	PMU_POWERUP_OK
45	INT_SUSPEND_ACK_L	99	SYS_BATT_ISNS1
44	INT_SUSPEND_REQ_L	98	PMU_OOPS
43	PMU_BYTE	95	THERM_I_OC
42	PMU_BYTE	93	PMU_AC_IN
41	PMU_BYTE	92	PMU_AC_DET
40	PMU_BYTE	91	SYS_BATT_ISNS2
39	PMU_BYTE	90	PMU_I2C_CLK
38	PMU_BYTE	89	PMU_I2C_DATA
37	PMU_BYTE	88	PMU_SMB_CLK
36	PMU_BYTE	87	PMU_SMB_DATA
35	PMU_BYTE	87	PMU_SMB_DATA
34	PMU_BYTE	87	PMU_SMB_DATA
33	PMU_BYTE	87	PMU_SMB_DATA
32	PMU_BYTE	87	PMU_SMB_DATA
31	PMU_BYTE	87	PMU_SMB_DATA
30	PMU_BYTE	87	PMU_SMB_DATA
29	PMU_BYTE	87	PMU_SMB_DATA
28	PMU_BYTE	87	PMU_SMB_DATA
27	PMU_BYTE	87	PMU_SMB_DATA
26	PMU_BYTE	87	PMU_SMB_DATA
25	PMU_BYTE	87	PMU_SMB_DATA
24	PMU_BYTE	87	PMU_SMB_DATA
23	PMU_BYTE	87	PMU_SMB_DATA
22	PMU_BYTE	87	PMU_SMB_DATA
21	PMU_BYTE	87	PMU_SMB_DATA
20	PMU_BYTE	87	PMU_SMB_DATA
19	PMU_BYTE	87	PMU_SMB_DATA
18	PMU_BYTE	87	PMU_SMB_DATA
17	PMU_BYTE	87	PMU_SMB_DATA
16	PMU_BYTE	87	PMU_SMB_DATA
15	PMU_BYTE	87	PMU_SMB_DATA
14	PMU_BYTE	87	PMU_SMB_DATA
13	PMU_BYTE	87	PMU_SMB_DATA
12	PMU_BYTE	87	PMU_SMB_DATA
11	PMU_BYTE	87	PMU_SMB_DATA
10	PMU_BYTE	87	PMU_SMB_DATA
9	PMU_BYTE	87	PMU_SMB_DATA
8	PMU_BYTE	87	PMU_SMB_DATA
7	PMU_BYTE	87	PMU_SMB_DATA
6	PMU_BYTE	87	PMU_SMB_DATA
5	PMU_BYTE	87	PMU_SMB_DATA
4	PMU_BYTE	87	PMU_SMB_DATA
3	PMU_BYTE	87	PMU_SMB_DATA
2	PMU_BYTE	87	PMU_SMB_DATA
1	PMU_BYTE	87	PMU_SMB_DATA

PMU RESET CIRCUIT



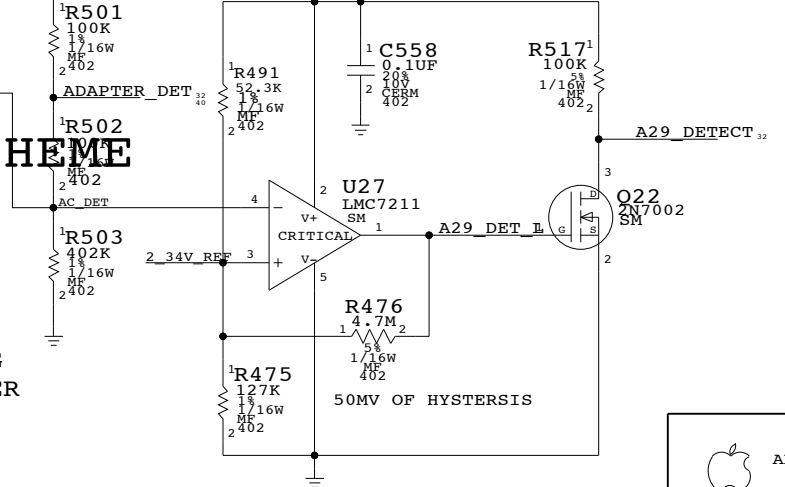
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0088	1	XTAL,10.0000MHZ,-013,12PF,8X4.5MM,SMD	Y6	CRITICAL	?

Q11 ADAPTER DETECTION SCHEME

CASE	ADAPTER	PIN VOLT	ID VOLT RANGE	SYSTEM STATUS
1	Q11 (65W)	2.007V 2.066V	1.65V 2.31V	RECOGNIZES AS Q11 FULL FUNCTIONS
2	A29 (45W)	2.558V 2.661V	2.31V 2.97V	RECOGNIZES AS A29 LIMITED FUNCTIONS
3	AIRLINE	0.589V 0.663V	0.33V 0.99V	FULL FUNCTIONS NO BATTERY CHARGING
4	HOOPER	3.19V- 3.28V	2.97V 3.30V	RECOGNIZES AS HOOPER LIMITED FUNCTIONS

Y7'S LOAD CAPACITANCE IS 12.5PF

A29 DETECT CIRCUIT



PMU

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	NONE	31	OF	B

DC POWER INPUT

(POWER JACK, ETC. ON SEPARATE BOARD)
CRITICAL

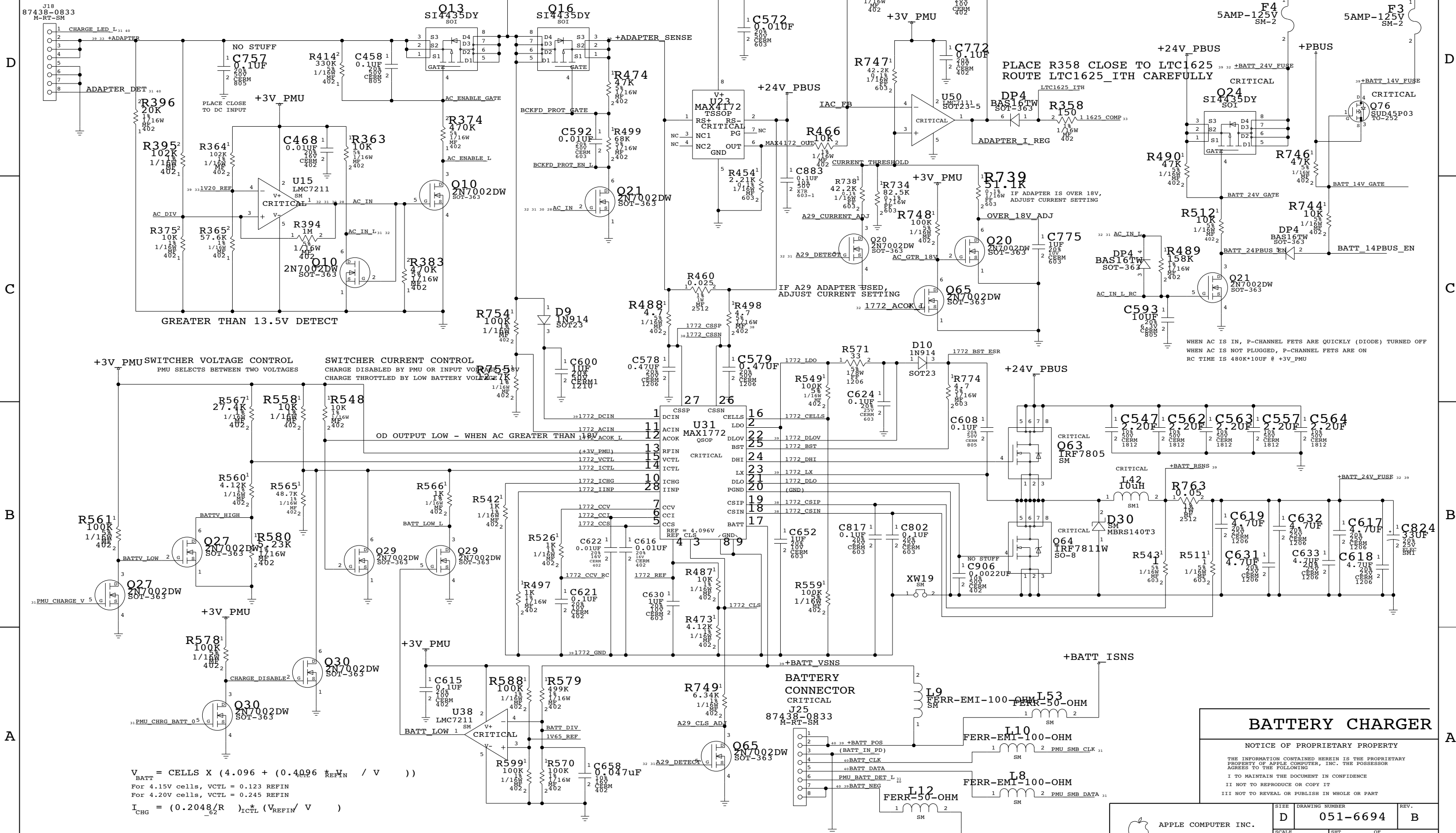
DC INRUSH LIMITER

PLACE U23 NEXT TO R460
U23 SENSE VOLTAGE DROP ACROSS R460

1MSEC INTEGRATION TIME

BATTERY SWITCH-OVER CIRCUIT

+BATT



$$V_{BATT} = CELLS \times (4.096 + (0.4096 \frac{R_{REFIN}}{V}))$$

For 4.15V cells, $V_{CTRL} = 0.123 \frac{R_{REFIN}}$
 For 4.20V cells, $V_{CTRL} = 0.245 \frac{R_{REFIN}}$

$$I_{CHG} = (0.2048/R_{ICL}) * (V_{REFIN}/V)$$

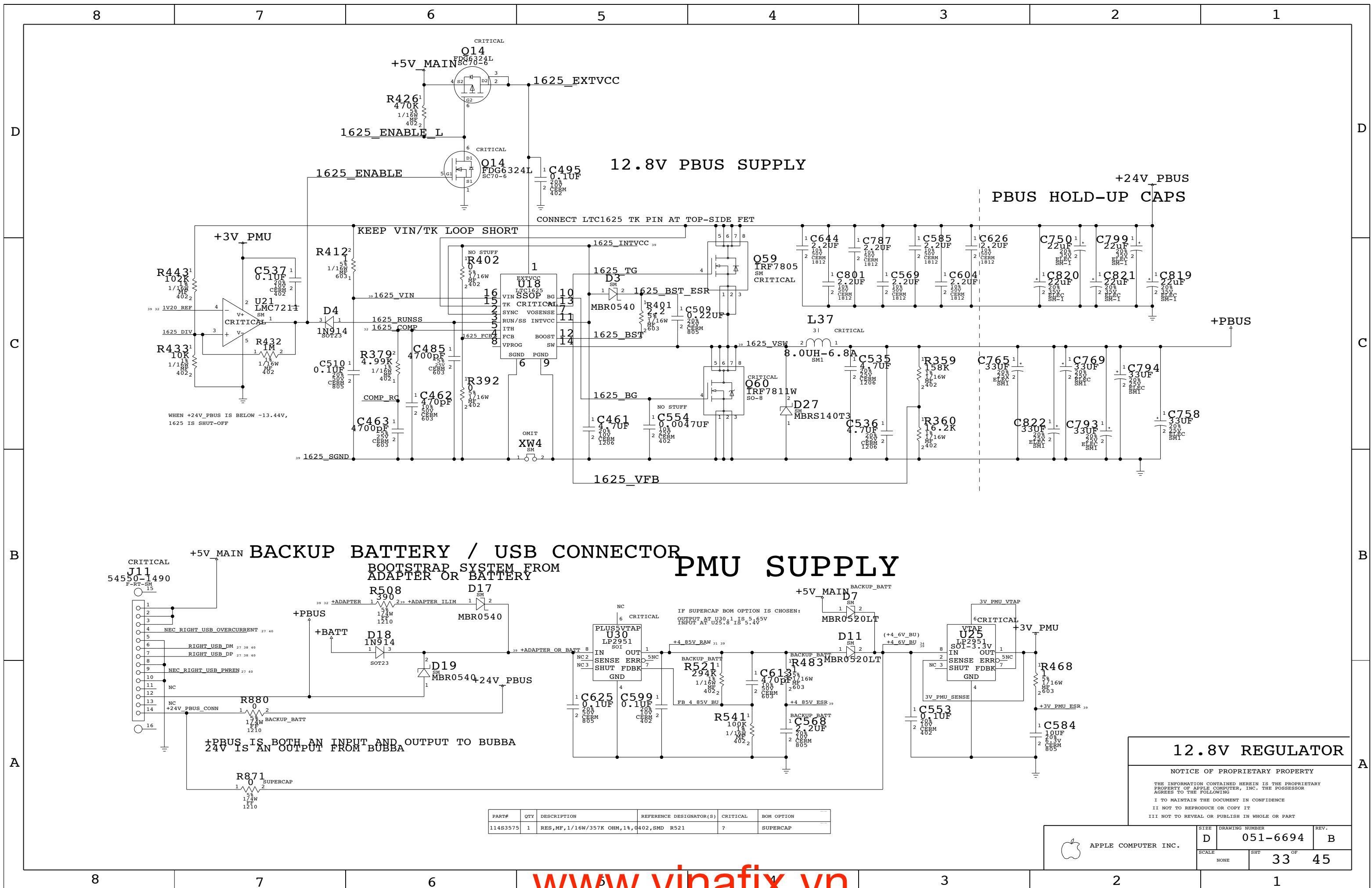
BATTERY CHARGER

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	D	051-6694	B
SCALE	SHT	OF	
NONE	32	45	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
11483575	1	RES, MF, 1/16W/357K OHM, 1%, 0402, SMD	R521	?	SUPERCAP

12.8V REGULATOR

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APPLE COMPUTER INC.

SCALE: NONE

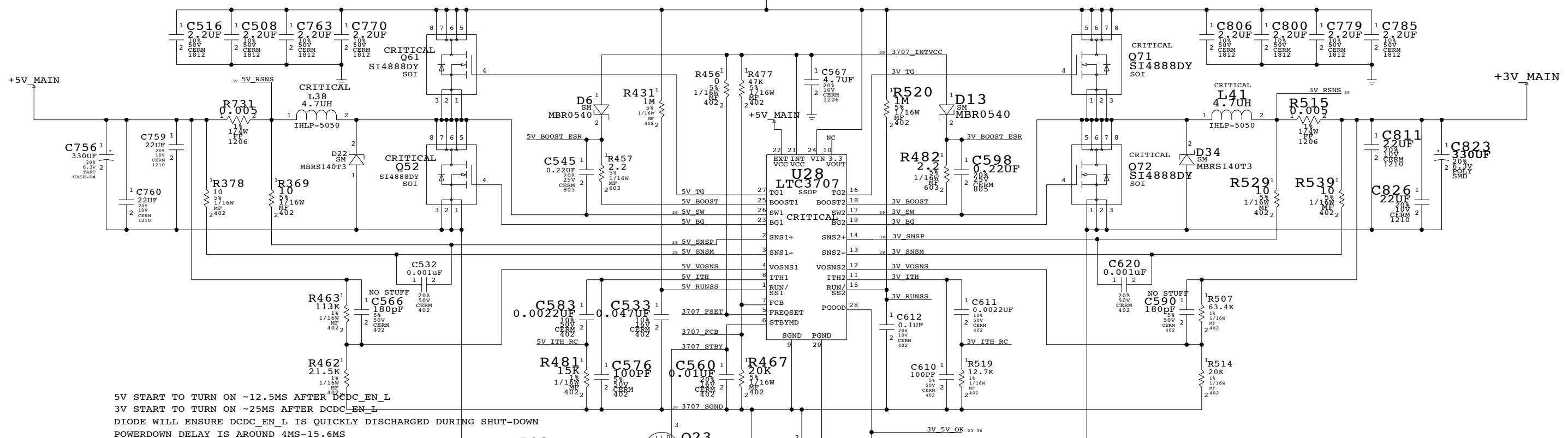
DRAWING NUMBER: 051-6694

SHT: 33 OF 45

REV: B

3.3V/5V MAIN SUPPLY

+24V PBUS



5V START TO TURN ON ~12.5MS AFTER DCDC_EN_L
 3V START TO TURN ON ~25MS AFTER DCDC_EN_L
 DIODE WILL ENSURE DCDC_EN_L IS QUICKLY DISCHARGED DURING SHUT-DOWN
 POWERDOWN DELAY IS AROUND 4MS-15.6MS

THERE'S NO 10UF INPUT CAP BECAUSE Q21 IS PLACED AT OUTPUT OF +3V_MAIN SWITCHER

DCDC_EN TRUTH TABLE

PMU_POWER_UP	SLEEP	DCDC_EN	DCDC_EN_L	State
0	0	1	0	Run
1 (2.99V)	1	1	0	Sleep
1	0	0	1	Shutdown

+3V_PMU +3V_PMU+4_6V_BU +3V_PMU VOLTAGE

- +5V_SLEEP LOADS
- 1) OPTICAL DRIVE
 - 2) DVI
 - 3) TRACKPAD
 - 4) FANS
 - 5) FIREWIRE PHY

- +3V_SLEEP LOADS
- 1) CPU PLL Config Control
 - 2) INTREPID - IIC AND PCI PULL-UPS
 - 3) MAP31 - 3V RAIL (IF USING D3COLD)
 - 4) GRAPHIC CHIP SPREAD SPECTRUM CHIP
 - 5) LVDS DDC PULL-UPS
 - 6) DVI LEVEL SHIFTERS & PULL-UPS & HPD
 - 7) SOUND BOARD
 - 8) BOOT BANGER
 - 9) HARD DRIVE (IF USING 3V LOGIC)
 - 10) WIRELESS (IF POWERING OFF IN SLEEP)
 - 11) PMU - IIC Pull-ups
 - 12) PCI PULL-UPS

3.3V/5V REGULATOR

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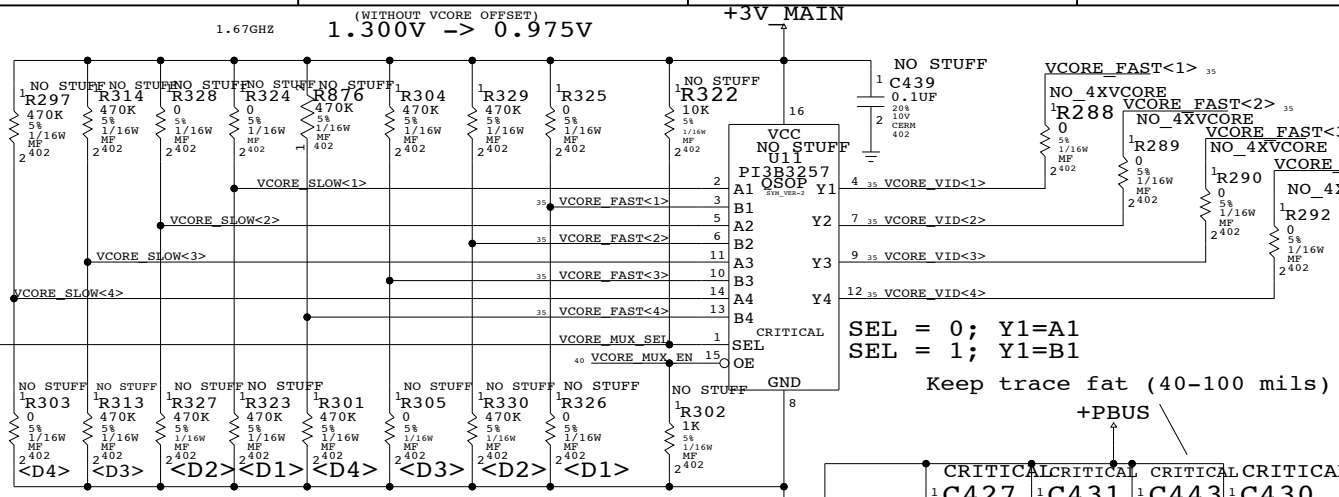
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	D	051-6694	B
SCALE	SHT	OF	
NONE	34	45	

VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage (approx. 7ms delay)

+5V MAIN



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S0242	1	IND,PWR,1.0UH,20,20.5A,SMD	L36	CRITICAL	

D

D

C

C

B

B

A

A

OUTPUT VOLTAGE

V _{DAC}	D3	D2	D1	D0
2.00	1	2	3	4
1.95	1	2	0	1
1.90	1	2	0	0
1.85	1	2	1	1
1.80	1	2	1	0
1.75	1	2	0	1
1.70	1	2	1	0
1.65	1	2	1	1
1.60	1	2	0	0
1.55	1	2	0	1
1.50	1	2	1	0
1.45	1	2	1	1
1.40	1	2	1	0
1.35	1	2	1	1
1.30	1	2	1	0
NO CPU	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ =	
	Hi/Fast	Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
 When A/B_ is low (slow): <=1K-ohm -> 0
 >=100K-ohm -> 1

If all pull-ups are >=100K and all pull-downs are <=1K, VB = V

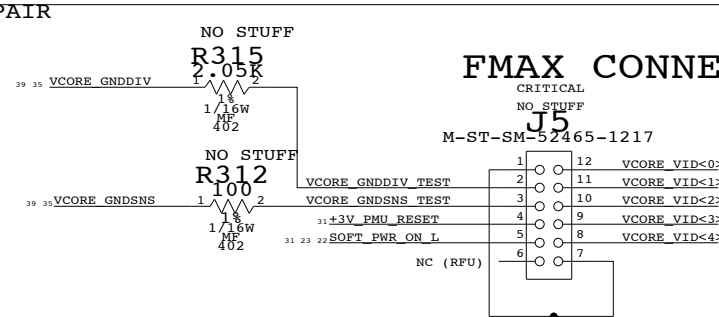
GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
 $V_{REF} = 2.0V$ WITH A 0.85 SCALE FACTOR, HENCE $V_{OFFSET} = 1.7V * (R1/(R1+R2))$ AND $V_{CORE} = V_{DAC} + V_{OFFSET}$.

NOTE: R310 (R2) NO STUFFED FOR NO OFFSET CASE

ROUTE AS DIFFERENTIAL PAIR

1.67GHZ 1.320V -> 0.990V
 (CPU SPEC: 1.280V -> 0.980V)



FMAX CONNECTOR

M-ST-SM-52465-1217

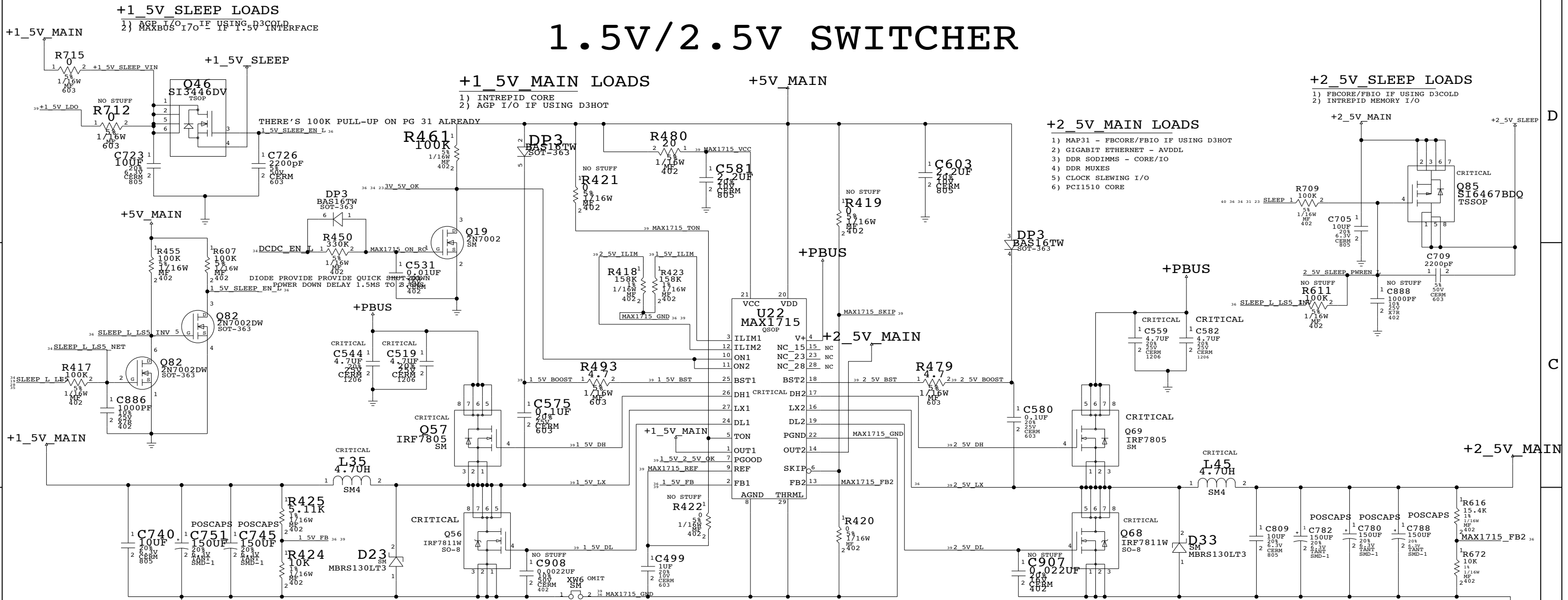
VCORE SUPPLY

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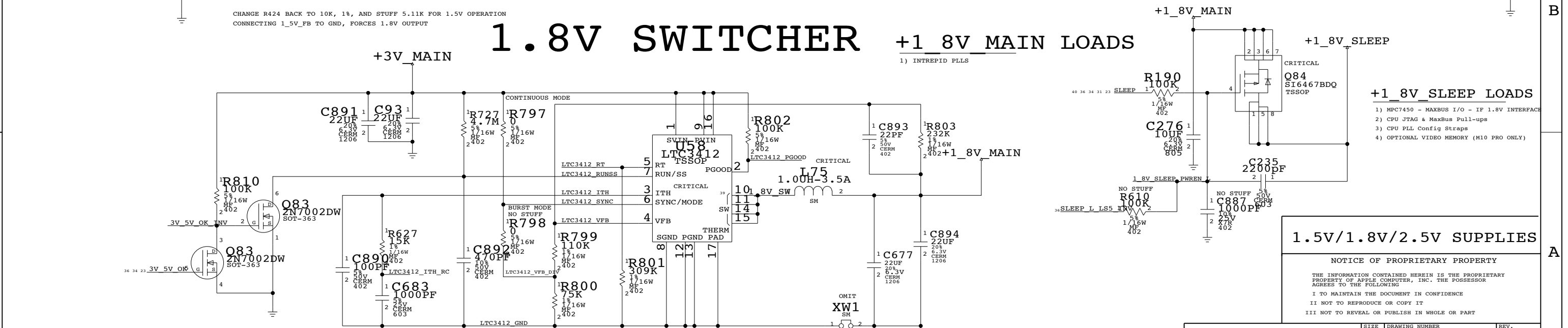
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	D	051-6694 B	
SCALE	SHT	OF	
NONE	35	45	

1.5V/2.5V SWITCHER



1.8V SWITCHER



APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6694	B
SCALE	SHT	OF	
NONE	36	45	

FUNCTIONAL TEST POINTS

8	7	6	5	4	3	2	1
FUNC_TEST=YES JTAG_ASIC_TMS 13 28	FUNC_TEST=YES TMD5_CONN_CLKP 22 38	FUNC_TEST=YES TV_C 22	FUNC_TEST=YES PCI_AD<7> 9 12 17 25 27 38	FUNC_TEST=YES PCI_PAR 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_CS0_L 25 38	FUNC_TEST=YES +5V_INV_SW 22 39	FUNC_TEST=YES +5V_INV_SW 22 39
FUNC_TEST=YES JTAG_ASIC_TDI 28	FUNC_TEST=YES VGA_R 22	FUNC_TEST=YES TV_Y 22	FUNC_TEST=YES PCI_AD<8> 9 12 17 25 27 38	FUNC_TEST=YES PCI_CBE<0> 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_CS1_L 25 38	FUNC_TEST=YES KBD_Y<0> 31	FUNC_TEST=YES LEFT_USB_DM 25 27 38
FUNC_TEST=YES JTAG_ASIC_TDO 13 14	FUNC_TEST=YES VGA_G 22	FUNC_TEST=YES TV_COMP 22	FUNC_TEST=YES PCI_AD<9> 9 12 17 25 27 38	FUNC_TEST=YES PCI_CBE<1> 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_RST_L 25 38	FUNC_TEST=YES KBD_Y<1> 31	FUNC_TEST=YES LEFT_USB_DP 25 27 38
FUNC_TEST=YES JTAG_ASIC_TCK 13 28	FUNC_TEST=YES VGA_B 22	FUNC_TEST=YES SND_TO_AUDIO 14 26	FUNC_TEST=YES PCI_AD<10> 9 12 17 25 27 38	FUNC_TEST=YES PCI_CBE<2> 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_WR_L 25 38	FUNC_TEST=YES FW_TP01P 30 38	FUNC_TEST=YES LEFT_USB_DM 25 27 38
FUNC_TEST=YES JTAG_ASIC_TRST_L 13 28	FUNC_TEST=YES VGA_VSYNC 22	FUNC_TEST=YES SND_SYNC 14 26	FUNC_TEST=YES PCI_AD<11> 9 12 17 25 27 38	FUNC_TEST=YES PCI_CBE<3> 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_WRL 25 38	FUNC_TEST=YES FW_TP01N 30 38	FUNC_TEST=YES RIGHT_USB_DM 27 33 38
FUNC_TEST=YES CPU_CHKSTP_OUT_L 5	FUNC_TEST=YES VGA_HSYNC 22	FUNC_TEST=YES SND_CLKOUT 14 26 37	FUNC_TEST=YES PCI_AD<12> 9 12 17 25 27 38	FUNC_TEST=YES AIRPORT_PCI_REQ_L 12 25	FUNC_TEST=YES EIDE_OPTICAL_IOCHRDRY 25 38	FUNC_TEST=YES KBD_Y<3> 31	FUNC_TEST=YES RIGHT_USB_DP 27 33 38
FUNC_TEST=YES CPU_SRESET_L 5	FUNC_TEST=YES DVI_DDC_CLK_UP 22	FUNC_TEST=YES SND_CLKOUT 14 26 37	FUNC_TEST=YES PCI_AD<13> 9 12 17 25 27 38	FUNC_TEST=YES AIRPORT_PCI_GNT_L 12 25	FUNC_TEST=YES EIDE_OPTICAL_INT 25 38	FUNC_TEST=YES KBD_Y<4> 31	FUNC_TEST=YES NEC_LEFT_USB_PWREN 25 27
FUNC_TEST=YES CPU_HRESET_L 5 6 7	FUNC_TEST=YES DVI_DDC_DATA_UP 22	FUNC_TEST=YES INT_AUDIO_TO_SND 14 26	FUNC_TEST=YES PCI_AD<14> 9 12 17 25 27 38	FUNC_TEST=YES AIRPORT_PCI_INT_L 14 25	FUNC_TEST=YES TPAD_F_TXD	FUNC_TEST=YES KBD_Y<6> 31	FUNC_TEST=YES NEC_LEFT_USB_OVERCURRENT 25 27
FUNC_TEST=YES JTAG_CPU_TMS 5 6	FUNC_TEST=YES DVI_HPD_UP 22	FUNC_TEST=YES SND_SCLK 14 26 37	FUNC_TEST=YES PCI_AD<15> 9 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DATA<0> 25 38	FUNC_TEST=YES LID_CLOSED_L 23	FUNC_TEST=YES KBD_Y<7> 31	FUNC_TEST=YES NEC_RIGHT_USB_PWREN 27 33
FUNC_TEST=YES JTAG_CPU_TDI 5 6	FUNC_TEST=YES LVDS_L0N 19 22 38	FUNC_TEST=YES SND_HW_RESET_L 14 26	FUNC_TEST=YES PCI_AD<16> 9 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DATA<1> 25 38	FUNC_TEST=YES COMM_RESET_L 14 26	FUNC_TEST=YES KBD_NUMLOCK_LED	FUNC_TEST=YES NEC_RIGHT_USB_OVERCURRENT 27 33
FUNC_TEST=YES JTAG_CPU_TDO 5	FUNC_TEST=YES LVDS_L0P 19 22 38	FUNC_TEST=YES SND_HP_SENSE_L 14 26	FUNC_TEST=YES PCI_AD<17> 9 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DATA<2> 25 38	FUNC_TEST=YES COMM_SHUTDOWN 14 26	FUNC_TEST=YES +BATT_POS 32 39	FUNC_TEST=YES DDDC_EN 19 30 34 35
FUNC_TEST=YES JTAG_CPU_TCK 5 6	FUNC_TEST=YES LVDS_L1N 19 22 38	FUNC_TEST=YES SND_LIN_SENSE_L 14 26	FUNC_TEST=YES PCI_AD<18> 9 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DATA<3> 25 38	FUNC_TEST=YES COMM_RING_DET_L 14 26 31	FUNC_TEST=YES BATT_CLK 32	FUNC_TEST=YES BBANG_HRESET_L 6
FUNC_TEST=YES JTAG_CPU_TRST_L 5 6 40	FUNC_TEST=YES LVDS_L1P 19 22 38	FUNC_TEST=YES SND_LIN_SENSE_L 14 26	FUNC_TEST=YES PCI_AD<19> 9 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DATA<4> 25 38	FUNC_TEST=YES COMM_RING_DET_L 14 26 31	FUNC_TEST=YES BATT_DATA 32	FUNC_TEST=YES MAIN_RESET_L 14 17 18 20 25 27 31
	FUNC_TEST=YES LVDS_L2N 19 22 38	FUNC_TEST=YES INT_I2C_DATA2 14 26	FUNC_TEST=YES PCI_AD<20> 9 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DATA<5> 25 38	FUNC_TEST=YES +5V_TPAD_SLEEP	FUNC_TEST=YES BATT_NEG 32 39	FUNC_TEST=YES RF_DISABLE_L_SPN 25
	FUNC_TEST=YES LVDS_L2P 19 22 38	FUNC_TEST=YES INT_I2C_CLK2 14 26	FUNC_TEST=YES PCI_AD<21> 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DATA<6> 25 38	FUNC_TEST=YES +3V_HALL_EFFECT 23 39	FUNC_TEST=YES PMU_BATT_DET_L 31 32	FUNC_TEST=YES AIRPORT_CLKRUN_L 25
	FUNC_TEST=YES CLKLVDS_LN 19 22 38	FUNC_TEST=YES CHGND4 39	FUNC_TEST=YES PCI_AD<22> 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DATA<7> 25 38	FUNC_TEST=YES KBD_CAPSLOCK_LED	FUNC_TEST=YES FANR_GND 39	FUNC_TEST=YES ROM_RW_L 9 12 25
	FUNC_TEST=YES CLKLVDS_LP 19 22 38	FUNC_TEST=YES SLEEP_LED	FUNC_TEST=YES PCI_AD<23> 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DATA<8> 25 38	FUNC_TEST=YES KBD_FUNCTION_L 23 31	FUNC_TEST=YES COMM_DTR_L 14 26	FUNC_TEST=YES ROM_ONBOARD_CS_L 9 25
	FUNC_TEST=YES INT_I2C_CLK0 6 11 13 23	FUNC_TEST=YES LVDS_U0N 19 22 38	FUNC_TEST=YES PCI_AD<24> 9 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DATA<9> 25 38	FUNC_TEST=YES KBD_CONTROL_L 23 31	FUNC_TEST=YES FANL_GND 39	FUNC_TEST=YES ROM_CS_L 9 12 25
	FUNC_TEST=YES INT_I2C_DATA0 6 11 13 23	FUNC_TEST=YES LVDS_U0P 19 22 38	FUNC_TEST=YES PCI_AD<25> 9 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DATA<10> 25 38	FUNC_TEST=YES +3V_BATT_ISSUE_N 24	FUNC_TEST=YES FANL_TACH	FUNC_TEST=YES CLK33M_AIRPORT 12 25 37
	FUNC_TEST=YES INT_I2C_CLK1 13 14 23 24 26	FUNC_TEST=YES LVDS_U1N 19 22 38	FUNC_TEST=YES PCI_AD<26> 9 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DATA<11> 25 38	FUNC_TEST=YES KBD_OPTION_L 23 31	FUNC_TEST=YES FANR_PWM	FUNC_TEST=YES AIRPORT_IDSEL 25
	FUNC_TEST=YES INT_I2C_DATA1 13 14 23 24 26	FUNC_TEST=YES LVDS_U1P 19 22 38	FUNC_TEST=YES PCI_AD<27> 9 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DATA<12> 25 38	FUNC_TEST=YES KBD_SHIFT_L 23 31	FUNC_TEST=YES FANL_PWM	FUNC_TEST=YES ROM_OE_L 9 12 25
	FUNC_TEST=YES CBUS_DET_1_L 17	FUNC_TEST=YES LVDS_U2N 19 22 38	FUNC_TEST=YES PCI_AD<28> 9 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DATA<13> 25 38	FUNC_TEST=YES KBD_X<0> 23 31	FUNC_TEST=YES RJ45_DP<0> 28 38	FUNC_TEST=YES INT_MOD_DTI 14 26
	FUNC_TEST=YES CBUS_DET_2_L 17	FUNC_TEST=YES LVDS_U2P 19 22 38	FUNC_TEST=YES PCI_AD<29> 9 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DATA<14> 25 38	FUNC_TEST=YES KBD_X<1> 23 31	FUNC_TEST=YES RJ45_DP<1> 28 38	FUNC_TEST=YES JTAG_CPU_TRST_L 5 6 40
	FUNC_TEST=YES TMD5_DN<0> 20 22 38	FUNC_TEST=YES CLKLVDS_UN 19 22 38	FUNC_TEST=YES PCI_AD<30> 9 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DATA<15> 25 38	FUNC_TEST=YES KBD_X<3> 23 31	FUNC_TEST=YES RJ45_DP<1> 28 38	FUNC_TEST=YES GPU_VCORE 18 19 39
	FUNC_TEST=YES TMD5_DF<0> 20 22 38	FUNC_TEST=YES CLKLVDS_UP 19 22 38	FUNC_TEST=YES PCI_AD<31> 9 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DMA_RQ 25 38	FUNC_TEST=YES MMN_ACC_SELFTEST 24	FUNC_TEST=YES RJ45_DP<2> 28 38	FUNC_TEST=YES CPU_VCORE_SLEEP 5 6 35 39
	FUNC_TEST=YES TMD5_DN<1> 20 22 38	FUNC_TEST=YES LVDS_DDC_CLK 19 22	FUNC_TEST=YES PCI_FRAME_L 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_RD_L 25 38	FUNC_TEST=YES MMN_ACC_X_AXIS 24	FUNC_TEST=YES RJ45_DP<2> 28 38	FUNC_TEST=YES MOD_BITCLK 14 26
	FUNC_TEST=YES TMD5_DP<1> 20 22 38	FUNC_TEST=YES LVDS_DDC_DATA 19 22	FUNC_TEST=YES PCI_TRDY_L 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DMAACK_L 25 38	FUNC_TEST=YES MMN_ACC_Y_AXIS 24	FUNC_TEST=YES RJ45_DP<3> 28 38	FUNC_TEST=YES MOD_SYNC 14 26
	FUNC_TEST=YES TMD5_DN<2> 20 22 38	FUNC_TEST=YES BRIGHT_PWM 22	FUNC_TEST=YES PCI_IRDY_L 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_ADDR<0> 25 38	FUNC_TEST=YES MMN_ACC_Z_AXIS 24	FUNC_TEST=YES RJ45_DP<3> 28 38	FUNC_TEST=YES SLEEP 23 31 34 36
	FUNC_TEST=YES TMD5_DP<2> 20 22 38	FUNC_TEST=YES TV_GND1 22 39	FUNC_TEST=YES PCI_DEVSEL_L 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_ADDR<1> 25 38	FUNC_TEST=YES MMN_ACC_Z_AXIS 24	FUNC_TEST=YES RJ45_DP<3> 28 38	FUNC_TEST=YES 1778_VFB 19 39
	FUNC_TEST=YES TMD5_CONN_CLKN 22 38	FUNC_TEST=YES TV_GND2 22 39	FUNC_TEST=YES PCI_STOP_L 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_ADDR<2> 25 38	FUNC_TEST=YES VCORE_VID0	FUNC_TEST=YES VCORE_VID0	
			FUNC_TEST=YES SND_AMP_MUTE 26	FUNC_TEST=YES SRCLK_TP 27	FUNC_TEST=YES VCORE_VID1	FUNC_TEST=YES VCORE_MUX_EN 35	
			FUNC_TEST=YES SND_HP_MUTE_INV	FUNC_TEST=YES SRMOD_TP 27	FUNC_TEST=YES VCORE_VID2		
				FUNC_TEST=YES TEB_TP 27	FUNC_TEST=YES VCORE_VID3		
				FUNC_TEST=YES TEST_TP 27	FUNC_TEST=YES VCORE_VID4		

FUNCTIONAL TEST POINTS

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6694	B
SCALE	SHT	OF	REV.
NONE	40	45	

REVISION HISTORY

12/11/03

- 1) IMPORTED Q41 PRODUCTION RELEASE SCHEMATIC
- 2) CHANGED CPU (U43) TO R7PM
- 3) CHANGED PLL CONFIG STUFFING FOR NEW CPU
- 4) CHANGED U44 TO 81 (S884 SYMBOL)
- 5) ADDED CPU_AVDD_LDO (U6)
- 6) ADDED R284 AND R604 TO ADD OPTION FOR PD_L OF U42 (CLOCK CHIP) TO BE DRIVEN BY JTAG_ASIC_TDO FROM INTREPID
- 7) ADDED R608 TO DISCONNECT INT_GP100 FROM OC_FSEL
- 8) CHANGED JTAG_ASIC_TDO TP TO JTAG_ASIC_TDO AND MOVED IT TO INTREPID'S TDO
- 9) CHANGED JTAG_ASIC_TDI TO CONNECT TO ETHERNET PHY'S TDI

12/15/03

- 10) CHANGED PIN 4 (DCDC_EN) ON J11 TO NEC_RIGHT_USBOVERCURRENT
- 11) CHANGED PIN 11 OF J11 TO NC

12/16/03

- 12) ADDED R633 AS PULLUP ON JTAG_ASIC_TDI
- 13) CHANGED CPU_TEMP_DM TO CPU_THERM_DM
- 14) CHANGED CPU_TEMP_DP TO CPU_THERM_DP
- 15) CHANGED GPU_THERM_DP TO GPU_THERM_DP_TP
- 16) CHANGED GPU_THERM_DP_TP TO GPU_THERM_DP_TP
- 17) CHANGED GPU_THERM_DP_TP TO GPU_THERM_DP_TP
- 18) CHANGED GPU_THERM_DP_TP TO GPU_THERM_DP_TP
- 19) FIXED MISSED CONNECTION WITH MAXBUS_SLEEP TO CPU

12/17/03

- 18) CHANGED R657 (EXTPELL_SDNV_POL_BOOT_STRAP) TO NO STUFF AND REMOVED NO STUFF FROM R153
- 19) UPDATE DIFF NET SPECTING TYPE PROPERTY ON POWER SUPPLY SENSE AND THERMAL DIODE DIFF PAIRS
- 20) CHANGED FIREWIRE_OSCILLATOR (G1) TO NEW PREFERRED SUNNY PART

12/18/03

- 21) CHANGED MAX VIA COUNT ON ALL AGP STB NETS TO 5 TO CLEAR DRCS

** RELEASED FOR EVT **

2/10/04

- 22) REMOVED XW11 - JUMPER ON 1.8V SWITCHER OUTPUT
- 23) CHANGED R657 TO STUFFE AND R153 TO NO STUFF
- 24) CHANGED CPU PLL CONFIG TO 9X HIGH AND 5X LOW

** RELEASED FOR DVT **

3/24/04

- 25) REMOVED ALTERNATE BOM OPTION FROM ALTERNATE ETHERNET CRYSTALS

3/29/04

- 26) ADDED ALTERNATE FOR Q41A REV 1.1.1 CPU (U43)
- 27) ADDED ALTERNATES FOR 129M AND 64M A16 W11'S
- 28) CHANGED TMS SERIES RPAKS TO 0 OHMS (RP57,RP27,RP32,RP28)
- 29) ADDED ALTERNATE FOR ALS_OP-AMP (U40)

** RELEASED TO REV A **

- 30) CHANGED TMS TERMINATION R,C AND LS TO PRODUCTION VALUES

** RELEASED TO REV A UNDER NEW PART NUMBER **

09/17/2004

- 1) GPU_DVOD<0..12> NETNAME CHANGE TO GPU_DVOD<0..23>
- 2) D8 FROM 1N5227B CHANGE TO BZX84C2V7LT1
- 3) R751 VALUE FROM 10K OHM CHANGE TO 604 OHM
- 4) ADD C935 (0.1UF)
- 5) ADD R867 (0 OHM) FOR IPOD ACTION
- 6) PMU_PIN74 NETNAME FROM NC TO PMU_SELECT
- 7) ADD R868 (10K OHM; NO_STUFF) PULL UP TO +3V_PMU
- 8) ADD R869 (10K OHM) PULL DOWN TO GND
- 9) PMU_PIN_91 NETNAME FROM NC TO SYS_BATT_ISNS2
- 10) ADD R870 (0 OHM) SYS_BATT_ISNS2 LINK TO SYS_BATT_ISNS
- 11) ADD U51 (INA138)
- 12) ADD R852 (0.010 OHM), R853 (150K OHM) AND R857 (49.9 OHM)
- 13) ADD C917 (0.1UF) AND C925 (10UF)
- 14) ADD DESCRIPTION FOR MMM_I2C_BUS
- 15) MMM_I2C_BUS LINK TO INTREPID:INT_I2C_CLK1 AND INT_I2C_DATA1
- 16) CHANGE NETNAME FROM INT_EXTINT11_PU TO MMM_FFIRQ_L
- 17) CHANGE NETNAME FROM INT_EXTINT12_PU TO MMM_SIRQ_L
- 18) ADD R863 (10K OHM) AND R864 (10K OHM) FOR MMM_FFIRQ_L & MMM_SIRQ_L PULL UP TO +3V_MAIN
- 19) ADD U53 (16F818) AND U5 (KXM52)
- 20) ADD R845 (0 OHM), R846 (0 OHM; NO_STUFF), R847 (10K OHM; NO_STUFF), R848 (10K OHM; NO_STUFF)
- 21) ADD R849 (10K OHM), R850 (10K OHM; NO_STUFF), R851 (0 OHM), R854 (10K OHM), R856 (10K OHM),
- 22) ADD R860 (0 OHM), R858 (0 OHM), R859 (0 OHM), R855 (10K OHM), R861 (10K OHM), R862 (10K OHM; NO_STUFF)
- 23) ADD C936 (0.1UF), C918 (0.1UF), C919 (0.1UF), C921 (0.0047UF), C923 (0.0047UF), C926 (0.0047UF), C927 (0.1UF)
- 24) DEL RP44 (100K OHM) AND ADD R874 (100K OHM), R875 (100K OHM) AND R873 (100K OHM)
- 25) ADD R872 (10K OHM) FOR AUDIO_LO_MUTE_L
- 26) ADD R871 (100 OHM) AND SUPERCAP C937 (N20P80; 5.5V; ELEC; 0.33F)
- 27) J21_PIN12 NETNAME FROM NC CHANGE TO THERM_L_OC
- 28) J21_PIN10 NETNAME FROM NC CHANGE TO INT_I2C_DATA1
- 29) J21_PIN11 NETNAME FROM NC CHANGE TO INT_I2C_CLK1
- 30) C592 VALUE FROM 0.001UF CHANGE TO 0.01UF (208, 50V, 0603)
- 31) U59 FROM MP1518DJ CHANGE TO MM3120
- 32) L11 CHANGE TO 152S0235 (22UH; 3.8*3.8*1.5MM)
- 33) DEL D31
- 34) R202 VALUE FROM 5.23 OHM CHANGE TO 25.5 OHM
- 35) C79 VALUE FROM 2.2UF CHANGE TO 1UF
- 36) ADD Q70 (SI3443), Q34 (2N7002)
- 37) ADD R866 (100K OHM), R865 (4.7 OHM), C929 (0.022UF)

09/20/2004

- 1) ADD R877 (10K OHM)
- 2) ADD R876 (470K OHM; NO_STUFF)

09/21/2004

- 1) ADD R878 AND R879 (0 OHM; NO_STUFF) [ADD A 0-OHM RESISTOR TO BY-PASS THE N-FET ON EACH FAN]

09/22/2004

- 1) R822 (680 OHM CHANGE TO 510 OHM) AND R826 (680 OHM CHANGE TO 510 OHM)

09/23/2004

- 1) ADD NC NETNAME AT U59_PIN6 AND PIN9
- 2) CHANGE R465 CAP SIZE FROM 0603 TO 0805
- 3) BOM OPTION FROM NO_STUFF CHANGE TO SUPERCAP

09/24/2004

- 1) CHANGE R465 FROM MF 1/16W TO FF 1/10W
- 2) ADD R880 AND R871 (0 OHM; BOM_OPTION; FOR SUPERCAP AND BACKUP BATTERY SWITCH)
- 3) ADD U60 (LIS3L02AQ; ST SENSOR)
- 4) ADD R881 (10K OHM), R882 (10K OHM), R883 (10K OHM)
- 5) ADD C937 (0.1UF, 10V, 208, 0402)
- 6) ADD BOM_OPTION (KIONIX_ACCEL AND ST_ACCEL)

10/04/2004

- 1) CHANGE TEST POINT FUNC_TEST=NO FOR FUNC_TP_WRONG_SIDE.LOG
- 2) ADD NO_TEST=YES FOR NOTP.LOG(MMM_PIC_AN2_PD, MMM_PIC_AN3_PU)

10/05/2004

- 1) ADD R850 (0 OHM)

10/15/2004

- 1) REPLACE BOOT BANGER EEPROM U32 WITH 32KX M24256B FUNC_TP_WRONG_SIDE.LOG

12/16/2004

- 1) SCHEMATIC RELEASE FOR PRODUCTION

REVISION HISTORY (1 OF 1)

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SIZE	DRAWING NUMBER	REV.
D	051-6694	B
SCALE	SHT	OF
NONE	41	45


8	7	6	5	4	3	2	1
A	B	C	D	E	F	G	H
8	7	6	5	4	3	2	1

8	7	6	5	4	3	2	1
D							D
C							C
B							B
A							A

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