1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
G		396923	PRODUCTION RELEASED	08/26/05	?

SCHEM,MLB,PB17"

08/25/2005

BOM OPTIONS	STUFF	NO STUFF
D3_HOT		✓
D3_COLD	✓	
GPU_SS	✓	
GPU_SWITCH	✓	
SERIAL_DEBUG		✓
VCORE_OFFSET	✓	
1_8V_MAXBUS	✓	
1_5V_MAXBUS		✓
NEC_USB	✓	
INTREPID_USB		✓
BBANG		✓
NO_BBANG		✓
ATI_MEMIO_HI	✓	
ATI_MEMIO_LO		✓
SSCG		✓
NO_SSCG	✓	
5V_HD_LOGIC	✓	
3V_HD_LOGIC		✓
EXT_TMDS	✓	
INT_TMDS		✓
MMM	✓	
INT_CLK	✓	
EXT_CLK		✓

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6694	1	SCHEM,MLB,PB17	SCH1	
820-1688	1	PCBF,MLB,PB17	PCB1	
826-4393	1	LABEL,PCB,28MM X 6MM	EEE:U3Y	LABEL_R15

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

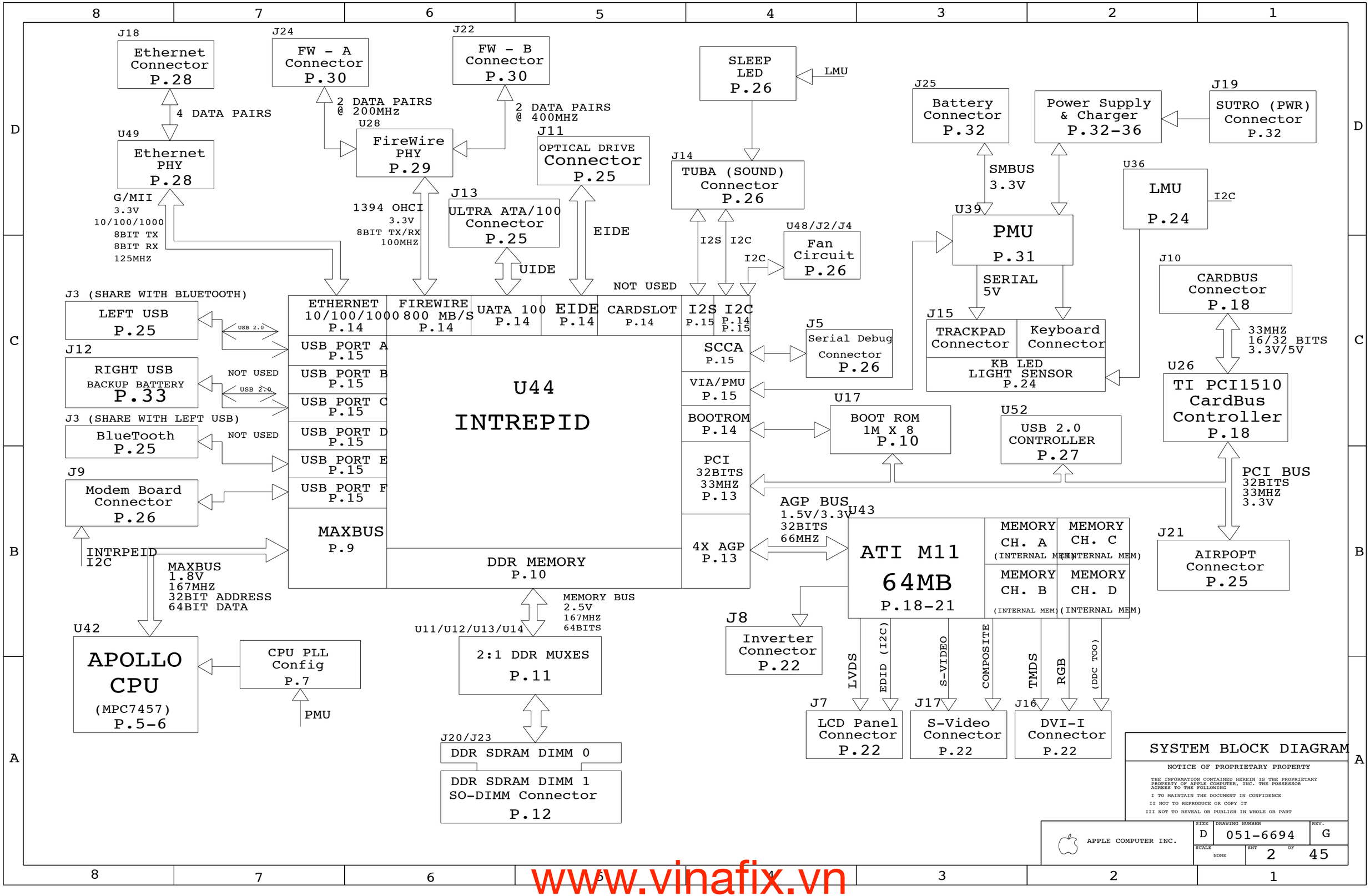
MATERIAL/FINISH NOTED AS APPLICABLE
SIZE D

Apple Computer Inc.

TITLE
SCHEM,MLB,PB17"

DRAWING NUMBER 051-6694 REV. G

SHT 1 OF 45



POWER SYSTEM ARCHITECTURE

AC ADAPTER IN PG 31

INRUSH LIMITER PG 30

+24V_PBUS

1V20_REF

>-13.44V TURNS-ON
<-13.44V SHUTS-OFF

U21 PG 31

RUN/SS

BUCK VCC REGULATOR (LTC1625) PG 32

AC: 12.8V
NO AC: BATTERY VOLTAGE 1625 NOT RUNNING

SHUTDOWN: RUNNING
SLEEP: RUNNING
RUN: RUNNING

+PBUS (12.8V)

BACKLIGHT INVERTER

+5V_MAIN

VCC MAIN 2.5V/1.5V DC/DC (MAX1715) PG 35

SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING

TURNS ON OUTPUT @ 2.4V ON1/ON2

MAP31 DDR I/O
MAP31 DDR CORE
DDR POWER

+2.5V_MAIN

PGOOD 1_5V_2_5V_OK

+1.5V_MAIN

INTREPID CORE
AGP I/O

+PBUS

DCDC_EN
SLEEP

MAXBUS SEQUENCING

+5V_MAIN

VCC SHDN

DC/DC (MAX1717) PG 34

SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING

CPU_VCORE (+1.4V/+1.5V)

14V_PBUS

+3V_PMU LDO PG 32

+5V_MAIN
+3V_PMU
+4_6V_BU

+BATT

RC AT 1M*0.047UF @ 24V
STARTS 2.0MSEC AFTER DCDC_EN_L BECOMES LOW

DCDC_EN_L

AFTER PMU IS UP AND RUNNING
DCDC_EN_L WILL PULL ON1/ON2 LOW IN SHUTDOWN

RUN/SS - 5V
TURNS ON AT >1V
<100UA ALLOWED
INTERNAL ZENER CLAMP TO 6V

MAIN 3V/5V DC/DC (LTC3707) PG 33

VCC STBYMD

SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING

INTERNAL ZENER CLAMP TO 6V
<100UA ALLOWED
TURNS ON AT >1V
RUN/SS - 3V

+5V_MAIN

PGOOD 3V_5V_OK

HOLDS BOTH RUN/SS AT GND WHEN IT'S CONNECTED TO GND

TURNS CONTROL TO RUN/SS WHEN IT'S OPEN

+3.3V_MAIN

+PBUS (12.8V)

+5V_MAIN

VCC EXT_VCC DC/DC (LTC1778) PG 20

SHUTDOWN: STOPPED
SLEEP: D3HOT/D3COLD
RUN: RUNNING

TURNS ON AS LOW AS 0.8V/TYP 1.5V
INTERNAL 1.2UA CURRENT SOURCE

RUN/SS

GPU_VCORE +1.2V/+1.0V

DCDC_EN
SLEEP

D3_COLD

GPU_VCORE SEQUENCING

1M & 0.1UF @14V, IT TAKES ~5.88MS TO START SWITCHER

1_5V_2_5V_OK

D3_HOT

DCDC_EN_L
D3_HOT

1_5V_2_5V_OK WILL NOT PULL LOW UNTIL +5V_MAIN TURNS ON
HOWEVER, 5V SHOULD TURN ON ~2.23MS AFTER DCDC_EN_L OR PMU_POWERUP_L BECOMES '1'; MUCH LESS THAN THE RC CHARGING AT INT_VCC (5V)

BACKUP BATTERY

CHARGER INPUT & BOOST OUTPUT PG 32

+PBUS

12.8V CHARGES BACKUP BATTERY

24V IS OUTPUT ONLY FROM BACKUP BATTERY

BACKUP BATTERY CIRCUIT CHARGES OFF +PBUS AND PREVENTS +PBUS AND +24V_PBUS FROM DROPPING BELOW 6V (UNTIL DRAINED)

RC AT 1M*0.1UF @ 24V
STARTS ~4.25MSEC AFTER DCDC_EN_L BECOMES LOW

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

+24V_PBUS

DC/DC (LTC3411) PG 35

SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING

+1.8V_MAIN

MAXBUS BROADCOM

BATTERY CHARGER (MAX1772) PG 31

+BATT

3S 3P PRISMATIC CELLS

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

BATTERY VOLTAGE FEED-IN PATH PG 31

+PBUS

SHUT-DOWN RUN SLEEP RUN SHUT-DOWN

SLEEP
SLEEP_L_LS5
DCDC_EN
DCDC_EN_L
+5V_MAIN ~11MS
+5V_SLEEP
+3V_MAIN ~13.5MS
+3V_SLEEP
3V_5V_OK 2.4V - ??? MS
+2_5V_MAIN 2.6 MS
+2_5V_SLEEP
+1_5V_MAIN 2.6 MS
+1_5V_SLEEP
1_5V_2_5V_OK (MAX1715 OUTPUT)
1_5V_2_5V_OK (AT LTC1778 RUN/SS)
GPU_VCORE (D3HOT) ~???MS
GPU_VCORE (D3COLD)
+1_8V_MAIN 1.9 MS

POWER BLOCK DIAGRAM

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6694 | REV. G

SCALE NONE | SHT 3 OF 45

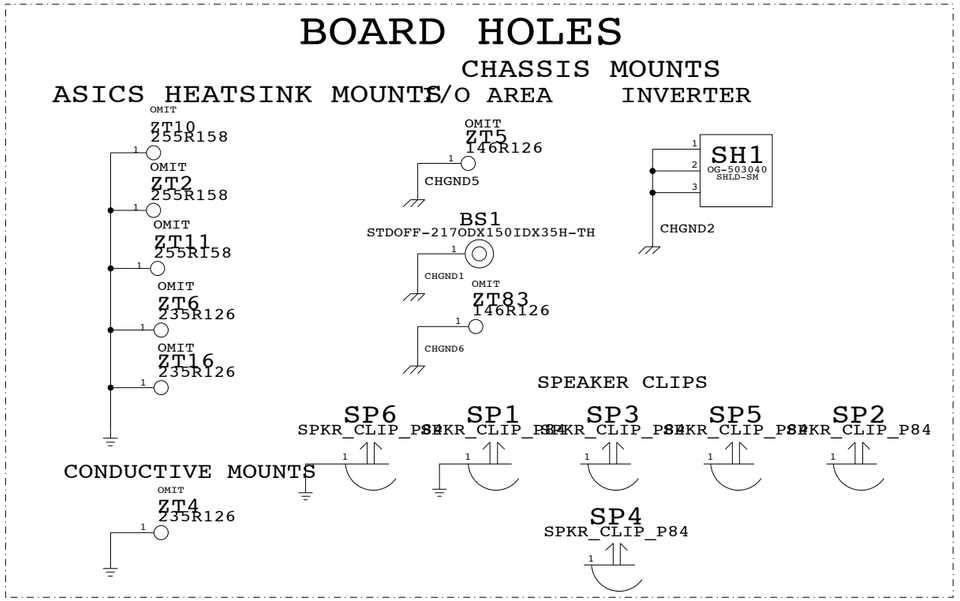
PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

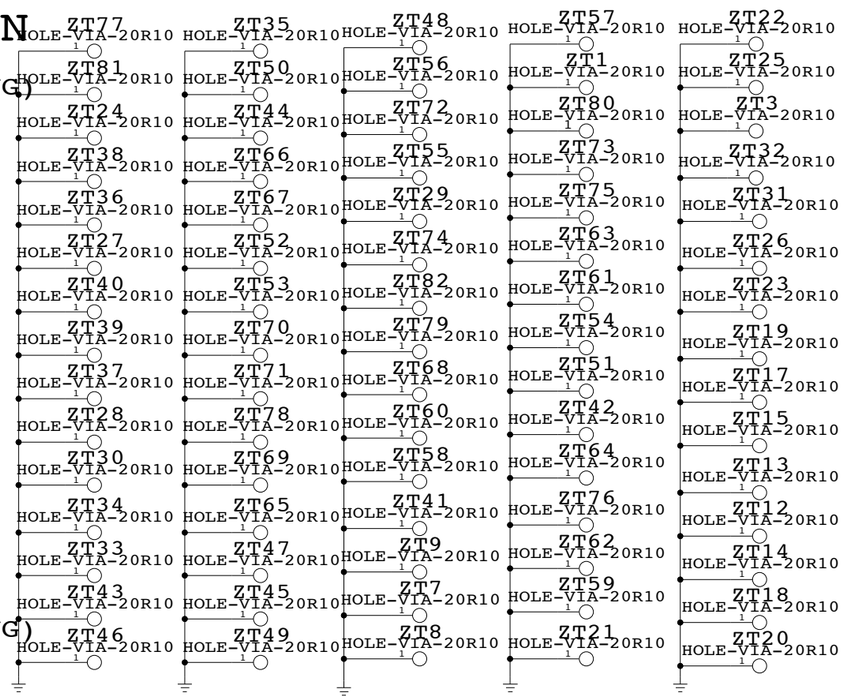
IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 12
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD HOLES



GROUND VIAS



BOARD STACK-UP AND CONSTRUCTION

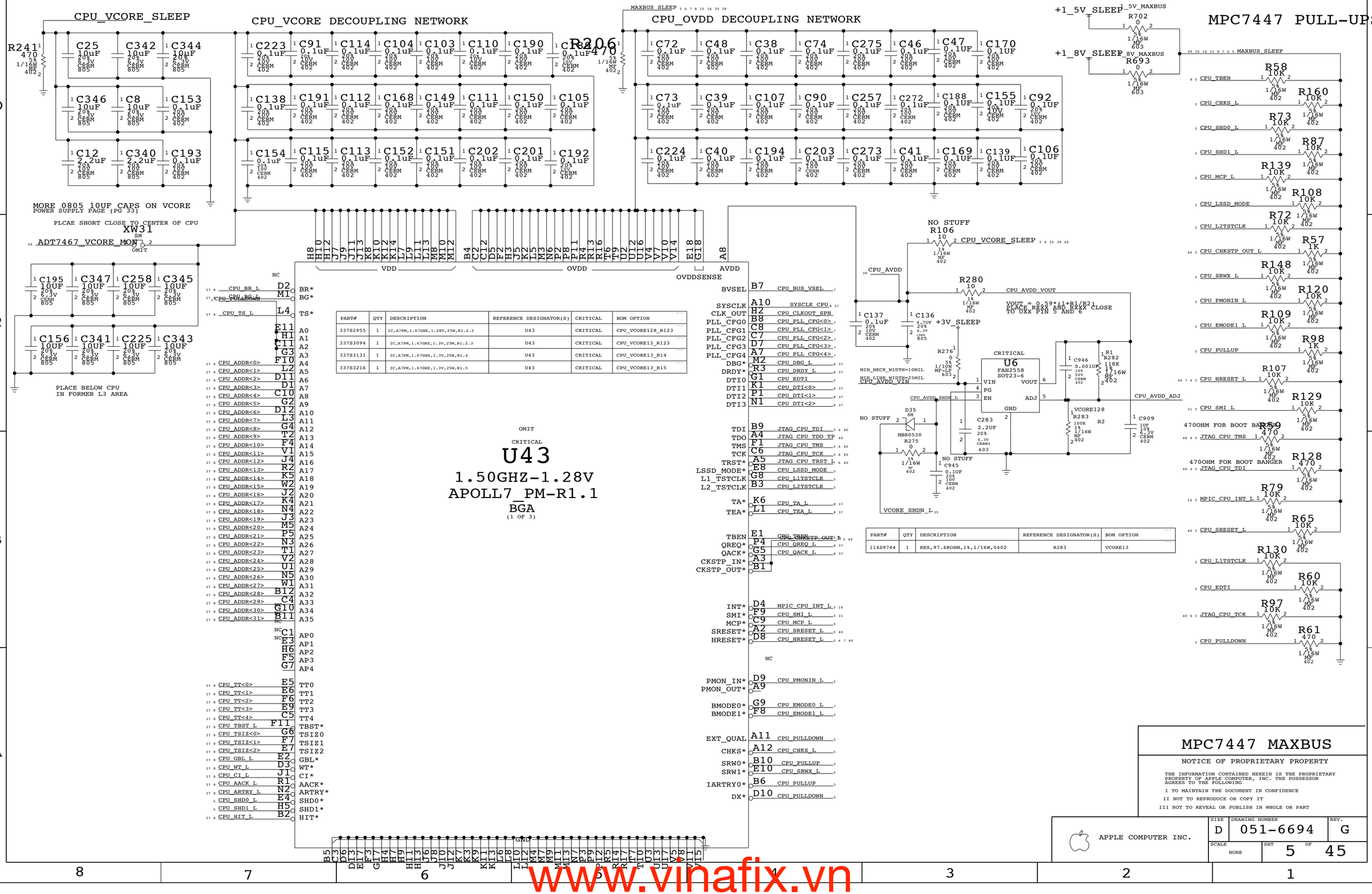
20R10 TH VIA OR VIA IN PAD

1		SIGNAL (1/3 OZ + COPPER PLATING)
2	PREPREG (3MIL)	GROUND (1/2 OZ)
3	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
4	PREPREG (3MIL)	SIGNAL (1/2 OZ)
5	LAMINATE (4MIL)	GROUND (1/2 OZ)
6	PREPREG (2MIL)	CUT POWER PLANE(1 OZ)
7	LAMINATE (3MIL)	CUT POWER PLANE(1 OZ)
8	PREPREG (2MIL)	GROUND (1/2 OZ)
9	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
10	PREPREG (3MIL)	SIGNAL (1/2 OZ)
11	LAMINATE (4MIL)	GROUND (1/2 OZ)
12	PREPREG (3MIL)	SIGNAL (1/3 OZ + COPPER PLATING)

BOARD INFORMATION

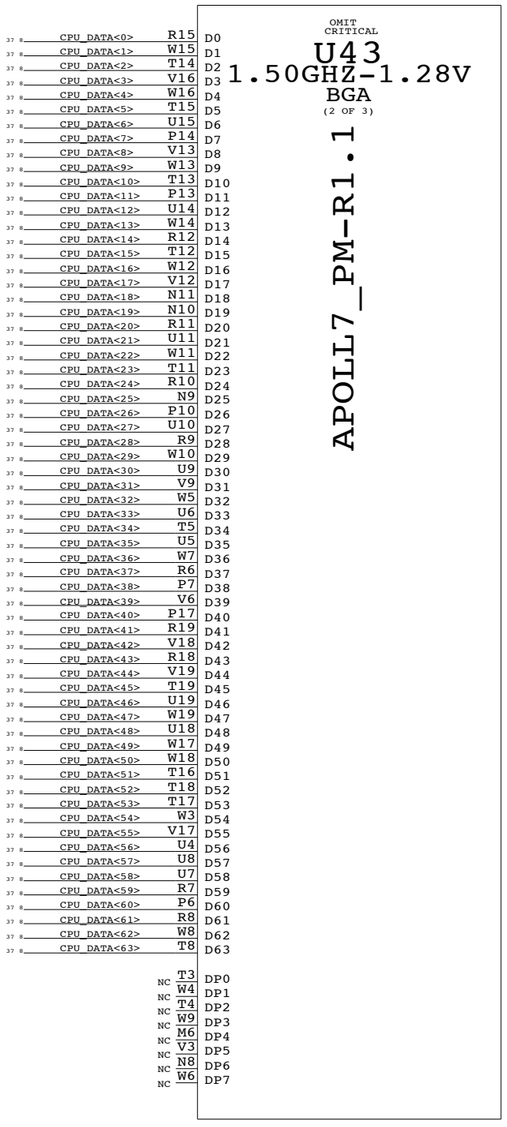
APPLE COMPUTER INC.

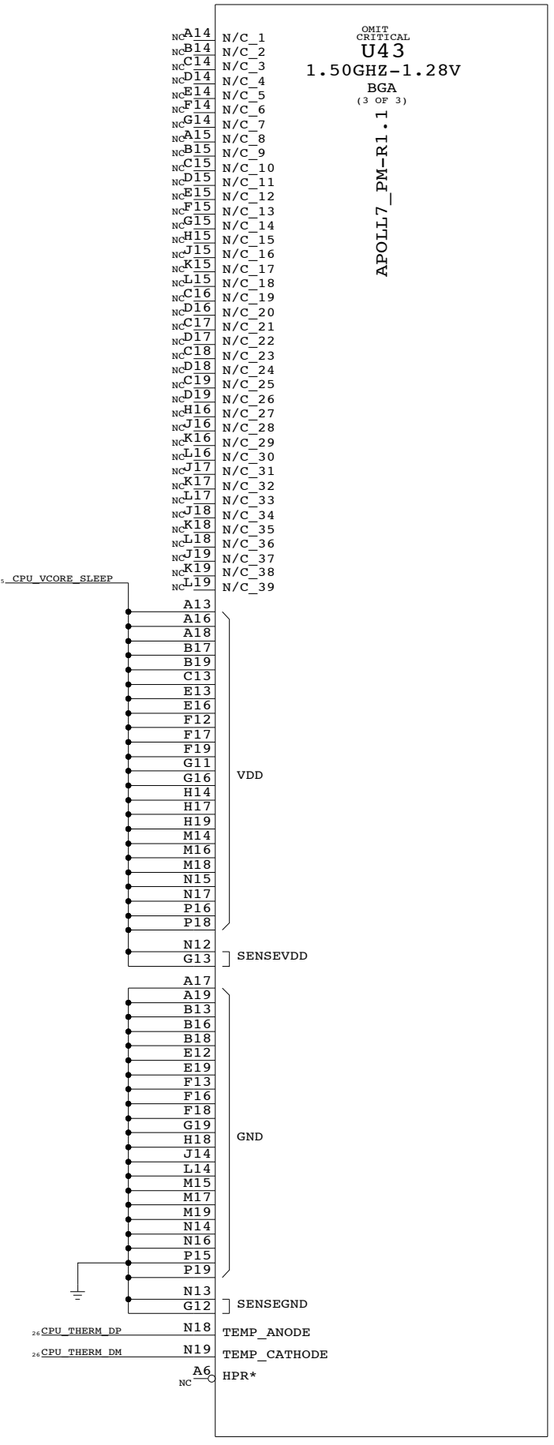
SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE: NONE	SHT 4 OF 45	



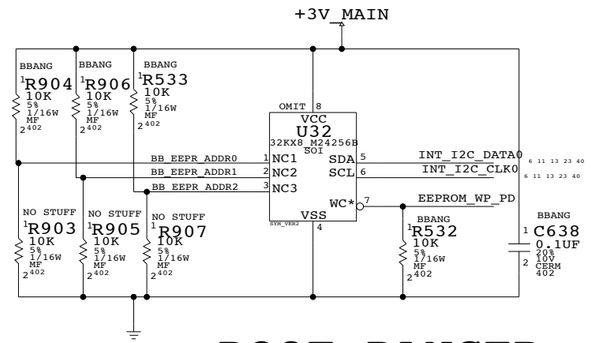
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S2955	1	IC,A7PM,1.67GHZ,1.28V,25W,R1.2.3	U43	CRITICAL	CPU_VCORE128_R123
337S3094	1	IC,A7PM,1.67GHZ,1.3V,25W,R1.2.3	U43	CRITICAL	CPU_VCORE13_R123
337S3131	1	IC,A7PM,1.67GHZ,1.3V,25W,R1.4	U43	CRITICAL	CPU_VCORE13_R14
337S3216	1	IC,A7PM,1.67GHZ,1.3V,25W,R1.5	U43	CRITICAL	CPU_VCORE13_R15

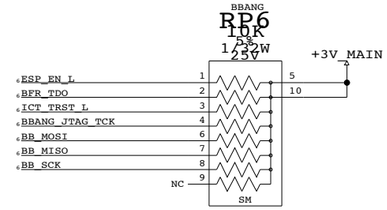
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S9764	1	RES,97.6KOHM,1%,1/16W,0402	R283	VCORE13



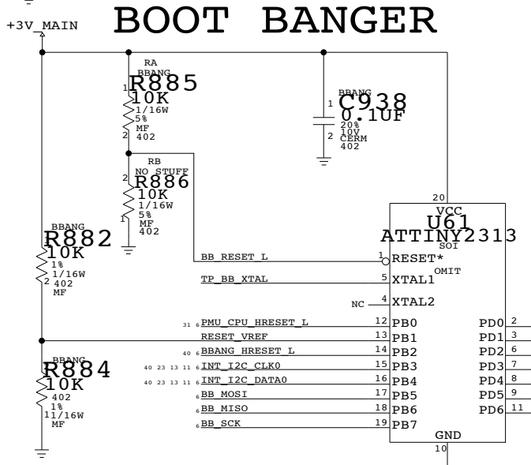


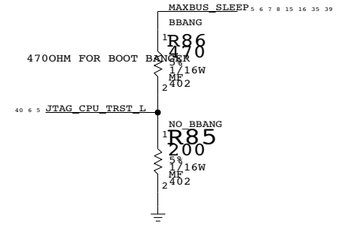
BOOT BANGER E2PROM





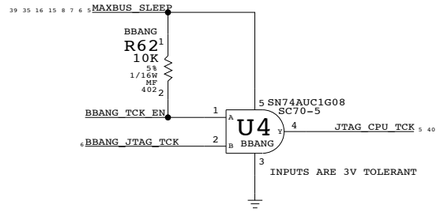
BOOT BANGER

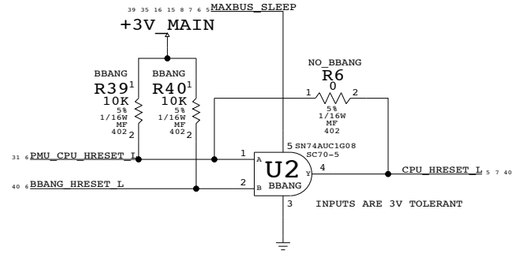




UNSTUFFING RA AND STUFFING RB
WILL DISABLE THE CONTROLLER

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1660	1	MCU,PROGRAMMED W/ BANGER	U61	BBANG
341S1661	1	I2C EEPROM,PROGRAMMED W/ BANGER	U32	BBANG





BOOT BANGING SIGNAL DEFINITION

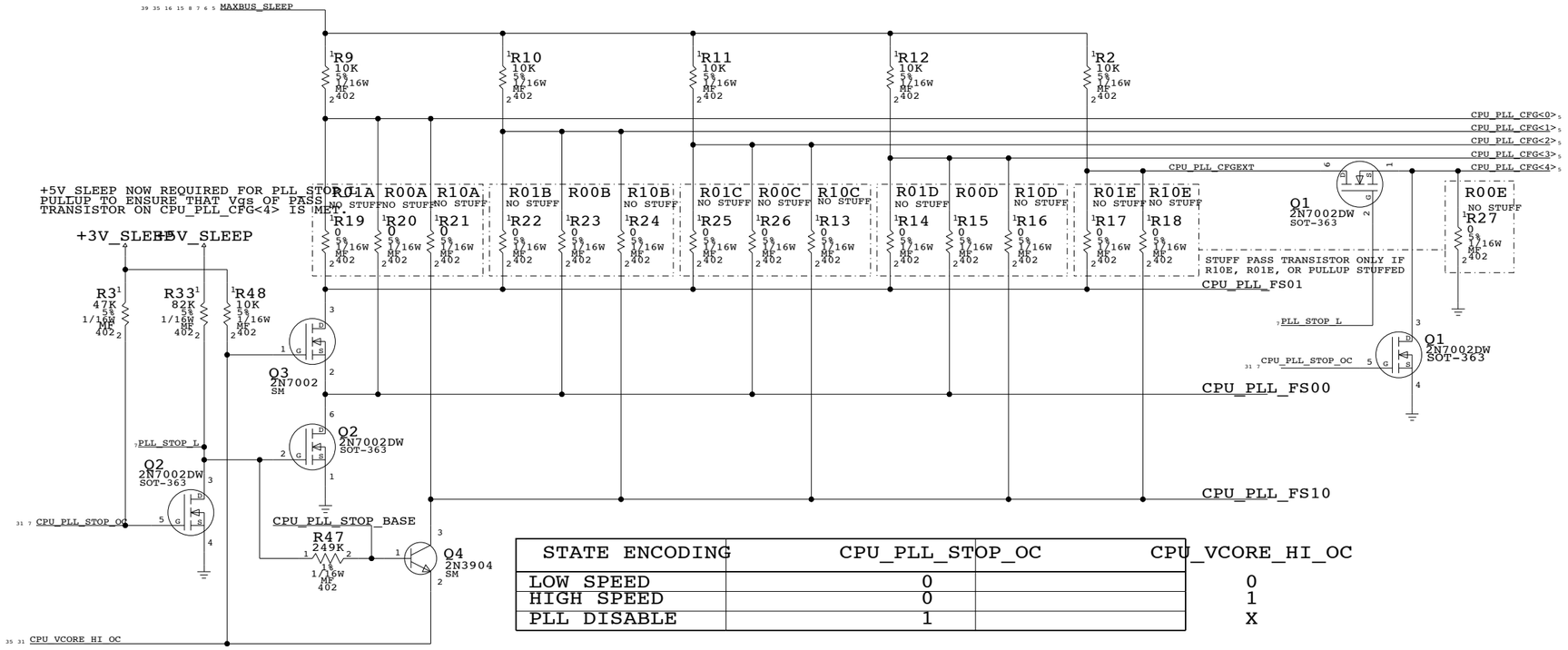
1/ BBANG_HRESET_L (OPEN COLLECTOR OUTPUT - 10K PULLUP ON MLB)
2/ PMU_HRESET_L (3V INPUT INTO LMU)
3/ BBANG_JTAG_TCK (REGULAR OUTPUT)
4/ JTAG_CPU_TMS (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
5/ JTAG_CPU_TDI (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
6/ JTAG_CPU_TRST_L (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)

MPC7447/BBANG

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE: NONE	SHT 6 OF 45	

CPU PLL CONFIG CIRCUITRY



STATE ENCODING	CPU_PLL_STOP_OC		CPU_VCORE_HI_OC
LOW SPEED	0		0
HIGH SPEED	0		1
PLL DISABLE	1		X

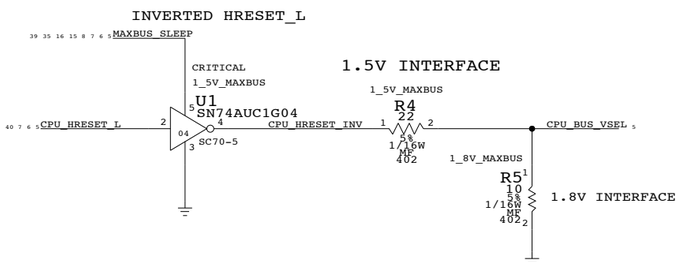
CPU FREQUENCY CONFIGURATION

APOLLO 7

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ (MHZ)	133MHZ	CPU_PLL_CFG 4 0123 E ABCD HEX
0.0X	PLL OFF		0 1111 0F
1.0X	PLL BYPASS		0 0011 03
2.0X	333	267	0 0100 04
3.0X	500	400	0 1000 08
4.0X	667	533	0 1010 0A
5.0X	833	667	0 1011 0B
5.5X	917	733	0 1001 09
6.0X	1000	800	0 1101 0D
6.5X	1083	867	0 0101 05
7.0X	1167	933	0 0010 02
7.5X	1250	1000	0 0001 01
8.0X	1333	1067	0 1100 0C
8.5X	1417	1133	0 0110 06
9.0X	1500	1200	1 0111 17
9.5X	1583	1267	0 0111 07
10.0X	1667	1333	1 1010 1A
10.5X	1750	1400	1 1000 18
11.0X	1833	1467	1 1001 19
11.5X	1917	1533	0 0000 00
12.0X	2000	1600	1 1011 1B
12.5X	2083	1667	1 1111 1F
13.0X	2167	1733	1 0101 15
13.5X	2250	1800	0 1110 0E
14.0X	2333	1867	1 1100 1C
15.0X	2500	2000	1 0001 11
16.0X	2667	2133	1 1101 1D
17.0X	2833	2267	1 0000 10
18.0X	3000	2400	1 0010 12
20.0X	3333	2667	1 0011 13
21.0X	3500	2800	1 0100 14
24.0X	4000	3200	1 0110 16
28.0X	4667	3733	1 1110 1E

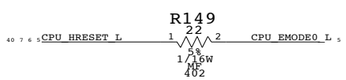
CPU CONFIGURATION

MAXBUS VSEL



DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L NEED TO CHARACTERIZE

BUSTYPE SELECT



APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

CPU CONFIGURATION

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE: NONE	SHT 7 OF 45	

INTREPID BOOT STRAPS

BIT 32 TO 39

MAXBUS_SLEEP

R642	R135	R123	R153	R166	R179	R651	R178
NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF
CPU_DATA<32>	CPU_DATA<33>	CPU_DATA<34>	CPU_DATA<35>	CPU_DATA<36>	CPU_DATA<37>	CPU_DATA<38>	CPU_DATA<39>

R136	R643	R639	R657	R664	R673	R143	R674
NO STUFF							
Output Impedance bit 2	Output Impedance bit 1	Output Impedance bit 0	PCI Arbiter Park to Low	PCI Arbiter Park to High	Spare	Spare	Spare

BIT 40 TO 47

MAXBUS_SLEEP

R122	R142	R164	R134	R184	R177	R152	R165
NO STUFF	NO STUFF	NO STUFF	EXT_CLK	NO STUFF	INT_CLK	INT_CLK	INT_CLK
CPU_DATA<40>	CPU_DATA<41>	CPU_DATA<42>	CPU_DATA<43>	CPU_DATA<44>	CPU_DATA<45>	CPU_DATA<46>	CPU_DATA<47>

R640	R652	R665	R644	R683	R675	R658	R666
			INT_CLK		EXT_CLK	EXT_CLK	EXT_CLK
Spare	Spare	BIT2	BIT1	BIT0	Disable Spread Spectrum	PCI1 Source Clock 0: PLL3 (NO SPREAD)	PCI0 Source Clock 0: PLL3 (NO SPREAD)

PLL4MODESEL_NXT[2:0]
000: 166.4MHZ (2.5X)
001: 149.76MHZ
010: 133.12MHZ (2.0X)
011: 99.84MHZ (1.5X)
100: 83.20MHZ

MODE A (2.5X) IS FOR STATIC OPERATION
MODE C (2.0X) IS FOR CLOCK SLEW OPERATION

BIT 48 TO 55

MAXBUS_SLEEP

R133	R121	R163	R151	R162	R141	R183	R176
EXT_CLK	EXT_CLK		NO STUFF	NO STUFF	NO STUFF		NO STUFF
CPU_DATA<48>	CPU_DATA<49>	CPU_DATA<50>	CPU_DATA<51>	CPU_DATA<52>	CPU_DATA<53>	CPU_DATA<54>	CPU_DATA<55>

R645	R641	R668	R659	R667	R653	R684	R676
INT_CLK	INT_CLK	NO STUFF				NO STUFF	
BUF_REF_CLK outputenable_h 1: Active	Select External source	Spare	BIT2	BIT1	BIT0	Spare	

MaxBus output impedance
111: 28.6 ohm
011: 33.3 ohm
101: 40 ohm
001: 50 ohm
110: 66.6 ohm
010: 100 ohm
100: 200 ohm
000: 200 ohm

THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:
1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
2/ D46 - SELPCI1SPREADCLK - SLEEP/WAKE CYCLE REQUIRED
3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT

IF A STRAP IS NOT LISTED, THEN
IT CANNOT BE CHANGED BY SOFTWARE

+1_5V_INTREPID_PLL — R227 4.7 5% 1/16W MF 402 — +1_5V_INTREPID_PLL7

C308 0.22UF 20% 6.3V CERM 2 402

H26

VDD15A_7 (PIL6) OMIT CRITICAL

U45 INTREPID-REV2.1 BGA

CPU_BR_L	E29	BR	INPUT
CPU_BG_L	E26	BG	NO BUS KEEPER
CPU_TS_L	B27	TS	NO BUS KEEPER

(1 OF 9)

CPU_ADDR<0>	D24	A_0
CPU_ADDR<1>	D25	A_1
CPU_ADDR<2>	A27	A_2
CPU_ADDR<3>	E24	A_3
CPU_ADDR<4>	G23	A_4
CPU_ADDR<5>	B26	A_5
CPU_ADDR<6>	A26	A_6
CPU_ADDR<7>	D23	A_7
CPU_ADDR<8>	A25	A_8
CPU_ADDR<9>	E23	A_9
CPU_ADDR<10>	J22	A_10
CPU_ADDR<11>	B25	A_11
CPU_ADDR<12>	H22	A_12
CPU_ADDR<13>	G22	A_13
CPU_ADDR<14>	D22	A_14
CPU_ADDR<15>	B24	A_15
CPU_ADDR<16>	B23	A_16
CPU_ADDR<17>	E22	A_17
CPU_ADDR<18>	J21	A_18
CPU_ADDR<19>	G21	A_19
CPU_ADDR<20>	E21	A_20
CPU_ADDR<21>	A24	A_21
CPU_ADDR<22>	D21	A_22
CPU_ADDR<23>	A23	A_23
CPU_ADDR<24>	H20	A_24
CPU_ADDR<25>	B22	A_25
CPU_ADDR<26>	H21	A_26
CPU_ADDR<27>	A22	A_27
CPU_ADDR<28>	E20	A_28
CPU_ADDR<29>	B21	A_29
CPU_ADDR<30>	D20	A_30
CPU_ADDR<31>	A21	A_31

MAXBUS INTERFACE

CPU_CI_L	G26	CI	
CPU_GBL_L	A29	GBL	
CPU_TBST_L	A28	TBST	
CPU_TSIZ<0>	G24	TSIZ_0	
CPU_TSIZ<1>	H24	TSIZ_1	
CPU_TSIZ<2>	D26	TSIZ_2	
CPU_TT<0>	E25	TT_0	
CPU_TT<1>	G25	TT_1	
CPU_TT<2>	B28	TT_2	
CPU_TT<3>	D27	TT_3	
CPU_TT<4>	J25	TT_4	
CPU_WT_L	D28	WT	
CPU_AACK_L	B29	AACK	NO BUS KEEPER - PU
CPU_ARTRY_L	H23	ARTRY	NO BUS KEEPER - PU
CPU_HIT_L	B31	HIT	INPUT - PU
CPU_QREQ_L	A32	QREQ	INPUT - PD
CPU_QACK_L	G27	QACK	NO BUS KEEPER - ?
INT_SUSPEND_REQ_L	AK9	SUSPENDREQ	
INT_SUSPEND_ACK_L	AM8	SUSPENDACK	

Vin = Intrepid Vcore (1.5V)
Vout = MaxBus rail (1.8V)

FB BUFFER HAS 50 OHM OUTPUT IMPEDANCE

INT_CPUFB_IN	J24	CPU_FB_IN	
INT_CPUFB_OUT	H16	CPU_FB_OUT	NO BUS KEEPER - PU
SYSCLK_LA_TP	G8	ANALYZER_CLK	
CPU_CLK_EN	AH9	STOPCPUCLK	INPUT - PU
INTREPID_ACS_REF	H13	ACS_REF	NO BUS KEEPER - PU
SYSCLK_CPU_UF	J15	CPU_CLK	NO BUS KEEPER - PU
CPU_TBEN	A31	TBEN	NO BUS KEEPER - PU

INTREPID OUTPUTS HIGH BY DEFAULT

CPU_DBG_L	A30	DBG_L	
CPU_DRDY_L	G28	DRDY_L	
CPU_DTI<0>	K25	DTI_0	
CPU_DTI<1>	D29	DTI_1	
CPU_DTI<2>	B30	DTI_2	
CPU_TA_L	E27	TA_L	
CPU_TEA_L	E28	TEA_L	

VSSA_7 (PLL6)
H25

R197 511 1% 1/16W MF 402

R144 0 5% 1/16W MF 402 — SYSCLK_CPU1

R137 1K 1% 1/16W MF 402

SHORT = 1" SHORTER THAN MATCHED LENGTH
LONG = 1" LONGER THAN MATCHED LENGTH

R167	R215	R207
0 5% 1/16W MF 402	0 5% 1/16W MF 402	NO STUFF
INT_CPUFB_OUT	INT_CPUFB_OUT_SHORT	INT_CPUFB_OUT_NORM

INT_CPUFB_LONG

R225	R208	R226	R196
NO STUFF	NO STUFF	0 5% 1/16W MF 402	0 5% 1/16W MF 402

INT_CPUFB_IN — INT_CPUFB_IN_NORM

MAXBUS PULL-UPS

MAXBUS_SLEEP

CPU_TS_L	RP21 10K 5% 1/16W SM1	2 7
CPU_TA_L	RP21 10K 5% 1/16W SM1	1 8
CPU_ARTRY_L	RP21 10K 5% 1/16W SM1	4 5
CPU_BR_L	RP23 10K 5% 1/16W SM1	1 8
CPU_HIT_L	RP24 10K 5% 1/16W SM1	3 6
CPU_DRDY_L	RP23 10K 5% 1/16W SM1	3 6
CPU_TEA_L	RP23 10K 5% 1/16W SM1	4 5
CPU_AACK_L	RP23 10K 5% 1/16W SM1	2 7
CPU_DBG_L	RP24 10K 5% 1/16W SM1	4 5
CPU_BG_L	RP21 10K 5% 1/16W SM1	3 6
CPU_QREQ_L	RP24 10K 5% 1/16W SM1	2 7

INTREPID BOOT STRAPS

BIT 56 TO 63

MAXBUS_SLEEP

R140	R161	R175	R132	R131	R150	R174	R182
NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF		NO STUFF
CPU_DATA<56>	CPU_DATA<57>	CPU_DATA<58>	CPU_DATA<59>	CPU_DATA<60>	CPU_DATA<61>	CPU_DATA<62>	CPU_DATA<63>

R654	R669	R677	R646	R647	R660	R678	R685
						NO STUFF	
Spare	Spare	Spare	PCI1_REQ2_L / PCI1_GNT2_L 1: GPIO5	PCI1_REQ1_L / PCI1_GNT1_L 1: GPIO3	PCI1_REQ0_L / PCI1_GNT0_L 1: GPIO2	Disable PCI interface 1: B mode	Processor Bug Mode 1: 60X Bus (63)

Intrepid MaxBus

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE: NONE	SHT 8 OF 45	

SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

PINS ARE SWAPABLE FOR RPAKS

U45
INTREPID-REV2.1
BGA
(2 OF 9)
OMIT
CRITICAL

DDR MEMORY INTERFACE

DDR_DATA_0	AK32	MEM_DATA<0>	37 10
DDR_DATA_1	AK33	MEM_DATA<1>	37 10
DDR_DATA_2	AK31	MEM_DATA<2>	37 10
DDR_DATA_3	AK35	MEM_DATA<3>	37 10
DDR_DATA_4	AK36	MEM_DATA<4>	37 10
DDR_DATA_5	AJ32	MEM_DATA<5>	37 10
DDR_DATA_6	AJ35	MEM_DATA<6>	37 10
DDR_DATA_7	AJ36	MEM_DATA<7>	37 10
DDR_DATA_8	AG33	MEM_DATA<8>	37 10
DDR_DATA_9	AG35	MEM_DATA<9>	37 10
DDR_DATA_10	AH35	MEM_DATA<10>	37 10
DDR_DATA_11	AG36	MEM_DATA<11>	37 10
DDR_DATA_12	AH36	MEM_DATA<12>	37 10
DDR_DATA_13	AH32	MEM_DATA<13>	37 10
DDR_DATA_14	AG32	MEM_DATA<14>	37 10
DDR_DATA_15	AG31	MEM_DATA<15>	37 10
DDR_DATA_16	AE32	MEM_DATA<16>	37 10
DDR_DATA_17	AF35	MEM_DATA<17>	37 10
DDR_DATA_18	AF36	MEM_DATA<18>	37 10
DDR_DATA_19	AE36	MEM_DATA<19>	37 10
DDR_DATA_20	AE35	MEM_DATA<20>	37 10
DDR_DATA_21	AE33	MEM_DATA<21>	37 10
DDR_DATA_22	AD36	MEM_DATA<22>	37 10
DDR_DATA_23	AD35	MEM_DATA<23>	37 10
DDR_DATA_24	AA36	MEM_DATA<24>	37 10
DDR_DATA_25	AA35	MEM_DATA<25>	37 10
DDR_DATA_26	AA33	MEM_DATA<26>	37 10
DDR_DATA_27	AB36	MEM_DATA<27>	37 10
DDR_DATA_28	AB35	MEM_DATA<28>	37 10
DDR_DATA_29	AC36	MEM_DATA<29>	37 10
DDR_DATA_30	AA32	MEM_DATA<30>	37 10
DDR_DATA_31	AB33	MEM_DATA<31>	37 10
DDR_DATA_32	V36	MEM_DATA<32>	37 10
DDR_DATA_33	U33	MEM_DATA<33>	37 10
DDR_DATA_34	U32	MEM_DATA<34>	37 10
DDR_DATA_35	V35	MEM_DATA<35>	37 10
DDR_DATA_36	T30	MEM_DATA<36>	37 10
DDR_DATA_37	U36	MEM_DATA<37>	37 10
DDR_DATA_38	U35	MEM_DATA<38>	37 10
DDR_DATA_39	T36	MEM_DATA<39>	37 10
DDR_DATA_40	P33	MEM_DATA<40>	37 10
DDR_DATA_41	R30	MEM_DATA<41>	37 10
DDR_DATA_42	P35	MEM_DATA<42>	37 10
DDR_DATA_43	P36	MEM_DATA<43>	37 10
DDR_DATA_44	R36	MEM_DATA<44>	37 10
DDR_DATA_45	R35	MEM_DATA<45>	37 10
DDR_DATA_46	R33	MEM_DATA<46>	37 10
DDR_DATA_47	R32	MEM_DATA<47>	37 10
DDR_DATA_48	N35	MEM_DATA<48>	37 10
DDR_DATA_49	M36	MEM_DATA<49>	37 10
DDR_DATA_50	L35	MEM_DATA<50>	37 10
DDR_DATA_51	M35	MEM_DATA<51>	37 10
DDR_DATA_52	M33	MEM_DATA<52>	37 10
DDR_DATA_53	L36	MEM_DATA<53>	37 10
DDR_DATA_54	N33	MEM_DATA<54>	37 10
DDR_DATA_55	M30	MEM_DATA<55>	37 10
DDR_DATA_56	J32	MEM_DATA<56>	37 10
DDR_DATA_57	J33	MEM_DATA<57>	37 10
DDR_DATA_58	J35	MEM_DATA<58>	37 10
DDR_DATA_59	K32	MEM_DATA<59>	37 10
DDR_DATA_60	K33	MEM_DATA<60>	37 10
DDR_DATA_61	J36	MEM_DATA<61>	37 10
DDR_DATA_62	K36	MEM_DATA<62>	37 10
DDR_DATA_63	K35	MEM_DATA<63>	37 10

DDR_A_0	H35	MEM_ADDR<0>	9 37
DDR_A_1	G35	MEM_ADDR<1>	9 37
DDR_A_2	G36	MEM_ADDR<2>	9 37
DDR_A_3	F36	MEM_ADDR<3>	9 37
DDR_A_4	F35	MEM_ADDR<4>	9 37
DDR_A_5	E35	MEM_ADDR<5>	9 37
DDR_A_6	E36	MEM_ADDR<6>	9 37
DDR_A_7	G32	MEM_ADDR<7>	9 37
DDR_A_8	D36	MEM_ADDR<8>	9 37
DDR_A_9	H36	MEM_ADDR<9>	9 37
DDR_A_10	G33	MEM_ADDR<10>	9 37
DDR_A_11	H33	MEM_ADDR<11>	9 37
DDR_A_12	D35	MEM_ADDR<12>	9 37
DDR_BA_0	L30	MEM_BA<0>	9 37
DDR_BA_1	M29	MEM_BA<1>	9 37
DDRCS_0	AN34	MEM_CS_L<0>	9 37
DDRCS_1	AN36	MEM_CS_L<1>	9 37
DDRCS_2	AL35	MEM_CS_L<2>	9 37
DDRCS_3	AL33	MEM_CS_L<3>	9 37
DDR_DQS_0	AJ31	MEM_DQS<0>	10 37
DDR_DQS_1	AH31	MEM_DQS<1>	10 37
DDR_DQS_2	AD32	MEM_DQS<2>	10 37
DDR_DQS_3	AB30	MEM_DQS<3>	10 37
DDR_DQS_4	V30	MEM_DQS<4>	10 37
DDR_DQS_5	P32	MEM_DQS<5>	10 37
DDR_DQS_6	N29	MEM_DQS<6>	10 37
DDR_DQS_7	L32	MEM_DQS<7>	10 37
DDR_DM_0	AJ33	MEM_DQM<0>	10 37
DDR_DM_1	AH33	MEM_DQM<1>	10 37
DDR_DM_2	AD33	MEM_DQM<2>	10 37
DDR_DM_3	AC35	MEM_DQM<3>	10 37
DDR_DM_4	T35	MEM_DQM<4>	10 37
DDR_DM_5	T33	MEM_DQM<5>	10 37
DDR_DM_6	N32	MEM_DQM<6>	10 37
DDR_DM_7	L33	MEM_DQM<7>	10 37
DDRRAS	L29	MEM_RAS_L	9 37
DDRCAS	H32	MEM_CAS_L	9 37
DDRWE	K30	MEM_WE_L	9 37
DDRCKE0	AN35	MEM_CKE<0>	9 37
DDRCKE1	AM35	MEM_CKE<1>	9 37
DDRCKE2	AM36	MEM_CKE<2>	9 37
DDRCKE3	AL36	MEM_CKE<3>	9 37
DDR_SELHI_0	AB32	MEM_MUXSEL_H<0>	10 37
DDR_SELHI_1	AE29	MEM_MUXSEL_H<1>	10 37
DDR_SELLO_0	N30	MEM_MUXSEL_L<0>	10 37
DDR_SELLO_1	T32	MEM_MUXSEL_L<1>	10 37
DDR_MCLK_0_P	Y32	SYSCLK_DDRCLK_A0_UF	9 37
DDR_MCLK_0_N	Y33	SYSCLK_DDRCLK_A0_L_UF	9 37
DDR_MCLK_1_P	Y35	SYSCLK_DDRCLK_A1_UF	9 37
DDR_MCLK_1_N	Y36	SYSCLK_DDRCLK_A1_L_UF	9 37
DDR_MCLK_2_P	Y30	INT_DDRCLK2_P_TP	
DDR_MCLK_2_N	W30	INT_DDRCLK2_N_TP	
DDR_MCLK_3_P	W32	SYSCLK_DDRCLK_B0_UF	9 37
DDR_MCLK_3_N	W33	SYSCLK_DDRCLK_B0_L_UF	9 37
DDR_MCLK_4_P	V33	SYSCLK_DDRCLK_B1_UF	9 37
DDR_MCLK_4_N	V32	SYSCLK_DDRCLK_B1_L_UF	9 37
DDR_MCLK_5_P	W35	INT_DDRCLK5_P_TP	
DDR_MCLK_5_N	W36	INT_DDRCLK5_N_TP	
DDR_REF	AA22	INT_MEM_REF_H	39
DDR_VREF_0	Y22	INT_MEM_VREF	9 39
DDR_VREF_1	T22		

'0' & '1' GO TO SLOT A
'2' & '3' GO TO SLOT B

'0'S ARE SAME POLARITY (ACTIVE-LO)
'1'S ARE SAME POLARITY (ACTIVE-HI)

'0' & '1' GO TO SLOT A
'2' & '3' GO TO SLOT B

MEM_VREF

R199 1K 1% 1/16W MF 402

39 16 15 10 +2_5V_INTREPID

R198 10K 1% 1/16W MF 402

R191 10K 1% 1/16W MF 402

C245 0.1UF 20% 10V CERM 402

INT_MEM_VREF 9 39

CLOCKS

SYSCLK_DDRCLK_A1_UF	RP33 4	5	SYSCLK_DDRCLK_A1 11 37
SYSCLK_DDRCLK_A1_L_UF	RP33 3	6	SYSCLK_DDRCLK_A1_L 11 37
SYSCLK_DDRCLK_A0_UF	RP34 1	8	SYSCLK_DDRCLK_A0 11 37
SYSCLK_DDRCLK_A0_L_UF	RP34 2	7	SYSCLK_DDRCLK_A0_L 11 37
SYSCLK_DDRCLK_B1_UF	RP33 2	7	SYSCLK_DDRCLK_B1 11 37
SYSCLK_DDRCLK_B1_L_UF	RP33 1	8	SYSCLK_DDRCLK_B1_L 11 37
SYSCLK_DDRCLK_B0_UF	RP34 3	6	SYSCLK_DDRCLK_B0 11 37
SYSCLK_DDRCLK_B0_L_UF	RP34 4	5	SYSCLK_DDRCLK_B0_L 11 37

CS

MEM_CS_L<0>	RP36 1	8	RAM_CS_L<0> 11 37
MEM_CS_L<1>	RP36 3	6	RAM_CS_L<1> 11 37
MEM_CS_L<2>	RP35 4	5	RAM_CS_L<2> 11 37
MEM_CS_L<3>	RP35 2	7	RAM_CS_L<3> 11 37

CKE

MEM_CKE<0>	RP36 2	7	RAM_CKE<0> 9 11 37
MEM_CKE<1>	RP36 4	5	RAM_CKE<1> 9 11 37
MEM_CKE<2>	RP35 1	8	RAM_CKE<2> 9 11 37
MEM_CKE<3>	RP35 3	6	RAM_CKE<3> 9 11 37

ADDR

MEM_ADDR<0>	RP31 1	8	RAM_ADDR<0> 11 37
MEM_ADDR<1>	RP25 1	8	RAM_ADDR<1> 11 37
MEM_ADDR<2>	RP25 2	7	RAM_ADDR<2> 11 37
MEM_ADDR<3>	RP25 4	5	RAM_ADDR<3> 11 37
MEM_ADDR<4>	RP25 3	6	RAM_ADDR<4> 11 37
MEM_ADDR<5>	RP30 1	8	RAM_ADDR<5> 11 37
MEM_ADDR<6>	RP30 2	7	RAM_ADDR<6> 11 37
MEM_ADDR<7>	RP31 3	6	RAM_ADDR<7> 11 37
MEM_ADDR<8>	RP30 4	5	RAM_ADDR<8> 11 37
MEM_ADDR<9>	RP31 2	7	RAM_ADDR<9> 11 37
MEM_ADDR<10>	RP31 4	5	RAM_ADDR<10> 11 37
MEM_ADDR<11>	RP26 4	5	RAM_ADDR<11> 11 37
MEM_ADDR<12>	RP30 3	6	RAM_ADDR<12> 11 37

BA

MEM_BA<0>	RP26 2	7	RAM_BA<0> 11 37
MEM_BA<1>	RP26 1	8	RAM_BA<1> 11 37

CNTL

MEM_WE_L	RP26 3	6	RAM_WE_L 11 37
MEM_CAS_L	R250 1	2	RAM_CAS_L 11 37
MEM_RAS_L	R238 1	2	RAM_RAS_L 11 37

1MB BOOT ROM

+3V_MAIN

C460 2.2UF 20% 10V CERM 805

C470 0.1UF 20% 10V CERM 402

C479 0.1UF 20% 10V CERM 402

U17
3.3V
TSOP
OMIT

A0	21	DQ0	25
A1	20	DQ1	26
A2	19	DQ2	27
A3	18	DQ3	28
A4	17	DQ4	32
A5	16	DQ5	33
A6	15	DQ6	34
A7	14	DQ7	35
A8	8		
A9	7		
A10	36		
A11	6		
A12	5		
A13	4		
A14	3		
A15	2		
A16	1		
A17	40		
A18	13		
A19	37		
A20	38		
CE	22		
OE	24		
WE	9		
WP	12		
PWD	10		

VPP 11, VCC 30, 31, GND 23, 39

PCI_AD<0>	40 38 27 25 17 12
PCI_AD<1>	40 38 27 25 17 12
PCI_AD<2>	40 38 27 25 17 12
PCI_AD<3>	40 38 27 25 17 12
PCI_AD<4>	40 38 27 25 17 12
PCI_AD<5>	40 38 27 25 17 12
PCI_AD<6>	40 38 27 25 17 12
PCI_AD<7>	40 38 27 25 17 12
PCI_AD<8>	40 38 27 25 17 12
PCI_AD<9>	40 38 27 25 17 12
PCI_AD<10>	40 38 27 25 17 12
PCI_AD<11>	40 38 27 25 17 12
PCI_AD<12>	40 38 27 25 17 12
PCI_AD<13>	40 38 27 25 17 12
PCI_AD<14>	40 38 27 25 17 12
PCI_AD<15>	40 38 27 25 17 12
PCI_AD<16>	40 38 27 25 17 12
PCI_AD<17>	40 38 27 25 17 12
PCI_AD<18>	40 38 27 25 17 12
PCI_AD<19>	40 38 27 25 17 12
PCI_AD<20>	40 38 27 25 17 12
PCI_AD<24>	12 17 25 27 38 40
PCI_AD<25>	12 17 25 27 38 40
PCI_AD<26>	12 17 25 27 38 40
PCI_AD<27>	12 17 25 27 38 40
PCI_AD<28>	12 17 25 27 38 40
PCI_AD<29>	12 17 25 27 38 40
PCI_AD<30>	12 17 25 27 38 40
PCI_AD<31>	12 17 25 27 38 40

+3V_MAIN

R338 10K 5% 1/16W MF 402

R386 10K 5% 1/16W MF 402

R357 1K 5% 1/16W MF 402

40 25 12 ROM_CS_L

40 25 ROM_ONBOARD_CS_L

40 25 12 ROM_OE_L

40 25 12 ROM_RW_L

ROM_WP_L

31 13 INT_RESET_L

OVERRIDE ROM MODULE
INTERCEPTS ROM CHIP SELECT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1793	1	IC,BOOTROM,4.9.1F3,Q41B	U17	CRITICAL	?

PULL-DOWN RESISTORS TO ENSURE
CKE STAYS LOW AFTER INTREPID
2.5V I/O SHUTS OFF

37 11 9 RAM_CKE<0>
37 11 9 RAM_CKE<1>
37 11 9 RAM_CKE<2>
37 11 9 RAM_CKE<3>

R500 10K 5% 1/16W MF 402

R439 10K 5% 1/16W MF 402

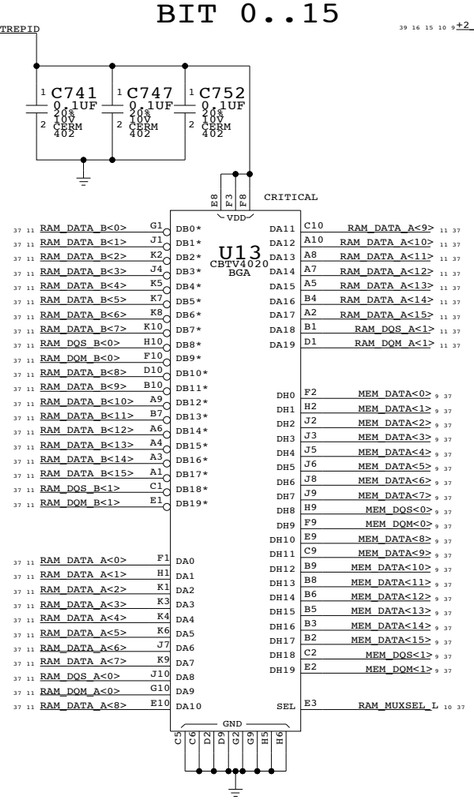
R409 10K 5% 1/16W MF 402

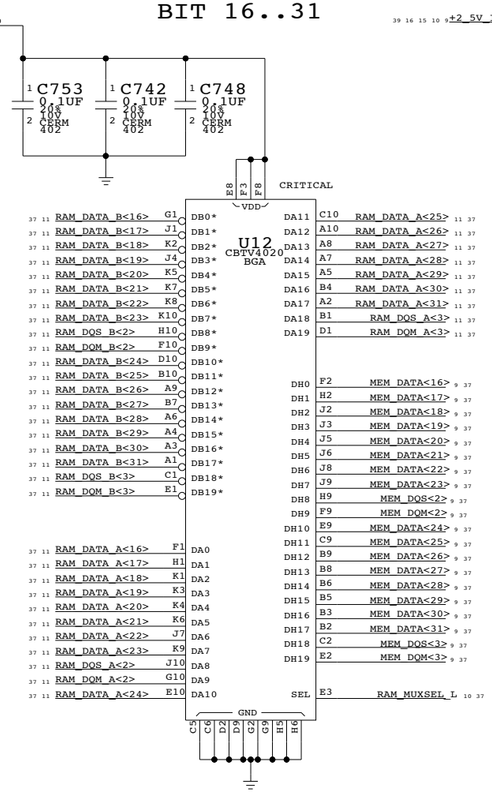
R387 10K 5% 1/16W MF 402

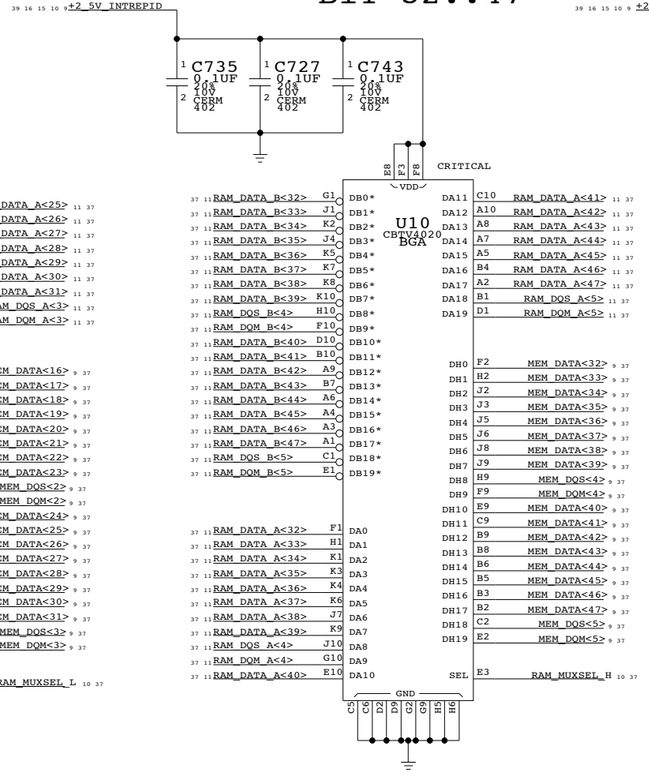
INT - DDR/BOOTROM

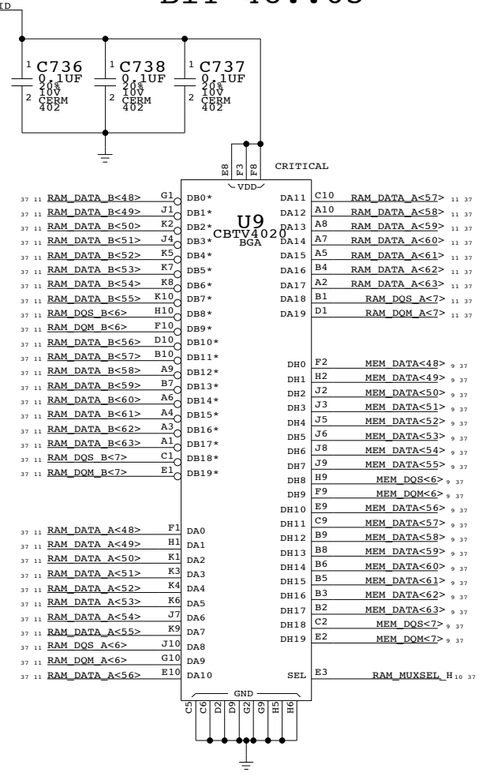
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE: NONE	SHT 9 OF 45	



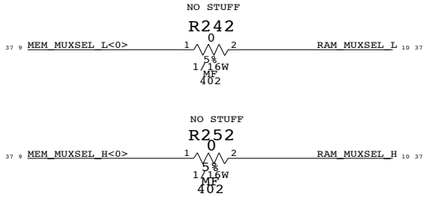


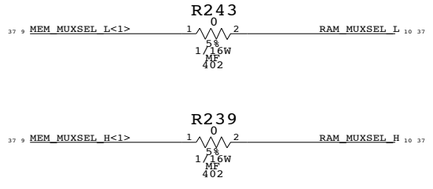




SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND
MEM_MUXSEL_H<0> AND MEM_MUXSEL_L<0> ARE ACTIVE LOW
MEM_MUXSEL_H<1> AND MEM_MUXSEL_L<1> ARE ACTIVE HIGH

ADDED 0 OHM RESISTORS IN CASE POLARITY IS WRONG



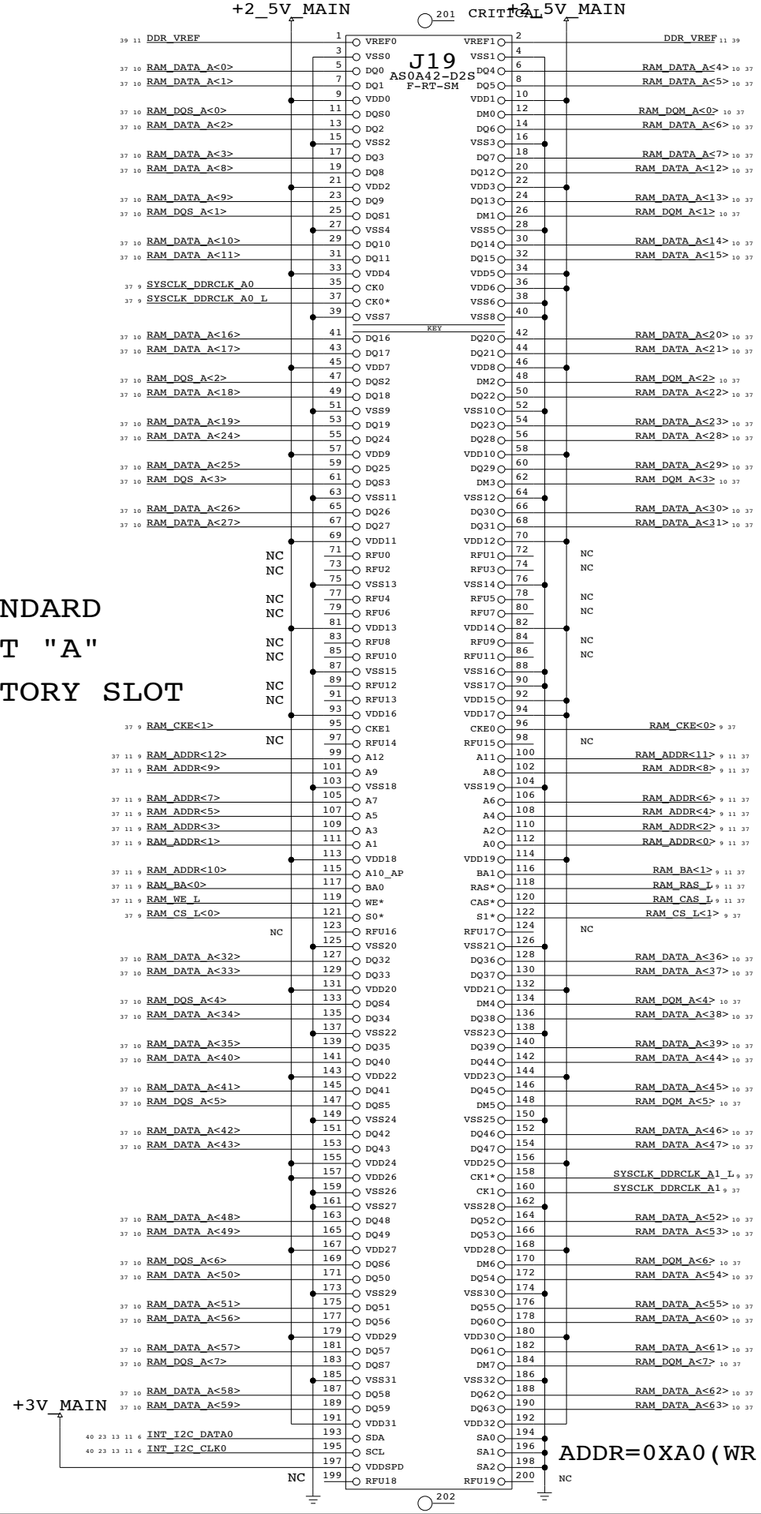


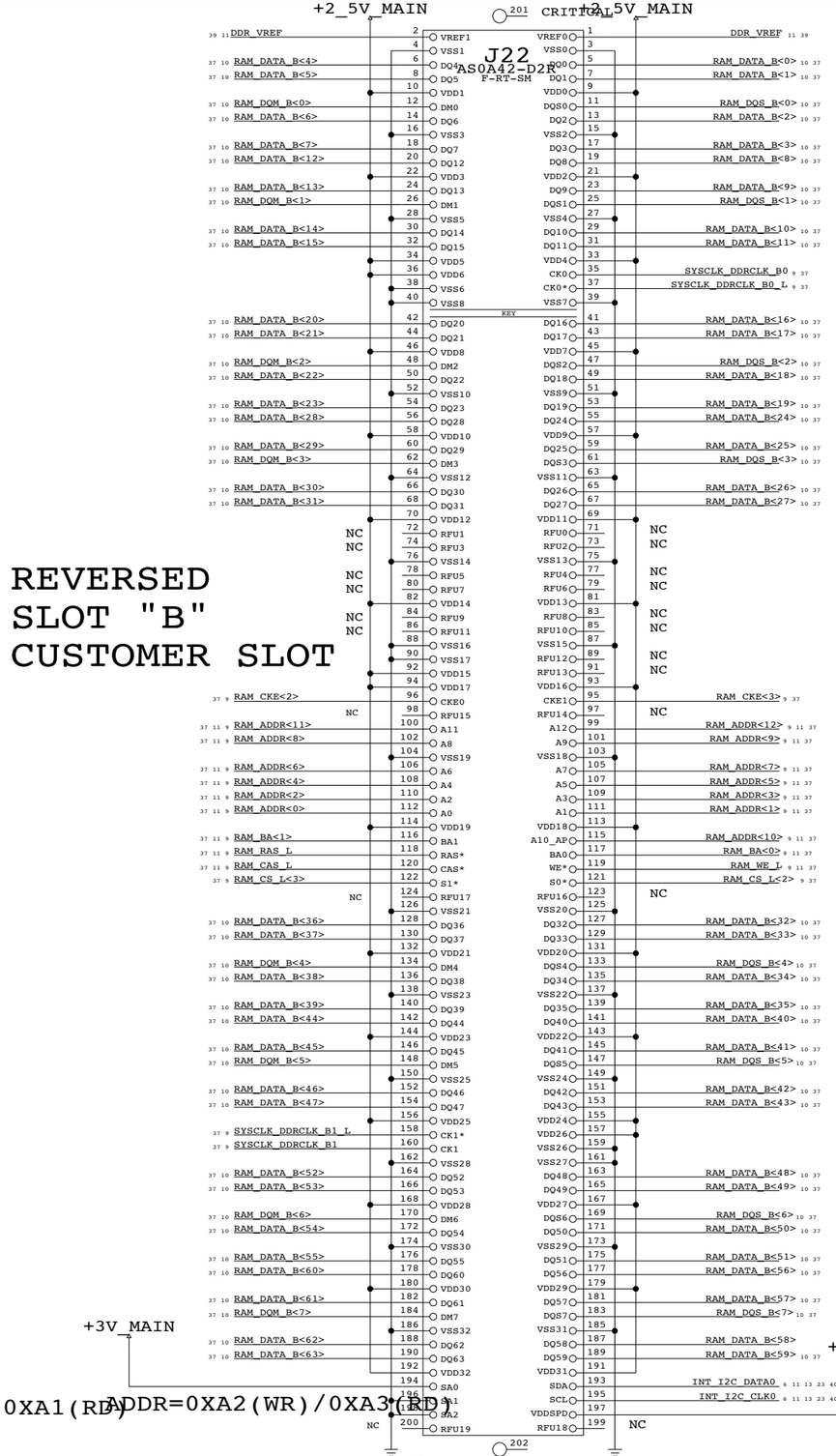
16BIT 2:1 DDR MUXES

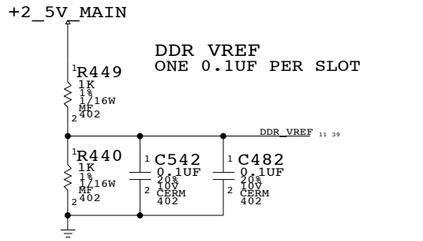
APPLE COMPUTER INC.

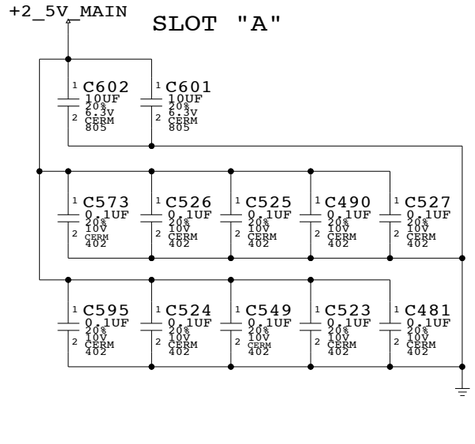
SIZE	DRAWING NUMBER	REV.
D	051-6694	G

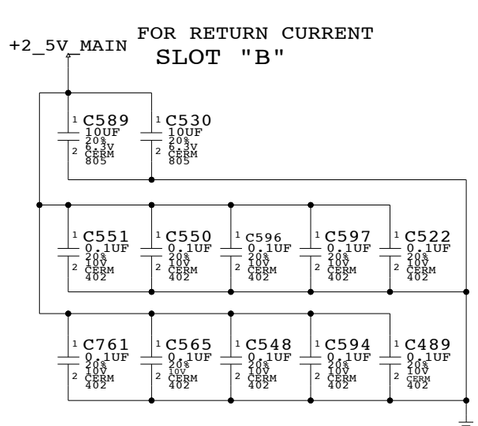
SCALE	SHT	OF
NONE	10	45











DDR SODIMM CONNS

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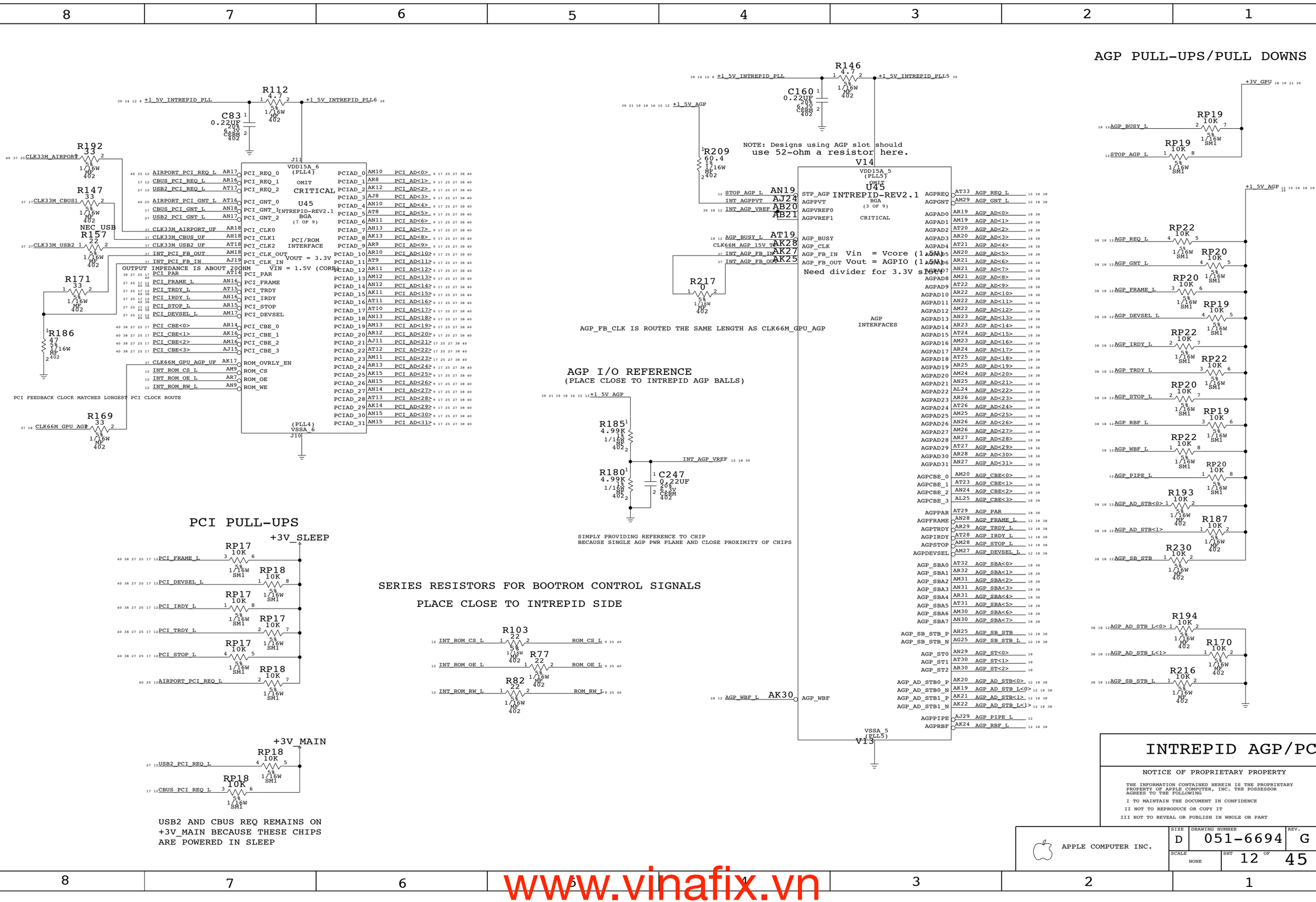
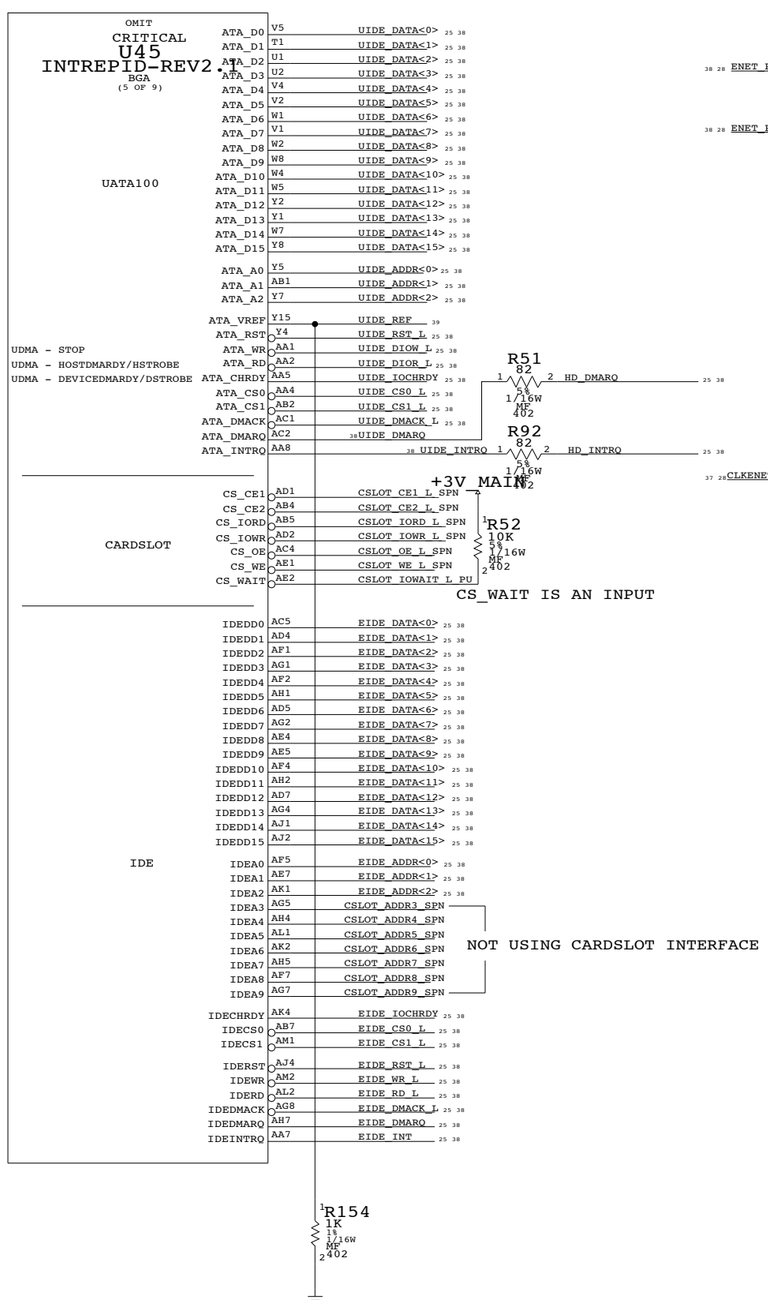
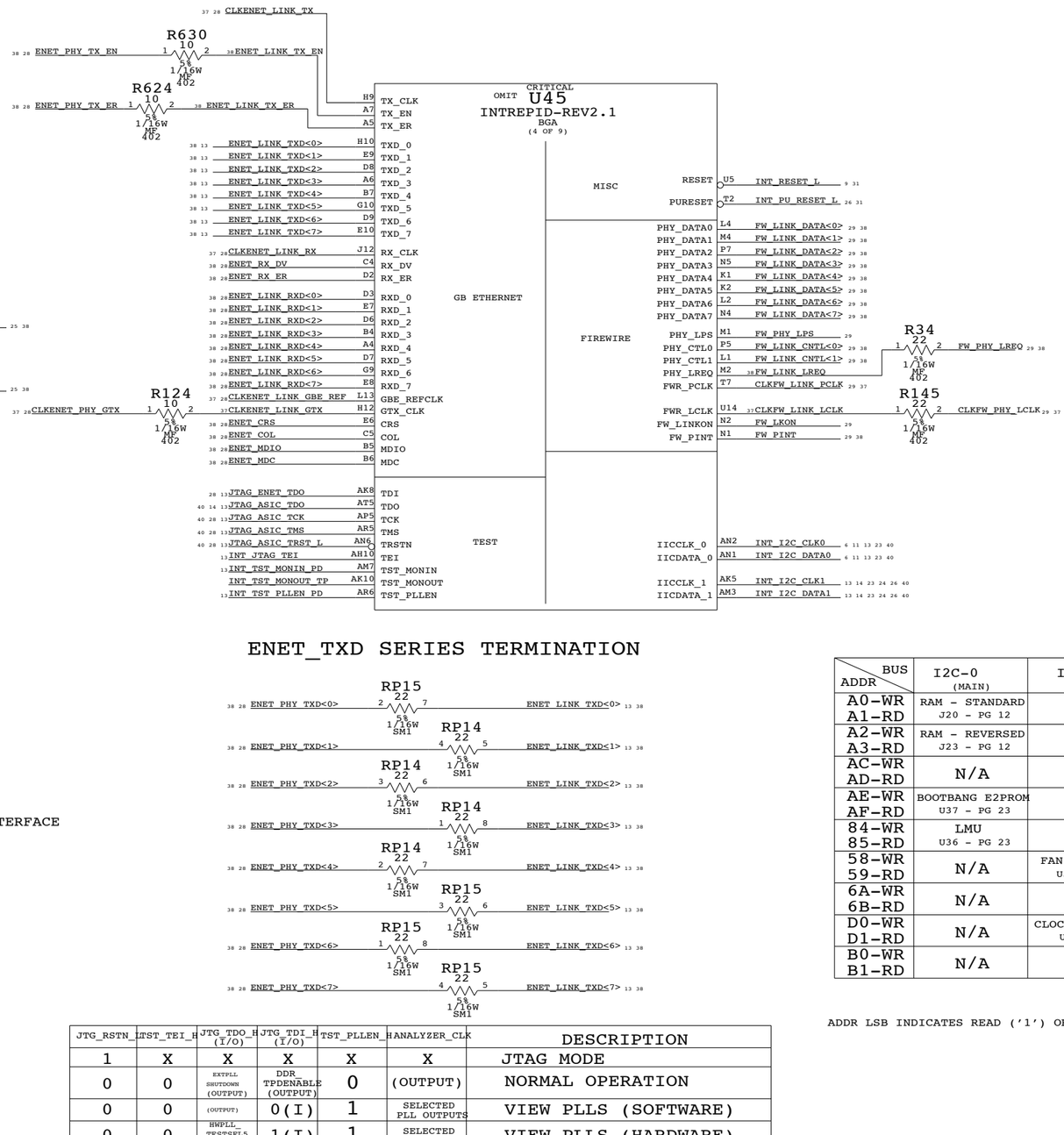
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G

SCALE	SHT
NONE	11 OF 45



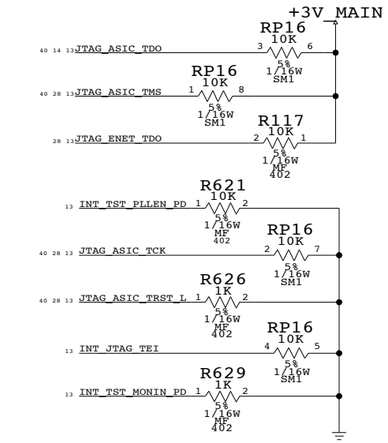




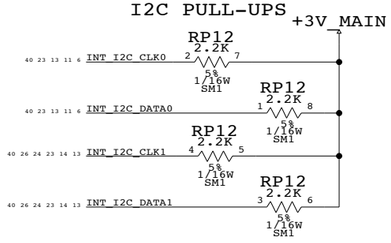
ENET_TXD SERIES TERMINATION

JTG_RSTN	TST_TEI_H	JTG_TDO_H (I/O)	JTG_TDI_H (I/O)	TST_PLLEN_H	ANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	EXTPLL SHUTDOWN (OUTPUT)	DDR_ TPDENABLE (OUTPUT)	0	(OUTPUT)	NORMAL OPERATION
0	0	(OUTPUT)	0(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	HWPLL_ TESTSEL5 (INPUT)	1(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0(I)	0(I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0(I)	1(I)	0	X(I)	ATPG IDDQ
0	1	0(I)	1(I)	1	X(I)	TEST TRI-STATE
0	1	1(I)	0(I)	0	X(I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1(I)	0(I)	1	X(I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1(I)	1(I)	X	X(I)	FUNCTIONAL TEST IDDQ

TEST PULL-UPS/DOWNS



I2C PULL-UPS



BUS / ADDR	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
A0-WR A1-RD	RAM - STANDARD J20 - PG 12	N/A	N/A	N/A
A2-WR A3-RD	RAM - REVERSED J23 - PG 12	N/A	N/A	N/A
AC-WR AD-RD	N/A	N/A	DASH MODEM J9 - PG 25	N/A
AE-WR AF-RD	BOOTBANG E2PROM U37 - PG 23	N/A	N/A	N/A
84-WR 85-RD	LMU U36 - PG 23	N/A	N/A	N/A
58-WR 59-RD	N/A	FAN CONTROLLER U3 - PG 24	N/A	N/A
6A-WR 6B-RD	N/A	N/A	SNAPPER SOUND J12 - PG 24	N/A
D0-WR D1-RD	N/A	CLOCK SLEW SSCG U56 - PG 15	N/A	N/A
B0-WR B1-RD	N/A	MMM	N/A	N/A

ADDR LSB INDICATES READ ('1') OR WRITE ('0') MODES

INT - ENET/FW/UATA EIDE/I2C

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SIZE D | DRAWING NUMBER 051-6694 | REV. G

SCALE NONE | SHT 13 OF 45

USB POWER FAULT SIGNALS

USB PORT ASSIGNMENTS

PORT A - RIGHT USB 1

PORT B - UNUSE

PORT C - LEFT USB

PORT D - MODEM

PORT E - BLUETOOTH

PORT F - TPAD

R89,R80 NEED PLACE NEAR TPAD CONNECTOR

PLACE R68 CLOSE TO INTREPID SIDE
OTHERWISE A LOT OF OVERSHOOT/UNDERSHOOT

CRYSTAL LOAD CAPACITANCE IS 16PF

HWPLL_TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
359S0074	359S0086	SSCG	U42	ALT FOR CY28512-2

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0090	1	XTAL,CER,LOW PROF,18,432MHZ,8X4.5MM,SMD	Y1	CRITICAL	?

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES,METAL FILM,10 K OHM,5,1/16W,0402,SM	R100	NO_SSCG

INT - USB/GPIOS/I2S

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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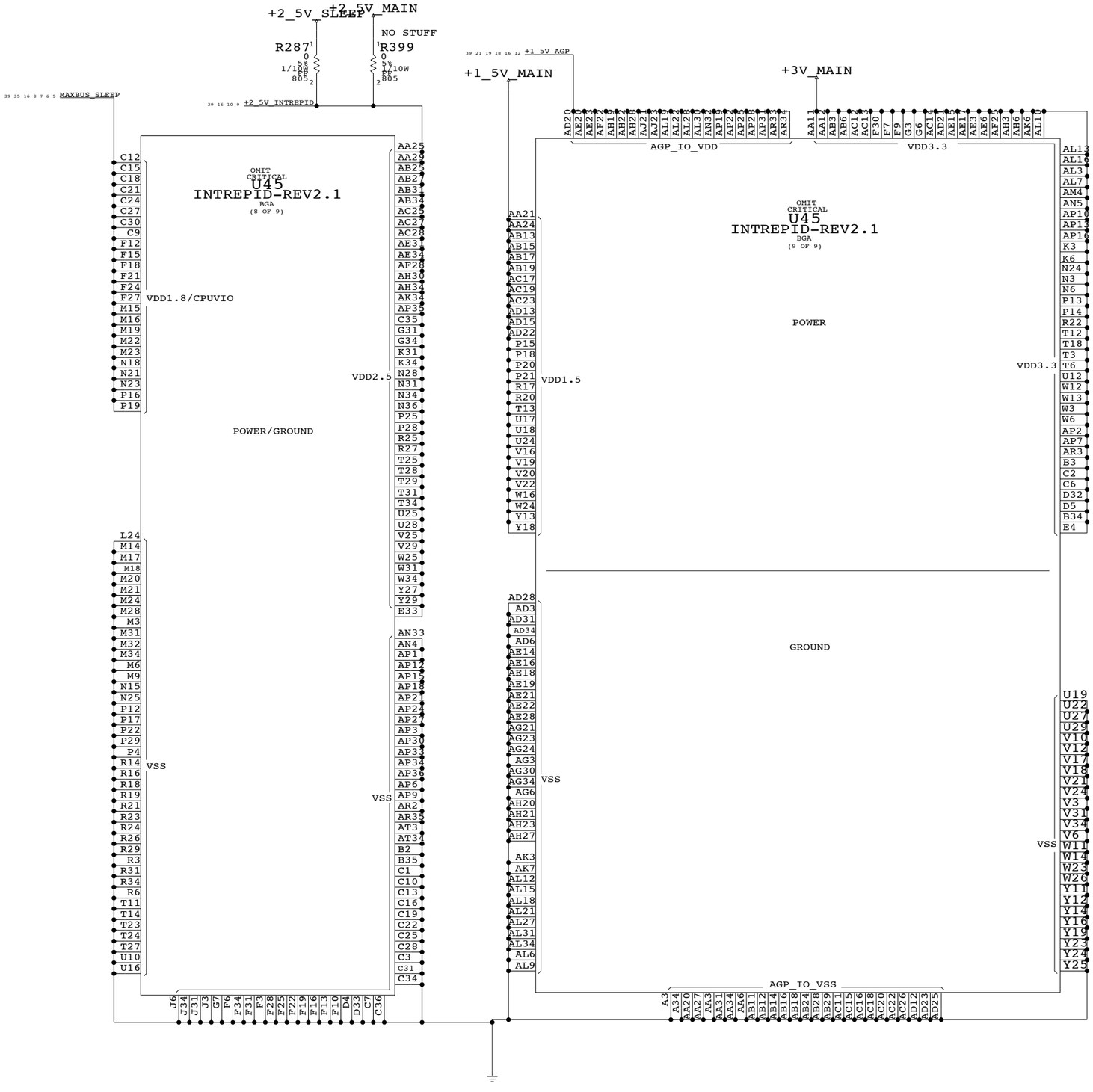
SCALE: NONE | SHT 14 OF 45



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0305	1	IC,ASIC,INTREPID,REV2.1,974BGA,FAST	U45	CRITICAL	?

Intrepid Power

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SCALE	SHT	OF
NONE	15	45

35 15 8 7 6 3 MAXBUS_SLEEP

INTREPID MAXBUS DECOUPLING

24 Balls
4 X 10UF (0805)
32 X 0.22UF (0402)

C204 10uF 20% 6.3V CERM 805 · C348 10uF 20% 6.3V CERM 805 · C236 10uF 20% 6.3V CERM 805 · C196 10uF 20% 6.3V CERM 805

C239 C240 C350 C312 C176 C288 C313 C94 C286 C158 C174 C206 C259 C237 C238 C95 C117 C241 C260 C314 C173 C171 C175 C226 C172 C207 C118 C287 C119 C349 C205 C209

0.22uF 20% 6.3V CERM 402

39 21 19 18 15 12 +1_5V_AGP

INTREPID AGP I/O DECOUPLING

21 Balls
4 X 10UF (0805)
24 X 0.22UF (0402)

C371 10uF 20% 6.3V CERM 805 · C231 10uF 20% 6.3V CERM 805 · C281 10uF 20% 6.3V CERM 805 · C394 10uF 20% 6.3V CERM 805

C356 C297 C268 C217 C355 C267 C250 C298 C377 C216 C228 C230 C265 C378 C357 C229 C325 C393 C324 C323 C251 C266 C249

0.22uF 20% 6.3V CERM 402

39 15 10 9 +2_5V_INTREPID

INTREPID DDR DECOUPLING

44 Balls
4 X 10UF (0805)
51 X 0.22UF (0402)

C422 10uF 20% 6.3V CERM 805 · C417 10uF 20% 6.3V CERM 805 · C418 10uF 20% 6.3V CERM 805 · C423 10uF 20% 6.3V CERM 805

C407 C391 C310 C317 C480 C390 C370 C320 C365 C366 C367 C292 C295 C403 C291 C352 C322 C392 C385 C376 C321 C318 C399 C410 C335 C369 C384 C294 C406 C405 C404 C400 C386 C289 C387 C401 C354 C389 C309 C398 C337 C290 C402 C397 C368 C334 C388 C293 C319 C336

0.22uF 20% 6.3V CERM 402

C316 0.22uF 20% 6.3V CERM 402

+1_5V_MAIN

INTREPID CORE DECOUPLING

30 Balls
4 X 10UF (0805)
29 X 0.22UF (0402)

C128 10uF 20% 6.3V CERM 805 · C101 10uF 20% 6.3V CERM 805 · C157 10uF 20% 6.3V CERM 805 · C315 10uF 20% 6.3V CERM 805

C147 C243 C262 C242 C227 C181 C142 C215 C278 C264 C244 C212 C178 C179 C177 C159 C161 C162 0.22uF C280 C279 C144 C246 C211 C263 C180 C213 C197 C208 C214

0.22uF 20% 6.3V CERM 402

+3V_MAIN

INTREPID 3.3V DECOUPLING

57 Balls
4 X 10UF (0805)
72 X 0.22UF (0402)

C164 10uF 20% 6.3V CERM 805 · C395 10uF 20% 6.3V CERM 805 · C10 10uF 20% 6.3V CERM 805 · C9 10uF 20% 6.3V CERM 805

C375 C351 C53 C42 C21 C185 C31 C143 C123 C121 C33 C184 C43 C35 C261 0.22uF C60 0.22uF C52 0.22uF C199 C57 C19 C16 C108 C55 C32 C125 C45 C76 C277 C28 C26 0.22uF C34 C23 C120 C146 C141 C30 0.22uF C145 C96 C54 C50 C75 C122 C51 C59 C163 C126 C98 C109 C56 C27 C296 C248 C210 C58 C22 C20 0.22uF C61 C44 C29 C24 C183 C18 C49 C36 C17 C99 C396 C124 C127 C100

0.22uF 20% 6.3V CERM 402

Intrepid Decoupling

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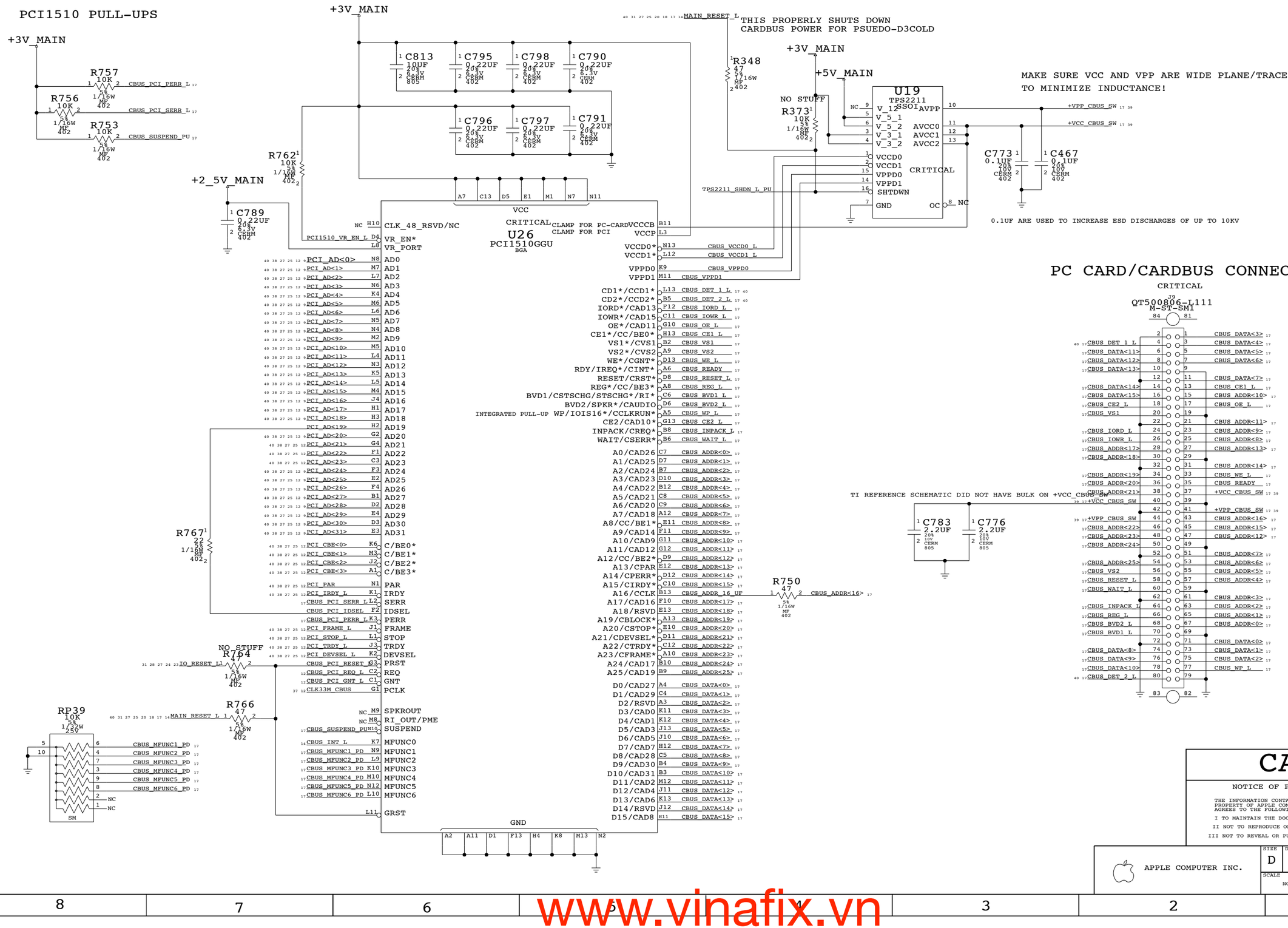
SCALE	SHT	OF
NONE	16	45



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0214	1	IC,ATI,M11-CSP128,GRPHCTLR,667BGA,HYNIX U44	U44	CRITICAL	M11_CSP128

27M OSC

(PLACE THE OSCILLATOR AND R189 AND R195 CLOSE TO ATI PIN AJ29)

+3V_SLEEP
L4 FERR-EMI-100-OHM SM
+3V ATI OSC SLEEP
C77 0.1uF 20% 10V CERM 402
C78 4.7uF 20% 6.3V CERM 805
NO STUFF R188 100K 5% 1/16W MF 402
CRITICAL
VCC
G2 27.0000M OSC SM-1
ATI OSC OE
OE
OUT
GND
ATI CLK27M OSC
(PLACE R200 CLOSE TO OSC)
GPU_SS
R200 0 5% 1/16W MF 402
ATI CLK27M OSC SS
R189 287 1% 1/16W MF 402
ATI CLK27M IN
R195 162 1% 1/16W MF 402

S0=1;S1=M => -1.5% DOWN-SPREAD
SPREAD SPECTRUM SUPPORT

+3V_SLEEP
GPU_SS
L3 FERR-EMI-100-OHM SM
+3V ATI SS
GPU_SS C70 10uF 20% 6.3V CERM 805
GPU_SS C71 0.1uF 20% 10V CERM 402
NO STUFF R173 0 5% 1/16W MF 402
GPU_SS R181 0 5% 1/16W MF 402
GPU_SS CRITICAL
U47 CY25811 SOI
ATI CLK27M OSC SS
XIN/CLKIN
XOUT
SSCLK
ATI SSCLK UF
NC
NC
FRSEL
CY25811 S1
CY25811 S0
S1
S0
VSS
GPU_SS R201 33 5% 1/16W MF 402
ATI SSCLK IN
NO STUFF R37 0 5% 1/16W MF 402
NO STUFF R38 0 5% 1/16W MF 402

U44 RAGE_MOBILITY M11-CSP64 64MB BGA (1 OF 6)

AGP_AD<31:0> AB30 AD31 … K28 AD0
AGP_CBE<3:0> W28 CBEB3 … N27 CBEB0
CLK66M_GPU_AGP AG30 PCICLK
AGP_FRAME_L U27 FRAMEB
AGP_IRDY_L T30 IRDYB
AGP_TRDY_L T28 TRDYB
AGP_STOP_L T27 STOPB
AGP_DEVSEL_L T29 DEVSELB
AGP_PAR R28 PAR
AGP_REQ_L AF29 REQB
AGP_GNT_L AF27 GNTB
AGP_INT_L AH29 INTAB
AGP_ATI_RESET_L AH30 RSTB
AGP_WBF_L AE27 WBF
AGP_ATI_VREFG AK3 VREFG
AGP_ATI_VREF D8 MVREF
VSS C19 P2 B18 P4 A19 R3 A18 R4 D19 P1 G29 G27 B29 C26 C16 A15 C11
AD_STB0 N29 AGP_AD_STB<0>
AD_STB1 W29 AGP_AD_STB<1>
AD_STBB0 M28 AGP_AD_STB_L<0>
AD_STBB1 Y29 AGP_AD_STB_L<1>
AGP_BUSYB AG28 AGP_BUSY_L
AGPREF K30
AGPTEST K29 GPU_AGP_TEST
AGP8X_DETB U25 AGP8X_DET_PU
SUS_STAT AJ28 AGP_SUS_STAT_L_PU
ST0 AF30 AGP_ST<0>
ST1 AF28 AGP_ST<1>
ST2 AE29 AGP_ST<2>
SBA7 AC28 AGP_SBA<7>
SBA6 AB29 AGP_SBA<6>
SBA5 AC27 AGP_SBA<5>
SBA4 AC30 AGP_SBA<4>
SBA3 AD27 AGP_SBA<3>
SBA2 AD30 AGP_SBA<2>
SBA1 AE28 AGP_SBA<1>
SBA0 AD29 AGP_SBA<0>
RBFB AE30 AGP_RBF_L
STP_AGPB AG29 AGP_STP_L
SB_STB AC29 AGP_SB_STB
SB_STBS AD28 AGP_SB_STB_L
RSTB_MSK AD24 ATI_RSTB_MSK
DBI_LO Y25 ATI_DBI_LO_PU
DBI_HI Y27 ATI_DBI_HI_PU
OMIT
A10 C5 A3 G4 E2 U2 V4 AB2 AC4 B23 K2 A23 K1 B22 L2 A22 L1
VSS
AC10 GPU_THERM_DP_TP
AC11 GPU_THERM_DM_TP
E8 +GPU_MEM
J6 (PULL-UP to GPU_MEM_IO)
TEST_YCLK
TEST_MLCK
C8 ATI_MEMTEST
MEMTEST
PLLTEST
AC22 NC
B7 MEMVMODE0
B6 MEMVMODE1

U44 RAGE_MOBILITY M11-CSP64 64MB BGA (6 OF 6)

M2 P3 A21 B19 M15 N15 P15 R15 T15 T12 T13 T14 W16 V16 U16 T16 R16 R17 R18 R19
VSS
U6 AF15 F18 P25
VDDCI
OMIT

U44 RAGE_MOBILITY M11-CSP64 64MB BGA (2 OF 6)

B26 A26 B25 A25 C22 D21 C21 D20 C20 D22 C23 D23 A27 B27 H2 H1 J2 J1 K4 K3 L4 M3 L3 M4 N2 N1 N4 N3 G30 G28 D16 B30 D26 B15 D11 B10 D5 B3 G3 E1 U1 V3 AB1 AC3 J30 J29 H30 H29 F30 F29 E30 E29 J28 J27 H28 H27 F28 F27 E28 E27 D30 D29 C30 C29 A30 A29 A28 B28 B28 C28 D27 C27 D25 C25 D24 C24 D18 C18 D17 C17 D15 C15 D14 C14 B17
VSS
A17 B16 A16 B14 A14 B13 A13 D13 C13 D12 C12 D10 C10 D9 C9 B12 A12 B11 A11 B9 A9 B8 A8 C7 D7 C6 D6 C4 D4 C3 D3 A5 B5 A4 B4 A2 B2 A1 B1 E4 E3 F3 F4 H3 H4 J3 J4 C1 C2 D1 D2 F1 F2 G1 G2 R1 R2 T1 T2 V1 V2 W1 W2 T3 T4 U3 U4 W3 W4 Y3 Y4 Y1 Y2 AA1 AA2 AC1 AC2 AD1 AD2 AA3 AA4 AB3 AB4 AD3 AD4 AE3 AE4
VSS

MAIN_RESET_L IS TOGGLED FOR SLEEP
+3V_GPU
R53 47 5% 1/16W MF 402
MAIN_RESET_L
R54 10K 5% 1/16W MF 402

R43 1K 1% 1/16W MF 402 +3V_GPU
R44 1K 1% 1/16W MF 402 +GPU_MEM
R45 1K 1% 1/16W MF 402
PLACE VREF VOLTAGE DIVIDER CLOSE TO ATI M10 VREF PIN
R46 1K 1% 1/16W MF 402
C11 0.1uF 20% 10V CERM 402
C37 10uF 20% 6.3V CERM 805

R119 47 5% 1/16W MF 402 +1_5V_AGP
R127 10K 5% 1/16W MF 402 +3V_GPU
R159 20K 5% 1/16W MF 402
INT_AGP_VREF
C62 0.1uF 20% 10V CERM 402
C63 0.01uF 20% 16V CERM 402
(PLACE C1002 CLOSE TO AGPREF PIN)
OMIT
R172 20K 5% 1/16W MF 402 +3V_GPU
R158 0 5% 1/16W MF 402
R126 47K 5% 1/16W MF 402 +1_5V_AGP
R138 47K 5% 1/16W MF 402
R118 45.3 1% 1/16W MF 402

+1_8V_GPU
ATI_MEMIO_LO R55 4.7K 5% 1/16W MF 402
ATI_MEMIO_HI R104 4.7K 5% 1/16W MF 402
ATI_MEMIO_HI R70 4.7K 5% 1/16W MF 402
ATI_MEMIO_LO R105 4.7K 5% 1/16W MF 402
FOR 2.5 VDDR1
MEMVMODE0=1.8V
MEMVMODE1=GND
FOR 1.8 VDDR1
MEMVMODE0=GND
MEMVMODE1=1.8V

GPU_VCORE
L2 60-OHM-EMI SM
GPU_VCORE_VDDCI
C64 0.01uF 20% 16V CERM 402
C67 10uF 20% 6.3V CERM 805
C65 0.01uF 20% 16V CERM 402
C68 0.01uF 20% 16V CERM 402
C66 0.01uF 20% 16V CERM 402
C69 0.01uF 20% 16V CERM 402

M11 AGP INTERFACE

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SCALE: NONE	SHT 18 OF 45	

GPU VCORE - 1.2V

(PUT ALL CAPs BELOW ATI ASIC)

M10 Power Shut down Sequencing

GPU VCORE SUPPLY

+PBUS

WHEN VCORE_CNTL HIGH => 1.2V
1.2V = 0.8V * (1 + R332 / (R331//R333))

WHEN VCORE_CNTL LOW => 1.0V
1.0V = 0.8V * (1 + R332 / R333)

R210,R99,R110 PLACE NEAR ATI CHIP

M11 CORE PWR/LVDS/TMDS

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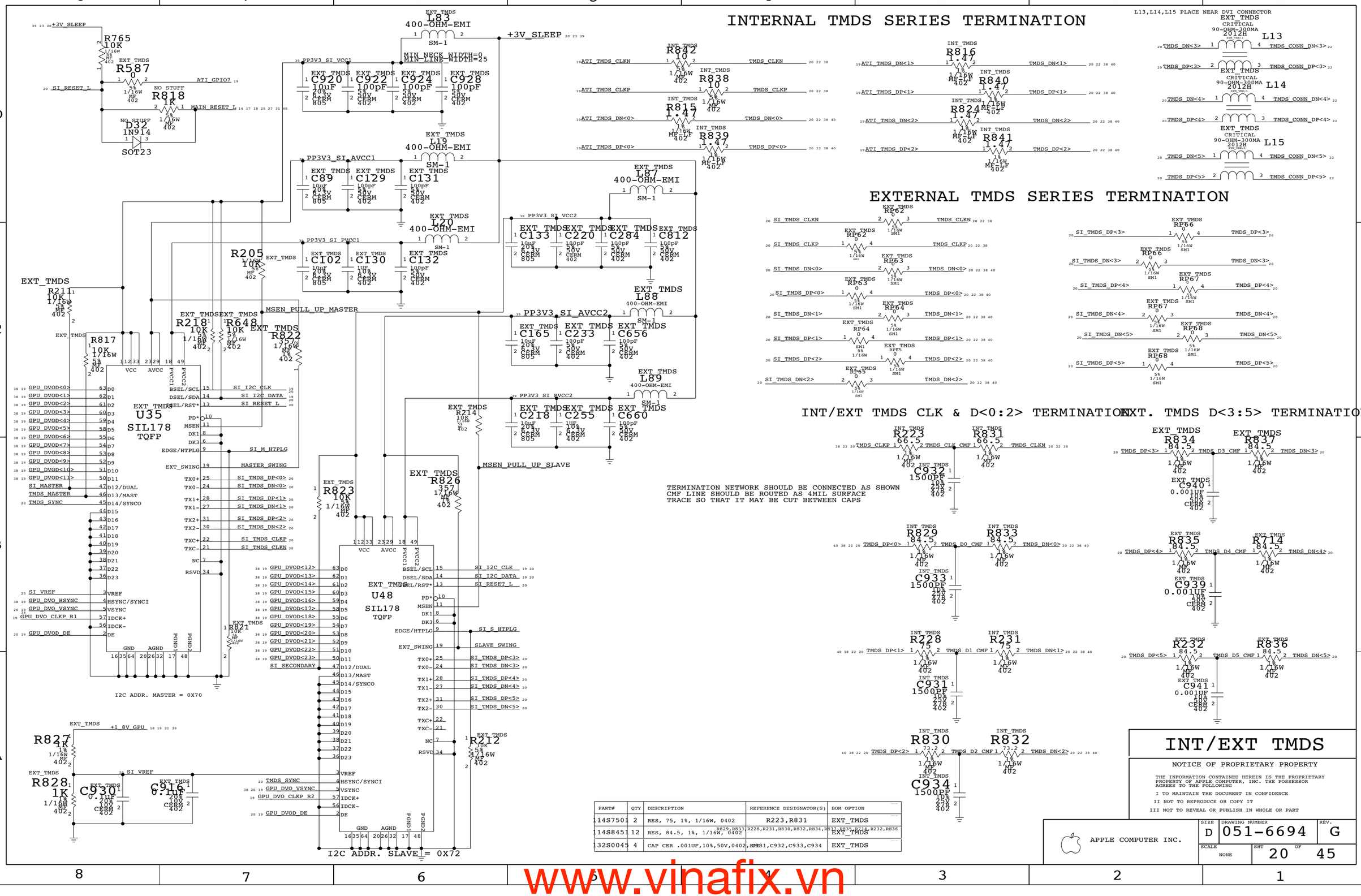
SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE: NONE	SHT 19 OF 45	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S7501	2	RES, 75, 1%, 1/16W, 0402	R223,R831	EXT_TMDS
114S8451	12	RES, 84.5, 1%, 1/16W, 0402	R829,R833,R228,R231,R830,R832,R834,R837,R835,R714,R232,R836	EXT_TMDS
132S0045	4	CAP CER .001UF,10%,50V,0402,X7R	C931,C932,C933,C934	EXT_TMDS

GPU PLL - 1.8V

+2_5V_GPU → U55 MM1571J (100mA MAX) SOT-25A (CRITICAL) → +1_8V_ATI_PVDD (Total PVDD = 66mA)
GPU_CORE_OK, CONT_NOISE, ATI_PVDD_BYP
C889 1UF 10% 6.3V CERM 603
C379 0.01uF 20% 16V CERM 402
C380 10uF 20% 6.3V CERM 805

+2_5V_GPU → L58 FERR-220-OHM 0402 (140mA) → +2_5V_GPU_A2VDD
C360 10uF 20% 6.3V CERM 805
C364 0.01uF 20% 16V CERM 402
C374 0.01uF 20% 16V CERM 402

+1_8V_GPU → L55 FERR-220-OHM 0402 (2mA) → +1_8V_GPU_AVDDQ
C339 10uF 20% 6.3V CERM 805
C363 0.01uF 20% 16V CERM 402

+1_8V_GPU → L56 FERR-220-OHM 0402 (AVDD+VDDDI=75mA) → +1_8V_GPU_VDDDI
C358 10uF 20% 6.3V CERM 805
C361 0.01uF 20% 16V CERM 402
C372 0.01uF 20% 16V CERM 402

+GPU_MEM → L57 FERR-220-OHM 0402 → +GPU_MCLK
C359 10uF 20% 6.3V CERM 805
C362 0.01uF 20% 16V CERM 402
C373 0.01uF 20% 16V CERM 402

+1_5V_SLEEP → R722 0 5% 1/10W MF 805 → +1_5V_AGP
1.5V

+1_8V_SLEEP → R284 0 5% 1/10W MF 805 → +1_8V_GPU
1.8V

+1_8V_SLEEP, +2_5V_SLEEP
ATI_MEMIO_LO → R729 0 5% 1/4W FF 1210
ATI_MEMIO_HI → R728 0 5% 1/4W FF 1210 → +GPU_MEM
1.8V
2.5V

+3V_GPU → U8 MAX8860 OMIT (UMAX) IN, SHDN*, SET, GND, OUT1, OUT2, FAULT*, CC
C910 2.2UF 20% 6.3V CERM1 603
C911 0.033UF 20% 10V X7R 402
R635 100K 5% 1/16W MF 402 → MAX8860_FAULT
C912 2.2UF 20% 6.3V CERM1 603
+2_8V_GPU_LVDS_LDO

+2_5V_SLEEP → R721 0 5% 1/10W MF 805 → +2_5V_GPU
2.5V

+3V_SLEEP → R299 0 5% 1/10W MF 805 → +3V_GPU
3.3V

GPU POWER SOURCES - 1.5V, 1.8V, 2.5V & 3.3V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S0828	1	IC,MAX8860,LDO,2.77V	U8	?

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0647	353S0828	?	U8	ALT FOR 2.82V PART

GPU PLL - 1.8V

+1_8V_GPU → L65 FERR-220-OHM 0402 → +1_8V_GPU_PLL (21mA)
C438 10uF 20% 6.3V CERM 805
C865 0.1uF 20% 10V CERM 402
C716 0.01uF 20% 16V CERM 402

+1_8V_GPU → L66 FERR-220-OHM 0402 → +1_8V_GPU_AVDD (AVDD+VDDDI=75mA)
C415 10uF 20% 6.3V CERM 805
C437 0.01uF 20% 16V CERM 402
C870 0.01uF 20% 16V CERM 402

AK29 PVDD
AF23 AVDD0
AF24 AVDD1
AE21 A2VDD0 ← +2_5V_GPU_A2VDD
AF21 A2VDD1
AJ23 A2VDDQ ← +1_8V_GPU_AVDDQ
AH23 VDD1DI ← +1_8V_GPU_VDDDI
AF20 VDD2DI
F19 VDDRH0 ← +GPU_MCLK
N6 VDDRH1

AGP 4X I/O - 1.5V

+1_5V_AGP → L59 FERR-10-OHM-500MA SM → +1_5V_AGP_GPU (20mA)
C381 0.1uF 20% 10V CERM 402
C420 0.1uF 20% 10V CERM 402
C446 0.1uF 20% 10V CERM 402
C543 0.1uF 20% 10V CERM 402
C871 10uF 20% 6.3V CERM 805
C382 0.01uF 20% 16V CERM 402
C421 0.01uF 20% 16V CERM 402
C447 0.01uF 20% 16V CERM 402
C671 0.01uF 20% 16V CERM 402

K25 L25 T25 Y28 K27 AA25 K26 L26 M26 N26 P26 R26 T26 U26 V26 Y26 AA26 AB26 AC26 VDDP

MEMORY CORE - 2.5V

+GPU_MEM → L63 FERR-220-OHM 0805 → +GPU_MEMCORE (1800mA)
C383 0.1uF 20% 10V CERM 402
C425 0.1uF 20% 10V CERM 402
C866 0.1uF 20% 10V CERM 402
C672 0.1uF 20% 10V CERM 402
C715 10uF 20% 6.3V CERM 805
C408 0.01uF 20% 16V CERM 402
C426 0.01uF 20% 16V CERM 402
C450 0.01uF 20% 16V CERM 402
C701 0.01uF 20% 16V CERM 402

E5 E6 E12 E13 E18 E19 E20 E26 F26 VDDM

LVDS PLL - 1.8V

+1_8V_ATI_PVDD → L61 FERR-220-OHM 0402 → +1_8V_GPU_ENLPLL (40mA)
C409 10uF 20% 6.3V CERM 805
C428 0.01uF 20% 16V CERM 402
C867 0.01uF 20% 16V CERM 402
EXT_TMDS R279 0 5% 1/16W MF 603 → +1_8V_GPU_TP_PLL
C877 10uF 20% 6.3V CERM 805
C878 0.01uF 20% 16V CERM 402

E7 H26 E9 E10 E11 E14 E15 E16 E17 E27 E22 E23 E24 E25 VDDR1

MEMORY PLL - 1.8V

+1_8V_ATI_PVDD → L62 FERR-220-OHM 0402 → +1_8V_GPU_MEMPLL
C411 10uF 20% 6.3V CERM 805
C429 0.01uF 20% 16V CERM 402

AK21 LPVDD
AK11 TPVDD
A7 MPVDD

LVDS - 2.5V

+2_5V_GPU → L64 FERR-10-OHM-500MA SM (NO_STUFF)
L17 FERR-10-OHM-500MA SM → +2_5V_GPU_PNLIO (350mA)
C412 10uF 20% 6.3V CERM 805
C434 0.01uF 20% 16V CERM 402
C868 0.01uF 20% 16V CERM 402

AE16 LVDDR_18
AF16 LVDDR_18
AG16 LVDDR_25
AF17 LVDDR_25
AG12 TXVDDR0
AG13 TXVDDR1
AG14 TXVDDR2
AG15 TXVDDR3

LVDS/TMDS - 1.8V

+1_8V_GPU → L60 FERR-220-OHM 0402 → +1_8V_GPU_PNLIO (180mA)
C413 10uF 20% 6.3V CERM 805
C435 0.1uF 20% 10V CERM 402
C864 0.1uF 20% 10V CERM 402
C704 0.1uF 20% 10V CERM 402
C414 0.1uF 20% 10V CERM 402
C436 0.01uF 20% 16V CERM 402
C869 0.01uF 20% 16V CERM 402

GPU_CORE

AK30 PVSS
AF22 AVSSQ
AJ22 A2VSSQ
AE22 AVSSN0
AE23 AVSSN1
AE19 A2VSSN0
AE20 A2VSSN1
AG23 VSS1DI
AF19 VSS2DI
F20 VSSRH0
M6 VSSRH1

F5 G5 H5 J5 K5 L5 M5 N5 P5 R5 T5 U5 V5 W5 Y5 AA5 AB5 AC5 AD5 G26 K6 R6 Y6 AA6 F8 F9 F15 F16 F21 F22 H25 J25 J26 VDDR2

AF6 AE7 AF7 AE8 AF8 AE9 AF9 AF10 AD25 AE25 AE26 AF26 VDDR4 VDDR3

AJ21 LPVSS
AJ11 TPVSS
A6 MPVSS

AH16 LVSSR0
AG17 LVSSR1
AH17 LVSSR2
AF18 LVSSR3

AH12 DVOVMODE
AH13 TXVSSR1
AH14 TXVSSR2
AH15 TXVSSR3

OMIT U44 RAGE_MOBILITY M11-CSP64 64MB BGA (4 OF 6)

M11 SHUT DOWN POWER SEQUENCING

+2_5V_SLEEP → OMIT XW27 SM (+2_5V_SLEEP_NECK2) → DP7 BAS16TW SOT-363 → OMIT XW30 SM (+3V_SLEEP_NECK)
+1_8V_SLEEP → OMIT XW28 SM (+1_8V_SLEEP_NECK) → DP7 BAS16TW SOT-363
+1_5V_SLEEP → OMIT XW29 SM (+1_5V_SLEEP_NECK) → DP7 BAS16TW SOT-363

INT_TMDS

+2_5V_GPU → U54 MM1571J SOT-25A (CRITICAL) → +1_8V_ATI_TPVDD
INT_TMDS GPU_CORE_OK, CONT_NOISE, ATI_TPVDD_BYP
C879 1UF 10% 6.3V CERM 603
C880 0.01UF 10% 16V CERM 402
C881 10UF 20% 6.3V CERM 805
INT_TMDS L69 FERR-220-OHM 0402 → +1_8V_GPU_TP_PLL

MEMORY I/O

+GPU_MEM → L67 FERR-220-OHM 0805 (1200mA) → GPU_MEM_IO_FLT
C872 10uF 20% 6.3V CERM 805
C875 0.1uF 20% 10V CERM 402
C850 0.1uF 20% 10V CERM 402
C855 0.1uF 20% 10V CERM 402
C860 0.1uF 20% 10V CERM 402
C873 0.1uF 20% 10V CERM 402
C876 0.1uF 20% 10V CERM 402
C851 0.1uF 20% 10V CERM 402
C856 0.1uF 20% 10V CERM 402
C861 0.1uF 20% 10V CERM 402
C874 0.1uF 20% 10V CERM 402
C847 0.1uF 20% 10V CERM 402
C852 0.1uF 20% 10V CERM 402
C857 0.1uF 20% 10V CERM 402
C862 0.01uF 20% 16V CERM 402

3.3V IO SUPPLY

(Max Current varies, depends on usage)

+1_8V_GPU → L16 FERR-10-OHM-500MA SM (+1_8V_DVO_F)
C304 10uF 20% 6.3V CERM 805
C327 0.1uF 20% 10V CERM 402
C647 0.1uF 20% 10V CERM 402
INT_TMDS R268 0 5% 1/16W MF 603

+3V_GPU → L68 FERR-10-OHM-500MA SM → +3V_GPU_FLT
C722 10uF 20% 6.3V CERM 805
C848 0.1uF 20% 10V CERM 402
C853 0.1uF 20% 10V CERM 402
C858 0.1uF 20% 10V CERM 402
C863 0.1uF 20% 10V CERM 402
C725 0.1uF 20% 10V CERM 402
C849 0.1uF 20% 10V CERM 402
C854 0.1uF 20% 10V CERM 402
C859 0.1uF 20% 10V CERM 402

EXT_TMDS R255 0 5% 1/16W MF 402 → +1_8V_GPU
ATI_DVOVMODE → INT_TMDS R251 0 5% 1/16W MF 402

M11 POWER

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE: NONE	SHT 21 OF 45	

EXTERNAL VIDEO (DVI) INTERFACE

ANALOG FILTERING PLACE CLOSE TO CONNECTOR

FL2 CRITICAL LCFILTER SM-220MHZ — GPU_B → VGA_B
FL1 CRITICAL LCFILTER SM-220MHZ — GPU_G → VGA_G
FL3 CRITICAL LCFILTER SM-220MHZ — GPU_R → VGA_R
C685 3.3PF, C676 3.3PF, C684 3.3PF (50V CERM 402)

+3V_MAIN

VGA VSYNC BUFFERS

CRITICAL 74AHC1G32 SM U56: ATI_HSYNC → R718 33 1/16W MF 402 → VGA_HSYNC_BUF → VGA_HSYNC
CRITICAL 74AHC1G32 SM U57: ATI_VSYNC → R687 33 1/16W MF 402 → VGA_VSYNC_BUF → VGA_VSYNC

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)

+5V_SLEEP F1 0.5AMP-13.2V SM — +5V_DDC_SLEEP_UF
L23 400-OHM-EMI SM-1 — +5V_DDC_SLEEP
Isolation required for DVI power switch

D21 SM MBR0530: DDC_CLK_ISO
R655 4.7K 5% 1/16W MF 402
R661 4.7K 5% 1/16W MF 402

CRITICAL J14 QH1112 F-RT-TH 36-pin connector

TMDS_CONN_DN<0> TMDS_CONN_DP<0> TMDS_CONN_DN<1> TMDS_CONN_DP<1> TMDS_CONN_DN<2> TMDS_CONN_DP<2> TMDS_CONN_DN<3> TMDS_CONN_DP<3> TMDS_CONN_DN<4> TMDS_CONN_DP<4> TMDS_CONN_DN<5> TMDS_CONN_DP<5>
TMDS_CONN_CLKP TMDS_CONN_CLKN
DVI_DDC_CLK_UF (+5V_DDC_SLEEP) DVI_DDC_DATA_UF
VGA_VSYNC DVI_HPD_UF VGA_R VGA_G VGA_B VGA_HSYNC

C706 100pF 5% 50V CERM 402
C669 100pF 5% 50V CERM 402
C1 100pF 5% 50V CERM 402
C710 0.01UF 20% 50V CERM 603
R650 100 5% 1/16W MF 402
R649 100 5% 1/16W MF 402
R670 100 5% 1/16W MF 402
R706 0 5% 1/16W MF 402
R1 0 5% 1/16W MF 402 — PLACE NEAR C5A & C5B
PLACE NEAR 3, 11 & 19
CHGND1 CHGND5

3V LEVEL SHIFTERS

+3V_SLEEP
Q38 2N7002DW SOT-363: DVI_DDC_CLK → GPU_DVI_DDC_CLK
Q38 2N7002DW SOT-363: DVI_DDC_DATA → GPU_DVI_DDC_DATA
Q35 2N7002DW SOT-363: DVI_HPD → GPU_HPD
R662 10K 5% 1/16W MF 402
R671 10K 5% 1/16W MF 402
R694 100K 5% 1/16W MF 402

NOTE: Pulldown for DVI_HPD provided by DVI power switch interface
NOTE: DVI_HPD SHARES Q68 WITH ALS BECAUSE OF BOARD REAL ESTATE

DVI POWER SWITCH

Power key detect path when system is shutdown or asleep.. DDC CLK is isolated from NV17M DURING SHUTDOWN. WHEN power key on remote device is pressed, 5V will be driven into DDC CLK. since both rails will be low, TP0610 will turn on, driving SOFT_PWR_ON_L low. As both rails rise, TP0610 will turn off, as will remote device path to DDC CLK. Isolation will be disabled as well.

Q40 TP0610 SM: DVI_DDC_CLK_UP → DVI_DDC_CLK
R690 680 5% 1/16W MF 402: DVI_TURN_ON → DVI_TURN_ON_ILIM
R688 330 5% 1/16W MF 402: Pulldown prevents 3904 from turning on when DVI monitor has active self-powered DDC clock pullup.
R691 10K 5% 1/16W MF 402
Q42 2N3904 SM: DVI_TURN_ON_BASE → SOFT_PWR_ON_L

Power key detect path when system is running. 3.3V when power key +3V_SLEEP on remote device pressed. HPD will be driven to 5V. COMPARATOR ENABLED BY NV17MAP GPIO.

R680 68.1 1/16W MF 402
C696 0.1UF 10% 10V CERM 402
U46 LMC7211 SM CRITICAL: HPD_4V_REF, DVI_HPD_DIV → HPD_PWR_SW
R663 10K 1% 1/16W MF 402: DVI_HPD_UF
R686 10K 1% 1/16W MF 402
R681 100K 1% 1/16W MF 402
Q41 2N7002DW SOT-363: HPD_PWR_SW → HPD_ON
R703 330 5% 1/16W MF 402
R700 20K 5% 1/16W MF 402
Q44 2N3904 SM: HPD_BASE → HPD_ON_RC
+PBUS
Q45 TP0610: COMP_ENABLE → COMP_DISABLE
R696 100K 5% 1/16W MF 402
R704 100K 5% 1/16W MF 402
C703 47UF 20% 6.3V CERM 1210
R705 68K 5% 1/16W MF 402
NEED PULL-DOWN BECAUSE THIS SIGNAL IS TRISTATED INITIALLY
Q41 2N7002DW SOT-363: HPD_PWR_SNS_EN
R213 100K 1% 1/16W MF 402

TMDS FILTERING PLACE CLOSE TO CONNECTOR

CRITICAL L72 90-OHM-300MA 2012H: TMDS_DN<0> → TMDS_CONN_DN<0>
CRITICAL L73 90-OHM-300MA 2012H: TMDS_DP<0> → TMDS_CONN_DP<0>
CRITICAL L21 165-OHM SM: TMDS_CLKP → TMDS_CONN_CLKP; TMDS_CLKN → TMDS_CONN_CLKN
CRITICAL L74 90-OHM-300MA 2012H: TMDS_DN<1> → TMDS_CONN_DN<1>; TMDS_DP<1> → TMDS_CONN_DP<1>
CRITICAL L74 90-OHM-300MA 2012H: TMDS_DN<2> → TMDS_CONN_DN<2>; TMDS_DP<2> → TMDS_CONN_DP<2>

S-VIDEO/COMP OUT INTERFACE

Place GND shorts at graphics controller

XW12 SM: GPU_TV_GND1 → L26 FERR-10-OHM-500MA SM → TV_GND1
XW13 SM: GPU_TV_GND2 → L28 FERR-10-OHM-500MA SM → TV_GND2
L25 3.3UH 0603: GPU_Y → TV_C
L29 3.3UH 0603: GPU_C → TV_Y
L27 3.3UH 0603: GPU_COMP → TV_COMP
C712 0.01UF 20% 50V CERM 603
C702 560PF 10% 50V CERM 402
C707 560PF 10% 50V CERM 402
C718 560PF 10% 50V CERM 402
C724 560PF 10% 50V CERM 402
C714 560PF 10% 50V CERM 402
C713 560PF 10% 50V CERM 402
C717 0.01UF 20% 50V CERM 603
CRITICAL J15 MINIDIN RT-TH MH1177
CHGND1

Place GND shorts at graphics controller

LCD INTERFACE

LVDS INTERFACE

100K pull-ups are for no-panel case (development) Panel has 2K pull-ups

+3V_SLEEP
R342 100K 5% 1/16W MF 402: LVDS_DDC_CLK
R320 100K 5% 1/16W MF 402: LVDS_DDC_DATA
NO STUFF
C449 0.001uF 20% 50V CERM 402
C452 0.001uF 20% 50V CERM 402
C416 0.001uF 20% 50V CERM 402
CRITICAL J6 G-501973 F-RT-SM 34-pin connector
+3V_LCD (LVDS DDC POWER) NC
LVDS_L0N LVDS_L0P LVDS_L1N LVDS_L1P LVDS_L2N LVDS_L2P CLKLVDS_LN CLKLVDS_LP LVDS_U0N LVDS_U0P LVDS_U1N LVDS_U1P LVDS_U2N LVDS_U2P CLKLVDS_UN CLKLVDS_UP
C500 0.001uF 20% 50V CERM 402
CHGND4

LCD POWER SWITCHES

+3V_MAIN
R400 100K 5% 1/16W MF 402
C484 2200pF 5% 50V CERM 603
R391 100K 5% 1/16W MF 402: LCD_PWREN_L
LCD_DIGON_L
SI3443DV TSOP Q11
+3V_LCD_SW
L6 FERR-250-OHM SM
C474 0.001uF 20% 50V CERM 402
Q8 2N7002 SM: FP_PWR_EN
CHGND1 CHGND2 CHGND4

INVERTER INTERFACE

+PBUS
L33 FERR-1K-OHM-EMI SM: +12_8V_INV
+5V_MAIN
Q7 FDG6324L SC70-6
+5V_INV_UF_SW
L32 400-OHM-EMI SM-1: +5V_INV_SW
R317 100K 5% 1/16W MF 402: FP_PWR_EN
C440 10UF 20% 6.3V CERM 805
C746 0.001UF 20% 50V CERM 402
C749 0.001UF 20% 50V CERM 402
C739 0.001UF 20% 50V CERM 402
CRITICAL J7 SM-2MT
L31 400-OHM-EMI SM-1: BRIGHT_PWM
+3V_PMU
C552 0.1UF 20% 10V CERM 402
74LVC32 TSSOP U24: INV_ON_PWM → BRIGHT_PWM_UF
INVERTER EXPECTS ACTIVE HIGH SIGNAL

SHARES LOGIC WITH KB RESET SIGNALS (PG 28)
R724 0 5% 1/16W MF 402
C744 0.01uF 20% 50V CERM 603

VIDEO CONNECTORS

APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-6694 | REV. G
SCALE NONE | SHT 22 OF 45

MLB - ALS SENSOR

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
385-0044	385-0053		PD1	ALT FOR BS520EOF

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0856	353S0504	?	U40	ALT FOR SUPPLY PROBLEM

+3V_MAIN
C673 0.1UF 20% 10V CERM 402
CRITICAL
U40 MAX4236EUTT SOT23-6
MLB_ALS_OP_COMP
MLB_ALS_OP_IN
SHDN_L
MLB_ALS_OUT_FB
R619 1K 1% 1/16W MF 402
MLB_ALS_OUT 23
MLB_PHOTODIODE
R606 1K 1% 1/16W MF 402
CRITICAL
PD1 BS520EOF TH
R605 5.1M 5% 1/16W MF 402
C670 0.01UF 20% 16V CERM 402
R617 120K 5% 1/16W MF 402
R615 15K 1% 1/16W MF 402
R618 1K 1% 1/16W MF 402
C675 0.22UF 20% 6.3V CERM 402
GAIN_SETTING2
Q35 2N7002DW SOT-363
23 MLB_ALS_GAIN_SW

LMU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1194	1	IC,LMU,P84	U52	CRITICAL	?

+3V_MAIN
C663 0.1UF 20% 10V CERM 402
31 28 27 24 17 IO_RESET_L
R550 47 5% 1/16W MF 402
23 ST7_ICP_SEL_PD
U52 ST72264G2H1 256KX8 BGA
OMIT
ST7_RESET*
ST7_OSC1
ST7_OSC2
R568 0 5% 1/16W MF 402
OMIT
CRITICAL
Y4 8.000M 8X4.5MM-SM
C637 0.1UF 20% 10V CERM 402
C654 27PF 5% 50V CERM 402
C648 27PF 5% 50V CERM 402
ST7_XTAL_IN
LOAD CAPACITANCE = 16PF

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0091	1	XTAL,CER,LOW PROF,8.000MHZ,8X4.5MM,SMD	Y4	CRITICAL	?

U52 pin		
B5	TEST	
A2	RESET*	
C4	OSC1	XIN
B3	OSC2	XOUT
C6	PA3	PD
D4	PA2	PD
A6	ST7_SENSOR5_SCK	
A5	ST7_SENSOR5_SDA	
A2	SLEEP	
A1	ST7_PB6_PD	
B1	SUTRO_ALS_GAIN_SW	
B2	PB4_PD	
C3	PB3_PD	
D2	PB2_PD	
E1	ST7_KBD_LED_OUT	
F1	MLB_ALS_GAIN_SW	
F2	SUTRO_ALS_OUT	
E2	PMU_LID_CLOSED_L	
F3	(PMU_PWM)	PMU_SLEEP_LED
E3	MLB_ALS_OUT	
F4	ST7_SLEEP_LED_H	
D3	PC0_PD	
B4	VDD	
A4	VSS	
E4	ST7_SENSOR4_SCK_PD	
F5	INT_I2C_DATA0	
F6	ST7_SENSOR4_SDA_PD	
E6	INT_I2C_CLK0	

C655 0.1UF 20% 10V CERM 402
C636 0.1UF 20% 10V CERM 402

SLEEP LED

+5V_MAIN
R773 2.2K 5% 1/16W MF 402
R772 100 5% 1/16W MF 402
SLEEP_LED_L
SLEEP_LED_I
Q74 2N3906 SM
R777 4.7K 5% 1/16W MF 402
SLEEP_LED_SW_L1
SLEEP_LED_UF
23 ST7_SLEEP_LED_H
Q75 2N7002DW SOT-363
R776 10K 5% 1/16W MF 402
L52 400-OHM-EMI SM-1
NOTE: KEEP L39 CLOSE TO C781
SLEEP_ANODE 26
C828 470PF 10% 50V CERM 603
+3V_MAIN
RP52 10K 5% 1/16W SM1
+3V_PMU
R598 100K 5% 1/16W MF 402
Q75 2N7002DW SOT-363
PMU_SLEEP_LED_L 31

KEYBOARD PULLUPS

+3V_PMU
R771 100K 5% 1/16W MF 402
31 KBD_ID
RP43 10K 5% 1/32W 25V SM
31 KBD_X<6>
31 KBD_X<7>
31 KBD_X<8>
31 KBD_X<9>
31 KBD_X<2>
31 KBD_X<4>
40 31 KBD_X<3>
31 KBD_X<5>
RP42 10K 5% 1/32W 25V SM
40 31 KBD_FUNCTION_L
40 31 KBD_CONTROL_L
40 31 KBD_SHIFT_L
31 KBD_COMMAND_L
NC
40 31 KBD_OPTION_L
40 31 KBD_X<1>
40 31 KBD_X<0>

LMU PULL-DOWNS

RP27 10K 5% 1/16W SM1
23 PC0_PD
RP27 10K 5% 1/16W SM1
23 PB2_PD
RP27 10K 5% 1/16W SM1
23 PA2_PD
RP27 10K 5% 1/16W SM1
23 PA3_PD
RP53 10K 5% 1/16W SM1
23 PB4_PD
RP53 10K 5% 1/16W SM1
23 PB3_PD
RP52 10K 5% 1/16W SM1
23 ST7_SENSOR4_SDA_PD
RP52 10K 5% 1/16W SM1
23 ST7_SENSOR4_SCK_PD
RP53 10K 5% 1/16W SM1
23 ST7_PB6_PD
RP53 10K 5% 1/16W SM1
23 ST7_ICP_SEL_PD

USB Trackpad Connector

+5V_MAIN
+3V_PMU
R866 100K 1/16W 5% MF 1
3V_5V_OK_T
3V_5V_OK_G
R865 470K 5% 1/16W MF 402
Q34 2N7002 SM
C929 0.1UF 20% 10V CERM 402
SI3443DV TSOP Q70
R88 22 5% 1/16W MF 402
40 39 +3V_HALL_EFFECT
400-OHM-EMI L90 SM-1
+5V_TPAD
+5V_TPAD_FB
400-OHM-EMI L91 SM-1
39 +3V_MAIN
+3V_MAIN_CONN
3V_5V_OK 34 36
CRITICAL
J21 54550-1490 F-RT-SM
L49 400-OHM-EMI SM-1
31 23 PMU_LID_CLOSED_L
40 LID_CLOSED_L
14 USB_TPAD_N
14 USB_TPAD_P
39 23 KBDLED_RETURN
39 23 KBDLED_ANODE
40 26 24 14 13 INT_I2C_CLK1
40 26 24 14 13 INT_I2C_DATA1
THERM_L_OC_CONN
R850 0 5% 1/16W MF 402
26 ADT7467_THERM
L46 400-OHM-EMI SM-1
35 31 22 SOFT_PWR_ON_L
40 26 PWR_BUTTON_L
C14 0.001UF 10% 50V CERM 402
C814 0.001UF 10% 50V CERM 402
C815 0.001UF 10% 50V CERM 402
C816 0.001UF 10% 50V CERM 402
C914 0.001UF 10% 50V CERM 402

Keyboard LED Driver

39 20 +3V_SLEEP
NO STUFF
R222 10K 5% 1/16W MF 402
23 ST7_KBD_LED_OUT
R235 10K 5% 1/16W MF 402
L11 22UH 3.8X3.8X1.5MM
39 +5V_SLEEP
+5V_SLEEP_MM3120
U59 MM3120 LLP
VDD SW CNTRL VOUT NC FB THRML_PAD PGND AGND NC
C79 1UF 10% 6.3V CERM 603
C80 0.22UF 10% 25V CERM 1210
R202 25.5 1% 1/8W MF-LF 805
KBDLED_ANODE 23 39
KBDLED_RETURN 23 39

+3V_MAIN
NO STUFF
R901 10K 5% 1/16W MF 402
23 ST7_SENSOR5_SDA
R902 10K 5% 1/16W MF 402
+3V_MAIN
NO STUFF
R899 10K 5% 1/16W MF 402
23 ST7_SENSOR5_SCK
R900 10K 5% 1/16W MF 402

LMU/BOOTBANGER/SPIDEY

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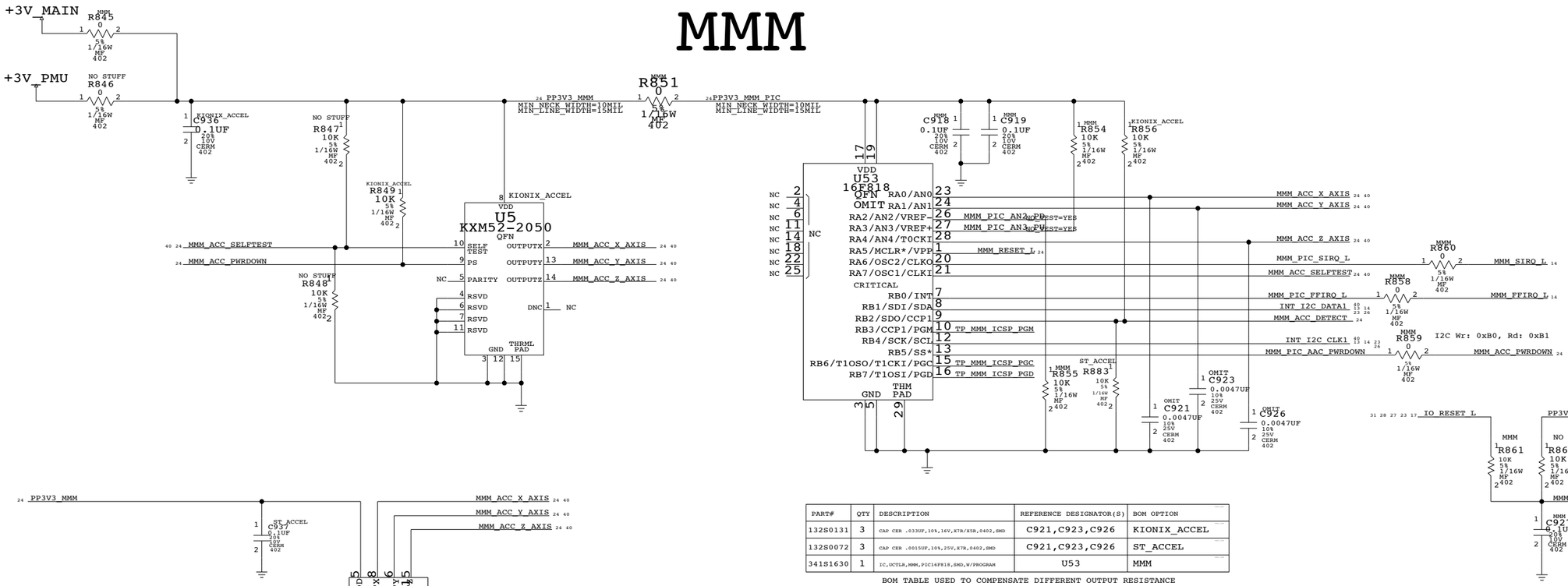
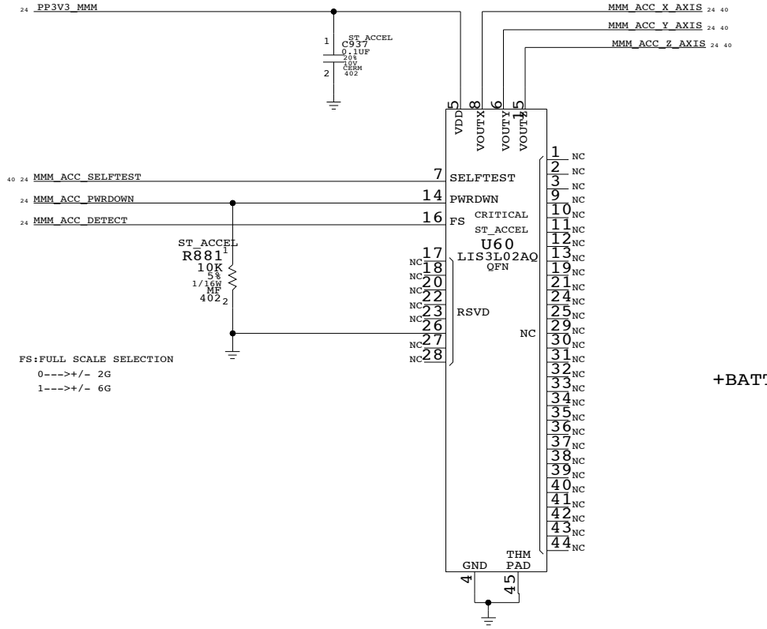
MMM

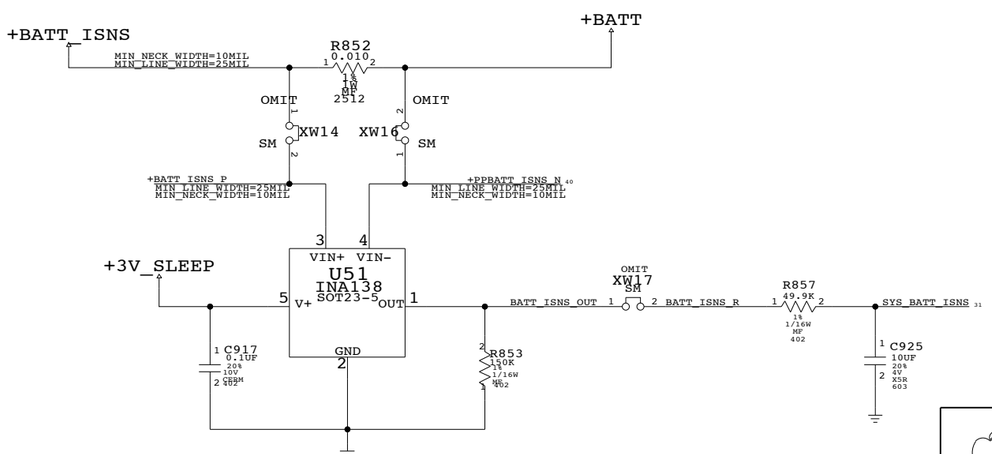




PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0131	3	CAP CER .033UF,10%,16V,X7R/X5R,0402,SMD	C921,C923,C926	KIONIX_ACCEL
132S0072	3	CAP CER .0015UF,10%,25V,X7R,0402,SMD	C921,C923,C926	ST_ACCEL
341S1630	1	IC,UCTLR,MMM,PIC16F818,SMD,W/PROGRAM	U53	MMM

BOM TABLE USED TO COMPENSATE DIFFERENT OUTPUT RESISTANCE

BATTERY CURRENT SENSE



MMM, BATTERY CURRENT SENSE

APPLE COMPUTER INC.

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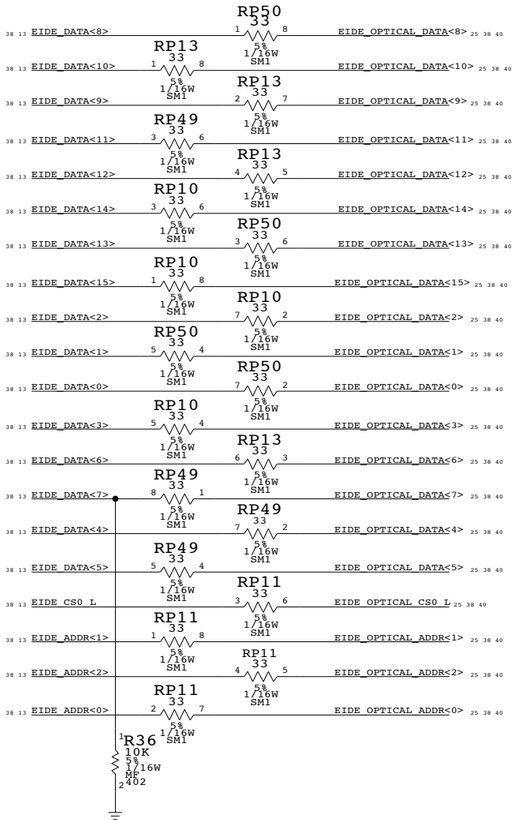
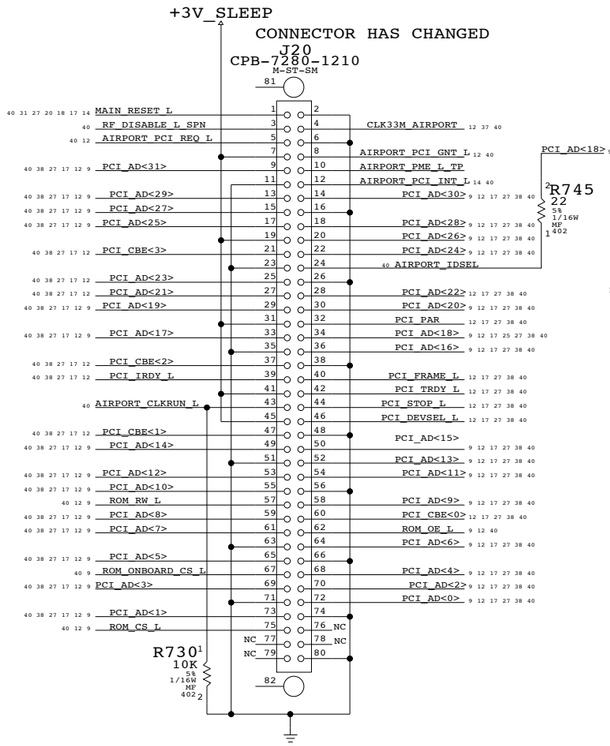
EIDE SERIES TERMINATION

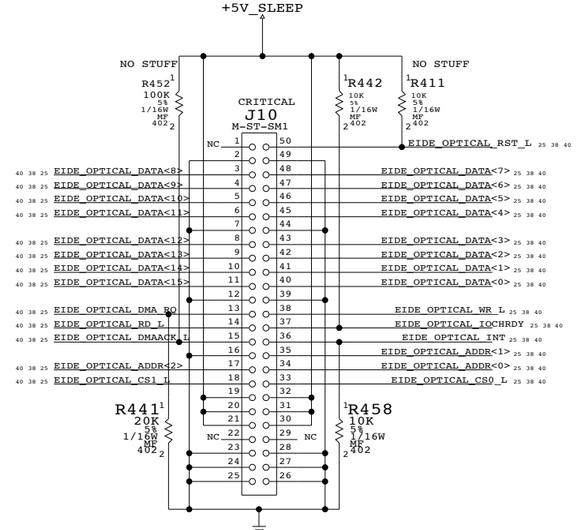
PLACE TERMINATORS NEAR INTREPID



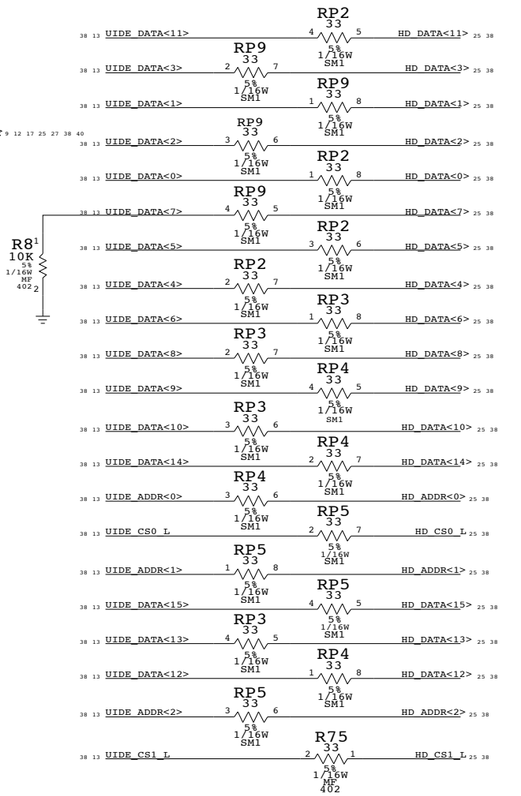
WIRELESS INTERFACE



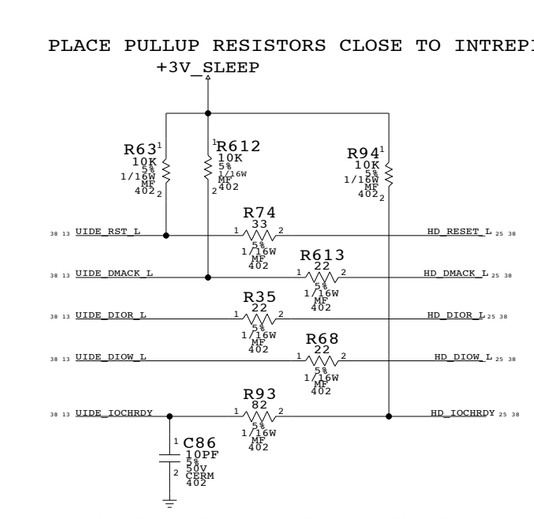
OPTICAL DRIVE INTERFACE (EIDE)



PLACE SERIES R CLOSE TO INTERPID

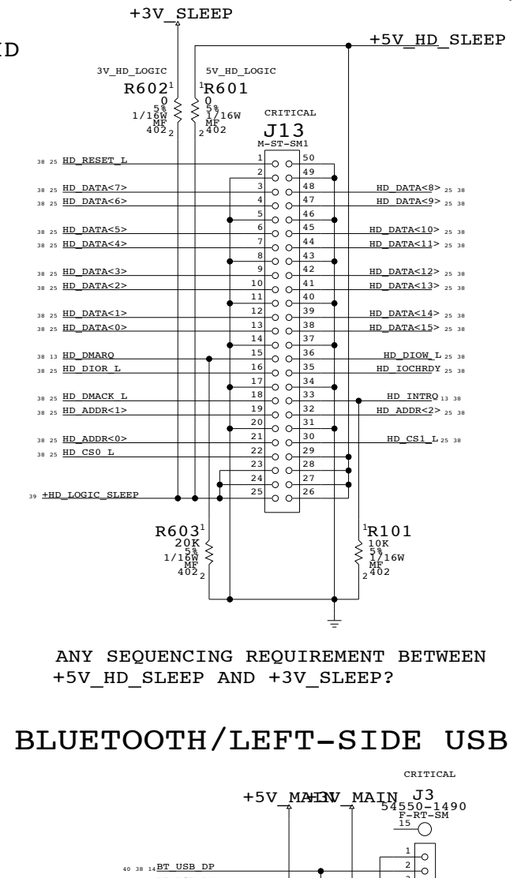


PLACE PULLUP RESISTORS CLOSE TO INTREPID



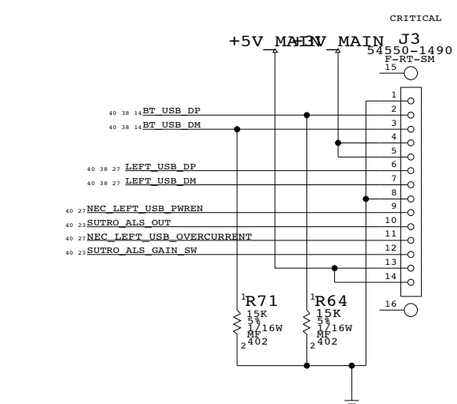
IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V

HARD DRIVE INTERFACE (UATA100)



ANY SEQUENCING REQUIREMENT BETWEEN +5V_HD_SLEEP AND +3V_SLEEP?

BLUETOOTH/LEFT-SIDE USB



INTERNAL I/O CONNECTORS

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SOUND BOARD (SOUSAPHONE)

AUDIO - CRYSTAL SND - INTREPID

Sound Board Connector

Place shorts at 3.3V and 5V regulators

+5V_MAIN

XW9 SM — This is an internal board short. PLACE XW9 CLOSE TO 5V SWITCHER (U27)

+5V_MAIN_AUDIO

CRITICAL J12 QT500406-L111 M-ST-SM1

XW10 SM +3V_SLEEP — This is an internal board short

+3V_SLEEP_AUDIO

XW11 SM — This is an internal board short

SND_AGND

(SLEEP_LED_GND)

SLEEP_ANODE

VER_1 516S0154

R534 0 5% 1/16W MF 402 — SOUND_SPDIF_GPO0 — SPDIF_GPO0

R581 0 5% 1/16W MF 402 — AUDIO_MCLK_SEL — AUDIO_EXT_MCLK_SEL

R552 0 5% 1/16W MF 402 — AUDIO_LO_SPDIF_PLUG — AUDIO_LO_OPTICAL_PLUG_L

R582 0 5% 1/16W MF 402 — AUDIO_LI_SPDIF_PLUG — AUDIO_LI_OPTICAL_PLUG_L

R918 0 5% 1/16W MF 402 — +5V_MAIN_AUDIO_0

R917 NO STUFF 0 5% 1/16W MF 402

SPDIF_GPO0 — AUDIO_LO_DET_L

+3V_SLEEP_AUDIO — AUDIO_LO_OPTICAL_PLUG_L

AUDIO_EXT_MCLK_SEL — AUDIO_LI_DET_L

AUDIO_LO_MUTE_L — AUDIO_LI_OPTICAL_PLUG_L

AUDIO_SPKR_MUTE_F

I2S0_MCLK_F

I2S0_BITCLK_F — I2S0_RESET_L_F

I2S0_SYNC_F — I2S1_RESET_L_F

I2S0_SB_TO_DEV_DTO_F

I2S0_DEV_TO_SB_DTI_F — INT_I2C_DATA2

INT_I2C_CLK2

I2S1_BITCLK_F

I2S1_SYNC_F

I2S1_DEV_TO_SB_DTI_F

L77 FERR-220-OHM 0402 — SND_SYNC — I2S0_SYNC_F — C895 NO STUFF 0.01UF 20% 16V CERM 402

L80 FERR-220-OHM 0402 — SND_CLKOUT — I2S0_MCLK_F — C899 NO STUFF 0.01UF 20% 16V CERM 402

L81 FERR-220-OHM 0402 — INT_AUDIO_TO_SND — I2S0_DEV_TO_SB_DTI_F — C896 NO STUFF 0.01UF 20% 16V CERM 402

L82 FERR-220-OHM 0402 — SND_TO_AUDIO — I2S0_SB_TO_DEV_DTO_F — C897 NO STUFF 0.01UF 20% 16V CERM 402

L76 FERR-220-OHM 0402 — SND_AMP_MUTE_INV — AUDIO_SPKR_MUTE_F — C898 NO STUFF 0.01UF 20% 16V CERM 402

L78 FERR-220-OHM 0402 — SND_HW_RESET_L — I2S0_RESET_L_F — C900 NO STUFF 0.01UF 20% 16V CERM 402

L79 FERR-220-OHM 0402 — SND_SCLK — I2S0_BITCLK_F — C901 NO STUFF 0.01UF 20% 16V CERM 402

L84 FERR-220-OHM 0402 — MOD_SYNC — I2S1_SYNC_F — C81 NO STUFF 0.01UF 20% 16V CERM 402

L48 FERR-220-OHM 0402 — MOD_BITCLK — I2S1_BITCLK_F — C82 NO STUFF 0.01UF 20% 16V CERM 402

L85 FERR-220-OHM 0402 — INT_MOD_DTI — I2S1_DEV_TO_SB_DTI_F — C87 NO STUFF 0.01UF 20% 16V CERM 402

L86 FERR-220-OHM 0402 — AUDIO_SPDIF_RESET_C — I2S1_RESET_L_F — C88 NO STUFF 0.01UF 20% 16V CERM 402

CAPS FOR EMI EXPERIMENTATION ONLY

KEEP STUFFING RESISTORS CLOSE TO ADT7467 CONTROLLER

R719 0 5% 1/16W MF 402 — CPU_M_DP — THERM1_DP

R725 0 5% 1/16W MF 402 — CPU_M_DM — THERM1_DM

R713 0 5% 1/16W MF 402 — SUPPLY_M_DP — THERM2_DP

R716 0 5% 1/16W MF 402 — SUPPLY_M_DM — THERM2_DM

KEEP STUFFING RESISTORS CLOSE TO ADT7467 CONTROLLER

PLACE CAPS AS CLOSE TO THERMISTORS AS POSSIBLE

PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY

PLACE CLOSE TO CPU

MAIN1

SUPPLY_M_DP — C681 0.001UF 20% 50V CERM 402 — Q66 2N3904 SM — SUPPLY_M_DM

MAIN2

CPU_M_DP — C668 0.001UF 20% 50V CERM 402 — Q39 2N3904 SM — CPU_M_DM

PLACE UNDERNEATH UPPER RAM

ALTERNATE1

THERM1_A_DP — C678 NO STUFF 0.001UF 20% 50V CERM 402 — Q47 NO STUFF 2N3904 SM — THERM1_A_DM

PLACE CLOSE TO BATTERY CHARGER/VCORE

ALTERNATE2

THERM2_A_DP — C651 NO STUFF 0.001UF 20% 50V CERM 402 — Q62 NO STUFF 2N3904 SM — THERM2_A_DM

R628 NO STUFF 0 5% 1/16W MF 402 — CPU_THERM_DP — THERM1_DP

R620 NO STUFF 0 5% 1/16W MF 402 — CPU_THERM_DM1 — THERM1_DM

R723 NO STUFF 0 5% 1/16W MF 402 — THERM1_A_DP — THERM1_DM

R726 NO STUFF 0 5% 1/16W MF 402 — THERM1_A_DM — THERM2_DM

R710 NO STUFF 0 5% 1/16W MF 402 — THERM2_A_DP — THERM2_DP

R717 NO STUFF 0 5% 1/16W MF 402 — THERM2_A_DM — THERM2_DM

MODEM

SUPPORTS BOTH THE LAST DASH AND Q52 SOFT MODEM

+5V_MAIN

R874 100K 5% 1/16W MF 402 — SND_AMP_MUTE

R224 NO STUFF 10K 5% 1/16W MF 402

SND_AMP_MUTE_INV — Q26 2N7002DW SOT-363 — SND_AMP_MUTE_L

R915 0 5% 1/16W MF 402

Q33 NO STUFF 2N7002 SM — AMP_CONTROL — R875 100K 5% 1/16W MF 402

SND_AMP_MUTE — Q26 2N7002DW SOT-363 — INT_PU_RESET_L

+5V_MAIN

C767 10UF 20% 6.3V CERM 805 — NO STUFF C513 0.1UF 20% 10V CERM 402

+3V_MAIN

R405 10K 5% 1/16W MF 402 — CRITICAL J8 QT510166-L010 F-ST-SM1

NO STUFF C478 0.1UF 20% 10V CERM 402 — C469 10UF 20% 6.3V CERM 805

MOD_DTO — MOD_SYNC

MOD_CLKOUT — INT_MOD_DTI

COMM_RESET_L — MOD_BITCLK

COMM_SHUTDOWN — MODEM_USB_DM

INT_I2C_CLK2 — MODEM_USB_DP

INT_I2C_DATA2 — COMM_RING_DET_L

+5V_MAIN

SERIAL_DEBUG CRITICAL J16 M-ST-5087 SM

COMM_TXD_L — COMM_DTR_L

COMM_TRXC — COMM_RTS_L

COMM_GPIO_L — COMM_RXD

SERIAL DEBUG INTERFACE

DEBUG POWER BUTTON

NO STUFF R527 0 5% 1/16W MF 603 — PWR_BUTTON_L

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S0608	1	IC,ADT7460,FAN,CTLR,16P,QSOP	U3	ADT7460

FAN CONTROLLER

+3V_MAIN

R872 10K 5% 1/16W MF 402 — R689 100K 5% 1/16W MF 402 — AUDIO_LO_MUTE_L

Q31 2N7002DW SOT-363 — SND_HP_MUTE

Q31 2N7002DW SOT-363 — SND_HP_MUTE_L

AMP_CONTROL

+3V_MAIN

R814 10 5% 1/16W MF 402 — ADT7467_VCC — C904 1UF 20% 10V CERM 603

+3V_SLEEP

ADT7460 R692 10K 5% 1/16W MF 402 — R293 10K 5% 1/16W MF 402

ADT7460 R695 10K 5% 1/16W MF 402 — R295 10K 5% 1/16W MF 402

R42 10K 5% 1/16W MF 402

C711 0.1UF 20% 10V CERM 402

U3 ADT7467 QSOP

ADT7467_VCORE_MON — VCCP

INT_I2C_DATA1 — SDA

INT_I2C_CLK1 — SCL

THERM1_DP — D1+

THERM1_DM — D1-

THERM2_DP — D2+

THERM2_DM — D2-

ADT7467 PWM1 XTO TACH1 PWM2/ SMBALERT# TACH2 PWM3 TACH3 TACH4 THERM#/ SMBALERT#/GPIO GND

FAN1_PWM_L — FAN1_TACH — FAN2_PWM_L — FAN2_TACH

ADT7467_ADR_EN_L

ADT7460_TACH3_TP

ADT7467_THERM

C688 NO STUFF 0.001UF 20% 50V CERM 402

C690 NO STUFF 0.001UF 20% 50V CERM 402

C846 NO STUFF 0.001UF 20% 50V CERM 402

C905 NO STUFF 0.001UF 20% 50V CERM 402

THERM ISOLATION

+3V_MAIN

R813 100K 5% 1/16W MF 402 — R811 100K 5% 1/16W MF 402 — R812 100K 5% 1/16W MF 402

+3V_PMU_AVCC — THERM_L_OC

THERM_INV — Q87 2N7002DW SOT-363

Q87 2N7002DW SOT-363 — C903 0.1UF 20% 10V CERM 402 — ADT7467_THERM

DEBUG JUMPERS

NO STUFF R537 0 5% 1/16W MF 603 — PMU_NMI_BUTTON_L

NO STUFF R553 0 5% 1/16W MF 603 — PMU_RESET_BUTTON_L

FAN INTERFACE

LEFT FAN (CPU)

+5V_SLEEP

R679 10K 5% 1/16W MF 402 — NO STUFF R910 10K 5% 1/16W MF 402 — R908 0 5% 1/16W MF 603 — CRITICAL J4 SM-2MT

+FAN1_PWR — FAN1_TACH — FAN1_PWM

ADT7467 R878 0 5% 1/16W MF 402

Q78 ADT7460 2N7002DW SOT-363

C134 4.7UF 20% 10V CERM 1206 PLACE CLOSE TO CONNECTOR

FAN1_PWM_L — FAN2_PWM

RIGHT FAN (GPU)

+5V_SLEEP

R623 10K 5% 1/16W MF 402 — NO STUFF R911 10K 5% 1/16W MF 402 — R909 0 5% 1/16W MF 603 — CRITICAL J2 SM-2MT

ADT7467 R679 0 5% 1/16W MF 402

+FAN2_PWR — FAN2_TACH — FAN2_PWM

Q78 ADT7460 2N7002DW SOT-363

C135 4.7UF 20% 10V CERM 1206 PLACE CLOSE TO CONNECTOR

FAN2_PWM

FAN/MODEM/SOUND/SLEEP LED/DEBUG

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0087	1	XTAL,CER,LW PROF,30.0000MHZ,8X4.5MM,SMD	Y5	CRITICAL	NEC_USB

Y7 LOAD CAPACITANCE IS 16PF

Low/Full/High Speed (External)

Low/Full/High Speed (External)

SERR_L AND PERR_L
HAS DEDICATED PULL-UP
FOR BOTH CBUS AND USB2

Series Rpaks required to facilitate NAND-tree testing

Tie to GND at ball N11

NEED PULL-UP RESISTORS IN CASE USB 1.0 IS USED FOR PORT POWER

PLACE NEAR J3

SUTRO CONNECTOR

PLACE NEAR J12

BUBBA CONNECTOR

INTREPID USB CONSTRAINTS

USB_DAM	USB_DA	5 MIL SPACING	14
USB_DAP	USB_DA	5 MIL SPACING	14
USB_DCM	USB_DC	5 MIL SPACING	14
USB_DCP	USB_DC	5 MIL SPACING	14
USB_D1M	USB_D1	5 MIL SPACING	14 27
USB_D1P	USB_D1	5 MIL SPACING	14 27
USB_D2M	USB_D2	5 MIL SPACING	
USB_D2P	USB_D2	5 MIL SPACING	

USB 2.0

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Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0079	338S0223	?	U49	ALT FOR 88E1111-BDIE

PLACE ALL SERIES RES CLOSE TO PHY

PLACES PHY IN "COMA" MODE WHEN ASLEEP ON BATTERY (SAVES POWER)

PLACE CAPS (IN ORDER) ON PINS 1, 6, 10/15, 57/62, 67/71, 85

PLACE CAPS (IN ORDER) ON PINS 5, 21/26, 48/52, 66/72, 88, 96

PLACE CAPS (IN ORDER) ON PINS 32/35, 36/40, 45 & 78

PLACE CAPS AT TRANSFORMER PINS 1, 4, 7 & 10

PLACE CLOSE TO ETHERNET CONNECTOR

PLACE RESISTORS CLOSE TO PHY

SEE CONFIG TABLES (BELOW)

VOUT = 0.8V*(1+R2EQV/R1)
R2EQV = R2A||R2B

Y3'S LOAD CAPACITANCE IS 20PF

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0086	1	XTAL,CER,25MHZ,.005%,20PF,8X4.5MM,SMD	Y3	CRITICAL	?

CONFIG DEFINITIONS

PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS

PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

MARVELL 88E1111 10/100/1000 ETHERNET

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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0011	197S0052	?	G1	SIWARD ALT FOR FW OSC

DSX STRAP OPTIONS

0 -> BILINGUAL PORT

1 -> A-ONLY PORT

PLACE NEAR PHY

PLACE NEAR PHY

SPEC SAID TO USE 10K

CAPACITOR IN CONJUCTION WITH INTERNAL PULLUP PROVIDES RESET PULSE WHEN PHY FIRST RECEIVES POWER

VOUT = 1.22*(1+R2/R1)+ IADJ*R2

IADJ = 30NA AT 25C

PWR CLASS = 100

(MAY PROVIDE POWER, OR MAY REQUIRE UP TO 3W)

(PC0 IS MSB, PC2 IS LSB)

1MA(MAX) BUS HOLDER EACH

FIREWIRE

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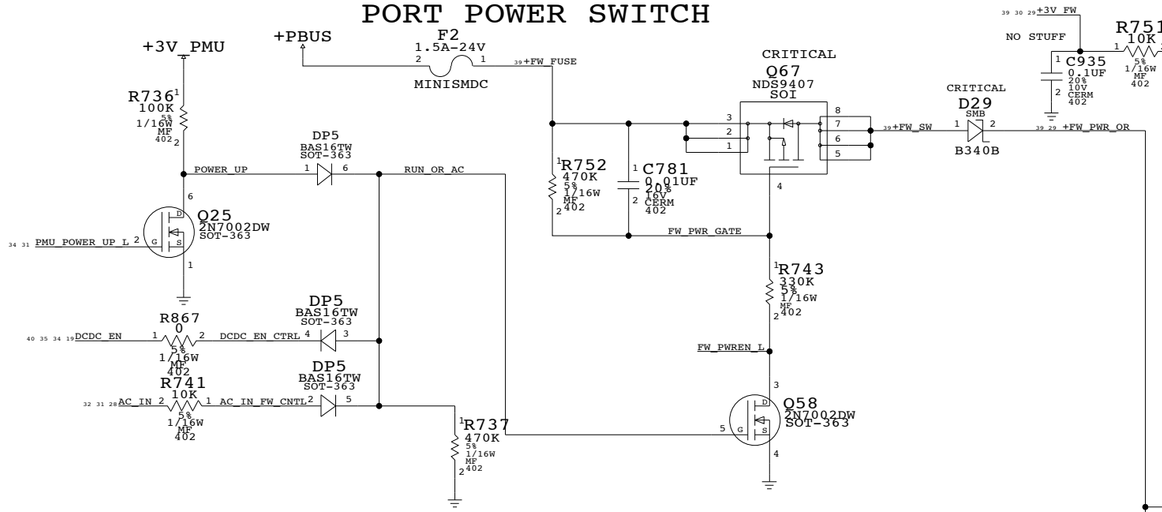
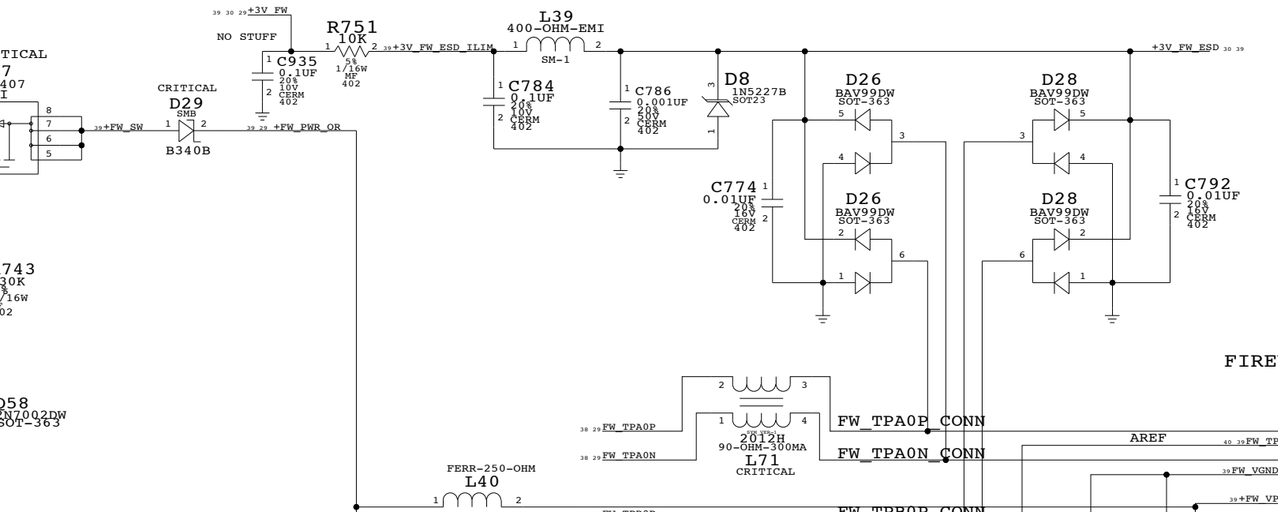
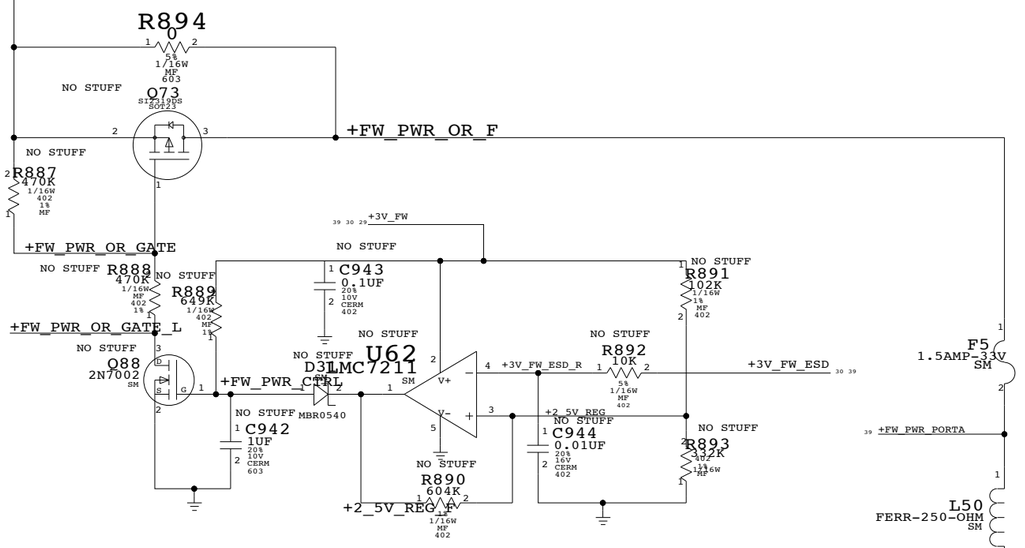
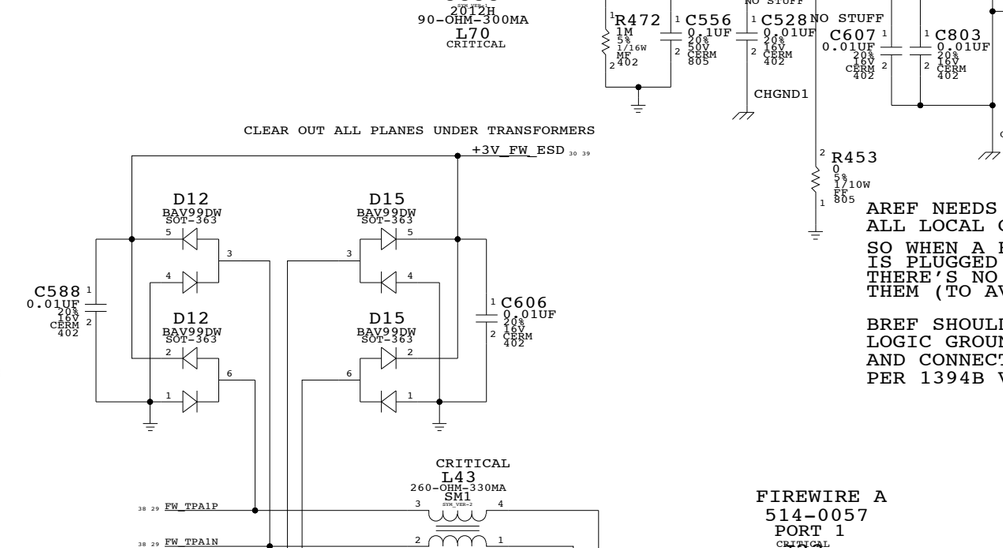
PORT POWER SWITCH









AREF NEEDS TO BE ISOLATED FROM ALL LOCAL GROUNDS PER 1394B SPEC

SO WHEN A BILINGUAL DEVICE IS PLUGGED TO BETA-ONLY DEVICE, THERE'S NO DC PATH BETWEEN THEM (TO AVOID GROUND OFFSET ISSUE)

BREF SHOULD BE HARD CONNECTED TO LOGIC GROUND FOR SPEED SIGNALING AND CONNECTION DETECTION CURRENTS PER 1394B V1.33

ENABLES PORT POWER WHEN MACHINE IS RUNNING, SHUTDOEN OR WHEN ASLEEP ON AC

STATE	PMU_POWER_UP_L	POWER_UP	DCDC_EN	AC_IN	STUFF R867	NO STUFF R867
SHUTDOWN (AC)	1	0	0	1	OFF	ON
SLEEP (AC)	1	0	1	1	ON	ON
RUN (AC)	0	1	1	1	ON	ON
SHUTDOWN (BATT)	1	0	0	0	OFF	OFF
SLEEP (BATT)	1	0	1	0	OFF (PULL-DOWN RESISTOR)	OFF (PULL-DOWN RESISTOR)
RUN (BATT)	0	1	1	0	ON	ON
	2.99V	+3V_PMU	+4_6V_BU	+3V_PMU		

FIREWIRE PORTS

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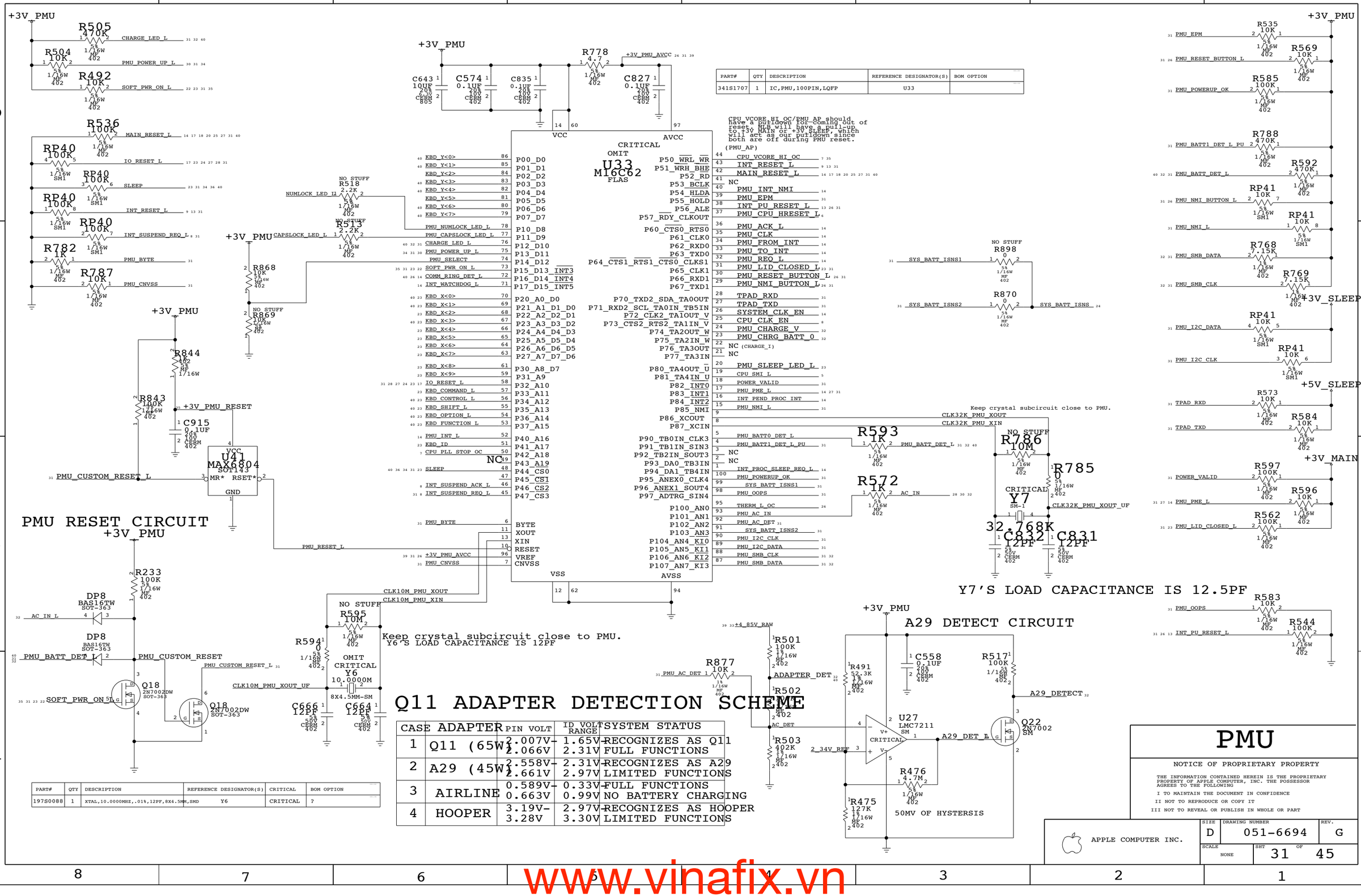
SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE: NONE	SHT 30 OF 45	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1707	1	IC,PMU,100PIN,LQFP	U33	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0088	1	XTAL,10.0000MHZ,.01%,12PF,8X4.5MM,SMD	Y6	CRITICAL	?

Q11 ADAPTER DETECTION SCHEME

CASE	ADAPTER	PIN VOLT	ID VOLT RANGE	SYSTEM STATUS
1	Q11 (65W)	2.007V-2.066V	1.65V-2.31V	RECOGNIZES AS Q11 FULL FUNCTIONS
2	A29 (45W)	2.558V-2.661V	2.31V-2.97V	RECOGNIZES AS A29 LIMITED FUNCTIONS
3	AIRLINE	0.589V-0.663V	0.33V-0.99V	FULL FUNCTIONS NO BATTERY CHARGING
4	HOOPER	3.19V-3.28V	2.97V-3.30V	RECOGNIZES AS HOOPER LIMITED FUNCTIONS

DC POWER INPUT

(POWER JACK, ETC. ON SEPARATE BOARD)
CRITICAL

J18
87438-0833
M-RT-SM

CHARGE_LED_L
+ADAPTER
ADAPTER_DET

NO STUFF
C757 0.1UF 20% 50V CERM 805
PLACE CLOSE TO DC INPUT

R396 20K 1% 1/16W MF 402
R395 102K 1% 1/16W MF 402
R364 102K 1% 1/16W MF 402
R375 10K 1% 1/16W MF 402
R365 57.6K 1% 1/16W MF 402

+3V_PMU

C468 0.01UF 20% 16V CERM 402
R363 10K 5% 1/16W MF 402
R394 1M 5% 1/16W MF 402
R383 470K 5% 1/16W MF 402
R374 470K 5% 1/16W MF 402

U15 LMC7211 SM
CRITICAL
1V20_REF
AC_DIV
AC_IN
AC_IN_L

Q10 2N7002DW SOT-363
Q10 2N7002DW SOT-363
Q10 2N7002DW SOT-363

AC_ENABLE_L

GREATER THAN 13.5V DETECT

DC INRUSH LIMITER

Q13 SI4435DY SOI
Q16 SI4435DY SOI
GATE
AC_ENABLE_GATE
BCKFD_PROT_GATE
BCKFD_PROT_EN_L

R414 330K 1% 1/16W MF 402
C458 0.1UF 20% 50V CERM 805
R474 47K 5% 1/16W MF 402
C592 0.01UF 20% 16V CERM 603
R499 68K 5% 1/16W MF 402

Q21 2N7002DW SOT-363

+ADAPTER_SW
+ADAPTER_SENSE

C572 0.010UF 20% 50V CERM 603

PLACE U23 NEXT TO R460

U23 SENSE VOLTAGE DROP ACROSS R460

U23 MAX4172 TSSOP
RS+ RS-
CRITICAL
PG
NC1 NC2 OUT GND
MAX4172_OUT

+24V_PBUS

R454 2.21K 1% 1/16W MF 603
C883 0.1UF 10% 50V X7R 603-1

R460 0.025 1% 1W MF 2512
R488 4.7 5% 1/16W MF 402
R498 4.7 5% 1/16W MF 402
1772_CSSP
1772_CSSN

IF A29 ADAPTER USED,
ADJUST CURRENT SETTING

1MSEC INTEGRATION TIME

R742 1K 1% 1/16W MF 402
C771 0.1UF 20% 10V CERM 402
IAC_RC_COMP

+3V_PMU

C772 0.1UF 20% 10V CERM 402
R747 42.2K 1% 1/16W MF 603
U50 LMC7111 SOT23-5
CRITICAL
IAC_FB

PLACE R358 CLOSE TO LTC1625
ROUTE LTC1625_ITH CAREFULLY

LTC1625_ITH
DP4 BAS16TW SOT-363
R358 150 1% 1/16W MF 402
1_1625_COMP
ADAPTER_I_REG

R466 10K 1% 1/16W MF 402
CURRENT_THRESHOLD

R738 42.2K 1% 1/16W MF 603
R734 82.5K 1% 1/16W MF 603
A29_CURRENT_ADJ

Q20 2N7002DW SOT-363
A29_DETECT_G

+3V_PMU

R739 57.1K 1% 1/16W MF 603
IF ADAPTER IS OVER 18V,
ADJUST CURRENT SETTING

R748 100K 5% 1/16W MF 402
OVER_18V_ADJ

Q20 2N7002DW SOT-363
AC_GTR_18V
C775 1UF 20% 16V CERM 603

Q65 2N7002DW SOT-363
1772_ACOK_L

BATTERY SWITCH-OVER CIRCUIT

+BATT

F4 5AMP-125V SM-2
F3 5AMP-125V SM-2

+24V_PBUS
+PBUS
+BATT_24V_FUSE
+BATT_14V_FUSE

CRITICAL
Q24 SI4435DY SOI
GATE
CRITICAL
Q76 SUD45P03 TO-252

R490 47K 5% 1/16W MF 402
R746 47K 5% 1/16W MF 402
BATT_14V_GATE
BATT_24V_GATE

R512 10K 5% 1/16W MF 402
R744 10K 5% 1/16W MF 402
DP4 BAS16TW SOT-363
BATT_24PBUS_EN
BATT_14PBUS_EN

AC_IN_L
DP4 BAS16TW SOT-363
R489 158K 1% 1/16W MF 402
AC_IN_L_RC
C593 10UF 20% 6.3V CERM 805

Q21 2N7002DW SOT-363

WHEN AC IS IN, P-CHANNEL FETS ARE QUICKLY (DIODE) TURNED OFF
WHEN AC IS NOT PLUGGED, P-CHANNEL FETS ARE ON
RC TIME IS 480K*10UF @ +3V_PMU

SWITCHER VOLTAGE CONTROL

PMU SELECTS BETWEEN TWO VOLTAGES

+3V_PMU

R567 27.4K 1% 1/16W MF 402
R558 10K 1% 1/16W MF 402
R548 10K 1% 1/16W MF 402
R560 4.12K 1% 1/16W MF 402
R565 48.7K 1% 1/16W MF 402
R566 1K 1% 1/16W MF 402
R542 1K 1% 1/16W MF 402

BATTV_HIGH
BATT_LOW_L
BATTV_LOW
PMU_CHARGE_V

R561 100K 5% 1/16W MF 402
R580 5.23K 1% 1/16W MF 402

Q27 2N7002DW SOT-363
Q27 2N7002DW SOT-363
Q29 2N7002DW SOT-363
Q29 2N7002DW SOT-363

SWITCHER CURRENT CONTROL

CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V
CHARGE THROTTLED BY LOW BATTERY VOLTAGE

R754 100K 1% 1/16W MF 402
D9 1N914 SOT23
R755 12.7K 1% 1/16W MF 402
C600 1UF 20% 50V CERM 1210

OD OUTPUT LOW - WHEN AC GREATER THAN 18V

U31 MAX1772 QSOP
CRITICAL

1772_DCIN	1	CSSP	
	27	CSSN	
1772_ACIN	11	ACIN	
1772_ACOK_L	12	ACOK	
(+3V_PMU)	13	RFIN	
1772_VCTL	15	VCTL	
1772_ICTL	14	ICTL	
1772_ICHG	10	ICHG	
1772_IINP	28	IINP	
1772_CCV	7	CCV	
1772_CCI	6	CCI	
1772_CCS	5	CCS	
		REF = 4.096V	
	4	REF	
	3	CLS	
	8	GND	
	9		
1772_CELLS	16	CELLS	
	2	LDO	
1772_DLOV	22	DLOV	
1772_BST	25	BST	
1772_DHI	24	DHI	
1772_LX	23	LX	
1772_DLO	21	DLO	
	20	PGND	(GND)
1772_CSIP	19	CSIP	
1772_CSIN	18	CSIN	
	17	BATT	

C578 0.47UF 10% 50V CERM 1206
C579 0.470UF 10% 50V CERM 1206
1772_LDO
R571 33 1% 1/8W PF 1206
D10 1N914 SOT23
1772_BST_ESR
R549 100K 5% 1/16W MF 402
C624 0.1UF 20% 25V CERM 603
R774 4.7 5% 1/16W MF 603
C608 0.1UF 20% 50V CERM 805

+24V_PBUS

C547 2.2UF 10% 50V CERM 1812
C562 2.2UF 10% 50V CERM 1812
C563 2.2UF 10% 50V CERM 1812
C557 2.2UF 10% 50V CERM 1812
C564 2.2UF 10% 50V CERM 1812

CRITICAL
Q63 IRF7805 SM

CRITICAL
L42 10UH SM1
R763 0.05 1% 1W MF 2512
+BATT_RSNS
+BATT_24V_FUSE

C619 4.7UF 20% 25V CERM 1206
C632 4.7UF 20% 25V CERM 1206
C617 4.7UF 20% 25V CERM 1206
C824 33UF 20% 25V ELEC SM1

CRITICAL
D30 SM MBRS140T3
CRITICAL
Q64 IRF7811W SO-8

R543 1 5% 1/16W MF 603
R511 1 5% 1/16W MF 603
C631 4.7UF 20% 25V CERM 1206
C633 4.7UF 20% 25V CERM 1206
C618 4.7UF 20% 25V CERM 1206

NO STUFF
C906 0.0022UF 10% 50V CERM 402
XW19 SM

R526 1K 1% 1/16W MF 402
C622 0.01UF 20% 16V CERM 402
C616 0.01UF 20% 16V CERM 402
C652 1UF 20% 10V CERM 603
C817 0.1UF 20% 25V CERM 603
C802 0.1UF 20% 25V CERM 603

1772_CCV_RC
1772_REF
1772_CLS
1772_GND

R497 1K 1% 1/16W MF 402
C621 0.1UF 20% 10V CERM 402
C630 1UF 20% 10V CERM 603
R487 10K 1% 1/16W MF 402
R473 4.12K 1% 1/16W MF 402
R559 100K 5% 1/16W MF 402

+3V_PMU

C615 0.1UF 20% 10V CERM 402
R588 100K 1% 1/16W MF 402
R579 499K 1% 1/16W MF 402
U38 LMC7211 SM
CRITICAL
BATT_LOW
BATT_DIV
1V65_REF
R599 100K 1% 1/16W MF 402
R570 100K 1% 1/16W MF 402
C658 0.047uF 10% 50V CERM 402

R749 6.34K 1% 1/16W MF 402
A29_CLS_ADJ
A29_DETECT

+BATT_VSNS

BATTERY CONNECTOR
CRITICAL
J25
87438-0833
M-RT-SM

+BATT_POS
(BATT_IN_PD)
BATT_CLK
BATT_DATA
PMU_BATT_DET_L
BATT_NEG

L9 FERR-EMI-100-OHM SM
L53 FERR-50-OHM SM
L10 FERR-EMI-100-OHM SM
PMU_SMB_CLK
L8 FERR-EMI-100-OHM SM
PMU_SMB_DATA
L12 FERR-50-OHM SM

+BATT_ISNS

$V_{BATT} = CELLS \times (4.096 + (0.4096 \times V_{VCTL} / V_{REFIN}))$

For 4.15V cells, VCTL = 0.123 REFIN
For 4.20V cells, VCTL = 0.245 REFIN

$I_{CHG} = (0.2048/R_{62}) * ICTL (V_{REFIN} / V)$

BATTERY CHARGER

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SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE: NONE	SHT 32 OF 45	

12.8V PBUS SUPPLY

+5V_MAIN
1625_EXTVCC
1625_ENABLE_L
1625_ENABLE
Q14 FDG6324L SC70-6 (CRITICAL)
R426 470K 5% 1/16W MF 402
C495 0.1UF 20% 10V CERM 402
CONNECT LTC1625 TK PIN AT TOP-SIDE FET
KEEP VIN/TK LOOP SHORT
+3V_PMU
R443 102K 1% 1/16W MF 402
R433 10K 1% 1/16W MF 402
C537 0.1UF 20% 10V CERM 402
U21 LMC7211 SM (CRITICAL)
R432 1M 1% 1/16W MF 402
1V20_REF
1625_DIV
WHEN +24V_PBUS IS BELOW ~13.44V, 1625 IS SHUT-OFF
R412 1 5% 1/16W MF 603
D4 1N914 SOT23
1625_VIN
1625_RUNSS
1625_COMP
1625_FCB
COMP_RC
C510 0.1UF 20% 10V CERM 805
R379 4.99K 1% 1/16W MF 402
C485 4700PF 5% 25V CERM 603
C462 470PF 10% 50V CERM 603
C463 4700PF 5% 25V CERM 603
R392 0 5% 1/16W MF 402
NO STUFF R402 0 5% 1/16W MF 402
U18 LTC1625 SSOP (CRITICAL)
VIN SSOP BG
TK SYNC VOSENSE
RUN/SS INTVCC
ITH
FCB BOOST
VPROG SW
SGND PGND
1625_INTVCC
1625_TG
1625_BST_ESR
1625_BST
1625_BG
1625_VSW
1625_SGND
1625_VFB
D3 MBR0540 SM
R401 2.2 1% 1/16W MF 603
C509 0.22UF 20% 25V CERM 805
Q59 IRF7805 SM (CRITICAL)
Q60 IRF7811W SO-8 (CRITICAL)
C461 4.7UF 20% 10V CERM 1206
C554 0.0047UF 10% 25V CERM 402
NO STUFF
OMIT XW4 SM
D27 MBRS140T3 SM
L37 8.0UH-6.8A SM1 (CRITICAL)
C535 4.7UF 20% 25V CERM 1206
C536 4.7UF 20% 25V CERM 1206
R359 158K 1% 1/16W MF 402
R360 16.2K 1% 1/16W MF 402
+PBUS
+24V_PBUS
PBUS HOLD-UP CAPS
C644 2.2UF 10% 50V CERM 1812
C787 2.2UF 10% 50V CERM 1812
C585 2.2UF 10% 50V CERM 1812
C626 2.2UF 10% 50V CERM 1812
C801 2.2UF 10% 50V CERM 1812
C569 2.2UF 10% 50V CERM 1812
C604 2.2UF 10% 50V CERM 1812
C750 22UF 20% 35V ELEC SM-1
C799 22UF 20% 35V ELEC SM-1
C820 22UF 20% 35V ELEC SM-1
C821 22UF 20% 35V ELEC SM-1
C819 22UF 20% 35V ELEC SM-1
C765 33UF 20% 25V ELEC SM1
C769 33UF 20% 25V ELEC SM1
C794 33UF 20% 25V ELEC SM1
C822 33UF 20% 25V ELEC SM1
C793 33UF 20% 25V ELEC SM1
C758 33UF 20% 25V ELEC SM1

BACKUP BATTERY / USB CONNECTOR

CRITICAL
J11 54550-1490 F-RT-SM
+5V_MAIN
NEC_RIGHT_USB_OVERCURRENT 27 40
RIGHT_USB_DM 27 38 40
RIGHT_USB_DP 27 38 40
NEC_RIGHT_USB_PWREN 27 40
NC
NC
+24V_PBUS_CONN
R880 0 5% 1/4W FF 1210
BACKUP_BATT
+PBUS IS BOTH AN INPUT AND OUTPUT TO BUBBA
24V IS AN OUTPUT FROM BUBBA
R871 0 5% 1/4W FF 1210 SUPERCAP

BOOTSTRAP SYSTEM FROM ADAPTER OR BATTERY
+PBUS
+BATT
R508 390 5% 1/4W FF 1210
+ADAPTER
+ADAPTER_ILIM
D17 MBR0540 SM
D18 1N914 SOT23
D19 MBR0540 SM
+ADAPTER_OR_BATT

PMU SUPPLY

U30 LP2951 SOI PLUS5VTAP (CRITICAL)
IN OUT
SENSE ERROR
SHUT FDBK
GND
NC
+4_85V_RAW
IF SUPERCAP BOM OPTION IS CHOSEN:
OUTPUT AT U30.1 IS 5.65V
INPUT AT U25.8 IS 5.4V
C625 0.1UF 20% 50V CERM 805
C599 0.1UF 20% 10V CERM 402
R521 294K 1% 1/16W MF 402
C613 470PF 10% 50V CERM 603
R541 100K 1% 1/16W MF 402
FB_4_85V_BU
+4_85V_ESR
C568 2.2UF 20% 10V CERM 805
BACKUP_BATT
+5V_MAIN
D7 MBR0520LT SM
D11 MBR0520LT SM
R483 1 5% 1/16W MF 603
(+4_6V_BU)
+4_6V_BU
U25 LP2951 SOI-3.3V VTAP (CRITICAL)
3V_PMU_VTAP
3V_PMU_SENSE
+3V_PMU
C553 0.1UF 20% 10V CERM 402
R468 1 5% 1/16W MF 603
+3V_PMU_ESR
C584 10UF 20% 6.3V CERM 805

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S3575	1	RES,MF,1/16W/357K OHM,1%,0402,SMD	R521	?	SUPERCAP

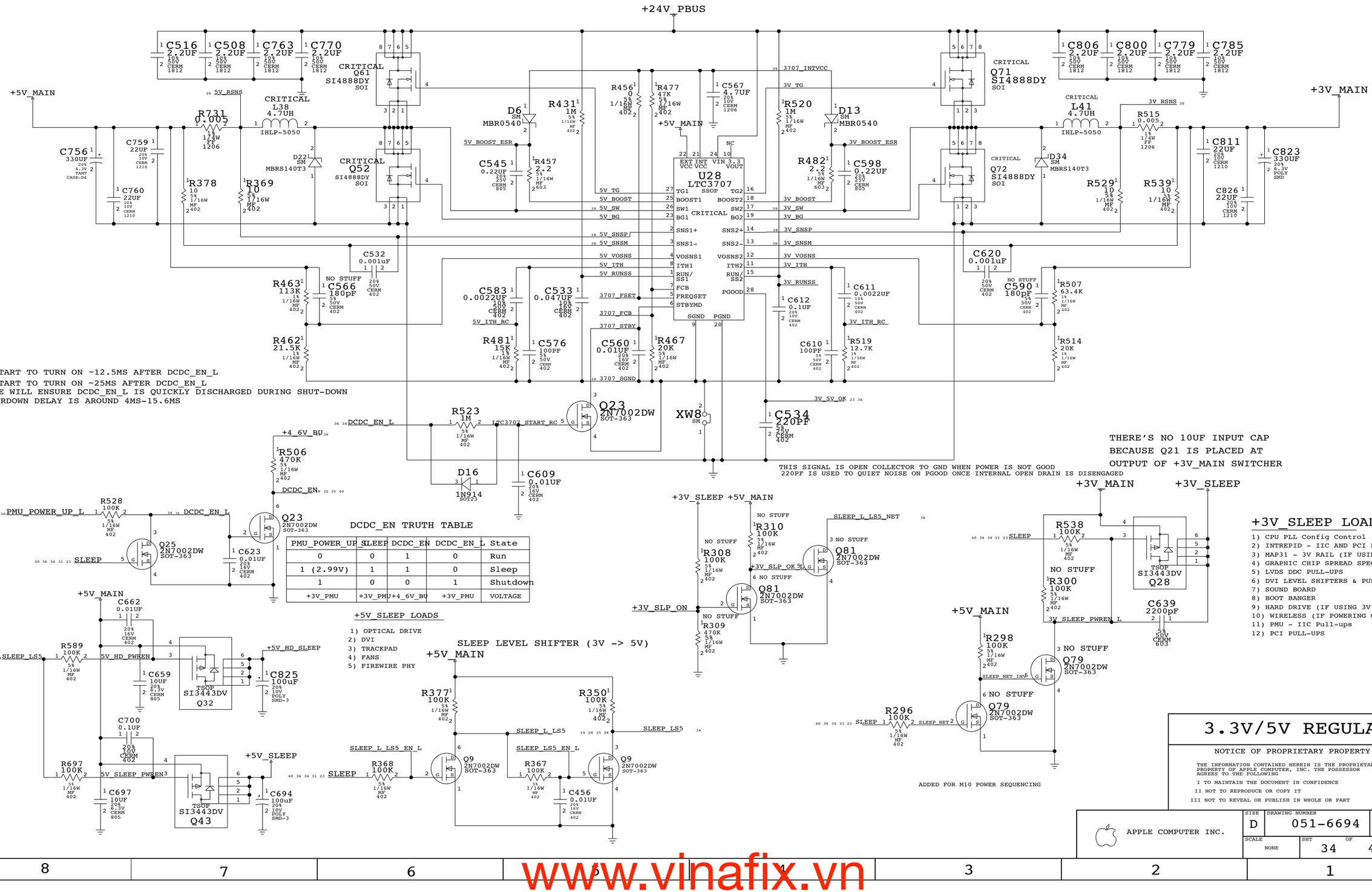
12.8V REGULATOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G

SCALE: NONE
SHT 33 OF 45

3.3V/5V MAIN SUPPLY



3.3V/5V REGULATOR

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SCALE: NONE	SHT 34 OF 45	

VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage
(approx. 7ms delay)

+5V_MAIN

R408 100K 1% 1/16W MF 402
R398 100K 1% 1/16W MF 402
R356 100K 1% 1/16W MF 402
DP2 BAS16TW SOT-363

MAXBUS_SLEEP
CPU_VCORE_PWR_SEQ
CPU_VCORE_SEQ_L
CPU_VCORE_SEQ

R267 10K 5% 1/16W MF 402
Q12 2N3904 SM
Q17 2N3904 SM

DP2 BAS16TW SOT-363
SLEEP_L
DP2 BAS16TW SOT-363
DCDC_EN

R318 0 5% 1/16W MF 402
CPU_VCORE_HI_OC

1.67GHZ (WITHOUT VCORE OFFSET) 1.300V -> 0.975V

+3V_MAIN

R297 470K 5% 1/16W MF 402 NO STUFF
R314 470K 5% 1/16W MF 402 NO STUFF
R328 0 5% 1/16W MF 402 NO STUFF
R324 0 5% 1/16W MF 402 NO STUFF
R876 470K 5% 1/16W MF 402 NO STUFF
R304 470K 5% 1/16W MF 402
R329 470K 5% 1/16W MF 402
R325 0 5% 1/16W MF 402
R322 10K 5% 1/16W MF 402 NO STUFF

VCORE_SLOW<1>
VCORE_SLOW<2>
VCORE_SLOW<3>
VCORE_SLOW<4>

VCC NO STUFF U11 PI3B3257 QSOP
A1 B1 A2 B2 A3 B3 A4 B4 SEL OE GND Y1 Y2 Y3 Y4 CRITICAL

VCORE_FAST<1> VCORE_FAST<2> VCORE_FAST<3> VCORE_FAST<4>
VCORE_MUX_SEL
VCORE_MUX_EN

C439 0.1UF 20% 10V CERM 402 NO STUFF

VCORE_VID<1> VCORE_VID<2> VCORE_VID<3> VCORE_VID<4>

R288 0 5% 1/16W MF 402 NO_4XVCORE
R289 0 5% 1/16W MF 402 NO_4XVCORE
R290 0 5% 1/16W MF 402 NO_4XVCORE
R292 0 5% 1/16W MF 402 NO_4XVCORE

SEL = 0; Y1=A1
SEL = 1; Y1=B1

R303 0 5% 1/16W MF 402 NO STUFF <D4>
R313 470K 5% 1/16W MF 402 NO STUFF <D3>
R327 470K 5% 1/16W MF 402 NO STUFF <D2>
R323 470K 5% 1/16W MF 402 NO STUFF <D1>
R301 470K 5% 1/16W MF 402 <D4>
R305 0 5% 1/16W MF 402 NO STUFF <D3>
R330 470K 5% 1/16W MF 402 NO STUFF <D2>
R326 0 5% 1/16W MF 402 NO STUFF <D1>
R302 1K 5% 1/16W MF 402 NO STUFF

Keep trace fat (40-100 mils) and short!!

+PBUS

C427 C431 C443 C430 8.2UF 20% 16V TANT CASE-D CRITICAL
C432 C441 C444 C445 8.2UF 20% 16V TANT CASE-D CRITICAL

CPU_VCORE_SLEEP

C2 C689 C5 C699 C234 10UF 20% 6.3V CERM 805
C682 C674 C274 C7 C680 10UF 20% 6.3V CERM 805
C693 C13 C116 C6 C695 10UF 20% 6.3V CERM 805
C679 C285 C4 C3 C687 10UF 20% 6.3V CERM 805

+5V_MAIN

R349 20 5% 1/16W MF 402
VCORE_VCC
PLACE C423 CLOSE TO PINS 15 & 13
C498 1UF 20% 10V CERM 603
D2 SM MBR0530
VCORE_BOOST

R407 0 5% 1/16W MF 402
C507 1UF 20% 10V CERM 603
R397 27.4K 1% 1/16W MF 402

U20 MAX1717 QSOP
VCC VDD SKP/SDN FBS ILIM GNDS A/B REF TON CC D0 D1 D2 D3 D4 V+ BST DH LX DL GND FB TIME VGATE

VCORE_SHDN_L
(VCORE_SNS)
VCORE_ILIM
(VCORE_GNDSNS)
MAX1717_AB_SEL
VCORE_REF
VCORE_TON
VCORE_CC
MIN_LINE_WIDTH=10

VCORE_VPLUS
VCORE_BST
VCORE_DH
VCORE_LX
VCORE_DL
VCORE_GND
VCORE_FB
VCORE_TIME
VCORE_VGATE

R429 2.2 5% 1/16W MF 603
C518 0.1UF 20% 10V CERM 603
C455 0.0047uF 10% 25V CERM 402 NO STUFF
C768 0.0047uF 20% 25V CERM 402
C521 0.001UF 20% 50V CERM 402
R434 390K 5% 1/16W MF 402
R415 100 5% 1/16W MF 402
XW5 SM
XW7 SM

Q50 SI7860DP SO-8-PWRPK CRITICAL
Q49 SI7860DP SO-8-PWRPK CRITICAL
Q54 IRF7832 SO-8 CRITICAL
Q55 IRF7832 SO-8 CRITICAL
Q53 IRF7832 SO-8 CRITICAL

Keep trace fat and short!!

OMIT CRITICAL L36 1.2UH-18.3A SM1
R331 0.001 1% 1W MF 2512 CRITICAL
R732 2.2 5% 1/4W MF 1210 NO STUFF CPU_VCORE_SNUB
D25 BS40C SM CRITICAL
C764 0.0022UF 10% 50V CERM 603 NO STUFF CPU_VCORE_SNUB

XW15 SM CPU_VCORE_SLEEP_F

Keep trace fat and short!!

C728 330UF 20% 2.5V-ESR9V POLY CASE-D2E CRITICAL
C734 330UF 20% 2.5V-ESR9V POLY CASE-D2E CRITICAL
C733 330UF 20% 2.5V-ESR9V POLY CASE-D2E CRITICAL
C732 330UF 20% 2.5V-ESR9V POLY CASE-D2E CRITICAL
C885 330UF 20% 2.5V-ESR9V POLY CASE-D2E CRITICAL
C731 330UF 20% 2.5V-ESR9V POLY CASE-D2E CRITICAL
C730 330UF 20% 2.5V-ESR9V POLY CASE-D2E CRITICAL
C729 330UF 20% 2.5V-ESR9V POLY CASE-D2E CRITICAL
C884 330UF 20% 2.5V-ESR9V POLY CASE-D2E CRITICAL

R384 0 5% 1/16W MF 402 NO STUFF +3V_MAIN
R366 0 5% 1/16W MF 402
INT_GPIO1_PU
R337 470K 5% 1/16W MF 402 NO STUFF <D0>

MAX1717 VID CAN TAKE 3.3V TO 5.5V INPUTS

R336 470K 5% 1/16W MF 402
C529 0.01UF 10% 25V CERM 402
R448 66.5K 1% 1/16W MF 402
R385 12.7K 1% 1/16W MF 402
C459 1UF 10% 10V CERM 603
C512 220PF 5% 25V CERM 402

VCORE_GNDA

+5V_MAIN
R805 100K 5% 1/16W MF 402
VCORE_OFFSET_SW
VCORE_SEL_OFF_L
VCORE_SEL_ON
R806 0 5% 1/16W MF 402
R807 0 5% 1/16W MF 402
MAX1717_AB_SEL
AB_SEL_LOW
R808 100K 5% 1/16W MF 402 NO STUFF
Q86 2N7002DW SOT-363

VCORE128
R809 6.04K 1% 1/16W MF 402
R376 162K 1% 1/16W MF 603 R2
R321 2K 1% 1/16W MF 402 R1
VCORE_OFFSET
VCORE_GNDDIV

Connect MAX1717 GND pin 13 to GND at bottom-side FET

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V WITH A 0.85 SCALE FACTOR, HENCE VOFFSET = 1.7V * (R1/(R1+R2)) AND VCORE = VDAC + VOFFSET.

NOTE: R310 (R2) NO STUFFED FOR NO OFFSET CASE

ROUTE AS DIFFERENTIAL PAIR

PLACE THIS SHORT AT PIN OF 1000uF CAP CLOSEST TO CPU
XW3 SM
VCORE_GNDSNS
VCORE_SNS

1.67GHZ (WITH VCORE OFFSET) 1.320V -> 0.990V
(CPU SPEC: 1.280V -> 0.980V)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S4023	1	RES,4.02KOHM,1%,1/16W,0402,LF	R321	VCORE13
114S2433	1	RES,2.43KOHM,1%,1/16W,0402,LF	R809	VCORE13

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S0242	1	IND,PWR,1.0UH,20,20.5A,SMD	L36	CRITICAL	

OUTPUT VOLTAGE

V_{DAC} D4=0	V_{DAC} D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	UNO CPU	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	A/B_ = Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1

If all pull-ups are >=100K and all pull-downs are <=1K, VB = V .

FMAX CONNECTOR

R315 2.05K 1% 1/16W MF 402 NO STUFF
R312 100 1% 1/16W MF 402 NO STUFF
VCORE_GNDDIV
VCORE_GNDSNS
VCORE_GNDDIV_TEST
VCORE_GNDSNS_TEST
+3V_PMU_RESET
SOFT_PWR_ON_L
NC (RFU)

J5 M-ST-SM-52465-1217 CRITICAL NO STUFF
VCORE_VID<0> VCORE_VID<1> VCORE_VID<2> VCORE_VID<3> VCORE_VID<4>

VCORE SUPPLY

APPLE COMPUTER INC.
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SCALE NONE | SHT 35 OF 45

1.5V/2.5V SWITCHER

+1_5V_SLEEP LOADS

1) AGP I/O IF USING D3COLD
2) MAXBUS I7O - IF 1.5V INTERFACE

+1_5V_MAIN LOADS

1) INTREPID CORE
2) AGP I/O IF USING D3HOT

THERE'S 100K PULL-UP ON PG 31 ALREADY

+2_5V_MAIN LOADS

1) MAP31 - FBCORE/FBIO IF USING D3HOT
2) GIGABIT ETHERNET - AVDDL
3) DDR SODIMMS - CORE/IO
4) DDR MUXES
5) CLOCK SLEWING I/O
6) PCI1510 CORE

+2_5V_SLEEP LOADS

1) FBCORE/FBIO IF USING D3COLD
2) INTREPID MEMORY I/O

DIODE PROVIDE PROVIDE QUICK SHUT-DOWN POWER DOWN DELAY 1.5MS TO 3.5MS

CHANGE R424 BACK TO 10K, 1%, AND STUFF 5.11K FOR 1.5V OPERATION
CONNECTING 1_5V_FB TO GND, FORCES 1.8V OUTPUT

1.8V SWITCHER

+1_8V_MAIN LOADS

1) INTREPID PLLS

+1_8V_SLEEP LOADS

1) MPC7450 - MAXBUS I/O - IF 1.8V INTERFACE
2) CPU JTAG & MaxBus Pull-ups
3) CPU PLL Config Straps
4) OPTIONAL VIDEO MEMORY (M10 PRO ONLY)

1.5V/1.8V/2.5V SUPPLIES

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE: NONE	SHT 36 OF 45	

DIGITAL SIGNALS

GROUP	SIG_NAME		MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
MAXBUS	CPU_AACK_L				250.0000	10 MIL SPACING			5 8
	CPU_ADDR<0..31>		5		250			83 MHZ	5 8
	CPU_ARTRY_L				250.0000	10 MIL SPACING			5 8
	CPU_BG_L				250.0000	10 MIL SPACING			5 8
	CPU_BR_L				250.0000	10 MIL SPACING			5 8
	CPU_CI_L		5		250.0000				5 8
	CPU_DATA<0..31>		5		250			83 MHZ	6 8
	CPU_DATA<32..63>		5		250			83 MHZ	6 8
	CPU_DBG_L		5		250.0000	10 MIL SPACING			5 8
	CPU_DTI<0..2>		5		250				5 8
	CPU_DRDY_L_UF					10 MIL SPACING			
	CPU_DRDY_L				250.0000	10 MIL SPACING			5 8
	CPU_GBL_L		5		250.0000				5 8
	CPU_HIT_L				250.0000	10 MIL SPACING			5 8
	CPU_QACK_L		5		250.0000	10 MIL SPACING			5 8
	CPU_QREQ_L				250.0000	10 MIL SPACING			5 8
	CPU_TA_L				250.0000	10 MIL SPACING			5 8
	CPU_TBST_L		5		250.0000	10 MIL SPACING			5 8
	CPU_TEA_L				250.0000				5 8
	CPU_TS_L				250.0000	10 MIL SPACING			5 8
	CPU_TSIZ<0..2>		5		250				5 8
	CPU_TT<0..4>		5		250				5 8
	CPU_WT_L		5		250.0000				5 8
GROUP 0	MEM_DATA<7..0>		4		200			167 MHZ	9 10
	RAM_DATA_A<7..0>		4		200			167 MHZ	10 11
	RAM_DATA_B<7..0>		4		200			167 MHZ	10 11
	MEM_DQS<0>	TOTAL LENGTH CONTROLLED BY SPREADSHEET			200				9 10
	RAM_DQS_A<0>		4		200				10 11
	RAM_DQS_B<0>		4		200				10 11
	MEM_DQM<0>		4		200				9 10
	RAM_DQM_A<0>		4		200				10 11
	RAM_DQM_B<0>		4		200				10 11
GROUP 1	MEM_DATA<15..8>		4		200			167 MHZ	9 10
	RAM_DATA_A<15..8>		4		200			167 MHZ	10 11
	RAM_DATA_B<15..8>		4		200			167 MHZ	10 11
	MEM_DQS<1>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200				9 10
	RAM_DQS_A<1>		4		200				10 11
	RAM_DQS_B<1>		4		200				10 11
	MEM_DQM<1>				200				9 10
	RAM_DQM_A<1>		4		200				10 11
	RAM_DQM_B<1>		4		200				10 11
GROUP 2/3	MEM_DATA<31..16>		4		200			167 MHZ	9 10
	RAM_DATA_A<31..16>		4		200			167 MHZ	10 11
	RAM_DATA_B<31..16>		4		200			167 MHZ	10 11
	MEM_DQS<3..2>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200			167 MHZ	9 10
DDR RAM	RAM_DQS_A<3..2>		4		200			167 MHZ	10 11
	RAM_DQS_B<3..2>		4		200			167 MHZ	10 11
	MEM_DQM<3..2>		4		200			167 MHZ	9 10
	RAM_DQM_A<3..2>		4		200			167 MHZ	10 11
	RAM_DQM_B<3..2>		4		200			167 MHZ	10 11
GROUP 4/5	MEM_DATA<47..32>		4		200			167 MHZ	9 10
	RAM_DATA_A<47..32>		4		200			167 MHZ	10 11
	RAM_DATA_B<47..32>		4		200			167 MHZ	10 11
	MEM_DQS<5..4>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200			167 MHZ	9 10
	RAM_DQS_A<5..4>		4		200			167 MHZ	10 11
	RAM_DQS_B<5..4>		4		200			167 MHZ	10 11
	MEM_DQM<5..4>		4		200			167 MHZ	9 10
	RAM_DQM_A<5..4>		4		200			167 MHZ	10 11
	RAM_DQM_B<5..4>		4		200			167 MHZ	10 11
GROUP 6	MEM_DATA<55..48>		4		200			167 MHZ	9 10
	RAM_DATA_A<55..48>		4		200			167 MHZ	10 11
	RAM_DATA_B<55..48>		4		200			167 MHZ	10 11
	MEM_DQS<6>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200				9 10
	RAM_DQS_A<6>				200				10 11
	RAM_DQS_B<6>		4		200				10 11
	MEM_DQM<6>				200				9 10
	RAM_DQM_A<6>		4		200				10 11
	RAM_DQM_B<6>		4		200				10 11
GROUP 7	MEM_DATA<63..56>		4		200			167 MHZ	9 10
	RAM_DATA_A<63..56>		4		200			167 MHZ	10 11
	RAM_DATA_B<63..56>		4		200			167 MHZ	10 11
	MEM_DQS<7>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200				9 10
	RAM_DQS_A<7>				200				10 11
	RAM_DQS_B<7>				200				10 11
	MEM_DQM<7>		4		200				9 10
	RAM_DQM_A<7>		4		200				10 11
	RAM_DQM_B<7>		4		200				10 11
ADDR	MEM_ADDR<12..0>		4					83 MHZ	9
	RAM_ADDR<12..0>		6		200				9 11
	MEM_BA<1..0>		4						9
	RAM_BA<1..0>		6		200				9 11
CONTROL	MEM_CS_L<3..0>		4						9
	RAM_CS_L<3..0>		6		200				9 11
	MEM_CKE<3..0>		4						9
	RAM_CKE<3..0>		6		200				9 11
	MEM_RAS_L		4						9
	RAM_RAS_L				200.0000				9 11
	MEM_CAS_L		4						9
	RAM_CAS_L				200.0000				9 11
	MEM_WE_L		4						9
	RAM_WE_L				200.0000				9 11
	MEM_MUXSEL_H<1..0>		3						9 10
	MEM_MUXSEL_L<1..0>		3						9 10
	RAM_MUXSEL_H		5						10
	RAM_MUXSEL_L		5						10

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME		MAX VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM	
INTREPID CLOCKS	SYSCLK_CPU_UF					10 MIL SPACING		8
	SYSCLK_CPU		4		200.0000	10 MIL SPACING		5 8
	INT_CPUFB_OUT		3			10 MIL SPACING		8
	INT_CPUFB_OUT_SHORT		3			10 MIL SPACING		8
	INT_CPUFB_OUT_NORM		3			10 MIL SPACING		8
	INT_CPUFB_IN_NORM		3			10 MIL SPACING		8
	INT_CPUFB_LONG		3			10 MIL SPACING		8
	INT_CPUFB_IN				200.0000	10 MIL SPACING		8
	SYSCLK_DDRCLK_A0_UF		3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A0_L_UF		3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A1_UF		3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A1_L_UF		3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B0_UF		3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B0_L_UF		3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B1_UF		3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B1_L_UF		3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A0	DDRCLK_A0	3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_A0_L	DDRCLK_A0			200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_A1	DDRCLK_A1	3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_A1_L	DDRCLK_A1			200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B0	DDRCLK_B0	3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B0_L	DDRCLK_B0	3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B1	DDRCLK_B1	3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B1_L	DDRCLK_B1	3		200.0000	10 MIL SPACING		9 11
	INT_REF_CLK_OUT		3		200.0000	10 MIL SPACING		14
	INT_REF_CLK_IN				200.0000	10 MIL SPACING		14
	CLK66M_GPU_AGP_UF				200.0000	10 MIL SPACING		12
	CLK66M_GPU_AGP		4		200.0000	10 MIL SPACING		12 18
	INT_AGP_FB_OUT				200.0000	10 MIL SPACING		12
	INT_AGP_FB_IN		4		200.0000	10 MIL SPACING		12
	CLK33M_CBUS_UF				200.0000	10 MIL SPACING		12
	CLK33M_CBUS	SHOULD BE AT MOST 4 VIAS FOR CLK	6		200.0000	10 MIL SPACING		12 17
	CLK33M_AIRPORT_UF				200.0000	10 MIL SPACING		12
	CLK33M_AIRPORT	SHOULD BE AT MOST 4 VIAS FOR CLK	6		200.0000	10 MIL SPACING		12 25 40
	CLK33M_USB2_UF				200.0000	10 MIL SPACING		12
	CLK33M_USB2	SHOULD BE AT MOST 4 VIAS FOR CLK	6		200.0000	10 MIL SPACING		12 27
	INT_PCI_FB_OUT				200.0000	10 MIL SPACING		12
	INT_PCI_FB_IN		3		200.0000	10 MIL SPACING		12
MAP31	GPU_CLK27M_OUT					10 MIL SPACING		
	GPU_CLK27M_UF					10 MIL SPACING		
	GPU_SSCLK_UF					10 MIL SPACING		
	GPU_SSCLK_IN					10 MIL SPACING		
	GPU_FBCLK0					10 MIL SPACING		
	GPU_FBCLK0_L					10 MIL SPACING		
	GPU_FBCLK1					10 MIL SPACING		
	GPU_FBCLK1_L					10 MIL SPACING		
	GPU_DVO_CLKP					10 MIL SPACING		19
CRYSTALS	CLK27M_GPU_XOUT					10 MIL SPACING		
	CLK27M_XTAL_IN					10 MIL SPACING		
	CLK27M_GPU_XIN					10 MIL SPACING		
	CLK18M_INT_XIN					10 MIL SPACING		14
	CLK18M_INT_XOUT					10 MIL SPACING		14
	CLK18M_XTAL_IN					10 MIL SPACING		14
	CLK18M_INT_EXT					10 MIL SPACING		14
	CLK25M_ENET_XIN					10 MIL SPACING		28
	CLK25M_ENET_XOUT					10 MIL SPACING		28
	NEC_XT1					10 MIL SPACING		27
	NEC_XT2	THERE'S ANOTHER 280MIL LEG				10 MIL SPACING		27
SOUND	SND_SCLK		7		200.0000	10 MIL SPACING		14 26 40
	SND_CLKOUT				200.0000	10 MIL SPACING		14 26 40
ETHERNET MARVELL	CLKENET_PHY_RX				200.0000			28
	CLKENET_LINK_RX		3		200.0000	10 MIL SPACING		13 28
	CLKENET_PHY_GBE_REF				200.0000			28
	CLKENET_LINK_GBE_REF		3		200.0000	10 MIL SPACING		13 28
	CLKENET_PHY_TX				200.0000			28
	CLKENET_LINK_TX		5		200.0000	10 MIL SPACING		13 28
	CLKENET_LINK_GTX				200.0000			13
	CLKENET_PHY_GTX		3		200.0000	10 MIL SPACING		13 28
FIREWIRE	CLKFW_PHY_PCLK				200.0000			29
	CLKFW_LINK_PCLK		3		200.0000	10 MIL SPACING		13 29
	CLKFW_PHY_LCLK		3		200.0000	10 MIL SPACING		13 29
	CLKFW_LINK_LCLK				200.0000			13
	FW_XI				200.0000	10 MIL SPACING		29
	FW_OSC				200.0000	10 MIL SPACING		29

SIGNAL CONSTRAINTS - PAGE 1

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6694 | REV. G

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Digital Signals (cont'd)

GROUP	SIG_NAME	DELAY_RULE	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
AGP	AGP_AD<15..0>		5	100				66 MHz	12 18
AGP BYTES 0-1	AGP_CBE<1..0>		5	100				66 MHz	12 18
	AGP_AD_STB<0>		5	100		8 MIL SPACING			12 18
	AGP_AD_STB_L<0>		5	100		8 MIL SPACING			12 18
AGP BYTES 2-3	AGP_AD<31..16>		5	100				66 MHz	12 18
	AGP_CBE<3..2>		5	100				66 MHz	12 18
	AGP_AD_STB<1>		5	100		8 MIL SPACING			12 18
	AGP_AD_STB_L<1>			100		8 MIL SPACING			12 18
AGP SIDEBAND	AGP_SBA<7..0>		5	100				66 MHz	12 18
	AGP_SB_STB			100.0000		8 MIL SPACING			12 18
	AGP_SB_STB_L		5	100.0000		8 MIL SPACING			12 18
AGP CONTROL	AGP_FRAME_L			250.0000					12 18
	AGP_IRDY_L			250.0000					12 18
	AGP_TRDY_L		6	250.0000					12 18
	AGP_DEVSEL_L			250.0000					12 18
	AGP_STOP_L		6	250.0000					12 18
	AGP_PAR		6	250.0000					12 18
	AGP_REQ_L			285.0000					12 18
	AGP_GNT_L			250.0000					12 18
	AGP_RBF_L			250.0000					12 18
DVO	GPU_DVOD<0..23>		5	250					19 20
	GPU_DVO_HSYNC								19 20
	GPU_DVO_VSYNC								19 20
PCI	PCI_AD<31..0>					MIN_DAISY_CHAIN		33 MHz	9 12 17 25 27 40
	PCI_CBE<3..0>					MIN_DAISY_CHAIN		33 MHz	12 17 25 27 40
	PCI_FRAME_L					MIN_DAISY_CHAIN			12 17 25 27 40
	PCI_IRDY_L					MIN_DAISY_CHAIN			12 17 25 27 40
	PCI_TRDY_L					MIN_DAISY_CHAIN			12 17 25 27 40
	PCI_DEVSEL_L					MIN_DAISY_CHAIN			12 17 25 27 40
	PCI_STOP_L					MIN_DAISY_CHAIN			12 17 25 27 40
	PCI_PAR					MIN_DAISY_CHAIN			12 17 25 27 40
ULTRA ATA-100	UIDE_DATA<15..8>				200			100 MHZ	13 25
	UIDE_DATA<7>			NEED TO MATCH DELAY TO 250	200				13 25
	UIDE_DATA<6..0>				200			100 MHZ	13 25
	UIDE_ADDR<2..0>				200			100 MHZ	13 25
	UIDE_RST_L				200.0000				13 25
	UIDE_DIOW_L				200.0000				13 25
	UIDE_DIOR_L			10 MIL SPACING	200.0000				13 25
	UIDE_DMACK_L				200.0000				13 25
	UIDE_CS0_L				200.0000				13 25
	UIDE_CS1_L				200.0000				13 25
	UIDE_DMARQ				200.0000				13
	UIDE_IOCHRDY			10 MIL SPACING	200.0000				13 25
	UIDE_INTRQ				200.0000				13
	HD_DATA<15..0>		5	TOTAL UIDE+HD SKEW <500MIL	200			100 MHZ	25
	HD_ADDR<2..0>		5		200			100 MHZ	25
	HD_RESET_L		5		200.0000				25
	HD_DIOW_L		5		200.0000				25
	HD_DIOR_L		5	10 MIL SPACING	200.0000				25
	HD_DMACK_L		5		200.0000				25
	HD_CS0_L		5		200.0000				25
	HD_CS1_L		5		200.0000				25
	HD_DMARQ				200.0000				13 25
	HD_IOCHRDY		5	10 MIL SPACING	200.0000				25
	HD_INTRQ		5						13 25
EIDE INTREPID	EIDE_DATA<15..0>							33 MHZ	13 25
	EIDE_ADDR<2..0>							33 MHZ	13 25
	EIDE_CS0_L								13 25
	EIDE_CS1_L								13 25
	EIDE_RD_L								13 25
	EIDE_WR_L								13 25
	EIDE_IOCHRDY								13 25
	EIDE_INT								13 25
	EIDE_RST_L								13 25
	EIDE_DMACK_L								13 25
	EIDE_DMARQ								13 25
OPTICAL	EIDE_OPTICAL_DATA<15..0>							33 MHZ	25 40
	EIDE_OPTICAL_ADDR<2..0>							33 MHZ	25 40
	EIDE_OPTICAL_CS0_L								25 40
	EIDE_OPTICAL_CS1_L								25 40
	EIDE_OPTICAL_RD_L								25 40
	EIDE_OPTICAL_WR_L								25 40
	EIDE_OPTICAL_IOCHRDY								25 40
	EIDE_OPTICAL_INT								25 40
	EIDE_OPTICAL_RST_L								25 40
	EIDE_OPTICAL_DMAACK_L								25 40
	EIDE_OPTICAL_DMA_RQ								25 40
ETHERNET MII	ENET_LINK_RXD<7..0>		5						13 28
	ENET_RX_DV								13 28
	ENET_RX_ER								13 28
	ENET_PHY_TXD<7..0>		5						13 28
	ENET_LINK_TXD<7..0>								13
	ENET_PHY_TX_ER		5						13 28
	ENET_LINK_TX_ER								13
	ENET_PHY_TX_EN		5						13 28
	ENET_LINK_TX_EN								13
	ENET_MDIO								13 28
	ENET_MDC								13 28
	ENET_COL								13 28
	ENET_CRS								13 28
FIREWIRE MII	FW_LINK_DATA<7..0>		5						13 29
	FW_PHY_DATA<7..0>		5						29
	FW_LINK_CNTL<1..0>								13 29
	FW_PHY_CNTL<1..0>								29
	FW_LINK_LREQ								13
	FW_PHY_LREQ								13 29
	FW_PINT								13 29

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR	MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS	
ETHERNET	MDI_M<0>	ENET_MDI0				28
	MDI_P<0>	ENET_MDI0				28
	MDI_M<1>	ENET_MDI1	SPACING DELETED BECAUSE			28
	MDI_P<1>	ENET_MDI1	OF PHYSICAL CONSTRAINTS			28
	MDI_M<2>	ENET_MDI2	AROUND MARVELL PHY			28
	MDI_P<2>	ENET_MDI2				28
	MDI_M<3>	ENET_MDI3				28
	MDI_P<3>	ENET_MDI3				28
	RJ45_DN<0>	RJ45_DP0		10 MIL SPACING		28 40
	RJ45_DP<0>	RJ45_DP0		10 MIL SPACING		28 40
	RJ45_DN<1>	RJ45_DP1		10 MIL SPACING		28 40
	RJ45_DP<1>	RJ45_DP1		10 MIL SPACING		28 40
	RJ45_DN<2>	RJ45_DP2		10 MIL SPACING		28 40
	RJ45_DP<2>	RJ45_DP2		10 MIL SPACING		28 40
	RJ45_DN<3>	RJ45_DP3		10 MIL SPACING		28 40
	RJ45_DP<3>	RJ45_DP3		10 MIL SPACING		28 40
FIREWIRE	FW_TPA0N	FW_TPA0		MIN_LINE_WIDTH=3.4		
	FW_TPA0P	FW_TPA0		10 MIL SPACING		29 30
	FW_TPB0N	FW_TPB0		MIN_LINE_WIDTH=3.4		
	FW_TPB0P	FW_TPB0		10 MIL SPACING		29 30
	FW_TPI0N	FW_TPI0		MIN_LINE_WIDTH=3.4		
	FW_TPI0P	FW_TPI0		10 MIL SPACING		29 30
	FW_TPO0N	FW_TPO0		MIN_LINE_WIDTH=3.4		
	FW_TPO0P	FW_TPO0		10 MIL SPACING		30 40
	FW_TPA1N	FW_TPA1	500.0000	MIN_LINE_WIDTH=3.4		
	FW_TPA1P	FW_TPA1	500.0000	10 MIL SPACING		29 30
	FW_TPB1N	FW_TPB1	500.0000	MIN_LINE_WIDTH=3.4		
	FW_TPB1P	FW_TPB1	500.0000	10 MIL SPACING		29 30
	FW_TPI1N	FW_TPI1		MIN_LINE_WIDTH=3.4		
	FW_TPI1P	FW_TPI1		10 MIL SPACING		29 30
	FW_TPO1N	FW_TPO1		MIN_LINE_WIDTH=3.4		
	FW_TPO1P	FW_TPO1		10 MIL SPACING		30 40
LVDS LOWER	CLKLVDS_LN	CLKLVDS_L		10 MIL SPACING	4	30 40
	CLKLVDS_LP	CLKLVDS_L		10 MIL SPACING	4	19 22 40
	LVDS_L0N	LVDS_L0		10 MIL SPACING		19 22 40
	LVDS_L0P	LVDS_L0		10 MIL SPACING		19 22 40
	LVDS_L1N	LVDS_L1		10 MIL SPACING		19 22 40
	LVDS_L1P	LVDS_L1		10 MIL SPACING		19 22 40
	LVDS_L2N	LVDS_L2		10 MIL SPACING		19 22 40
	LVDS_L2P	LVDS_L2		10 MIL SPACING		19 22 40
UPPER	CLKLVDS_UN	CLKLVDS_U		10 MIL SPACING	4	19 22 40
	CLKLVDS_UP	CLKLVDS_U		10 MIL SPACING	4	19 22 40
	LVDS_U0N	LVDS_U0		10 MIL SPACING		19 22 40
	LVDS_U0P	LVDS_U0		10 MIL SPACING		19 22 40
	LVDS_U1N	LVDS_U1		10 MIL SPACING		19 22 40
	LVDS_U1P	LVDS_U1		10 MIL SPACING		19 22 40
	LVDS_U2N	LVDS_U2		10 MIL SPACING		19 22 40
	LVDS_U2P	LVDS_U2		10 MIL SPACING		19 22 40
TMDS	TMDS_CONN_CLKN	CLKCONN_TMDS		10 MIL SPACING	4	22 40
	TMDS_CONN_CLKP	CLKCONN_TMDS		10 MIL SPACING	4	22 40
	TMDS_CLKN	CLKTMDS		10 MIL SPACING	4	20 22
	TMDS_CLKP	CLKTMDS		10 MIL SPACING	4	20 22
	TMDS_DN<0>	TMDS_D0		10 MIL SPACING		20 22 40
	TMDS_DP<0>	TMDS_D0		10 MIL SPACING		20 22 40
	TMDS_DN<1>	TMDS_D1		10 MIL SPACING		20 22 40
	TMDS_DP<1>	TMDS_D1		10 MIL SPACING		20 22 40
	TMDS_DN<2>	TMDS_D2		10 MIL SPACING		20 22 40
	TMDS_DP<2>	TMDS_D2		10 MIL SPACING		20 22 40
USB	NEC_USB_DAM	NEC_USB_DA	MIN_LINE_WIDTH=5	10 MIL SPACING		27
	NEC_USB_DAP	NEC_USB_DA	MIN_LINE_WIDTH=5	10 MIL SPACING		27
	USB_DEM	USB_DE		5 MIL SPACING		14
	USB_DEP	USB_DE		5 MIL SPACING		14
	NEC_USB_DBM	NEC_USB_DB	MIN_LINE_WIDTH=5	10 MIL SPACING		27
	NEC_USB_DBP	NEC_USB_DB	MIN_LINE_WIDTH=5	10 MIL SPACING		27
	USB_DFM	USB_DF		5 MIL SPACING		14
	USB_DFP	USB_DF		5 MIL SPACING		14
	BT_USB_DM	BT_USB_D		5 MIL SPACING		14 25 40
	BT_USB_DP	BT_USB_D		5 MIL SPACING		14 25 40
	NEC_USB_RSDM1	NEC_USB_RSD1	MIN_LINE_WIDTH=5	10 MIL SPACING		27
	NEC_USB_RSDP1	NEC_USB_RSD1	MIN_LINE_WIDTH=5	10 MIL SPACING		27
	NEC_USB_RSDM2	NEC_USB_RSD2	MIN_LINE_WIDTH=5	10 MIL SPACING		27
	NEC_USB_RSDP2	NEC_USB_RSD2	MIN_LINE_WIDTH=5	10 MIL SPACING		27
	MODEM_USB_DM	MODEM_USB_D		5 MIL SPACING		14 26 40
	MODEM_USB_DP	MODEM_USB_D		5 MIL SPACING		14 26 40
	LEFT_USB_DM	LEFT_USB	MIN_LINE_WIDTH=5	10 MIL SPACING		25 27 40
	LEFT_USB_DP	LEFT_USB	MIN_LINE_WIDTH=5	10 MIL SPACING		25 27 40
	RIGHT_USB_DM	RIGHT_USB	MIN_LINE_WIDTH=5	10 MIL SPACING		27 33 40
	RIGHT_USB_DP	RIGHT_USB	MIN_LINE_WIDTH=5	10 MIL SPACING		27 33 40
POWER SUPPLIES	1772_CSSN	1772_CSS		DIFF		32
	1772_CSSP	1772_CSS		DIFF		32
	1772_CSIN	1772_CSI		DIFF		32
	1772_CSIP	1772_CSI		DIFF		32
	3V_SNSM	3V_SNS		DIFF		34
	3V_SNSP	3V_SNS		DIFF		34
	5V_SNSM	5V_SNS		DIFF		34
	5V_SNSP	5V_SNS		DIFF		34
THERMOSTAT	THERM1_DM	THERM1		DIFF		26
	THERM1_DP	THERM1		DIFF		26
	THERM2_DM	THERM2		DIFF		26
	THERM2_DP	THERM2		DIFF		26
	THERM1_M_DM	THERM1_MAIN		DIFF		
	THERM1_M_DP	THERM1_MAIN		DIFF		
	THERM2_M_DM	THERM2_MAIN		DIFF		
	THERM2_M_DP	THERM2_MAIN		DIFF		
	THERM1_A_DM	THERM1_ALT		DIFF		26
	THERM1_A_DP	THERM1_ALT		DIFF		26
	THERM2_A_DM	THERM2_ALT		DIFF		26
	THERM2_A_DP	THERM2_ALT		DIFF		26

INTERNAL LAYER

ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.57OHM
ZDIFF = 99.8OHM

FOR FIREWIRE
ER = 4.3 (DIELECTRIC CONSTANT)
W = 3.4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 53.37OHM
ZDIFF = 107.17OHM

INTERNAL LAYER (USB1.1/USB 2.0)

ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL(USB 1.1)/ 5MIL(USB 2.0) (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 5MIL (USB 1.1) (SEPERATION OF DIFF TRACES)
S = 10MIL (USB 2.0) (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.5OHM (USB 1.1)/ 46.2OHM (USB 2.0)
ZDIFF = 89.3OHM (USB 1.1)/ 89.4OHM (USB 2.0)

SIGNAL CONSTRAINTS - PAGE 2

APPLE COMPUTER INC.

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POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH
MAIN/SLEEP	+24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 40
	+BATT	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 40
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 23
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 23
	+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6 20 23
	+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 40
	+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+2_5V_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6 40
	+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+1_5V_SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	+1_5V_LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 36
	+1_5V_SLEEP_VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 36
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 32 33
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 32
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 32
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 32 40
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 32 40
	1772_DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10	32
	1772_LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 32
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 32
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 32
	+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 32
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 32
	1772_LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 32
	1772_DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 32
	1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 32
PMU	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 33
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 33
	+4_85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 31 33
	+4_6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 33 34
	+4_85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 33
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 33
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 26 31
MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 25 34
	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 25
TRACKPAD	+5V_MAIN_CONN	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 23 40
VIDEO	+12_8V_INV	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 22 40
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 22
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 22 40
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 22 40
	+5V_DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 22
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10 22
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 22
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 22
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 22
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 22 40
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 22 40
KB LED	KBDLED_ANODE	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 23
	KBDLED_RETURN	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 23
FAN GND	FANL_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 40
	FANR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 40
SOUND	+5V_SOUND_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	SND_AGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=15 26

	GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6
I/O AREA	CHGND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12 CHGND1
INVERTER	CHGND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12 CHGND2
TRACKPAD	CHGND3	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12 CHGND3
LVDS	CHGND4	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12 CHGND4 40
I/O AREA	CHGND5	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12 CHGND5
I/O AREA	CHGND6	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12 CHGND6
	ENET_CTAP_CHGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12 28

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 5 6 35 40
	CPU_AVDD	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 5
	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 5 6 7 8 15 16 35
DDR RAM	DDR_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 11
INTREPID	+2_5V_INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 9 10 15 16
	+3V_INTREPID_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 14
PLLS	+1_5V_INTREPID_PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 8 12 14
	+1_5V_INTREPID_PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6 14
	+1_5V_INTREPID_PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6 14
	+1_5V_INTREPID_PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6 14
	+1_5V_INTREPID_PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5 14
	+1_5V_INTREPID_PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5 12
	+1_5V_INTREPID_PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6 12
	+1_5V_INTREPID_PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6 8
	+1_5V_INTREPID_PLL8	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6 14
REFERENCE	INT_MEM_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 9
	INT_AGP_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 12 18
	INT_MEM_REF_H	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 9
	UIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 13
CARDBUS	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 17
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 17
ATI M11	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10 18 19 40
	+GPU_MEM	VOLTAGE=2.5V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10 18 21
	+3V_GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 12 18 19 21
	+3V_GPU_FLT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8 21
	+1_5V_AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 12 15 16 18 19 21
	GPU_MEM_IO	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	GPU_MEM_IO_FLT	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 21
	+GPU_MEMCORE	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 21
	+1_8V_GPU	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 18 19 20 21
	+2_5V_GPU_PNLIO	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 21
	+1_8V_ATI_PVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 19 21
	+1_5V_AGP_GPU	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 21
	+1_5V_GPU_VDD15	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 19
	+1_8V_GPU_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 21
134	+1_8V_GPU_VDDDI	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 21
135	GPU_VCORE_VDDCI	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 18
136	+2_5V_GPU_A2VDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 21
137	+1_8V_GPU_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 21
138	+1_8V_GPU_PNLPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 21
139	+1_8V_GPU_PNLIO	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 21
140	GPU_MCLK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 21
141	+1_8V_GPU_AVDDQ	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 21
142	+1_8V_GPU_MEMPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 21
143	+3V_ATI_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 18
144	+3V_ATI_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 18
145	+GPU_VDD15_UF	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 19
146	+2_5V_SLEEP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 19
147	+3V_SLEEP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 21
148	+1_5V_AGP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 19
149	+1_8V_PVDD_NECK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 19
150	GPU_VCORE_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 19
151	+GPU_VDD15_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 19
152	+2_5V_SLEEP_NECK2	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 21
153	+1_8V_SLEEP_NECK	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 21
154	+2_5V_SLEEP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 21
155	+2_5V_GPU	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 21
SILICON IMIAGE	PP3V3_SI_PVCC1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0 20
	PP3V3_SI_AVCC1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0 20
	PP3V3_SI_VCC1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0 20
156	PP3V3_SI_PVCC2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0 20
157	PP3V3_SI_AVCC2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0 20
158	PP3V3_SI_VCC2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0 20
88E1111	+2_5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 28
	+2_5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8 28
	+1_0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8 28
	LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8 28
	LM2594_IN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
FW	+3V_FW_ESD_ILIM	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 30
	+3V_FW_ESD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 30
	+FW_FUSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30
	+FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30
	+FW_PWR_OR	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 29 30
	+FW_VP0	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30
	+FW_PWR_PORTA	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30
	+FW_VP1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30
	+3V_FW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29 30
	+3V_FW_UF	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6 29
	+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_PLLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	+1_95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 29
	FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30
	FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12 30
	FW_TPO0R	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 30 40
USB 2.0	NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 27
INTREPID	+3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 27
SSCG	+3V_CG_PLL_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8 14
	+2_5V_CG_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8 14

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 33
	1625_VSW	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 33
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 33
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 33
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 33
	1V20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 2 33
LTC3707 5V SWITCHER	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10 4
	5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 4
	5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 4
3V SWITCHER	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 4
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 4
	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6 34
MAX1715 2.5V SWITCHER	2_5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 6
	2_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 6
	2_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 6
	2_5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 6
	2_5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 6
1.5V SWITCHER	1_5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 36
	1_5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 6
	1_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 6
	1_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 6
	1_5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 6
	1_5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 6
CONTROL	1_5V_ILIM		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 36
	2_5V_ILIM		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 36
	MAX1715_TON		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 36
	MAX1715_SKIP		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 36
	MAX1715_REF	VOLTAGE=2.0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 36
	MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 6
	MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10 6
MAX1717	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 5
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 5
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 5
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 5
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 5
	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 5
	VCORE_ILIM		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 35
	VCORE_REF		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 35
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 35
	VCORE_CC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 35
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 35 40
	VCORE_TIME		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 35
	VCORE_VGATE		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 14 35
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=15 5
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 35
	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 35
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 35
LTC1778	1778_VIN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 9
	1778_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 9
	1778_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10 9
	1778_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 9
	1778_BST_RC	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10 9
	1778_TG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 9
	1778_BG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 9
	GPU_VCORE_SW	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10 9
	1778_ION		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 19
	1778_ITH		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 19
	1778_ITH_RC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 19
	1_5V_2_5V_OK		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 36
	1778_VFB		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 19 40
	1778_FCB		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 19
	1778_VRNG		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6 19
LTC3411	LTC3411_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	LTC3411_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10
	1_8V_SW	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10 6
	1_8V_VFB		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6
	LTC3411_ITH_RC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6
	LTC3411_ITH		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6
	LTC3411_SYNC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6
	LTC3411_SHDN		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6
LTC1962 INT PLLS	LTC1962_INT_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10 4
	LTC1962_L3_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	LTC1962_L3_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	LTC1962_1V5_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10
	LTC1962_1V5_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10

SIGNAL CONSTRAINTS - PAGE 3

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE: NONE	SHT 39 OF 45	

FUNCTIONAL TEST POINTS

FUNC_TEST=YES JTAG_ASIC_TMS 13 28
FUNC_TEST=YES JTAG_ASIC_TDI 28
FUNC_TEST=YES JTAG_ASIC_TDO 13 14
FUNC_TEST=YES JTAG_ASIC_TCK 13 28
FUNC_TEST=YES JTAG_ASIC_TRST_L 13 28
FUNC_TEST=YES CPU_CHKSTP_OUT_L 5
FUNC_TEST=YES CPU_SRESET_L 5
FUNC_TEST=YES CPU_HRESET_L 5 6 7
FUNC_TEST=YES JTAG_CPU_TMS 5 6
FUNC_TEST=YES JTAG_CPU_TDI 5 6
FUNC_TEST=YES JTAG_CPU_TDO_TP 5
FUNC_TEST=YES JTAG_CPU_TCK 5 6
FUNC_TEST=YES JTAG_CPU_TRST_L 5 6 40

FUNC_TEST=YES TMDS_CONN_CLKP 22 38
FUNC_TEST=YES VGA_R 22
FUNC_TEST=YES VGA_G 22
FUNC_TEST=YES VGA_B 22
FUNC_TEST=YES VGA_VSYNC 22
FUNC_TEST=YES VGA_HSYNC 22
FUNC_TEST=YES DVI_DDC_CLK_UF 22
FUNC_TEST=YES DVI_DDC_DATA_UF 22
FUNC_TEST=YES DVI_HPD_UF 22
FUNC_TEST=YES LVDS_L0N 19 22 38
FUNC_TEST=YES LVDS_L0P 19 22 38
FUNC_TEST=YES LVDS_L1N 19 22 38
FUNC_TEST=YES LVDS_L1P 19 22 38
FUNC_TEST=YES LVDS_L2N 19 22 38
FUNC_TEST=YES LVDS_L2P 19 22 38
FUNC_TEST=YES CLKLVDS_LN 19 22 38
FUNC_TEST=YES CLKLVDS_LP 19 22 38
FUNC_TEST=YES LVDS_U0N 19 22 38
FUNC_TEST=YES LVDS_U0P 19 22 38
FUNC_TEST=YES LVDS_U1N 19 22 38
FUNC_TEST=YES LVDS_U1P 19 22 38
FUNC_TEST=YES LVDS_U2N 19 22 38
FUNC_TEST=YES LVDS_U2P 19 22 38
FUNC_TEST=YES CLKLVDS_UN 19 22 38
FUNC_TEST=YES CLKLVDS_UP 19 22 38
FUNC_TEST=YES LVDS_DDC_CLK 19 22
FUNC_TEST=YES LVDS_DDC_DATA 19 22
FUNC_TEST=YES BRIGHT_PWM 22
FUNC_TEST=YES TV_GND1 22 39
FUNC_TEST=YES TV_GND2 22 39

FUNC_TEST=YES TV_C 22
FUNC_TEST=YES TV_Y 22
FUNC_TEST=YES TV_COMP 22
FUNC_TEST=YES SND_TO_AUDIO 14 26
FUNC_TEST=YES SND_SYNC 14 26
FUNC_TEST=YES SND_CLKOUT 14 26 37

FUNC_TEST=YES INT_AUDIO_TO_SND 14 26
FUNC_TEST=YES SND_SCLK 14 26 37
FUNC_TEST=YES SND_HW_RESET_L 14 26
FUNC_TEST=YES SND_HP_SENSE_L
FUNC_TEST=YES SND_LIN_SENSE_L
FUNC_TEST=YES INT_I2C_DATA2 14 26
FUNC_TEST=YES INT_I2C_CLK2 14 26

T393 FUNC_TEST=YES CHGND4 39
T394 FUNC_TEST=YES SLEEP_LED

FUNC_TEST=YES INT_I2C_CLK0 6 11 13 23
FUNC_TEST=YES INT_I2C_DATA0 6 11 13 23
FUNC_TEST=YES INT_I2C_CLK1 13 14 23 24 26
FUNC_TEST=YES INT_I2C_DATA1 13 14 23 24 26
FUNC_TEST=YES CBUS_DET_1_L 17
FUNC_TEST=YES CBUS_DET_2_L 17
FUNC_TEST=YES TMDS_DN<0> 20 22 38
FUNC_TEST=YES TMDS_DP<0> 20 22 38
FUNC_TEST=YES TMDS_DN<1> 20 22 38
FUNC_TEST=YES TMDS_DP<1> 20 22 38
FUNC_TEST=YES TMDS_DN<2> 20 22 38
FUNC_TEST=YES TMDS_DP<2> 20 22 38
FUNC_TEST=YES TMDS_CONN_CLKN 22 38

FUNC_TEST=YES BT_USB_DM 14 25 38
FUNC_TEST=YES BT_USB_DP 14 25 38
FUNC_TEST=YES MODEM_USB_DM 14 26 38
FUNC_TEST=YES MODEM_USB_DP 14 26 38
FUNC_TEST=YES PCI_AD<0> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<1> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<2> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<3> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<4> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<5> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<6> 9 12 17 25 27 38

FUNC_TEST=YES PCI_AD<7> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<8> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<9> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<10> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<11> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<12> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<13> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<14> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<15> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<16> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<17> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<18> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<19> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<20> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<21> 12 17 25 27 38
FUNC_TEST=YES PCI_AD<22> 12 17 25 27 38
FUNC_TEST=YES PCI_AD<23> 12 17 25 27 38
FUNC_TEST=YES PCI_AD<24> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<25> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<26> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<27> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<28> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<29> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<30> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<31> 9 12 17 25 27 38
FUNC_TEST=YES PCI_FRAME_L 12 17 25 27 38
FUNC_TEST=YES PCI_TRDY_L 12 17 25 27 38
FUNC_TEST=YES PCI_IRDY_L 12 17 25 27 38
FUNC_TEST=YES PCI_DEVSEL_L 12 17 25 27 38
FUNC_TEST=YES PCI_STOP_L 12 17 25 27 38

FUNC_TEST=YES PCI_PAR 12 17 25 27 38
FUNC_TEST=YES PCI_CBE<0> 12 17 25 27 38
FUNC_TEST=YES PCI_CBE<1> 12 17 25 27 38
FUNC_TEST=YES PCI_CBE<2> 12 17 25 27 38
FUNC_TEST=YES PCI_CBE<3> 12 17 25 27 38
FUNC_TEST=YES AIRPORT_PCI_REQ_L 12 25
FUNC_TEST=YES AIRPORT_PCI_GNT_L 12 25
FUNC_TEST=YES AIRPORT_PCI_INT_L 14 25
FUNC_TEST=YES EIDE_OPTICAL_DATA<0> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<1> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<2> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<3> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<4> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<5> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<6> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<7> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<8> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<9> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<10> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<11> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<12> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<13> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<14> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<15> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DMA_RQ 25 38
FUNC_TEST=YES EIDE_OPTICAL_RD_L 25 38
FUNC_TEST=YES EIDE_OPTICAL_DMAACK_L 25 38
FUNC_TEST=YES EIDE_OPTICAL_ADDR<0> 25 38
FUNC_TEST=YES EIDE_OPTICAL_ADDR<1> 25 38
FUNC_TEST=YES EIDE_OPTICAL_ADDR<2> 25 38
U29 FUNC_TEST=YES SND_AMP_MUTE 26
U29 FUNC_TEST=YES SND_HP_MUTE_INV

FUNC_TEST=YES EIDE_OPTICAL_CS0_L 25 38
FUNC_TEST=YES EIDE_OPTICAL_CS1_L 25 38
FUNC_TEST=YES EIDE_OPTICAL_RST_L 25 38
FUNC_TEST=YES EIDE_OPTICAL_WR_L 25 38
FUNC_TEST=YES EIDE_OPTICAL_IOCHRDY 25 38
FUNC_TEST=YES EIDE_OPTICAL_INT 25 38
FUNC_TEST=YES TPAD_F_TXD
FUNC_TEST=YES TPAD_F_RXD
FUNC_TEST=YES LID_CLOSED_L 23
FUNC_TEST=YES COMM_RESET_L 14 26
FUNC_TEST=YES COMM_SHUTDOWN 14 26
FUNC_TEST=YES COMM_RING_DET_L 14 26 31

FUNC_TEST=YES +5V_TPAD_SLEEP
FUNC_TEST=YES +3V_HALL_EFFECT 23 39
FUNC_TEST=YES KBD_CAPSLOCK_LED
FUNC_TEST=YES KBD_FUNCTION_L 23 31
FUNC_TEST=YES KBD_CONTROL_L 23 31
U29 FUNC_TEST=YES +PPBATT_ISNS_N 24
FUNC_TEST=YES KBD_OPTION_L 23 31
FUNC_TEST=YES KBD_SHIFT_L 23 31
FUNC_TEST=YES KBD_X<0> 23 31
FUNC_TEST=YES KBD_X<1> 23 31
FUNC_TEST=YES KBD_X<3> 23 31
U29 FUNC_TEST=YES MMM_ACC_SELFTEST 24
U29 FUNC_TEST=YES MMM_ACC_X_AXIS 24
U29 FUNC_TEST=YES MMM_ACC_Y_AXIS 24
U29 FUNC_TEST=YES MMM_ACC_Z_AXIS 24

U28 FUNC_TEST=YES SRCLK_TP 27
U28 FUNC_TEST=YES SRMOD_TP 27
U28 FUNC_TEST=YES TEB_TP 27
U29 FUNC_TEST=YES TEST_TP 27

FUNC_TEST=YES KBD_Y<0> 31
FUNC_TEST=YES KBD_Y<1> 31
FUNC_TEST=YES KBD_Y<3> 31
FUNC_TEST=YES KBD_Y<4> 31
FUNC_TEST=YES KBD_Y<6> 31
FUNC_TEST=YES KBD_Y<7> 31
FUNC_TEST=YES KBD_NUMLOCK_LED
FUNC_TEST=YES +BATT_POS 32 39
FUNC_TEST=YES BATT_CLK 32
FUNC_TEST=YES BATT_DATA 32
FUNC_TEST=YES BATT_NEG 32 39
FUNC_TEST=YES PMU_BATT_DET_L 31 32
FUNC_TEST=YES FANR_GND 39

FUNC_TEST=YES FANL_GND 39
FUNC_TEST=YES FANL_TACH
FUNC_TEST=YES FANR_PWM
U27 FUNC_TEST=YES FANL_PWM
FUNC_TEST=YES RJ45_DP<0> 28 38
FUNC_TEST=YES RJ45_DN<0> 28 38
FUNC_TEST=YES RJ45_DP<1> 28 38
FUNC_TEST=YES RJ45_DN<1> 28 38
FUNC_TEST=YES RJ45_DP<2> 28 38
FUNC_TEST=YES RJ45_DN<2> 28 38
FUNC_TEST=YES RJ45_DP<3> 28 38
FUNC_TEST=YES RJ45_DN<3> 28 38
FUNC_TEST=YES FW_TPO0R 30 39
FUNC_TEST=YES VCORE_VID0
U28 FUNC_TEST=YES VCORE_VID1
U28 FUNC_TEST=YES VCORE_VID2
U28 FUNC_TEST=YES VCORE_VID3
U28 FUNC_TEST=YES VCORE_VID4

FUNC_TEST=YES FW_TPO1P 30 38
FUNC_TEST=YES FW_TPO1N 30 38
FUNC_TEST=YES FW_TPI1P 30 38
FUNC_TEST=YES FW_TPI1N 30 38
FUNC_TEST=YES CHARGE_LED_L 31 32
FUNC_TEST=YES ADAPTER_DET 31 32
FUNC_TEST=YES SUTRO_ALS_GAIN_SW 23 25
FUNC_TEST=YES SUTRO_ALS_OUT 23 25
FUNC_TEST=YES KBD_LED1_OUT
FUNC_TEST=YES KBD_LED2_OUT
FUNC_TEST=YES COMM_TXD_L 14 26
FUNC_TEST=YES COMM_TRXC 14 26
FUNC_TEST=YES COMM_GPIO_L 14 26
FUNC_TEST=YES COMM_DTR_L 14 26
FUNC_TEST=YES COMM_RTS_L 14 26
FUNC_TEST=YES COMM_RXD 14 26
FUNC_TEST=YES PMU_KB_RESET_L
FUNC_TEST=YES PWR_BUTTON_L 23 26
FUNC_TEST=YES +PBUS 39
FUNC_TEST=YES +24V_PBUS 39
FUNC_TEST=YES GPU_VCORE 18 19 39
FUNC_TEST=YES CPU_VCORE_SLEEP 5 6 35 39
FUNC_TEST=YES VCORE_FB 35 39
FUNC_TEST=YES +1_8V_MAIN 39
FUNC_TEST=YES +3V_PMU 39
FUNC_TEST=YES +5V_DDC_SLEEP 22 39
FUNC_TEST=YES +12_8V_INV 22 39
U28 FUNC_TEST=YES VCORE_MUX_EN 35

FUNC_TEST=YES +5V_INV_SW 22 39
FUNC_TEST=YES LEFT_USB_DM 25 27 38
FUNC_TEST=YES LEFT_USB_DP 25 27 38
FUNC_TEST=YES RIGHT_USB_DM 27 33 38
FUNC_TEST=YES RIGHT_USB_DP 27 33 38
FUNC_TEST=YES NEC_LEFT_USB_PWREN 25 27
FUNC_TEST=YES NEC_LEFT_USB_OVERCURRENT 25 27
FUNC_TEST=YES NEC_RIGHT_USB_PWREN 27 33
FUNC_TEST=YES NEC_RIGHT_USB_OVERCURRENT 27 33
FUNC_TEST=YES DCDC_EN 19 30 34 35
FUNC_TEST=YES BBANG_HRESET_L 6

FUNC_TEST=YES MAIN_RESET_L 14 17 18 20 25 27 31
FUNC_TEST=YES RF_DISABLE_L_SPN 25
FUNC_TEST=YES AIRPORT_CLKRUN_L 25
FUNC_TEST=YES ROM_RW_L 9 12 25
FUNC_TEST=YES ROM_ONBOARD_CS_L 9 25
FUNC_TEST=YES ROM_CS_L 9 12 25
FUNC_TEST=YES CLK33M_AIRPORT 12 25 37
FUNC_TEST=YES AIRPORT_IDSEL 25
FUNC_TEST=YES ROM_OE_L 9 12 25
FUNC_TEST=YES INT_MOD_DTI 14 26
U27 FUNC_TEST=YES JTAG_CPU_TRST_L 5 6 40
FUNC_TEST=YES MOD_BITCLK 14 26
U27 FUNC_TEST=YES MOD_CLKOUT 14 26
FUNC_TEST=YES MOD_DTO 14 26
U27 FUNC_TEST=YES MOD_SYNC 14 26
U27 FUNC_TEST=YES SLEEP 23 31 34 36
U28 FUNC_TEST=YES 1778_VFB 19 39

FUNCTIONAL TEST POINTS

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE: NONE	SHT 40 OF 45	

REVISION HISTORY

12/11/03

1) IMPORTED Q41 PRODUCTION RELEASE SCHEMATIC
2) CHANGED CPU (U43) TO A7PM
3) CHANGED PLL CONFIG STUFFING FOR NEW CPU
4) CHANGED U44 TO M1Y-PSP64 SYMBOL
5) ADDED CPU AVDD LDO (U6)
6) ADDED R284 AND R604 TO ADD OPTION FOR PD_I OF U42 (CLOCK CHIP) TO BE DRIVEN BY JTAG_ASIC_TDO FROM INTREPID
7) ADDED R608 TO DISCONNECT INT_GPIO0 FROM CS_FSEL
8) CHANGED JTAG_ASIC_TDO_TP TO JTAG_ASIC_TDO AND MOVED IT TO INTREPID'S TDO
9) CHANGED JTAG_ASIC_TDI TO CONNECT TO ETHERNET PHY'S TDI

12/15/03

10) CHANGED PIN 4 (DCDC_EN) ON J11 TO NEC_RIGHT_USBOVERCURRENT
11) CHANGED PIN 11 OF J11 TO NC

12/16/03

12) ADDED R633 AS PULLUP ON JTAG_ASIC_TDI
13) CHANGED CPU_TEMP_DM TO CPU_THERM_DM
14) CHANGED CPU_TEMP_DP TO CPU_THERM_DP
15) CHANGED GPU_THERM_DP TO GPU_THERM_DP_TP
16) CHANGED GPU_THERM_DM TO GPU_THERM_DM_TP
17) FIXED MISSED CONNECTION WITH MAXBUS_SLEEP TO CPU

12/17/03

18) CHANGED R657 (EXTPLL_SDWN_POL BOOT STRAP) TO NO STUFF AND REMOVED NO STUFF FROM R153
19) UPDATE DIFF NET SPACING TYPE PROPERTY ON POWER SUPPLY SENSE AND THERMAL DIODE DIFF PAIRS
20) CHANGED FIREWIRE OSCILLATOR (G1) TO NEW PREFERRED SUNNY PART

12/18/03

21) CHANGED MAX VIA COUNT ON ALL AGP STB NETS TO 5 TO CLEAR DRCS

** RELEASED FOR EVT **

2/10/04

22) REMOVED XW11 - JUMPER ON 1.8V SWITCHER OUTPUT
23) CHANGED R657 TO STUFFE AND R153 TO NO STUFF
24) CHANGED CPU PLL CONFIG TO 9X HIGH AND 5X LOW

** RELEASED FOR DVT **

3/24/04

25) REMOVED ALTERNATE BOM OPTION FROM ALTERNATE ETHERNET CRYSTALS

3/29/04

26) ADDED ALTERNATE FOR Q41A REV 1.1.1 CPU (U43)
27) ADDED ALTERNATES FOR 128MB AND 64MB A16_M11_S
28) CHANGED TMDS SERIES RPAKS TO 0 OHMS (RP57,RP27,RP32,RP28)
29) ADDED ALTERNATE FOR ALS OP-AMP (U40)

** RELEASED TO REV A **

30) CHANGED TMDS TERMINATION R,C AND LS TO PRODUCTION VALUES

** RELEASED TO REV A UNDER NEW PART NUMBER **

09/17/2004

1) GPU_DVOD<0..12> NETNAME CHANGE TO GPU_DVOD<0..23>
2) D8 FROM 1N5227B CHANGE TO BZX84C2V7LT1
3) R751 VALUE FROM 10K OHM CHANGE TO 604 OHM
4) ADD C935 (0.1UF)
5) ADD R867 (0 OHM) FOR IPOD ACTION
6) PMU PIN74 NETNAME FROM NC TO PMU_SELECT
7) ADD R868 (10K OHM; NO_STUFF) PULL UP TO +3V_PMU
8) ADD R869 (10K OHM) PULL DOWN TO GND
9) PMU PIN 91 NETNAME FROM NC TO SYS_BATT_ISNS2
10)ADD R870 (0 OHM) SYS_BATT_ISNS2 LINK TO SYS_BATT_ISNS
11)ADD U51 (INA138)
12)ADD R852 (0.010 OHM),R853 (150K OHM) AND R857(49.9 OHM)
13)ADD C917 (0.1UF) AND C925 (10UF)
14)ADD DESCRIPTION FOR MMM I2C BUS
15)MMM I2C BUS LINK TO INTREPID :INT_I2C_CLK1 AND INT_I2C_DATA1
16)CHANGE NETNAME FROM INT_EXTINT11_PU TO MMM_FFIRQ_L
17)CHANGE NETNAME FROM INT_EXTINT12_PU TO MMM_SIRQ_L
18)ADD R863 (10K OHM) AND R864 (10K OHM) FOR MMM_FFIRQ_L&MMM_SIRQ_L PULL UP TO +3V_MAIN
19)ADD U53 (16F818) AND U5 (KXM52)
20)ADD R845 (0 OHM),R846 (0 OHM;NO_STUFF),R847 (10K OHM;NO_STUFF),R848 (10K OHM;NO_STUFF)
21)ADD R849 (10K OHM),R850 (10K OHM;NO_STUFF),R851(0 OHM),R854 (10K OHM),R856 (10K OHM),
22)ADD R860 (0 OHM),R858 (0 OHM),R859 (0 OHM),R855 (10K OHM),R861 (10K OHM),R862(10K OHM;NO_STUFF)
23)ADD C936(0.1UF),C918(0.1UF),C919(0.1UF),C921(0.0047UF),C923(0.0047UF),C926(0.0047UF),C927(0.1UF)
24)DEL RP44 (100K OHM) AND ADD R874 (100K OHM), R875 (100K OHM) AND R873 (100K OHM)
25)ADD R872 (10K OHM) FOR AUDIO_LO_MUTE_L
26)ADD R871 (100 OHM) AND SUPERCAP C937 (N20P80;5.5V;ELEC;0.33F)
27)J21 PIN12 NETNAME FROM NC CHANGE TO THERM_L_OC
28)J21 PIN10 NETNAME FROM NC CHANGE TO INT_I2C_DATA1
29)J21 PIN11 NETNAME FROM NC CHANGE TO INT_I2C_CLK1
30)C592 VALUE FROM 0.001UF CHANGE TO 0.01UF (20%,50V,0603)
31)U59 FROM MP1518DJ CHANGE TO MM3120
32)L11 CHANGE TO 152S0235 (22UH;3.8*3.8*1.5MM)
33)DEL D31
34)R202 VALUE FROM 5.23 OHM CHANGE TO 25.5 OHM
35)C79 VALUE FROM 2.2UF CHANGE TO 1UF
36)ADD Q70 (SI3443), Q34 (2N7002)
37)ADD R866 (100K OHM),R865 (4.7 OHM),C929 (0.022UF)

09/20/2004

1) ADD R877 (10K OHM)
2) ADD R876 (470K OHM;NO_STUFF)

09/21/2004

1) ADD R878 AND R879 (0 OHM;NO_STUFF)[ADD A 0-OHM RESISTOR TO BY-PASS THE N-FET ON EACH FAN]

09/22/2004

1) R822 (680 OHM CHANGE TO 510 OHM) AND R826 (680 OHM CHANGE TO 510 OHM)

09/23/2004

1) ADD NC NETNAME AT U59 PIN6 AND PIN9
2) CHANGE R465 CAP SIZE FROM 0603 TO 0805
3) BOM OPTION FROM NO STUFF CHANGE TO SUPERCAP

09/24/2004

1) CHANGE R465 FROM MF 1/16W TO FF 1/10W
2) ADD R880 AND R871 (0 OHM;BOM_OPTIOM;FOR SUPERCAP AND BACKUP BATTERY SWITCH)
3) ADD U60 (LIS3L02AQ;ST SENSOR)
4) ADD R881 (10K OHM) ,R882 (10K OHM), R883 (10K OHM)
5) ADD C937 (0.1UF,10V,20%,0402)
6) ADD BOM_OPTION (KIONIX_ACCEL AND ST_ACCEL)

10/04/2004

1) CHANGE TEST POINT FUNC_TEST=NO FOR FUNC_TP_WRONG_SIDE.LOG
2) ADD NO_TEST=YES FOR NOTP.LOG(MMM_PIC_AN2_PD,MMM_PIC_AN3_PU)

10/05/2004

1) ADD R850 (0 OHM)

10/15/2004

1) REPLACE BOOT BANGER EEPROM U32 WITH 32KX M24256B FUNC_TP_WRONG_SIDE.LOG

12/16/2004

1) SCHEMATIC RELEASE FOR PRODUCTION

04/27/2005 REV.E

1) ADD LEAD FREE PHOTO SENSOR (385-0053)
2) ADD 337S3094 AND 337S3131

06/20/2005 REV.F

1) ADD LEAD FREE PHOTO SENSOR (385-0053)

08/25/2005 REV.G

1) ADDED 337S3216 (IC,A7PM,R1.5,1.67GHZ,1.3V,25W) AS OPTION
2) REPLACED 341S1561 (BOOTROM 4.91.F1) WITH 341S1793 (BOOTROM 4.9.1.F3)
3) ADDED LABEL WITH EEE:U3Y

REVISION HISTORY(1 OF 1)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE: NONE	SHT 41 OF 45	

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*** Signal Cross-Reference for the entire design ***

+1_0V_MARVELL    28D2< 39B3>
+1_5V_AGP        12C5< 12D1< 12D4< 15D6< 16C8<
                18C6< 18D6< 19A8< 19B4<> 19D5<>
                21B8< 21D6< 39C3>
+1_5V_AGP_GPU    21C5< 39C3>
+1_5V_AGP_NECK   19B4<> 39B3>
+1_5V_GPU_VDD15  19D3< 39C3>
+1_5V_INTREPID_PLL  8D6< 12D4< 12D8< 14D6<> 39D3>
+1_5V_INTREPID_PLL1  14C3< 39D3>
+1_5V_INTREPID_PLL2  14D3< 39D3>
+1_5V_INTREPID_PLL3  14D3< 39D3>
+1_5V_INTREPID_PLL4  14D3< 39D3>
+1_5V_INTREPID_PLL5  12D3< 39D3>
+1_5V_INTREPID_PLL6  12D6< 39D3>
+1_5V_INTREPID_PLL7  8D5< 39D3>
+1_5V_INTREPID_PLL8  14D3< 39D3>
+1_5V_LDO        36D8< 39D6>
+1_5V_MAIN       39D6>
+1_5V_SLEEP      39D6>
+1_5V_SLEEP_NECK  21A3<> 39B3>
+1_5V_SLEEP_VIN  36D8<> 39D6>
+1_8V_ATI_PVDD   19C5<> 21B6< 21B6< 21D6<> 39C3>
+1_8V_ATI_TPVDD  21D2<>
+1_8V_DVO_F      21B2<
+1_8V_GPU        18A7< 19C8< 20A8< 21A2< 21A6<
                21B1< 21B6< 21C8< 21D6< 21D8< 39C3>
+1_8V_GPU_AVDD   21D5< 39C3>
+1_8V_GPU_AVDDQ  21D4< 21D7< 39C3>
+1_8V_GPU_MEMPLL  21B5< 39C3>
+1_8V_GPU_PLL    21D5< 39C3>
+1_8V_GPU_PNLIO  21A5< 39C3>
+1_8V_GPU_PNLPLL  21B5< 39C3>
+1_8V_GPU_TP_PLL  21B4< 21D1<
```

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

D

```
NEC_PPON5_TP      27B5>
NEC_RIGHT_USB_OVERCURRENT  27D1< 33B7<> 40C1>
NEC_RIGHT_USB_PWREN  27B5<> 33A7<> 40C1>
NEC_RREF          27B5<>
NEC_SMI_L_TP      27A7>
NEC_USB_DAM       27B4< 27C2<> 38B2>
NEC_USB_DAP       27A4< 27C2<> 38B2>
NEC_USB_DBM       27A4< 27C2<> 38B2>
NEC_USB_DBP       27A4< 27C2<> 38B2>
NEC_USB_RSDM1     27C5<> 38B2>
NEC_USB_RSDM2     27C5<> 38B2>
NEC_USB_RSDP1     27C5<> 38B2>
NEC_USB_RSDP2     27C5<> 38B2>
NEC_XT1           27D5< 37B1>
NEC_XT2           27D5<> 37B1>
NEC_XT2_R         27D4<
NTEST1_TP         27B5<
NUMLOCK_LED_L     31D7<
OVER_18V_ADJ      32C3<>
PA2_PD            23B2< 23C4<>
PA3_PD            23B2< 23C4<>
PB2_PD            23B2< 23C4<>
PB3_PD            23B2< 23C4<>
PB4_PD            23B2< 23C4<>
PC0_PD            23B2< 23B4<>
PCI1510_VR_EN_L  17C7<
PCI_AD<0>       9C3< 12D6<> 17C7<> 25B5<> 27D7<>
                40B6>
PCI_AD<31..0>   3BC5>
PCI_AD<1>       9C3< 12D6<> 17C7<> 25B6<> 27D7<>
                40A6>
PCI_AD<2>       9C3< 12D6<> 17C7<> 25C5<> 27D7<>
                40A6>
PCI_AD<3>       9C3< 12D6<> 17C7<> 25C6<> 27C7<>
                40A6>
PCI_AD<4>       9C3< 12D6<> 17C7<> 25C5<> 27C7<>
                40A6>
PCI_AD<5>       9C3< 12D6<> 17C7<> 25C6<> 27C7<>
                40A6>
PCI_AD<6>       9C3< 12C6<> 17C7<> 25C5<> 27C7<>
                40A6>
PCI_AD<7>       9C3< 12C6<> 17C7<> 25C6<> 27C7<>
                40D5>
PCI_AD<8>       9C3< 12C6<> 17C7<> 25C6<> 27C7<>
                40D5>
PCI_AD<9>       9C3< 12C6<> 17C7<> 25C5<> 27C7<>
                40D5>
PCI_AD<10>      9C3< 12C6<> 17C7<> 25C6<> 27C7<>
                40D5>
PCI_AD<11>      9C3< 12C6<> 17C7<> 25C5<> 27C7<>
                40D5>
PCI_AD<12>      9C3< 12C6<> 17C7<> 25C6<> 27C7<>
                40C5>
PCI_AD<13>      9C3< 12C6<> 17C7<> 25C5<> 27C7<>
                40C5>
PCI_AD<14>      9C3< 12C6<> 17C7<> 25C6<> 27C7<>
                40C5>
PCI_AD<15>      9C3< 12C6<> 17C7<> 25C5<> 27C7<>
                40C5>
PCI_AD<16>      9C3< 12C6<> 17C7<> 25C5<> 27C7<>
                40C5>
PCI_AD<17>      9C3< 12C6<> 17C7<> 25C6<> 27C7<>
                40C5>
PCI_AD<18>      9C3< 12C6<> 17B7<> 25C5<> 25D4<
                27C7<> 40C5>
PCI_AD<19>      9C3< 12C6<> 17B7<> 25C6<> 27C7<>
                40C5>
PCI_AD<20>      9B3< 12C6<> 17B7<> 25C5<> 27C7<>
                40C5>
PCI_AD<21>      12C6<> 17B7<> 25C6<> 27C7<> 40C5>
PCI_AD<22>      12C6<> 17B7<> 25C5<> 27C7<> 40B5>
PCI_AD<23>      12C6<> 17B7<> 25C6<> 27C7<> 40B5>
PCI_AD<24>      9C1<> 12C6<> 17B7<> 25C5<> 27C7<>
                40B5>
PCI_AD<25>      9C1<> 12C6<> 17B7<> 25D6<> 27C7<>
                40B5>
PCI_AD<26>      9C1<> 12C6<> 17B7<> 25C5<> 27C7<>
                40B5>
PCI_AD<27>      9C1<> 12C6<> 17B7<> 25D6<> 27C8<>
                40B5>
PCI_AD<28>      9C1<> 12C6<> 17B7<> 25D5<> 27C7<>
                40B5>
PCI_AD<29>      9C1<> 12C6<> 17B7<> 25D6<> 27B7<>
                40B5>
PCI_AD<30>      9C1<> 12C6<> 17B7<> 25D5<> 27B7<>
                40B5>
PCI_AD<31>      9C1<> 12C6<> 17B7<> 25D6<> 27B7<>
                40A5>
PCI_CBE<0>      12C7<> 17B7<> 25C5<> 27B7<> 40D4>
PCI_CBE<3..0>   3BC5>
PCI_CBE<1>      12C7<> 17B7<> 25C6<> 27B7<> 40D4>
PCI_CBE<2>      12C7<> 17B7<> 25C6<> 27B7<> 40D4>
PCI_CBE<3>      12C7<> 17B7<> 25C6<> 27B7<> 40D4>
PCI_DEVSEL_L    12B7< 12C7<> 17A7<> 25C5<> 27B7<>
                38C5> 40A5>
PCI_FRAME_L     12B7< 12C7<> 17B7<> 25C5<> 27B7<>
                38C5> 40A5>
PCI_IRDY_L      12B7< 12C7<> 17B7<> 25C6<> 27B7<>
                38C5> 40A5>
PCI_PAR         12C7<> 17B7<> 25C5<> 27B7<> 38C5>
                40D4>
PCI_STOP_L      12A7< 12C7<> 17B7<> 25C5<> 27B7<>
                38C5> 40A5>
PCI_TRDY_L      12B7< 12C7<> 17A7<> 25C5<> 27B7<>
                38C5> 40A5>
PLL_STOP_L      7C4<> 7C8<>
PMU_ACK_L       14C2< 31C4<>
PMU_AC_DET      31A5< 31B4<>
PMU_AC_IN       31B4<>
PMU_BATT0_DET_L  31B4<>
PMU_BATT1_DET_L_PU  31B4<> 31D2<
PMU_BATT_DET_L   31A8<> 31B3< 31D2< 32A4<> 40C3>
PMU_BYTE        31B6< 31C7<>
PMU_CAPSLOCK_LED_L  3IC6<>
PMU_CHARGE_V    31C4<> 32B8<>
PMU_CHRG_BATT_S  31C4<> 32A8<>
PMU_CLK         14C2<> 31C4<>
PMU_CNVSS       31B6< 31C7<
PMU_CPU_RESET_L  4A2< 6C3<> 31C4<>
PMU_CUSTOM_RESET  31A8<>
PMU_CUSTOM_RESET_L  31A7<> 31B8<
PMU_EPM         31D2< 31D4<>
PMU_FROM_INT    14C2<> 31C4<>
PMU_I2C_CLK     31B4<> 31C2<
PMU_I2C_DATA    31B4<> 31C2<
PMU_INT_L       14B5<> 14B7< 31B6<>
PMU_INT_NMI     14B5<> 14B7< 31D4<>
PMU_KB_RESET_L   40B2>
PMU_LID_CLOSED_L  23A8< 23B4<> 31B2< 31C4<>
PMU_NMI_BUTTON_L  26A1< 31C2< 31C4<>
PMU_NMI_L       31C2< 31C4<>
PMU_NUMLOCK_LED_L  31C6<>
PMU_OOPS        31B2< 31B4<>
PMU_PME_L       14B5<> 27B8< 31B2< 31C4<>
PMU_POWERUP_OK  31B4<> 31D2<
PMU_POWER_UP_L  30DB<> 31C6<> 31D7< 34B8<
PMU_RPG_L       14B7< 14C2> 31C4<>
PMU_RESET_BUTTON_L  26A2< 31C4<> 31D2<
PMU_RESET_L     31B7<>
PMU_SELECT      31C6<>
PMU_SLEEP_LED   23B4<>
PMU_SLEEP_LED_L  23B3<> 31C4<>
PMU_SMB_CLK     31B4<> 31C2< 32A3<
PMU_SMB_DATA    31B4<> 31C2< 32A2<
PMU_TO_INT      14C2<> 31C4<>
POWER_UP        30DB<>
POWER_VALID     31B2< 31C4<>
PP1V2_MMM       24C8< 24D6<
PP3V3_MMM_PIC   24C1< 24D5<
PP3V3_SI_AVCC1  20D7< 39B3>
PP3V3_SI_AVCC2  20C5< 39B3>
PP3V3_SI_PVCC1  20C7< 39B3>
PP3V3_SI_PVCC2  20C5< 39B3>
PP3V3_SI_VCC1   20D7< 39B3>
PP3V3_SI_VCC2   20C5< 39B3>
PWR_BUTTON_L    23A7<> 26C1< 40B2>
RAM_ADDR<0>     9B4< 11B5<> 11B6<>
RAM_ADDR<12..0>  37A5>
RAM_ADDR<1>     9B4< 11B3<> 11B8<>
RAM_ADDR<2>     9B4< 11B5<> 11B6<>
RAM_ADDR<3>     9B4< 11B3<> 11B8<>
RAM_ADDR<4>     9B4< 11B5<> 11B6<>
RAM_ADDR<5>     9B4< 11B3<> 11B8<>
RAM_ADDR<6>     9B4< 11B5<> 11B6<>
RAM_ADDR<7>     9B4< 11B3<> 11B8<>
RAM_ADDR<8>     9B4< 11B5<> 11B6<>
RAM_ADDR<9>     9A4< 11B3<> 11B8<>
RAM_ADDR<10>    9A4< 11B3<> 11B8<>

RAM_ADDR<11>    9A4< 11B5<> 11B6<>
RAM_ADDR<12>    9A4< 11B3<> 11B8<>
RAM_BA<0>       9A4< 11B3<> 11B8<>
RAM_BA<1..0>    37A5>
RAM_BA<1>       9A4< 11B5<> 11B6<>
RAM_CAS_L       9A4< 11B5<> 11B6<> 37A5>
RAM_CKE<0>      9A3< 9C4< 11B6<>
RAM_CKE<3..0>   37A5>
RAM_CKE<3>      9A3< 9C4< 11C3<>
RAM_CS_L<0>     9C4< 11B8<>
RAM_CS_L<3..0>  37A5>
RAM_CS_L<1>     9C4< 11B6<>
RAM_CS_L<2>     9C4< 11B3<>
RAM_CS_L<3>     9C4< 11B5<>
RAM_DATA_A<0>   10C8<> 11D8<>
RAM_DATA_A<7..0>  37C5>
RAM_DATA_A<1>   10C8<> 11D8<>
RAM_DATA_A<2>   10C8<> 11D8<>
RAM_DATA_A<3>   10B8<> 11D8<>
RAM_DATA_A<4>   10B8<> 11D6<>
RAM_DATA_A<5>   10B8<> 11D6<>
RAM_DATA_A<6>   10B8<> 11D6<>
RAM_DATA_A<7>   10B8<> 11D6<>
RAM_DATA_A<8>   10B8<> 11D8<>
RAM_DATA_A<15..8>  37C5>
RAM_DATA_A<9>   10C7<> 11D8<>
RAM_DATA_A<10>  10C7<> 11D8<>
RAM_DATA_A<11>  10C7<> 11D6<>
RAM_DATA_A<12>  10C7<> 11D6<>
RAM_DATA_A<13>  10C7<> 11D6<>
RAM_DATA_A<14>  10C7<> 11D6<>
RAM_DATA_A<15>  10C7<> 11D6<>
RAM_DATA_A<16>  10C6<> 11D8<>
RAM_DATA_A<31..16>  37B5>
RAM_DATA_A<17>  10C6<> 11C8<>
RAM_DATA_A<18>  10C6<> 11C8<>
RAM_DATA_A<19>  10B6<> 11C8<>
RAM_DATA_A<20>  10B6<> 11D6<>
RAM_DATA_A<21>  10B6<> 11C6<>
RAM_DATA_A<22>  10B6<> 11C6<>
RAM_DATA_A<23>  10B6<> 11C6<>
RAM_DATA_A<24>  10B6<> 11C8<>
RAM_DATA_A<25>  10C5<> 11C8<>
RAM_DATA_A<26>  10C5<> 11C8<>
RAM_DATA_A<27>  10C5<> 11C8<>
RAM_DATA_A<28>  10C5<> 11C6<>
RAM_DATA_A<29>  10C5<> 11C6<>
RAM_DATA_A<30>  10C5<> 11C6<>
RAM_DATA_A<31>  10C5<> 11C6<>
RAM_DATA_A<32>  10C4<> 11B8<>
RAM_DATA_A<47..32>  37B5>
RAM_DATA_A<33>  10C4<> 11B6<>
RAM_DATA_A<34>  10C4<> 11B8<>
RAM_DATA_A<35>  10C4<> 11B8<>
RAM_DATA_A<36>  10B4<> 11B6<>
RAM_DATA_A<37>  10B4<> 11B6<>
RAM_DATA_A<38>  10B4<> 11B6<>
RAM_DATA_A<39>  10B4<> 11B6<>
RAM_DATA_A<40>  10B4<> 11B8<>
RAM_DATA_A<41>  10D3<> 11B8<>
RAM_DATA_A<42>  10C3<> 11A8<>
RAM_DATA_A<43>  10C3<> 11A6<>
RAM_DATA_A<44>  10C3<> 11B6<>
RAM_DATA_A<45>  10C2<> 11A8<>
RAM_DATA_A<46>  10C3<> 11A6<>
RAM_DATA_A<47>  10C3<> 11A6<>
RAM_DATA_A<48>  10C2<> 11A8<>
RAM_DATA_A<55..48>  37B5>
RAM_DATA_A<49>  10C2<> 11A8<>
RAM_DATA_A<50>  10C2<> 11A8<>
RAM_DATA_A<51>  10C2<> 11A8<>
RAM_DATA_A<52>  10C2<> 11A6<>
RAM_DATA_A<53>  10B2<> 11A6<>
RAM_DATA_A<54>  10B2<> 11A6<>
RAM_DATA_A<55>  10B2<> 11A6<>
RAM_DATA_A<56>  10B2<> 11A8<>
RAM_DATA_A<63..56>  37A5>
RAM_DATA_A<57>  10D1<> 11A8<>
RAM_DATA_A<58>  10C1<> 11A8<>
RAM_DATA_A<59>  10C1<> 11A8<>
RAM_DATA_A<60>  10C1<> 11A6<>
RAM_DATA_A<61>  10C1<> 11A6<>
RAM_DATA_A<62>  10C1<> 11A6<>
RAM_DATA_A<63>  10C2<> 11A5<>
RAM_DQM_A<0>    10B8<> 11D6<> 37C5>
RAM_DQM_A<1>    10C7<> 11D6<> 37C5>
RAM_DQM_A<2>    10B6<> 11C6<>
RAM_DQM_A<3..2>  37B5>
RAM_DQM_A<3>    10C5<> 11C6<>
RAM_DQM_A<4>    10B4<> 11B6<>
RAM_DQM_A<5..4>  37B5>
RAM_DQM_A<5>    10C3<> 11A6<>
RAM_DQM_A<6>    10B2<> 11A6<> 37B5>
RAM_DQM_A<7>    10C1<> 11A6<> 37A5>
RAM_DQM_B<0>    10C8<> 11D5<> 37C5>
RAM_DQM_B<1>    10C8<> 11D5<> 37C5>

RAM_DQM_B<2>    10C6<> 11C5<>
RAM_DQM_B<3..2>  37B5>
RAM_DQM_B<3>    10C6<> 11C5<>
RAM_DQM_B<4>    10C4<> 11B5<>
RAM_DQM_B<5..4>  37B5>
RAM_DQM_B<5>    10C4<> 11B5<>
RAM_DQM_B<6>    10C2<> 11A5<> 37B5>
RAM_DQM_B<7>    10C2<> 11A5<> 37A5>
RAM_DQS_A<1>    10C7<> 11D8<> 37C5>
RAM_DQS_A<2>    10B6<> 11C8<>
RAM_DQS_A<3..2>  37B5>
RAM_DQS_A<3>    10C5<> 11C8<>
RAM_DQS_A<4>    10B4<> 11B8<>
RAM_DQS_A<5..4>  37B5>
RAM_DQS_A<5>    10C3<> 11A8<>
RAM_DQS_A<6>    10B2<> 11A8<> 37B5>
RAM_DQS_A<7>    10C1<> 11A8<> 37A5>
RAM_DQS_B<1>    10C8<> 11D3<> 37C5>
RAM_DQS_B<2>    10C6<> 11C3<>
RAM_DQS_B<3..2>  37B5>
RAM_DQS_B<3>    10C6<> 11C3<>
RAM_DQS_B<4>    10C4<> 11B3<>
RAM_DQS_B<5..4>  37B5>
RAM_DQS_B<5>    10C4<> 11B3<>
RAM_DQS_B<6>    10C2<> 11A3<> 37B5>
RAM_DQS_B<7>    10C2<> 11A3<> 37A5>
RAM_MUXSEL_H    10A3< 10A5< 10B1<> 10B3<> 37A5>
RAM_MUXSEL_L    10A3< 10A5< 10B5<> 10B7<> 37A5>
RAM_RAS_L       9A4< 11B5<> 11B6<> 37A5>
RAM_WE_L        9A4< 11B3<> 11B8<> 37A5>
RESET_VREF      6C3<>
RF_DISABLE_L_SPN  25D6<> 40C1>
RIGHT_USB_DM    27A3< 33A7<> 38A2> 40D1>
RIGHT_USB_DP    27A3< 33A7<> 38A2> 40D1>
RJ45_C0_PD      28B2<>
RJ45_C1_PD      28B2<>
RJ45_C2_PD      28B2<>
RJ45_C3_PD      28B2<>
RJ45_DN<0>      28B2<> 38D2> 40B3>
RJ45_DN<1>      28B2<> 38D2> 40B3>
RJ45_DN<2>      28B2<> 38D2> 40A3>
RJ45_DN<3>      28B2<> 38D2> 40A3>
RJ45_DP<0>      28B2<> 38D2> 40B3>
RJ45_DP<1>      28B2<> 38D2> 40B3>
RJ45_DP<2>      28B2<> 38D2> 40A3>
RJ45_DP<3>      28B2<> 38D2> 40A3>
ROM_CS_L        9B3< 12A5< 25B6<> 40B1>
ROM_OE_L        9B3< 12A5< 25C5<> 40B1>
ROM_ONBOARD_CS_L  9B3< 25C6<> 40B1>
ROM_RW_L        9B3< 12A5< 25C6<> 40B1>
ROM_WP_L        9B3<
RSDM1_TP        27C5>
RSDM5_TP        27C5>
RSDP1_TP        27C5>
RSDP4_TP        27C5>
RSDP5_TP        27C5>
RUN_OR_AC       30D7>
SI_I2C_CLK      19C5>< 20B5<> 20C7<>
SI_I2C_DATA     19C5>< 20B5<> 20C7<>
SI_MASTER       20B8<
SI_M_HTPLG      20B7<
SI_RESET_L      20B5< 20C7< 20D8<
SI_SECONDARY    20C8<
SI_S_HTPLG      20A5<
SI_TMDS_CLKN    20B7< 20C4<
SI_TMDS_CLKP    20B7< 20C4<
SI_TMDS_DN<0>   20B7< 20C4<
SI_TMDS_DN<1>   20B7< 20C4<
SI_TMDS_DN<2>   20B7< 20C4<
SI_TMDS_DN<3>   20A5< 20C2<
SI_TMDS_DN<4>   20A5< 20C2<
SI_TMDS_DN<5>   20A5< 20C2<
SI_TMDS_DP<0>   20B7< 20C4<
SI_TMDS_DP<1>   20B7< 20C4<
SI_TMDS_DP<2>   20B7< 20C4<
SI_TMDS_DP<3>   20A5< 20C2<
SI_TMDS_DP<4>   20A5< 20C2<
SI_TMDS_DP<5>   20A5< 20C2<
SI_VREF         20A8< 20B8<
SLEEP           23C4<> 31B6<> 31D7< 34A4< 34A6<
                34B3< 34B8<> 36B3< 36D2< 40A1>
SLEEP_ANODE     23C2< 26C5>
SLEEP_LED       40B6>
SLEEP_LED_I     23C2<
SLEEP_LED_L     23C2<
SLEEP_LED_SW_L  23C3<>
SLEEP_LED_UF    23C2<
SLEEP_LS5       34A5<> 34A8<
SLEEP_LS5_EN_L  34A5<>
SLEEP_L_LS5     19A7<> 28A8<> 34A5<> 35C8<> 36C8<
SLEEP_L_LS5_EN_L  34A6<>
SLEEP_L_LS5_INV  36A3< 36C2< 36C8<>
SLEEP_L_LS5_NET  34B3<> 36C8<>
SLEEP_NET       34A3<>
SLEEP_NET_INV   34A3<>
SMC_TP          27B5<
SND_AGND        26C6<> 39B6>
SND_AMP_MUTE    26D4< 26D4<> 40A4>
SND_AMP_MUTE_INV  26C8< 26D4<
SND_AMP_MUTE_L  14C5<> 26D3<>
SND_CLKOUT      14B1< 26C8< 37B1> 40D6>
SND_HP_MUTE     26C4<>
SND_HP_MUTE_INV  40A4>
SND_HP_MUTE_L   14C5<> 26C4<>
SND_HP_SENSE_L  40C6>
SND_HW_RESET_L  14A7< 14B5<> 26B8< 40C6>
SND_LIN_SENSE_L  40C6>
SND_SCLK        14B1< 26B8< 37B1> 40C6>
SND_SYNC        14B1< 26C8< 40D6>
SND_TO_AUDIO    14B1< 26C8< 40D6>
SOFT_PWR_ON_L   22D1< 23A8< 31A8<> 31C6<> 31D7<
                35A3<>
SOUND_SPDIF_GPO0  14C5< 26D8<
SPDIF_GPO0      26D7<> 26D7<
SRCLK_TP        27A5> 40A4>
SRNOD_TP        27A5< 40A4>
ST7_ICP_SEL_PD  23A2< 23C6<
ST7_KBD_LED_OUT  23A5<> 23C4<>
ST7_OSC1        23C6<
ST7_OSC2        23C6<>
ST7_PB6_PD      23A2< 23C4<>
ST7_RESET_L     23C6<>
ST7_SENSOR4_SCK_PD  23B2< 23C4<>
ST7_SENSOR4_SDA_PD  23B2< 23C4<>
ST7_SENSOR5_SCK  23B2< 23C4<>
ST7_SENSOR5_SDA  23B3< 23C4<>
ST7_SLEEP_LED_H  23B4<> 23C4<>
ST7_XTAL_IN     23C6< 31B3<>
STOP_AGP_L      12D2< 12D4<>
SUPPLY_M_DP     26A8< 26B6<
SUPPLY_M_DP     26A8< 26B6<
SUTRO_ALS_GAIN_SW  23C4<> 25B2<> 40C2>
SUTRO_ALS_OUT   23B4<> 25B2<> 40C2>
SYSCLK_CPU      5C4< 8A6< 37D1>
SYSCLK_CPU_UF   8A6<> 37D1>
SYSCLK_DDRCLK_A0  9D4< 11D8<> 37D1>
SYSCLK_DDRCLK_A0_L  9D4< 11D8<> 37D1>
SYSCLK_DDRCLK_A0_L_UF  9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_A0_UF  9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_A1  9D4< 11A6<> 37D1>
SYSCLK_DDRCLK_A1_L  9D4< 11A6<> 37D1>
SYSCLK_DDRCLK_A1_L_UF  9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_A1_UF  9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_B0  9D4< 11D3<> 37D1>
SYSCLK_DDRCLK_B0_L  9C4< 11D3<> 37C1>
SYSCLK_DDRCLK_B0_L_UF  9B6<> 9C5< 37D1>
SYSCLK_DDRCLK_B0_UF  9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_B1  9D4< 11A5<> 37C1>
SYSCLK_DDRCLK_B1_L  9D4< 11A5<> 37C1>
SYSCLK_DDRCLK_B1_L_UF  9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_B1_UF  9B6<> 9D5< 37D1>
SYSCLK_LA_TP    8A6<>
SYSTEM_CLK_EN   14A5< 14A7< 31C4<>
SYS_BATT_ISNS   24A2< 31C2<
SYS_BATT_ISNS1  31B4<> 31C3<
SYS_BATT_ISNS2  31B4<> 31C3<
TEB_TP          27A5< 40A4>
TEST_TP         27A5< 40A4>
THERM1_A_DM     26A6< 26A8< 38A2>
THERM1_A_DP     26A6< 26A8< 38A2>
THERM1_DM       26A5< 26A5< 26B5<> 26B5< 38A2>
THERM1_DP       26A5< 26A5< 26B5<> 26B5< 38A2>
THERM1_M_DM     38A2>
THERM1_M_DP     38A2>

THERM2_A_DM     26A6< 26A7< 38A2>
THERM2_A_DP     26A6< 26A7< 38A2>
THERM2_DM       26A5< 26B5<> 26B5< 38A2>
THERM2_DP       26A5< 26B5<> 26B5< 38A2>
THERM2_M_DM     38A2>
THERM2_M_DP     38A2>
THERM_INV       26B2<>
THERM_L_OC      26B1<> 31B4<>
THERM_L_OC_CONN  23A7<>
TMDS_CLKN       20B2< 20C3< 20D4< 22B7<> 38B2>
TMDS_CLKP       20B3< 20C3< 20D4< 22C7<> 38B2>
TMDS_CLK_CMP    20B3<
TMDS_CONN_CLKN  22B6<> 22C7<> 38B2> 40A8>
TMDS_CONN_CLKP  22C6<> 22C7<> 38B2> 40D7>
TMDS_CONN_DN<0>  22C7<> 22D6<>
TMDS_CONN_DN<1>  22B7<> 22D5<>
TMDS_CONN_DN<2>  22B6<> 22D5<>
TMDS_CONN_DN<3>  20D1<> 22C5<>
TMDS_CONN_DN<4>  20D1<> 22C5<>
TMDS_CONN_DN<5>  20D1<> 22C7<>
TMDS_CONN_DP<0>  22B7<> 22D6<>
TMDS_CONN_DP<1>  22B7<> 22D5<>
TMDS_CONN_DP<2>  22B6<> 22D5<>
TMDS_CONN_DP<3>  20D1<> 22C5<>
TMDS_CONN_DP<4>  20D1<> 22C5<>
TMDS_CONN_DP<5>  20D1<> 22C7<>
TMDS_D0_CMF     20B3<
TMDS_D1_CMF     20A3<
TMDS_D2_CMF     20A3<
TMDS_D3_CMF     20B2<
TMDS_D4_CMF     20B1<
TMDS_D5_CMF     20A1<
TMDS_DN<0>      20B2< 20C3< 20D4< 22C8<> 38B2>
                40B8>
TMDS_DN<1>      20A2< 20C3< 20D2< 22B8<> 38B2>
                40A8>
TMDS_DN<2>      20A2< 20C3< 20D2< 22B7<> 38B2>
                40A8>
TMDS_DN<3>      20B1< 20C1< 20D2<>
TMDS_DN<4>      20B1< 20C1< 20D2<>
TMDS_DN<5>      20A1< 20C1< 20D2<>
TMDS_DP<0>      20B3< 20C3< 20D4< 22B8<> 38B2>
                40A8>
TMDS_DP<1>      20A3< 20C3< 20D2< 22B8<> 38B2>
                40A8>
TMDS_DP<2>      20A3< 20C3< 20D2< 22B7<> 38B2>
                40A8>
TMDS_DP<3>      20B2< 20C1< 20D2<>
TMDS_DP<4>      20B2< 20C1< 20D2<>
TMDS_DP<5>      20A2< 20C1< 20D2<>
TMDS_MASTER     20B8<
TMDS_SYNC       20A7< 20B8<
TPAD_F_RXD      40C4>
TPAD_F_TXD      40C4>
TPAD_RXD        31C2< 31C4<>
TPAD_TXD        31B2< 31C4<>
TPS22111_SHDN_L_PU  17C4<
TP_B8_XTAL      6C3<>
TP_MMM_ICSP_PGC  24C3<>
TP_MMM_ICSP_PGD  24C3<>
TP_MMM_ICSP_PGM  24C3<>
TV_C            22A6<> 40D6>
TV_COMP         22A6<> 40D6>
TV_GND1         22B6<> 39B6> 40A7>
TV_GND2         22A6<> 39B6> 40A7>
TV_Y            22A6<> 40D6>
UIDE_ADDR<0>    13D7<> 25C4<
UIDE_ADDR<2..0>  38C5>
UIDE_ADDR<1>    13D7<> 25C4<
UIDE_ADDR<2>    13D7<> 25B4<
UIDE_CS0_L      13C7<> 25C4< 38C5>
UIDE_CS1_L      13C7<> 25B4< 38C5>
UIDE_DATA<0>    13D7<> 25D4<
UIDE_DATA<6..0>  38C5>
UIDE_DATA<1>    13D7<> 25D4<
UIDE_DATA<2>    13D7<> 25D4<
UIDE_DATA<3>    13D7<> 25D4<
UIDE_DATA<4>    13D7<> 25C4<
UIDE_DATA<5>    13D7<> 25C4<
UIDE_DATA<6>    13D7<> 25C4<
UIDE_DATA<7>    13D7<> 25C4< 38C5>
UIDE_DATA<8>    13D7<> 25C4<
UIDE_DATA<15..8>  38C5>
UIDE_DATA<9>    13D7<> 25C4<
UIDE_DATA<10>   13D7<> 25C4<
UIDE_DATA<11>   13D7<> 25D4<
UIDE_DATA<12>   13D7<> 25B4<
UIDE_DATA<13>   13D7<> 25B4<
UIDE_DATA<14>   13D7<> 25C4<
UIDE_DATA<15>   13D7<> 25B4<
UIDE_DIOR_L     13C7<> 25A4< 38C5>
UIDE_DIOW_L     13C7<> 25A4< 38C5>
UIDE_DMACK_L    13C7<> 25A4< 38C5>
UIDE_DMARQ      13C7<> 38C5>
UIDE_INTRQ      13C7< 38C5>
UIDE_IOCHRDY    13C7< 25A4< 38C5>
UIDE_RST        13C7<> 39D3>
UIDE_RST_L      13C7<> 25A4< 38C5>
USB2_PCI_GNT_L  12C7<> 27B7<
USB2_PCI_INT_L  14B5<> 14C7< 27A8<
USB2_PCI_REQ_L  12A7< 12D7<> 27B7>
USB_D1M         14D1< 27A5> 27B4<
USB_D1P         14D1< 27A4< 27A5>
USB_D2M         27A5>
USB_D2P         27A5>
USB_DAM         14B2<> 14D2< 27A5>
USB_DAP         14B2<> 14D2< 27A5>
USB_DBM         14B2<> 14D1<
USB_DBP         14B2<> 14D1<
USB_DCM         14B2<> 14D2< 27A5>
USB_DCP         14B2<> 14D2< 27A5>
USB_DDM         14B2<> 14C2<
USB_DDP         14B2<> 14C2<
USB_DEM         14B2<> 14C2< 38B2>
USB_DEP         14B2<> 14C2< 38B2>
USB_DFM         14B2<> 14B2< 38B2>
USB_DFP         14B2< 14B2<> 38B2>
USB_OC_AB_L     14B2< 14C7<
USB_OC_CD_L     14B2< 14C7<
USB_OC_EF_L     14B2< 14D7<
USB_PWREN_AB_L  14B2<> 14C7<
USB_PWREN_CD_L  14B2<> 14C7<
USB_PWREN_EF_L  14B2<> 14D7<
USB_TPAD_N      14B1< 23A7<>
USB_TPAD_P      14B1< 23A7<>
VCORE_BOOST     35C4<> 39C1>
VCORE_BST       35C5<> 39C1>
VCORE_CC        35B6<> 39B1>
VCORE_CNTL_RC   19A3<>
VCORE_DH        35B5<> 39C1>
VCORE_DL        35B5<> 39C1>
VCORE_FAST<1>   35D3< 35D5<
VCORE_FAST<2>   35D3< 35D5<
VCORE_FAST<3>   35D3< 35D5<
VCORE_FAST<4>   35D3< 35D5<
VCORE_FB        35B5< 39B1> 40A2>
VCORE_GND       35B5<> 39B1>
VCORE_GNDA      35B6<>
VCORE_GNDDIV    35A4< 35B5< 39B1>
VCORE_GNDDIV_TEST  35A3<>
VCORE_GNDSNS    35A2<> 35A4< 39B1>
VCORE_GNDSNS_TEST  35A3<>
VCORE_ILIM      35C6<> 39C1>
VCORE_LX        35B5<> 39C1>
VCORE_MUX_EN    35D5<> 40A2>
VCORE_MUX_SEL   35D5<>
VCORE_REF       35B6<> 39C1>
VCORE_SEL_OFF_PU  35B6<>
VCORE_SEL_ON    35B6<>
VCORE_SHDN_L    5B3<> 35C6<>
VCORE_SLOW<1>   35D6<
VCORE_SLOW<2>   35D6<
VCORE_SLOW<3>   35D6<
VCORE_SLOW<4>   35D6<
VCORE_SNS       35A1<> 39B1>
VCORE_TIME      35B4<> 39B1>
VCORE_TON       35B6< 39C1>
VCORE_VCC       35C6< 39C1>
VCORE_VGATE     14B6< 14B7< 35B4> 39B1>
VCORE_VID0      40A3>
VCORE_VID1      40A3>
VCORE_VID2      40A3>
VCORE_VID3      40A3>
VCORE_VID4      40A3>
VCORE_VID<0>    35A2<> 35B8<
VCORE_VID<1>    35A2<> 35B8< 35D4<>
VCORE_VID<2>    35A2<> 35B8< 35D4<>
VCORE_VID<3>    35A2<> 35B8< 35D4<>

VCORE_VID<4>    35A2<> 35B8< 35D4<>
VGA_B           22C6<> 22D7< 40D7>
VGA_G           22C5<> 22D7< 40D7>
VGA_HSYNC       22C6<> 22C7< 40D7>
VGA_HSYNC_BUF   22C8<>
VGA_R           22C5<> 22D7< 40D7>
VGA_VSYNC       22C5<> 22C7< 40D7>
VGA_VSYNC_BUF   22C8<>
```

C

B

A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE: NONE	SHT 43 OF 45	

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*** Part Cross-Reference for the entire design ***

BS1   PCB_STANDOFF 4
C1    CAP    22
C2    CAP    35
C3    CAP    35
C4    CAP    35
C5    CAP    35
C6    CAP    35
C7    CAP    35
C8    CAP    5
C9    CAP    16
C10   CAP    16
C11   CAP    18
C12   CAP    5
C13   CAP    35
C14   CAP    23
C15   CAP    14
C16   CAP    16
C17   CAP    16
C18   CAP    16
C19   CAP    16
C20   CAP    16
C21   CAP    16
C22   CAP    16
C23   CAP    16
C24   CAP    16
C25   CAP    5
C26   CAP    16
C27   CAP    16
C28   CAP    16
C29   CAP    16
C30   CAP    16
C31   CAP    16
C32   CAP    16
C33   CAP    16
C34   CAP    16
C35   CAP    16
C36   CAP    16
C37   CAP    18
C38   CAP    5
C39   CAP    5
C40   CAP    5
C41   CAP    5
C42   CAP    16
C43   CAP    16
C44   CAP    16
C45   CAP    16
C46   CAP    5
C47   CAP    5
C48   CAP    5
C49   CAP    16
C50   CAP    16
C51   CAP    16
C52   CAP    16
C53   CAP    16
C54   CAP    16
C55   CAP    16
C56   CAP    16
C57   CAP    16
C58   CAP    16
C59   CAP    16
C60   CAP    16
C61   CAP    16
C62   CAP    18
C63   CAP    18
C64   CAP    18
C65   CAP    18
C66   CAP    18
C67   CAP    18
C68   CAP    18
C69   CAP    18
C70   CAP    18
C71   CAP    18
C72   CAP    5
C73   CAP    5
C74   CAP    5
C75   CAP    16
C76   CAP    16
C77   CAP    18
C78   CAP    18
C79   CAP    23
C80   CAP    23
C81   CAP    26
C82   CAP    26
C83   CAP    12
C84   CAP    14
C85   CAP    14
C86   CAP    25
C87   CAP    26
C88   CAP    26
C89   CAP    20
C90   CAP    5
C91   CAP    5
C92   CAP    5
C93   CAP    36
C94   CAP    16
C95   CAP    16
C96   CAP    16
C97   CAP    14
C98   CAP    16
C99   CAP    16
C100  CAP    16
C101  CAP    16
C102  CAP    20
C103  CAP    5
C104  CAP    5
C105  CAP    5
C106  CAP    5
C107  CAP    5
C108  CAP    16
C109  CAP    16
C110  CAP    5
C111  CAP    5
C112  CAP    5
C113  CAP    5
C114  CAP    5
C115  CAP    5
C116  CAP    35
C117  CAP    16
C118  CAP    16
C119  CAP    16
C120  CAP    16
C121  CAP    16
C122  CAP    16
C123  CAP    16
C124  CAP    16
C125  CAP    16
C126  CAP    16
C127  CAP    16
C128  CAP    16
C129  CAP    20
C130  CAP    20
C131  CAP    20
C132  CAP    20
C133  CAP    20
C134  CAP    26
C135  CAP    26
C136  CAP    5
C137  CAP    5
C138  CAP    5
C139  CAP    5
C140  CAP    14
C141  CAP    16
C142  CAP    16
C143  CAP    16
C144  CAP    16
C145  CAP    16
C146  CAP    16
C147  CAP    16
C148  CAP    14
C149  CAP    5
C150  CAP    5
C151  CAP    5
C152  CAP    5
C153  CAP    5
C154  CAP    5
C155  CAP    5
C156  CAP    5
C157  CAP    16
C158  CAP    16
C159  CAP    16
C160  CAP    12
C161  CAP    16
C162  CAP    16
C163  CAP    16
C164  CAP    16
C165  CAP    20
C166  CAP    19
C167  CAP    19
C168  CAP    5
C169  CAP    5
C170  CAP    5
C171  CAP    16
C172  CAP    16
C173  CAP    16
C174  CAP    16
C175  CAP    16
C176  CAP    16
C177  CAP    16
C178  CAP    16
C179  CAP    16
C180  CAP    16
C181  CAP    16
C182  CAP    14
C183  CAP    16
C184  CAP    16
C185  CAP    16
C186  CAP    19
C187  CAP    19
C188  CAP    5
C189  CAP    5
C190  CAP    5
C191  CAP    5
C192  CAP    5
C193  CAP    5
C194  CAP    5
C195  CAP    5
C196  CAP    16
C197  CAP    16
C198  CAP    14
C199  CAP    16
C200  CAP    14
C201  CAP    5
C202  CAP    5
C203  CAP    5
C204  CAP    16
C205  CAP    16
C206  CAP    16
C207  CAP    16
C208  CAP    16
C209  CAP    16
C210  CAP    16
C211  CAP    16
C212  CAP    16
C213  CAP    16
C214  CAP    16
C215  CAP    16
C216  CAP    16
C217  CAP    16
C218  CAP    20
C219  CAP    19
C220  CAP    20
C221  CAP    19
C222  CAP    19
C223  CAP    5
C224  CAP    5
C225  CAP    5
C226  CAP    16
C227  CAP    16
C228  CAP    16
C229  CAP    16
C230  CAP    16
C231  CAP    16
C232  CAP    19
C233  CAP    20
C234  CAP    35
C235  CAP    36
C236  CAP    16
C237  CAP    16
C238  CAP    16
C239  CAP    16
C240  CAP    16
C241  CAP    16
C242  CAP    16
C243  CAP    16
C244  CAP    16
C245  CAP    9
C246  CAP    16
C247  CAP    12
C248  CAP    16
C249  CAP    16
C250  CAP    16
C251  CAP    16
C252  CAP    19
C253  CAP    19
C254  CAP    19
C255  CAP    20
C256  CAP    19
C257  CAP    5
C258  CAP    5
C259  CAP    16
C260  CAP    16
C261  CAP    16
C262  CAP    16
C263  CAP    16
C264  CAP    16
C265  CAP    16
C266  CAP    16
C267  CAP    16
C268  CAP    19
C269  CAP    19
C270  CAP    19
C271  CAP    19
C272  CAP    5
C273  CAP    5
C274  CAP    35
C275  CAP    5
C276  CAP    36
C277  CAP    16
C278  CAP    16
C279  CAP    16
C280  CAP    16
C281  CAP    16
C282  CAP    19
C283  CAP    5
C284  CAP    20
C285  CAP    35
C286  CAP    16
C287  CAP    16
C288  CAP    16
C289  CAP    16
C290  CAP    16
C291  CAP    16
C292  CAP    16
C293  CAP    16
C294  CAP    16
C295  CAP    16
C296  CAP    16
C297  CAP    16
C298  CAP    16
C299  CAP    19
C300  CAP    19
C301  CAP    19
C302  CAP    19
C303  CAP    19
C304  CAP    21
C305  CAP    19
C306  CAP    19
C307  CAP    19
C308  CAP    8
C309  CAP    16
C310  CAP    16
C311  CAP    19
C312  CAP    16
C313  CAP    16
C314  CAP    16
C315  CAP    16
C316  CAP    16
C317  CAP    16
C318  CAP    16
C319  CAP    16
C320  CAP    16
C321  CAP    16
C322  CAP    16
C323  CAP    16
C324  CAP    16
C325  CAP    16
C326  CAP    19
C327  CAP    21
C328  CAP    19
C329  CAP    19
C330  CAP    19
C331  CAP    19
C332  CAP    19
C333  CAP    19
C334  CAP    16
C335  CAP    16
C336  CAP    16
C337  CAP    16
C338  CAP    19
C339  CAP    21
C340  CAP    5
C341  CAP    5
C342  CAP    5
C343  CAP    5
C344  CAP    5
C345  CAP    5
C346  CAP    5
C347  CAP    5
C348  CAP    16
C349  CAP    16
C350  CAP    16
C351  CAP    16
C352  CAP    16
C353  CAP    14
C354  CAP    16
C355  CAP    16
C356  CAP    16
C357  CAP    16
C358  CAP    21
C359  CAP    21
C360  CAP    21
C361  CAP    21
C362  CAP    21
C363  CAP    21
C364  CAP    21
C365  CAP    16
C366  CAP    16
C367  CAP    16
C368  CAP    16
C369  CAP    16
C370  CAP    16
C371  CAP    16
C372  CAP    21
C373  CAP    21
C374  CAP    21
C375  CAP    16
C376  CAP    16
C377  CAP    16
C378  CAP    16
C379  CAP    21
C380  CAP    21
C381  CAP    21
C382  CAP    21
C383  CAP    21
C384  CAP    16
C385  CAP    16
C386  CAP    16
C387  CAP    16
C388  CAP    16
C389  CAP    16
C390  CAP    16
C391  CAP    16
C392  CAP    16
C393  CAP    16
C394  CAP    16
C395  CAP    16
C396  CAP    16
C397  CAP    16
C398  CAP    16
C399  CAP    16
C400  CAP    16
C401  CAP    16
C402  CAP    16
C403  CAP    16
C404  CAP    16
C405  CAP    16
C406  CAP    16
C407  CAP    16
C408  CAP    21
C409  CAP    21
C410  CAP    16
C411  CAP    21
C412  CAP    21
C413  CAP    21
C414  CAP    21
C415  CAP    21
C416  CAP    22
C417  CAP    16
C418  CAP    16
C419  CAP    14
C420  CAP    21
C421  CAP    21
C422  CAP    16
C423  CAP    16
C424  CAP    14
C425  CAP    21
C426  CAP    21
C427  CAP_P  35
C428  CAP    21
C429  CAP    21
C430  CAP_P  35
C431  CAP_P  35
C432  CAP_P  35
C433  CAP    14
C434  CAP    21
C435  CAP    21
C436  CAP    21
C437  CAP    21
C438  CAP    21
C439  CAP    35
C440  CAP    22
C441  CAP_P  35
C442  CAP    28
C443  CAP_P  35
C444  CAP_P  35
C445  CAP_P  35
C446  CAP    21
C447  CAP    21
C448  CAP    19
C449  CAP    22
C450  CAP    21
C451  CAP    19
C452  CAP    22
C453  CAP    28
C454  CAP    28
C455  CAP    35
C456  CAP    34
C457  CAP    28
C458  CAP    32
C459  CAP    35
C460  CAP    9
C461  CAP    33
C462  CAP    33
C463  CAP    33
C464  CAP    28
C465  CAP    28
C466  CAP    28
C467  CAP    17
C468  CAP    32
C469  CAP    26
C470  CAP    9
C471  CAP    28
C472  CAP    28
C473  CAP    19
C474  CAP    22
C475  CAP    28
C476  CAP    28
C477  CAP    28
C478  CAP    26
C479  CAP    9
C480  CAP    16
C481  CAP    11
C482  CAP    11
C483  CAP    19
C484  CAP    22
C485  CAP    33
C486  CAP    28
C487  CAP    28
C488  CAP    28
C489  CAP    11
C490  CAP    11
C491  CAP    28
C492  CAP    28
C493  CAP    28
C494  CAP    19
C495  CAP    33
C496  CAP    28
C497  CAP    28
C498  CAP    35
C499  CAP    36
C500  CAP    22
C501  CAP    28
C502  CAP    28
C503  CAP    28
C504  CAP    28
C505  CAP    28
C506  CAP    28
C507  CAP    35
C508  CAP    34
C509  CAP    33
C510  CAP    33
C511  CAP    28
C512  CAP    35
C513  CAP    26
C514  CAP    19
C515  CAP    19
C516  CAP    34
C517  CAP    28
C518  CAP    35
C519  CAP    36
C520  CAP    28
C521  CAP    35
C522  CAP    11
C523  CAP    11
C524  CAP    11
C525  CAP    11
C526  CAP    11
C527  CAP    11
C528  CAP    30
C529  CAP    35
C530  CAP    11
C531  CAP    36
C532  CAP    34
C533  CAP    34
C534  CAP    34
C535  CAP    33
C536  CAP    33
C537  CAP    33
C538  CAP    29
C539  CAP    29
C540  CAP    29
C541  CAP    29
C542  CAP    11
C543  CAP    21
C544  CAP    36
C545  CAP    34
C546  CAP    29
C547  CAP    32
C548  CAP    11
C549  CAP    11
C550  CAP    11
C551  CAP    11
C552  CAP    22
C553  CAP    33
C554  CAP    33
C555  CAP    28
C556  CAP    30
C557  CAP    32
C558  CAP    31
C559  CAP    36
C560  CAP    34
C561  CAP    29
C562  CAP    32
C563  CAP    32
C564  CAP    32
C565  CAP    11
C566  CAP    34
C567  CAP    34
C568  CAP    33
C569  CAP    33
C570  CAP    29
C571  CAP    29
C572  CAP    32
C573  CAP    11
C574  CAP    31
C575  CAP    36
C576  CAP    34
C577  CAP    29
C578  CAP    32
C579  CAP    32
C580  CAP    36
C581  CAP    36
C582  CAP    36
C583  CAP    34
C584  CAP    33
C585  CAP    33
C586  CAP    29
C587  CAP    29
C588  CAP    30
C589  CAP    11
C590  CAP    34
C591  CAP    29
C592  CAP    32
C593  CAP    32
C594  CAP    11
C595  CAP    11
C596  CAP    11
C597  CAP    11
C598  CAP    34
C599  CAP    33
C600  CAP    32
C601  CAP    11
C602  CAP    11
C603  CAP    36
C604  CAP    33
C605  CAP    29
C606  CAP    30
C607  CAP    30
C608  CAP    32
C609  CAP    34
C610  CAP    34
C611  CAP    34
C612  CAP    34
C613  CAP    33
C614  CAP    29
C615  CAP    32
C616  CAP    32
C617  CAP    32
C618  CAP    32
C619  CAP    32
C620  CAP    34
C621  CAP    32
C622  CAP    32
C623  CAP    34
C624  CAP    32
C625  CAP    33
C626  CAP    33
C627  CAP    29
C628  CAP    29
C629  CAP    29
C630  CAP    32
C631  CAP    32
C632  CAP    32
C633  CAP    32
C634  CAP    29
C635  CAP    29
C636  CAP    23
C637  CAP    23
C638  CAP    6
C639  CAP    34
C640  CAP    29
C641  CAP    29
C642  CAP    29
C643  CAP    31
C644  CAP    33
C645  CAP    29
C646  CAP    29
C647  CAP    21
C648  CAP    23
C649  CAP    27
C650  CAP    29
C651  CAP    26
C652  CAP    32
C653  CAP    29
C654  CAP    23
C655  CAP    23
C656  CAP    20
C657  CAP    27
C658  CAP    32
C659  CAP    34
C660  CAP    20
C661  CAP    27
C662  CAP    34
C663  CAP    23
C664  CAP    31
C665  CAP    27
C666  CAP    31
C667  CAP    27
C668  CAP    26
C669  CAP    22
C670  CAP    23
C671  CAP    21
C672  CAP    21
C673  CAP    23
C674  CAP    35
C675  CAP    23
C676  CAP    22
C677  CAP    36
C678  CAP    26
C679  CAP    35
C680  CAP    35
C681  CAP    26
C682  CAP    35
C683  CAP    36
C684  CAP    22
C685  CAP    22
C686  CAP    14
C687  CAP    35
C688  CAP    26
C689  CAP    35
C690  CAP    26
C691  CAP    14
C692  CAP    14
C693  CAP    35
C694  CAP_P  34
C695  CAP    35
C696  CAP    22
C697  CAP    34
C698  CAP    14
C699  CAP    35
C700  CAP    34
C701  CAP    21
C702  CAP    22
C703  CAP    22
C704  CAP    21
C705  CAP    36
C706  CAP    22
C707  CAP    22
C708  CAP    19
C709  CAP    36
C710  CAP    22
C711  CAP    26
C712  CAP    22
C713  CAP    22
C714  CAP    22
C715  CAP    21
C716  CAP    21
C717  CAP    22
C718  CAP    22
C719  CAP_P  19
C720  CAP_P  19
C721  CAP_P  19
C722  CAP    21
C723  CAP    36
C724  CAP    22
C725  CAP    21
C726  CAP    36
C727  CAP    10
C728  CAP_P  35
C729  CAP_P  35
C730  CAP_P  35
C731  CAP_P  35
C732  CAP_P  35
C733  CAP_P  35
C734  CAP_P  35
C735  CAP    10
C736  CAP    10
C737  CAP    10
C738  CAP    10
C739  CAP    22
C740  CAP    36
C741  CAP    10
C742  CAP    10
C743  CAP    10
C744  CAP    22
C745  CAP_P  36
C746  CAP    22
C747  CAP    10
C748  CAP    10
C749  CAP    22
C750  CAP_P  33
C751  CAP_P  36
C752  CAP    10
C753  CAP    10
C754  CAP    28
C755  CAP    28
C756  CAP_P  34
C757  CAP    32
C758  CAP_P  33
C759  CAP    34
C760  CAP    34
C761  CAP    11
C762  CAP    19
C763  CAP    34
C764  CAP    35
C765  CAP_P  33
C766  CAP    19
C767  CAP    26
C768  CAP    35
C769  CAP_P  33
C770  CAP    34
C771  CAP    32
C772  CAP    32
C773  CAP    17
C774  CAP    30
C775  CAP    32
C776  CAP    17
C777  CAP    29
C778  CAP    29
C779  CAP    34
C780  CAP_P  36
C781  CAP    30
C782  CAP_P  36
C783  CAP    17
C784  CAP    30
C785  CAP    34
C786  CAP    30
C787  CAP    33
C788  CAP_P  36
C789  CAP    17
C790  CAP    17
C791  CAP    17
C792  CAP    30
C793  CAP_P  33
C794  CAP_P  33
C795  CAP    17
C796  CAP    17
C797  CAP    17
C798  CAP    17
C799  CAP_P  33
C800  CAP    34
C801  CAP    33
C802  CAP    32
C803  CAP    30
C804  CAP    29
C805  CAP    30
C806  CAP    34
C807  CAP    30
C808  CAP    29
C809  CAP    36
C810  CAP    29
C811  CAP    34
C812  CAP    20
C813  CAP    17
C814  CAP    23
C815  CAP    23
C816  CAP    23
C817  CAP    32
C818  CAP_P  29
C819  CAP_P  33
C820  CAP_P  33
C821  CAP_P  33
C822  CAP_P  33
C823  CAP_P  34
C824  CAP_P  32
C825  CAP_P  34
C826  CAP    34
C827  CAP    31
C828  CAP    23
C829  CAP    27
C830  CAP    27
C831  CAP    31
C832  CAP    31
C833  CAP    27
C834  CAP    27
C835  CAP    31
C836  CAP    27
C837  CAP    27
C838  CAP    27
C839  CAP    27
C840  CAP    27
C841  CAP    27
C842  CAP    27
C843  CAP    27
C844  CAP    27
C845  CAP    27
C846  CAP    26
C847  CAP    21
C848  CAP    21
C849  CAP    21
C850  CAP    21
C851  CAP    21
C852  CAP    21
C853  CAP    21
C854  CAP    21
C855  CAP    21
C856  CAP    21
C857  CAP    21
C858  CAP    21
C859  CAP    21
C860  CAP    21
C861  CAP    21
C862  CAP    21
C863  CAP    21
C864  CAP    21
C865  CAP    21
C866  CAP    21
C867  CAP    21
C868  CAP    21
C869  CAP    21
C870  CAP    21
C871  CAP    21
C872  CAP    21
C873  CAP    21
C874  CAP    21
C875  CAP    21
C876  CAP    21
C877  CAP    21
C878  CAP    21
C879  CAP    21
C880  CAP    21
C881  CAP    21
C882  CAP    19
C883  CAP    32
C884  CAP_P  35
C885  CAP_P  35
C886  CAP    36
C887  CAP    36
C888  CAP    36
C889  CAP    21
C890  CAP    36
C891  CAP    36
C892  CAP    36
C893  CAP    36
C894  CAP    36
C895  CAP    26
C896  CAP    26
C897  CAP    26
C898  CAP    26
C899  CAP    26
C900  CAP    26
C901  CAP    26
C902  CAP    19
C903  CAP    26
C904  CAP    26
C905  CAP    26
C906  CAP    32
C907  CAP    36
C908  CAP    36
C909  CAP    5
C910  CAP    21
C911  CAP    21
C912  CAP    21
C913  CAP    19
C914  CAP    23
C915  CAP    31
C916  CAP    20
C917  CAP    24
C918  CAP    24
C919  CAP    24
C920  CAP    20
C921  CAP    24
C922  CAP    20
C923  CAP    24
C924  CAP    20
C925  CAP    24
C926  CAP    24
C927  CAP    24
C928  CAP    20
C929  CAP    23
C930  CAP    20
C931  CAP    20
C932  CAP    20
C933  CAP    20
C934  CAP    20
C935  CAP    30
C936  CAP    24
C937  CAP    24
C938  CAP    6
C939  CAP    20
C940  CAP    20
C941  CAP    20
C942  CAP    30
C943  CAP    30
C944  CAP    30
C945  CAP    5
C946  CAP    5
D1    DIODE       28
D2    DIODE_SCHOT 35
D3    DIODE_SCHOT 33
D4    DIODE       33
D5    DIODE_SCHOT 19
D6    DIODE_SCHOT 34
D7    DIODE_SCHOT 33
D8    ZENER       30
D9    DIODE       32
D10   DIODE       32
D11   DIODE_SCHOT 33
D12   DIODE_DUAL_6P 30
D13   DIODE_SCHOT 34
D14   DIODE_SCHOT_3P2 29
D15   DIODE_DUAL_6P 30
D16   DIODE       34
D17   DIODE_SCHOT 33
D18   DIODE       33
D19   DIODE_SCHOT 33
D20   DIODE_SCHOT 29
D21   DIODE_SCHOT 22
D22   DIODE_SCHOT 34
D23   DIODE_SCHOT 36
D24   DIODE_SCHOT 19
D25   DIODE       35
D26   DIODE_DUAL_6P 30
D27   DIODE_SCHOT 33
D28   DIODE_DUAL_6P 30
D29   DIODE_SCHOT 30
D30   DIODE_SCHOT 32
D31   DIODE_SCHOT 30
D32   DIODE       20
D33   DIODE_SCHOT 36
D34   DIODE_SCHOT 34
D35   DIODE_SCHOT 5
DP1   DPAK3P      19
DP2   DPAK3P      35
DP3   DPAK3P      36
DP4   DPAK3P      32
DP5   DPAK3P      30
DP6   DPAK3P      19
DP7   DPAK3P      21
DP8   DPAK3P      31
F1    FUSE        22
F2    FUSE        30
F3    FUSE        32
F4    FUSE        32
F5    FUSE        30
FL1   FILTER_LC 22
FL2   FILTER_LC 22
FL3   FILTER_LC 22
G1    OSC         29
G2    OSC         18
J1    CON_F1ST_S2MT_SM 14
J2    CON_4RT_WRIB 26
J3    CON_F14RT_S2MT_SM 25
J4    CON_4RT_WRIB 26
J5    CON_12      35
J6    CON_F30RT_S2MT_SM 22
J7    CON_4RT_WRIB 22
J8    CON_F16ST_D_SMA 26
J9    CON_M80ST_D4MT_SM 17
J10   CON_M50SM_5MM 25
J11   CON_F14RT_S2MT_SM 33
J12   CON_M40ST_D4MT_SM 26
J13   CON_M50SM_5MM 25
J14   CON_F30RT_T6MT_TH1 22
J15   CON_F5RT_MINIDIN_TH 22
J16   CON_10STSM_5087 26
J17   CON_RJ45_SHORT_4MT_TH 28
J18   CON_M8RT_S_SM 32
J19   CON_F200RT_DDRDIMM_SM1 11
J20   CON_M80ST_D2MT_SM3 25
J21   CON_F14RT_S2MT_SM 23
J22   CON_F200RT_DDRDIMM_SM2 11
J23   CON_F6RT_S4MT_TH1 30
J25   CON_M8RT_S_SM 32
J26   CON_F9RT_1394B_S6MT_SMA 30
L1    IND         14
L2    IND         18
L3    IND         18
L4    IND         18
L5    IND         28
L6    IND         22
L7    IND         29
L8    IND         32
L9    IND         32
L10   IND         32
L11   IND         23
L12   IND         32
L13   FILTER_4P 20
L14   FILTER_4P 20
L15   FILTER_4P 20
L16   IND         21
L17   IND         21
L18   IND         14
L19   IND         20
L20   IND         20
L21   FILTER_4P 22
L22   IND         14
L23   IND         22
L24   IND         19
L25   IND         22
L26   IND         22
L27   IND         22
L28   IND         22
L29   IND         22
L30   IND_3P      19
L31   IND         22
L32   IND         22
L33   IND         22
L34   IND         28
L35   IND         36
L36   IND_3P      35
L37   IND_3P      33
L38   IND         34
L39   IND         30
L40   IND         30
L41   IND         34
L42   IND         32
L43   FILTER_4P 30
L44   FILTER_4P 30
L45   IND         36
L46   IND         23
L48   IND         26
L49   IND         23
L50   IND         30
L51   IND         29
L52   IND         23
L53   IND         32
L54   IND         27
L55   IND         21
L56   IND         21
L57   IND         21
L58   IND         21
L59   IND         21
L60   IND         21
L61   IND         21
L62   IND         21
L63   IND         21
L64   IND         21
L65   IND         21
L66   IND         21
L67   IND         21
L68   IND         21
L69   IND         21
L70   FILTER_4P 30
L71   FILTER_4P 30
L72   FILTER_4P 22
L73   FILTER_4P 22
L74   FILTER_4P 22
L75   IND         36
L76   IND         26
L77   IND         26
L78   IND         26
L79   IND         26
L80   IND         26
L81   IND         26
L82   IND         26
L83   IND         20
L84   IND         26
L85   IND         26
L86   IND         26
L87   IND         20
L88   IND         20
L89   IND         20
L90   IND         23
L91   IND         23
PD1   PHOTODIODE_2P 23
Q1    TRA_2N7002DW 7
Q2    TRA_2N7002DW 7
Q3    TRA_2N7002 7
Q4    TRA_2N3904 7
Q5    TRA_2N3904 19
Q6    TRA_2N3904 19
Q7    TRA_FDG6324L 22
Q8    TRA_2N7002 22
Q9    TRA_2N7002DW 34
Q10   TRA_2N7002DW 32
Q11   TRA_SI3443DV 22
Q12   TRA_2N3904 35
Q13   TRA_SI4435DY 32
Q14   TRA_FDG6324L 33
Q15   TRA_2N7002DW 28
Q16   TRA_SI4435DY 32
Q17   TRA_2N3904 35
Q18   TRA_2N7002DW 31
Q19   TRA_2N7002 36
Q20   TRA_2N7002DW 32
Q21   TRA_2N7002DW 32
Q22   TRA_2N7002 31
Q23   TRA_2N7002DW 34
Q24   TRA_SI4435DY 32
Q25   TRA_2N7002DW 30 34
Q26   TRA_2N7002DW 26
Q27   TRA_2N7002DW 32
Q28   TRA_SI3443DV 34
Q29   TRA_2N7002DW 32
Q30   TRA_2N7002DW 32
Q31   TRA_2N7002DW 26
Q32   TRA_SI3443DV 34
Q33   TRA_2N7002 26
Q34   TRA_2N7002 23
Q35   TRA_2N7002DW 22 23
Q36   TRA_2N7002DW 14
Q38   TRA_2N7002DW 22
Q39   TRA_2N3904 26
Q40   TRA_TP0610 22
Q41   TRA_2N7002DW 22
Q42   TRA_2N3904 22
Q43   TRA_SI3443DV 34
Q44   TRA_2N3904 22
Q45   TRA_TP0610 22
Q46   TRA_SI3446DV 36
Q47   TRA_2N3904 26
Q48   TRA_SI7892DP 19
Q49   TRA_SI7860DP 35
Q50   TRA_SI7860DP 35
Q51   TRA_SI7860DP 19
Q52   TRA_SI4888DY 34
Q53   TRA_IRF7832 35
Q54   TRA_IRF7832 35
Q55   TRA_IRF7832 35
Q56   TRA_IRF7811W 36
Q57   TRA_IRF7805 36
Q58   TRA_2N7002DW 30
Q59   TRA_IRF7805 33
Q60   TRA_IRF7811W 33
Q61   TRA_SI4888DY 34
Q62   TRA_2N3904 26
Q63   TRA_IRF7805 32
Q64   TRA_IRF7811W 32
Q65   TRA_2N7002DW 32
Q66   TRA_2N3904 26
Q67   TRA_NDS9407 30
Q68   TRA_IRF7811W 36
Q69   TRA_IRF7805 36
Q70   TRA_SI3443DV 23
Q71   TRA_SI4888DY 34
Q72   TRA_SI4888DY 34
Q73   TRA_SI2319DS 30
Q74   TRA_2N3906 23
Q75   TRA_2N7002DW 23
Q76   TRA_SUD45P03 32
Q77   TRA_SI3446DV 19
Q78   TRA_2N7002DW 26
Q79   TRA_2N7002DW 34
Q80   TRA_2N7002DW 19
Q81   TRA_2N7002DW 34
Q82   TRA_2N7002DW 36
Q83   TRA_2N7002DW 36
Q84   TRA_SI6467BDQ 36
Q85   TRA_SI6467BDQ 36
Q86   TRA_2N7002DW 35
Q87   TRA_2N7002DW 26
Q88   TRA_2N7002 30
R1    RES    22
R2    RES    7
R3    RES    7
R4    RES    7
R5    RES    7
R6    RES    6
R7    RES    14
R8    RES    25
R9    RES    7
R10   RES    7
R11   RES    7
R12   RES    7
R13   RES    7
R14   RES    7
R15   RES    7
R16   RES    7
R17   RES    7
R18   RES    7
R19   RES    7
R20   RES    7
R21   RES    7
R22   RES    7
R23   RES    7
R24   RES    7
R25   RES    7
R26   RES    7
R27   RES    7
R28   RES    14
R29   RES    14
R30   RES    25
R31   RES    25
R32   RES    25
R33   RES    7
R34   RES    13
R35   RES    25
R36   RES    25
R37   RES    18
R38   RES    18
R39   RES    6
R40   RES    6
R41   RES    14
R42   RES    26
R43   RES    18
R44   RES    18
R45   RES    18
R46   RES    18
R47   RES    7
R48   RES    7
R49   RES    14
R50   RES    14
R51   RES    13
R52   RES    13
R53   RES    18
R54   RES    18
R55   RES    18
R56   RES    27
R57   RES    5
R58   RES    5
R59   RES    5
R60   RES    5
R61   RES    5
R62   RES    6
R63   RES    25
R64   RES    25
R65   RES    5
R66   RES    14
R67   RES    14
R68   RES    25
R69   RES    25
R70   RES    18
R71   RES    25
R72   RES    5
R73   RES    5
R74   RES    25
R75   RES    25
R76   RES    25
R77   RES    12
R78   RES    27
R79   RES    5
R80   RES    14
R81   RES    25
R82   RES    12
R83   RES    27
R84   RES    27
R85   RES    6
R86   RES    6
R87   RES    5
R88   RES    23
R89   RES    14
R90   RES    14
R91   RES    14
R92   RES    13
R93   RES    25
R94   RES    25
R95   RES    25
R96   RES    27
R97   RES    5
R98   RES    5
R99   RES    19
R100  RES    14
R101  RES    25
R102  RES    14
R103  RES    12
R104  RES    18
R105  RES    18
R106  RES    5
R107  RES    5
R108  RES    5
R109  RES    5
R110  RES    19
R111  RES    14
R112  RES    12
R113  RES    14
R114  RES    14
R115  RES    14
R116  RES    25
R117  RES    13
R118  RES    18
R119  RES    18
R120  RES    5
R121  RES    8
R122  RES    8
R123  RES    8
R124  RES    13
R125  RES    14
R126  RES    18
R127  RES    18
R128  RES    5
R129  RES    5
R130  RES    5
R131  RES    8
R132  RES    8
R133  RES    8
R134  RES    8
R135  RES    8
R136  RES    8
R137  RES    8
R138  RES    18
R139  RES    5
R140  RES    8
R141  RES    8
R142  RES    8
R143  RES    8
R144  RES    8
R145  RES    13
R146  RES    12
R147  RES    12
R148  RES    5
R149  RES    7
R150  RES    8
R151  RES    8
R152  RES    8
R153  RES    8
R154  RES    13
R155  RES    14
R156  RES    14
R157  RES    12
R158  RES    18
R159  RES    18
R160  RES    5
R161  RES    8
R162  RES    8
R163  RES    8
R164  RES    8
R165  RES    8
R166  RES    8
R167  RES    8
R168  RES    14
R169  RES    12
R170  RES    12
R171  RES    12
R172  RES    18
R173  RES    18
R174  RES    8
R175  RES    8
R176  RES    8
R177  RES    8
R178  RES    8
R179  RES    8
R180  RES    12
R181  RES    18
R182  RES    8
R183  RES    8
R184  RES    8
R185  RES    12
R186  RES    12
R187  RES    12
R188  RES    18
R189  RES    18
R190  RES    36
R191  RES    9
R192  RES    12
R193  RES    12
R194  RES    12
R195  RES    18
R196  RES    8
R197  RES    8
R198  RES    9
R199  RES    9
R200  RES    18
R201  RES    18
R202  RES    23
R203  RES    19
R204  RES    14
R205  RES    20
R206  RES    5
R207  RES    8
R208  RES    8
R209  RES    12
R210  RES    19
R211  RES    20
R212  RES    20
R213  RES    22
R214  RES    20
R215  RES    8
R216  RES    12
R217  RES    12
R218  RES    20
R219  RES    14
R220  RES    14
R221  RES    19
R222  RES    23
R223  RES    20
R224  RES    26
R225  RES    8
R226  RES    8
R227  RES    8
R228  RES    20
R229  RES    19
R230  RES    12
R231  RES    20
R232  RES    20
R233  RES    31
R234  RES    19
R235  RES    23
R236  RES    19
R237  RES    19
R238  RES    9
R239  RES    10
R240  RES    19
R241  RES    5
R242  RES    10
R243  RES    10
R244  RES    14
R245  RES    19
R246  RES    19
R247  RES    19
R248  RES    19
R249  RES    19
R250  RES    9
R251  RES    21
R252  RES    10
R253  RES    19
R254  RES    19
R255  RES    21
R256  RES    19
R257  RES    19
R258  RES    19
R259  RES    19
R260  RES    19
R261  RES    19
R262  RES    19
R263  RES    19
R264  RES    14
R265  RES    19
R266  RES    19
R267  RES    35
R268  RES    21
R269  RES    19
R270  RES    19
R271  RES    19
R272  RES    19
R273  RES    19
R274  RES    19
R275  RES    5
R276  RES    5
R277  RES    14
R278  RES    14
R279  RES    21
R280  RES    5
R281  RES    14
R282  RES    5
R283  RES    5
R284  RES    21
R285  RES    14
R286  RES    27
R287  RES    15
R288  RES    35
R289  RES    35
R290  RES    35
R291  RES    14
R292  RES    35
R293  RES    26
R294  RES    19
R295  RES    26
R296  RES    34
R297  RES    35
R298  RES    34
R299  RES    21
R300  RES    34
R301  RES    35
R302  RES    35
R303  RES    35
R304  RES    35
R305  RES    35
R306  RES    19
R307  RES    19
```

R308	RES	34
R309	RES	34
R310	RES	34
R311	RES	19
R312	RES	35
R313	RES	35
R314	RES	35
R315	RES	35
R316	RES	19
R317	RES	22
R318	RES	35
R319	RES	28
R320	RES	22
R321	RES	35
R322	RES	35
R323	RES	35
R324	RES	35
R325	RES	35
R326	RES	35
R327	RES	35
R328	RES	35
R329	RES	35
R330	RES	35
R331	RES	35
R332	RES	19
R333	RES	28
R334	RES	28
R335	RES	28
R336	RES	35
R337	RES	35
R338	RES	9
R339	RES	19
R340	RES	19
R341	RES	19
R342	RES	22
R343	RES	28
R344	RES	28
R345	RES	28
R346	RES	28
R347	RES	28
R348	RES	17
R349	RES	35
R350	RES	34
R351	RES	19
R352	RES	19
R353	RES	28
R354	RES	28
R355	RES	28
R356	RES	35
R357	RES	9
R358	RES	32
R359	RES	33
R360	RES	33
R361	RES	28
R362	RES	28
R363	RES	32
R364	RES	32
R365	RES	32
R366	RES	35
R367	RES	34
R368	RES	34
R369	RES	34
R370	RES	28
R371	RES	28
R372	RES	28
R373	RES	17
R374	RES	32
R375	RES	32
R376	RES	35
R377	RES	34
R378	RES	34
R379	RES	33
R380	RES	28
R381	RES	28
R382	RES	28
R383	RES	32
R384	RES	35
R385	RES	35
R386	RES	9
R387	RES	9
R388	RES	19
R389	RES	19
R390	RES	19
R391	RES	22
R392	RES	33
R393	RES	28
R394	RES	32
R395	RES	32
R396	RES	32
R397	RES	35
R398	RES	35
R399	RES	15
R400	RES	22
R401	RES	33
R402	RES	33
R403	RES	28
R404	RES	28
R405	RES	26
R406	RES	28
R407	RES	35
R408	RES	35
R409	RES	9
R410	RES	19
R411	RES	25
R412	RES	33
R413	RES	28
R414	RES	32
R415	RES	35
R416	RES	19
R417	RES	36
R418	RES	36
R419	RES	36
R420	RES	36
R421	RES	36
R422	RES	36
R423	RES	36
R424	RES	36
R425	RES	36
R426	RES	33
R427	RES	28
R428	RES	28
R429	RES	35
R430	RES	19
R431	RES	34
R432	RES	33
R433	RES	33
R434	RES	35
R435	RES	28
R436	RES	29
R437	RES	29
R438	RES	28
R439	RES	9
R440	RES	11
R441	RES	25
R442	RES	25
R443	RES	33
R444	RES	29
R445	RES	29
R446	RES	29
R447	RES	29
R448	RES	35
R449	RES	11
R450	RES	36
R451	RES	19
R452	RES	25
R453	RES	30
R454	RES	32
R455	RES	36
R456	RES	34
R457	RES	34
R458	RES	25
R459	RES	29
R460	RES	32
R461	RES	36
R462	RES	34
R463	RES	34
R464	RES	29
R465	RES	28
R466	RES	32
R467	RES	34
R468	RES	33
R469	RES	29
R470	RES	29
R471	RES	29
R472	RES	30
R473	RES	32
R474	RES	32
R475	RES	31

R476	RES	31
R477	RES	34
R478	RES	29
R479	RES	36
R480	RES	36
R481	RES	34
R482	RES	34
R483	RES	33
R484	RES	29
R485	RES	29
R486	RES	29
R487	RES	32
R488	RES	32
R489	RES	32
R490	RES	32
R491	RES	31
R492	RES	31
R493	RES	36
R494	RES	29
R495	RES	29
R496	RES	29
R497	RES	32
R498	RES	32
R499	RES	32
R500	RES	9
R501	RES	31
R502	RES	31
R503	RES	31
R504	RES	31
R505	RES	31
R506	RES	34
R507	RES	34
R508	RES	33
R509	RES	29
R510	RES	29
R511	RES	32
R512	RES	32
R513	RES	31
R514	RES	34
R515	RES	34
R516	RES	29
R517	RES	31
R518	RES	31
R519	RES	34
R520	RES	34
R521	RES	33
R522	RES	29
R523	RES	34
R524	RES	29
R525	RES	29
R526	RES	32
R527	RES	26
R528	RES	34
R529	RES	34
R530	RES	14
R531	RES	27
R532	RES	6
R533	RES	6
R534	RES	26
R535	RES	31
R536	RES	31
R537	RES	26
R538	RES	34
R539	RES	34
R540	RES	27
R541	RES	33
R542	RES	32
R543	RES	32
R544	RES	31
R545	RES	27
R546	RES	29
R547	RES	29
R548	RES	32
R549	RES	32
R550	RES	23
R551	RES	27
R552	RES	26
R553	RES	26
R554	RES	14
R555	RES	29
R556	RES	29
R557	RES	29
R558	RES	32
R559	RES	32
R560	RES	32
R561	RES	32
R562	RES	31
R563	RES	29
R564	RES	29
R565	RES	32
R566	RES	32
R567	RES	32
R568	RES	23
R569	RES	31
R570	RES	32
R571	RES	32
R572	RES	31
R573	RES	31
R574	RES	29
R575	RES	29
R576	RES	29
R577	RES	29
R578	RES	32
R579	RES	32
R580	RES	32
R581	RES	26
R582	RES	26
R583	RES	31
R584	RES	31
R585	RES	31
R586	RES	27
R587	RES	20
R588	RES	32
R589	RES	34
R590	RES	27
R591	RES	27
R592	RES	31
R593	RES	31
R594	RES	31
R595	RES	31
R596	RES	31
R597	RES	31
R598	RES	23
R599	RES	32
R600	RES	27
R601	RES	25
R602	RES	25
R603	RES	25
R604	RES	14
R605	RES	23
R606	RES	23
R607	RES	36
R608	RES	14
R609	RES	14
R610	RES	36
R611	RES	36
R612	RES	25
R613	RES	25
R614	RES	14
R615	RES	23
R616	RES	36
R617	RES	23
R618	RES	23
R619	RES	23
R620	RES	26
R621	RES	13
R622	RES	14
R623	RES	26
R624	RES	13
R625	RES	14
R626	RES	13
R627	RES	36
R628	RES	26
R629	RES	13
R630	RES	13
R631	RES	14
R632	RES	14
R633	RES	28
R634	RES	14
R635	RES	21
R636	RES	14
R637	RES	19
R638	RES	14
R639	RES	8
R640	RES	8
R641	RES	8
R642	RES	8
R643	RES	8

R644	RES	8
R645	RES	8
R646	RES	8
R647	RES	8
R648	RES	20
R649	RES	22
R650	RES	22
R651	RES	8
R652	RES	8
R653	RES	8
R654	RES	8
R655	RES	22
R656	RES	14
R657	RES	8
R658	RES	8
R659	RES	8
R660	RES	8
R661	RES	22
R662	RES	22
R663	RES	22
R664	RES	8
R665	RES	8
R666	RES	8
R667	RES	8
R668	RES	8
R669	RES	8
R670	RES	22
R671	RES	22
R672	RES	36
R673	RES	8
R674	RES	8
R675	RES	8
R676	RES	8
R677	RES	8
R678	RES	8
R679	RES	26
R680	RES	22
R681	RES	22
R682	RES	14
R683	RES	8
R684	RES	8
R685	RES	8
R686	RES	22
R687	RES	22
R688	RES	22
R689	RES	26
R690	RES	22
R691	RES	22
R692	RES	26
R693	RES	5
R694	RES	22
R695	RES	26
R696	RES	22
R697	RES	34
R698	RES	14
R699	RES	14
R700	RES	22
R701	RES	14
R702	RES	5
R703	RES	22
R704	RES	22
R705	RES	22
R706	RES	22
R707	RES	14
R708	RES	14
R709	RES	36
R710	RES	26
R711	RES	19
R712	RES	36
R713	RES	26
R714	RES	20
R715	RES	36
R716	RES	26
R717	RES	26
R718	RES	22
R719	RES	26
R720	RES	14
R721	RES	21
R722	RES	21
R723	RES	26
R724	RES	22
R725	RES	26
R726	RES	26
R727	RES	36
R728	RES	21
R729	RES	21
R730	RES	25
R731	RES	34
R732	RES	35
R733	RES	28
R734	RES	32
R735	RES	28
R736	RES	30
R737	RES	30
R738	RES	32
R739	RES	32
R740	RES	29
R741	RES	30
R742	RES	32
R743	RES	30
R744	RES	32
R745	RES	25
R746	RES	32
R747	RES	32
R748	RES	32
R749	RES	32
R750	RES	17
R751	RES	30
R752	RES	30
R753	RES	17
R754	RES	32
R755	RES	32
R756	RES	17
R757	RES	17
R758	RES	29
R759	RES	29
R760	RES	29
R761	RES	29
R762	RES	17
R763	RES	32
R764	RES	17
R765	RES	20
R766	RES	17
R767	RES	17
R768	RES	31
R769	RES	31
R770	RES	14
R771	RES	23
R772	RES	23
R773	RES	23
R774	RES	32
R775	RES	29
R776	RES	23
R777	RES	23
R778	RES	31
R779	RES	30
R780	RES	14
R781	RES	29
R782	RES	31
R783	RES	27
R784	RES	27
R785	RES	31
R786	RES	31
R787	RES	31
R788	RES	31
R789	RES	27
R790	RES	27
R791	RES	27
R792	RES	27
R793	RES	27
R794	RES	27
R795	RES	27
R796	RES	27
R797	RES	36
R798	RES	36
R799	RES	36
R800	RES	36
R801	RES	36
R802	RES	36
R803	RES	36
R804	RES	19
R805	RES	35
R806	RES	35
R807	RES	35
R808	RES	35
R809	RES	35
R810	RES	36
R811	RES	26

R812	RES	26
R813	RES	26
R814	RES	26
R815	RES	20
R816	RES	20
R817	RES	20
R818	RES	20
R819	RES	14
R820	RES	14
R821	RES	20
R822	RES	20
R823	RES	20
R824	RES	20
R825	RES	14
R826	RES	20
R827	RES	20
R828	RES	20
R829	RES	20
R830	RES	20
R831	RES	20
R832	RES	20
R833	RES	20
R834	RES	20
R835	RES	20
R836	RES	20
R837	RES	20
R838	RES	20
R839	RES	20
R840	RES	20
R841	RES	20
R842	RES	20
R843	RES	31
R844	RES	31
R845	RES	24
R846	RES	24
R847	RES	24
R848	RES	24
R849	RES	24
R850	RES	23
R851	RES	24
R852	RES	24
R853	RES	24
R854	RES	24
R855	RES	24
R856	RES	24
R857	RES	24
R858	RES	24
R859	RES	24
R860	RES	24
R861	RES	24
R862	RES	24
R863	RES	14
R864	RES	14
R865	RES	23
R866	RES	23
R867	RES	30
R868	RES	31
R869	RES	31
R870	RES	31
R871	RES	33
R872	RES	26
R873	RES	26
R874	RES	26
R875	RES	26
R876	RES	35
R877	RES	31
R878	RES	26
R879	RES	26
R880	RES	33
R881	RES	24
R882	RES	6
R883	RES	24
R884	RES	6
R885	RES	6
R886	RES	6
R887	RES	30
R888	RES	30
R889	RES	30
R890	RES	30
R891	RES	30
R892	RES	30
R893	RES	30
R894	RES	30
R895	RES	14
R896	RES	14
R897	RES	14
R898	RES	31
R899	RES	23
R900	RES	23
R901	RES	23
R902	RES	23
R903	RES	6
R904	RES	6
R905	RES	6
R906	RES	6
R907	RES	6
R908	RES	26
R909	RES	26
R910	RES	26
R911	RES	26
R912	RES	14
R913	RES	14
R914	RES	14
R915	RES	26
R916	RES	14
R917	RES	26
R918	RES	26
RP1	RPAK4P	14
RP2	RPAK4P	25
RP3	RPAK4P	25
RP4	RPAK4P	25
RP5	RPAK4P	25
RP6	RPAK10P2C	6
RP7	RPAK4P	14
RP8	RPAK4P	14
RP9	RPAK4P	25
RP10	RPAK4P	25
RP11	RPAK4P	25
RP12	RPAK4P	13
RP13	RPAK4P	25
RP14	RPAK4P	13
RP15	RPAK4P	13
RP16	RPAK4P	13
RP17	RPAK4P	12
RP18	RPAK4P	12
RP19	RPAK4P	12
RP20	RPAK4P	12
RP21	RPAK4P	8
RP22	RPAK4P	12
RP23	RPAK4P	8
RP24	RPAK4P	8 14
RP25	RPAK4P	9
RP26	RPAK4P	9
RP27	RPAK4P	23
RP29	RPAK4P	14
RP30	RPAK4P	9
RP31	RPAK4P	9
RP33	RPAK4P	9
RP34	RPAK4P	9
RP35	RPAK4P	9
RP36	RPAK4P	9
RP37	RPAK4P	29
RP38	RPAK4P	29
RP39	RPAK10P2C	17
RP40	RPAK4P	31
RP41	RPAK4P	31
RP42	RPAK10P2C	23
RP43	RPAK10P2C	23
RP45	RPAK4P	27
RP47	RPAK4P	14
RP48	RPAK4P	14
RP49	RPAK4P	25
RP50	RPAK4P	25
RP51	RPAK4P	14
RP52	RPAK4P	23 27
RP53	RPAK4P	23
RP54	RPAK4P	27
RP55	RPAK4P	27
RP56	RPAK4P	14
RP62	RPAK2P	20
RP63	RPAK2P	20
RP64	RPAK2P	20
RP65	RPAK2P	20
RP66	RPAK2P	20
RP67	RPAK2P	20
RP68	RPAK2P	20
SH1	SHLD_3P_EMI	4
SP1	SPKR_CLIP_P84	4

SP2	SPKR_CLIP_P84	4
SP3	SPKR_CLIP_P84	4
SP4	SPKR_CLIP_P84	4
SP5	SPKR_CLIP_P84	4
SP6	SPKR_CLIP_P84	4
T1	XFR_ENET_10008P	28
U1	SN74AUC1G04	7
U2	SN74AUC1G08	6
U3	AZ97467	26
U4	SN74AUC1G08	6
U5	KXM52	24
U6	FAN2558	5
U7	VREG_LT1962	14
U8	MAX8860	21
U9	CBTV4020	10
U10	CBTV4020	10
U11	PI3B3257	35
U12	CBTV4020	10
U13	CBTV4020	10
U14	LTC3405	28
U15	COMPARATOR_LMC7211	32
U16	LTC1778	19
U17	FEPR_1MX8	9
U18	LTC1625	33
U19	PWR_CNTRL_TPS2211	17
U20	MAX1717	35
U21	COMPARATOR_LMC7211	33
U22	MAX1715	36
U23	AMP_MAX4172	32
U24	7432	22
U25	VREG_LP2951	33
U26	PC115190GU	17
U27	COMPARATOR_LMC7211	31
U28	LTC3707	34
U29	T8B818A3A	29
U30	VREG_LP2951	33
U31	MAX1772	32
U32	EEPROM_32KX8_M24256B	6
U33	M16C62	31
U34	VREG_LM2594	29
U35	SIL178	20
U36	LTC1761	29
U37	VREG_LT1962	29
U38	COMPARATOR_LMC7211	32
U39	UPD720101_FBGA	27
U40	OPAMP_MAX4236EUTT	23
U41	MAX6804	31
U42	CLK_GEN_CY28512	14
U43	APOLLO_MPC7447A_360	5 6
U44	RAGE_MBLTY_M11_C8P64_667	18 19 21
U45	INTREPID	8 9 12 13 14 15
U46	COMPARATOR_LMC7211	22
U47	CLK_GEN_CY25811	18
U48	SIL178	20
U49	TRANSCEIVER_88E1111	28
U50	OPAMP_LMC7111	32
U51	INA138	24
U52	FEPR_256X8X8_ST72264_BGA	23
U53	PIC16F818_QFN	24
U54	VREG_MH1571J	21
U55	VREG_MH1571J	21
U56	741G32	22
U57	741G32	22
U58	LTC3412	36
U59	MM3120	23
U60	LI83LG28Q	24
U61	ATTINY2313	6
U62	COMPARATOR_LMC7211	30
XW1	SHORT	36
XW2	SHORT	19
XW3	SHORT	35
XW4	SHORT	33
XW5	SHORT	35
XW6	SHORT	36
XW7	SHORT	35
XW8	SHORT	34
XW9	SHORT	26
XW10	SHORT	26
XW11	SHORT	26
XW12	SHORT	22
XW13	SHORT	22
XW14	SHORT	24
XW15	SHORT	35
XW16	SHORT	24
XW17	SHORT	24
XW18	SHORT	24
XW19	SHORT	32
XW20	SHORT	19
XW21	SHORT	19
XW22	SHORT	19
XW23	SHORT	19
XW24	SHORT	19
XW27	SHORT	21
XW28	SHORT	21
XW29	SHORT	21
XW30	SHORT	21
XW31	SHORT	5
Y1	CRYSTAL	14
Y3	CRYSTAL	28
Y4	CRYSTAL	23
Y5	CRYSTAL	27
Y6	CRYSTAL	31
Y7	CRYSTAL_4PIN	31
ZT1	HOLE_VIA	4
ZT2	MTGHOLE	4
ZT3	HOLE_VIA	4
ZT4	MTGHOLE	4
ZT5	MTGHOLE	4
ZT6	MTGHOLE	4
ZT7	HOLE_VIA	4
ZT8	HOLE_VIA	4
ZT9	HOLE_VIA	4
ZT10	MTGHOLE	4
ZT11	MTGHOLE	4
ZT12	HOLE_VIA	4
ZT13	HOLE_VIA	4
ZT14	HOLE_VIA	4
ZT15	HOLE_VIA	4
ZT16	MTGHOLE	4
ZT17	HOLE_VIA	4
ZT18	HOLE_VIA	4
ZT19	HOLE_VIA	4
ZT20	HOLE_VIA	4
ZT21	HOLE_VIA	4
ZT22	HOLE_VIA	4
ZT23	HOLE_VIA	4
ZT24	HOLE_VIA	4
ZT25	HOLE_VIA	4
ZT26	HOLE_VIA	4
ZT27	HOLE_VIA	4
ZT28	HOLE_VIA	4
ZT29	HOLE_VIA	4
ZT30	HOLE_VIA	4
ZT31	HOLE_VIA	4
ZT32	HOLE_VIA	4
ZT33	HOLE_VIA	4
ZT34	HOLE_VIA	4
ZT35	HOLE_VIA	4
ZT36	HOLE_VIA	4
ZT37	HOLE_VIA	4
ZT38	HOLE_VIA	4
ZT39	HOLE_VIA	4
ZT40	HOLE_VIA	4
ZT41	HOLE_VIA	4
ZT42	HOLE_VIA	4
ZT43	HOLE_VIA	4
ZT44	HOLE_VIA	4
ZT45	HOLE_VIA	4
ZT46	HOLE_VIA	4
ZT47	HOLE_VIA	4
ZT48	HOLE_VIA	4
ZT49	HOLE_VIA	4
ZT50	HOLE_VIA	4
ZT51	HOLE_VIA	4
ZT52	HOLE_VIA	4
ZT53	HOLE_VIA	4
ZT54	HOLE_VIA	4
ZT55	HOLE_VIA	4
ZT56	HOLE_VIA	4
ZT57	HOLE_VIA	4
ZT58	HOLE_VIA	4
ZT59	HOLE_VIA	4
ZT60	HOLE_VIA	4
ZT61	HOLE_VIA	4
ZT62	HOLE_VIA	4
ZT63	HOLE_VIA	4
ZT64	HOLE_VIA	4
ZT65	HOLE_VIA	4
ZT66	HOLE_VIA	4
ZT67	HOLE_VIA	4
ZT68	HOLE_VIA	4
ZT69	HOLE_VIA	4
ZT70	HOLE_VIA	4
ZT71	HOLE_VIA	4
ZT72	HOLE_VIA	4
ZT73	HOLE_VIA	4
ZT74	HOLE_VIA	4
ZT75	HOLE_VIA	4
ZT76	HOLE_VIA	4
ZT77	HOLE_VIA	4
ZT78	HOLE_VIA	4
ZT79	HOLE_VIA	4
ZT80	HOLE_VIA	4
ZT81	HOLE_VIA	4
ZT82	HOLE_VIA	4
ZT83	MYOHOLE	4