

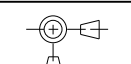
1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
E		408395	PRODUCTION RELEASED	11/02/05	?

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-6839	1	SCHEM,BOZEMAN,Q41C	SCH1		
820-1810	1	PCBF,BOZEMAN,Q41C	PCB1	CRITICAL	
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6MM	[EEE:SYV]	CRITICAL	EEE_SYV
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6MM	[EEE:TML]	CRITICAL	EEE_TML
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6MM	[EEE:USH]	CRITICAL	EEE_USH
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6MM	[EEE:USJ]	CRITICAL	EEE_USJ

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X.XXX : _____		QA APPD	DESIGNER		
ANGLES : _____		RELEASE	SCALE		
DO NOT SCALE DRAWING		NONE		TITLE	
 THIRD ANGLE PROJECTION		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE D	DRAWING NUMBER
				826-4393	REV. E
				SHEET 1 OF 115	

Design-Specific Rules

TABLE_SPACING_RULE	STANDARD	=DEFAULT	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT
BGA_P1MM	10	*	0.10 MM	1.25 MM	0.1 MM	12.5 MM	15.0 MM	
BGA_P2MM	20	*	0.20 MM	1.25 MM	0.1 MM	12.5 MM	15.0 MM	
DEFAULT	*		0.1 MM	2.5 MM	0.15 MM	10.0 MM	15.0 MM	

TABLE_SPACING_ASSIGNMENT

TABLE_SPACING_ASSIGNMENT	*	1MM	BGA_P1MM
AGP_STB	*	1MM	BGA_P2MM
CLOCK	*	1MM	BGA_P2MM
RAM_DIFF	*	1MM	BGA_P2MM

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE	STANDARD	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT
DEFAULT	*	Y	0.100 MM	0.100 mm	1.25 MM

Layer-specific rules for 90-ohm differential impedance

TABLE_SPACING_RULE	90_OHM_DIFF	TOP,BOTTOM	2.5 MM	0.200 MM	2.5 MM	1.0 MM
TABLE_SPACING_RULE	90_OHM_DIFF	*	2.5 MM	0.200 MM	2.5 MM	1.0 MM

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE	90_OHM_DIFF	TOP,BOTTOM	Y	0.118 MM	0.1 MM	5 MM
TABLE_PHYSICAL_RULE	90_OHM_DIFF	*	Y	0.125 MM	0.1 MM	5 MM

Layer-specific rules for 100-ohm differential impedance

TABLE_SPACING_RULE	100_OHM_DIFF	TOP,BOTTOM	2.5 MM	0.200 MM	2.5 MM	1.0 MM
TABLE_SPACING_RULE	100_OHM_DIFF	*	2.5 MM	0.200 MM	2.5 MM	1.0 MM

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE	100_OHM_DIFF	TOP,BOTTOM	Y	0.092 MM	0.1 MM	5 MM
TABLE_PHYSICAL_RULE	100_OHM_DIFF	*	Y	0.100 MM	0.1 MM	5 MM

Layer-specific rules for 110-ohm differential impedance

TABLE_SPACING_RULE	110_OHM_DIFF	TOP,BOTTOM	2.5 MM	0.330 MM	2.5 MM	1.0 MM
TABLE_SPACING_RULE	110_OHM_DIFF	*	2.5 MM	0.300 MM	2.5 MM	1.0 MM

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE	110_OHM_DIFF	TOP,BOTTOM	Y	0.080 MM	0.1 MM	5 MM
TABLE_PHYSICAL_RULE	110_OHM_DIFF	*	Y	0.085 MM	0.1 MM	5 MM

Portable-specific Override Rules

TABLE_SPACING_RULE	AGP	201	*	0.2 MM
TABLE_SPACING_RULE	AGP_STB	251	*	0.25 MM
TABLE_SPACING_RULE	VGA	151	*	0.15 MM
TABLE_SPACING_RULE	TV	151	*	0.15 MM

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE	VGA	*	=60_OHM_SE	=60_OHM_SE	=60_OHM_SE	=60_OHM_SE
TABLE_PHYSICAL_RULE	TV	*	=60_OHM_SE	=60_OHM_SE	=60_OHM_SE	=60_OHM_SE

Layer-specific rules for 60-ohm single-ended impedance

TABLE_PHYSICAL_RULE	60_OHM_SE	*	Y	0.076 MM	=50_OHM_SE	=50_OHM_SE
TABLE_PHYSICAL_RULE	50_OHM_SE	*	Y	0.076 MM <td>=50_OHM_SE</td> <td>=50_OHM_SE</td>	=50_OHM_SE	=50_OHM_SE

Layer-specific rules for 50-ohm single-ended impedance

TABLE_SPACING_RULE	50_OHM_SE	*	Y	0.100 MM	0.100 MM	1.25 MM
TABLE_SPACING_RULE	50_OHM_SE	*	Y <th>0.100 MM</th> <th>0.100 MM</th> <th>1.25 MM</th>	0.100 MM	0.100 MM	1.25 MM

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE	50_OHM_SE	*	Y	0.100 MM	0.100 MM	1.25 MM
TABLE_PHYSICAL_RULE	50_OHM_SE	*	Y <th>0.100 MM</th> <th>0.100 MM</th> <th>1.25 MM</th>	0.100 MM	0.100 MM	1.25 MM

Layer-specific rules for 50-ohm single-ended impedance

TABLE_SPACING_RULE	50_OHM_SE	*	Y	0.100 MM	0.100 MM	1.25 MM
TABLE_SPACING_RULE	50_OHM_SE	*	Y <th>0.100 MM</th> <th>0.100 MM</th> <th>1.25 MM</th>	0.100 MM	0.100 MM	1.25 MM

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE	50_OHM_SE	*	Y	0.100 MM	0.100 MM	1.25 MM
TABLE_PHYSICAL_RULE	50_OHM_SE	*	Y <th>0.100 MM</th> <th>0.100 MM</th> <th>1.25 MM</th>	0.100 MM	0.100 MM	1.25 MM

Layer-specific rules for 50-ohm single-ended impedance

TABLE_SPACING_RULE	50_OHM_SE	*	Y	0.100 MM	0.100 MM	1.25 MM
TABLE_SPACING_RULE	50_OHM_SE	*	Y <th>0.100 MM</th> <th>0.100 MM</th> <th>1.25 MM</th>	0.100 MM	0.100 MM	1.25 MM

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE	50_OHM_SE	*	Y	0.100 MM	0.100 MM	1.25 MM
TABLE_PHYSICAL_RULE	50_OHM_SE	*	Y <th>0.100 MM</th> <th>0.100 MM</th> <th>1.25 MM</th>	0.100 MM	0.100 MM	1.25 MM

Layer-specific rules for 50-ohm single-ended impedance

TABLE_SPACING_RULE	50_OHM_SE	*	Y	0.100 MM	0.100 MM	1.25 MM
TABLE_SPACING_RULE	50_OHM_SE	*	Y <th>0.100 MM</th> <th>0.100 MM</th> <th>1.25 MM</th>	0.100 MM	0.100 MM	1.25 MM

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE	50_OHM_SE	*	Y	0.100 MM	0.100 MM	1.25 MM
TABLE_PHYSICAL_RULE	50_OHM_SE	*	Y <th>0.100 MM</th> <th>0.100 MM</th> <th>1.25 MM</th>	0.100 MM	0.100 MM	1.25 MM

Layer-specific rules for 50-ohm single-ended impedance

TABLE_SPACING_RULE	50_OHM_SE	*	Y	0.100 MM	0.100 MM	1.25 MM
TABLE_SPACING_RULE	50_OHM_SE	*	Y <th>0.100 MM</th> <th>0.100 MM</th> <th>1.25 MM</th>	0.100 MM	0.100 MM	1.25 MM

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE	50_OHM_SE	*	Y	0.100 MM	0.100 MM	1.25 MM
TABLE_PHYSICAL_RULE	50_OHM_SE	*	Y <th>0.100 MM</th> <th>0.100 MM</th> <th>1.25 MM</th>	0.100 MM	0.100 MM	1.25 MM

Layer-specific rules for 50-ohm single-ended impedance

TABLE_SPACING_RULE	50_OHM_SE	*	Y	0.100 MM	0.100 MM	1.25 MM
TABLE_SPACING_RULE	50_OHM_SE	*	Y <th>0.100 MM</th> <th>0.100 MM</th> <th>1.25 MM</th>	0.100 MM	0.100 MM	1.25 MM

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE	50_OHM_SE	*	Y	0.100 MM	0.100 MM	1.25 MM
TABLE_PHYSICAL_RULE	50_OHM_SE	*	Y <th>0.100 MM</th> <th>0.100 MM</th> <th>1.25 MM</th>	0.100 MM	0.100 MM	1.25 MM

Layer-specific rules for 50-ohm single-ended impedance

TABLE_SPACING_RULE	50_OHM_SE	*	Y	0.100 MM	0.100 MM	1.25 MM
TABLE_SPACING_RULE	50_OHM_SE	*	Y <th>0.100 MM</th> <th>0.100 MM</th> <th>1.25 MM</th>	0.100 MM	0.100 MM	1.25 MM

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE	50_OHM_SE	*	Y	0.100 MM	0.100 MM	1.25 MM
TABLE_PHYSICAL_RULE	50_OHM_SE	*	Y <th>0.100 MM</th> <th>0.100 MM</th> <th>1.25 MM</th>	0.100 MM	0.100 MM	1.25 MM

Layer-specific rules for 50-ohm single-ended impedance

TABLE_SPACING_RULE	50_OHM_SE	*	Y	0.100 MM	0.100 MM	1.25 MM
TABLE_SPACING_RULE	50_OHM_SE	*	Y <th>0.100 MM</th> <th>0.100 MM</th> <th>1.25 MM</th>	0.100 MM	0.100 MM	1.25 MM

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE	50_OHM_SE	*	Y	0.100 MM	0.100 MM	1.25 MM
TABLE_PHYSICAL_RULE	50_OHM_SE	*	Y <th>0.100 MM</th> <th>0.100 MM</th> <th>1.25 MM</th>	0.100 MM	0.100 MM	1.25 MM

Layer-specific rules for 50-ohm single-ended impedance

TABLE_SPACING_RULE	50_OHM_SE	*	Y	0.100 MM	0.100 MM	1.25 MM
TABLE_SPACING_RULE	50_OHM_SE	*	Y <th>0.100 MM</th> <th>0.100 MM</th> <th>1.25 MM</th>	0.100 MM	0.100 MM	1.25 MM

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE	50_OHM_SE	*	Y	0.100 MM	0.100 MM	1.25 MM
TABLE_PHYSICAL_RULE	50_OHM_SE	*	Y <th>0.100 MM</th> <th>0.100 MM</th> <th>1.25 MM</th>	0.100 MM	0.100 MM	1.25 MM

Layer-specific rules for 50-ohm single-ended impedance

TABLE_SPACING_RULE	50_OHM_SE	*	Y	0.100 MM	0.100 MM	1.25 MM
TABLE_SPACING_RULE	50_OHM_SE	*	Y <th>0.100 MM</th> <th>0.100 MM</th> <th>1.25 MM</th>	0.100 MM	0.100 MM	1.25 MM

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE	50_OHM_SE	*	Y	0.100 MM	0.100 MM	1.25 MM
TABLE_PHYSICAL_RULE	50_OHM_SE	*	Y <th>0.100 MM</th> <th>0.100 MM</th> <th>1.25 MM</th>	0.100 MM	0.100 MM	1.25 MM

Layer-specific rules for 50-ohm single-ended impedance

TABLE_SPACING_RULE	50_OHM_SE	*	Y	0.100 MM	0.100 MM	1.25 MM
TABLE_SPACING_RULE	50_OHM_SE	*	Y <th>0.100 MM</th> <th>0.100 MM</th> <th>1.25 MM</th>	0.100 MM	0.100 MM	1.25 MM

TABLE_PHYSICAL_RULE

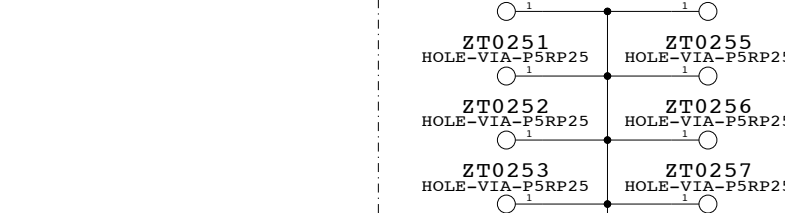
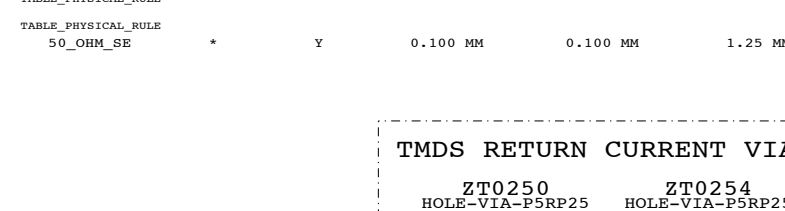
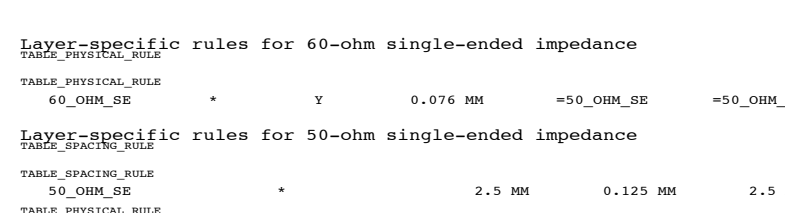
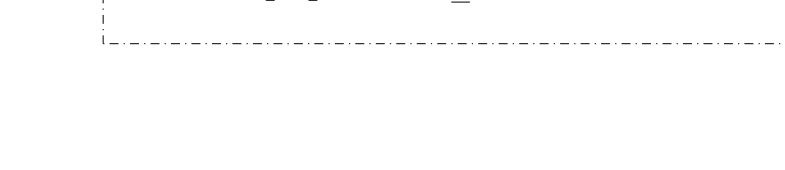
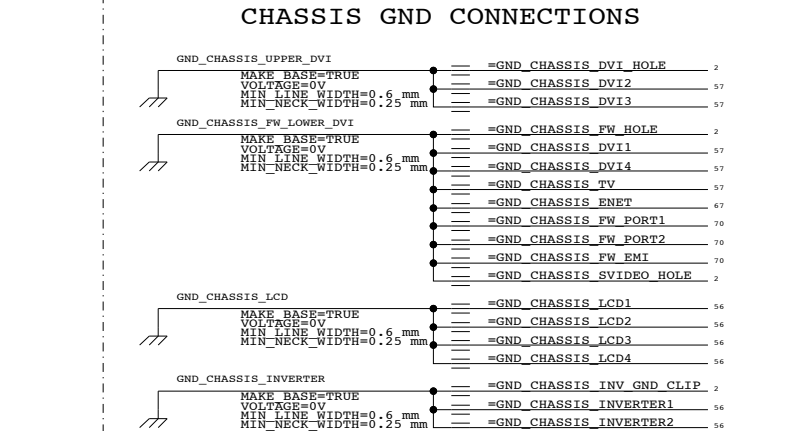
TABLE_PHYSICAL_RULE	50_OHM_SE	*	Y	0.100 MM	0.100 MM	1.25 MM
TABLE_PHYSICAL_RULE	50_OHM_SE	*	Y <th>0.100 MM</th> <th>0.100 MM</th> <th>1.25 MM</th>	0.100 MM	0.100 MM	1.25 MM

Layer-specific rules for 50-ohm single-ended impedance

TABLE_SPACING_RULE	50_OHM_SE	*	Y	0.100 MM	0.100 MM	1.25 MM
TABLE_SPACING_RULE	50_OHM_SE	*	Y <th>0.100 MM</th> <th>0.100 MM</th> <th>1.25 MM</th>	0.100 MM	0.100 MM	1.25 MM

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE	50_OHM_SE	*	Y	0.100 MM	0.100 MM	1.25 MM
TABLE_PHYSICAL_RULE	50_OHM_SE	*	Y <th>0.100 MM</th> <th>0.100 MM</th> <th>1.25 MM</th>	0.100 MM	0.100 MM	1.25 MM



Module Components

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S0383	1	IC,ASIC,I2,REV1.2,NB/SB,974 BGA	U2100	CRITICAL	
337S3135	1	IC,PMU05,BLANK,QFP	U2700	CRITICAL	PMU_BLANK
341S1772	1	IC,PMU05,Vxxx,QFP	U2700	CRITICAL	PMU_PROG
337S3181	1	IC,A7PM,R1.5,1.67GHZ,LGA,1.28V,25W,85C	U3600	CRITICAL	A7PM_1P67_LGA
337S3077	1	IC,A8,xxxGHZ	U3600	CRITICAL	CPU_A8
338S0252	1	IC,GPU,M11P	U5700	CRITICAL	GPU_LF
338S0299	1	IC,GPU,M11P,EUTECTIC	U5700	CRITICAL	GPU_EUTECTIC
335S0088	1	BOOTROM,BLANK	U7100	CRITICAL	BOOTROM_BLANK
341S1739	1	IC,BOOTROM,B,Q41C	U7100	CRITICAL	BOOTROM_PROG
343S0356	1	IC,ASIC,VESTA,V1.3,LF	U8500	CRITICAL	
333S0317	4	IC,GDDR SDRAM,2MX32X4,300MHZ, LF FBGA144	U6200,U6250,U6300,U6350	CRITICAL	VRAM_SAMSUNG
333S0314	4	IC,GDDR SDRAM,2MX32X4,300MHZ, LF FBGA144	U6200,U6250,U6300,U6350	CRITICAL	VRAM_HYNIX

BOM OPTIONS

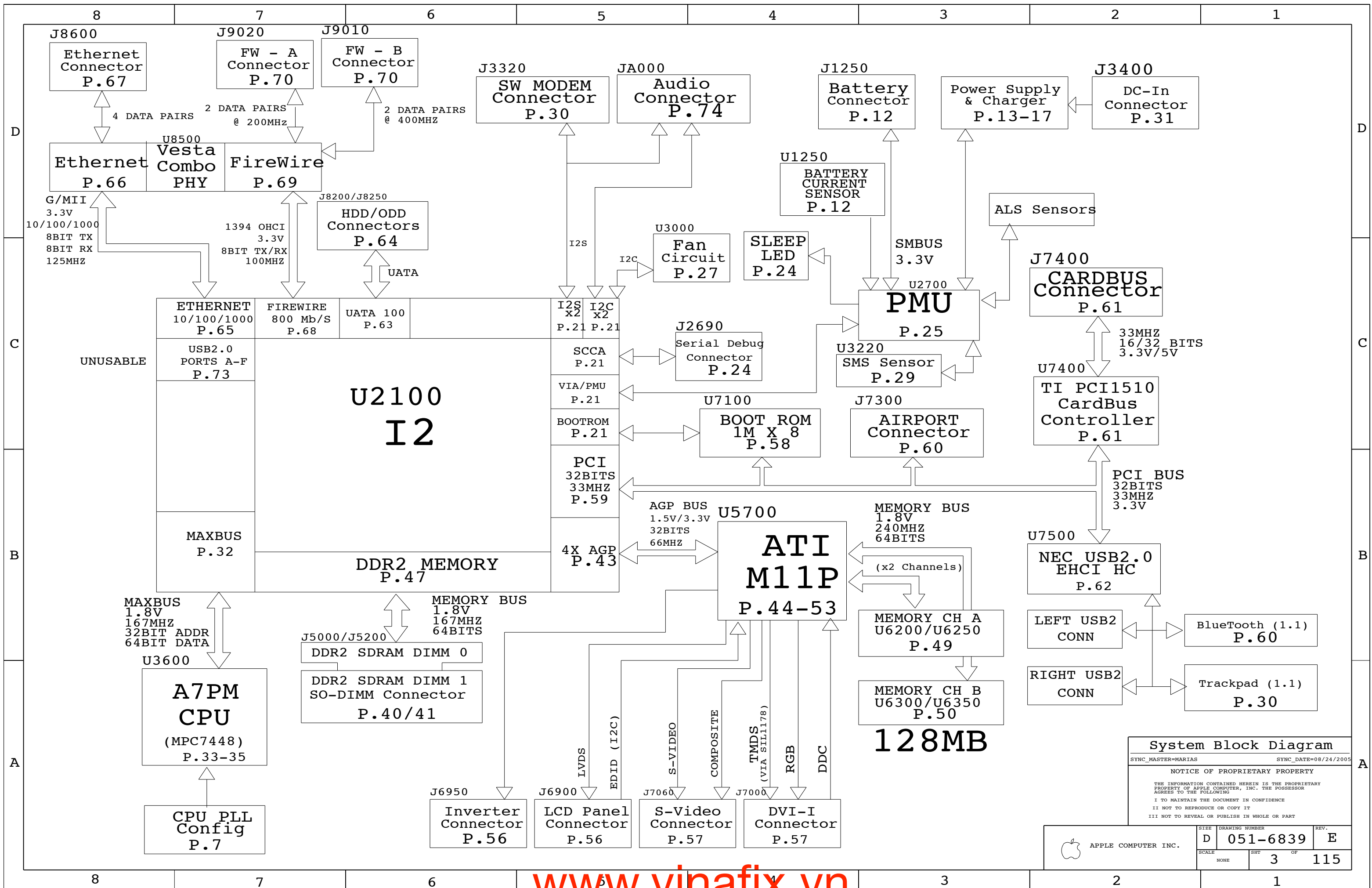
BOM NUMBER	BOM NAME	BOM OPTIONS
630-7017	PCBA,MLB,BESTMHZ,BOZEMAN,VRAM_S,Q41C	COMMON,ALTERNATE,EEE_SYV,GPU_LF,VRAM_SAMSUNG,gQ41C,gCommon
630-7186	PCBA,MLB,BESTMHZ,BOZEMAN,VRAM_H,Q41C	COMMON,ALTERNATE,EEE_TML,GPU_LF,VRAM_HYNIX,gQ41C,gCommon
630-7443	PCBA,MLB,BESTMHZ,GPU_EUT,VRAM_S,PB17	COMMON,ALTERNATE,EEE_USH,GPU_EUTECTIC,VRAM_SAMSUNG,gQ41C,gCommon
630-7444	PCBA,MLB,BESTMHZ,GPU_EUT,VRAM_H,PB17	COMMON,ALTERNATE,EEE_USJ,GPU_EUTECTIC,VRAM_HYNIX,gQ41C,gCommon

Board Information

SYNC_MASTER=N/A	SYNC_DATE=N/A
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Apple Computer Inc. Drawing Information

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NONE	2	OF	E
DRAWING NUMBER			051-6839
NONE			115



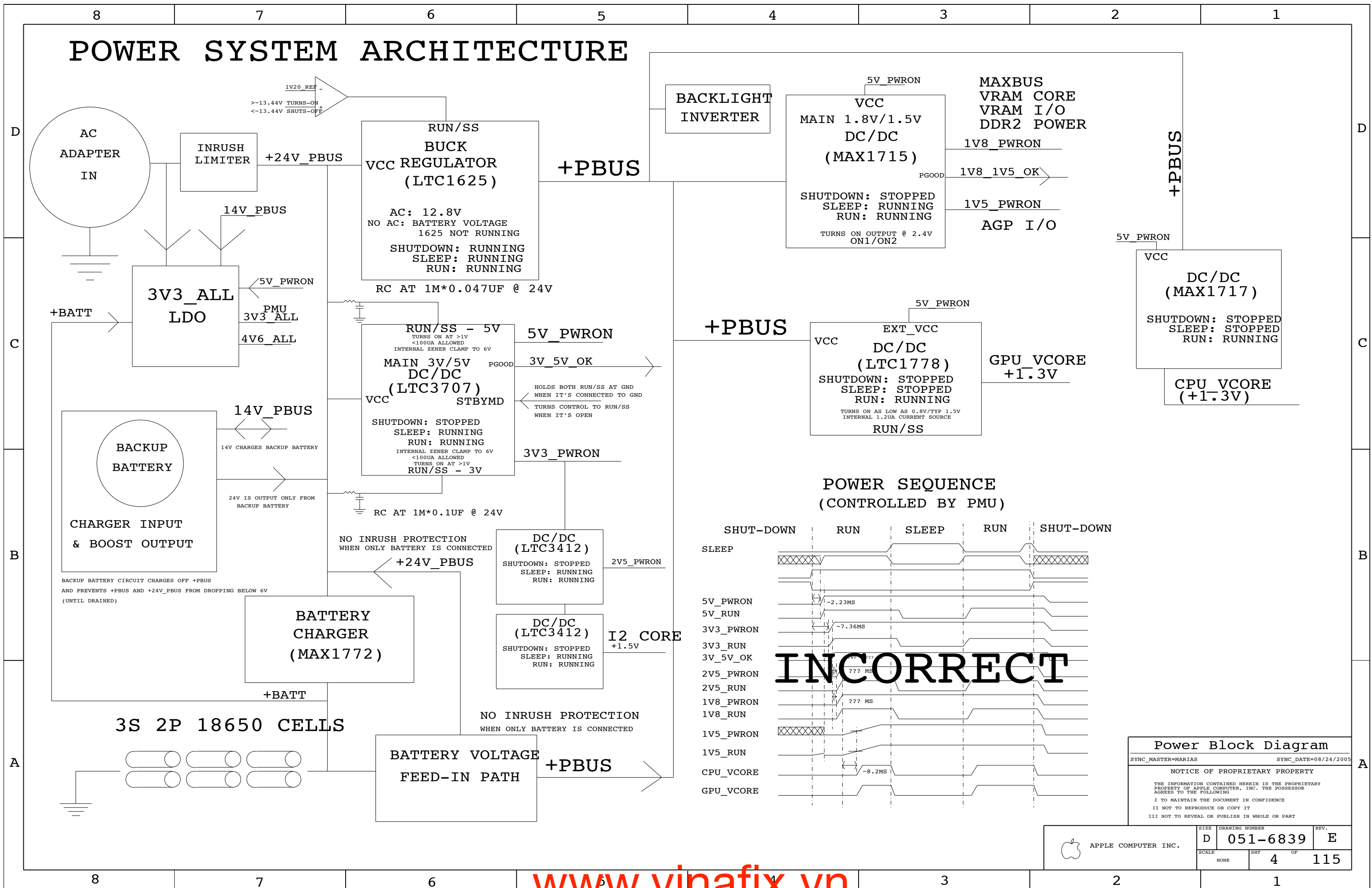
System Block Diagram

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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NONE	3		115

POWER SYSTEM ARCHITECTURE



Power Block Diagram
 SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005
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	D	051-6839	E
SCALE	SHT	OF	REV.
NONE	4	115	

REVISION HISTORY

PROTO

- 04/05/2005 - Beginning revision history
- Sync'd FB pin swaps from 051-5838
- Pinned out audio connector per flex cable
- 04/07/2005 - Pinned out fire/USB/AFIC connector per flex cable
- Moved modem connector to non-stuffed page
- Updated chassis ground connections
- 04/11/2005 - Pin swapped DDR2 according to layout
- 04/12/2005 - Changed audio caps to X5R (CA050, CA051)
- Updated wireless connector pinout according to flex
- Implemented more DDR2 pin swaps
- Implemented pin swaps on FW data lines
- Added RMI I2C pull-downs
- Corrected mosF line and neck width properties
- 04/14/2005 - Switched GPU to M11
- 04/15/2005 - Added CPU Vcore mux circuit
- Added NO TEST property to buses between JTAG enabled devices
- 04/19/2005 - Pin swapped FB 1/2 for M11
- Corrected ENET power rail to PWRON instead of RUN (Wake-on-LAN)
- Corrected Vesta reset and Ethernet LOWPWR circuits
- Changed R5880 to 6.34K to take GPU Vcore to 1.3V/1.05V
- Added page 6 and modified pages 11, 35, 81 for design specific pin swaps
- 04/26/2005 - Separated GPU MVRREF into two dividers
- Added LVDS electrical constraint set properties
- 04/27/2005 - Added NO TEST property to SI TMD5 DP-2 (no room for TP)
- Changed MIN NECK WIDTH property on TMD5 power rails to 0.2 mm
- Changed gender of debug connector
- Removed C567 due to MDO violation
- 04/29/2005 - Schematic released as REV 01 for PROTO

EVT

- 05/04/2005 - Added SYNONYMS to allow DVO and USB pull-down pin-swaps
- 05/09/2005 - Added missing pullup to SYS LID OPEN
- Added missing pull-down to Vesta-LPWR 1394
- 05/16/2005 - Lead-free resistor replacement on page 86
- Various lead-free replacements
- 05/17/2005 - Added Hynix VRAM option and PCBAs
- 05/25/2005 - Added 2 0.1uF caps to VCA sync buffers
- Added NEC USB2 controller and PCI clock buffer
- Various lead-free replacements
- 05/26/2005 - Added pullup to BATT0 DET
- 05/31/2005 - Added 2 0.1uF caps to GPU Vcore output
- 06/01/2005 - Corrected USB diff. pair and spacing/physical rules on ports
- Corrected caps on fire/wire rail to 50V
- Various lead-free replacements

DVT

- 06/28/2005 - Added 10K pullup to VIA REQ L
- Changed Q2941 to level shift/pass FET to correct GPU VCore and CPU Vcore power sequencing
- Moved R2943 to SYS PWRSE01 L to correct trackpad power state in sleep
- Moved R2943 to SYS PWRSE01 L to correct pumpup problem in sleep
- Changed to USBIF1 NEC BOMOPTION
- 07/06/2005 - Various Pb-free replacements
- Changed TMS drive strength resistors to 301 ohm, which was built at EVT
- 07/08/2005 - Added FET to allow PMU control of trackpad power sequencing
- 07/09/2005 - Added resistor mux for I2S MAXBUS I/O rail (PWRON vs RUN)
- Changed CPU Vcore to 2-states only (no MUX)
- Removed I2S connection to TSEN (leakage path)
- Changed 32.768kHz crystal to new APN specifying 1uW drive parts
- 07/14/2005 - Added line width constraints to LTL1625 and CPU Vcore gate nodes
- 07/18/2005 - Added external 1K pullups in parallel with all I2 internal pullups
- Changed NEC USB2 series R value to 39.2 ohm
- Changed 150 ohm pull-downs to FW Ctrl lines at Vesta
- Changed TMS transmitter ferrites to part with higher current rating (1.5A)
- Added BOMOPTIONs for and stuffed CPU Vcore at 1.28V and 1.30V
- 07/19/2005 - Added audio mute sequencing FETs
- Moved U1A DRYORE cap to other side of series resistor
- 07/22/2005 - Released as REV 06 for DVT
- Changed I2 external I2 GPIO pullups to 10K
- Stuffed R2452, R2462, R2463 to correct I2 2.5v pullup problem
- 07/25/2005 - Released as REV 04 for DVT
- Replaced 371S0299 with 371S0300
- Swapped I2 MAXBUS 130HM and I2 MAXBUS 500HM BOMOPTIONs
- Changed to Vesta v1.4 as primary 08500 Vesta v1.3 as alternate
- 07/26/2005 - Changed PCI AD8 output series term to 22 ohms
- 07/29/2005 - Swapped locations (i.e. values) of C2500 and C2501
- 08/03/2005 - Released as REV 05 for DVT
- Added R3772 on CPU0 JTAG TCK 10K pull down (no stuff).
- Changed C1721 and C2205 to 2200pF.
- Changed C1730 to 5.6pF
- Changed C1700 and C1701 and C2215 and C2216 to 47uF.
- Changed R1720 and R2205 to 7.5K.
- Released as REV 06 for DVT

Pre-PVT

- 08/16/2005 - Replaced C3940-C3947 with ceramic caps
- 08/17/2005 - Changed power supply solder jumpers to shorts
- Added five ceramic caps to VcoreB supply input
- Changed D1460 D1461 to 60V schotcky to reduce reverse leakage
- 08/18/2005 - Changed R2958 to 10K to improve power sequencing timing
- 08/22/2005 - Added FETs to control leakage on Vesta rails
- 08/24/2005 - Changed C8600-C8601 to 100K due to FET isolation
- Changed R5822 to 100K for power sequencing improvements
- Added R2959 for power sequencing improvements
- Released as REV 07 for Pre-PVT

PVT

- 08/29/2005 - Released as REV A for PVT/Production
- 09/02/2005 - Stuffed R8420 with 10K 5% to ensure MDIO logic levels
- Stuffed R2464 to correct unused GPIO logic level

E

SYNC_MASTER=N/A SYNC_DATE=N/A


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	D	051-6839	E
SCALE	SHT	OF	
NONE	5	115	

	8	7	6	5	4	3	2	1	
D	<h3>I2S Series Rs</h3> <pre> MAKE_BASE=TRUE 22 I2S0_SB_TO_DEV.DTO_R == RP1150P1 11 11 ==RP1150P8 == I2S0_SB_TO_DEV.DTO 7 74 MAKE_BASE=TRUE MAKE_BASE=TRUE 22 I2S0_BITCLK_R == RP1150P2 11 11 ==RP1150P7 == I2S0_BITCLK 7 74 MAKE_BASE=TRUE MAKE_BASE=TRUE 22 I2S0_MCLK_R == RP1150P3 11 11 ==RP1150P6 == I2S0_MCLK 7 74 MAKE_BASE=TRUE MAKE_BASE=TRUE 22 I2S0_SYNC_R == RP1150P4 11 11 ==RP1150P5 == I2S0_SYNC 7 74 MAKE_BASE=TRUE MAKE_BASE=TRUE 22 I2S1_SB_TO_DEV.DTO_R == RP1151P1 11 11 ==RP1151P8 == I2S1_SB_TO_DEV.DTO 30 MAKE_BASE=TRUE MAKE_BASE=TRUE 22 I2S1_SYNC_R == RP1151P2 11 11 ==RP1151P7 == I2S1_SYNC 30 MAKE_BASE=TRUE MAKE_BASE=TRUE 22 I2S1_MCLK_R == RP1151P3 11 11 ==RP1151P6 == I2S1_MCLK 30 MAKE_BASE=TRUE MAKE_BASE=TRUE 22 I2S1_BITCLK_R == RP1151P4 11 11 ==RP1151P5 == I2S1_BITCLK 30 MAKE_BASE=TRUE </pre>				<h3>Lower DVO Series Rs</h3> <pre> MAKE_BASE=TRUE 53 GPU_DVOD_R<0> == RP6720P1 54 54 ==RP6720P8 == GPU_DVOD<0> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<1> == RP6720P2 54 54 ==RP6720P7 == GPU_DVOD<1> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<2> == RP6720P3 54 54 ==RP6720P6 == GPU_DVOD<2> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<3> == RP6720P4 54 54 ==RP6720P5 == GPU_DVOD<3> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<11> == RP6721P1 54 54 ==RP6721P8 == GPU_DVOD<11> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<10> == RP6721P2 54 54 ==RP6721P7 == GPU_DVOD<10> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<9> == RP6721P3 54 54 ==RP6721P6 == GPU_DVOD<9> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<8> == RP6721P4 54 54 ==RP6721P5 == GPU_DVOD<8> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<6> == RP6722P1 54 54 ==RP6722P8 == GPU_DVOD<6> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<4> == RP6722P2 54 54 ==RP6722P7 == GPU_DVOD<4> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<7> == RP6722P3 54 54 ==RP6722P6 == GPU_DVOD<7> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<5> == RP6722P4 54 54 ==RP6722P5 == GPU_DVOD<5> 54 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVO_HSYNC_R == RP6723P1 54 54 ==RP6723P8 == GPU_DVO_HSYNC 54 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVO_VSYNC_R == RP6723P2 54 54 ==RP6723P7 == GPU_DVO_VSYNC 54 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVO_DE_R == RP6723P3 54 54 ==RP6723P6 == GPU_DVO_DE 54 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVO_CLKP_R == RP6723P4 54 54 ==RP6723P5 == GPU_DVO_CLKP 54 55 MAKE_BASE=TRUE </pre>				D
C	<h3>UATA Series Rs</h3> <pre> MAKE_BASE=TRUE 63 UATA_DD_R<12> == RP8150P1 63 63 ==RP8150P8 == UATA_DD<12> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_CS0_L_R == RP8150P2 63 63 ==RP8150P7 == UATA_CS0_L 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<14> == RP8150P3 63 63 ==RP8150P6 == UATA_DD<14> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<11> == RP8150P4 63 63 ==RP8150P5 == UATA_DD<11> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<7> == RP8151P1 63 63 ==RP8151P8 == UATA_DD<7> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<2> == RP8151P2 63 63 ==RP8151P7 == UATA_DD<2> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<3> == RP8151P3 63 63 ==RP8151P6 == UATA_DD<3> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<15> == RP8151P4 63 63 ==RP8151P5 == UATA_DD<15> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<9> == RP8152P1 63 63 ==RP8152P8 == UATA_DD<9> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<4> == RP8152P2 63 63 ==RP8152P7 == UATA_DD<4> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<6> == RP8152P3 63 63 ==RP8152P6 == UATA_DD<6> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<5> == RP8152P4 63 63 ==RP8152P5 == UATA_DD<5> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DA_R<2> == RP8153P1 63 63 ==RP8153P8 == UATA_DA<2> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<8> == RP8153P2 63 63 ==RP8153P7 == UATA_DD<8> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<10> == RP8153P3 63 63 ==RP8153P6 == UATA_DD<10> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DA_R<0> == RP8153P4 63 63 ==RP8153P5 == UATA_DA<0> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<13> == RP8154P1 63 63 ==RP8154P8 == UATA_DD<13> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<0> == RP8154P2 63 63 ==RP8154P7 == UATA_DD<0> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DD_R<1> == RP8154P3 63 63 ==RP8154P6 == UATA_DD<1> 7 63 64 MAKE_BASE=TRUE MAKE_BASE=TRUE 63 UATA_DA_R<1> == RP8154P4 63 63 ==RP8154P5 == UATA_DA<1> 7 63 64 MAKE_BASE=TRUE </pre>				<h3>Upper DVO Series Rs</h3> <pre> MAKE_BASE=TRUE 53 GPU_DVOD_R<13> == RP6821P1 55 55 ==RP6821P8 == GPU_DVOD<13> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<12> == RP6821P2 55 55 ==RP6821P7 == GPU_DVOD<12> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<14> == RP6821P3 55 55 ==RP6821P6 == GPU_DVOD<14> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<15> == RP6821P4 55 55 ==RP6821P5 == GPU_DVOD<15> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<18> == RP6822P1 55 55 ==RP6822P8 == GPU_DVOD<18> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<19> == RP6822P2 55 55 ==RP6822P7 == GPU_DVOD<19> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<16> == RP6822P3 55 55 ==RP6822P6 == GPU_DVOD<16> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<17> == RP6822P4 55 55 ==RP6822P5 == GPU_DVOD<17> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<21> == RP6823P1 55 55 ==RP6823P8 == GPU_DVOD<21> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<20> == RP6823P2 55 55 ==RP6823P7 == GPU_DVOD<20> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<23> == RP6823P3 55 55 ==RP6823P6 == GPU_DVOD<23> 55 MAKE_BASE=TRUE MAKE_BASE=TRUE 53 GPU_DVOD_R<22> == RP6823P4 55 55 ==RP6823P5 == GPU_DVOD<22> 55 MAKE_BASE=TRUE </pre>				C
B	<h3>MAXBUS Pullups</h3> <pre> MAKE_BASE=TRUE 33 MAXBUS_TS_L == RP3510P1 32 32 MAKE_BASE=TRUE 33 MAXBUS_CPU1_BG_L == RP3510P2 32 32 MAKE_BASE=TRUE 33 MAXBUS_CPU0_DBG_L == RP3510P3 32 32 MAKE_BASE=TRUE 33 NC_MAXBUS_TREN_I2_NO_TEST=YES == RP3510P4 32 32 MAKE_BASE=TRUE 33 MAXBUS_CPU0_BG_L == RP3511P1 32 32 MAKE_BASE=TRUE 33 MAXBUS_CPU1_HIT_L == RP3511P2 32 32 MAKE_BASE=TRUE 33 MAXBUS_CPU0_HIT_L == RP3511P3 32 32 MAKE_BASE=TRUE 33 MAXBUS_CPU0_BR_L == RP3511P4 32 32 MAKE_BASE=TRUE 33 MAXBUS_CPU1_BR_L == RP3512P1 32 32 MAKE_BASE=TRUE 33 MAXBUS_TA_L == RP3512P2 32 32 MAKE_BASE=TRUE 34 MAXBUS_CPU0_INT_L == RP3512P3 32 32 MAKE_BASE=TRUE 33 MAXBUS_CPU1_INT_L == RP3512P4 32 32 MAKE_BASE=TRUE 33 MAXBUS_CPU0_DRDY_L == RP3513P2 32 32 MAKE_BASE=TRUE 33 MAXBUS_CPU1_DRDY_L == RP3513P3 32 32 MAKE_BASE=TRUE 33 MAXBUS_AACK_L == RP3513P4 32 32 MAKE_BASE=TRUE 33 MAXBUS_ARTRY_L == RP3514P1 32 32 MAKE_BASE=TRUE 33 MAXBUS_CPU1_DBG_L == RP3514P2 32 32 MAKE_BASE=TRUE 33 MAXBUS_TEA_L == RP3514P3 32 32 </pre>		<h3>AGP Pullups</h3> <pre> MAKE_BASE=TRUE 44 AGP_TRDY_L == RP5610P1 43 43 MAKE_BASE=TRUE 44 AGP_IRDY_L == RP5610P2 43 43 MAKE_BASE=TRUE 44 AGP_REQ_L == RP5610P3 43 43 MAKE_BASE=TRUE 44 AGP_RBF_L == RP5610P4 43 43 MAKE_BASE=TRUE 44 AGP_FRAME_L == RP5611P1 43 43 MAKE_BASE=TRUE 44 AGP_DEVSEL_L == RP5611P2 43 43 MAKE_BASE=TRUE 44 AGP_STOP_L == RP5611P3 43 43 MAKE_BASE=TRUE 44 AGP_GNT_L == RP5611P4 43 43 </pre>		<h3>USB Pulldowns</h3> <pre> 72 ==RP9210P8 == USB2_I2_LEFT_PORT_P 11 MAKE_BASE=TRUE 72 ==RP9210P7 == USB2_I2_LEFT_PORT_N 11 MAKE_BASE=TRUE 72 ==RP9210P6 == USB2_I2_P<1> 72 MAKE_BASE=TRUE 72 ==RP9210P5 == USB2_I2_N<1> 72 MAKE_BASE=TRUE 72 ==RP9211P8 == USB2_I2_RIGHT_PORT_P 11 MAKE_BASE=TRUE 72 ==RP9211P7 == USB2_I2_RIGHT_PORT_N 11 MAKE_BASE=TRUE 72 ==RP9211P6 == USB2_I2_P<3> 72 MAKE_BASE=TRUE 72 ==RP9211P5 == USB2_I2_N<3> 72 MAKE_BASE=TRUE 72 ==RP9212P8 == USB_I2_BT_P 11 MAKE_BASE=TRUE 72 ==RP9212P7 == USB_I2_BT_N 11 MAKE_BASE=TRUE 72 ==RP9212P6 == USB_I2_TPAD_P 11 MAKE_BASE=TRUE 72 ==RP9212P5 == USB_I2_TPAD_N 11 MAKE_BASE=TRUE 72 ==RP9300P8 == USB2_NEC_LEFT_PORT_P 11 MAKE_BASE=TRUE 72 ==RP9300P7 == USB2_NEC_LEFT_PORT_N 11 MAKE_BASE=TRUE 72 ==RP9300P6 == USB2_NEC_RIGHT_PORT_N 11 MAKE_BASE=TRUE 72 ==RP9300P5 == USB2_NEC_RIGHT_PORT_P 11 MAKE_BASE=TRUE 72 ==RP9301P8 == USB_NEC_BT_P 11 MAKE_BASE=TRUE 72 ==RP9301P7 == USB_NEC_BT_N 11 MAKE_BASE=TRUE 72 ==RP9301P6 == USB_NEC_TPAD_N 11 MAKE_BASE=TRUE 72 ==RP9301P5 == USB_NEC_TPAD_P 11 MAKE_BASE=TRUE </pre>		B		
A	<h3>FW Series Rs</h3> <pre> MAKE_BASE=TRUE 68 9 FW_D_R<3> == RP9100P1 71 71 ==RP9100P8 == FW_D<3> 9 69 MAKE_BASE=TRUE MAKE_BASE=TRUE 68 9 FW_D_R<1> == RP9100P2 71 71 ==RP9100P7 == FW_D<1> 9 69 MAKE_BASE=TRUE MAKE_BASE=TRUE 68 9 FW_D_R<0> == RP9100P3 71 71 ==RP9100P6 == FW_D<0> 9 69 MAKE_BASE=TRUE MAKE_BASE=TRUE 68 9 FW_D_R<2> == RP9100P4 71 71 ==RP9100P5 == FW_D<2> 9 69 MAKE_BASE=TRUE MAKE_BASE=TRUE 68 9 FW_D_R<7> == RP9101P1 71 71 ==RP9101P8 == FW_D<7> 9 69 MAKE_BASE=TRUE MAKE_BASE=TRUE 68 9 FW_D_R<5> == RP9101P2 71 71 ==RP9101P7 == FW_D<5> 9 69 MAKE_BASE=TRUE MAKE_BASE=TRUE 68 9 FW_D_R<6> == RP9101P3 71 71 ==RP9101P6 == FW_D<6> 9 69 MAKE_BASE=TRUE MAKE_BASE=TRUE 68 9 FW_D_R<4> == RP9101P4 71 71 ==RP9101P5 == FW_D<4> 9 69 MAKE_BASE=TRUE </pre>				A				

Q41C Pin Swaps

SYNC_MASTER=N/A SYNC_DATE=N/A

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SCALE	NONE	SHT	6 OF 115

Enhanced MAC-1 Test Coverage

Functional test points use a P6 pad placed on bottom side.

Category	Test Point	Pin	Function	Notes	
POWER	PP24V_ADAPTER	10	FUNC_TEST=YES	Place 2 TPs @ connector.	
	PP24V_ALL_PBUS_A	10	FUNC_TEST=YES		
	PP12V8_ALL_PBUS_B	10	FUNC_TEST=YES		
	PPVCORE_RUN_GPU	10	FUNC_TEST=YES		
	PPVCORE_RUN_CPU	10	FUNC_TEST=YES	Place within 50 mm of power supply.	
	PP1V8_PWRON	10	FUNC_TEST=YES		
	PP2V5_PWRON	10	FUNC_TEST=YES		
	PP5V_PWRON	10	FUNC_TEST=YES		
	PP3V3_PWRON	10	FUNC_TEST=YES	Place 5-10 GND TPs.	
	PP5V_RUN	10	FUNC_TEST=YES		
	PP3V3_ALL	10	FUNC_TEST=YES		
	=FTP_GND	7 10	FUNC_TEST=YES		
	LVDS	LVDS_U0_P	53 56	FUNC_TEST=YES	Place within 25 mm of LVDS connector.
		LVDS_U0_N	53 56	FUNC_TEST=YES	
LVDS_U1_P		53 56	FUNC_TEST=YES		
LVDS_U1_N		53 56	FUNC_TEST=YES		
LVDS_U2_P		53 56	FUNC_TEST=YES		
LVDS_U2_N		53 56	FUNC_TEST=YES		
CLKLVDS_U_P		53 56	FUNC_TEST=YES		
CLKLVDS_U_N		53 56	FUNC_TEST=YES		
LVDS_L0_P		53 56	FUNC_TEST=YES		
LVDS_L0_N		53 56	FUNC_TEST=YES		
LVDS_L1_P		53 56	FUNC_TEST=YES		
LVDS_L1_N		53 56	FUNC_TEST=YES		
LVDS_L2_P		53 56	FUNC_TEST=YES		
LVDS_L2_N		53 56	FUNC_TEST=YES		
CLKLVDS_L_P		53 56	FUNC_TEST=YES		
CLKLVDS_L_N		53 56	FUNC_TEST=YES		
LVDS_DDC_CLK		51 56	FUNC_TEST=YES		
LVDS_DDC_DATA		51 56	FUNC_TEST=YES		
=PP3V3_DDC_LCD	10 56	FUNC_TEST=YES			
PP3V3_LCD_CONN	56	FUNC_TEST=YES			
INVERTER	PPBUS_INVERTER	56	FUNC_TEST=YES	Place within 25 mm of inverter connector.	
	PP5V_INV_SW	56	FUNC_TEST=YES		
	BRIGHT_PWM	56	FUNC_TEST=YES		
	GND_INVERTER	56	FUNC_TEST=YES		
UATA	=PP5V_RUN_ODD	10 64	FUNC_TEST=YES	Place within 50 mm of ODD/HDD connector.	
	=PP5V_RUN_HDD	10 64	FUNC_TEST=YES		
	PP3V3R5V_RUN_HDD_LOGIC	64	FUNC_TEST=YES		
	UATA_DD<15..0>	6 63 64	FUNC_TEST=YES		
	UATA_DMAR0	63 64	FUNC_TEST=YES		
	UATA_DSTROBE	63 64	FUNC_TEST=YES		
	UATA_DMACK_L	63 64	FUNC_TEST=YES		
	UATA_DA<2..0>	6 63 64	FUNC_TEST=YES		
	UATA_CS0_L	6 63 64	FUNC_TEST=YES		
	UATA_CS1_L	63 64	FUNC_TEST=YES		
	UATA_RESET_L	63 64	FUNC_TEST=YES		
	UATA_HSTROBE	63 64	FUNC_TEST=YES		
	UATA_STOP	63 64	FUNC_TEST=YES		
	UATA_INTRQ	63 64	FUNC_TEST=YES		
AUDIO	PP5V_PWRON_AUDIO_PVDD	74	FUNC_TEST=YES	Place within 25 mm of audio connector.	
	PP5V_PWRON_AUDIO_AVDD	74	FUNC_TEST=YES		
	PP3V3_PWRON_AUDIO_AVDD	74	FUNC_TEST=YES		
	=PP3V3_RUN_AUDIO	10 74	FUNC_TEST=YES		
	=I2C_AUDIO_SCL	8 74	FUNC_TEST=YES		
	=I2C_AUDIO_SDA	8 74	FUNC_TEST=YES		
	I2S0_MCLK	6 74	FUNC_TEST=YES		
	I2S0_BITCLK	6 74	FUNC_TEST=YES		
	I2S0_SYNC	6 74	FUNC_TEST=YES		
	I2S0_SB_TO_DEV_DTO	6 74	FUNC_TEST=YES		
	I2S0_DEV_TO_SB_DTI	22 74	FUNC_TEST=YES		
	AUDIO_LO_MUTE_L	22 74	FUNC_TEST=YES		
	AUDIO_SPKR_MUTE_L	22 74	FUNC_TEST=YES		
	AUDIO_CODEC_RESET_L	22 74	FUNC_TEST=YES		
	AUDIO_SPDIFRX_RESET_L	22 74	FUNC_TEST=YES		
	AUDIO_LO_DET_L	22 74	FUNC_TEST=YES		
	AUDIO_LI_DET_L	22 74	FUNC_TEST=YES		
	AUDIO_LO_OPTICAL_PLUG_L	22 74	FUNC_TEST=YES		
AUDIO_LI_OPTICAL_PLUG_L	22 74	FUNC_TEST=YES			
AUDIO_I2S_DTIB_SEL	22 74	FUNC_TEST=YES			
AUDIO_EXT_MCLK_SEL	22 74	FUNC_TEST=YES			
AUDIO_GPIO_11	22 74	FUNC_TEST=YES			
GND_AUDIO_AGND	74	FUNC_TEST=YES			
GND_AUDIO_PGND	74	FUNC_TEST=YES			

Category	Test Point	Pin	Function	Notes
SYSTEM	PP5V_TPAD_F	30	FUNC_TEST=YES	Place within 25 mm of TPAD connector.
	USB_TPAD_P	11 30	FUNC_TEST=YES	
	USB_TPAD_N	11 30	FUNC_TEST=YES	
	PP3V3_PWRON_DS1775_R	30	FUNC_TEST=YES	
	SYS_OVERTEMP_L	11 25 30	FUNC_TEST=YES	
	PP3V3_ALL_HALL_EFFECT_R	30	FUNC_TEST=YES	
	SYS_LID_OPEN_F	30	FUNC_TEST=YES	
	SYS_POWER_BUTTON_L_F	30	FUNC_TEST=YES	
	=FTP_SLEEP_LED	74	FUNC_TEST=YES	
	SYS_CHARGE_LED_L	24 31	FUNC_TEST=YES	
	SYS_ADAPTER_ANALOG_AC_DET	12 31	FUNC_TEST=YES	
	KBDLED_ANODE	28 30	FUNC_TEST=YES	
	KBDLED_RETURN	28 30	FUNC_TEST=YES	
	=I2C_DS1775_SDA	8 30	FUNC_TEST=YES	
=I2C_DS1775_SCL	8 30	FUNC_TEST=YES		
CPU FAN	=PP5V_FAN1_PWR	10 31	FUNC_TEST=YES	Place within 25 mm of fan connector.
	FAN1_TACH	27 31	FUNC_TEST=YES	
	FAN1_PWM	27 31	FUNC_TEST=YES	
	=FTP_GND	7 10	FUNC_TEST=YES	
GPU FAN	=PP5V_FAN2_PWR	10 31	FUNC_TEST=YES	Place within 25 mm of fan connector.
	FAN2_TACH	27 31	FUNC_TEST=YES	
	FAN2_PWM	27 31	FUNC_TEST=YES	
	=FTP_GND	7 10	FUNC_TEST=YES	
ALS	=PP3V3_PWRON_LEFT_ALS	10 31	FUNC_TEST=YES	Place within 25 mm of ALS connector.
	ALS_0_OUT	25 31	FUNC_TEST=YES	
	ALS_GAIN_BOOST	25 28 31	FUNC_TEST=YES	
SCCA	SCCA_RXD	22 24	FUNC_TEST=YES	Place within 25 mm of debug connector.
	SCCA_TXD_L	22 24	FUNC_TEST=YES	
BACKUP BATT	=PPVIO_BU_BATT	10 31	FUNC_TEST=YES	Place within 25 mm of battery connector.
	=PPVOUT_BU_BATT	10 31	FUNC_TEST=YES	
RT USB	=PP5V_PWRON_RIGHT_USB	10 31	FUNC_TEST=YES	Place within 25 mm of right USB connector.
	USB2_RIGHT_PORT_P	11 31	FUNC_TEST=YES	
	USB2_RIGHT_PORT_N	11 31	FUNC_TEST=YES	
LT USB	=PP5V_PWRON_LEFT_USB	10 31	FUNC_TEST=YES	Place within 25 mm of left USB connector.
	USB2_LEFT_PORT_P	11 31	FUNC_TEST=YES	
	USB2_LEFT_PORT_N	11 31	FUNC_TEST=YES	

Functional Test Points

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NONE	7	115

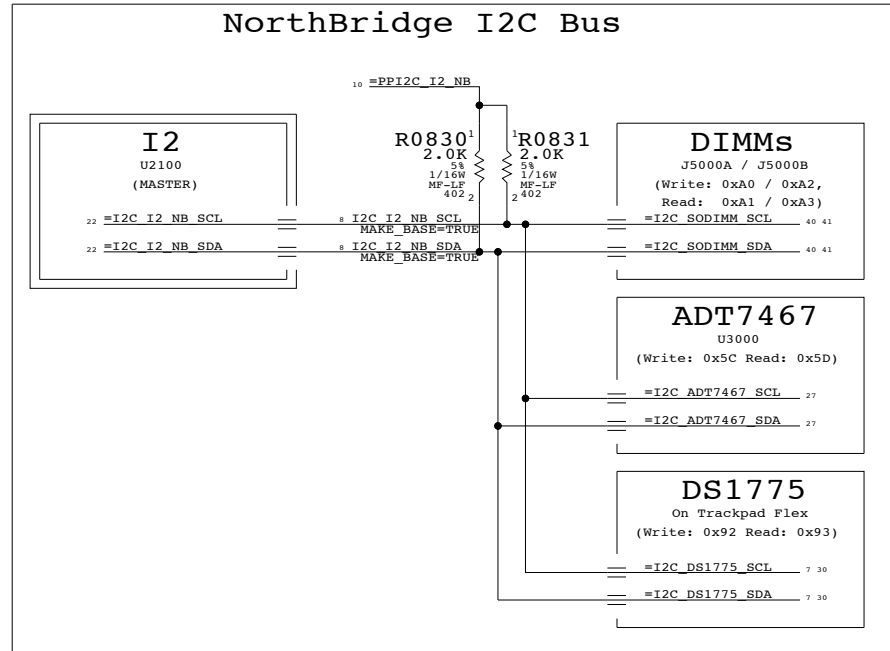
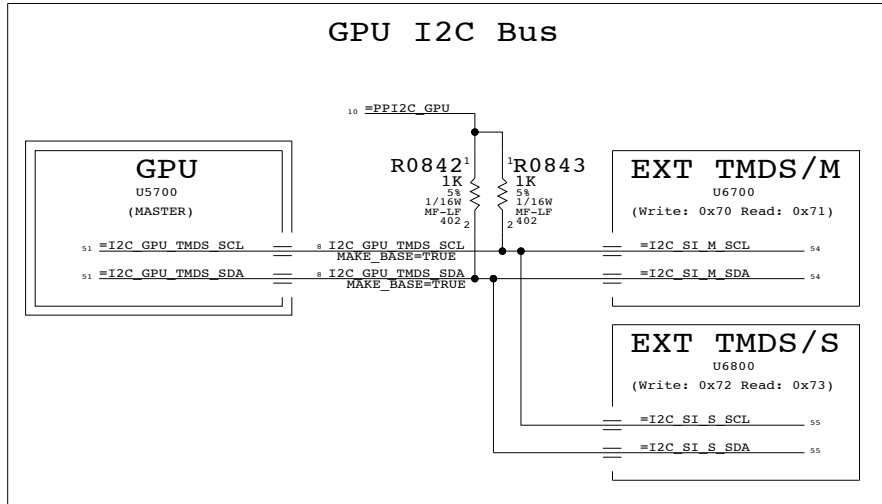
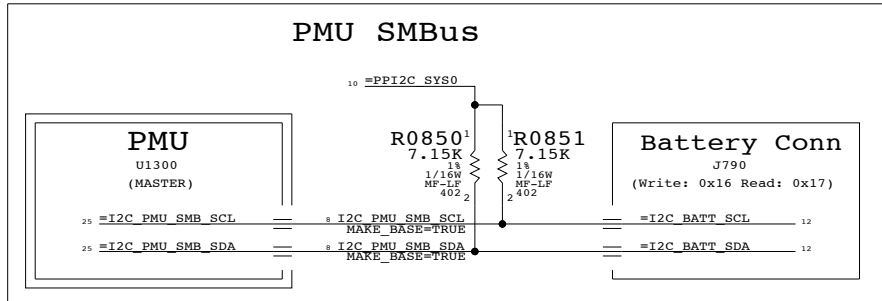
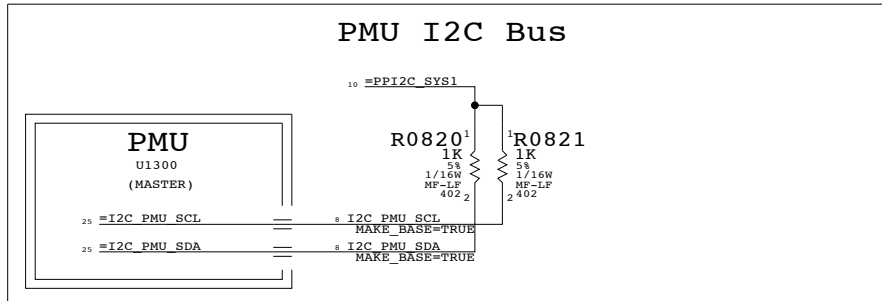
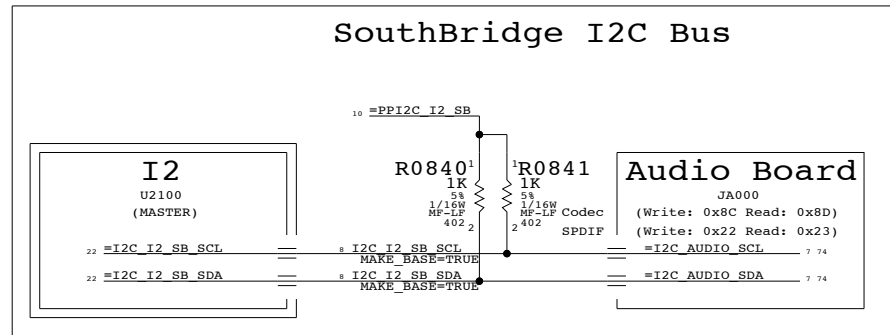
ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
I2C_PMU_SMB_SCL	I2C	I2C	
I2C_PMU_SMB_SDA	I2C	I2C	
I2C_PMU_SCL	I2C	I2C	
I2C_PMU_SDA	I2C	I2C	
I2C_NB	I2C	I2C	
I2C_NB	I2C	I2C	
I2C_I2_SB_SCL	I2C	I2C	
I2C_I2_SB_SDA	I2C	I2C	
I2C_GPU_TMDS_SCL	I2C	I2C	
I2C_GPU_TMDS_SDA	I2C	I2C	

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- GOV_I2C / GOV_I2C_BYPASS
Allows bypassing Governor I2C bus.
Most devices are connected directly to PMU instead. One ADT7467 connects to NB I2C bus 1 to resolve address conflict.
- MMM_PWR_ALL / MMM_PWR_PWRON
Selects whether MMM MCU is powered all the time or only when the system is on. ALL moves the MCU to the PMU I2C bus so it can be monitored by in shutdown.
NOTE: Neither option is necessary when MMM_MCU_PMU BOM option is selected.



I2C Connections

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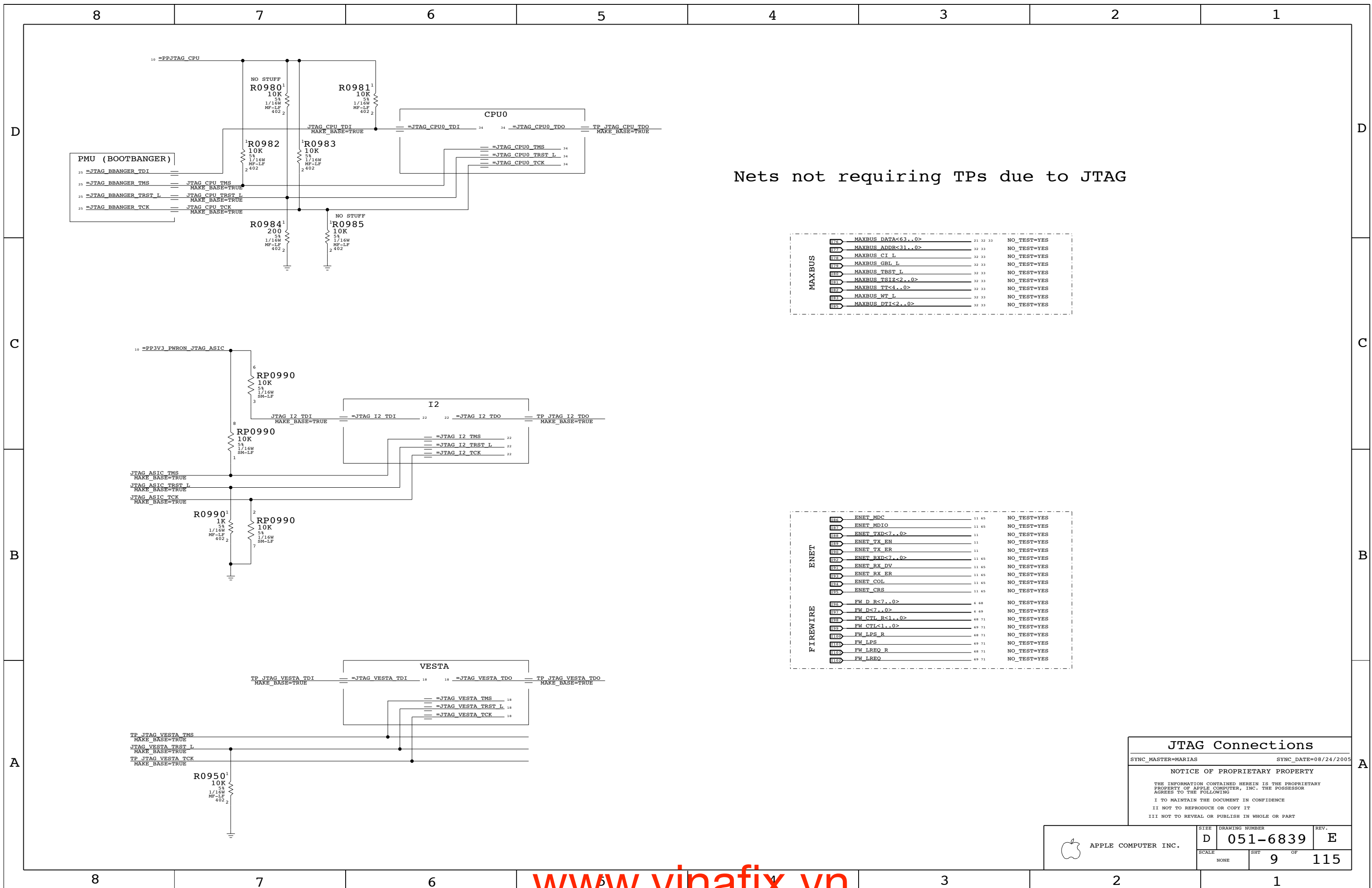
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NONE	8	115	



Nets not requiring TPs due to JTAG

NET	MAXBUS DATA<63..0>	21 32 33	NO_TEST=YES
MAXBUS	MAXBUS ADDR<31..0>	32 33	NO_TEST=YES
MAXBUS	MAXBUS CI L	32 33	NO_TEST=YES
MAXBUS	MAXBUS GBL L	32 33	NO_TEST=YES
MAXBUS	MAXBUS TRST L	32 33	NO_TEST=YES
MAXBUS	MAXBUS TSI<2..0>	32 33	NO_TEST=YES
MAXBUS	MAXBUS TT<4..0>	32 33	NO_TEST=YES
MAXBUS	MAXBUS WT L	32 33	NO_TEST=YES
MAXBUS	MAXBUS DTI<2..0>	32 33	NO_TEST=YES

NET	ENET MDC	11 65	NO_TEST=YES
ENET	ENET MDIO	11 65	NO_TEST=YES
ENET	ENET TXD<7..0>	11	NO_TEST=YES
ENET	ENET TX_EN	11	NO_TEST=YES
ENET	ENET TX_ER	11	NO_TEST=YES
ENET	ENET RXD<7..0>	11 65	NO_TEST=YES
ENET	ENET RX_DV	11 65	NO_TEST=YES
ENET	ENET RX_ER	11 65	NO_TEST=YES
ENET	ENET COL	11 65	NO_TEST=YES
ENET	ENET CRS	11 65	NO_TEST=YES
FIREWIRE	FW D R<7..0>	6 69	NO_TEST=YES
FIREWIRE	FW D<7..0>	6 69	NO_TEST=YES
FIREWIRE	FW CTL R<1..0>	69 71	NO_TEST=YES
FIREWIRE	FW CTL<1..0>	69 71	NO_TEST=YES
FIREWIRE	FW LPS_R	69 71	NO_TEST=YES
FIREWIRE	FW LPS	69 71	NO_TEST=YES
FIREWIRE	FW LREQ_R	69 71	NO_TEST=YES
FIREWIRE	FW LREQ	69 71	NO_TEST=YES

JTAG Connections

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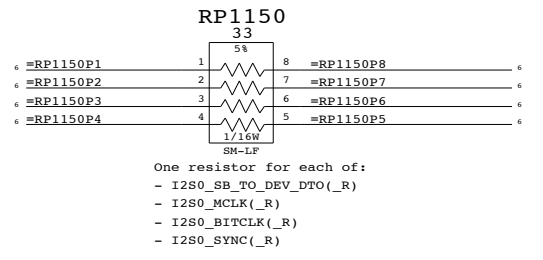
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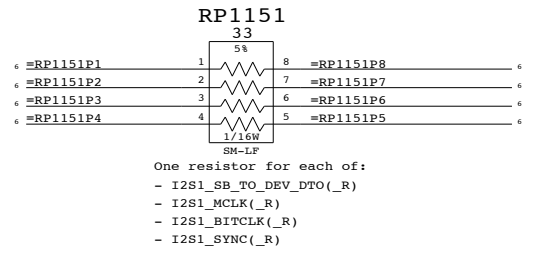
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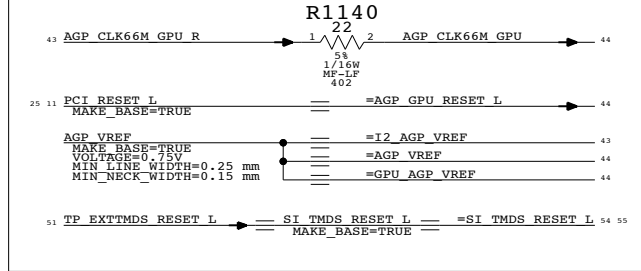
I2S0 Series Rs



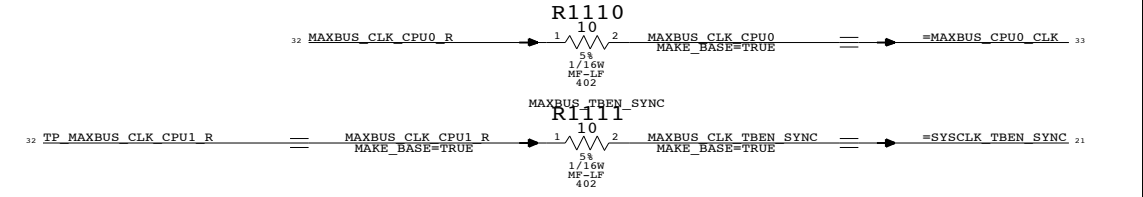
I2S1 Series Rs



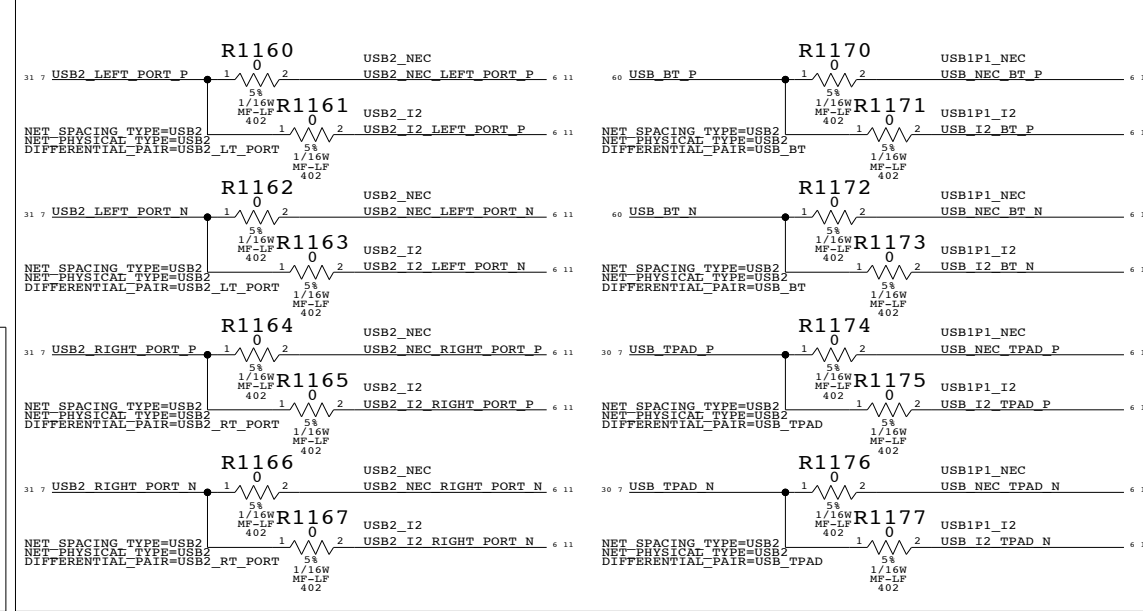
GPU



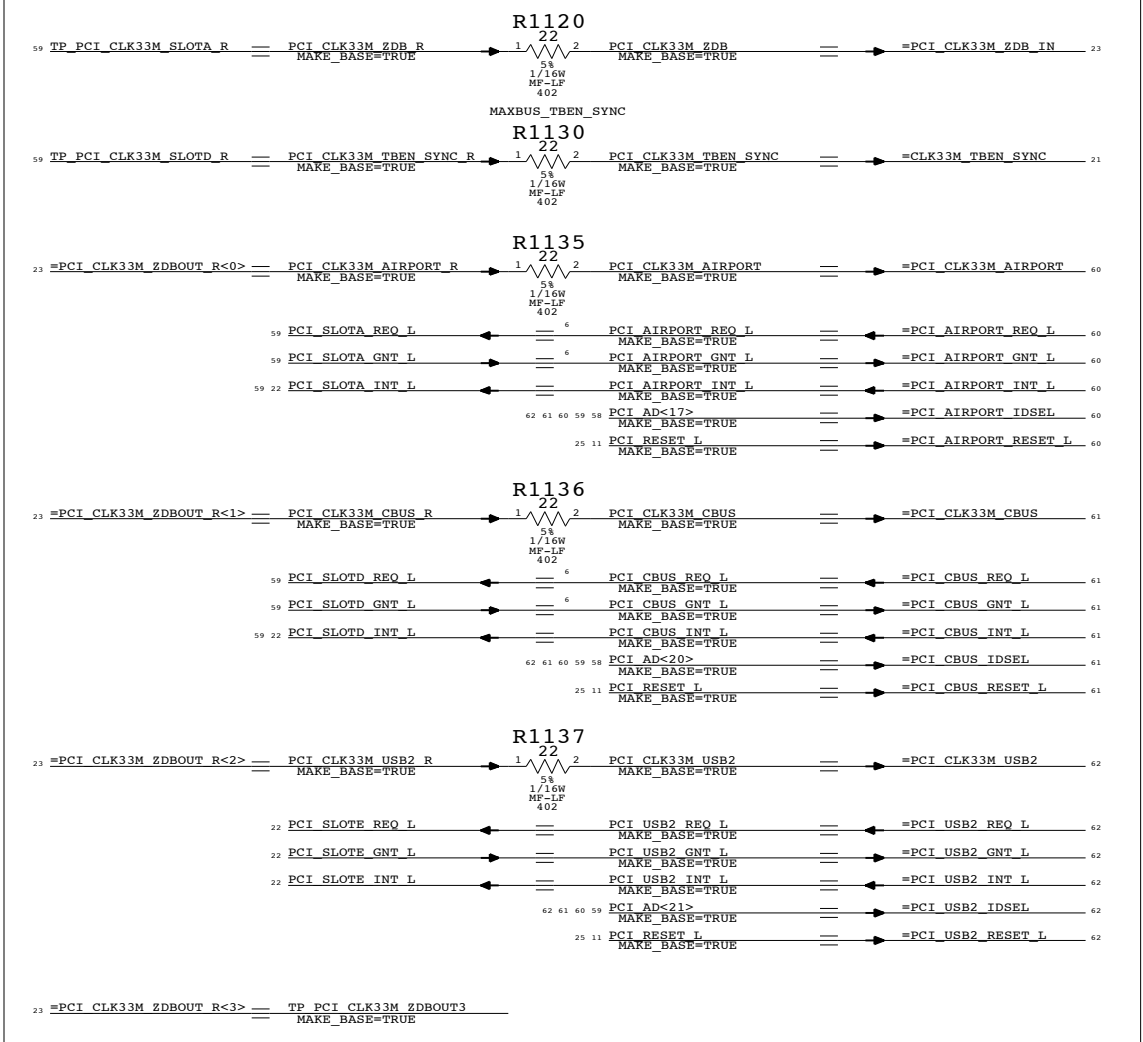
CPU Clocks



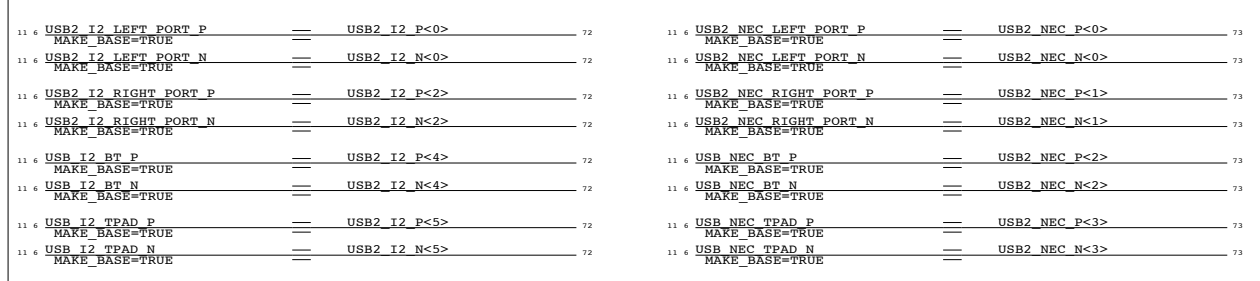
USB Controller Mux



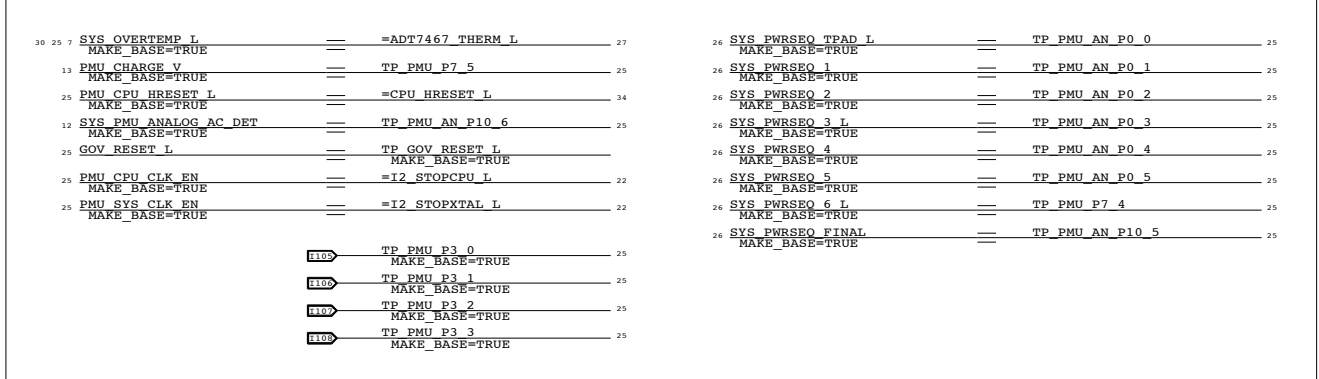
PCI



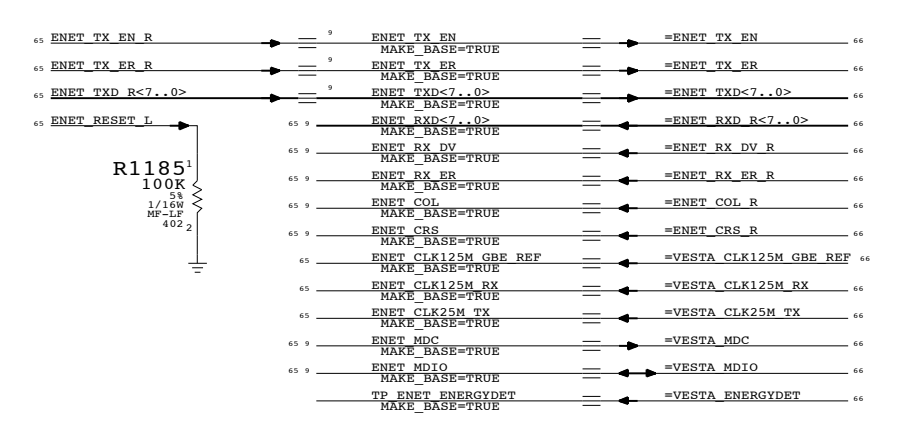
USB Port Assignments



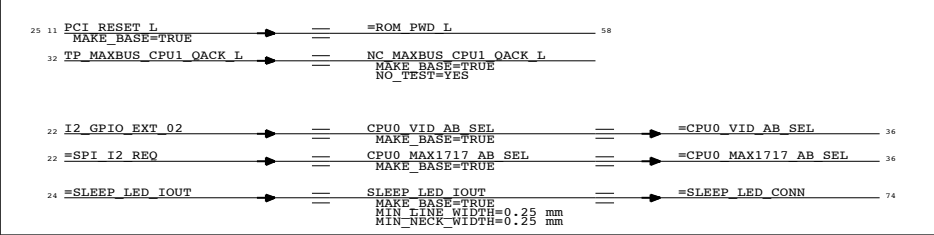
PMU Connections



Vesta Ethernet



MISC



Signal Synonyms

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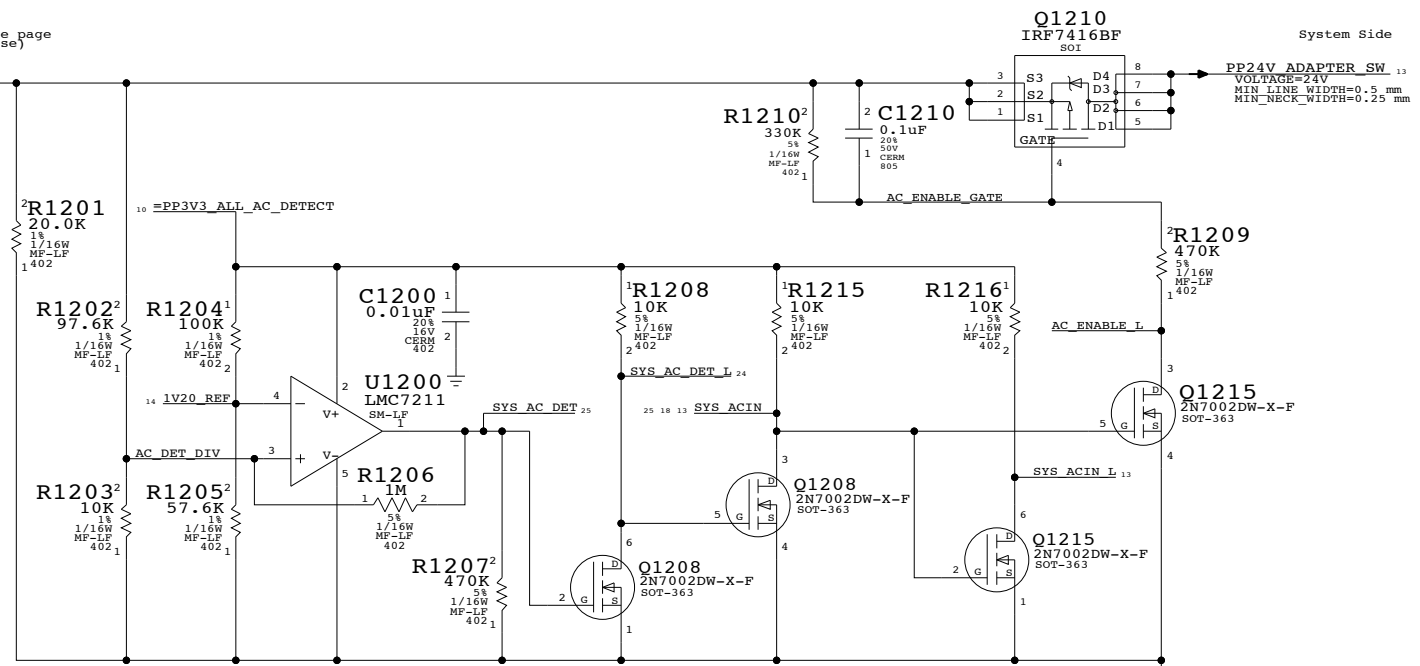
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SCALE	SHEET	OF	
NONE	11	115	

NET_TYPE		SPACING	PHYSICAL	DIFFERENTIAL_PAIR
ELECTRICAL_CONSTRAINT_SET				
BATT	THERM	THERM	BATTERY_ISNS	PPVBATT_ISNS_VINP 12
BATT	THERM	THERM	BATTERY_ISNS	PPVBATT_ISNS_VINN 12

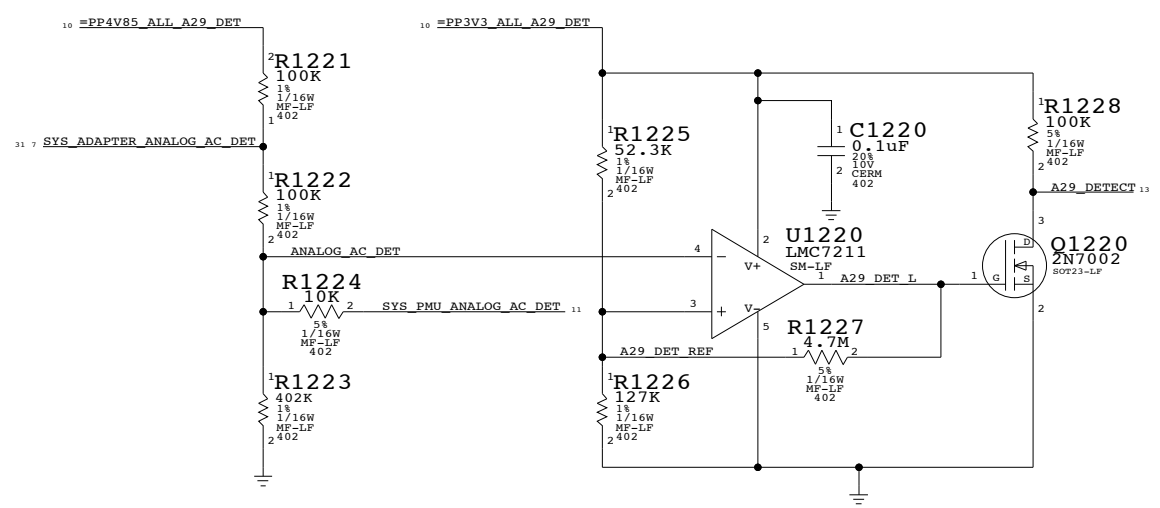
ADAPTER INPUT/INRUSH LIMITER

Adapter Connector Side
(Connector is on separate page to facilitate design reuse)



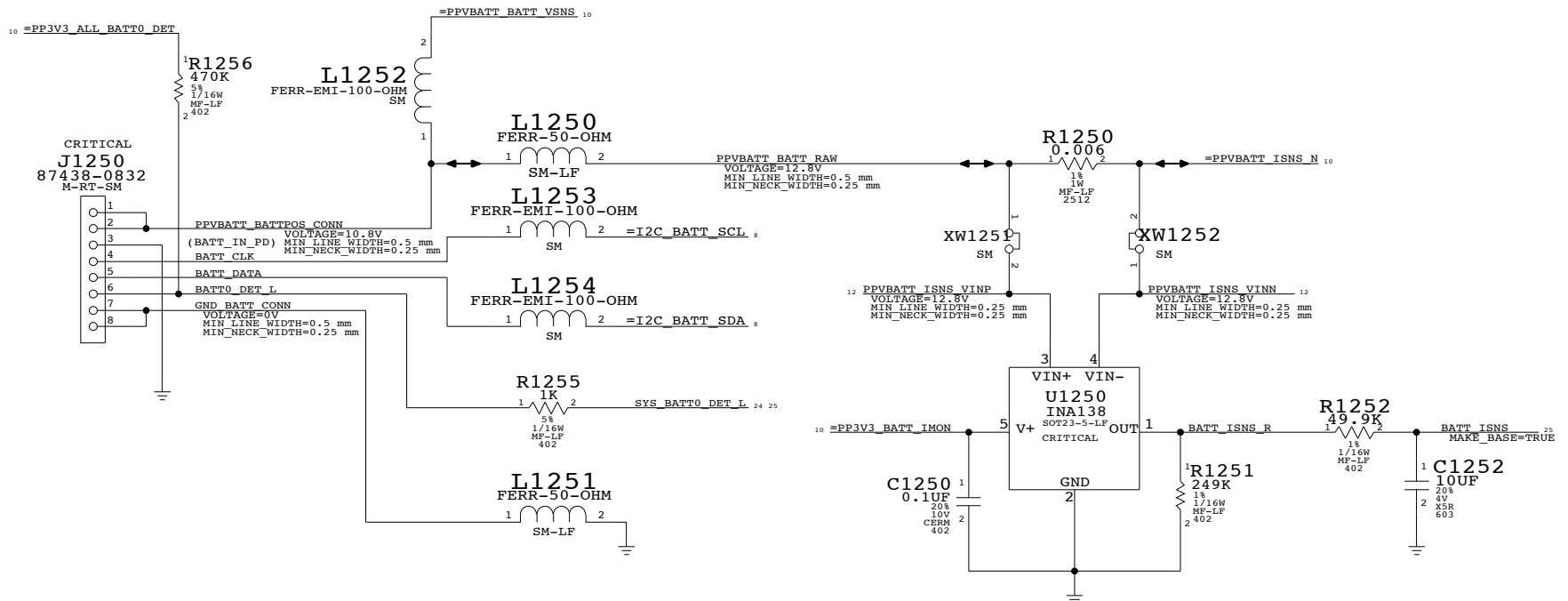
GREATER THAN 13.1V DETECT SYS AC DET indicates adapter presence. SYS ACIN is code-controlled signal to enable use of AC in system. Q1208 ensures SYS ACIN goes low as soon as SYS AC DET goes low. Therefore, hardware immediately disables the AC upon removal but only software can enable AC after detection by the PMU.

A29 ADAPTER DETECTION



ADAPTER IDS		
ADAPTER	ID RANGE	PIN VOLTAGE
Q11 (65W)	1.65-2.31V	2.007-2.066V
A29 (45W)	2.31-2.97V	2.558-2.661V
AIRLINE	0.33-0.99V	0.589-0.663V

BATTERY INPUT/CURRENT SENSE



Power Inputs

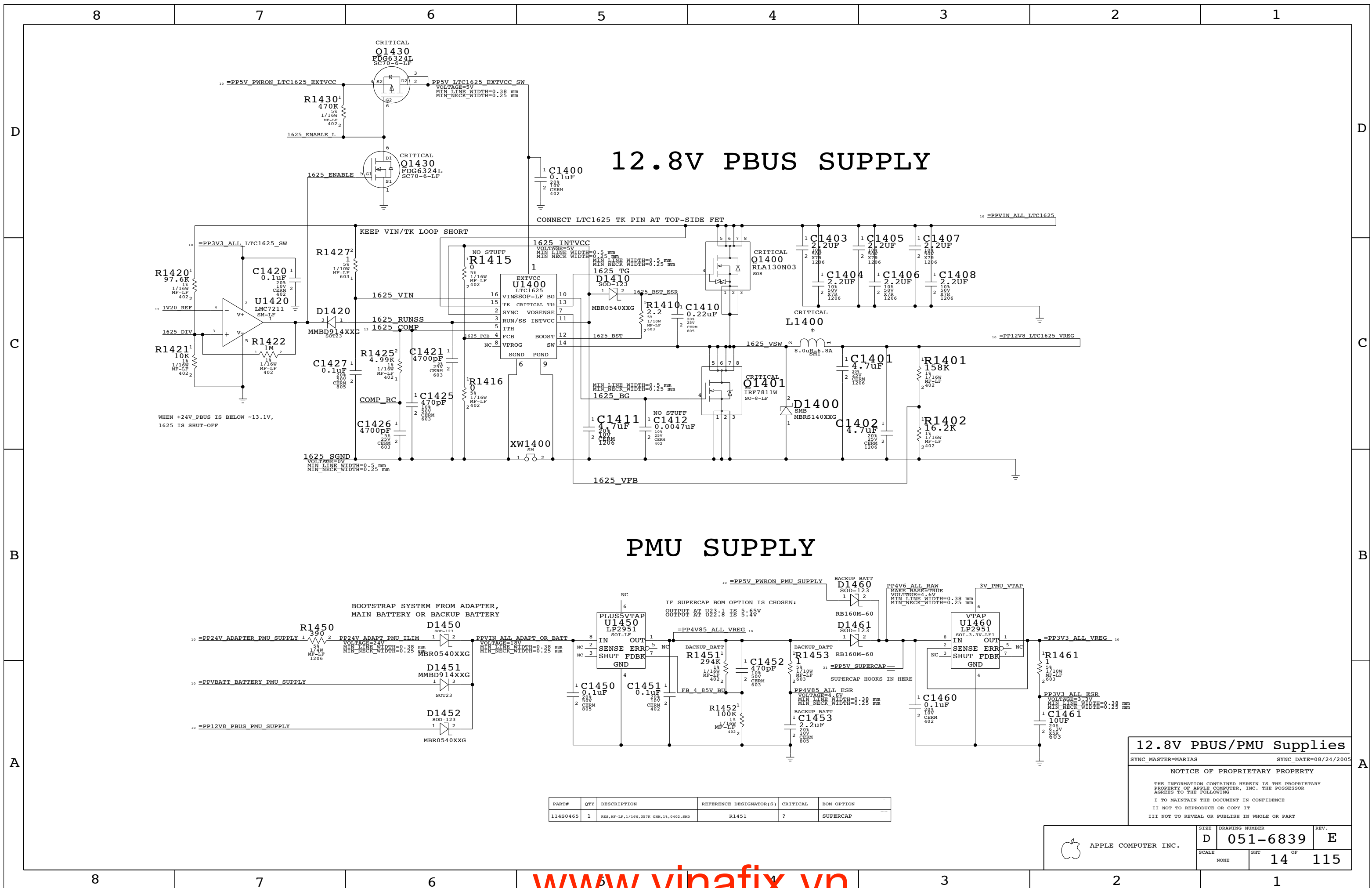
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NONE		12	115



12.8V PBUS SUPPLY

PMU SUPPLY

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
11480465	1	RES, MF-LP, 1/16W, 357K OHM, 1%, 0402, SMD	R1451	?	SUPERCAP

12.8V PBUS/PMU Supplies

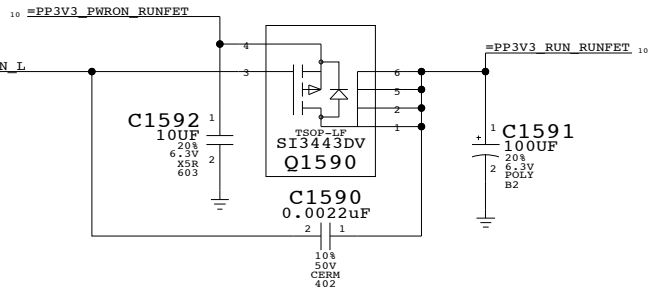
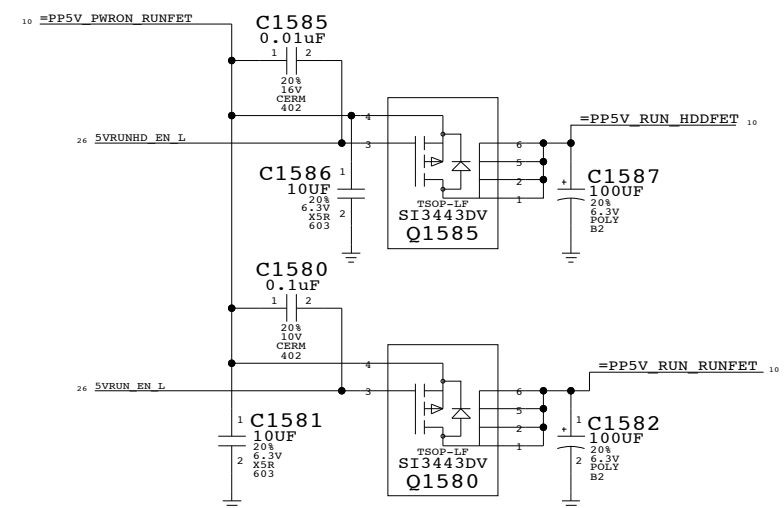
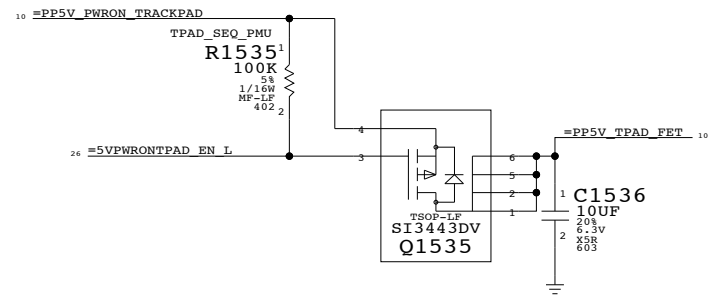
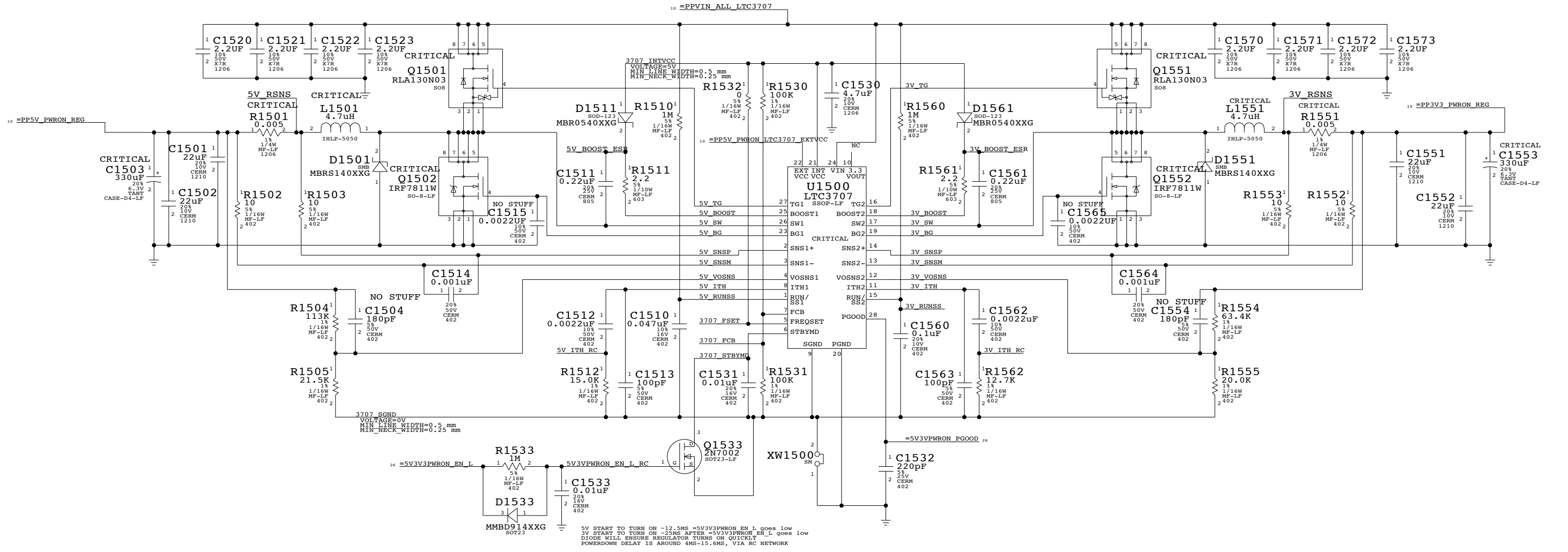
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NONE	14 OF		115

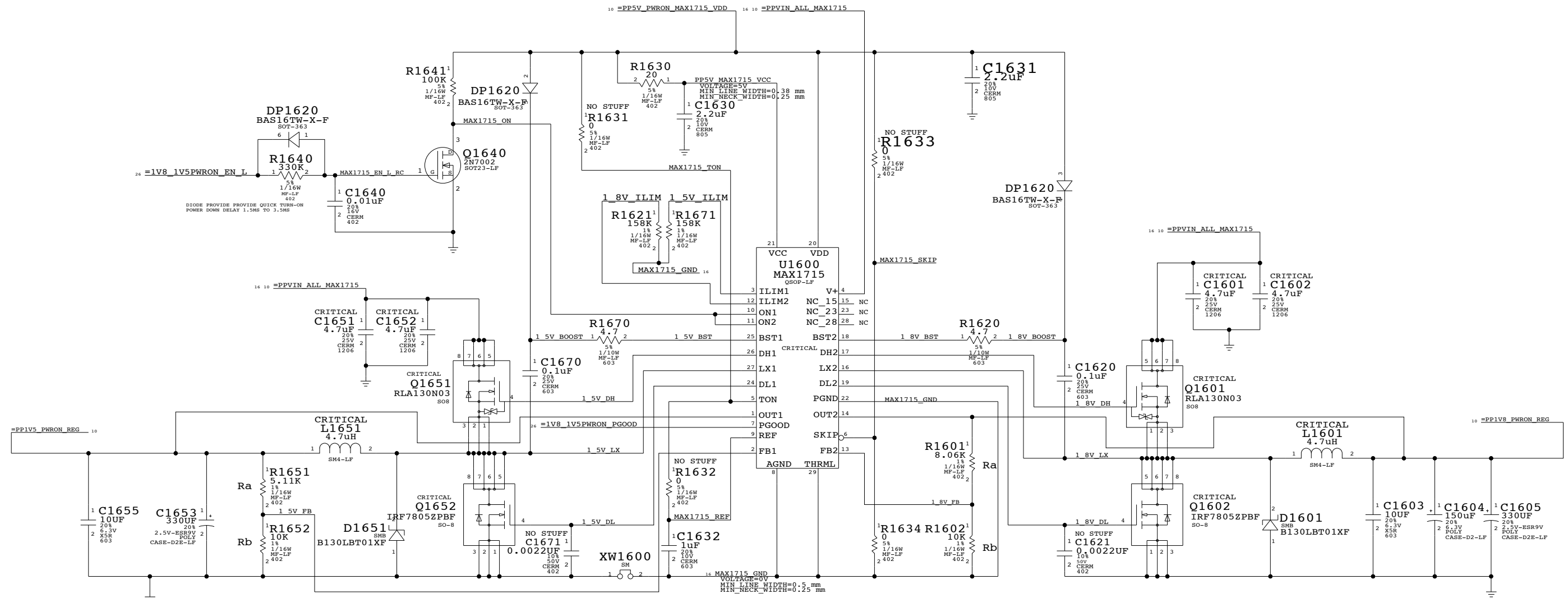
3.3V/5V SWITCHER



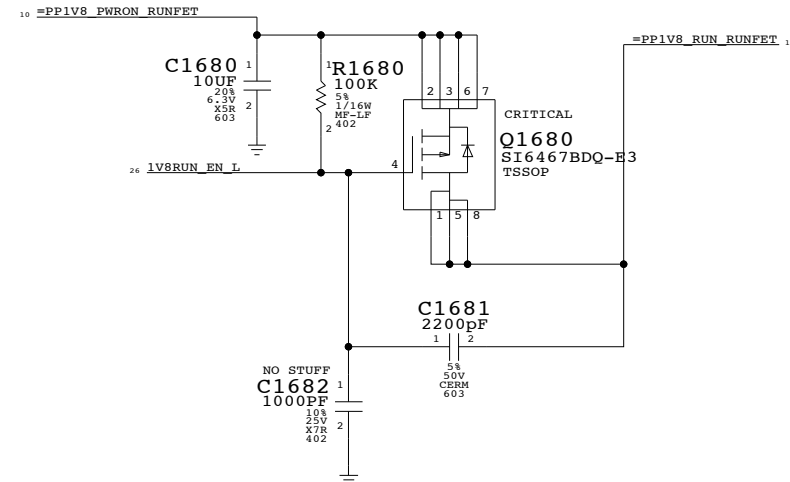
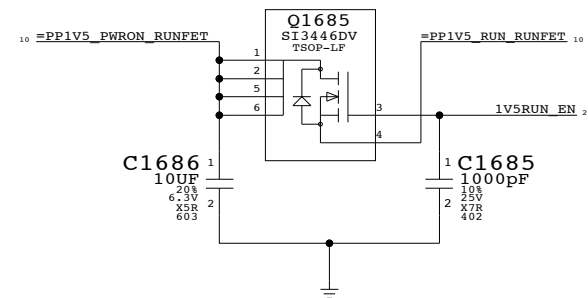
5V/3.3V Supplies
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SCALE	NONE	SHT	15 OF 115

1.5V/1.8V SWITCHER



$$V_{out} = 1.0V * (1 + R_a/R_b)$$



1.8V/1.5V Supplies

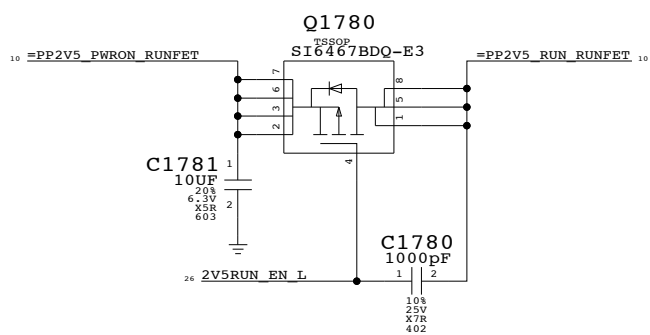
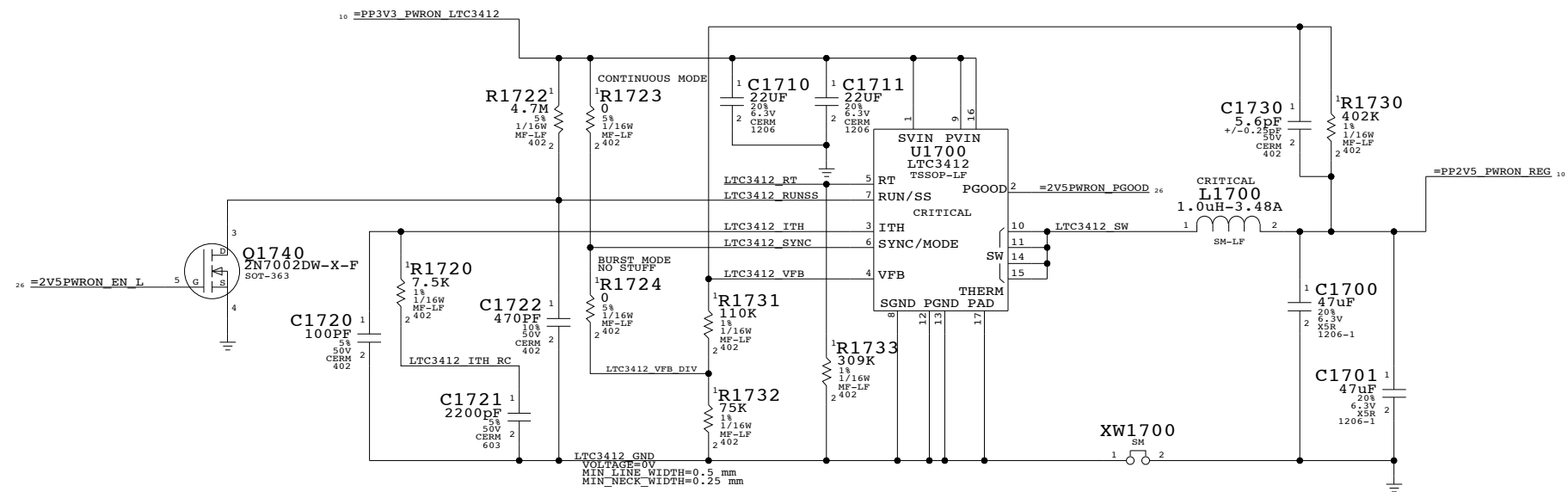
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2.5V SWITCHER



2.5V Supply

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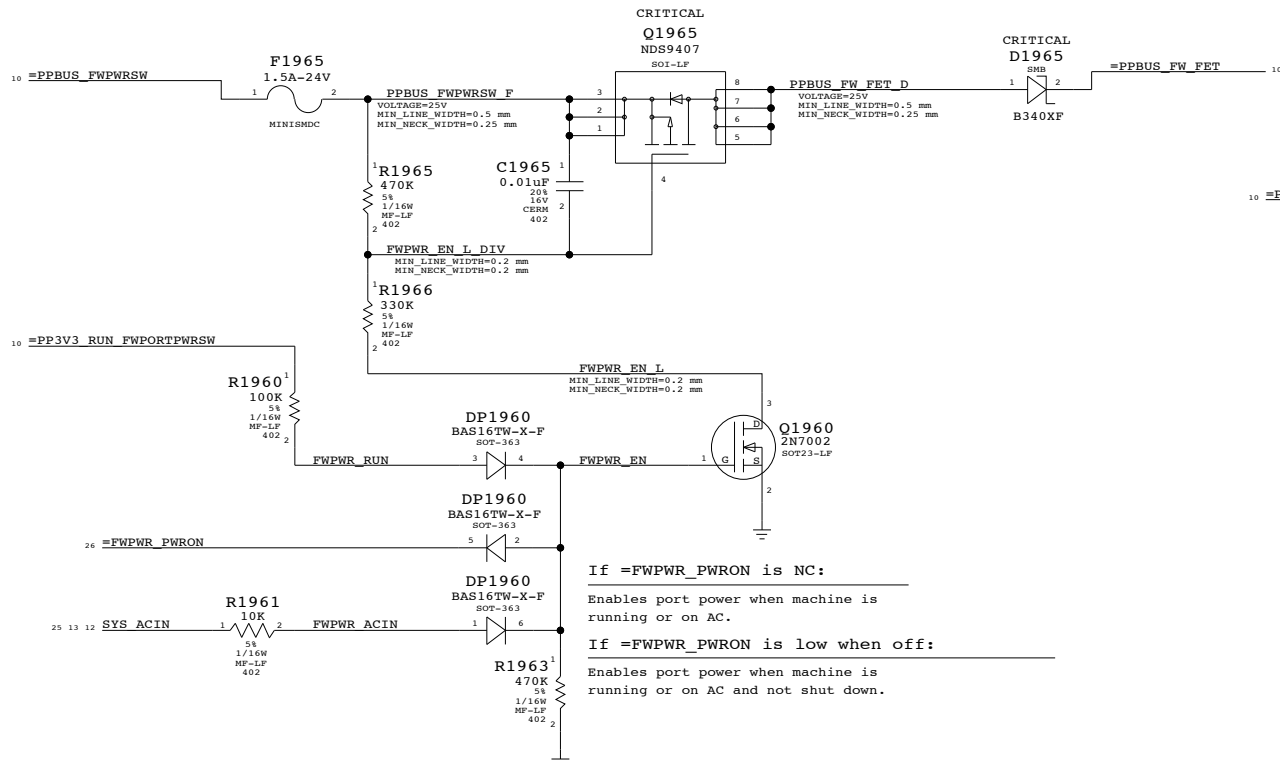
Page Notes

Power aliases required by this page:
 - =PPBUS_FW (system supply for bus power)
 - =PPBUS_RUN_FW (backup PHY power)
 - =PP3V3_RUN_FWPORTFWRWSW

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - VESTA1V2_BURST / VESTA1V2_PULSE
 Controls operating mode of Vesta 1.2V regulator. If both options are off the regulator will be in continuous mode.

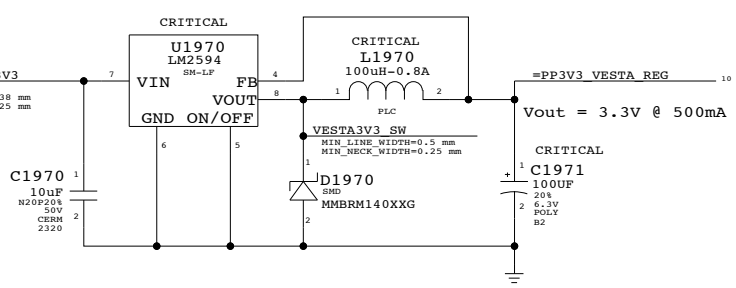
Port Power Switch



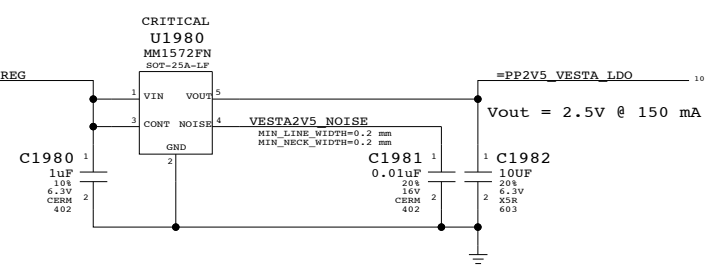
If =FWPWR_PWRON is NC:
 Enables port power when machine is running or on AC.

If =FWPWR_PWRON is low when off:
 Enables port power when machine is running or on AC and not shut down.

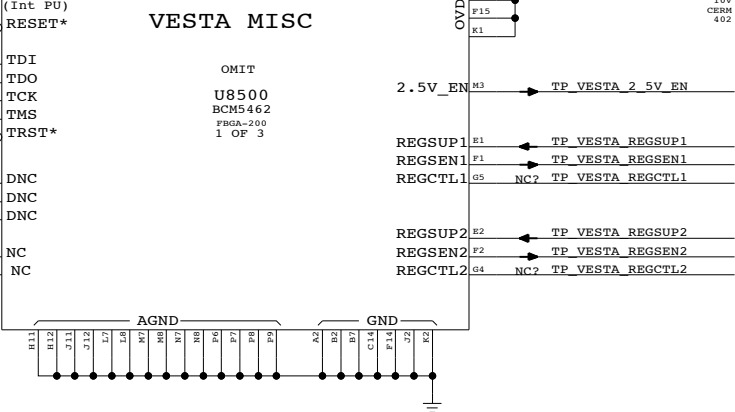
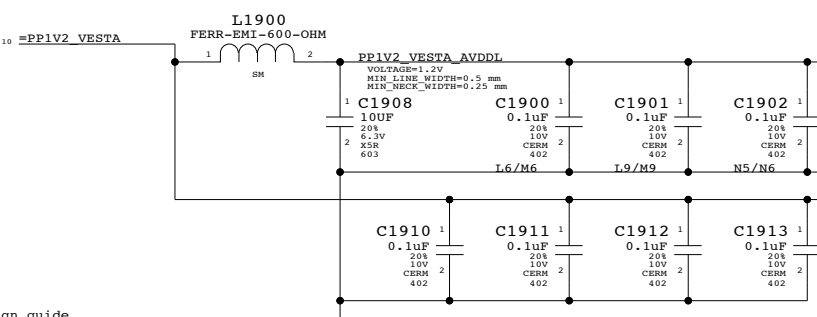
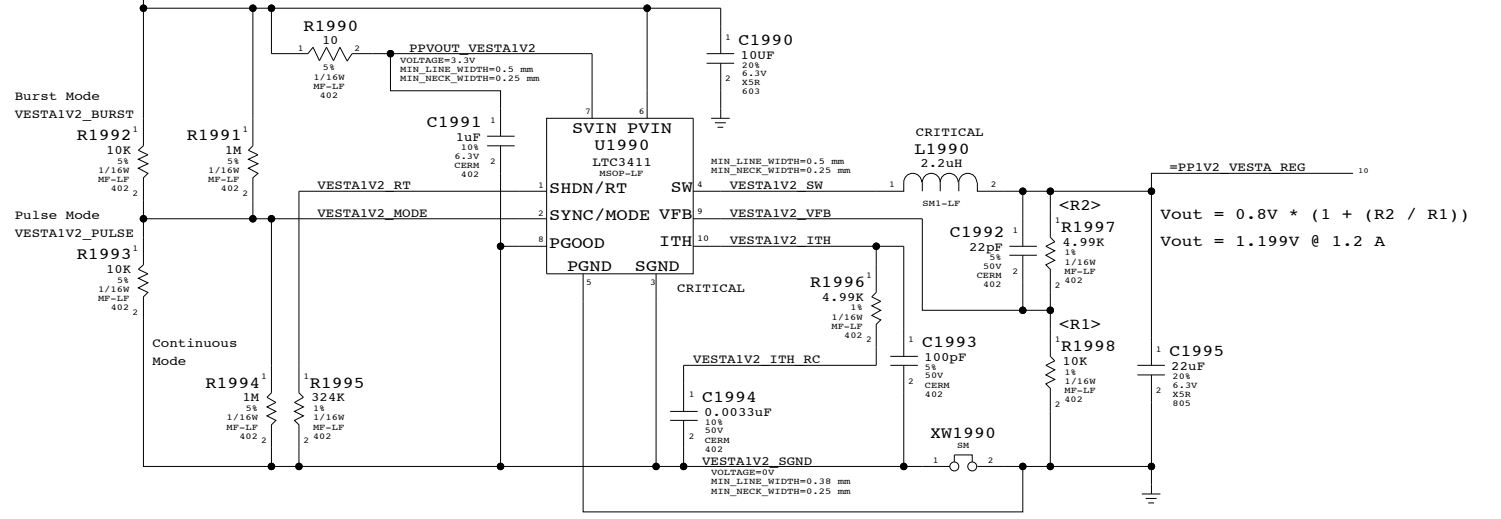
3.3V Regulator



2.5V LDO



1.2V Regulator



Vesta Power & Misc

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NONE	19	115	

Page Notes

Power aliases required by this page:

- =PPVCORE_PWRON_I2
- =PP1V5_PWRON_I2_PLL
- =PP3V3_PWRON_I2_IO1
- =PP3V3_PWRON_I2_IO2
- =PP3V3_PWRON_I2_MAXBUS
- =PP3V3_PWRON_I2_AGPPCI
- =PP3V3_PWRON_I2_MAXBUS

NOTE: The four 3.3V rails are meant to be aliased together. They are called out separately for test purposes.
NOTE: When these four rails are not aliased together, make sure there is at least one 10uF cap per rail.

Signal aliases required by this page:

(NONE)

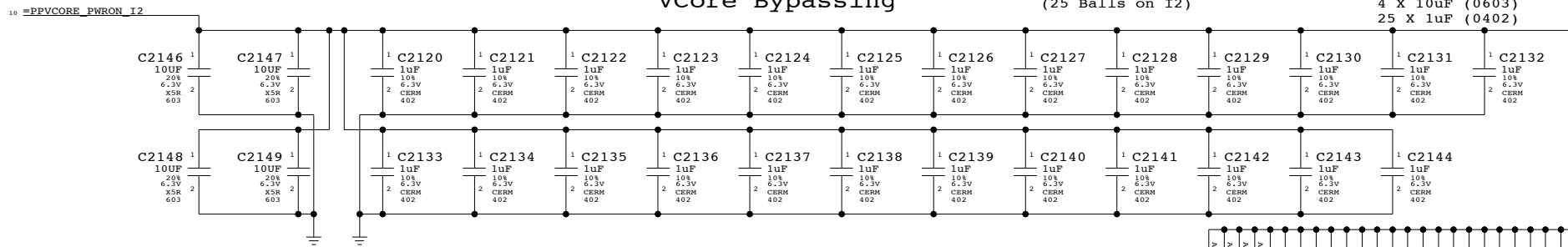
BOM options provided by this page:

(NONE)

VCore Bypassing

(25 Balls on I2)

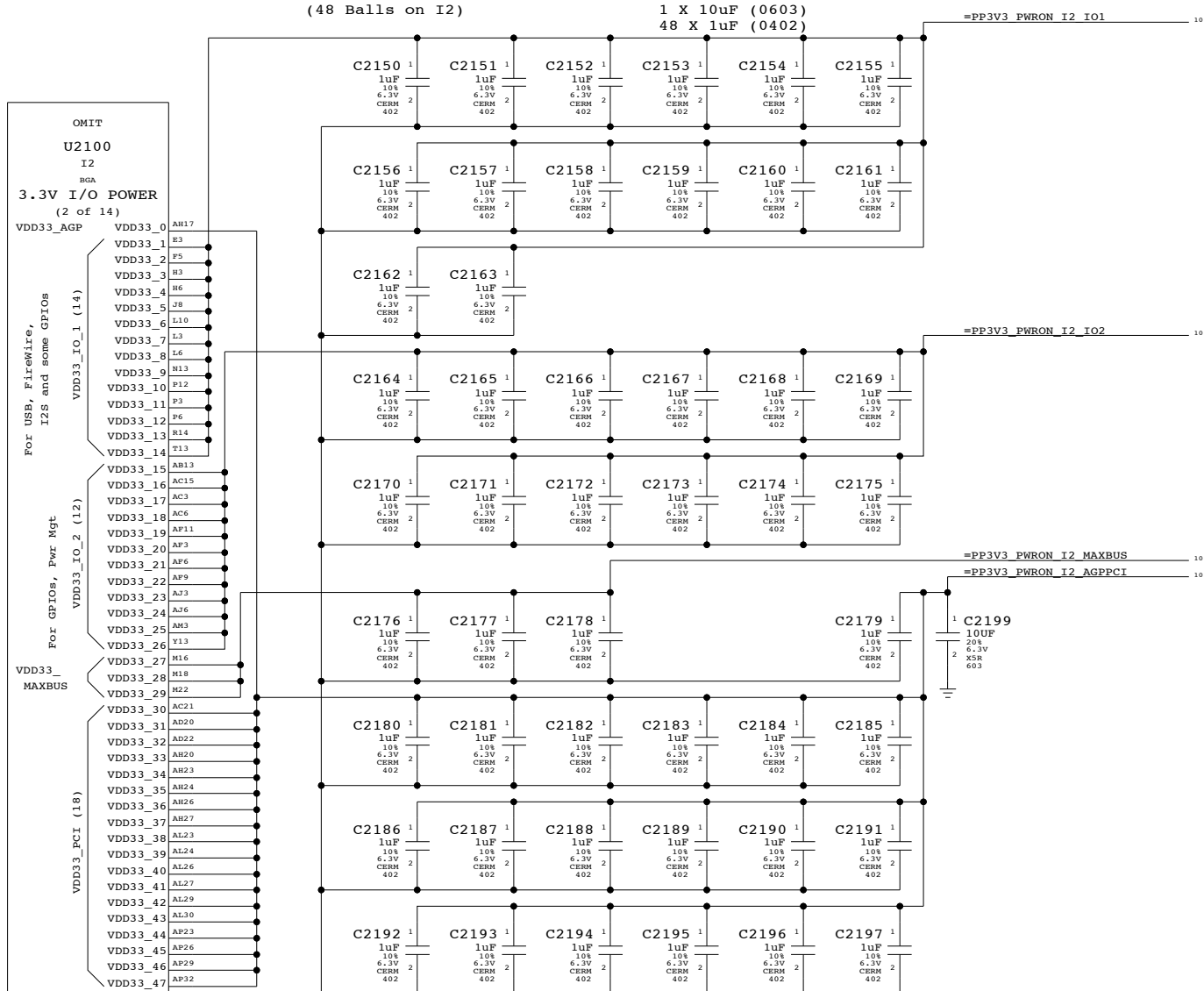
4 X 10uF (0603)
25 X 1uF (0402)



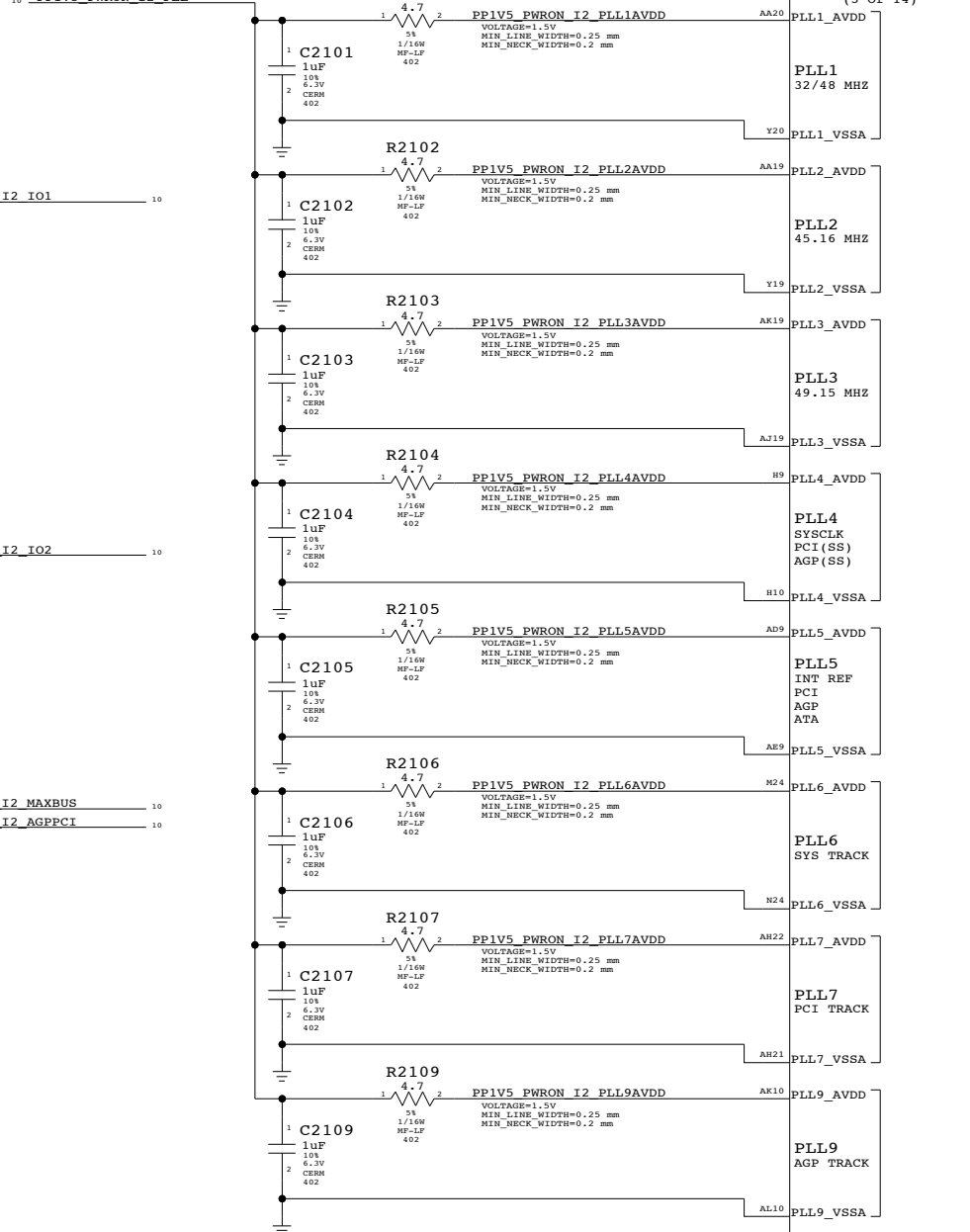
3.3V I/O DECOUPLING

(48 Balls on I2)

1 X 10uF (0603)
48 X 1uF (0402)



10=PP1V5_PWRON_I2_PLL



I2 Power

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NONE	21	115	

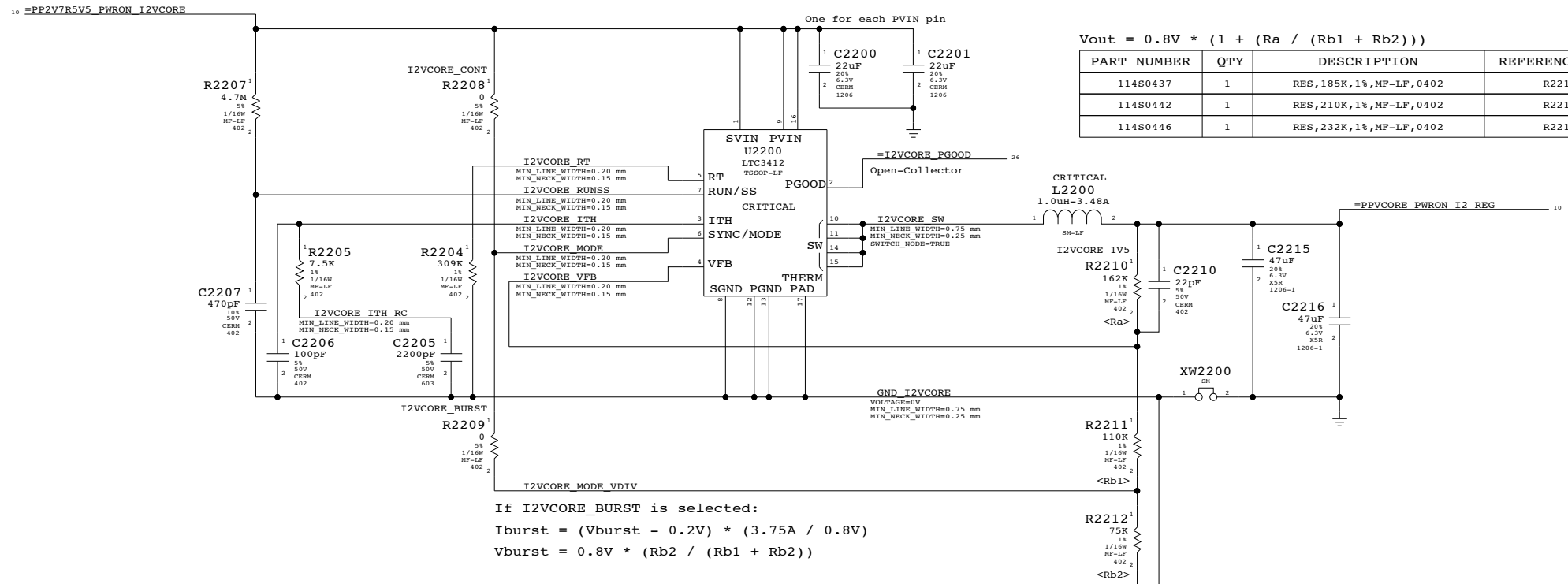
Page Notes

Power aliases required by this page:
 - =PP2V7R5V5_PWRON_I2VCORE
 - =PPVCORE_PWRON_I2_REG
 - =PPVIN_PWRON_I2PLLVD
 - =PP1V5_PWRON_I2PLLVD_LDO

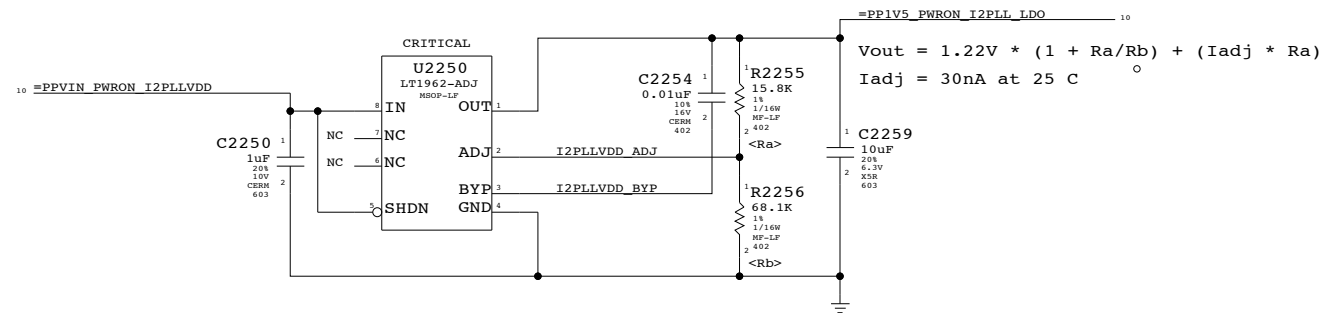
Signal aliases required by this page:
 - =I2VCORE_PGOOD

BOM options provided by this page:
 - I2VCORE_CONT / I2VCORE_BURST
 Selects between forced continuous and burst mode for LTC3412 regulator.
 - I2VCORE_xv
 Selects appropriate resistor for the indicated LTC3412 output voltage.

I2 VCore Regulator



I2 PLL LDO



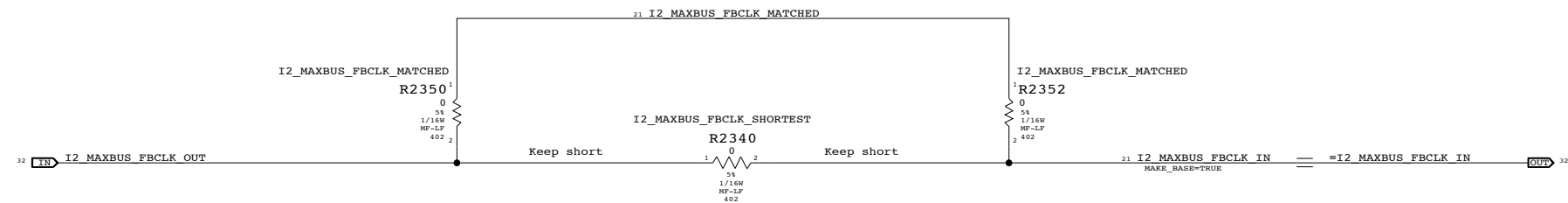
I2 Power Supplies
 SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005
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	D	051-6839	E
SCALE	SHT	OF	
NONE	22	115	

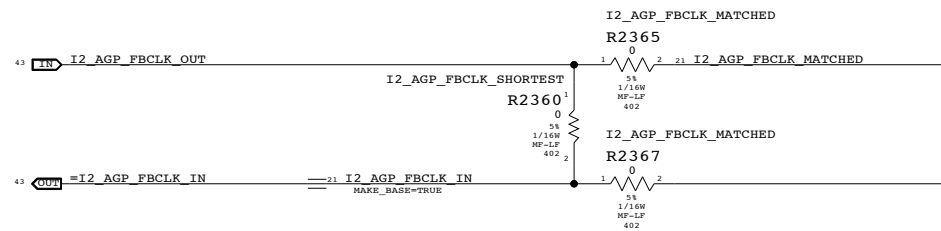
ELECTRICAL_CONSTRAINT_SET	NET_TYPE	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
	I2_FBCLK	12	I2_FBCLK	
	I2_FBCLK	12	I2_FBCLK	
	I2_FBCLK	12	I2_FBCLK	
	I2_FBCLK	12	I2_FBCLK	
H105	I2_FBCLK	12	I2_FBCLK	
H105	I2_FBCLK	12	I2_FBCLK	
H115	CLOCK	CLOCK	CLOCK	
H120	CLOCK	CLOCK	CLOCK	

I2_MAXBUS_FBCLK_IN	21
I2_MAXBUS_FBCLK_MATCHED	21
I2_AGP_FBCLK_IN	21
I2_AGP_FBCLK_MATCHED	21
I2_PCI_FBCLK_IN	21
I2_PCI_FBCLK_MATCHED	21
=CLK33M_TBEN_SYNC	11 21
=SYSCLK_TBEN_SYNC	11 21

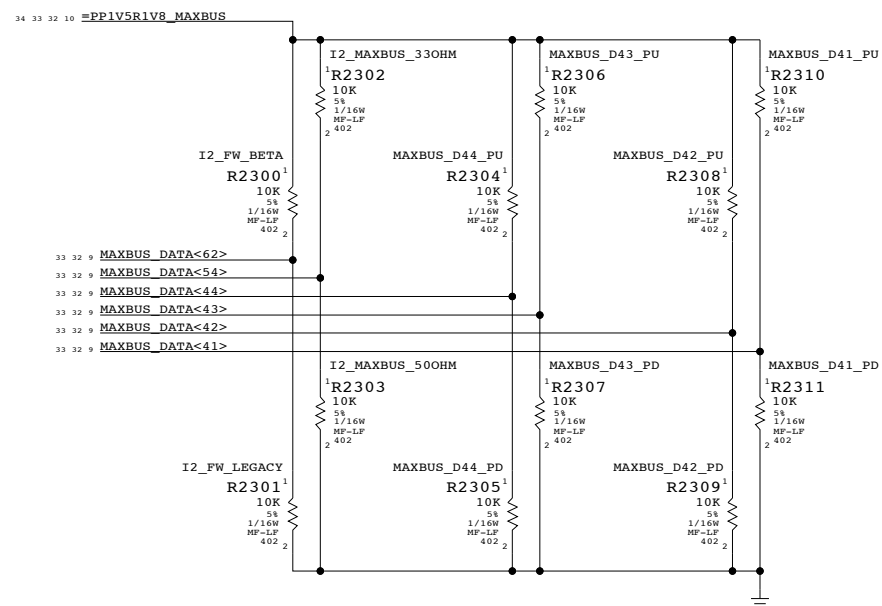
MaxBus Feedback Clock Network



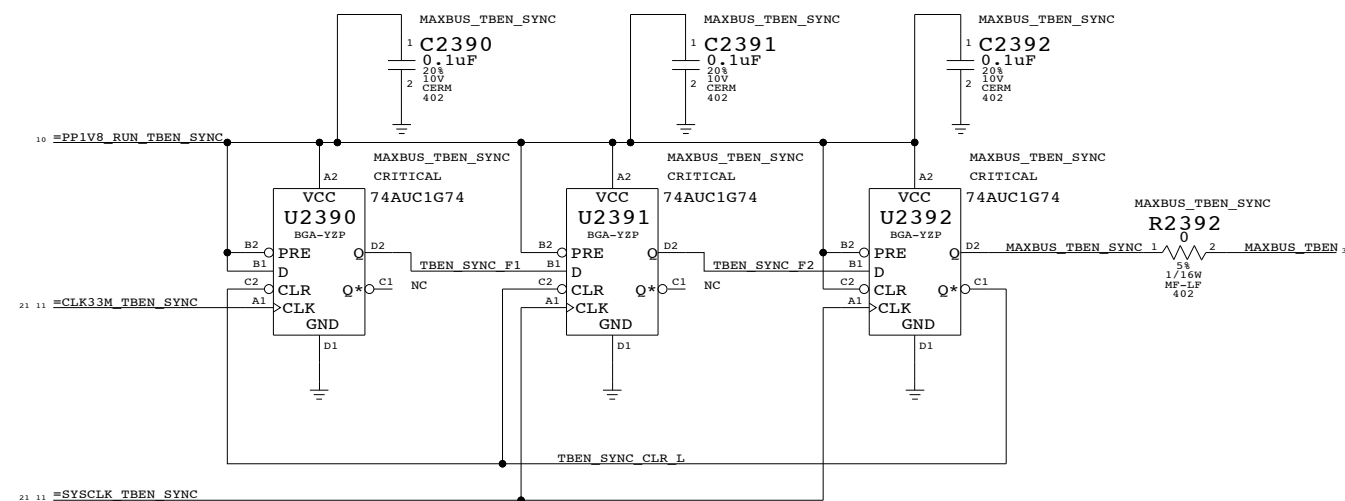
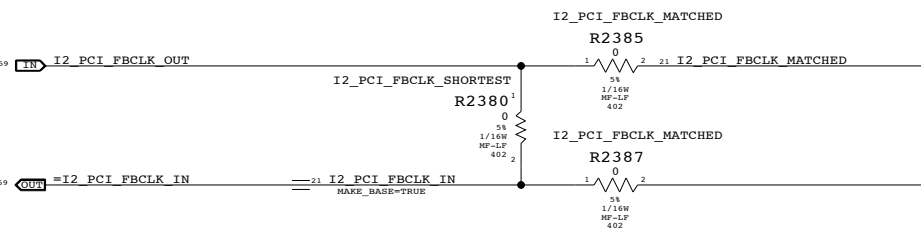
AGP Feedback Clock Ladder



I2 Configuration Straps



PCI Feedback Clock Ladder



Signal	Tied	Description
MAXBUS_DATA<62>	HIGH	1394b Support (Beta Mode)
	LOW	1394a Support (Legacy Mode)
MAXBUS_DATA<54>	HIGH	50-Ohm MaxBus Drivers
	LOW	33-Ohm MaxBus Drivers
MAXBUS_DATA<44:41>		See Table Below

BOM GROUP	Tied	Description	BOM OPTIONS
I2_MAXBUS_133MHZ	0000	133.12MHz CPU / 266.24MHz DDR	MAXBUS_D44_PD,MAXBUS_D43_PD,MAXBUS_D42_PD,MAXBUS_D41_PD
I2_MAXBUS_150MHZ	1000	149.76MHz CPU / 299.52MHz DDR	MAXBUS_D44_PU,MAXBUS_D43_PD,MAXBUS_D42_PD,MAXBUS_D41_PD
I2_MAXBUS_166MHZ	0100	166.40MHz CPU / 332.80MHz DDR	MAXBUS_D44_PD,MAXBUS_D43_PU,MAXBUS_D42_PD,MAXBUS_D41_PD
I2_MAXBUS_172MHZ	1100	171.95MHz CPU / 342.90MHz DDR	MAXBUS_D44_PU,MAXBUS_D43_PU,MAXBUS_D42_PD,MAXBUS_D41_PD
I2_MAXBUS_177MHZ	0010	177.49MHz CPU / 354.98MHz DDR	MAXBUS_D44_PD,MAXBUS_D43_PD,MAXBUS_D42_PU,MAXBUS_D41_PD
I2_MAXBUS_183MHZ	1010	183.04MHz CPU / 366.08MHz DDR	MAXBUS_D44_PU,MAXBUS_D43_PD,MAXBUS_D42_PU,MAXBUS_D41_PD
I2_MAXBUS_189MHZ	0110	188.59MHz CPU / 377.18MHz DDR	MAXBUS_D44_PD,MAXBUS_D43_PU,MAXBUS_D42_PU,MAXBUS_D41_PD
I2_MAXBUS_194MHZ	1110	194.13MHz CPU / 388.26MHz DDR	MAXBUS_D44_PU,MAXBUS_D43_PU,MAXBUS_D42_PU,MAXBUS_D41_PD
I2_MAXBUS_200MHZ	0001	199.68MHz CPU / 399.36MHz DDR	MAXBUS_D44_PD,MAXBUS_D43_PD,MAXBUS_D42_PD,MAXBUS_D41_PU

I2 Supplemental

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NONE	23	115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
I2S0_DTO	I2S	128	128	I2S0_DEV_TO_SB DTI
I2S0_DTO	I2S	128	128	I2S0_SB_TO_DEV DTO R
I2S0_MCLK	I2S	128	128	I2S0_MCLK R
I2S0_BITCLK	I2S	128	128	I2S0_BITCLK R
I2S0_SYNC	I2S	128	128	I2S0_SYNC R
I2S1_DTO	I2S	128	128	I2S1_DEV_TO_SB DTI
I2S1_DTO	I2S	128	128	I2S1_SB_TO_DEV DTO R
I2S1_MCLK	I2S	128	128	I2S1_MCLK R
I2S1_BITCLK	I2S	128	128	I2S1_BITCLK R
I2S1_SYNC	I2S	128	128	I2S1_SYNC R
I2_XTAL	XTAL	XTAL	XTAL	I2_CLK18M XOUT R
(I2_XTAL)	XTAL	XTAL	XTAL	I2_CLK18M XOUT
(I2_XTAL)	XTAL	XTAL	XTAL	I2_CLK18M XIN

Page Notes

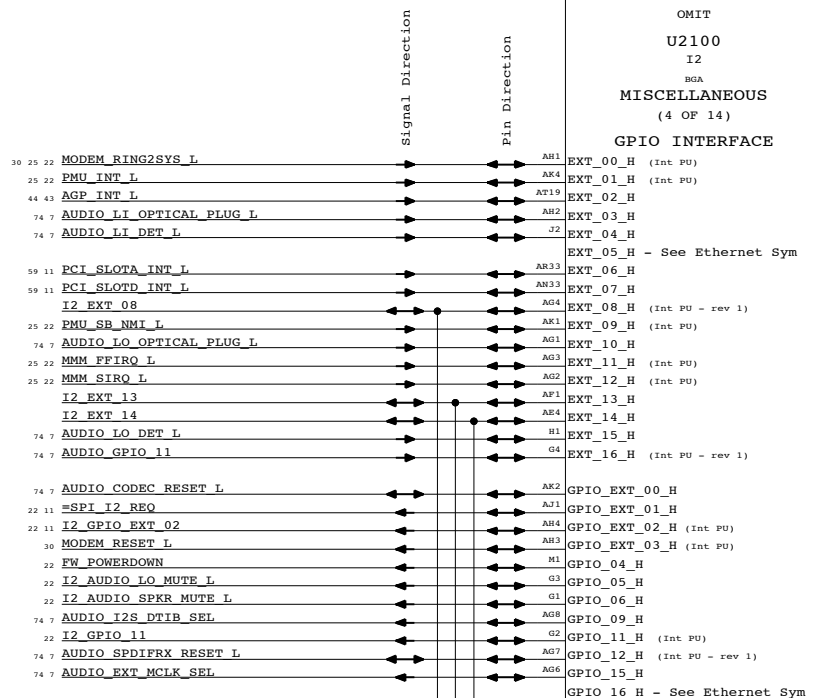
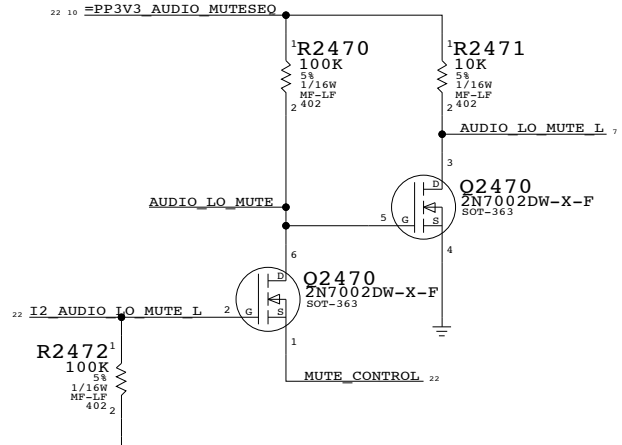
Power aliases required by this page:
 - =PP3V3_PWRON_I2_GPIO
 - =PP3V3_I2_PCISLOTTEGPIO (PWRON or PCI)
 Should be same as =PP3V3_PCI if slot E is used, or else =PP3V3_PWRON_I2_GPIO.

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - I2_REV1_NOT
 Use for I2 revisions > 1.0

Audio Mute Sequencing

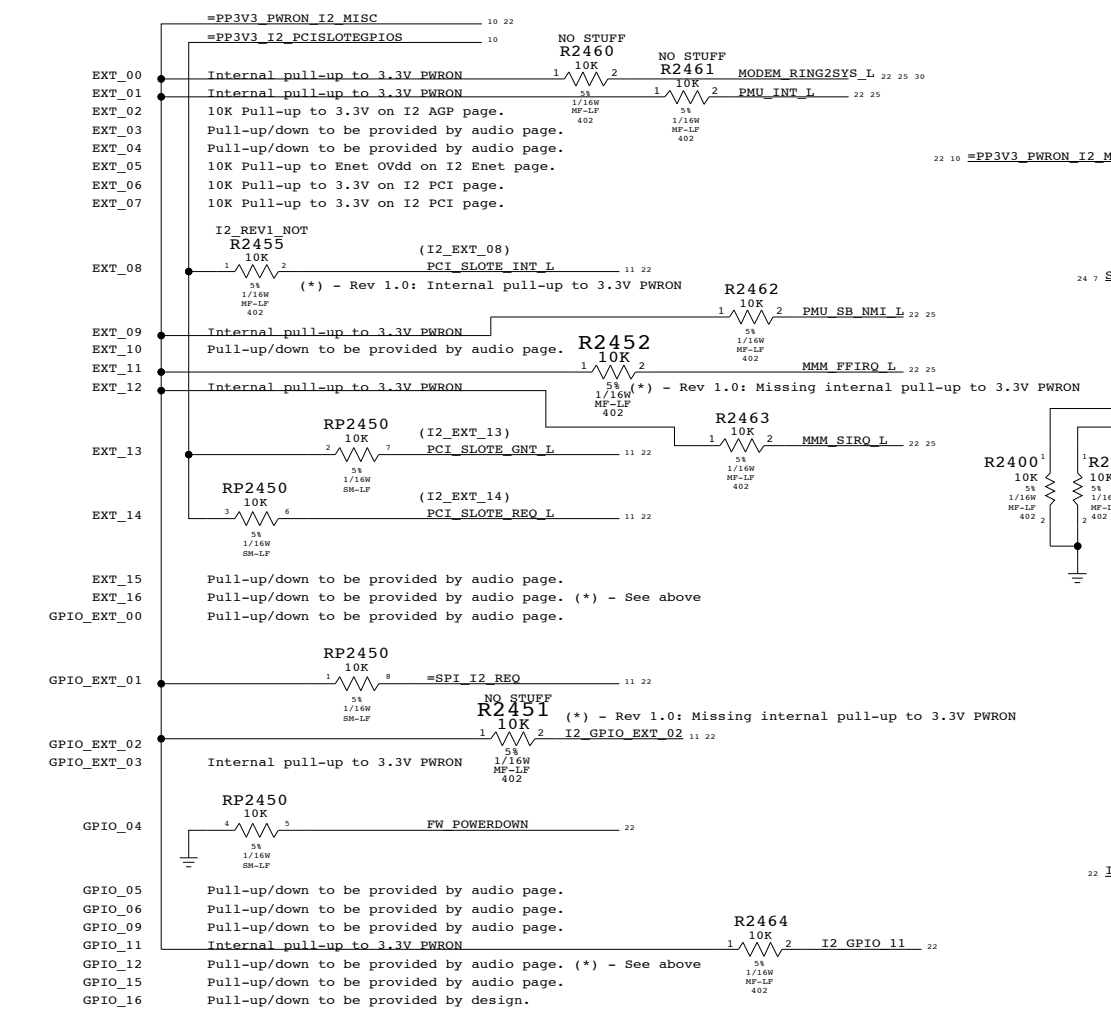
Prevents mute glitch from reaching audio circuit



Alternate GPIO Functions
Use MAKE_BASE to force net name

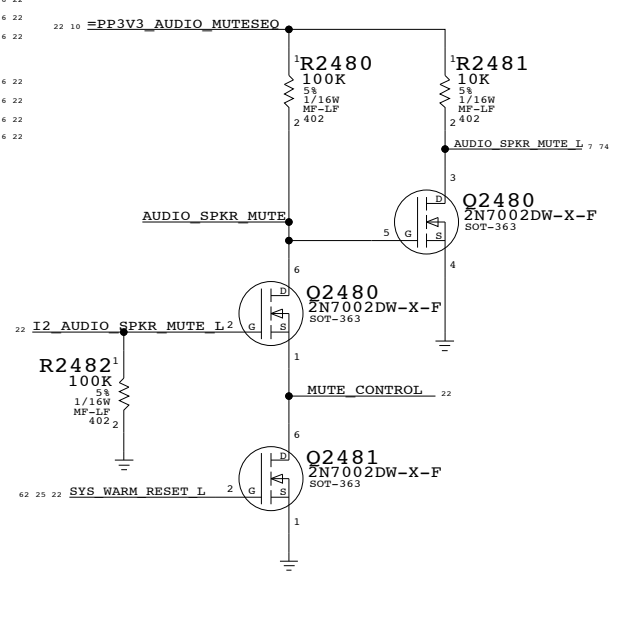
Pin	Address	MPIC	Int	Int PU?	Alt Func
EXT_00	0x0_0058	46	(0x2E)	Yes	PCI_REQ_2_L (When PCI1_Slot2En = 10)
EXT_01	0x0_0059	47	(0x2F)	Yes	
EXT_02	0x0_005A	48	(0x30)	No	
EXT_03	0x0_005B	49	(0x31)	No	
EXT_04	0x0_005C	50	(0x32)	No	
EXT_05	0x0_005D	51	(0x33)	No	
EXT_06	0x0_005E	52	(0x34)	No	
EXT_07	0x0_005F	53	(0x35)	No	
EXT_08	0x0_0060	54	(0x36)	Yes	
EXT_09	0x0_0061	55	(0x37)	Yes	
EXT_10	0x0_0062	56	(0x38)	No	
EXT_11	0x0_0063	57	(0x39)	Yes	
EXT_12	0x0_0064	58	(0x3A)	Yes	
EXT_13	0x0_0065	59	(0x3B)	No	PCI_GNT_2_L (When PCI1_Slot2En = 11)
EXT_14	0x0_0066	60	(0x3C)	No	PCI_REQ_2_L (When PCI1_Slot2En = 11)
EXT_15	0x0_0067	61	(0x3D)	No	
EXT_16	0x0_0068	62	(0x3F)	Yes	
GPIO_00	0x0_006A	14	(0x0E)	No	
GPIO_01	0x0_006B	15	(0x0F)	No	SPIREQ (When SPISReqEn = 1)
GPIO_02	0x0_006C	16	(0x10)	Yes	PCI_GNT_2_L (When PCI1_Slot2En = 10)
GPIO_03	0x0_006D	17	(0x11)	Yes	
GPIO_04	0x0_006E	N/A		No	
GPIO_05	0x0_006F	N/A		No	
GPIO_06	0x0_0070	N/A		No	
GPIO_09	0x0_0073	N/A		No	
GPIO_11	0x0_0075	N/A		Yes	
GPIO_12	0x0_0076	N/A		Yes	
GPIO_15	0x0_0079	N/A		No	
GPIO_16	0x0_007A	N/A		No	

GPIO Pull-ups / Pull-downs



Audio Mute Sequencing

Prevents mute glitch from reaching audio circuit



I2 Miscellaneous

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SCALE	SHT	OF	
NONE	24	115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		DIFFERENTIAL_PAIR
	SPACING	PHYSICAL	
PCI_ZDBOUT0	CLOCK	CLOCK	
PCI_ZDBOUT1	CLOCK	CLOCK	
PCI_ZDBOUT2	CLOCK	CLOCK	
PCI_ZDBOUT3	CLOCK	CLOCK	

```

=PCI_CLK33M_ZDB_IN 11 23
=PCI_CLK33M_ZDBOUT_R<0> 11 23
=PCI_CLK33M_ZDBOUT_R<1> 11 23
=PCI_CLK33M_ZDBOUT_R<2> 11 23
=PCI_CLK33M_ZDBOUT_R<3> 11 23

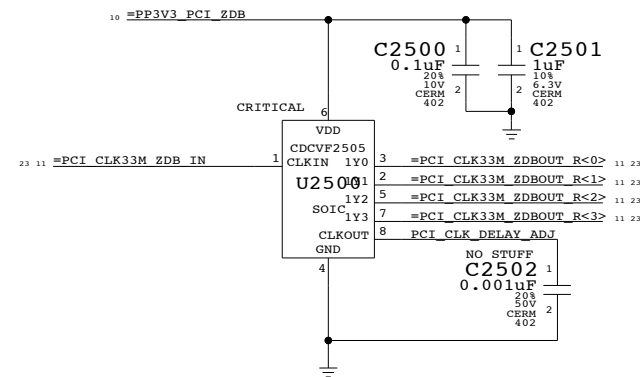
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Page Notes

Power aliases required by this page:
- =PP3V3_PWRON_I2_GPIO
- =PP3V3_I2_PCISLOTEGPIOs (PWRON or PCI)
Should be same as =PP3V3_PCI if slot E is used, or else =PP3V3_PWRON_I2_GPIO.

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- I2_REV1_NOT
Use for I2 revisions > 1.0



PCI Clock Buffer

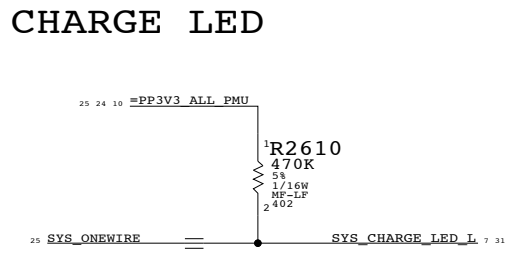
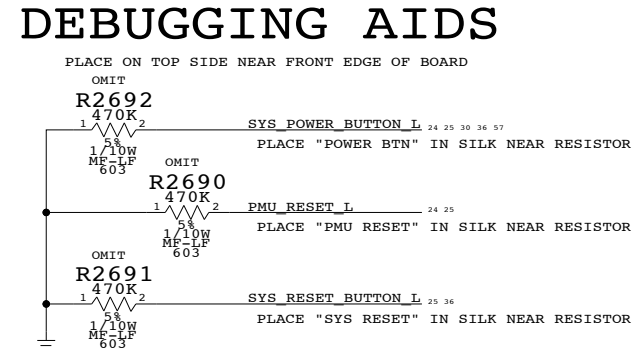
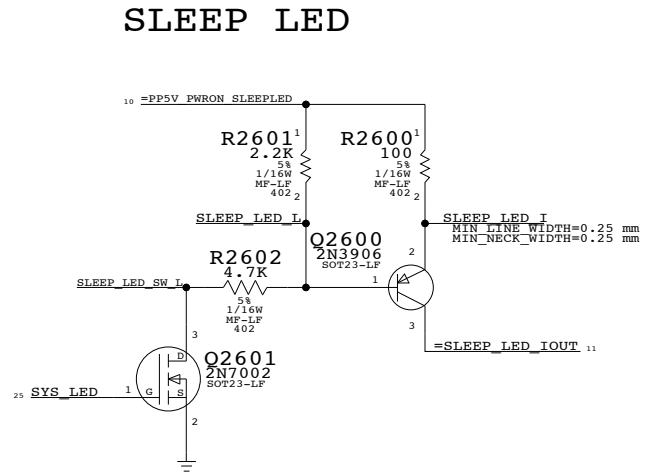
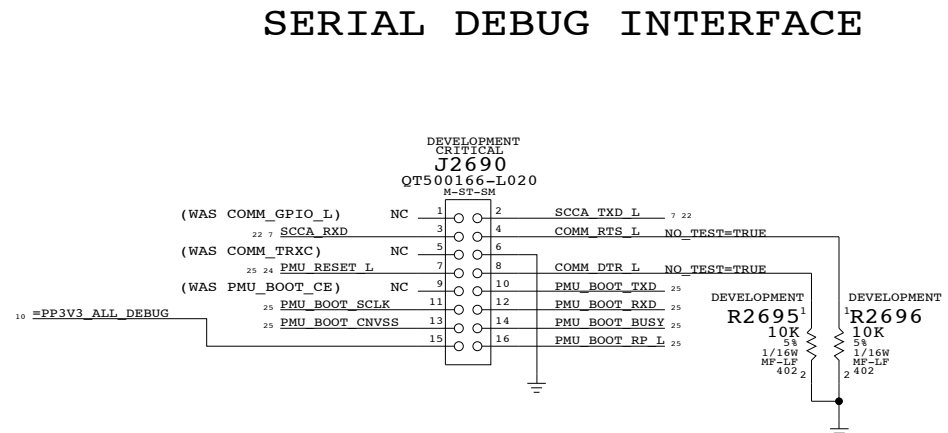
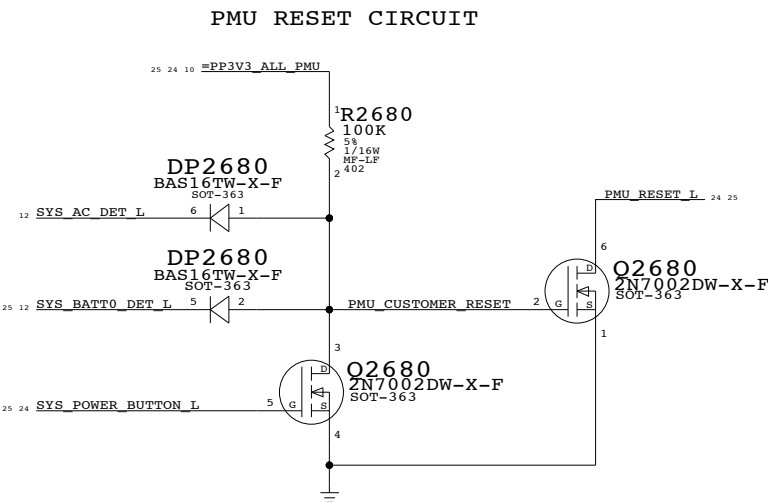
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LEDs/Reset/Debug

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NONE	26		115

Power Management Unit

NET TYPE		SPACING	PHYSICAL	DIFFERENTIAL_PAIR
ELECTRICAL_CONSTRAINT_SET	PMU_CLK10M_XTAL	XTAL	XTAL	
	PMU_CLK10M_XOUT	XTAL	XTAL	
	PMU_CLK10M_XOUT_R	XTAL	XTAL	
PMU_CLK32K_XTAL	PMU_CLK32K_XIN	XTAL	XTAL	
	PMU_CLK32K_XOUT	XTAL	XTAL	
	PMU_CLK32K_XOUT_R	XTAL	XTAL	

Page Notes

Power aliases required by this page:
 - =PP3V3_ALL_PMU
 - =PP3V3_PWRON_PMU
 - =PPVREF_PMU (PMU AVCC or 2.5V reference)

Signal aliases required by this page:
 - =I2C_PMU_SCL
 - =I2C_PMU_SDA
 - =I2C_PMU_SMB_SCL
 - =I2C_PMU_SMB_SDA
 - =JTAG_BBANGER_TCK
 - =JTAG_BBANGER_TDI
 - =JTAG_BBANGER_TMS
 - =JTAG_BBANGER_TRST_L

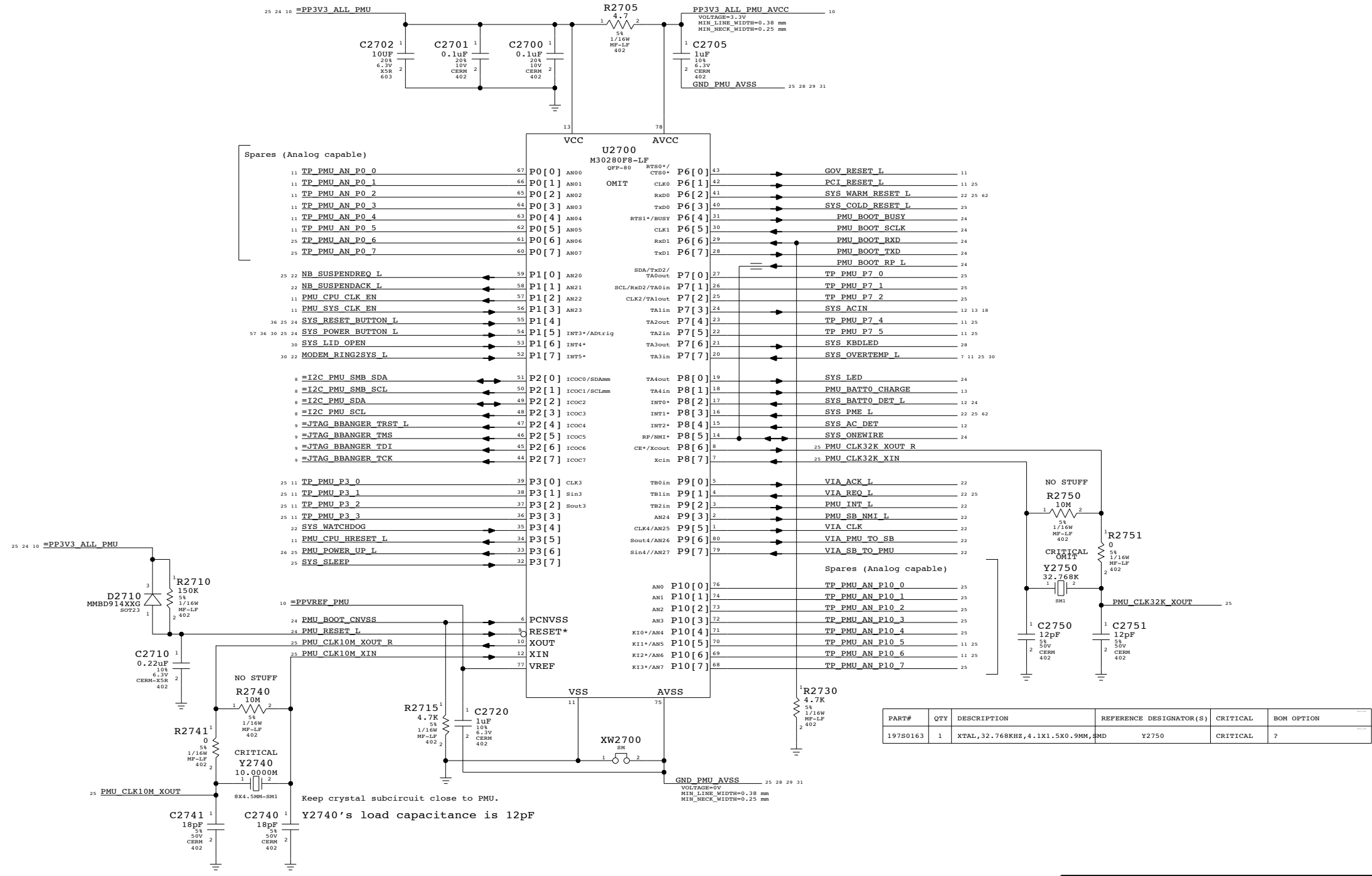
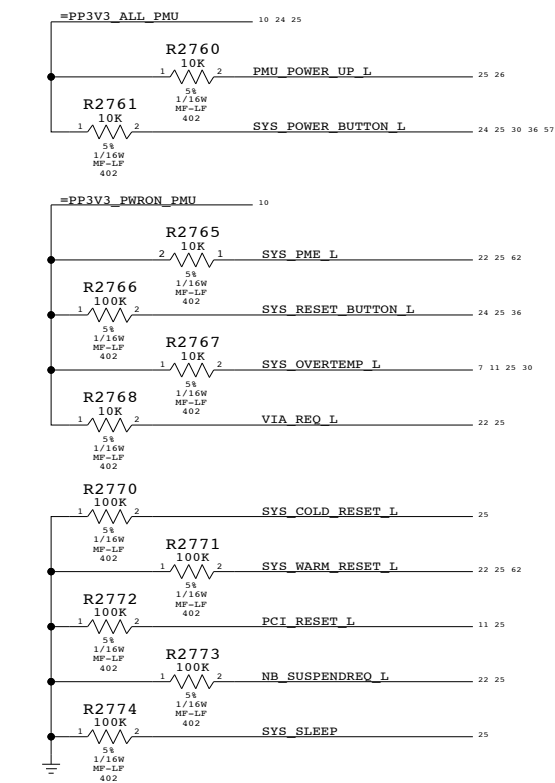
NOTE: Boot-banger pins can be aliased to TP_ or NC_ if not implemented.

BOM options provided by this page:
 (NONE)

NOTE: TP_PMU_Fx_x signals are general-purpose spares. Some pins are reserved for alternate functions. TP_PMU_AN_Fx_x signals are general-purpose spares that can also be used as analog inputs.

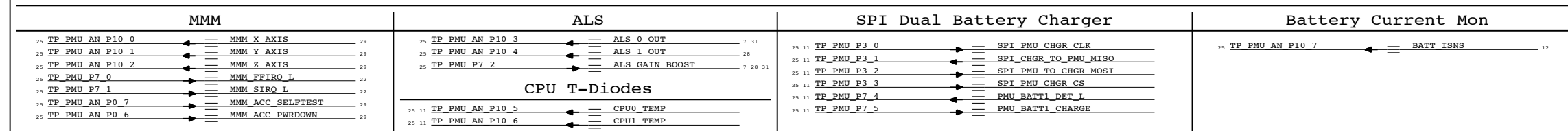
NOTE: All analog inputs to PMU should have a 100pF capacitor to the PMU AVSS signal (GND_PMU_AVSS). None of those capacitors are provided on this page.

PMU Pull-ups / pull-downs



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
19790163	1	XTAL, 32.768KHZ, 4.1X1.5X0.9MM, 4MD	Y2750	CRITICAL	?

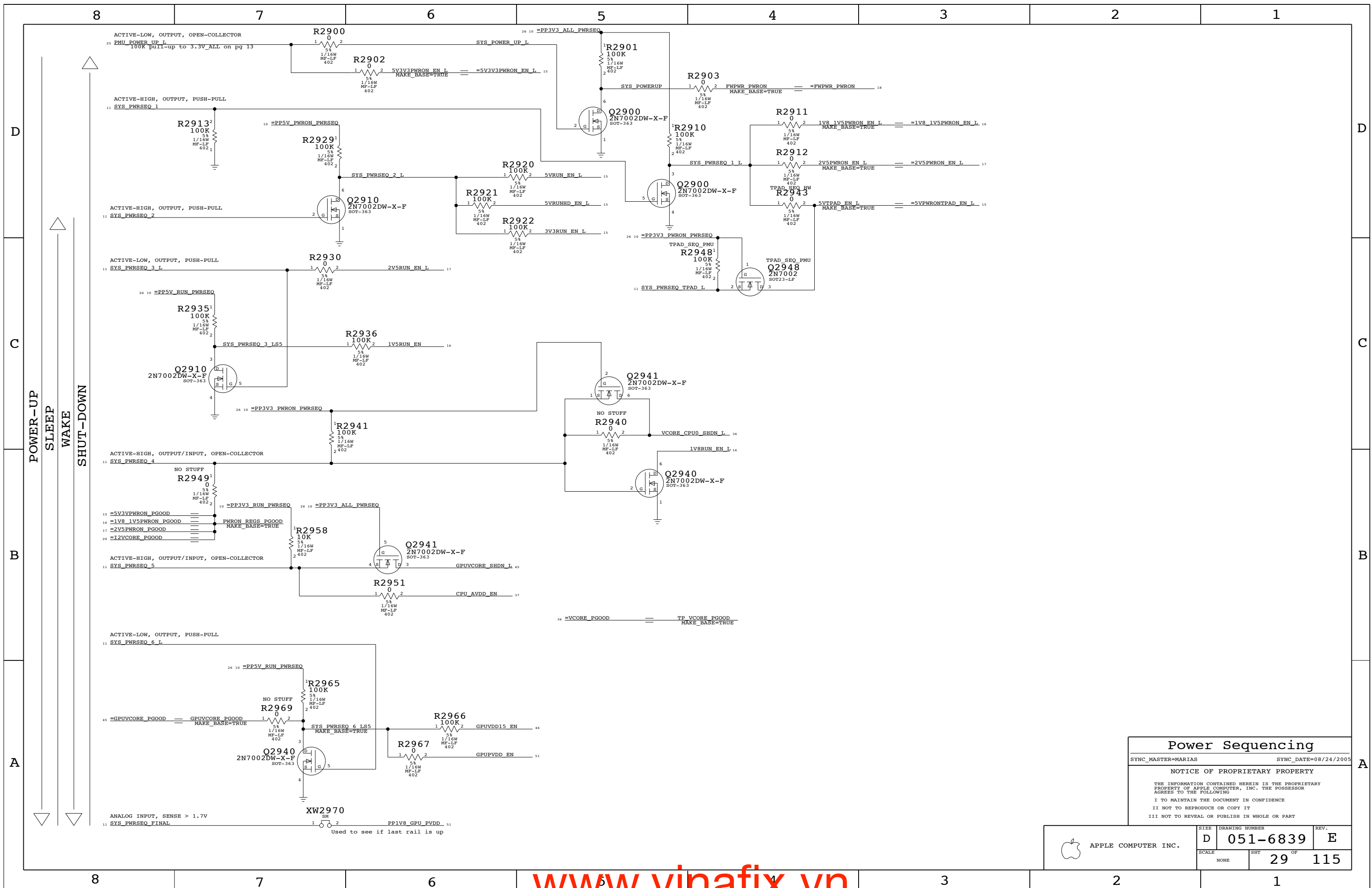
Additional PMU05 "Modules"



Power Management Unit (PMU05)
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27		115	

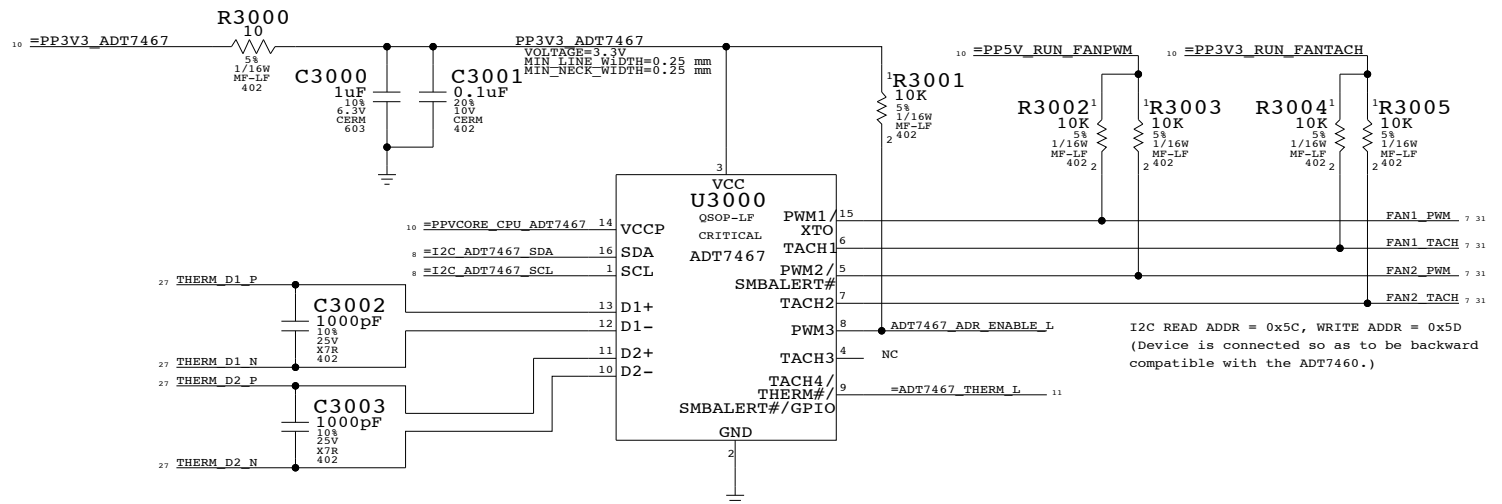


Power Sequencing
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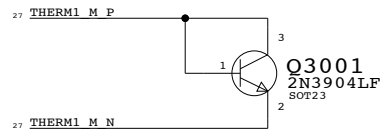
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	NONE	051-6839	E
SCALE		SHT	OF
NONE		29	115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			THERM1_M_P	THERM1_M_N	THERM2_M_P	THERM2_M_N	THERM1_A_P	THERM1_A_N	THERM2_A_P	THERM2_A_N	THERM_D1_P	THERM_D1_N	THERM_D2_P	THERM_D2_N
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR												
E520	THERM	THERM	THERM1_M												
E520	THERM	THERM	THERM1_M												
E530	THERM	THERM	THERM2_M												
E530	THERM	THERM	THERM2_M												
E530	THERM	THERM	THERM1_A												
E530	THERM	THERM	THERM1_A												
E530	THERM	THERM	THERM2_A												
E530	THERM	THERM	THERM2_A												
E530	THERM	THERM	THERM_D1												
E530	THERM	THERM	THERM_D1												
E530	THERM	THERM	THERM_D2												
E530	THERM	THERM	THERM_D2												

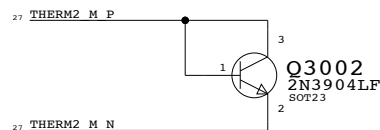
FAN CONTROLLER



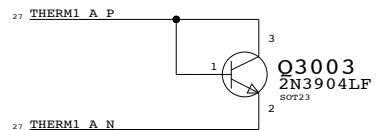
PLACE CLOSE TO CPU MAIN1



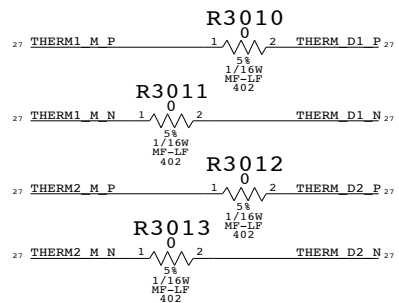
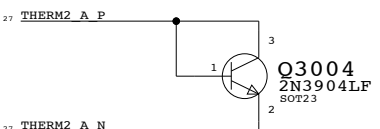
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY MAIN2



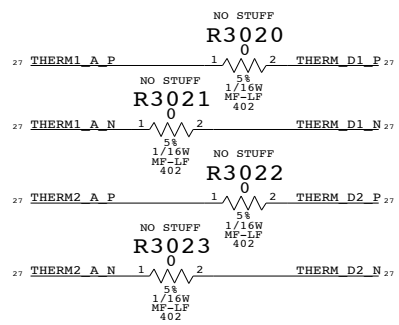
PLACE UNDERNEATH UPPER RAM ALTERNATE1



PLACE CLOSE TO BATTERY CHARGER/VCORE ALTERNATE2

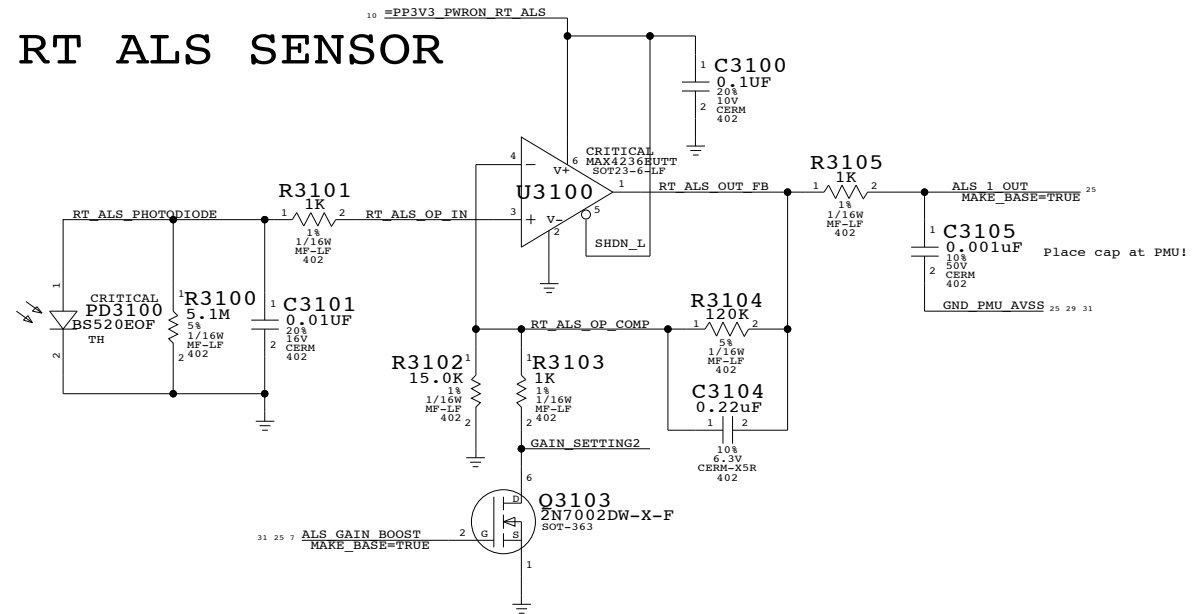


KEEP STUFFING RESISTORS CLOSE TO ADT7467 CONTROLLER



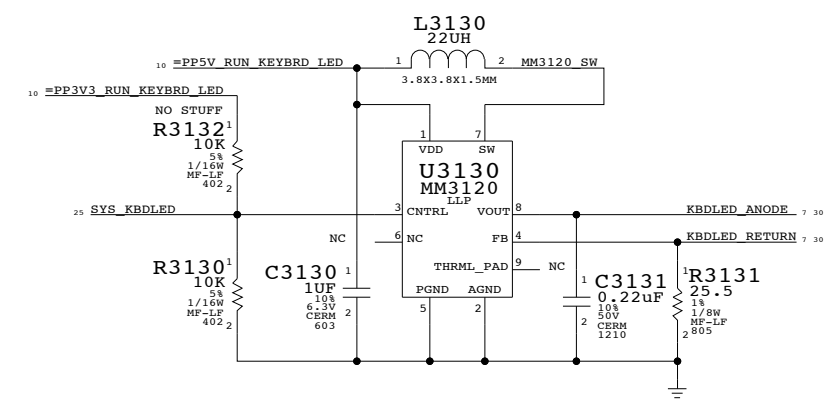
Fan Controller
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NONE	30		115



PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1191	353S1186		U3100	Primary is unity gain stable/als is stable at G5

Keyboard LED Driver



ALS Support

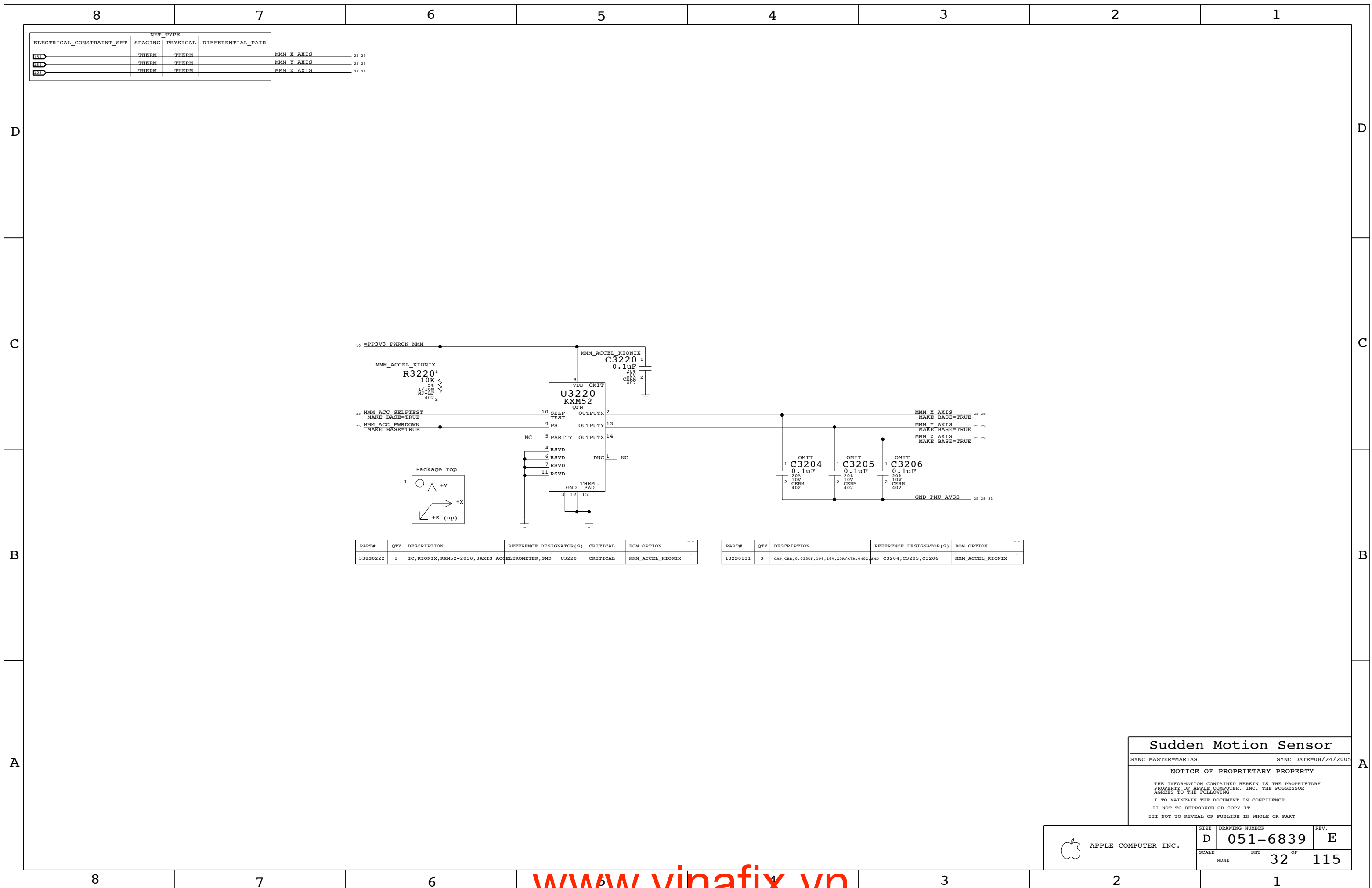
SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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SCALE	SHT OF		
NONE	31 OF		115



ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
E57	THERM	THERM	MMM_X_AXIS 25 29
E58	THERM	THERM	MMM_Y_AXIS 25 29
E59	THERM	THERM	MMM_Z_AXIS 25 29

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33880222	1	IC, KIONIX, KXM52-2050, 3AXIS ACCELEROMETER, SMD	U3220	CRITICAL	MMM_ACCEL_KIONIX

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
13280131	3	CAP, CER, 0.033UF, 10%, 16V, X5R/X7R, 0402, SMD	C3204, C3205, C3206	MMM_ACCEL_KIONIX

Sudden Motion Sensor
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SCALE	SHT OF		
NONE	32 OF		115

8

7

6

5

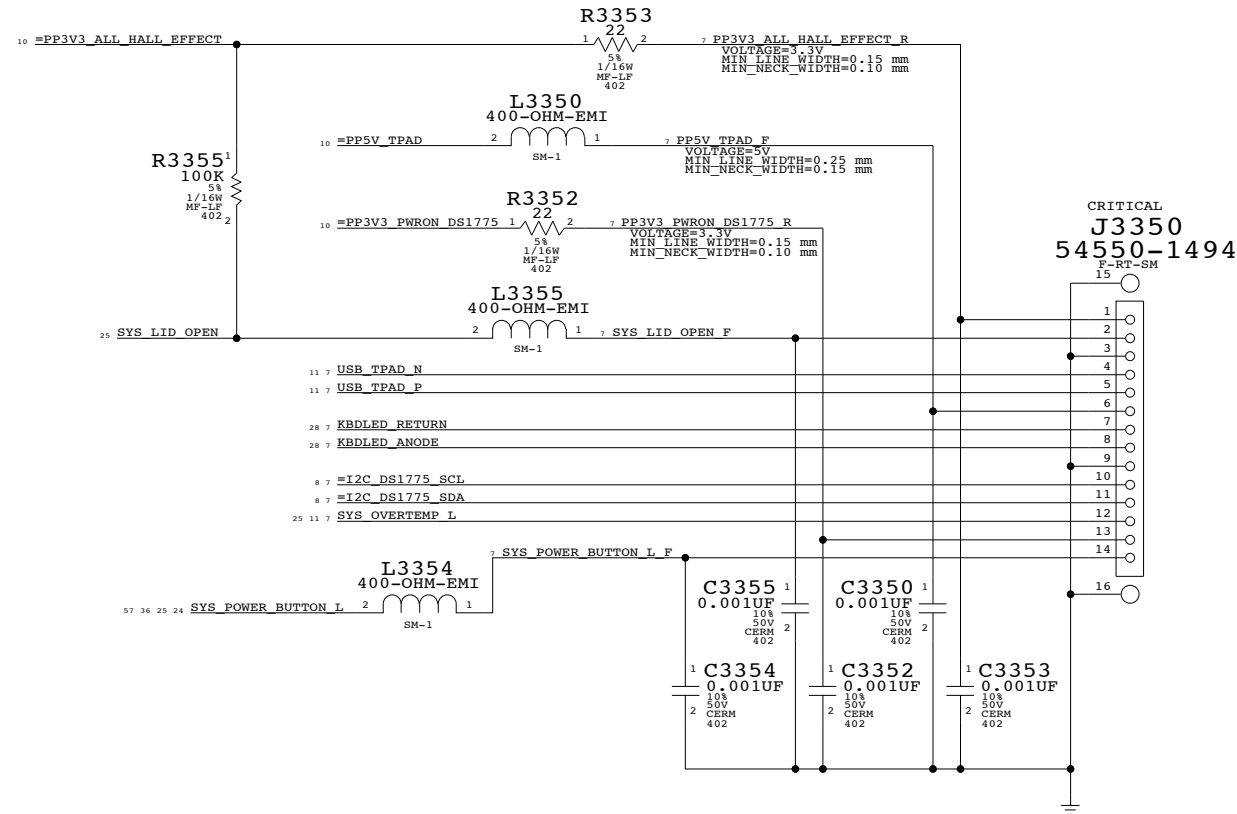
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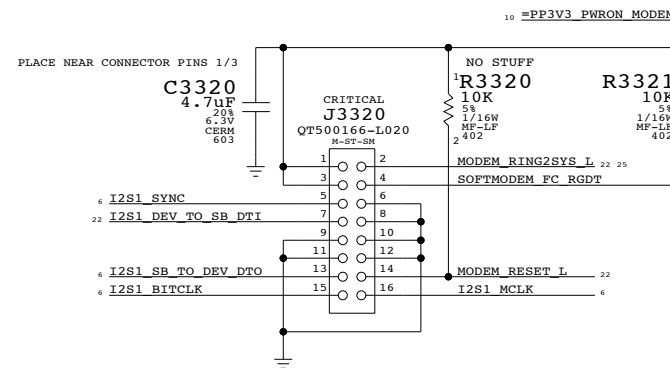
2

1

USB Trackpad Conn



SOFT MODEM CONN



Q41C Internal I/O I

SYNC_MASTER=N/A SYNC_DATE=N/A

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6839	E
SCALE	NONE	SHT	OF
		33	115

8

7

6

5

4

3

2

1

8

7

6

5

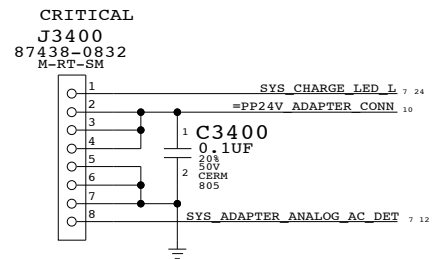
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3

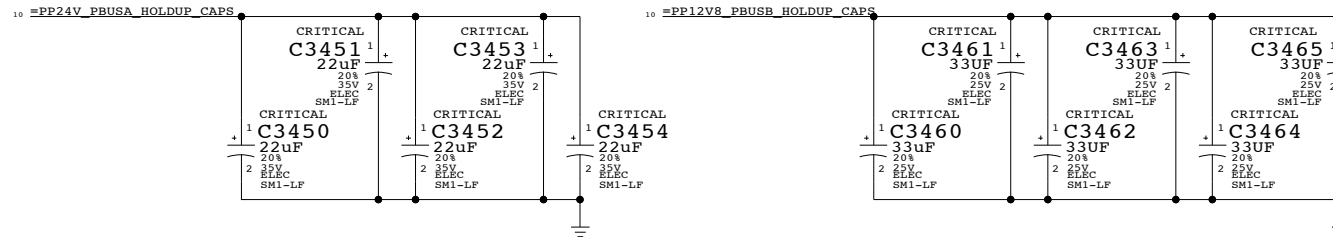
2

1

ADAPTER CONNECTOR



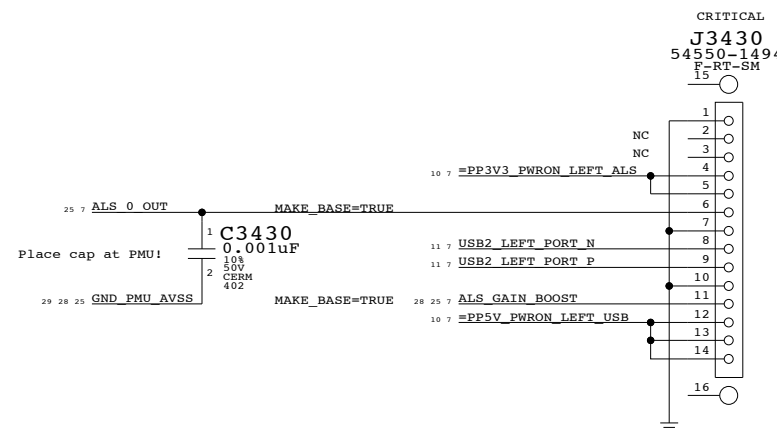
PBUS HOLD-UP CAPS



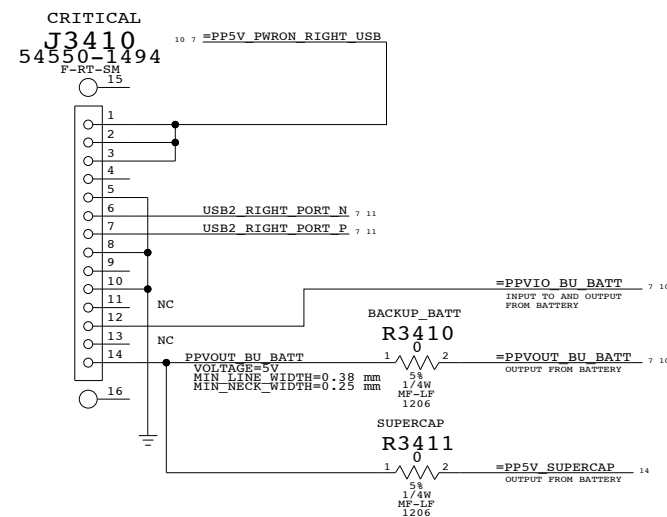
PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
12680085	12680080		C3450,C3451,C3452,C3453,C3454	primary is 246C/Alt. is 250C part

PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
12680084	12680079		C3460,C3461,C3462,C3463,C3464,C3465	primary is 246C/Alt. is 250C part

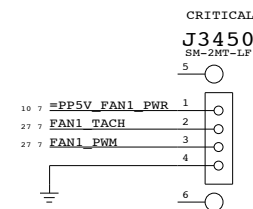
LEFT USB/LEFT ALS



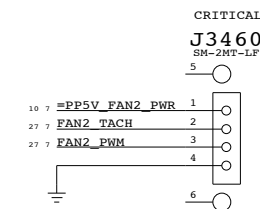
BACKUP BATTERY / RT USB CONNECTOR



CPU FAN



GPU FAN



Q41C Internal I/O II

SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-6839	E
SCALE	SHT OF		
NONE	34		115

8

7

6

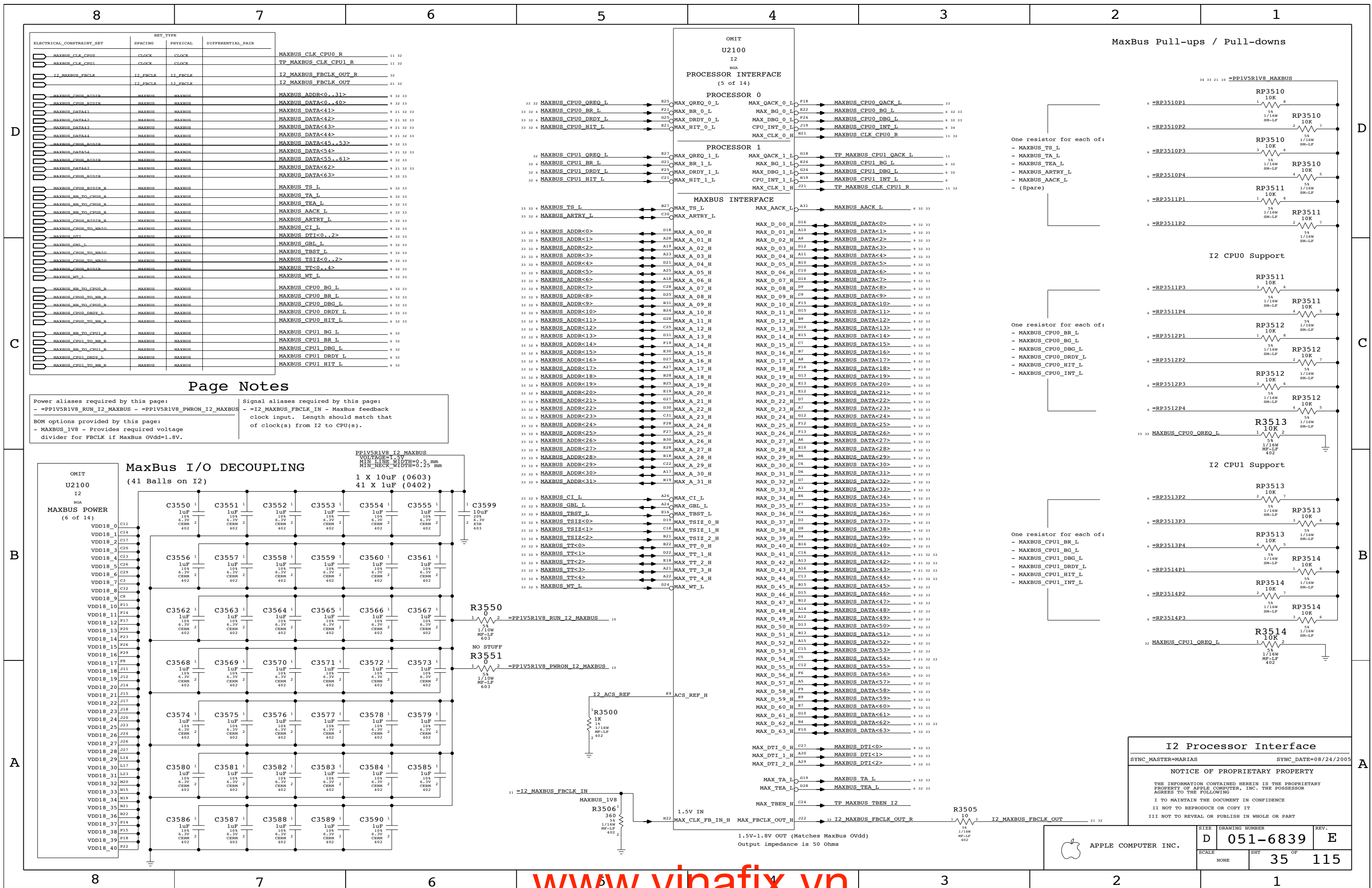
5

4

3

2

1



ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
MAXBUS_CLK_CPU0	CLOCK	CLOCK	
MAXBUS_CLK_CPU1	CLOCK	CLOCK	
I2_MAXBUS_FBCLK	I2_FBCLK	I2_FBCLK	
MAXBUS_CPU0_BNTR	MAXBUS	MAXBUS	
MAXBUS_CPU0_DRDY	MAXBUS	MAXBUS	
MAXBUS_CPU0_HIT	MAXBUS	MAXBUS	
MAXBUS_CPU0_OREQ	MAXBUS	MAXBUS	
MAXBUS_CPU0_BR	MAXBUS	MAXBUS	
MAXBUS_CPU0_DBG	MAXBUS	MAXBUS	
MAXBUS_CPU0_INT	MAXBUS	MAXBUS	
MAXBUS_CPU0_CLK	MAXBUS	MAXBUS	
MAXBUS_CPU1_BNTR	MAXBUS	MAXBUS	
MAXBUS_CPU1_DRDY	MAXBUS	MAXBUS	
MAXBUS_CPU1_HIT	MAXBUS	MAXBUS	
MAXBUS_CPU1_OREQ	MAXBUS	MAXBUS	
MAXBUS_CPU1_BR	MAXBUS	MAXBUS	
MAXBUS_CPU1_DBG	MAXBUS	MAXBUS	
MAXBUS_CPU1_INT	MAXBUS	MAXBUS	
MAXBUS_CPU1_CLK	MAXBUS	MAXBUS	
MAXBUS_TS_L	MAXBUS	MAXBUS	
MAXBUS_TA_L	MAXBUS	MAXBUS	
MAXBUS_TE_A_L	MAXBUS	MAXBUS	
MAXBUS_TB_A_L	MAXBUS	MAXBUS	
MAXBUS_TG_A_L	MAXBUS	MAXBUS	
MAXBUS_TH_A_L	MAXBUS	MAXBUS	
MAXBUS_TI_A_L	MAXBUS	MAXBUS	
MAXBUS_TJ_A_L	MAXBUS	MAXBUS	
MAXBUS_TK_A_L	MAXBUS	MAXBUS	
MAXBUS_TL_A_L	MAXBUS	MAXBUS	
MAXBUS_TM_A_L	MAXBUS	MAXBUS	
MAXBUS_TN_A_L	MAXBUS	MAXBUS	
MAXBUS_TO_A_L	MAXBUS	MAXBUS	
MAXBUS_TP_A_L	MAXBUS	MAXBUS	
MAXBUS_TQ_A_L	MAXBUS	MAXBUS	
MAXBUS_TR_A_L	MAXBUS	MAXBUS	
MAXBUS_TS_A_L	MAXBUS	MAXBUS	
MAXBUS_TT_A_L	MAXBUS	MAXBUS	
MAXBUS_TU_A_L	MAXBUS	MAXBUS	
MAXBUS_TV_A_L	MAXBUS	MAXBUS	
MAXBUS_TW_A_L	MAXBUS	MAXBUS	
MAXBUS_TX_A_L	MAXBUS	MAXBUS	
MAXBUS_TY_A_L	MAXBUS	MAXBUS	
MAXBUS_TZ_A_L	MAXBUS	MAXBUS	
MAXBUS_TA_L	MAXBUS	MAXBUS	
MAXBUS_TB_L	MAXBUS	MAXBUS	
MAXBUS_TC_L	MAXBUS	MAXBUS	
MAXBUS_TD_L	MAXBUS	MAXBUS	
MAXBUS_TE_L	MAXBUS	MAXBUS	
MAXBUS_TF_L	MAXBUS	MAXBUS	
MAXBUS_TG_L	MAXBUS	MAXBUS	
MAXBUS_TH_L	MAXBUS	MAXBUS	
MAXBUS_TI_L	MAXBUS	MAXBUS	
MAXBUS_TJ_L	MAXBUS	MAXBUS	
MAXBUS_TK_L	MAXBUS	MAXBUS	
MAXBUS_TL_L	MAXBUS	MAXBUS	
MAXBUS_TM_L	MAXBUS	MAXBUS	
MAXBUS_TN_L	MAXBUS	MAXBUS	
MAXBUS_TO_L	MAXBUS	MAXBUS	
MAXBUS_TP_L	MAXBUS	MAXBUS	
MAXBUS_TQ_L	MAXBUS	MAXBUS	
MAXBUS_TR_L	MAXBUS	MAXBUS	
MAXBUS_TS_L	MAXBUS	MAXBUS	
MAXBUS_TT_L	MAXBUS	MAXBUS	
MAXBUS_TU_L	MAXBUS	MAXBUS	
MAXBUS_TV_L	MAXBUS	MAXBUS	
MAXBUS_TW_L	MAXBUS	MAXBUS	
MAXBUS_TX_L	MAXBUS	MAXBUS	
MAXBUS_TY_L	MAXBUS	MAXBUS	
MAXBUS_TZ_L	MAXBUS	MAXBUS	

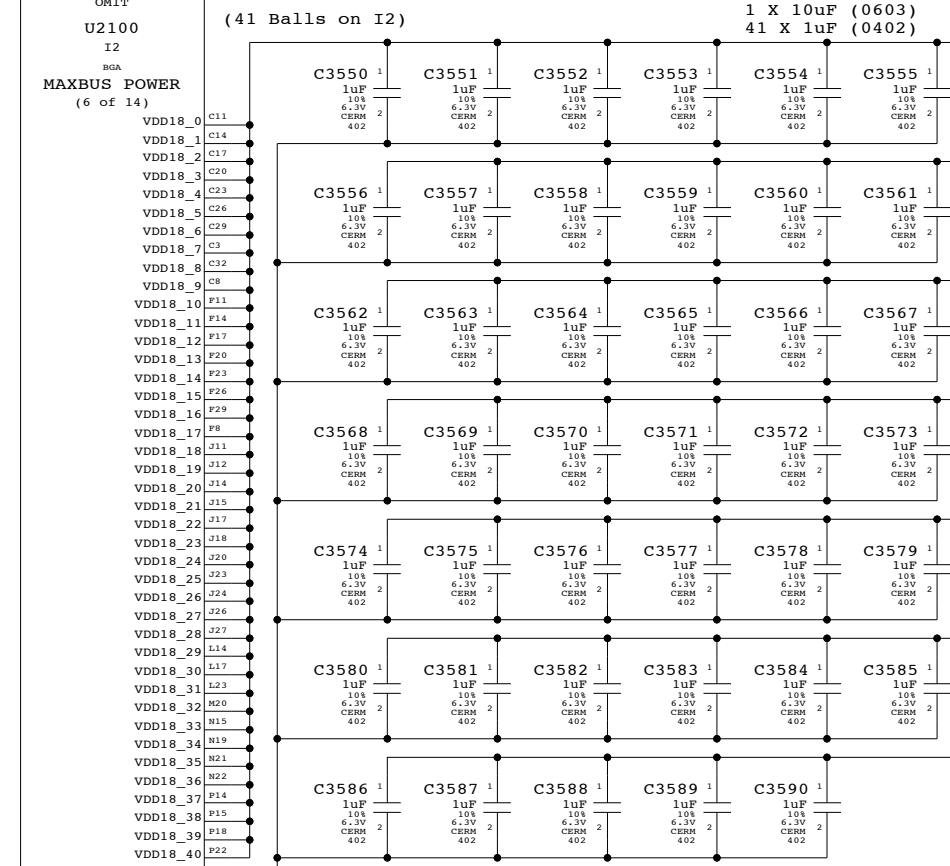
Page Notes

Power aliases required by this page:
 - =PPIV5R1V8_RUN_I2_MAXBUS - =PPIV5R1V8_PWRON_I2_MAXBUS

Signal aliases required by this page:
 - =I2_MAXBUS_FBCLK_IN - MaxBus feedback clock input. Length should match that of clock(s) from I2 to CPU(s).

BOM options provided by this page:
 - MAXBUS_V18 - Provides required voltage divider for FBCLK if MaxBus OVdd=1.8V.

MaxBus I/O DECOUPLING



I2 Processor Interface

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE	SHT	OF
NONE	35	115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		DIFFERENTIAL_PAIR
	SPACING	PHYSICAL	
R3320	CLOCK	CLOCK	

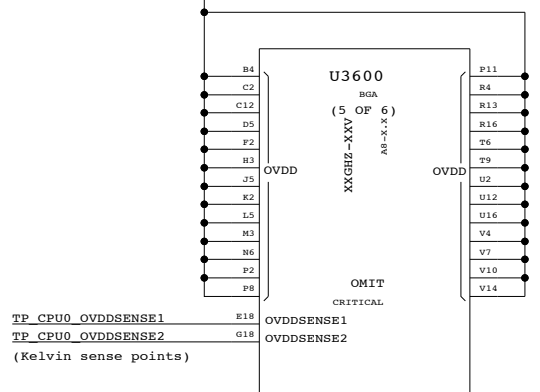
Page Notes

Power aliases required by this page:
 - =PP1V5R1V8_MAXBUS

Signal aliases required by this page:
 - =MAXBUS_CPU0_CLK

BOM options provided by this page:
 (NONE)

34 33 32 21 10 =PP1V5R1V8_MAXBUS

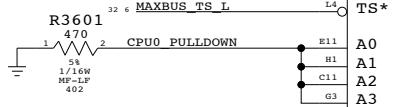
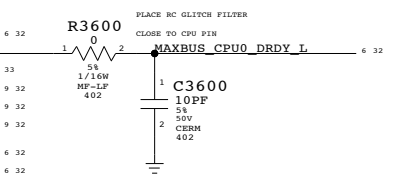


32 9	MAXBUS_DATA<0>	R15	D0
32 9	MAXBUS_DATA<1>	M15	D1
32 9	MAXBUS_DATA<2>	T14	D2
32 9	MAXBUS_DATA<3>	V16	D3
32 9	MAXBUS_DATA<4>	W16	D4
32 9	MAXBUS_DATA<5>	T15	D5
32 9	MAXBUS_DATA<6>	U15	D6
32 9	MAXBUS_DATA<7>	P14	D7
32 9	MAXBUS_DATA<8>	V13	D8
32 9	MAXBUS_DATA<9>	W13	D9
32 9	MAXBUS_DATA<10>	T13	D10
32 9	MAXBUS_DATA<11>	P13	D11
32 9	MAXBUS_DATA<12>	U14	D12
32 9	MAXBUS_DATA<13>	W14	D13
32 9	MAXBUS_DATA<14>	R12	D14
32 9	MAXBUS_DATA<15>	T12	D15
32 9	MAXBUS_DATA<16>	W12	D16
32 9	MAXBUS_DATA<17>	V12	D17
32 9	MAXBUS_DATA<18>	M11	D18
32 9	MAXBUS_DATA<19>	M10	D19
32 9	MAXBUS_DATA<20>	R11	D20
32 9	MAXBUS_DATA<21>	U11	D21
32 9	MAXBUS_DATA<22>	M11	D22
32 9	MAXBUS_DATA<23>	T11	D23
32 9	MAXBUS_DATA<24>	R10	D24
32 9	MAXBUS_DATA<25>	N9	D25
32 9	MAXBUS_DATA<26>	P10	D26
32 9	MAXBUS_DATA<27>	U10	D27
32 9	MAXBUS_DATA<28>	R9	D28
32 9	MAXBUS_DATA<29>	W10	D29
32 9	MAXBUS_DATA<30>	U9	D30
32 9	MAXBUS_DATA<31>	V9	D31
32 9	MAXBUS_DATA<32>	W5	D32
32 9	MAXBUS_DATA<33>	U6	D33
32 9	MAXBUS_DATA<34>	T5	D34
32 9	MAXBUS_DATA<35>	U5	D35
32 9	MAXBUS_DATA<36>	W7	D36
32 9	MAXBUS_DATA<37>	R6	D37
32 9	MAXBUS_DATA<38>	P7	D38
32 9	MAXBUS_DATA<39>	V6	D39
32 9	MAXBUS_DATA<40>	P17	D40
32 21 9	MAXBUS_DATA<41>	R19	D41
32 21 9	MAXBUS_DATA<42>	V18	D42
32 21 9	MAXBUS_DATA<43>	R18	D43
32 21 9	MAXBUS_DATA<44>	V19	D44
32 9	MAXBUS_DATA<45>	T19	D45
32 9	MAXBUS_DATA<46>	U19	D46
32 9	MAXBUS_DATA<47>	M19	D47
32 9	MAXBUS_DATA<48>	U18	D48
32 9	MAXBUS_DATA<49>	W17	D49
32 9	MAXBUS_DATA<50>	W18	D50
32 9	MAXBUS_DATA<51>	T18	D51
32 9	MAXBUS_DATA<52>	T18	D52
32 9	MAXBUS_DATA<53>	T17	D53
32 21 9	MAXBUS_DATA<54>	W3	D54
32 9	MAXBUS_DATA<55>	V17	D55
32 9	MAXBUS_DATA<56>	U4	D56
32 9	MAXBUS_DATA<57>	U8	D57
32 9	MAXBUS_DATA<58>	U7	D58
32 9	MAXBUS_DATA<59>	R7	D59
32 9	MAXBUS_DATA<60>	P6	D60
32 9	MAXBUS_DATA<61>	R8	D61
32 21 9	MAXBUS_DATA<62>	W8	D62
32 9	MAXBUS_DATA<63>	T8	D63

U3600
 BGA
 (2 OF 6)
 XXGHZ-XXV
 AB-X-X

OMIT
 CRITICAL

DP0	T3	NC
DP1	W4	NC
DP2	T4	NC
DP3	W9	NC
DP4	M6	NC
DP5	V3	NC
DP6	N6	NC
DP7	W6	NC
DBG*	N2	MAXBUS_CPU0_DBG_L
DRDY*	R3	MAXBUS_CPU0_DRDY_L_R
DTIO	G1	MAXBUS_EDTI
DTI1	K1	MAXBUS_DTI<0>
DTI2	P1	MAXBUS_DTI<1>
DTI3	N1	MAXBUS_DTI<2>
TA*	K6	MAXBUS_TA_L
TEA*	L1	MAXBUS_TEA_L
HIT*	N2	MAXBUS_CPU0_HIT_L



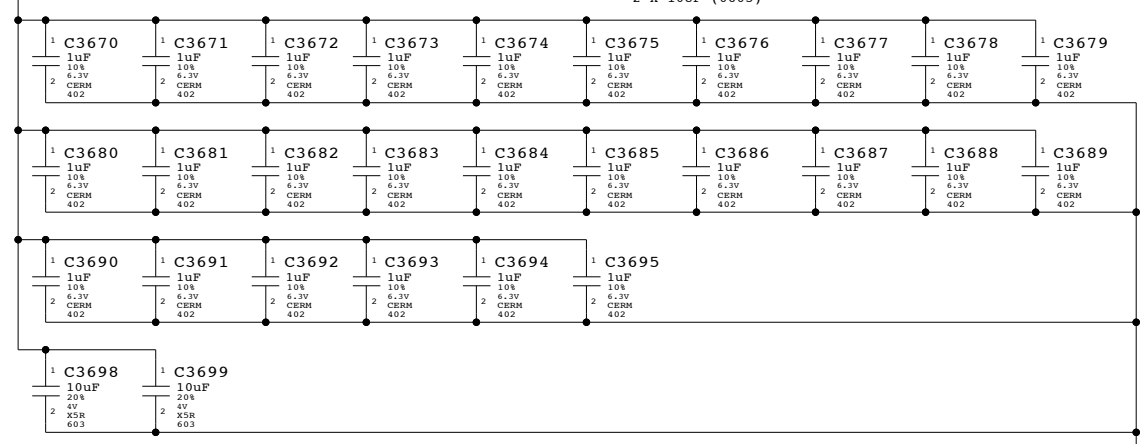
U3600
 BGA
 (1 OF 6)
 XXGHZ-XXV
 AB-X-X

OMIT
 CRITICAL

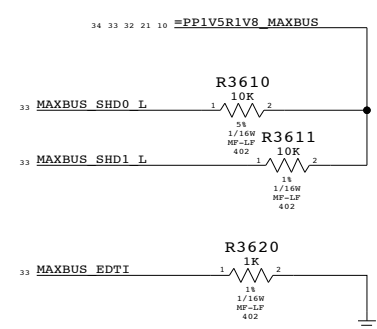
AP0	C1	NC
AP1	E2	NC
AP2	H6	NC
AP3	F5	NC
AP4	G7	NC
TT0	R5	MAXBUS_TT<0>
TT1	E6	MAXBUS_TT<1>
TT2	F6	MAXBUS_TT<2>
TT3	E9	MAXBUS_TT<3>
TT4	C5	MAXBUS_TT<4>
TBST*	F11	MAXBUS_TBST_L
TSIZ0	G6	MAXBUS_TSIZ<0>
TSIZ1	F7	MAXBUS_TSIZ<1>
TSIZ2	E7	MAXBUS_TSIZ<2>
GBL*	B2	MAXBUS_GBL_L
WT*	D3	MAXBUS_WT_L
CI*	J1	MAXBUS_CI_L
AACK*	R1	MAXBUS_AACK_L
ARTRY*	N2	MAXBUS_ARTRY_L
SHD0*	E4	MAXBUS_SHD0_L
SHD1*	H5	MAXBUS_SHD1_L
SYSCLK	A10	=MAXBUS_CPU0_CLK
CLK_OUT	H2	TP_CPU0_CLKOUT
TBEN	E1	MAXBUS_TBEN
QREQ*	F4	MAXBUS_CPU0_QREQ_L
QACK*	G5	MAXBUS_CPU0_QACK_L
CKSTP_IN*	A3	
CKSTP_OUT*	B1	CPU_CHKSTP_OUT_L

=PP1V5R1V8_MAXBUS 10 21 32 33 34

VIO DECOUPLING (28 PINS)



MAXBUS Straps



A8 MaxBus (CPU0)
 SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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SCALE	SHT	OF	
NONE	36	115	

Page Notes

Power aliases required by this page:

- =PPIV5R1V8_MAXBUS
- =PP3V3_PWRON_PLLSEL

Signal aliases required by this page:

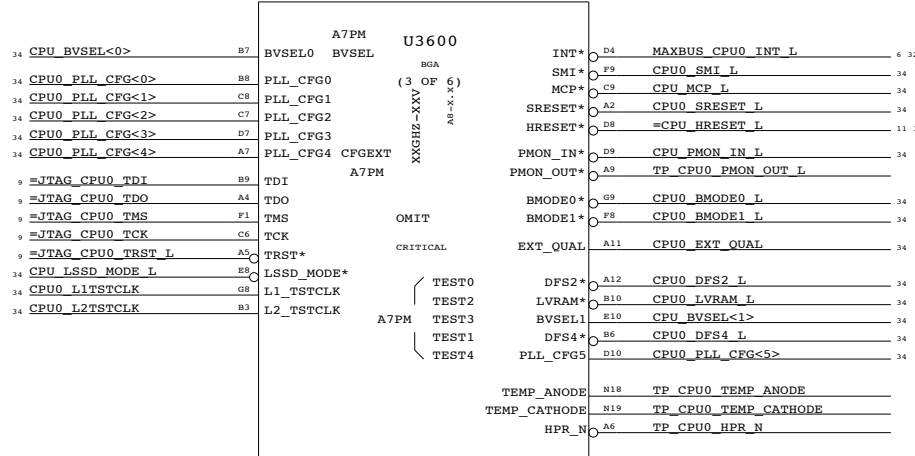
- =CPU0_JTAG_TDI
- =CPU0_JTAG_TDO
- =CPU0_JTAG_TMS
- =CPU0_JTAG_TCK
- =CPU0_JTAG_TRST_L
- =CPU_HRESET_L (Reset given to all processors)

BOM options provided by this page:

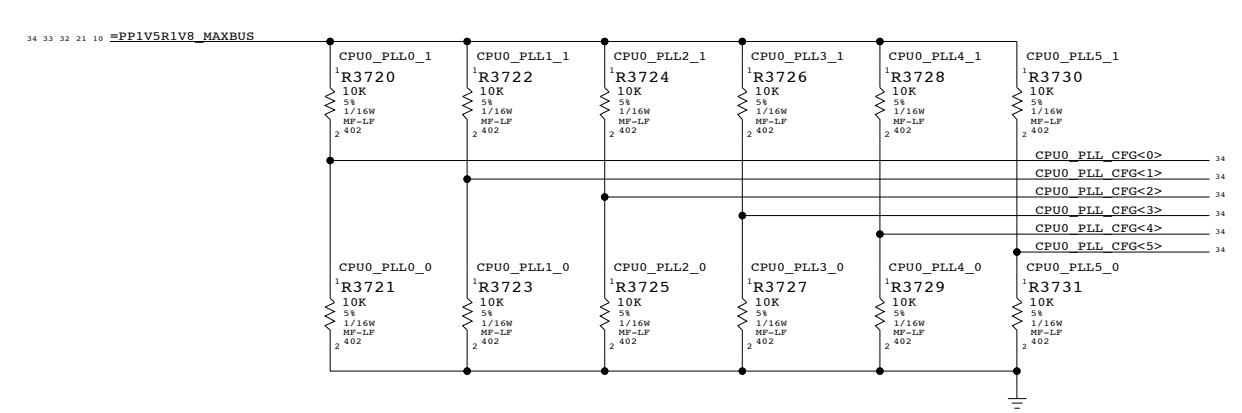
- CPU0_PLL0_0/1
- CPU0_PLL1_0/1
- CPU0_PLL2_0/1
- CPU0_PLL3_0/1
- CPU0_PLL4_0/1
- CPU0_PLL5_0/1

These must be selected to set the CPU core to Maxbus frequency ratio to attain the desired spec

- MAXBUS_1V5 - MAXBUS_1V8
- One of these must be selected to set the Maxbus voltage
- * the MAXBUS_1V5 option does not exist for A7PM
- CPU_A7PM - CPU_A8
- One of these must be selected to ensure the the above strap is interpreted correctly

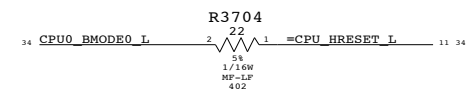


CPU0 PLL CONFIG CIRCUITRY

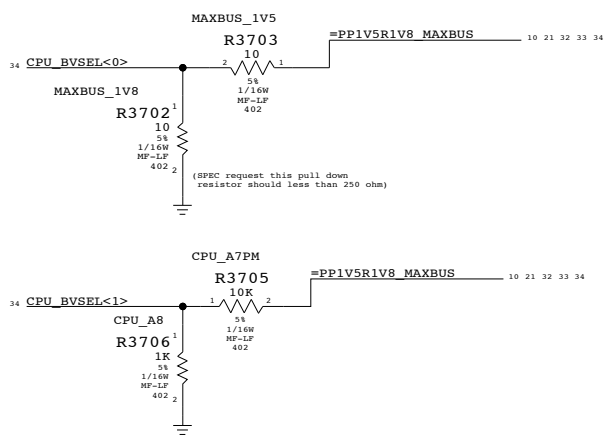


BUS TYPE SELECT

SIGNAL	TIED	MODE
CPU0_BMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE



MAXBUS VSEL

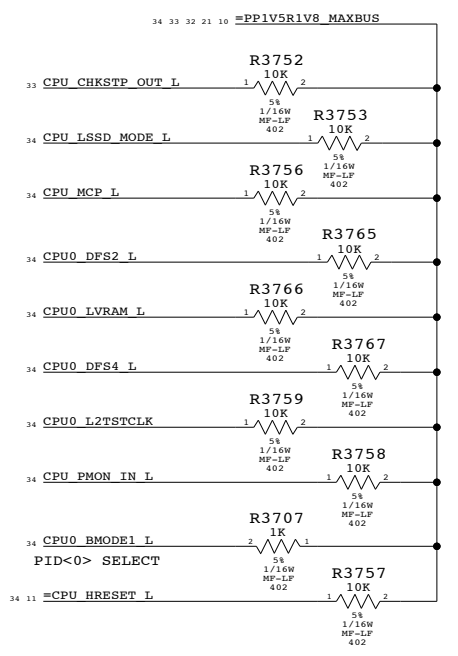


CPU0 FREQUENCY CONFIGURATION

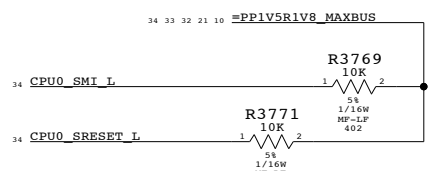
() Indicates DFS setting supported by A8 only

BOM GROUP	DFS SUPPORT	F/2	F/4	PLL BITS 012345	BOM OPTIONS
CPU0_BUSRATIO_1.0X	-	-	-	001100	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_2.0X	-	-	-	010000	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_3.0X	-	-	-	100000	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_4.0X	2.0X	-	-	101000	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_5.0X	2.5X	-	-	101100	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_5.5X	(2.75X)	-	-	100100	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_6.0X	3.0X	-	-	110100	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_6.5X	(3.25X)	-	-	010100	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_7.0X	3.5X	-	-	001000	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_7.5X	(3.75X)	-	-	000100	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_8.0X	4.0X	2.0X	-	110000	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_8.5X	(4.25X)	-	-	011000	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_9.0X	4.5X	(2.25X)	-	011100	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_9.5X	(4.75X)	-	-	011100	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_10.0X	5.0X	2.5X	-	101010	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_10.5X	(5.25X)	-	-	100010	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_11.0X	5.5X	(2.75X)	-	100110	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_11.5X	(5.75X)	-	-	000000	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_12.0X	6.0X	3.0X	-	101110	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_12.5X	(6.25X)	-	-	111110	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_13.0X	6.5X	(3.25X)	-	010110	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_13.5X	(6.75X)	-	-	111000	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_14.0X	7.0X	3.5X	-	110010	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_15.0X	7.5X	(3.75X)	-	000110	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_16.0X	8.0X	4.0X	-	110110	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_17.0X	8.5X	(4.25X)	-	000010	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_18.0X	9.0X	4.5X	-	001010	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_20.0X	10.0X	5.0X	-	001110	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_21.0X	10.5X	(5.25X)	-	010010	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_24.0X	12.0X	6.0X	-	011010	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_28.0X	14.0X	7.0X	-	111010	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0

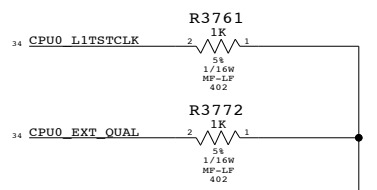
CPU PULLUPS



INTERRUPT PULL-UPS



CPU PULLDOWNS



A8 Configuration Straps

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6839	E
SCALE	NONE	SHT	OF
		37	115

Page Notes

Power aliases required by this page:
 - =PPVCORE_CPU0

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

D

C

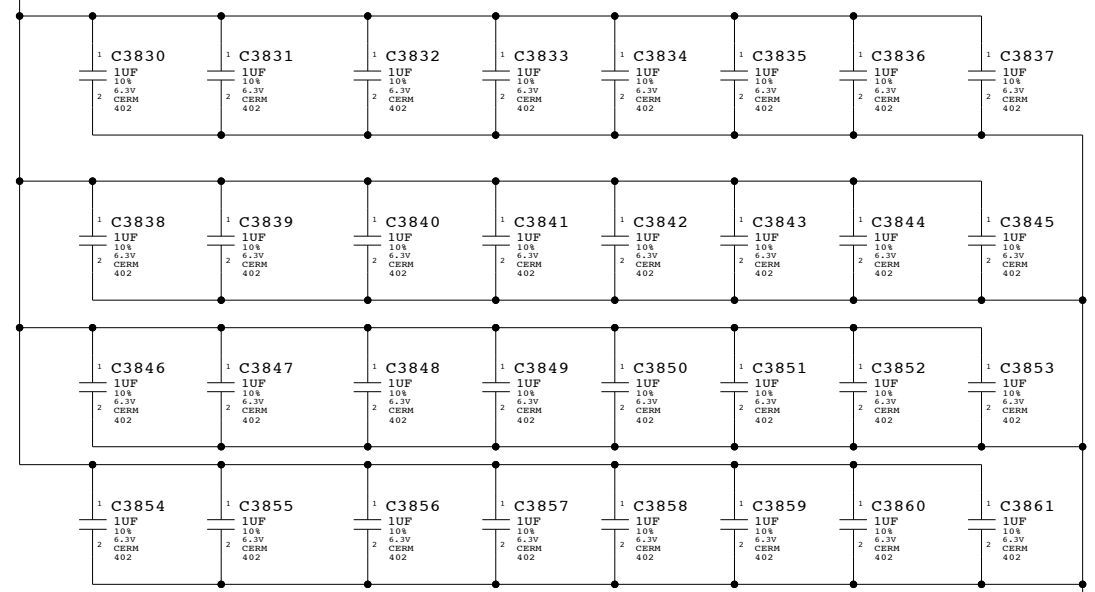
B

A

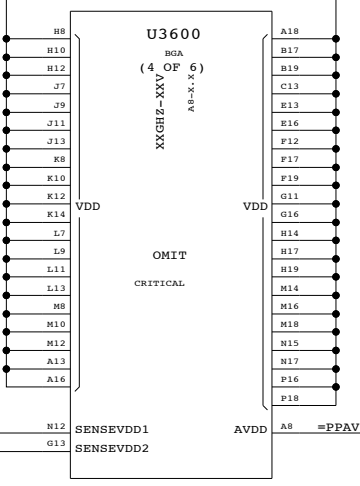
8 7 6 5 4 3 2 1

VCORE BULK CAPS

40 X 1 UF (0402)

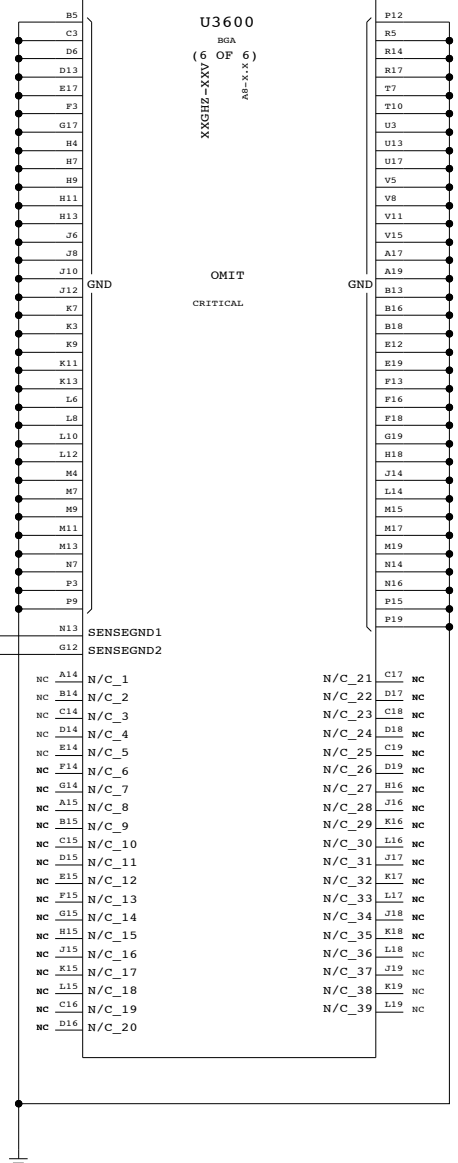


35 10 =PPVCORE_CPU0



TP_CPU0_SENSEGND1
 TP_CPU0_SENSEGND2
 (Kelvin sense points)

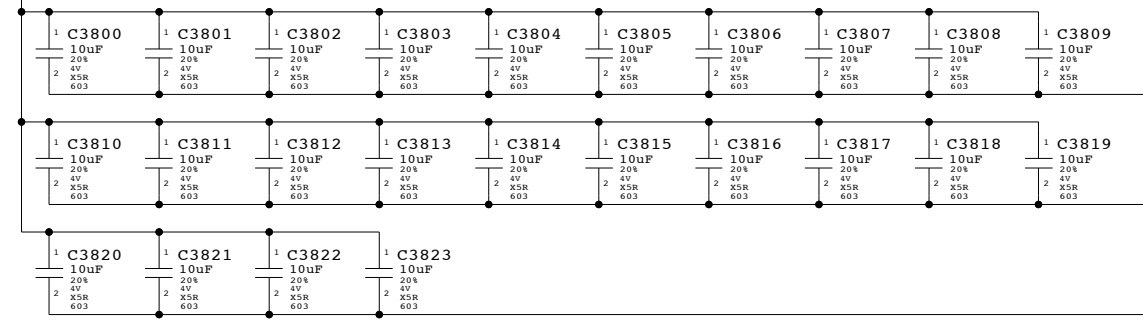
AVDD A8 =PPAVDD_CPU0 10



U3600
 BGA
 (6 OF 6)
 AB=X.X
 OMIT
 CRITICAL

35 10 =PPVCORE_CPU0

24 X 10 UF (0603)



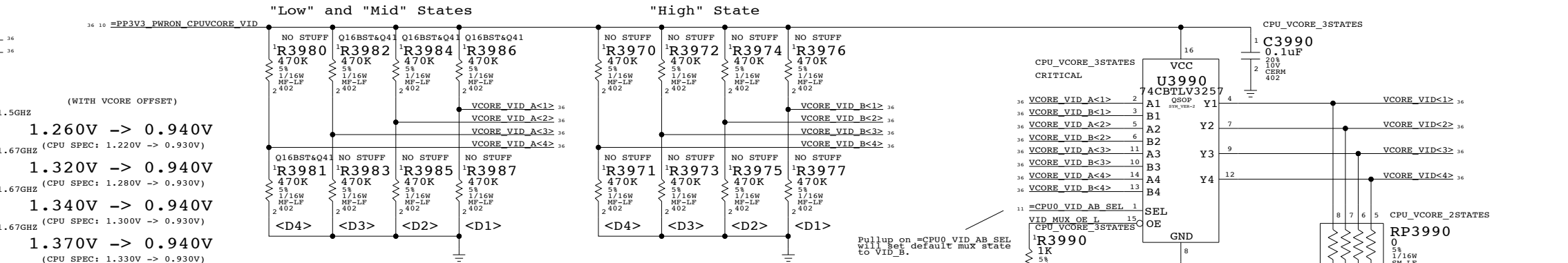
A8 Power (CPU0)
 SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6839	E
SCALE	SHT OF		
NONE	38 OF		115

8 7 6 5 4 3 2 1

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
MEM	THERM	THERM	
MEM	THERM	THERM	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11480270	1	RES, 3.48K, 1%, 1/16W, MF-LF, 402, SMD	R3946	CPU0_VCORE_IV22
11480258	1	RES, 2.61K, 1%, 1/16W, MF-LF, 402, SMD	R3944	CPU0_VCORE_IV22
11480246	1	RES, 2.0K, 1%, 1/16W, MF-LF, 402, SMD	R3946	CPU0_VCORE_IV28
11480294	1	RES, 6.04K, 1%, 1/16W, MF-LF, 402, SMD	R3944	CPU0_VCORE_IV28
11480276	1	RES, 4.02K, 1%, 1/16W, MF-LF, 402, SMD	R3946	CPU0_VCORE_IV30
11480254	1	RES, 2.43K, 1%, 1/16W, MF-LF, 402, SMD	R3944	CPU0_VCORE_IV30
11480246	1	RES, 2.0K, 1%, 1/16W, MF-LF, 402, SMD	R3946	CPU0_VCORE_IV33
11480294	1	RES, 6.04K, 1%, 1/16W, MF-LF, 402, SMD	R3944	CPU0_VCORE_IV33



(WITH VCORE OFFSET)

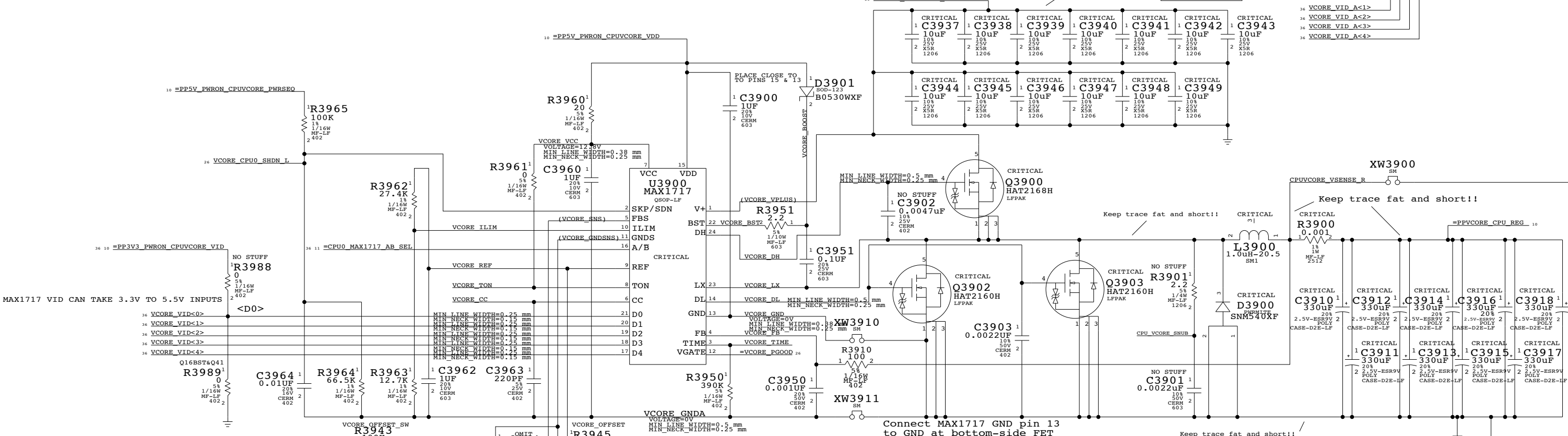
1.5GHZ
1.260V -> 0.940V
(CPU SPEC: 1.220V -> 0.930V)

1.67GHZ
1.320V -> 0.940V
(CPU SPEC: 1.280V -> 0.930V)

1.67GHZ
1.340V -> 0.940V
(CPU SPEC: 1.300V -> 0.930V)

1.67GHZ
1.370V -> 0.940V
(CPU SPEC: 1.330V -> 0.930V)

Keep trace fat (1.00-2.54 mm) and short!!



OUTPUT VOLTAGE

VDAC	D4	D3	D2	D1	D0
2.00	1	275	0	0	0
1.95	1	250	0	0	0
1.90	1	225	0	0	1
1.85	1	200	0	1	1
1.80	1	175	0	1	0
1.75	1	150	0	1	0
1.70	1	125	0	1	1
1.65	1	100	0	1	1
1.60	1	075	1	0	0
1.55	1	050	1	0	1
1.50	1	025	1	0	0
1.45	1	000	1	0	1
1.40	0	975	1	1	0
1.35	0	950	1	1	0
1.30	0	925	1	1	0
NO CPU	NO CPU		1	1	1

FOR V-STEP:

D<4..0>	A/B_ =	
	Hi/Fast	Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

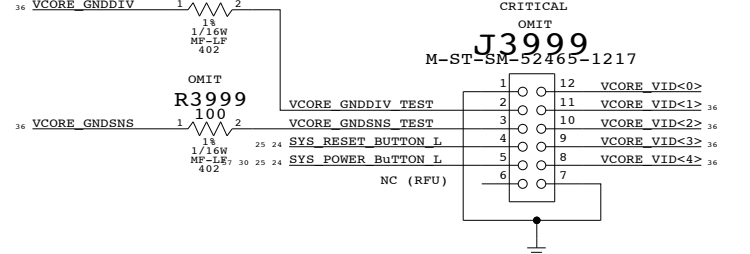
When A/B_ is high (fast): D4-D0 read as-is
 When A/B_ is low (slow): <=1K-ohm -> 0
 >=100K-ohm -> 1
 If all pull-ups are >=100K and all pull-downs are <=1K, V_A = V_B.

GROUND SENSE VOLTAGE DIVIDER
 This allows for an offset to the ground sense to adjust the output voltage.
 $V_{REF} = 2.0V$ WITH A 0.85 SCALE FACTOR, HENCE $V_{OFFSET} = 1.7V * (R1/(R1+R2))$ AND $V_{CORE} = V_{DAC} + V_{OFFSET}$.

NOTE: R3945 (R2) NO STUFFED FOR NO OFFSET CASE

ROUTE AS DIFFERENTIAL PAIR

FMAX CONNECTOR



CPU VCore Supply

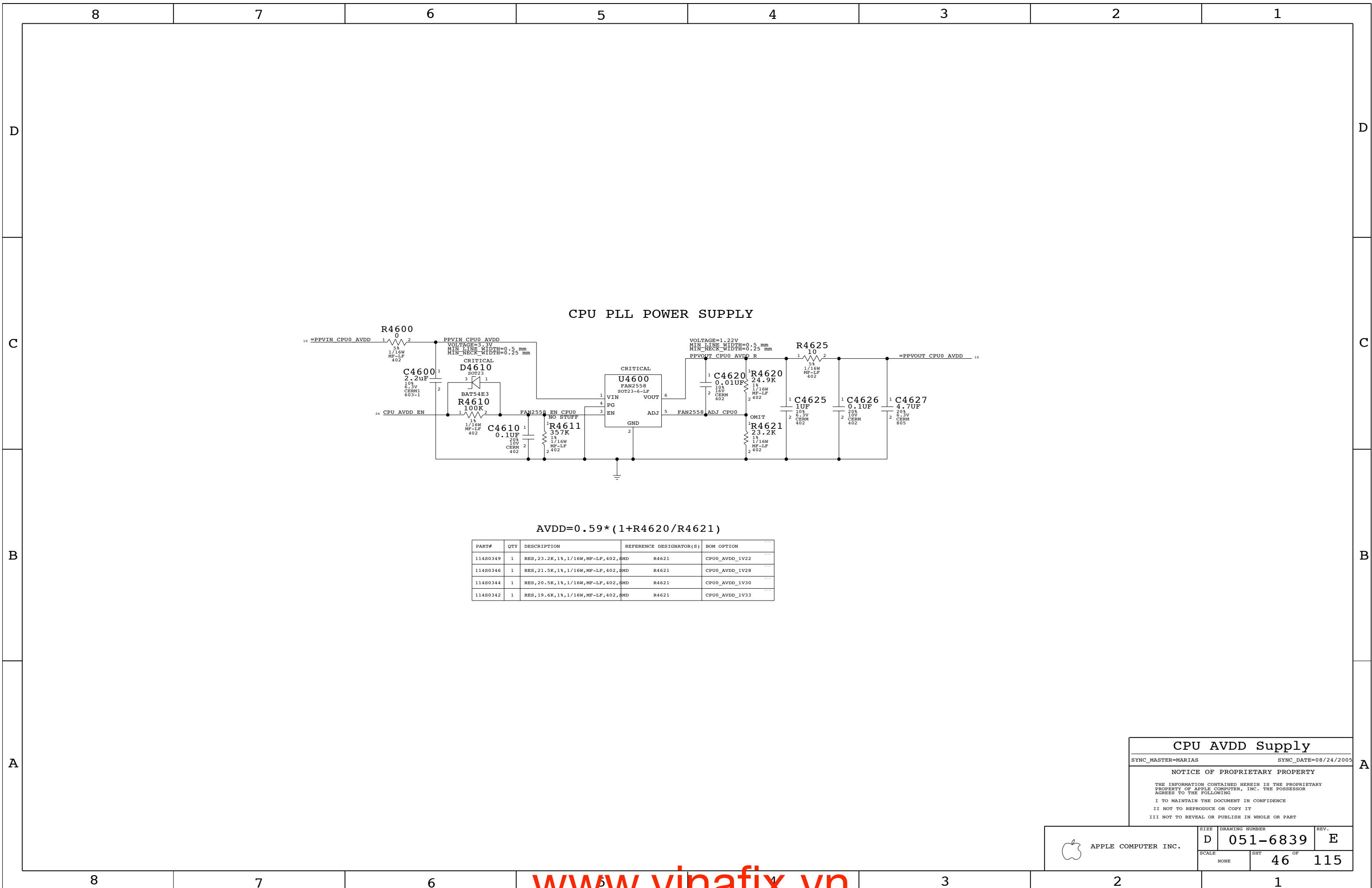
SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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D	051-6839	E
SCALE	SHEET	OF
NONE	39	115



CPU PLL POWER SUPPLY

$$AVDD = 0.59 * (1 + R4620 / R4621)$$

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11480349	1	RES, 23.2K, 1%, 1/16W, MF-LF, 402, SMD	R4621	CPU0_AVDD_1V22
11480346	1	RES, 21.5K, 1%, 1/16W, MF-LF, 402, SMD	R4621	CPU0_AVDD_1V28
11480344	1	RES, 20.5K, 1%, 1/16W, MF-LF, 402, SMD	R4621	CPU0_AVDD_1V30
11480342	1	RES, 19.6K, 1%, 1/16W, MF-LF, 402, SMD	R4621	CPU0_AVDD_1V33

CPU AVDD Supply

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

NOTICE OF PROPRIETARY PROPERTY

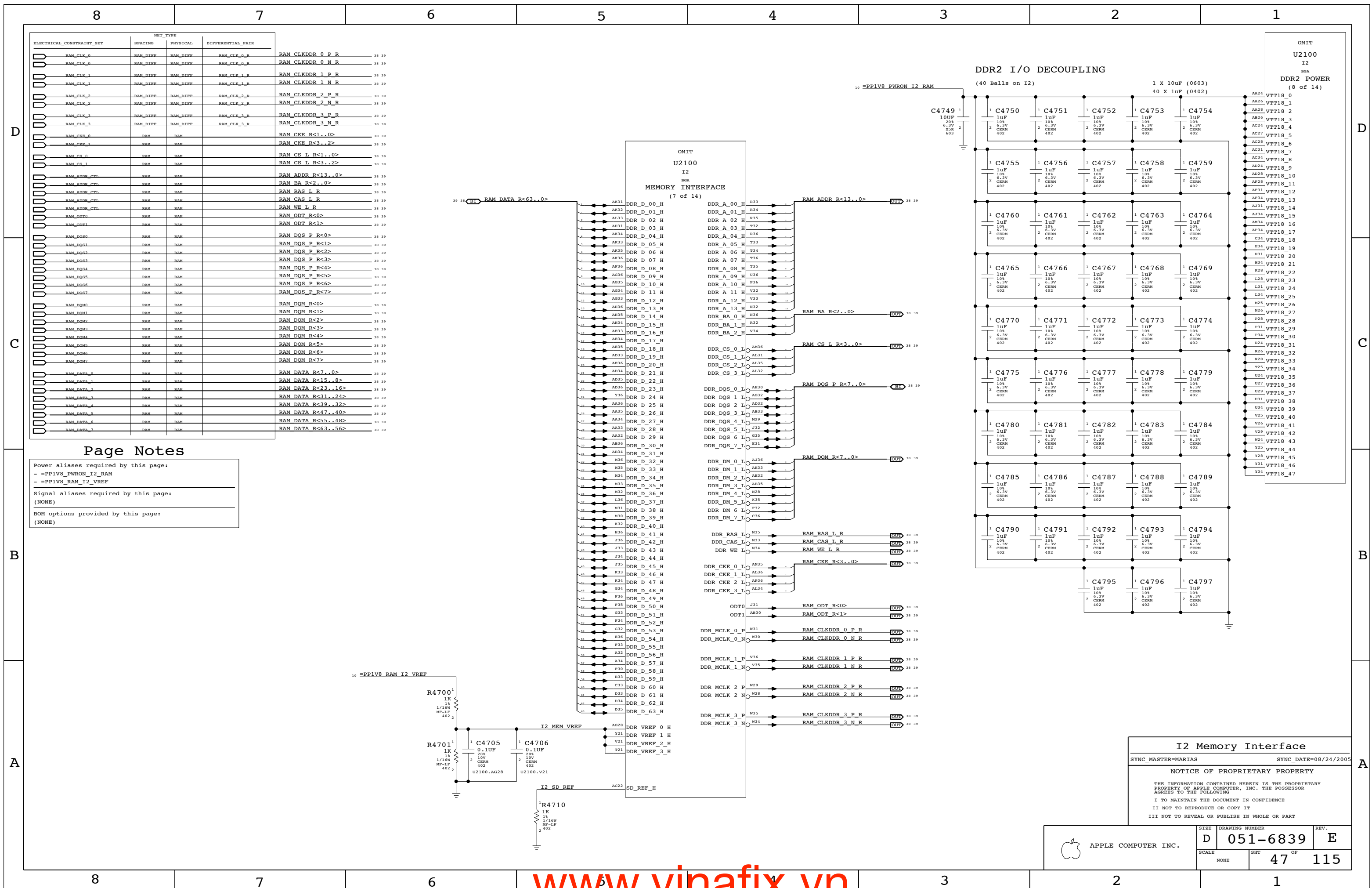
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	D	051-6839	E
SCALE	SHT		OF
NONE	46		115



ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	NET_TYPE
				RAM_CLK_0
				RAM_CLK_1
				RAM_CLK_2
				RAM_CLK_3
				RAM_CKE_0
				RAM_CKE_1
				RAM_CS_0
				RAM_CS_1
				RAM_ADDR_CTL_0
				RAM_ADDR_CTL_1
				RAM_ADDR_CTL_2
				RAM_ADDR_CTL_3
				RAM_ODT_0
				RAM_ODT_1
				RAM_ODT_2
				RAM_ODT_3
				RAM_DQS_0
				RAM_DQS_1
				RAM_DQS_2
				RAM_DQS_3
				RAM_DQS_4
				RAM_DQS_5
				RAM_DQS_6
				RAM_DQS_7
				RAM_DQM_0
				RAM_DQM_1
				RAM_DQM_2
				RAM_DQM_3
				RAM_DQM_4
				RAM_DQM_5
				RAM_DQM_6
				RAM_DQM_7
				RAM_DATA_0
				RAM_DATA_1
				RAM_DATA_2
				RAM_DATA_3
				RAM_DATA_4
				RAM_DATA_5
				RAM_DATA_6
				RAM_DATA_7

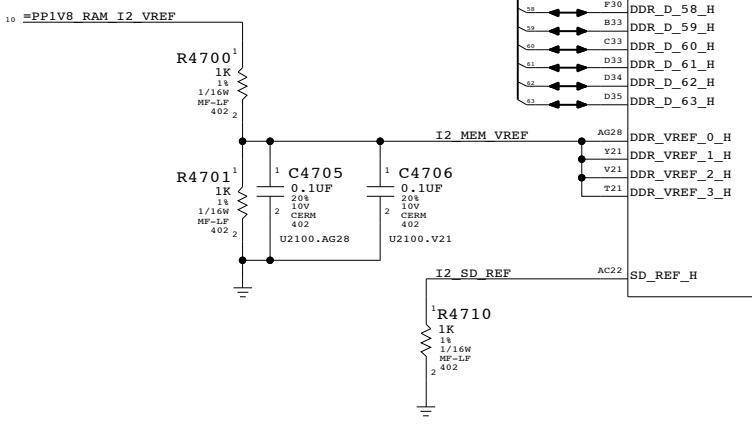
				RAM_CLKDDR_0_P_R
				RAM_CLKDDR_0_N_R
				RAM_CLKDDR_1_P_R
				RAM_CLKDDR_1_N_R
				RAM_CLKDDR_2_P_R
				RAM_CLKDDR_2_N_R
				RAM_CLKDDR_3_P_R
				RAM_CLKDDR_3_N_R
				RAM_CKE_R<1..0>
				RAM_CKE_R<3..2>
				RAM_CS_L_R<1..0>
				RAM_CS_L_R<3..2>
				RAM_ADDR_R<13..0>
				RAM_BA_R<2..0>
				RAM_RAS_L_R
				RAM_CAS_L_R
				RAM_WE_L_R
				RAM_ODT_R<0>
				RAM_ODT_R<1>
				RAM_DQS_P_R<0>
				RAM_DQS_P_R<1>
				RAM_DQS_P_R<2>
				RAM_DQS_P_R<3>
				RAM_DQS_P_R<4>
				RAM_DQS_P_R<5>
				RAM_DQS_P_R<6>
				RAM_DQS_P_R<7>
				RAM_DQM_R<0>
				RAM_DQM_R<1>
				RAM_DQM_R<2>
				RAM_DQM_R<3>
				RAM_DQM_R<4>
				RAM_DQM_R<5>
				RAM_DQM_R<6>
				RAM_DQM_R<7>
				RAM_DATA_R<7..0>
				RAM_DATA_R<15..8>
				RAM_DATA_R<23..16>
				RAM_DATA_R<31..24>
				RAM_DATA_R<39..32>
				RAM_DATA_R<47..40>
				RAM_DATA_R<55..48>
				RAM_DATA_R<63..56>

Page Notes

Power aliases required by this page:
 - =PP1V8_PWRON_I2_RAM
 - =PP1V8_RAM_I2_VREF

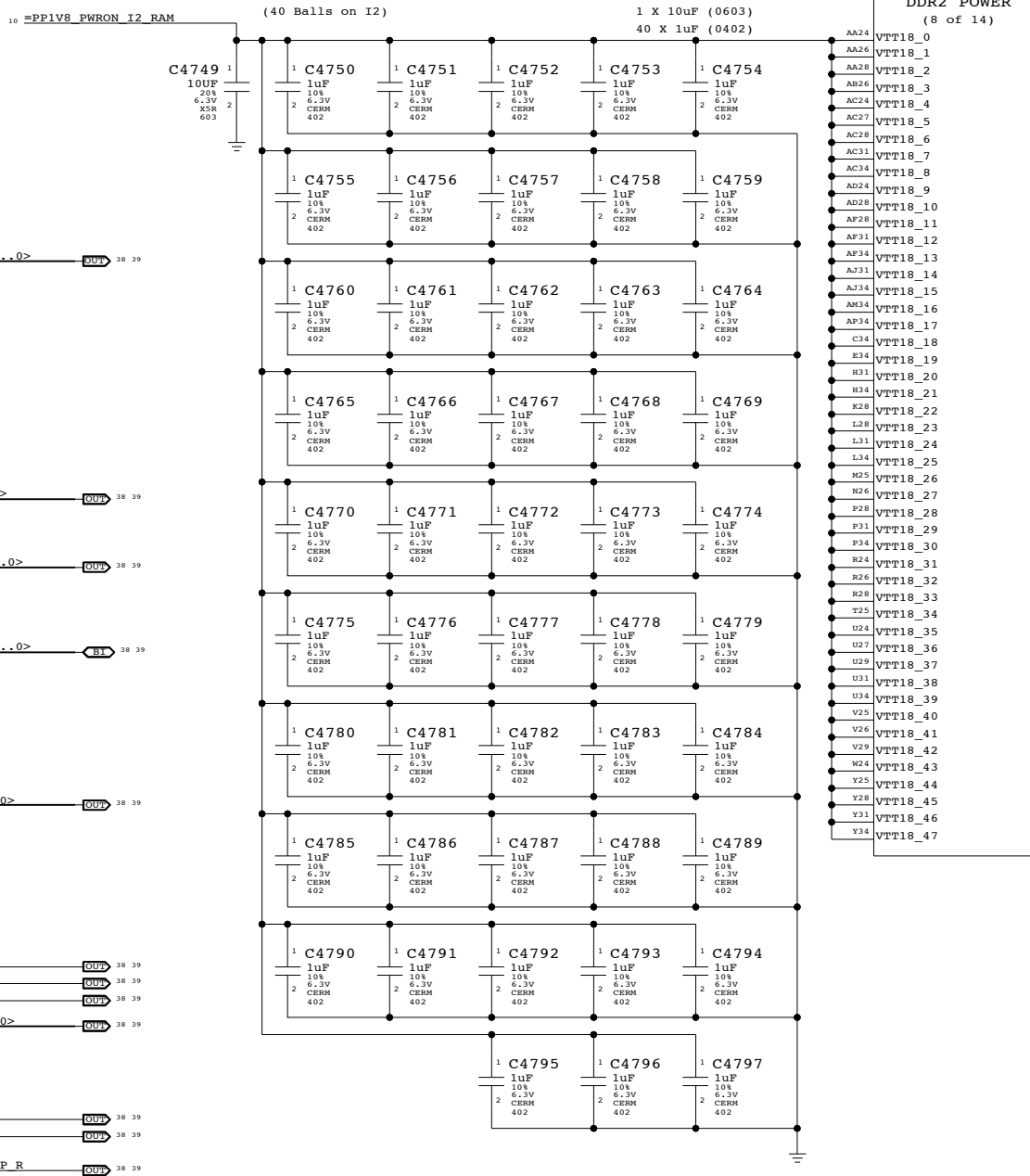
Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



OMIT
 U2100
 I2
 BGA
 MEMORY INTERFACE
 (7 of 14)

DDR2 I/O DECOUPLING
 (40 Balls on I2)



I2 Memory Interface
 SYNC_MASTER=MARIAS
 SYNC_DATE=08/24/2005

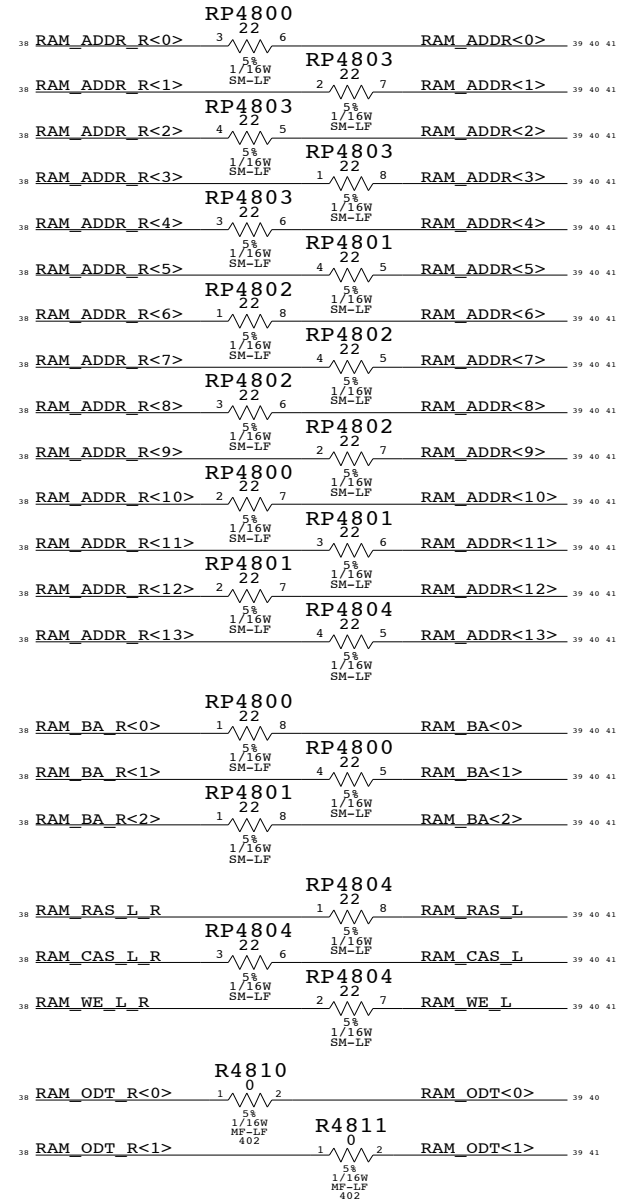
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	D	051-6839	E
SCALE	SHT	OF	
NONE	47	115	

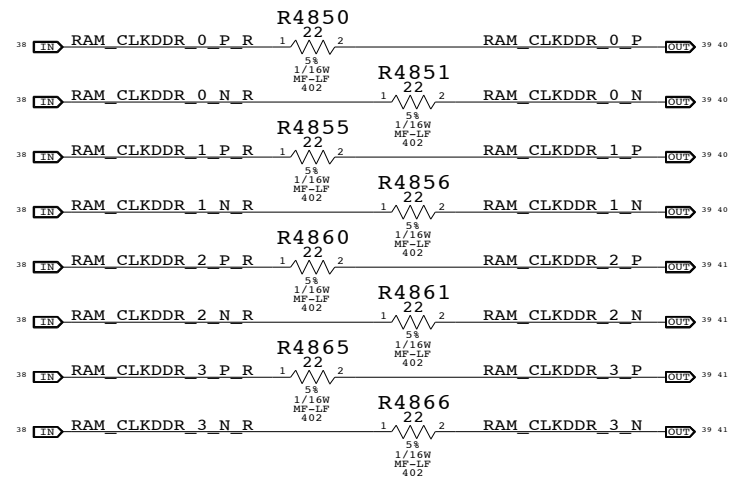
Main Memory Series Termination

SERIES RESISTORS FOR CONTROL SIGNALS

PINS ARE SWAPPABLE FOR RPAKS RP4800-RP4804

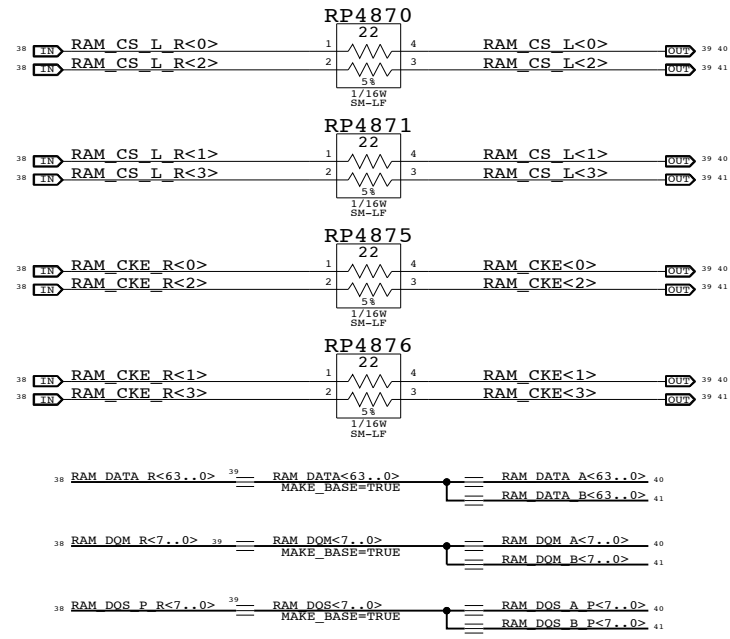


SERIES RESISTORS FOR CLOCKS



SERIES RESISTORS FOR CS / CKE

Do not swap with other RPAKS



ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
1230	RAM_DIFF	RAM_DIFF	RAM_CLK_0	RAM_CLKDDR_0_P 39 40
1230	RAM_DIFF	RAM_DIFF	RAM_CLK_0	RAM_CLKDDR_0_N 39 40
1230	RAM_DIFF	RAM_DIFF	RAM_CLK_1	RAM_CLKDDR_1_P 39 40
1230	RAM_DIFF	RAM_DIFF	RAM_CLK_1	RAM_CLKDDR_1_N 39 40
1230	RAM_DIFF	RAM_DIFF	RAM_CLK_2	RAM_CLKDDR_2_P 39 41
1230	RAM_DIFF	RAM_DIFF	RAM_CLK_2	RAM_CLKDDR_2_N 39 41
1230	RAM_DIFF	RAM_DIFF	RAM_CLK_3	RAM_CLKDDR_3_P 39 41
1230	RAM_DIFF	RAM_DIFF	RAM_CLK_3	RAM_CLKDDR_3_N 39 41
1230	RAM	RAM	RAM_CKE<3..0>	39 40 41
1230	RAM	RAM	RAM_CS_L<3..0>	39 40 41
1230	RAM	RAM	RAM_ADDR<13..0>	39 40 41
1230	RAM	RAM	RAM_BA<2..0>	39 40 41
1230	RAM	RAM	RAM_RAS_L	39 40 41
1230	RAM	RAM	RAM_CAS_L	39 40 41
1230	RAM	RAM	RAM_WE_L	39 40 41
1230	RAM	RAM	RAM_ODT<1..0>	39 40 41
1230	RAM	RAM	RAM_DOS<7..0>	39
1230	RAM	RAM	RAM_DQM<7..0>	39
1230	RAM	RAM	RAM_DATA<63..0>	39

ECSETS provided by memory controller.

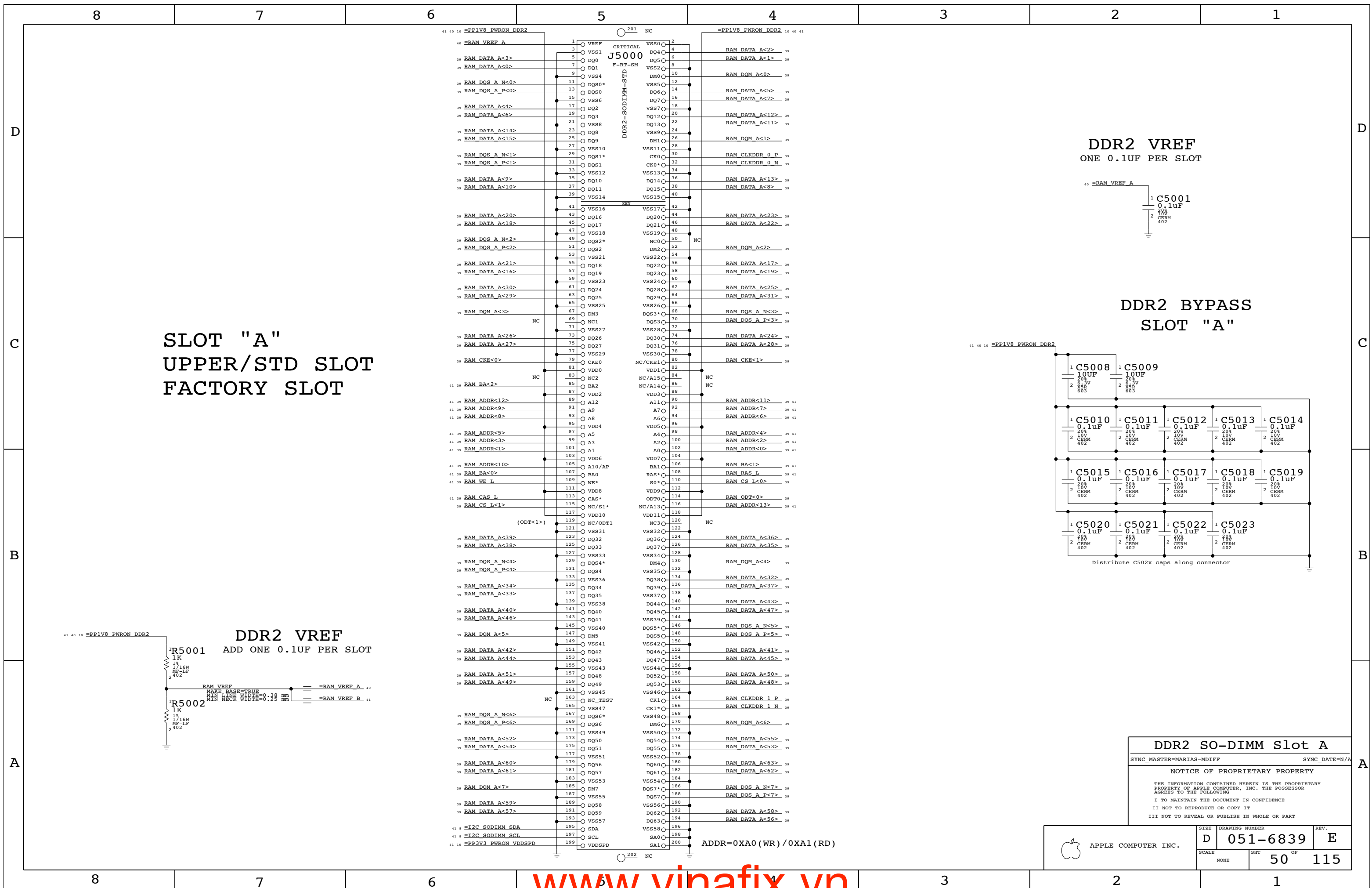
Memory Series Termination

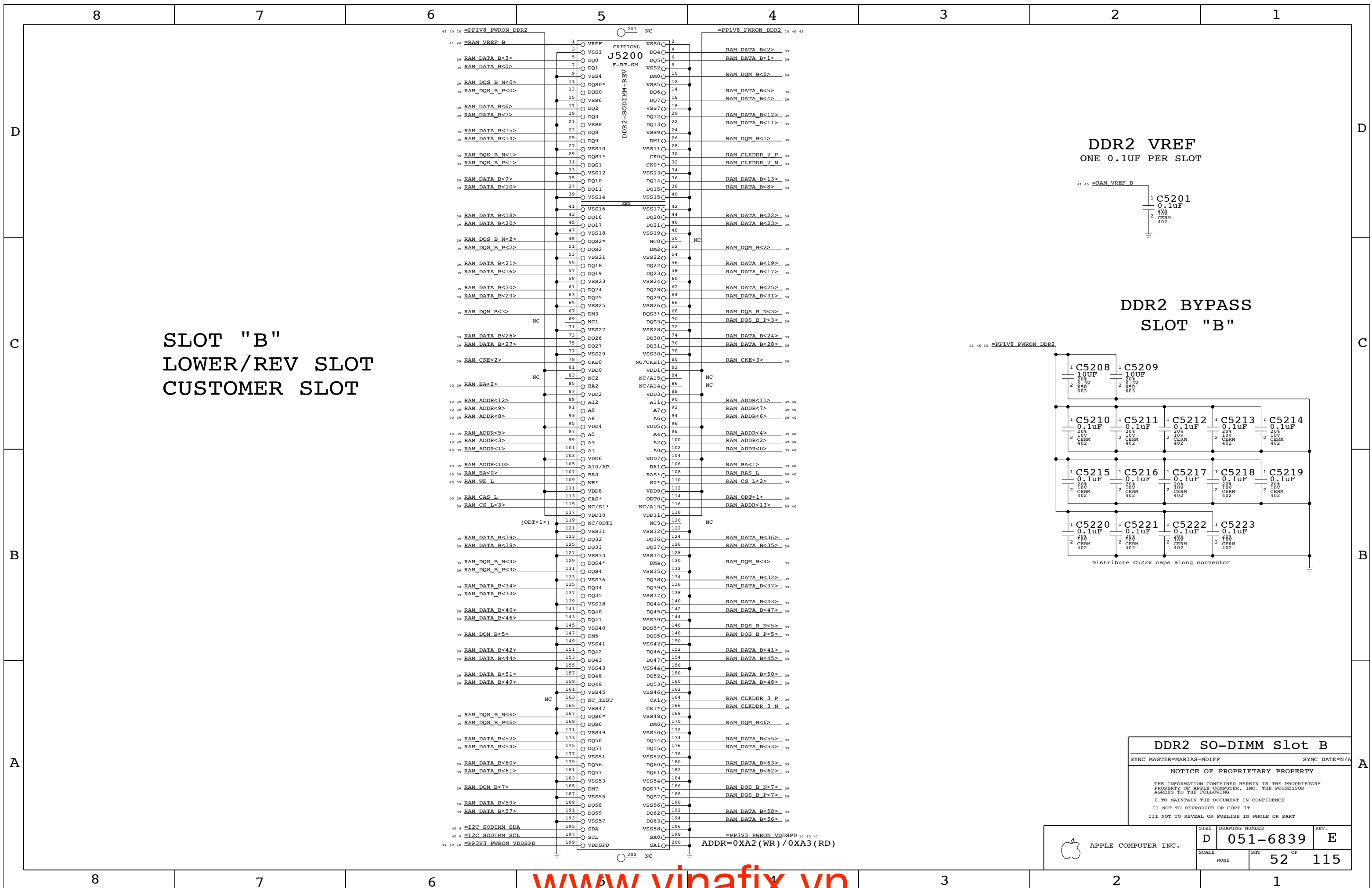
SYNC_MASTER=MARIAS-NDIFF SYNC_DATE=N/A

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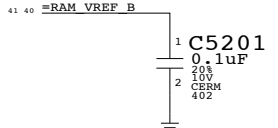
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6839	E
SCALE	NONE	SHT	OF
		48	115



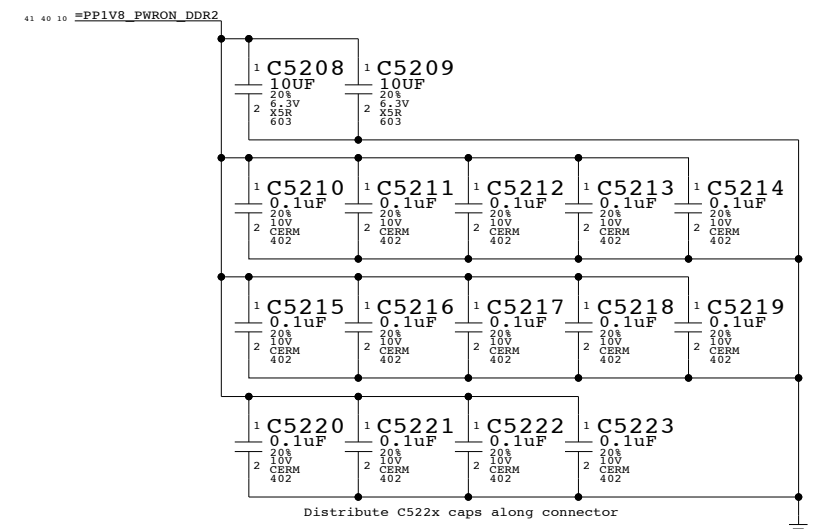


SLOT "B"
LOWER/REV SLOT
CUSTOMER SLOT

DDR2 VREF
ONE 0.1UF PER SLOT



DDR2 BYPASS
SLOT "B"



DDR2 SO-DIMM Slot B
 SYNC_MASTER=MARIAS-MDIFF SYNC_DATE=N/A
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	D	051-6839	E
SCALE	NONE	SHT	OF
		52	115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
AGP_CLK	CLOCK	CLOCK		AGP_CLK66M_GPU_R 11 43
I2_AGP_FBCLK	I2_FBCLK	I2_FBCLK		I2_AGP_FBCLK_OUT_R 43
I2_AGP_FBCLK	I2_FBCLK	I2_FBCLK		I2_AGP_FBCLK_OUT 21 43
AGP_AD_0	AGP	AGP		AGP_AD<15..0> 43 44
AGP_AD_1	AGP	AGP		AGP_AD<31..16> 43 44
AGP_AD_0	AGP	AGP		AGP_CBE_L<1..0> 43 44
AGP_AD_1	AGP	AGP		AGP_CBE_L<3..2> 43 44
AGP_AD_STB_0	AGP_STB	AGP_STB	AGP_AD_STB0	AGP_AD_STB0_P 43 44
AGP_AD_STB_0	AGP_STB	AGP_STB	AGP_AD_STB0	AGP_AD_STB0_N 43 44
AGP_AD_STB_1	AGP_STB	AGP_STB	AGP_AD_STB1	AGP_AD_STB1_P 43 44
AGP_AD_STB_1	AGP_STB	AGP_STB	AGP_AD_STB1	AGP_AD_STB1_N 43 44
AGP_SBA	AGP	AGP		AGP_SBA<7..0> 43 44
AGP_SB_STB	AGP_STB	AGP_STB	AGP_SB_STB	AGP_SB_STB_P 43 44
AGP_SB_STB	AGP_STB	AGP_STB	AGP_SB_STB	AGP_SB_STB_N 43 44
AGP_ST	AGP	AGP		AGP_ST<3..0> 43 44
AGP_CTL	AGP	AGP		AGP_FRAME_L 6 43 44
AGP_CTL	AGP	AGP		AGP_DEVSEL_L 6 43 44
AGP_CTL	AGP	AGP		AGP_TRDY_L 6 43 44
AGP_CTL	AGP	AGP		AGP_STOP_L 6 43 44
AGP_CTL	AGP	AGP		AGP_DEVSEL_L 6 43 44
AGP_CTL	AGP	AGP		AGP_PAR 43 44
AGP_CTL	AGP	AGP		AGP_PIPE_L 43
AGP_CTL	AGP	AGP		AGP_WBF_L 43 44
AGP_CTL	AGP	AGP		AGP_RBF_L 43 44
AGP_CTL	AGP	AGP		AGP_REQ_L 6 43 44
AGP_CTL	AGP	AGP		AGP_GNT_L 6 43 44

Page Notes

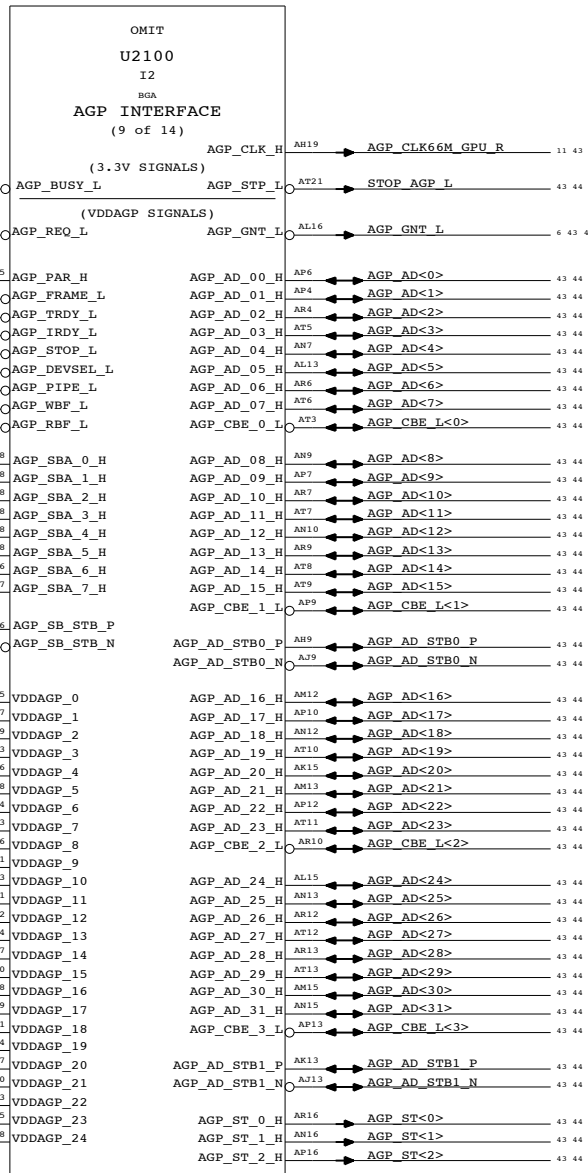
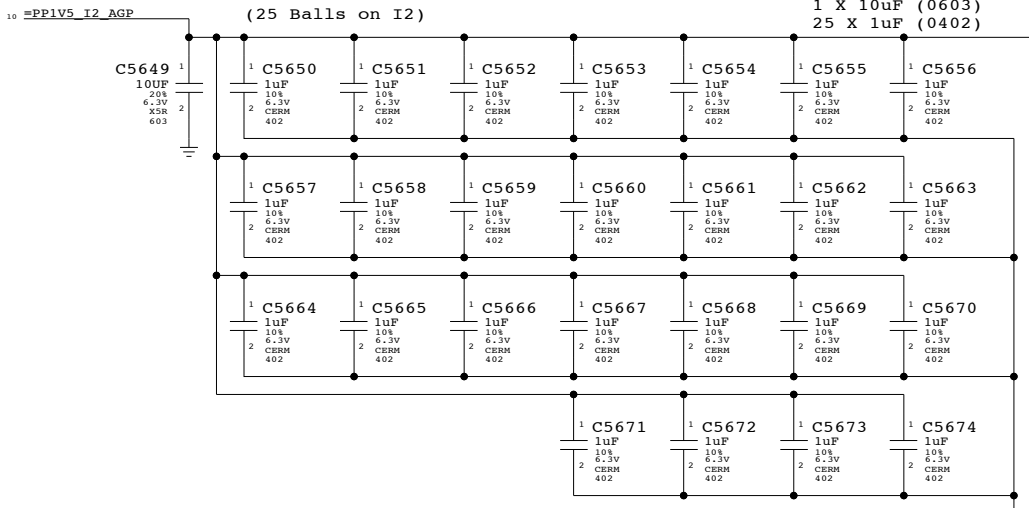
Power aliases required by this page:
 - =PP3V3_AGP
 - =PP1V5_AGP
 - =PP1V5_I2_AGP

Signal aliases required by this page:
 - =I2_AGP_VREF - VRef from graphics card or on-board graphics controller
 - =I2_AGP_FBCLK_IN - AGP feedback clock input. Length should match that of clock from I2 to AGP device.

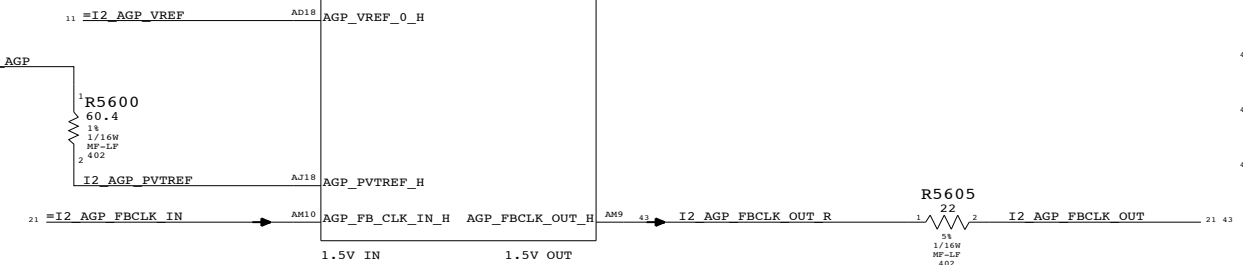
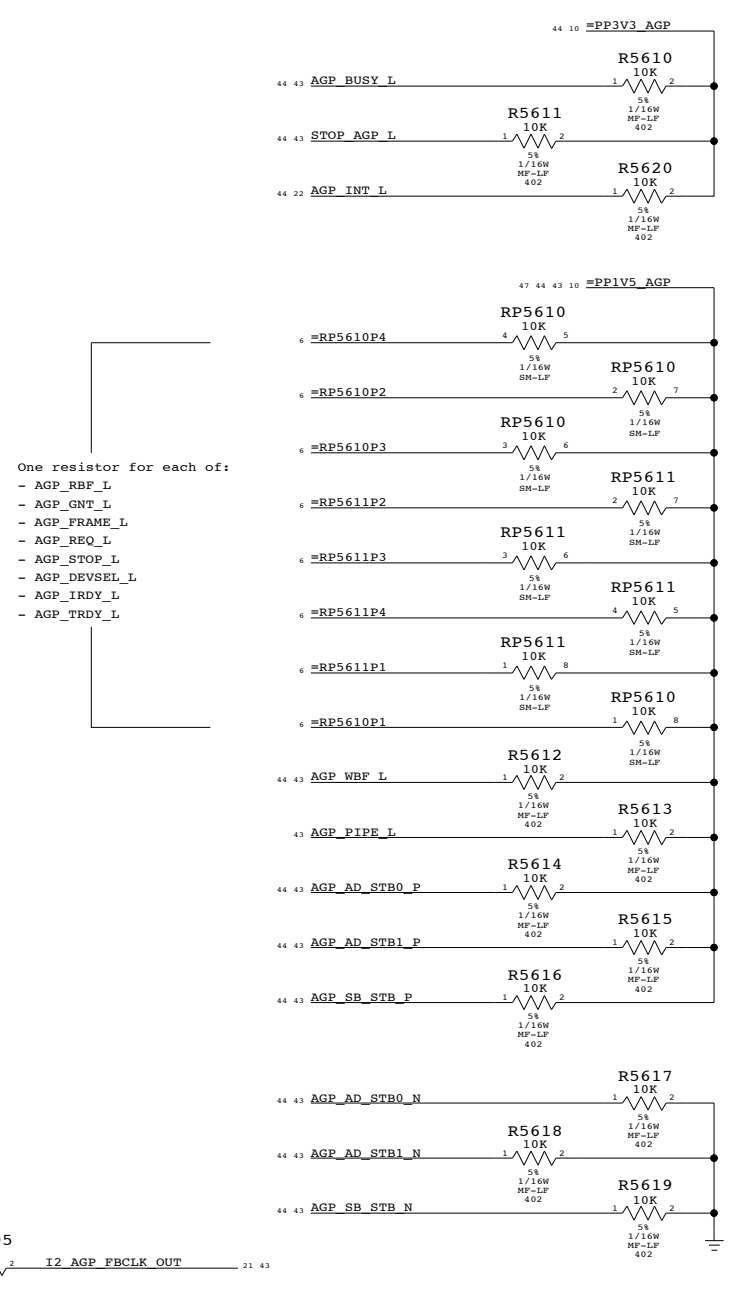
BOM options provided by this page:
 (NONE)

NOTE: I2 implements an AGP 4x bridge. AGP 8x signals are not provided by this page.

AGP I/O DECOUPLING



AGP PULL-UPS/PULL DOWNS



I2 AGP Interface

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SCALE	NONE	SHT	56	OF	115	REV.	D	051-6839	E
							DRAWING NUMBER		



APPLE COMPUTER INC.

NET TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
7700	CLOCK	CLOCK	

AGP_CLK66M_GPU 11 44

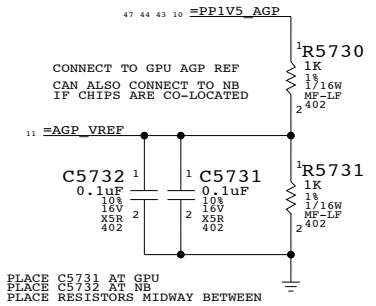
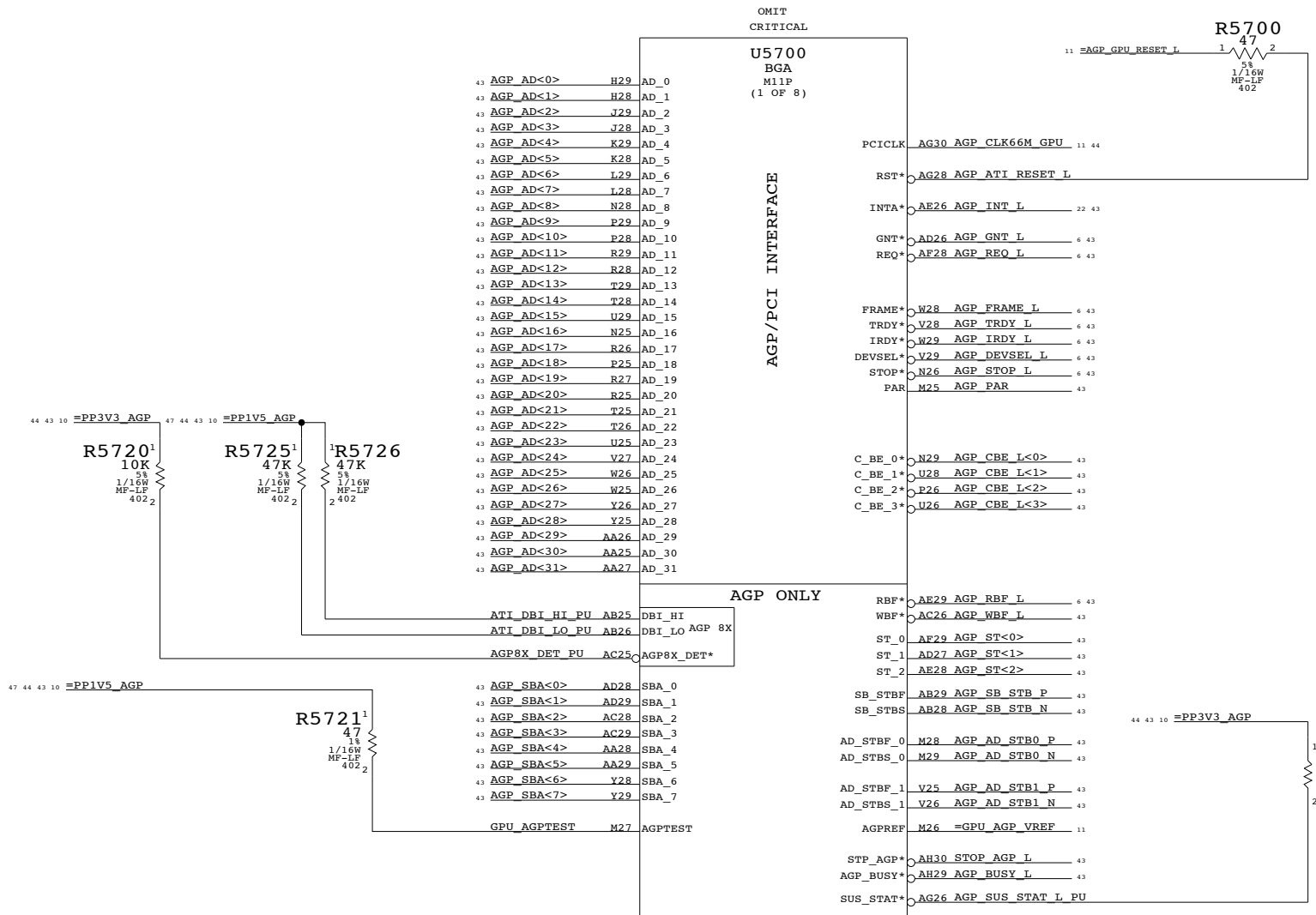
Page Notes

Power aliases required by this page:
 - =PP3V3_AGP
 - =PP1V5_AGP

Signal aliases required by this page:
 - =AGP_VREF - Vref divider output for both GPU and NB
 - =AGP_GPU_RESET_L - Active low reset for GPU

BOM options provided by this page:
 (NONE)

NOTE: AGP 8x signals are not provided by this page.



GPU (M11) AGP Interface

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	D	051-6839	E
SCALE	NONE	SHT	OF
		57	115

Page Notes

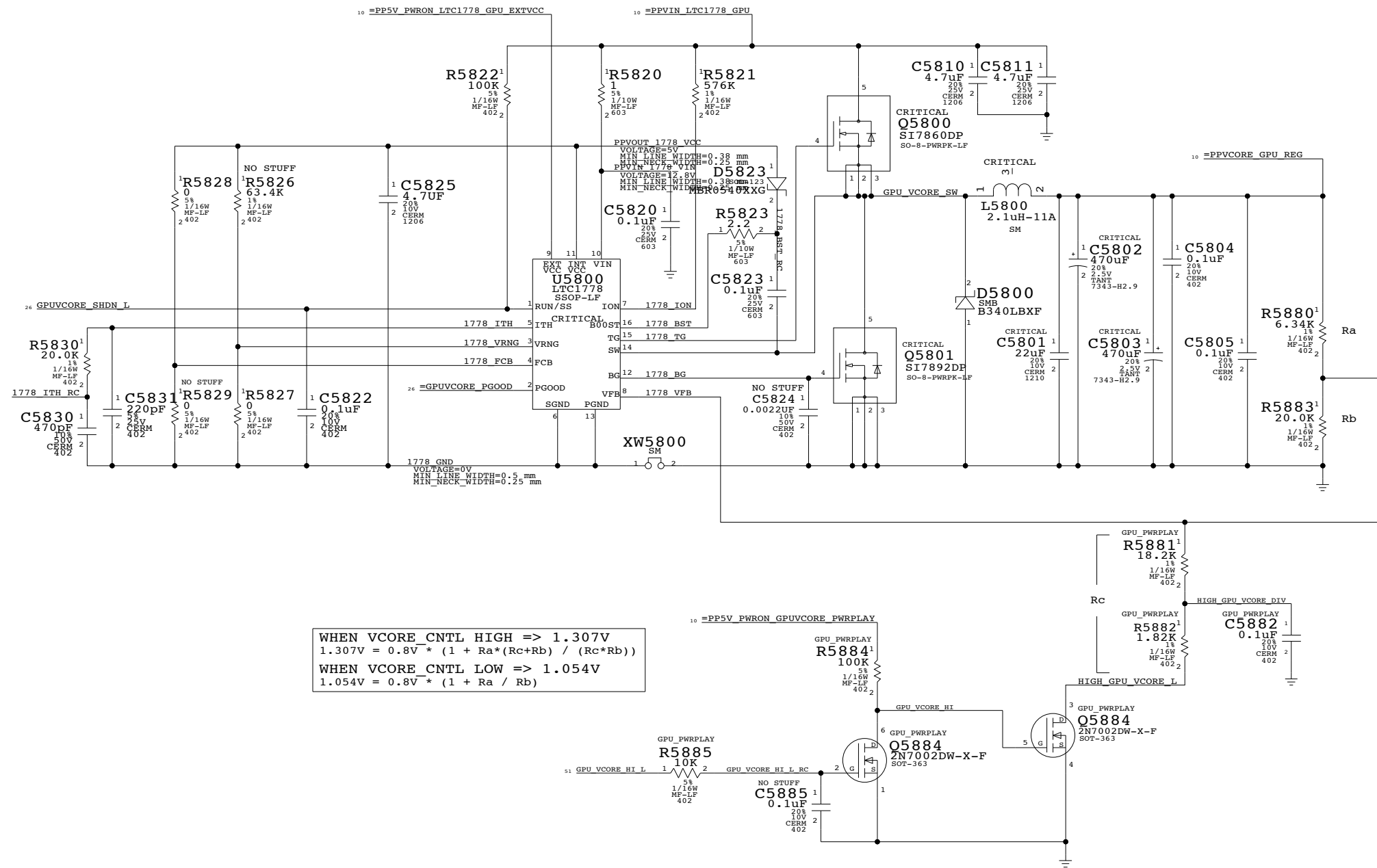
Power aliases required by this page:
 - =PPVIN_LTC1778_GPU
 - =PP5V_PWRON_LTC1778_GPU_EXTVCC
 - =PPVCORE_GPU_REG

Signal aliases required by this page:
 - =GPUVCORE_PGOOD - Active high Power Good signal for power sequencing

BOM options provided by this page:
 - GPU_PWRPLAY

NOTE: Implements "Power Miser" feature for ATI GPUs

GPU VCore SUPPLY



WHEN VCORE_CNTL HIGH => 1.307V
 $1.307V = 0.8V * (1 + Ra*(Rc+Rb) / (Rc*Rb))$
 WHEN VCORE_CNTL LOW => 1.054V
 $1.054V = 0.8V * (1 + Ra / Rb)$

GPU VCore Supply
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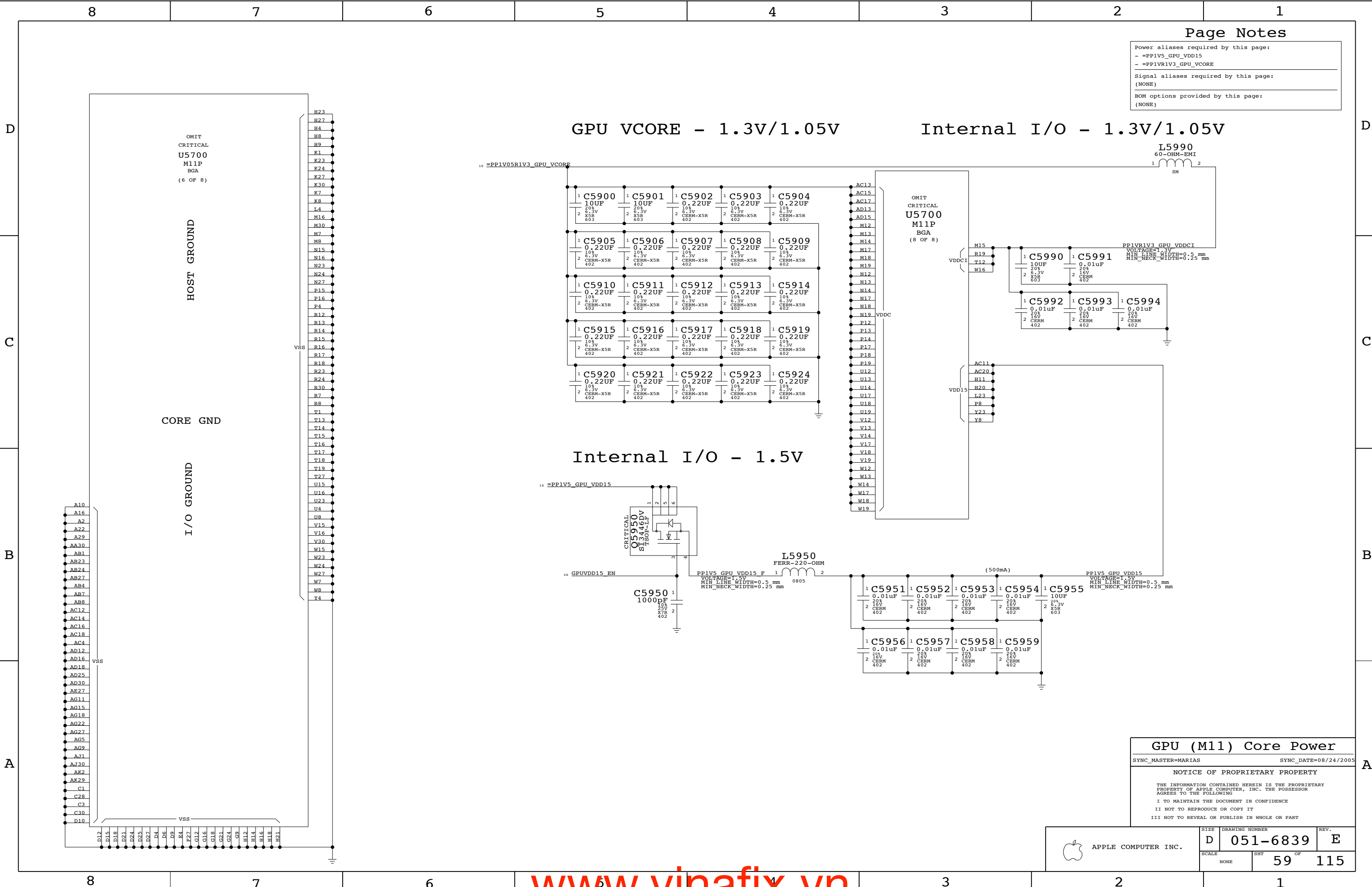
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	D	051-6839	E
SCALE	NONE	SHT OF	58 OF 115

Power aliases required by this page:
 - =PP1V5_GPU_VDD15
 - =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



GPU (M11) Core Power

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6839	E
SCALE	NONE	SHT	OF
		59	115

Page Notes

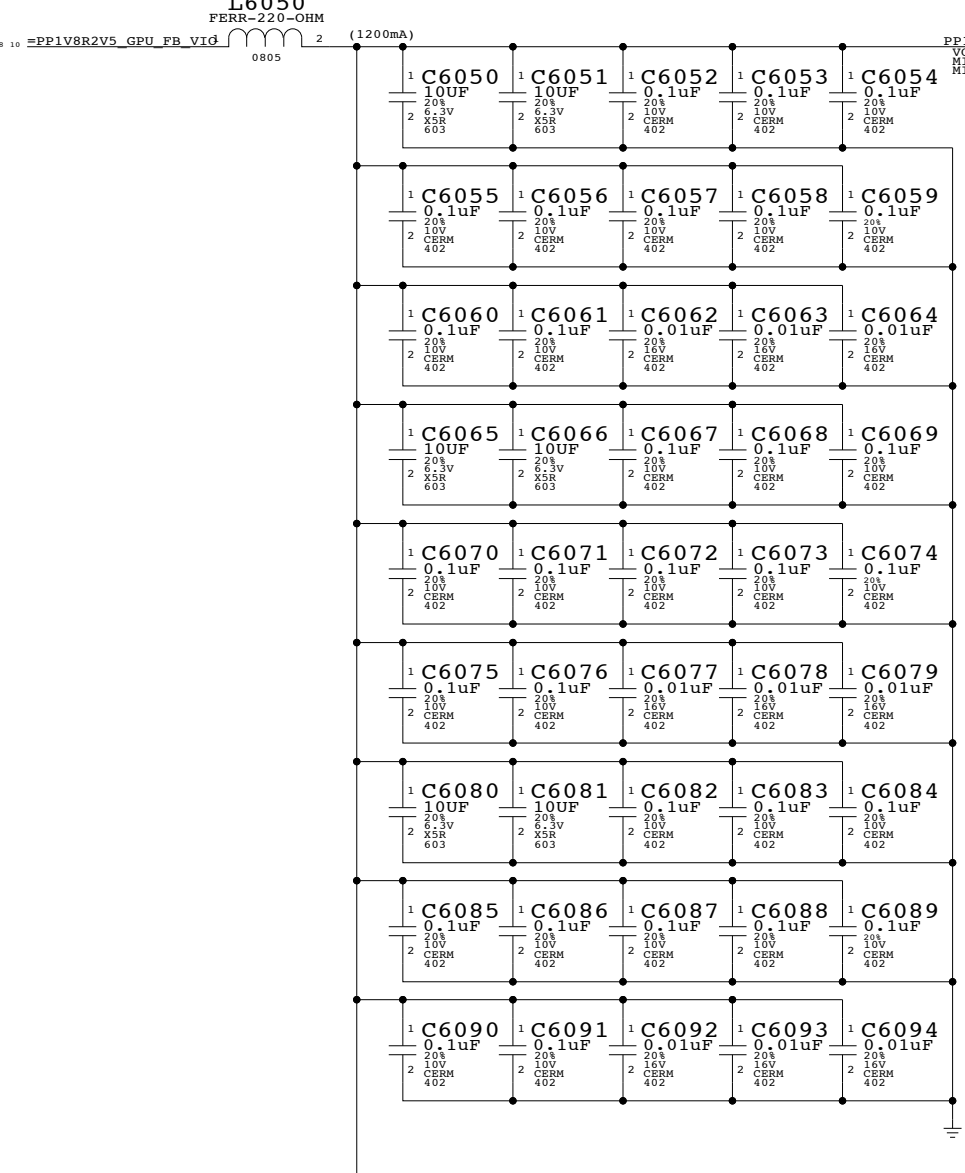
Power aliases required by this page:
 - =PP1V8R2V5_GPU_FB_VIO - =PP1V8_GPU_PANEL_IO
 - =PP3V3_GPU_VDDR3 - =PP1V8_GPU_LVDS_PLL
 - =PP1V5_GPU_DVO - =PP2V5_GPU_LVDS_IO
 - =PP1V8_GPU_DVO - =PP2V5_GPU_LVDS_IO
 - =PP1V5R3V3_DVO_VREF - =PP1V5_AGP

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - DVO_1V5 - GPU_LVDDR_2V5
 - DVO_1V8 - GPU_LVDDR_2V8

NOTE: Implements a low-swing DVO bus only

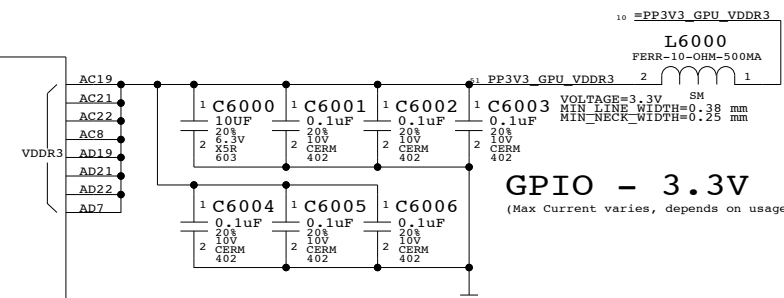
MEMORY I/O - 1.8V/2.5V



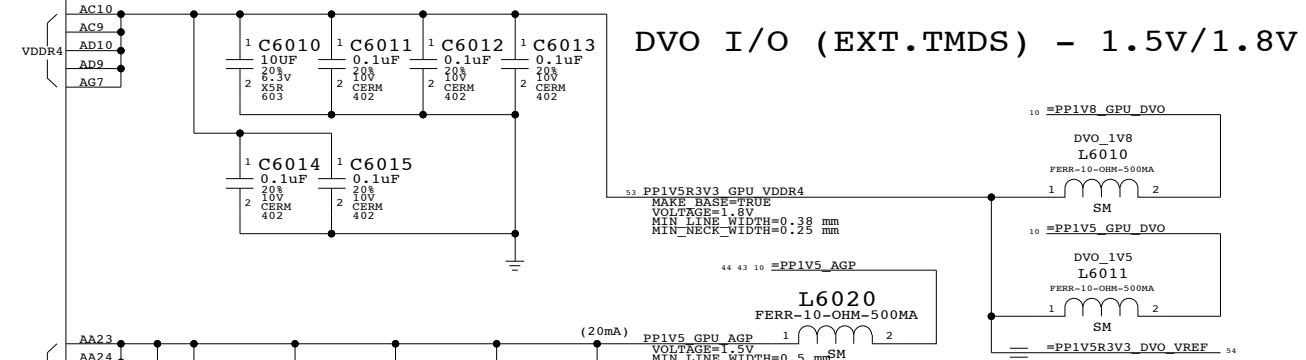
OMIT
 CRITICAL
U5700
 M11P
 BGA
 (7 OF 8)

- A15
- A21
- A28
- A3
- A9
- AA1
- AA4
- AA7
- AA8
- AD4
- B1
- B30
- D11
- D13
- D14
- D17
- D19
- D20
- D23
- D26
- D5
- D8
- E27
- F4
- G10
- G13
- G15
- G19
- G22
- G27
- H7
- H10
- H13
- H15
- H17
- H19
- H22
- J1
- J23
- J24
- J4
- J7
- J8
- L27
- L8
- M4
- N4
- N7
- N8
- R1
- R4
- T4
- T7
- T8
- V4
- V7
- V8

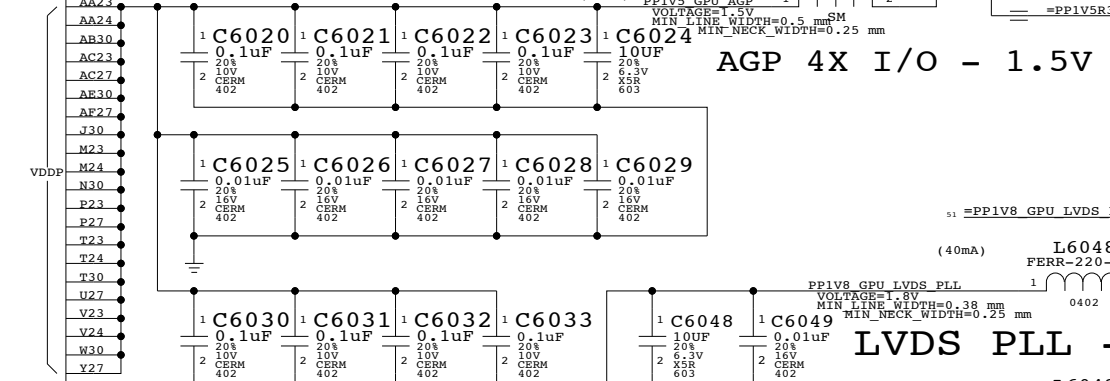
GPIO - 3.3V
 (Max Current varies, depends on usage)



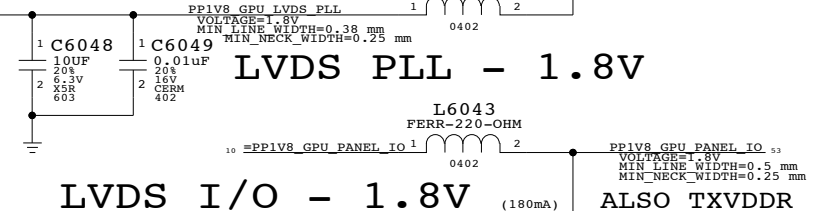
DVO I/O (EXT.TMDS) - 1.5V/1.8V



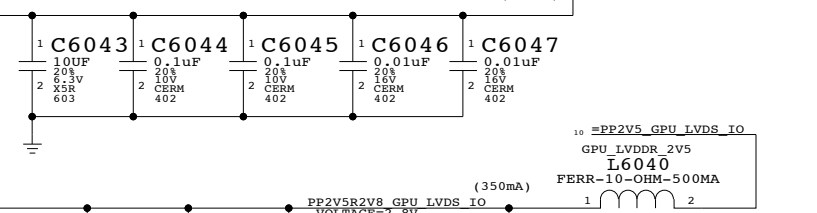
AGP 4X I/O - 1.5V



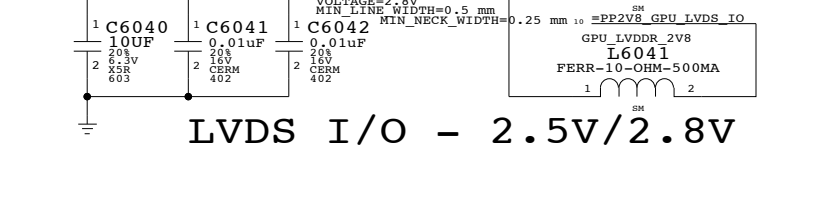
LVDS PLL - 1.8V



LVDS I/O - 1.8V
 (180mA) ALSO TXVDDR



LVDS I/O - 2.5V/2.8V



GPU (M11) I/O Power

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SCALE	SHT	OF	
NONE	60	115	

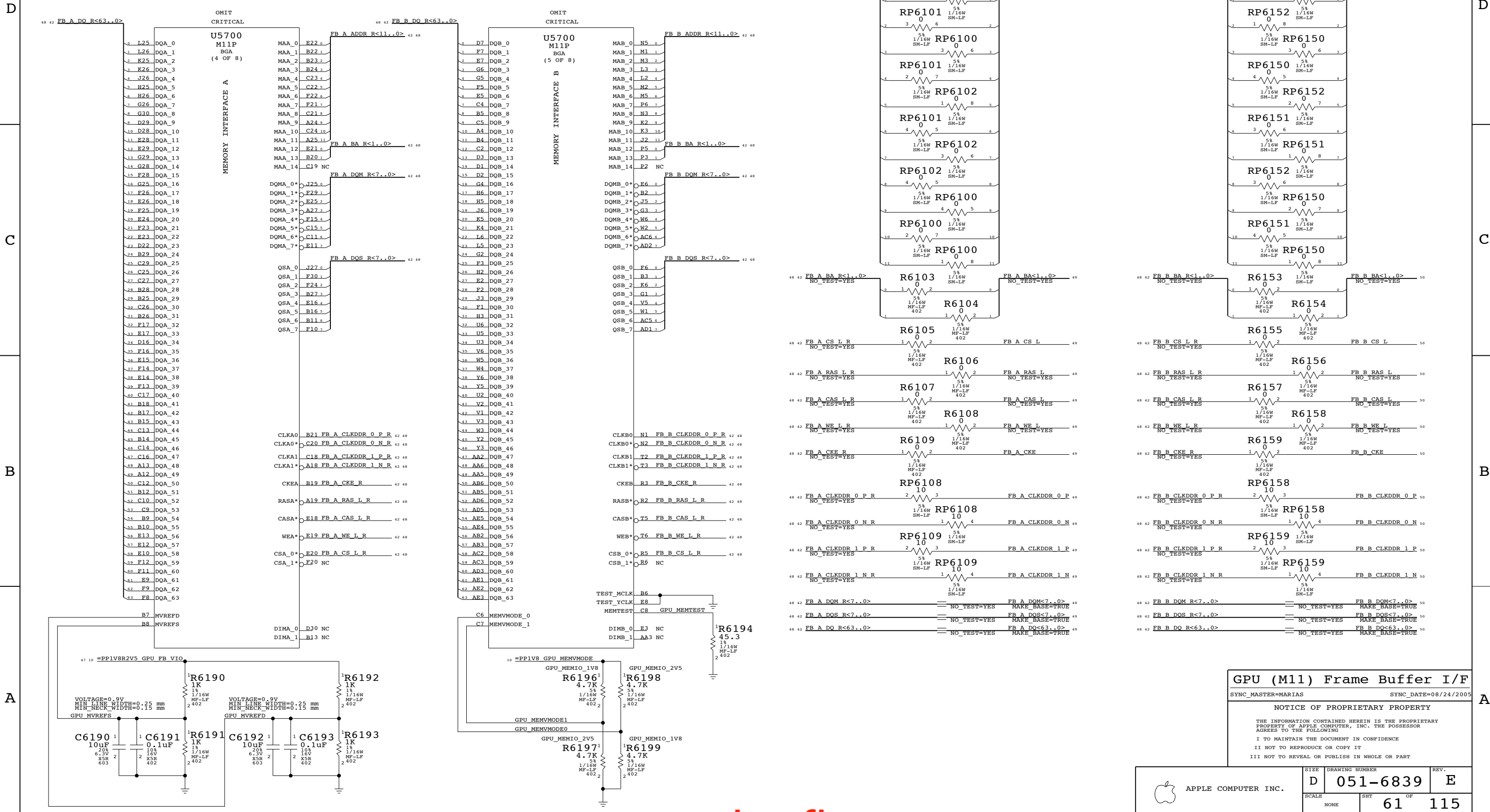
Page Notes

Power aliases required by this page:
 - =PP1V8R2V5_GPU_FB_VIO
 - =PP1V8_GPU_MEMVMODE

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - GPU_MEMIO_1V8
 - GPU_MEMIO_2V5

GPU Frame Buffer Series Term



GPU (M11) Frame Buffer I/F

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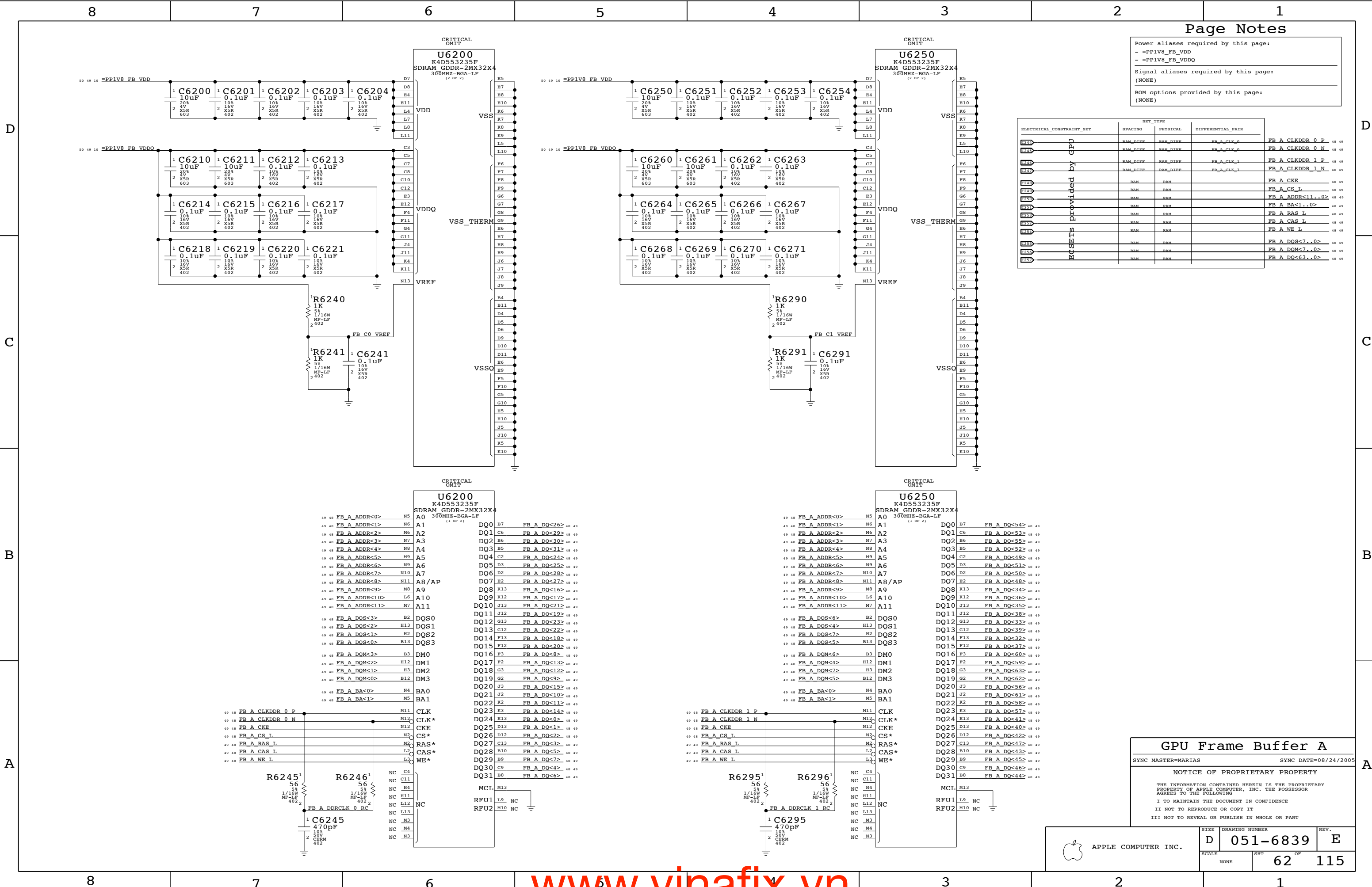
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6839	E
SCALE	NONE	SHT	OF
		61	115

Power aliases required by this page:
 - =PPIV8_FB_VDD
 - =PPIV8_FB_VDDQ

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
FB_A0	RAM_DIFF	RAM_DIFF	FB_A_CLK_0
FB_A1	RAM_DIFF	RAM_DIFF	FB_A_CLK_0
FB_A2	RAM_DIFF	RAM_DIFF	FB_A_CLK_1
FB_A3	RAM_DIFF	RAM_DIFF	FB_A_CLK_1
FB_A4	RAM	RAM	FB_A_CKE
FB_A5	RAM	RAM	FB_A_CS_L
FB_A6	RAM	RAM	FB_A_ADDR<11..0>
FB_A7	RAM	RAM	FB_A_BA<1..0>
FB_A8	RAM	RAM	FB_A_RAS_L
FB_A9	RAM	RAM	FB_A_CAS_L
FB_A10	RAM	RAM	FB_A_WE_L
FB_A11	RAM	RAM	FB_A_DQS<7..0>
FB_A12	RAM	RAM	FB_A_DQM<7..0>
FB_A13	RAM	RAM	FB_A_DQ<63..0>



GPU Frame Buffer A

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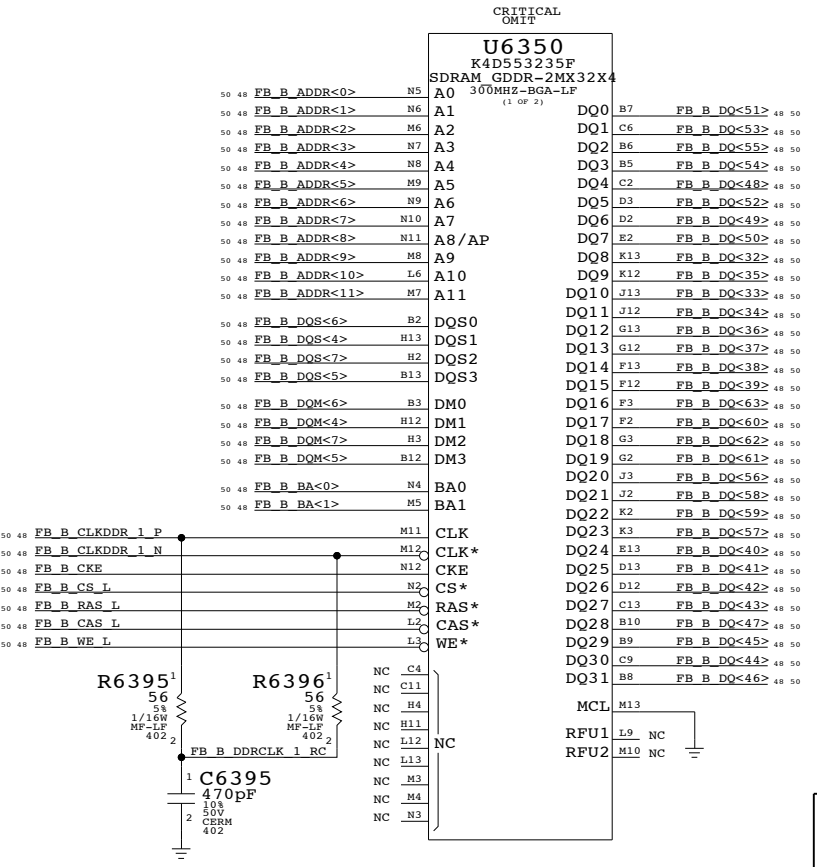
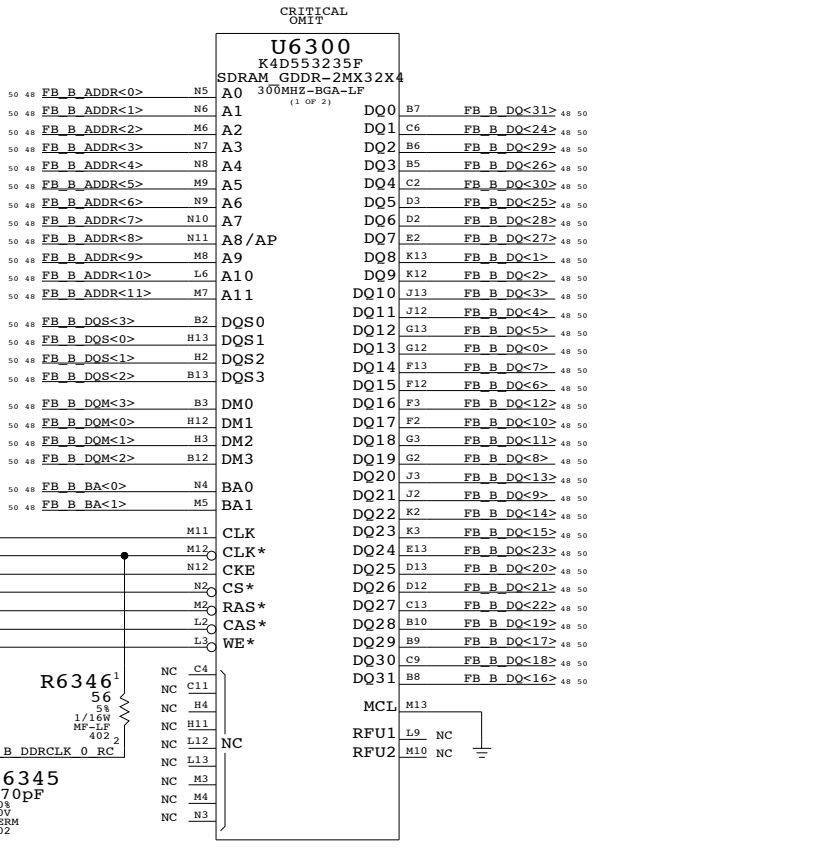
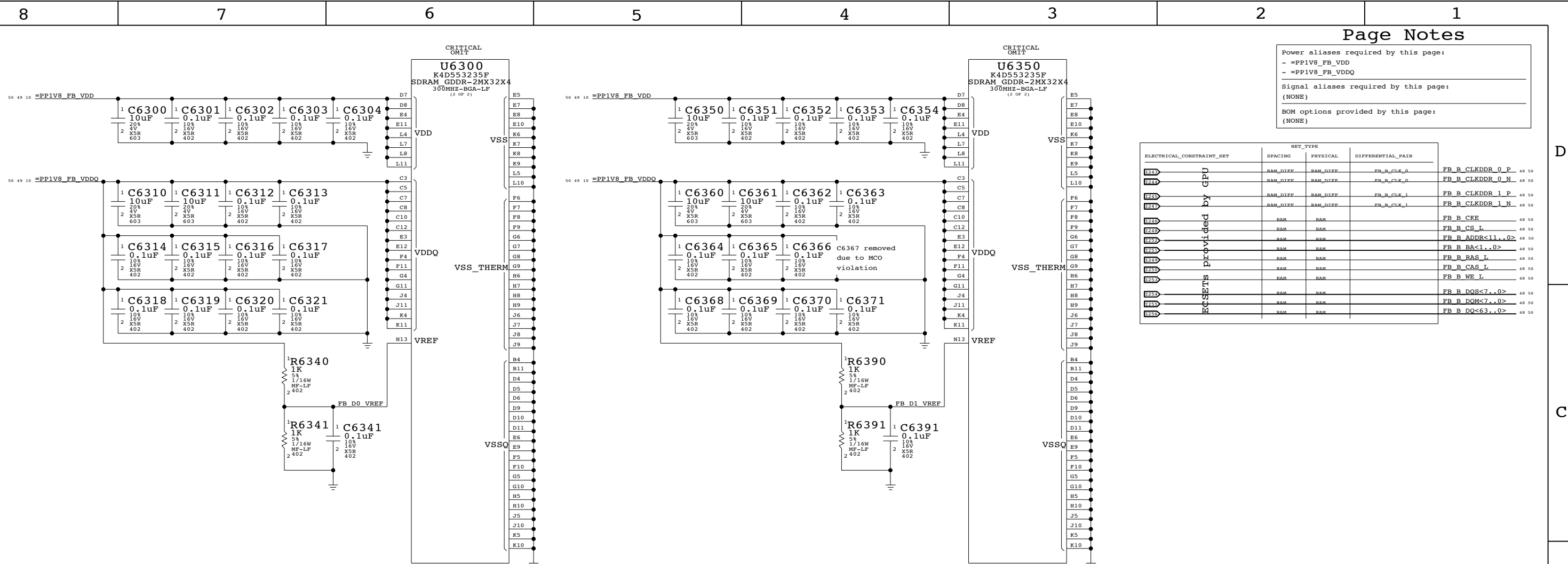
SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE	SHT	OF
NONE	62	115

Power aliases required by this page:
 - =PPIV8_FB_VDD
 - =PPIV8_FB_VDDQ

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
FB00	RAM_DIFF	RAM_DIFF	FB_B_CLK_0
FB00	RAM_DIFF	RAM_DIFF	FB_B_CLK_0_N
FB00	RAM_DIFF	RAM_DIFF	FB_B_CLK_1
FB00	RAM_DIFF	RAM_DIFF	FB_B_CLK_1_N
FB00	RAM	RAM	FB_B_CKE
FB00	RAM	RAM	FB_B_CS_L
FB00	RAM	RAM	FB_B_ADDR<11..0>
FB00	RAM	RAM	FB_B_BA<1..0>
FB00	RAM	RAM	FB_B_RAS_L
FB00	RAM	RAM	FB_B_CAS_L
FB00	RAM	RAM	FB_B_WE_L
FB00	RAM	RAM	FB_B_DQS<7..0>
FB00	RAM	RAM	FB_B_DQM<7..0>
FB00	RAM	RAM	FB_B_DQ<63..0>



GPU Frame Buffer B

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	D	051-6839	E
SCALE	NONE	SHT	OF
		63	115

Page Notes

Power aliases required by this page:
 - =PP3V3_GPU_GPIOS
 - =PP2V5_PVDD
 - =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
 - =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
 - =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
 (NONE)

D

D

C

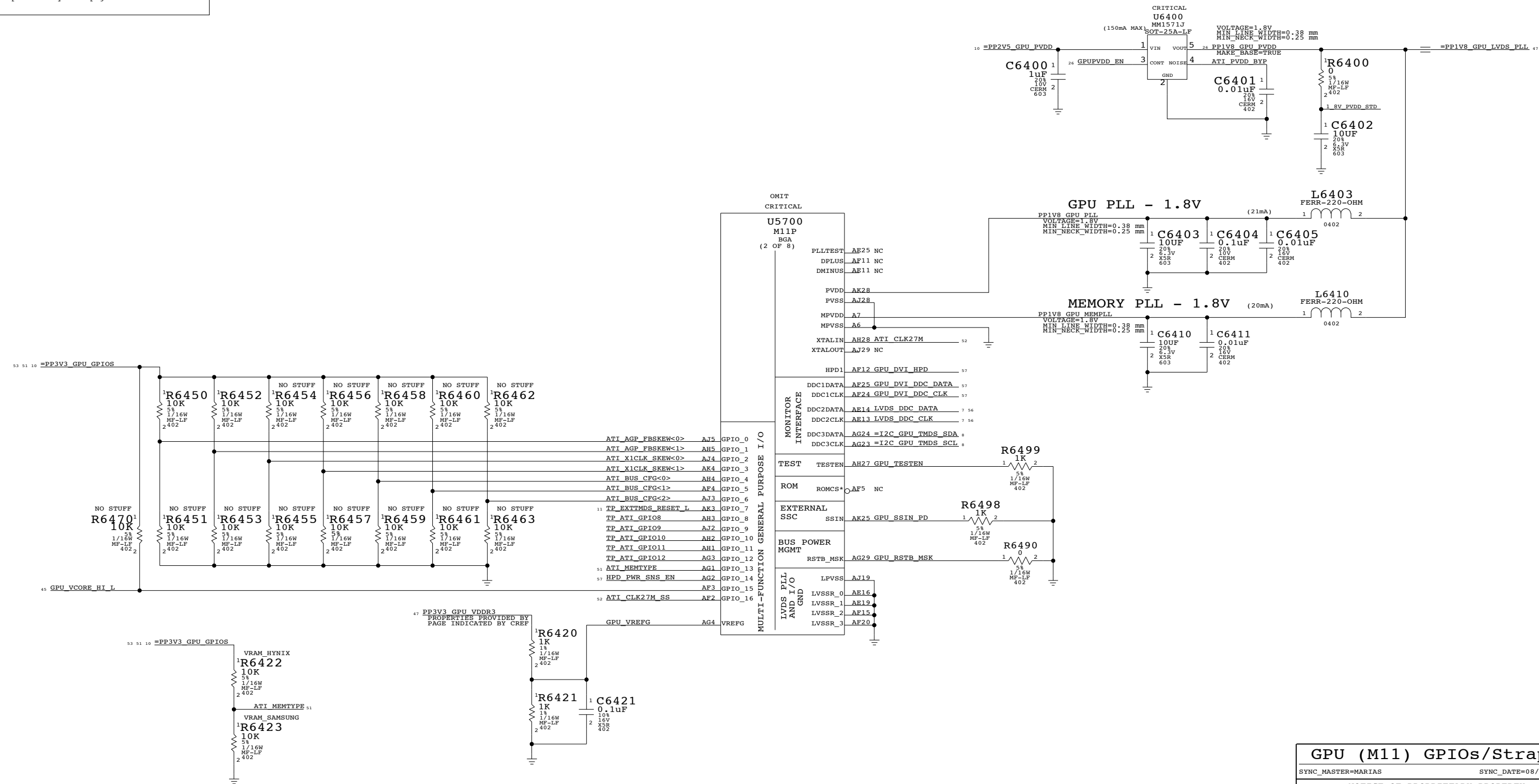
C

B

B

A

A



GPU (M11) GPIOs/Straps

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SCALE	SHT	OF	
NONE	64	115	

Page Notes

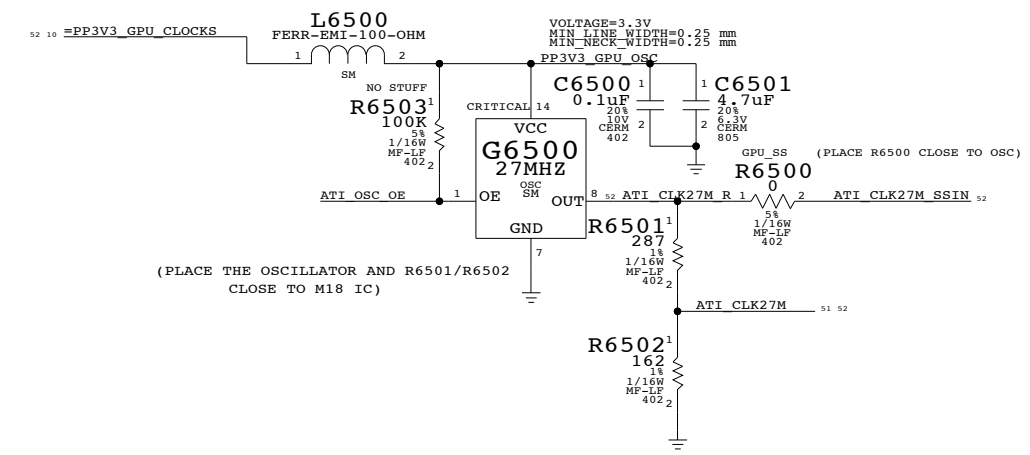
Power aliases required by this page:
 - =PP3V3_GPU_CLOCKS - =PP3V3_GPU_PWRSEQ
 - =PPVIN_GPU_LVDDR_LDO - =PP2V5_GPU_PWRSEQ
 - =PP2V5_GPU_LVDDR_LDO - =PP1V8_GPU_PWRSEQ
 - =PP1V5_GPU_PWRSEQ

Signal aliases required by this page:
 (NONE)

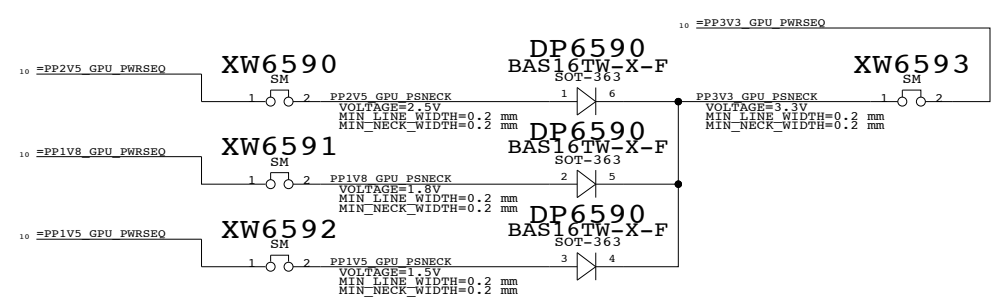
BOM options provided by this page:
 - GPU_SS - GPU_LVDDR_2V8

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
E50	ATI_CLK27M	CLOCK	CLOCK	
E54	ATI_CLK27M	CLOCK	CLOCK	
E55	ATI_CLK27M	CLOCK	CLOCK	
E51	ATI_CLK27M_SS	CLOCK	CLOCK	
E52	ATI_CLK27M_SS	CLOCK	CLOCK	

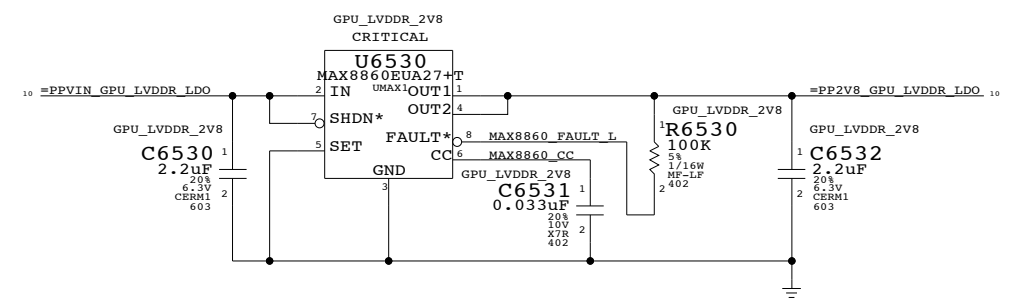
27M OSC



M11 Power Shutdown Sequencing

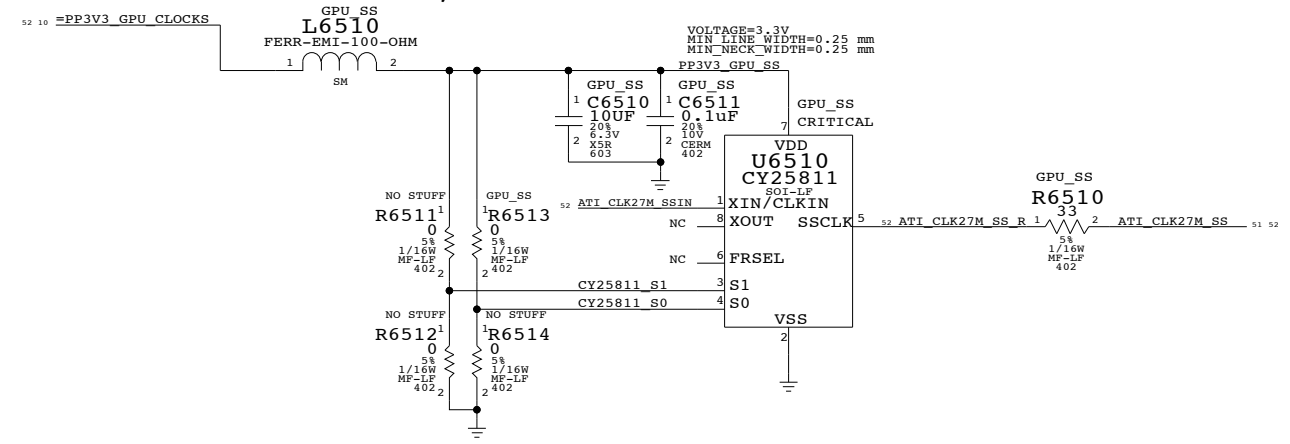


LVDDR 2.8V LDO



PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
35381188	35381140	GPU_LVDDR_2V8	U6530	Primary is 2.77V/A11 to 2.82V

SPREAD SPECTRUM SUPPORT
 S0=1;S1=M => -1.5% DOWN-SPREAD



GPU (M11) Clocks/Misc

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SCALE	NONE	SHT OF	65 OF 115

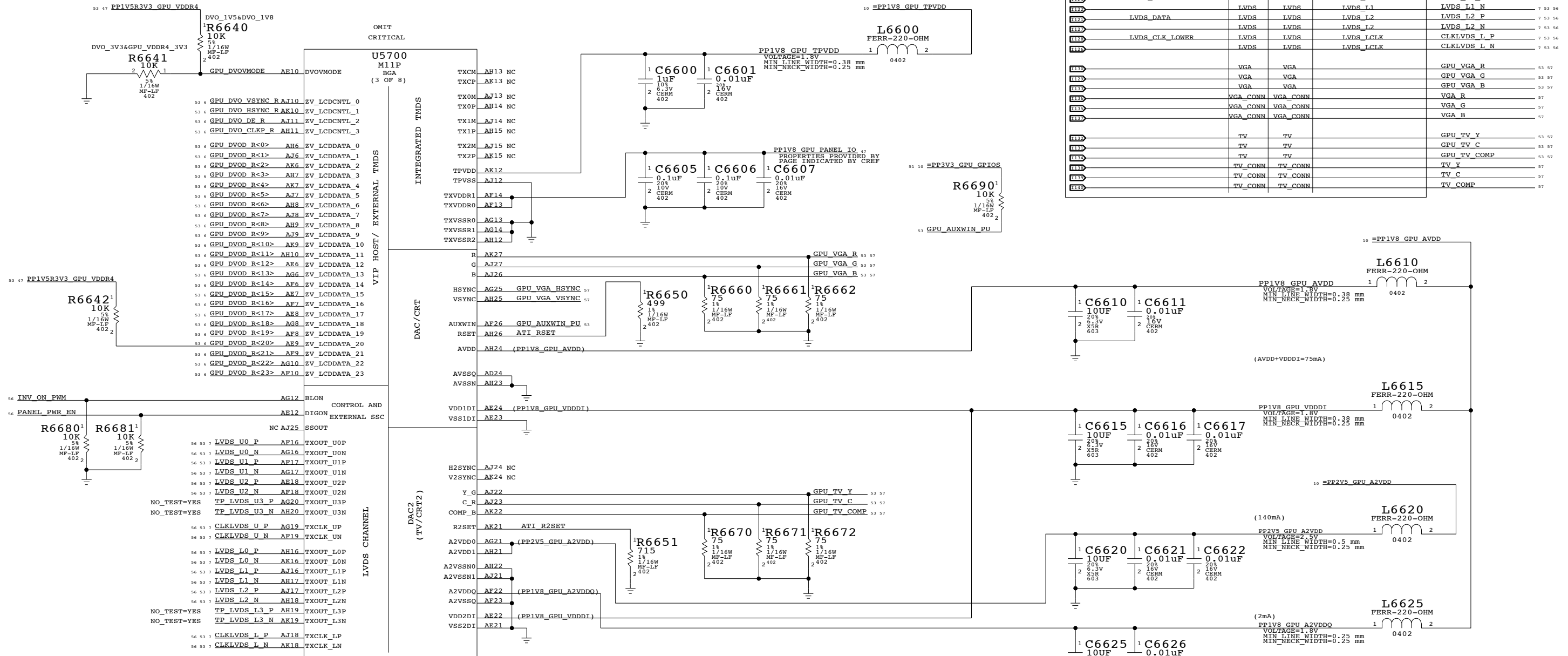
Page Notes

Power aliases required by this page:
 - =PP2V5_GPU_A2VDD - =PP1V8_GPU_AVDD
 - =PP1V8_GPU_TPVD - =PP3V3_GPU_GPIOS

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - DVO_1V5 - GPU_VDDR4_3V3
 - DVO_1V8 - DVO_3V3

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		DIFFERENTIAL_PAIR	
	SPACING	PHYSICAL		
R660	DVO	DVO	GPU DVOD R<23..0>	6 53
R660	DVO	DVO	GPU DVO_HSYNC_R	6 53
R660	DVO	DVO	GPU DVO_VSYNC_R	6 53
R660	DVO	DVO	GPU DVO_DE_R	6 53
R660	DVO	DVO	GPU DVO_CLKP_R	6 53
R660	LVDS_DATA	LVDS	LVDS_U0	7 53 56
R660	LVDS_DATA	LVDS	LVDS_U0_P	7 53 56
R660	LVDS_DATA	LVDS	LVDS_U0_N	7 53 56
R660	LVDS_DATA	LVDS	LVDS_U1_P	7 53 56
R660	LVDS_DATA	LVDS	LVDS_U1_N	7 53 56
R660	LVDS_DATA	LVDS	LVDS_U2_P	7 53 56
R660	LVDS_DATA	LVDS	LVDS_U2_N	7 53 56
R660	LVDS_CLK_UPPER	LVDS	LVDS_UCLK	7 53 56
R660	LVDS_CLK_UPPER	LVDS	CLKLVDS_U_P	7 53 56
R660	LVDS_CLK_UPPER	LVDS	CLKLVDS_U_N	7 53 56
R660	LVDS_DATA	LVDS	LVDS_L0	7 53 56
R660	LVDS_DATA	LVDS	LVDS_L0_P	7 53 56
R660	LVDS_DATA	LVDS	LVDS_L0_N	7 53 56
R660	LVDS_DATA	LVDS	LVDS_L1_P	7 53 56
R660	LVDS_DATA	LVDS	LVDS_L1_N	7 53 56
R660	LVDS_DATA	LVDS	LVDS_L2_P	7 53 56
R660	LVDS_DATA	LVDS	LVDS_L2_N	7 53 56
R660	LVDS_CLK_LOWER	LVDS	LVDS_LCLK	7 53 56
R660	LVDS_CLK_LOWER	LVDS	CLKLVDS_L_P	7 53 56
R660	LVDS_CLK_LOWER	LVDS	CLKLVDS_L_N	7 53 56
R660	VGA	VGA	GPU VGA_R	53 57
R660	VGA	VGA	GPU VGA_G	53 57
R660	VGA	VGA	GPU VGA_B	53 57
R660	VGA_CONN	VGA_CONN	VGA_R	57
R660	VGA_CONN	VGA_CONN	VGA_G	57
R660	VGA_CONN	VGA_CONN	VGA_B	57
R660	TV	TV	GPU TV_Y	53 57
R660	TV	TV	GPU TV_C	53 57
R660	TV	TV	GPU TV_COMP	53 57
R660	TV_CONN	TV_CONN	TV_Y	57
R660	TV_CONN	TV_CONN	TV_C	57
R660	TV_CONN	TV_CONN	TV_COMP	57



GPU (M11) DVI/DAC Outputs

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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	D	051-6839	E
SCALE	SHT	OF	
NONE	66	115	

Page Notes

Power aliases required by this page:
 - =PP3V3_RUN_SI - =PP1V5R3V3_DVO_VREF

Signal aliases required by this page:
 - =SI_TMDS_RESET_L - =RP67xxPy (pinswappable series R)
 - =SI_I2C_CLK
 - =SI_I2C_DATA

BOM options provided by this page:
 - TMDS_EXT - DVO_1V5 - DVO_3V3
 - TMDS_DUAL - DVO_1V8

Net Spacing Type: TMDS
 Net Physical Type: TMDS

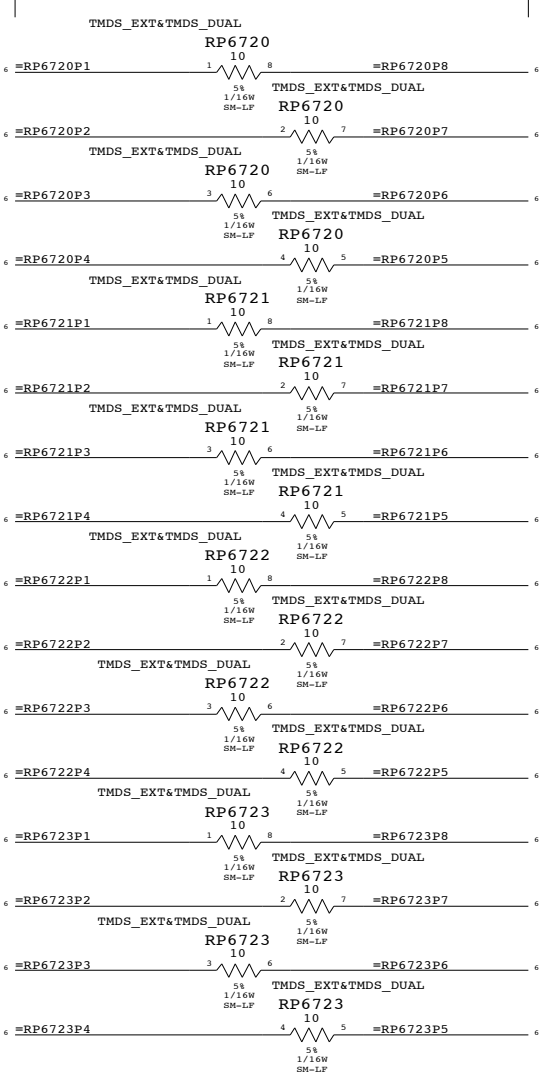
NOTE: Target differential impedance for TMDS data pairs is 100 ohms.

ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
E005		DVO	DVO
E006		DVO	DVO
E007		DVO	DVO
E008		DVO	DVO
E009		DVO	DVO
E010		DVO	DVO
E011		DVO	DVO
E012		DVO	DVO
E013		DVO	DVO
E014		DVO	DVO
E015		DVO	DVO
E016		DVO	DVO
E017		DVO	DVO
E018		DVO	DVO
E019		DVO	DVO
E020		DVO	DVO
E021		DVO	DVO
E022		DVO	DVO
E023		DVO	DVO
E024		DVO	DVO
E025		DVO	DVO
E026		DVO	DVO
E027		DVO	DVO
E028		DVO	DVO
E029		DVO	DVO
E030		DVO	DVO
E031		DVO	DVO
E032		DVO	DVO
E033		DVO	DVO
E034		DVO	DVO
E035		DVO	DVO
E036		DVO	DVO
E037		DVO	DVO
E038		DVO	DVO
E039		DVO	DVO
E040		DVO	DVO
E041		DVO	DVO
E042		DVO	DVO
E043		DVO	DVO
E044		DVO	DVO
E045		DVO	DVO
E046		DVO	DVO
E047		DVO	DVO
E048		DVO	DVO
E049		DVO	DVO
E050		DVO	DVO
E051		DVO	DVO
E052		DVO	DVO
E053		DVO	DVO
E054		DVO	DVO
E055		DVO	DVO
E056		DVO	DVO
E057		DVO	DVO
E058		DVO	DVO
E059		DVO	DVO
E060		DVO	DVO
E061		DVO	DVO
E062		DVO	DVO
E063		DVO	DVO
E064		DVO	DVO
E065		DVO	DVO
E066		DVO	DVO
E067		DVO	DVO
E068		DVO	DVO
E069		DVO	DVO
E070		DVO	DVO
E071		DVO	DVO
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E076		DVO	DVO
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E080		DVO	DVO
E081		DVO	DVO
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E085		DVO	DVO
E086		DVO	DVO
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E094		DVO	DVO
E095		DVO	DVO
E096		DVO	DVO
E097		DVO	DVO
E098		DVO	DVO
E099		DVO	DVO
E100		DVO	DVO

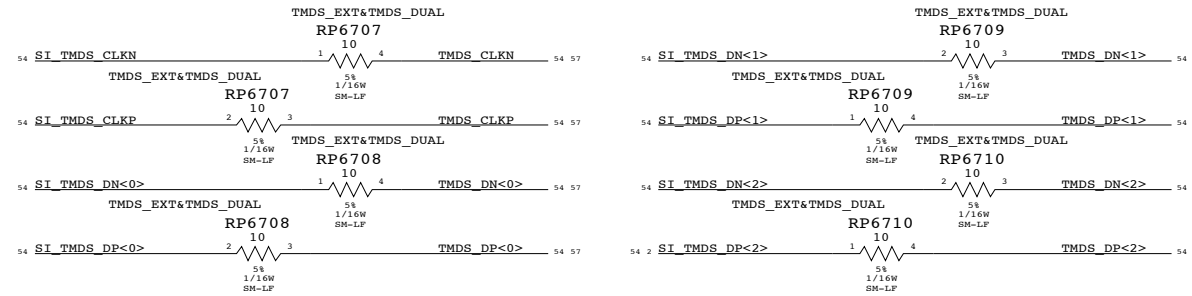
Lower DVO Termination

Place close to GPU

One each for: GPU_DVOD<0..11>
 GPU_DVO_HSYNC
 GPU_DVO_VSYNC
 GPU_DVO_DE
 GPU_DVO_CLKP

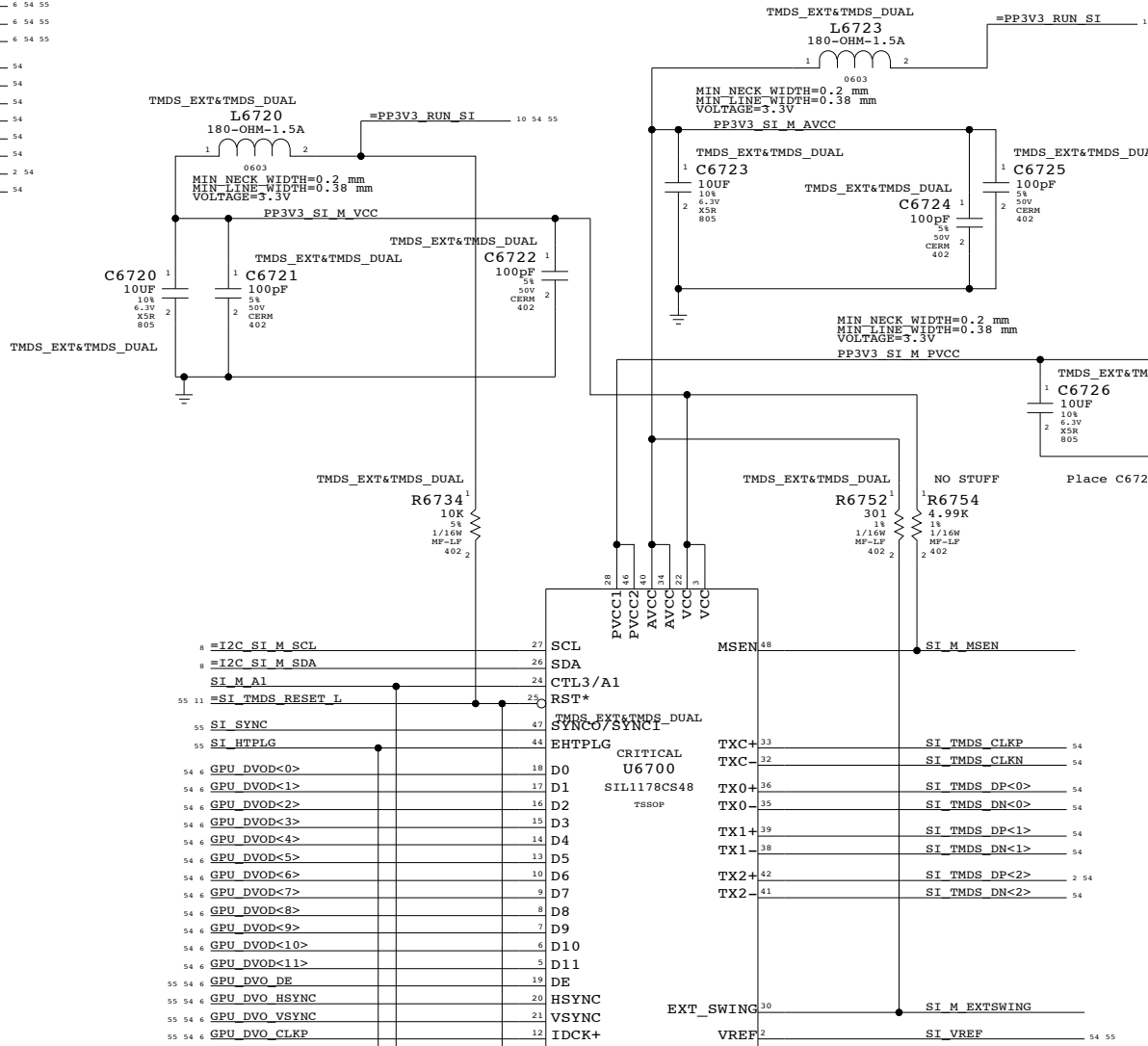
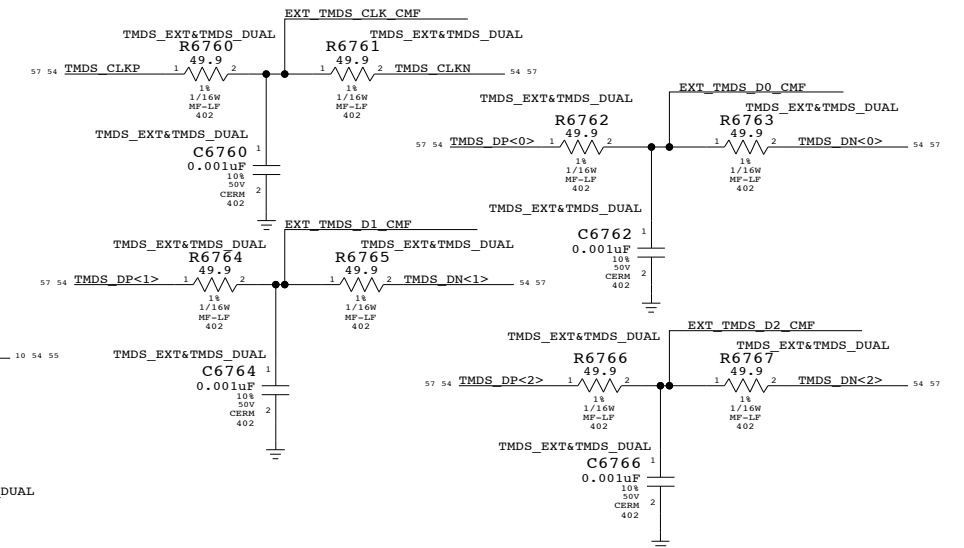


SILICON IMAGE TMDS



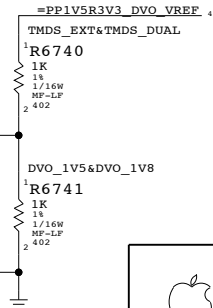
EXTERNAL TMDS TERMINATION

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN



ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
E005		TMDS	TMDS
E006		TMDS	TMDS
E007		TMDS	TMDS
E008		TMDS	TMDS
E009		TMDS	TMDS
E010		TMDS	TMDS
E011		TMDS	TMDS
E012		TMDS	TMDS
E013		TMDS	TMDS
E014		TMDS	TMDS
E015		TMDS	TMDS
E016		TMDS	TMDS
E017		TMDS	TMDS
E018		TMDS	TMDS
E019		TMDS	TMDS
E020		TMDS	TMDS
E021		TMDS	TMDS
E022		TMDS	TMDS
E023		TMDS	TMDS
E024		TMDS	TMDS
E025		TMDS	TMDS
E026		TMDS	TMDS
E027		TMDS	TMDS
E028		TMDS	TMDS
E029		TMDS	TMDS
E030		TMDS	TMDS
E031		TMDS	TMDS
E032		TMDS	TMDS
E033		TMDS	TMDS
E034		TMDS	TMDS
E035		TMDS	TMDS
E036		TMDS	TMDS
E037		TMDS	TMDS
E038		TMDS	TMDS
E039		TMDS	TMDS
E040		TMDS	TMDS
E041		TMDS	TMDS
E042		TMDS	TMDS
E043		TMDS	TMDS
E044		TMDS	TMDS
E045		TMDS	TMDS
E046		TMDS	TMDS
E047		TMDS	TMDS
E048		TMDS	TMDS
E049		TMDS	TMDS
E050		TMDS	TMDS
E051		TMDS	TMDS
E052		TMDS	TMDS
E053		TMDS	TMDS
E054		TMDS	TMDS
E055		TMDS	TMDS
E056		TMDS	TMDS
E057		TMDS	TMDS
E058		TMDS	TMDS
E059		TMDS	TMDS
E060		TMDS	TMDS
E061		TMDS	TMDS
E062		TMDS	TMDS
E063		TMDS	TMDS
E064		TMDS	TMDS
E065		TMDS	TMDS
E066		TMDS	TMDS
E067		TMDS	TMDS
E068		TMDS	TMDS
E069		TMDS	TMDS
E070		TMDS	TMDS
E071		TMDS	TMDS
E072		TMDS	TMDS
E073		TMDS	TMDS
E074		TMDS	TMDS
E075		TMDS	TMDS
E076		TMDS	TMDS
E077		TMDS	TMDS
E078		TMDS	TMDS
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E084		TMDS	TMDS
E085		TMDS	TMDS
E086		TMDS	TMDS
E087		TMDS	TMDS
E088		TMDS	TMDS
E089		TMDS	TMDS
E090		TMDS	TMDS
E091		TMDS	TMDS
E092		TMDS	TMDS
E093		TMDS	TMDS
E094		TMDS	TMDS
E095		TMDS	TMDS
E096		TMDS	TMDS
E097		TMDS	TMDS
E098		TMDS	TMDS
E099		TMDS	TMDS
E100		TMDS	TMDS

The DVO bus can be run with 3.3V or 1.5V/1.8V signaling. The power rail for the reference should be connected to the GPU DVO rail.



Lower TMDS Transmitter
 SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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	D	051-6839	E
SCALE	SHEET	OF	
NONE	67	115	

Page Notes

Power aliases required by this page:
 - =PP3V3_RUN_SI

Signal aliases required by this page:
 - =SI_I2C_CLK - =SI_TMDS_RESET_L
 - =SI_I2C_DATA - =RP68xxPy (pinswappable series R)

BOM options provided by this page:
 - TMDS_DUAL

Net Spacing Type: TMDS
 Net Physical Type: TMDS

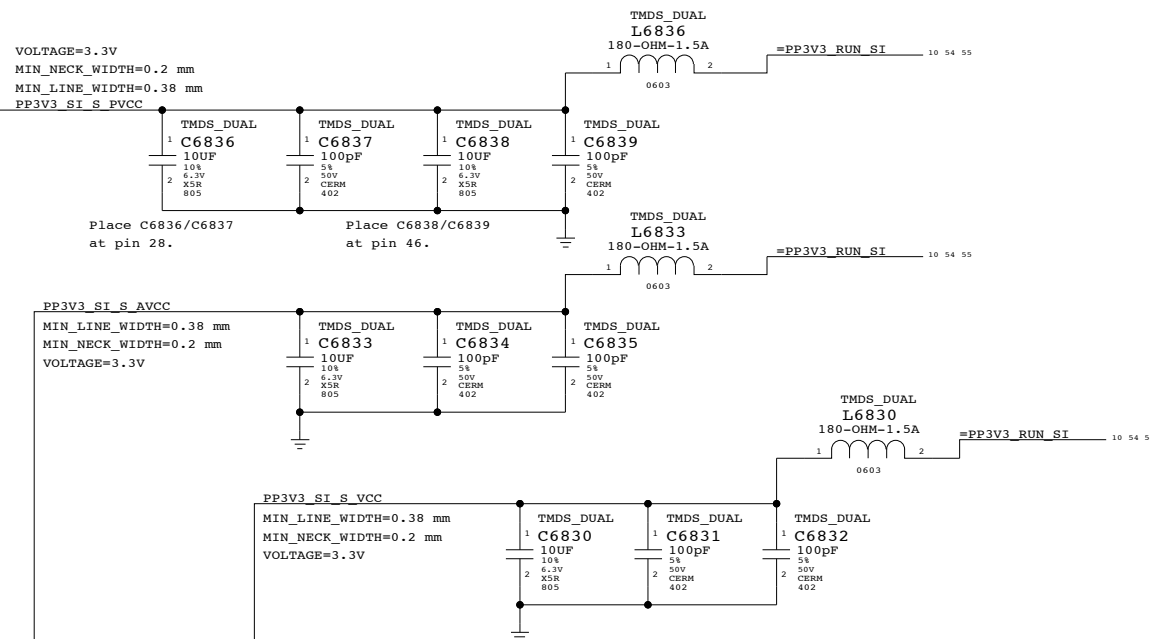
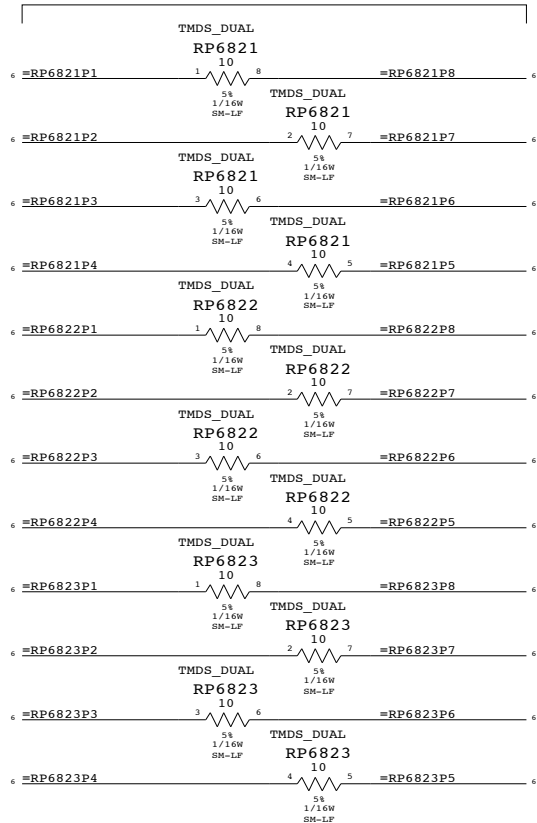
NOTE: Target differential impedance for TMDS data pairs is 100 ohms.

ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
GPU_DVO_UPPER	DVO	DVO	
GPU_DVOD20	DVO	DVO	
GPU_DVO_UPPER	DVO	DVO	
	PROVIDED BY LOWER TXNR		
	PROVIDED BY LOWER TXNR		
	PROVIDED BY LOWER TXNR		
TMDS_DATA	TMDS	TMDS	SI_TMDS_D3
TMDS_DATA	TMDS	TMDS	SI_TMDS_D3
TMDS_DATA	TMDS	TMDS	SI_TMDS_D4
TMDS_DATA	TMDS	TMDS	SI_TMDS_D4
TMDS_DATA	TMDS	TMDS	SI_TMDS_D5
TMDS_DATA	TMDS	TMDS	SI_TMDS_D5
	TMDS	TMDS	TMDS_D3
	TMDS	TMDS	TMDS_D3
	TMDS	TMDS	TMDS_D4
	TMDS	TMDS	TMDS_D4
	TMDS	TMDS	TMDS_D5
	TMDS	TMDS	TMDS_D5

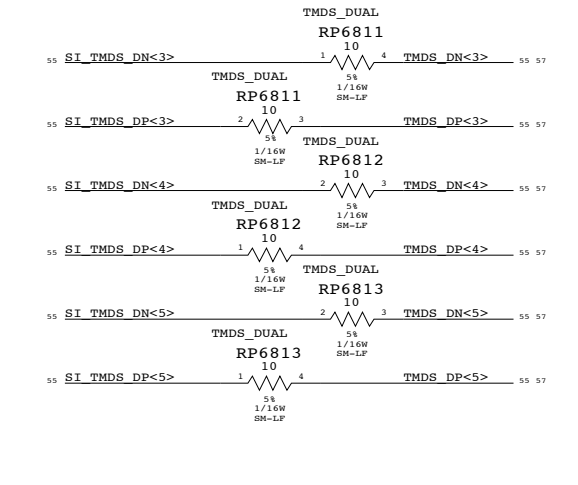
Upper DVO series termination

Place close to GPU

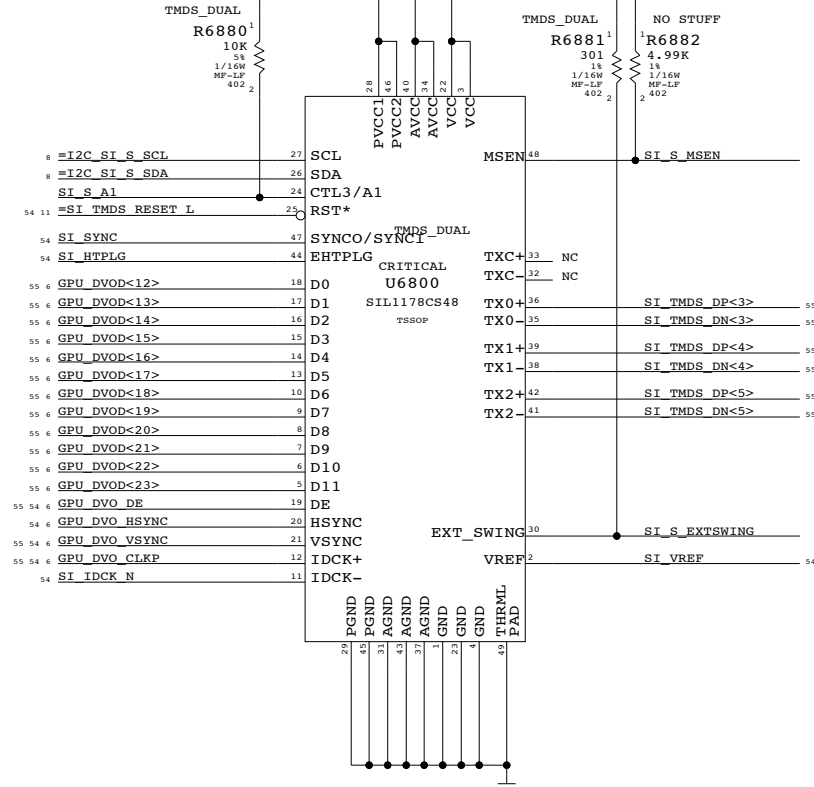
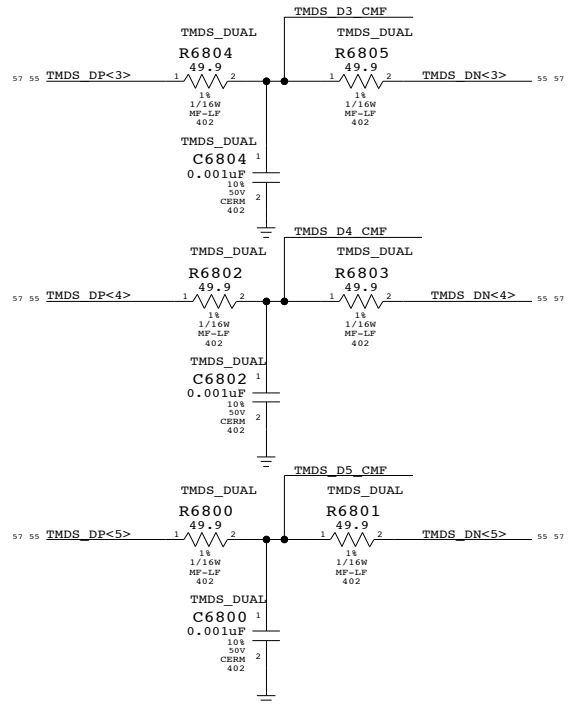
One for each of: GPU_DVOD<12..23>



Upper Channel Series Termination



Upper Channel Common-mode Termination

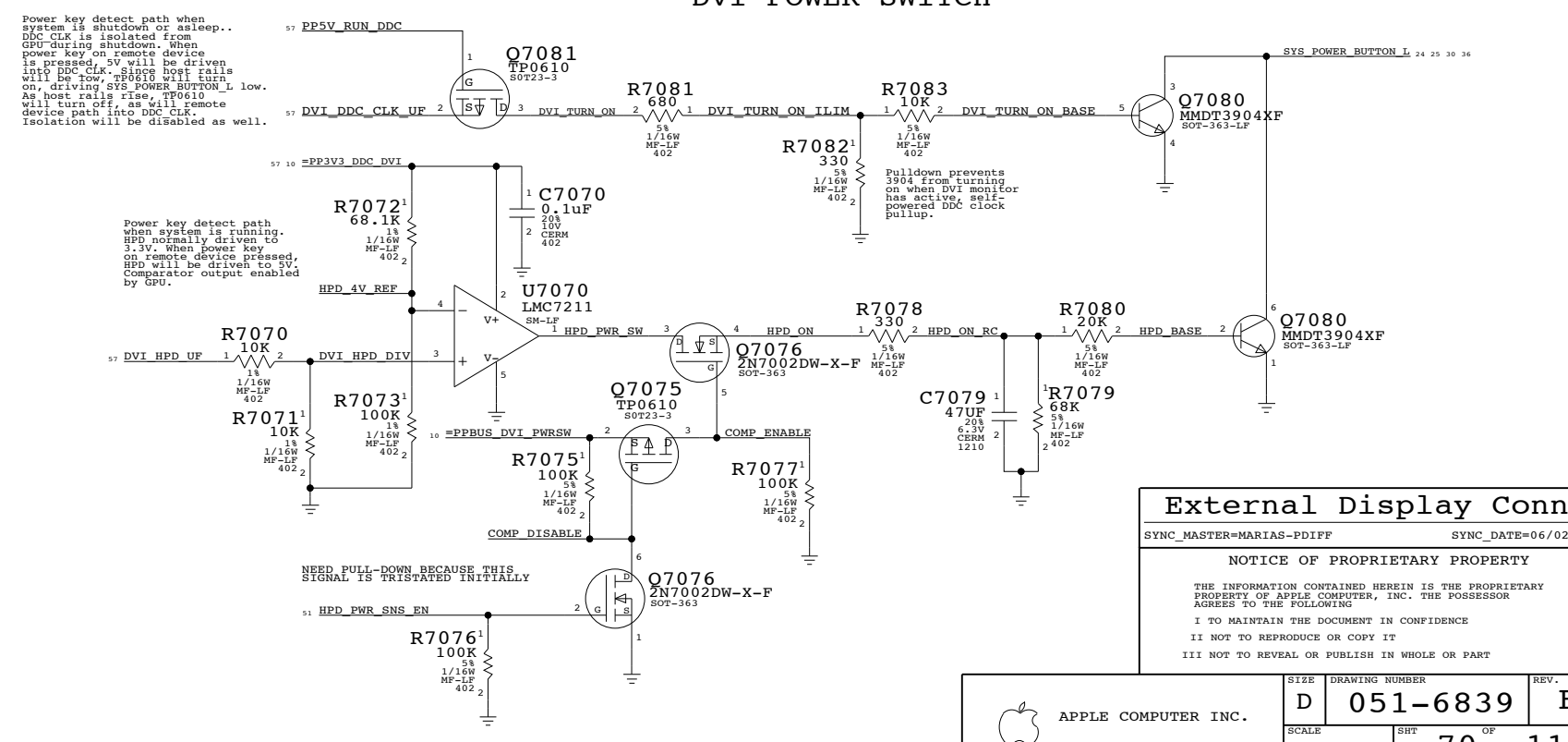
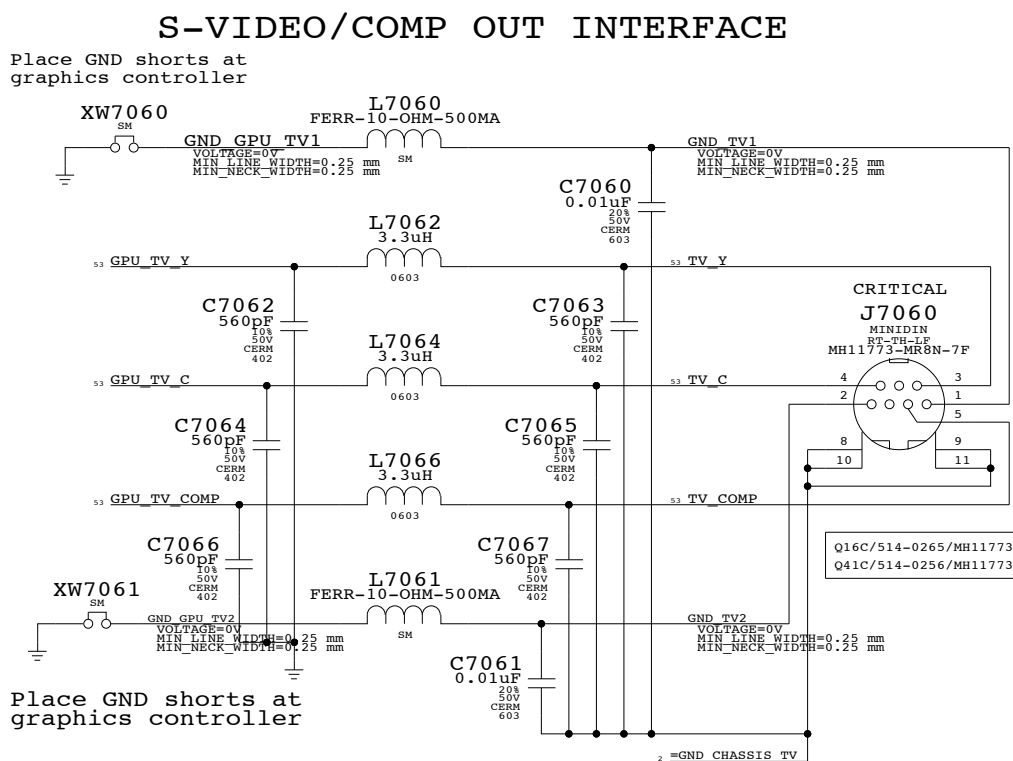
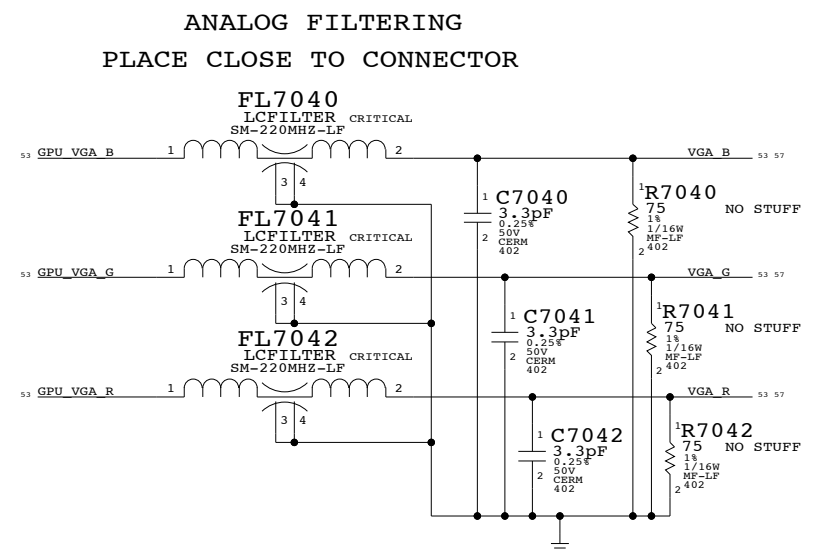
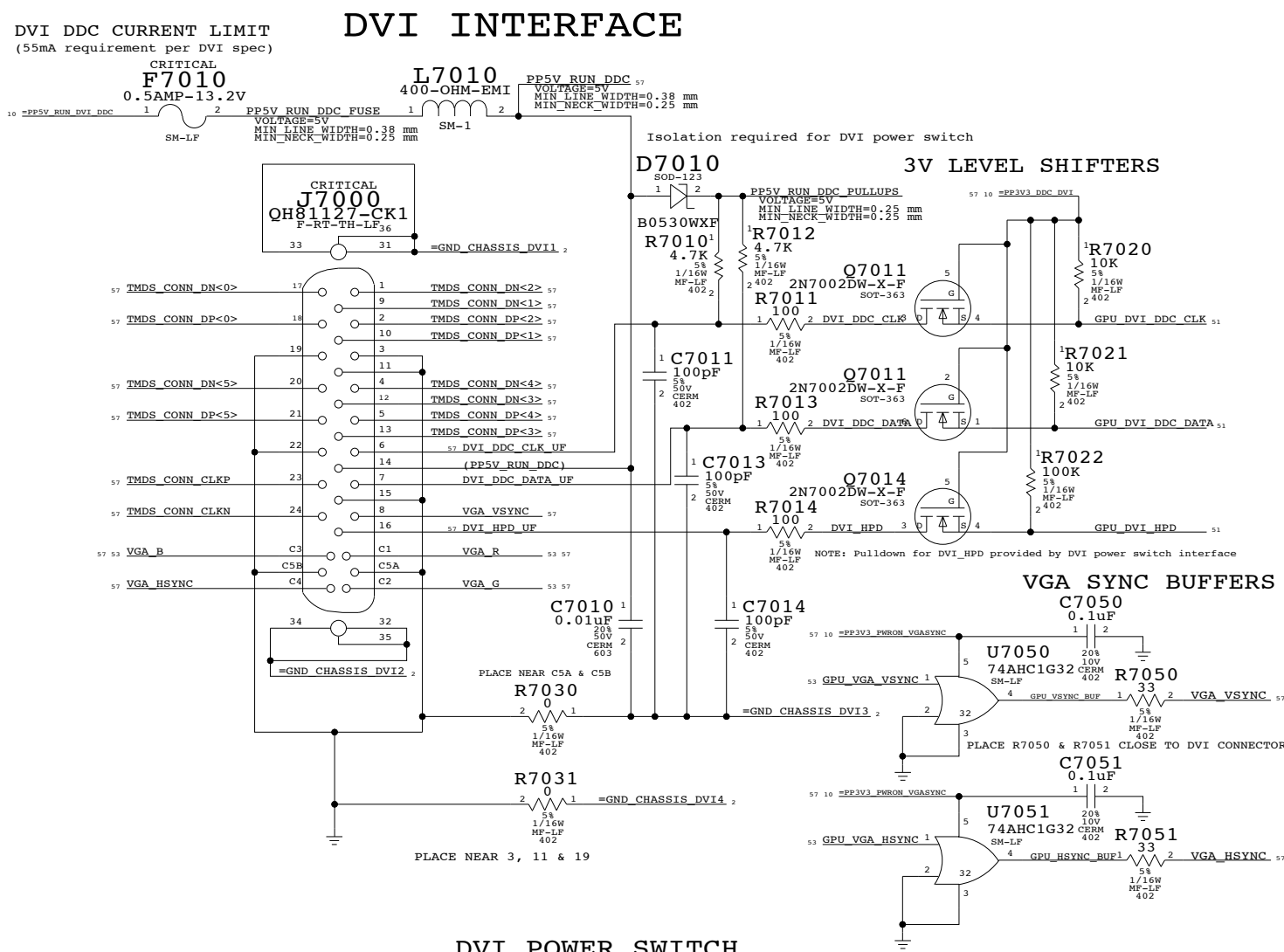
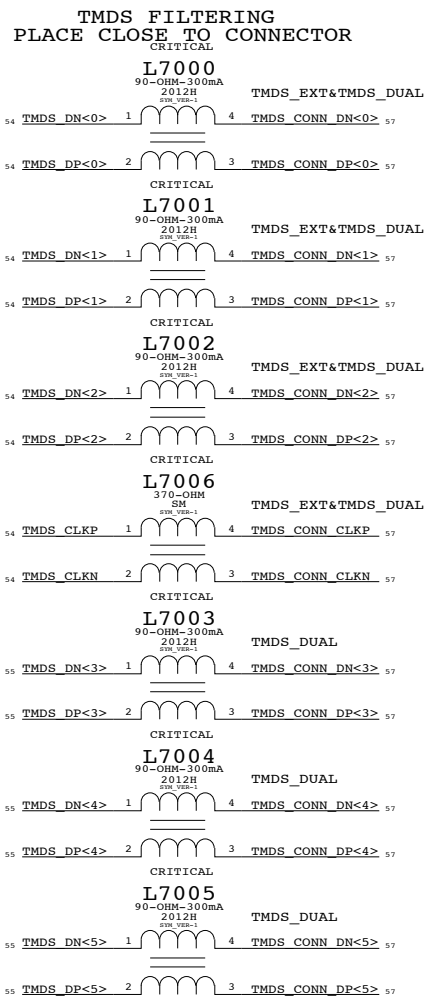


Upper TMDS Transmitter
 SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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	D	051-6839	E
SCALE	SHT	OF	
NONE	68	115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_CLK	TMDS_CONN_CLK
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_CLKN	TMDS_CONN_CLKN
E550	TMDS_CONN_TMDS_CONN		TMDS_CONN_D0	TMDS_CONN_DP<0>
E550	TMDS_CONN_TMDS_CONN		TMDS_CONN_D0	TMDS_CONN_DP<0>
E550	TMDS_CONN_TMDS_CONN		TMDS_CONN_D1	TMDS_CONN_DP<1>
E550	TMDS_CONN_TMDS_CONN		TMDS_CONN_D1	TMDS_CONN_DP<1>
E550	TMDS_CONN_TMDS_CONN		TMDS_CONN_D2	TMDS_CONN_DP<2>
E550	TMDS_CONN_TMDS_CONN		TMDS_CONN_D2	TMDS_CONN_DP<2>
E550	TMDS_CONN_TMDS_CONN		TMDS_CONN_D3	TMDS_CONN_DP<3>
E550	TMDS_CONN_TMDS_CONN		TMDS_CONN_D3	TMDS_CONN_DP<3>
E560	TMDS_CONN_TMDS_CONN		TMDS_CONN_D4	TMDS_CONN_DP<4>
E560	TMDS_CONN_TMDS_CONN		TMDS_CONN_D4	TMDS_CONN_DP<4>
E560	TMDS_CONN_TMDS_CONN		TMDS_CONN_D5	TMDS_CONN_DP<5>
E560	TMDS_CONN_TMDS_CONN		TMDS_CONN_D5	TMDS_CONN_DP<5>



External Display Conns

SYNC_MASTER=MARIAS-PDIFF SYNC_DATE=06/02/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6839	E
SCALE	SHT	OF	
NONE	70	115	

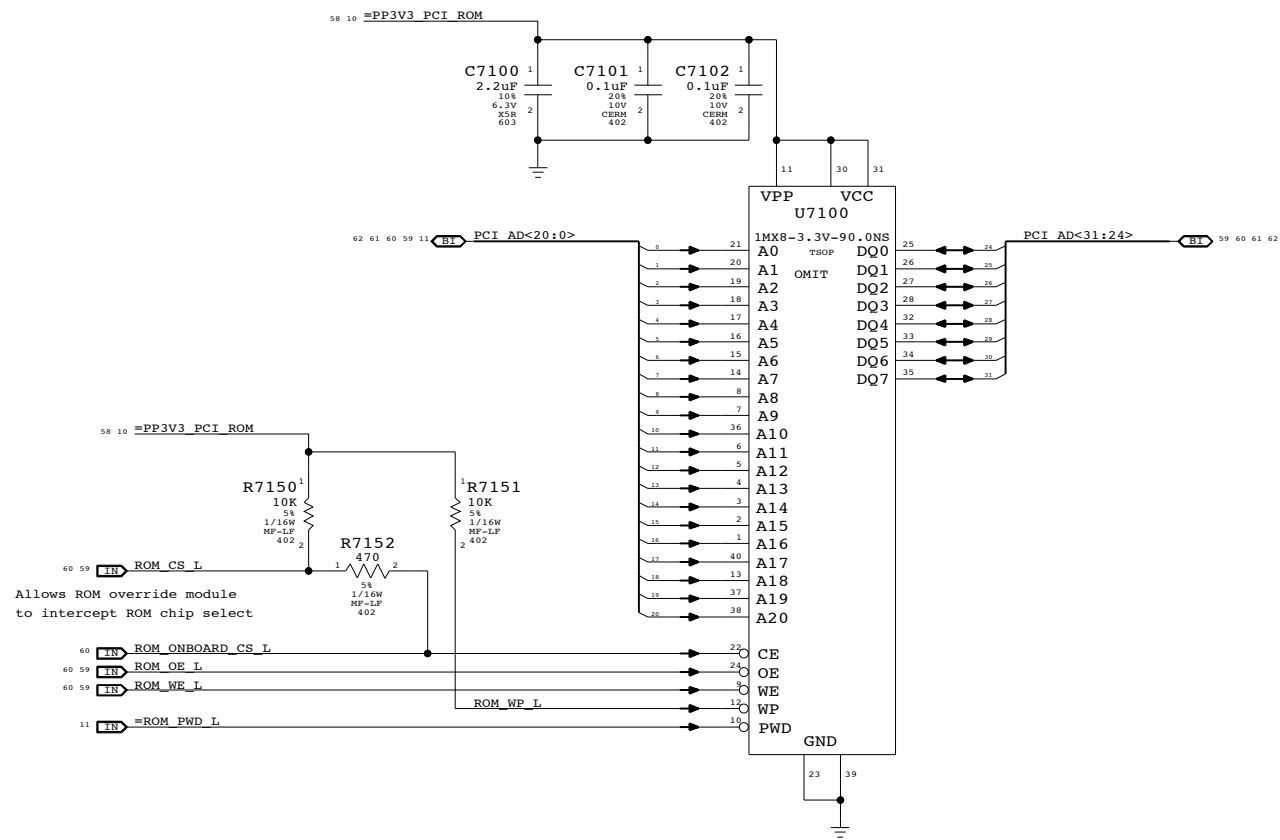
Page Notes

Power aliases required by this page:
 - =PP3V3_PCI_ROM

Signal aliases required by this page:
 - =ROM_PWD_L

BOM options provided by this page:
 (NONE)

NOTE: This page does not specify a BootROM part number. Must use a TABLE_x_ITEM symbol to declare U7100 part number.



BootROM

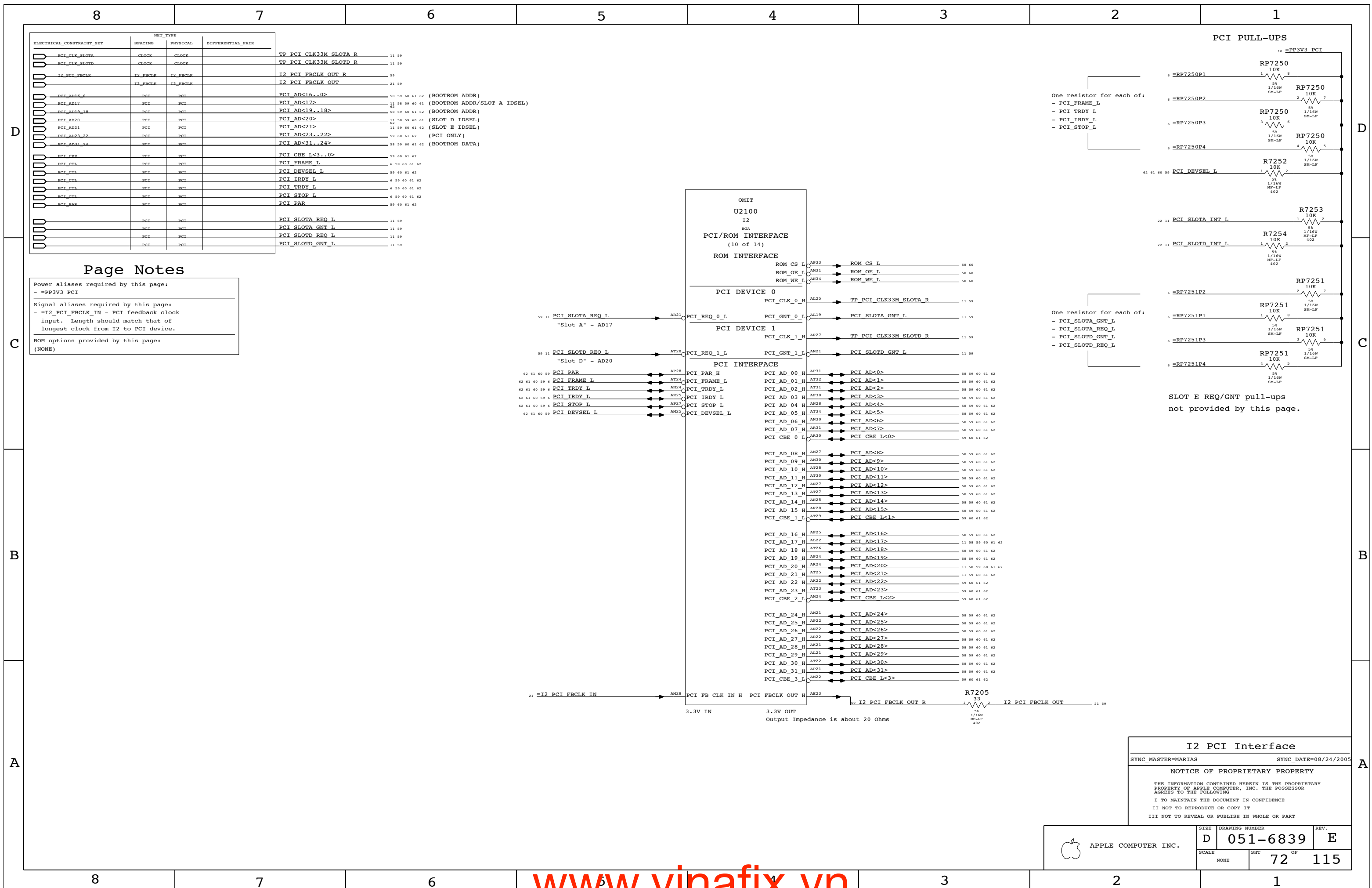
SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6839	E
SCALE	SHT	OF	
NONE	71	115	

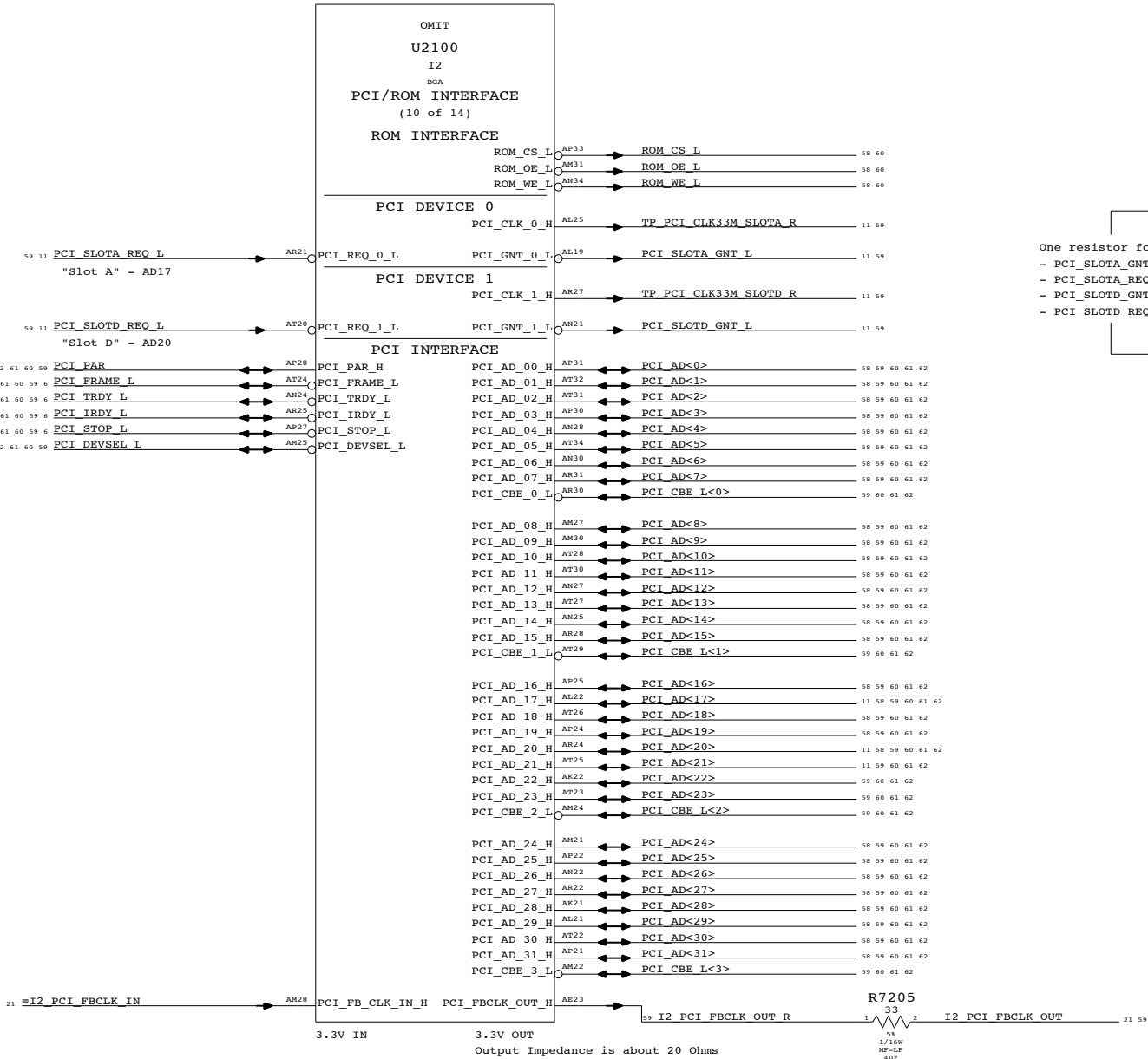


ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
PCI_CLK_SLOTA	CLOCK	CLOCK	
PCI_CLK_SLOTD	CLOCK	CLOCK	
I2_PCI_FBCLK	I2_FBCLK	I2_FBCLK	
PCI_AD<16..0>	PCI	PCI	
PCI_AD<17>	PCI	PCI	
PCI_AD<19..18>	PCI	PCI	
PCI_AD<20>	PCI	PCI	
PCI_AD<21>	PCI	PCI	
PCI_AD<23..22>	PCI	PCI	
PCI_AD<31..24>	PCI	PCI	
PCI_CBE L<3..0>	PCI	PCI	
PCI_FRAME L	PCI	PCI	
PCI_DEVSEL L	PCI	PCI	
PCI_IRDY L	PCI	PCI	
PCI_TRDY L	PCI	PCI	
PCI_STOP L	PCI	PCI	
PCI_PAR	PCI	PCI	
PCI_SLOTA_REQ L	PCI	PCI	
PCI_SLOTA_GNT L	PCI	PCI	
PCI_SLOTD_REQ L	PCI	PCI	
PCI_SLOTD_GNT L	PCI	PCI	

NET	TYPE	DESCRIPTION
TP_PCI_CLK33M_SLOTA_R	11 59	(BOOTROM ADDR)
TP_PCI_CLK33M_SLOTD_R	11 59	(BOOTROM ADDR/SLOT A IDSEL)
I2_PCI_FBCLK_OUT_R	59	(BOOTROM ADDR)
I2_PCI_FBCLK_OUT	21 59	(BOOTROM ADDR)
PCI_AD<16..0>	58 59 60 61 62	(BOOTROM ADDR)
PCI_AD<17>	11 58 59 60 61	(BOOTROM ADDR/SLOT A IDSEL)
PCI_AD<19..18>	58 59 60 61 62	(BOOTROM ADDR)
PCI_AD<20>	11 58 59 60 61	(SLOT D IDSEL)
PCI_AD<21>	11 59 60 61 62	(SLOT E IDSEL)
PCI_AD<23..22>	59 60 61 62	(PCI ONLY)
PCI_AD<31..24>	58 59 60 61 62	(BOOTROM DATA)
PCI_CBE L<3..0>	59 60 61 62	
PCI_FRAME L	6 59 60 61 62	
PCI_DEVSEL L	59 60 61 62	
PCI_IRDY L	6 59 60 61 62	
PCI_TRDY L	6 59 60 61 62	
PCI_STOP L	6 59 60 61 62	
PCI_PAR	59 60 61 62	
PCI_SLOTA_REQ L	11 59	
PCI_SLOTA_GNT L	11 59	
PCI_SLOTD_REQ L	11 59	
PCI_SLOTD_GNT L	11 59	

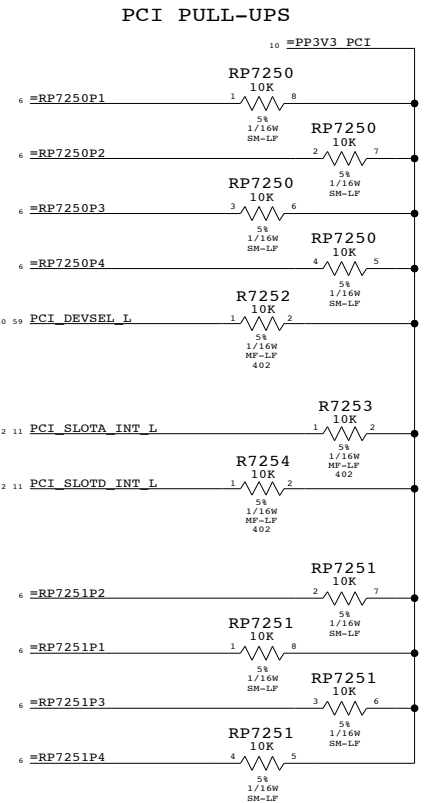
Page Notes

- Power aliases required by this page:
 - =PP3V3_PCI
- Signal aliases required by this page:
 - =I2_PCI_FBCLK_IN - PCI feedback clock input. Length should match that of longest clock from I2 to PCI device.
- BOM options provided by this page:
 (NONE)



One resistor for each of:
 - PCI_FRAME_L
 - PCI_TRDY_L
 - PCI_IRDY_L
 - PCI_STOP_L

One resistor for each of:
 - PCI_SLOTA_GNT_L
 - PCI_SLOTA_REQ_L
 - PCI_SLOTD_GNT_L
 - PCI_SLOTD_REQ_L



SLOT E REQ/GNT pull-ups not provided by this page.

I2 PCI Interface
 SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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	D	051-6839	E
SCALE	NONE	SHT	OF
		72	115

NET TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
MEM	CLOCK	CLOCK	

=PCI_CLK33M_AIRPORT 11 60

Page Notes

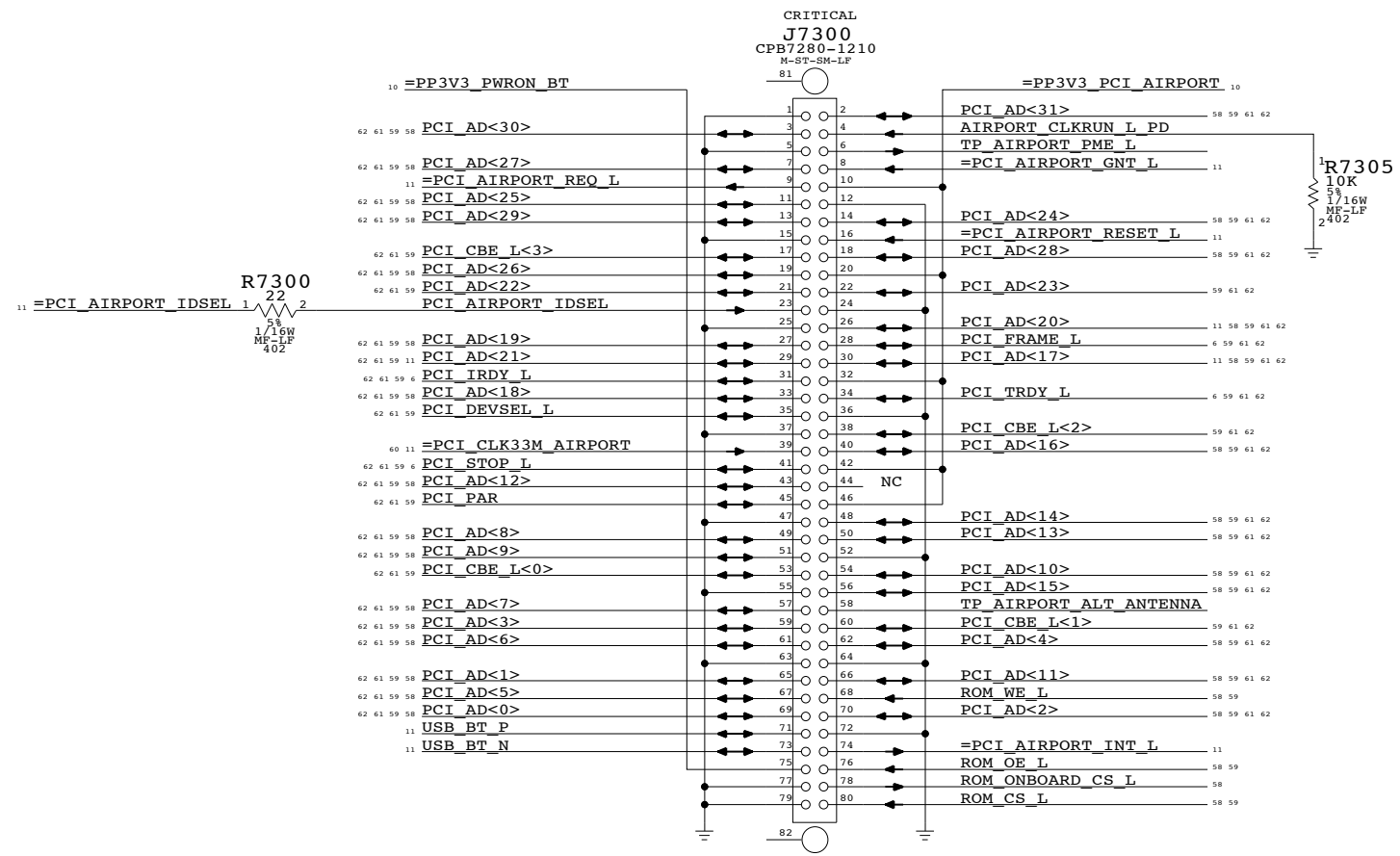
Power aliases required by this page:
 - =PP3V3_PCI (802.11g Power)
 - =PP3V3_PWRON_BT (Bluetooth Power)

Signal aliases required by this page:
 - =PCI_CLK33M_AIRPORT (33MHz PCI clock)
 - =PCI_AIRPORT_RESET_L (PCI Reset)
 - =USB_BT_P (Bluetooth USB D+)
 - =USB_BT_N (Bluetooth USB D-)

BOM options provided by this page:
 (NONE)

PCI Devices implemented on this page:
 AD17 (Slot "A") - AirPort (0x????/0x????)

NOTE: This AirPort implementation does not support PME#.

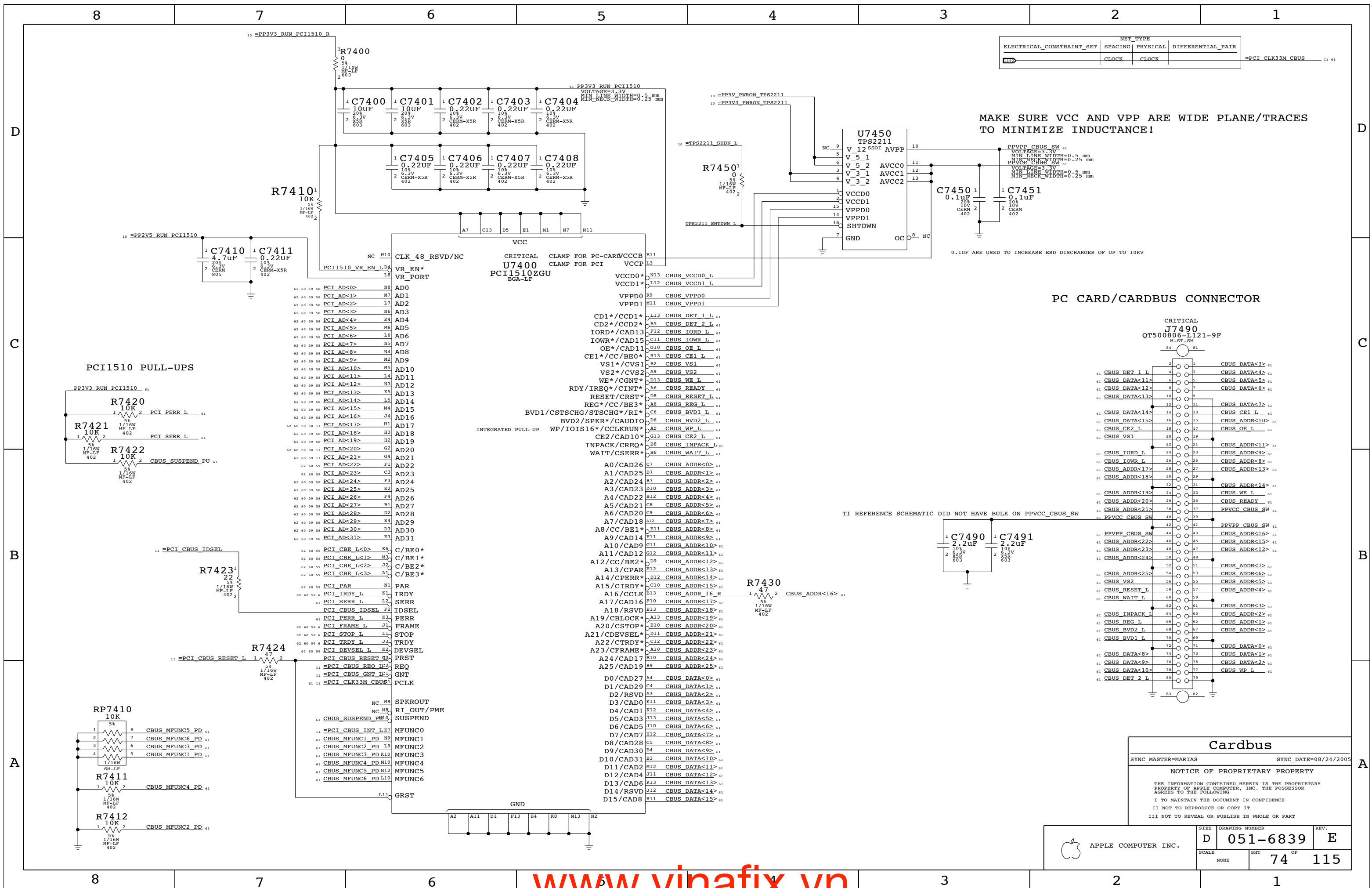


Q85 Connector
 Q16C/516S0361/F-ST-SM
 Q41C/516S0352/M-ST-SM-LF

Q85 AIRPORT/BT CONN
 SYNC_MASTER=MARIAS-MDIFF SYNC_DATE=N/A

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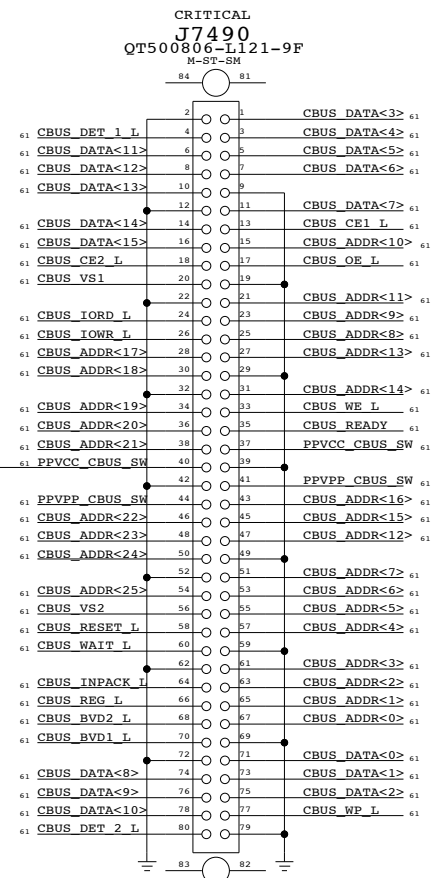
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6839	E
SCALE	SHT OF		
NONE	73 OF		115



NET TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
E12	CLOCK	CLOCK	

MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES TO MINIMIZE INDUCTANCE!

PC CARD/CARDBUS CONNECTOR



Cardbus

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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	D	051-6839	E
SCALE	SHT	OF	
NONE	74	115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		DIFFERENTIAL_PAIR
	SPACING	PHYSICAL	
10	CLOCK	CLOCK	

=PCI_CLK33M_USB2 11 02

Page Notes

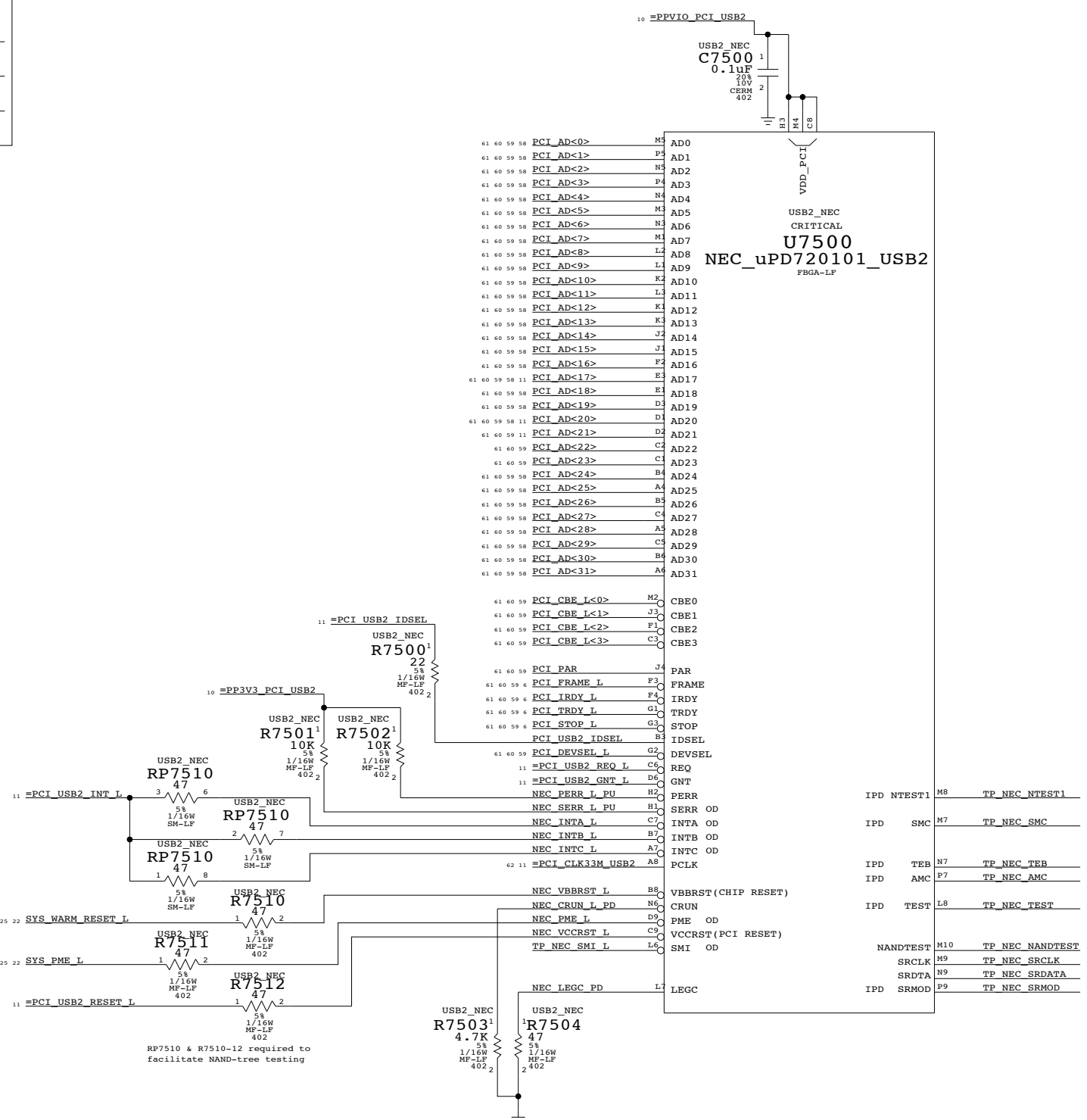
Power aliases required by this page:
 - =PPVIO_PCI (to 3.3V or 5V)
 - =PP3V3_PCI_USB2 (D3cold rail)

Signal aliases required by this page:
 - =PCI_CLK33M_USB2
 - =PCI_USB2_REQ_L - =PCI_USB2_IDSEL
 - =PCI_USB2_GNT_L - =PCI_USB2_RESET_L
 - =PCI_USB2_INT_L

BOM options provided by this page:
 - USB2_NEC

PCI Devices implemented on this page:
 AD27 (Slot "G") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports D3cold.



RP7510 & R7510-12 required to facilitate NAND-tree testing

NEC USB2

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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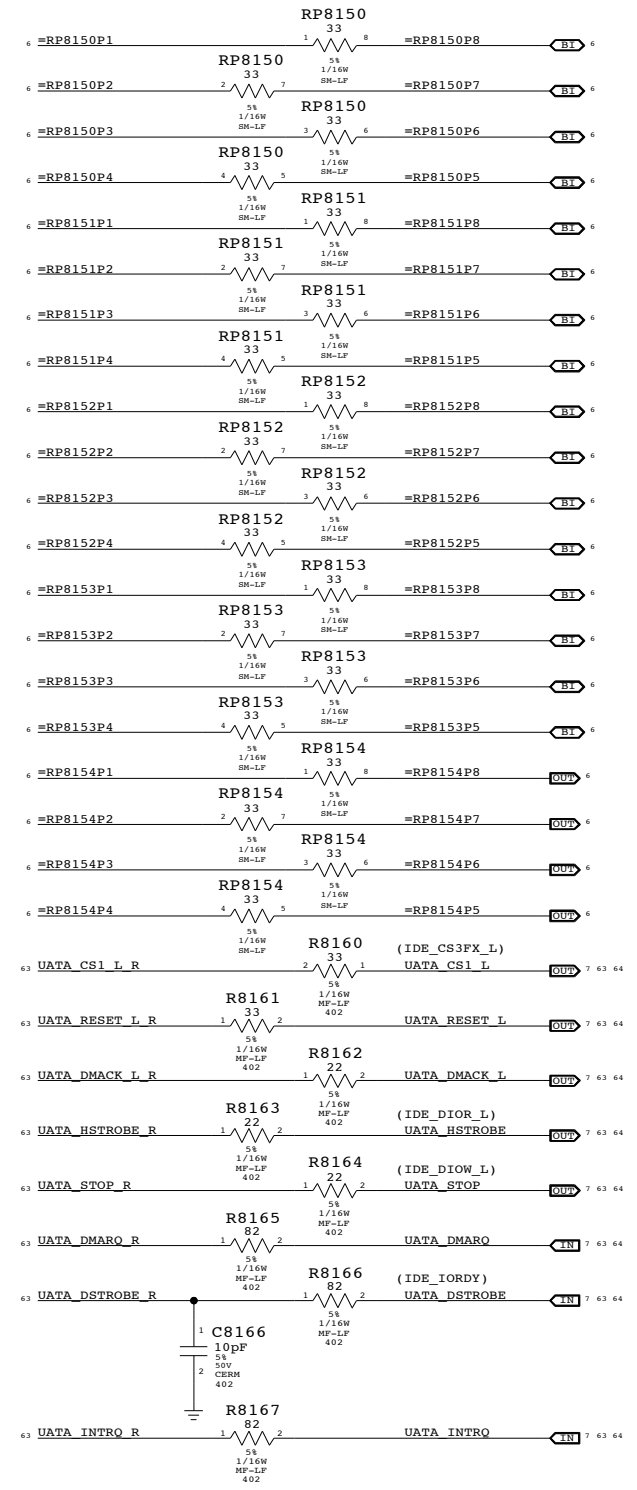
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	D	051-6839	E
SCALE	SHT OF		
NONE	75 OF		115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		DIFFERENTIAL_PAIR
	SPACING	PHYSICAL	
UATA_DD	DATA	DATA	UATA_DD R<15..8>
UATA_DD7	DATA	DATA	UATA_DD R<7>
UATA_DD	DATA	DATA	UATA_DD R<6..0>
UATA_HBST	DATA	DATA	UATA_DA R<2..0>
UATA_HBST	DATA	DATA	UATA_CS0 L R
UATA_HBST	DATA	DATA	UATA_CS1 L R
UATA_HSTROBE	DATA	DATA	UATA_HSTROBE R
UATA_HBST	DATA	DATA	UATA_STOP R
UATA_HBST_R	DATA	DATA	UATA_DMACK L R
UATA_HBST_R	DATA	DATA	UATA_RESET L R
UATA_HSTROBE	DATA	DATA	UATA_DSTROBE R
UATA_DEV_R	DATA	DATA	UATA_DMARQ R
UATA_DEV_R	DATA	DATA	UATA_INTRQ R
UATA_DEV_R	DATA	DATA	UATA_DD<15..0>
UATA_DEV_R	DATA	DATA	UATA_DA<2..0>
UATA_DEV_R	DATA	DATA	UATA_CS0 L
UATA_DEV_R	DATA	DATA	UATA_CS1 L
UATA_DEV_R	DATA	DATA	UATA_HSTROBE
UATA_DEV_R	DATA	DATA	UATA_STOP
UATA_DEV_R	DATA	DATA	UATA_DMACK L
UATA_DEV_R	DATA	DATA	UATA_RESET L
UATA_DEV_R	DATA	DATA	UATA_DSTROBE
UATA_DEV_R	DATA	DATA	UATA_DMARQ
UATA_DEV_R	DATA	DATA	UATA_INTRQ

UATA100 SERIES TERMINATION

PLACE CLOSE TO I2



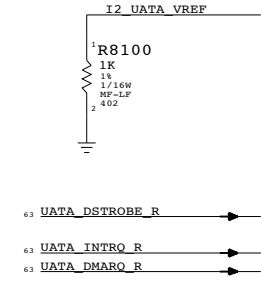
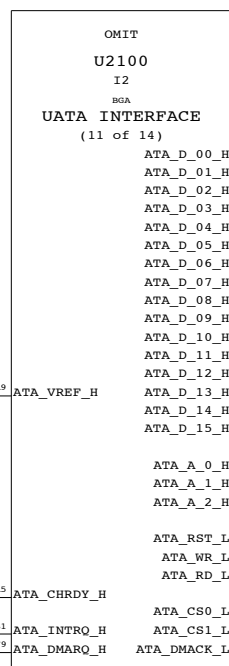
One resistor for each of:
 - UATA_DD<15..0>(_R)
 - UATA_DA<2..0>(_R)
 - UATA_CS0 L(_R)
 - UATA_CS1FX L

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



I2 UATA Interface
 SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6839	E
SCALE	NONE	SHT	OF
		81	115

D

D

C

C

B

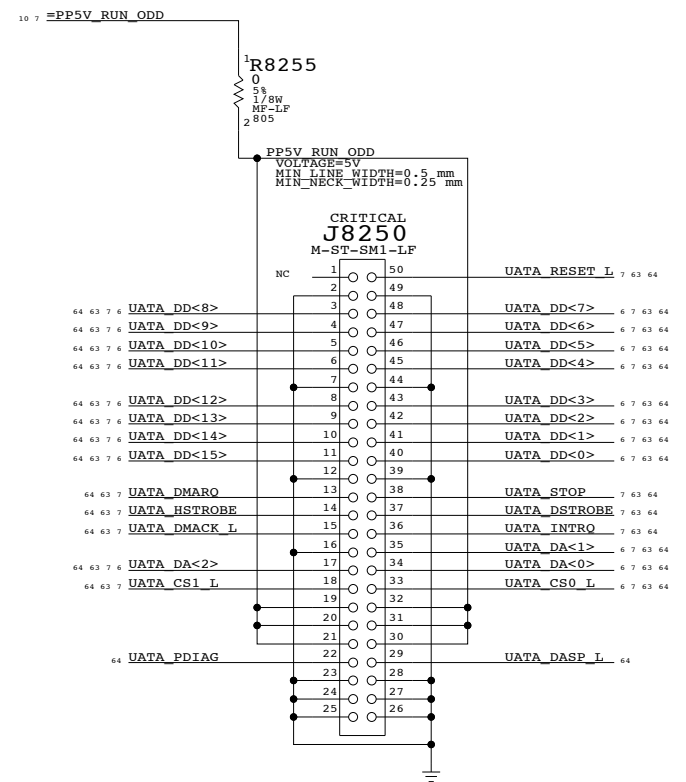
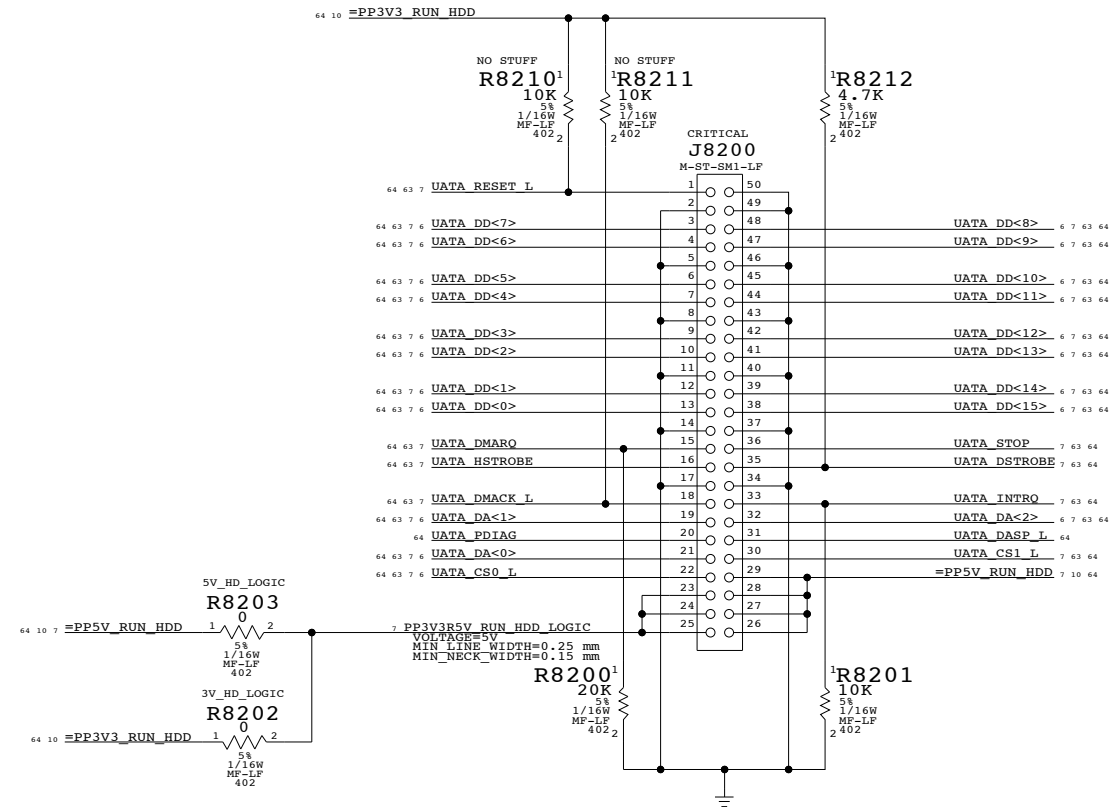
B

A

A

HDD CONNECTOR

ODD CONNECTOR



ATA Connectors
 Q16C/516S0357/M-ST-SM2-LF
 Q41C/516S0335/M-ST-SM1-LF

HDD/ODD Connectors
 SYNC_MASTER=MARIAS-PDIFF SYNC_DATE=06/02/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6839	E
SCALE	SHT OF		
NONE	82 OF		115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
ENET_RX_CLK25M	CLOCK	CLOCK		
ENET_RX_CLK125M	CLOCK	CLOCK		
ENET_GBE_REF	CLOCK	CLOCK		
ENET_TX_CLK	CLOCK	CLOCK		
ENET_RXD<0>	ENET	ENET		
ENET_RXD<1>	ENET	ENET		
ENET_RXD<2>	ENET	ENET		
ENET_RXD<3>	ENET	ENET		
ENET_RXD<4>	ENET	ENET		
ENET_RXD<5>	ENET	ENET		
ENET_RXD<6>	ENET	ENET		
ENET_RXD<7>	ENET	ENET		
ENET_RX_DV	ENET	ENET		
ENET_RX_ER	ENET	ENET		
ENET_TXD<0>	ENET	ENET		
ENET_TXD<1>	ENET	ENET		
ENET_TXD<2>	ENET	ENET		
ENET_TXD<3>	ENET	ENET		
ENET_TXD<4>	ENET	ENET		
ENET_TXD<5>	ENET	ENET		
ENET_TXD<6>	ENET	ENET		
ENET_TXD<7>	ENET	ENET		
ENET_TX_EN	ENET	ENET		
ENET_TX_ER	ENET	ENET		
ENET_COL	ENET	ENET		
ENET_CR	ENET	ENET		
ENET_MDC	ENET	ENET		
ENET_MDIO	ENET	ENET		
I2_ENET_MDIO	ENET	ENET		

Page Notes

Power aliases required by this page:
- =PP2V5R3V3_PWRON_I2_ENET

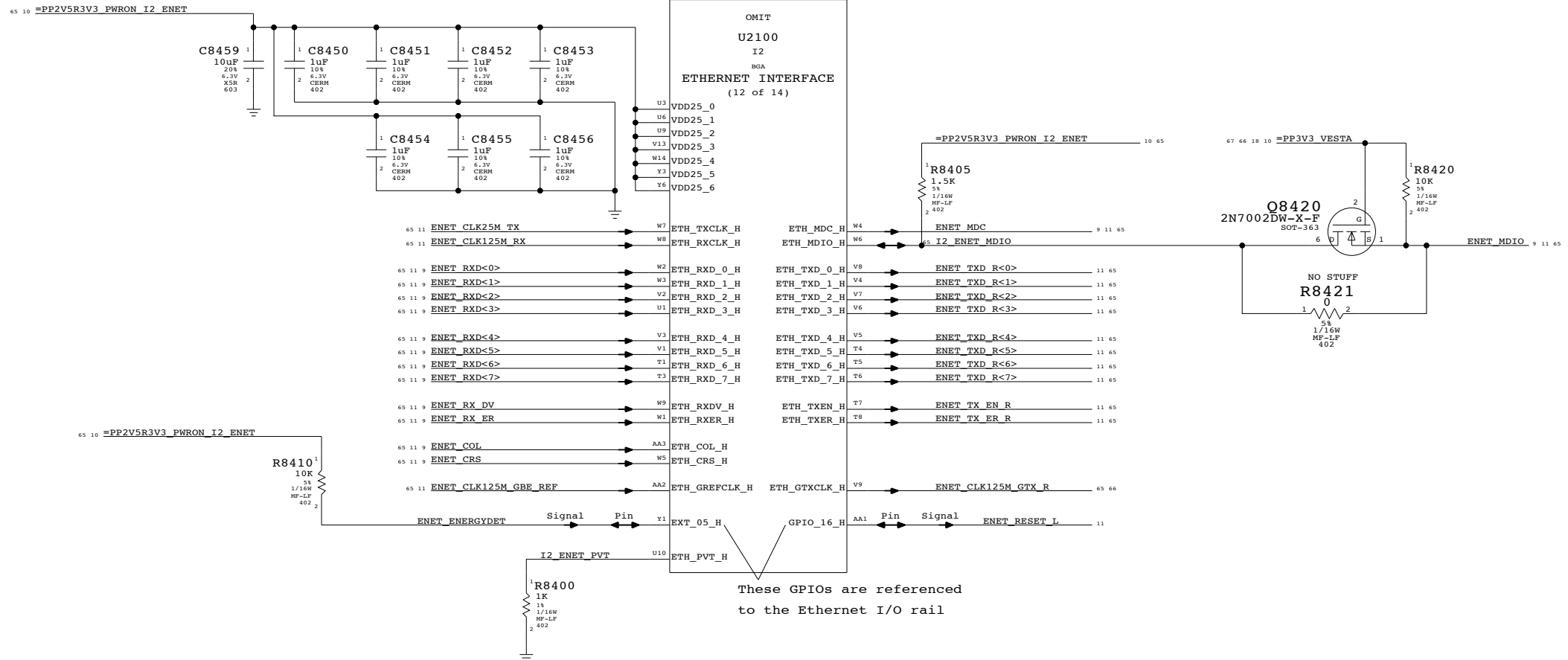
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: This page does not provide any series termination. Any termination, including clock signals, should be provided by the PHY page or a non-shared schematic page.

NOTE: All I2 GPIOs should have a pull-up or pull-down resistor. This page does not provide a resistor for GPIO 16. It must be provided by the PHY page or a non-shared schematic page.

NOTE: ENET_RX_DV has a hold spec violation on I2. May want to lengthen net by ~250ps. Net has a unique ECSet name to allow this.



These GPIOs are referenced to the Ethernet I/O rail

I2 Ethernet Interface

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6839	E
SCALE	SHT	OF	
NONE	84	115	

NET TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
(PROVIDED BY LINK PAGE)	CLOCK	CLOCK	
(PROVIDED BY LINK PAGE)	CLOCK	CLOCK	
(PROVIDED BY LINK PAGE)	CLOCK	CLOCK	
ENETCONN	ENETCONN	ENETCONN	ENETCONN_0
ENETCONN	ENETCONN	ENETCONN	ENETCONN_0
ENETCONN	ENETCONN	ENETCONN	ENETCONN_1
ENETCONN	ENETCONN	ENETCONN	ENETCONN_1
ENETCONN	ENETCONN	ENETCONN	ENETCONN_2
ENETCONN	ENETCONN	ENETCONN	ENETCONN_2
ENETCONN	ENETCONN	ENETCONN	ENETCONN_3
ENETCONN	ENETCONN	ENETCONN	ENETCONN_3
VESTA_CLK25M_XTAL	XTAL	XTAL	
VESTA_CLK25M_XTALO	XTAL	XTAL	
VESTA_CLK25M_XTALO_R	XTAL	XTAL	

Page Notes

Power aliases required by this page:
 - =PP2V5_ENETFW
 - =PP1V2_ENETFW

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

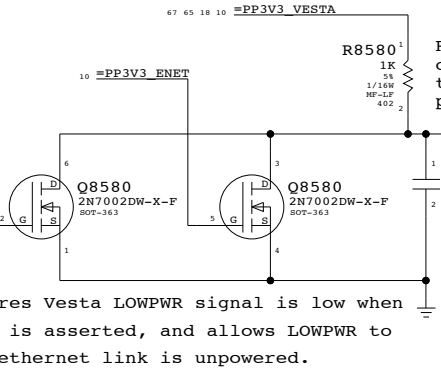
Net Spacing Type: ENET_MDI

Line to Line: 0.38 mms
 Length Tolerance: 50 mils
 Primary Max Sep: 5 mils
 Secondary Max Sep: 100 mils
 Secondary Length: 500 mils

NOTE: Target differential impedance for ENET data pairs is 100 ohms.

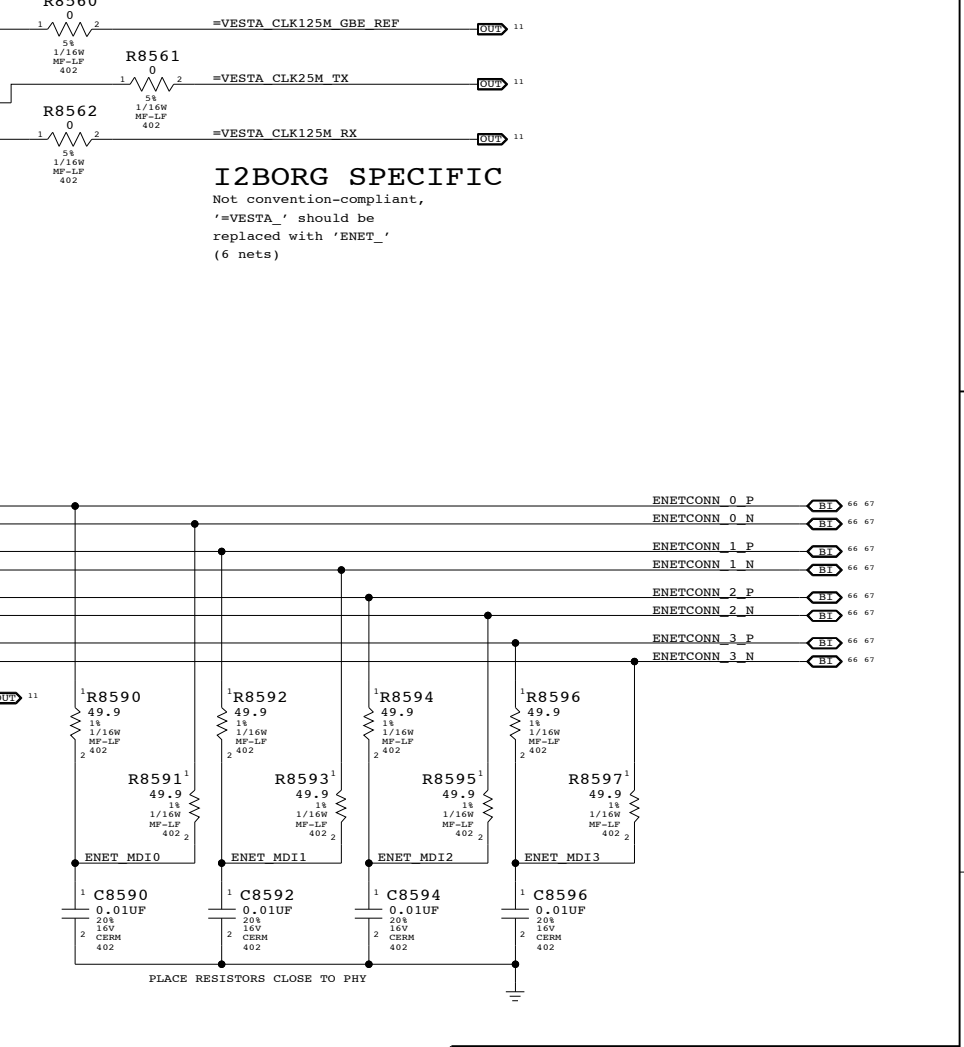
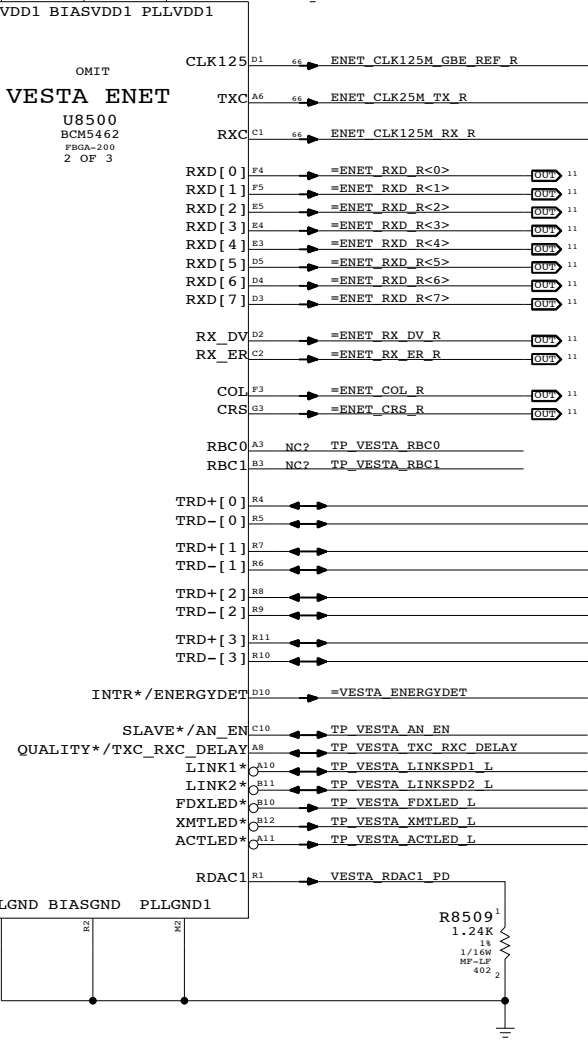
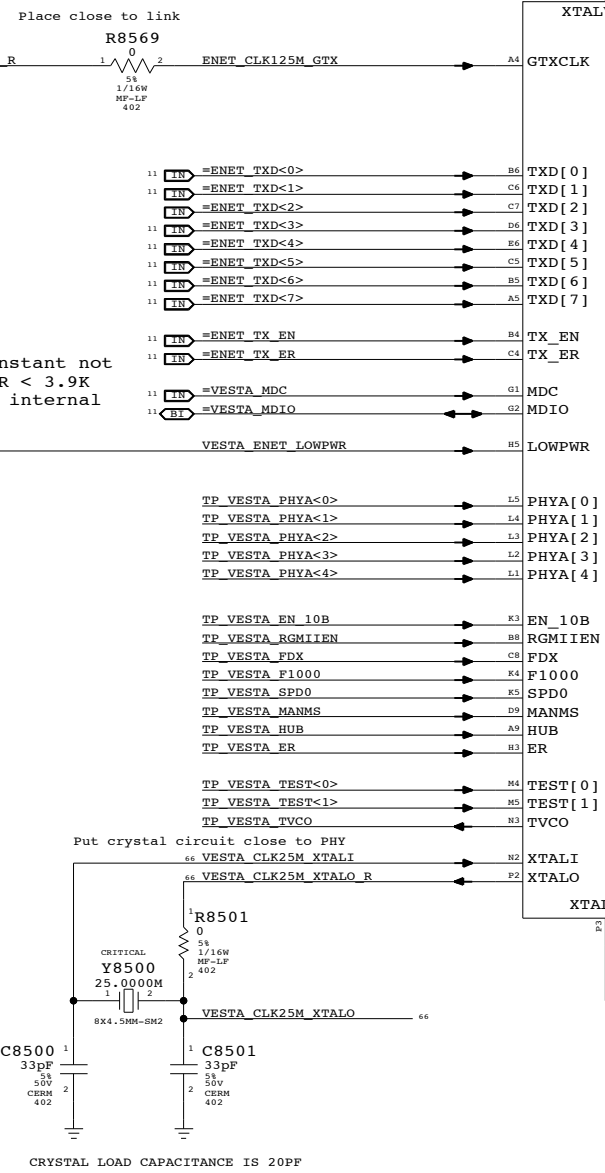
Vesta Ethernet LowPwr

Disables Vesta Ethernet Circuit



Vesta Config Straps:

PHYA<4..0> - PHY Address Select (Internal Pull-downs)	MANMS - Manual Master/Slave Configuration Select (Internal Pull-down)	EN_10B - TBI Interface Select (Internal Pull-down)	HUB - Repeater Select (Internal Pull-down)	RGMIEN - RGMI Enable (Internal Pull-down)	ER - Edge Rate Select (Internal Pull-down)	FDX - Full-Duplex Select (Internal Pull-up)	AN_EN - Auto-Negotiation Select (Internal Pull-up)	F1000 - Speed Select (Internal Pull-up)	TXC_RXC_DELAY (Internal Pull-up)	SPD0 - Speed Select (Internal Pull-down)	AN_EN F1000 SPD0 Description
0 - GMII/RGMII Mode	Sets manual master/slave configuration enable bit	1 - TBI/RTBI Mode	Sets Hub/DTE bit and master/slave configuration value bit	0 - GMII/TBI Mode	1 - Rise time approx. 5 ns	0 - Auto-negotiation enabled	1 - Auto-negotiation enabled	See table below	1 - If RGMII Mode enabled, RxC clock and GTXCLK are delayed by 1.9 ns	0 - No clock delay	0 0 0 Force 10BASE-T
0 - GMII/TBI Mode	(Internal Pull-down)	0 - GMII/RTBI Mode	(Internal Pull-down)	1 - RGMII/TBI Mode	0 - Rise time approx. 4 ns	0 - Auto-negotiation disabled	0 - Auto-negotiation disabled	See table below	(Internal Pull-down)	1 - Auto-negotiate advertise 10BASE-T	0 0 1 Force 100BASE-TX
1 - RGMII/TBI Mode	(Internal Pull-down)	1 - RGMII/TBI Mode	(Internal Pull-down)	0 - GMII/TBI Mode	(Internal Pull-down)	1 - Auto-negotiation enabled	1 - Auto-negotiation enabled	See table below	(Internal Pull-up)	1 0 1 Auto-negotiate advertise 10/100BASE-TX	0 1 X Force 1000BASE-T (test use only)
0 - GMII/TBI Mode	(Internal Pull-down)	0 - GMII/TBI Mode	(Internal Pull-down)	1 - RGMII/TBI Mode	(Internal Pull-down)	0 - Auto-negotiation disabled	0 - Auto-negotiation disabled	See table below	(Internal Pull-up)	1 1 0 Auto-negotiate advertise 10/100/1000BASE-T	1 0 0 Auto-negotiate advertise 10BASE-T
1 - RGMII/TBI Mode	(Internal Pull-down)	1 - RGMII/TBI Mode	(Internal Pull-down)	0 - GMII/TBI Mode	(Internal Pull-down)	1 - Auto-negotiation enabled	1 - Auto-negotiation enabled	See table below	(Internal Pull-up)	1 1 1 Auto-negotiate advertise 10/100/1000BASE-T	1 1 0 Auto-negotiate advertise 10/100BASE-T
0 - GMII/TBI Mode	(Internal Pull-down)	0 - GMII/TBI Mode	(Internal Pull-down)	1 - RGMII/TBI Mode	(Internal Pull-down)	0 - Auto-negotiation disabled	0 - Auto-negotiation disabled	See table below	(Internal Pull-up)	1 1 1 Auto-negotiate advertise 1000BASE-T	1 1 1 Auto-negotiate advertise 1000BASE-T



Vesta Ethernet PHY

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE	SHT	OF
NONE	85	115

APPLE COMPUTER INC.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
R243	ENETCONN	ENETCONN	ENET_RJ45_0	ENETRJ45_0_P
R244	ENETCONN	ENETCONN	ENET_RJ45_0	ENETRJ45_0_N
R245	ENETCONN	ENETCONN	ENET_RJ45_1	ENETRJ45_1_P
R246	ENETCONN	ENETCONN	ENET_RJ45_1	ENETRJ45_1_N
R247	ENETCONN	ENETCONN	ENET_RJ45_2	ENETRJ45_2_P
R248	ENETCONN	ENETCONN	ENET_RJ45_2	ENETRJ45_2_N
R249	ENETCONN	ENETCONN	ENET_RJ45_3	ENETRJ45_3_P
R250	ENETCONN	ENETCONN	ENET_RJ45_3	ENETRJ45_3_N

Page Notes

Power aliases required by this page:
 - _PP2V5_ENET
 - _GND_CHASSIS_ENET

Signal aliases required by this page:
 (NONE)

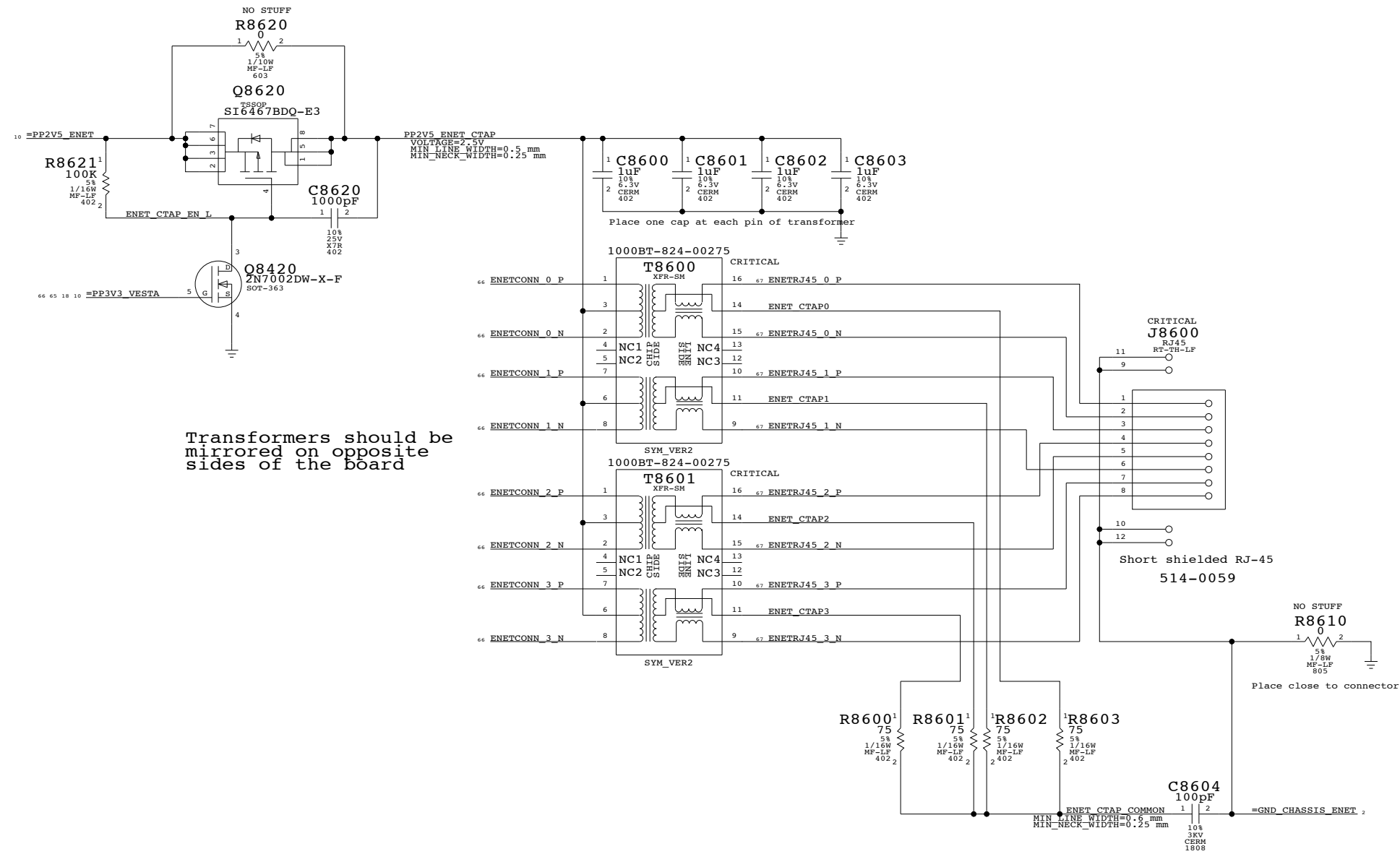
BOM options provided by this page:
 (NONE)

Ethernet routing priority:
 1. Decoupling caps
 2. TX SERIES TERMINATION - LOCATE NEAR LINK
 3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds



Transformers should be mirrored on opposite sides of the board

Ethernet Connector			
SYNC_MASTER=N/A		SYNC_DATE=N/A	
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	D	051-6839	E
SCALE	SHT	OF	REV.
NONE	86	115	

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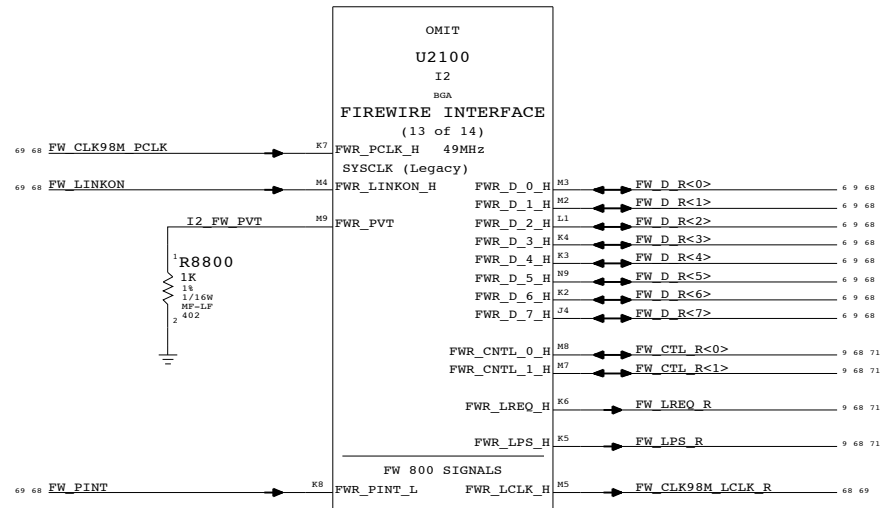
ELECTRICAL_CONSTRAINT_SET	NET_TYPE				
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR		
FW_D	FW	FW		FW_D_R<7..0>	6 9 68
FW_CTL	FW	FW		FW_CTL_R<1..0>	9 68 71
FW_LREQ	FW	FW		FW_LREQ_R	9 68 71
	FW	FW		FW_LPS_R	9 68 71
	FW	FW		FW_LINKON	68 69
FW_CLK	CLOCK	CLOCK		FW_CLK98M_PCLK	68 69
FW_LCLK	CLOCK	CLOCK		FW_CLK98M_LCLK_R	68 69
FW_PINT	FW	FW		FW_PINT	68 69

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



I2 FireWire Interface

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6839	E
SCALE	SHT OF		
NONE	88 OF		115

8

7

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1

ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
PROVIDED BY LINK PAGE	CLOCK	CLOCK	
FW_CLK98M_PCLK_R	CLOCK	CLOCK	
FW_CLK98M_LCLK	CLOCK	CLOCK	
FW_TPA0	FW_TP	FW_TP	FW_TPA0
FW_TPA0	FW_TP	FW_TP	FW_TPA0
FW_TPA0	FW_TP	FW_TP	FW_TPA0
FW_TPB0	FW_TP	FW_TP	FW_TPB0
FW_TPB0	FW_TP	FW_TP	FW_TPB0
FW_TPB0	FW_TP	FW_TP	FW_TPB0
FW_TPA1	FW_TP	FW_TP	FW_TPA1
FW_TPA1	FW_TP	FW_TP	FW_TPA1
FW_TPA1	FW_TP	FW_TP	FW_TPA1
FW_TPB1	FW_TP	FW_TP	FW_TPB1
FW_TPB1	FW_TP	FW_TP	FW_TPB1
FW_TPB1	FW_TP	FW_TP	FW_TPB1
FW_TPA2	FW_TP	FW_TP	FW_TPA2
FW_TPA2	FW_TP	FW_TP	FW_TPA2
FW_TPA2	FW_TP	FW_TP	FW_TPA2
FW_TPB2	FW_TP	FW_TP	FW_TPB2
FW_TPB2	FW_TP	FW_TP	FW_TPB2
FW_TPB2	FW_TP	FW_TP	FW_TPB2
VESTA_CLK24M_XTALI	XTAL	XTAL	VESTA_CLK24M_XTALI
VESTA_CLK24M_XTALO	XTAL	XTAL	VESTA_CLK24M_XTALO
VESTA_CLK24M_XTALO_R	XTAL	XTAL	VESTA_CLK24M_XTALO_R

Page Notes

Power aliases required by this page:
 - =PPFW_PHY_CPS
 - =PP3V3_FW
 - =PP3V3_ENETFW
 - =PP2V5_ENETFW
 - =PP1V2_ENETFW

Signal aliases required by this page:
 - NONE

BOM options provided by this page:
 - VESTA_BILINGUAL_EN12
 If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.
 - VESTA_DS_ONLY_EN0
 If stuffed, adds external pull-up to counter internal pull-down in Vesta. See straps table for more information.
 - VESTA_PORT1_DISABLE
 If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.
 - VESTA_PORT2_DISABLE
 If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.
 - VESTA_PWR_CLASS_0
 If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.

Net Spacing Type: FW_TP

Line to Line: 0.38 mms
 Length Tolerance: 100 mils
 Primary Max Sep: 7.5 mils
 Secondary Max Sep: 100 mils
 Secondary Length: 500 mils

NOTE: Target differential impedance for FW data pairs is 110 ohms.

Vesta Config Straps:

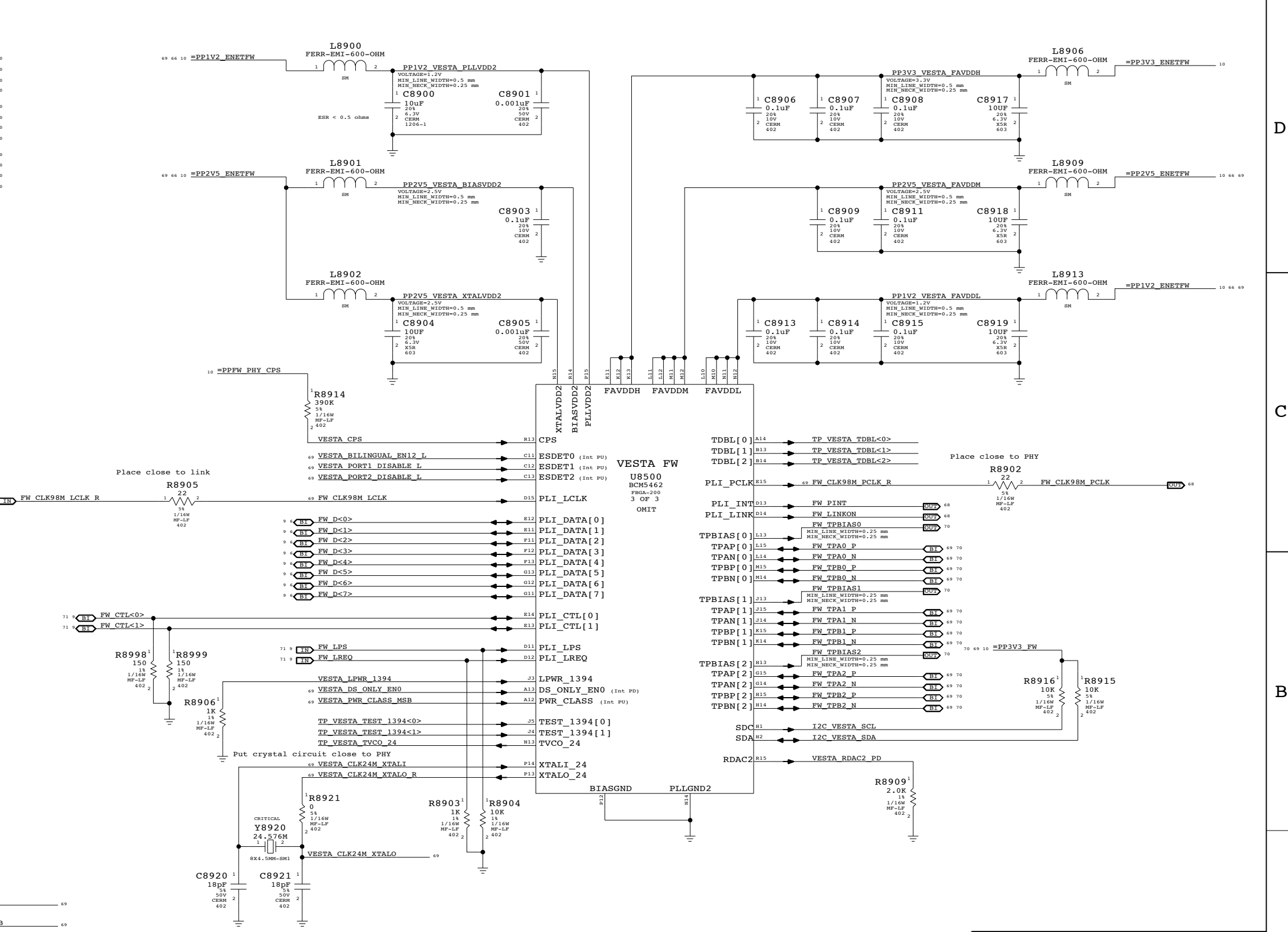
DS_ONLY_EN12 - Port 1&2 Data/Strobe
 1 - Port 1&2 Data/Strobe mode only
 0 - Port 1&2 Bilingual mode
 (Internal Pull-up)

DS_ONLY_EN0 - Port 0 Data/Strobe
 1 - Port 0 Data/Strobe mode only
 0 - Port 0 Bilingual mode
 (Internal Pull-down)

PORT1_ENABLE - Port 1 Enable
 1 - Port 1 Enabled
 0 - Port 1 Disabled (saves power)
 (Internal Pull-up)

PORT2_ENABLE - Port 2 Enable
 1 - Port 2 Enabled
 0 - Port 2 Disabled (saves power)
 (Internal Pull-up)

PWR_CLASS - FireWire Power Class
 1 - Sets Power Class to 0x4
 0 - Sets Power Class to 0x0
 (Internal Pull-up)



Vesta FireWire PHY
 SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6839	E
SCALE	SHT	OF
NONE	89	115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
PROVIDED	FW	FW	FW_PORT1_TPA_P_FL
BY	FW	FW	FW_PORT1_TPA_N_FL
PHY	FW	FW	FW_PORT1_TPB_FL
PAGE	FW	FW	FW_PORT1_TPB_N_FL
	FW	FW	FW_PORT2_TPA_P_FL
	FW	FW	FW_PORT2_TPA_N_FL
	FW	FW	FW_PORT2_TPB_FL
	FW	FW	FW_PORT2_TPB_N_FL

Page Notes

Power aliases required by this page:
 - PPFW_PORT1
 - PPFW_PORT2
 - PPFW_PORT3
 - PP3V3_FW
 - GND_CHASSIS_FW_PORT1
 - GND_CHASSIS_FW_PORT2
 - GND_CHASSIS_FW_PORT3

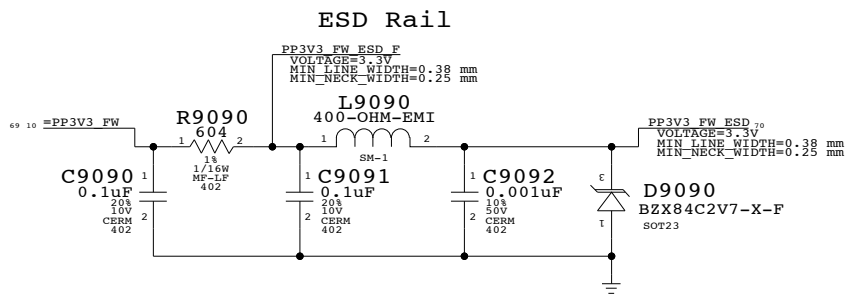
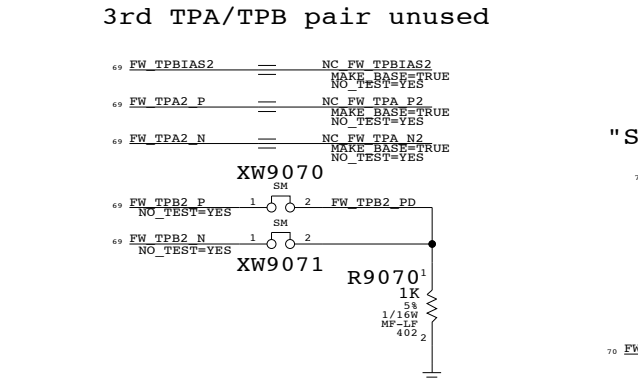
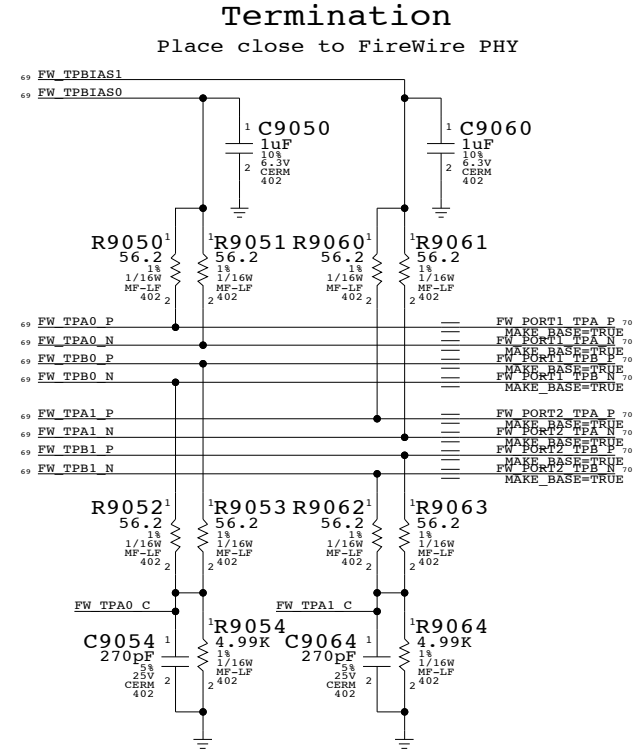
Signal aliases required by this page:
 (NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

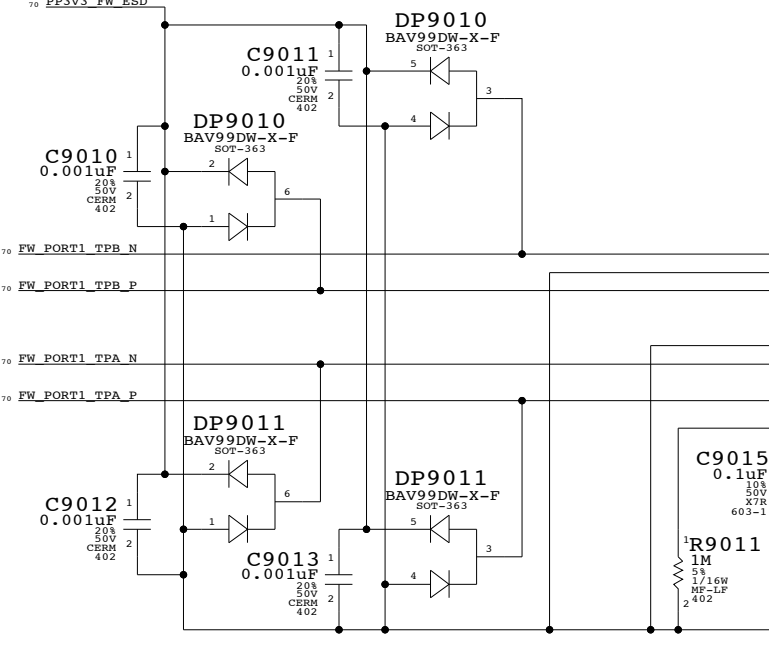
BOM options provided by this page:
 (NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

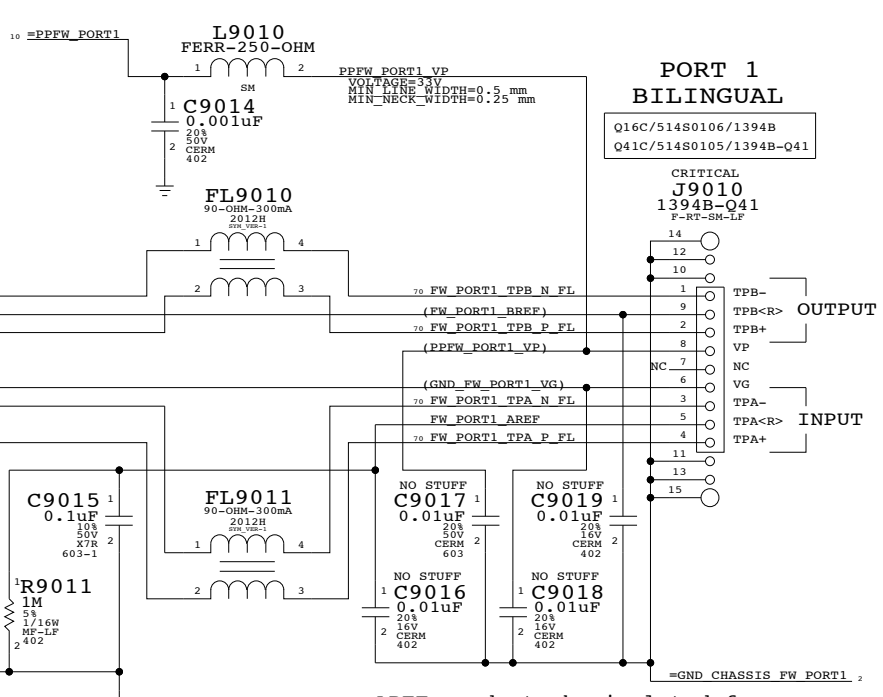
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)



"Snapback" & "Late VG" Protection



Cable Power

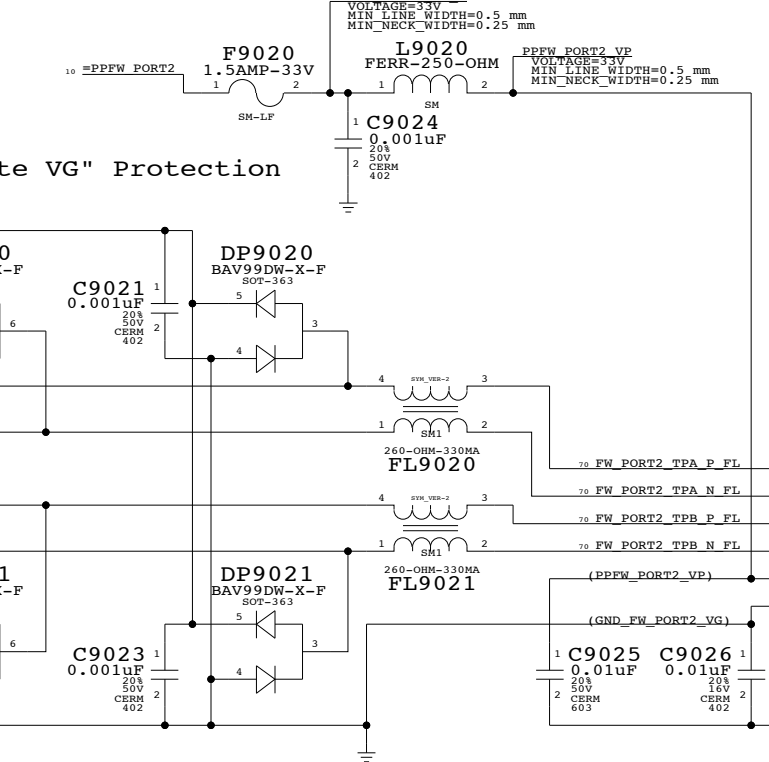


AREF needs to be isolated from all local grounds per 1394b spec

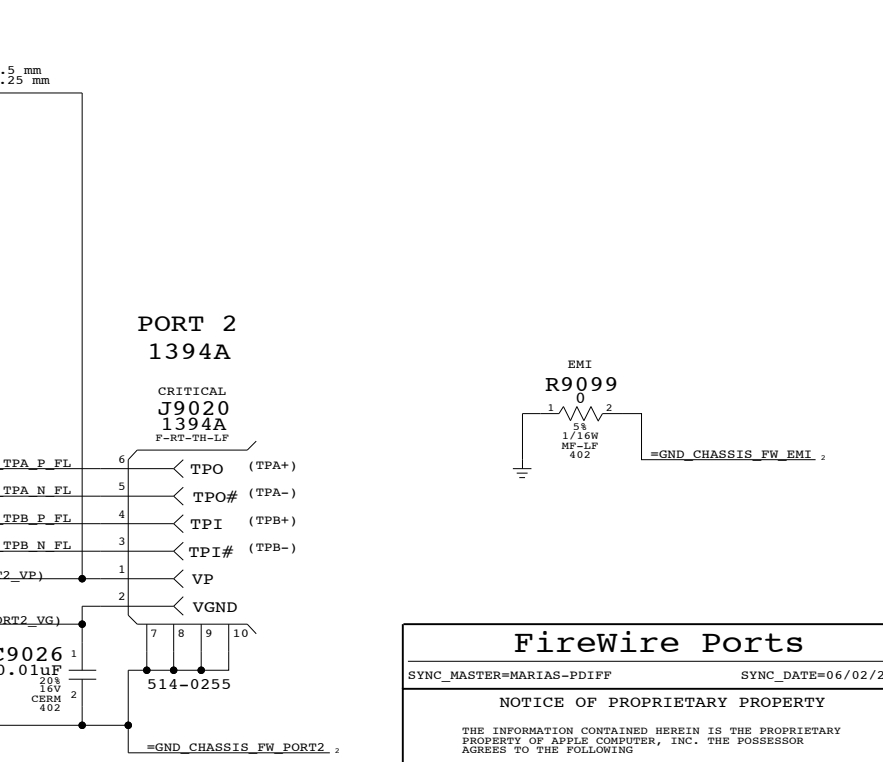
When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

"Snapback" & "Late VG" Protection



Cable Power



FireWire Ports

SYNC_MASTER=MARIAS-PDIFF SYNC_DATE=06/02/2005

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D	051-6839	E
SCALE	SHT	OF
NONE	90	115

8

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D

D

C

C

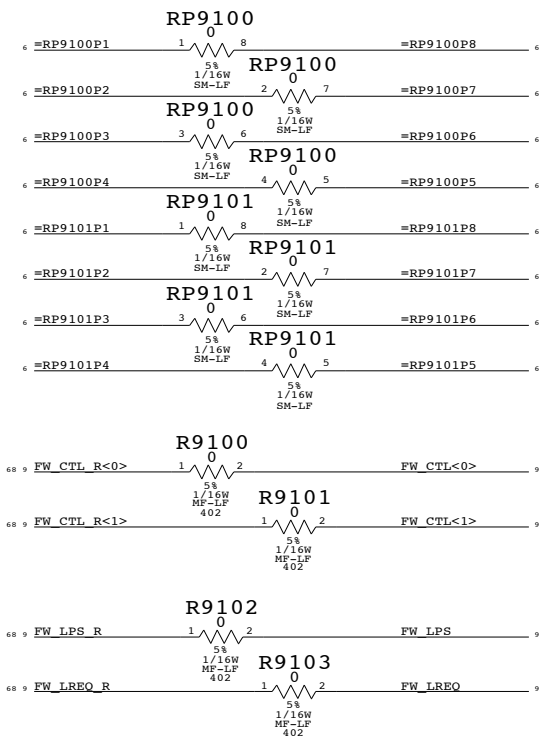
B

B

A

A

Place series terminators approximately halfway between Vesta and NB.
(They should probably be slightly closer to Vesta than the NB.)



FireWire Series Term

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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	D	051-6839	E
SCALE	SHT	OF	
NONE	91	115	

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
USB2_0	USB2	USB2	USB2	USB2_I2_P<0>	11 72
				USB2_I2_N<0>	11 72
USB2_1	USB2	USB2	USB2	USB2_I2_P<1>	6 72
				USB2_I2_N<1>	6 72
USB2_2	USB2	USB2	USB2	USB2_I2_P<2>	11 72
				USB2_I2_N<2>	11 72
USB2_3	USB2	USB2	USB2	USB2_I2_P<3>	6 72
				USB2_I2_N<3>	6 72
USB2_4	USB2	USB2	USB2	USB2_I2_P<4>	11 72
				USB2_I2_N<4>	11 72
USB2_5	USB2	USB2	USB2	USB2_I2_P<5>	11 72
				USB2_I2_N<5>	11 72
USB2_I2_XTAL	XTAL	XTAL		I2_CLK30M_USB2_XOUT_R	72
(USB2_I2_XTAL)	XTAL	XTAL		I2_CLK30M_USB2_XOUT	72
(USB2_I2_XTAL)	XTAL	XTAL		I2_CLK30M_USB2_XIN	72

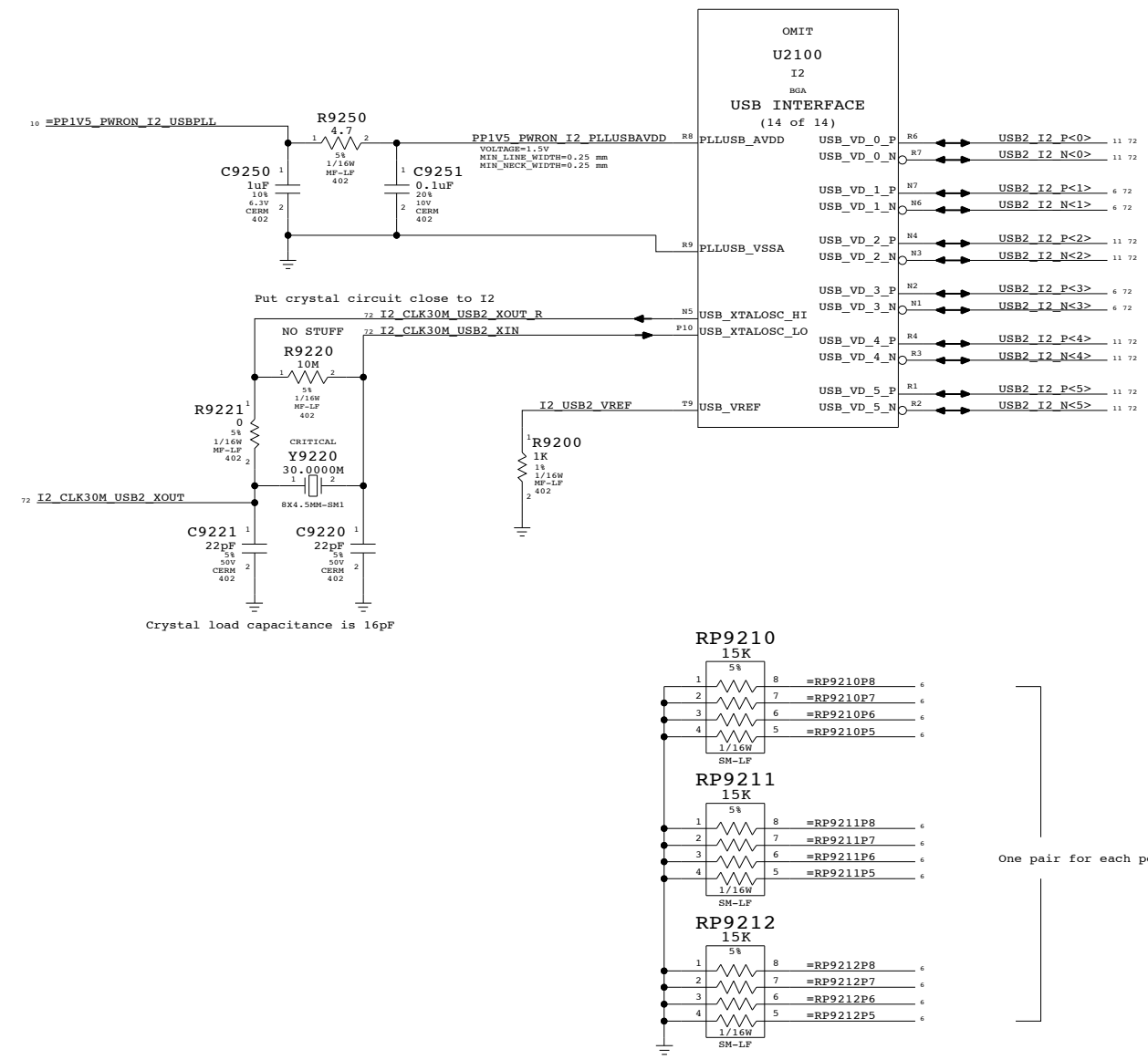
Page Notes

Power aliases required by this page:
 - =PP3V3_PWRON_USB
 Signal aliases required by this page:
 - =RP92xxPy (pinswappable USB pulldowns)
 BOM options provided by this page:
 (NONE)

Net Spacing Type: USB2

Line To Line: 19.5 mils
 Length Tolerance: 50 mils
 Primary Max Sep: 7.5 mils
 Secondary Max Sep: 100 mils
 Secondary Length: 500 mils

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.



I2 USB Interface

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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	D	051-6839	E
SCALE	SHT	OF	REV.
NONE	92	115	

ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
E30	USB2	USB2	USB2_NEC_0
E31	USB2	USB2	USB2_NEC_0
E32	USB2	USB2	USB2_NEC_1
E33	USB2	USB2	USB2_NEC_1
E34	USB2	USB2	USB2_NEC_2
E35	USB2	USB2	USB2_NEC_2
E36	USB2	USB2	USB2_NEC_3
E37	USB2	USB2	USB2_NEC_3

NET_TYPE	NET	TYPE	PAIR
USB2_NEC	USB2_NEC_P<0>		
USB2_NEC	USB2_NEC_N<0>		
USB2_NEC	USB2_NEC_P<1>		
USB2_NEC	USB2_NEC_N<1>		
USB2_NEC	USB2_NEC_P<2>		
USB2_NEC	USB2_NEC_N<2>		
USB2_NEC	USB2_NEC_P<3>		
USB2_NEC	USB2_NEC_N<3>		

Page Notes

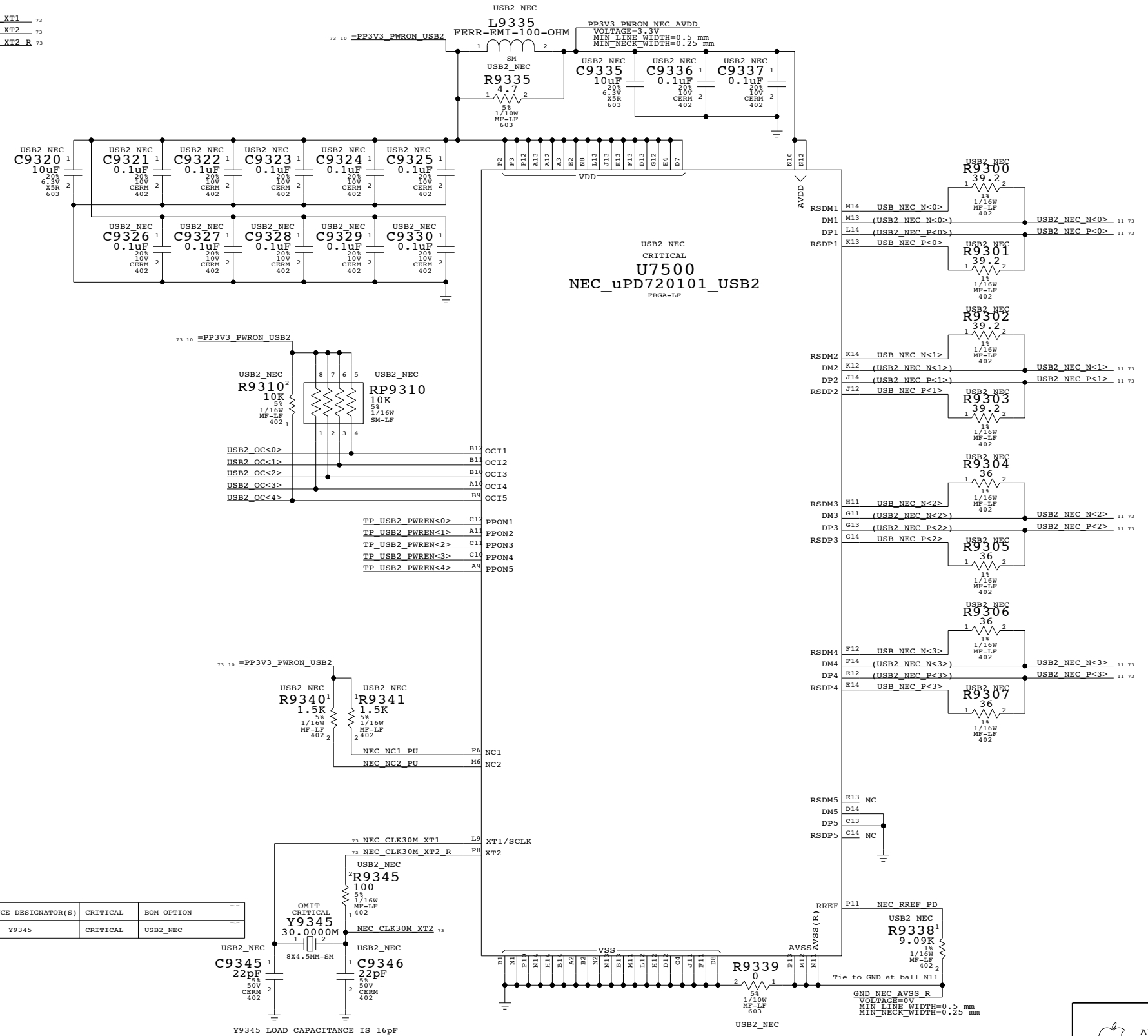
Power aliases required by this page:
 - =PP3V3_PWRON_USB2

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 USB2_NEC

Net Spacing Type: USB2

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
19750087	1	XTAL,CER,10.0000MHZ,LW PROF,8X4.5MM,SMD	Y9345	CRITICAL	USB2_NEC

NEC USB2 Interface

SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005

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SCALE	SHT	OF	
NONE	93	115	

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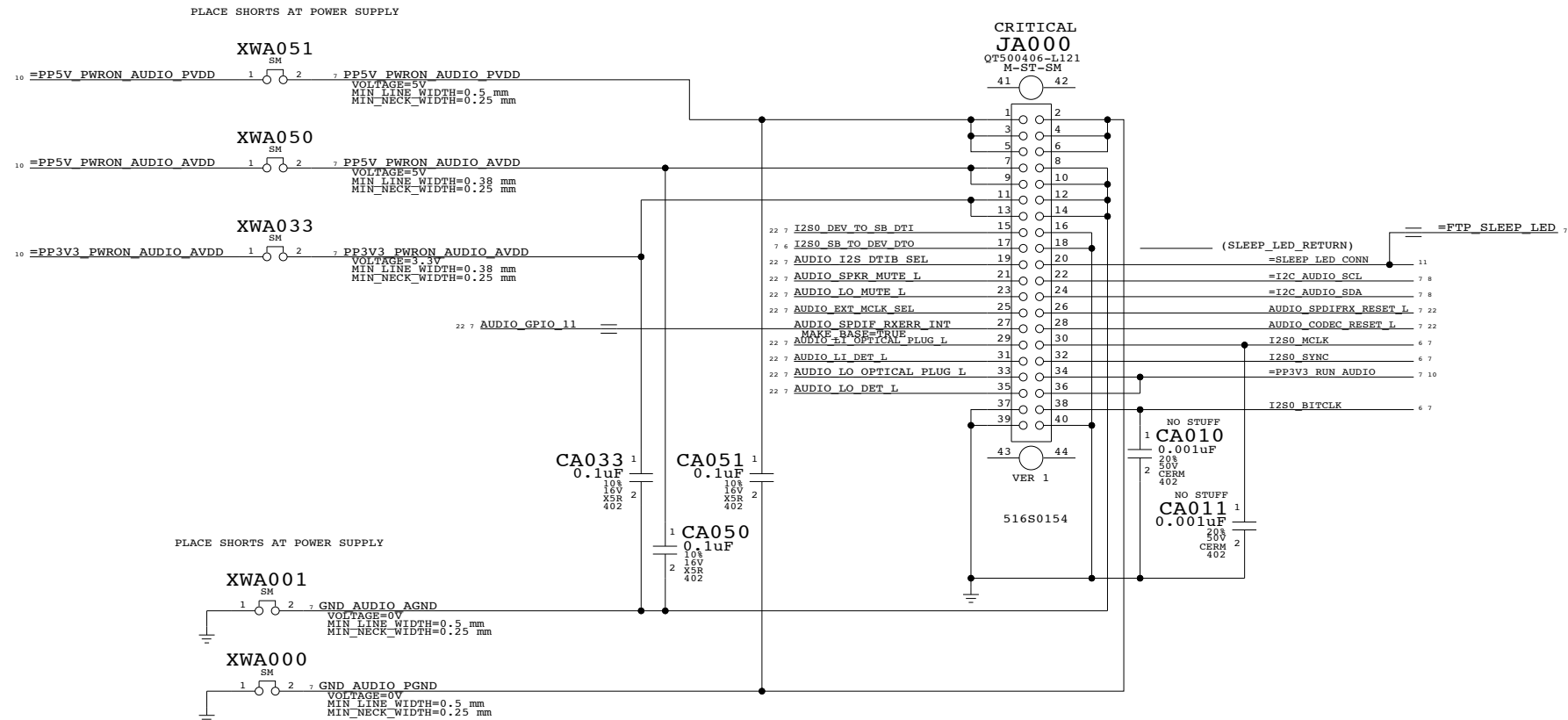
B

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AUDIO BOARD CONNECTOR

Place all shorts at output of 3.3V and 5V regulator



Audio Board Connector

SYNC_MASTER=N/A SYNC_DATE=N/A

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SCALE	SHT OF		
NONE	100		115

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D	AGP TABLE_SPACING_RULE TABLE_SPACING_RULE AGP 401 * 0.4 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_SPACING_RULE AGP_STB 601 * 0.6 MM 2.5 MM =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE AGP * =STANDARD =60_OHM_SE =60_OHM_SE =60_OHM_SE TABLE_PHYSICAL_RULE AGP_STB * =STANDARD =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF						AUDIO TABLE_SPACING_RULE TABLE_SPACING_RULE AUDIO 251 * 0.25 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE AUDIO * =50_OHM_SE =50_OHM_SE =50_OHM_SE =50_OHM_SE			D																			
	CLOCK TABLE_SPACING_RULE TABLE_SPACING_RULE CLOCK 251 * 0.25 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE CLOCK * =STANDARD =50_OHM_SE =50_OHM_SE =50_OHM_SE						I2S TABLE_SPACING_RULE TABLE_SPACING_RULE I2S 251 * 0.25 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE I2S * =50_OHM_SE =50_OHM_SE =50_OHM_SE =50_OHM_SE				D																		
	ENET (Ethernet Digital) TABLE_SPACING_RULE TABLE_SPACING_RULE ENET_SELF =STANDARD * =STANDARD =STANDARD =STANDARD =STANDARD =STANDARD TABLE_SPACING_RULE ENET 201 * 0.2 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE ENET * =STANDARD =50_OHM_SE =50_OHM_SE =50_OHM_SE						ENETCONN TABLE_SPACING_RULE TABLE_SPACING_RULE ENETCONN 501 * 0.50 MM 3.81 MM =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE ENETCONN * =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF					D																	
	FW (FireWire Digital) TABLE_SPACING_RULE TABLE_SPACING_RULE FW_SELF =STANDARD * =STANDARD =STANDARD =STANDARD =STANDARD =STANDARD TABLE_SPACING_RULE FW 201 * 0.2 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE FW * =STANDARD =50_OHM_SE =50_OHM_SE =50_OHM_SE						FW_TP TABLE_SPACING_RULE TABLE_SPACING_RULE FW_TP 501 * 0.50 MM 3.81 MM =110_OHM_DIFF =110_OHM_DIFF =110_OHM_DIFF TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE FW_TP * =110_OHM_DIFF =110_OHM_DIFF =110_OHM_DIFF =110_OHM_DIFF						D																
	I2C TABLE_SPACING_RULE TABLE_SPACING_RULE I2C 201 * 0.2 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE I2C * =STANDARD =50_OHM_SE =50_OHM_SE =50_OHM_SE						I2_FBCLK / XTAL TABLE_SPACING_ASSIGNMENT TABLE_SPACING_ASSIGNMENT I2_FBCLK * * CLOCK TABLE_SPACING_ASSIGNMENT XTAL * * CLOCK TABLE_PHYSICAL_ASSIGNMENT TABLE_PHYSICAL_ASSIGNMENT I2_FBCLK * * CLOCK TABLE_PHYSICAL_ASSIGNMENT XTAL * * CLOCK							D															
	MaxBus TABLE_SPACING_RULE TABLE_SPACING_RULE MAXBUS 151 * 0.15 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE MAXBUS * =STANDARD =50_OHM_SE =50_OHM_SE =50_OHM_SE														D														
	PCI TABLE_SPACING_RULE TABLE_SPACING_RULE PCI =STANDARD * =STANDARD =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE PCI * =STANDARD =50_OHM_SE =50_OHM_SE =50_OHM_SE															D													
	RAM TABLE_SPACING_RULE TABLE_SPACING_RULE RAM 201 * 0.2 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_SPACING_RULE RAM_DIFF 251 * 0.25 MM 2.5 MM =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE RAM * =50_OHM_SE =50_OHM_SE =50_OHM_SE =50_OHM_SE TABLE_PHYSICAL_RULE RAM_DIFF * =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF =100_OHM_DIFF																D												
	UATA TABLE_SPACING_RULE TABLE_SPACING_RULE UATA 151 * 0.15 MM =STANDARD =STANDARD =STANDARD =STANDARD TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE UATA * =50_OHM_SE =50_OHM_SE =50_OHM_SE =50_OHM_SE																	D											
	USB2 TABLE_SPACING_RULE TABLE_SPACING_RULE USB2 501 * 0.50 MM 3.81 MM =90_OHM_DIFF =90_OHM_DIFF =90_OHM_DIFF TABLE_PHYSICAL_RULE TABLE_PHYSICAL_RULE USB2 * =90_OHM_DIFF =90_OHM_DIFF =90_OHM_DIFF =90_OHM_DIFF																		D										
						Spacing & Physical Constraints SYNC_MASTER=MARIAS SYNC_DATE=08/24/2005 NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART			D																				
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						<table border="1"> <tr> <td>SIZE</td> <td>DRAWING NUMBER</td> <td>REV.</td> </tr> <tr> <td>D</td> <td>051-6839</td> <td>E</td> </tr> <tr> <td>SCALE</td> <td colspan="2">SHT OF</td> </tr> <tr> <td>NONE</td> <td colspan="2">110 OF 115</td> </tr> </table>					SIZE	DRAWING NUMBER								REV.	D	051-6839	E	SCALE	SHT OF		NONE	110 OF 115	
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TABLE_SPACING_RULE							
TABLE_SPACING_RULE	DVO	151	*	0.15 MM	=STANDARD	=STANDARD	=STANDARD
TABLE_PHYSICAL_RULE	DVO						=STANDARD
TABLE_PHYSICAL_RULE	DVO		*		=STANDARD	=50_OHM_SE	=50_OHM_SE
TABLE_SPACING_RULE							
TABLE_SPACING_RULE	TV	151	*	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE
TABLE_SPACING_RULE	TV_CONN	151	*	=TV	=TV	=TV	=TV
TABLE_PHYSICAL_RULE							=TV
TABLE_PHYSICAL_RULE	TV		*	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE
TABLE_PHYSICAL_RULE	TV_CONN		*	=TV	=TV	=TV	=TV
TABLE_SPACING_RULE							
TABLE_SPACING_RULE	VGA	151	*	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE
TABLE_SPACING_RULE	VGA_CONN	151	*	=VGA	=VGA	=VGA	=VGA
TABLE_PHYSICAL_RULE							=VGA
TABLE_PHYSICAL_RULE	VGA		*	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE
TABLE_PHYSICAL_RULE	VGA_CONN		*	=VGA	=VGA	=VGA	=VGA
TABLE_SPACING_RULE							
TABLE_SPACING_RULE	LVDS	151	*		=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TABLE_PHYSICAL_RULE	LVDS		*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TABLE_SPACING_RULE							
TABLE_SPACING_RULE	TMDS	251	*	0.25 MM	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TABLE_SPACING_RULE	TMDS_CONN	=TMDS	*	=TMDS	=TMDS	=TMDS	=TMDS
TABLE_PHYSICAL_RULE							=TMDS
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TABLE_PHYSICAL_RULE	TMDS_CONN		*	=TMDS	=TMDS	=TMDS	=TMDS
TABLE_SPACING_RULE							
TABLE_SPACING_RULE	THERM	251	*	0.25 MM	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TABLE_PHYSICAL_RULE	THERM		*	Y	0.25 MM	=100_OHM_DIFF	=100_OHM_DIFF

DVO

S-VIDEO

VGA

LVDS

TMDS

THERM

Spacing & Physical Constraints 2

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NONE	111	115	

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