1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
B		448475	PRODUCTION RELEASED	07/12/06	

SCHEM,MLB,PB17",SVC

07/12/2006

BOM OPTIONS	STUFF	NO STUFF
D3_HOT		✓
D3_COLD	✓	
GPU_SS	✓	
GPU_SWITCH	✓	
SERIAL_DEBUG		✓
VCORE_OFFSET	✓	
1_8V_MAXBUS	✓	
1_5V_MAXBUS		✓
NEC_USB	✓	
INTREPID_USB		✓
BBANG		✓
NO_BBANG	✓	
ATI_MEMIO_HI	✓	
ATI_MEMIO_LO		✓
SSCG		✓
NO_SSCG	✓	
5V_HD_LOGIC	✓	
3V_HD_LOGIC		✓
EXT_TMDS		✓
INT_TMDS	✓	
NO_4XVCORE	✓	
INT_CLK	✓	
EXT_CLK		✓

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-7202	1	SCHEM,MLB,PB17,SVC	SCH1	
820-1615	1	PCBF,MLB,PBG4 17	PCB1	
826-4393	1	LABEL,PCB,28MM X 6MM	EEE:WEY	LABEL_64MB
826-4393	1	LABEL,PCB,28MM X 6MM	EEE:WF1	LABEL_128MB

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES °
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

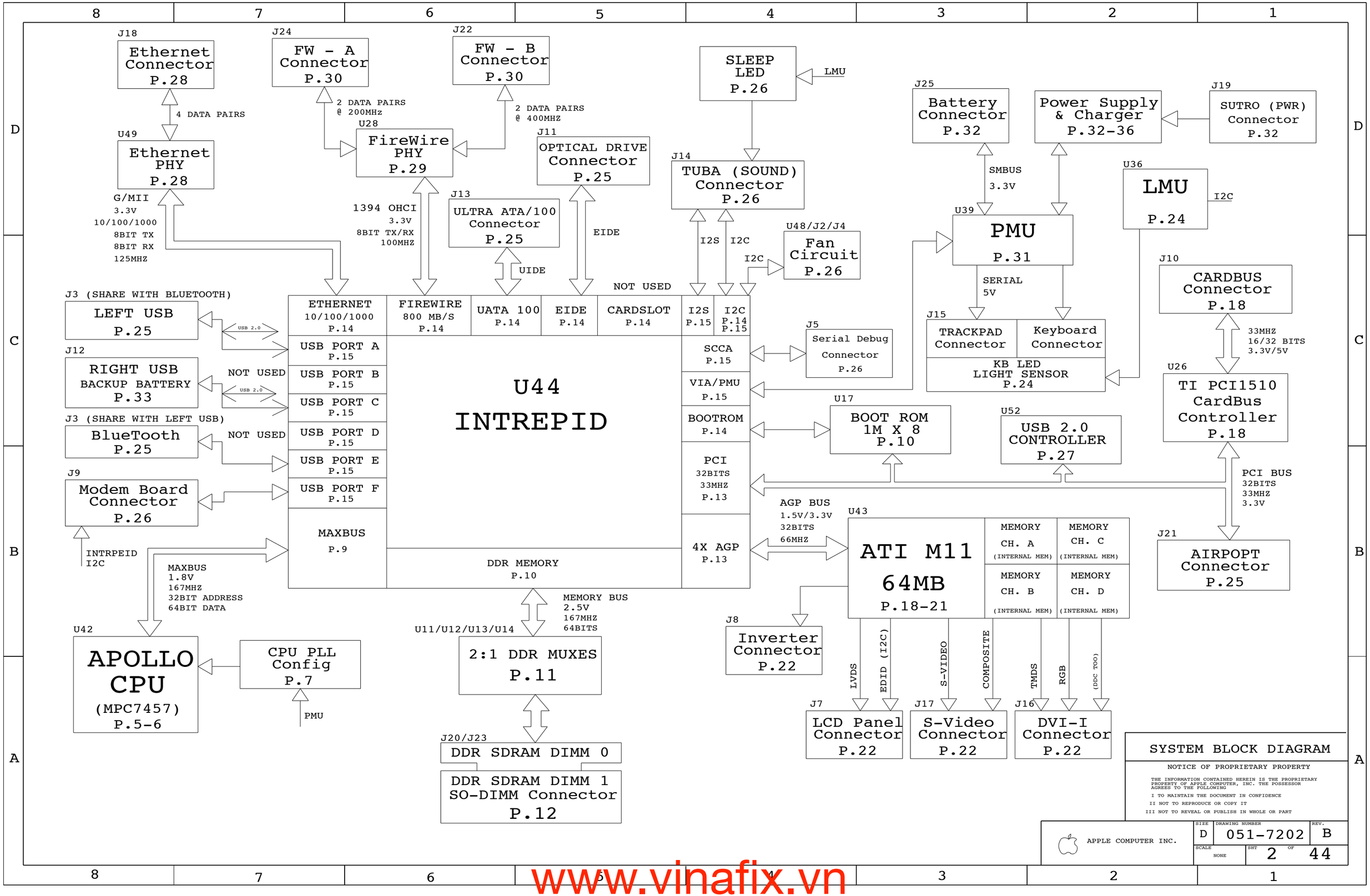
DRAFTER | DESIGN CK
ENG APPD | MFG APPD
QA APPD | DESIGNER
RELEASE | SCALE NONE
MATERIAL/FINISH NOTED AS APPLICABLE | SIZE D

Apple Computer Inc.

TITLE
SCHEM,MLB,PB17,SVC

DRAWING NUMBER 051-7202 | REV. B

SHT 1 OF 44



POWER SYSTEM ARCHITECTURE

AC ADAPTER IN PG 31

INRUSH LIMITER PG 30

+24V_PBUS

1V20_REF
U21 PG 31
>=13.44V TURNS-ON
<=13.44V SHUTS-OFF

RUN/SS
BUCK REGULATOR (LTC1625) PG 32
VCC
AC: 12.8V
NO AC: BATTERY VOLTAGE
1625 NOT RUNNING
SHUTDOWN: RUNNING
SLEEP: RUNNING
RUN: RUNNING

+PBUS (12.8V)

BACKLIGHT INVERTER

+5V_MAIN
VCC
MAIN 2.5V/1.5V DC/DC (MAX1715) PG 35
PGOOD
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING
TURNS ON OUTPUT @ 2.4V ON1/ON2

MAP31 DDR I/O
MAP31 DDR CORE
DDR POWER
+2.5V_MAIN
1_5V_2_5V_OK
+1.5V_MAIN
INTREPID CORE
AGP I/O

+PBUS

DCDC_EN
SLEEP
MAXBUS SEQUENCING

+5V_MAIN
VCC
SHDN
DC/DC (MAX1717) PG 34
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING
CPU_VCORE (+1.4V/+1.5V)

14V_PBUS

+3V_PMU LDO PG 32
+BATT
+5V_MAIN
+3V_PMU
+4_6V_BU

RC AT 1M*0.047UF @ 24V
STARTS 2.0MSEC AFTER DCDC_EN_L BECOMES LOW

RUN/SS - 5V
TURNS ON AT >1V
<100UA ALLOWED
INTERNAL ZENER CLAMP TO 6V
MAIN 3V/5V DC/DC (LTC3707) PG 33
VCC
PGOOD
STBYMD
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING
INTERNAL ZENER CLAMP TO 6V
<100UA ALLOWED
TURNS ON AT >1V
RUN/SS - 3V

+5V_MAIN
3V_5V_OK
HOLDS BOTH RUN/SS AT GND WHEN IT'S CONNECTED TO GND
TURNS CONTROL TO RUN/SS WHEN IT'S OPEN
+3.3V_MAIN

DCDC_EN_L
AFTER PMU IS UP AND RUNNING
DCDC_EN_L WILL PULL ON1/ON2 LOW IN SHUTDOWN

+5V_MAIN
+PBUS (12.8V)
EXT_VCC
VCC
DC/DC (LTC1778) PG 20
SHUTDOWN: STOPPED
SLEEP: D3HOT/D3COLD
RUN: RUNNING
TURNS ON AS LOW AS 0.8V/TYP 1.5V
INTERNAL 1.2UA CURRENT SOURCE
RUN/SS
GPU_VCORE +1.2V/+1.0V

DCDC_EN
SLEEP
D3_COLD
GPU_VCORE SEQUENCING
1M & 0.1UF @14V, IT TAKES ~5.88MS TO START SWITCHER
1_5V_2_5V_OK
D3_HOT
DCDC_EN_L
D3_HOT
1_5V_2_5V_OK WILL NOT PULL LOW UNTIL +5V_MAIN TURNS ON
HOWEVER, 5V SHOULD TURN ON ~2.23MS AFTER DCDC_EN_L OR PMU_POWERUP_L BECOMES '1'; MUCH LESS THAN THE RC CHARGING AT INT_VCC (5V)

+PBUS
BACKUP BATTERY
CHARGER INPUT & BOOST OUTPUT PG 32
12.8V CHARGES BACKUP BATTERY
24V IS OUTPUT ONLY FROM BACKUP BATTERY
BACKUP BATTERY CIRCUIT CHARGES OFF +PBUS AND PREVENTS +PBUS AND +24V_PBUS FROM DROPPING BELOW 6V (UNTIL DRAINED)

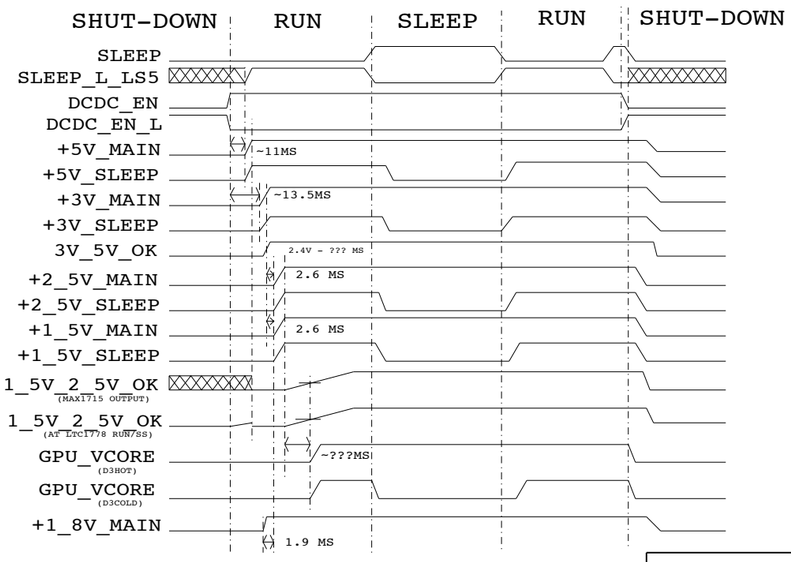
RC AT 1M*0.1UF @ 24V
STARTS ~4.25MSEC AFTER DCDC_EN_L BECOMES LOW
NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED
+24V_PBUS

DC/DC (LTC3411) PG 35
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING
+1.8V_MAIN
MAXBUS BROADCOM

BATTERY CHARGER (MAX1772) PG 31
+BATT

3S 3P PRISMATIC CELLS

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED
BATTERY VOLTAGE FEED-IN PATH PG 31
+PBUS



POWER BLOCK DIAGRAM

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-7202 | REV. B

SCALE NONE | SHT 3 OF 44

PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 12
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

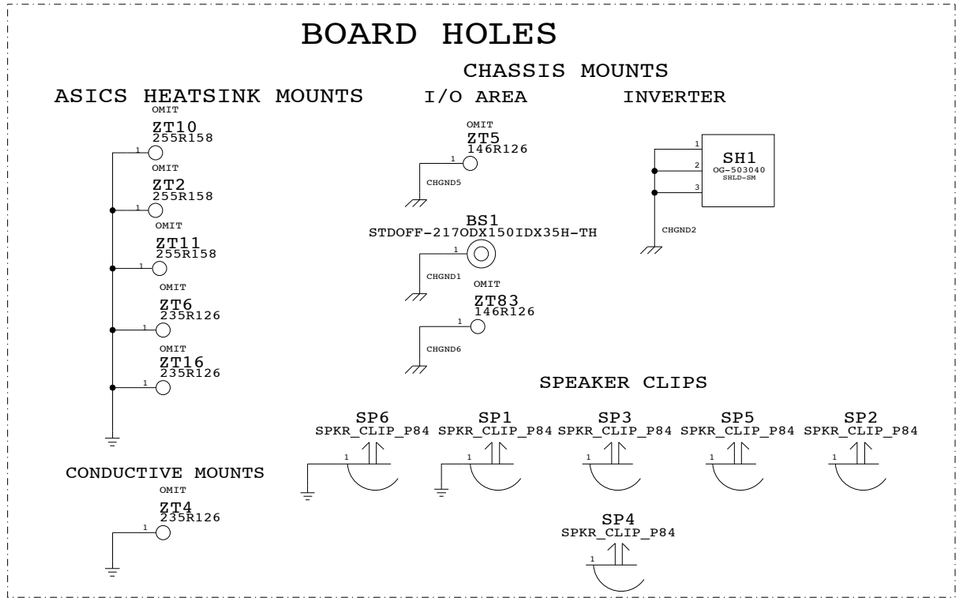
SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

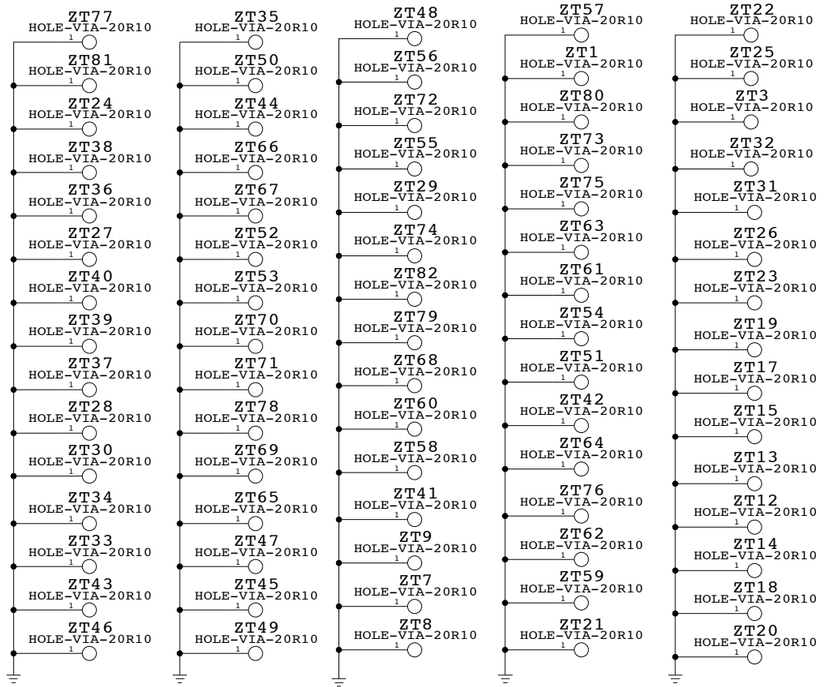
20R10 TH VIA OR VIA IN PAD

1		SIGNAL (1/3 OZ + COPPER PLATING)
2	PREPREG (3MIL)	GROUND (1/2 OZ)
3	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
4	PREPREG (3MIL)	SIGNAL (1/2 OZ)
5	LAMINATE (4MIL)	GROUND (1/2 OZ)
6	PREPREG (2MIL)	CUT POWER PLANE(1 OZ)
7	LAMINATE (3MIL)	CUT POWER PLANE(1 OZ)
8	PREPREG (2MIL)	GROUND (1/2 OZ)
9	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
10	PREPREG (3MIL)	SIGNAL (1/2 OZ)
11	LAMINATE (4MIL)	GROUND (1/2 OZ)
12	PREPREG (3MIL)	SIGNAL (1/3 OZ + COPPER PLATING)

BOARD HOLES



GROUND VIAS



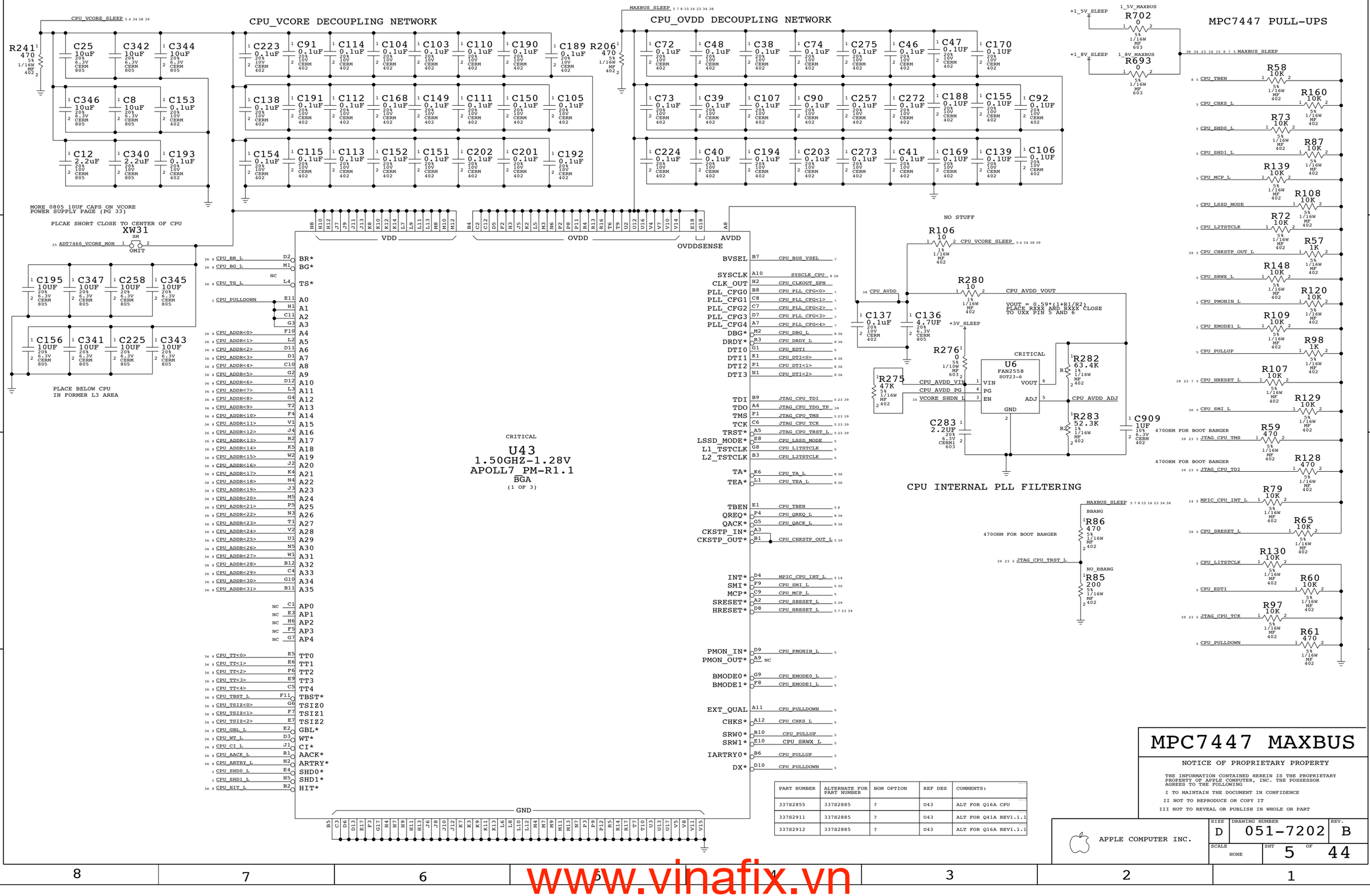
BOARD INFORMATION

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7202	B

SCALE: NONE

SHT 4 OF 44



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
337S2855	337S2885	?	U43	ALT FOR Q16A CPU
337S2911	337S2885	?	U43	ALT FOR Q41A REV1.1.1
337S2912	337S2885	?	U43	ALT FOR Q16A REV1.1.1

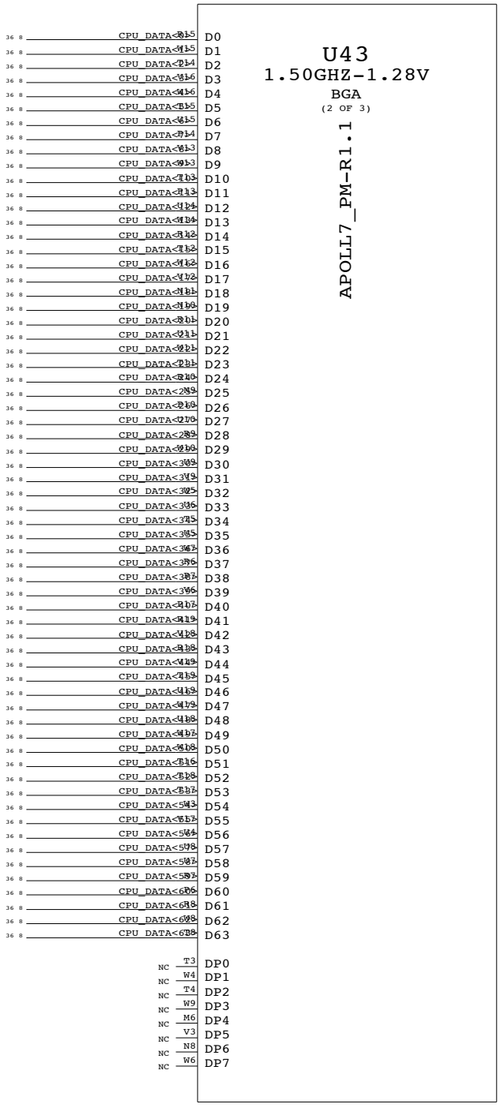
MPC7447 MAXBUS

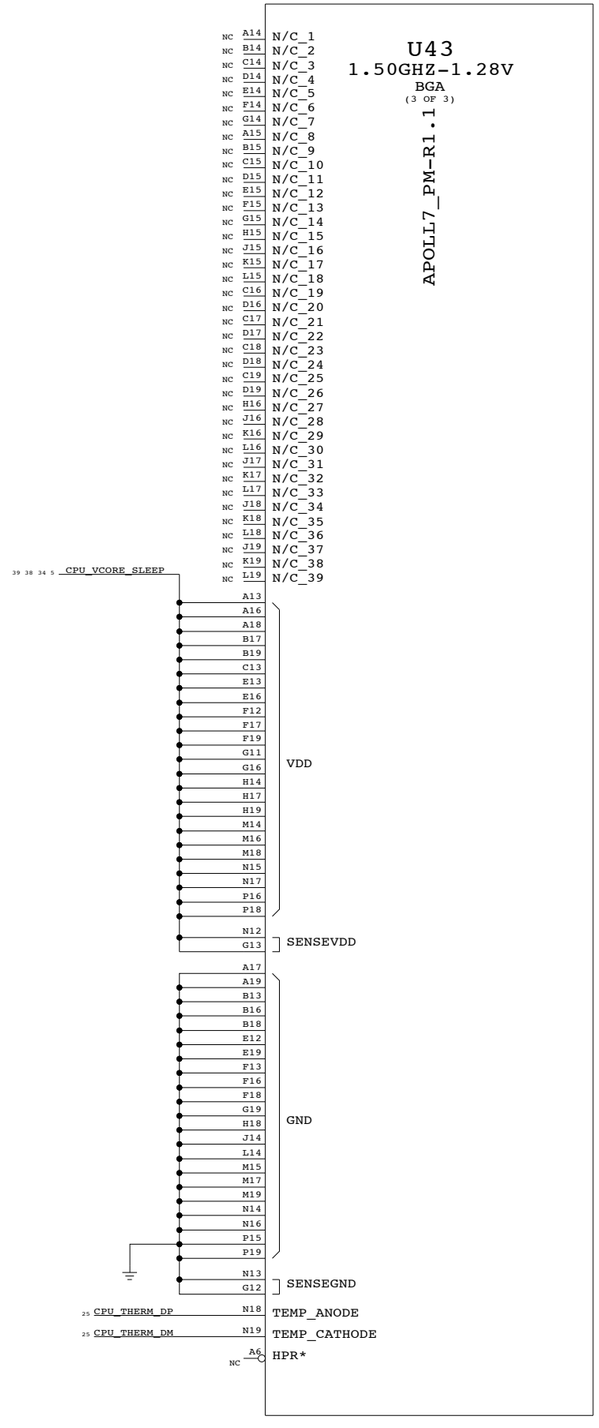
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7202	B

SCALE	SHT	OF
NONE	5	44

BOOT BANGER - LMU PERORMS THIS FUNCTION IF NEEDED
SEE PAGE 22





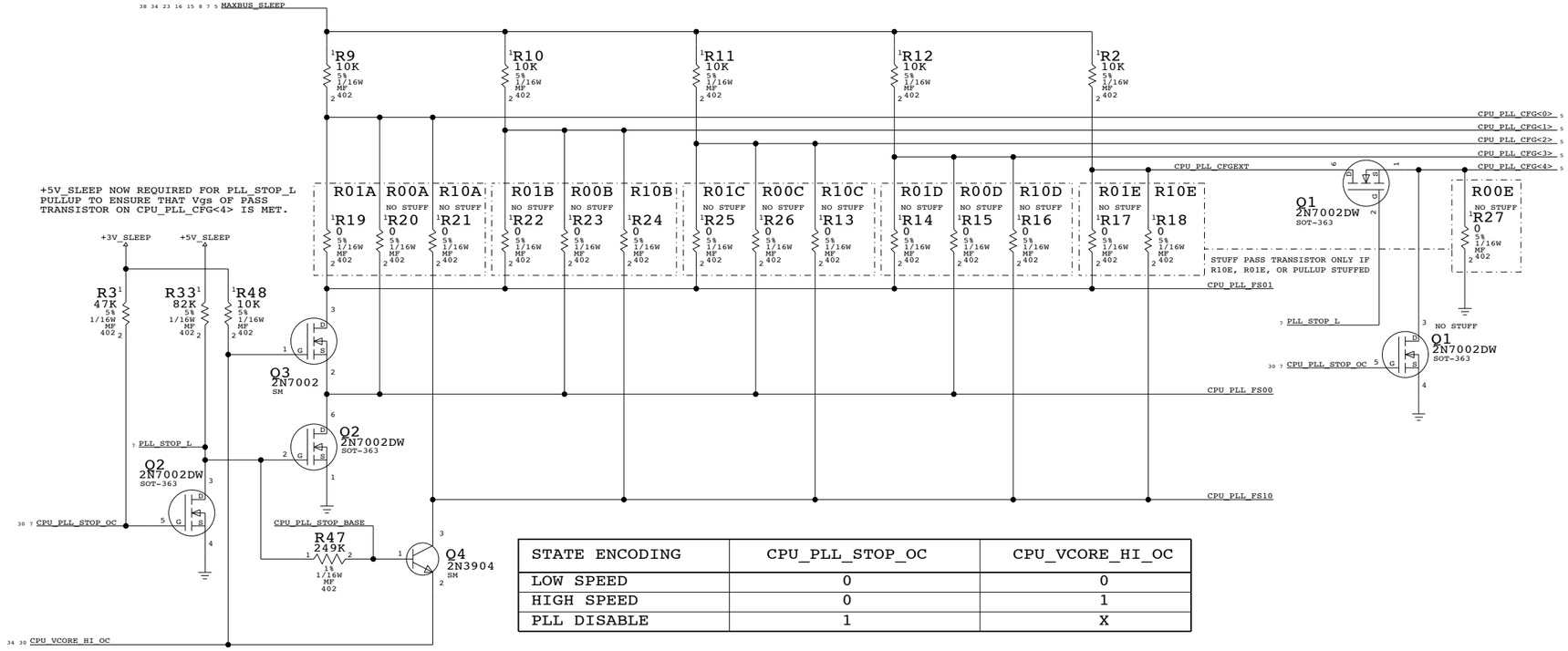
MPC7447/BBANG

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7202	B
SCALE: NONE	SHT 6 OF 44	

CPU PLL CONFIG CIRCUITRY



STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

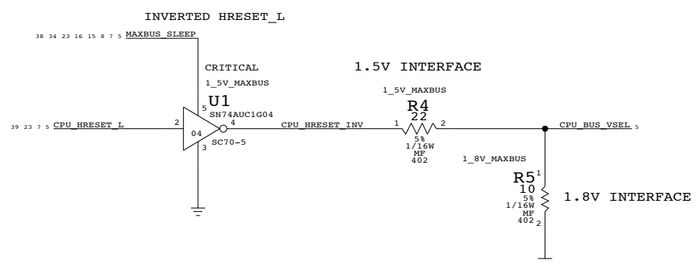
CPU FREQUENCY CONFIGURATION

APOLLO 7

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ (MHZ)	133MHZ (MHZ)	CPU_PLL_CFG 4 E	0123 ABCD	HEX
0.0X	PLL OFF		0	1111	0F
1.0X	PLL BYPASS		0	0011	03
2.0X	333	267	0	0100	04
3.0X	500	400	0	1000	08
4.0X	667	533	0	1010	0A
5.0X	833	667	0	1011	0B
5.5X	917	733	0	1001	09
6.0X	1000	800	0	1101	0D
6.5X	1083	867	0	0101	05
7.0X	1167	933	0	0010	02
7.5X	1250	1000	0	0001	01
8.0X	1333	1067	0	1100	0C
8.5X	1417	1133	0	0110	06
9.0X	1500	1200	1	0111	17
9.5X	1583	1267	0	0111	07
10.0X	1667	1333	1	1010	1A
10.5X	1750	1400	1	1000	18
11.0X	1833	1467	1	1001	19
11.5X	1917	1533	0	0000	00
12.0X	2000	1600	1	1011	1B
12.5X	2083	1667	1	1111	1F
13.0X	2167	1733	1	0101	15
13.5X	2250	1800	0	1110	0E
14.0X	2333	1867	1	1100	1C
15.0X	2500	2000	1	0001	11
16.0X	2667	2133	1	1101	1D
17.0X	2833	2267	1	0000	10
18.0X	3000	2400	1	0010	12
20.0X	3333	2667	1	0011	13
21.0X	3500	2800	1	0100	14
24.0X	4000	3200	1	0110	16
28.0X	4667	3733	1	1110	1E

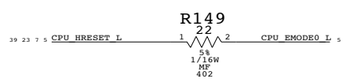
CPU CONFIGURATION

MAXBUS VSEL



DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L NEED TO CHARACTERIZE

BUSTYPE SELECT



APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

CPU CONFIGURATION

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7202	B
SCALE: NONE	SHT 7 OF 44	

INTREPID BOOT STRAPS

BIT 32 TO 39

38 34 23 16 15 8 7 5 MAXBUS_SLEEP

R642	R135	R123	R153	R166	R179	R651	R178
NO STUFF	NO STUFF	NO STUFF		NO STUFF	NO STUFF	NO STUFF	NO STUFF
10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402
36 8 6 CPU_DATA<32>	36 8 6 CPU_DATA<33>	36 8 6 CPU_DATA<34>	36 8 6 CPU_DATA<35>	36 8 6 CPU_DATA<36>	36 8 6 CPU_DATA<37>	36 8 6 CPU_DATA<38>	36 8 6 CPU_DATA<39>

R136	R643	R639	R657	R664	R673	R143	R674
10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	NO STUFF 10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402

0: Disable PWM interface (Default) 1: Enable PWM interface

Reserved. Must be 1

0: Disable Intel Flash Descriptor Override Strap 1: Enable Intel Flash Descriptor Override Strap

Spare

Spare

Spare

Spare

BIT 40 TO 47

38 34 23 16 15 8 7 5 MAXBUS_SLEEP

R122	R142	R164	R134	R184	R177	R152	R165
NO STUFF	NO STUFF	NO STUFF	EXT_CLK	NO STUFF	INT_CLK	INT_CLK	INT_CLK
10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402
36 8 6 CPU_DATA<40>	36 8 6 CPU_DATA<41>	36 8 6 CPU_DATA<42>	36 8 6 CPU_DATA<43>	36 8 6 CPU_DATA<44>	36 8 6 CPU_DATA<45>	36 8 6 CPU_DATA<46>	36 8 6 CPU_DATA<47>

R640	R652	R665	R644	R683	R675	R658	R666
10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	INT_CLK 10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	EXT_CLK 10K 5% 1/16W MF 402	EXT_CLK 10K 5% 1/16W MF 402	EXT_CLK 10K 5% 1/16W MF 402

Spare

Spare

BIT2 BIT1 BIT0

PLL4MODESEL_NXT[2:0]
000: 166.4MHZ (2.5X)
001: 149.76MHZ
010: 133.12MHZ (2.0X)
011: 99.84MHZ (1.5X)
100: 83.20MHZ

MODE A (2.5X) IS FOR STATIC OPERATION
MODE C (2.0X) IS FOR CLOCK SLEW OPERATION

0: Internal spreadEn 1: Active

10: PLL5 (NO SPREAD) 11: PLL4 (NO SPREAD) PCIE Source Clock

10: PLL5 (NO SPREAD) 11: PLL4 (NO SPREAD) PCIE Source Clock

BIT 48 TO 55

38 34 23 16 15 8 7 5 MAXBUS_SLEEP

R133	R121	R163	R151	R162	R141	R183	R176
EXT_CLK	EXT_CLK		NO STUFF	NO STUFF	NO STUFF		NO STUFF
10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402
36 8 6 CPU_DATA<48>	36 8 6 CPU_DATA<49>	36 8 6 CPU_DATA<50>	36 8 6 CPU_DATA<51>	36 8 6 CPU_DATA<52>	36 8 6 CPU_DATA<53>	36 8 6 CPU_DATA<54>	36 8 6 CPU_DATA<55>

R645	R641	R668	R659	R667	R653	R684	R676
INT_CLK	INT_CLK	NO STUFF				NO STUFF	
10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402

0: Buffer Ref Clock OutEnable_h 1: Active

0: Select48ExtSrc 1: External source

Spare

0: TI 1394b workaround 1: TI PHY workaround

BIT2 BIT1 BIT0

MaxBus output impedance
111: 28.6 ohm
011: 33.3 ohm
101: 40 ohm
001: 50 ohm
110: 66.6 ohm
010: 100 ohm
100: 200 ohm
000: 200 ohm

Spare

THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:

1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
2/ D46 - SELPCI1SPREADCLK - SLEEP/WAKE CYCLE REQUIRED
3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT

IF A STRAP IS NOT LISTED, THEN
IT CANNOT BE CHANGED BY SOFTWARE

38 14 12 +1_5V_INTREPID_PLL — R227 4.7 5% 1/16W MF 402 — 38 +1_5V_INTREPID_PLL7

C308 0.22UF 20% 6.3V CERM 402

H26 VDD15A_7 (PLL6) CRITICAL

U45 INTREPID-REV2.1 BGA

(1 OF 9)

36 8 5 CPU_BR_L	E29	BR	INPUT	
36 8 5 CPU_BG_L	E26	BG	NO BUS KEEPER	
36 8 5 CPU_TS_L	B27	TS	NO BUS KEEPER	
36 5 CPU_ADDR<0>	D24	A_0		
36 5 CPU_ADDR<1>	D25	A_1		
36 5 CPU_ADDR<2>	A27	A_2		
36 5 CPU_ADDR<3>	E24	A_3		
36 5 CPU_ADDR<4>	G23	A_4		
36 5 CPU_ADDR<5>	B26	A_5		
36 5 CPU_ADDR<6>	A26	A_6		
36 5 CPU_ADDR<7>	D23	A_7		
36 5 CPU_ADDR<8>	A25	A_8		
36 5 CPU_ADDR<9>	E23	A_9		
36 5 CPU_ADDR<10>	J22	A_10		
36 5 CPU_ADDR<11>	B25	A_11		
36 5 CPU_ADDR<12>	H22	A_12		
36 5 CPU_ADDR<13>	G22	A_13		
36 5 CPU_ADDR<14>	D22	A_14		
36 5 CPU_ADDR<15>	B24	A_15		
36 5 CPU_ADDR<16>	B23	A_16		
36 5 CPU_ADDR<17>	E22	A_17		
36 5 CPU_ADDR<18>	J21	A_18		
36 5 CPU_ADDR<19>	G21	A_19		
36 5 CPU_ADDR<20>	E21	A_20		
36 5 CPU_ADDR<21>	A24	A_21		
36 5 CPU_ADDR<22>	D21	A_22		
36 5 CPU_ADDR<23>	A23	A_23		
36 5 CPU_ADDR<24>	H20	A_24		
36 5 CPU_ADDR<25>	B22	A_25		
36 5 CPU_ADDR<26>	H21	A_26		
36 5 CPU_ADDR<27>	A22	A_27		
36 5 CPU_ADDR<28>	E20	A_28		
36 5 CPU_ADDR<29>	B21	A_29		
36 5 CPU_ADDR<30>	D20	A_30		
36 5 CPU_ADDR<31>	A21	A_31		
36 5 CPU_CI_L	G26	CI		
36 5 CPU_GBL_L	A29	GBL		
36 5 CPU_TBST_L	A28	TBST		
36 5 CPU_TSIZ<0>	G24	TSIZ_0		
36 5 CPU_TSIZ<1>	H24	TSIZ_1		
36 5 CPU_TSIZ<2>	D26	TSIZ_2		
36 5 CPU_TT<0>	E25	TT_0		
36 5 CPU_TT<1>	G25	TT_1		
36 5 CPU_TT<2>	B28	TT_2		
36 5 CPU_TT<3>	D27	TT_3		
36 5 CPU_TT<4>	J25	TT_4		
36 5 CPU_WT_L	D28	WT		
36 8 5 CPU_AACK_L	B29	AACK	NO BUS KEEPER - PU	
36 8 5 CPU_ARTRY_L	H23	ARTRY	NO BUS KEEPER - PU	
36 8 5 CPU_HIT_L	B31	HIT	INPUT - PU	
36 8 5 CPU_QREQ_L	A32	QREQ	INPUT - PD	
36 5 CPU_QACK_L	G27	QACK	NO BUS KEEPER - ?	
30 INT_SUSPEND_REQ_L	AK9	SUSPENDREQ		
30 INT_SUSPEND_ACK_L	AM8	SUSPENDACK		
		CPU_FB_IN	Vin = Intrepid Vcore (1.5V) Vout = MaxBus rail (1.8V)	
36 8 INT_CPUFB_IN	J24			
36 8 INT_CPUFB_OUT	H16	CPU_FB_OUT	NO BUS KEEPER - PU	
SYSCLK_LA_TP	G8	ANALYZER_CLK		
30 CPU_CLK_EN	AH9	STOPCPUCLK	INPUT - PU	
INTREPID_ACS_REF	H13	ACS_REF	NO BUS KEEPER - ?	
36 SYSCLK_CPU_UF	J15	CPU_CLK	NO BUS KEEPER - PU	
5 CPU_TBEN	A31	TBEN	NO BUS KEEPER - PU	

INTREPID OUTPUTS HIGH BY DEFAULT

VSSA_7 (PLL6) H25

D_0	D10	CPU_DATA<0>	6 36
D_1	G12	CPU_DATA<1>	6 36
D_2	E11	CPU_DATA<2>	6 36
D_3	H11	CPU_DATA<3>	6 36
D_4	B9	CPU_DATA<4>	6 36
D_5	B8	CPU_DATA<5>	6 36
D_6	A9	CPU_DATA<6>	6 36
D_7	A8	CPU_DATA<7>	6 36
D_8	E12	CPU_DATA<8>	6 36
D_9	D11	CPU_DATA<9>	6 36
D_10	B10	CPU_DATA<10>	6 36
D_11	J13	CPU_DATA<11>	6 36
D_12	A10	CPU_DATA<12>	6 36
D_13	D12	CPU_DATA<13>	6 36
D_14	E13	CPU_DATA<14>	6 36
D_15	G13	CPU_DATA<15>	6 36
D_16	B11	CPU_DATA<16>	6 36
D_17	D13	CPU_DATA<17>	6 36
D_18	A11	CPU_DATA<18>	6 36
D_19	G14	CPU_DATA<19>	6 36
D_20	H14	CPU_DATA<20>	6 36
D_21	E14	CPU_DATA<21>	6 36
D_22	B12	CPU_DATA<22>	6 36
D_23	G15	CPU_DATA<23>	6 36
D_24	B13	CPU_DATA<24>	6 36
D_25	H15	CPU_DATA<25>	6 36
D_26	D14	CPU_DATA<26>	6 36
D_27	B14	CPU_DATA<27>	6 36
D_28	A12	CPU_DATA<28>	6 36
D_29	G16	CPU_DATA<29>	6 36
D_30	E15	CPU_DATA<30>	6 36
D_31	J16	CPU_DATA<31>	6 36
D_32	D15	CPU_DATA<32>	6 8 36
D_33	A14	CPU_DATA<33>	6 8 36
D_34	A13	CPU_DATA<34>	6 8 36
D_35	D16	CPU_DATA<35>	6 8 36
D_36	E16	CPU_DATA<36>	6 8 36
D_37	G17	CPU_DATA<37>	6 8 36
D_38	B15	CPU_DATA<38>	6 8 36
D_39	H17	CPU_DATA<39>	6 8 36
D_40	A15	CPU_DATA<40>	6 8 36
D_41	B16	CPU_DATA<41>	6 8 36
D_42	E17	CPU_DATA<42>	6 8 36
D_43	A16	CPU_DATA<43>	6 8 36
D_44	J18	CPU_DATA<44>	6 8 36
D_45	H18	CPU_DATA<45>	6 8 36
D_46	D17	CPU_DATA<46>	6 8 36
D_47	G18	CPU_DATA<47>	6 8 36
D_48	A17	CPU_DATA<48>	6 8 36
D_49	B17	CPU_DATA<49>	6 8 36
D_50	E18	CPU_DATA<50>	6 8 36
D_51	B18	CPU_DATA<51>	6 8 36
D_52	D18	CPU_DATA<52>	6 8 36
D_53	A18	CPU_DATA<53>	6 8 36
D_54	A19	CPU_DATA<54>	6 8 36
D_55	H19	CPU_DATA<55>	6 8 36
D_56	B19	CPU_DATA<56>	6 8 36
D_57	J19	CPU_DATA<57>	6 8 36
D_58	A20	CPU_DATA<58>	6 8 36
D_59	D19	CPU_DATA<59>	6 8 36
D_60	E19	CPU_DATA<60>	6 8 36
D_61	G19	CPU_DATA<61>	6 8 36
D_62	B20	CPU_DATA<62>	6 8 36
D_63	G20	CPU_DATA<63>	6 8 36
DBG	A30	CPU_DBG_L	5 8 36
DRDY	G28	CPU_DRDY_L	5 8 36
DTI_0	K25	CPU_DTI<0>	5 36
DTI_1	D29	CPU_DTI<1>	5 36
DTI_2	B30	CPU_DTI<2>	5 36
TA	E27	CPU_TA_L	5 8 36
TEA	E28	CPU_TEA_L	5 8 36

FB BUFFER HAS 50 OHM OUTPUT IMPEDANCE

R197 511 1% 1/16W MF 402

R144 0 5% 1/16W MF 402

R137 1K 1% 1/16W MF 402

SHORT = 1" SHORTER THAN MATCHED LENGTH

LONG = 1" LONGER THAN MATCHED LENGTH

36 8 INT_CPUFB_OUT	R167 0 5% 1/16W MF 402	36 INT_CPUFB_OUT_SHORT	R215 0 5% 1/16W MF 402	36 INT_CPUFB_OUT_NORM	NO STUFF R207 0 5% 1/16W MF 402	36 INT_CPUFB_LONG
36 8 INT_CPUFB_IN	NO STUFF R225 0 5% 1/16W MF 402		R226 0 5% 1/16W MF 402	36 INT_CPUFB_IN_NORM	R208 0 5% 1/16W MF 402 NO STUFF R196 0 5% 1/16W MF 402	

MAXBUS PULL-UPS

MAXBUS_SLEEP 5 7 8 15 16 23 34 38

36 8 5 CPU_TS_L	RP21 10K 5% 1/16W SM1	2 7
36 8 5 CPU_TA_L	RP21 10K 5% 1/16W SM1	1 8
36 8 5 CPU_ARTRY_L	RP21 10K 5% 1/16W SM1	4 5
36 8 5 CPU_BR_L	RP23 10K 5% 1/16W SM1	1 8
36 8 5 CPU_HIT_L	RP24 10K 5% 1/16W SM1	3 6
36 8 5 CPU_DRDY_L	RP23 10K 5% 1/16W SM1	3 6
36 8 5 CPU_TEA_L	RP23 10K 5% 1/16W SM1	4 5
36 8 5 CPU_AACK_L	RP23 10K 5% 1/16W SM1	2 7
36 8 5 CPU_DBG_L	RP24 10K 5% 1/16W SM1	4 5
36 8 5 CPU_BG_L	RP21 10K 5% 1/16W SM1	3 6
36 8 5 CPU_QREQ_L	RP24 10K 5% 1/16W SM1	2 7

INTREPID BOOT STRAPS

BIT 56 TO 63

38 34 23 16 15 8 7 5 MAXBUS_SLEEP

R140	R161	R175	R132	R131	R150	R174	R182
NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF		NO STUFF
10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402
36 8 6 CPU_DATA<56>	36 8 6 CPU_DATA<57>	36 8 6 CPU_DATA<58>	36 8 6 CPU_DATA<59>	36 8 6 CPU_DATA<60>	36 8 6 CPU_DATA<61>	36 8 6 CPU_DATA<62>	36 8 6 CPU_DATA<63>

R654	R669	R677	R646	R647	R660	R678	R685
10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	NO STUFF 10K 5% 1/16W MF 402	10K 5% 1/16W MF 402

Spare

Spare

Spare

0: PCI1_REQ2_L / GPIO[26] 1: GPIO[26]

0: PCI1_REQ1_L / PCI1_GNT1_L 1: GPIO[25]

0: PCI1_REQ0_L / PCI1_GNT0_L 1: GPIO[24]

0: Legacy interface 1: B-mode interface

0: Disable PWM interface 1: Enable PWM interface

0: 66X Mode (G3) 1: 100X Mode (G3)

Processor Bus Mode

Intrepid MaxBus

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7202	B
SCALE: NONE	SHT 8 OF 44	

SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

PINS ARE SWAPABLE FOR RPAKS

U45
INTREPID-REV2.1
BGA
(2 OF 9)
CRITICAL

DDR MEMORY INTERFACE

DDR_DATA_0	AK32	MEM_DATA<0>	36 10
DDR_DATA_1	AK33	MEM_DATA<1>	36 10
DDR_DATA_2	AK31	MEM_DATA<2>	36 10
DDR_DATA_3	AK35	MEM_DATA<3>	36 10
DDR_DATA_4	AK36	MEM_DATA<4>	36 10
DDR_DATA_5	AJ32	MEM_DATA<5>	36 10
DDR_DATA_6	AJ35	MEM_DATA<6>	36 10
DDR_DATA_7	AJ36	MEM_DATA<7>	36 10
DDR_DATA_8	AG33	MEM_DATA<8>	36 10
DDR_DATA_9	AG35	MEM_DATA<9>	36 10
DDR_DATA_10	AH35	MEM_DATA<10>	36 10
DDR_DATA_11	AG36	MEM_DATA<11>	36 10
DDR_DATA_12	AH36	MEM_DATA<12>	36 10
DDR_DATA_13	AH32	MEM_DATA<13>	36 10
DDR_DATA_14	AG32	MEM_DATA<14>	36 10
DDR_DATA_15	AG31	MEM_DATA<15>	36 10
DDR_DATA_16	AE32	MEM_DATA<16>	36 10
DDR_DATA_17	AF35	MEM_DATA<17>	36 10
DDR_DATA_18	AF36	MEM_DATA<18>	36 10
DDR_DATA_19	AE36	MEM_DATA<19>	36 10
DDR_DATA_20	AE35	MEM_DATA<20>	36 10
DDR_DATA_21	AE33	MEM_DATA<21>	36 10
DDR_DATA_22	AD36	MEM_DATA<22>	36 10
DDR_DATA_23	AD35	MEM_DATA<23>	36 10
DDR_DATA_24	AA36	MEM_DATA<24>	36 10
DDR_DATA_25	AA35	MEM_DATA<25>	36 10
DDR_DATA_26	AA33	MEM_DATA<26>	36 10
DDR_DATA_27	AB36	MEM_DATA<27>	36 10
DDR_DATA_28	AB35	MEM_DATA<28>	36 10
DDR_DATA_29	AC36	MEM_DATA<29>	36 10
DDR_DATA_30	AA32	MEM_DATA<30>	36 10
DDR_DATA_31	AB33	MEM_DATA<31>	36 10
DDR_DATA_32	V36	MEM_DATA<32>	36 10
DDR_DATA_33	U33	MEM_DATA<33>	36 10
DDR_DATA_34	U32	MEM_DATA<34>	36 10
DDR_DATA_35	V35	MEM_DATA<35>	36 10
DDR_DATA_36	T30	MEM_DATA<36>	36 10
DDR_DATA_37	U36	MEM_DATA<37>	36 10
DDR_DATA_38	U35	MEM_DATA<38>	36 10
DDR_DATA_39	T36	MEM_DATA<39>	36 10
DDR_DATA_40	P33	MEM_DATA<40>	36 10
DDR_DATA_41	R30	MEM_DATA<41>	36 10
DDR_DATA_42	P35	MEM_DATA<42>	36 10
DDR_DATA_43	P36	MEM_DATA<43>	36 10
DDR_DATA_44	R36	MEM_DATA<44>	36 10
DDR_DATA_45	R35	MEM_DATA<45>	36 10
DDR_DATA_46	R33	MEM_DATA<46>	36 10
DDR_DATA_47	R32	MEM_DATA<47>	36 10
DDR_DATA_48	N35	MEM_DATA<48>	36 10
DDR_DATA_49	M36	MEM_DATA<49>	36 10
DDR_DATA_50	L35	MEM_DATA<50>	36 10
DDR_DATA_51	M35	MEM_DATA<51>	36 10
DDR_DATA_52	M33	MEM_DATA<52>	36 10
DDR_DATA_53	L36	MEM_DATA<53>	36 10
DDR_DATA_54	N33	MEM_DATA<54>	36 10
DDR_DATA_55	M30	MEM_DATA<55>	36 10
DDR_DATA_56	J32	MEM_DATA<56>	36 10
DDR_DATA_57	J33	MEM_DATA<57>	36 10
DDR_DATA_58	J35	MEM_DATA<58>	36 10
DDR_DATA_59	K32	MEM_DATA<59>	36 10
DDR_DATA_60	K33	MEM_DATA<60>	36 10
DDR_DATA_61	J36	MEM_DATA<61>	36 10
DDR_DATA_62	K36	MEM_DATA<62>	36 10
DDR_DATA_63	K35	MEM_DATA<63>	36 10

DDR_A_0	H35	MEM_ADDR<0>	9 36
DDR_A_1	G35	MEM_ADDR<1>	9 36
DDR_A_2	G36	MEM_ADDR<2>	9 36
DDR_A_3	F36	MEM_ADDR<3>	9 36
DDR_A_4	F35	MEM_ADDR<4>	9 36
DDR_A_5	E35	MEM_ADDR<5>	9 36
DDR_A_6	E36	MEM_ADDR<6>	9 36
DDR_A_7	G32	MEM_ADDR<7>	9 36
DDR_A_8	D36	MEM_ADDR<8>	9 36
DDR_A_9	H36	MEM_ADDR<9>	9 36
DDR_A_10	G33	MEM_ADDR<10>	9 36
DDR_A_11	H33	MEM_ADDR<11>	9 36
DDR_A_12	D35	MEM_ADDR<12>	9 36
DDR_BA_0	L30	MEM_BA<0>	9 36
DDR_BA_1	M29	MEM_BA<1>	9 36
DDRCS_0	AN34	MEM_CS_L<0>	9 36
DDRCS_1	AN36	MEM_CS_L<1>	9 36
DDRCS_2	AL35	MEM_CS_L<2>	9 36
DDRCS_3	AL33	MEM_CS_L<3>	9 36
DDR_DQS_0	AJ31	MEM_DQS<0>	10 36
DDR_DQS_1	AH31	MEM_DQS<1>	10 36
DDR_DQS_2	AD32	MEM_DQS<2>	10 36
DDR_DQS_3	AB30	MEM_DQS<3>	10 36
DDR_DQS_4	V30	MEM_DQS<4>	10 36
DDR_DQS_5	P32	MEM_DQS<5>	10 36
DDR_DQS_6	N29	MEM_DQS<6>	10 36
DDR_DQS_7	L32	MEM_DQS<7>	10 36
DDR_DM_0	AJ33	MEM_DQM<0>	10 36
DDR_DM_1	AH33	MEM_DQM<1>	10 36
DDR_DM_2	AD33	MEM_DQM<2>	10 36
DDR_DM_3	AC35	MEM_DQM<3>	10 36
DDR_DM_4	T35	MEM_DQM<4>	10 36
DDR_DM_5	T33	MEM_DQM<5>	10 36
DDR_DM_6	N32	MEM_DQM<6>	10 36
DDR_DM_7	L33	MEM_DQM<7>	10 36
DDRRAS	L29	MEM_RAS_L	9 36
DDRCAS	H32	MEM_CAS_L	9 36
DDRWE	E30	MEM_WE_L	9 36
DDRCKE0	AM35	MEM_CKE<0>	9 36
DDRCKE1	AM35	MEM_CKE<1>	9 36
DDRCKE2	AM36	MEM_CKE<2>	9 36
DDRCKE3	AL36	MEM_CKE<3>	9 36
DDR_SELHI_0	AB32	MEM_MUXSEL_H<0>	10 36
DDR_SELHI_1	AE29	MEM_MUXSEL_H<1>	10 36
DDR_SELLO_0	N30	MEM_MUXSEL_L<0>	10 36
DDR_SELLO_1	T32	MEM_MUXSEL_L<1>	10 36
DDR_MCLK_0_P	Y32	SYSCLK_DDRCLK_A0_UF	9 36
DDR_MCLK_0_N	Y33	SYSCLK_DDRCLK_A0_L_UF	9 36
DDR_MCLK_1_P	Y35	SYSCLK_DDRCLK_A1_UF	9 36
DDR_MCLK_1_N	Y36	SYSCLK_DDRCLK_A1_L_UF	9 36
DDR_MCLK_2_P	Y30	INT_DDRCLK2_P_TP	
DDR_MCLK_2_N	W30	INT_DDRCLK2_N_TP	
DDR_MCLK_3_P	W32	SYSCLK_DDRCLK_B0_UF	9 36
DDR_MCLK_3_N	W33	SYSCLK_DDRCLK_B0_L_UF	9 36
DDR_MCLK_4_P	V33	SYSCLK_DDRCLK_B1_UF	9 36
DDR_MCLK_4_N	V32	SYSCLK_DDRCLK_B1_L_UF	9 36
DDR_MCLK_5_P	W35	INT_DDRCLK5_P_TP	
DDR_MCLK_5_N	W36	INT_DDRCLK5_N_TP	
DDR_REF	AA22	INT_MEM_REF_H	38
DDR_VREF_0	Y22	INT_MEM_VREF	9 38
DDR_VREF_1	T22		

'0' & '1' GO TO SLOT A
'2' & '3' GO TO SLOT B

'0' & '1' GO TO SLOT A
'2' & '3' GO TO SLOT B

'0'S ARE SAME POLARITY (ACTIVE-LO)
'1'S ARE SAME POLARITY (ACTIVE-HI)

R199 1K 1% 1/16W MF 402

MEM_VREF

38 16 15 10 +2_5V_INTREPID

R198 10K 1% 1/16W MF 402
R191 10K 1% 1/16W MF 402
C245 0.1UF 20% 10V CERM 402
INT_MEM_VREF 9 38

CLOCKS

SYSCLK_DDRCLK_A1_UF	RP33	4	SYSCLK_DDRCLK_A1 11 36
SYSCLK_DDRCLK_A1_L_UF	RP33	6	SYSCLK_DDRCLK_A1_L 11 36
SYSCLK_DDRCLK_A0_UF	RP34	1	SYSCLK_DDRCLK_A0 11 36
SYSCLK_DDRCLK_A0_L_UF	RP34	7	SYSCLK_DDRCLK_A0_L 11 36
SYSCLK_DDRCLK_B1_UF	RP33	2	SYSCLK_DDRCLK_B1 11 36
SYSCLK_DDRCLK_B1_L_UF	RP33	8	SYSCLK_DDRCLK_B1_L 11 36
SYSCLK_DDRCLK_B0_UF	RP34	3	SYSCLK_DDRCLK_B0 11 36
SYSCLK_DDRCLK_B0_L_UF	RP34	5	SYSCLK_DDRCLK_B0_L 11 36

CS

MEM_CS_L<0>	RP36	1	RAM_CS_L<0> 11 36
MEM_CS_L<1>	RP36	3	RAM_CS_L<1> 11 36
MEM_CS_L<2>	RP35	4	RAM_CS_L<2> 11 36
MEM_CS_L<3>	RP35	2	RAM_CS_L<3> 11 36

CKE

MEM_CKE<0>	RP36	2	RAM_CKE<0> 9 11 36
MEM_CKE<1>	RP36	4	RAM_CKE<1> 9 11 36
MEM_CKE<2>	RP35	1	RAM_CKE<2> 9 11 36
MEM_CKE<3>	RP35	3	RAM_CKE<3> 9 11 36

ADDR

MEM_ADDR<0>	RP31	1	RAM_ADDR<0> 11 36
MEM_ADDR<1>	RP25	1	RAM_ADDR<1> 11 36
MEM_ADDR<2>	RP25	2	RAM_ADDR<2> 11 36
MEM_ADDR<3>	RP25	4	RAM_ADDR<3> 11 36
MEM_ADDR<4>	RP25	3	RAM_ADDR<4> 11 36
MEM_ADDR<5>	RP30	1	RAM_ADDR<5> 11 36
MEM_ADDR<6>	RP30	2	RAM_ADDR<6> 11 36
MEM_ADDR<7>	RP31	3	RAM_ADDR<7> 11 36
MEM_ADDR<8>	RP30	4	RAM_ADDR<8> 11 36
MEM_ADDR<9>	RP31	2	RAM_ADDR<9> 11 36
MEM_ADDR<10>	RP31	4	RAM_ADDR<10> 11 36
MEM_ADDR<11>	RP26	4	RAM_ADDR<11> 11 36
MEM_ADDR<12>	RP30	3	RAM_ADDR<12> 11 36

BA

MEM_BA<0>	RP26	2	RAM_BA<0> 11 36
MEM_BA<1>	RP26	1	RAM_BA<1> 11 36

CNTL

MEM_WE_L	RP26	3	RAM_WE_L 11 36
MEM_CAS_L	R250	1	RAM_CAS_L 11 36
MEM_RAS_L	R238	1	RAM_RAS_L 11 36

All: 22 5% 1/16W SM1

1MB BOOT ROM

+3V_MAIN

C460 2.2UF 20% 10V CERM 805
C470 0.1UF 20% 10V CERM 402
C479 0.1UF 20% 10V CERM 402

U17
3.3V
TSOP
OMIT

A0	21	PCI_AD<0>	39 37 26 24 17 12
A1	20	PCI_AD<1>	39 37 26 24 17 12
A2	19	PCI_AD<2>	39 37 26 24 17 12
A3	18	PCI_AD<3>	39 37 26 24 17 12
A4	17	PCI_AD<4>	39 37 26 24 17 12
A5	16	PCI_AD<5>	39 37 26 24 17 12
A6	15	PCI_AD<6>	39 37 26 24 17 12
A7	14	PCI_AD<7>	39 37 26 24 17 12
A8	8	PCI_AD<8>	39 37 26 24 17 12
A9	7	PCI_AD<9>	39 37 26 24 17 12
A10	36	PCI_AD<10>	39 37 26 24 17 12
A11	6	PCI_AD<11>	39 37 26 24 17 12
A12	5	PCI_AD<12>	39 37 26 24 17 12
A13	4	PCI_AD<13>	39 37 26 24 17 12
A14	3	PCI_AD<14>	39 37 26 24 17 12
A15	2	PCI_AD<15>	39 37 26 24 17 12
A16	1	PCI_AD<16>	39 37 26 24 17 12
A17	40	PCI_AD<17>	39 37 26 24 17 12
A18	13	PCI_AD<18>	39 37 26 24 17 12
A19	37	PCI_AD<19>	39 37 26 24 17 12
A20	38	PCI_AD<20>	39 37 26 24 17 12
CE	22	ROM_ONBOARD_CS_L	39 24 12
OE	24	ROM_OE_L	39 24 12
WE	9	ROM_RW_L	39 24 12
WP	12	ROM_WP_L	
PWD	10	INT_RESET_L	30 13
GND	23 39		

DQ0	25	PCI_AD<24>	12 17 24 26 37 39
DQ1	26	PCI_AD<25>	12 17 24 26 37 39
DQ2	27	PCI_AD<26>	12 17 24 26 37 39
DQ3	28	PCI_AD<27>	12 17 24 26 37 39
DQ4	32	PCI_AD<28>	12 17 24 26 37 39
DQ5	33	PCI_AD<29>	12 17 24 26 37 39
DQ6	34	PCI_AD<30>	12 17 24 26 37 39
DQ7	35	PCI_AD<31>	12 17 24 26 37 39

VPP 11, VCC 30 31

+3V_MAIN

R338 10K 5% 1/16W MF 402
R386 10K 5% 1/16W MF 402
R357 1K 5% 1/16W MF 402

39 24 12 ROM_CS_L

OVERRIDE ROM MODULE
INTERCEPTS ROM CHIP SELECT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1940	1	SVC,IC,BOOTROM,PB17,4.9.7FO/Q41A	U17	CRITICAL	?

PULL-DOWN RESISTORS TO ENSURE
CKE STAYS LOW AFTER INTREPID
2.5V I/O SHUTS OFF

36 11 9 RAM_CKE<0>
36 11 9 RAM_CKE<1>
36 11 9 RAM_CKE<2>
36 11 9 RAM_CKE<3>

R500 10K 5% 1/16W MF 402
R439 10K 5% 1/16W MF 402
R409 10K 5% 1/16W MF 402
R387 10K 5% 1/16W MF 402

INT - DDR/BOOTROM

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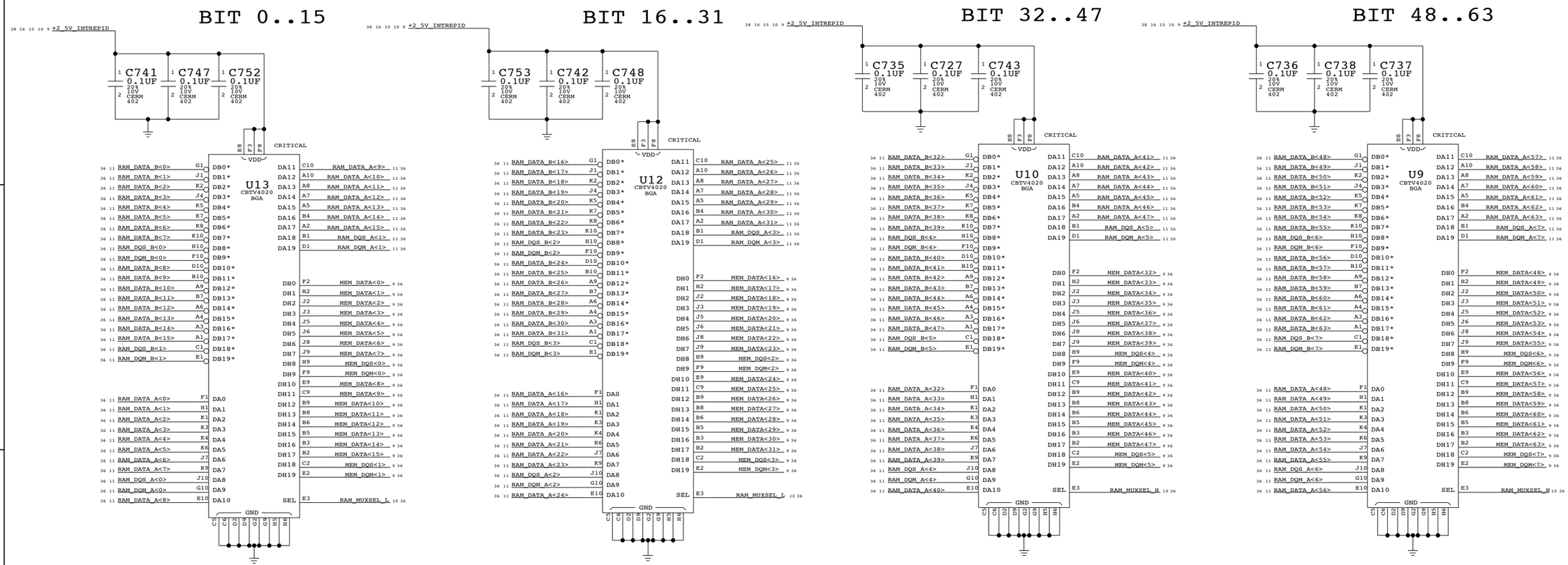
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7202	B
SCALE: NONE	SHT 9 OF 44	



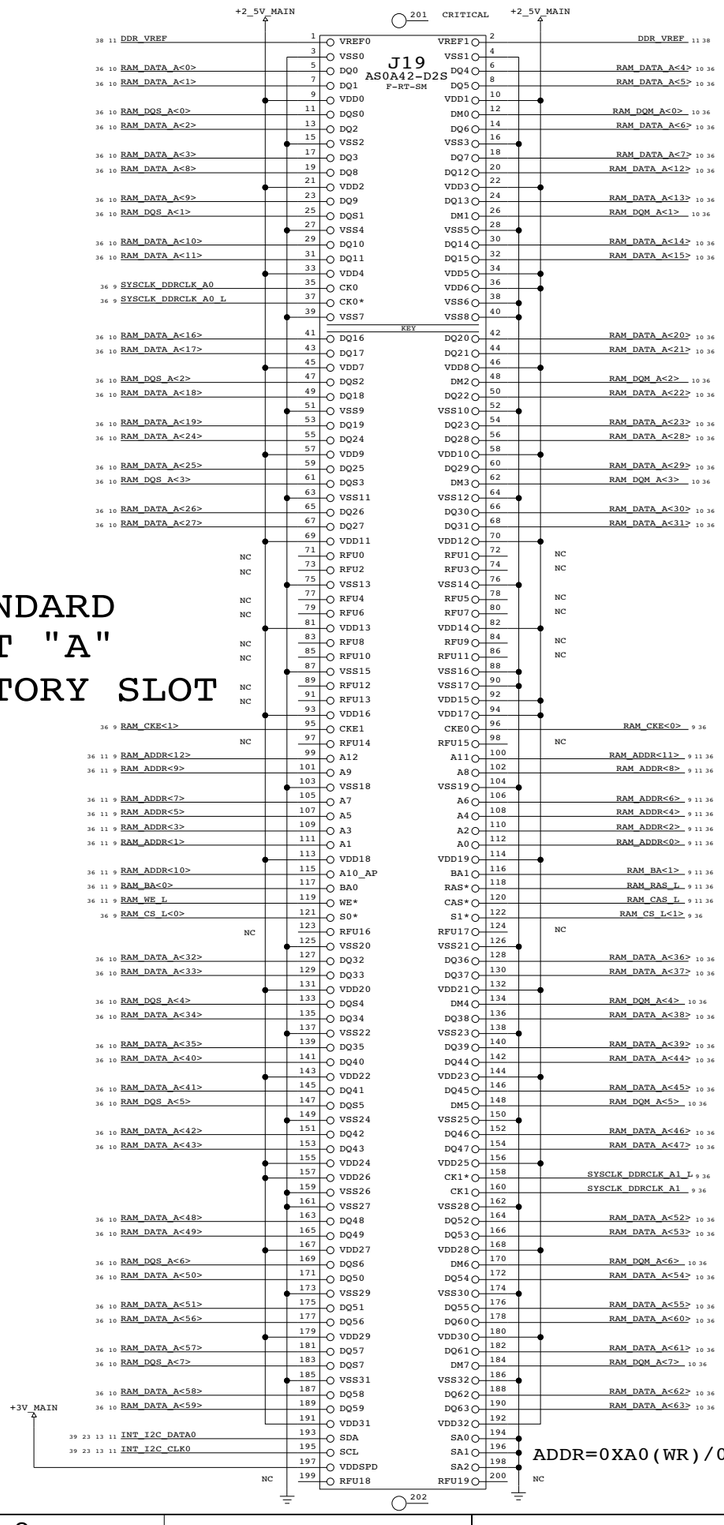
SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND
MEM_MUXSEL_H<0> AND MEM_MUXSEL_L<0> ARE ACTIVE LOW
MEM_MUXSEL_H<1> AND MEM_MUXSEL_L<1> ARE ACTIVE HIGH

ADDED 0 OHM RESISTORS IN CASE POLARITY IS WRONG

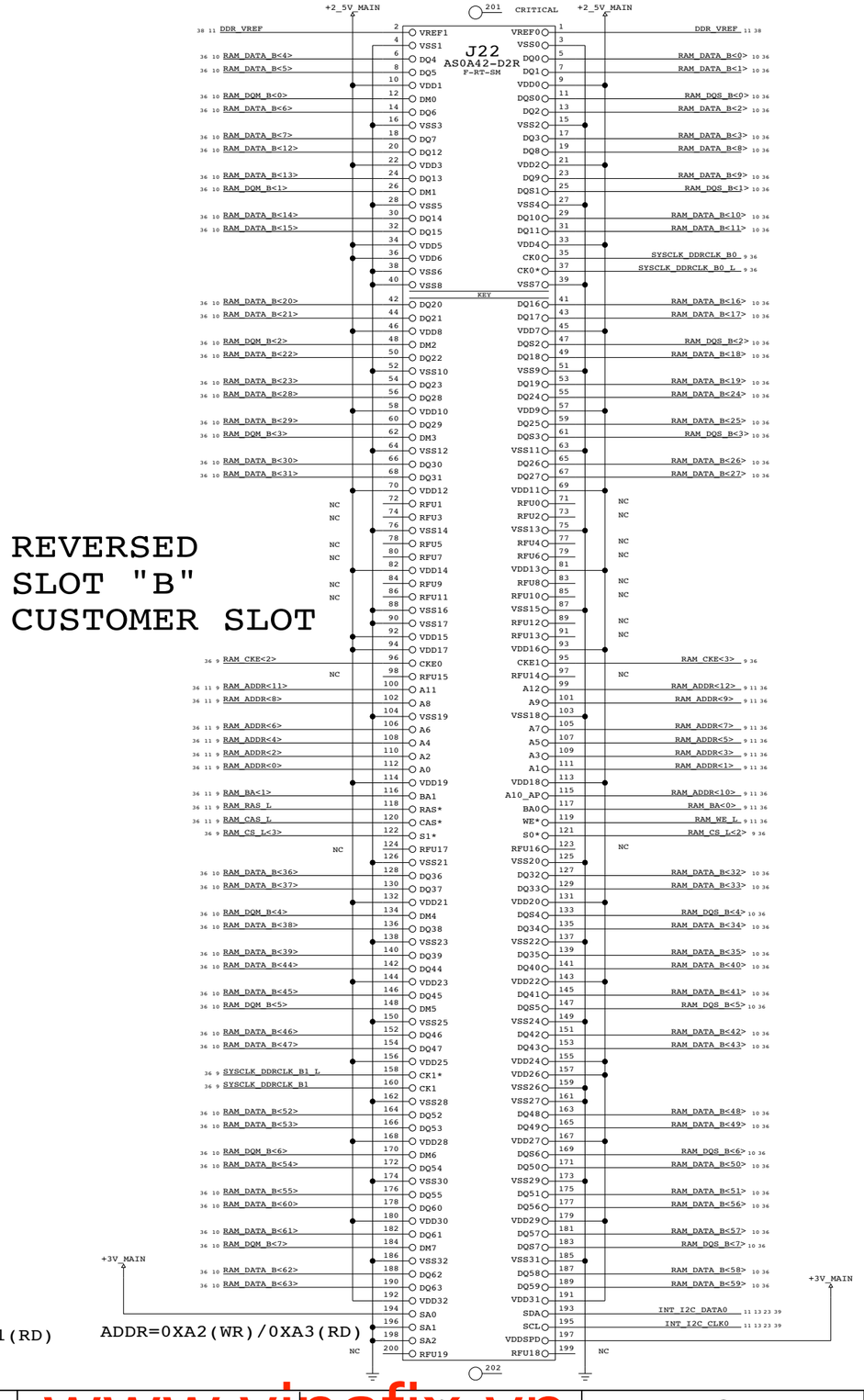
16BIT 2:1 DDR MUXES

APPLE COMPUTER INC.

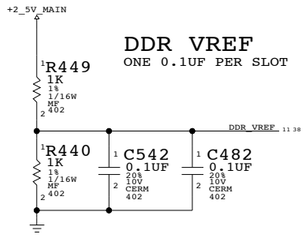
SIZE	DRAWING NUMBER	REV.
D	051-7202	B
SCALE: NONE	SHT 10 OF 44	

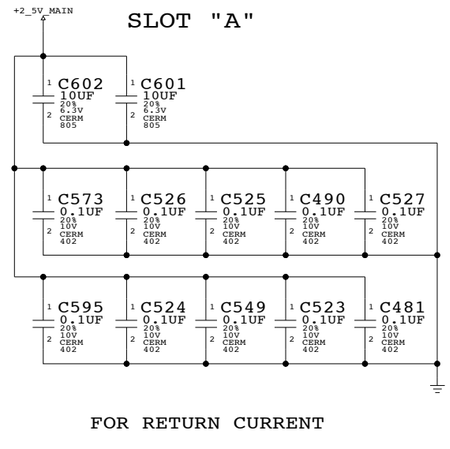


STANDARD
SLOT "A"
FACTORY SLOT

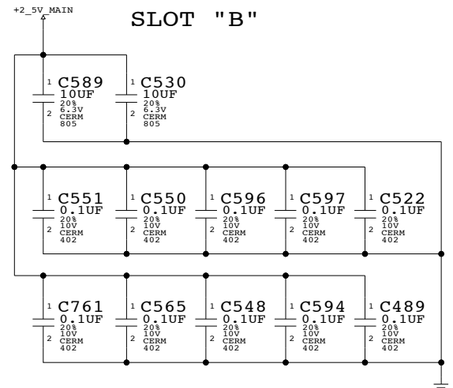


REVERSED
SLOT "B"
CUSTOMER SLOT





FOR RETURN CURRENT



DDR SODIMM CONNS

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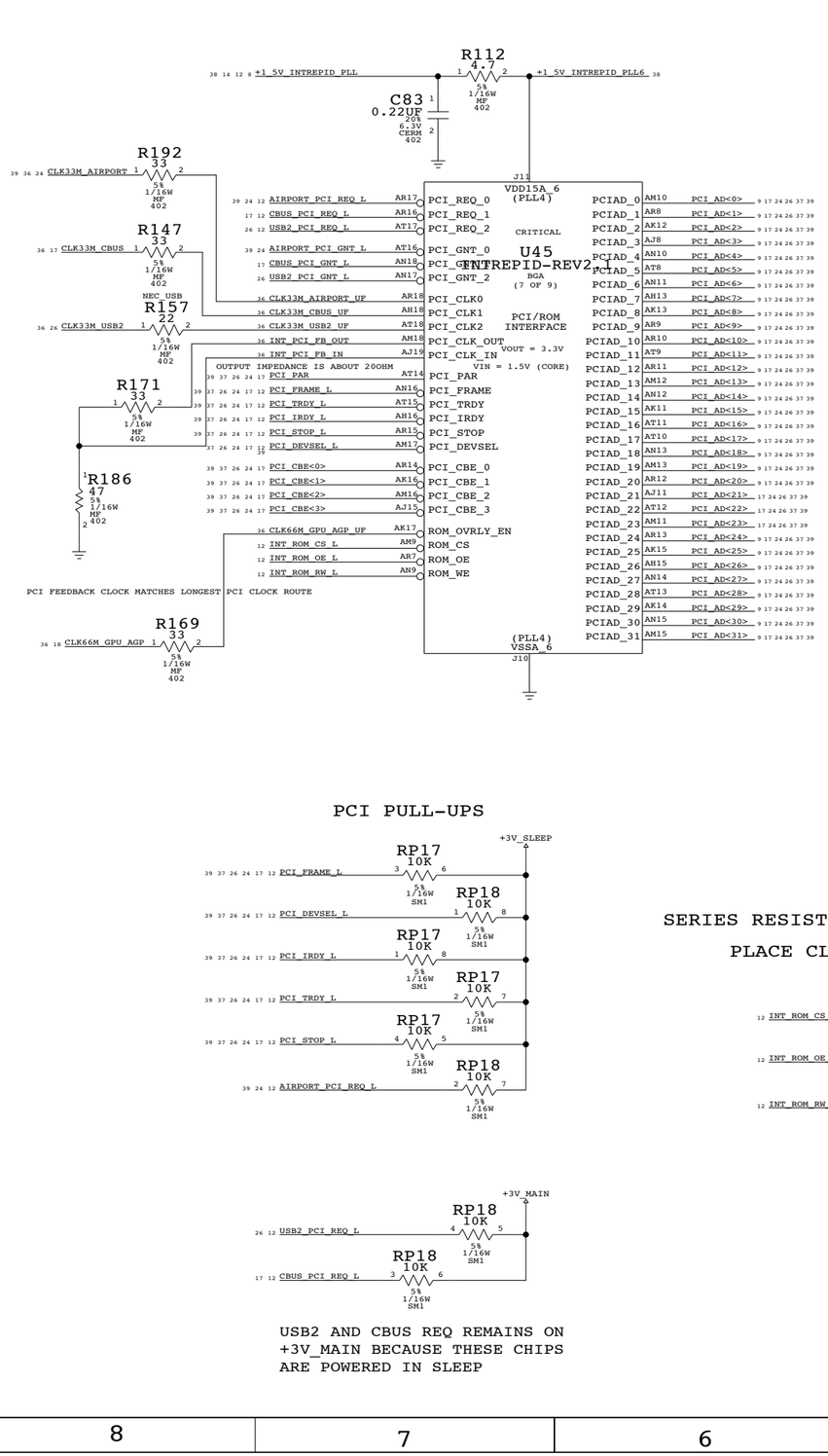
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7202	B

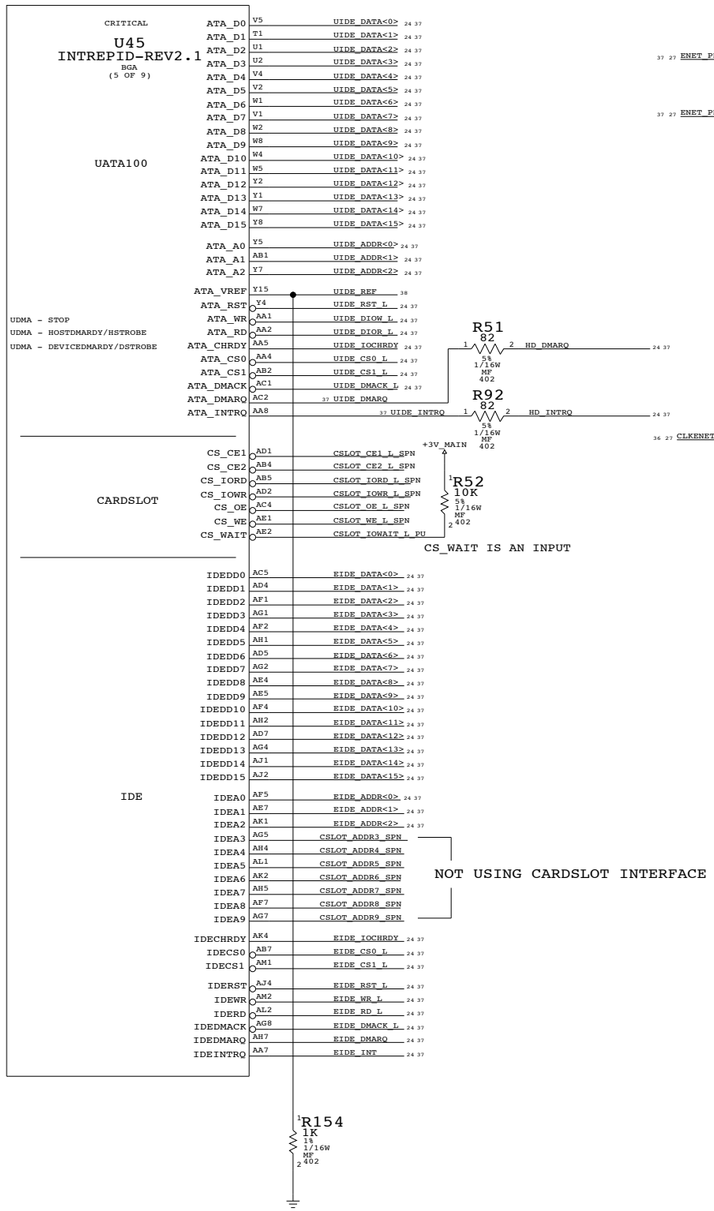
SCALE NONE | SHT 11 OF 44

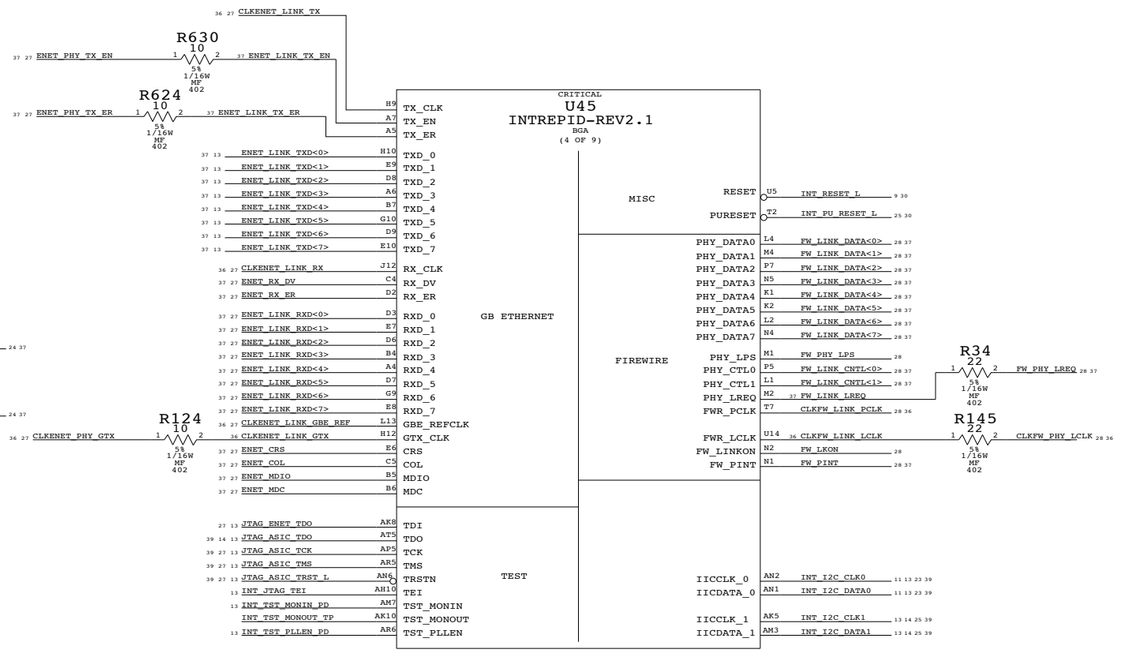


INTREPID AGP/PCI

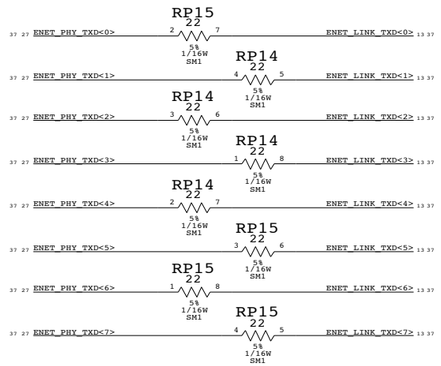
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7202	B
SCALE: NONE	SHT 12 OF 44	



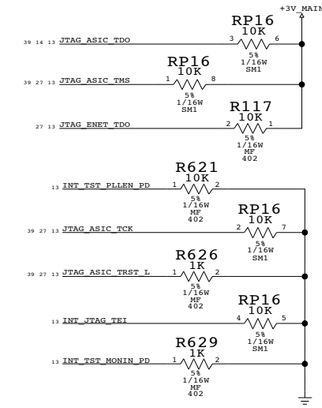


ENET_TXD SERIES TERMINATION

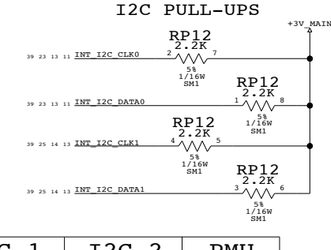


JTG_RSTN_L	TST_TEI_H	JTG_TDO_H (I/O)	JTG_TDI_H (I/O)	TST_PLLEN_H	ANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	EXTPLL SHUTDOWN (OUTPUT)	DDR_ TPDENABLE (OUTPUT)	0	(OUTPUT)	NORMAL OPERATION
0	0	(OUTPUT)	0(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	HWPLL_ TESTSEL5 (INPUT)	1(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0(I)	0(I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0(I)	1(I)	0	X(I)	ATPG IDDQ
0	1	0(I)	1(I)	1	X(I)	TEST TRI-STATE
0	1	1(I)	0(I)	0	X(I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1(I)	0(I)	1	X(I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1(I)	1(I)	X	X(I)	FUNCTIONAL TEST IDDQ

TEST PULL-UPS/DOWNS



I2C PULL-UPS



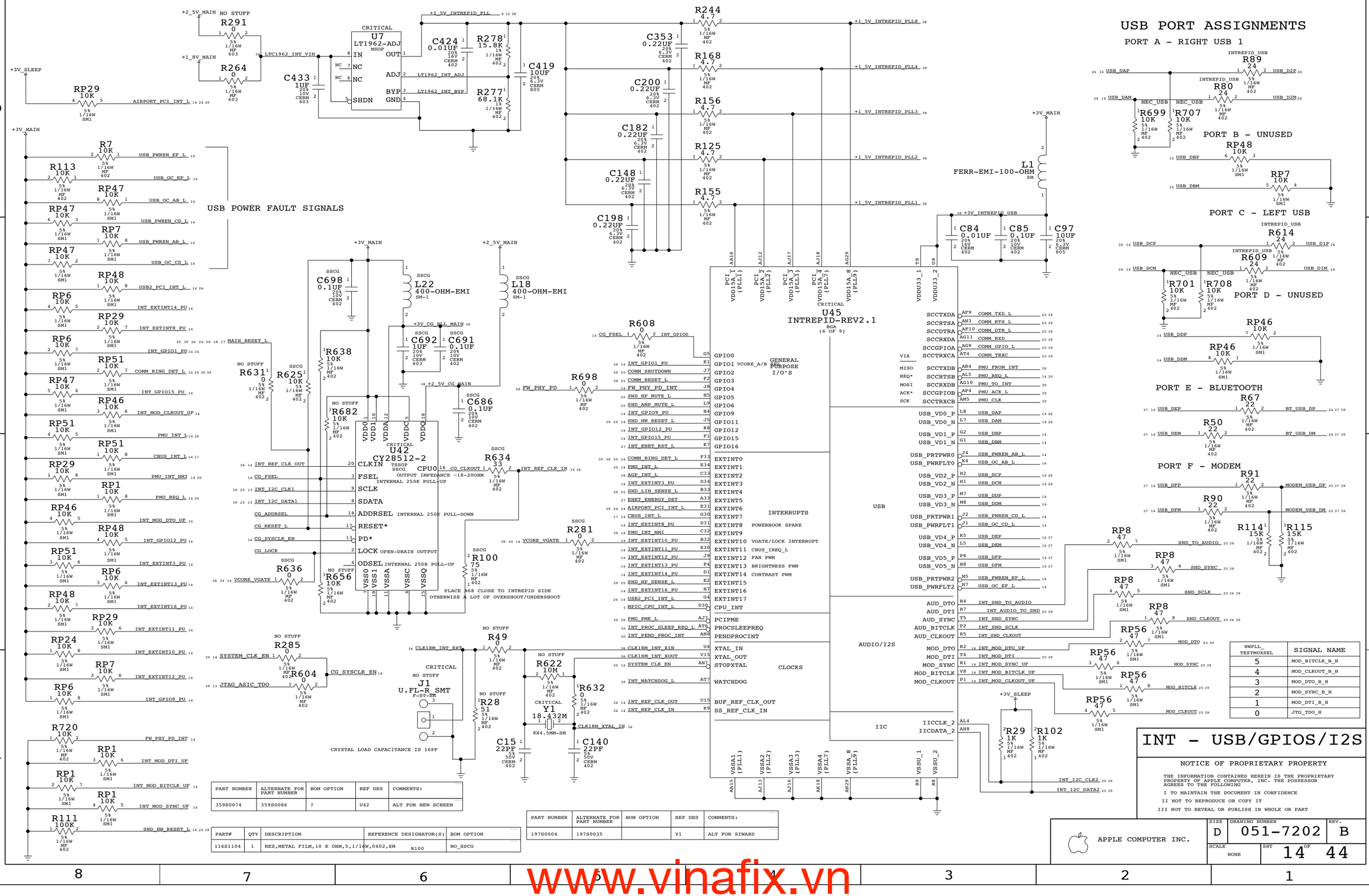
BUS / ADDR	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
A0-WR A1-RD	RAM - STANDARD J20 - PG 12	N/A	N/A	N/A
A2-WR A3-RD	RAM - REVERSED J23 - PG 12	N/A	N/A	N/A
AC-WR AD-RD	N/A	N/A	DASH MODEM J9 - PG 25	N/A
AE-WR AF-RD	BOOTBANG E2PROM U37 - PG 23	N/A	N/A	N/A
84-WR 85-RD	LMU U36 - PG 23	N/A	N/A	N/A
58-WR 59-RD	N/A	FAN CONTROLLER U3 - PG 24	N/A	N/A
6A-WR 6B-RD	N/A	N/A	SNAPPER SOUND J12 - PG 24	N/A
D0-WR D1-RD	N/A	CLOCK SLEW SSCG U56 - PG 15	N/A	N/A

ADDR LSB INDICATES READ ('1') OR WRITE ('0') MODES

INT - ENET/FW/UATA EIDE/I2C

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7202	B
SCALE: NONE	SHT 13 OF 44	

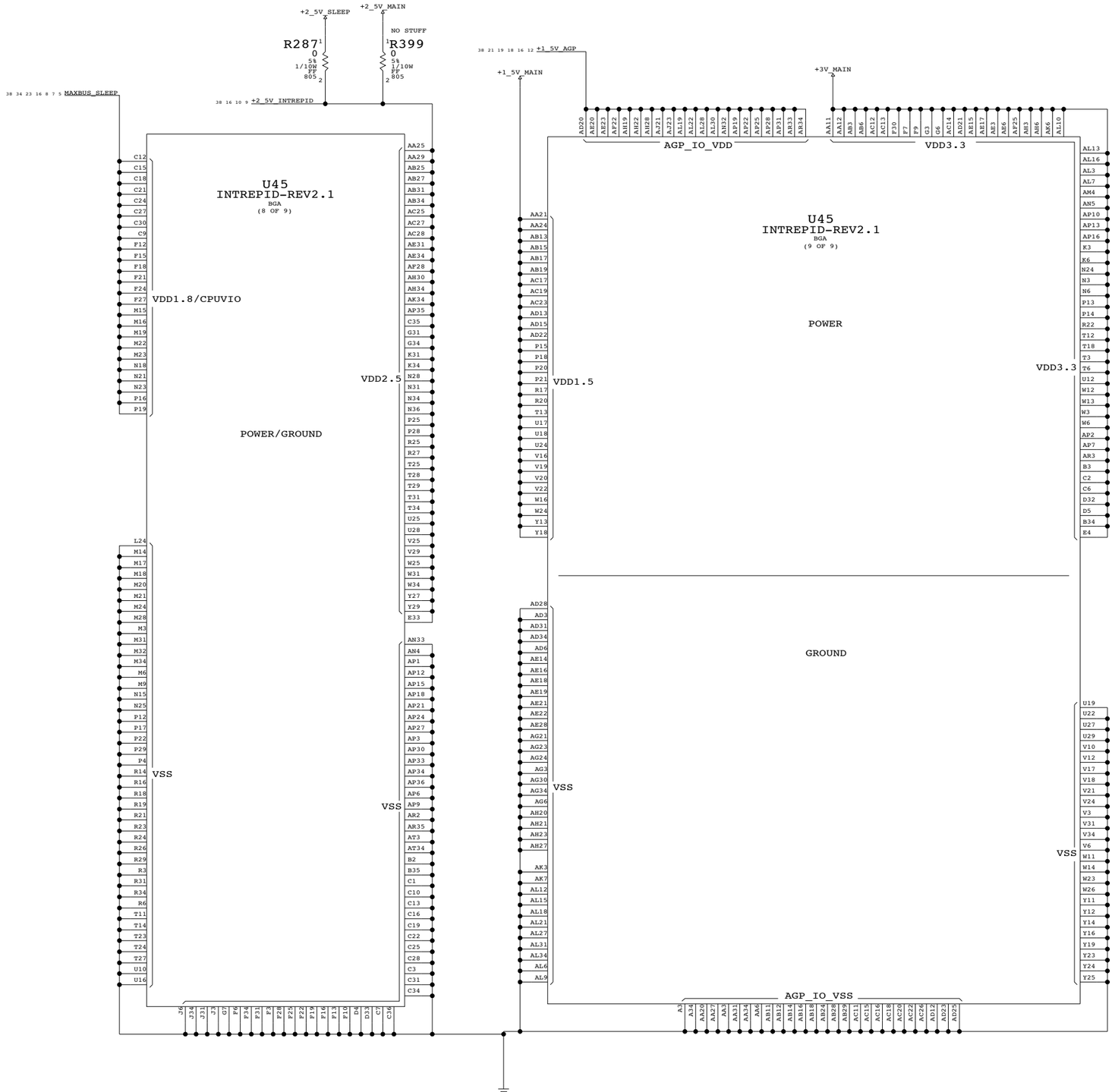


HWPLL_TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
359S0074	359S0086	?	U42	ALT FOR NEW SCREEN

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0004	197S0035		Y1	ALT FOR SIWARD

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES,METAL FILM,10 K OHM,5,1/16W,0402,SM	R100	NO_SSCG



Intrepid Power

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SIZE	DRAWING NUMBER	REV.
D	051-7202	B
SCALE: NONE	SHT 15 OF 44	

INTREPID MAXBUS DECOUPLING

24 Balls
4 X 10UF (0805)
32 X 0.22UF (0402)

23 15 8 7 5 38 34 MAXBUS_SLEEP

C204 10uF 20% 6.3V CERM 805 · C348 10uF 20% 6.3V CERM 805 · C239 0.22uF 20% 6.3V CERM 402 · C240 0.22uF 20% 6.3V CERM 402 · C350 0.22uF 20% 6.3V CERM 402 · C312 0.22uF 20% 6.3V CERM 402 · C176 0.22uF 20% 6.3V CERM 402 · C288 0.22uF 20% 6.3V CERM 402 · C313 0.22uF 20% 6.3V CERM 402 · C94 0.22uF 20% 6.3V CERM 402 · C286 0.22uF 20% 6.3V CERM 402 · C158 0.22uF 20% 6.3V CERM 402

C236 10uF 20% 6.3V CERM 805 · C196 10uF 20% 6.3V CERM 805 · C174 0.22uF 20% 6.3V CERM 402 · C206 0.22uF 20% 6.3V CERM 402 · C259 0.22uF 20% 6.3V CERM 402 · C237 0.22uF 20% 6.3V CERM 402 · C238 0.22uF 20% 6.3V CERM 402 · C95 0.22uF 20% 6.3V CERM 402 · C117 0.22uF 20% 6.3V CERM 402 · C241 0.22uF 20% 6.3V CERM 402 · C260 0.22uF 20% 6.3V CERM 402 · C314 0.22uF 20% 6.3V CERM 402

C173 0.22uF 20% 6.3V CERM 402 · C171 0.22uF 20% 6.3V CERM 402 · C175 0.22uF 20% 6.3V CERM 402 · C226 0.22uF 20% 6.3V CERM 402 · C172 0.22uF 20% 6.3V CERM 402 · C207 0.22uF 20% 6.3V CERM 402 · C118 0.22uF 20% 6.3V CERM 402 · C287 0.22uF 20% 6.3V CERM 402 · C119 0.22uF 20% 6.3V CERM 402 · C349 0.22uF 20% 6.3V CERM 402

C205 0.22uF 20% 6.3V CERM 402 · C209 0.22uF 20% 6.3V CERM 402

INTREPID AGP I/O DECOUPLING

21 Balls
4 X 10UF (0805)
24 X 0.22UF (0402)

38 21 19 18 15 12 +1_5V_AGP

C371 10uF 20% 6.3V CERM 805 · C231 10uF 20% 6.3V CERM 805 · C356 0.22uF 20% 6.3V CERM 402 · C297 0.22uF 20% 6.3V CERM 402 · C268 0.22uF 20% 6.3V CERM 402 · C217 0.22uF 20% 6.3V CERM 402 · C355 0.22uF 20% 6.3V CERM 402 · C267 0.22uF 20% 6.3V CERM 402 · C250 0.22uF 20% 6.3V CERM 402 · C298 0.22uF 20% 6.3V CERM 402 · C377 0.22uF 20% 6.3V CERM 402 · C216 0.22uF 20% 6.3V CERM 402

C281 10uF 20% 6.3V CERM 805 · C394 10uF 20% 6.3V CERM 805 · C228 0.22uF 20% 6.3V CERM 402 · C230 0.22uF 20% 6.3V CERM 402 · C265 0.22uF 20% 6.3V CERM 402 · C378 0.22uF 20% 6.3V CERM 402 · C357 0.22uF 20% 6.3V CERM 402 · C229 0.22uF 20% 6.3V CERM 402 · C325 0.22uF 20% 6.3V CERM 402 · C393 0.22uF 20% 6.3V CERM 402 · C324 0.22uF 20% 6.3V CERM 402 · C323 0.22uF 20% 6.3V CERM 402

C251 0.22uF 20% 6.3V CERM 402 · C266 0.22uF 20% 6.3V CERM 402 · C249 0.22uF 20% 6.3V CERM 402

INTREPID DDR DECOUPLING

44 Balls
4 X 10UF (0805)
51 X 0.22UF (0402)

38 15 10 9 +2_5V_INTREPID

C422 10uF 20% 6.3V CERM 805 · C417 10uF 20% 6.3V CERM 805 · C407 0.22uF 20% 6.3V CERM 402 · C391 0.22uF 20% 6.3V CERM 402 · C310 0.22uF 20% 6.3V CERM 402 · C317 0.22uF 20% 6.3V CERM 402 · C480 0.22uF 20% 6.3V CERM 402 · C390 0.22uF 20% 6.3V CERM 402 · C370 0.22uF 20% 6.3V CERM 402 · C320 0.22uF 20% 6.3V CERM 402 · C365 0.22uF 20% 6.3V CERM 402 · C366 0.22uF 20% 6.3V CERM 402

C418 10uF 20% 6.3V CERM 805 · C423 10uF 20% 6.3V CERM 805 · C367 0.22uF 20% 6.3V CERM 402 · C292 0.22uF 20% 6.3V CERM 402 · C295 0.22uF 20% 6.3V CERM 402 · C403 0.22uF 20% 6.3V CERM 402 · C291 0.22uF 20% 6.3V CERM 402 · C352 0.22uF 20% 6.3V CERM 402 · C322 0.22uF 20% 6.3V CERM 402 · C392 0.22uF 20% 6.3V CERM 402 · C385 0.22uF 20% 6.3V CERM 402 · C376 0.22uF 20% 6.3V CERM 402

C321 0.22uF 20% 6.3V CERM 402 · C318 0.22uF 20% 6.3V CERM 402 · C399 0.22uF 20% 6.3V CERM 402 · C410 0.22uF 20% 6.3V CERM 402 · C335 0.22uF 20% 6.3V CERM 402 · C369 0.22uF 20% 6.3V CERM 402 · C384 0.22uF 20% 6.3V CERM 402 · C294 0.22uF 20% 6.3V CERM 402 · C406 0.22uF 20% 6.3V CERM 402 · C405 0.22uF 20% 6.3V CERM 402

C404 0.22uF 20% 6.3V CERM 402 · C400 0.22uF 20% 6.3V CERM 402 · C386 0.22uF 20% 6.3V CERM 402 · C289 0.22uF 20% 6.3V CERM 402 · C387 0.22uF 20% 6.3V CERM 402 · C401 0.22uF 20% 6.3V CERM 402 · C354 0.22uF 20% 6.3V CERM 402 · C389 0.22uF 20% 6.3V CERM 402 · C309 0.22uF 20% 6.3V CERM 402 · C398 0.22uF 20% 6.3V CERM 402

C337 0.22uF 20% 6.3V CERM 402 · C290 0.22uF 20% 6.3V CERM 402 · C402 0.22uF 20% 6.3V CERM 402 · C397 0.22uF 20% 6.3V CERM 402 · C368 0.22uF 20% 6.3V CERM 402 · C334 0.22uF 20% 6.3V CERM 402 · C388 0.22uF 20% 6.3V CERM 402 · C293 0.22uF 20% 6.3V CERM 402 · C319 0.22uF 20% 6.3V CERM 402 · C336 0.22uF 20% 6.3V CERM 402

C316 0.22uF 20% 6.3V CERM 402

INTREPID CORE DECOUPLING

30 Balls
4 X 10UF (0805)
29 X 0.22UF (0402)

+1_5V_MAIN

C128 10uF 20% 6.3V CERM 805 · C101 10uF 20% 6.3V CERM 805 · C147 0.22uF 20% 6.3V CERM 402 · C243 0.22uF 20% 6.3V CERM 402 · C262 0.22uF 20% 6.3V CERM 402 · C242 0.22uF 20% 6.3V CERM 402 · C227 0.22uF 20% 6.3V CERM 402 · C181 0.22uF 20% 6.3V CERM 402 · C142 0.22uF 20% 6.3V CERM 402 · C215 0.22uF 20% 6.3V CERM 402 · C278 0.22uF 20% 6.3V CERM 402 · C264 0.22uF 20% 6.3V CERM 402

C157 10uF 20% 6.3V CERM 805 · C315 10uF 20% 6.3V CERM 805 · C244 0.22uF 20% 6.3V CERM 402 · C212 0.22uF 20% 6.3V CERM 402 · C178 0.22uF 20% 6.3V CERM 402 · C179 0.22uF 20% 6.3V CERM 402 · C177 0.22uF 20% 6.3V CERM 402 · C159 0.22uF 20% 6.3V CERM 402 · C161 0.22uF 20% 6.3V CERM 402 · C162 0.22uF 20% 6.3V CERM 402 · C280 0.22uF 20% 6.3V CERM 402 · C279 0.22uF 20% 6.3V CERM 402

C144 0.22uF 20% 6.3V CERM 402 · C246 0.22uF 20% 6.3V CERM 402 · C211 0.22uF 20% 6.3V CERM 402 · C263 0.22uF 20% 6.3V CERM 402 · C180 0.22uF 20% 6.3V CERM 402 · C213 0.22uF 20% 6.3V CERM 402 · C197 0.22uF 20% 6.3V CERM 402 · C208 0.22uF 20% 6.3V CERM 402 · C214 0.22uF 20% 6.3V CERM 402

INTREPID 3.3V DECOUPLING

57 Balls
4 X 10UF (0805)
72 X 0.22UF (0402)

+3V_MAIN

C164 10uF 20% 6.3V CERM 805 · C395 10uF 20% 6.3V CERM 805 · C375 0.22uF 20% 6.3V CERM 402 · C351 0.22uF 20% 6.3V CERM 402 · C53 0.22uF 20% 6.3V CERM 402 · C42 0.22uF 20% 6.3V CERM 402 · C21 0.22uF 20% 6.3V CERM 402 · C185 0.22uF 20% 6.3V CERM 402 · C31 0.22uF 20% 6.3V CERM 402 · C143 0.22uF 20% 6.3V CERM 402 · C123 0.22uF 20% 6.3V CERM 402 · C121 0.22uF 20% 6.3V CERM 402

C10 10uF 20% 6.3V CERM 805 · C9 10uF 20% 6.3V CERM 805 · C33 0.22uF 20% 6.3V CERM 402 · C184 0.22uF 20% 6.3V CERM 402 · C43 0.22uF 20% 6.3V CERM 402 · C35 0.22uF 20% 6.3V CERM 402 · C261 0.22uF 20% 6.3V CERM 402 · C60 0.22uF 20% 6.3V CERM 402 · C52 0.22uF 20% 6.3V CERM 402 · C199 0.22uF 20% 6.3V CERM 402 · C57 0.22uF 20% 6.3V CERM 402 · C19 0.22uF 20% 6.3V CERM 402

C16 0.22uF 20% 6.3V CERM 402 · C108 0.22uF 20% 6.3V CERM 402 · C55 0.22uF 20% 6.3V CERM 402 · C32 0.22uF 20% 6.3V CERM 402 · C125 0.22uF 20% 6.3V CERM 402 · C45 0.22uF 20% 6.3V CERM 402 · C76 0.22uF 20% 6.3V CERM 402 · C277 0.22uF 20% 6.3V CERM 402 · C28 0.22uF 20% 6.3V CERM 402 · C26 0.22uF 20% 6.3V CERM 402

C34 0.22uF 20% 6.3V CERM 402 · C23 0.22uF 20% 6.3V CERM 402 · C120 0.22uF 20% 6.3V CERM 402 · C146 0.22uF 20% 6.3V CERM 402 · C141 0.22uF 20% 6.3V CERM 402 · C30 0.22uF 20% 6.3V CERM 402 · C145 0.22uF 20% 6.3V CERM 402 · C96 0.22uF 20% 6.3V CERM 402 · C54 0.22uF 20% 6.3V CERM 402 · C50 0.22uF 20% 6.3V CERM 402

C75 0.22uF 20% 6.3V CERM 402 · C122 0.22uF 20% 6.3V CERM 402 · C51 0.22uF 20% 6.3V CERM 402 · C59 0.22uF 20% 6.3V CERM 402 · C163 0.22uF 20% 6.3V CERM 402 · C126 0.22uF 20% 6.3V CERM 402 · C98 0.22uF 20% 6.3V CERM 402 · C109 0.22uF 20% 6.3V CERM 402 · C56 0.22uF 20% 6.3V CERM 402 · C27 0.22uF 20% 6.3V CERM 402

C296 0.22uF 20% 6.3V CERM 402 · C248 0.22uF 20% 6.3V CERM 402 · C210 0.22uF 20% 6.3V CERM 402 · C58 0.22uF 20% 6.3V CERM 402 · C22 0.22uF 20% 6.3V CERM 402 · C20 0.22uF 20% 6.3V CERM 402 · C61 0.22uF 20% 6.3V CERM 402 · C44 0.22uF 20% 6.3V CERM 402 · C29 0.22uF 20% 6.3V CERM 402 · C24 0.22uF 20% 6.3V CERM 402

C183 0.22uF 20% 6.3V CERM 402 · C18 0.22uF 20% 6.3V CERM 402 · C49 0.22uF 20% 6.3V CERM 402 · C36 0.22uF 20% 6.3V CERM 402 · C17 0.22uF 20% 6.3V CERM 402 · C99 0.22uF 20% 6.3V CERM 402 · C396 0.22uF 20% 6.3V CERM 402 · C124 0.22uF 20% 6.3V CERM 402 · C127 0.22uF 20% 6.3V CERM 402 · C100 0.22uF 20% 6.3V CERM 402

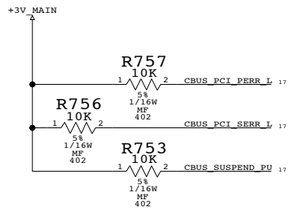
Intrepid Decoupling

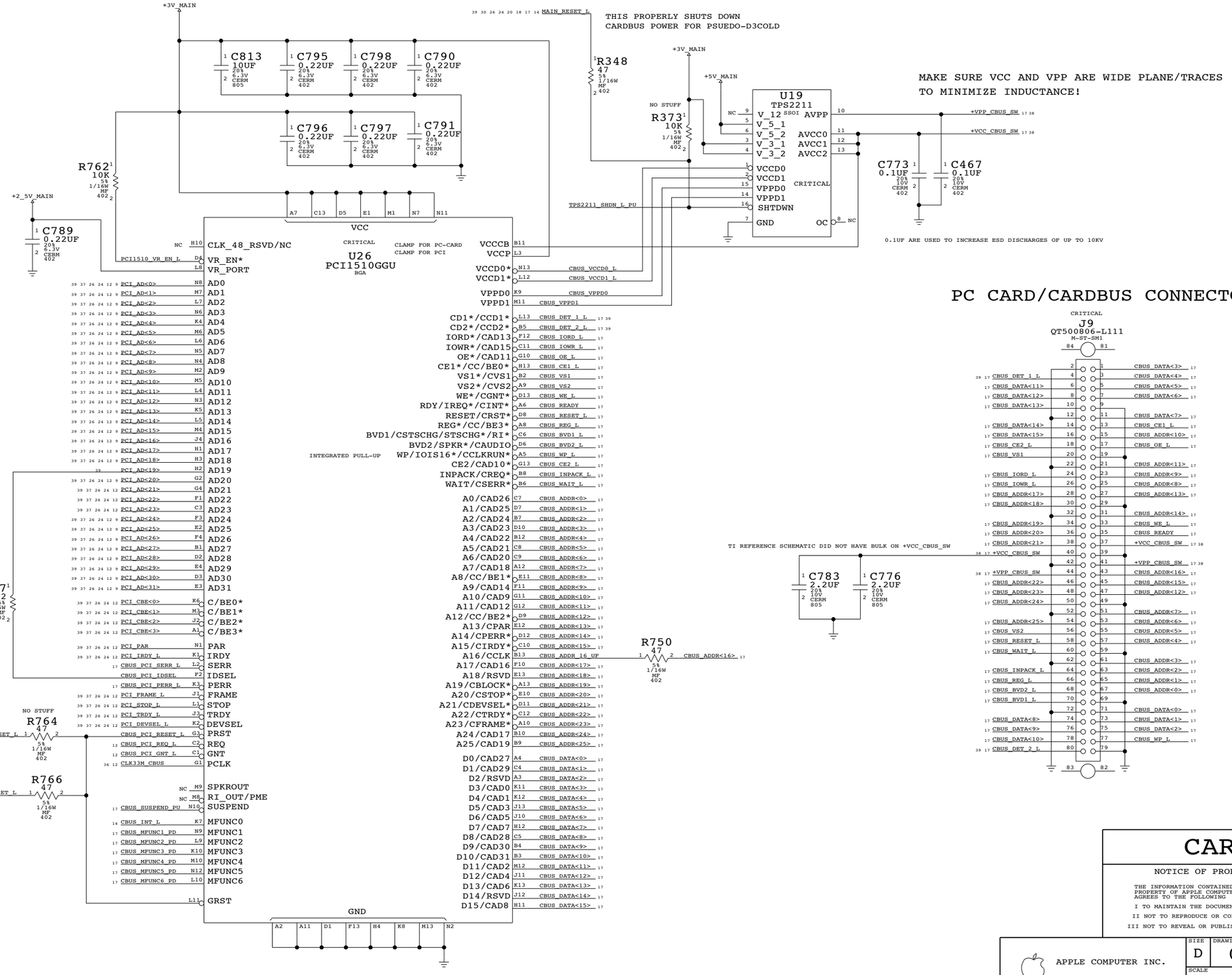
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7202	B

SCALE	SHT	OF
NONE	16	44

PCI1510 PULL-UPS





PC CARD/CARDBUS CONNECTOR

CARDBUS

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SIZE	DRAWING NUMBER	REV.
D	051-7202	B
SCALE: NONE	SHT 17 OF 44	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0158	1	IC,ATI,M11-CSP128,GC,GPHCTRL,667B	U44	CRITICAL	M11_CSP128
338S0154	1	IC,ASSP,ATI,M11-CSP64,HYN,A16,667BGA	U44	CRITICAL	M11_CSP64

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0214	338S0158	M11_CSP128	U44	ALT FOR A16
338S0207	338S0154	M11_CSP64	U44	ALT FOR A16

U44
RAGE_MOBILITY
M11-CSP64
64MB
BGA
(1 OF 6)

AD31 AGP_AD<31> 37 12
AD30 AGP_AD<30> 37 12
AD29 AGP_AD<29> 37 12
AD28 AGP_AD<28> 37 12
AD27 AGP_AD<27> 37 12
AD26 AGP_AD<26> 37 12
AD25 AGP_AD<25> 37 12
AD24 AGP_AD<24> 37 12
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AD8 AGP_AD<8> 37 12
AD7 AGP_AD<7> 37 12
AD6 AGP_AD<6> 37 12
AD5 AGP_AD<5> 37 12
AD4 AGP_AD<4> 37 12
AD3 AGP_AD<3> 37 12
AD2 AGP_AD<2> 37 12
AD1 AGP_AD<1> 37 12
AD0 AGP_AD<0> 37 12

CBEB3 AGP_CBE<3> 37 12
CBEB2 AGP_CBE<2> 37 12
CBEB1 AGP_CBE<1> 37 12
CBEB0 AGP_CBE<0> 37 12
PCICLK CLK66M_GPU_AGP 36 12
FRAMEB AGP_FRAME_L 37 12
IRDYB AGP_IRDY_L 37 12
TRDYB AGP_TRDY_L 37 12
STOPB AGP_STOP_L 37 12
DEVSELB AGP_DEVSEL_L 37 12
PAR AGP_PAR 37 12
REQB AGP_REQ_L 37 12
GNTB AGP_GNT_L 37 12
INTAB AGP_INT_L 14
RSTB AGP_ATI_RESET_L
WBF AGP_WBF_L 12
VREFG AGP_ATI_VREFG
MVREF AGP_ATI_VREF

AD_STB0 N29 AGP_AD_STB<0> 12 37
AD_STB1 W29 AGP_AD_STB<1> 12 37
AD_STBB0 M28 AGP_AD_STB_L<0> 12 37
AD_STBB1 Y29 AGP_AD_STB_L<1> 12 37
AGP_BUSYB AG28 AGP_BUSY_L 12
AGPREF K30
AGPTEST K29 GPU_AGP_TEST
AGP8X_DETB U25 AGP8X_DET_PU
SUS_STAT AJ28 AGP_SUS_STAT_L_PU
ST0 AF30 AGP_ST<0> 12
ST1 AF28 AGP_ST<1> 12
ST2 AE29 AGP_ST<2> 12
SBA7 AC28 AGP_SBA<7> 12 37
SBA6 AB29 AGP_SBA<6> 12 37
SBA5 AC27 AGP_SBA<5> 12 37
SBA4 AC30 AGP_SBA<4> 12 37
SBA3 AD27 AGP_SBA<3> 12 37
SBA2 AD30 AGP_SBA<2> 12 37
SBA1 AE28 AGP_SBA<1> 12 37
SBA0 AD29 AGP_SBA<0> 12 37
RBFB AE30 AGP_RBF_L 12 37
STP_AGPB AG29 AGP_STP_L
SB_STB AC29 AGP_SB_STB 12 37
SB_STBS AD28 AGP_SB_STB_L 12 37
RSTB_MSK AD24 ATI_RSTB_MSK
DBI_LO Y25 ATI_DBI_LO_PU
DBI_HI Y27 ATI_DBI_HI_PU

OMIT

38 21 19 18 12 +3V_GPU
38 21 19 18 16 15 12 +1_5V_AGP
R119 1 47 5% 1/16W MF 402
R127 1 10K 5% 1/16W MF 402
R159 1 20K 5% 1/16W MF 402
INT_AGP_VREF 12 38
C62 1 0.1uF 20% 10V CERM 402
C63 1 0.01uF 20% 16V CERM 402
(PLACE C1002 CLOSE TO AGPREF PIN)
38 21 19 18 12 +3V_GPU
R172 1 20K 5% 1/16W MF 402
R158 0 5% 1/16W MF 402
38 21 19 18 12 +3V_GPU
MAIN_RESET_L IS TOGGLED FOR SLEEP
R54 1 10K 5% 1/16W MF 402
R53 47 5% 1/16W MF 402
24 20 17 14 39 30 26 MAIN_RESET_L
21 19 18 12 38 +3V_GPU
R43 1 1K 1% 1/16W MF 402
R44 1 1K 1% 1/16W MF 402
38 21 16 +GPU_MEM
R45 1 1K 1% 1/16W MF 402
R46 1 1K 1% 1/16W MF 402
PLACE VERF VOLTAGE DIVIDER CLOSE TO ATI M10 VREF PIN
C11 1 0.1uF 20% 10V CERM 402
C37 1 10uF 20% 6.3V CERM 805
38 21 19 18 12 +1_5V_AGP
R126 1 47K 5% 1/16W MF 402
R138 1 47K 5% 1/16W MF 402
38 21 20 19 +1_8V_GPU
ATI_MEMIO_LO R55 1 4.7K 5% 1/16W MF 402
ATI_MEMIO_HI R104 4.7K 5% 1/16W MF 402
ATI_MEMVMODE0 B7 MEMVMODE0
ATI_MEMVMODE1 B6 MEMVMODE1
ATI_MEMIO_HI R70 1 4.7K 5% 1/16W MF 402
ATI_MEMIO_LO R105 4.7K 5% 1/16W MF 402
FOR 2.5 VDDR1
MEMVMODE0=1.8V
MEMVMODE1=GND
FOR 1.8 VDDR1
MEMVMODE0=GND
MEMVMODE1=1.8V
TEST_VCLK J6
TEST_MLCK C8 ATI_MEMTEST
MEMTEST
PLLTEST AC22 NC
R118 1 45.3 1% 1/16W MF 402
D+ AC10 GPU_THERM_DP_TP
D- AC11 GPU_THERM_DM_TP
E8 +GPU_MEM 18 21 38
(PULL-UP to GPU_MEM_IO)

U44
RAGE_MOBILITY
M11-CSP64
64MB
BGA
(6 OF 6)

OMIT

M2 P3 A21 B19 M15 N15 P15 R15 T15 T12 T13 T14 W16 V16 U16 T16 R16 R17 R18 R19 U6 AE15 F18 P25 VSS VDDCI

39 38 19 GPU_VCORE
L2
60-OHM-EMI
SM
38 GPU_VCORE_VDDCI
C64 0.01uF 20% 16V CERM 402
C67 10uF 20% 6.3V CERM 805
C65 0.01uF 20% 16V CERM 402
C68 0.01uF 20% 16V CERM 402
C66 0.01uF 20% 16V CERM 402
C69 0.01uF 20% 16V CERM 402

U44
RAGE_MOBILITY
M11-CSP64
64MB
BGA
(2 OF 6)

B26 A26 B25 A25 C22 D21 C21 D20 C20 D22 C23 D23 A27 B27 H2 H1 J2 J1 K4 K3 L4 M3 L3 M4 N2 N1 N4 N3 G30 G28 B30 D26 D16 B15 D11 B10 D5 B3 G3 E1 U1 V3 AB1 AC3 J30 J29 H30 H29 F30 F29 E30 E29 J28 J27 H28 H27 F28 F27 E28 E27 D30 D29 C30 C29 A30 A29 A28 B28 D28 C28 D27 C27 D25 C25 D24 C24 D18 C18 D17 C17 D15 C15 D14 C14 B17 VSS

OMIT

A17 B16 A16 B14 A14 B13 A13 D13 C13 D12 C12 D10 C10 D9 C9 B12 A12 B11 A11 B9 A9 B8 A8 C7 D7 C6 D6 C4 D4 C3 D3 A5 B5 A4 B4 A2 B2 A1 B1 E4 E3 F3 F4 H3 H4 J3 J4 C1 C2 D1 D2 F1 F2 G1 G2 R1 R2 T1 T2 V1 V2 W1 W2 T3 T4 U3 U4 W3 W4 Y3 Y4 Y1 Y2 AA1 AA2 AC1 AC2 AD1 AD2 AA3 AA4 AB3 AB4 AD3 AD4 AE3 AE4 VSS

27M OSC

(PLACE THE OSCILLATOR AND R189 AND R195 CLOSE TO ATI PIN AJ29)

+3V_SLEEP
L4
FERR-EMI-100-OHM
SM
38 +3V_ATI_OSC_SLEEP
C77 1 0.1uF 20% 10V CERM 402
C78 1 4.7uF 20% 6.3V CERM 805
NO STUFF
R188 1 100K 5% 1/16W MF 402
CRITICAL
G2
27.0000M
OSC SM-1
VCC
OE
OUT
GND
ATI_OSC_OE
ATI_CLK27M_OSC
(PLACE R200 CLOSE TO OSC)
GPU_SS
R200 0 5% 1/16W MF 402
ATI_CLK27M_OSC_SS 18
R189 1 287 1% 1/16W MF 402
R195 1 162 1% 1/16W MF 402
ATI_CLK27M_IN 19

S0=1;S1=M => -1.5% DOWN-SPREAD
SPREAD SPECTRUM SUPPORT

+3V_SLEEP
GPU_SS
L3
FERR-EMI-100-OHM
SM
38 +3V_ATI_SS
GPU_SS C70 10uF 20% 6.3V CERM 805
GPU_SS C71 0.1uF 20% 10V CERM 402
NO STUFF
R173 1 0 5% 1/16W MF 402
GPU_SS
R181 1 0 5% 1/16W MF 402
18 ATI_CLK27M_OSC_SS
GPU_SS 7 CRITICAL
VDD
U47
CY25811
SOI
XIN/CLKIN
XOUT
SSCLK
ATI_SSCLK_UF
NC
FRSEL
S1
S0
VSS
CY25811_S1
CY25811_S0
GPU_SS
R201 1 33 5% 1/16W MF 402
ATI_SSCLK_IN 19
NO STUFF
R37 1 0 5% 1/16W MF 402
NO STUFF
R38 1 0 5% 1/16W MF 402

M10 AGP INTERFACE

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SIZE	DRAWING NUMBER	REV.
D	051-7202	B
SCALE: NONE	SHT 18 OF 44	

TMDS TERMINATION

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN
CMF LINE SHOULD BE ROUTED AS 4MIL SURFACE
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS

EXT_TMDS R228 10K 5% 1/16W MF 402 — +1_8V_GPU
INT_TMDS R234 10K 5% 1/16W MF 402 — +3V_GPU
ZV_LCDDATA20_PU

R221 1K 5% 1/16W MF 402 — +3V_GPU
R223 10K 5% 1/16W MF 402 — NO STUFF

R229 1K 5% 1/16W MF 402 — ATI_TESTEN

U44 RAGE_MOBILITY M11-CSP64 64MB BGA (3 OF 6)

GPU_DVOD<0>	AJ5	ZV_LCDDATA0
GPU_DVOD<1>	AK5	ZV_LCDDATA1
GPU_DVOD<2>	AG6	ZV_LCDDATA2
GPU_DVOD<3>	AH6	ZV_LCDDATA3
GPU_DVOD<4>	AJ6	ZV_LCDDATA4
GPU_DVOD<5>	AK6	ZV_LCDDATA5
GPU_DVOD<6>	AG7	ZV_LCDDATA6
GPU_DVOD<7>	AH7	ZV_LCDDATA7
GPU_DVOD<8>	AJ7	ZV_LCDDATA8
GPU_DVOD<9>	AK7	ZV_LCDDATA9
GPU_DVOD<10>	AG8	ZV_LCDDATA10
GPU_DVOD<11>	AH8	ZV_LCDDATA11
NC	AJ8	ZV_LCDDATA12
NC	AK8	ZV_LCDDATA13
NC	AG9	ZV_LCDDATA14
NC	AH9	ZV_LCDDATA15
NC	AJ9	ZV_LCDDATA16
NC	AK9	ZV_LCDDATA17
NC	AG10	ZV_LCDDATA18
NC	AH10	ZV_LCDDATA19
	AJ10	ZV_LCDDATA20
NC	AK10	ZV_LCDDATA21
NC	AG11	ZV_LCDDATA22
NC	AH11	ZV_LCDDATA23
GPU_DVO_VSYNC	AJ4	ZV_LCDCNTL0
GPU_DVO_HSYNC	AK4	ZV_LCDCNTL1
GPU_DVOD_DE	AH5	ZV_LCDCNTL2
GPU_DVO_CLKP	AG5	ZV_LCDCNTL3
ATI_AGP_FBSKEW<0>	AJ2	GPIO0
ATI_AGP_FBSKEW<1>	AK2	GPIO1
ATI_X1CLK_SKEW<0>	AK1	GPIO2
ATI_X1CLK_SKEW<1>	AH3	GPIO3
ATI_BUS_CFG<0>	AH2	GPIO4
ATI_BUS_CFG<1>	AJ1	GPIO5
ATI_BUS_CFG<2> (NO ICT TEST)	AF4	GPIO6
ATI_GPIO7_SPN	AH1	GPIO7
ATI_GPIO8_RD (NO ICT TEST)	AG3	GPIO8
ATI_GPIO9_SPN (NO ICT TEST)	AF3	GPIO9
ATI_GPIO10_SPN (NO ICT TEST)	AG2	GPIO10
ATI_GPIO11_SPN (NO ICT TEST)	AF2	GPIO11
ATI_GPIO12_SPN (NO ICT TEST)	AG1	GPIO12
ATI_GPIO13_SPN	AF1	GPIO13
HPD_PWR_SNS_EN	AE2	GPIO14
GPU_VCORE_CNTL_L	AE1	GPIO15
ATI_SSCLK_IN	M1	GPIO16
ATI_TMDS_DN<0>	AJ13	TX0M
ATI_TMDS_DP<0>	AK13	TX0P
ATI_TMDS_DN<1>	AJ14	TX1M
ATI_TMDS_DP<1>	AK14	TX1P
ATI_TMDS_DN<2>	AJ15	TX2M
ATI_TMDS_DP<2>	AK15	TX2P
ATI_TMDS_CLKN	AJ12	TXCM
ATI_TMDS_CLKP	AK12	TXCP
ATI_CLK27M_IN	AJ29	XTALIN
NC	AJ30	XTALOUT
ATI_TESTEN	AH24	TESTEN
NC	AJ26	SSIN
	B24	VSS
	B20	VSS
	A24	VSS

OMIT

ROMCSB	AE5 NC	
R	AK28	GPU_R
G	AK27	GPU_G
B	AK26	GPU_B
VSYNC	AG27	ATI_VSYNC
V2SYNC	AG25 NC	
HSYNC	AG26	ATI_HSYNC
H2SYNC	AG24 NC	
RSET	AK25	ATI_RSET
R2SET	AJ24	ATI_R2SET
Y_G	AK23	GPU_Y
C_R	AK24	GPU_C
COMP_R	AK22	GPU_COMP
DIGON	AE13	FP_PWR_EN
BLON	AF13	INV_ON_PWM
HPD1	AF11	+3V_GPU
AUXWIN	AJ27	GPU_AUXWIN
DDC1DATA	AH28	GPU_DVI_DDC_DATA
DDC1CLK	AH27	GPU_DVI_DDC_CLK
DDC2DATA	AE12	LVDS_DDC_DATA
DDC2CLK	AF12	LVDS_DDC_CLK
DDC3DATA	AH26	SI_DDC_DATA
DDC3CLK	AH25	SI_DDC_CLK
TXOUT_U0N	AH18	LVDS_U0N
TXOUT_U0P	AG18	LVDS_U0P
TXOUT_U1N	AH19	LVDS_U1N
TXOUT_U1P	AG19	LVDS_U1P
TXOUT_U2N	AH20	LVDS_U2N
TXOUT_U2P	AG20	LVDS_U2P
TXOUT_U3N	AH22	LVDS_U3N_TP (NO ICT TEST)
TXOUT_U3P	AG22	LVDS_U3P_TP (NO ICT TEST)
TXCLK_UN	AH21	CLKLVDS_UN
TXCLK_UP	AG21	CLKLVDS_UP
TXOUT_L0N	AK16	LVDS_L0N
TXOUT_L0P	AJ16	LVDS_L0P
TXOUT_L1N	AK17	LVDS_L1N
TXOUT_L1P	AJ17	LVDS_L1P
TXOUT_L2N	AK18	LVDS_L2N
TXOUT_L2P	AJ18	LVDS_L2P
TXOUT_L3N	AK20	LVDS_L3N_TP (NO ICT TEST)
TXOUT_L3P	AJ20	LVDS_L3P_TP (NO ICT TEST)
TXCLK_LN	AK19	CLKLVDS_LN
TXCLK_LP	AJ19	CLKLVDS_LP
SSOUT	AJ25 NC	
VSS	A20	
VSS	B21	

R240 75 1% 1/16W MF 402 — ATI_VSYNC
R246 75 1% 1/16W MF 402 — GPU_R
R249 75 1% 1/16W MF 402 — ATI_HSYNC
R256 715 1% 1/16W MF 402
R257 499 1% 1/16W MF 402
R245 75 1% 1/16W MF 402 — GPU_G
R248 75 1% 1/16W MF 402 — GPU_B
R254 75 1% 1/16W MF 402 — GPU_COMP
R711 10K 5% 1/16W MF 402 — +3V_GPU
R247 10K 5% 1/16W MF 402 — GPU_AUXWIN
R253 10K 5% 1/16W MF 402

Q77 SI3446DV TSOP

+1_5V_AGP → GPU_CORE_OK

L24 FERR-220-OHM 0805

+5V_GPU_VDD15 (500mA) → +GPU_VDD15_UF

C166 1000pF 10% 25V X7R 402

C222 C256 C299 C305 C328 — 0.01uF 20% 16V CERM 402 / 10uF 20% 6.3V CERM 805
C232 C269 C300 C306 — 0.01uF 20% 16V CERM 402

U44 RAGE_MOBILITY M11-CSP64 64MB BGA (5 OF 6)

F12	VDD15
L6	
T6	
AB6	
F17	
G25	
R25	
AB25	
AJ3	
AF25	
AG4	
AH4	
AF5	
F6	
G6	
H6	
P6	
AD26	
V6	
W6	
AC6	
AD6	
AE6	
F7	
F10	
AE10	
F11	
AE11	
F13	VDDC
F14	
AE14	
AF14	
W26	
AF15	
AE17	
AC25	
AE18	
F23	
F24	
AE24	
F25	
M25	
N25	
W25	
V25	

OMIT

G7	VSS
G8	
G9	
G10	
G11	
G12	
G13	
G14	
G15	
G16	
G17	
G18	
G19	
G20	
G21	
G22	
G23	
G24	
H7	
H8	
H23	
H24	
J7	
J24	
K7	
K24	
L7	
L24	
M7	
M24	
N7	
N24	
P7	
P24	
R7	
R24	
T7	
T24	
U7	
U24	
V7	
V24	
W7	
W24	
Y7	
Y24	
AA7	
AA24	
AB7	
AB24	
AC7	
AC8	
AC23	
AC24	
AD7	
AD8	
AD9	
AD10	
AD11	
AD12	
AD13	
AD14	
AD15	
AD16	
AD17	
AD18	
AD19	
AD20	
AD21	
AD22	
AD23	

GPU VCORE - 1.2V

(PUT ALL CAPs BELOW ATI ASIC)

GPU_VCORE

C167 C219 C252 C270 C301 C307 C329 C332 — 10uF 20% 6.3V CERM 805 / 0.22uF 20% 6.3V CERM 402
C186 C220 C253 C271 C302 C311 C330 C333 — 0.22uF 20% 6.3V CERM 402
C187 C221 C254 C282 C303 C326 C331 C338 — 0.22uF 20% 6.3V CERM 402

M10 Power Shut down Sequencing

XW21 SM — DP6 BAS16TW SOT-363 — +1_8V_ATI_PVDD
XW20 SM — DP6 BAS16TW SOT-363 — +1_8V_PVDD_NECK
XW22 SM — DP6 BAS16TW SOT-363 — +GPU_VDD15_UF / +GPU_VDD15_NECK
XW24 SM — +2_5V_SLEEP
XW23 SM — +1_5V_AGP_NECK

R258 R260 R262 R265 R269 R271 R273 — 10K 5% 1/16W MF 402 — NO STUFF
R259 R261 R263 R266 R270 R272 R274 — 10K 5% 1/16W MF 402 — NO STUFF

(GPIO0) ATI_AGP_FBSKEW<0>
(GPIO1) ATI_AGP_FBSKEW<1>
(GPIO2) ATI_X1CLK_SKEW<0>
(GPIO3) ATI_X1CLK_SKEW<1>
(GPIO4) ATI_BUS_CFG<0>
(GPIO5) ATI_BUS_CFG<1>
(GPIO6) ATI_BUS_CFG<2>

GPU VCORE SUPPLY

WHEN VCORE_CNTL HIGH => 1.2V
1.2V = 0.8V * (1 + R332 / (R331//R333))

WHEN VCORE_CNTL LOW => 1.0V
1.0V = 0.8V * (1 + R332 / R333)

+PBUS

R389 1M 5% 1/16W MF 402
R430 1 5% 1/16W MF 603
R339 576K 1% 1/16W MF 402

C762 C766 — 4.7UF 20% 25V CERM 1206

Q51 SI7860DP SO-8-PWRPK CRITICAL

L30 2.1UH-11A SM — CRITICAL

D24 SMB B340LB

Q48 SI7892DP SO-8-PWRPK — CRITICAL — NO STUFF

C882 0.0022UF 10% 50V CERM 402

R352 4.99K 1% 1/16W MF 402
R451 18.2K 1% 1/16W MF 402
R351 20K 1% 1/16W MF 402
R804 1.82K 1% 1/16W MF 402

C708 22uF 20% 10V CERM 1210
C719 330UF 20% 6.3V POLY SMD
C721 330UF 20% 6.3V POLY SMD
C720 330UF 20% 6.3V POLY SMD

R307 100K 5% 1/16W MF 402
C902 0.1UF 20% 10V CERM 402
Q80 2N7002DW SOT-363
R410 10K 5% 1/16W MF 402
C515 0.1UF 10% 10V CERM 402

R388 0 5% 1/16W MF 402 — NO STUFF
R341 63.4K 1% 1/16W MF 402 — NO STUFF
C473 4.7UF 20% 10V CERM 1206
C494 0.1UF 20% 25V CERM 603
R416 2.2 5% 1/16W MF 603
C514 0.1UF 20% 25V CERM 603
D5 MBR0540 SM

R306 100K 5% 1/16W MF 402
R316 100K 5% 1/16W MF 402
DP1 BAS16TW SOT-363 — SLEEP_L_LS5
DP1 BAS16TW SOT-363 — DCDC_EN
R390 0 5% 1/16W MF 402 — 1778_SHDN_L_D3COLD
R294 10K 5% 1/16W MF 402
Q6 2N3904 SM — GPU_VCORE_PWR_SEQ
Q5 2N3904 SM — GPU_VCORE_SEQ_L
R203 33K 5% 1/16W MF 402

R236 100K 5% 1/16W MF 402 — 1778_SHDN_L
R340 20K 1% 1/16W MF 402 — 1778_ITH_RC
C448 470PF 10% 50V CERM 402
C451 220PF 5% 25V CERM 402
R311 0 5% 1/16W MF 402
R332 0 5% 1/16W MF 402
C483 0.1UF 20% 10V CERM 402

U16 LTC1778 SSOP — CRITICAL

EXT_VCC	9	
INT_VCC	11	
VIN	10	
RUN/SS	1	
ITH	5	1778_ITH
VRNG	3	1778_VRNG
FCB	4	1778_FCB
PGOOD	2	GPU_CORE_OK
SGND	6	
PGND	13	
ION	7	1778_ION
BOOST	16	1778_BST
TG	15	1778_TG
SW	14	
BG	12	1778_BG
VFB	8	1778_VFB

1778_BST_RC

+5V_MAIN
+3V_GPU
+2_5V_SLEEP
+1_5V_AGP
+1_8V_ATI_PVDD
+1_8V_PVDD_NECK
+GPU_VDD15_UF
+GPU_VDD15_NECK
GPU_VCORE
GPU_VCORE_NECK
GPU_CORE_OK
+1_5V_AGP_NECK
GPU_VCORE_SW
1778_VCC
1778_VIN
1778_VFB
GPU_VCORE_CNTL_L
VCORE_CNTL_RC
GPU_VCORE_CNTL
HIGH_VCORE_DIV
HIGH_VCORE
GPU_PWRMSR

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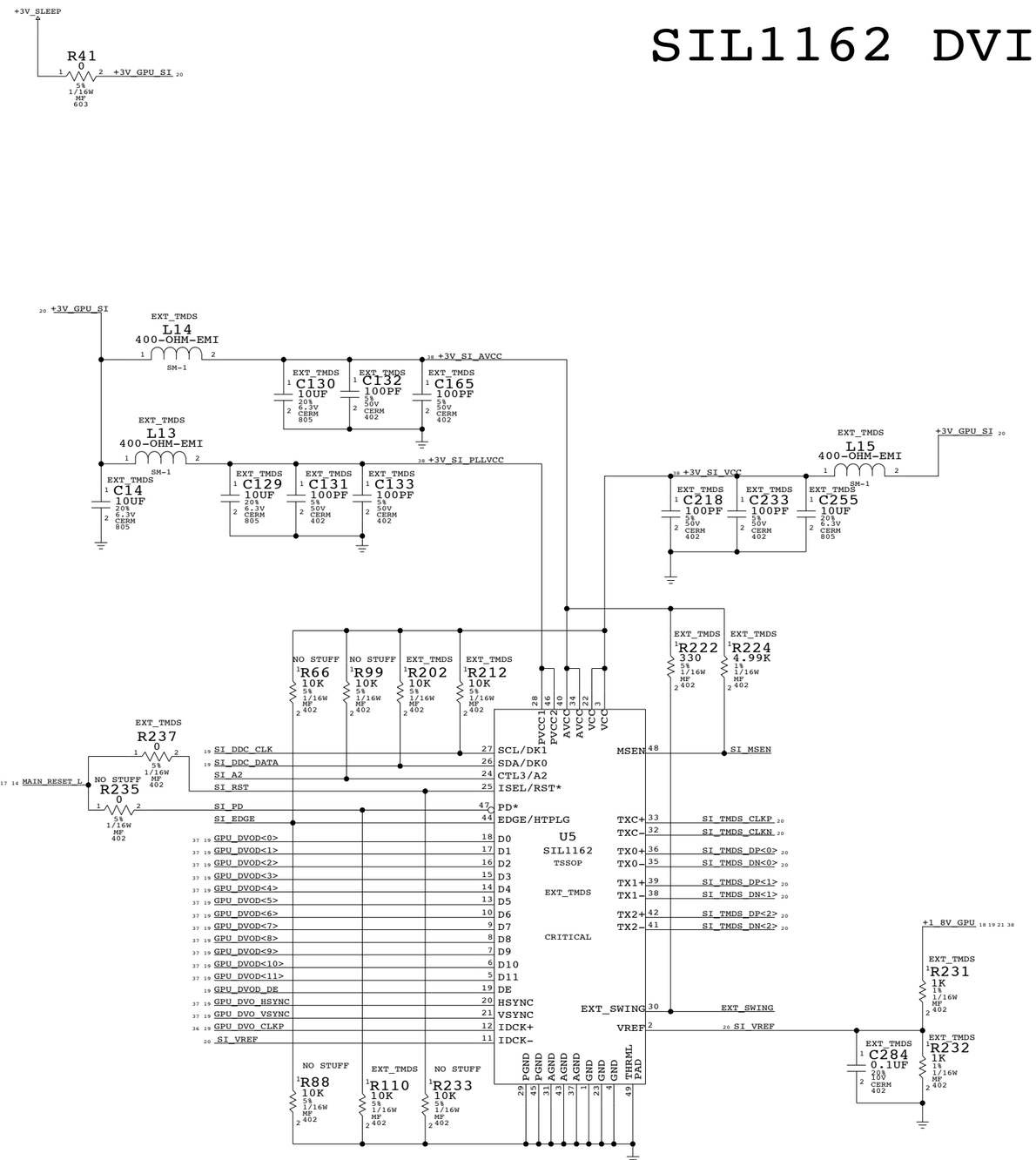
SIZE	DRAWING NUMBER	REV.
D	051-7202	B
SCALE: NONE	SHT 19 OF 44	

SIL1162 DVI TRANSMITTER



APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7202	B
	SCALE	SHT OF	
	NONE	20 44	

GPU PLL - 1.8V

U55 MM1571J (100mA MAX) SOT-25A CRITICAL — VIN, VOUT, CONT, NOISE, GND, ATI_PVDD_BYP

(Total PVDD = 66mA)

C889 1UF 10% 6.3V CERM 603 — C379 0.01uF 20% 16V CERM 402 — C380 10uF 20% 6.3V CERM 805

L65 FERR-220-OHM 0402 — C438 10uF 20% 6.3V CERM 805 — C865 0.1uF 20% 10V CERM 402 — C716 0.01uF 20% 16V CERM 402 (21mA)

L58 FERR-220-OHM 0402 (140mA) — C360 10uF 20% 6.3V CERM 805 — C364 0.01uF 20% 16V CERM 402 — C374 0.01uF 20% 16V CERM 402

L66 FERR-220-OHM 0402 — C415 10uF 20% 6.3V CERM 805 — C437 0.01uF 20% 16V CERM 402 — C870 0.01uF 20% 16V CERM 402 (AVDD+VDDDI=75mA)

L55 FERR-220-OHM 0402 (2mA) — C339 10uF 20% 6.3V CERM 805 — C363 0.01uF 20% 16V CERM 402

L56 FERR-220-OHM 0402 (AVDD+VDDDI=75mA) — C358 10uF 20% 6.3V CERM 805 — C361 0.01uF 20% 16V CERM 402 — C372 0.01uF 20% 16V CERM 402

L57 FERR-220-OHM 0402 — C359 10uF 20% 6.3V CERM 805 — C362 0.01uF 20% 16V CERM 402 — C373 0.01uF 20% 16V CERM 402

R722 0 5% 1/10W FF 805 — +1_5V_AGP — 1.5V

R284 0 5% 1/10W FF 805 — +1_8V_GPU — 1.8V

R729 0 5% 1/4W FF 1210 — ATI_MEMIO_LO — 1.8V

R728 0 5% 1/4W FF 1210 — ATI_MEMIO_HI — 2.5V — +GPU_MEM

AGP 4X I/O - 1.5V

L59 FERR-10-OHM-500MA SM — C381 0.1uF 20% 10V CERM 402 — C420 0.1uF 20% 10V CERM 402 — C446 0.1uF 20% 10V CERM 402 — C543 0.1uF 20% 10V CERM 402 — C871 10uF 20% 6.3V CERM 805 (20mA)

C382 0.01uF 20% 16V CERM 402 — C421 0.01uF 20% 16V CERM 402 — C447 0.01uF 20% 16V CERM 402 — C671 0.01uF 20% 16V CERM 402

MEMORY CORE - 2.5V

L63 FERR-220-OHM 0805 — C383 0.1uF 20% 10V CERM 402 — C425 0.1uF 20% 10V CERM 402 — C866 0.1uF 20% 10V CERM 402 — C672 0.1uF 20% 10V CERM 402 — C715 10uF 20% 6.3V CERM 805 (1800mA)

C408 0.01uF 20% 16V CERM 402 — C426 0.01uF 20% 16V CERM 402 — C450 0.01uF 20% 16V CERM 402 — C701 0.01uF 20% 16V CERM 402

LVDS PLL - 1.8V

L61 FERR-220-OHM 0402 — C409 10uF 20% 6.3V CERM 805 — C428 0.1uF 20% 10V CERM 402 — C867 0.01uF 20% 16V CERM 402 (40mA)

MEMORY PLL - 1.8V

L62 FERR-220-OHM 0402 — C411 10uF 20% 6.3V CERM 805 — C429 0.01uF 20% 16V CERM 402 (20mA)

R279 0 5% 1/16W MF 603 — EXT_TMDS

C877 10uF 20% 6.3V CERM 805 — C878 0.01uF 20% 16V CERM 402

LVDS - 2.5V

L64 FERR-10-OHM-500MA SM — NO STUFF

L17 FERR-10-OHM-500MA SM

C412 10uF 20% 6.3V CERM 805 — C434 0.01uF 20% 16V CERM 402 — C868 0.01uF 20% 16V CERM 402 (350mA)

U8 MAX8860 UMAX — IN, OUT1, OUT2, SHDN*, SET, FAULT*, CC, GND — OMIT

C910 2.2UF 20% 6.3V CERM1 603 — C911 0.033UF 20% 10V X7R 402 — C912 2.2UF 20% 6.3V CERM1 603

R635 100K 5% 1/16W MF 402 — +2_8V_GPU_LVDS_LDO — MAX8860_CC — MAX8860_FAULT

LVDS/TMDS - 1.8V

L60 FERR-220-OHM 0402 (180mA)

C413 10uF 20% 6.3V CERM 805 — C435 0.1uF 20% 10V CERM 402 — C864 0.1uF 20% 10V CERM 402 — C704 0.1uF 20% 10V CERM 402

C414 0.1uF 20% 10V CERM 402 — C436 0.01uF 20% 16V CERM 402 — C869 0.01uF 20% 16V CERM 402

R721 0 5% 1/10W FF 805 — +2_5V_GPU — 2.5V

R299 0 5% 1/10W FF 805 — +3V_GPU — 3.3V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S0828	1	IC,MAX8860,LDO,2.77V	U8	?

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0647	353S0828	?	U8	ALT FOR 2.82V PART

GPU POWER SOURCES - 1.5V, 1.8V, 2.5V & 3.3V

GPU I/O

U44 RAGE_MOBILITY M11-CSP64 64MB BGA (4 OF 6) — OMIT

AK29 PVDD — AF23 AVDD0 — AF24 AVDD1 — AE21 A2VDD0 — AF21 A2VDD1 — AJ23 A2VDDQ — AH23 VDD1DI — AF20 VDD2DI — F19 VDDRH0 — N6 VDDRH1

K25 — L25 — T25 — Y28 — K27 — AA25 — K26 — L26 — M26 — N26 — P26 — R26 VDDP — T26 — U26 — V26 — Y26 — AA26 — AB26 — AC26

E5 — E6 — E12 — E13 — E18 VDDM — E19 — E20 — E26 — F26

E7 — H26 — E9 — E10 — E11 — E14 — E15 — E16 VDDR1 — E17 — E21 — E22 — E23 — E24 — E25

AK21 LPVDD — AK11 TPVDD — A7 MPVDD

AE16 LVDDR_18 — AF16 LVDDR_18 — AG16 LVDDR_25 — AF17 LVDDR_25

AG12 TXVDDR0 — AG13 TXVDDR1 — AG14 TXVDDR2 — AG15 TXVDDR3

PVSS AK30 — AVSSQ AF22 — A2VSSQ AJ22 — AVSSN0 AE22 — AVSSN1 AE23 — A2VSSN0 AE19 — A2VSSN1 AE20 — VSS1DI AG23 — VSS2DI AF19 — VSSRH0 F20 — VSSRH1 M6

F5 — G5 — H5 — J5 — K5 — L5 — M5 — N5 — P5 — R5 — T5 — U5 — V5 — W5 — Y5 — AA5 — AB5 — AC5 — AD5 — G26 — K6 — R6 — Y6 — AA6 — F8 — F9 — F15 — F16 — F21 — F22 — H25 — J25 — J26

VDDR1 — AF6 — AE7 — VDDR4 AF7 — AE8 — AF8 — AE9 — AF9 — AF10 — VDDR3 AD25 — AE25 — AE26 — AF26

LPVSS AJ21 — TPVSS AJ11 — MPVSS A6

LVSSR0 AH16 — LVSSR1 AG17 — LVSSR2 AH17 — LVSSR3 AF18

DVOVMODE AH12 — TXVSSR1 AH13 — TXVSSR2 AH14 — TXVSSR3 AH15

MEMORY I/O

U54 INT_TMDS CRITICAL MM1571J SOT-25A — VIN, VOUT, CONT, NOISE, GND, ATI_TPVDD_BYP

C879 1UF 10% 6.3V CERM 603 — C880 0.01UF 10% 16V CERM 402 — C881 10UF 20% 6.3V CERM 805

L69 FERR-220-OHM 0402 — +1_8V_GPU_TP_PLL

L67 FERR-220-OHM 0805 — +GPU_MEM

(1200mA) — +GPU_MEM_IO_FLT

C872 10uF 20% 6.3V CERM 805 — C875 0.1uF 20% 10V CERM 402 — C850 0.1uF 20% 10V CERM 402 — C855 0.1uF 20% 10V CERM 402 — C860 0.1uF 20% 10V CERM 402

C873 0.1uF 20% 10V CERM 402 — C876 0.1uF 20% 10V CERM 402 — C851 0.1uF 20% 10V CERM 402 — C856 0.1uF 20% 10V CERM 402 — C861 0.1uF 20% 10V CERM 402

C874 0.1uF 20% 10V CERM 402 — C847 0.1uF 20% 10V CERM 402 — C852 0.1uF 20% 10V CERM 402 — C857 0.1uF 20% 10V CERM 402 — C862 0.01uF 20% 16V CERM 402

L16 FERR-10-OHM-500MA SM — EXT_TMDS — +1_8V_GPU

+1_8V_DVO_F — C304 10uF 20% 6.3V CERM 805 — C327 0.1uF 20% 10V CERM 402 — C647 0.1uF 20% 10V CERM 402

R268 0 5% 1/16W MF 603 — INT_TMDS

L68 FERR-10-OHM-500MA SM — +3V_GPU

+3V_GPU_FLT — C722 10uF 20% 6.3V CERM 805 — C848 0.1uF 20% 10V CERM 402 — C853 0.1uF 20% 10V CERM 402 — C858 0.1uF 20% 10V CERM 402 — C863 0.1uF 20% 10V CERM 402

C725 0.1uF 20% 10V CERM 402 — C849 0.1uF 20% 10V CERM 402 — C854 0.1uF 20% 10V CERM 402 — C859 0.1uF 20% 10V CERM 402

R255 0 5% 1/16W MF 402 — EXT_TMDS — +1_8V_GPU

R251 0 5% 1/16W MF 402 — INT_TMDS

3.3V IO SUPPLY

(Max Current varies, depends on usage)

M10 SHUT DOWN POWER SEQUENCING

XW27 SM — +2_5V_SLEEP_NECK2 — DP7 BAS16TW SOT-363 — +3V_SLEEP_NECK — XW30 SM — OMIT

XW28 SM — +1_8V_SLEEP_NECK — DP7 BAS16TW SOT-363 — OMIT

XW29 SM — +1_5V_SLEEP_NECK — DP7 BAS16TW SOT-363 — OMIT

M10 POWER

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7202	B
SCALE: NONE	SHT 21 OF 44	

EXTERNAL VIDEO (DVI) INTERFACE

ANALOG FILTERING PLACE CLOSE TO CONNECTOR

FL2 CRITICAL LCFILTER SM-220MHZ — GPU_B → VGA_B
FL1 CRITICAL LCFILTER SM-220MHZ — GPU_G → VGA_G
FL3 CRITICAL LCFILTER SM-220MHZ — GPU_R → VGA_R
C685 3.3PF 0.25% 50V CERM 402
C676 3.3PF 0.25% 50V CERM 402
C684 3.3PF 0.25% 50V CERM 402

VGA VSYNC BUFFERS

+3V_MAIN
U56 CRITICAL 74AHC1G32 SM — ATI_HSYNC → R718 33 5% 1/16W MF 402 → VGA_HSYNC_BUF → VGA_HSYNC
U57 CRITICAL 74AHC1G32 SM — ATI_VSYNC → R714 33 5% 1/16W MF 402 → VGA_VSYNC_BUF → VGA_VSYNC

DVI DDC CURRENT LIMIT

(55mA requirement per DVI spec)

+5V_SLEEP → F1 0.5AMP-13.2V SM → +5V_DDC_SLEEP_UF → L23 400-OHM-EMI SM-1 → +5V_DDC_SLEEP

Isolation required for DVI power switch

D21 SM MBR0530 — DDC_CLK_ISO

R661 4.7K 5% 1/16W MF 402
R655 4.7K 5% 1/16W MF 402

J14 CRITICAL QH1112 F-RT-TH

TMDS_CONN_DN<0> TMDS_CONN_DP<0> TMDS_CONN_DN<2> TMDS_CONN_DN<1> TMDS_CONN_DP<2> TMDS_CONN_DP<1>
TMDS_DN<2> TMDS_DP<2> TMDS_DN<1> TMDS_DP<1>
TMDS_CONN_CLKP TMDS_CONN_CLKN
DVI_DDC_CLK_UF DVI_DDC_DATA_UF (+5V_DDC_SLEEP) DVI_HPD_UF
VGA_VSYNC VGA_R VGA_G VGA_B VGA_HSYNC

R670 100 5% 1/16W MF 402 — DVI_DDC_CLK
R649 100 5% 1/16W MF 402 — DVI_DDC_DATA
R650 100 5% 1/16W MF 402 — DVI_HPD

C706 100pF 5% 50V CERM 402
C669 100pF 5% 50V CERM 402
C710 0.01UF 20% 50V CERM 603
C1 100pF 5% 50V CERM 402

R706 0 5% 1/16W MF 402 — PLACE NEAR 3, 11 & 19
R1 0 5% 1/16W MF 402 — PLACE NEAR C5A & C5B

CHGND1 CHGND5

NOTE: Pulldown for DVI_HPD provided by DVI power switch interface

NOTE: DVI_HPD SHARES Q68 WITH ALS BECAUSE OF BOARD REAL ESTATE

3V LEVEL SHIFTERS

+3V_SLEEP

Q38 2N7002DW SOT-363 — DVI_DDC_CLK → GPU_DVI_DDC_CLK
Q38 2N7002DW SOT-363 — DVI_DDC_DATA → GPU_DVI_DDC_DATA
Q35 2N7002DW SOT-363 — DVI_HPD → GPU_HPD

R662 10K 5% 1/16W MF 402
R671 10K 5% 1/16W MF 402
R694 100K 5% 1/16W MF 402

DVI POWER SWITCH

Power key detect path when system is shutdown or asleep.. DDC_CLK is isolated from NV17M DURING SHUTDOWN. WHEN power key on remote device is pressed, 5V will be driven into DDC_CLK. Since host rails will be low, TP0610 will turn on, driving SOFT_PWR_ON_L low. As host rails rise, TP0610 will turn off, as will remote device path into DDC CLK. Isolation will be disabled as well.

Q40 TP0610 SM — DVI_DDC_CLK_UF, DVI_TURN_ON
R690 680 5% 1/16W MF 402
R691 10K 5% 1/16W MF 402 — DVI_TURN_ON_BASE, DVI_TRUN_ON_ILIM
Q42 2N3904 SM — SOFT_PWR_ON_L
R688 330 5% 1/16W MF 402 — Pulldown prevents 3904 from turning on when DVI monitor has active, self-powered DDC clock pullup.

Power key detect path when system is running. HPD normally driven to 3.3V. When power key on remote device pressed, HPD will be driven to 5V. COMPARATOR ENABLED BY NV17MAP GPIO.

+3V_SLEEP
R680 68.1K 1% 1/16W MF 402
C696 0.1UF 20% 10V CERM 402
HPD_4V_REF
U46 LMC7211 SM CRITICAL — V+, V−
DVI_HPD_UF → R663 10K 1% 1/16W MF 402 → DVI_HPD_DIV
R686 10K 1% 1/16W MF 402
R681 100K 1% 1/16W MF 402
HPD_PWR_SW
Q41 2N7002DW SOT-363 — HPD_ON
R703 330 5% 1/16W MF 402
+PBUS
Q45 TP0610 SM — COMP_ENABLE
R700 20K 5% 1/16W MF 402 — HPD_BASE
Q44 2N3904 SM — HPD_ON_RC
COMP_DISABLE
R696 100K 5% 1/16W MF 402
R704 100K 5% 1/16W MF 402
C703 47UF 20% 6.3V CERM 1210
R705 68K 5% 1/16W MF 402

NEED PULL-DOWN BECAUSE THIS SIGNAL IS TRISTATED INITIALLY

HPD_PWR_SNS_EN → R213 100K 5% 1/16W MF 402 → Q41 2N7002DW SOT-363

TMDS FILTERING PLACE CLOSE TO CONNECTOR

L72 CRITICAL 90-OHM-300MA 2012H — TMDS_DN<0> → TMDS_CONN_DN<0>
L73 CRITICAL 90-OHM-300MA 2012H — TMDS_DP<0> → TMDS_CONN_DP<0>
L21 CRITICAL 16?-OHM SM OMIT — TMDS_CLKP → TMDS_CONN_CLKP
L74 CRITICAL 90-OHM-300MA 2012H — TMDS_CLKN → TMDS_CONN_CLKN
L74 CRITICAL 90-OHM-300MA 2012H — TMDS_DN<2> → TMDS_CONN_DN<2>
L73 CRITICAL 90-OHM-300MA 2012H — TMDS_DP<2> → TMDS_CONN_DP<2>
L73 CRITICAL 90-OHM-300MA 2012H — TMDS_DN<1> → TMDS_CONN_DN<1>
L74 CRITICAL 90-OHM-300MA 2012H — TMDS_DP<1> → TMDS_CONN_DP<1>

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
155S0147	1	370OHM COMMON MODE CHOKE	L21	?

LCD INTERFACE

LVDS INTERFACE

100K pull-ups are for no-panel case (development) Panel has 2K pull-ups

C416 0.001uF 20% 50V CERM 402 — CHGND4

CRITICAL J6 G-501973 F-RT-SM

+3V_SLEEP
R342 100K 5% 1/16W MF 402
R320 100K 5% 1/16W MF 402
+3V_LCD — (LVDS DDC POWER) — NC
LVDS_DDC_CLK LVDS_DDC_DATA
NO STUFF
C449 0.001uF 20% 50V CERM 402
C452 0.001uF 20% 50V CERM 402 — CHGND4

LVDS_L0N LVDS_L0P LVDS_L1N LVDS_L1P LVDS_L2N LVDS_L2P CLKLVDS_LN CLKLVDS_LP LVDS_U0N LVDS_U0P LVDS_U1N LVDS_U1P LVDS_U2N LVDS_U2P CLKLVDS_UN CLKLVDS_UP

C500 0.001uF 20% 50V CERM 402 — CHGND4

LCD POWER SWITCHES

+3V_MAIN
R400 100K 5% 1/16W MF 402
C484 2200pF 5% 50V CERM 603
R391 100K 5% 1/16W MF 402 — LCD_PWREN_L
Q11 TSOP SI3443DV
+3V_LCD_SW
L6 FERR-250-OHM SM
C474 0.001uF 20% 50V CERM 402 — CHGND4
LCD_DIGON_L
Q8 2N7002 SM — FP_PWR_EN

INVERTER INTERFACE

+PBUS
L33 FERR-1K-OHM-EMI SM — +12_8V_INV
+5V_MAIN
Q7 FDG6324L SC70-6 — +5V_INV_UF_SW
L32 400-OHM-EMI SM-1 — +5V_INV_SW
R317 100K 5% 1/16W MF 402
C440 10UF 20% 6.3V CERM 805
FP_PWR_EN_L
Q7 FDG6324L SC70-6 — FP_PWR_EN
L31 400-OHM-EMI SM-1 — BRIGHT_PWM
C746 0.001UF 20% 50V CERM 402
C749 0.001UF 20% 50V CERM 402
C739 0.001UF 20% 50V CERM 402
CRITICAL J7 SM-2MT
+3V_PMU
C552 0.1UF 20% 10V CERM 402
INV_ON_PWM → U24 74LVC32 TSSOP → BRIGHT_PWM_UF
INVERTER EXPECTS ACTIVE HIGH SIGNAL

SHARES LOGIC WITH KB RESET SIGNALS (PG 28)

R724 0 5% 1/16W MF 402
C744 0.01uF 20% 50V CERM 603 — CHGND2

S-VIDEO/COMP OUT INTERFACE

Place GND shorts at graphics controller

XW12 SM — GPU_TV_GND1 → L26 FERR-10-OHM-500MA SM → TV_GND1
L25 3.3UH 0603 — GPU_Y → TV_C
L29 3.3UH 0603 — GPU_C → TV_Y
L27 3.3UH 0603 — GPU_COMP → TV_COMP
XW13 SM — GPU_TV_GND2 → L28 FERR-10-OHM-500MA SM → TV_GND2

C712 0.01UF 20% 50V CERM 603
C702 560PF 10% 50V CERM 402
C707 560PF 10% 50V CERM 402
C718 560PF 10% 50V CERM 402
C724 560PF 10% 50V CERM 402
C714 560PF 10% 50V CERM 402
C713 560PF 10% 50V CERM 402
C717 0.01UF 20% 50V CERM 603

CRITICAL J15 MINIDIN RT-TH MH1177

CHGND1

Place GND shorts at graphics controller

VIDEO CONNECTORS

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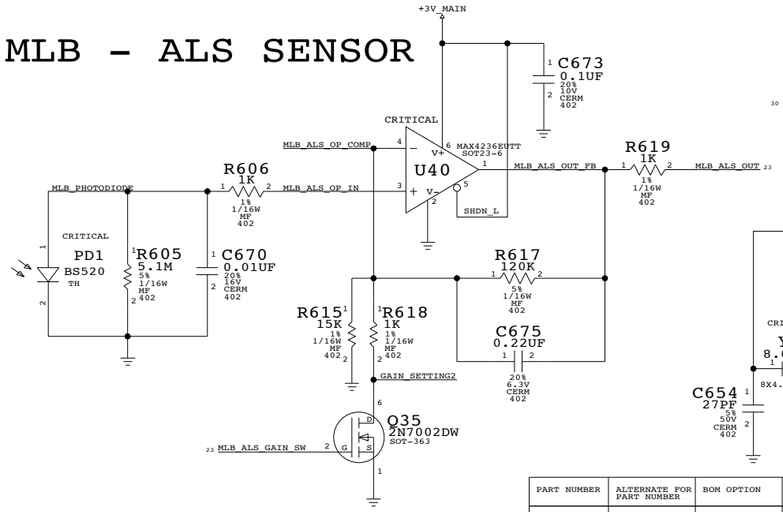
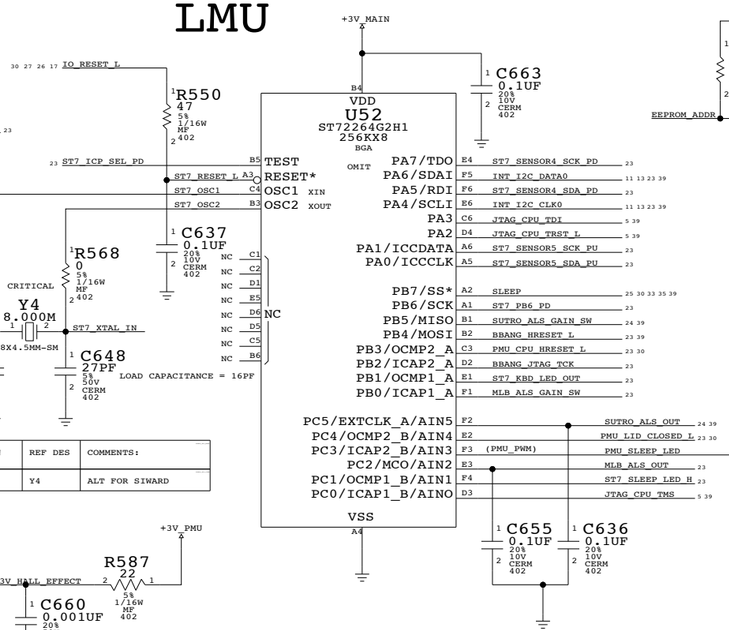
SIZE	DRAWING NUMBER	REV.
D	051-7202	B
SCALE: NONE	SHT 22 OF 44	

MLB - ALS SENSOR



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0856	353S0504	?	U40	ALT FOR SUPPLY PROBLEM

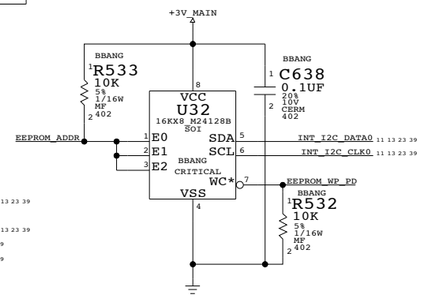
LMU



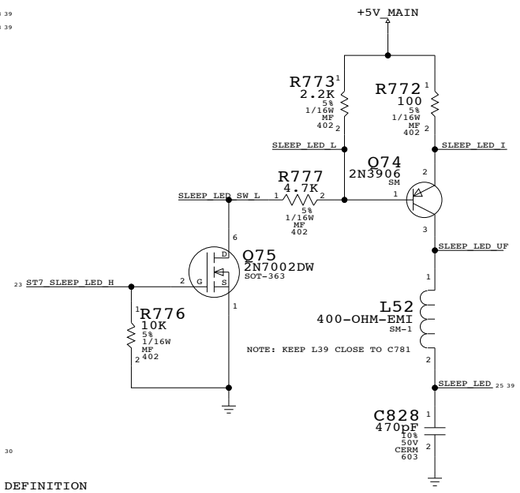
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0008	197S0040		Y4	ALT FOR SIWARD

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1194	1	IC,LMU,P84	U52	CRITICAL	?

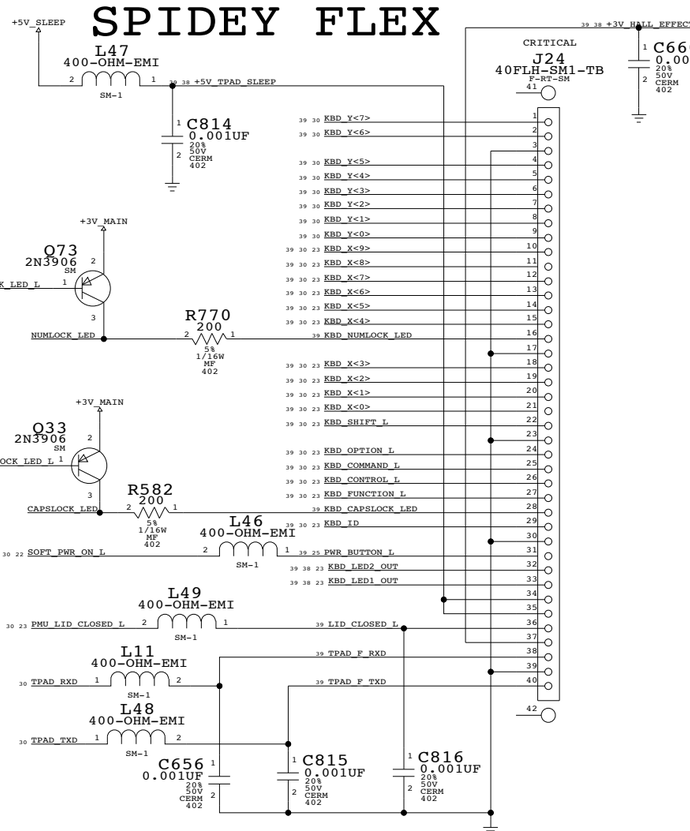
BOOT BANGER E2PROM



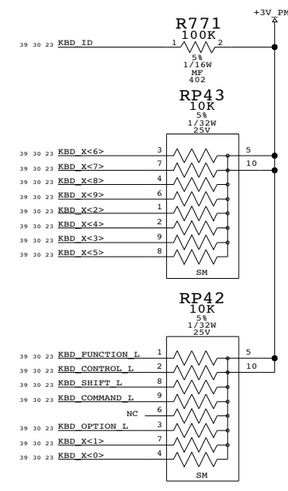
SLEEP LED



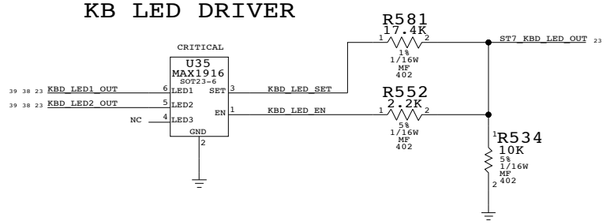
SPIDEY FLEX



KEYBOARD PULLUPS

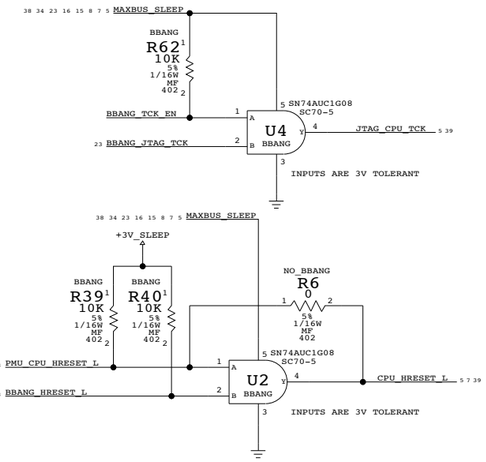


KB LED DRIVER

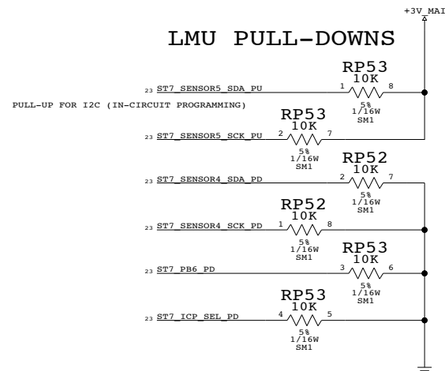


BOOT BANGER SIGNAL DEFINITION

1/ BBANG_HRESET_L (OPEN COLLECTOR OUTPUT - 10K PULLUP ON MLB)
2/ PMU_HRESET_L (3V INPUT INTO LMU)
3/ BBANG_JTAG_TCK (REGULAR OUTPUT)
4/ JTAG_CPU_TMS (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
5/ JTAG_CPU_TDI (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
6/ JTAG_CPU_TRST_L (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)



LMU PULL-DOWNS



LMU/BOOTBANGER/SPIDEY

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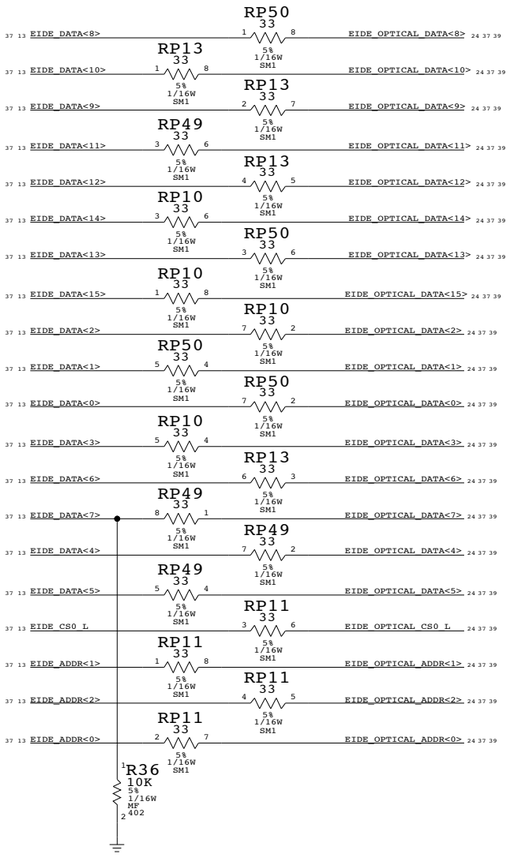
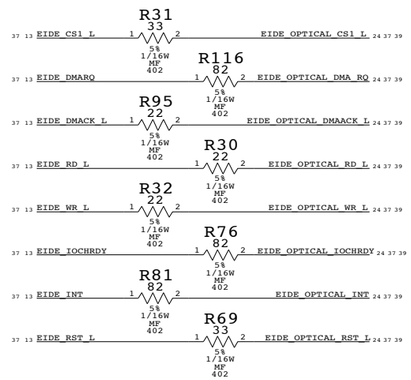
SIZE	DRAWING NUMBER	REV.
D	051-7202	B
SCALE: NONE	SHT 23 OF 44	

HARD DRIVE INTERFACE (UATA100)

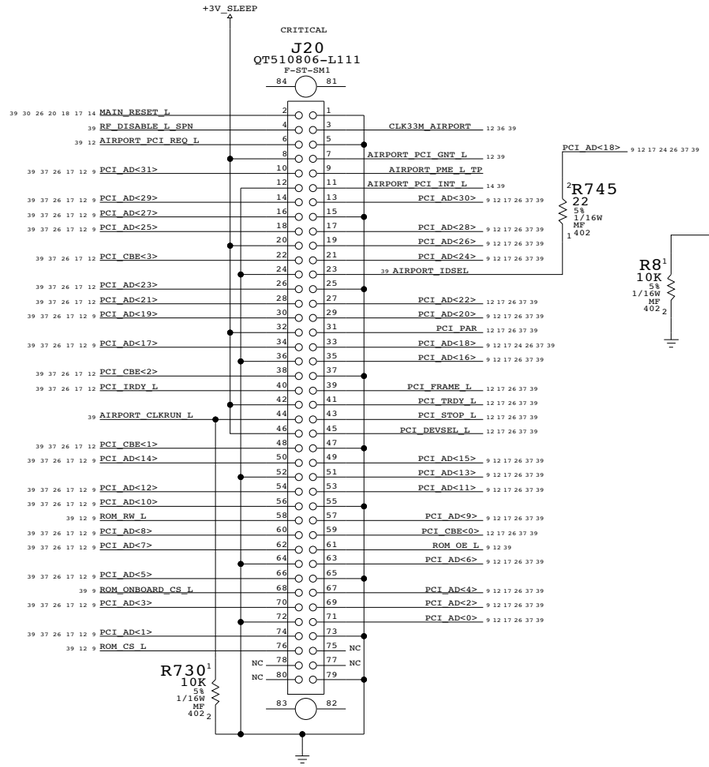
EIDE SERIES TERMINATION

PLACE TERMINATORS NEAR INTREPID

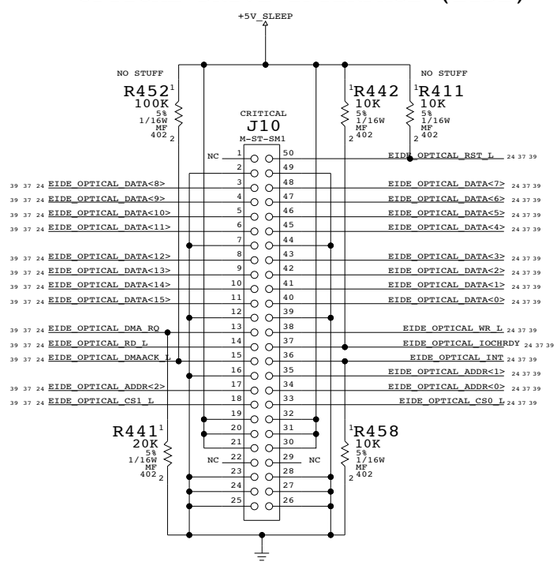




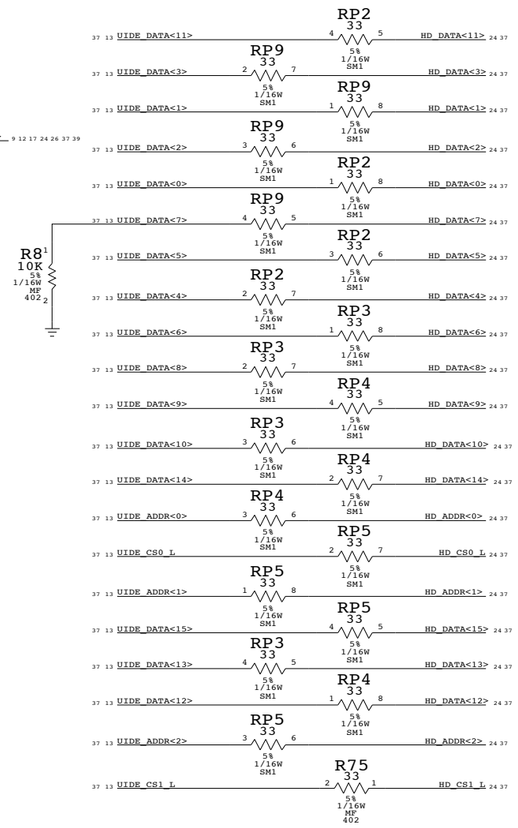
WIRELESS INTERFACE



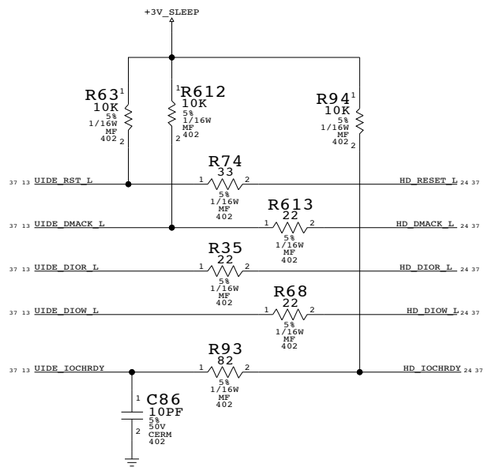
OPTICAL DRIVE INTERFACE (EIDE)



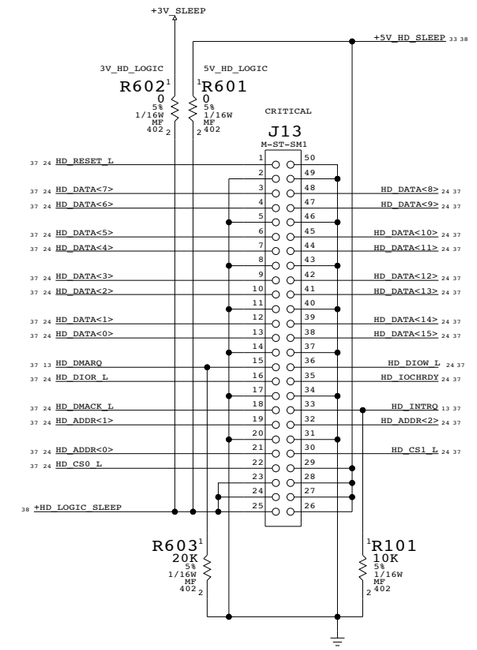
PLACE SERIES R CLOSE TO INTERPID



PLACE PULLUP RESISTORS CLOSE TO INTREPID

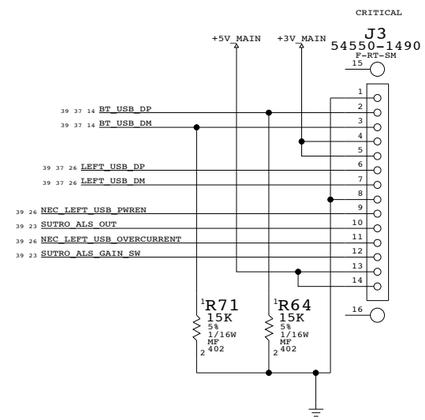


IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V



ANY SEQUENCING REQUIREMENT BETWEEN +5V_HD_SLEEP AND +3V_SLEEP?

BLUETOOTH/LEFT-SIDE USB



INTERNAL I/O CONNECTORS

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APPLE COMPUTER INC.

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SOUND BOARD (SOUSAPHONE)

AUDIO - SNAPPER
SND - INTREPID

L77 FERR-220-OHM 0402
L80 FERR-220-OHM 0402
L81 FERR-220-OHM 0402
L82 FERR-220-OHM 0402
L76 FERR-220-OHM 0402
L78 FERR-220-OHM 0402
L79 FERR-220-OHM 0402

SND_SYNC → SND_SYNC_F
SND_CLKOUT → SND_CLKOUT_F
INT_AUDIO_TO_SND → INT_AUDIO_TO_SND_F
SND_TO_AUDIO → SND_TO_AUDIO_F
SND_AMP_MUTE → SND_AMP_MUTE_F
SND_HW_RESET_L → SND_HW_RESET_L_F
SND_SCLK → SND_SCLK_F

C895 0.01UF 20% 16V CERM 402 NO STUFF
C899 0.01UF 20% 16V CERM 402 NO STUFF
C896 0.01UF 20% 16V CERM 402 NO STUFF
C897 0.01UF 20% 16V CERM 402 NO STUFF
C898 0.01UF 20% 16V CERM 402 NO STUFF
C900 0.01UF 20% 16V CERM 402 NO STUFF
C901 0.01UF 20% 16V CERM 402 NO STUFF

+3V_MAIN
+5V_MAIN

CRITICAL
J12 QT510306-L111 F-ST-SM1

INT_AUDIO_TO_SND_F → SND_TO_AUDIO_F
INT_I2C_CLK2 → SND_HP_SENSE_L
SND_SCLK_F → SND_LIN_SENSE_L
SND_CLKOUT_F → SND_AMP_MUTE_F
SLEEP
INT_I2C_DATA2 → SND_HW_RESET_L_F
SLEEP_LED → SND_HP_MUTE_INV

XW9 SM 1 2 SND_AGND

+5V_MAIN
RP44 100K 5% 1/16W SM1 7
SND_AMP_MUTE
Q26 2N7002DW SOT-363
SND_AMP_MUTE_L
AMP_CONTROL
RP44 100K 5% 1/16W SM1 5
Q26 2N7002DW SOT-363
INT_PU_RESET_L

+3V_MAIN
RP44 100K 5% 1/16W SM1 8
R689 100K 5% 1/16W MF 402
SND_HP_MUTE_INV
Q31 2N7002DW SOT-363
SND_HP_MUTE
Q31 2N7002DW SOT-363
SND_HP_MUTE_L
AMP_CONTROL
RP44 100K 5% 1/16W SM1 3

PLACE XW9 CLOSE TO 5V SWITCHER (U27)
PLACE CAPS AS CLOSE TO THERMISTORS AS POSSIBLE
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY

CAPS FOR EMI EXPERIMENTATION ONLY

FAN INTERFACE

MAIN1
SUPPLY_M_DP
C681 0.001UF 20% 50V CERM 402
Q66 2N3904 SM
SUPPLY_M_DM

PLACE CLOSE TO CPU
MAIN2
CPU_M_DP
C668 0.001UF 20% 50V CERM 402
Q39 2N3904 SM
CPU_M_DM

PLACE UNDERNEATH UPPER RAM
ALTERNATE1
THERM1_A_DP
NO STUFF C678 0.001UF 20% 50V CERM 402
NO STUFF Q47 2N3904 SM
THERM1_A_DM

PLACE CLOSE TO BATTERY CHARGER/VCORE
ALTERNATE2
THERM2_A_DP
NO STUFF C651 0.001UF 20% 50V CERM 402
NO STUFF Q62 2N3904 SM
THERM2_A_DM

KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

R719 0 5% 1/16W MF 402 CPU_M_DP → THERM1_DP
R725 0 5% 1/16W MF 402 CPU_M_DM → THERM1_DM
R713 0 5% 1/16W MF 402 SUPPLY_M_DP → THERM2_DP
R716 0 5% 1/16W MF 402 SUPPLY_M_DM → THERM2_DM

KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

NO STUFF R628 0 5% 1/16W MF 402 CPU_THERM_DP → THERM1_DP
NO STUFF R620 0 5% 1/16W MF 402 CPU_THERM_DM → THERM1_DM
NO STUFF R723 0 5% 1/16W MF 402 THERM1_A_DP → THERM1_DP
NO STUFF R726 0 5% 1/16W MF 402 THERM1_A_DM → THERM1_DM
NO STUFF R710 0 5% 1/16W MF 402 THERM2_A_DP → THERM2_DP
NO STUFF R717 0 5% 1/16W MF 402 THERM2_A_DM → THERM2_DM

MODEM

SUPPORTS BOTH THE LAST DASH AND Q52 SOFT MODEM

+5V_MAIN
C767 10UF 20% 6.3V CERM 805
NO STUFF C513 0.1UF 20% 10V CERM 402
+3V_MAIN
R405 10K 5% 1/16W MF 402
NO STUFF C478 0.1UF 20% 10V CERM 402
C469 10UF 20% 6.3V CERM 805

CRITICAL
J8 QT51066-L010 F-ST-SM1

MOD_DTO → MOD_SYNC
MOD_CLKOUT → INT_MOD_DTI
MOD_BITCLK
COMM_RESET_L → COMM_SHUTDOWN
MODEM_USB_DM
INT_I2C_CLK2 → MODEM_USB_DP
INT_I2C_DATA2 → COMM_RING_DET_L

FAN CONTROLLER

+3V_MAIN
R814 10 5% 1/16W MF 402
ADT7460_VCC
C904 1UF 20% 10V CERM 603
C711 0.1UF 20% 10V CERM 402

VCC U3 ADT7460 QSOP
+2.5V/SMBALERT# SDA SCL
ADT7460_VCORE_MON
INT_I2C_DATA1
INT_I2C_CLK1
D1+ D1- D2+ D2-
THERM1_DP
THERM1_DM
THERM2_DP
THERM2_DM
PWM1/XTO TACH1 PWM2/SMBALERT# TACH2 PWM3/ADR ENABLE# TACH3 TACH4/ADR SELECT/THERM#
GND

R42 10K 5% 1/16W MF 402 ADT7460_FAN1_PWM
FANL_TACH
ADT7460_FAN2_PWM
FANR_TACH
ADT7460_ADR_EN_L
NC
ADT7460_THERM

+5V_SLEEP
R692 10K 5% 1/16W MF 402
R695 10K 5% 1/16W MF 402
Q78 2N7002DW SOT-363
Q78 2N7002DW SOT-363

C688 0.001UF 20% 50V CERM 402
NO STUFF C690 0.001UF 20% 50V CERM 402
NO STUFF C846 0.001UF 20% 50V CERM 402
NO STUFF C905 0.001UF 20% 50V CERM 402

THERM ISOLATION

+3V_MAIN
R811 100K 5% 1/16W MF 402
+3V_PMU_AVCC
R812 100K 5% 1/16W MF 402
THERM_L_OC
R813 100K 5% 1/16W MF 402
THERM_INV
ADT7460_THERM
Q87 2N7002DW SOT-363
Q87 2N7002DW SOT-363
C903 0.1UF 20% 10V CERM 402

LEFT FAN (CPU)

+5V_SLEEP
R679 10K 5% 1/16W MF 402
CRITICAL
J4 SM-2MT
FANL_TACH
FANL_GND
Q37 SI3446DV TSOP
PLACE CLOSE TO CONNECTOR
C134 4.7UF 20% 10V CERM 1206
FANL_PWM

SERIAL DEBUG INTERFACE

+5V_MAIN
SERIAL_DEBUG CRITICAL
J16 M-ST-5087 SM
COMM_TXD_L → COMM_DTR_L
COMM_TRXC → COMM_RTS_L
COMM_GPIO_L → COMM_RXD

DEBUG POWER BUTTON

NO STUFF R527 0 5% 1/16W MF 603
PWR_BUTTON_L

DEBUG JUMPERS

+5V_SLEEP
R293 10K 5% 1/16W MF 402
R295 10K 5% 1/16W MF 402
FANL_PWM
FANR_PWM
NO STUFF R537 0 5% 1/16W MF 603
PMU_NMI_BUTTON_L
NO STUFF R553 0 5% 1/16W MF 603
PMU_RESET_BUTTON_L

RIGHT FAN (GPU)

+5V_SLEEP
R623 10K 5% 1/16W MF 402
CRITICAL
J2 SM-2MT
FANR_GND
FANR_TACH
Q36 SI3446DV TSOP
PLACE CLOSE TO CONNECTOR
C135 4.7UF 20% 10V CERM 1206
FANR_PWM

FAN/MODEM/SOUND/SLEEP LED/DEBUG

APPLE COMPUTER INC.

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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0608	197S0038	NEC_USB	Y5	ALT FOR SIWARD

Y7 LOAD CAPACITANCE IS 16PF

SERR_L AND PERR_L
HAS DEDICATED PULL-UP
FOR BOTH CBUS AND USB2

Series Rpaks required to facilitate NAND-tree testing

INTREPID USB CONSTRAINTS

NEED PULL-UP RESISTORS IN CASE USB 1.0 IS USED FOR PORT POWER

PLACE NEAR J3

SUTRO CONNECTOR

PLACE NEAR J12

BUBBA CONNECTOR

USB 2.0

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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SCALE: NONE	SHT 26 OF 44	

Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0223	338S0079	?	U49	ALT PART

PLACE ALL SERIES RES CLOSE TO PHY

PLACES PHY IN "COMA" MODE WHEN ASLEEP ON BATTERY (SAVES POWER)

PUT CRYSTAL CIRCUIT CLOSE TO PHY

Y3'S LOAD CAPACITANCE IS 20PF

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0703	197S0037		Y3	
197S0603	197S0037		Y3	ALT FOR SIWARD

VOUT = 0.8V*(1+R2EQV/R1)
R2EQV = R2A||R2B

PLACE CAPS (IN ORDER) ON PINS 1, 6, 10/15, 57/62, 67/71, 85

PLACE CAPS (IN ORDER) ON PINS 5, 21/26, 48/52, 66/72, 88, 96

PLACE CAPS (IN ORDER) ON PINS 32/35, 36/40, 45 & 78

PLACE RESISTORS CLOSE TO PHY

SEE CONFIG TABLES (BELOW)

PLACE CLOSE TO ETHERNET CONNECTOR

PLACE CAPS AT TRANSFORMER PINS 1, 4, 7 & 10

Short shielded RJ-45

CONFIG DEFINITIONS	
PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS			
PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

MARVELL 88E1111

10/100/1000 ETHERNET

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-7202 | REV. B

SCALE NONE | SHT 27 OF 44

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0011	197S0052	?	G1	SIWARD ALT FOR FW OSC

DSX STRAP OPTIONS

0 -> BILINGUAL PORT

1 -> A-ONLY PORT

PLACE NEAR PHY

PLACE NEAR PHY

CAPACITOR IN CONJUCTION WITH INTERNAL PULLUP PROVIDES RESET PULSE WHEN PHY FIRST RECEIVES POWER

FIREWIRE

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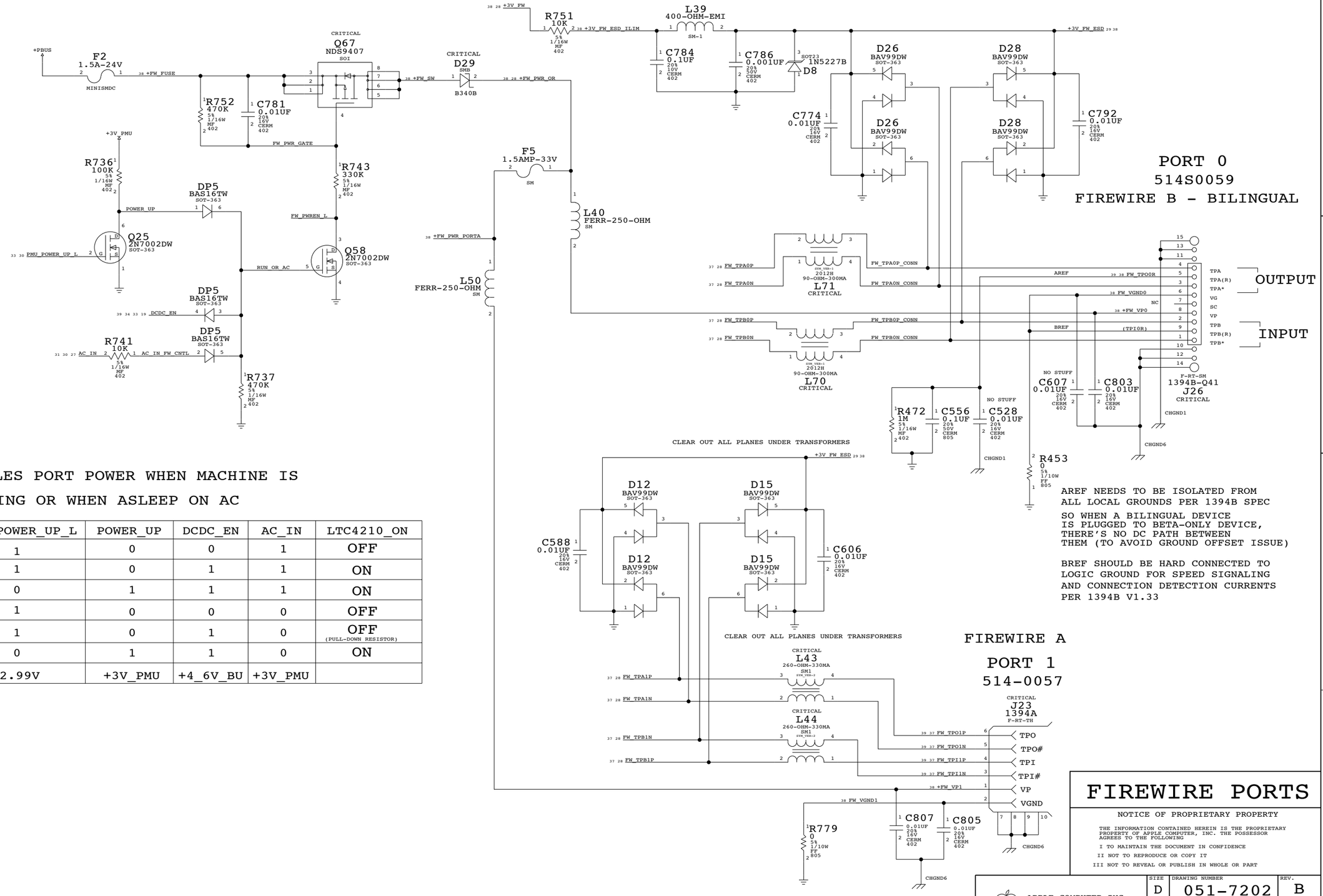
PORT POWER SWITCH

ENABLES PORT POWER WHEN MACHINE IS RUNNING OR WHEN ASLEEP ON AC

STATE	PMU_POWER_UP_L	POWER_UP	DCDC_EN	AC_IN	LTC4210_ON
SHUTDOWN (AC)	1	0	0	1	OFF
SLEEP (AC)	1	0	1	1	ON
RUN (AC)	0	1	1	1	ON
SHUTDOWN (BATT)	1	0	0	0	OFF
SLEEP (BATT)	1	0	1	0	OFF (PULL-DOWN RESISTOR)
RUN (BATT)	0	1	1	0	ON
	2.99V	+3V_PMU	+4_6V_BU	+3V_PMU	



FIREWIRE PORTS

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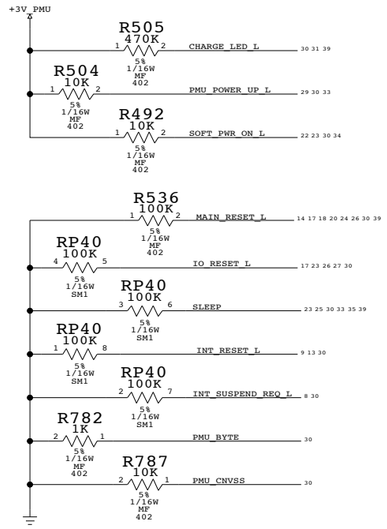
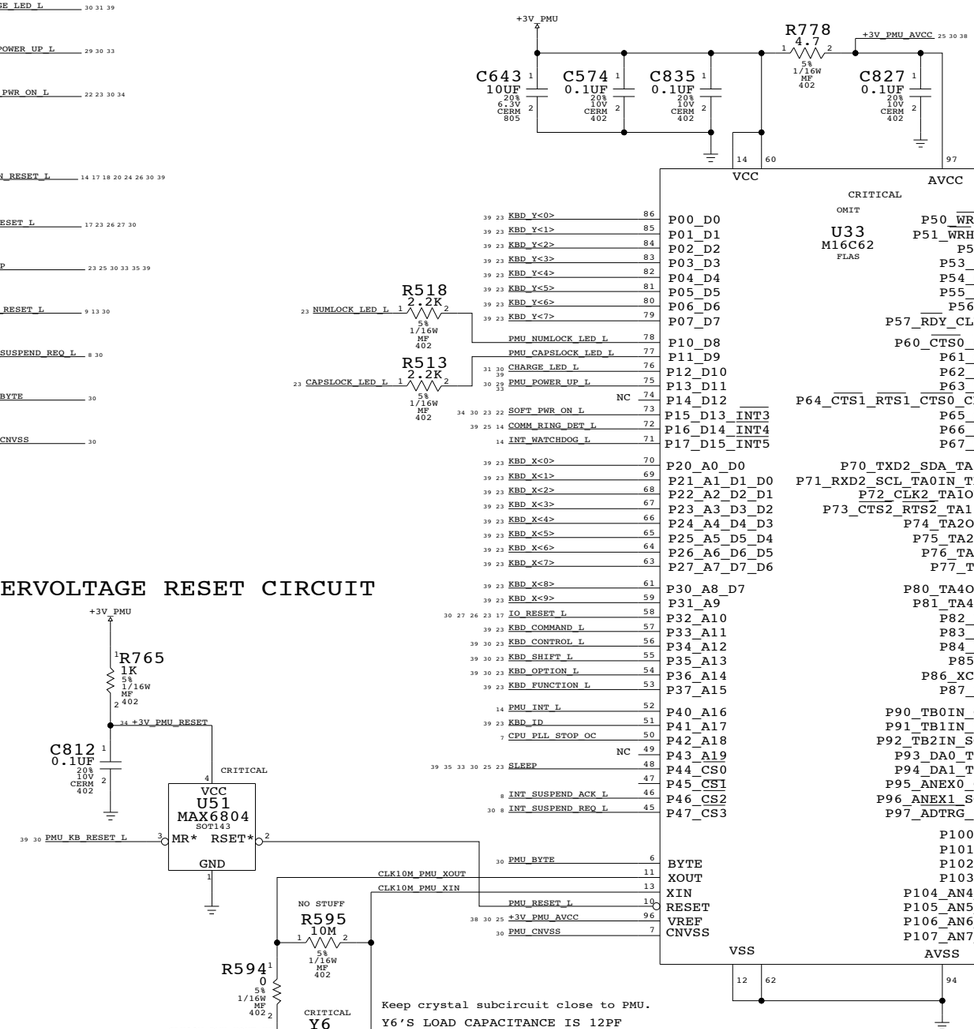




CPU_VCORE_HI_OC/PMU_AP should have a pulldown for coming out of reset. MLB will have a pull-up to +3V_MAIN or +3V_SLEEP, which will act as our pulldown since both are off during PMU reset.

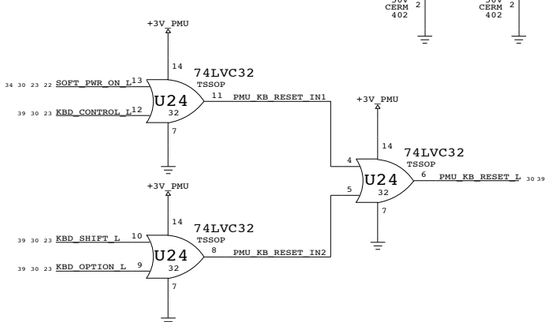
(PMU_AP)

44 CPU_VCORE_HI_OC 7 34
43 INT_RESET_L 9 13 30
42 MAIN_RESET_L 14 17 18 20 24 26 30 39
41 NC
40 PMU_INT_NMI 14
39 PMU_EPM 30
38 INT_PU_RESET_L 13 25 30
37 PMU_CPU_HRESET_L 23
36 PMU_ACK_L 14
35 PMU_CLK 14
34 PMU_FROM_INT 14
33 PMU_TO_INT 14
32 PMU_REQ_L 14
31 PMU_LID_CLOSED_L 23 30
30 PMU_RESET_BUTTON_L 25 30
29 PMU_NMI_BUTTON_L 25 30
28 TPAD_RXD 23 30
27 TPAD_TXD 23 30
26 SYSTEM_CLK_EN 14
25 CPU_CLK_EN 8
24 PMU_CHARGE_V 31
23 PMU_CHRG_BATT_0 31

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1008	1	IC,PMU,V81B	U33	

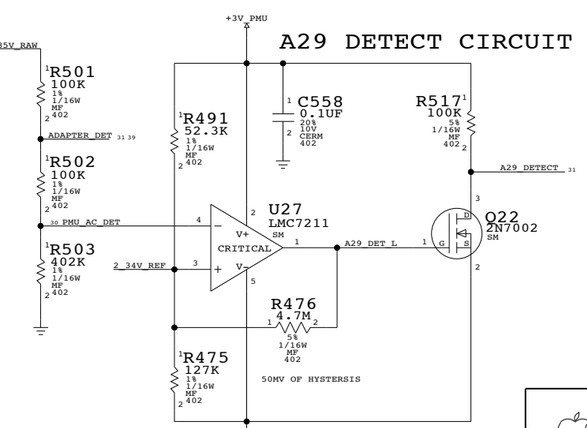
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0704	197S0041		Y6	ALT CRYSTAL SIZE
197S0604	197S0041		Y6	ALT FOR SIWARD

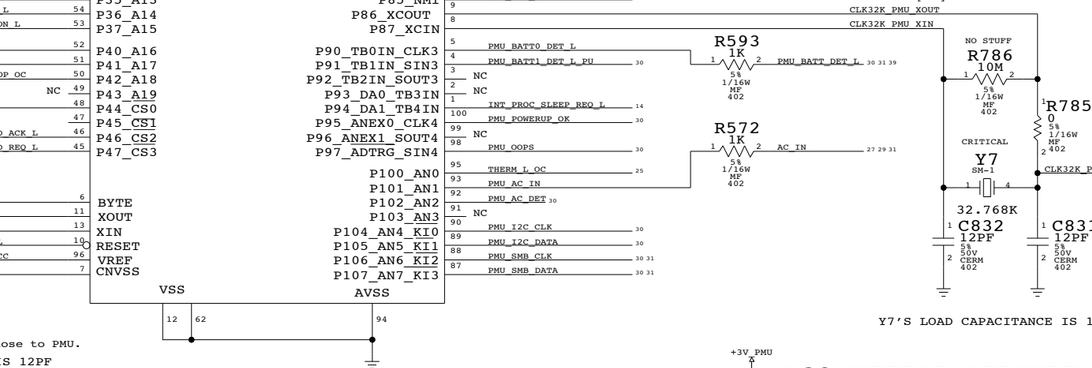
PMU KEYBOARD RESET CIRCUIT

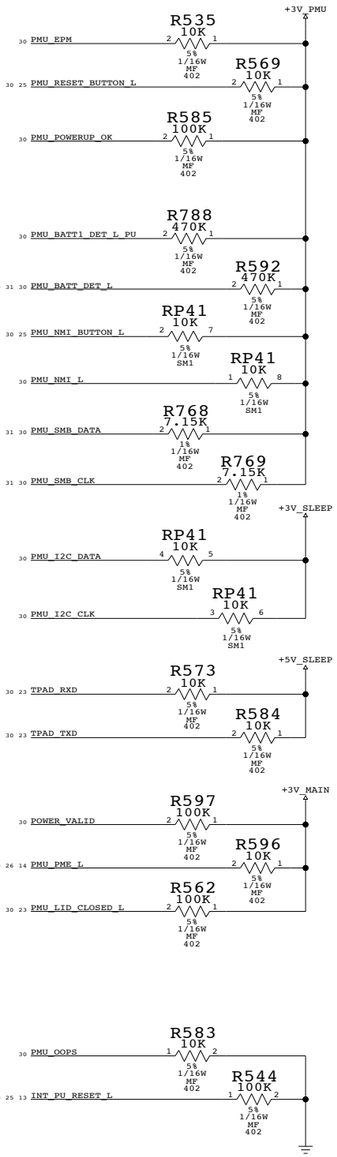


Q11 ADAPTER DETECTION SCHEME

CASE	ADAPTER	PIN VOLT	ID VOLT RANGE	SYSTEM STATUS
1	Q11 (65W)	2.007V- 2.066V	1.65V- 2.31V	RECOGNIZES AS Q11 FULL FUNCTIONS
2	A29 (45W)	2.558V- 2.661V	2.31V- 2.97V	RECOGNIZES AS A29 LIMITED FUNCTIONS
3	AIRLINE	0.589V- 0.663V	0.33V- 0.99V	FULL FUNCTIONS NO BATTERY CHARGING
4	HOOPER	3.19V- 3.28V	2.97V- 3.30V	RECOGNIZES AS HOOPER LIMITED FUNCTIONS







PMU

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DC POWER INPUT

(POWER JACK, ETC. ON SEPARATE BOARD)

CRITICAL

J18
87438-0833
M-RT-SM

CHARGE_LED_L
+ADAPTER
ADAPTER_DET

NO STUFF
C757 0.1UF 20% 50V CERM 805

PLACE CLOSE TO DC INPUT

R396 20K 1% 1/16W MF 402

R395 102K 1% 1/16W MF 402
R364 102K 1% 1/16W MF 402
R375 10K 1% 1/16W MF 402
R365 57.6K 1% 1/16W MF 402

C468 0.01UF 20% 16V CERM 402
R363 10K 5% 1/16W MF 402
R394 1M 5% 1/16W MF 402

U15 LMC7211 SM
CRITICAL

+3V_PMU
1V20_REF
AC_DIV
AC_IN
AC_IN_L

Q10 2N7002DW SOT-363
Q10 2N7002DW SOT-363

R383 470K 5% 1/16W MF 402

GREATER THAN 13.5V DETECT

DC INRUSH LIMITER

+ADAPTER_SW
+ADAPTER_SENSE

Q13 SI4435DY SOI
Q16 SI4435DY SOI

R414 330K 5% 1/16W MF 402
C458 0.1UF 20% 50V CERM 805

R474 47K 5% 1/16W MF 402
R499 68K 5% 1/16W MF 402

AC_ENABLE_GATE
AC_ENABLE_L
BCKFD_PROT_GATE
BCKFD_PROT_EN_L

R374 470K 5% 1/16W MF 402

C592 0.1UF 20% 50V CERM 805

Q10 2N7002DW SOT-363
Q21 2N7002DW SOT-363

PLACE U23 NEXT TO R460

U23 SENSE VOLTAGE DROP ACROSS R460

C572 0.01UF 20% 50V CERM 603

U23 MAX4172 TSSOP
RS+ RS- PG NC1 NC2 OUT GND NC
CRITICAL
MAX4172_OUT

R454 2.21K 0.1% 1/16W MF 603-1
C883 0.1UF 20% 50V X7R 603-1

R460 0.025 1% 1W MF 2512

IF A29 ADAPTER USED, ADJUST CURRENT SETTING

R488 4.7 5% 1/16W MF 402
R498 4.7 5% 1/16W MF 402

1772_CSSP
1772_CSSN

C578 0.47UF 10% 10V CERM 1206
C579 0.47UF 10% 50V CERM 1206

1MSEC INTEGRATION TIME

R742 1K 1% 1/16W MF 402
C771 0.1UF 20% 10V CERM 402

IAC_RC_COMP

+3V_PMU
R747 42.2K 0.1% 1/16W FF 603
C772 0.1UF 20% 10V CERM 402

U50 LMC7111 SOT23-5
CRITICAL

IAC_FB
R466 10K 1% 1/16W MF 402
CURRENT_THRESHOLD

DP4 BAS16TW SOT-363
LTC1625_ITH
R358 150 1% 1/16W MF 402
1625_COMP

PLACE R358 CLOSE TO LTC1625
ROUTE LTC1625_ITH CAREFULLY

ADAPTER_I_REG

R738 42.2K 0.1% 1/16W FF 603
R734 82.5K 0.1% 1/16W FF 603

A29_CURRENT_ADJ

R739 51.1K 0.1% 1/16W FF 603

IF ADAPTER IS OVER 18V, ADJUST CURRENT SETTING

OVER_18V_ADJ

R748 100K 5% 1/16W MF 402

Q20 2N7002DW SOT-363
Q20 2N7002DW SOT-363
Q65 2N7002DW SOT-363

A29_DETECT
AC_GTR_18V
1772_ACOK_L

C775 1UF 20% 10V CERM 603

BATTERY SWITCH-OVER CIRCUIT

+BATT
F4 5AMP-125V SM-2
F3 5AMP-125V SM-2

+24V_PBUS
+PBUS
+BATT_24V_FUSE
+BATT_14V_FUSE

Q24 SI4435DY SOI
CRITICAL
Q76 SUD45P03 TO-252

R490 47K 5% 1/16W MF 402
R746 47K 5% 1/16W MF 402

BATT_24V_GATE
BATT_14V_GATE

R512 10K 5% 1/16W MF 402
R744 10K 5% 1/16W MF 402

DP4 BAS16TW SOT-363
BATT_24PBUS_EN
BATT_14PBUS_EN

Q21 2N7002DW SOT-363

AC_IN_L
R489 158K 1% 1/16W MF 402
DP4 BAS16TW SOT-363
AC_IN_L_RC
C593 10UF 20% 6.3V CERM 805

WHEN AC IS IN, P-CHANNEL FETS ARE QUICKLY (DIODE) TURNED OFF
WHEN AC IS NOT PLUGGED, P-CHANNEL FETS ARE ON
RC TIME IS 480K*10UF @ +3V_PMU

SWITCHER VOLTAGE CONTROL

PMU SELECTS BETWEEN TWO VOLTAGES

R567 27.4K 1% 1/16W MF 402
R558 10K 1% 1/16W MF 402
R548 10K 1% 1/16W MF 402
R560 4.12K 1% 1/16W MF 402
R565 48.7K 1% 1/16W MF 402

BATTV_HIGH
BATTV_LOW

R561 100K 5% 1/16W MF 402
Q27 2N7002DW SOT-363
R580 5.23K 1% 1/16W MF 402
Q27 2N7002DW SOT-363

PMU_CHARGE_V

R578 100K 5% 1/16W MF 402
CHARGE_DISABLE
Q30 2N7002DW SOT-363
Q30 2N7002DW SOT-363

PMU_CHRG_BATT_0

$V_{BATT} = CELLS \times (4.096 + (0.4096 * V_{VCTL} / V_{REFIN}))$

For 4.15V cells, VCTL = 0.123 REFIN

For 4.20V cells, VCTL = 0.245 REFIN

$I_{CHG} = (0.2048/R_{62}) * (V_{ICTL} / V_{REFIN})$

SWITCHER CURRENT CONTROL

CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V

CHARGE THROTTLED BY LOW BATTERY VOLTAGE

OD OUTPUT LOW - WHEN AC GREATER THAN 18V

R754 100K 1% 1/16W MF 402
D9 1N914 SOT23
C600 1UF 20% 50V CERM1 1210
R755 12.7K 1% 1/16W MF 402

U31 MAX1772 QSOP
CRITICAL

CSSP CSSN DCIN CELLS ACIN LDO ACOK DLOV RFIN BST VCTL DHI ICTL LX ICHG DLO IINP PGND (GND) CCV CSIP CCI CSIN CCS BATT REF = 4.096V REF_CLS GND

1772_DCIN
1772_ACIN
1772_ACOK_L
(+3V_PMU)
1772_VCTL
1772_ICTL
1772_ICHG
1772_IINP
1772_CCV
1772_CCI
1772_CCS
1772_CELLS
1772_DLOV
1772_BST
1772_DHI
1772_LX
1772_DLO
(GND)
1772_CSIP
1772_CSIN
1772_GND

R542 1K 1% 1/16W MF 402
R566 1K 1% 1/16W MF 402
BATT_LOW_L

Q29 2N7002DW SOT-363
Q29 2N7002DW SOT-363

R526 1K 1% 1/16W MF 402
C622 0.01UF 20% 16V CERM 402
C616 0.01UF 20% 16V CERM 402
1772_CCV_RC
R497 1K 1% 1/16W MF 402
C621 0.1UF 20% 10V CERM 402

1772_REF
C630 1UF 20% 10V CERM 603

R487 10K 1% 1/16W MF 402
R473 4.12K 1% 1/16W MF 402
1772_CLS

C652 1UF 20% 10V CERM 603
R559 100K 5% 1/16W MF 402

C817 0.1UF 20% 25V CERM 603
C802 0.1UF 20% 25V CERM 603

NO STUFF
C906 0.0022UF 10% 50V CERM 402

XW19 SM

+BATT_VSNS

R571 33 5% 1/8W FF 1206
D10 1N914 SOT23
1772_BST_ESR
R549 100K 5% 1/16W MF 402
C624 0.1UF 20% 25V CERM 603
R774 4.7 5% 1/16W MF 603
C608 0.1UF 20% 50V CERM 805

Q63 IRF7805 SM
CRITICAL

C547 2.2UF 10% 50V CERM 1812
C562 2.2UF 10% 50V CERM 1812
C563 2.2UF 10% 50V CERM 1812
C557 2.2UF 10% 50V CERM 1812
C564 2.2UF 10% 50V CERM 1812

L42 10uH SM1
CRITICAL
D30 SM MBRS140T3

R763 0.05 1% 1W MF 2512
+BATT_RSNS

Q64 IRF7811W SO-8
CRITICAL

R543 1 5% 1/16W MF 603
R511 1 5% 1/16W MF 603

C619 4.7UF 20% 25V CERM 1206
C632 4.7UF 20% 25V CERM 1206
C617 4.7UF 20% 25V CERM 1206
C824 33UF 20% 25V ELEC SM1
C631 4.7UF 20% 25V CERM 1206
C633 4.7UF 20% 25V CERM 1206
C618 4.7UF 20% 25V CERM 1206

R749 6.34K 1% 1/16W MF 402
A29_CLS_ADJ

Q65 2N7002DW SOT-363
A29_DETECT

C615 0.1UF 20% 10V CERM 402
U38 LMC7211 SM
CRITICAL
BATT_LOW

R588 100K 1% 1/16W MF 402
R579 499K 1% 1/16W MF 402
BATT_DIV
1V65_REF
R599 100K 1% 1/16W MF 402
R570 100K 1% 1/16W MF 402
C658 0.047uF 10% 16V CERM 402

BATTERY CONNECTOR

CRITICAL
J25
87438-0833
M-RT-SM

+BATT_POS
(BATT_IN_PD)
BATT_CLK
BATT_DATA
PMU_BATT_DET_L
BATT_NEG

L9 FERR-EMI-100-OHM SM
L53 FERR-50-OHM SM
L10 FERR-EMI-100-OHM SM
PMU_SMB_CLK
L8 FERR-EMI-100-OHM SM
PMU_SMB_DATA
L12 FERR-50-OHM SM

BATTERY CHARGER

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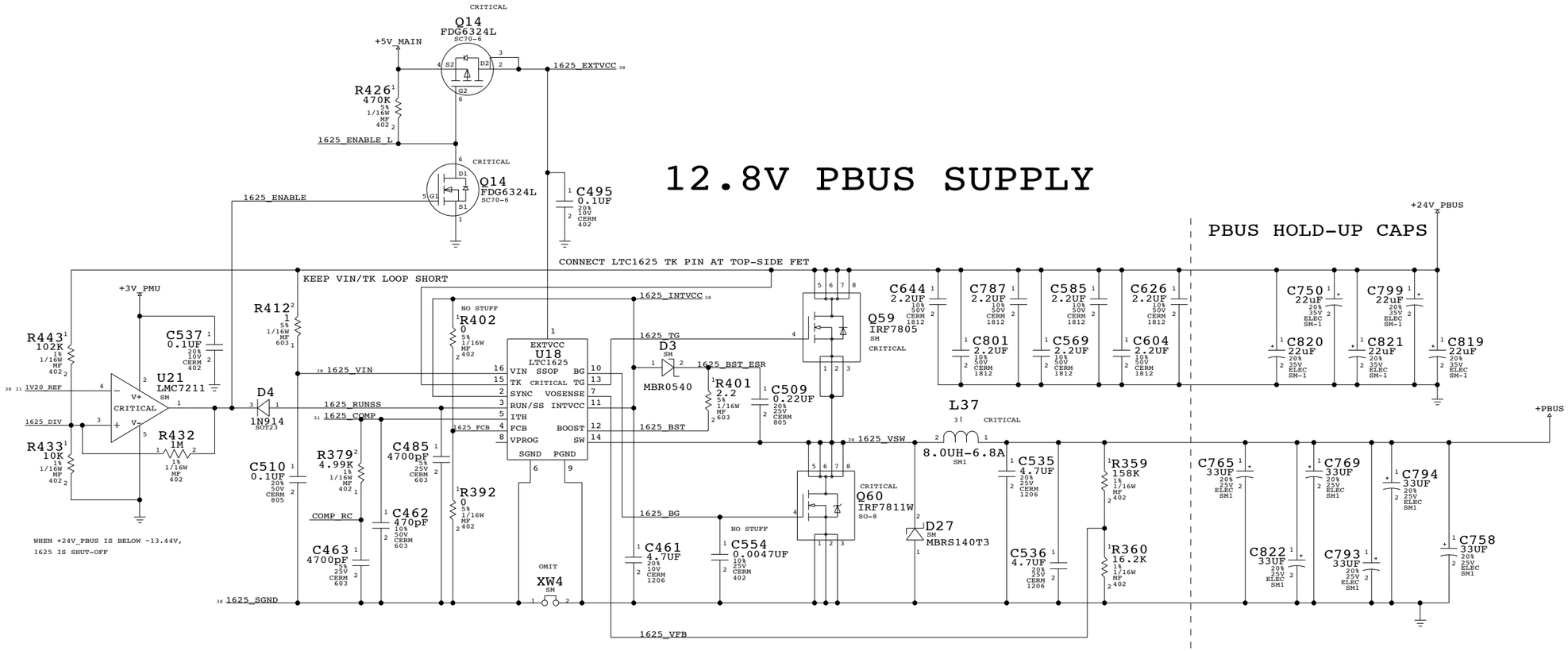
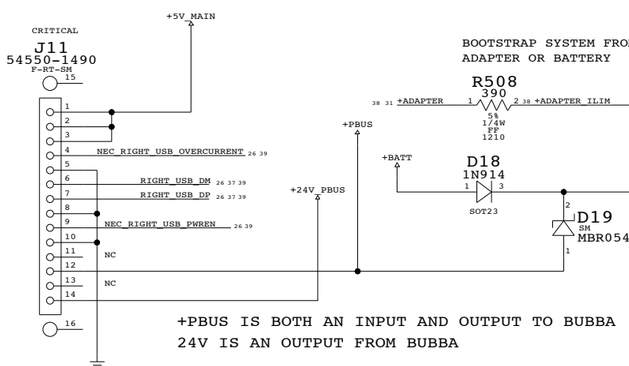
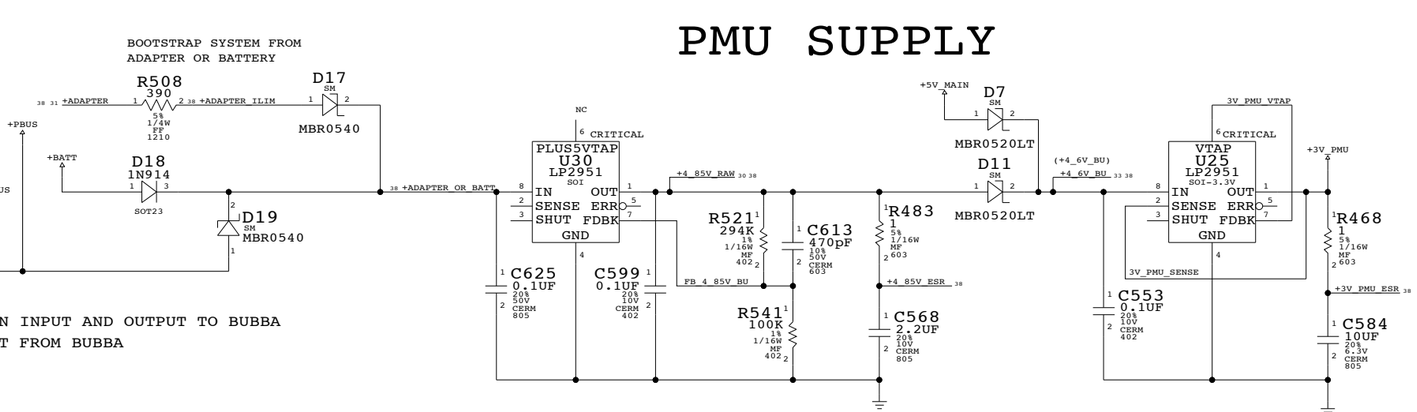
SIZE	DRAWING NUMBER	REV.
D	051-7202	B
SCALE: NONE	SHT 31 OF 44	

12.8V PBUS SUPPLY



BACKUP BATTERY / USB CONNECTOR





PMU SUPPLY

12.8V REGULATOR

APPLE COMPUTER INC.

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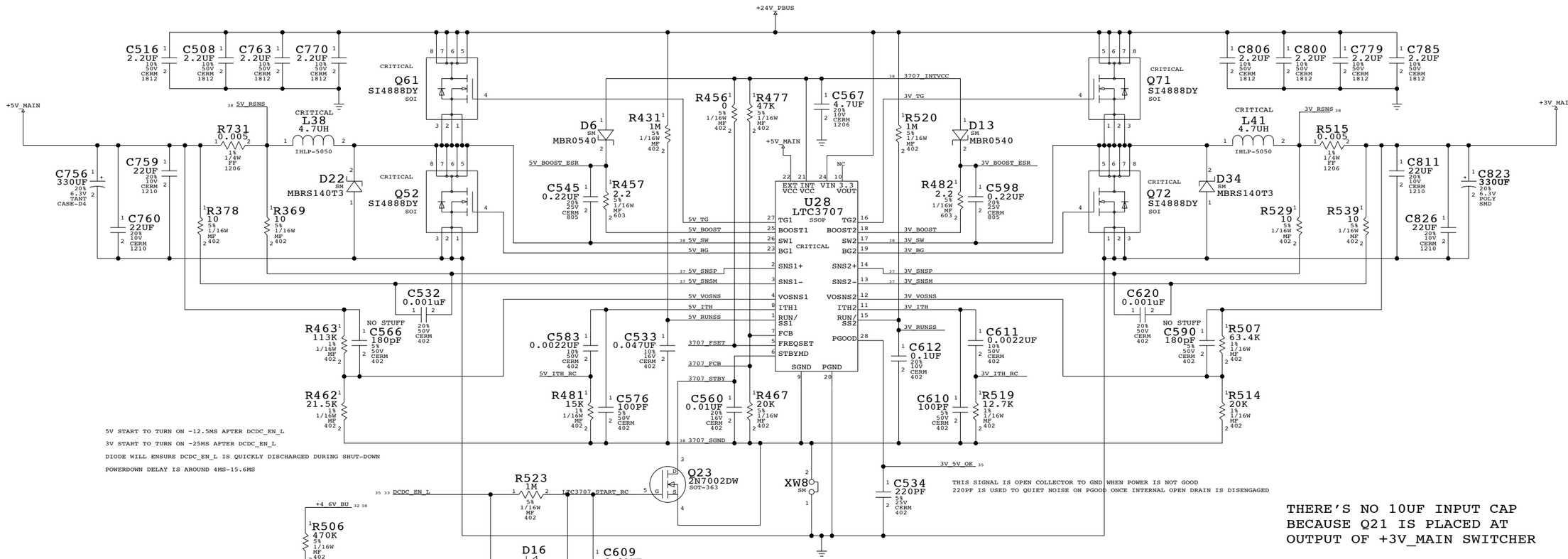
SCALE: NONE

SHT 32 OF 44

3.3V/5V MAIN SUPPLY



5V START TO TURN ON ~12.5MS AFTER DCDC_EN_L
3V START TO TURN ON ~25MS AFTER DCDC_EN_L
DIODE WILL ENSURE DCDC_EN_L IS QUICKLY DISCHARGED DURING SHUT-DOWN
POWERDOWN DELAY IS AROUND 4MS-15.6MS

THERE'S NO 10UF INPUT CAP
BECAUSE Q21 IS PLACED AT
OUTPUT OF +3V_MAIN SWITCHER

3.3V/5V REGULATOR

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VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage
(approx. 7ms delay)

1.175V -> 1.025V 1.30V -> 0.975V

SEL = 0; Y1=A1
SEL = 1; Y1=B1

Keep trace fat (40-100 mils) and short!!

MAX1717 VID CAN TAKE 3.3V TO 5.5V INPUTS

Connect MAX1717 GND pin 13 to GND at bottom-side FET

Keep trace fat and short!!

Keep trace fat and short!!

Keep trace fat and short!!

PLACE THIS SHORT AT PIN OF 1000uF CAP CLOSEST TO CPU

ROUTE AS DIFFERENTIAL PAIR

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V WITH A 0.85 SCALE FACTOR, HENCE VOFFSET = 1.7V * (R1/(R1+R2)) AND VCORE = VDAC + VOFFSET.

NOTE: R310 (R2) NO STUFFED FOR NO OFFSET CASE

OUTPUT VOLTAGE

V_{DAC} D4=0	V_{DAC} D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	A/B_ = Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1

If all pull-ups are >=100K and all pull-downs are <=1K, $V_A = V_B$.

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0022	128S0034	?	C728,C729,C730,C731,C732,C733,C734,C884,C885	

FMAX CONNECTOR

CRITICAL
NO STUFF
J5
M-ST-SM-52465-1217

VCORE SUPPLY

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SCALE: NONE	SHT 34 OF 44	

1.5V/2.5V SWITCHER

+1_5V_SLEEP LOADS

1) AGP I/O - IF USING D3COLD
2) MAXBUS I/O - IF 1.5V INTERFACE

+1_5V_MAIN LOADS

1) INTREPID CORE
2) AGP I/O IF USING D3HOT

+2_5V_MAIN LOADS

1) MAP31 - FBCORE/FBIO IF USING D3HOT
2) GIGABIT ETHERNET - AVDDL
3) DDR SODIMMS - CORE/IO
4) DDR MUXES
5) CLOCK SLEWING I/O
6) PCI1510 CORE

+2_5V_SLEEP LOADS

1) FBCORE/FBIO IF USING D3COLD
2) INTREPID MEMORY I/O

CHANGE R424 BACK TO 10K, 1%, AND STUFF 5.11K FOR 1.5V OPERATION
CONNECTING 1_5V_FB TO GND, FORCES 1.8V OUTPUT

1.8V SWITCHER

+1_8V_MAIN LOADS

1) INTREPID PLLS

+1_8V_SLEEP LOADS

1) MPC7450 - MAXBUS I/O - IF 1.8V INTERFACE
2) CPU JTAG & MaxBus Pull-ups
3) CPU PLL Config Straps
4) OPTIONAL VIDEO MEMORY (M10 PRO ONLY)

1.5V/1.8V/2.5V SUPPLIES

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7202	B
SCALE: NONE	SHT 35 OF 44	

DIGITAL SIGNALS

GROUP	SIG_NAME		MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
MAXBUS	CPU_AACK_L				250.0000	10_MIL_SPACING			5 8
	CPU_ADDR<0..31>		5		250			83_MHZ	5 8
	CPU_ARTRY_L				250.0000	10_MIL_SPACING			5 8
	CPU_BG_L				250.0000	10_MIL_SPACING			5 8
	CPU_BR_L				250.0000	10_MIL_SPACING			5 8
	CPU_CI_L		5		250.0000				5 8
	CPU_DATA<0..31>		5		250			83_MHZ	6 8
	CPU_DATA<32..63>		5		250			83_MHZ	6 8
	CPU_DBG_L		5		250.0000	10_MIL_SPACING			5 8
	CPU_DTI<0..2>		5		250				5 8
	CPU_DRDY_L_UF					10_MIL_SPACING			
	CPU_DRDY_L				250.0000	10_MIL_SPACING			5 8
	CPU_GBL_L		5		250.0000				5 8
	CPU_HIT_L				250.0000	10_MIL_SPACING			5 8
	CPU_QACK_L		5		250.0000	10_MIL_SPACING			5 8
	CPU_QREQ_L				250.0000	10_MIL_SPACING			5 8
	CPU_TA_L				250.0000	10_MIL_SPACING			5 8
	CPU_TBST_L		5		250.0000	10_MIL_SPACING			5 8
	CPU_TEA_L				250.0000				5 8
	CPU_TS_L				250.0000	10_MIL_SPACING			5 8
	CPU_TSIZ<0..2>		5		250				5 8
	CPU_TT<0...4>		5		250				5 8
	CPU_WT_L		5		250.0000				5 8
GROUP 0	MEM_DATA<7..0>		4		200			167_MHZ	9 10
	RAM_DATA_A<7..0>		4		200			167_MHZ	10 11
	RAM_DATA_B<7..0>		4		200			167_MHZ	10 11
	MEM_DQS<0>	TOTAL LENGTH CONTROLLED BY SPREADSHEET			200				9 10
	RAM_DQS_A<0>		4		200				10 11
	RAM_DQS_B<0>		4		200				10 11
	MEM_DQM<0>		4		200				9 10
	RAM_DQM_A<0>		4		200				10 11
	RAM_DQM_B<0>		4		200				10 11
GROUP 1	MEM_DATA<15..8>		4		200			167_MHZ	9 10
	RAM_DATA_A<15..8>		4		200			167_MHZ	10 11
	RAM_DATA_B<15..8>		4		200			167_MHZ	10 11
	MEM_DQS<1>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200				9 10
	RAM_DQS_A<1>		4		200				10 11
	RAM_DQS_B<1>		4		200				10 11
	MEM_DQM<1>				200				9 10
	RAM_DQM_A<1>		4		200				10 11
	RAM_DQM_B<1>		4		200				10 11
GROUP 2/3	MEM_DATA<31..16>		4		200			167_MHZ	9 10
	RAM_DATA_A<31..16>		4		200			167_MHZ	10 11
	RAM_DATA_B<31..16>		4		200			167_MHZ	10 11
	MEM_DQS<3..2>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200			167_MHZ	9 10
DDR RAM	RAM_DQS_A<3..2>		4		200			167_MHZ	10 11
	RAM_DQS_B<3..2>		4		200			167_MHZ	10 11
	MEM_DQM<3..2>		4		200			167_MHZ	9 10
	RAM_DQM_A<3..2>		4		200			167_MHZ	10 11
	RAM_DQM_B<3..2>		4		200			167_MHZ	10 11
GROUP 4/5	MEM_DATA<47..32>		4		200			167_MHZ	9 10
	RAM_DATA_A<47..32>		4		200			167_MHZ	10 11
	RAM_DATA_B<47..32>		4		200			167_MHZ	10 11
	MEM_DQS<5..4>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200			167_MHZ	9 10
	RAM_DQS_A<5..4>		4		200			167_MHZ	10 11
	RAM_DQS_B<5..4>		4		200			167_MHZ	10 11
	MEM_DQM<5..4>		4		200			167_MHZ	9 10
	RAM_DQM_A<5..4>		4		200			167_MHZ	10 11
	RAM_DQM_B<5..4>		4		200			167_MHZ	10 11
GROUP 6	MEM_DATA<55..48>		4		200			167_MHZ	9 10
	RAM_DATA_A<55..48>		4		200			167_MHZ	10 11
	RAM_DATA_B<55..48>		4		200			167_MHZ	10 11
	MEM_DQS<6>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200				9 10
	RAM_DQS_A<6>				200				10 11
	RAM_DQS_B<6>		4		200				10 11
	MEM_DQM<6>				200				9 10
	RAM_DQM_A<6>		4		200				10 11
	RAM_DQM_B<6>		4		200				10 11
GROUP 7	MEM_DATA<63..56>		4		200			167_MHZ	9 10
	RAM_DATA_A<63..56>		4		200			167_MHZ	10 11
	RAM_DATA_B<63..56>		4		200			167_MHZ	10 11
	MEM_DQS<7>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200				9 10
	RAM_DQS_A<7>				200				10 11
	RAM_DQS_B<7>				200				10 11
	MEM_DQM<7>		4		200				9 10
	RAM_DQM_A<7>		4		200				10 11
	RAM_DQM_B<7>		4		200				10 11
ADDR	MEM_ADDR<12..0>		4					83_MHZ	9
	RAM_ADDR<12..0>		6		200				9 11
	MEM_BA<1..0>		4						9
	RAM_BA<1..0>		6		200				9 11
CONTROL	MEM_CS_L<3..0>		4						9
	RAM_CS_L<3..0>		6		200				9 11
	MEM_CKE<3..0>		4						9
	RAM_CKE<3..0>		6		200				9 11
	MEM_RAS_L		4						9
	RAM_RAS_L				200.0000				9 11
	MEM_CAS_L		4						9
	RAM_CAS_L				200.0000				9 11
	MEM_WE_L		4						9
	RAM_WE_L				200.0000				9 11
	MEM_MUXSEL_H<1..0>		3						9 10
	MEM_MUXSEL_L<1..0>		3						9 10
	RAM_MUXSEL_H		5						10
	RAM_MUXSEL_L		5						10

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME			MAX VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM	
INTREPID CLOCKS	SYSCLK_CPU_UF						10_MIL_SPACING		8
	SYSCLK_CPU			4		200.0000	10_MIL_SPACING		5 8
	INT_CPUFB_OUT			3			10_MIL_SPACING		8
	INT_CPUFB_OUT_SHORT			3			10_MIL_SPACING		8
	INT_CPUFB_OUT_NORM			3			10_MIL_SPACING		8
	INT_CPUFB_IN_NORM			3			10_MIL_SPACING		8
	INT_CPUFB_LONG			3			10_MIL_SPACING		8
	INT_CPUFB_IN					200.0000	10_MIL_SPACING		8
	SYSCLK_DDRCLK_A0_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_A0_L_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_A1_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_A1_L_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_B0_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_B0_L_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_B1_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_B1_L_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_A0	DDRCLK_A0		3		200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_A0_L	DDRCLK_A0				200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_A1	DDRCLK_A1		3		200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_A1_L	DDRCLK_A1				200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_B0	DDRCLK_B0		3		200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_B0_L	DDRCLK_B0		3		200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_B1	DDRCLK_B1		3		200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_B1_L	DDRCLK_B1		3		200.0000	10_MIL_SPACING		9 11
	INT_REF_CLK_OUT			3		200.0000	10_MIL_SPACING		14
	INT_REF_CLK_IN					200.0000	10_MIL_SPACING		14
	CLK66M_GPU_AGP_UF					200.0000	10_MIL_SPACING		12
	CLK66M_GPU_AGP			4		200.0000	10_MIL_SPACING		12 18
	INT_AGP_FB_OUT					200.0000	10_MIL_SPACING		12
	INT_AGP_FB_IN			4		200.0000	10_MIL_SPACING		12
	CLK33M_CBUS_UF					200.0000	10_MIL_SPACING		12
	CLK33M_CBUS	SHOULD BE AT MOST 4 VIAS FOR CLK		6		200.0000	10_MIL_SPACING		12 17
	CLK33M_AIRPORT_UF					200.0000	10_MIL_SPACING		12
	CLK33M_AIRPORT	SHOULD BE AT MOST 4 VIAS FOR CLK		6		200.0000	10_MIL_SPACING		12 24 39
	CLK33M_USB2_UF					200.0000	10_MIL_SPACING		12
	CLK33M_USB2	SHOULD BE AT MOST 4 VIAS FOR CLK		6		200.0000	10_MIL_SPACING		12 26
	INT_PCI_FB_OUT					200.0000	10_MIL_SPACING		12
	INT_PCI_FB_IN			3		200.0000	10_MIL_SPACING		12
MAP31	GPU_CLK27M_OUT						10_MIL_SPACING		
	GPU_CLK27M_UF						10_MIL_SPACING		
	GPU_SSCLK_UF						10_MIL_SPACING		
	GPU_SSCLK_IN						10_MIL_SPACING		
	GPU_FBCLK0						10_MIL_SPACING		
	GPU_FBCLK0_L						10_MIL_SPACING		
	GPU_FBCLK1						10_MIL_SPACING		
	GPU_FBCLK1_L						10_MIL_SPACING		
	GPU_DVO_CLKP						10_MIL_SPACING		19 20
CRYSTALS	CLK27M_GPU_XOUT						10_MIL_SPACING		
	CLK27M_XTAL_IN						10_MIL_SPACING		
	CLK27M_GPU_XIN						10_MIL_SPACING		
	CLK18M_INT_XIN						10_MIL_SPACING		14
	CLK18M_INT_XOUT						10_MIL_SPACING		14
	CLK18M_XTAL_IN						10_MIL_SPACING		14
	CLK18M_INT_EXT						10_MIL_SPACING		14
	CLK25M_ENET_XIN						10_MIL_SPACING		27
	CLK25M_ENET_XOUT						10_MIL_SPACING		27
	NEC_XT1						10_MIL_SPACING		26
	NEC_XT2	THERE'S ANOTHER 280MIL LEG					10_MIL_SPACING		26
SOUND	SND_SCLK			7		200.0000	10_MIL_SPACING		14 25 39
	SND_CLKOUT					200.0000	10_MIL_SPACING		14 25 39
ETHERNET MARVELL	CLKENET_PHY_RX					200.0000			27
	CLKENET_LINK_RX			3		200.0000	10_MIL_SPACING		13 27
	CLKENET_PHY_GBE_REF					200.0000			27
	CLKENET_LINK_GBE_REF			3		200.0000	10_MIL_SPACING		13 27
	CLKENET_PHY_TX					200.0000			27
	CLKENET_LINK_TX			5		200.0000	10_MIL_SPACING		13 27
	CLKENET_LINK_GTX					200.0000			13
	CLKENET_PHY_GTX			3		200.0000	10_MIL_SPACING		13 27
FIREWIRE	CLKFW_PHY_PCLK					200.0000			28
	CLKFW_LINK_PCLK			3		200.0000	10_MIL_SPACING		13 28
	CLKFW_PHY_LCLK			3		200.0000	10_MIL_SPACING		13 28
	CLKFW_LINK_LCLK					200.0000			13
	FW_XI					200.0000	10_MIL_SPACING		28
	FW_OSC					200.0000	10_MIL_SPACING		28

SIGNAL CONSTRAINTS - PAGE 1

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Digital Signals (cont'd)

GROUP	SIG_NAME	DELAY_RULE	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
AGP	AGP_AD<15..0>		5	100				66_MHz	12 18
AGP BYTES 0-1	AGP_CBE<1..0>		5	100				66_MHz	12 18
	AGP_AD_STB<0>		5	100		8_MIL_SPACING			12 18
	AGP_AD_STB_L<0>		5	100		8_MIL_SPACING			12 18
AGP BYTES 2-3	AGP_AD<31..16>		5	100				66_MHz	12 18
	AGP_CBE<3..2>		5	100				66_MHz	12 18
	AGP_AD_STB<1>		5	100		8_MIL_SPACING			12 18
	AGP_AD_STB_L<1>			100		8_MIL_SPACING			12 18
AGP SIDEBAND	AGP_SBA<7..0>		5	100				66_MHz	12 18
	AGP_SB_STB			100.0000		8_MIL_SPACING			12 18
	AGP_SB_STB_L		5	100.0000		8_MIL_SPACING			12 18
AGP CONTROL	AGP_FRAME_L			250.0000					12 18
	AGP_IRDY_L			250.0000					12 18
	AGP_TRDY_L		6	250.0000					12 18
	AGP_DEVSEL_L			250.0000					12 18
	AGP_STOP_L		6	250.0000					12 18
	AGP_PAR		6	250.0000					12 18
	AGP_REQ_L			285.0000					12 18
	AGP_GNT_L			250.0000					12 18
	AGP_RBF_L			250.0000					12 18
DVO	GPU_DVOD<0..11>		5	250					19 20
	GPU_DVO_HSYNC								19 20
	GPU_DVO_VSYNC								19 20
PCI	PCI_AD<31..0>					MIN_DAISY_CHAIN		33_MHz	9 12 17 24 26 39
	PCI_CBE<3..0>					MIN_DAISY_CHAIN		33_MHz	12 17 24 26 39
	PCI_FRAME_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_IRDY_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_TRDY_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_DEVSEL_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_STOP_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_PAR					MIN_DAISY_CHAIN			12 17 24 26 39
ULTRA ATA-100	UIDE_DATA<15..8>			NEED TO MATCH DELAY TO 250	200			100_MHz	13 24
	UIDE_DATA<7>				200				13 24
	UIDE_DATA<6..0>				200			100_MHz	13 24
	UIDE_ADDR<2..0>				200			100_MHz	13 24
	UIDE_RST_L				200.0000				13 24
	UIDE_DIOW_L				200.0000				13 24
	UIDE_DIOR_L			10_MIL_SPACING	200.0000				13 24
	UIDE_DMACK_L				200.0000				13 24
	UIDE_CS0_L				200.0000				13 24
	UIDE_CS1_L				200.0000				13 24
	UIDE_DMARQ				200.0000				13
	UIDE_IOCHRDY			10_MIL_SPACING	200.0000				13 24
	UIDE_INTRQ				200.0000				13
	HD_DATA<15..0>		5	TOTAL UIDE+HD SKEW <500MIL	200			100_MHz	24
	HD_ADDR<2..0>		5		200			100_MHz	24
	HD_RESET_L		5		200.0000				24
	HD_DIOW_L		5		200.0000				24
	HD_DIOR_L		5	10_MIL_SPACING	200.0000				24
	HD_DMACK_L		5		200.0000				24
	HD_CS0_L		5		200.0000				24
	HD_CS1_L		5		200.0000				24
	HD_DMARQ				200.0000				13 24
	HD_IOCHRDY		5	10_MIL_SPACING	200.0000				24
	HD_INTRQ		5						13 24
EIDE INTREPID	EIDE_DATA<15..0>							33_MHZ	13 24
	EIDE_ADDR<2..0>							33_MHZ	13 24
	EIDE_CS0_L								13 24
	EIDE_CS1_L								13 24
	EIDE_RD_L								13 24
	EIDE_WR_L								13 24
	EIDE_IOCHRDY								13 24
	EIDE_INT								13 24
	EIDE_RST_L								13 24
	EIDE_DMACK_L								13 24
	EIDE_DMARQ								13 24
OPTICAL	EIDE_OPTICAL_DATA<15..0>							33_MHZ	24 39
	EIDE_OPTICAL_ADDR<2..0>							33_MHZ	24 39
	EIDE_OPTICAL_CS0_L								24 39
	EIDE_OPTICAL_CS1_L								24 39
	EIDE_OPTICAL_RD_L								24 39
	EIDE_OPTICAL_WR_L								24 39
	EIDE_OPTICAL_IOCHRDY								24 39
	EIDE_OPTICAL_INT								24 39
	EIDE_OPTICAL_RST_L								24 39
	EIDE_OPTICAL_DMAACK_L								24 39
	EIDE_OPTICAL_DMA_RQ								24 39
ETHERNET MII	ENET_LINK_RXD<7..0>		5						13 27
	ENET_RX_DV								13 27
	ENET_RX_ER								13 27
	ENET_PHY_TXD<7..0>		5						13 27
	ENET_LINK_TXD<7..0>								13
	ENET_PHY_TX_ER		5						13 27
	ENET_LINK_TX_ER								13
	ENET_PHY_TX_EN		5						13 27
	ENET_LINK_TX_EN								13
	ENET_MDIO								13 27
	ENET_MDC								13 27
	ENET_COL								13 27
	ENET_CRS								13 27
FIREWIRE MII	FW_LINK_DATA<7..0>		5						13 28
	FW_PHY_DATA<7..0>		5						28
	FW_LINK_CNTL<1..0>								13 28
	FW_PHY_CNTL<1..0>								28
	FW_LINK_LREQ								13
	FW_PHY_LREQ								13 28
	FW_PINT								13 28

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR		MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS	
ETHERNET	MDI_M<0>	ENET_MDI0					27
	MDI_P<0>	ENET_MDI0					27
	MDI_M<1>	ENET_MDI1		SPACING DELETED BECAUSE			27
	MDI_P<1>	ENET_MDI1		OF PHYSICAL CONSTRAINTS			27
	MDI_M<2>	ENET_MDI2		AROUND MARVELL PHY			27
	MDI_P<2>	ENET_MDI2					27
	MDI_M<3>	ENET_MDI3					27
	MDI_P<3>	ENET_MDI3					27
	RJ45_DN<0>	RJ45_DP0			10_MIL_SPACING		27 39
	RJ45_DP<0>	RJ45_DP0			10_MIL_SPACING		27 39
	RJ45_DN<1>	RJ45_DP1			10_MIL_SPACING		27 39
	RJ45_DP<1>	RJ45_DP1			10_MIL_SPACING		27 39
	RJ45_DN<2>	RJ45_DP2			10_MIL_SPACING		27 39
	RJ45_DP<2>	RJ45_DP2			10_MIL_SPACING		27 39
	RJ45_DN<3>	RJ45_DP3			10_MIL_SPACING		27 39
	RJ45_DP<3>	RJ45_DP3			10_MIL_SPACING		27 39
FIREWIRE	FW_TPA0N	FW_TPA0			MIN_LINE_WIDTH=3.4 10_MIL_SPACING		28 29
	FW_TPA0P	FW_TPA0			MIN_LINE_WIDTH=3.4 10_MIL_SPACING		28 29
	FW_TPB0N	FW_TPB0			MIN_LINE_WIDTH=3.4 10_MIL_SPACING		28 29
	FW_TPB0P	FW_TPB0			MIN_LINE_WIDTH=3.4 10_MIL_SPACING		28 29
	FW_TPI0N	FW_TPI0			MIN_LINE_WIDTH=3.4 10_MIL_SPACING		
	FW_TPI0P	FW_TPI0			MIN_LINE_WIDTH=3.4 10_MIL_SPACING		
	FW_TPO0N	FW_TPO0			MIN_LINE_WIDTH=3.4 10_MIL_SPACING		
	FW_TPO0P	FW_TPO0			MIN_LINE_WIDTH=3.4 10_MIL_SPACING		
	FW_TPA1N	FW_TPA1		500.0000	MIN_LINE_WIDTH=3.4 10_MIL_SPACING		28 29
	FW_TPA1P	FW_TPA1		500.0000	MIN_LINE_WIDTH=3.4 10_MIL_SPACING		28 29
	FW_TPB1N	FW_TPB1		500.0000	MIN_LINE_WIDTH=3.4 10_MIL_SPACING		28 29
	FW_TPB1P	FW_TPB1		500.0000	MIN_LINE_WIDTH=3.4 10_MIL_SPACING		28 29
	FW_TPI1N	FW_TPI1			MIN_LINE_WIDTH=3.4 10_MIL_SPACING		29 39
	FW_TPI1P	FW_TPI1			MIN_LINE_WIDTH=3.4 10_MIL_SPACING		29 39
	FW_TPO1N	FW_TPO1			MIN_LINE_WIDTH=3.4 10_MIL_SPACING		29 39
	FW_TPO1P	FW_TPO1			MIN_LINE_WIDTH=3.4 10_MIL_SPACING		29 39
LVDS LOWER	CLKLVDS_LN	CLKLVDS_L			10_MIL_SPACING	4	19 22 39
	CLKLVDS_LP	CLKLVDS_L			10_MIL_SPACING	4	19 22 39
	LVDS_L0N	LVDS_L0			10_MIL_SPACING		19 22 39
	LVDS_L0P	LVDS_L0			10_MIL_SPACING		19 22 39
	LVDS_L1N	LVDS_L1			10_MIL_SPACING		19 22 39
	LVDS_L1P	LVDS_L1			10_MIL_SPACING		19 22 39
	LVDS_L2N	LVDS_L2			10_MIL_SPACING		19 22 39
	LVDS_L2P	LVDS_L2			10_MIL_SPACING		19 22 39
UPPER	CLKLVDS_UN	CLKLVDS_U			10_MIL_SPACING	4	19 22 39
	CLKLVDS_UP	CLKLVDS_U			10_MIL_SPACING	4	19 22 39
	LVDS_U0N	LVDS_U0			10_MIL_SPACING		19 22 39
	LVDS_U0P	LVDS_U0			10_MIL_SPACING		19 22 39
	LVDS_U1N	LVDS_U1			10_MIL_SPACING		19 22 39
	LVDS_U1P	LVDS_U1			10_MIL_SPACING		19 22 39
	LVDS_U2N	LVDS_U2			10_MIL_SPACING		19 22 39
	LVDS_U2P	LVDS_U2			10_MIL_SPACING		19 22 39
TMDS	TMDS_CONN_CLKN	CLKCONN_TMDS			10_MIL_SPACING	4	22 39
	TMDS_CONN_CLKP	CLKCONN_TMDS			10_MIL_SPACING	4	22 39
	TMDS_CLKN	CLKTMDS			10_MIL_SPACING	4	20 22
	TMDS_CLKP	CLKTMDS			10_MIL_SPACING	4	20 22
	TMDS_DN<0>	TMDS_D0			10_MIL_SPACING		20 22 39
	TMDS_DP<0>	TMDS_D0			10_MIL_SPACING		20 22 39
	TMDS_DN<1>	TMDS_D1			10_MIL_SPACING		20 22 39
	TMDS_DP<1>	TMDS_D1			10_MIL_SPACING		20 22 39
	TMDS_DN<2>	TMDS_D2			10_MIL_SPACING		20 22 39
	TMDS_DP<2>	TMDS_D2			10_MIL_SPACING		20 22 39
USB	NEC_USB_DAM	NEC_USB_DA		MIN_LINE_WIDTH=5	10_MIL_SPACING		26
	NEC_USB_DAP	NEC_USB_DA		MIN_LINE_WIDTH=5	10_MIL_SPACING		26
	USB_DEM	USB_DE			5_MIL_SPACING		14
	USB_DEP	USB_DE			5_MIL_SPACING		14
	NEC_USB_DBM	NEC_USB_DB		MIN_LINE_WIDTH=5	10_MIL_SPACING		26
	NEC_USB_DBP	NEC_USB_DB		MIN_LINE_WIDTH=5	10_MIL_SPACING		26
	USB_DFM	USB_DF			5_MIL_SPACING		14
	USB_DFP	USB_DF			5_MIL_SPACING		14
	BT_USB_DM	BT_USB_D			5_MIL_SPACING		14 24 39
	BT_USB_DP	BT_USB_D			5_MIL_SPACING		14 24 39
	NEC_USB_RSDM1	NEC_USB_RSD1		MIN_LINE_WIDTH=5	10_MIL_SPACING		26
	NEC_USB_RSDP1	NEC_USB_RSD1		MIN_LINE_WIDTH=5	10_MIL_SPACING		26
	NEC_USB_RSDM2	NEC_USB_RSD2		MIN_LINE_WIDTH=5	10_MIL_SPACING		26
	NEC_USB_RSDP2	NEC_USB_RSD2		MIN_LINE_WIDTH=5	10_MIL_SPACING		26
	MODEM_USB_DM	MODEM_USB_D			5_MIL_SPACING		14 25 39
	MODEM_USB_DP	MODEM_USB_D			5_MIL_SPACING		14 25 39
	LEFT_USB_DM	LEFT_USB		MIN_LINE_WIDTH=5	10_MIL_SPACING		24 26 39
	LEFT_USB_DP	LEFT_USB		MIN_LINE_WIDTH=5	10_MIL_SPACING		24 26 39
	RIGHT_USB_DM	RIGHT_USB		MIN_LINE_WIDTH=5	10_MIL_SPACING		26 32 39
	RIGHT_USB_DP	RIGHT_USB		MIN_LINE_WIDTH=5	10_MIL_SPACING		26 32 39
POWER SUPPLIES	1772_CSSN	1772_CSS			DIFF		31
	1772_CSSP	1772_CSS			DIFF		31
	1772_CSIN	1772_CSI			DIFF		31
	1772_CSIP	1772_CSI			DIFF		31
	3V_SNSM	3V_SNS			DIFF		33
	3V_SNSP	3V_SNS			DIFF		33
	5V_SNSM	5V_SNS			DIFF		33
	5V_SNSP	5V_SNS			DIFF		33
THERMOSTAT	THERM1_DM	THERM1			DIFF		25
	THERM1_DP	THERM1			DIFF		25
	THERM2_DM	THERM2			DIFF		25
	THERM2_DP	THERM2			DIFF		25
	THERM1_M_DM	THERM1_MATN			DIFF		
	THERM1_M_DP	THERM1_MATN			DIFF		
	THERM2_M_DM	THERM2_MATN			DIFF		
	THERM2_M_DP	THERM2_MATN			DIFF		
	THERM1_A_DM	THERM1_ALT			DIFF		25
	THERM1_A_DP	THERM1_ALT			DIFF		25
	THERM2_A_DM	THERM2_ALT			DIFF		25
	THERM2_A_DP	THERM2_ALT			DIFF		25

INTERNAL LAYER
ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.57OHM
ZDIFF = 99.8OHM

FOR FIREWIRE
ER = 4.3 (DIELECTRIC CONSTANT)
W = 3.4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 53.37OHM
ZDIFF = 107.17OHM

INTERNAL LAYER (USB1.1/USB 2.0)
ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL(USB 1.1)/ 5MIL(USB 2.0) (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 5MIL (USB 1.1) (SEPERATION OF DIFF TRACES)
S = 10MIL (USB 2.0) (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.5OHM (USB 1.1)/ 46.2OHM (USB 2.0)
ZDIFF = 89.3OHM (USB 1.1)/ 89.4OHM (USB 2.0)

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POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
MAIN/SLEEP	+24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+BATT	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	
	+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+2_5V_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	39
	+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	35
	+1_5V_SLEEP_VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	35
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31 32
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31 39
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31 39
	1772_DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	1772_LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	31
	1772_LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	31
	1772_DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	31
	1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	31
PMU	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32
	+4_85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	30 32
	+4_6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32 33
	+4_85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	25 30
MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24 33
	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24
TRACKPAD	+5V_TPAD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	23 39
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	23 39
VIDEO	+12_8V_INV	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	22
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
KB LED	KBD_LED1_OUT	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	23 39
	KBD_LED2_OUT	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	23 39
FAN GND	FANL_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 39
	FANR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 39
SOUND	+5V_SOUND_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	SND_AGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=15	25

I/O AREA	GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	
	CHGND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND1
INVERTER	CHGND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND2
TRACKPAD	CHGND3	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND3
LVDS	CHGND4	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND4 39
I/O AREA	CHGND5	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND5
I/O AREA	CHGND6	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND6
	ENET_CTAP_CHGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	27

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 6 34 39
	CPU_AVDD	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
DDR RAM	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 7 8 15 16 23 34
INTREPID	DDR_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	11
	+2_5V_INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	9 10 15 16
	+3V_INTREPID_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14
PLLS	+1_5V_INTREPID_PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	8 12 14
	+1_5V_INTREPID_PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5	14
	+1_5V_INTREPID_PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5	12
	+1_5V_INTREPID_PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	8
	+1_5V_INTREPID_PLL8	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
REFERENCE	INT_MEM_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	9
	INT_AGP_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	12 18
	INT_MEM_REF_H	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	9
	UIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	13
CARDBUS	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	MIN_NECK_WIDTH REDUCED FOR TESTPOINTS 17
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
ATI M10	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	18 19 39
	+GPU_MEM	VOLTAGE=2.5V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	18 21
	+3V_GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 18 19 21
	+3V_GPU_FLT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	21
	+1_5V_AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 15 16 18 19 21
	GPU_MEM_IO	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	GPU_MEM_IO_FLT	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+GPU_MEMCORE	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+1_8V_GPU	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18 19 20 21
	+2_5V_GPU_PNLIO	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_8V_ATI_PVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19 21
	+1_5V_AGP_GPU	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_5V_GPU_VDD15	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	+1_8V_GPU_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1331	+1_8V_GPU_VDDDI	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1332	GPU_VCORE_VDDCI	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	18
1333	+2_5V_GPU_A2VDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1334	+1_8V_GPU_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1335	+1_8V_GPU_PNLPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1336	+1_8V_GPU_PNLIO	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1337	+GPU_MCLK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1338	+1_8V_GPU_AVDDQ	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1341	+1_8V_GPU_MEMPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1342	+3V_ATI_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	18
1339	+3V_ATI_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	18
1343	+GPU_VDD15_UF	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
1344	+2_5V_SLEEP_NECK1	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
1345	+3V_SLEEP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1346	+1_5V_AGP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
1347	+1_8V_PVDD_NECK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
1348	GPU_VCORE_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
1349	+GPU_VDD15_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
1351	+2_5V_SLEEP_NECK2	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1349	+1_8V_SLEEP_NECK	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1350	+1_5V_SLEEP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1352	+2_5V_GPU	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
SILICON IMIAGE	+3V_SI_PLLVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	20
	+3V_SI_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	20
	+3V_SI_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	20
88E1111	+2_5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+2_5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
	+1_0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
	LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
FW	LM2594_IN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_ESD_ILIM	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+3V_FW_ESD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+FW_FUSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_PWR_OR	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28 29
	+FW_VP0	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_PWR_PORTA	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_VP1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+3V_FW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28 29
	+3V_FW_UF	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	28
	+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
USB 2.0	FW_TPO0R	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29 39
	NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
INTREPID SSCG	+3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+3V_CG_PLL_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	14
	+2_5V_CG_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	14

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32
	1625_VSW	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32
	1V20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	31 32
LTC3707 5V SWITCHER	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	33
	5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
3V SWITCHER	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	33
MAX1715 2.5V SWITCHER	2_5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	35
	2_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	2_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	2_5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	2_5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
1.5V SWITCHER	1_5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	1_5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	35
	1_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	1_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	1_5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	1_5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
CONTROL	1_5V_ILIM		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	2_5V_ILIM		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	MAX1715_TON		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	MAX1715_SKIP		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	MAX1715_REF	VOLTAGE=2.0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	35
MAX1717	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=200	MIN_NECK_WIDTH=10	34
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	VCORE_ILIM		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	34
	VCORE_REF		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	34
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	34
	VCORE_CC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	34
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	34 39
	VCORE_TIME		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	34
	VCORE_VGATE		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	14 34
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=15	34
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	34
	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	34
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	34
LTC1778	1778_VIN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	19
	1778_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	1778_BST_RC	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	1778_TG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_BG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	GPU_VCORE_SW	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	19
	1778_ION		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19
	1778_ITH		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19
	1778_ITH_RC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19
	1_5V_2_5V_OK		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	1778_VFB		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19 39
	1778_FCB		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19
	1778_VRNG		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19
LTC3411	LTC3411_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC3411_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	
	1_8V_SW	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	35
	1_8V_VFB		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
	LTC3411_ITH_RC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
	LTC3411_ITH		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
	LTC3411_SYNC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
	LTC3411_SHDN		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
LTC1962 INT PLLS	LTC1962_INT_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	14
	LTC1962_L3_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_L3_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_1V5_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_1V5_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	

SIGNAL CONSTRAINTS - PAGE 3

APPLE COMPUTER INC.

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SCALE: NONE	SHT 38 OF 44	

FUNCTIONAL TEST POINTS

FUNC_TEST=YES JTAG_ASIC_TMS 13 27
FUNC_TEST=YES JTAG_ASIC_TDI 27
FUNC_TEST=YES JTAG_ASIC_TDO 13 14
FUNC_TEST=YES JTAG_ASIC_TCK 13 27
FUNC_TEST=YES JTAG_ASIC_TRST_L 13 27
FUNC_TEST=YES CPU_CHKSTP_OUT_L 5
FUNC_TEST=YES CPU_SRESET_L 5
FUNC_TEST=YES CPU_HRESET_L 5 7 23
FUNC_TEST=YES JTAG_CPU_TMS 5 23
FUNC_TEST=YES JTAG_CPU_TDI 5 23
FUNC_TEST=YES JTAG_CPU_TDO_TP 5
FUNC_TEST=YES JTAG_CPU_TCK 5 23
FUNC_TEST=YES JTAG_CPU_TRST_L 5 23 39

FUNC_TEST=YES TMDS_CONN_CLKP 22 37
FUNC_TEST=YES VGA_R 22
FUNC_TEST=YES VGA_G 22
FUNC_TEST=YES VGA_B 22
FUNC_TEST=YES VGA_VSYNC 22
FUNC_TEST=YES VGA_HSYNC 22
FUNC_TEST=YES DVI_DDC_CLK_UF 22
FUNC_TEST=YES DVI_DDC_DATA_UF 22
FUNC_TEST=YES DVI_HPD_UF 22
FUNC_TEST=YES LVDS_L0N 19 22 37
FUNC_TEST=YES LVDS_L0P 19 22 37
FUNC_TEST=YES LVDS_L1N 19 22 37
FUNC_TEST=YES LVDS_L1P 19 22 37
FUNC_TEST=YES LVDS_L2N 19 22 37
FUNC_TEST=YES LVDS_L2P 19 22 37
FUNC_TEST=YES CLKLVDS_LN 19 22 37
FUNC_TEST=YES CLKLVDS_LP 19 22 37
FUNC_TEST=YES LVDS_U0N 19 22 37
FUNC_TEST=YES LVDS_U0P 19 22 37
FUNC_TEST=YES LVDS_U1N 19 22 37
FUNC_TEST=YES LVDS_U1P 19 22 37
FUNC_TEST=YES LVDS_U2N 19 22 37
FUNC_TEST=YES LVDS_U2P 19 22 37
FUNC_TEST=YES CLKLVDS_UN 19 22 37
FUNC_TEST=YES CLKLVDS_UP 19 22 37
FUNC_TEST=YES LVDS_DDC_CLK 19 22
FUNC_TEST=YES LVDS_DDC_DATA 19 22
FUNC_TEST=YES BRIGHT_PWM 22
FUNC_TEST=YES TV_GND1 22 38
FUNC_TEST=YES TV_GND2 22 38

FUNC_TEST=YES TV_C 22
FUNC_TEST=YES TV_Y 22
FUNC_TEST=YES TV_COMP 22
FUNC_TEST=YES SND_TO_AUDIO 14 25
FUNC_TEST=YES SND_SYNC 14 25
FUNC_TEST=YES SND_CLKOUT 14 25 36

FUNC_TEST=YES INT_AUDIO_TO_SND 14 25
FUNC_TEST=YES SND_SCLK 14 25 36
FUNC_TEST=YES SND_HW_RESET_L 14 25
FUNC_TEST=YES SND_HP_SENSE_L 14 25
FUNC_TEST=YES SND_LIN_SENSE_L 14 25
FUNC_TEST=YES INT_I2C_DATA2 14 25
FUNC_TEST=YES INT_I2C_CLK2 14 25
FUNC_TEST=YES CHGND4 38
FUNC_TEST=YES SLEEP_LED 23 25

FUNC_TEST=YES INT_I2C_CLK0 11 13 23
FUNC_TEST=YES INT_I2C_DATA0 11 13 23
FUNC_TEST=YES INT_I2C_CLK1 13 14 25
FUNC_TEST=YES INT_I2C_DATA1 13 14 25
FUNC_TEST=YES CBUS_DET_1_L 17
FUNC_TEST=YES CBUS_DET_2_L 17
FUNC_TEST=YES TMDS_DN<0> 20 22 37
FUNC_TEST=YES TMDS_DP<0> 20 22 37
FUNC_TEST=YES TMDS_DN<1> 20 22 37
FUNC_TEST=YES TMDS_DP<1> 20 22 37
FUNC_TEST=YES TMDS_DN<2> 20 22 37
FUNC_TEST=YES TMDS_DP<2> 20 22 37
FUNC_TEST=YES TMDS_CONN_CLKN 22 37

FUNC_TEST=YES BT_USB_DM 14 24 37
FUNC_TEST=YES BT_USB_DP 14 24 37
FUNC_TEST=YES MODEM_USB_DM 14 25 37
FUNC_TEST=YES MODEM_USB_DP 14 25 37
FUNC_TEST=YES PCI_AD<0> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<1> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<2> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<3> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<4> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<5> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<6> 9 12 17 24 26 37

FUNC_TEST=YES PCI_AD<7> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<8> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<9> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<10> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<11> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<12> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<13> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<14> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<15> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<16> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<17> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<18> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<19> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<20> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<21> 12 17 24 26 37
FUNC_TEST=YES PCI_AD<22> 12 17 24 26 37
FUNC_TEST=YES PCI_AD<23> 12 17 24 26 37
FUNC_TEST=YES PCI_AD<24> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<25> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<26> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<27> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<28> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<29> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<30> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<31> 9 12 17 24 26 37
FUNC_TEST=YES PCI_FRAME_L 12 17 24 26 37
FUNC_TEST=YES PCI_TRDY_L 12 17 24 26 37
FUNC_TEST=YES PCI_IRDY_L 12 17 24 26 37
FUNC_TEST=YES PCI_DEVSEL_L 12 17 24 26 37
FUNC_TEST=YES PCI_STOP_L 12 17 24 26 37

FUNC_TEST=YES PCI_PAR 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<0> 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<1> 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<2> 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<3> 12 17 24 26 37
FUNC_TEST=YES AIRPORT_PCI_REQ_L 12 24
FUNC_TEST=YES AIRPORT_PCI_GNT_L 12 24
FUNC_TEST=YES AIRPORT_PCI_INT_L 14 24
FUNC_TEST=YES EIDE_OPTICAL_DATA<0> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<1> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<2> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<3> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<4> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<5> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<6> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<7> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<8> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<9> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<10> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<11> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<12> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<13> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<14> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<15> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DMA_RQ 24 37
FUNC_TEST=YES EIDE_OPTICAL_RD_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_DMAACK_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_ADDR<0> 24 37
FUNC_TEST=YES EIDE_OPTICAL_ADDR<1> 24 37
FUNC_TEST=YES EIDE_OPTICAL_ADDR<2> 24 37
FUNC_TEST=YES SND_AMP_MUTE 25
FUNC_TEST=YES SND_HP_MUTE_INV 25

FUNC_TEST=YES EIDE_OPTICAL_CS0_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_CS1_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_RST_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_WR_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_IOCHRDY 24 37
FUNC_TEST=YES EIDE_OPTICAL_INT 24 37
FUNC_TEST=YES TPAD_F_TXD 23
FUNC_TEST=YES TPAD_F_RXD 23
FUNC_TEST=YES LID_CLOSED_L 23
FUNC_TEST=YES COMM_RESET_L 14 25
FUNC_TEST=YES COMM_SHUTDOWN 14 25
FUNC_TEST=YES COMM_RING_DET_L 14 25 30
FUNC_TEST=YES KBD_ID 23 30
FUNC_TEST=YES +5V_TPAD_SLEEP 23 38
FUNC_TEST=YES +3V_HALL_EFFECT 23 38
FUNC_TEST=YES KBD_CAPSLOCK_LED 23
FUNC_TEST=YES KBD_FUNCTION_L 23 30
FUNC_TEST=YES KBD_CONTROL_L 23 30
FUNC_TEST=YES KBD_COMMAND_L 23 30
FUNC_TEST=YES KBD_OPTION_L 23 30
FUNC_TEST=YES KBD_SHIFT_L 23 30
FUNC_TEST=YES KBD_X<0> 23 30
FUNC_TEST=YES KBD_X<1> 23 30
FUNC_TEST=YES KBD_X<2> 23 30
FUNC_TEST=YES KBD_X<3> 23 30
FUNC_TEST=YES KBD_X<4> 23 30
FUNC_TEST=YES KBD_X<5> 23 30
FUNC_TEST=YES KBD_X<6> 23 30
FUNC_TEST=YES KBD_X<7> 23 30
FUNC_TEST=YES KBD_X<8> 23 30
FUNC_TEST=YES SRCLK_TP 26
FUNC_TEST=YES SRMOD_TP 26
FUNC_TEST=YES TEB_TP 26
FUNC_TEST=YES TEST_TP 26

FUNC_TEST=YES KBD_X<9> 23 30
FUNC_TEST=YES KBD_Y<0> 23 30
FUNC_TEST=YES KBD_Y<1> 23 30
FUNC_TEST=YES KBD_Y<2> 23 30
FUNC_TEST=YES KBD_Y<3> 23 30
FUNC_TEST=YES KBD_Y<4> 23 30
FUNC_TEST=YES KBD_Y<5> 23 30
FUNC_TEST=YES KBD_Y<6> 23 30
FUNC_TEST=YES KBD_Y<7> 23 30
FUNC_TEST=YES KBD_NUMLOCK_LED 23
FUNC_TEST=YES +BATT_POS 31 38
FUNC_TEST=YES BATT_CLK 31
FUNC_TEST=YES BATT_DATA 31
FUNC_TEST=YES BATT_NEG 31 38
FUNC_TEST=YES PMU_BATT_DET_L 30 31
FUNC_TEST=YES FANR_GND 25 38
FUNC_TEST=YES FANL_GND 25 38
FUNC_TEST=YES FANL_TACH 25
FUNC_TEST=YES FANR_PWM 25
FUNC_TEST=YES FANL_PWM 25
FUNC_TEST=YES RJ45_DP<0> 27 37
FUNC_TEST=YES RJ45_DN<0> 27 37
FUNC_TEST=YES RJ45_DP<1> 27 37
FUNC_TEST=YES RJ45_DN<1> 27 37
FUNC_TEST=YES RJ45_DP<2> 27 37
FUNC_TEST=YES RJ45_DN<2> 27 37
FUNC_TEST=YES RJ45_DP<3> 27 37
FUNC_TEST=YES RJ45_DN<3> 27 37
FUNC_TEST=YES FW_TPOOR 29 38
FUNC_TEST=YES VCORE_VID0
FUNC_TEST=YES VCORE_VID1
FUNC_TEST=YES VCORE_VID2
FUNC_TEST=YES VCORE_VID3
FUNC_TEST=YES VCORE_VID4

FUNC_TEST=YES FW_TPO1P 29 37
FUNC_TEST=YES FW_TPO1N 29 37
FUNC_TEST=YES FW_TPI1P 29 37
FUNC_TEST=YES FW_TPI1N 29 37
FUNC_TEST=YES CHARGE_LED_L 30 31
FUNC_TEST=YES ADAPTER_DET 30 31
FUNC_TEST=YES SUTRO_ALS_GAIN_SW 23 24
FUNC_TEST=YES SUTRO_ALS_OUT 23 24
FUNC_TEST=YES KBD_LED1_OUT 23 38
FUNC_TEST=YES KBD_LED2_OUT 23 38
FUNC_TEST=YES COMM_TXD_L 14 25
FUNC_TEST=YES COMM_TRXC 14 25
FUNC_TEST=YES COMM_GPIO_L 14 25
FUNC_TEST=YES COMM_DTR_L 14 25
FUNC_TEST=YES COMM_RTS_L 14 25
FUNC_TEST=YES COMM_RXD 14 25
FUNC_TEST=YES PMU_KB_RESET_L 30
FUNC_TEST=YES PWR_BUTTON_L 23 25
FUNC_TEST=YES +PBUS 38
FUNC_TEST=YES +24V_PBUS 38
FUNC_TEST=YES GPU_VCORE 18 19 38
FUNC_TEST=YES CPU_VCORE_SLEEP 5 6 34 38
FUNC_TEST=YES VCORE_FB 34 38
FUNC_TEST=YES +1_8V_MAIN 38
FUNC_TEST=YES +3V_PMU 38
FUNC_TEST=YES +5V_DDC_SLEEP 22 38
FUNC_TEST=YES +12_8V_INV 22 38
FUNC_TEST=YES VCORE_MUX_EN 34

FUNC_TEST=YES +5V_INV_SW 22 38
FUNC_TEST=YES LEFT_USB_DM 24 26 37
FUNC_TEST=YES LEFT_USB_DP 24 26 37
FUNC_TEST=YES RIGHT_USB_DM 26 32 37
FUNC_TEST=YES RIGHT_USB_DP 26 32 37
FUNC_TEST=YES NEC_LEFT_USB_PWREN 24 26
FUNC_TEST=YES NEC_LEFT_USB_OVERCURRENT 24 26
FUNC_TEST=YES NEC_RIGHT_USB_PWREN 26 32
FUNC_TEST=YES NEC_RIGHT_USB_OVERCURRENT 26 32
FUNC_TEST=YES DCDC_EN 19 29 33 34
FUNC_TEST=YES BBANG_HRESET_L 23
FUNC_TEST=YES MAIN_RESET_L 14 17 18 20 24 26 30
FUNC_TEST=YES RF_DISABLE_L_SPN 24
FUNC_TEST=YES AIRPORT_CLKRUN_L 24
FUNC_TEST=YES ROM_RW_L 9 12 24
FUNC_TEST=YES ROM_ONBOARD_CS_L 9 24
FUNC_TEST=YES ROM_CS_L 9 12 24
FUNC_TEST=YES CLK33M_AIRPORT 12 24 36
FUNC_TEST=YES AIRPORT_IDSEL 24
FUNC_TEST=YES ROM_OE_L 9 12 24
FUNC_TEST=YES INT_MOD_DTI 14 25
FUNC_TEST=YES JTAG_CPU_TRST_L 5 23 39
FUNC_TEST=YES MOD_BITCLK 14 25
FUNC_TEST=YES MOD_CLKOUT 14 25
FUNC_TEST=YES MOD_DTO 14 25
FUNC_TEST=YES MOD_SYNC 14 25
FUNC_TEST=YES SLEEP 23 25 30 33 35
FUNC_TEST=YES 1778_VFB 19 38

APPLE COMPUTER INC.

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REVISION HISTORY (051-6654)

12/11/03

1) IMPORTED Q41 PRODUCTION RELEASE SCHEMATIC
2) CHANGED CPU (U43) TO A7PM
3) CHANGED PLL CONFIG STUFFING FOR NEW CPU
4) CHANGED U44 TO M1Y-PSP64 SYMBOL
5) ADDED CPU AVDD LDO (U6)
6) ADDED R284 AND R604 TO ADD OPTION FOR PD_I OF U42 (CLOCK CHIP) TO BE DRIVEN BY JTAG_ASIC_TDO FROM INTREPID
7) ADDED R608 TO DISCONNECT INT GPIO0 FROM CG FSEL
8) CHANGED JTAG_ASIC_TDO TP TO JTAG_ASIC_TDO AND MOVED IT TO INTREPID'S TDO
9) CHANGED JTAG_ASIC_TDI TO CONNECT TO ETHERNET PHY'S TDI

12/15/03

10) CHANGED PIN 4 (DCDC_EN) ON J11 TO NEC_RIGHT_USBOVERCURRENT
11) CHANGED PIN 11 OF J11 TO NC

12/16/03

12) ADDED R633 AS PULLUP ON JTAG_ASIC_TDI
13) CHANGED CPU_TEMP_DM TO CPU_THERM_DM
14) CHANGED CPU_TEMP_DP TO CPU_THERM_DP
15) CHANGED GPU_THERM_DP TO GPU_THERM_DP_TP
16) CHANGED GPU_THERM_DM TO GPU_THERM_DM_TP
17) FIXED MISSED CONNECTION WITH MAXBUS_SLEEP TO CPU

12/17/03

18) CHANGED R657 (EXTPLL_SDWN_POL BOOT STRAP) TO NO STUFF AND REMOVED NO STUFF FROM R153
19) UPDATE DIFF NET SPACING TYPE PROPERTY ON POWER SUPPLY SENSE AND THERMAL DIODE DIFF PAIRS
20) CHANGED FIREWIRE OSCILLATOR (G1) TO NEW PREFERRED SUNNY PART

12/18/03

21) CHANGED MAX VIA COUNT ON ALL AGP STB NETS TO 5 TO CLEAR DRCS

** RELEASED FOR EVT **

2/10/04

22) REMOVED XW11 - JUMPER ON 1.8V SWITCHER OUTPUT
23) CHANGED R657 TO STUFFE AND R153 TO NO STUFF
24) CHANGED CPU PLL CONFIG TO 9X HIGH AND 5X LOW

** RELEASED FOR DVT **

3/24/04

25) REMOVED ALTERNATE BOM OPTION FROM ALTERNATE ETHERNET CRYSTALS

3/29/04

26) ADDED ALTERNATE FOR Q41A REV 1.1.1 CPU (U43)
27) ADDED ALTERNATES FOR 128MB AND 64MB A16 M11'S
28) CHANGED TMDS SERIES RPAKS TO 0 OHMS (RP57,RP27,RP32,RP28)
29) ADDED ALTERNATE FOR ALS OP-AMP (U40)

** RELEASED TO REV A **

30) CHANGED TMDS TERMINATION R,C AND LS TO PRODUCTION VALUES

** RELEASED TO REV A UNDER NEW PART NUMBER **

7/6/05

ADDED 338S0223 (88E1111 REV. B1) AS AN ALTERNATE OF 338S0079

8/22/05

REPLACED 740S0006 EITH 740S0018 (FUSE,1.5A,24V,SMD,LF)
ADDED 128S0022 (220 UF) AS AN ALTERNATE OF 128S0034 (330 UF) FOR MPU VCORE CAPS
ADDED LABELS WITH EEE

** RELEASED TO 051-6654-C **

REVISION HISTORY (051-7202)

07/07/2006

INITIAL DRAFT REV A FOR 17" Q41A SERVICE BOM (FROM 051-6654-C)
1) CHANGED THE DOCUMENT TITLE INFO.
2) CHANGED THE BOM OPTION FROM 341S1645 TO 341S1940 (PAGE-9).
3) CHANGED THE BOM OPTION ALTERNATE FROM 338S0182/338S0183 TO 338S0214/338S0207 (PAGE-18).

07/07/2006

REVISED TO REV B WITH BELOW CHANGES:
1) CORRECT THE TYPO 051-6654 TO 051-7202 IN BOM OPTION (PAGE-01).
2) CHANGED THE 826- P/N BACK TO 826-4393 (PAGE-01).
3) UPDATED THE REVISION TO REV B.

APPLE COMPUTER INC.

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8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

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*** Signal Cross-Reference for the entire design ***

+1_0V_MARVELL     27D2< 38B3>
+1_5V_AGP         12C5< 12D1< 12D4< 15D5< 16C8<
                  18C6< 18D6< 19A8< 19B4<> 19D5<>
                  21B8< 21D6< 38C3>
+1_5V_AGP_GPU     21C5< 38C3>
+1_5V_AGP_NECK    19B4<> 38B3>
+1_5V_GPU_VDD15   19D3< 38C3>
+1_5V_INTREPID_PLL  8D6< 12D4< 12D8< 14D6<> 38D3>
+1_5V_INTREPID_PLL1  14C3< 38D3>
+1_5V_INTREPID_PLL2  14D3< 38D3>
+1_5V_INTREPID_PLL3  14D3< 38D3>
+1_5V_INTREPID_PLL4  14D3< 38D3>
+1_5V_INTREPID_PLL5  12D3< 38D3>
+1_5V_INTREPID_PLL6  12D6< 38D3>
+1_5V_INTREPID_PLL7  8D5< 38D3>
+1_5V_INTREPID_PLL8  14D3< 38D3>
+1_5V_LDO         35D8< 38D6>
+1_5V_MAIN        38D6>
+1_5V_SLEEP       38D6>
+1_5V_SLEEP_NECK  21A3<> 38B3>
+1_5V_SLEEP_VIN   35D8<> 38D6>
+1_8V_ATI_PVDD    19C5<> 21B6< 21B6< 21D6<> 38C3>
+1_8V_ATI_TPVDD   21D2<>
+1_8V_DVO_F       21B2<
+1_8V_GPU         18A7< 19D8< 20A5< 21A2< 21A6<
                  21B1< 21B6< 21C8< 21D6< 21D8< 38C3>
+1_8V_GPU_AVDD    21D5< 38C3>
+1_8V_GPU_AVDDQ   21D4< 21D7< 38C3>
+1_8V_GPU_MEMPLL  21B5< 38C3>
+1_8V_GPU_PLL     21D5< 38C3>
+1_8V_GPU_PNLIO   21A5< 38C3>
+1_8V_GPU_PNLPLL  21B5< 38C3>
+1_8V_GPU_TP_PLL  21B4< 21D1<
+1_8V_GPU_VDDDI   21C7< 21D4< 38C3>
+1_8V_MAIN        38D6> 39A2>
+1_8V_PVDD_NECK   19B5<> 38B3>
+1_8V_SLEEP       38D6>
+1_8V_SLEEP_NECK  21A3<> 38B3>
+1_95V_FW_DVDD    28C4< 28C7<> 28D5< 38A3>
+1_95V_FW_DVDD_PORT1  28D6< 38A3>
+1_95V_FW_DVDD_RX0  28C5< 38A3>
+1_95V_FW_DVDD_TX0  28C5< 38A3>
+1_95V_FW_PLL400VDD  28D5< 38A3>
+1_95V_FW_PLL500VDD  28D5< 38A3>
+1_95V_FW_PLLVDD  28D5< 28D7<> 38A3>
+2_5V_CG_MAIN     14C6< 38A3>
+2_5V_GPU         21A8< 21B6< 21D3< 21D7< 21D8<
                  38B3>
+2_5V_GPU_A2VDD   21D4< 21D7< 38C3>
+2_5V_GPU_PNLIO   21A5< 38C3>
+2_5V_INTREPID    9A8< 10D3< 10D5< 10D6< 10D8< 15D7<
                  16B8< 38D3>
+2_5V_MAIN        38D6>
+2_5V_MARVELL     27B8< 27C4<> 38B3>
+2_5V_MARVELL_AVDD  27C4< 38B3>
+2_5V_SLEEP       38D6>
+2_5V_SLEEP_NECK1  19C4<> 38B3>
+2_5V_SLEEP_NECK2  21A3<> 38B3>
+2_8V_GPU_LVDS_LDO  21A6<>
+3V_ATI_OSC_SLEEP  18D2< 38C3>
+3V_ATI_SS        18B2< 38C3>
+3V_CG_PLL_MAIN   14C6< 38A3>
+3V_FW            28A3< 28D7<> 29D5< 38A3>
+3V_FW_AVDD       28C6< 38A3>
+3V_FW_AVDD_PORT0  28C6< 38A3>
+3V_FW_AVDD_PORT1  28C6< 38A3>
+3V_FW_AVDD_PORT2  28D6< 38A3>
+3V_FW_ESD        29B3<> 29D2<> 38B3>
+3V_FW_ESD_ILIM   29D4< 38B3>
+3V_FW_UF         28D7<> 38A3>
+3V_GPU           12D1< 18B8< 18C5< 18C7< 18D6<
                  19C4< 19C6< 19C7< 19D7< 21A7< 21B1<
                  21B8< 38C3>
+3V_GPU_FLT       21B2< 38C3>
+3V_GPU_SI        20C4< 20C8< 20D8<
+3V_HALL_EFFECT   23C6<> 38B6> 39C4>
+3V_INTREPID_USB  14C3< 38D3>
+3V_LCD           22B4<> 38B6>
+3V_LCD_SW        22A4<> 38B6>
+3V_MAIN          38D6>
+3V_NEC_VDD       26D7< 26D7< 38A3>
+3V_PMU           38D6> 39A2>
+3V_PMU_AVCC      25A4< 30B6< 30D5<> 38C6>
+3V_PMU_ESR       32A2< 38C6>
+3V_PMU_RESET     30B7< 34A3<>
+3V_SI_AVCC       20C7< 38B3>
+3V_SI_PLLVCC     20C7< 38B3>
+3V_SI_VCC        20C6< 38B3>
+3V_SLEEP         38D6>
+3V_SLEEP_NECK    21A3<> 38B3>
+3V_SLP_OK_L      33B4<>
+3V_SLP_ON        33A5<>
+4_6V_BU          32A3<> 33B7< 38C6>
+4_85V_ESR        32A4< 38C6>
+4_85V_RAW        30B4< 32A4<> 38C6>
+5V_DDC_SLEEP     22D3<> 22D5<> 38B6> 39A2>
+5V_DDC_SLEEP_UF  22D6< 38B6>
+5V_HD_SLEEP      24D1<> 33A7<> 38C6>
+5V_INV_SW        22B1<> 38B6> 39D1>
+5V_INV_UF_SW     22B2<> 38B6>
+5V_MAIN          38D6>
+5V_SLEEP         38D6>
+5V_SOUND_SLEEP   38B6>
+5V_TPAD_SLEEP    23C7<> 38B6> 39C4>
+12_8V_INV        22B1<> 38B6> 39A2>
+24V_PBUS         38D6> 39B2>
+ADAPTER          31D8<> 32B7< 38D6>
+ADAPTER_ILIM     32B6<> 38C6>
+ADAPTER_OR_BATT  32A5<> 38C6>
+ADAPTER_SENSE    31D5<> 38C6>
+ADAPTER_SW       31D6<> 38C6>
+BATT             38D6>
+BATT_14V_FUSE    31D1<> 38C6>
+BATT_24V_FUSE    31B1< 31D2<> 38C6>
+BATT_POS         31A4<> 38C6> 39C3>
+BATT_RSNS        31B2< 38C6>
+BATT_VSNS        31A4< 38C6>
+FW_FUSE          29D7<> 38A3>
+FW_PWR_OR        28B8< 28D8<> 29D5<> 38A3>
+FW_PWR_PORTA     29C5< 38A3>
+FW_SW            29D5<> 38A3>
+FW_VP0           29C2<> 38A3>
+FW_VP1           29A3<> 38A3>
+GPU_MCLK         21C7< 21D4< 38C3>
+GPU_MEM          18A6<> 18B8< 21B4< 21B7< 21C6<
                  21C8< 21D2< 38C3>
+GPU_MEMCORE      21C5< 38C3>
+GPU_VDD15_NECK   19B5<> 38B3>
+GPU_VDD15_UF     19B5<> 19D4<> 38C3>
+HD_LOGIC_SLEEP   24C2<> 38C6>
+PBUS             38D6> 39B2>
+VCC_CBUS_SW      17B1<> 17B2<> 17D2<> 38D3>
+VPP_CBUS_SW      17B1<> 17B2<> 17D2<> 38C3>
1V20_REF          31C7< 32C8< 38D1>
1V65_REF          31A5<
1_5V_2_5V_OK      35C5> 38B1>
1_5V_BOOST        35C6<> 38C1>
1_5V_BST          35C5<> 38C1>
1_5V_DH           35C5<> 38C1>
1_5V_DL           35B5<> 38C1>
1_5V_FB           35B5< 35B7< 38C1>
1_5V_ILIM         35C5<> 38C1>
1_5V_LX           35B5<> 38C1>
1_5V_SLEEP_EN_L   35C7<> 35D7<>
1_8V_SLEEP_PWREN_L  35A3<>
1_8V_SW           35A5<> 38A1>
1_8V_VFB          38A1>
2_5V_BOOST        35C4<> 38D1>
2_5V_BST          35C4<> 38D1>
2_5V_DH           35C4<> 38D1>
2_5V_DL           35B4<> 38D1>
2_5V_ILIM         35C5<> 38C1>
2_5V_LX           35B4<> 38D1>
2_5V_SLEEP_PWREN_L  35C2<>
2_34V_REF         30A4<
3V_5V_OK          33B4<> 35A8<> 35D6<
3V_5V_OK_INV      35A8<>
3V_BG             33C4<>
3V_BOOST          33C4<>
3V_BOOST_ESR      33D3<>
3V_ITH            33C4<>
3V_ITH_RC         33C3<
3V_PMU_VTAP       32B3<
3V_RSNS           33D2< 38D1>
3V_RUNSS          33C4<
3V_SLEEP_PWREN_L  33A3<>

3V_SNSM           33C4< 37A2>
3V_SNSP           33C4< 37A2>
3V_SW             33C4<> 38D1>
3V_TG             33D4<>
3V_VOSNS          33C4<>
5V_BG             33C5<>
5V_BOOST          33C5<>
5V_BOOST_ESR      33D6<>
5V_HD_PWREN       33A8<>
5V_ITH            33C5<>
5V_ITH_RC         33C6<
5V_RSNS           33D7< 38D1>
5V_RUNSS          33C5<
5V_SLEEP_PWREN    33A8<>
5V_SNSM           33C5< 37A2>
5V_SNSP           33C5< 37A2>
5V_SW             33C5<> 38D1>
5V_TG             33C5<>
5V_VOSNS          33C5<>
1625_BG           32C5<>
1625_BST          32C5<
1625_BST_ESR      32C5<>
1625_COMP         31D2< 32C6<
1625_DIV          32C8<
1625_ENABLE       32D7<>
1625_ENABLE_L     32D6<>
1625_EXTVCC       32D5<> 38D1>
1625_FCB          32C6<
1625_INTVCC       32C5<> 38D1>
1625_RUNSS        32C6<
1625_SGND         32B7<> 38D1>
1625_TG           32C5<>
1625_VFB          32B5<>
1625_VIN          32C6< 38D1>
1625_VSW          32C4<> 38D1>
1772_ACIN         31B5<
1772_ACOK_L       31B5<> 31C4<>
1772_BST          31B4<>
1772_BST_ESR      31C3<
1772_CCI          31B5<>
1772_CCS          31B5<
1772_CCV          31B5<>
1772_CCV_RC       31B5<
1772_CELLS        31B4<
1772_CLS          31A4<
1772_CSIN         31B4<> 37A2>
1772_CSIP         31B4<> 37A2>
1772_CSSN         31C5< 37A2>
1772_CSSP         31C5< 37A2>
1772_DCIN         31B5< 38C6>
1772_DHI          31B4<>
1772_DLO          31B4<>
1772_DLOV         31B4<> 38C6>
1772_GND          31A5<> 38C6>
1772_ICHG         31B5<>
1772_ICTL         31B5<>
1772_IINP         31B5<
1772_LDO          31C4<> 38C6>
1772_LX           31B4<> 38C6>
1772_REF          31B5<>
1772_VCTL         31B5<
1778_BG           19A5<> 38B1>
1778_BST          19A5<> 38B1>
1778_BST_RC       19A4<> 38B1>
1778_FCB          19A5< 38B1>
1778_GND          19A5< 19A7<> 38B1>
1778_ION          19A5< 38B1>
1778_ITH          19A5<> 38B1>
1778_ITH_RC       19A7< 38B1>
1778_SHDN_L       19A6<
1778_SHDN_L_D3COLD  19A7<>
1778_TG           19A5<> 38B1>
1778_VCC          19A5<> 38B1>
1778_VFB          19A2< 19A5< 38B1> 39A1>
1778_VIN          19A5< 38B1>
1778_VRNG         19A5< 38B1>
3405_MODE         27D5<
3405_VFB          27D4<>
3707_FCB          33C5<
3707_FSET         33C5<
3707_INTVCC       33D4<> 38D1>
3707_SGND         33B5<> 38D1>
3707_STBY         33C5<>
A29_CLS_ADJ       31A5<>
A29_CURRENT_ADJ   31C4<>
A29_DETECT        30A2< 31A5<> 31C4<>
A29_DET_L         30A3<
AB_SEL_LOW        34A6<>
AC_DIV            31C8<
AC_ENABLE_GATE    31D6<>
AC_ENABLE_L       31C6<>
AC_GTR_18V        31C4<>
AC_IN             27B8<> 29C7< 30B3< 31C5<> 31C7<>
AC_IN_FW_CNTL     29C7<>
AC_IN_L           31C2<> 31C6<>
AC_IN_L_RC        31C2<>
ADAPTER_DET       30A4< 31D8<> 39C2>
ADAPTER_I_REG     31D3<>
ADT7460_ADR_EN_L  25B3<>
ADT7460_FAN1_PWM  25B3<>
ADT7460_FAN2_PWM  25B3<>
ADT7460_THERM     25A5<> 25B3<>
ADT7460_VCC       25C4<
ADT7460_VCORE_MON  5C8<> 25B4<>
AGP8X_DET_PU      18C6<>
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AGP_AD<15..0>     37D5>
AGP_AD<1>         12C2<> 18C7<>
AGP_AD<2>         12C2<> 18C7<>
AGP_AD<3>         12C2<> 18C7<>
AGP_AD<4>         12C2<> 18C7<>
AGP_AD<5>         12C2<> 18C7<>
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AGP_AD<12>        12C2<> 18C7<>
AGP_AD<13>        12C2<> 18C7<>
AGP_AD<14>        12C2<> 18C7<>
AGP_AD<15>        12C2<> 18C7<>
AGP_AD<16>        12C2<> 18C7<>
AGP_AD<31..16>    37D5>
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AGP_AD<18>        12C2<> 18C7<>
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AGP_AD<20>        12C2<> 18C7<>
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AGP_AD<28>        12B2<> 18D7<>
AGP_AD<29>        12B2<> 18D7<>
AGP_AD<30>        12B2<> 18D7<>
AGP_AD<31>        12B2<> 18D7<>
AGP_AD_STB<0>     12A2<> 12B2< 18D6<> 37D5>
AGP_AD_STB<1>     12A2<> 12B2< 18D6<> 37D5>
AGP_AD_STB_L<0>   12A2<> 12B2< 18D6<> 37D5>
AGP_AD_STB_L<1>   12A2< 12A2<> 18D6<> 37D5>
AGP_ATI_RESET_L   18B7<
AGP_ATI_VREF      18B7<
AGP_ATI_VREFG     18B7<
AGP_BUSY_L        12C4<> 12D2< 18D6>
AGP_CBE<0>        12B2<> 18B7<>
AGP_CBE<1..0>     37D5>
AGP_CBE<1>        12B2<> 18B7<>
AGP_CBE<2>        12B2<> 18B7<>
AGP_CBE<3..2>     37D5>
AGP_CBE<3>        12B2<> 18C7<>
AGP_DEVSEL_L      12B2<> 12C2< 18B7<> 37D5>
AGP_FRAME_L       12B2<> 12C2< 18B7<> 37D5>
AGP_GNT_L         12C2< 12D2<> 18B7< 37D5>
AGP_INT_L         14B5<> 18B7<>
AGP_IRDY_L        12B2<> 12C2< 18B7<> 37D5>
AGP_PAR           12B2<> 18B7> 37D5>
AGP_PIPE_L        12A2<> 12B2<
AGP_RBF_L         12A2<> 12C2< 18C6<> 37D5>
AGP_REQ_L         12C2< 12D2<> 18B7<> 37D5>
AGP_SBA<0>        12B2< 18C6>
AGP_SBA<7..0>     37D5>
AGP_SBA<1>        12B2<> 18C6>
AGP_SBA<2>        12B2<> 18C6>
AGP_SBA<3>        12B2<> 18C6>
AGP_SBA<4>        12B2<> 18C6>

AGP_SBA<5>        12B2<> 18C6>
AGP_SBA<6>        12B2<> 18C6>
AGP_SBA<7>        12B2<> 18C6<>
AGP_SB_STB        12B2< 12B2<> 18C6<> 37D5>
AGP_SB_STB_L      12A2< 12A2<> 18C6<> 37D5>
AGP_ST<0>         12A2<> 18C6<
AGP_ST<1>         12A2<> 18C6<
AGP_ST<2>         12A2<> 18C6<
AGP_STOP_L        12B2<> 12C2< 18B7<> 37D5>
AGP_STP_L         18C6<
AGP_SUS_STAT_L_PU  18C6<
AGP_TRDY_L        12B2<> 12C2< 18B7<> 37D5>
AGP_WBF_L         12A4<> 12B2< 18B7>
AIRPORT_CLKRUN_L  24C6<> 39C1>
AIRPORT_IDSEL     24C5<> 39B1>
AIRPORT_PCI_GNT_L  12D7<> 24D5<> 39C4>
AIRPORT_PCI_INT_L  14B5<> 14D7< 24D5<> 39C4>
AIRPORT_PCI_REQ_L  12A7< 12D7<> 24D6<> 39D4>
AIRPORT_PME_L_TP  24D5<>
AMP_CONTROL       25C5<> 25D5<>
ATI_AGP_FBSKEW<0>  19C2< 19C7<>
ATI_AGP_FBSKEW<1>  19C2< 19C7<>
ATI_BUS_CFG<0>    19B2< 19C7<>
ATI_BUS_CFG<1>    19B2< 19C7<>
ATI_BUS_CFG<2>    19B2< 19C7<>
ATI_CLK27M_IN     18C1< 19B7<
ATI_CLK27M_OSC    18D2<
ATI_CLK27M_OSC_SS  18B2< 18D1<
ATI_DBI_HI_PU     18C6<>
ATI_DBI_LO_PU     18C6<>
ATI_GPIO7_SPN     19C7<>
ATI_GPIO8_PD      19C7<>
ATI_GPIO9_SPN     19C7<>
ATI_GPIO10_SPN    19C7<>
ATI_GPIO11_SPN    19C7<>
ATI_GPIO12_SPN    19C7<>
ATI_GPIO13_SPN    19C7<>
ATI_HSYNC         19D5<> 22C8<
ATI_MEMTEST       18A6<>
ATI_MEMVMODE0     18A7<
ATI_MEMVMODE1     18A7<
ATI_OSC_OE        18D3<
ATI_PVDD_BYP      21D6<>
ATI_R2SET         19D6<>
ATI_RSET          19D6<>
ATI_RSTB_MSK      18C6<>
ATI_SSCLK_IN      18B1< 19B7<>
ATI_SSCLK_UF      18B1<>
ATI_TESTEN        19B7<
ATI_TMDS_CLKN     19B7> 20B4<
ATI_TMDS_CLKP     19B7> 20B4<
ATI_TMDS_DN<0>    19B7> 20B4<
ATI_TMDS_DN<1>    19B7> 20A4<
ATI_TMDS_DN<2>    19B7> 20A4<
ATI_TMDS_DP<0>    19B7> 20B4<
ATI_TMDS_DP<1>    19B7> 20A4<
ATI_TMDS_DP<2>    19B7> 20A4<
ATI_TPVDD_BYP     21D1<>
ATI_VSYNC         19D5<> 22C8<
ATI_X1CLK_SKEW<0>  19C2< 19C7<>
ATI_X1CLK_SKEW<1>  19B2< 19C7<>
BATTV_HIGH        31B7<>
BATTV_LOW         31B8<>
BATT_14PBUS_EN    31C1<>
BATT_14V_GATE     31C1<>
BATT_24PBUS_EN    31C2<>
BATT_24V_GATE     31C1<>
BATT_CLK          31A4<> 39C3>
BATT_DATA         31A4<> 39C3>
BATT_DIV          31A5<
BATT_LOW          31A6<>
BATT_LOW_L        31B6<>
BATT_NEG          31A4<> 38C6> 39C3>
BBANG_HRESET_L    23A4< 23C4<> 39C1>
BBANG_JTAG_TCK    23B3< 23C4<>
BBANG_TCK_EN      23B3<
BCKFD_PROT_EN_L   31C6<>
BCKFD_PROT_GATE   31D6<>
BRIGHT_PWM        22A1<> 39A7>
BRIGHT_PWM_UF     22A2<>
BT_USB_DM         14B1< 24B2<> 37B2> 39B6>
BT_USB_DP         14C1< 24B2<> 37B2> 39B6>
CAPSLOCK_LED      23A8<
CAPSLOCK_LED_L    23B8< 30C7<
CBUS_ADDR<0>      17B1<> 17B4>
CBUS_ADDR<1>      17B1<> 17B4>
CBUS_ADDR<2>      17B1<> 17B4>
CBUS_ADDR<3>      17B1<> 17B4>
CBUS_ADDR<4>      17B1<> 17B4>
CBUS_ADDR<5>      17B1<> 17B4>
CBUS_ADDR<6>      17B1<> 17B4>
CBUS_ADDR<7>      17B1<> 17B4>
CBUS_ADDR<8>      17B1<> 17B4>
CBUS_ADDR<9>      17B1<> 17B4>
CBUS_ADDR<10>     17B4> 17C1<>
CBUS_ADDR<11>     17B1<> 17B4>
CBUS_ADDR<12>     17B1<> 17B4>
CBUS_ADDR<13>     17B1<> 17B4>
CBUS_ADDR<14>     17B1<> 17B4>
CBUS_ADDR<15>     17B1<> 17B4>
CBUS_ADDR<16>     17B1<> 17B4<
CBUS_ADDR<17>     17B2<> 17B4>
CBUS_ADDR<18>     17B2<> 17B4>
CBUS_ADDR<19>     17B2<> 17B4>
CBUS_ADDR<20>     17B2<> 17B4>
CBUS_ADDR<21>     17B2<> 17B4>
CBUS_ADDR<22>     17A4> 17B2<>
CBUS_ADDR<23>     17A4> 17B2<>
CBUS_ADDR<24>     17A4> 17B2<>
CBUS_ADDR<25>     17A4> 17B2<>
CBUS_ADDR_16_UF   17B5<>
CBUS_BVD1_L       17B2<> 17C4<
CBUS_BVD2_L       17B2<> 17C4<
CBUS_CE1_L        17C1<> 17C4>
CBUS_CE2_L        17B4> 17C2<>
CBUS_DATA<0>      17A1<> 17A4<>
CBUS_DATA<1>      17A1<> 17A4<>
CBUS_DATA<2>      17A1<> 17A4<>
CBUS_DATA<3>      17A4<> 17C1<>
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CBUS_DATA<7>      17A4<> 17C1<>
CBUS_DATA<8>      17A2<> 17A4<>
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CBUS_DATA<11>     17A4<> 17C2<>
CBUS_DATA<12>     17A4<> 17C2<>
CBUS_DATA<13>     17A4<> 17C2<>
CBUS_DATA<14>     17A4<> 17C2<>
CBUS_DATA<15>     17A4<> 17C2<>
CBUS_DET_1_L      17C2<> 17C4< 39B8>
CBUS_DET_2_L      17A2<> 17C4< 39B8>
CBUS_INPACK_L     17B2<> 17B4<
CBUS_INT_L        14B5<> 14B7< 17A7<>
CBUS_IORD_L       17B2<> 17C4>
CBUS_IOWR_L       17B2<> 17C4>
CBUS_MFUNC1_PD    17A7<> 17A7<
CBUS_MFUNC2_PD    17A7<> 17A7<
CBUS_MFUNC3_PD    17A7<> 17A7<
CBUS_MFUNC4_PD    17A7<> 17A7<
CBUS_MFUNC5_PD    17A7<> 17A7<
CBUS_MFUNC6_PD    17A7< 17A7<>
CBUS_OE_L         17C1<> 17C4>
CBUS_PCI_GNT_L    12D7<> 17A7<
CBUS_PCI_IDSEL    17B7<
CBUS_PCI_PERR_L   17B7<> 17D7<
CBUS_PCI_REQ_L    12A7< 12D7<> 17A7>
CBUS_PCI_RESET_L  17A7<
CBUS_PCI_SERR_L   17B7> 17D7<
CBUS_READY        17B1<> 17C4<
CBUS_REG_L        17B2<> 17C4>
CBUS_RESET_L      17B2<> 17C4>
CBUS_SUSPEND_PU   17A7< 17D7<
CBUS_VCCD0_L      17C4<>
CBUS_VCCD1_L      17C4<>
CBUS_VPPD0        17C4<>
CBUS_VPPD1        17C5<>
CBUS_VS1          17B2<> 17C4<>
CBUS_VS2          17B2<> 17C4<>
CBUS_WAIT_L       17B2<> 17B4<
CBUS_WE_L         17B1<> 17C4>
CBUS_WP_L         17A1<> 17B4<
CG_ADDRSEL        14B7<
CG_CLKOUT         14B6<>
CG_FSEL           14B7< 14C5<
CG_LOCK           14B7<>
CG_RESET_L        14B7<

CG_SYSCLK_EN      14A6< 14B7<
CHARGE_DISABLE    31A7<>
CHARGE_LED_L      30C6<> 30D7< 31D8<> 39D2>
CHGND1            38A6>
CHGND2            38A6>
CHGND3            38A6>
CHGND4            38A6> 39B6>
CHGND5            38A6>
CHGND6            38A6>
CLK10M_PMU_XIN    30B6<
CLK10M_PMU_XOUT   30B6<
CLK10M_PMU_XOUT_UF  30B7<
CLK18M_INT_EXT    14A6<> 36B1>
CLK18M_INT_XIN    14A5< 36B1>
CLK18M_INT_XOUT   14A5<> 36B1>
CLK18M_XTAL_IN    14A5< 36B1>
CLK25M_ENET_XIN   27A7< 36B1>
CLK25M_ENET_XOUT  27A7<> 36B1>
CLK25M_XTAL_IN    27A7<
CLK27M_GPU_XIN    36B1>
CLK27M_GPU_XOUT   36B1>
CLK27M_XTAL_IN    36B1>
CLK32K_PMU_XIN    30B3<>
CLK32K_PMU_XOUT   30B3<>
CLK32K_PMU_XOUT_UF  30B2<>
CLK33M_AIRPORT    12D8< 24D5<> 36C1> 39B1>
CLK33M_AIRPORT_UF  12C7<> 36C1>
CLK33M_CBUS       12D8< 17A7<> 36C1>
CLK33M_CBUS_UF    12C7<> 36C1>
CLK33M_USB2       12C8< 26B7<> 36C1>
CLK33M_USB2_UF    12C7<> 36C1>
CLK66M_AGP_15V_TP  12C4<
CLK66M_GPU_AGP    12C8< 18B7<> 36C1>
CLK66M_GPU_AGP_UF  12C7<> 36C1>
CLKENET_LINK_GBE_REF  13C5< 27C8< 36B1>
CLKENET_LINK_GTX  13C5<> 36A1>
CLKENET_LINK_RX   13D5< 27C8<> 36A1>
CLKENET_LINK_TX   13D5< 27D8<> 36A1>
CLKENET_PHY_GBE_REF  27C7<> 36B1>
CLKENET_PHY_GTX   13C6< 27C7<> 36A1>
CLKENET_PHY_RX    27C7<> 36B1>
CLKENET_PHY_TX    27D7<> 36B1>
CLKFW_LINK_LCLK   13C3<> 36A1>
CLKFW_LINK_PCLK   13C3<> 28C3<> 36A1>
CLKFW_PHY_LCLK    13C2< 28B8< 36A1>
CLKFW_PHY_PCLK    28B4<> 28C3< 36A1>
CLKLVDS_LN        19B5> 22A4<> 37C2> 39B7>
CLKLVDS_LP        19B5> 22A4<> 37C2> 39B7>
CLKLVDS_UN        19B5> 22A4<> 37C2> 39B7>
CLKLVDS_UP        19B5> 22A4<> 37C2> 39A7>
COMM_DTR_L        14C2> 25D1<> 39B2>
COMM_GPIO_L       14C2<> 25D2<> 39C2>
COMM_RESET_L      14C5<> 25C4<> 39C4>
COMM_RING_DET_L   14B5<> 14C7< 25C3<> 30C6<> 39C4>
COMM_RTS_L        14C2> 25D1<> 39B2>
COMM_RXD          14C2<> 25D2<> 39B2>
COMM_SHUTDOWN     14C5<> 25C4<> 39C4>
COMM_TRXC         14C2<> 25D2<> 39C2>
COMM_TXD_L        14C2<> 25D2<> 39C2>
COMP_DISABLE      22C2<>
COMP_ENABLE       22C1<>
COMP_RC           32C6<
CPU_AACK_L        5A7< 8B6<> 8C2< 36D5>
CPU_ADDR<0>       5C7<> 8D6<>
CPU_ADDR<0..31>   36D5>
CPU_ADDR<1>       5C7<> 8D6<>
CPU_ADDR<2>       5C7<> 8D6<>
CPU_ADDR<3>       5C7<> 8D6<>
CPU_ADDR<4>       5C7<> 8D6<>
CPU_ADDR<5>       5C7<> 8C6<>
CPU_ADDR<6>       5C7<> 8C6<>
CPU_ADDR<7>       5C7<> 8C6<>
CPU_ADDR<8>       5C7<> 8C6<>
CPU_ADDR<9>       5C7<> 8C6<>
CPU_ADDR<10>      5B7<> 8C6<>
CPU_ADDR<11>      5B7<> 8C6<>
CPU_ADDR<12>      5B7<> 8C6<>
CPU_ADDR<13>      5B7<> 8C6<>
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CPU_ADDR<15>      5B7<> 8C6<>
CPU_ADDR<16>      5B7<> 8C6<>
CPU_ADDR<17>      5B7<> 8C6<>
CPU_ADDR<18>      5B7<> 8C6<>
CPU_ADDR<19>      5B7<> 8C6<>
CPU_ADDR<20>      5B7<> 8C6<>
CPU_ADDR<21>      5B7<> 8C6<>
CPU_ADDR<22>      5B7<> 8C6<>
CPU_ADDR<23>      5B7<> 8C6<>
CPU_ADDR<24>      5B7<> 8C6<>
CPU_ADDR<25>      5B7<> 8C6<>
CPU_ADDR<26>      5B7<> 8C6<>
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CPU_ADDR<28>      5B7<> 8C6<>
CPU_ADDR<29>      5B7<> 8C6<>
CPU_ADDR<30>      5B7<> 8C6<>
CPU_ADDR<31>      5B7<> 8B6<>
CPU_ARTRY_L       5A7<> 8B6<> 8D2< 36D5>
CPU_AVDD          5C3< 38D3>
CPU_AVDD_ADJ      5C2<>
CPU_AVDD_PG       5C3<>
CPU_AVDD_VIN      5C3<
CPU_AVDD_VOUT     5C3<>
CPU_BG_L          5C7< 8C2< 8D6<> 36D5>
CPU_BR_L          5C7> 8D2< 8D6< 36D5>
CPU_BUS_VSEL      5C4< 7A6<
CPU_CHKSTP_OUT_L  5B4<> 5C2< 39D8>
CPU_CHKS_L        5A4< 5D2<
CPU_CI_L          5A7< 8B6<> 36D5>
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CPU_DATA<0..31>   36D5>
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CPU_DATA<4>       6D8<> 8D4<>
CPU_DATA<5>       6D8<> 8D4<>
CPU_DATA<6>       6D8<> 8D4<>
CPU_DATA<7>       6D8<> 8D4<>
CPU_DATA<8>       6D8<> 8D4<>
CPU_DATA<9>       6D8<> 8D4<>
CPU_DATA<10>      6C8<> 8D4<>
CPU_DATA<11>      6C8<> 8D4<>
CPU_DATA<12>      6C8<> 8C4<>
CPU_DATA<13>      6C8<> 8C4<>
CPU_DATA<14>      6C8<> 8C4<>
CPU_DATA<15>      6C8<> 8C4<>
CPU_DATA<16>      6C8<> 8C4<>
CPU_DATA<17>      6C8<> 8C4<>
CPU_DATA<18>      6C8<> 8C4<>
CPU_DATA<19>      6C8<> 8C4<>
CPU_DATA<20>      6C8<> 8C4<>
CPU_DATA<21>      6C8<> 8C4<>
CPU_DATA<22>      6C8<> 8C4<>
CPU_DATA<23>      6C8<> 8C4<>
CPU_DATA<24>      6C8<> 8C4<>
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CPU_DATA<26>      6C8<> 8C4<>
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CPU_DATA<28>      6C8<> 8C4<>
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CPU_DATA<32>      6C8<> 8C4<> 8D8<
CPU_DATA<32..63>  36D5>
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CPU_DATA<34>      6C8<> 8C4<> 8D8<
CPU_DATA<35>      6C8<> 8C4<> 8D8<
CPU_DATA<36>      6B8<> 8C4<> 8D8<
CPU_DATA<37>      6B8<> 8C4<> 8D8<
CPU_DATA<38>      6B8<> 8B4<> 8D8<
CPU_DATA<39>      6B8<> 8B4<> 8D8<
CPU_DATA<40>      6B8<> 8B4<> 8C8<
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CPU_DATA<42>      6B8<> 8B4<> 8C8<
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CPU_DATA<44>      6B8<> 8B4<> 8C8<
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CPU_DATA<49>      6B8<> 8A8< 8B4<>
CPU_DATA<50>      6B8<> 8A8< 8B4<>
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CPU_DATA<55>      6B8<> 8A8< 8B4<>

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CPU_DATA<58>      6B8<> 8B3< 8B4<>
CPU_DATA<59>      6B8<> 8B3< 8B4<>
CPU_DATA<60>      6B8<> 8B3< 8B4<>
CPU_DATA<61>      6B8<> 8B3< 8B4<>
CPU_DATA<62>      6A8<> 8B3< 8B4<>
CPU_DATA<63>      6A8<> 8B3< 8B4<>
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CPU_DRDY_L        5C4> 8A4< 8C2< 36D5>
CPU_DRDY_L_UF     36D5>
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CPU_DTI<0..2>     36D5>
CPU_DTI<1>        5C4< 8A4<>
CPU_DTI<2>        5C4< 8A4<>
CPU_EDTI          5B2< 5C4<
CPU_EMODE0_L      5A4< 7A4<
CPU_EMODE1_L      5A4< 5C2<
CPU_GBL_L         5A7<> 8B6<> 36D5>
CPU_HIT_L         5A7> 8B6< 8D2< 36D5>
CPU_HRESET_INV    7A7<>
CPU_HRESET_L      5B4< 5C2< 7A5< 7A8< 23A2<> 39C8>
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CPU_L2TSTCLK      5B4< 5C2<
CPU_LSSD_MODE     5B4< 5C2<
CPU_MCP_L         5B4< 5D2<
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CPU_M_DP          25B6< 25B8<
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CPU_PLL_CFG<2>    5C4< 7D3<
CPU_PLL_CFG<3>    5C4< 7D3<
CPU_PLL_CFG<4>    5C4< 7D3<>
CPU_PLL_CFGEXT    7D4<>
CPU_PLL_FS00      7C4<>
CPU_PLL_FS01      7C4<
CPU_PLL_FS10      7C4<
CPU_PLL_STOP_BASE  7C7<
CPU_PLL_STOP_OC   7C4<> 7C8<> 30B6<>
CPU_PMONIN_L      5A4< 5C2<
CPU_PULLDOWN      5A2< 5A4< 5A4< 5C7<>
CPU_PULLUP        5A4< 5A4< 5C2<
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CPU_QREQ_L        5B4> 8B6< 8C2< 36D5>
CPU_SHD0_L        5A7<> 5D2<
CPU_SHD1_L        5A7<> 5D2<
CPU_SMI_L         5B4< 5C2< 30C4<>
CPU_SRESET_L      5B2< 5B4< 39C8>
CPU_SRWX_L        5A4< 5C2<
CPU_TA_L          5B4< 8A4<> 8D2< 36D5>
CPU_TBEN          5B4< 5D2< 8A6<>
CPU_TBST_L        5A7> 8B6<> 36D5>
CPU_TEA_L         5B4< 8A4<> 8C2< 36D5>
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CPU_THERM_DP      6A6<> 25A6<
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CPU_TSIZ<0..2>    36D5>
CPU_TSIZ<1>       5A7> 8B6<>
CPU_TSIZ<2>       5A7> 8B6<>
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CPU_TT<0..4>      36C5>
CPU_TT<1>         5A7<> 8B6<>
CPU_TT<2>         5A7<> 8B6<>
CPU_TT<3>         5A7<> 8B6<>
CPU_TT<4>         5A7<> 8B6<>
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CPU_VCORE_SEQ     34D8<
CPU_VCORE_SEQ_L   34D8<
CPU_VCORE_SLEEP   5C3<> 5D8<> 6C6<> 34C1< 34D2< 38D3>
                  39B2>
CPU_VCORE_SLEEP_F  34C2<>
CPU_VCORE_SNUB    34B3<
CPU_WT_L          5A7> 8B6<> 36C5>
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CSLOT_ADDR4_SPN   13B7>
CSLOT_ADDR5_SPN   13B7>
CSLOT_ADDR6_SPN   13B7>
CSLOT_ADDR7_SPN   13B7>
CSLOT_ADDR8_SPN   13B7>
CSLOT_ADDR9_SPN   13B7>
CSLOT_CE1_L_SPN   13C7>
CSLOT_CE2_L_SPN   13C7>
CSLOT_IORD_L_SPN  13C7>
CSLOT_IOWAIT_L_PU  13C7<
CSLOT_IOWR_L_SPN  13C7>
CSLOT_OE_L_SPN    13C7>
CSLOT_WE_L_SPN    13C7>
CURRENT_THRESHOLD  31C4<
CY25811_S0        18B2<
CY25811_S1        18B2<
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DCDC_EN_L         33B6< 33B7<> 35C7<>
DDC_CLK_ISO       22D4<>
DDR_VREF          11D1< 11D3<> 11D5<> 11D6<> 11D8<>
                  38D3>
DVI_DDC_CLK       22D4<>
DVI_DDC_CLK_UF    22C5<> 22D3<> 39C7>
DVI_DDC_DATA      22C4<>
DVI_DDC_DATA_UF   22C5<> 39C7>
DVI_HPD           22C4<>
DVI_HPD_DIV       22C3<
DVI_HPD_UF        22C3< 22C5<> 39C7>
DVI_TRUN_ON_ILIM  22D2<
DVI_TURN_ON       22D3<>
DVI_TURN_ON_BASE  22D2<
EEPROM_ADDR       23D4<
EEPROM_WP_PD      23D3<>
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EIDE_ADDR<2>      13B7> 24B8<
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EIDE_CS1_L        13B7> 24B8< 37B5>
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EIDE_DATA<15..0>  37B5>
EIDE_DATA<1>      13C7<> 24C8<
EIDE_DATA<2>      13C7<> 24C8<
EIDE_DATA<3>      13C7<> 24C8<
EIDE_DATA<4>      13C7<> 24C8<
EIDE_DATA<5>      13B7<> 24B8<
EIDE_DATA<6>      13B7<> 24C8<
EIDE_DATA<7>      13B7<> 24C8<
EIDE_DATA<8>      13B7<> 24D8<
EIDE_DATA<9>      13B7<> 24D8<
EIDE_DATA<10>     13B7<> 24D8<
EIDE_DATA<11>     13B7<> 24D8<
EIDE_DATA<12>     13B7<> 24D8<
EIDE_DATA<13>     13B7<> 24C8<
EIDE_DATA<14>     13B7<> 24C8<
EIDE_DATA<15>     13B7<> 24C8<
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EIDE_IOCHRDY      13B7< 24A8< 37B5>
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EIDE_OPTICAL_ADDR<2..0>  37B5>
EIDE_OPTICAL_ADDR<1>  24A5<> 24B7< 39A4>
EIDE_OPTICAL_ADDR<2>  24A6<> 24B7< 39A4>
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EIDE_OPTICAL_CS1_L  24A6<> 24B7< 37B5> 39D4>
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EIDE_OPTICAL_DATA<15..0>  37B5>
EIDE_OPTICAL_DATA<1>  24A5<> 24C7< 39C4>
EIDE_OPTICAL_DATA<2>  24A5<> 24C7< 39C4>
EIDE_OPTICAL_DATA<3>  24A5<> 24C7< 39C4>
EIDE_OPTICAL_DATA<4>  24A5<> 24C7< 39C4>
EIDE_OPTICAL_DATA<5>  24A5<> 24B7< 39C4>
EIDE_OPTICAL_DATA<6>  24A5<> 24C7< 39C4>
EIDE_OPTICAL_DATA<7>  24A5<> 24C7< 39B4>
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EIDE_OPTICAL_DATA<14>  24A6<> 24C7< 39B4>
EIDE_OPTICAL_DATA<15>  24A6<> 24C7< 39B4>
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EIDE_OPTICAL_DMA_RQ  24A6<> 24B7< 37A5> 39A4>
EIDE_OPTICAL_INT  24A5<> 24A7< 37A5> 39D4>
EIDE_OPTICAL_IOCHRDY  24A5<> 24A7< 37A5> 39D4>
EIDE_OPTICAL_RD_L  24A6<> 24A7< 37B5> 39A4>
EIDE_OPTICAL_RST_L  24A7< 24B5<> 37A5> 39D4>
EIDE_OPTICAL_WR_L  24A5<> 24A7< 37A5> 39D4>
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EIDE_RST_L        13B7> 24A8< 37B5>

EIDE_WR_L         13A7> 24A8< 37B5>
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ENET_COMA         27B7<>
ENET_CRS          13C5< 27B7> 37A5>
ENET_CTAP_CHGND   27A1< 38A6>
ENET_ENERGY_DET   14B5<> 27B7<>
ENET_HSDACM       27A7<>
ENET_HSDACP       27A7<>
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ENET_LINK_RXD<7..0>  37A5>
ENET_LINK_RXD<1>  13C5< 27C7>
ENET_LINK_RXD<2>  13C5< 27C7>
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ENET_LINK_RXD<7>  13C5< 27B7>
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ENET_LINK_TXD<7..0>  37A5>
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ENET_LINK_TXD<2>  13B4< 13D5>
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ENET_LINK_TXD<5>  13B4< 13D5>
ENET_LINK_TXD<6>  13A4< 13D5>
ENET_LINK_TXD<7>  13A4< 13D5>
ENET_LINK_TX_EN   13D5<> 37A5>
ENET_LINK_TX_ER   13D5<> 37A5>
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ENET_MDIO         13C5<> 27B7<> 37A5>
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ENET_PHY_TXD<7..0>  37A5>
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ENET_PHY_TXD<3>   13B5> 27C7<
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ENET_PHY_TXD<6>   13A5> 27C7<
ENET_PHY_TXD<7>   13A5> 27C7<
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ENET_PHY_TX_ER    13D6> 27C7< 37A5>
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ENET_RST_L        27B7<
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ENET_RX_ER        13C5< 27B7> 37A5>
ENET_VSSC         27A7<>
EXT_SWING         20A5<>
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FANL_PWM          25A3<> 25B2<> 39B3>
FANL_TACH         25A3<> 25B2< 39B3>
FANR_GND          25B2<> 38B6> 39B3>
FANR_PWM          25A2<> 25B1<> 39B3>
FANR_TACH         25B2<> 25B2<
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FP_PWR_EN_L       22B3<>
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FWB_TPB1          28A4<
FWPLL_BYP         28C8<>
FW_BIAS0          28A5<>
FW_BIAS1          28A5<>
FW_BMODE          28B7<
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FW_LINK_CNTL<1..0>  37A5>
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FW_LINK_DATA<7..0>  37A5>
FW_LINK_DATA<1>   13D3<> 28B8<
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FW_LINK_DATA<7>   13C3<> 28A8<
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FW_LKON           13C3<> 28B5<>
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FW_PC_PU          28B7<
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FW_PHY_CNTL<1..0>  37A5>
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FW_PHY_DATA<3>    28A8<>
FW_PHY_DATA<4>    28A8<>
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FW_PHY_DATA<7>    28A8<>
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FW_PHY_LREQ       13C2< 28B8< 37A5>
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FW_PHY_PD_INT     14A7< 14C5<>
FW_PHY_RESET_L    28A8<
FW_PINT           13C3<> 28B4> 37A5>
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FW_PORT1_SEL      28B6<
FW_PWREN_L        29C6<>
FW_PWR_GATE       29D6<>
FW_R0             28A5<>
FW_R1             28A5<>
FW_TESTM          28A7<
FW_TPA0N          28B1<> 29C4<> 37D2>
FW_TPA0N_CONN     29C3<>
FW_TPA0P          28B1<> 29C4<> 37D2>
FW_TPA0P_CONN     29C3<>
FW_TPA1N          28B1<> 29A4<> 37C2>
FW_TPA1P          28B1<> 29A4<> 37C2>
FW_TPB0N          28B1<> 29C4<> 37D2>
FW_TPB0N_CONN     29C3<>
FW_TPB0P          28B1<> 29C4<> 37D2>
FW_TPB0P_CONN     29C3<>
FW_TPB1N          28B1<> 29A4<> 37C2>
FW_TPB1P          28B1<> 29A4<> 37C2>
FW_TPB2_PD        28A5<>
FW_TPI0N          37C2>
FW_TPI0P          37C2>
FW_TPI1N          29A3<> 37C2> 39D2>
FW_TPI1P          29A3<> 37C2> 39D2>
FW_TPO0N          37C2>
FW_TPO0P          37C2>
FW_TPO0R          29C2<> 38A3> 39A3>
FW_TPO1N          29A3<> 37C2> 39D2>
FW_TPO1P          29A3<> 37C2> 39D2>
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FW_VGND1          29A3<> 38A3>
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FW_XI             28A5<> 36A1>
GAIN_SETTING2     23C7<>
GPU_AGP_TEST      18D6<
GPU_AUXWIN        19C5<>
GPU_B             19D6<> 22D8<
GPU_C             19D6<> 22A8<
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GPU_CLK27M_UF     36C1>
GPU_COMP          19C6<> 22A8<
GPU_CORE_OK       19A6<> 19D4<> 21D2<> 21D7<>
GPU_DVI_DDC_CLK   19C5<> 22D3<>
GPU_DVI_DDC_DATA  19C5<> 22C3<>
GPU_DVOD<0>       19D7<> 20B7<
GPU_DVOD<0..11>   37D5>
GPU_DVOD<1>       19D7<> 20B7<
GPU_DVOD<2>       19D7<> 20B7<
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GPU_DVOD<4>       19D7<> 20B7<
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GPU_DVOD<6>       19D7<> 20A7<
GPU_DVOD<7>       19D7<> 20A7<
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GPU_DVOD<9>       19D7<> 20A7<
GPU_DVOD<10>      19D7<> 20A7<
GPU_DVOD<11>      19D7<> 20A7<
GPU_DVOD_DE       19C7<> 20A7<
GPU_DVO_CLKP      19C7<> 20A7< 36B1>
GPU_DVO_HSYNC     19C7<> 20A7< 37C5>
GPU_DVO_VSYNC     19C7<> 20A7< 37C5>
GPU_FBCLK0        36B1>
GPU_FBCLK0_L      36B1>
GPU_FBCLK1        36B1>
GPU_FBCLK1_L      36B1>
GPU_G             19D6<> 22D8<

GPU_HPD           19C5< 22C3<>
GPU_MEM_IO        38C3>
GPU_MEM_IO_FLT    21C2< 38C3>
GPU_R             19D6<> 22D8<
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GPU_SSCLK_UF      36C1>
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GPU_THERM_DP_TP   18A6<>
GPU_TV_GND1       22B8<> 38B6>
GPU_TV_GND2       22A8<> 38B6>
GPU_VCORE         18A6<> 19A3<> 19B5<> 19D4<> 38C3>
                  39B2>
GPU_VCORE_CNTL    19A3<>
GPU_VCORE_CNTL_L  19A3< 19B7<>
GPU_VCORE_NECK    19B5<> 38B3>
GPU_VCORE_PWR_SEQ  19A8<>
GPU_VCORE_SEQ     19A8<
GPU_VCORE_SEQ_L   19A8<
GPU_VCORE_SW      19A4<> 38B1>
GPU_VCORE_VDDCI   18A5<> 38C3>
GPU_Y             19D6<> 22B8<
HD_ADDR<0>        24C2<> 24C3<
HD_ADDR<2..0>     37C5>
HD_ADDR<1>        24C2<> 24C3<
HD_ADDR<2>        24B3<> 24C1<>
HD_CS0_L          24C2<> 24C3<> 37B5>
HD_CS1_L          24B3<> 24C1<> 37B5>
HD_DATA<0>        24C2<> 24D3<
HD_DATA<15..0>    37C5>
HD_DATA<1>        24C2<> 24D3<
HD_DATA<2>        24D2<> 24D3<
HD_DATA<3>        24D2<> 24D3<
HD_DATA<4>        24C3< 24D2<>
HD_DATA<5>        24C3< 24D2<>
HD_DATA<6>        24C3< 24D2<>
HD_DATA<7>        24C3< 24D2<>
HD_DATA<8>        24C3< 24D1<>
HD_DATA<9>        24C3< 24D1<>
HD_DATA<10>       24C3< 24D1<>
HD_DATA<11>       24D1<> 24D3<
HD_DATA<12>       24B3< 24D1<>
HD_DATA<13>       24B3< 24D1<>
HD_DATA<14>       24C1<> 24C3<
HD_DATA<15>       24B3< 24C1<>
HD_DIOR_L         24A3< 24C2<> 37B5>
HD_DIOW_L         24A3< 24C1<> 37B5>
HD_DMACK_L        24A3< 24C2<> 37B5>
HD_DMARQ          13C6< 24C2<> 37B5>
HD_INTRQ          13C6< 24C1<> 37B5>
HD_IOCHRDY        24A3< 24C1<> 37B5>
HD_RESET_L        24A3< 24D2<> 37B5>
HIGH_VCORE        19A2<>
HIGH_VCORE_DIV    19A3<
HPD_4V_REF        22C3<
HPD_BASE          22C1<
HPD_ON            22C2<>
HPD_ON_RC         22C2<
HPD_PWR_SNS_EN    19C7<> 22C3<>
HPD_PWR_SW        22C2<>
IAC_FB            31D4<
IAC_RC_COMP       31D4<
INTREPID_ACS_REF  8A6<
INT_AGPPVT        12D4<>
INT_AGP_FB_IN     12C4<> 36C1>
INT_AGP_FB_OUT    12C4<> 36C1>
INT_AGP_VREF      12B4< 12D4<> 18D5< 38D3>
INT_AUDIO_TO_SND  14B2< 25D8<> 39C6>
INT_AUDIO_TO_SND_F  25D7<> 25D7<
INT_CPUFB_IN      8A6< 8B6<> 36D1>
INT_CPUFB_IN_NORM  8A4< 36D1>
INT_CPUFB_LONG    8A4< 36D1>
INT_CPUFB_OUT     8A6< 8A6<> 36D1>
INT_CPUFB_OUT_NORM  8A4< 36D1>
INT_CPUFB_OUT_SHORT  8A5< 36D1>
INT_DDRCLK2_N_TP  9B6<>
INT_DDRCLK2_P_TP  9B6<>
INT_DDRCLK5_N_TP  9B6<>
INT_DDRCLK5_P_TP  9B6<>
INT_ENET_RST_L    14B5<> 27B8<
INT_EXTINT3_PU    14B5<> 14B7<
INT_EXTINT8_PU    14B5<> 14C7<
INT_EXTINT10_PU   14A7< 14B5<>
INT_EXTINT11_PU   14A7< 14B5<>
INT_EXTINT12_PU   14A7< 14B5<>
INT_EXTINT13_PU   14B5<> 14B7<
INT_EXTINT14_PU   14B5<> 14C7<
INT_EXTINT16_PU   14B5<> 14B7<
INT_GPIO0         14C5<>
INT_GPIO1_PU      14C5<> 14C7< 34C8<
INT_GPIO9_PU      14A7< 14B5<>
INT_GPIO12_PU     14B5<> 14B7<
INT_GPIO15_PU     14B5<> 14C7<
INT_I2C_CLK0      11A3<> 11A8<> 13C2< 13C3<> 23D2<
                  23D4<> 39B8>
INT_I2C_CLK1      13C2< 13C3<> 14B7< 25B4<> 39B8>
INT_I2C_CLK2      14A2<> 25C4<> 25D7<> 39C6>
INT_I2C_DATA0     11A3<> 11A8<> 13C2< 13C3<> 23D2<>
                  23D4<> 39B8>
INT_I2C_DATA1     13B2< 13C3<> 14B7< 25B4<> 39B8>
INT_I2C_DATA2     14A2<> 25C4<> 25C7<> 39C6>
INT_JTAG_TEI      13C2< 13C5<
INT_MEM_REF_H     9B6< 38D3>
INT_MEM_VREF      9A7< 9B6<> 38D3>
INT_MOD_BITCLK_UF  14A3<> 14A7<
INT_MOD_CLKOUT_UF  14A3<> 14B7<
INT_MOD_DTI       14A2< 25C3<> 39B1>
INT_MOD_DTI_UF    14A7<
INT_MOD_DTO_UF    14A3<> 14B7<
INT_MOD_SYNC_UF   14A3<> 14A7<
INT_PCI_FB_IN     12C7<> 36C1>
INT_PCI_FB_OUT    12C7<> 36C1>
INT_PEND_PROC_INT  14A5<> 30C4<>
INT_PROC_SLEEP_REQ_L  14A5< 30B4<>
INT_PU_RESET_L    13D3< 25D4<> 30A2< 30C4<>
INT_REF_CLK_IN    14A5< 14B5< 36C1>
INT_REF_CLK_OUT   14A5> 14B7< 36C1>
INT_RESET_L       9B3< 13D3< 30C7< 30D4<>
INT_ROM_CS_L      12A6< 12C7>
INT_ROM_OE_L      12A6< 12C7>
INT_ROM_RW_L      12A6< 12C7>
INT_SND_CLKOUT    14A3<>
INT_SND_SCLK      14A3<>
INT_SND_SYNC      14B3<>
INT_SND_TO_AUDIO  14B3<>
INT_SUSPEND_ACK_L  8B6> 30B6<>
INT_SUSPEND_REQ_L  8B6< 30B6<> 30C7<
INT_TST_MONIN_PD  13C2< 13C5<
INT_TST_MONOUT_TP  13C5>
INT_TST_PLLEN_PD  13C5< 13D2<
INT_WATCHDOG_L    14A5> 30C6<>
INV_ON_PWM        19C6<> 22A3<
IO_RESET_L        17A7< 23D6< 26B8< 27B8< 30C6<>
                  30D7<
JTAG_ASIC_TCK     13C5< 13D2< 27A5< 39D8>
JTAG_ASIC_TDI     27A5< 27D7< 39D8>
JTAG_ASIC_TDO     13C5> 13D2< 14A7< 39D8>
JTAG_ASIC_TMS     13C5< 13D2< 27A5< 39D8>
JTAG_ASIC_TRST_L  13C2< 13C5< 27A5< 39D8>
JTAG_CPU_TCK      5B2< 5B4< 23B2> 39C8>
JTAG_CPU_TDI      5B2< 5C4< 23D4<> 39C8>
JTAG_CPU_TDO_TP   5C4> 39C8>
JTAG_CPU_TMS      5B2< 5B4< 23C4<> 39C8>
JTAG_CPU_TRST_L   5B3< 5B4< 23D4<> 39B1> 39C8>
JTAG_ENET_TDO     13C5< 13D2< 27A5>
KBD_CAPSLOCK_LED  23A7<> 39B4>
KBD_COMMAND_L     23A5< 23A7<> 30A8< 30C6<> 39B4>
KBD_CONTROL_L     23A5< 23A7<> 30A8< 30C6<> 39B4>
KBD_FUNCTION_L    23A5< 23A7<> 30B6<> 39B4>
KBD_ID            23A7<> 23B5< 30B6<> 39C4>
KBD_LED1_OUT      23A5<> 23A7<> 38B6> 39C2>
KBD_LED2_OUT      23A5<> 23A7<> 38B6> 39C2>
KBD_LED_EN        23A5<>
KBD_LED_SET       23A5<
KBD_NUMLOCK_LED   23B7<> 39C3>
KBD_OPTION_L      23A5< 23B7<> 30A8< 30B6<> 39B4>
KBD_SHIFT_L       23A5< 23B7<> 30A8< 30C6<> 39B4>
KBD_X<0>          23A5< 23B7<> 30C6<> 39B4>
KBD_X<1>          23A5< 23B7<> 30C6<> 39B4>
KBD_X<2>          23B5< 23B7<> 30C6<> 39B4>
KBD_X<3>          23B5< 23B7<> 30C6<> 39A4>
KBD_X<4>          23B5< 23B7<> 30C6<> 39A4>
KBD_X<5>          23B5< 23B7<> 30C6<> 39A4>
KBD_X<6>          23B5< 23B7<> 30C6<> 39A4>
KBD_X<7>          23B5< 23B7<> 30C6<> 39A4>
KBD_X<8>          23B5< 23B7<> 30C6<> 39A4>
KBD_X<9>          23B5< 23B7<> 30C6<> 39D3>
KBD_Y<0>          23B7<> 30D6<> 39D3>
KBD_Y<1>          23B7<> 30D6<> 39D3>

KBD_Y<2>          23B7<> 30D6<> 39D3>
KBD_Y<3>          23B7<> 30D6<> 39D3>
KBD_Y<4>          23B7<> 30D6<> 39D3>
KBD_Y<5>          23B7<> 30D6<> 39D3>
KBD_Y<6>          23B7<> 30C6<> 39C3>
KBD_Y<7>          23B7<> 30C6<> 39C3>
LCD_DIGON_L       22A6<
LCD_PWREN_L       22A5<>
LED_LINK10        27B5<>
LED_LINK100       27B5<>
LED_RX_SPN        27B5>
LEFT_USB_DM       24B2<> 26B3< 37A2> 39D1>
LEFT_USB_DP       24B2<> 26A3< 37A2> 39D1>
LID_CLOSED_L      23A7<> 39C4>
LM2594_IN         28D8<> 38B3>
LT1962_INT_ADJ    14D6<
LT1962_INT_BYP    14D6<>
LTC1625_ITH       31D3<>
LTC1962_1V5_VIN   38A1>
LTC1962_1V5_VOUT  38A1>
LTC1962_INT_VIN   14D7<> 38A1>
LTC1962_L3_VIN    38A1>
LTC1962_L3_VOUT   38A1>
LTC3405_SW        27D4<> 38B3>
LTC3411_GND       38A1>
LTC3411_ITH       38A1>
LTC3411_ITH_RC    38A1>
LTC3411_SHDN      38A1>
LTC3411_SYNC      38A1>
LTC3411_VCC       38B1>
LTC3412_GND       35A6<>
LTC3412_ITH       35A6<>
LTC3412_ITH_RC    35A6<
LTC3412_PGOOD     35A4<>
LTC3412_RT        35A6<
LTC3412_RUNSS     35A6<>
LTC3412_SYNC      35A6<>
LTC3412_VFB       35A6<>
LTC3412_VFB_DIV   35A6<
LTC3707_START_RC  33B6<>
LVDS_DDC_CLK      19C5<> 22B5<> 39A7>
LVDS_DDC_DATA     19C5<> 22B5<> 39A7>
LVDS_L0N          19B5> 22B4<> 37C2> 39C7>
LVDS_L0P          19B5> 22B4<> 37C2> 39C7>
LVDS_L1N          19B5> 22B4<> 37C2> 39C7>
LVDS_L1P          19B5> 22B4<> 37C2> 39C7>
LVDS_L2N          19B5> 22B4<> 37C2> 39C7>
LVDS_L2P          19B5> 22B4<> 37C2> 39C7>
LVDS_L3N_TP       19B5>
LVDS_L3P_TP       19B5>
LVDS_U0N          19C5> 22A4<> 37C2> 39B7>
LVDS_U0P          19C5> 22A4<> 37C2> 39B7>
LVDS_U1N          19C5> 22A4<> 37C2> 39B7>
LVDS_U1P          19C5> 22A4<> 37C2> 39B7>
LVDS_U2N          19B5> 22A4<> 37B2> 39B7>
LVDS_U2P          19B5> 22A4<> 37B2> 39B7>
LVDS_U3N_TP       19B5>
LVDS_U3P_TP       19B5>
MAIN_RESET_L      14C7< 17A7< 17D5< 18C8< 20B8<
                  24D6<> 26B8< 30D4<> 30D7< 39C1>
MAX1715_FB2       35B1< 35B4<
MAX1715_GND       35B5<> 35C5< 38C1>
MAX1715_ON_RC     35C7<>
MAX1715_REF       35B5<> 38C1>
MAX1715_SKIP      35C4<> 38C1>
MAX1715_TON       35C5< 38C1>
MAX1715_VCC       35D5<> 38C1>
MAX1717_AB_SEL    34A7< 34C6<
MAX4172_OUT       31D4<>
MAX8860_CC        21A6<>
MAX8860_FAULT     21A6<>
MAXBUS_SLEEP      5B2< 5D1< 5D5< 7B7< 7D8< 8B8< 8C3<
                  8C8< 8D1< 8D8< 15D8< 16D8< 23B3<
                  23B3< 34D8< 38D3>
MDI0_PD           27B4<
MDI1_PD           27B4<
MDI2_PD           27B4<
MDI3_PD           27B3<
MDI_M<0>          27B5<> 37D2>
MDI_M<1>          27B5<> 37D2>
MDI_M<2>          27B5<> 37D2>
MDI_M<3>          27B5<> 37D2>
MDI_P<0>          27B5<> 37D2>
MDI_P<1>          27B5<> 37D2>
MDI_P<2>          27B5<> 37D2>
MDI_P<3>          27B5<> 37D2>
MEM_ADDR<0>       9B5< 9D6<>
MEM_ADDR<12..0>   36A5>
MEM_ADDR<1>       9B5< 9D6<>
MEM_ADDR<2>       9B5< 9D6<>
MEM_ADDR<3>       9B5< 9D6<>
MEM_ADDR<4>       9B5< 9D6<>
MEM_ADDR<5>       9B5< 9D6<>
MEM_ADDR<6>       9B5< 9D6<>
MEM_ADDR<7>       9B5< 9D6<>
MEM_ADDR<8>       9B5< 9D6<>
MEM_ADDR<9>       9A5< 9D6<>
MEM_ADDR<10>      9A5< 9D6<>
MEM_ADDR<11>      9A5< 9D6<>
MEM_ADDR<12>      9A5< 9D6<>
MEM_BA<0>         9A5< 9D6<>
MEM_BA<1..0>      36A5>
MEM_BA<1>         9A5< 9C6<>
MEM_CAS_L         9A5< 9C6<> 36A5>
MEM_CKE<0>        9B6<> 9C5<
MEM_CKE<3..0>     36A5>
MEM_CKE<1>        9B6<> 9C5<
MEM_CKE<2>        9B6<> 9C5<
MEM_CKE<3>        9B6<> 9C5<
MEM_CS_L<0>       9C5< 9C6<>
MEM_CS_L<3..0>    36A5>
MEM_CS_L<1>       9C5< 9C6<>
MEM_CS_L<2>       9C5< 9C6<>
MEM_CS_L<3>       9C5< 9C6<>
MEM_DATA<0>       9D8<> 10C7<>
MEM_DATA<7..0>    36C5>
MEM_DATA<1>       9D8<> 10C7<>
MEM_DATA<2>       9D8<> 10C7<>
MEM_DATA<3>       9D8<> 10C7<>
MEM_DATA<4>       9D8<> 10C7<>
MEM_DATA<5>       9D8<> 10C7<>
MEM_DATA<6>       9D8<> 10C7<>
MEM_DATA<7>       9D8<> 10C7<>
MEM_DATA<8>       9D8<> 10C7<>
MEM_DATA<15..8>   36C5>
MEM_DATA<9>       9D8<> 10C7<>
MEM_DATA<10>      9D8<> 10C7<>
MEM_DATA<11>      9D8<> 10C7<>
MEM_DATA<12>      9D8<> 10B7<>
MEM_DATA<13>      9C8<> 10B7<>
MEM_DATA<14>      9C8<> 10B7<>
MEM_DATA<15>      9C8<> 10B7<>
MEM_DATA<16>      9C8<> 10C5<>
MEM_DATA<31..16>  36C5>
MEM_DATA<17>      9C8<> 10C5<>
MEM_DATA<18>      9C8<> 10C5<>
MEM_DATA<19>      9C8<> 10C5<>
MEM_DATA<20>      9C8<> 10C5<>
MEM_DATA<21>      9C8<> 10C5<>
MEM_DATA<22>      9C8<> 10C5<>
MEM_DATA<23>      9C8<> 10C5<>
MEM_DATA<24>      9C8<> 10C5<>
MEM_DATA<25>      9C8<> 10C5<>
MEM_DATA<26>      9C8<> 10C5<>
MEM_DATA<27>      9C8<> 10C5<>
MEM_DATA<28>      9C8<> 10C5<>
MEM_DATA<29>      9C8<> 10B5<>
MEM_DATA<30>      9C8<> 10B5<>
MEM_DATA<31>      9C8<> 10B5<>
MEM_DATA<32>      9C8<> 10C3<>
MEM_DATA<47..32>  36B5>
MEM_DATA<33>      9C8<> 10C3<>
MEM_DATA<34>      9C8<> 10C3<>
MEM_DATA<35>      9C8<> 10C3<>
MEM_DATA<36>      9C8<> 10C3<>
MEM_DATA<37>      9C8<> 10C3<>
MEM_DATA<38>      9C8<> 10C3<>
MEM_DATA<39>      9B8<> 10C3<>
MEM_DATA<40>      9B8<> 10C3<>
MEM_DATA<41>      9B8<> 10C3<>
MEM_DATA<42>      9B8<> 10C3<>
MEM_DATA<43>      9B8<> 10C3<>
MEM_DATA<44>      9B8<> 10C3<>
MEM_DATA<45>      9B8<> 10B3<>
MEM_DATA<46>      9B8<> 10B3<>
MEM_DATA<47>      9B8<> 10B3<>
MEM_DATA<48>      9B8<> 10C1<>
MEM_DATA<55..48>  36B5>

MEM_DATA<49>      9B8<> 10C1<>
MEM_DATA<50>      9B8<> 10C1<>
MEM_DATA<51>      9B8<> 10C1<>
MEM_DATA<52>      9B8<> 10C1<>
MEM_DATA<53>      9B8<> 10C1<>
MEM_DATA<54>      9B8<> 10C1<>
MEM_DATA<55>      9B8<> 10C1<>
MEM_DATA<56>      9B8<> 10C1<>
MEM_DATA<63..56>  36A5>
MEM_DATA<57>      9B8<> 10C1<>
MEM_DATA<58>      9B8<> 10C1<>
MEM_DATA<59>      9B8<> 10C1<>
MEM_DATA<60>      9B8<> 10C1<>
MEM_DATA<61>      9B8<> 10B1<>
MEM_DATA<62>      9B8<> 10B1<>
MEM_DATA<63>      9B8<> 10B1<>
MEM_DQM<0>        9C6<> 10C7<> 36C5>
MEM_DQM<1>        9C6<> 10B7<> 36C5>
MEM_DQM<2>        9C6<> 10C5<>
MEM_DQM<3..2>     36B5>
MEM_DQM<3>        9C6<> 10B5<>
MEM_DQM<4>        9C6<> 10C3<>
MEM_DQM<5..4>     36B5>
MEM_DQM<5>        9C6<> 10B3<>
MEM_DQM<6>        9C6<> 10C1<> 36B5>
MEM_DQM<7>        9C6<> 10B1<> 36A5>
MEM_DQS<0>        9C6<> 10C7<> 36C5>
MEM_DQS<1>        9C6<> 10B7<> 36C5>
MEM_DQS<2>        9C6<> 10C5<>
MEM_DQS<3..2>     36B5>
MEM_DQS<3>        9C6<> 10B5<>
MEM_DQS<4>        9C6<> 10C3<>
MEM_DQS<5..4>     36B5>
MEM_DQS<5>        9C6<> 10B3<>
MEM_DQS<6>        9C6<> 10C1<> 36B5>
MEM_DQS<7>        9C6<> 10B1<> 36A5>
MEM_MUXSEL_H<0>   9B6< 10A6<
MEM_MUXSEL_H<1..0>  36A5>
MEM_MUXSEL_H<1>   9B6< 10A4<
MEM_MUXSEL_L<0>   9B6< 10A6<
MEM_MUXSEL_L<1..0>  36A5>
MEM_MUXSEL_L<1>   9B6< 10A4<
MEM_RAS_L         9A5< 9C6<> 36A5>
MEM_WE_L          9A5< 9C6<> 36A5>
MLB_ALS_GAIN_SW   23C4<> 23C8<>
MLB_ALS_OP_COMP   23D7<
MLB_ALS_OP_IN     23D7<
MLB_ALS_OUT       23C4<> 23D6<
MLB_ALS_OUT_FB    23D7<>
MLB_PHOTODIODE    23D8<>
MODEM_USB_DM      14B1< 25C3<> 37A2> 39B6>
MODEM_USB_DP      14B1< 25C3<> 37A2> 39B6>
MOD_BITCLK        14A2< 25C3<> 39B1>
MOD_CLKOUT        14A2< 25C4<> 39A1>
MOD_DTO           14A2< 25C4<> 39A1>
MOD_SYNC          14A2< 25C3<> 39A1>
MPIC_CPU_INT_L    5B2< 5B4< 14B5>
NEC_AMC_TP        26A5<
NEC_AVDD          26D6< 38A3>
NEC_AVSS_F        26A5< 26B4<
NEC_CRUN_L        26A7<>
NEC_IDSEL         26B7<
NEC_IO_RESET_L    26B7< 26B7<
NEC_LEFT_USB_OVERCURRENT  24B2<> 26C1< 39D1>
NEC_LEFT_USB_PWREN  24B2<> 26B5<> 39D1>
NEC_LEGC          26A7<
NEC_MAIN_RESET_L  26A7< 26B7<
NEC_NANDTESTEN_TP  26A5<
NEC_NANDTESTOUT_TP  26A4<>
NEC_NC1_TP        26B5<>
NEC_NC2_TP        26B5<>
NEC_OCI<1>        26B5< 26C3<
NEC_OCI<2>        26B5< 26C3<
NEC_OCI<3>        26B5<
NEC_OCI<4>        26B5<
NEC_OCI<5>        26B5<
NEC_PCI_INTA_L    26A7< 26B7>
NEC_PCI_INTB_L    26A7< 26B7>
NEC_PCI_INTC_L    26A7< 26B7>
NEC_PCI_PERR_L    26B7<> 26C8<
NEC_PCI_SERR_L    26B7> 26C8<
NEC_PME_L         26A7> 26B7<
NEC_PPON3_TP      26B5>
NEC_PPON4_TP      26B5>
NEC_PPON5_TP      26B5>
NEC_RIGHT_USB_OVERCURRENT  26C1< 32B7<> 39C1>
NEC_RIGHT_USB_PWREN  26B5<> 32A7<> 39C1>
NEC_RREF          26B5<>
NEC_SMI_L_TP      26A7>
NEC_USB_DAM       26B4< 26C3<> 37B2>
NEC_USB_DAP       26A4< 26C4<> 37B2>
NEC_USB_DBM       26A4< 26C3<> 37B2>
NEC_USB_DBP       26A4< 26C3<> 37B2>
NEC_USB_RSDM1     26C5<> 37B2>
NEC_USB_RSDM2     26C5<> 37B2>
NEC_USB_RSDP1     26C5<> 37B2>
NEC_USB_RSDP2     26C5<> 37B2>
NEC_XT1           26D5< 36B1>
NEC_XT2           26D5<> 36B1>
NEC_XT2_R         26D4<
NTEST1_TP         26B5<
NUMLOCK_LED       23B8<
NUMLOCK_LED_L     23B8< 30C7<
OVER_18V_ADJ      31C3<>
PCI1510_VR_EN_L   17C7<
PCI_AD<0>         9C3< 12D6<> 17C7<> 24B5<> 26D7<>
                  39B6>
PCI_AD<31..0>     37C5>
PCI_AD<1>         9C3< 12D6<> 17C7<> 24B6<> 26D7<>
                  39A6>
PCI_AD<2>         9C3< 12D6<> 17C7<> 24C5<> 26D7<>
                  39A6>
PCI_AD<3>         9C3< 12D6<> 17C7<> 24C6<> 26C7<>
                  39A6>
PCI_AD<4>         9C3< 12D6<> 17C7<> 24C5<> 26C7<>
                  39A6>
PCI_AD<5>         9C3< 12D6<> 17C7<> 24C6<> 26C7<>
                  39A6>
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D | C | B | A

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

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PCI_PAR          12C7<> 17B7<> 24C5<> 26B7<> 37C5>
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PCI_TRDY_L       12B7< 12C7<> 17A7<> 24C5<> 26B7<>
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PMU_AC_IN        30B4<>
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PMU_BATT1_DET_L_PU  30B4<> 30D2<
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PMU_CAPSLOCK_LED_L  30C6<>
PMU_CHARGE_V     30C4<> 31B8<>
PMU_CHRG_BATT_S  30C4<> 31A8<>
PMU_CLK          14C2<> 30C4<>
PMU_CNVSS        30B6< 30C7<>
PMU_CPU_RESET_L  23A4< 23C4<> 30C4<>
PMU_EPM          30D2< 30D4<>
PMU_FROM_INT     14C2<> 30C4<>
PMU_I2C_CLK      30B4<> 30C2<
PMU_I2C_DATA     30B4<> 30C2<
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PMU_INT_NMI      14B5<> 14B7< 30D4<>
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PMU_KB_RESET_IN2  30A7<>
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PMU_NMI_BUTTON_L  25C1< 30C2< 30C4<>
PMU_NMI_L        30C2< 30C4<>
PMU_NUMLOCK_LED_L  30C6<>
PMU_OOPS         30B2< 30B4<>
PMU_PME_L        14B5<> 26B8< 30B2< 30C4<>
PMU_POWERUP_OK   30B4<> 30D2<
PMU_POWER_UP_L   29C7<> 30C6<> 30D7< 33B6<
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PMU_RESET_BUTTON_L  25B1< 30C4<> 30D2<
PMU_RESET_L      30B6<>
PMU_SLEEP_LED    23C4<>
PMU_SLEEP_LED_L  23C2<> 30C4<>
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PMU_SMB_DATA     30B4<> 30C2< 31A2<
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RAM_ADDR<4>      9B4< 11B5<> 11B6<>
RAM_ADDR<5>      9B4< 11B3<> 11B8<>
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RAM_ADDR<7>      9B4< 11B3<> 11B8<>
RAM_ADDR<8>      9B4< 11B5<> 11B6<>
RAM_ADDR<9>      9A4< 11B3<> 11B8<>
RAM_ADDR<10>     9A4< 11B3<> 11B8<>
RAM_ADDR<11>     9A4< 11B5<> 11B6<>
RAM_ADDR<12>     9A4< 11B3<> 11B8<>
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RAM_DQM_B<6>     10C2<> 11A3<> 36B5>
RAM_DQM_B<7>     10C2<> 11A3<> 36A5>
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RAM_MUXSEL_L     10A4< 10A5< 10B5<> 10B7<> 36A5>
RAM_RAS_L        9A4< 11B5<> 11B6<> 36A5>
RAM_WE_L         9A4< 11B3<> 11B8<> 36A5>
RF_DISABLE_L_EPM  24B4<> 39C1>
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ROM_OE_L         9B3< 12A5< 24C5<> 39B1>
ROM_ONBOARD_CS_L  9B3< 24C6<> 39B1>
ROM_RW_L         9B3< 12A5< 24C6<> 39B1>
ROM_WP_L         9B3<
RSDM3_TP         26C5>
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RSDM5_TP         26C5>
RSDP3_TP         26C5>
RSDP4_TP         26C5>
RSDP5_TP         26C5>
RUN_ON_AC        29C6<>
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SI_DDC_DATA      19C5<> 20B7<
SI_EDGE          20B7<
SI_MSEN          20B6<>
SI_PD            20B7<
SI_RST           20B7<
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SI_VREF          20A5< 20A7<
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SLEEP_L_LS5_NET  33B3<> 35C8<>
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SND_AMP_MUTE_L   14C5<> 25D5<>
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SRMOD_TP         26A5< 39A4>
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ST7_SENSOR4_SDA_PD  23B2< 23D4<>
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ST7_SENSOR5_SDA_PU  23B2< 23D4<>
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ST7_XTAL_IN      23C5<
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SYSCLK_CPU_UF    8A6<> 36D1>
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7202	B
SCALE: NONE	SHT 42 OF 44	

*** Part Cross-Reference for the entire design ***

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J3	CON_F14RT_S2MT_SM	24
J4	CON_3RTSM_125	25
J5	CON_12	34
J6	CON_F30RT_S2MT_SM	22
J7	CON_4RT_WRIB	22
J8	CON_F16ST_D_SMA	25
J9	CON_M80ST_D4MT_SM	17
J10	CON_M50SM_5MM	24
J11	CON_F14RT_S2MT_SM	32
J12	CON_F30ST_D_SM	25
J13	CON_M50SM_5MM	24
J14	CON_F30RT_T6MT_TH1	22
J15	CON_F5RT_MINIDIN_TH	22
J16	CON_10STSM_5087	25
J17	CON_RJ45_SHORT_4MT_TH	27
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J22	CON_F200RT_DDRDIMM_SM2	11
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