1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
C		397426	PRODUCTION RELEASED	08/30/05	?

SCHEM,MLB,PBG4 17"

8/23/2005

BOM OPTIONS	STUFF	NO STUFF
D3_HOT		√
D3_COLD	√	
GPU_SS	√	
GPU_SWITCH	√	
SERIAL_DEBUG		√
VCORE_OFFSET	√	
1_8V_MAXBUS	√	
1_5V_MAXBUS		√
NEC_USB	√	
INTREPID_USB		√
BBANG		√
NO_BBANG	√	
ATI_MEMIO_HI	√	
ATI_MEMIO_LO		√
SSCG		√
NO_SSCG	√	
5V_HD_LOGIC	√	
3V_HD_LOGIC		√
EXT_TMDS		√
INT_TMDS	√	
NO_4XVCORE	√	
INT_CLK	√	
EXT_CLK		√

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6654	1	SCHEM,MLB,PBG4 17	SCH1	
820-1615	1	PCBF,MLB,PBG4 17	PCB1	
826-4393	1	LABEL,PCB,28MM X 6MM	EEE:R94	LABEL_64MB
826-4393	1	LABEL,PCB,28MM X 6MM	EEE:R95	LABEL_128MB

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES °
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer Inc.

TITLE
SCHEM,MLB,PBG4 17"

DRAWING NUMBER 051-6654 REV. C

SHT 1 OF 44

U44 INTREPID

J18 Ethernet Connector P.28
4 DATA PAIRS
U49 Ethernet PHY P.28
G/MII
3.3V
10/100/1000
8BIT TX
8BIT RX
125MHZ

J24 FW - A Connector P.30
2 DATA PAIRS @ 200MHz
J22 FW - B Connector P.30
2 DATA PAIRS @ 400MHz
U28 FireWire PHY P.29
1394 OHCI
3.3V
8BIT TX/RX
100MHZ

J11 OPTICAL DRIVE Connector P.25
EIDE
J13 ULTRA ATA/100 Connector P.25
UIDE

SLEEP LED P.26
LMU
J14 TUBA (SOUND) Connector P.26
I2S
I2C
U48/J2/J4 Fan Circuit P.26
I2C

J25 Battery Connector P.32
Power Supply & Charger P.32-36
J19 SUTRO (PWR) Connector P.32
SMBUS
3.3V
U39 PMU P.31
SERIAL
5V
U36 LMU P.24
I2C

J10 CARDBUS Connector P.18
33MHZ
16/32 BITS
3.3V/5V
U26 TI PCI1510 CardBus Controller P.18
PCI BUS
32BITS
33MHZ
3.3V

J3 (SHARE WITH BLUETOOTH) LEFT USB P.25
USB 2.0
J12 RIGHT USB BACKUP BATTERY P.33
NOT USED
USB 2.0
J3 (SHARE WITH LEFT USB) BlueTooth P.25
NOT USED
J9 Modem Board Connector P.26
INTRPEID
I2C

ETHERNET 10/100/1000 P.14	FIREWIRE 800 MB/S P.14	UATA 100 P.14	EIDE P.14	CARDSLOT P.14	I2S P.15	I2C P.14 P.15

NOT USED

USB PORT A P.15
USB PORT B P.15
USB PORT C P.15
USB PORT D P.15
USB PORT E P.15
USB PORT F P.15
MAXBUS P.9

SCCA P.15
VIA/PMU P.15
BOOTROM P.14
PCI 32BITS 33MHZ P.13
4X AGP P.13

J5 Serial Debug Connector P.26

U17 BOOT ROM 1M X 8 P.10
U52 USB 2.0 CONTROLLER P.27

J15 TRACKPAD Connector | Keyboard Connector
KB LED LIGHT SENSOR P.24

AGP BUS
1.5V/3.3V
32BITS
66MHZ

U43 ATI M11 64MB P.18-21
MEMORY CH. A (INTERNAL MEM)
MEMORY CH. C (INTERNAL MEM)
MEMORY CH. B (INTERNAL MEM)
MEMORY CH. D (INTERNAL MEM)

J21 AIRPOPT Connector P.25

J8 Inverter Connector P.22
LVDS
EDID (I2C)
S-VIDEO
COMPOSITE
TMDS
RGB
(DDC TOO)

J7 LCD Panel Connector P.22
J17 S-Video Connector P.22
J16 DVI-I Connector P.22

MAXBUS
1.8V
167MHZ
32BIT ADDRESS
64BIT DATA
U42 APOLLO CPU (MPC7457) P.5-6
CPU PLL Config P.7
PMU

DDR MEMORY P.10
MEMORY BUS
2.5V
167MHZ
64BITS
U11/U12/U13/U14 2:1 DDR MUXES P.11
J20/J23 DDR SDRAM DIMM 0
DDR SDRAM DIMM 1 SO-DIMM Connector P.12

SYSTEM BLOCK DIAGRAM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	C

SCALE NONE | SHT 2 OF 44

POWER SYSTEM ARCHITECTURE

AC ADAPTER IN PG 31

INRUSH LIMITER PG 30

+24V_PBUS

1V20_REF
>-13.44V TURNS-ON
<-13.44V SHUTS-OFF
U21 PG 31

RUN/SS
BUCK REGULATOR (LTC1625) PG 32
VCC
AC: 12.8V
NO AC: BATTERY VOLTAGE
1625 NOT RUNNING
SHUTDOWN: RUNNING
SLEEP: RUNNING
RUN: RUNNING

+PBUS (12.8V)

BACKLIGHT INVERTER

+5V_MAIN
VCC
MAIN 2.5V/1.5V DC/DC (MAX1715) PG 35
PGOOD
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING
TURNS ON OUTPUT @ 2.4V ON1/ON2

MAP31 DDR I/O
MAP31 DDR CORE
DDR POWER
+2.5V_MAIN
1_5V_2_5V_OK
+1.5V_MAIN
INTREPID CORE
AGP I/O

DCDC_EN
SLEEP
MAXBUS SEQUENCING

+PBUS

+5V_MAIN
VCC
SHDN
DC/DC (MAX1717) PG 34
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING
CPU_VCORE (+1.4V/+1.5V)

14V_PBUS

+3V_PMU LDO PG 32
+BATT
+5V_MAIN
+3V_PMU
+4_6V_BU

RC AT 1M*0.047UF @ 24V
STARTS 2.0MSEC AFTER DCDC_EN_L BECOMES LOW

RUN/SS - 5V
TURNS ON AT >1V
<100UA ALLOWED
INTERNAL ZENER CLAMP TO 6V
MAIN 3V/5V DC/DC (LTC3707) PG 33
VCC
PGOOD
STBYMD
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING
INTERNAL ZENER CLAMP TO 6V
<100UA ALLOWED
TURNS ON AT >1V
RUN/SS - 3V

+5V_MAIN
3V_5V_OK
HOLDS BOTH RUN/SS AT GND WHEN IT'S CONNECTED TO GND
TURNS CONTROL TO RUN/SS WHEN IT'S OPEN
+3.3V_MAIN

DCDC_EN_L
AFTER PMU IS UP AND RUNNING
DCDC_EN_L WILL PULL ON1/ON2 LOW IN SHUTDOWN

+5V_MAIN
+PBUS (12.8V)
EXT_VCC
VCC
DC/DC (LTC1778) PG 20
SHUTDOWN: STOPPED
SLEEP: D3HOT/D3COLD
RUN: RUNNING
TURNS ON AS LOW AS 0.8V/TYP 1.5V
INTERNAL 1.2UA CURRENT SOURCE
RUN/SS
GPU_VCORE +1.2V/+1.0V

DCDC_EN
SLEEP
D3_COLD
GPU_VCORE SEQUENCING
1M & 0.1UF @14V, IT TAKES ~5.88MS TO START SWITCHER
1_5V_2_5V_OK
D3_HOT
DCDC_EN_L
D3_HOT
1_5V_2_5V_OK WILL NOT PULL LOW UNTIL +5V_MAIN TURNS ON
HOWEVER, 5V SHOULD TURN ON ~2.23MS AFTER DCDC_EN_L OR PMU_POWERUP_L BECOMES '1'; MUCH LESS THAN THE RC CHARGING AT INT_VCC (5V)

+PBUS
BACKUP BATTERY
CHARGER INPUT & BOOST OUTPUT PG 32
12.8V CHARGES BACKUP BATTERY
24V IS OUTPUT ONLY FROM BACKUP BATTERY
BACKUP BATTERY CIRCUIT CHARGES OFF +PBUS AND PREVENTS +PBUS AND +24V_PBUS FROM DROPPING BELOW 6V (UNTIL DRAINED)

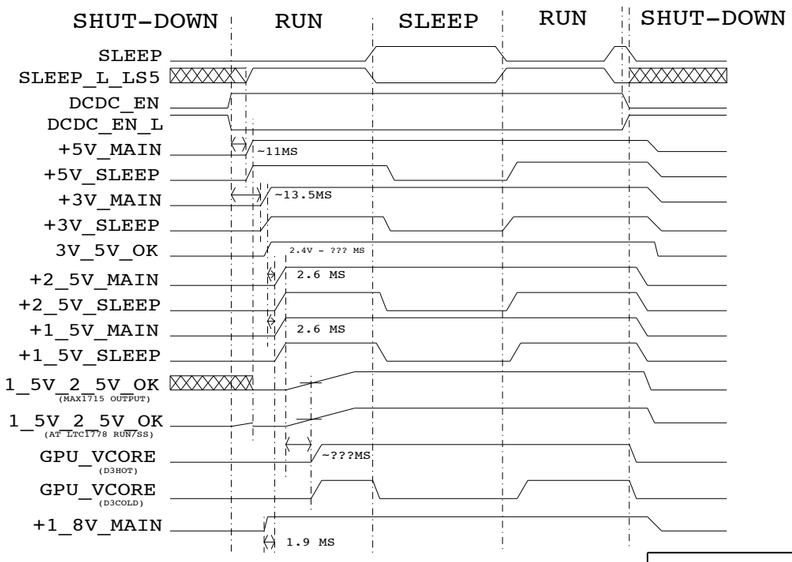
RC AT 1M*0.1UF @ 24V
STARTS ~4.25MSEC AFTER DCDC_EN_L BECOMES LOW
NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED
+24V_PBUS

DC/DC (LTC3411) PG 35
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING
+1.8V_MAIN
MAXBUS BROADCOM

BATTERY CHARGER (MAX1772) PG 31
+BATT

3S 3P PRISMATIC CELLS

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED
BATTERY VOLTAGE FEED-IN PATH PG 31
+PBUS



POWER BLOCK DIAGRAM

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6654 | REV. C

SCALE NONE | SHT 3 OF 44

PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 12
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

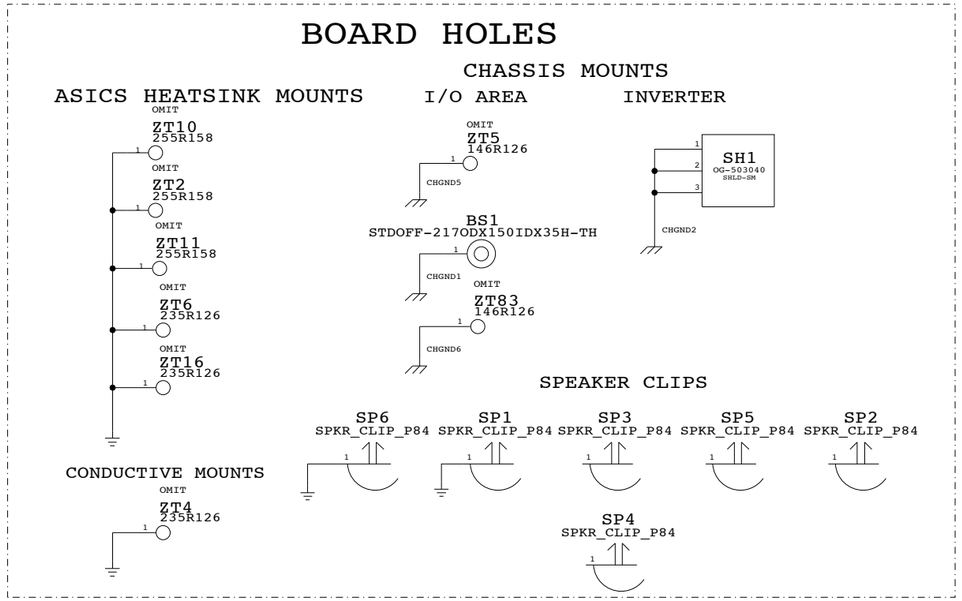
SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

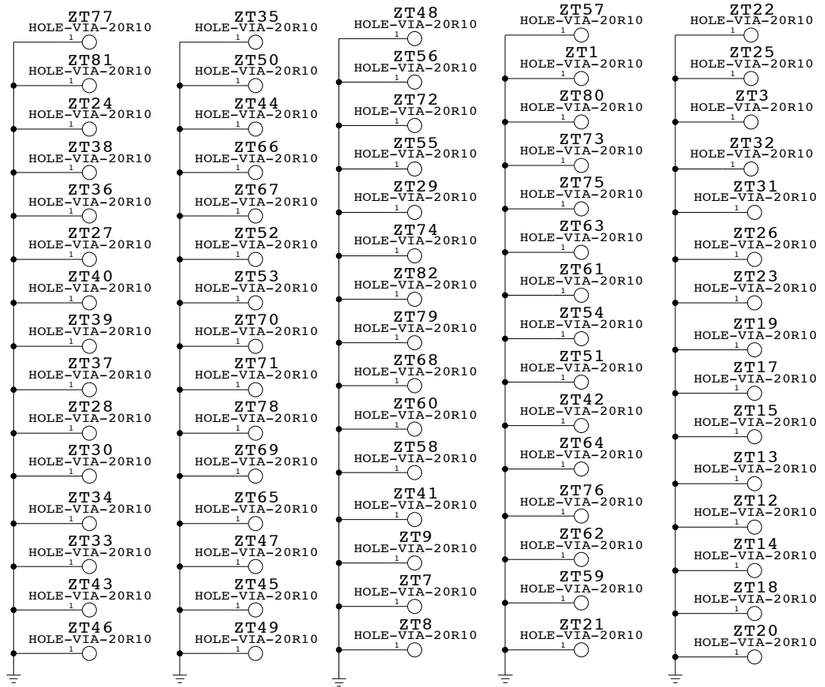
20R10 TH VIA OR VIA IN PAD

1		SIGNAL (1/3 OZ + COPPER PLATING)
2	PREPREG (3MIL)	GROUND (1/2 OZ)
3	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
4	PREPREG (3MIL)	SIGNAL (1/2 OZ)
5	LAMINATE (4MIL)	GROUND (1/2 OZ)
6	PREPREG (2MIL)	CUT POWER PLANE(1 OZ)
7	LAMINATE (3MIL)	CUT POWER PLANE(1 OZ)
8	PREPREG (2MIL)	GROUND (1/2 OZ)
9	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
10	PREPREG (3MIL)	SIGNAL (1/2 OZ)
11	LAMINATE (4MIL)	GROUND (1/2 OZ)
12	PREPREG (3MIL)	SIGNAL (1/3 OZ + COPPER PLATING)

BOARD HOLES



GROUND VIAS



BOARD INFORMATION

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	C
SCALE: NONE	SHT 4 OF 44	

CPU_VCORE DECOUPLING NETWORK

CPU_VCORE_SLEEP 5 6 34 38 39

R241 470 5% 1/16W MF 402

C25 10uF 20% 6.3V CERM 805
C342 10uF 20% 6.3V CERM 805
C344 10uF 20% 6.3V CERM 805
C346 10uF 20% 6.3V CERM 805
C8 10uF 20% 6.3V CERM 805
C153 0.1uF 20% 10V CERM 402
C12 2.2uF 20% 10V CERM 805
C340 2.2uF 20% 10V CERM 805
C193 0.1uF 20% 10V CERM 402

C223 0.1uF 20% 10V CERM 402
C91 0.1uF 20% 10V CERM 402
C114 0.1uF 20% 10V CERM 402
C104 0.1uF 20% 10V CERM 402
C103 0.1uF 20% 10V CERM 402
C110 0.1uF 20% 10V CERM 402
C190 0.1uF 20% 10V CERM 402
C189 0.1uF 20% 10V CERM 402
C138 0.1uF 20% 10V CERM 402
C191 0.1uF 20% 10V CERM 402
C112 0.1uF 20% 10V CERM 402
C168 0.1uF 20% 10V CERM 402
C149 0.1uF 20% 10V CERM 402
C111 0.1uF 20% 10V CERM 402
C150 0.1uF 20% 10V CERM 402
C105 0.1uF 20% 10V CERM 402
C154 0.1uF 20% 10V CERM 402
C115 0.1uF 20% 10V CERM 402
C113 0.1uF 20% 10V CERM 402
C152 0.1uF 20% 10V CERM 402
C151 0.1uF 20% 10V CERM 402
C202 0.1uF 20% 10V CERM 402
C201 0.1uF 20% 10V CERM 402
C192 0.1uF 20% 10V CERM 402

MORE 0805 10UF CAPS ON VCORE POWER SUPPLY PAGE (PG 33)

PLCAE SHORT CLOSE TO CENTER OF CPU

XW31 SM

25 ADT7460_VCORE_MON 1 OMIT 2

C195 10UF 20% 6.3V CERM 805
C347 10UF 20% 6.3V CERM 805
C258 10UF 20% 6.3V CERM 805
C345 10UF 20% 6.3V CERM 805
C156 10UF 20% 6.3V CERM 805
C341 10UF 20% 6.3V CERM 805
C225 10UF 20% 6.3V CERM 805
C343 10UF 20% 6.3V CERM 805

PLACE BELOW CPU IN FORMER L3 AREA

CPU_OVDD DECOUPLING NETWORK

MAXBUS_SLEEP 5 7 8 15 16 23 34 38

R206 470 5% 1/16W MF 402

C72 0.1uF 20% 10V CERM 402
C48 0.1uF 20% 10V CERM 402
C38 0.1uF 20% 10V CERM 402
C74 0.1uF 20% 10V CERM 402
C275 0.1uF 20% 10V CERM 402
C46 0.1uF 20% 10V CERM 402
C47 0.1UF 20% 10V CERM 402
C170 0.1UF 20% 10V CERM 402
C73 0.1uF 20% 10V CERM 402
C39 0.1uF 20% 10V CERM 402
C107 0.1uF 20% 10V CERM 402
C90 0.1uF 20% 10V CERM 402
C257 0.1uF 20% 10V CERM 402
C272 0.1uF 20% 10V CERM 402
C188 0.1UF 20% 10V CERM 402
C155 0.1UF 20% 10V CERM 402
C92 0.1UF 20% 10V CERM 402
C224 0.1uF 20% 10V CERM 402
C40 0.1uF 20% 10V CERM 402
C194 0.1uF 20% 10V CERM 402
C203 0.1uF 20% 10V CERM 402
C273 0.1uF 20% 10V CERM 402
C41 0.1uF 20% 10V CERM 402
C169 0.1UF 20% 10V CERM 402
C139 0.1UF 20% 10V CERM 402
C106 0.1UF 20% 10V CERM 402

VDD H8 H10 H12 J7 J9 J11 J13 K8 K10 K12 K14 L7 L9 L11 L13 M8 M10 M12

OVDD B4 C2 C12 D5 F2 H3 J5 K2 L5 M3 N6 P2 P8 P11 R4 R13 R16 T6 T9 U2 U12 U16 V4 V7 V10 V14 E18 G18

AVDD A8

OVDDSENSE

CPU_VCORE_SLEEP

R106 10 1% 1/16W MF 402 — CPU_VCORE_SLEEP 5 6 34 38 39

NO STUFF

38 CPU_AVDD

C137 0.1uF 20% 10V CERM 402
C136 4.7UF 20% 6.3V CERM 805

R280 10 1% 1/16W MF 402 — CPU_AVDD_VOUT

VOUT = 0.59*(1+R1/R2)
PLACE RXXX AND RXXX CLOSE TO UXX PIN 5 AND 6

+3V_SLEEP

R276 0 5% 1/10W MF 603

CRITICAL

U6 FAN2558 SOT23-6

CPU_AVDD_VIN 1 VIN
CPU_AVDD_PG 4 PG
VCORE_SHDN_L 34 3 EN
GND 2
VOUT 6
ADJ 5

R275 47K 5% 1/16W MF 402

R282 63.4K 1% 1/16W MF 402
R283 52.3K 1% 1/16W MF 402

CPU_AVDD_ADJ

C283 2.2UF 20% 6.3V CERM1 603

C909 1UF 10% 6.3V CERM 402

CPU INTERNAL PLL FILTERING

MAXBUS_SLEEP 5 7 8 15 16 23 34 38

BBANG

R86 470 5% 1/16W MF 402

470OHM FOR BOOT BANGER

39 23 5 JTAG_CPU_TRST_L

NO_BBANG

R85 200 5% 1/16W MF 402

MPC7447 PULL-UPS

+1_5V_SLEEP — 1_5V_MAXBUS — R702 0 5% 1/16W MF 603

+1_8V_SLEEP — 1_8V_MAXBUS — R693 0 5% 1/16W MF 603

38 34 23 16 15 8 7 5 MAXBUS_SLEEP

8 5 CPU_TBEN	R58 10K 5% 1/16W MF 402	
5 CPU_CHKS_L		R160 10K 5% 1/16W MF 402
5 CPU_SHD0_L	R73 10K 5% 1/16W MF 402	
5 CPU_SHD1_L		R87 10K 5% 1/16W MF 402
5 CPU_MCP_L	R139 10K 5% 1/16W MF 402	
5 CPU_LSSD_MODE		R108 10K 5% 1/16W MF 402
5 CPU_L2TSTCLK	R72 10K 5% 1/16W MF 402	
39 5 CPU_CHKSTP_OUT_L		R57 1K 5% 1/16W MF 402
5 CPU_SRWX_L	R148 10K 5% 1/16W MF 402	
5 CPU_PMONIN_L		R120 10K 5% 1/16W MF 402
5 CPU_EMODE1_L	R109 10K 5% 1/16W MF 402	
5 CPU_PULLUP		R98 1K 5% 1/16W MF 402
39 23 7 5 CPU_HRESET_L	R107 10K 5% 1/16W MF 402	
30 5 CPU_SMI_L		R129 10K 5% 1/16W MF 402
39 23 5 JTAG_CPU_TMS	R59 470 5% 1/16W MF 402	
39 23 5 JTAG_CPU_TDI		R128 470 5% 1/16W MF 402
14 5 MPIC_CPU_INT_L	R79 10K 5% 1/16W MF 402	
39 5 CPU_SRESET_L		R65 10K 5% 1/16W MF 402
5 CPU_L1TSTCLK	R130 10K 5% 1/16W MF 402	
5 CPU_EDTI		R60 10K 5% 1/16W MF 402
39 23 5 JTAG_CPU_TCK	R97 10K 5% 1/16W MF 402	
5 CPU_PULLDOWN		R61 470 5% 1/16W MF 402

4700HM FOR BOOT BANGER

4700HM FOR BOOT BANGER

4700HM FOR BOOT BANGER

CPU_BUS_VSEL

CPU_BR_L D2 → BR*
CPU_BG_L M1 → BG*
NC → TS*
CPU_TS_L L4
CPU_PULLDOWN 5 → A0 E11
A1 H1
A2 C11
A3 G3
CPU_ADDR<0> F10 → A4
CPU_ADDR<1> L2 → A5
CPU_ADDR<2> D11 → A6
CPU_ADDR<3> D1 → A7
CPU_ADDR<4> C10 → A8
CPU_ADDR<5> G2 → A9
CPU_ADDR<6> D12 → A10
CPU_ADDR<7> L3 → A11
CPU_ADDR<8> G4 → A12
CPU_ADDR<9> T2 → A13
CPU_ADDR<10> F4 → A14
CPU_ADDR<11> V1 → A15
CPU_ADDR<12> J4 → A16
CPU_ADDR<13> R2 → A17
CPU_ADDR<14> K5 → A18
CPU_ADDR<15> W2 → A19
CPU_ADDR<16> J2 → A20
CPU_ADDR<17> K4 → A21
CPU_ADDR<18> N4 → A22
CPU_ADDR<19> J3 → A23
CPU_ADDR<20> M5 → A24
CPU_ADDR<21> P5 → A25
CPU_ADDR<22> N3 → A26
CPU_ADDR<23> T1 → A27
CPU_ADDR<24> V2 → A28
CPU_ADDR<25> U1 → A29
CPU_ADDR<26> N5 → A30
CPU_ADDR<27> W1 → A31
CPU_ADDR<28> B12 → A32
CPU_ADDR<29> C4 → A33
CPU_ADDR<30> G10 → A34
CPU_ADDR<31> B11 → A35

NC C1 → AP0
NC E3 → AP1
NC H6 → AP2
NC F5 → AP3
NC G7 → AP4

CPU_TT<0> E5 → TT0
CPU_TT<1> E6 → TT1
CPU_TT<2> F6 → TT2
CPU_TT<3> E9 → TT3
CPU_TT<4> C5 → TT4
CPU_TBST_L F11 → TBST*
CPU_TSIZ<0> G6 → TSIZ0
CPU_TSIZ<1> F7 → TSIZ1
CPU_TSIZ<2> E7 → TSIZ2
CPU_GBL_L E2 → GBL*
CPU_WT_L D3 → WT*
CPU_CI_L J1 → CI*
CPU_AACK_L R1 → AACK*
CPU_ARTRY_L N2 → ARTRY*
5 CPU_SHD0_L E4 → SHD0*
5 CPU_SHD1_L H5 → SHD1*
CPU_HIT_L B2 → HIT*

CRITICAL

U43
1.50GHZ-1.28V
APOLL7_PM-R1.1
BGA
(1 OF 3)

BVSEL	B7	CPU_BUS_VSEL 7
SYSCLK	A10	SYSCLK_CPU 8 36
CLK_OUT	H2	CPU_CLKOUT_SPN
PLL_CFG0	B8	CPU_PLL_CFG<0> 7
PLL_CFG1	C8	CPU_PLL_CFG<1> 7
PLL_CFG2	C7	CPU_PLL_CFG<2> 7
PLL_CFG3	D7	CPU_PLL_CFG<3> 7
PLL_CFG4	A7	CPU_PLL_CFG<4> 7
DBG*	M2	CPU_DBG_L 8 36
DRDY*	R3	CPU_DRDY_L 8 36
DTI0	G1	CPU_EDTI 5
DTI1	K1	CPU_DTI<0> 8 36
DTI2	P1	CPU_DTI<1> 8 36
DTI3	N1	CPU_DTI<2> 8 36
TDI	B9	JTAG_CPU_TDI 5 23 39
TDO	A4	JTAG_CPU_TDO_TP 39
TMS	F1	JTAG_CPU_TMS 5 23 39
TCK	C6	JTAG_CPU_TCK 5 23 39
TRST*	A5	JTAG_CPU_TRST_L 5 23 39
LSSD_MODE*	E8	CPU_LSSD_MODE 5
L1_TSTCLK	G8	CPU_L1TSTCLK 5
L2_TSTCLK	B3	CPU_L2TSTCLK 5
TA*	K6	CPU_TA_L 8 36
TEA*	L1	CPU_TEA_L 8 36
TBEN	E1	CPU_TBEN 5 8
QREQ*	P4	CPU_QREQ_L 8 36
QACK*	G5	CPU_QACK_L 8 36
CKSTP_IN*	A3	
CKSTP_OUT*	B1	CPU_CHKSTP_OUT_L 5 39
INT*	D4	MPIC_CPU_INT_L 5 14
SMI*	F9	CPU_SMI_L 5 30
MCP*	C9	CPU_MCP_L 5
SRESET*	A2	CPU_SRESET_L 5 39
HRESET*	D8	CPU_HRESET_L 5 7 23 39
PMON_IN*	D9	CPU_PMONIN_L 5
PMON_OUT*	A9	NC
BMODE0*	G9	CPU_EMODE0_L 7
BMODE1*	F8	CPU_EMODE1_L 5
EXT_QUAL	A11	CPU_PULLDOWN 5
CHKS*	A12	CPU_CHKS_L 5
SRW0*	B10	CPU_PULLUP 5
SRW1*	E10	CPU_SRWX_L 5
IARTRY0*	B6	CPU_PULLUP 5
DX*	D10	CPU_PULLDOWN 5

GND: B5 C3 D6 D13 E17 F3 G17 H4 H7 H9 H11 H13 J6 J8 J10 J12 K7 K3 K9 K11 K13 L6 L8 L10 L12 M4 M7 M9 M11 M13 N7 P3 P9 P12 R5 R14 R17 T7 T10 U3 U13 U17 V5 V8 V11 V15

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
337S2855	337S2885	?	U43	ALT FOR Q16A CPU
337S2911	337S2885	?	U43	ALT FOR Q41A REV1.1.1
337S2912	337S2885	?	U43	ALT FOR Q16A REV1.1.1

MPC7447 MAXBUS

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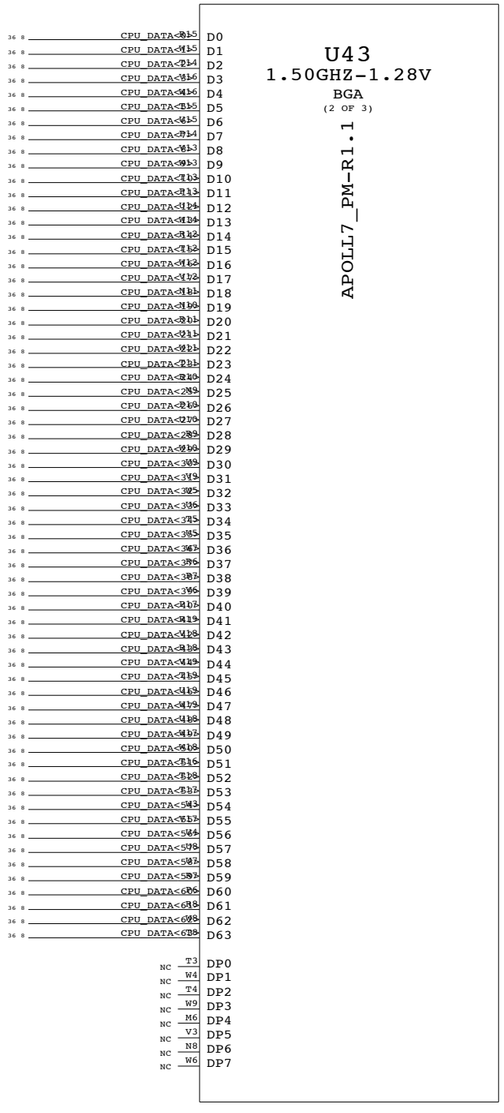
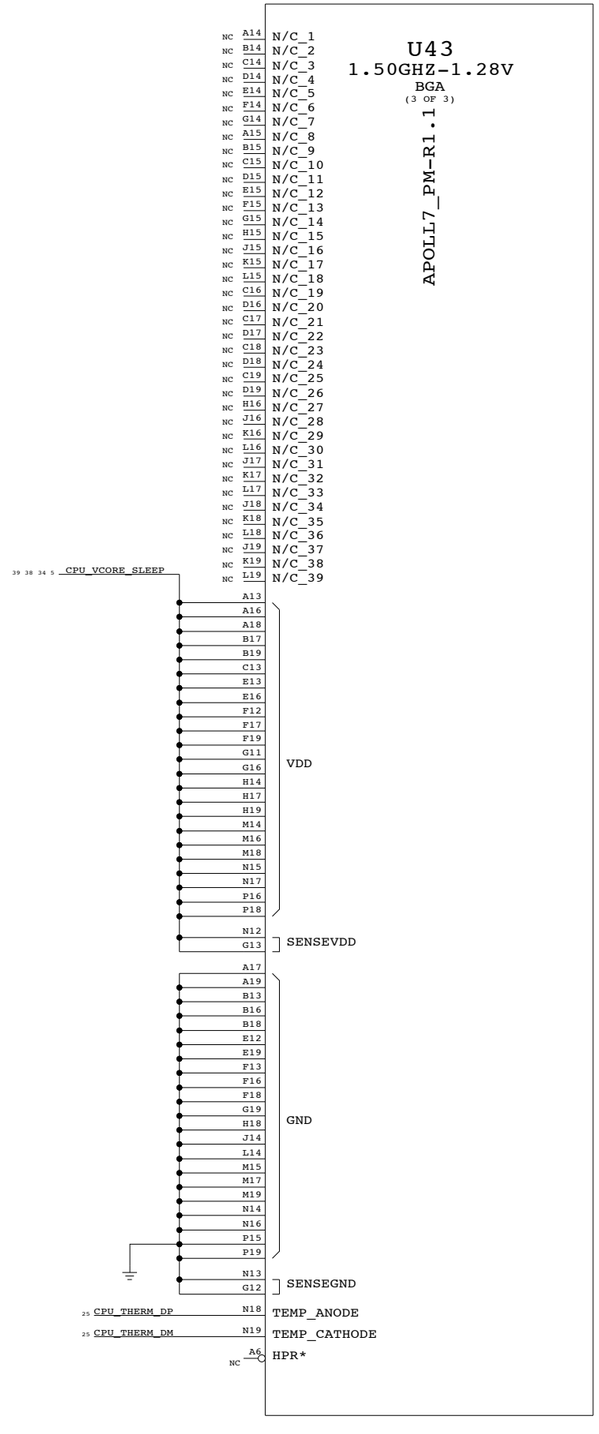
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	C
SCALE: NONE	SHT 5 OF 44	

BOOT BANGER - LMU PERORMS THIS FUNCTION IF NEEDED
SEE PAGE 22





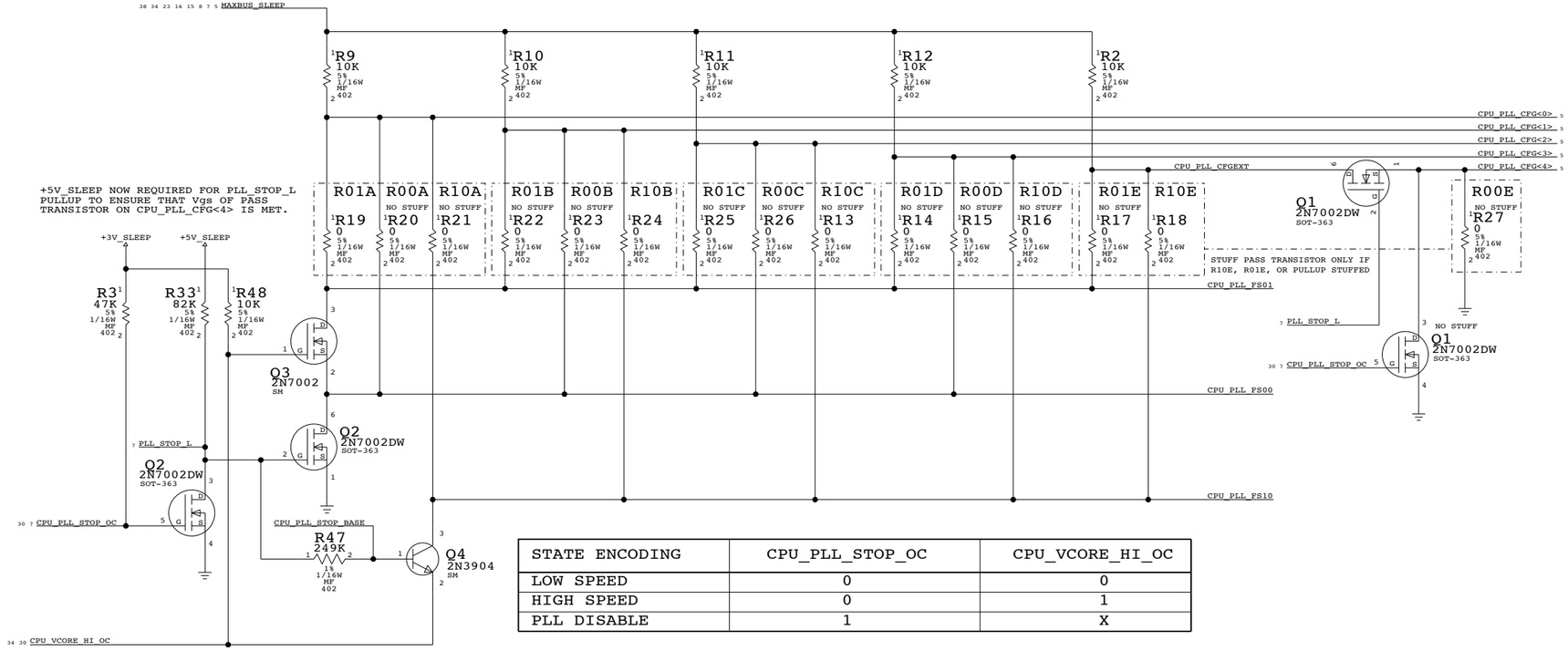
MPC7447/BBANG

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	C
SCALE: NONE	SHT 6 OF 44	

CPU PLL CONFIG CIRCUITRY



STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

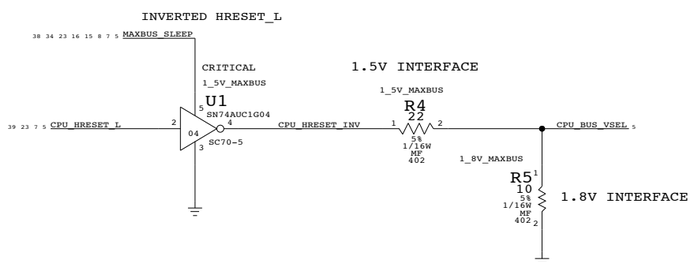
CPU FREQUENCY CONFIGURATION

APOLLO 7

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ (MHZ)	133MHZ (MHZ)	CPU_PLL_CFG 4 0123 E ABCD HEX
0.0X	PLL OFF		0 1111 0F
1.0X	PLL BYPASS		0 0011 03
2.0X	333	267	0 0100 04
3.0X	500	400	0 1000 08
4.0X	667	533	0 1010 0A
5.0X	833	667	0 1011 0B
5.5X	917	733	0 1001 09
6.0X	1000	800	0 1101 0D
6.5X	1083	867	0 0101 05
7.0X	1167	933	0 0010 02
7.5X	1250	1000	0 0001 01
8.0X	1333	1067	0 1100 0C
8.5X	1417	1133	0 0110 06
9.0X	1500	1200	1 0111 17
9.5X	1583	1267	0 0111 07
10.0X	1667	1333	1 1010 1A
10.5X	1750	1400	1 1000 18
11.0X	1833	1467	1 1001 19
11.5X	1917	1533	0 0000 00
12.0X	2000	1600	1 1011 1B
12.5X	2083	1667	1 1111 1F
13.0X	2167	1733	1 0101 15
13.5X	2250	1800	0 1110 0E
14.0X	2333	1867	1 1100 1C
15.0X	2500	2000	1 0001 11
16.0X	2667	2133	1 1101 1D
17.0X	2833	2267	1 0000 10
18.0X	3000	2400	1 0010 12
20.0X	3333	2667	1 0011 13
21.0X	3500	2800	1 0100 14
24.0X	4000	3200	1 0110 16
28.0X	4667	3733	1 1110 1E

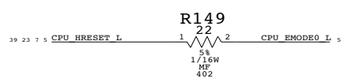
CPU CONFIGURATION

MAXBUS VSEL



DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L NEED TO CHARACTERIZE

BUSTYPE SELECT



APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

CPU CONFIGURATION

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6654 | REV. C

SCALE NONE | SHT 7 OF 44

INTREPID BOOT STRAPS

BIT 32 TO 39

38 34 23 16 15 8 7 5 MAXBUS_SLEEP

R642	R135	R123	R153	R166	R179	R651	R178
NO STUFF	NO STUFF	NO STUFF		NO STUFF	NO STUFF	NO STUFF	NO STUFF
10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402
36 8 6 CPU_DATA<32>	36 8 6 CPU_DATA<33>	36 8 6 CPU_DATA<34>	36 8 6 CPU_DATA<35>	36 8 6 CPU_DATA<36>	36 8 6 CPU_DATA<37>	36 8 6 CPU_DATA<38>	36 8 6 CPU_DATA<39>

R136	R643	R639	R657	R664	R673	R143	R674
10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	NO STUFF 10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402

BIT2 BIT1 BIT0

PLL4MODESEL_NXT[2:0]
000: 166.4MHZ (2.5X)
001: 149.76MHZ
010: 133.12MHZ (2.0X)
011: 99.84MHz (1.5X)
100: 83.20MHz

MODE A (2.5X) IS FOR STATIC OPERATION
MODE C (2.0X) IS FOR CLOCK SLEW OPERATION

Spare | Spare | PLL4MODESEL_NXT[2:0] | Internal spreadEn 0: Disable (Input output) 1: Active | PCI Source Clock 10: PLL1 (NO SPREAD) 11: PLL2 (NO SPREAD) | PCI Source Clock 10: PLL1 (NO SPREAD) 11: PLL2 (NO SPREAD)

BIT 40 TO 47

38 34 23 16 15 8 7 5 MAXBUS_SLEEP

R122	R142	R164	R134	R184	R177	R152	R165
NO STUFF	NO STUFF	NO STUFF	EXT_CLK	NO STUFF	INT_CLK	INT_CLK	INT_CLK
10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402
36 8 6 CPU_DATA<40>	36 8 6 CPU_DATA<41>	36 8 6 CPU_DATA<42>	36 8 6 CPU_DATA<43>	36 8 6 CPU_DATA<44>	36 8 6 CPU_DATA<45>	36 8 6 CPU_DATA<46>	36 8 6 CPU_DATA<47>

R640	R652	R665	R644	R683	R675	R658	R666
10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	INT_CLK 10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	EXT_CLK 10K 5% 1/16W MF 402	EXT_CLK 10K 5% 1/16W MF 402	EXT_CLK 10K 5% 1/16W MF 402

BIT2 BIT1 BIT0

Spare | Spare | PLL4MODESEL_NXT[2:0] | Internal spreadEn 0: Disable (Input output) 1: Active | PCI Source Clock 10: PLL1 (NO SPREAD) 11: PLL2 (NO SPREAD) | PCI Source Clock 10: PLL1 (NO SPREAD) 11: PLL2 (NO SPREAD)

BIT 48 TO 55

38 34 23 16 15 8 7 5 MAXBUS_SLEEP

R133	R121	R163	R151	R162	R141	R183	R176
EXT_CLK	EXT_CLK		NO STUFF	NO STUFF	NO STUFF		NO STUFF
10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402
36 8 6 CPU_DATA<48>	36 8 6 CPU_DATA<49>	36 8 6 CPU_DATA<50>	36 8 6 CPU_DATA<51>	36 8 6 CPU_DATA<52>	36 8 6 CPU_DATA<53>	36 8 6 CPU_DATA<54>	36 8 6 CPU_DATA<55>

R645	R641	R668	R659	R667	R653	R684	R676
INT_CLK	INT_CLK	NO STUFF				NO STUFF	
10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402

BIT2 BIT1 BIT0

BUF_REF_CLK_OUTEnable_h 1: Active | SelPll4ExtSrc 0: Internal source 1: External source | Spare | TTI 1394b workaround 0: Disable 1: TTI PHY workaround | Spare

MaxBus output impedance
111: 28.6 ohm
011: 33.3 ohm
101: 40 ohm
001: 50 ohm
110: 66.6 ohm
010: 100 ohm
100: 200 ohm
000: 200 ohm

THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:

1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
2/ D46 - SELPCI1SPREADCLK - SLEEP/WAKE CYCLE REQUIRED
3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT

IF A STRAP IS NOT LISTED, THEN
IT CANNOT BE CHANGED BY SOFTWARE

38 14 12 +1_5V_INTREPID_PLL — R227 4.7 5% 1/16W MF 402 — 38 +1_5V_INTREPID_PLL7

C308 0.22UF 20% 6.3V CERM 402

H26 VDD15A_7 (PLL6) CRITICAL

U45 INTREPID-REV2.1 BGA

(1 OF 9)

36 8 5 CPU_BR_L	E29	BR	INPUT	
36 8 5 CPU_BG_L	E26	BG	NO BUS KEEPER	
36 8 5 CPU_TS_L	B27	TS	NO BUS KEEPER	
36 5 CPU_ADDR<0>	D24	A_0		
36 5 CPU_ADDR<1>	D25	A_1		
36 5 CPU_ADDR<2>	A27	A_2		
36 5 CPU_ADDR<3>	E24	A_3		
36 5 CPU_ADDR<4>	G23	A_4		
36 5 CPU_ADDR<5>	B26	A_5		
36 5 CPU_ADDR<6>	A26	A_6		
36 5 CPU_ADDR<7>	D23	A_7		
36 5 CPU_ADDR<8>	A25	A_8		
36 5 CPU_ADDR<9>	E23	A_9		
36 5 CPU_ADDR<10>	J22	A_10		
36 5 CPU_ADDR<11>	B25	A_11		
36 5 CPU_ADDR<12>	H22	A_12		
36 5 CPU_ADDR<13>	G22	A_13		
36 5 CPU_ADDR<14>	D22	A_14		
36 5 CPU_ADDR<15>	B24	A_15		
36 5 CPU_ADDR<16>	B23	A_16		
36 5 CPU_ADDR<17>	E22	A_17		
36 5 CPU_ADDR<18>	J21	A_18		
36 5 CPU_ADDR<19>	G21	A_19		
36 5 CPU_ADDR<20>	E21	A_20		
36 5 CPU_ADDR<21>	A24	A_21		
36 5 CPU_ADDR<22>	D21	A_22		
36 5 CPU_ADDR<23>	A23	A_23		
36 5 CPU_ADDR<24>	H20	A_24		
36 5 CPU_ADDR<25>	B22	A_25		
36 5 CPU_ADDR<26>	H21	A_26		
36 5 CPU_ADDR<27>	A22	A_27		
36 5 CPU_ADDR<28>	E20	A_28		
36 5 CPU_ADDR<29>	B21	A_29		
36 5 CPU_ADDR<30>	D20	A_30		
36 5 CPU_ADDR<31>	A21	A_31		
36 5 CPU_CI_L	G26	CI		
36 5 CPU_GBL_L	A29	GBL		
36 5 CPU_TBST_L	A28	TBST		
36 5 CPU_TSIZ<0>	G24	TSIZ_0		
36 5 CPU_TSIZ<1>	H24	TSIZ_1		
36 5 CPU_TSIZ<2>	D26	TSIZ_2		
36 5 CPU_TT<0>	E25	TT_0		
36 5 CPU_TT<1>	G25	TT_1		
36 5 CPU_TT<2>	B28	TT_2		
36 5 CPU_TT<3>	D27	TT_3		
36 5 CPU_TT<4>	J25	TT_4		
36 5 CPU_WT_L	D28	WT		
36 8 5 CPU_AACK_L	B29	AACK	NO BUS KEEPER - PU	
36 8 5 CPU_ARTRY_L	H23	ARTRY	NO BUS KEEPER - PU	
36 8 5 CPU_HIT_L	B31	HIT	INPUT - PU	
36 8 5 CPU_QREQ_L	A32	QREQ	INPUT - PD	
36 5 CPU_QACK_L	G27	QACK	NO BUS KEEPER - ?	
30 INT_SUSPEND_REQ_L	AK9	SUSPENDREQ		
30 INT_SUSPEND_ACK_L	AM8	SUSPENDACK		
		CPU_FB_IN	Vin = Intrepid Vcore (1.5V) Vout = MaxBus rail (1.8V)	
36 8 INT_CPUFB_IN	J24			
36 8 INT_CPUFB_OUT	H16	CPU_FB_OUT	NO BUS KEEPER - PU	
SYSCLK_LA_TP	G8	ANALYZER_CLK		
30 CPU_CLK_EN	AH9	STOPCPUCLK	INPUT - PU	
INTREPID_ACS_REF	H13	ACS_REF	NO BUS KEEPER - ?	
36 SYSCLK_CPU_UF	J15	CPU_CLK	NO BUS KEEPER - PU	
5 CPU_TBEN	A31	TBEN	NO BUS KEEPER - PU	
			INTREPID OUTPUTS HIGH BY DEFAULT	

VSSA_7 (PLL6) H25

D_0	D10	CPU_DATA<0>	6 36
D_1	G12	CPU_DATA<1>	6 36
D_2	E11	CPU_DATA<2>	6 36
D_3	H11	CPU_DATA<3>	6 36
D_4	B9	CPU_DATA<4>	6 36
D_5	B8	CPU_DATA<5>	6 36
D_6	A9	CPU_DATA<6>	6 36
D_7	A8	CPU_DATA<7>	6 36
D_8	E12	CPU_DATA<8>	6 36
D_9	D11	CPU_DATA<9>	6 36
D_10	B10	CPU_DATA<10>	6 36
D_11	J13	CPU_DATA<11>	6 36
D_12	A10	CPU_DATA<12>	6 36
D_13	D12	CPU_DATA<13>	6 36
D_14	E13	CPU_DATA<14>	6 36
D_15	G13	CPU_DATA<15>	6 36
D_16	B11	CPU_DATA<16>	6 36
D_17	D13	CPU_DATA<17>	6 36
D_18	A11	CPU_DATA<18>	6 36
D_19	G14	CPU_DATA<19>	6 36
D_20	H14	CPU_DATA<20>	6 36
D_21	E14	CPU_DATA<21>	6 36
D_22	B12	CPU_DATA<22>	6 36
D_23	G15	CPU_DATA<23>	6 36
D_24	B13	CPU_DATA<24>	6 36
D_25	H15	CPU_DATA<25>	6 36
D_26	D14	CPU_DATA<26>	6 36
D_27	B14	CPU_DATA<27>	6 36
D_28	A12	CPU_DATA<28>	6 36
D_29	G16	CPU_DATA<29>	6 36
D_30	E15	CPU_DATA<30>	6 36
D_31	J16	CPU_DATA<31>	6 36
D_32	D15	CPU_DATA<32>	6 8 36
D_33	A14	CPU_DATA<33>	6 8 36
D_34	A13	CPU_DATA<34>	6 8 36
D_35	D16	CPU_DATA<35>	6 8 36
D_36	E16	CPU_DATA<36>	6 8 36
D_37	G17	CPU_DATA<37>	6 8 36
D_38	B15	CPU_DATA<38>	6 8 36
D_39	H17	CPU_DATA<39>	6 8 36
D_40	A15	CPU_DATA<40>	6 8 36
D_41	B16	CPU_DATA<41>	6 8 36
D_42	E17	CPU_DATA<42>	6 8 36
D_43	A16	CPU_DATA<43>	6 8 36
D_44	J18	CPU_DATA<44>	6 8 36
D_45	H18	CPU_DATA<45>	6 8 36
D_46	D17	CPU_DATA<46>	6 8 36
D_47	G18	CPU_DATA<47>	6 8 36
D_48	A17	CPU_DATA<48>	6 8 36
D_49	B17	CPU_DATA<49>	6 8 36
D_50	E18	CPU_DATA<50>	6 8 36
D_51	B18	CPU_DATA<51>	6 8 36
D_52	D18	CPU_DATA<52>	6 8 36
D_53	A18	CPU_DATA<53>	6 8 36
D_54	A19	CPU_DATA<54>	6 8 36
D_55	H19	CPU_DATA<55>	6 8 36
D_56	B19	CPU_DATA<56>	6 8 36
D_57	J19	CPU_DATA<57>	6 8 36
D_58	A20	CPU_DATA<58>	6 8 36
D_59	D19	CPU_DATA<59>	6 8 36
D_60	E19	CPU_DATA<60>	6 8 36
D_61	G19	CPU_DATA<61>	6 8 36
D_62	B20	CPU_DATA<62>	6 8 36
D_63	G20	CPU_DATA<63>	6 8 36
DBG	A30	CPU_DBG_L	5 8 36
DRDY	G28	CPU_DRDY_L	5 8 36
DTI_0	K25	CPU_DTI<0>	5 36
DTI_1	D29	CPU_DTI<1>	5 36
DTI_2	B30	CPU_DTI<2>	5 36
TA	E27	CPU_TA_L	5 8 36
TEA	E28	CPU_TEA_L	5 8 36

FB BUFFER HAS 50 OHM OUTPUT IMPEDANCE

R197 511 1% 1/16W MF 402

R144 0 5% 1/16W MF 402 — 36 SYSCLK_CPU — 36 SYSCLK_CPU_UF

R137 1K 1% 1/16W MF 402

SHORT = 1" SHORTER THAN MATCHED LENGTH
LONG = 1" LONGER THAN MATCHED LENGTH

36 8 INT_CPUFB_OUT — R167 0 5% 1/16W MF 402 — 36 INT_CPUFB_OUT_SHORT

36 INT_CPUFB_OUT_SHORT — R215 0 5% 1/16W MF 402 — 36 INT_CPUFB_OUT_NORM

36 INT_CPUFB_OUT_NORM — R207 0 5% 1/16W MF 402 — 36 INT_CPUFB_LONG

36 INT_CPUFB_OUT_SHORT — NO STUFF R225 0 5% 1/16W MF 402 — 36 INT_CPUFB_IN

36 INT_CPUFB_OUT_NORM — R208 0 5% 1/16W MF 402 — NO STUFF R196 0 5% 1/16W MF 402 — 36 INT_CPUFB_IN_NORM

36 INT_CPUFB_IN — R226 0 5% 1/16W MF 402 — 36 INT_CPUFB_IN_NORM

MAXBUS PULL-UPS

MAXBUS_SLEEP 5 7 8 15 16 23 34 38

36 8 5 CPU_TS_L	RP21 10K 5% 1/16W SM1	2 7
36 8 5 CPU_TA_L	RP21 10K 5% 1/16W SM1	1 8
36 8 5 CPU_ARTRY_L	RP21 10K 5% 1/16W SM1	4 5
36 8 5 CPU_BR_L	RP23 10K 5% 1/16W SM1	1 8
36 8 5 CPU_HIT_L	RP24 10K 5% 1/16W SM1	3 6
36 8 5 CPU_DRDY_L	RP23 10K 5% 1/16W SM1	3 6
36 8 5 CPU_TEA_L	RP23 10K 5% 1/16W SM1	4 5
36 8 5 CPU_AACK_L	RP23 10K 5% 1/16W SM1	2 7
36 8 5 CPU_DBG_L	RP24 10K 5% 1/16W SM1	4 5
36 8 5 CPU_BG_L	RP21 10K 5% 1/16W SM1	3 6
36 8 5 CPU_QREQ_L	RP24 10K 5% 1/16W SM1	2 7

INTREPID BOOT STRAPS

BIT 56 TO 63

38 34 23 16 15 8 7 5 MAXBUS_SLEEP

R140	R161	R175	R132	R131	R150	R174	R182
NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF		NO STUFF
10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402
36 8 6 CPU_DATA<56>	36 8 6 CPU_DATA<57>	36 8 6 CPU_DATA<58>	36 8 6 CPU_DATA<59>	36 8 6 CPU_DATA<60>	36 8 6 CPU_DATA<61>	36 8 6 CPU_DATA<62>	36 8 6 CPU_DATA<63>

R654	R669	R677	R646	R647	R660	R678	R685
10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	10K 5% 1/16W MF 402	NO STUFF 10K 5% 1/16W MF 402	10K 5% 1/16W MF 402

Spare | Spare | Spare | PCI1_REQ2_L / GPIO[2] | PCI1_REQ1_L / GPIO[1] | PCI1_REQ0_L / GPIO[0] | Disable PHY interface 0: Legacy interface 1: B-mode interface | Processor Bus Mode 000: 60X Bus (G3)

Intrepid MaxBus

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	C
SCALE: NONE	SHT 8 OF 44	

SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

PINS ARE SWAPABLE FOR RPAKS

U45
INTREPID-REV2.1
BGA
(2 OF 9)
CRITICAL

DDR MEMORY INTERFACE

DDR_DATA_0	AK32	H35	DDR_A_0
DDR_DATA_1	AK33	G35	DDR_A_1
DDR_DATA_2	AK31	G36	DDR_A_2
DDR_DATA_3	AK35	F36	DDR_A_3
DDR_DATA_4	AK36	F35	DDR_A_4
DDR_DATA_5	AJ32	E35	DDR_A_5
DDR_DATA_6	AJ35	E36	DDR_A_6
DDR_DATA_7	AJ36	G32	DDR_A_7
DDR_DATA_8	AG33	D36	DDR_A_8
DDR_DATA_9	AG35	H36	DDR_A_9
DDR_DATA_10	AH35	G33	DDR_A_10
DDR_DATA_11	AG36	H33	DDR_A_11
DDR_DATA_12	AH36	D35	DDR_A_12
DDR_DATA_13	AH32	L30	DDR_BA_0
DDR_DATA_14	AG32	M29	DDR_BA_1
DDR_DATA_15	AG31		
DDR_DATA_16	AE32	AN34	DDRCS_0
DDR_DATA_17	AF35	AN36	DDRCS_1
DDR_DATA_18	AF36	AL35	DDRCS_2
DDR_DATA_19	AE36	AL33	DDRCS_3
DDR_DATA_20	AE35		
DDR_DATA_21	AE33	AJ31	DDR_DQS_0
DDR_DATA_22	AD36	AH31	DDR_DQS_1
DDR_DATA_23	AD35	AD32	DDR_DQS_2
DDR_DATA_24	AA36	AB30	DDR_DQS_3
DDR_DATA_25	AA35	V30	DDR_DQS_4
DDR_DATA_26	AA33	P32	DDR_DQS_5
DDR_DATA_27	AB36	N29	DDR_DQS_6
DDR_DATA_28	AB35	L32	DDR_DQS_7
DDR_DATA_29	AC36		
DDR_DATA_30	AA32	AJ33	DDR_DM_0
DDR_DATA_31	AB33	AH33	DDR_DM_1
DDR_DATA_32	V36	AD33	DDR_DM_2
DDR_DATA_33	U33	AC35	DDR_DM_3
DDR_DATA_34	U32	T35	DDR_DM_4
DDR_DATA_35	V35	T33	DDR_DM_5
DDR_DATA_36	T30	N32	DDR_DM_6
DDR_DATA_37	U36	L33	DDR_DM_7
DDR_DATA_38	U35		
DDR_DATA_39	T36	L29	DDRRAS
DDR_DATA_40	P33	H32	DDRCAS
DDR_DATA_41	R30	E30	DDRWE
DDR_DATA_42	P35	AM35	DDRCKE0
DDR_DATA_43	P36	AM35	DDRCKE1
DDR_DATA_44	R36	AM36	DDRCKE2
DDR_DATA_45	R35	AL36	DDRCKE3
DDR_DATA_46	R33		
DDR_DATA_47	R32	AB32	DDR_SELHI_0
DDR_DATA_48	N35	AE29	DDR_SELHI_1
DDR_DATA_49	M36	N30	DDR_SELLO_0
DDR_DATA_50	L35	T32	DDR_SELLO_1
DDR_DATA_51	M35		
DDR_DATA_52	M33	Y32	DDR_MCLK_0_P
DDR_DATA_53	L36	Y33	DDR_MCLK_0_N
DDR_DATA_54	N33	Y35	DDR_MCLK_1_P
DDR_DATA_55	M30	Y36	DDR_MCLK_1_N
DDR_DATA_56	J32	Y30	DDR_MCLK_2_P
DDR_DATA_57	J33	W30	DDR_MCLK_2_N
DDR_DATA_58	J35	W32	DDR_MCLK_3_P
DDR_DATA_59	K32	W33	DDR_MCLK_3_N
DDR_DATA_60	K33	V33	DDR_MCLK_4_P
DDR_DATA_61	J36	V32	DDR_MCLK_4_N
DDR_DATA_62	K36	W35	DDR_MCLK_5_P
DDR_DATA_63	K35	W36	DDR_MCLK_5_N
		AA22	DDR_REF
		Y22	DDR_VREF_0
		T22	DDR_VREF_1

‘0’ & ‘1’ GO TO SLOT A
‘2’ & ‘3’ GO TO SLOT B

‘0’ & ‘1’ GO TO SLOT A
‘2’ & ‘3’ GO TO SLOT B

‘0’S ARE SAME POLARITY (ACTIVE-LO)
‘1’S ARE SAME POLARITY (ACTIVE-HI)

INT_MEM_REF_H
INT_MEM_VREF

R199 1K 1% 1/16W MF 402

MEM_VREF

+2_5V_INTREPID
R198 10K 1% 1/16W MF 402
R191 10K 1% 1/16W MF 402
C245 0.1UF 20% 10V CERM 402
INT_MEM_VREF

CLOCKS

SYSCLK_DDRCLK_A1_UF	RP33 22	SYSCLK_DDRCLK_A1
SYSCLK_DDRCLK_A1_L_UF	RP33 22	SYSCLK_DDRCLK_A1_L
SYSCLK_DDRCLK_A0_UF	RP34 22	SYSCLK_DDRCLK_A0
SYSCLK_DDRCLK_A0_L_UF	RP34 22	SYSCLK_DDRCLK_A0_L
SYSCLK_DDRCLK_B1_UF	RP33 22	SYSCLK_DDRCLK_B1
SYSCLK_DDRCLK_B1_L_UF	RP33 22	SYSCLK_DDRCLK_B1_L
SYSCLK_DDRCLK_B0_UF	RP34 22	SYSCLK_DDRCLK_B0
SYSCLK_DDRCLK_B0_L_UF	RP34 22	SYSCLK_DDRCLK_B0_L

CS

MEM_CS_L<0>	RP36 22	RAM_CS_L<0>
MEM_CS_L<1>	RP36 22	RAM_CS_L<1>
MEM_CS_L<2>	RP35 22	RAM_CS_L<2>
MEM_CS_L<3>	RP35 22	RAM_CS_L<3>

CKE

MEM_CKE<0>	RP36 22	RAM_CKE<0>
MEM_CKE<1>	RP36 22	RAM_CKE<1>
MEM_CKE<2>	RP35 22	RAM_CKE<2>
MEM_CKE<3>	RP35 22	RAM_CKE<3>

ADDR

MEM_ADDR<0>	RP31 22	RAM_ADDR<0>
MEM_ADDR<1>	RP25 22	RAM_ADDR<1>
MEM_ADDR<2>	RP25 22	RAM_ADDR<2>
MEM_ADDR<3>	RP25 22	RAM_ADDR<3>
MEM_ADDR<4>	RP30 22	RAM_ADDR<4>
MEM_ADDR<5>	RP30 22	RAM_ADDR<5>
MEM_ADDR<6>	RP31 22	RAM_ADDR<6>
MEM_ADDR<7>	RP30 22	RAM_ADDR<7>
MEM_ADDR<8>	RP31 22	RAM_ADDR<8>
MEM_ADDR<9>	RP31 22	RAM_ADDR<9>
MEM_ADDR<10>	RP26 22	RAM_ADDR<10>
MEM_ADDR<11>	RP30 22	RAM_ADDR<11>
MEM_ADDR<12>	RP26 22	RAM_ADDR<12>

BA

MEM_BA<0>	RP26 22	RAM_BA<0>
MEM_BA<1>	RP26 22	RAM_BA<1>

CNTL

MEM_WE_L	RP26 22	RAM_WE_L
MEM_CAS_L	R250 22	RAM_CAS_L
MEM_RAS_L	R238 22	RAM_RAS_L

All: 5% 1/16W SM1

1MB BOOT ROM

+3V_MAIN
C460 2.2UF 20% 10V CERM 805
C470 0.1UF 20% 10V CERM 402
C479 0.1UF 20% 10V CERM 402

U17
3.3V TSOP OMIT
VPP, VCC

PCI_AD<0>	21	A0	DQ0
PCI_AD<1>	20	A1	DQ1
PCI_AD<2>	19	A2	DQ2
PCI_AD<3>	18	A3	DQ3
PCI_AD<4>	17	A4	DQ4
PCI_AD<5>	16	A5	DQ5
PCI_AD<6>	15	A6	DQ6
PCI_AD<7>	14	A7	DQ7
PCI_AD<8>	8	A8	
PCI_AD<9>	7	A9	
PCI_AD<10>	36	A10	
PCI_AD<11>	6	A11	
PCI_AD<12>	5	A12	
PCI_AD<13>	4	A13	
PCI_AD<14>	3	A14	
PCI_AD<15>	2	A15	
PCI_AD<16>	1	A16	
PCI_AD<17>	40	A17	
PCI_AD<18>	13	A18	
PCI_AD<19>	37	A19	
PCI_AD<20>	38	A20	
ROM_ONBOARD_CS_L	22	CE	
ROM_OE_L	24	OE	
ROM_RW_L	9	WE	
ROM_WP_L	12	WP	
INT_RESET_L	10	PWD	
	23, 39	GND	

PCI_AD<24>	25		
PCI_AD<25>	26		
PCI_AD<26>	27		
PCI_AD<27>	28		
PCI_AD<28>	32		
PCI_AD<29>	33		
PCI_AD<30>	34		
PCI_AD<31>	35		

+3V_MAIN
R338 10K 5% 1/16W MF 402
R386 10K 5% 1/16W MF 402
R357 1K 5% 1/16W MF 402
ROM_CS_L

OVERRIDE ROM MODULE
INTERCEPTS ROM CHIP SELECT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1465	1	BOOTROM,FINAL,Q41A	U17	CRITICAL	?

PULL-DOWN RESISTORS TO ENSURE
CKE STAYS LOW AFTER INTREPID
2.5V I/O SHUTS OFF

RAM_CKE<0>
RAM_CKE<1>
RAM_CKE<2>
RAM_CKE<3>
R500 10K 5% 1/16W MF 402
R439 10K 5% 1/16W MF 402
R409 10K 5% 1/16W MF 402
R387 10K 5% 1/16W MF 402

INT - DDR/BOOTROM

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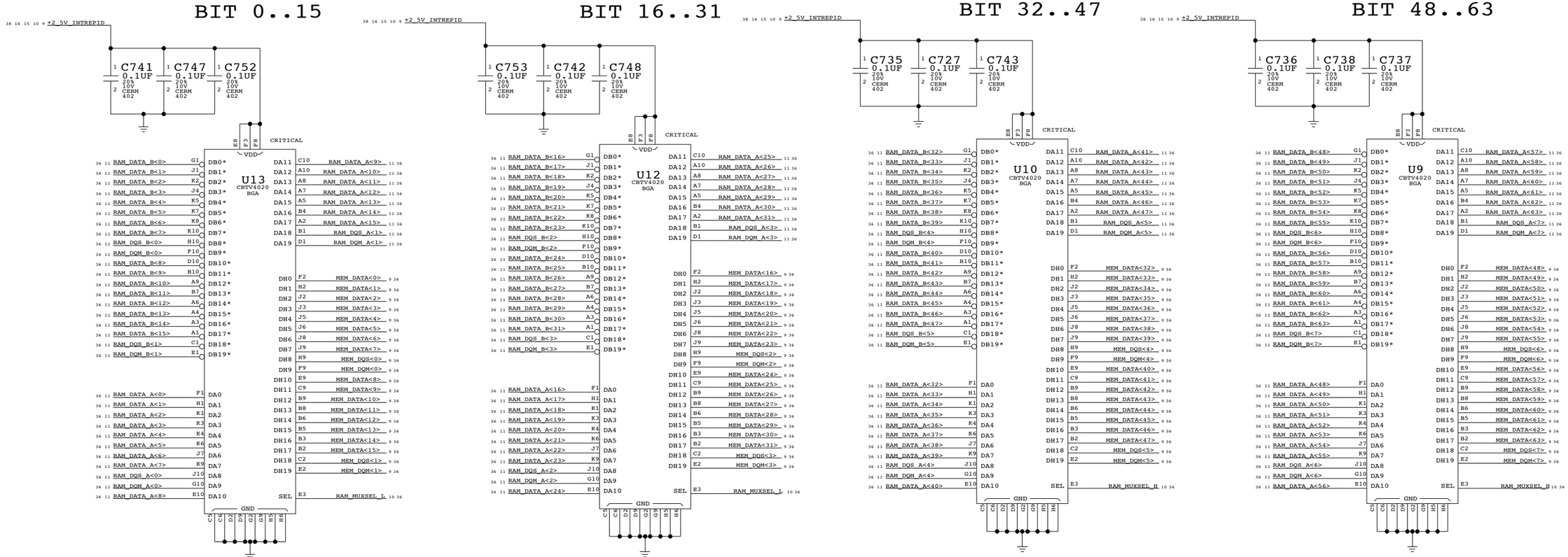

SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND
MEM_MUXSEL_H<0> AND MEM_MUXSEL_L<0> ARE ACTIVE LOW
MEM_MUXSEL_H<1> AND MEM_MUXSEL_L<1> ARE ACTIVE HIGH

ADDED 0 OHM RESISTORS IN CASE POLARITY IS WRONG

16BIT 2:1 DDR MUXES

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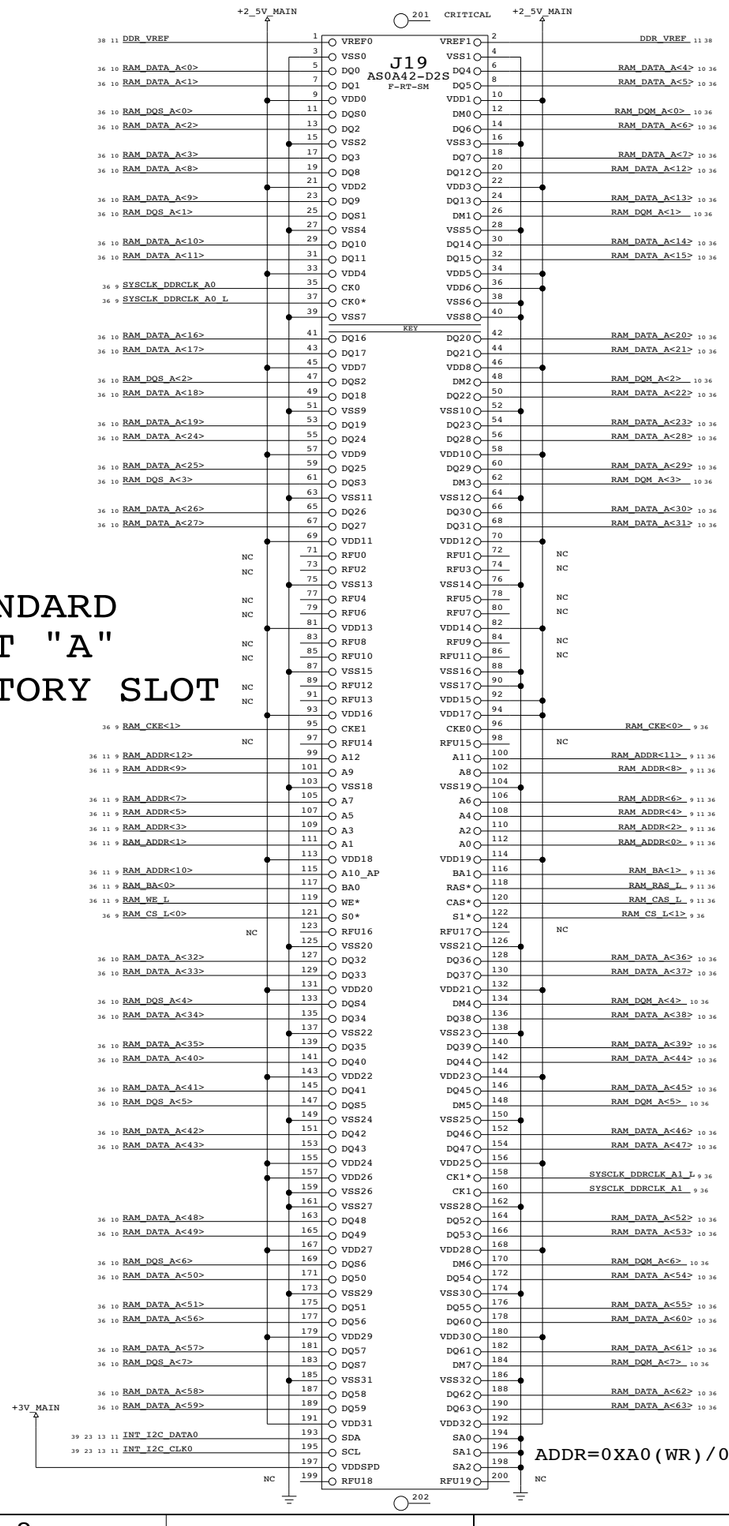
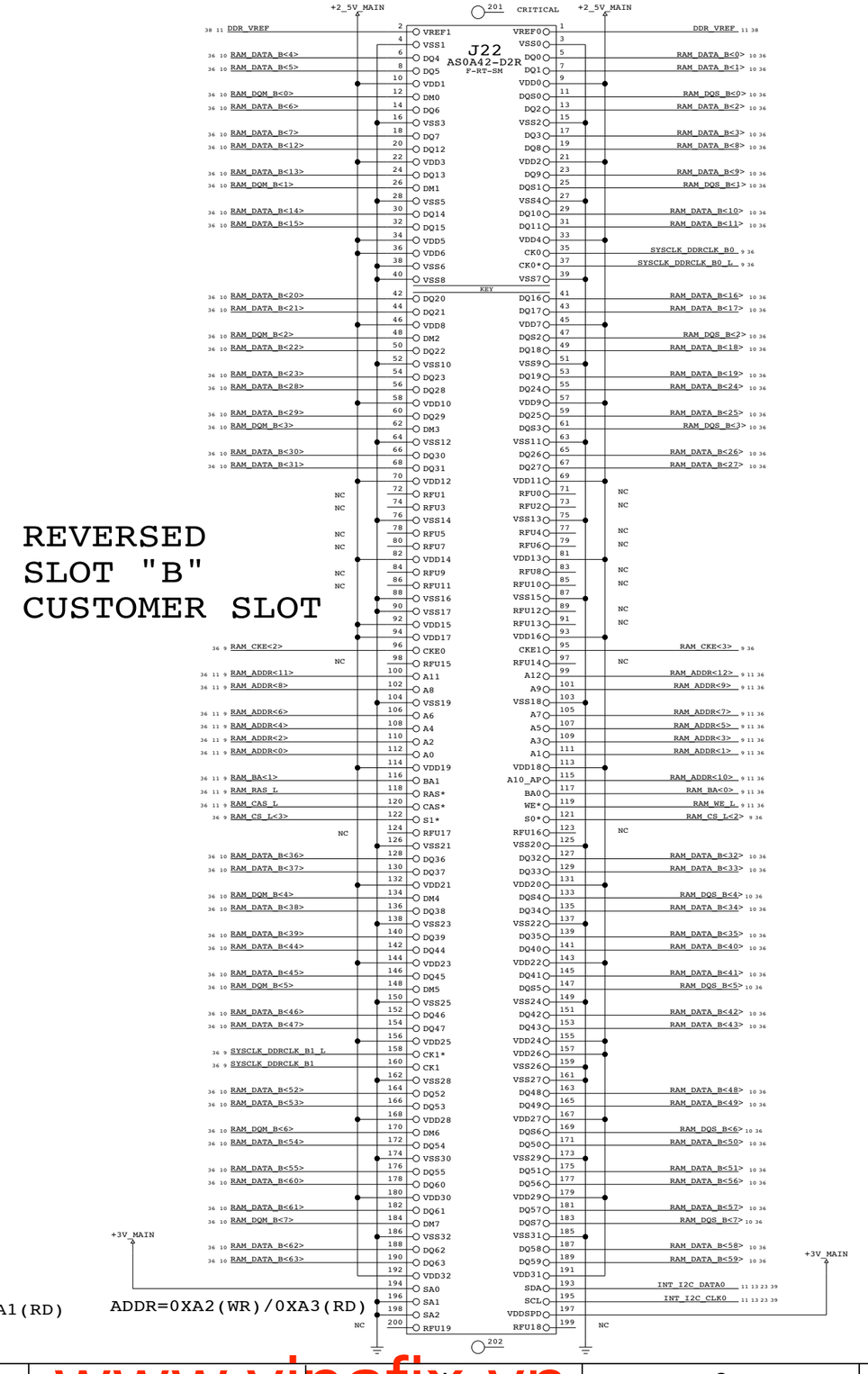
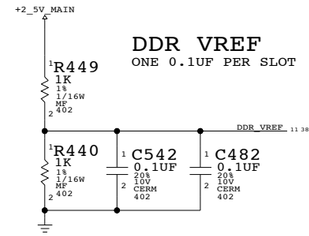
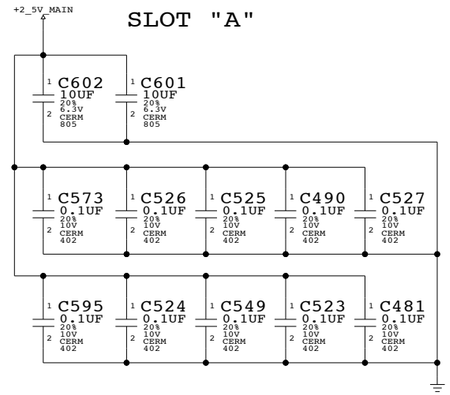


STANDARD
SLOT "A"
FACTORY SLOT



REVERSED
SLOT "B"
CUSTOMER SLOT





DDR SODIMM CONNS

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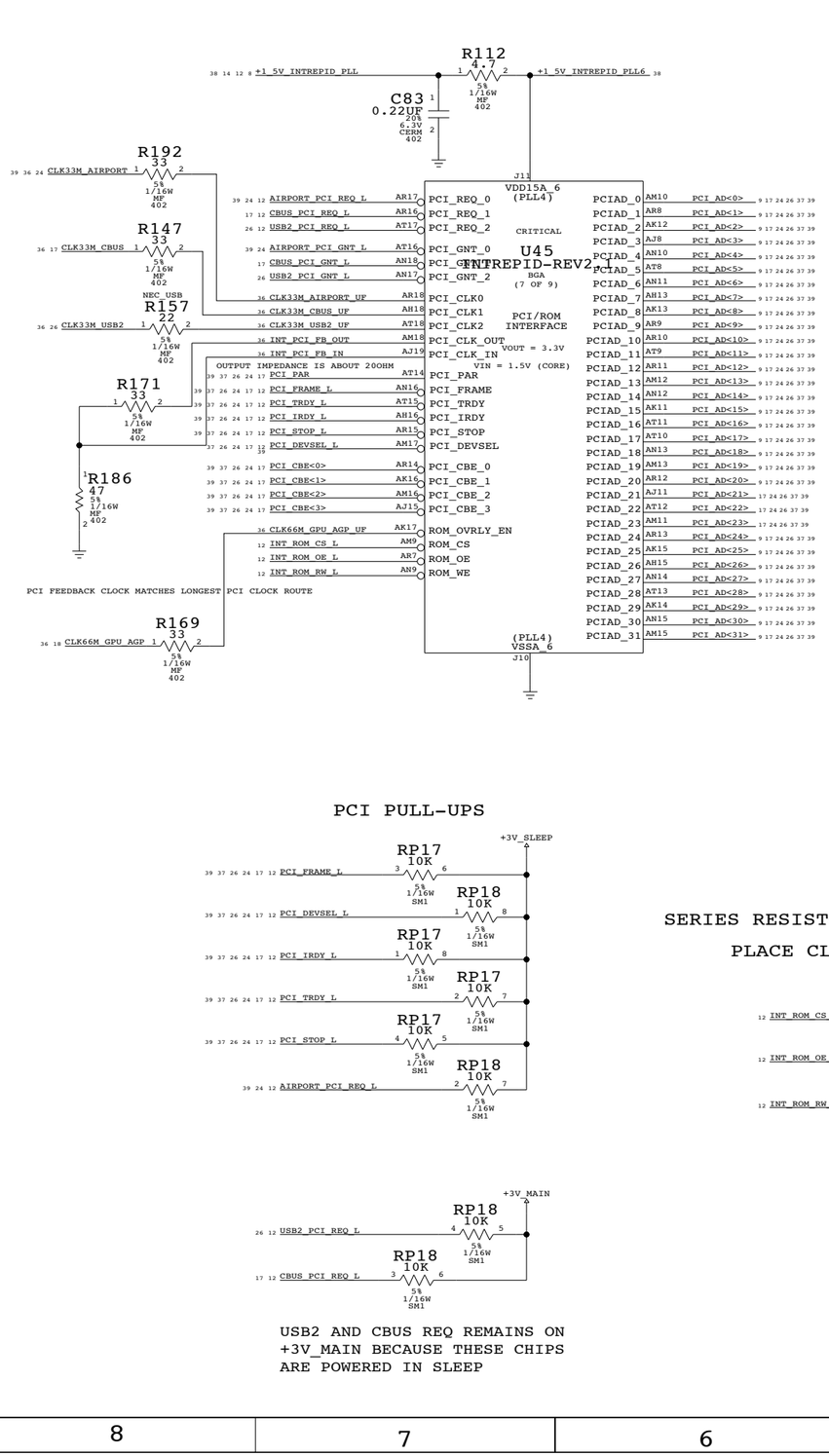

INTREPID AGP/PCI

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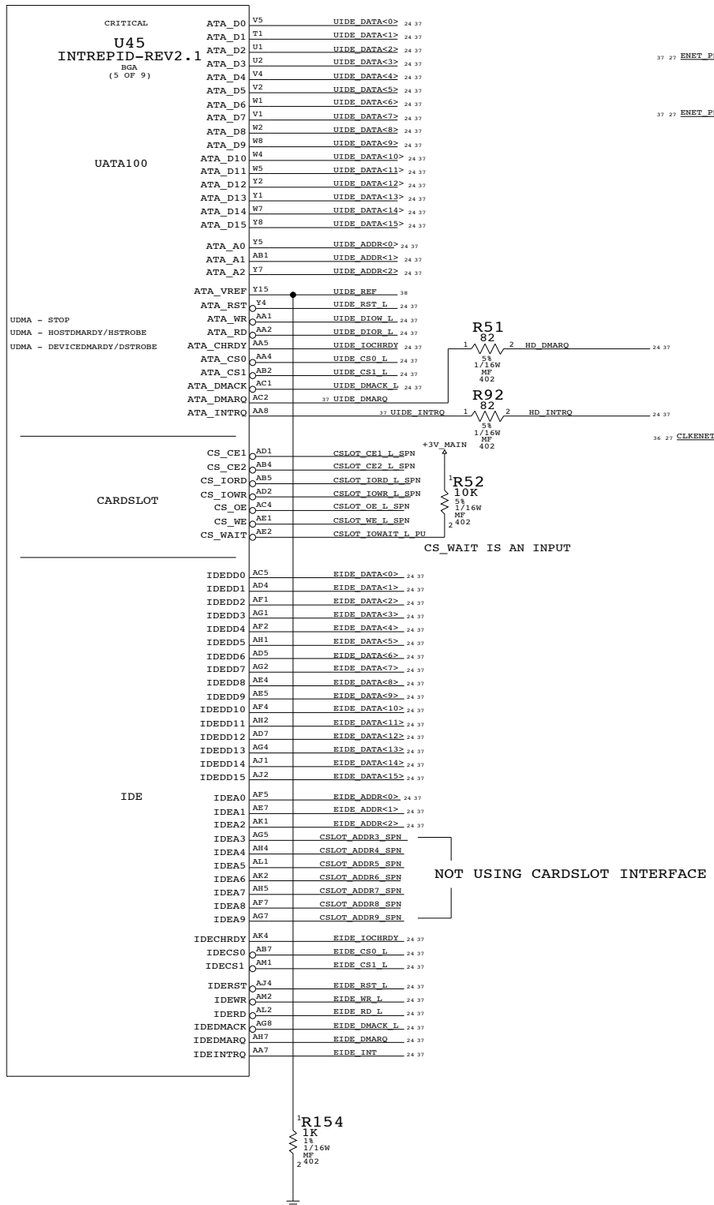
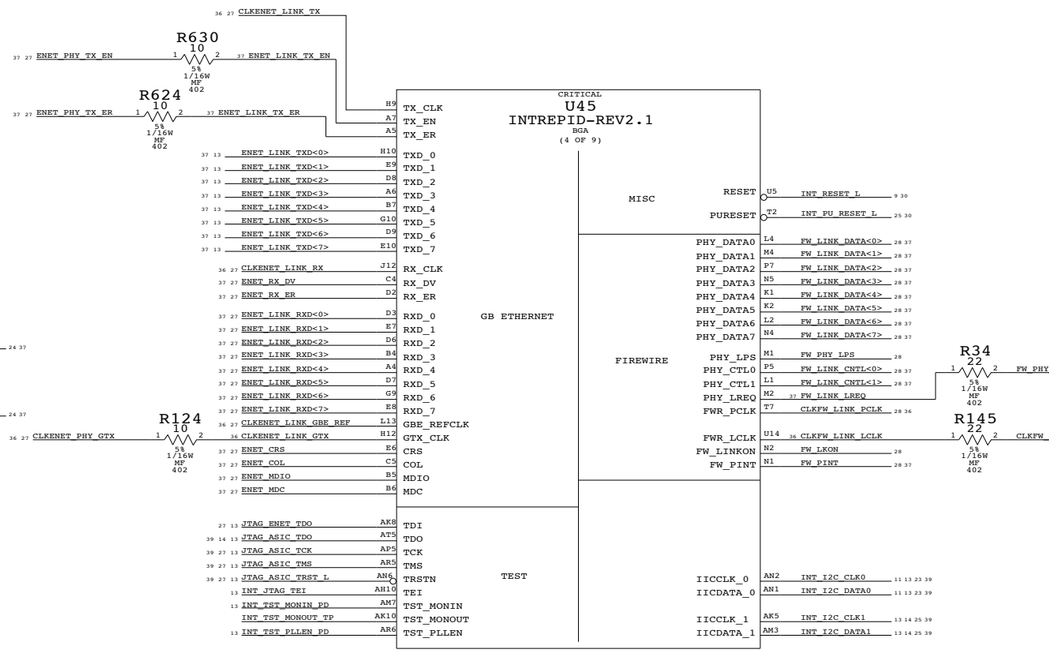
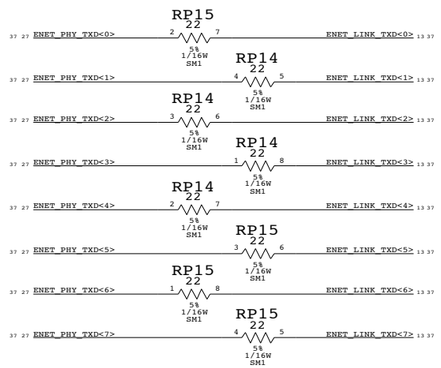
SHT 12 OF 44



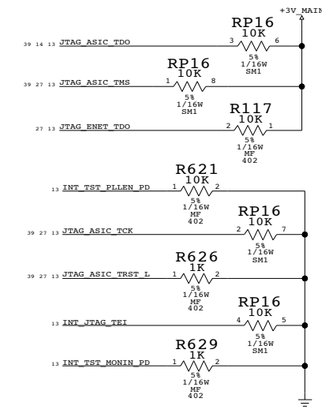


ENET_TXD SERIES TERMINATION

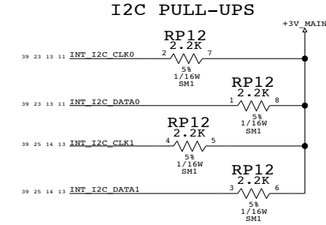


JTG_RSTN_L	TST_TEI_H	JTG_TDO_H (I/O)	JTG_TDI_H (I/O)	TST_PLLEN_H	ANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	EXTPLL SHUTDOWN (OUTPUT)	DDR_ TPDENABLE (OUTPUT)	0	(OUTPUT)	NORMAL OPERATION
0	0	(OUTPUT)	0(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	HWPLL_ TESTSEL5 (INPUT)	1(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0(I)	0(I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0(I)	1(I)	0	X(I)	ATPG IDDQ
0	1	0(I)	1(I)	1	X(I)	TEST TRI-STATE
0	1	1(I)	0(I)	0	X(I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1(I)	0(I)	1	X(I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1(I)	1(I)	X	X(I)	FUNCTIONAL TEST IDDQ

TEST PULL-UPS/DOWNS



I2C PULL-UPS



BUS / ADDR	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
A0-WR A1-RD	RAM - STANDARD J20 - PG 12	N/A	N/A	N/A
A2-WR A3-RD	RAM - REVERSED J23 - PG 12	N/A	N/A	N/A
AC-WR AD-RD	N/A	N/A	DASH MODEM J9 - PG 25	N/A
AE-WR AF-RD	BOOTBANG E2PROM U37 - PG 23	N/A	N/A	N/A
84-WR 85-RD	LMU U36 - PG 23	N/A	N/A	N/A
58-WR 59-RD	N/A	FAN CONTROLLER U3 - PG 24	N/A	N/A
6A-WR 6B-RD	N/A	N/A	SNAPPER SOUND J12 - PG 24	N/A
D0-WR D1-RD	N/A	CLOCK SLEW SSCG U56 - PG 15	N/A	N/A

ADDR LSB INDICATES READ ('1') OR WRITE ('0') MODES

INT - ENET/FW/UATA EIDE/I2C

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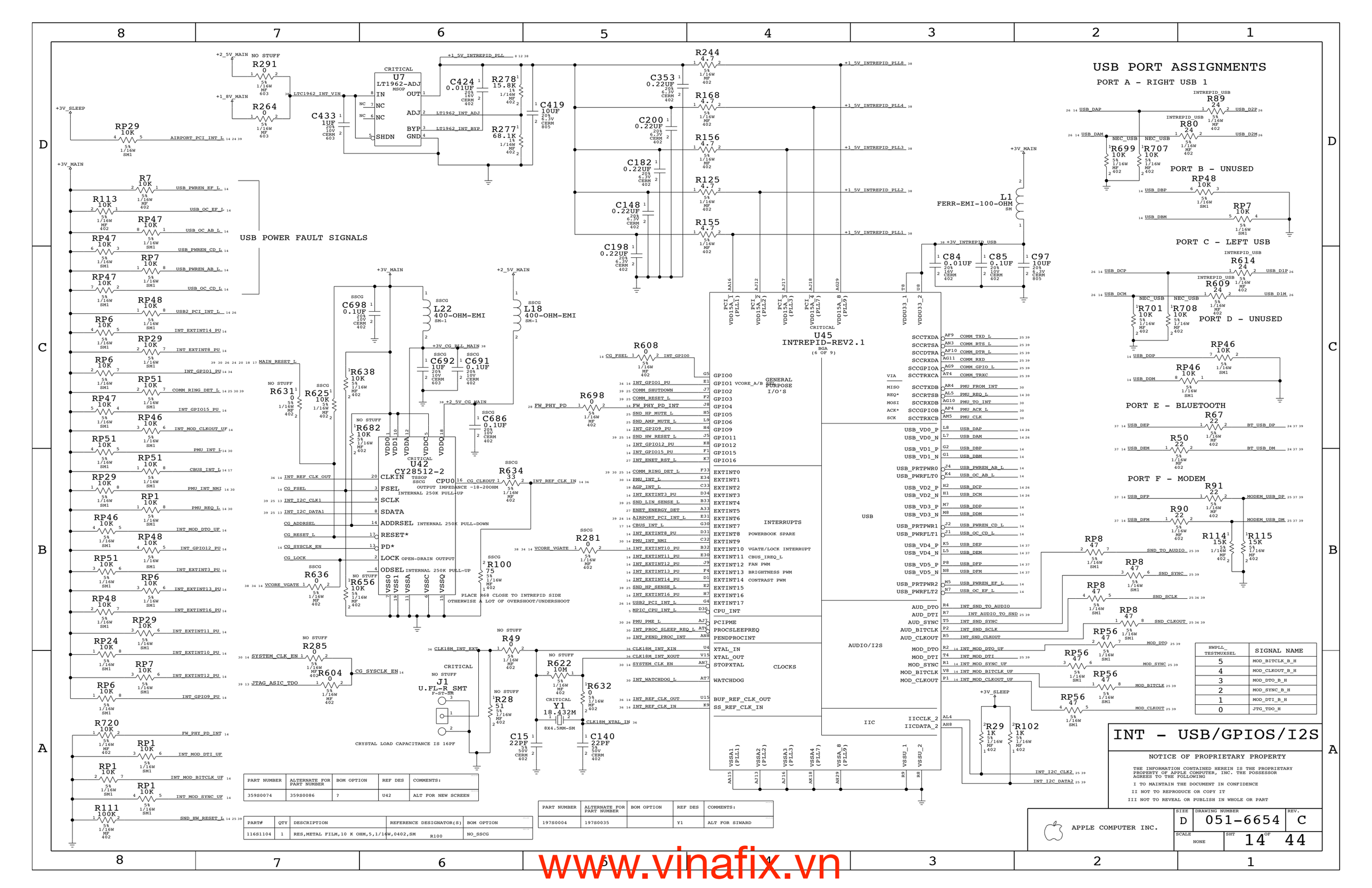
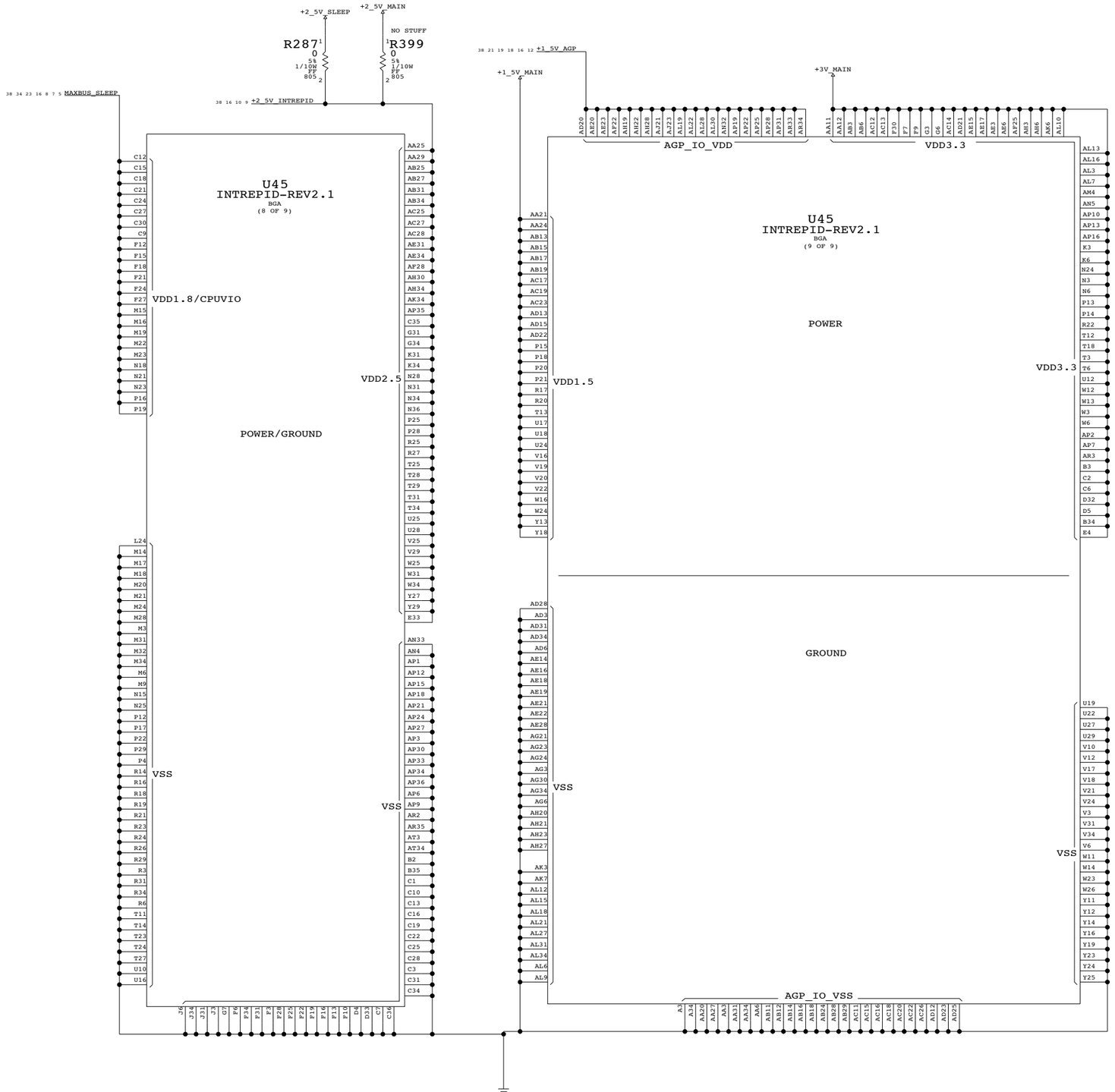


HWPLL_TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
359S0074	359S0086	?	U42	ALT FOR NEW SCREEN

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0004	197S0035		Y1	ALT FOR SIWARD

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES,METAL FILM,10 K OHM,5,1/16W,0402,SM	R100	NO_SSCG



Intrepid Power

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INTREPID MAXBUS DECOUPLING

24 Balls
4 X 10UF (0805)
32 X 0.22UF (0402)

23 15 8 7 5 38 34 MAXBUS_SLEEP

C204 10uF 20% 6.3V CERM 805 · C348 10uF 20% 6.3V CERM 805 · C236 10uF 20% 6.3V CERM 805 · C196 10uF 20% 6.3V CERM 805

C239 C240 C350 C312 C176 C288 C313 C94 C286 C158 — 0.22uF 20% 6.3V CERM 402

C174 C206 C259 C237 C238 C95 C117 C241 C260 C314 — 0.22uF 20% 6.3V CERM 402

C173 C171 C175 C226 C172 C207 C118 C287 C119 C349 — 0.22uF 20% 6.3V CERM 402

C205 C209 — 0.22uF 20% 6.3V CERM 402

INTREPID AGP I/O DECOUPLING

21 Balls
4 X 10UF (0805)
24 X 0.22UF (0402)

38 21 19 18 15 12 +1_5V_AGP

C371 10uF 20% 6.3V CERM 805 · C231 10uF 20% 6.3V CERM 805 · C281 10uF 20% 6.3V CERM 805 · C394 10uF 20% 6.3V CERM 805

C356 C297 C268 C217 C355 C267 C250 C298 C377 C216 — 0.22uF 20% 6.3V CERM 402

C228 C230 C265 C378 C357 C229 C325 C393 C324 C323 — 0.22uF 20% 6.3V CERM 402

C251 C266 C249 — 0.22uF 20% 6.3V CERM 402

INTREPID DDR DECOUPLING

44 Balls
4 X 10UF (0805)
51 X 0.22UF (0402)

38 15 10 9 +2_5V_INTREPID

C422 10uF 20% 6.3V CERM 805 · C417 10uF 20% 6.3V CERM 805 · C418 10uF 20% 6.3V CERM 805 · C423 10uF 20% 6.3V CERM 805

C407 C391 C310 C317 C480 C390 C370 C320 C365 C366 — 0.22uF 20% 6.3V CERM 402

C367 C292 C295 C403 C291 C352 C322 C392 C385 C376 — 0.22uF 20% 6.3V CERM 402

C321 C318 C399 C410 C335 C369 C384 C294 C406 C405 — 0.22uF 20% 6.3V CERM 402

C404 C400 C386 C289 C387 C401 C354 C389 C309 C398 — 0.22uF 20% 6.3V CERM 402

C337 C290 C402 C397 C368 C334 C388 C293 C319 C336 — 0.22uF 20% 6.3V CERM 402

C316 — 0.22uF 20% 6.3V CERM 402

INTREPID CORE DECOUPLING

30 Balls
4 X 10UF (0805)
29 X 0.22UF (0402)

+1_5V_MAIN

C128 10uF 20% 6.3V CERM 805 · C101 10uF 20% 6.3V CERM 805 · C157 10uF 20% 6.3V CERM 805 · C315 10uF 20% 6.3V CERM 805

C147 C243 C262 C242 C227 C181 C142 C215 C278 C264 — 0.22uF 20% 6.3V CERM 402

C244 C212 C178 C179 C177 C159 C161 C162 C280 C279 — 0.22uF 20% 6.3V CERM 402

C144 C246 C211 C263 C180 C213 C197 C208 C214 — 0.22uF 20% 6.3V CERM 402

INTREPID 3.3V DECOUPLING

57 Balls
4 X 10UF (0805)
72 X 0.22UF (0402)

+3V_MAIN

C164 10uF 20% 6.3V CERM 805 · C395 10uF 20% 6.3V CERM 805 · C10 10uF 20% 6.3V CERM 805 · C9 10uF 20% 6.3V CERM 805

C375 C351 C53 C42 C21 C185 C31 C143 C123 C121 — 0.22uF 20% 6.3V CERM 402

C33 C184 C43 C35 C261 C60 C52 C199 C57 C19 — 0.22uF 20% 6.3V CERM 402

C16 C108 C55 C32 C125 C45 C76 C277 C28 C26 — 0.22uF 20% 6.3V CERM 402

C34 C23 C120 C146 C141 C30 C145 C96 C54 C50 — 0.22uF 20% 6.3V CERM 402

C75 C122 C51 C59 C163 C126 C98 C109 C56 C27 — 0.22uF 20% 6.3V CERM 402

C296 C248 C210 C58 C22 C20 C61 C44 C29 C24 — 0.22uF 20% 6.3V CERM 402

C183 C18 C49 C36 C17 C99 C396 C124 C127 C100 — 0.22uF 20% 6.3V CERM 402

Intrepid Decoupling

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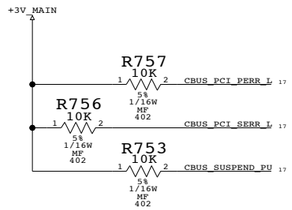
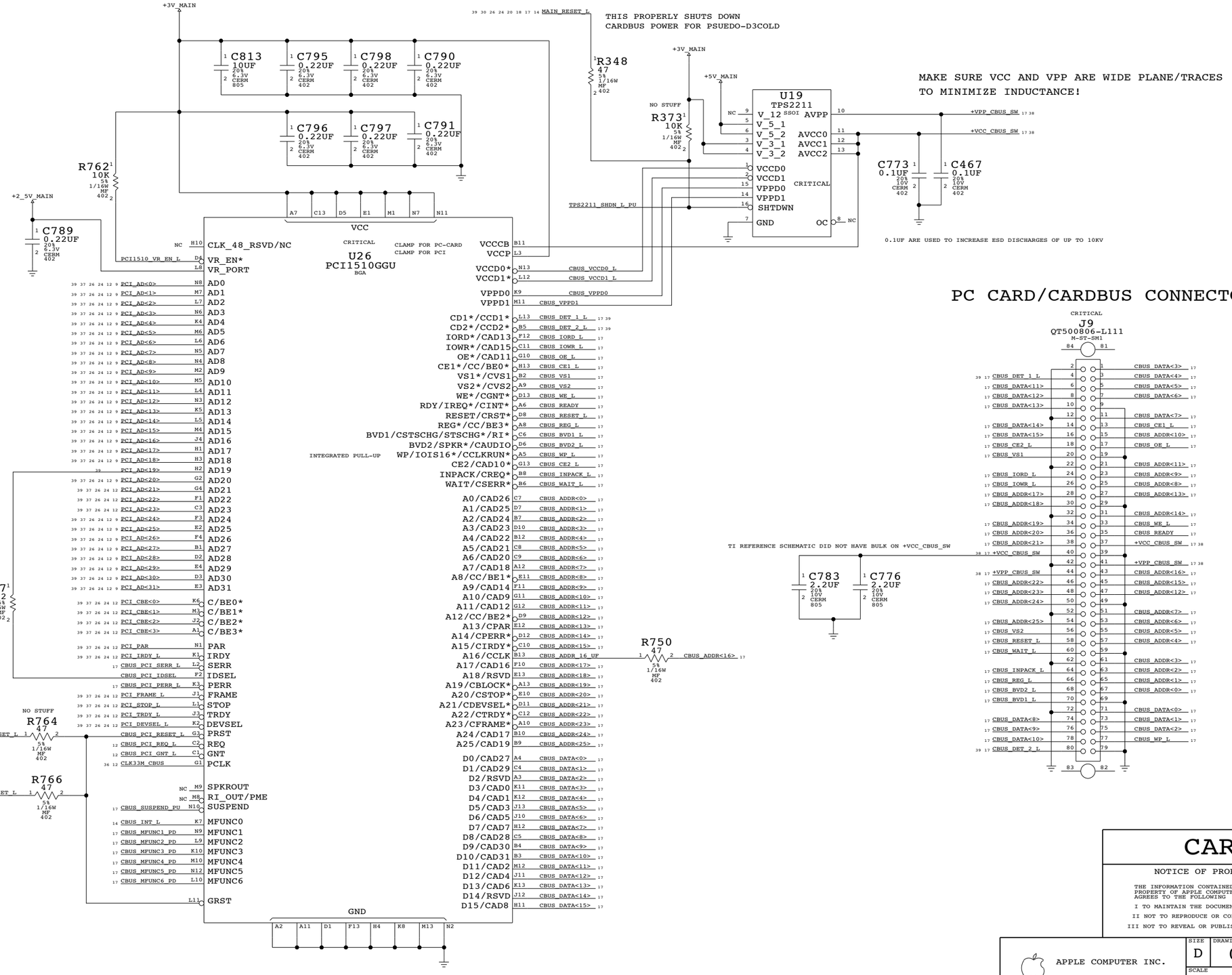
NONE	16 44

PCI1510 PULL-UPS





PC CARD/CARDBUS CONNECTOR

CARDBUS

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D	051-6654	C
SCALE: NONE	SHT 17 OF 44	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0158	1	IC,ATI,M11-CSP128,GRPHCTLR,667BGA	U44	CRITICAL	M11_CSP128
338S0154	1	IC,ATI,M11-CSP64,GRPHSCTLR,667BGA	U44	CRITICAL	M11_CSP64

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0182	338S0158	M11_CSP128	U44	ALT FOR A16
338S0183	338S0154	M11_CSP64	U44	ALT FOR A16

U44
RAGE_MOBILITY
M11-CSP64
64MB
BGA
(1 OF 6)

AGP_AD<31> AB30 AD31
AGP_AD<30> AB27 AD30
AGP_AD<29> AA29 AD29
AGP_AD<28> AB28 AD28
AGP_AD<27> AA30 AD27
AGP_AD<26> AA27 AD26
AGP_AD<25> Y30 AD25
AGP_AD<24> AA28 AD24
AGP_AD<23> W30 AD23
AGP_AD<22> W27 AD22
AGP_AD<21> V30 AD21
AGP_AD<20> V28 AD20
AGP_AD<19> V29 AD19
AGP_AD<18> V27 AD18
AGP_AD<17> U30 AD17
AGP_AD<16> U28 AD16
AGP_AD<15> R27 AD15
AGP_AD<14> R29 AD14
AGP_AD<13> P28 AD13
AGP_AD<12> P30 AD12
AGP_AD<11> P27 AD11
AGP_AD<10> P29 AD10
AGP_AD<9> N28 AD9
AGP_AD<8> N30 AD8
AGP_AD<7> M30 AD7
AGP_AD<6> M27 AD6
AGP_AD<5> M29 AD5
AGP_AD<4> L28 AD4
AGP_AD<3> L30 AD3
AGP_AD<2> L27 AD2
AGP_AD<1> L29 AD1
AGP_AD<0> K28 AD0

AGP_CBE<3> W28 CBEB3
AGP_CBE<2> U29 CBEB2
AGP_CBE<1> R30 CBEB1
AGP_CBE<0> N27 CBEB0

CLK66M_GPU_AGP AG30 PCICLK
AGP_FRAME_L U27 FRAMEB
AGP_IRDY_L T30 IRDYB
AGP_TRDY_L T28 TRDYB
AGP_STOP_L T27 STOPB
AGP_DEVSEL_L T29 DEVSELB
AGP_PAR R28 PAR
AGP_REQ_L AF29 REQB
AGP_GNT_L AF27 GNTB
AGP_INT_L AH29 INTAB
AGP_ATI_RESET_L AH30 RSTB
AGP_WBF_L AE27 WBF
AGP_ATI_VREFG AK30 VREFG
AGP_ATI_VREF D8 MVREF

AD_STB0 N29 AGP_AD_STB<0>
AD_STB1 W29 AGP_AD_STB<1>
AD_STBB0 M28 AGP_AD_STB_L<0>
AD_STBB1 Y29 AGP_AD_STB_L<1>
AGP_BUSYB AG28 AGP_BUSY_L
AGPREF K30
AGPTEST K29 GPU_AGP_TEST
AGP8X_DETB U25 AGP8X_DET_PU
SUS_STAT AJ28 AGP_SUS_STAT_L_PU
ST0 AF30 AGP_ST<0>
ST1 AF28 AGP_ST<1>
ST2 AE29 AGP_ST<2>
SBA7 AC28 AGP_SBA<7>
SBA6 AB29 AGP_SBA<6>
SBA5 AC27 AGP_SBA<5>
SBA4 AC30 AGP_SBA<4>
SBA3 AD27 AGP_SBA<3>
SBA2 AD30 AGP_SBA<2>
SBA1 AE28 AGP_SBA<1>
SBA0 AD29 AGP_SBA<0>
RBFB AE30 AGP_RBF_L
STP_AGPB AG29 AGP_STP_L
SB_STB AC29 AGP_SB_STB
SB_STBS AD28 AGP_SB_STB_L
RSTB_MSK AD24 ATI_RSTB_MSK
DBI_LO Y25 ATI_DBI_LO_PU
DBI_HI Y27 ATI_DBI_HI_PU

OMIT

38 21 19 18 12 +3V_GPU
38 21 19 18 16 15 12 +1_5V_AGP
R119 47 5% 1/16W MF 402
R127 10K 5% 1/16W MF 402
R159 20K 5% 1/16W MF 402
INT_AGP_VREF 12 38
C62 0.1uF 20% 10V CERM 402
C63 0.01uF 20% 16V CERM 402
(PLACE C1002 CLOSE TO AGPREF PIN)
38 21 19 18 12 +3V_GPU
R172 20K 5% 1/16W MF 402
R158 0 5% 1/16W MF 402
38 21 19 18 12 +3V_GPU
MAIN_RESET_L IS TOGGLED FOR SLEEP
R54 10K 5% 1/16W MF 402
R53 47 5% 1/16W MF 402
24 20 17 14 39 30 26 MAIN_RESET_L
21 19 18 12 38 +3V_GPU
R43 1K 1% 1/16W MF 402
R44 1K 38 21 16 +GPU_MEM
R45 1K 1% 1/16W MF 402
R46 1K 1% 1/16W MF 402
PLACE VERF VOLTAGE DIVIDER CLOSE TO ATI M10 VREF PIN
C11 0.1uF 20% 10V CERM 402
C37 10uF 20% 6.3V CERM 805
38 21 19 18 12 +3V_GPU
38 21 19 18 16 15 12 +1_5V_AGP
R126 47K 5% 1/16W MF 402
R138 47K 5% 1/16W MF 402
38 21 20 19 +1_8V_GPU
ATI_MEMIO_LO R55 4.7K 5% 1/16W MF 402
ATI_MEMIO_HI R104 4.7K 5% 1/16W MF 402
ATI_MEMIO_HI R70 4.7K 5% 1/16W MF 402
ATI_MEMIO_LO R105 4.7K 5% 1/16W MF 402
ATI_MEMVMODE0 MEMVMODE0
ATI_MEMVMODE1 MEMVMODE1
FOR 2.5 VDDR1
MEMVMODE0=1.8V
MEMVMODE1=GND
FOR 1.8 VDDR1
MEMVMODE0=GND
MEMVMODE1=1.8V
TEST_VCLK E8
TEST_MLCK J6
MEMTEST C8 ATI_MEMTEST
PLLTEST AC22 NC
D+ AC10 GPU_THERM_DP_TP
D- AC11 GPU_THERM_DM_TP
+GPU_MEM 18 21 38
(PULL-UP to GPU_MEM_IO)
R118 45.3 1% 1/16W MF 402
39 38 19 GPU_VCORE
L2 60-OHM-EMI SM
38 GPU_VCORE_VDDCI
C64 0.01uF 20% 16V CERM 402
C67 10uF 20% 6.3V CERM 805
C65 0.01uF 20% 16V CERM 402
C68 0.01uF 20% 16V CERM 402
C66 0.01uF 20% 16V CERM 402
C69 0.01uF 20% 16V CERM 402

U44
RAGE_MOBILITY
M11-CSP64
64MB
BGA
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OMIT

M2 P3 A21 B19 M15 N15 P15 R15 T15 T12 T13 T14 W16 V16 U16 T16 R16 R17 R18 R19 U6 AE15 F18 P25 VSS VDDCI

U44
RAGE_MOBILITY
M11-CSP64
64MB
BGA
(2 OF 6)

OMIT

B26 A26 B25 A25 C22 D21 C21 D20 C20 D22 C23 D23 A27 B27 H2 H1 J2 J1 K4 K3 L4 M3 L3 M4 N2 N1 N4 N3 G30 G28 B30 D26 D16 B15 D11 B10 D5 B3 G3 E1 U1 V3 AB1 AC3 J30 J29 H30 H29 F30 F29 E30 E29 J28 J27 H28 H27 F28 F27 E28 E27 D30 D29 C30 C29 A30 A29 A28 B28 D28 C28 D27 C27 D25 C25 D24 C24 D18 C18 D17 C17 D15 C15 D14 C14 B17 VSS

A17 B16 A16 B14 A14 B13 A13 D13 C13 D12 C12 D10 C10 D9 C9 B12 A12 B11 A11 B9 A9 B8 A8 C7 D7 C6 D6 C4 D4 C3 D3 A5 B5 A4 B4 A2 B2 A1 B1 E4 E3 F3 F4 H3 H4 J3 J4 C1 C2 D1 D2 F1 F2 G1 G2 R1 R2 T1 T2 V1 V2 W1 W2 T3 T4 U3 U4 W3 W4 Y3 Y4 Y1 Y2 AA1 AA2 AC1 AC2 AD1 AD2 AA3 AA4 AB3 AB4 AD3 AD4 AE3 AE4 VSS

27M OSC

(PLACE THE OSCILLATOR AND R189 AND R195 CLOSE TO ATI PIN AJ29)

+3V_SLEEP
L4 FERR-EMI-100-OHM SM
38 +3V_ATI_OSC_SLEEP
C77 0.1uF 20% 10V CERM 402
C78 4.7uF 20% 6.3V CERM 805
NO STUFF
R188 100K 5% 1/16W MF 402
CRITICAL
G2 27.0000M OSC SM-1
VCC OE OUT GND
ATI_OSC_OE
ATI_CLK27M_OSC
(PLACE R200 CLOSE TO OSC)
GPU_SS
R200 0 5% 1/16W MF 402
ATI_CLK27M_OSC_SS 18
R189 287 1% 1/16W MF 402
ATI_CLK27M_IN 19
R195 162 1% 1/16W MF 402

S0=1;S1=M => -1.5% DOWN-SPREAD
SPREAD SPECTRUM SUPPORT

+3V_SLEEP
GPU_SS
L3 FERR-EMI-100-OHM SM
38 +3V_ATI_SS
GPU_SS C70 10uF 20% 6.3V CERM 805
GPU_SS C71 0.1uF 20% 10V CERM 402
NO STUFF
R173 0 5% 1/16W MF 402
GPU_SS
R181 0 5% 1/16W MF 402
ATI_CLK27M_OSC_SS 18
GPU_SS 7 CRITICAL
VDD
U47
CY25811
SOT
XIN/CLKIN
XOUT SSCLK
NC NC FRSEL S1 S0 VSS
ATI_SSCLK_UF
GPU_SS
R201 33 5% 1/16W MF 402
ATI_SSCLK_IN 19
CY25811_S1
CY25811_S0
NO STUFF
R37 0 5% 1/16W MF 402
NO STUFF
R38 0 5% 1/16W MF 402

M10 AGP INTERFACE

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SIZE	DRAWING NUMBER	REV.
D	051-6654	C
SCALE: NONE	SHT 18 OF 44	

TMDS TERMINATION

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN
CMF LINE SHOULD BE ROUTED AS 4MIL SURFACE
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS

EXT_TMDS R228 10K 5% 1/16W MF 402 — +1_8V_GPU
INT_TMDS R234 10K 5% 1/16W MF 402 — +3V_GPU
ZV_LCDDATA20_PU

R223 NO STUFF 10K 5% 1/16W MF 402 — +3V_GPU
R221 1K 5% 1/16W MF 402
ATI_GPIO7_SPN (NO ICT TEST)
ATI_GPIO8_RD (NO ICT TEST)
ATI_GPIO9_SPN (NO ICT TEST)
ATI_GPIO10_SPN (NO ICT TEST)
ATI_GPIO11_SPN (NO ICT TEST)
ATI_GPIO12_SPN (NO ICT TEST)
ATI_GPIO13_SPN
HPD_PWR_SNS_EN
GPU_VCORE_CNTL_L

R229 1K 5% 1/16W MF 402 — ATI_TESTEN

U44 RAGE_MOBILITY M11-CSP64 64MB BGA (3 OF 6)

OMIT

GPU_DVOD<0>	AJ5	ZV_LCDDATA0
GPU_DVOD<1>	AK5	ZV_LCDDATA1
GPU_DVOD<2>	AG6	ZV_LCDDATA2
GPU_DVOD<3>	AH6	ZV_LCDDATA3
GPU_DVOD<4>	AJ6	ZV_LCDDATA4
GPU_DVOD<5>	AK6	ZV_LCDDATA5
GPU_DVOD<6>	AG7	ZV_LCDDATA6
GPU_DVOD<7>	AH7	ZV_LCDDATA7
GPU_DVOD<8>	AJ7	ZV_LCDDATA8
GPU_DVOD<9>	AK7	ZV_LCDDATA9
GPU_DVOD<10>	AG8	ZV_LCDDATA10
GPU_DVOD<11>	AH8	ZV_LCDDATA11
NC	AJ8	ZV_LCDDATA12
NC	AK8	ZV_LCDDATA13
NC	AG9	ZV_LCDDATA14
NC	AH9	ZV_LCDDATA15
NC	AJ9	ZV_LCDDATA16
NC	AK9	ZV_LCDDATA17
NC	AG10	ZV_LCDDATA18
NC	AH10	ZV_LCDDATA19
	AJ10	ZV_LCDDATA20
NC	AK10	ZV_LCDDATA21
NC	AG11	ZV_LCDDATA22
NC	AH11	ZV_LCDDATA23
GPU_DVO_VSYNC	AJ4	ZV_LCDCNTL0
GPU_DVO_HSYNC	AK4	ZV_LCDCNTL1
GPU_DVOD_DE	AH5	ZV_LCDCNTL2
GPU_DVO_CLKP	AG5	ZV_LCDCNTL3
ATI_AGP_FBSKEW<0>	AJ2	GPIO0
ATI_AGP_FBSKEW<1>	AK2	GPIO1
ATI_X1CLK_SKEW<0>	AK1	GPIO2
ATI_X1CLK_SKEW<1>	AH3	GPIO3
ATI_BUS_CFG<0>	AH2	GPIO4
ATI_BUS_CFG<1>	AJ1	GPIO5
ATI_BUS_CFG<2>	AF4	GPIO6
	AH1	GPIO7
	AG3	GPIO8
	AF3	GPIO9
	AG2	GPIO10
	AF2	GPIO11
	AG1	GPIO12
	AF1	GPIO13
	AE2	GPIO14
	AE1	GPIO15
	M1	GPIO16
ATI_TMDS_DN<0>	AJ13	TX0M
ATI_TMDS_DP<0>	AK13	TX0P
ATI_TMDS_DN<1>	AJ14	TX1M
ATI_TMDS_DP<1>	AK14	TX1P
ATI_TMDS_DN<2>	AJ15	TX2M
ATI_TMDS_DP<2>	AK15	TX2P
ATI_TMDS_CLKN	AJ12	TXCM
ATI_TMDS_CLKP	AK12	TXCP
ATI_CLK27M_IN	AJ29	XTALIN
NC	AJ30	XTALOUT
ATI_TESTEN	AH24	TESTEN
NC	AJ26	SSIN
	B24	VSS
	B20	VSS
	A24	VSS
	A20	VSS
	B21	VSS

ROMCSB	AE5	NC
R	AK28	GPU_R
G	AK27	GPU_G
B	AK26	GPU_B
VSYNC	AG27	ATI_VSYNC
V2SYNC	AG25	NC
HSYNC	AG26	ATI_HSYNC
H2SYNC	AG24	NC
RSET	AK25	ATI_RSET
R2SET	AJ24	ATI_R2SET
Y_G	AK23	GPU_Y
C_R	AK24	GPU_C
COMP_R	AK22	GPU_COMP
DIGON	AE13	FP_PWR_EN
BLON	AF13	INV_ON_PWM
HPD1	AF11	+3V_GPU
AUXWIN	AJ27	GPU_AUXWIN
DDC1DATA	AH28	GPU_DVI_DDC_DATA
DDC1CLK	AH27	GPU_DVI_DDC_CLK
DDC2DATA	AE12	LVDS_DDC_DATA
DDC2CLK	AF12	LVDS_DDC_CLK
DDC3DATA	AH26	SI_DDC_DATA
DDC3CLK	AH25	SI_DDC_CLK
TXOUT_U0N	AH18	LVDS_U0N
TXOUT_U0P	AG18	LVDS_U0P
TXOUT_U1N	AH19	LVDS_U1N
TXOUT_U1P	AG19	LVDS_U1P
TXOUT_U2N	AH20	LVDS_U2N
TXOUT_U2P	AG20	LVDS_U2P
TXOUT_U3N	AH22	LVDS_U3N_TP (NO ICT TEST)
TXOUT_U3P	AG22	LVDS_U3P_TP (NO ICT TEST)
TXCLK_UN	AH21	CLKLVDS_UN
TXCLK_UP	AG21	CLKLVDS_UP
TXOUT_L0N	AK16	LVDS_L0N
TXOUT_L0P	AJ16	LVDS_L0P
TXOUT_L1N	AK17	LVDS_L1N
TXOUT_L1P	AJ17	LVDS_L1P
TXOUT_L2N	AK18	LVDS_L2N
TXOUT_L2P	AJ18	LVDS_L2P (NO ICT TEST)
TXOUT_L3N	AK20	LVDS_L3N_TP (NO ICT TEST)
TXOUT_L3P	AJ20	LVDS_L3P_TP
TXCLK_LN	AK19	CLKLVDS_LN
TXCLK_LP	AJ19	CLKLVDS_LP
SSOUT	AJ25	NC

R240 75 1% 1/16W MF 402 — GPU_R
R246 75 1% 1/16W MF 402 — GPU_G
R249 75 1% 1/16W MF 402 — GPU_B
R256 715 1% 1/16W MF 402 — GPU_Y
R257 499 1% 1/16W MF 402 — GPU_C
R245 75 1% 1/16W MF 402 — GPU_COMP
R248 75 1% 1/16W MF 402 — FP_PWR_EN
R254 75 1% 1/16W MF 402 — INV_ON_PWM
R711 10K 5% 1/16W MF 402 — +3V_GPU
R247 10K 5% 1/16W MF 402 — GPU_DVI_DDC_DATA
R253 10K 5% 1/16W MF 402 — GPU_DVI_DDC_CLK

Q77 SI3446DV TSOP

+1_5V_AGP → pins 1,2,5,6 — pin 3 GPU_CORE_OK — pin 4 +GPU_VDD15_UF

L24 FERR-220-OHM 0805

+1_5V_GPU_VDD15 (500mA) → +GPU_VDD15_UF

C166 1000pF 10% 25V X7R 402

C222 C256 C299 C305 C328 0.01uF 20% 16V CERM 402 (C328 10uF 20% 6.3V CERM 805)
C232 C269 C300 C306 0.01uF 20% 16V CERM 402

U44 RAGE_MOBILITY M11-CSP64 64MB BGA (5 OF 6)

OMIT

F12		VDD15
L6		VDD15
T6		VDD15
AB6		VDD15
F17		VDD15
G25		VDD15
R25		VDD15
AB25		VDD15
AJ3		VDDC
AF25		VDDC
AG4		VDDC
AH4		VDDC
AF5		VDDC
F6		VDDC
G6		VDDC
H6		VDDC
P6		VDDC
AD26		VDDC
V6		VDDC
W6		VDDC
AC6		VDDC
AD6		VDDC
AE6		VDDC
F7		VDDC
F10		VDDC
AE10		VDDC
F11		VDDC
AE11		VDDC
F13		VDDC
F14		VDDC
AE14		VDDC
AF14		VDDC
W26		VDDC
AF15		VDDC
AE17		VDDC
AC25		VDDC
AE18		VDDC
F23		VDDC
F24		VDDC
AE24		VDDC
F25		VDDC
M25		VDDC
N25		VDDC
W25		VDDC
V25		VDDC
G7		VSS
G8		VSS
G9		VSS
G10		VSS
G11		VSS
G12		VSS
G13		VSS
G14		VSS
G15		VSS
G16		VSS
G17		VSS
G18		VSS
G19		VSS
G20		VSS
G21		VSS
G22		VSS
G23		VSS
G24		VSS
H7		VSS
H8		VSS
H23		VSS
H24		VSS
J7		VSS
J24		VSS
K7		VSS
K24		VSS
L7		VSS
L24		VSS
M7		VSS
M24		VSS
N7		VSS
N24		VSS
P7		VSS
P24		VSS
R7		VSS
R24		VSS
T7		VSS
T24		VSS
U7		VSS
U24		VSS
V7		VSS
V24		VSS
W7		VSS
W24		VSS
Y7		VSS
Y24		VSS
AA7		VSS
AA24		VSS
AB7		VSS
AB24		VSS
AC7		VSS
AC8		VSS
AC23		VSS
AC24		VSS
AD7		VSS
AD8		VSS
AD9		VSS
AD10		VSS
AD11		VSS
AD12		VSS
AD13		VSS
AD14		VSS
AD15		VSS
AD16		VSS
AD17		VSS
AD18		VSS
AD19		VSS
AD20		VSS
AD21		VSS
AD22		VSS
AD23		VSS

GPU VCORE - 1.2V

(PUT ALL CAPs BELOW ATI ASIC)

GPU_VCORE → C167 C219 C252 C270 C301 C307 C329 C332 10uF 20% 6.3V CERM 805 / 0.22uF 20% 6.3V CERM 402
C186 C220 C253 C271 C302 C311 C330 C333 0.22uF 20% 6.3V CERM 402
C187 C221 C254 C282 C303 C326 C331 C338 0.22uF 20% 6.3V CERM 402

M10 Power Shut down Sequencing

XW21 SM — DP6 BAS16TW SOT-363 — +1_8V_ATI_PVDD
XW20 SM — DP6 BAS16TW SOT-363 — +1_8V_PVDD_NECK
XW22 SM — DP6 BAS16TW SOT-363 — +GPU_VDD15_UF / +GPU_VDD15_NECK
XW24 SM — +2_5V_SLEEP
XW23 SM — +1_5V_AGP_NECK → +1_5V_AGP

R258 R260 10K 5% 1/16W MF 402
R262 R265 R269 R271 10K NO STUFF 5% 1/16W MF 402
R259 R261 R263 R266 R270 R272 R274 10K NO STUFF 5% 1/16W MF 402

(GPIO0) ATI_AGP_FBSKEW<0>
(GPIO1) ATI_AGP_FBSKEW<1>
(GPIO2) ATI_X1CLK_SKEW<0>
(GPIO3) ATI_X1CLK_SKEW<1>
(GPIO4) ATI_BUS_CFG<0>
(GPIO5) ATI_BUS_CFG<1>
(GPIO6) ATI_BUS_CFG<2>

GPU VCORE SUPPLY

WHEN VCORE_CNTL HIGH => 1.2V
1.2V = 0.8V * (1 + R332 / (R331//R333))

WHEN VCORE_CNTL LOW => 1.0V
1.0V = 0.8V * (1 + R332 / R333)

+PBUS
R389 1M 5% 1/16W MF 402
R430 1 5% 1/16W MF 603
R339 576K 1% 1/16W MF 402
C762 C766 4.7UF 20% 25V CERM 1206
Q51 SI7860DP SO-8-PWRPK CRITICAL
L30 2.1UH-11A SM CRITICAL
D24 SMB B340LB
D5 SM MBR0540
Q48 SI7892DP SO-8-PWRPK CRITICAL
C882 0.0022UF 10% 50V CERM 402 NO STUFF
XW2 SM OMIT

R388 NO STUFF 0 5% 1/16W MF 402
R341 63.4K 1% 1/16W MF 402
C473 4.7UF 20% 10V CERM 1206
C494 0.1UF 20% 25V CERM 603
R236 100K 5% 1/16W MF 402
R416 2.2 5% 1/16W MF 603
C514 0.1UF 20% 25V CERM 603
R390 0 5% 1/16W MF 402
R340 20K 1% 1/16W MF 402
C451 220pF 5% 25V CERM 402
C448 470pF 10% 50V CERM 402
R311 R332 0 5% 1/16W MF 402
C483 0.1UF 20% 10V CERM 402

U16 LTC1778 SSOP CRITICAL
EXT VCC INT VCC VIN
RUN/SS ITH VRNG FCB PGOOD SGND PGND
ION BOOST TG SW BG VFB

R306 R316 100K 5% 1/16W MF 402
DP1 BAS16TW SOT-363 — SLEEP_L_LS5
DP1 BAS16TW SOT-363 — DCDC_EN
R294 10K 5% 1/16W MF 402 — GPU_VCORE_PWR_SEQ
Q6 2N3904 SM — GPU_VCORE_SEQ_L
Q5 2N3904 SM — GPU_VCORE_SEQ
R203 33K 5% 1/16W MF 402

C708 22uF 20% 10V CERM 1210
C719 330UF 20% 6.3V POLY SMD
C721 C720 330UF 20% 6.3V POLY SMD
R307 100K 5% 1/16W MF 402
C902 0.1UF 20% 10V CERM 402
Q80 2N7002DW SOT-363
C515 0.1UF 10% 10V CERM 402
R410 10K 5% 1/16W MF 402 — VCORE_CNTL_RC
R352 4.99K 1% 1/16W MF 402
R451 18.2K 1% 1/16W MF 402
R804 1.82K 1% 1/16W MF 402
R351 20K 1% 1/16W MF 402

M10 CORE PWR/LVDS/TMDS	
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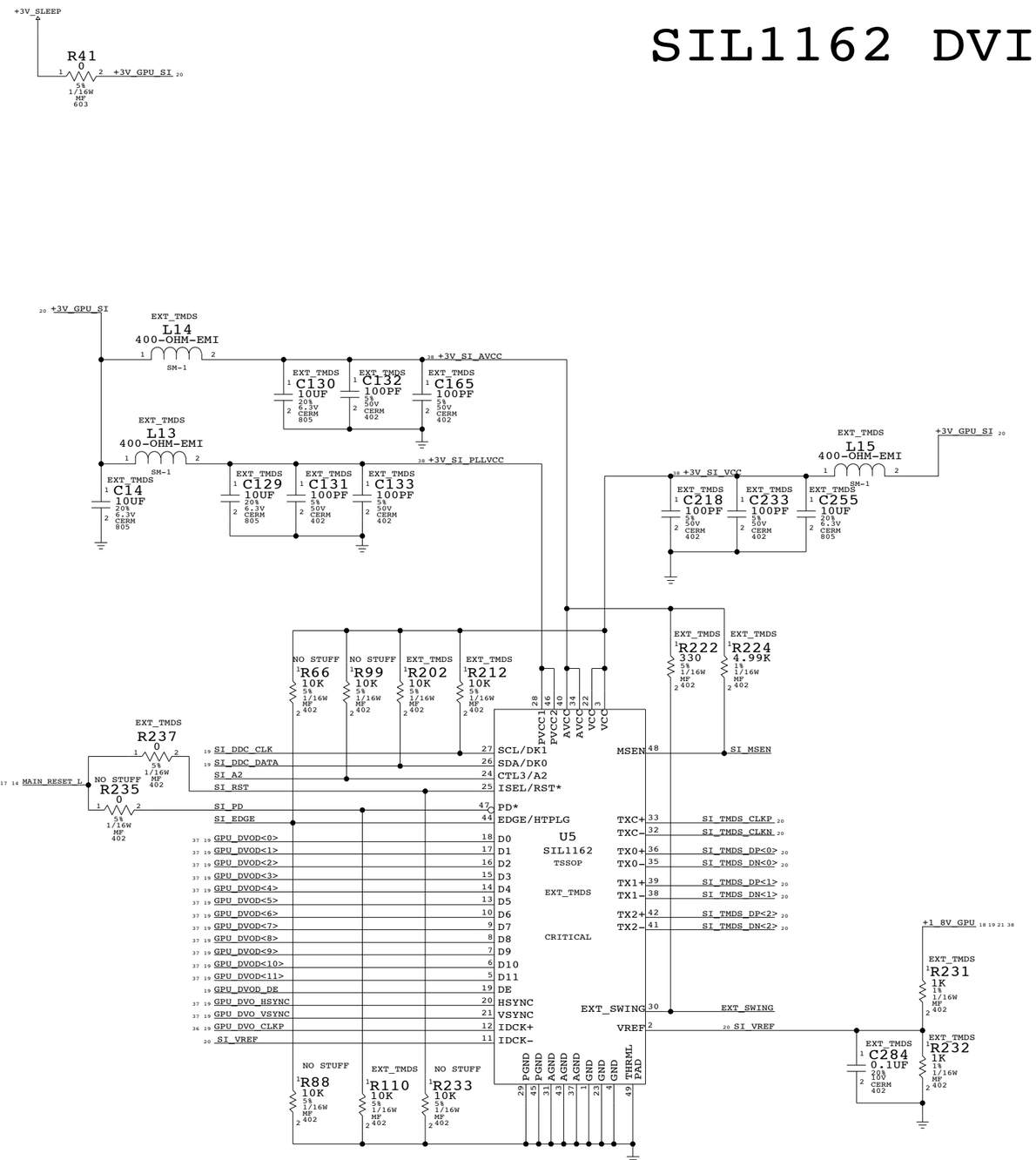
	SCALE NONE — SHT 19 OF 44

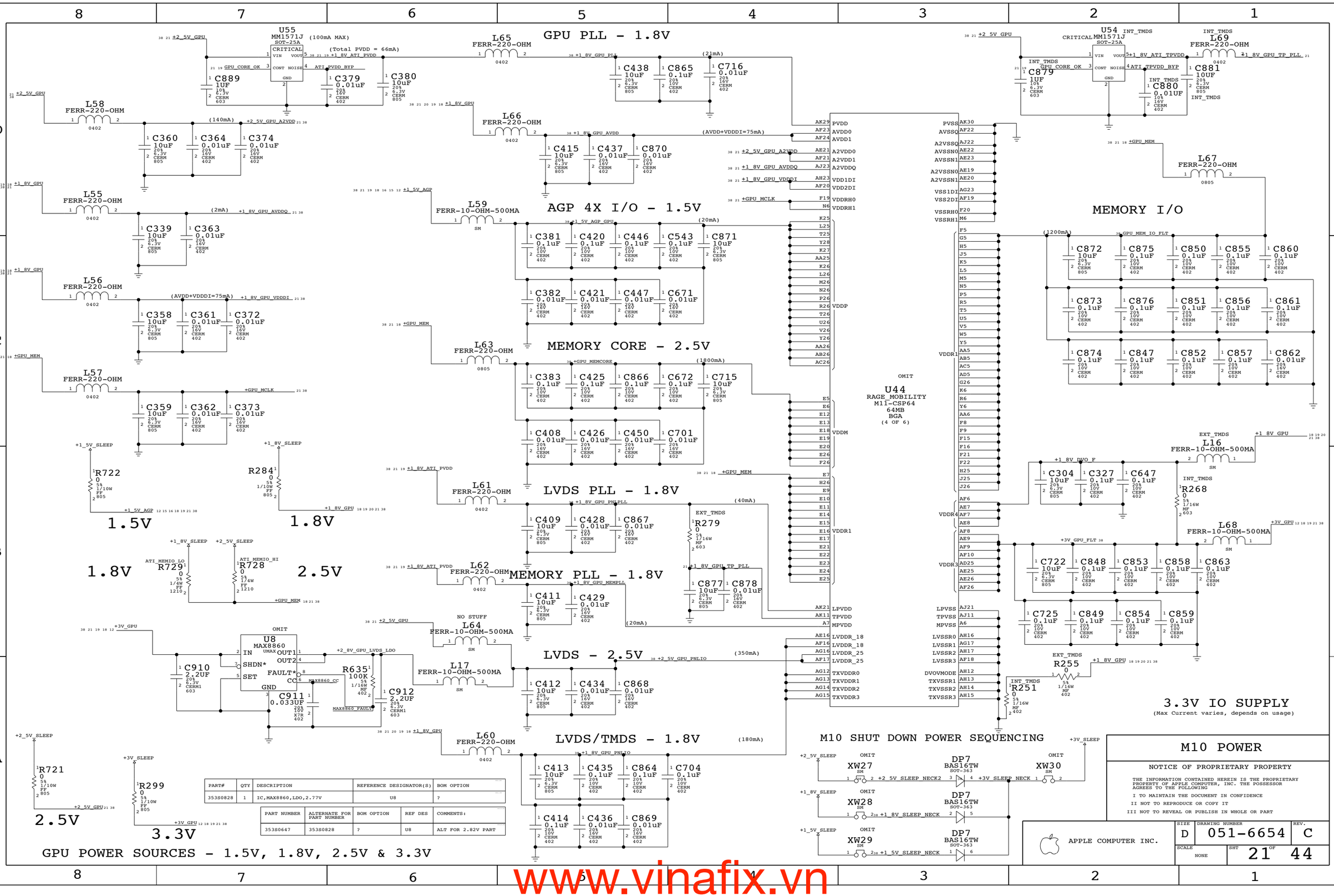
SIL1162 DVI TRANSMITTER



APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	C

SCALE	SHT	OF
NONE	20	44



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S0828	1	IC,MAX8860,LDO,2.77V	U8	?

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0647	353S0828	?	U8	ALT FOR 2.82V PART

EXTERNAL VIDEO (DVI) INTERFACE

ANALOG FILTERING PLACE CLOSE TO CONNECTOR

FL2 CRITICAL LCFILTER SM-220MHZ — GPU_B → VGA_B
FL1 CRITICAL LCFILTER SM-220MHZ — GPU_G → VGA_G
FL3 CRITICAL LCFILTER SM-220MHZ — GPU_R → VGA_R
C685 3.3PF 0.25% 50V CERM 402
C676 3.3PF 0.25% 50V CERM 402
C684 3.3PF 0.25% 50V CERM 402

VGA VSYNC BUFFERS

+3V_MAIN
U56 CRITICAL 74AHC1G32 SM — ATI_HSYNC → R718 33 5% 1/16W MF 402 → VGA_HSYNC
U57 CRITICAL 74AHC1G32 SM — ATI_VSYNC → R714 33 5% 1/16W MF 402 → VGA_VSYNC

DVI DDC CURRENT LIMIT

(55mA requirement per DVI spec)

+5V_SLEEP → F1 0.5AMP-13.2V SM → +5V_DDC_SLEEP_UF → L23 400-OHM-EMI SM-1 → +5V_DDC_SLEEP

Isolation required for DVI power switch

D21 SM MBR0530 — DDC_CLK_ISO

R661 4.7K 5% 1/16W MF 402
R655 4.7K 5% 1/16W MF 402

J14 CRITICAL QH1112 F-RT-TH

TMDS_CONN_DN<0>	17	1	TMDS_CONN_DN<2>
TMDS_CONN_DN<1>	9	2	TMDS_CONN_DP<2>
TMDS_CONN_DP<0>	18	10	TMDS_CONN_DP<1>
(TMDS_DN<5>)	19	3	
	20 NC	11	(TMDS_DN<4>)
	NC	4 NC	(TMDS_DN<3>)
(TMDS_DP<5>)	21	12 NC	(TMDS_DP<4>)
	NC	5 NC	(TMDS_DP<3>)
	22	13 NC	
		6	DVI_DDC_CLK_UF
		14	(+5V_DDC_SLEEP)
TMDS_CONN_CLKP	23	7	DVI_DDC_DATA_UF
TMDS_CONN_CLKN	24	15	
		8	VGA_VSYNC
VGA_B	C3	16	DVI_HPD_UF
VGA_HSYNC	C5B	C1	VGA_R
	C4	C5A	
		C2	VGA_G
	34	32	
		35	

R706 0 5% 1/16W MF 402 — PLACE NEAR 3, 11 & 19
R1 0 5% 1/16W MF 402 — PLACE NEAR C5A & C5B

C706 100pF 5% 50V CERM 402
C669 100pF 5% 50V CERM 402
C710 0.01UF 20% 50V CERM 603
C1 100pF 5% 50V CERM 402

CHGND5 CHGND1

3V LEVEL SHIFTERS

+3V_SLEEP

Q38 2N7002DW SOT-363 — DVI_DDC_CLK → GPU_DVI_DDC_CLK
Q38 2N7002DW SOT-363 — DVI_DDC_DATA → GPU_DVI_DDC_DATA
Q35 2N7002DW SOT-363 — DVI_HPD → GPU_HPD

R662 10K 5% 1/16W MF 402
R671 10K 5% 1/16W MF 402
R694 100K 5% 1/16W MF 402
R670 100 5% 1/16W MF 402
R649 100 5% 1/16W MF 402
R650 100 5% 1/16W MF 402

NOTE: Pulldown for DVI_HPD provided by DVI power switch interface

NOTE: DVI_HPD SHARES Q68 WITH ALS BECAUSE OF BOARD REAL ESTATE

DVI POWER SWITCH

Power key detect path when system is shutdown or asleep.. DDC_CLK is isolated from NV17M DURING SHUTDOWN. WHEN power key on remote device is pressed, 5V will be driven into DDC_CLK. Since host rails will be low, TP0610 will turn on, driving SOFT_PWR_ON_L low. As host rails rise, TP0610 will turn off, as will remote device path into DDC_CLK. Isolation will be disabled as well.

Q40 TP0610 SM — DVI_DDC_CLK_UF → DVI_TURN_ON
R690 680 5% 1/16W MF 402 — DVI_TURN_ON → DVI_TRUN_ON_ILIM
R691 10K 5% 1/16W MF 402 — DVI_TURN_ON_BASE
Q42 2N3904 SM — SOFT_PWR_ON_L
R688 330 5% 1/16W MF 402 — +5V_DDC_SLEEP

Pulldown prevents 3904 from turning on when DVI monitor has active, self-powered DDC clock pullup.

Power key detect path when system is running. HPD normally driven to 3.3V. When power key on remote device pressed, HPD will be driven to 5V. COMPARATOR ENABLED BY NV17MAP GPIO.

+3V_SLEEP
R680 68.1K 1% 1/16W MF 402 — HPD_4V_REF
C696 0.1UF 20% 10V CERM 402
U46 LMC7211 SM CRITICAL — HPD_PWR_SW → Q41 2N7002DW SOT-363 → HPD_ON
DVI_HPD_UF → R663 10K 1% 1/16W MF 402 → DVI_HPD_DIV
R686 10K 1% 1/16W MF 402
R681 100K 1% 1/16W MF 402
+PBUS
Q45 TP0610 SM — COMP_ENABLE
R696 100K 5% 1/16W MF 402
R704 100K 5% 1/16W MF 402
COMP_DISABLE
R703 330 5% 1/16W MF 402
R700 20K 5% 1/16W MF 402 — HPD_BASE → Q44 2N3904 SM
HPD_ON_RC
C703 47UF 20% 6.3V CERM 1210
R705 68K 5% 1/16W MF 402

NEED PULL-DOWN BECAUSE THIS SIGNAL IS TRISTATED INITIALLY

HPD_PWR_SNS_EN → Q41 2N7002DW SOT-363
R213 100K 5% 1/16W MF 402

INVERTER INTERFACE

+PBUS
L33 FERR-1K-OHM-EMI SM — +12_8V_INV
+5V_MAIN
Q7 FDG6324L SC70-6 — +5V_INV_UF_SW
L32 400-OHM-EMI SM-1 — +5V_INV_SW
R317 100K 5% 1/16W MF 402
C440 10UF 20% 6.3V CERM 805
FP_PWR_EN_L
Q7 FDG6324L SC70-6 — FP_PWR_EN
C746 0.001UF 20% 50V CERM 402
C749 0.001UF 20% 50V CERM 402
C739 0.001UF 20% 50V CERM 402
CRITICAL J7 SM-2MT
L31 400-OHM-EMI SM-1 — BRIGHT_PWM
+3V_PMU
C552 0.1UF 20% 10V CERM 402
INV_ON_PWM → U24 74LVC32 TSSOP → BRIGHT_PWM_UF
INVERTER EXPECTS ACTIVE HIGH SIGNAL
SHARES LOGIC WITH KB RESET SIGNALS (PG 28)
R724 0 5% 1/16W MF 402
C744 0.01UF 20% 50V CERM 603
CHGND2

LCD INTERFACE

LVDS INTERFACE

C416 0.001uF 20% 50V CERM 402 — CHGND4
CRITICAL J6 G-501973 F-RT-SM

100K pull-ups are for no-panel case (development) Panel has 2K pull-ups

+3V_SLEEP
R342 100K 5% 1/16W MF 402
R320 100K 5% 1/16W MF 402
+3V_LCD
(LVDS DDC POWER)
NC
LVDS_DDC_CLK
LVDS_DDC_DATA
NO STUFF
C449 0.001uF 20% 50V CERM 402
C452 0.001uF 20% 50V CERM 402
CHGND4

	1	1	
	2	2	
	3	3	
(LVDS DDC POWER)	4	4	
NC	5	5	
	6	6	
	7	7	
LVDS_L0N	8	8	
LVDS_L0P	9	9	
LVDS_L1N	10	10	
LVDS_L1P	11	11	
LVDS_L2N	12	12	
LVDS_L2P	13	13	
CLKLVDS_LN	14	14	
CLKLVDS_LP	15	15	
LVDS_U0N	16	16	
LVDS_U0P	17	17	
LVDS_U1N	18	18	
LVDS_U1P	19	19	
LVDS_U2N	20	20	
LVDS_U2P	21	21	
CLKLVDS_UN	22	22	
CLKLVDS_UP	23	23	
	24	24	
	25	25	
	26	26	
	27	27	
	28	28	
	29	29	
	30	30	
	33	33	

C500 0.001uF 20% 50V CERM 402

LCD POWER SWITCHES

+3V_MAIN
R400 100K 5% 1/16W MF 402
C484 2200pF 5% 50V CERM 603
R391 100K 5% 1/16W MF 402
LCD_PWREN_L
LCD_DIGON_L
Q11 TSOP SI3443DV
+3V_LCD_SW
L6 FERR-250-OHM SM
C474 0.001uF 20% 50V CERM 402
Q8 2N7002 SM — FP_PWR_EN
CHGND4

S-VIDEO/COMP OUT INTERFACE

Place GND shorts at graphics controller

XW12 SM — GPU_TV_GND1 → L26 FERR-10-OHM-500MA SM → TV_GND1
L25 3.3UH 0603 — GPU_Y → TV_C
L29 3.3UH 0603 — GPU_C → TV_Y
L27 3.3UH 0603 — GPU_COMP → TV_COMP
C712 0.01UF 20% 50V CERM 603
C702 560PF 10% 50V CERM 402
C707 560PF 10% 50V CERM 402
C718 560PF 10% 50V CERM 402
C724 560PF 10% 50V CERM 402
C714 560PF 10% 50V CERM 402
C713 560PF 10% 50V CERM 402
CRITICAL J15 MINIDIN RT-TH MH1177
XW13 SM — GPU_TV_GND2 → L28 FERR-10-OHM-500MA SM → TV_GND2
C717 0.01UF 20% 50V CERM 603
CHGND1

Place GND shorts at graphics controller

TMDS FILTERING PLACE CLOSE TO CONNECTOR

CRITICAL L72 90-OHM-300MA 2012H — TMDS_DN<0> → TMDS_CONN_DN<0>
CRITICAL L73 90-OHM-300MA 2012H — TMDS_DP<0> → TMDS_CONN_DP<0>
CRITICAL L74 90-OHM-300MA 2012H — TMDS_DN<1> → TMDS_CONN_DN<1>
CRITICAL L75 90-OHM-300MA 2012H — TMDS_DP<1> → TMDS_CONN_DP<1>
CRITICAL L21 165-OHM SM OMIT — TMDS_CLKP → TMDS_CONN_CLKP; TMDS_CLKN → TMDS_CONN_CLKN
CRITICAL L76 90-OHM-300MA 2012H — TMDS_DN<2> → TMDS_CONN_DN<2>
CRITICAL L77 90-OHM-300MA 2012H — TMDS_DP<2> → TMDS_CONN_DP<2>

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
155S0147	1	370OHM COMMON MODE CHOKE	L21	?

VIDEO CONNECTORS

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APPLE COMPUTER INC.

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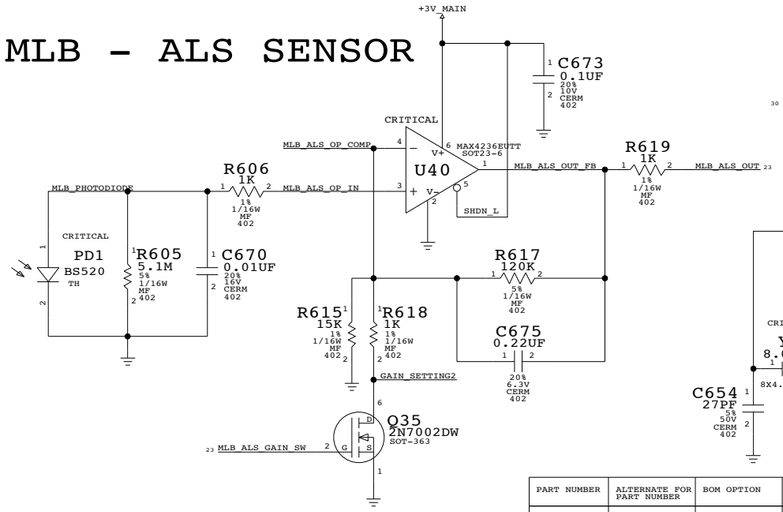
D	051-6654	C
SCALE: NONE	SHT 22 OF 44	

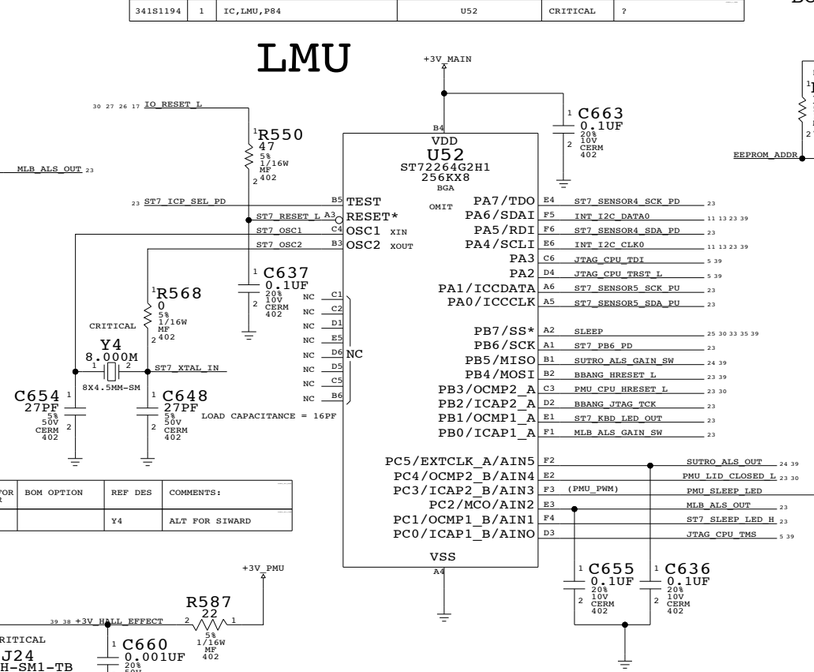
MLB - ALS SENSOR



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0856	353S0504	?	U40	ALT FOR SUPPLY PROBLEM

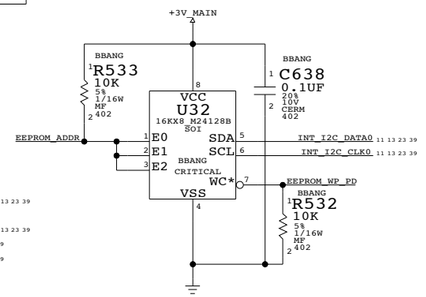
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1194	1	IC,LMU,P84	U52	CRITICAL	?

LMU

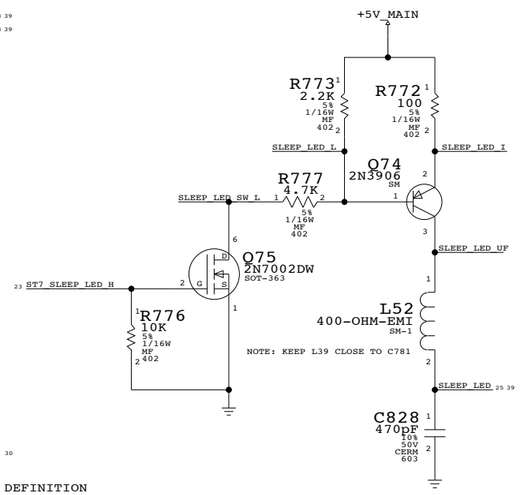


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0008	197S0040		Y4	ALT FOR SIWARD

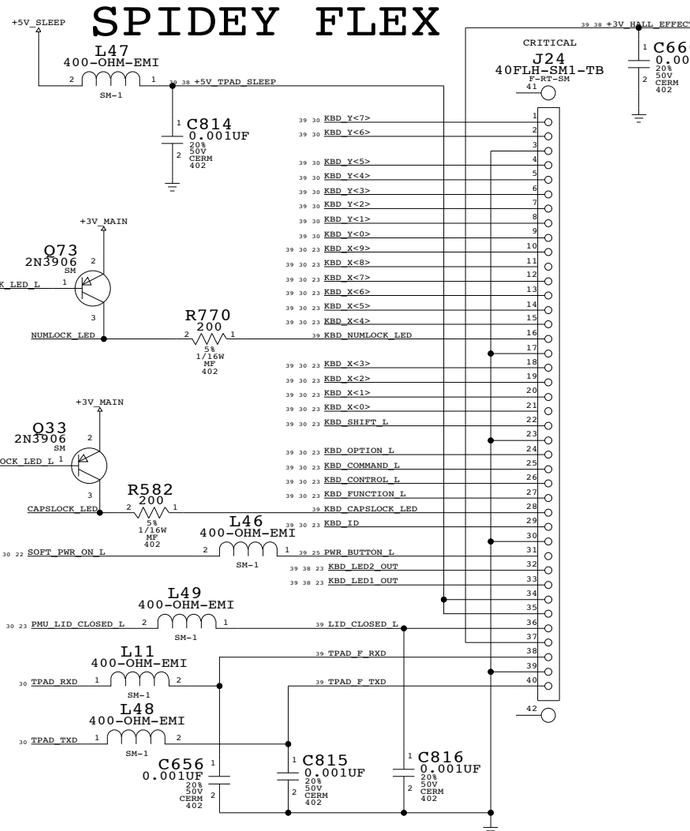
BOOT BANGER E2PROM



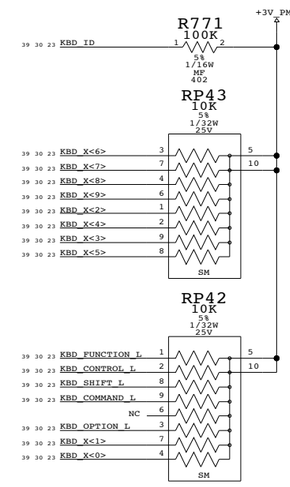
SLEEP LED



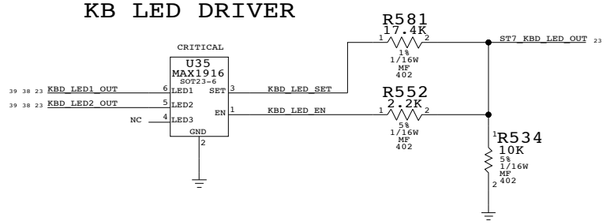
SPIDEY FLEX



KEYBOARD PULLUPS

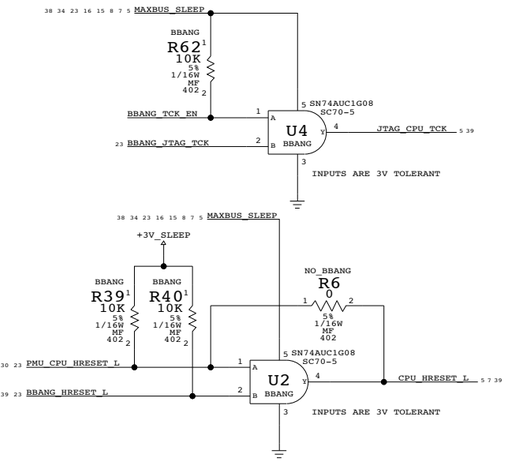


KB LED DRIVER

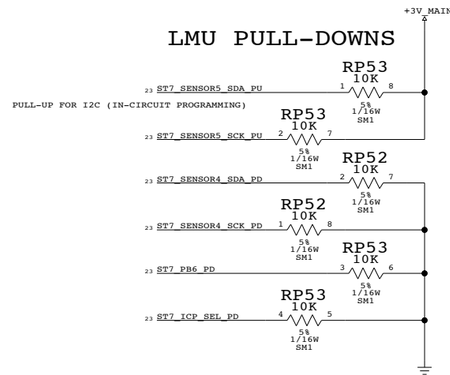


BOOT BANGER SIGNAL DEFINITION

1/ BBANG_HRESET_L (OPEN COLLECTOR OUTPUT - 10K PULLUP ON MLB)
2/ PMU_HRESET_L (3V INPUT INTO LMU)
3/ BBANG_JTAG_TCK (REGULAR OUTPUT)
4/ JTAG_CPU_TMS (OPEN COLLECTOR OUTPUT - 4700HM PULLUP ON MLB)
5/ JTAG_CPU_TDI (OPEN COLLECTOR OUTPUT - 4700HM PULLUP ON MLB)
6/ JTAG_CPU_TRST_L (OPEN COLLECTOR OUTPUT - 4700HM PULLUP ON MLB)



LMU PULL-DOWNS



LMU/BOOTBANGER/SPIDEY

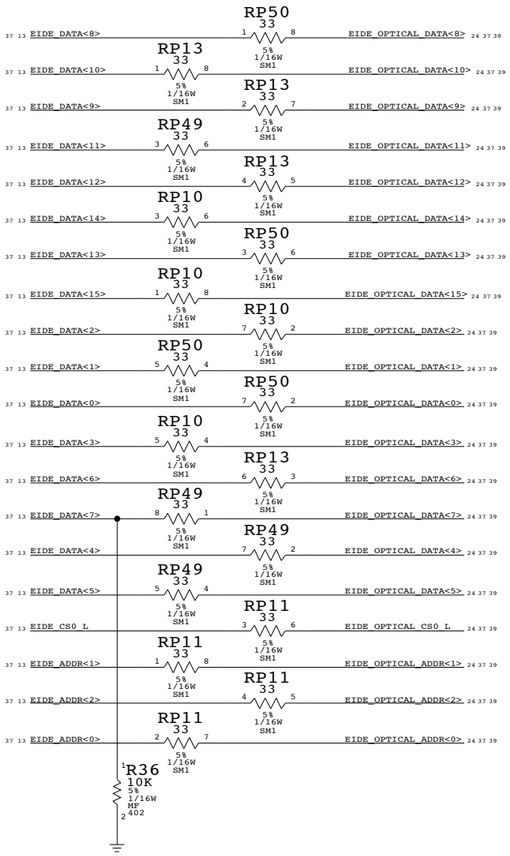
APPLE COMPUTER INC.

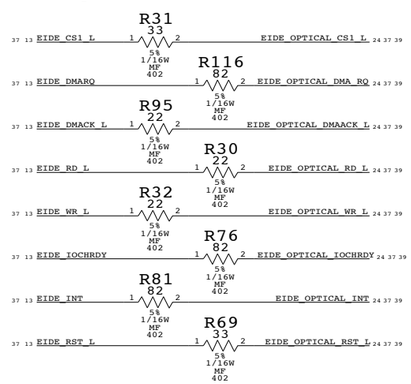
SIZE	DRAWING NUMBER	REV.
D	051-6654	C
SCALE: NONE	SHT 23 OF 44	

HARD DRIVE INTERFACE (UATA100)

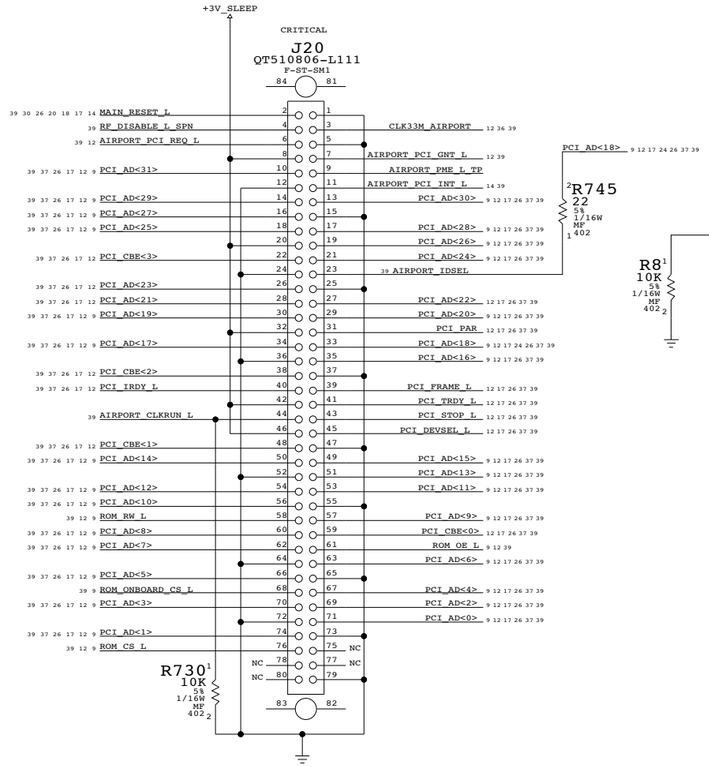
EIDE SERIES TERMINATION

PLACE TERMINATORS NEAR INTREPID

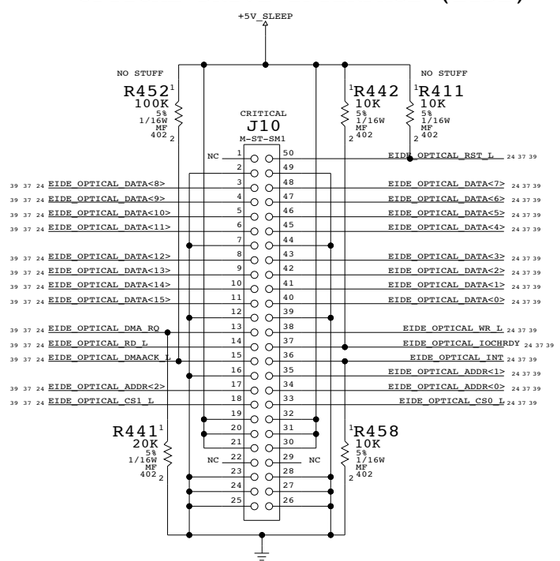




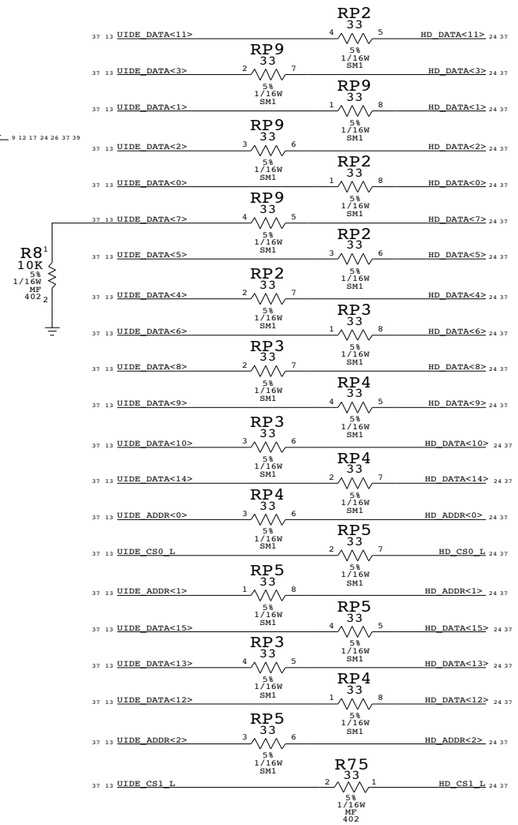
WIRELESS INTERFACE



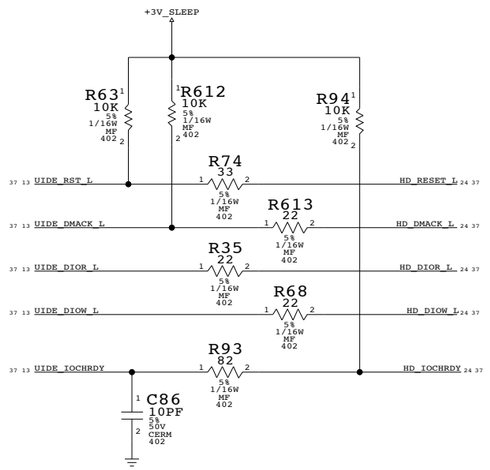
OPTICAL DRIVE INTERFACE (EIDE)



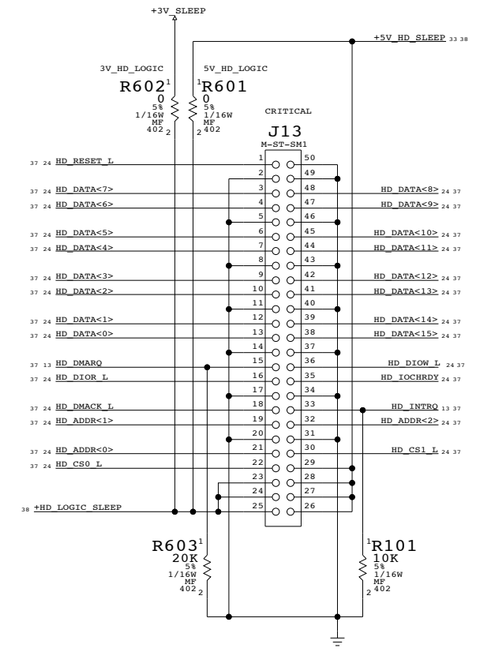
PLACE SERIES R CLOSE TO INTERPID



PLACE PULLUP RESISTORS CLOSE TO INTREPID

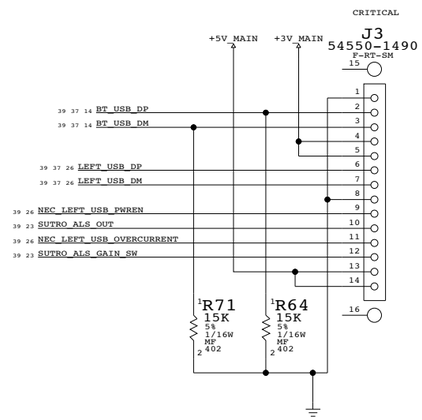


IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V



ANY SEQUENCING REQUIREMENT BETWEEN +5V_HD_SLEEP AND +3V_SLEEP?

BLUETOOTH/LEFT-SIDE USB



INTERNAL I/O CONNECTORS

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SCALE: NONE	SHT 24 OF 44	

SOUND BOARD (SOUSAPHONE)

AUDIO - SNAPPER
SND - INTREPID

L77 FERR-220-OHM 0402
L80 FERR-220-OHM 0402
L81 FERR-220-OHM 0402
L82 FERR-220-OHM 0402
L76 FERR-220-OHM 0402
L78 FERR-220-OHM 0402
L79 FERR-220-OHM 0402

SND_SYNC → SND_SYNC_F
SND_CLKOUT → SND_CLKOUT_F
INT_AUDIO_TO_SND → INT_AUDIO_TO_SND_F
SND_TO_AUDIO → SND_TO_AUDIO_F
SND_AMP_MUTE → SND_AMP_MUTE_F
SND_HW_RESET_L → SND_HW_RESET_L_F
SND_SCLK → SND_SCLK_F

C895 0.01UF 20% 16V CERM 402 NO STUFF
C899 0.01UF 20% 16V CERM 402 NO STUFF
C896 0.01UF 20% 16V CERM 402 NO STUFF
C897 0.01UF 20% 16V CERM 402 NO STUFF
C898 0.01UF 20% 16V CERM 402 NO STUFF
C900 0.01UF 20% 16V CERM 402 NO STUFF
C901 0.01UF 20% 16V CERM 402 NO STUFF

+3V_MAIN
+5V_MAIN

J12 QT510306-L111 F-ST-SM1 CRITICAL

INT_AUDIO_TO_SND_F → SND_TO_AUDIO_F
INT_I2C_CLK2 → SND_HP_SENSE_L
SND_SCLK_F → SND_LIN_SENSE_L
SND_CLKOUT_F → SND_AMP_MUTE_F
SND_SYNC_F → SLEEP
INT_I2C_DATA2 → SND_HW_RESET_L_F
SLEEP_LED → SND_HP_MUTE_INV
SND_AGND

XW9 SM

RP44 100K 5% 1/16W SM1
Q26 2N7002DW SOT-363
SND_AMP_MUTE → SND_AMP_MUTE_L
AMP_CONTROL
INT_PU_RESET_L

RP44 100K 5% 1/16W SM1
R689 100K 5% 1/16W MF 402
SND_HP_MUTE_INV
Q31 2N7002DW SOT-363
SND_HP_MUTE
Q31 2N7002DW SOT-363
SND_HP_MUTE_L
AMP_CONTROL
RP44 100K 5% 1/16W SM1

MODEM

SUPPORTS BOTH THE LAST DASH AND Q52 SOFT MODEM

C767 10UF 20% 6.3V CERM 805 NO STUFF
C513 0.1UF 20% 10V CERM 402
R405 10K 5% 1/16W MF 402
C478 0.1UF 20% 10V CERM 402 NO STUFF
C469 10UF 20% 6.3V CERM 805

J8 QT51066-L010 F-ST-SM1 CRITICAL

MOD_DTO → MOD_SYNC
MOD_CLKOUT → INT_MOD_DTI
MOD_BITCLK
COMM_RESET_L → MODEM_USB_DM
COMM_SHUTDOWN → MODEM_USB_DP
INT_I2C_CLK2 → COMM_RING_DET_L
INT_I2C_DATA2

FAN CONTROLLER

R814 10 5% 1/16W MF 402
C904 1UF 20% 10V CERM 603
ADT7460_VCC
C711 0.1UF 20% 50V CERM 402

U3 ADT7460 QSOP CRITICAL

+2.5V/SMBALERT# SDA SCL
D1+ D1- D2+ D2-
PWM1/XTO TACH1 PWM2/SMBALERT# TACH2 PWM3/ADR ENABLE# TACH3 TACH4/ADR SELECT/THERM# GND

ADT7460_VCORE_MON
INT_I2C_DATA1
INT_I2C_CLK1
THERM1_DP
THERM1_DM
THERM2_DP
THERM2_DM

ADT7460_FAN1_PWM
FANL_TACH
ADT7460_FAN2_PWM
FANR_TACH
ADT7460_ADR_EN_L
NC
ADT7460_THERM

R42 10K 5% 1/16W MF 402
R692 10K 5% 1/16W MF 402
R695 10K 5% 1/16W MF 402
Q78 2N7002DW SOT-363
Q78 2N7002DW SOT-363

C688 0.001UF 20% 50V CERM 402 NO STUFF
C690 0.001UF 20% 50V CERM 402 NO STUFF
C846 0.001UF 20% 50V CERM 402 NO STUFF
C905 0.001UF 20% 50V CERM 402 NO STUFF

SERIAL DEBUG INTERFACE

J16 M-ST-5087 SM SERIAL_DEBUG CRITICAL

COMM_TXD_L → COMM_DTR_L
COMM_TRXC → COMM_RTS_L
COMM_GPIO_L → COMM_RXD

DEBUG POWER BUTTON

R527 0 5% 1/16W MF 603 NO STUFF
PWR_BUTTON_L

DEBUG JUMPERS

R293 10K 5% 1/16W MF 402
R295 10K 5% 1/16W MF 402
FANL_PWM
FANR_PWM
R537 0 5% 1/16W MF 603 NO STUFF
PMU_NMI_BUTTON_L
R553 0 5% 1/16W MF 603 NO STUFF
PMU_RESET_BUTTON_L

RIGHT FAN (GPU)

R623 10K 5% 1/16W MF 402
J2 SM-2MT CRITICAL
Q36 SI3446DV TSOP
FANR_GND
FANR_TACH
FANR_PWM
C135 4.7UF 20% 10V CERM 1206 PLACE CLOSE TO CONNECTOR

LEFT FAN (CPU)

R679 10K 5% 1/16W MF 402
J4 SM-2MT CRITICAL
Q37 SI3446DV TSOP
FANL_TACH
FANL_GND
FANL_PWM
C134 4.7UF 20% 10V CERM 1206 PLACE CLOSE TO CONNECTOR

PLACE XW9 CLOSE TO 5V SWITCHER (U27)
PLACE CAPS AS CLOSE TO THERMISTORS AS POSSIBLE
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY

CAPS FOR EMI EXPERIMENTATION ONLY

FAN INTERFACE

MAIN1
C681 0.001UF 20% 50V CERM 402
Q66 2N3904 SM
SUPPLY_M_DP
SUPPLY_M_DM

PLACE CLOSE TO CPU
MAIN2
C668 0.001UF 20% 50V CERM 402
Q39 2N3904 SM
CPU_M_DP
CPU_M_DM

PLACE UNDERNEATH UPPER RAM
ALTERNATE1
C678 0.001UF 20% 50V CERM 402 NO STUFF
Q47 2N3904 SM NO STUFF
THERM1_A_DP
THERM1_A_DM

PLACE CLOSE TO BATTERY CHARGER/VCORE
ALTERNATE2
C651 0.001UF 20% 50V CERM 402 NO STUFF
Q62 2N3904 SM NO STUFF
THERM2_A_DP
THERM2_A_DM

KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

R719 0 5% 1/16W MF 402
R725 0 5% 1/16W MF 402
R713 0 5% 1/16W MF 402
R716 0 5% 1/16W MF 402

CPU_M_DP → THERM1_DP
CPU_M_DM → THERM1_DM
SUPPLY_M_DP → THERM2_DP
SUPPLY_M_DM → THERM2_DM

KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

R628 0 5% 1/16W MF 402 NO STUFF
R620 0 5% 1/16W MF 402 NO STUFF
R723 0 5% 1/16W MF 402
R726 0 5% 1/16W MF 402 NO STUFF
R710 0 5% 1/16W MF 402 NO STUFF
R717 0 5% 1/16W MF 402 NO STUFF

CPU_THERM_DP → THERM1_DP
CPU_THERM_DM → THERM1_DM
THERM1_A_DP → THERM1_DP
THERM1_A_DM → THERM1_DM
THERM2_A_DP → THERM2_DP
THERM2_A_DM → THERM2_DM

THERM ISOLATION

R811 100K 5% 1/16W MF 402
R812 100K 5% 1/16W MF 402
R813 100K 5% 1/16W MF 402
Q87 2N7002DW SOT-363
Q87 2N7002DW SOT-363
C903 0.1UF 20% 10V CERM 402
THERM_INV
THERM_L_OC
ADT7460_THERM

FAN/MODEM/SOUND/SLEEP LED/DEBUG

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	C
SCALE: NONE	SHT 25 OF 44	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0608	197S0038	NEC_USB	Y5	ALT FOR SIWARD

+3V_NEC_VDD

C841 0.1uF 20% 10V CERM 402 — C837 0.1uF 20% 10V CERM 402 — C843 0.1uF 20% 10V CERM 402 — C836 0.1uF 20% 10V CERM 402

C840 0.1uF 20% 10V CERM 402 — C829 0.1uF 20% 10V CERM 402 — C834 0.1uF 20% 10V CERM 402 — C838 0.1uF 20% 10V CERM 402

C842 0.1uF 20% 10V CERM 402 — C845 10uF 20% 6.3V CERM 805 — C830 0.1uF 20% 10V CERM 402 — C833 0.1uF 20% 10V CERM 402

+3V_MAIN — L54 FERR-EMI-100-OHM (SM) — NEC_AVDD

C839 0.1uF 20% 10V CERM 402 — C844 0.1uF 20% 10V CERM 402 — C667 10uF 20% 6.3V CERM 805

R796 0 5% 1/16W MF 603 — +3V_NEC_VDD

Y7 LOAD CAPACITANCE IS 16PF

Y5 30.0000M (CRITICAL, 8X4.5MM-SM) — C649 27PF 5% 50V CERM 402 — C657 27PF 5% 50V CERM 402 — R590 100 5% 1/16W MF 402 — NEC_XT2_R

U39 NEC_UPD720101_USB2 FBGA (CRITICAL)

Low/Full/High Speed (External)

Low/Full/High Speed (External)

H3	AD0	M5	PCI_AD<0>
M4	AD1	P5	PCI_AD<1>
C8	AD2	N5	PCI_AD<2>
P2	AD3	P4	PCI_AD<3>
P3	AD4	N4	PCI_AD<4>
P12	AD5	M3	PCI_AD<5>
A13	AD6	N3	PCI_AD<6>
A12	AD7	M1	PCI_AD<7>
A3	AD8	L2	PCI_AD<8>
E2	AD9	L1	PCI_AD<9>
N8	AD10	K2	PCI_AD<10>
L13	AD11	L3	PCI_AD<11>
J13	AD12	K1	PCI_AD<12>
H13	AD13	K3	PCI_AD<13>
F13	AD14	J2	PCI_AD<14>
D13	AD15	J1	PCI_AD<15>
G12	AD16	F2	PCI_AD<16>
H4	AD17	E3	PCI_AD<17>
D7	AD18	E1	PCI_AD<18>
	AD19	D3	PCI_AD<19>
	AD20	D1	PCI_AD<20>
	AD21	D2	PCI_AD<21>
	AD22	C2	PCI_AD<22>
	AD23	C1	PCI_AD<23>
	AD24	B4	PCI_AD<24>
	AD25	A4	PCI_AD<25>
	AD26	B5	PCI_AD<26>
	AD27	C4	(PCI_AD<27>)
	AD28	A5	PCI_AD<28>
	AD29	C5	PCI_AD<29>
	AD30	B6	PCI_AD<30>
	AD31	A6	PCI_AD<31>
	CBE0	M2	PCI_CBE<0>
	CBE1	J3	PCI_CBE<1>
	CBE2	F1	PCI_CBE<2>
	CBE3	C3	PCI_CBE<3>
	PAR	J4	PCI_PAR
	FRAME	F3	PCI_FRAME_L
	IRDY	F4	PCI_IRDY_L
	TRDY	G1	PCI_TRDY_L
	STOP	G3	PCI_STOP_L
	IDSEL	B3	NEC_IDSEL
	DEVSEL	G2	PCI_DEVSEL_L
	REQ	C6	USB2_PCI_REQ_L
	GNT	D6	USB2_PCI_GNT_L
	PERR	H2	NEC_PCI_PERR_L
	SERR OD	H1	NEC_PCI_SERR_L
	INTA OD	C7	NEC_PCI_INTA_L
	INTB OD	B7	NEC_PCI_INTB_L
	INTC OD	A7	NEC_PCI_INTC_L
	PCLK	A8	CLK33M_USB2
	VBBRST	B8	NEC_IO_RESET_L
	CRUN	N6	NEC_CRUN_L
	PME OD	D9	NEC_PME_L
	VCCRST	C9	NEC_MAIN_RESET_L
	SMI OD	L6	NEC_SMI_L_TP
	LEGC	L7	

VDD_PCI — VDD — AVDD

XT1/SCLK	L9	NEC_XT1	
XT2	P8	NEC_XT2	
RSDM1	M14	NEC_USB_RSDM1	R795 1% 36 402 NEC_USB → NEC_USB_DAM
DM1	M13	(NEC_USB_DAM)	
DP1	L14	(NEC_USB_DAP)	
RSDP1	K13	NEC_USB_RSDP1	→ NEC_USB_DAP
RSDM2	K14	NEC_USB_RSDM2	R792 1% 36 402 NEC_USB
DM2	K12	(NEC_USB_DBM)	
DP2	J14	(NEC_USB_DBP)	
RSDP2	J12	NEC_USB_RSDP2	
RSDM3	H11	RSDM3_TP	R791 1% 36 402 NEC_USB → NEC_USB_DBM
DM3	G11		
DP3	G13		→ NEC_USB_DBP
RSDP3	G14	RSDP3_TP	R790 1% 36 402 NEC_USB
RSDM4	F12	RSDM4_TP	
DM4	F14		
DP4	E12		
RSDP4	E14	RSDP4_TP	
RSDM5	E13	RSDM5_TP	
DM5	D14		
DP5	C13		
RSDP5	C14	RSDP5_TP	
RREF	P11	NEC_RREF	R794 9.09K 1% 1/16W MF 402 → NEC_AVSS_F

Tie to GND at ball N11

LEFT PORT	OCI1	B12	NEC_OCI<1>
RIGHT PORT	OCI2	B11	NEC_OCI<2>
	OCI3	B10	NEC_OCI<3>
	OCI4	A10	NEC_OCI<4>
	OCI5	B9	NEC_OCI<5>
OUT	PPON1	C12	NEC_LEFT_USB_PWREN
OUT	PPON2	A11	NEC_RIGHT_USB_PWREN
OUT	PPON3	C11	NEC_PPON3_TP
OUT	PPON4	C10	NEC_PPON4_TP
OUT	PPON5	A9	NEC_PPON5_TP
	NC1	P6	NEC_NC1_TP
	NC2	M6	NEC_NC2_TP

NEED PULL-UP RESISTORS IN CASE USB 1.0 IS USED FOR PORT POWER

IPD	NTEST1	M8	NTEST1_TP
IPD	SMC	M7	SMC_TP
IPD	TEB	N7	TEB_TP
IPD	AMC	P7	NEC_AMC_TP
IPD	TEST	L8	TEST_TP
	NANDTEST	M10	NEC_NANDTESTEN_TP
	SRCLK	M9	SRCLK_TP
	SRDTA	N9	NEC_NANDTESTOUT_TP
	SRMOD(R)	P9	SRMOD_TP
	AVSS	H11, P13, M12	

R286 0 5% 1/16W MF 603 — NEC_AVSS_F

VSS: B1, N1, P10, N14, H14, B14, A2, B2, N2, N13, B13, M11, L12, H12, D12, G4, J11, F11, D8

INTREPID USB CONSTRAINTS

USB_DAM	USB_DA	5 MIL SPACING	14
USB_DAP	USB_DA	5 MIL SPACING	14
USB_DCM	USB_DC	5 MIL SPACING	14
USB_DCP	USB_DC	5 MIL SPACING	14
USB_D1M	USB_D1	5 MIL SPACING	14 26
USB_D1P	USB_D1	5 MIL SPACING	14 26
USB_D2M	USB_D2	5 MIL SPACING	14 26
USB_D2P	USB_D2	5 MIL SPACING	14 26

SERR_L AND PERR_L HAS DEDICATED PULL-UP FOR BOTH CBUS AND USB2

+3V_MAIN — RP52 10K 5% 1/16W MF SM1 — R783 10K 5% 1/16W MF 402

NEC_PCI_SERR_L — NEC_PCI_PERR_L

R784 22 5% 1/16W MF 402

RP55 47 5% 1/16W SM1

IO_RESET_L	1	8	NEC_IO_RESET_L
PMU_PME_L	2	7	NEC_PME_L
MAIN_RESET_L	3	6	NEC_MAIN_RESET_L
	4	5	

R551 4.7K 5% 1/16W MF 402

Series Rpaks required to facilitate NAND-tree testing

RP54 47 5% 1/16W SM1

USB2_PCI_INT_L	1	8	NEC_PCI_INTA_L
	2	7	NEC_PCI_INTB_L
	3	6	NEC_PCI_INTC_L
	4	5	NEC_LEGC

+3V_MAIN

INTREPID_USB R56 10K 5% 1/16W MF 402 — INTREPID_USB R531 10K 5% 1/16W MF 402 — RP45 10K 5% 1/16W SM1 (5 NEC_USB) — RP45 10K 5% 1/16W SM1 (6 NEC_USB) — R586 10K 5% 1/16W MF 402

R789 1.5K 5% 1/16W MF 402 — R793 1.5K 5% 1/16W MF 402

R84 0 5% 1/16W MF 402 — NEC_USB_DAM → LEFT_USB_DM

R96 0 5% 1/16W MF 402 (INTREPID_USB) — USB_D1M

R83 0 5% 1/16W MF 402 — NEC_USB_DAP → LEFT_USB_DP

R78 0 5% 1/16W MF 402 (INTREPID_USB) — USB_D1P

R545 0 5% 1/16W MF 402 — NEC_USB_DBM → RIGHT_USB_DM

R554 0 5% 1/16W MF 402 (INTREPID_USB) — USB_D2M

R540 0 5% 1/16W MF 402 — NEC_USB_DBP → RIGHT_USB_DP

R530 0 5% 1/16W MF 402 (INTREPID_USB) — USB_D2P

+3V_MAIN

RP45 10K 5% 1/16W SM1 (7 NEC_USB) — RP45 10K 5% 1/16W SM1 (8 NEC_USB)

R591 15K 5% 1/16W MF 402 — NEC_OCI<1> → NEC_LEFT_USB_OVERCURRENT

R600 15K 5% 1/16W MF 402 — NEC_OCI<2> → NEC_RIGHT_USB_OVERCURRENT

C661 0.1uF 20% 10V CERM 402 — C665 0.1uF 20% 10V CERM 402

PLACE NEAR J3

SUTRO CONNECTOR

PLACE NEAR J12

BUBBA CONNECTOR

USB 2.0

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6654 | REV. C

SCALE NONE | SHT 26 OF 44

Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

+3V_MAIN
R633 10K 5% 1/16W MF 402
JTAG_ASIC_TDI 27 39

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0223	338S0079	?	U49	ALT PART

PLACE ALL SERIES RES CLOSE TO PHY

R370 0 5% 1/16W MF 402 — CLKENET_LINK_TX 36 13 — CLKENET_PHY_TX 36
R353 0 5% 1/16W MF 402 — CLKENET_LINK_RX 36 13 — CLKENET_PHY_RX 36
R344 0 5% 1/16W MF 402 — CLKENET_LINK_GBE_REF 36 13 — CLKENET_PHY_GBE_REF 36

U49 88E1111 BCC (CRITICAL)

TX_CLK	4		
RX_CLK	2		
125CLK	22		
TXD0	11	ENET_PHY_TXD<0>	37 13
TXD1	12	ENET_PHY_TXD<1>	37 13
TXD2	14	ENET_PHY_TXD<2>	37 13
TXD3	16	ENET_PHY_TXD<3>	37 13
TXD4	17	ENET_PHY_TXD<4>	37 13
TXD5	18	ENET_PHY_TXD<5>	37 13
TXD6	19	ENET_PHY_TXD<6>	37 13
TXD7	20	ENET_PHY_TXD<7>	37 13
TX_EN	9	ENET_PHY_TX_EN	37 13
TX_ER	7	ENET_PHY_TX_ER	37 13
GTX_CLK	8	CLKENET_PHY_GTX	36 13
RXD0	95	ENET_LINK_RXD<0>	37 13
RXD1	92	ENET_LINK_RXD<1>	37 13
RXD2	93	ENET_LINK_RXD<2>	37 13
RXD3	91	ENET_LINK_RXD<3>	37 13
RXD4	90	ENET_LINK_RXD<4>	37 13
RXD5	89	ENET_LINK_RXD<5>	37 13
RXD6	87	ENET_LINK_RXD<6>	37 13
RXD7	86	ENET_LINK_RXD<7>	37 13
RX_DV	94	ENET_RX_DV	37 13
RX_ER	3	ENET_RX_ER	37 13
CRS	84	ENET_CRS	37 13
COL	83	ENET_COL	37 13
MDC	25	ENET_MDC	37 13
MDIO	24	ENET_MDIO	37 13
INT-/INT+	23	ENET_ENERGY_DET	14
RESET	28	ENET_RST_L	
COMA	27	ENET_COMA	
S_IN+	82 (NC)		
S_IN-	81 (NC)		
S_OUT+	77 (NC)		
S_OUT-	75 (NC)		
S_CLK+	79 (NC)		
S_CLK-	80 (NC)		
HSDAC+	37	ENET_HSDACP	
HSDAC-	38	ENET_HSDACM	
XTAL1	55	CLK25M_ENET_XIN	36
XTAL2	54	CLK25M_ENET_XOUT	36
VSSC	53	ENET_VSSC	
GND	97		
CTRL10	51 (NC)		
DVDD	1, 6, 10, 15, 57, 62, 67, 71, 85		
VDDO	5, 21, 88, 96		
VDDOH	52, 66, 72		
VDDOX	26, 48		
AVDD	32, 35, 36, 40, 45, 78		
MDI0+	29	MDI_P<0>	37
MDI0-	31	MDI_M<0>	37
MDI1+	33	MDI_P<1>	37
MDI1-	34	MDI_M<1>	37
MDI2+	39	MDI_P<2>	37
MDI2-	41	MDI_M<2>	37
MDI3+	42	MDI_P<3>	37
MDI3-	43	MDI_M<3>	37
LED_LINK10	76	LED_LINK10	
LED_LINK100	74	LED_LINK100	
LED_LINK1000	73 (NC)		
LED_DUPLEX	70 (NC)		
LED_RX	69	LED_RX_SPN	
LED_TX	68 (NC)		
CONFIG0	65	(000)	
CONFIG1	64	(000)	
CONFIG2	63	(111)	
CONFIG3	61	(110)	
CONFIG4	60	(111)	
CONFIG5	59	(101)	
CONFIG6	58	(000)	
TDI	44	JTAG_ASIC_TDI	27 39
TDO	50	JTAG_ENET_TDO	13
TCK	49	JTAG_ASIC_TCK	13 39
TMS	46	JTAG_ASIC_TMS	13 39
TRST	47	JTAG_ASIC_TRST_L	13 39
RSET	30	ENET_RSET	
SEL_OSC	56 (NC)		
SEL_2.5V	13		

SEE CONFIG TABLES (BELOW)

+3V_MAIN
C442 10uF 20% 6.3V CERM 805
NO STUFF R333 0 5% 1/16W MF 402
3405_MODE
R319 0 5% 1/16W MF 402
U14 LTC3405 SOT23-6 (CRITICAL)
VIN, RUN, MODE, SW, VFB, GND
LTC3405_SW 38
CRITICAL L5 3.3uH SM1
R334 665K 1% 1/16W MF 402 R2A
C471 22pF 5% 50V CERM 402
R361 49.9K 1% 1/16W MF 402 R2B
3405_VFB
R362 182K 1% 1/16W MF 402 R1
+1_0V_MARVELL 38
C486 10uF 20% 6.3V CERM 805

VOUT = 0.8V*(1+R2EQV/R1)
R2EQV = R2A||R2B

C492 C511 C517 C502 C465 C475 0.1UF 20% 10V CERM 402 / 0.01UF 20% 16V CERM 402
PLACE CAPS (IN ORDER) ON PINS 1, 6, 10/15, 57/62, 67/71, 85

C464 C472 C453 C503 C501 C496 0.1UF 20% 10V CERM 402 / 0.01UF 20% 16V CERM 402 / 10uF 20% 6.3V CERM 805
38 27 +2_5V_MARVELL
PLACE CAPS (IN ORDER) ON PINS 5, 21/26, 48/52, 66/72, 88, 96

+2_5V_MAIN
R465 0 5% 1/16W MF 603
C488 C466 C506 C520 0.1UF 20% 10V CERM 402
PLACE CAPS AT TRANSFORMER PINS 1, 4, 7 & 10

L34 FERR-EMI-600-OHM SM
38 +2_5V_MARVELL_AVDD

C497 C504 C487 C476 0.1UF 20% 16V CERM 402 / 0.01UF 20% 10V CERM 402
C754 10uF 20% 6.3V CERM 805
PLACE CAPS (IN ORDER) ON PINS 32/35, 36/40, 45 & 78

PLACE CLOSE TO ETHERNET CONNECTOR
NO STUFF R438 0 5% 1/10W MF 805
CHGND1

CRITICAL J17 RJ45 RT-TH
13 39 37 RJ45_DP<0>
15 RJ45_C0_PD
14 39 37 RJ45_DN<0>
16 39 37 RJ45_DP<1>
18 RJ45_C1_PD
17 39 37 RJ45_DN<1>
19 39 37 RJ45_DP<2>
21 RJ45_C2_PD
20 39 37 RJ45_DN<2>
22 39 37 RJ45_DP<3>
24 RJ45_C3_PD
23 39 37 RJ45_DN<3>
Short shielded RJ-45
CHGND1

CRITICAL XFR-ENET-1000BT T1 SM

R346 R372 R404 R413 R428 49.9 1% 1/16W MF 402
R355 R381 R406 49.9 1% 1/16W MF 402
MDI0_PD MDI1_PD MDI2_PD MDI3_PD
C454 C477 C493 C505 0.01UF 20% 16V CERM 402
PLACE RESISTORS CLOSE TO PHY

R735 R733 R382 R347 75 5% 1/16W MF 402
ENET_CTAP_CHGND 38
C457 100PF 10% 3KV CERM 1808
CHGND1

D1 1N914 SOT23
Q15 2N7002DW SOT-363
Q15 2N7002DW SOT-363
R371 10K 5% 1/16W MF 402
R345 10K 5% 1/16W MF 402
R354 1.5K 5% 1/16W MF 402
R343 1K 5% 1/16W MF 402
14 INT_ENET_RST_L
30 26 23 17 IO_RESET_L
31 30 29 AC_IN
35 34 33 19 SLEEP_L_LS5
C755 2.2uF 20% 10V CERM 805

PLACES PHY IN "COMA" MODE WHEN ASLEEP ON BATTERY (SAVES POWER)

NO STUFF R435 20K 5% 1/16W MF 402
PUT CRYSTAL CIRCUIT CLOSE TO PHY
R427 0 5% 1/16W MF 402
CRITICAL Y3 25.0000M 8X4.5MM-SM
CLK25M_XTAL_IN
C555 33pF 5% 50V CERM 402
C491 33pF 5% 50V CERM 402
Y3'S LOAD CAPACITANCE IS 20PF

NO STUFF R393 49.9 1% 1/16W MF 402
NO STUFF R403 49.9 1% 1/16W MF 402
R335 10K 5% 1/16W MF 402
R380 4.99K 1% 1/16W MF 402

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0703	197S0037		Y3	
197S0603	197S0037		Y3	ALT FOR SIWARD

CONFIG DEFINITIONS	
PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS			
PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

MARVELL 88E1111

10/100/1000 ETHERNET

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	C
SCALE: NONE	SHT 27 OF 44	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0011	197S0052	?	G1	SIWARD ALT FOR FW OSC

DSX STRAP OPTIONS

0 -> BILINGUAL PORT

1 -> A-ONLY PORT

PLACE NEAR PHY

PLACE NEAR PHY

CAPACITOR IN CONJUCTION WITH INTERNAL PULLUP PROVIDES RESET PULSE WHEN PHY FIRST RECEIVES POWER

FIREWIRE

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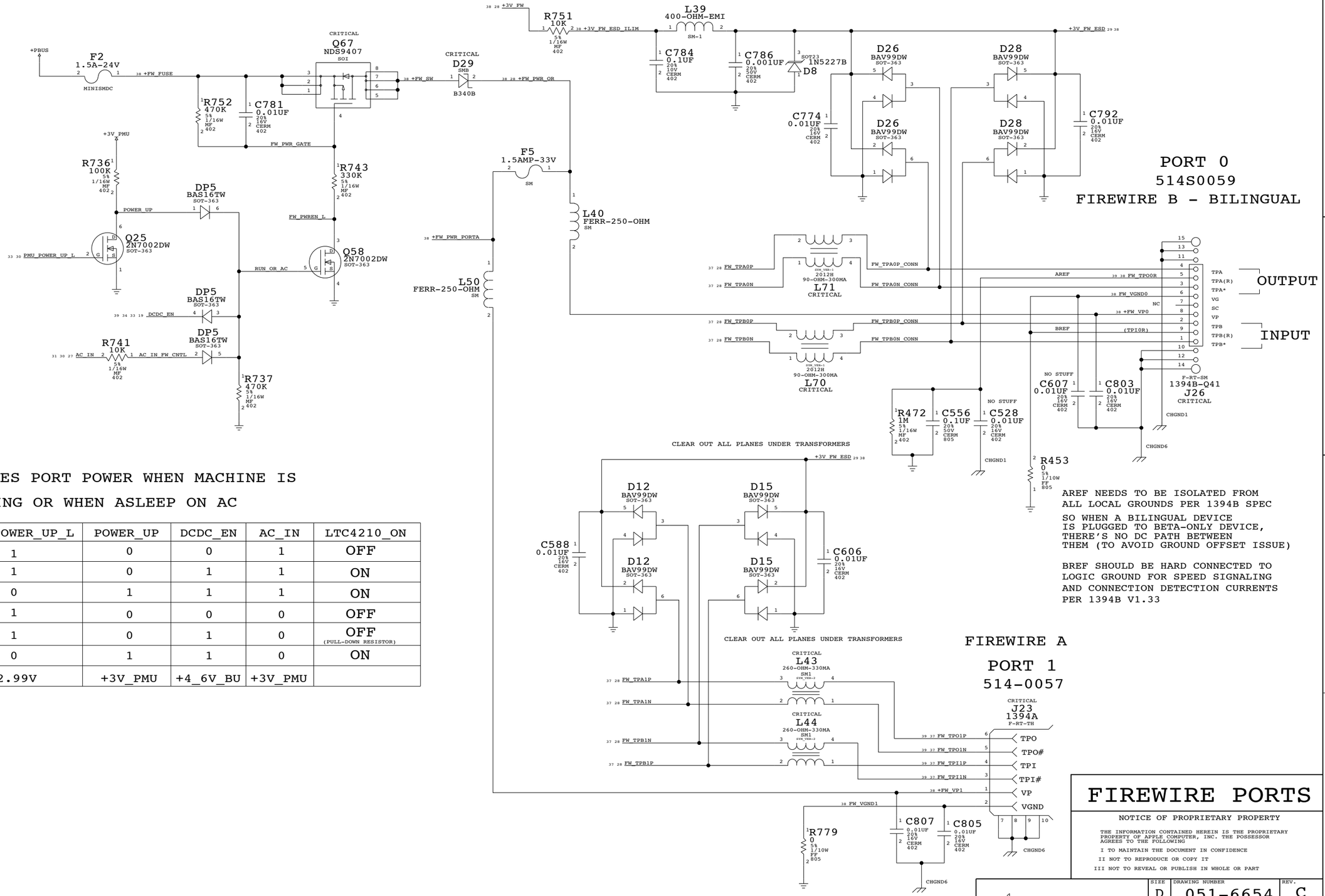
PORT POWER SWITCH



ENABLES PORT POWER WHEN MACHINE IS RUNNING OR WHEN ASLEEP ON AC

STATE	PMU_POWER_UP_L	POWER_UP	DCDC_EN	AC_IN	LTC4210_ON
SHUTDOWN (AC)	1	0	0	1	OFF
SLEEP (AC)	1	0	1	1	ON
RUN (AC)	0	1	1	1	ON
SHUTDOWN (BATT)	1	0	0	0	OFF
SLEEP (BATT)	1	0	1	0	OFF (PULL-DOWN RESISTOR)
RUN (BATT)	0	1	1	0	ON
	2.99V	+3V_PMU	+4_6V_BU	+3V_PMU	

FIREWIRE PORTS

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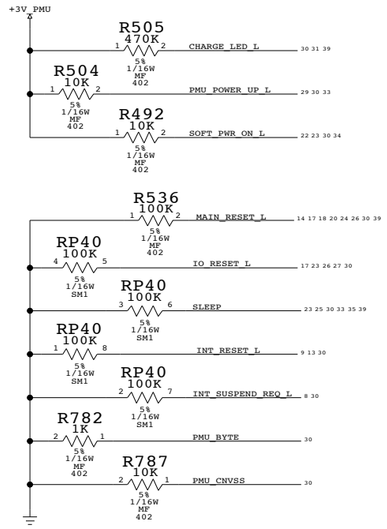
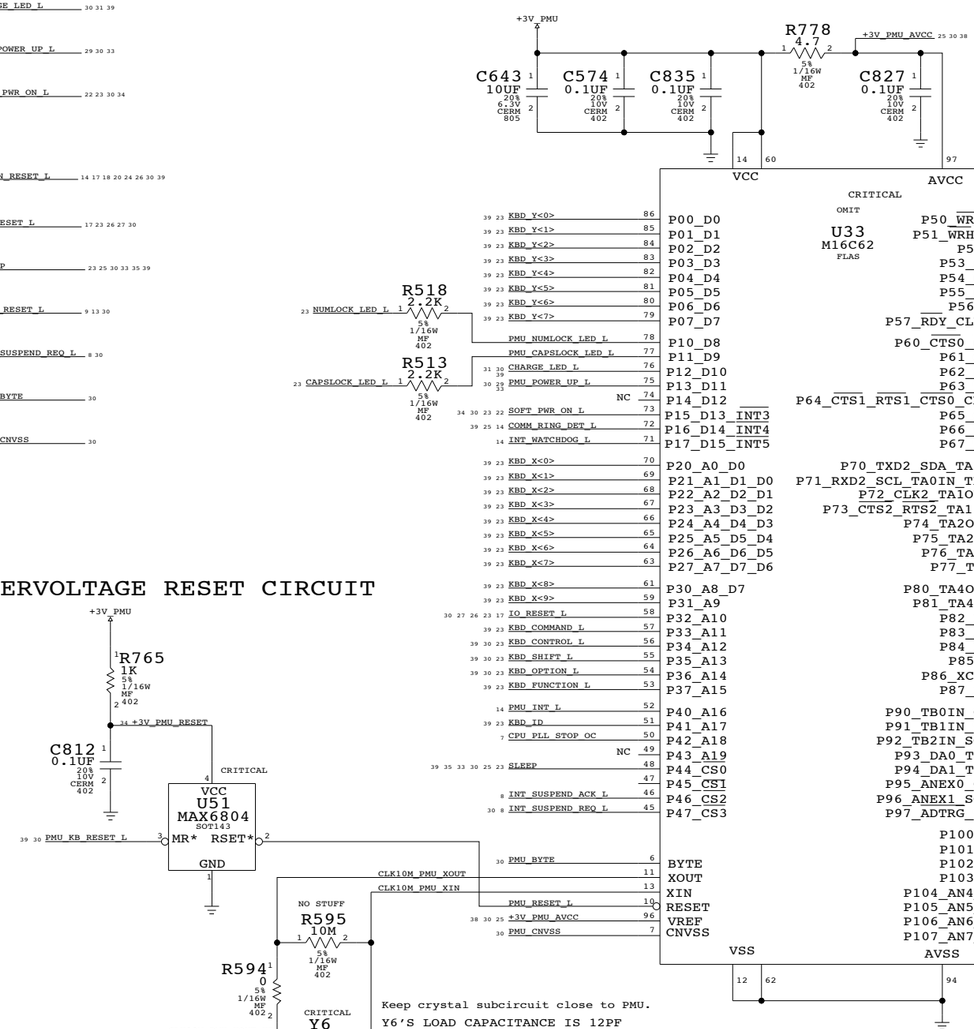
D	051-6654	C
SCALE: NONE	SHT 29 OF 44	

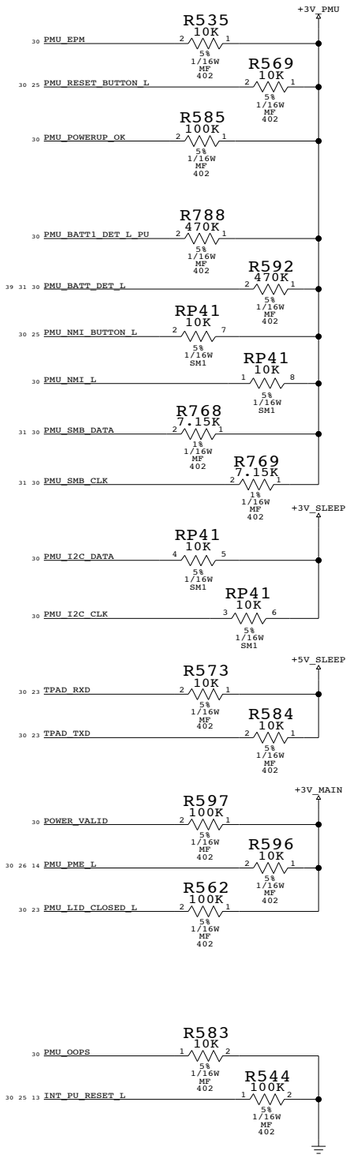




CPU_VCORE_HI_OC/PMU_AP should have a pulldown for coming out of reset. MLB will have a pull-up to +3V_MAIN or +3V_SLEEP, which will act as our pulldown since both are off during PMU reset.

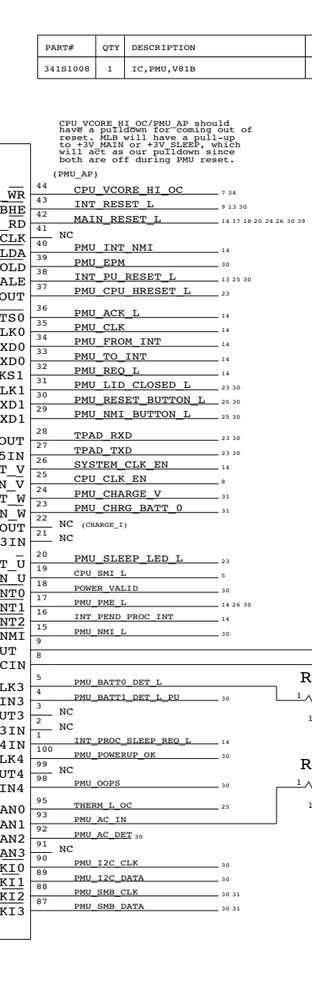
(PMU_AP)

44	CPU_VCORE_HI_OC	7 34
43	INT_RESET_L	9 13 30
42	MAIN_RESET_L	14 17 18 20 24 26 30 39
41	NC	
40	PMU_INT_NMI	14
39	PMU_EPM	30
38	INT_PU_RESET_L	13 25 30
37	PMU_CPU_HRESET_L	23
36	PMU_ACK_L	14
35	PMU_CLK	14
34	PMU_FROM_INT	14
33	PMU_TO_INT	14
32	PMU_REQ_L	14
31	PMU_LID_CLOSED_L	23 30
30	PMU_RESET_BUTTON_L	25 30
29	PMU_NMI_BUTTON_L	25 30
28	TPAD_RXD	23 30
27	TPAD_TXD	23 30
26	SYSTEM_CLK_EN	14
25	CPU_CLK_EN	8
24	PMU_CHARGE_V	31
23	PMU_CHRG_BATT_0	31
22	NC (CHARGE_I)	
21	NC	
20	PMU_SLEEP_LED_L	23
19	CPU_SMI_L	5
18	POWER_VALID	30
17	PMU_PME_L	14 26 30
16	INT_PEND_PROC_INT	14
15	PMU_NMI_L	30

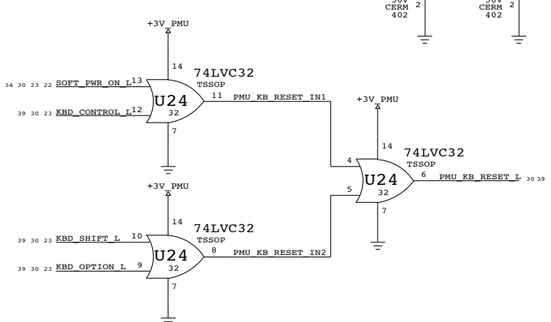


UNDERVOLTAGE RESET CIRCUIT

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0704	197S0041		Y6	ALT CRYSTAL SIZE
197S0604	197S0041		Y6	ALT FOR SIWARD



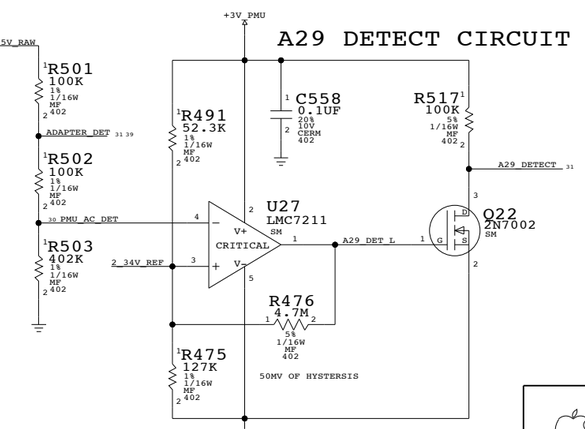
PMU KEYBOARD RESET CIRCUIT



Q11 ADAPTER DETECTION SCHEME

CASE	ADAPTER	PIN VOLT	ID VOLT RANGE	SYSTEM STATUS
1	Q11 (65W)	2.007V- 2.066V	1.65V- 2.31V	RECOGNIZES AS Q11 FULL FUNCTIONS
2	A29 (45W)	2.558V- 2.661V	2.31V- 2.97V	RECOGNIZES AS A29 LIMITED FUNCTIONS
3	AIRLINE	0.589V- 0.663V	0.33V- 0.99V	FULL FUNCTIONS NO BATTERY CHARGING
4	HOOPER	3.19V- 3.28V	2.97V- 3.30V	RECOGNIZES AS HOOPER LIMITED FUNCTIONS

A29 DETECT CIRCUIT



PMU

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SIZE	DRAWING NUMBER	REV.
D	051-6654	C
SCALE: NONE	SHT 30 OF 44	

DC POWER INPUT

(POWER JACK, ETC. ON SEPARATE BOARD)

CRITICAL

J18
87438-0833
M-RT-SM

CHARGE_LED_L
+ADAPTER
ADAPTER_DET

NO STUFF
C757 0.1UF 20% 50V CERM 805

PLACE CLOSE TO DC INPUT

R396 20K 1% 1/16W MF 402

DC INRUSH LIMITER

+ADAPTER_SW
+ADAPTER_SENSE

Q13 SI4435DY SOI
Q16 SI4435DY SOI

R414 330K 5% 1/16W MF 402
C458 0.1UF 20% 50V CERM 805

AC_ENABLE_GATE
AC_ENABLE_L

R374 470K 5% 1/16W MF 402

BCKFD_PROT_GATE
C592 0.1UF 20% 50V CERM 805
R499 68K 5% 1/16W MF 402
BCKFD_PROT_EN_L

Q21 2N7002DW SOT-363

R474 47K 5% 1/16W MF 402

C572 0.01UF 20% 50V CERM 603

+3V_PMU

R395 102K 1% 1/16W MF 402
R364 102K 1% 1/16W MF 402
C468 0.01UF 20% 16V CERM 402
R363 10K 5% 1/16W MF 402

1V20_REF
AC_DIV
AC_IN
AC_IN_L

U15 LMC7211 SM
CRITICAL

R394 1M 5% 1/16W MF 402
R375 10K 1% 1/16W MF 402
R365 57.6K 1% 1/16W MF 402

Q10 2N7002DW SOT-363
Q10 2N7002DW SOT-363

R383 470K 5% 1/16W MF 402

GREATER THAN 13.5V DETECT

PLACE U23 NEXT TO R460

U23 SENSE VOLTAGE DROP ACROSS R460

U23 MAX4172 TSSOP
CRITICAL
RS+ RS- PG NC1 NC2 OUT GND NC NC

+24V_PBUS
MAX4172_OUT
CURRENT_THRESHOLD

R454 2.21K 0.1% 1/16W MF 603-1
C883 0.1UF 10% 50V X7R 603-1

R460 0.025 1% 1W MF 2512

IF A29 ADAPTER USED, ADJUST CURRENT SETTING

R488 4.7 5% 1/16W MF 402
R498 4.7 5% 1/16W MF 402

1772_CSSP
1772_CSSN

C578 0.47UF 10% 50V CERM 1206
C579 0.47UF 10% 50V CERM 1206

R754 100K 1% 1/16W MF 402
D9 1N914 SOT23
R755 12.7K 1% 1/16W MF 402
C600 1UF 20% 50V CERM1 1210

1772_DCIN
1772_ACIN
1772_ACOK_L
(+3V_PMU)
1772_VCTL
1772_ICTL
1772_ICHG
1772_IINP

U31 MAX1772 QSOP
CRITICAL
CSSP CSSN DCIN ACIN ACOK RFIN VCTL ICTL ICHG IINP CELLS LDO DLOV BST DHI LX DLO PGND CSIP CSIN BATT CCV CCI CCS REF GND

1772_CELLS
1772_DLOV
1772_BST
1772_DHI
1772_LX
1772_DLO
(GND)
1772_CSIP
1772_CSIN

REF = 4.096V
REF_CLS

OD OUTPUT LOW - WHEN AC GREATER THAN 18V

R526 1K 1% 1/16W MF 402
C622 0.01UF 10% 16V CERM 402
C616 0.01UF 10% 16V CERM 402
1772_CCV_RC
C621 0.1UF 20% 10V CERM 402
R497 1K 1% 1/16W MF 402
1772_REF
C630 1UF 20% 10V CERM 603
R487 10K 1% 1/16W MF 402
R473 4.12K 1% 1/16W MF 402
1772_CLS

C652 1UF 20% 10V CERM 603
C817 0.1UF 20% 25V CERM 603
C802 0.1UF 20% 25V CERM 603

R559 100K 5% 1/16W MF 402

1772_GND
+BATT_VSNS

1MSEC INTEGRATION TIME

R742 1K 1% 1/16W MF 402
C771 0.1UF 20% 10V CERM 402
IAC_RC_COMP

R747 42.2K 0.1% 1/16W FF 603
C772 0.1UF 20% 10V CERM 402

U50 LMC7111 SOT23-5
CRITICAL
IAC_FB

PLACE R358 CLOSE TO LTC1625
ROUTE LTC1625_ITH CAREFULLY

LTC1625_ITH
DP4 BAS16TW SOT-363
R358 150 1% 1/16W MF 402
1625_COMP
ADAPTER_I_REG

R466 10K 1% 1/16W MF 402

R738 42.2K 0.1% 1/16W FF 603
R734 82.5K 0.1% 1/16W FF 603
A29_CURRENT_ADJ

R739 51.1K 0.1% 1/16W FF 603
IF ADAPTER IS OVER 18V, ADJUST CURRENT SETTING

R748 100K 5% 1/16W MF 402
OVER_18V_ADJ

Q20 2N7002DW SOT-363
A29_DETECT
Q20 2N7002DW SOT-363
AC_GTR_18V

C775 1UF 20% 10V CERM 603

Q65 2N7002DW SOT-363
1772_ACOK_L

R571 33 5% 1/8W FF 1206
D10 1N914 SOT23
1772_BST_ESR

R549 100K 5% 1/16W MF 402
C624 0.1UF 20% 25V CERM 603

R774 4.7 5% 1/16W MF 603

C608 0.1UF 20% 50V CERM 805

BATTERY SWITCH-OVER CIRCUIT

+BATT
F4 5AMP-125V SM-2
F3 5AMP-125V SM-2

+24V_PBUS
+PBUS
+BATT_24V_FUSE
+BATT_14V_FUSE

CRITICAL
Q24 SI4435DY SOI
Q76 SUD45P03 TO-252

R490 47K 5% 1/16W MF 402
R746 47K 5% 1/16W MF 402
BATT_14V_GATE
BATT_24V_GATE

R512 10K 5% 1/16W MF 402
R744 10K 5% 1/16W MF 402

DP4 BAS16TW SOT-363
BATT_24PBUS_EN
BATT_14PBUS_EN

Q21 2N7002DW SOT-363

AC_IN_L
DP4 BAS16TW SOT-363
R489 158K 1% 1/16W MF 402
AC_IN_L_RC
C593 10UF 20% 6.3V CERM 805

WHEN AC IS IN, P-CHANNEL FETS ARE QUICKLY (DIODE) TURNED OFF
WHEN AC IS NOT PLUGGED, P-CHANNEL FETS ARE ON
RC TIME IS 480K*10UF @ +3V_PMU

SWITCHER VOLTAGE CONTROL

PMU SELECTS BETWEEN TWO VOLTAGES

+3V_PMU

R567 27.4K 1% 1/16W MF 402
R558 10K 1% 1/16W MF 402
R548 10K 1% 1/16W MF 402
R560 4.12K 1% 1/16W MF 402
R565 48.7K 1% 1/16W MF 402
R566 1K 1% 1/16W MF 402
R542 1K 1% 1/16W MF 402

BATTV_HIGH
BATTV_LOW
BATT_LOW_L

R561 100K 5% 1/16W MF 402
Q27 2N7002DW SOT-363
R580 5.23K 1% 1/16W MF 402
Q27 2N7002DW SOT-363
PMU_CHARGE_V

Q29 2N7002DW SOT-363
Q29 2N7002DW SOT-363

SWITCHER CURRENT CONTROL

CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V
CHARGE THROTTLED BY LOW BATTERY VOLTAGE

+3V_PMU

R578 100K 5% 1/16W MF 402
CHARGE_DISABLE
Q30 2N7002DW SOT-363
Q30 2N7002DW SOT-363
PMU_CHRG_BATT_0

C615 0.1UF 20% 10V CERM 402

U38 LMC7211 SM
CRITICAL
BATT_LOW

R588 100K 1% 1/16W MF 402
R579 499K 1% 1/16W MF 402
BATT_DIV
1V65_REF
R599 100K 1% 1/16W MF 402
R570 100K 1% 1/16W MF 402
C658 0.047uF 10% 16V CERM 402

R749 6.34K 1% 1/16W MF 402
A29_CLS_ADJ
Q65 2N7002DW SOT-363
A29_DETECT

$V_{BATT} = CELLS \times (4.096 + (0.4096 * V_{VCTL} / V_{REFIN}))$

For 4.15V cells, VCTL = 0.123 REFIN

For 4.20V cells, VCTL = 0.245 REFIN

$I_{CHG} = (0.2048/R_{62}) * (V_{ICTL} / V_{REFIN})$

BATTERY CONNECTOR

CRITICAL
J25
87438-0833
M-RT-SM

+BATT_POS
(BATT_IN_PD)
BATT_CLK
BATT_DATA
PMU_BATT_DET_L
BATT_NEG

L9 FERR-EMI-100-OHM SM
L53 FERR-50-OHM SM
L10 FERR-EMI-100-OHM SM
PMU_SMB_CLK
L8 FERR-EMI-100-OHM SM
PMU_SMB_DATA
L12 FERR-50-OHM SM

+24V_PBUS

Q63 IRF7805 SM
CRITICAL

C547 2.2UF 10% 25V CERM 1812
C562 2.2UF 10% 25V CERM 1812
C563 2.2UF 10% 25V CERM 1812
C557 2.2UF 10% 25V CERM 1812
C564 2.2UF 10% 25V CERM 1812

+BATT_RSNS
L42 10uH SM1
CRITICAL
R763 0.05 1% 1W MF 2512

D30 MBRS140T3 SM

Q64 IRF7811W SO-8
CRITICAL

NO STUFF
C906 0.0022UF 10% 50V CERM 402

XW19 SM

R543 1 5% 1/16W MF 603
R511 1 5% 1/16W MF 603

C619 4.7UF 20% 25V CERM 1206
C632 4.7UF 20% 25V CERM 1206
C617 4.7UF 20% 25V CERM 1206
C824 33UF 20% 25V ELEC SM1
C631 4.7UF 20% 25V CERM 1206
C633 4.7UF 20% 25V CERM 1206
C618 4.7UF 20% 25V CERM 1206

BATTERY CHARGER

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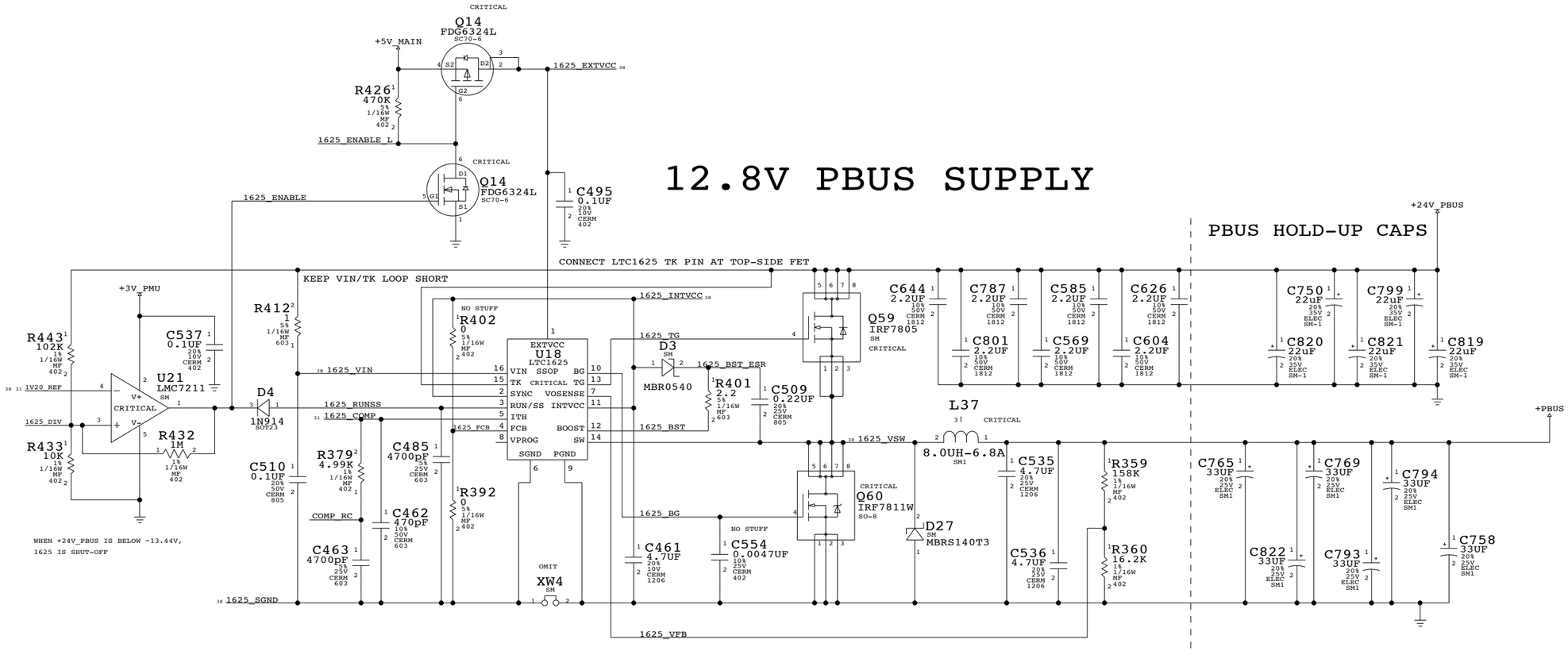
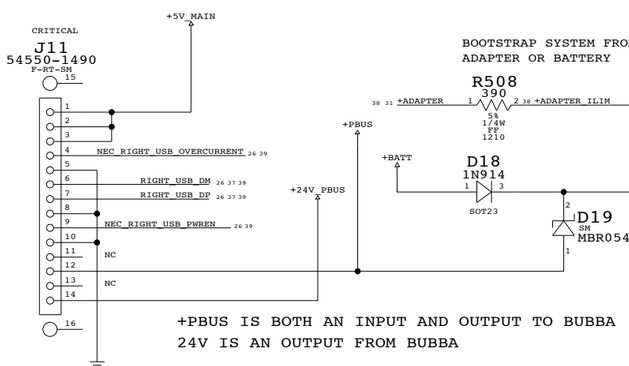
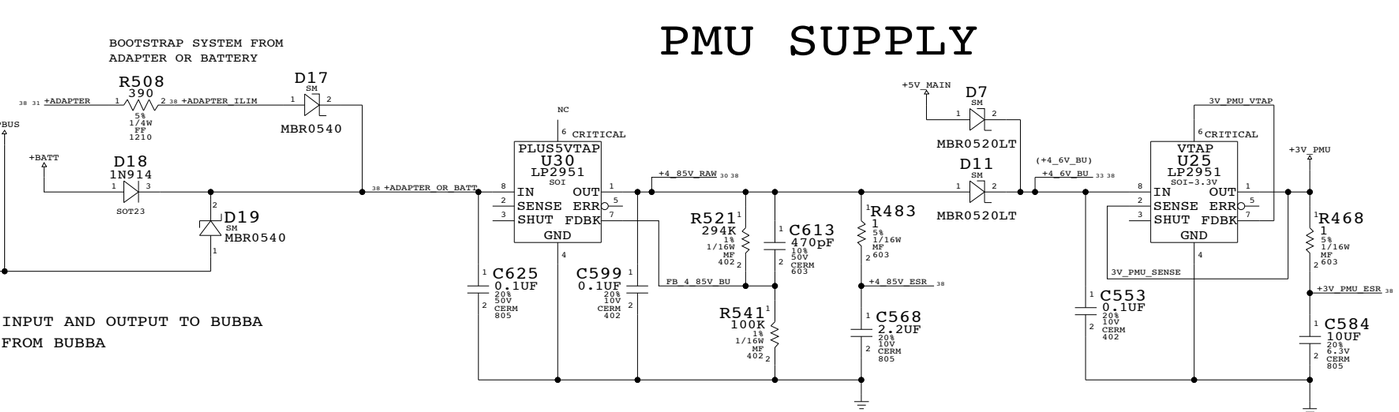
SCALE: NONE	SHT 31 OF 44	

12.8V PBUS SUPPLY



BACKUP BATTERY / USB CONNECTOR





PMU SUPPLY

12.8V REGULATOR

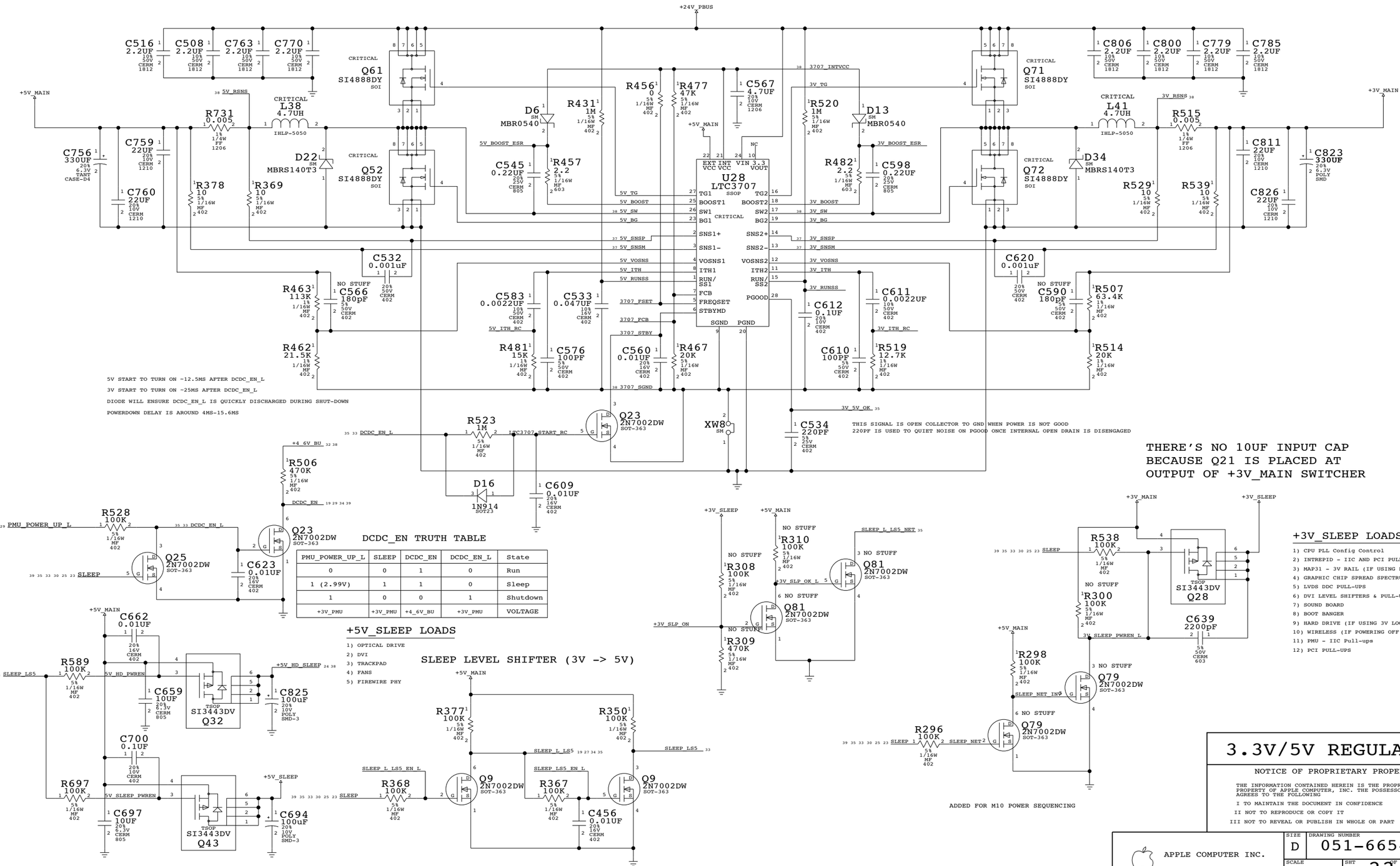
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	C

SCALE: NONE

SHT 32 OF 44

3.3V/5V MAIN SUPPLY



3.3V/5V REGULATOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	C
SCALE: NONE	SHT 33 OF 44	

VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage
(approx. 7ms delay)

1.175V -> 1.025V 1.30V -> 0.975V

SEL = 0; Y1=A1
SEL = 1; Y1=B1

Keep trace fat (40-100 mils) and short!!

MAX1717 VID CAN TAKE 3.3V TO 5.5V INPUTS

Connect MAX1717 GND pin 13 to GND at bottom-side FET

Keep trace fat and short!!

Keep trace fat and short!!

Keep trace fat and short!!

PLACE THIS SHORT AT PIN OF 1000uF CAP CLOSEST TO CPU

ROUTE AS DIFFERENTIAL PAIR

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V WITH A 0.85 SCALE FACTOR, HENCE VOFFSET = 1.7V * (R1/(R1+R2)) AND VCORE = VDAC + VOFFSET.

NOTE: R310 (R2) NO STUFFED FOR NO OFFSET CASE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0022	128S0034	?	C728,C729,C730,C731,C732,C733,C734,C884,C885	

OUTPUT VOLTAGE

V_{DAC} D4=0	V_{DAC} D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	A/B_ = Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1

If all pull-ups are >=100K and all pull-downs are <=1K, $V_A = V_B$.

FMAX CONNECTOR

J5
M-ST-SM-52465-1217

VCORE SUPPLY

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SCALE: NONE	SHT 34 OF 44	

1.5V/2.5V SWITCHER

+1_5V_SLEEP LOADS

1) AGP I/O - IF USING D3COLD
2) MAXBUS I/O - IF 1.5V INTERFACE

+1_5V_MAIN LOADS

1) INTREPID CORE
2) AGP I/O IF USING D3HOT

+2_5V_MAIN LOADS

1) MAP31 - FBCORE/FBIO IF USING D3HOT
2) GIGABIT ETHERNET - AVDDL
3) DDR SODIMMS - CORE/IO
4) DDR MUXES
5) CLOCK SLEWING I/O
6) PCI1510 CORE

+2_5V_SLEEP LOADS

1) FBCORE/FBIO IF USING D3COLD
2) INTREPID MEMORY I/O

THERE'S 100K PULL-UP ON PG 31 ALREADY

DIODE PROVIDE PROVIDE QUICK SHUT-DOWN
POWER DOWN DELAY 1.5MS TO 3.5MS

CHANGE R424 BACK TO 10K, 1%, AND STUFF 5.11K FOR 1.5V OPERATION
CONNECTING 1_5V_FB TO GND, FORCES 1.8V OUTPUT

1.8V SWITCHER

+1_8V_MAIN LOADS

1) INTREPID PLLS

+1_8V_SLEEP LOADS

1) MPC7450 - MAXBUS I/O - IF 1.8V INTERFACE
2) CPU JTAG & MaxBus Pull-ups
3) CPU PLL Config Straps
4) OPTIONAL VIDEO MEMORY (M10 PRO ONLY)

1.5V/1.8V/2.5V SUPPLIES

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	C
SCALE: NONE	SHT 35 OF 44	

DIGITAL SIGNALS

GROUP	SIG_NAME		MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
MAXBUS	CPU_AACK_L				250.0000	10_MIL_SPACING			5 8
	CPU_ADDR<0..31>		5		250			83_MHZ	5 8
	CPU_ARTRY_L				250.0000	10_MIL_SPACING			5 8
	CPU_BG_L				250.0000	10_MIL_SPACING			5 8
	CPU_BR_L				250.0000	10_MIL_SPACING			5 8
	CPU_CI_L		5		250.0000				5 8
	CPU_DATA<0..31>		5		250			83_MHZ	6 8
	CPU_DATA<32..63>		5		250			83_MHZ	6 8
	CPU_DBG_L		5		250.0000	10_MIL_SPACING			5 8
	CPU_DTI<0..2>		5		250				5 8
	CPU_DRDY_L_UF					10_MIL_SPACING			
	CPU_DRDY_L				250.0000	10_MIL_SPACING			5 8
	CPU_GBL_L		5		250.0000				5 8
	CPU_HIT_L				250.0000	10_MIL_SPACING			5 8
	CPU_QACK_L		5		250.0000	10_MIL_SPACING			5 8
	CPU_QREQ_L				250.0000	10_MIL_SPACING			5 8
	CPU_TA_L				250.0000	10_MIL_SPACING			5 8
	CPU_TBST_L		5		250.0000	10_MIL_SPACING			5 8
	CPU_TEA_L				250.0000				5 8
	CPU_TS_L				250.0000	10_MIL_SPACING			5 8
	CPU_TSIZ<0..2>		5		250				5 8
	CPU_TT<0...4>		5		250				5 8
	CPU_WT_L		5		250.0000				5 8
GROUP 0	MEM_DATA<7..0>		4		200			167_MHZ	9 10
	RAM_DATA_A<7..0>		4		200			167_MHZ	10 11
	RAM_DATA_B<7..0>		4		200			167_MHZ	10 11
	MEM_DQS<0>	TOTAL LENGTH CONTROLLED BY SPREADSHEET			200				9 10
	RAM_DQS_A<0>		4		200				10 11
	RAM_DQS_B<0>		4		200				10 11
	MEM_DQM<0>		4		200				9 10
	RAM_DQM_A<0>		4		200				10 11
	RAM_DQM_B<0>		4		200				10 11
GROUP 1	MEM_DATA<15..8>		4		200			167_MHZ	9 10
	RAM_DATA_A<15..8>		4		200			167_MHZ	10 11
	RAM_DATA_B<15..8>		4		200			167_MHZ	10 11
	MEM_DQS<1>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200				9 10
	RAM_DQS_A<1>		4		200				10 11
	RAM_DQS_B<1>		4		200				10 11
	MEM_DQM<1>				200				9 10
	RAM_DQM_A<1>		4		200				10 11
	RAM_DQM_B<1>		4		200				10 11
GROUP 2/3	MEM_DATA<31..16>		4		200			167_MHZ	9 10
	RAM_DATA_A<31..16>		4		200			167_MHZ	10 11
	RAM_DATA_B<31..16>		4		200			167_MHZ	10 11
	MEM_DQS<3..2>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200			167_MHZ	9 10
DDR RAM	RAM_DQS_A<3..2>		4		200			167_MHZ	10 11
	RAM_DQS_B<3..2>		4		200			167_MHZ	10 11
	MEM_DQM<3..2>		4		200			167_MHZ	9 10
	RAM_DQM_A<3..2>		4		200			167_MHZ	10 11
	RAM_DQM_B<3..2>		4		200			167_MHZ	10 11
GROUP 4/5	MEM_DATA<47..32>		4		200			167_MHZ	9 10
	RAM_DATA_A<47..32>		4		200			167_MHZ	10 11
	RAM_DATA_B<47..32>		4		200			167_MHZ	10 11
	MEM_DQS<5..4>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200			167_MHZ	9 10
	RAM_DQS_A<5..4>		4		200			167_MHZ	10 11
	RAM_DQS_B<5..4>		4		200			167_MHZ	10 11
	MEM_DQM<5..4>		4		200			167_MHZ	9 10
	RAM_DQM_A<5..4>		4		200			167_MHZ	10 11
	RAM_DQM_B<5..4>		4		200			167_MHZ	10 11
GROUP 6	MEM_DATA<55..48>		4		200			167_MHZ	9 10
	RAM_DATA_A<55..48>		4		200			167_MHZ	10 11
	RAM_DATA_B<55..48>		4		200			167_MHZ	10 11
	MEM_DQS<6>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200				9 10
	RAM_DQS_A<6>				200				10 11
	RAM_DQS_B<6>		4		200				10 11
	MEM_DQM<6>				200				9 10
	RAM_DQM_A<6>		4		200				10 11
	RAM_DQM_B<6>		4		200				10 11
GROUP 7	MEM_DATA<63..56>		4		200			167_MHZ	9 10
	RAM_DATA_A<63..56>		4		200			167_MHZ	10 11
	RAM_DATA_B<63..56>		4		200			167_MHZ	10 11
	MEM_DQS<7>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200				9 10
	RAM_DQS_A<7>				200				10 11
	RAM_DQS_B<7>				200				10 11
	MEM_DQM<7>		4		200				9 10
	RAM_DQM_A<7>		4		200				10 11
	RAM_DQM_B<7>		4		200				10 11
ADDR	MEM_ADDR<12..0>		4					83_MHZ	9
	RAM_ADDR<12..0>		6		200				9 11
CONTROL	MEM_BA<1..0>		4						9
	RAM_BA<1..0>		6		200				9 11
	MEM_CS_L<3..0>		4						9
	RAM_CS_L<3..0>		6		200				9 11
	MEM_CKE<3..0>		4						9
	RAM_CKE<3..0>		6		200				9 11
	MEM_RAS_L		4						9
	RAM_RAS_L				200.0000				9 11
	MEM_CAS_L		4						9
	RAM_CAS_L				200.0000				9 11
	MEM_WE_L		4						9
	RAM_WE_L				200.0000				9 11
	MEM_MUXSEL_H<1..0>		3						9 10
	MEM_MUXSEL_L<1..0>		3						9 10
	RAM_MUXSEL_H		5						10
	RAM_MUXSEL_L		5						10

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME			MAX VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM	
INTREPID CLOCKS	SYSCLK_CPU_UF						10_MIL_SPACING		8
	SYSCLK_CPU			4		200.0000	10_MIL_SPACING		5 8
	INT_CPUFB_OUT			3			10_MIL_SPACING		8
	INT_CPUFB_OUT_SHORT			3			10_MIL_SPACING		8
	INT_CPUFB_OUT_NORM			3			10_MIL_SPACING		8
	INT_CPUFB_IN_NORM			3			10_MIL_SPACING		8
	INT_CPUFB_LONG			3			10_MIL_SPACING		8
	INT_CPUFB_IN					200.0000	10_MIL_SPACING		8
	SYSCLK_DDRCLK_A0_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_A0_L_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_A1_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_A1_L_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_B0_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_B0_L_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_B1_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_B1_L_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_A0	DDRCLK_A0		3		200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_A0_L	DDRCLK_A0				200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_A1	DDRCLK_A1		3		200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_A1_L	DDRCLK_A1				200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_B0	DDRCLK_B0		3		200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_B0_L	DDRCLK_B0		3		200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_B1	DDRCLK_B1		3		200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_B1_L	DDRCLK_B1		3		200.0000	10_MIL_SPACING		9 11
	INT_REF_CLK_OUT			3		200.0000	10_MIL_SPACING		14
	INT_REF_CLK_IN					200.0000	10_MIL_SPACING		14
	CLK66M_GPU_AGP_UF					200.0000	10_MIL_SPACING		12
	CLK66M_GPU_AGP			4		200.0000	10_MIL_SPACING		12 18
	INT_AGP_FB_OUT					200.0000	10_MIL_SPACING		12
	INT_AGP_FB_IN			4		200.0000	10_MIL_SPACING		12
	CLK33M_CBUS_UF					200.0000	10_MIL_SPACING		12
	CLK33M_CBUS	SHOULD BE AT MOST 4 VIAS FOR CLK		6		200.0000	10_MIL_SPACING		12 17
	CLK33M_AIRPORT_UF					200.0000	10_MIL_SPACING		12
	CLK33M_AIRPORT	SHOULD BE AT MOST 4 VIAS FOR CLK		6		200.0000	10_MIL_SPACING		12 24 39
	CLK33M_USB2_UF					200.0000	10_MIL_SPACING		12
	CLK33M_USB2	SHOULD BE AT MOST 4 VIAS FOR CLK		6		200.0000	10_MIL_SPACING		12 26
	INT_PCI_FB_OUT					200.0000	10_MIL_SPACING		12
	INT_PCI_FB_IN			3		200.0000	10_MIL_SPACING		12
MAP31	GPU_CLK27M_OUT						10_MIL_SPACING		
	GPU_CLK27M_UF						10_MIL_SPACING		
	GPU_SSCLK_UF						10_MIL_SPACING		
	GPU_SSCLK_IN						10_MIL_SPACING		
	GPU_FBCLK0						10_MIL_SPACING		
	GPU_FBCLK0_L						10_MIL_SPACING		
	GPU_FBCLK1						10_MIL_SPACING		
	GPU_FBCLK1_L						10_MIL_SPACING		
	GPU_DVO_CLKP						10_MIL_SPACING		19 20
CRYSTALS	CLK27M_GPU_XOUT						10_MIL_SPACING		
	CLK27M_XTAL_IN						10_MIL_SPACING		
	CLK27M_GPU_XIN						10_MIL_SPACING		
	CLK18M_INT_XIN						10_MIL_SPACING		14
	CLK18M_INT_XOUT						10_MIL_SPACING		14
	CLK18M_XTAL_IN						10_MIL_SPACING		14
	CLK18M_INT_EXT						10_MIL_SPACING		14
	CLK25M_ENET_XIN						10_MIL_SPACING		27
	CLK25M_ENET_XOUT						10_MIL_SPACING		27
	NEC_XT1						10_MIL_SPACING		26
	NEC_XT2	THERE'S ANOTHER 280MIL LEG					10_MIL_SPACING		26
SOUND	SND_SCLK			7		200.0000	10_MIL_SPACING		14 25 39
	SND_CLKOUT					200.0000	10_MIL_SPACING		14 25 39
ETHERNET MARVELL	CLKENET_PHY_RX					200.0000			27
	CLKENET_LINK_RX			3		200.0000	10_MIL_SPACING		13 27
	CLKENET_PHY_GBE_REF					200.0000			27
	CLKENET_LINK_GBE_REF			3		200.0000	10_MIL_SPACING		13 27
	CLKENET_PHY_TX					200.0000			27
	CLKENET_LINK_TX			5		200.0000	10_MIL_SPACING		13 27
	CLKENET_LINK_GTX					200.0000			13
	CLKENET_PHY_GTX			3		200.0000	10_MIL_SPACING		13 27
FIREWIRE	CLKFW_PHY_PCLK					200.0000			28
	CLKFW_LINK_PCLK			3		200.0000	10_MIL_SPACING		13 28
	CLKFW_PHY_LCLK			3		200.0000	10_MIL_SPACING		13 28
	CLKFW_LINK_LCLK					200.0000			13
	FW_XI					200.0000	10_MIL_SPACING		28
	FW_OSC					200.0000	10_MIL_SPACING		28

SIGNAL CONSTRAINTS - PAGE 1

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	C
SCALE: NONE	SHT 36 OF 44	

Digital Signals (cont'd)

GROUP	SIG_NAME	DELAY_RULE	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
AGP	AGP_AD<15..0>		5	100				66_MHz	12 18
AGP BYTES 0-1	AGP_CBE<1..0>		5	100				66_MHz	12 18
	AGP_AD_STB<0>		5	100		8_MIL_SPACING			12 18
	AGP_AD_STB_L<0>		5	100		8_MIL_SPACING			12 18
AGP BYTES 2-3	AGP_AD<31..16>		5	100				66_MHz	12 18
	AGP_CBE<3..2>		5	100				66_MHz	12 18
	AGP_AD_STB<1>		5	100		8_MIL_SPACING			12 18
	AGP_AD_STB_L<1>			100		8_MIL_SPACING			12 18
AGP SIDEBAND	AGP_SBA<7..0>		5	100				66_MHz	12 18
	AGP_SB_STB			100.0000		8_MIL_SPACING			12 18
	AGP_SB_STB_L		5	100.0000		8_MIL_SPACING			12 18
AGP CONTROL	AGP_FRAME_L			250.0000					12 18
	AGP_IRDY_L			250.0000					12 18
	AGP_TRDY_L		6	250.0000					12 18
	AGP_DEVSEL_L			250.0000					12 18
	AGP_STOP_L		6	250.0000					12 18
	AGP_PAR		6	250.0000					12 18
	AGP_REQ_L			285.0000					12 18
	AGP_GNT_L			250.0000					12 18
	AGP_RBF_L			250.0000					12 18
DVO	GPU_DVOD<0..11>		5	250					19 20
	GPU_DVO_HSYNC								19 20
	GPU_DVO_VSYNC								19 20
PCI	PCI_AD<31..0>					MIN_DAISY_CHAIN		33_MHz	9 12 17 24 26 39
	PCI_CBE<3..0>					MIN_DAISY_CHAIN		33_MHz	12 17 24 26 39
	PCI_FRAME_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_IRDY_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_TRDY_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_DEVSEL_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_STOP_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_PAR					MIN_DAISY_CHAIN			12 17 24 26 39
ULTRA ATA-100	UIDE_DATA<15..8>			NEED TO MATCH DELAY TO 250	200			100_MHz	13 24
	UIDE_DATA<7>				200				13 24
	UIDE_DATA<6..0>				200			100_MHz	13 24
	UIDE_ADDR<2..0>				200			100_MHz	13 24
	UIDE_RST_L				200.0000				13 24
	UIDE_DIOW_L				200.0000				13 24
	UIDE_DIOR_L			10_MIL_SPACING	200.0000				13 24
	UIDE_DMACK_L				200.0000				13 24
	UIDE_CS0_L				200.0000				13 24
	UIDE_CS1_L				200.0000				13 24
	UIDE_DMARQ				200.0000				13
	UIDE_IOCHRDY			10_MIL_SPACING	200.0000				13 24
	UIDE_INTRQ				200.0000				13
	HD_DATA<15..0>		5	TOTAL UIDE+HD SKEW <500MIL	200			100_MHz	24
	HD_ADDR<2..0>		5		200			100_MHz	24
	HD_RESET_L		5		200.0000				24
	HD_DIOW_L		5		200.0000				24
	HD_DIOR_L		5	10_MIL_SPACING	200.0000				24
	HD_DMACK_L		5		200.0000				24
	HD_CS0_L		5		200.0000				24
	HD_CS1_L		5		200.0000				24
	HD_DMARQ				200.0000				13 24
	HD_IOCHRDY		5	10_MIL_SPACING	200.0000				24
	HD_INTRQ		5						13 24
EIDE INTREPID	EIDE_DATA<15..0>							33_MHZ	13 24
	EIDE_ADDR<2..0>							33_MHZ	13 24
	EIDE_CS0_L								13 24
	EIDE_CS1_L								13 24
	EIDE_RD_L								13 24
	EIDE_WR_L								13 24
	EIDE_IOCHRDY								13 24
	EIDE_INT								13 24
	EIDE_RST_L								13 24
	EIDE_DMACK_L								13 24
	EIDE_DMARQ								13 24
OPTICAL	EIDE_OPTICAL_DATA<15..0>							33_MHZ	24 39
	EIDE_OPTICAL_ADDR<2..0>							33_MHZ	24 39
	EIDE_OPTICAL_CS0_L								24 39
	EIDE_OPTICAL_CS1_L								24 39
	EIDE_OPTICAL_RD_L								24 39
	EIDE_OPTICAL_WR_L								24 39
	EIDE_OPTICAL_IOCHRDY								24 39
	EIDE_OPTICAL_INT								24 39
	EIDE_OPTICAL_RST_L								24 39
	EIDE_OPTICAL_DMAACK_L								24 39
	EIDE_OPTICAL_DMA_RQ								24 39
ETHERNET MII	ENET_LINK_RXD<7..0>		5						13 27
	ENET_RX_DV								13 27
	ENET_RX_ER								13 27
	ENET_PHY_TXD<7..0>		5						13 27
	ENET_LINK_TXD<7..0>								13
	ENET_PHY_TX_ER		5						13 27
	ENET_LINK_TX_ER								13
	ENET_PHY_TX_EN		5						13 27
	ENET_LINK_TX_EN								13
	ENET_MDIO								13 27
	ENET_MDC								13 27
	ENET_COL								13 27
	ENET_CRS								13 27
FIREWIRE MII	FW_LINK_DATA<7..0>		5						13 28
	FW_PHY_DATA<7..0>		5						28
	FW_LINK_CNTL<1..0>								13 28
	FW_PHY_CNTL<1..0>								28
	FW_LINK_LREQ								13
	FW_PHY_LREQ								13 28
	FW_PINT								13 28

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR		MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS	
ETHERNET	MDI_M<0>	ENET_MDI0					27
	MDI_P<0>	ENET_MDI0					27
	MDI_M<1>	ENET_MDI1		SPACING DELETED BECAUSE			27
	MDI_P<1>	ENET_MDI1		OF PHYSICAL CONSTRAINTS			27
	MDI_M<2>	ENET_MDI2		AROUND MARVELL PHY			27
	MDI_P<2>	ENET_MDI2					27
	MDI_M<3>	ENET_MDI3					27
	MDI_P<3>	ENET_MDI3					27
	RJ45_DN<0>	RJ45_DP0			10_MIL_SPACING		27 39
	RJ45_DP<0>	RJ45_DP0			10_MIL_SPACING		27 39
	RJ45_DN<1>	RJ45_DP1			10_MIL_SPACING		27 39
	RJ45_DP<1>	RJ45_DP1			10_MIL_SPACING		27 39
	RJ45_DN<2>	RJ45_DP2			10_MIL_SPACING		27 39
	RJ45_DP<2>	RJ45_DP2			10_MIL_SPACING		27 39
	RJ45_DN<3>	RJ45_DP3			10_MIL_SPACING		27 39
	RJ45_DP<3>	RJ45_DP3			10_MIL_SPACING		27 39
FIREWIRE	FW_TPA0N	FW_TPA0			MIN_LINE_WIDTH=3.4 10_MIL_SPACING		28 29
	FW_TPA0P	FW_TPA0			MIN_LINE_WIDTH=3.4 10_MIL_SPACING		28 29
	FW_TPB0N	FW_TPB0			MIN_LINE_WIDTH=3.4 10_MIL_SPACING		28 29
	FW_TPB0P	FW_TPB0			MIN_LINE_WIDTH=3.4 10_MIL_SPACING		28 29
	FW_TPI1N	FW_TPI0			MIN_LINE_WIDTH=3.4 10_MIL_SPACING		
	FW_TPI1P	FW_TPI0			MIN_LINE_WIDTH=3.4 10_MIL_SPACING		
	FW_TPO0N	FW_TPO0			MIN_LINE_WIDTH=3.4 10_MIL_SPACING		
	FW_TPO0P	FW_TPO0			MIN_LINE_WIDTH=3.4 10_MIL_SPACING		
	FW_TPA1N	FW_TPA1		500.0000	MIN_LINE_WIDTH=3.4 10_MIL_SPACING		28 29
	FW_TPA1P	FW_TPA1		500.0000	MIN_LINE_WIDTH=3.4 10_MIL_SPACING		28 29
	FW_TPB1N	FW_TPB1		500.0000	MIN_LINE_WIDTH=3.4 10_MIL_SPACING		28 29
	FW_TPB1P	FW_TPB1		500.0000	MIN_LINE_WIDTH=3.4 10_MIL_SPACING		28 29
	FW_TPI1N	FW_TPI1			MIN_LINE_WIDTH=3.4 10_MIL_SPACING		29 39
	FW_TPI1P	FW_TPI1			MIN_LINE_WIDTH=3.4 10_MIL_SPACING		29 39
	FW_TPO1N	FW_TPO1			MIN_LINE_WIDTH=3.4 10_MIL_SPACING		29 39
	FW_TPO1P	FW_TPO1			MIN_LINE_WIDTH=3.4 10_MIL_SPACING		29 39
LVDS LOWER	CLKLVDS_LN	CLKLVDS_L			10_MIL_SPACING	4	19 22 39
	CLKLVDS_LP	CLKLVDS_L			10_MIL_SPACING	4	19 22 39
	LVDS_L0N	LVDS_L0			10_MIL_SPACING		19 22 39
	LVDS_L0P	LVDS_L0			10_MIL_SPACING		19 22 39
	LVDS_L1N	LVDS_L1			10_MIL_SPACING		19 22 39
	LVDS_L1P	LVDS_L1			10_MIL_SPACING		19 22 39
	LVDS_L2N	LVDS_L2			10_MIL_SPACING		19 22 39
	LVDS_L2P	LVDS_L2			10_MIL_SPACING		19 22 39
UPPER	CLKLVDS_UN	CLKLVDS_U			10_MIL_SPACING	4	19 22 39
	CLKLVDS_UP	CLKLVDS_U			10_MIL_SPACING	4	19 22 39
	LVDS_U0N	LVDS_U0			10_MIL_SPACING		19 22 39
	LVDS_U0P	LVDS_U0			10_MIL_SPACING		19 22 39
	LVDS_U1N	LVDS_U1			10_MIL_SPACING		19 22 39
	LVDS_U1P	LVDS_U1			10_MIL_SPACING		19 22 39
	LVDS_U2N	LVDS_U2			10_MIL_SPACING		19 22 39
	LVDS_U2P	LVDS_U2			10_MIL_SPACING		19 22 39
TMDS	TMDS_CONN_CLKN	CLKCONN_TMDS			10_MIL_SPACING	4	22 39
	TMDS_CONN_CLKP	CLKCONN_TMDS			10_MIL_SPACING	4	22 39
	TMDS_CLKN	CLKTMDS			10_MIL_SPACING	4	20 22
	TMDS_CLKP	CLKTMDS			10_MIL_SPACING	4	20 22
	TMDS_DN<0>	TMDS_D0			10_MIL_SPACING		20 22 39
	TMDS_DP<0>	TMDS_D0			10_MIL_SPACING		20 22 39
	TMDS_DN<1>	TMDS_D1			10_MIL_SPACING		20 22 39
	TMDS_DP<1>	TMDS_D1			10_MIL_SPACING		20 22 39
	TMDS_DN<2>	TMDS_D2			10_MIL_SPACING		20 22 39
	TMDS_DP<2>	TMDS_D2			10_MIL_SPACING		20 22 39
USB	NEC_USB_DAM	NEC_USB_DA		MIN_LINE_WIDTH=5	10_MIL_SPACING		26
	NEC_USB_DAP	NEC_USB_DA		MIN_LINE_WIDTH=5	10_MIL_SPACING		26
	USB_DEM	USB_DE			5_MIL_SPACING		14
	USB_DEP	USB_DE			5_MIL_SPACING		14
	NEC_USB_DBM	NEC_USB_DB		MIN_LINE_WIDTH=5	10_MIL_SPACING		26
	NEC_USB_DBP	NEC_USB_DB		MIN_LINE_WIDTH=5	10_MIL_SPACING		26
	USB_DFM	USB_DF			5_MIL_SPACING		14
	USB_DFP	USB_DF			5_MIL_SPACING		14
	BT_USB_DM	BT_USB_D			5_MIL_SPACING		14 24 39
	BT_USB_DP	BT_USB_D			5_MIL_SPACING		14 24 39
	NEC_USB_RSDM1	NEC_USB_RSD1		MIN_LINE_WIDTH=5	10_MIL_SPACING		26
	NEC_USB_RSDP1	NEC_USB_RSD1		MIN_LINE_WIDTH=5	10_MIL_SPACING		26
	NEC_USB_RSDM2	NEC_USB_RSD2		MIN_LINE_WIDTH=5	10_MIL_SPACING		26
	NEC_USB_RSDP2	NEC_USB_RSD2		MIN_LINE_WIDTH=5	10_MIL_SPACING		26
	MODEM_USB_DM	MODEM_USB_D			5_MIL_SPACING		14 25 39
	MODEM_USB_DP	MODEM_USB_D			5_MIL_SPACING		14 25 39
	LEFT_USB_DM	LEFT_USB		MIN_LINE_WIDTH=5	10_MIL_SPACING		24 26 39
	LEFT_USB_DP	LEFT_USB		MIN_LINE_WIDTH=5	10_MIL_SPACING		24 26 39
	RIGHT_USB_DM	RIGHT_USB		MIN_LINE_WIDTH=5	10_MIL_SPACING		26 32 39
	RIGHT_USB_DP	RIGHT_USB		MIN_LINE_WIDTH=5	10_MIL_SPACING		26 32 39
POWER SUPPLIES	1V72_CSSN	1V72_CSS			DIFF		31
	1V72_CSSP	1V72_CSS			DIFF		31
	1V72_CSIN	1V72_CSI			DIFF		31
	1V72_CSIP	1V72_CSI			DIFF		31
	3V_SNSM	3V_SNS			DIFF		33
	3V_SNSP	3V_SNS			DIFF		33
	5V_SNSM	5V_SNS			DIFF		33
	5V_SNSP	5V_SNS			DIFF		33
THERMOSTAT	THERM1_DM	THERM1			DIFF		25
	THERM1_DP	THERM1			DIFF		25
	THERM2_DM	THERM2			DIFF		25
	THERM2_DP	THERM2			DIFF		25
	THERM1_M_DM	THERM1_MATN			DIFF		
	THERM1_M_DP	THERM1_MATN			DIFF		
	THERM2_M_DM	THERM2_MATN			DIFF		
	THERM2_M_DP	THERM2_MATN			DIFF		
	THERM1_A_DM	THERM1_ALT			DIFF		25
	THERM1_A_DP	THERM1_ALT			DIFF		25
	THERM2_A_DM	THERM2_ALT			DIFF		25
	THERM2_A_DP	THERM2_ALT			DIFF		25

INTERNAL LAYER
ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.57OHM
ZDIFF = 99.80HM

FOR FIREWIRE
ER = 4.3 (DIELECTRIC CONSTANT)
W = 3.4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 53.37OHM
ZDIFF = 107.17OHM

INTERNAL LAYER (USB1.1/USB 2.0)
ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL(USB 1.1)/ 5MIL(USB 2.0) (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 5MIL (USB 1.1) (SEPERATION OF DIFF TRACES)
S = 10MIL (USB 2.0) (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.5OHM (USB 1.1)/ 46.2OHM (USB 2.0)
ZDIFF = 89.3OHM (USB 1.1)/ 89.4OHM (USB 2.0)

SIGNAL CONSTRAINTS - PAGE 2

APPLE COMPUTER INC.

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POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
MAIN/SLEEP	+24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+BATT	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	
	+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+2_5V_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	39
	+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	35
	+1_5V_SLEEP_VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	35
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31 32
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31 39
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31 39
	1772_DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	1772_LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	31
	1772_LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	31
	1772_DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	31
	1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	31
PMU	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32
	+4_85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	30 32
	+4_6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32 33
	+4_85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	25 30
MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24 33
	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24
TRACKPAD	+5V_TPAD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	23 39
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	23 39
VIDEO	+12_8V_INV	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	22
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
KB LED	KBD_LED1_OUT	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	23 39
	KBD_LED2_OUT	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	23 39
FAN GND	FANL_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 39
	FANR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 39
SOUND	+5V_SOUND_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	SND_AGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=15	25

	GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	
I/O AREA	CHGND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND1
INVERTER	CHGND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND2
TRACKPAD	CHGND3	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND3
LVDS	CHGND4	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND4 39
I/O AREA	CHGND5	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND5
I/O AREA	CHGND6	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND6
	ENET_CTAP_CHGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	27

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 6 34 39
	CPU_AVDD	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
DDR RAM	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 7 8 15 16 23 34
INTREPID	DDR_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	11
	+2_5V_INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	9 10 15 16
	+3V_INTREPID_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14
PLLS	+1_5V_INTREPID_PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	8 12 14
	+1_5V_INTREPID_PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5	14
	+1_5V_INTREPID_PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5	12
	+1_5V_INTREPID_PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	8
	+1_5V_INTREPID_PLL8	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
REFERENCE	INT_MEM_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	9
	INT_AGP_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	12 18
	INT_MEM_REF_H	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	9
	UIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	13
CARDBUS	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	MIN_NECK_WIDTH REDUCED FOR TESTPOINTS 17
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
ATI M10	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	18 19 39
	+GPU_MEM	VOLTAGE=2.5V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	18 21
	+3V_GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 18 19 21
	+3V_GPU_FLT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	21
	+1_5V_AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 15 16 18 19 21
	GPU_MEM_IO	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	GPU_MEM_IO_FLT	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+GPU_MEMCORE	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+1_8V_GPU	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18 19 20 21
	+2_5V_GPU_PNLIO	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_8V_ATI_PVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19 21
	+1_5V_AGP_GPU	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_5V_GPU_VDD15	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	+1_8V_GPU_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1338	+1_8V_GPU_VDDDI	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1339	GPU_VCORE_VDDCI	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	18
1340	+2_5V_GPU_A2VDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1341	+1_8V_GPU_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1342	+1_8V_GPU_PNLPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1343	+1_8V_GPU_PNLIO	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1344	+GPU_MCLK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1345	+1_8V_GPU_AVDDQ	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1346	+1_8V_GPU_MEMPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1347	+3V_ATI_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	18
1348	+3V_ATI_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	18
1349	+GPU_VDD15_UF	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
1350	+2_5V_SLEEP_NECK1	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
1351	+3V_SLEEP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1352	+1_5V_AGP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
1353	+1_8V_PVDD_NECK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
1354	GPU_VCORE_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
1355	+GPU_VDD15_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
1356	+2_5V_SLEEP_NECK2	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1357	+1_8V_SLEEP_NECK	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1358	+1_5V_SLEEP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1359	+2_5V_GPU	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
SILICON IMIAGE	1360 +3V_SI_PLLVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	20
	1361 +3V_SI_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	20
	1362 +3V_SI_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	20
88E1111	+2_5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+2_5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
	+1_0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
	LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
FW	LM2594_IN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_ESD_ILIM	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+3V_FW_ESD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+FW_FUSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_PWR_OR	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28 29
	+FW_VP0	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_PWR_PORTA	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_VP1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+3V_FW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28 29
	+3V_FW_UF	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	28
	+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
USB 2.0	FW_TPO0R	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29 39
	NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
INTREPID SSCG	+3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+3V_CG_PLL_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	14
	+2_5V_CG_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	14

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32
	1625_VSW	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32
	1V20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	31 32
LTC3707 5V SWITCHER	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	33
	5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
3V SWITCHER	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	33
MAX1715 2.5V SWITCHER	2_5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	35
	2_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	2_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	2_5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	2_5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
1.5V SWITCHER	1_5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	1_5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	35
	1_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	1_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	1_5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	1_5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
CONTROL	1_5V_ILIM		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	2_5V_ILIM		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	MAX1715_TON		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	MAX1715_SKIP		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	MAX1715_REF	VOLTAGE=2.0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	35
MAX1717	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=200	MIN_NECK_WIDTH=10	34
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	VCORE_ILIM		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	34
	VCORE_REF		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	34
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	34
	VCORE_CC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	34
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	34 39
	VCORE_TIME		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	34
	VCORE_VGATE		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	14 34
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=15	34
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	34
	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	34
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	34
LTC1778	1778_VIN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	19
	1778_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	1778_BST_RC	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	1778_TG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_BG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	GPU_VCORE_SW	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	19
	1778_ION		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19
	1778_ITH		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19
	1778_ITH_RC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19
	1_5V_2_5V_OK		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	1778_VFB		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19 39
	1778_FCB		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19
	1778_VRNG		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19
LTC3411	LTC3411_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC3411_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	
	1_8V_SW	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	35
	1_8V_VFB		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
	LTC3411_ITH_RC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
	LTC3411_ITH		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
	LTC3411_SYNC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
	LTC3411_SHDN		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
LTC1962 INT PLLS	LTC1962_INT_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	14
	LTC1962_L3_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_L3_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_1V5_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_1V5_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	

SIGNAL CONSTRAINTS - PAGE 3

APPLE COMPUTER INC.

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FUNCTIONAL TEST POINTS

FUNC_TEST=YES JTAG_ASIC_TMS 13 27
FUNC_TEST=YES JTAG_ASIC_TDI 27
FUNC_TEST=YES JTAG_ASIC_TDO 13 14
FUNC_TEST=YES JTAG_ASIC_TCK 13 27
FUNC_TEST=YES JTAG_ASIC_TRST_L 13 27
FUNC_TEST=YES CPU_CHKSTP_OUT_L 5
FUNC_TEST=YES CPU_SRESET_L 5
FUNC_TEST=YES CPU_HRESET_L 5 7 23
FUNC_TEST=YES JTAG_CPU_TMS 5 23
FUNC_TEST=YES JTAG_CPU_TDI 5 23
FUNC_TEST=YES JTAG_CPU_TDO_TP 5
FUNC_TEST=YES JTAG_CPU_TCK 5 23
FUNC_TEST=YES JTAG_CPU_TRST_L 5 23 39

FUNC_TEST=YES INT_I2C_CLK0 11 13 23
FUNC_TEST=YES INT_I2C_DATA0 11 13 23
FUNC_TEST=YES INT_I2C_CLK1 13 14 25
FUNC_TEST=YES INT_I2C_DATA1 13 14 25
FUNC_TEST=YES CBUS_DET_1_L 17
FUNC_TEST=YES CBUS_DET_2_L 17
FUNC_TEST=YES TMDS_DN<0> 20 22 37
FUNC_TEST=YES TMDS_DP<0> 20 22 37
FUNC_TEST=YES TMDS_DN<1> 20 22 37
FUNC_TEST=YES TMDS_DP<1> 20 22 37
FUNC_TEST=YES TMDS_DN<2> 20 22 37
FUNC_TEST=YES TMDS_DP<2> 20 22 37
FUNC_TEST=YES TMDS_CONN_CLKN 22 37

FUNC_TEST=YES TMDS_CONN_CLKP 22 37
FUNC_TEST=YES VGA_R 22
FUNC_TEST=YES VGA_G 22
FUNC_TEST=YES VGA_B 22
FUNC_TEST=YES VGA_VSYNC 22
FUNC_TEST=YES VGA_HSYNC 22
FUNC_TEST=YES DVI_DDC_CLK_UF 22
FUNC_TEST=YES DVI_DDC_DATA_UF 22
FUNC_TEST=YES DVI_HPD_UF 22
FUNC_TEST=YES LVDS_L0N 19 22 37
FUNC_TEST=YES LVDS_L0P 19 22 37
FUNC_TEST=YES LVDS_L1N 19 22 37
FUNC_TEST=YES LVDS_L1P 19 22 37
FUNC_TEST=YES LVDS_L2N 19 22 37
FUNC_TEST=YES LVDS_L2P 19 22 37
FUNC_TEST=YES CLKLVDS_LN 19 22 37
FUNC_TEST=YES CLKLVDS_LP 19 22 37
FUNC_TEST=YES LVDS_U0N 19 22 37
FUNC_TEST=YES LVDS_U0P 19 22 37
FUNC_TEST=YES LVDS_U1N 19 22 37
FUNC_TEST=YES LVDS_U1P 19 22 37
FUNC_TEST=YES LVDS_U2N 19 22 37
FUNC_TEST=YES LVDS_U2P 19 22 37
FUNC_TEST=YES CLKLVDS_UN 19 22 37
FUNC_TEST=YES CLKLVDS_UP 19 22 37
FUNC_TEST=YES LVDS_DDC_CLK 19 22
FUNC_TEST=YES LVDS_DDC_DATA 19 22
FUNC_TEST=YES BRIGHT_PWM 22
FUNC_TEST=YES TV_GND1 22 38
FUNC_TEST=YES TV_GND2 22 38

FUNC_TEST=YES TV_C 22
FUNC_TEST=YES TV_Y 22
FUNC_TEST=YES TV_COMP 22
FUNC_TEST=YES SND_TO_AUDIO 14 25
FUNC_TEST=YES SND_SYNC 14 25
FUNC_TEST=YES SND_CLKOUT 14 25 36

FUNC_TEST=YES INT_AUDIO_TO_SND 14 25
FUNC_TEST=YES SND_SCLK 14 25 36
FUNC_TEST=YES SND_HW_RESET_L 14 25
FUNC_TEST=YES SND_HP_SENSE_L 14 25
FUNC_TEST=YES SND_LIN_SENSE_L 14 25
FUNC_TEST=YES INT_I2C_DATA2 14 25
FUNC_TEST=YES INT_I2C_CLK2 14 25
FUNC_TEST=YES CHGND4 38
FUNC_TEST=YES SLEEP_LED 23 25

FUNC_TEST=YES BT_USB_DM 14 24 37
FUNC_TEST=YES BT_USB_DP 14 24 37
FUNC_TEST=YES MODEM_USB_DM 14 25 37
FUNC_TEST=YES MODEM_USB_DP 14 25 37
FUNC_TEST=YES PCI_AD<0> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<1> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<2> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<3> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<4> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<5> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<6> 9 12 17 24 26 37

FUNC_TEST=YES PCI_AD<7> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<8> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<9> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<10> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<11> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<12> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<13> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<14> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<15> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<16> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<17> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<18> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<19> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<20> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<21> 12 17 24 26 37
FUNC_TEST=YES PCI_AD<22> 12 17 24 26 37
FUNC_TEST=YES PCI_AD<23> 12 17 24 26 37
FUNC_TEST=YES PCI_AD<24> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<25> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<26> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<27> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<28> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<29> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<30> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<31> 9 12 17 24 26 37
FUNC_TEST=YES PCI_FRAME_L 12 17 24 26 37
FUNC_TEST=YES PCI_TRDY_L 12 17 24 26 37
FUNC_TEST=YES PCI_IRDY_L 12 17 24 26 37
FUNC_TEST=YES PCI_DEVSEL_L 12 17 24 26 37
FUNC_TEST=YES PCI_STOP_L 12 17 24 26 37

FUNC_TEST=YES PCI_PAR 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<0> 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<1> 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<2> 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<3> 12 17 24 26 37
FUNC_TEST=YES AIRPORT_PCI_REQ_L 12 24
FUNC_TEST=YES AIRPORT_PCI_GNT_L 12 24
FUNC_TEST=YES AIRPORT_PCI_INT_L 14 24
FUNC_TEST=YES EIDE_OPTICAL_DATA<0> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<1> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<2> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<3> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<4> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<5> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<6> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<7> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<8> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<9> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<10> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<11> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<12> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<13> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<14> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<15> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DMA_RQ 24 37
FUNC_TEST=YES EIDE_OPTICAL_RD_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_DMAACK_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_ADDR<0> 24 37
FUNC_TEST=YES EIDE_OPTICAL_ADDR<1> 24 37
FUNC_TEST=YES EIDE_OPTICAL_ADDR<2> 24 37
FUNC_TEST=YES SND_AMP_MUTE 25
FUNC_TEST=YES SND_HP_MUTE_INV 25

FUNC_TEST=YES EIDE_OPTICAL_CS0_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_CS1_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_RST_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_WR_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_IOCHRDY 24 37
FUNC_TEST=YES EIDE_OPTICAL_INT 24 37
FUNC_TEST=YES TPAD_F_TXD 23
FUNC_TEST=YES TPAD_F_RXD 23
FUNC_TEST=YES LID_CLOSED_L 23
FUNC_TEST=YES COMM_RESET_L 14 25
FUNC_TEST=YES COMM_SHUTDOWN 14 25
FUNC_TEST=YES COMM_RING_DET_L 14 25 30
FUNC_TEST=YES KBD_ID 23 30
FUNC_TEST=YES +5V_TPAD_SLEEP 23 38
FUNC_TEST=YES +3V_HALL_EFFECT 23 38
FUNC_TEST=YES KBD_CAPSLOCK_LED 23
FUNC_TEST=YES KBD_FUNCTION_L 23 30
FUNC_TEST=YES KBD_CONTROL_L 23 30
FUNC_TEST=YES KBD_COMMAND_L 23 30
FUNC_TEST=YES KBD_OPTION_L 23 30
FUNC_TEST=YES KBD_SHIFT_L 23 30
FUNC_TEST=YES KBD_X<0> 23 30
FUNC_TEST=YES KBD_X<1> 23 30
FUNC_TEST=YES KBD_X<2> 23 30
FUNC_TEST=YES KBD_X<3> 23 30
FUNC_TEST=YES KBD_X<4> 23 30
FUNC_TEST=YES KBD_X<5> 23 30
FUNC_TEST=YES KBD_X<6> 23 30
FUNC_TEST=YES KBD_X<7> 23 30
FUNC_TEST=YES KBD_X<8> 23 30
FUNC_TEST=YES SRCLK_TP 26
FUNC_TEST=YES SRMOD_TP 26
FUNC_TEST=YES TEB_TP 26
FUNC_TEST=YES TEST_TP 26

FUNC_TEST=YES KBD_X<9> 23 30
FUNC_TEST=YES KBD_Y<0> 23 30
FUNC_TEST=YES KBD_Y<1> 23 30
FUNC_TEST=YES KBD_Y<2> 23 30
FUNC_TEST=YES KBD_Y<3> 23 30
FUNC_TEST=YES KBD_Y<4> 23 30
FUNC_TEST=YES KBD_Y<5> 23 30
FUNC_TEST=YES KBD_Y<6> 23 30
FUNC_TEST=YES KBD_Y<7> 23 30
FUNC_TEST=YES KBD_NUMLOCK_LED 23
FUNC_TEST=YES +BATT_POS 31 38
FUNC_TEST=YES BATT_CLK 31
FUNC_TEST=YES BATT_DATA 31
FUNC_TEST=YES BATT_NEG 31 38
FUNC_TEST=YES PMU_BATT_DET_L 30 31
FUNC_TEST=YES FANR_GND 25 38

FUNC_TEST=YES FANL_GND 25 38
FUNC_TEST=YES FANL_TACH 25
FUNC_TEST=YES FANR_PWM 25
FUNC_TEST=YES FANL_PWM 25
FUNC_TEST=YES RJ45_DP<0> 27 37
FUNC_TEST=YES RJ45_DN<0> 27 37
FUNC_TEST=YES RJ45_DP<1> 27 37
FUNC_TEST=YES RJ45_DN<1> 27 37
FUNC_TEST=YES RJ45_DP<2> 27 37
FUNC_TEST=YES RJ45_DN<2> 27 37
FUNC_TEST=YES RJ45_DP<3> 27 37
FUNC_TEST=YES RJ45_DN<3> 27 37
FUNC_TEST=YES FW_TPOOR 29 38
FUNC_TEST=YES VCORE_VID0
FUNC_TEST=YES VCORE_VID1
FUNC_TEST=YES VCORE_VID2
FUNC_TEST=YES VCORE_VID3
FUNC_TEST=YES VCORE_VID4

FUNC_TEST=YES FW_TPO1P 29 37
FUNC_TEST=YES FW_TPO1N 29 37
FUNC_TEST=YES FW_TPI1P 29 37
FUNC_TEST=YES FW_TPI1N 29 37
FUNC_TEST=YES CHARGE_LED_L 30 31
FUNC_TEST=YES ADAPTER_DET 30 31
FUNC_TEST=YES SUTRO_ALS_GAIN_SW 23 24
FUNC_TEST=YES SUTRO_ALS_OUT 23 24
FUNC_TEST=YES KBD_LED1_OUT 23 38
FUNC_TEST=YES KBD_LED2_OUT 23 38
FUNC_TEST=YES COMM_TXD_L 14 25
FUNC_TEST=YES COMM_TRXC 14 25
FUNC_TEST=YES COMM_GPIO_L 14 25
FUNC_TEST=YES COMM_DTR_L 14 25
FUNC_TEST=YES COMM_RTS_L 14 25
FUNC_TEST=YES COMM_RXD 14 25
FUNC_TEST=YES PMU_KB_RESET_L 30
FUNC_TEST=YES PWR_BUTTON_L 23 25
FUNC_TEST=YES +PBUS 38
FUNC_TEST=YES +24V_PBUS 38
FUNC_TEST=YES GPU_VCORE 18 19 38
FUNC_TEST=YES CPU_VCORE_SLEEP 5 6 34 38
FUNC_TEST=YES VCORE_FB 34 38
FUNC_TEST=YES +1_8V_MAIN 38
FUNC_TEST=YES +3V_PMU 38
FUNC_TEST=YES +5V_DDC_SLEEP 22 38
FUNC_TEST=YES +12_8V_INV 22 38

FUNC_TEST=YES VCORE_MUX_EN 34

FUNC_TEST=YES +5V_INV_SW 22 38
FUNC_TEST=YES LEFT_USB_DM 24 26 37
FUNC_TEST=YES LEFT_USB_DP 24 26 37
FUNC_TEST=YES RIGHT_USB_DM 26 32 37
FUNC_TEST=YES RIGHT_USB_DP 26 32 37
FUNC_TEST=YES NEC_LEFT_USB_PWREN 24 26
FUNC_TEST=YES NEC_LEFT_USB_OVERCURRENT 24 26
FUNC_TEST=YES NEC_RIGHT_USB_PWREN 26 32
FUNC_TEST=YES NEC_RIGHT_USB_OVERCURRENT 26 32
FUNC_TEST=YES DCDC_EN 19 29 33 34
FUNC_TEST=YES BBANG_HRESET_L 23
FUNC_TEST=YES MAIN_RESET_L 14 17 18 20 24 26 30
FUNC_TEST=YES RF_DISABLE_L_SPN 24
FUNC_TEST=YES AIRPORT_CLKRUN_L 24
FUNC_TEST=YES ROM_RW_L 9 12 24
FUNC_TEST=YES ROM_ONBOARD_CS_L 9 24
FUNC_TEST=YES ROM_CS_L 9 12 24
FUNC_TEST=YES CLK33M_AIRPORT 12 24 36
FUNC_TEST=YES AIRPORT_IDSEL 24
FUNC_TEST=YES ROM_OE_L 9 12 24
FUNC_TEST=YES INT_MOD_DTI 14 25
FUNC_TEST=YES JTAG_CPU_TRST_L 5 23 39
FUNC_TEST=YES MOD_BITCLK 14 25
FUNC_TEST=YES MOD_CLKOUT 14 25
FUNC_TEST=YES MOD_DTO 14 25
FUNC_TEST=YES MOD_SYNC 14 25
FUNC_TEST=YES SLEEP 23 25 30 33 35
FUNC_TEST=YES 1778_VFB 19 38

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REVISION HISTORY

12/11/03

1) IMPORTED Q41 PRODUCTION RELEASE SCHEMATIC
2) CHANGED CPU (U43) TO A7PM
3) CHANGED PLL CONFIG STUFFING FOR NEW CPU
4) CHANGED U44 TO M1Y-PSP64 SYMBOL
5) ADDED CPU AVDD LDO (U6)
6) ADDED R284 AND R604 TO ADD OPTION FOR PD_I OF U42 (CLOCK CHIP) TO BE DRIVEN BY JTAG_ASIC_TDO FROM INTREPID
7) ADDED R608 TO DISCONNECT INT GPIO0 FROM CS FSEL
8) CHANGED JTAG_ASIC_TDO_TP TO JTAG_ASIC_TDO AND MOVED IT TO INTREPID'S TDO
9) CHANGED JTAG_ASIC_TDI TO CONNECT TO ETHERNET PHY'S TDI

12/15/03

10) CHANGED PIN 4 (DCDC_EN) ON J11 TO NEC_RIGHT_USBOVERCURRENT
11) CHANGED PIN 11 OF J11 TO NC

12/16/03

12) ADDED R633 AS PULLUP ON JTAG_ASIC_TDI
13) CHANGED CPU_TEMP_DM TO CPU_THERM_DM
14) CHANGED CPU_TEMP_DP TO CPU_THERM_DP
15) CHANGED GPU_THERM_DP TO GPU_THERM_DP_TP
16) CHANGED GPU_THERM_DM TO GPU_THERM_DM_TP
17) FIXED MISSED CONNECTION WITH MAXBUS_SLEEP TO CPU

12/17/03

18) CHANGED R657 (EXTPLL_SDWN_POL_BOOT_STRAP) TO NO STUFF AND REMOVED NO STUFF FROM R153
19) UPDATE DIFF NET SPACING TYPE PROPERTY ON POWER SUPPLY SENSE AND THERMAL DIODE DIFF PAIRS
20) CHANGED FIREWIRE OSCILLATOR (G1) TO NEW PREFERRED SUNNY PART

12/18/03

21) CHANGED MAX VIA COUNT ON ALL AGP STB NETS TO 5 TO CLEAR DRCS

** RELEASED FOR EVT **

2/10/04

22) REMOVED XW11 - JUMPER ON 1.8V SWITCHER OUTPUT
23) CHANGED R657 TO STUFFE AND R153 TO NO STUFF
24) CHANGED CPU PLL CONFIG TO 9X HIGH AND 5X LOW

** RELEASED FOR DVT **

3/24/04

25) REMOVED ALTERNATE BOM OPTION FROM ALTERNATE ETHERNET CRYSTALS

3/29/04

26) ADDED ALTERNATE FOR Q41A REV 1.1.1 CPU (U43)
27) ADDED ALTERNATES FOR 128MB AND 64MB A16_M11_S
28) CHANGED TMDS SERIES RPAKS TO 0 OHMS (RP57,RP27,RP32,RP28)
29) ADDED ALTERNATE FOR ALS OP-AMP (U40)

** RELEASED TO REV A **

30) CHANGED TMDS TERMINATION R,C AND LS TO PRODUCTION VALUES

** RELEASED TO REV A UNDER NEW PART NUMBER **

7/6/05

ADDED 338S0223 (88E1111 REV. B1) AS AN ALTERNATE OF 338S0079

8/22/05

REPLACED 740S0006 EITH 740S0018 (FUSE,1.5A,24V,SMD,LF)
ADDED 128S0022 (220 UF) AS AN ALTERNATE OF 128S0034 (330 UF) FOR MPU VCORE CAPS
ADDED LABELS WITH EEE

** RELEASED TO 051-6654-C **

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	C
SCALE: NONE	SHT 40 OF 44	

8	7	6	5	4	3	2	1

```
*** Signal Cross-Reference for the entire design ***

+1_0V_MARVELL      27D2< 38B3>
+1_5V_AGP          12C5< 12D1< 12D4< 15D5< 16C8<
                  18C6< 18D6< 19A8< 19B4<> 19D5<>
                  21B8< 21D6< 38C3>
+1_5V_AGP_GPU      21C5< 38C3>
+1_5V_AGP_NECK     19B4<> 38B3>
+1_5V_GPU_VDD15    19D3< 38C3>
+1_5V_INTREPID_PLL  8D6< 12D4< 12D8< 14D6<> 38D3>
+1_5V_INTREPID_PLL1  14C3< 38D3>
+1_5V_INTREPID_PLL2  14D3< 38D3>
+1_5V_INTREPID_PLL3  14D3< 38D3>
+1_5V_INTREPID_PLL4  14D3< 38D3>
+1_5V_INTREPID_PLL5  12D3< 38D3>
+1_5V_INTREPID_PLL6  12D6< 38D3>
+1_5V_INTREPID_PLL7  8D5< 38D3>
+1_5V_INTREPID_PLL8  14D3< 38D3>
+1_5V_LDO          35D8< 38D6>
+1_5V_MAIN         38D6>
+1_5V_SLEEP        38D6>
+1_5V_SLEEP_NECK   21A3<> 38B3>
+1_5V_SLEEP_VIN    35D8<> 38D6>
+1_8V_ATI_PVDD     19C5<> 21B6< 21B6< 21D6<> 38C3>
+1_8V_ATI_TPVDD    21D2<>
+1_8V_DVO_F        21B2<
+1_8V_GPU          18A7< 19D8< 20A5< 21A2< 21A6<
                  21B1< 21B6< 21C8< 21D6< 21D8< 38C3>
+1_8V_GPU_AVDD     21D5< 38C3>
+1_8V_GPU_AVDDQ    21D4< 21D7< 38C3>
+1_8V_GPU_MEMPLL   21B5< 38C3>
+1_8V_GPU_PLL      21D5< 38C3>
+1_8V_GPU_PNLIO    21A5< 38C3>
+1_8V_GPU_PNLPLL   21B5< 38C3>
+1_8V_GPU_TP_PLL   21B4< 21D1<
+1_8V_GPU_VDDDI    21C7< 21D4< 38C3>
+1_8V_MAIN         38D6> 39A2>
+1_8V_PVDD_NECK    19B5<> 38B3>
+1_8V_SLEEP        38D6>
+1_8V_SLEEP_NECK   21A3<> 38B3>
+1_95V_FW_DVDD     28C4< 28C7<> 28D5< 38A3>
+1_95V_FW_DVDD_PORT1  28D6< 38A3>
+1_95V_FW_DVDD_RX0  28C5< 38A3>
+1_95V_FW_DVDD_TX0  28C5< 38A3>
+1_95V_FW_PLL400VDD  28D5< 38A3>
+1_95V_FW_PLL500VDD  28D5< 38A3>
+1_95V_FW_PLLVDD   28D5< 28D7<> 38A3>
+2_5V_CG_MAIN      14C6< 38A3>
+2_5V_GPU          21A8< 21B6< 21D3< 21D7< 21D8<
                  38B3>
+2_5V_GPU_A2VDD    21D4< 21D7< 38C3>
+2_5V_GPU_PNLIO    21A5< 38C3>
+2_5V_INTREPID     9A8< 10D3< 10D5< 10D6< 10D8< 15D7<
                  16B8< 38D3>
+2_5V_MAIN         38D6>
+2_5V_MARVELL      27B8< 27C4<> 38B3>
+2_5V_MARVELL_AVDD  27C4< 38B3>
+2_5V_SLEEP        38D6>
+2_5V_SLEEP_NECK1  19C4<> 38B3>
+2_5V_SLEEP_NECK2  21A3<> 38B3>
+2_8V_GPU_LVDS_LDO  21A6<>
+3V_ATI_OSC_SLEEP  18D2< 38C3>
+3V_ATI_SS         18B2< 38C3>
+3V_CG_PLL_MAIN    14C6< 38A3>
+3V_FW             28A3< 28D7<> 29D5< 38A3>
+3V_FW_AVDD        28C6< 38A3>
+3V_FW_AVDD_PORT0  28C6< 38A3>
+3V_FW_AVDD_PORT1  28C6< 38A3>
+3V_FW_AVDD_PORT2  28D6< 38A3>
+3V_FW_ESD         29B3<> 29D2<> 38B3>
+3V_FW_ESD_ILIM    29D4< 38B3>
+3V_FW_UF          28D7<> 38A3>
+3V_GPU            12D1< 18B8< 18C5< 18C7< 18D6<
                  19C4< 19C6< 19C7< 19D7< 21A7< 21B1<
                  21B8< 38C3>
+3V_GPU_FLT        21B2< 38C3>
+3V_GPU_SI         20C4< 20C8< 20D8<
+3V_HALL_EFFECT    23C6<> 38B6> 39C4>
+3V_INTREPID_USB   14C3< 38D3>
+3V_LCD            22B4<> 38B6>
+3V_LCD_SW         22A4<> 38B6>
+3V_MAIN           38D6>
+3V_NEC_VDD        26D7< 26D7< 38A3>
+3V_PMU            38D6> 39A2>
+3V_PMU_AVCC       25A4< 30B6< 30D5<> 38C6>
+3V_PMU_ESR        32A2< 38C6>
+3V_PMU_RESET      30B7< 34A3<>
+3V_SI_AVCC        20C7< 38B3>
+3V_SI_PLLVCC      20C7< 38B3>
+3V_SI_VCC         20C6< 38B3>
+3V_SLEEP          38D6>
+3V_SLEEP_NECK     21A3<> 38B3>
+3V_SLP_OK_L       33B4<>
+3V_SLP_ON         33A5<>
+4_6V_BU           32A3<> 33B7< 38C6>
+4_85V_ESR         32A4< 38C6>
+4_85V_RAW         30B4< 32A4<> 38C6>
+5V_DDC_SLEEP      22D3<> 22D5<> 38B6> 39A2>
+5V_DDC_SLEEP_UF   22D6< 38B6>
+5V_HD_SLEEP       24D1<> 33A7<> 38C6>
+5V_INV_SW         22B1<> 38B6> 39D1>
+5V_INV_UF_SW      22B2<> 38B6>
+5V_MAIN           38D6>
+5V_SLEEP          38D6>
+5V_SOUND_SLEEP    38B6>
+5V_TPAD_SLEEP     23C7<> 38B6> 39C4>
+12_8V_INV         22B1<> 38B6> 39A2>
+24V_PBUS          38D6> 39B2>
+ADAPTER           31D8<> 32B7< 38D6>
+ADAPTER_ILIM      32B6<> 38C6>
+ADAPTER_OR_BATT   32A5<> 38C6>
+ADAPTER_SENSE     31D5<> 38C6>
+ADAPTER_SW        31D6<> 38C6>
+BATT              38D6>
+BATT_14V_FUSE     31D1<> 38C6>
+BATT_24V_FUSE     31B1< 31D2<> 38C6>
+BATT_POS          31A4<> 38C6> 39C3>
+BATT_RSNS         31B2< 38C6>
+BATT_VSNS         31A4< 38C6>
+FW_FUSE           29D7<> 38A3>
+FW_PWR_OR         28B8< 28D8<> 29D5<> 38A3>
+FW_PWR_PORTA      29C5< 38A3>
+FW_SW             29D5<> 38A3>
+FW_VP0            29C2<> 38A3>
+FW_VP1            29A3<> 38A3>
+GPU_MCLK          21C7< 21D4< 38C3>
+GPU_MEM           18A6<> 18B8< 21B4< 21B7< 21C6<
                  21C8< 21D2< 38C3>
+GPU_MEMCORE       21C5< 38C3>
+GPU_VDD15_NECK    19B5<> 38B3>
+GPU_VDD15_UF      19B5<> 19D4<> 38C3>
+HD_LOGIC_SLEEP    24C2<> 38C6>
+PBUS              38D6> 39B2>
+VCC_CBUS_SW       17B1<> 17B2<> 17D2<> 38D3>
+VPP_CBUS_SW       17B1<> 17B2<> 17D2<> 38C3>
1V20_REF           31C7< 32C8< 38D1>
1V65_REF           31A5<
1_5V_2_5V_OK       35C5> 38B1>
1_5V_BOOST         35C6<> 38C1>
1_5V_BST           35C5<> 38C1>
1_5V_DH            35C5<> 38C1>
1_5V_DL            35B5<> 38C1>
1_5V_FB            35B5< 35B7< 38C1>
1_5V_ILIM          35C5<> 38C1>
1_5V_LX            35B5<> 38C1>
1_5V_SLEEP_EN_L    35C7<> 35D7<>
1_8V_SLEEP_PWREN_L  35A3<>
1_8V_SW            35A5<> 38A1>
1_8V_VFB           38A1>
2_5V_BOOST         35C4<> 38D1>
2_5V_BST           35C4<> 38D1>
2_5V_DH            35C4<> 38D1>
2_5V_DL            35B4<> 38D1>
2_5V_ILIM          35C5<> 38C1>
2_5V_LX            35B4<> 38D1>
2_5V_SLEEP_PWREN_L  35C2<>
2_34V_REF          30A4<
3V_5V_OK           33B4<> 35A8<> 35D6<
3V_5V_OK_INV       35A8<>
3V_BG              33C4<>
3V_BOOST           33C4<>
3V_BOOST_ESR       33D3<>
3V_ITH             33C4<>
3V_ITH_RC          33C3<
3V_PMU_VTAP        32B3<
3V_RSNS            33D2< 38D1>
3V_RUNSS           33C4<
3V_SLEEP_PWREN_L   33A3<>
```

```
3V_SNSM            33C4< 37A2>
3V_SNSP            33C4< 37A2>
3V_SW              33C4<> 38D1>
3V_TG              33D4<>
3V_VOSNS           33C4<>
5V_BG              33C5<>
5V_BOOST           33C5<>
5V_BOOST_ESR       33D6<>
5V_HD_PWREN        33A8<>
5V_ITH             33C5<>
5V_ITH_RC          33C6<
5V_RSNS            33D7< 38D1>
5V_RUNSS           33C5<
5V_SLEEP_PWREN     33A8<>
5V_SNSM            33C5< 37A2>
5V_SNSP            33C5< 37A2>
5V_SW              33C5<> 38D1>
5V_TG              33C5<>
5V_VOSNS           33C5<>
1625_BG            32C5<>
1625_BST           32C5<
1625_BST_ESR       32C5<>
1625_COMP          31D2< 32C6<
1625_DIV           32C8<
1625_ENABLE        32D7<>
1625_ENABLE_L      32D6<>
1625_EXTVCC        32D5<> 38D1>
1625_FCB           32C6<
1625_INTVCC        32C5<> 38D1>
1625_RUNSS         32C6<
1625_SGND          32B7<> 38D1>
1625_TG            32C5<>
1625_VFB           32B5<>
1625_VIN           32C6< 38D1>
1625_VSW           32C4<> 38D1>
1772_ACIN          31B5<
1772_ACOK_L        31B5<> 31C4<>
1772_BST           31B4<>
1772_BST_ESR       31C3<
1772_CCI           31B5<>
1772_CCS           31B5<
1772_CCV           31B5<>
1772_CCV_RC        31B5<
1772_CELLS         31B4<
1772_CLS           31A4<
1772_CSIN          31B4<> 37A2>
1772_CSIP          31B4<> 37A2>
1772_CSSN          31C5< 37A2>
1772_CSSP          31C5< 37A2>
1772_DCIN          31B5< 38C6>
1772_DHI           31B4<>
1772_DLO           31B4<>
1772_DLOV          31B4<> 38C6>
1772_GND           31A5<> 38C6>
1772_ICHG          31B5<>
1772_ICTL          31B5<>
1772_IINP          31B5<
1772_LDO           31C4<> 38C6>
1772_LX            31B4<> 38C6>
1772_REF           31B5<>
1772_VCTL          31B5<
1778_BG            19A5<> 38B1>
1778_BST           19A5<> 38B1>
1778_BST_RC        19A4<> 38B1>
1778_FCB           19A5< 38B1>
1778_GND           19A5< 19A7<> 38B1>
1778_ION           19A5< 38B1>
1778_ITH           19A5<> 38B1>
1778_ITH_RC        19A7< 38B1>
1778_SHDN_L        19A6<
1778_SHDN_L_D3COLD  19A7<>
1778_TG            19A5<> 38B1>
1778_VCC           19A5<> 38B1>
1778_VFB           19A2< 19A5< 38B1> 39A1>
1778_VIN           19A5< 38B1>
1778_VRNG          19A5< 38B1>
3405_MODE          27D5<
3405_VFB           27D4<>
3707_FCB           33C5<
3707_FSET          33C5<
3707_INTVCC        33D4<> 38D1>
3707_SGND          33B5<> 38D1>
3707_STBY          33C5<>
A29_CLS_ADJ        31A5<>
A29_CURRENT_ADJ    31C4<>
A29_DETECT         30A2< 31A5<> 31C4<>
A29_DET_L          30A3<
AB_SEL_LOW         34A6<>
AC_DIV             31C8<
AC_ENABLE_GATE     31D6<>
AC_ENABLE_L        31C6<>
AC_GTR_18V         31C4<>
AC_IN              27B8<> 29C7< 30B3< 31C5<> 31C7<>
AC_IN_FW_CNTL      29C7<>
AC_IN_L            31C2<> 31C6<>
AC_IN_L_RC         31C2<>
ADAPTER_DET        30A4< 31D8<> 39C2>
ADAPTER_I_REG      31D3<>
ADT7460_ADR_EN_L   25B3<>
ADT7460_FAN1_PWM   25B3<>
ADT7460_FAN2_PWM   25B3<>
ADT7460_THERM      25A5<> 25B3<>
ADT7460_VCC        25C4<
ADT7460_VCORE_MON  5C8<> 25B4<>
AGP8X_DET_PU       18C6<>
AGP_AD<0>          12D2<> 18C7<>
AGP_AD<15..0>      37D5>
AGP_AD<1>          12C2<> 18C7<>
AGP_AD<2>          12C2<> 18C7<>
AGP_AD<3>          12C2<> 18C7<>
AGP_AD<4>          12C2<> 18C7<>
AGP_AD<5>          12C2<> 18C7<>
AGP_AD<6>          12C2<> 18C7<>
AGP_AD<7>          12C2<> 18C7<>
AGP_AD<8>          12C2<> 18C7<>
AGP_AD<9>          12C2<> 18C7<>
AGP_AD<10>         12C2<> 18C7<>
AGP_AD<11>         12C2<> 18C7<>
AGP_AD<12>         12C2<> 18C7<>
AGP_AD<13>         12C2<> 18C7<>
AGP_AD<14>         12C2<> 18C7<>
AGP_AD<15>         12C2<> 18C7<>
AGP_AD<16>         12C2<> 18C7<>
AGP_AD<31..16>     37D5>
AGP_AD<17>         12C2<> 18C7<>
AGP_AD<18>         12C2<> 18C7<>
AGP_AD<19>         12C2<> 18C7<>
AGP_AD<20>         12C2<> 18C7<>
AGP_AD<21>         12C2<> 18C7<>
AGP_AD<22>         12C2<> 18C7<>
AGP_AD<23>         12C2<> 18C7<>
AGP_AD<24>         12C2<> 18C7<>
AGP_AD<25>         12C2<> 18D7<>
AGP_AD<26>         12C2<> 18D7<>
AGP_AD<27>         12B2<> 18D7<>
AGP_AD<28>         12B2<> 18D7<>
AGP_AD<29>         12B2<> 18D7<>
AGP_AD<30>         12B2<> 18D7<>
AGP_AD<31>         12B2<> 18D7<>
AGP_AD_STB<0>      12A2<> 12B2< 18D6<> 37D5>
AGP_AD_STB<1>      12A2<> 12B2< 18D6<> 37D5>
AGP_AD_STB_L<0>    12A2<> 12B2< 18D6<> 37D5>
AGP_AD_STB_L<1>    12A2< 12A2<> 18D6<> 37D5>
AGP_ATI_RESET_L    18B7<
AGP_ATI_VREF       18B7<
AGP_ATI_VREFG      18B7<
AGP_BUSY_L         12C4<> 12D2< 18D6>
AGP_CBE<0>         12B2<> 18B7<>
AGP_CBE<1..0>      37D5>
AGP_CBE<1>         12B2<> 18B7<>
AGP_CBE<2>         12B2<> 18B7<>
AGP_CBE<3..2>      37D5>
AGP_CBE<3>         12B2<> 18C7<>
AGP_DEVSEL_L       12B2<> 12C2< 18B7<> 37D5>
AGP_FRAME_L        12B2<> 12C2< 18B7<> 37D5>
AGP_GNT_L          12C2< 12D2<> 18B7< 37D5>
AGP_INT_L          14B5<> 18B7<>
AGP_IRDY_L         12B2<> 12C2< 18B7<> 37D5>
AGP_PAR            12B2<> 18B7> 37D5>
AGP_PIPE_L         12A2<> 12B2<
AGP_RBF_L          12A2<> 12C2< 18C6> 37D5>
AGP_REQ_L          12C2< 12D2<> 18B7<> 37D5>
AGP_SBA<0>         12B2< 18C6>
AGP_SBA<7..0>      37D5>
AGP_SBA<1>         12B2<> 18C6>
AGP_SBA<2>         12B2<> 18C6>
AGP_SBA<3>         12B2<> 18C6>
AGP_SBA<4>         12B2<> 18C6>
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AGP_SBA<5>         12B2<> 18C6>
AGP_SBA<6>         12B2<> 18C6>
AGP_SBA<7>         12B2<> 18C6<>
AGP_SB_STB         12B2< 12B2<> 18C6<> 37D5>
AGP_SB_STB_L       12A2< 12A2<> 18C6<> 37D5>
AGP_ST<0>          12A2<> 18C6<
AGP_ST<1>          12A2<> 18C6<
AGP_ST<2>          12A2<> 18C6<
AGP_STOP_L         12B2<> 12C2< 18B7<> 37D5>
AGP_STP_L          18C6<
AGP_SUS_STAT_L_PU  18C6<
AGP_TRDY_L         12B2<> 12C2< 18B7<> 37D5>
AGP_WBF_L          12A4<> 12B2< 18B7>
AIRPORT_CLKRUN_L   24C6<> 39C1>
AIRPORT_IDSEL      24C5<> 39B1>
AIRPORT_PCI_GNT_L  12D7<> 24D5<> 39C4>
AIRPORT_PCI_INT_L  14B5<> 14D7< 24D5<> 39C4>
AIRPORT_PCI_REQ_L  12A7< 12D7<> 24D6<> 39D4>
AIRPORT_PME_L_TP   24D5<>
AMP_CONTROL        25C5<> 25D5<>
ATI_AGP_FBSKEW<0>  19C2< 19C7<>
ATI_AGP_FBSKEW<1>  19C2< 19C7<>
ATI_BUS_CFG<0>     19B2< 19C7<>
ATI_BUS_CFG<1>     19B2< 19C7<>
ATI_BUS_CFG<2>     19B2< 19C7<>
ATI_CLK27M_IN      18C1< 19B7<
ATI_CLK27M_OSC     18D2<
ATI_CLK27M_OSC_SS  18B2< 18D1<
ATI_DBI_HI_PU      18C6<>
ATI_DBI_LO_PU      18C6<>
ATI_GPIO7_SPN      19C7<>
ATI_GPIO8_PD       19C7<>
ATI_GPIO9_SPN      19C7<>
ATI_GPIO10_SPN     19C7<>
ATI_GPIO11_SPN     19C7<>
ATI_GPIO12_SPN     19C7<>
ATI_GPIO13_SPN     19C7<>
ATI_HSYNC          19D5<> 22C8<
ATI_MEMTEST        18A6<>
ATI_MEMVMODE0      18A7<
ATI_MEMVMODE1      18A7<
ATI_OSC_OE         18D3<
ATI_PVDD_BYP       21D6<>
ATI_R2SET          19D6<>
ATI_RSET           19D6<>
ATI_RSTB_MSK       18C6<>
ATI_SSCLK_IN       18B1< 19B7<>
ATI_SSCLK_UF       18B1<>
ATI_TESTEN         19B7<
ATI_TMDS_CLKN      19B7> 20B4<
ATI_TMDS_CLKP      19B7> 20B4<
ATI_TMDS_DN<0>     19B7> 20B4<
ATI_TMDS_DN<1>     19B7> 20A4<
ATI_TMDS_DN<2>     19B7> 20A4<
ATI_TMDS_DP<0>     19B7> 20B4<
ATI_TMDS_DP<1>     19B7> 20A4<
ATI_TMDS_DP<2>     19B7> 20A4<
ATI_TPVDD_BYP      21D1<>
ATI_VSYNC          19D5<> 22C8<
ATI_X1CLK_SKEW<0>  19C2< 19C7<>
ATI_X1CLK_SKEW<1>  19B2< 19C7<>
BATTV_HIGH         31B7<>
BATTV_LOW          31B8<>
BATT_14PBUS_EN     31C1<>
BATT_14V_GATE      31C1<>
BATT_24PBUS_EN     31C2<>
BATT_24V_GATE      31C1<>
BATT_CLK           31A4<> 39C3>
BATT_DATA          31A4<> 39C3>
BATT_DIV           31A5<
BATT_LOW           31A6<>
BATT_LOW_L         31B6<>
BATT_NEG           31A4<> 38C6> 39C3>
BBANG_HRESET_L     23A4< 23C4<> 39C1>
BBANG_JTAG_TCK     23B3< 23C4<>
BBANG_TCK_EN       23B3<
BCKFD_PROT_EN_L    31C6<>
BCKFD_PROT_GATE    31D6<>
BRIGHT_PWM         22A1<> 39A7>
BRIGHT_PWM_UF      22A2<>
BT_USB_DM          14B1< 24B2<> 37B2> 39B6>
BT_USB_DP          14C1< 24B2<> 37B2> 39B6>
CAPSLOCK_LED       23A8<
CAPSLOCK_LED_L     23B8< 30C7<
CBUS_ADDR<0>       17B1<> 17B4>
CBUS_ADDR<1>       17B1<> 17B4>
CBUS_ADDR<2>       17B1<> 17B4>
CBUS_ADDR<3>       17B1<> 17B4>
CBUS_ADDR<4>       17B1<> 17B4>
CBUS_ADDR<5>       17B1<> 17B4>
CBUS_ADDR<6>       17B1<> 17B4>
CBUS_ADDR<7>       17B1<> 17B4>
CBUS_ADDR<8>       17B1<> 17B4>
CBUS_ADDR<9>       17B1<> 17B4>
CBUS_ADDR<10>      17B4> 17C1<>
CBUS_ADDR<11>      17B1<> 17B4>
CBUS_ADDR<12>      17B1<> 17B4>
CBUS_ADDR<13>      17B1<> 17B4>
CBUS_ADDR<14>      17B1<> 17B4>
CBUS_ADDR<15>      17B1<> 17B4>
CBUS_ADDR<16>      17B1<> 17B4<
CBUS_ADDR<17>      17B2<> 17B4>
CBUS_ADDR<18>      17B2<> 17B4>
CBUS_ADDR<19>      17B2<> 17B4>
CBUS_ADDR<20>      17B2<> 17B4>
CBUS_ADDR<21>      17B2<> 17B4>
CBUS_ADDR<22>      17A4> 17B2<>
CBUS_ADDR<23>      17A4> 17B2<>
CBUS_ADDR<24>      17A4> 17B2<>
CBUS_ADDR<25>      17A4> 17B2<>
CBUS_ADDR_16_UF    17B5<>
CBUS_BVD1_L        17B2<> 17C4<
CBUS_BVD2_L        17B2<> 17C4<
CBUS_CE1_L         17C1<> 17C4>
CBUS_CE2_L         17B4> 17C2<>
CBUS_DATA<0>       17A1<> 17A4<>
CBUS_DATA<1>       17A1<> 17A4<>
CBUS_DATA<2>       17A1<> 17A4<>
CBUS_DATA<3>       17A4<> 17C1<>
CBUS_DATA<4>       17A4<> 17C1<>
CBUS_DATA<5>       17A4<> 17C1<>
CBUS_DATA<6>       17A4<> 17C1<>
CBUS_DATA<7>       17A4<> 17C1<>
CBUS_DATA<8>       17A2<> 17A4<>
CBUS_DATA<9>       17A2<> 17A4<>
CBUS_DATA<10>      17A2<> 17A4<>
CBUS_DATA<11>      17A4<> 17C2<>
CBUS_DATA<12>      17A4<> 17C2<>
CBUS_DATA<13>      17A4<> 17C2<>
CBUS_DATA<14>      17A4<> 17C2<>
CBUS_DATA<15>      17A4<> 17C2<>
CBUS_DET_1_L       17C2<> 17C4< 39B8>
CBUS_DET_2_L       17A2<> 17C4< 39B8>
CBUS_INPACK_L      17B2<> 17B4<
CBUS_INT_L         14B5<> 14B7< 17A7<
CBUS_IORD_L        17B2<> 17C4>
CBUS_IOWR_L        17B2<> 17C4>
CBUS_MFUNC1_PD     17A7<> 17A7<
CBUS_MFUNC2_PD     17A7<> 17A7<
CBUS_MFUNC3_PD     17A7<> 17A7<
CBUS_MFUNC4_PD     17A7<> 17A7<
CBUS_MFUNC5_PD     17A7<> 17A7<
CBUS_MFUNC6_PD     17A7< 17A7<>
CBUS_OE_L          17C1<> 17C4>
CBUS_PCI_GNT_L     12D7<> 17A7<
CBUS_PCI_IDSEL     17B7<
CBUS_PCI_PERR_L    17B7<> 17D7<
CBUS_PCI_REQ_L     12A7< 12D7<> 17A7<
CBUS_PCI_RESET_L   17A7<
CBUS_PCI_SERR_L    17B7> 17D7<
CBUS_READY         17B1<> 17C4<
CBUS_REG_L         17B2<> 17C4>
CBUS_RESET_L       17B2<> 17C4>
CBUS_SUSPEND_PU    17A7< 17D7<
CBUS_VCCD0_L       17C4<>
CBUS_VCCD1_L       17C4<>
CBUS_VPPD0         17C4<>
CBUS_VPPD1         17C5<>
CBUS_VS1           17B2<> 17C4<>
CBUS_VS2           17B2<> 17C4<>
CBUS_WAIT_L        17B2<> 17B4<
CBUS_WE_L          17B1<> 17C4>
CBUS_WP_L          17A1<> 17B4<
CG_ADDRSEL         14B7<
CG_CLKOUT          14B6<>
CG_FSEL            14B7< 14C5<
CG_LOCK            14B7<
CG_RESET_L         14B7<
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```
CG_SYSCLK_EN       14A6< 14B7<
CHARGE_DISABLE     31A7<>
CHARGE_LED_L       30C6<> 30D7< 31D8<> 39D2>
CHGND1             38A6>
CHGND2             38A6>
CHGND3             38A6>
CHGND4             38A6> 39B6>
CHGND5             38A6>
CHGND6             38A6>
CLK10M_PMU_XIN     30B6<
CLK10M_PMU_XOUT    30B6<
CLK10M_PMU_XOUT_UF  30B7<
CLK18M_INT_EXT     14A6<> 36B1>
CLK18M_INT_XIN     14A5< 36B1>
CLK18M_INT_XOUT    14A5<> 36B1>
CLK18M_XTAL_IN     14A5< 36B1>
CLK25M_ENET_XIN    27A7< 36B1>
CLK25M_ENET_XOUT   27A7<> 36B1>
CLK25M_XTAL_IN     27A7<
CLK27M_GPU_XIN     36B1>
CLK27M_GPU_XOUT    36B1>
CLK27M_XTAL_IN     36B1>
CLK32K_PMU_XIN     30B3<>
CLK32K_PMU_XOUT    30B3<>
CLK32K_PMU_XOUT_UF  30B2<>
CLK33M_AIRPORT     12D8< 24D5<> 36C1> 39B1>
CLK33M_AIRPORT_UF  12C7<> 36C1>
CLK33M_CBUS        12D8< 17A7< 36C1>
CLK33M_CBUS_UF     12C7<> 36C1>
CLK33M_USB2        12C8< 26B7< 36C1>
CLK33M_USB2_UF     12C7<> 36C1>
CLK66M_AGP_15V_TP  12C4>
CLK66M_GPU_AGP     12C8< 18B7< 36C1>
CLK66M_GPU_AGP_UF  12C7<> 36C1>
CLKENET_LINK_GBE_REF  13C5< 27C8< 36B1>
CLKENET_LINK_GTX   13C5<> 36A1>
CLKENET_LINK_RX    13D5< 27C8< 36B1>
CLKENET_LINK_TX    13D5< 27D8< 36A1>
CLKENET_PHY_GBE_REF  27C7<> 36B1>
CLKENET_PHY_GTX    13C6< 27C7< 36A1>
CLKENET_PHY_RX     27C7<> 36B1>
CLKENET_PHY_TX     27D7<> 36B1>
CLKFW_LINK_LCLK    13C3<> 36A1>
CLKFW_LINK_PCLK    13C3<> 28C3< 36A1>
CLKFW_PHY_LCLK     13C2< 28B8< 36A1>
CLKFW_PHY_PCLK     28B4> 28C3< 36A1>
CLKLVDS_LN         19B5> 22A4<> 37C2> 39B7>
CLKLVDS_LP         19B5> 22A4<> 37C2> 39B7>
CLKLVDS_UN         19B5> 22A4<> 37C2> 39B7>
CLKLVDS_UP         19B5> 22A4<> 37C2> 39A7>
COMM_DTR_L         14C2> 25D1<> 39B2>
COMM_GPIO_L        14C2<> 25D2<> 39C2>
COMM_RESET_L       14C5<> 25C4<> 39C4>
COMM_RING_DET_L    14B5<> 14C7< 25C3<> 30C6<> 39C4>
COMM_RTS_L         14C2> 25D1<> 39B2>
COMM_RXD           14C2<> 25D1<> 39B2>
COMM_SHUTDOWN      14C5<> 25C4<> 39C4>
COMM_TRXC          14C2<> 25D2<> 39C2>
COMM_TXD_L         14C2<> 25D2<> 39C2>
COMP_DISABLE       22C2<>
COMP_ENABLE        22C1<>
COMP_RC            32C6<
CPU_AACK_L         5A7<> 8B6<> 8C2< 36D5>
CPU_ADDR<0>        5C7<> 8D6<>
CPU_ADDR<0..31>    36D5>
CPU_ADDR<1>        5C7<> 8D6<>
CPU_ADDR<2>        5C7<> 8D6<>
CPU_ADDR<3>        5C7<> 8D6<>
CPU_ADDR<4>        5C7<> 8D6<>
CPU_ADDR<5>        5C7<> 8C6<>
CPU_ADDR<6>        5C7<> 8C6<>
CPU_ADDR<7>        5C7<> 8C6<>
CPU_ADDR<8>        5C7<> 8C6<>
CPU_ADDR<9>        5C7<> 8C6<>
CPU_ADDR<10>       5B7<> 8C6<>
CPU_ADDR<11>       5B7<> 8C6<>
CPU_ADDR<12>       5B7<> 8C6<>
CPU_ADDR<13>       5B7<> 8C6<>
CPU_ADDR<14>       5B7<> 8C6<>
CPU_ADDR<15>       5B7<> 8C6<>
CPU_ADDR<16>       5B7<> 8C6<>
CPU_ADDR<17>       5B7<> 8C6<>
CPU_ADDR<18>       5B7<> 8C6<>
CPU_ADDR<19>       5B7<> 8C6<>
CPU_ADDR<20>       5B7<> 8C6<>
CPU_ADDR<21>       5B7<> 8C6<>
CPU_ADDR<22>       5B7<> 8C6<>
CPU_ADDR<23>       5B7<> 8C6<>
CPU_ADDR<24>       5B7<> 8C6<>
CPU_ADDR<25>       5B7<> 8C6<>
CPU_ADDR<26>       5B7<> 8C6<>
CPU_ADDR<27>       5B7<> 8C6<>
CPU_ADDR<28>       5B7<> 8C6<>
CPU_ADDR<29>       5B7<> 8C6<>
CPU_ADDR<30>       5B7<> 8C6<>
CPU_ADDR<31>       5B7<> 8B6<>
CPU_ARTRY_L        5A7<> 8B6<> 8D2< 36D5>
CPU_AVDD           5C3< 38D3>
CPU_AVDD_ADJ       5C2<>
CPU_AVDD_PG        5C3<>
CPU_AVDD_VIN       5C3<
CPU_AVDD_VOUT      5C3<>
CPU_BG_L           5C7< 8C2< 8D6<> 36D5>
CPU_BR_L           5C7> 8D2< 8D6< 36D5>
CPU_BUS_VSEL       5C4< 7A6<
CPU_CHKSTP_OUT_L   5B4<> 5C2< 39D8>
CPU_CHKS_L         5A4< 5D2<
CPU_CI_L           5A7> 8B6<> 36D5>
CPU_CLKOUT_SPN     5C4>
CPU_CLK_EN         8A6< 30C4<>
CPU_DATA<0>        6D8<> 8D4<>
CPU_DATA<0..31>    36D5>
CPU_DATA<1>        6D8<> 8D4<>
CPU_DATA<2>        6D8<> 8D4<>
CPU_DATA<3>        6D8<> 8D4<>
CPU_DATA<4>        6D8<> 8D4<>
CPU_DATA<5>        6D8<> 8D4<>
CPU_DATA<6>        6D8<> 8D4<>
CPU_DATA<7>        6D8<> 8D4<>
CPU_DATA<8>        6D8<> 8D4<>
CPU_DATA<9>        6D8<> 8D4<>
CPU_DATA<10>       6C8<> 8D4<>
CPU_DATA<11>       6C8<> 8D4<>
CPU_DATA<12>       6C8<> 8C4<>
CPU_DATA<13>       6C8<> 8C4<>
CPU_DATA<14>       6C8<> 8C4<>
CPU_DATA<15>       6C8<> 8C4<>
CPU_DATA<16>       6C8<> 8C4<>
CPU_DATA<17>       6C8<> 8C4<>
CPU_DATA<18>       6C8<> 8C4<>
CPU_DATA<19>       6C8<> 8C4<>
CPU_DATA<20>       6C8<> 8C4<>
CPU_DATA<21>       6C8<> 8C4<>
CPU_DATA<22>       6C8<> 8C4<>
CPU_DATA<23>       6C8<> 8C4<>
CPU_DATA<24>       6C8<> 8C4<>
CPU_DATA<25>       6C8<> 8C4<>
CPU_DATA<26>       6C8<> 8C4<>
CPU_DATA<27>       6C8<> 8C4<>
CPU_DATA<28>       6C8<> 8C4<>
CPU_DATA<29>       6C8<> 8C4<>
CPU_DATA<30>       6C8<> 8C4<>
CPU_DATA<31>       6C8<> 8C4<>
CPU_DATA<32>       6C8<> 8C4<> 8D8<
CPU_DATA<32..63>   36D5>
CPU_DATA<33>       6C8<> 8C4<> 8D8<
CPU_DATA<34>       6C8<> 8C4<> 8D8<
CPU_DATA<35>       6C8<> 8C4<> 8D8<
CPU_DATA<36>       6B8<> 8C4<> 8D8<
CPU_DATA<37>       6B8<> 8C4<> 8D8<
CPU_DATA<38>       6B8<> 8B4<> 8D8<
CPU_DATA<39>       6B8<> 8B4<> 8D8<
CPU_DATA<40>       6B8<> 8B4<> 8C8<
CPU_DATA<41>       6B8<> 8B4<> 8C8<
CPU_DATA<42>       6B8<> 8B4<> 8C8<
CPU_DATA<43>       6B8<> 8B4<> 8C8<
CPU_DATA<44>       6B8<> 8B4<> 8C8<
CPU_DATA<45>       6B8<> 8B4<> 8B8<
CPU_DATA<46>       6B8<> 8B4<> 8B8<
CPU_DATA<47>       6B8<> 8B4<> 8B8<
CPU_DATA<48>       6B8<> 8A8< 8B4<>
CPU_DATA<49>       6B8<> 8A8< 8B4<>
CPU_DATA<50>       6B8<> 8A8< 8B4<>
CPU_DATA<51>       6B8<> 8A8< 8B4<>
CPU_DATA<52>       6B8<> 8A8< 8B4<>
CPU_DATA<53>       6B8<> 8A8< 8B4<>
CPU_DATA<54>       6B8<> 8A8< 8B4<>
CPU_DATA<55>       6B8<> 8A8< 8B4<>
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```
CPU_DATA<56>       6B8<> 8B3< 8B4<>
CPU_DATA<57>       6B8<> 8B3< 8B4<>
CPU_DATA<58>       6B8<> 8B3< 8B4<>
CPU_DATA<59>       6B8<> 8B3< 8B4<>
CPU_DATA<60>       6B8<> 8B3< 8B4<>
CPU_DATA<61>       6B8<> 8B3< 8B4<>
CPU_DATA<62>       6A8<> 8B3< 8B4<>
CPU_DATA<63>       6A8<> 8B3< 8B4<>
CPU_DBG_L          5C4< 8A4<> 8C2< 36D5>
CPU_DRDY_L         5C4> 8A4< 8C2< 36D5>
CPU_DRDY_L_UF      36D5>
CPU_DTI<0>         5C4< 8A4<>
CPU_DTI<0..2>      36D5>
CPU_DTI<1>         5C4< 8A4<>
CPU_DTI<2>         5C4< 8A4<>
CPU_EDTI           5B2< 5C4<
CPU_EMODE0_L       5A4< 7A4<
CPU_EMODE1_L       5A4< 5C2<
CPU_GBL_L          5A7<> 8B6<> 36D5>
CPU_HIT_L          5A7> 8B6< 8D2< 36D5>
CPU_HRESET_INV     7A7<>
CPU_HRESET_L       5B4< 5C2< 7A5< 7A8< 23A2<> 39C8>
CPU_L1TSTCLK       5B2< 5B4<
CPU_L2TSTCLK       5B4< 5C2<
CPU_LSSD_MODE      5B4< 5C2<
CPU_MCP_L          5B4< 5D2<
CPU_M_DM           25A8< 25B6<
CPU_M_DP           25B6< 25B8<
CPU_PLL_CFG<0>     5C4< 7D3<
CPU_PLL_CFG<1>     5C4< 7D3<
CPU_PLL_CFG<2>     5C4< 7D3<
CPU_PLL_CFG<3>     5C4< 7D3<
CPU_PLL_CFG<4>     5C4< 7D3<>
CPU_PLL_CFGEXT     7D4<>
CPU_PLL_FS00       7C4<>
CPU_PLL_FS01       7C4<
CPU_PLL_FS10       7C4<
CPU_PLL_STOP_BASE  7C7<
CPU_PLL_STOP_OC    7C4<> 7C8<> 30B6<>
CPU_PMONIN_L       5A4< 5C2<
CPU_PULLDOWN       5A2< 5A4< 5A4< 5C7<>
CPU_PULLUP         5A4< 5A4< 5C2<
CPU_QACK_L         5B4< 8B6<> 36D5>
CPU_QREQ_L         5B4> 8B6< 8C2< 36D5>
CPU_SHD0_L         5A7<> 5D2<
CPU_SHD1_L         5A7<> 5D2<
CPU_SMI_L          5B4< 5C2< 30C4<>
CPU_SRESET_L       5B2< 5B4< 39C8>
CPU_SRWX_L         5A4< 5C2<
CPU_TA_L           5B4< 8A4<> 8D2< 36D5>
CPU_TBEN           5B4< 5D2< 8A6<>
CPU_TBST_L         5A7<> 8B6<> 36D5>
CPU_TEA_L          5B4< 8A4<> 8C2< 36D5>
CPU_THERM_DM       6A6<> 25A6<
CPU_THERM_DP       6A6<> 25A6<
CPU_TSIZ<0>        5A7<> 8B6<>
CPU_TSIZ<0..2>     36D5>
CPU_TSIZ<1>        5A7<> 8B6<>
CPU_TSIZ<2>        5A7<> 8B6<>
CPU_TS_L           5C7<> 8D2< 8D6<> 36D5>
CPU_TT<0>          5A7<> 8B6<>
CPU_TT<0..4>       36C5>
CPU_TT<1>          5A7<> 8B6<>
CPU_TT<2>          5A7<> 8B6<>
CPU_TT<3>          5A7<> 8B6<>
CPU_TT<4>          5A7<> 8B6<>
CPU_VCORE_HI_OC    7B8< 30D4<> 34C8< 34D7<
CPU_VCORE_PWR_SEQ  34D8<>
CPU_VCORE_SEQ      34D8<
CPU_VCORE_SEQ_L    34D8<
CPU_VCORE_SLEEP    5C3< 5D8<> 6C6<> 34C1< 34D2< 38D3>
                  39B2>
CPU_VCORE_SLEEP_F  34C2<>
CPU_VCORE_SNUB     34B3<
CPU_WT_L           5A7<> 8B6<> 36C5>
CSLOT_ADDR3_SPN    13B7>
CSLOT_ADDR4_SPN    13B7>
CSLOT_ADDR5_SPN    13B7>
CSLOT_ADDR6_SPN    13B7>
CSLOT_ADDR7_SPN    13B7>
CSLOT_ADDR8_SPN    13B7>
CSLOT_ADDR9_SPN    13B7>
CSLOT_CE1_L_SPN    13C7>
CSLOT_CE2_L_SPN    13C7>
CSLOT_IORD_L_SPN   13C7>
CSLOT_IOWAIT_L_PU  13C7<
CSLOT_IOWR_L_SPN   13C7>
CSLOT_OE_L_SPN     13C7>
CSLOT_WE_L_SPN     13C7>
CURRENT_THRESHOLD  31C4<
CY25811_S0         18B2<
CY25811_S1         18B2<
DCDC_EN            19A7<> 29C7<> 33B7<> 34C8<> 39C1>
DCDC_EN_L          33B6< 33B7<> 35C7<>
DDC_CLK_ISO        22D4<>
DDR_VREF           11D1< 11D3<> 11D5<> 11D6<> 11D8<>
                  38D3>
DVI_DDC_CLK        22D4<>
DVI_DDC_CLK_UF     22C5<> 22D3<> 39C7>
DVI_DDC_DATA       22C4<>
DVI_DDC_DATA_UF    22C5<> 39C7>
DVI_HPD            22C4<>
DVI_HPD_DIV        22C3<
DVI_HPD_UF         22C3< 22C5<> 39C7>
DVI_TRUN_ON_ILIM   22D2<
DVI_TURN_ON        22D3<>
DVI_TURN_ON_BASE   22D2<
EEPROM_ADDR        23D4<
EEPROM_WP_PD       23D3<>
EIDE_ADDR<0>       13B7> 24B8<
EIDE_ADDR<2..0>    37B5>
EIDE_ADDR<1>       13B7> 24B8<
EIDE_ADDR<2>       13B7> 24B8<
EIDE_CS0_L         13B7> 24B8< 37B5>
EIDE_CS1_L         13B7> 24B8< 37B5>
EIDE_DATA<0>       13C7<> 24C8<
EIDE_DATA<15..0>   37B5>
EIDE_DATA<1>       13C7<> 24C8<
EIDE_DATA<2>       13C7<> 24C8<
EIDE_DATA<3>       13C7<> 24C8<
EIDE_DATA<4>       13C7<> 24C8<
EIDE_DATA<5>       13B7<> 24B8<
EIDE_DATA<6>       13B7<> 24C8<
EIDE_DATA<7>       13B7<> 24C8<
EIDE_DATA<8>       13B7<> 24D8<
EIDE_DATA<9>       13B7<> 24D8<
EIDE_DATA<10>      13B7<> 24D8<
EIDE_DATA<11>      13B7<> 24D8<
EIDE_DATA<12>      13B7<> 24D8<
EIDE_DATA<13>      13B7<> 24C8<
EIDE_DATA<14>      13B7<> 24C8<
EIDE_DATA<15>      13B7<> 24C8<
EIDE_DMACK_L       13A7<> 24A8< 37B5>
EIDE_DMARQ         13A7< 24B8< 37B5>
EIDE_INT           13A7< 24A8< 37B5>
EIDE_IOCHRDY       13B7< 24A8< 37B5>
EIDE_OPTICAL_ADDR<0>  24A5<> 24B7< 39A4>
EIDE_OPTICAL_ADDR<2..0>  37B5>
EIDE_OPTICAL_ADDR<1>  24A5<> 24B7< 39A4>
EIDE_OPTICAL_ADDR<2>  24A6<> 24B7< 39A4>
EIDE_OPTICAL_CS0_L  24A5<> 24B7< 37B5> 39D4>
EIDE_OPTICAL_CS1_L  24A6<> 24B7< 37B5> 39D4>
EIDE_OPTICAL_DATA<0>  24A5<> 24C7< 39C4>
EIDE_OPTICAL_DATA<15..0>  37B5>
EIDE_OPTICAL_DATA<1>  24A5<> 24C7< 39C4>
EIDE_OPTICAL_DATA<2>  24A5<> 24C7< 39C4>
EIDE_OPTICAL_DATA<3>  24A5<> 24C7< 39C4>
EIDE_OPTICAL_DATA<4>  24A5<> 24C7< 39C4>
EIDE_OPTICAL_DATA<5>  24A5<> 24B7< 39C4>
EIDE_OPTICAL_DATA<6>  24A5<> 24C7< 39C4>
EIDE_OPTICAL_DATA<7>  24A5<> 24C7< 39B4>
EIDE_OPTICAL_DATA<8>  24A6<> 24D7< 39B4>
EIDE_OPTICAL_DATA<9>  24A6<> 24D7< 39B4>
EIDE_OPTICAL_DATA<10>  24A6<> 24D7< 39B4>
EIDE_OPTICAL_DATA<11>  24A6<> 24D7< 39B4>
EIDE_OPTICAL_DATA<12>  24A6<> 24D7< 39B4>
EIDE_OPTICAL_DATA<13>  24A6<> 24C7< 39B4>
EIDE_OPTICAL_DATA<14>  24A6<> 24C7< 39B4>
EIDE_OPTICAL_DATA<15>  24A6<> 24C7< 39B4>
EIDE_OPTICAL_DMAACK_L  24A6<> 24A7< 37A5> 39A4>
EIDE_OPTICAL_DMA_RQ  24A6<> 24B7< 37A5> 39A4>
EIDE_OPTICAL_INT   24A5<> 24A7< 37A5> 39D4>
EIDE_OPTICAL_IOCHRDY  24A5<> 24A7< 37A5> 39D4>
EIDE_OPTICAL_RD_L  24A6<> 24A7< 37B5> 39A4>
EIDE_OPTICAL_RST_L  24A7< 24B5<> 37A5> 39D4>
EIDE_OPTICAL_WR_L  24A5<> 24A7< 37A5> 39D4>
EIDE_RD_L          13A7> 24A8< 37B5>
EIDE_RST_L         13B7> 24A8< 37B5>
```

```
EIDE_WR_L          13A7> 24A8< 37B5>
ENET_COL           13C5< 27B7> 37A5>
ENET_COMA          27B7<>
ENET_CRS           13C5< 27B7> 37A5>
ENET_CTAP_CHGND    27A1< 38A6>
ENET_ENERGY_DET    14B5<> 27B7<>
ENET_HSDACM        27A7<>
ENET_HSDACP        27A7<>
ENET_LINK_RXD<0>   13C5< 27C7>
ENET_LINK_RXD<7..0>  37A5>
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[illegible]

[illegible]

[illegible]

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RSDP4_TP         26C5>
RSDP5_TP         26C5>
RUN_ON_AC        29C6<>
SI_A2            20B7<
SI_DDC_CLK       19C5<> 20B7<
SI_DDC_DATA      19C5<> 20B7<
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SI_MSEN          20B6<>
SI_PD            20B7<
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SI_VREF          20A5< 20A7<
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SLEEP_LED        23C1< 25C7<> 39B6>
SLEEP_LED_I      23D1<
SLEEP_LED_L      23D1<
SLEEP_LED_SW_L   23C2<>
SLEEP_LED_UF     23C1<
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SLEEP_LS5_EN_L   33A5<>
SLEEP_L_LS5      19A7<> 27A8<> 33A5<> 34C8<> 35C8<
SLEEP_L_LS5_EN_L  33A6<>
SLEEP_L_LS5_INV  35A3< 35C2< 35C8<>
SLEEP_L_LS5_NET  33B3<> 35C8<>
SLEEP_NET        33A3<>
SLEEP_NET_INV    33A3<>
SMC_TP           26B5<
SND_AGND         25C7<> 38B6>
SND_AMP_MUTE     25C8< 25D6<> 39A4>
SND_AMP_MUTE_F   25C7< 25D6<>
SND_AMP_MUTE_L   14C5<> 25D5<>
SND_CLKOUT       14B1< 25D8< 36B1> 39D6>
SND_CLKOUT_F     25C7<> 25D7<
SND_HP_MUTE      25C5<>
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SND_HP_MUTE_L    14C5<> 25C6<>
SND_HP_SENSE_L   14B5<> 25D6<> 39C6>
SND_HW_RESET_L   14A7< 14B5<> 25C8< 39C6>
SND_HW_RESET_L_F  25C6<> 25C7<
SND_LIN_SENSE_L  14B5<> 25D6<> 39C6>
SND_RCLK         14B1< 25C8< 36B1> 39C6>
SND_RCLK_F       25C7< 25D7<>
SND_SYNC         14B1< 25D8< 39D6>
SND_SYNC_F       25C7<> 25D7<
SND_TO_AUDIO     14B1< 25D8< 39D6>
SND_TO_AUDIO_F   25D6<> 25D7<
SOFT_PWR_ON_L    22D1< 23A8< 30A8< 30C6<> 30D7<
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SRCLK_TP         26A5> 39A4>
SRMOD_TP         26A5< 39A4>
ST7_ICP_SEL_PD   23A2< 23D6<
ST7_KBD_LED_OUT  23A4< 23C6<>
ST7_OSC1         23D5<
ST7_OSC2         23D5<>
ST7_P86_PD       23B2< 23C4<>
ST7_RESET_L      23D5<>
ST7_SENSOR4_SCK_PD  23B2< 23D4<>
ST7_SENSOR4_SDA_PD  23B2< 23D4<>
ST7_SENSOR5_SCK_PU  23B2< 23D4<>
ST7_SENSOR5_SDA_PU  23B2< 23D4<>
ST7_SLEEP_LED_H  23C2<> 23C4<>
ST7_XTAL_IN      23C5<
STOP_AGP_L       12D2< 12D4<>
SUPPLY_M_DM      25B6< 25B8<
SUPPLY_M_DP      25B6< 25B8<
SUTRO_ALS_GAIN_SW  23C4<> 24B2<> 39C2>
SUTRO_ALS_OUT    23C4<> 24B2<> 39C2>
SYSCLK_CPU       5C4< 8A4< 36D1>
SYSCLK_CPU_UF    8A6<> 36D1>
SYSCLK_DDRCLK_A0  9D4< 11D8<> 36D1>
SYSCLK_DDRCLK_A0_L_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_A0_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_A1  9D4< 11A6<> 36D1>
SYSCLK_DDRCLK_A1_L  9D4< 11A6<> 36D1>
SYSCLK_DDRCLK_A1_L_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_A1_UF  9B6<> 9D5< 36D1>
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SYSCLK_DDRCLK_B0_L  9C4< 11D3<> 36C1>
SYSCLK_DDRCLK_B0_L_UF  9B6<> 9C5< 36D1>
SYSCLK_DDRCLK_B0_UF  9B6<> 9D5< 36D1>
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SYSCLK_DDRCLK_B1_L  9D4< 11A5<> 36C1>
SYSCLK_DDRCLK_B1_L_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_B1_UF  9B6<> 9D5< 36D1>
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TEST_TP          26A5< 39A4>
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THERM1_DP        25A5< 25A5< 25B5<> 25B5< 37A2>
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THERM1_M_DP      37A2>
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THERM2_A_DP      25A6< 25A8< 37A2>
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THERM2_DP        25A5< 25B5<> 25B5< 37A2>
THERM2_M_DM      37A2>
THERM2_M_DP      37A2>
THERM_INV        25A5<>
THERM_L_OC       25A4<> 30B4<>
TMDS_CLKN        20B3< 20C1< 20C3< 22B7<> 37B2>
TMDS_CLKP        20B3< 20C2< 20C3< 22C7<> 37B2>
TMDS_CLK_CWP     20C1<
TMDS_CONN_CLKN   22B6<> 22C7<> 37B2> 39A8>
TMDS_CONN_CLKP   22C6<> 22C7<> 37B2> 39D7>
TMDS_CONN_DN<0>  22C7<> 22D6<>
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TMDS_CONN_DP<0>  22B7<> 22D6<>
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TMDS_D2_CWP      20A1<
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TMDS_DN<1>       20A3< 20B1< 20C3< 22B8<> 37B2>
                 39A8>
TMDS_DN<2>       20A1< 20A3< 20B3< 22B7<> 37B2>
                 39A8>
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TMDS_DP<1>       20A3< 20B2< 20C3< 22B8<> 37B2>
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TMDS_DP<2>       20A2< 20A3< 20B3< 22B7<> 37B2>
                 39A8>
TPAD_F_RXD       23A7<> 39C4>
TPAD_F_TXD       23A7<> 39C4>
TPAD_RXD         23A8< 30C2< 30C4<>
TPAD_TXD         23A8< 30B2< 30C4<>
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TV_COMP          22A6<> 39D6>
TV_GND1          22B6<> 38B6> 39A7>
TV_GND2          22A6<> 38B6> 39A7>
TV_Y             22A6<> 39D6>
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UIDE_ADDR<2>     13D7> 24B4<
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UIDE_DATA<8>     13D7<> 24C4<
UIDE_DATA<15..8>  37C5>
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UIDE_DIOR_L      13C7<> 24A4< 37C5>
UIDE_DIOW_L      13C7<> 24A4< 37C5>
UIDE_DMACK_L     13C7<> 24A4< 37C5>
UIDE_DMARQ       13C7<> 37C5>
UIDE_INTRQ       13C7< 37C5>
UIDE_IOCHRDY     13C7< 24A4< 37C5>
UIDE_RST         13C7<> 38D3>
UIDE_RST_L       13C7<> 24A4< 37C5>
USB2_PCI_CNT_I   12C7<> 26B7<
USB2_PCI_INT_L   14B5<> 14C7< 26A8<
USB2_PCI_REQ_L   12A7< 12D7<> 26B7>
USB_D1N          14C1< 26A5> 26B4<
USB_D1P          14C1< 26A4< 26A5>
USB_D2N          14D1< 26A4< 26A5>
USB_D2P          14D1< 26A4< 26A5>
USB_DAN          14B2<> 14D2< 26A5>
USB_DAP          14B2<> 14D2< 26A5>
USB_DBN          14B2<> 14D2<
USB_DBP          14B2<> 14D2<
USB_DCN          14B2<> 14C2< 26A5>
USB_DCP          14B2<> 14C2< 26A5>
USB_DDN          14B2<> 14C2<
USB_DDP          14B2<> 14C2<
USB_DEN          14B2<> 14B2< 37B2>
USB_DEP          14B2<> 14C2< 37B2>
USB_DFN          14B2<> 14B2< 37B2>
USB_DFP          14B2<> 14B2< 37B2>
USB_OC_AB_L      14B2< 14C7<
USB_OC_CD_L      14B2< 14C7<
USB_OC_EF_L      14B2< 14D7<
USB_PWREN_AB_L   14B2<> 14C7<
USB_PWREN_CD_L   14B2<> 14C7<
USB_PWREN_EF_L   14B2<> 14D7<
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VCORE_BST        34C5<> 38C1>
VCORE_CC         34B6<> 38B1>
VCORE_CNTL_RC    19A3<>
VCORE_DH         34B5<> 38C1>
VCORE_DL         34B5<> 38C1>
VCORE_FAST<1>    34D3< 34D5<
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VCORE_FAST<4>    34D3< 34D5<
VCORE_FB         34B5< 38B1> 39A2>
VCORE_GND        34B5<> 38B1>
VCORE_GNDA       34B6<>
VCORE_GNDDIV     34A4< 34B5< 38B1>
VCORE_GNDDIV_TEST  34A3<>
VCORE_GNDSNS     34A2<> 34A4< 38B1>
VCORE_GNDSNS_TEST  34A3<>
VCORE_ILIM       34C6<> 38C1>
VCORE_LX         34B5<> 38C1>
VCORE_MUX_EN     34D5<> 39A2>
VCORE_MUX_SEL    34D5<>
VCORE_REF        34B6<> 38C1>
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VCORE_SEL_ON     34B6<>
VCORE_SHDN_L     5C3< 34C6<>
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VCORE_SLOW<2>    34D6<
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VCORE_SNS        34A1<> 38B1>
VCORE_TIME       34B4<> 38B1>
VCORE_TON        34B6< 38C1>
VCORE_VCC        34C6< 38C1>
VCORE_VGATE      14B5< 14B7< 34B4> 38B1>
VCORE_VID0       39A3>
VCORE_VID1       39A3>
VCORE_VID2       39A3>
VCORE_VID3       39A3>
VCORE_VID4       39A3>
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VCORE_VID<2>     34A2<> 34B8< 34D4<>
VCORE_VID<3>     34A2<> 34B8< 34D4<>
VCORE_VID<4>     34A2<> 34B8< 34D4<>
VGA_B            22C6<> 22D7< 39D7>
VGA_G            22C5<> 22D7< 39D7>
VGA_HSYNC        22C6<> 22C7< 39D7>
VGA_HSYNC_BUF    22C8<>
VGA_R            22C5<> 22D7< 39D7>
VGA_VSYNC        22C5<> 22C7< 39D7>
VGA_VSYNC_BUF    22C8<>
EV_LCDDATA20_PU  19C7<>
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	C
SCALE: NONE	SHT 42 OF 44	

*** Part Cross-Reference for the entire design ***

B81 PCB_STANDOFF 4
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J11 COM_F14RT_S2MT_SM 32
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U18	LTC1625	32
U19	PWR_CNTRL_TPS2211	17
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U22	MAX1715	35
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