

- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
		?		?	?

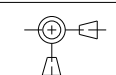
Page	Circuits	ENG	Block
1	Table of Contents	KG	
2	Block Diagram	KG	
3	Microprocessor	KG	
4	L3 CACHE & BYPASS	KG	Processor
5	PANGEA PROCESSOR IF	KG	
6	PANGEA SDRAM IF & SDRAM DIMMS	KG	Sys Memory
7	SYSTEM CLOCKS, TERMS, CKE LATCH	KG	Clocks
8	PANGEA AGP INTERFACE, SYSTEM ROM	KG,LL	
9	VIDEO ASIC SEC 1 (AGP & VIDEO OUT)	LL	AGP,
10	VIDEO ASIC SEC 2 (FRAME BUFFER IF)	LL	Graphics
11	GRAPHICS SDRAMS	LL	& ROM
12	VIDEO ASIC SEC 3 (UNUSED CRUD!)	LL	
13	PANGEA ETHERNET, FIREWIRE, PWR/GNDS	RM	
14	PANGEA BYPASS	KG	
15	Ethernet PHY	RM	Enet, FW
16	Firewire PHY, Termination	LL	
17	PANGEA ATA, & PCMCIA BUSSES	RM	
18	PANGEA SER/AUD/USB, BOOTSTRAP PINS	RM	HD, Cdbus
19	USB CONN & PWR	RM	Modem, USB
20	MLB Pull-ups	ALL	PUs
21	L3 VOLTAGE REGULATORS, BOOTBANGER	KK	
22	Voltage Regulators	KK	Power
23	Power Manager Unit	KK	
24	ESP, LA CONNECTORS, AND CPU BYPASS	KG	
25	Internal & External Video Conns	LL	CONNECTORS
26	HD/CD/MODEM/PCMCIA/KITCHENSINK CONN'S	RM	
27	DC/DC CONVERTER (5V AND 3.3V)	KK	POWER STUFF
28	MORE POWER SUPPLY STUFF	KK	
29	TUMBLER AUDIO, CONTROL & D/A	LH	
30	TUMBLER AUDIO, HEADPHONE DRIVER	LH	Audio
31	TUMBLER AUDIO, INTERNAL MIC AND CALL PROGRESS	LH	
32	TUMBLER AUDIO, POWER AMPLIFIER	LH	
33	HOLES AND SLOTS, AND EMC TABLES	KG	
34-40	CONSTRAINT TABLES	ALL	
41-44	Part Tables	RM	

CROSS REFERENCES ACCURATE? YES  
PART TABLES ACCURATE? YES

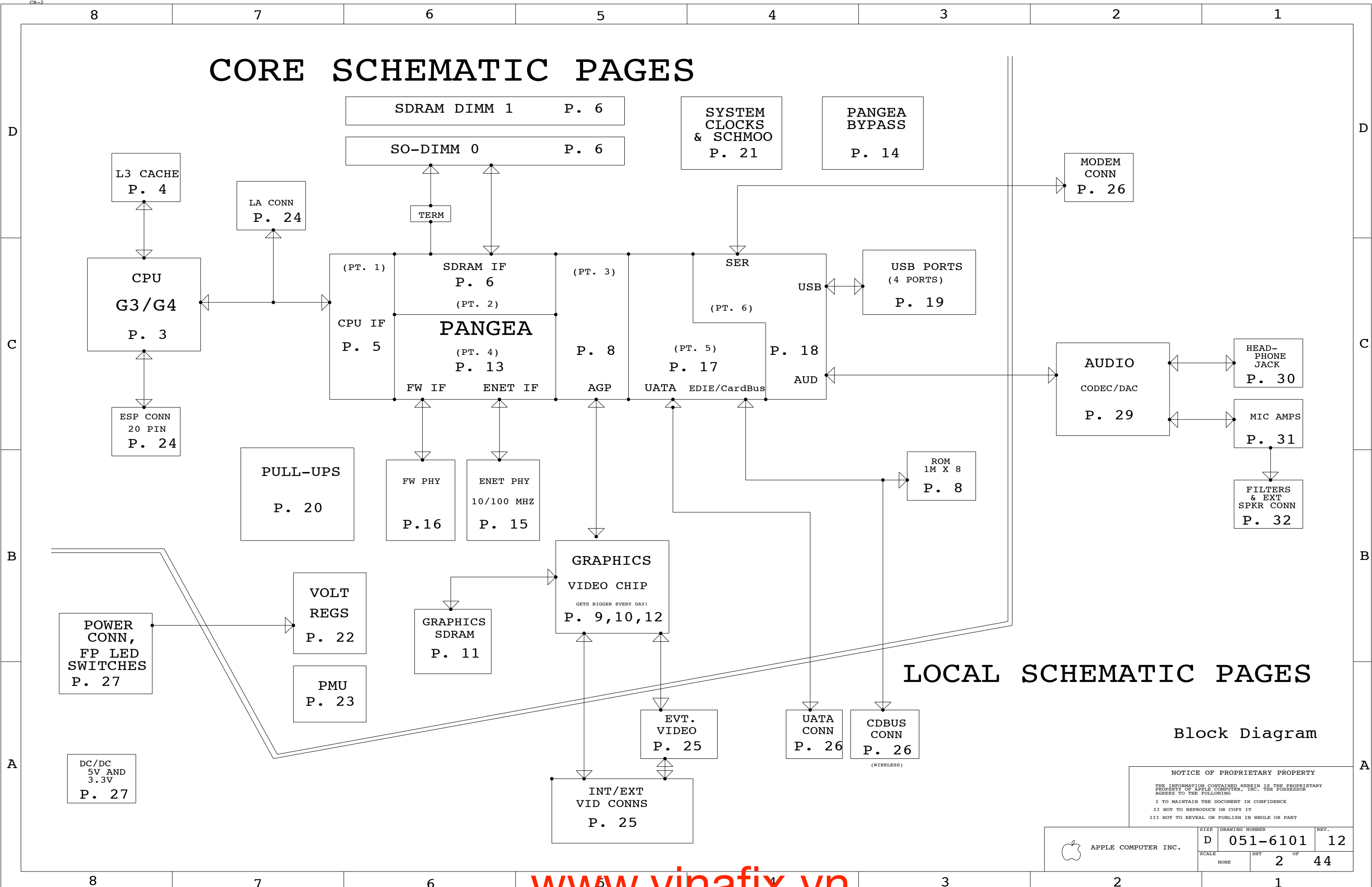
**DVT**  
**AUG 30, 2001**

POWER RAIL DEFINITIONS

	RUN	SLEEP	SHUTDOWN
+5V	ON	ON	OFF
+5VSD	ON	OFF	OFF
+12V_MAIN	ON	ON	ON
+12VSD	ON	OFF	OFF
+3.3V	ON	ON	OFF

DIMENSIONS ARE IN MILLIMETERS		METRIC		Apple Computer Inc.	
xx : _____	_____	DRAPFER	DESIGN CK	NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	
x.xx : _____	_____	ENG APPD	MFG APPD		
x.xxx : _____	_____	QA APPD	DESIGNER		
ANGLES : _____	_____	RELEASE	SCALE		
DO NOT SCALE DRAWING		NONE		TITLE	
 THIRD ANGLE PROJECTION		MATERIAL/FINISH NOTED AS APPLICABLE		DRAWING NUMBER	
		SIZE D		051-6101	
				REV. 12	
				SHT 1 OF 44	

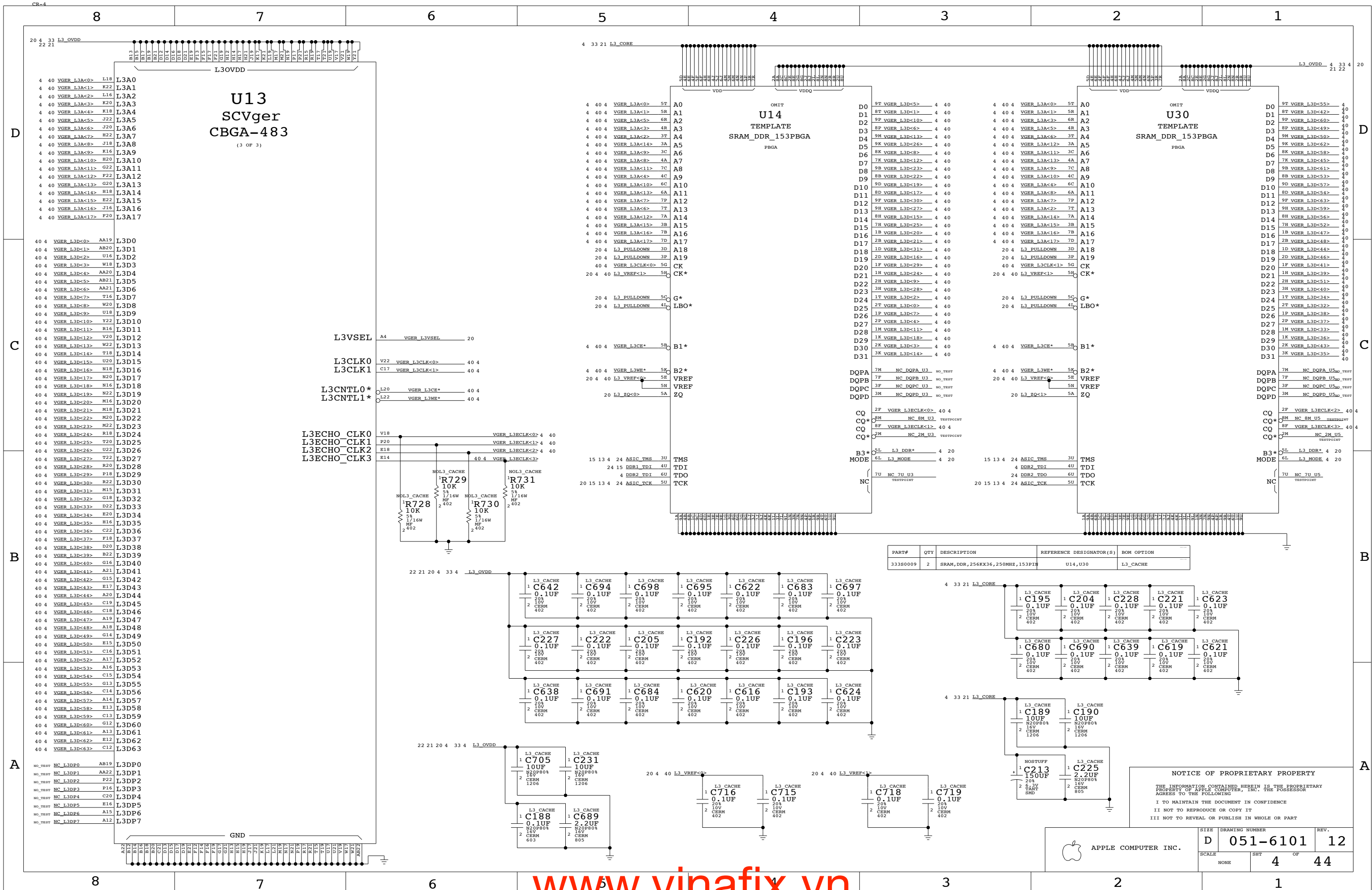
# CORE SCHEMATIC PAGES



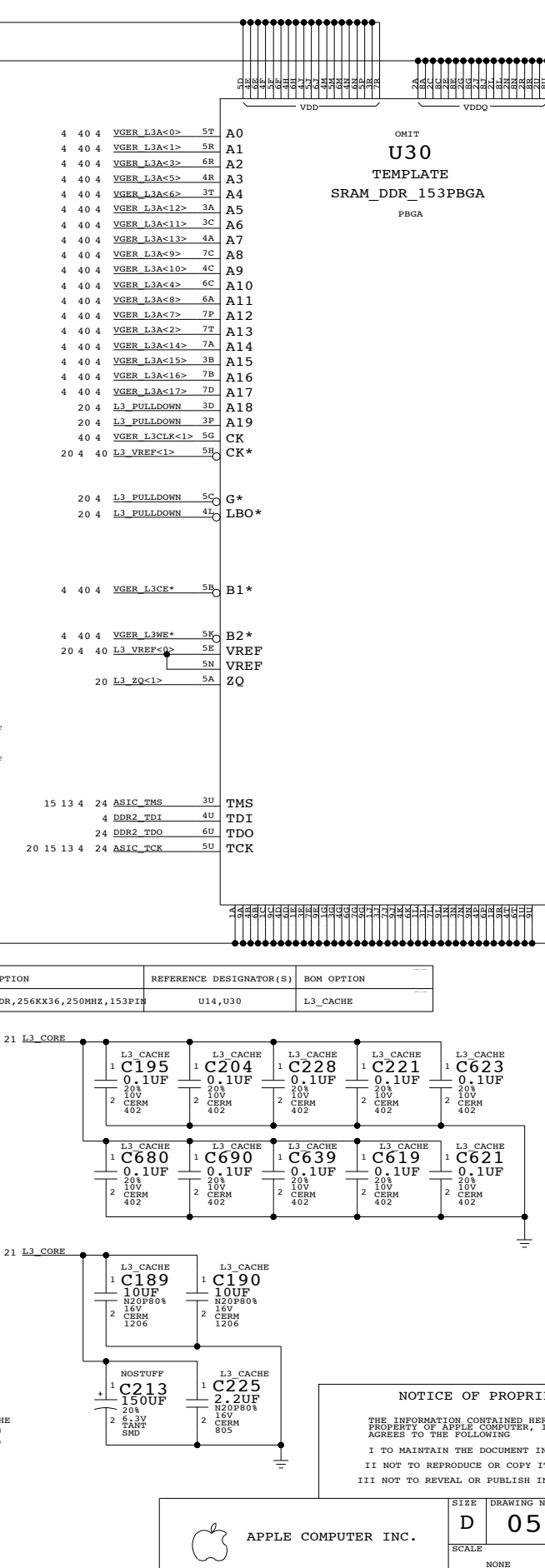
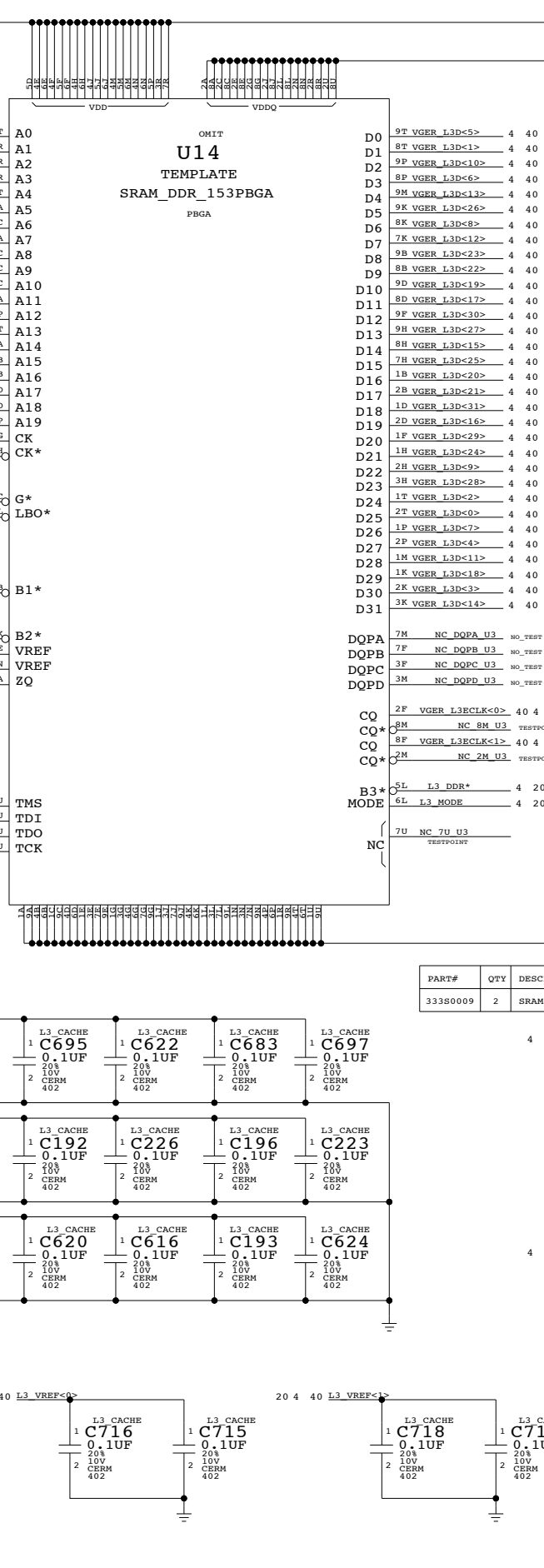
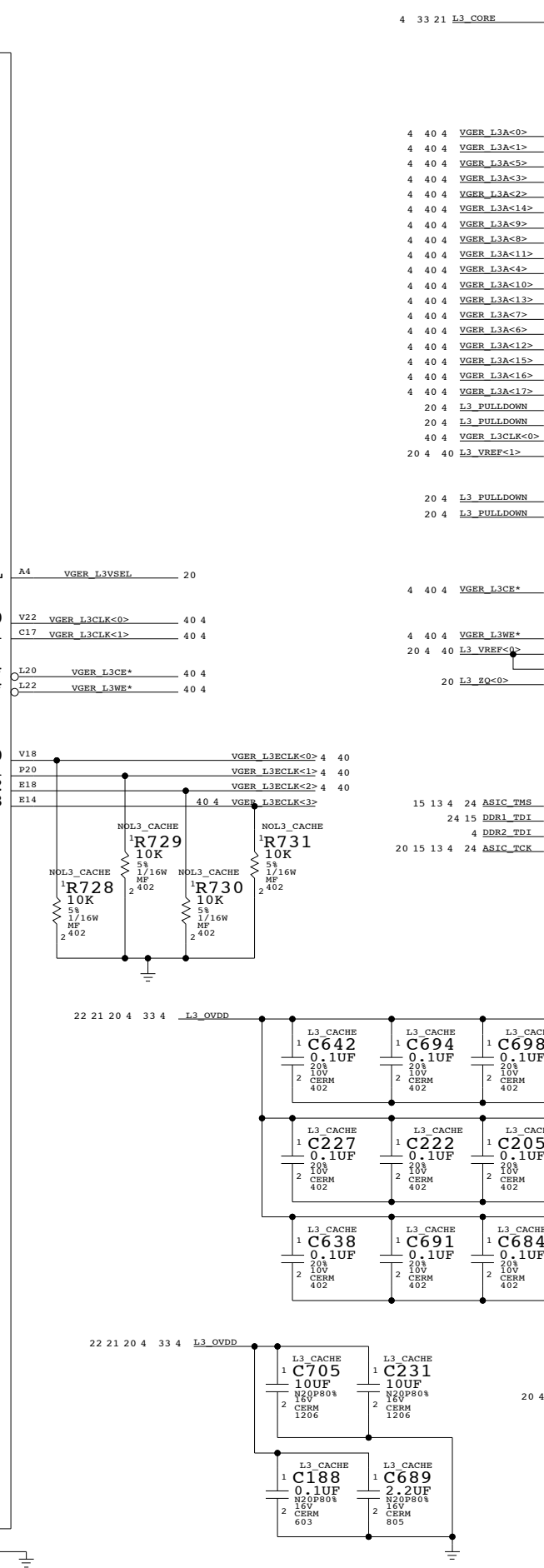
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6101	12
SCALE	SHT	OF	
NONE	2	44	





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40	40	VGER_L3A<1>	K22	L3A1
40	40	VGER_L3A<2>	L16	L3A2
40	40	VGER_L3A<3>	K20	L3A3
40	40	VGER_L3A<4>	M18	L3A4
40	40	VGER_L3A<5>	J22	L3A5
40	40	VGER_L3A<6>	J20	L3A6
40	40	VGER_L3A<7>	H22	L3A7
40	40	VGER_L3A<8>	J18	L3A8
40	40	VGER_L3A<9>	K16	L3A9
40	40	VGER_L3A<10>	H20	L3A10
40	40	VGER_L3A<11>	G22	L3A11
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40	40	VGER_L3D<59>	C13	L3D59
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40	40	VGER_L3D<61>	A13	L3D61
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NO_TEST	NC	L3DP1	AA22	L3DP1
NO_TEST	NC	L3DP2	P22	L3DP2
NO_TEST	NC	L3DP3	P16	L3DP3
NO_TEST	NC	L3DP4	C20	L3DP4
NO_TEST	NC	L3DP5	E16	L3DP5
NO_TEST	NC	L3DP6	A15	L3DP6
NO_TEST	NC	L3DP7	A12	L3DP7



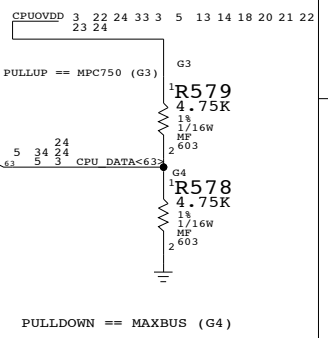
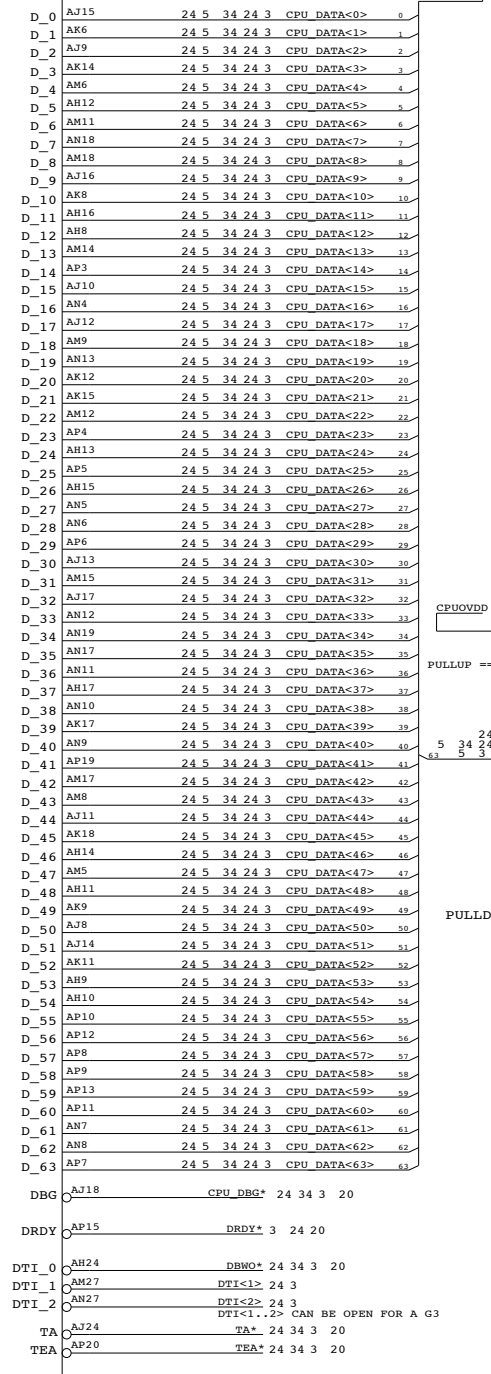
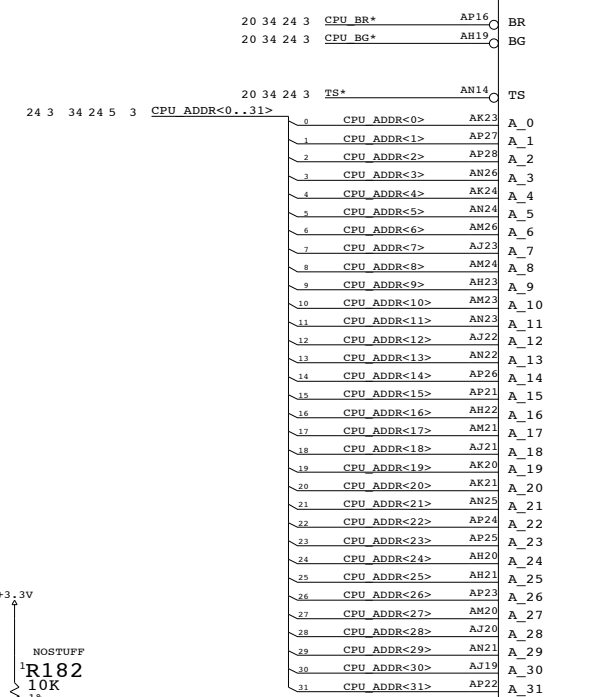
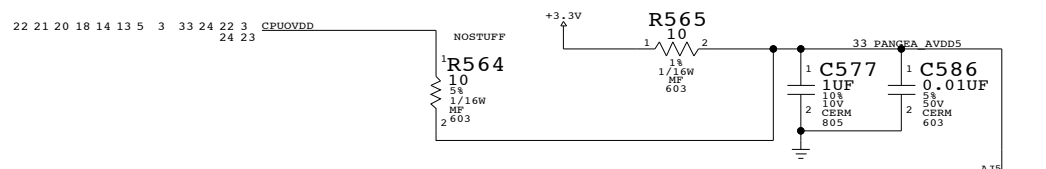
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
33380009	2	SRAM,DDR,256KX36,250MHZ,153PIN	U14,U30	L3_CACHE

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6101	12
SCALE	SHT	OF	
NONE	4	44	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0555	1	PANGEA	U6	PROJECT	OMIT
343S0194	1	PANGEA, 688 BALL PANGEA	U6	PROJECT	

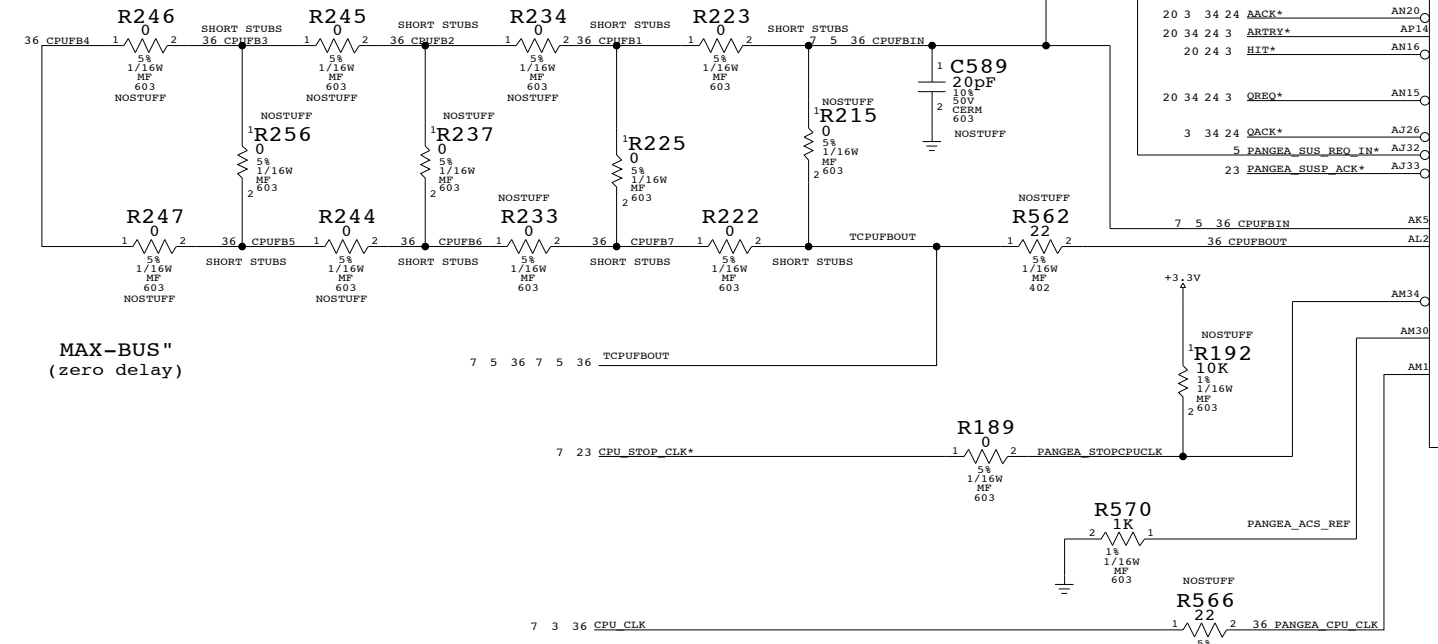
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
343S0557	343S0194		U6	700 BALL PANGEA



D  
C  
B  
A

D  
C  
B  
A

ROUTE DELAY NETWORK ON INTERNAL LAYER



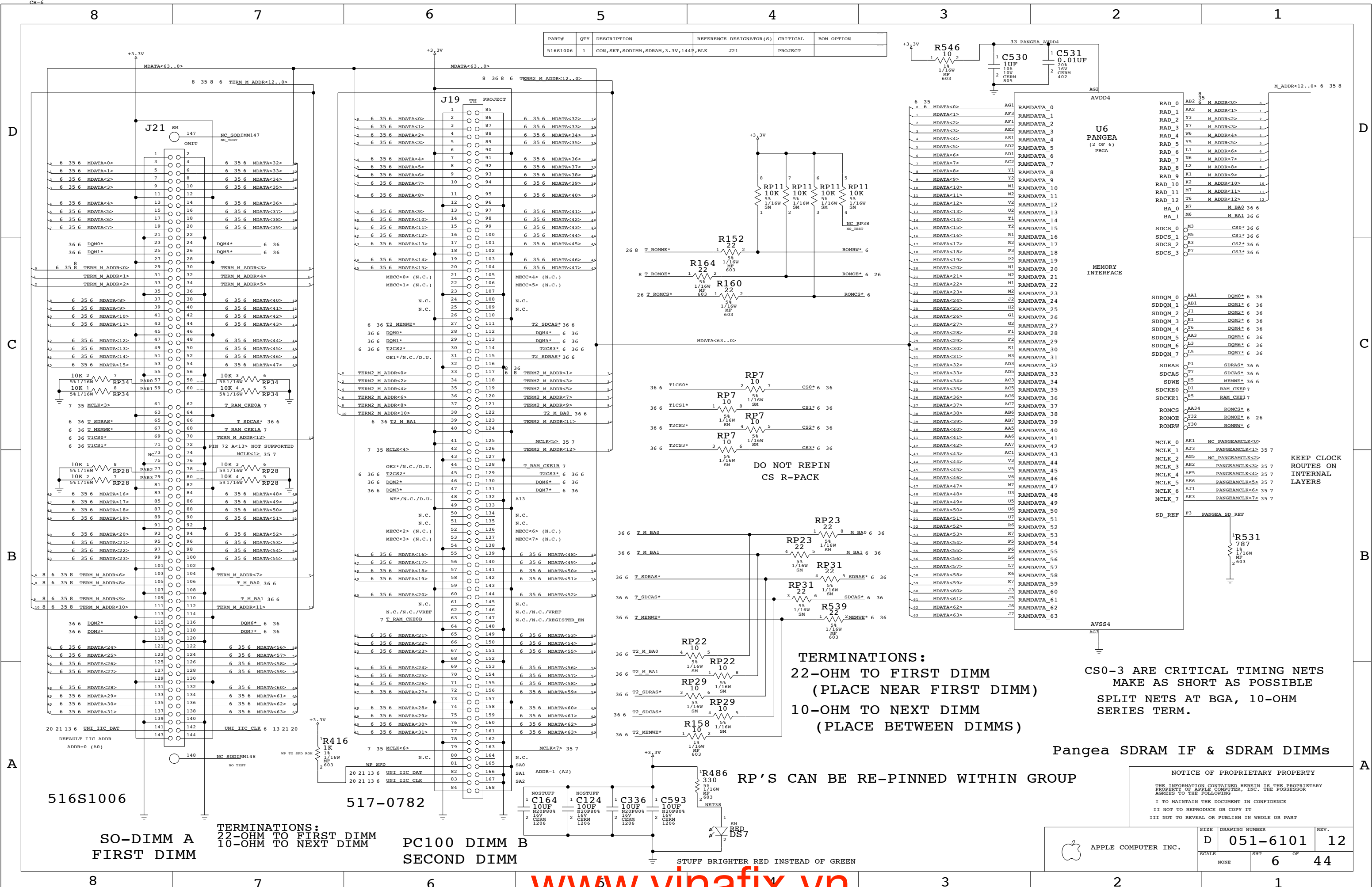
Series R on CPU\_CLK work with shunt R to drop voltage to 1.8V/2.5V

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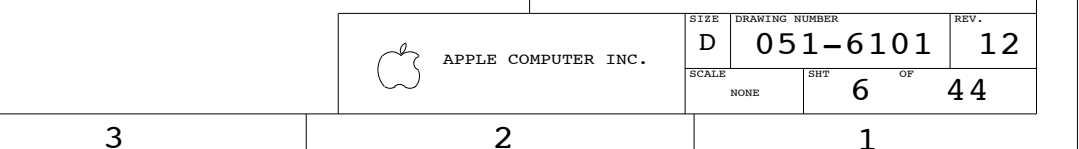
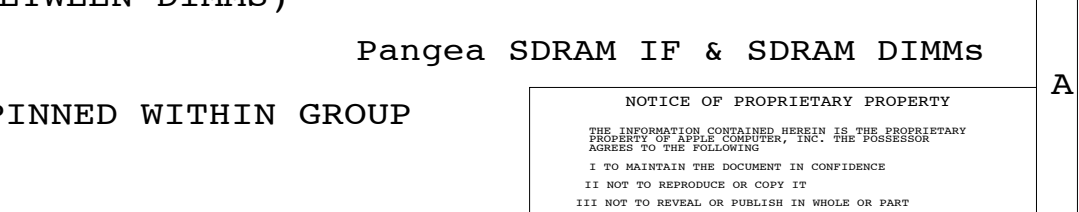
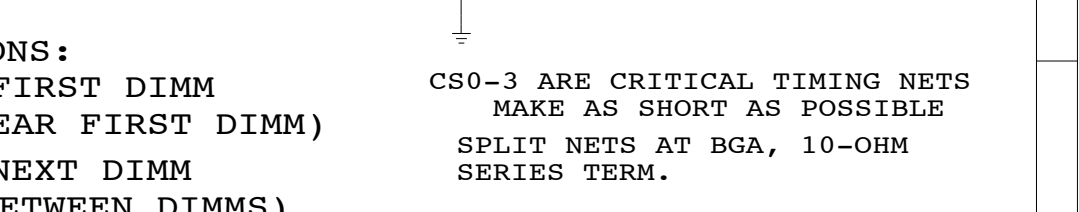
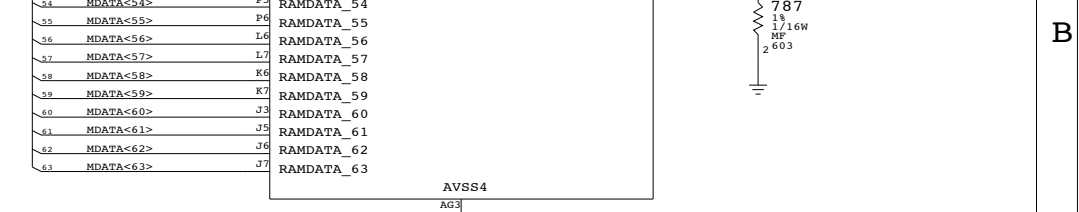
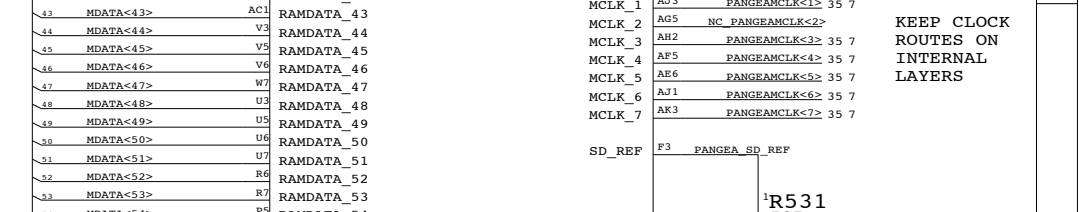
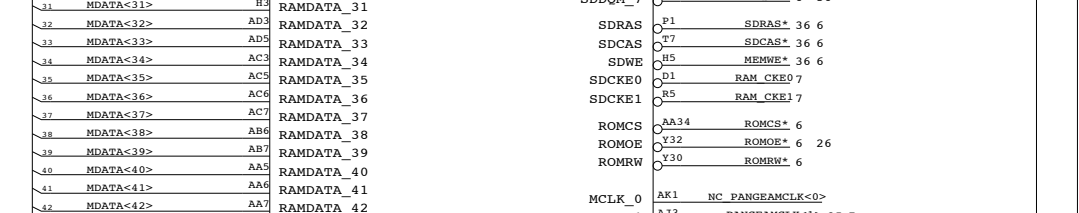
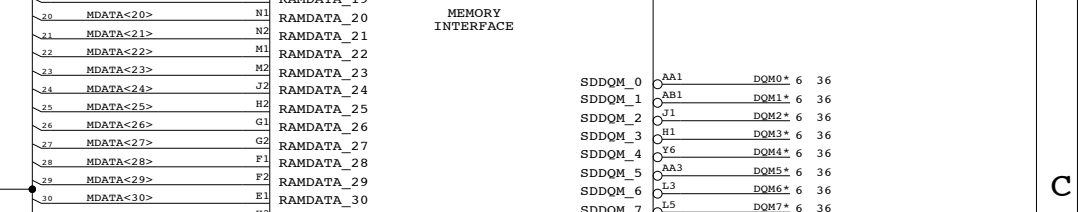
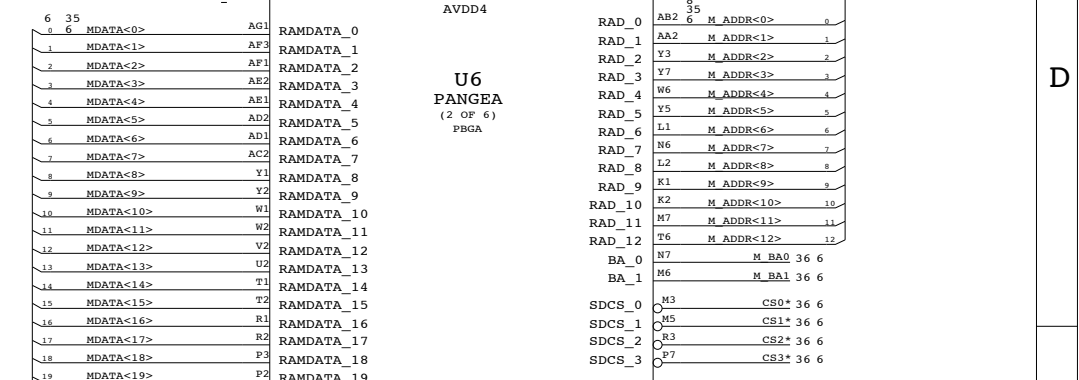
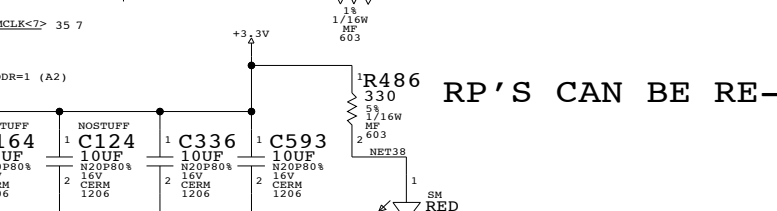
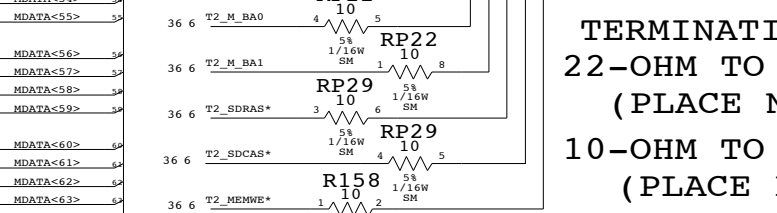
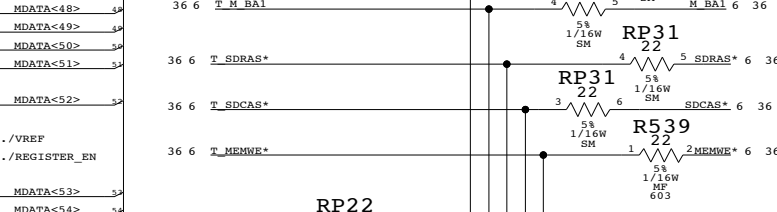
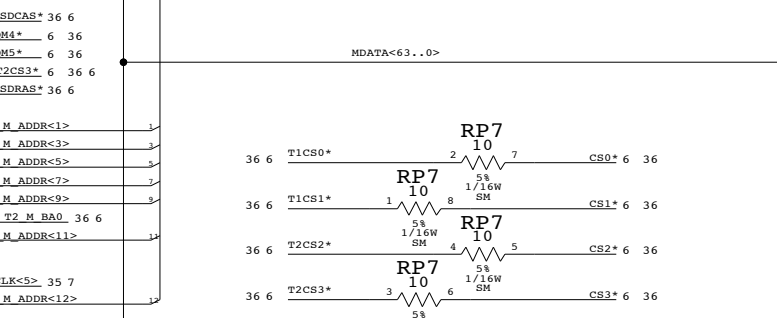
Pangea Processor IF

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6101	12
SCALE	SHT	OF	
NONE	5	44	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S1006	1	CON, SKT, SODIMM, SDRAM, 3.3V, 144P, BLK	J21	PROJECT	



TERM	DESCRIPTION	TERM	DESCRIPTION
1	MDATA<0>	85	MDATA<32>
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516S1006

517-0782

C114 10UF N20P80% 2 16V CERM 1206

C124 10UF N20P80% 2 16V CERM 1206

C336 10UF N20P80% 2 16V CERM 1206

C593 10UF N20P80% 2 16V CERM 1206

R486 330 1% 1/16W MF 603

SO-DIMM A  
FIRST DIMM

PC100 DIMM B  
SECOND DIMM

RP'S CAN BE RE-PINNED WITHIN GROUP

TERMINATIONS:  
22-OHM TO FIRST DIMM  
(PLACE NEAR FIRST DIMM)  
10-OHM TO NEXT DIMM  
(PLACE BETWEEN DIMMS)

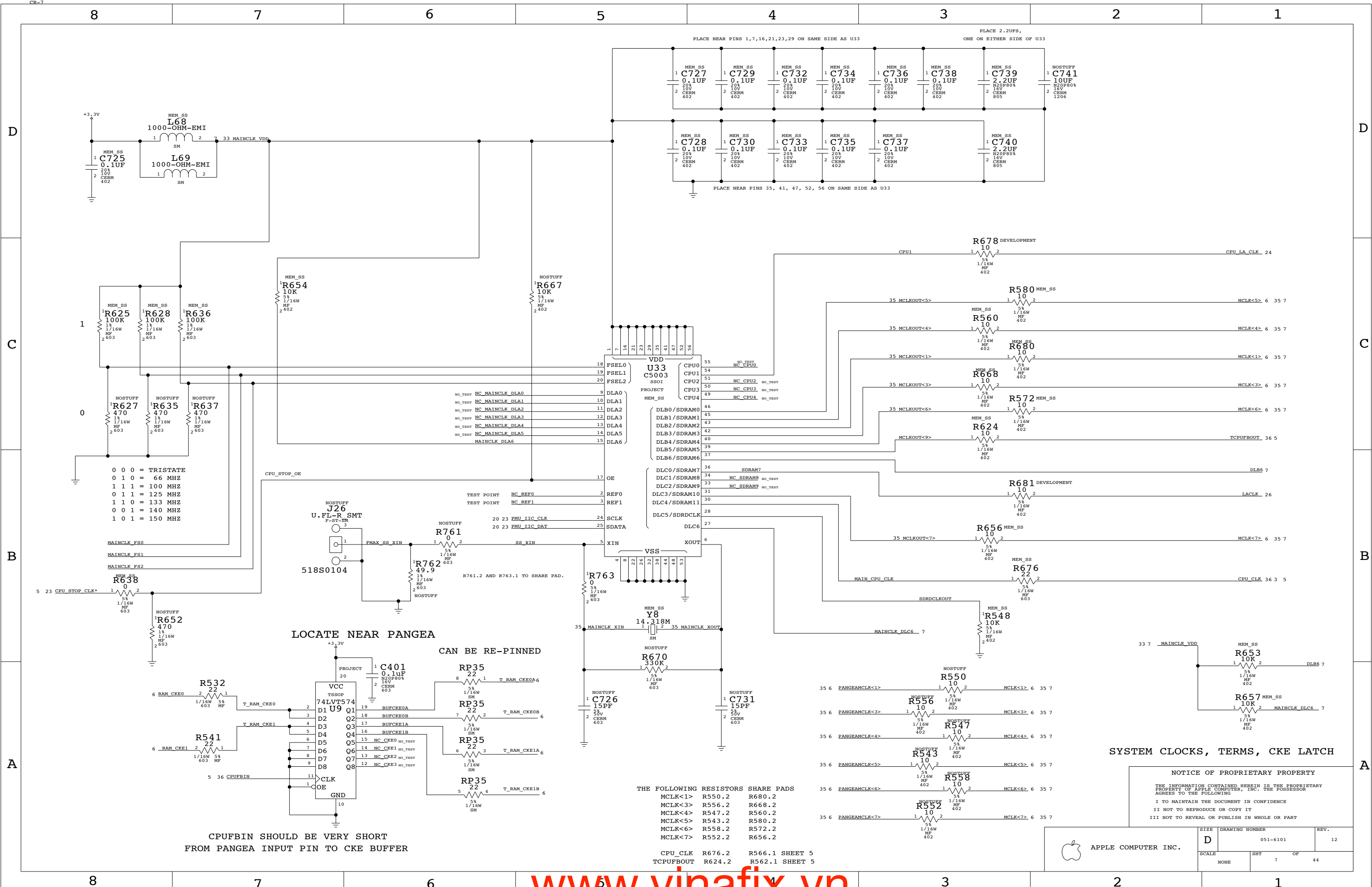
CS0-3 ARE CRITICAL TIMING NETS  
MAKE AS SHORT AS POSSIBLE  
SPLIT NETS AT BGA, 10-OHM  
SERIES TERM.

Pangea SDRAM IF & SDRAM DIMMS

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SCALE	SHT	OF
NONE	6	44



THE FOLLOWING RESISTORS SHARE PADS

MCLK<1>	R550.2	R680.2
MCLK<3>	R556.2	R668.2
MCLK<4>	R547.2	R560.2
MCLK<5>	R543.2	R580.2
MCLK<6>	R558.2	R572.2
MCLK<7>	R552.2	R656.2

CPU_CLK	R676.2	R566.1	SHEET 5
TCPUFBOUT	R624.2	R562.1	SHEET 5

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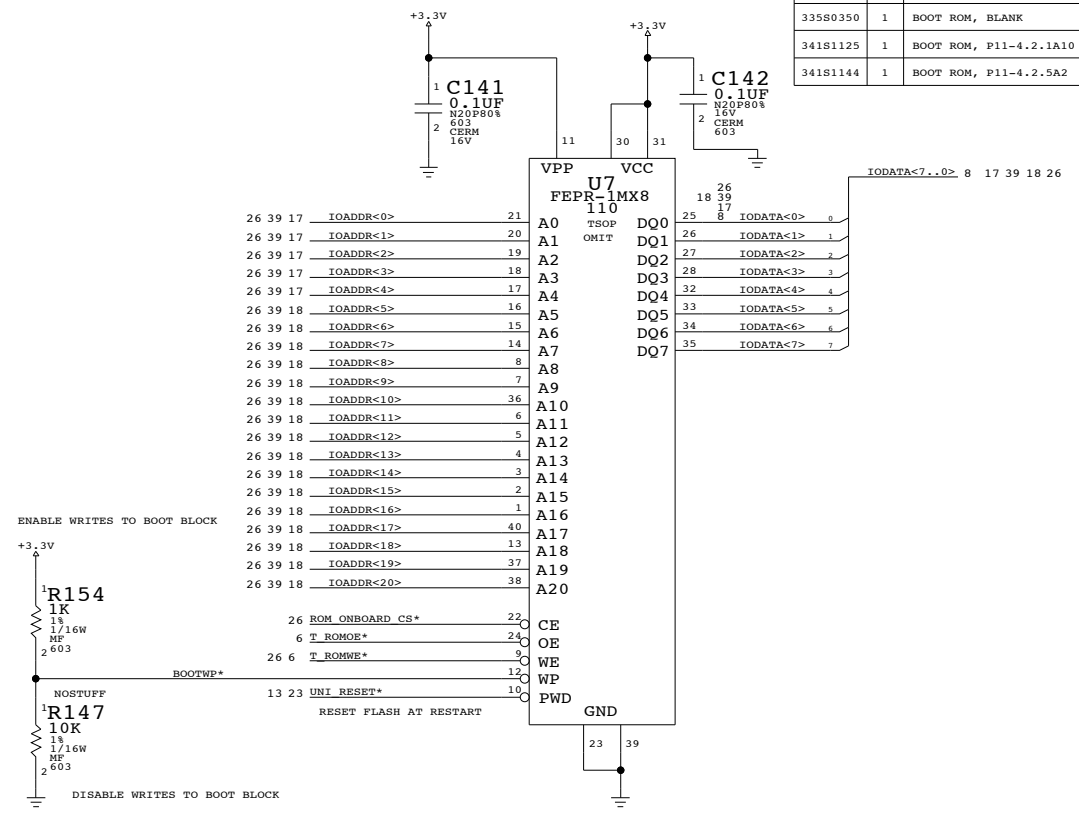
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

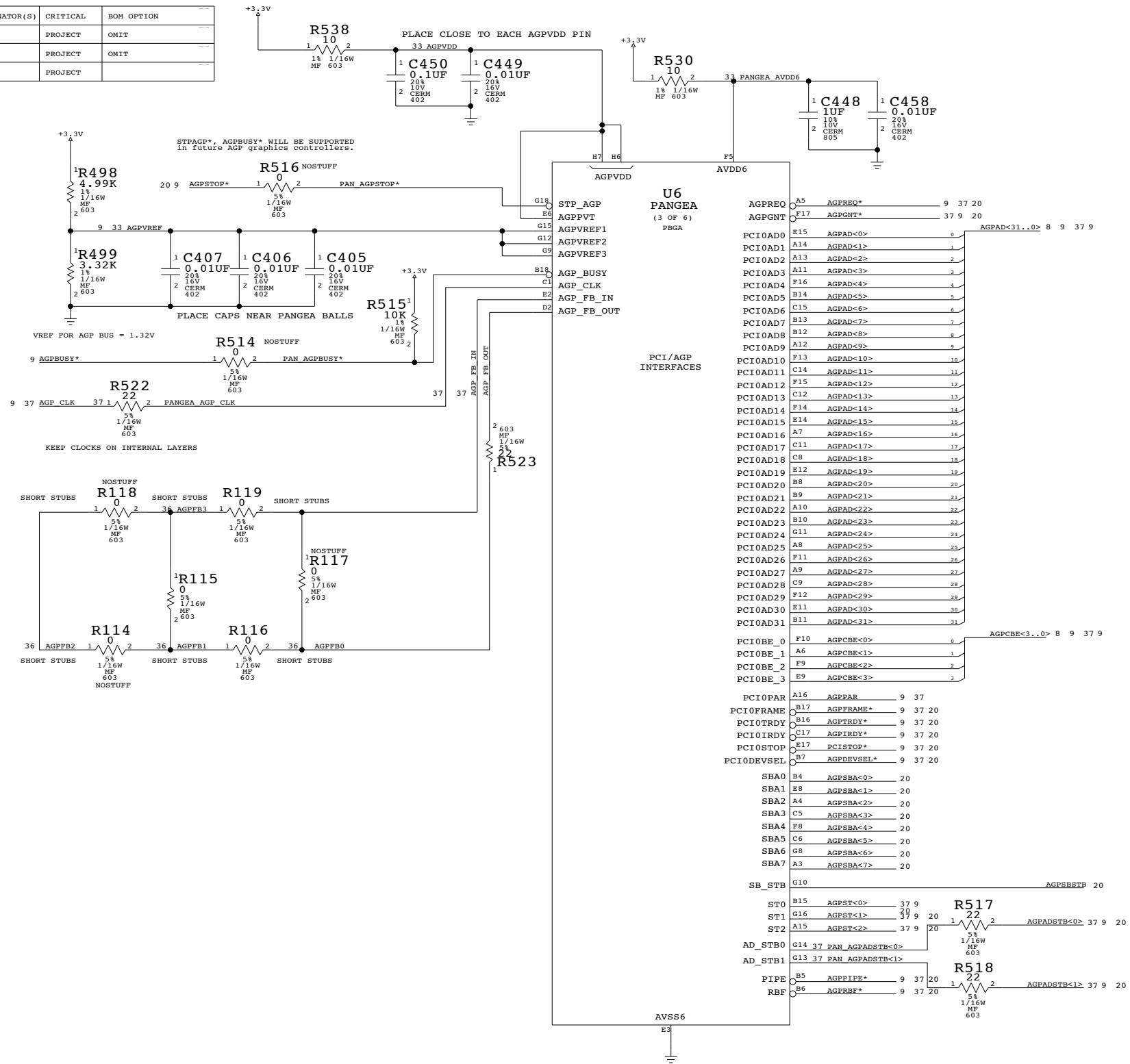
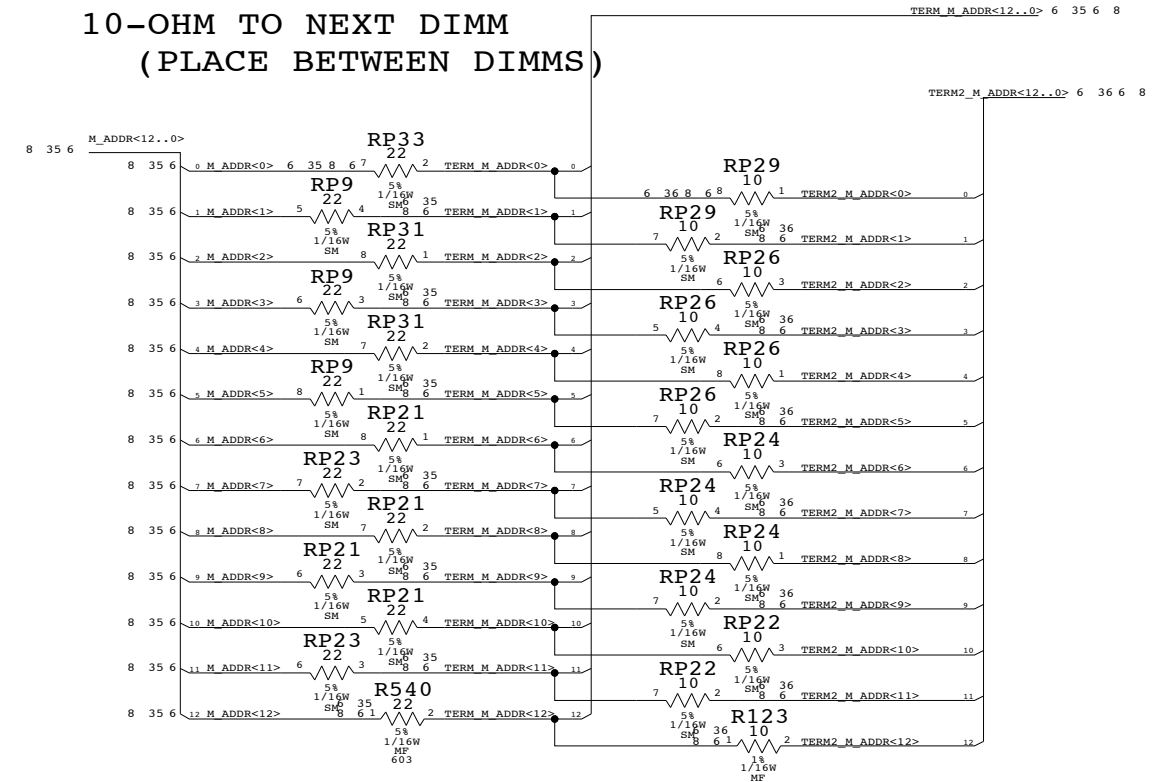
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6101	12
SCALE	SHT	OF	
NONE	7	44	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0350	1	BOOT ROM, BLANK	U7	PROJECT	OMIT
341S1125	1	BOOT ROM, P11-4.2.1A10	U7	PROJECT	OMIT
341S1144	1	BOOT ROM, P11-4.2.5A2	U7	PROJECT	OMIT

**FLASH ROM**



**TERMINATIONS:**  
 22-OHM TO FIRST DIMM  
 (PLACE NEAR FIRST DIMM)  
 10-OHM TO NEXT DIMM  
 (PLACE BETWEEN DIMMS)



**Pangea AGP IF, System ROM**

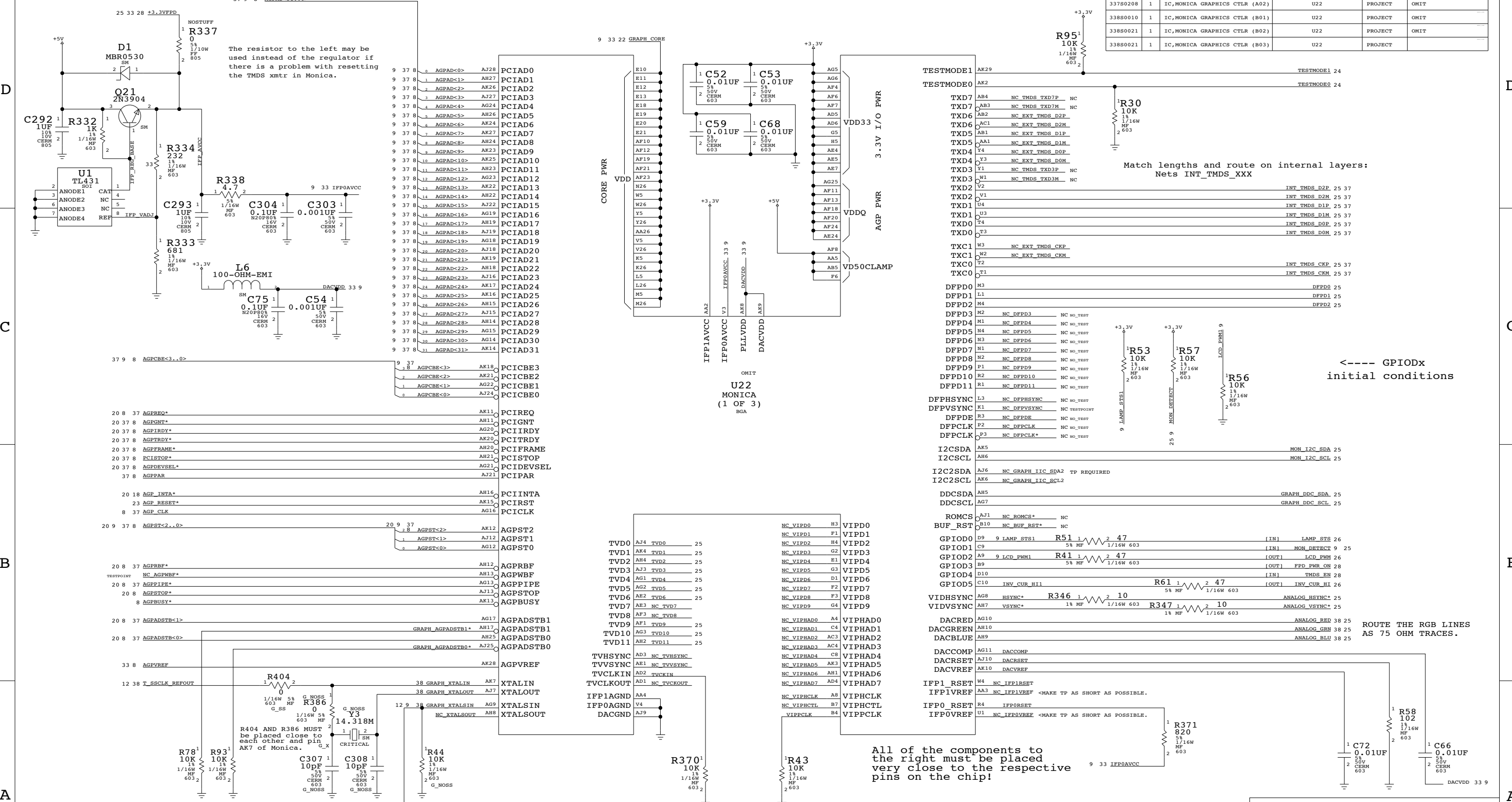
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	D	051-6101	12
SCALE	NONE	SHT	OF
		8	44



# GRAPHICS CONTROLLER - AGP AND VIDEO INTERFACES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33780208	1	IC, MONICA GRAPHICS CTLR (A02)	U22	PROJECT	OMIT
33880010	1	IC, MONICA GRAPHICS CTLR (B01)	U22	PROJECT	OMIT
33880021	1	IC, MONICA GRAPHICS CTLR (B02)	U22	PROJECT	OMIT
33880021	1	IC, MONICA GRAPHICS CTLR (B03)	U22	PROJECT	OMIT



The resistor to the left may be used instead of the regulator if there is a problem with resetting the TMDS xmtr in Monica.

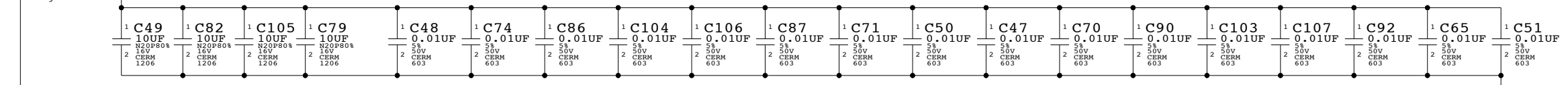
Match lengths and route on internal layers:  
Nets INT\_TMDS\_XXX

----- GPIODx  
initial conditions

ROUTE THE RGB LINES  
AS 75 OHM TRACES.

All of the components to the right must be placed very close to the respective pins on the chip!

## GRAPHICS CORE BYPASS (VDD)



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SIZE	DRAWING NUMBER	REV.
D	051-6101	12
SCALE	SHT	OF
NONE	9	44

# GRAPHICS CONTROLLER - MEMORY INTERFACE

8 7 6 5 4 3 2 1

D

D

C

C

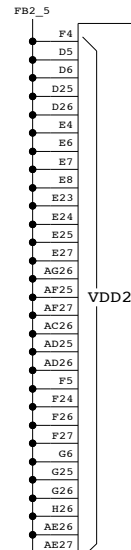
B

B

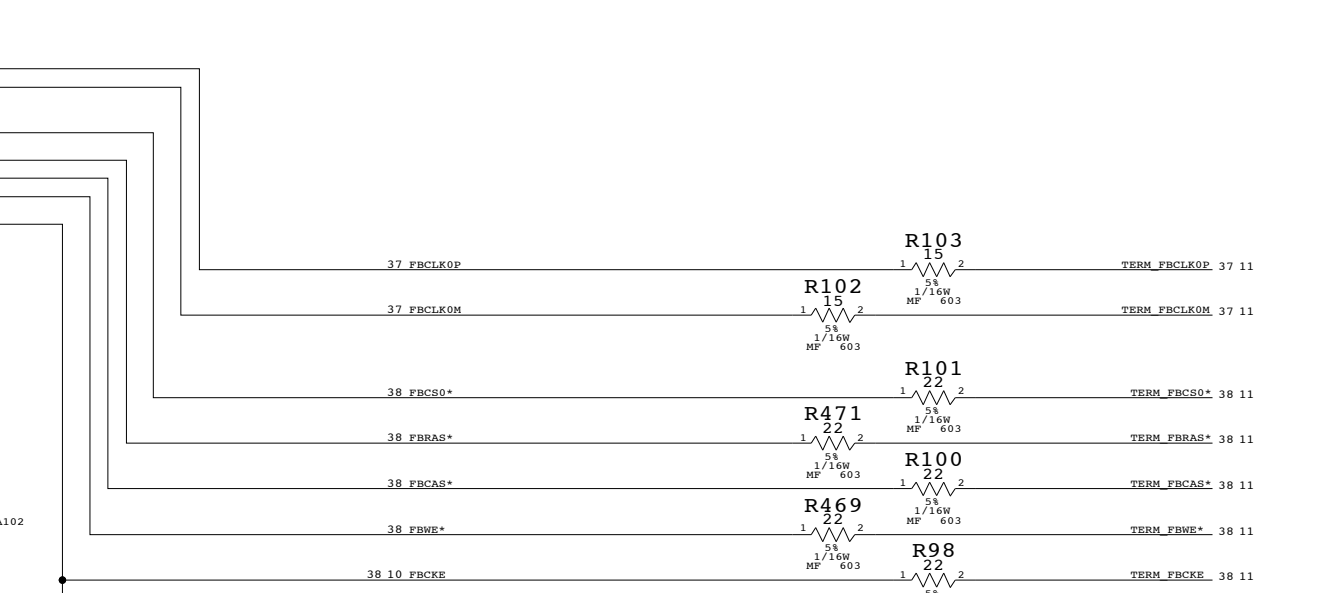
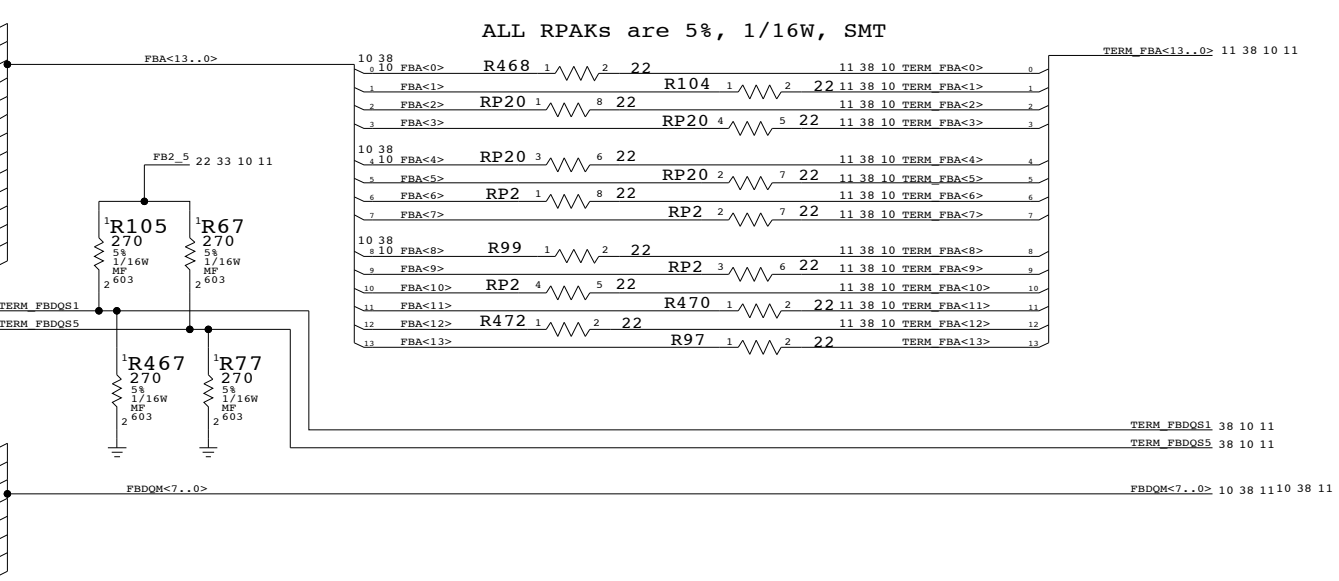
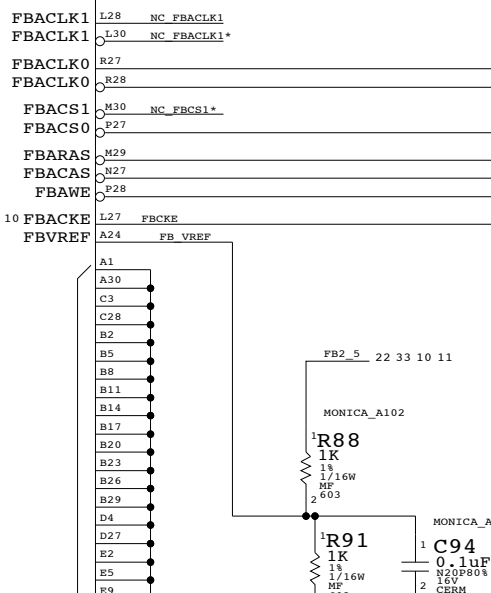
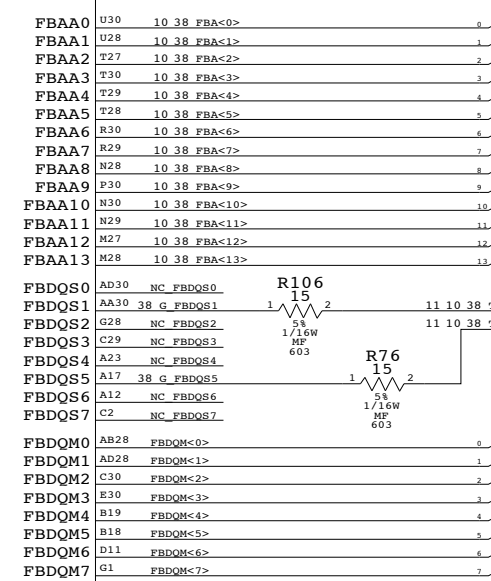
A

A

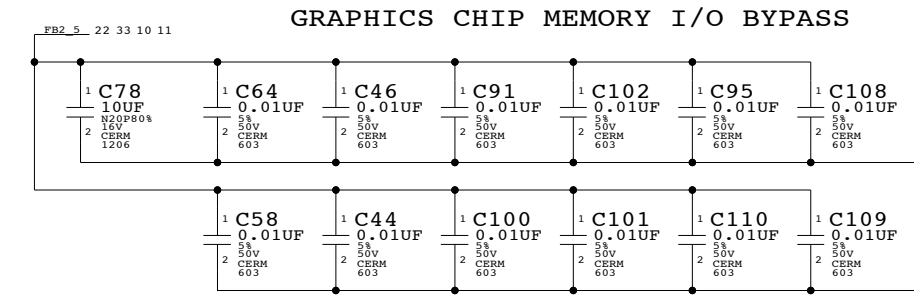
11 38 11 10 FBDC63..0>



VDD25  
ADD TP TO B30  
TO COVER UP  
PINOUT MISTAKES?



Route the following nets on internal layers:  
 TERM\_FBCLK0\* (ROUTE AS DIFFERENTIAL PAIRS)  
 TERM\_FBCS0\*      TERM\_FBWE\*  
 TERM\_FBRAS\*      TERM\_FBCKE  
 TERM\_FBCAS\*



DISTRIBUTE THESE CAPS AMONG THE VDD25 PINS ON THE GRAPHICS CHIP

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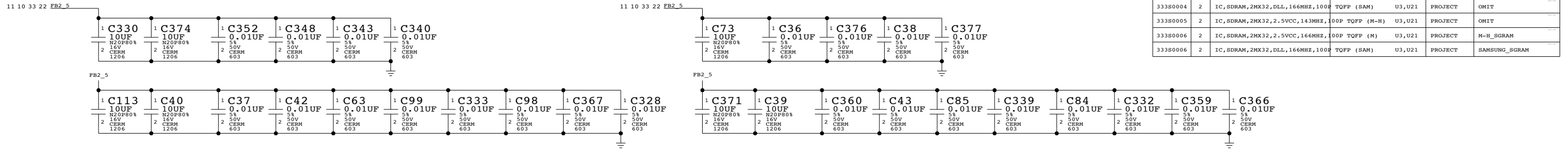
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
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SCALE	NONE	SHT	OF
		10	44

8 7 6 5 4 3 2 1

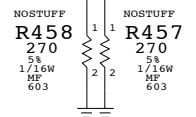
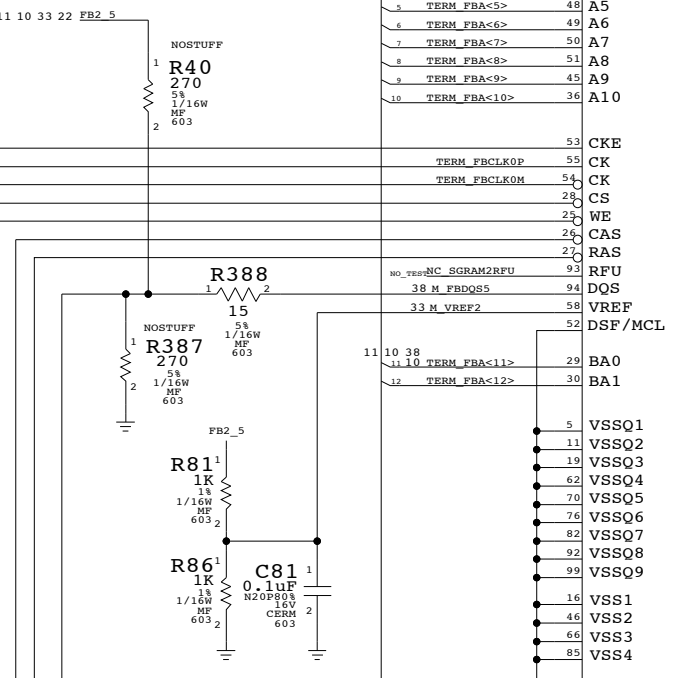
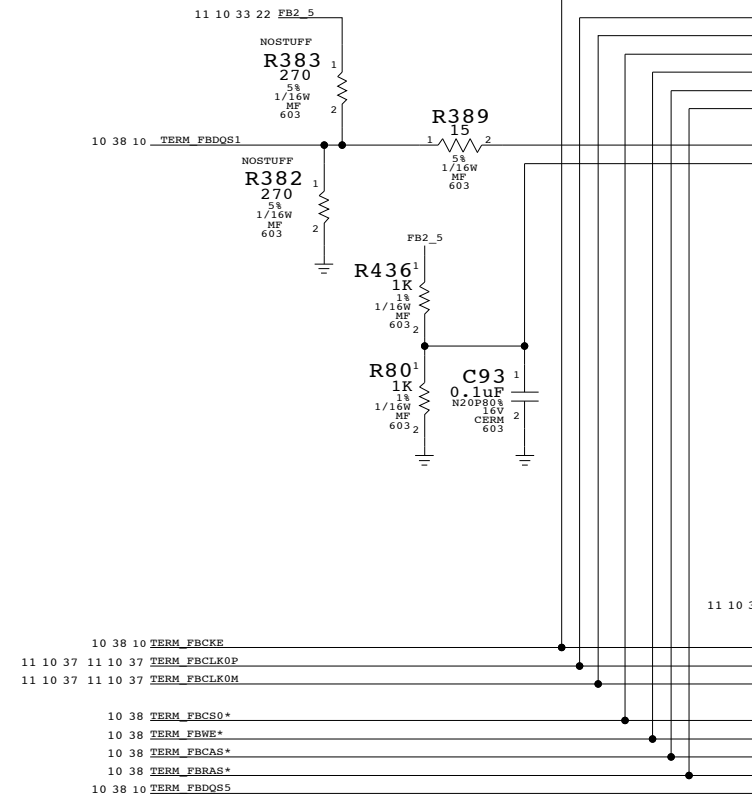
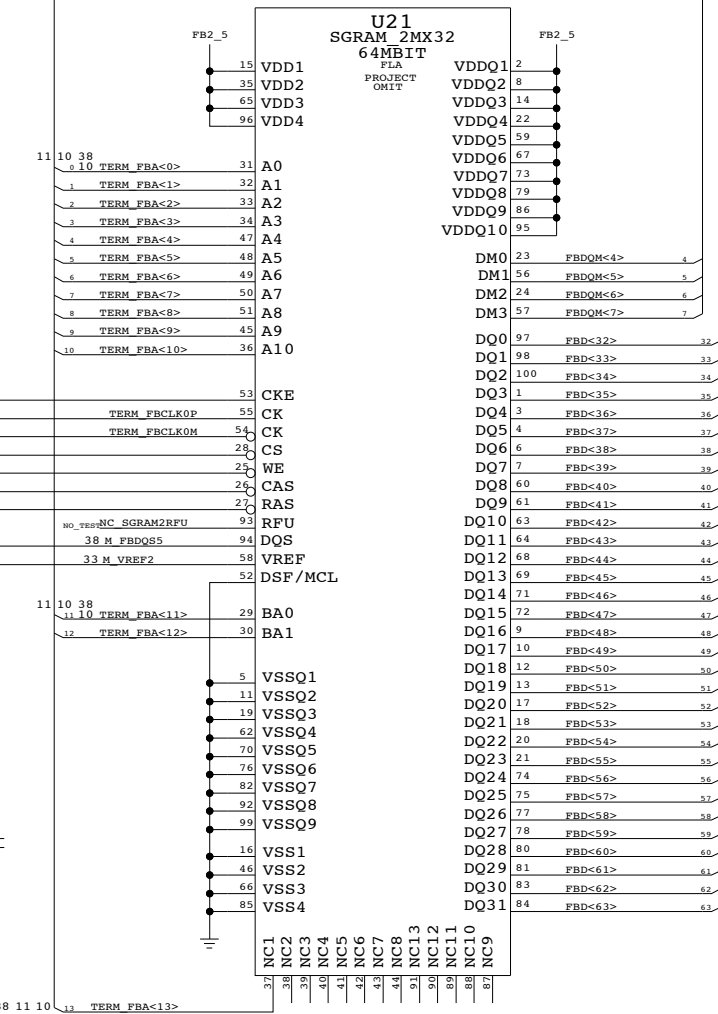
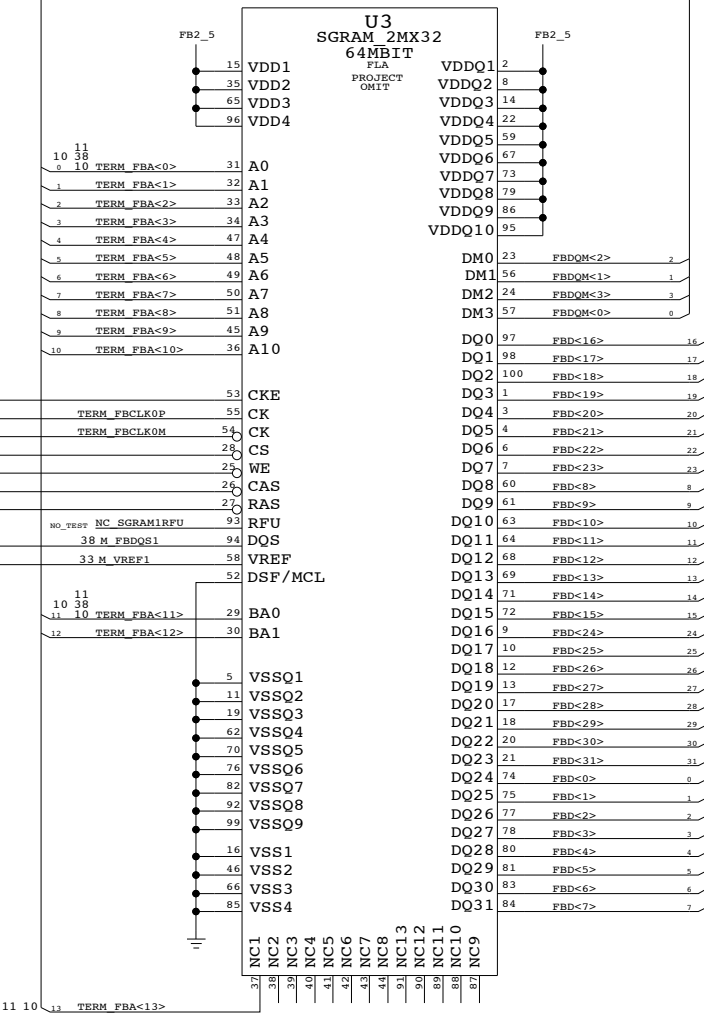
# GRAPHICS SDRAMS - 16/32 MB

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
33380055	33380006	SAMSUNG_SGRAM	U3,U21	2MX32,2.5VCC,183MHZ

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33380075	2	IC, SGRAM, DDR, 2MX32, 125MHZ, 100P	TQFP, NO DLL U3,U21	PROJECT	OMIT
33380076	2	IC, SGRAM, DDR, 2MX32, 143MHZ, 100P	TQFP, NO DLL U3,U21	PROJECT	OMIT
33380077	2	IC, SGRAM, DDR, 2MX32, 166MHZ, 100P	TQFP, NO DLL U3,U21	PROJECT	OMIT
33380003	2	IC, SDRAM, 2MX32, DLL, 143MHZ, 100P	TQFP (SAM) U3,U21	PROJECT	OMIT
33380004	2	IC, SDRAM, 2MX32, DLL, 166MHZ, 100P	TQFP (SAM) U3,U21	PROJECT	OMIT
33380005	2	IC, SDRAM, 2MX32, 2.5VCC, 143MHZ, 100P	TQFP (M-H) U3,U21	PROJECT	OMIT
33380006	2	IC, SDRAM, 2MX32, 2.5VCC, 166MHZ, 100P	TQFP (M) U3,U21	PROJECT	M-H_SGRAM
33380006	2	IC, SDRAM, 2MX32, DLL, 166MHZ, 100P	TQFP (SAM) U3,U21	PROJECT	SAMSUNG_SGRAM



10 38 11 10 FBDQ<63..0>  
 11 38 10 FBDQ<7..0>  
 11 10 38 11 10 TERM FBA<13..0>



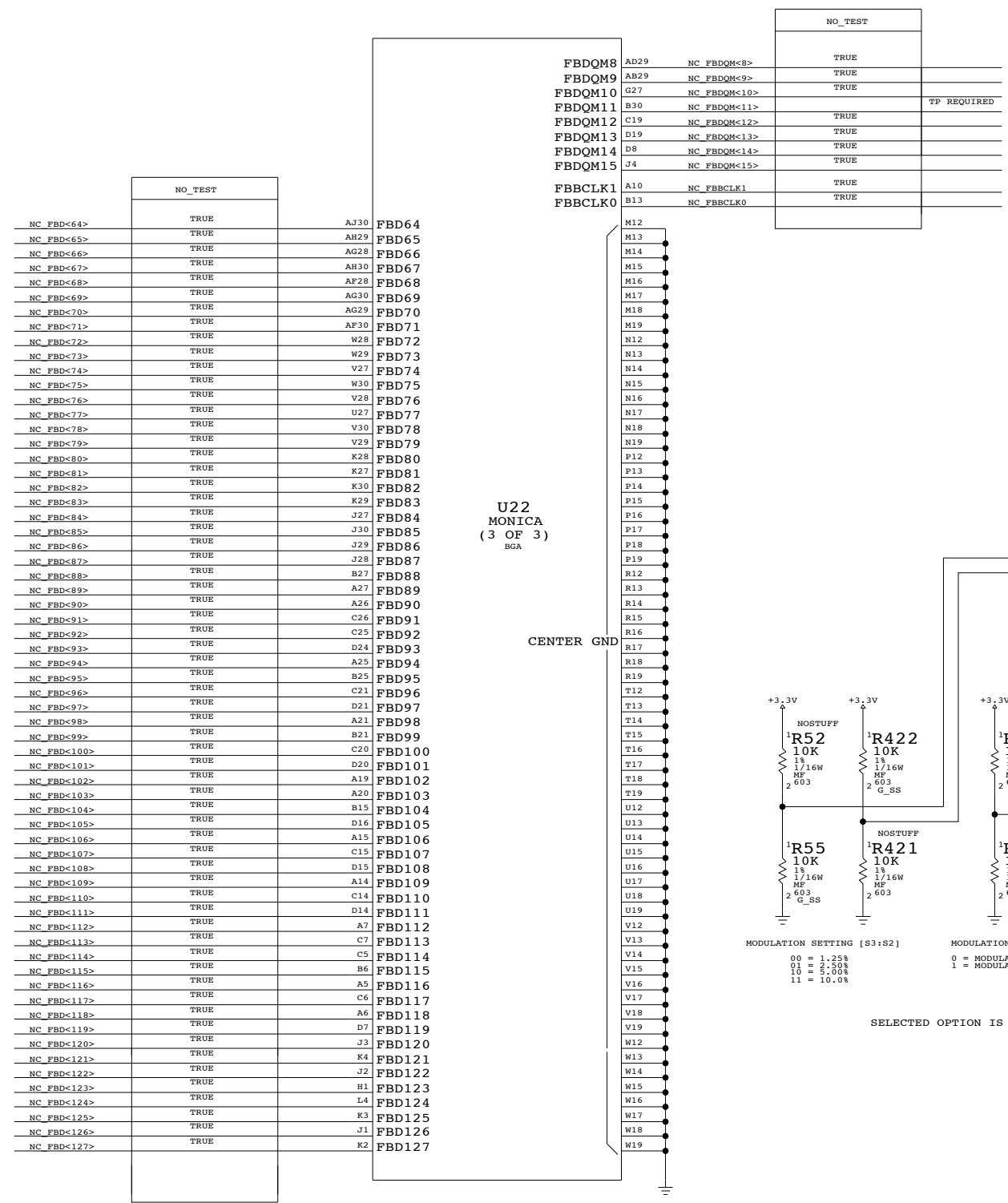
10 38 10 TERM FBCKE  
 11 10 37 11 10 37 TERM FBCLKOP  
 11 10 37 11 10 37 TERM FBCLKOM

10 38 TERM FBCKE\*  
 10 38 TERM FBWE\*  
 10 38 TERM FBCKAS\*  
 10 38 TERM FBCKAS\*  
 10 38 10 TERM FBDQS5

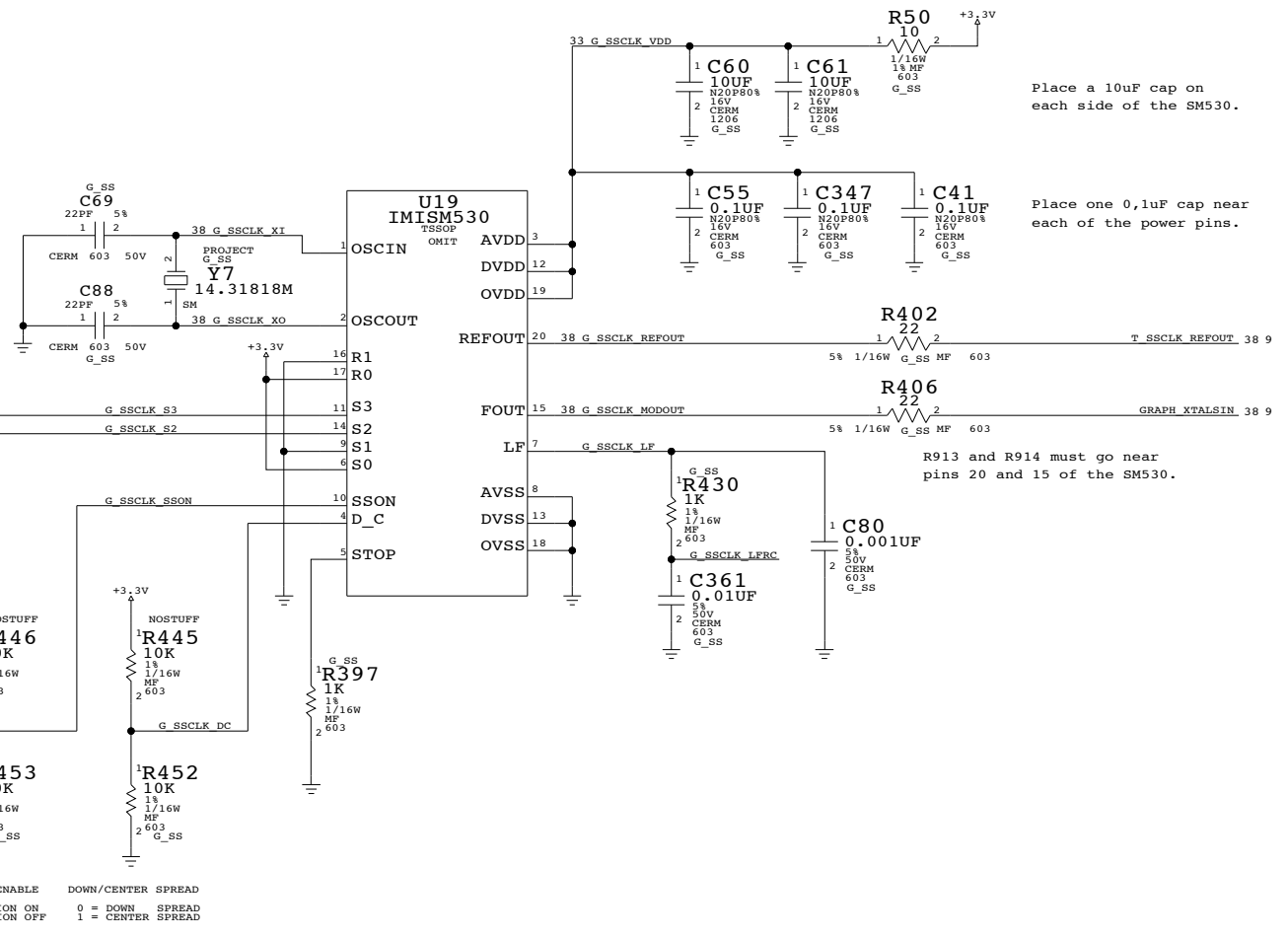
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	NONE	D 051-6101	12
SCALE		SHT	OF
NONE		11	44

# GRAPHICS CHIP - UPPER 64-BIT DATA BUS & SUPPORT AND CENTER GROUND BALLS



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
35980055	1	IC, SM530, SPREAD SPECTR CLK GEN, 20P TSSOP	U19	PROJECT	G_SS



Place a 10uF cap on each side of the SM530.

Place one 0.1uF cap near each of the power pins.

R913 and R914 must go near pins 20 and 15 of the SM530.

MODULATION SETTING (S3:S2)      MODULATION ENABLE      DOWN/CENTER SPREAD

00 = 1.25%                              0 = MODULATION ON              0 = DOWN SPREAD

01 = 2.50%                              1 = MODULATION OFF             1 = CENTER SPREAD

10 = 5.00%                                   

11 = 10.0%                                     

SELECTED OPTION IS THIS COLOR!

**NOTICE OF PROPRIETARY PROPERTY**

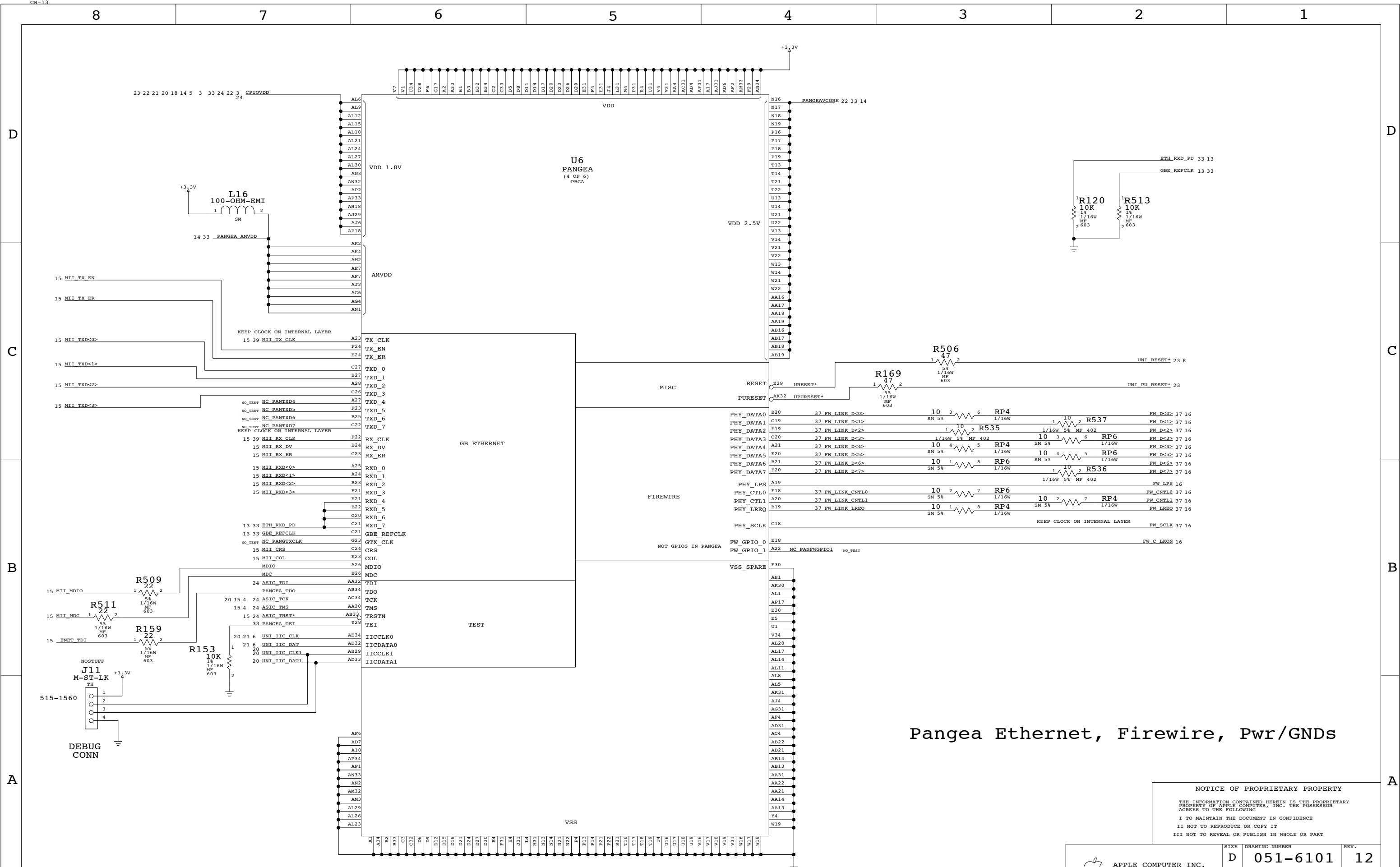
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	D	051-6101	12
SCALE	NONE	SHT OF	12 OF 44



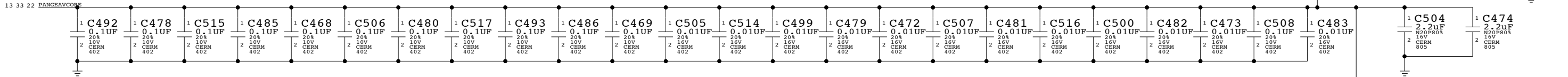
Pangea Ethernet, Firewire, Pwr/GNDs

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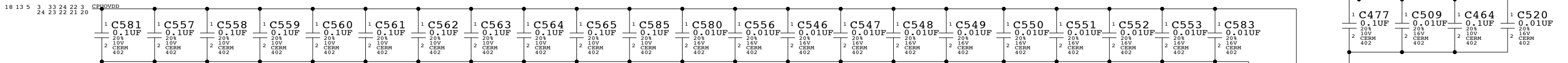
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6101	12
SCALE	NONE	SHT	OF
		13	44

8 7 6 5 4 3 2 1

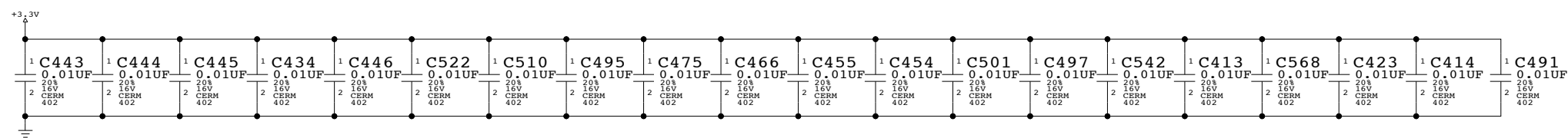
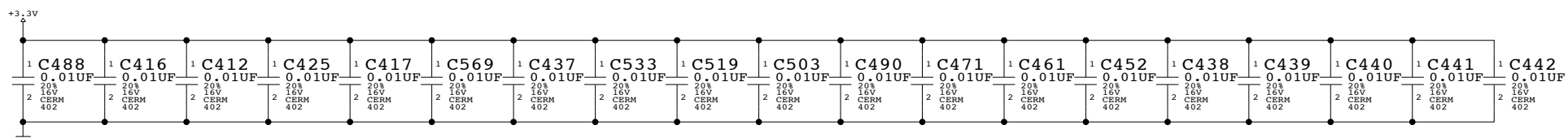
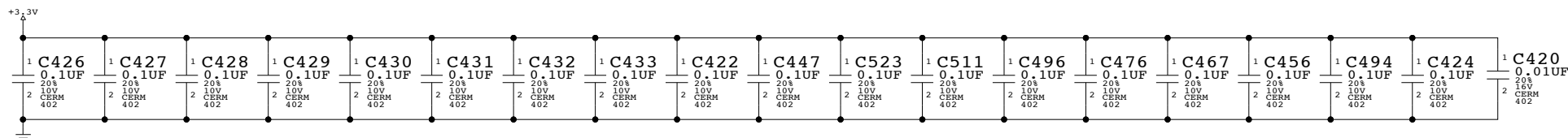
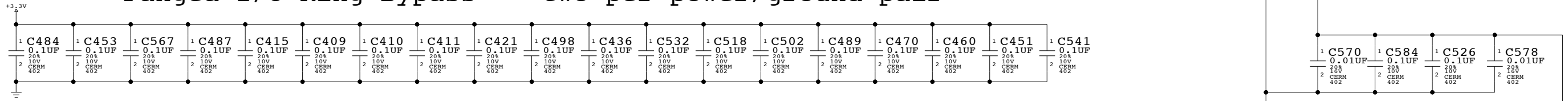
### PANGEA CORE BYPASS



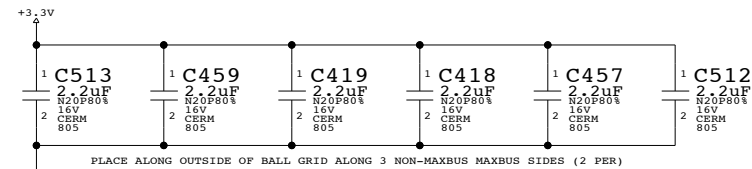
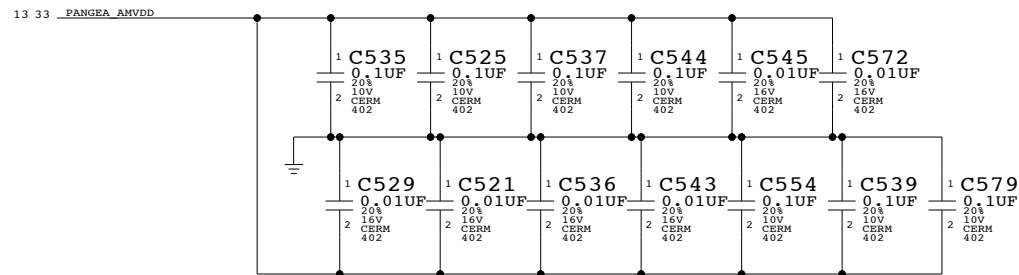
### Pangea Processor I/F Bypass -- two per power/ground pair



### Pangea I/O Ring Bypass -- two per power/ground pair



### Pangea AMVDD Bypass (one pair per pin)



### Pangea Bypass

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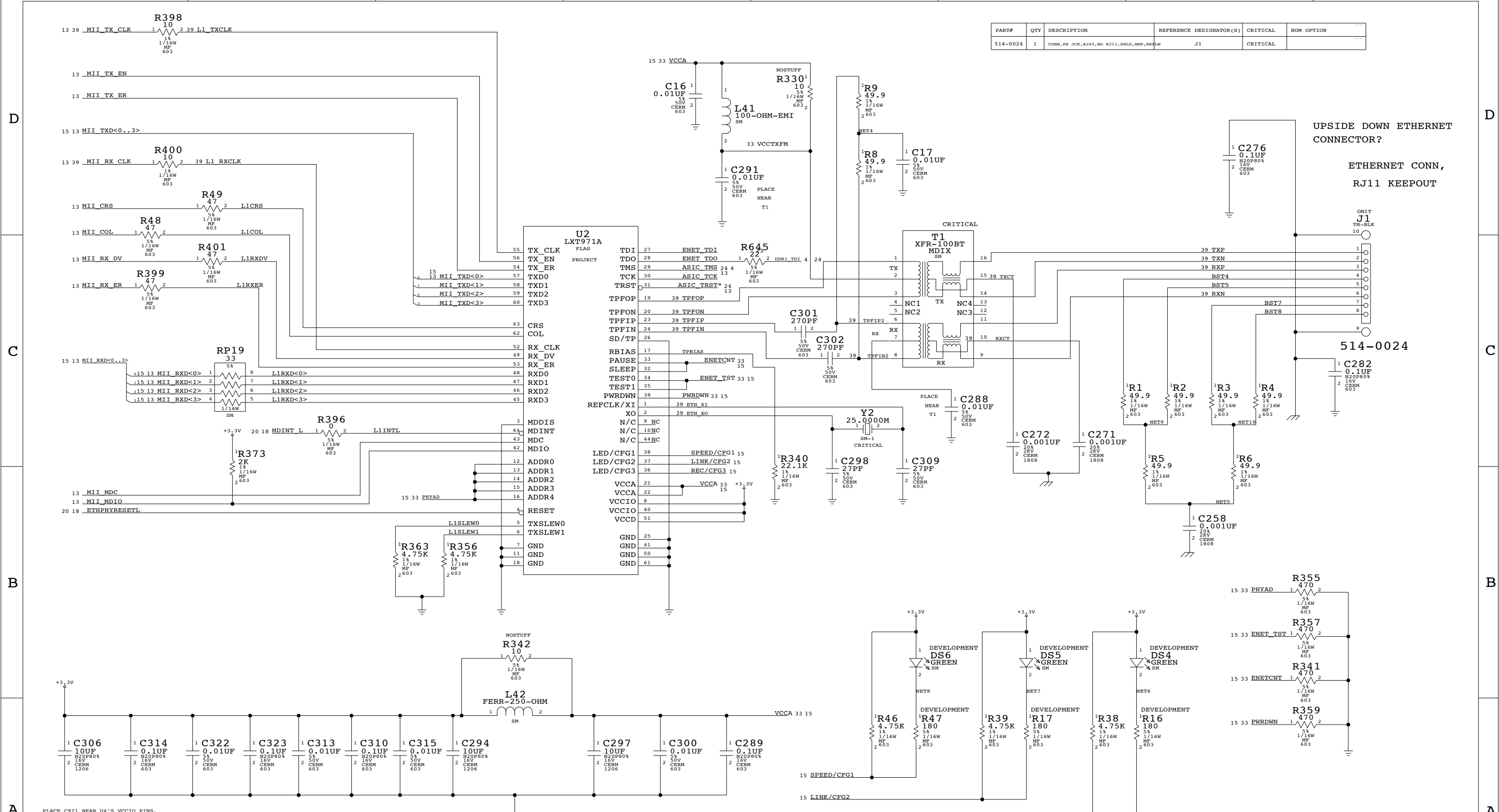
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	D	051-6101	12
SCALE	SHT OF		
NONE	14 OF		44

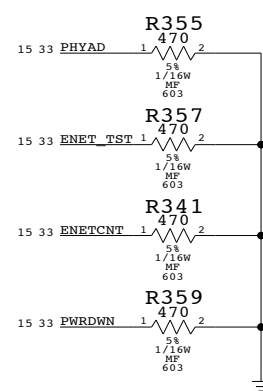
8 7 6 5 4 3 2 1

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0024	1	CONN, PH JCK, R245, NO RJ11, SHLD, NMP, REFLW	J1	CRITICAL	



UPSIDE DOWN ETHERNET CONNECTOR?  
ETHERNET CONN, RJ11 KEEPOUT

514-0024



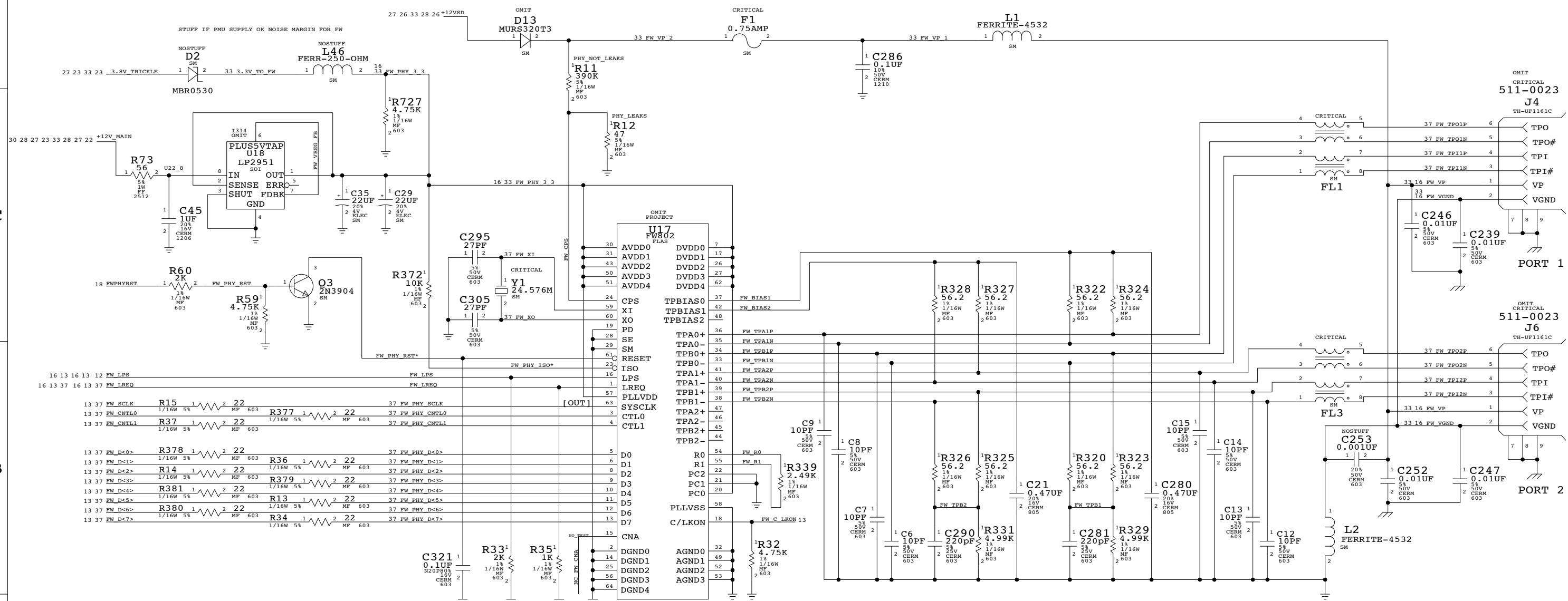
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### ETHERNET PHY

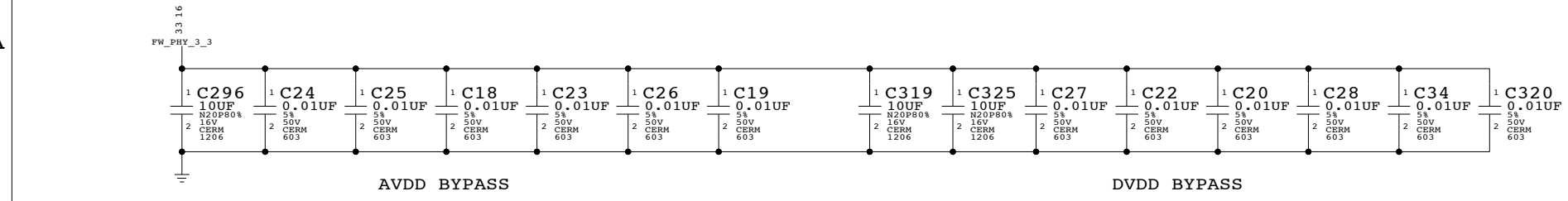
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6101	12
SCALE		SHT	OF
NONE		15	44

# Firewire PHY and Termination

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33880018	1	FLAS-64M431-H63, 2PORT FW PHY, FW802A	REV A U17	PROJECT	OMIT
33780509	1	FLAS-64M431-H63, 2PORT FW PHY, FW802	REV 9 U17	PROJECT	OMIT
37180058	1	DIODE, FAST RECOVERY, 200V, 3A, SMD	D13		
35380094	1	5V FIXED/ADJ VREG, SOI-S	U18	PROJECT	OMIT
35380275	1	3.3V FIXED/ADJ VREG, SOI-S	U18	PROJECT	
514-0023	2	CONN, RCPT, R/A, 1394, NOFLANGES, RMP, 6P	J4, J6	CRITICAL	



## Firewire PHY



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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6101	12
SCALE	SHT	OF	
NONE	16	44	



D

D

C

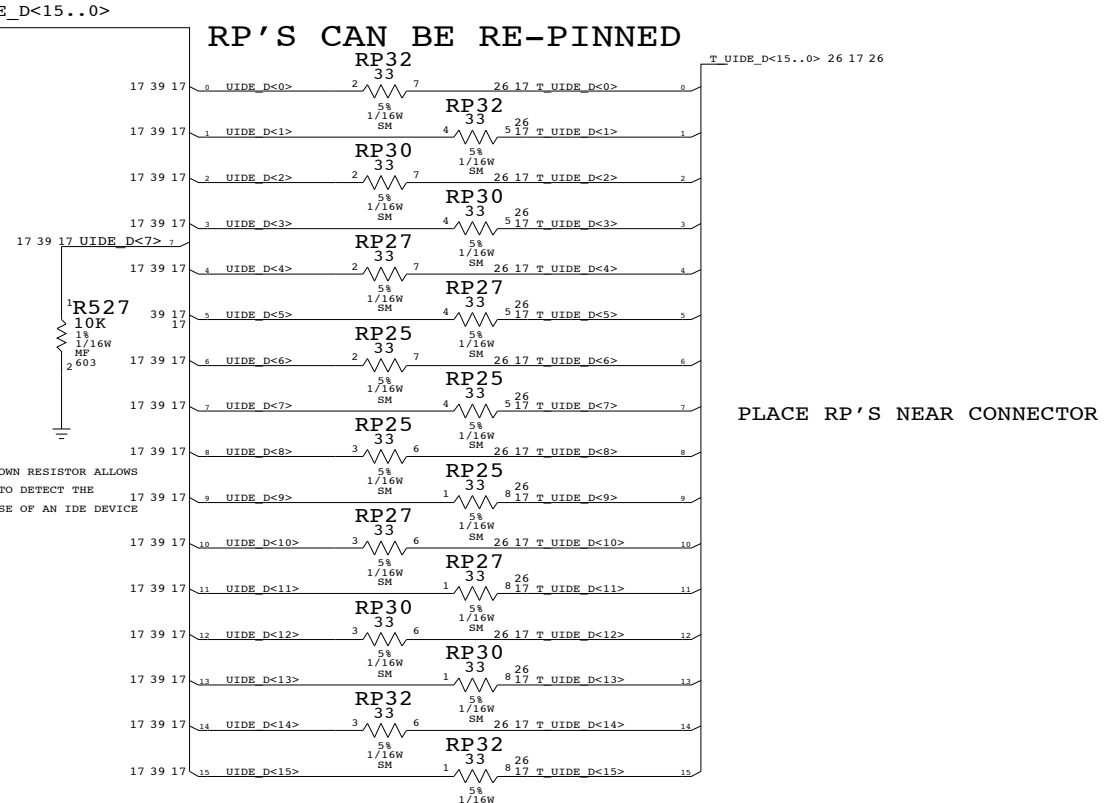
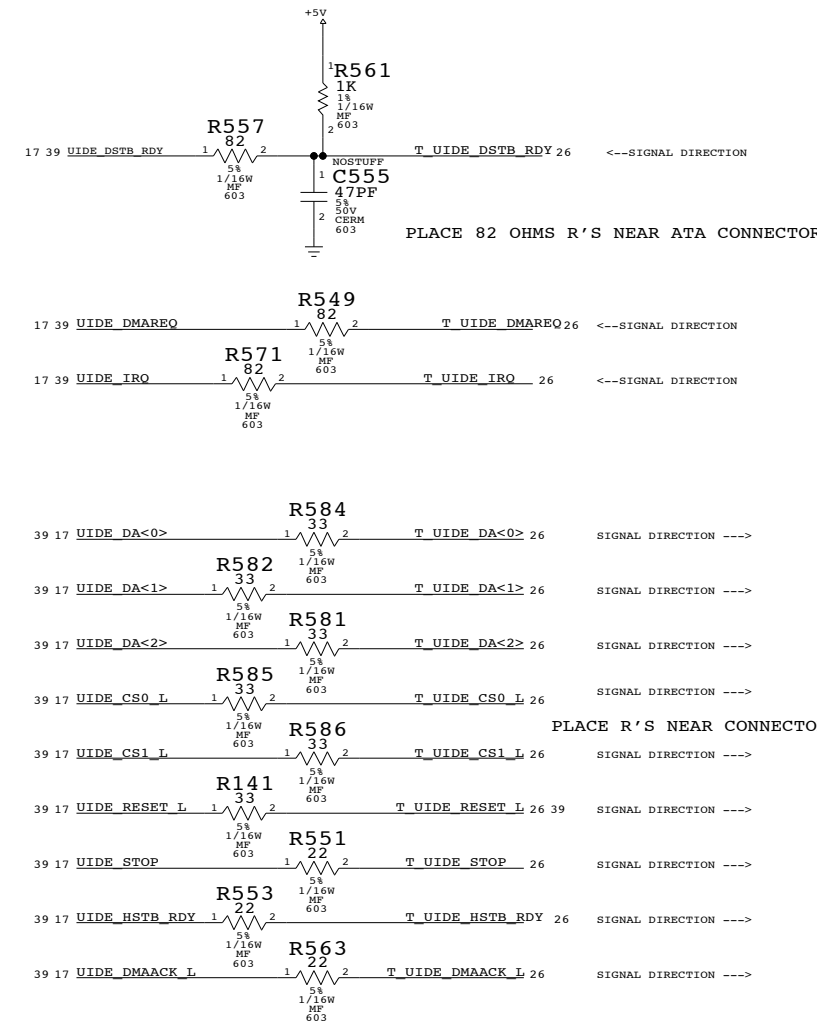
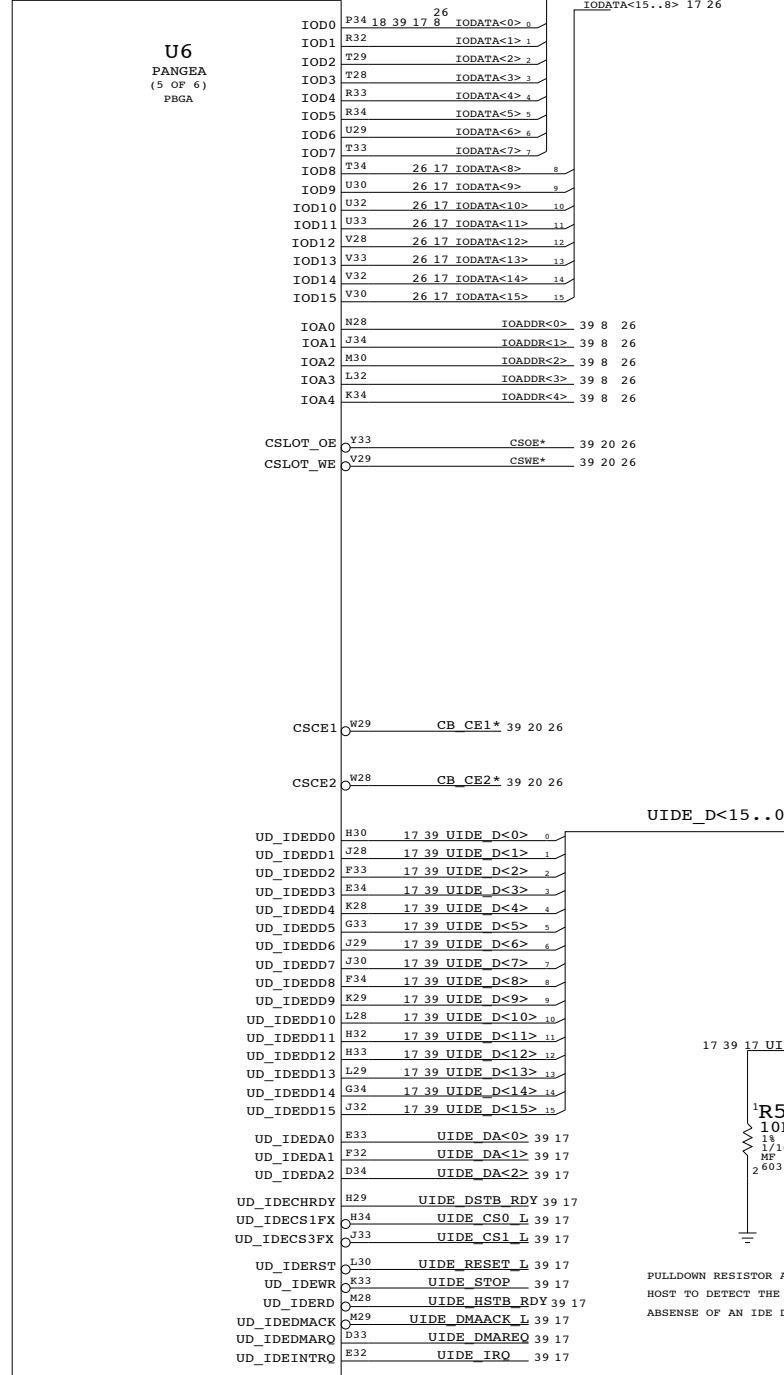
C

B

B

A

A



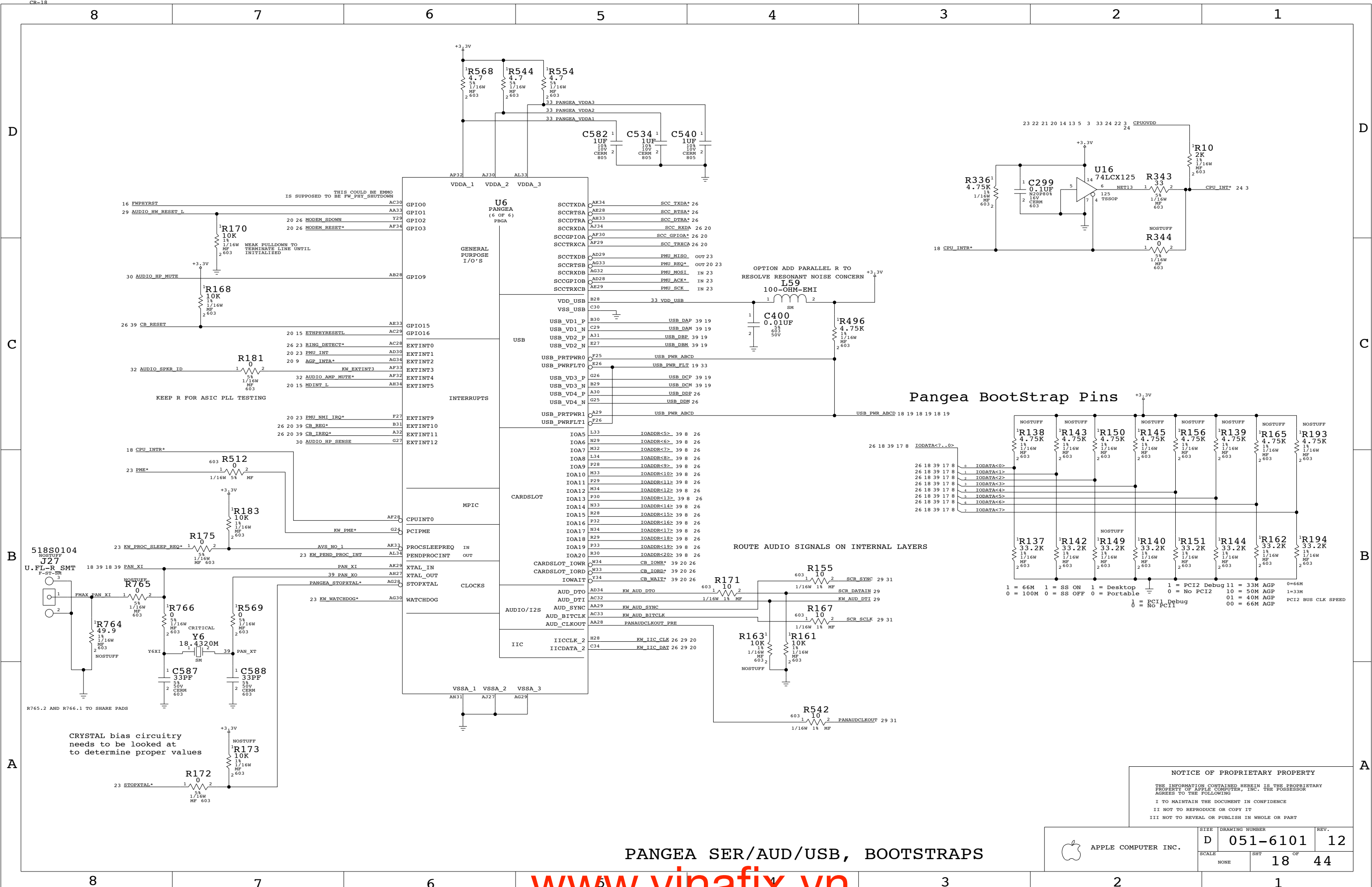
# PANGEA ATA, & PCMCIA BUS

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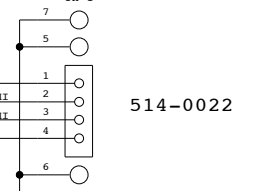
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6101	12
SCALE	NONE	SHT	OF
		17	44



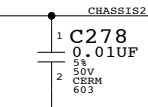
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0022	3	CONN,RCPT,USB,UPRIGHT R/A,NMP	J2,J3,J5	PROJECT	

USB PORT 3

OMIT PROJECT  
J5  
F-RT-89485  
TH-1

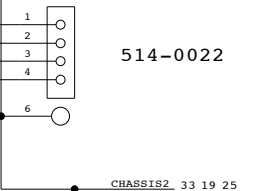


514-0022

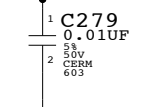


OMIT PROJECT  
J3  
F-RT-89485  
TH-1

USB PORT 1

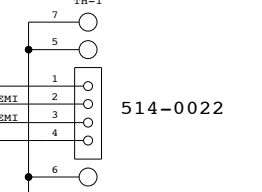


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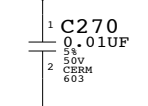


OMIT PROJECT  
J2  
F-RT-89485  
TH-1

USB PORT 2

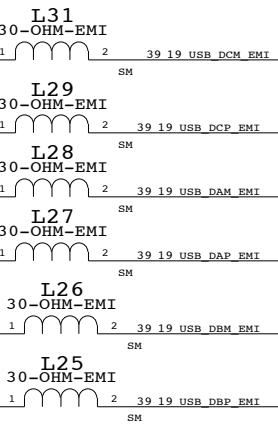
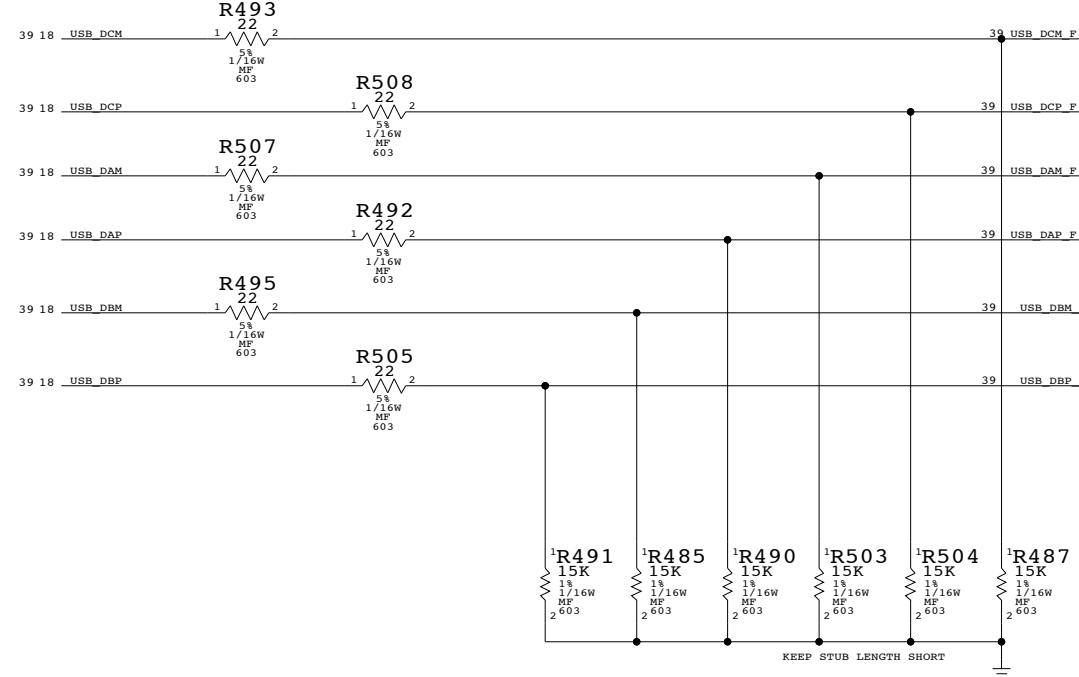


514-0022

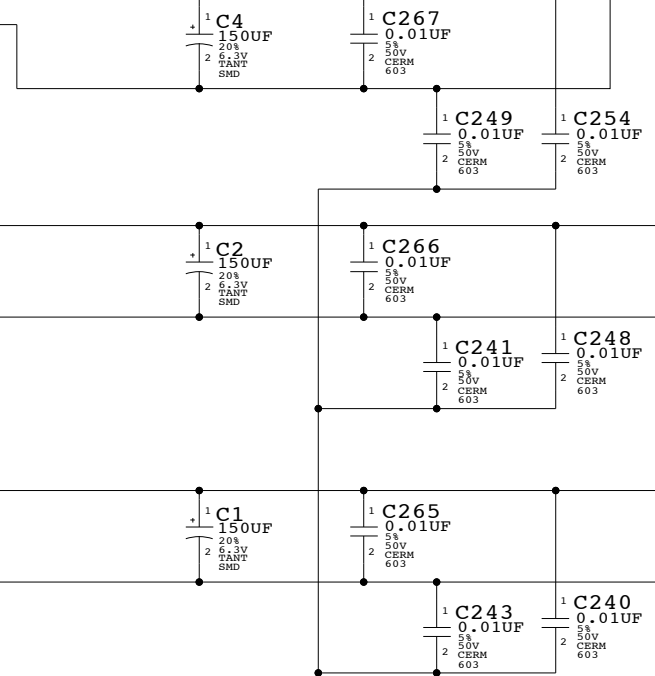
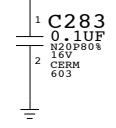
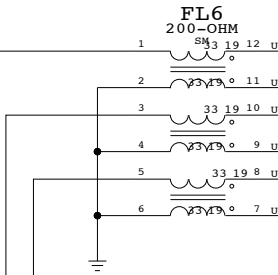
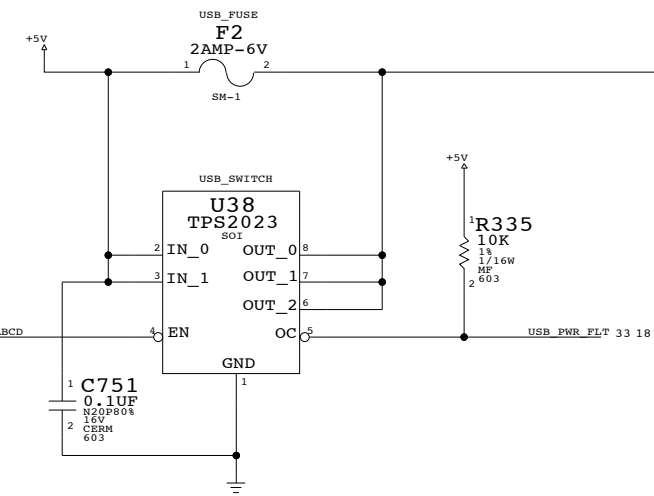


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PLACE NEAR PANGEA



PLACE NEAR CONNECTOR

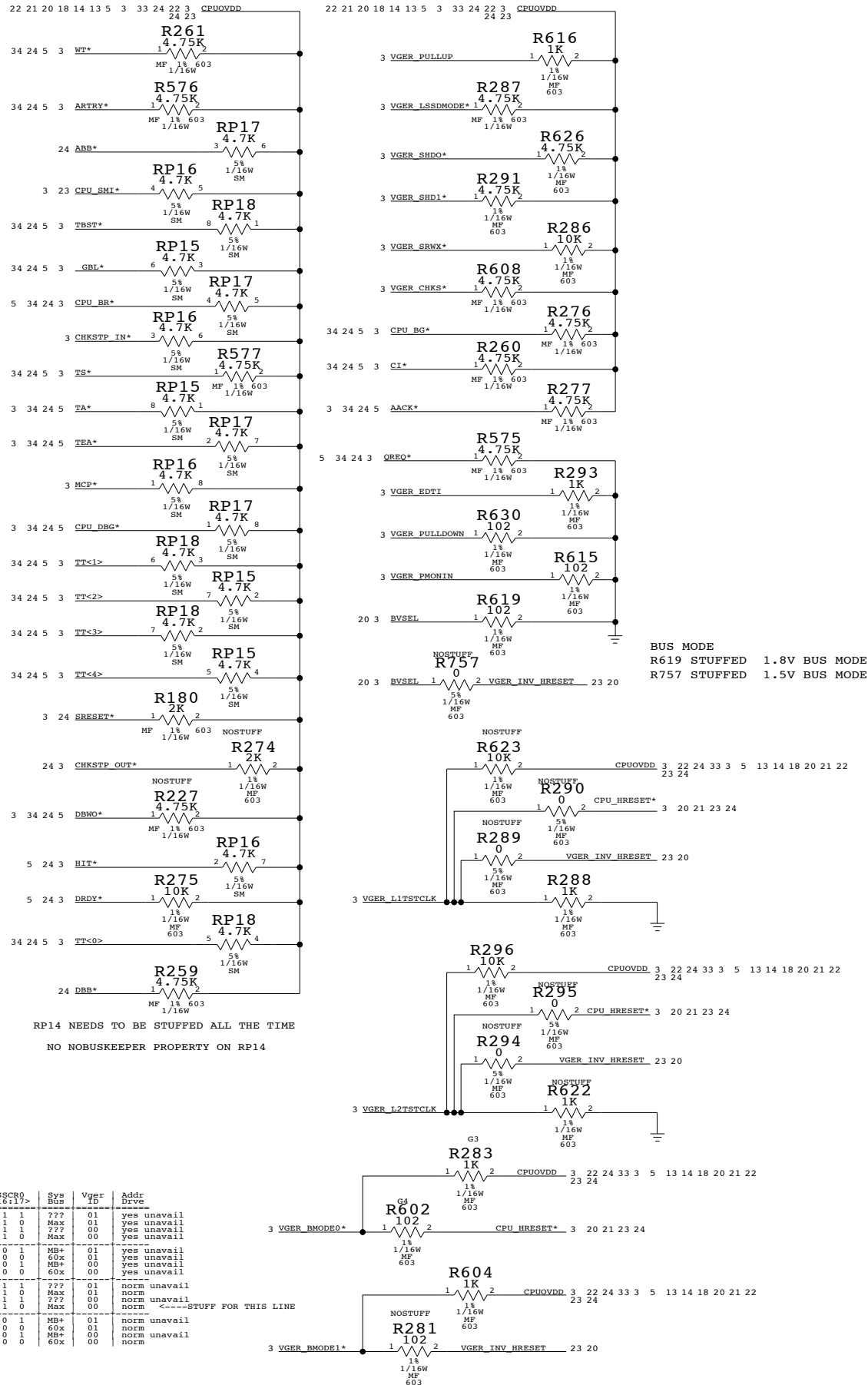


USB CONN & PWR

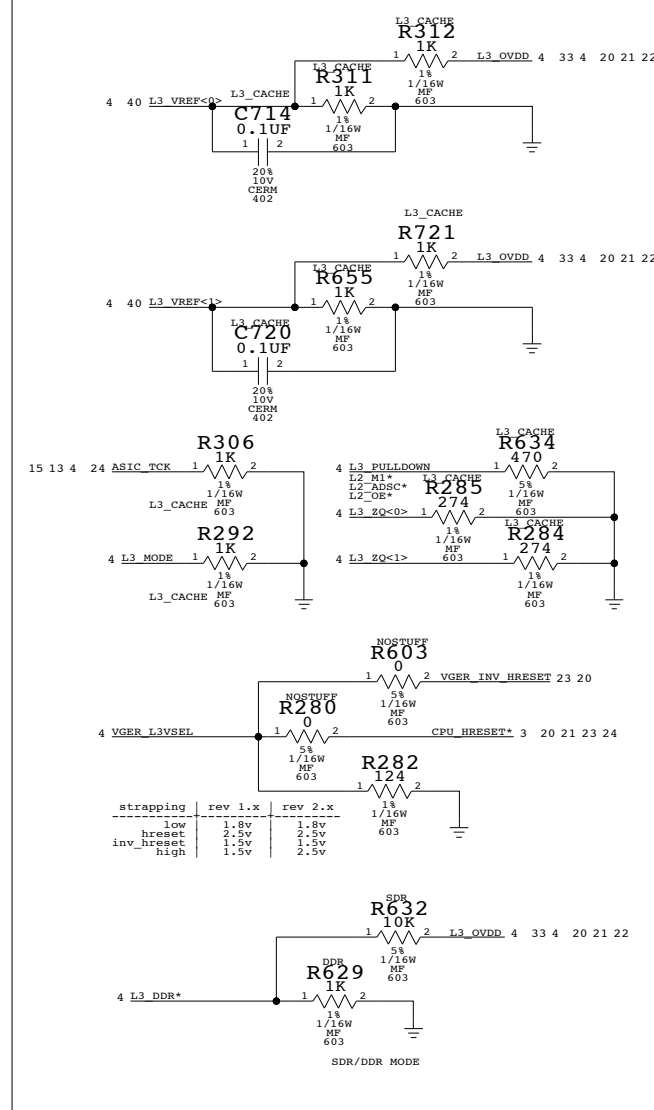
SIZE	DRAWING NUMBER	REV.
D	051-6101	12
SCALE	SHT	OF
NONE	19	44

### PROCESSOR PULLUP/PULLDOWN

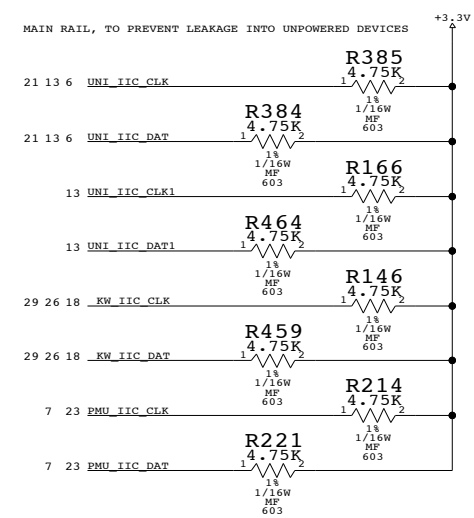
R-PACKS CAN BE RE-PINNED



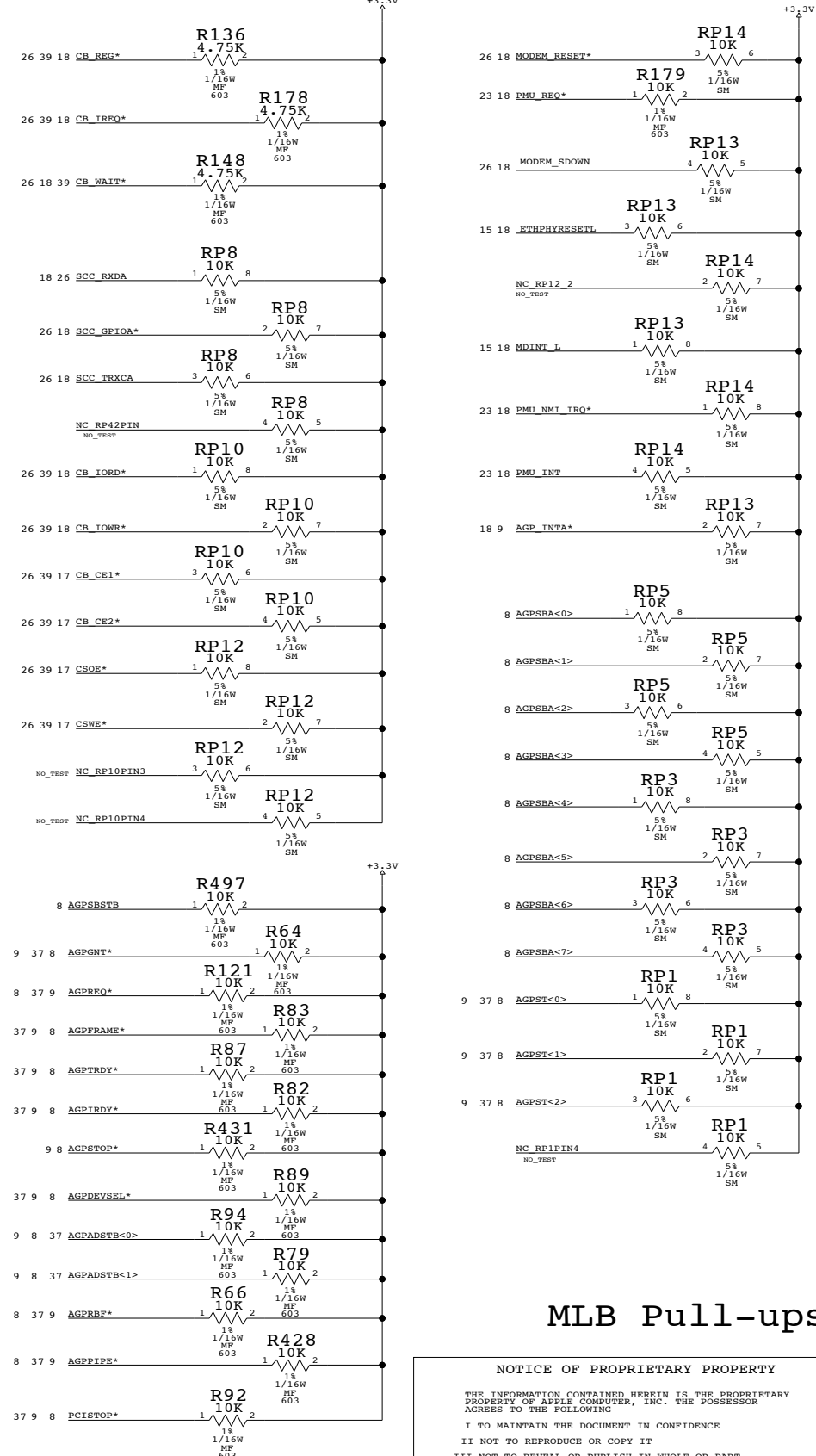
### L3 CACHE PULLUP/PULLDOWN



### IIC BUS PULLUPS



### PANGEA PULLUPS

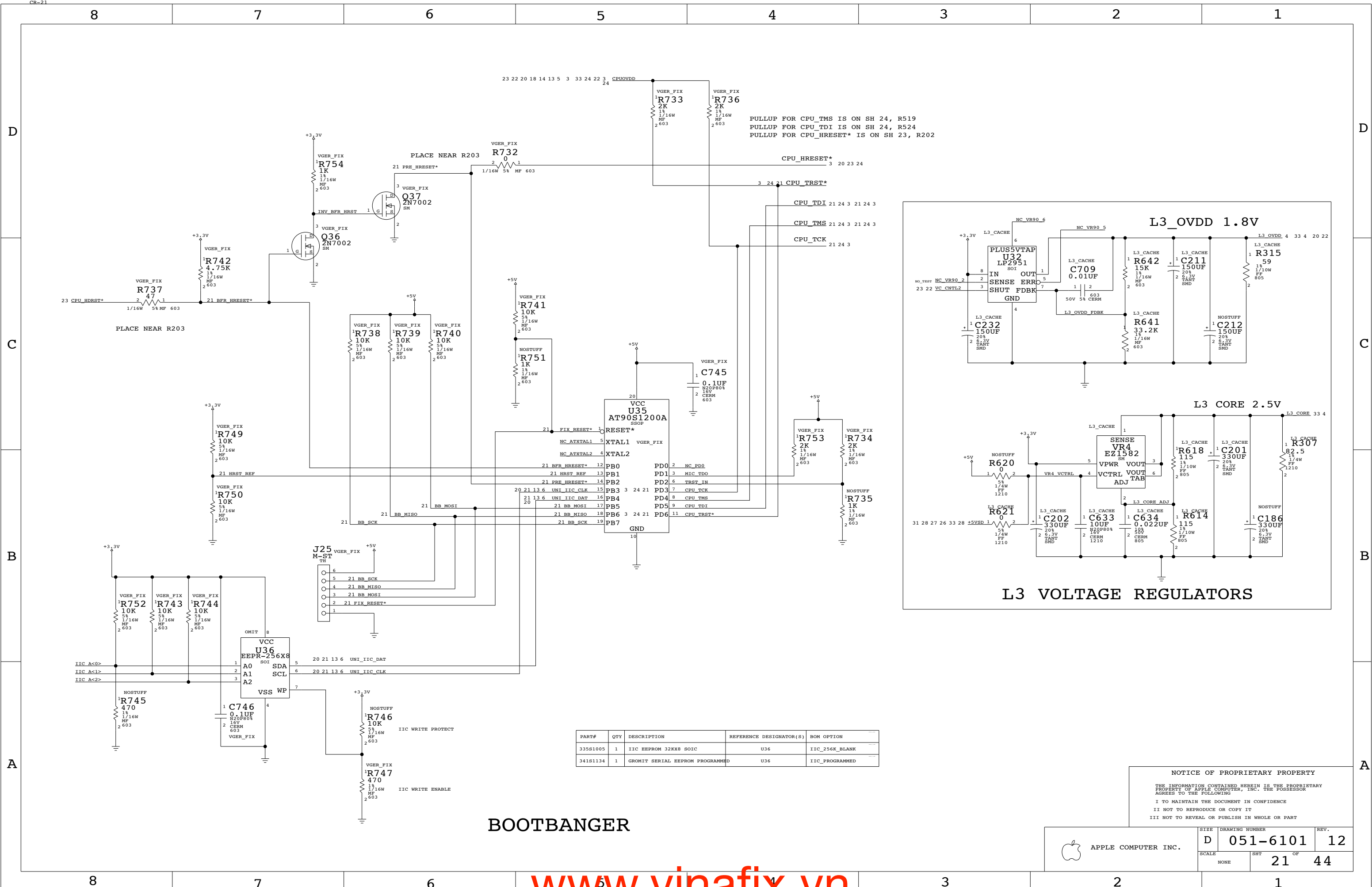


**NOTICE OF PROPRIETARY PROPERTY**

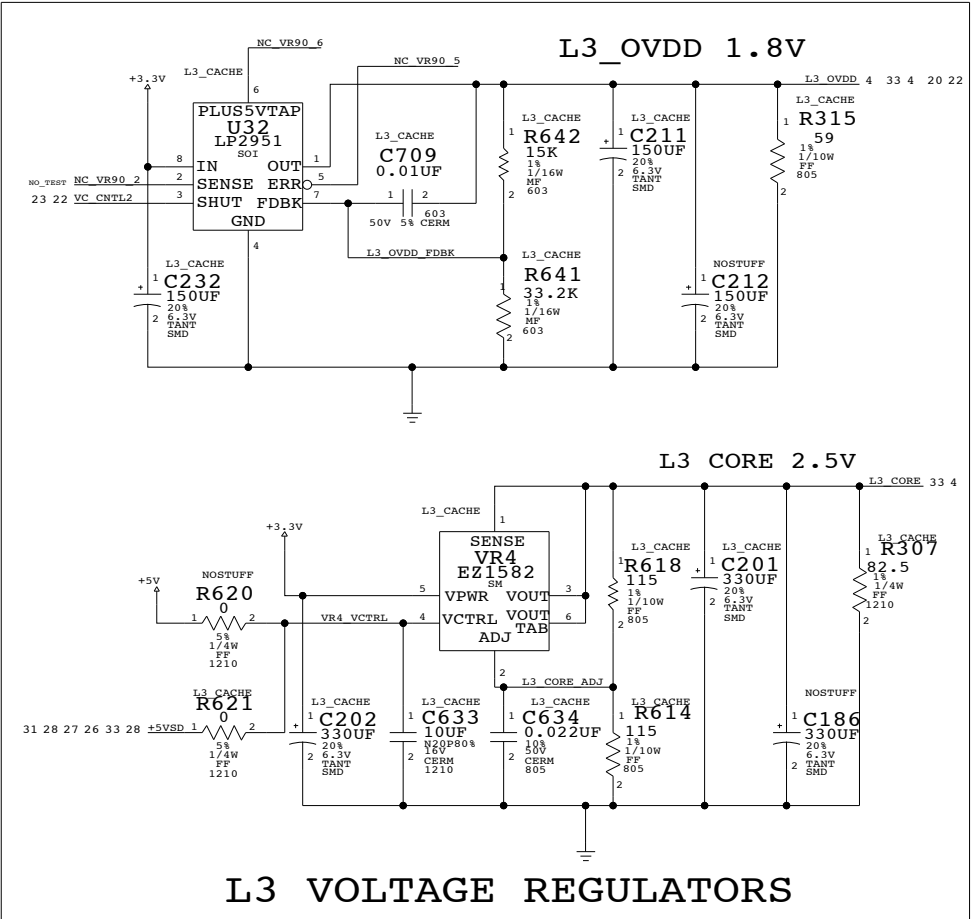
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SIZE	DRAWING NUMBER	REV.
D	051-6101	12
SCALE	SHT	OF
NONE	20	44



PULLUP FOR CPU\_TMS IS ON SH 24, R519  
 PULLUP FOR CPU\_TDI IS ON SH 24, R524  
 PULLUP FOR CPU\_HRESET\* IS ON SH 23, R202



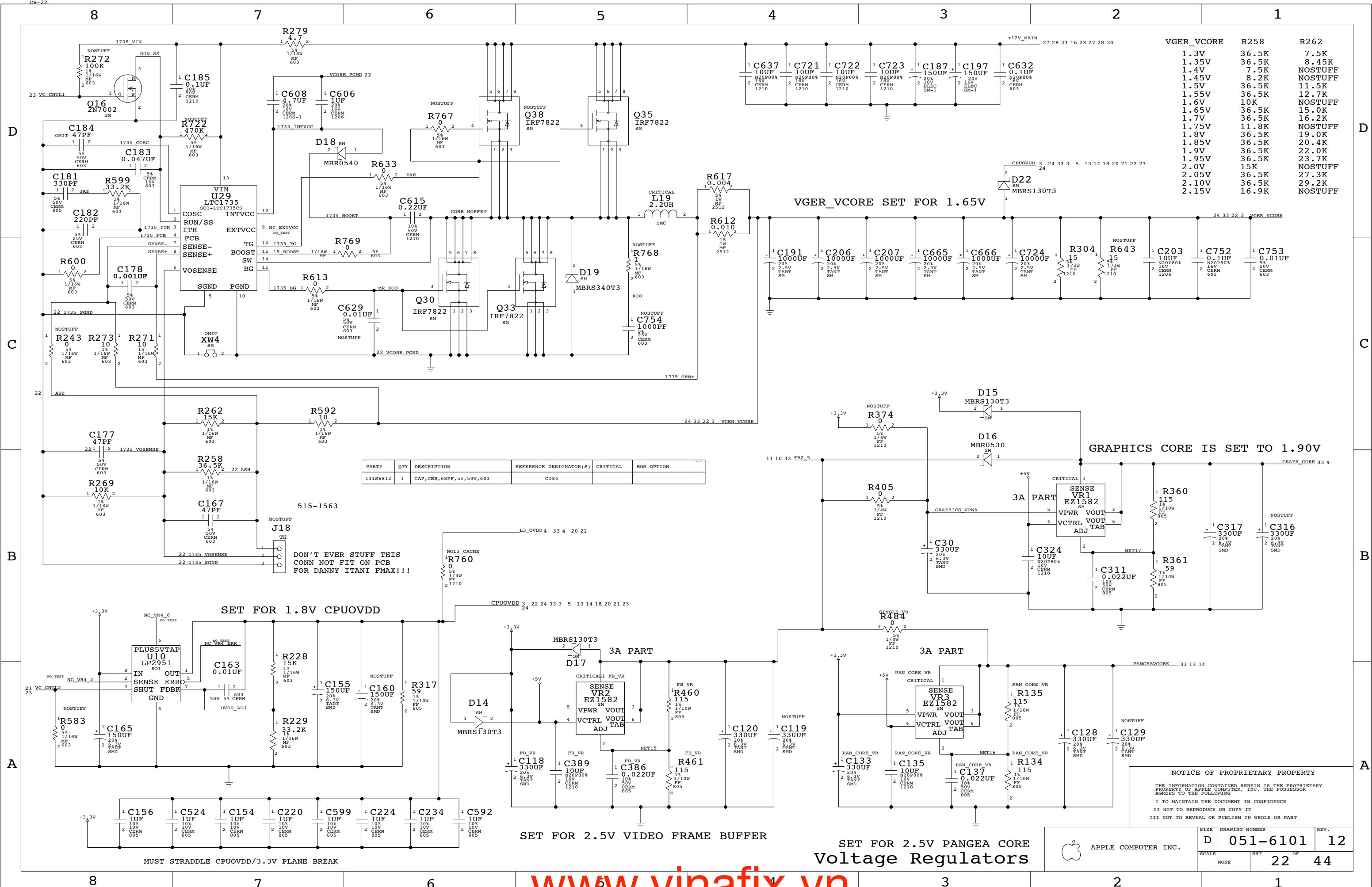
L3 VOLTAGE REGULATORS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S1005	1	IIC EEPROM 32KX8 SOIC	U36	IIC_256K_BLANK
341S1134	1	GROMIT SERIAL EEPROM PROGRAMMED	U36	IIC_PROGRAMMED

BOOTBANGER

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	D	051-6101	12
SCALE	SHT	OF	
NONE	21	44	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
13186812	1	CAP,CER,68PF,5%,50V,603	C184		

DON'T EVER STUFF THIS  
CONN NOT FIT ON PCB  
FOR DANNY ITANI FMAX!!!

SET FOR 1.8V CPUOVDD

SET FOR 2.5V VIDEO FRAME BUFFER

SET FOR 2.5V PANGEA CORE  
Voltage Regulators

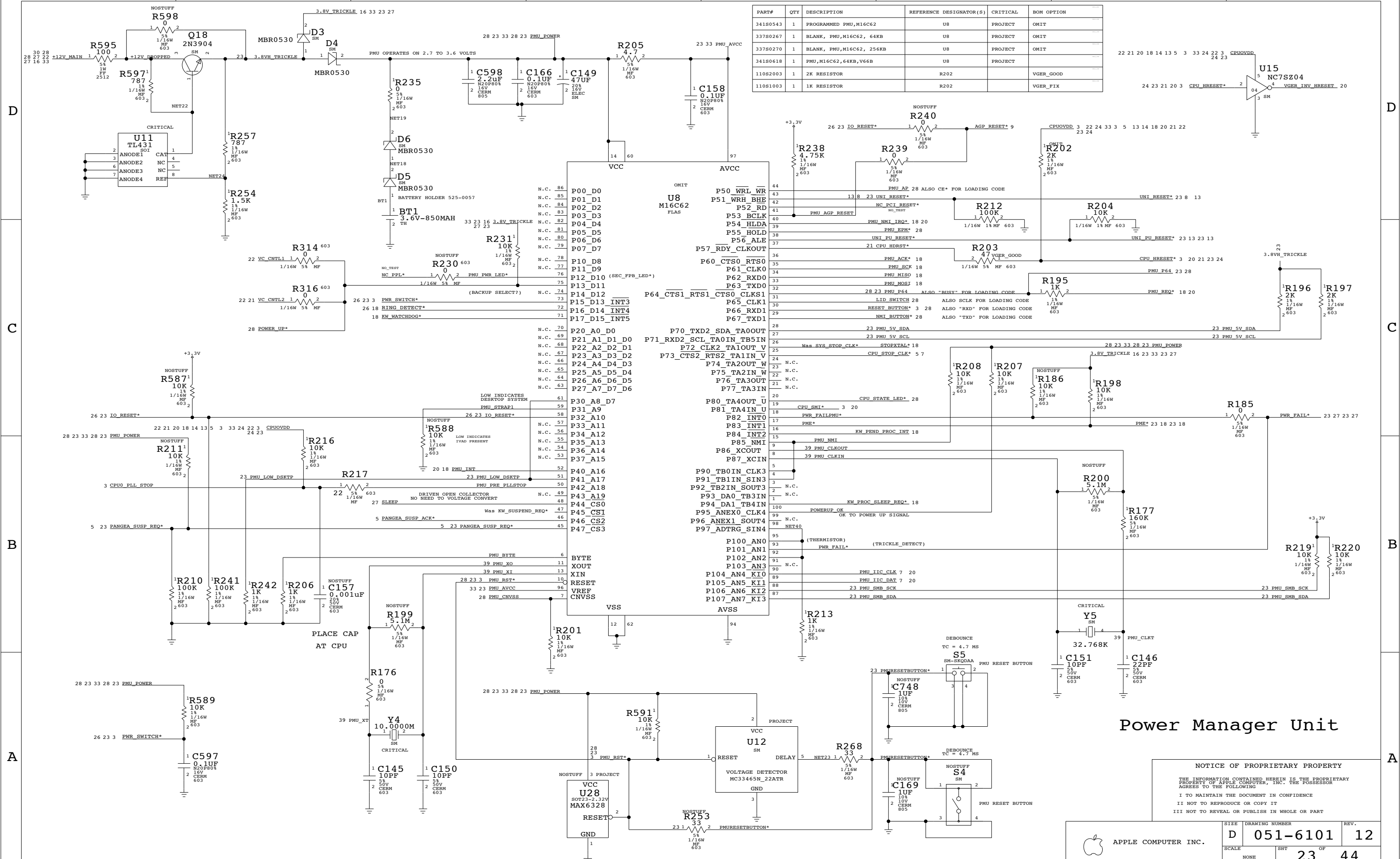
GRAPHICS CORE IS SET TO 1.90V

VGER_VCORE	R258	R262
1.3V	36.5K	7.5K
1.35V	36.5K	8.45K
1.4V	7.5K	NOSTUFF
1.45V	8.2K	NOSTUFF
1.5V	36.5K	11.5K
1.55V	36.5K	12.7K
1.6V	10K	NOSTUFF
1.65V	36.5K	15.0K
1.7V	36.5K	16.2K
1.75V	11.8K	NOSTUFF
1.8V	36.5K	19.0K
1.85V	36.5K	20.4K
1.9V	36.5K	22.0K
1.95V	36.5K	23.7K
2.0V	15K	NOSTUFF
2.05V	36.5K	27.3K
2.10V	36.5K	29.2K
2.15V	16.9K	NOSTUFF

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6101	12
SCALE	NONE	SHT	OF
		22	44

MUST STRADDLE CPUOVDD/3.3V PLANE BREAK



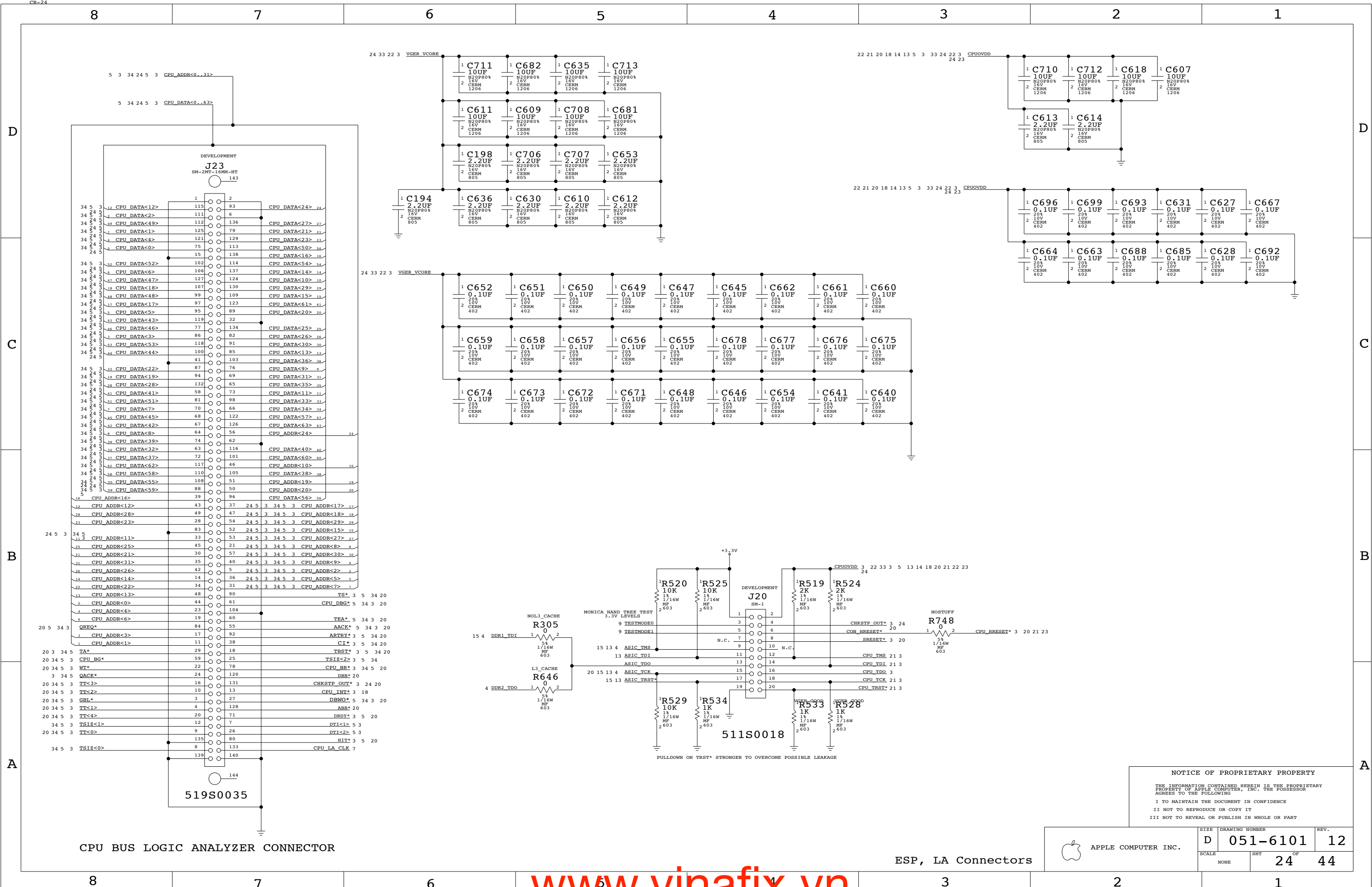
# Power Manager Unit

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	D	051-6101	12
SCALE	SHT	OF	
NONE	23	44	



CPU BUS LOGIC ANALYZER CONNECTOR

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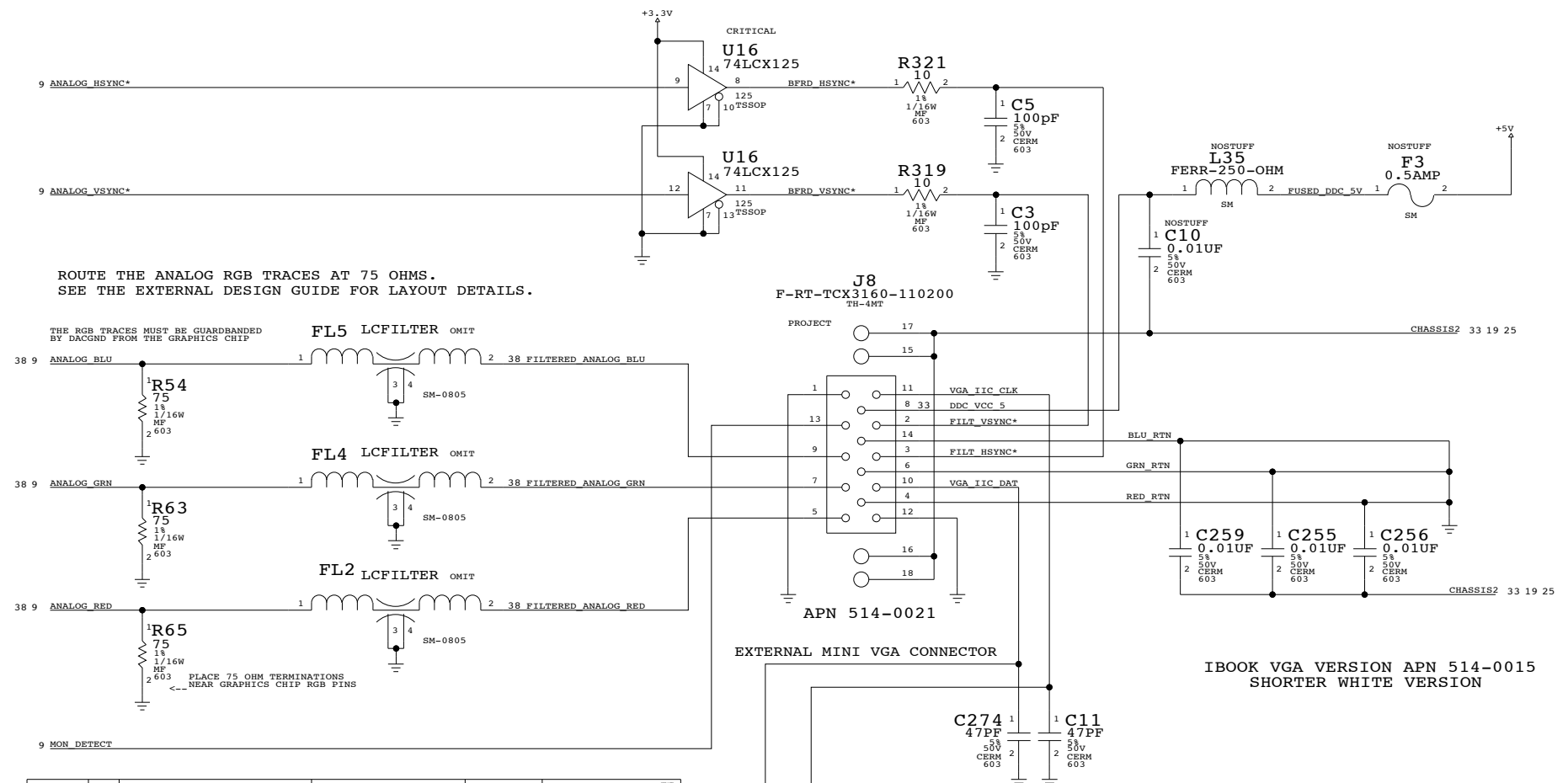
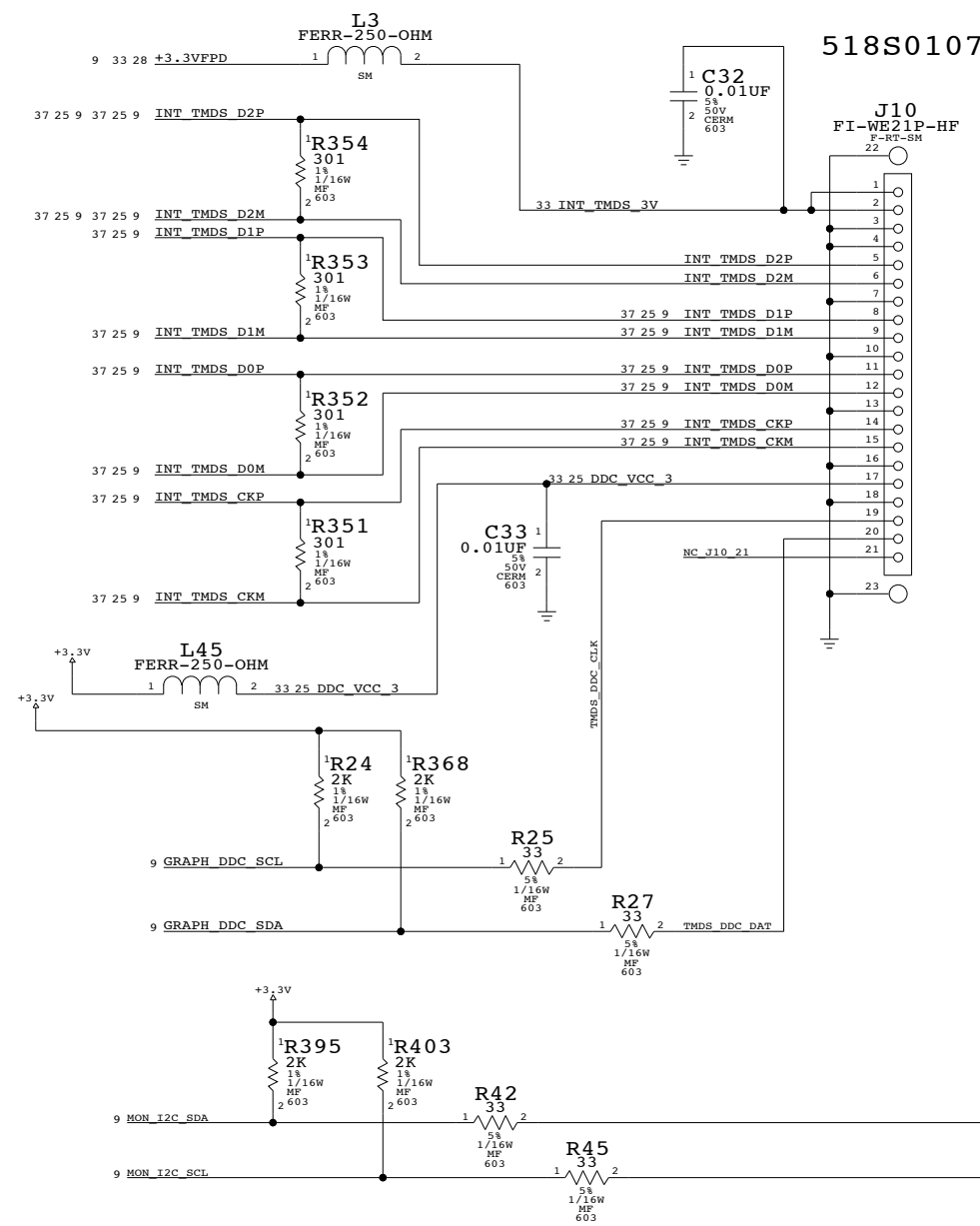
SIZE	DRAWING NUMBER	REV.
D	051-6101	12
SCALE	SHT	OF
NONE	24	44

ESP, LA Connectors



# INTERNAL TMDS CONNECTOR, EXTERNAL VGA CONNECTOR AND GRAPHICS CHIP STRAP OPTIONS

## Internal TMDS Connector



ROUTE THE ANALOG RGB TRACES AT 75 OHMS.  
SEE THE EXTERNAL DESIGN GUIDE FOR LAYOUT DETAILS.

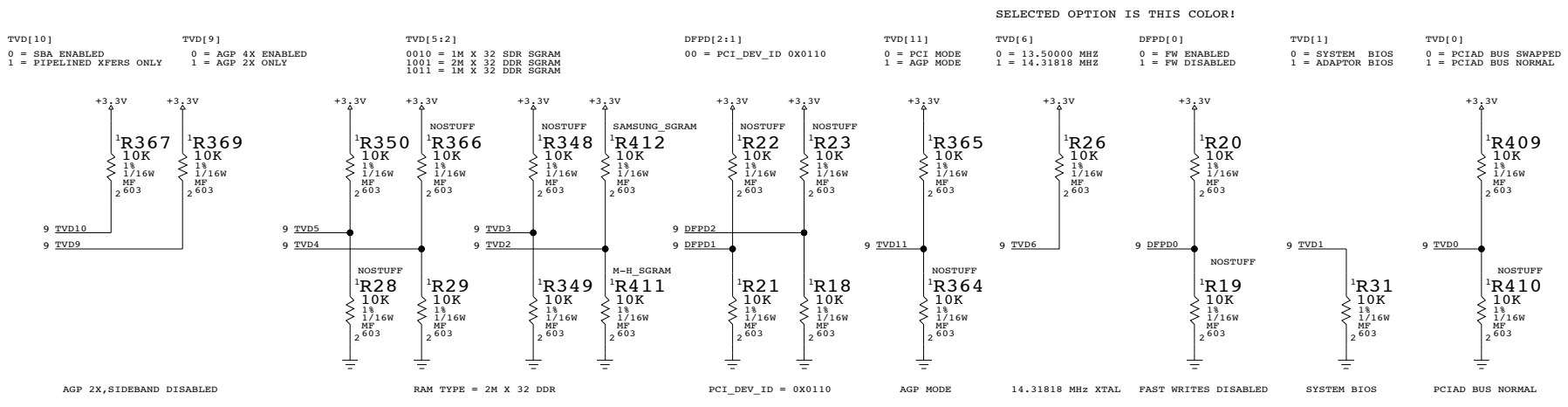
THE RGB TRACES MUST BE GUARDBANDED BY DACOND FROM THE GRAPHICS CHIP

PLACE 75 OHM TERMINATIONS  
NEAR GRAPHICS CHIP RGB PINS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S0012	3	FILTER_LC	FL5, FL4, FL2		

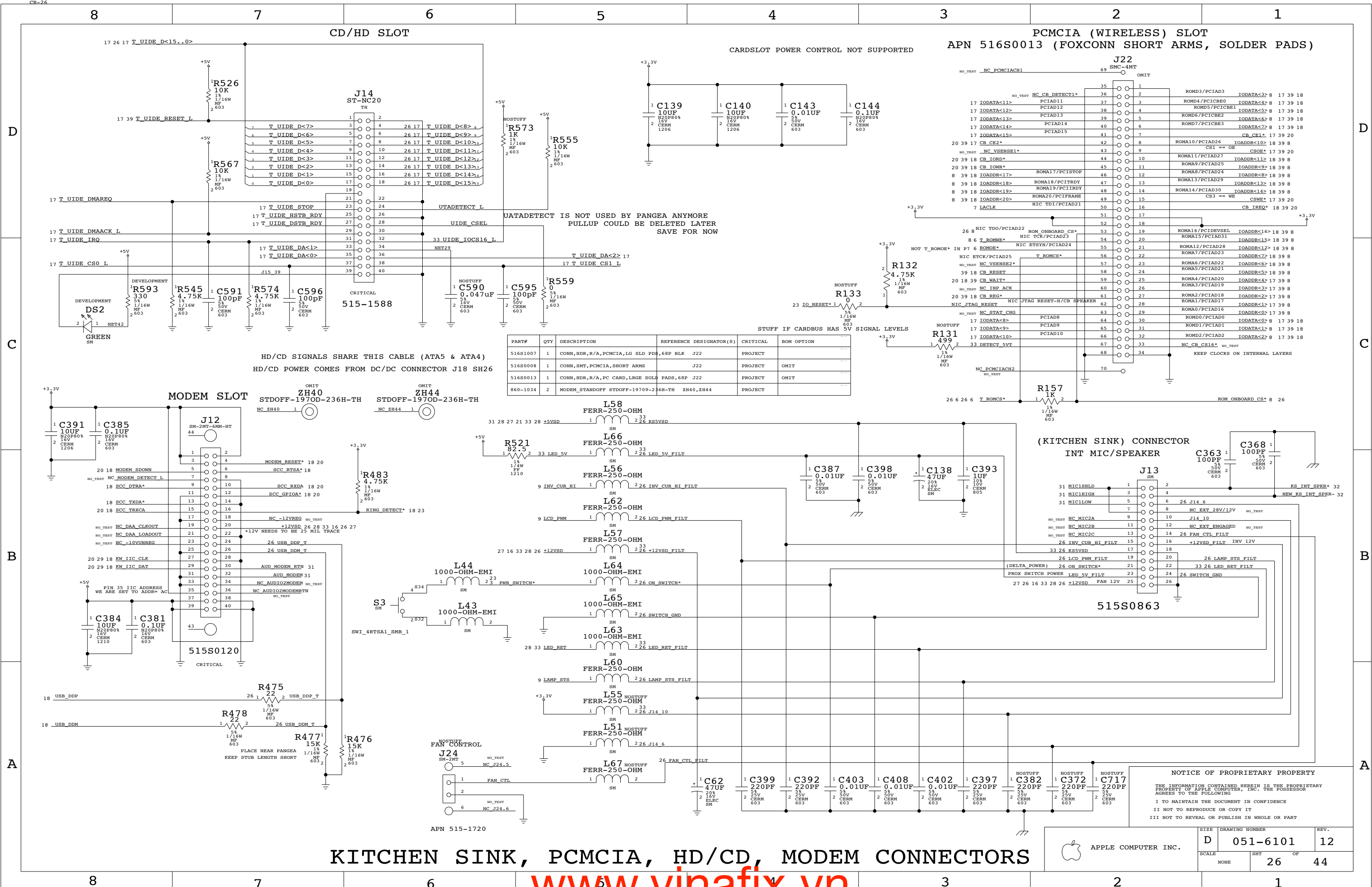
APN 155S0012 DOESN'T EXIST IN DATABASE, SYMBOLS ARE 155S0010

## External VGA Connector



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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6101	12
SCALE	SHT	OF	
NONE	25	44	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
51681007	1	CONN,HDR,R/A,PCMCIA, LG SLD PDS, 68P BLK	J22	PROJECT	OMIT
51680008	1	CONN,SMT,PCMCIA, SHORT ARMS	J22	PROJECT	OMIT
51680013	1	CONN,HDR,R/A, PC CARD, LRGE SLD PADS, 68P	J22	PROJECT	OMIT
860-1034	2	MODEM_STANDOFF STD0FF-19709-236H-TH	ZH40, ZH44	PROJECT	

HD/CD SIGNALS SHARE THIS CABLE (ATA5 & ATA4)  
 HD/CD POWER COMES FROM DC/DC CONNECTOR J18 SH26

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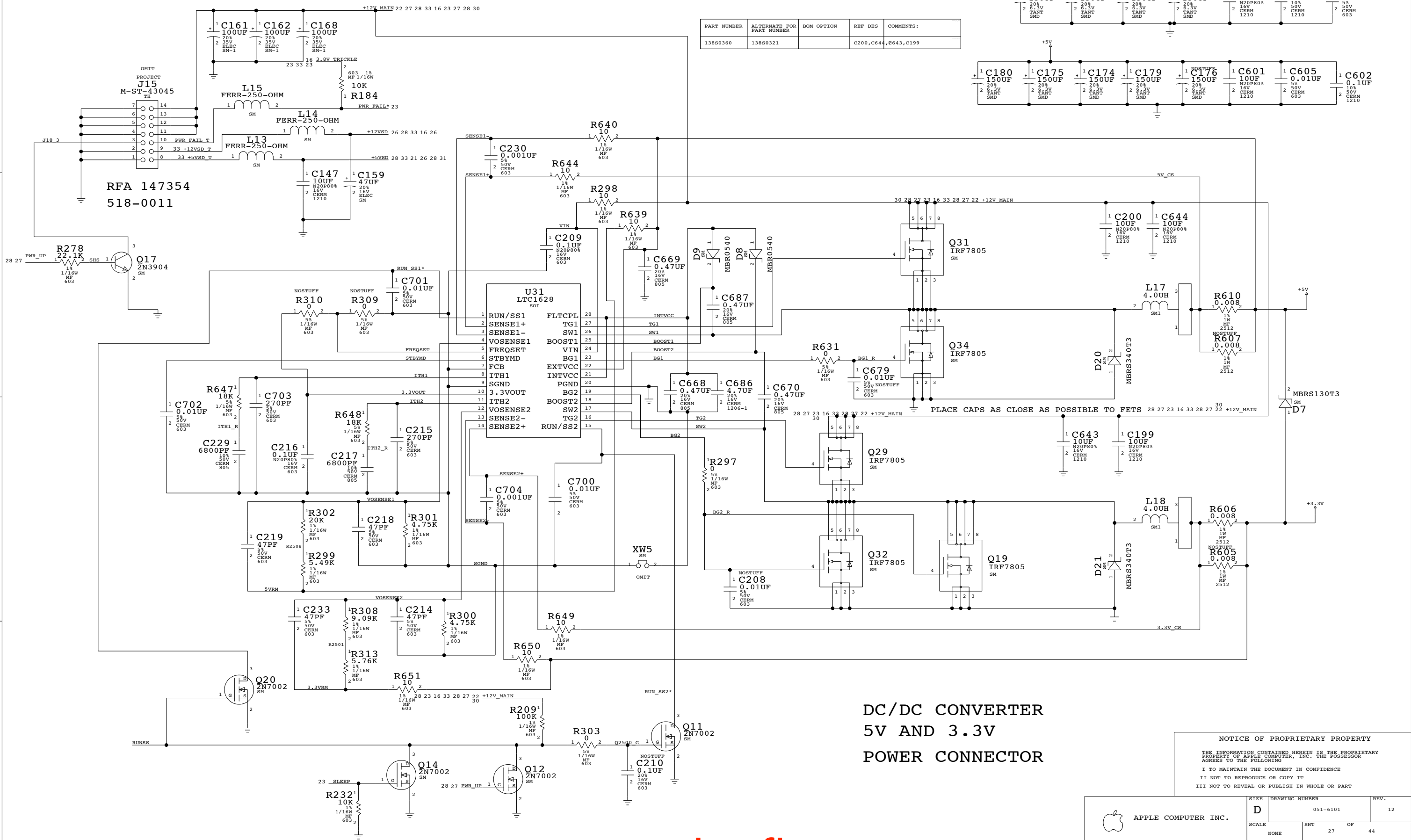
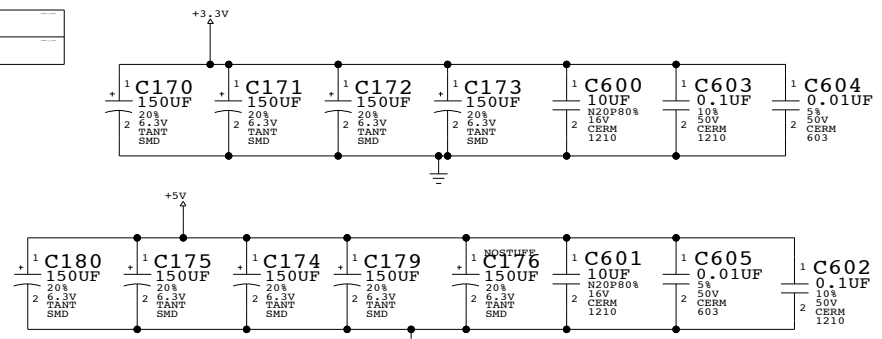
# KITCHEN SINK, PCMCIA, HD/CD, MODEM CONNECTORS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6101	12
SCALE	SHT	OF
NONE	26	44

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
518-0011	1	CONN,HDR,STR,3MM PTCH,14-P,REFLOW	J15	PROJECT	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0360	138S0321		C200,C644,C643,C199	



DC/DC CONVERTER  
5V AND 3.3V  
POWER CONNECTOR

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6101	12
SCALE	SHT	OF	
NONE	27	44	

D

C

B

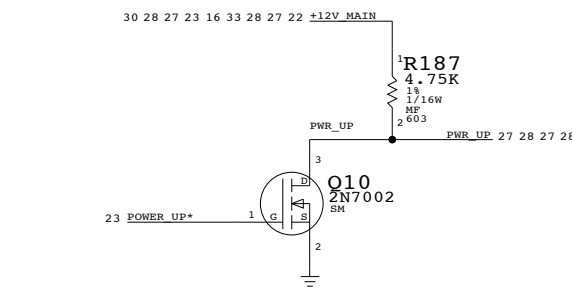
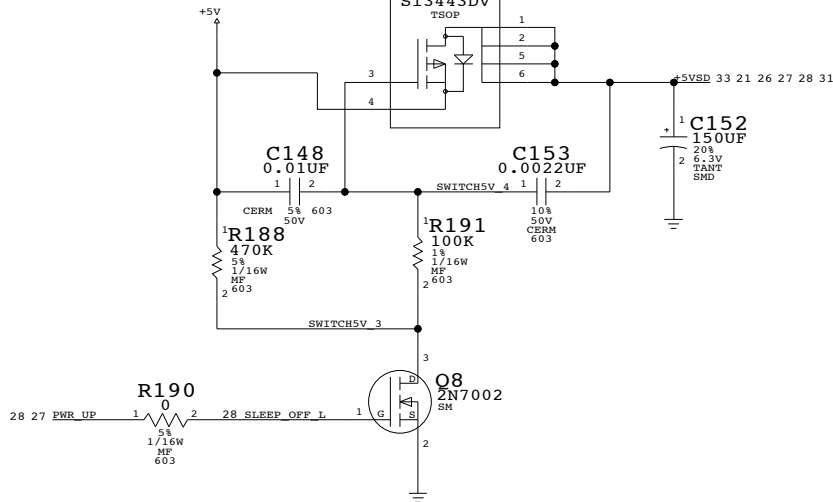
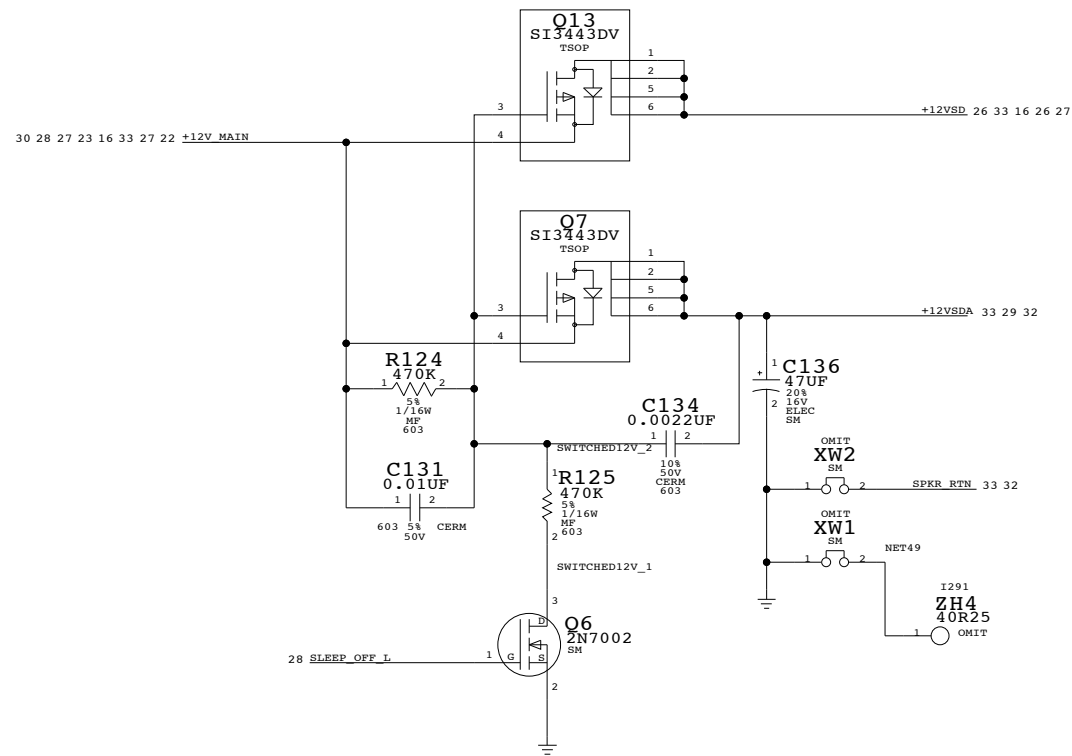
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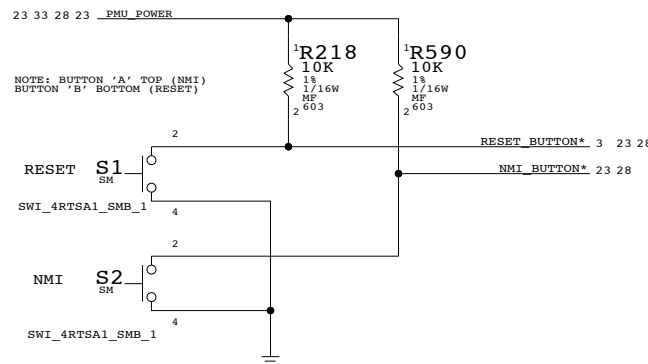
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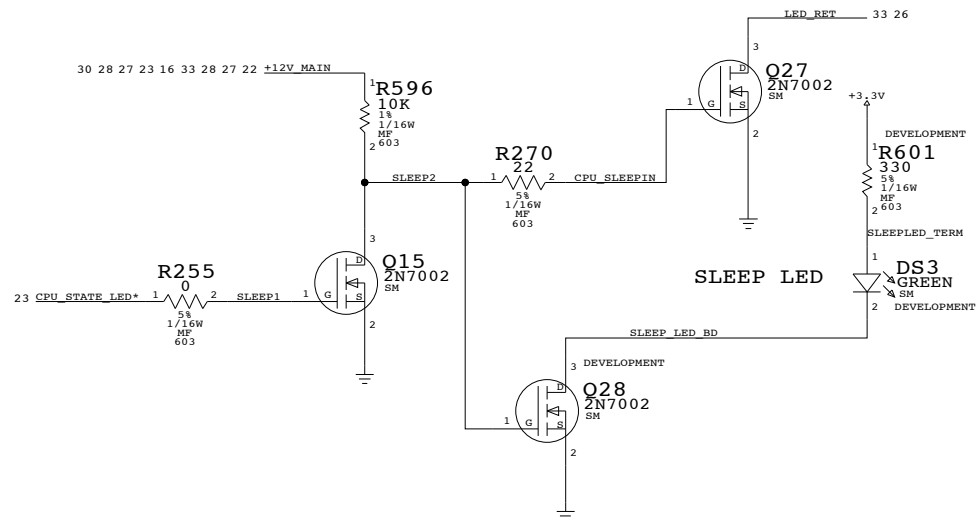
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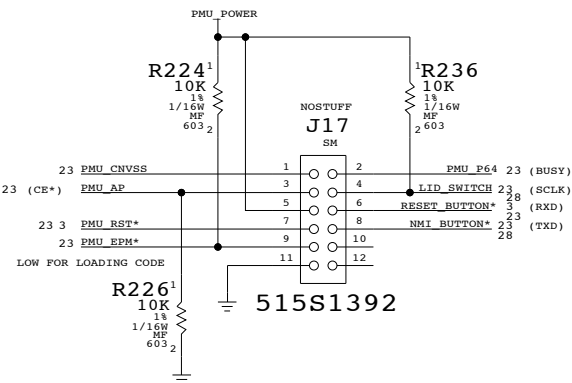
CPU SLEEP LED CKT FROM TRINITY



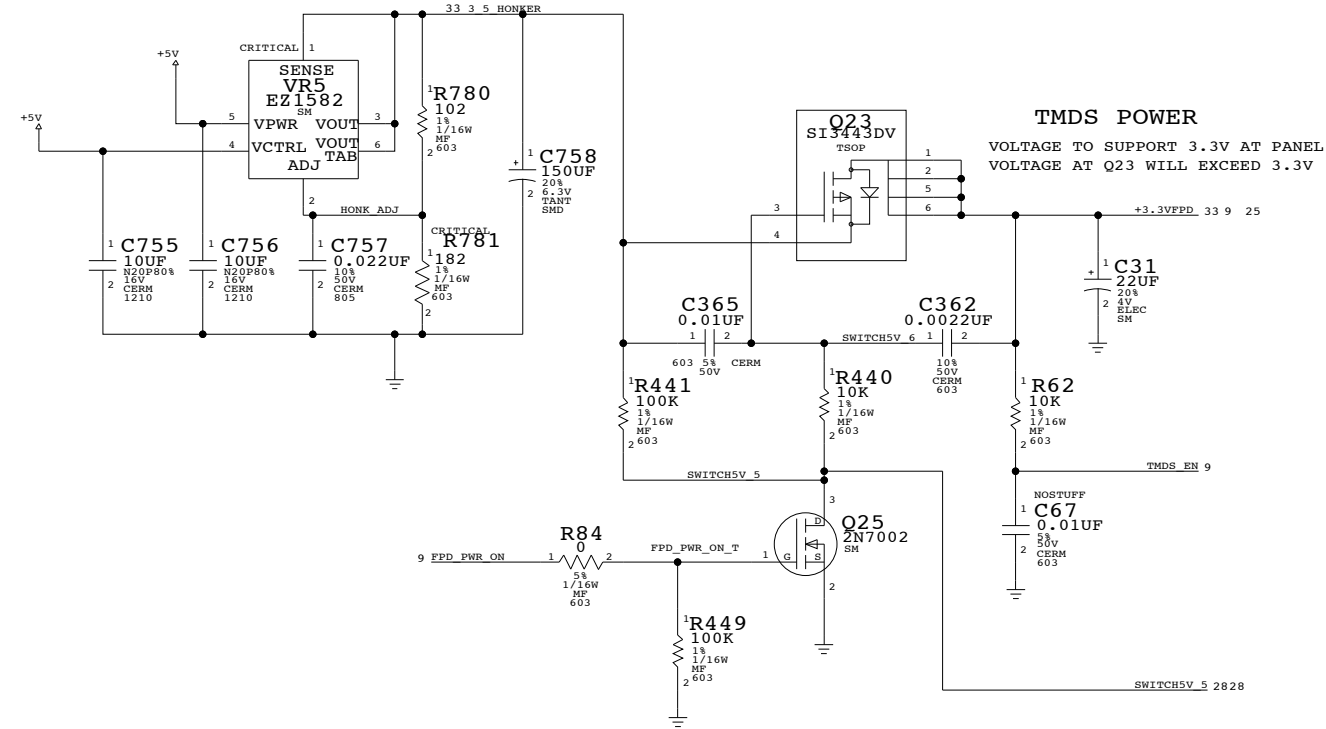
SERIAL DOWNLOAD CONNECTOR



SLEEP LED



PMU SERIAL DL, LPWR CTRL, TMDS POWER

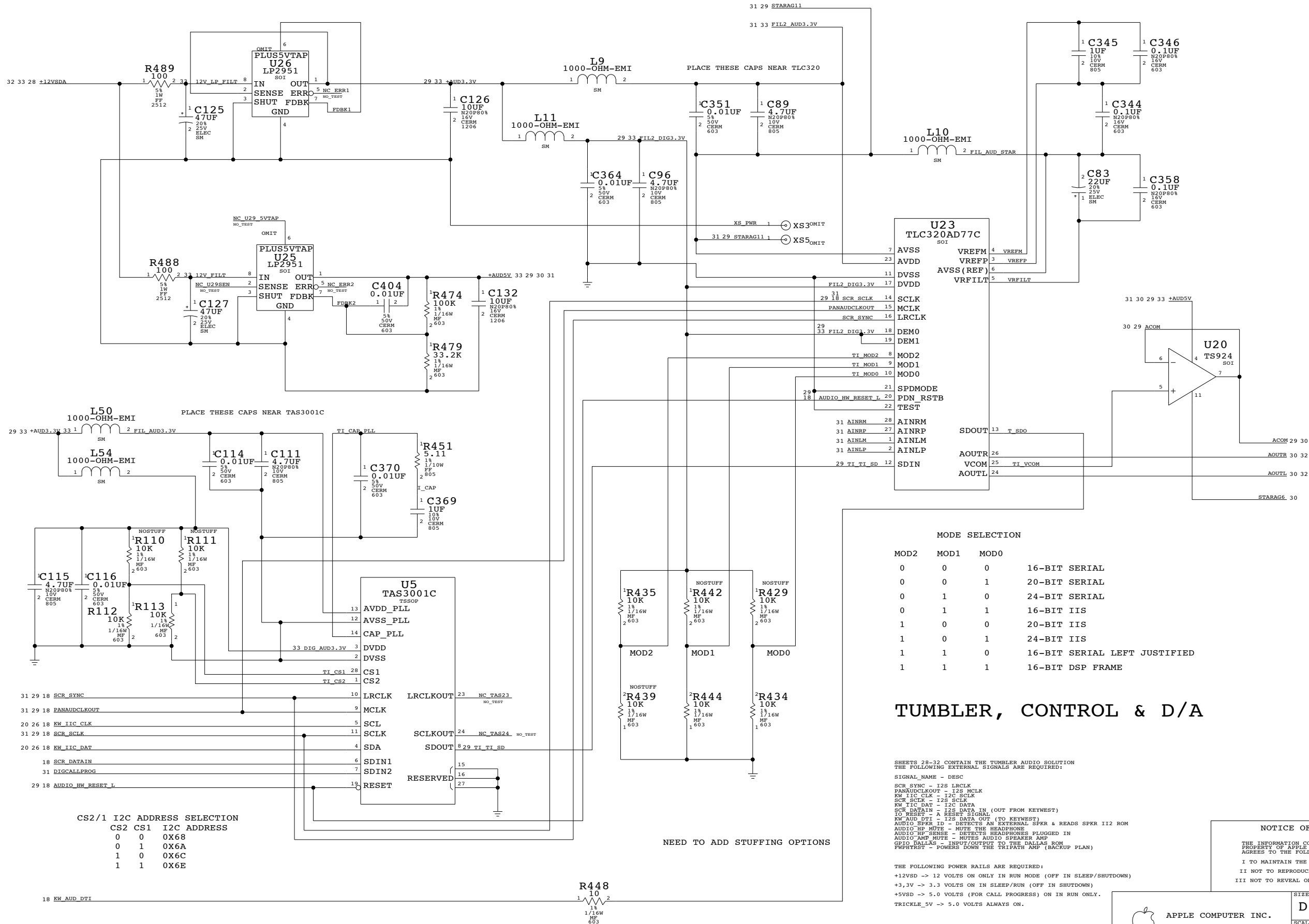


TMDS POWER  
VOLTAGE TO SUPPORT 3.3V AT PANEL  
VOLTAGE AT Q23 WILL EXCEED 3.3V

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	D	051-6101	12
SCALE	NONE	SHT	OF
		28	44

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
35380275	2	IC, 2951, ADJ, UPWR, REG, 8P, SOP	U25, U26		



CS2/1 I2C ADDRESS SELECTION

CS2	CS1	I2C ADDRESS
0	0	0X68
0	1	0X6A
1	0	0X6C
1	1	0X6E

MODE SELECTION

MOD2	MOD1	MOD0	MODE
0	0	0	16-BIT SERIAL
0	0	1	20-BIT SERIAL
0	1	0	24-BIT SERIAL
0	1	1	16-BIT IIS
1	0	0	20-BIT IIS
1	0	1	24-BIT IIS
1	1	0	16-BIT SERIAL LEFT JUSTIFIED
1	1	1	16-BIT DSP FRAME

### TUMBLER, CONTROL & D/A

SHEETS 28-32 CONTAIN THE TUMBLER AUDIO SOLUTION THE FOLLOWING EXTERNAL SIGNALS ARE REQUIRED:

SIGNAL\_NAME - DESC

SCR\_SYNC - I2S LRCLK  
 PANAUDCLKOUT - I2S MCLK  
 KW\_IIC\_CLK - I2C SCLK  
 SCR\_SCLK - I2S SCLK  
 KW\_IIC\_DAT - I2C DATA  
 SCR\_DATAIN - I2S DATA IN (OUT FROM KEYWEST)  
 IO\_RESET - A RESET SIGNAL  
 KW\_AUD\_DTI - I2S DATA OUT (TO KEYWEST)  
 AUDIO\_SPKR\_ID - DETECTS AN EXTERNAL SPKR & READS SPKR I12 ROM  
 AUDIO\_HP\_MUTE - MUTE THE HEADPHONE PLUGGED IN  
 AUDIO\_AMP\_MUTE - MUTES AUDIO SPEAKER AMP  
 GPIO\_DALLAS - INPUT/OUTPUT TO THE DALLAS ROM  
 FWRESET - POWERS DOWN THE TRIPATH AMP (BACKUP PLAN)

THE FOLLOWING POWER RAILS ARE REQUIRED:

+12VSD -> 12 VOLTS ON ONLY IN RUN MODE (OFF IN SLEEP/SHUTDOWN)  
 +3,3V -> 3.3 VOLTS ON IN SLEEP/RUN (OFF IN SHUTDOWN)  
 +5VSD -> 5.0 VOLTS (FOR CALL PROGRESS) ON IN RUN ONLY.  
 TRICKLE\_5V -> 5.0 VOLTS ALWAYS ON.

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SIZE	D	DRAWING NUMBER	051-6101	REV.	12
SCALE	NONE	SHT	29	OF	44

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0029	1	CONN, RCPT, R/A, 3.5MMHPFINE, 6.5MM H, 8MM, 3P	J9	PROJECT	

D

D

C

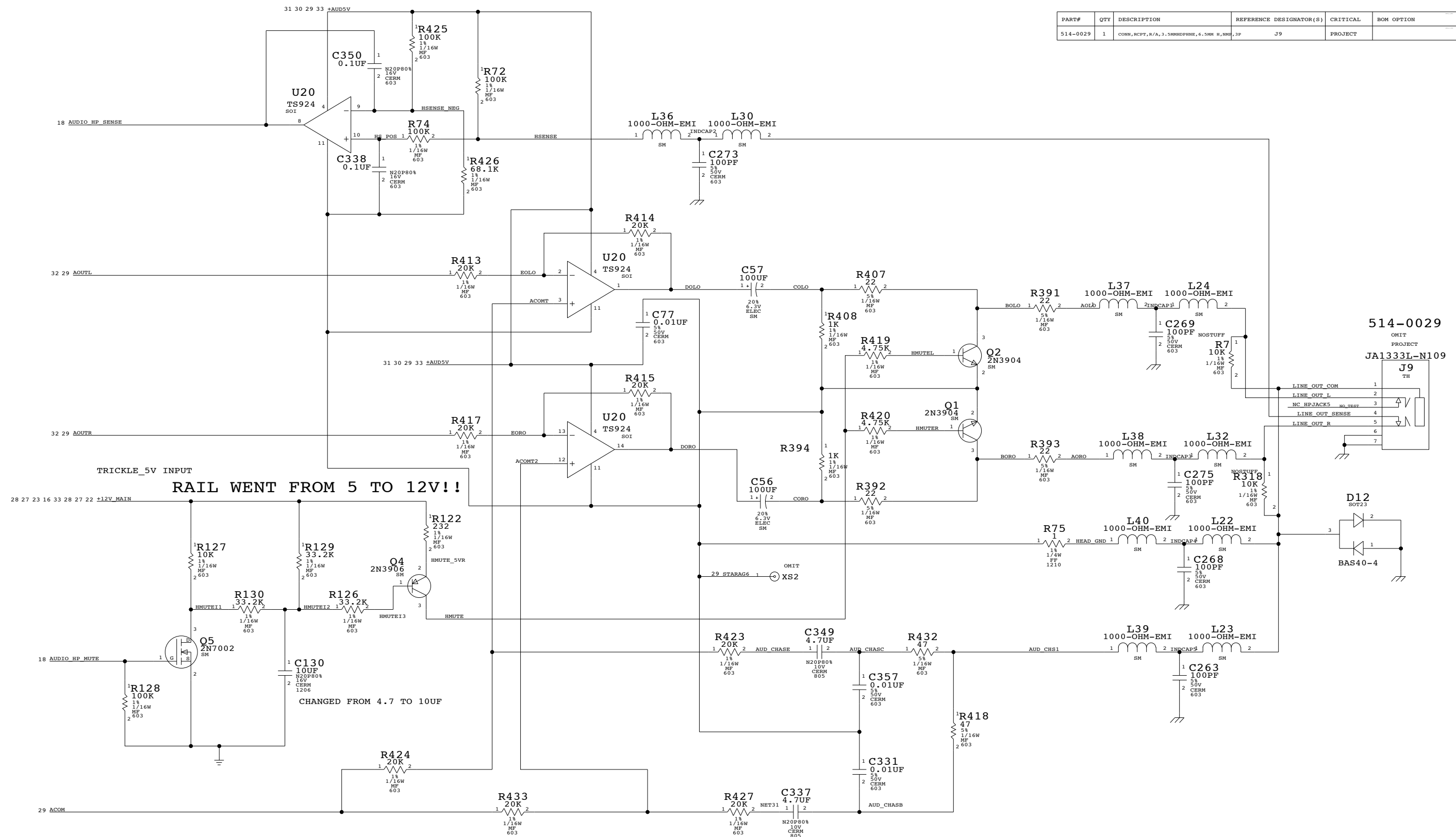
C

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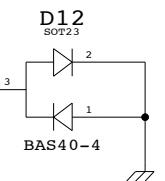
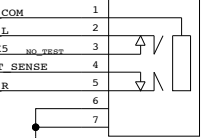
B

A

A



514-0029  
OMIT  
PROJECT  
JA1333L-N109



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### TUMBLER AUDIO, HEADPHONE DRIVER

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6101	12
SCALE	NONE	SHT	OF
		30	44

D

C

B

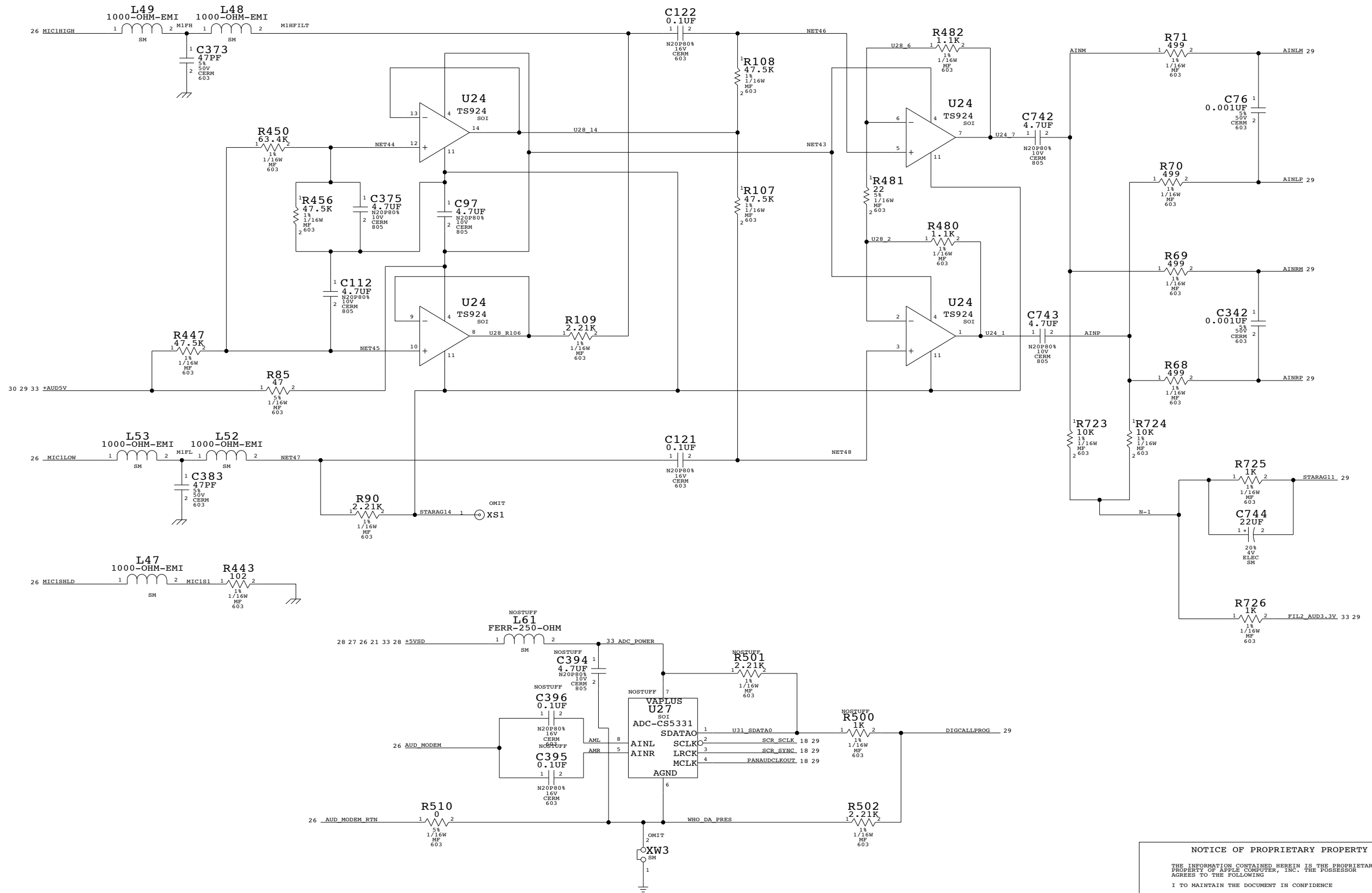
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D

C

B

A



### TUMBLER AUDIO, MICROPHONE PREAMP AND MODEM CALL PROGRESS

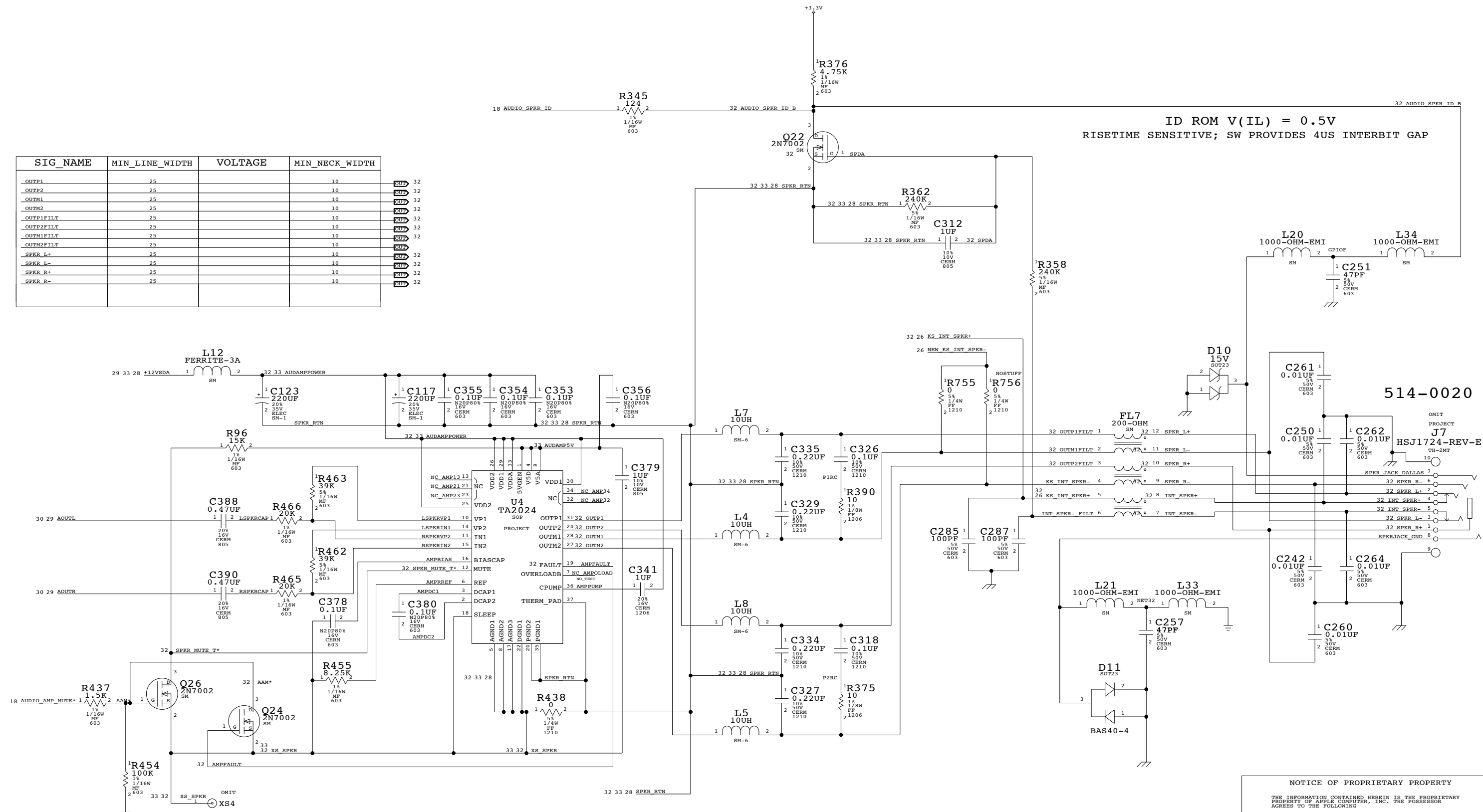
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6101	12
SCALE	SHT OF		
NONE	31 OF		44

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0020	1	CONN, 2.5MM PH JACK, RT ANG, 6-P	NMP J7	PROJECT	

SIG_NAME	MIN_LINE_WIDTH	VOLTAGE	MIN_NECK_WIDTH
OUTP1	25		10
OUTP2	25		10
OUTM1	25		10
OUTM2	25		10
OUTP1FILT	25		10
OUTP2FILT	25		10
OUTM1FILT	25		10
OUTM2FILT	25		10
SPKR L+	25		10
SPKR L-	25		10
SPKR R+	25		10
SPKR R-	25		10

ID ROM V(IL) = 0.5V  
RISETIME SENSITIVE; SW PROVIDES 4US INTERBIT GAP



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	D	051-6101	12
SCALE	SHT	OF	
NONE	32	44	

TUMBLER AUDIO, POWER AMP.



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6101	1	SCHEM,PCBA,P11	PCB1	
056-0862	1	DESIGN GUIDE	PCB1	
056-0928	1	DWG,DSGN GD,MLB,P11	PCB1	OMIT
613-3302	1	GEN DWG, PCBA MECH SUBASSY	PCB1	
820-1257	1	PCBF,MLB,P11	PCB1	

DESIGN IF SPECIAL G3 NEEDED>

HARDWARE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
410-1105	2	WIRELESS CONENCTOR SCREW	J22,J22	
835-0101	2	WIRELESS CONNECTOR NUT	J22,J22	
600-9413	1	HEATSINK,MONICA,REAL	U22	OMIT
730-0231	1	HEATSINK,MONICA,STEALTH	U22	OMIT
730-0214	1	HEATSINK,MICROPROCESSOR	U13	OMIT
730-0202	1	HEATSINK,MICROPROCESSOR	U13	OMIT
730-0217	1	HEATSINK,PANGEA	U6	STEALTH
730-0217	1	HEATSINK,PANGEA	U6	REAL
600-9414	1	HEATSINK,TRIPATH,REAL	U4	OMIT
730-0230	1	HEATSINK,TRIPATH,STEALTH	U4	OMIT
875-0498	1	GAP FILLER VGER CPU	U13	REAL

MODEM/MISC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
525-0057	1	BATTERY HOLDER	BT1		
825-2029	1	LABEL,SERIAL NUMBER BARCODE	PCB1		
617-0186	1	MODEM, SPRING, W/RJ11	J12	PROJECT	OMIT
617-0201	1	MODEM, DASH, W/RJ11	J12	PROJECT	OMIT
617-0205	1	MODEM, DASH, W/NO RJ11	J12	PROJECT	OMIT
617-0212	1	EMI FILTER PCB,DASH,W/NO RJ11	J12	PROJECT	OMIT
617-0196	1	MODEM, B4, W/NO RJ11	J12	PROJECT	OMIT
617-0196	1	MODEM, AUS, W/NO RJ11	J12	PROJECT	OMIT

617-0196 ALSO REQUIRES DONGLE 611-0138, BUT THAT IS INCLUDED IN ACCESSORY KIT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
617-0213	1	MODEM, SPRING2, W/NO RJ11	J12	PROJECT	OMIT
617-0212	1	EMI FILTER PCB,SPRING2,W/NO RJ11	J12	PROJECT	OMIT

SODIMMS

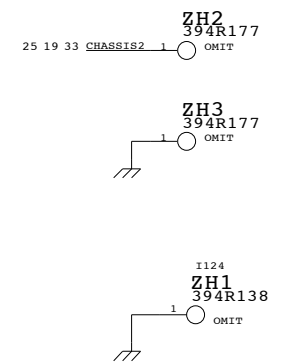
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333-0336	1	IC,SDRAM,64MB ,PC100,SODIMM	J21	PROJECT	OMIT
333-0360	1	IC,SDRAM,128MB,PC100,SODIMM	J21	PROJECT	OMIT
333-0362	1	IC,SDRAM,256MB,PC100,MICRON,SODIMM	J21	PROJECT	OMIT
333-0363	1	IC,SDRAM,256MB,PC100,SAM/HYUN,SODIMM	J21	PROJECT	OMIT
333-0364	1	IC,SDRAM,512MB,PC100,SODIMM	J21	PROJECT	OMIT

MICRON<br>SAMSUNG/HUNDAI>

168 PIN DIMMS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333-0112	1	IC,SDRAM,64MB,PC100,4BK,168P DIMM	J19	PROJECT	OMIT
333-0346	1	IC,SDRAM,128MB,PC100,4BK,168P DIMM	J19	PROJECT	OMIT
333-0347	1	IC,SDRAM,256MB,PC100,4BK,168P DIMM	J19	PROJECT	OMIT
333-0349	1	IC,SDRAM,512MB,PC100,4BK,168P DIMM	J19	PROJECT	OMIT

HOLES AND SLOTS



SIG_NAME	MIN_LINE_WIDTH	VOLTAGE	MIN_NECK_WIDTH
	200	5	10
	25	3.3	10
	100	12	10
	25	0	10
	25	0	10
CPUOVDD	15	1.8	10
VGER_VCORE	15	2.0	10
+AVDD_CPU	25	2.0	10
L3_OVDD	15	1.5	10
L3_CORE	15	2.5	10
PANGEA_AVDD5	10	1.8	10
PANGEA_AVDD4	10	3.3	10
+12VSD_FILT	100	12	10
AGPVDD	10	3.3	10
PANGEA_AVDD6	10	3.3	7
AGPVREF	10	1.32	10
GRAPH_CORE	25	1.9	10
+5VSD	100	5	10
+12VSD	100	12	10
IFP_AVCC	10	3.3	10
MAINCLK_VDD	25	3.3	10
IFP0AVCC	10	3.3	7
DACVDD	10	3.3	10
FB2_5	25	2.5	10
M_VREF1	10	1.25	10
M_VREF2	10	1.25	10
PANGEA_AMVDD	10	3.3	10
PANGEA_TEI	0	0	10
RTH_RXD_PD	0	0	10
GBE_REFCLK	0	0	10
PANGEA_VCORE	25	2.5	10
VCCA	10	3.3	10
VCC_TFXM	10	3.3	10
PHYAD	0	0	10
ENET_TST	0	0	10
ENETCNT	0	0	10
PWRDWN	0	0	10
FW_PHY_3_3	10	3.3	10
3.8V_TRICKLE	10	3.8	10
3.3V_TO_FW	10	3.3	10
G_SSCLK_VDD	25	3.3	10
FW_VP_2	40	3.0	10
FW_VP_1	40	3.0	10
FW_VP	40	3.0	10
FW_VGND	40	0	10
AUDAMPPOWER	70	12	10
12V_LP_FILT	25	12	10
12V_FILT	25	12	10
J14_10	25	3.3	10
LED_RET	25	5	10
LED_RET_FILT	25	5	10
XS_SPKR	70	0	10

SIG_NAME	MIN_LINE_WIDTH	VOLTAGE	MIN_NECK_WIDTH
CHASSIS2	25	0	10
K55VSD	15	5	10
LED_5V	25	5	10
LED_5V_FILT	25	5	10
PANGEA_VDDA3	10	3.3	7
PANGEA_VDDA2	10	3.3	10
PANGEA_VDDA1	10	3.3	10
VDD_USB	10	3.3	7
USB_PWR_AB	10	3.3	10
USB_PWR_CD	10	3.3	10
USB_PWR_FLT	10	5	10
AUD_STAR	10	0	10
USB_PWR	200	5	10
USB1_PWR	200	5	10
USB1_GND	200	0	10
USB2_PWR	200	5	10
USB2_GND	200	0	10
USB3_PWR	200	5	10
USB3_GND	200	0	10
PMU_POWER	10	3.3	10
PMU_AVCC	10	3.3	10
+3.3VFPD	25	3.3	10
DDC_VCC_3	10	3.3	10
INT_TMD5_3V	10	3.3	10
3_5_HONKER	50	3.5	25
DETECT_5VT	10	3.3	10
+12V_MAIN	600	12	25
+12V_DROPPED	50	12	10
UIDE_IOC816_L	10	5	10
+12VSDA	100	12	10
+5VSD_T	40	5	10
+12VSD_T	40	12	10
+AUD5V	10	5	10
FIL2_DIG3_3V	10	3.3	10
ADC_POWER	40	5	10
DIG_AUD3_3V	10	3.3	10
FIL_AUD3_3V	10	3.3	10
+AUD3_3V	15	3.3	10
AUD_STAR	15	0	10
FIL2_AUD3_3V	10	3.3	10
AUDAMP5V	10	5	10
SPKR_RTN	100	0	10
DDC_VCC_5	50	0	10
FUSED_DDC_5V	50	0	10

I/O CONNECTORS

CONNECTOR	SHEET	DESIGNATOR
USB	SHEET 18	J2, J3, J5
ETHERNET	SHEET 14	J1
FIREWIRE	SHEET 15	J4, J6
VGA	SHEET 24	J8
HEADPHONE	SHEET 29	J9
MODEM	MODEM SCHEM	MODEM SCHEM
DC IN	SHEET 26	J15
SPKR	SHEET 31	J7

Holes and Slots AND EMC INFO

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	D	051-6101	12
SCALE	SHT	OF	
NONE	33	44	



8 7 6 5 4 3 2 1

SIG_NAME	PULSE_PARAM	MAX_VIA_COUNT	DELAY_RULE	STUB_LENGTH	NET_SPACING_TYPE	NET_SCHED
MDATA<0>	100000000::	6	::1850:4400	200		U6.AG1 J21.3 J19.2
MDATA<1>	100000000::	6	::1850:4400	200		U6.AF3 J21.5 J19.3
MDATA<2>	100000000::	6	::1850:4400	200		U6.AF1 J21.7 J19.4
MDATA<3>	100000000::	6	::1850:4400	200		U6.AE2 J21.9 J19.5
MDATA<4>	100000000::	6	::1850:4400	200		U6.AE1 J21.13 J19.7
MDATA<5>	100000000::	6	::1850:4400	200		U6.AD2 J21.15 J19.8
MDATA<6>	100000000::	6	::1850:4400	200		U6.AD1 J21.17 J19.9
MDATA<7>	100000000::	6	::1850:4400	200		U6.AC2 J21.19 J19.10
MDATA<8>	100000000::	6	::1850:4400	200		U6.Y1 J21.37 J19.11
MDATA<9>	100000000::	6	::1850:4400	200		U6.Y2 J21.39 J19.13
MDATA<10>	100000000::	6	::1850:4400	200		U6.W1 J21.41 J19.14
MDATA<11>	100000000::	6	::1850:4400	200		U6.W2 J21.43 J19.15
MDATA<12>	100000000::	6	::1850:4400	200		U6.V2 J21.47 J19.16
MDATA<13>	100000000::	6	::1850:4400	200		U6.U2 J21.49 J19.17
MDATA<14>	100000000::	6	::1850:4400	200		U6.T1 J21.51 J19.19
MDATA<15>	100000000::	6	::1850:4400	200		U6.T2 J21.53 J19.20
MDATA<16>	100000000::	6	::1850:4400	200		U6.R1 J21.83 J19.55
MDATA<17>	100000000::	6	::1850:4400	200		U6.R2 J21.85 J19.56
MDATA<18>	100000000::	6	::1850:4400	200		U6.P3 J21.87 J19.57
MDATA<19>	100000000::	6	::1850:4400	200		U6.P2 J21.89 J19.58
MDATA<20>	100000000::	6	::1850:4400	200		U6.N1 J21.93 J19.60
MDATA<21>	100000000::	6	::1850:4400	200		U6.N2 J21.95 J19.65
MDATA<22>	100000000::	6	::1850:4400	200		U6.M1 J21.97 J19.66
MDATA<23>	100000000::	6	::1850:4400	200		U6.M2 J21.99 J19.67
MDATA<24>	100000000::	6	::1850:4400	200		U6.J2 J21.121 J19.69
MDATA<25>	100000000::	6	::1850:4400	200		U6.H2 J21.123 J19.70
MDATA<26>	100000000::	6	::1850:4400	200		U6.G1 J21.125 J19.71
MDATA<27>	100000000::	6	::1850:4400	200		U6.G2 J21.127 J19.72
MDATA<28>	100000000::	6	::1850:4400	200		U6.F1 J21.131 J19.74
MDATA<29>	100000000::	6	::1850:4400	200		U6.F2 J21.133 J19.75
MDATA<30>	100000000::	6	::1850:4400	200		U6.E1 J21.135 J19.76
MDATA<31>	100000000::	6	::1850:4400	200		U6.H3 J21.137 J19.77
MDATA<32>	100000000::	6	::1850:4400	200		U6.AD3 J21.4 J19.86
MDATA<33>	100000000::	6	::1850:4400	200		U6.AD5 J21.6 J19.87
MDATA<34>	100000000::	6	::1850:4400	200		U6.AC3 J21.8 J19.88
MDATA<35>	100000000::	6	::1850:4400	200		U6.AC5 J21.10 J19.89
MDATA<36>	100000000::	6	::1850:4400	200		U6.AC6 J21.14 J19.91
MDATA<37>	100000000::	6	::1850:4400	200		U6.AC7 J21.16 J19.92
MDATA<38>	100000000::	6	::1850:4400	200		U6.AB6 J21.18 J19.93
MDATA<39>	100000000::	6	::1850:4400	200		U6.AB7 J21.20 J19.94
MDATA<40>	100000000::	6	::1850:4400	200		U6.AA5 J21.38 J19.95
MDATA<41>	100000000::	6	::1850:4400	200		U6.AA6 J21.40 J19.97
MDATA<42>	100000000::	6	::1850:4400	200		U6.AA7 J21.42 J19.98
MDATA<43>	100000000::	6	::1850:4400	200		U6.AC1 J21.44 J19.99
MDATA<44>	100000000::	6	::1850:4400	200		U6.V3 J21.48 J19.100
MDATA<45>	100000000::	6	::1850:4400	200		U6.V5 J21.50 J19.101
MDATA<46>	100000000::	6	::1850:4400	200		U6.V6 J21.52 J19.103
MDATA<47>	100000000::	6	::1850:4400	200		U6.W7 J21.54 J19.104
MDATA<48>	100000000::	6	::1850:4400	200		U6.U3 J21.84 J19.139
MDATA<49>	100000000::	6	::1850:4400	200		U6.U5 J21.86 J19.140
MDATA<50>	100000000::	6	::1850:4400	200		U6.U6 J21.88 J19.141
MDATA<51>	100000000::	6	::1850:4400	200		U6.U7 J21.90 J19.142
MDATA<52>	100000000::	6	::1850:4400	200		U6.R6 J21.94 J19.144
MDATA<53>	100000000::	6	::1850:4400	200		U6.R7 J21.96 J19.149
MDATA<54>	100000000::	6	::1850:4400	200		U6.P5 J21.98 J19.150
MDATA<55>	100000000::	6	::1850:4400	200		U6.P6 J21.100 J19.151
MDATA<56>	100000000::	6	::1850:4400	200		U6.L6 J21.122 J19.153
MDATA<57>	100000000::	6	::1850:4400	200		U6.L7 J21.124 J19.154
MDATA<58>	100000000::	6	::1850:4400	200		U6.K6 J21.126 J19.155
MDATA<59>	100000000::	6	::1850:4400	200		U6.K7 J21.128 J19.156
MDATA<60>	100000000::	6	::1850:4400	200		U6.J3 J21.132 J19.158
MDATA<61>	100000000::	6	::1850:4400	200		U6.J5 J21.134 J19.159
MDATA<62>	100000000::	6	::1850:4400	200		U6.J6 J21.136 J19.160
MDATA<63>	100000000::	6	::1850:4400	200		U6.J7 J21.138 J19.161

SIG_NAME	PULSE_PARAM	MAX_VIA_COUNT	MIN_LINE_WIDTH	NET_SCHED	DELAY_RULE	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE
PANGAMCLK<1>	100000000::	3	6		::1800:2000		100	10 MIL SPACING
PANGAMCLK<3>	100000000::	3	6		::1800:2000		100	10 MIL SPACING
PANGAMCLK<4>	100000000::	3	6		::1800:2000		100	10 MIL SPACING
PANGAMCLK<5>	100000000::	3	6		::1800:2000		100	10 MIL SPACING
PANGAMCLK<6>	100000000::	3	6		::1800:2000		100	10 MIL SPACING
PANGAMCLK<7>	100000000::	3	6		::1800:2000		100	10 MIL SPACING
MAINCLK_XIN	100000000::				::1800:2000			10 MIL SPACING
MAINCLK_XOUT	100000000::				::1800:2000			10 MIL SPACING
MCLK<1>	100000000::	4	6	J21.74 R550.2 R680.2	::2000:3500	250		10 MIL SPACING
MCLK<3>	100000000::	4	6	J21.61 R556.2 R668.2	::2000:3500	250		10 MIL SPACING
MCLK<4>	100000000::	4	6	J19.42 R547.2 R560.2	::2000:3500	250		10 MIL SPACING
MCLK<5>	100000000::	4	6	J19.125 R543.2 R580.2	::2000:3500	250		10 MIL SPACING
MCLK<6>	100000000::	4	6	J19.79 R558.2 R572.2	::2000:4500	250		10 MIL SPACING
MCLK<7>	100000000::	4	6	J19.163 R552.2 R656.2	::2000:4500	250		10 MIL SPACING
MCLKOUT<1>	100000000::	2	6		:::250			10 MIL SPACING
MCLKOUT<3>	100000000::	2	6		:::250			10 MIL SPACING
MCLKOUT<4>	100000000::	2	6		:::250			10 MIL SPACING
MCLKOUT<5>	100000000::	2	6		:::250			10 MIL SPACING
MCLKOUT<6>	100000000::	2	6		:::250			10 MIL SPACING
MCLKOUT<7>	100000000::	2	6		:::250			10 MIL SPACING
M_ADDR<0>	100000000::	4			::400:1200		200	
M_ADDR<1>	100000000::	4			::400:1200		200	
M_ADDR<2>	100000000::	4			::400:1200		200	
M_ADDR<3>	100000000::	4			::400:1200		200	
M_ADDR<4>	100000000::	4			::400:1200		200	
M_ADDR<5>	100000000::	4			::400:1200		200	
M_ADDR<6>	100000000::	4			::400:1200		200	
M_ADDR<7>	100000000::	4			::400:1200		200	
M_ADDR<8>	100000000::	4			::400:1200		200	
M_ADDR<9>	100000000::	4			::400:1200		200	
M_ADDR<10>	100000000::	4			::400:1200		200	
M_ADDR<11>	100000000::	4			::400:1200		200	
M_ADDR<12>	100000000::	4			::400:1200		200	
TERM_M_ADDR<0>	100000000::	8		RP33.2 J21.29 RP29.8	::1100:3200			
TERM_M_ADDR<1>	100000000::	8		RP9.4 J21.31 RP29.7	::1100:3200			
TERM_M_ADDR<2>	100000000::	8		RP31.1 J21.33 RP26.6	::1100:3200			
TERM_M_ADDR<3>	100000000::	8		6RP9.3 J21.30 RP26.5	::1100:3200			
TERM_M_ADDR<4>	100000000::	8		RP31.2 J21.32 RP26.8	::1100:3200			
TERM_M_ADDR<5>	100000000::	8		RP9.1 J21.34 RP26.7	::1100:3300			
TERM_M_ADDR<6>	100000000::	8		RP21.1 J21.103 RP24.6	::1100:3200			
TERM_M_ADDR<7>	100000000::	8		RP23.2 J21.104 RP24.5	::1100:3200			
TERM_M_ADDR<8>	100000000::	8		RP21.2 J21.105 RP24.8				
TERM_M_ADDR<9>	100000000::	8		RP21.3 J21.109 RP24.7				
TERM_M_ADDR<10>	100000000::	8		RP21.4 J21.111 RP22.6	::1050:3200			
TERM_M_ADDR<11>	100000000::	8		RP23.3 J21.112 RP22.7	::1100:3200			
TERM_M_ADDR<12>	100000000::	8		R540.2 J21.70 R123.1				

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CONSTRAINTS -- MEMORY PAGE 1

APPLE COMPUTER INC.	SCALE	DRAWING NUMBER	REV.
	NONE	D 051-6101	12
SHT		OF	
35		44	

8 7 6 5 4 3 2 1



AGP RELATED DOO-DAHS

CONSTRAINTS -- AGP, FIREWIRE, PARTIAL GRAPHICS (1 OF 2)

Table with columns: SIG\_NAME, PULSE\_PARAM / MAX VIA COUNT, MAX\_EXPOSED\_LENGTH / STUB\_LENGTH, NET\_SCHED, NET\_SPACING\_TYPE, DELAY\_RULE, MIN\_LINE\_WIDTH. Includes rows for AGP signals like PANGEA\_AGP\_CLK, AGP\_CLK, AGP\_FB\_IN, AGP\_FB\_OUT, and various AGPCBE and AGPAD signals.

FIREWIRE RELATED DOO-DAHS

Table with columns: SIG\_NAME, PULSE\_PARAM / MAX VIA COUNT, MAX\_EXPOSED\_LENGTH, STUB\_LENGTH, NET\_SPACING\_TYPE, DELAY\_RULE. Includes rows for FIREWIRE signals like FW\_XI, FW\_XO, FW\_SCLK, FW\_PHY\_SCLK, FW\_LINK D<7>, FW\_LINK D<6>, FW\_LINK D<5>, FW\_LINK D<4>, FW\_LINK D<3>, FW\_LINK D<2>, FW\_LINK D<1>, FW\_LINK D<0>, FW\_LINK\_CNTL0, FW\_LINK\_CNTL1, FW\_LINK\_LREQ, FW D<7>, FW D<6>, FW D<5>, FW D<4>, FW D<3>, FW D<2>, FW D<1>, FW D<0>, FW\_CNTL0, FW\_CNTL1, FW\_LREQ, FW\_PHY D<7>, FW\_PHY D<6>, FW\_PHY D<5>, FW\_PHY D<4>, FW\_PHY D<3>, FW\_PHY D<2>, FW\_PHY D<1>, FW\_PHY D<0>, FW\_PHY\_CNTL1, FW\_PHY\_CNTL0.

FIREWIRE DIFFERENTIAL THINGIES

Table with columns: SIG\_NAME, PULSE\_PARAM / MAX VIA COUNT, MAX\_EXPOSED\_LENGTH, NET\_SPACING\_TYPE, ECL, DIFFERENTIAL\_PAIR. Includes rows for differential pairs like FW\_TPB2P, FW\_TPB2N, FW\_TPB2X, FW\_TPA2P, FW\_TPA2N, FW\_TPA2X, FW\_TPB1P, FW\_TPB1N, FW\_TPB1X, FW\_TPA1P, FW\_TPA1N, FW\_TPA1X, FW\_TPI2P, FW\_TPI2N, FW\_TPI2X, FW\_TPO2P, FW\_TPO2N, FW\_TPO2X, FW\_TPI1P, FW\_TPI1N, FW\_TPI1X, FW\_TPO1P, FW\_TPO1N, FW\_TPO1X.

GRAPHICS DIFFERENTIAL THINGIES

Table with columns: SIG\_NAME, PULSE\_PARAM / MAX VIA COUNT, MAX\_EXPOSED\_LENGTH, NET\_SPACING\_TYPE, ECL, DIFFERENTIAL\_PAIR, DELAY\_RULE, RATSNET\_SCHEDULE. Includes rows for graphics signals like INT\_TMDS D2P, INT\_TMDS D2M, INT\_TMDS D1P, INT\_TMDS D1M, INT\_TMDS D0P, INT\_TMDS D0M, INT\_TMDS CKP, INT\_TMDS CKM, FBCLKOP, FBCLKOM, TERM\_FBCLKOP, TERM\_FBCLKOM.

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D 051-6101 12
SCALE NONE SHT 37 OF 44

CONSTRAINTS -- GRAPHICS (2 OF 2)

GRAPHICS RELATED DOO-DAHS

MORE GRAPHICS RELATED DOO-DAHS

Table with columns: SIG\_NAME, PULSE\_PARAM / MAX VIA COUNT, MAX\_EXPOSED\_LENGTH / STUB\_LENGTH, RATSNET\_SCHEDULE, NET\_SPACING\_TYPE, DELAY\_RULE. Lists various signal constraints like GRAPH\_XTALIN, FBD<63>, etc.

Table with columns: SIG\_NAME, PULSE\_PARAM / MAX VIA COUNT, RATSNET\_SCHEDULE, STUB\_LENGTH, NET\_SPACING\_TYPE, DELAY\_RULE. Lists various signal constraints like FBA<13>, FBA<12>, etc.

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8 7 6 5 4 3 2 1

SIG_NAME	PULSE_PARAM	MAX_EXPOSED_LENGTH	ECL	DIFFERENTIAL_PAIR	MAX_VIA_COUNT	STUB_LENGTH	DELAY_RULE	NET_SPACING_TPYE
UIDE_DA<0>	66MHZ				6		::5170:6000	10 MIL SPACING
UIDE_DA<1>	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_DA<2>	66MHZ				6		::5170:6100	10 MIL SPACING
UIDE_DSTR_RDY	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_CS0_L	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_CS1_L	66MHZ				6		::5000:6700	10 MIL SPACING
UIDE_RESET_L	66MHZ				6		::1600:2000	10 MIL SPACING
UIDE_STOP	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_HSTR_RDY	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_DMAACK_L	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_DMAREQ	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_IRQ	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_D<0>	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_D<1>	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_D<2>	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_D<3>	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_D<4>	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_D<5>	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_D<6>	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_D<7>	66MHZ				6		U6.J30:RP25.4:5170:5920	10 MIL SPACING
UIDE_D<8>	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_D<9>	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_D<10>	66MHZ				6		::5000:5920	10 MIL SPACING
UIDE_D<11>	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_D<12>	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_D<13>	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_D<14>	66MHZ				6		::5130:5920	10 MIL SPACING
UIDE_D<15>	66MHZ				6		::5170:5920	10 MIL SPACING
T_UIDE_RESET_L	66MHZ				6	100	R141.2:J14.1:3508:3858	10 MIL SPACING
L1_TXCLK	2.5MHZ,25MHZ				4	100	::300:500	10 MIL SPACING
L1_RXCLK	2.5MHZ,25MHZ				4		::300:500	10 MIL SPACING
MII_TX_CLK	2.5MHZ,25MHZ				4	100	:::6000	10 MIL SPACING
MII_RX_CLK	2.5MHZ,25MHZ	250			4	100	:::6000	10 MIL SPACING
TPFOP	10MHZ,100MHZ	200			2	100		10 MIL SPACING
TPFON	10MHZ,100MHZ	202			2	100		10 MIL SPACING
TPFIP	10MHZ,100MHZ	200			2	100		10 MIL SPACING
TPFIN	10MHZ,100MHZ	225			2	100		10 MIL SPACING
TPFIP2	10MHZ,100MHZ	900			2	100		10 MIL SPACING
TPFIN2	10MHZ,100MHZ	400			2	100		10 MIL SPACING
TXP	10MHZ,100MHZ				2	100		
TXN	10MHZ,100MHZ				2	100		
RXP	10MHZ,100MHZ				2	100		
RXN	10MHZ,100MHZ				2	100		
TXCT	10MHZ,100MHZ				2	100		
RXCT	10MHZ,100MHZ				2	100		
ETH_XI	25MHZ	250			3	100	:::1500	10 MIL SPACING
ETH_XO	25MHZ	250			3	100	:::1500	10 MIL SPACING
PAN_XI	18.432MHZ				3		:::1100	10 MIL SPACING
PAN_XO	18.432MHZ	250			2	100	:::1000	10 MIL SPACING
PAN_XT	18.432MHZ				2		:::500	10 MIL SPACING
PMU_XO	10MHZ	250			2	100	:::1000	10 MIL SPACING
PMU_XI	10MHZ				2	100	:::1000	10 MIL SPACING
PMU_XT	10MHZ				2	100	:::1000	10 MIL SPACING
PMU_CLKOUT	0.032768MHZ	250			2	100	:::1000	10 MIL SPACING
PMU_CLKIN	0.032768MHZ				2	100	:::1000	10 MIL SPACING
PMU_CLKT	0.032768MHZ	250			2	100	:::1000	10 MIL SPACING

2KV\_ISO == 100MIL SPACING

### CONSTRAINTS -- MISCELLANEOUS

SIG_NAME	ECL
USB_DCM	TRUE
USB_DCP	TRUE
USB_DAM	TRUE
USB_DAP	TRUE
USB_DBM	TRUE
USB_DBP	TRUE
USB_DCM_F	TRUE
USB_DCP_F	TRUE
USB_DAM_F	TRUE
USB_DAP_F	TRUE
USB_DBM_F	TRUE
USB_DBP_F	TRUE
USB_DCM_EMI	TRUE
USB_DCP_EMI	TRUE
USB_DAM_EMI	TRUE
USB_DAP_EMI	TRUE
USB_DBM_EMI	TRUE
USB_DBP_EMI	TRUE

SIG_NAME	NET_SCHED
IODATA<0>	U6.P34 R138.2 R137.1 U7.25 J22.30
IODATA<1>	U6.R32 R143.2 R142.1 U7.26 J22.31
IODATA<2>	U6.T29 R150.2 R149.1 U7.27 J22.32
IODATA<3>	U6.T28 R145.2 R140.1 U7.28 J22.2
IODATA<4>	U6.R33 R156.2 R151.1 U7.32 J22.3
IODATA<5>	U6.R34 R139.2 R144.1 U7.33 J22.4
IODATA<6>	U6.U29 R165.2 R162.1 U7.34 J22.5
IOADDR<7>	U6.T33 U7.35 J22.6
IOADDR<0>	U6.N28 U7.21 J22.29
IOADDR<1>	U6.J34 U7.20 J22.28
IOADDR<2>	U6.M30 U7.19 J22.27
IOADDR<3>	U6.L32 U7.18 J22.26
IOADDR<4>	U6.K34 U7.17 J22.25
IOADDR<5>	U6.L33 U7.16 J22.24
IOADDR<6>	U6.N29 U7.15 J22.23
IOADDR<7>	U6.M32 U7.14 J22.22
IOADDR<8>	U6.L34 U7.8 J22.12
IOADDR<9>	U6.P28 U7.7 J22.11
IOADDR<10>	U6.M33 U7.36 J22.8
IOADDR<11>	U6.P29 U7.6 J22.10
IOADDR<12>	U6.M34 U7.5 J22.21
IOADDR<13>	U6.P30 U7.4 J22.13
IOADDR<14>	U6.N33 U7.3 J22.14
IOADDR<15>	U6.R28 U7.2 J22.20
IOADDR<16>	U6.P32 U7.1 J22.19
IOADDR<17>	U6.N34 U7.40 J22.46
IOADDR<18>	U6.R29 U7.13 J22.47
IOADDR<19>	U6.P33 U7.37 J22.48
IOADDR<20>	U6.R30 U7.38 J22.49

SIG_NAME	NET_SCHED
CB_CE2*	U6.W28 RP10.4 J22.42
CB_CE1*	U6.W29 RP10.3 J22.7
CB_IORD*	U6.W33 RP10.1 J22.44
CB_IOWR*	U6.W34 RP10.2 J22.45
CB_IRQ*	U6.A32 R178.1 J22.16
CB_REG*	U6.B31 R136.1 J22.61
CB_RESET	U6.AE33 R168.2 J22.58
CB_WAIT*	U6.Y34 R148.1 J22.59
CSWE*	U6.V29 RP12.2 J22.15
CSOE*	U6.Y33 RP12.1 J22.9

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6101	12
SCALE	SHT OF		
NONE	39 OF		44

8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1

SIG_NAME	PULSE_PARAM	MAX_VIA_COUNT	NET_SCHED	DELAY_RULE	STUB_LENGTH	NET_SPACING_TYPE
VGER_L3D<0>	200MHZ	4		::1200:2500	100	4
VGER_L3D<1>	200MHZ	4		::1200:2500	100	4
VGER_L3D<2>	200MHZ	4		::1200:2500	100	4
VGER_L3D<3>	200MHZ	4		::1200:2500	100	4
VGER_L3D<4>	200MHZ	4		::1200:2500	100	4
VGER_L3D<5>	200MHZ	4		::1200:2500	100	4
VGER_L3D<6>	200MHZ	4		::1200:2500	100	4
VGER_L3D<7>	200MHZ	4		::1200:2500	100	4
VGER_L3D<8>	200MHZ	4		::1200:2500	100	4
VGER_L3D<9>	200MHZ	4		::1200:2500	100	4
VGER_L3D<10>	200MHZ	4		::1200:2500	100	4
VGER_L3D<11>	200MHZ	4		::1200:2500	100	4
VGER_L3D<12>	200MHZ	4		::1200:2500	100	4
VGER_L3D<13>	200MHZ	4		::1200:2500	100	4
VGER_L3D<14>	200MHZ	4		::1200:2500	100	4
VGER_L3D<15>	200MHZ	4		::1200:2500	100	4
VGER_L3D<16>	200MHZ	4		::1200:2500	100	4
VGER_L3D<17>	200MHZ	4		::1200:2500	100	4
VGER_L3D<18>	200MHZ	4		::1200:2500	100	4
VGER_L3D<19>	200MHZ	4		::1200:2500	100	4
VGER_L3D<20>	200MHZ	4		::1200:2500	100	4
VGER_L3D<21>	200MHZ	4		::1200:2500	100	4
VGER_L3D<22>	200MHZ	4		::1200:2500	100	4
VGER_L3D<23>	200MHZ	4		::1200:2500	100	4
VGER_L3D<24>	200MHZ	4		::1200:2500	100	4
VGER_L3D<25>	200MHZ	4		::1200:2500	100	4
VGER_L3D<26>	200MHZ	4		::1200:2500	100	4
VGER_L3D<27>	200MHZ	4		::1200:2500	100	4
VGER_L3D<28>	200MHZ	4		::1200:2500	100	4
VGER_L3D<29>	200MHZ	4		::1200:2500	100	4
VGER_L3D<30>	200MHZ	4		::1200:2500	100	4
VGER_L3D<31>	200MHZ	4		::1200:2500	100	4
VGER_L3D<32>	200MHZ	4		::1200:2500	100	4
VGER_L3D<33>	200MHZ	4		::1200:2500	100	4
VGER_L3D<34>	200MHZ	4		::1200:2500	100	4
VGER_L3D<35>	200MHZ	4		::1200:2500	100	4
VGER_L3D<36>	200MHZ	4		::1200:2500	100	4
VGER_L3D<37>	200MHZ	4		::1200:2500	100	4
VGER_L3D<38>	200MHZ	4		::1200:2500	100	4
VGER_L3D<39>	200MHZ	4		::1200:2500	100	4
VGER_L3D<40>	200MHZ	4		::1200:2500	100	4
VGER_L3D<41>	200MHZ	4		::1200:2500	100	4
VGER_L3D<42>	200MHZ	4		::1200:2500	100	4
VGER_L3D<43>	200MHZ	4		::1200:2500	100	4
VGER_L3D<44>	200MHZ	4		::1200:2500	100	4
VGER_L3D<45>	200MHZ	4		::1200:2500	100	4
VGER_L3D<46>	200MHZ	4		::1200:2500	100	4
VGER_L3D<47>	200MHZ	4		::1200:2500	100	4
VGER_L3D<48>	200MHZ	4		::1200:2500	100	4
VGER_L3D<49>	200MHZ	4		::1200:2500	100	4
VGER_L3D<50>	200MHZ	4		::1200:2500	100	4
VGER_L3D<51>	200MHZ	4		::1200:2500	100	4
VGER_L3D<52>	200MHZ	4		::1200:2500	100	4
VGER_L3D<53>	200MHZ	4		::1200:2500	100	4
VGER_L3D<54>	200MHZ	4		::1200:2500	100	4
VGER_L3D<55>	200MHZ	4		::1200:2500	100	4
VGER_L3D<56>	200MHZ	4		::1200:2500	100	4
VGER_L3D<57>	200MHZ	4		::1200:2500	100	4
VGER_L3D<58>	200MHZ	4		::1200:2500	100	4
VGER_L3D<59>	200MHZ	4		::1200:2500	100	4
VGER_L3D<60>	200MHZ	4		::1200:2500	100	4
VGER_L3D<61>	200MHZ	4		::1200:2500	100	4
VGER_L3D<62>	200MHZ	4		::1200:2500	100	4
VGER_L3D<63>	200MHZ	4		::1200:2500	100	4

SIG_NAME	PULSE_PARAM	MAX_VIA_COUNT	MIN_LIN_WIDTH	DELAY_RULE	STUB_LENGTH	NET_SPACING_TYPE
VGER_L3A<0>	200MHZ	4		::2500:2800	100	4
VGER_L3A<1>	200MHZ	4		::2500:2800	100	4
VGER_L3A<2>	200MHZ	4		::2500:2800	100	4
VGER_L3A<3>	200MHZ	4		::2500:2800	100	4
VGER_L3A<4>	200MHZ	4		::2500:2800	100	4
VGER_L3A<5>	200MHZ	4		::2500:2800	100	4
VGER_L3A<6>	200MHZ	4		::2500:2800	100	4
VGER_L3A<7>	200MHZ	4		::2500:2800	100	4
VGER_L3A<8>	200MHZ	4		::2500:2800	100	4
VGER_L3A<9>	200MHZ	4		::2500:2800	100	4
VGER_L3A<10>	200MHZ	4		::2500:2800	100	4
VGER_L3A<11>	200MHZ	4		::2500:2800	100	4
VGER_L3A<12>	200MHZ	4		::2500:2800	100	4
VGER_L3A<13>	200MHZ	4		::2500:2800	100	4
VGER_L3A<14>	200MHZ	4		::2500:2800	100	4
VGER_L3A<15>	200MHZ	4		::2500:2800	100	4
VGER_L3A<16>	200MHZ	4		::2500:2800	100	4
VGER_L3A<17>	200MHZ	4		::2500:2800	100	4
VGER_L3CLK<0>	200MHZ	4		::2345:2355	100	4
VGER_L3CLK<1>	200MHZ	4		::2345:2355	100	4
VGER_L3CF*	200MHZ	4		::2500:2800	100	4
VGER_L3WE*	200MHZ	4		::2500:2800	100	4
VGER_L3RCLK<0>	200MHZ	4		::2545:2555	100	4
VGER_L3RCLK<1>	200MHZ	4		::2545:2555	100	4
VGER_L3RCLK<2>	200MHZ	4		::2545:2555	100	4
VGER_L3RCLK<3>	200MHZ	4		::2545:2555	100	4
L3 VREF<0>			10			4 20
L3 VREF<1>			10			4 20

D

D

C

C

B

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A

A

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CONSTRAINTS -- L3

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	D	051-6101	12
SCALE	NONE	SHT	OF
		40	44

8 7 6 5 4 3 2 1



8			7			6			5			4			3			2			1		
D	BT1	23	BATTERY	C95	10	CAP	C190	4	CAP	C285	32	CAP	C380	32	CAP								
	C1	19	CAP_P	C96	29	CAP	C191	22	CAP_P	C286	16	CAP	C381	26	CAP								
	C2	19	CAP_P	C97	31	CAP	C192	4	CAP	C287	32	CAP	C382	26	CAP								
	C3	25	CAP	C98	11	CAP	C193	4	CAP	C288	15	CAP	C383	31	CAP								
	C4	19	CAP_P	C99	11	CAP	C194	24	CAP	C289	15	CAP	C384	26	CAP								
	C5	25	CAP	C100	10	CAP	C195	4	CAP	C290	16	CAP	C385	26	CAP								
	C6	16	CAP	C101	10	CAP	C196	4	CAP	C291	15	CAP	C386	22	CAP								
	C7	16	CAP	C102	10	CAP	C197	22	CAP_P	C292	9	CAP	C387	26	CAP								
	C8	16	CAP	C103	9	CAP	C198	24	CAP	C293	9	CAP	C388	32	CAP								
	C9	16	CAP	C104	9	CAP	C199	27	CAP	C294	15	CAP	C389	22	CAP								
	C10	25	CAP	C105	9	CAP	C200	27	CAP	C295	16	CAP	C390	32	CAP								
	C11	25	CAP	C106	9	CAP	C201	21	CAP_P	C296	16	CAP	C391	26	CAP								
	C12	16	CAP	C107	9	CAP	C202	21	CAP_P	C297	15	CAP	C392	26	CAP								
	C13	16	CAP	C108	10	CAP	C203	22	CAP	C298	15	CAP	C393	26	CAP								
	C14	16	CAP	C109	10	CAP	C204	4	CAP	C299	18	CAP	C394	31	CAP								
	C15	16	CAP	C110	10	CAP	C205	4	CAP	C300	15	CAP	C395	31	CAP								
	C16	15	CAP	C111	29	CAP	C206	22	CAP_P	C301	15	CAP	C396	31	CAP								
	C17	15	CAP	C112	31	CAP	C207	22	CAP_P	C302	15	CAP	C397	26	CAP								
	C18	16	CAP	C113	11	CAP	C208	27	CAP	C303	9	CAP	C398	26	CAP								
	C19	16	CAP	C114	29	CAP	C209	27	CAP	C304	9	CAP	C399	26	CAP								
	C20	16	CAP	C115	29	CAP	C210	27	CAP	C305	16	CAP	C400	18	CAP								
	C21	16	CAP	C116	29	CAP	C211	21	CAP_P	C306	15	CAP	C401	7	CAP								
	C22	16	CAP	C117	32	CAP_P	C212	21	CAP_P	C307	9	CAP	C402	26	CAP								
	C23	16	CAP	C118	22	CAP_P	C213	4	CAP_P	C308	9	CAP	C403	26	CAP								
	C24	16	CAP	C119	22	CAP_P	C214	27	CAP	C309	15	CAP	C404	29	CAP								
	C25	16	CAP	C120	22	CAP_P	C215	27	CAP	C310	15	CAP	C405	8	CAP								
	C26	16	CAP	C121	31	CAP	C216	27	CAP	C311	22	CAP	C406	8	CAP								
	C27	16	CAP	C122	31	CAP	C217	27	CAP	C312	32	CAP	C407	8	CAP								
	C28	16	CAP	C123	32	CAP_P	C218	27	CAP	C313	15	CAP	C408	26	CAP								
	C29	16	CAP_P	C124	6	CAP	C219	27	CAP	C314	15	CAP	C409	14	CAP								
	C30	22	CAP_P	C125	29	CAP_P	C220	22	CAP	C315	15	CAP	C410	14	CAP								
	C31	28	CAP_P	C126	29	CAP	C221	4	CAP	C316	22	CAP_P	C411	14	CAP								
	C32	25	CAP	C127	29	CAP_P	C222	4	CAP	C317	22	CAP_P	C412	14	CAP								
	C33	25	CAP	C128	22	CAP_P	C223	4	CAP	C318	32	CAP	C413	14	CAP								
	C34	16	CAP	C129	22	CAP_P	C224	22	CAP	C319	16	CAP	C414	14	CAP								
	C35	16	CAP_P	C130	30	CAP	C225	4	CAP	C320	16	CAP	C415	14	CAP								
	C36	11	CAP	C131	28	CAP	C226	4	CAP	C321	16	CAP	C416	14	CAP								
	C37	11	CAP	C132	29	CAP	C227	4	CAP	C322	15	CAP	C417	14	CAP								
	C38	11	CAP	C133	22	CAP_P	C228	4	CAP	C323	15	CAP	C418	14	CAP								
	C39	11	CAP	C134	28	CAP	C229	27	CAP	C324	22	CAP	C419	14	CAP								
	C40	11	CAP	C135	22	CAP	C230	27	CAP	C325	16	CAP	C420	14	CAP								
	C41	12	CAP	C136	28	CAP_P	C231	4	CAP	C326	32	CAP	C421	14	CAP								
	C42	11	CAP	C137	22	CAP	C232	21	CAP_P	C327	32	CAP	C422	14	CAP								
	C43	11	CAP	C138	26	CAP_P	C233	27	CAP	C328	11	CAP	C423	14	CAP								
	C44	10	CAP	C139	26	CAP	C234	22	CAP	C329	32	CAP	C424	14	CAP								
	C45	16	CAP	C140	26	CAP	C235	19	CAP	C330	11	CAP	C425	14	CAP								
	C46	10	CAP	C141	8	CAP	C236	19	CAP	C331	30	CAP	C426	14	CAP								
	C47	9	CAP	C142	8	CAP	C237	19	CAP	C332	11	CAP	C427	14	CAP								
	C48	9	CAP	C143	26	CAP	C238	19	CAP	C333	11	CAP	C428	14	CAP								
	C49	9	CAP	C144	26	CAP	C239	16	CAP	C334	32	CAP	C429	14	CAP								
	C50	9	CAP	C145	23	CAP	C240	19	CAP	C335	32	CAP	C430	14	CAP								
	C51	9	CAP	C146	23	CAP	C241	19	CAP	C336	6	CAP	C431	14	CAP								
	C52	9	CAP	C147	27	CAP	C242	32	CAP	C337	30	CAP	C432	14	CAP								
	C53	9	CAP	C148	28	CAP	C243	19	CAP	C338	30	CAP	C433	14	CAP								
	C54	9	CAP	C149	23	CAP_P	C244	19	CAP	C339	11	CAP	C434	14	CAP								
	C55	12	CAP	C150	23	CAP	C245	19	CAP	C340	11	CAP	C436	14	CAP								
	C56	30	CAP_P	C151	23	CAP	C246	16	CAP	C341	32	CAP	C437	14	CAP								
	C57	30	CAP_P	C152	28	CAP_P	C247	16	CAP	C342	31	CAP	C438	14	CAP								
	C58	10	CAP	C153	28	CAP	C248	19	CAP	C343	11	CAP	C439	14	CAP								
	C59	9	CAP	C154	22	CAP	C249	19	CAP	C344	29	CAP	C440	14	CAP								
	C60	12	CAP	C155	22	CAP_P	C250	32	CAP	C345	29	CAP	C441	14	CAP								
	C61	12	CAP	C156	22	CAP	C251	32	CAP	C346	29	CAP	C442	14	CAP								
	C62	26	CAP_P	C157	23	CAP	C252	16	CAP	C347	12	CAP	C443	14	CAP								
	C63	11	CAP	C158	23	CAP	C253	16	CAP	C348	11	CAP	C444	14	CAP								
	C64	10	CAP	C159	27	CAP_P	C254	19	CAP	C349	30	CAP	C445	14	CAP								
	C65	9	CAP	C160	22	CAP_P	C255	25	CAP	C350	30	CAP	C446	14	CAP								
	C66	9	CAP	C161	27	CAP_P	C256	25	CAP	C351	29	CAP	C447	14	CAP								
	C67	28	CAP	C162	27	CAP_P	C257	32	CAP	C352	11	CAP	C448	8	CAP								
	C68	9	CAP	C163	22	CAP	C258	15	CAP	C353	32	CAP	C449	8	CAP								
	C69	12	CAP	C164	6	CAP	C259	25	CAP	C354	32	CAP	C450	8	CAP								
	C70	9	CAP	C165	22	CAP_P	C260	32	CAP	C355	32	CAP	C451	14	CAP								
	C71	9	CAP	C166	23	CAP	C261	32	CAP	C356	32	CAP	C452	14	CAP								
	C72	9	CAP	C167	22	CAP	C262	32	CAP	C357	30	CAP	C453	14	CAP								
	C73	11	CAP	C168	27	CAP_P	C263	30	CAP	C358	29	CAP	C454	14	CAP								
	C74	9	CAP	C169	23	CAP	C264	32	CAP	C359	11	CAP	C455	14	CAP								
	C75	9	CAP	C170	27	CAP_P	C265	19	CAP	C360	11	CAP	C456	14	CAP								
	C76	31	CAP	C171	27	CAP_P	C266	19	CAP	C361	12	CAP	C457	14	CAP								
	C77	30	CAP	C172	27	CAP_P	C267	19	CAP	C362	28	CAP	C458	8	CAP								
	C78	10	CAP	C173	27	CAP_P	C268	30	CAP	C363	26	CAP	C459	14	CAP								
	C79	9	CAP	C174	27	CAP_P	C269	30	CAP	C364	29	CAP	C460	14	CAP								
	C80	12	CAP	C175	27	CAP_P	C270	19	CAP	C365	28	CAP	C461	14	CAP								
	C81	11	CAP	C176	27	CAP_P	C271	15	CAP	C366	11	CAP	C462	14	CAP								
	C82	9	CAP	C177	22	CAP	C272	15	CAP	C367	11	CAP	C463	14	CAP								
	C83	29	CAP_P	C178	22	CAP	C273	30	CAP	C368	26	CAP	C464	14	CAP								
	C84	11	CAP	C179	27	CAP_P	C274	25	CAP	C369	29	CAP	C465	14	CAP								
	C85	11	CAP	C180	27	CAP_P	C275	30	CAP	C370	29	CAP	C466	14	CAP								
	C86	9	CAP	C181	22	CAP	C276	15	CAP	C371	11	CAP	C467	14	CAP								

8			7			6			5			4			3			2			1		
C476	14	CAP	C571	14	CAP	C667	24	CAP	D7	27	DIODE_SCHOT	L36	30	IND									
C477	14	CAP	C572	14	CAP	C668	27	CAP	D8	27	DIODE_SCHOT	L37	30	IND									
C478	14	CAP	C573	14	CAP	C669	27	CAP	D9	27	DIODE_SCHOT	L38	30	IND									
C479	14	CAP	C574	14	CAP	C670	27	CAP	D10	32	ZENER_MMBZ15VDLT1	L39	30	IND									
C480	14	CAP	C575	14	CAP	C671	24	CAP	D11	32	DIODE_SCHOT_3P	L40	30	IND									
C481	14	CAP	C576	14	CAP	C672	24	CAP	D12	30	DIODE_SCHOT_3P	L41	15	IND									
C482	14	CAP	C577	5	CAP	C673	24	CAP	D13	16	DIODE	L42	15	IND									
C483	14	CAP	C578	14	CAP	C674	24	CAP	D14	22	DIODE_SCHOT	L43	26	IND									
C484	14	CAP	C579	14	CAP	C675	24	CAP	D15	22	DIODE_SCHOT	L44	26	IND									
C485	14	CAP	C580	14	CAP	C676	24	CAP	D16	22	DIODE_SCHOT	L45	25	IND									
C486	14	CAP	C581	14	CAP	C677	24	CAP	D17	22	DIODE_SCHOT	L46	16	IND									
C487	14	CAP	C582	18	CAP	C678	24	CAP	D18	22	DIODE_SCHOT	L47	31	IND									
C488	14	CAP	C583	14	CAP	C679	27	CAP	D19	22	DIODE_SCHOT	L48	31	IND									
C489	14	CAP	C584	14	CAP	C680	4	CAP	D20	27	DIODE_SCHOT	L49	31	IND									
C490	14	CAP	C585	14	CAP	C681	24	CAP	D21	27	DIODE_SCHOT	L50	29	IND									
C491	14	CAP	C586	5	CAP	C682	24	CAP	D22	22	DIODE_SCHOT	L51	26	IND									
C492	14	CAP	C587	18	CAP	C683	4	CAP	DS1	28	LED	L52	31	IND									
C493	14	CAP	C588	18	CAP	C684	4	CAP	DS2	26	LED	L53	31	IND									
C494	14	CAP	C589	5	CAP	C685	24	CAP	DS3	28	LED	L54	29	IND									
C495	14	CAP	C590	26	CAP	C686	27	CAP	DS4	15	LED	L55	26	IND									
C496	14	CAP	C591	26	CAP	C687	27	CAP	DS5	15	LED	L56	26	IND									
C497	14	CAP	C592	22	CAP	C688	24	CAP	DS6	15	LED	L57	26	IND									
C498	14	CAP	C593	6	CAP	C689	4	CAP	DS7	6	LED	L58	26	IND									
C499	14	CAP	C595	26	CAP	C690	4	CAP	F1	16	FUSE	L59	18	IND									
C500	14	CAP	C596	26	CAP	C691	4	CAP	F2	19	FUSE	L60	26	IND									
C501	14	CAP	C597	23	CAP	C692	24	CAP	F3	25	FUSE	L61	31	IND									
C502	14	CAP	C598	23	CAP	C693	24	CAP	FL1	16	FILTER_CHOKE_DUAL	L62	26	IND									
C503	14	CAP	C599	22	CAP	C694	4	CAP	FL2	25	FILTER_LC	L63	26	IND									
C504	14	CAP	C600	27	CAP	C695	4	CAP	FL3	16	FILTER_CHOKE_DUAL	L64	26	IND									
C505	14	CAP	C601	27	CAP	C696	24	CAP	FL4	25	FILTER_LC	L65	26	IND									
C506	14	CAP	C602	27	CAP	C697	4	CAP	FL5	25	FILTER_LC	L66	26	IND									
C507	14	CAP	C603	27	CAP	C698	4	CAP	FL6	19	FILTER_12P	L67	26	IND									
C508	14	CAP	C604	27	CAP	C699	24	CAP	FL7	32	FILTER_12P	L68	7	IND									
C509	14	CAP	C605	27	CAP	C700	27	CAP	J1	15	CON_RJ45	L69	7	IND									
C510	14	CAP	C606	22	CAP	C701	27	CAP	J2	19	CON_F4RT_USB_UPRIGHT	Q1	30	TRA_2N3904									
C511	14	CAP	C607	24	CAP	C702	27	CAP	J3	19	CON_F4RT_USB_UPRIGHT	Q2	30	TRA_2N3904									
C512	14	CAP	C608	22	CAP	C703	27	CAP	J4	16	CON_FWVERT_SKT	Q3	16	TRA_2N3904									
C513	14	CAP	C609	24	CAP	C704	27	CAP	J5	19	CON_F4RT_USB_UPRIGHT	Q4	30	TRA_2N3906									
C514	14	CAP	C610	24	CAP	C705	4	CAP	J6	16	CON_FWVERT_SKT	Q5	30	TRA_2N7002									
C515	14	CAP	C611	24	CAP	C706	24	CAP	J7	32	CON_F8RT_S_TH1	Q6	28	TRA_2N7002									
C516	14	CAP	C612	24	CAP	C707	24	CAP	J8	25	CON_F14RT_D4MT_TH1	Q7	28	TRA_SI3443DV									
C517	14	CAP	C613	24	CAP	C708	24	CAP	J9	30	CON_F5RT_S_2MT_TH1	Q8	28	TRA_2N7002									
C518	14	CAP	C614	24	CAP	C709	21	CAP	J10	25	CON_F21RT_S2MT_SM	Q9	28	TRA_SI3443DV									
C519	14	CAP	C615	22	CAP	C710	24	CAP	J11	13	CON_M4ST_LCK	Q10	28	TRA_2N7002									
C520	14	CAP	C616	4	CAP	C711	24	CAP	J12	26	CON_M40SM_635	Q11	27	TRA_2N7002									
C521	14	CAP	C617	3	CAP	C712	24	CAP	J13	26	CON_M26ST_SMBM	Q12	27	TRA_2N7002									
C522	14	CAP	C618	24	CAP	C713	24	CAP	J14	26	CON_M40ST_NC20	Q13	28	TRA_SI3443DV									
C523	14	CAP	C619	4	CAP	C714	20	CAP	J15	27	CON_M14ST_D_TH	Q14	27	TRA_2N7002									
C524	22	CAP	C620	4	CAP	C715	4	CAP	J17	28	CON_M12ST_SM	Q15	28	TRA_2N7002									
C525	14	CAP	C621	4	CAP	C716	4	CAP	J18	22	CON_M3ST_LCK	Q16	22	TRA_2N7002									
C526	14	CAP	C622	4	CAP	C717	26	CAP	J19	6	CON_168ST_UDRM	Q17	27	TRA_2N3904									
C527	14	CAP	C623	4	CAP	C718	4	CAP	J20	24	CON_F20SM_KX	Q18	23	TRA_2N3904									
C528	14	CAP	C624	4	CAP	C719	4	CAP	J21	6	CON_144_33SM72	Q19	27	TRA_IRF7805									
C529	14	CAP	C625	3	CAP	C720	20	CAP	J22	26	CON_68_FCMCIA_FOXCN	Q20	27	TRA_2N7002									
C530	6	CAP	C626	3	CAP	C721	22	CAP	J23	24	CON_F140SM_BTBC	Q21	9	TRA_2N3904									
C531	6	CAP	C627	24	CAP	C722	22	CAP	J24	26	CON_M2SM_DF13	Q22	32	TRA_2N7002									
C532	14	CAP	C628	24	CAP	C723	22	CAP	J25	21	CON_M6ST_BTRY	Q23	28	TRA_SI3443DV									
C533	14	CAP	C629	22	CAP	C724	22	CAP_P	J26	7	CON_F1ST_S2MT_SM	Q24	32	TRA_2N7002									
C534	18	CAP	C630	24	CAP	C725	7	CAP	J27	18	CON_F1ST_S2MT_SM	Q25	28	TRA_2N7002									
C535	14	CAP	C631	24	CAP	C726	7	CAP	J28	3	CON_F12RT_S2MT_SM	Q26	32	TRA_2N7002									
C536	14	CAP	C632	22	CAP	C727	7	CAP	L1	16	IND	Q27	28	TRA_2N7002									
C537	14	CAP	C633	21	CAP	C728	7	CAP	L2	16	IND	Q28	28	TRA_2N7002									
C538	14	CAP	C634	21	CAP	C729	7	CAP	L3	25	IND	Q29	27	TRA_IRF7805									
C539	14	CAP	C635	24	CAP	C730	7	CAP	L4	32	IND	Q30	22	TRA_IRF7822									
C540	18	CAP	C636	24	CAP	C731	7	CAP	L5	32	IND	Q31	27	TRA_IRF7805									
C541	14	CAP	C637	22	CAP	C732	7	CAP	L6	9	IND	Q32	27	TRA_IRF7805									
C542	14	CAP	C638	4	CAP	C733	7	CAP	L7	32	IND	Q33	22	TRA_IRF7822									
C543	14	CAP	C639	4	CAP	C734	7	CAP	L8	32	IND	Q34	27	TRA_IRF7805									
C544	14	CAP	C640	24	CAP	C735	7	CAP	L9	29	IND	Q35	22	TRA_IRF7822									
C545	14	CAP	C641	24	CAP	C736	7	CAP	L10	29	IND	Q36	21	TRA_2N7002									
C546	14	CAP	C642	4	CAP	C737	7	CAP	L11	29	IND	Q37	21	TRA_2N7002									
C547	14	CAP	C643	27	CAP	C738	7	CAP	L12	32	IND	Q38	22	TRA_IRF7822									
C548	14	CAP	C644	27	CAP	C739	7	CAP	L13	27	IND	R1	15	RES									
C549	14	CAP	C645	24	CAP	C740	7	CAP	L14	27	IND	R2	15	RES									
C550	14	CAP	C646	24	CAP	C741	7	CAP	L15	27	IND	R3	15	RES									
C551	14	CAP	C647	24	CAP	C742	31	CAP	L16	13	IND	R4	15	RES									
C552	14	CAP	C648	24	CAP	C743	31	CAP	L17	27	IND_3P	R5	15	RES									
C553	14	CAP	C649	24	CAP	C744	31	CAP_P	L18	27	IND_3P	R6	15	RES									
C554	14	CAP	C650	24	CAP	C745	21	CAP	L19	22	IND	R7	30	RES									
C555	17	CAP	C651	24	CAP	C746	21	CAP	L20	32	IND	R8	15	RES									
C556	14	CAP	C652	24	CAP	C748	23	CAP	L21	32	IND	R9	15	RES									
C557	14	CAP	C653	24	CAP	C751	19	CAP	L22	30	IND	R10	18	RES									
C558	14	CAP	C654	24	CAP	C752	22	CAP	L23	30	IND	R11	16	RES									
C559	14	CAP	C655	24	CAP	C753	22	CAP	L24	30	IND	R12	16	RES									
C560	14	CAP	C656	24	CAP	C754	22	CAP	L25	19	IND	R13	16	RES									
C561	14	CAP	C657	24	CAP	C755	28	CAP	L26	19	IND	R14	16	RES									
C562	14	CAP	C658	24	CAP	C756	28	CAP	L27	19	IND	R15	16	RES									
C563	14	CAP	C659	24	CAP	C757	28	CAP	L28	19	IND	R16	15	RES									
C564	14	CAP	C660	24	CAP	C758	28	CAP_P	L29	19	IND	R17	15	RES									
C565	14	CAP	C661	24	CAP	D1	9	DIODE_SCHOT	L30	30	IND	R18	25	RES									
C566	14	CAP	C662	24	CAP	D2	16	DIODE_SCHOT	L31	19	IND	R19	25	RES									
C567	14	CAP	C663	24	CAP	D3	23	DIODE_SCHOT	L32	30	IND	R20	25	RES									
C568	14	CAP	C664	24	CAP	D4	23	DIODE_SCHOT	L33	32	IND	R21	25	RES									
C569	14	CAP	C665	22	CAP_P	D5	23	DIODE_SCHOT	L34	32	IND	R22	25	RES									
C570	14	CAP	C666	22	CAP_P	D6	23	DIODE_SCHOT	L35	25	IND	R23	25	RES									

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	?	?
SCALE	NONE	SHT	OF
		?	?

8			7			6			5			4			3			2			1		
R24	25	RES	R119	8	RES	R214	20	RES	R309	27	RES	R404	9	RES									
R25	25	RES	R120	13	RES	R215	5	RES	R310	27	RES	R405	22	RES									
R26	25	RES	R121	20	RES	R216	23	RES	R311	20	RES	R406	12	RES									
R27	25	RES	R122	30	RES	R217	23	RES	R312	20	RES	R407	30	RES									
R28	25	RES	R123	8	RES	R218	28	RES	R313	27	RES	R408	30	RES									
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R35	16	RES	R130	30	RES	R225	5	RES	R320	16	RES	R415	30	RES									
R36	16	RES	R131	26	RES	R226	28	RES	R321	25	RES	R416	6	RES									
R37	16	RES	R132	26	RES	R227	20	RES	R322	16	RES	R417	30	RES									
R38	15	RES	R133	26	RES	R228	22	RES	R323	16	RES	R418	30	RES									
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R104	10	RES	R199	23	RES	R294	20	RES	R389	11	RES	R484	22	RES									
R105	10	RES	R200	23	RES	R295	20	RES	R390	32	RES	R485	19	RES									
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R107	31	RES	R202	23	RES	R297	27	RES	R392	30	RES	R487	19	RES									
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R118	8	RES	R213	23	RES	R308	27	RES	R403	25	RES	R499	8	RES									

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	?	?
SCALE	SHT	OF	?
NONE	?		

	8	7	6	5	4	3	2	1				
D	R500	31	RES	R595	23	RES	R746	21	RES	U31	27	LTC1628
	R501	31	RES	R596	28	RES	R747	21	RES	U32	21	VREG_LP2951
	R502	31	RES	R597	23	RES	R748	24	RES	U33	7	CLK_GEN_IMIC5003
	R503	19	RES	R598	23	RES	R749	21	RES	U35	21	AT90S1200
	R504	19	RES	R599	22	RES	R750	21	RES	U36	21	EEPROM_256X8
	R505	19	RES	R600	22	RES	R751	21	RES	U38	19	SWI_TPS2023
	R506	13	RES	R601	28	RES	R752	21	RES	VR1	22	VREG_EZ1582
	R507	19	RES	R602	20	RES	R753	21	RES	VR2	22	VREG_EZ1582
	R508	19	RES	R603	20	RES	R754	21	RES	VR3	22	VREG_EZ1582
	R509	13	RES	R604	20	RES	R755	32	RES	VR4	21	VREG_EZ1582
	R510	31	RES	R605	27	RES	R756	32	RES	VR5	28	VREG_EZ1582
	R511	13	RES	R606	27	RES	R757	20	RES	XS1	31	STAR
	R512	18	RES	R607	27	RES	R760	22	RES	XS2	30	STAR
	R513	13	RES	R608	20	RES	R761	7	RES	XS3	29	STAR
	R514	8	RES	R609	3	RES	R762	7	RES	XS4	32	STAR
	R515	8	RES	R610	27	RES	R763	7	RES	XS5	29	STAR
	R516	8	RES	R611	3	RES	R764	18	RES	XW1	28	SHORT
	R517	8	RES	R612	22	RES	R765	18	RES	XW2	28	SHORT
	R518	8	RES	R613	22	RES	R766	18	RES	XW3	31	SHORT
	R519	24	RES	R614	21	RES	R767	22	RES	XW4	22	SHORT
	R520	24	RES	R615	20	RES	R768	22	RES	XW5	27	SHORT
	R521	26	RES	R616	20	RES	R769	22	RES	Y1	16	CRYSTAL
	R522	8	RES	R617	22	RES	R780	28	RES	Y2	15	CRYSTAL
	R523	8	RES	R618	21	RES	R781	28	RES	Y3	9	CRYSTAL
	R524	24	RES	R619	20	RES	RP1	20	RPAK4P	Y4	23	CRYSTAL
R525	24	RES	R620	21	RES	RP2	10	RPAK4P	Y5	23	CRYSTAL_4PIN	
R526	26	RES	R621	21	RES	RP3	20	RPAK4P	Y6	18	CRYSTAL	
R527	17	RES	R622	20	RES	RP4	13	RPAK4P	Y7	12	CRYSTAL	
R528	24	RES	R623	20	RES	RP5	20	RPAK4P	Y8	7	CRYSTAL	
R529	24	RES	R624	7	RES	RP6	13	RPAK4P	ZH1	33	MTGHOLE	
R530	8	RES	R625	7	RES	RP7	6	RPAK4P	ZH2	33	MTGHOLE	
R531	6	RES	R626	20	RES	RP8	20	RPAK4P	ZH3	33	MTGHOLE	
R532	7	RES	R627	7	RES	RP9	8	RPAK4P	ZH4	28	MTGHOLE	
R533	24	RES	R628	7	RES	RP10	20	RPAK4P	ZH40	26	PCB_STANDOFF	
R534	24	RES	R629	20	RES	RP11	6	RPAK4P	ZH44	26	PCB_STANDOFF	
R535	13	RES	R630	20	RES	RP12	20	RPAK4P				
R536	13	RES	R631	27	RES	RP13	20	RPAK4P				
R537	13	RES	R632	20	RES	RP14	20	RPAK4P				
R538	8	RES	R633	22	RES	RP15	20	RPAK4P				
R539	6	RES	R634	20	RES	RP16	20	RPAK4P				
R540	8	RES	R635	7	RES	RP17	20	RPAK4P				
R541	7	RES	R636	7	RES	RP18	20	RPAK4P				
R542	18	RES	R637	7	RES	RP19	15	RPAK4P				
R543	7	RES	R638	7	RES	RP20	10	RPAK4P				
R544	18	RES	R639	27	RES	RP21	8	RPAK4P				
R545	26	RES	R640	27	RES	RP22	6, 8	RPAK4P				
R546	6	RES	R641	21	RES	RP23	6, 8	RPAK4P				
R547	7	RES	R642	21	RES	RP24	8	RPAK4P				
R548	7	RES	R643	22	RES	RP25	17	RPAK4P				
R549	17	RES	R644	27	RES	RP26	8	RPAK4P				
R550	7	RES	R645	15	RES	RP27	17	RPAK4P				
R551	17	RES	R646	24	RES	RP28	6	RPAK4P				
R552	7	RES	R647	27	RES	RP29	6, 8	RPAK4P				
R553	17	RES	R648	27	RES	RP30	17	RPAK4P				
R554	18	RES	R649	27	RES	RP31	6, 8	RPAK4P				
R555	26	RES	R650	27	RES	RP32	17	RPAK4P				
R556	7	RES	R651	27	RES	RP33	8	RPAK4P				
R557	17	RES	R652	7	RES	RP34	6	RPAK4P				
R558	7	RES	R653	7	RES	RP35	7	RPAK4P				
R559	26	RES	R654	7	RES	S1	28	SWI_4RTSA1_SMB				
R560	7	RES	R655	20	RES	S2	28	SWI_4RTSA1_SMB				
R561	17	RES	R656	7	RES	S3	26	SWI_4RTSA1_SMB				
R562	5	RES	R657	7	RES	S4	23	SWI_TACT_4SM				
R563	17	RES	R667	7	RES	S5	23	SWI_TACT				
R564	5	RES	R668	7	RES	T1	15	XFR_100BT_MDIX				
R565	5	RES	R670	7	RES	U1	9	VREG_TL431				
R566	5	RES	R676	7	RES	U2	15	TRANSCEIVER_ENET_LXT971A				
R567	26	RES	R678	7	RES	U3	11	SGRAM_2MX32				
R568	18	RES	R680	7	RES	U4	32	AMP_TA2024				
R569	18	RES	R681	7	RES	U5	29	TAS3001C				
R570	5	RES	R721	20	RES	U6	5, 6, 8, 13	PANGEA				
R571	17	RES	R722	22	RES	U7	8	FEPR_1MX8				
R572	7	RES	R723	31	RES	U8	23	M16C62				
R573	26	RES	R724	31	RES	U9	7	74574				
R574	26	RES	R725	31	RES	U10	22	VREG_LP2951				
R575	20	RES	R726	31	RES	U11	23	VREG_TL431				
R576	20	RES	R727	16	RES	U12	23	VDET_MC33465N_22ATR				
R577	20	RES	R728	4	RES	U13	3, 4	SCVGER483				
R578	5	RES	R729	4	RES	U14	4	SRAM_DDR_153PBGA				
R579	5	RES	R730	4	RES	U15	23	NC7SZ04				
R580	7	RES	R731	4	RES	U16	18, 25	74125				
R581	17	RES	R732	21	RES	U17	16	FW802				
R582	17	RES	R733	21	RES	U18	16	VREG_LP2951				
R583	22	RES	R734	21	RES	U19	12	CLK_GEN_IMISM530				
R584	17	RES	R735	21	RES	U20	29, 30	OPAMP_TS924				
R585	17	RES	R736	21	RES	U21	11	SGRAM_2MX32				
R586	17	RES	R737	21	RES	U22	9, 10, 12	MONICA				
R587	23	RES	R738	21	RES	U23	29	ADDAC_TLC320AD77C				
R588	23	RES	R739	21	RES	U24	31	OPAMP_TS924				
R589	23	RES	R740	21	RES	U25	29	VREG_LP2951				
R590	28	RES	R741	21	RES	U26	29	VREG_LP2951				
R591	23	RES	R742	21	RES	U27	31	ADC_CS5331				
R592	22	RES	R743	21	RES	U28	23	MAX6328				
R593	26	RES	R744	21	RES	U29	22	SWREG_LTC1735				
R594	28	RES	R745	21	RES	U30	4	SRAM_DDR_153PBGA				

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NONE	?		