1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

10/15/2004

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
B		328536	PRODUCTION RELEASED	05/19/04	

SCHEM,SAPPHIRE,Q41B

BOM OPTIONS	STUFF	NO STUFF
D3_HOT		✓
D3_COLD	✓	
GPU_SS	✓	
GPU_SWITCH	✓	
SERIAL_DEBUG		✓
VCORE_OFFSET	✓	
1_8V_MAXBUS	✓	
1_5V_MAXBUS		✓
NEC_USB	✓	
INTREPID_USB		✓
BBANG		✓
NO_BBANG	✓	
ATI_MEMIO_HI	✓	
ATI_MEMIO_LO		✓
SSCG		✓
NO_SSCG	✓	
5V_HD_LOGIC	✓	
3V_HD_LOGIC		✓
EXT_TMDS	CTO	✓
INT_TMDS	✓	CTO
NO_4XVCORE	✓	
INT_CLK	✓	
EXT_CLK		✓

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6694	1	SCHEM,SAPPHIRE,Q41B	SCH1	
820-1688	1	PCBF,SAPPHIRE,Q41B	PCB1	

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

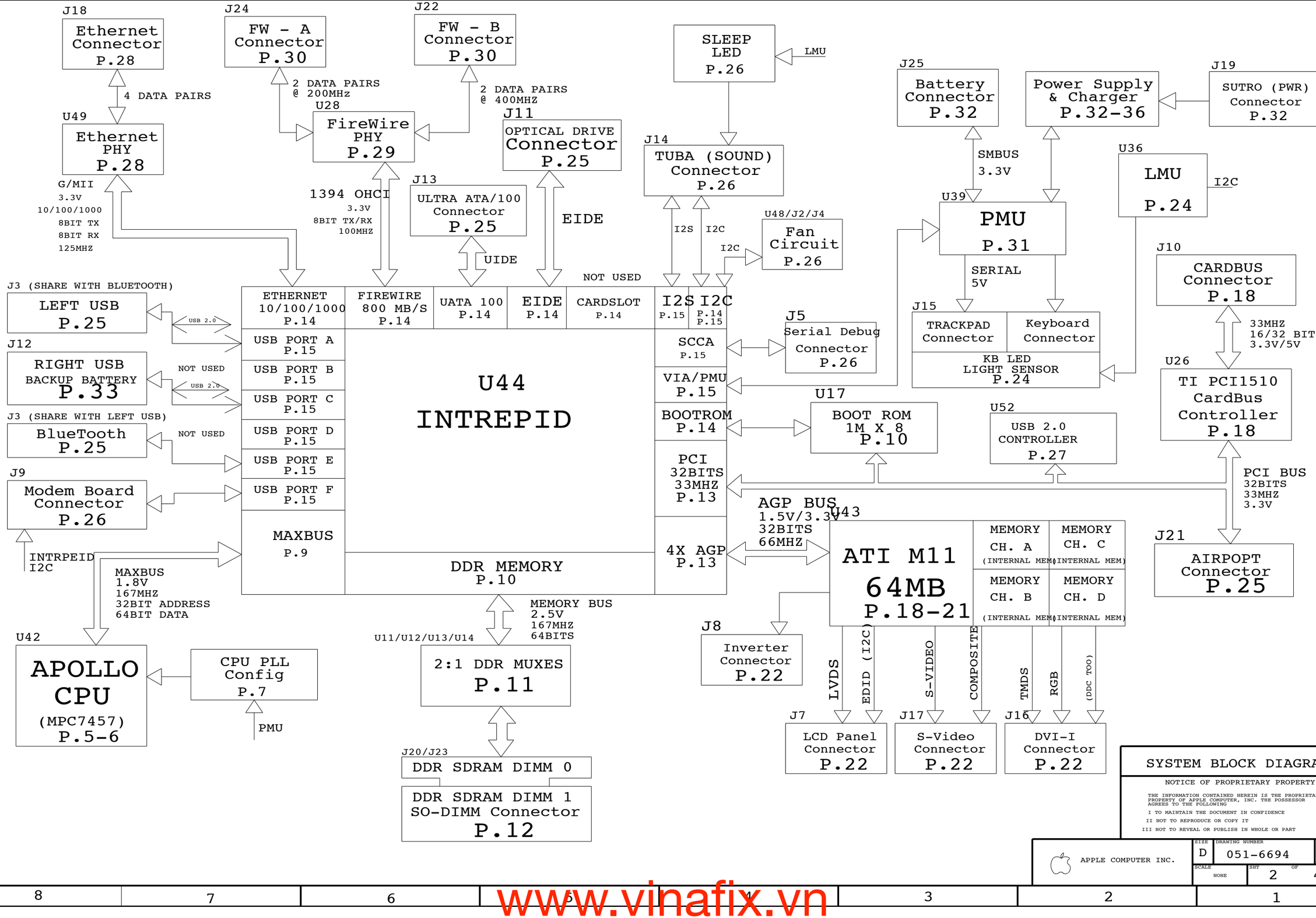
DRAFTER / DESIGN CK / ENG APPD / MFG APPD / QA APPD / DESIGNER / RELEASE / SCALE NONE
MATERIAL/FINISH NOTED AS APPLICABLE
SIZE D

Apple Computer Inc.

TITLE
SCHEM,SAPPHIRE,Q41B

DRAWING NUMBER 051-6694 REV. 02

SHT 1 OF 45



POWER SYSTEM ARCHITECTURE

AC ADAPTER IN PG 31

INRUSH LIMITER PG 30

+24V_PBUS

1V20_REF → U21 PG 31
>=13.44V TURNS-ON
<=13.44V SHUTS-OFF

RUN/SS
BUCK REGULATOR (LTC1625) PG 32
VCC
AC: 12.8V
NO AC: BATTERY VOLTAGE
1625 NOT RUNNING
SHUTDOWN: RUNNING
SLEEP: RUNNING
RUN: RUNNING

+PBUS (12.8V)

BACKLIGHT INVERTER

+5V_MAIN
VCC
MAIN 2.5V/1.5V DC/DC (MAX1715) PG 35
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING
TURNS ON OUTPUT @ 2.4V
ON1/ON2
PGOOD
1_5V_2_5V_OK

MAP31 DDR I/O
MAP31 DDR CORE
DDR POWER
+2.5V_MAIN
+1.5V_MAIN
INTREPID CORE
AGP I/O

+PBUS

DCDC_EN
SLEEP
MAXBUS SEQUENCING

+5V_MAIN
VCC
SHDN
DC/DC (MAX1717) PG 34
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING
CPU_VCORE (+1.4V/+1.5V)

14V_PBUS

+3V_PMU LDO PG 32
+BATT
+5V_MAIN
+3V_PMU
+4_6V_BU

RC AT 1M*0.047UF @ 24V
STARTS 2.0MSEC AFTER DCDC_EN_L BECOMES LOW

DCDC_EN_L
AFTER PMU IS UP AND RUNNING
DCDC_EN_L WILL PULL ON1/ON2
LOW IN SHUTDOWN

RUN/SS - 5V
TURNS ON AT >1V
<100UA ALLOWED
INTERNAL ZENER CLAMP TO 6V
MAIN 3V/5V DC/DC (LTC3707) PG 33
VCC
STBYMD
PGOOD
3V_5V_OK
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING
INTERNAL ZENER CLAMP TO 6V
<100UA ALLOWED
TURNS ON AT >1V
RUN/SS - 3V

HOLDS BOTH RUN/SS AT GND WHEN IT'S CONNECTED TO GND
TURNS CONTROL TO RUN/SS WHEN IT'S OPEN

+5V_MAIN

+PBUS (12.8V)

EXT_VCC
VCC
DC/DC (LTC1778) PG 20
SHUTDOWN: STOPPED
SLEEP: D3HOT/D3COLD
RUN: RUNNING
TURNS ON AS LOW AS 0.8V/TYP 1.5V
INTERNAL 1.2UA CURRENT SOURCE
RUN/SS
GPU_VCORE +1.2V/+1.0V

DCDC_EN
SLEEP
D3_COLD
GPU_VCORE SEQUENCING
1M & 0.1UF @14V, IT TAKES ~5.88MS TO START SWITCHER
1_5V_2_5V_OK
D3_HOT
DCDC_EN_L
D3_HOT

1_5V_2_5V_OK WILL NOT PULL LOW UNTIL +5V_MAIN TURNS ON
HOWEVER, 5V SHOULD TURN ON ~2.23MS AFTER DCDC_EN_L OR PMU_POWERUP_L BECOMES '1'; MUCH LESS THAN THE RC CHARGING AT INT_VCC (5V)

+PBUS

BACKUP BATTERY
CHARGER INPUT & BOOST OUTPUT PG 32
12.8V CHARGES BACKUP BATTERY
24V IS OUTPUT ONLY FROM BACKUP BATTERY

BACKUP BATTERY CIRCUIT CHARGES OFF +PBUS AND PREVENTS +PBUS AND +24V_PBUS FROM DROPPING BELOW 6V (UNTIL DRAINED)

RC AT 1M*0.1UF @ 24V
STARTS ~4.25MSEC AFTER DCDC_EN_L BECOMES LOW

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

+24V_PBUS

+3.3V_MAIN

DC/DC (LTC3411) PG 35
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING
+1.8V_MAIN
MAXBUS
BROADCOM

BATTERY CHARGER (MAX1772) PG 31

+BATT

3S 3P PRISMATIC CELLS

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

BATTERY VOLTAGE FEED-IN PATH PG 31

+PBUS

SHUT-DOWN RUN SLEEP RUN SHUT-DOWN

SLEEP
SLEEP_L_LS5
DCDC_EN
DCDC_EN_L
+5V_MAIN ~11MS
+5V_SLEEP
+3V_MAIN ~13.5MS
+3V_SLEEP
3V_5V_OK 2.4V - ??? MS
+2_5V_MAIN 2.6 MS
+2_5V_SLEEP
+1_5V_MAIN 2.6 MS
+1_5V_SLEEP
1_5V_2_5V_OK (MAX1715 OUTPUT)
1_5V_2_5V_OK (AT LTC1778 RUN/SS) ~???MS
GPU_VCORE (D3HOT)
GPU_VCORE (D3COLD)
+1_8V_MAIN 1.9 MS

POWER BLOCK DIAGRAM

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6694 | REV. 02

SCALE NONE | SHT 3 OF 45

PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 12
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

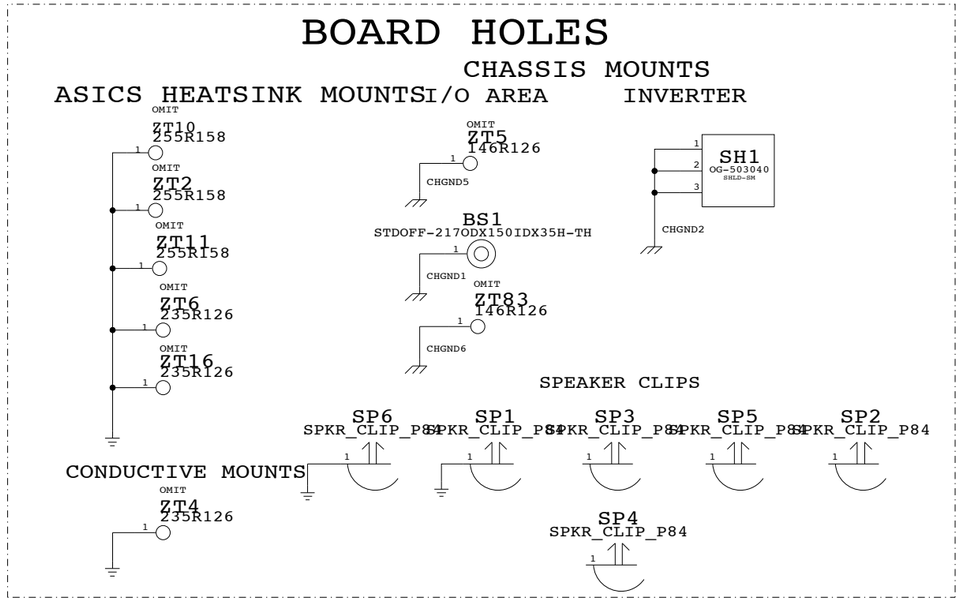
SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

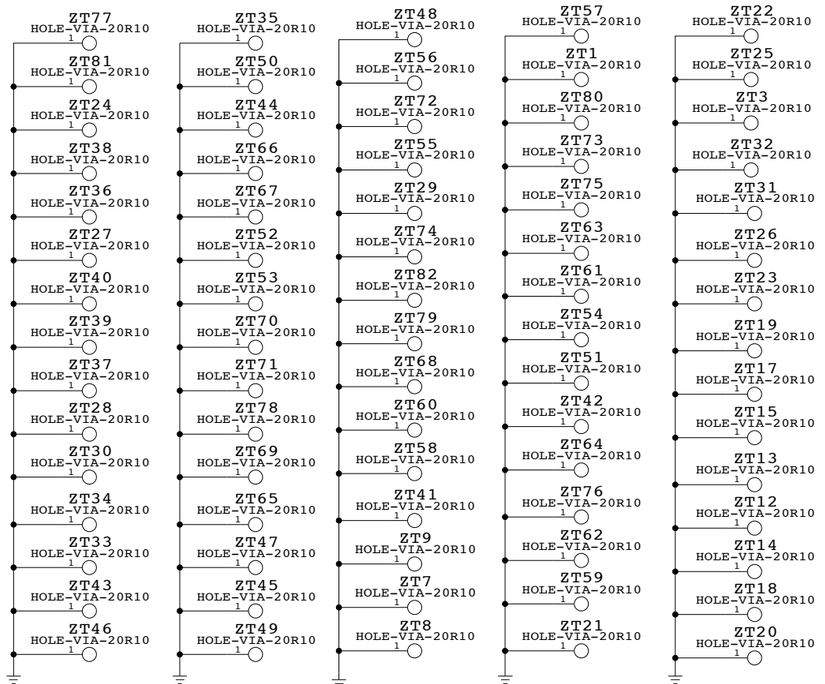
20R10 TH VIA OR VIA IN PAD

1		SIGNAL (1/3 OZ + COPPER PLATING)
2	PREPREG (3MIL)	GROUND (1/2 OZ)
3	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
4	PREPREG (3MIL)	SIGNAL (1/2 OZ)
5	LAMINATE (4MIL)	GROUND (1/2 OZ)
6	PREPREG (2MIL)	CUT POWER PLANE(1 OZ)
7	LAMINATE (3MIL)	CUT POWER PLANE(1 OZ)
8	PREPREG (2MIL)	GROUND (1/2 OZ)
9	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
10	PREPREG (3MIL)	SIGNAL (1/2 OZ)
11	LAMINATE (4MIL)	GROUND (1/2 OZ)
12	PREPREG (3MIL)	SIGNAL (1/3 OZ + COPPER PLATING)

BOARD HOLES



GROUND VIAS



BOARD INFORMATION

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	02

SCALE	SHT	OF
NONE	4	45

CPU_VCORE_SLEEP

CPU_VCORE DECOUPLING NETWORK

CPU_OVDD DECOUPLING NETWORK

MAXBUS_SLEEP 5 6 7 8 15 16 35 39

+1_5V_SLEEP 1_5V_MAXBUS

+1_8V_SLEEP 1_8V_MAXBUS

MPC7447 PULL-UPS

MORE 0805 10UF CAPS ON VCORE
POWER SUPPLY PAGE (PG 33)

PLCAE SHORT CLOSE TO CENTER OF CPU

XW31 SM

ADT7460_VCORE_MON 26 OMIT

PLACE BELOW CPU
IN FORMER L3 AREA

VDD

OVDD

AVDD

OVDDSENSE

NO STUFF

OMIT

CRITICAL

U43
1.50GHZ-1.28V
APOLL7_PM-R1.1
BGA
(1 OF 3)

CPU INTERNAL PLL FILTERING

470OHM FOR BOOT BANGER

BBANG

NO_BBANG

GND

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S2955	1	IC,A7PM,R1.2,1.67GHZ,1.24V	U43	CRITICAL	?

MPC7447 MAXBUS

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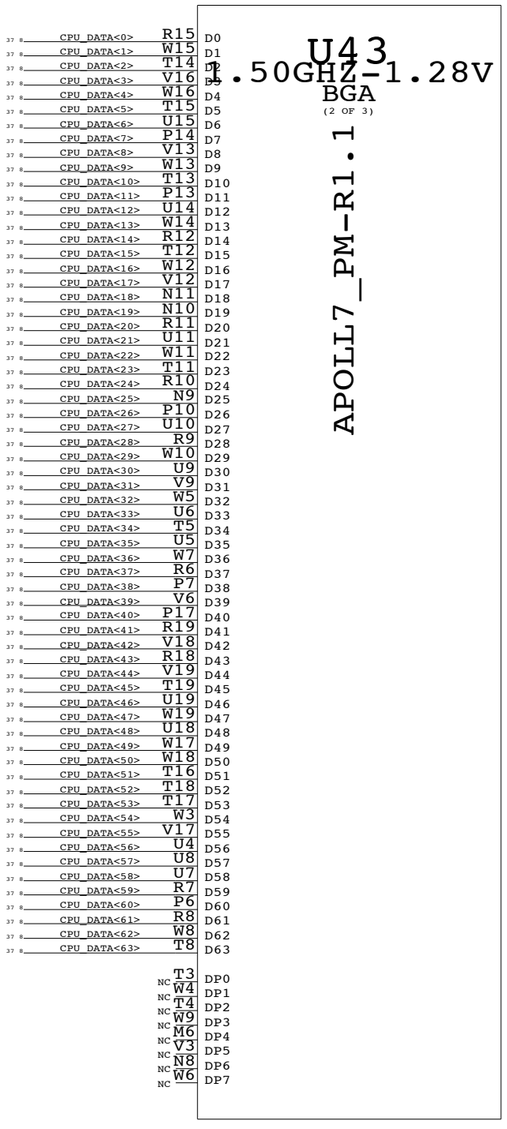
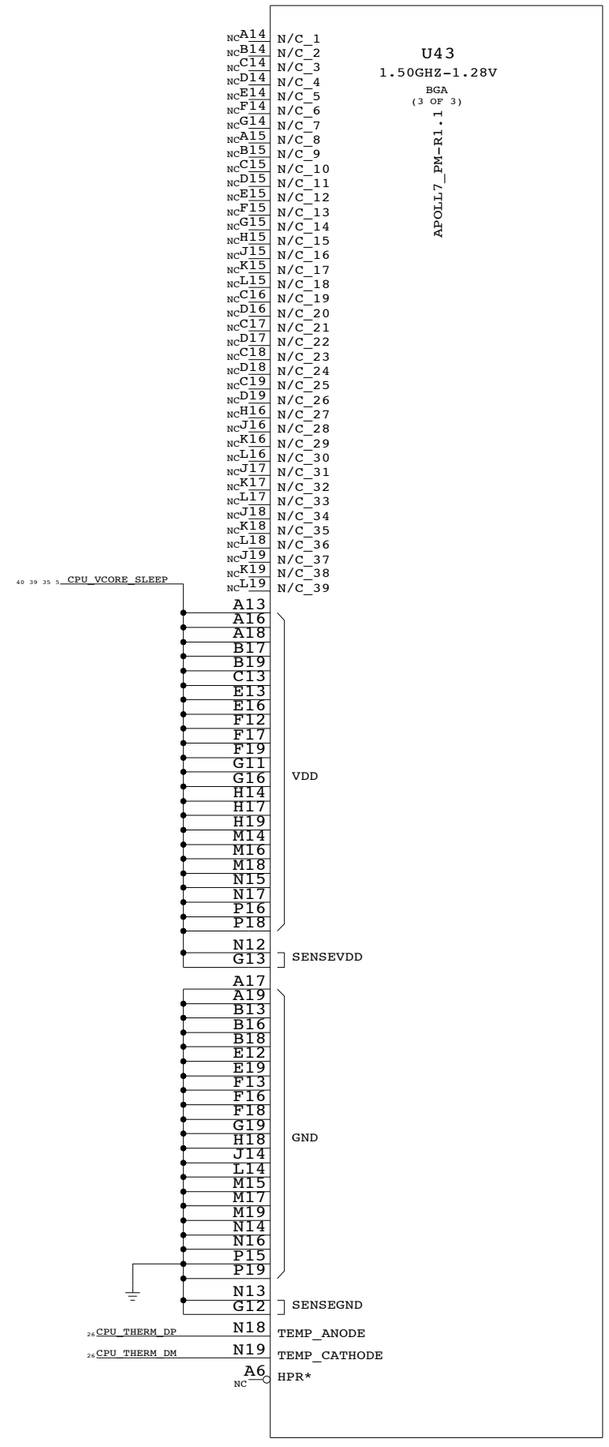
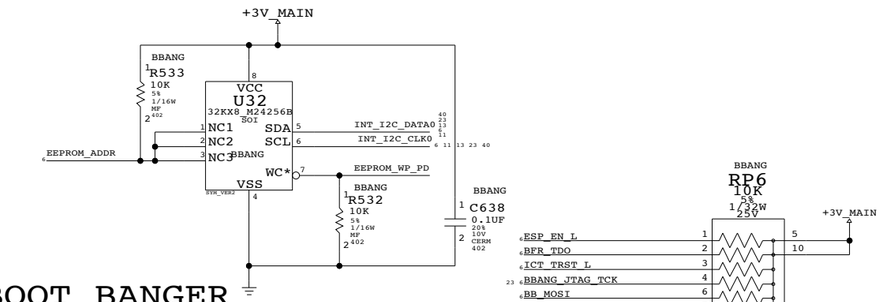
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	02
SCALE: NONE	SHT 5 OF 45	

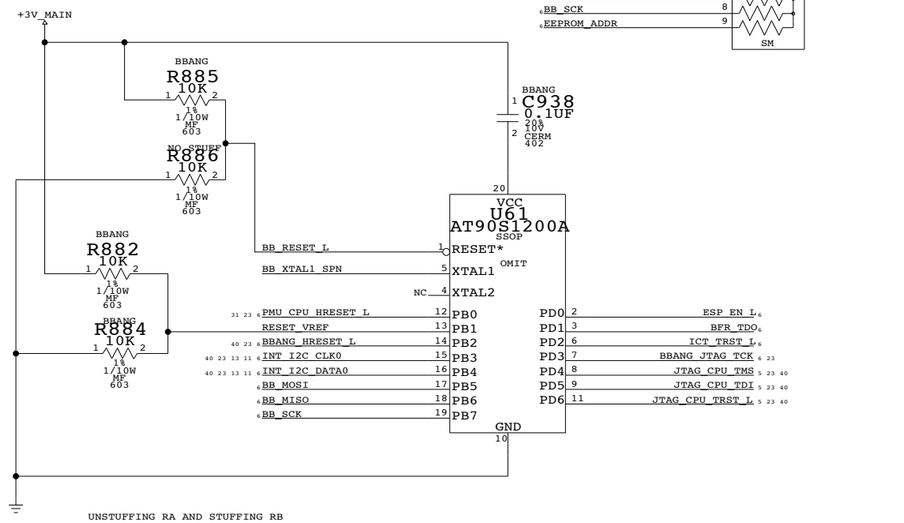




BOOT BANGER E2PROM

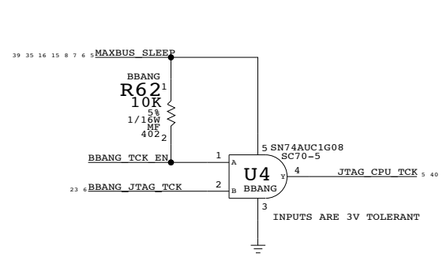


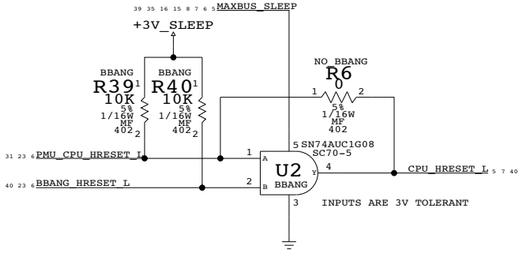
BOOT BANGER



UNSTUFFING RA AND STUFFING RB
WILL DISABLE THE CONTROLLER

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1135	1	009-6240 FW G74 BBANGER MCU,PROGRAMMED W/	U54	BBANG





BOOT BANGING SIGNAL DEFINITION

1/ BBANG_HRESET_L (OPEN COLLECTOR OUTPUT - 10K PULLUP ON MLB)
2/ PMU_HRESET_L (3V INPUT INTO LMU)
3/ BBANG_JTAG_TCK (REGULAR OUTPUT)
4/ JTAG_CPU_TMS (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
5/ JTAG_CPU_TDI (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
6/ JTAG_CPU_TRST_L (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)

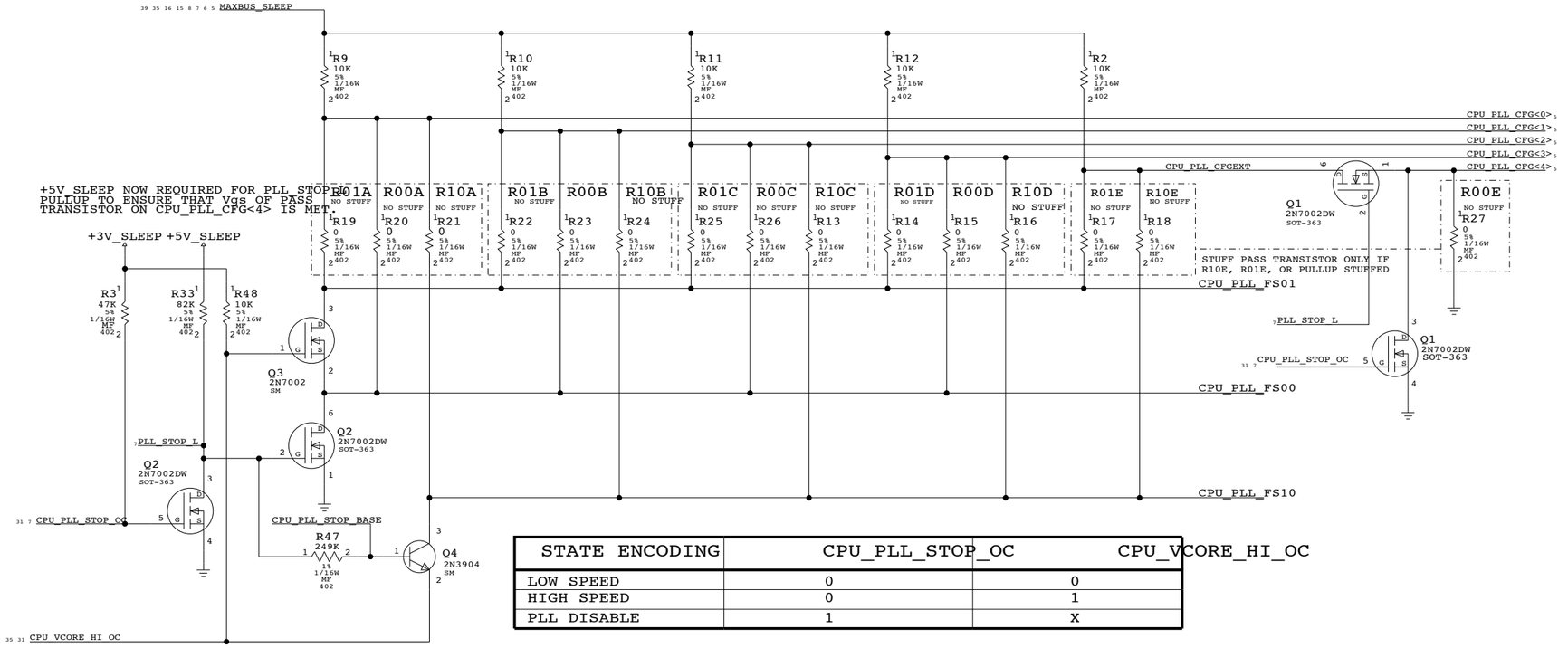
MPC7447/BBANG

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6654	02

SCALE	SHT	OF
NONE	6	45

CPU PLL CONFIG CIRCUITRY



STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

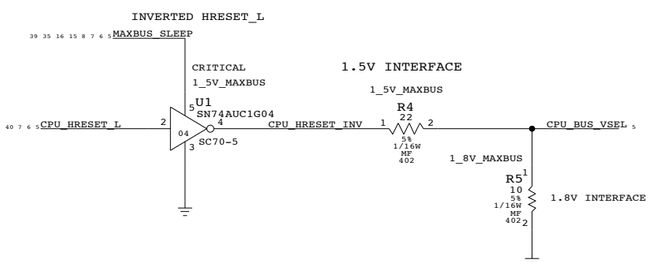
CPU FREQUENCY CONFIGURATION

APOLLO 7

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ (MHZ)	133MHZ (MHZ)	CPU_PLL_CFG 4 0123 HEX
0.0X	PLL OFF		0 1111 0F
1.0X	PLL BYPASS		0 0011 03
2.0X	333	267	0 0100 04
3.0X	500	400	0 1000 08
4.0X	667	533	0 1010 0A
5.0X	833	667	0 1011 0B
5.5X	917	733	0 1001 09
6.0X	1000	800	0 1101 0D
6.5X	1083	867	0 0101 05
7.0X	1167	933	0 0010 02
7.5X	1250	1000	0 0001 01
8.0X	1333	1067	0 1100 0C
8.5X	1417	1133	0 0110 06
9.0X	1500	1200	1 0111 17
9.5X	1583	1267	0 0111 07
10.0X	1667	1333	1 1010 1A
10.5X	1750	1400	1 1000 18
11.0X	1833	1467	1 1001 19
11.5X	1917	1533	0 0000 00
12.0X	2000	1600	1 1011 1B
12.5X	2083	1667	1 1111 1F
13.0X	2167	1733	1 0101 15
13.5X	2250	1800	0 1110 0E
14.0X	2333	1867	1 1100 1C
15.0X	2500	2000	1 0001 11
16.0X	2667	2133	1 1101 1D
17.0X	2833	2267	1 0000 10
18.0X	3000	2400	1 0010 12
20.0X	3333	2667	1 0011 13
21.0X	3500	2800	1 0100 14
24.0X	4000	3200	1 0110 16
28.0X	4667	3733	1 1110 1E

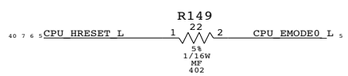
CPU CONFIGURATION

MAXBUS VSEL



DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L NEED TO CHARACTERIZE

BUSTYPE SELECT



APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

CPU CONFIGURATION

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6694 | REV. 02

SCALE NONE | SHT 7 OF 45

INTREPID BOOT STRAPS

BIT 32 TO 39

MAXBUS_SLEEP

NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF
R642[1] 10K 5% 1/16W MF 402	R135[1] 10K 5% 1/16W MF 402	R123[1] 10K 5% 1/16W MF 402	R153[1] 10K 5% 1/16W MF 402	R166[1] 10K 5% 1/16W MF 402	R179[1] 10K 5% 1/16W MF 402	R651[1] 10K 5% 1/16W MF 402	R178[1] 10K 5% 1/16W MF 402
CPU_DATA<32>	CPU_DATA<33>	CPU_DATA<34>	CPU_DATA<35>	CPU_DATA<36>	CPU_DATA<37>	CPU_DATA<38>	CPU_DATA<39>

NO STUFF							
R136[1] 10K 5% 1/16W MF 402	R643[1] 10K 5% 1/16W MF 402	R639[1] 10K 5% 1/16W MF 402	R657[1] 10K 5% 1/16W MF 402	R664[1] 10K 5% 1/16W MF 402	R673[1] 10K 5% 1/16W MF 402	R143[1] 10K 5% 1/16W MF 402	R674[1] 10K 5% 1/16W MF 402
0: TDI input (JTAG) 1: TDI output (JTAG)	0: Disable 1: Enable	0: Disable 1: Enable	0: Disable 1: Enable	Spare	Spare	Spare	Spare

BIT 40 TO 47

MAXBUS_SLEEP

NO STUFF	NO STUFF	NO STUFF	EXT_CLK	NO STUFF	INT_CLK	INT_CLK	INT_CLK
R122[1] 10K 5% 1/16W MF 402	R142[1] 10K 5% 1/16W MF 402	R164[1] 10K 5% 1/16W MF 402	R134[1] 10K 5% 1/16W MF 402	R184[1] 10K 5% 1/16W MF 402	R177[1] 10K 5% 1/16W MF 402	R152[1] 10K 5% 1/16W MF 402	R165[1] 10K 5% 1/16W MF 402
CPU_DATA<40>	CPU_DATA<41>	CPU_DATA<42>	CPU_DATA<43>	CPU_DATA<44>	CPU_DATA<45>	CPU_DATA<46>	CPU_DATA<47>

INT_CLK			EXT_CLK	EXT_CLK	EXT_CLK	EXT_CLK	
R640[1] 10K 5% 1/16W MF 402	R652[1] 10K 5% 1/16W MF 402	R665[1] 10K 5% 1/16W MF 402	R644[1] 10K 5% 1/16W MF 402	R683[1] 10K 5% 1/16W MF 402	R675[1] 10K 5% 1/16W MF 402	R658[1] 10K 5% 1/16W MF 402	R666[1] 10K 5% 1/16W MF 402
Spare	Spare	BIT2	BIT1	BIT0	0: Internal Spread Clock 1: Active	0: PLL1 Source Clock (NO SPREAD) 1: PLL1 Source Clock (SPREAD)	0: PLL2 Source Clock (NO SPREAD) 1: PLL2 Source Clock (SPREAD)

PLL4MODESEL_NXT[2:0]
000: 166.4MHZ (2.5X)
001: 149.76MHZ
010: 133.12MHZ (2.0X)
011: 99.84MHZ (1.5X)
100: 83.20MHZ

MODE A (2.5X) IS FOR STATIC OPERATION
MODE C (2.0X) IS FOR CLOCK SLEW OPERATION

BIT 48 TO 55

MAXBUS_SLEEP

EXT_CLK	EXT_CLK	NO STUFF	NO STUFF	NO STUFF		NO STUFF	
R133[1] 10K 5% 1/16W MF 402	R121[1] 10K 5% 1/16W MF 402	R163[1] 10K 5% 1/16W MF 402	R151[1] 10K 5% 1/16W MF 402	R162[1] 10K 5% 1/16W MF 402	R141[1] 10K 5% 1/16W MF 402	R183[1] 10K 5% 1/16W MF 402	R176[1] 10K 5% 1/16W MF 402
CPU_DATA<48>	CPU_DATA<49>	CPU_DATA<50>	CPU_DATA<51>	CPU_DATA<52>	CPU_DATA<53>	CPU_DATA<54>	CPU_DATA<55>

INT_CLK	INT_CLK	NO STUFF				NO STUFF	
R645[1] 10K 5% 1/16W MF 402	R641[1] 10K 5% 1/16W MF 402	R668[1] 10K 5% 1/16W MF 402	R659[1] 10K 5% 1/16W MF 402	R667[1] 10K 5% 1/16W MF 402	R653[1] 10K 5% 1/16W MF 402	R684[1] 10K 5% 1/16W MF 402	R676[1] 10K 5% 1/16W MF 402
0: Active 1: Buffer Reset	0: Internal 1: External source	Spare	Spare	BIT2	BIT1	BIT0	Spare

0: 1394b workaround Active
1: 1394b workaround Not Active

MaxBus output impedance
111: 28.6 ohm
011: 33.3 ohm
101: 40 ohm
001: 50 ohm
110: 66.6 ohm
010: 100 ohm
100: 200 ohm
000: 200 ohm

THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:

1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
2/ D46 - SELPCI1SPREADCLK - SLEEP/WAKE CYCLE REQUIRED
3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT

IF A STRAP IS NOT LISTED, THEN
IT CANNOT BE CHANGED BY SOFTWARE

R227 4.7 5% 1/16W MF 402
+1_5V_INTREPID_PLL — +1_5V_INTREPID_PLL7
C308 0.22UF 20% 6.3V CERM 402

H26 VDD15A_7 (PLL6) CRITICAL

U45 INTREPID-REV2.1 BGA

CPU_BR_L	E29	BR	INPUT
CPU_BG_L	E26	BG	NO BUS KEEPER
CPU_TS_L	B27	TS	NO BUS KEEPER

(1 OF 9)

CPU_ADDR<0>	D24	A_0
CPU_ADDR<1>	D25	A_1
CPU_ADDR<2>	A27	A_2
CPU_ADDR<3>	E24	A_3
CPU_ADDR<4>	G23	A_4
CPU_ADDR<5>	B26	A_5
CPU_ADDR<6>	A26	A_6
CPU_ADDR<7>	D23	A_7
CPU_ADDR<8>	A25	A_8
CPU_ADDR<9>	E23	A_9
CPU_ADDR<10>	J22	A_10
CPU_ADDR<11>	B25	A_11
CPU_ADDR<12>	H22	A_12
CPU_ADDR<13>	G22	A_13
CPU_ADDR<14>	D22	A_14
CPU_ADDR<15>	B24	A_15
CPU_ADDR<16>	B23	A_16
CPU_ADDR<17>	E22	A_17
CPU_ADDR<18>	J21	A_18
CPU_ADDR<19>	G21	A_19
CPU_ADDR<20>	E21	A_20
CPU_ADDR<21>	A24	A_21
CPU_ADDR<22>	D21	A_22
CPU_ADDR<23>	A23	A_23
CPU_ADDR<24>	H20	A_24
CPU_ADDR<25>	B22	A_25
CPU_ADDR<26>	H21	A_26
CPU_ADDR<27>	A22	A_27
CPU_ADDR<28>	E20	A_28
CPU_ADDR<29>	B21	A_29
CPU_ADDR<30>	D20	A_30
CPU_ADDR<31>	A21	A_31

MAXBUS INTERFACE

CPU_CI_L	G26	CI	
CPU_GBL_L	A29	GBL	
CPU_TBST_L	A28	TBST	
CPU_TSIZ<0>	G24	TSIZ_0	
CPU_TSIZ<1>	H24	TSIZ_1	
CPU_TSIZ<2>	D26	TSIZ_2	
CPU_TT<0>	E25	TT_0	
CPU_TT<1>	G25	TT_1	
CPU_TT<2>	B28	TT_2	
CPU_TT<3>	D27	TT_3	
CPU_TT<4>	J25	TT_4	
CPU_WT_L	D28	WT	
CPU_AACK_L	B29	AACK	NO BUS KEEPER - PU
CPU_ARTRY_L	H23	ARTRY	NO BUS KEEPER - PU
CPU_HIT_L	B31	HIT	INPUT - PU
CPU_QREQ_L	A32	QREQ	INPUT - PD
CPU_QACK_L	G27	QACK	NO BUS KEEPER - ?
INT_SUSPEND_REQ_L	AK9	SUSPENDREQ	
INT_SUSPEND_ACK_L	AM8	SUSPENDACK	

Vin = Intrepid Vcore (1.5V)
Vout = Maxbus rail (1.8V)

CPU_FB_IN			
CPU_FB_OUT		NO BUS KEEPER - PU	
ANALYZER_CLK			
STOPCPUCLK		INPUT - PU	
ACS_REF	H13	NO BUS KEEPER - ?	
CPU_CLK	J15	NO BUS KEEPER - ?	
		NO BUS KEEPER - PU	
		NO BUS KEEPER - PU	
TBEN	A31	NO BUS KEEPER - PU	

INTREPID OUTPUTS HIGH BY DEFAULT

VSSA_7 (PLL6)
H25

DBG	A30	CPU_DBG_L	5 8 37
DRDY	G28	CPU_DRDY_L	5 8 37
DTI_0	K25	CPU_DTI<0>	5 37
DTI_1	D29	CPU_DTI<1>	5 37
DTI_2	B30	CPU_DTI<2>	5 37
TA	E27	CPU_TA_L	5 8 37
TEA	E28	CPU_TEA_L	5 8 37

D_0	D10	CPU_DATA<0>	6 37
D_1	G12	CPU_DATA<1>	6 37
D_2	E11	CPU_DATA<2>	6 37
D_3	H11	CPU_DATA<3>	6 37
D_4	B9	CPU_DATA<4>	6 37
D_5	B8	CPU_DATA<5>	6 37
D_6	A9	CPU_DATA<6>	6 37
D_7	A8	CPU_DATA<7>	6 37
D_8	E12	CPU_DATA<8>	6 37
D_9	D11	CPU_DATA<9>	6 37
D_10	B10	CPU_DATA<10>	6 37
D_11	J13	CPU_DATA<11>	6 37
D_12	A10	CPU_DATA<12>	6 37
D_13	D12	CPU_DATA<13>	6 37
D_14	E13	CPU_DATA<14>	6 37
D_15	G13	CPU_DATA<15>	6 37
D_16	B11	CPU_DATA<16>	6 37
D_17	D13	CPU_DATA<17>	6 37
D_18	A11	CPU_DATA<18>	6 37
D_19	G14	CPU_DATA<19>	6 37
D_20	H14	CPU_DATA<20>	6 37
D_21	E14	CPU_DATA<21>	6 37
D_22	B12	CPU_DATA<22>	6 37
D_23	G15	CPU_DATA<23>	6 37
D_24	B13	CPU_DATA<24>	6 37
D_25	H15	CPU_DATA<25>	6 37
D_26	D14	CPU_DATA<26>	6 37
D_27	B14	CPU_DATA<27>	6 37
D_28	A12	CPU_DATA<28>	6 37
D_29	G16	CPU_DATA<29>	6 37
D_30	E15	CPU_DATA<30>	6 37
D_31	J16	CPU_DATA<31>	6 37
D_32	D15	CPU_DATA<32>	6 8 37
D_33	A14	CPU_DATA<33>	6 8 37
D_34	A13	CPU_DATA<34>	6 8 37
D_35	D16	CPU_DATA<35>	6 8 37
D_36	E16	CPU_DATA<36>	6 8 37
D_37	G17	CPU_DATA<37>	6 8 37
D_38	B15	CPU_DATA<38>	6 8 37
D_39	H17	CPU_DATA<39>	6 8 37
D_40	A15	CPU_DATA<40>	6 8 37
D_41	B16	CPU_DATA<41>	6 8 37
D_42	E17	CPU_DATA<42>	6 8 37
D_43	A16	CPU_DATA<43>	6 8 37
D_44	J18	CPU_DATA<44>	6 8 37
D_45	H18	CPU_DATA<45>	6 8 37
D_46	D17	CPU_DATA<46>	6 8 37
D_47	G18	CPU_DATA<47>	6 8 37
D_48	A17	CPU_DATA<48>	6 8 37
D_49	B17	CPU_DATA<49>	6 8 37
D_50	E18	CPU_DATA<50>	6 8 37
D_51	B18	CPU_DATA<51>	6 8 37
D_52	D18	CPU_DATA<52>	6 8 37
D_53	A18	CPU_DATA<53>	6 8 37
D_54	A19	CPU_DATA<54>	6 8 37
D_55	H19	CPU_DATA<55>	6 8 37
D_56	B19	CPU_DATA<56>	6 8 37
D_57	J19	CPU_DATA<57>	6 8 37
D_58	A20	CPU_DATA<58>	6 8 37
D_59	D19	CPU_DATA<59>	6 8 37
D_60	E19	CPU_DATA<60>	6 8 37
D_61	G19	CPU_DATA<61>	6 8 37
D_62	B20	CPU_DATA<62>	6 8 37
D_63	G20	CPU_DATA<63>	6 8 37

FB BUFFER HAS 50 OHM OUTPUT IMPEDANCE

INT_CPUFB_IN	J24		
INT_CPUFB_OUT	H16		
SYSCLK_LA_TP	G8		
CPU_CLK_EN	AH9		
INTREPID_ACS_REF	H13		
SYSCLK_CPU	J15		
CPU_TBEN	A31		

R197[1] 511 1% 1/16W MF 402
R144 0 5% 1/16W MF 402
R137[1] 1K 1% 1/16W MF 402

SHORT = 1" SHORTER THAN MATCHED LENGTH
LONG = 1" LONGER THAN MATCHED LENGTH
NO STUFF

INT_CPUFB_OUT2	R167 0 5% 1/16W MF 402	INT_CPUFB_OUT_SHORT	R215 0 5% 1/16W MF 402	INT_CPUFB_OUT_NORM	R207 0 5% 1/16W MF 402	INT_CPUFB_LONG	
INT_CPUFB_IN	R225[1] 0 5% 1/16W MF 402	R226 0 5% 1/16W MF 402		INT_CPUFB_IN_NORM	R208[1] 0 5% 1/16W MF 402	R196 0 5% 1/16W MF 402	

MAXBUS PULL-UPS

MAXBUS_SLEEP

CPU_TS_L	RP21 10K 5% 1/16W SM1	2	7
CPU_TA_L	RP21 10K 5% 1/16W SM1	1	8
CPU_ARTRY_L	RP21 10K 5% 1/16W SM1	4	5
CPU_BR_L	RP23 10K 5% 1/16W SM1	1	8
CPU_HIT_L	RP24 10K 5% 1/16W SM1	3	6
CPU_DRDY_L	RP23 10K 5% 1/16W SM1	3	6
CPU_TEA_L	RP23 10K 5% 1/16W SM1	4	5
CPU_AACK_L	RP23 10K 5% 1/16W SM1	2	7
CPU_DBG_L	RP24 10K 5% 1/16W SM1	4	5
CPU_BG_L	RP21 10K 5% 1/16W SM1	3	6
CPU_QREQ_L	RP24 10K 5% 1/16W SM1	2	7

INTREPID BOOT STRAPS

BIT 56 TO 63

MAXBUS_SLEEP

NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF		NO STUFF
R140[1] 10K 5% 1/16W MF 402	R161[1] 10K 5% 1/16W MF 402	R175[1] 10K 5% 1/16W MF 402	R132[1] 10K 5% 1/16W MF 402	R131[1] 10K 5% 1/16W MF 402	R150[1] 10K 5% 1/16W MF 402	R174[1] 10K 5% 1/16W MF 402	R182[1] 10K 5% 1/16W MF 402
CPU_DATA<56>	CPU_DATA<57>	CPU_DATA<58>	CPU_DATA<59>	CPU_DATA<60>	CPU_DATA<61>	CPU_DATA<62>	CPU_DATA<63>

						NO STUFF	
R654[1] 10K 5% 1/16W MF 402	R669[1] 10K 5% 1/16W MF 402	R677[1] 10K 5% 1/16W MF 402	R646[1] 10K 5% 1/16W MF 402	R647[1] 10K 5% 1/16W MF 402	R660[1] 10K 5% 1/16W MF 402	R678[1] 10K 5% 1/16W MF 402	R685[1] 10K 5% 1/16W MF 402
Spare	Spare	Spare	PCI1_REQ2_L / PCI1_GNT2_L 0: GPIOs 1: GPIOs	PCI1_REQ1_L / PCI1_GNT1_L 0: GPIOs 1: GPIOs	PCI1_REQ0_L / PCI1_GNT0_L 0: GPIOs 1: GPIOs	0: Legacy PCI interface 1: Legacy PCI interface 0: I2C bus 1: I2C bus	0: Processor Bus Mode 1: I2C bus (DS)

Intrepid MaxBus

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	02
SCALE: NONE	SHT 8 OF 45	

SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

PINS ARE SWAPABLE FOR RPAKS

U45
INTREPID-REV2.1
BGA
(2 OF 9)
CRITICAL

MEM_DATA<0>	AK32	DDR_DATA_0	H35	MEM_ADDR<0>	DDR_A_0
MEM_DATA<1>	AK33	DDR_DATA_1	G35	MEM_ADDR<1>	DDR_A_1
MEM_DATA<2>	AK31	DDR_DATA_2	G36	MEM_ADDR<2>	DDR_A_2
MEM_DATA<3>	AK35	DDR_DATA_3	F36	MEM_ADDR<3>	DDR_A_3
MEM_DATA<4>	AK36	DDR_DATA_4	F35	MEM_ADDR<4>	DDR_A_4
MEM_DATA<5>	AJ32	DDR_DATA_5	E35	MEM_ADDR<5>	DDR_A_5
MEM_DATA<6>	AJ35	DDR_DATA_6	E36	MEM_ADDR<6>	DDR_A_6
MEM_DATA<7>	AJ36	DDR_DATA_7	G32	MEM_ADDR<7>	DDR_A_7
MEM_DATA<8>	AG33	DDR_DATA_8	D36	MEM_ADDR<8>	DDR_A_8
MEM_DATA<9>	AG35	DDR_DATA_9	H36	MEM_ADDR<9>	DDR_A_9
MEM_DATA<10>	AH35	DDR_DATA_10	G33	MEM_ADDR<10>	DDR_A_10
MEM_DATA<11>	AG36	DDR_DATA_11	H33	MEM_ADDR<11>	DDR_A_11
MEM_DATA<12>	AH36	DDR_DATA_12	D35	MEM_ADDR<12>	DDR_A_12
MEM_DATA<13>	AH32	DDR_DATA_13	L30	MEM_BA<0>	DDR_BA_0
MEM_DATA<14>	AG32	DDR_DATA_14	M29	MEM_BA<1>	DDR_BA_1
MEM_DATA<15>	AG31	DDR_DATA_15	AN34	MEM_CS_L<0>	DDRCS_0
MEM_DATA<16>	AE32	DDR_DATA_16	AN36	MEM_CS_L<1>	DDRCS_1
MEM_DATA<17>	AF35	DDR_DATA_17	AL35	MEM_CS_L<2>	DDRCS_2
MEM_DATA<18>	AF36	DDR_DATA_18	AL33	MEM_CS_L<3>	DDRCS_3
MEM_DATA<19>	AE36	DDR_DATA_19	AJ31	MEM_DQS<0>	DDR_DQS_0
MEM_DATA<20>	AE35	DDR_DATA_20	AH31	MEM_DQS<1>	DDR_DQS_1
MEM_DATA<21>	AE33	DDR_DATA_21	AD32	MEM_DQS<2>	DDR_DQS_2
MEM_DATA<22>	AD36	DDR_DATA_22	AB30	MEM_DQS<3>	DDR_DQS_3
MEM_DATA<23>	AD35	DDR_DATA_23	V30	MEM_DQS<4>	DDR_DQS_4
MEM_DATA<24>	AA36	DDR_DATA_24	P32	MEM_DQS<5>	DDR_DQS_5
MEM_DATA<25>	AA35	DDR_DATA_25	N29	MEM_DQS<6>	DDR_DQS_6
MEM_DATA<26>	AA33	DDR_DATA_26	L32	MEM_DQS<7>	DDR_DQS_7
MEM_DATA<27>	AB36	DDR_DATA_27	AJ33	MEM_DM<0>	DDR_DM_0
MEM_DATA<28>	AB35	DDR_DATA_28	AH33	MEM_DQM<1>	DDR_DM_1
MEM_DATA<29>	AC36	DDR_DATA_29	AD33	MEM_DQM<2>	DDR_DM_2
MEM_DATA<30>	AA32	DDR_DATA_30	AC35	MEM_DQM<3>	DDR_DM_3
MEM_DATA<31>	AB33	DDR_DATA_31	P35	MEM_DQM<4>	DDR_DM_4
MEM_DATA<32>	V36	DDR_DATA_32	P33	MEM_DQM<5>	DDR_DM_5
MEM_DATA<33>	U33	DDR_DATA_33	N32	MEM_DQM<6>	DDR_DM_6
MEM_DATA<34>	U32	DDR_DATA_34	L33	MEM_DQM<7>	DDR_DM_7
MEM_DATA<35>	V35	DDR_DATA_35	L29	MEM_RAS_L	DDRRAS
MEM_DATA<36>	T30	DDR_DATA_36	H32	MEM_CAS_L	DDRCAS
MEM_DATA<37>	U36	DDR_DATA_37	K30	MEM_WE_L	DDRWE
MEM_DATA<38>	U35	DDR_DATA_38	AN35	MEM_CKE<0>	DDRCKE0
MEM_DATA<39>	T36	DDR_DATA_39	AM35	MEM_CKE<1>	DDRCKE1
MEM_DATA<40>	P33	DDR_DATA_40	AM36	MEM_CKE<2>	DDRCKE2
MEM_DATA<41>	R30	DDR_DATA_41	AL36	MEM_CKE<3>	DDRCKE3
MEM_DATA<42>	P35	DDR_DATA_42	AB32	MEM_MUXSEL_H<0>	DDR_SELHI_0
MEM_DATA<43>	P36	DDR_DATA_43	AE29	MEM_MUXSEL_H<1>	DDR_SELHI_1
MEM_DATA<44>	R36	DDR_DATA_44	N30	MEM_MUXSEL_L<0>	DDR_SELLO_0
MEM_DATA<45>	R35	DDR_DATA_45	T32	MEM_MUXSEL_L<1>	DDR_SELLO_1
MEM_DATA<46>	R33	DDR_DATA_46	Y32	SYSCLK_DDRCLK_A0_UF	DDR_MCLK_0_P
MEM_DATA<47>	R32	DDR_DATA_47	Y33	SYSCLK_DDRCLK_A0_L_UF	DDR_MCLK_0_N
MEM_DATA<48>	N35	DDR_DATA_48	Y35	SYSCLK_DDRCLK_A1_UF	DDR_MCLK_1_P
MEM_DATA<49>	M36	DDR_DATA_49	Y36	SYSCLK_DDRCLK_A1_L_UF	DDR_MCLK_1_N
MEM_DATA<50>	L35	DDR_DATA_50	Y30	INT_DDRCLK2_P_TP	DDR_MCLK_2_P
MEM_DATA<51>	M35	DDR_DATA_51	W30	INT_DDRCLK2_N_TP	DDR_MCLK_2_N
MEM_DATA<52>	M33	DDR_DATA_52	W32	SYSCLK_DDRCLK_B0_UF	DDR_MCLK_3_P
MEM_DATA<53>	L36	DDR_DATA_53	W33	SYSCLK_DDRCLK_B0_L_UF	DDR_MCLK_3_N
MEM_DATA<54>	N33	DDR_DATA_54	V33	SYSCLK_DDRCLK_B1_UF	DDR_MCLK_4_P
MEM_DATA<55>	M30	DDR_DATA_55	V32	SYSCLK_DDRCLK_B1_L_UF	DDR_MCLK_4_N
MEM_DATA<56>	J32	DDR_DATA_56	W35	INT_DDRCLK5_P_TP	DDR_MCLK_5_P
MEM_DATA<57>	J33	DDR_DATA_57	W36	INT_DDRCLK5_N_TP	DDR_MCLK_5_N
MEM_DATA<58>	J35	DDR_DATA_58	AA22	INT_MEM_REF_H	DDR_REF
MEM_DATA<59>	K32	DDR_DATA_59	Y22	INT_MEM_VREF	DDR_VREF_0
MEM_DATA<60>	K33	DDR_DATA_60	T22		DDR_VREF_1
MEM_DATA<61>	J36	DDR_DATA_61			
MEM_DATA<62>	K36	DDR_DATA_62			
MEM_DATA<63>	K35	DDR_DATA_63			

DDR MEMORY INTERFACE

'0' & '1' GO TO SLOT A
'2' & '3' GO TO SLOT B

'0'S ARE SAME POLARITY (ACTIVE-LO)
'1'S ARE SAME POLARITY (ACTIVE-HI)

MEM_VREF

R199 1K 1% 1/16W MF 402

+2_5V_INTREPID

R198 10K 1% 1/16W MF 402
R191 10K 1% 1/16W MF 402
C245 0.1UF 20% 10V CERM 402

CLOCKS

SYSCLK_DDRCLK_A1_UF	RP33	SYSCLK_DDRCLK_A1
SYSCLK_DDRCLK_A1_L_UF	RP33	SYSCLK_DDRCLK_A1_L
SYSCLK_DDRCLK_A0_UF	RP34	SYSCLK_DDRCLK_A0
SYSCLK_DDRCLK_A0_L_UF	RP34	SYSCLK_DDRCLK_A0_L
SYSCLK_DDRCLK_B1_UF	RP33	SYSCLK_DDRCLK_B1
SYSCLK_DDRCLK_B1_L_UF	RP33	SYSCLK_DDRCLK_B1_L
SYSCLK_DDRCLK_B0_UF	RP34	SYSCLK_DDRCLK_B0
SYSCLK_DDRCLK_B0_L_UF	RP34	SYSCLK_DDRCLK_B0_L

CS

MEM_CS_L<0>	RP36	RAM_CS_L<0>
MEM_CS_L<1>	RP36	RAM_CS_L<1>
MEM_CS_L<2>	RP35	RAM_CS_L<2>
MEM_CS_L<3>	RP35	RAM_CS_L<3>

CKE

MEM_CKE<0>	RP36	RAM_CKE<0>
MEM_CKE<1>	RP36	RAM_CKE<1>
MEM_CKE<2>	RP35	RAM_CKE<2>
MEM_CKE<3>	RP35	RAM_CKE<3>

ADDR

MEM_ADDR<0>	RP31	RAM_ADDR<0>
MEM_ADDR<1>	RP25	RAM_ADDR<1>
MEM_ADDR<2>	RP25	RAM_ADDR<2>
MEM_ADDR<3>	RP25	RAM_ADDR<3>
MEM_ADDR<4>	RP25	RAM_ADDR<4>
MEM_ADDR<5>	RP30	RAM_ADDR<5>
MEM_ADDR<6>	RP30	RAM_ADDR<6>
MEM_ADDR<7>	RP31	RAM_ADDR<7>
MEM_ADDR<8>	RP30	RAM_ADDR<8>
MEM_ADDR<9>	RP31	RAM_ADDR<9>
MEM_ADDR<10>	RP31	RAM_ADDR<10>
MEM_ADDR<11>	RP26	RAM_ADDR<11>
MEM_ADDR<12>	RP30	RAM_ADDR<12>

BA

MEM_BA<0>	RP26	RAM_BA<0>
MEM_BA<1>	RP26	RAM_BA<1>

CNTL

MEM_WE_L	RP26	RAM_WE_L
MEM_CAS_L	R250	RAM_CAS_L
MEM_RAS_L	R238	RAM_RAS_L

All: 22 5% 1/16W SM1

1MB BOOT ROM

+3V_MAIN

C460 2.2UF 20% 10V CERM 805
C470 0.1UF 20% 10V CERM 402
C479 0.1UF 20% 10V CERM 402

U17
FEPR-1MX8
3.3V
TSOP
OMIT

VPP 11, VCC 30, 31

A0	21	PCI_AD<0>	
A1	20	PCI_AD<1>	
A2	19	PCI_AD<2>	
A3	18	PCI_AD<3>	
A4	17	PCI_AD<4>	
A5	16	PCI_AD<5>	
A6	15	PCI_AD<6>	
A7	14	PCI_AD<7>	
A8	8	PCI_AD<8>	
A9	7	PCI_AD<9>	
A10	36	PCI_AD<10>	
A11	6	PCI_AD<11>	
A12	5	PCI_AD<12>	
A13	4	PCI_AD<13>	
A14	3	PCI_AD<14>	
A15	2	PCI_AD<15>	
A16	1	PCI_AD<16>	
A17	40	PCI_AD<17>	
A18	13	PCI_AD<18>	
A19	37	PCI_AD<19>	
A20	38	PCI_AD<20>	
CE	22	ROM_ONBOARD_CS_L	
OE	24	ROM_OE_L	
WE	9	ROM_RW_L	
WP	12	ROM_WP_L	
PWD	10	INT_RESET_L	

DQ0	25	PCI_AD<24>	
DQ1	26	PCI_AD<25>	
DQ2	27	PCI_AD<26>	
DQ3	28	PCI_AD<27>	
DQ4	32	PCI_AD<28>	
DQ5	33	PCI_AD<29>	
DQ6	34	PCI_AD<30>	
DQ7	35	PCI_AD<31>	

GND 23, 39

+3V_MAIN

R338 10K 5% 1/16W MF 402
R386 10K 5% 1/16W MF 402
R357 1K 5% 1/16W MF 402

ROM_CS_L

OVERRIDE ROM MODULE
INTERCEPTS ROM CHIP SELECT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1556	1	IC,BOOTROM,Q41B	U17	CRITICAL	?

PULL-DOWN RESISTORS TO ENSURE
CKE STAYS LOW AFTER INTREPID
2.5V I/O SHUTS OFF

RAM_CKE<0>
RAM_CKE<1>
RAM_CKE<2>
RAM_CKE<3>

R500 10K 5% 1/16W MF 402
R439 10K 5% 1/16W MF 402
R409 10K 5% 1/16W MF 402
R387 10K 5% 1/16W MF 402

INT - DDR/BOOTROM

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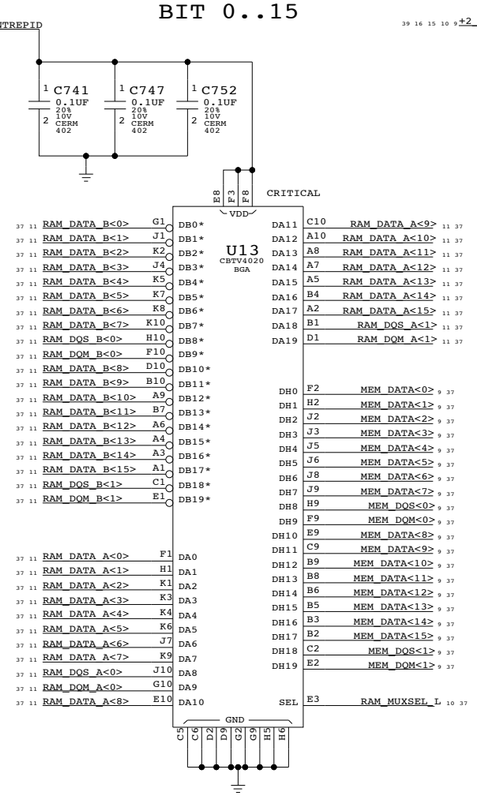
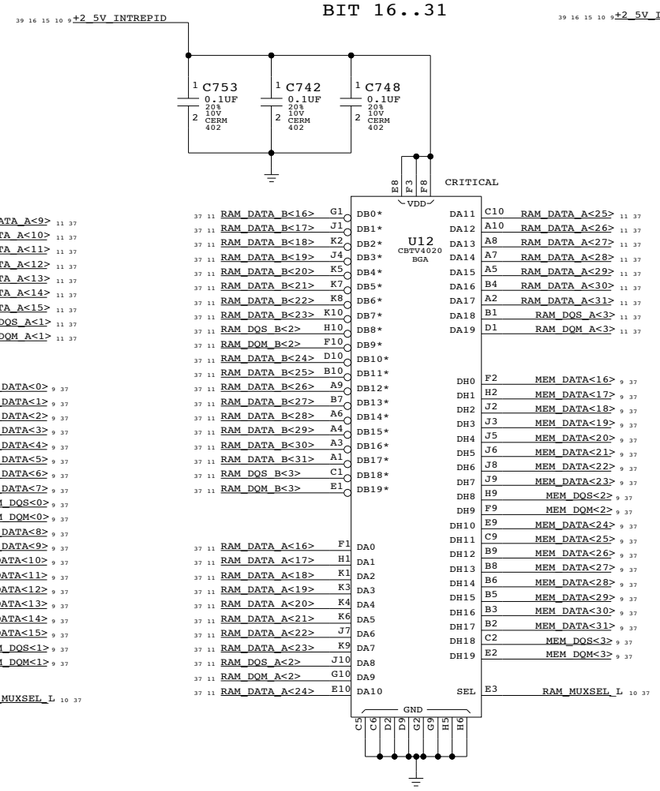
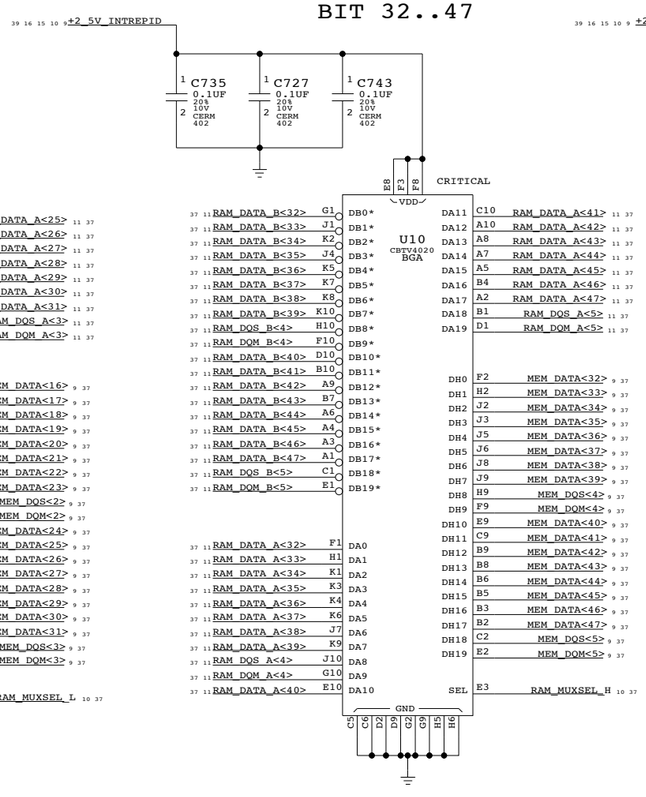
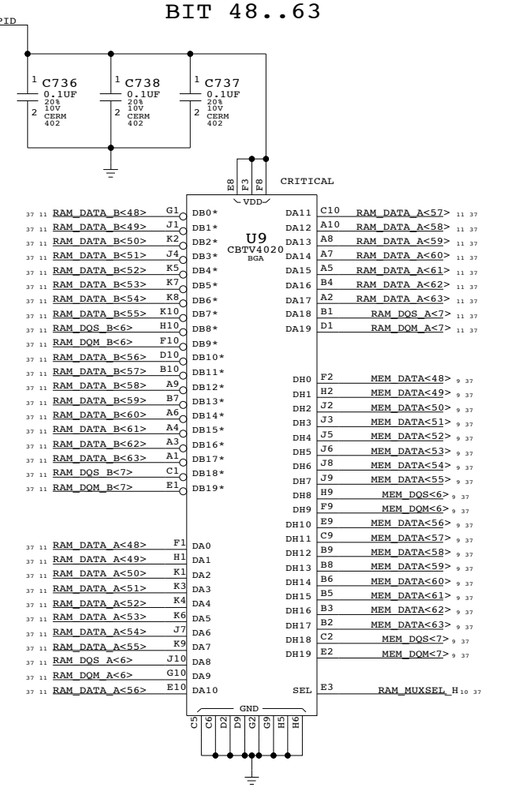
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	02
SCALE: NONE	SHT 9 OF 45	









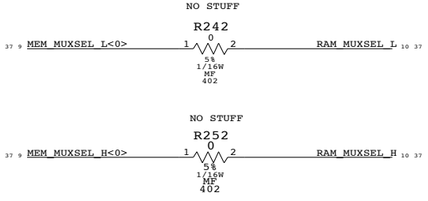
SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND

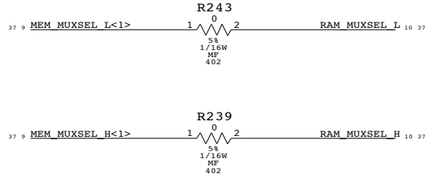
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND

MEM_MUXSEL_H<0> AND MEM_MUXSEL_L<0> ARE ACTIVE LOW

MEM_MUXSEL_H<1> AND MEM_MUXSEL_L<1> ARE ACTIVE HIGH

ADDED 0 OHM RESISTORS IN CASE POLARITY IS WRONG



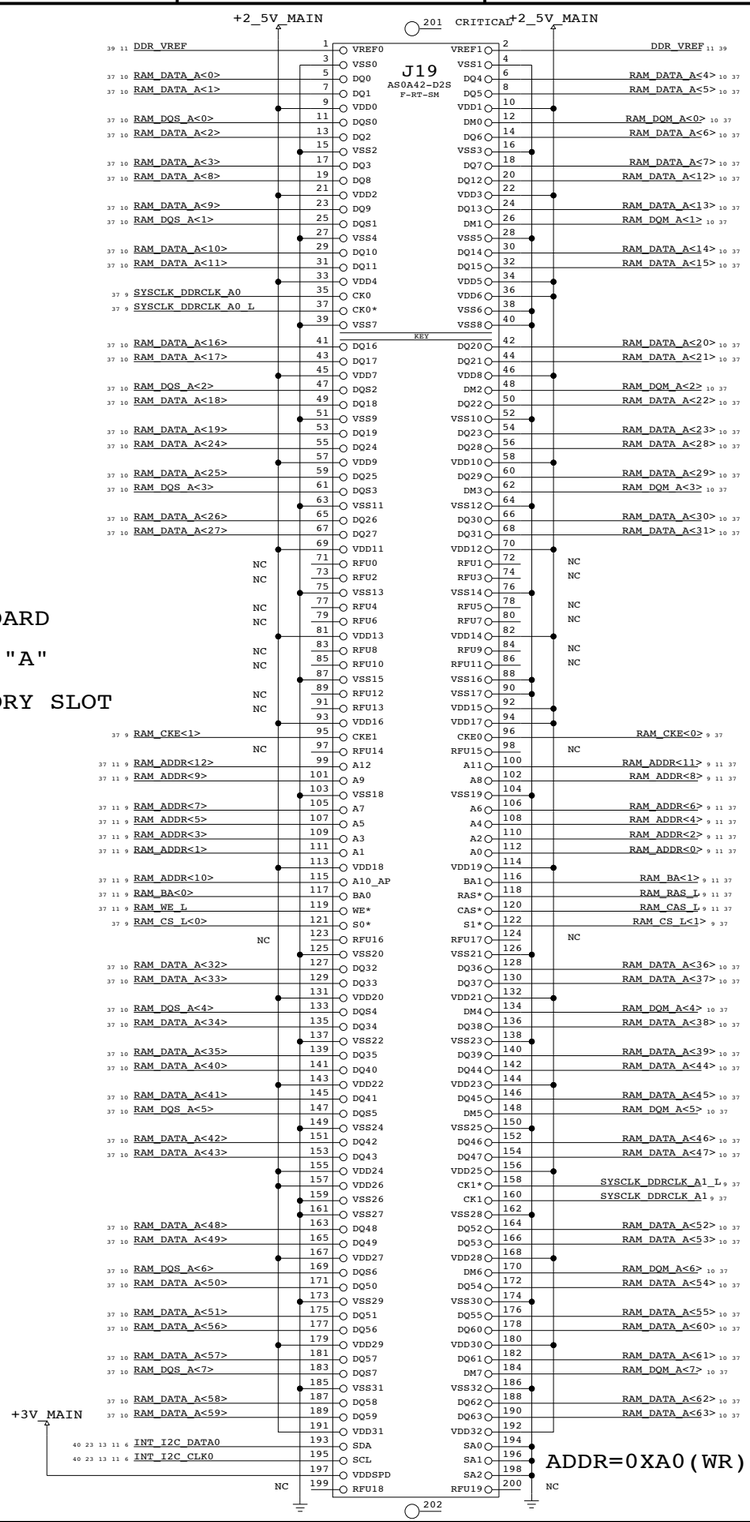


16BIT 2:1 DDR MUXES

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	02

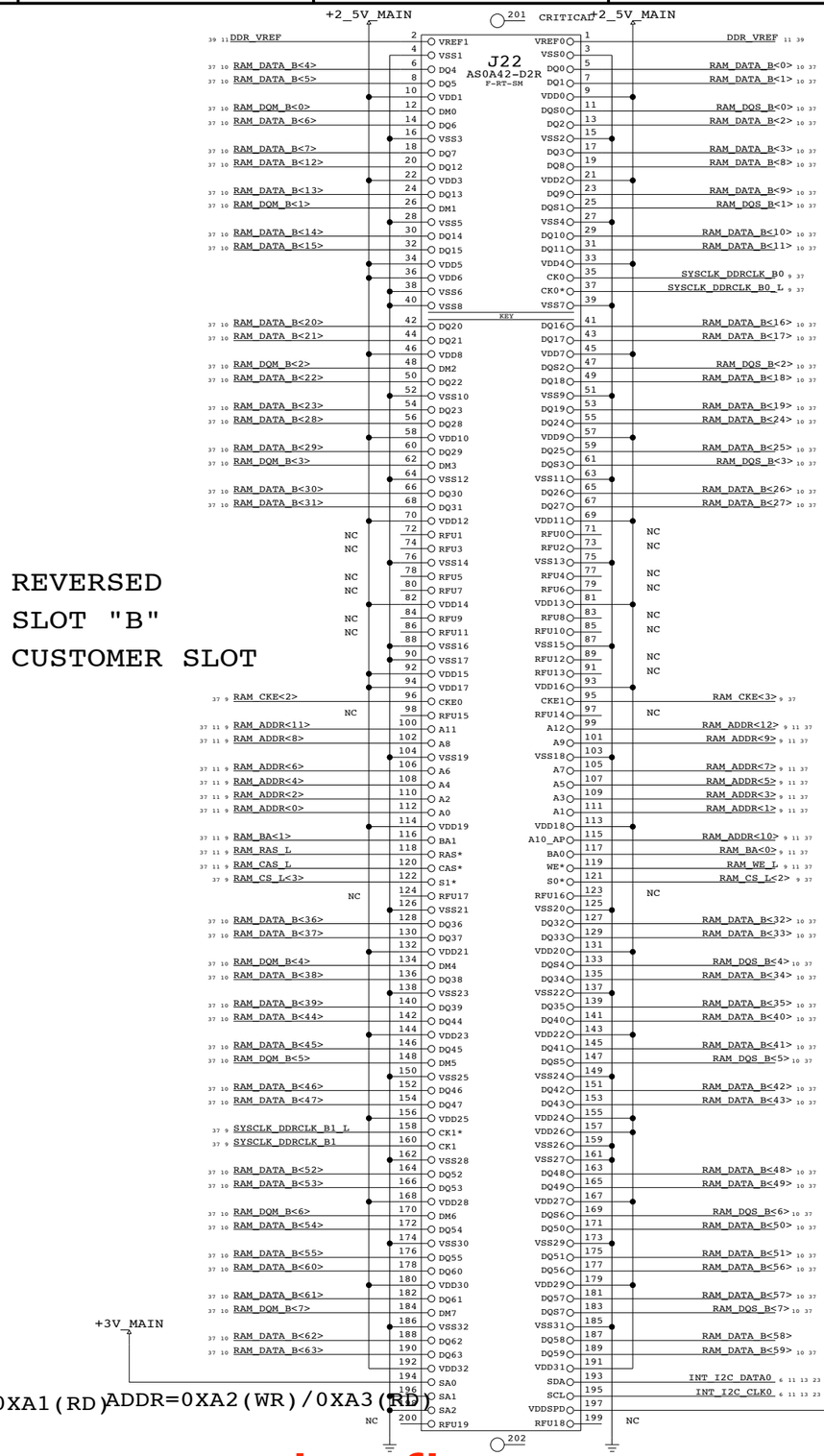
SCALE	SHT	OF
NONE	10	45



STANDARD

SLOT "A"

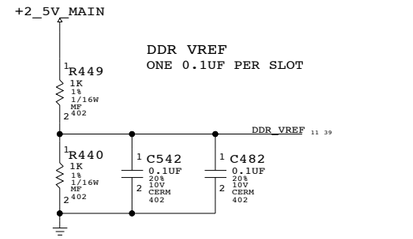
FACTORY SLOT

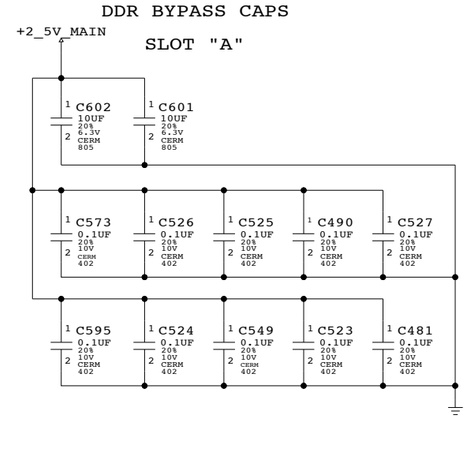


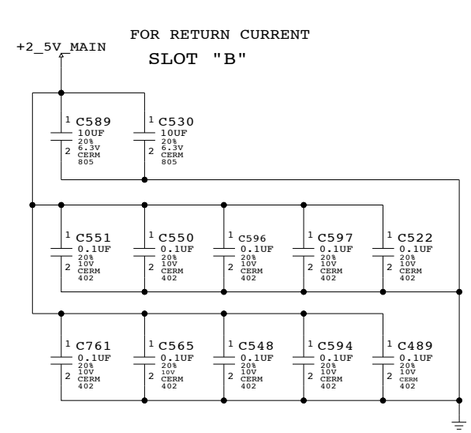
REVERSED

SLOT "B"

CUSTOMER SLOT







DDR SODIMM CONNS

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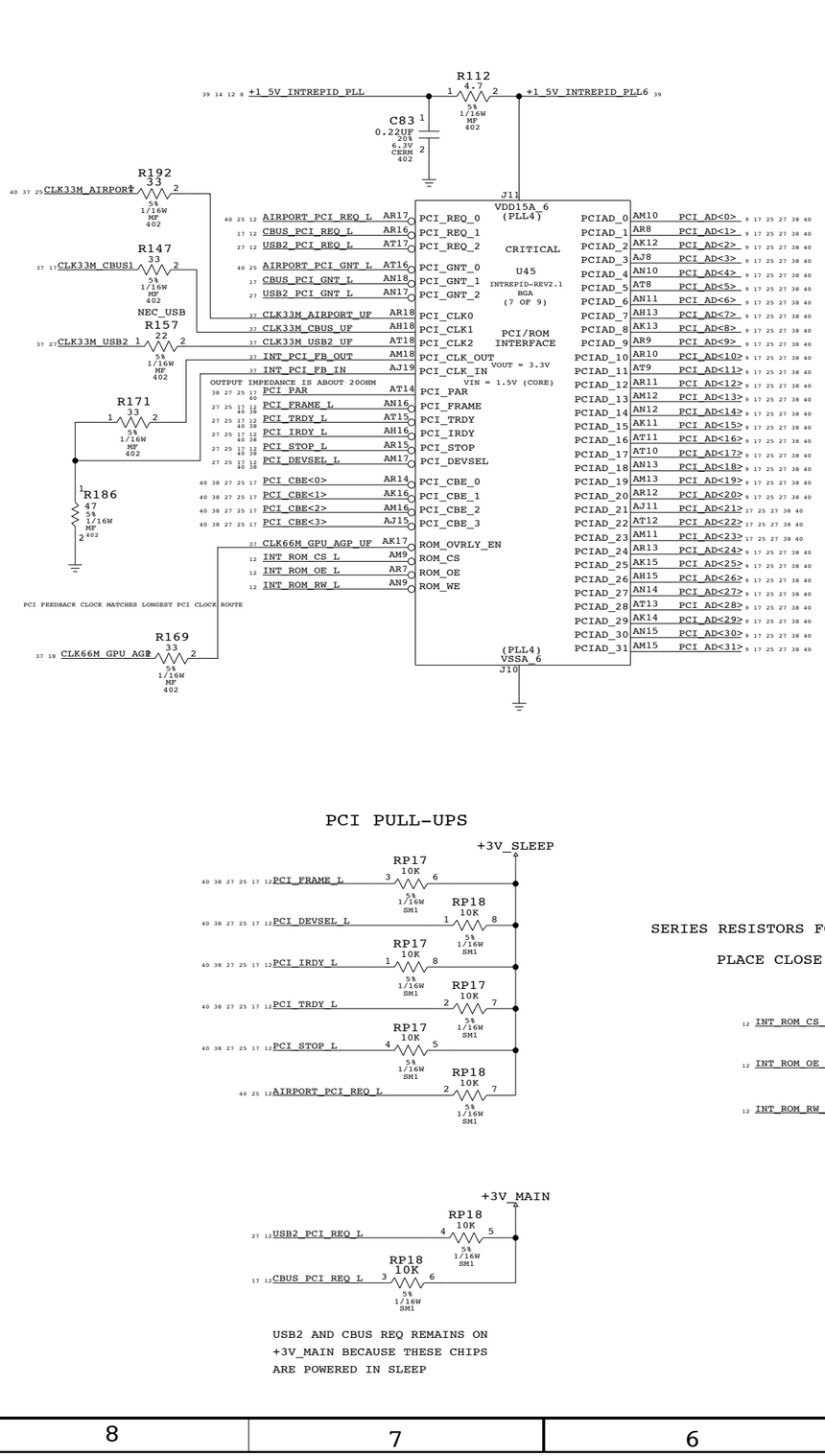
SIZE	DRAWING NUMBER	REV.
D	051-6694	02

SCALE	SHT	OF
NONE	11	45



INTREPID AGP/PCI

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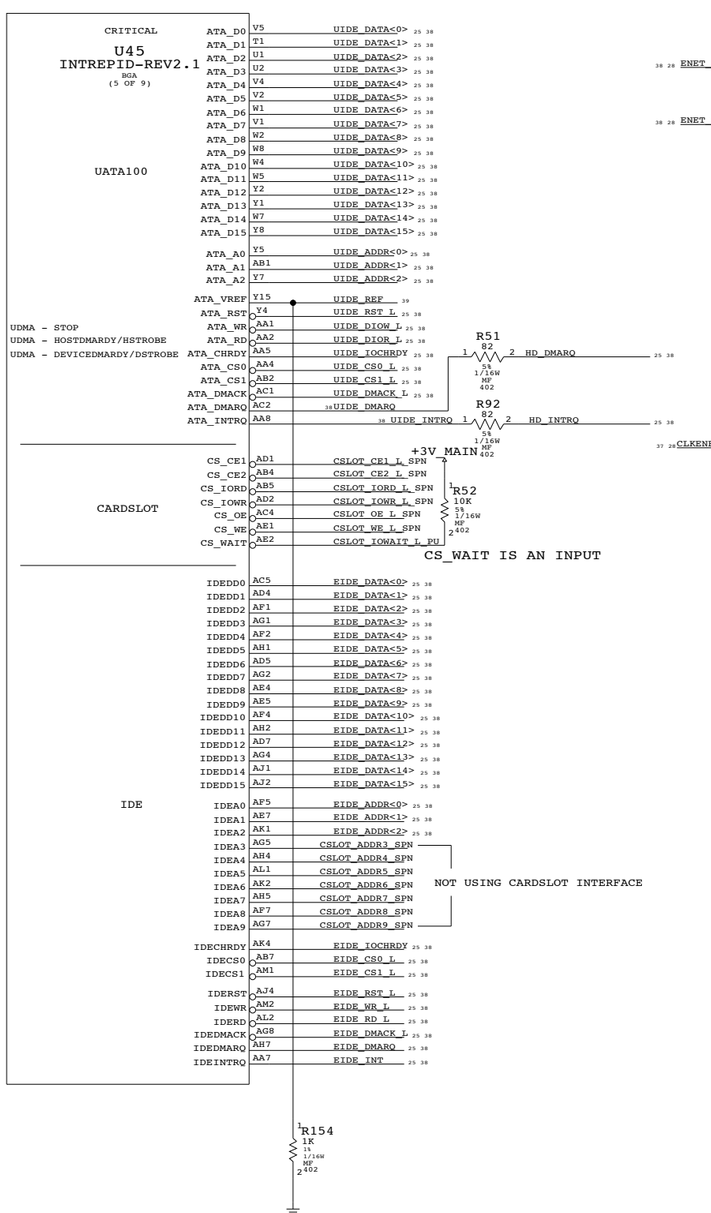
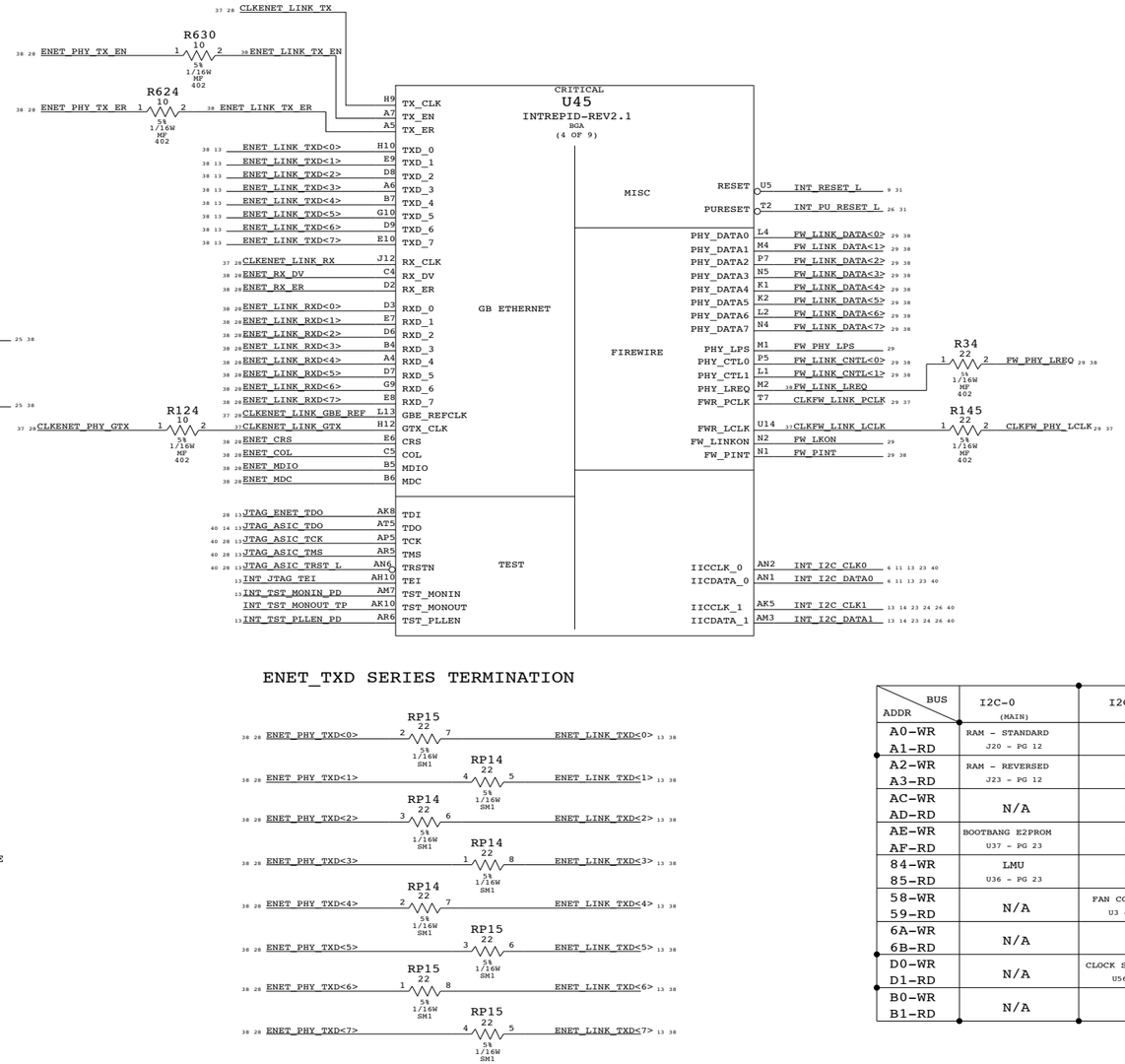
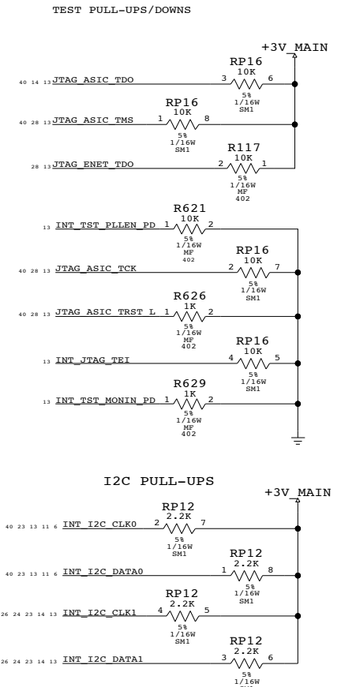
SIZE	DRAWING NUMBER	REV.
D	051-6694	02
SCALE: NONE	SHT 12 OF 45	







ENET_TXD SERIES TERMINATION

JTG_RSTN_L	TST_TEI_H	JTG_TDO_H (I/O)	JTG_TDI_H (I/O)	TST_PLLEN_H	ANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	EXTPLL SHUTDOWN (OUTPUT)	DDR_ TPDENABLE (OUTPUT)	0	(OUTPUT)	NORMAL OPERATION
0	0	(OUTPUT)	0(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	HMPLL_ TESTSEL5 (INPUT)	1(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0(I)	0(I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0(I)	1(I)	0	X(I)	ATPG IDDQ
0	1	0(I)	1(I)	1	X(I)	TEST TRI-STATE
0	1	1(I)	0(I)	0	X(I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1(I)	0(I)	1	X(I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1(I)	1(I)	X	X(I)	FUNCTIONAL TEST IDDQ

ADDR \ BUS	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
A0-WR A1-RD	RAM - STANDARD J20 - PG 12	N/A	N/A	N/A
A2-WR A3-RD	RAM - REVERSED J23 - PG 12	N/A	N/A	N/A
AC-WR AD-RD	N/A	N/A	DASH MODEM J9 - PG 25	N/A
AE-WR AF-RD	BOOTBANG E2PROM U37 - PG 23	N/A	N/A	N/A
84-WR 85-RD	LMU U36 - PG 23	N/A	N/A	N/A
58-WR 59-RD	N/A	FAN CONTROLLER U3 - PG 24	N/A	N/A
6A-WR 6B-RD	N/A	N/A	SNAPPER SOUND J12 - PG 24	N/A
D0-WR D1-RD	N/A	CLOCK SLEW SSCG U56 - PG 15	N/A	N/A
B0-WR B1-RD	N/A	MMM	N/A	N/A

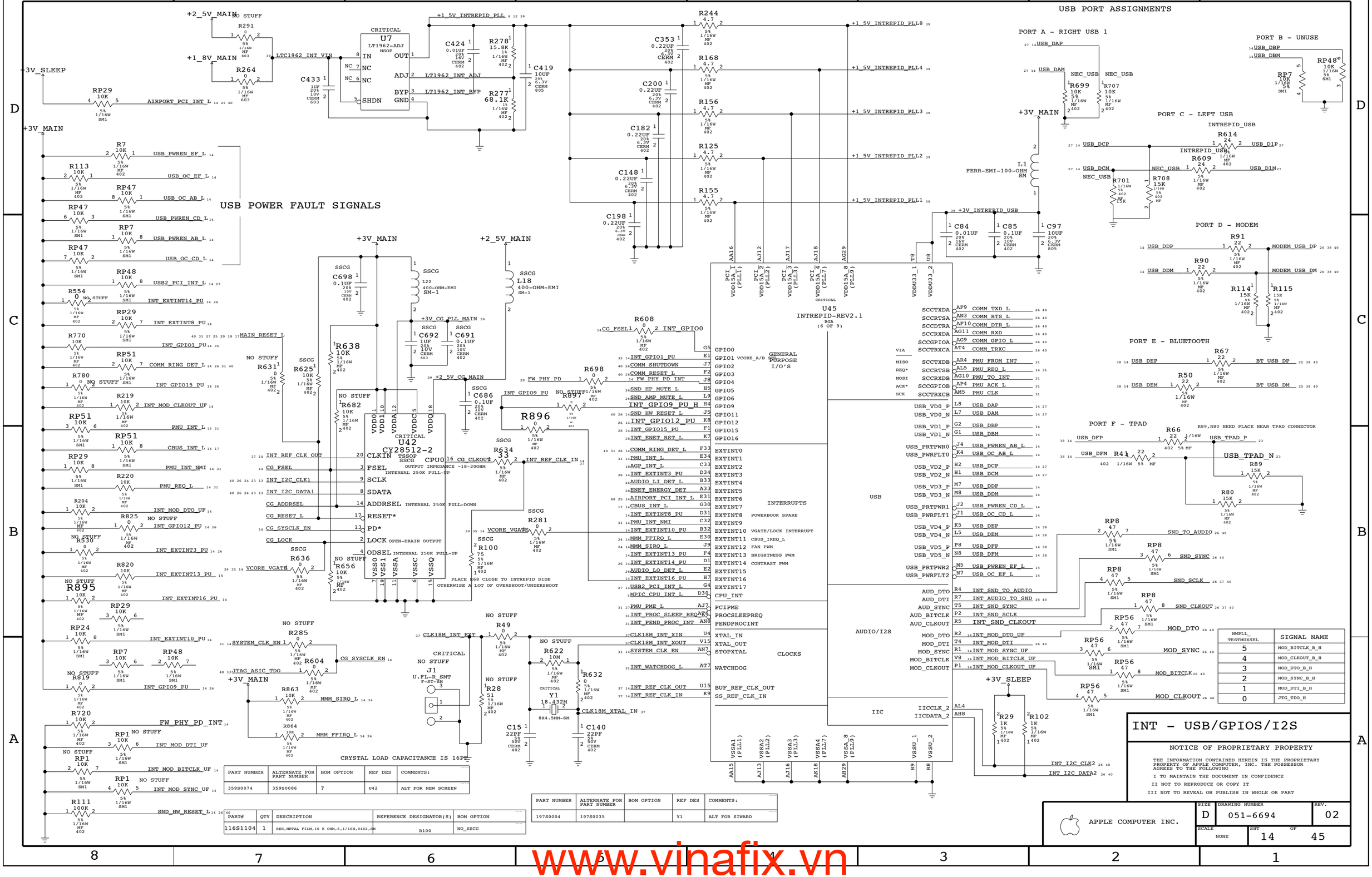
ADDR LSB INDICATES READ ('1') OR WRITE ('0') MODES

INT - ENET/FW/UATA EIDE/I2C

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	02

SCALE	SHT	OF
NONE	13	45

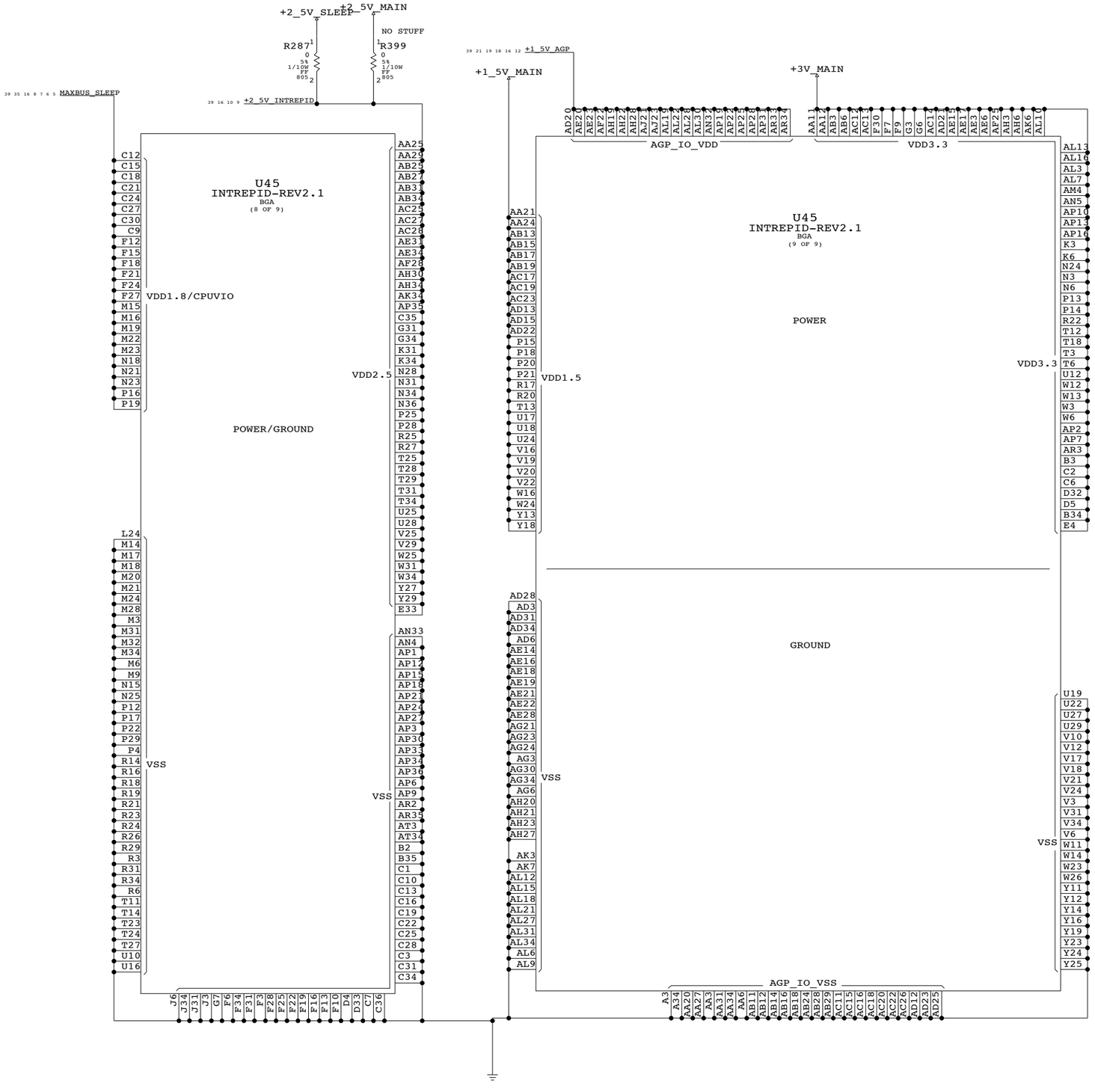


HWPLL_TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
359S0074	359S0086	?	U42	ALT FOR NEW SCREEN

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0004	197S0035		Y1	ALT FOR SIWARD

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES,METAL FILM,10 K OHM,5,1/16W,0402,SM	R100	NO_SSCG



Intrepid Power

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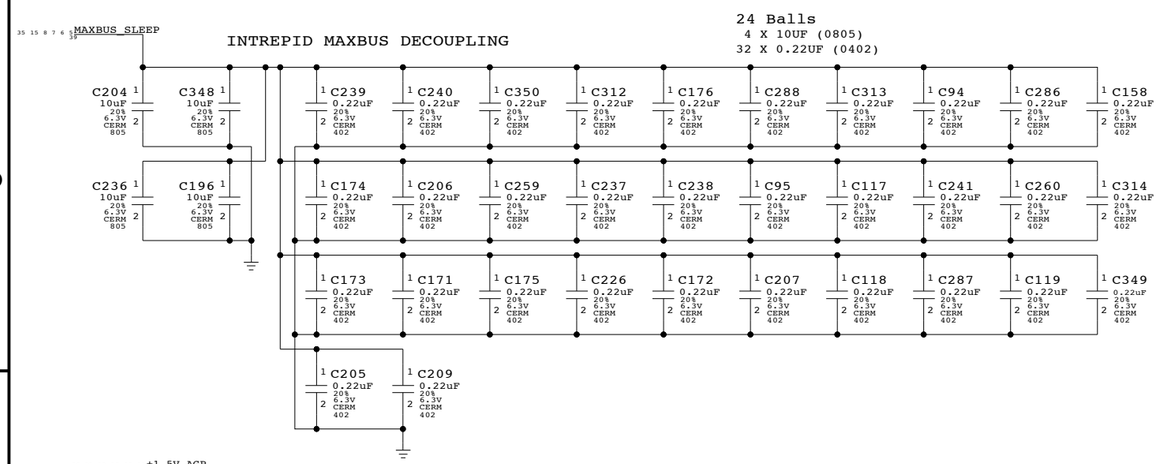
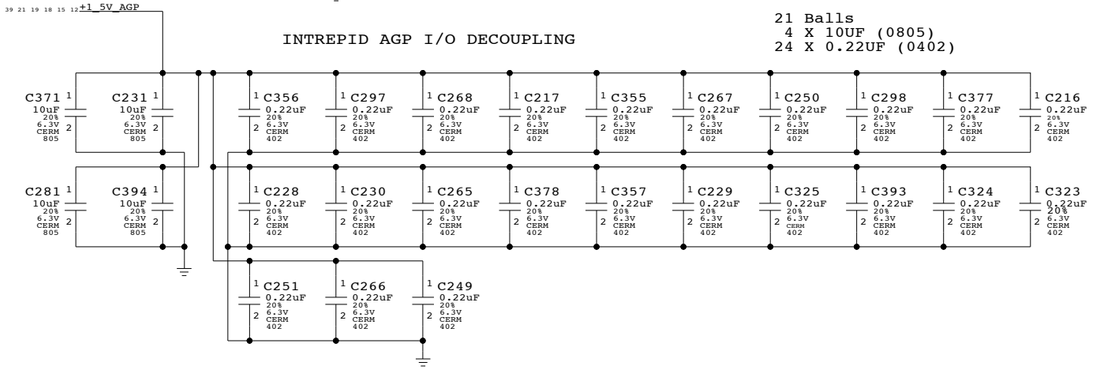
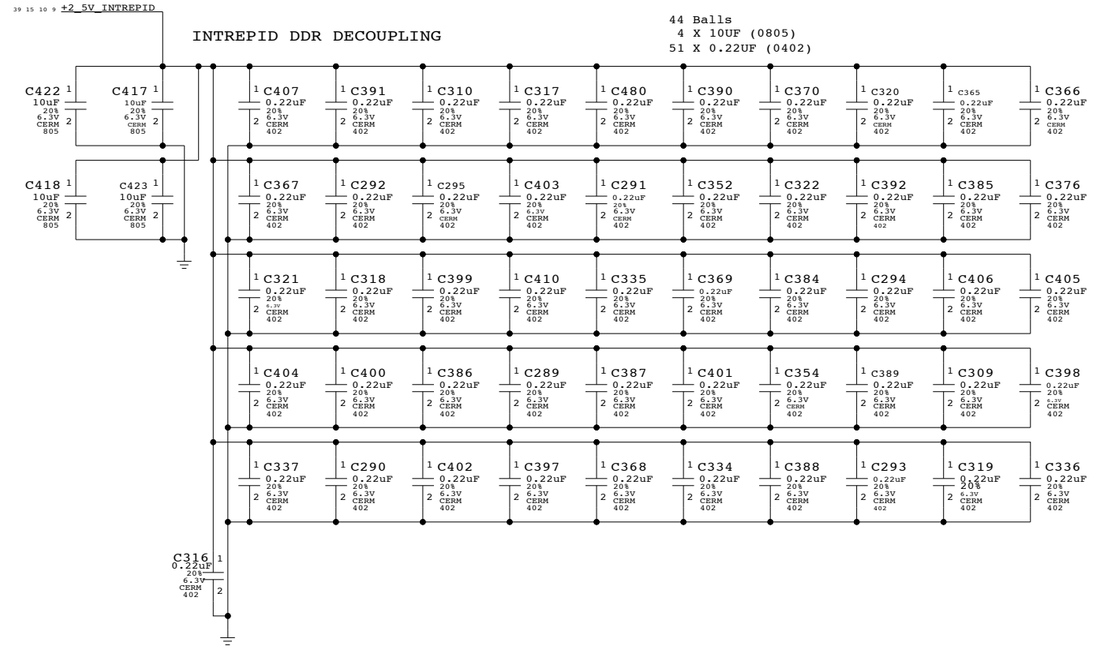
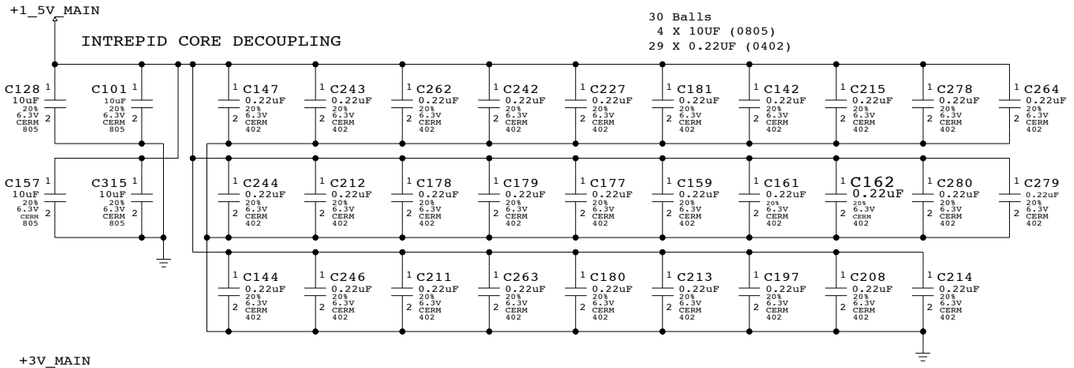
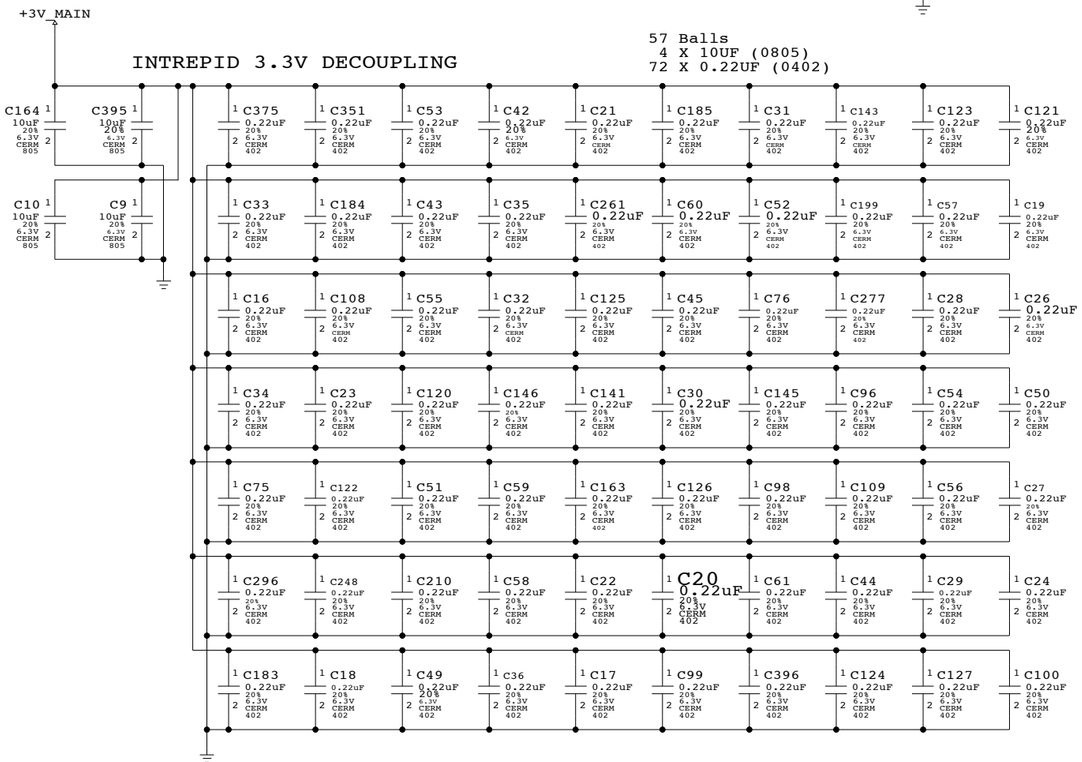
SIZE	DRAWING NUMBER	REV.
D	051-6694	02
SCALE: NONE	SHT 15 OF 45	









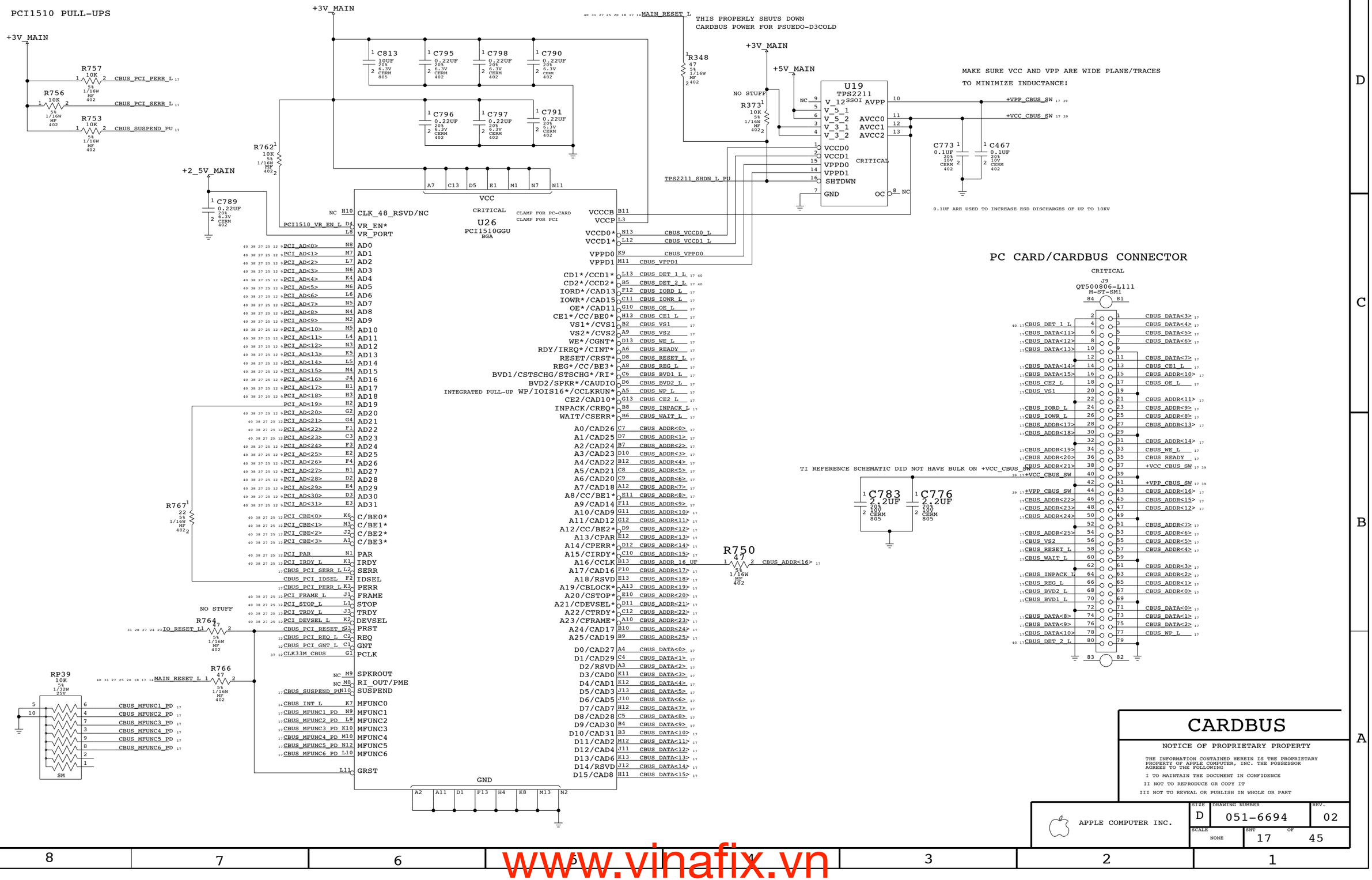


Intrepid Decoupling

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	02

SCALE	SHT	OF
NONE	16	45



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0158	1	IC,ATI,M11-CSP128,GRPHCTLR,667BGA	U44	CRITICAL	M11_CSP128
338S0154	1	IC,ATI,M11-CSP64,GRPHSCTLR,667BGA	U44	CRITICAL	M11_CSP64

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0182	338S0158	M11_CSP128	U44	ALT FOR A16
338S0183	338S0154	M11_CSP64	U44	ALT FOR A16

27M OSC

(PLACE THE OSCILLATOR AND R189 AND R195 CLOSE TO ATI PIN AJ29)

+3V_SLEEP

L4 FERR-EMI-100-OHM SM

+3V_ATI_OSC_SLEEP

C77 0.1uF 20% 10V CERM 402

C78 4.7uF 20% 6.3V CERM 805

NO STUFF R188 100K 5% 1/16W MF 402

CRITICAL G2 27.0000M OSC SM-1

VCC OE OUT GND

ATI_OSC_OE

ATI_CLK27M_OSC

(PLACE R200 CLOSE TO OSC) GPU_SS R200 0 5% 1/16W MF 402

ATI_CLK27M_OSC_SS

R189 287 1% 1/16W MF 402

R195 162 1% 1/16W MF 402

ATI_CLK27M_IN

S0=1;S1=M => -1.5% DOWN-SPREAD

SPREAD SPECTRUM SUPPORT

+3V_SLEEP

GPU_SS L3 FERR-EMI-100-OHM SM

+3V_ATI_SS

GPU_SS C70 10uF 20% 6.3V CERM 805

GPU_SS C71 0.1uF 20% 10V CERM 402

NO STUFF R173 0 5% 1/16W MF 402

GPU_SS R181 0 5% 1/16W MF 402

GPU_SS CRITICAL

U47 CY25811 SOI

XIN/CLKIN XOUT SSCLK FRSEL S1 S0 VDD VSS

ATI_CLK27M_OSC_SS

ATI_SSCLK_UF

GPU_SS R201 33 5% 1/16W MF 402

ATI_SSCLK_IN

CY25811_S1

CY25811_S0

NO STUFF R37 0 5% 1/16W MF 402

NO STUFF R38 0 5% 1/16W MF 402

U44 RAGE MOBILITY M11-CSP64 64MB BGA (1 OF 6)

AGP_AD<31:0> AGP_AD<31> AB30 … AGP_AD<0> K28

AGP_CBE<3:0> W28 U29 R30 N27

CLK66M_GPU_AGP AG30

AGP_FRAME_L U27

AGP_IRDY_L T30

AGP_TRDY_L T28

AGP_STOP_L T27

AGP_DEVSEL_L T29

AGP_PAR R28

AGP_REQ_L AF29

AGP_GNT_L AF27

AGP_INT_L AH29

AGP_ATI_RESET AH30

AGP_WBF_L AE27

AGP_ATI_VREFG AK3

AGP_ATI_VREF D8

AD_STB0 N29 AGP_AD_STB<0>

AD_STB1 W29 AGP_AD_STB<1>

AD_STBB0 M28 AGP_AD_STB_L<0>

AD_STBB1 Y29 AGP_AD_STB_L<1>

AGP_BUSYB AG28 AGP_BUSY_L

AGPREF K30

AGPTEST K29 GPU_AGP_TEST

AGP8X_DETB U25 AGP8X_DET_PU

SUS_STAT AJ28 AGP_SUS_STAT_L_PU

ST0 AF30 AGP_ST<0>

ST1 AF28 AGP_ST<1>

ST2 AE29 AGP_ST<2>

SBA7 AC28 AGP_SBA<7>

SBA6 AB29 AGP_SBA<6>

SBA5 AC27 AGP_SBA<5>

SBA4 AC30 AGP_SBA<4>

SBA3 AD27 AGP_SBA<3>

SBA2 AD30 AGP_SBA<2>

SBA1 AE28 AGP_SBA<1>

SBA0 AD29 AGP_SBA<0>

RBFB AE30 AGP_RBF_L

STP_AGPB AG29 AGP_STP_L

SB_STB AC29 AGP_SB_STB

SB_STBS AD28 AGP_SB_STB_L

RSTB_MSK AD24 ATI_RSTB_MSK

DBI_LO Y25 ATI_DBI_LO_PU

DBI_HI Y27 ATI_DBI_HI_PU

TEST_YCLK E8

TEST_MLCK J6 (PULL-UP to GPU_MEM_IO)

MEMTEST C8 ATI_MEMTEST

PLLTEST AC22 NC

CBEB3 CBEB2 CBEB1 CBEB0 PCICLK FRAMEB IRDYB TRDYB STOPB DEVSELB PAR REQB GNTB INTAB RSTB WBF VREFG MVREF

VSS

D+ AC10 GPU_THERM_DP_TP

D- AC11 GPU_THERM_DM_TP

+GPU_MEM

OMIT

R119 47 5% 1/16W MF 402 +1_5V_AGP

R127 10K 5% 1/16W MF 402 +3V_GPU

R159 20K 5% 1/16W MF 402

INT_AGP_VREF

C62 0.1uF 20% 10V CERM 402

C63 0.01uF 20% 16V CERM 402

(PLACE C1002 CLOSE TO AGPREF PIN)

R172 20K 5% 1/16W MF 402 +3V_GPU

R158 0 5% 1/16W MF 402

R126 47K 5% 1/16W MF 402 +1_5V_AGP

R138 47K 5% 1/16W MF 402

R118 45.3 1% 1/16W MF 402

U44 RAGE MOBILITY M11-CSP64 64MB BGA (6 OF 6)

OMIT

VSS VDDCI U6

GPU_VCORE L2 60-OHM-EMI SM +GPU_VCORE_VDDCI

C64 0.01uF 20% 16V CERM 402

C67 10uF 20% 6.3V CERM 805

C65 0.01uF 20% 16V CERM 402

C68 0.01uF 20% 16V CERM 402

C66 0.01uF 20% 16V CERM 402

C69 0.01uF 20% 16V CERM 402

U44 RAGE MOBILITY M11-CSP64 64MB BGA (2 OF 6)

OMIT

VSS

MAIN_RESET_L IS TOGGLED FOR SLEEP

MAIN_RESET_L R53 47 5% 1/16W MF 402 R54 10K 5% 1/16W MF 402 +3V_GPU

R43 1K 1% 1/16W MF 402 +3V_GPU

R44 1K 1% 1/16W MF 402 +GPU_MEM

R45 1K 1% 1/16W MF 402

PLACE VERF VOLTAGE DIVIDER CLOSE TO ATI M10 VREF PIN

R46 1K 1% 1/16W MF 402

C11 0.1uF 20% 10V CERM 402

C37 10uF 20% 6.3V CERM 805

+1_8V_GPU

ATI_MEMIO_LO R55 4.7K 5% 1/16W MF 402

ATI_MEMIO_HI R104 4.7K 5% 1/16W MF 402

ATI_MEMVMODE0 B7 MEMVMODE0

ATI_MEMVMODE1 B6 MEMVMODE1

ATI_MEMIO_HI R70 4.7K 5% 1/16W MF 402

ATI_MEMIO_LO R105 4.7K 5% 1/16W MF 402

FOR 2.5 VDDR1
MEMVMODE0=1.8V
MEMVMODE1=GND

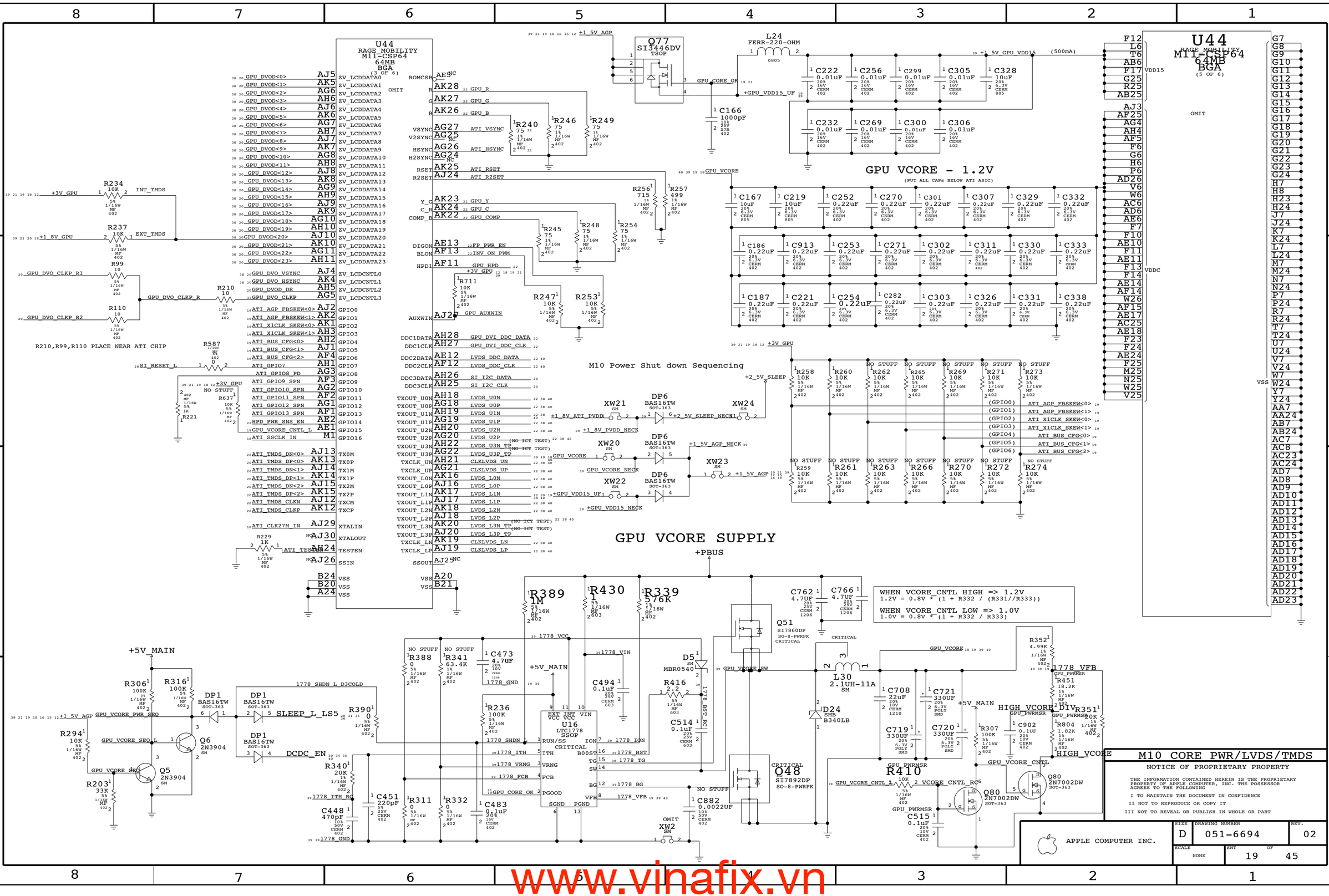
FOR 1.8 VDDR1
MEMVMODE0=GND
MEMVMODE1=1.8V

M10 AGP INTERFACE

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	02

SCALE	SHT	OF
NONE	18	45



Page Notes

Power aliases required by this page:
(None)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: TMDS

Line To Line:	15 mils
Length Tolerance:	50 mils
Primary Max Sep:	10 mils
Secondary Max Sep:	100 mils
Secondary Length:	250 mils

NOTE: Target differential impedance for TMDS data pairs is 100 ohms.

INTERNAL TMDS TERMINATION

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN
CMF LINE SHOULD BE ROUTED AS 4MIL SURFACE
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS

EXTERNAL TMDS TERMINATION

L13,L14,L15 PLACE NEAR DVI CONNECTOR

I2C ADDR. MASTER = 0X70

I2C ADDR. SLAVE = 0X72

SILICON IMAGE TMDS

SIZE	D
DRAWING NUMBER	051-6694
REV.	02
SCALE	NONE
SHT	20
OF	45

SIL_178

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GPU POWER SOURCES - 1.5V, 1.8V, 2.5V & 3.3V

GPU PLL - 1.8V

AGP 4X I/O - 1.5V

MEMORY CORE - 2.5V

LVDS PLL - 1.8V

MEMORY PLL - 1.8V

LVDS - 2.5V

LVDS/TMDS - 1.8V

MEMORY I/O

3.3V IO SUPPLY

(Max Current varies, depends on usage)

M10 SHUT DOWN POWER SEQUENCING

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S0828	1	IC,MAX8860,LDO,2.77V	U8	?

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0647	353S0828	?	U8	ALT FOR 2.82V PART

M10 POWER		
NOTICE OF PROPRIETARY PROPERTY		
APPLE COMPUTER INC.	SIZE: D	DRAWING NUMBER: 051-6694
	SCALE: NONE	SHT: 21 OF 45
		REV: 02

EXTERNAL VIDEO (DVI) INTERFACE

ANALOG FILTERING — PLACE CLOSE TO CONNECTOR

FL2 LCFILTER (CRITICAL) — GPU_B → VGA_B
FL1 LCFILTER (CRITICAL) — GPU_G → VGA_G
FL3 LCFILTER (CRITICAL) — GPU_R → VGA_R
SM-220MHZ

C685 3.3PF 0.25% 50V CERM 402
C676 3.3PF 0.25% 50V CERM 402
C684 3.3PF 0.25% 50V CERM 402

+3V_MAIN

U56 74AHC1G32 SM (CRITICAL) — ATI_HSYNC → VGA_HSYNC_BUF → R718 33 5% 1/16W MF 402 → VGA_HSYNC
U57 74AHC1G32 SM (CRITICAL) — ATI_VSYNC → VGA_VSYNC_BUF → R687 33 5% 1/16W MF 402 → VGA_VSYNC

VGA VSYNC BUFFERS

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)

+5V_SLEEP → F1 0.5AMP-13.2V SM → +5V_DDC_SLEEP_UF → L23 400-OHM-EMI SM-1 → +5V_DDC_SLEEP
Isolation required for DVI power switch

D21 MBR0530 SM — DDC_CLK_ISO
R655 4.7K 5% 1/16W MF 402
R661 4.7K 5% 1/16W MF 402

J14 QH1112 F-RT-TH (CRITICAL)

TMDS_CONN_DN<0>	17	1	TMDS_CONN_DN<2>
TMDS_CONN_DP<0>	18	9	TMDS_CONN_DN<1>
	19	2	TMDS_CONN_DP<2>
TMDS_CONN_DN<5>	20	10	TMDS_CONN_DP<1>
TMDS_CONN_DP<5>	21	3	TMDS_CONN_DN<4>
	22	11	TMDS_CONN_DN<3>
TMDS_CONN_CLKP	23	4	TMDS_CONN_DP<4>
TMDS_CONN_CLKN	24	12	TMDS_CONN_DP<3>
VGA_B	C3	5	DVI_DDC_CLK_UF
VGA_HSYNC	C5B	13	(+5V_DDC_SLEEP)
	C4	6	DVI_DDC_DATA_UF
		14	VGA_VSYNC
		7	DVI_HPD_UF
	C1	15	VGA_R
	C5A	8	VGA_G
	C2	16	
	34	32	
		35	

R670 100 5% 1/16W MF 402 — DVI_DDC_CLK
R649 100 5% 1/16W MF 402 — DVI_DDC_DATA
R650 100 5% 1/16W MF 402 — DVI_HPD

C706 100PF 5% 50V CERM 402
C669 100PF 5% 50V CERM 402
C1 100PF 5% 50V CERM 402
C710 0.01UF 20% 50V CERM 603

R706 0 5% 1/16W MF 402 — PLACE NEAR 3, 11 & 19
R1 0 5% 1/16W MF 402 — PLACE NEAR C5A & C5B

CHGND1 CHGND5

NOTE: Pulldown for DVI_HPD provided by DVI power switch interface
NOTE: DVI_HPD SHARES Q68 WITH ALS BECAUSE OF BOARD REAL ESTATE

3V LEVEL SHIFTERS

+3V_SLEEP

Q38 2N7002DW SOT-363 — DVI_DDC_CLK → GPU_DVI_DDC_CLK
Q38 2N7002DW SOT-363 — DVI_DDC_DATA → GPU_DVI_DDC_DATA
Q35 2N7002DW SOT-363 — DVI_HPD → GPU_HPD

R662 10K 5% 1/16W MF 402
R671 10K 5% 1/16W MF 402
R694 100K 5% 1/16W MF 402

DVI POWER SWITCH

Power key detect path when system is shutdown or asleep.. DDC_CLK is isolated from NV17M DURING SHUTDOWN. WHEN power key on remote device is pressed, 5V will be driven into DDC_CLK. Since host rails will be low, TP0610 will turn on, driving SOFT_PWR_ON_L low. As host rails rise, TP0610 will turn off, as will remote device path into DDC_CLK. Isolation will be disabled as well.

Q40 TP0610 SM — DVI_DDC_CLK_UP → DVI_TURN_ON → DVI_TRUN_ON_ILIM → +5V_DDC_SLEEP
R690 680 5% 1/16W MF 402
R688 330 5% 1/16W MF 402 — Pulldown prevents 3904 from turning on when DVI monitor has active, self-powered DDC clock pullup.
R691 10K 5% 1/16W MF 402
Q42 2N3904 SM — DVI_TURN_ON_BASE
SOFT_PWR_ON_L

Power key detect path when system is running. HPD normally driven to 3.3V. When power key on remote device pressed, HPD will be driven to 5V. COMPARATOR ENABLED BY NV17MAP GPIO.

+3V_SLEEP

R680 68.1K 1% 1/16W MF 402
C696 0.1UF 20% 10V CERM 402
HPD_4V_REF

U46 LMC7211 SM (CRITICAL)
R663 10K 1% 1/16W MF 402 — DVI_HPD_UF1 → DVI_HPD_DIV
R686 10K 1% 1/16W MF 402
R681 100K 1% 1/16W MF 402

HPD_PWR_SW
Q41 2N7002DW SOT-363 — HPD_ON
R703 330 5% 1/16W MF 402

+PBUS
Q45 TP0610 SM — COMP_ENABLE
R696 100K 5% 1/16W MF 402
R704 100K 5% 1/16W MF 402
COMP_DISABLE
HPD_ON_RC
R700 20K 5% 1/16W MF 402 — HPD_BASE
Q44 2N3904 SM
C703 47UF 20% 6.3V CERM 1210
R705 68K 5% 1/16W MF 402

NEED PULL-DOWN BECAUSE THIS SIGNAL IS TRISTATED INITIALLY
Q41 2N7002DW SOT-363 — HPD_PWR_SNS_EN
R213 100K 5% 1/16W MF 402

TMDS FILTERING

PLACE CLOSE TO CONNECTOR

L72 90-OHM-300MA 2012H (CRITICAL) — TMDS_DN<0> → TMDS_CONN_DN<0>; TMDS_DP<0> → TMDS_CONN_DP<0>
L21 165-OHM SM (CRITICAL) — TMDS_CLKP → TMDS_CONN_CLKP; TMDS_CLKN → TMDS_CONN_CLKN
L73 90-OHM-300MA 2012H (CRITICAL) — TMDS_DN<1> → TMDS_CONN_DN<1>; TMDS_DP<1> → TMDS_CONN_DP<1>
L74 90-OHM-300MA 2012H (CRITICAL) — TMDS_DN<2> → TMDS_CONN_DN<2>; TMDS_DP<2> → TMDS_CONN_DP<2>

S-VIDEO/COMP OUT INTERFACE

Place GND shorts at graphics controller

XW12 SM — GPU_TV_GND1 → L26 FERR-10-OHM-500MA SM → TV_GND1
L25 3.3UH 0603 — GPU_Y → TV_C
L29 3.3UH 0603 — GPU_C → TV_Y
L27 3.3UH 0603 — GPU_COMP → TV_COMP
XW13 SM — GPU_TV_GND2 → L28 FERR-10-OHM-500MA SM → TV_GND2

C712 0.01UF 20% 50V CERM 603
C702 560PF 10% 50V CERM 402
C707 560PF 10% 50V CERM 402
C718 560PF 10% 50V CERM 402
C724 560PF 10% 50V CERM 402
C714 560PF 10% 50V CERM 402
C713 560PF 10% 50V CERM 402
C717 0.01UF 20% 50V CERM 603

J15 MINIDIN RT-TH MH1177 (CRITICAL)

Place GND shorts at graphics controller

CHGND1

LCD POWER SWITCHES

+3V_MAIN

R400 100K 5% 1/16W MF 402
C484 2200PF 5% 50V CERM 603
R391 100K 5% 1/16W MF 402 — LCD_PWREN_D
LCD_DIGON_D
Q11 TSOP SI3443DV — +3V_LCD_SW
Q8 2N7002 SM — FP_PWR_EN
L6 FERR-250-OHM SM
C474 0.001uF 20% 50V CERM 402

CHGND4

LCD INTERFACE

LVDS INTERFACE

100K pull-ups are for no-panel case (development) Panel has 2K pull-ups

+3V_SLEEP
R342 100K 5% 1/16W MF 402 — LVDS_DDC_CLK
R320 100K 5% 1/16W MF 402 — LVDS_DDC_DATA
NO STUFF
C449 0.001uF 20% 50V CERM 402
C452 0.001uF 20% 50V CERM 402

C416 0.001uF 20% 50V CERM 402

J6 G-501973 F-RT-SM (CRITICAL)

	1	2	+3V_LCD
	3	4	(LVDS DDC POWER)
	5	6	NC
	7	8	LVDS_L0N
	9	10	LVDS_L0P
	11	12	LVDS_L1N
	13	14	LVDS_L1P
	15	16	LVDS_L2N
	17	18	LVDS_L2P
	19	20	CLKLVDS_LN
	21	22	CLKLVDS_LP
	23	24	LVDS_U0N
	25	26	LVDS_U0P
	27	28	LVDS_U1N
	29	30	LVDS_U1P
	31	32	LVDS_U2N
	33	34	LVDS_U2P
			CLKLVDS_UN
			CLKLVDS_UP

C500 0.001uF 20% 50V CERM 402

CHGND4

INVERTER INTERFACE

+PBUS
L33 FERR-1K-OHM-EMI SM — +12_8V_INV
+5V_MAIN
Q7 FDG6324L SC70-6 — +5V_INV_UF_SW
L32 400-OHM-EMI SM-1 — +5V_INV_SW
R317 100K 5% 1/16W MF 402 — FP_PWR_EN
C440 10UF 20% 6.3V CERM 805
C746 0.001UF 20% 50V CERM 402
C749 0.001UF 20% 50V CERM 402
C739 0.001UF 20% 50V CERM 402
J7 SM-2MT (CRITICAL)
Q7 FDG6324L SC70-6 — FP_PWR_EN
L31 400-OHM-EMI SM-1 — BRIGHT_PWM
+3V_PMU
C552 0.1UF 20% 10V CERM 402
U24 74LVC32 TSSOP — INV_ON_PWM → BRIGHT_PWM_UF
INVERTER EXPECTS ACTIVE HIGH SIGNAL

CHGND2

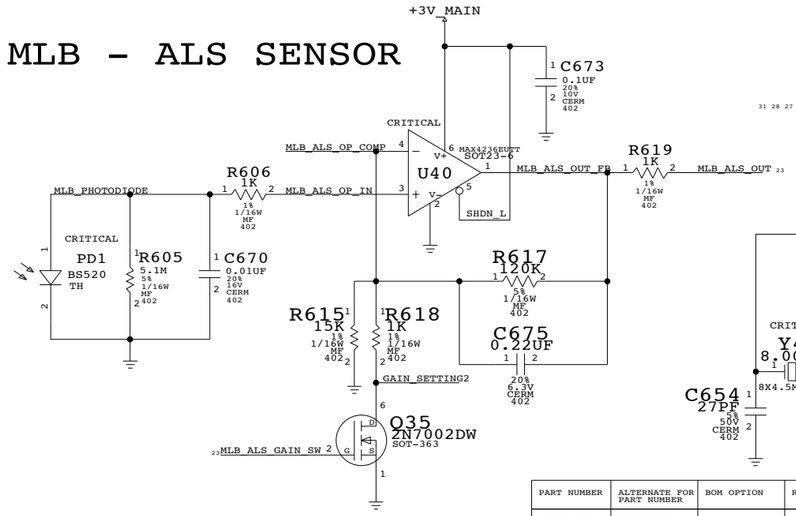
SHARES LOGIC WITH KB RESET SIGNALS (PG 28)
R724 0 5% 1/16W MF 402
C744 0.01UF 20% 50V CERM 603

CHGND2

VIDEO CONNECTORS

APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-6694 | REV. 02
SCALE NONE | SHT 22 OF 45

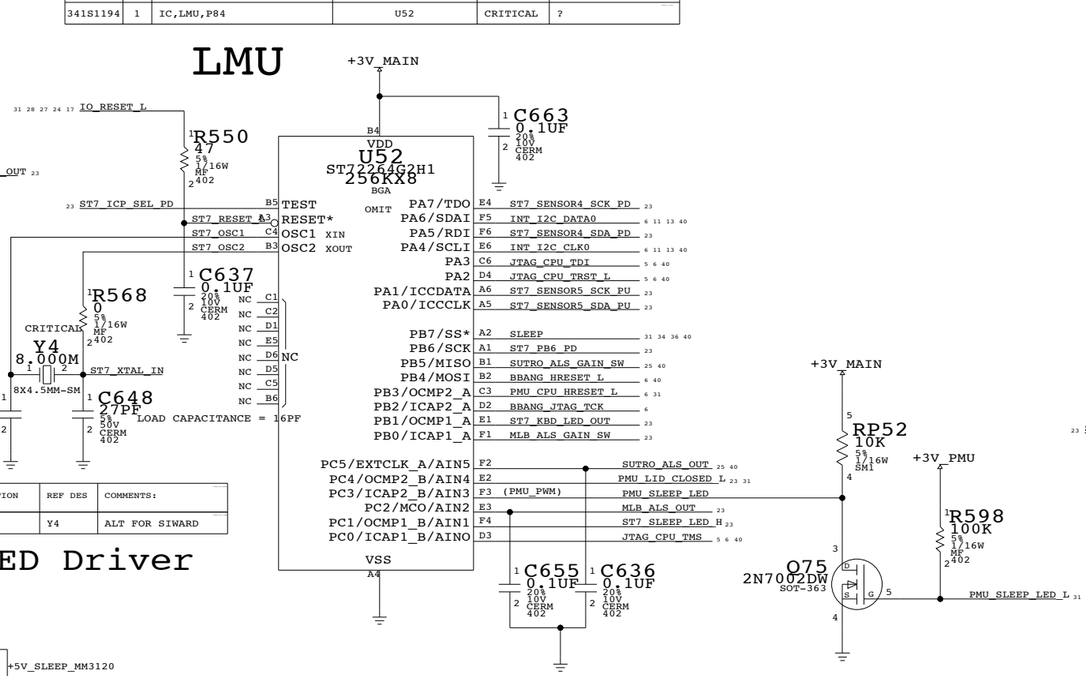
MLB - ALS SENSOR



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0856	353S0504	?	U40	ALT FOR SUPPLY PROBLEM

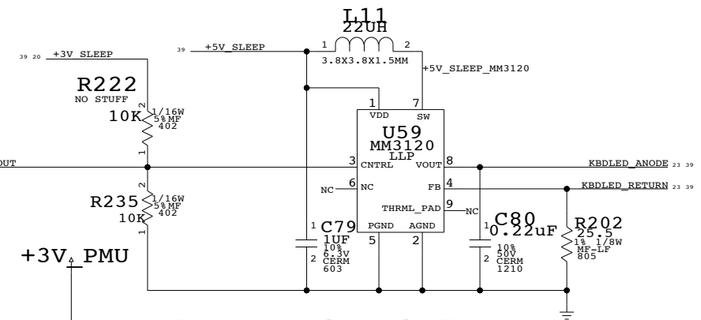
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1194	1	IC,LMU,P84	U52	CRITICAL	?

LMU



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0008	197S0040		Y4	ALT FOR SIWARD

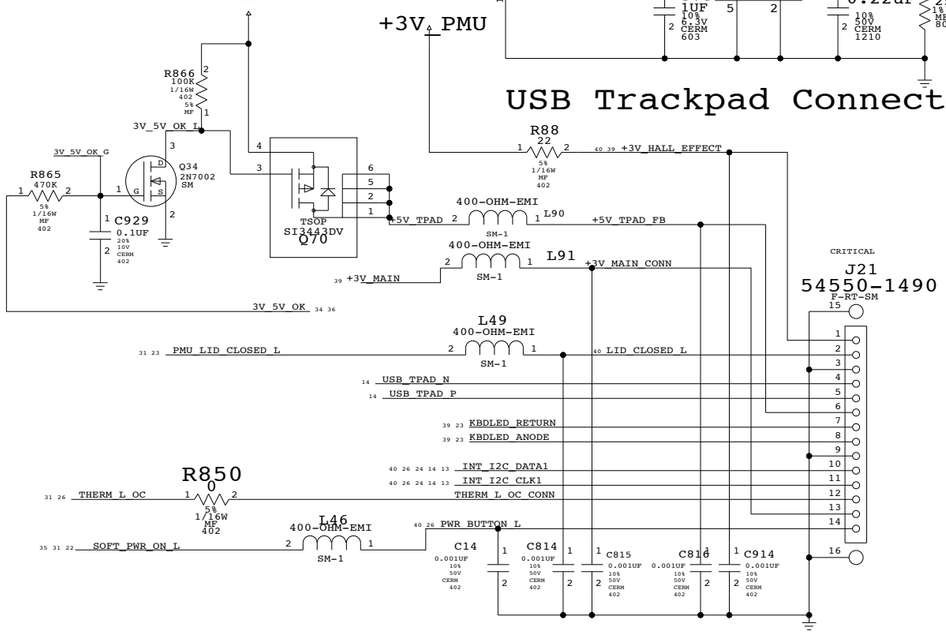
Keyboard LED Driver



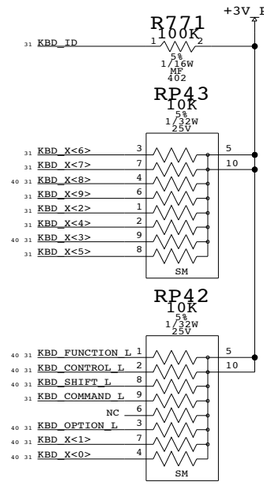
+5V_MAIN

+3V_PMU

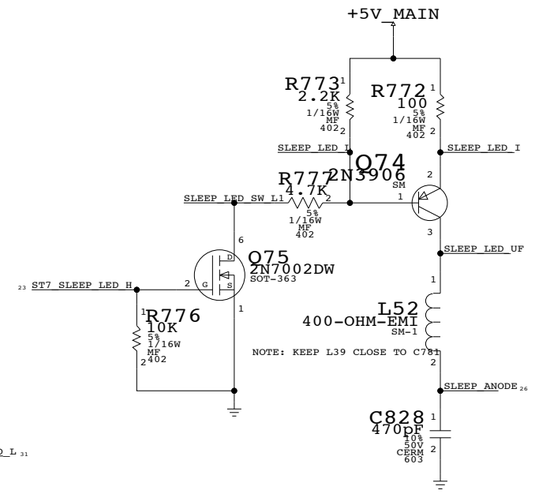
USB Trackpad Connector



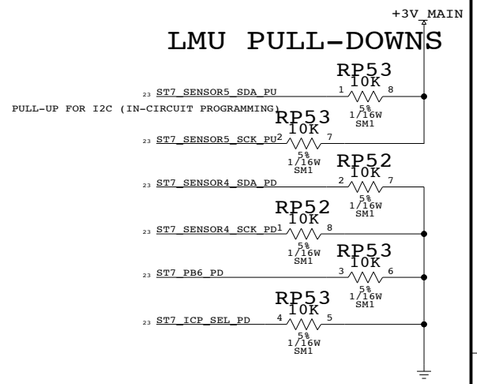
KEYBOARD PULLUPS



SLEEP LED



LMU PULL-DOWNS

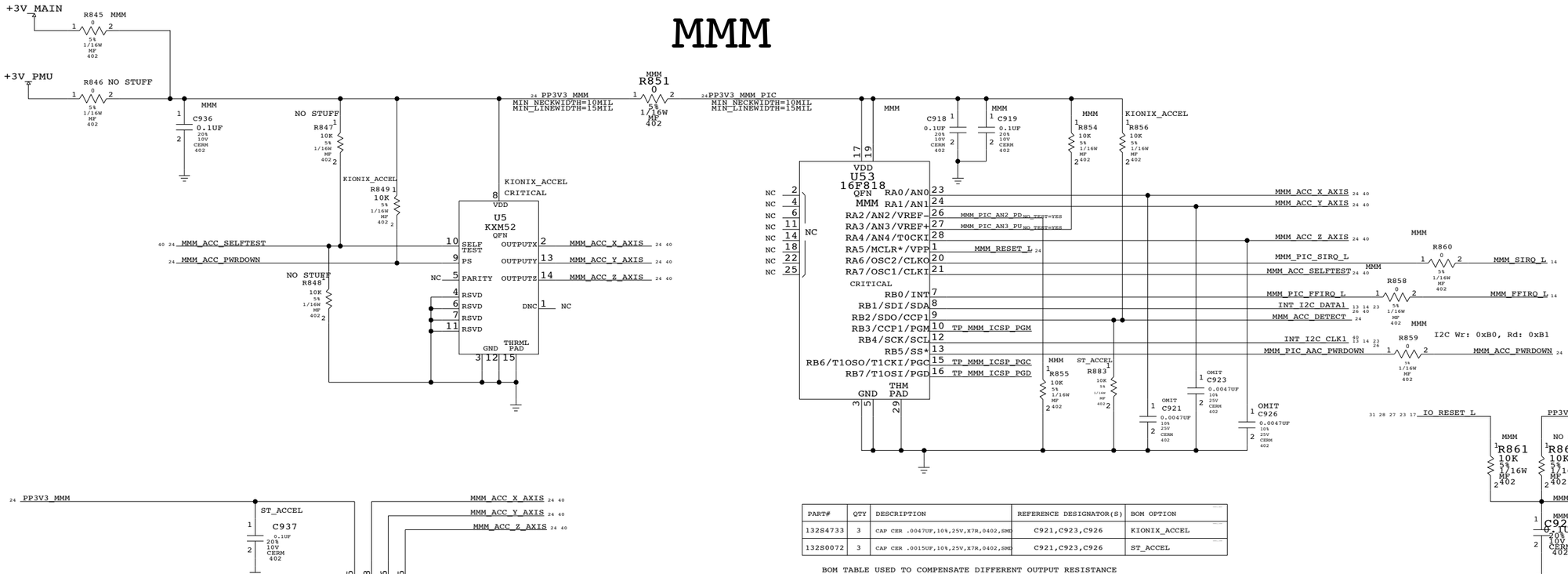


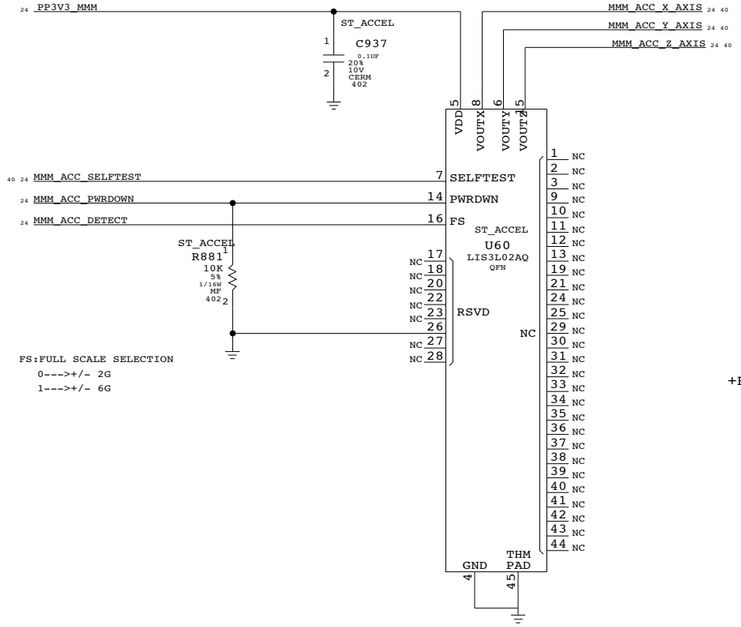
LMU/BOOTBANGER/SPIDEY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	?	02
SCALE: NONE	SHT 23 OF 45	

MMM

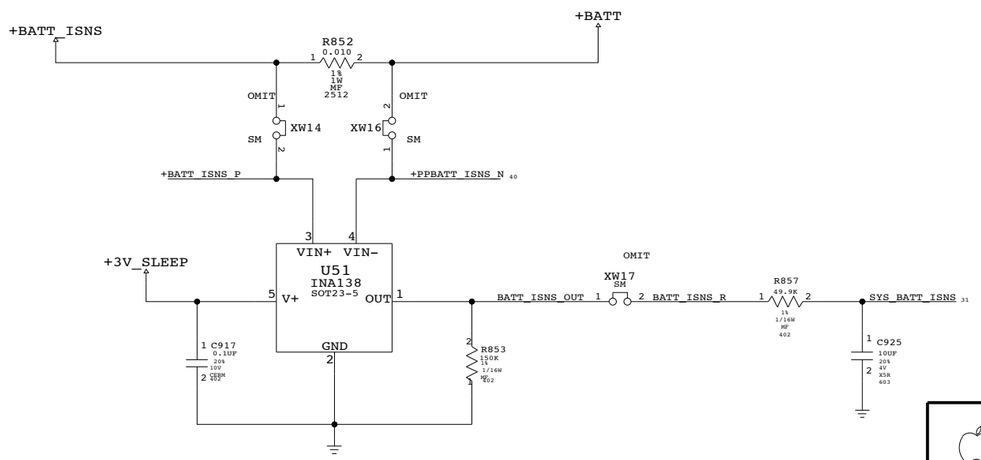




PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S4733	3	CAP CER .0047UF,10%,25V,X7R,0402,SMD	C921,C923,C926	KIONIX_ACCEL
132S0072	3	CAP CER .0015UF,10%,25V,X7R,0402,SMD	C921,C923,C926	ST_ACCEL

BOM TABLE USED TO COMPENSATE DIFFERENT OUTPUT RESISTANCE

BATTERY CURRENT SENSE



APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	?	02
SCALE: NONE	SHT 24 OF 45	

EIDE SERIES TERMINATION

PLACE TERMINATORS NEAR INTREPID

RP50 33 5% 1/16W SM1
- EIDE_DATA<8> ↔ EIDE_OPTICAL_DATA<8>

RP13 33 5% 1/16W SM1
- EIDE_DATA<10> ↔ EIDE_OPTICAL_DATA<10>

RP13 33 5% 1/16W SM1
- EIDE_DATA<9> ↔ EIDE_OPTICAL_DATA<9>

RP49 33 5% 1/16W SM1
- EIDE_DATA<11> ↔ EIDE_OPTICAL_DATA<11>

RP13 33 5% 1/16W SM1
- EIDE_DATA<12> ↔ EIDE_OPTICAL_DATA<12>

RP10 33 5% 1/16W SM1
- EIDE_DATA<14> ↔ EIDE_OPTICAL_DATA<14>

RP50 33 5% 1/16W SM1
- EIDE_DATA<13> ↔ EIDE_OPTICAL_DATA<13>

RP10 33 5% 1/16W SM1
- EIDE_DATA<15> ↔ EIDE_OPTICAL_DATA<15>

RP10 33 5% 1/16W SM1
- EIDE_DATA<2> ↔ EIDE_OPTICAL_DATA<2>

RP50 33 5% 1/16W SM1
- EIDE_DATA<1> ↔ EIDE_OPTICAL_DATA<1>

RP50 33 5% 1/16W SM1
- EIDE_DATA<0> ↔ EIDE_OPTICAL_DATA<0>

RP10 33 5% 1/16W SM1
- EIDE_DATA<3> ↔ EIDE_OPTICAL_DATA<3>

RP13 33 5% 1/16W SM1
- EIDE_DATA<6> ↔ EIDE_OPTICAL_DATA<6>

RP49 33 5% 1/16W SM1
- EIDE_DATA<7> ↔ EIDE_OPTICAL_DATA<7>

RP49 33 5% 1/16W SM1
- EIDE_DATA<4> ↔ EIDE_OPTICAL_DATA<4>

RP49 33 5% 1/16W SM1
- EIDE_DATA<5> ↔ EIDE_OPTICAL_DATA<5>

RP11 33 5% 1/16W SM1
- EIDE_CS0_L ↔ EIDE_OPTICAL_CS0_L

RP11 33 5% 1/16W SM1
- EIDE_ADDR<1> ↔ EIDE_OPTICAL_ADDR<1>

RP11 33 5% 1/16W SM1
- EIDE_ADDR<2> ↔ EIDE_OPTICAL_ADDR<2>

RP11 33 5% 1/16W SM1
- EIDE_ADDR<0> ↔ EIDE_OPTICAL_ADDR<0>

R36 10K 5% 1/16W MF 402 (to GND)

R31 33 5% 1/16W MF 402
- EIDE_CS1_L ↔ EIDE_OPTICAL_CS1_L

R116 82 5% 1/16W MF 402
- EIDE_DMARQ ↔ EIDE_OPTICAL_DMA_RQ

R95 22 5% 1/16W MF 402
- EIDE_DMACK_L ↔ EIDE_OPTICAL_DMAACK_L

R30 22 5% 1/16W MF 402
- EIDE_RD_L ↔ EIDE_OPTICAL_RD_L

R32 22 5% 1/16W MF 402
- EIDE_WR_L ↔ EIDE_OPTICAL_WR_L

R76 82 5% 1/16W MF 402
- EIDE_IOCHRDY ↔ EIDE_OPTICAL_IOCHRDY

R81 82 5% 1/16W MF 402
- EIDE_INT ↔ EIDE_OPTICAL_INT

R69 33 5% 1/16W MF 402
- EIDE_RST_L ↔ EIDE_OPTICAL_RST_L

WIRELESS INTERFACE

+3V_SLEEP

CONNECTOR HAS CHANGED
J20
CPB-7280-1210
M-ST-SM

MAIN_RESET_L	1	2	
RF_DISABLE_L_SPN	3	4	CLK33M_AIRPORT
AIRPORT_PCI_REQ_L	5	6	
	7	8	AIRPORT_PCI_GNT_L
PCI_AD<31>	9	10	AIRPORT_PME_L_TP
	11	12	AIRPORT_PCI_INT_L
PCI_AD<29>	13	14	PCI_AD<30>
PCI_AD<27>	15	16	
PCI_AD<25>	17	18	PCI_AD<28>
	19	20	PCI_AD<26>
PCI_CBE<3>	21	22	PCI_AD<24>
	23	24	AIRPORT_IDSEL
PCI_AD<23>	25	26	
PCI_AD<21>	27	28	PCI_AD<22>
PCI_AD<19>	29	30	PCI_AD<20>
	31	32	PCI_PAR
PCI_AD<17>	33	34	PCI_AD<18>
	35	36	PCI_AD<16>
PCI_CBE<2>	37	38	
PCI_IRDY_L	39	40	PCI_FRAME_L
	41	42	PCI_TRDY_L
AIRPORT_CLKRUN_L	43	44	PCI_STOP_L
	45	46	PCI_DEVSEL_L
PCI_CBE<1>	47	48	PCI_AD<15>
PCI_AD<14>	49	50	
	51	52	PCI_AD<13>
PCI_AD<12>	53	54	PCI_AD<11>
PCI_AD<10>	55	56	
ROM_RW_L	57	58	PCI_AD<9>
PCI_AD<8>	59	60	PCI_CBE<0>
PCI_AD<7>	61	62	ROM_OE_L
	63	64	PCI_AD<6>
PCI_AD<5>	65	66	
ROM_ONBOARD_CS_L	67	68	PCI_AD<4>
PCI_AD<3>	69	70	PCI_AD<2>
	71	72	PCI_AD<0>
PCI_AD<1>	73	74	
ROM_CS_L	75	76	NC
	77	78	NC
	79	80	NC
	81	82	

R730 10K 5% 1/16W MF 402 (to GND)

R745 22 5% 1/16W MF 402 (PCI_AD<18>)

PLACE SERIES R CLOSE TO INTERPID

R8 10K 5% 1/16W MF 402 (to GND)

RP2 33 5% 1/16W SM1
- UIDE_DATA<11> ↔ HD_DATA<11>

RP9 33 5% 1/16W SM1
- UIDE_DATA<3> ↔ HD_DATA<3>

RP9 33 5% 1/16W SM1
- UIDE_DATA<1> ↔ HD_DATA<1>

RP9 33 5% 1/16W SM1
- UIDE_DATA<2> ↔ HD_DATA<2>

RP2 33 5% 1/16W SM1
- UIDE_DATA<0> ↔ HD_DATA<0>

RP9 33 5% 1/16W SM1
- UIDE_DATA<7> ↔ HD_DATA<7>

RP2 33 5% 1/16W SM1
- UIDE_DATA<5> ↔ HD_DATA<5>

RP2 33 5% 1/16W SM1
- UIDE_DATA<4> ↔ HD_DATA<4>

RP3 33 5% 1/16W SM1
- UIDE_DATA<6> ↔ HD_DATA<6>

RP3 33 5% 1/16W SM1
- UIDE_DATA<8> ↔ HD_DATA<8>

RP4 33 5% 1/16W SM1
- UIDE_DATA<9> ↔ HD_DATA<9>

RP3 33 5% 1/16W SM1
- UIDE_DATA<10> ↔ HD_DATA<10>

RP4 33 5% 1/16W SM1
- UIDE_DATA<14> ↔ HD_DATA<14>

RP4 33 5% 1/16W SM1
- UIDE_ADDR<0> ↔ HD_ADDR<0>

RP5 33 5% 1/16W SM1
- UIDE_CS0_L ↔ HD_CS0_L

RP5 33 5% 1/16W SM1
- UIDE_ADDR<1> ↔ HD_ADDR<1>

RP5 33 5% 1/16W SM1
- UIDE_DATA<15> ↔ HD_DATA<15>

RP3 33 5% 1/16W SM1
- UIDE_DATA<13> ↔ HD_DATA<13>

RP4 33 5% 1/16W SM1
- UIDE_DATA<12> ↔ HD_DATA<12>

RP5 33 5% 1/16W SM1
- UIDE_ADDR<2> ↔ HD_ADDR<2>

R75 33 5% 1/16W MF 402
- UIDE_CS1_L ↔ HD_CS1_L

HARD DRIVE INTERFACE (UATA100)

+3V_SLEEP

3V_HD_LOGIC
R602 0 5% 1/16W MF 402 (to +3V_SLEEP)

5V_HD_LOGIC
R601 0 5% 1/16W MF 402 (to +5V_HD_SLEEP)

CRITICAL
J13
M-ST-SM1

HD_RESET_L	1	50	
HD_DATA<7>	2	49	
HD_DATA<6>	3	48	HD_DATA<8>
HD_DATA<5>	4	47	HD_DATA<9>
HD_DATA<4>	5	46	
HD_DATA<3>	6	45	HD_DATA<10>
HD_DATA<2>	7	44	HD_DATA<11>
HD_DATA<1>	8	43	
HD_DATA<0>	9	42	HD_DATA<12>
HD_DMARQ	10	41	HD_DATA<13>
HD_DIOR_L	11	40	
HD_DMACK_L	12	39	HD_DATA<14>
HD_ADDR<1>	13	38	HD_DATA<15>
HD_ADDR<0>	14	37	
HD_CS0_L	15	36	HD_DIOW_L
+HD_LOGIC_SLEEP	16	35	HD_IOCHRDY
	17	34	
HD_INTRQ	18	33	
HD_ADDR<2>	19	32	
HD_CS1_L	20	31	
	21	30	
	22	29	
	23	28	
	24	27	
	25	26	

R603 20K 5% 1/16W MF 402 (to +HD_LOGIC_SLEEP)

R101 10K 5% 1/16W MF 402 (to +5V_HD_SLEEP)

ANY SEQUENCING REQUIREMENT BETWEEN
+5V_HD_SLEEP AND +3V_SLEEP?

OPTICAL DRIVE INTERFACE (EIDE)

+5V_SLEEP

R452 100K 5% 1/16W MF 402 (NO STUFF)

R442 10K 5% 1/16W MF 402

R411 10K 5% 1/16W MF 402 (NO STUFF)

CRITICAL
J10
M-ST-SM1

NC	1	50	EIDE_OPTICAL_RST_L
	2	49	
EIDE_OPTICAL_DATA<8>	3	48	EIDE_OPTICAL_DATA<7>
EIDE_OPTICAL_DATA<9>	4	47	EIDE_OPTICAL_DATA<6>
EIDE_OPTICAL_DATA<10>	5	46	EIDE_OPTICAL_DATA<5>
EIDE_OPTICAL_DATA<11>	6	45	EIDE_OPTICAL_DATA<4>
	7	44	
EIDE_OPTICAL_DATA<12>	8	43	EIDE_OPTICAL_DATA<3>
EIDE_OPTICAL_DATA<13>	9	42	EIDE_OPTICAL_DATA<2>
EIDE_OPTICAL_DATA<14>	10	41	EIDE_OPTICAL_DATA<1>
EIDE_OPTICAL_DATA<15>	11	40	EIDE_OPTICAL_DATA<0>
	12	39	
EIDE_OPTICAL_DMA_RQ	13	38	EIDE_OPTICAL_WR_L
EIDE_OPTICAL_RD_L	14	37	EIDE_OPTICAL_IOCHRDY
EIDE_OPTICAL_DMAACK_L	15	36	EIDE_OPTICAL_INT
	16	35	EIDE_OPTICAL_ADDR<1>
EIDE_OPTICAL_ADDR<2>	17	34	EIDE_OPTICAL_ADDR<0>
EIDE_OPTICAL_CS1_L	18	33	EIDE_OPTICAL_CS0_L
	19	32	
	20	31	
	21	30	
NC	22	29	NC
	23	28	
	24	27	
	25	26	

R441 20K 5% 1/16W MF 402 (to GND)

R458 10K 5% 1/16W MF 402 (to GND)

PLACE PULLUP RESISTORS CLOSE TO INTREPID

+3V_SLEEP

R63 10K 5% 1/16W MF 402 (to GND)

R612 10K 5% 1/16W MF 402 (to +3V_SLEEP)

R94 10K 5% 1/16W MF 402 (to +3V_SLEEP)

R74 33 5% 1/16W MF 402
- UIDE_RST_L ↔ HD_RESET_L

R613 22 5% 1/16W MF 402
- UIDE_DMACK_L ↔ HD_DMACK_L

R35 22 5% 1/16W MF 402
- UIDE_DIOR_L ↔ HD_DIOR_L

R68 22 5% 1/16W MF 402
- UIDE_DIOW_L ↔ HD_DIOW_L

R93 82 5% 1/16W MF 402
- UIDE_IOCHRDY ↔ HD_IOCHRDY

C86 10PF 5% 50V CERM 402 (to GND)

IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V

BLUETOOTH/LEFT-SIDE USB

CRITICAL
J3
54550-1490
F-RT-SM

+5V_MAIN +3V_MAIN

BT_USB_DP	2	
BT_USB_DM	3	
	4	
	5	
LEFT_USB_DP	6	
LEFT_USB_DM	7	
	8	
NEC_LEFT_USB_PWREN	9	
SUTRO_ALS_OUT	10	
NEC_LEFT_USB_OVERCURRENT	11	
SUTRO_ALS_GAIN_SW	12	
	13	
	14	
	15	
	16	

R71 15K 5% 1/16W MF 402

R64 15K 5% 1/16W MF 402

INTERNAL I/O CONNECTORS

APPLE COMPUTER INC.

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D	051-6694	02
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SOUND BOARD (SOUSAPHONE)

AUDIO - KAZOO SND - INTREPID

Sound Board Connector

Place shorts at 3.3V and 5V regulators

This is an internal board short

This is an internal board short

This is an internal board short

CRITICAL

J12 QT500406-L111 M-ST-SM1

51650154

VER 1

R534 0 5% 1/16W MF 402 — INT_GPIO9_PU — AUDIO_GPIO_11

R581 0 5% 1/16W MF 402 — INT_GPIO15_PU — AUDIO_EXT_MCLK_SEL

R552 0 5% 1/16W MF 402 — INT_EXTINT14_PU — AUDIO_LO_OPTICAL_PLUG_L

R582 0 5% 1/16W MF 402 — INT_EXTINT3_PU — AUDIO_LI_OPTICAL_PLUG_L

L77 FERR-220-OHM 0402 — SND_SYNC — I2S0_SYNC_F

L80 FERR-220-OHM 0402 — SND_CLKOUT — I2S0_MCLK_F

L81 FERR-220-OHM 0402 — INT_AUDIO_TO_SND — I2S0_DEV_TO_SB_DTI_F

L82 FERR-220-OHM 0402 — SND_TO_AUDIO — I2S0_SB_TO_DEV_DTO_F

L76 FERR-220-OHM 0402 — SND_AMP_MUTE_INV — AUDIO_SPKR_MUTE_L_F

L78 FERR-220-OHM 0402 — SND_HW_RESET_L — I2S0_RESET_L_F

L79 FERR-220-OHM 0402 — SND_SCLK — I2S0_BITCLK_F

L84 FERR-220-OHM 0402 — MOD_SYNC — I2S2_SYNC_F

L48 FERR-220-OHM 0402 — MOD_BITCLK — I2S2_BITCLK_F

C895 0.01UF 20% 16V CERM 402 (NO STUFF)
C899 0.01UF 20% 16V CERM 402 (NO STUFF)
C896 0.01UF 20% 16V CERM 402 (NO STUFF)
C897 0.01UF 20% 16V CERM 402 (NO STUFF)
C898 0.01UF 20% 16V CERM 402 (NO STUFF)
C900 0.01UF 20% 16V CERM 402 (NO STUFF)
C901 0.01UF 20% 16V CERM 402 (NO STUFF)
C81 0.01UF 20% 16V CERM 402 (NO STUFF)
C82 0.01UF 20% 16V CERM 402 (NO STUFF)

XW9 SM — XW10 SM — XW11 SM

+3V_SLEEP

+5V_MAIN

+3V_SLEEP_AUDIO

SND_AGND

(SLEEP_LED_GND)

AUDIO_GPIO_11 ↔ AUDIO_LO_DET_L
+3V_SLEEP_AUDIO ↔ AUDIO_LO_OPTICAL_PLUG_L
AUDIO_EXT_MCLK_SEL ↔ AUDIO_LI_DET_L
AUDIO_LO_MUTE_L ↔ AUDIO_LI_OPTICAL_PLUG_L
AUDIO_SPKR_MUTE_L_F
I2S0_MCLK_F
I2S0_BITCLK_F ↔ I2S0_RESET_L_F
I2S0_SYNC_F
I2S0_SB_TO_DEV_DTO_F
I2S0_DEV_TO_SB_DTI_F ↔ INT_I2C_DATA2
INT_I2C_CLK2
I2S2_BITCLK_F
I2S2_SYNC_F ↔ SLEEP_ANODE
I2S2_DEV_TO_SB_DTI_F

L85 FERR-220-OHM 0402 — INT_MOD_DTI — I2S2_DEV_TO_SB_DTI_F
C87 0.01UF 20% 16V CERM 402 (NO STUFF)

L86 FERR-220-OHM 0402 — INT_GPIO12_PU — I2S2_RESET_L_F
C88 0.01UF 20% 16V CERM 402 (NO STUFF)

FAN INTERFACE

CAPS FOR EMI EXPERIMENTATION ONLY

KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

R719 0 5% 1/16W MF 402 — CPU_M_DP ↔ THERM1_DP
R725 0 5% 1/16W MF 402 — CPU_M_DM ↔ THERM1_DM
R713 0 5% 1/16W MF 402 — SUPPLY_M_DP ↔ THERM2_DP
R716 0 5% 1/16W MF 402 — SUPPLY_M_DM ↔ THERM2_DM

PLACE XW9 CLOSE TO 5V SWITCHER (U27)

PLACE CAPS AS CLOSE TO THERMISTORS AS POSSIBLE

PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY

MAIN1

C681 0.001UF 20% 50V CERM 402
Q66 2N3904 SM

SUPPLY_M_DP — SUPPLY_M_DM

PLACE CLOSE TO CPU

MAIN2

C668 0.001UF 20% 50V CERM 402
Q39 2N3904 SM

CPU_M_DP — CPU_M_DM

PLACE UNDERNEATH UPPER RAM

ALTERNATE1

C678 0.001UF 20% 50V CERM 402 (NO STUFF)
Q47 2N3904 SM (NO STUFF)

THERM1_A_DP — THERM1_A_DM

PLACE CLOSE TO BATTERY CHARGER/VCORE

ALTERNATE2

C651 0.001UF 20% 50V CERM 402 (NO STUFF)
Q62 2N3904 SM (NO STUFF)

THERM2_A_DP — THERM2_A_DM

KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

R628 0 5% 1/16W MF 402 (NO STUFF) — CPU_THERM_DP ↔ THERM1_DP
R620 0 5% 1/16W MF 402 (NO STUFF) — CPU_THERM_DM ↔ THERM1_DM
R723 0 5% 1/16W MF 402 (NO STUFF) — THERM1_A_DP ↔ THERM1_DP
R726 0 5% 1/16W MF 402 (NO STUFF) — THERM1_A_DM ↔ THERM1_DM
R710 0 5% 1/16W MF 402 (NO STUFF) — THERM2_A_DP ↔ THERM2_DP
R717 0 5% 1/16W MF 402 (NO STUFF) — THERM2_A_DM ↔ THERM2_DM

THERM ISOLATION

+3V_MAIN

R811 100K 5% 1/16W MF 402 — R812 100K 5% 1/16W MF 402 — R813 100K 5% 1/16W MF 402

+3V_PMU_AVCC

THERM_L_OC

THERM_INV

Q87 2N7002DW SOT-363 — Q87 2N7002DW SOT-363 — Q87 2N7002DW SOT-363

C903 0.1UF 20% 10V CERM 402

ADT7460_THERM

MODEM

SUPPORTS BOTH THE LAST DASH AND Q52 SOFT MODEM

+5V_MAIN

R874 100K 5% 1/16W MF 402 — SND_AMP_MUTE

Q26 2N7002DW SOT-363 — SND_AMP_MUTE_L

R875 100K 5% 1/16W MF 402 — AMP_CONTROL — INT_PU_RESET_L

Q26 2N7002DW SOT-363

+5V_MAIN

R224 10K 5% 1/16W MF 402 — SND_AMP_MUTE_INV

Q33 2N7002 SM — SND_AMP_MUTE

+3V_MAIN

R872 10K 5% 1/16W MF 402 — AUDIO_LO_MUTE_L

R689 100K 5% 1/16W MF 402

Q31 2N7002DW SOT-363 — SND_HP_MUTE

Q31 2N7002DW SOT-363 — SND_HP_MUTE_L

AMP_CONTROL

R873 100K 5% 1/16W MF 402 1/16W

C711 0.1UF 20% 10V CERM 402

+3V_MAIN

R814 10 5% 1/16W MF 402

ADT7460_VCC

C904 1UF 20% 10V CERM 603

FAN CONTROLLER

+5V_SLEEP

R42 10K 5% 1/16W MF 402

R692 10K 5% 1/16W MF 402

R695 10K 5% 1/16W MF 402

R293 10K 5% 1/16W MF 402

R295 10K 5% 1/16W MF 402

R878 0 5% 1/16W MF 402 (NO STUFF) — FANL_PWM

R879 0 5% 1/16W MF 402 (NO STUFF) — FANR_PWM

Q78 2N7002DW SOT-363

Q78 2N7002DW SOT-363

U3 QSOP ADT7460

ADT7460_VCORE_MON — +2.5V
INT_I2C_DATA1 — SDA
INT_I2C_CLK1 — SCL
SMBALERT#
CRITICAL
ADR ENABLE#
ADR SELECT
THERM#
GND
NC

PWM1 — ADT7460_FAN1_PWM
TACH1 — FANL_TACH
PWM2 — ADT7460_FAN2_PWM
TACH2 — FANR_TACH
PWM3 — ADT7460_ADR_EN_L
TACH3
TACH4 — ADT7460_THERM

THERM1_DP — D1+
THERM1_DM — D1-
THERM2_DP — D2+
THERM2_DM — D2-

C688 0.001UF 20% 50V CERM 402 (NO STUFF)
C690 0.001UF 20% 50V CERM 402 (NO STUFF)
C846 0.001UF 20% 50V CERM 402 (NO STUFF)
C905 0.001UF 20% 50V CERM 402 (NO STUFF)

DEBUG JUMPERS

R537 0 5% 1/16W MF 603 (NO STUFF) — PMU_NMI_BUTTON_L
R553 0 5% 1/16W MF 603 (NO STUFF) — PMU_RESET_BUTTON_L

LEFT FAN (CPU)

+5V_SLEEP

R679 10K 5% 1/16W MF 402

CRITICAL J4 SM-2MT

Q37 SI3446DV TSOP

PLACE CLOSE TO CONNECTOR

C134 4.7UF 20% 10V CERM 1206

FANL_TACH — FANL_GND — FANL_PWM

SERIAL DEBUG INTERFACE

+5V_MAIN

SERIAL_DEBUG CRITICAL J16 M-ST-5087 SM

COMM_TXD_L ↔ COMM_DTR_L
COMM_TRXC ↔ COMM_RTS_L
COMM_GPIO_L ↔ COMM_RXD

+3V_MAIN

CRITICAL J8 QT510166-L010 F-ST-SM1

MOD_DTO ↔ MOD_SYNC
MOD_CLKOUT ↔ INT_MOD_DTI
MOD_BITCLK
COMM_RESET_L
COMM_SHUTDOWN
MODEM_USB_DM
MODEM_USB_DP
INT_I2C_CLK2
INT_I2C_DATA2 ↔ COMM_RING_DET_L

R405 10K 5% 1/16W MF 402 (NO STUFF)

C767 10UF 20% 6.3V CERM 805 (NO STUFF)
C513 0.1UF 20% 10V CERM 402
C478 0.1UF 20% 10V CERM 402 (NO STUFF)
C469 10UF 20% 6.3V CERM 805

DEBUG POWER BUTTON

R527 0 5% 1/16W MF 603 (NO STUFF) — PWR_BUTTON_L

+5V_SLEEP RIGHT FAN (GPU)

R623 10K 5% 1/16W MF 402

CRITICAL J2 SM-2MT

FANR_GND
FANR_TACH
FANR_PWM

Q36 SI3446DV TSOP

PLACE CLOSE TO CONNECTOR

C135 4.7UF 20% 10V CERM 1206

FAN/MODEM/SOUND/SLEEP LED/DEBUG

APPLE COMPUTER INC.

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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0608	197S0038	NEC_USB	Y5	ALT FOR SIWARD

Y7 LOAD CAPACITANCE IS 16PF

Low/Full/High Speed (External)

Low/Full/High Speed (External)

SERR_L AND PERR_L
HAS DEDICATED PULL-UP
FOR BOTH CBUS AND USB2

Series Rpaks required to facilitate NAND-tree testing

NEED PULL-UP RESISTORS IN CASE USB 1.0 IS USED FOR PORT POWER

PLACE NEAR J3

SUTRO CONNECTOR

PLACE NEAR J12

BUBBA CONNECTOR

INTREPID USB CONSTRAINTS

USB_DAM	USB_DA	5 MIL SPACING	14
USB_DAP	USB_DA	5 MIL SPACING	14
USB_DCM	USB_DC	5 MIL SPACING	14
USB_DCP	USB_DC	5 MIL SPACING	14
USB_D1M	USB_D1	5 MIL SPACING	14 27
USB_D1P	USB_D1	5 MIL SPACING	14 27
USB_D2M	USB_D2	5 MIL SPACING	
USB_D2P	USB_D2	5 MIL SPACING	

USB 2.0

APPLE COMPUTER INC.

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Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

+3V_MAIN

R633 10K 5% 1/16W MF 402

JTAG_ASIC_TDI 28 40

+3V_MAIN

NO STUFF R333 0 5% 1/16W MF 402

C442 10uF 20% 6.3V CERM 805

3405_MODE

R319 0 5% 1/16W MF 402

U14 LTC3405 SOT23-6 CRITICAL

VIN, RUN, MODE, GND, SW, VFB

LTC3405_SW 39

CRITICAL L5 3.3uH SM1

R334 665K 1% 1/16W MF 402 R2A

C471 22pF 5% 50V CERM 402

R361 49.9K 1% 1/16W MF 402 R2B

3405_VFB

C486 10uF 20% 6.3V CERM 805

R362 182K 1% 1/16W MF 402 R1

+1_0V_MARVELL 39

VOUT = 0.8V*(1+R2EQV/R1)

R2EQV = R2A||R2B

PLACE ALL SERIES RES CLOSE TO PHY

R370 0 5% 1/16W MF 402

R353 0 5% 1/16W MF 402

R344 0 5% 1/16W MF 402

37 13 CLKENET_LINK_TX — 37 CLKENET_PHY_TX

37 13 CLKENET_LINK_RX — 37 CLKENET_PHY_RX

37 13 CLKENET_LINK_GBE_REF — 37 CLKENET_PHY_GBE_REF

U49 88E1111 BCC CRITICAL

TX_CLK 4, RX_CLK 2, 125CLK 22

38 13 ENET_PHY_TXD<0> 11 — TXD0
38 13 ENET_PHY_TXD<1> 12 — TXD1
38 13 ENET_PHY_TXD<2> 14 — TXD2
38 13 ENET_PHY_TXD<3> 16 — TXD3
38 13 ENET_PHY_TXD<4> 17 — TXD4
38 13 ENET_PHY_TXD<5> 18 — TXD5
38 13 ENET_PHY_TXD<6> 19 — TXD6
38 13 ENET_PHY_TXD<7> 20 — TXD7

38 13 ENET_PHY_TX_EN 9 — TX_EN
38 13 ENET_PHY_TX_ER 7 — TX_ER
37 13 CLKENET_PHY_GTX 8 — GTX_CLK

38 13 ENET_LINK_RXD<0> 95 — RXD0
38 13 ENET_LINK_RXD<1> 92 — RXD1
38 13 ENET_LINK_RXD<2> 93 — RXD2
38 13 ENET_LINK_RXD<3> 91 — RXD3
38 13 ENET_LINK_RXD<4> 90 — RXD4
38 13 ENET_LINK_RXD<5> 89 — RXD5
38 13 ENET_LINK_RXD<6> 87 — RXD6
38 13 ENET_LINK_RXD<7> 86 — RXD7

38 13 ENET_RX_DV 94 — RX_DV
38 13 ENET_RX_ER 3 — RX_ER

38 13 ENET_CRS 84 — CRS
38 13 ENET_COL 83 — COL

38 13 ENET_MDC 25 — MDC
38 13 ENET_MDIO 24 — MDIO

14 ENET_ENERGY_DET 23 — INT-/INT+

31 27 24 23 17 IO_RESET_L — ENET_RST_L 28 — RESET

ENET_COMA 27 — COMA

C755 2.2uF 20% 10V CERM 805

NC 82 S_IN+, NC 81 S_IN-, NC 77 S_OUT+, NC 75 S_OUT-, NC 79 S_CLK+, NC 80 S_CLK-

ENET_HSDACP 37 — HSDAC+
ENET_HSDACM 38 — HSDAC-

37 CLK25M_ENET_XIN 55 — XTAL1
37 CLK25M_ENET_XOUT 54 — XTAL2

ENET_VSSC 53 — VSSC

GND 97

CTRL10 51 NC

DVDD: 1, 6, 10, 15, 57, 62, 67, 71, 85

C492 0.1UF 20% 10V CERM 402
C511 0.01UF 20% 16V CERM 402
C517 0.1UF 20% 10V CERM 402
C502 0.01UF 20% 16V CERM 402
C465 0.1UF 20% 10V CERM 402
C475 0.01UF 20% 16V CERM 402

PLACE CAPS (IN ORDER) ON PINS 1, 6, 10/15, 57/62, 67/71, 85

VDDO: 5, 21/26, 88, 96

C464 0.1UF 20% 10V CERM 402
C472 0.01UF 20% 16V CERM 402
C453 0.1UF 20% 10V CERM 402
C503 0.01UF 20% 16V CERM 402
C501 0.1UF 20% 10V CERM 402
C496 10uF 20% 6.3V CERM 805

39 28 +2_5V_MARVELL

PLACE CAPS (IN ORDER) ON PINS 5, 21/26, 48/52, 66/72, 88, 96

VDDOH: 52, 66, 72

VDDOX: 26, 48

+2_5V_MARVELL_AVDD 39

L34 FERR-EMI-600-OHM SM

AVDD: 32, 35, 36, 40, 45, 78

C497 0.1UF 20% 10V CERM 402
C504 0.01UF 20% 16V CERM 402
C487 0.1UF 20% 10V CERM 402
C476 0.01UF 20% 16V CERM 402
C754 10uF 20% 6.3V CERM 805

PLACE CAPS (IN ORDER) ON PINS 32/35, 36/40, 45 & 78

MDI0+ 29 — 38 MDI_P<0>
MDI0- 31 — 38 MDI_M<0>
MDI1+ 33 — 38 MDI_P<1>
MDI1- 34 — 38 MDI_M<1>
MDI2+ 39 — 38 MDI_P<2>
MDI2- 41 — 38 MDI_M<2>
MDI3+ 42 — 38 MDI_P<3>
MDI3- 43 — 38 MDI_M<3>

LED_LINK10 76 — LED_LINK10
LED_LINK100 74 — LED_LINK100
LED_LINK1000 73 NC
LED_DUPLEX 70 NC
LED_RX 69 — LED_RX_SPN
LED_TX 68 NC

CONFIG0 65 (000)
CONFIG1 64 (000)
CONFIG2 63 (111)
CONFIG3 61 (110)
CONFIG4 60 (111)
CONFIG5 59 (101)
CONFIG6 58 (000)

SEE CONFIG TABLES (BELOW)

TDI 44 — JTAG_ASIC_TDI 28 40
TDO 50 — JTAG_ENET_TDO 13
TCK 49 — JTAG_ASIC_TCK 13 40
TMS 46 — JTAG_ASIC_TMS 13 40
TRST 47 — JTAG_ASIC_TRST_L 13 40

RSET 30 — ENET_RSET

SEL_OSC 56 NC
SEL_2.5V 13

R380 4.99K 1% 1/16W MF 402

R346 49.9 1% 1/16W MF 402 — MDI0_PD
R372 49.9 1% 1/16W MF 402 — MDI1_PD
R404 49.9 1% 1/16W MF 402 — MDI2_PD
R413 49.9 1% 1/16W MF 402 — MDI3_PD

R355 49.9 1% 1/16W MF 402
R381 49.9 1% 1/16W MF 402
R406 49.9 1% 1/16W MF 402
R428 49.9 1% 1/16W MF 402

C454 0.01UF 20% 16V CERM 402
C477 0.01UF 20% 16V CERM 402
C493 0.01UF 20% 16V CERM 402
C505 0.01UF 20% 16V CERM 402

PLACE RESISTORS CLOSE TO PHY

+2_5V_MAIN

R465 5% 1/10W MF 805

C488 0.1UF 20% 10V CERM 402
C466 0.1UF 20% 10V CERM 402
C506 0.1UF 20% 10V CERM 402
C520 0.1UF 20% 10V CERM 402

PLACE CAPS AT TRANSFORMER PINS 1, 4, 7 & 10

PLACE CLOSE TO ETHERNET CONNECTOR

NO STUFF R438 0 5% 1/10W FF 805

CHGND1

CRITICAL J17 RJ45 RT-TH

12 RJ45_DP<0>
10 RJ45_C0_PD
11 RJ45_DN<0>
9 RJ45_DN<1>
7 RJ45_C1_PD
8 RJ45_DP<1>
6 RJ45_DP<2>
4 RJ45_C2_PD
5 RJ45_DN<2>
3 RJ45_DP<3>
1 RJ45_C3_PD
2 RJ45_DN<3>

XFR-ENET-1000BT SM

T1 CRITICAL

11 9 1 2 3 4 5 6 7 8 10 12

Short shielded RJ-45

CHGND1

R735 75 5% 1/16W MF 402
R733 75 5% 1/16W MF 402
R382 75 5% 1/16W MF 402
R347 75 5% 1/16W MF 402

ENET_CTAP_CHGND 39

C457 100pF 10% 3KV CERM 1808

CHGND1

39 28 +2_5V_MARVELL

R371 10K 5% 1/16W MF 402

R345 10K 5% 1/16W MF 402

R354 1.5K 5% 1/16W MF 402

R343 1K 5% 1/16W MF 402

14 INT_ENET_RST_L

D1 1N914 SOT23

Q15 2N7002DW SOT-363

Q15 2N7002DW SOT-363

32 31 30 AC_IN

36 35 34 19 SLEEP_L_LS5

PLACES PHY IN "COMA" MODE WHEN ASLEEP ON BATTERY (SAVES POWER)

PUT CRYSTAL CIRCUIT CLOSE TO PHY

NO STUFF R435 20K 5% 1/16W MF 402

R427 0 5% 1/16W MF 402

CRITICAL Y3 25.0000M 8X4.5MM-SM

CLK25M_XTAL_IN

C555 33pF 5% 50V CERM 402

C491 33pF 5% 50V CERM 402

Y3'S LOAD CAPACITANCE IS 20PF

NO STUFF R393 49.9 1% 1/16W MF 402

NO STUFF R403 49.9 1% 1/16W MF 402

R335 10K 5% 1/16W MF 402

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0703	197S0037		Y3	
197S0603	197S0037		Y3	ALT FOR SIWARD

CONFIG DEFINITIONS

PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS

PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50_OHM

MARVELL 88E1111

10/100/1000 ETHERNET

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6694 | REV. 02

SCALE NONE | SHT 28 OF 45

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0011	197S0052	?	G1	SIWARD ALT FOR FW OSC

DSX STRAP OPTIONS

0 -> BILINGUAL PORT

1 -> A-ONLY PORT

PLACE NEAR PHY

PLACE NEAR PHY

SPEC SAID TO USE 10K

PHY PINS 72,76

PHY PIN 64

PHY PIN 25

PHY PIN 28

PHY PIN 38

PHY PINS 4,14

PHY PIN 61

PHY PIN 50

PHY PIN 40

PHY PIN 21

VOUT = 1.22*(1+R2/R1)+ IADJ*R2

IADJ = 30NA AT 25C

PWR CLASS = 100

(MAY PROVIDE POWER, OR MAY REQUIRE UP TO 3W)

(PC0 IS MSB, PC2 IS LSB)

1MA(MAX) BUS HOLDER EACH

CAPACITOR IN CONJUCTION WITH INTERNAL PULLUP PROVIDES RESET PULSE WHEN PHY FIRST RECEIVES POWER

FIREWIRE

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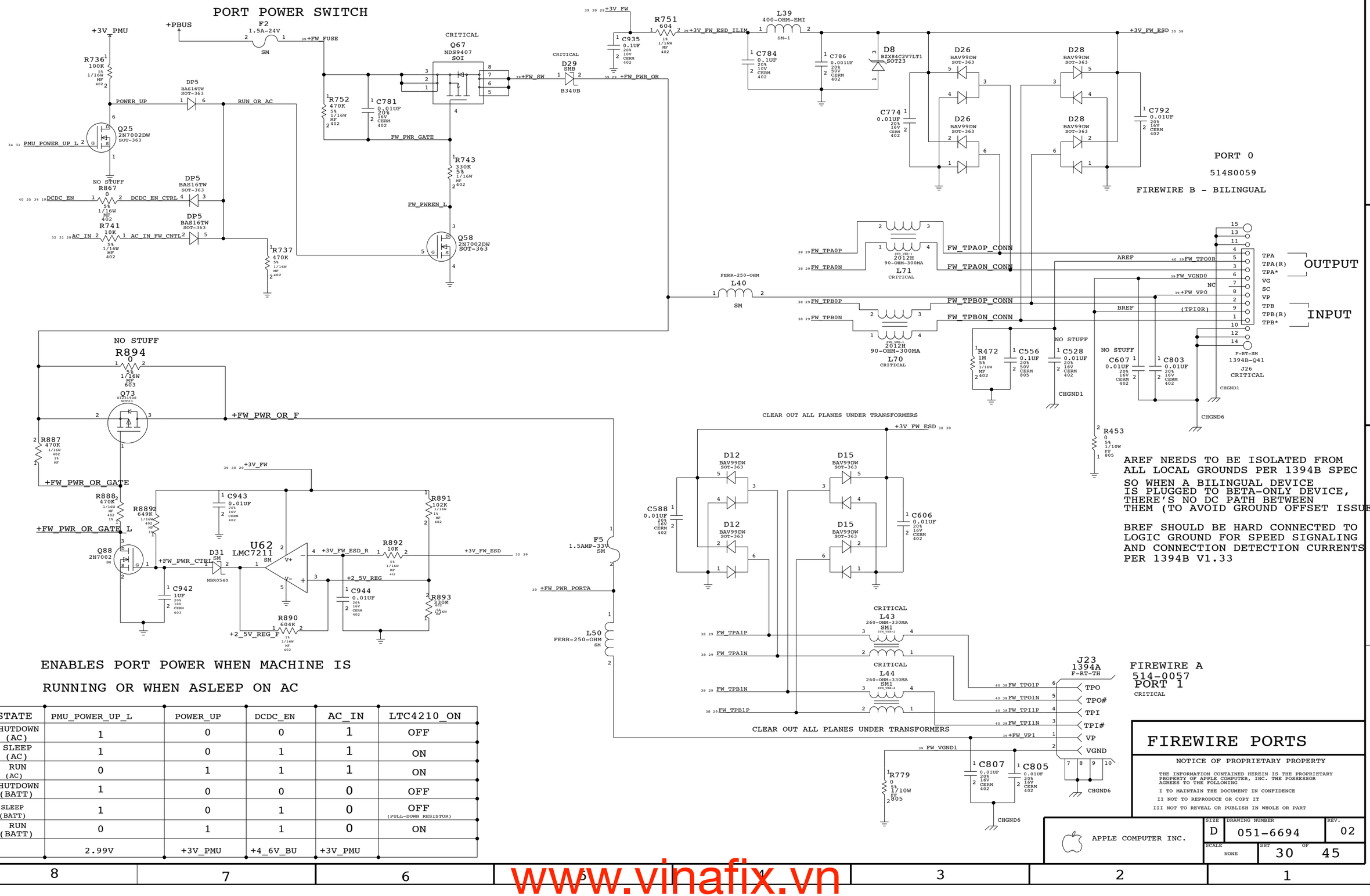

ENABLES PORT POWER WHEN MACHINE IS RUNNING OR WHEN ASLEEP ON AC

STATE	PMU_POWER_UP_L	POWER_UP	DCDC_EN	AC_IN	LTC4210_ON
SHUTDOWN (AC)	1	0	0	1	OFF
SLEEP (AC)	1	0	1	1	ON
RUN (AC)	0	1	1	1	ON
SHUTDOWN (BATT)	1	0	0	0	OFF
SLEEP (BATT)	1	0	1	0	OFF (PULL-DOWN RESISTOR)
RUN (BATT)	0	1	1	0	ON
	2.99V	+3V_PMU	+4_6V_BU	+3V_PMU	

FIREWIRE PORTS

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SIZE	DRAWING NUMBER	REV.
D	051-6694	02
SCALE: NONE	SHT 30 OF 45	

+3V_PMU

R505 470K 5% 1/16W MF 402 — CHARGE_LED_L 31 32 40
R504 10K 5% 1/16W MF 402 — PMU_POWER_UP_L 30 31 34
R492 10K 5% 1/16W MF 402 — SOFT_PWR_ON_L 22 23 31 35
R536 100K 5% 1/16W MF 402 — MAIN_RESET_L 14 17 18 20 25 27 31 40
RP40 100K 5% 1/16W SM1 — IO_RESET_L 17 23 24 27 28 31
RP40 100K 5% 1/16W SM1 — SLEEP 23 31 34 36 40
RP40 100K 5% 1/16W SM1 — INT_RESET_L 9 13 31
RP40 100K 5% 1/16W SM1 — INT_SUSPEND_REQ_L 8 31
R782 1K 5% 1/16W MF 402 — PMU_BYTE 31
R787 10K 5% 1/16W MF 402 — PMU_CNVSS 31

+3V_PMU

C643 10UF 20% 6.3V CERM 805
C574 0.1UF 20% 10V CERM 402
C835 0.1UF 20% 10V CERM 402
R778 4.7 5% 1/16W MF 402 — +3V_PMU_AVCC 26 31 39
C827 0.1UF 20% 10V CERM 402

VCC 14 60 — AVCC 97
VSS 12 62 — AVSS 94

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1008	1	IC,PMU,V81B	U33	

CPU VCORE_HI_OC/PMU_AP should have a pulldown for coming out of reset. MLB will have a pull-up to +3V_MAIN or +3V_SLEEP, which will act as our pulldown since both are off during PMU reset.

U33 M16C62 FLAS — CRITICAL — OMIT

40 KBD_Y<0>	86	P00_D0	
40 KBD_Y<1>	85	P01_D1	
KBD_Y<2>	84	P02_D2	
40 KBD_Y<3>	83	P03_D3	
40 KBD_Y<4>	82	P04_D4	
KBD_Y<5>	81	P05_D5	
40 KBD_Y<6>	80	P06_D6	
40 KBD_Y<7>	79	P07_D7	
PMU_NUMLOCK_LED_L	78	P10_D8	
PMU_CAPSLOCK_LED_L	77	P11_D9	
40 32 31 CHARGE_LED_L	76	P12_D10	
34 31 30 PMU_POWER_UP_L	75	P13_D11	
PMU_SELECT	74	P14_D12	
35 31 23 22 SOFT_PWR_ON_L	73	P15_D13_INT3	
40 26 14 COMM_RING_DET_L	72	P16_D14_INT4	
14 INT_WATCHDOG_L	71	P17_D15_INT5	
40 23 KBD_X<0>	70	P20_A0_D0	
40 23 KBD_X<1>	69	P21_A1_D1_D0	
23 KBD_X<2>	68	P22_A2_D2_D1	
40 23 KBD_X<3>	67	P23_A3_D3_D2	
23 KBD_X<4>	66	P24_A4_D4_D3	
23 KBD_X<5>	65	P25_A5_D5_D4	
23 KBD_X<6>	64	P26_A6_D6_D5	
23 KBD_X<7>	63	P27_A7_D7_D6	
40 23 KBD_X<8>	61	P30_A8_D7	
23 KBD_X<9>	59	P31_A9	
31 28 27 24 23 17 IO_RESET_L	58	P32_A10	
23 KBD_COMMAND_L	57	P33_A11	
40 23 KBD_CONTROL_L	56	P34_A12	
40 23 KBD_SHIFT_L	55	P35_A13	
40 23 KBD_OPTION_L	54	P36_A14	
40 23 KBD_FUNCTION_L	53	P37_A15	
14 PMU_INT_L	52	P40_A16	
23 KBD_ID	51	P41_A17	
7 CPU_PLL_STOP_OC	50	P42_A18	
NC	49	P43_A19	
40 36 34 31 23 SLEEP	48	P44_CS0	
	47	P45_CS1	
8 INT_SUSPEND_ACK_L	46	P46_CS2	
31 8 INT_SUSPEND_REQ_L	45	P47_CS3	
31 PMU_BYTE	6	BYTE	
	11	XOUT	
	13	XIN	
	10	RESET	
39 31 26 +3V_PMU_AVCC	96	VREF	
31 PMU_CNVSS	7	CNVSS	

		P50_WRL_WR	
		P51_WRH_BHE	
		P52_RD	
		P53_BCLK	
		P54_HLDA	
		P55_HOLD	
		P56_ALE	
		P57_RDY_CLKOUT	
		P60_CTS0_RTS0	
		P61_CLK0	
		P62_RXD0	
		P63_TXD0	
		P64_CTS1_RTS1_CTS0_CLKS1	
		P65_CLK1	
		P66_RXD1	
		P67_TXD1	
		P70_TXD2_SDA_TA0OUT	
		P71_RXD2_SCL_TA0IN_TB5IN	
		P72_CLK2_TA1OUT_V	
		P73_CTS2_RTS2_TA1IN_V	
		P74_TA2OUT_W	
		P75_TA2IN_W	
		P76_TA3OUT	
		P77_TA3IN	
		P80_TA4OUT_U	
		P81_TA4IN_U	
		P82_INT0	
		P83_INT1	
		P84_INT2	
		P85_NMI	
		P86_XCOUT	
		P87_XCIN	
		P90_TB0IN_CLK3	
		P91_TB1IN_SIN3	
		P92_TB2IN_SOUT3	
		P93_DA0_TB3IN	
		P94_DA1_TB4IN	
		P95_ANEX0_CLK4	
		P96_ANEX1_SOUT4	
		P97_ADTRG_SIN4	
		P100_AN0	
		P101_AN1	
		P102_AN2	
		P103_AN3	
		P104_AN4_KI0	
		P105_AN5_KI1	
		P106_AN6_KI2	
		P107_AN7_KI3	

(PMU_AP)

44	CPU_VCORE_HI_OC	7 35
43	INT_RESET_L	9 13 31
42	MAIN_RESET_L	14 17 18 20 25 27 31 40
41	NC	
40	PMU_INT_NMI	14
39	PMU_EPM	31
38	INT_PU_RESET_L	13 26 31
37	PMU_CPU_HRESET_L	6 23
36	PMU_ACK_L	14
35	PMU_CLK	14
34	PMU_FROM_INT	14
33	PMU_TO_INT	14
32	PMU_REQ_L	14
31	PMU_LID_CLOSED_L	23 31
30	PMU_RESET_BUTTON_L	26 31
29	PMU_NMI_BUTTON_L	26 31
28	TPAD_RXD	31
27	TPAD_TXD	31
26	SYSTEM_CLK_EN	14
25	CPU_CLK_EN	8
24	PMU_CHARGE_V	32
23	PMU_CHRG_BATT_0	32
22	NC (CHARGE_I)	
21	NC	
20	PMU_SLEEP_LED_L	23
19	CPU_SMI_L	5
18	POWER_VALID	31
17	PMU_PME_L	14 27 31
16	INT_PEND_PROC_INT	14
15	PMU_NMI_L	31
9		
8		
5	PMU_BATT0_DET_L	
4	PMU_BATT1_DET_L_PU	31
3	NC	
2	NC	
1	INT_PROC_SLEEP_REQ_L	14
100	PMU_POWERUP_OK	31
99	NC	
98	PMU_OOPS	31
95	THERM_L_OC	23 26
93	PMU_AC_IN	
92	PMU_AC_DET	31
91	SYS_BATT_ISNS2	
90	PMU_I2C_CLK	31
89	PMU_I2C_DATA	31
88	PMU_SMB_CLK	31 32
87	PMU_SMB_DATA	31 32

R518 2.2K 5% 1/16W MF 402 — NUMLOCK_LED_L1
R513 2.2K 5% 1/16W MF 402 — CAPSLOCK_LED_L

+3V_PMU
R868 10K 5% 1/16W MF 402
NO STUFF R869 10K 5% 1/16W MF 402

+3V_PMU
R844 1K 5% 1/16W MF 402
R843 100K 5% 1/16W MF 402
C915 0.1UF 20% 10V CERM 402
+3V_PMU_RESET
VCC U41 MAX6804 SOT143 MR* RSET* GND
31 PMU_CUSTOM_RESET_L

PMU RESET CIRCUIT

+3V_PMU
R233 100K 5% 1/16W MF 402
DP8 BAS16TW SOT-363 — 32 AC_IN_L
DP8 BAS16TW SOT-363 — 40 32 PMU_BATT_DET_L
PMU_CUSTOM_RESET
Q18 2N7002DW SOT-363 — 35 31 23 22 SOFT_PWR_ON_L
Q18 2N7002DW SOT-363
PMU_CUSTOM_RESET_L 31
CLK10M_PMU_XOUT_UF

PMU_RESET_L
39 31 26 +3V_PMU_AVCC
31 PMU_CNVSS
CLK10M_PMU_XOUT
CLK10M_PMU_XIN

NO STUFF R595 10M 5% 1/16W MF 402
R594 0 5% 1/16W MF 402
CRITICAL Y6 10.0000M 8X4.5MM-SM
C666 12PF 5% 50V CERM 402
C664 12PF 5% 50V CERM 402

Keep crystal subcircuit close to PMU.
Y6'S LOAD CAPACITANCE IS 12PF

Q11 ADAPTER DETECTION SCHEME

CASE	ADAPTER	PIN VOLT	ID VOLT RANGE	SYSTEM STATUS
1	Q11 (65W)	2.007V- 2.066V	1.65V- 2.31V	RECOGNIZES AS Q11 FULL FUNCTIONS
2	A29 (45W)	2.558V- 2.661V	2.31V- 2.97V	RECOGNIZES AS A29 LIMITED FUNCTIONS
3	AIRLINE	0.589V- 0.663V	0.33V- 0.99V	FULL FUNCTIONS NO BATTERY CHARGING
4	HOOPER	3.19V- 3.28V	2.97V- 3.30V	RECOGNIZES AS HOOPER LIMITED FUNCTIONS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0704	197S0041		Y6	ALT CRYSTAL SIZE
197S0604	197S0041		Y6	ALT FOR SIWARD

+3V_PMU
39 33 +4.85V_RAW
R877 10K 1% 1/16W MF 402 — 31 PMU_AC_DET 1
R501 100K 1% 1/16W MF 402
ADAPTER_DET 32 40
R502 100K 1% 1/16W MF 402
AC_DET
R503 402K 1% 1/16W MF 402

A29 DETECT CIRCUIT

R491 52.3K 1% 1/16W MF 402
C558 0.1UF 20% 10V CERM 402
R517 100K 5% 1/16W MF 402
A29_DETECT 32
U27 LMC7211 SM CRITICAL
2_34V_REF
A29_DET_L
Q22 2N7002 SM
R476 4.7M 5% 1/16W MF 402
R475 127K 1% 1/16W MF 402
50MV OF HYSTERSIS

Keep crystal subcircuit close to PMU.
CLK32K_PMU_XOUT
CLK32K_PMU_XIN
R593 1K 5% 1/16W MF 402 — PMU_BATT_DET_L 31 32 40
R572 1K 5% 1/16W MF 402 — AC_IN 28 30 32
R870 0 5% 1/16W MF 402 — SYS_BATT_ISNS 24
NO STUFF R786 10M 5% 1/16W MF 402
R785 0 5% 1/16W MF 402
CRITICAL Y7 32.768K SM-1
C832 12PF 5% 50V CERM 402
C831 12PF 5% 50V CERM 402
CLK32K_PMU_XOUT_UF

Y7'S LOAD CAPACITANCE IS 12.5PF

+3V_PMU
R535 10K 5% 1/16W MF 402 — 31 PMU_EPM
R569 10K 5% 1/16W MF 402 — 31 26 PMU_RESET_BUTTON_L
R585 100K 5% 1/16W MF 402 — 31 PMU_POWERUP_OK
R788 470K 5% 1/16W MF 402 — 31 PMU_BATT1_DET_L_PU
R592 470K 5% 1/16W MF 402 — 40 32 31 PMU_BATT_DET_L
RP41 10K 5% 1/16W SM1 — 31 26 PMU_NMI_BUTTON_L
RP41 10K 5% 1/16W SM1 — 31 PMU_NMI_L
R768 7.15K 1% 1/16W MF 402 — 32 31 PMU_SMB_DATA
R769 7.15K 1% 1/16W MF 402 — 32 31 PMU_SMB_CLK

+3V_SLEEP
RP41 10K 5% 1/16W SM1 — 31 PMU_I2C_DATA
RP41 10K 5% 1/16W SM1 — 31 PMU_I2C_CLK

+5V_SLEEP
R573 10K 5% 1/16W MF 402 — 31 TPAD_RXD
R584 10K 5% 1/16W MF 402 — 31 TPAD_TXD

+3V_MAIN
R597 100K 5% 1/16W MF 402 — 31 POWER_VALID
R596 10K 5% 1/16W MF 402 — 31 27 14 PMU_PME_L
R562 100K 5% 1/16W MF 402 — 31 23 PMU_LID_CLOSED_L
R583 10K 5% 1/16W MF 402 — 31 PMU_OOPS
R544 100K 5% 1/16W MF 402 — 31 26 13 INT_PU_RESET_L

PMU

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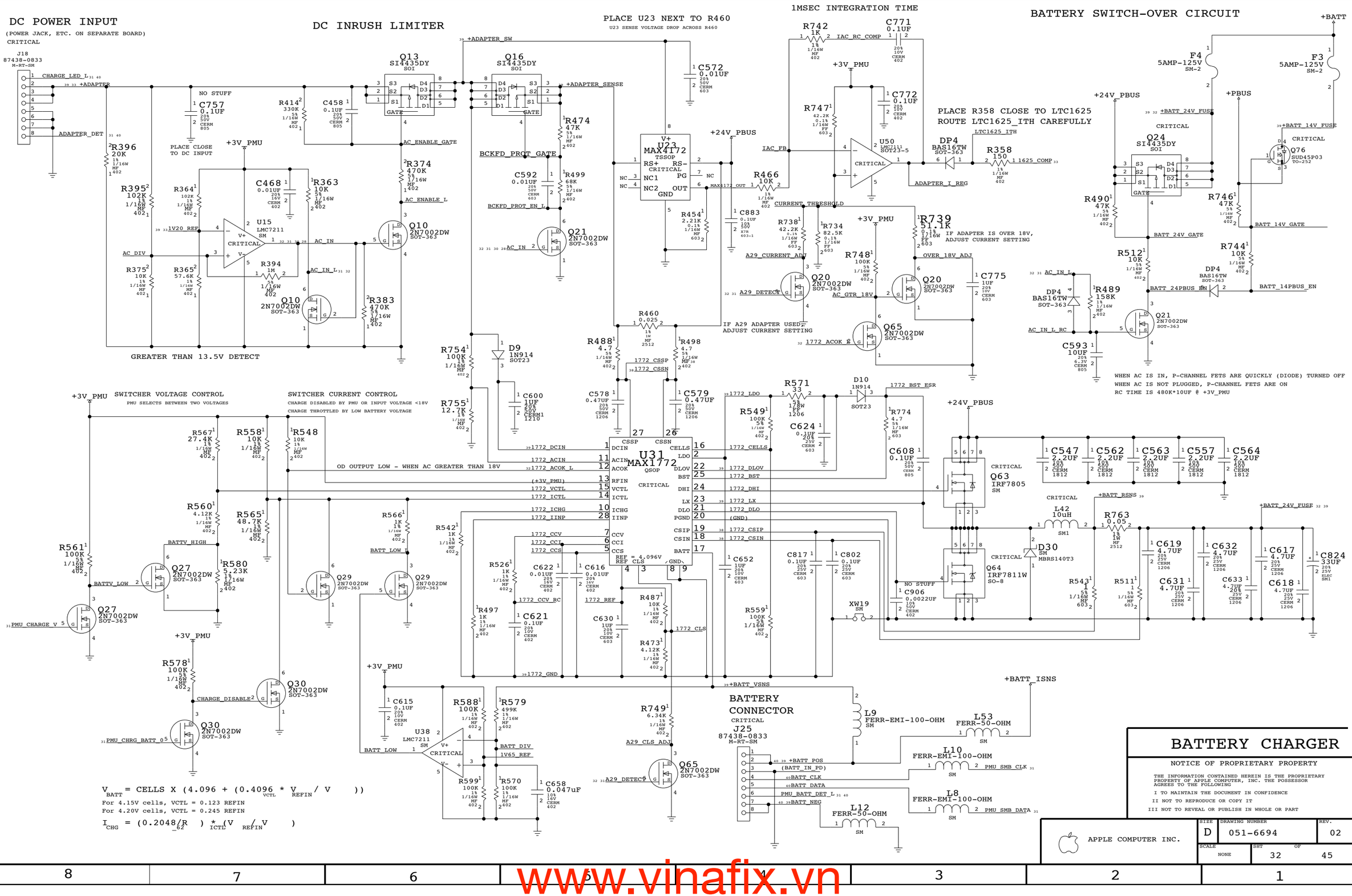
SIZE	DRAWING NUMBER	REV.
D	051-6694	02
SCALE: NONE	SHT 31 OF 45	



12.8V PBUS SUPPLY

CRITICAL
Q14
FDG6324L
SC70-6
+5V_MAIN
1625_EXTVCC
R426 470K 5% 1/16W MF 402
1625_ENABLE_L
CRITICAL
Q14
FDG6324L
SC70-6
1625_ENABLE
C495 0.1UF 20% 10V CERM 402
CONNECT LTC1625 TK PIN AT TOP-SIDE FET
KEEP VIN/TK LOOP SHORT
+3V_PMU
R443 102K 1% 1/16W MF 402
1V20_REF
C537 0.1UF 20% 10V CERM 402
U21 LMC7211 SM
CRITICAL
1625_DIV
R433 10K 1% 1/16W MF 402
R432 1M 1% 1/16W MF 402
WHEN +24V_PBUS IS BELOW ~13.44V, 1625 IS SHUT-OFF
R412 1 5% 1/16W MF 603
D4 1N914 SOT23
1625_VIN
1625_RUNSS
1625_COMP
1625_FCB
R379 4.99K 1% 1/16W MF 402
C510 0.1UF 20% 50V CERM 805
C485 4700pF 5% 25V CERM 603
COMP_FC
C462 470pF 10% 50V CERM 603
C463 4700pF 5% 25V CERM 603
NO STUFF
R402 0 5% 1/16W MF 402
R392 0 5% 1/16W MF 402
OMIT
XW4 SM
1625_SGND
1625_INTVCC
EXTVCC
U18 LTC1625
VIN SSOP BG
TK CRITICAL TG
SYNC VOSENSE
RUN/SS INTVCC
ITH
FCB BOOST
VPROG SW
SGND PGND
1625_TG
1625_BST_ESR
D3 MBR0540 SM
R401 2.2 5% 1/16W MF 603
C509 0.22UF 20% 25V CERM 805
1625_BST
1625_BG
NO STUFF
C461 4.7UF 20% 10V CERM 1206
C554 0.0047UF 10% 25V CERM 402
Q59 IRF7805 SM CRITICAL
CRITICAL
Q60 IRF7811W SO-8
D27 MBRS140T3 SM
1625_VSW
L37 CRITICAL
8.0UH-6.8A SM1
C535 4.7UF 20% 25V CERM 1206
C536 4.7UF 20% 25V CERM 1206
R359 158K 1% 1/16W MF 402
R360 16.2K 1% 1/16W MF 402
1625_VFB
+24V_PBUS
PBUS HOLD-UP CAPS
C644 2.2UF 10% 50V CERM 1812
C787 2.2UF 10% 50V CERM 1812
C585 2.2UF 10% 50V CERM 1812
C626 2.2UF 10% 50V CERM 1812
C801 2.2UF 10% 50V CERM 1812
C569 2.2UF 10% 50V CERM 1812
C604 2.2UF 10% 50V CERM 1812
C750 22uF 20% 35V ELEC SM-1
C799 22uF 20% 35V ELEC SM-1
C820 22uF 20% 35V ELEC SM-1
C821 22uF 20% 35V ELEC SM-1
C819 22uF 20% 35V ELEC SM-1
+PBUS
C765 33UF 20% 25V ELEC SM1
C769 33UF 20% 25V ELEC SM1
C794 33UF 20% 25V ELEC SM1
C822 33UF 20% 25V ELEC SM1
C793 33UF 20% 25V ELEC SM1
C758 33UF 20% 25V ELEC SM1

BACKUP BATTERY / USB CONNECTOR

CRITICAL
J11
54550-1490
F-RT-SM
+5V_MAIN
BOOTSTRAP SYSTEM FROM ADAPTER OR BATTERY
R508 390 5% 1/4W FF 1210
+ADAPTER
+ADAPTER_ILIM
D17 MBR0540 SM
+PBUS
+BATT
D18 1N914 SOT23
D19 MBR0540 SM
+ADAPTER_OR_BATT
NEC_RIGHT_USB_OVERCURRENT
RIGHT_USB_DM
RIGHT_USB_DP
NEC_RIGHT_USB_PWREN
NC
+24V_PBUS_CONN
R880 0 5% 1/4W FF 1210
BACKUP_BATT
+PBUS IS BOTH AN INPUT AND OUTPUT TO BUBBA
24V IS AN OUTPUT FROM BUBBA
R871 0 5% 1/4W FF 1210
SUPERCAP

PMU SUPPLY

+5V_MAIN
D7 MBR0520LT SM
D11 MBR0520LT SM
(+4_6V_BU)
+4_6V_BU
3V_PMU_VTAP
VTAP U25 LP2951 SOI-3.3V
IN OUT
SENSE ERROR
SHUT FDBK
GND
3V_PMU_SENSE
+3V_PMU
R468 1 5% 1/16W MF 603
+3V_PMU_ESR
C584 10UF 20% 6.3V CERM 805
C553 0.1UF 20% 10V CERM 402
NC
PLUS5VTAP U30 LP2951 SOI
IN OUT
SENSE ERROR
SHUT FDBK
GND
+4_85V_RAW
R521 294K 1% 1/16W MF 402
FB_4_85V_BU
C613 470pF 10% 50V CERM 603
R541 100K 1% 1/16W MF 402
R483 1 5% 1/16W MF 603
+4_85V_ESR
C568 2.2UF 20% 10V CERM 805
C625 0.1UF 20% 50V CERM 805
C599 0.1UF 20% 10V CERM 402

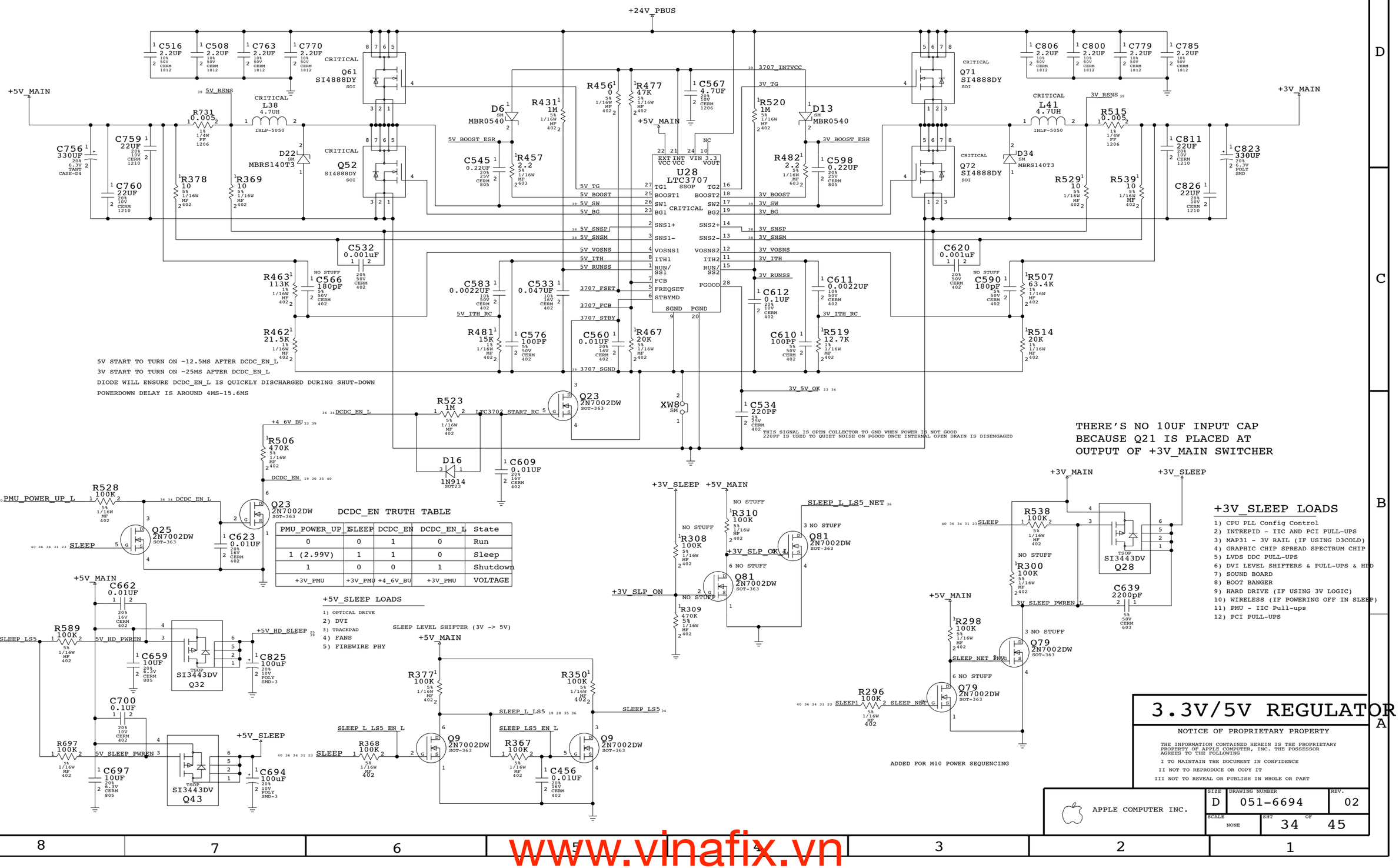
12.8V REGULATOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	02

SCALE	SHT	OF
NONE	33	45

3.3V/5V MAIN SUPPLY



3.3V/5V REGULATOR

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D	051-6694	02
SCALE: NONE	SHT 34 OF 45	

VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage
(approx. 7ms delay)

1.175V -> 1.025V 1.30V -> 0.975V

+5V_MAIN

MAXBUS_SLEEP

CPU_VCORE_PWR_SEQ

CPU_VCORE_SEQ_L

CPU_VCORE_SEQ

SLEEP_L_LS

DCDC_EN

CPU_VCORE_HI_OC

INT_GPIO1_PU

VCORE_SLOW<1>
VCORE_SLOW<2>
VCORE_SLOW<3>
VCORE_SLOW<4>

VCORE_FAST<1>
VCORE_FAST<2>
VCORE_FAST<3>
VCORE_FAST<4>

VCORE_MUX_SEL
VCORE_MUX_EN

U11 PI3B3257 QSOP
SEL = 0; Y1=A1
SEL = 1; Y1=B1

VCORE_VID<1>
VCORE_VID<2>
VCORE_VID<3>
VCORE_VID<4>

CPU_VCORE_SLEEP

Keep trace fat (40-100 mils) and short!!

+PBUS

PLACE C423 CLOSE TO PINS 15 & 13

U20 MAX1717 QSOP

VCORE_VCC
VCORE_BOOST
VCORE_VPLUS
VCORE_BST
VCORE_DH
VCORE_LX
VCORE_DL
VCORE_GND
VCORE_FB
VCORE_TIME
VCORE_VGATE

MAX1717_AB_SEL

MIN_LINE_WIDTH=10

Connect MAX1717 GND pin 13 to GND at bottom-side FET

Keep trace fat and short!!

XW15 SM

CPU_VCORE_SLEEP_F

L36 1.2UH-18.3A

R331 0.001 1% 1W MF 2512

D25 B540C SM

R732 2.2 5% 1/4W MF 1210

NO STUFF CPU_VCORE_SNUB

C764 0.0022UF 10% 50V CERM 603

XW3 SM

PLACE THIS SHORT AT PIN OF 1000uF CAP CLOSEST TO CPU

VCORE_GNDSNS
VCORE_SNS

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V WITH A 0.85 SCALE FACTOR, HENCE VOFFSET = 1.7V * (R1/(R1+R2)) AND VCORE = VDAC + VOFFSET.

NOTE: R310 (R2) NO STUFFED FOR NO OFFSET CASE

ROUTE AS DIFFERENTIAL PAIR

MAX1717 VID CAN TAKE 3.3V TO 5.5V INPUTS

OUTPUT VOLTAGE

V_{DAC} D4=0	V_{DAC} D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	A/B_ = Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1

If all pull-ups are >=100K and all pull-downs are <=1K, V B= V .

FMAX CONNECTOR

J5 M-ST-SM-52465-1217

VCORE_GNDDIV_TEST
VCORE_GNDSNS_TEST
+3V_PMU_RESET
SOFT_PWR_ON_L
NC (RFU)

VCORE SUPPLY

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	02
SCALE: NONE	SHT 35 OF 45	

1.5V/2.5V SWITCHER

+1_5V_SLEEP LOADS

1) AGP I/O - IF USING D3COLD
2) MAXBUS I/O - IF 1.5V INTERFACE

+1_5V_MAIN LOADS

1) INTREPID CORE
2) AGP I/O IF USING D3HOT

+2_5V_MAIN LOADS

1) MAP31 - FBCORE/FBIO IF USING D3HOT
2) GIGABIT ETHERNET - AVDDL
3) DDR SODIMMS - CORE/IO
4) DDR MUXES
5) CLOCK SLEWING I/O
6) PCI1510 CORE

+2_5V_SLEEP LOADS

1) FBCORE/FBIO IF USING D3COLD
2) INTREPID MEMORY I/O

THERE'S 100K PULL-UP ON PG 31 ALREADY

DIODE PROVIDE PROVIDE QUICK SHUT-DOWN POWER DOWN DELAY 1.5MS TO 3.25MS

CHANGE R424 BACK TO 10K, 1%, AND STUFF 5.11K FOR 1.5V OPERATION
CONNECTING 1_5V_FB TO GND, FORCES 1.8V OUTPUT

1.8V SWITCHER

+1_8V_MAIN LOADS

1) INTREPID PLLS

+1_8V_SLEEP LOADS

1) MPC7450 - MAXBUS I/O - IF 1.8V INTERFACE
2) CPU JTAG & MaxBus Pull-ups
3) CPU PLL Config Straps
4) OPTIONAL VIDEO MEMORY (M10 PRO ONLY)

1.5V/1.8V/2.5V SUPPLIES

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SCALE	SHT	OF
NONE	36	45

DIGITAL SIGNALS

GROUP	SIG_NAME		MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
MAXBUS	CPU_AACK_L				250.0000	10 MIL SPACING			5 8
	CPU_ADDR<0..31>		5		250			83 MHZ	5 8
	CPU_ARTRY_L				250.0000	10 MIL SPACING			5 8
	CPU_BG_L				250.0000	10 MIL SPACING			5 8
	CPU_BR_L				250.0000	10 MIL SPACING			5 8
	CPU_CI_L		5		250.0000				5 8
	CPU_DATA<0..31>		5		250			83 MHZ	6 8
	CPU_DATA<32..63>		5		250			83 MHZ	6 8
	CPU_DBG_L		5		250.0000	10 MIL SPACING			5 8
	CPU_DTI<0..2>		5		250				5 8
	CPU_DRDY_L_UF					10 MIL SPACING			
	CPU_DRDY_L				250.0000	10 MIL SPACING			5 8
	CPU_GBL_L		5		250.0000				5 8
	CPU_HIT_L				250.0000	10 MIL SPACING			5 8
	CPU_QACK_L		5		250.0000	10 MIL SPACING			5 8
	CPU_QREQ_L				250.0000	10 MIL SPACING			5 8
	CPU_TA_L				250.0000	10 MIL SPACING			5 8
	CPU_TBST_L		5		250.0000	10 MIL SPACING			5 8
	CPU_TEA_L				250.0000				5 8
	CPU_TS_L				250.0000	10 MIL SPACING			5 8
	CPU_TSIZ<0..2>		5		250				5 8
	CPU_TT<0..4>		5		250				5 8
	CPU_WT_L		5		250.0000				5 8
GROUP 0	MEM_DATA<7..0>		4		200			167 MHZ	9 10
	RAM_DATA_A<7..0>		4		200			167 MHZ	10 11
	RAM_DATA_B<7..0>		4		200			167 MHZ	10 11
	MEM_DQS<0>			TOTAL LENGTH CONTROLLED BY SPREADSHEET	200				9 10
	RAM_DQS_A<0>		4		200				10 11
	RAM_DQS_B<0>		4		200				10 11
	MEM_DQM<0>		4		200				9 10
	RAM_DQM_A<0>		4		200				10 11
	RAM_DQM_B<0>		4		200				10 11
GROUP 1	MEM_DATA<15..8>		4		200			167 MHZ	9 10
	RAM_DATA_A<15..8>		4		200			167 MHZ	10 11
	RAM_DATA_B<15..8>		4		200			167 MHZ	10 11
	MEM_DQS<1>		4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200				9 10
	RAM_DQS_A<1>		4		200				10 11
	RAM_DQS_B<1>		4		200				10 11
	MEM_DQM<1>				200				9 10
	RAM_DQM_A<1>		4		200				10 11
	RAM_DQM_B<1>		4		200				10 11
GROUP 2/3	MEM_DATA<31..16>		4		200			167 MHZ	9 10
	RAM_DATA_A<31..16>		4		200			167 MHZ	10 11
	RAM_DATA_B<31..16>		4		200			167 MHZ	10 11
	MEM_DQS<3..2>		4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200			167 MHZ	9 10
	RAM_DQS_A<3..2>		4		200			167 MHZ	10 11
DDR RAM	RAM_DQS_B<3..2>		4		200			167 MHZ	10 11
	MEM_DQM<3..2>		4		200			167 MHZ	9 10
	RAM_DQM_A<3..2>		4		200			167 MHZ	10 11
	RAM_DQM_B<3..2>		4		200			167 MHZ	10 11
GROUP 4/5	MEM_DATA<47..32>		4		200			167 MHZ	9 10
	RAM_DATA_A<47..32>		4		200			167 MHZ	10 11
	RAM_DATA_B<47..32>		4		200			167 MHZ	10 11
	MEM_DQS<5..4>		4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200			167 MHZ	9 10
	RAM_DQS_A<5..4>		4		200			167 MHZ	10 11
	RAM_DQS_B<5..4>		4		200			167 MHZ	10 11
	MEM_DQM<5..4>		4		200			167 MHZ	9 10
	RAM_DQM_A<5..4>		4		200			167 MHZ	10 11
	RAM_DQM_B<5..4>		4		200			167 MHZ	10 11
GROUP 6	MEM_DATA<55..48>		4		200			167 MHZ	9 10
	RAM_DATA_A<55..48>		4		200			167 MHZ	10 11
	RAM_DATA_B<55..48>		4		200			167 MHZ	10 11
	MEM_DQS<6>		4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200				9 10
	RAM_DQS_A<6>				200				10 11
	RAM_DQS_B<6>		4		200				10 11
	MEM_DQM<6>				200				9 10
	RAM_DQM_A<6>		4		200				10 11
	RAM_DQM_B<6>		4		200				10 11
GROUP 7	MEM_DATA<63..56>		4		200			167 MHZ	9 10
	RAM_DATA_A<63..56>		4		200			167 MHZ	10 11
	RAM_DATA_B<63..56>		4		200			167 MHZ	10 11
	MEM_DQS<7>		4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200				9 10
	RAM_DQS_A<7>				200				10 11
	RAM_DQS_B<7>				200				10 11
	MEM_DQM<7>		4		200				9 10
	RAM_DQM_A<7>		4		200				10 11
	RAM_DQM_B<7>		4		200				10 11
ADDR	MEM_ADDR<12..0>		4					83 MHZ	9
	RAM_ADDR<12..0>		6		200				9 11
	MEM_BA<1..0>		4						9
	RAM_BA<1..0>		6		200				9 11
CONTROL	MEM_CS_L<3..0>		4						9
	RAM_CS_L<3..0>		6		200				9 11
	MEM_CKE<3..0>		4						9
	RAM_CKE<3..0>		6		200				9 11
	MEM_RAS_L		4						9
	RAM_RAS_L				200.0000				9 11
	MEM_CAS_L		4						9
	RAM_CAS_L				200.0000				9 11
	MEM_WE_L		4						9
	RAM_WE_L				200.0000				9 11
	MEM_MUXSEL_H<1..0>		3						9 10
	MEM_MUXSEL_L<1..0>		3						9 10
	RAM_MUXSEL_H		5						10
	RAM_MUXSEL_L		5						10

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME			MAX VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM	
INTREPID CLOCKS	SYSCLK_CPU_UF						10 MIL SPACING		8
	SYSCLK_CPU			4		200.0000	10 MIL SPACING		5 8
	INT_CPUFB_OUT			3			10 MIL SPACING		8
	INT_CPUFB_OUT_SHORT			3			10 MIL SPACING		8
	INT_CPUFB_OUT_NORM			3			10 MIL SPACING		8
	INT_CPUFB_IN_NORM			3			10 MIL SPACING		8
	INT_CPUFB_LONG			3			10 MIL SPACING		8
	INT_CPUFB_IN					200.0000	10 MIL SPACING		8
	SYSCLK_DDRCLK_A0_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A0_L_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A1_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A1_L_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B0_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B0_L_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B1_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B1_L_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A0	DDRCLK_A0		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_A0_L	DDRCLK_A0				200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_A1	DDRCLK_A1		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_A1_L	DDRCLK_A1				200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B0	DDRCLK_B0		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B0_L	DDRCLK_B0		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B1	DDRCLK_B1		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B1_L	DDRCLK_B1		3		200.0000	10 MIL SPACING		9 11
	INT_REF_CLK_OUT			3		200.0000	10 MIL SPACING		14
	INT_REF_CLK_IN					200.0000	10 MIL SPACING		14
	CLK66M_GPU_AGP_UF					200.0000	10 MIL SPACING		12
	CLK66M_GPU_AGP			4		200.0000	10 MIL SPACING		12 18
	INT_AGP_FB_OUT					200.0000	10 MIL SPACING		12
	INT_AGP_FB_IN			4		200.0000	10 MIL SPACING		12
	CLK33M_CBUS_UF					200.0000	10 MIL SPACING		12
	CLK33M_CBUS		SHOULD BE AT MOST 4 VIAS FOR CLK			200.0000	10 MIL SPACING		12 17
	CLK33M_AIRPORT_UF					200.0000	10 MIL SPACING		12
	CLK33M_AIRPORT		SHOULD BE AT MOST 4 VIAS FOR CLK			200.0000	10 MIL SPACING		12 25 40
	CLK33M_USB2_UF					200.0000	10 MIL SPACING		12
	CLK33M_USB2		SHOULD BE AT MOST 4 VIAS FOR CLK			200.0000	10 MIL SPACING		12 27
	INT_PCI_FB_OUT					200.0000	10 MIL SPACING		12
	INT_PCI_FB_IN			3		200.0000	10 MIL SPACING		12
MAP31	GPU_CLK27M_OUT						10 MIL SPACING		
	GPU_CLK27M_UF						10 MIL SPACING		
	GPU_SSCLK_UF						10 MIL SPACING		
	GPU_SSCLK_IN						10 MIL SPACING		
	GPU_FBCLK0						10 MIL SPACING		
	GPU_FBCLK0_L						10 MIL SPACING		
	GPU_FBCLK1						10 MIL SPACING		
	GPU_FBCLK1_L						10 MIL SPACING		
	GPU_DVO_CLKP						10 MIL SPACING		19
CRYSTALS	CLK27M_GPU_XOUT						10 MIL SPACING		
	CLK27M_XTAL_IN						10 MIL SPACING		
	CLK27M_GPU_XIN						10 MIL SPACING		
	CLK18M_INT_XIN						10 MIL SPACING		14
	CLK18M_INT_XOUT						10 MIL SPACING		14
	CLK18M_XTAL_IN						10 MIL SPACING		14
	CLK18M_INT_EXT						10 MIL SPACING		14
	CLK25M_ENET_XIN						10 MIL SPACING		28
	CLK25M_ENET_XOUT						10 MIL SPACING		28
	NEC_XT1						10 MIL SPACING		27
	NEC_XT2		THERE'S ANOTHER 280MIL LEG				10 MIL SPACING		27
SOUND	SND_SCLK			7		200.0000	10 MIL SPACING		14 26 40
	SND_CLKOUT					200.0000	10 MIL SPACING		14 26 40
ETHERNET MARVELL	CLKENET_PHY_RX					200.0000			28
	CLKENET_LINK_RX			3		200.0000	10 MIL SPACING		13 28
	CLKENET_PHY_GBE_REF					200.0000			28
	CLKENET_LINK_GBE_REF			3		200.0000	10 MIL SPACING		13 28
	CLKENET_PHY_TX					200.0000			28
	CLKENET_LINK_TX			5		200.0000	10 MIL SPACING		13 28
	CLKENET_LINK_GTX					200.0000			13
	CLKENET_PHY_GTX			3		200.0000	10 MIL SPACING		13 28
FIREWIRE	CLKFW_PHY_PCLK					200.0000			29
	CLKFW_LINK_PCLK			3		200.0000	10 MIL SPACING		13 29
	CLKFW_PHY_LCLK			3		200.0000	10 MIL SPACING		13 29
	CLKFW_LINK_LCLK					200.0000			13
	FW_XI					200.0000	10 MIL SPACING		29
	FW_OSC					200.0000	10 MIL SPACING		29

SIGNAL CONSTRAINTS - PAGE 1

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	02

SCALE	SHT	OF
NONE	37	45

Digital Signals (cont'd)

GROUP	SIG_NAME	DELAY_RULE	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
AGP	AGP_AD<15..0>		5	100				66_MHz	12 18
AGP BYTES 0-1	AGP_CBE<1..0>		5	100				66_MHz	12 18
	AGP_AD_STB<0>		5	100		8_MIL_SPACING			12 18
	AGP_AD_STB_L<0>		5	100		8_MIL_SPACING			12 18
AGP BYTES 2-3	AGP_AD<31..16>		5	100				66_MHz	12 18
	AGP_CBE<3..2>		5	100				66_MHz	12 18
	AGP_AD_STB<1>		5	100		8_MIL_SPACING			12 18
	AGP_AD_STB_L<1>			100		8_MIL_SPACING			12 18
AGP SIDEBAND	AGP_SBA<7..0>		5	100				66_MHz	12 18
	AGP_SB_STB			100.0000		8_MIL_SPACING			12 18
	AGP_SB_STB_L		5	100.0000		8_MIL_SPACING			12 18
AGP CONTROL	AGP_FRAME_L			250.0000					12 18
	AGP_IRDY_L			250.0000					12 18
	AGP_TRDY_L		6	250.0000					12 18
	AGP_DEVSEL_L			250.0000					12 18
	AGP_STOP_L		6	250.0000					12 18
	AGP_PAR		6	250.0000					12 18
	AGP_REQ_L			285.0000					12 18
	AGP_GNT_L			250.0000					12 18
	AGP_RBF_L			250.0000					12 18
DVO	GPU_DVOD<0..23>		5	250					19 20
	GPU_DVO_HSYNC								19 20
	GPU_DVO_VSYNC								19 20
PCI	PCI_AD<31..0>					MIN_DAISY_CHAIN		33_MHz	9 12 17 25 27 40
	PCI_CBE<3..0>					MIN_DAISY_CHAIN		33_MHz	12 17 25 27 40
	PCI_FRAME_L					MIN_DAISY_CHAIN			12 17 25 27 40
	PCI_IRDY_L					MIN_DAISY_CHAIN			12 17 25 27 40
	PCI_TRDY_L					MIN_DAISY_CHAIN			12 17 25 27 40
	PCI_DEVSEL_L					MIN_DAISY_CHAIN			12 17 25 27 40
	PCI_STOP_L					MIN_DAISY_CHAIN			12 17 25 27 40
	PCI_PAR					MIN_DAISY_CHAIN			12 17 25 27 40
ULTRA ATA-100	UIDE_DATA<15..8>				200			100_MHZ	13 25
	UIDE_DATA<7>			NEED TO MATCH DELAY TO 250	200				13 25
	UIDE_DATA<6..0>				200			100_MHZ	13 25
	UIDE_ADDR<2..0>				200			100_MHZ	13 25
	UIDE_RST_L				200.0000				13 25
	UIDE_DIOW_L				200.0000				13 25
	UIDE_DIOR_L			10_MIL_SPACING	200.0000				13 25
	UIDE_DMACK_L				200.0000				13 25
	UIDE_CS0_L				200.0000				13 25
	UIDE_CS1_L				200.0000				13 25
	UIDE_DMARQ				200.0000				13
	UIDE_IOCHRDY			10_MIL_SPACING	200.0000				13 25
	UIDE_INTRQ				200.0000				13
	HD_DATA<15..0>		5	TOTAL UIDE+HD SKEW <500MIL	200			100_MHZ	25
	HD_ADDR<2..0>		5		200			100_MHZ	25
	HD_RESET_L		5		200.0000				25
	HD_DIOW_L		5		200.0000				25
	HD_DIOR_L		5	10_MIL_SPACING	200.0000				25
	HD_DMACK_L		5		200.0000				25
	HD_CS0_L		5		200.0000				25
	HD_CS1_L		5		200.0000				25
	HD_DMARQ				200.0000				13 25
	HD_IOCHRDY		5	10_MIL_SPACING	200.0000				25
	HD_INTRQ		5						13 25
EIDE INTREPID	EIDE_DATA<15..0>							33_MHZ	13 25
	EIDE_ADDR<2..0>							33_MHZ	13 25
	EIDE_CS0_L								13 25
	EIDE_CS1_L								13 25
	EIDE_RD_L								13 25
	EIDE_WR_L								13 25
	EIDE_IOCHRDY								13 25
	EIDE_INT								13 25
	EIDE_RST_L								13 25
	EIDE_DMACK_L								13 25
	EIDE_DMARQ								13 25
OPTICAL	EIDE_OPTICAL_DATA<15..0>							33_MHZ	25 40
	EIDE_OPTICAL_ADDR<2..0>							33_MHZ	25 40
	EIDE_OPTICAL_CS0_L								25 40
	EIDE_OPTICAL_CS1_L								25 40
	EIDE_OPTICAL_RD_L								25 40
	EIDE_OPTICAL_WR_L								25 40
	EIDE_OPTICAL_IOCHRDY								25 40
	EIDE_OPTICAL_INT								25 40
	EIDE_OPTICAL_RST_L								25 40
	EIDE_OPTICAL_DMAACK_L								25 40
	EIDE_OPTICAL_DMA_RQ								25 40
ETHERNET MII	ENET_LINK_RXD<7..0>		5						13 28
	ENET_RX_DV								13 28
	ENET_RX_ER								13 28
	ENET_PHY_TXD<7..0>		5						13 28
	ENET_LINK_TXD<7..0>								13
	ENET_PHY_TX_ER		5						13 28
	ENET_LINK_TX_ER								13
	ENET_PHY_TX_EN		5						13 28
	ENET_LINK_TX_EN								13
	ENET_MDIO								13 28
	ENET_MDC								13 28
	ENET_COL								13 28
	ENET_CRS								13 28
FIREWIRE MII	FW_LINK_DATA<7..0>		5						13 29
	FW_PHY_DATA<7..0>		5						29
	FW_LINK_CNTL<1..0>								13 29
	FW_PHY_CNTL<1..0>								29
	FW_LINK_LREQ								13
	FW_PHY_LREQ								13 29
	FW_PINT								13 29

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR	MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS	
ETHERNET	MDI_M<0>	ENET_MDI0				28
	MDI_P<0>	ENET_MDI0				28
	MDI_M<1>	ENET_MDI1	SPACING DELETED BECAUSE			28
	MDI_P<1>	ENET_MDI1	OF PHYSICAL CONSTRAINTS			28
	MDI_M<2>	ENET_MDI2	AROUND MARVELL PHY			28
	MDI_P<2>	ENET_MDI2				28
	MDI_M<3>	ENET_MDI3				28
	MDI_P<3>	ENET_MDI3				28
	RJ45_DN<0>	RJ45_DP0		10_MIL_SPACING		28 40
	RJ45_DP<0>	RJ45_DP0		10_MIL_SPACING		28 40
	RJ45_DN<1>	RJ45_DP1		10_MIL_SPACING		28 40
	RJ45_DP<1>	RJ45_DP1		10_MIL_SPACING		28 40
	RJ45_DN<2>	RJ45_DP2		10_MIL_SPACING		28 40
	RJ45_DP<2>	RJ45_DP2		10_MIL_SPACING		28 40
	RJ45_DN<3>	RJ45_DP3		10_MIL_SPACING		28 40
	RJ45_DP<3>	RJ45_DP3		10_MIL_SPACING		28 40
FIREWIRE	FW_TPA0N	FW_TPA0		MIN_LINE_WIDTH=3.4 10_MIL_SPACING		29 30
	FW_TPA0P	FW_TPA0		MIN_LINE_WIDTH=3.4 10_MIL_SPACING		29 30
	FW_TPB0N	FW_TPB0		MIN_LINE_WIDTH=3.4 10_MIL_SPACING		29 30
	FW_TPB0P	FW_TPB0		MIN_LINE_WIDTH=3.4 10_MIL_SPACING		29 30
	FW_TPI0N	FW_TPI0		MIN_LINE_WIDTH=3.4 10_MIL_SPACING		
	FW_TPI0P	FW_TPI0		MIN_LINE_WIDTH=3.4 10_MIL_SPACING		
	FW_TPO0N	FW_TPO0		MIN_LINE_WIDTH=3.4 10_MIL_SPACING		
	FW_TPO0P	FW_TPO0		MIN_LINE_WIDTH=3.4 10_MIL_SPACING		
	FW_TPA1N	FW_TPA1	500.0000	MIN_LINE_WIDTH=3.4 10_MIL_SPACING		29 30
	FW_TPA1P	FW_TPA1	500.0000	MIN_LINE_WIDTH=3.4 10_MIL_SPACING		29 30
	FW_TPB1N	FW_TPB1	500.0000	MIN_LINE_WIDTH=3.4 10_MIL_SPACING		29 30
	FW_TPB1P	FW_TPB1	500.0000	MIN_LINE_WIDTH=3.4 10_MIL_SPACING		29 30
	FW_TPI1N	FW_TPI1		MIN_LINE_WIDTH=3.4 10_MIL_SPACING		30 40
	FW_TPI1P	FW_TPI1		MIN_LINE_WIDTH=3.4 10_MIL_SPACING		30 40
	FW_TPO1N	FW_TPO1		MIN_LINE_WIDTH=3.4 10_MIL_SPACING		30 40
	FW_TPO1P	FW_TPO1		MIN_LINE_WIDTH=3.4 10_MIL_SPACING		30 40
LVDS LOWER	CLKLVDS_LN	CLKLVDS_L		10_MIL_SPACING	4	19 22 40
	CLKLVDS_LP	CLKLVDS_L		10_MIL_SPACING	4	19 22 40
	LVDS_L0N	LVDS_L0		10_MIL_SPACING		19 22 40
	LVDS_L0P	LVDS_L0		10_MIL_SPACING		19 22 40
	LVDS_L1N	LVDS_L1		10_MIL_SPACING		19 22 40
	LVDS_L1P	LVDS_L1		10_MIL_SPACING		19 22 40
	LVDS_L2N	LVDS_L2		10_MIL_SPACING		19 22 40
	LVDS_L2P	LVDS_L2		10_MIL_SPACING		19 22 40
UPPER	CLKLVDS_UN	CLKLVDS_U		10_MIL_SPACING	4	19 22 40
	CLKLVDS_UP	CLKLVDS_U		10_MIL_SPACING	4	19 22 40
	LVDS_U0N	LVDS_U0		10_MIL_SPACING		19 22 40
	LVDS_U0P	LVDS_U0		10_MIL_SPACING		19 22 40
	LVDS_U1N	LVDS_U1		10_MIL_SPACING		19 22 40
	LVDS_U1P	LVDS_U1		10_MIL_SPACING		19 22 40
	LVDS_U2N	LVDS_U2		10_MIL_SPACING		19 22 40
	LVDS_U2P	LVDS_U2		10_MIL_SPACING		19 22 40
TMDS	TMDS_CONN_CLKN	CLKCONN_TMDS		10_MIL_SPACING	4	22 40
	TMDS_CONN_CLKP	CLKCONN_TMDS		10_MIL_SPACING	4	22 40
	TMDS_CLKN	CLKTMDS		10_MIL_SPACING	4	20 22
	TMDS_CLKP	CLKTMDS		10_MIL_SPACING	4	20 22
	TMDS_DN<0>	TMDS_D0		10_MIL_SPACING		20 22 40
	TMDS_DP<0>	TMDS_D0		10_MIL_SPACING		20 22 40
	TMDS_DN<1>	TMDS_D1		10_MIL_SPACING		20 22 40
	TMDS_DP<1>	TMDS_D1		10_MIL_SPACING		20 22 40
	TMDS_DN<2>	TMDS_D2		10_MIL_SPACING		20 22 40
	TMDS_DP<2>	TMDS_D2		10_MIL_SPACING		20 22 40
USB	NEC_USB_DAM	NEC_USB_DA	MIN_LINE_WIDTH=5	10_MIL_SPACING		27
	NEC_USB_DAP	NEC_USB_DA	MIN_LINE_WIDTH=5	10_MIL_SPACING		27
	USB_DEM	USB_DE		5_MIL_SPACING		14
	USB_DEP	USB_DE		5_MIL_SPACING		14
	NEC_USB_DBM	NEC_USB_DB	MIN_LINE_WIDTH=5	10_MIL_SPACING		27
	NEC_USB_DBP	NEC_USB_DB	MIN_LINE_WIDTH=5	10_MIL_SPACING		27
	USB_DFM	USB_DF		5_MIL_SPACING		14
	USB_DFP	USB_DF		5_MIL_SPACING		14
	BT_USB_DM	BT_USB_D		5_MIL_SPACING		14 25 40
	BT_USB_DP	BT_USB_D		5_MIL_SPACING		14 25 40
	NEC_USB_RSDM1	NEC_USB_RSD1	MIN_LINE_WIDTH=5	10_MIL_SPACING		27
	NEC_USB_RSDP1	NEC_USB_RSD1	MIN_LINE_WIDTH=5	10_MIL_SPACING		27
	NEC_USB_RSDM2	NEC_USB_RSD2	MIN_LINE_WIDTH=5	10_MIL_SPACING		27
	NEC_USB_RSDP2	NEC_USB_RSD2	MIN_LINE_WIDTH=5	10_MIL_SPACING		27
	MODEM_USB_DM	MODEM_USB_D		5_MIL_SPACING		14 26 40
	MODEM_USB_DP	MODEM_USB_D		5_MIL_SPACING		14 26 40
	LEFT_USB_DM	LEFT_USB	MIN_LINE_WIDTH=5	10_MIL_SPACING		25 27 40
	LEFT_USB_DP	LEFT_USB	MIN_LINE_WIDTH=5	10_MIL_SPACING		25 27 40
	RIGHT_USB_DM	RIGHT_USB	MIN_LINE_WIDTH=5	10_MIL_SPACING		27 33 40
	RIGHT_USB_DP	RIGHT_USB	MIN_LINE_WIDTH=5	10_MIL_SPACING		27 33 40
POWER SUPPLIES	1772_CSSN	1772_CSS		DIFF		32
	1772_CSSP	1772_CSS		DIFF		32
	1772_CSIN	1772_CSI		DIFF		32
	1772_CSIP	1772_CSI		DIFF		32
	3V_SNSM	3V_SNS		DIFF		34
	3V_SNSP	3V_SNS		DIFF		34
	5V_SNSM	5V_SNS		DIFF		34
	5V_SNSP	5V_SNS		DIFF		34
THERMOSTAT	THERM1_DM	THERM1		DIFF		26
	THERM1_DP	THERM1		DIFF		26
	THERM2_DM	THERM2		DIFF		26
	THERM2_DP	THERM2		DIFF		26
	THERM1_M_DM	THERM1_MAIN		DIFF		
	THERM1_M_DP	THERM1_MAIN		DIFF		
	THERM2_M_DM	THERM2_MAIN		DIFF		
	THERM2_M_DP	THERM2_MAIN		DIFF		
	THERM1_A_DM	THERM1_ALT		DIFF		26
	THERM1_A_DP	THERM1_ALT		DIFF		26
	THERM2_A_DM	THERM2_ALT		DIFF		26
	THERM2_A_DP	THERM2_ALT		DIFF		26

INTERNAL LAYER
ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.57OHM
ZDIFF = 99.8OHM

FOR FIREWIRE
ER = 4.3 (DIELECTRIC CONSTANT)
W = 3.4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 53.37OHM
ZDIFF = 107.17OHM

INTERNAL LAYER (USB1.1/USB 2.0)
ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL(USB 1.1)/ 5MIL(USB 2.0) (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 5MIL (USB 1.1) (SEPERATION OF DIFF TRACES)
S = 10MIL (USB 2.0) (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.5OHM (USB 1.1)/ 46.2OHM (USB 2.0)
ZDIFF = 89.3OHM (USB 1.1)/ 89.4OHM (USB 2.0)

SIGNAL CONSTRAINTS - PAGE 2

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	02
SCALE: NONE	SHT 38 OF 45	

POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
MAIN/SLEEP	+24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	40
	+BATT	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	40
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23
	+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	20 23
	+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	40
	+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+2_5V_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	40
	+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	36
	+1_5V_SLEEP_VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	36
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	32 33
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	32
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	32
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32 40
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32 40
	1772_DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	1772_LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	32
	1772_LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32
	1772_DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32
	1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32
PMU	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	33
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	33
	+4_85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	31 33
	+4_6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	33 34
	+4_85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	33
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	33
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	26 31
MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 34
	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25
TRACKPAD	+5V_MAIN_CONN	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	23 40
VIDEO	+12_8V_INV	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 40
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 40
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22 40
	+5V_DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	22
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 40
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 40
KB LED	KBDLED_ANODE	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	23
	KBDLED_RETURN	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	23
FAN GND	FANL_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26 40
	FANR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26 40
SOUND	+5V_SOUND_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	SND_AGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=15	26

I/O AREA	GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	
	CHGND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND1
INVERTER	CHGND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND2
TRACKPAD	CHGND3	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND3
LVDS	CHGND4	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND4 40
I/O AREA	CHGND5	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND5
I/O AREA	CHGND6	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND6
	ENET_CTAP_CHGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	28

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 6 35 40
	CPU_AVDD	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 6 7 8 15 16 35
DDR RAM	DDR_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	11
INTREPID PLLS	+2_5V_INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	9 10 15 16
	+3V_INTREPID_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14
	+1_5V_INTREPID_PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	8 12 14
	+1_5V_INTREPID_PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5	14
	+1_5V_INTREPID_PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5	12
	+1_5V_INTREPID_PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	8
	+1_5V_INTREPID_PLL8	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
REFERENCE	INT_MEM_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	9
	INT_AGP_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	12 18
	INT_MEM_REF_H	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	9
	UIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	13
CARDBUS	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN NECK WIDTH REDUCED FOR TESTPOINTS MIN_NECK_WIDTH=10	17
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
ATI M10	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	18 19 40
	+GPU_MEM	VOLTAGE=2.5V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	18 21
	+3V_GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 18 19 21
	+3V_GPU_FLT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	21
	+1_5V_AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 15 16 18 19 21
	GPU_MEM_IO	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	GPU_MEM_IO_FLT	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+GPU_MEMCORE	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+1_8V_GPU	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18 19 20 21
	+2_5V_GPU_PNLIO	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_8V_ATI_PVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19 21
	+1_5V_AGP_GPU	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_5V_GPU_VDD15	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	+1_8V_GPU_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_VDDDI	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	GPU_VCORE_VDDCI	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	18
	+2_5V_GPU_A2VDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_PNLPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_PNLIO	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+GPU_MCLK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_AVDDQ	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_MEMPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+3V_ATI_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	18
	+3V_ATI_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	18
	+GPU_VDD15_UF	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	+2_5V_SLEEP_NECK1	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	+3V_SLEEP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+1_5V_AGP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	+1_8V_PVDD_NECK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	GPU_VCORE_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	+GPU_VDD15_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	+2_5V_SLEEP_NECK2	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+1_8V_SLEEP_NECK	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+1_5V_SLEEP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+2_5V_GPU	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
SILICON IMIAGE	PP3V3_SI_PVCC1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0	20
	PP3V3_SI_AVCC1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0	20
	PP3V3_SI_VCC1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0	20
	PP3V3_SI_PVCC2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0	20
	PP3V3_SI_AVCC2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0	20
	PP3V3_SI_VCC2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0	20
88E1111	+2_5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+2_5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	28
	+1_0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	28
FW	LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	28
	LM2594_IN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+3V_FW_ESD_ILIM	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+3V_FW_ESD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+FW_FUSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30
	+FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30
	+FW_PWR_OR	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29 30
	+FW_VP0	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30
	+FW_PWR_PORTA	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30
	+FW_VP1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30
	+3V_FW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29 30
	+3V_FW_UF	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	29
	+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_PLLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30
	FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30
	FW_TPO0R	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30 40
USB 2.0 INTREPID SSCG	NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_CG_PLL_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	14
	+2_5V_CG_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	14

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	33
	1625_VSW	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	33
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	33
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	33
	1V20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	32 33
LTC3707 5V SWITCHER	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	32 34
	5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	34
	5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	34
3V SWITCHER	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	34
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	34
	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	34
MAX1715 2.5V SWITCHER	2_5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	36
	2_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	36
	2_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	36
	2_5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	36
	2_5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	36
1.5V SWITCHER	1_5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	36
	1_5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	36
	1_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	36
	1_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	36
	1_5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	36
	1_5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	36
CONTROL	1_5V_ILIM		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	36
	2_5V_ILIM		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	36
	MAX1715_TON		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	36
	MAX1715_SKIP		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	36
	MAX1715_REF	VOLTAGE=2.0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	36
	MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	36
	MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	36
MAX1717	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=200	MIN_NECK_WIDTH=10	35
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	VCORE_ILIM		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	VCORE_REF		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	VCORE_CC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35 40
	VCORE_TIME		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	VCORE_VGATE		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	14 35
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=15	35
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
LTC1778	1778_VIN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	19
	1778_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	1778_BST_RC	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	1778_TG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_BG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	GPU_VCORE_SW	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	19
	1778_ION		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19
	1778_ITH		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19
	1778_ITH_RC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19
	1_5V_2_5V_OK		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	36
	1778_VFB		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19 40
	1778_FCB		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19
	1778_VRNG		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19
LTC3411	LTC3411_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC3411_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	
	1_8V_SW	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	36
	1_8V_VFB		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
	LTC3411_ITH_RC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
	LTC3411_ITH		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
	LTC3411_SYNC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
	LTC3411_SHDN		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
LTC1962 INT PLLS	LTC1962_INT_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	14
	LTC1962_L3_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_L3_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_1V5_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_1V5_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	

SIGNAL CONSTRAINTS - PAGE 4

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FUNCTIONAL TEST POINTS

FUNC_TEST=YES JTAG_ASIC_TMS 13 28
FUNC_TEST=YES JTAG_ASIC_TDI 28
FUNC_TEST=YES JTAG_ASIC_TDO 13 14
FUNC_TEST=YES JTAG_ASIC_TCK 13 28
FUNC_TEST=YES JTAG_ASIC_TRST_L 13 28
FUNC_TEST=YES CPU_CHKSTP_OUT_L 5
FUNC_TEST=YES CPU_SRESET_L 5
FUNC_TEST=YES CPU_HRESET_L 5 6 7
FUNC_TEST=YES JTAG_CPU_TMS 5 6 23
FUNC_TEST=YES JTAG_CPU_TDI 5 6 23
FUNC_TEST=YES JTAG_CPU_TDO_TP 5
FUNC_TEST=YES JTAG_CPU_TCK 5 6
FUNC_TEST=YES JTAG_CPU_TRST_L 5 6 23 40

FUNC_TEST=YES INT_I2C_CLK0 6 11 13 23
FUNC_TEST=YES INT_I2C_DATA0 6 11 13 23
FUNC_TEST=YES INT_I2C_CLK1 13 14 23 24 26
FUNC_TEST=YES INT_I2C_DATA1 13 14 23 24 26
FUNC_TEST=YES CBUS_DET_1_L 17
FUNC_TEST=YES CBUS_DET_2_L 17
FUNC_TEST=YES TMDS_DN<0> 20 22 38
FUNC_TEST=YES TMDS_DP<0> 20 22 38
FUNC_TEST=YES TMDS_DN<1> 20 22 38
FUNC_TEST=YES TMDS_DP<1> 20 22 38
FUNC_TEST=YES TMDS_DN<2> 20 22 38
FUNC_TEST=YES TMDS_DP<2> 20 22 38
FUNC_TEST=YES TMDS_CONN_CLKN 22 38

FUNC_TEST=YES TMDS_CONN_CLKP 22 38
FUNC_TEST=YES VGA_R 22
FUNC_TEST=YES VGA_G 22
FUNC_TEST=YES VGA_B 22
FUNC_TEST=YES VGA_VSYNC 22
FUNC_TEST=YES VGA_HSYNC 22
FUNC_TEST=YES DVI_DDC_CLK_UF 22
FUNC_TEST=YES DVI_DDC_DATA_UF 22
FUNC_TEST=YES DVI_HPD_UF 22
FUNC_TEST=YES LVDS_L0N 19 22 38
FUNC_TEST=YES LVDS_L0P 19 22 38
FUNC_TEST=YES LVDS_L1N 19 22 38
FUNC_TEST=YES LVDS_L1P 19 22 38
FUNC_TEST=YES LVDS_L2N 19 22 38
FUNC_TEST=YES LVDS_L2P 19 22 38
FUNC_TEST=YES CLKLVDS_LN 19 22 38
FUNC_TEST=YES CLKLVDS_LP 19 22 38
FUNC_TEST=YES LVDS_U0N 19 22 38
FUNC_TEST=YES LVDS_U0P 19 22 38
FUNC_TEST=YES LVDS_U1N 19 22 38
FUNC_TEST=YES LVDS_U1P 19 22 38
FUNC_TEST=YES LVDS_U2N 19 22 38
FUNC_TEST=YES LVDS_U2P 19 22 38
FUNC_TEST=YES CLKLVDS_UN 19 22 38
FUNC_TEST=YES CLKLVDS_UP 19 22 38
FUNC_TEST=YES LVDS_DDC_CLK 19 22
FUNC_TEST=YES LVDS_DDC_DATA 19 22
FUNC_TEST=YES BRIGHT_PWM 22
FUNC_TEST=YES TV_GND1 22 39
FUNC_TEST=YES TV_GND2 22 39

FUNC_TEST=YES TV_C 22
FUNC_TEST=YES TV_Y 22
FUNC_TEST=YES TV_COMP 22
FUNC_TEST=YES SND_TO_AUDIO 14 26
FUNC_TEST=YES SND_SYNC 14 26
FUNC_TEST=YES SND_CLKOUT 14 26 37

FUNC_TEST=YES INT_AUDIO_TO_SND 14 26
FUNC_TEST=YES SND_SCLK 14 26 37
FUNC_TEST=YES SND_HW_RESET_L 14 26
FUNC_TEST=YES SND_HP_SENSE_L
FUNC_TEST=YES SND_LIN_SENSE_L
FUNC_TEST=YES INT_I2C_DATA2 14 26
FUNC_TEST=YES INT_I2C_CLK2 14 26
FUNC_TEST=YES CHGND4 39
FUNC_TEST=YES SLEEP_LED

FUNC_TEST=YES BT_USB_DM 14 25 38
FUNC_TEST=YES BT_USB_DP 14 25 38
FUNC_TEST=YES MODEM_USB_DM 14 26 38
FUNC_TEST=YES MODEM_USB_DP 14 26 38
FUNC_TEST=YES PCI_AD<0> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<1> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<2> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<3> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<4> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<5> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<6> 9 12 17 25 27 38

FUNC_TEST=YES PCI_AD<7> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<8> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<9> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<10> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<11> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<12> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<13> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<14> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<15> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<16> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<17> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<18> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<19> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<20> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<21> 12 17 25 27 38
FUNC_TEST=YES PCI_AD<22> 12 17 25 27 38
FUNC_TEST=YES PCI_AD<23> 12 17 25 27 38
FUNC_TEST=YES PCI_AD<24> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<25> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<26> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<27> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<28> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<29> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<30> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<31> 9 12 17 25 27 38
FUNC_TEST=YES PCI_FRAME_L 12 17 25 27 38
FUNC_TEST=YES PCI_TRDY_L 12 17 25 27 38
FUNC_TEST=YES PCI_IRDY_L 12 17 25 27 38
FUNC_TEST=YES PCI_DEVSEL_L 12 17 25 27 38
FUNC_TEST=YES PCI_STOP_L 12 17 25 27 38

FUNC_TEST=YES PCI_PAR 12 17 25 27 38
FUNC_TEST=YES PCI_CBE<0> 12 17 25 27 38
FUNC_TEST=YES PCI_CBE<1> 12 17 25 27 38
FUNC_TEST=YES PCI_CBE<2> 12 17 25 27 38
FUNC_TEST=YES PCI_CBE<3> 12 17 25 27 38
FUNC_TEST=YES AIRPORT_PCI_REQ_L 12 25
FUNC_TEST=YES AIRPORT_PCI_GNT_L 12 25
FUNC_TEST=YES AIRPORT_PCI_INT_L 14 25
FUNC_TEST=YES EIDE_OPTICAL_DATA<0> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<1> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<2> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<3> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<4> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<5> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<6> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<7> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<8> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<9> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<10> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<11> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<12> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<13> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<14> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<15> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DMA_RQ 25 38
FUNC_TEST=YES EIDE_OPTICAL_RD_L 25 38
FUNC_TEST=YES EIDE_OPTICAL_DMAACK_L 25 38
FUNC_TEST=YES EIDE_OPTICAL_ADDR<0> 25 38
FUNC_TEST=YES EIDE_OPTICAL_ADDR<1> 25 38
FUNC_TEST=YES EIDE_OPTICAL_ADDR<2> 25 38
FUNC_TEST=YES SND_AMP_MUTE 26
FUNC_TEST=YES SND_HP_MUTE_INV

FUNC_TEST=YES EIDE_OPTICAL_CS0_L 25 38
FUNC_TEST=YES EIDE_OPTICAL_CS1_L 25 38
FUNC_TEST=YES EIDE_OPTICAL_RST_L 25 38
FUNC_TEST=YES EIDE_OPTICAL_WR_L 25 38
FUNC_TEST=YES EIDE_OPTICAL_IOCHRDY 25 38
FUNC_TEST=YES EIDE_OPTICAL_INT 25 38
FUNC_TEST=YES TPAD_F_TXD
FUNC_TEST=YES TPAD_F_RXD
FUNC_TEST=YES LID_CLOSED_L 23
FUNC_TEST=YES COMM_RESET_L 14 26
FUNC_TEST=YES COMM_SHUTDOWN 14 26
FUNC_TEST=YES COMM_RING_DET_L 14 26 31

FUNC_TEST=YES +5V_TPAD_SLEEP
FUNC_TEST=YES +3V_HALL_EFFECT 23 39
FUNC_TEST=YES KBD_CAPSLOCK_LED
FUNC_TEST=YES KBD_FUNCTION_L 23 31
FUNC_TEST=YES KBD_CONTROL_L 23 31
FUNC_TEST=YES +PPBATT_ISNS_N 24
FUNC_TEST=YES KBD_OPTION_L 23 31
FUNC_TEST=YES KBD_SHIFT_L 23 31
FUNC_TEST=YES KBD_X<0> 23 31
FUNC_TEST=YES KBD_X<1> 23 31
FUNC_TEST=YES KBD_X<3> 23 31
FUNC_TEST=YES MMM_ACC_SELFTEST 24
FUNC_TEST=YES MMM_ACC_X_AXIS 24
FUNC_TEST=YES MMM_ACC_Y_AXIS 24
FUNC_TEST=YES MMM_ACC_Z_AXIS 24

FUNC_TEST=NO KBD_X<8> 23 31
FUNC_TEST=YES SRCLK_TP 27
FUNC_TEST=YES SRMOD_TP 27
FUNC_TEST=YES TEB_TP 27
FUNC_TEST=YES TEST_TP 27

FUNC_TEST=YES KBD_Y<0> 31
FUNC_TEST=YES KBD_Y<1> 31
FUNC_TEST=YES KBD_Y<3> 31
FUNC_TEST=YES KBD_Y<4> 31
FUNC_TEST=YES KBD_Y<6> 31
FUNC_TEST=YES KBD_Y<7> 31
FUNC_TEST=YES KBD_NUMLOCK_LED
FUNC_TEST=YES +BATT_POS 32 39
FUNC_TEST=YES BATT_CLK 32
FUNC_TEST=YES BATT_DATA 32
FUNC_TEST=YES BATT_NEG 32 39
FUNC_TEST=YES PMU_BATT_DET_L 31 32
FUNC_TEST=YES FANR_GND 26 39
FUNC_TEST=YES FANL_GND 26 39
FUNC_TEST=YES FANL_TACH 26
FUNC_TEST=YES FANR_PWM 26
FUNC_TEST=YES FANL_PWM 26
FUNC_TEST=YES RJ45_DP<0> 28 38
FUNC_TEST=YES RJ45_DN<0> 28 38
FUNC_TEST=YES RJ45_DP<1> 28 38
FUNC_TEST=YES RJ45_DN<1> 28 38
FUNC_TEST=YES RJ45_DP<2> 28 38
FUNC_TEST=YES RJ45_DN<2> 28 38
FUNC_TEST=YES RJ45_DP<3> 28 38
FUNC_TEST=YES RJ45_DN<3> 28 38
FUNC_TEST=YES FW_TPO0R 30 39
FUNC_TEST=YES VCORE_VID0
FUNC_TEST=YES VCORE_VID1
FUNC_TEST=YES VCORE_VID2
FUNC_TEST=YES VCORE_VID3
FUNC_TEST=YES VCORE_VID4

FUNC_TEST=YES FW_TPO1P 30 38
FUNC_TEST=YES FW_TPO1N 30 38
FUNC_TEST=YES FW_TPI1P 30 38
FUNC_TEST=YES FW_TPI1N 30 38
FUNC_TEST=YES CHARGE_LED_L 31 32
FUNC_TEST=YES ADAPTER_DET 31 32
FUNC_TEST=YES SUTRO_ALS_GAIN_SW 23 25
FUNC_TEST=YES SUTRO_ALS_OUT 23 25
FUNC_TEST=YES KBD_LED1_OUT
FUNC_TEST=YES KBD_LED2_OUT
FUNC_TEST=YES COMM_TXD_L 14 26
FUNC_TEST=YES COMM_TRXC 14 26
FUNC_TEST=YES COMM_GPIO_L 14 26
FUNC_TEST=YES COMM_DTR_L 14 26
FUNC_TEST=YES COMM_RTS_L 14 26
FUNC_TEST=YES COMM_RXD 14 26
FUNC_TEST=YES PMU_KB_RESET_L
FUNC_TEST=YES PWR_BUTTON_L 23 26
FUNC_TEST=YES +PBUS 39
FUNC_TEST=YES +24V_PBUS 39
FUNC_TEST=YES GPU_VCORE 18 19 39
FUNC_TEST=YES CPU_VCORE_SLEEP 5 6 35 39
FUNC_TEST=YES VCORE_FB 35 39
FUNC_TEST=YES +1_8V_MAIN 39
FUNC_TEST=YES +3V_PMU 39
FUNC_TEST=YES +5V_DDC_SLEEP 22 39
FUNC_TEST=YES +12_8V_INV 22 39
FUNC_TEST=YES VCORE_MUX_EN 35

FUNC_TEST=YES +5V_INV_SW 22 39
FUNC_TEST=YES LEFT_USB_DM 25 27 38
FUNC_TEST=YES LEFT_USB_DP 25 27 38
FUNC_TEST=YES RIGHT_USB_DM 27 33 38
FUNC_TEST=YES RIGHT_USB_DP 27 33 38
FUNC_TEST=YES NEC_LEFT_USB_PWREN 25 27
FUNC_TEST=YES NEC_LEFT_USB_OVERCURRENT 25 27
FUNC_TEST=YES NEC_RIGHT_USB_PWREN 27 33
FUNC_TEST=YES NEC_RIGHT_USB_OVERCURRENT 27 33
FUNC_TEST=YES DCDC_EN 19 30 34 35
FUNC_TEST=YES BBANG_HRESET_L 6 23

FUNC_TEST=YES MAIN_RESET_L 14 17 18 20 25 27 31
FUNC_TEST=YES RF_DISABLE_L_SPN 25
FUNC_TEST=YES AIRPORT_CLKRUN_L 25
FUNC_TEST=YES ROM_RW_L 9 12 25
FUNC_TEST=YES ROM_ONBOARD_CS_L 9 25
FUNC_TEST=YES ROM_CS_L 9 12 25
FUNC_TEST=YES CLK33M_AIRPORT 12 25 37
FUNC_TEST=YES AIRPORT_IDSEL 25
FUNC_TEST=YES ROM_OE_L 9 12 25
FUNC_TEST=YES INT_MOD_DTI 14 26
FUNC_TEST=YES JTAG_CPU_TRST_L 5 6 23 40
FUNC_TEST=YES MOD_BITCLK 14 26
FUNC_TEST=YES MOD_CLKOUT 14 26
FUNC_TEST=YES MOD_DTO 14 26
FUNC_TEST=YES MOD_SYNC 14 26
FUNC_TEST=YES SLEEP 23 31 34 36
FUNC_TEST=YES 1778_VFB 19 39

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SCALE: NONE	SHT 40 OF 45	

REVISION HISTORY

12/11/03

1) IMPORTED Q41 PRODUCTION RELEASE SCHEMATIC
2) CHANGED CPU (U43) TO A7PM
3) CHANGED PLL CONFIG STUFFING FOR NEW CPU
4) CHANGED U44 TO M1Y-PSP64 SYMBOL
5) ADDED CPU AVDD LDO (U6)
6) ADDED R284 AND R604 TO ADD OPTION FOR PD_I OF U42 (CLOCK CHIP) TO BE DRIVEN BY JTAG_ASIC_TDO FROM INTREPID
7) ADDED R608 TO DISCONNECT INT_GPIO0 FROM CG_FSEL
8) CHANGED JTAG_ASIC_TDO_TP TO JTAG_ASIC_TDO AND MOVED IT TO INTREPID'S TDO
9) CHANGED JTAG_ASIC_TDI TO CONNECT TO ETHERNET PHY'S TDI

12/15/03

10) CHANGED PIN 4 (DCDC_EN) ON J11 TO NEC_RIGHT_USBOVERCURRENT
11) CHANGED PIN 11 OF J11 TO NC

12/16/03

12) ADDED R633 AS PULLUP ON JTAG_ASIC_TDI
13) CHANGED CPU_TEMP_DN TO CPU_THERM_DM
14) CHANGED CPU_TEMP_DP TO CPU_THERM_DP
15) CHANGED GPU_THERM_DP TO GPU_THERM_DP_TP
16) CHANGED GPU_THERM_DN TO GPU_THERM_DM_TP
17) FIXED MISSED CONNECTION WITH MAXBUS_SLEEP TO CPU

12/17/03

18) CHANGED R657 (EXTPLL_SDWN_POL_BOOT_STRAP) TO NO_STUFF AND REMOVED NO_STUFF FROM R153
19) UPDATE DIFF_NET_SPACING_TYPE PROPERTY ON POWER_SUPPLY_SENSE AND THERMAL_DIODE_DIFF_PAIRS
20) CHANGED FIREWIRE OSCILLATOR (G1) TO NEW PREFERRED SUNNY PART

12/18/03

21) CHANGED MAX VIA COUNT ON ALL AGP STB NETS TO 5 TO CLEAR DRCS

** RELEASED FOR EVT **

2/10/04

22) REMOVED XW11 - JUMPER ON 1.8V SWITCHER OUTPUT
23) CHANGED R657 TO STUFFE AND R153 TO NO STUFF
24) CHANGED CPU PLL CONFIG TO 9X HIGH AND 5X LOW

** RELEASED FOR DVT **

3/24/04

25) REMOVED ALTERNATE BOM OPTION FROM ALTERNATE ETHERNET CRYSTALS

3/29/04

26) ADDED ALTERNATE FOR Q41A REV 1.1.1 CPU (U43)
27) ADDED ALTERNATES FOR 128MB AND 64MB A16_M11S
28) CHANGED TMDS SERIES RPAKS TO 0 OHMS (RP57,RP27,RP32,RP28)
29) ADDED ALTERNATE FOR ALS OP-AMP (U40)

** RELEASED TO REV A **

30) CHANGED TMDS TERMINATION R,C AND LS TO PRODUCTION VALUES

** RELEASED TO REV A UNDER NEW PART NUMBER **

09/17/2004

1) GPU_DVOD<0..12> NETNAME CHANGE TO GPU_DVOD<0..23>
2) D8 FROM 1N5227B CHANGE TO BZX84C2V7LT1
3) R751 VALUE FROM 10K OHM CHANGE TO 604 OHM
4) ADD C935 (0.1UF)
5) ADD R867 (0 OHM) FOR IPOD ACTION
6) PMU PIN74 NETNAME FROM NC TO PMU_SELECT
7) ADD R868 (10K OHM; NO_STUFF) PULL UP TO +3V_PMU
8) ADD R869 (10K OHM) PULL DOWN TO GND
9) PMU PIN 91 NETNAME FROM NC TO SYS_BATT_ISNS2
10) ADD R870 (0 OHM) SYS_BATT_ISNS2 LINK TO SYS_BATT_ISNS
11) ADD U51 (INA138)
12) ADD R852 (0.010 OHM),R853 (150K OHM) AND R857(49.9 OHM)
13) ADD C917 (0.1UF) AND C925 (10UF)
14) ADD DESCRIPTION FOR MMM I2C BUS
15) MMM I2C BUS LINK TO INTREPID :INT_I2C_CLK1 AND INT_I2C_DATA1
16) CHANGE NETNAME FROM INT_EXTINT11_PU TO MMM_FFIRQ_L
17) CHANGE NETNAME FROM INT_EXTINT12_PU TO MMM_SIRQ_L
18) ADD R863 (10K OHM) AND R864 (10K OHM) FOR MMM_FFIRQ_L&MMM_SIRQ_L PULL UP TO +3V_MAIN
19) ADD U53 (16F818) AND U5 (KXM52)
20) ADD R845 (0 OHM),R846 (0 OHM;NO_STUFF),R847 (10K OHM;NO_STUFF),R848 (10K OHM;NO_STUFF)
21) ADD R849 (10K OHM),R850 (10K OHM;NO_STUFF),R851(0 OHM),R854 (10K OHM),R856 (10K OHM),
22) ADD R860 (0 OHM),R858 (0 OHM),R859 (0 OHM),R855 (10K OHM),R861 (10K OHM),R862(10K OHM;NO_STUFF)
23) ADD C936(0.1UF),C918(0.1UF),C919(0.1UF),C921(0.0047UF),C923(0.0047UF),C926(0.0047UF),C927(0.1UF)
24) DEL RP44 (100K OHM) AND ADD R874 (100K OHM), R875 (100K OHM) AND R873 (100K OHM)
25) ADD R872 (10K OHM) FOR AUDIO_LO_MUTE_L
26) ADD R871 (100 OHM) AND SUPERCAP C937 (N20P80;5.5V;ELEC;0.33F)
27) J21 PIN12 NETNAME FROM NC CHANGE TO THERM_L_OC
28) J21 PIN10 NETNAME FROM NC CHANGE TO INT_I2C_DATA1
29) J21 PIN11 NETNAME FROM NC CHANGE TO INT_I2C_CLK1
30) C592 VALUE FROM 0.001UF CHANGE TO 0.01UF (20%,50V,0603)
31) U59 FROM MP1518DJ CHANGE TO MM3120
32) L11 CHANGE TO 152S0235 (22UH;3.8*3.8*1.5MM)
33) DEL D31
34) R202 VALUE FROM 5.23 OHM CHANGE TO 25.5 OHM
35) C79 VALUE FROM 2.2UF CHANGE TO 1UF
36) ADD Q70 (SI3443), Q34 (2N7002)
37) ADD R866 (100K OHM),R865 (4.7 OHM),C929 (0.022UF)

09/20/2004

1) ADD R877 (10K OHM)
2) ADD R876 (470K OHM;NO_STUFF)

09/21/2004

1) ADD R878 AND R879 (0 OHM;NO_STUFF)[ADD A 0-OHM RESISTOR TO BY-PASS THE N-FET ON EACH FAN]

09/22/2004

1) R822 (680 OHM CHANGE TO 510 OHM) AND R826 (680 OHM CHANGE TO 510 OHM)

09/23/2004

1) ADD NC NETNAME AT U59 PIN6 AND PIN9
2) CHANGE R465 CAP SIZE FROM 0603 TO 0805
3) BOM OPTION FROM NO STUFF CHANGE TO SUPERCAP

09/24/2004

1) CHANGE R465 FROM MF 1/16W TO FF 1/10W
2) ADD R880 AND R871 (0 OHM;BOM_OPTIOM;FOR SUPERCAP AND BACKUP BATTERY SWITCH)
3) ADD U60 (LIS3L02AQ;ST SENSOR)
4) ADD R881 (10K OHM) ,R882 (10K OHM), R883 (10K OHM)
5) ADD C937 (0.1UF,10V,20%,0402)
6) ADD BOM_OPTION (KIONIX_ACCEL AND ST_ACCEL)

10/04/2004

1) CHANGE TEST POINT FUNC_TEST=NO FOR FUNC_TP_WRONG_SIDE.LOG
2) ADD NO_TEST=YES FOR NOTP.LOG(MMM_PIC_AN2_PD,MMM_PIC_AN3_PU)

10/05/2004

1) ADD R850 (0 OHM)

QUANTA EE, PLEASE ADD SCHEMATIC UPDATE DETAILS HERE.

10/15/2004

1) REPLACE BOOT BANGER EEPROM U32 WITH 32KX M24256B FUNC_TP_WRONG_SIDE.LOG

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	02

SCALE	SHT	OF
NONE	41	45

*** Signal Cross-Reference for the entire design ***

```
+1_0V_MARVELL    28D2< 39B3>
+1_5V_AGP        12C5< 12D1< 12D4< 15D6< 16C8<
               18C6< 18D6< 19A8< 19B4<> 19D5<>
               21B8< 21D6< 39C3>
+1_5V_AGP_GPU    21C5< 39C3>
+1_5V_AGP_NECK   19B4<> 39B3>
+1_5V_GPU_VDD15  19D3< 39C3>
+1_5V_INTREPID_PLL  8D6< 12D4< 12D8< 14D6<> 39D3>
+1_5V_INTREPID_PLL1  14C3< 39D3>
+1_5V_INTREPID_PLL2  14D3< 39D3>
+1_5V_INTREPID_PLL3  14D3< 39D3>
+1_5V_INTREPID_PLL4  14D3< 39D3>
+1_5V_INTREPID_PLL5  12D3< 39D3>
+1_5V_INTREPID_PLL6  12D6< 39D3>
+1_5V_INTREPID_PLL7  8D5< 39D3>
+1_5V_INTREPID_PLL8  14D3< 39D3>
+1_5V_LDO        36D8< 39D6>
+1_5V_MAIN       39D6>
+1_5V_SLEEP      39D6>
+1_5V_SLEEP_NECK  21A3<> 39B3>
+1_5V_SLEEP_VIN  36D8<> 39D6>
+1_8V_ATI_PVDD   19C5<> 21B6< 21B6< 21D6<> 39C3>
+1_8V_ATI_TPVDD  21D2<>
+1_8V_DVO_F      21B2<
+1_8V_GPU        18A7< 19C8< 20A8< 21A2< 21A6<
               21B1< 21B6< 21C8< 21D6< 21D8< 39C3>
+1_8V_GPU_AVDD   21D5< 39C3>
+1_8V_GPU_AVDDQ  21D4< 21D7< 39C3>
```

```
NEC_USB_DBM         27A4< 27C2<> 38B2>
NEC_USB_DBP         27A4< 27C2<> 38B2>
NEC_USB_RSDM1       27C5<> 38B2>
NEC_USB_RSDM2       27C5<> 38B2>
NEC_USB_RSDP1       27C5<> 38B2>
NEC_USB_RSDP2       27C5<> 38B2>
NEC_XT1             27D5< 37B1>
NEC_XT2             27D5<> 37B1>
NEC_XT2_R           27D4<
NTEST1_TP           27B5<
NUMLOCK_LED_L       31D7<
OVER_18V_ADJ        32C3<>
PCI1510_VR_EN_L     17C7<
PCI_AD<0>           9C3< 12D6<> 17C7<> 25B5<> 27D7<>
                  40B6>
PCI_AD<31..0>       38C5>
PCI_AD<1>           9C3< 12D6<> 17C7<> 25B6<> 27D7<>
                  40A6>
PCI_AD<2>           9C3< 12D6<> 17C7<> 25C5<> 27D7<>
                  40A6>
PCI_AD<3>           9C3< 12D6<> 17C7<> 25C6<> 27C7<>
                  40A6>
PCI_AD<4>           9C3< 12D6<> 17C7<> 25C5<> 27C7<>
                  40A6>
PCI_AD<5>           9C3< 12D6<> 17C7<> 25C6<> 27C7<>
                  40A6>
PCI_AD<6>           9C3< 12C6<> 17C7<> 25C5<> 27C7<>
                  40A6>
PCI_AD<7>           9C3< 12C6<> 17C7<> 25C6<> 27C7<>
                  40D5>
PCI_AD<8>           9C3< 12C6<> 17C7<> 25C6<> 27C7<>
                  40D5>
PCI_AD<9>           9C3< 12C6<> 17C7<> 25C5<> 27C7<>
                  40D5>
PCI_AD<10>          9C3< 12C6<> 17C7<> 25C6<> 27C7<>
                  40D5>
PCI_AD<11>          9C3< 12C6<> 17C7<> 25C5<> 27C7<>
                  40D5>
PCI_AD<12>          9C3< 12C6<> 17C7<> 25C6<> 27C7<>
                  40D5>
PCI_AD<13>          9C3< 12C6<> 17C7<> 25C5<> 27C7<>
                  40C5>
PCI_AD<14>          9C3< 12C6<> 17C7<> 25C6<> 27C7<>
                  40C5>
PCI_AD<15>          9C3< 12C6<> 17C7<> 25C5<> 27C7<>
                  40C5>
PCI_AD<16>          9C3< 12C6<> 17C7<> 25C5<> 27C7<>
                  40C5>
PCI_AD<17>          9C3< 12C6<> 17C7<> 25C6<> 27C7<>
                  40C5>
PCI_AD<18>          9C3< 12C6<> 17B7<> 25C5<> 25D4<
                  27C7<> 40C5>
PCI_AD<19>          9C3< 12C6<> 17B7<> 25C6<> 27C7<>
                  40C5>
PCI_AD<20>          9B3< 12C6<> 17B7<> 25C5<> 27C7<>
                  40C5>
PCI_AD<21>          12C6<> 17B7<> 25C6<> 27C7<> 40C5>
PCI_AD<22>          12C6<> 17B7<> 25C5<> 27C7<> 40B5>
PCI_AD<23>          12C6<> 17B7<> 25C6<> 27C7<> 40B5>
PCI_AD<24>          9C1<> 12C6<> 17B7<> 25C5<> 27C7<>
                  40B5>
PCI_AD<25>          9C1<> 12C6<> 17B7<> 25D6<> 27C7<>
                  40B5>
PCI_AD<26>          9C1<> 12C6<> 17B7<> 25C5<> 27C7<>
                  40B5>
PCI_AD<27>          9C1<> 12C6<> 17B7<> 25D6<> 27C8<>
                  40B5>
PCI_AD<28>          9C1<> 12C6<> 17B7<> 25D5<> 27C7<>
                  40B5>
PCI_AD<29>          9C1<> 12C6<> 17B7<> 25D6<> 27B7<>
                  40B5>
PCI_AD<30>          9C1<> 12C6<> 17B7<> 25D5<> 27B7<>
                  40B5>
PCI_AD<31>          9C1<> 12C6<> 17B7<> 25D6<> 27B7<>
                  40A5>
PCI_CBE<0>          12C7<> 17B7<> 25C5<> 27B7<> 40D4>
PCI_CBE<3..0>       38C5>
PCI_CBE<1>          12C7<> 17B7<> 25C6<> 27B7<> 40D4>
PCI_CBE<2>          12C7<> 17B7<> 25C6<> 27B7<> 40D4>
PCI_CBE<3>          12C7<> 17B7<> 25C6<> 27B7<> 40D4>
PCI_DEVSEL_L        12B7< 12C7<> 17A7<> 25C5<> 27B7<>
                  38C5> 40A5>
PCI_FRAME_L         12B7< 12C7<> 17B7<> 25C5<> 27B7<>
                  38C5> 40A5>
PCI_IRDY_L          12B7< 12C7<> 17B7<> 25C6<> 27B7<>
                  38C5> 40A5>
PCI_PAR             12C7<> 17B7<> 25C5<> 27B7<> 38C5>
                  40D4>
PCI_STOP_L          12A7< 12C7<> 17B7<> 25C5<> 27B7<>
                  38C5> 40A5>
PCI_TRDY_L          12B7< 12C7<> 17A7<> 25C5<> 27B7<>
                  38C5> 40A5>
PLL_STOP_L          7C4<> 7C8<>
PMU_ACK_L           14C2< 31C4<>
PMU_AC_DET          31A5< 31B4<>
PMU_AC_IN           31B4<>
PMU_BATT0_DET_L     31B4<>
PMU_BATT1_DET_L_PU  31B4<> 31D2<
PMU_BATT_DET_L      31A8<> 31B3< 31D2< 32A4<> 40C3>
PMU_BYTE            31B6< 31C7<
PMU_CAPSLOCK_LED_L  31C6<>
PMU_CHARGE_V        31C4<> 32B8<>
PMU_CHRG_BATT_0     31C4<> 32A8<>
PMU_CLK             14C2<> 31C4<>
PMU_CNVSS           31B6< 31C7<
PMU_CPU_HRESET_L    6A2< 6C3<> 23C4<> 31C4<>
PMU_CUSTOM_RESET    31A8<>
PMU_CUSTOM_RESET_L  31A7<> 31B8<
PMU_EPM             31D2< 31D4<>
PMU_FROM_INT        14C2<> 31C4<>
PMU_I2C_CLK         31B4<> 31C2<
PMU_I2C_DATA        31B4<> 31C2<
PMU_INT_L           14B5<> 14B7< 31B6<>
PMU_INT_NMI         14B5<> 14B7< 31D4<>
PMU_KB_RESET_L      40B2>
PMU_LID_CLOSED_L    23A8< 23C4<> 31B2< 31C4<>
PMU_NMI_BUTTON_L    26B3< 31C2< 31C4<>
PMU_NMI_L           31C2< 31C4<>
PMU_NUMLOCK_LED_L   31C6<>
PMU_OOPS            31B2< 31B4<>
PMU_PME_L           14B5<> 27B8< 31B2< 31C4<>
PMU_POWERUP_OK      31B4<> 31D2<
PMU_POWER_UP_L      30D8<> 31C6<> 31D7< 34B8<
PMU_REQ_L           14B7< 14C2> 31C4<>
PMU_RESET_BUTTON_L  26B3< 31C4<> 31D2<
PMU_RESET_L         31B7<>
PMU_SELECT          31C6<>
PMU_SLEEP_LED       23C4<>
PMU_SLEEP_LED_L     23C2<> 31C4<>
PMU_SMB_CLK         31B4<> 31C2< 32A3<
PMU_SMB_DATA        31B4<> 31C2< 32A2<
PMU_TO_INT          14C2<> 31C4<>
POWER_UP            30D8<>
POWER_VALID         31B2< 31C4<>
PP3V3_MMM           24C8< 24D6<
PP3V3_MMM_PIC       24C1< 24D5<
PP3V3_SI_AVCC1      20D7< 39B3>
PP3V3_SI_AVCC2      20C5< 39B3>
PP3V3_SI_PVCC1      20C7< 39B3>
PP3V3_SI_PVCC2      20C5< 39B3>
PP3V3_SI_VCC1       20D7< 39B3>
PP3V3_SI_VCC2       20C5< 39B3>
PWR_BUTTON_L        23A7<> 26C1< 40B2>
RAM_ADDR<0>         9B4< 11B5<> 11B6<>
RAM_ADDR<12..0>     37A5>
RAM_ADDR<1>         9B4< 11B3<> 11B8<>
RAM_ADDR<2>         9B4< 11B5<> 11B6<>
RAM_ADDR<3>         9B4< 11B3<> 11B8<>
RAM_ADDR<4>         9B4< 11B5<> 11B6<>
RAM_ADDR<5>         9B4< 11B3<> 11B8<>
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RAM_ADDR<8>         9B4< 11B5<> 11B6<>
RAM_ADDR<9>         9A4< 11B3<> 11B8<>
RAM_ADDR<10>        9A4< 11B3<> 11B8<>
RAM_ADDR<11>        9A4< 11B5<> 11B6<>
RAM_ADDR<12>        9A4< 11B3<> 11B8<>
RAM_BA<0>           9A4< 11B3<> 11B8<>
RAM_BA<1..0>        37A5>
RAM_BA<1>           9A4< 11B5<> 11B6<>
RAM_CAS_L           9A4< 11B5<> 11B6<> 37A5>
RAM_CKE<0>          9A3< 9C4< 11B6<>
RAM_CKE<3..0>       37A5>
RAM_CKE<1>          9A3< 9C4< 11B8<>
RAM_CKE<2>          9A3< 9C4< 11C5<>
RAM_CKE<3>          9A3< 9C4< 11C3<>
RAM_CS_L<0>         9C4< 11B8<>
RAM_CS_L<3..0>      37A5>

RAM_CS_L<1>         9C4< 11B6<>
RAM_CS_L<2>         9C4< 11B3<>
RAM_CS_L<3>         9C4< 11B5<>
RAM_DATA_A<0>       10C8<> 11D8<>
RAM_DATA_A<7..0>    37C5>
RAM_DATA_A<1>       10C8<> 11D8<>
RAM_DATA_A<2>       10C8<> 11D8<>
RAM_DATA_A<3>       10B8<> 11D8<>
RAM_DATA_A<4>       10B8<> 11D6<>
RAM_DATA_A<5>       10B8<> 11D6<>
RAM_DATA_A<6>       10B8<> 11D6<>
RAM_DATA_A<7>       10B8<> 11D6<>
RAM_DATA_A<8>       10B8<> 11D8<>
RAM_DATA_A<15..8>   37C5>
RAM_DATA_A<9>       10C7<> 11D8<>
RAM_DATA_A<10>      10C7<> 11D8<>
RAM_DATA_A<11>      10C7<> 11D8<>
RAM_DATA_A<12>      10C7<> 11D6<>
RAM_DATA_A<13>      10C7<> 11D6<>
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RAM_DATA_A<15>      10C7<> 11D6<>
RAM_DATA_A<16>      10C6<> 11D8<>
RAM_DATA_A<31..16>  37B5>
RAM_DATA_A<17>      10C6<> 11C8<>
RAM_DATA_A<18>      10C6<> 11C8<>
RAM_DATA_A<19>      10B6<> 11C8<>
RAM_DATA_A<20>      10B6<> 11D6<>
RAM_DATA_A<21>      10B6<> 11C6<>
RAM_DATA_A<22>      10B6<> 11C6<>
RAM_DATA_A<23>      10B6<> 11C6<>
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RAM_DATA_A<26>      10C5<> 11C8<>
RAM_DATA_A<27>      10C5<> 11C8<>
RAM_DATA_A<28>      10C5<> 11C6<>
RAM_DATA_A<29>      10C5<> 11C6<>
RAM_DATA_A<30>      10C5<> 11C6<>
RAM_DATA_A<31>      10C5<> 11C6<>
RAM_DATA_A<32>      10C4<> 11B8<>
RAM_DATA_A<47..32>  37B5>
RAM_DATA_A<33>      10C4<> 11B8<>
RAM_DATA_A<34>      10C4<> 11B8<>
RAM_DATA_A<35>      10C4<> 11B8<>
RAM_DATA_A<36>      10B4<> 11B6<>
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RAM_DATA_A<44>      10C3<> 11B6<>
RAM_DATA_A<45>      10C3<> 11B6<>
RAM_DATA_A<46>      10C3<> 11A6<>
RAM_DATA_A<47>      10C3<> 11A6<>
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RAM_DATA_A<55..48>  37B5>
RAM_DATA_A<49>      10C2<> 11A8<>
RAM_DATA_A<50>      10C2<> 11A8<>
RAM_DATA_A<51>      10C2<> 11A8<>
RAM_DATA_A<52>      10B2<> 11A6<>
RAM_DATA_A<53>      10B2<> 11A6<>
RAM_DATA_A<54>      10B2<> 11A6<>
RAM_DATA_A<55>      10B2<> 11A6<>
RAM_DATA_A<56>      10B2<> 11A8<>
RAM_DATA_A<63..56>  37A5>
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RAM_DATA_A<58>      10C1<> 11A8<>
RAM_DATA_A<59>      10C1<> 11A8<>
RAM_DATA_A<60>      10C1<> 11A6<>
RAM_DATA_A<61>      10C1<> 11A6<>
RAM_DATA_A<62>      10C1<> 11A6<>
RAM_DATA_A<63>      10C1<> 11A6<>
RAM_DATA_B<0>       10C8<> 11D3<>
RAM_DATA_B<7..0>    37C5>
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RAM_DATA_B<2>       10C8<> 11D3<>
RAM_DATA_B<3>       10C8<> 11D3<>
RAM_DATA_B<4>       10C8<> 11D5<>
RAM_DATA_B<5>       10C8<> 11D5<>
RAM_DATA_B<6>       10C8<> 11D5<>
RAM_DATA_B<7>       10C8<> 11D5<>
RAM_DATA_B<8>       10C8<> 11D3<>
RAM_DATA_B<15..8>   37C5>
RAM_DATA_B<9>       10C8<> 11D3<>
RAM_DATA_B<10>      10C8<> 11D3<>
RAM_DATA_B<11>      10C8<> 11D3<>
RAM_DATA_B<12>      10C8<> 11D5<>
RAM_DATA_B<13>      10C8<> 11D5<>
RAM_DATA_B<14>      10C8<> 11D5<>
RAM_DATA_B<15>      10C8<> 11D5<>
RAM_DATA_B<16>      10C6<> 11D3<>
RAM_DATA_B<31..16>  37B5>
RAM_DATA_B<17>      10C6<> 11C3<>
RAM_DATA_B<18>      10C6<> 11C3<>
RAM_DATA_B<19>      10C6<> 11C3<>
RAM_DATA_B<20>      10C6<> 11D5<>
RAM_DATA_B<21>      10C6<> 11C5<>
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RAM_DATA_B<24>      10C6<> 11C3<>
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RAM_DATA_B<28>      10C6<> 11C5<>
RAM_DATA_B<29>      10C6<> 11C5<>
RAM_DATA_B<30>      10C6<> 11C5<>
RAM_DATA_B<31>      10C6<> 11C5<>
RAM_DATA_B<32>      10D4<> 11B3<>
RAM_DATA_B<47..32>  37B5>
RAM_DATA_B<33>      10C4<> 11B3<>
RAM_DATA_B<34>      10C4<> 11B3<>
RAM_DATA_B<35>      10C4<> 11B3<>
RAM_DATA_B<36>      10C4<> 11B5<>
RAM_DATA_B<37>      10C4<> 11B5<>
RAM_DATA_B<38>      10C4<> 11B5<>
RAM_DATA_B<39>      10C4<> 11B5<>
RAM_DATA_B<40>      10C4<> 11B3<>
RAM_DATA_B<41>      10C4<> 11B3<>
RAM_DATA_B<42>      10C4<> 11A3<>
RAM_DATA_B<43>      10C4<> 11A3<>
RAM_DATA_B<44>      10C4<> 11B5<>
RAM_DATA_B<45>      10C4<> 11B5<>
RAM_DATA_B<46>      10C4<> 11A5<>
RAM_DATA_B<47>      10C4<> 11A5<>
RAM_DATA_B<48>      10D2<> 11A3<>
RAM_DATA_B<55..48>  37B5>
RAM_DATA_B<49>      10C2<> 11A3<>
RAM_DATA_B<50>      10C2<> 11A3<>
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RAM_DATA_B<55>      10C2<> 11A5<>
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RAM_DATA_B<63..56>  37A5>
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RAM_DATA_B<62>      10C2<> 11A5<>
RAM_DATA_B<63>      10C2<> 11A5<>
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RAM_DQM_A<1>        10C7<> 11D6<> 37C5>
RAM_DQM_A<2>        10B6<> 11C6<>
RAM_DQM_A<3..2>     37B5>
RAM_DQM_A<3>        10C5<> 11C6<>
RAM_DQM_A<4>        10B4<> 11B6<>
RAM_DQM_A<5..4>     37B5>
RAM_DQM_A<5>        10C3<> 11A6<>
RAM_DQM_A<6>        10B2<> 11A6<> 37B5>
RAM_DQM_A<7>        10C1<> 11A6<> 37A5>
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RAM_DQM_B<1>        10C8<> 11D5<> 37C5>
RAM_DQM_B<2>        10C6<> 11C5<>
RAM_DQM_B<3..2>     37B5>
RAM_DQM_B<3>        10C6<> 11C5<>
RAM_DQM_B<4>        10C4<> 11B5<>
RAM_DQM_B<5..4>     37B5>
RAM_DQM_B<5>        10C4<> 11B5<>
RAM_DQM_B<6>        10C2<> 11A5<> 37B5>
RAM_DQM_B<7>        10C2<> 11A5<> 37A5>
RAM_DQS_A<0>        10B8<> 11D8<> 37C5>
RAM_DQS_A<1>        10C7<> 11D8<> 37C5>
RAM_DQS_A<2>        10B6<> 11C8<>
RAM_DQS_A<3..2>     37B5>
RAM_DQS_A<3>        10C5<> 11C8<>

RAM_DQS_A<4>        10B4<> 11B8<>
RAM_DQS_A<5..4>     37B5>
RAM_DQS_A<5>        10C3<> 11A8<>
RAM_DQS_A<6>        10B2<> 11A8<> 37B5>
RAM_DQS_A<7>        10C1<> 11A8<> 37A5>
RAM_DQS_B<0>        10C8<> 11D3<> 37C5>
RAM_DQS_B<1>        10C8<> 11D3<> 37C5>
RAM_DQS_B<2>        10C6<> 11C3<>
RAM_DQS_B<3..2>     37B5>
RAM_DQS_B<3>        10C6<> 11C3<>
RAM_DQS_B<4>        10C4<> 11B3<>
RAM_DQS_B<5..4>     37B5>
RAM_DQS_B<5>        10C4<> 11B3<>
RAM_DQS_B<6>        10C2<> 11A3<> 37B5>
RAM_DQS_B<7>        10C2<> 11A3<> 37A5>
RAM_MUXSEL_H        10A3< 10A5< 10B1<> 10B3<> 37A5>
RAM_MUXSEL_L        10A3< 10A5< 10B5<> 10B7<> 37A5>
RAM_RAS_L           9A4< 11B5<> 11B6<> 37A5>
RAM_WE_L            9A4< 11B3<> 11B8<> 37A5>
RESET_VREF          6C3<>
RF_DISABLE_L_SPN    25D6<> 40C1>
RIGHT_USB_DM        27A3< 33A7<> 38A2> 40D1>
RIGHT_USB_DP        27A3< 33A7<> 38A2> 40D1>
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RJ45_C1_PD          28B2<>
RJ45_C2_PD          28B2<>
RJ45_C3_PD          28B2<>
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RJ45_DN<1>          28B2<> 38D2> 40B3>
RJ45_DN<2>          28B2<> 38D2> 40A3>
RJ45_DN<3>          28B2<> 38D2> 40A3>
RJ45_DP<0>          28B2<> 38D2> 40B3>
RJ45_DP<1>          28B2<> 38D2> 40B3>
RJ45_DP<2>          28B2<> 38D2> 40A3>
RJ45_DP<3>          28B2<> 38D2> 40A3>
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ROM_OE_L            9B3< 12A5< 25C5<> 40B1>
ROM_ONBOARD_CS_L    9B3< 25C6<> 40B1>
ROM_RW_L            9B3< 12A5< 25C6<> 40B1>
ROM_WP_L            9B3<
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RSDM4_TP            27C5>
RSDM5_TP            27C5>
RSDP3_TP            27C5>
RSDP4_TP            27C5>
RSDP5_TP            27C5>
RUN_OR_AC           30D7<>
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SI_I2C_DATA         19C5<> 20B5<> 20C7<>
SI_MASTER           20B8<
SI_M_HTPLG          20B7<
SI_RESET_L          19C8< 20B5< 20C3< 20C7<
SI_SECONDARY        20A7<
SI_S_HTPLG          20A5<
SI_TMDS_CLKN        20B5< 20B7<
SI_TMDS_CLKP        20B5< 20B7<
SI_TMDS_DN<0>       20B5< 20B7<
SI_TMDS_DN<1>       20B5< 20B7<
SI_TMDS_DN<2>       20A5< 20B7<
SI_TMDS_DN<3>       20A5< 20A5<
SI_TMDS_DN<4>       20A5< 20A5<
SI_TMDS_DN<5>       20A5< 20A5<
SI_TMDS_DP<0>       20B5< 20B7<
SI_TMDS_DP<1>       20B5< 20B7<
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SLEEP_LED_L         23D2<
SLEEP_LED_SW_L      23C2<>
SLEEP_LED_UF        23C1<
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SLEEP_L_LS5_INV     36A3< 36C2< 36C8<>
SLEEP_L_LS5_NET     34B3<> 36C8<>
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SLEEP_NET_INV       34A3<>
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SND_AMP_MUTE        26D4<> 26D4< 40A4>
SND_AMP_MUTE_INV    26C8< 26D5<
SND_AMP_MUTE_L      14C5<> 26D3<>
SND_CLKOUT          14B1< 26D8< 37B1> 40D6>
SND_HP_MUTE         26C4<>
SND_HP_MUTE_INV     40A4>
SND_HP_MUTE_L       14C5<> 26C4<>
SND_HP_SENSE_L      40C6>
SND_HW_RESET_L      14A7< 14B5<> 26C8< 40C6>
SND_LIN_SENSE_L     40C6>
SND_SCLK            14B1< 26C8< 37B1> 40C6>
SND_SYNC            14B1< 26D8< 40D6>
SND_TO_AUDIO        14B1< 26C8< 40D6>
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SRMOD_TP            27A5< 40A4>
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ST7_OSC1            23D5<
ST7_OSC2            23D5<>
ST7_PB6_PD          23B2< 23C4<>
ST7_RESET_L         23D5<>
ST7_SENSOR4_SCK_PD  23B2< 23D4<>
ST7_SENSOR4_SDA_PD  23B2< 23D4<>
ST7_SENSOR5_SCK_PU  23B2< 23D4<>
ST7_SENSOR5_SDA_PU  23B2< 23D4<>
ST7_SLEEP_LED_H     23C2<> 23C4<>
ST7_XTAL_IN         23C5<
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SUPPLY_M_DM         26A8< 26B6<
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SUTRO_ALS_OUT       23C4<> 25B2<> 40C2>
SYSCLK_CPU          5C4< 8A6< 37D1>
SYSCLK_CPU_UF       8A6<> 37D1>
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SYSCLK_DDRCLK_A0_L_UF  9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_A0_UF  9B6<> 9D5< 37D1>
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SYSCLK_DDRCLK_A1_L  9D4< 11A6<> 37D1>
SYSCLK_DDRCLK_A1_L_UF  9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_A1_UF  9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_B0    9D4< 11D3<> 37D1>
SYSCLK_DDRCLK_B0_L  9C4< 11D3<> 37C1>
SYSCLK_DDRCLK_B0_L_UF  9B6<> 9C5< 37D1>
SYSCLK_DDRCLK_B0_UF  9B6<> 9D5< 37D1>
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SYSCLK_DDRCLK_B1_L  9D4< 11A5<> 37C1>
SYSCLK_DDRCLK_B1_L_UF  9B6<> 9D5< 37D1>
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THERM2_DP           26A5< 26B5<> 26B5< 38A2>
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TMDS_CONN_CLKP      22C6<> 22C7<> 38B2> 40D7>
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TMDS_CONN_DN<5>     20C1<> 22C7<>
TMDS_CONN_DP<0>     22B7<> 22D6<>
TMDS_CONN_DP<1>     22B7<> 22D5<>
TMDS_CONN_DP<2>     22B6<> 22D5<>
TMDS_CONN_DP<3>     20D1<> 22C5<>
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                  40A8>
TMDS_DN<2>          20A3< 20A4< 20C2< 22B7<> 38B2>
                  40A8>
TMDS_DN<3>          20A4< 20C1< 20D2<>
TMDS_DN<4>          20A4< 20B1< 20D2<>
TMDS_DN<5>          20A4< 20B1< 20C2<>
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TPAD_TXD            31B2< 31C4<>
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TP_MMM_ICSP_PGD     24C3<>
TP_MMM_ICSP_PGM     24C3<>
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TV_COMP             22A6<> 40D6>
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TV_GND2             22A6<> 39B6> 40A7>
TV_Y                22A6<> 40D6>
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UIDE_ADDR<2>        13D7<> 25B4<
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UIDE_DATA<6..0>     38C5>
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UIDE_DATA<3>        13D7<> 25D4<
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UIDE_DATA<5>        13D7<> 25C4<
UIDE_DATA<6>        13D7<> 25C4<
UIDE_DATA<7>        13D7<> 25C4< 38C5>
UIDE_DATA<8>        13D7<> 25C4<
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UIDE_DATA<13>       13D7<> 25B4<
UIDE_DATA<14>       13D7<> 25C4<
UIDE_DATA<15>       13D7<> 25B4<
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UIDE_DIOW_L         13C7<> 25A4< 38C5>
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UIDE_DMARQ          13C7<> 38C5>
UIDE_INTRQ          13C7< 38C5>
UIDE_IOCHRDY        13C7< 25A4< 38C5>
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UIDE_RST_L          13C7<> 25A4< 38C5>
USB2_PCI_GNT_L      12C7<> 27B7<
USB2_PCI_INT_L      14B5<> 14C7< 27A8<
USB2_PCI_REQ_L      12A7< 12D7<> 27B7>
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USB_D1P             14D1< 27A4< 27A5>
USB_D2M             27A5>
USB_D2P             27A5>
USB_DAM             14B2<> 14D2< 27A5>
USB_DAP             14B2<> 14D2< 27A5>
USB_DBM             14B2<> 14D1<
USB_DBP             14B2<> 14D1<
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USB_DDM             14B2<> 14C2<
USB_DDP             14B2<> 14C2<
USB_DEM             14B2<> 14C2< 38B2>
USB_DEP             14B2<> 14C2< 38B2>
USB_DFM             14B2<> 14B2< 38B2>
USB_DFP             14B2<> 14B2< 38B2>
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USB_OC_CD_L         14B2< 14C7<
USB_OC_EF_L         14B2< 14D7<
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USB_PWREN_CD_L      14B2<> 14C7<
USB_PWREN_EF_L      14B2<> 14D7<
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USB_TPAD_P          14B1< 23A7<>
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VCORE_BST           35C5<> 39C1>
VCORE_CC            35B6<> 39B1>
VCORE_CNTL_RC       19A3<>
VCORE_DH            35B5<> 39C1>
VCORE_DL            35B5<> 39C1>
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VCORE_FAST<3>       35D3< 35D5<
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VCORE_FB            35B5< 39B1> 40A2>
VCORE_GND           35B5<> 39B1>
VCORE_GNDA          35B6<>
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VCORE_GNDDIV_TEST   35A3<>
VCORE_GNDSNS        35A2<> 35A4< 39B1>
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VCORE_ILIM          35C6<> 39C1>
VCORE_LX            35B5<> 39C1>
VCORE_MUX_EN        35D5<> 40A2>
VCORE_MUX_SEL       35D5<>
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VCORE_SEL_ON        35B6<>
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VCORE_SLOW<1>       35D6<
VCORE_SLOW<2>       35D6<
VCORE_SLOW<3>       35D6<
VCORE_SLOW<4>       35D6<
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VCORE_TIME          35B4<> 39B1>
VCORE_TON           35B6< 39C1>
VCORE_VCC           35C6< 39C1>
VCORE_VGATE         14B6< 14B7< 35B4> 39B1>
VCORE_VID0          40A3>
VCORE_VID1          40A3>
VCORE_VID2          40A3>
VCORE_VID3          40A3>
VCORE_VID4          40A3>
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VCORE_VID<1>        35A2<> 35B8< 35D4<>
VCORE_VID<2>        35A2<> 35B8< 35D4<>
VCORE_VID<3>        35A2<> 35B8< 35D4<>
VCORE_VID<4>        35A2<> 35B8< 35D4<>
VGA_B               22C6<> 22D7< 40D7>
VGA_G               22C5<> 22D7< 40D7>
VGA_HSYNC           22C6<> 22C7< 40D7>
VGA_HSYNC_BUF       22C8<>
VGA_R               22C5<> 22D7< 40D7>
VGA_VSYNC           22C5<> 22C7< 40D7>
VGA_VSYNC_BUF       22C8<>
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	?	?
SCALE NONE	SHT ?43	OF ?

*** Part Cross-Reference for the entire design ***

B61 PCB_STANDOFF 4
C1 CAP 22
C2 CAP 35
C3 CAP 35
C4 CAP 35
C5 CAP 35
C6 CAP 35
C7 CAP 35
C8 CAP 5
C9 CAP 16
C10 CAP 16
C11 CAP 18
C12 CAP 5
C13 CAP 35
C14 CAP 23
C15 CAP 14
C16 CAP 16
C17 CAP 16
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C19 CAP 16
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C72 CAP 5
C73 CAP 5
C74 CAP 5
C75 CAP 16
C76 CAP 16
C77 CAP 18
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XW27	SHORT	21
XW28	SHORT	21
XW29	SHORT	21
XW30	SHORT	21
XW31	SHORT	5
Y1	CRYSTAL	14
Y3	CRYSTAL	28
Y4	CRYSTAL	23
Y5	CRYSTAL	27
Y6	CRYSTAL	31
Y7	CRYSTAL_4PIN	31
ZT1	HOLE_VIA	4
ZT2	MTGHOLE	4
ZT3	HOLE_VIA	4
ZT4	MTGHOLE	4
ZT5	MTGHOLE	4
ZT6	MTGHOLE	4
ZT7	HOLE_VIA	4
ZT8	HOLE_VIA	4
ZT9	HOLE_VIA	4
ZT10	MTGHOLE	4
ZT11	MTGHOLE	4
ZT12	HOLE_VIA	4
ZT13	HOLE_VIA	4
ZT14	HOLE_VIA	4
ZT15	HOLE_VIA	4
ZT16	MTGHOLE	4
ZT17	HOLE_VIA	4
ZT18	HOLE_VIA	4
ZT19	HOLE_VIA	4
ZT20	HOLE_VIA	4
ZT21	HOLE_VIA	4
ZT22	HOLE_VIA	4
ZT23	HOLE_VIA	4
ZT24	HOLE_VIA	4
ZT25	HOLE_VIA	4
ZT26	HOLE_VIA	4
ZT27	HOLE_VIA	4
ZT28	HOLE_VIA	4
ZT29	HOLE_VIA	4
ZT30	HOLE_VIA	4
ZT31	HOLE_VIA	4
ZT32	HOLE_VIA	4
ZT33	HOLE_VIA	4
ZT34	HOLE_VIA	4
ZT35	HOLE_VIA	4
ZT36	HOLE_VIA	4
ZT37	HOLE_VIA	4
ZT38	HOLE_VIA	4
ZT39	HOLE_VIA	4
ZT40	HOLE_VIA	4
ZT41	HOLE_VIA	4
ZT42	HOLE_VIA	4
ZT43	HOLE_VIA	4
ZT44	HOLE_VIA	4
ZT45	HOLE_VIA	4
ZT46	HOLE_VIA	4
ZT47	HOLE_VIA	4
ZT48	HOLE_VIA	4
ZT49	HOLE_VIA	4
ZT50	HOLE_VIA	4
ZT51	HOLE_VIA	4
ZT52	HOLE_VIA	4
ZT53	HOLE_VIA	4
ZT54	HOLE_VIA	4
ZT55	HOLE_VIA	4
ZT56	HOLE_VIA	4
ZT57	HOLE_VIA	4
ZT58	HOLE_VIA	4
ZT59	HOLE_VIA	4
ZT60	HOLE_VIA	4
ZT61	HOLE_VIA	4
ZT62	HOLE_VIA	4
ZT63	HOLE_VIA	4
ZT64	HOLE_VIA	4
ZT65	HOLE_VIA	4
ZT66	HOLE_VIA	4
ZT67	HOLE_VIA	4
ZT68	HOLE_VIA	4
ZT69	HOLE_VIA	4
ZT70	HOLE_VIA	4
ZT71	HOLE_VIA	4
ZT72	HOLE_VIA	4
ZT73	HOLE_VIA	4
ZT74	HOLE_VIA	4
ZT75	HOLE_VIA	4
ZT76	HOLE_VIA	4
ZT77	HOLE_VIA	4
ZT78	HOLE_VIA	4
ZT79	HOLE_VIA	4
ZT80	HOLE_VIA	4
ZT81	HOLE_VIA	4
ZT82	HOLE_VIA	4
ZT83	MTGHOLE	4