

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.  
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.  
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

# SCHEM, TAUPO, M87

10/13/2007

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
?		?	?	?	?

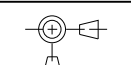
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10	10	CPU FSB	T9_NOME	03/16/2007
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12	12	CPU Decoupling & VID	M76_MLB	03/19/2007
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14	14	NB CPU Interface	T9_NOME	03/16/2007
15	15	NB PEG / Video Interfaces	T9_NOME	03/16/2007
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21	21	NB Standard Decoupling	T9_NOME	01/17/2007
22	22	NB Graphics Decoupling	M76_MLB	03/12/2007
23	23	SB Enet, Disk, FSB, LPC	T9_NOME	03/16/2007
24	24	SB PCI, PCIE, DMI, USB	T9_NOME	03/16/2007
25	25	SB Pwr Mgt, GPIO, Clink	T9_NOME	03/16/2007
26	26	SB Power & Ground	T9_NOME	03/16/2007
27	27	SB Decoupling	T9_NOME	01/17/2007
28	28	SB Misc	(T9_MLB)	08/24/2006
29	29	Clock (CK505)	T9_NOME	03/16/2007
30	30	Clock Termination	(MASTER)	08/23/2006
31	31	DDR2 SO-DIMM Connector A	(M59_SYNC)	08/24/2006
32	32	DDR2 SO-DIMM Connector B	(M59_SYNC)	08/24/2006
33	33	Memory Active Termination	(T9_NOME)	11/14/2006
34	34	Left I/O Board Connector	(M59_SYNC)	08/24/2006
35	35	Ethernet (Yukon)	T9_NOME	03/16/2007
36	36	Yukon Power Control	T9_NOME	03/16/2007
37	37	Ethernet Connector	M76_MLB	03/19/2007
38	38	FireWire Link (TSB83AA22)	M76_MLB	03/19/2007
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40	40	FireWire Port Power	M76_MLB	03/19/2007
41	41	FireWire Ports	M76_MLB	03/19/2007
42	42	PATA Connector	(MASTER)	(MASTER)
43	43	External USB Connector	M88	08/02/2007
44	44	Left Clutch Barrel Interconnect	M87	07/16/2007
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57	70	Power FETs	M76_MLB	03/19/2007
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59	73	5V / 3.3V Power Supply	M76_MLB	03/19/2007
60	74	1.25V / 1.05V Power Supply	M76_MLB	03/12/2007
61	75	1.8V DDR2 Supply	M76_MLB	03/19/2007
62	76	1.5V Power Supply	M76_MLB	03/12/2007
63	77	FW PHY Power Supplies	M76_MLB	03/19/2007
64	78	3.425V G3Hot Supply & Power Control	M88	08/02/2007
65	80	NV G84M PCI-E	(MASTER)	(MASTER)
66	81	NV G84M Core/FB Power	(MASTER)	(MASTER)
67	82	NV G84M Frame Buffer I/F	(MASTER)	(MASTER)
68	84	GDDR3 Frame Buffer A (Top)	(MASTER)	(MASTER)
69	85	GDDR3 Frame Buffer B (Top)	(MASTER)	(MASTER)
70	86	NV G84M GPIO/MIO/Misc	(MASTER)	(MASTER)
71	87	GPU Straps	M88	08/02/2007
72	88	NV G84M Video Interfaces	(MASTER)	(MASTER)
73	89	GPU (G84M) Core Supply	M88	08/02/2007
74	90	LVDS Display Connector	(MASTER)	(MASTER)
75	91	GDDR3 Frame Buffer A (Bot)	M88_MLB_VRAM_BOT	06/19/2007
76	92	GDDR3 Frame Buffer B (Bot)	M88_MLB_VRAM_BOT	06/19/2007
77	93	1.8V FB Power Supply	(MASTER)	(MASTER)
78	94	DVI Display Connector	(MASTER)	(MASTER)
79	96	Project Specific Connectors	(M59_SYNC)	08/24/2006
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83	103	SB Constraints (1 of 2)	T9_NOME	01/17/2007
84	104	SB Constraints (2 of 2)	T9_NOME	01/17/2007
85	105	Clock & SMC Constraints	T9_NOME	01/17/2007
86	106	FireWire Constraints	T9_NOME	01/17/2007
87	107	GPU (G84M) Constraints	(MASTER)	(MASTER)
88	108	Project Specific Constraints	(MASTER)	(MASTER)
89	109	PCB Rule Definitions	(MASTER)	(MASTER)

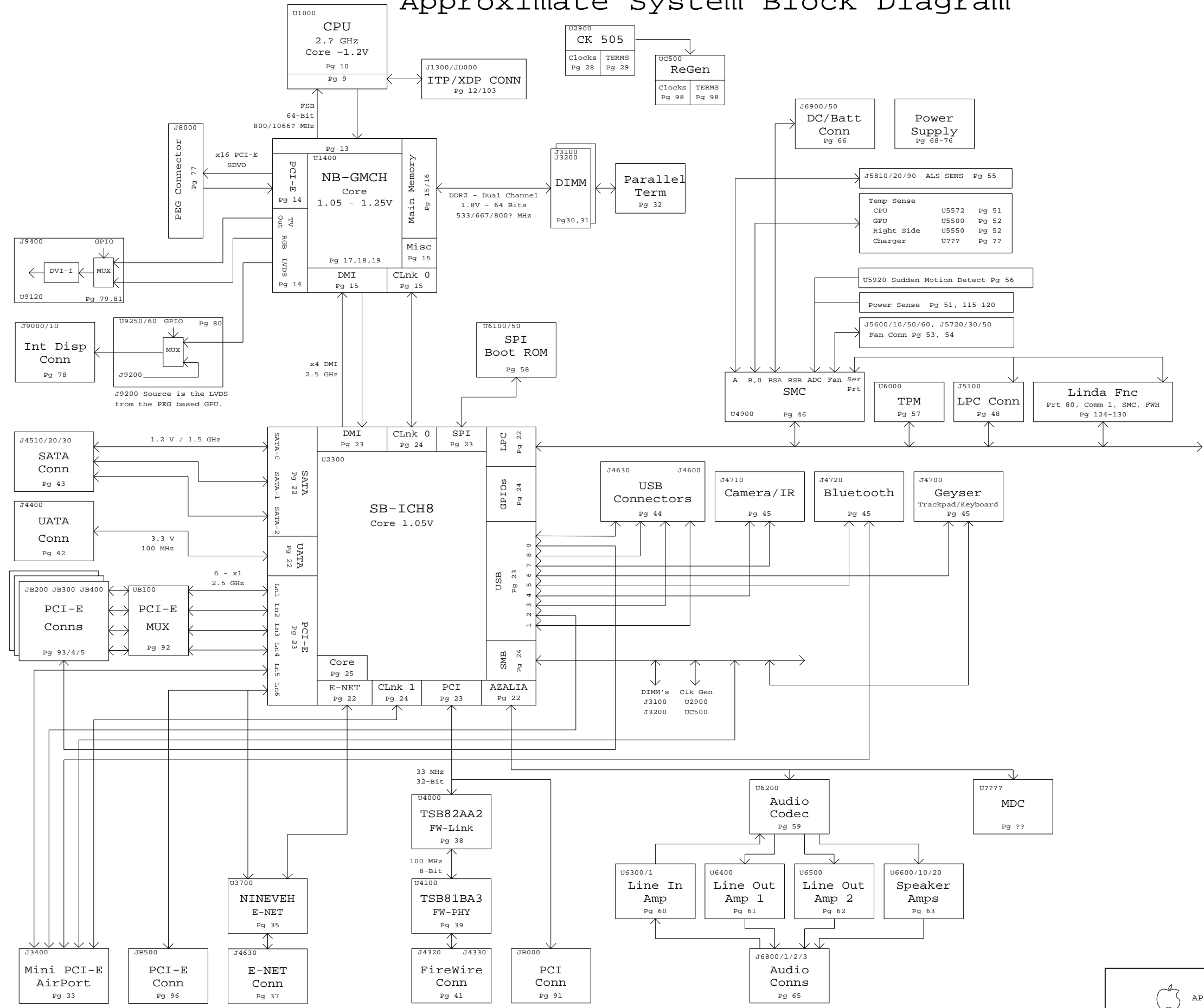
### Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7413	1	SCHEM,TAUPO,M87	SCH	CRITICAL	
820-2249	1	PCBF,TAUPO,M87	PCB	CRITICAL	

DRAWING  
 TITLE=MLB  
 ABBREV=DRAWING  
 LAST\_MODIFIED=Fri Oct 12 18:10:11 2007

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 THIRD ANGLE PROJECTION		DRAFTER ENG APPD QA APPD RELEASE	DESGN CK MFG APPD DESIGNER SCALE	TITLE <b>SCHEM, TAUPO, M87</b>	
		MATERIAL/FINISH NOTED AS APPLICABLE	SIZE D	DRAWING NUMBER	REV. 11.0.0
				051-7413	1 OF 89

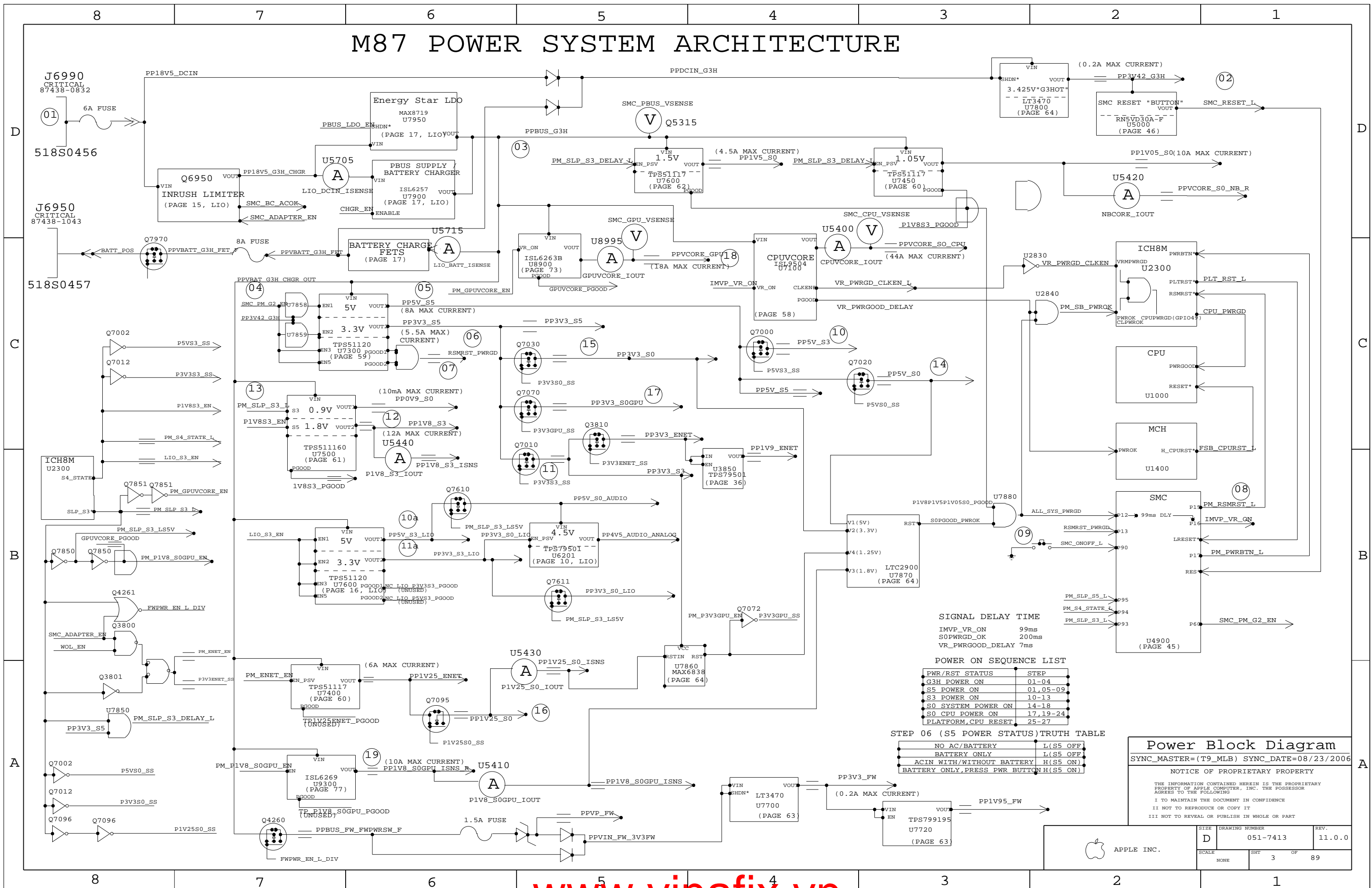
# Approximate System Block Diagram



**System Block Diagram**  
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NONE	2	89	

# M87 POWER SYSTEM ARCHITECTURE

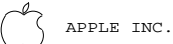


## Power Block Diagram

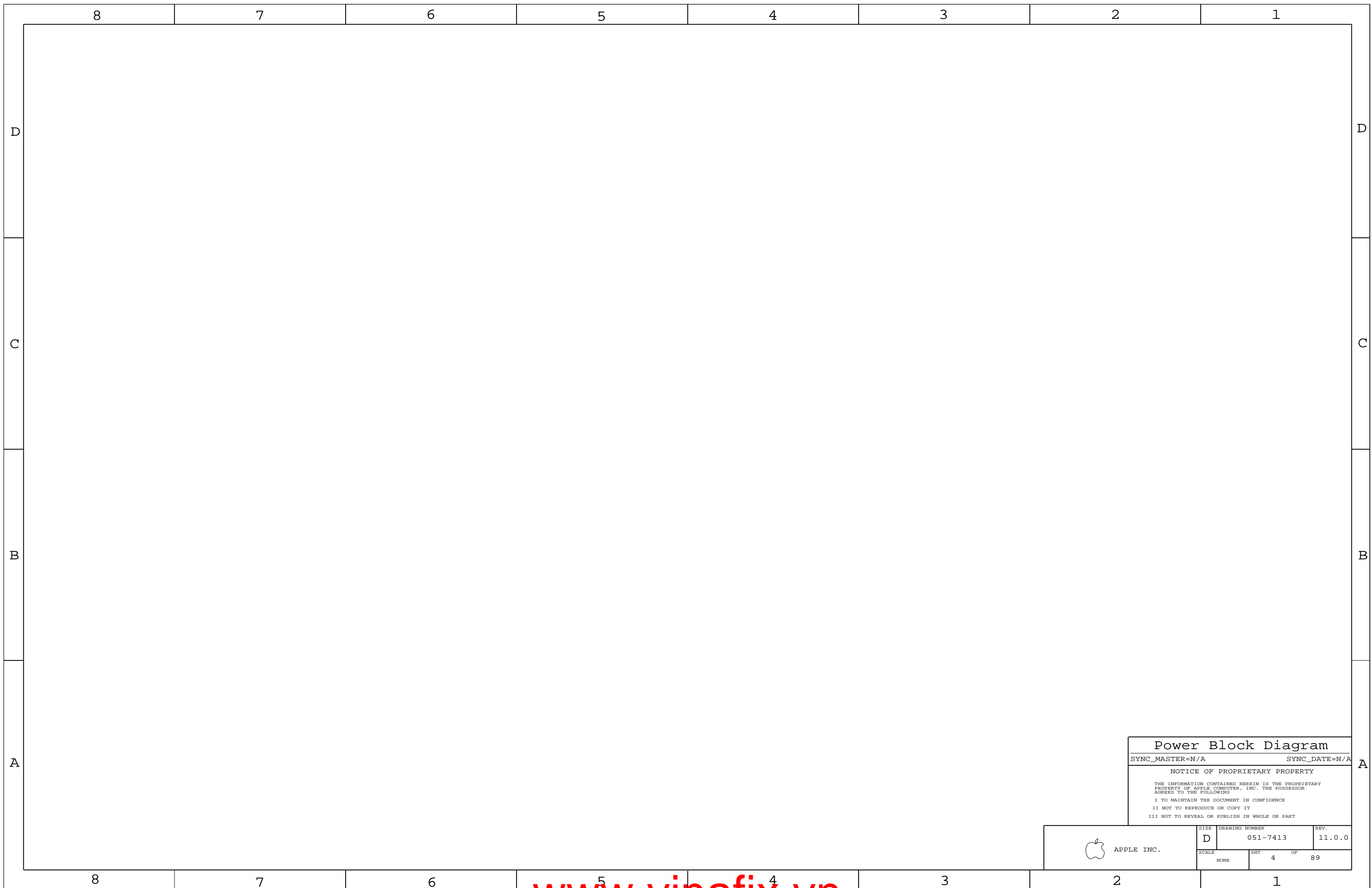
SYNC\_MASTER=(T9\_MLB) SYNC\_DATE=08/23/2006

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NONE	3	89



Power Block Diagram

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NONE		4	89

### BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9089	PCBA, 2.5GHZ, 512SAM_VRAM, M87	M87_COMMON, EEE_Z3G, CPU_2_5GHZ, FB_512_SAMSUNG
630-9091	PCBA, 2.6GHZ, 512SAM_VRAM, M87	M87_COMMON, EEE_Z3J, CPU_2_6GHZ, FB_512_SAMSUNG
630-9088	PCBA, 2.5GHZ, 512HY_VRAM, M87	M87_COMMON, EEE_Z3F, CPU_2_5GHZ, FB_512_HYNIX
630-9090	PCBA, 2.6GHZ, 512HY_VRAM, M87	M87_COMMON, EEE_Z3H, CPU_2_6GHZ, FB_512_HYNIX
630-9213	PCBA, 2.4GHZ, 256SAM_VRAM, M87	M87_COMMON, EEE_ZUP, CPU_2_4GHZ, FB_256_SAMSUNG
630-9238	PCBA, 2.4GHZ, 256HY_VRAM, M87	M87_COMMON, EEE_043, CPU_2_4GHZ, FB_256_HYNIX

### M75 BOM Groups

BOM GROUP	BOM OPTIONS
M87_COMMON	ALTERNATE, COMMON, M87_COMMON1, M87_COMMON2, M87_DEBUG, M87_PROGPARTS
M87_COMMON1	ISL9504B, ONEWIRE_PU
M87_COMMON2	GPUVID_1P13V, P1V8S3_1V8, SMS_MOT_DIS, YUKON_ULTRA, VGA_TERM_CONN, GPU_TMP401
M87_DEBUG	SMC_DEBUG_YES, XDP, XDP_CONN, LPCPLUS
M87_PROGPARTS	BOOTROM_PROG, SMC_PROG

BOM GROUP	BOM OPTIONS
FB_512_SAMSUNG	VRAM8, VRAM_16M, VRAM_SAMSUNG, VRAM_512_SAMSUNG
FB_512_HYNIX	VRAM8, VRAM_16M, VRAM_HYNIX, VRAM_512_HYNIX
FB_256_SAMSUNG	VRAM4, VRAM_16M, VRAM_SAMSUNG, VRAM_256_SAMSUNG
FB_256_HYNIX	VRAM4, VRAM_16M, VRAM_HYNIX, VRAM_256_HYNIX

### Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:Z3F]	CRITICAL	EEE_Z3F
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:Z3G]	CRITICAL	EEE_Z3G
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:Z3H]	CRITICAL	EEE_Z3H
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:Z3J]	CRITICAL	EEE_Z3J
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:ZUP]	CRITICAL	EEE_ZUP
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:043]	CRITICAL	EEE_043

### Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3540	1	IC, PDC, SR, QS, CO, 2.5G, 35W, 800FSB, 6M, BGA	U1000	CRITICAL	CPU_2_5GHZ
337S3541	1	IC, PDC, SR, QS, CO, 2.6G, 35W, 800FSB, 6M, BGA	U1000	CRITICAL	CPU_2_6GHZ
338S0509	1	IC, GPU, NV G84M, BGA, LOW LEAK	U8000	CRITICAL	
338S0432	1	IC, NB, CRESTLINE, GM, CO, PRQ, 965PM	U1400	CRITICAL	
338S0434	1	IC, SB, ICH8M, B1, PRQ, BGA	U2300	CRITICAL	
353S1651	1	IC, ISL9504B, 2PH IMVP6 REG, EMON, QFN48	U7100	CRITICAL	ISL9504B
359S0130	1	IC, SLG2AP101, LM PWR CLCK GEN, CK505, QFN68	U2900	CRITICAL	
338S0386	1	IC, 8888058, GIGABIT EMET XCVR, 64P QFN	U3700	CRITICAL	
338S0274	1	IC, SMC, HSB/2116	U4900	CRITICAL	SMC_BLANK
341S2193	1	IC, SMC, DEVELOPMENT, M75	U4900	CRITICAL	SMC_PROG
335S0384	1	IC, 16MBIT 8-PIN SPI SERIAL FLASH, SOIC8	U6100	CRITICAL	BOOTROM_BLANK
341S2192	1	IC, EFI ROM, DEVELOPMENT, M75	U6100	CRITICAL	BOOTROM_PROG
337S3556	1	IC, PDC, SR, QS, CO, 2.4G, 35W, 800FSB, 3M, BGA	U1000	CRITICAL	CPU_2_4GHZ

333S0423	8	IC, SGRAM, GDDR3, 16Mx32, 800MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_512_SAMSUNG
333S0424	8	IC, SGRAM, GDDR3, 16Mx32, 900MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_512_HYNIX
333S0423	4	IC, SGRAM, GDDR3, 16Mx32, 800MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_256_SAMSUNG
333S0424	4	IC, SGRAM, GDDR3, 16Mx32, 900MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_256_HYNIX

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
157S0011	157S0030		ALL	See alt to 157S0030
152S0476	152S0276		ALL	Inductor alternate
353S1681	353S1294		ALL	TI alt to National
138S0603	138S0602		ALL	Muratec alt to Samsung
353S1681	353S1294		ALL	LM5011, ORAMP, GME
152S0684	152S0368		ALL	Meplayers alt to Dale/Vishay
152S0683	152S0276		ALL	Meplayers alt to Dale/Vishay
104S0023	104S0018		ALL	Cytec alt to sense resistor
104S0024	104S0017		ALL	Panasonic alt to PE resistor

BOM Configuration		
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SCALE	SHT		OF
NONE	5		89

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PROTO

0.1.0:  
04/26/07 -- Design branched from 051-7225-A  
04/26/07 -- Clock Termination: Removed support for SLG8LP537 device (GPU\_CLK\_27M/27MSS muxes, etc)  
04/26/07 -- Clock Termination: Added S0-powered AND gate between GPU\_PGOOD and SLG2AP101 enable pin to eliminate leakage path (rdar://5086613)  
04/26/07 -- SB Misc: Removed EXTGPU\_RST\_L support for resetting the GPU (hardware control only)  
04/26/07 -- Power Control: Removed U7858 and R7860. Tied SMC\_PM\_G2\_EN/PM\_G2\_EN directly to S5 regulators  
04/26/07 -- SB Decoupling: Replaced L2700 with 155S0333 for AVL updates  
04/26/07 -- FW Port Power: Replaced D4260 with proper symbol (instead of table)  
04/30/07 -- FW Port Power: Updated U4210 to 353S1744 for AVL updates  
05/01/07 -- Current Sensors: Changed R5425/35/45 to RES\_SENSE symbol which implements kelvin sensing without the need for XW shorts  
0.1.2:  
05/08/07 -- SB Decoupling: Changed C2703 to 138S0578 per Intel recommendations (rdar://5185100)  
05/08/07 -- GPU Straps: Stuffed R8728 to put GPU PEG I/F into mobile mode (rdar://5188253)  
0.2.0:  
05/10/07 -- Thermal Sensors: Added SIGNAL\_MODEL=EMPTY properties to thermal sense diff pairs (rdar://5192397)  
05/10/07 -- Current Sensors: Added SIGNAL\_MODEL=EMPTY properties to current sense diff pairs (rdar://5192397)  
0.3.0:  
05/14/07 -- Power Control: Added U7858,U7859 to properly enable/disable S5 regulators (rdar://TBD)  
05/14/07 -- 5V/3.3V Regulators: Added C7307,C7308 to allow soft-start control of S5 regulators (rdar://TBD)  
0.4.0:  
05/22/07 -- Power Control: Added C7858 to decouple U7858/59  
05/22/07 -- GPU Vcore: Removed Power Control circuitry  
05/22/07 -- GPU Straps: Added R8734 to get PCIDEVID3 pullup  
0.5.0:  
06/06/07 -- GPU FB: Reassigned CS1/BA2 for future memory expansion  
06/06/07 -- GPU FB: Changed 22uF, 0805 caps to 10uF, 0603 for future memory expansion  
06/06/07 -- GPU FB: Reworked/added FB device Vrefs (with smaller FETs) for future memory expansion  
06/06/07 -- Left clutch I/C: Removed SIM I/F connector  
0.6.0:  
06/07/07 -- GPU Straps: U8700 changed to TS3V340 only  
06/18/07 -- GPU FB: Added support for 1Gb density ICs (added MA<12> and CS1)  
06/18/07 -- Left Clutch I/C: Added alternate camera connections (CCP2 I/F)  
06/18/07 -- DFM: Added NC nets to allow copper on BGA corner balls (CPU and GPU)  
06/19/07 -- GPU FB: Added 4 more 16Mx32 VRAM devices  
06/20/07 -- Muxed Gfx: Began removing support for this feature  
0.7.0:  
06/25/07 -- GPU VCORE: U8900 Changed to IMVP6  
06/25/07 -- FB REGULATOR: Added U9300  
06/25/07 -- Muxed Gfx: Removed LVDS/BKLT muxes and support  
06/25/07 -- Power Fet: Removed 1V8 and 1V25 Fets  
06/25/07 -- Current Sense: Removed U5410 NBGfx Sense  
06/25/07 -- Regulators: Changed Q7320,Q7360,Q7410,Q7460 to SI7110N  
0.8.0:  
06/27/07 -- Power Fet: Removed 1v8 S0 Fet, cleaned up aliasing  
0.9.0:  
06/27/07 -- Current Sense: Added 1v8 FB current sense  
06/27/07 -- GPU VCORE: Added additional High side Input Cap  
0.10.0:  
06/27/07 -- MUX Gfx: Delete GPU PGOOD Monitor  
0.11.0:  
06/27/07 -- Aliasing:Cleanup  
06/27/07 -- BOM: Changed BOM option table for M87  
0.12.0:  
07/02/07 -- Power CTL:Added 1.25 PGOOD/3V3 GPU EN,Moved 1V8\_S3 to pgood chain  
07/02/07 -- LCC: Added Camera/MIC pins  
07/02/07 -- DVI: Removed SB Hotplug Detect support(muxed gfx)  
0.13.0:  
07/05/07 -- Aliasing: Moved pages back in sync with T9, aliasing now on separate page  
07/05/07 -- Regulators: Changed L7100,L7101 to 4mm 152S0433  
1.2.0:  
08/02/07 -- USB: Change to active enable USB ports  
08/02/07 -- Regulators: Changed U8900 to use VID instead of Feedback resistors  
EVT  
4.1.0:  
08/09/07 -- Current Sense: Change Q5322 TO FDN337 to accommodate TH1H  
08/09/07 -- Ethernet: Change T3900,T3901 to 157S0053  
5.1.0:  
08/13/07 -- Regulators: Change GPUVCORE VID pullup/pulldowns to 2.2K  
DVT  
10.0.0:  
09/21/07 -- BOM OPTION: Add 2.4Ghz 256MB VRAM Config, change 2.5Ghz Conifgs to 512MB VRAM

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Revision History		
SYNC_MASTER=N/A	SYNC_DATE=N/A	
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	SCALE NONE	SHEET 6	OF 89



## Functional Test Points

## ICT Test Points

### Fan Connectors

FUNC_TEST	Pin
TRUE =PP3V3 S0 FAN LT	8 52
TRUE FAN LT PWM	52
TRUE FAN LT TACH	52
TRUE FAN RT PWM	52
TRUE FAN RT TACH	52

### Battery Digital Connector

FUNC_TEST	Pin
TRUE SMC BS ALRT L	45 46 56
TRUE =SMBUS BATT_SCL	48 56
TRUE =SMBUS BATT_SDA	48 56
TRUE GND BATT	56

### CPU FSB NO\_TESTS

NO_TEST	Pin
TRUE FSB A L<31..3>	10 14 80
TRUE FSB ADS L	10 14 80
TRUE FSB ADSTB L<1..0>	10 14 80
TRUE FSB BNR L	10 14 80
TRUE FSB BREQ L	10 14 80
TRUE FSB D L<63..0>	10 14 80
TRUE FSB DBSY L	10 14 80
TRUE FSB DINV L<3..0>	10 14 80
TRUE FSB DRDY L	10 14 80
TRUE FSB DSTB L N<3..0>	10 14 80
TRUE FSB DSTB L P<3..0>	10 14 80
TRUE FSB HIT L	10 14 80
TRUE FSB HITM L	10 14 80
TRUE FSB LOCK L	10 14 80
TRUE FSB REQ L<4..0>	10 14 80

### NB NO\_TESTS

NO_TEST	Pin
TRUE NC NB NC<1..16>	== TP NB NC<1..16> 16

### LPC+ Debug Connector

FUNC_TEST	Pin
TRUE =PP3V3 S5 LPCPLUS	8 47
TRUE =PP5V S0 LPCPLUS	8 47
TRUE LPC AD<0>	23 45 47
TRUE LPC AD<1>	23 45 47
TRUE LPC FRAME L	23 45 47
TRUE PM_CLKRUN L	25 45 47
TRUE BOOT_LPC_SPI L	24 47
TRUE SMC TMS	45 46 47
TRUE DEBUG_RESET L	28 47
TRUE SMC TRST L	45 47
TRUE SMC TDO	45 46 47
TRUE SMC MD1	45 47
TRUE SMC TX L	43 45 46 47
TRUE FW_H_INIT L	47
TRUE PCI_CLK33M LPCPLUS	30 47 85
TRUE LPC AD<2>	23 45 47
TRUE LPC AD<3>	23 45 47
TRUE INT_SERRIO	25 45 47
TRUE PM_SUS_STAT L	25 45 46 47
TRUE SMC TDI	45 46 47
TRUE SMC TCK	45 46 47
TRUE SMC RESET L	45 46 47
TRUE SMC NMI	45 47
TRUE SMC_RX L	43 45 46 47
TRUE LINDACARD_GPIO	25 47

### Left I/O Power Connector

FUNC_TEST	Pin
TRUE =PPBUS G3H LIO_CONN	8 56
TRUE GND	

Request for at least 10 GND test points  
NOTE: 10 additional GND test points are called out separately in these notes.

### RTC Battery Connector

FUNC_TEST	Pin
TRUE PPVBATT_G3_RTC	28
TRUE GND	

### Current Sense Calibration

FUNC_TEST	Pin
TRUE ISENSE_CAL_EN	45 49
TRUE =PP5V_S0_ISENSECAL	8 49
TRUE =PPVCORE_S0_CPU_REG	8 49 58
TRUE =PPVCORE_GPU_REG	8 49 73
TRUE GND	

2 TPs per

6 TPs, 2 with each of above TP pairs

### Left Clutch Barrel Connector

FUNC_TEST	Pin
TRUE =PP5V_S3_CAMERA	8 44
TRUE USB_CAMERA_N	24 44 83
TRUE USB_CAMERA_P	24 44 83
TRUE =PP5V_S3_WWAN	8

### Left ALS Connector

FUNC_TEST	Pin
TRUE =PP3V3_S3_LTALS	8 79
TRUE ALS_GAIN	45 53 79
TRUE LTALS_OUT	53 79
TRUE GND	

### Other Func Test Points

FUNC_TEST	Pin
TRUE PM_SYSRST_L	25 28 45
TRUE SMC_ONOFF_L	45 46 79

### Thermal Diode Connectors

FUNC_TEST	Pin
TRUE HSTHMSNS_D_P	51 88
TRUE HSTHMSNS_D_N	51 88
TRUE RSFTHMSNS_D_P	51 88
TRUE RSFTHMSNS_D_N	51 88
TRUE CPUTHMSNS_D2_P	51 88
TRUE CPUTHMSNS_D2_N	51 88

CPUTHMSNS can not be supported due to layout constraints

## System Validation TPs

FUNC_TEST	Pin
TRUE CPU_PWRGD	10 13 23 80
TRUE CPU_DPSLP_L	7 10 23 80
TRUE PM_DPRS_LPVR	16 25 58 80
TRUE CPU_DPSLP_L	7 10 23 80
TRUE PM_LAN_ENABLE	25 45
TRUE PCI_RST_L	24 28
TRUE PM_RSMRST_L	25 45
TRUE PM_SB_PWROK	9 25 28
TRUE SB_RTC_RST_L	23 28
TRUE PM_STPCPU_L	25 29 30
TRUE PM_STPPCI_L	25 29 30
TRUE VR_PWRGD_CLKEN	25 28
TRUE VR_PWRGD_DELAY	9 16 28 58
TRUE FSB_CPURST_L	10 13 14 80
TRUE FSB_CPUSLP_L	10 14 80
TRUE FSB_DPWR_L	10 14 80
TRUE NB_SB_SYNC_L	16 25

FUNC_TEST	Pin
TRUE IMVP_VR_ON	45 58
TRUE IMVP_DPRS_LPVR	58 80
TRUE PM_SLP_S3_L	25 36 40 45 64
TRUE PM_S4_STATE_L	25 45 64
TRUE PM_SLP_S5_L	25 45 66
TRUE PM_ENET_EN	36 64
TRUE P1V8P1V5P1V05S0_PGOOD	64
TRUE CPU_DPRSTP_L	10 16 23 58 80
TRUE IMVP6_VID<6..0>	12 58 80
TRUE PLT_RST_L	24 28
TRUE NB_RESET_L	16 28
TRUE GPU_RESET_L	28 65
TRUE SMC_LRESET_L	28 45
TRUE CPU_STPCLK_L	10 23 80
TRUE FSB_CLK_NB_P	14 30 85
TRUE FSB_CLK_NB_N	14 30 85
TRUE NB_CLKREQ_L	16 29
TRUE NB_CLK100M_PCIE_P	16 30 85
TRUE NB_CLK100M_PCIE_N	16 30 85

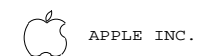
FUNC_TEST	Pin
TRUE CPU_THERMTRIP_R	33

## Functional / ICT Test

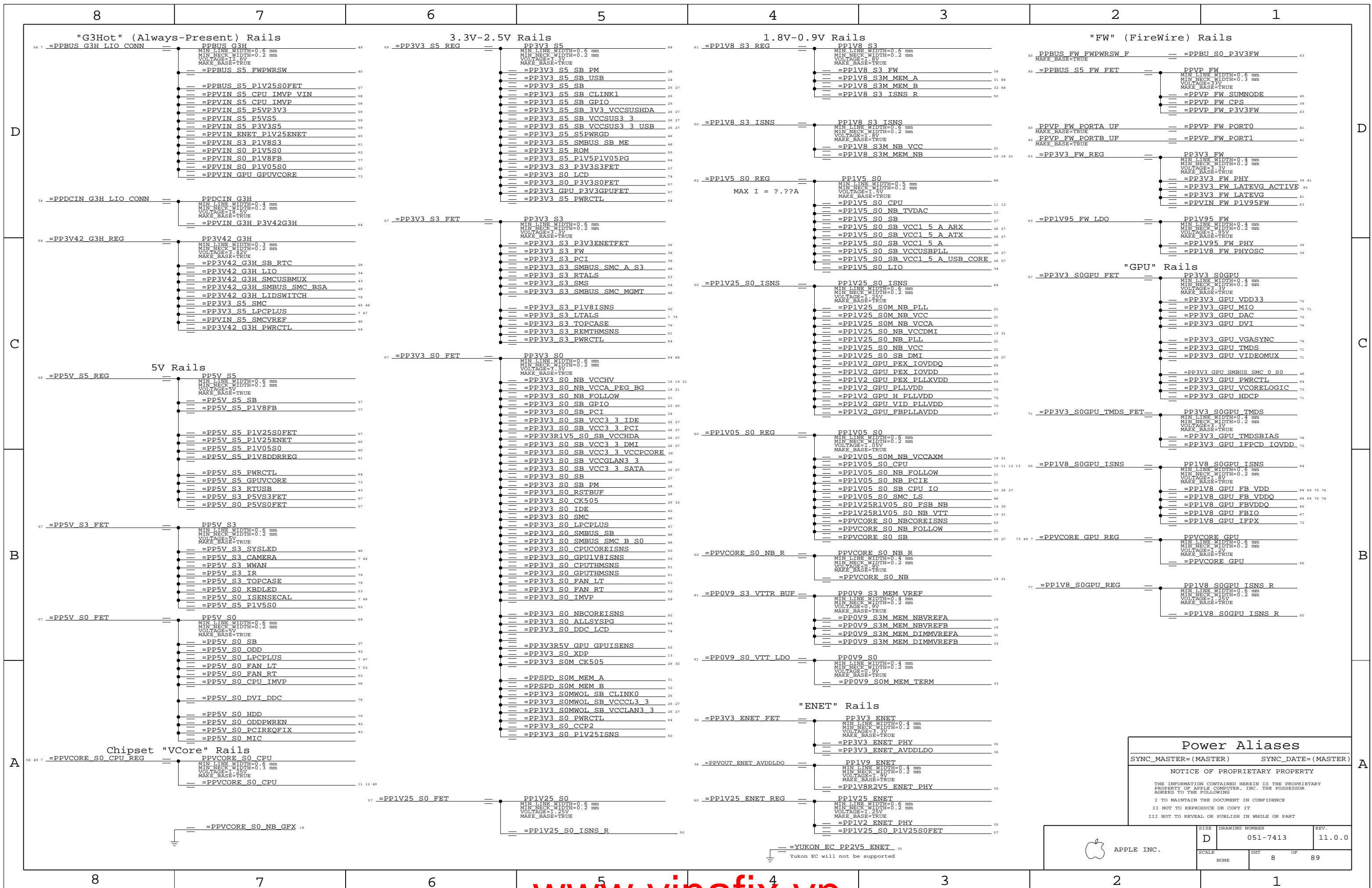
SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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SCALE	SHT	OF
NONE	7	89



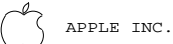
**Power Aliases**

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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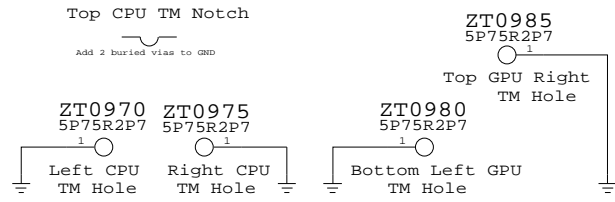
SCALE	SIZE	DRAWING NUMBER	REV.
	NONE	D	051-7413
SHEET		OF	
8		89	



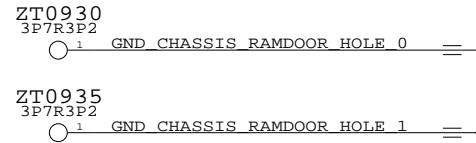
=YUKON\_EC\_PP2V5\_ENET 35  
 Yukon EC will not be supported



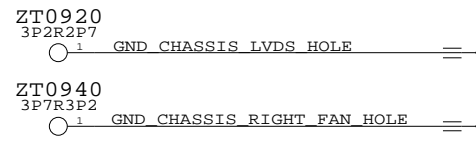
### Thermal Module Holes



### RAM Door (Torx) Holes

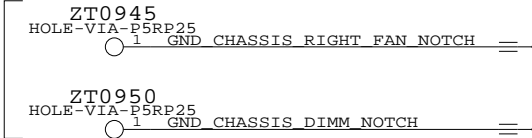


### Frame Holes



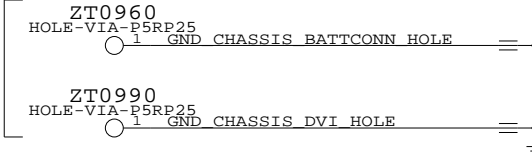
### Board Edge Notches

(Can't be PTH)



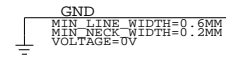
### Tooling Holes

(Can't be PTH)



23	EXTGPU PWR EN	==	TP_EXTGPU_PWR_EN	24	83
	MAKE_BASE=TRUE		MAKE_BASE=TRUE		
	TP_USB_EXTPDP	==	USB_EXTPDP	24	83
	MAKE_BASE=TRUE		MAKE_BASE=TRUE		
	TP_USB_EXTDN	==	USB_EXTDN	24	83
	MAKE_BASE=TRUE		MAKE_BASE=TRUE		
28	25	7	PM_SB_PWROK	==	SB_CLINK_MPWROK
	MAKE_BASE=TRUE		MAKE_BASE=TRUE		
58	28	16	VR_PWRGOOD_DELAY	==	NB_CLINK_MPWROK
	MAKE_BASE=TRUE		MAKE_BASE=TRUE		
54	SMC_SMS_INT	==	SMC_SMS_INT	45	
	MAKE_BASE=TRUE		MAKE_BASE=TRUE		
65	10	PEG_CLK100M_GPU_P	==	PEG_CLK100M_P	85
	MAKE_BASE=TRUE		MAKE_BASE=TRUE		
65	10	PEG_CLK100M_GPU_N	==	PEG_CLK100M_N	85
	MAKE_BASE=TRUE		MAKE_BASE=TRUE		
	TP_MEM_A_A<15>	==	MEM_A_A<15>	31	
	MAKE_BASE=TRUE		MAKE_BASE=TRUE		
	TP_MEM_B_A<15>	==	MEM_B_A<15>	32	
	MAKE_BASE=TRUE		MAKE_BASE=TRUE		
	TP_USB_EXTCP	==	USB_EXTCP	24	83
	MAKE_BASE=TRUE		MAKE_BASE=TRUE		
	TP_USB_EXTCN	==	USB_EXTCN	24	83
	MAKE_BASE=TRUE		MAKE_BASE=TRUE		
84	24	INT_PIROE_L	==	IPHS_SW_INT	34
	MAKE_BASE=TRUE		MAKE_BASE=TRUE		
25	SB_SLOAD	==	IPHS_SW_BIAS_EN_L	34	
	MAKE_BASE=TRUE		MAKE_BASE=TRUE		

### Digital Ground

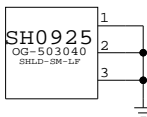


### Signal Aliases

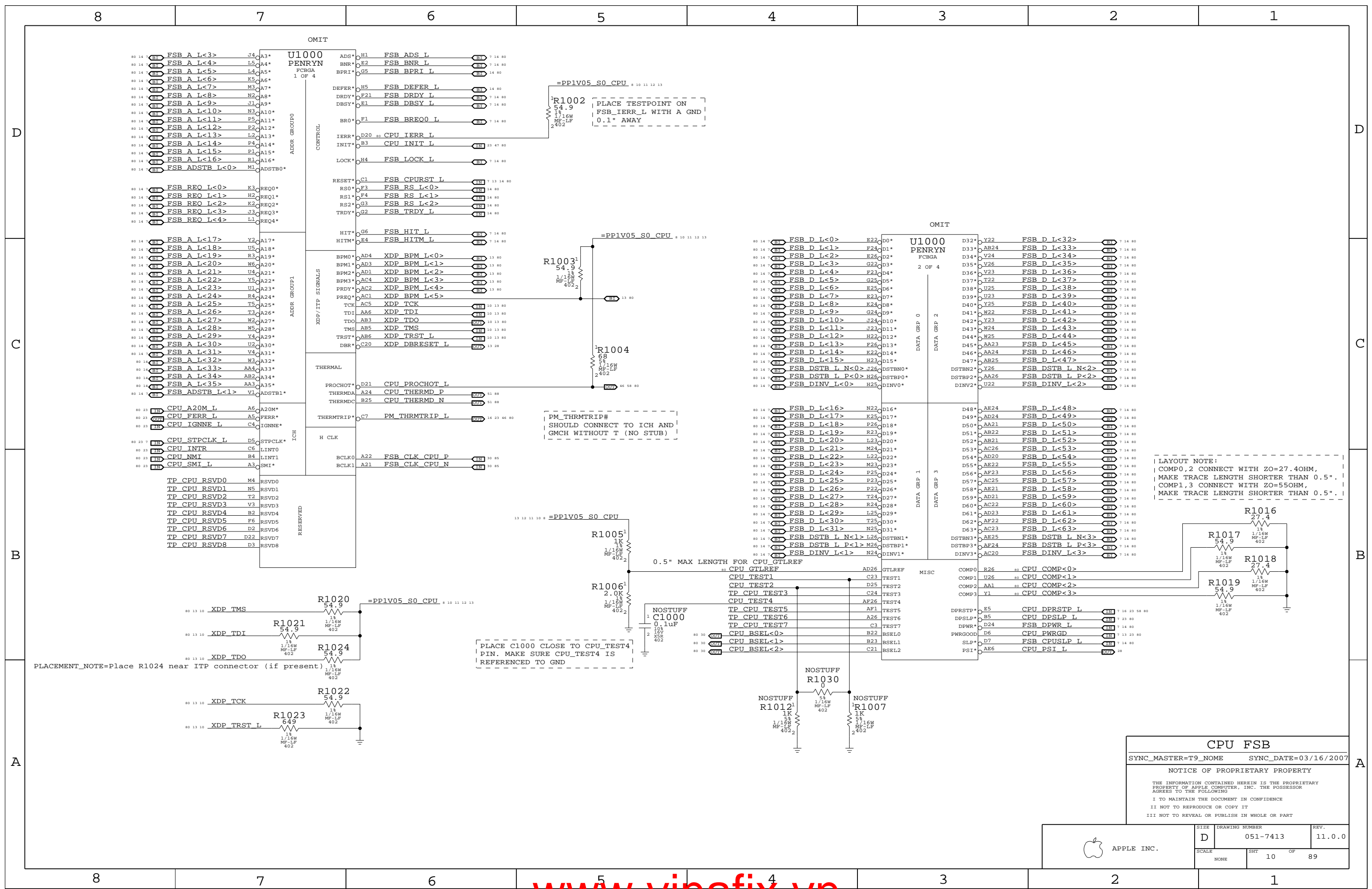
SYNC\_MASTER=(T9\_MLB) SYNC\_DATE=08/23/2006

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SCALE	SHT	OF	
NONE	9	89	



LAYOUT NOTE:  
 COMPO,2 CONNECT WITH ZO=27.4OHM,  
 MAKE TRACE LENGTH SHORTER THAN 0.5".  
 COMPL,3 CONNECT WITH ZO=55OHM,  
 MAKE TRACE LENGTH SHORTER THAN 0.5".

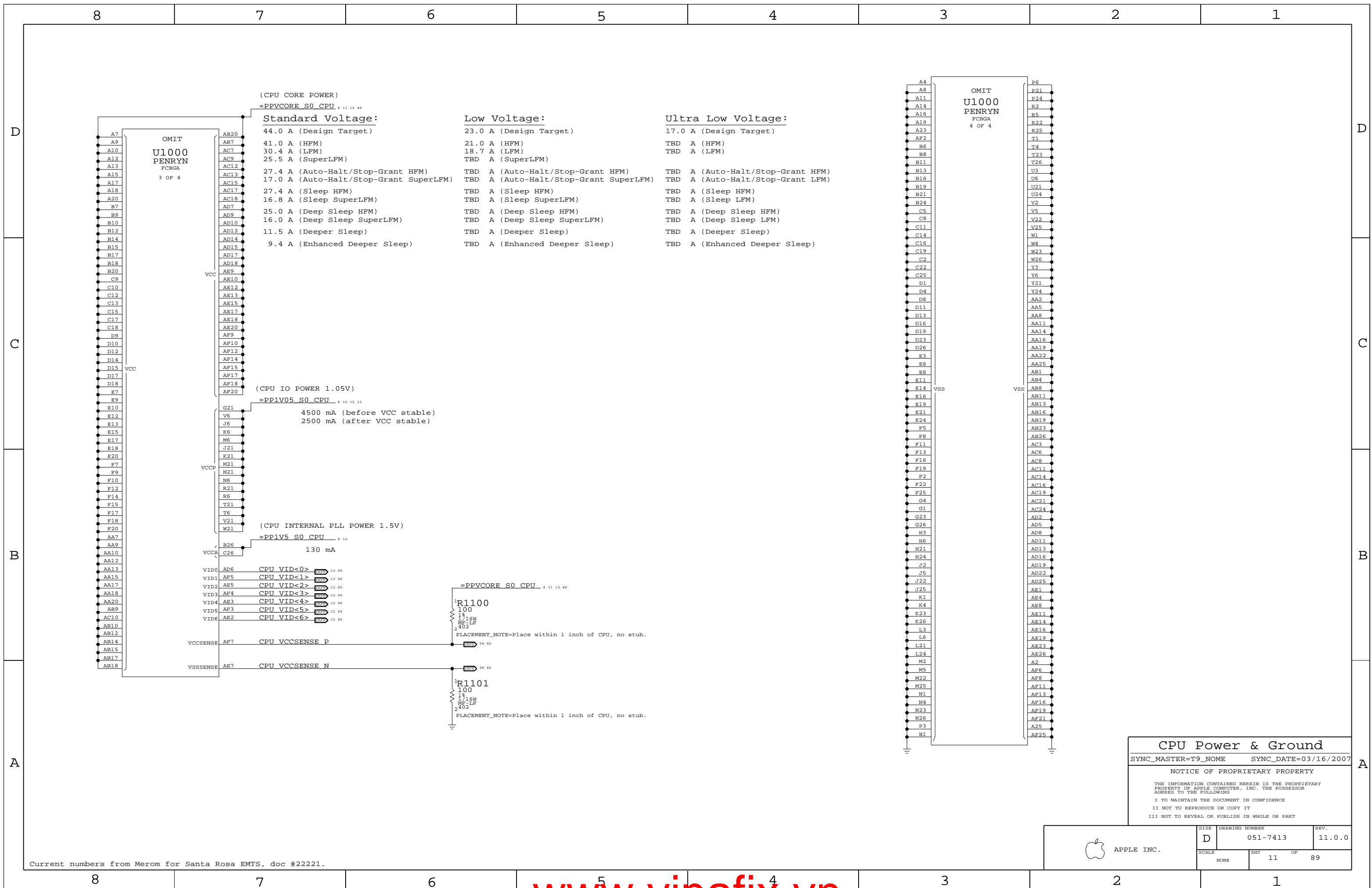
PLACE C1000 CLOSE TO CPU\_TEST4  
 PIN. MAKE SURE CPU\_TEST4 IS  
 REFERENCED TO GND

PM\_THRMTRIP#  
 SHOULD CONNECT TO ICH AND  
 GMCH WITHOUT T (NO STUB)

PLACEMENT\_NOTE=Place R1024 near ITP connector (if present)

**CPU FSB**  
 SYNC\_MASTER=T9\_NOME SYNC\_DATE=03/16/2007  
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NONE	10	89	



**CPU Power & Ground**

SYNC\_MASTER=T9\_NOME      SYNC\_DATE=03/16/2007

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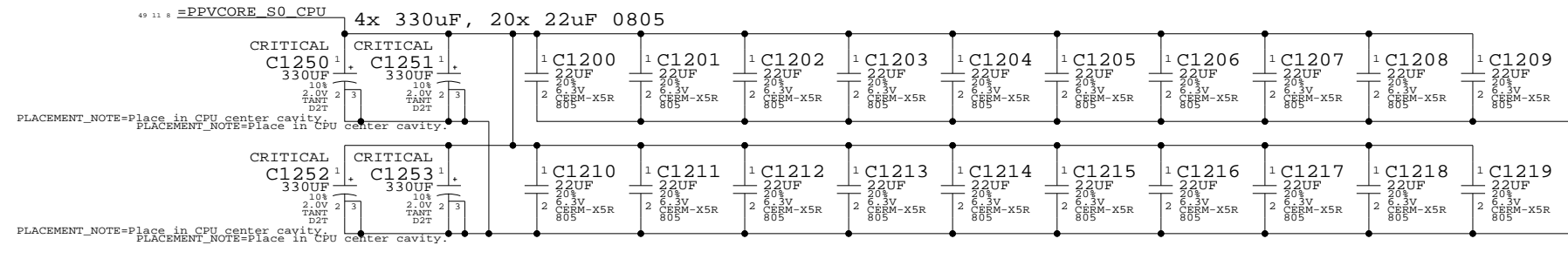
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	D	051-7413	11.0.0
SCALE	SHT	OF	
NONE	11	89	

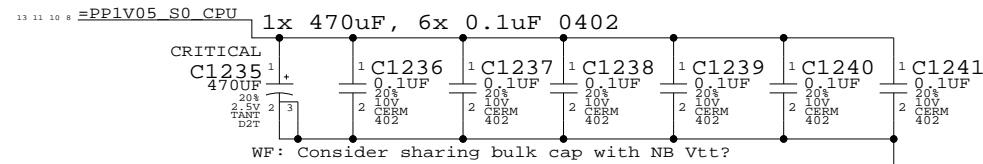
### CPU VCORE HF AND BULK DECOUPLING



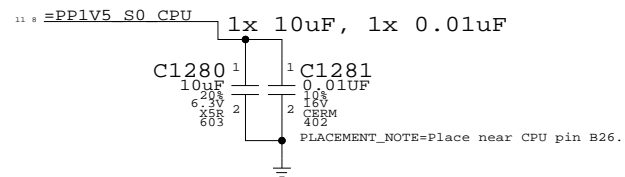
### CPU VCORE VID CONNECTIONS

80 11 CPU\_VID<0..6> = IMVP6\_VID<0..6> 7 88 80  
MAKE\_BASE=TRUE

### VCCP (CPU I/O) DECOUPLING



### VCCA (CPU AVdd) DECOUPLING

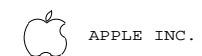


### CPU Decoupling & VID

SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/19/2007

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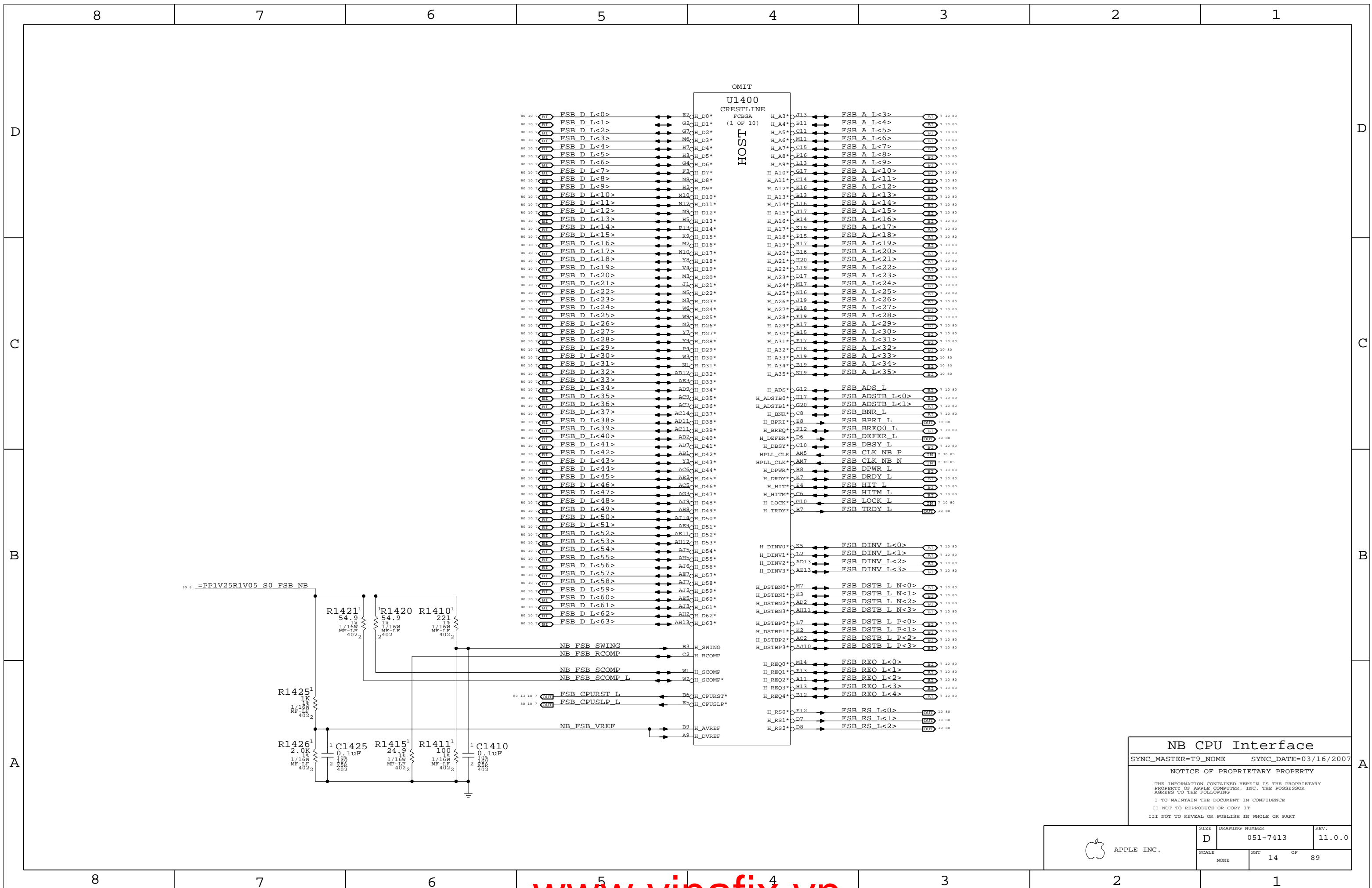
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NONE	12	89







**NB CPU Interface**  
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	SCALE NONE	SHEET 14	OF 89

**LVDS Disable**

Can leave all signals NC if LVDS is not implemented.  
Tie VCC\_TX\_LVDS and VCCA\_LVDS to GND.

If SDVO is used, VCCD\_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD\_LVDS to GND also.

Note: SR DG says to tie LVDS\_VREFH/L to GND. This causes a glitch during wake-up on LVDS DATA/CLK pairs. New recommendation is to float both signals, see Radar #5067636.

**TV-Out Signal Usage:**

Composite: DACA only  
S-Video: DACB & DACC only  
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

**TV-Out Disable / CRT Enable**

Tie TVx\_DAC and TVx\_RTN to GND. Must power all TVDAC rails. VCCA\_TVx\_DAC and VCCA\_DAC\_BG can share filtering with VCCA\_CRT\_DAC.

**CRT Disable / TV-Out Enable**

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND. All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA\_CRT.

**CRT & TV-Out Disable**

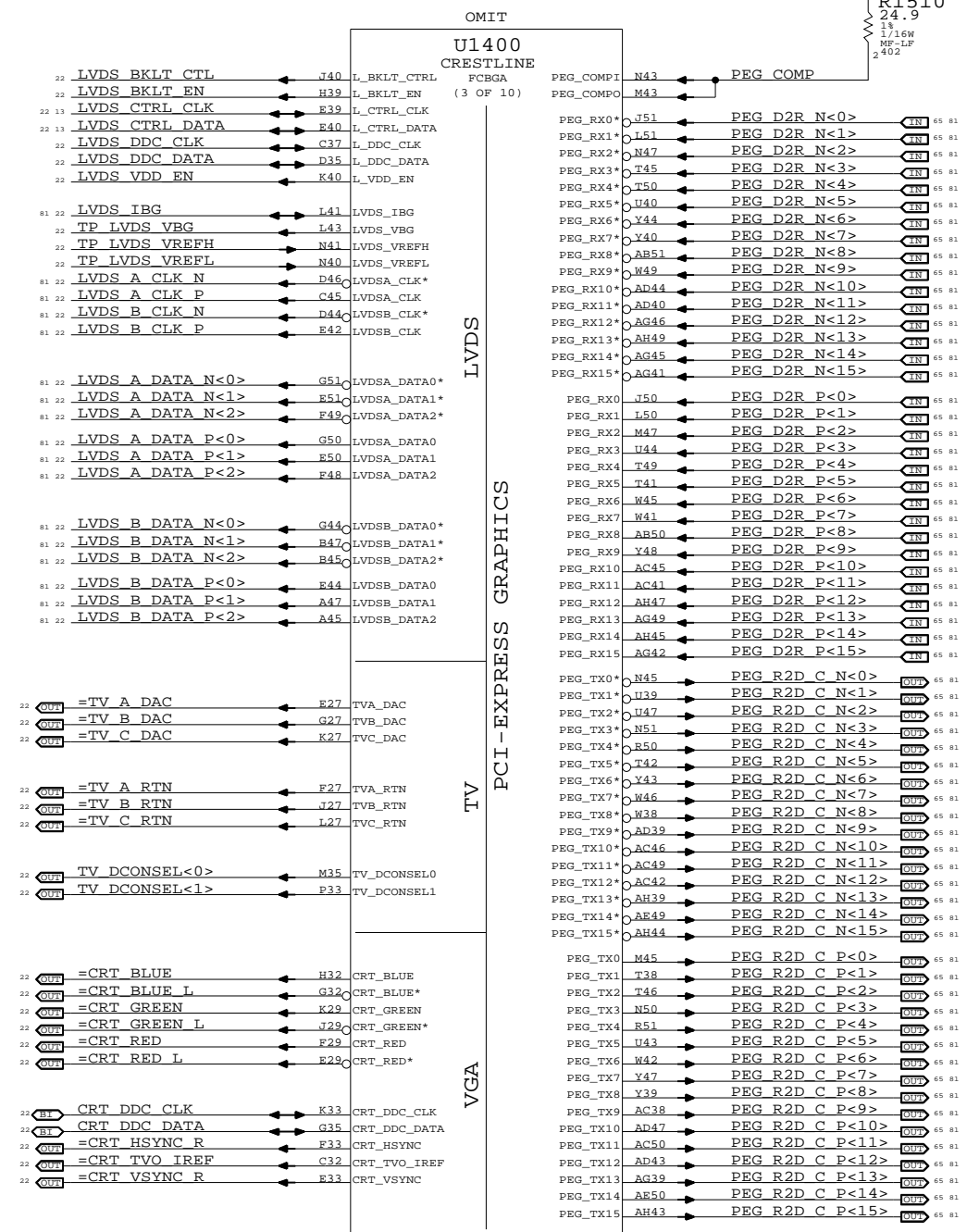
Tie TVx\_DAC, TVx\_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT\_TVO\_IREF to GND.  
Can tie the following rails to GND:  
VCCA\_CRT\_DAC, VCCA\_DAC\_BG, VCCA\_TVx\_DAC, VCCD\_CRT, VCCD\_QDAC and VCC\_SYNC.

NOTE: Must keep VDDC\_TVDAC powered and filtered at all times!

**Internal Graphics Disable**

Follow instructions for LVDS and CRT & TV-Out Disable above. Can also tie CRT\_DDC\_\*, L\_CTRL\_\*, L\_DDC\_\*, SDVO\_CTRL\_\* and TV\_DCONSELx to GND.

Tie DPLL\_REF\_CLK and DPLL\_REF\_SSCLK to GND.  
Tie DPLL\_REF\_CLK\* and DPLL\_REF\_SSCLK\* to VCC (VCore).  
Tie VCCA\_DPLLA and VCCA\_DPLLB to VCC (VCore).  
Tie VCC\_AXG and VCC\_AXG\_NCTF to GND.  
Leave GFX\_VID<3..0> and GFX\_VR\_EN as NC.



**SDVO Alternate Function**

SDVO\_TVCLKIN#  
SDVO\_INT#  
SDVO\_FLDSTALL#

SDVO\_TVCLKIN  
SDVO\_INT  
SDVO\_FLDSTALL

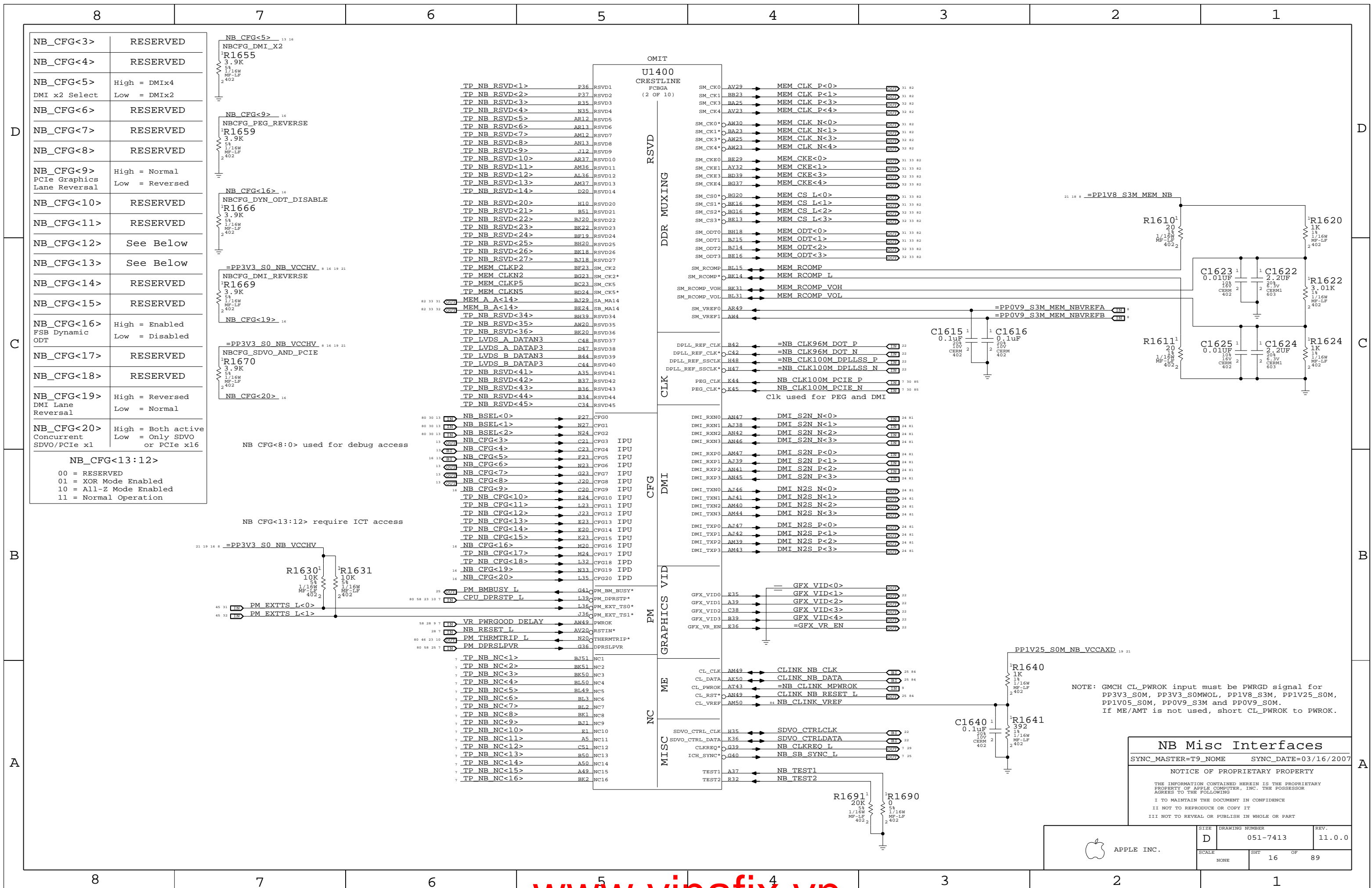
SDVOB\_RED#  
SDVOB\_GREEN#  
SDVOB\_BLUE#  
SDVOB\_CLKN  
SDVOC\_RED#  
SDVOC\_GREEN#  
SDVOC\_BLUE#  
SDVOC\_CLKN

SDVOB\_RED  
SDVOB\_GREEN  
SDVOB\_BLUE  
SDVOB\_CLKP  
SDVOC\_RED  
SDVOC\_GREEN  
SDVOC\_BLUE  
SDVOC\_CLKP

**NB PEG / Video Interfaces**  
SYNC\_MASTER=T9\_NOME SYNC\_DATE=03/16/2007

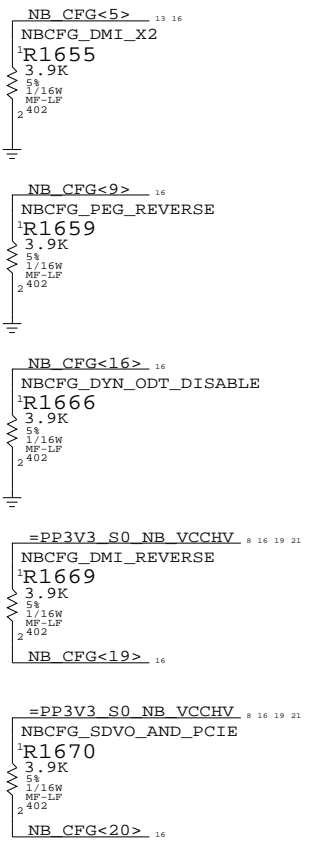
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NONE	15	89	



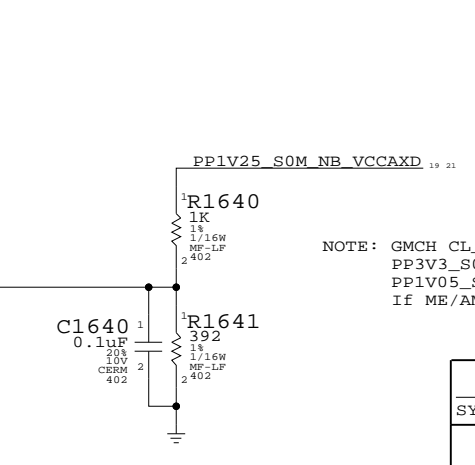
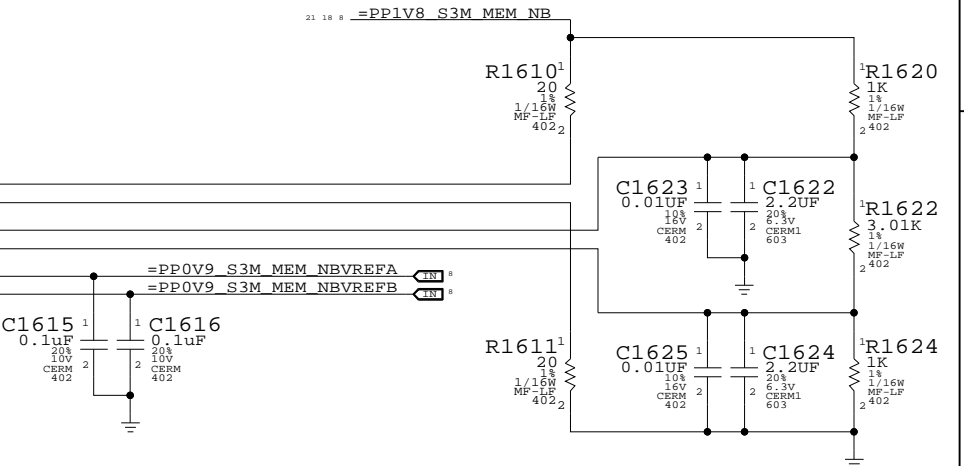
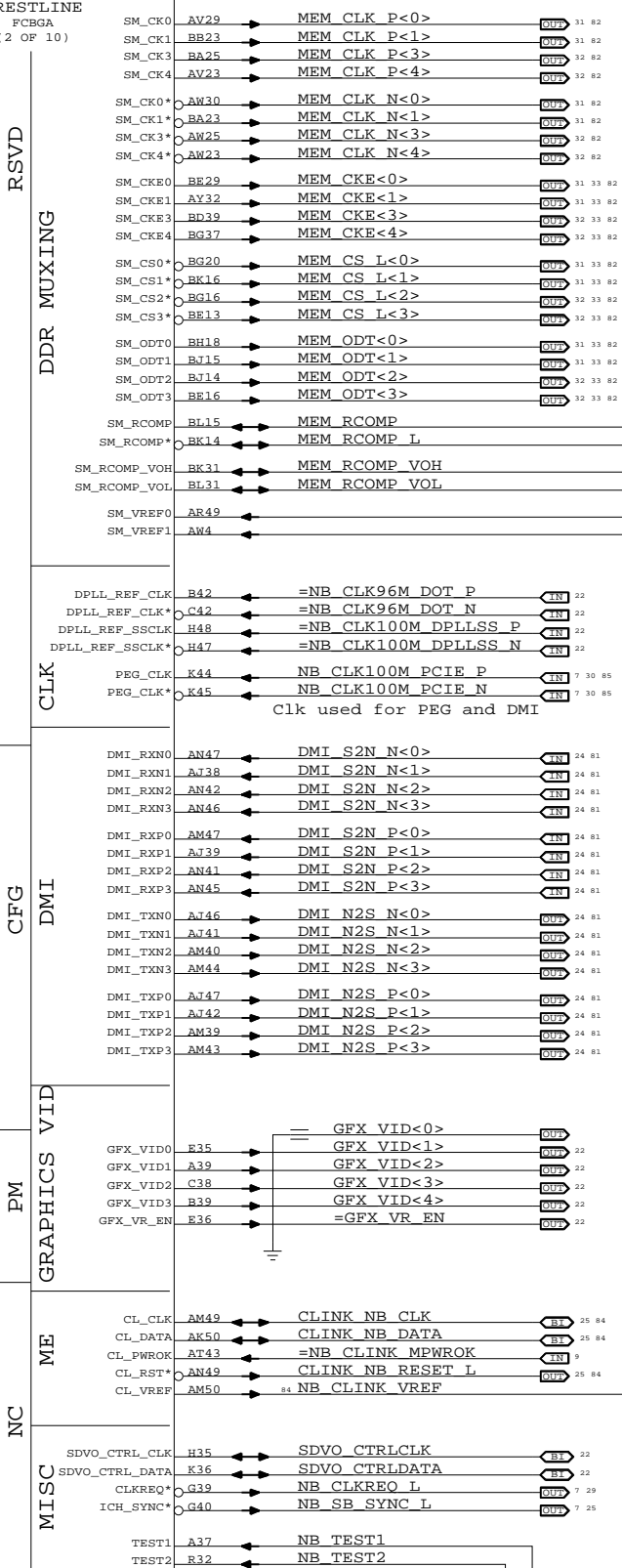
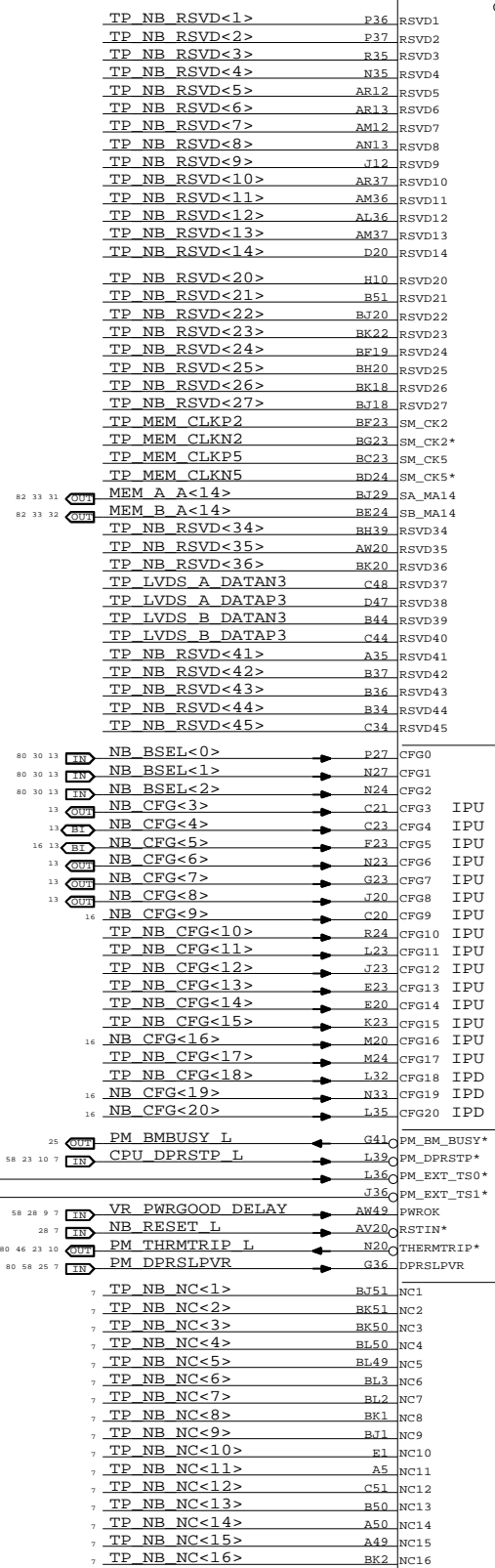
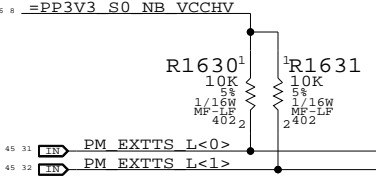
NB_CFG<3>	RESERVED
NB_CFG<4>	RESERVED
NB_CFG<5>	High = DMIx4 Low = DMIx2
NB_CFG<6>	RESERVED
NB_CFG<7>	RESERVED
NB_CFG<8>	RESERVED
NB_CFG<9>	High = Normal PCIe Graphics Lane Reversal Low = Reversed
NB_CFG<10>	RESERVED
NB_CFG<11>	RESERVED
NB_CFG<12>	See Below
NB_CFG<13>	See Below
NB_CFG<14>	RESERVED
NB_CFG<15>	RESERVED
NB_CFG<16>	High = Enabled FSB Dynamic ODT Low = Disabled
NB_CFG<17>	RESERVED
NB_CFG<18>	RESERVED
NB_CFG<19>	High = Reversed DMI Lane Reversal Low = Normal
NB_CFG<20>	High = Both active Concurrent Low = Only SDVO SDVO/PCIe x1 or PCIe x16

NB\_CFG<13:12>  
 00 = RESERVED  
 01 = XOR Mode Enabled  
 10 = All-Z Mode Enabled  
 11 = Normal Operation



NB\_CFG<8:0> used for debug access

NB\_CFG<13:12> require ICT access



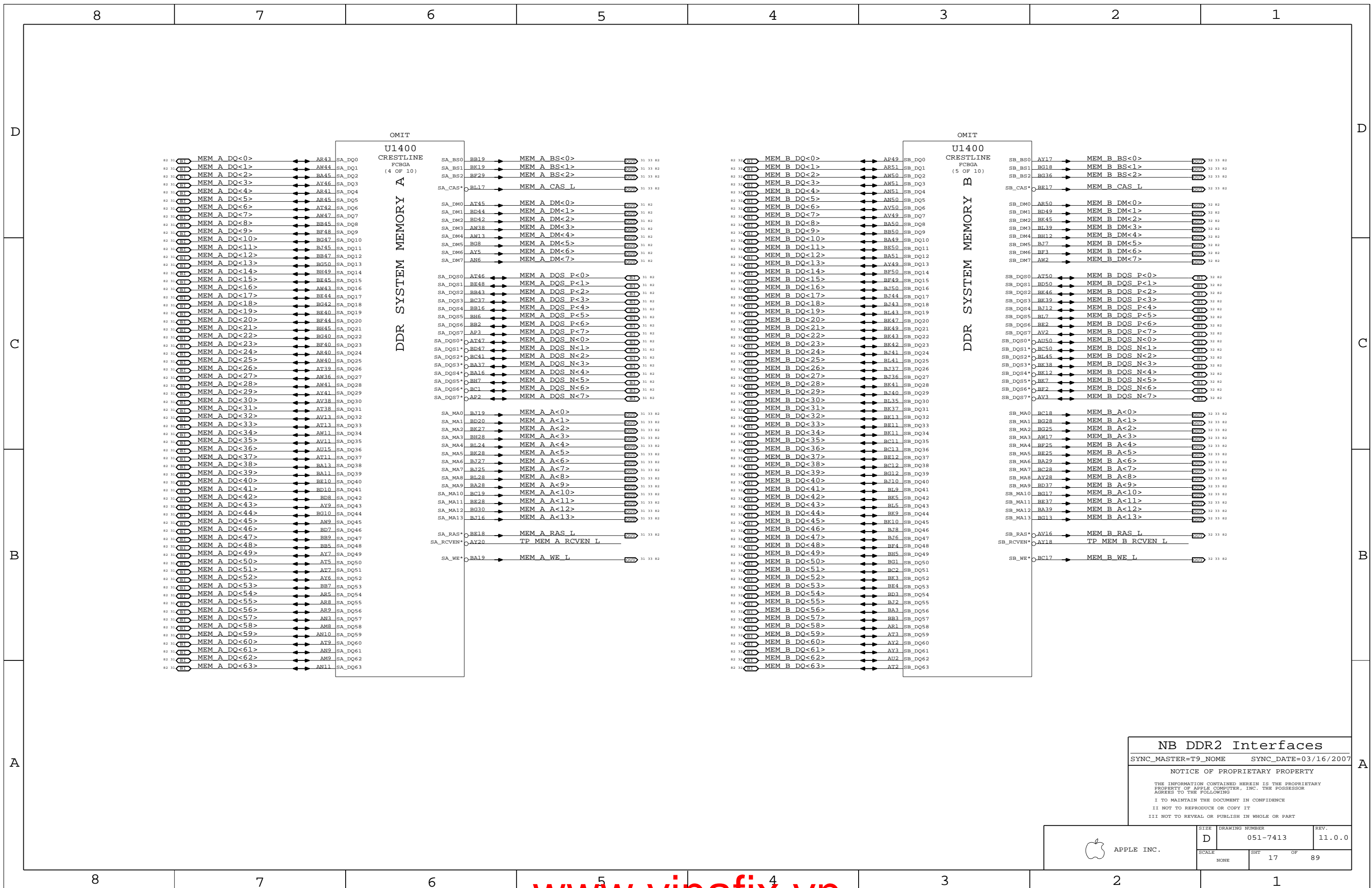
NOTE: GMCH CL\_PWROK input must be PWRGD signal for PP3V3\_SOM, PP3V3\_SOMWOL, PP1V8\_S3M, PP1V25\_SOM, PP1V05\_SOM, PP0V9\_S3M and PP0V9\_SOM. If ME/AMT is not used, short CL\_PWROK to PWROK.

NB Misc Interfaces		
SYNC_MASTER=T9_NOME	SYNC_DATE=03/16/2007	
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SIZE D	DRAWING NUMBER 051-7413	REV. 11.0.0
SCALE NONE	SHT 16	OF 89







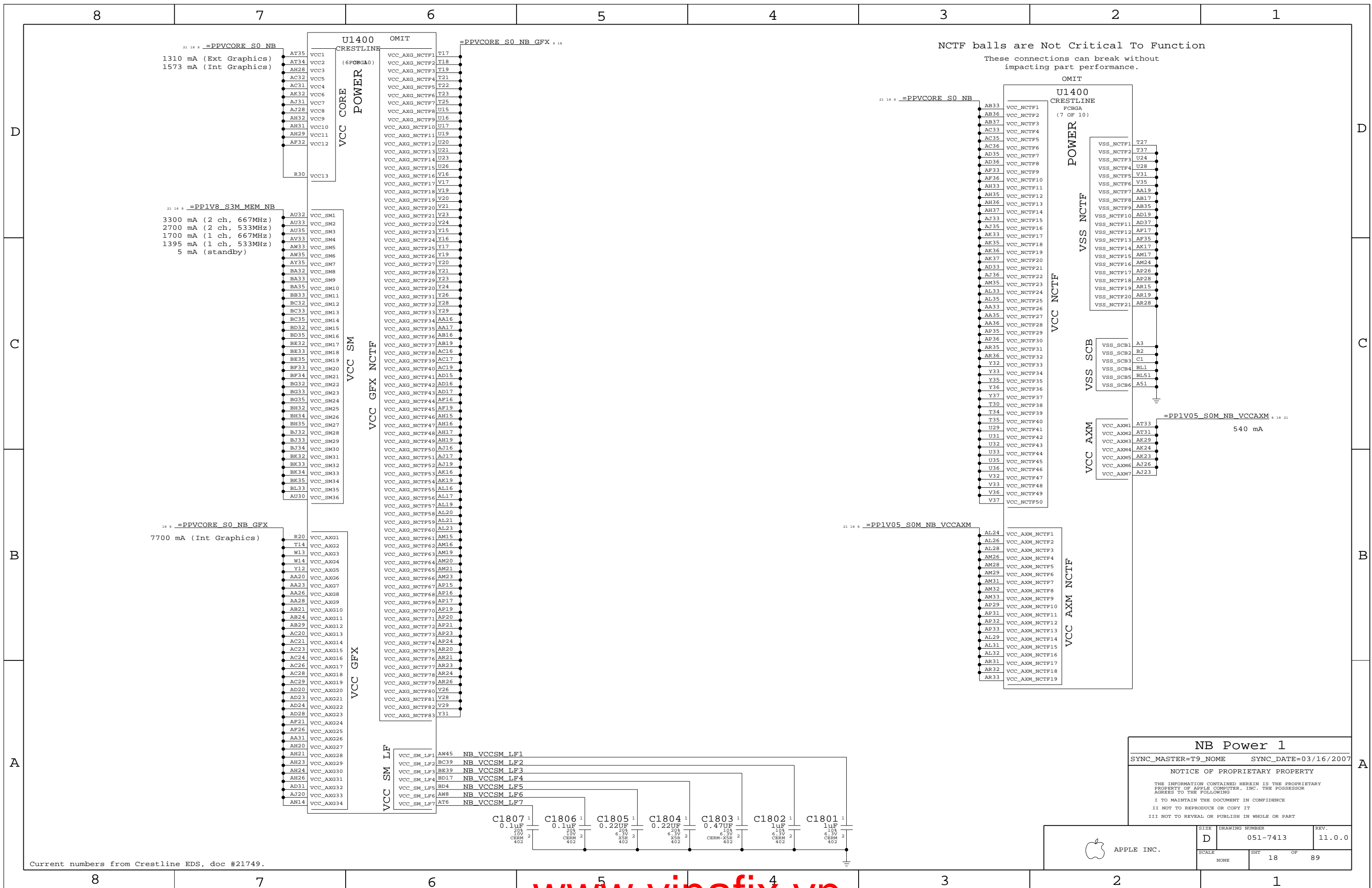
**NB DDR2 Interfaces**  
 SYNC\_MASTER=T9\_NOME      SYNC\_DATE=03/16/2007

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SCALE	SHT	OF	
NONE	17	89	



NCTF balls are Not Critical To Function  
 These connections can break without impacting part performance.

21 18 # =PPVCORE\_S0\_NB  
 1310 mA (Ext Graphics)  
 1573 mA (Int Graphics)

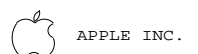
21 16 # =PP1V8\_S3M\_MEM\_NB  
 3300 mA (2 ch, 667MHz)  
 2700 mA (2 ch, 533MHz)  
 1700 mA (1 ch, 667MHz)  
 1395 mA (1 ch, 533MHz)  
 5 mA (standby)

18 # =PPVCORE\_S0\_NB\_GFX  
 7700 mA (Int Graphics)

NB Power 1  
 SYNC\_MASTER=T9\_NOME SYNC\_DATE=03/16/2007

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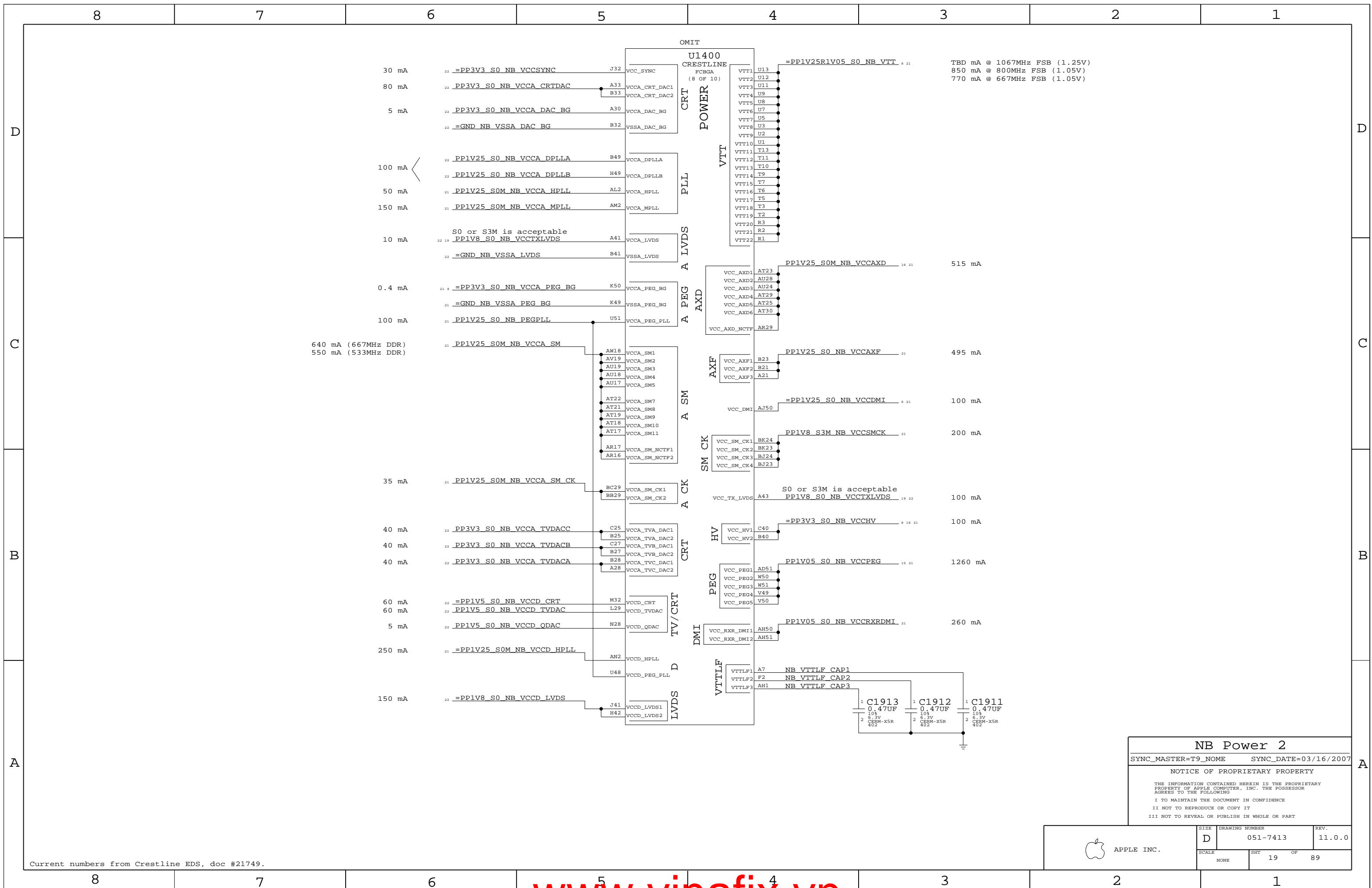


SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0

SCALE	SHT	OF
NONE	18	89

Current numbers from Crestline EDS, doc #21749.

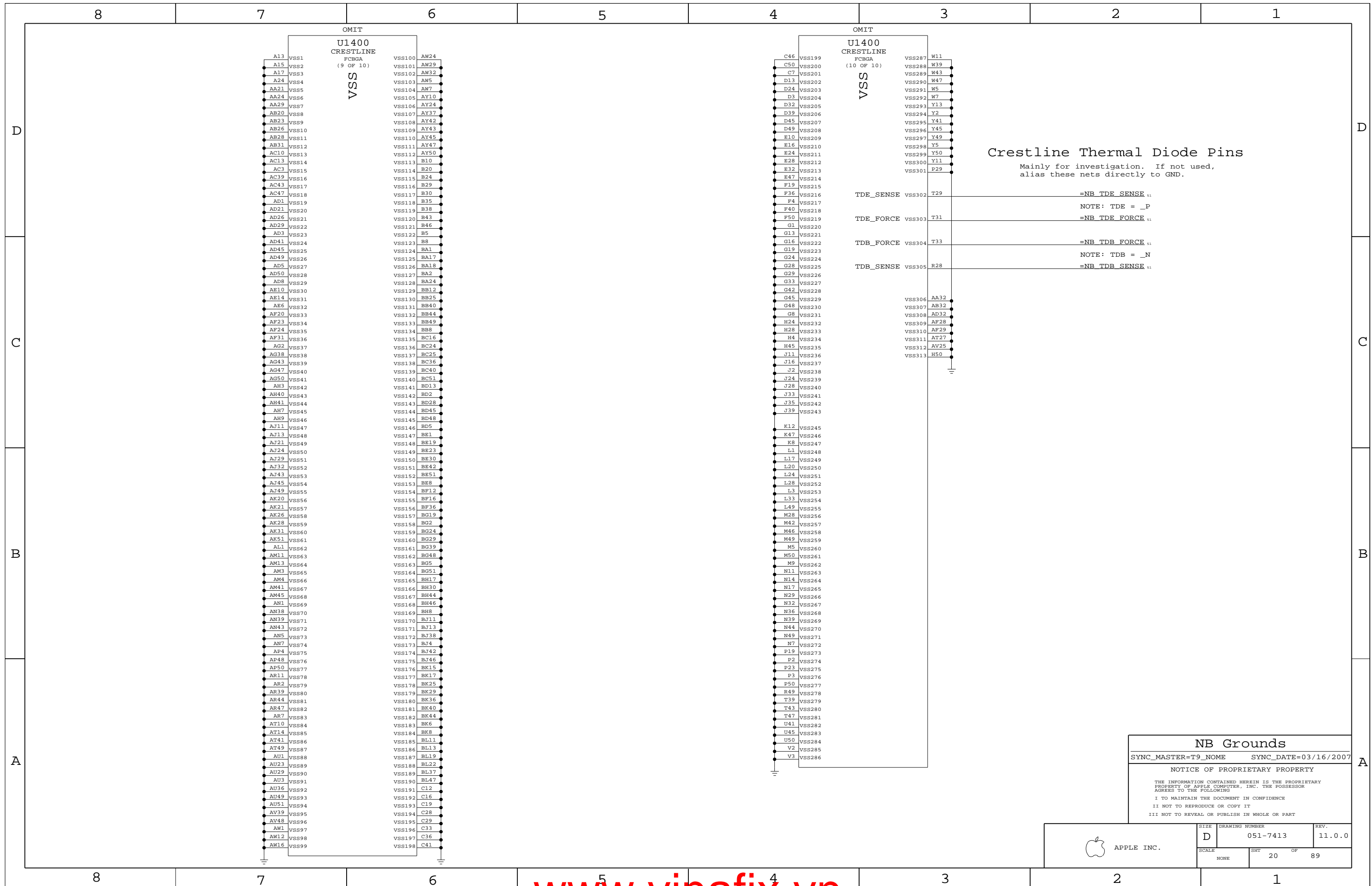




Current numbers from Crestline EDS, doc #21749.

**NB Power 2**  
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APPLE INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7413	REV. 11.0.0
	SCALE NONE	SHEET 19	OF 89

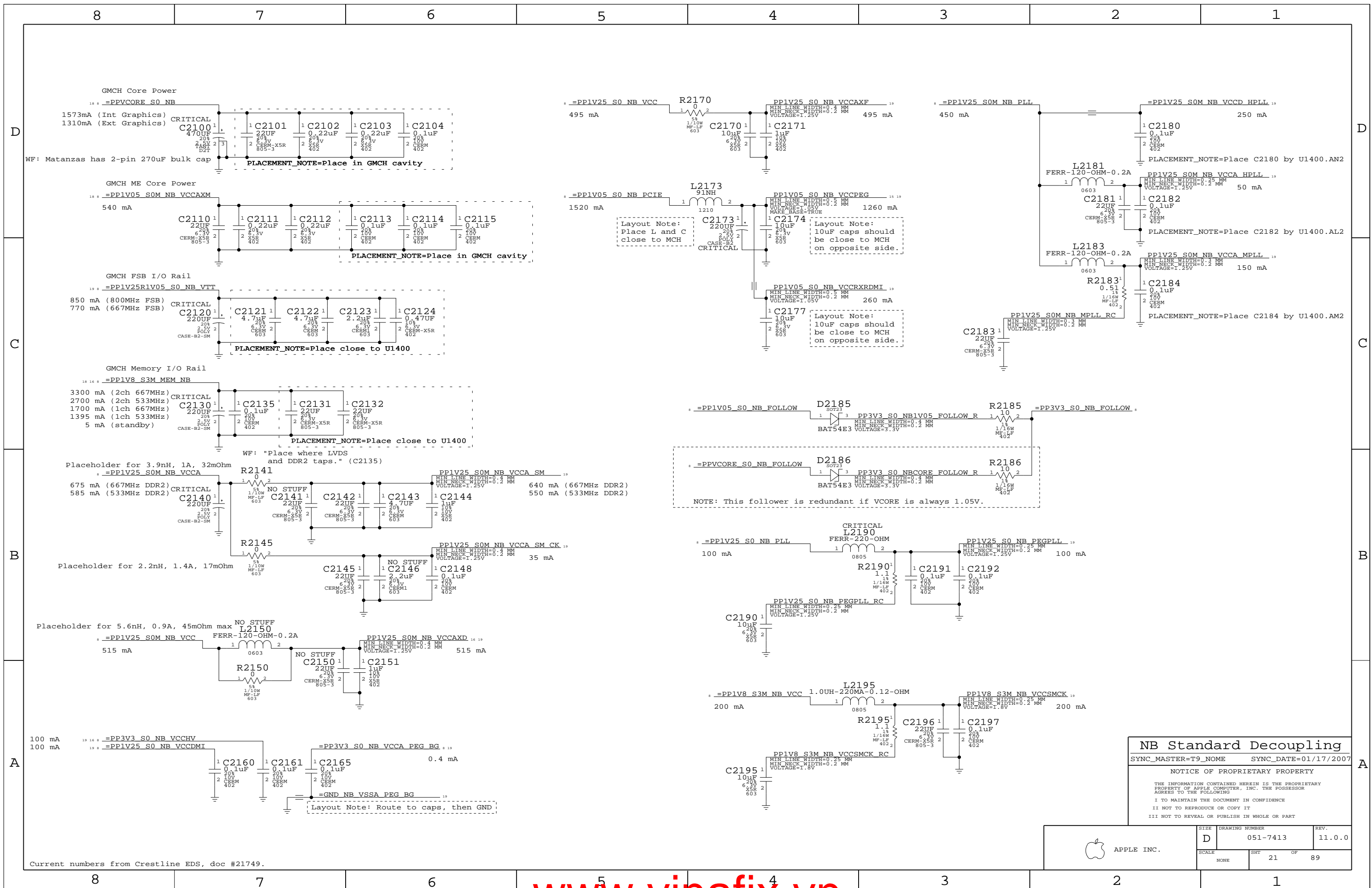


**Crestline Thermal Diode Pins**  
 Mainly for investigation. If not used, alias these nets directly to GND.

**NB Grounds**  
 SYNC\_MASTER=T9\_NAME SYNC\_DATE=03/16/2007

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SCALE	SHT	OF	
NONE	20	89	



**NB Standard Decoupling**

SYNC\_MASTER=T9\_NOME SYNC\_DATE=01/17/2007

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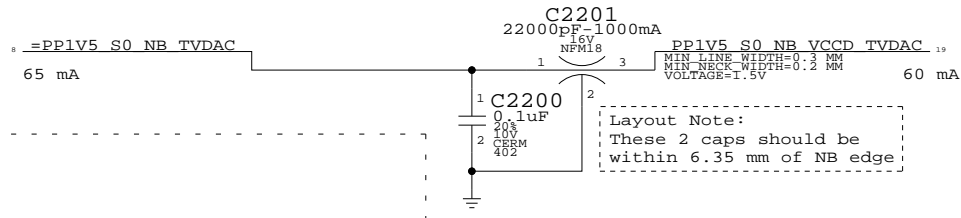
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	SCALE	DRAWING NUMBER	REV.
	NONE	D 051-7413	11.0.0
SHEET		OF	
21		89	

Current numbers from Crestline EDS, doc #21749.

# Crestline LVDS Strapping

NOTE: This filter is required even if using only external graphics.  
 VCCD\_TVDAC also powers internal thermal sensors.



- 15 LVDS DDC CLK
- 15 LVDS DDC DATA
- 15 LVDS CTRL\_CLK
- 15 LVDS CTRL\_DATA
- 15 =CRT RED
- 15 =CRT RED L
- 15 =CRT GREEN
- 15 =CRT GREEN L
- 15 =CRT BLUE
- 15 =CRT BLUE L
- 15 =CRT HSYNC R
- 15 =CRT VSYNC R
- 15 =CRT TVO IREF
- 15 =TV A DAC
- 15 =TV A RTN
- 15 =TV B DAC
- 15 =TV B RTN
- 15 =TV C DAC
- 15 =TV C RTN
- 15 CRT DDC CLK
- 15 CRT DDC DATA
- 16 SDVO CTRLCLK
- 16 SDVO CTRLDATA
- 15 TV\_DCONSEL<0>
- 15 TV\_DCONSEL<1>
- 16 =NB\_CLK96M\_DOT\_N
- 16 =NB\_CLK96M\_DOT\_P
- 16 =NB\_CLK100M\_DPLLSS\_P
- 16 =NB\_CLK100M\_DPLLSS\_N

- 19 =GND\_NB\_VSSA\_LVDS
- 19 PPIV8\_S0\_NB\_VCCTLVDS
- 19 PPIV25\_S0\_NB\_VCCA\_DPLL
- 19 PPIV25\_S0\_NB\_VCCA\_DPLLA
- 19 =PPIV8\_S0\_NB\_VCCD\_LVDS
- 19 =PPIV5\_S0\_NB\_VCCD\_CRT
- 19 PP3V3\_S0\_NB\_VCCA\_CRTDAC
- 19 =PP3V3\_S0\_NB\_VCCSYNC
- 19 PPIV5\_S0\_NB\_VCCD\_QDAC
- 19 PP3V3\_S0\_NB\_VCCA\_DAC\_BG
- 19 =GND\_NB\_VSSA\_DAC\_BG
- 19 PP3V3\_S0\_NB\_VCCA\_TVDACA
- 19 PP3V3\_S0\_NB\_VCCA\_TVDACB
- 19 PP3V3\_S0\_NB\_VCCA\_TVDACC

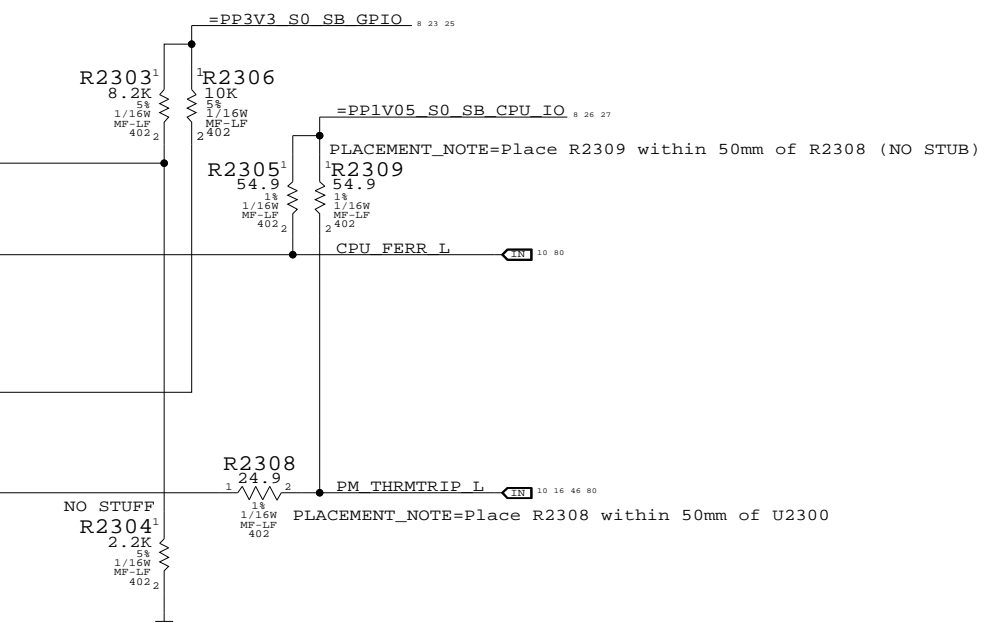
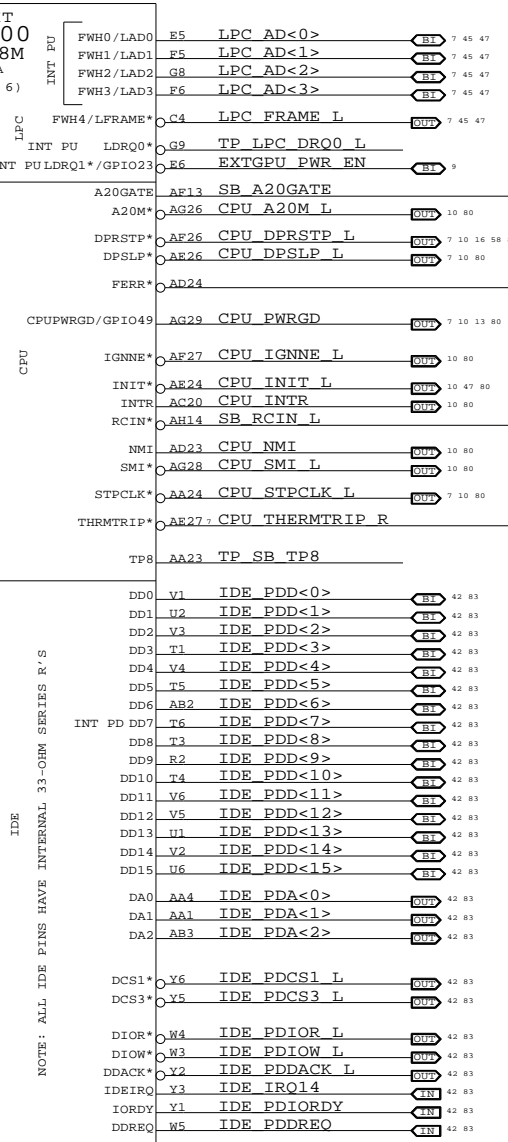
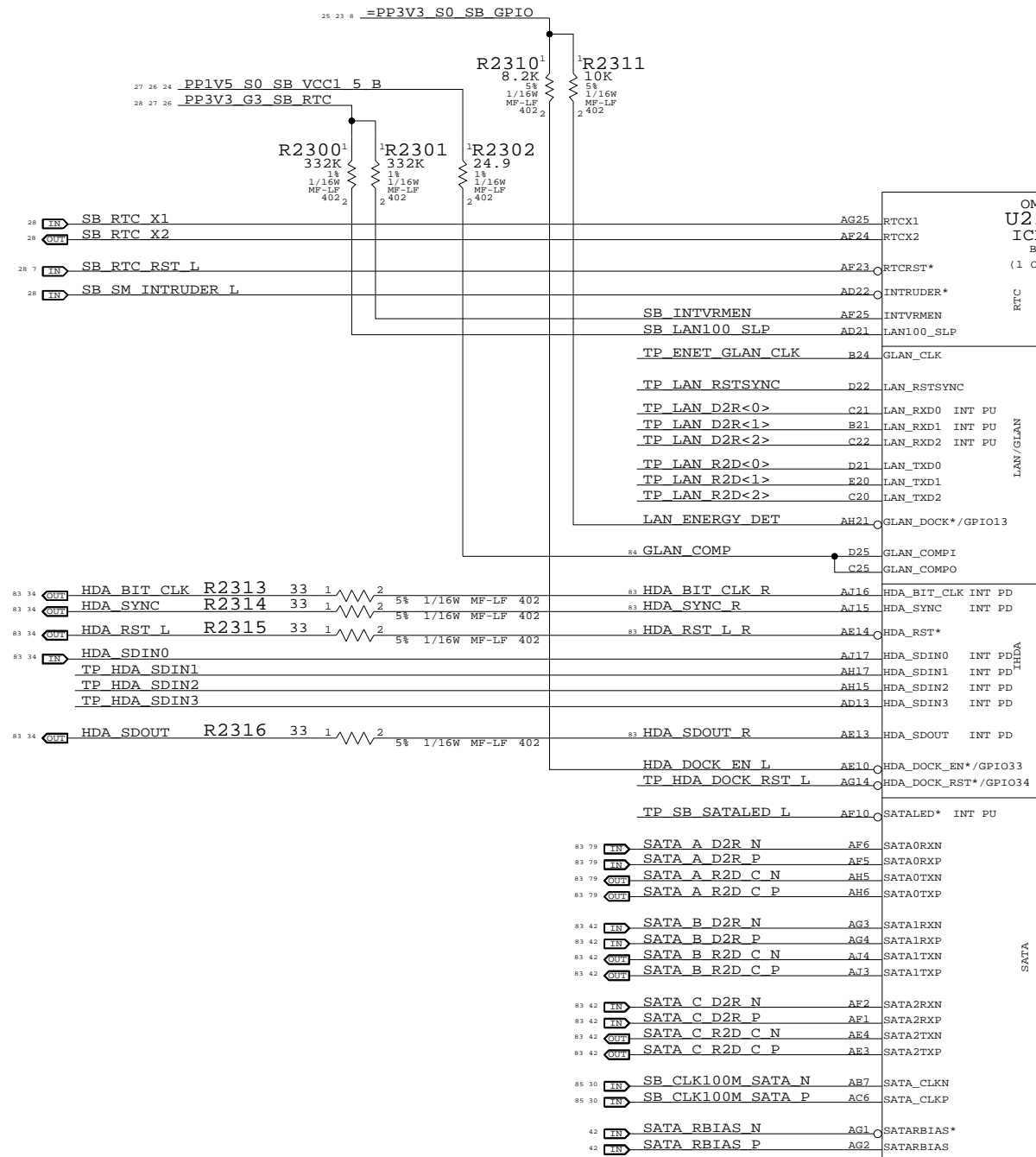
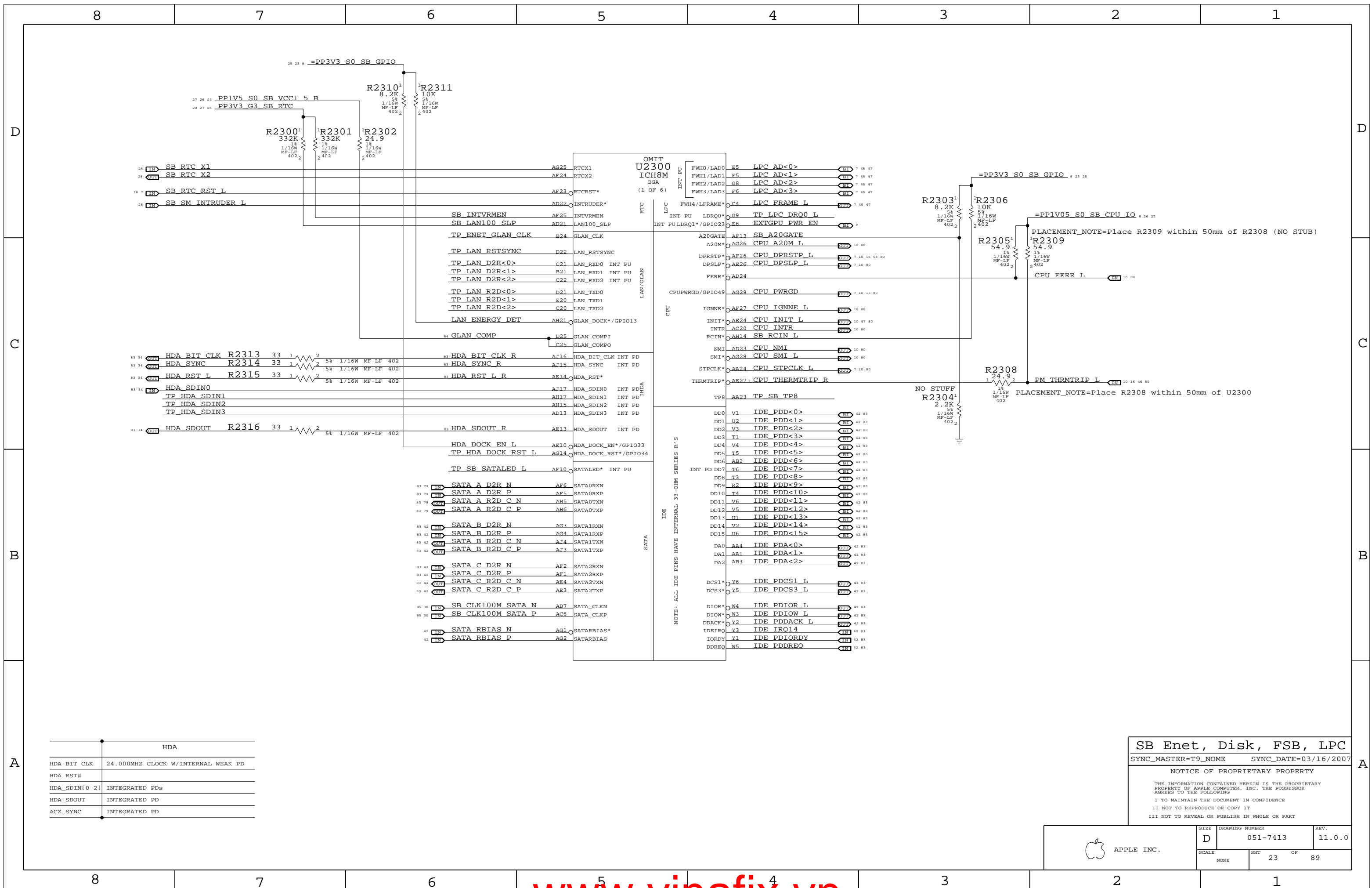
- 15 LVDS\_BKLT\_CTL
- 15 LVDS\_BKLT\_EN
- 15 LVDS\_VDD\_EN
- 15 LVDS\_IBG
- 15 TP\_LVDS\_VBG
- 15 LVDS\_A\_CLK\_N
- 15 LVDS\_A\_CLK\_P
- 15 LVDS\_B\_CLK\_N
- 15 LVDS\_B\_CLK\_P
- 15 LVDS\_A\_DATA\_N<0>
- 15 LVDS\_A\_DATA\_N<1>
- 15 LVDS\_A\_DATA\_N<2>
- 15 LVDS\_A\_DATA\_P<0>
- 15 LVDS\_A\_DATA\_P<1>
- 15 LVDS\_A\_DATA\_P<2>
- 15 LVDS\_B\_DATA\_N<0>
- 15 LVDS\_B\_DATA\_N<1>
- 15 LVDS\_B\_DATA\_N<2>
- 15 LVDS\_B\_DATA\_P<0>
- 15 LVDS\_B\_DATA\_P<1>
- 15 LVDS\_B\_DATA\_P<2>
- 15 TP\_LVDS\_VREFH
- 15 TP\_LVDS\_VREFL
- 16 GFX\_VID<1>
- 16 GFX\_VID<2>
- 16 GFX\_VID<3>
- 16 GFX\_VID<4>
- 16 =GFX\_VR\_EN

**NB Graphics Decoupling**  
 SYNC\_MASTER=M76\_MLB    SYNC\_DATE=03/12/2007

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	SCALE NONE	SHT 22	OF 89

Current numbers from Crestline EDS Addendum, doc #20127.



HDA	
HDA_BIT_CLK	24.000MHZ CLOCK W/INTERNAL WEAK PD
HDA_RST#	
HDA_SDIN[0-2]	INTEGRATED PDs
HDA_SDOUT	INTEGRATED PD
ACZ_SYNC	INTEGRATED PD

**SB Enet, Disk, FSB, LPC**  
 SYNC\_MASTER=T9\_NOME SYNC\_DATE=03/16/2007

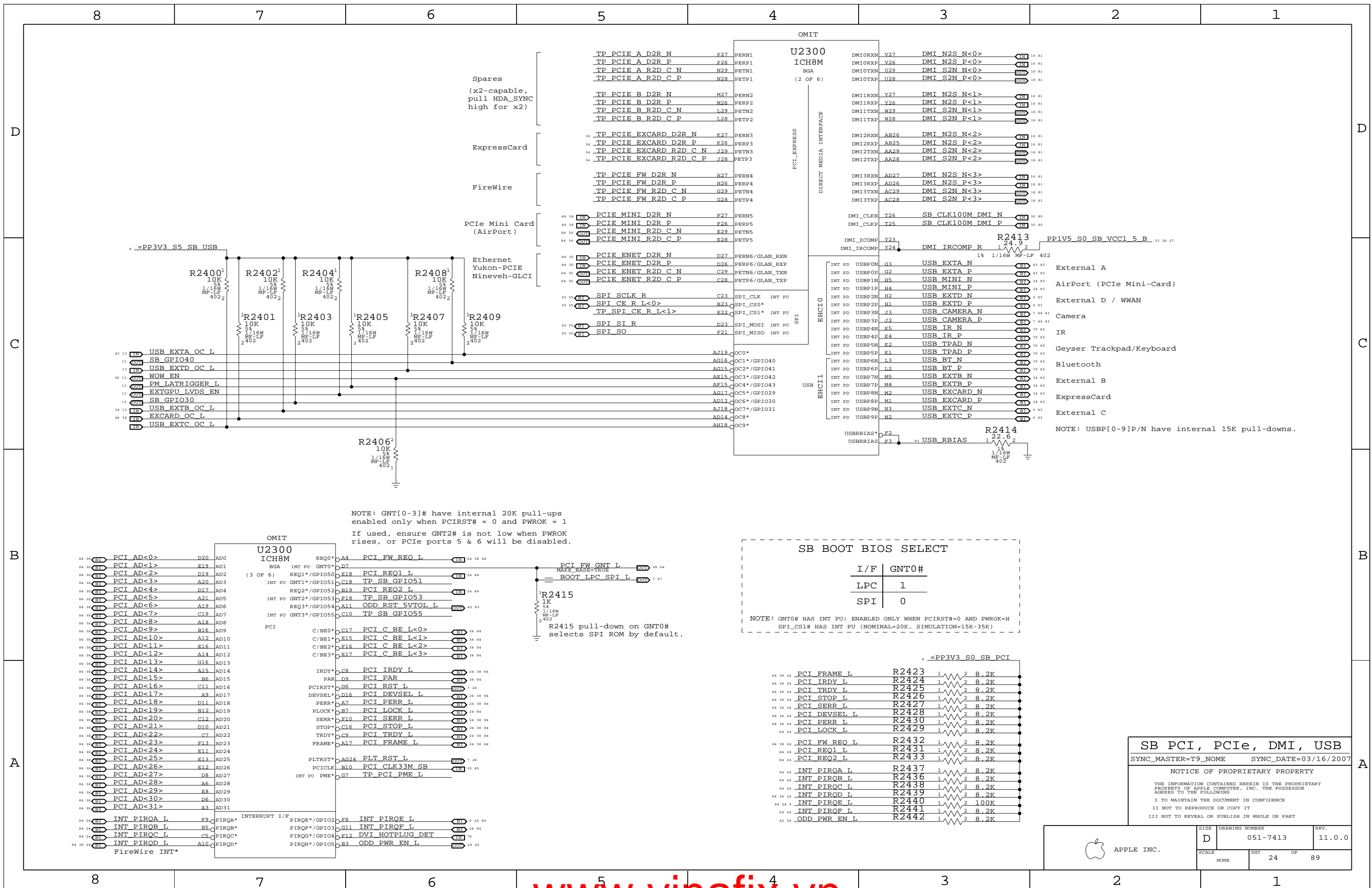
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NONE	23	89	





NOTE: GNT[0-3]# have internal 20K pull-ups enabled only when PCIRST# = 0 and PWROK = 1. If used, ensure GNT2# is not low when PWROK rises, or PCIe ports 5 & 6 will be disabled.

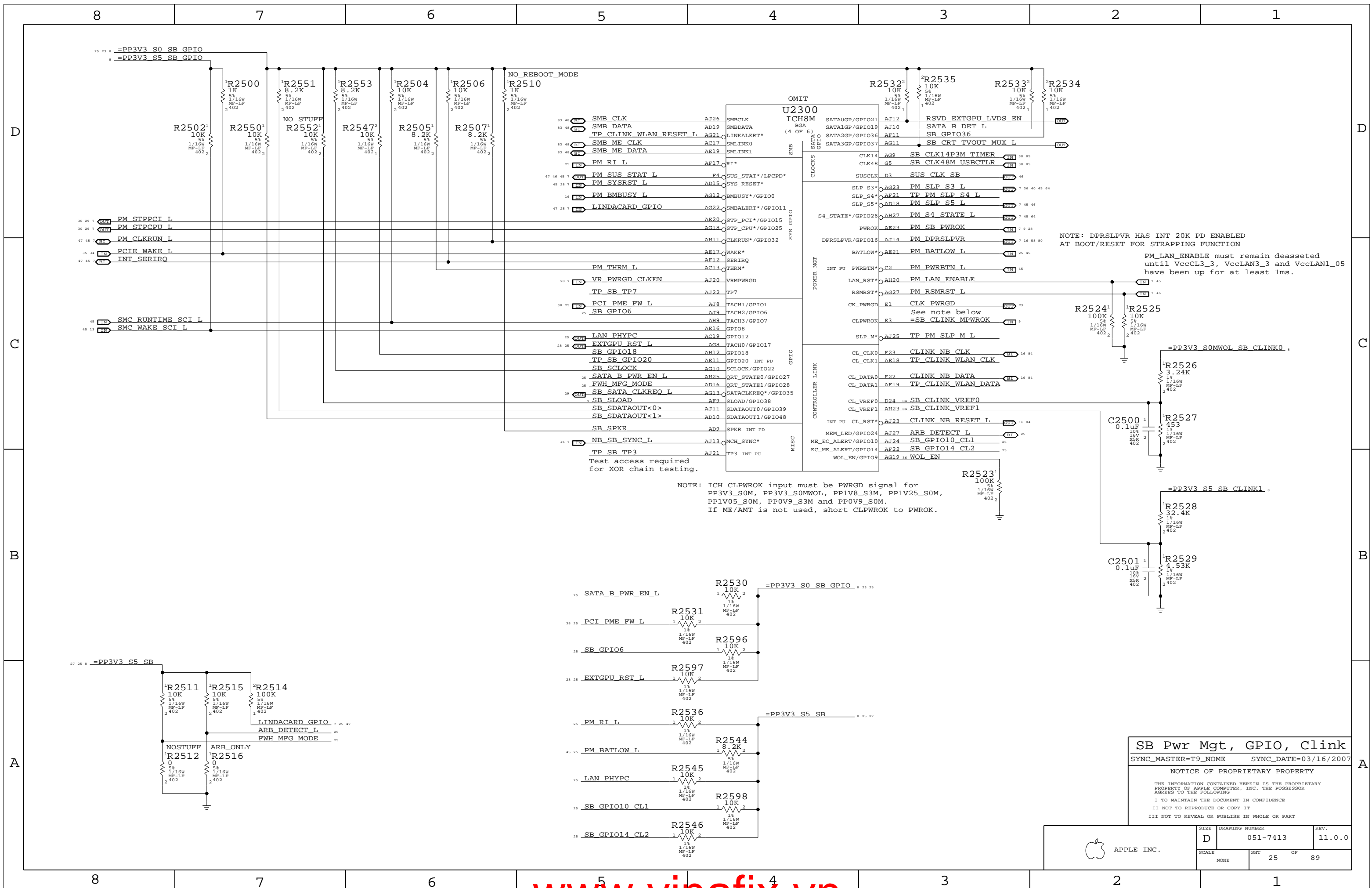
SB BOOT BIOS SELECT	
I/F	GNT0#
LPC	1
SPI	0

NOTE: GNT0# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H  
SPI\_CS1# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)

SB PCI, PCIe, DMI, USB  
SYNC\_MASTER=T9\_NOME SYNC\_DATE=03/16/2007

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	D	051-7413	11.0.0
SCALE	SHT	OF	
NONE	24	89	



NOTE: DPRSLPVR HAS INT 20K PD ENABLED AT BOOT/RESET FOR STRAPPING FUNCTION

PM\_LAN\_ENABLE must remain deasserted until VccCL3\_3, VccLAN3\_3 and VccLAN1\_05 have been up for at least 1ms.

NOTE: ICH CLPWROK input must be PWRGD signal for PP3V3\_S0M, PP3V3\_S0MWOL, PP1V8\_S3M, PP1V25\_S0M, PP1V05\_S0M, PP0V9\_S3M and PP0V9\_S0M. If ME/AMT is not used, short CLPWROK to PWROK.

**SB Pwr Mgt, GPIO, Clink**  
 SYNC\_MASTER=T9\_NOME SYNC\_DATE=03/16/2007

NOTICE OF PROPRIETARY PROPERTY

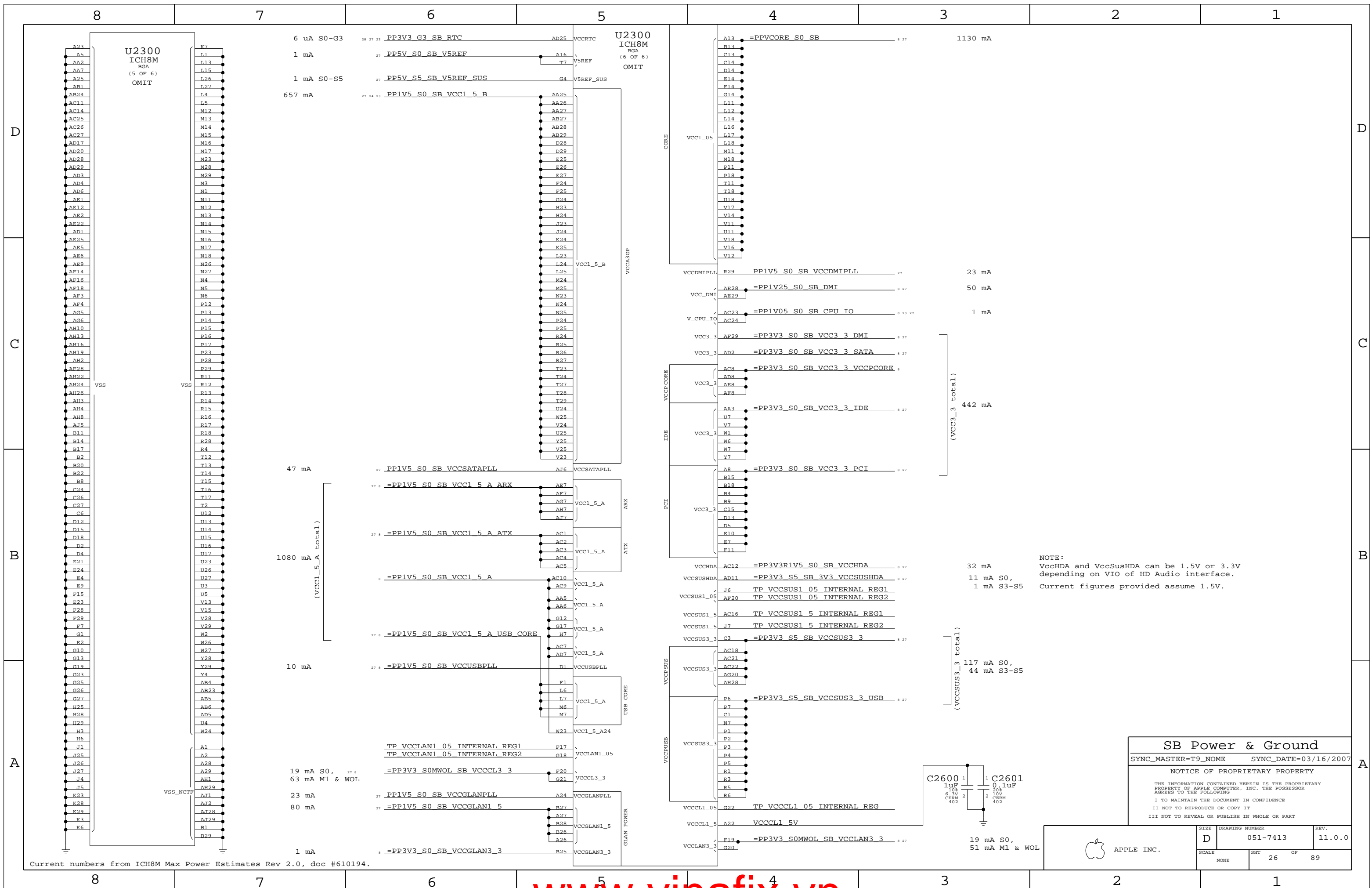
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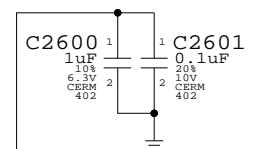
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7413	11.0.0
SCALE	SHT	OF	
NONE	25	89	



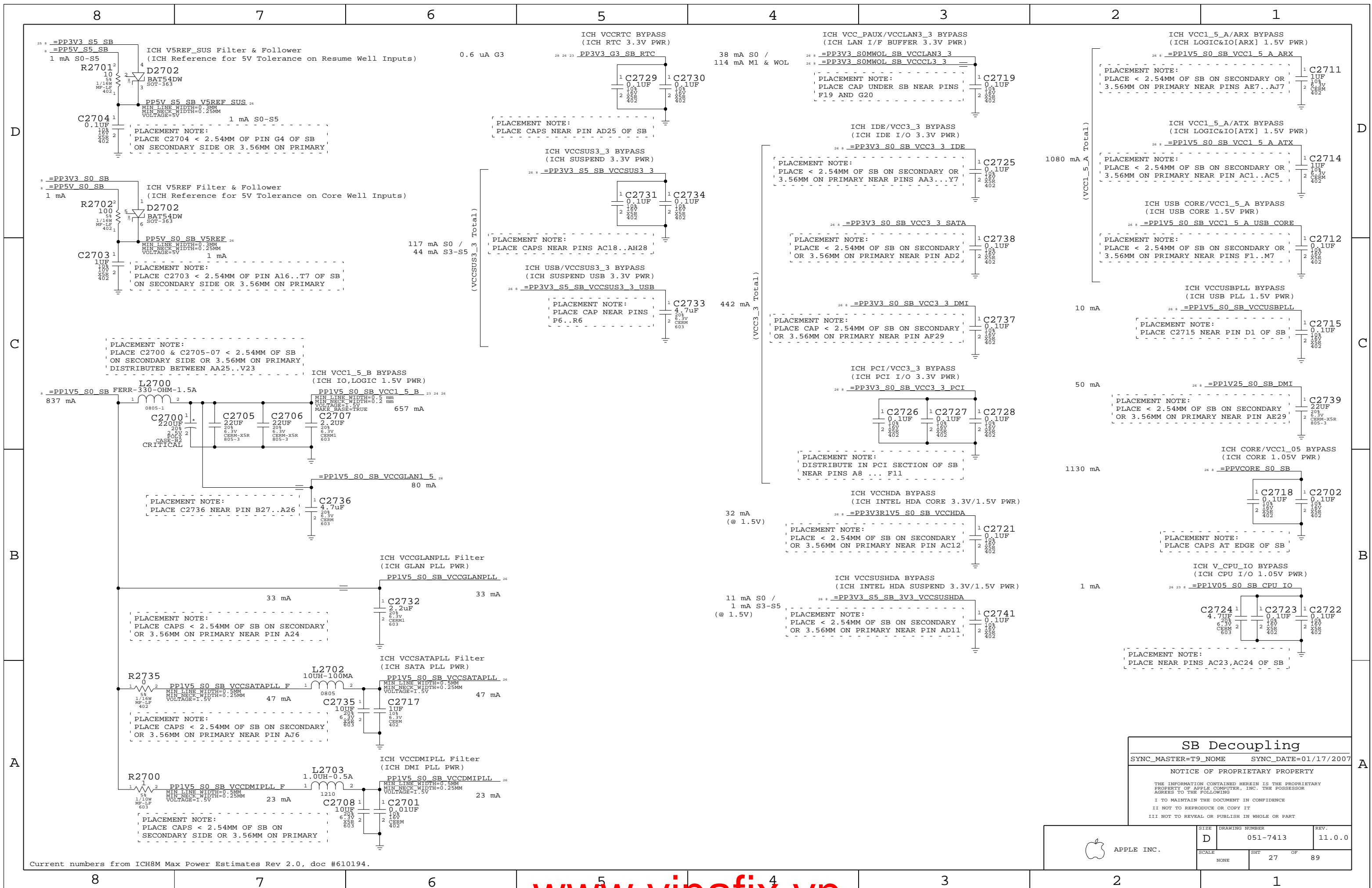
Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.

NOTE:  
VcchDA and VccSusHDA can be 1.5V or 3.3V depending on VIO of HD Audio interface.  
Current figures provided assume 1.5V.



SB Power & Ground		
SYNC_MASTER=T9_NOME	SYNC_DATE=03/16/2007	
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	SCALE NONE	SHEET 26	OF 89



**SB Decoupling**

SYNC\_MASTER=T9\_NOME    SYNC\_DATE=01/17/2007

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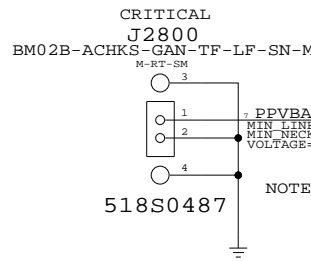
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7413	11.0.0
SCALE	SHT	OF	REV.
NONE	27	89	89

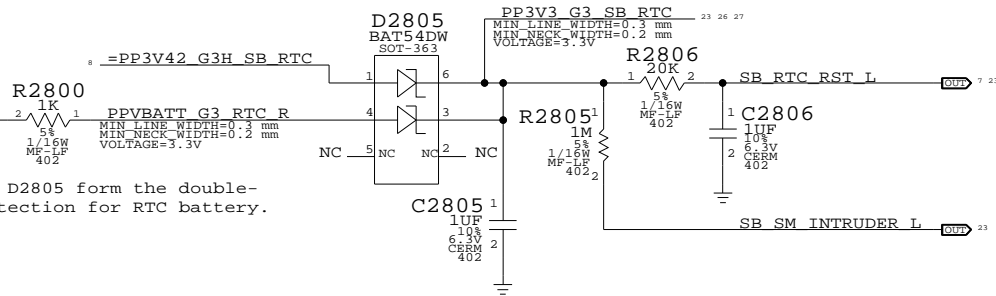
Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.



Coin-Cell Connector

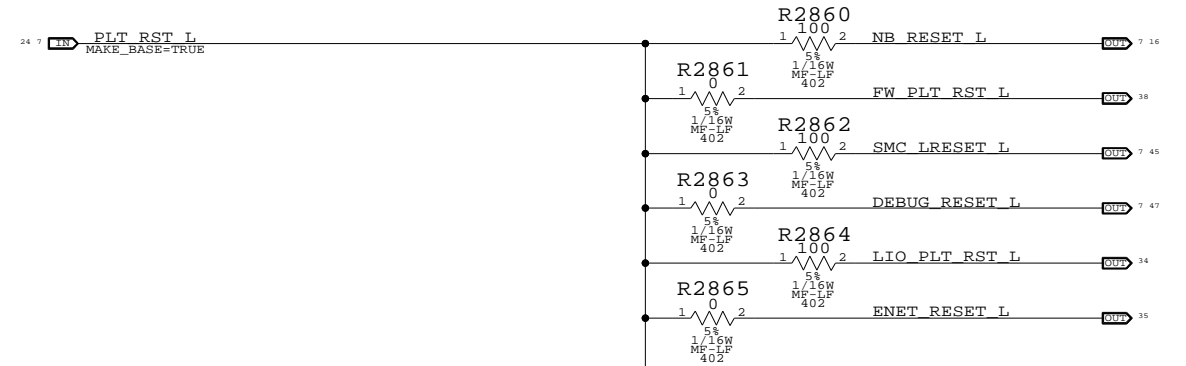


RTC Power Sources

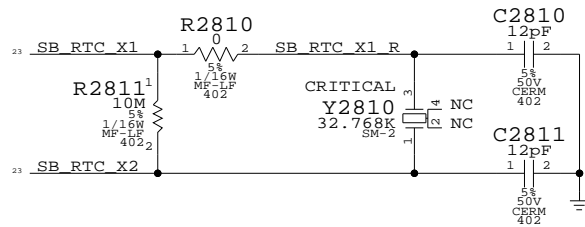


Platform Reset Connections

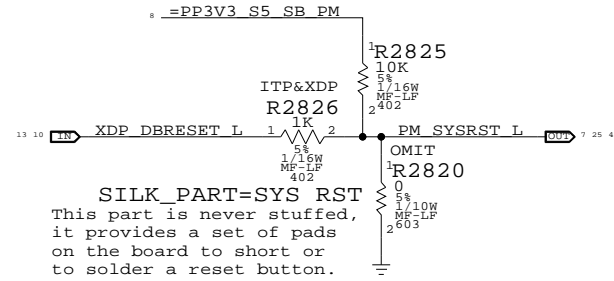
Unbuffered



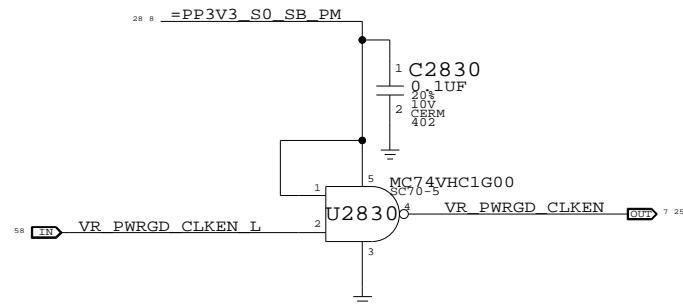
SB RTC Crystal



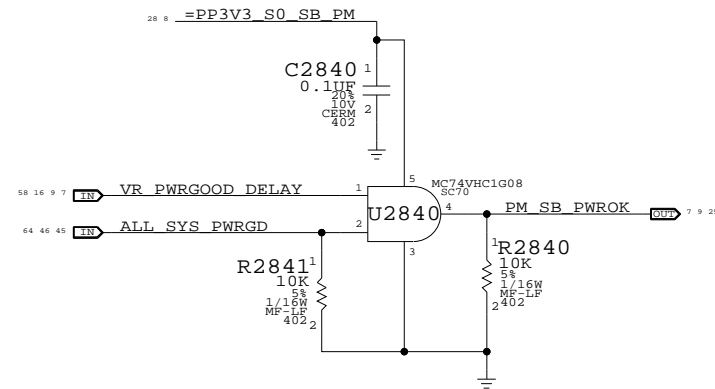
System Reset "Button"



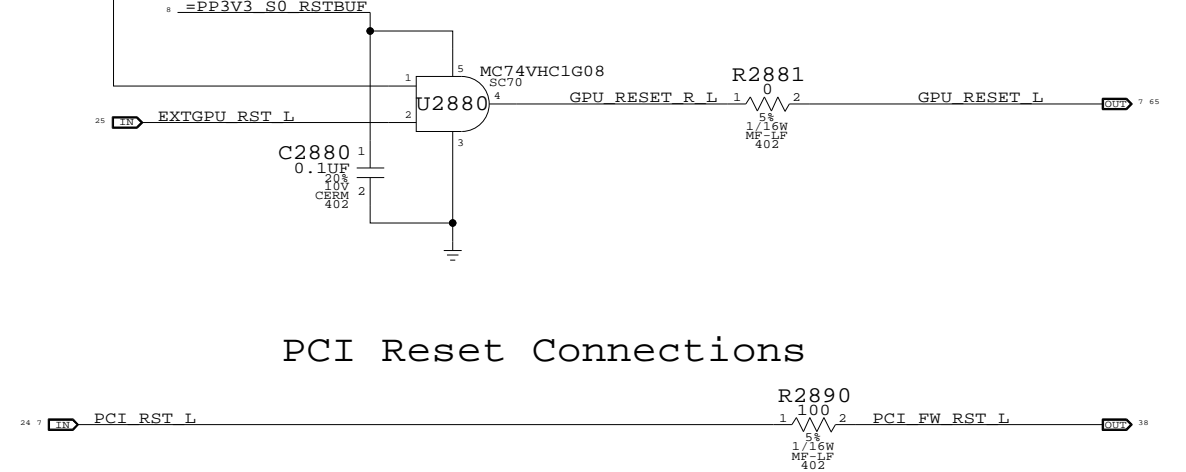
VRMPWRGD Inverter



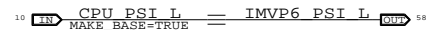
PWROK Circuit



PCI Reset Connections



CPU VCore ForcePSI

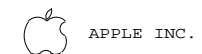


SB Misc

SYNC\_MASTER=(T9\_MLB) SYNC\_DATE=08/24/2006

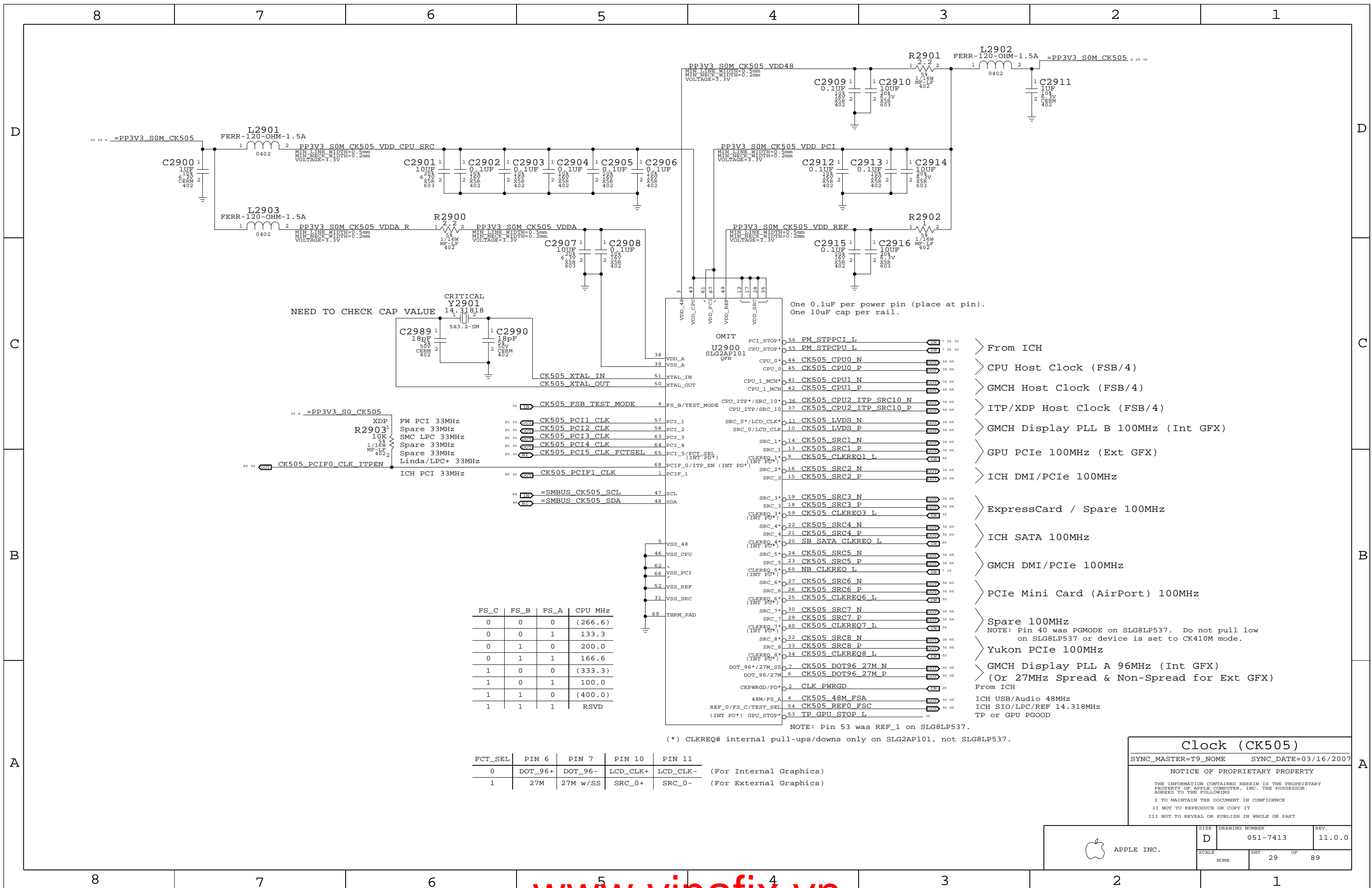
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SCALE	SHT	OF
NONE	28	89





NEED TO CHECK CAP VALUE

One 0.1uF per power pin (place at pin).  
One 10uF cap per rail.

FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

FCT_SEL	PIN 6	PIN 7	PIN 10	PIN 11	
0	DOT_96+	DOT_96-	LCD_CLK+	LCD_CLK-	(For Internal Graphics)
1	27M	27M w/SS	SRC_0+	SRC_0-	(For External Graphics)

- > From ICH
- > CPU Host Clock (FSB/4)
- > GMCH Host Clock (FSB/4)
- > ITP/XDP Host Clock (FSB/4)
- > GMCH Display PLL B 100MHz (Int GFX)
- > GPU PCIe 100MHz (Ext GFX)
- > ICH DMI/PCIe 100MHz
- > ExpressCard / Spare 100MHz
- > ICH SATA 100MHz
- > GMCH DMI/PCIe 100MHz
- > PCIe Mini Card (AirPort) 100MHz
- > Spare 100MHz
- NOTE: Pin 40 was PGMODE on SLG8LP537. Do not pull low on SLG8LP537 or device is set to CK410M mode.
- > Yukon PCIe 100MHz
- > GMCH Display PLL A 96MHz (Int GFX)
- > (Or 27MHz Spread & Non-Spread for Ext GFX)
- From ICH
- ICH USB/Audio 48MHz
- ICH SIO/LPC/REF 14.318MHz
- TP or GPU PGOOD

NOTE: Pin 53 was REF\_1 on SLG8LP537.

(\*) CLKREQ# internal pull-ups/downs only on SLG2AP101, not SLG8LP537.

**Clock (CK505)**

SYNC\_MASTER=T9\_NOME      SYNC\_DATE=03/16/2007

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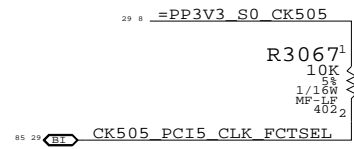
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7413	11.0.0
SCALE	SHT	OF	
NONE	29	89	

# CLK Termination

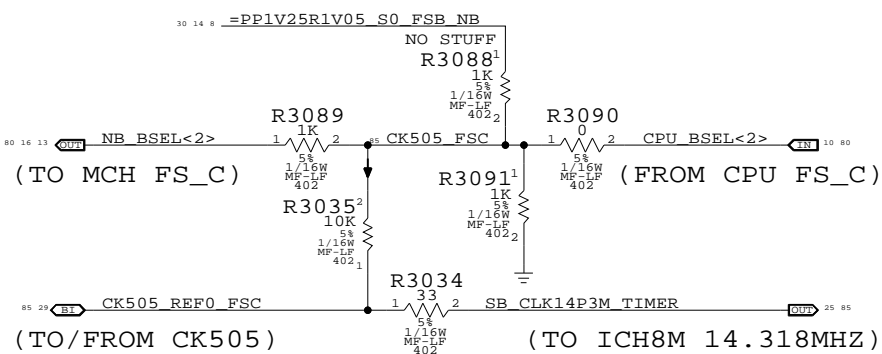
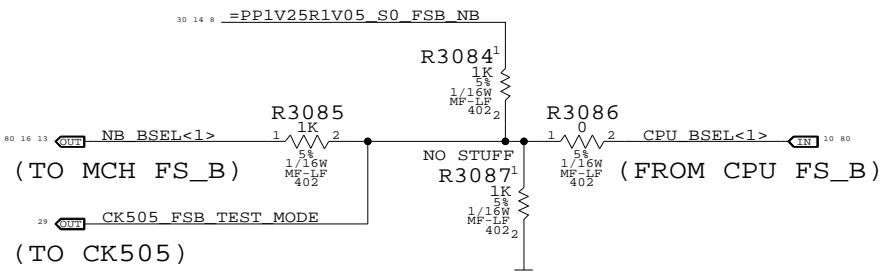
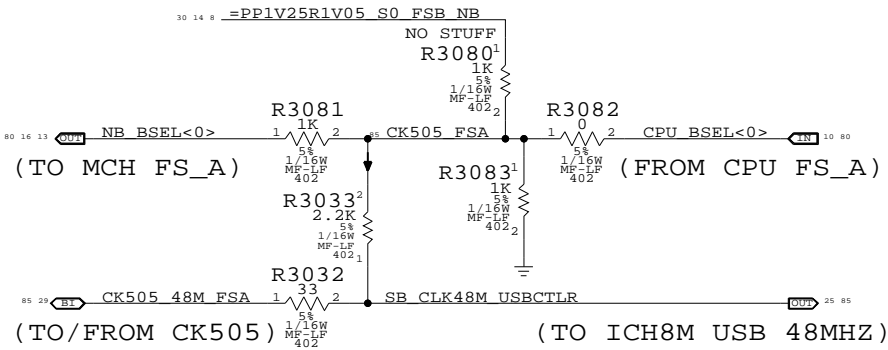
(Note: HOST/SRC/GFX clock termination removed. Silago SL8GLP536 or equiv. support only)

## CK505 Configuration Straps

FCT\_SEL (GFX clock select)



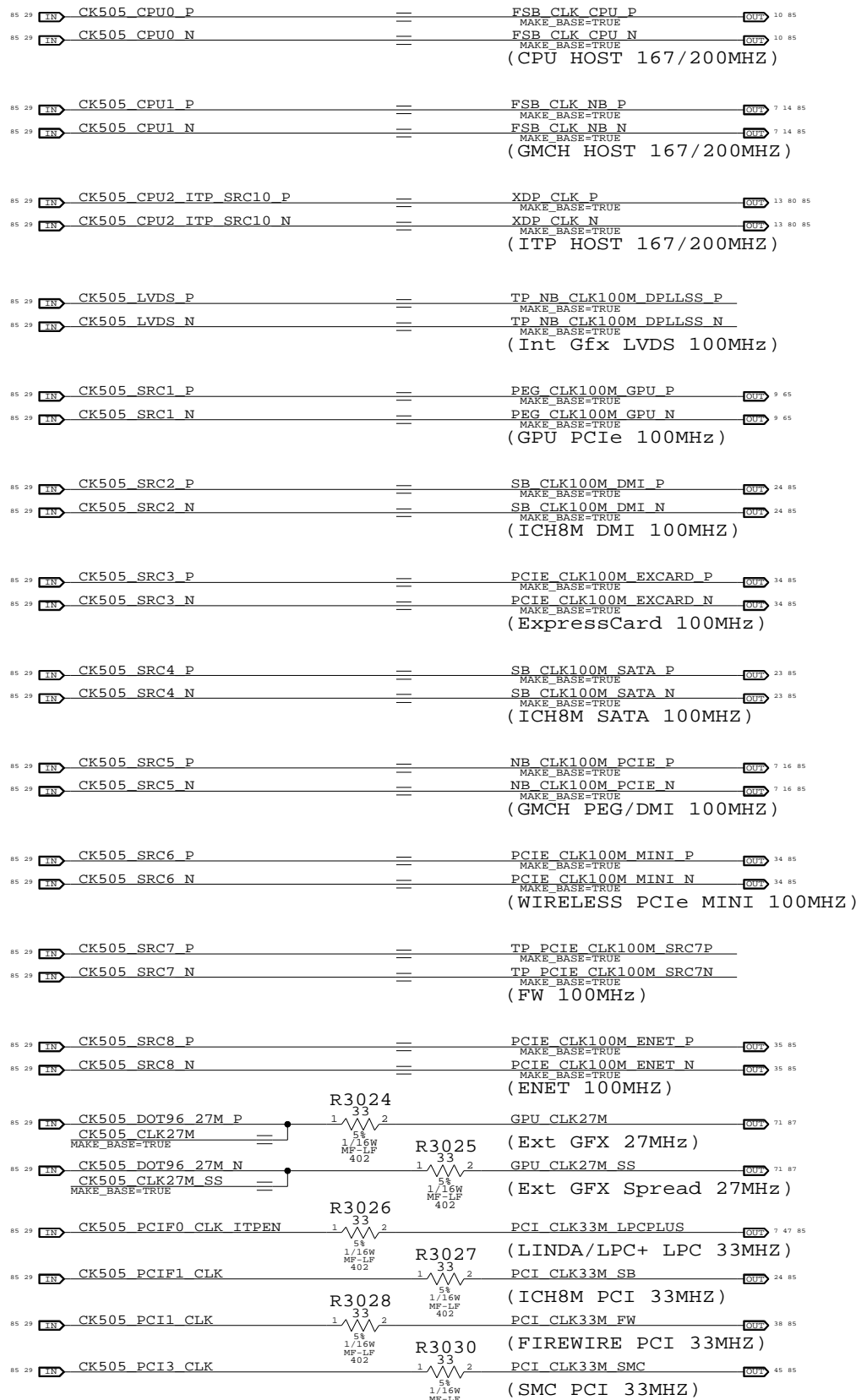
FS\_A, FS\_B, FS\_C (Host clock freq select)



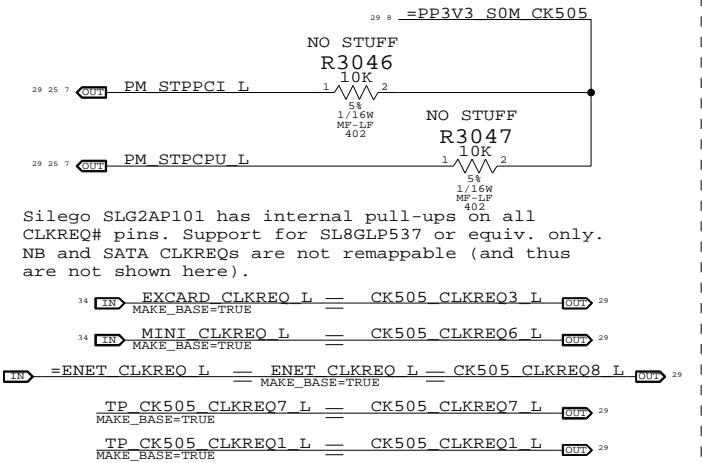
FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

NO STUFF R3082, R3086 & R3090 for manual CPU clk frequency.

(Only 100-200MHz supported by SLG8LP536 and CY28545-5)

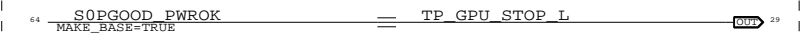


## CLKREQ Controls

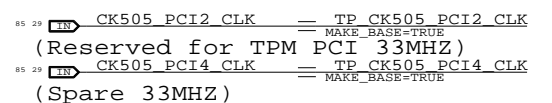


Silego SLG2AP101 has internal pull-ups on all CLKREQ# pins. Support for SL8GLP537 or equiv. only. NB and SATA CLKREQs are not remappable (and thus are not shown here).

## GPU Clock Gating



## Unused Clocks

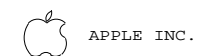


## Clock Termination

SYNC\_MASTER=(MASTER) SYNC\_DATE=08/23/2006

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SCALE	SHT	OF
NONE	30	89



# Page Notes

Power aliases required by this page:

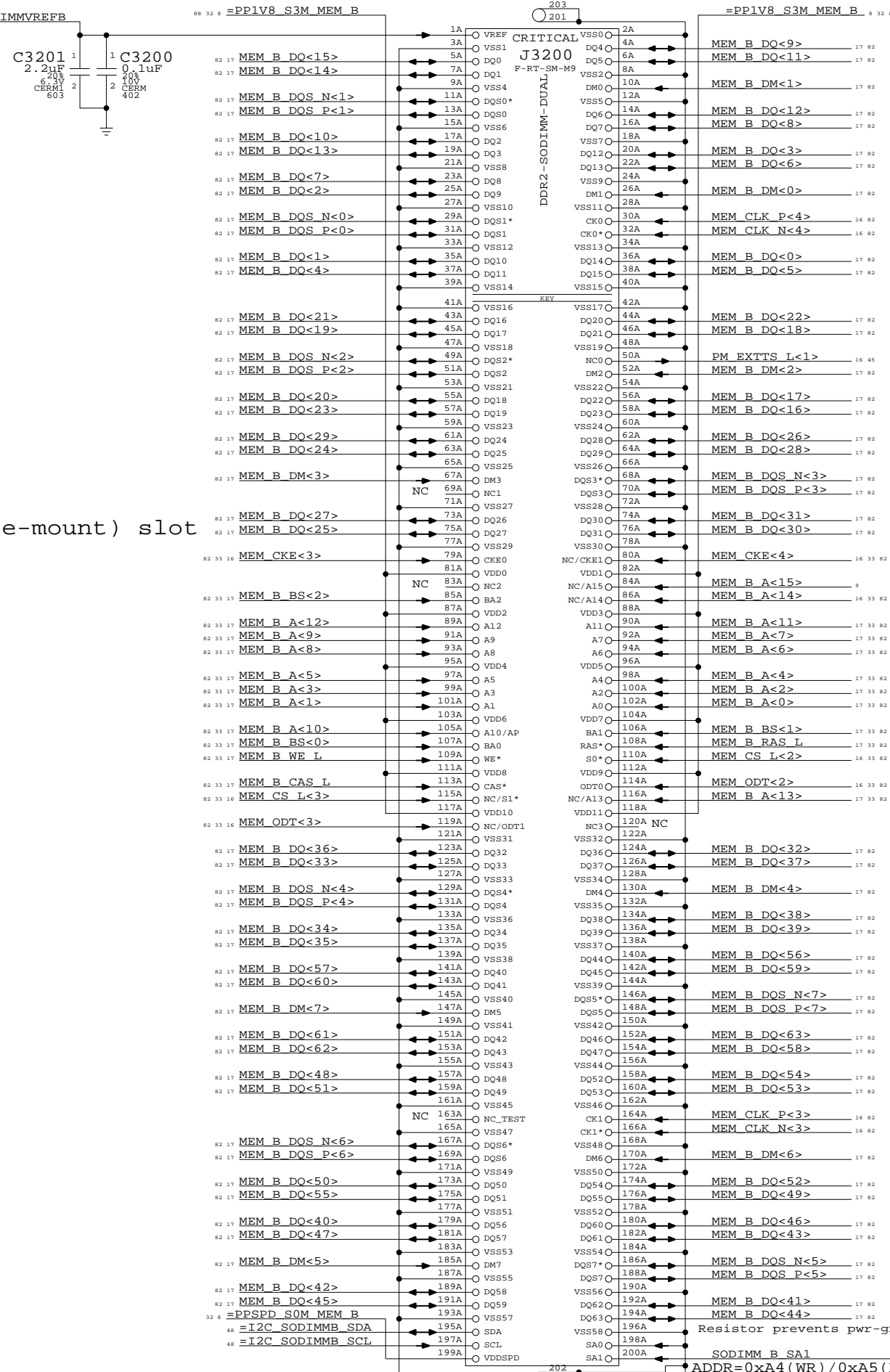
- =PP1V8\_S3M\_MEM\_B
- =PP0V9\_S3M\_MEM\_DIMMVREFB
- =PPSPD\_S0M\_MEM\_B (2.5V - 3.3V)

Signal aliases required by this page:

- =I2C\_SODIMMB\_SCL
- =I2C\_SODIMMB\_SDA

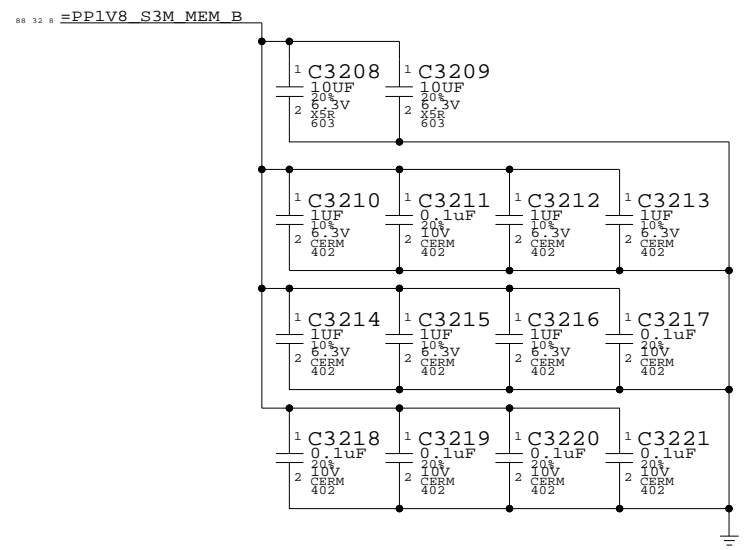
BOM options provided by this page:  
(NONE)

"Expansion" (surface-mount) slot



## DDR2 Bypass Caps

(For return current)



### DDR2 SO-DIMM Connector B

SYNC\_MASTER=(M59\_SYNC) SYNC\_DATE=08/24/2006

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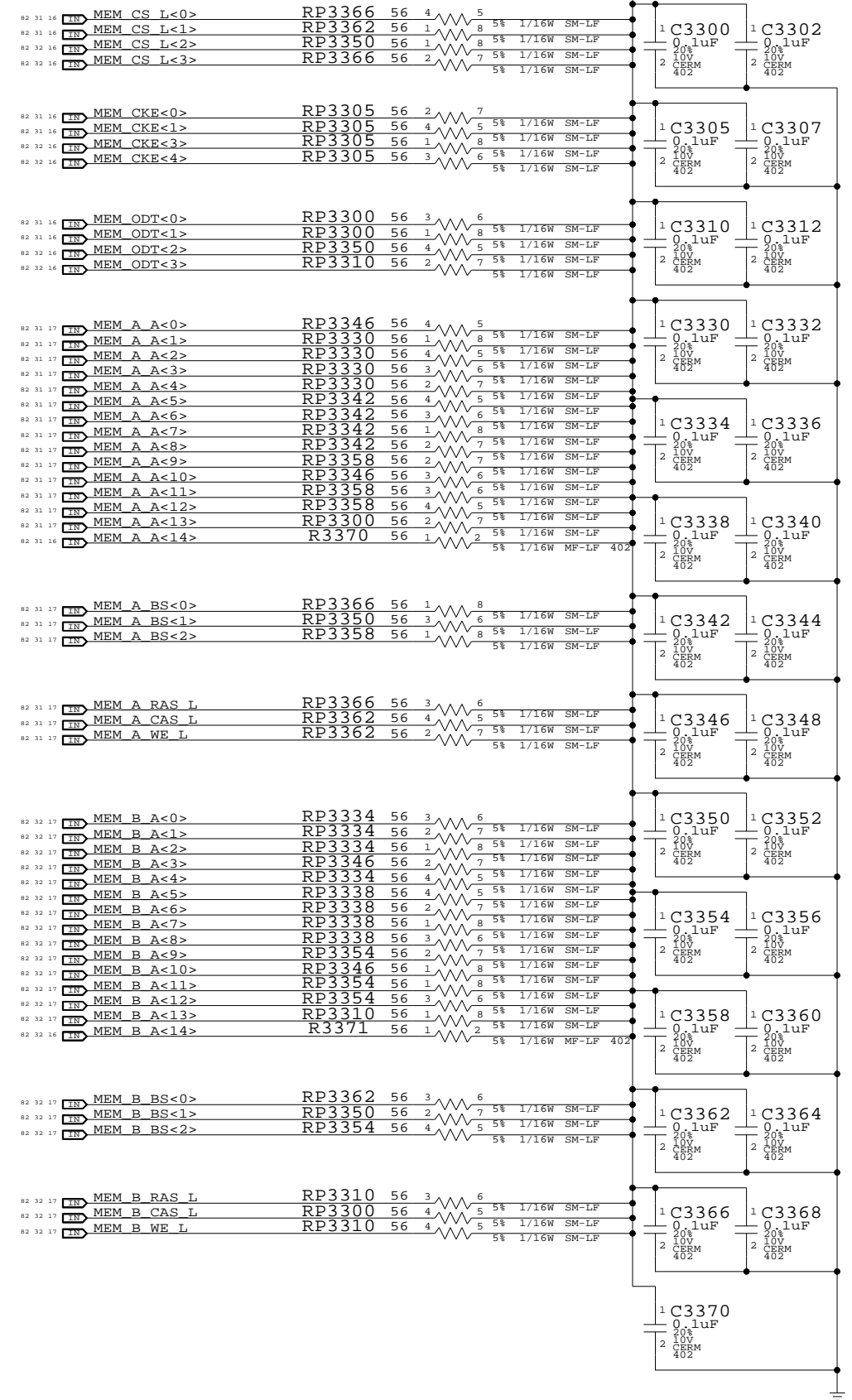
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE	SHT	OF
NONE	32	89



One cap for each side of every RPAK, one cap for every two discrete resistors  
 Ensure CS\_L and ODT resistors are close to SO-DIMM connector

=PPOV9 SOM MEM TERM



D

D

C

C

B

B

A

A

Memory Active Termination  
 SYNC\_MASTER=(T9\_NOME) SYNC\_DATE=11/14/2006

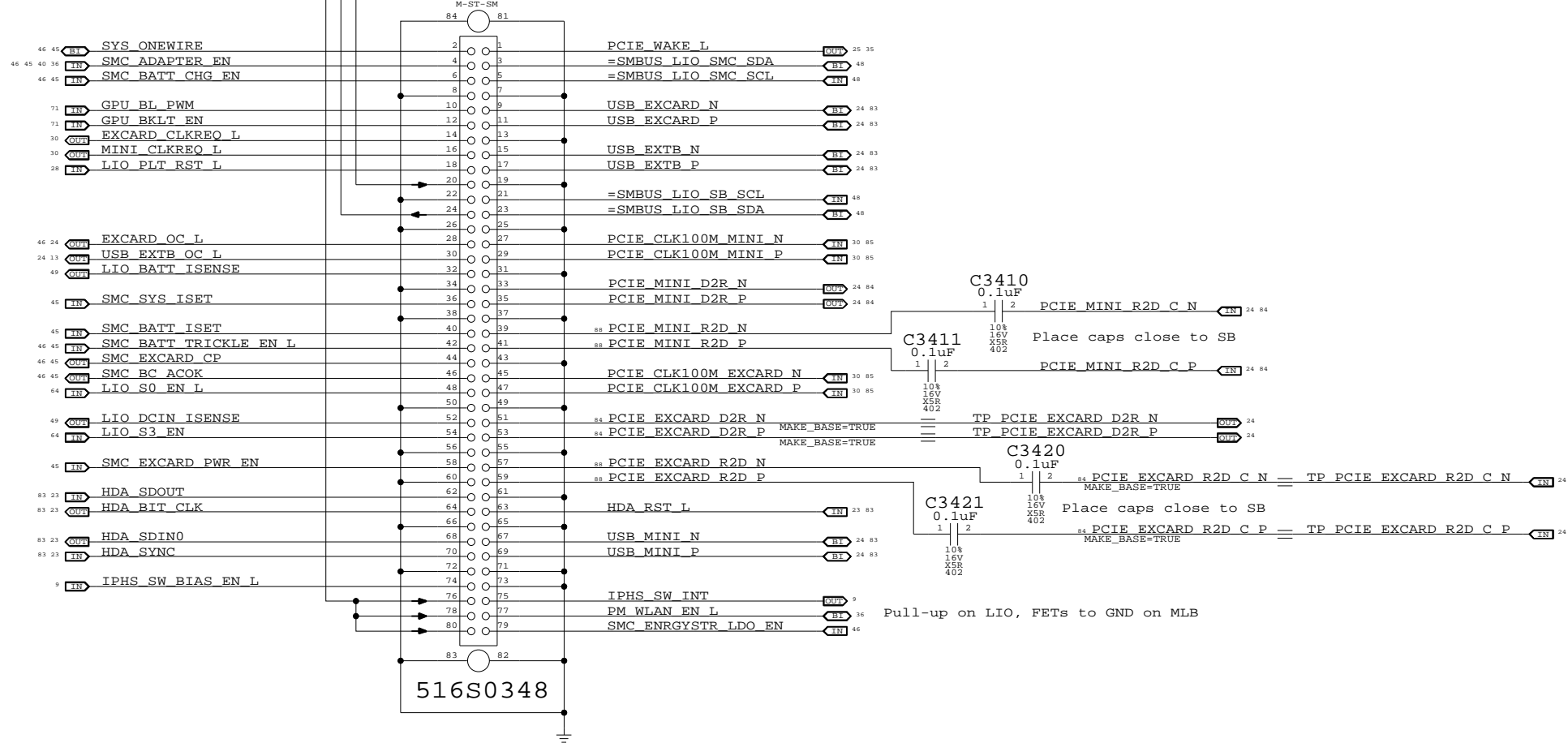
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SCALE	SHT	OF	
NONE	33	89	

# Left I/O Board Connector

(Output to LIO) =PP3V42\_G3H\_LIO  
 (Input from LIO) =PPDCIN\_G3H\_LIO\_CONN  
 (Output to LIO) =PP1V5\_S0\_LIO

CRITICAL  
**J3400**  
 QT500806-L121-9F  
 M-ST-SM



Left I/O Board Connector  
 SYNC\_MASTER=(M59\_SYNC) SYNC\_DATE=08/24/2006

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7413	11.0.0
SCALE	SHT		OF
NONE	34		89



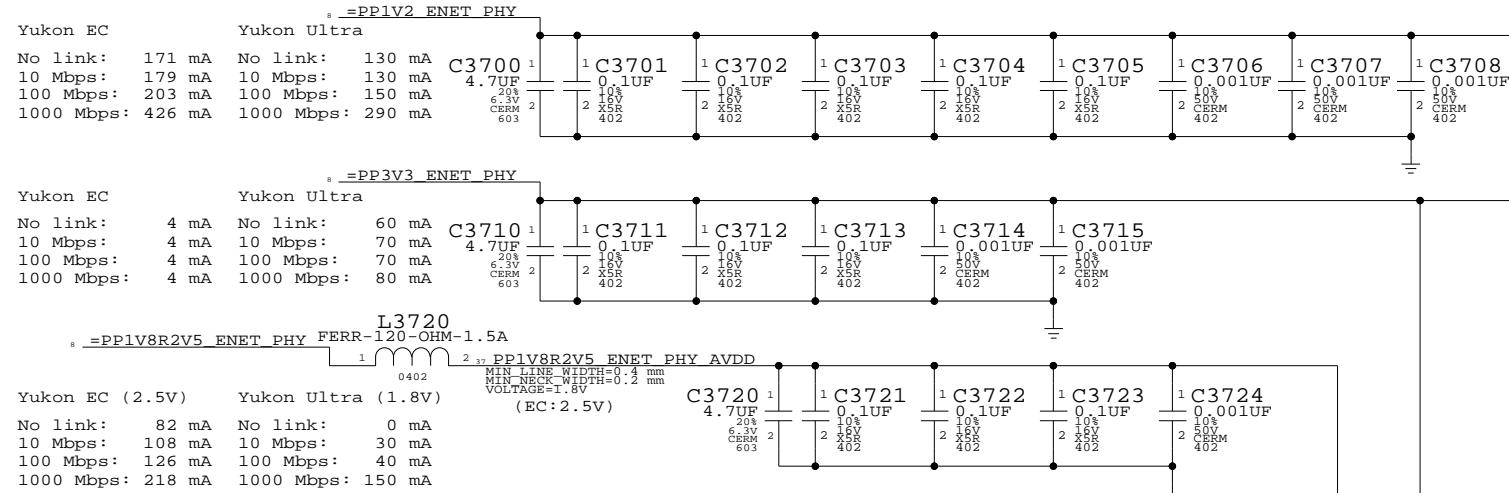
# Page Notes

Power aliases required by this page:  
 - =PP3V3\_ENET\_PHY (EC / Ultra)  
 - =PP1V8R2V5\_ENET\_PHY (2.5V / 1.8V)  
 - =YUKON\_EC\_PP2V5\_ENET (2.5V / GND)  
 - =PP1V2\_ENET\_PHY

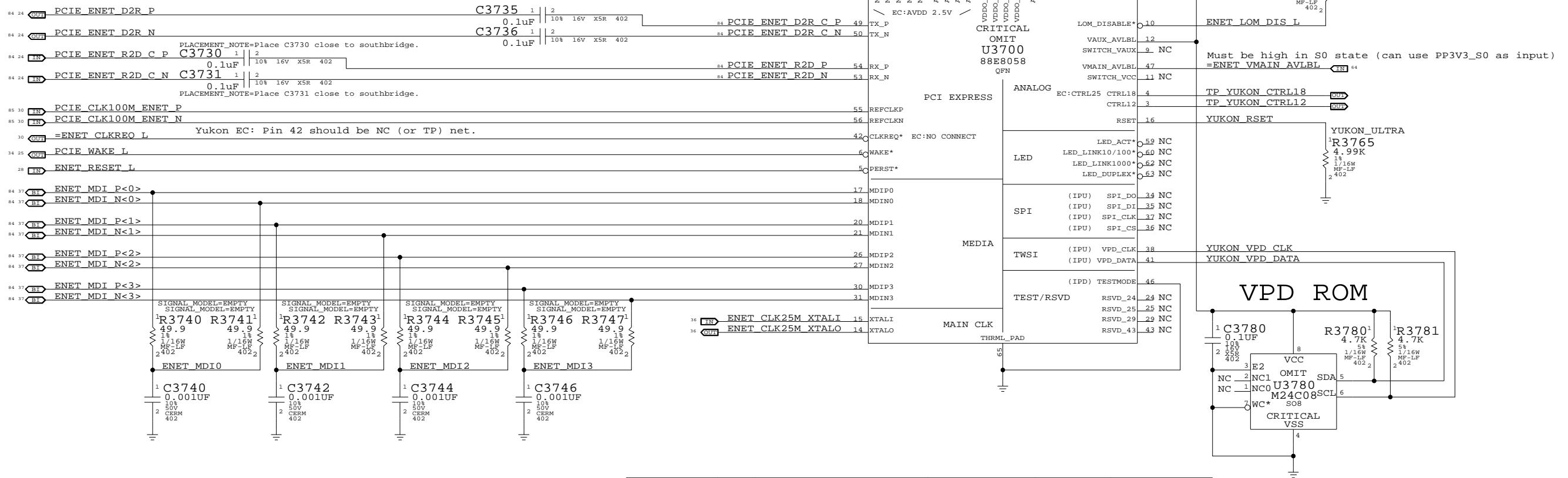
Signal aliases required by this page:  
 - =ENET\_CLKREQ\_L (NC/TP for Yukon EC)  
 - =ENET\_VMAIN\_AVLBLE (See note by pin)

BOM options provided by this page:  
 YUKON\_EC - Selects Yukon EC RSET value.  
 YUKON\_ULTRA - Selects Yukon Ultra RSET.

NOTE: See bottom of page for instructions for dual Yukon EC / Yukon Ultra schematic support.



=YUKON\_EC\_PP2V5\_ENET  
 Yukon EC: Alias to PP1V8R2V5\_ENET\_PHY\_AVDD, add 1x 0.1uF & 1x 0.001uF caps  
 Yukon Ultra: Alias to GND



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0386	1	IC, 88E8058, GIGABIT ENET XCVR, 64P QFN	U3700	CRITICAL	YUKON_ULTRA
341S2060	1	IC, FLASH, 88E8058 ETHERNET VPD, IIC, SO8	U3780	CRITICAL	YUKON_ULTRA
338S0270	1	IC, 88E8053, GIGABIT ENET XCVR, 64P QFN	U3700	CRITICAL	YUKON_EC
341S1797	1	IC, EEPROM, SERIAL IIC, 8KBIT, SO8	U3780	CRITICAL	YUKON_EC
114S0285	1	RES, 4.87K, 1%, 1/16W, 0402, LF	R3760		YUKON_EC

To support Yukon EC and Ultra on the same board:

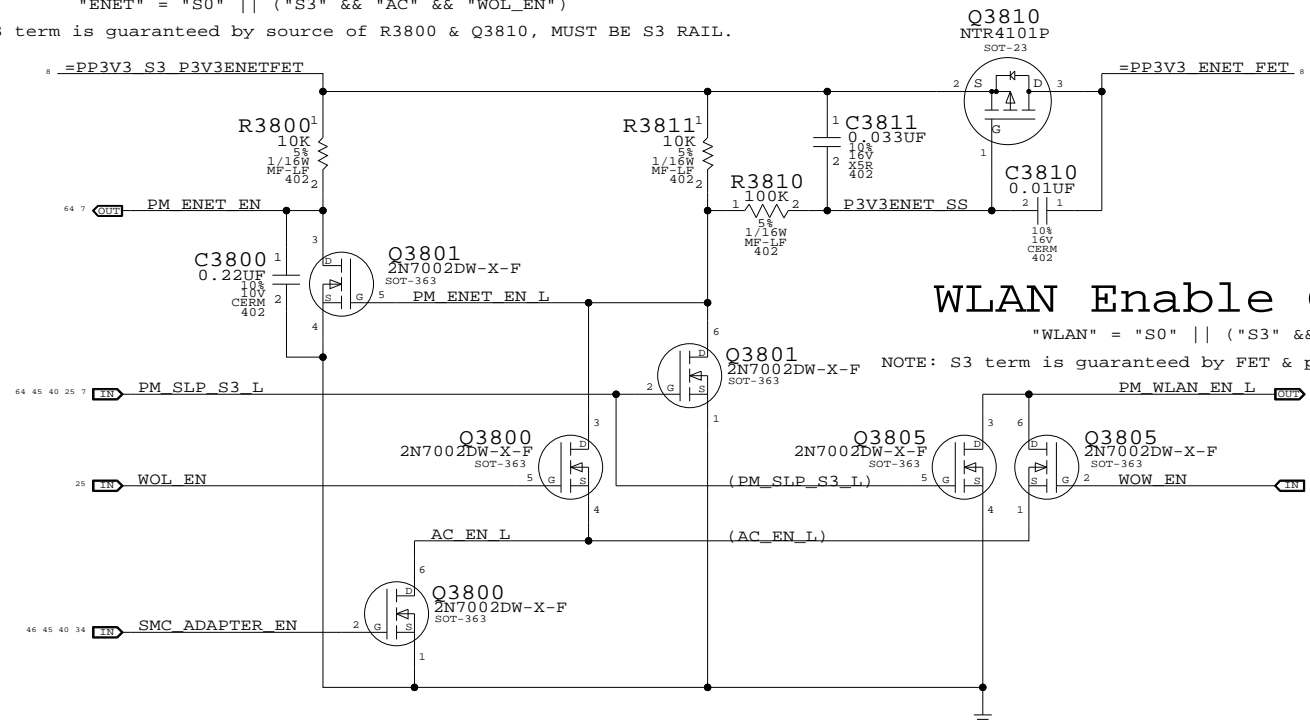
- Alias =YUKON\_EC\_PP2V5\_ENET to PP1V8R2V5\_ENET\_PHY\_AVDD, add 1x 0.1uF and 1x 0.001uF caps
- Use 0-ohm resistors or variable supply to provide 1.8V or 2.5V to =PP1V8R2V5\_ENET\_PHY and magnetics. Can also use BCP69T1 connected to CTRL18 pin 4 for internal VR.
- Connect =ENET\_CLKREQ\_L to clock generator via 0-ohm resistor (BOMOPTION: YUKON\_ULTRA)
- Use YUKON\_EC and YUKON\_ULTRA BOMOPTIONS to select stuffed part

**Ethernet (Yukon)**  
 SYNC\_MASTER=T9\_NOME SYNC\_DATE=03/16/2007  
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SCALE	SHT	OF	
NONE	35	89	

## ENET Enable Generation

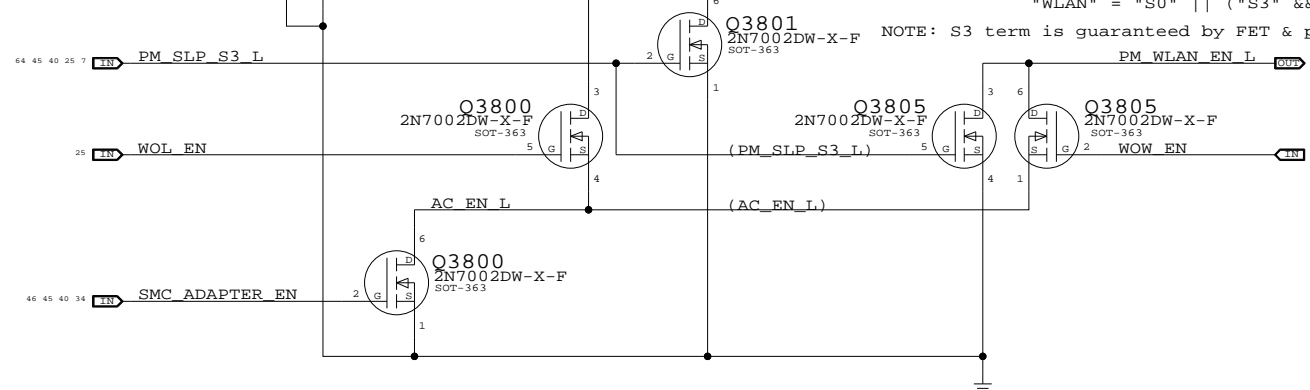
"ENET" = "S0" || ("S3" && "AC" && "WOL\_EN")  
 NOTE: S3 term is guaranteed by source of R3800 & Q3810, MUST BE S3 RAIL.



## 3.3V ENET FET

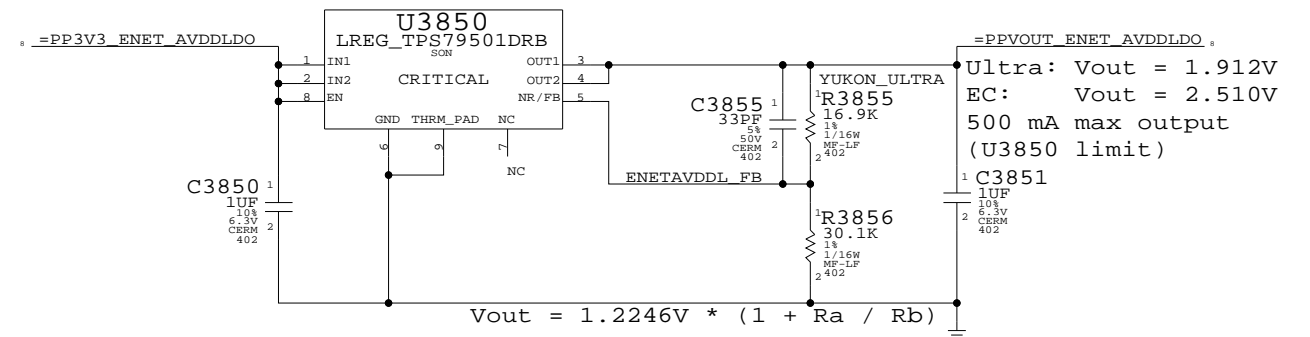
## WLAN Enable Generation

"WLAN" = "S0" || ("S3" && "AC" && "WOW\_EN")  
 NOTE: S3 term is guaranteed by FET & pull-up source, MUST BE S3 RAIL.



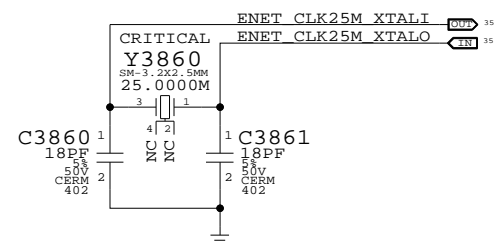
## Yukon AVDDL LDO

1.9V for Yukon Ultra, 2.5V for Yukon EC  
 Yukon Ultra requires 1.9V on its magnetics to pass compliance tests



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0363	1	RES,31.6K,1%,1/16W,402,LF	R3855		YUKON_EC

## Yukon Crystal

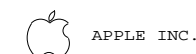


## Yukon Power Control

SYNC\_MASTER=T9\_NOME SYNC\_DATE=03/16/2007

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE	SHT	OF
NONE	36	89

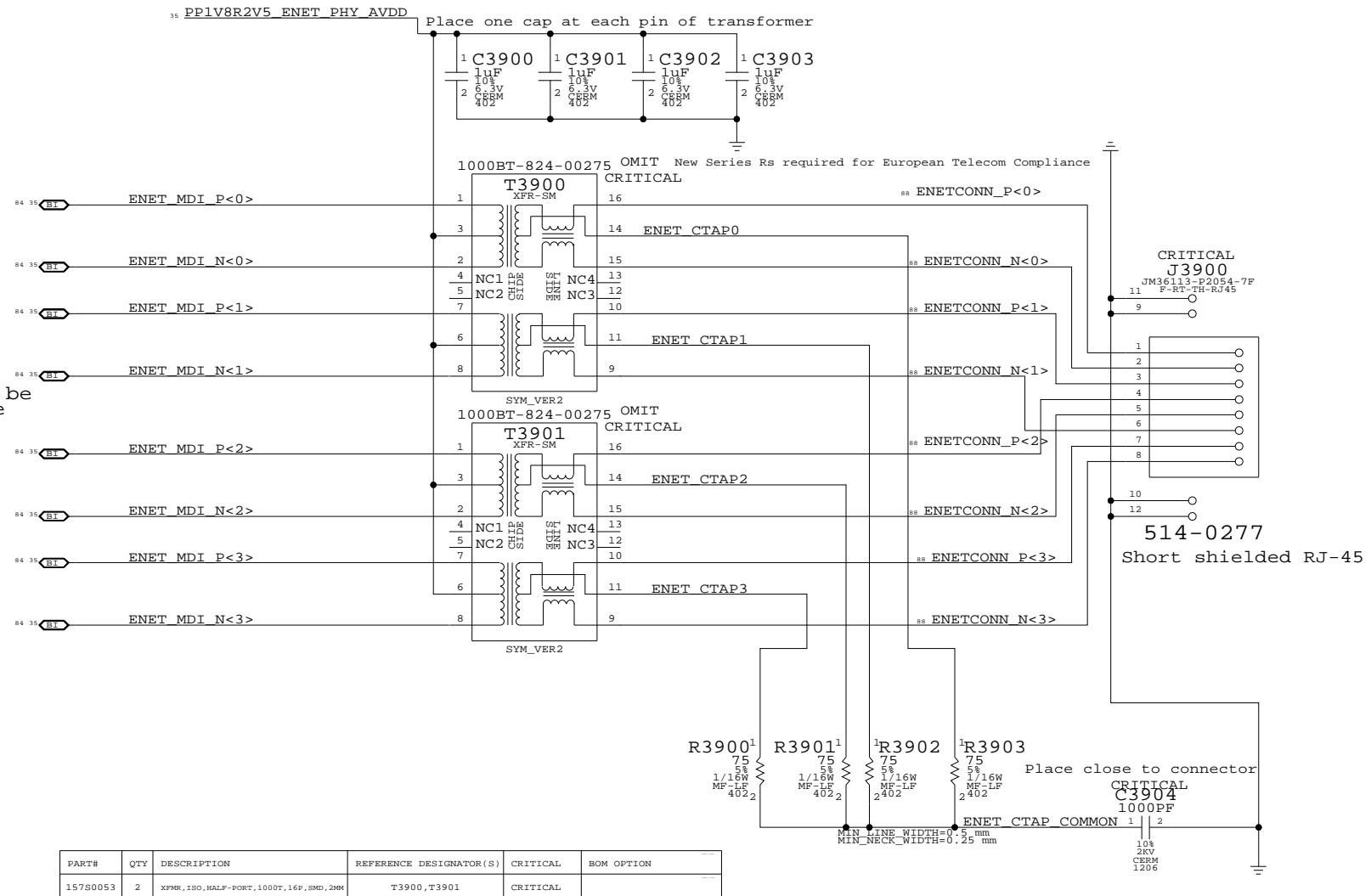
# Page Notes

Power aliases required by this page:  
 - =GND\_CHASSIS\_ENET

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 (NONE)

Transformers should be mirrored on opposite sides of the board



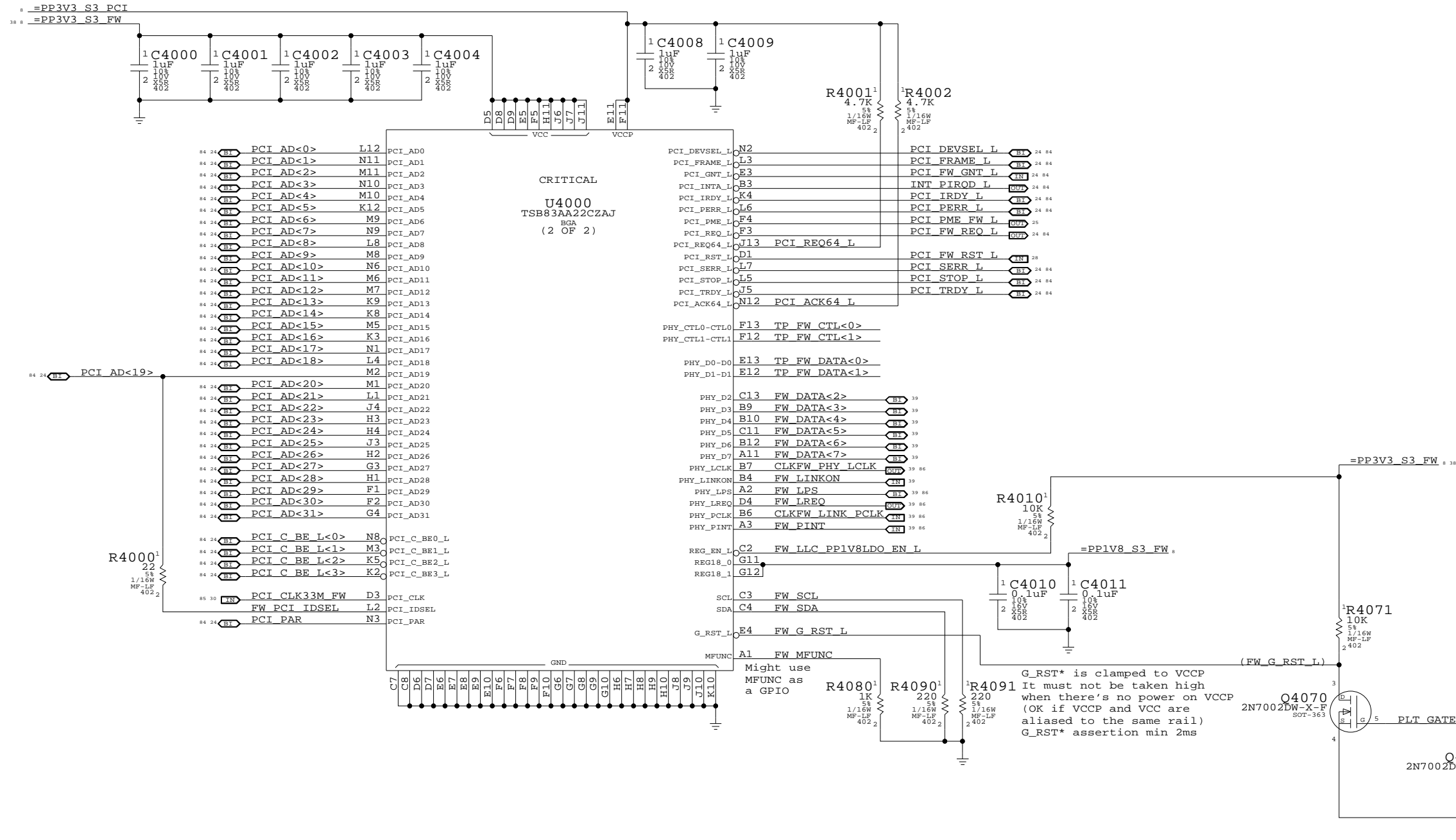
**Ethernet Connector**  
 SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/19/2007

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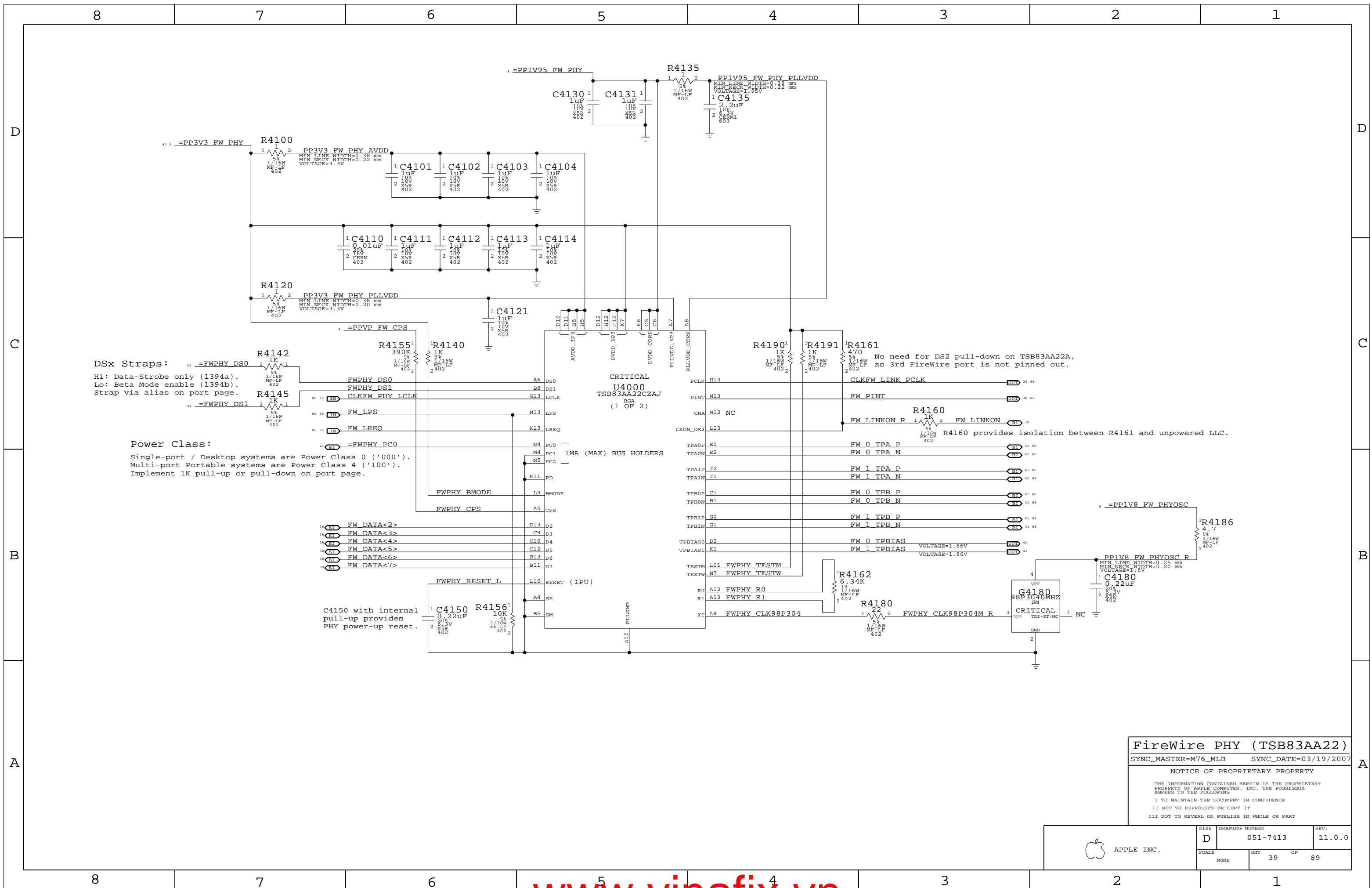
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7413	11.0.0
SCALE	SHT	OF	
NONE	37	89	



FireWire Link (TSB83AA22)  
 SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/19/2007

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	D	051-7413	11.0.0
SCALE	SHT 38 OF 89		
NONE			



**DSx Straps:**

Hi: Data-Strobe only (1394a).  
 Lo: Beta Mode enable (1394b).  
 Strap via alias on port page.

**Power Class:**

Single-port / Desktop systems are Power Class 0 ('000').  
 Multi-port Portable systems are Power Class 4 ('100').  
 Implement 1K pull-up or pull-down on port page.

No need for DS2 pull-down on TSB83AA22A,  
 as 3rd FireWire port is not pinned out.

R4160 provides isolation between R4161 and unpowered LLC.

**FireWire PHY (TSB83AA22)**  
 SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/19/2007

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7413	11.0.0
SCALE	SHT	OF	REV.
NONE	39	89	

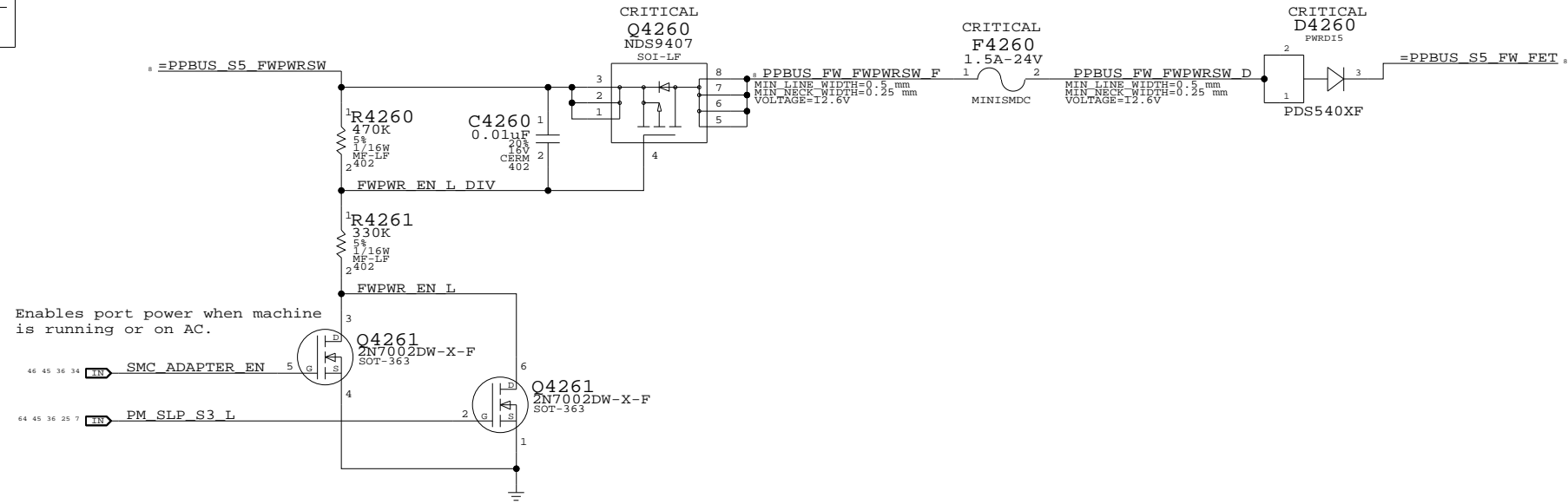
# Page Notes

Power aliases required by this page:  
 - =PPBUS\_S5\_FWPWSW (system supply for bus power)  
 - =PP3V3\_FW\_LATEVG\_ACTIVE  
 - =PPVP\_FW\_SUMNODE (power passthru summation node)

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 - FW\_PORT\_FAULT\_PU

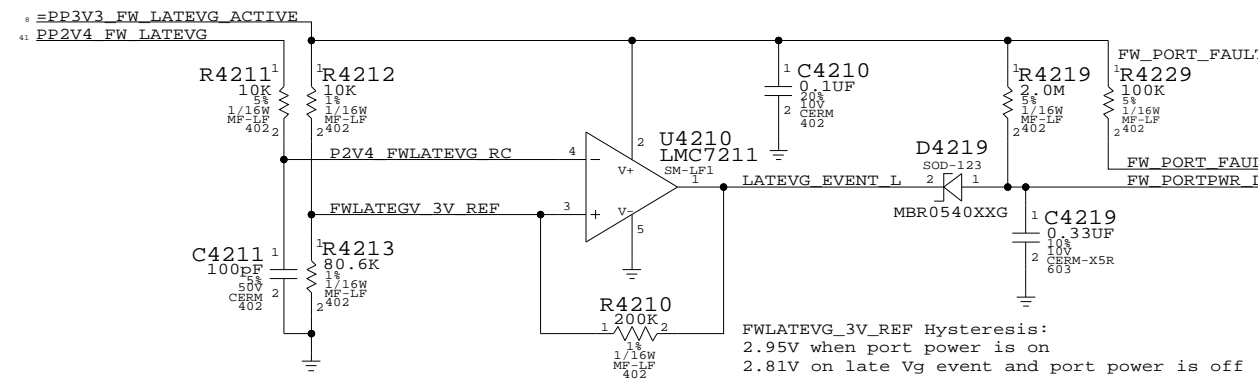
## FireWire Port Power Switch



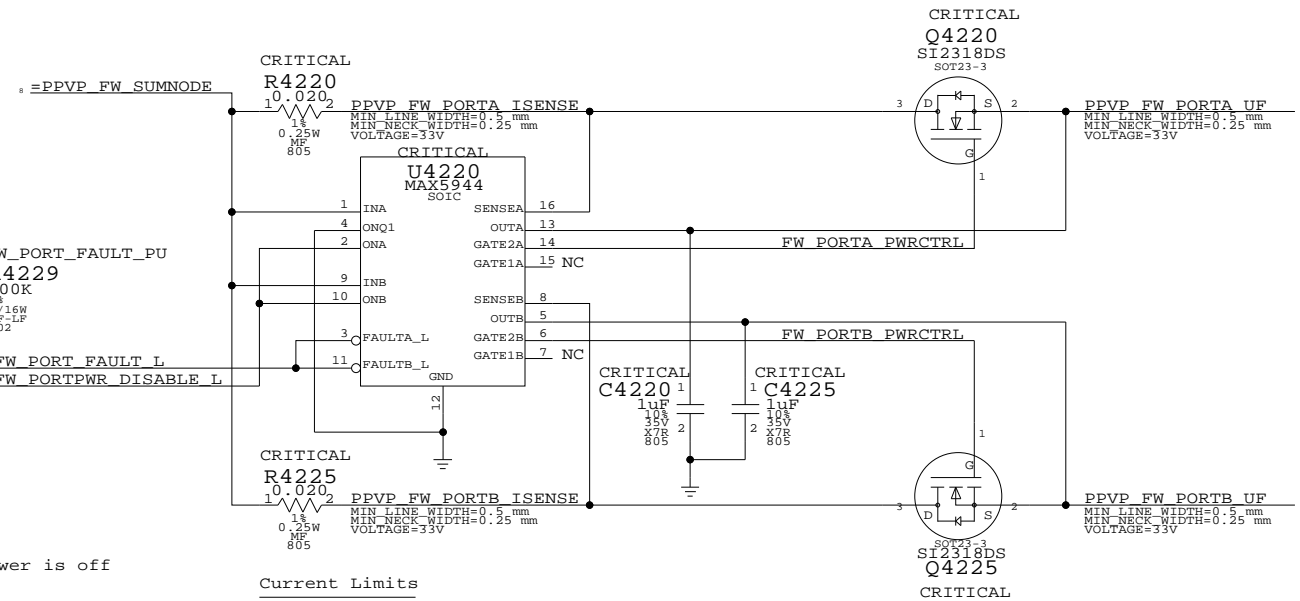
Enables port power when machine is running or on AC.

## Current Limit/Active Late-VG Protection

### Late-VG Event Detection



FWLATEVG\_3V\_REF Hysteresis:  
 2.95V when port power is on  
 2.81V on late Vg event and port power is off



Current Limits  
 0.020 ohm => 2.4A  
 0.025 ohm => 2A  
 0.030 ohm => 1.66A (Ideal)  
 0.033 ohm => 1.5A

MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

### FireWire Port Power

SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/19/2007

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	D	051-7413	11.0.0
SCALE	SHT	OF	REV.
NONE	40	89	



# Page Notes

Power aliases required by this page:  
 - =PPVP\_FW\_PORT0  
 - =PPVP\_FW\_PORT1  
 - =PP3V3\_FW\_LATEVG  
 - =GND\_CHASSIS\_FW\_PORT0L  
 - =GND\_CHASSIS\_FW\_PORT0U  
 - =GND\_CHASSIS\_FW\_PORT1  
 - =GND\_CHASSIS\_FW\_PORT1R

Signal aliases required by this page:  
 (NONE)  
 NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:  
 (NONE)  
 NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

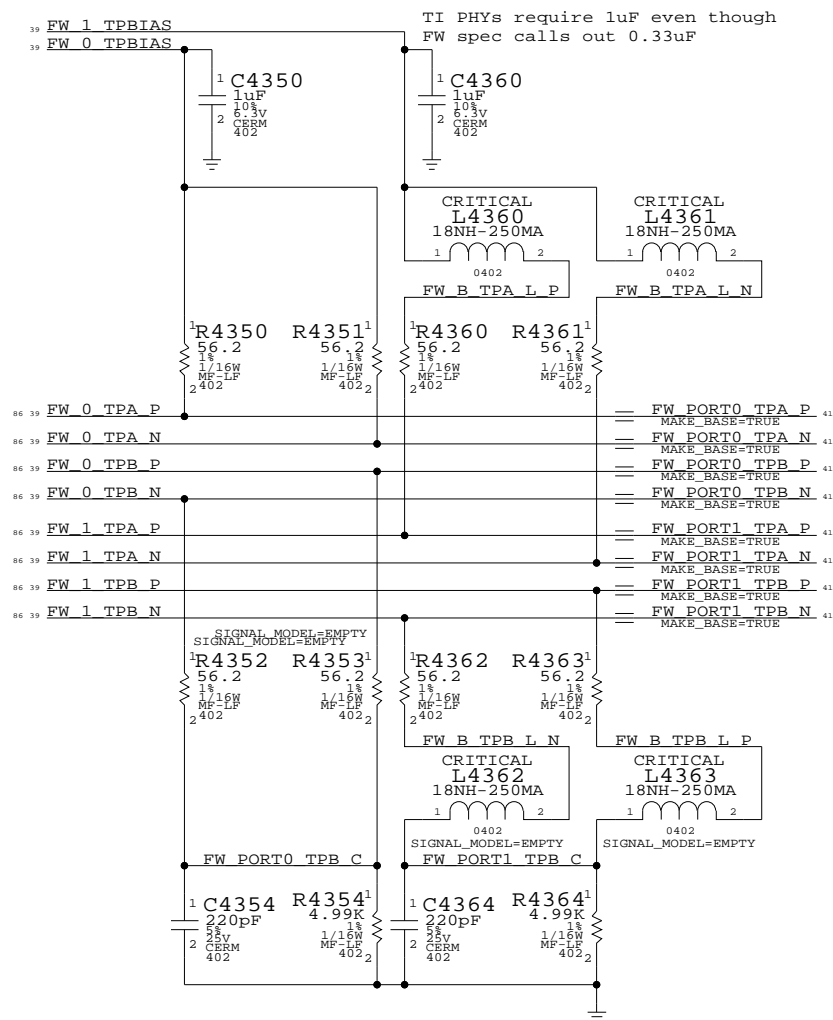
## FireWire PHY Config Straps

Configures PHY for:

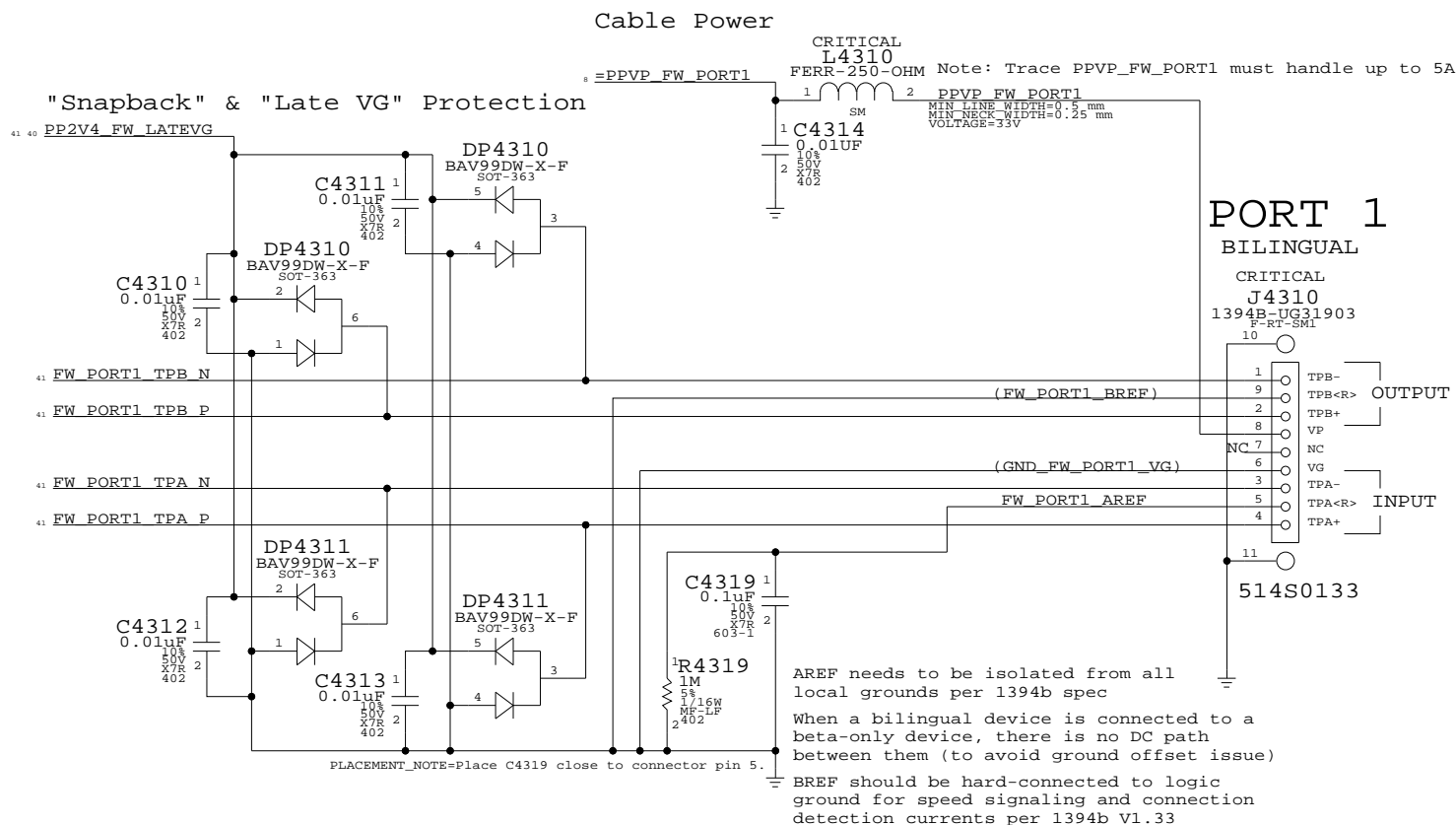
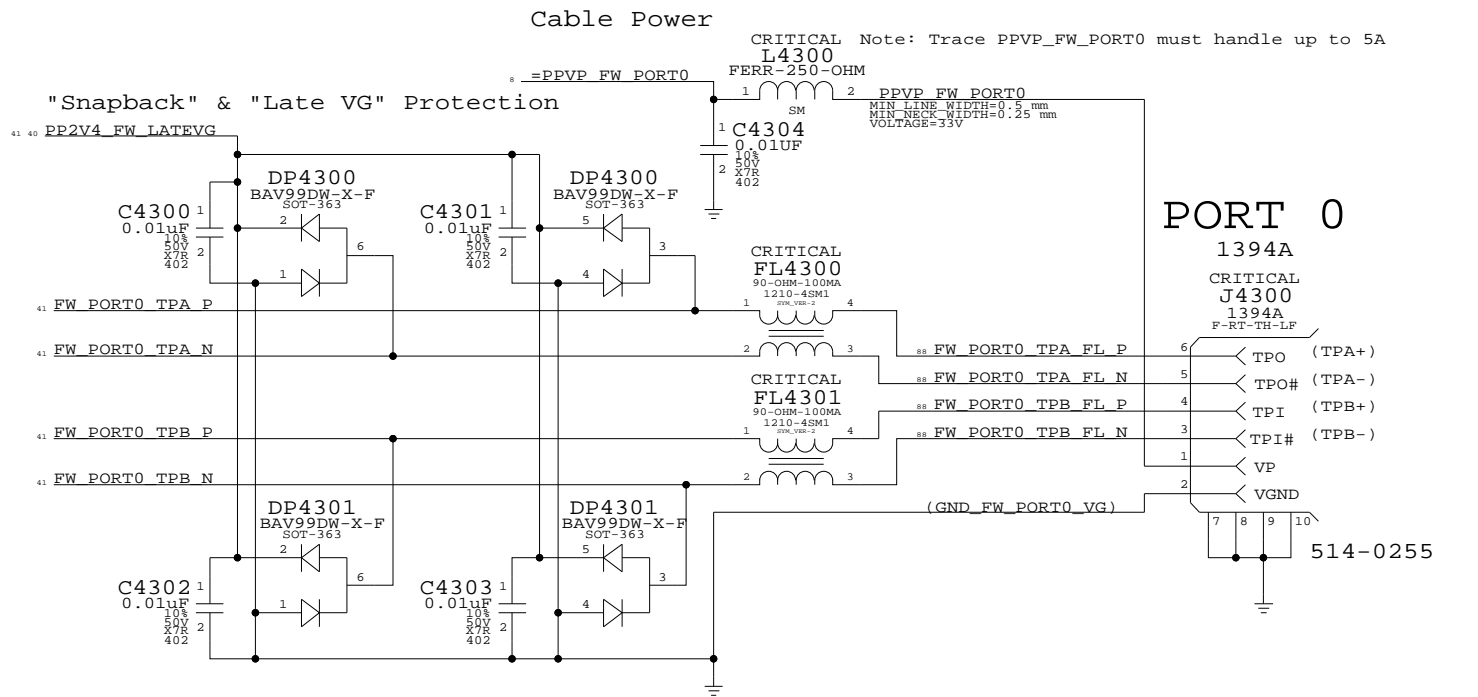
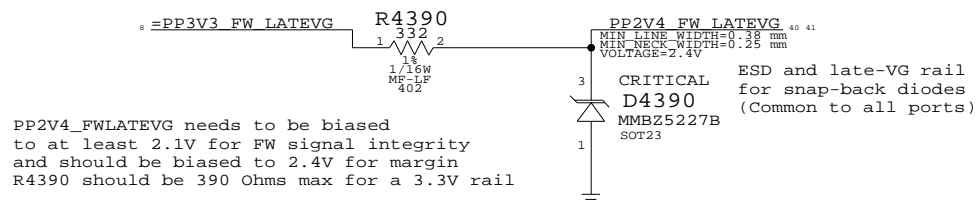
- 2-port Portable Power Class (4) =PP3V3\_FW\_PHY
- Port "0" Data-Strobe only (1394A) =FWPHY\_PC0
- Port "1" Bilingual (1394B) =FWPHY\_DS1

## Termination

Place close to FireWire PHY



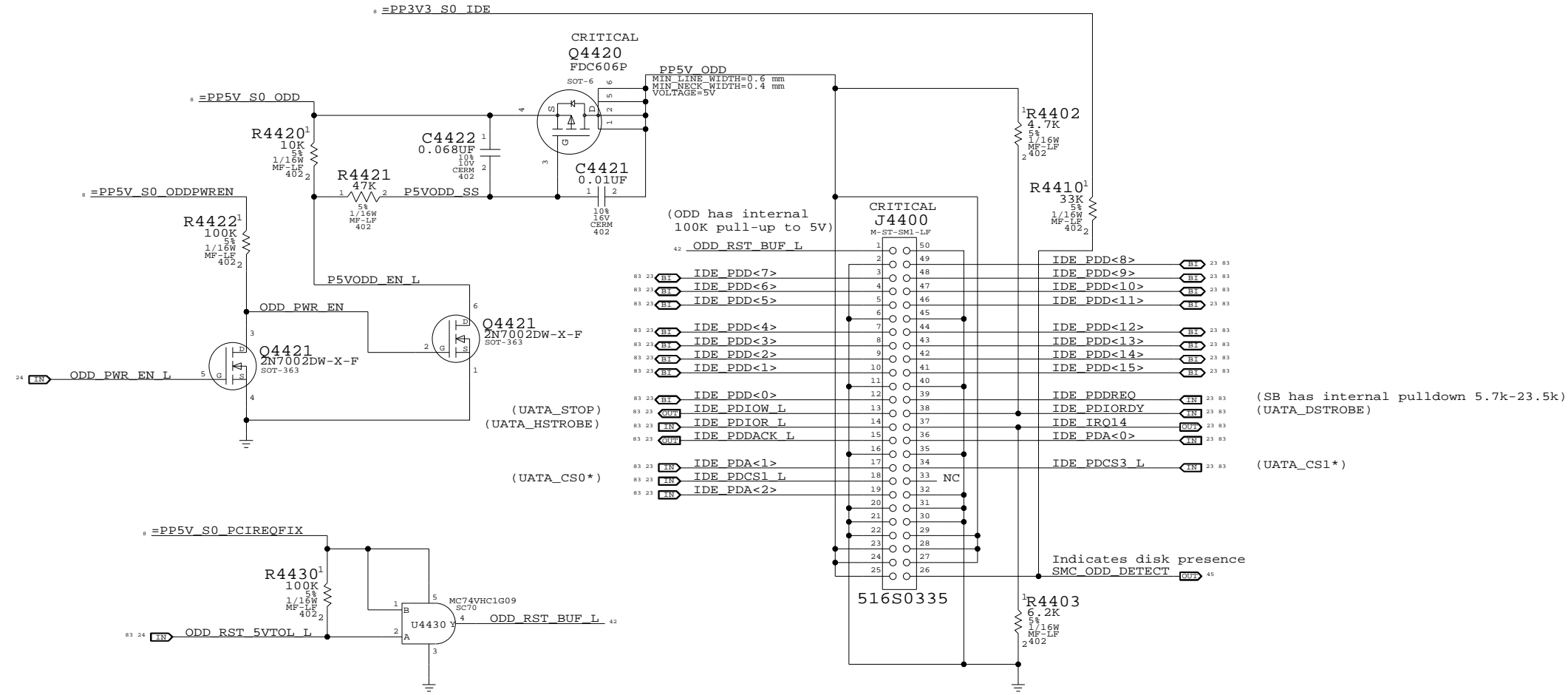
## Late-VG Protection Power



FireWire Ports		
SYNC_MASTER=M76_MLB	SYNC_DATE=03/19/2007	
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	D	051-7413	11.0.0
SCALE	SHT	OF	REV.
NONE	41	89	

# IDE (ODD) Connector

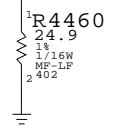


## Unused SATA Ports

- 23  SATA B R2D C P == TP SATA B R2DP  
MAKE\_BASE=TRUE
- 23  SATA B R2D C N == TP SATA B R2DN  
MAKE\_BASE=TRUE
- 23  SATA B D2R P == TP SATA B D2RP  
MAKE\_BASE=TRUE
- 23  SATA B D2R N == TP SATA B D2RN  
MAKE\_BASE=TRUE
- 23  SATA C R2D C P == TP SATA C R2DP  
MAKE\_BASE=TRUE
- 23  SATA C R2D C N == TP SATA C R2DN  
MAKE\_BASE=TRUE
- 23  SATA C D2R P == TP SATA C D2RP  
MAKE\_BASE=TRUE
- 23  SATA C D2R N == TP SATA C D2RN  
MAKE\_BASE=TRUE

- 23  SATA RBIAS P == SATA RBIAS  
MAKE\_BASE=TRUE
- 23  SATA RBIAS N ==

Placement note  
Place within 12.7mm  
from ball of SB



**PATA Connector**

SYNC\_MASTER=(MASTER)      SYNC\_DATE=(MASTER)

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SCALE	SHT	OF	REV.
NONE	42	89	

D

D

C

C

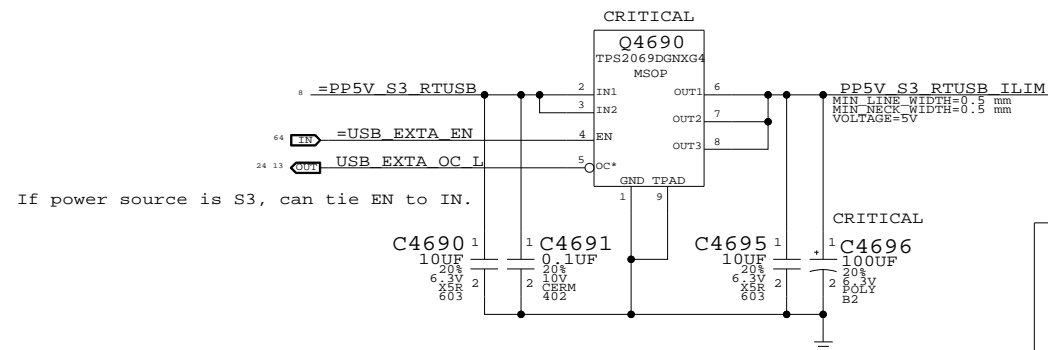
B

B

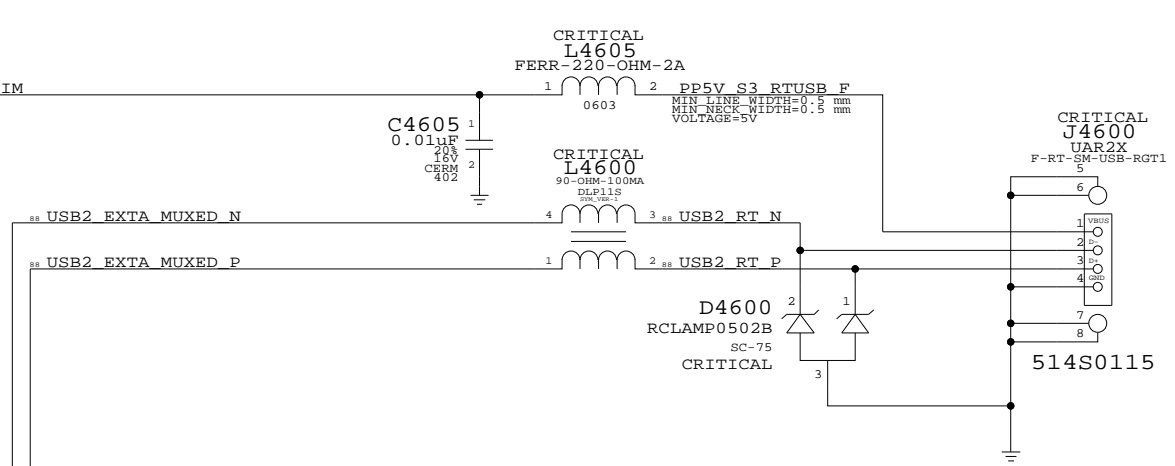
A

A

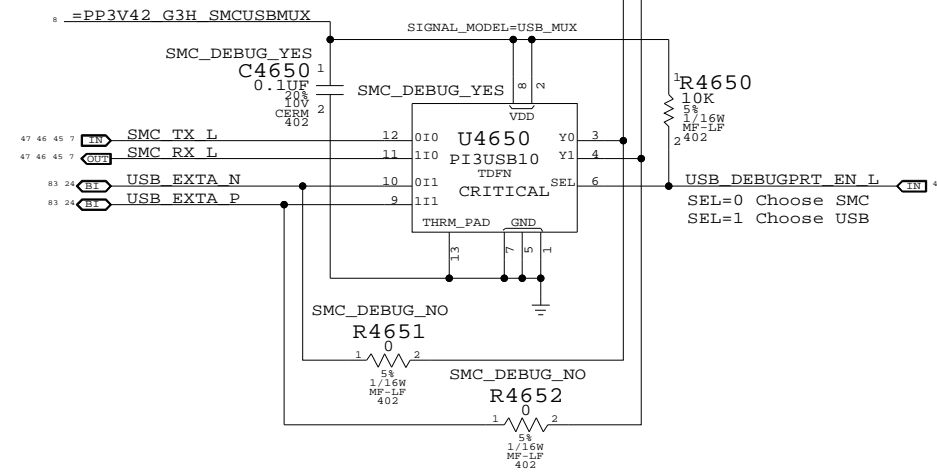
### Port Power Switch



### Right USB Port



### USB/SMC Debug Mux



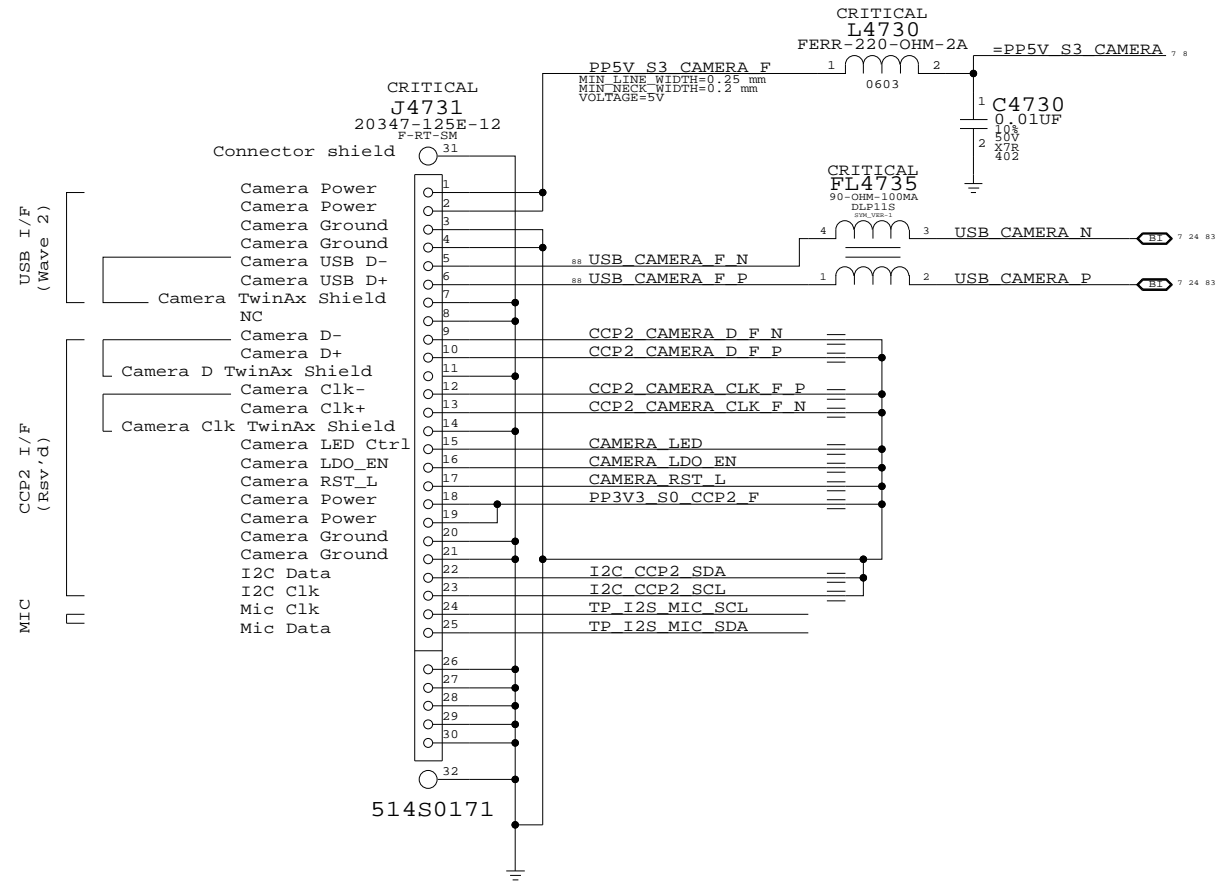
### External USB Connector

SYNC\_MASTER=M88 SYNC\_DATE=08/02/2007

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	D	051-7413	11.0.0
SCALE	SHT	OF	
NONE	43	89	

# Left Clutch Barrel Interconnect



Left Clutch Barrel Interconnect  
 SYNC\_MASTER=M87 SYNC\_DATE=07/16/2007

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	D	051-7413	11.0.0
SCALE	SHT	OF	
NONE	44	89	

NOTE: Unused pins have "SMC\_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

D

C

B

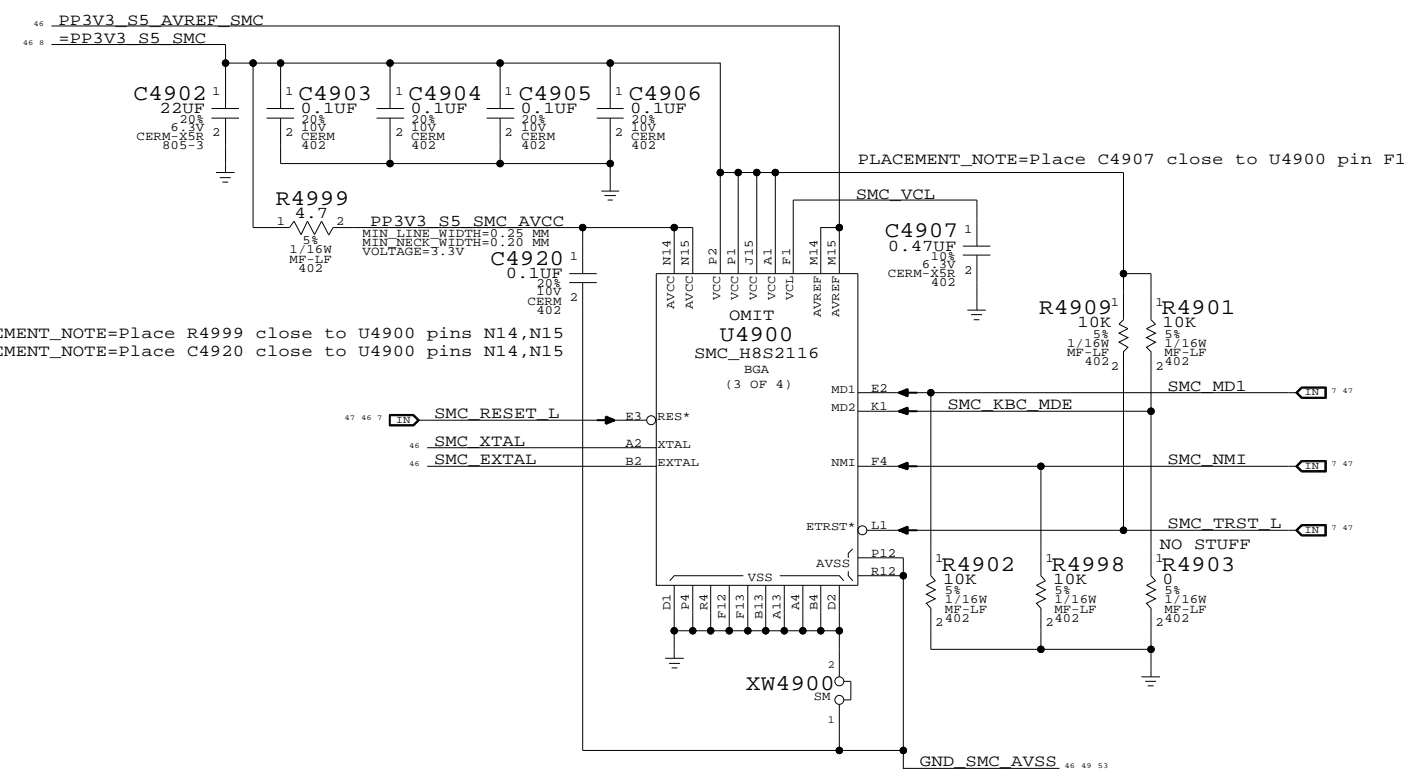
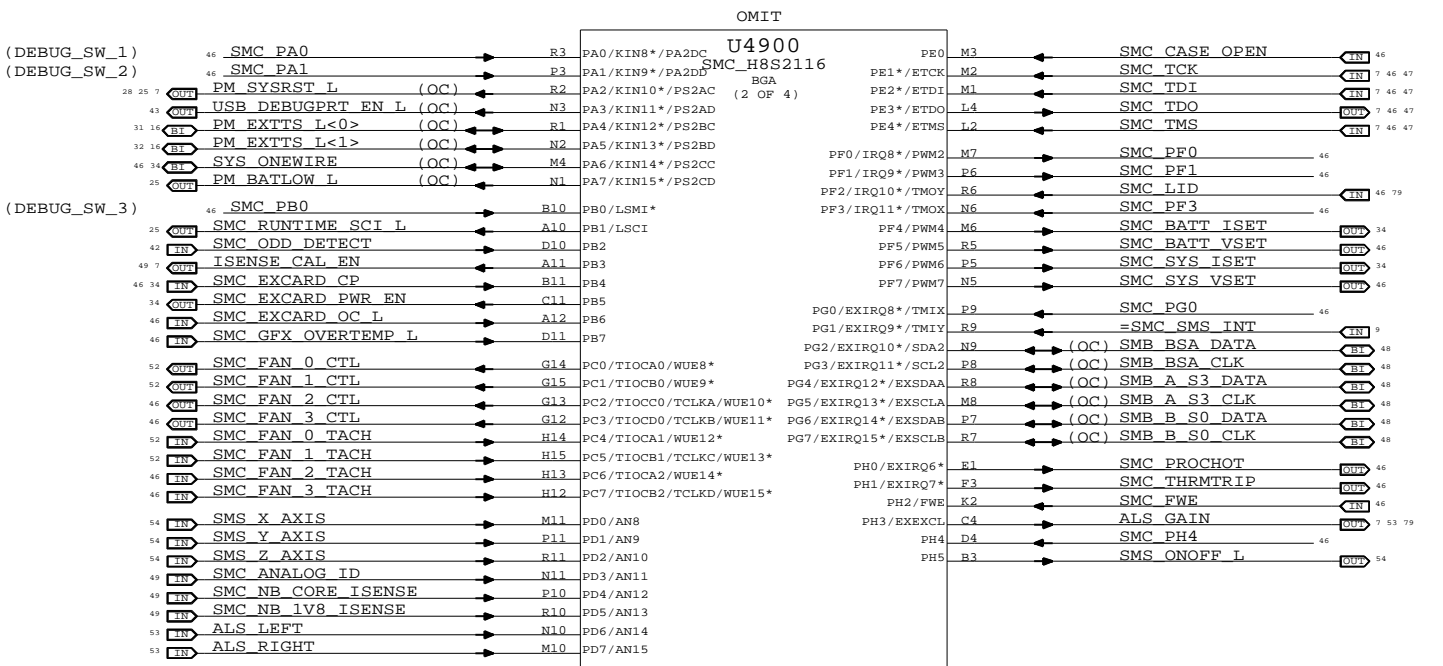
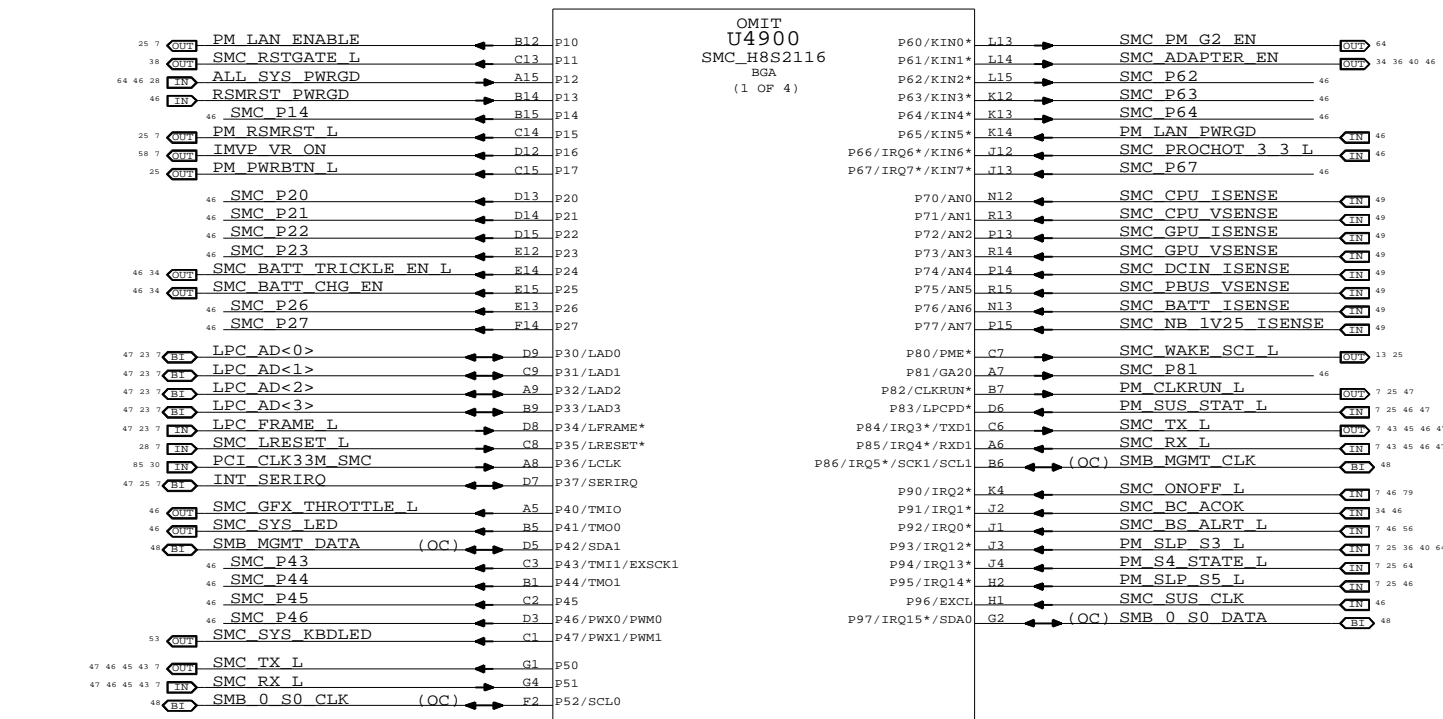
A

D

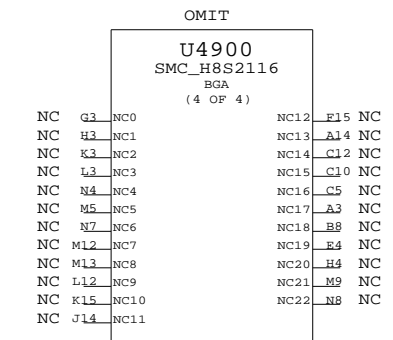
C

B

A



NOTE: SMS Interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.

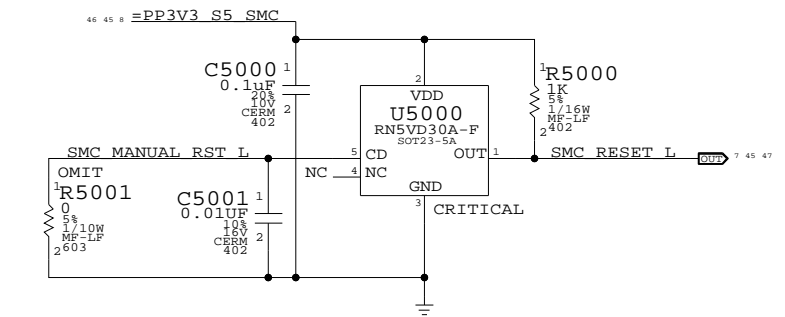


SMC  
 SYNC\_MASTER=T9\_NOME SYNC\_DATE=01/17/2007  
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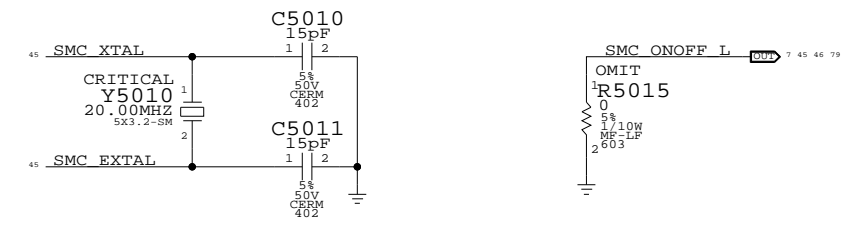
APPLE INC.	SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF	
NONE	45	89	



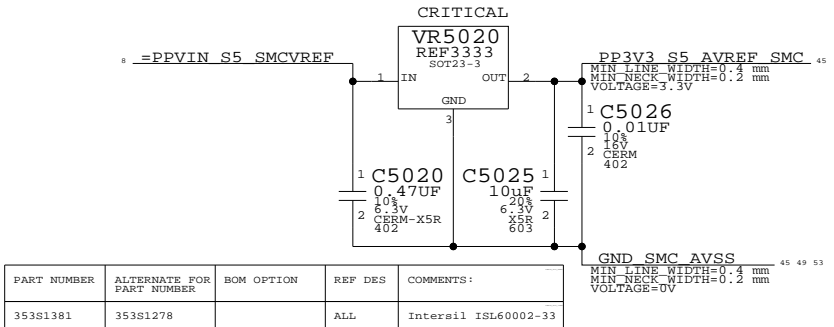
SMC Reset "Button" / Brownout Detect



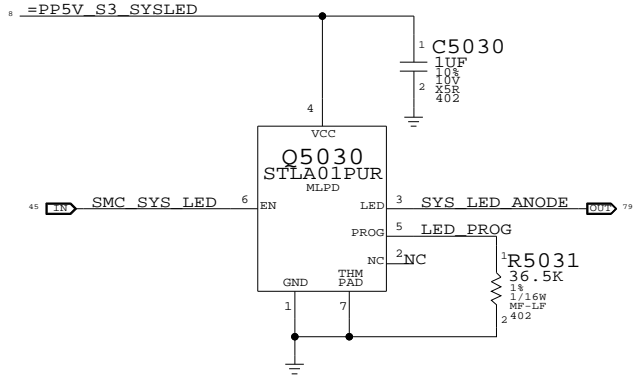
SMC Crystal Circuit Debug Power "Button"



SMC AVREF Supply

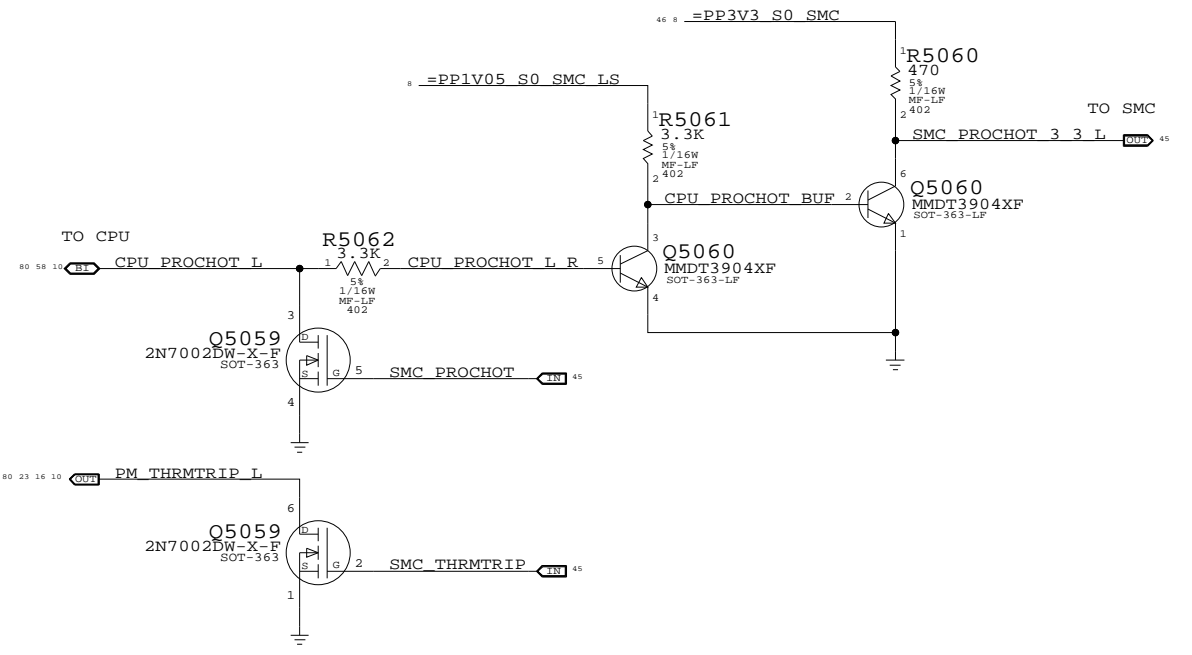


System (Sleep) LED Circuit



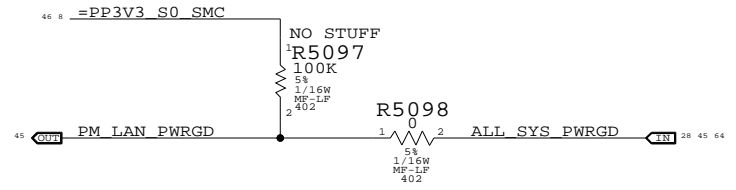
- SMC FAN 2 CTL == TP\_SMC\_FAN\_2\_CTL
- SMC FAN 2 TACH == TP\_SMC\_FAN\_2\_TACH
- SMC FAN 3 CTL == TP\_SMC\_FAN\_3\_CTL
- SMC FAN 3 TACH == TP\_SMC\_FAN\_3\_TACH
- SMC GFX OVERTEMP L == TP\_SMC\_GFX\_OVERTEMP\_L
- SMC GFX THROTTLE L == TP\_SMC\_GFX\_THROTTLE\_L
- SMC BATT VSET == TP\_SMC\_BATT\_VSET
- SMC SYS VSET == TP\_SMC\_SYS\_VSET
- SMC\_P14 == TP\_SMC\_P14
- SMC\_P20 == TP\_SMC\_P20
- SMC\_P21 == TP\_SMC\_P21
- SMC\_P22 == TP\_SMC\_P22
- SMC\_P23 == TP\_SMC\_P23
- SMC\_P26 == TP\_SMC\_P26
- SMC\_P27 == TP\_SMC\_P27
- SMC\_P43 == TP\_SMC\_P43
- SMC\_P44 == TP\_SMC\_P44
- SMC\_P46 == TP\_SMC\_P46
- SMC\_P62 == TP\_SMC\_P62
- SMC\_P63 == TP\_SMC\_P63
- SMC\_P64 == TP\_SMC\_P64
- SMC\_P81 == TP\_SMC\_P81
- SMC\_PFO == TP\_SMC\_PFO
- SMC\_PF1 == TP\_SMC\_PF1

SMC FSB to 3.3V Level Shifting

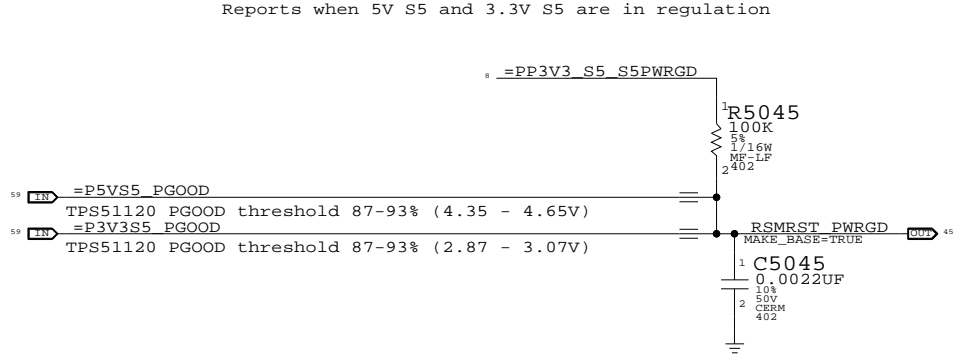


- SMC\_EXCARD\_OC\_L == EXCARD\_OC\_L
- SMC\_SUS\_CLK == SUS\_CLK\_SB
- SMC\_P45 == SMC\_ENRGYSTR\_LDO\_EN

LAN PWRGD Circuit



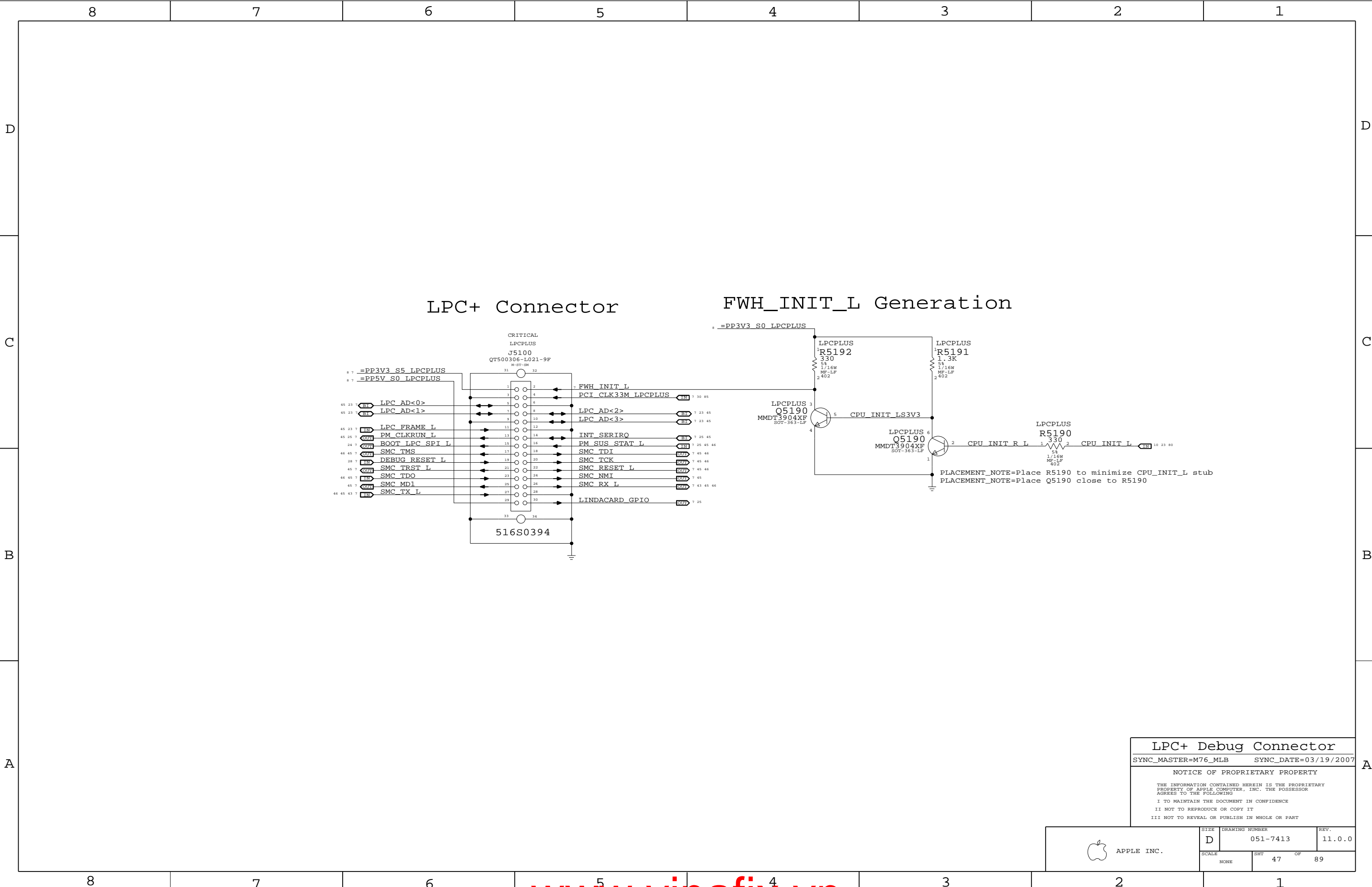
S5 Rail PWRGD Circuit



- SMC\_PA0 == R5091 100K
- SMC\_PA1 == R5092 100K
- SMC\_PB0 == R5093 100K
- SMC\_ONOFF\_L == R5070 10K
- SMC\_LID == R5071 100K
- SMC\_FWE == R5072 10K
- SMC\_TX\_L == R5073 10K
- SMC\_RX\_L == R5074 100K
- SMC\_BS\_ALRT\_L == R5076 100K
- SMC\_TMS == R5077 10K
- SMC\_TDO == R5078 10K
- SMC\_TDI == R5079 10K
- SMC\_TCK == R5080 10K
- SMC\_P67 == R5094 10K
- SMC\_P63 == R5081 10K
- SMC\_P60 == R5096 10K
- SMC\_PH4 == R5082 10K
- SMC\_BATT\_TRICKLE\_EN\_L == R5083 10K
- SMC\_BATT\_CHG\_EN == R5084 10K
- SMC\_ADAPTER\_EN == R5085 10K
- SMC\_CASE\_OPEN == R5086 10K
- SMC\_BC\_ACOK == R5087 470K
- SMC\_EXCARD\_CP == R5088 10K
- PM\_SUS\_STAT\_L == R5089 100K
- PM\_SLP\_S5\_L == R5090 100K

**SMC Support**  
 SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)  
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7413	11.0.0
SCALE	SHT	OF	
NONE	46	89	



LPC+ Connector

FWH\_INIT\_L Generation

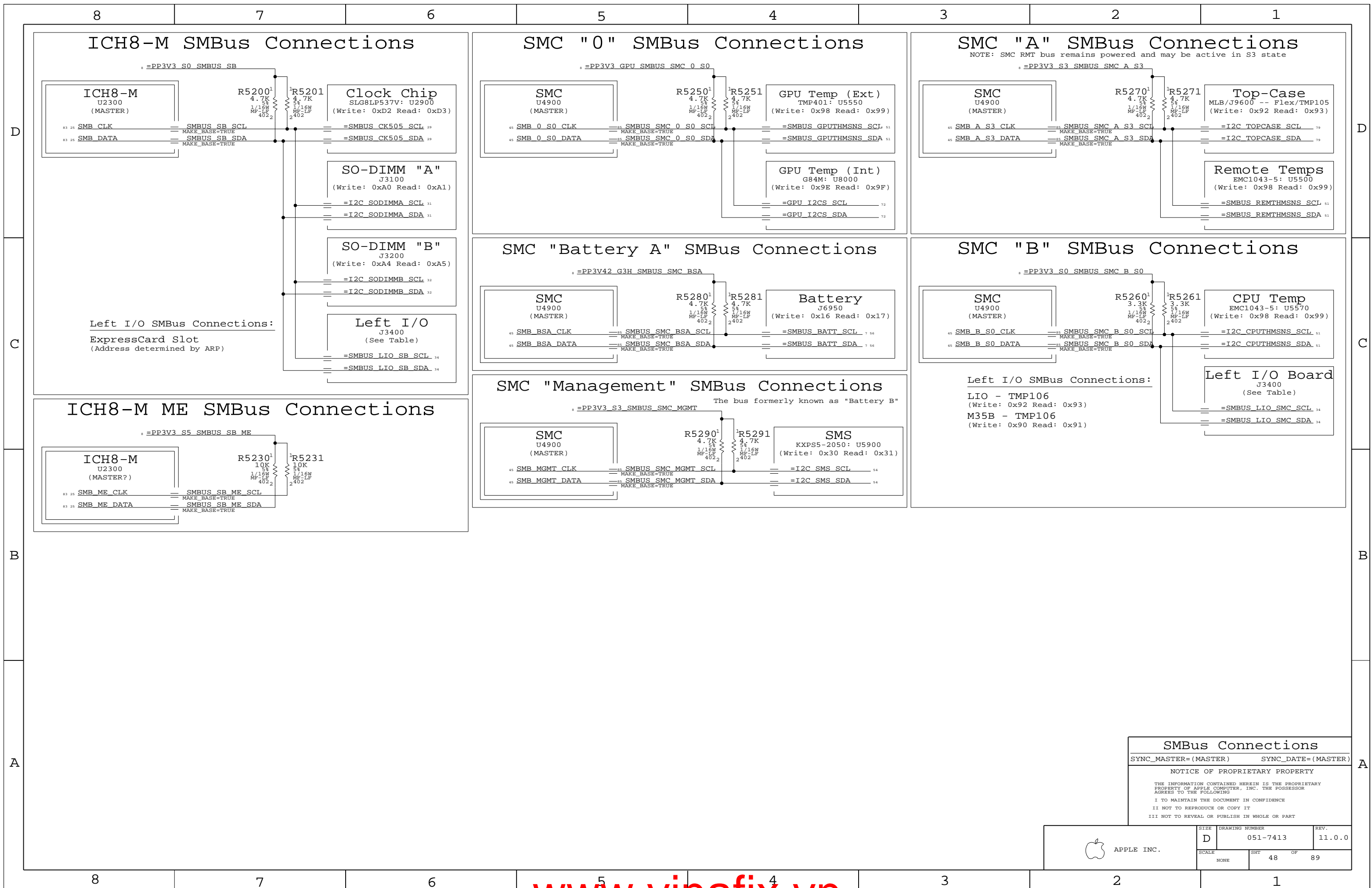
LPC+ Debug Connector

SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/19/2007

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	D	051-7413	11.0.0
SCALE	SHT	OF	
NONE	47	89	



**SMBus Connections**  
 SYNC\_MASTER=(MASTER)      SYNC\_DATE=(MASTER)

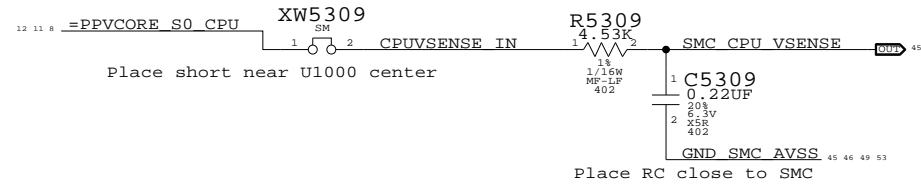
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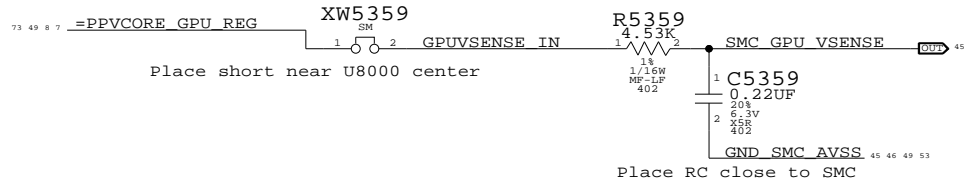
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
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 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7413	11.0.0
SCALE	SHT	OF	
NONE	48	89	

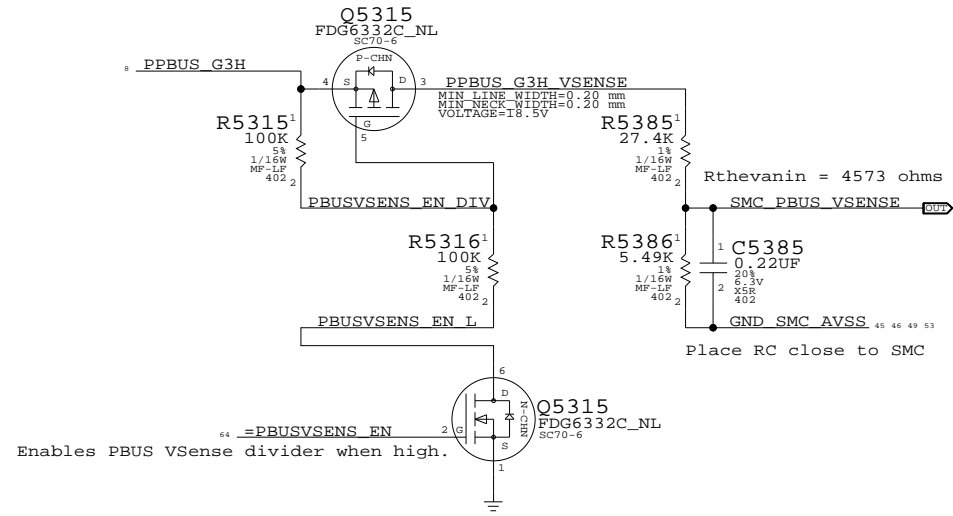
### CPU Voltage Sense / Filter



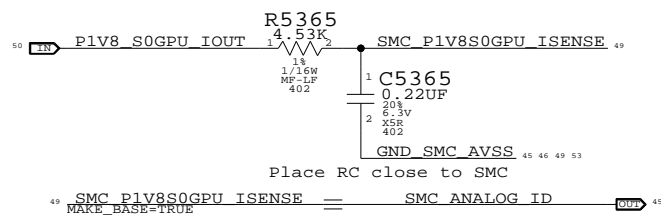
### GPU Voltage Sense / Filter



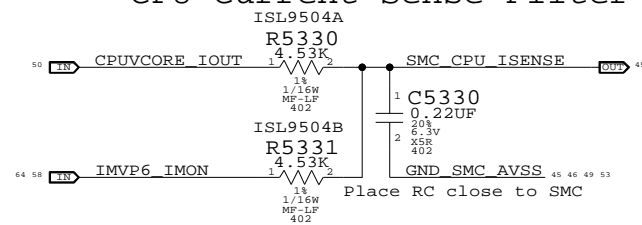
### PBUS Voltage Sense & Filter



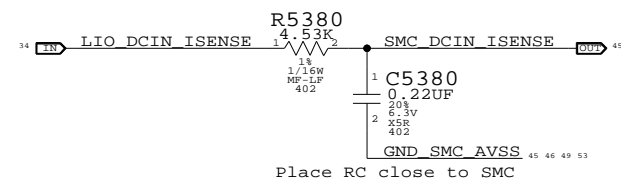
### 1.8V FB Current Sense Filter



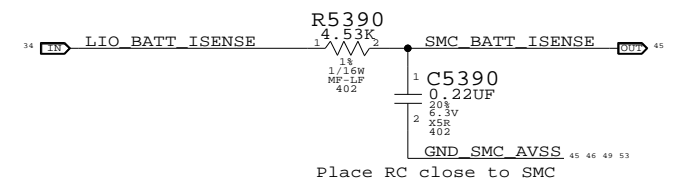
### CPU Current Sense Filter



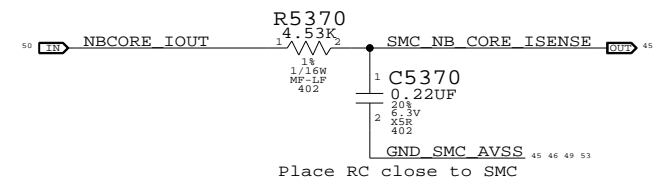
### DCIN Current Sense Filter



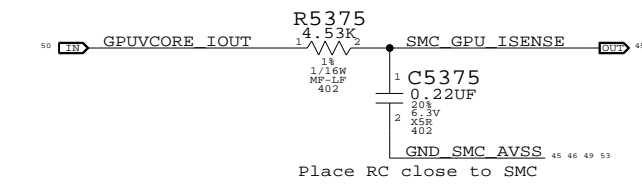
### Battery (PBUS) Current Sense Filter



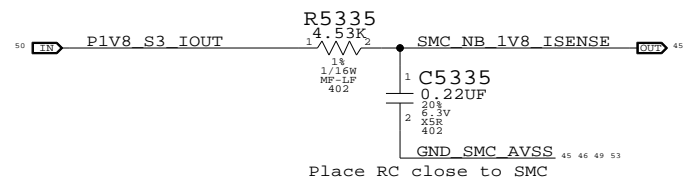
### NB Core Current Sense Filter



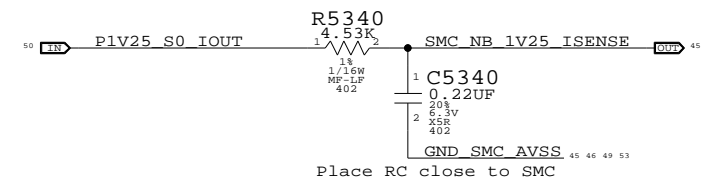
### GPU Current Sense Filter



### NB 1.8V Current Sense Filter

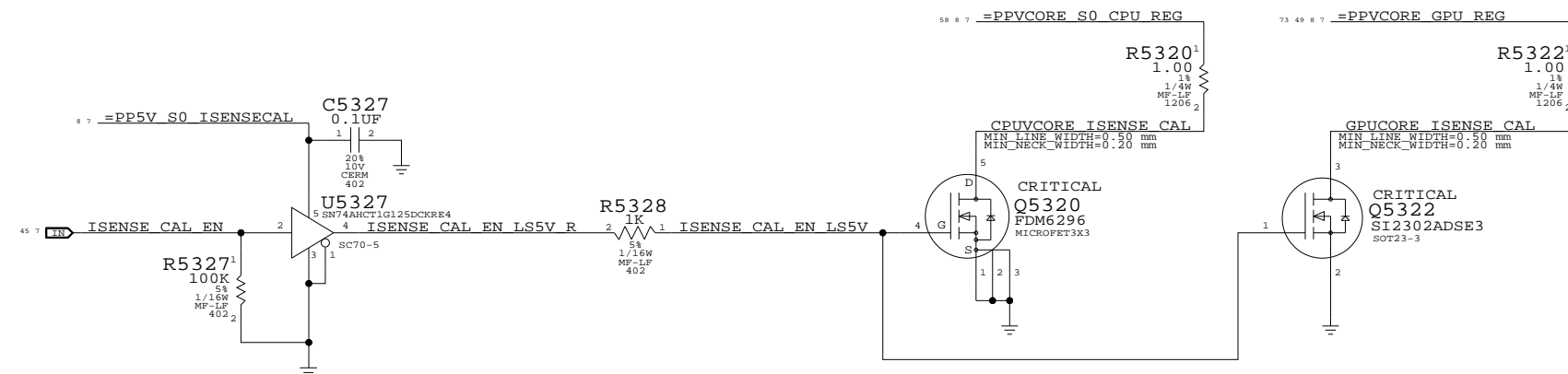


### S0/GPU 1.25V Current Sense Filter



## Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



### Current & Voltage Sensing

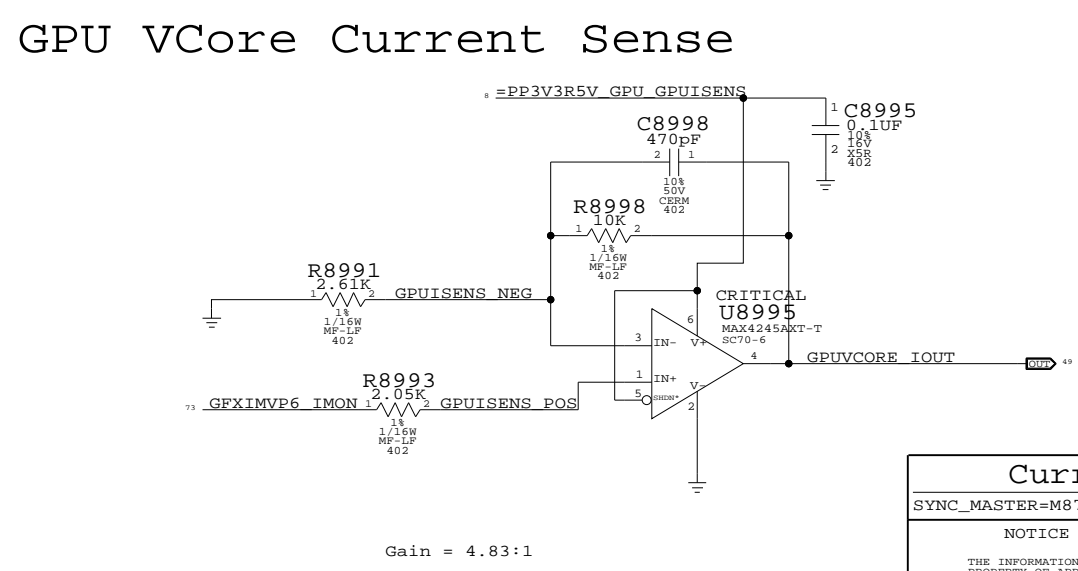
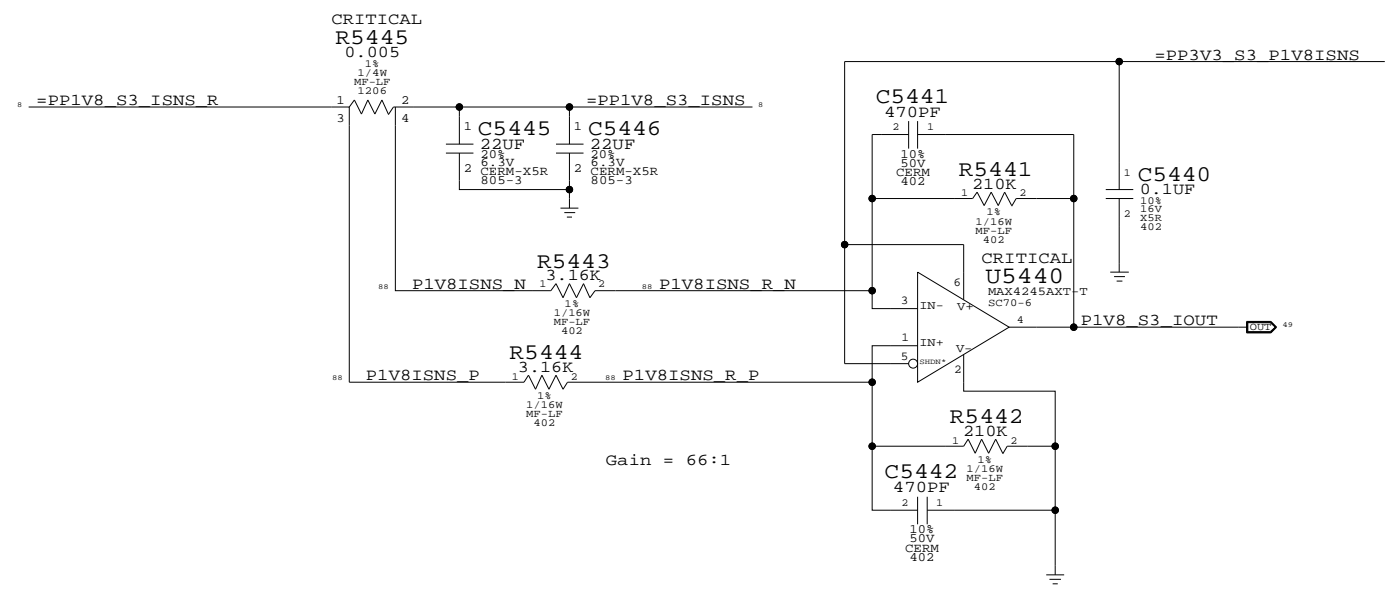
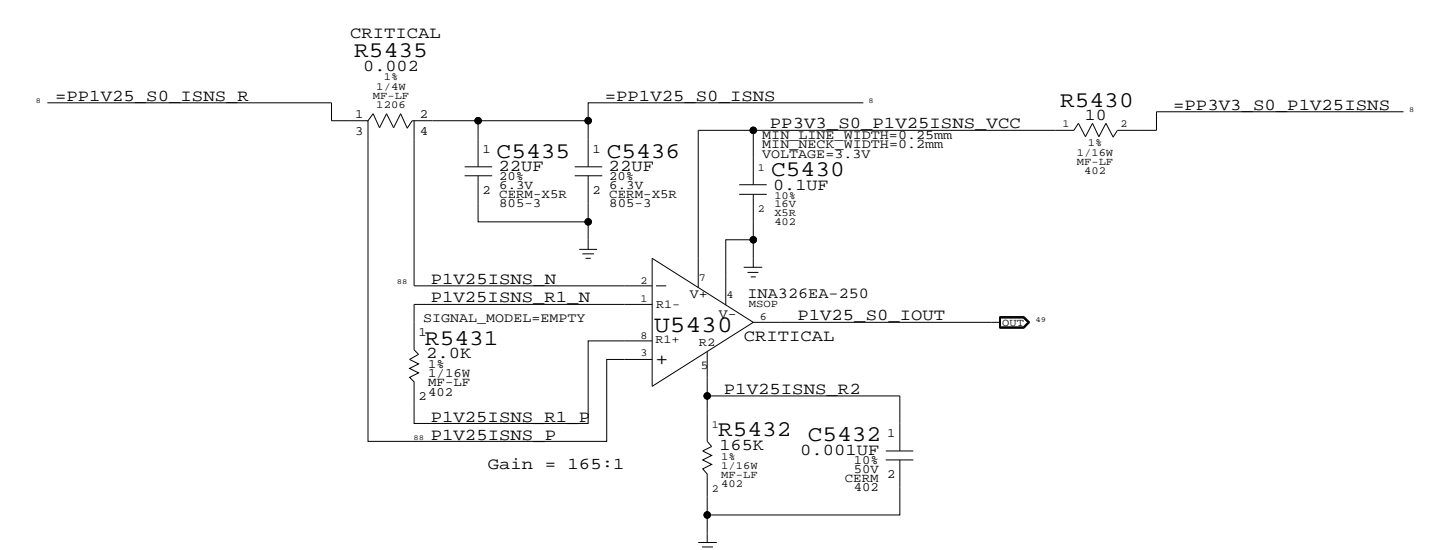
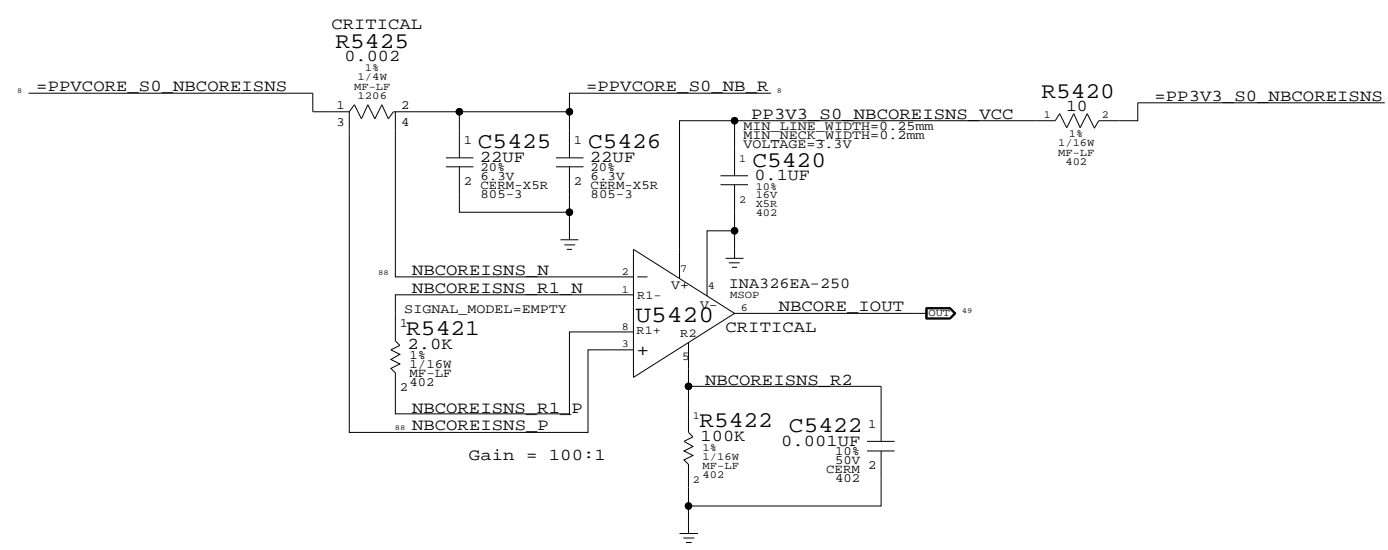
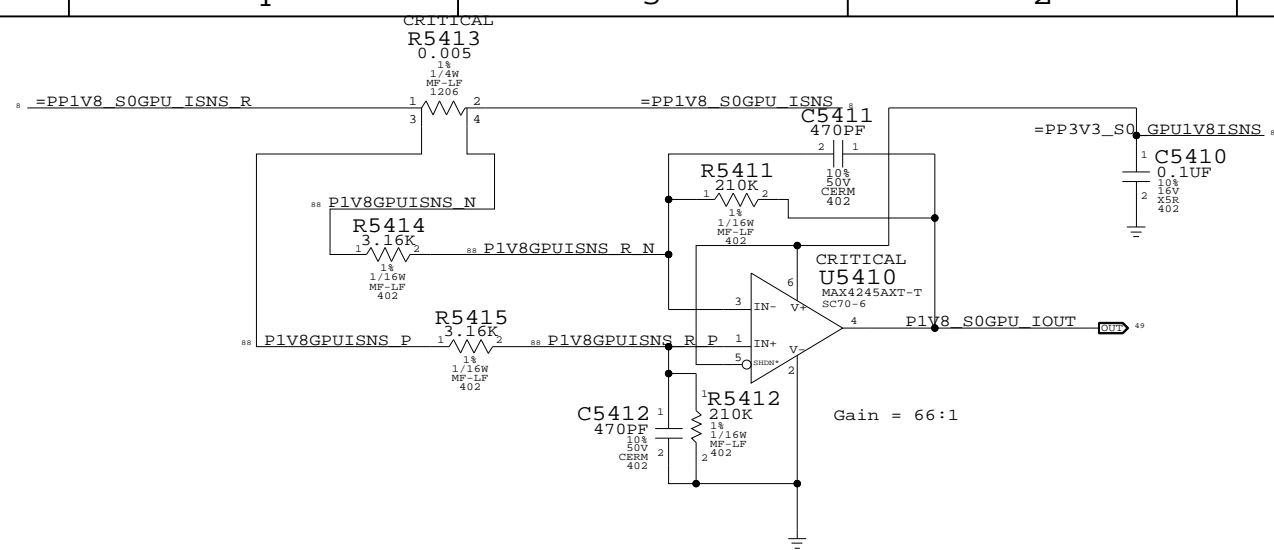
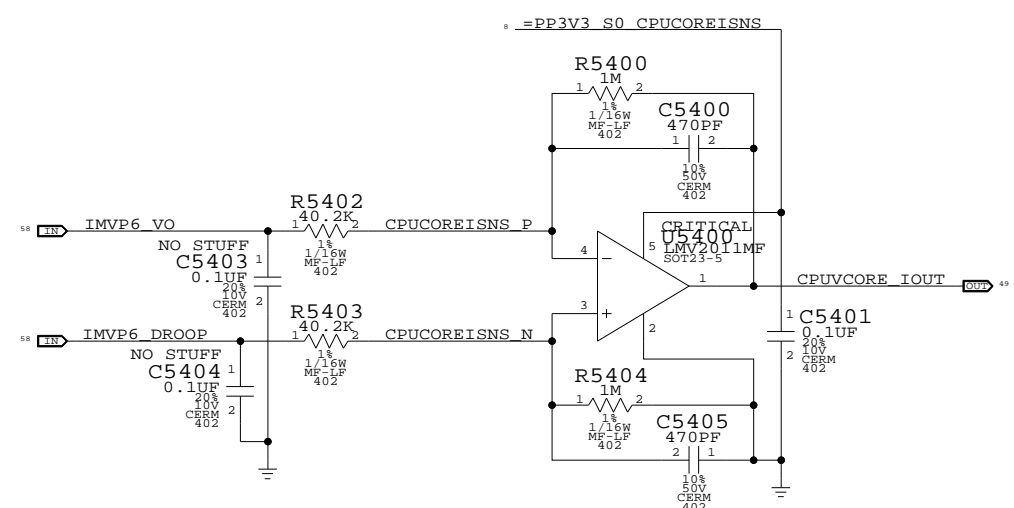
SYNC\_MASTER=M87\_MLB SYNC\_DATE=05/22/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE	SHT	OF
NONE	49	89



**Current Sensing**  
 SYNC\_MASTER=M87\_MLB SYNC\_DATE=05/22/2007

**NOTICE OF PROPRIETARY PROPERTY**

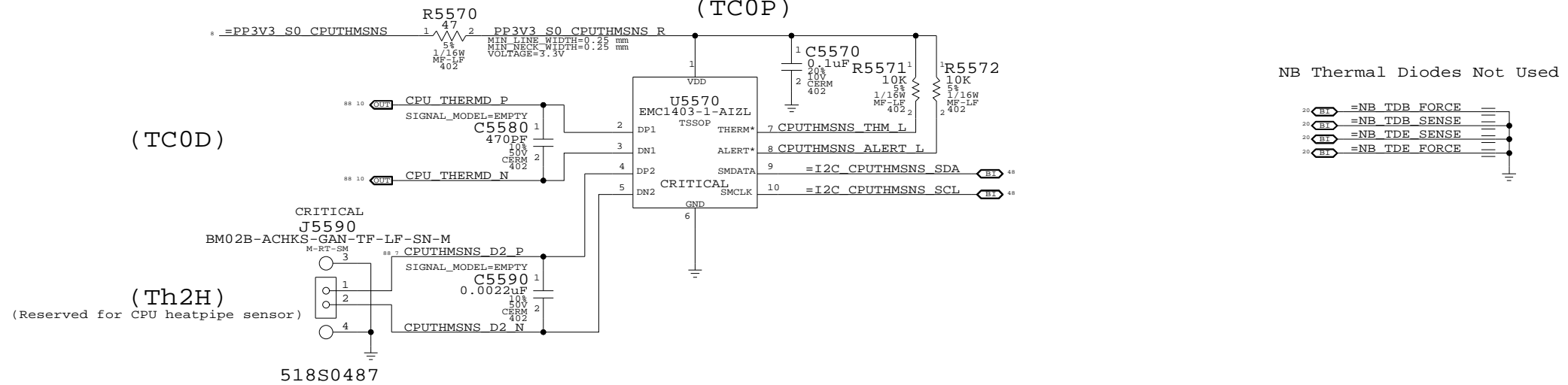
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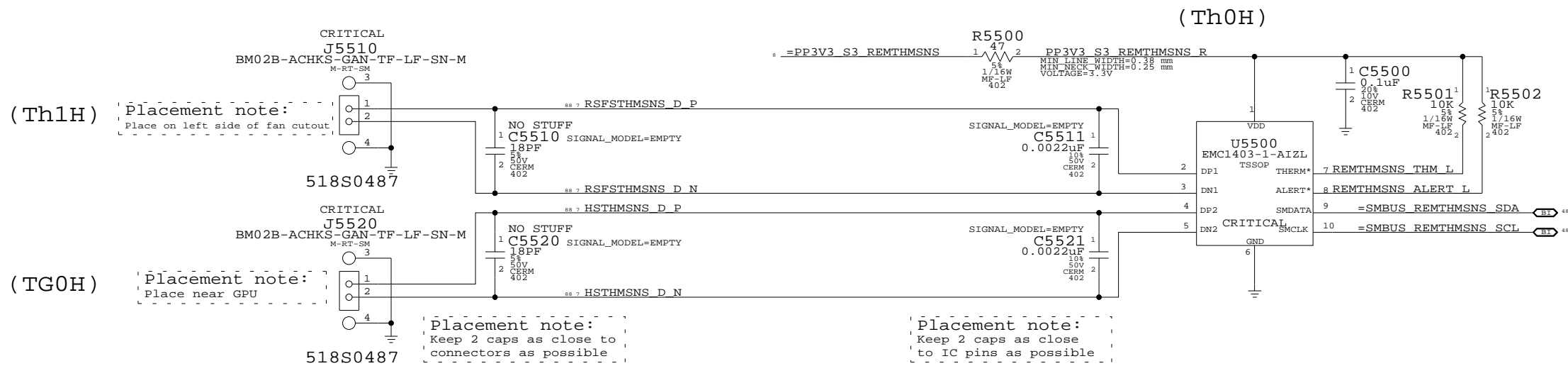
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7413	11.0.0
SCALE	SHT	OF	
NONE	50	89	



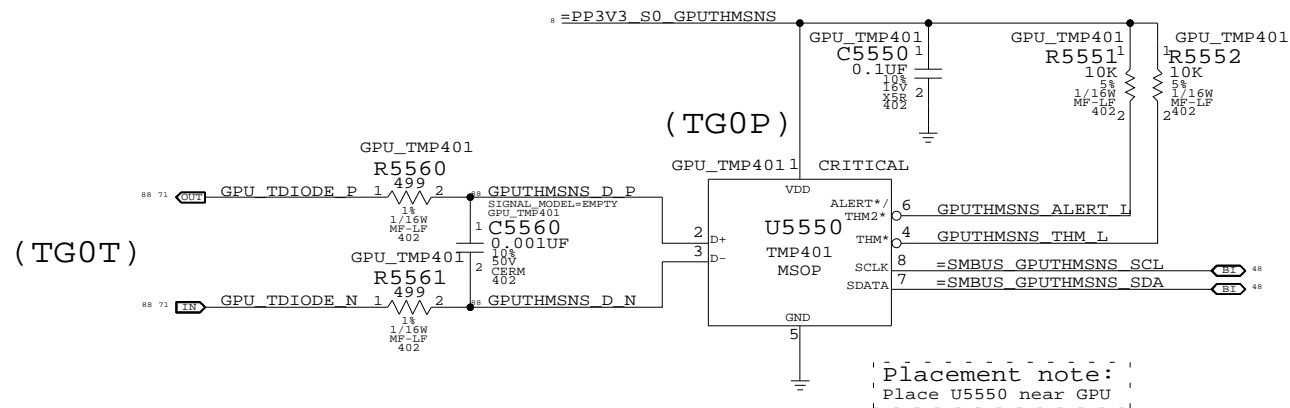
# CPU T-Diode Thermal Sensor (TC0P)



# GPU/Heat Pipe & Bottom Case Skin Thermal Sensor (Th0H)

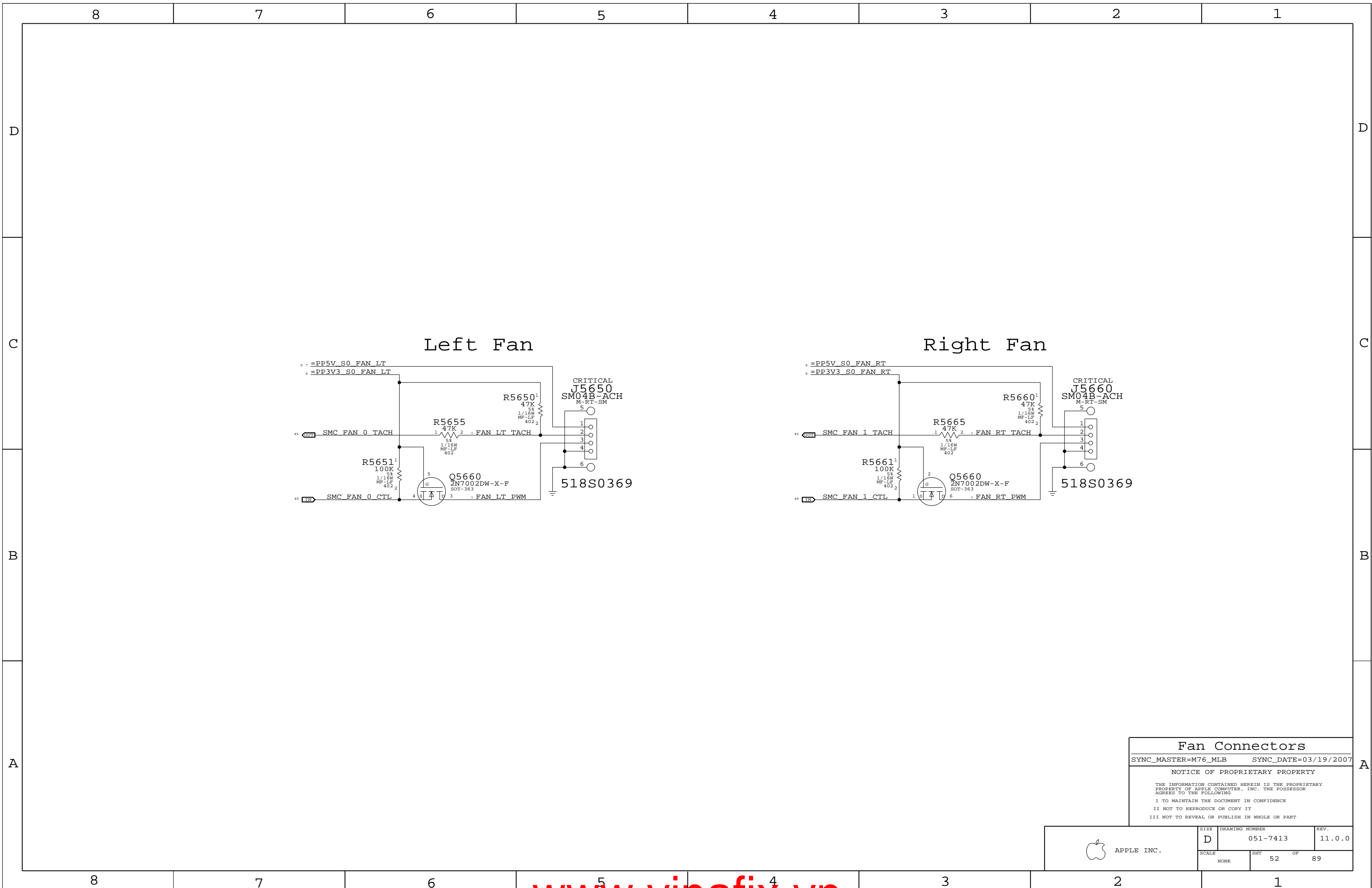


# GPU Die Thermal Sensor (TG0P)



Thermal Sensors		
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)	
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	D	051-7413	11.0.0
SCALE	SHT	OF	
NONE	51	89	



**Fan Connectors**

SYNC\_MASTER=M76\_MLB      SYNC\_DATE=03/19/2007

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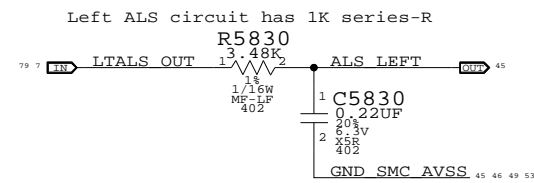
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II NOT TO REPRODUCE OR COPY IT

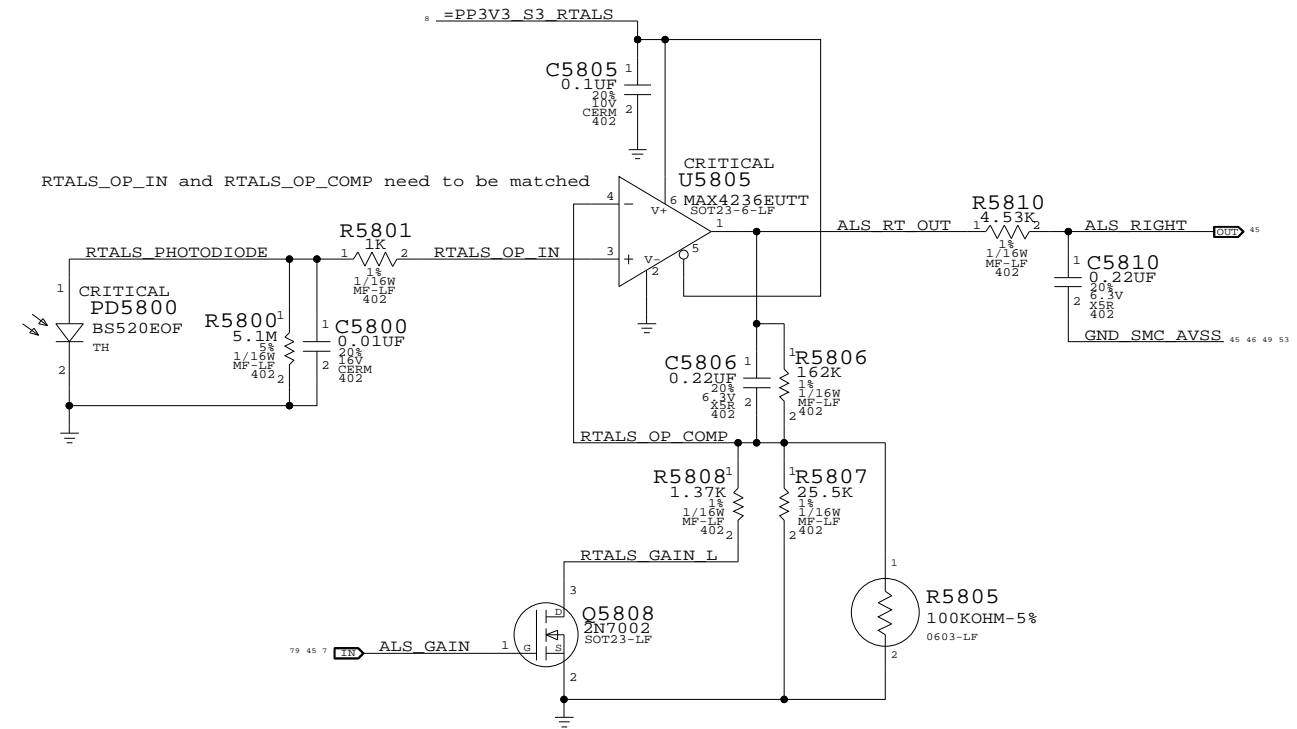
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

	SIZE <b>D</b>	DRAWING NUMBER 051-7413	REV. 11.0.0
	SCALE NONE	SHT 52	OF 89

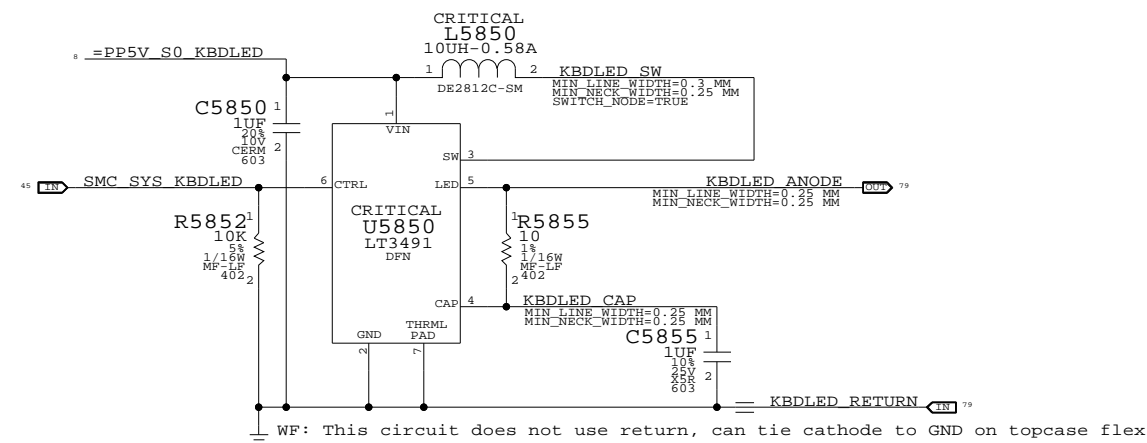
## Left ALS Filter



## Right ALS Circuit



## Keyboard LED Driver



### ALS Support

SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/19/2007

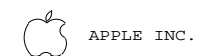
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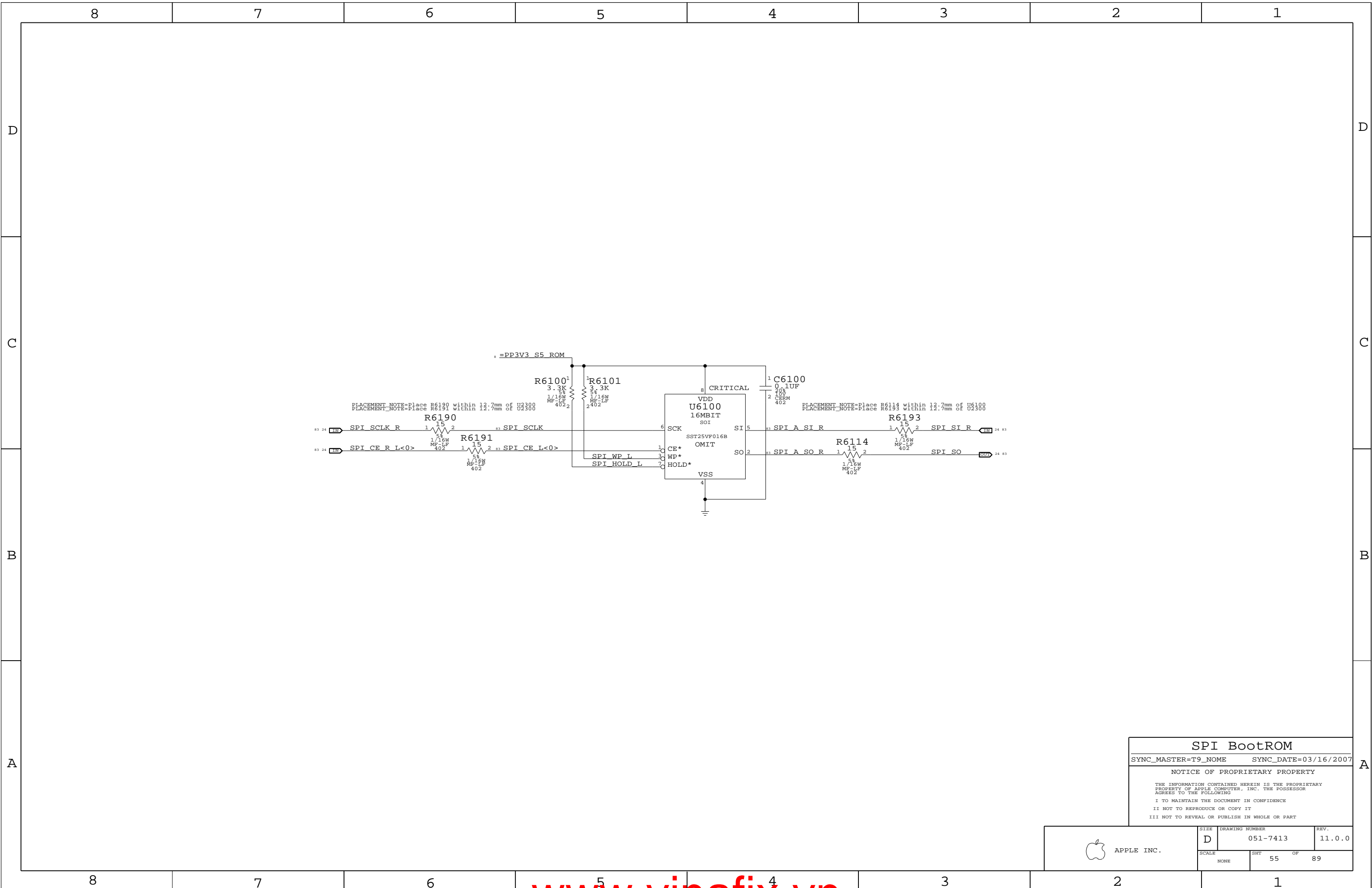
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE	SHT 53 OF 89	
NONE		





**SPI BootROM**

SYNC\_MASTER=T9\_NOME      SYNC\_DATE=03/16/2007

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	SCALE	SHEET	OF	REV.
	NONE	55	OF	89



8

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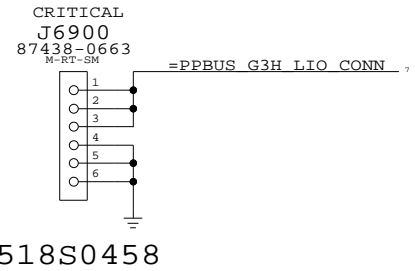
4

3

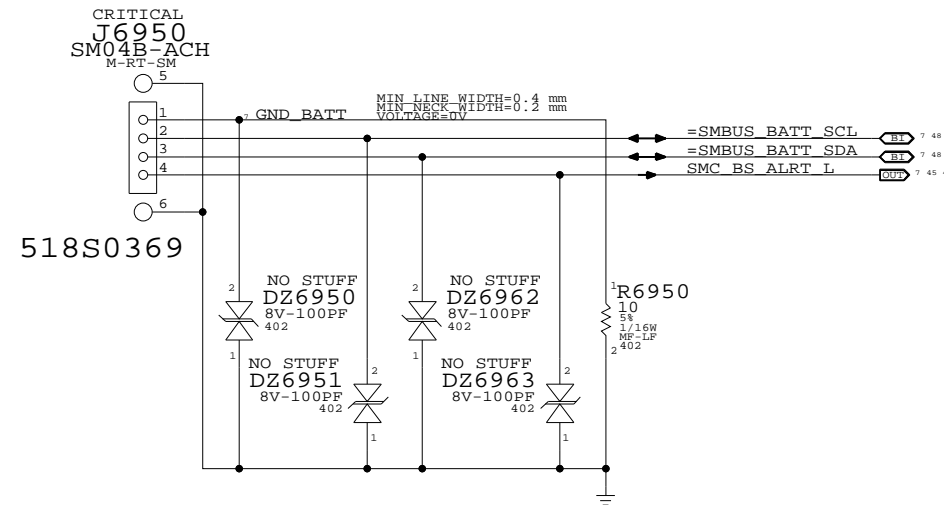
2

1

### Left I/O Power Connector



### Battery Connector (Digital Signals)



PBus-In & Battery Connectors  
 SYNC\_MASTER=(M59\_SYNC) SYNC\_DATE=09/09/2006

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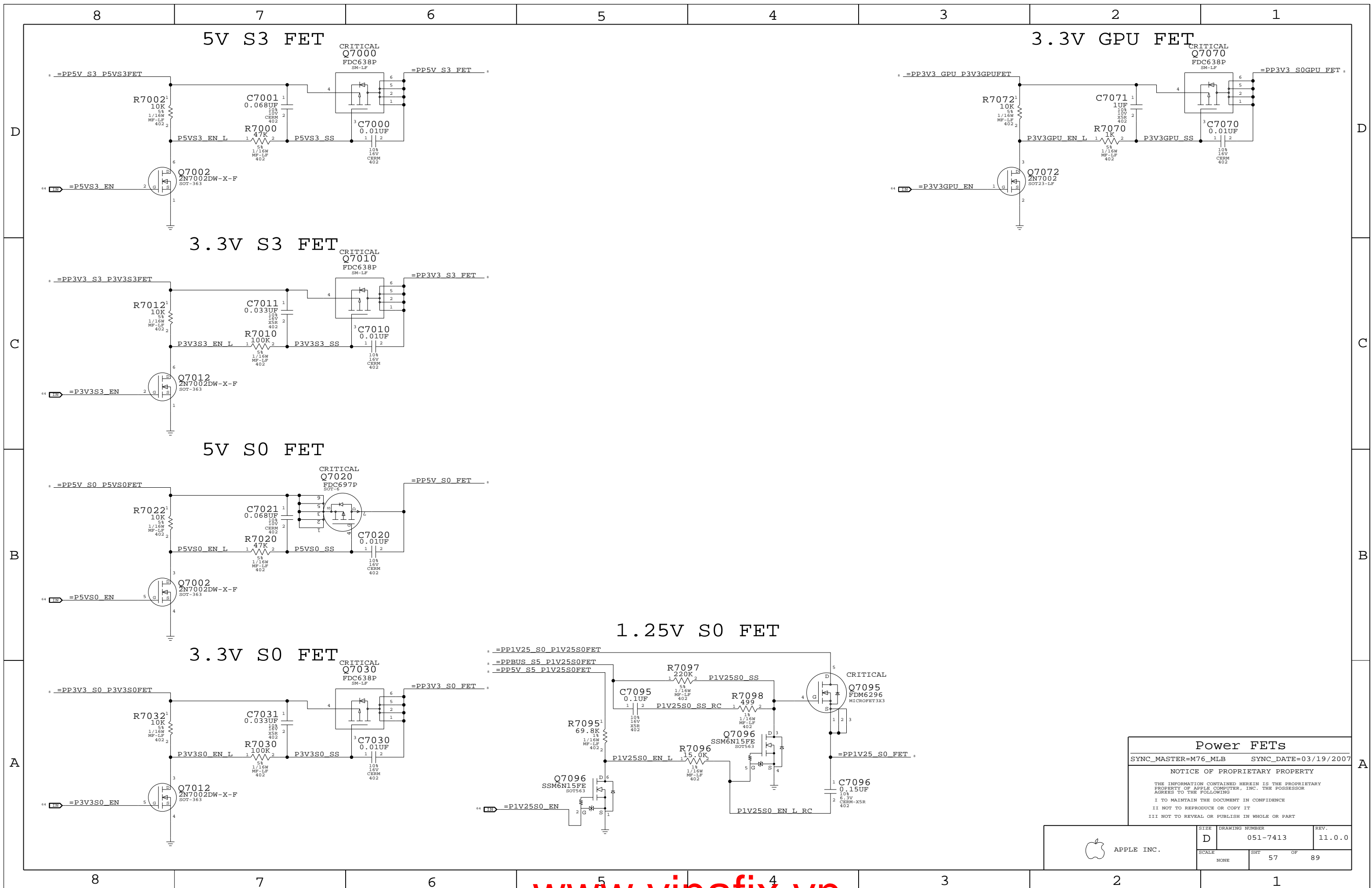
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

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SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE	SHT	OF
NONE	56	89



**Power FETs**

SYNC\_MASTER=M76\_MLB    SYNC\_DATE=03/19/2007

**NOTICE OF PROPRIETARY PROPERTY**

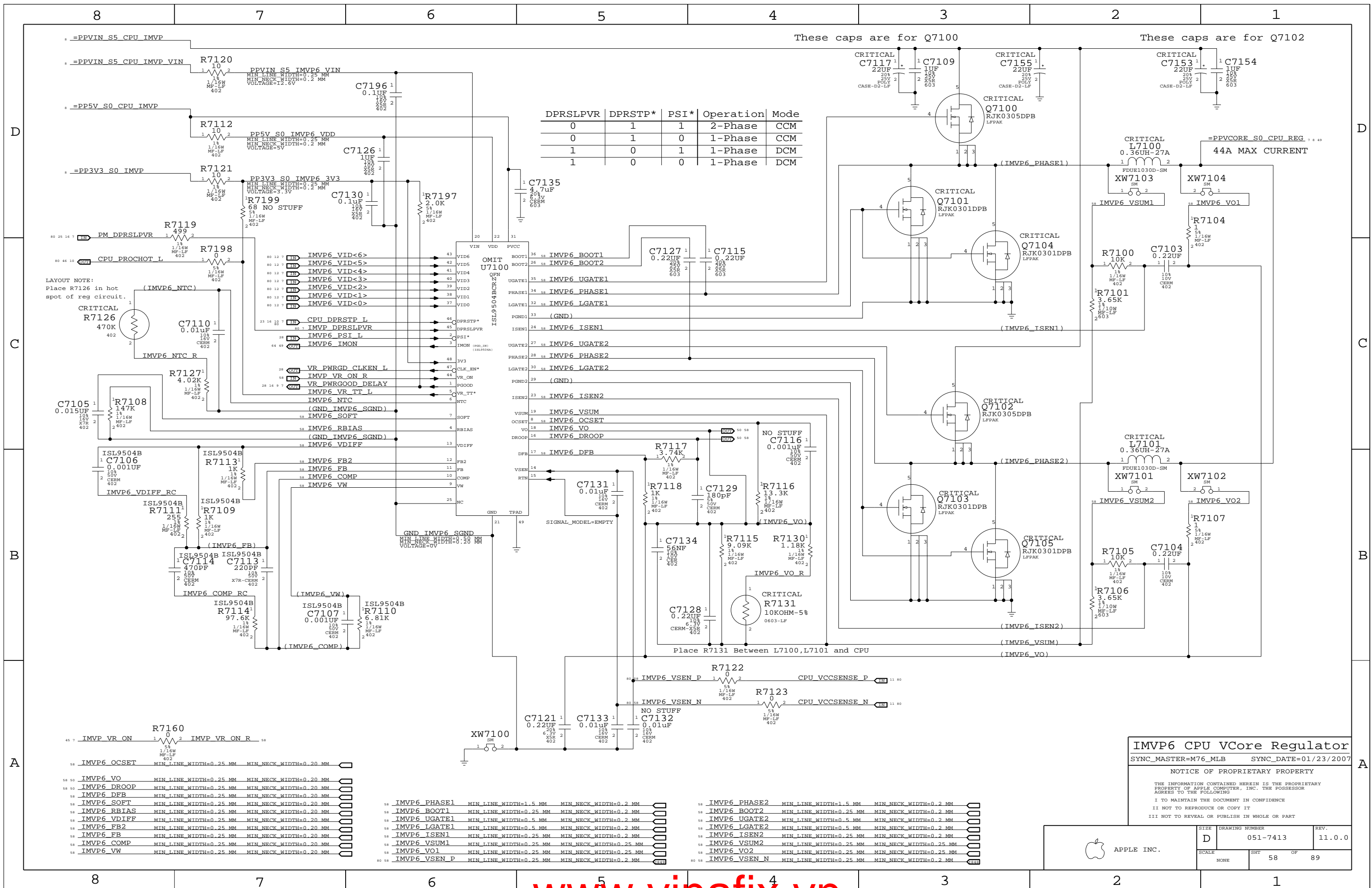
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APPLE INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7413	REV. 11.0.0
	SCALE NONE	SHEET 57	OF 89



DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	0	0	1-Phase	DCM

LAYOUT NOTE:  
Place R7126 in hot spot of reg circuit.

Place R7131 Between L7100, L7101 and CPU

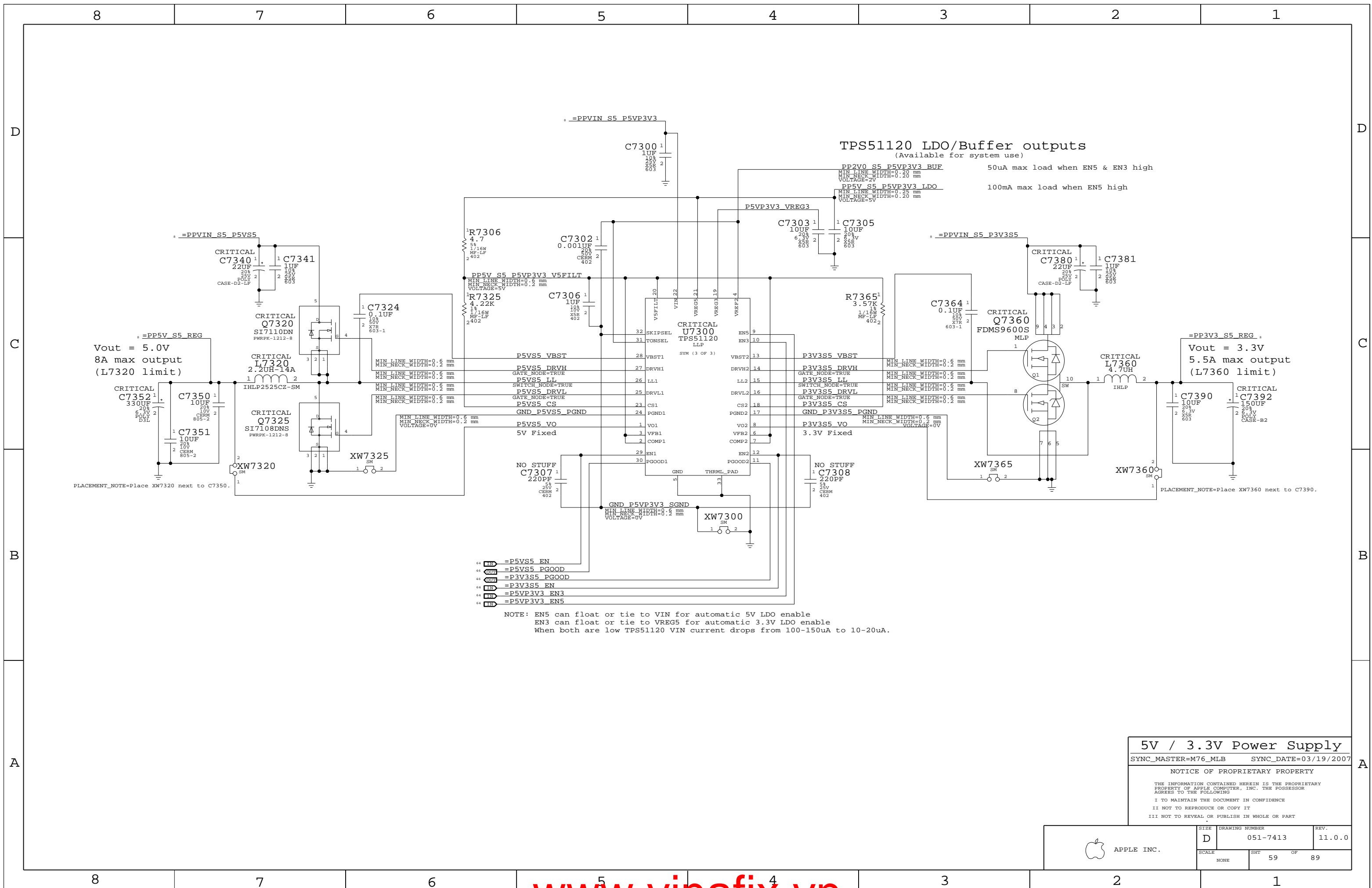
### IMVP6 CPU VCore Regulator

SYNC\_MASTER=M76\_MLB SYNC\_DATE=01/23/2007

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7413	11.0.0
SCALE	SHEET	OF	
NONE	58	OF	89



**TPS51120 LDO/Buffer outputs**  
(Available for system use)

PP2V0 S5 P5VP3V3 BUF 50uA max load when EN5 & EN3 high  
 PP5V S5 P5VP3V3 LDO 100mA max load when EN5 high

Vout = 5.0V  
8A max output  
(L7320 limit)

Vout = 3.3V  
5.5A max output  
(L7360 limit)

NOTE: EN5 can float or tie to VIN for automatic 5V LDO enable  
 EN3 can float or tie to VREG5 for automatic 3.3V LDO enable  
 When both are low TPS51120 VIN current drops from 100-150uA to 10-20uA.

**5V / 3.3V Power Supply**

SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/19/2007

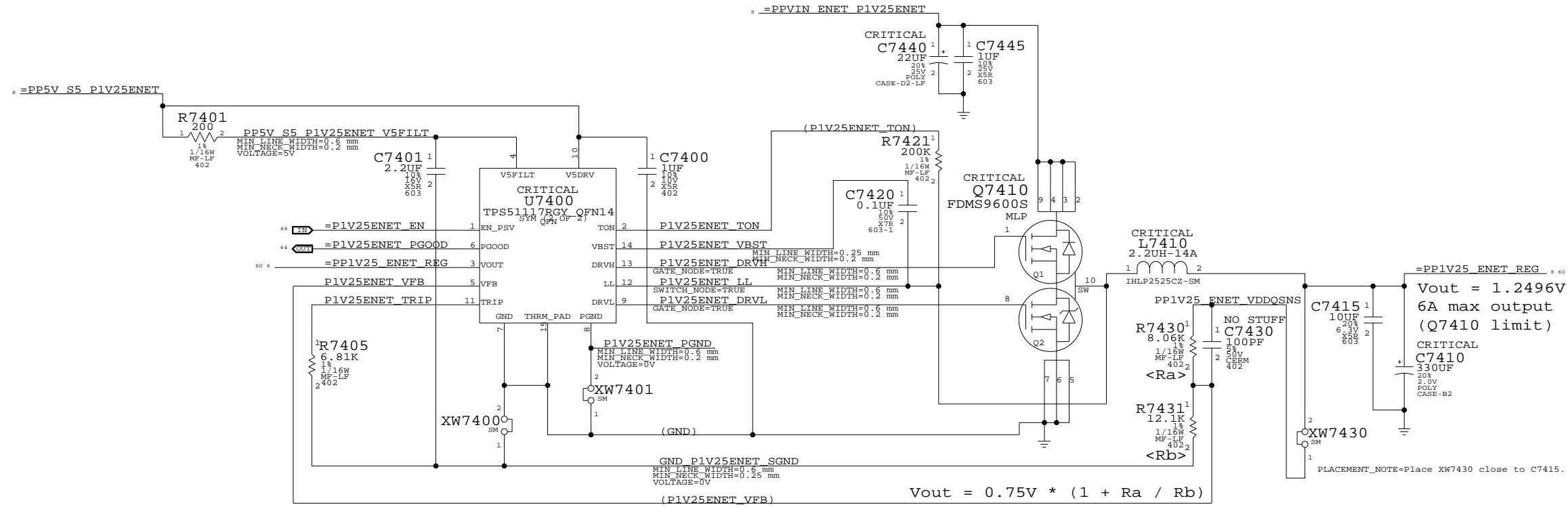
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SCALE	SHT	OF	REV.
NONE	59	89	

D

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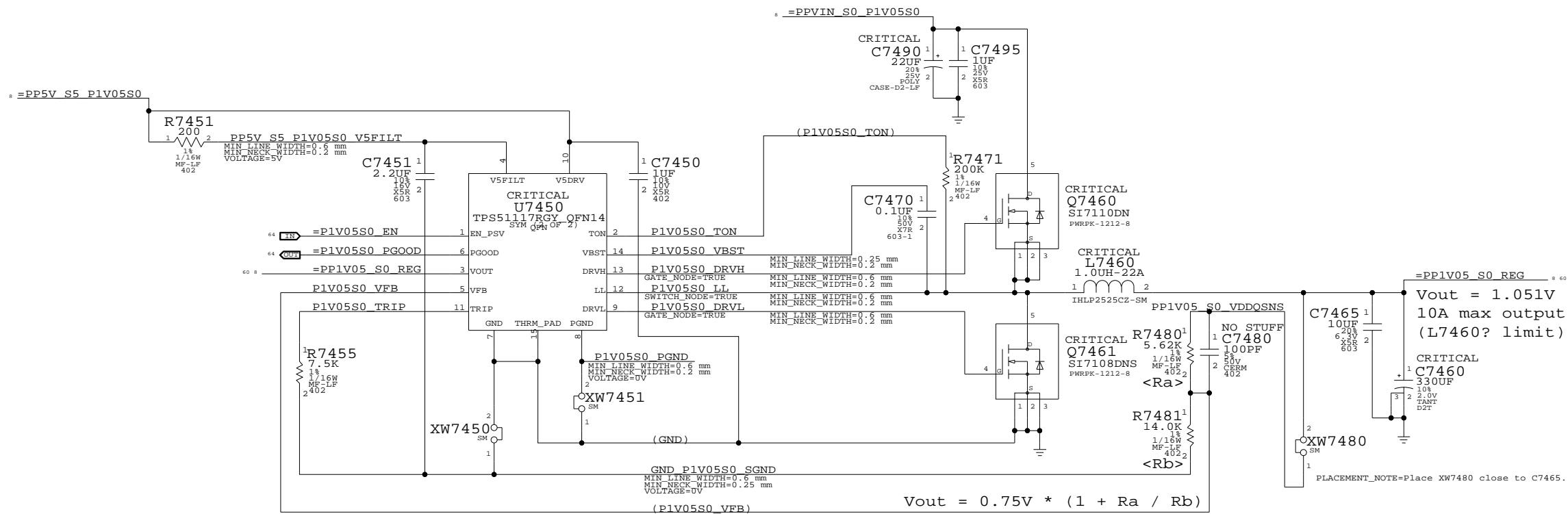


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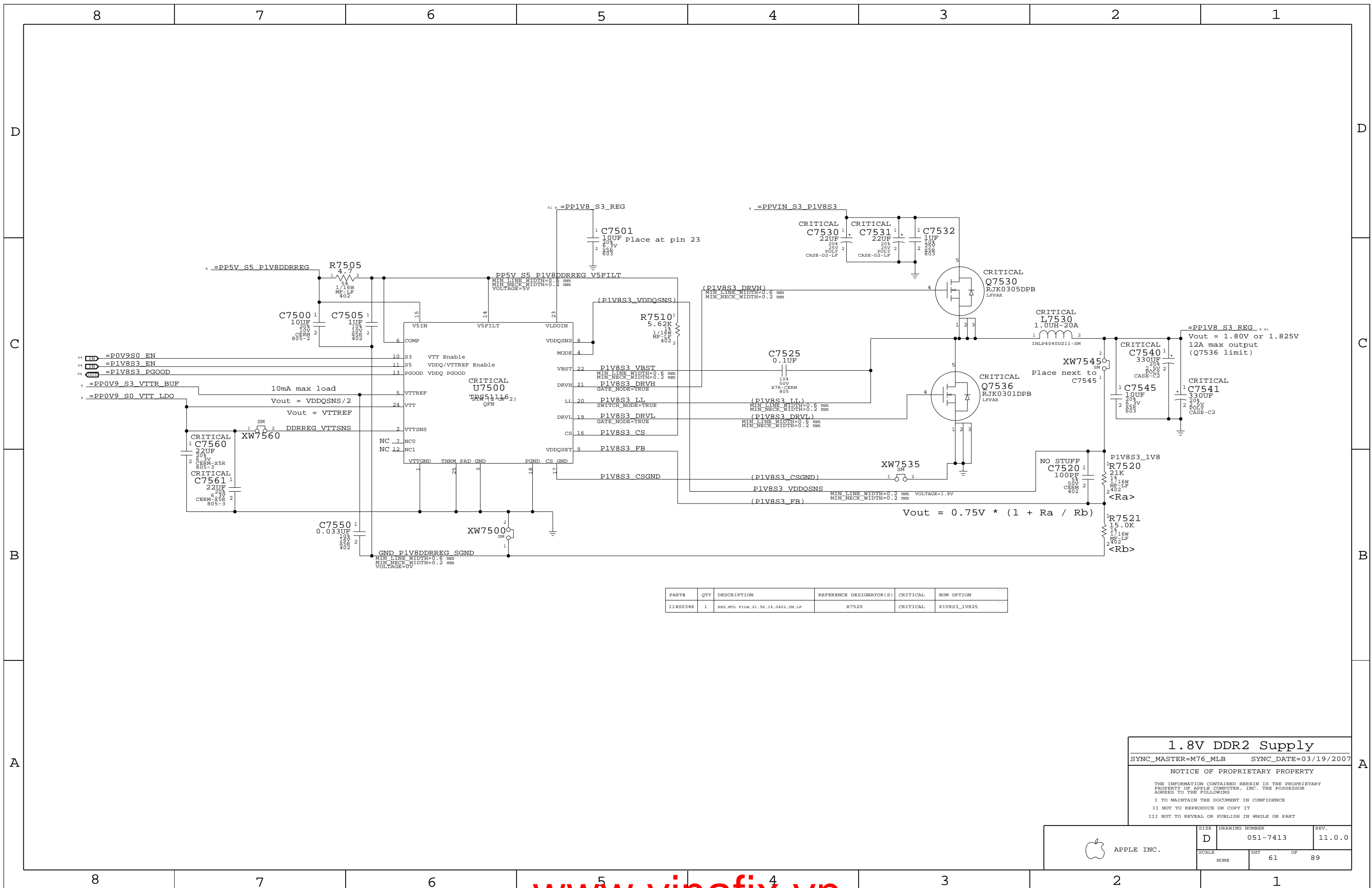
A

**1.25V / 1.05V Power Supply**  
 SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/12/2007

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	D	051-7413	11.0.0
SCALE	SHT	OF	
NONE	60	89	





PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
11480346	1	RES,MTL FILM,21 SK,18,0402,SM,LF	R7520	CRITICAL	P1V8S3_1V825

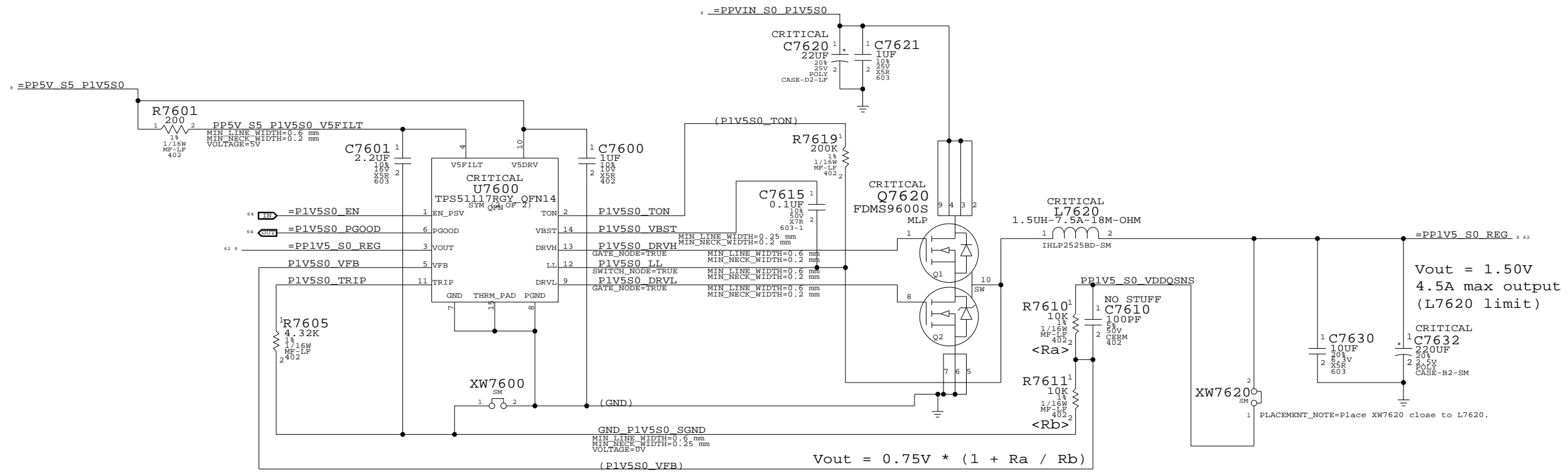
**1.8V DDR2 Supply**  
 SYNC\_MASTER=M76\_MLB    SYNC\_DATE=03/19/2007

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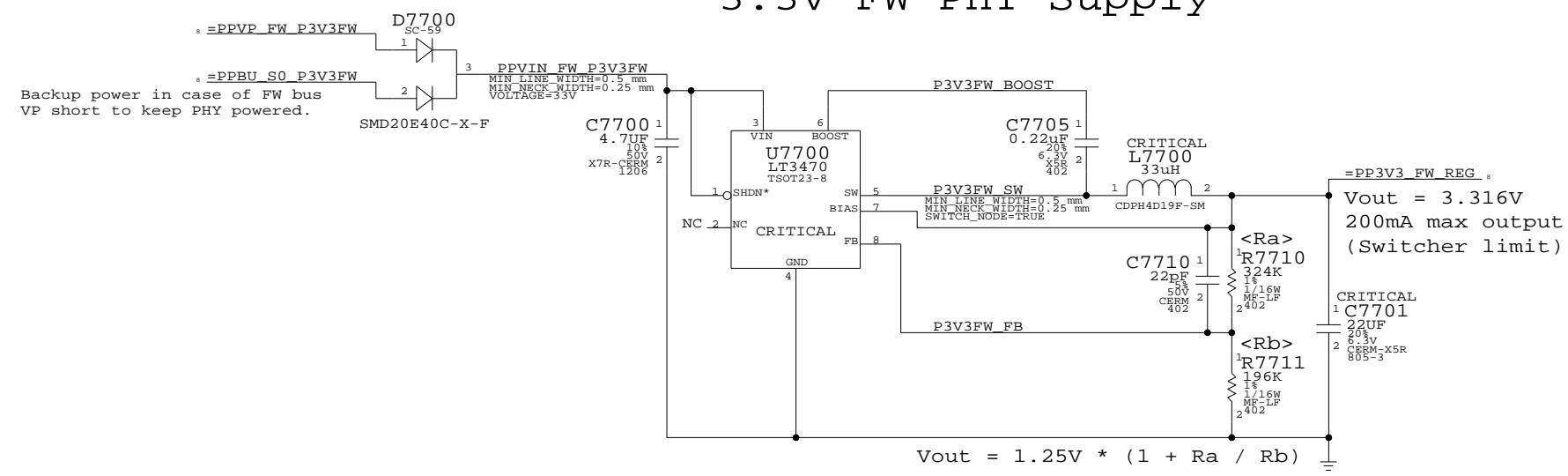
 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7413	11.0.0
SCALE	SHT	OF	REV.
NONE	61	89	



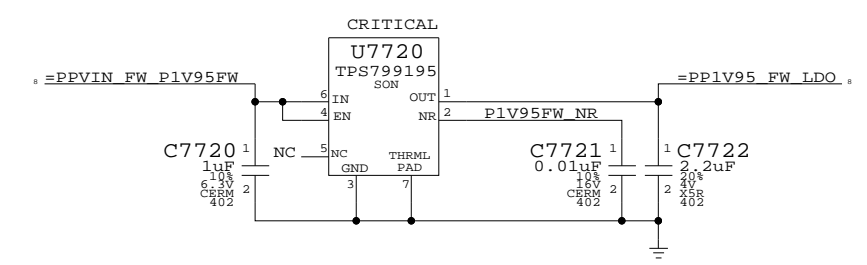
**1.5V Power Supply**  
 SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/12/2007  
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APPLE INC.	SIZE D	DRAWING NUMBER 051-7413	REV. 11.0.0
	SCALE NONE	SHEET 62	OF 89

### 3.3V FW PHY Supply



### 1.95V FW PHY Supply

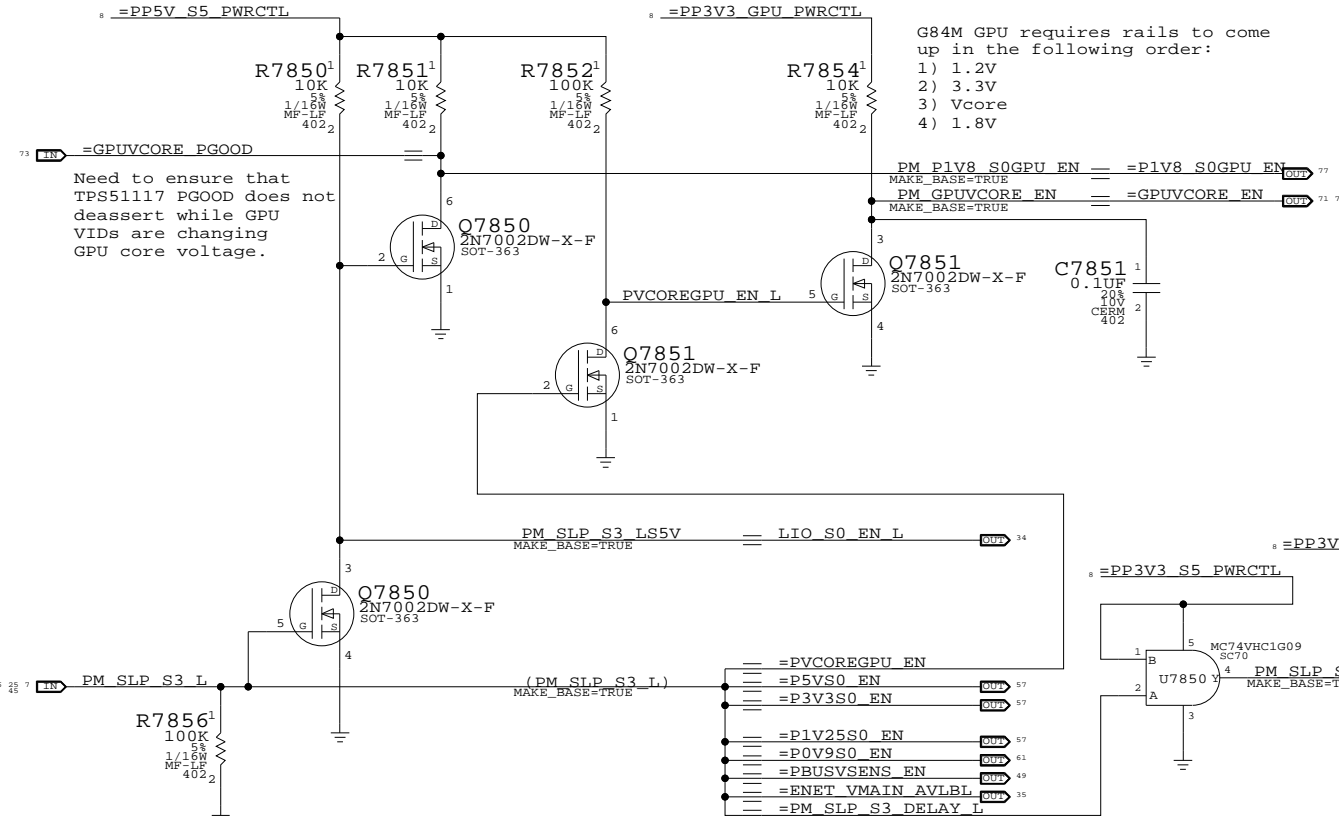


**FW PHY Power Supplies**  
 SYNC\_MASTER=M76\_MLB SYNC\_DATE=03/19/2007

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SCALE	SHT	OF	
NONE	63	89	

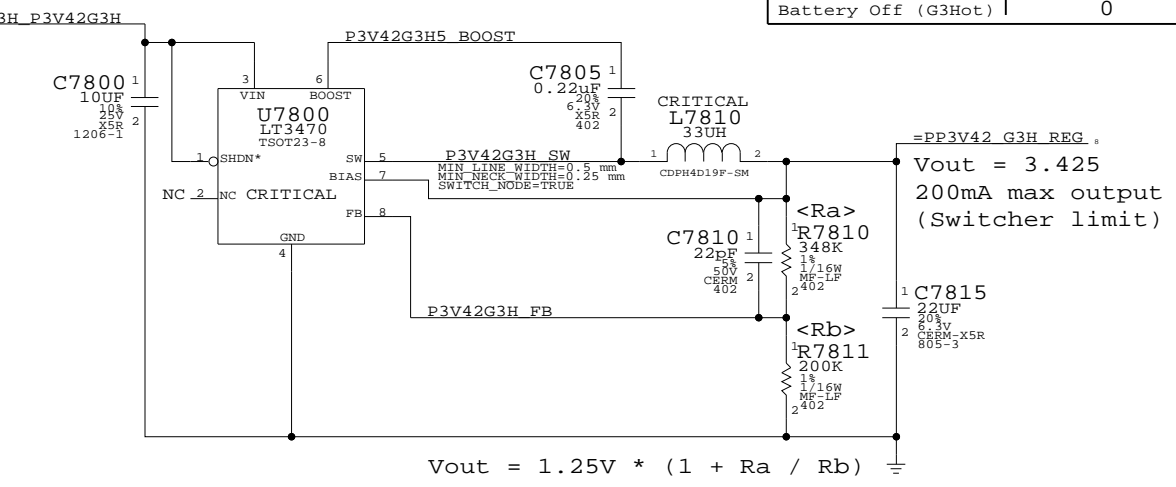
# Power Control Signals



# 3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC Vref generator

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

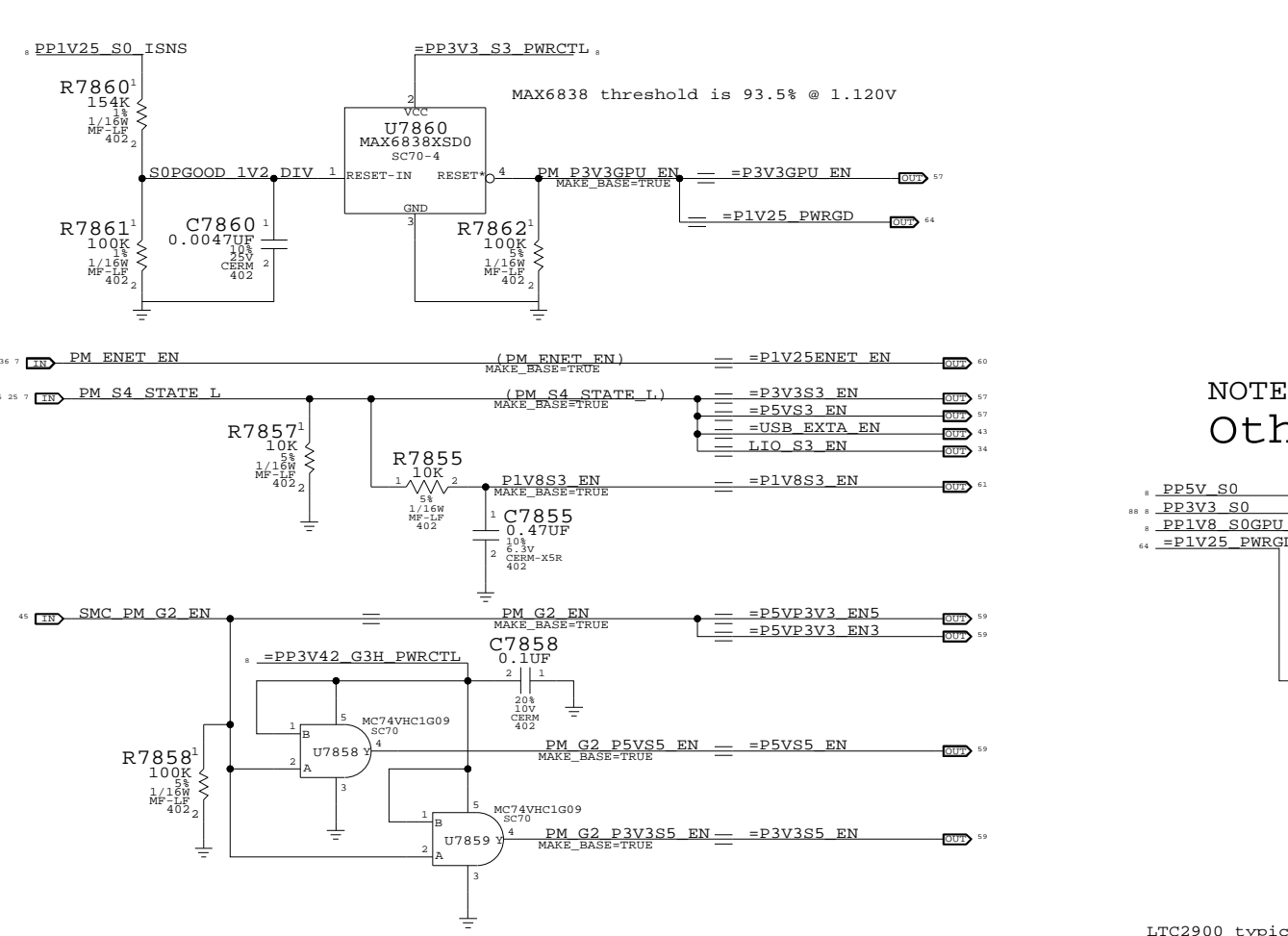


# Unused PG00D Signals

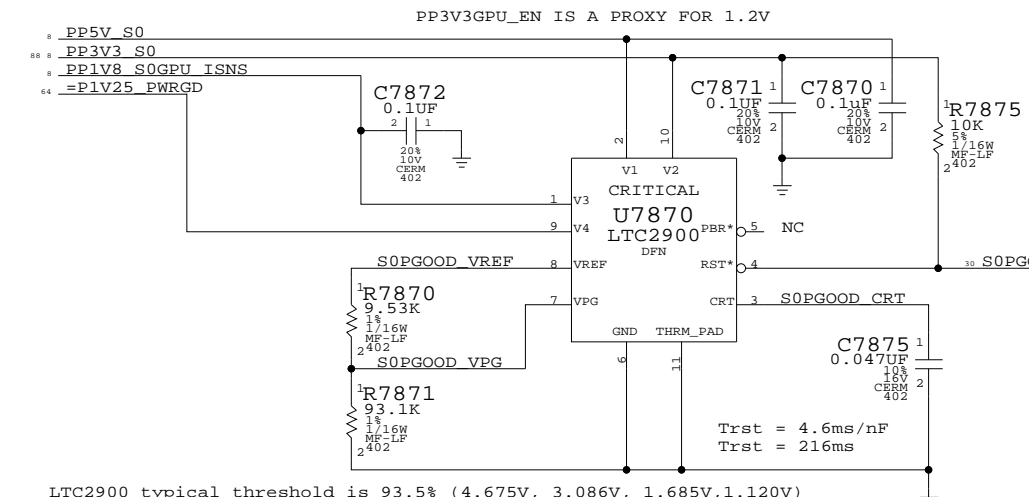
- TP P1V25ENET PG00D
- TP P1V8\_S0GPU PG00D

# 1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation



# NOTE: 0.9V is not checked! Other S0 Rails PWRGD Circuit



3.425V G3Hot Supply & Power Control  
 SYNC\_MASTER=M88 SYNC\_DATE=08/02/2007

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SCALE	SHT	OF	
NONE	64	89	





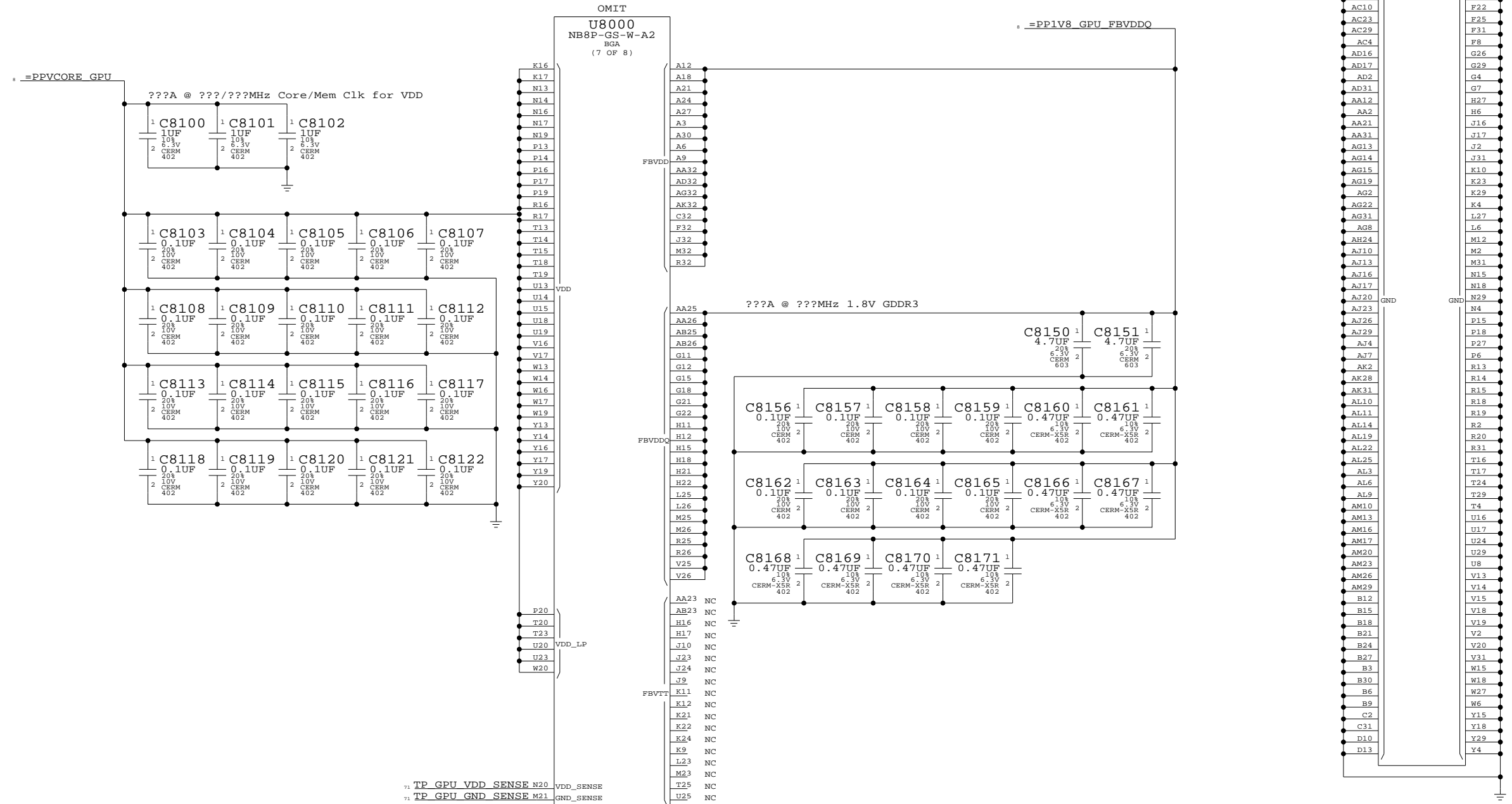
# Page Notes

Power aliases required by this page:

- =PPVCORE\_GPU
- =PP1V8\_GPU\_FBVDDQ

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
(NONE)



NV G84M Core/FB Power  
 SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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	D	051-7413	11.0.0
SCALE	SHT	OF	
NONE	66	89	

# Page Notes

Power aliases required by this page:

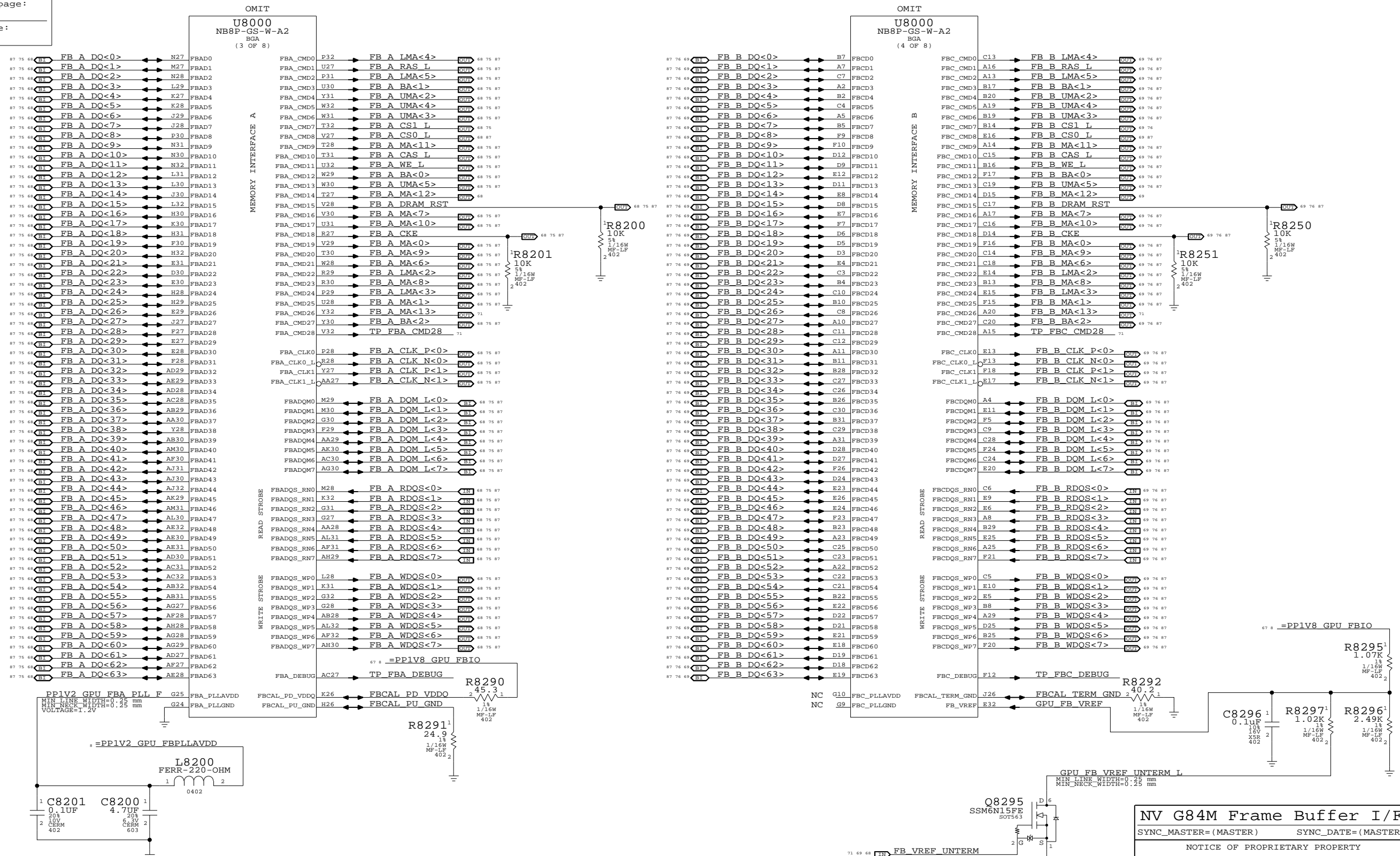
- =PP1V2\_GPU\_FBPLLAVDD
- =PP1V8\_GPU\_FBIO

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

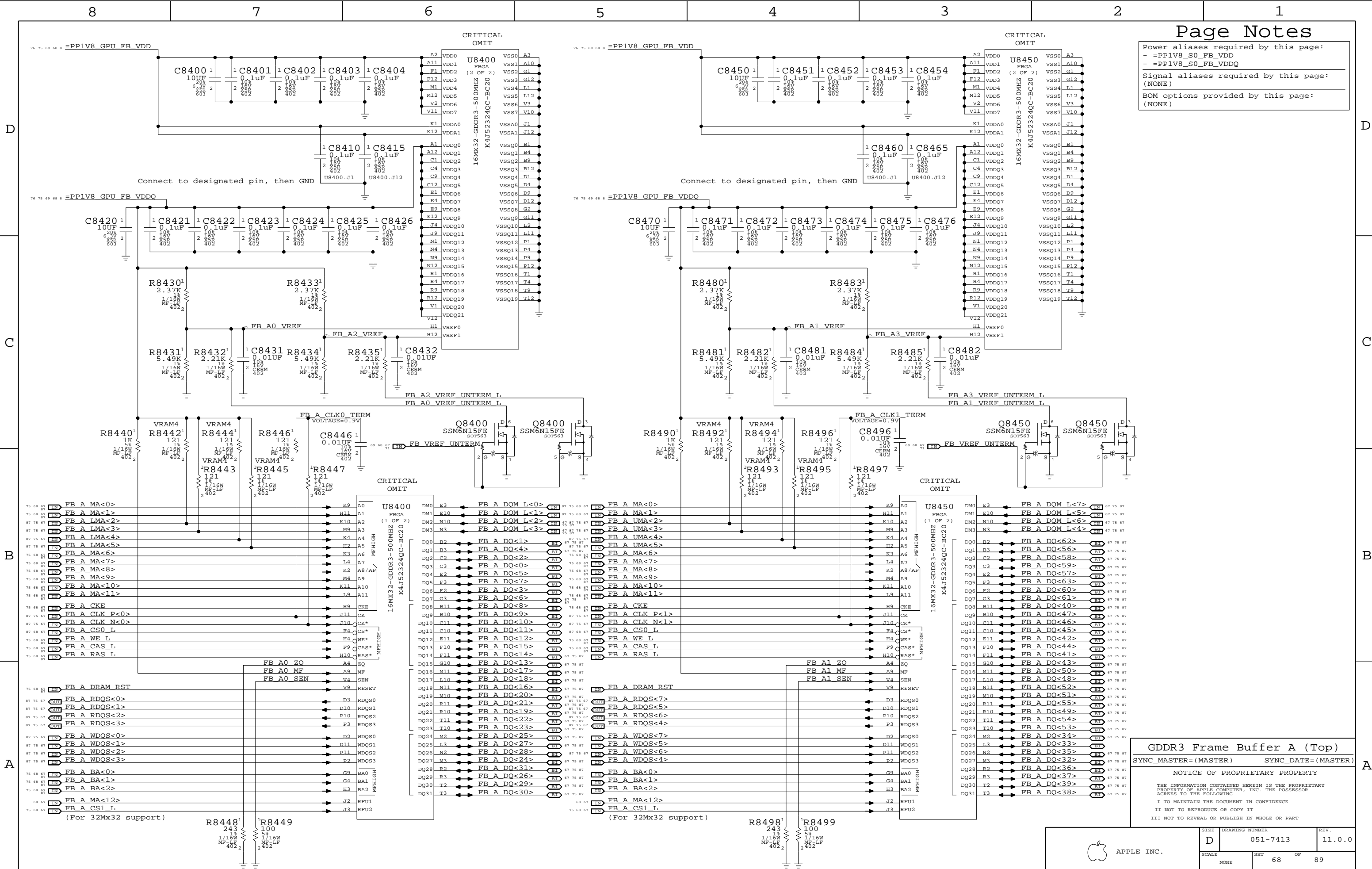


**NV G84M Frame Buffer I/F**  
 SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7413	11.0.0
SCALE	SHT	OF	
NONE	67	89	

Power aliases required by this page:  
- =PPIV8\_S0\_FB\_VDD  
- =PPIV8\_S0\_FB\_VDDQ  
Signal aliases required by this page:  
(NONE)  
BOM options provided by this page:  
(NONE)



GDDR3 Frame Buffer A (Top)

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

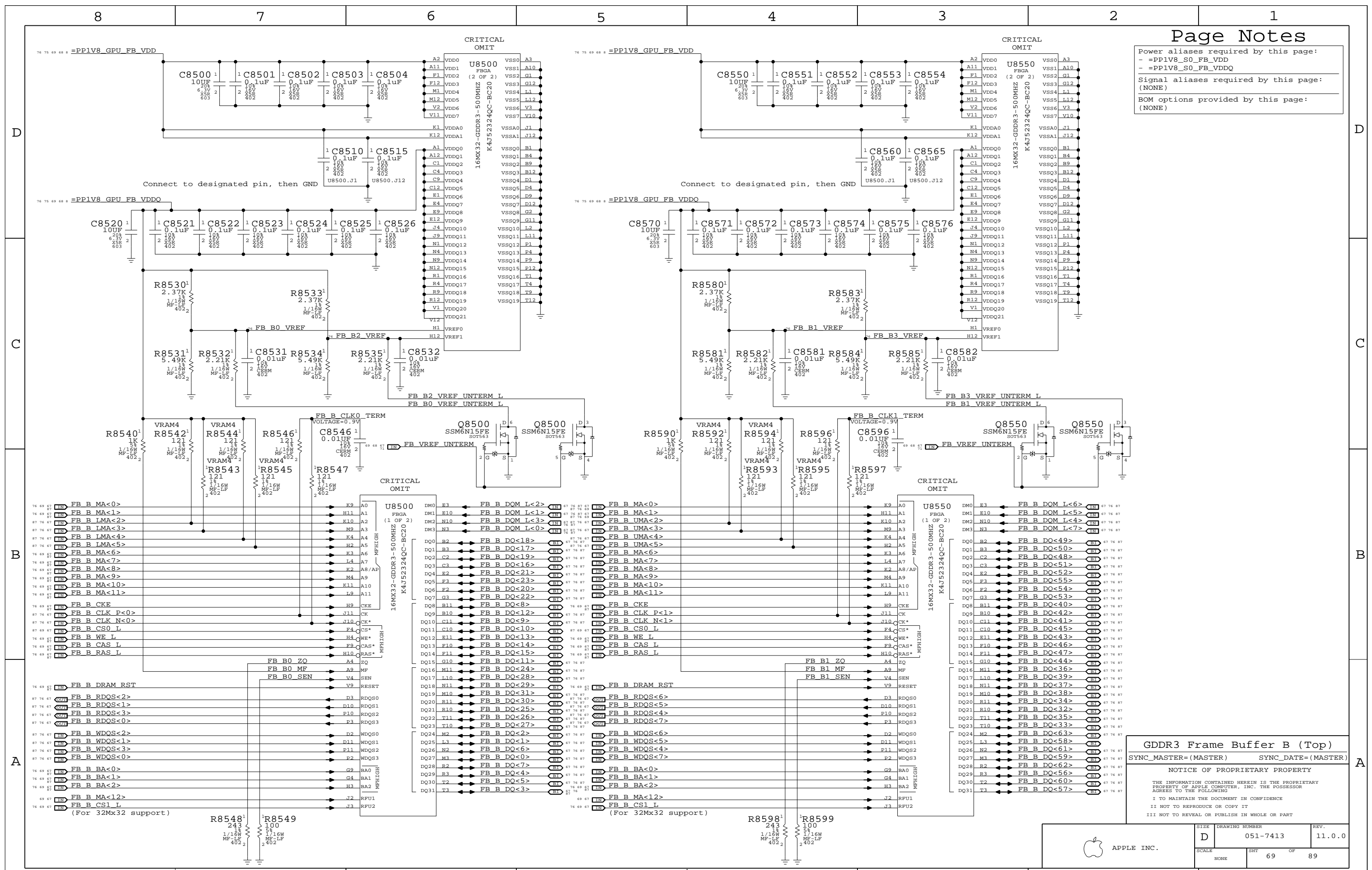
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7413	11.0.0
SCALE	SHT	OF	
NONE	68	89	



Power aliases required by this page:  
- =PPIV8\_S0\_FB\_VDD  
- =PPIV8\_S0\_FB\_VDDQ  
Signal aliases required by this page:  
(NONE)  
BOM options provided by this page:  
(NONE)



GDDR3 Frame Buffer B (Top)  
SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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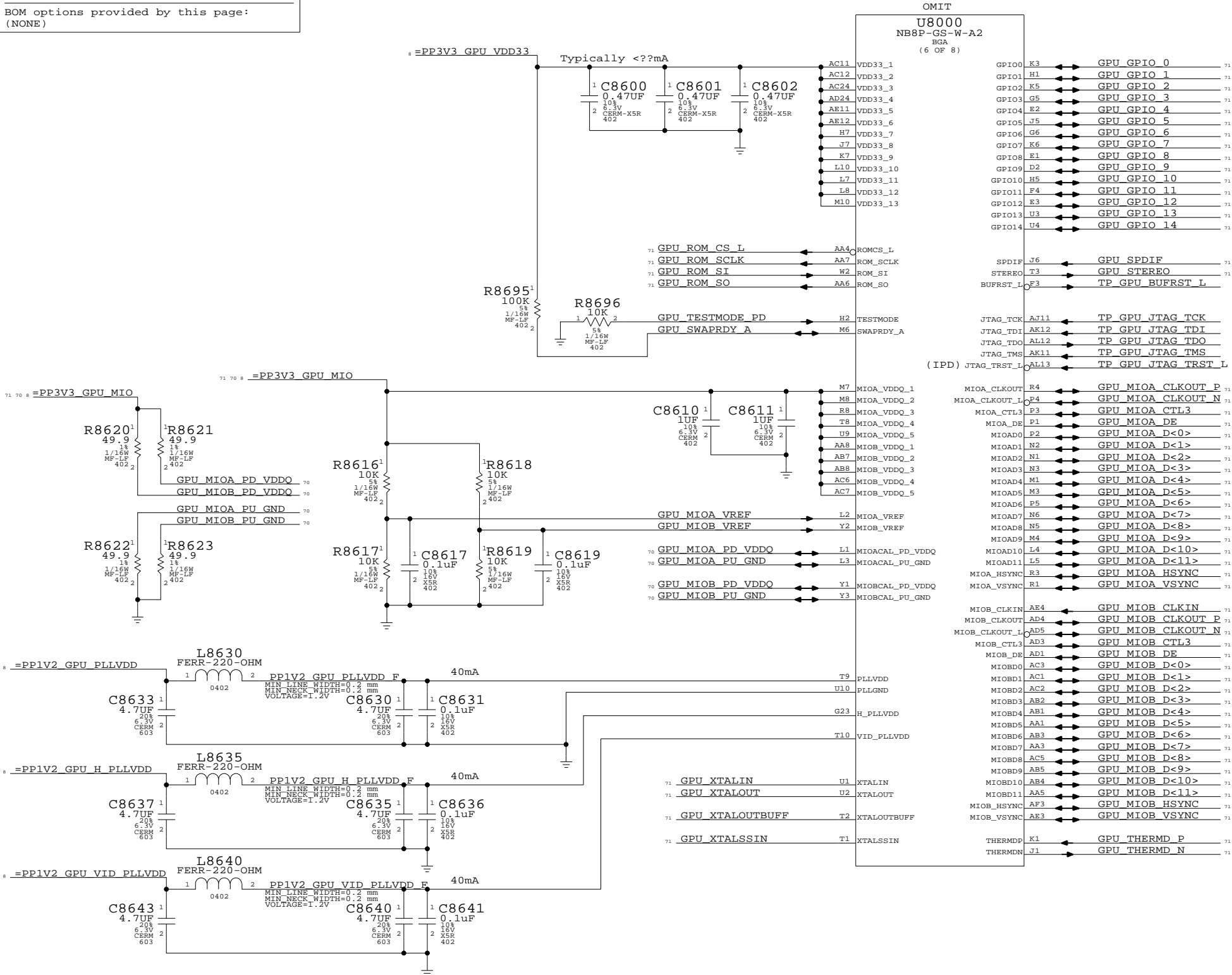
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7413	11.0.0
SCALE	SHT	OF	
NONE	69	89	

# Page Notes

Power aliases required by this page:  
 - =PP3V3\_GPU\_VDD33  
 - =PP3V3\_GPU\_MIO  
 - =PP1V2\_GPU\_PLLVDD  
 - =PP1V2\_GPU\_H\_PLLVDD  
 - =PP1V2\_GPU\_VID\_PLLVDD

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 (NONE)



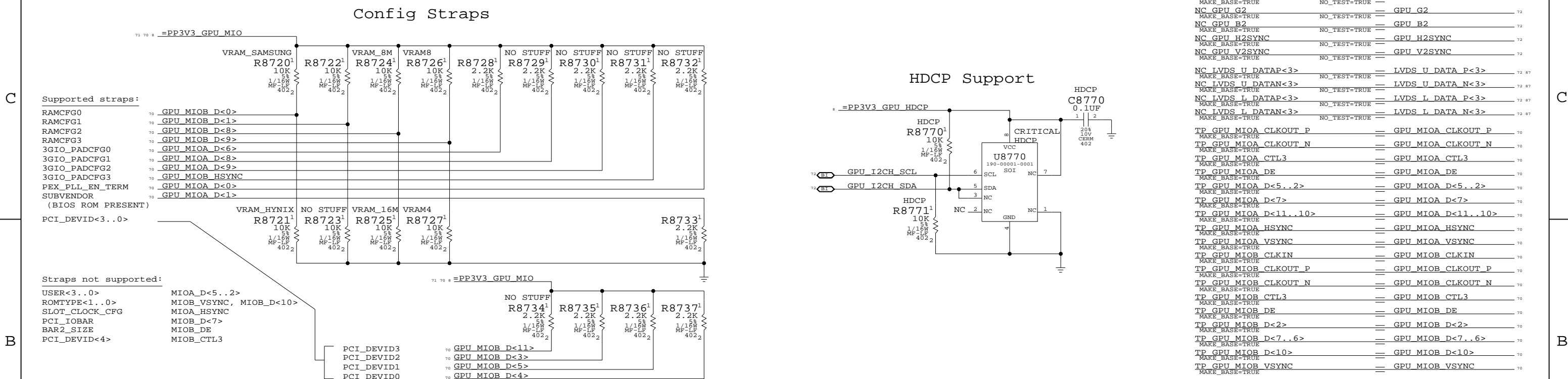
**NV G84M GPIO/MIO/Misc**  
 SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7413	11.0.0
SCALE	SHT	OF	
NONE	70	89	



GPIOs		Renamed signals		Unused signals	
70 GPU GPIO 0	HPD0	GPU HPD	GPU XTALIN	NC GPU XTALOUT	GPU XTALOUT
70 GPU GPIO 1	HPD1	NC GPU GPIO 1	GPU XTALSSIN	NC GPU SPDIF	GPU SPDIF
70 GPU GPIO 2	LCD0_BL_PWM	GPU BL_PWM	GPU THERMD P	NC GPU STEREO	GPU STEREO
70 GPU GPIO 3	LCD0_VDD	GPU PANEL_EN	GPU THERMD N		
70 GPU GPIO 4	LCD0_BL_EN	GPU BKLT_EN	GPU I2CB_SCL		
70 GPU GPIO 5	VID0	TP GPU GSTATE<0>	GPU I2CB_SDA		
70 GPU GPIO 6	VID1	TP GPU GSTATE<1>	GPU I2CC_SCL	NC FBA MA<13>	FB A MA<13>
70 GPU GPIO 7	MEM_VID	GPU VGA_EN L	GPU I2CC_SDA	NC FBB MA<13>	FB B MA<13>
70 GPU GPIO 8	THERM	NC GPU GPIO 8	TP GPU VDD SENSE	NC FBA CMD28	TP FBA CMD28
70 GPU GPIO 9	FAN_PWM	NC GPU GPIO 9	TP GPU GND SENSE	NC FBC CMD28	TP FBC CMD28
70 GPU GPIO 10	MEM_VREF	FB VREF UNTERM			
70 GPU GPIO 11	SLI_SYNC	GPU VCORE VID0			
70 GPU GPIO 12	AC_DET	GPU VCORE VID1			
70 GPU GPIO 13	PWR_CTL0	GPU VCORE VID2			
70 GPU GPIO 14	PWR_CTL1	GPU VCORE VID3			



### GPU Straps

SYNC\_MASTER=M88      SYNC\_DATE=08/02/2007

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7413	11.0.0
SCALE	SHT	OF	
NONE	71	89	

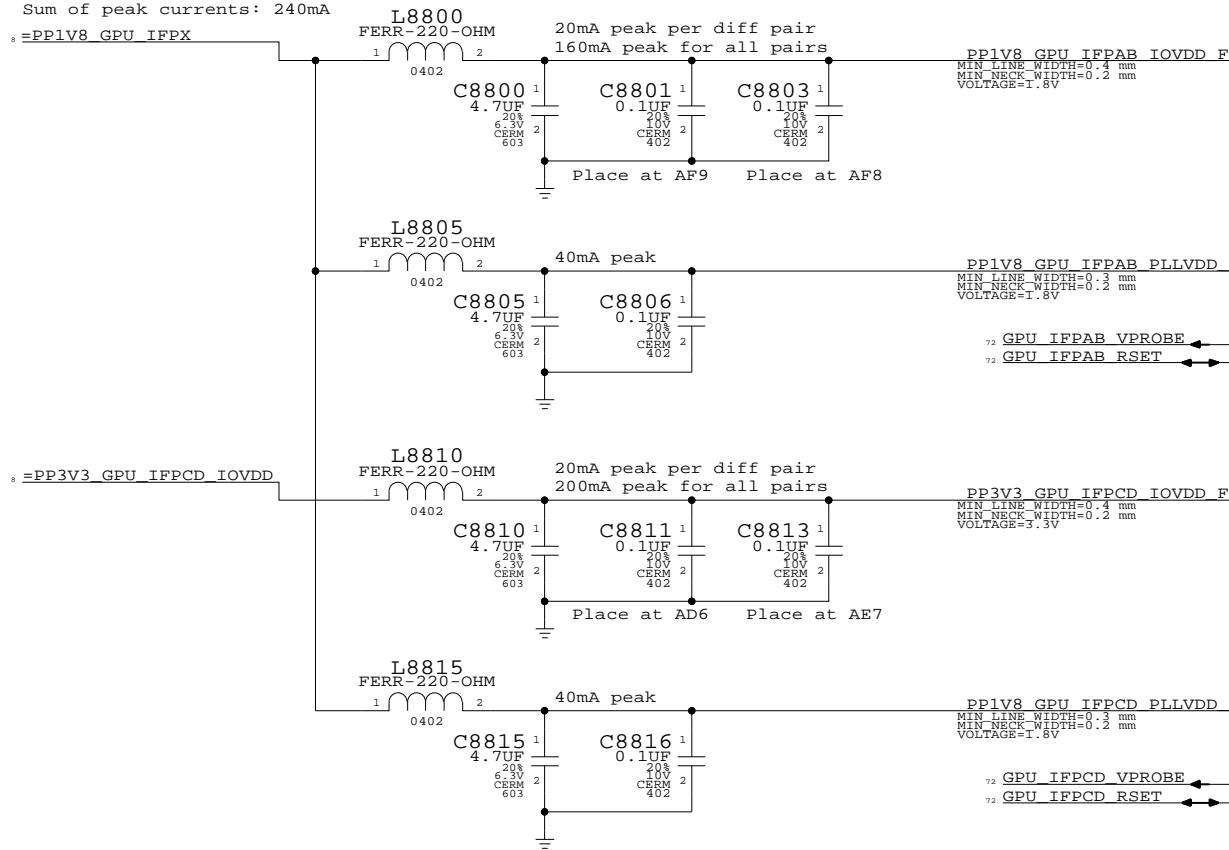
# Page Notes

Power aliases required by this page:  
 - =PP1V8\_GPU\_IFPX  
 - =PP3V3\_GPU\_IFPCD\_IOVDD  
 - =PP3V3\_GPU\_DAC

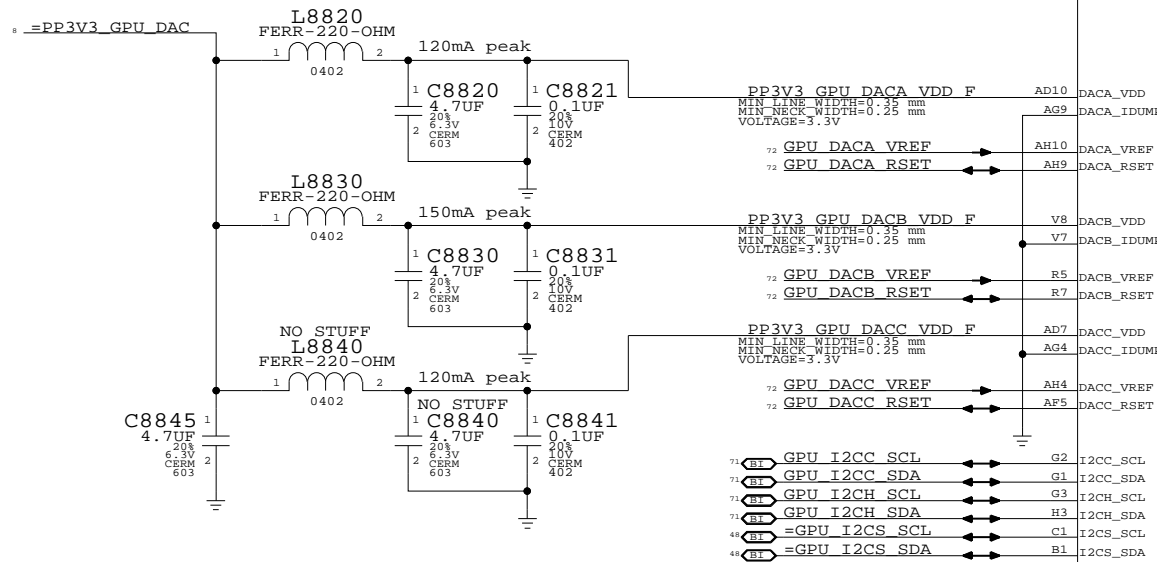
Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 (NONE)

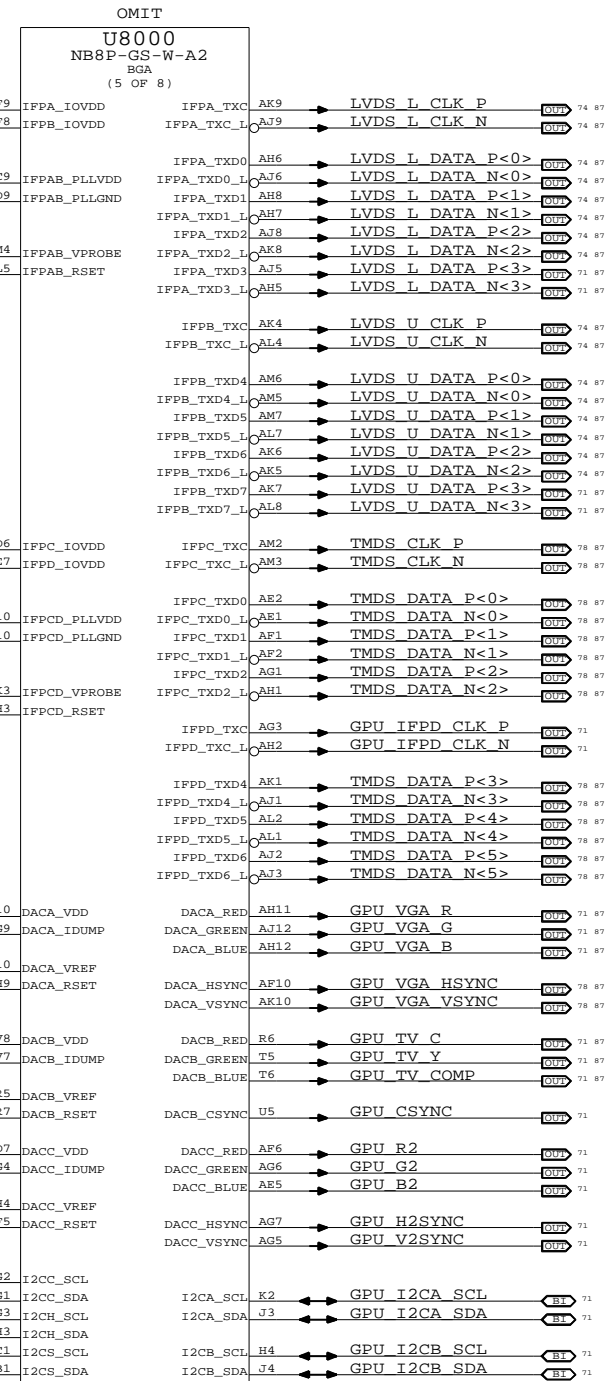
Sum of peak currents: 240mA  
 =PP1V8\_GPU\_IFPX



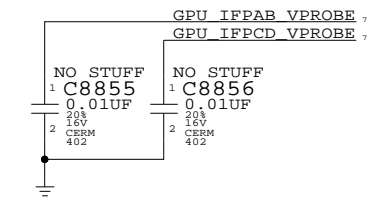
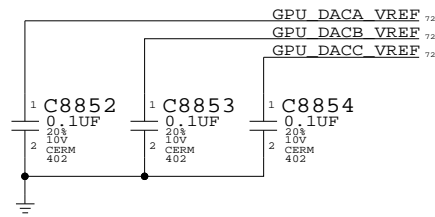
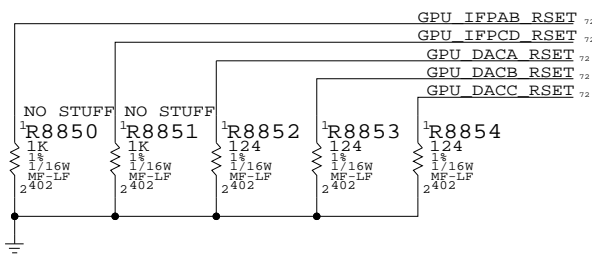
Sum of peak currents: 390mA  
 =PP3V3\_GPU\_DAC



I2CS must be pulled up if not used  
 I2CS addr fixed at 0x9E,0x9F



Composite/S-Video	VGA	Component
C	R	Pr
Y	G	Y
Comp	B	Pb



## NV G84M Video Interfaces

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

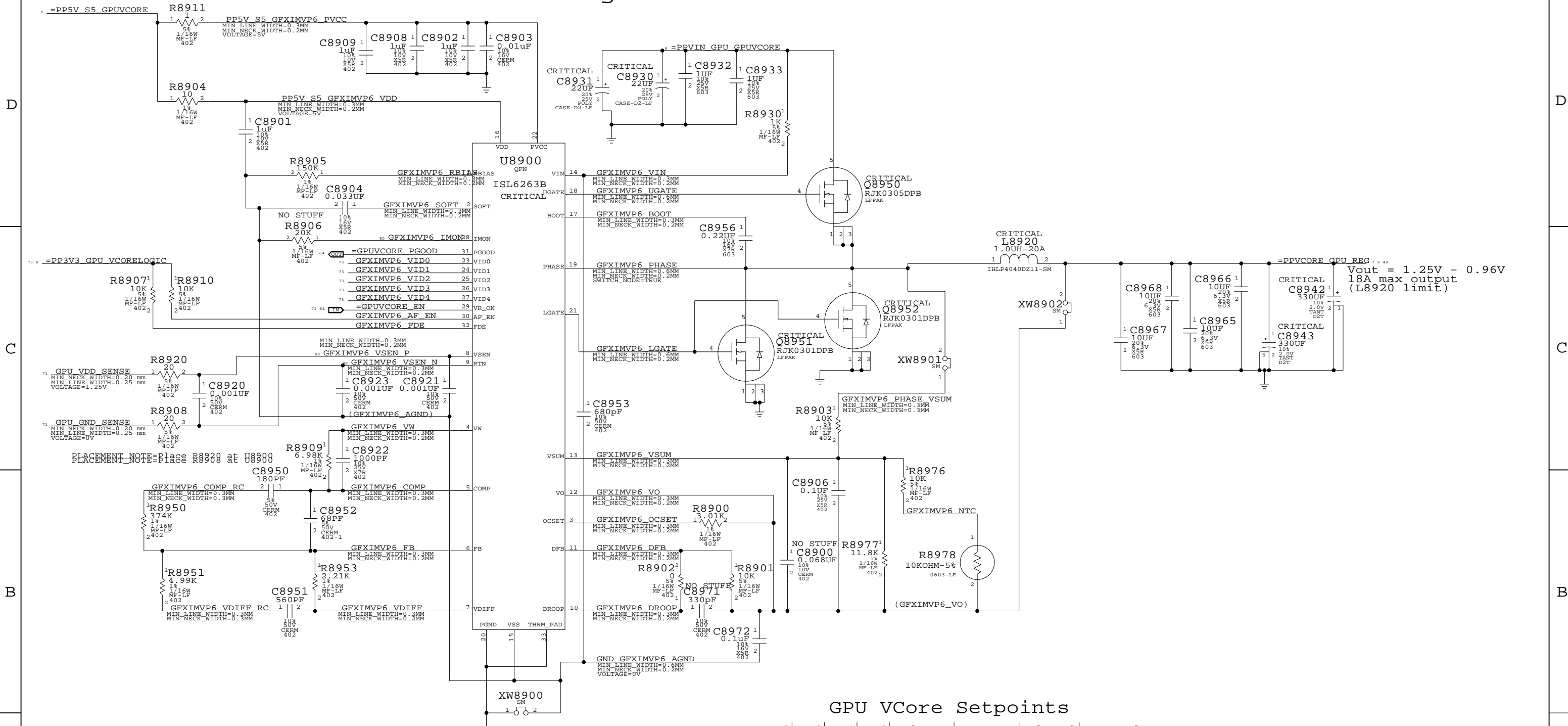
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SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE	SHT	OF
NONE	72	89

# GPU VCore Regulator



## GPU VCore Setpoints

VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	0	0	1	1.05575V	M87, M88	M87	-
0	1	1	0	1.13300V	-	M88	M87
0	0	1	0	1.23600V	-	-	M88

Other VID states may not be valid

## M87/M88 Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_1P26V	GPUVID3_0, GPUVID2_0, GPUVID1_1, GPUVID0_0
GPUVID_1P13V	GPUVID3_0, GPUVID2_1, GPUVID1_1, GPUVID0_0
GPUVID_1P05V	GPUVID3_1, GPUVID2_0, GPUVID1_0, GPUVID0_1

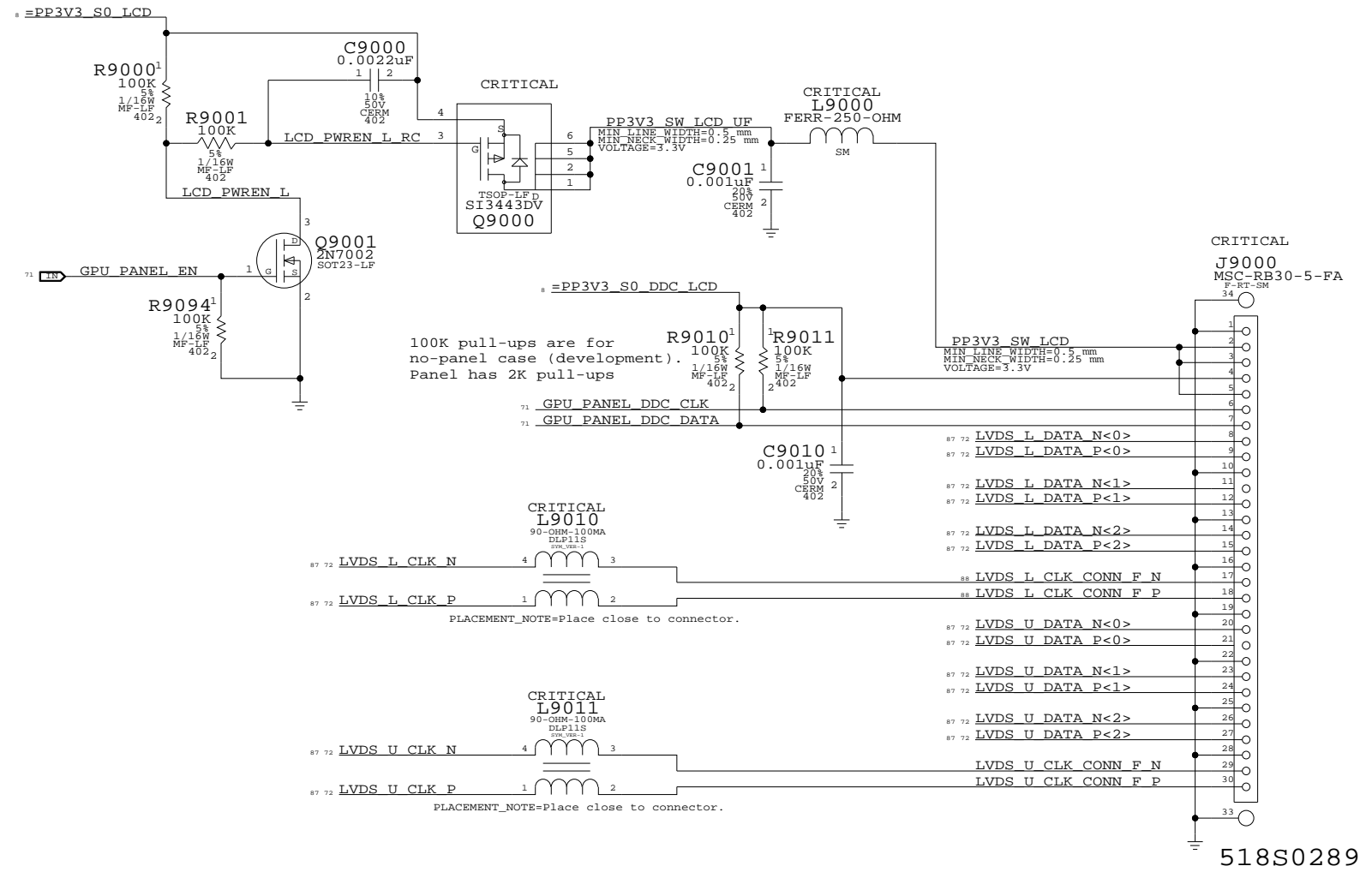
## GPU (G84M) Core Supply

SYNC\_MASTER=M88 SYNC\_DATE=08/02/2007

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	D	051-7413	11.0.0
SCALE	SHT	OF	
NONE	73	89	

# LCD (LVDS) INTERFACE



**LVDS Display Connector**  
 SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)  
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7413	11.0.0
SCALE		SHT	OF
NONE		74	89



Power aliases required by this page:
- =PP1V8\_S0\_FB\_VDD
- =PP1V8\_S0\_FB\_VDDQ
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)



GDDR3 Frame Buffer A (Bot)

SYNC\_MASTER=M88\_MLB\_VRAMSMT\_DATE=06/19/2007

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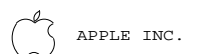
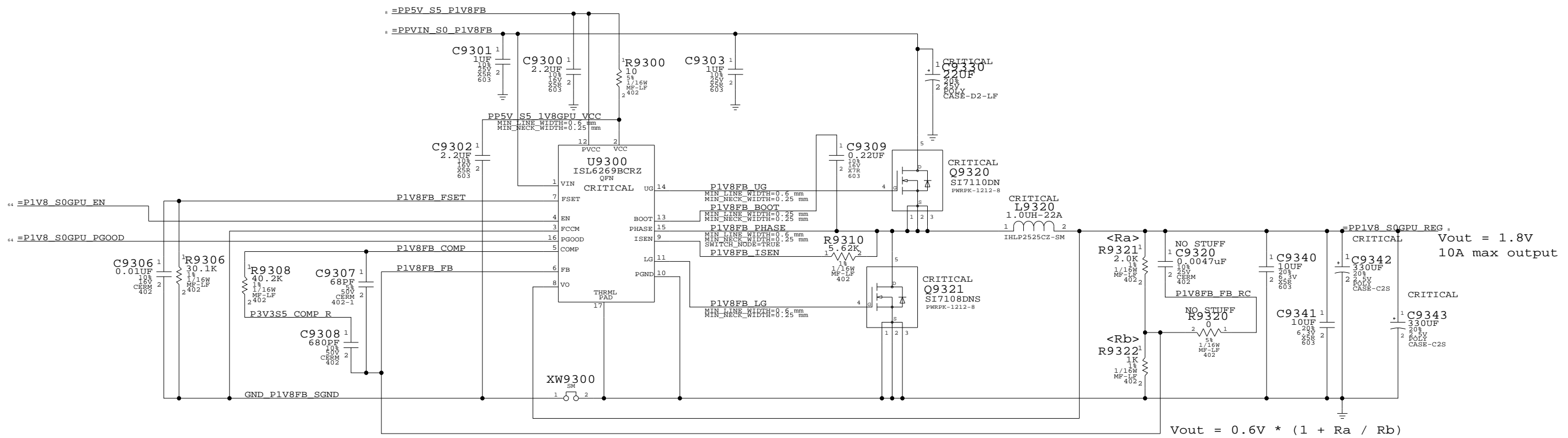


Table with columns: SIZE, DRAWING NUMBER, REV., SCALE, SHEET, OF, REV. Values: D, 051-7413, 11.0.0, NONE, 75, OF, 89





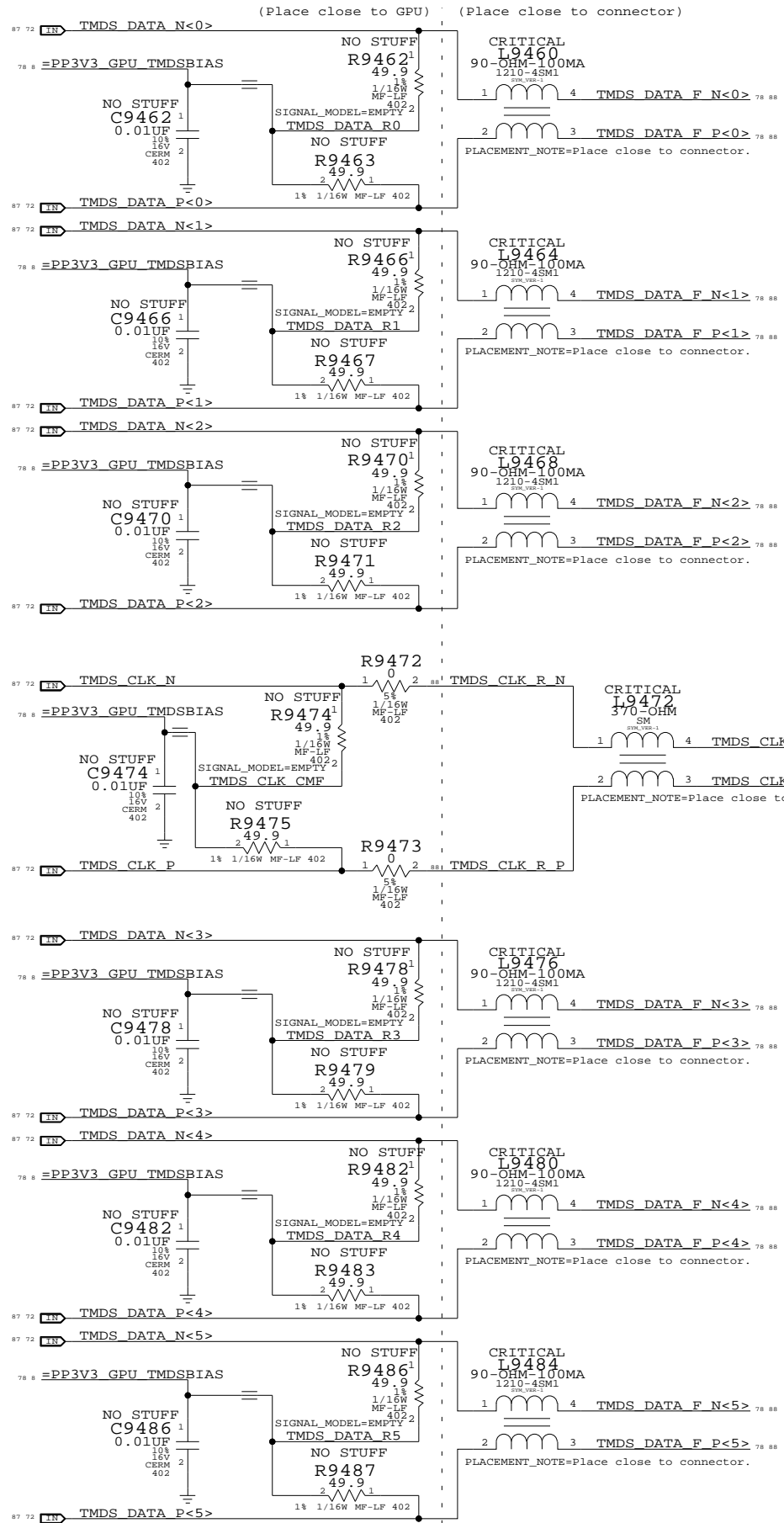
# 1.8V Frame Buffer Regulator



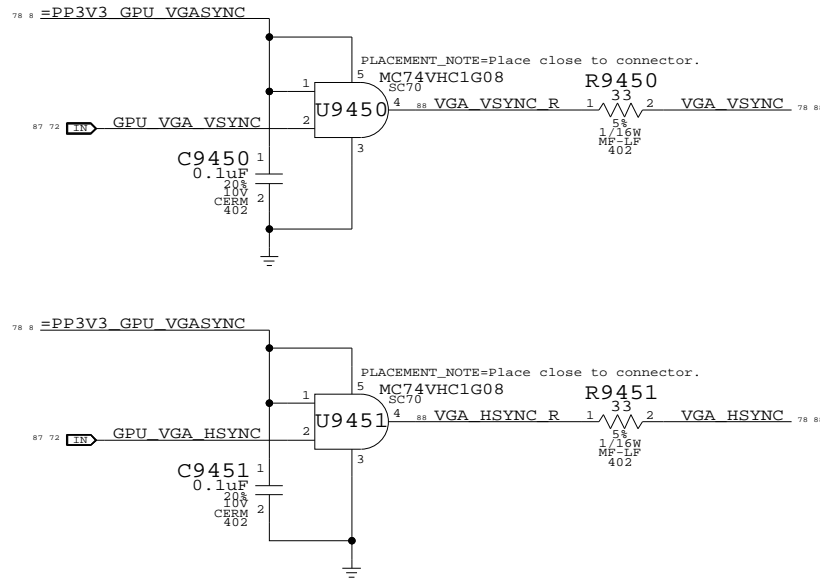
**1.8V FB Power Supply**  
 SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)  
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7413	11.0.0
SCALE	SHT 77 OF 89		
NONE			

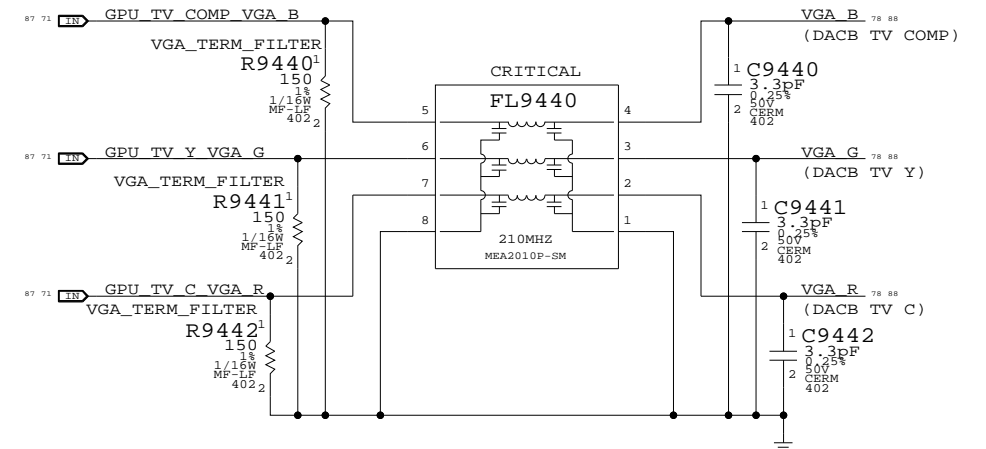
# TMDS Filtering



# VGA SYNC Buffers

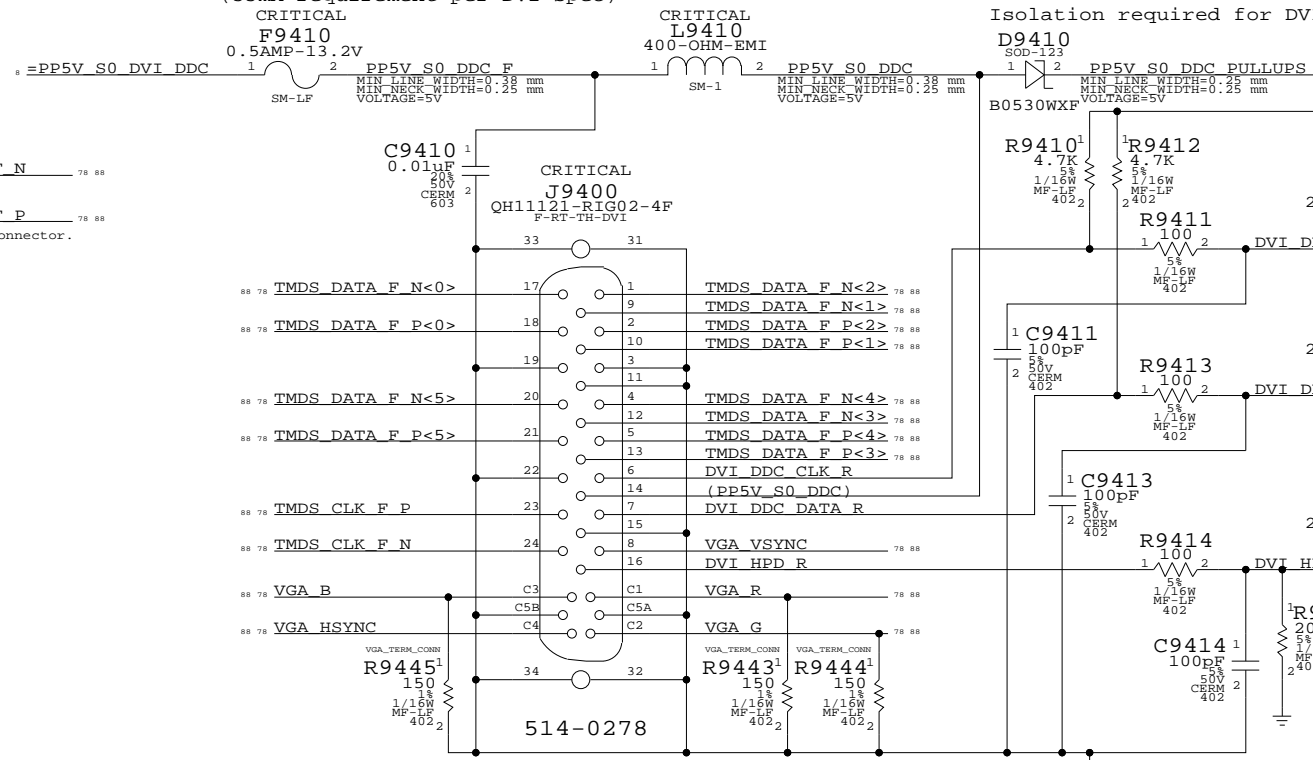


# ANALOG FILTERING PLACE CLOSE TO CONNECTOR

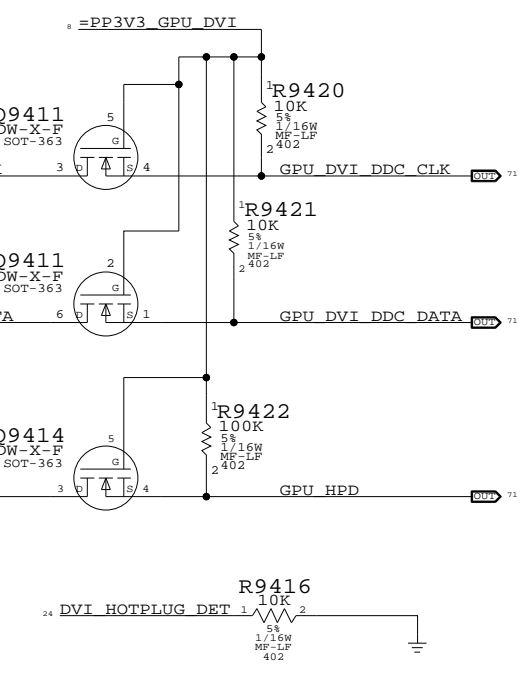


# DVI INTERFACE

## DVI DDC Current Limit (55mA requirement per DVI spec)



## GPU Isolation / Level-Shift



**DVI Display Connector**

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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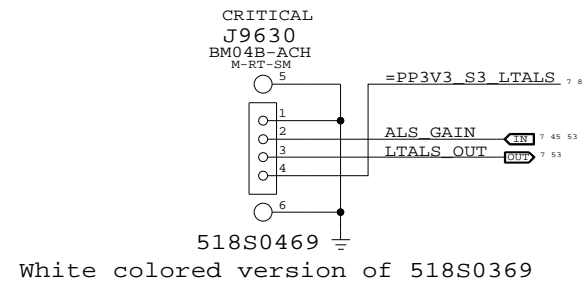
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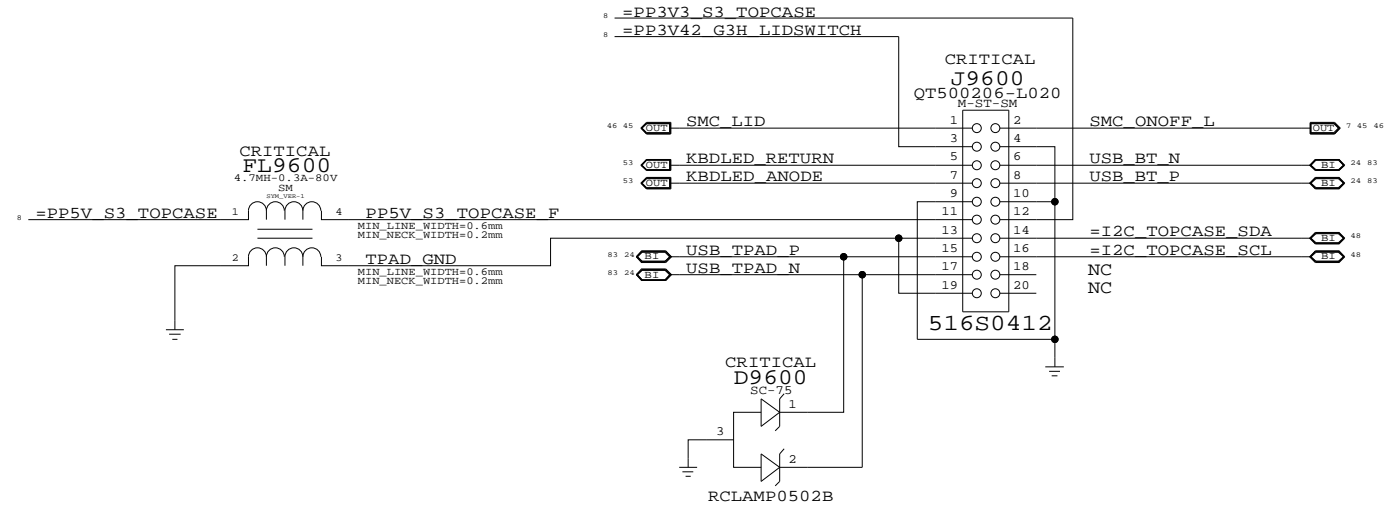
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7413	11.0.0
SCALE	SHT	OF	
NONE	78	89	

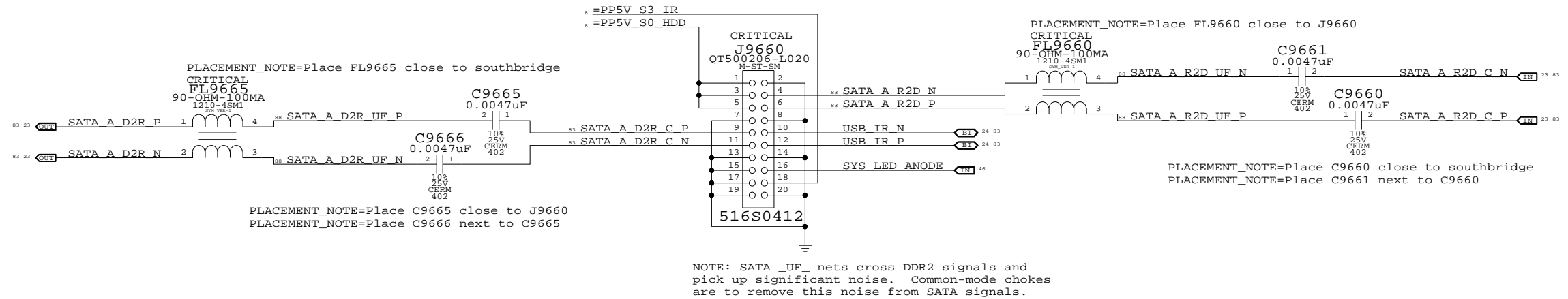
### Left ALS Connector



### Top-Case Connector



### SATA HDD & IR & SIL Flex Connector



Project Specific Connectors  
 SYNC\_MASTER=(M59\_SYNC) SYNC\_DATE=08/24/2006

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	D	051-7413	11.0.0
SCALE	SHT 79 OF 89		
NONE			

### FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	?
FSB_ADDR2ADDR	*	=2:1_SPACING	?
FSB_ADSTB	*	=3:1_SPACING	?
FSB_ADDR2ADSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=3:1_SPACING	?
FSB_DATA2DATA	*	=2:1_SPACING	?
FSB_DSTB	*	=3:1_SPACING	?
FSB_DATA2DSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended. Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs. Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs. DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group is routed on the same layer. Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1. NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

### CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2T01	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance.

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

### CPU / FSB Net Properties

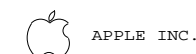
ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FSB_COMMON	FSB_55S	FSB_COMMON	FSB ADS L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB BNR L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB BPRI L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB BRQ0 L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DBSY L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DEFER L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DPWR L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DRDY L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB HIT L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB HITM L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB LOCK L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB RS L<2..0>	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB TRDY L	10 14
FSB_CPURST_L	FSB_55S	FSB_COMMON	FSB CPURST L	7 10 13 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB D L<15..0>	7 10 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB DINV L<0>	7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<0>	7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<0>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB D L<31..16>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB DINV L<1>	7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<1>	7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<1>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB D L<47..32>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB DINV L<2>	7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<2>	7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<2>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB D L<63..48>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB DINV L<3>	7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<3>	7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB A L<16..3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB REQ L<4..0>	7 10 14
FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB ADSTB L<0>	7 10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB A L<35..17>	7 10 14
FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB ADSTB L<1>	7 10 14
CPU_IERR_L	CPU_55S		CPU IERR L	10
CPU_FERR_L	CPU_55S		CPU FERR L	10 23
CPU_PROCHOT_L	CPU_55S	CPU_2T01	CPU PROCHOT L	10 46 58
CPU_PWRGD	CPU_55S		CPU PWRGD	7 10 13 23
CPU_FRGM_SB	CPU_55S		CPU INTR	10 23
CPU_FRGM_SB	CPU_55S		CPU NMI	10 23
CPU_FRGM_SB	CPU_55S		CPU A20M L	10 23
CPU_FRGM_SB	CPU_55S		CPU DPSTP L	7 10 23
CPU_FRGM_SB	CPU_55S		CPU IGNE L	10 23
CPU_INIT_L	CPU_55S		CPU INIT L	10 23 47
CPU_FRGM_SB	CPU_55S		CPU SMI L	10 23
CPU_FRGM_SB	CPU_55S		CPU STPCLK L	7 10 23
PM_THRMTRIP_L	CPU_55S	CPU_2T01	PM THRMTRIP L	10 16 23 46
FSB_CPUSLP_L	CPU_55S		FSB CPUSLP L	7 10 14
PM_DPRSLEVR	CPU_55S	CPU_2T01	PM DPRSLPVR	7 16 25 58
(See above)	CPU_55S	CPU_2T01	IMVP DPRSLPVR	7 8
CPU_BSEL0	CPU_55S	CPU_2T01	CPU BSEL<0>	10 30
(See above)	CPU_55S	CPU_2T01	NB BSEL<0>	13 16 30
CPU_BSEL1	CPU_55S	CPU_2T01	CPU BSEL<1>	10 30
(See above)	CPU_55S	CPU_2T01	NB BSEL<1>	13 16 30
CPU_BSEL2	CPU_55S	CPU_2T01	CPU BSEL<2>	10 30
(See above)	CPU_55S	CPU_2T01	NB BSEL<2>	13 16 30
CPU_DPRSTP_L	CPU_55S	CPU_2T01	CPU DPRSTP L	7 10 16 23 58
CPU_GTLREF	CPU_55S	CPU_GTLREF	CPU GTLREF	10
CPU_COMP	CPU_55S	CPU_COMP	CPU COMP<3>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2>	10
CPU_COMP	CPU_55S	CPU_COMP	CPU COMP<1>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0>	10
XDP_TDI	CPU_55S	CPU_ITP	XDP TDI	10 13
XDP_TDO	CPU_55S	CPU_ITP	XDP TDO	10 13
XDP_TMS	CPU_55S	CPU_ITP	XDP TMS	10 13
XDP_TCK	CPU_55S	CPU_ITP	XDP TCK	10 13
XDP_TEST_L	CPU_55S	CPU_ITP	XDP TRST L	10 13
XDP_BPM_L	CPU_55S	CPU_ITP	XDP BPM L<4..0>	10 13
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP BPM L<5>	10 13
CLK_FSB_1000	CLK_FSB	CLK_FSB	XDP CLK P	13 30 85
CLK_FSB_1000	CLK_FSB	CLK_FSB	XDP CLK N	13 30 85
(FSB_CPURST_L)	CPU_55S	CPU_ITP	XDP CPURST L	13
	CPU_55S	CPU_2T01	CPU VID<6..0>	11 12
	CPU_55S	CPU_2T01	IMVP6 VID<6..0>	7 12 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P	11 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N	11 58
	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN P	58
	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN N	58

### CPU/FSB Constraints

SYNC\_MASTER=T9\_NOME SYNC\_DATE=01/17/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE	SHT	OF
NONE	80	89

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
DMI	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CRT_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS	*	20 MIL	?
CRT	*	25 MIL	?
CRT_2CRT	*	20 MIL	?
CRT_SYNC	*	25 MIL	?
CRT_SYNC2SYNC	*	20 MIL	?
TVDAC	*	25 MIL	?
TVDAC_2TVDAC	*	20 MIL	?

DG Says 40 mil spacing minimum

DG Says 30 mil spacing minimum

DG Says 40 mil spacing minimum

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT
CRT_SYNC	CRT_SYNC	*	CRT_SYNC2SYNC
TVDAC	TVDAC	*	TVDAC_2TVDAC

LVDS signals are 100-ohm +/- 20% differential impedance.  
 CRT & TVDAC signal single-ended impedance varies by location:  
 - 37.5-ohm +/- 15% from GMCH to first termination resistor.  
 - 50-ohm +/- 15% from first to second termination resistor.  
 - 55-ohm +/- 15% from second termination resistor to connector.  
 CRT\_HSYNC/CRT\_VSYNC signals are 55-ohm +/- 15% single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
PEG_R2D	PCIE_100D	PCIE	PEG R2D P<15..0> 65
	PCIE_100D	PCIE	PEG R2D N<15..0> 65
	PCIE_100D	PCIE	PEG R2D C P<15..0> 15 65
	PCIE_100D	PCIE	PEG R2D C N<15..0> 15 65
PEG_D2R	PCIE_100D	PCIE	PEG D2R P<15..0> 15 65
	PCIE_100D	PCIE	PEG D2R N<15..0> 15 65
	PCIE_100D	PCIE	PEG D2R C P<15..0> 65
	PCIE_100D	PCIE	PEG D2R C N<15..0> 65
DMI_N2S	DMI_100D	DMI	DMI N2S P<3..0> 16 24
	DMI_100D	DMI	DMI N2S N<3..0> 16 24
DMI_S2N	DMI_100D	DMI	DMI S2N P<3..0> 16 24
	DMI_100D	DMI	DMI S2N N<3..0> 16 24
LVDS_A_CLK	LVDS_100D	LVDS	LVDS A CLK P 15 22
LVDS_A_CLK	LVDS_100D	LVDS	LVDS A CLK N 15 22
LVDS_A_DATA	LVDS_100D	LVDS	LVDS A DATA P<2..0> 15 22
LVDS_A_DATA	LVDS_100D	LVDS	LVDS A DATA N<2..0> 15 22
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS A DATA P<3> 15 22
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS A DATA N<3> 15 22
LVDS_B_CLK	LVDS_100D	LVDS	LVDS B CLK P 15 22
LVDS_B_CLK	LVDS_100D	LVDS	LVDS B CLK N 15 22
LVDS_B_DATA	LVDS_100D	LVDS	LVDS B DATA P<2..0> 15 22
LVDS_B_DATA	LVDS_100D	LVDS	LVDS B DATA N<2..0> 15 22
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS B DATA P<3> 15 22
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS B DATA N<3> 15 22
LVDS_IBG		LVDS	LVDS IBG 15 22
CRT_TVO_IREF		CRT	CRT TVO IREF
CRT_RED	CRT_50S	CRT	CRT RED
CRT_GREEN	CRT_50S	CRT	CRT GREEN
CRT_BLUE	CRT_50S	CRT	CRT BLUE
CRT_SYNC	CRT_55S	CRT_SYNC	CRT HSYNC R
CRT_SYNC	CRT_55S	CRT_SYNC	CRT VSYNC R
TV_A_DAC	CRT_50S	TVDAC	TV A DAC
TV_B_DAC	CRT_50S	TVDAC	TV B DAC
TV_C_DAC	CRT_50S	TVDAC	TV C DAC

NB Constraints

SYNC\_MASTER=T9\_NOME SYNC\_DATE=01/17/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE	SHT	OF
NONE	81	89



### DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

Need to support MEM\_\*-style wildcards!  
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

### Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PROPERTY	VALUE
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_CLK P<2..0>	16 31
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_CLK N<2..0>	16 31
MEM_A_CNTRL	MEM_45S	MEM_CTRL	MEM_CKE<1..0>	16 31 33
MEM_A_CNTRL	MEM_45S	MEM_CTRL	MEM_CS L<1..0>	16 31 33
MEM_A_CNTRL	MEM_45S	MEM_CTRL	MEM_ODT<1..0>	16 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A A<14..0>	16 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A BS<2..0>	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A RAS L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A CAS L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A WE L	17 31 33
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM A DQ<7..0>	17 31
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM A DQ<15..8>	17 31
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM A DQ<23..16>	17 31
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM A DQ<31..24>	17 31
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM A DQ<39..32>	17 31
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM A DQ<47..40>	17 31
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM A DQ<55..48>	17 31
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM A DQ<63..56>	17 31
MEM_A_DM0	MEM_55S	MEM_DATA	MEM A DM<0>	17 31
MEM_A_DM1	MEM_55S	MEM_DATA	MEM A DM<1>	17 31
MEM_A_DM2	MEM_55S	MEM_DATA	MEM A DM<2>	17 31
MEM_A_DM3	MEM_55S	MEM_DATA	MEM A DM<3>	17 31
MEM_A_DM4	MEM_55S	MEM_DATA	MEM A DM<4>	17 31
MEM_A_DM5	MEM_55S	MEM_DATA	MEM A DM<5>	17 31
MEM_A_DM6	MEM_55S	MEM_DATA	MEM A DM<6>	17 31
MEM_A_DM7	MEM_55S	MEM_DATA	MEM A DM<7>	17 31
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS P<0>	17 31
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS N<0>	17 31
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS P<1>	17 31
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS N<1>	17 31
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS P<2>	17 31
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS N<2>	17 31
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS P<3>	17 31
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS N<3>	17 31
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS P<4>	17 31
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS N<4>	17 31
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS P<5>	17 31
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS N<5>	17 31
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS P<6>	17 31
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS N<6>	17 31
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS P<7>	17 31
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS N<7>	17 31
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_CLK P<5..3>	16 32
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_CLK N<5..3>	16 32
MEM_B_CNTRL	MEM_45S	MEM_CTRL	MEM_CKE<4..3>	16 32 33
MEM_B_CNTRL	MEM_45S	MEM_CTRL	MEM CS L<3..2>	16 32 33
MEM_B_CNTRL	MEM_45S	MEM_CTRL	MEM_ODT<3..2>	16 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B A<14..0>	16 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B BS<2..0>	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B RAS L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B CAS L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B WE L	17 32 33
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM B DQ<7..0>	17 32
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM B DQ<15..8>	17 32
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM B DQ<23..16>	17 32
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM B DQ<31..24>	17 32
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM B DQ<39..32>	17 32
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM B DQ<47..40>	17 32
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM B DQ<55..48>	17 32
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM B DQ<63..56>	17 32
MEM_B_DM0	MEM_55S	MEM_DATA	MEM B DM<0>	17 32
MEM_B_DM1	MEM_55S	MEM_DATA	MEM B DM<1>	17 32
MEM_B_DM2	MEM_55S	MEM_DATA	MEM B DM<2>	17 32
MEM_B_DM3	MEM_55S	MEM_DATA	MEM B DM<3>	17 32
MEM_B_DM4	MEM_55S	MEM_DATA	MEM B DM<4>	17 32
MEM_B_DM5	MEM_55S	MEM_DATA	MEM B DM<5>	17 32
MEM_B_DM6	MEM_55S	MEM_DATA	MEM B DM<6>	17 32
MEM_B_DM7	MEM_55S	MEM_DATA	MEM B DM<7>	17 32
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS P<0>	17 32
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS N<0>	17 32
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS P<1>	17 32
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS N<1>	17 32
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS P<2>	17 32
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS N<2>	17 32
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS P<3>	17 32
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS N<3>	17 32
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS P<4>	17 32
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS N<4>	17 32
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS P<5>	17 32
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS N<5>	17 32
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS P<6>	17 32
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS N<6>	17 32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS P<7>	17 32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS N<7>	17 32

**Memory Constraints**  
 SYNC\_MASTER=T9\_NOME    SYNC\_DATE=01/17/2007

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7413	11.0.0
SCALE	SHT	OF	
NONE	82	89	



### Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

### HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

### USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_60S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	20 MIL	?
USB_2CLK	*	25 MIL	?

DG says minimum spacing 50 mils to clocks

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.13.2

### Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

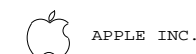
ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
IDE_PDD	IDE_55S	IDE	IDE_PDD<15..0> 23 42
IDE_PDA	IDE_55S	IDE	IDE_PDA<2..0> 23 42
IDE_PDCS	IDE_55S	IDE	IDE_PDCS1 L 23 42
IDE_PDCCS	IDE_55S	IDE	IDE_PDCCS3 L 23 42
IDE_CNVL	IDE_55S	IDE	IDE_PDIOW L 23 42
IDE_PDIOR_L	IDE_55S	IDE	IDE_PDIOR L 23 42
IDE_CNVL	IDE_55S	IDE	IDE_PDDACK L 23 42
IDE_CNVL	IDE_55S	IDE	IDE_PDDREO 23 42
IDE_PDIORDY	IDE_55S	IDE	IDE_PDIORDY 23 42
IDE_IRQ14	IDE_55S	IDE	IDE_IRQ14 23 42
IDE_RST_L	IDE_55S	IDE	ODD_RST_5VTOL L 24 42
SATA_A_R2D	SATA_100D	SATA	SATA_A_R2D C P 23 79
SATA_100D	SATA	SATA	SATA_A_R2D C N 23 79
SATA_100D	SATA	SATA	SATA_A_R2D P 79
SATA_100D	SATA	SATA	SATA_A_R2D N 79
SATA_A_D2R	SATA_100D	SATA	SATA_A_D2R P 23 79
SATA_100D	SATA	SATA	SATA_A_D2R N 23 79
SATA_100D	SATA	SATA	SATA_A_D2R C P 79
SATA_100D	SATA	SATA	SATA_A_D2R C N 79
SATA_B_R2D	SATA_100D	SATA	SATA_B_R2D C P 23 42
SATA_100D	SATA	SATA	SATA_B_R2D C N 23 42
SATA_100D	SATA	SATA	SATA_B_R2D P 23 42
SATA_100D	SATA	SATA	SATA_B_R2D N 23 42
SATA_B_D2R	SATA_100D	SATA	SATA_B_D2R P 23 42
SATA_100D	SATA	SATA	SATA_B_D2R N 23 42
SATA_100D	SATA	SATA	SATA_B_D2R C P 23 42
SATA_100D	SATA	SATA	SATA_B_D2R C N 23 42
SATA_C_R2D	SATA_100D	SATA	SATA_C_R2D C P 23 42
SATA_100D	SATA	SATA	SATA_C_R2D C N 23 42
SATA_100D	SATA	SATA	SATA_C_R2D P 23 42
SATA_100D	SATA	SATA	SATA_C_R2D N 23 42
SATA_C_D2R	SATA_100D	SATA	SATA_C_D2R P 23 42
SATA_100D	SATA	SATA	SATA_C_D2R N 23 42
SATA_100D	SATA	SATA	SATA_C_D2R C P 23 42
SATA_100D	SATA	SATA	SATA_C_D2R C N 23 42
SATA_RBIAS	SATA_55S	SATA	SATA_RBIAS 42
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK 23 34
HDA_55S	HDA	HDA	HDA_BIT_CLK R 23 34
HDA_SYNC	HDA_55S	HDA	HDA_SYNC 23 34
HDA_55S	HDA	HDA	HDA_SYNC R 23 34
HDA_RST_L	HDA_55S	HDA	HDA_RST L 23 34
HDA_55S	HDA	HDA	HDA_RST L R 23 34
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0 23 34
HDA_55S	HDA	HDA	HDA_SDIN CODEC 23 34
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT 23 34
HDA_55S	HDA	HDA	HDA_SDOUT R 23 34
USB_EXT_A	USB_90D	USB	USB_EXT_A P 24 43
USB_90D	USB	USB	USB_EXT_A N 24 43
USB_90D	USB	USB	USB_EXT_A MUXED P 24 43
USB_90D	USB	USB	USB_EXT_A MUXED N 24 43
USB_MINI	USB_90D	USB	USB_MINI P 24 34
USB_90D	USB	USB	USB_MINI N 24 34
USB_EXTD	USB_90D	USB	USB_EXTD P 9 24
USB_90D	USB	USB	USB_EXTD N 9 24
USB_CAMERA	USB_90D	USB	USB_CAMERA P 7 24 44
USB_90D	USB	USB	USB_CAMERA N 7 24 44
USB_BT	USB_90D	USB	USB_BT P 24 79
USB_90D	USB	USB	USB_BT N 24 79
USB_TPAD	USB_90D	USB	USB_TPAD P 24 79
USB_90D	USB	USB	USB_TPAD N 24 79
USB_IR	USB_90D	USB	USB_IR P 24 79
USB_90D	USB	USB	USB_IR N 24 79
USB_EXTB	USB_90D	USB	USB_EXTB P 24 34
USB_90D	USB	USB	USB_EXTB N 24 34
USB_EXCARD	USB_90D	USB	USB_EXCARD P 24 34
USB_90D	USB	USB	USB_EXCARD N 24 34
USB_EXTC	USB_90D	USB	USB_EXTC P 9 24
USB_90D	USB	USB	USB_EXTC N 9 24
USB_RBIAS	USB_60S	USB	USB_RBIAS 24
SMB_SB_SCL	SMB_55S	SMB	SMB_CLK 25 48
SMB_SB_SDA	SMB_55S	SMB	SMB_DATA 25 48
SMB_SB_ME_SCL	SMB_55S	SMB	SMB_ME_CLK 25 48
SMB_SB_ME_SDA	SMB_55S	SMB	SMB_ME_DATA 25 48
SPI_SCLK	SPI_55S	SPI	SPI_SCLK_R 24 55
SPI_55S	SPI	SPI	SPI_SCLK 55
SPI_55S	SPI	SPI	SPI_A_SCLK_R 55
SPI_55S	SPI	SPI	SPI_B_SCLK_R 55
SPI_SI	SPI_55S	SPI	SPI_SI_R 24 55
SPI_55S	SPI	SPI	SPI_SI 55
SPI_55S	SPI	SPI	SPI_A_SI_R 55
SPI_55S	SPI	SPI	SPI_B_SI_R 55
SPI_SO	SPI_55S	SPI	SPI_SO 24 55
SPI_55S	SPI	SPI	SPI_A_SO_R 55
SPI_55S	SPI	SPI	SPI_B_SO_R 55
SPI_55S	SPI	SPI	SPI_B_SO_R 55
SPI_CE_L0	SPI_55S	SPI	SPI_CE_R L<0> 24 55
SPI_55S	SPI	SPI	SPI_CE L<0> 55
SPI_CE_L1	SPI_55S	SPI	SPI_CE_R L<1> 55
SPI_55S	SPI	SPI	SPI_CE L<1> 55

### SB Constraints (1 of 2)

SYNC\_MASTER=T9\_NOME SYNC\_DATE=01/17/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE	SHT	OF
NONE	83	89

### PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

### Controller Link (AMT) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLINK_12MIL	*	=STANDARD	12 MILS	5 MILS	300 MILS	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLINK	*	=1.8:1_SPACING	?
CLINK_VREF	*	12 MILS	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

### Ethernet (Yukon) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MILS	?

SOURCE: Based on Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

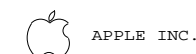
ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
PCI_AD	PCI_55S	PCI	PCI AD<18..0>	24 38
PCI_AD19	PCI_55S	PCI	PCI AD<19>	24 38
PCI_AD20	PCI_55S	PCI	PCI AD<20>	24 38
PCI_AD	PCI_55S	PCI	PCI AD<31..21>	24 38
PCI_AD	PCI_55S	PCI	PCI PAR	24 38
PCI_C_BE_L	PCI_55S	PCI	PCI C BE L<3..0>	24 38
PCI_CNTRL	PCI_55S	PCI	PCI IRDY_L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI DEVSEL_L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI PERR_L	24 38
PCI_LOCK_L	PCI_55S	PCI	PCI LOCK_L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI SERR_L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI STOP_L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI TRDY_L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI FRAME_L	24 38
PCI_FW_REQ_L	PCI_55S	PCI	PCI FW REQ_L	24 38
PCI_FW_GNT_L	PCI_55S	PCI	PCI FW GNT_L	24 38
PCI_REQ1_L	PCI_55S	PCI	PCI REQ1_L	24 38
PCI_GNT1_L	PCI_55S	PCI	PCI GNT1_L	24 38
PCI_REQ2_L	PCI_55S	PCI	PCI REQ2_L	24 38
PCI_GNT2_L	PCI_55S	PCI	PCI GNT2_L	24 38
INT_PIRQA_L	PCI_55S	PCI	INT PIRQA_L	24 38
INT_PIRQB_L	PCI_55S	PCI	INT PIRQB_L	24 38
INT_PIRQC_L	PCI_55S	PCI	INT PIRQC_L	24 38
INT_PIRQD_L	PCI_55S	PCI	INT PIRQD_L	24 38
INT_PIRQE_L	PCI_55S	PCI	INT PIRQE_L	24 38
INT_PIRQF_L	PCI_55S	PCI	INT PIRQF_L	24 38
PCIE_A_R2D	PCIE_100D	PCIE	PCIE A R2D C P	24 34
PCIE_A_R2D	PCIE_100D	PCIE	PCIE A R2D C N	24 34
PCIE_A_D2R	PCIE_100D	PCIE	PCIE A D2R P	24 34
PCIE_A_D2R	PCIE_100D	PCIE	PCIE A D2R N	24 34
PCIE_B_R2D	PCIE_100D	PCIE	PCIE B R2D C P	24 34
PCIE_B_R2D	PCIE_100D	PCIE	PCIE B R2D C N	24 34
PCIE_B_D2R	PCIE_100D	PCIE	PCIE B D2R P	24 34
PCIE_B_D2R	PCIE_100D	PCIE	PCIE B D2R N	24 34
PCIE_EXCARD_R2D	PCIE_100D	PCIE	PCIE EXCARD R2D C P	24 34
PCIE_EXCARD_R2D	PCIE_100D	PCIE	PCIE EXCARD R2D C N	24 34
PCIE_EXCARD_D2R	PCIE_100D	PCIE	PCIE EXCARD D2R P	24 34
PCIE_EXCARD_D2R	PCIE_100D	PCIE	PCIE EXCARD D2R N	24 34
PCIE_FW_R2D	PCIE_100D	PCIE	PCIE FW R2D C P	24 34
PCIE_FW_R2D	PCIE_100D	PCIE	PCIE FW R2D C N	24 34
PCIE_FW_D2R	PCIE_100D	PCIE	PCIE FW D2R P	24 34
PCIE_FW_D2R	PCIE_100D	PCIE	PCIE FW D2R N	24 34
PCIE_MINI_R2D	PCIE_100D	PCIE	PCIE MINI R2D C P	24 34
PCIE_MINI_R2D	PCIE_100D	PCIE	PCIE MINI R2D C N	24 34
PCIE_MINI_D2R	PCIE_100D	PCIE	PCIE MINI D2R P	24 34
PCIE_MINI_D2R	PCIE_100D	PCIE	PCIE MINI D2R N	24 34
GLAN_COMP			GLAN COMP	23
CLINK_NB	CLINK_55S	CLINK	CLINK NB CLK	16 25
CLINK_NB	CLINK_55S	CLINK	CLINK NB DATA	16 25
CLINK_NB_RESET_L	CLINK_55S	CLINK	CLINK NB RESET_L	16 25
CLINK_WLAN	CLINK_55S	CLINK	CLINK WLAN CLK	
CLINK_WLAN	CLINK_55S	CLINK	CLINK WLAN DATA	
CLINK_WLAN_RESET_L	CLINK_55S	CLINK	CLINK WLAN RESET_L	
NB_CLINK_VREF	CLINK_12MIL	CLINK_VREF	NB CLINK VREF	16
SB_CLINK_VREF0	CLINK_12MIL	CLINK_VREF	SB CLINK VREF0	25
SB_CLINK_VREF1	CLINK_12MIL	CLINK_VREF	SB CLINK VREF1	25
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE ENET R2D C P	24 35
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE ENET R2D C N	24 35
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE ENET R2D P	24 35
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE ENET R2D N	24 35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE ENET D2R P	24 35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE ENET D2R N	24 35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE ENET D2R C P	24 35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE ENET D2R C N	24 35
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI P<0>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI N<0>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI P<1>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI N<1>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI P<2>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI N<2>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI P<3>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI N<3>	35 37

### SB Constraints (2 of 2)

SYNC\_MASTER=T9\_NOME SYNC\_DATE=01/17/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE	SHT	OF
NONE	84	89

### Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

### Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
CK505_CPU0	CLK_FSB_100D	CLK_FSB	CK505_CPU0 P	29 30
CK505_CPU1	CLK_FSB_100D	CLK_FSB	CK505_CPU0 N	29 30
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1 P	29 30
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1 N	29 30
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2 ITP_SRC10 P	29 30
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2 ITP_SRC10 N	29 30
CK505_PCIF0	CLK_MED_55S	CLK_MED	CK505_PCIF0 CLK ITPEN	29 30
CK505_PCIF1	CLK_MED_55S	CLK_MED	CK505_PCIF1 CLK	29 30
CK505_PCI1	CLK_MED_55S	CLK_MED	CK505_PCI1 CLK	29 30
CK505_PCI2	CLK_MED_55S	CLK_MED	CK505_PCI2 CLK	29 30
CK505_PCI3	CLK_MED_55S	CLK_MED	CK505_PCI3 CLK	29 30
CK505_PCI4	CLK_MED_55S	CLK_MED	CK505_PCI4 CLK	29 30
CK505_PCI5	CLK_MED_55S	CLK_MED	CK505_PCI5 CLK FCTSEL	29 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_48M_FSA	29 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_REF0_FSC	29 30
CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M P	29 30
CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M N	29 30
CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS P	29 30
CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS N	29 30
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1 P	29 30
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1 N	29 30
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2 P	29 30
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2 N	29 30
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3 P	29 30
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3 N	29 30
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4 P	29 30
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4 N	29 30
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5 P	29 30
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5 N	29 30
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6 P	29 30
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6 N	29 30
CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7 P	29 30
CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7 N	29 30
CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8 P	29 30
CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8 N	29 30
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU P	10 30
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU N	10 30
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB P	7 14 30
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB N	7 14 30
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK P	13 30 80
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK N	13 30 80
(CK505_PCIF0)	CLK_MED_55S	CLK_MED	PCI_CLK33M_LPCPLUS	7 30 47
(CK505_PCIF1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SB	24 30
(CK505_PCI1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_FW	30 38
(CK505_PCI2)	CLK_MED_55S	CLK_MED	PCI_CLK33M_TPM	30 45
(CK505_PCI3)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SMC	30 45
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_PCI4 is project-specific	25 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_PCI5 is project-specific	25 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	SB_CLK48M_USBCTRL	25 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	SB_CLK14P3M_TIMER	25 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_FSA	30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_FSC	30
(CK505_DOT96)	CRT_50S	GND	NB_CLK96M_DOT P	9
(CK505_DOT96)	CRT_50S	GND	NB_CLK96M_DOT N	9
(CK505_LVDS)	CRT_50S	GND	NB_CLK100M_DPLLSS P	9
(CK505_LVDS)	CRT_50S	GND	NB_CLK100M_DPLLSS N	9
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M P	9
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M N	9
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI P	24 30
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI N	24 30
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD P	30 34
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD N	30 34
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA P	23 30
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA N	23 30
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE P	7 16 30
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE N	7 16 30
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI P	30 34
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI N	30 34
(CK505_SRC7)			CK505_SRC7 is project-specific	
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET P	30 35
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET N	30 35

### SMC SMBus Net Properties

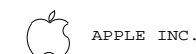
ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	48
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	48
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	48
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	48
SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	48
SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	48
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	48
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	48
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	48
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	48

### Clock & SMC Constraints

SYNC\_MASTER=T9\_NAME SYNC\_DATE=01/17/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE	SHT	OF
NONE	85	89

### FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF


SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW	*	=2:1_SPACING	?
FW_TP	*	=3:1_SPACING	?

### FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
EW_D_CTL	EW_55S	FW	FW LINK<7..0>
EW_D_CTL	EW_55S	FW	FW CTL<1..0>
EW_LCLK	CLK_MED_55S	CLK_MED	CLKFW LINK_LCLK
EW_LCLK	CLK_MED_55S	CLK_MED	CLKFW PHY_LCLK 38 39
EW_PCLK	CLK_MED_55S	CLK_MED	CLKFW LINK_PCLK 38 39
EW_PCLK	CLK_MED_55S	CLK_MED	CLKFW PHY_PCLK 38 39
EW_LKON	EW_55S	FW	FW LKON
EW_LKON	EW_55S	FW	FW LKON R
EW_LPS	EW_55S	FW	FW LPS 38 39
EW_LREQ	EW_55S	FW	FW LREQ 38 39
EW_PINT	EW_55S	FW	FW PINT 38 39
EWPHY_CLK98P304M_XI	CLK_MED_55S	CLK_MED	CLK98P304M FW_XI_R
EWPHY_CLK98P304M_XI	CLK_MED_55S	CLK_MED	CLK98P304M FW_XI
EW_0_TPA	EW_110D	EW_TP	FW 0 TPA P 39 41
EW_0_TPA	EW_110D	EW_TP	FW 0 TPA N 39 41
EW_0_TPB	EW_110D	EW_TP	FW 0 TPB P 39 41
EW_0_TPB	EW_110D	EW_TP	FW 0 TPB N 39 41
EW_1_TPA	EW_110D	EW_TP	FW 1 TPA P 39 41
EW_1_TPA	EW_110D	EW_TP	FW 1 TPA N 39 41
EW_1_TPB	EW_110D	EW_TP	FW 1 TPB P 39 41
EW_1_TPB	EW_110D	EW_TP	FW 1 TPB N 39 41
Port 2 Not Used			

**FireWire Constraints**  
 SYNC\_MASTER=T9\_NOME SYNC\_DATE=01/17/2007

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 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7413	11.0.0
SCALE	SHT	OF	
NONE	86	89	

### GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R55SE	*	=55_OHM_SE	=40_OHM_SE	=55_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR3_46SE	*	=46_OHM_SE	=46_OHM_SE	=46_OHM_SE	=46_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

### Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TMDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
VGA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TMDS	*	20 MIL	?
VGA	*	20 MIL	?
VGA_SYNC	*	20 MIL	?

### GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PROPERTY	VALUE
	PHYSICAL	SPACING		
FB_A_CLK_P	GDDR3_80D	GDDR3_CLK	FB A CLK P<0>	67 68 75
FB_A_CLK_N	GDDR3_80D	GDDR3_CLK	FB A CLK N<0>	67 68 75
FB_B_CLK_P	GDDR3_80D	GDDR3_CLK	FB B CLK P<1>	67 68 75
FB_B_CLK_N	GDDR3_80D	GDDR3_CLK	FB B CLK N<1>	67 68 75
FB_A_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A MA<1..0>	67 68 75
FB_B_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B MA<11..6>	67 68 75
FB_A_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A BA<2..0>	67 68 75
FB_B_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B RAS L	67 68 75
FB_A_CMD	GDDR3_40R55SE	GDDR3_CMD	FB A CAS L	67 68 75
FB_B_CMD	GDDR3_40R55SE	GDDR3_CMD	FB B WE L	67 68 75
FB_A_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB A CKE	67 68 75
FB_B_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB B CS0 L	67 68 75
FB_A_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB A DRAM RST	67 68 75
FB_B_CMD	GDDR3_46SE	GDDR3_CMD	FB A LMA<5..2>	67 68 75
FB_B_CMD	GDDR3_46SE	GDDR3_CMD	FB B UMA<5..2>	67 68 75
FB_A_WDQS0	GDDR3_46SE	GDDR3_DQS	FB A WDQS<0>	67 68 75
FB_B_WDQS1	GDDR3_46SE	GDDR3_DQS	FB B WDQS<1>	67 68 75
FB_A_WDQS2	GDDR3_46SE	GDDR3_DQS	FB A WDQS<2>	67 68 75
FB_B_WDQS3	GDDR3_46SE	GDDR3_DQS	FB B WDQS<3>	67 68 75
FB_A_RDQS0	GDDR3_46SE	GDDR3_DQS	FB A RDQS<0>	67 68 75
FB_B_RDQS1	GDDR3_46SE	GDDR3_DQS	FB B RDQS<1>	67 68 75
FB_A_RDQS2	GDDR3_46SE	GDDR3_DQS	FB A RDQS<2>	67 68 75
FB_B_RDQS3	GDDR3_46SE	GDDR3_DQS	FB B RDQS<3>	67 68 75
FB_A_DQ_BYTE0	GDDR3_46SE	GDDR3_DATA	FB A DQ<7..0>	67 68 75
FB_B_DQ_BYTE1	GDDR3_46SE	GDDR3_DATA	FB B DQ<15..8>	67 68 75
FB_A_DQ_BYTE2	GDDR3_46SE	GDDR3_DATA	FB A DQ<23..16>	67 68 75
FB_B_DQ_BYTE3	GDDR3_46SE	GDDR3_DATA	FB B DQ<31..24>	67 68 75
FB_A_DQM0	GDDR3_46SE	GDDR3_DATA	FB A DQM L<0>	67 68 75
FB_B_DQM1	GDDR3_46SE	GDDR3_DATA	FB B DQM L<1>	67 68 75
FB_A_DQM2	GDDR3_46SE	GDDR3_DATA	FB A DQM L<2>	67 68 75
FB_B_DQM3	GDDR3_46SE	GDDR3_DATA	FB B DQM L<3>	67 68 75
FB_A_WDQS0	GDDR3_46SE	GDDR3_DQS	FB A WDQS<4>	67 68 75
FB_B_WDQS1	GDDR3_46SE	GDDR3_DQS	FB B WDQS<5>	67 68 75
FB_A_WDQS2	GDDR3_46SE	GDDR3_DQS	FB A WDQS<6>	67 68 75
FB_B_WDQS3	GDDR3_46SE	GDDR3_DQS	FB B WDQS<7>	67 68 75
FB_A_RDQS0	GDDR3_46SE	GDDR3_DQS	FB A RDQS<4>	67 68 75
FB_B_RDQS1	GDDR3_46SE	GDDR3_DQS	FB B RDQS<5>	67 68 75
FB_A_RDQS2	GDDR3_46SE	GDDR3_DQS	FB A RDQS<6>	67 68 75
FB_B_RDQS3	GDDR3_46SE	GDDR3_DQS	FB B RDQS<7>	67 68 75
FB_A_DQ_BYTE0	GDDR3_46SE	GDDR3_DATA	FB A DQ<39..32>	67 68 75
FB_B_DQ_BYTE1	GDDR3_46SE	GDDR3_DATA	FB B DQ<47..40>	67 68 75
FB_A_DQ_BYTE2	GDDR3_46SE	GDDR3_DATA	FB A DQ<55..48>	67 68 75
FB_B_DQ_BYTE3	GDDR3_46SE	GDDR3_DATA	FB B DQ<63..56>	67 68 75
FB_A_DQM0	GDDR3_46SE	GDDR3_DATA	FB A DQM L<4>	67 68 75
FB_B_DQM1	GDDR3_46SE	GDDR3_DATA	FB B DQM L<5>	67 68 75
FB_A_DQM2	GDDR3_46SE	GDDR3_DATA	FB A DQM L<6>	67 68 75
FB_B_DQM3	GDDR3_46SE	GDDR3_DATA	FB B DQM L<7>	67 68 75

### GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PROPERTY	VALUE
	PHYSICAL	SPACING		
FB_C_CLK_P	GDDR3_80D	GDDR3_CLK	FB C CLK P<0>	67 68 76
FB_C_CLK_N	GDDR3_80D	GDDR3_CLK	FB C CLK N<0>	67 68 76
FB_D_CLK_P	GDDR3_80D	GDDR3_CLK	FB D CLK P<1>	67 68 76
FB_D_CLK_N	GDDR3_80D	GDDR3_CLK	FB D CLK N<1>	67 68 76
FB_C_CMD	GDDR3_40R55SE	GDDR3_CMD	FB C MA<1..0>	67 68 76
FB_D_CMD	GDDR3_40R55SE	GDDR3_CMD	FB D MA<11..6>	67 68 76
FB_C_CMD	GDDR3_40R55SE	GDDR3_CMD	FB C BA<2..0>	67 68 76
FB_D_CMD	GDDR3_40R55SE	GDDR3_CMD	FB D RAS L	67 68 76
FB_C_CMD	GDDR3_40R55SE	GDDR3_CMD	FB C CAS L	67 68 76
FB_D_CMD	GDDR3_40R55SE	GDDR3_CMD	FB D WE L	67 68 76
FB_C_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB C CKE	67 68 76
FB_D_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB D CS0 L	67 68 76
FB_C_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB C DRAM RST	67 68 76
FB_D_CMD	GDDR3_46SE	GDDR3_CMD	FB C LMA<5..2>	67 68 76
FB_D_CMD	GDDR3_46SE	GDDR3_CMD	FB D UMA<5..2>	67 68 76
FB_C_WDQS0	GDDR3_46SE	GDDR3_DQS	FB C WDQS<0>	67 68 76
FB_D_WDQS1	GDDR3_46SE	GDDR3_DQS	FB D WDQS<1>	67 68 76
FB_C_WDQS2	GDDR3_46SE	GDDR3_DQS	FB C WDQS<2>	67 68 76
FB_D_WDQS3	GDDR3_46SE	GDDR3_DQS	FB D WDQS<3>	67 68 76
FB_C_RDQS0	GDDR3_46SE	GDDR3_DQS	FB C RDQS<0>	67 68 76
FB_D_RDQS1	GDDR3_46SE	GDDR3_DQS	FB D RDQS<1>	67 68 76
FB_C_RDQS2	GDDR3_46SE	GDDR3_DQS	FB C RDQS<2>	67 68 76
FB_D_RDQS3	GDDR3_46SE	GDDR3_DQS	FB D RDQS<3>	67 68 76
FB_C_DQ_BYTE0	GDDR3_46SE	GDDR3_DATA	FB C DQ<7..0>	67 68 76
FB_D_DQ_BYTE1	GDDR3_46SE	GDDR3_DATA	FB D DQ<15..8>	67 68 76
FB_C_DQ_BYTE2	GDDR3_46SE	GDDR3_DATA	FB C DQ<23..16>	67 68 76
FB_D_DQ_BYTE3	GDDR3_46SE	GDDR3_DATA	FB D DQ<31..24>	67 68 76
FB_C_DQM0	GDDR3_46SE	GDDR3_DATA	FB C DQM L<0>	67 68 76
FB_D_DQM1	GDDR3_46SE	GDDR3_DATA	FB D DQM L<1>	67 68 76
FB_C_DQM2	GDDR3_46SE	GDDR3_DATA	FB C DQM L<2>	67 68 76
FB_D_DQM3	GDDR3_46SE	GDDR3_DATA	FB D DQM L<3>	67 68 76
FB_C_WDQS0	GDDR3_46SE	GDDR3_DQS	FB C WDQS<4>	67 68 76
FB_D_WDQS1	GDDR3_46SE	GDDR3_DQS	FB D WDQS<5>	67 68 76
FB_C_WDQS2	GDDR3_46SE	GDDR3_DQS	FB C WDQS<6>	67 68 76
FB_D_WDQS3	GDDR3_46SE	GDDR3_DQS	FB D WDQS<7>	67 68 76
FB_C_RDQS0	GDDR3_46SE	GDDR3_DQS	FB C RDQS<4>	67 68 76
FB_D_RDQS1	GDDR3_46SE	GDDR3_DQS	FB D RDQS<5>	67 68 76
FB_C_RDQS2	GDDR3_46SE	GDDR3_DQS	FB C RDQS<6>	67 68 76
FB_D_RDQS3	GDDR3_46SE	GDDR3_DQS	FB D RDQS<7>	67 68 76
FB_C_DQ_BYTE0	GDDR3_46SE	GDDR3_DATA	FB C DQ<39..32>	67 68 76
FB_D_DQ_BYTE1	GDDR3_46SE	GDDR3_DATA	FB D DQ<47..40>	67 68 76
FB_C_DQ_BYTE2	GDDR3_46SE	GDDR3_DATA	FB C DQ<55..48>	67 68 76
FB_D_DQ_BYTE3	GDDR3_46SE	GDDR3_DATA	FB D DQ<63..56>	67 68 76
FB_C_DQM0	GDDR3_46SE	GDDR3_DATA	FB C DQM L<4>	67 68 76
FB_D_DQM1	GDDR3_46SE	GDDR3_DATA	FB D DQM L<5>	67 68 76
FB_C_DQM2	GDDR3_46SE	GDDR3_DATA	FB C DQM L<6>	67 68 76
FB_D_DQM3	GDDR3_46SE	GDDR3_DATA	FB D DQM L<7>	67 68 76

### G84M Net Properties

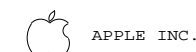
ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PROPERTY	VALUE
	PHYSICAL	SPACING		
(CK505_DOT96)	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M	30 71
CK505_CLK27MSS	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS	30 71
LVDS_L_CLK	LVDS_100D	LVDS	LVDS L CLK P	72 74
LVDS_L_CLK	LVDS_100D	LVDS	LVDS L CLK N	72 74
LVDS_L_DATA	LVDS_100D	LVDS	LVDS L DATA P<2..0>	72 74
LVDS_L_DATA	LVDS_100D	LVDS	LVDS L DATA N<2..0>	72 74
LVDS_L_DATA	LVDS_100D	LVDS	LVDS L DATA P<3>	71 72
LVDS_L_DATA	LVDS_100D	LVDS	LVDS L DATA N<3>	71 72
LVDS_U_CLK	LVDS_100D	LVDS	LVDS U CLK P	72 74
LVDS_U_CLK	LVDS_100D	LVDS	LVDS U CLK N	72 74
LVDS_U_DATA	LVDS_100D	LVDS	LVDS U DATA P<2..0>	72 74
LVDS_U_DATA	LVDS_100D	LVDS	LVDS U DATA N<2..0>	72 74
LVDS_U_DATA	LVDS_100D	LVDS	LVDS U DATA P<3>	71 72
LVDS_U_DATA	LVDS_100D	LVDS	LVDS U DATA N<3>	71 72
TMDS_CLK	TMDS_100D	TMDS	TMDS CLK P	72 78
TMDS_CLK	TMDS_100D	TMDS	TMDS CLK N	72 78
TMDS_DATA	TMDS_100D	TMDS	TMDS DATA P<5..0>	72 78
TMDS_DATA	TMDS_100D	TMDS	TMDS DATA N<5..0>	72 78
VGA_B_TV_C	VGA_50S	VGA	GPU TV C VGA R	71 78
VGA_G_TV_Y	VGA_50S	VGA	GPU TV Y VGA G	71 78
VGA_B_TV_COMP	VGA_50S	VGA	GPU TV COMP VGA B	71 78
VGA_50S	VGA_50S	VGA	GPU VGA R	71 72
VGA_50S	VGA_50S	VGA	GPU VGA G	71 72
VGA_50S	VGA_50S	VGA	GPU VGA B	71 72
VGA_50S	VGA_50S	VGA	GPU TV C	71 72
VGA_50S	VGA_50S	VGA	GPU TV Y	71 72
VGA_50S	VGA_50S	VGA	GPU TV COMP	71 72
VGA_SYNC	VGA_55S	VGA_SYNC	GPU VGA HSYNC	72 78
VGA_SYNC	VGA_55S	VGA_SYNC	GPU VGA VSYNC	72 78

### GPU (G84M) Constraints

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7413	11.0.0
SCALE	SHT	OF
NONE	87	89



PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILLS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V8_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PP1V8_MEM	*	PWR_P2MM
MEM_CMD	PP1V8_MEM	*	PWR_P2MM
MEM_CTRL	PP1V8_MEM	*	PWR_P2MM
MEM_DATA	PP1V8_MEM	*	PWR_P2MM
MEM_DQS	PP1V8_MEM	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_VREF	GND	*	GND_P2MM
CLK_MED	GND	*	GND_P2MM
CLK_PCIE	GND	*	GND_P2MM
DMI	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
DMI	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM
ENET_MDI	ENET_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_MED	FW_POWER	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

### Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_70D	BOTTOM			0.127 MM	6.35 MM		

Allow 0.1 mm necks for >0.1 mm lines between thru-hole SO-DIMM pins.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM	2.54 MM	OVERRIDE	OVERRIDE
MEM_70D	ISL10			0.100 MM	2.54 MM		
MEM_85D	ISL4, ISL10			0.100 MM	2.54 MM		

### Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	BGA	100_DIFF_BGA
TMDS_100D	BGA	100_DIFF_BGA
SATA_100D	BGA	100_DIFF_BGA

### M87 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE		
	PHYSICAL	SPACING	
(PCIE_EXCARD)	PCIE_100D	PCIE	PCIE_EXCARD_R2D_P
(PCIE_EXCARD)	PCIE_100D	PCIE	PCIE_EXCARD_R2D_N
(PCIE_MINI)	PCIE_100D	PCIE	PCIE_MINI_R2D_P
(PCIE_MINI)	PCIE_100D	PCIE	PCIE_MINI_R2D_N
	ENET_100D	ENET_MDI	ENET_MDI_R_P<3..0>
	ENET_100D	ENET_MDI	ENET_MDI_R_N<3..0>
	ENET_100D	ENETCONN	ENETCONN_P<3..0>
	ENET_100D	ENETCONN	ENETCONN_N<3..0>
	FW_110D	FW_TP	FW_PORT0_TPA_FL_P
	FW_110D	FW_TP	FW_PORT0_TPA_FL_N
	FW_110D	FW_TP	FW_PORT0_TPB_FL_P
	FW_110D	FW_TP	FW_PORT0_TPB_FL_N
(SATA_A_R2D)	SATA_100D	SATA	SATA_A_R2D_UF_P
(SATA_A_R2D)	SATA_100D	SATA	SATA_A_R2D_UF_N
(SATA_A_D2R)	SATA_100D	SATA	SATA_A_D2R_UF_P
(SATA_A_D2R)	SATA_100D	SATA	SATA_A_D2R_UF_N
(USB_EXT_A)	USB_90D	USB	USB2_EXT_A_MUXED_P
(USB_EXT_A)	USB_90D	USB	USB2_EXT_A_MUXED_N
(USB_EXT_A)	USB_90D	USB	USB2_RT_P
(USB_EXT_A)	USB_90D	USB	USB2_RT_N
(USB_EXT_D)	USB_90D	USB	USB_WWAN_F_P
(USB_EXT_D)	USB_90D	USB	USB_WWAN_F_N
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_F_P
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_F_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	GFXIMVP6_VSEN_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	GFXIMVP6_VSEN_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	NBCOREISNS_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	NBCOREISNS_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	P1V8ISNS_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	P1V8ISNS_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	P1V25ISNS_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	P1V25ISNS_N
THERM_DIFFPAIR	THERM_1T01_55S	THERM	CPUTHMSNS_D2_P
THERM_DIFFPAIR	THERM_1T01_55S	THERM	CPUTHMSNS_D2_N
THERM_DIFFPAIR	THERM_1T01_55S	THERM	CPU_THERMD_P
THERM_DIFFPAIR	THERM_1T01_55S	THERM	CPU_THERMD_N
THERM_DIFFPAIR	THERM_1T01_55S	THERM	GPUTHMSNS_D_P
THERM_DIFFPAIR	THERM_1T01_55S	THERM	GPUTHMSNS_D_N
THERM_DIFFPAIR	THERM_1T01_55S	THERM	GPU_TDIODE_P
THERM_DIFFPAIR	THERM_1T01_55S	THERM	GPU_TDIODE_N
THERM_DIFFPAIR	THERM_1T01_55S	THERM	HSTHMSNS_D_P
THERM_DIFFPAIR	THERM_1T01_55S	THERM	HSTHMSNS_D_N
THERM_DIFFPAIR	THERM_1T01_55S	THERM	RSFSTHMSNS_D_P
THERM_DIFFPAIR	THERM_1T01_55S	THERM	RSFSTHMSNS_D_N
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_F_P
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_F_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	P1V8ISNS_R_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	P1V8ISNS_R_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	P1V8GUISNS_R_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	P1V8GUISNS_R_N
	TMDS_100D	TMDS	TMDS_CLK_R_P
	TMDS_100D	TMDS	TMDS_CLK_R_N
	TMDS_100D	TMDS	TMDS_CLK_F_P
	TMDS_100D	TMDS	TMDS_CLK_F_N
	TMDS_100D	TMDS	TMDS_DATA_F_P<5..0>
	TMDS_100D	TMDS	TMDS_DATA_F_N<5..0>
(VGA_R_TV_Y)	VGA_50S	VGA	VGA_R
(VGA_G_TV_C)	VGA_50S	VGA	VGA_G
(VGA_B_TV_COMP)	VGA_50S	VGA	VGA_B
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_HSYNC_R
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_VSYNC_R
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_HSYNC
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_VSYNC
	PP1V8_MEM		=PP1V8_S3M_MEM_A
	PP1V8_MEM		=PP1V8_S3M_MEM_B
	GND		GND
	ENET_POWER		
	SB_POWER		PP3V3_S5
	SB_POWER		PP3V3_S0
	SB_POWER		PP1V5_S0
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	P1V8GUISNS_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	P1V8GUISNS_N
	FW_POWER		

**Project Specific Constraints**  
 SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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D	051-7413	11.0.0
SCALE	SHT	OF
NONE	88	89



# M75 Board-Specific Spacing & Physical Constraints

BOARD LAYERS				BOARD AREAS			BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA			MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.100 MM	0.100 MM			
55_OHM_SE	ISL2, ISL11	Y	0.250 MM	0.076 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.125 MM	0.125 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
46_OHM_SE	TOP, BOTTOM	Y	0.126 MM	0.126 MM			
46_OHM_SE	*	Y	0.100 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP, BOTTOM	Y	0.150 MM	0.150 MM			
45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.185 MM	0.185 MM			
40_OHM_SE	*	Y	0.131 MM	0.131 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.335 MM	0.335 MM			
27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3, ISL4	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM
70_OHM_DIFF	ISL9, ISL10	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM
70_OHM_DIFF	ISL2, ISL11	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM
70_OHM_DIFF	TOP, BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3, ISL4	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM
80_OHM_DIFF	ISL9, ISL10	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM
80_OHM_DIFF	ISL2, ISL11	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3, ISL4	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM
85_OHM_DIFF	ISL9, ISL10	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM
85_OHM_DIFF	ISL2, ISL11	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM
85_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9, ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2, ISL11	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3, ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9, ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2, ISL11	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3, ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9, ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL2, ISL11	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP, BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	N	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100\_DIFF\_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

## PCB Rule Definitions

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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NONE	89	89	