1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
?		?	?	?	?

SCHEM,TRUCKEE,M57

DVT2

8/16/2006

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7164	1	SCHEM,TRUCKEE,M57	SCH	CRITICAL	
820-2059	1	PCBF,TRUCKEE,M57	PCB	CRITICAL	

DRAWING
TITLE=TRUCKEE
ABBREV=DRAWING
LAST_MODIFIED=Wed Aug 16 19:10:01 2006

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

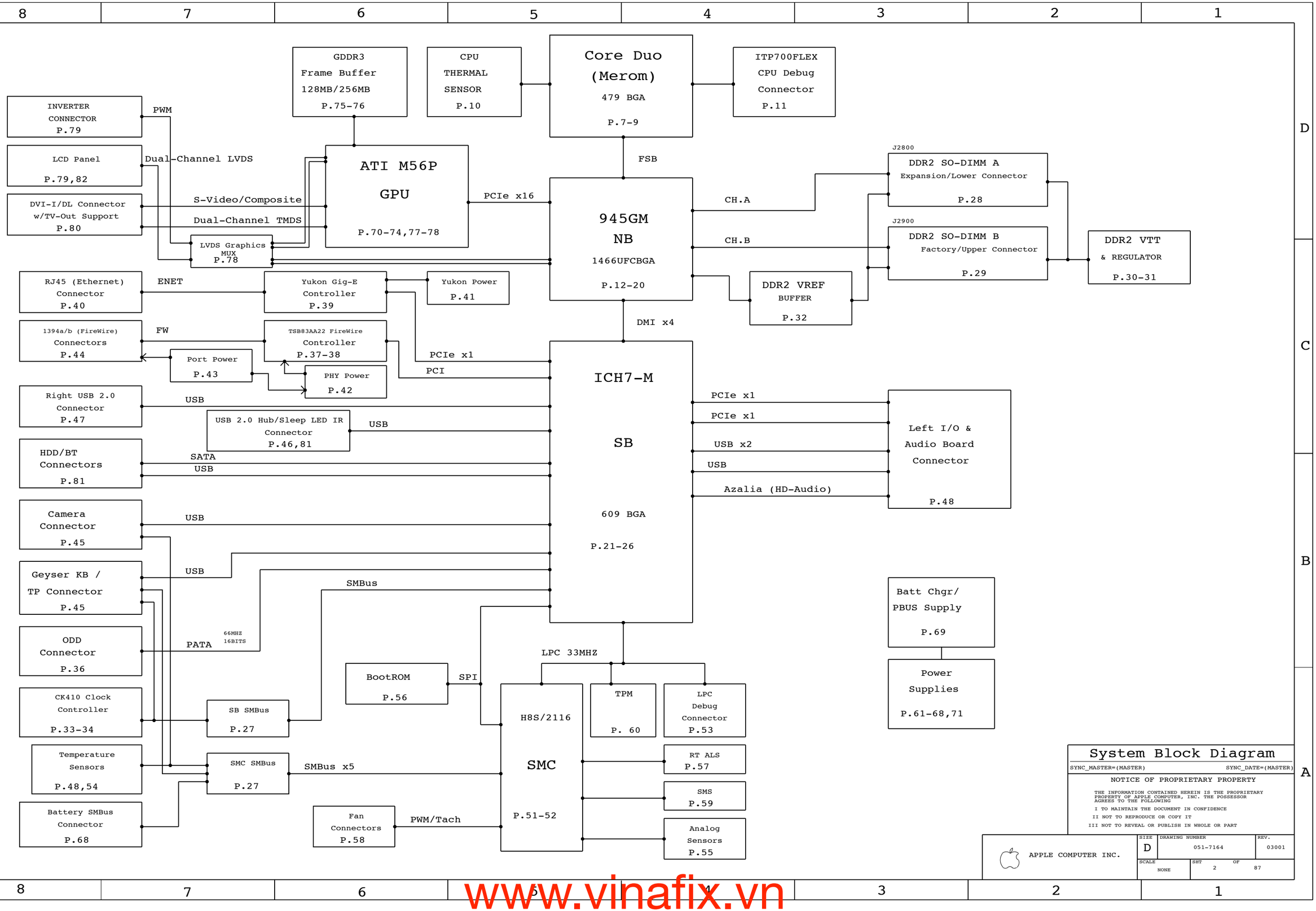
SIZE D

Apple Computer Inc.

TITLE
SCHEM.TRUCKEE,M57

DRAWING NUMBER 051-7164 REV. 03001

SHT 1 OF 87

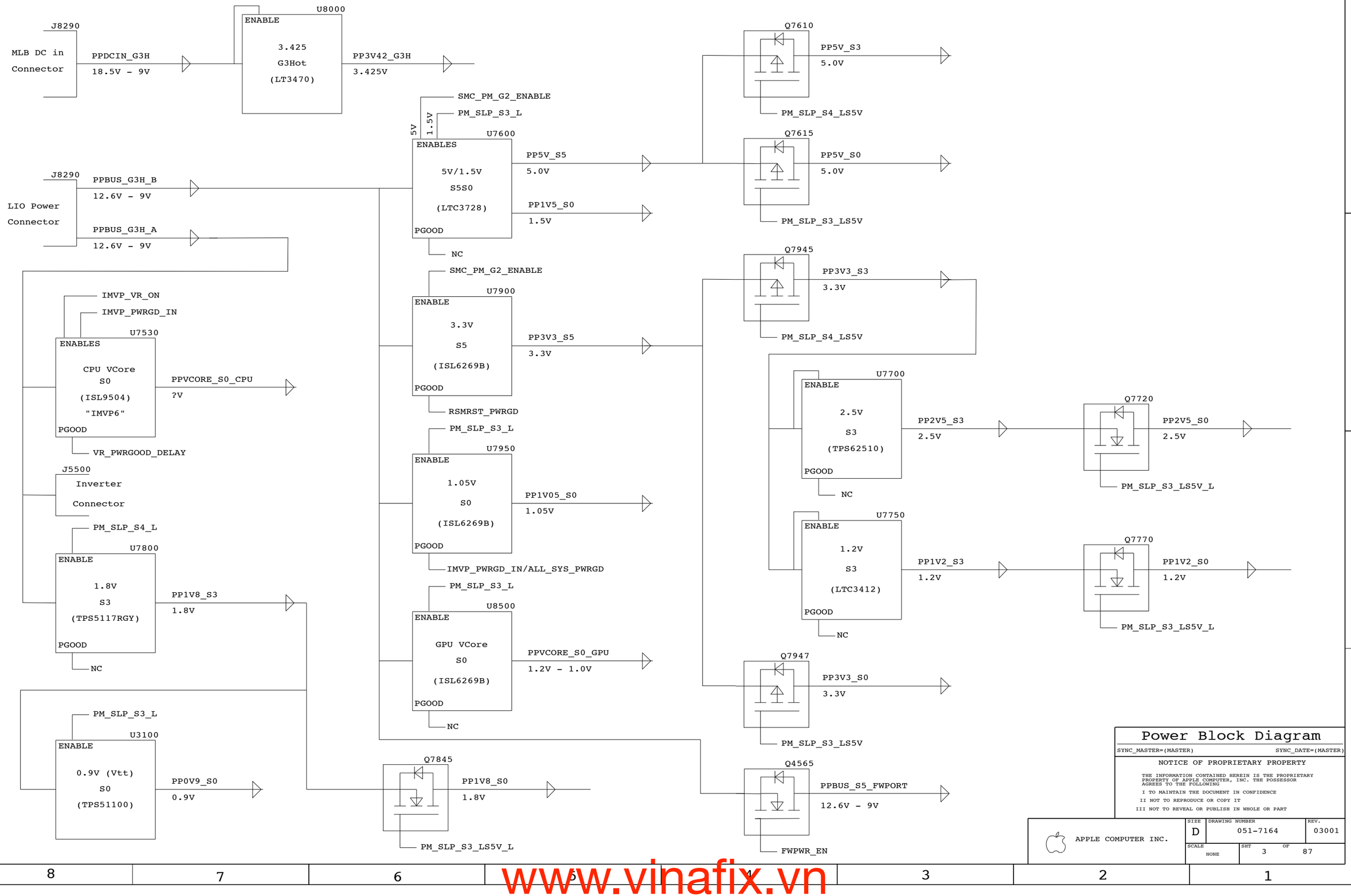


System Block Diagram

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 2 OF 87	



BOM NUMBER	BOM NAME	BOM OPTIONS
630-7813	TRUCKEE,2.16GHZ,B2,256VRAM,INF,M57	VRAM_256INF,M57_COMMON,CPU_2_16GHZ_B2,EEE_WJJ
630-7812	TRUCKEE,2.16GHZ,B2,256VRAM,SAM,M57	VRAM_256SAM,M57_COMMON,CPU_2_16GHZ_B2,EEE_WJH

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7815	TRUCKEE,2.33GHZ,B2,256VRAM,INF,M57	VRAM_256INF,M57_COMMON,CPU_2_33GHZ_B2,EEE_WJL
630-7814	TRUCKEE,2.33GHZ,B2,256VRAM,SAM,M57	VRAM_256SAM,M57_COMMON,CPU_2_33GHZ_B2,EEE_WJK

BOM GROUP	BOM OPTIONS
VRAM_128SAM	VRAM_128_SAMSUNG
VRAM_256SAM	GPU_MEM_256M,VRAM_256_SAMSUNG
VRAM_128INF	GPU_MEM_NOT_SAM,VRAM_128_INFINEON
VRAM_256INF	GPU_MEM_NOT_SAM,GPU_MEM_256M,VRAM_256_INFINEON

BOM GROUP	BOM OPTIONS
M57_COMMON	ALTERNATE,COMMON,M57_COMMON1,M57_COMMON2,M57_COMMON3,M57_COMMON4,M57_DEBUG,ISL6255A,M57_NO_3G
M57_COMMON1	ENET_LOWPWR_EN,ENETPWR_S3AC,GPU_BB_CTL
M57_COMMON2	KBDLED_HAS,MEMVREF_S3,MEMVTT_EN_PU,RTUSB_ESD,USB_C_OC_PU,USB_D_OC_PU,USB_E_OC_PU
M57_COMMON3	LVDS_PD,FW_PORT_FAULT_PU
M57_COMMON4	BOOTROM_DEVEL,SMC_PRGRM
M57_DEBUG	ITP,ITPCONN,LPCPLUS
M57_TPM	TPM
M57_3G	3G
M57_NO_3G	NO_3G

BAR CODE LABELS / EEE #'S

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:W9J]	CRITICAL	EEE_WJJ
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:W3A]	CRITICAL	EEE_WJH
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:W3A]	CRITICAL	EEE_WJK
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:WDV]	CRITICAL	EEE_WJL

MODULE PARTS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0368	1	IC,ATI,M56P,GRPHSCTRL,880BGA,LF	U8400	CRITICAL	
333S0354	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_SAMSUNG
333S0350	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_SAMSUNG
333S0358	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_HYNIX
333S0351	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_HYNIX
333S0376	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_INFINEON
333S0377	4	IC,SGRAM,GDDR3,16MX32,600MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_INFINEON

ALTERNATE PARTS

PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
37680448	37680445		ALL	SI7806ADN for FDM6296
12880083	12880073		C2516	1.86 MAX ALT TO 1.9 MAX
12880093	12880092		ALL	KEMET IS ALT TO SANYO
12880094	12880060		ALL	330UF,2V,9MOHM,D2
12880095	12880060		ALL	330UF,2V,6MOHM,D2
12880081	12880061		ALL	150UF,6.3V,25MOHM,C2
353B1465	353B1461		ALL	Screened ISL6262 for ISL9504
15280287	15280435		ALL	Alternates for Coilcraft MSS5131
15780030	15780111		ALL	Alternates for E&E Magnetics, TOE

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN, NO	U4101	CRITICAL	
338S0274	1	IC,SMC,HS8/2116	U5800	CRITICAL	SMC_BLANK
341S1931	1	IC,PRGRM,SMC(NEW),M57	U5800	CRITICAL	SMC_PRGRM
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U4102	CRITICAL	
335S0384	1	IC,16MBIT 8-PIN SPI SERIAL FLASH,SOIC8	U6301	CRITICAL	BOOTROM_BLANK
341S1924	1	IC, BOOTROM, DEVELOPMENT, UNLOCKED ,M57	U6301	CRITICAL	BOOTROM_DEVEL
341S1925	1	IC, BOOTROM, FINAL, LOCKED, M57	U6301	CRITICAL	BOOTROM_FINAL
353S1461	1	IC,ISL9504,SYNC REG CTL,QFN 48	U7530	CRITICAL	
359S0109	1	IC,LOW POWER CLOCK SYNTHESIZER,68PIN	U3301	CRITICAL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S1789	1	IC, TPM, 28-PIN TSSOP	U6700	CRITICAL	TPM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3391	1	IC,MDC,B2,PRQ,2.16GHZ,34W,667M,4M,479 BGA	U0700	CRITICAL	CPU_2_16GHZ_B2
337S3393	1	IC,MDC,B2,PRQ,2.33GHZ,34W,667M,4M,479 BGA	U0700	CRITICAL	CPU_2_33GHZ_B2
338S0269	1	IC,945GM,NORTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,ICH7M,BGA	U2100	CRITICAL	

Extra TPM options:
SMC_TPM_GPIO2
SMC_TPM_GPIO1
SMC_TPM_PP

BOM CONFIGURATION

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 4 OF 87	

Functional Test Points

Power Nets

	FUNC_TEST	
U12A	TRUE	PP0V9_S0
U12B	TRUE	PP1V05_S0
U12C	TRUE	PP1V2_D3C
U12D	TRUE	PP1V2_S3
U13A	TRUE	PP1V5_S0
U13B	TRUE	PP1V5_S0_NB
U13C	TRUE	PP1V8_S3
U13D	TRUE	PP1V8_D3C
U14A	TRUE	PP2V5_S0
U14B	TRUE	PP2V5_D3C
U14C	TRUE	PP3V3_S0
U14D	TRUE	PP3V3_S3
U15A	TRUE	PP3V3_S5
U15B	TRUE	PP5V_S0
U15C	TRUE	PP5V_S3
U15D	TRUE	PP5V_S5
U16A	TRUE	PPBUS_G3H
U16B	TRUE	GND

Request for at least 10 GND TPs

Characterization TPs

	FUNC_TEST	
E18	TRUE	IMVP_VR_ON
E20	TRUE	IMVP_DPRSLPVR
E19	TRUE	PM_SLP_S3_L
E21	TRUE	PM_SLP_S3BATT
E22	TRUE	PM_SLP_S4_L
E23	TRUE	PM_SLP_S5_L
E24	TRUE	P1V5P1V05S0_PGOOD
E25	TRUE	CPU_DPRSTP_L
E26	TRUE	IMVP6_VID<6..0>
E27	TRUE	FSB_CLK_CPU_N
E28	TRUE	FSB_CLK_CPU_P
E29	TRUE	PLT_RST_L
E30	TRUE	PLT_RST_L
E31	TRUE	PEG_RESET_L
E32	TRUE	SMC_LRESET_L
E33	TRUE	TPM_LRESET_L
E34	TRUE	CPU_STPCLK_L
E35	TRUE	FSB_CLK_NB_P
E36	TRUE	FSB_CLK_NB_N
E37	TRUE	CLK_NB_OE_L
E38	TRUE	NB_CLK100M_GCLKIN_P
E39	TRUE	NB_CLK100M_GCLKIN_N
E40	TRUE	NB_CLK_DREFCLKIN_P
E41	TRUE	NB_CLK_DREFCLKIN_N
E42	TRUE	NB_CLK_DREFSSCLKIN_P
E43	TRUE	NB_CLK_DREFSSCLKIN_N
E44	TRUE	CPU_THERMTRIP_R
E45	TRUE	TP_SB_SUS_CLK

MAC-1 TPs

	FUNC_TEST	
E27	TRUE	CPU_PWRGD
E28	TRUE	TP_CPU_CPUSLP_L
E29	TRUE	PM_DPRSLPVR
E30	TRUE	CPU_DPSLP_L
E31	TRUE	PM_LAN_ENABLE
E32	TRUE	PCI_RST_L
E33	TRUE	PM_RSMRST_L
E35	TRUE	PM_SB_PWROK
E36	TRUE	SB_RTC_RST_L
E38	TRUE	PM_STPCPU_L
E39	TRUE	PM_STPPCI_L
E37	TRUE	VR_PWRGD_CK410
E38	TRUE	VR_PWRGOOD_DELAY
E39	TRUE	FSB_CPURST_L
E40	TRUE	FSB_SLPCPU_L
E41	TRUE	FSB_DPWR_L
E42	TRUE	NB_SB_SYNC_L
E43	TRUE	PP2V5_S0_GPU_TPVDD
E44	TRUE	PP2V5_S0_GPU_TXVDDR
E45	TRUE	PP2V5_S0_GPU_AVDD
E46	TRUE	PP2V5_S0_GPU_A2VDD
E47	TRUE	PP2V5_S0_GPU_LPVDD
E48	TRUE	PP2V5_S0_GPU_LVDDR
E49	TRUE	PP3V3_S0
E50	TRUE	PP3V3_S0_CK410_VDD48
E51	TRUE	PP3V3_S0_CK410_VDD_PCI
E52	TRUE	PP3V3_S0_CK410_VDD_REF
E53	TRUE	PP3V3_S0_CK410_VDD_CPU_SRC
E54	TRUE	PP3V3_S0_CK410_VDDA
E55	TRUE	PP3V3_FWPHY
E56	TRUE	PP3V3_FWPHY_AVDD
E57	TRUE	PP3V3_FWPHY_PLLVDD
E58	TRUE	PP1V95_FWPHY
E59	TRUE	PP1V95_FWPHY_PLLVDD
E60	TRUE	PP1V2_S3
E61	TRUE	PP3V3_S3AC
E62	TRUE	PP2V5_S3
E63	TRUE	PP2V5_S3_ENET_AVDD

Fan Connectors

	FUNC_TEST	
J1A1	TRUE	PP5V_S0
J1A2	TRUE	FAN_LT_PWM
J1A3	TRUE	FAN_LT_TACH
J1B1	TRUE	FAN_RT_PWM
J1B2	TRUE	FAN_RT_TACH

LPC+ Debug Connector

	FUNC_TEST	
J1A1	TRUE	PP3V42_G3H
J1A2	TRUE	PP5V_S0
J1A3	TRUE	LPC_AD<0>
J1A4	TRUE	LPC_AD<1>
J1A5	TRUE	LPC_FRAME_L
J1A6	TRUE	PM_CLKRUN_L
J1A7	TRUE	BOOT_LPC_SPI_L
J1A8	TRUE	SMC_TMS
J1A9	TRUE	DEBUG_RST_L
J1A10	TRUE	SMC_TRST_L
J1B1	TRUE	SMC_TDO
J1B2	TRUE	SMC_MD1
J1B3	TRUE	SMC_TX_L
J1B4	TRUE	FWH_INIT_L
J1B5	TRUE	PCI_CLK_PORT80_LPC
J1B6	TRUE	LPC_AD<2>
J1B7	TRUE	LPC_AD<3>
J1B8	TRUE	INT_SERIRQ
J1B9	TRUE	PM_SUS_STAT_L
J1B10	TRUE	SMC_TDI
J1C1	TRUE	SMC_TCK
J1C2	TRUE	SMC_RST_L
J1C3	TRUE	SMC_NMI
J1C4	TRUE	SMC_RX_L
J1C5	TRUE	SV_SET_UP

Resistor Calibration

	FUNC_TEST	
R142	TRUE	PP5V_S0_ISENSECAL
R141	TRUE	PP1V8_S3
R140	TRUE	PP1V05_S0
R139	TRUE	PPVCORE_S0_CPU
R143	TRUE	PPVCORE_D3C_GPU
R144	TRUE	ISENSE_CAL_EN
R145	TRUE	GND

Request for at least 2 GND TPs per resistor

Camera Connector

	FUNC_TEST	
J16A	TRUE	PP5V_S3
J16B	TRUE	USB2_CAMERA_N
J16C	TRUE	USB2_CAMERA_P
J16D	TRUE	PP5V_S3_CAMERA_F

Inverter Connector

J27A	TRUE	GND_CHASSIS_INVERTER
J27B	TRUE	PPBUS_S0_INVERTER
J27C	TRUE	PP5V_INVERTER_SW
J27D	TRUE	INVERTER_PWM
J27E	TRUE	GND_CHASSIS_INVERTER

Thermal Sensors

	FUNC_TEST	
R172	TRUE	HSTHMSNS_DX_P
R174	TRUE	HSTHMSNS_DX_N
R171	TRUE	RSFSTHMSNS_D_P
R175	TRUE	RSFSTHMSNS_D_N

SMC TPs

	FUNC_TEST	
U27A	TRUE	PM_SYSRST_L
U27B	TRUE	SMC_ONOFF_L

Battery Connector

	FUNC_TEST	
J15A	TRUE	BATT_POS
J15B	TRUE	BATT_NEG
J15C	TRUE	SMC_BS_ALRT_L
J15D	TRUE	SMBUS_SMC_BSA_SCL
J15E	TRUE	SMBUS_SMC_BSA_SDA

Left I/O Data Connector

	FUNC_TEST	
J18A	TRUE	PP1V5_S0
J18B	TRUE	ALS_GAIN
J18C	TRUE	LTALS_OUT
J18D	TRUE	ACZ_SDATAIN<0>
J18E	TRUE	ACZ_SDATAOUT
J18F	TRUE	ACZ_BITCLK
J18G	TRUE	ACZ_RST_L
J18H	TRUE	EXCARD_OC_L
J18J	TRUE	LTUSB_OC_L
J18K	TRUE	LT2USB_OC_L
J18L	TRUE	PM_SLP_S3_LS5V
J18M	TRUE	PM_SLP_S4_L
J18N	TRUE	SYS_ONEWIRE
J18P	TRUE	MINI_CLKREQ_L
J18R	TRUE	SMC_EXCARD_CP
J18S	TRUE	EXCARD_CLKREQ_L
J18T	TRUE	SMC_EXCARD_PWR_EN
J18U	TRUE	LIO_PLT_RESET_L
J18V	TRUE	ACZ_SYNC
J18W	TRUE	USB2_LT_N
J18X	TRUE	USB2_LT_P
J18Y	TRUE	USB2_EXCARD_N
J18Z	TRUE	USB2_EXCARD_P
J19A	TRUE	PCIE_EXCARD_R2D_C_N
J19B	TRUE	PCIE_EXCARD_R2D_C_P
J19C	TRUE	PCIE_EXCARD_D2R_N
J19D	TRUE	PCIE_EXCARD_D2R_P
J19E	TRUE	PCIE_CLK100M_EXCARD_P
J19F	TRUE	PCIE_CLK100M_EXCARD_N
J19G	TRUE	USB2_LT2_N
J19H	TRUE	USB2_LT2_P
J19J	TRUE	PCIE_MINI_R2D_C_N
J19K	TRUE	PCIE_MINI_R2D_C_P
J19L	TRUE	PCIE_MINI_D2R_N
J19M	TRUE	PCIE_MINI_D2R_P
J19N	TRUE	PCIE_CLK100M_MINI_P
J19P	TRUE	PCIE_CLK100M_MINI_N
J19R	TRUE	SMBUS_SB_SCL
J19S	TRUE	SMBUS_SB_SDA
J19T	TRUE	PCIE_WAKE_L
J19U	TRUE	SMC_BC_ACOK
J19V	TRUE	SMBUS_SMC_A_S3_SCL
J19W	TRUE	SMBUS_SMC_A_S3_SDA

Left I/O Power Connector

	FUNC_TEST	
J17A	TRUE	PP18V5_DCIN
J17B	TRUE	PPBUS_G3H
J17C	TRUE	GND

Request for at least 10 GND test points

Power Supply NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		IMVP6_RBIAS	61C7
TRUE		P5VS5_RUNSS	62C5 66A6
TRUE		P1V5S0_RUNSS	62C4 66C6
TRUE		P2V5S3_MODE	
TRUE		P2V5S3_SHDNRT	
TRUE		P1V2S3_RT	63B6
TRUE		P1V2S3_RUNSS	41C4 63B7
TRUE		P1V8S3_COMP	
TRUE		P1V8S3_FSET	
TRUE		P3V3S5_COMP	65C6
TRUE		P3V3S5_FSET	65D6
TRUE		P1V05S0_COMP	65A7
TRUE		P1V05S0_FSET	65B7
TRUE		P3V42G3H_FB	64C3
TRUE		GPUVCORE_COMP	71C7
TRUE		GPUVCORE_FSET	71C7
TRUE		GPUBBP_ADJ	71B7

CPU FSB NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		FSB_A_L<31..3>	7C8 7D8 12C4 12D4 87D6
TRUE		FSB_ADS_L	7D6 12C4 87D6
TRUE	TRUE	FSB_ADSTB_L<1..0>	7C8 7D8 12C4 87C6
TRUE		FSB_BNR_L	7D6 12C4 87D6
TRUE		FSB_BREQ0_L	7D6 12C4 87D6
TRUE		FSB_D_L<63..0>	7B3 7B4 7C3 7C4 12B6 12C6 12D6 87D6
TRUE		FSB_DBSY_L	7D6 12B4 87D6
TRUE	TRUE	FSB_DINV_L<3..0>	7B3 7B4 7C3 7C4 12B4 87D6
TRUE		FSB_DRDY_L	7D6 12B4 87D6
TRUE	TRUE	FSB_DSTBN_L<3..0>	7B3 7B4 7C3 7C4 12B4 87D6
TRUE	TRUE	FSB_DSTBP_L<3..0>	7B3 7B4 7C3 7C4 12B4 87D6
TRUE		FSB_HIT_L	7D6 12B4 87D6
TRUE		FSB_HITM_L	7D6 12B4 87D6
TRUE		FSB_LOCK_L	7D6 12B4 87D6
TRUE		FSB_REQ_L<4..0>	7D8 12A4 12B4 87D6

EXPOSED_VIA property indicates that the net should have a via with 10-mil soldermask opening for use as engineering probe point.

Misc EXPOSED_VIA Nets

EXPOSED_VIA		
TRUE	DMI_N2S_P<1..0>	14B4 22D2
TRUE	DMI_N2S_N<1..0>	14B4 22D2
TRUE	SB_CLK100M_SATA_P	21B6 33B4 34C3 34C5
TRUE	SB_CLK100M_SATA_N	21B6 33B4 34C3 34C5
TRUE	USB_BT_P	6C1 6C2 6C3 22C2 81A4
TRUE	USB_BT_N	6C1 6C2 6C3 22C2 81A4

Misc NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		USB2_CAMERA_P_F	45B5
TRUE		USB2_CAMERA_N_F	45B5
TRUE		TP_FW_CTL<0>	37C3

Functional / ICT Test

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 5 OF 87	

NC_CPU_A32_L
NC_CPU_A33_L
NC_CPU_A34_L
NC_CPU_A35_L
NC_CPU_A36_L
NC_CPU_A37_L
NC_CPU_A38_L
NC_CPU_A39_L
NC_CPU_APM0_L
NC_CPU_APM1_L
NC_CPU_EXTBREF
NC_CPU_HFPLL
NC_CPU_SPARE0
NC_CPU_SPARE1
NC_CPU_SPARE2
NC_CPU_SPARE4

NC_MEM_A_A<15..14>
NC_MEM_B_A<15..14>
TP_NB_CFG<4..3>
TP_NB_CFG<6>
TP_NB_CFG<8>
TP_NB_CFG<11..10>
TP_NB_CFG<15..14>
TP_NB_CFG<17>

NOTE: NB_CFG<13..12> require test access

TP_NB_CFG<13..12>
TP_SB_SUS_CLK

Inverter PWM Reset Alias

PLT_RST_L

R0600
0
5%
1/16W
MF-LF
402

ALS_GAIN
RTALS_GAIN
NC_ENET_CTRL12
NC_ENET_CTRL25

Ethernet Powr Management Support

ENET_LOWPWR_EN

R0690
0
5%
1/16W
MF-LF
402

SB_GPIO30

NOTE: BOM options "USB_G_OC_PU" and "ENET_LOWPWR_EN" are mutually-exclusive.

FireWire Aliases

PPFW_PORTA_VP_UF
PPFW_PORTB_VP_UF

PP3V3_FWPHY
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.20 mm
MAKE_BASE=TRUE

PP1V95_FWPHY
VOLTAGE=1.95V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
MAKE_BASE=TRUE

SMC_RSTGATE_L
PCI_AD<19>
=FW_PCI_IDSEL
PCI_GNT3_L
PCI_REQ3_L

USB Port "A" (Debug Port) = Right USB 2.0 Port

USB2_RT_P
USB2_RT_N
RTUSB_OC_L

USB Port "B" = Trackpad (Geyser)

USB_TRACKPAD_P
USB_TRACKPAD_N
UNUSED_USB_B_OC_L

USB Port "C" = Left USB 2.0 Port

USB2_LT_P
USB2_LT_N
LTUSB_OC_L

USB Port "D" = Camera

USB2_CAMERA_P
USB2_CAMERA_N
UNUSED_USB_D_OC_L

USB Port "E" = ExpressCard

USB2_EXCARD_P
USB2_EXCARD_N
EXCARD_OC_L

USB Port "F" = USB 1.1 Hub

USB_HUB_P
USB_HUB_N

USB Port "G" = Bluetooth (M13P)

USB_BT_P
USB_BT_N

USB Port "H" = 2nd Left USB 2.0 Port

USB2_LT2_P
USB2_LT2_N
LT2USB_OC_L

TP_USB2_3G_P
TP_USB2_3G_N

LVDS Pull Down Aliases

=LVDS_PD_L_CLK_N
=LVDS_PD_L_CLK_P
=LVDS_PD_L_DATA_P<2>
=LVDS_PD_L_DATA_N<2>
=LVDS_PD_U_CLK_N
=LVDS_PD_U_CLK_P
=LVDS_PD_U_DATA_P<1>
=LVDS_PD_U_DATA_N<1>

LVDS_L_DATA_P<1>
LVDS_L_DATA_N<1>
LVDS_L_DATA_P<0>
LVDS_L_DATA_N<0>
LVDS_L_CLK_N
LVDS_L_CLK_P
LVDS_L_DATA_N<2>
LVDS_L_DATA_P<2>
LVDS_U_DATA_N<1>
LVDS_U_DATA_P<1>
LVDS_U_DATA_N<0>
LVDS_U_DATA_P<0>
LVDS_U_DATA_P<2>
LVDS_U_DATA_N<2>
LVDS_U_CLK_N
LVDS_U_CLK_P

Base net is PM_SLP_S3_LS5V

PM_SLP_S4_L

Base net is PM_SLP_S4_L

PM_SLP_S3_LS5V

Chassis connection to be made at the fan cutout near the right ALS. Not stuffed at Proto.

NO STUFF
SH0601
EMI-SPRING
SG-5624208
GND_CHASSIS_FANFRAME
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
NO STUFF
R0601
0
5%
1/16W
MF-LF
402

Chassis connection to be made at the mounting hole northwest of the DVI connector. Plated hole.

ZT0600
195R106
GND_CHASSIS_DVI_TOP
C0600
0.01UF
10%
50V
X7R
402
GND

Chassis connection to be made on FW shell

ZT0603
HOLE-VIA-P5RP25
GND_CHASSIS_DVI_BOT
NO STUFF
R0602
0
5%
1/16W
MF-LF
402

ZT0604
HOLE-VIA-P5RP25
GND_CHASSIS_ENET

Chassis connection to be made at the mounting hole southwest of the USB connector. Plated hole.

ZT0601
195R106
GND_CHASSIS_USB

Chassis connection to be made at the mounting hole east of the LVDS connector

ZT0602
HOLE-VIA-P5RP25
GND_CHASSIS_LVDS
C0602
0.01UF
10%
50V
X7R
402

SH0600
OG-503040
SHLD-SM-LF
GND_CHASSIS_INVERTER

LEFT CLUTCH BARREL CABLING

Thermal Module Holes

Add one through via per hole to GND or 2 blind vias per side per hole to GND

Top CPU TM Hole
Top GPU Right TM Hole
Left CPU TM Hole
Right CPU TM Hole
Lower Left GPU TM Hole

Frame holes

ZT0612
HOLE-VIA-P5RP25
GND_CHASSIS_LIOFLEX_HOLE
C0612
C0613
0.01UF
10%
50V
X7R
402

ZT0613
HOLE-VIA-P5RP25
GND_CHASSIS_ODD_HOLE
C0610
C0611

ZT0611
HOLE-VIA-P5RP25
GND_CHASSIS_BATTCONN_HOLE
C0619
C0614

ZT0610
HOLE-VIA-P5RP25
GND_CHASSIS_LNDACARD_HOLE
C0615
C0616

ZT0614
HOLE-VIA-P5RP25
GND_CHASSIS_LEFT_DIMM_HOLE
C0617
C0618

Signal Aliases

SYNC_MASTER=(MASTER)
SYNC_DATE=(MASTER)

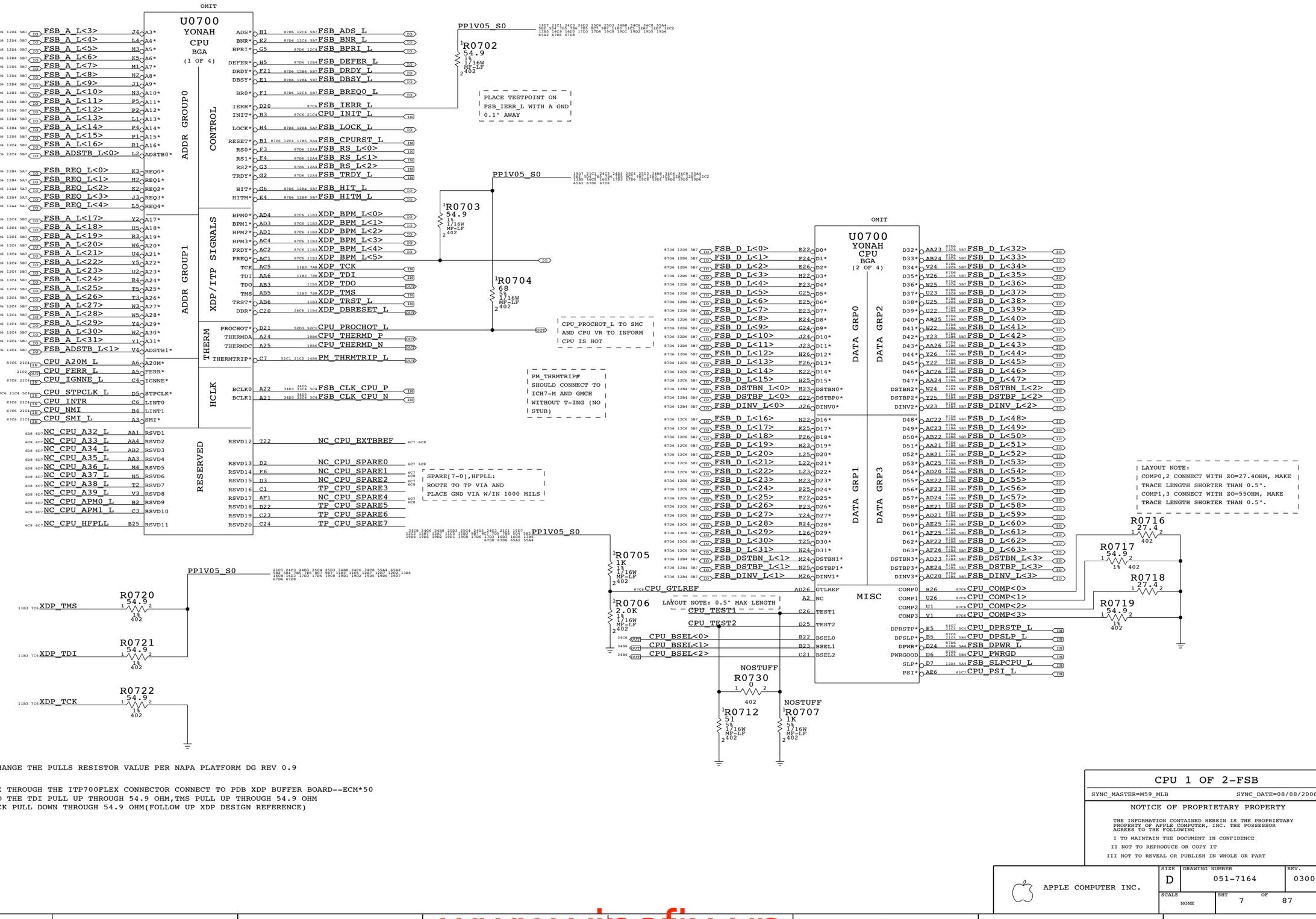
NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 6 OF 87	



CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9

WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM*50
SO THE TDI PULL UP THROUGH 54.9 OHM,TMS PULL UP THROUGH 54.9 OHM
TCK PULL DOWN THROUGH 54.9 OHM(FOLLOW UP XDP DESIGN REFERENCE)

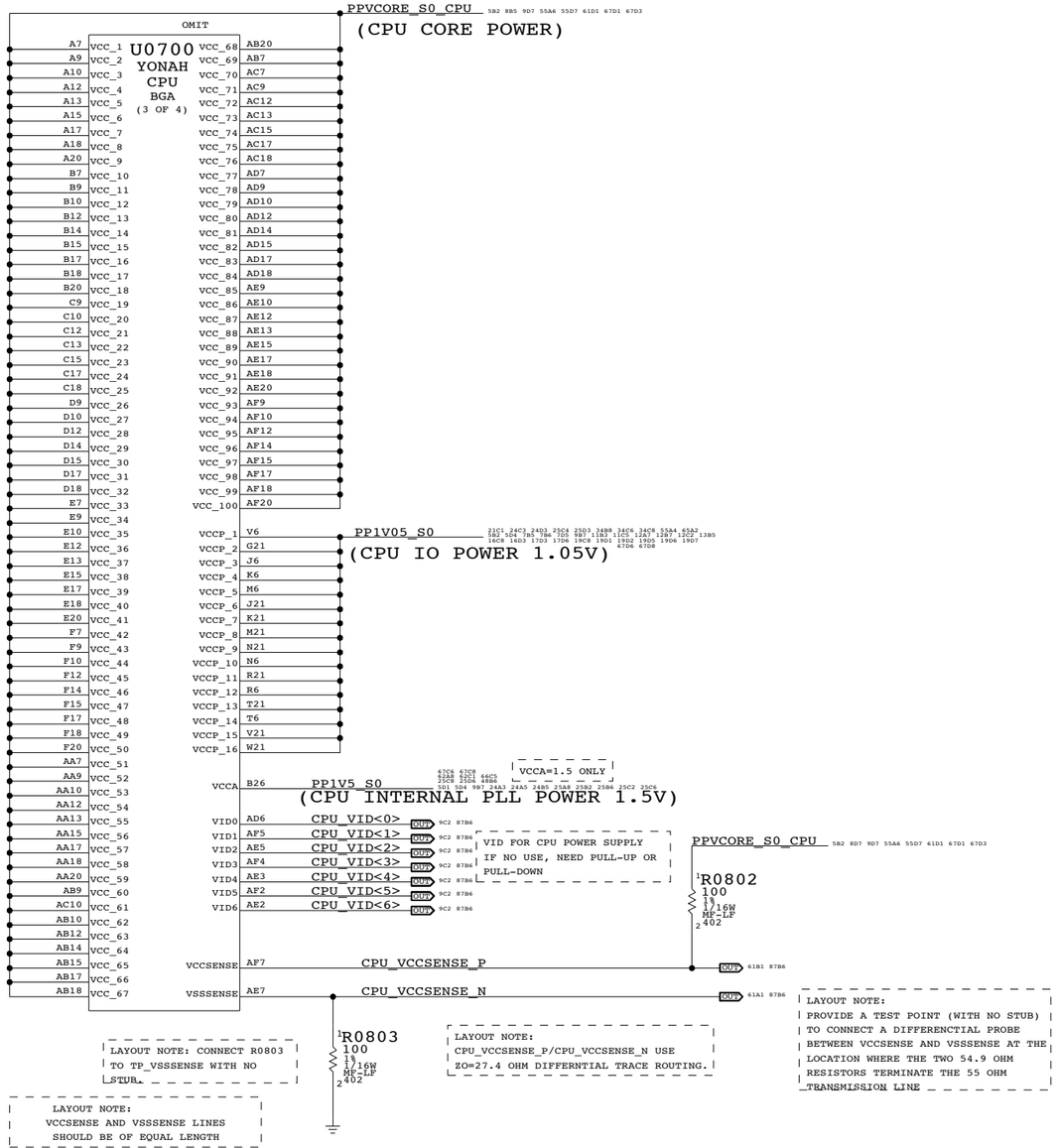
CPU 1 OF 2-FSB

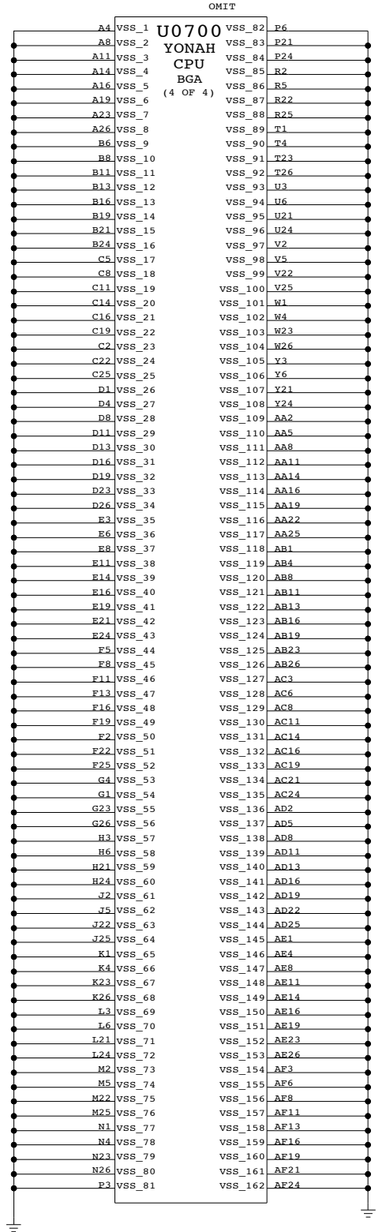
SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	7	87





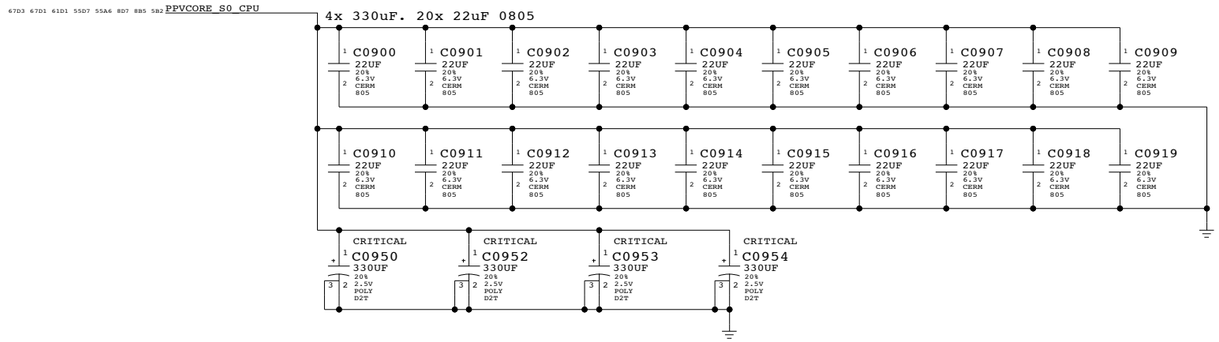
CPU 2 OF 2-PWR/GND

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

APPLE COMPUTER INC.

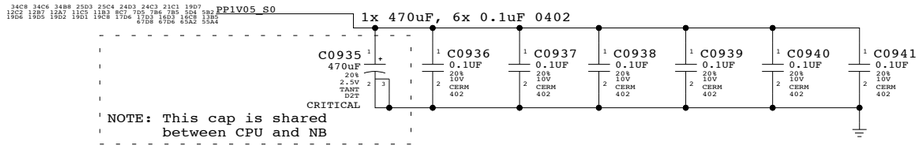
SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 8 OF 87	

CPU VCORE HF AND BULK DECOUPLING



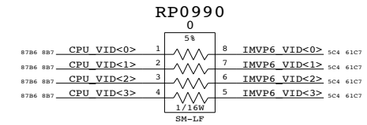
VCCA (CPU AVdd) Decoupling

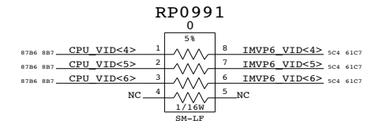
VCCP (CPU I/O) Decoupling



CPU VCORE VID Connections

Resistors to allow for override of CPU VID
Will probably be removed before production





CPU Decoupling & VID

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	9	87

CPU ZONE THERMAL SENSOR

LAYOUT NOTE:
ADD GND GUARD TRACE
FOR CPU_THERMD_P AND
CPU_THERMD_N

LAYOUT NOTE:
ROUTE CPU_THERMD_P AND
CPU_THERMD_N ON SAME
LAYER.
10 MIL TRACE
10 MIL SPACING

67C3 67B3 67A3 66B6 66B5 66B1 65D6 65B3
54B5 26D4 26B6 26B4 25D8 25D5 25C6 25C4 25B8
26D1 26B4 26B6 26B4 25D8 25D5 25C6 25C4 25B8
21C3 20B4 20A4 19C7 19C6 17C6 14D6 14C7 5D4 5A4
25B4 25B3 24D3 24C3 24B5 24B3 23D3 23B3 23B5 23D3
22B4 22A4 21D3 21C3 21B4 21A4 20D3 20B3 20A3 20D3
62A6 61D8 61A5 60D4 60C7 58C7 58C4 57B6 54D4
82D5 82C6 82B3 82A4 79D3 79A8 71D2 67C5

EP3V3_S0

C1002 0.1UF 10% 16V X5R 402

R1006 10K 5% 1/16W MF-LF 402

R1005 10K 5% 1/16W MF-LF 402

U1001 TMP401 MSOP CRITICAL

VDD

ALERT*/THM2* — THERM_ALERT_L

THM* — THERM_ALERT

SCLK — SMBUS_SMC_B_S0_SCL (51B5 49B5 27D3 27D2 27D1) TO

SDATA — SMBUS_SMC_B_S0_SDA (51B5 49B5 27D3 27D2 27D1) TO

GND

D+ — THRM_CPU_DX_P

D- — THRM_CPU_DX_N

OUT 7C6 CPU_THERMD_P

R1001 499 1% 1/16W MF-LF 402

(TO CPU INTERNAL THERMAL DIODE)
(TC0D)

C1001 0.001UF 10% 50V CERM 402

R1002 499 1% 1/16W MF-LF 402

IN 7C6 CPU_THERMD_N

PLACE U1001 NEAR THE U1200

CPU MISC1-TEMP SENSOR

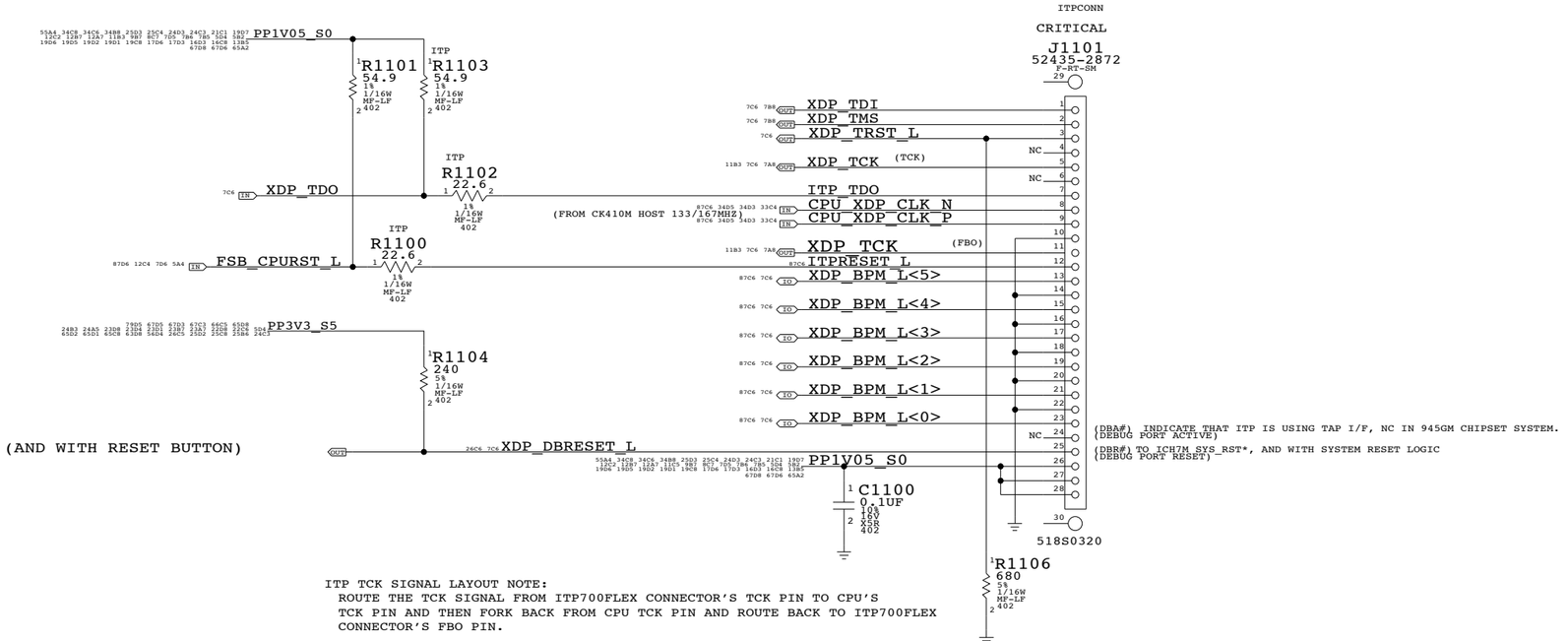
SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	10	87

CPU ITP700FLEX DEBUG SUPPORT



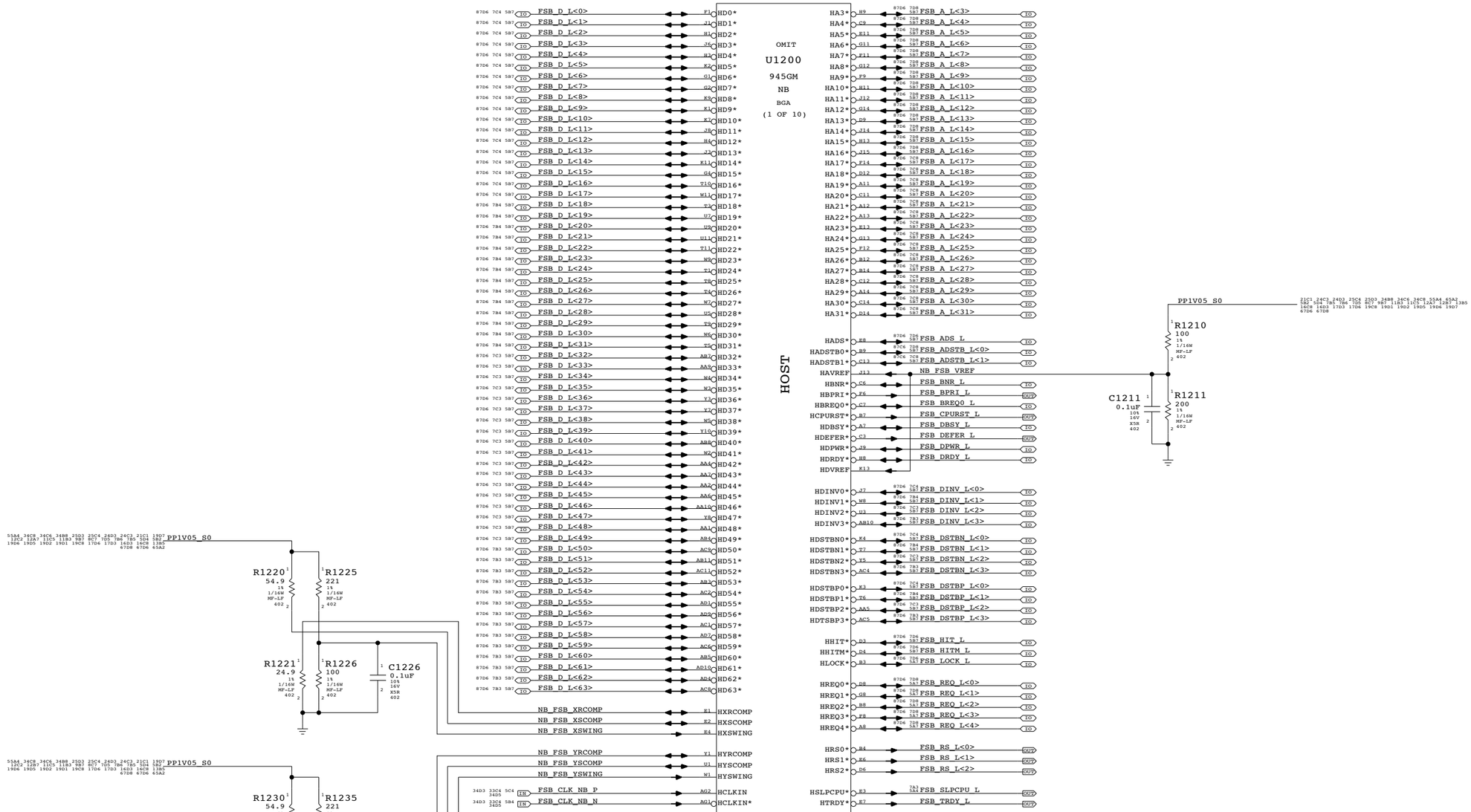
ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 11 OF 87	



NB CPU Interface

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	12	87

LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

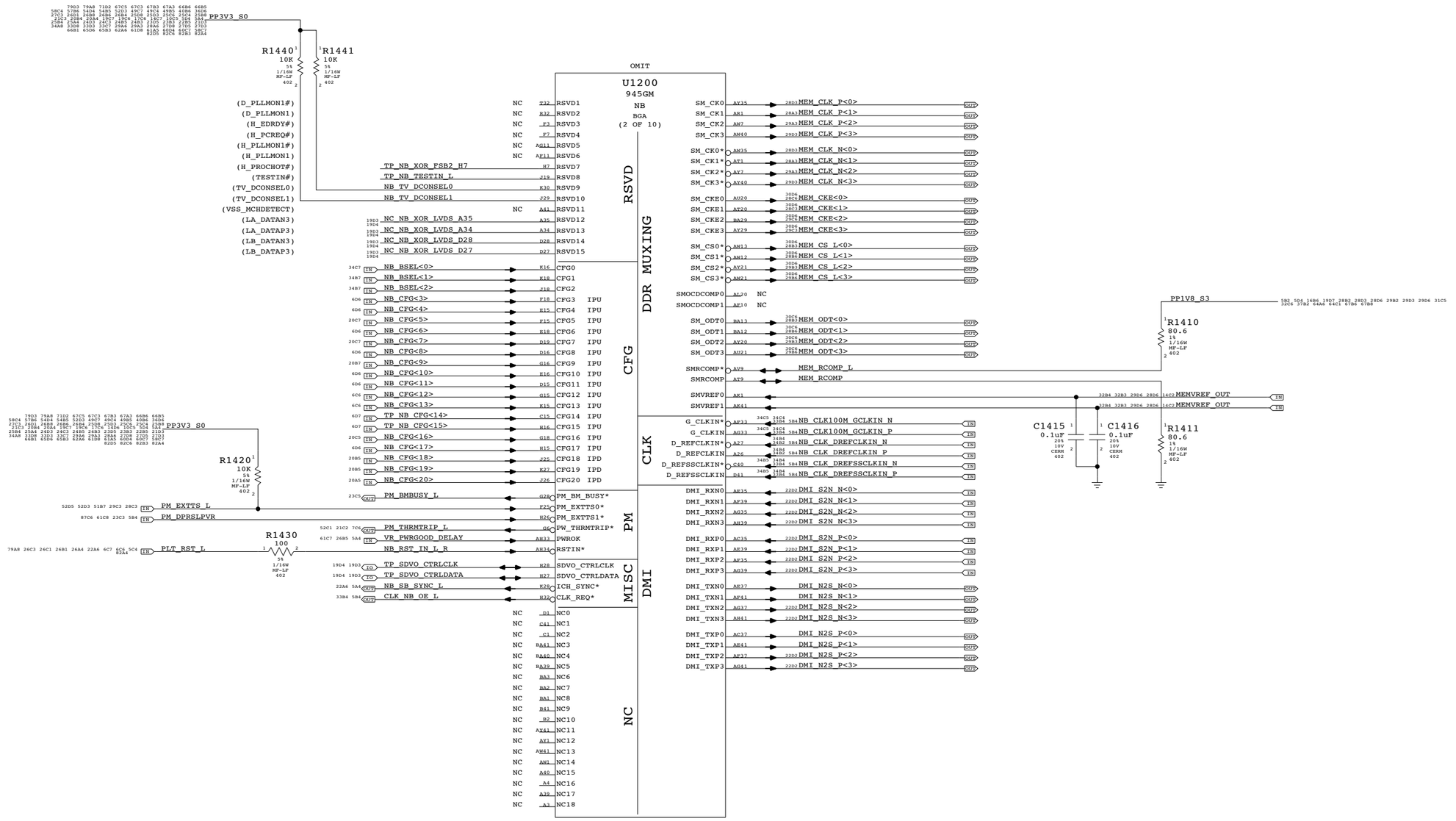
Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.

NB PEG / Video Interfaces

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 13 OF 87	

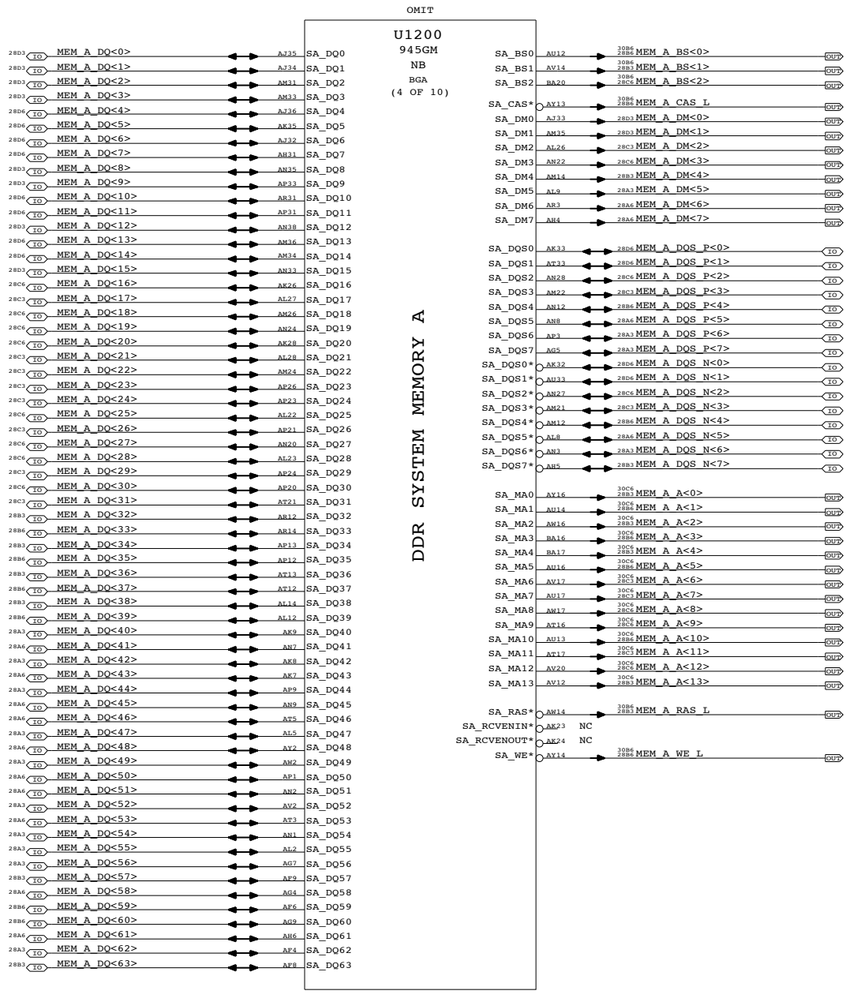


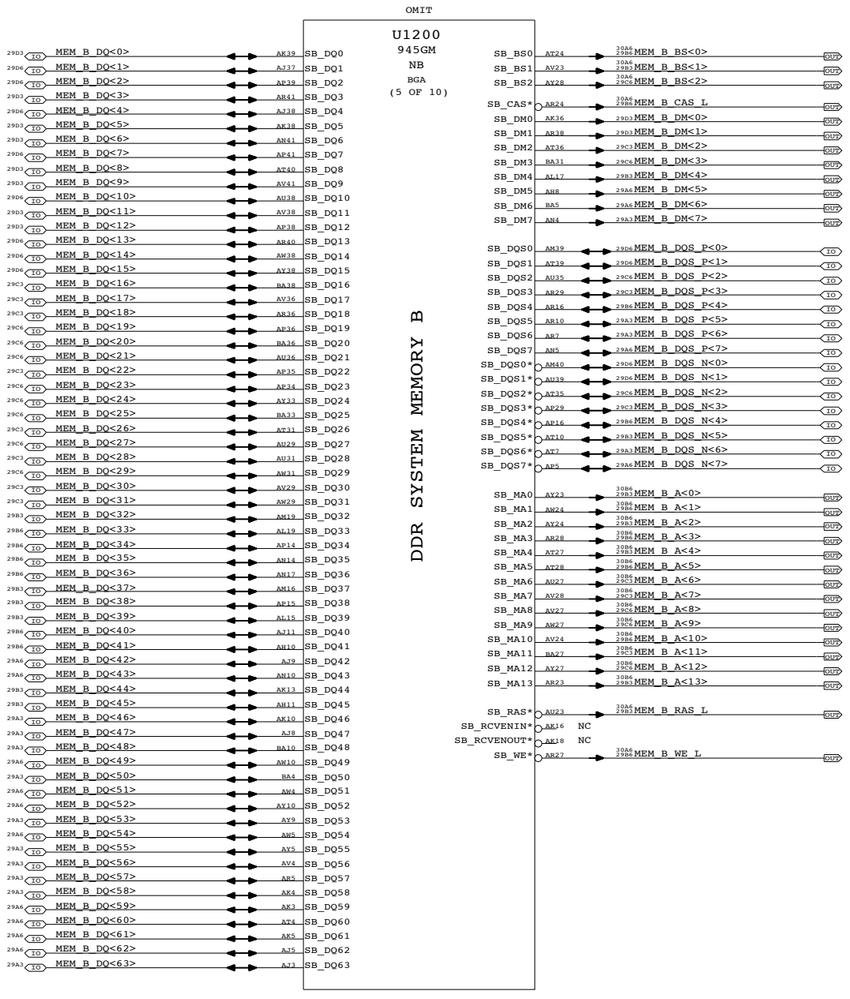
NB Misc Interfaces

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 14 OF 87	





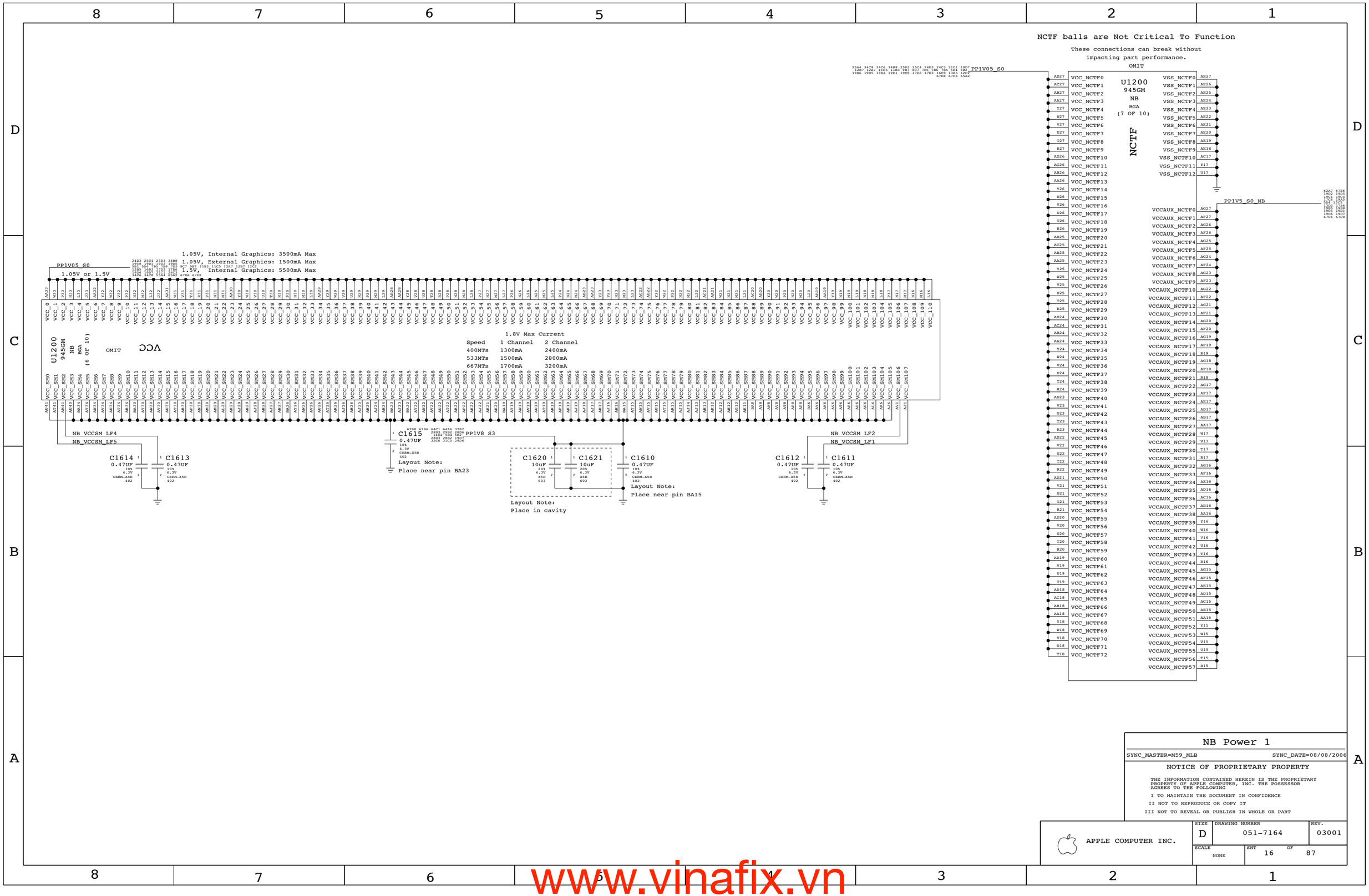
NB DDR2 Interfaces

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	15	87



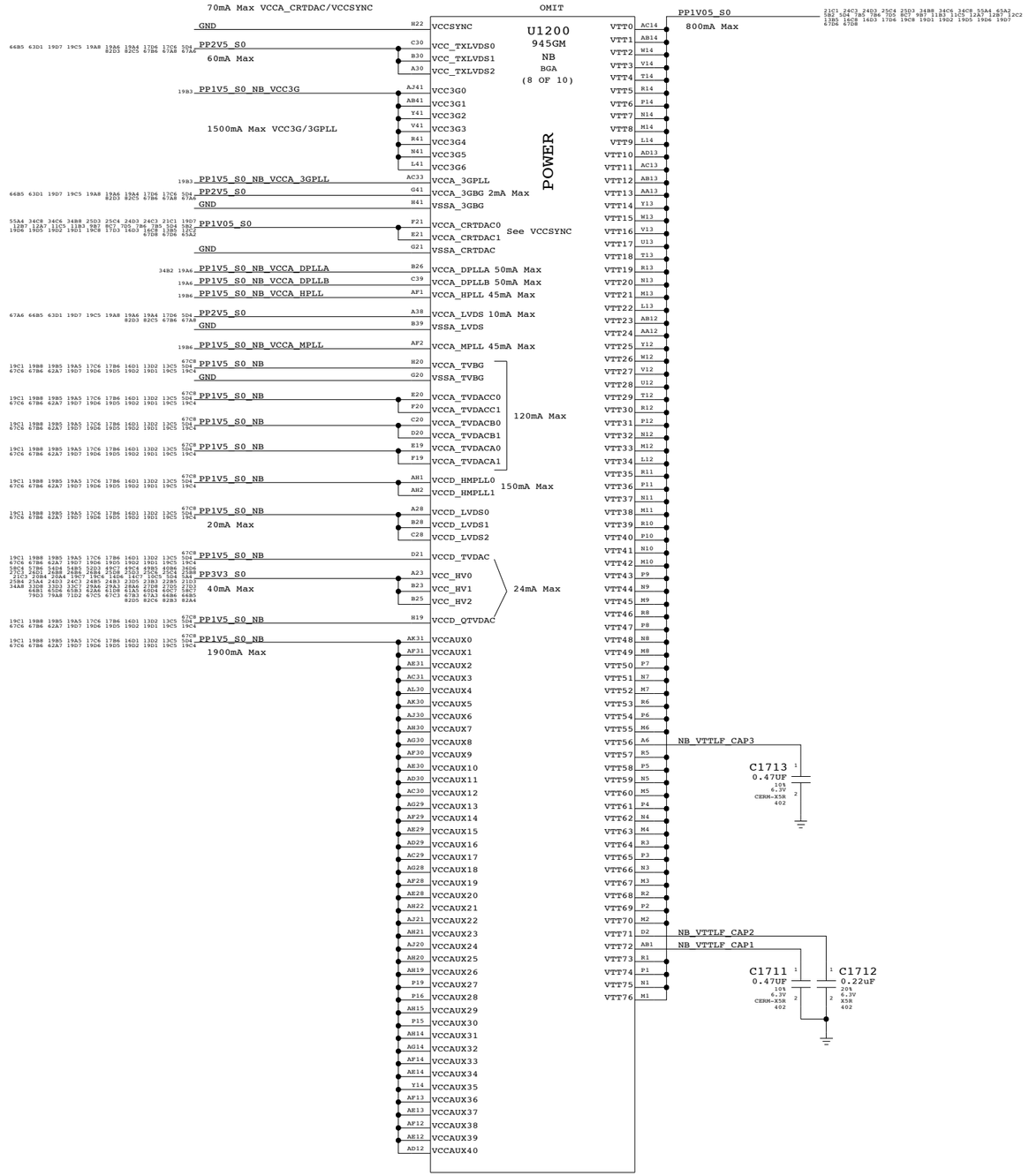
NB Power 1

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	16	87



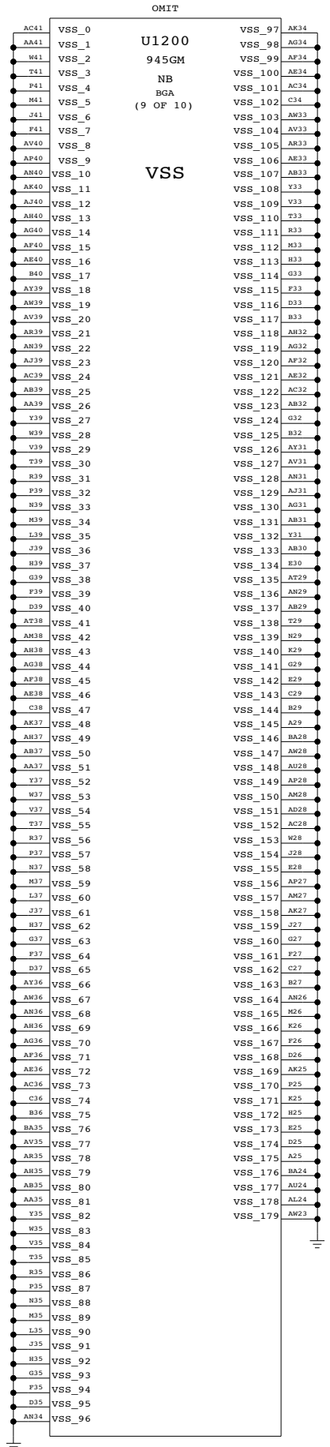
NB Power 2

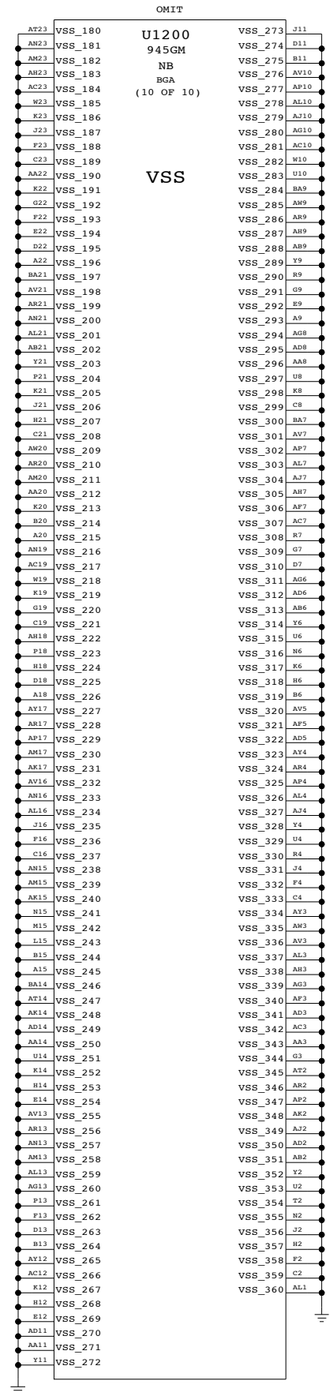
SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	17	87





NB Grounds

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	18	87

Power Interface

These are the power signals that leave the NB "block"

Rail Totals:

2310mA Max?
- PP1V05_S0 — 10mA Max?
- PP1V05_S0 — 1500mA Max
- PP1V05_S0 — 800mA Max
- PP1V05_S0 — 7mA Max

3674mA Max
- PP1V5_S0_NB — 7mA Max
- PP1V5_S0_NB — 1500mA Max
- PP1V5_S0_NB — 7mA Max
- PP1V5_S0_NB — 100mA Max
- PP1V5_S0_NB — 24mA Max
- PP1V5_S0_NB — 150mA Max
- PP1V5_S0_NB — 1900mA Max

3200mA Max
- PP1V8_S3 — 3200mA Max

132mA Max
- GND — 70mA Max
- PP2V5_S0 — 60mA Max
- PP2V5_S0 — 2mA Max

40mA Max?
- PP3V3_S0 — 40mA Max

PP1V05_S0 → PP1V05_S0 ×6, GND, GND

PP1V5_S0_NB → PP1V5_S0_NB ×8

TP_CRT_DDC_CLK — MAKE_BASE=TRUE → TP_CRT_DDC_CLK

TP_CRT_DDC_DATA — MAKE_BASE=TRUE → TP_CRT_DDC_DATA

TP_LVDS_CLKCTLA → TP_LVDS_CLKCTLA

TP_LVDS_CLKCTLB — MAKE_BASE=TRUE → TP_LVDS_CLKCTLB

NC_NB_XOR_LVDS_A34 — MAKE_BASE=TRUE, NO_TEST=TRUE → NC_NB_XOR_LVDS_A34

NC_NB_XOR_LVDS_A35 — MAKE_BASE=TRUE, NO_TEST=TRUE → NC_NB_XOR_LVDS_A35

NC_NB_XOR_LVDS_D27 — MAKE_BASE=TRUE, NO_TEST=TRUE → NC_NB_XOR_LVDS_D27

NC_NB_XOR_LVDS_D28 — MAKE_BASE=TRUE, NO_TEST=TRUE → NC_NB_XOR_LVDS_D28

TP_SDVO_CTRLCLK — MAKE_BASE=TRUE → TP_SDVO_CTRLCLK

TP_SDVO_CTRLDATA — MAKE_BASE=TRUE → TP_SDVO_CTRLDATA

LVDS_IBG

R1990 1.5K 1% 1/16W MF-LF 402 — GND, GND

PP1V05_S0 → (MCH CRTDAC ANALOG 2.5V PWR) PP1V05_S0, GND

(MCH H/V SYNC 2.5V PWR) GND

PP1V5_S0_NB → (MCH TVDAC DEDICATED PWR 1.5V) PP1V5_S0_NB

(MCH TVDAC DIGITAL QUIET 1.5V PWR) PP1V5_S0_NB

(MCH TV OUT CHANNEL A 3.3V PWR) PP1V5_S0_NB

(MCH TV OUT CHANNEL B 3.3V PWR) PP1V5_S0_NB

(MCH TV OUT CHANNEL C 3.3V PWR) PP1V5_S0_NB

(MCH TV DAC BAND GAP 3.3V PWR) PP1V5_S0_NB — GND

GMCH CORE PWR 1.05V BYPASS

PP1V05_S0 — 1500mA Max

CRITICAL
- C1900 470uF 20% 2.5V TANT D2T
- C1902 10uF 20% 6.3V X5R 603
- C1903 10uF 20% 6.3V X5R 603
- C1904 1uF 10% 6.3V CERM 402
- C1905 0.22uF 20% 6.3V X5R 402
- C1906 0.22uF 20% 6.3V X5R 402
- C1907 0.22uF 20% 6.3V X5R 402

MCH VTT BYPASS (MCH FSB 1.05V PWR)

PP1V05_S0 — 800mA Max

- C1965 4.7uF 20% 6.3V CERM 603
- C1966 2.2uF 20% 6.3V CERM1 603

Layout Note: Place in cavity

MCH VCC_HV BYPASS (MCH HV BUFFER 3.3V PWR)

PP3V3_S0 — 40mA Max

- C1967 0.22uF 20% 6.3V X5R 402 (SHARE C0940 470UF)

Layout Note: Place on the edge

MCH VCCA_3GBG BYPASS (MCH PCIE/DMI BAND GAP 2.5V PWR)

PP2V5_S0 — 2mA Max

- C1914 10uF 20% 6.3V X5R 603
- C1915 0.1uF 20% 10V CERM 402
- C1916 0.1uF 20% 10V CERM 402

GMCH VCCAUX FILTER (MCH DDR DLL&IO, FSB HSIO&IO PWR 1.5V)

PP1V5_S0_NB — 1900mA Max

- C1918 0.1uF 20% 10V CERM 402

GMCH VCCA_HPLL FILTER (HOST PLL 1.5V PWR)

PP1V5_S0_NB — 100mA Max

- L1934 FERR-120-OHM-0.2A 0603
- C1934 22UF 20% 6.3V CERM 805
- C1935 0.1uF 20% 10V CERM 402

PP1V5_S0_NB_VCCA_HPLL — MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V — 45mA Max

GMCH VCCA_MPLL FILTER (MCH MEMORY PLL 1.5V PWR)

PP1V5_S0_NB — 1500mA Max

- L1936 FERR-120-OHM-0.2A 0603
- C1936 22UF 20% 6.3V CERM 805
- C1937 0.1uF 20% 10V CERM 402

PP1V5_S0_NB_VCCA_MPLL — MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V — 45mA Max

GMCH VCC3G FILTER (PCI-E/DMI ANALOG 1.5V PWR)

PP1V5_S0_NB — 1500mA Max

- L1970 91nH 1210
- C1970 220UF 20% 2.5V POLY CASE-B2

Layout Note: Place L and C close to MCH

- C1971 10uF 20% 6.3V X5R 603
- C1972 10uF 20% 6.3V X5R 603

Layout Note: 10uF caps should be close to MCH on opposite side.

PP1V5_S0_NB_VCC3G — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V — 1500mA Max

GMCH VCCA_3GPLL FILTER (3GIO PLL 1.5V PWR)

PP1V5_S0_NB → L1975 1.0UH-220MA-0.12-OHM 0805 → PP1V5_S0_NB_3GPLL_F — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.4 mm, VOLTAGE=1.5V → R1975 0.5 1% 1/16W MF-LF 402

- C1975 10uF 20% 6.3V X5R 603
- C1976 0.1uF 20% 10V CERM 402 — GND

Layout Note: 3GPLL 10uF cap should be placed in cavity

Layout Note: Route to caps, then GND

PP1V5_S0_NB_VCCA_3GPLL — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V

GMCH VCCA_DPLLA FILTER (CRT/TVOUT PLL 1.5V PWR)

NO STUFF — R1953 0 5% 1/16W MF-LF 402

PP1V5_S0_NB_VCCA_DPLLA — MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V — 50MA MAX

GMCH VCCA_DPLLB FILTER (LVDS PLL 1.5V PWR)

NO STUFF — R1954 0 5% 1/16W MF-LF 402

PP1V5_S0_NB_VCCA_DPLLB — MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V — 50MA MAX

CRITICAL

U1900 TPS73115 SOT23-5 — IN, EN, GND, OUT → PP1V5_S0_NB_DPLL, NR/FB → TPS73115_NR

PP2V5_S0

- C1950 1uF 10% 6.3V CERM 402
- C1951 0.01uF 10% 16V CERM 402
- C1952 10uF 20% 6.3V X5R 603
- C1953 0.1uF 20% 10V CERM 402
- C1954 0.1uF 20% 10V CERM 402

MCH VCC_TXLVDS BYPASS (MCH LVDS TRANSMITTER 2.5V PWR)

PP2V5_S0 — 60MA MAX

- C1990 4.7UF 20% 6.3V CERM 603
- C1991 0.1uF 20% 10V CERM 402

MCH VCCD_LVDS BYPASS (MCH LVDS DIGITAL 1.5V PWR)

PP1V5_S0_NB — 20MA MAX

- C1992 10uF 20% 6.3V X5R 603
- C1993 0.1uF 20% 10V CERM 402

MCH VCCA_LVDS BYPASS (MCH LVDS ANALOG 2.5V PWR)

PP2V5_S0 — 10MA MAX

- C1994 0.01UF 10% 16V CERM 402
- C1995 0.1uF 20% 10V CERM 402 — GND

Layout Note: Route to caps, then GND

NB (GM) Decoupling

SYNC_MASTER=M57_MLB_MG SYNC_DATE=08/08/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE: NONE SHT 19 OF 87

NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

14C6 NB_CFG<5>
Internal pull-up
NBCFG_DMI_X2
R2075 2.2K 5% 1/16W MF-LF 402

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

14C6 NB_CFG<7>
Internal pull-up
NO STUFF
R2077 2.2K 5% 1/16W MF-LF 402

NB_CFG<8>	RESERVED

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

14C6 NB_CFG<9>
Internal pull-up
NBCFG_PEG_REVERSE
R2079 2.2K 5% 1/16W MF-LF 402

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

14C6 NB_CFG<16>
Internal pull-up
NBCFG_DYN_ODT_DISABLE
R2085 2.2K 5% 1/16W MF-LF 402

NB_CFG<17>	RESERVED

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

PP3V3_S0
NBCFG_VCC_1V5
R2058 2.2K 5% 1/16W MF-LF 402
14C6 NB_CFG<18>
Internal pull-down

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

PP3V3_S0
NBCFG_DMI_REVERSE
R2059 2.2K 5% 1/16W MF-LF 402
14C6 NB_CFG<19>
Internal pull-down

945 External Design Spec says reserved

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

PP3V3_S0
NBCFG_SDVO_AND_PCIE
R2060 2.2K 5% 1/16W MF-LF 402
14B6 NB_CFG<20>
Internal pull-down

PROBABLY NOT NEEDED

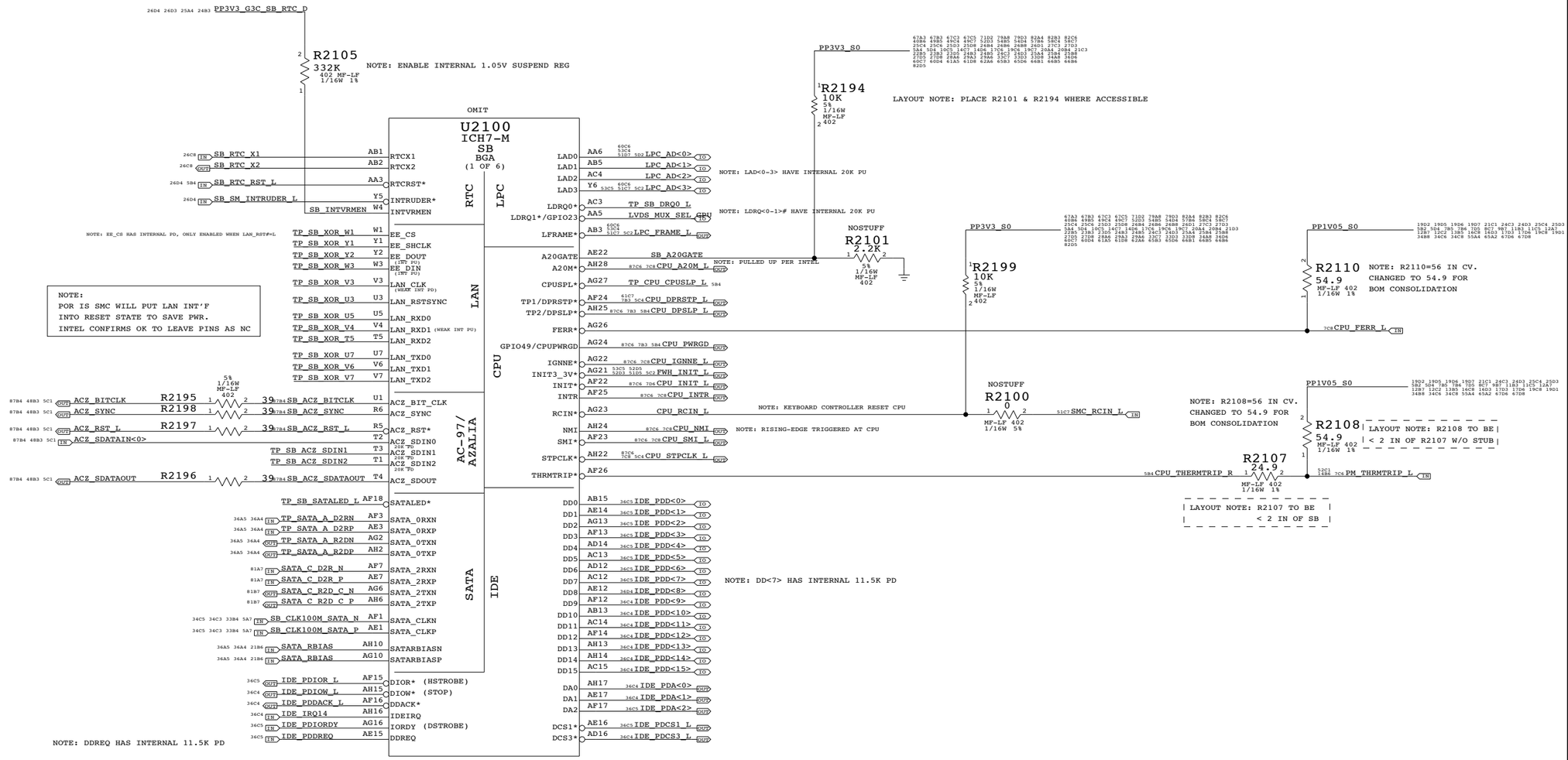
NB Config Straps

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	20	87



	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#		NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

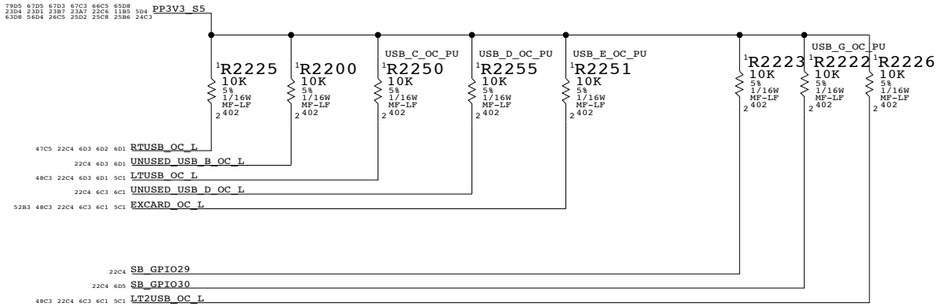
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

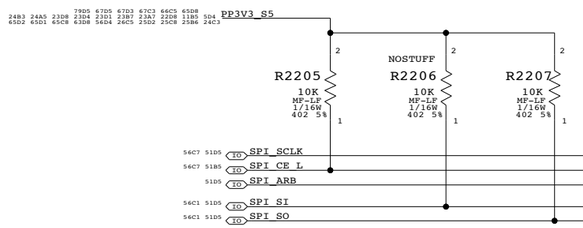
II NOT TO REPRODUCE OR COPY IT

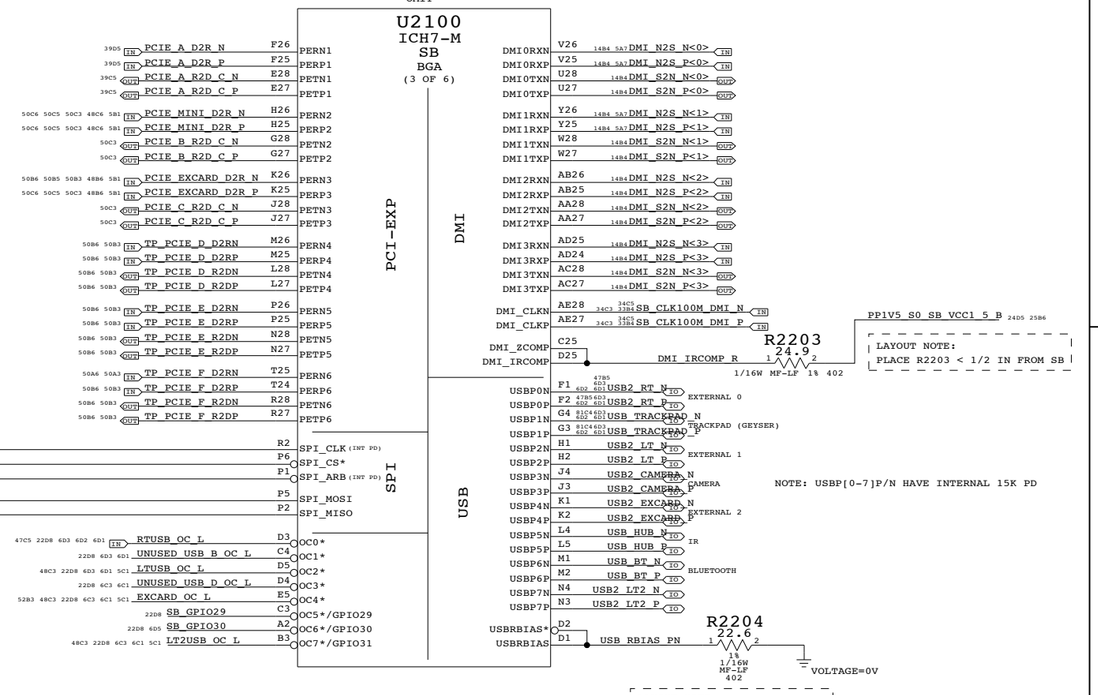
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

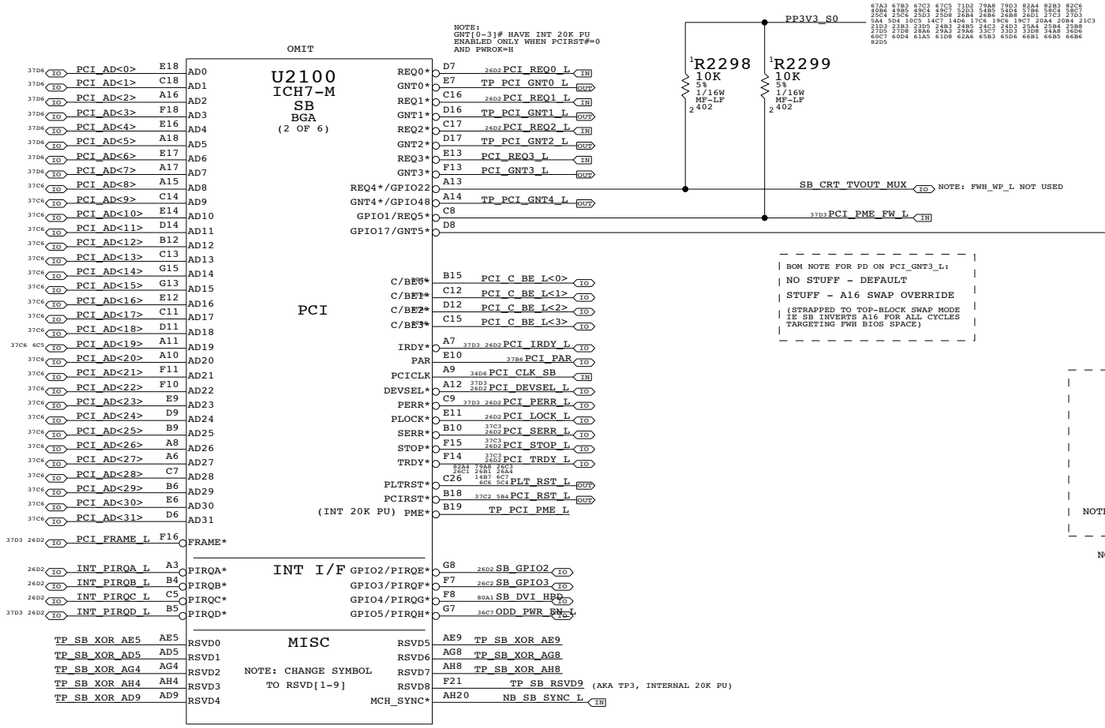
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 21 OF 87	









SB BOOT BIOS SELECT

	STRAP	GNT5# R2211	GNT4# R2210
LPC (DEFAULT)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

NOTE: GNT4# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
GNT5# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)

NOTE: R2210 WAS PD ON PIN A14 = FWH_TBL_L

SB: 2 OF 4

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 22 OF 87	

NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING 8 PWROK RISING:
SB WILL DISABLE TCO TIMER
SYSTEM REBOOT FEATURE

PP3V3_S0

PP3V3_S5

RP2300 10K 5% 1/16W SM-LF

R2318 10K 1/16W 402 MF-LF 5%
R2395 8.2K 1/16W 402 MF-LF 5%
R2396 10K 1/16W 402 MF-LF 5%
R2397 8.2K 1/16W 402 MF-LF 5%
R2327 10K 1/16W 402 MF-LF 5% NOSTUFF
R2326 10K 1/16W 402 MF-LF 5% NOSTUFF
R2323 1K 1/16W 402 MF-LF 5% NO_REBOOT_MODE

R2398 1K 1/16W 402 MF-LF 5%
R2320 10K 1/16W 402 MF-LF 5%
R2317 10K 1/16W 402 MF-LF 5%
R2316 10K 1/16W 402 MF-LF 5%

OMIT

U2100
ICH7-M
SB
BGA
(4 OF 6)

SMBUS_SB_SCL → SMBCLK C22
SMBUS_SB_SDA → SMBDATA B22
SMB_LINK_ALERT_L → LINKALERT* A26
SMLINK<0> → SMLINK0 B25
SMLINK<1> → SMLINK1 A25
NOT USED
PM_RI_L → RI* A28
SB_SPKR → SPKR (INT WEAK PD) A19
PM_SUS_STAT_L → SUS_STAT* A27
PM_SYSRST_L → SYS_RST* A22
PM_BMBUSY_L → GPIO0/BM_BUSY* AB18
SMB_ALERT_L → GPIO11/SMBALERT* B23
NOTE: RESERVED FOR FUTURE
PM_STPPCI_L → GPIO18/STPPCI* AC20
PM_STPCPU_L → GPIO20/STPCPU* AF21
SB_GPIO26 → GPIO26 A21
BIOS_REC → GPIO27 B21
FWH_MFG_MODE → GPIO28 E23
PM_CLKRUN_L → GPIO32/CLKRUN* AG18
GPU_D3COLD_RESET_L → GPIO33/AZ_DOCK_EN* AC19
TP_AZ_DOCK_RST_L → GPIO34/AZ_DOCK_RST* U2
PCIE_WAKE_L → WAKE* F20
INT_SERIRQ → SERIRQ AH21
PM_THRM_L → THRM* AF20
VR_PWRGD_CK410 → VRMPWRGD AD22
TP_SB_GPIO6 → GPIO6 AC21
GPIO7 AC18
GPIO8 E21

SMBUS
CLKS
SYS PWR MNGT
GPIO

SATA GPIO
GPIO21/SATA0GP AF19 SB_GPIO21 100 R2302
GPIO19/SATA1GP AH18 SB_GPIO19 100 R2303
GPIO36/SATA2GP AH19
GPIO37/SATA3GP AE19 SB_GPIO37 100 R2305
SATA_C_DET_L

CLK14 AC1 SB_CLK14P3M_TIMER
CLK48 B2 SB_CLK48M_USBCTLR
SUSCLK C20 TP_SB_SUS_CLK
SLP_S3* B24 PM_SLP_S3_L
SLP_S4* D23 PM_SLP_S4_L
SLP_S5* F22 PM_SLP_S5_L
PWROK AA4 PM_SB_PWROK
GPIO16/DPRSLPVR AC22 PM_DPRSLPVR
TP0/BATLOW* C21 NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN
(INT 20K PU) PWRBTN* C23 PM_PWRBTN_L
LAN_RST* C19 PM_LAN_ENABLE NOTE: SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F IN RESET STATE TO SAVE PWR
RSMRST* Y4
GPIO9 E20 SMS_INT_L
GPIO10 A20 SMC_SB_NMI
DEF=GPI GPIO12 F19 LAN_ENERGY_DET
GPIO13 E19
DEF=GPI GPIO14 R4 IDE_RESET_L
GPIO15 E22 SV_SET_UP
GPIO24 R3 CRB_SV_DET
GPIO25 D20 TP_SB_GPIO25_DO_NOT_USE
OD GPIO35 AD21 SB_CLK100M_SATA_OE_L
GPIO36 AD20 SB_GPUVCORE_DISABLE_L
DEF=GPI GPIO39 AE20 SATA_C_PWR_EN_L

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 350S AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

PP3V3_S5

R2319 10K 1/16W 402 MF-LF 5%
R2343 8.2K 1/16W 402 MF-LF 5%
R2399 100K 1/16W 402 MF-LF 5%

PM_BATLOW_L
PM_RSMRST_L
SMC_WAKE_SCI_L

PP3V3_S5

R2306 10K 1/16W 402 MF-LF 5% NOSTUFF
R2308 10K 1/16W 402 MF-LF 5%
R2307 10K 1/16W 402 MF-LF 5%
R2309 0 1/16W 402 MF-LF 5% NOSTUFF

SV_SET_UP
CRB_SV_DET

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

PP3V3_S0

R2388 10K 5% 1/16W MF-LF 402

SATA_C_PWR_EN_L

PP3V3_S5

R2313 10K 1/16W 402 MF-LF 5%
R2310 10K 1/16W 402 MF-LF 5%
R2314 0 1/16W 402 MF-LF 5% NOSTUFF
R2311 10K 1/16W 402 MF-LF 5% NOSTUFF

FWH_MFG_MODE
BIOS_REC

SB: 3 OF 4

SYNC_MASTER=M57_MLB_MG SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

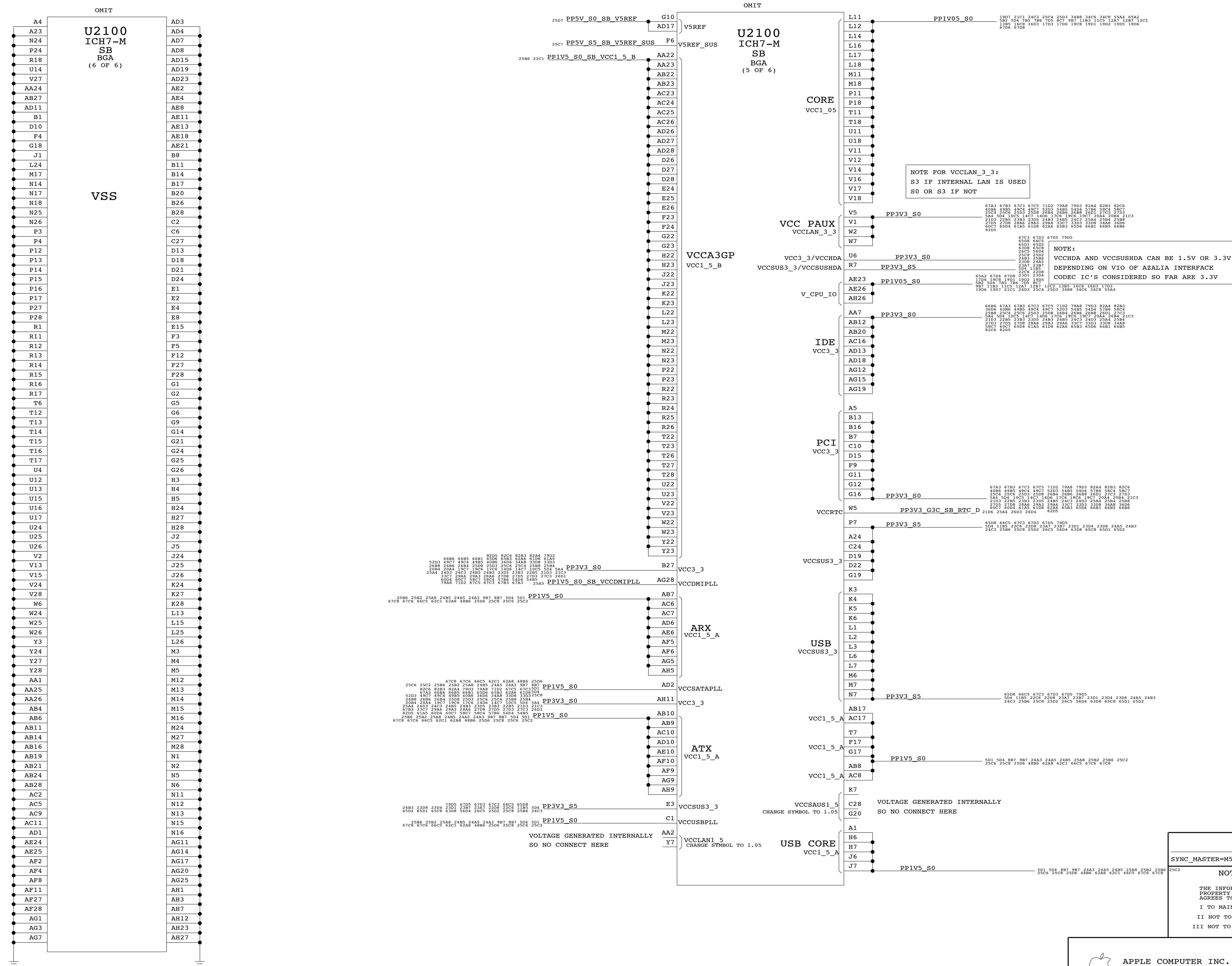
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 23 OF 87	



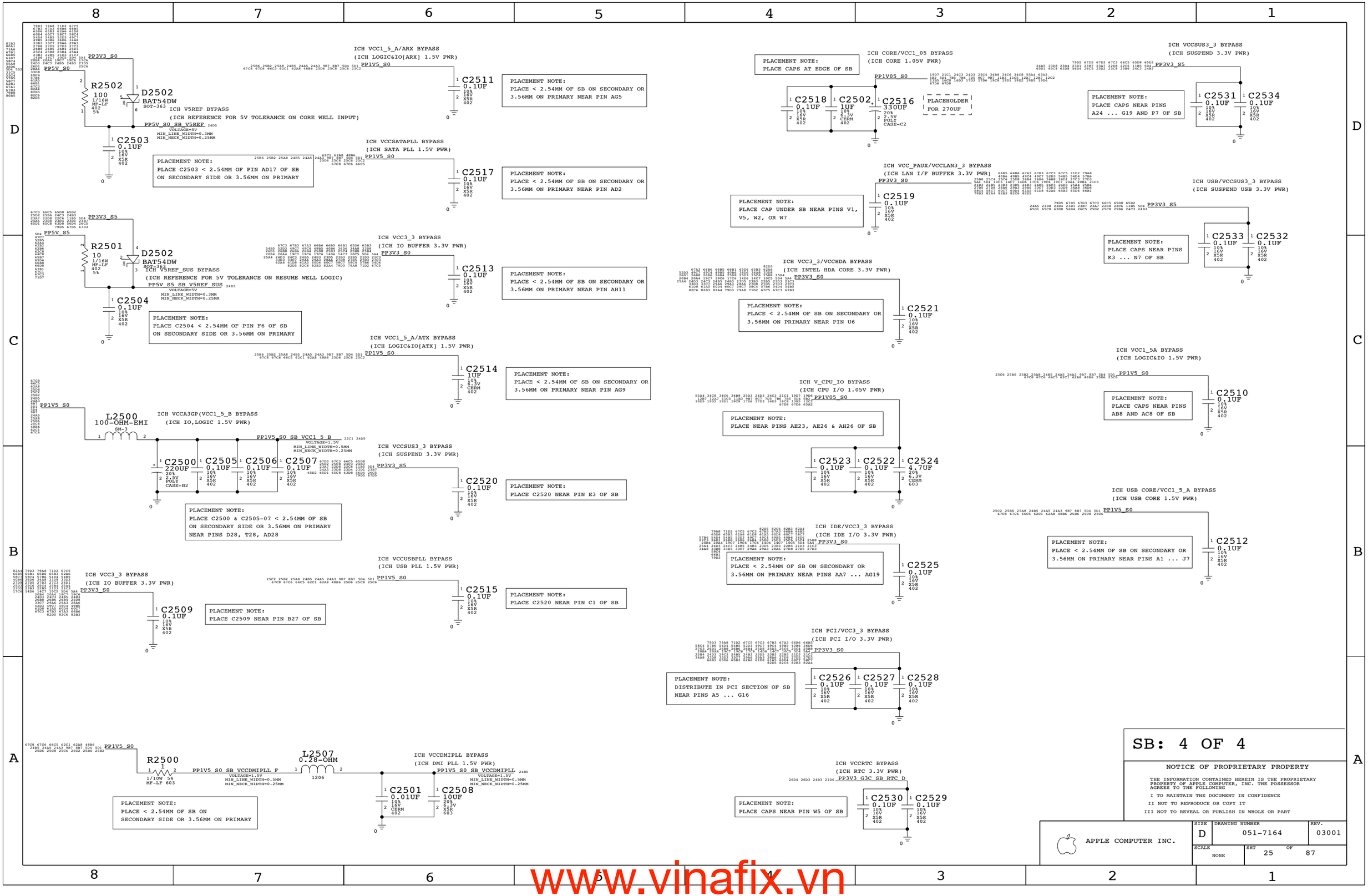
SB: 4 OF 4

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

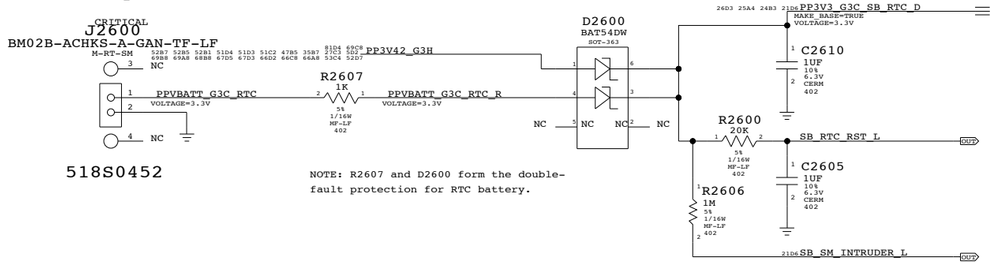
NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE NONE	SHT 24	OF 87

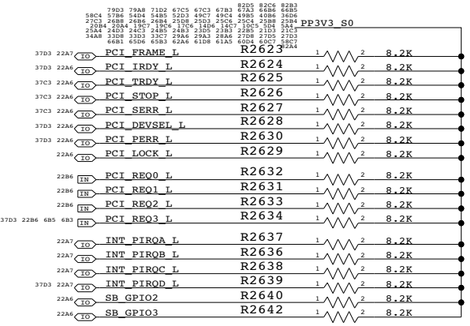


RTC Battery Connector



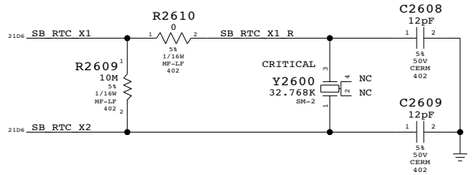
518S0452

NOTE: R2607 and D2600 form the double-fault protection for RTC battery.

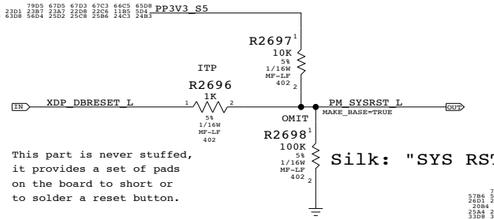


Pullup on SB_GPIO4 removed as it now defaults low for use as DVI_HPD in muxed graphics solution.

SB RTC Crystal Circuit



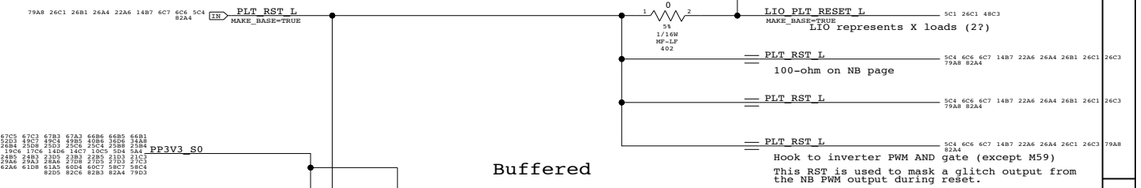
Platform Reset Connections



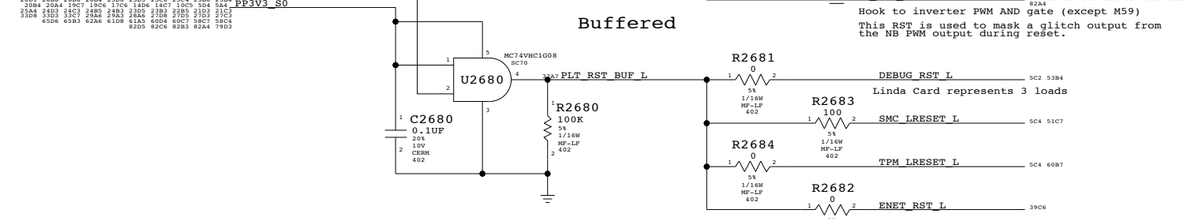
This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

Silk: "SYS RST"

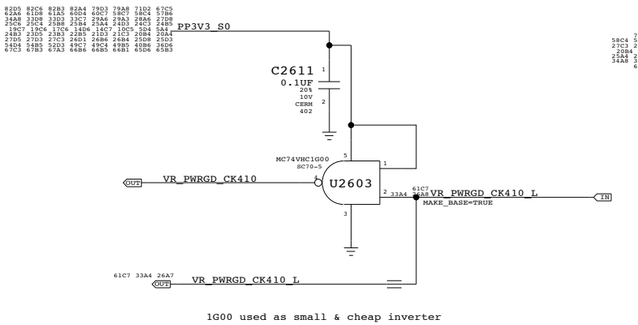
Unbuffered



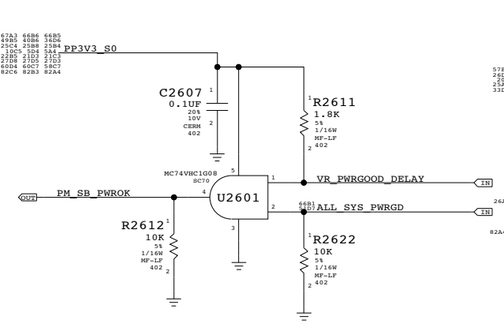
Buffered

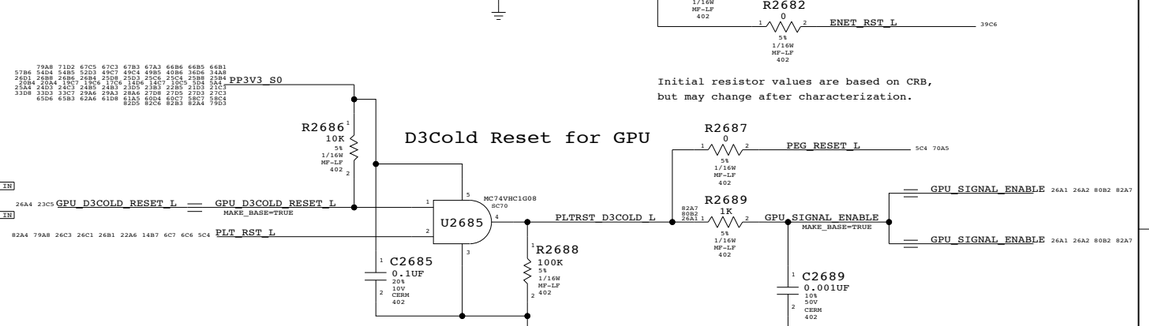


Initial resistor values are based on CRB, but may change after characterization.



1G00 used as small & cheap inverter





SB Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

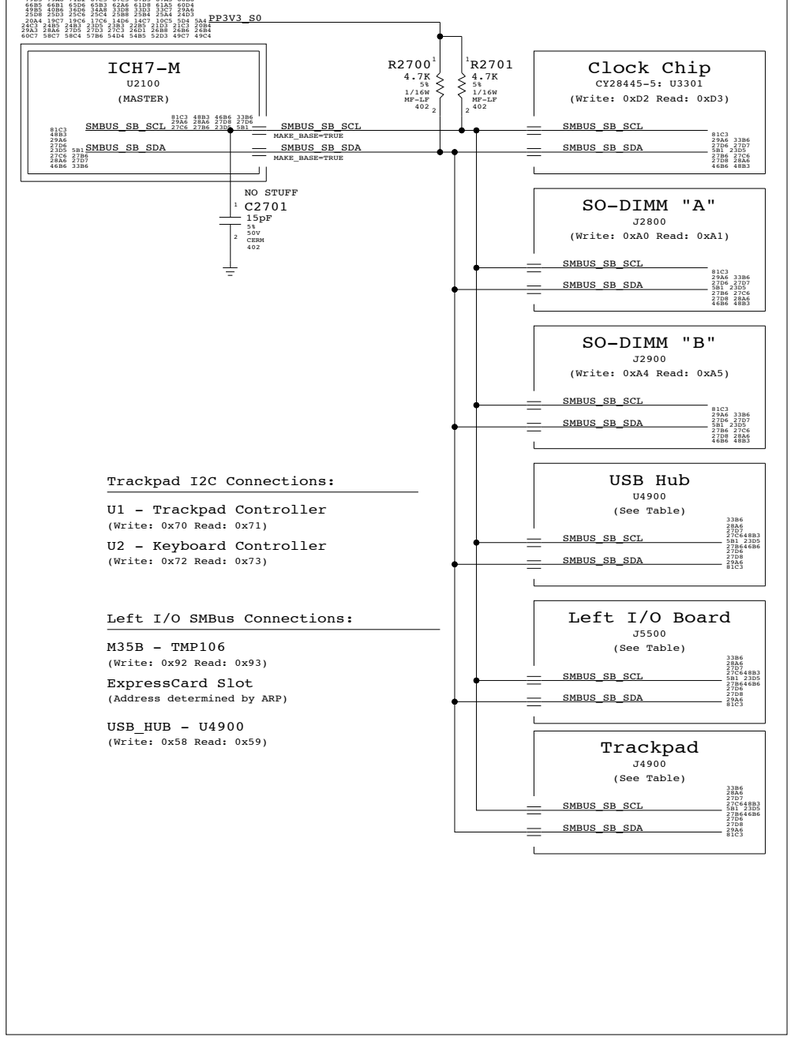
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 26 OF 87	

ICH7-M SMBus Connections



Trackpad I2C Connections:

U1 - Trackpad Controller
(Write: 0x70 Read: 0x71)

U2 - Keyboard Controller
(Write: 0x72 Read: 0x73)

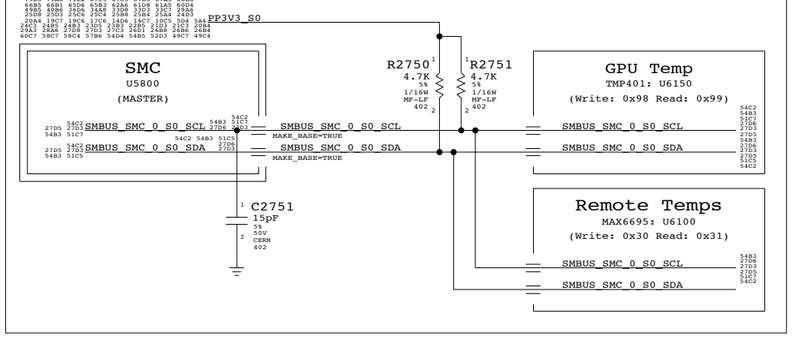
Left I/O SMBus Connections:

M35B - TMP106
(Write: 0x92 Read: 0x93)

ExpressCard Slot
(Address determined by ARP)

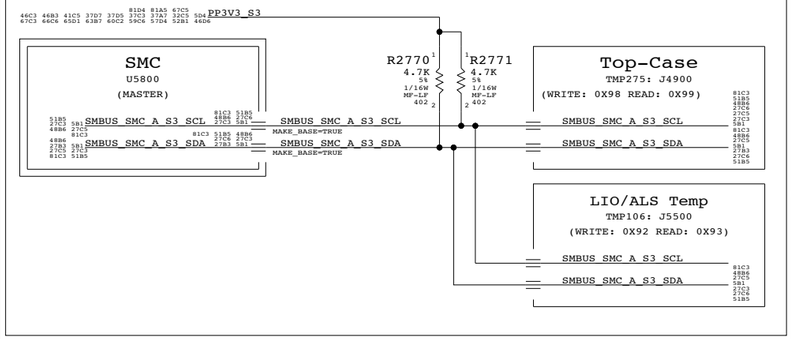
USB_HUB - U4900
(Write: 0x58 Read: 0x59)

SMC "0" SMBus Connections

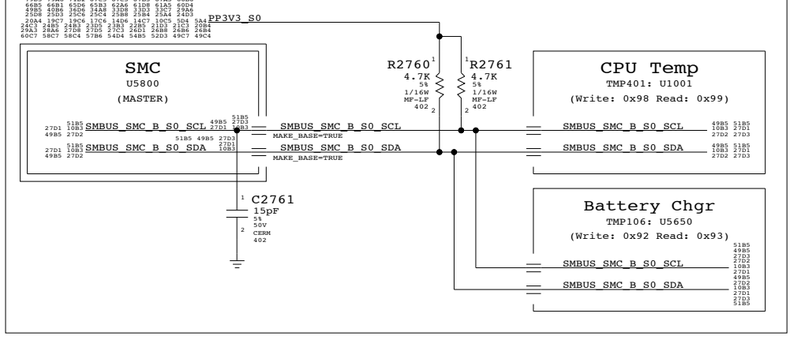


SMC "A" SMBus Connections

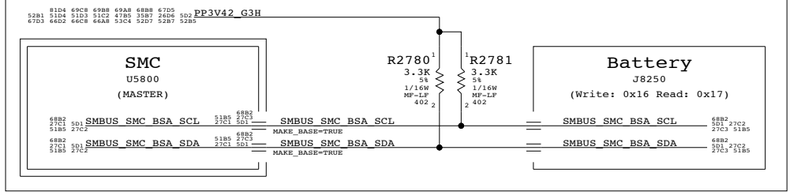
NOTE: SMC RMT bus remains powered and may be active in S3 state



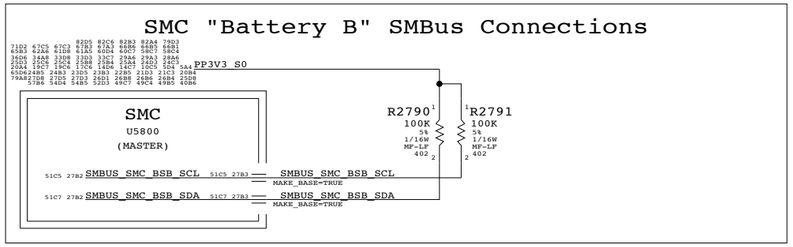
SMC "B" SMBus Connections



SMC "Battery A" SMBus Connections



SMC "Battery B" SMBus Connections



M57 SMBUS CONNECTIONS

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE: NONE SHT 27 OF 87

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

"Expansion" (surface-mount) slot

MEMVREF_OUT

C2801 2.2uF 20% 6.3V CERM1 603

C2800 0.1uF 20% 10V CERM 402

PP1V8_S3

J2800 DDR2-SODIMM-DUAL F-RT-SM-M9

CRITICAL

NC

KEY

1A	VREF		2A	VSS0			
3A	VSS1		4A	DQ4	MEM_A_DQ<8>	15C7	
5A	DQ0	MEM_A_DQ<14>	6A	DQ5	MEM_A_DQ<12>	15C7	
7A	DQ1	MEM_A_DQ<13>	8A	VSS2			
9A	VSS4		10A	DM0	MEM_A_DM<1>	15D5	
11A	DQS0*	MEM_A_DQS_N<1>	12A	VSS5			
13A	DQS0	MEM_A_DQS_P<1>	14A	DQ6	MEM_A_DQ<15>	15C7	
15A	VSS6		16A	DQ7	MEM_A_DQ<9>	15C7	
17A	DQ2	MEM_A_DQ<10>	18A	VSS7			
19A	DQ3	MEM_A_DQ<11>	20A	DQ12	MEM_A_DQ<2>	15D7	
21A	VSS8		22A	DQ13	MEM_A_DQ<3>	15D7	
23A	DQ8	MEM_A_DQ<5>	24A	VSS9			
25A	DQ9	MEM_A_DQ<4>	26A	DM1	MEM_A_DM<0>	15D5	
27A	VSS10		28A	VSS11			
29A	DQS1*	MEM_A_DQS_N<0>	30A	CK0	MEM_CLK_P<0>	14D4	
31A	DQS1	MEM_A_DQS_P<0>	32A	CK0*	MEM_CLK_N<0>	14D4	
33A	VSS12		34A	VSS13			
35A	DQ10	MEM_A_DQ<6>	36A	DQ14	MEM_A_DQ<1>	15D7	
37A	DQ11	MEM_A_DQ<7>	38A	DQ15	MEM_A_DQ<0>	15D7	
39A	VSS14		40A	VSS15			
41A	VSS16		42A	VSS17			
43A	DQ16	MEM_A_DQ<19>	44A	DQ20	MEM_A_DQ<23>	15C7	
45A	DQ17	MEM_A_DQ<18>	46A	DQ21	MEM_A_DQ<22>	15C7	
47A	VSS18		48A	VSS19			
49A	DQS2*	MEM_A_DQS_N<2>	50A	NC0	PM_EXTTS_L	14B7 29C3 51B7 52D3 52D5	
51A	DQS2	MEM_A_DQS_P<2>	52A	DM2	MEM_A_DM<2>	15D5	
53A	VSS21		54A	VSS22			
55A	DQ18	MEM_A_DQ<20>	56A	DQ22	MEM_A_DQ<21>	15C7	
57A	DQ19	MEM_A_DQ<16>	58A	DQ23	MEM_A_DQ<17>	15C7	
59A	VSS23		60A	VSS24			
61A	DQ24	MEM_A_DQ<28>	62A	DQ28	MEM_A_DQ<29>	15C7	
63A	DQ25	MEM_A_DQ<25>	64A	DQ29	MEM_A_DQ<24>	15C7	
65A	VSS25		66A	VSS26			
67A	DM3	MEM_A_DM<3>	68A	DQS3*	MEM_A_DQS_N<3>	15C5	
69A	NC1	NC	70A	DQS3	MEM_A_DQS_P<3>	15C5	
71A	VSS27		72A	VSS28			
73A	DQ26	MEM_A_DQ<27>	74A	DQ30	MEM_A_DQ<26>	15C7	
75A	DQ27	MEM_A_DQ<30>	76A	DQ31	MEM_A_DQ<31>	15C7	
77A	VSS29		78A	VSS30			
79A	CKE0	30D6 14C4 MEM_CKE<0>	80A	NC/CKE1	MEM_CKE<1>	14C4 30D6	
81A	VDD0		82A	VDD1			
83A	NC2	NC	84A	NC/A15	NC_MEM_A_A<15>	4D7	
85A	BA2	30B6 15D5 MEM_A_BS<2>	86A	NC/A14	NC_MEM_A_A<14>	4D7	
87A	VDD2		88A	VDD3			
89A	A12	30C6 15B5 MEM_A_A<12>	90A	A11	MEM_A_A<11>	15B5 30C6	
91A	A9	30C6 15B5 MEM_A_A<9>	92A	A7	MEM_A_A<7>	15B5 30C6	
93A	A8	30C6 15B5 MEM_A_A<8>	94A	A6	MEM_A_A<6>	15B5 30C6	
95A	VDD4		96A	VDD5			
97A	A5	30C6 15B5 MEM_A_A<5>	98A	A4	MEM_A_A<4>	15B5 30C6	
99A	A3	30C6 15B5 MEM_A_A<3>	100A	A2	MEM_A_A<2>	15C5 30C6	
101A	A1	30C6 15C5 MEM_A_A<1>	102A	A0	MEM_A_A<0>	15C5 30C6	
103A	VDD6		104A	VDD7			
105A	A10/AP	30C6 15B5 MEM_A_A<10>	106A	BA1	MEM_A_BS<1>	15D5 30B6	
107A	BA0	30B6 15D5 MEM_A_BS<0>	108A	RAS*	MEM_A_RAS_L	15B5 30B6	
109A	WE*	30B6 15B5 MEM_A_WE_L	110A	S0*	MEM_CS_L<0>	14C4 30D6	
111A	VDD8		112A	VDD9			
113A	CAS*	30B6 15D5 MEM_A_CAS_L	114A	ODT0	MEM_ODT<0>	14C4 30C6	
115A	NC/S1*	30D6 14C4 MEM_CS_L<1>	116A	NC/A13	MEM_A_A<13>	15B5 30C6	
117A	VDD10		118A	VDD11			
119A	NC/ODT1	30C6 14C4 MEM_ODT<1>	120A	NC3	NC		
121A	VSS31		122A	VSS32			
123A	DQ32	15B7 MEM_A_DQ<35>	124A	DQ36	MEM_A_DQ<38>	15B7	
125A	DQ33	15B7 MEM_A_DQ<39>	126A	DQ37	MEM_A_DQ<34>	15B7	
127A	VSS33		128A	VSS34			
129A	DQS4*	15C5 MEM_A_DQS_N<4>	130A	DM4	MEM_A_DM<4>	15C5	
131A	DQS4	15C5 MEM_A_DQS_P<4>	132A	VSS35			
133A	VSS36		134A	DQ38	MEM_A_DQ<32>	15C7	
135A	DQ34	15B7 MEM_A_DQ<37>	136A	DQ39	MEM_A_DQ<36>	15B7	
137A	DQ35	15C7 MEM_A_DQ<33>	138A	VSS37			
139A	VSS38		140A	DQ44	MEM_A_DQ<57>	15B7	
141A	DQ40	15A7 MEM_A_DQ<60>	142A	DQ45	MEM_A_DQ<63>	15A7	
143A	DQ41	15B7 MEM_A_DQ<59>	144A	VSS39			
145A	VSS40		146A	DQS5*	MEM_A_DQS_N<7>	15C5	
147A	DM5	15C5 MEM_A_DM<7>	148A	DQS5	MEM_A_DQS_P<7>	15C5	
149A	VSS41		150A	VSS42			
151A	DQ42	15B7 MEM_A_DQ<58>	152A	DQ46	MEM_A_DQ<56>	15B7	
153A	DQ43	15A7 MEM_A_DQ<61>	154A	DQ47	MEM_A_DQ<62>	15A7	
155A	VSS43		156A	VSS44			
157A	DQ48	15B7 MEM_A_DQ<43>	158A	DQ52	MEM_A_DQ<40>	15B7	
159A	DQ49	15B7 MEM_A_DQ<45>	160A	DQ53	MEM_A_DQ<42>	15B7	
161A	VSS45		162A	VSS46			
163A	NC_TEST	NC	164A	CK1	MEM_CLK_P<1>	14D4	
165A	VSS47		166A	CK1*	MEM_CLK_N<1>	14D4	
167A	DQS6*	15C5 MEM_A_DQS_N<5>	168A	VSS48			
169A	DQS6	15C5 MEM_A_DQS_P<5>	170A	DM6	MEM_A_DM<5>	15C5	
171A	VSS49		172A	VSS50			
173A	DQ50	15B7 MEM_A_DQ<41>	174A	DQ54	MEM_A_DQ<47>	15B7	
175A	DQ51	15B7 MEM_A_DQ<46>	176A	DQ55	MEM_A_DQ<44>	15B7	
177A	VSS51		178A	VSS52			
179A	DQ56	15B7 MEM_A_DQ<51>	180A	DQ60	MEM_A_DQ<54>	15B7	
181A	DQ57	15B7 MEM_A_DQ<50>	182A	DQ61	MEM_A_DQ<55>	15B7	
183A	VSS53		184A	VSS54			
185A	DM7	15C5 MEM_A_DM<6>	186A	DQS7*	MEM_A_DQS_N<6>	15C5	
187A	VSS55		188A	DQS7	MEM_A_DQS_P<6>	15C5	
189A	DQ58	15B7 MEM_A_DQ<53>	190A	VSS56			
191A	DQ59	15B7 MEM_A_DQ<48>	192A	DQ62	MEM_A_DQ<52>	15B7	
193A	VSS57		194A	DQ63	MEM_A_DQ<49>	15B7	
195A	SDA	PP3V3_S0 SMBUS_SB_SDA	196A	VSS58			
197A	SCL	SMBUS_SB_SCL	198A	SA0			
199A	VDDSPD		200A	SA1	ADDR=0xA0(WR)/0xA1(RD)		
202	NC		203	NC			
204			201				

516S0471

DDR2 Bypass Caps

(For return current)

PP1V8_S3

C2808 10UF 20% 6.3V X5R 603

C2809 10UF 20% 6.3V X5R 603

C2810 1UF 10% 6.3V CERM 402

C2811 1UF 10% 6.3V CERM 402

C2812 1UF 10% 6.3V CERM 402

C2813 1UF 10% 6.3V CERM 402

C2814 1UF 10% 6.3V CERM 402

C2815 1UF 10% 6.3V CERM 402

C2816 1UF 10% 6.3V CERM 402

C2817 1UF 10% 6.3V CERM 402

C2818 1UF 10% 6.3V CERM 402

C2819 1UF 10% 6.3V CERM 402

C2820 1UF 10% 6.3V CERM 402

C2821 1UF 10% 6.3V CERM 402

DDR2 SO-DIMM Connector A

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 28 OF 87	

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

"Factory" (thru-hole) slot

PP1V8_S3

MEMVREF_OUT

C2901 2.2uF 20% 6.3V CERM1 603

C2900 0.1uF 20% 10V CERM 402

CRITICAL
J2900
F-RT-TH1
DDR2-SODIMM-DUAL

	1	VREF	VSS0	2			
	3	VSS1	DQ4	4	MEM_B_DQ<9>	15C4	
MEM_B_DQ<15>	15C4	5	DQ0	DQ5	6	MEM_B_DQ<11>	15C4
MEM_B_DQ<14>	15C4	7	DQ1	VSS2	8		
	9	VSS4	DM0	10	MEM_B_DM<1>	15D2	
MEM_B_DQS_N<1>	15C2	11	DQS0*	VSS5	12		
MEM_B_DQS_P<1>	15C2	13	DQS0	DQ6	14	MEM_B_DQ<12>	15C4
	15	VSS6	DQ7	16	MEM_B_DQ<8>	15C4	
MEM_B_DQ<10>	15C4	17	DQ2	VSS7	18		
MEM_B_DQ<13>	15C4	19	DQ3	DQ12	20	MEM_B_DQ<3>	15D4
	21	VSS8	DQ13	22	MEM_B_DQ<6>	15D4	
MEM_B_DQ<7>	15D4	23	DQ8	VSS9	24		
MEM_B_DQ<2>	15D4	25	DQ9	DM1	26	MEM_B_DM<0>	15D2
	27	VSS10	VSS11	28			
MEM_B_DQS_N<0>	15C2	29	DQS1*	CK0	30	MEM_CLK_P<3>	14D4
MEM_B_DQS_P<0>	15C2	31	DQS1	CK0*	32	MEM_CLK_N<3>	14D4
	33	VSS12	VSS13	34			
MEM_B_DQ<1>	15D4	35	DQ10	DQ14	36	MEM_B_DQ<0>	15D4
MEM_B_DQ<4>	15D4	37	DQ11	DQ15	38	MEM_B_DQ<5>	15D4
	39	VSS14	VSS15	40			
	41	VSS16	VSS17	42			
MEM_B_DQ<21>	15C4	43	DQ16	DQ20	44	MEM_B_DQ<22>	15C4
MEM_B_DQ<19>	15C4	45	DQ17	DQ21	46	MEM_B_DQ<18>	15C4
	47	VSS18	VSS19	48			
MEM_B_DQS_N<2>	15C2	49	DQS2*	NC0	50	PM_EXTTS_L	14B7 28C3 51B7 52D3 52D5
MEM_B_DQS_P<2>	15C2	51	DQS2	DM2	52	MEM_B_DM<2>	15D2
	53	VSS21	VSS22	54			
MEM_B_DQ<20>	15C4	55	DQ18	DQ22	56	MEM_B_DQ<17>	15C4
MEM_B_DQ<23>	15C4	57	DQ19	DQ23	58	MEM_B_DQ<16>	15C4
	59	VSS23	VSS24	60			
MEM_B_DQ<29>	15C4	61	DQ24	DQ28	62	MEM_B_DQ<26>	15C4
MEM_B_DQ<24>	15C4	63	DQ25	DQ29	64	MEM_B_DQ<28>	15C4
	65	VSS25	VSS26	66			
MEM_B_DM<3>	15C2	67	DM3	DQS3*	68	MEM_B_DQS_N<3>	15C2
NC		69	NC1	DQS3	70	MEM_B_DQS_P<3>	15C2
	71	VSS27	VSS28	72			
MEM_B_DQ<27>	15C4	73	DQ26	DQ30	74	MEM_B_DQ<31>	15C4
MEM_B_DQ<25>	15C4	75	DQ27	DQ31	76	MEM_B_DQ<30>	15C4
	77	VSS29	VSS30	78			
MEM_CKE<2>	30D6 14C4	79	CKE0	NC/CKE1	80	MEM_CKE<3>	14C4 30D6
	81	VDD0	VDD1	82			
NC		83	NC2	NC/A15	84	NC_MEM_B_A<15>	6D7
MEM_B_BS<2>	30A6 15D2	85	BA2	NC/A14	86	NC_MEM_B_A<14>	6D7
	87	VDD2	VDD3	88			
MEM_B_A<12>	30B6 15B2	89	A12	A11	90	MEM_B_A<11>	15B2 30B6
MEM_B_A<9>	30B6 15B2	91	A9	A7	92	MEM_B_A<7>	15B2 30B6
MEM_B_A<8>	30B6 15B2	93	A8	A6	94	MEM_B_A<6>	15B2 30B6
	95	VDD4	VDD5	96			
MEM_B_A<5>	30B6 15B2	97	A5	A4	98	MEM_B_A<4>	15B2 30B6
MEM_B_A<3>	30B6 15B2	99	A3	A2	100	MEM_B_A<2>	15C2 30B6
MEM_B_A<1>	30B6 15C2	101	A1	A0	102	MEM_B_A<0>	15C2 30B6
	103	VDD6	VDD7	104			
MEM_B_A<10>	30B6 15B2	105	A10/AP	BA1	106	MEM_B_BS<1>	15D2 30A6
MEM_B_BS<0>	30A6 15D2	107	BA0	RAS*	108	MEM_B_RAS_L	15B2 30A6
MEM_B_WE_L	30A6 15B2	109	WE*	S0*	110	MEM_CS_L<2>	14C4 30D6
	111	VDD8	VDD9	112			
MEM_B_CAS_L	30A6 15D2	113	CAS*	ODT0	114	MEM_ODT<2>	14C4 30D6
MEM_CS_L<3>	30D6 14C4	115	NC/S1*	NC/A13	116	MEM_B_A<13>	15B2 30B6
	117	VDD10	VDD11	118			
MEM_ODT<3>	30C6 14C4	119	NC/ODT1	NC3	120	NC	
	121	VSS31	VSS32	122			
MEM_B_DQ<36>	15B4	123	DQ32	DQ36	124	MEM_B_DQ<32>	15C4
MEM_B_DQ<33>	15C4	125	DQ33	DQ37	126	MEM_B_DQ<37>	15B4
	127	VSS33	VSS34	128			
MEM_B_DQS_N<4>	15C2	129	DQS4*	DM4	130	MEM_B_DM<4>	15C2
MEM_B_DQS_P<4>	15C2	131	DQS4	VSS35	132		
	133	VSS36	DQ38	134	MEM_B_DQ<38>	15B4	
MEM_B_DQ<34>	15B4	135	DQ34	DQ39	136	MEM_B_DQ<39>	15B4
MEM_B_DQ<35>	15B4	137	DQ35	VSS37	138		
	139	VSS38	DQ44	140	MEM_B_DQ<44>	15B4	
MEM_B_DQ<40>	15B4	141	DQ40	DQ45	142	MEM_B_DQ<45>	15B4
MEM_B_DQ<41>	15B4	143	DQ41	VSS39	144		
	145	VSS40	DQS5*	146	MEM_B_DQS_N<5>	15C2	
MEM_B_DM<5>	15C2	147	DM5	DQS5	148	MEM_B_DQS_P<5>	15C2
	149	VSS41	VSS42	150			
MEM_B_DQ<42>	15B4	151	DQ42	DQ46	152	MEM_B_DQ<46>	15B4
MEM_B_DQ<43>	15B4	153	DQ43	DQ47	154	MEM_B_DQ<47>	15B4
	155	VSS43	VSS44	156			
MEM_B_DQ<62>	15A4	157	DQ48	DQ52	158	MEM_B_DQ<58>	15B4
MEM_B_DQ<59>	15B4	159	DQ49	DQ53	160	MEM_B_DQ<63>	15A4
	161	VSS45	VSS46	162			
NC		163	NC_TEST	CK1	164	MEM_CLK_P<2>	14D4
	165	VSS47	CK1*	166	MEM_CLK_N<2>	14D4	
MEM_B_DQS_N<7>	15C2	167	DQS6*	VSS48	168		
MEM_B_DQS_P<7>	15C2	169	DQS6	DM6	170	MEM_B_DM<7>	15C2
	171	VSS49	VSS50	172			
MEM_B_DQ<60>	15A4	173	DQ50	DQ54	174	MEM_B_DQ<56>	15B4
MEM_B_DQ<61>	15A4	175	DQ51	DQ55	176	MEM_B_DQ<57>	15B4
	177	VSS51	VSS52	178			
MEM_B_DQ<54>	15B4	179	DQ56	DQ60	180	MEM_B_DQ<55>	15B4
MEM_B_DQ<51>	15B4	181	DQ57	DQ61	182	MEM_B_DQ<50>	15B4
	183	VSS53	VSS54	184			
MEM_B_DM<6>	15C2	185	DM7	DQS7*	186	MEM_B_DQS_N<6>	15C2
	187	VSS55	DQS7	188	MEM_B_DQS_P<6>	15C2	
MEM_B_DQ<52>	15B4	189	DQ58	VSS56	190		
MEM_B_DQ<49>	15B4	191	DQ59	DQ62	192	MEM_B_DQ<53>	15B4
	193	VSS57	DQ63	194	MEM_B_DQ<48>	15B4	
PP3V3_S0		195	SDA	VSS58	196	Resistor prevents pwr-gnd short	
SMBUS_SB_SDA		197	SCL	SA0	198		
SMBUS_SB_SCL		199	VDDSPD	SA1	200	SODIMM_A_SA1	

201 NC

202 NC

516-0140

ADDR=0xA4(WR)/0xA5(RD)

PP3V3_S0

R2900 10K 5% 1/16W MF-LF 402

DDR2 Bypass Caps

(For return current)

PP1V8_S3

C2908	10UF	20% 6.3V	X5R 603
C2909	10UF	20% 6.3V	X5R 603
C2910	1UF	10% 6.3V	CERM 402
C2911	0.1uF	20% 10V	CERM 402
C2912	1UF	10% 6.3V	CERM 402
C2913	1UF	10% 6.3V	CERM 402
C2914	1UF	10% 6.3V	CERM 402
C2915	1UF	10% 6.3V	CERM 402
C2916	1UF	10% 6.3V	CERM 402
C2917	0.1uF	20% 10V	CERM 402
C2918	0.1uF	20% 10V	CERM 402
C2919	0.1uF	20% 10V	CERM 402
C2920	0.1uF	20% 10V	CERM 402
C2921	0.1uF	20% 10V	CERM 402

DDR2 SO-DIMM Connector B

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

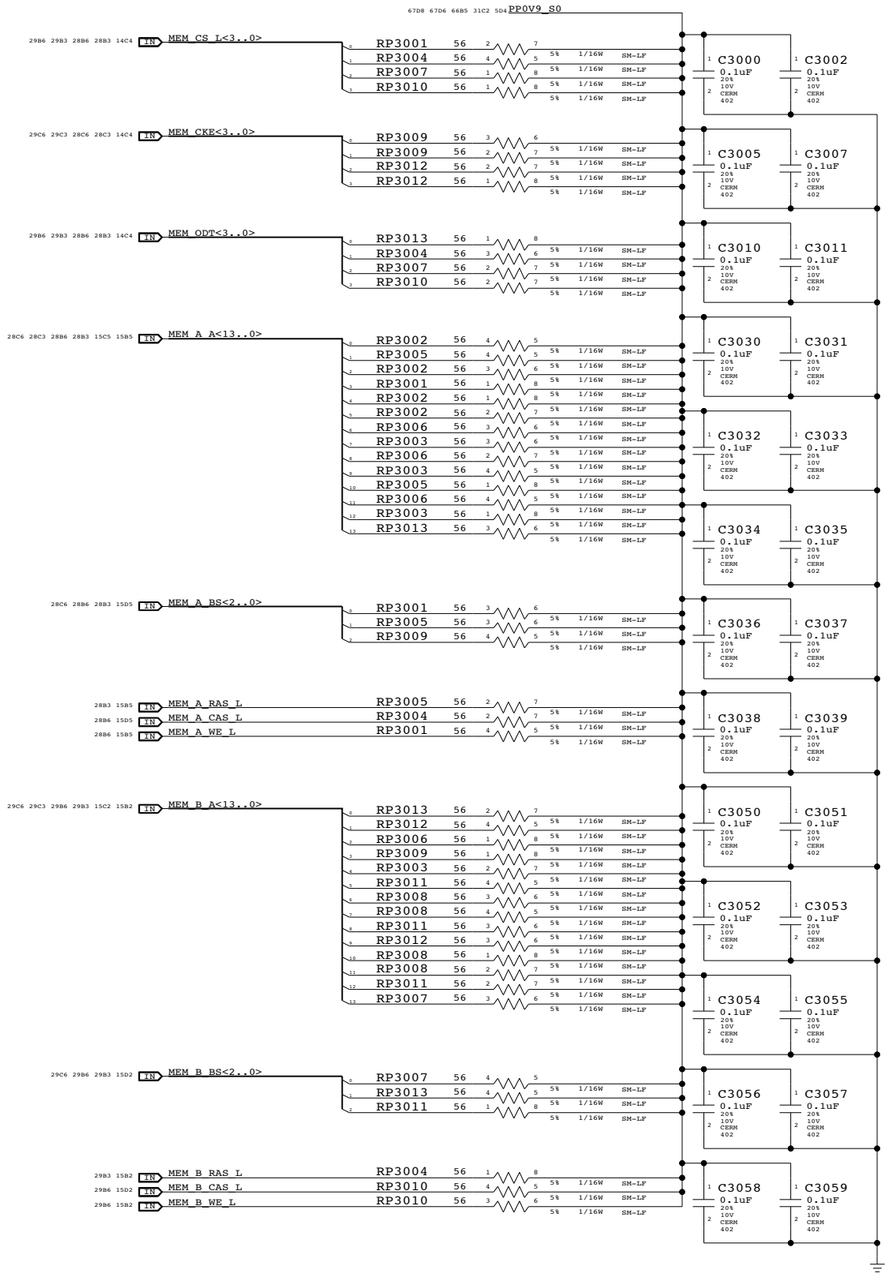
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 29 OF 87	

One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE NONE SHT 30 OF 87

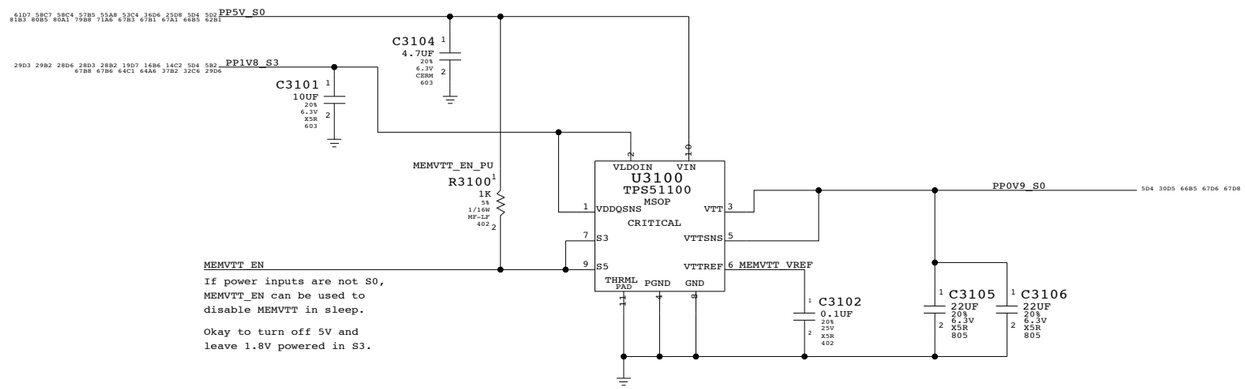
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



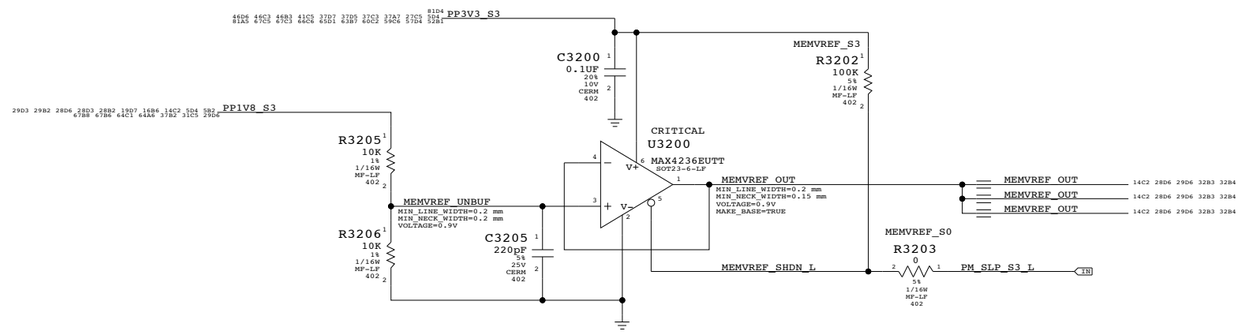
Memory Vtt Supply

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE: NONE SHT 31 OF 87



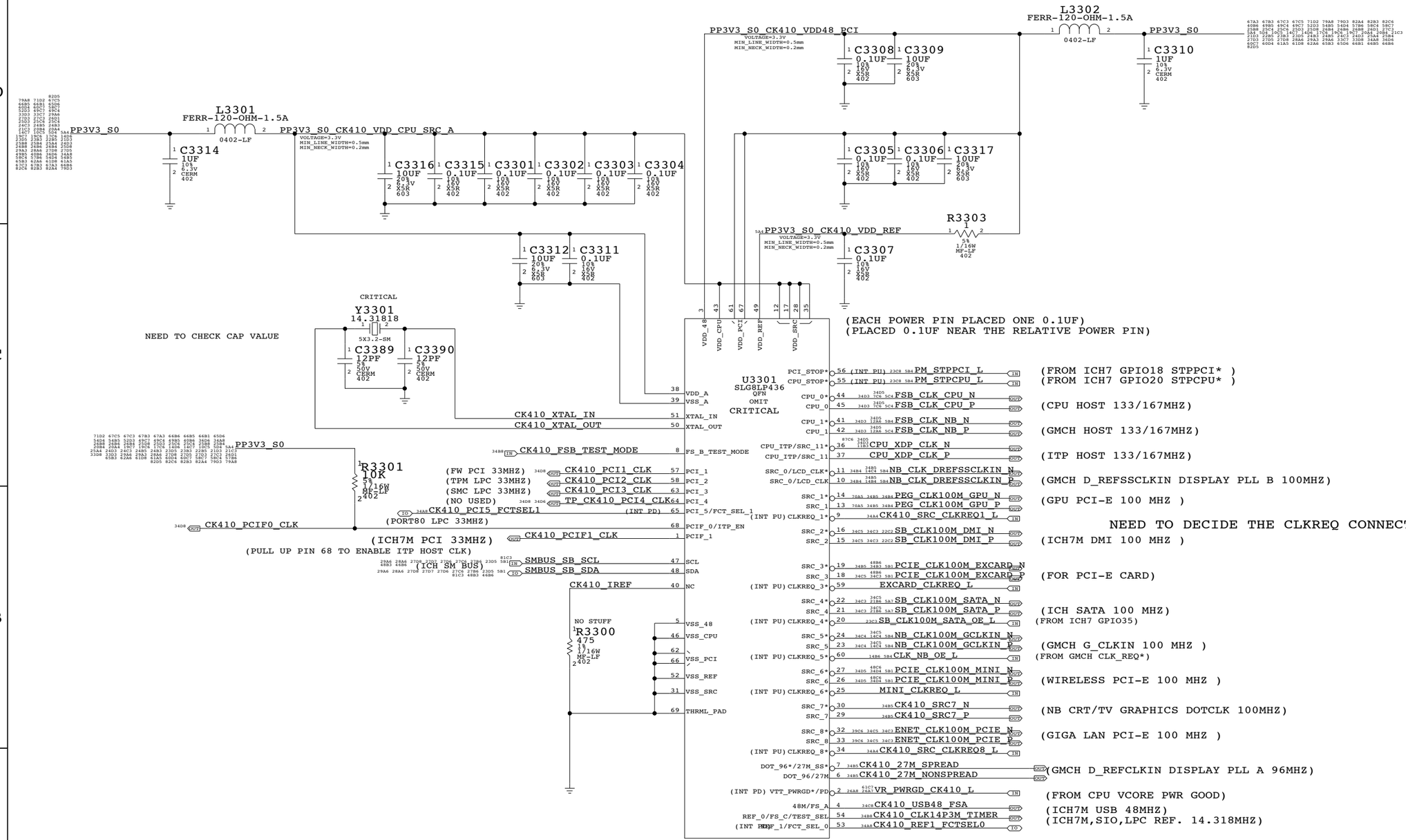
DDR2 VRef

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE: NONE SHT 32 OF 87



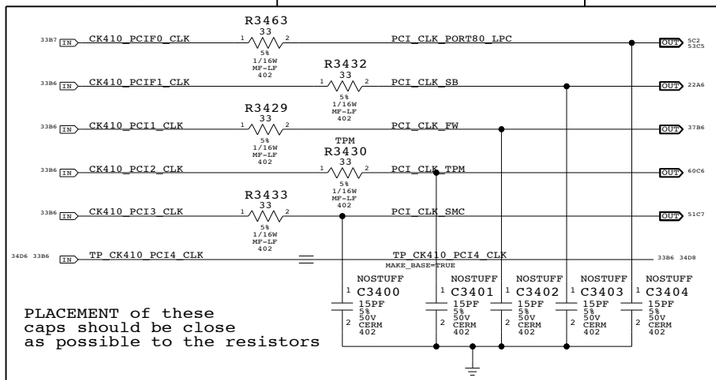
FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	TBD	SRCT0	SRCC0	

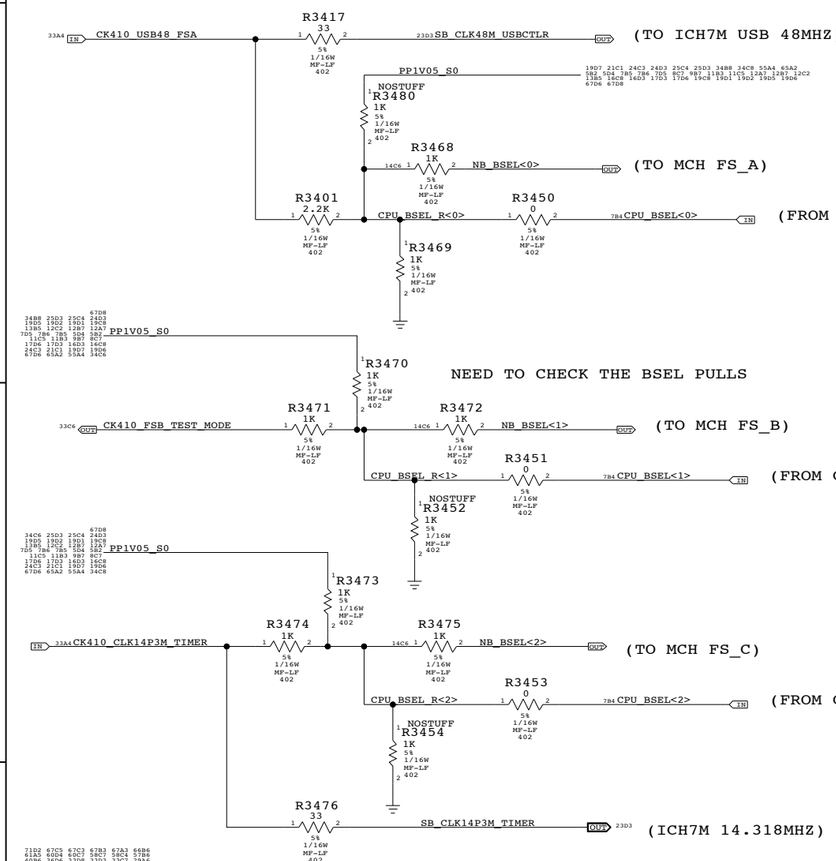
CLOCKS

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 33 OF 87	

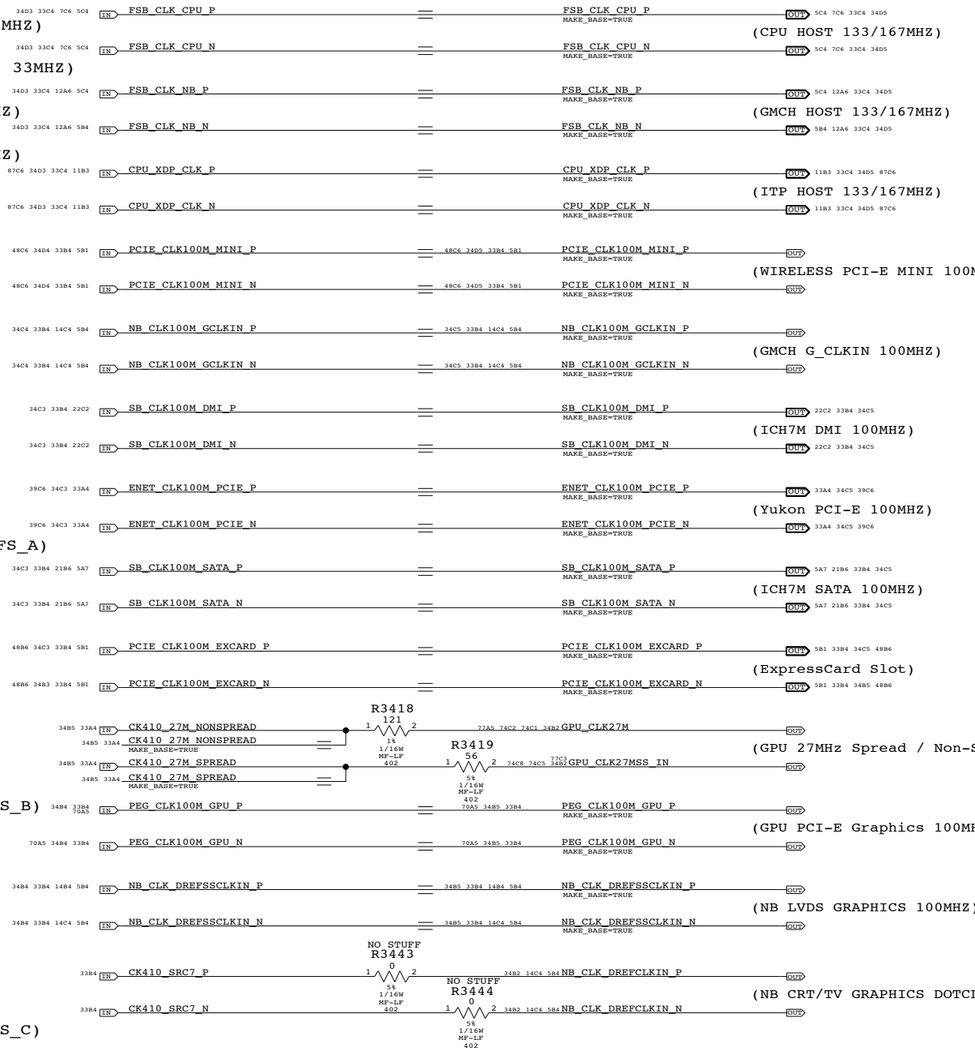




NOSTUFF R3450,R3451,R3453 FOR MANUAL CPU FREQUENCY

FS_C	FS_B	FS_A	CPU
0	0	0	266M
# 0	0	1	133M
# 0	1	0	166M
0	1	1	200M
1	0	0	100M
1	0	1	333M
1	1	0	400M
1	1	1	RESERVED

NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED



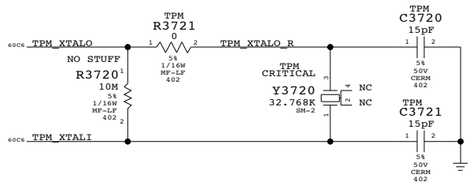
Clock Termination

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

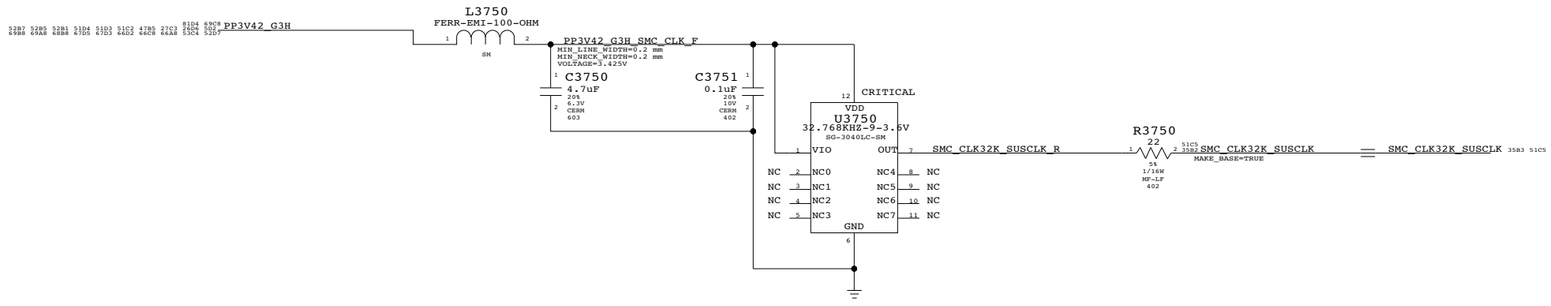
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 34 OF 87	

TPM Crystal Circuit



SMC G3Hot Oscillator



Mobile Clocking

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 35 OF 87	

IDE (ODD) Connector

71D2 67C5 67C3 67B3 67A3 66B6 66B5 66B1 65D6
54D4 54B5 52D3 49C7 49C4 49B5 49B6 34A8 33D8
26B8 26B6 26B4 25D8 25D3 25C6 25C4 25B8 25B4
20B4 20A4 19C7 19C5 17C6 14D6 14C7 10C5 5D4 5A4
23A4 24D3 24C3 24B5 24B3 23D5 23B3 22B5 21D3 21C3
33D3 33B3 32B5 32A6 31A5 31A3 30D4 30C7 30C5 29C4
82D5 82C6 82B3 82A4 79D3 79A8

71D7 58C7 58C4 57B5 55A8 53C4 31C5 25D8 5D4 5D2
81B3 80B5 80A1 79B8 71A6 67B3 67B1 67A1 66B5 62B1

PP3V3_S0

CRITICAL
Q3820
FDZ293P
8SOA

PP5V_S0

PP5V_S0_IDE_ODD
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=5V

R3820 10K 5% 1/16W MF-LF 402

C3821 0.22uF 20% 6.3V X5R 402

ODD_PWR_EN_L_RC

R3821 10K 5% 1/16W MF-LF 402

22A6 IN ODD_PWR_EN_L

NO STUFF
R3801 4.7K 5% 1/16W MF-LF 402

R3802 4.7K 5% 1/16W MF-LF 402

R3810 33K 5% 1/16W MF-LF 402

CRITICAL
J3800
M-ST-SM1-LF

23C3 IN	IDE_RESET_L	1	50		
		2	49	21B5 IO	IDE_PDD<8>
21B5 IO	IDE_PDD<7>	3	48	21B5 IO	IDE_PDD<9>
21B5 IO	IDE_PDD<6>	4	47	21B5 IO	IDE_PDD<10>
21B5 IO	IDE_PDD<5>	5	46	21B5 IO	IDE_PDD<11>
21B5 IO	IDE_PDD<4>	6	45		
		7	44	21B5 IO	IDE_PDD<12>
21B5 IO	IDE_PDD<3>	8	43	21B5 IO	IDE_PDD<13>
21B5 IO	IDE_PDD<2>	9	42	21B5 IO	IDE_PDD<14>
21B5 IO	IDE_PDD<1>	10	41	21B5 IO	IDE_PDD<15>
21C5 IO	IDE_PDD<0>	11	40		
		12	39	21B6 IN	IDE_PDIOW_L (UATA_STOP)
21B6 OUTP	IDE_PDDREQ	13	38	21B6 IN	IDE_PDDACK_L
21B6 IN	IDE_PDIOR_L (UATA_HSTROBE)	14	37	21B6 OUTP	IDE_IRQ14
21B6 OUTP	IDE_PDIORDY (UATA_DSTROBE)	15	36	21B5 IN	IDE_PDA<1>
		16	35		
21B5 IN	IDE_PDA<2>	17	34	21B5 IN	IDE_PDA<0>
21B5 IN	IDE_PDCS1_L (UATA_CS0*)	18	33	21B5 IN	IDE_PDCS3_L (UATA_CS1*)
		19	32		
		20	31		
		21	30		
NC		22	29	51B7 OUTP	Indicates disk presence SMC_ODD_DETECT
		23	28		
		24	27		
		25	26		

516S0335

R3811 15K 5% 1/16W MF-LF 402

R3803 6.2K 5% 1/16W MF-LF 402

Counters 10K pull-up to 5V in
ODD to keep SB GPIO <= 3.3V

23D2 SATA_C_DET_L

R3850 100 1% 1/16W MF-LF 402

36A4 21B6	TP_SATA_A_R2DP	TP_SATA_A_R2DP	21B6 36A5
36A4 21B6	TP_SATA_A_R2DN	TP_SATA_A_R2DN	21B6 36A5
36A4 21B6	TP_SATA_A_D2RP	TP_SATA_A_D2RP	21B6 36A5
36A4 21B6	TP_SATA_A_D2RN	TP_SATA_A_D2RN	21B6 36A5

MAKE_BASE=TRUE

36A5 36A4 21B6 SATA_RBIAS — 36A5 SATA_RBIAS (MAKE_BASE=TRUE)

R3860 24.9 1% 1/16W MF-LF 402

Placement note
Place within 12.7mm
from ball of SB

PATA Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

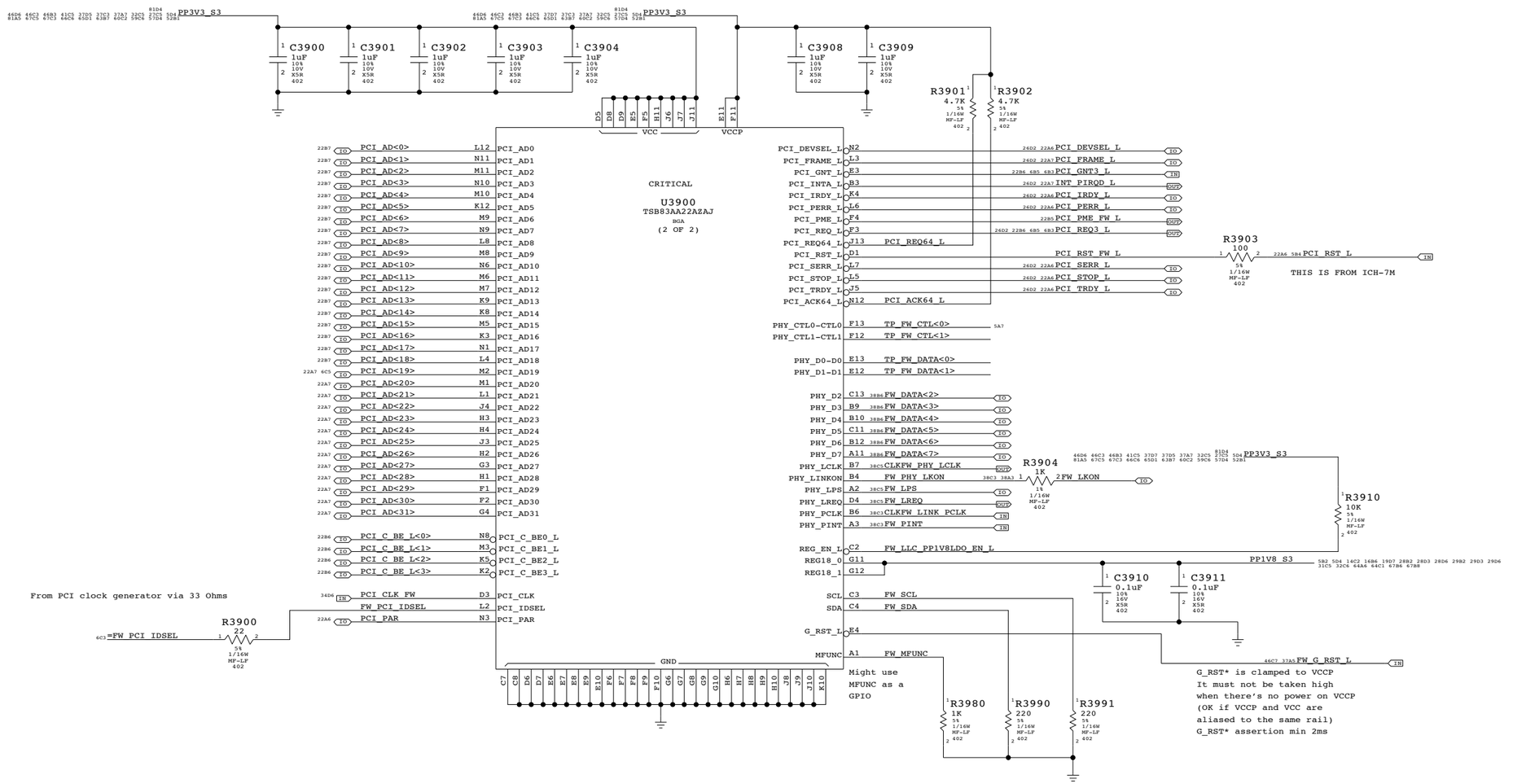
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	36	87



FireWire Link (TSB83AA22)

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

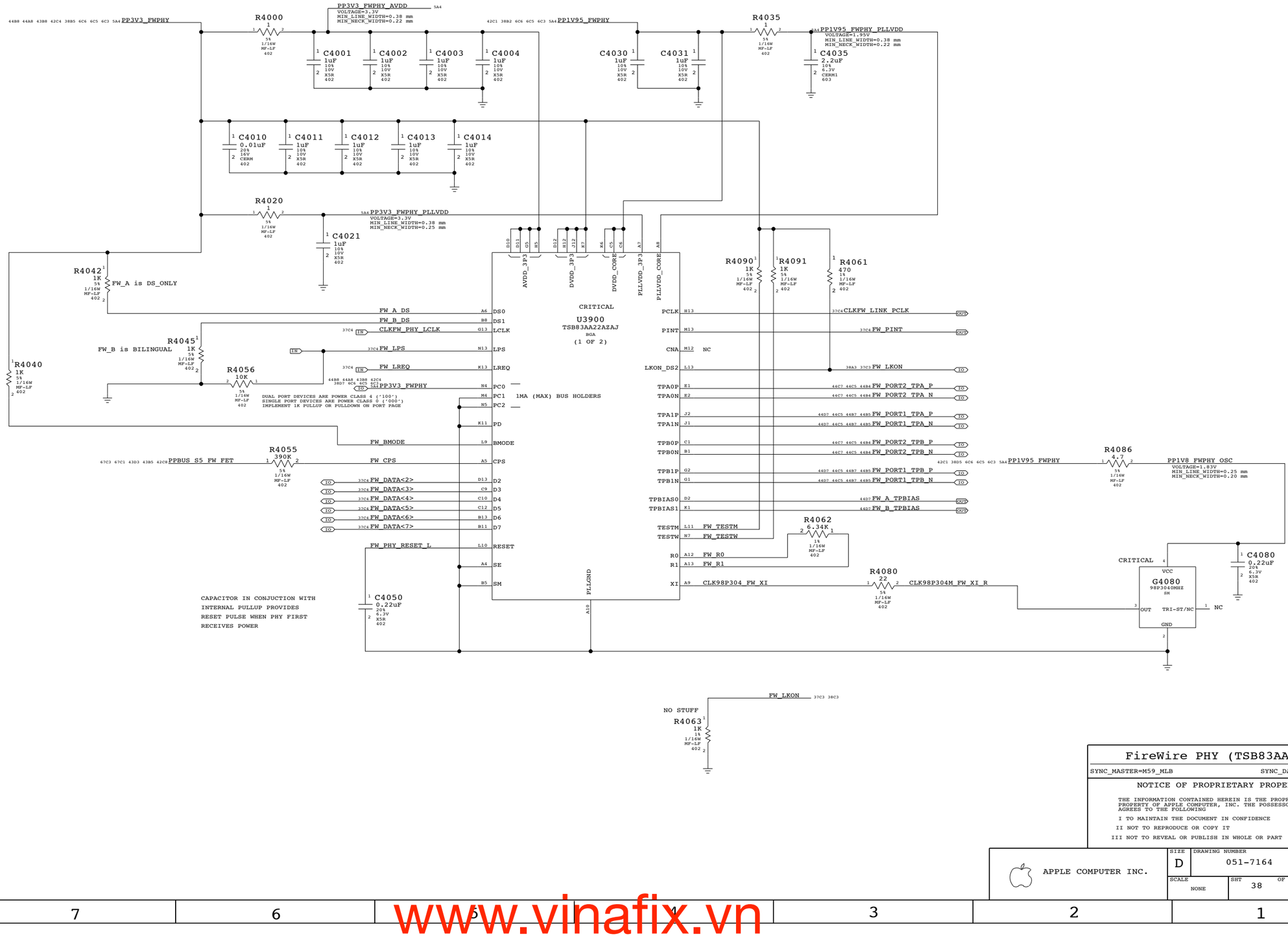
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	37	87



FireWire PHY (TSB83AA22)

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE: NONE SHT 38 OF 87

PLACE C4100-C4106 NEAR PINS AVDLL0-AVDLL6.
SCHEME MATCHES DOC MVL100258-01

MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.22MM
VOLTAGE=2.5V

PP2V5_S3_ENET_AVDD

C4100 1UF 10% 6.3V CERM 402
C4101 0.1UF 10% 16V X5R 402
C4102 0.1UF 10% 16V X5R 402
C4103 0.1UF 10% 16V X5R 402
C4104 0.1UF 10% 16V X5R 402
C4105 0.001UF 10% 50V CERM 402
C4106 0.001UF 10% 50V CERM 402
C4107 0.1UF 10% 16V X5R 402

L4100 FERR-120-OHM-1.5A 0402-LF

PP2V5_S3

PLACE C4107 NEAR U4101 AVDD

PP3V3_S3AC
PP1V2_S3
PP3V3_S3AC

PLACE C4110 AND C4111 WITHIN
12 MIL OF U4101 PIN 49 AND 50

C4110 0.1UF 10% 16V X5R 402
C4111 0.1UF 10% 16V X5R 402
C4112 0.1UF X5R 10% 16V 402
C4113 0.1UF 402 X5R 16V 10%

PLACE C4113 AND C4112 WITHIN
12 MIL OF U2100 E27 AND E28

PCIE_A_D2R_C_P
PCIE_A_D2R_C_N
PCIE_A_D2R_P
PCIE_A_D2R_N
PCIE_A_R2D_P
PCIE_A_R2D_N
PCIE_A_R2D_C_P
PCIE_A_R2D_C_N

OMIT
CRITICAL
U4101
88E8053
QFN

ENET_LOM_DIS_L
PM_SLP_S3_L

LOM_DISABLE*
VAUX_AVLBL
VMAIN_AVLBL
SWITCH_VCC
SWITCH_VAUX
HSDACP
HSDACN
CTRL25
CTRL12
RSET
LED_ACT*
LED_LINK10/100*
LED_LINK1000*
LINK*
TSTPT
TESTMODE
TX_P
TX_N
RX_P
RX_N
REFCLKP
REFCLKN
WAKE*
PERST*
MDIP0
MDIN0
MDIP1
MDIN1
MDIP2
MDIN2
MDIP3
MDIN3
VPD_CLK
VPD_DATA
PU_VDDO_TTL0
PU_VDDO_TTL1
SPI_DI
SPI_DO
SPI_CLK
SPI_CS
XTALI
XTALO
THRML_PAD

ANALOG
OPTIONAL EXTERNAL LDO
NC_ENET_CTRL25
NC_ENET_CTRL12
ENET_RSET
R4102 4.87K 1% 1/16W MF-LF 402
NO PULL-UP NEEDED
LED
TEST
PCI EXPRESS
MEDIA
TWSI
TEST
SPI
MAIN CLK

ENET_CLK100M_PCIE_P
ENET_CLK100M_PCIE_N
PCIE_WAKE_L
ENET_RST_L
ENET_VPD_CLK
ENET_VPD_DATA
ENET_PU_VDD_TTL0
ENET_PU_VDD_TTL1

ASF IS UNAVAILABLE ON 8053
INTERNAL PULL-UP

CRITICAL
ENET_XTALI
ENET_XTALO
Y4101 SM-3.2X2.5MM 25.0000M
C4150 27pF 5% 50V CERM 402
C4151 27pF 5% 50V CERM 402

1. KEEP ENET_XTALI AND ENET_XTALO
TRACE LENGTH <12MIL.
2. DO NOT ROUTE UNDER CRYSTAL

ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<2>
ENET_MDI_N<2>
ENET_MDI_P<3>
ENET_MDI_N<3>

R4106 49.9 1% 1/16W MF-LF 402
R4105 49.9 1% 1/16W MF-LF 402
R4104 49.9 1% 1/16W MF-LF 402
R4103 49.9 1% 1/16W MF-LF 402
R4120 49.9 1% 1/16W MF-LF 402
R4119 49.9 1% 1/16W MF-LF 402
R4118 49.9 1% 1/16W MF-LF 402
R4117 49.9 1% 1/16W MF-LF 402

ENET_MDI0 VOLTAGE=1.234V
ENET_MDI1 VOLTAGE=1.234V
ENET_MDI2 VOLTAGE=1.234V
ENET_MDI3 VOLTAGE=1.234V

C4116 0.001UF 10% 50V CERM 402
C4115 0.001UF 10% 50V CERM 402
C4117 0.001UF 10% 50V CERM 402
C4118 0.001UF 10% 50V CERM 402

Setting attribute VOLTAGE
to arbitrary value
to help constraint manager
find correct topology

PLACE RESISTORS CLOSE TO U4101

R4101 4.7K 5% 1/16W MF-LF 402
ENET_LOM_DIS_L
Q4100 2N7002 SOT23-LF
ENET_LOWPWR_EN
R4132 100K 5% 1/16W MF-LF 402

R4130 4.7K 5% 1/16W MF-LF 402
R4131 4.7K 5% 1/16W MF-LF 402

PLACE C4140 NEAR U4102 VCC
C4140 0.1UF 10% 16V X5R 402

OMIT
CRITICAL
U4102
M24C08
SO8
VCC
E2
NC1
NC0
WC*
SDA
SCL
VSS

R4122 10K 5% 1/16W MF-LF 402
R4123 10K 5% 1/16W MF-LF 402

PLACE C4127-C4134 NEAR PINS VDD0-VDD7 ON U4101
SCHEME MATCHES DOC MVL100258-01

C4126 0.1UF 10% 16V X5R 402
C4127 0.1UF 10% 16V X5R 402
C4128 0.1UF 10% 16V X5R 402
C4129 0.1UF 10% 16V X5R 402
C4130 0.1UF 10% 16V X5R 402
C4131 0.001UF 10% 50V CERM 402
C4132 0.001UF 10% 50V CERM 402
C4133 0.001UF 10% 50V CERM 402
C4134 0.001UF 10% 50V CERM 402

PLACE C4135-C4139 NEAR VDDO_TTL0-VDD_TTL4 ON U4101
SCHEME MATCHES DOC MVL100258-01

C4135 0.1UF 10% 16V X5R 402
C4136 0.1UF 10% 16V X5R 402
C4137 0.1UF 10% 16V X5R 402
C4138 0.001UF 10% 50V CERM 402
C4139 0.001UF 10% 50V CERM 402

ETHERNET CONTROLLER

SYNC_MASTER=M59_MLB
SYNC_DATE=08/08/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 39 OF 87	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED	ENETCONN	ENET_100D	ENETCONN_P<0> 40D3
	ENETCONN	ENET_100D	ENETCONN_N<0> 40C3
BY	ENETCONN	ENET_100D	ENETCONN_P<1> 40C3
	ENETCONN	ENET_100D	ENETCONN_N<1> 40C3
ETHERNET	ENETCONN	ENET_100D	ENETCONN_P<2> 40C3
	ENETCONN	ENET_100D	ENETCONN_N<2> 40C3
PHY	ENETCONN	ENET_100D	ENETCONN_P<3> 40C3
	ENETCONN	ENET_100D	ENETCONN_N<3> 40B3

Page Notes

Power aliases required by this page:
- =PP2V5_ENET
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

39D5 5A4 PP2V5_S3_ENET_AVDD

Place one cap at each pin of transformer

C4200 1uF 10% 6.3V CERM 402
C4201 1uF 10% 6.3V CERM 402
C4202 1uF 10% 6.3V CERM 402
C4203 1uF 10% 6.3V CERM 402

Transformers should be mirrored on opposite sides of the board

1000BT-824-00275 CRITICAL
T4200 XFR-SM
SYM_VER2

39C3 IO ENET_MDI_P<0> 1
40B7 39C3 IO ENET_MDI_N<0> 2
39C3 IO ENET_MDI_P<1> 7
40A7 39C3 IO ENET_MDI_N<1> 8
3 ENET_CTAP0
6 ENET_CTAP1
4 NC1 CHAS SIDE
5 NC2
13 NC4 LINE SIDE
12 NC3
16 40D7 ENETCONN_P<0>
15 40D7 ENETCONN_N<0>
10 40D7 ENETCONN_P<1>
9 40D7 ENETCONN_N<1>

1000BT-824-00275 CRITICAL
T4201 XFR-SM
SYM_VER2

39C3 IO ENET_MDI_P<2> 1
39C3 IO ENET_MDI_N<2> 2
39C3 IO ENET_MDI_P<3> 7
39C3 IO ENET_MDI_N<3> 8
3 ENET_CTAP2
6 ENET_CTAP3
4 NC1 CHAS SIDE
5 NC2
13 NC4 LINE SIDE
12 NC3
16 40D7 ENETCONN_P<2>
15 40D7 ENETCONN_N<2>
10 40D7 ENETCONN_P<3>
9 40D7 ENETCONN_N<3>

CRITICAL
J4200
JM36113-P2054-7F
F-RT2-TH-RJ45

514-0277
Short shielded RJ-45

NO STUFF
R4210 0 5% 1/16W MF-LF 402
Place close to connector

R4200 75 5% 1/16W MF-LF 402
R4201 75 5% 1/16W MF-LF 402
R4202 75 5% 1/16W MF-LF 402
R4203 75 5% 1/16W MF-LF 402

ENET_CTAP_COMMON
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

C4204 100pF 10% 16V CERM 1808
GND_CHASSIS_ENET

LAN ENERGY DETECT

PP3V3_S0

C4220 68PF 5% 50V CERM 402-1
40C4 39C3 ENET_MDI_N<0>
ED_MDIN0_C VOLTAGE=1.234V
R4220 2.4K 5% 1/16W MF-LF 402

C4221 68PF 5% 50V CERM 402-1
40C4 39C3 ENET_MDI_N<1>
ED_MDIN1_C VOLTAGE=1.234V
R4221 2.4K 5% 1/16W MF-LF 402

Setting attribute VOLTAGE to arbitrary value to help constraint manager find correct topolgy

PLACE C4220 & C4221
NEAR ENET_MDI_N<0/1>

R4227 470K 1% 1/16W MF-LF 402
R4223 3.3K 5% 1/16W MF-LF 402
R4228 392K 1% 1/16W MF-LF 402
R4224 100K 1% 1/16W MF-LF 402
C4223 0.1uF 10% 10V X5R 402

EDET_MDIN_AMP
ED_MDIN_R
Q4220 MMDT3904XF SOT-363-LF
Q4220 MMDT3904XF SOT-363-LF

NO STUFF
C4222 100pF 5% 50V CERM 402
R4225 51.1K 1% 1/16W MF-LF 402

EDET_ACT
EDET_REF
U4200 LMC7211 SM-LF
LAN_ENERGY_DET 23C3
R4226 10K 5% 1/16W MF-LF 402

Ethernet Connector		
SYNC_MASTER=M59_MLB		SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

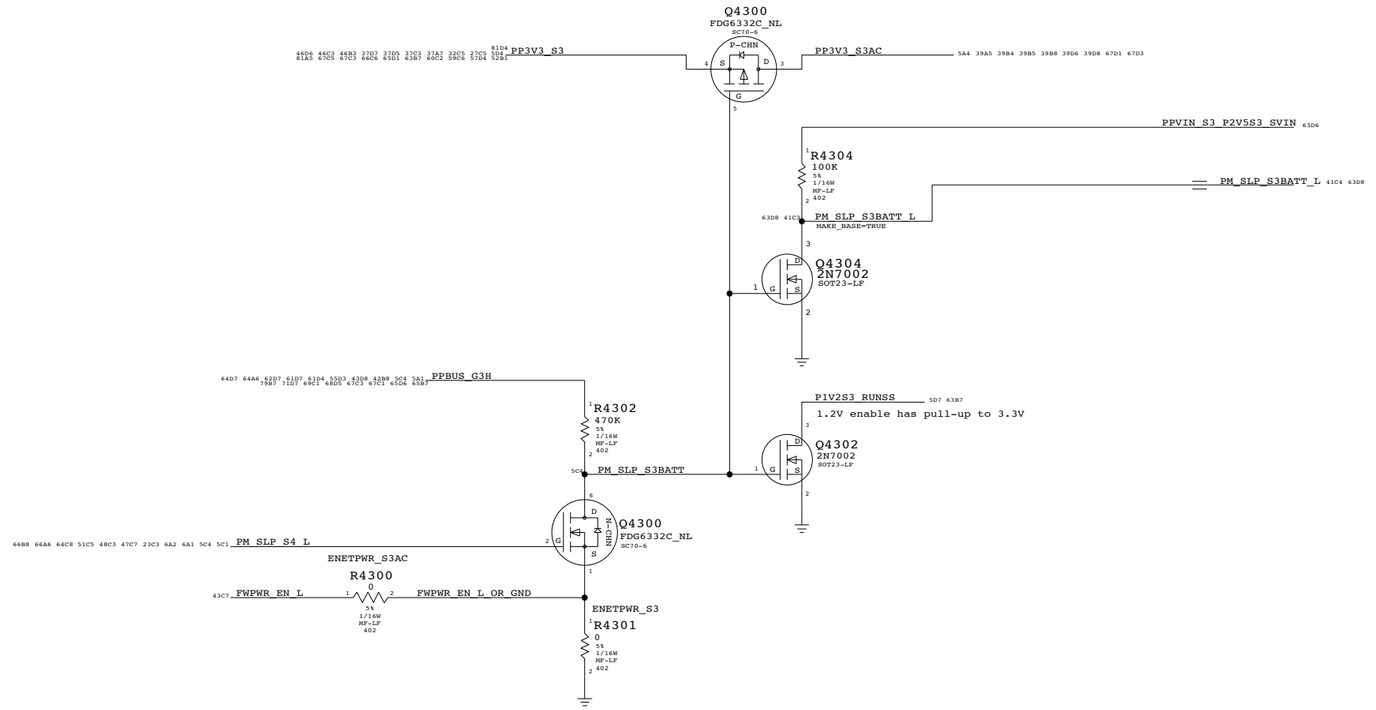
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7164	03001
	SCALE NONE	SHT 40 OF 87	

Yukon Power Control

Allows powering Yukon down during battery sleep to save power



When ENETPWR_S3AC BOMOPTION is active:

State	FWPWR_EN_L	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN	P1V2S3_RUNSS
S0 AC	0V	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S0 Batt	0V	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S3 AC	0V	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S3 Batt	PBUS	3.3V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
S5 AC	0V	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
S5 Batt	PBUS	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
G3H Batt	PBUS	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)

When ENETPWR_S3 BOMOPTION is active:

State	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN	P1V2S3_RUNSS
S0	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S3	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S5	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
G3H	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)

Yukon Power Control

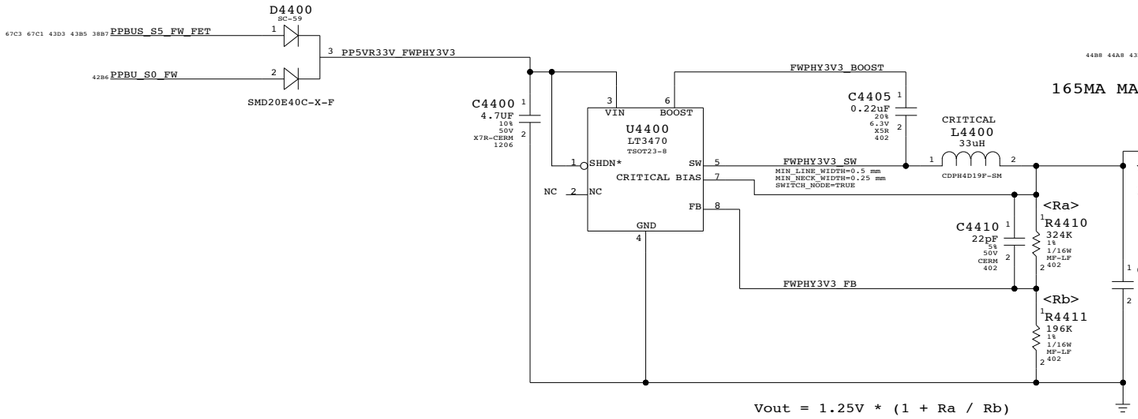
SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

APPLE COMPUTER INC.

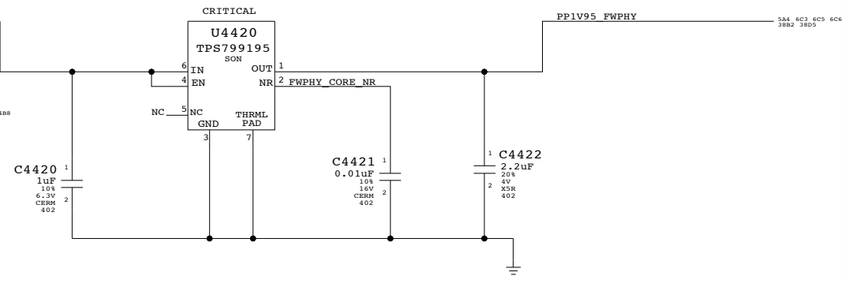
SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE: NONE SHT: 41 OF: 87

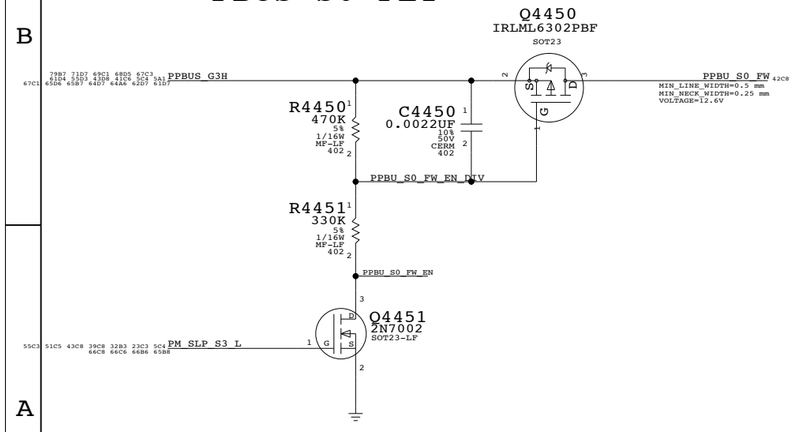
3.3V Supply for FWPHY



1.95V Supply for FW PHY



PBUS S0 FET



FW PHY Power Supply

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	42	87

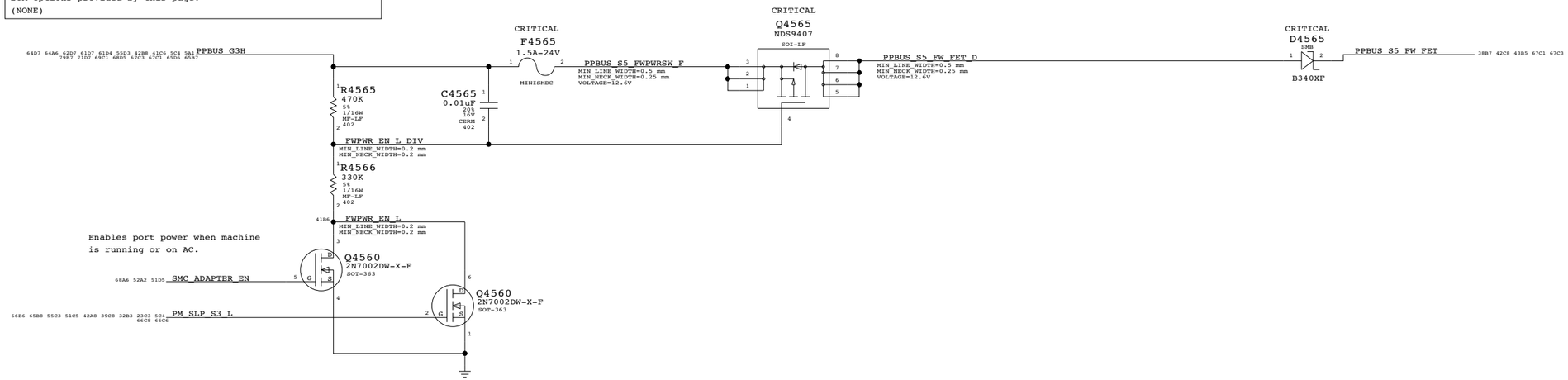
Page Notes

Power aliases required by this page:
- =PPBUS_S0_FWPWRSW (system supply for bus power)
- =PP3V3_S0_FWPORTPWRSW

Signal aliases required by this page:
- =FWPWR_PWRON (see related text note below)

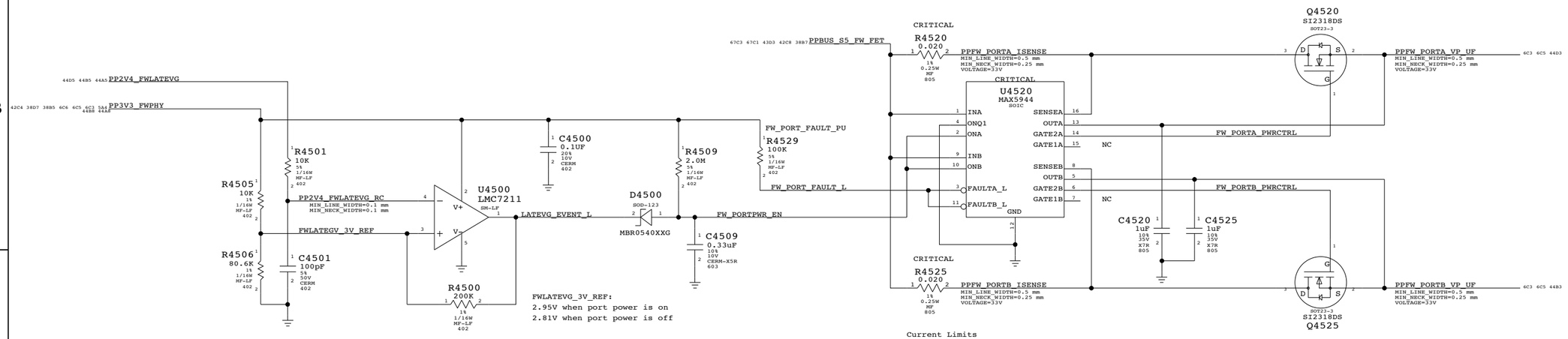
BOM options provided by this page:
(NONE)

Port Power Switch



Current Limit/Active Late-VG Protection

Late-VG Event Detection



Current Limits

0.020 ohm => 2.4A
0.025 ohm => 2A
0.030 ohm => 1.66A (Ideal)
0.033 ohm => 1.5A

MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

FireWire Port Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	43	87

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL
PROVIDED	FW	FW_110ΩD
BY	FW	FW_110ΩD
PHY	FW	FW_110ΩD
PAGE	FW	FW_110ΩD

FW_PORT1_TPA_P 38B3 44B5 44B7 44C5
FW_PORT1_TPA_N 38B3 44B5 44B7 44C5
FW_PORT1_TPB_P 38B3 44B5 44B7 44C5
FW_PORT1_TPB_N 38B3 44B5 44B7 44C5
FW_PORT2_TPA_FL_P 44B2
FW_PORT2_TPA_FL_N 44B2
FW_PORT2_TPB_FL_P 44B2
FW_PORT2_TPB_FL_N 44B2

Page Notes

Power aliases required by this page:
- =PPFW_PORT1
- =PP3V3_S5_FWLATEVG
- =GND_CHASSIS_FW_PORT1

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

Termination

Place close to FireWire PHY

38B3 FW_B_TPBIAS
38B3 FW_A_TPBIAS

TI PHYs require 1uF even though FW spec calls out 0.33uF

C4650 1uF 10% 6.3V CERM 402
C4660 1uF 10% 6.3V CERM 402

Setting attribute VOLTAGE to arbitrary value to help constraint manager find correct topology

VOLTAGE=1.234V

OMIT L4660 0 5% 1/16W MF-LF 402
OMIT L4661 0 5% 1/16W MF-LF 402

FW_B_TPA_L_P VOLTAGE=1.234V
FW_B_TPA_L_N VOLTAGE=1.234V

R4650 56.2 1% 1/16W MF-LF 402
R4651 56.2 1% 1/16W MF-LF 402
R4660 56.2 1% 1/16W MF-LF 402
R4661 56.2 1% 1/16W MF-LF 402

44C5 44B4 38B3 FW_PORT2_TPA_P — FW_PORT2_TPA_P MAKE_BASE=TRUE 38B3 44B4 44C7
44C5 44B4 38B3 FW_PORT2_TPA_N — FW_PORT2_TPA_N MAKE_BASE=TRUE 38B3 44B4 44C7
44C5 44B4 38B3 FW_PORT2_TPB_P — FW_PORT2_TPB_P MAKE_BASE=TRUE 38B3 44B4 44C7
44C5 44B4 38B3 FW_PORT2_TPB_N — FW_PORT2_TPB_N MAKE_BASE=TRUE 38B3 44B4 44C7
44D7 44C5 44B5 38B3 FW_PORT1_TPA_P — FW_PORT1_TPA_P MAKE_BASE=TRUE 38B3 44B7 44C5 44D7
44D7 44C5 44B5 38B3 FW_PORT1_TPA_N — FW_PORT1_TPA_N MAKE_BASE=TRUE 38B3 44B7 44C5 44D7
44D7 44C5 44B5 38B3 FW_PORT1_TPB_P — FW_PORT1_TPB_P MAKE_BASE=TRUE 38B3 44B7 44C5 44D7
44D7 44C5 44B5 38B3 FW_PORT1_TPB_N — FW_PORT1_TPB_N MAKE_BASE=TRUE 38B3 44B7 44C5 44D7 43B8 44D5 44A3

44B8 44A8 43B8 42C4 38D7 38B5 6C6 6C5 6C3 5A4 PP3V3_FWPHY
38D7 38B5 6C6 6C5 6C3 5A4 PP3V3_FWPHY — PP3V3_FWPHY 44B8 44A8 43B8 42C4

R4652 56.2 1% 1/16W MF-LF 402
R4653 56.2 1% 1/16W MF-LF 402
R4662 56.2 1% 1/16W MF-LF 402
R4663 56.2 1% 1/16W MF-LF 402

FW_B_TPB_L_N VOLTAGE=1.234V
FW_B_TPB_L_P VOLTAGE=1.234V

OMIT L4662 0 5% 1/16W MF-LF 402
OMIT L4663 0 5% 1/16W MF-LF 402

FW_PORT2_TPB_C VOLTAGE=1.234V
FW_PORT1_TPB_C VOLTAGE=1.234V

C4654 220pF 5% 25V CERM 402
R4654 4.99K 1% 1/16W MF-LF 402
C4664 220pF 5% 25V CERM 402
R4664 4.99K 1% 1/16W MF-LF 402

Note: The peaking inductors were changed to resistors to allow placement in an area restricted by DFM rules for only Rs and Cs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S0414	4	IND,18nH-15mA,0402	L4660,L4661,L4662,L4663	CRITICAL	

Late-VG Protection Power

44B8 43B8 42C4 38D7 38B5 6C6 6C5 6C3 5A4 PP3V3_FWPHY
R4690 332 1% 1/16W MF-LF 402

PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin
R4690 should be 390 Ohms max for a 3.3V rail

PP2V4_FWLATEVG MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=2.4V 43B8 44B5 44D5

C4691 0.01UF 10% 50V X7R 402
CRITICAL
D4690 MMBZ5227B SOT23

ESD and late-VG rail for snap-back diodes (Common to all ports)

Cable Power

43B2 6C5 6C3 PPFW_PORTA_VP_UF
L4620 FERR-250-OHM SM
C4624 0.001uF 20% 50V CERM 402
PPFW_PORT1_VP MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=33V

Note:Trace PPFW_PORT1_VP should handle up to 5A

"Snapback" & "Late VG" Protection

44B5 44A5 43B8 PP2V4_FWLATEVG

DP4620 BAV99DW-X-F SOT-363
C4621 0.01uF 10% 50V X7R 402
C4620 0.01uF 10% 50V X7R 402

44D7 44B7 44B5 38B3 FW_PORT1_TPB_N
44D7 44B7 44B5 38B3 FW_PORT1_TPB_P
44D7 44B7 44B5 38B3 FW_PORT1_TPA_N
44D7 44B7 44B5 38B3 FW_PORT1_TPA_P

DP4621 BAV99DW-X-F SOT-363
C4622 0.01uF 10% 50V X7R 402
C4623 0.01uF 10% 50V X7R 402

C4629 0.1uF 10% 50V X7R 603-1
Place C4629 close to pin 5 of connector
R4629 1M 5% 1/16W MF-LF 402

C4625 0.01uF 20% 50V CERM 603
NO STUFF
C4627 0.01uF 20% 16V CERM 402
C4626 0.01uF 20% 16V CERM 402

PORT 1
BILINGUAL
CRITICAL
J4620 1394B-UG31903 F-RT-SM1

(FW_PORT1_BREF)
(PPFW_PORT1_VP)
(GND_FW_PORT1_VG)
FW_PORT1_AREF

TPB- TPB<R> TPB+ VP NC VG TPA- TPA<R> TPA+ — OUTPUT / INPUT

514S0133

GND_CHASSIS_ENET 4A6 6A8 40B2 44A1

Cable Power

43A2 6C5 6C3 PPFW_PORTB_VP_UF
L4630 FERR-250-OHM SM
C4634 0.001uF 20% 50V CERM 402
PPFW_PORT2_VP MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=33V

"Snapback" & "Late VG" Protection

PP2V4_FWLATEVG

DP4630 BAV99DW-X-F SOT-363
C4630 0.01uF 10% 50V X7R 402
C4631 0.01uF 10% 50V X7R 402

44C7 44C5 38B3 FW_PORT2_TPA_P
44C7 44C5 38B3 FW_PORT2_TPA_N
44C7 44C5 38B3 FW_PORT2_TPB_P
44C7 44C5 38B3 FW_PORT2_TPB_N

FI4630 1210-420R1 90-OHM-100MA CRITICAL
FI4631 1210-420R1 90-OHM-100MA CRITICAL

DP4631 BAV99DW-X-F SOT-363
C4632 0.01uF 10% 50V X7R 402
C4633 0.01uF 10% 50V X7R 402

C4635 0.01uF 20% 50V CERM 603
C4636 0.01uF 20% 16V CERM 402

PORT 2
1394A
CRITICAL
J4630 1394A F-RT-TH-LF

44D7 FW_PORT2_TPA_FL_P
44D7 FW_PORT2_TPA_FL_N
44D7 FW_PORT2_TPB_FL_P
44D7 FW_PORT2_TPB_FL_N
(PPFW_PORT2_VP)
(GND_FW_PORT2_VG)

TPO (TPA+) TPO# (TPA-) TPI (TPB+) TPI# (TPB-) VP VGND

514-0255

GND_CHASSIS_USB 47B2 6A6 6A8 44A3
GND_CHASSIS_ENET 44C1 6A6 6A8 40B2

R4699 0 5% 1/16W MF-LF 402
GND_CHASSIS_USB 6A6 6A8 44A1 47B2

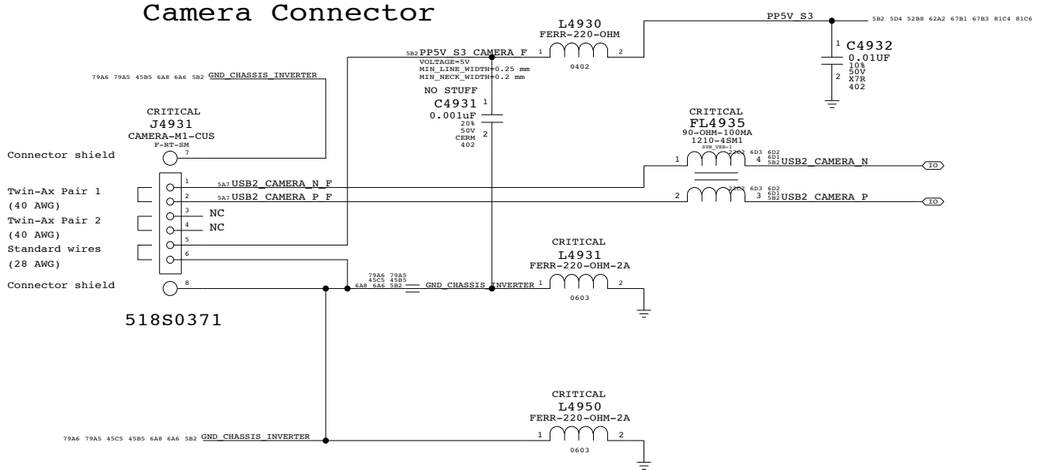
FireWire Ports

SYNC_MASTER=M59_MLB SYNC_DATE=06/27/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 44 OF 87	

Camera Connector



Camera Connector

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

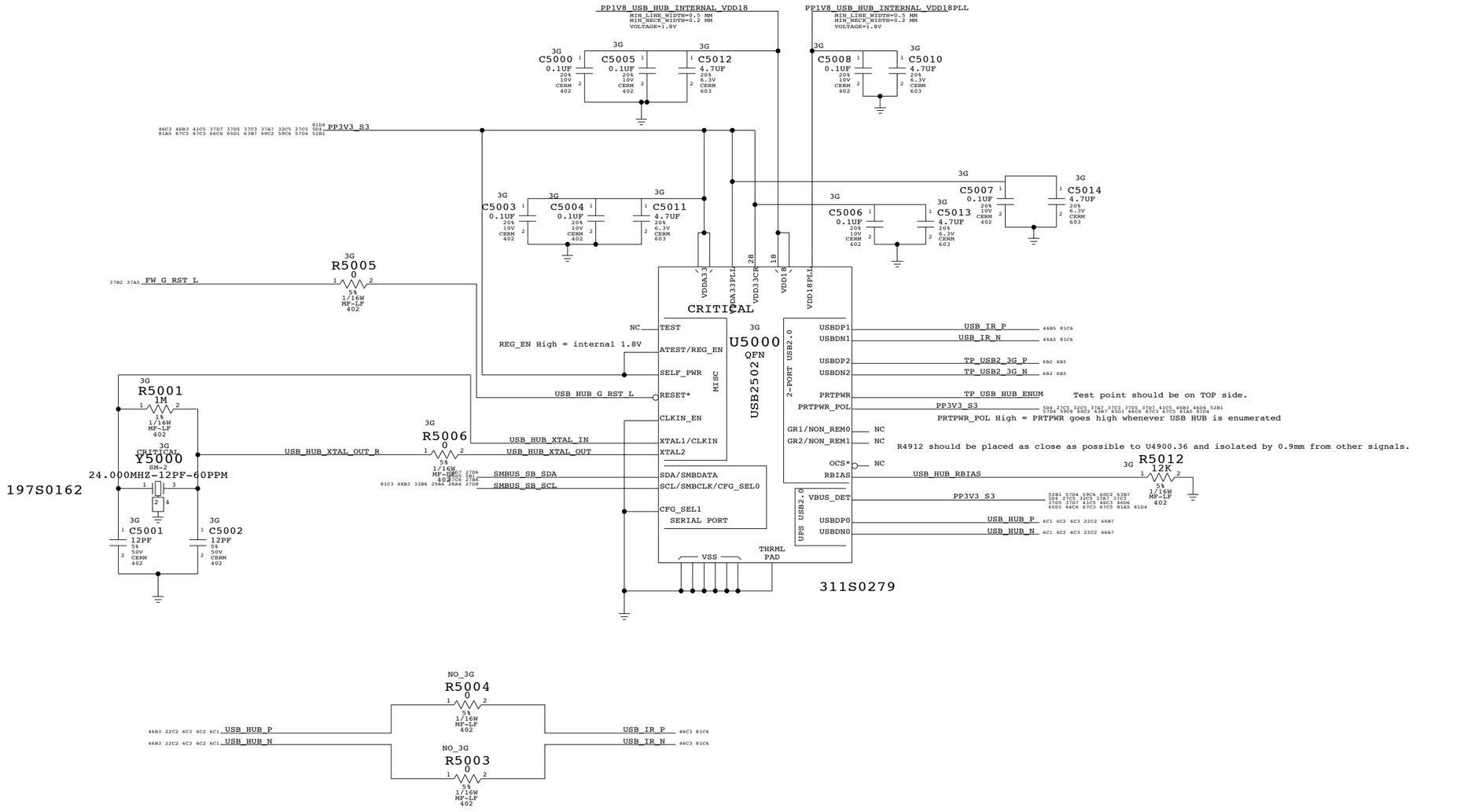
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE: NONE SHT 45 OF 87



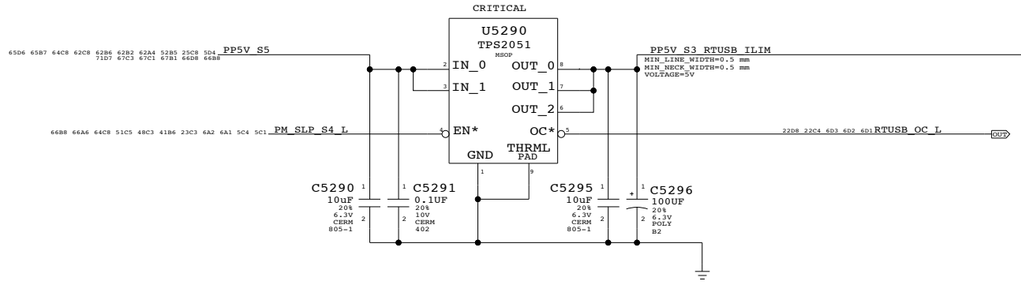
Internal USB Hub

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

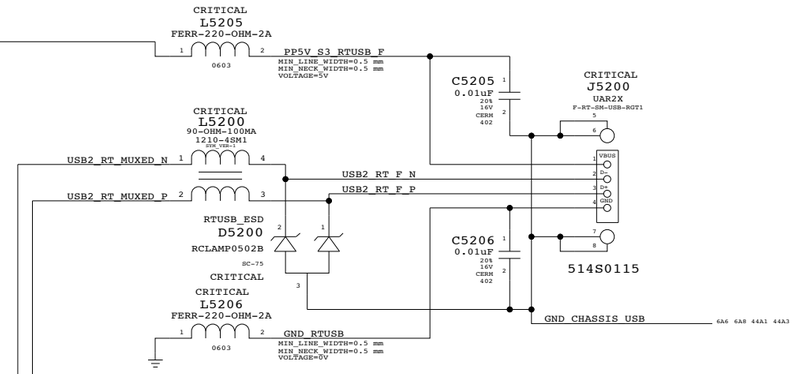
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 46 OF 87	

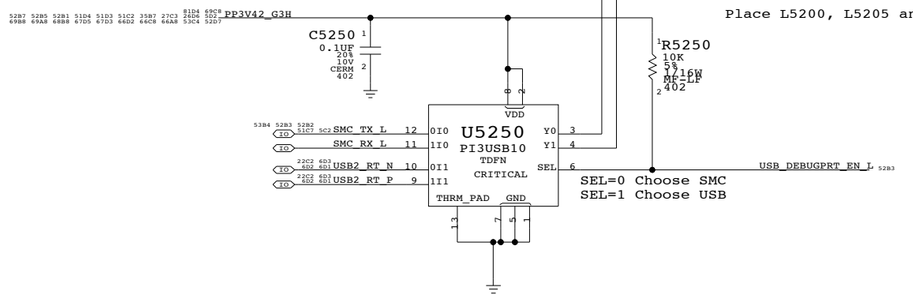
Port Power Switch



Right USB Port



USB/SMC Debug Mux



Place L5200, L5205 and L5206 across moat

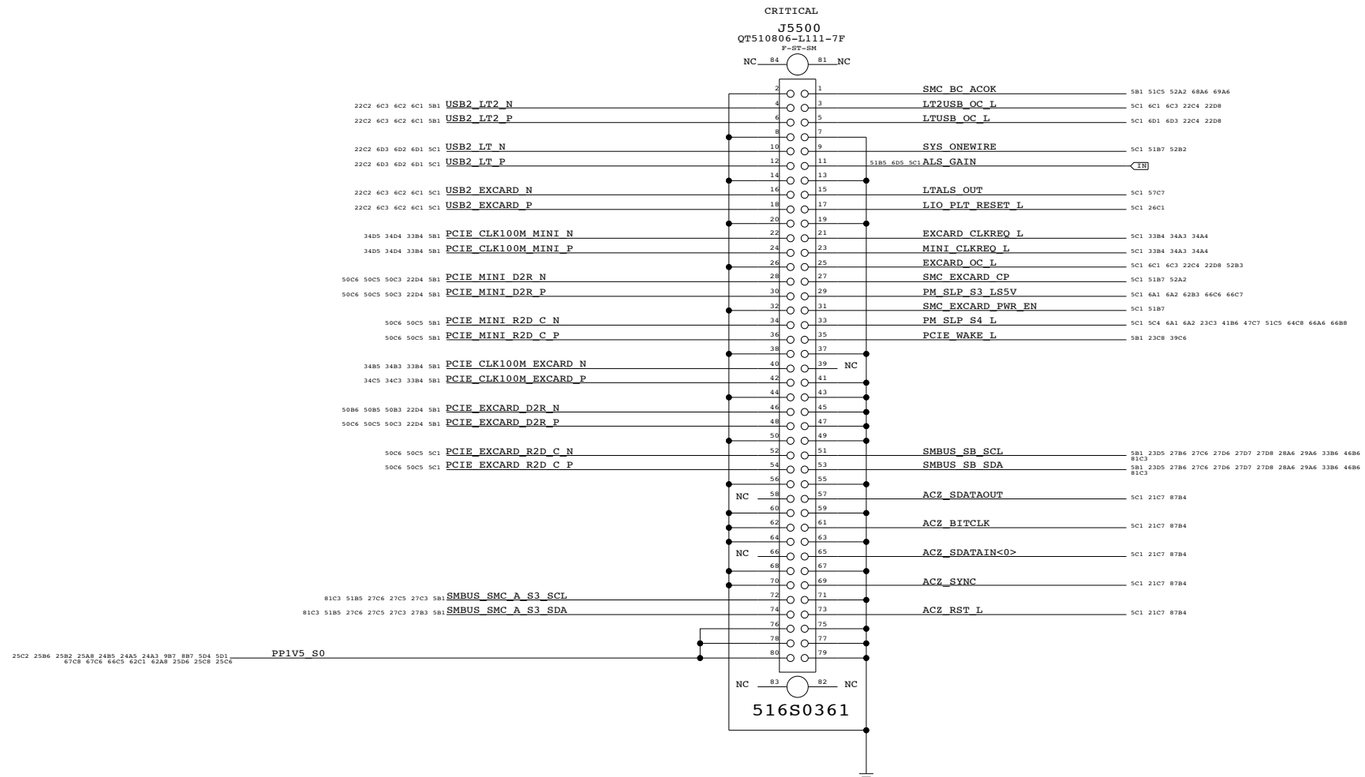
External USB Connector

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 47 OF 87	

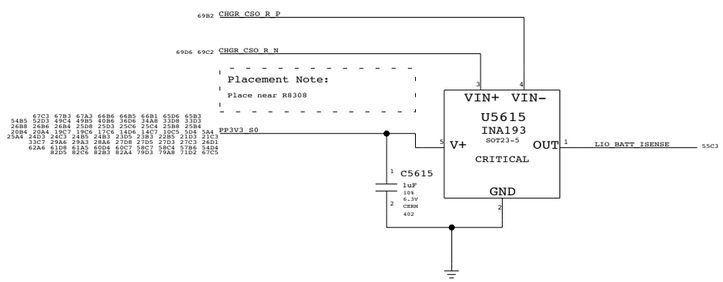
Left I/O Board Connector



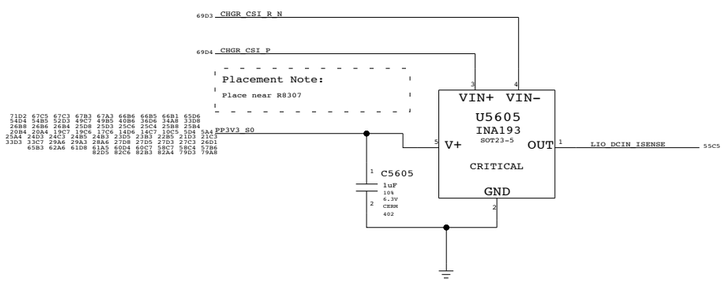
Left I/O Board Connector		
SYNC_MASTER=(MASTER)		SYNC_DATE=(MASTER)

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7164	03001
	SCALE	SHT	OF
	NONE	48	87

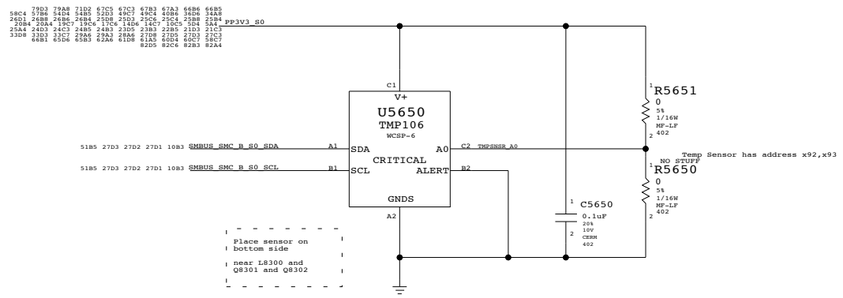
Battery Current Sense



DCIn Current Sense



TMP106 Thermal Sensor



Current & Thermal Sensors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

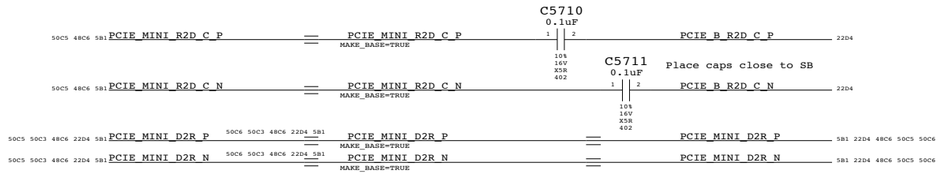
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

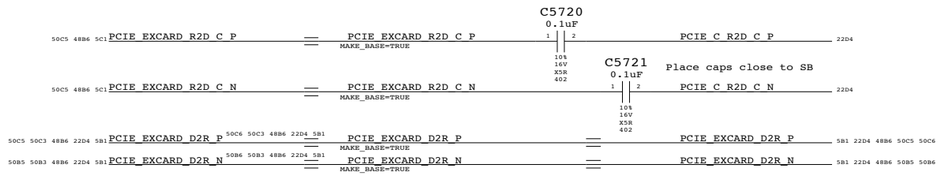
SCALE	SHT	OF
NONE	49	87

PCI-E x1 Port "A" = Ethernet (Yukon)

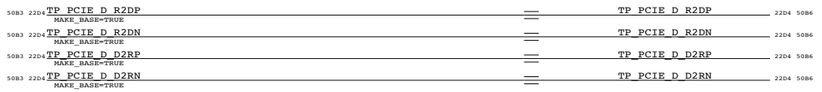
PCI-E x1 Port "B" = PCI-E Mini Card



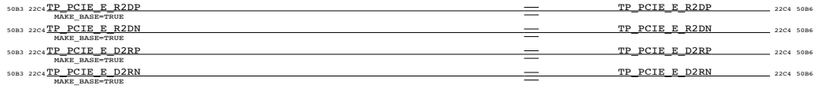
PCI-E x1 Port "C" = ExpressCard



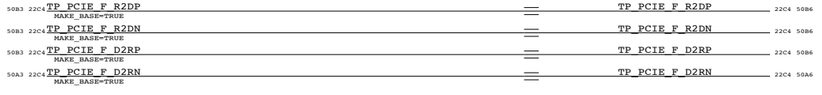
PCI-E x1 Port "D" = Unused



PCI-E x1 Port "E" = Unused



PCI-E x1 Port "F" = Unused



PCI-E Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	50	87

UNUSED PINS HAVE THE FORMAT
SMC_XXX_WHERE_XXX_IS_THE_PORT_NUMBER.
THEY ARE SET BY SOFTWARE TO BE
DRIVEN OUTPUTS ALWAYS SO THEY
CAN BE LEFT NO-CONNECTED.

OMIT
U5800
SMC_H8S2116
BGA
(1 OF 4)

PM_LAN_ENABLE	B12	P10	
SMC_RSTGATE_L	C13	P11	
ALL_SYS_PWRGD	A15	P12	
RSMRST_PWRGD	B14	P13	
SMC_SB_NMI	B15	P14	
PM_RSMRST_L	C14	P15	
IMVP_VR_ON	D12	P16	
PM_PWRBTN_L	C15	P17	
TP_SMC_P20	D13	P20	
TP_SMC_P21	D14	P21	
TP_SMC_P22	D15	P22	
TP_SMC_P23	E12	P23	
SMC_BATT_TRICKLE_EN_L	E14	P24	
SMC_BATT_CHG_EN	E15	P25	
TP_SMC_P26	E13	P26	
TP_SMC_P27	F14	P27	
LPC_AD<0>	D9	P30/LAD0	
LPC_AD<1>	C9	P31/LAD1	
LPC_AD<2>	A9	P32/LAD2	
LPC_AD<3>	B9	P33/LAD3	
LPC_FRAME_L	D8	P34/LFRAME*	
SMC_LRESET_L	C8	P35/LRESET*	
PCI_CLK_SMC	A8	P36/LCLK	
INT_SERIRQ	D7	P37/SERIRQ	
TP_SMC_XDP_TMS	A5	P40/TMI0	
SMC_SYS_LED_16B	B5	P41/TMO0	
SMBUS_SMC_BSB_SDA	D5	P42/SDA1	
SMC_TPM_PP	C3	P43/TMI1/EXSCK1	
TP_SMC_XDP_TRST_L	B1	P44/TMO1	
TP_SMC_XDP_TCK	C2	P45	
TP_SMC_SYS_LED	D3	P46/PWX0/PWM0	
SMC_SYS_KBDLED	C1	P47/PWX1/PWM1	
SMC_TX_L	G1	P50	
SMC_RX_L	G4	P51	
SMBUS_SMC_0_S0_SCL	F2	P52/SCL0	

P60/KIN0*	L13		SMC_PM_G2_EN
P61/KIN1*	L14		SMC_ADAPTER_EN
P62/KIN2*	L15		SPI_ARB
P63/KIN3*	K12		SPI_SCLK
P64/KIN4*	K13		SPI_SI
P65/KIN5*	K14		SPI_SO
P66/IRQ6*/KIN6*	J12		SMC_PROCHOT_3_3_L
P67/IRQ7*/KIN7*	J13		FWH_INIT_L
P70/AN0	N12		SMC_CPU_ISENSE
P71/AN1	R13		SMC_CPU_VSENSE
P72/AN2	P13		SMC_GPU_ISENSE
P73/AN3	R14		SMC_GPU_VSENSE
P74/AN4	P14		SMC_DCIN_ISENSE
P75/AN5	R15		SMC_PBUS_VSENSE
P76/AN6	N13		SMC_BATT_ISENSE
P77/AN7	P15		SMC_P1V5S0_NB_ISENSE
P80/PME*	C7		SMC_WAKE_SCI_L
P81/GA20	A7		SMC_TPM_GPIO
P82/CLKRUN*	B7		PM_CLKRUN_L
P83/LPCPD*	D6		PM_SUS_STAT_L
P84/IRQ3*/TXD1	C6		SC_TX_L
P85/IRQ4*/RXD1	A6		SC_RX_L
P86/IRQ5*/SCK1/SCL1	B6		SMBUS_SMC_BSB_SCL
P90/IRQ2*	K4		SMC_ONOFF_L
P91/IRQ1*	J2		SMC_BC_ACOK
P92/IRQ0*	J1		SMC_BS_ALRT_L
P93/IRQ12*	J3		PM_SLP_S3_L
P94/IRQ13*	J4		PM_SLP_S4_L
P95/IRQ14*	H2		PM_SLP_S5_L
P96/EXCL	H1		SMC_CLK32K_SUSCLK
P97/IRQ15*/SDA0	G2		SMBUS_SMC_0_S0_SDA

OMIT
U5800
SMC_H8S2116
BGA
(2 OF 4)

SMC_RCIN_L	R3	PA0/KIN8*/PA2DC	
BOOT_LPC_SPI_L	P3	PA1/KIN9*/PA2DD	
PM_SYSRST_L	R2	PA2/KIN10*/PS2AC	
SMC_USB_DEBUG_MUX	N3	PA3/KIN11*/PS2AD	
PM_EXTTS_L	R1	PA4/KIN12*/PS2BC	
PM_THRM_L	N2	PA5/KIN13*/PS2BD	
SYS_ONEWIRE	M4	PA6/KIN14*/PS2CC	
PM_BATLOW_L	N1	PA7/KIN15*/PS2CD	
SMC_EXTSMI_L	B10	PB0/LSMI*	
SMC_RUNTIME_SCI_L	A10	PB1/LSCI	
SMC_ODD_DETECT	D10	PB2	
ISENSE_CAL_EN	A11	PB3	
SMC_EXCARD_CP	B11	PB4	
SMC_EXCARD_PWR_EN	C11	PB5	
SMC_EXCARD_OC_L	A12	PB6	
SMC_XDP_TDO_3_3	D11	PB7	
SMC_FAN_0_CTL	G14	PC0/TIOCA0/WUE8*	
SMC_FAN_1_CTL	G15	PC1/TIOCB0/WUE9*	
TP_SMC_FAN_2_CTL	G13	PC2/TIOCC0/TCLKA/WUE10*	
TP_SMC_FAN_3_CTL	G12	PC3/TIOCD0/TCLKB/WUE11*	
SMC_FAN_0_TACH	H14	PC4/TIOCA1/WUE12*	
SMC_FAN_1_TACH	H15	PC5/TIOCB1/TCLKC/WUE13*	
TP_SMC_FAN_2_TACH	H13	PC6/TIOCA2/WUE14*	
TP_SMC_FAN_3_TACH	H12	PC7/TIOCB2/TCLKD/WUE15*	
SMS_X_AXIS	M11	PD0/AN8	
SMS_Y_AXIS	P11	PD1/AN9	
SMS_Z_AXIS	R11	PD2/AN10	
TP_SMC_ANALOG_ID	N11	PD3/AN11	
SMC_P1V05S0_ISENSE	P10	PD4/AN12	
SMC_MEM_ISENSE	R10	PD5/AN13	
ALS_LEFT	N10	PD6/AN14	
ALS_RIGHT	M10	PD7/AN15	

PE0	M3		SMC_CASE_OPEN
PE1*/ETCK	M2		SMC_TCK
PE2*/ETDI	M1		SMC_TDI
PE3*/ETDO	L4		SMC_TDO
PE4*/ETMS	L2		SMC_TMS
PF0/IRQ8*/PWM2	M7		TP_SMC_PF0
PF1/IRQ9*/PWM3	P6		TP_SMC_PF1
PF2/IRQ10*/TMOY	R6		SMC_LID
PF3/IRQ11*/TMOX	N6		SMC_CPU_RESET_3_3_L
PF4/PWM4	M6		SMC_BATT_ISET
PF5/PWM5	R5		TP_SMC_BATT_VSET
PF6/PWM6	P5		SMC_SYS_ISET
PF7/PWM7	N5		TP_SMC_SYS_VSET
PG0/EXIRQ8*/TMIX	P9		SPI_CE_L
PG1/EXIRQ9*/TMIY	R9		SMC_XDP_TCK_3_3
PG2/EXIRQ10*/SDA2	N9		SMBUS_SMC_BSA_SDA
PG3/EXIRQ11*/SCL2	P8		SMBUS_SMC_BSA_SCL
PG4/EXIRQ12*/EXSDAA	R8		SMBUS_SMC_A_S3_SDA
PG5/EXIRQ13*/EXSCLA	M8		SMBUS_SMC_A_S3_SCL
PG6/EXIRQ14*/EXSDAB	P7		SMBUS_SMC_B_S0_SDA
PG7/EXIRQ15*/EXSCLB	R7		SMBUS_SMC_B_S0_SCL
PH0/EXIRQ6*	E1		SMC_PROCHOT
PH1/EXIRQ7*	F3		SMC_THRMTRIP
PH2/FWE	K2		SMC_FWE
PH3/EXEXCL	C4		ALS_GAIN
PH4	D4		SMS_INT_L
PH5	B3		SMS_ONOFF_L

OMIT
U5800
SMC_H8S2116
BGA
(4 OF 4)

G3	NC0	NC12	F15
H3	NC1	NC13	A14
K3	NC2	NC14	C12
L3	NC3	NC15	C10
N4	NC4	NC16	C5
M5	NC5	NC17	A3
N7	NC6	NC18	B8
M12	NC7	NC19	E4
M13	NC8	NC20	H4
L12	NC9	NC21	M9
K15	NC10	NC22	N8
J14	NC11		

PP3V42_G3H

C5802 22UF 20% 6.3V CERM 805
C5803 0.1UF 20% 10V CERM 402
C5804 0.1UF 20% 10V CERM 402
C5805 0.1UF 20% 10V CERM 402
C5806 0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE C5807 NEAR PIN F1

SMC_VCL
C5807 0.47UF 10% 6.3V CERM-X5R 402
VCL IS INTERNAL RAIL

LAYOUT NOTE:
PLACE R5899 AND C5820 NEAR SMC PIN N14,N15

PP3V42_G3H
R5899 4.7 5% 1/16W MF-LF 402
PP3V3_AVCC_SMC
C5820 0.1UF 20% 10V CERM 402
GND_SMC_AVSS

PP3V3_AVREF_SMC
PP3V42_G3H

OMIT
U5800
SMC_H8S2116
BGA
(3 OF 4)

SMC_RST_L
SMC_XTAL
SMC_EXTAL

R5809 10K 5% 1/16W MF-LF 402
R5801 10K 5% 1/16W MF-LF 402
KBC_MDE
SMC_MD1
SMC_NMI
SMC_TRST_L
NOSTUFF
R5898 10K 5% 1/16W MF-LF 402
R5803 0 5% 1/16W MF-LF 402
R5802 10K 5% 1/16W MF-LF 402

XW5800 SM
GND_SMC_AVSS

SMC

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

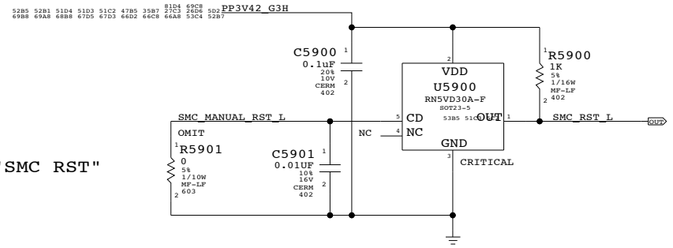
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

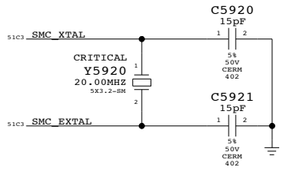
SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 51 OF 87	

SMC Reset Button / Brownout Detect

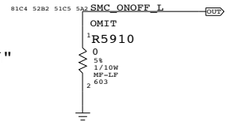


Silk: "SMC RST"

SMC Crystal Circuit

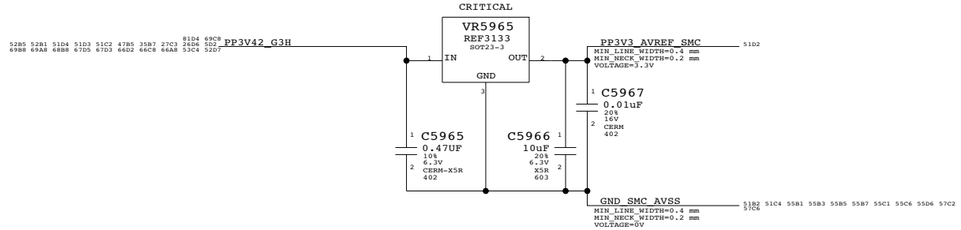


Debug Power Button

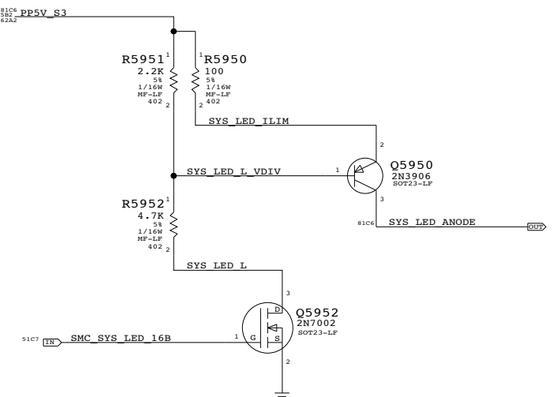


Silk: "PWR BTN"

SMC AVREF Supply

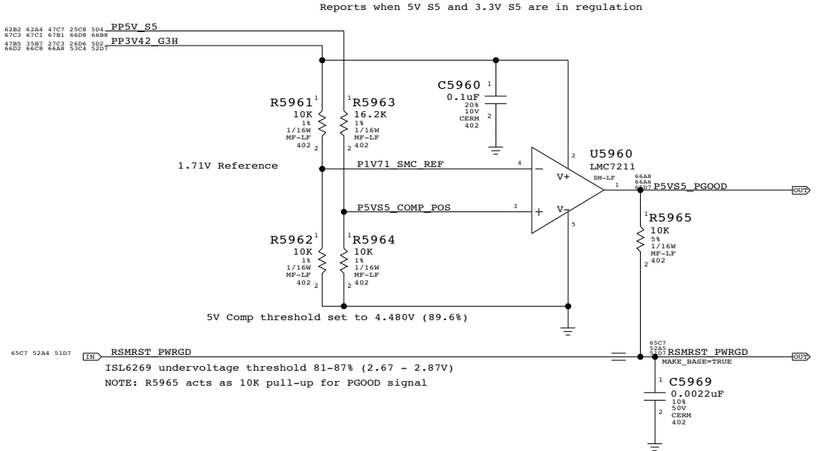


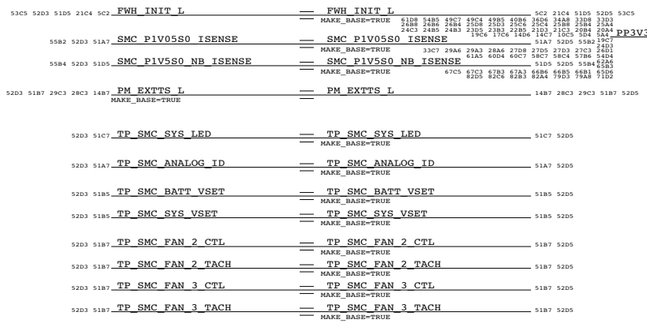
System (Sleep) LED Circuit

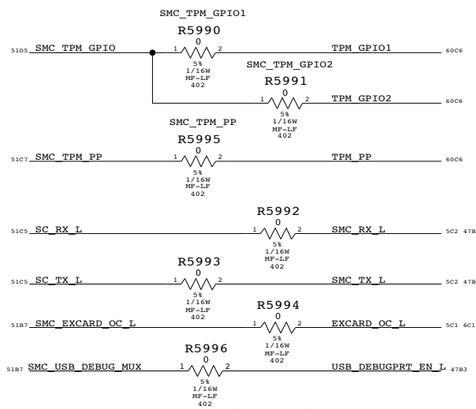


SMC PWRGD Circuit

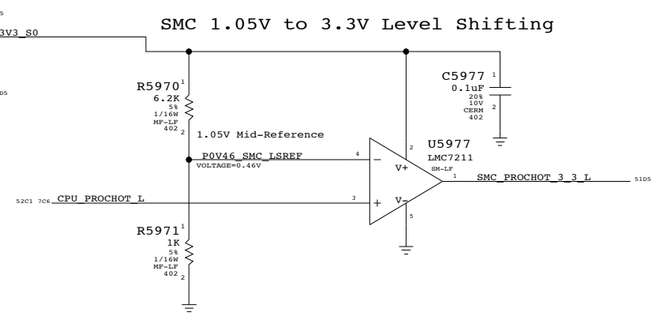
Reports when 5V S5 and 3.3V S5 are in regulation



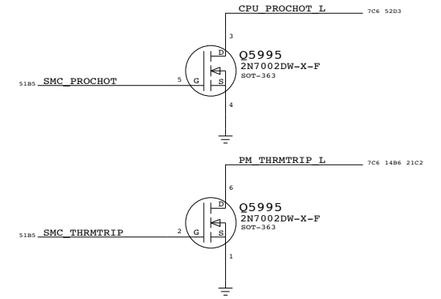


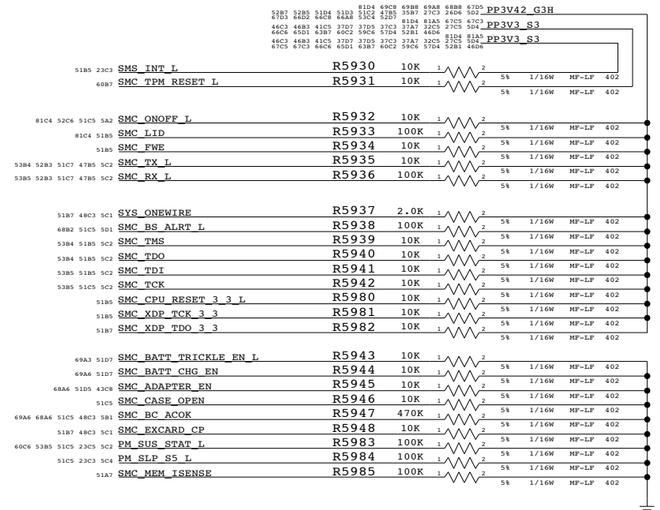


SMC 1.05V to 3.3V Level Shifting



SMC 3.3V to 1.05V Level Shifting





SMC Support

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

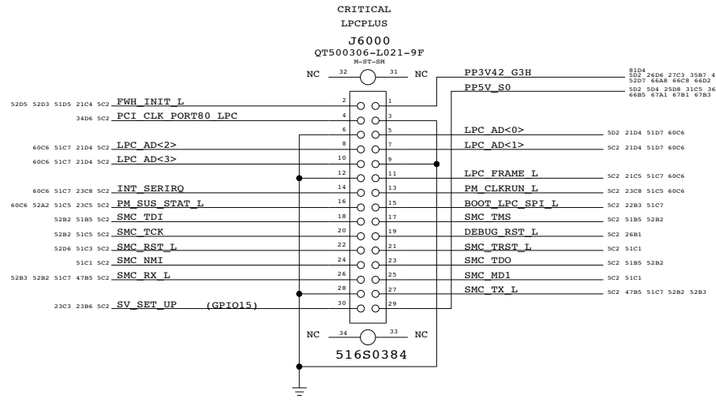
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 52 OF 87	



81D4
5D2 26D6 27C3 35B7 47B5 51C2 51D3 51D4 52B1 52B5 52B7
52D7 66A8 66C8 66D2 67D3 67D5 68B8 69A8 69B8 69C8
5D2 5D4 25D8 31C5 36D6 55A8 57B5 58C4 58C7 61D7 62B1
66B5 67A1 67B1 67B3 71A6 79B8 80A1 80B5 81B3

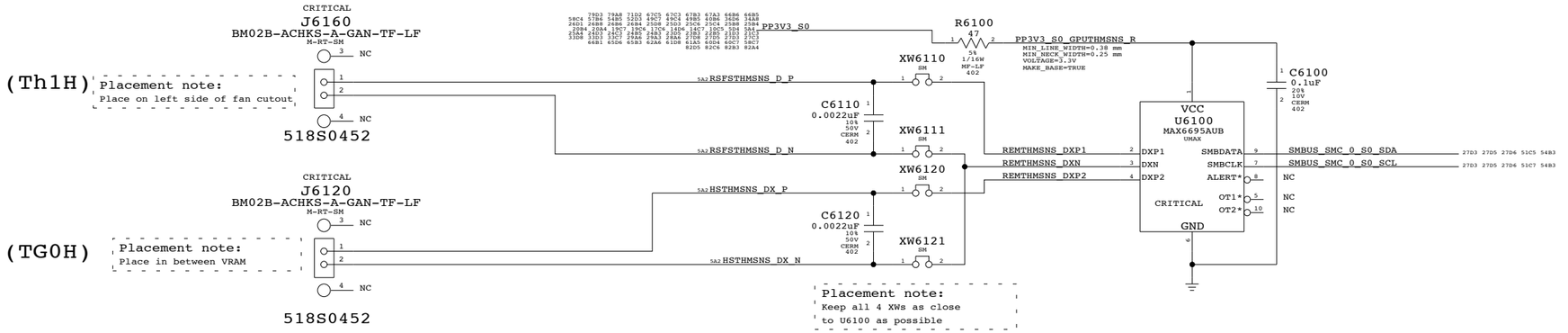
LPC+ Debug Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

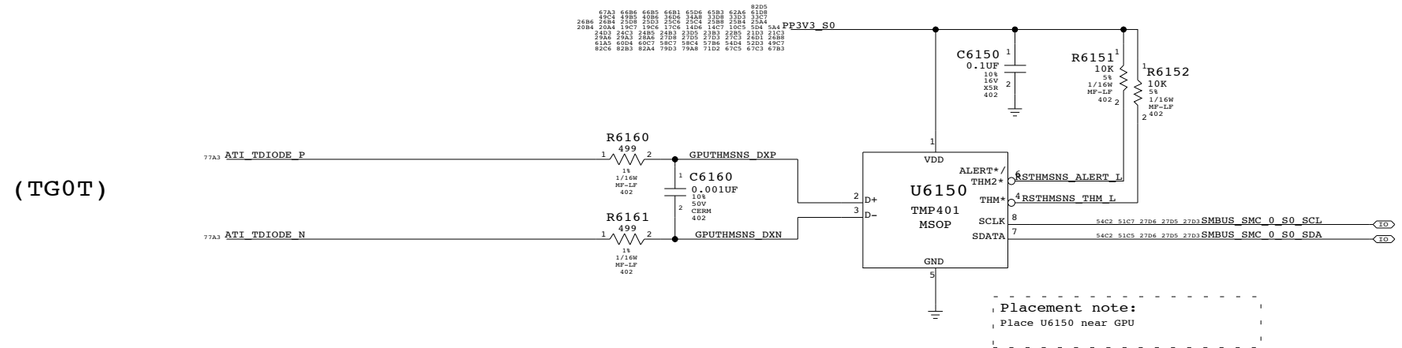
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 53 OF 87	

GPU/Heat Pipe & Bottom Case Skin Thermal Sensor



GPU Die Thermal Sensor



Thermal Sensors

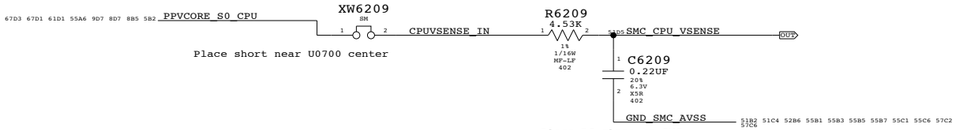
SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

APPLE COMPUTER INC.

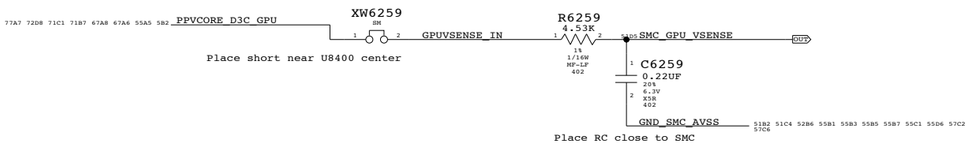
SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	54	87

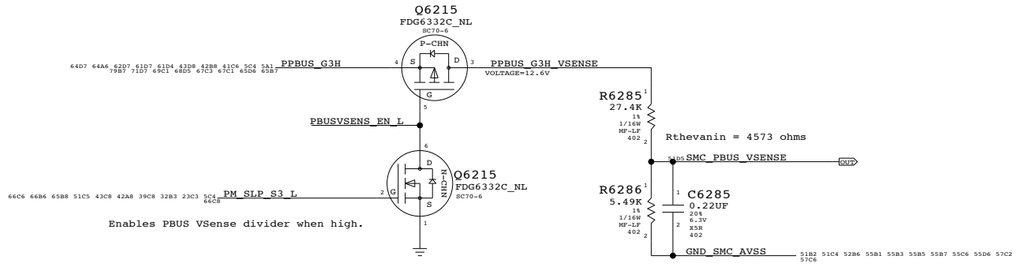
CPU Voltage Sense / Filter



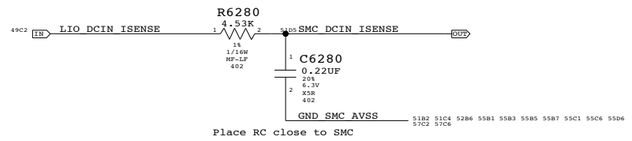
GPU Voltage Sense / Filter



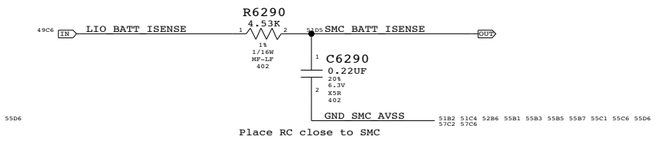
PBUS Voltage Sense Enable & Filter



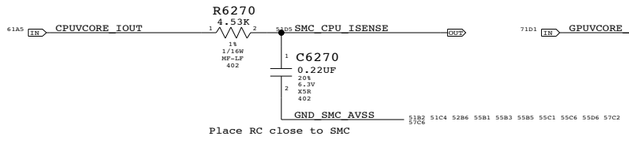
DCIN Current Sense Filter



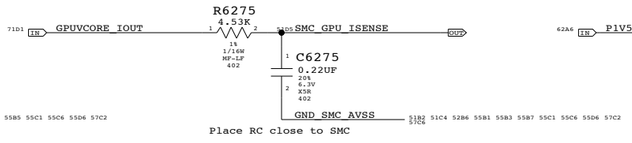
Battery Current Sense Filter



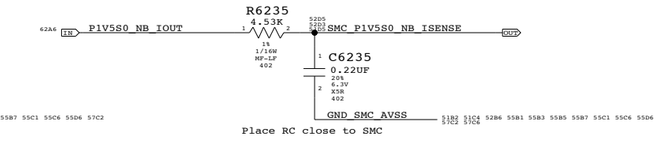
CPU Current Sense Filter



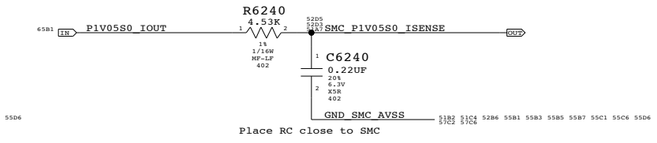
GPU Current Sense Filter



1.5V S0 (NB) Current Sense Filter

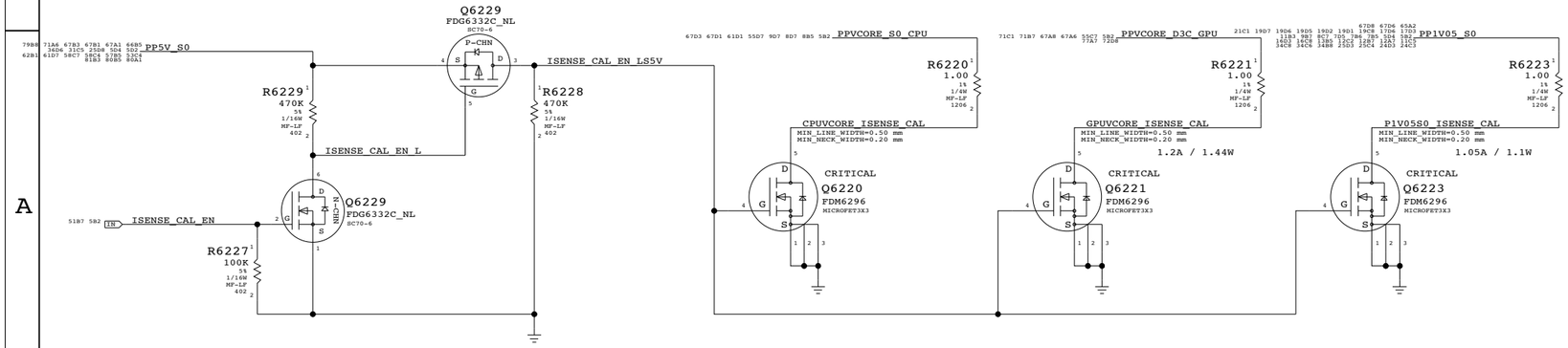


1.05V S0 (NB) Current Sense Filter



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits

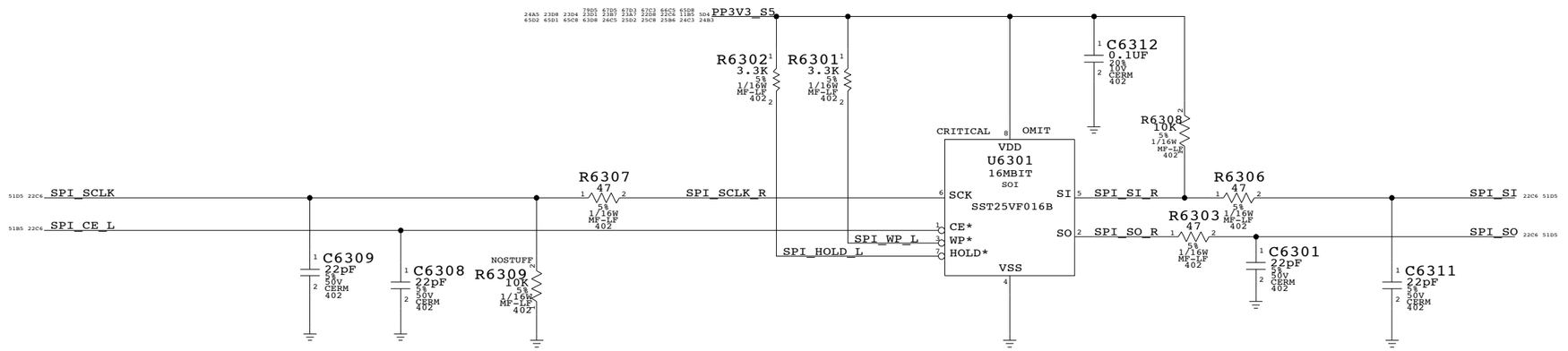


Current & Voltage Sensing

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 55 OF 87	



R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M

R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

SPI BOOTROM

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

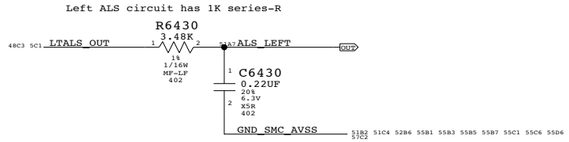
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

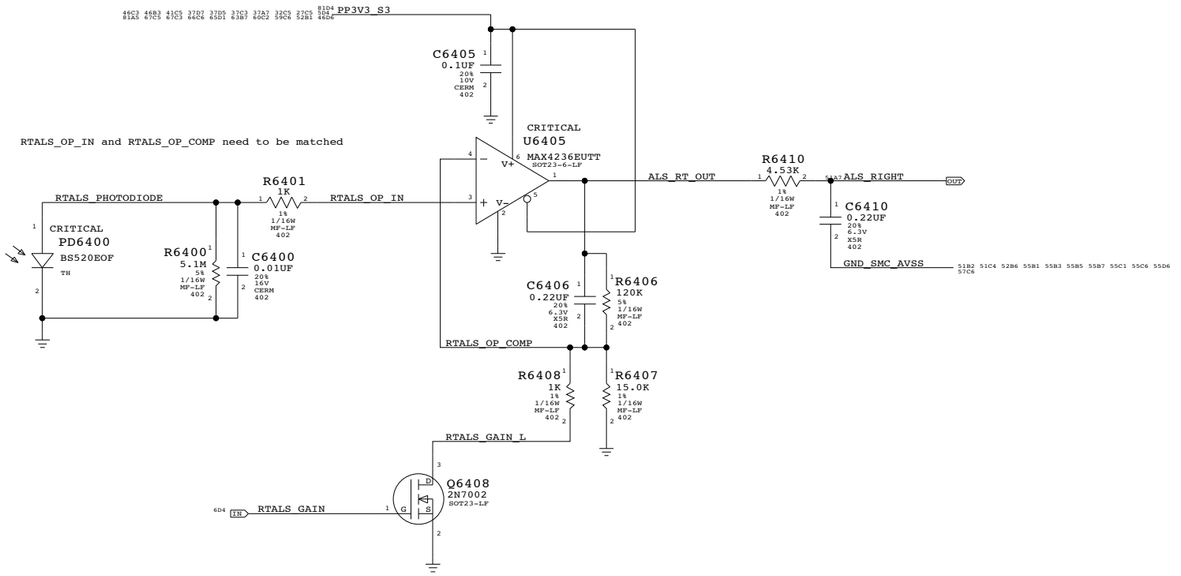
SCALE	SHT	OF
NONE	56	87

Left ALS Filter

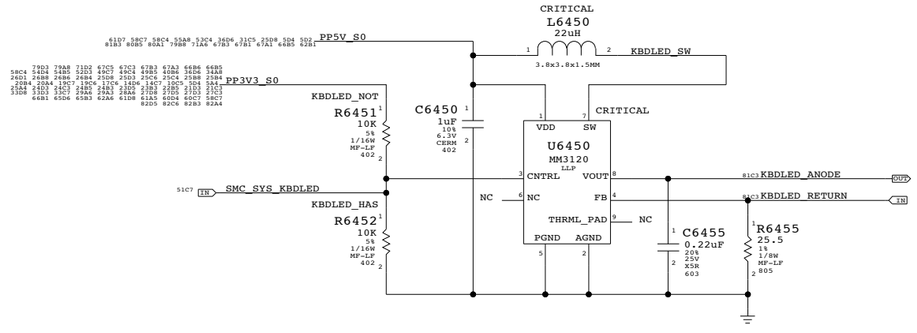
Left ALS circuit has 1K series-R



Right ALS Circuit



Keyboard LED Driver



ALS Support

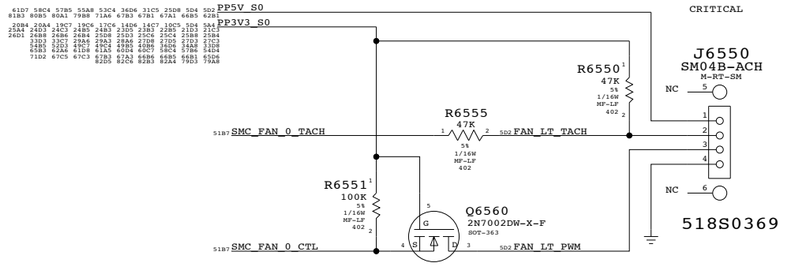
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

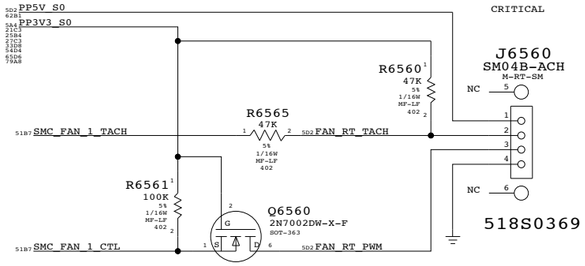
SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	57	87

Left Fan



Right Fan



Fan Connectors

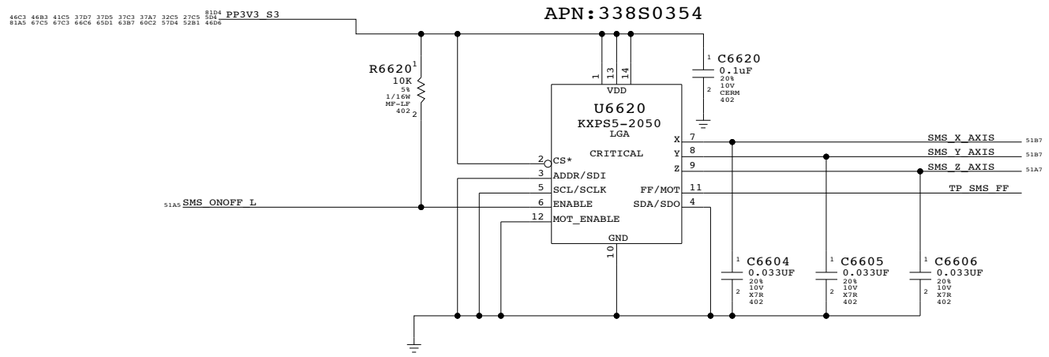
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

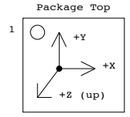
SCALE	SHT	OF
NONE	58	87

APN:338S0354



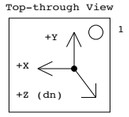
Desired orientation when placed on board top-side:

Package Top



Desired orientation when placed on board bottom-side:

Top-through View



M59 placement: Bottom-side

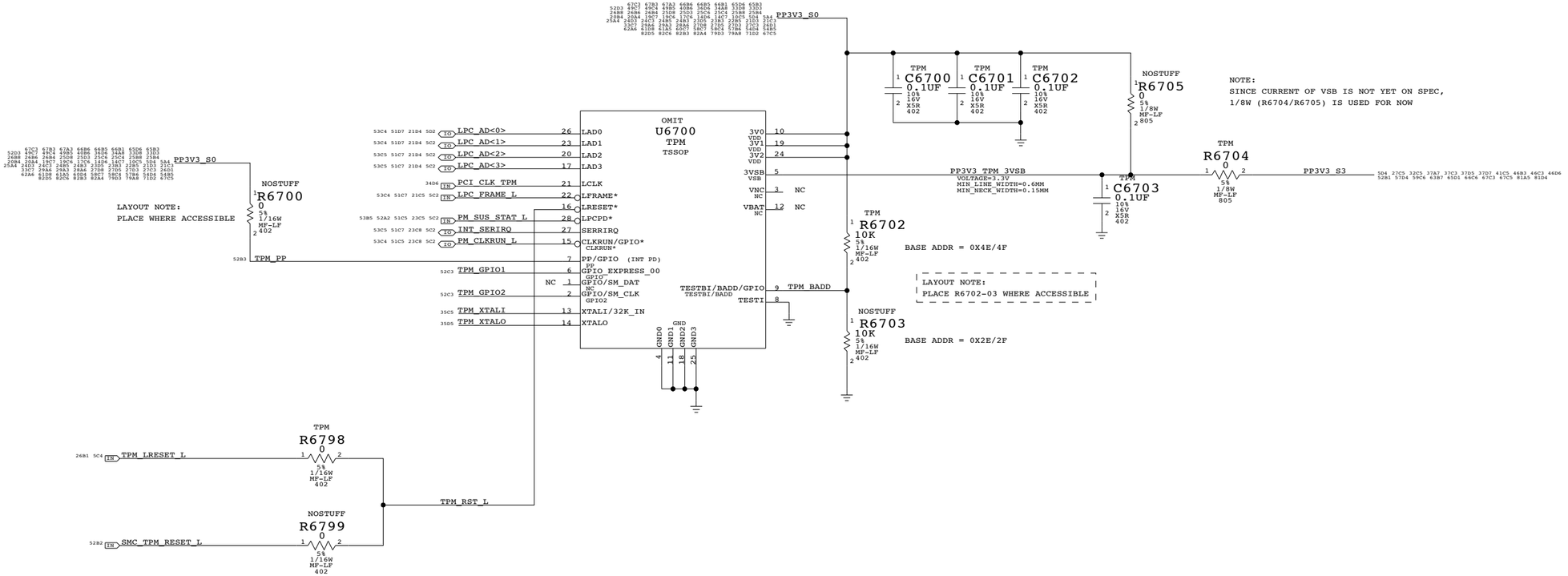
Sudden Motion Sensor (SMS)

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE NONE SHT 59 OF 87



TPM

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	60	87

DPRSLPVR	DPRSTP*	PSI*	Operation Mode	
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	1	0	1-Phase	DCM

These caps for Q7500

These caps for Q7550

Vout = Variable
36A max output
(Inductors limit)

U7530 ISL9504CRZ QFN

OMIT

Vout = Gain * ((2.1 mV/A * Iload) + Voffset)

Voffset = (Vdrp_offset * Kdroop) + Vamp_offset

Gain = Rc / (Ra + Rb)

Voffset worst-case -2.3mV (+/- ~1A offset)

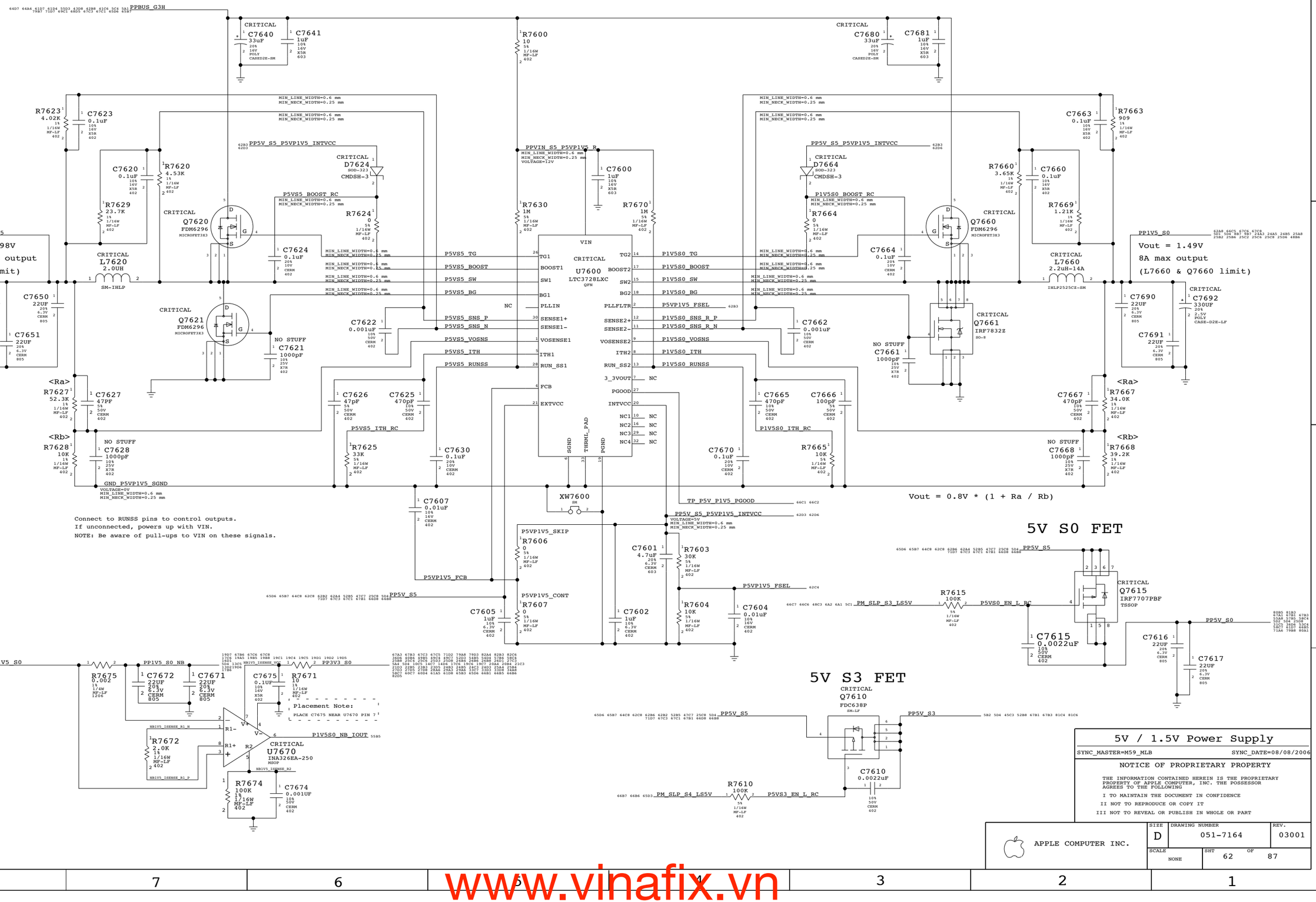
Vout @ 36A = 2.44V-2.60V

IMVP6 CPU VCore Regulator

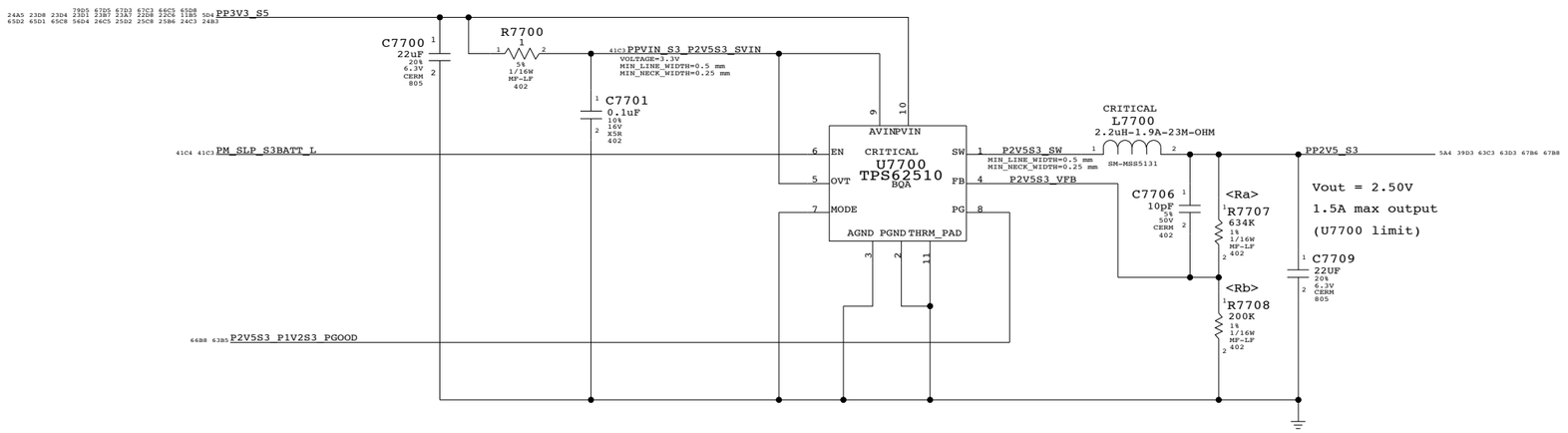
SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 61 OF 87	

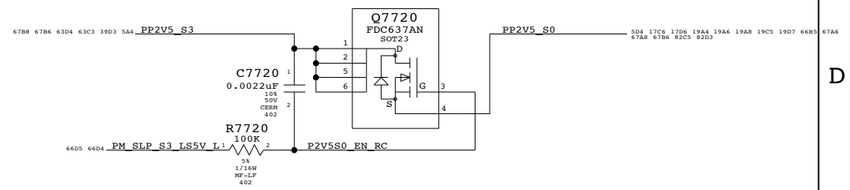


2.5V S3 Regulator

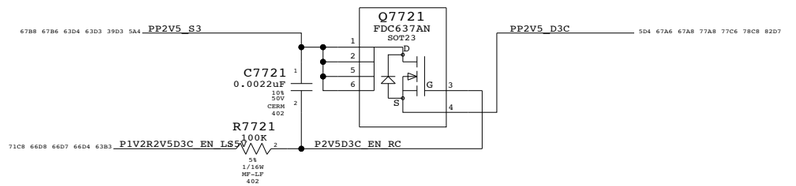


Vout = 0.6V * (1 + Ra / Rb)

2.5V S0 FET



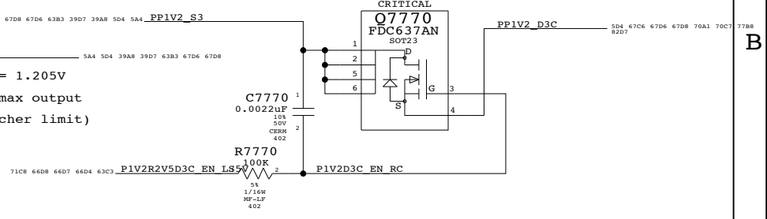
2.5V D3Cold FET



1.2V S3 Regulator

Vout = 0.8V * (1 + Ra / (Rb + Rc))

1.2V D3Cold FET

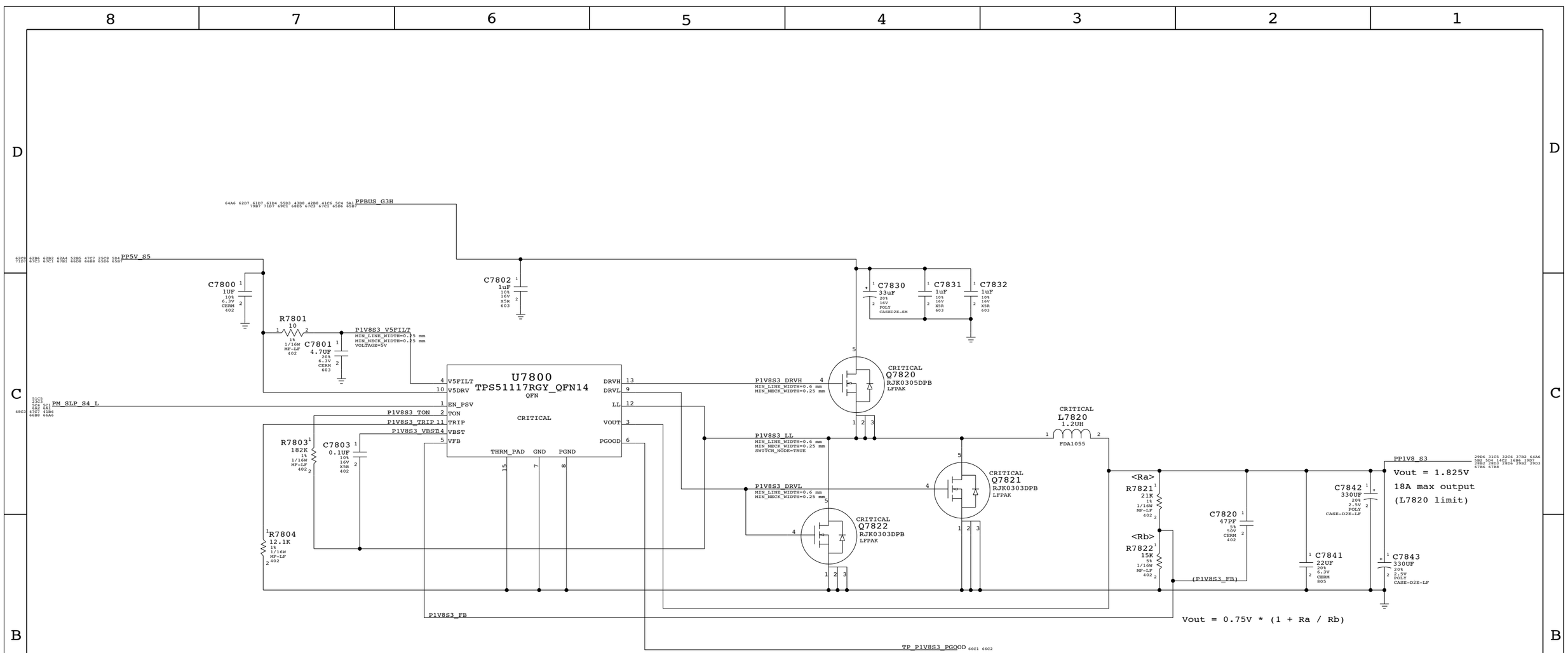


2.5V & 1.2V Regulators

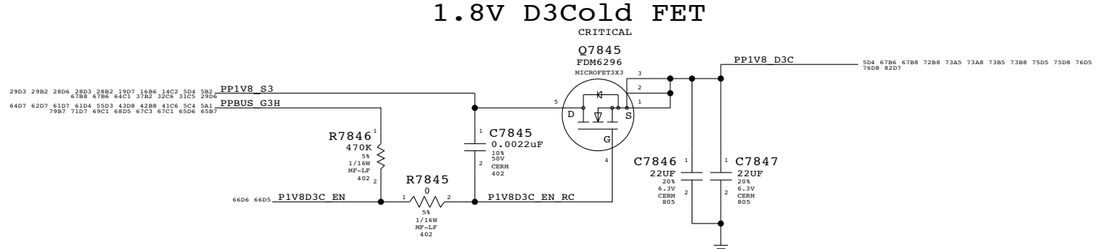
SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 63 OF 87	



1.8V D3Cold FET



1.8V Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

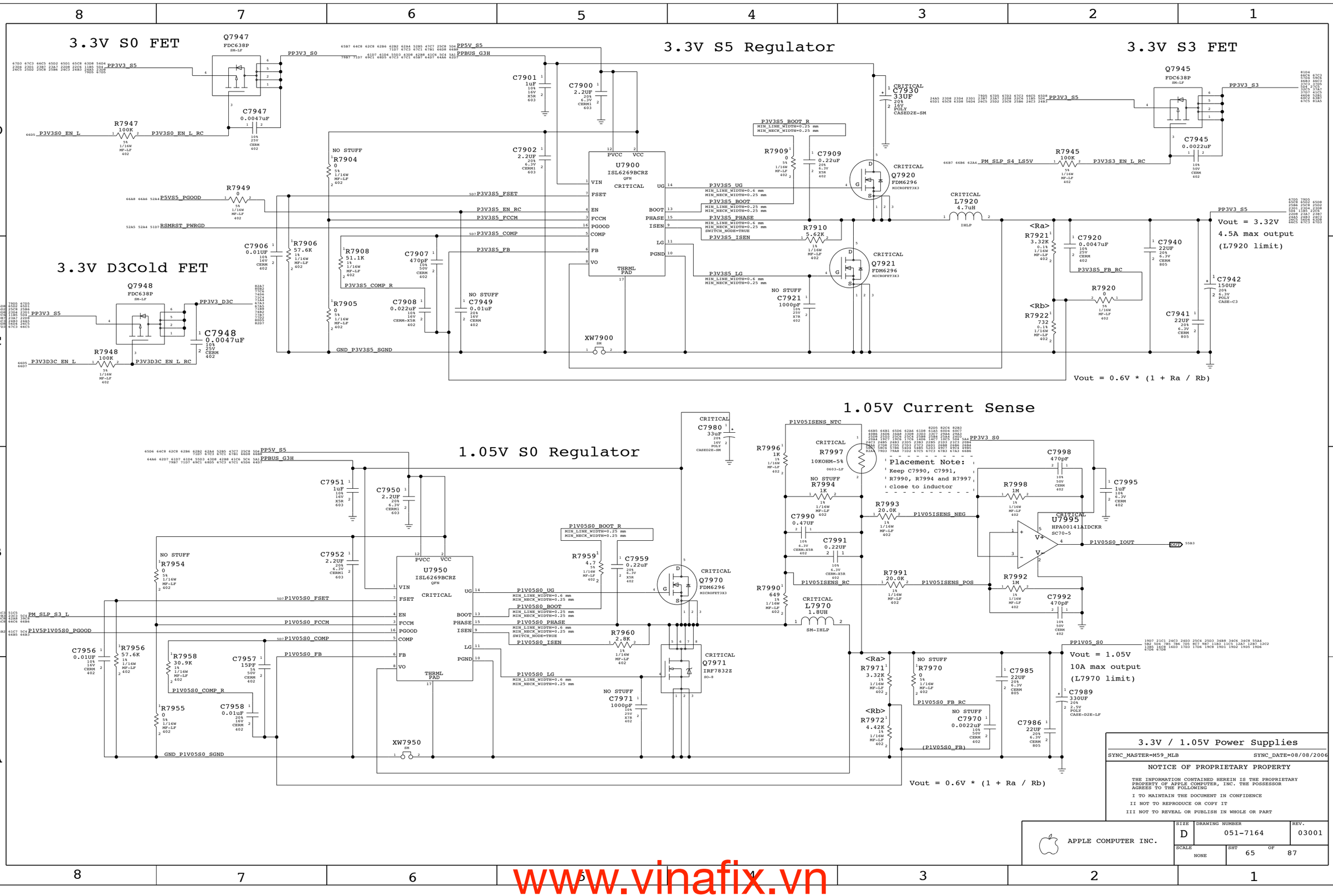
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	64	87



Power Control Signals

PP5V_S5

R8050 10K 5% 1/16W MF-LF 402

R8051 10K 5% 1/16W MF-LF 402

R8052 10K 5% 1/16W MF-LF 402

GPU requires 1.2V, 1.8V, 2.5V and 3.3V rise after VCore is up.

R8068 10K 5% 1/16W MF-LF 402

R8069 10K 5% 1/16W MF-LF 402

IN P1V2R2V5D3C_EN_LS5V

Need to ensure that ISL6269 PGOOD does not deassert while GPU PowerPlay is changing GPU core voltage.

P1V2R2V5D3C_EN_LS5V (MAKE_BASE=TRUE)

P1V2R2V5D3C_EN_LS5V

P1V2R2V5D3C_EN_LS5V

P3V3D3C_EN_L (MAKE_BASE=TRUE)

P3V3D3C_EN_L

P1V8D3C_EN (MAKE_BASE=TRUE)

P1V8D3C_EN

1.8V Enable has pull-up to PBUS

Q8055 2N7002DW-X-F SOT-363

Q8056 2N7002DW-X-F SOT-363

Q8050 2N7002DW-X-F SOT-363

Q8058 2N7002DW-X-F SOT-363

PM_SLP_S3_LS5V_L (MAKE_BASE=TRUE)

PM_SLP_S3_LS5V_L

P3V3S0_EN_L (MAKE_BASE=TRUE)

P3V3S0_EN_L

Q8058 2N7002DW-X-F SOT-363

PM_SLP_S3_LS5V (MAKE_BASE=TRUE)

PM_SLP_S3_LS5V

PM_SLP_S3_LS5V

P1V5S0_RUNSS

1.5V Enable has pull-up to PBUS

PP3V42_G3H

Q8050 2N7002DW-X-F SOT-363

R8054 100K 5% 1/16W MF-LF 402

Q8057 2N7002DW-X-F SOT-363

PM_SLP_S3

IN PM_SLP_S3_L

R8056 100K 5% 1/16W MF-LF 402

(PM_SLP_S3_L) MAKE_BASE=TRUE

PM_SLP_S3_L

PM_SLP_S3_L

PM_SLP_S3_L

PM_SLP_S3_L

PP3V3_S3

C8081 0.1uF 20% 10V CERM 402

R8053 10K 5% 1/16W MF-LF 402

R8081 10K 5% 1/16W MF-LF 402

IN P2V5S3_P1V2S3_PGOOD

IN P2V5S3_P1V2S3_PGOOD

Ensure 1.2V and 2.5V S3 supplies are up before enabling GPU VCore to support removing ethernet power in battery sleep.

R8060 NO STUFF 0 5% 1/16W MF-LF 402

P2V5S3_P1V2S3_PGOOD (MAKE_BASE=TRUE)

PM_SLP_S3_L_GPUVCORE_EN

MC74VHC1G08 SC70

U8081

GPUVCORE_EN (MAKE_BASE=TRUE)

GPUVCORE_EN

SB_GPUVCORE_DISABLE_L (MAKE_BASE=TRUE)

SB_GPUVCORE_DISABLE_L

The SB can turn off the GPUVcore (and by extension all D3Cold rails) by driving GPIO38 low.

PP5V_S5

R8055 10K 5% 1/16W MF-LF 402

PM_SLP_S4_LS5V (MAKE_BASE=TRUE)

PM_SLP_S4_LS5V

PM_SLP_S4_LS5V

Q8055 2N7002DW-X-F SOT-363

IN PM_SLP_S4_L

R8057 100K 5% 1/16W MF-LF 402

2.5V S3 and 1.2V S3 supplies are controlled by ethernet power control circuit.

(PM_SLP_S4_L) MAKE_BASE=TRUE

PM_SLP_S4_L

PM_SLP_S4_L

PM_SLP_S4_L

PP3V42_G3H

IN P5VS5_PGOOD

(P5VS5_PGOOD) MAKE_BASE=TRUE

P5VS5_PGOOD

P5VS5_RUNSS

5V Enable has pull-up to PBUS

R8059 470K 5% 1/16W MF-LF 402

Q8059 2N7002DW-X-F SOT-363

SMC_PM_G2_EN_L

Q8059 2N7002DW-X-F SOT-363

IN SMC_PM_G2_EN

R8058 100K 5% 1/16W MF-LF 402

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

PPDCIN_G3H

C8000 10UF 10% 25V X5R 1206-1

U8000 LT3470 TSOT23-8

VIN BOOST SHDN* SW BIAS NC NC CRITICAL FB GND

P3V42G3H5_BOOST

C8005 0.22uF 20% 6.3V X5R 402

CRITICAL L8010 33uH CDPH4D19F-SM

P3V42G3H_SW

MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE

P3V42G3H_FB

C8010 22pF 5% 50V CERM 402

<Ra> R8010 348K 1% 1/16W MF-LF 402

<Rb> R8011 200K 1% 1/16W MF-LF 402

PP3V42_G3H

Vout = 3.425
200mA max output
(Switcher limit)

C8015 22UF 20% 6.3V CERM 805

Vout = 1.25V * (1 + Ra / Rb)

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

PP3V3_S5

PP1V5_S0

0.89V Reference

R8061 27.4K 1% 1/16W MF-LF 402

R8063 4.99K 1% 1/16W MF-LF 402

C8060 0.1uF 20% 10V CERM 402

U8060 LMC7211 SM-LF

P1V0_P1V5PG_REF

P1V5S0_COMP_POS

P1V5S0_PGOOD

R8062 10K 1% 1/16W MF-LF 402

R8064 10K 1% 1/16W MF-LF 402

R8065 10K 5% 1/16W MF-LF 402

1.5V Comp threshold set to 1.32V (88%)

P1V5P1V05S0_PGOOD (OUT)

IN P1V5P1V05S0_PGOOD

P1V5P1V05S0_PGOOD (MAKE_BASE=TRUE)

ISL6269 undervoltage threshold 81-87% (0.85 - 0.91V)
NOTE: R8065 acts as 10K pull-up for PGOOD signal

Unused PGOOD Signals

TP_P5V_P1V5_PGOOD — TP_P5V_P1V5_PGOOD (MAKE_BASE=TRUE)

TP_P1V8S3_PGOOD — TP_P1V8S3_PGOOD (MAKE_BASE=TRUE)

Other S0 Rails PWRGD Circuit

Does not include D3C rails for GPU!!

PP3V3_S0

PP5V_S0

PP2V5_S0

PPDV9_S0

R8074 68.1K 1% 1/16W MF-LF 402

R8072 365K 1% 1/16W MF-LF 402

R8070 845K 1% 1/16W MF-LF 402

C8070 0.1uF 20% 10V CERM 402

U8070 LTC2903 TSOT-23

V1 V2 V3 V4 RST* GND

CRITICAL

S0PGOOD_5V_DIV

S0PGOOD_2V5_DIV

S0PGOOD_0V9_DIV

S0PGOOD_PWROK

R8076 10K 5% 1/16W MF-LF 402

R8075 100K 1% 1/16W MF-LF 402

C8075 0.1UF 20% 10V CERM 402

R8073 100K 1% 1/16W MF-LF 402

C8073 0.1UF 20% 10V CERM 402

R8071 100K 1% 1/16W MF-LF 402

C8071 0.1UF 20% 10V CERM 402

LTC2903 guaranteed threshold is 93.5% (3.055V, 4.725V, 2.325V, 0.840V)

PP3V3_S0

MC74VHC1G08 SC70

U8080

ALL_SYS_PWRGD (OUT)

PGOOD_MUXED_S0_OR_S0D3C

C8080 0.1UF 20% 10V CERM 402

3.3V G3Hot Supply & Power Control

SYNC_MASTER=M57_MLB_MG SYNC_DATE=08/08/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE: NONE SHT 66 OF 87

"S3AC" rail is ON in S3 on AC, OFF in S3 on battery

PP0V9_S0
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE

PP1V05_S0
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE

PP1V2_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.22 mm
VOLTAGE=1.2V
MAKE_BASE=TRUE

PP1V2_D3C
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.2V
MAKE_BASE=TRUE

PP1V5_S0
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE

PP1V5_S0_NB
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE

PP1V8_S3
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE

PP1V8_D3C
MIN_LINE_WIDTH=0.6 mm MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.8V

PP2V5_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=2.5V
MAKE_BASE=TRUE

PP2V5_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=2.5V
MAKE_BASE=TRUE

PP2V5_D3C
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=2.5V
MAKE_BASE=TRUE

PPVCORE_D3C_GPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.2V
MAKE_BASE=TRUE

PPDCIN_G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V
MAKE_BASE=TRUE

GND
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.25mm
VOLTAGE=0V

PP3V42_G3H
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.425V
MAKE_BASE=TRUE

PP3V3_S5
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S3
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S0
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_D3C
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S3AC
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.22 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE

PNBB_S0_GPU
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0.7V
MAKE_BASE=TRUE

PPBB_S0_GPU
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.9V
MAKE_BASE=TRUE

PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.1V
MAKE_BASE=TRUE

PPBUS_G3H
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE

PPBUS_S5_FW_FET
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.3 mm
VOLTAGE=33V
MAKE_BASE=TRUE

PP5V_S5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S3
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE

Power Aliases

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

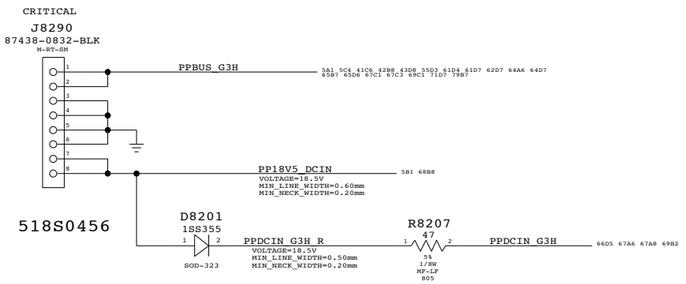
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

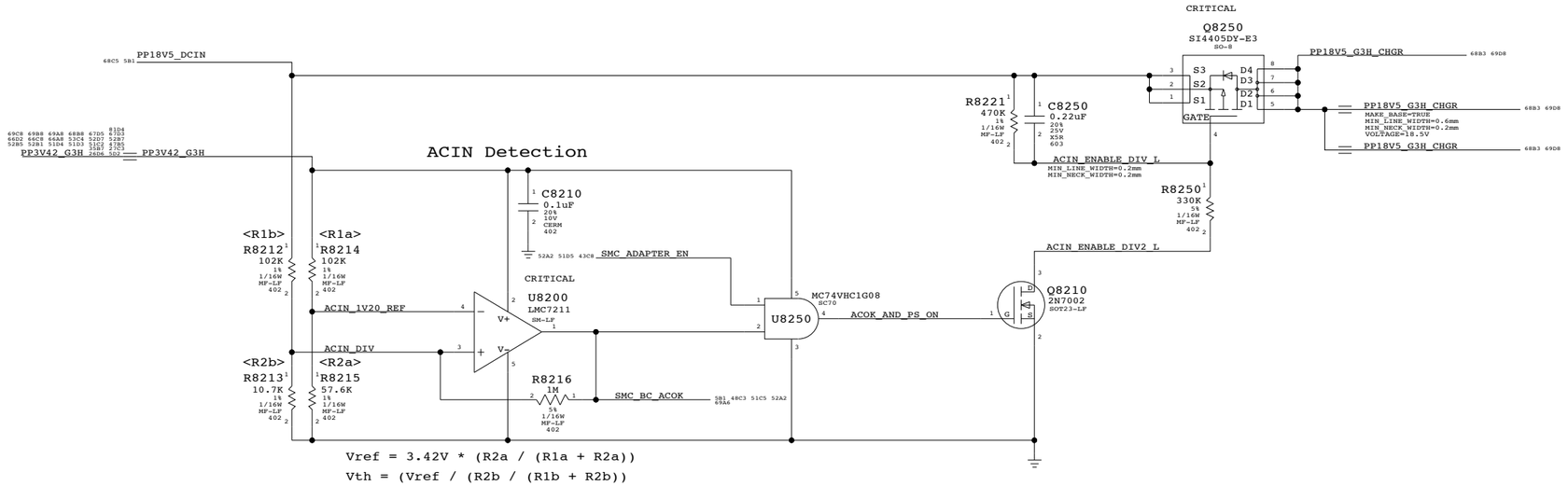
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 67 OF 87	

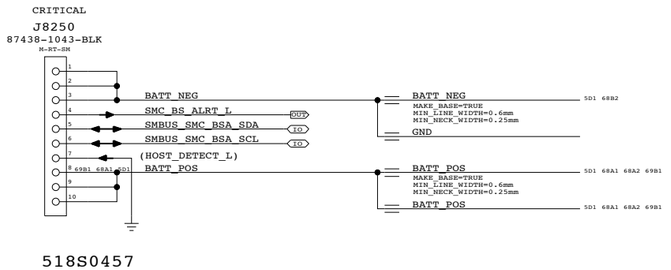
DC-In Connector



Inrush Limiter



Battery Connector



DC-In & Battery Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	68	87

PBus Supply & Battery Charger

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1510	1	ISL6257H,BATT CHGR,28P,QFN,LF	U8300	CRITICAL	ISL6257H
116S0004	1	0 OHM,5%,1/16W,0402,SMD,LF	R8304		ISL6257H

VOLTAGE FOLLOWER GUARANTEES CURRENT LIMIT CIRCUITS ARE PROVIDED WITH SUFFICIENT CURRENT WITHOUT SINKING CURRENT FROM VREF.

Adapter Input Current Limit

As shown, Isys =-4.6A max

Battery Charge Current Limit

As shown, Ichg = 3.9A max

Battery Charge FET

PBus Supply & Batt. Charger	
SYNC_MASTER=M59_LIO	SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

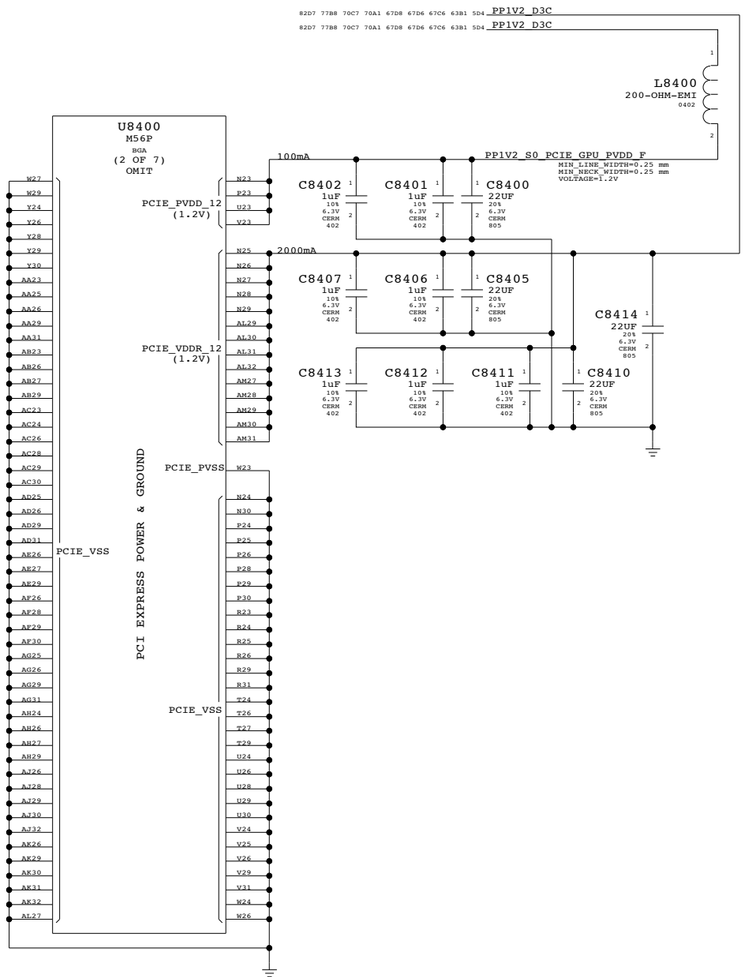
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

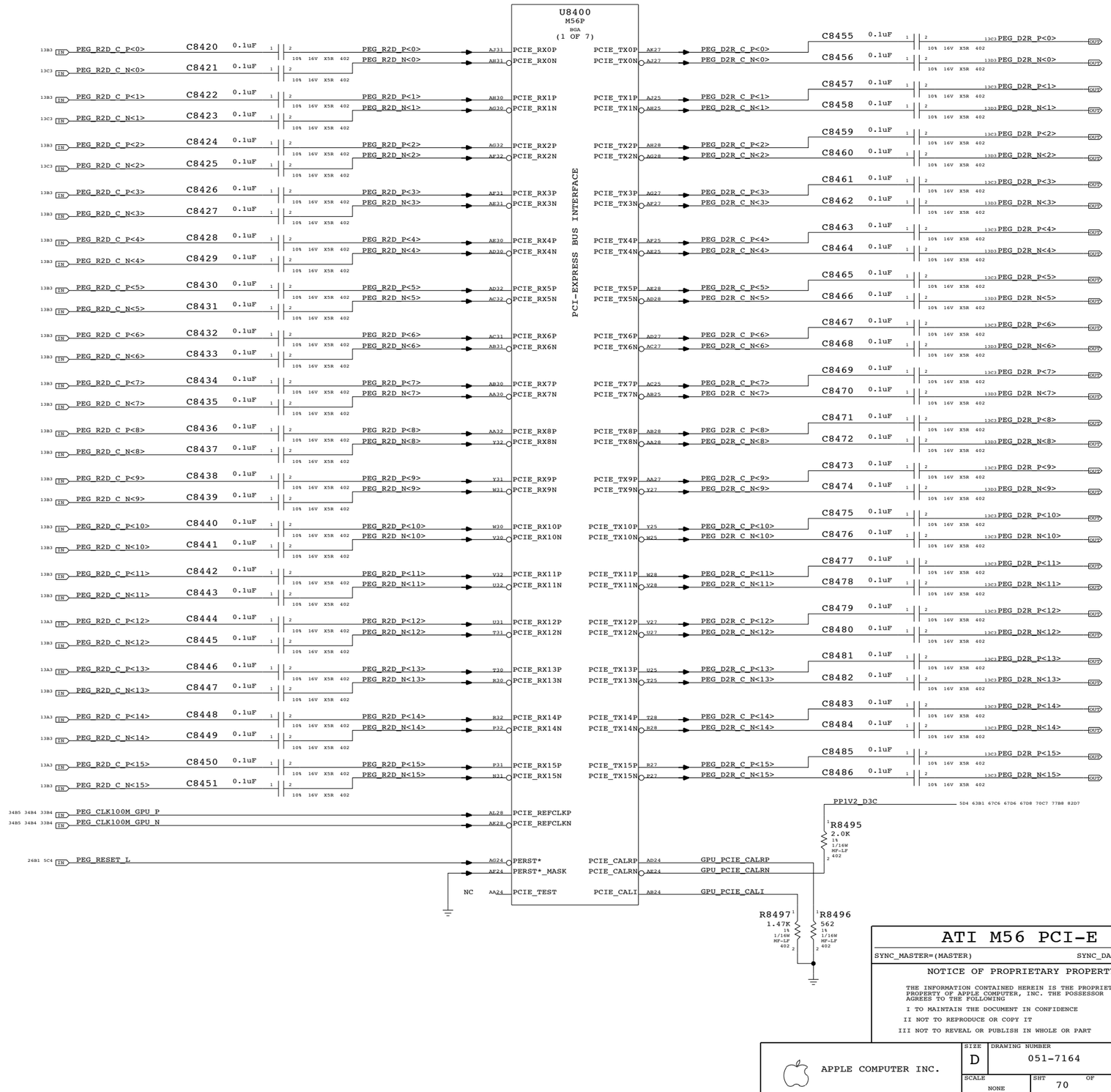
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

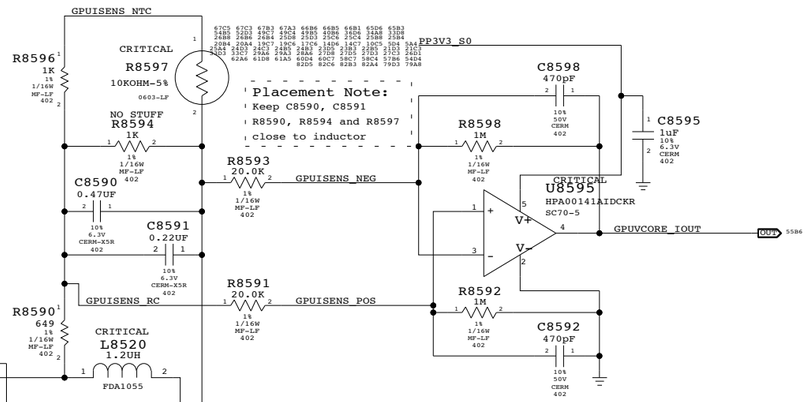
SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 69 OF 87	





ATI M56 PCI-E			
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)		
NOTICE OF PROPRIETARY PROPERTY			
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART			
APPLE COMPUTER INC.	SIZE: D	DRAWING NUMBER: 051-7164	REV.: 03001
	SCALE: NONE	SHT: 70 OF 87	

GPU VCore Current Sense

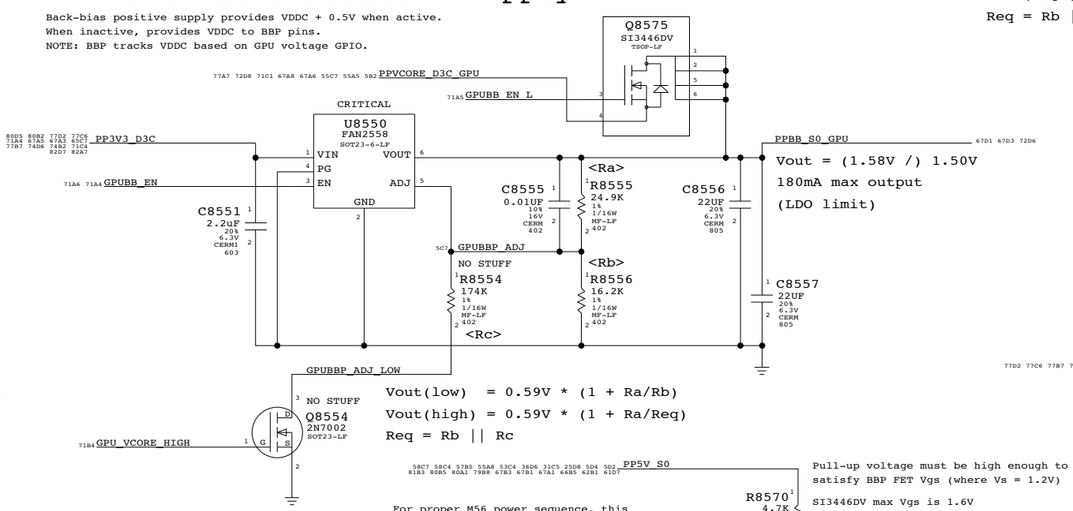


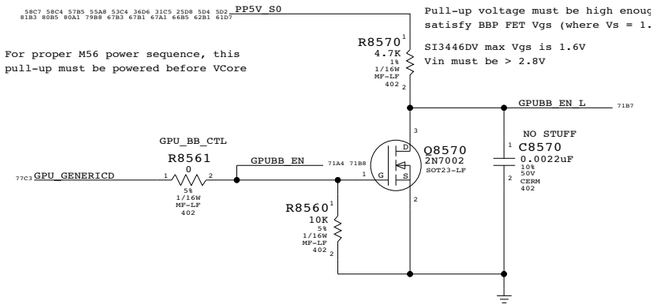
GPU VCore Supply

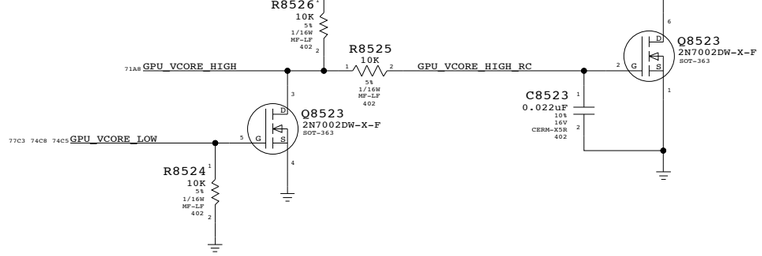
Vout(low) = 0.6V * (1 + Ra / Rb)
Vout(high) = 0.6V * (1 + Ra / Req)
Req = Rb || Rc

Back-Bias Positive Supply

Back-bias positive supply provides VDDC + 0.5V when active.
When inactive, provides VDDC to BBP pins.
NOTE: BBP tracks VDDC based on GPU voltage GPIO.

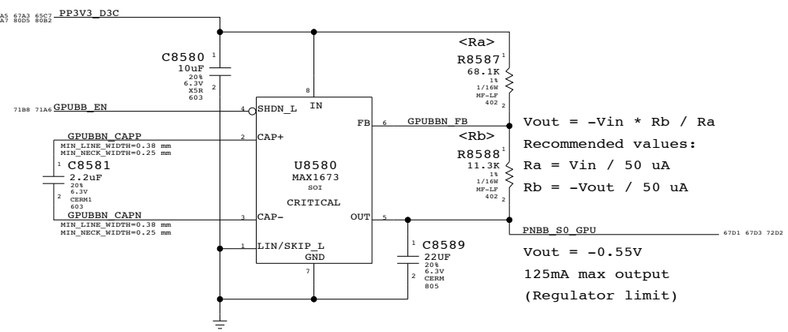






Back-Bias Negative Supply

Back-bias negative supply provides VSS - 0.55V when active.
When inactive, provides VSS to BBN pins.



GPU (M56) Core Supplies		
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)	

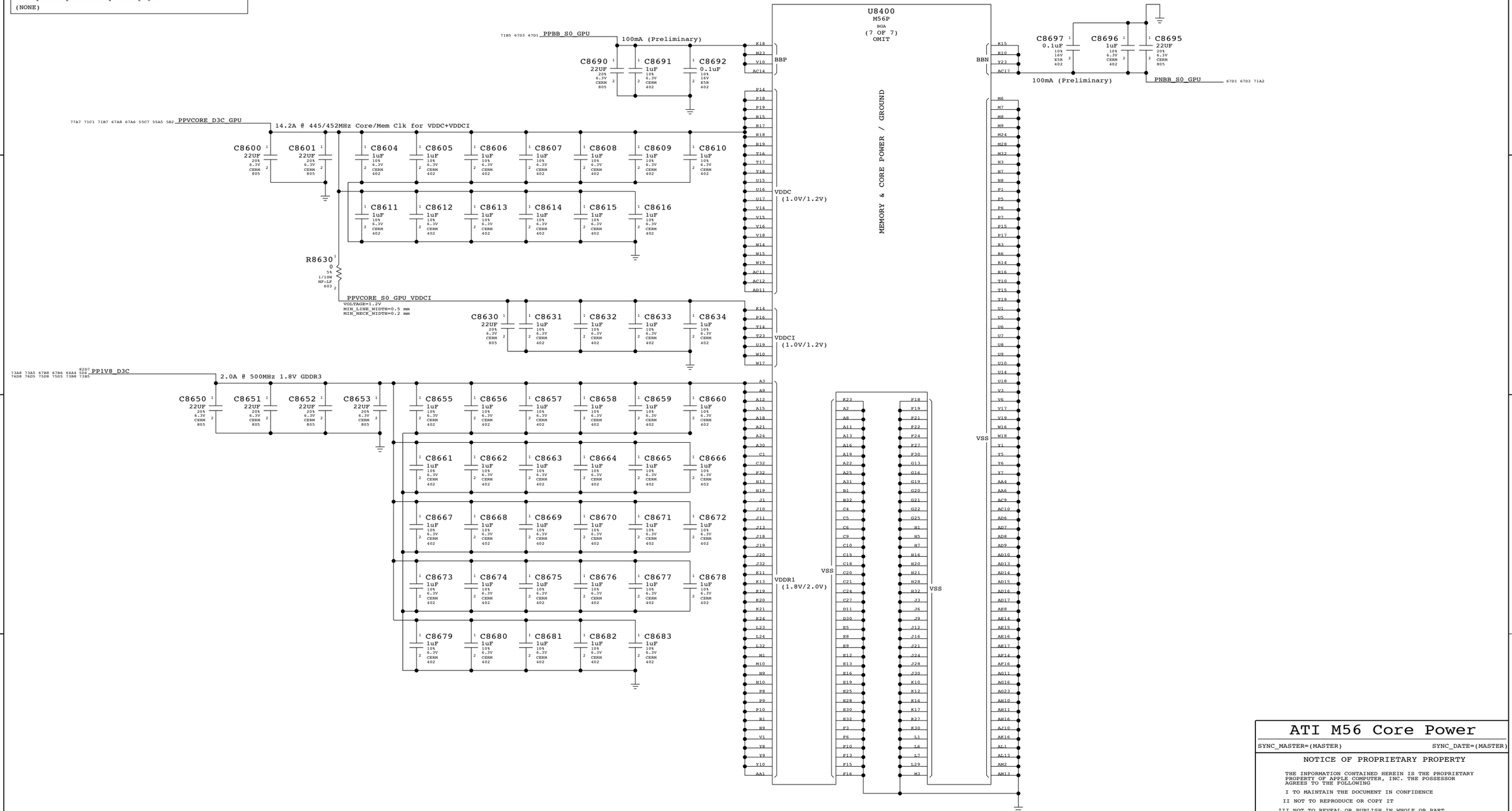
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7164	03001
	SCALE: NONE	SHT 71 OF 87	

Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Core Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

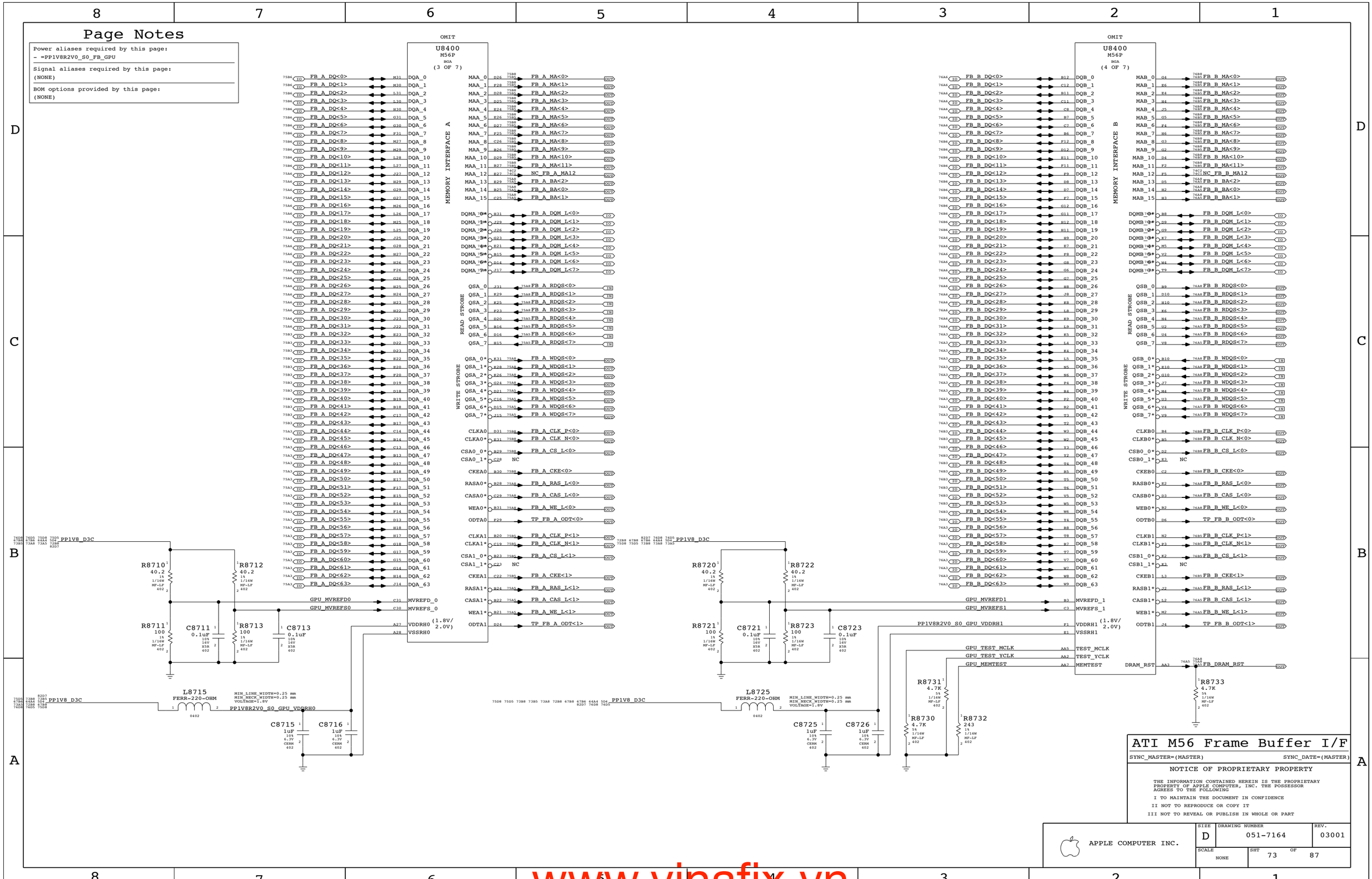
SCALE: NONE SHT 72 OF 87

Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 73 OF 87	

ROMCFGID[3..0]

0000 = 128MB
0010 = 256MB
0100 = 64MB
0110 = Reserved

77D2 77C6 77B7 74B2 71C4 71B8 71A4 67A5 67A3 65C7 82D7 82A7 80D5 80B2 PP3V3_D3C

R8800 10K 5% 1/16W MF-LF 402
GPU_DEEPMH_EN
R8801 10K 5% 1/16W MF-LF 402
NO STUFF
R8802 10K 5% 1/16W MF-LF 402
NO STUFF
R8803 10K 5% 1/16W MF-LF 402
NO STUFF
R8804 10K 5% 1/16W MF-LF 402
NO STUFF
R8805 10K 5% 1/16W MF-LF 402
NO STUFF
R8806 10K 5% 1/16W MF-LF 402
NO STUFF
R8808 10K 5% 1/16W MF-LF 402
NO STUFF
R8809 10K 5% 1/16W MF-LF 402
GPU_MEM_64M
R8813 10K 5% 1/16W MF-LF 402
GPU_MEM_256M
R8812 10K 5% 1/16W MF-LF 402
NO STUFF
R8811 10K 5% 1/16W MF-LF 402
GPU_MEM_256M
R8824 10K 5% 1/16W MF-LF 402
GPU_MEM_NOT_SAM
R8827 10K 5% 1/16W MF-LF 402

		Serial ROM	Test Bus	Misc	Straps
77D3 GPU_GPIO_0	IPD		TESTIN[0]		TX_PWRS_ENb
77D3 GPU_GPIO_1	IPD		TESTIN[1]		TX_DEEMPH_EN
77D3 GPU_GPIO_2		VDD_VCL	TESTIN[2]		Reserved
77D3 GPU_GPIO_3			TESTIN[3]		Reserved
77D3 GPU_GPIO_4	IPD		TESTIN[4]		DEBUG_ACCESS
77D3 GPU_GPIO_5			TESTIN[5]		Reserved
77D3 GPU_GPIO_6			TESTIN[6]		Reserved
82A4 77D3 74C5 GPU_BLON		ENA_BL	TESTIN[7]		
77D3 GPU_GPIO_8		ROMSO	TESTWR		Reserved
77C3 GPU_GPIO_9	IPD	ROMSI			ROMIDCFG[3]
77C3 74C5 TP_GPU_GPIO_10		ROMSCK	TESTOUT[8]		
77C3 GPU_GPIO_11	IPD		TESTOUT[9]		ROMIDCFG[0]
77C3 GPU_GPIO_12	IPD		TESTOUT[10]		ROMIDCFG[1]
77C3 GPU_GPIO_13	IPD		TESTOUT[11]		ROMIDCFG[2]
77C3 74C5 NC_GPU_GPIO_14			TESTIN[8]		
77C3 74C5 71B4 GPU_VCORE_LOW			TESTIN[9]	PWRCNTL	
77C3 74C5 34B4 34B2 GPU_CLK27MSS_IN				SS_IN	
77C3 74C5 NC_GPU_GPIO_17				Thm Mon	Int

GPU_BLON — MAKE_BASE=TRUE — 74C8 77D3 82A4
TP_GPU_GPIO_10 — MAKE_BASE=TRUE — 74C8 77C3
NC_GPU_GPIO_14 — MAKE_BASE=TRUE NO_TEST=TRUE — 74C8 77C3
GPU_VCORE_LOW — MAKE_BASE=TRUE — 71B4 74C8 77C3
GPU_CLK27MSS_IN — MAKE_BASE=TRUE — 34B2 34B4 74C8 77C3
NC_GPU_GPIO_17 — MAKE_BASE=TRUE NO_TEST=TRUE — 74C8 77C3

Required for debug access
Required for debug access
Required for debug access
Required for debug access

77D5 74B7 NC_GPU_GPIO_18 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_18 — 74B8 77D5
77D5 74B7 NC_GPU_GPIO_19 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_19 — 74B8 77D5
77D5 74B7 NC_GPU_GPIO_20 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_20 — 74B8 77D5
77D5 74B7 NC_GPU_GPIO_21 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_21 — 74B8 77D5
77D5 74B7 NC_GPU_GPIO_22 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_22 — 74B8 77D5
77D5 74B7 NC_GPU_GPIO_23 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_23 — 74B8 77D5
77D5 74B6 GPU_MEM_256M — 77D5 74B8 GPU_MEM_256M — MAKE_BASE=TRUE
77D5 74B7 NC_GPU_GPIO_25 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_25 — 74B8 77D5
77D5 74B7 NC_GPU_GPIO_26 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_26 — 74B8 77D5
77D5 74B6 GPU_MEMID — 77D5 74B8 GPU_MEMID — MAKE_BASE=TRUE
77D5 74B7 NC_GPU_GPIO_28 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_28 — 74B8 77D5
77C5 74B7 NC_GPU_GPIO_29 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_29 — 74B8 77C5
77C5 74B7 NC_GPU_GPIO_30 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_30 — 74B8 77C5
77C5 74B7 NC_GPU_GPIO_31 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_31 — 74B8 77C5
77C5 74B7 NC_GPU_GPIO_32 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_32 — 74B8 77C5
77C5 74B7 NC_GPU_GPIO_33 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_33 — 74B8 77C5
77C5 74B7 NC_GPU_GPIO_34 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_34 — 74B8 77C5

Renamed signals

77A5 74C1 34B4 34B2 GPU_CLK27M — MAKE_BASE=TRUE — GPU_CLK27M — 34B2 34B4 74C2 77A5

Unused signals

77A5 74C1 NC_GPU_XTALOUT — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_XTALOUT — 74C2 77A5
77A3 74C1 NC_ATI_ROMCS_L — MAKE_BASE=TRUE NO_TEST=TRUE — NC_ATI_ROMCS_L — 74C2 77A3
74C1 73D5 NC_FB_A_MA12 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_FB_A_MA12 — 73D5 74C2
74C1 73D1 NC_FB_B_MA12 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_FB_B_MA12 — 73D1 74C2
77C3 74C1 NC_GPU_GENERICA — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GENERICA — 74C2 77C3
77C3 74C1 NC_GPU_GENERICB — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GENERICB — 74C2 77C3
77C3 74C1 NC_GPU_GENERICC — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GENERICC — 74C2 77C3
78C3 74C1 NC_GPU_VGA_R — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_VGA_R — 74C2 78C3
78C3 74C1 NC_GPU_VGA_G — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_VGA_G — 74C2 78C3
78C3 74C1 NC_GPU_VGA_B — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_VGA_B — 74C2 78C3
78B3 74C1 TP_GPU_VGA_HSYNC — MAKE_BASE=TRUE — TP_GPU_VGA_HSYNC — 74C2 78B3
78B3 74C1 TP_GPU_VGA_VSYNC — MAKE_BASE=TRUE — TP_GPU_VGA_VSYNC — 74C2 78B3
78B3 74C1 NC_GPU_TV_Y — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_TV_Y — 74C2 78B3
78B3 74B1 NC_GPU_TV_C — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_TV_C — 74B2 78B3
78B3 74B1 NC_GPU_TV_COMP — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_TV_COMP — 74B2 78B3
78B3 74B1 NC_LVDS_U_DATAP<3> — MAKE_BASE=TRUE NO_TEST=TRUE — NC_LVDS_U_DATAP<3> — 74B2 78B3
78B3 74B1 NC_LVDS_U_DATAN<3> — MAKE_BASE=TRUE NO_TEST=TRUE — NC_LVDS_U_DATAN<3> — 74B2 78B3
78A3 74B1 NC_LVDS_L_DATAP<3> — MAKE_BASE=TRUE NO_TEST=TRUE — NC_LVDS_L_DATAP<3> — 74B2 78A3
78A3 74B1 NC_LVDS_L_DATAN<3> — MAKE_BASE=TRUE NO_TEST=TRUE — NC_LVDS_L_DATAN<3> — 74B2 78A3
77C3 74B1 NC_ATI_DVPCLK — MAKE_BASE=TRUE NO_TEST=TRUE — NC_ATI_DVPCLK — 74B2 77C3
77C3 77B3 NC_ATI_DVPCNTL<2..0> — MAKE_BASE=TRUE NO_TEST=TRUE — ATI_DVPCNTL<2..0>
77B3 NC_ATI_DVPDATA<15..0> — MAKE_BASE=TRUE NO_TEST=TRUE — ATI_DVPDATA<15..0>

Required for debug access

77B3 77A3 TP_ATI_DVPDATA<23..16> — MAKE_BASE=TRUE — ATI_DVPDATA<23..16>

Also required: GPIO10 - GPIO13

77D2 77C6 77B7 74D6 71C4 71B8 71A4 67A5 67A3 65C7 82D7 82A7 80D5 80B2 PP3V3_D3C

R8890 4.7K 5% 1/16W MF-LF 402
R8891 4.7K 5% 1/16W MF-LF 402

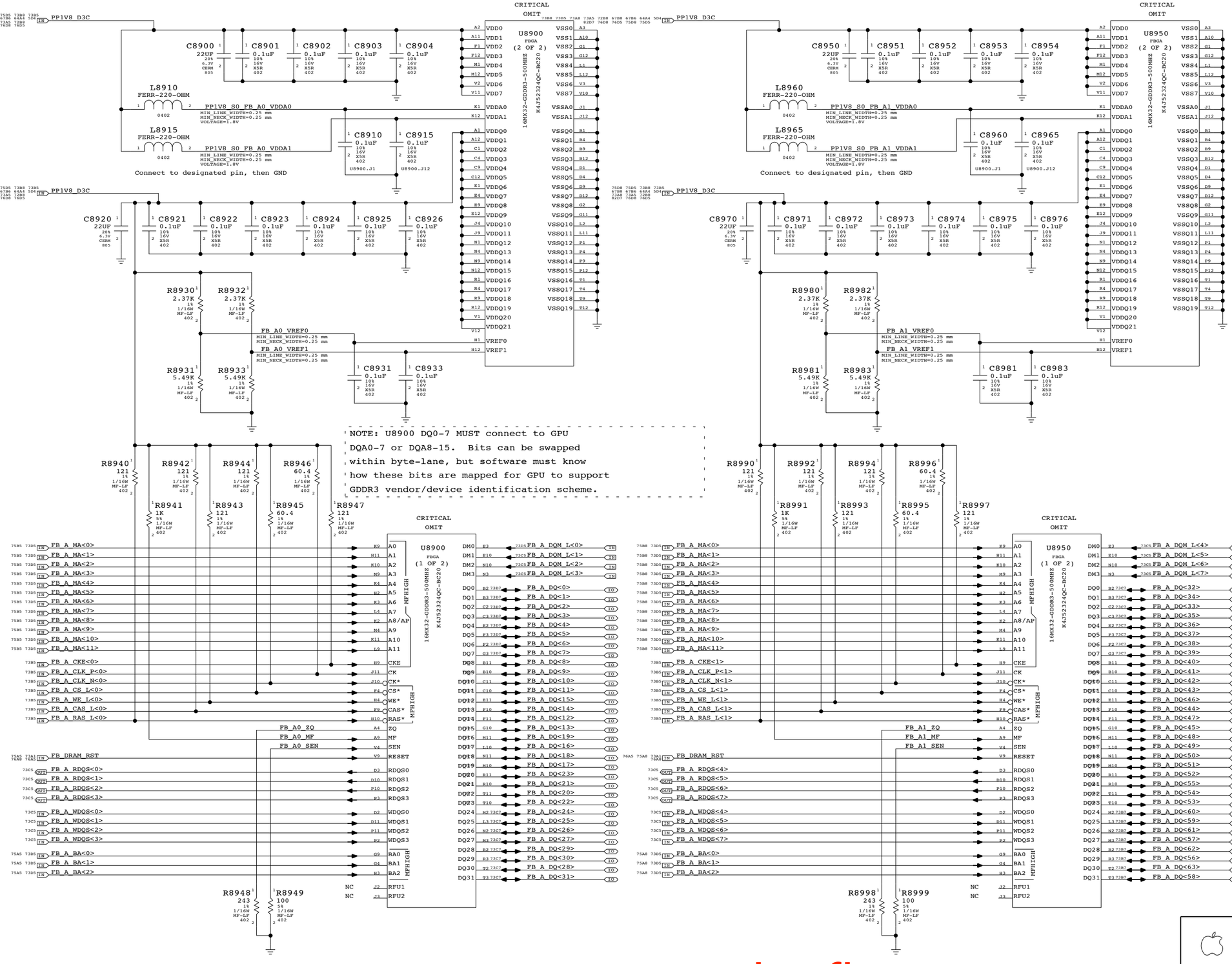
78A3 GPU_DDC_B_CLK
78A3 GPU_DDC_B_DATA

GPU Straps

SYNC_MASTER=M57_MLB_MG SYNC_DATE=08/08/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 74 OF 87	



Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

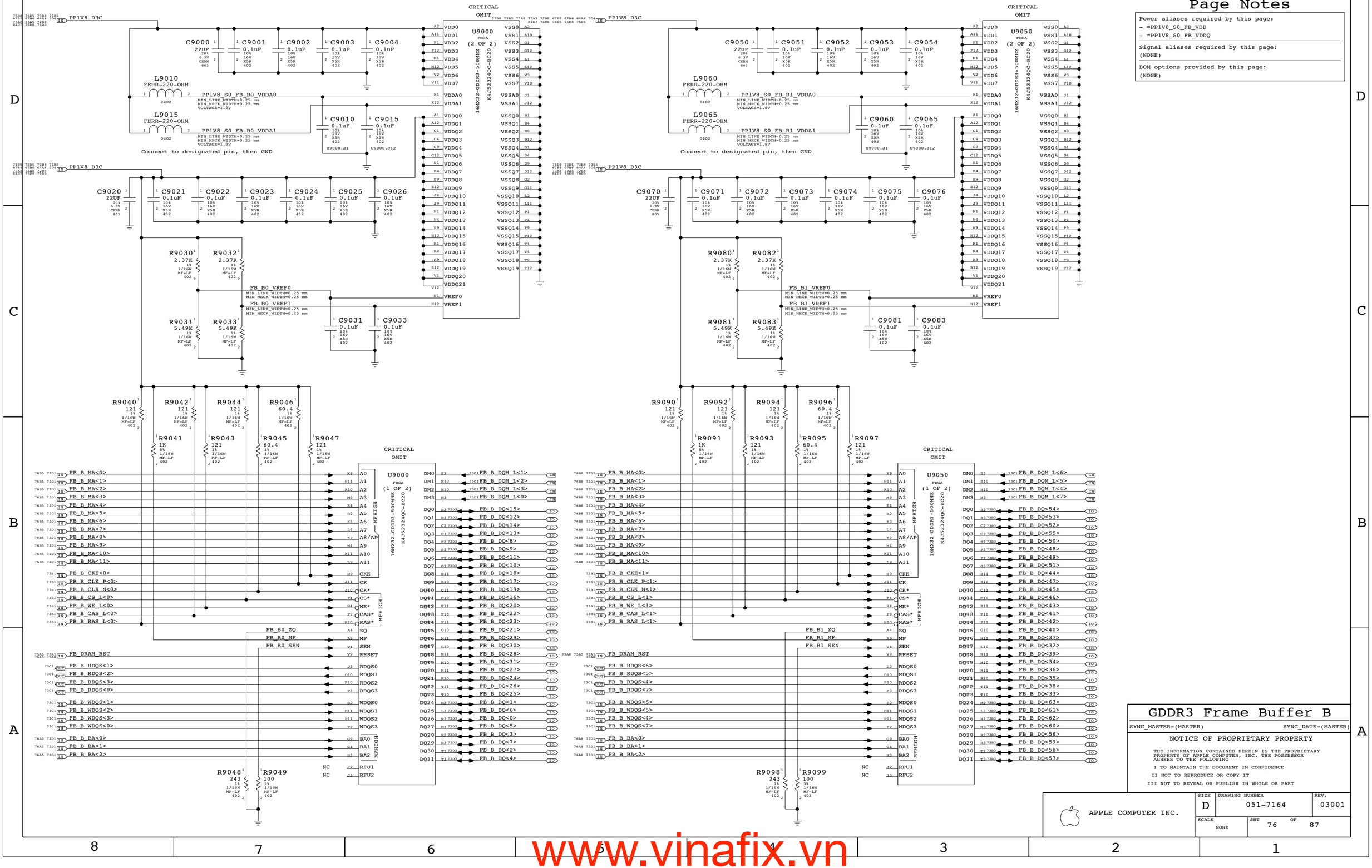
GDDR3 Frame Buffer A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	75	87

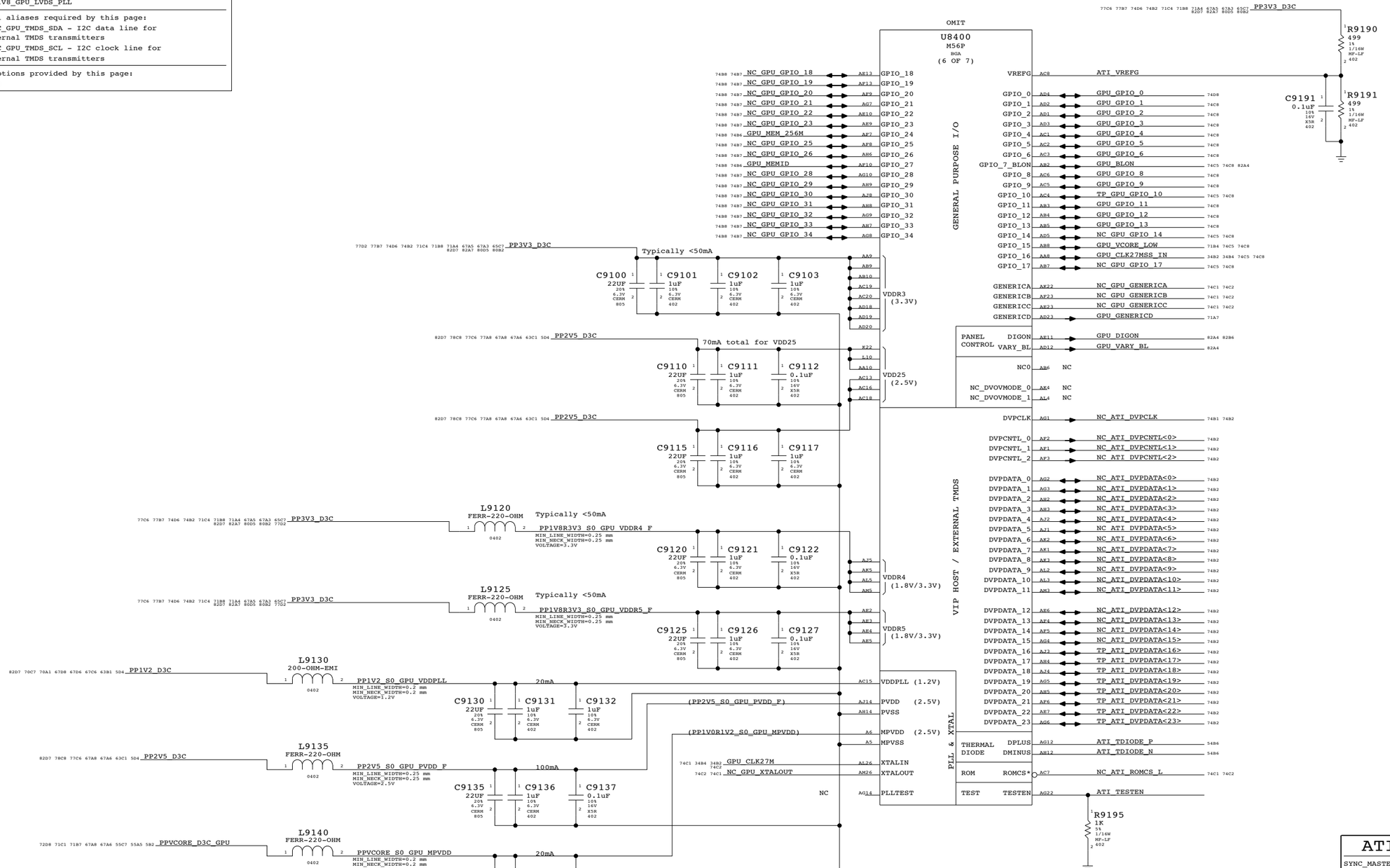


Page Notes

Power aliases required by this page:
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)



ATI M56 GPIO/DVO/Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE: NONE SHT 77 OF 87

Page Notes

Power aliases required by this page:
- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

82D7 77C6 77A8 67A8 67A6 63C1 5D4 PP2V5_D3C

Sum of peak currents on this page: 605mA

L9300 FERR-220-OHM 0402 — PP2V5_S0_GPU_TPVDD — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
C9300 22UF 20% 6.3V CERM 805; C9301 1uF 10% 6.3V CERM 402; C9302 1uF 10% 6.3V CERM 402

L9305 FERR-220-OHM 0402 — PP2V5_S0_GPU_TXVDDR — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 150mA peak
C9305 22UF 20% 6.3V CERM 805; C9306 1uF 10% 6.3V CERM 402; C9307 0.1uF 10% 16V X5R 402

L9310 FERR-220-OHM 0402 — PP2V5_S0_GPU_AVDD — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 65mA peak
C9310 22UF 20% 6.3V CERM 805; C9311 1uF 10% 6.3V CERM 402; C9312 0.1uF 10% 16V X5R 402

L9315 FERR-220-OHM 0402 — PP2V5_S0_GPU_VDD1DI — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
C9315 22UF 20% 6.3V CERM 805; C9316 1uF 10% 6.3V CERM 402; C9317 0.1uF 10% 16V X5R 402

L9320 FERR-220-OHM 0402 — PP2V5_S0_GPU_A2VDD — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 130mA peak
C9320 22UF 20% 6.3V CERM 805; C9321 1uF 10% 6.3V CERM 402; C9322 0.1uF 10% 16V X5R 402

L9325 FERR-220-OHM 0402 — PP2V5_S0_GPU_VDD2DI — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
C9325 22UF 20% 6.3V CERM 805; C9326 1uF 10% 6.3V CERM 402; C9327 0.1uF 10% 16V X5R 402

L9330 FERR-220-OHM 0402 — PP2V5_S0_GPU_LPVDD — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
C9330 22UF 20% 6.3V CERM 805; C9331 1uF 10% 6.3V CERM 402; C9332 1uF 10% 6.3V CERM 402

L9345 FERR-220-OHM 0402 — PP2V5_S0_GPU_LVDDR — MIN_LINE_WIDTH=0.35 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 200mA peak
C9340 22UF 20% 6.3V CERM 805; C9345 22UF 20% 6.3V CERM 805; C9341 1uF 10% 6.3V CERM 402; C9342 0.1uF 10% 16V X5R 402; C9346 0.1uF 10% 16V X5R 402; C9347 0.1uF 10% 16V X5R 402

OMIT

U8400 M56P BGA (5 OF 7)

INTEGRATED TMDS

AM8	TPVDD (2.5V)	
AL8	TPVSS	
AJ6, AK6, AL6, AM6	TXVDDR (2.5V)	
AJ7, AK7, AK8, AL7, AM7	TXVSSR	
AL25, AM25	AVDD (2.5V)	
AJ24, AK25	AVSS	
AK23	AVSSQ	
AM23	VDD1DI (2.5V)	
AL23	VSS1DI	
AL22	RSET	78A8 ATI_RSET
AL16, AM16	A2VDD (2.5V)	
AL17, AM17	A2VSS	
AL14	NC_A2VDDQ	NC
AK13	A2VSSQ	
AJ16	VDD2DI (2.5V)	
AJ17	VSS2DI	
AK14	R2SET	78A8 ATI_R2SET
AM19	LPVDD (2.5V)	
AM18	LPVSS	
AC21, AC22, AD21, AD22, AE20, AE21, AE22, AF19, AF20	LVDDR (2.5V)	
AF17, AF18, AF21, AF22, AG17, AG19, AH17, AH19, AJ19, AK17	LVSSR	
AF11	HPD1	80A2 GPU_HPD

DAC (CRT)

R	AK24	NC_GPU_VGA_R
G	AM24	NC_GPU_VGA_G
B	AL24	NC_GPU_VGA_B
HSYNC	AJ23	TP_GPU_VGA_HSYNC
VSYNC	AJ22	TP_GPU_VGA_VSYNC

DAC2 (TV/CRT2)

R2	AK15	GPU_R2
G2	AM15	GPU_G2
B2	AL15	GPU_B2
H2SYNC	AF15	GPU_H2SYNC
V2SYNC	AG15	GPU_V2SYNC
Y	AJ15	NC_GPU_TV_Y
C	AJ13	NC_GPU_TV_C
COMP	AH15	NC_GPU_TV_COMP

LVDS

TXCLK_UP	AJ21	LVDS_U_CLK_P
TXCLK_UN	AK21	LVDS_U_CLK_N
TXOUT_U0P	AG18	LVDS_U_DATA_P<0>
TXOUT_U0N	AH18	LVDS_U_DATA_N<0>
TXOUT_U1P	AK20	LVDS_U_DATA_P<1>
TXOUT_U1N	AJ20	LVDS_U_DATA_N<1>
TXOUT_U2P	AG20	LVDS_U_DATA_P<2>
TXOUT_U2N	AH20	LVDS_U_DATA_N<2>
TXOUT_U3P	AH21	NC_LVDS_U_DATAP<3>
TXOUT_U3N	AG21	NC_LVDS_U_DATAN<3>
TXCLK_LP	AM18	LVDS_L_CLK_P
TXCLK_LN	AL18	LVDS_L_CLK_N
TXOUT_L0P	AL19	LVDS_L_DATA_P<0>
TXOUT_L0N	AK19	LVDS_L_DATA_N<0>
TXOUT_L1P	AM20	LVDS_L_DATA_P<1>
TXOUT_L1N	AL20	LVDS_L_DATA_N<1>
TXOUT_L2P	AM21	LVDS_L_DATA_P<2>
TXOUT_L2N	AL21	LVDS_L_DATA_N<2>
TXOUT_L3P	AJ18	NC_LVDS_L_DATAP<3>
TXOUT_L3N	AK18	NC_LVDS_L_DATAN<3>

MONITOR IDENTIFICATION

DDC1CLK	AH23	GPU_DDC_A_CLK
DDC1DATA	AH22	GPU_DDC_A_DATA
DDC2CLK	AG13	GPU_DDC_B_CLK
DDC2DATA	AH13	GPU_DDC_B_DATA
DDC3CLK	AF12	GPU_DDC_C_CLK
DDC3DATA	AE12	GPU_DDC_C_DATA

Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb

ATI_RSET 78B5
ATI_R2SET 78B5

R9350 499 1% 1/16W MF-LF 402
R9351 715 1% 1/16W MF-LF 402

ATI M56 Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE: NONE SHT 78 OF 87

LCD (LVDS) INTERFACE

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
	VGA	VGA	GPU_R2
	VGA	VGA	GPU_G2
	VGA	VGA	GPU_B2
	LVDS	LVDS	LVDS_U_CLK_P
	LVDS	LVDS	LVDS_U_CLK_N
	LVDS	LVDS	LVDS_U_DATA_P<2..0>
	LVDS	LVDS	LVDS_U_DATA_N<2..0>
	LVDS	LVDS	LVDS_L_CLK_P
	LVDS	LVDS	LVDS_L_CLK_N
	LVDS	LVDS	LVDS_L_DATA_P<2..0>
	LVDS	LVDS	LVDS_L_DATA_N<2..0>
	LVDS	LVDS	LVDS_U_CLK_CONN_P
	LVDS	LVDS	LVDS_U_CLK_CONN_N
	LVDS	LVDS	LVDS_U_DATA_CONN_P<2..0>
	LVDS	LVDS	LVDS_U_DATA_CONN_N<2..0>
	LVDS	LVDS	LVDS_L_CLK_CONN_P
	LVDS	LVDS	LVDS_L_CLK_CONN_N
	LVDS	LVDS	LVDS_L_DATA_CONN_P<2..0>
	LVDS	LVDS	LVDS_L_DATA_CONN_N<2..0>
	TMDS	TMDS	TMDS_CLK_P
	TMDS	TMDS	TMDS_CLK_N
	TMDS	TMDS	TMDS_DATA_P<5..3>
	TMDS	TMDS	TMDS_DATA_N<5..3>
	TMDS	TMDS	TMDS_DATA_P<2..0>
	TMDS	TMDS	TMDS_DATA_N<2..0>

PP3V3_S5

R9400 100K 5% 1/16W MF-LF 402

C9400 0.0022uF 10% 50V CERM 402

R9401 100K 5% 1/16W MF-LF 402

LCD_PWREN_L_RC

Q9400 SI3443DV TSOP-LF

PP3V3_LCD_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

L9400 FERR-250-OHM SM

C9401 0.001uF 20% 50V CERM 402

GND_CHASSIS_LVDS

LCD_PWREN_L

Q9401 2N7002 SOT23-LF

LVDS_PANEL_EN

R9494 100K 5% 1/16W MF-LF 402

PP3V3_S0

100K pull-ups are for no-panel case (development). Panel has 2K pull-ups

R9410 100K 5% 1/16W MF-LF 402

R9411 100K 5% 1/16W MF-LF 402

LVDS_CONN_DDC_CLK

LVDS_CONN_DDC_DATA

C9410 0.001uF 20% 50V CERM 402

GND_CHASSIS_LVDS

CRITICAL
J9400 MSC-RB30-5-FA F-RT-SM

C9420 0.001uF 20% 50V CERM 402

GND_CHASSIS_LVDS

PP3V3_LCD_CONN
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

NC

LVDS_L_DATA_CONN_N<0>
LVDS_L_DATA_CONN_P<0>
LVDS_L_DATA_CONN_N<1>
LVDS_L_DATA_CONN_P<1>
LVDS_L_DATA_CONN_N<2>
LVDS_L_DATA_CONN_P<2>
LVDS_L_CLK_CONN_N
LVDS_L_CLK_CONN_P
LVDS_U_DATA_CONN_N<0>
LVDS_U_DATA_CONN_P<0>
LVDS_U_DATA_CONN_N<1>
LVDS_U_DATA_CONN_P<1>
LVDS_U_DATA_CONN_N<2>
LVDS_U_DATA_CONN_P<2>
LVDS_U_CLK_CONN_N
LVDS_U_CLK_CONN_P

C9421 0.001uF 20% 50V CERM 402

GND_CHASSIS_LVDS

518S0289

INVERTER INTERFACE

CRITICAL
L9450 FERR-220-OHM-2A 0603

PPBUS_G3H

PPBUS_S0_INVERTER
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.8V

C9450 0.001uF 20% 50V CERM 402

PP5V_S0

Q9450 FDG6332C_NL SC70-6 P-CHN

R9450 100K 5% 1/16W MF-LF 402

PP5V_INVERTER_SW_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

L9452 400-OHM-EMI SM-1

C9451 10UF 20% 6.3V X5R 603

FP_PWR_EN_L

Q9450 FDG6332C_NL SC70-6 N-CHN

INVERTER_BKLTON

R9489 100K 5% 1/16W MF-LF 402

PP5V_INVERTER_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

C9452 0.001uF 20% 50V CERM 402

L9454 400-OHM-EMI SM-1

INVERTER_PWM

GND_CHASSIS_INVERTER

C9454 0.001uF 20% 50V CERM 402

CRITICAL
J9450 SM04B-ACH M-RT-SM

NC

518S0369

CRITICAL
L9455 FERR-220-OHM-2A 0603

PP3V3_S0

PLT_RST_L

INVERTER_PWM_UNBUF

U9453 MC74VHC1G08 SC70

INVERTER_PWM_F

INVERTER EXPECTS ACTIVE HIGH PWM SIGNAL

C9453 0.1uF 20% 10V CERM 402

GND_CHASSIS_INVERTER

Internal Display Connectors

SYNC_MASTER=M57_MLB_MG SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 79 OF 87	

TMDS Filtering

Place termination components close to GPU, common mode chokes near connector.

TMDS_DATA_N<0> — TMDS_DATA_RL<0> (VOLTAGE=0V, NO_TEST=TRUE) — R9762 182 1% 1/16W MF-LF 402 — L9743 47nH 0402 — TMDS_DATA_P<0>

CRITICAL L9700 90-OHM-100MA 1210-4SM1 (SYM_VER=1)
TMDS_DATA_F_N<0> — TMDS_DATA_F_P<0>

TMDS_DATA_N<1> — TMDS_DATA_RL<1> (VOLTAGE=0V, NO_TEST=TRUE) — R9766 182 1% 1/16W MF-LF 402 — L9744 47nH 0402 — TMDS_DATA_P<1>

CRITICAL L9701 90-OHM-100MA 1210-4SM1 (SYM_VER=1)
TMDS_DATA_F_N<1> — TMDS_DATA_F_P<1>

TMDS_DATA_N<2> — TMDS_DATA_RL<2> (VOLTAGE=0V, NO_TEST=TRUE) — R9770 182 1% 1/16W MF-LF 402 — L9745 47nH 0402 — TMDS_DATA_P<2>

CRITICAL L9702 90-OHM-100MA 1210-4SM1 (SYM_VER=1)
TMDS_DATA_F_N<2> — TMDS_DATA_F_P<2>

TMDS_CLK_N — R9772 0 5% 1/16W MF-LF 402 — TMDS_CLK_R_N
TMDS_CLK_P — R9774 182 1% 1/16W MF-LF 402 — R9773 0 5% 1/16W MF-LF 402 — TMDS_CLK_R_P

CRITICAL L9706 370-OHM 8M (SYM_VER=1)
TMDS_CLK_F_N — TMDS_CLK_F_P

TMDS_DATA_N<3> — TMDS_DATA_RL<3> (VOLTAGE=0V, NO_TEST=TRUE) — R9778 182 1% 1/16W MF-LF 402 — L9746 47nH 0402 — TMDS_DATA_P<3>

CRITICAL L9703 90-OHM-100MA 1210-4SM1 (SYM_VER=1)
TMDS_DATA_F_N<3> — TMDS_DATA_F_P<3>

TMDS_DATA_N<4> — TMDS_DATA_RL<4> (VOLTAGE=0V, NO_TEST=TRUE) — R9782 182 1% 1/16W MF-LF 402 — L9747 47nH 0402 — TMDS_DATA_P<4>

CRITICAL L9704 90-OHM-100MA 1210-4SM1 (SYM_VER=1)
TMDS_DATA_F_N<4> — TMDS_DATA_F_P<4>

TMDS_DATA_N<5> — TMDS_DATA_RL<5> (VOLTAGE=0V, NO_TEST=TRUE) — R9786 182 1% 1/16W MF-LF 402 — L9748 47nH 0402 — TMDS_DATA_P<5>

CRITICAL L9705 90-OHM-100MA 1210-4SM1 (SYM_VER=1)
TMDS_DATA_F_N<5> — TMDS_DATA_F_P<5>

VGA SYNC BUFFERS

PP3V3_D3C — U9750 (MC74VHC1G08 SC70) — GPU_V2SYNC
C9750 0.1uF 20% 10V CERM 402
VGA_VSYNC_R — R9750 33 5% 1/16W MF-LF 402 — VGA_VSYNC

PLACE U9750 & U9751 CLOSE TO DVI CONNECTOR

PP3V3_D3C — U9751 (MC74VHC1G08 SC70) — GPU_H2SYNC
C9751 0.1uF 20% 10V CERM 402
VGA_HSYNC_R — R9751 33 5% 1/16W MF-LF 402 — VGA_HSYNC

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

GPU_B2 (DAC2 Comp) — R9740 75 1% 1/16W MF-LF 402 — CRITICAL FL9740 LCFILTER SM-220MHZ-LF — VGA_B — C9740 3.3pF 0.25% 50V CERM 402
GPU_G2 (DAC2 Y) — R9741 75 1% 1/16W MF-LF 402 — CRITICAL FL9741 LCFILTER SM-220MHZ-LF — VGA_G — C9741 3.3pF 0.25% 50V CERM 402
GPU_R2 (DAC2 C) — R9742 75 1% 1/16W MF-LF 402 — CRITICAL FL9742 LCFILTER SM-220MHZ-LF — VGA_R — C9742 3.3pF 0.25% 50V CERM 402

DVI INTERFACE

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)

PP5V_S0 — CRITICAL F9710 0.5AMP-13.2V SM-LF — PP5V_S0_DDC_F — L9710 400-OHM-EMI SM-1 — PP5V_S0_DDC
VOLTAGE=5V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm

CRITICAL J9700 QH11121-RIG02-4F F-RT-TH-DVI

GND_CHASSIS_DVI_BOT		
TMDS_DATA_F_N<0>	TMDS_DATA_F_N<2>	
TMDS_DATA_F_P<0>	TMDS_DATA_F_N<1>	
	TMDS_DATA_F_P<2>	
	TMDS_DATA_F_P<1>	
TMDS_DATA_F_N<5>	TMDS_DATA_F_N<4>	
TMDS_DATA_F_P<5>	TMDS_DATA_F_N<3>	
	TMDS_DATA_F_P<4>	
	TMDS_DATA_F_P<3>	
TMDS_CLK_F_P	DVI_DDC_CLK_R	
	(PP5V_S0_DDC)	
TMDS_CLK_F_N	DVI_DDC_DATA_R	
	VGA_VSYNC	
	DVI_HPD_R	
VGA_B	VGA_R	
VGA_HSYNC	VGA_G	
GND_CHASSIS_DVI_TOP		

514-0278

PLACE NEAR C5A & C5B
R9730 0 5% 1/16W MF-LF 402
C9710 0.01uF 20% 50V CERM 603
C9714 100pF 5% 50V CERM 402
GND_CHASSIS_DVI_BOT — GND

R9731 0 5% 1/16W MF-LF 402 — GND_CHASSIS_DVI_TOP
PLACE NEAR 3, 11 & 19

Isolation required for DVI power switch

D9710 SOD-123 B0530WXF
PP5V_S0_DDC_PULLUPS (VOLTAGE=5V, MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm)
R9710 4.7K 5% 1/16W MF-LF 402 — DVI_DDC_CLK
R9712 4.7K 5% 1/16W MF-LF 402 — DVI_DDC_DATA
C9711 100pF 5% 50V CERM 402

3V LEVEL SHIFTERS

PP3V3_D3C
R9711 100 5% 1/16W MF-LF 402 — DVI_DDC_CLK — Q9711 2N7002DW-X-F SOT-363 — R9720 10K 5% 1/16W MF-LF 402 — GPU_DDC_A_CLK
R9713 100 5% 1/16W MF-LF 402 — DVI_DDC_DATA — Q9711 2N7002DW-X-F SOT-363 — R9721 10K 5% 1/16W MF-LF 402 — GPU_DDC_A_DATA
C9713 100pF 5% 50V CERM 402
GPU_SIGNAL_ENABLE
R9714 100 5% 1/16W MF-LF 402 — DVI_HPD — Q9714 2N7002DW-X-F SOT-363 — Q9714 2N7002DW-X-F SOT-363 — R9722 270K 5% 1/16W MF-LF 402 — GPU_HPD_R
GPU_HPD_BILAT
PP5V_S0 — R9723 270K 5% 1/16W MF-LF 402 — Q9715 2N7002DW-X-F SOT-363 — SB_DVI_HPD — SB_DVI_HPD
MAKE_BASE=TRUE
R9715 20K 5% 1/16W MF-LF 402
R9724 0 5% 1/16W MF-LF 402 — GPU_HPD_R — GPU_HPD

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	
	TMDS	TMDS	TMDS_CLK_R_P
	TMDS	TMDS	TMDS_CLK_R_N
	TMDSCONN	TMDSCONN	TMDS_CLK_F_P
	TMDSCONN	TMDSCONN	TMDS_CLK_F_N
	TMDSCONN	TMDSCONN	TMDS_DATA_F_P<5..0>
	TMDSCONN	TMDSCONN	TMDS_DATA_F_N<5..0>

External Display Connector

SYNC_MASTER=M57_MLB_MG — SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

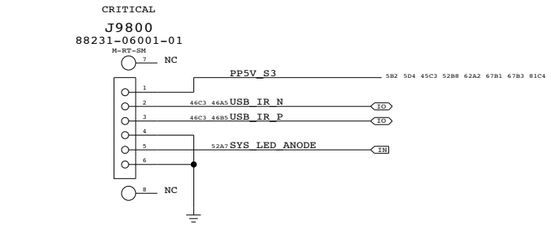
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

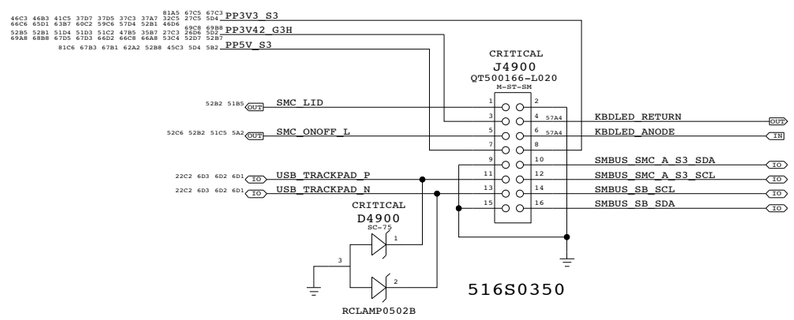
SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 80 OF 87	

IR & Sleep LED Connector



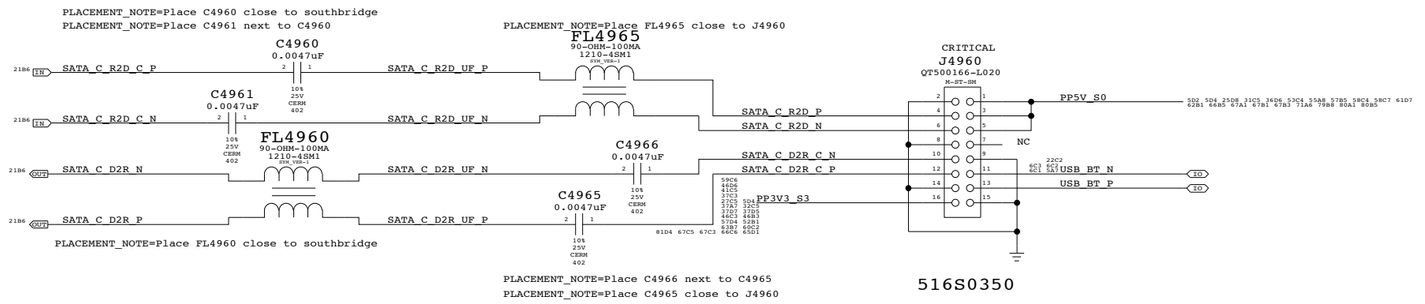
518S0474

Top-Case Connector



516S0350

Bluetooth (M13P) & SATA HDD Flex Connector



516S0350

M57 SPECIFIC CONNECTORS

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 81 OF 87	

LVDS Interface Pull-downs

NOTE: These parts are to counter an invalid state caused by the M56 part. Bias voltage is present on LVDS interface pins even when they should be tri-stated to meet panel power sequence requirements. Resulting pump-up in LCD panel can cause startup and long-term reliability issues. Pull-down resistors reduce the pump-up in the panel, though some voltage will still be seen on LVDS signals when they should be 0V.

LVDS_L_DATA_P<0>
LVDS_L_DATA_N<0>
LVDS_L_CLK_N
LVDS_L_CLK_P
=LVDS_PD_L_DATA_P<2>
=LVDS_PD_L_DATA_N<2>
=LVDS_PD_L_CLK_P
=LVDS_PD_L_CLK_N
LVDS_U_DATA_N<0>
LVDS_U_DATA_P<0>
=LVDS_PD_U_DATA_P<1>
=LVDS_PD_U_DATA_N<1>
LVDS_U_CLK_N
LVDS_U_CLK_P
=LVDS_PD_U_CLK_P
=LVDS_PD_U_CLK_N

LVDS_PD RP9900 8.2K
LVDS_PD RP9901 8.2K
LVDS_PD RP9902 8.2K
LVDS_PD RP9903 8.2K

5% 1/16W 8M-LF

PGOOD Monitor for GPU Rails

PP3V3_D3C
PP2V5_D3C
PP1V8_D3C
PP1V2_D3C

R9994 124K 1% 1/16W MF-LF 402
R9992 237K 1% 1/16W MF-LF 402
R9990 365K 1% 1/16W MF-LF 402

C9990 0.1uF 20% 10V CERM 402

U9990 LTC2903 TSOT-23
CRITICAL
V1 V2 V3 V4 RST* GND
D3CPGOOD_2V5_DIV
D3CPGOOD_1V8_DIV
D3CPGOOD_1V2_DIV
D3CPGOOD_PWROK

R9997 10K 5% 1/16W MF-LF 402

C9991 0.1uF 20% 10V CERM 402

PP3V3_S0

U9991 MC74VHC1G08 SC70
S0PGOOD_PWROK
S0D3CPGOOD_PWROK

R9995 100K 1% 1/16W MF-LF 402
R9993 100K 1% 1/16W MF-LF 402
R9991 100K 1% 1/16W MF-LF 402
R9996 470K 5% 1/16W MF-LF 402

C9995 0.1UF 20% 10V CERM 402
C9993 0.1UF 20% 10V CERM 402
C9992 0.1UF 20% 10V CERM 402

LTC2903 guaranteed threshold is 93.5% (3.055V, 2.325V, 1.685V, 1.120V)

LVDS Mux Selection Qualification

Enables the GPU LVDS path in the mux with the qualification that the GPU has turned on panel power and that the panel power has risen to (near) 3.3V. This should eliminate need for LVDS pulldowns

PP3V3_S0
PP2V5_S0

C9985 0.1UF 20% 10V CERM 402
C9980 0.1UF 20% 10V CERM 402

U9985 MC74VHC1G08 SC70
GPU_DIGON
LVDS_MUX_SEL_GPU
GPU_DIGON_AND_SELECTED

U9980 SN74LVC1G132 SC70-5
CRITICAL

R9980 10K 5% 1/16W MF-LF 402
R9981 13.3K 1% 1/16W MF-LF 402
PP3V3_LCD_SW
PANEL_PWR_ON

Divider set to rise to 1.88V nom/1.74V min when panel power is at 3.3V/3.315V. Schmitt trigger voltage max is 1.70V (@2.625V Vcc). R9981 can also be used as pad for cap, creating an RC filter.

GPU DDC Pass FETs

GPU_SIGNAL_ENABLE
PP3V3_D3C

R9970 15.8K 1% 1/16W MF-LF 402
R9971 15.8K 1% 1/16W MF-LF 402

Q9970 2N7002DW-X-F SOT-363

GPU_DDC_C_CLK
GPU_DDC_C_DATA
LVDS_CONN_DDC_CLK MAKE_BASE=TRUE
LVDS_CONN_DDC_DATA MAKE_BASE=TRUE

LVDS I/F Mux

PP2V5_S0

C9950 0.1UF 20% 10V CERM 402

U9950 CBTV4020 BGA-LF
CRITICAL
VDD GND

NB LVDS I/F

LVDS_B_DATA_N<2>
LVDS_B_DATA_N<0>
LVDS_B_DATA_P<0>
LVDS_A_CLK_P
LVDS_A_CLK_N
LVDS_A_DATA_N<0>
LVDS_A_DATA_P<0>
LVDS_A_DATA_P<2>
LVDS_A_DATA_N<2>
LVDS_A_DATA_N<1>
LVDS_A_DATA_P<1>
LVDS_B_DATA_P<1>
LVDS_B_DATA_N<1>
LVDS_B_CLK_N
LVDS_B_CLK_P
LVDS_B_DATA_P<2>

GPU LVDS I/F

LVDS_U_DATA_N<2>
LVDS_U_DATA_N<0>
LVDS_U_DATA_P<0>
LVDS_L_CLK_P
LVDS_L_CLK_N
LVDS_L_DATA_N<0>
LVDS_L_DATA_P<0>
LVDS_L_DATA_P<2>
LVDS_L_DATA_N<2>
LVDS_L_DATA_N<1>
LVDS_L_DATA_P<1>
LVDS_U_DATA_P<1>
LVDS_U_DATA_N<1>
LVDS_U_CLK_N
LVDS_U_CLK_P
LVDS_U_DATA_P<2>

DH0 LVDS_U_DATA_CONN_N<2>
DH1 LVDS_U_DATA_CONN_N<0>
DH2 LVDS_U_DATA_CONN_P<0>
DH3 NC
DH4 LVDS_L_CLK_CONN_P
DH5 LVDS_L_CLK_CONN_N
DH6 NC
DH7 LVDS_L_DATA_CONN_N<0>
DH8 LVDS_L_DATA_CONN_P<0>
DH9 LVDS_L_DATA_CONN_P<2>
DH10 LVDS_L_DATA_CONN_N<2>
DH11 LVDS_L_DATA_CONN_N<1>
DH12 LVDS_L_DATA_CONN_P<1>
DH13 NC
DH14 LVDS_U_DATA_CONN_P<1>
DH15 LVDS_U_DATA_CONN_N<1>
DH16 NC
DH17 LVDS_U_CLK_CONN_N
DH18 LVDS_U_CLK_CONN_P
DH19 LVDS_U_DATA_CONN_P<2>

SEL LVDS_MUX_SEL_GPU_L

NOTE: SEL = LOW selects port B

Panel/Backlight Control Mux

PP3V3_S0

C9960 0.1UF 20% 10V CERM 402

U9960 74CBTLV3257 QFN
CRITICAL
VCC GND THRML PAD

LVDS_VDDEN
GPU_DIGON
LVDS_BKLTEN
GPU_BLON
LVDS_BKLTCTL
GPU_VARY_BL
S0PGOOD_PWROK
S0D3CPGOOD_PWROK

LVDS_PANEL_EN
INVERTER_BKLTON
INVERTER_PWM_UNBUF
PGOOD_MUXED_S0_OR_S0D3C

LVDS_MUX_SEL_GPU_MUXED
NOTE: S = HIGH selects xB2

R9961 100K 5% 1/16W MF-LF 402
R9960 10K 5% 1/16W MF-LF 402

C9961 0.1UF 20% 10V CERM 402

U9961 MC74VHC1G08 SC70
PLT_RST_L
LVDS_MUX_SEL_GPU

NO STUFF
R9962 0 5% 1/16W MF-LF 402

LVDS_MUX_SEL_GPU MAKE_BASE=TRUE

NOTE: SB_GPIO23 has internal 20K PU to default selection to GPU

LVDS Interface Pull-downs

SYNC_MASTER=M57_MLB_MG
SYNC_DATE=08/08/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 82 OF 87	

Revision History

Revision History

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	83	87

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	?
FSB_ADDR2ADDR	*	=2:1_SPACING	?
FSB_ADSTB	*	=3:1_SPACING	?
FSB_ADDR2ADSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=3:1_SPACING	?
FSB_DATA2DATA	*	=2:1_SPACING	?
FSB_DSTB	*	=3:1_SPACING	?
FSB_DATA2DSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 3:1, even in constraint areas.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2TO1	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.4, 4.6.2, & 5.8.2.4

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	Y	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	Y	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Need to support MEM_*-style wildcards!

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 6.2

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
DMI	*	20 MIL	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 7.2, 9.2 & 10.5.2

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 10.6 & 10.7.2

Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIO_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB2_90D	*	Y	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2	*	=4:1_SPACING	?
USB2_2CLK	*	25 MIL	DG says minimum spacing 50 mils to clocks

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.10.1.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.17.1.1

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

Napa Platform Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	84	87

GDDR3 (Frame Buffer) Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FB_35S_TO_55S	*	Y	=35_OHM_SE	=55_OHM_SE	=35_55_OHM_SE	=STANDARD	=STANDARD
FB_40S	*	Y	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
FB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FB_75D	*	Y	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FB_ADCTRL	*	=2.5:1_SPACING	?
FB_CLK	*	=2.5:1_SPACING	?
FB_DATA	*	=2.5:1_SPACING	?

ADDR/CTRL lines should route 35-ohms to T, then 55-ohms to each VRAM device.
CTRL lines are 55-ohm single-ended impedence.
DQ/DQM/DQS lines are 40-ohm single-ended impedence.

NOTE: CLK lines are specified in Layout Guide as 40-ohm single-ended. We treat as 75-ohm differential.
NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TMDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_75S	*	Y	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS	*	=3:1_SPACING	?
TMDS	*	=3:1_SPACING	?
VGA	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS_PAIR2PAIR	*	25 MIL	?
TMDS_PAIR2PAIR	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	LVDS	*	LVDS_PAIR2PAIR
TMDS	TMDS	*	TMDS_PAIR2PAIR

LVDS and TMDS signals are 100-ohm +/- 10% differential impedence.
LVDS and TMDS pairs should be kept at least 25 mils apart.
Ground shields can be used around each pair if spacing cannot be met.
VGA should be routed as close to 75-ohms single-ended impedence as possible.
VGA signals should be kept at least 15 mils from other traces.
Ground shields recommended around VGA signals.

NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

High-Speed I/O Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
FW_110D	*	Y	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET	*	=3:1_SPACING	?
FW	*	=3:1_SPACING	?

note

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?

More System Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE: NONE SHT 85 OF 87

M9 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.100 MM	0.100 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.124 MM	0.124 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.150 MM	0.150 MM			
45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.185 MM			
40_OHM_SE	*	Y	0.131 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.230 MM	0.230 MM			
35_OHM_SE	*	Y	0.165 MM	0.165 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.335 MM	0.335 MM			
27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_55_OHM_SE	TOP,BOTTOM	Y	0.230 MM	0.100 MM			
35_55_OHM_SE	*	Y	0.165 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

Unsupported rule

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	0.149 MM	0.149 MM	=STANDARD	0.125 MM	0.125 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_DIFF	*	Y	0.131 MM	0.131 MM	=STANDARD	0.125 MM	0.125 MM
75_OHM_DIFF	TOP,BOTTOM	Y	0.161 MM	0.161 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.115 MM	0.111 MM	=STANDARD	0.125 MM	0.125 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.101 MM	0.101 MM	=STANDARD	0.125 MM	0.125 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.102 MM	0.102 MM	=STANDARD	0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.080 MM	0.080 MM	=STANDARD	0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	Y	0.077 MM	0.077 MM	=STANDARD	0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FB_CLK	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

Allow 0.1 MM on blind-to-buried via dogbones (layers 2 & 11)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	ISL2,ISL11	0.1 MM	?
1.8:1_SPACING	ISL2,ISL11	0.1 MM	?
2:1_SPACING	ISL2,ISL11	0.1 MM	?
2.5:1_SPACING	ISL2,ISL11	0.1 MM	?
3:1_SPACING	ISL2,ISL11	0.1 MM	?
4:1_SPACING	ISL2,ISL11	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	ISL2,ISL11	0.1 MM	?
CLK_PCIE	ISL2,ISL11	0.1 MM	?
CLK_MED	ISL2,ISL11	0.1 MM	?
CLK_SLOW	ISL2,ISL11	0.1 MM	?
CPU_COMP	ISL2,ISL11	0.1 MM	?
CPU_GTLREF	ISL2,ISL11	0.1 MM	?
CPU_VCCSENSE	ISL2,ISL11	0.1 MM	?
DMI	ISL2,ISL11	0.1 MM	?
LVDS_PAIR2PAIR	ISL2,ISL11	0.1 MM	?
MEM_2OTHER	ISL2,ISL11	0.1 MM	?
PCIE	ISL2,ISL11	0.1 MM	?
SATA	ISL2,ISL11	0.1 MM	?
TMDS_PAIR2PAIR	ISL2,ISL11	0.1 MM	?
VGA	ISL2,ISL11	0.1 MM	?

Rules for "Topology #3" for FSB signals, Napa DG tables 4-7 & 4-12.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_ADDR2ADDR OVERRIDE	* OVERRIDE	=STANDARD OVERRIDE	? OVERRIDE
FSB_ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_ADDR2ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_DATA2DATA OVERRIDE	* OVERRIDE	=STANDARD OVERRIDE	? OVERRIDE
FSB_DSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_DATA2DSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS	*	LVDS_100D
TMDS	*	TMDS_100D
TMDSCONN	*	TMDS_100D
VGA	*	VGA_75S

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_2OTHER OVERRIDE	* OVERRIDE	0.5 MM OVERRIDE	? OVERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI_2PCI OVERRIDE	* OVERRIDE	0.1 MM OVERRIDE	? OVERRIDE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCI	PCI	*	PCI_2PCI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENETCONN	*	*	ENET
TMDSCONN	*	*	TMDS

"Stale" physical / spacing types

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ANALOG	*	*	FSB_COMMON
FSB_P2MM	*	*	FSB_COMMON
I2C	*	*	SMB
GND	*	*	STANDARD
MEM_PP1V8_S3	*	*	STANDARD
FB_PP1V8	*	*	STANDARD

FSB_ANALOG
FSB_P2MM
I2C
GND
MEM_PP1V8_S3
FB_PP1V8
PCI PCI_5SE

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

M9 Spacing & Physical Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 86 OF 87	

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
	FSB_55S	FSB_COMMON	FSB_ADS_L	5B7 7D6 12C4
	FSB_55S	FSB_COMMON	FSB_BNR_L	5B7 7D6 12C4
	FSB_55S	FSB_COMMON	FSB_BPRI_L	7D6 12C4
	FSB_55S	FSB_COMMON	FSB_BREQ0_L	5B7 7D6 12C4
	FSB_55S	FSB_COMMON	FSB_DBSY_L	5B7 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_DEFER_L	7D6 12B4
	FSB_55S	FSB_COMMON	FSB_DPWR_L	5A4 7B3 12B4
	FSB_55S	FSB_COMMON	FSB_DRDY_L	5B7 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_HIT_L	5B7 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_HITM_L	5B7 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_LOCK_L	5A7 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	7D6 12A4
	FSB_55S	FSB_COMMON	FSB_TRDY_L	7D6 12A4
	FSB_55S	FSB_COMMON	FSB_CPURST_L	5A4 7D6 11B5 12C4
	FSB_55S	FSB_DATA	FSB_D_L<63..0>	5B7 7B3 7B4 7C3 7C4 12B6 12C6 12D6
	FSB_55S	FSB_DATA	FSB_DINV_L<3..0>	5B7 7B3 7B4 7C3 7C4 12B4
	FSB_55S	FSB_DSTB	FSB_DSTBP_L<3..0>	5B7 7B3 7B4 7C3 7C4 12B4
	FSB_55S	FSB_DSTB	FSB_DSTBN_L<3..0>	5B7 7B3 7B4 7C3 7C4 12B4
	FSB_55S	FSB_ADDR	FSB_A_L<31..3>	5B7 7C8 7D8 12C4 12D4
	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	5A7 7D8 12A4 12B4
	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<3..0>	5B7 7C8 7D8 12C4
	CPU_55S		FSB_IERR_L	7D6
	CPU_55S		FSB_FERR_L	
	CPU_55S		CPU_PWRGD	5B4 7B3 21C4
	CPU_55S		CPU_INTR	7C8 21C4
	CPU_55S		CPU_NMI	7C8 21C4
	CPU_55S		CPU_A20M_L	7C8 21C4
	CPU_55S		CPU_DPSLP_L	5B4 7B3 21C4
	CPU_55S		CPU_IGNNE_L	7C8 21C4
	CPU_55S		CPU_INIT_L	7D6 21C4
	CPU_55S		CPU_SMI_L	7C8 21C4
	CPU_55S		CPU_STPCLK_L	5C4 7C8 21C4
	CPU_55S	CPU_2TO1	CPU_THERMTRIP_L	
	CPU_55S	CPU_2TO1	PM_DPRSLPVR	5B4 14B7 23C3 61C8
	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	5C4 61C7
	CPU_55S	CPU_GTLREF	CPU_GTLREF	7B4
	CPU_55S	CPU_COMP	CPU_COMP<3>	7B3
	CPU_27P4S	CPU_COMP	CPU_COMP<2>	7B3
	CPU_55S	CPU_COMP	CPU_COMP<1>	7B3
	CPU_27P4S	CPU_COMP	CPU_COMP<0>	7B3
	CPU_55S	CPU_ITP	XDP_BPM_L<5..0>	7C6 11B3
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_P	11B3 33C4 34D3 34D5
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_N	11B3 33C4 34D3 34D5
	CPU_55S	CPU_ITP	ITPRESET_L	11B3
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8B7 9C2 87B6
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8B7 9C2 87B6
THERM	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8B6 61B1
THERM	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	8B6 61A1
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	61A3
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	61A3

MEM_CLK	MEM_76D
MEM_CTRL	MEM_45S
MEM_CMD	MEM_55S
MEM_DATA	MEM_55S
MEM_DQS	MEM_85D
FB_CLK	FB_75D
FB_ADCTRL	FB_35S_TO_55S
FB_ADCTRL	FB_55S
FB_DATA	FB_40S
LVDS	LVDS_100D
TMDS	TMDS_100D
VGA	VGA_75S
PCIE	PCIE_100D
DMI	DMI_100D
SATA	SATA_100D
IDE	IDE_55S
USB2	USB2_90D
ENET	ENET_100D
FW	FW_110D
SMB	SMB_55S
SPI	SPI_55S
CLK_FSB	CLK_FSB_100D
CLK_PCIE	CLK_PCIE_100D
CLK_MED	CLK_MED_55S
CLK_SLOW	CLK_SLOW_55S

AUDIO_55S	AUDIO	SB_ACZ_BITCLK	21C6
AUDIO_55S	AUDIO	ACZ_BITCLK	5C1 21C7 48B3
AUDIO_55S	AUDIO	SB_ACZ_SYNC	21C6
AUDIO_55S	AUDIO	ACZ_SYNC	5C1 21C7 48B3
AUDIO_55S	AUDIO	SB_ACZ_RST_L	21C6
AUDIO_55S	AUDIO	ACZ_RST_L	5C1 21C7 48B3
AUDIO_55S	AUDIO	ACZ_SDATAIN<0>	5C1 21C7 48B3
AUDIO_55S	AUDIO	SB_ACZ_SDATAOUT	21C6
AUDIO_55S	AUDIO	ACZ_SDATAOUT	5C1 21C7 48B3

TMDS	TMDS	TMDS_CLK_P	78C3 79C7 80B8
TMDS	TMDS	TMDS_CLK_N	78C3 79C7 80C8
TMDS	TMDS	TMDS_DATA_P<5..3>	78C3 79C7 80A8 80B8
TMDS	TMDS	TMDS_DATA_N<5..3>	78C3 79C7 80A8 80B8
TMDS	TMDS	TMDS_DATA_P<2..0>	78C3 79C7 80C8 80D8
TMDS	TMDS	TMDS_DATA_N<2..0>	78C3 79C7 80C8 80D8
TMDSCONN	TMDSCONN	TMDS_CLK_F_P	80B5 80B6 80D1
TMDSCONN	TMDSCONN	TMDS_CLK_F_N	80A5 80C6 80D1
TMDSCONN	TMDSCONN	TMDS_DATA_F_P<5..3>	80A6 80B3 80B5 80B6 80D1
TMDSCONN	TMDSCONN	TMDS_DATA_F_N<5..3>	80A6 80B3 80B5 80B6 80D1
TMDSCONN	TMDSCONN	TMDS_DATA_F_P<2..0>	80B3 80B5 80C6 80D1 80D6
TMDSCONN	TMDSCONN	TMDS_DATA_F_N<2..0>	80B3 80B5 80C6 80D1 80D6

M57 NET PROPERTIES

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	87	87