ZC1 SYSTEM BLOCK DIAGRAM

EV@: Stuff when external VGA used
SH@: Stuff when SATA HDD used
PH@: Stuff when PATA HDD used

X'TAL 14.318MHZ
Clock Generator
ICS954310BGLF P2

Yonah/Merom 479
uFCPGA P3,P4

CPU Thermal Sensor P5

533/667 MHZ FSB

DVI P25
TVOUT P25
TFT LCD Panel 15.4" WXGA WSXGA+ P25
CRT P26

DVI
TVout
LVDS
VGA

VRAM X 4(GDDR3) 128M/256M P23

VGA ATI M56P P18,P19,P20,P21,P22,P24

PCI-Express 16X Lan

CALISTOGA-945PM 1466 FCBGA P6,P7,P8,P9,P10,P11

Dual Channel DDR2
533/667 Mhz

DDR II SODIMM0
DDR II SODIMM1 P12,P13

EZ4 Docking Connector
PCIE1~2 , Lan
Ser & Par Port
PS2 , VGA, DVI
SPDIF,SM BUS
P32

PCI-Express X 2
TV out / CRT → Switch P25,26
Audio → Switch P37
DVI
10/100/1G → Switch MAX4892 P25,P28

X'TAL 27M
X'TAL 25M

HDD P35 — IDE — SPIF3811 P34 — SATA

DMI X4 interface

ICH7-M Digital Home
652 BGA
P14,P15,P16,P17

MiniCard / WLAN P29
USB5
New Card P33

PCI-Express

Bluetooth USB6 P29
Media-Bay ODD/2nd HDD/2nd Battery P35
Camera Module(1.3M) USB7 P25
Smart card(OZ776PSN) USB4 P31
USB Port x 4 USB0~3 P29
X'TAL 6M

USB 2.0

PCI Bus interface

X'TAL24.576MHZ
PCMCIA+1394 +Cardreader Controller
O2 711MP1
P30,P31

X'TAL 25M
Intel Tekoa GigaLAN
82573E P27

EEPROM P27
Transformer P28
RJ45 P28

SMBUS
G-SENSOR P35
X'TAL 32.768KHZ

LPC

Int MIC P37
Azalia Audio Controller Realtek ALC883 P36
Azalia
Audio Amplifier Maxim Max 9750 P37

X'TAL 32.768K
KBC PC97551 P39

OSC 48MHZ

IEEE 1394 Port P31
6 in 1 Cardreader Socket P30
PCMCIA Slot P30
Fan Header P5

Primary Battery
Secod Battery
P45,P46

MIC Jack P37
Line in P37

BIOS P39

Speaker P37
Phone Jack P37
Azalia MDC P36
RJ11 P28

Touch Pad (Dual-Point) P40

Super I/O NS PC87383 P38
FIR P38
TPM 1.2 P38

PROJECT : ZC1
Quanta Computer Inc.

Size	Document Number	Rev
	BLOCK DIAGRAM	1A
Date: Monday, October 03, 2005	Sheet 1 of 46	

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	200	100	33

Default

A1A-change X1,X2 capacitor from 27pf to 33pf(CL=20pf)

Close to IC <500mils

Place these termination to close CK410M.

CK-410M

ICS954310BGLF

A1A:Remove PCIE clock

A1A:Change pin 3 PCLK_LAN to PCLK_TPM

ITP/SRC7 SELECT
0: SRC7 1: ITP

PREQ3(PCIE) Latched Select
"0" : CLK Enable
"1" : CLK Disable Control : PCIE 2,4,6,8

PREQ4(PCIE) Latched Select
"0" : CLK Enable
"1" : CLK Disable Control : PCIE 1,3,5,7

A1A-FSB Frequency Select:by CPU driven

Stuff 0 ohm for 533MHz, NC for 667MHz

swap

Latched Select. (Pin 17,18)
"0" : LCD CLK(UMA)
"1" : PCIEX CLK(M56)

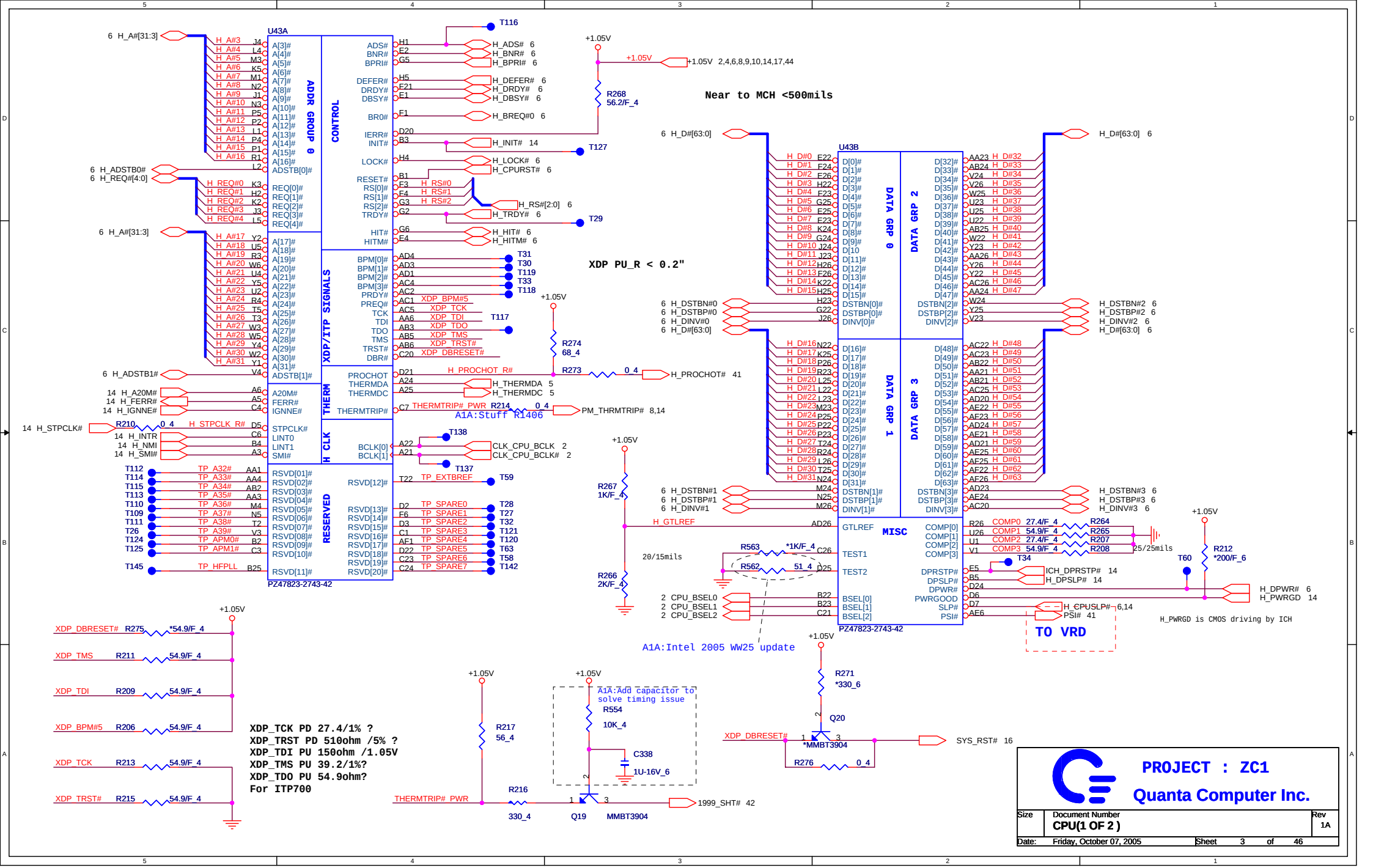
Latched Select. (Pin 40,41)
"0" : PCIEX CLK
"1" : PEREQ#

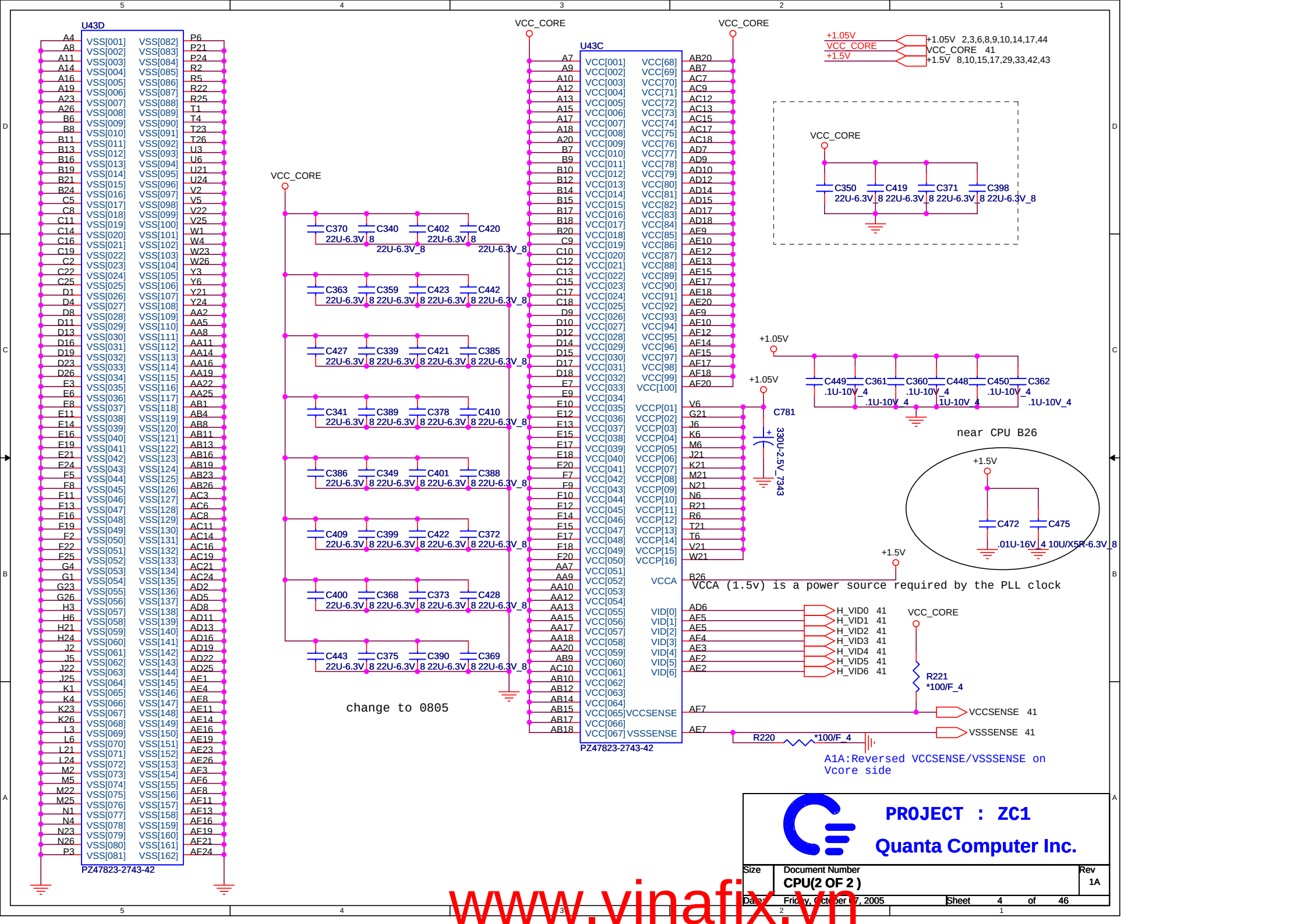
SELLCD_27# Select. (Pin 17,18)
"0" : 27MHzSS/27MHzSS# pair
"1" : LCD CLK pair

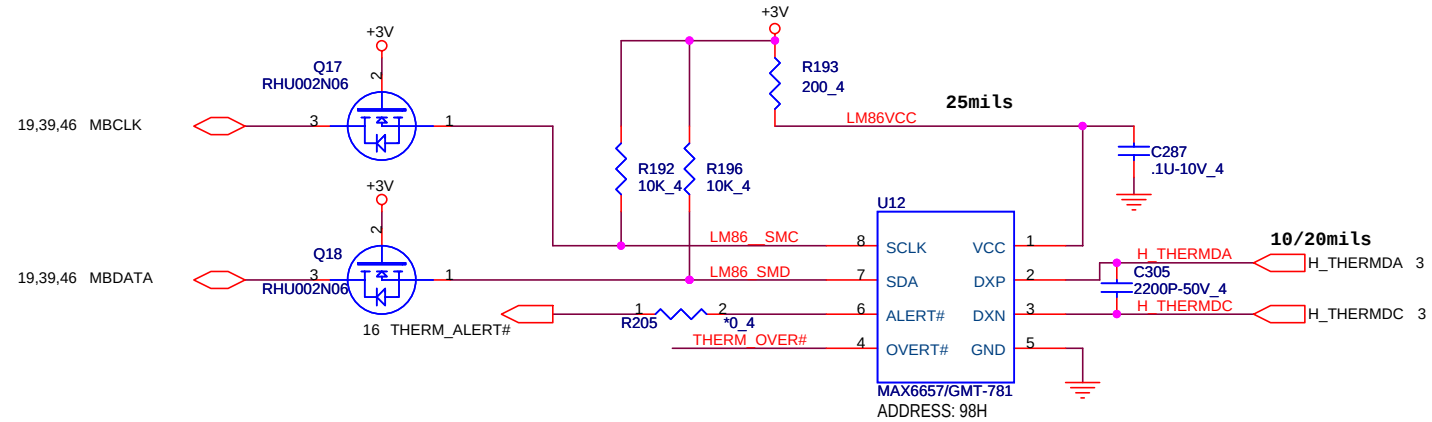
PROJECT : ZC1

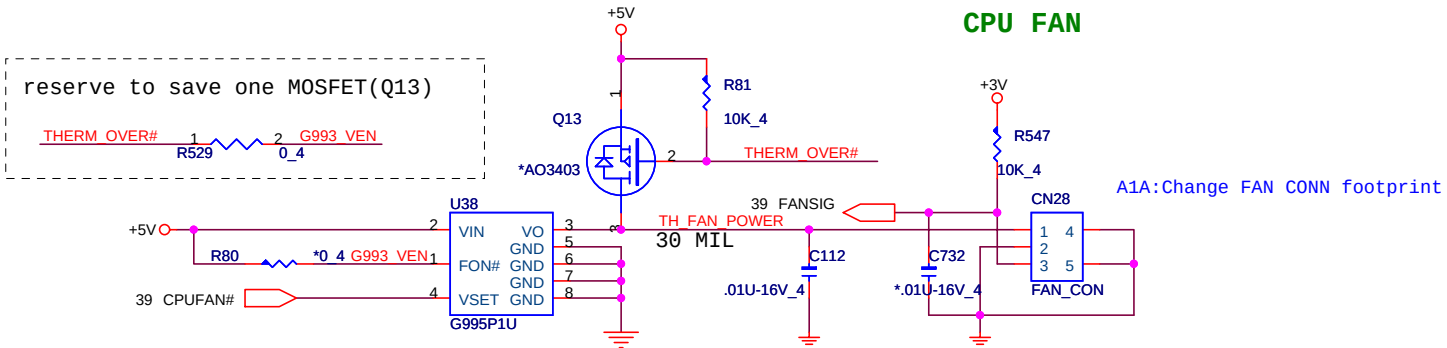
Quanta Computer Inc.

Size	Document Number	Rev
	CLOCK GENERATOR	1A
Date: Friday, October 07, 2005	Sheet 2 of 46	

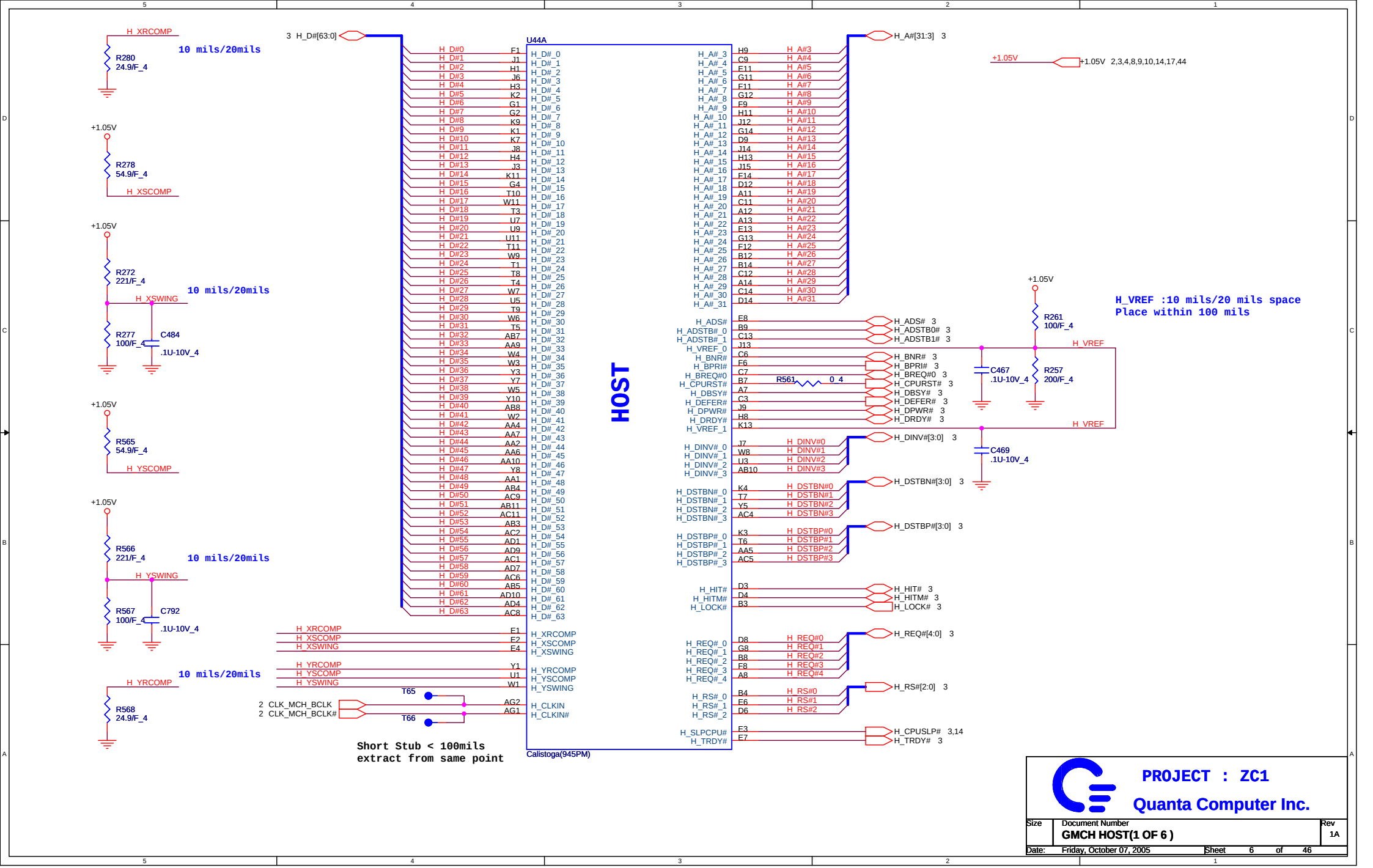


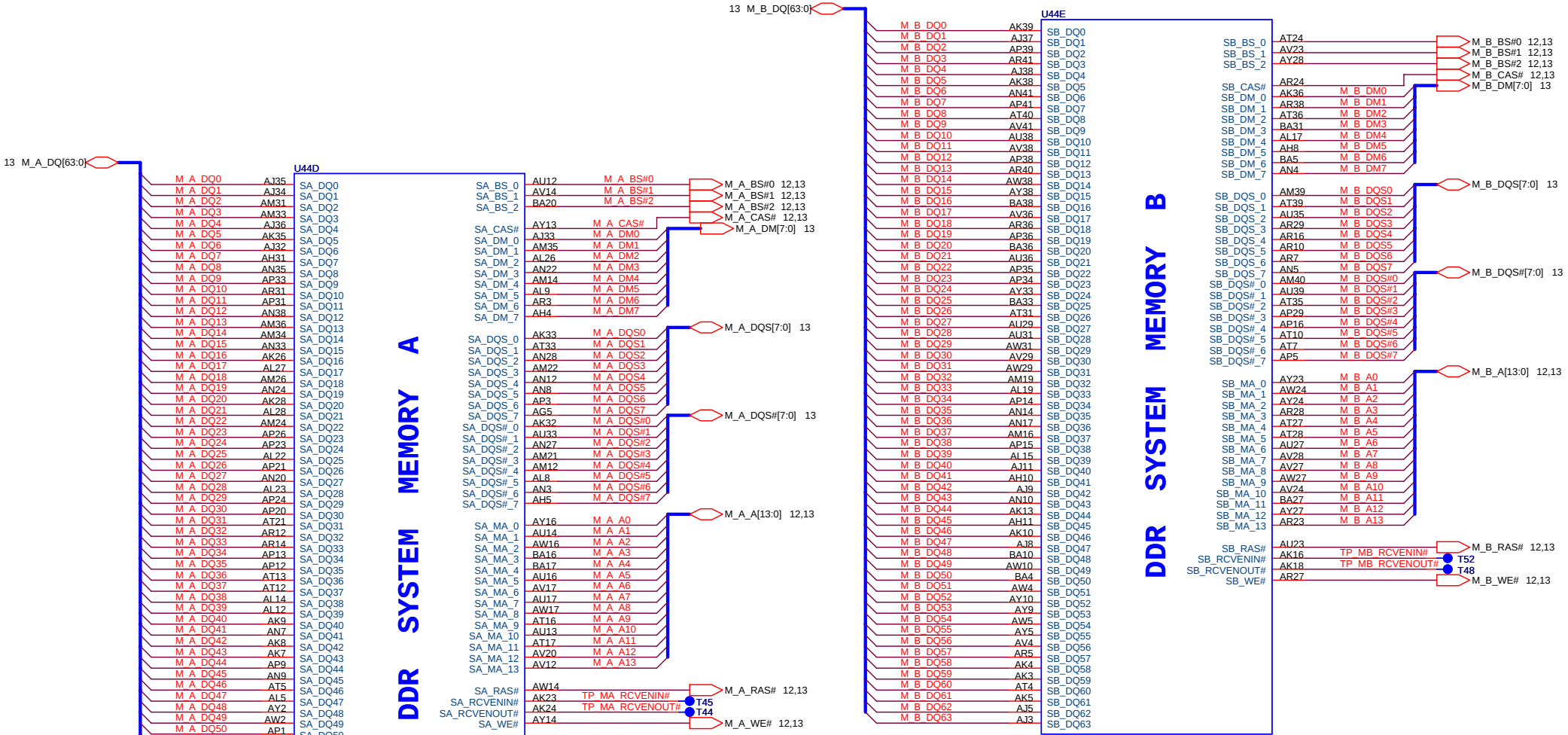






Quanta Computer Inc.	PROJECT : ZC1	
Size	Document Number: Thermal Sensor,FAN	Rev: 1A
Date: Friday, October 07, 2005	Sheet 5 of 46	

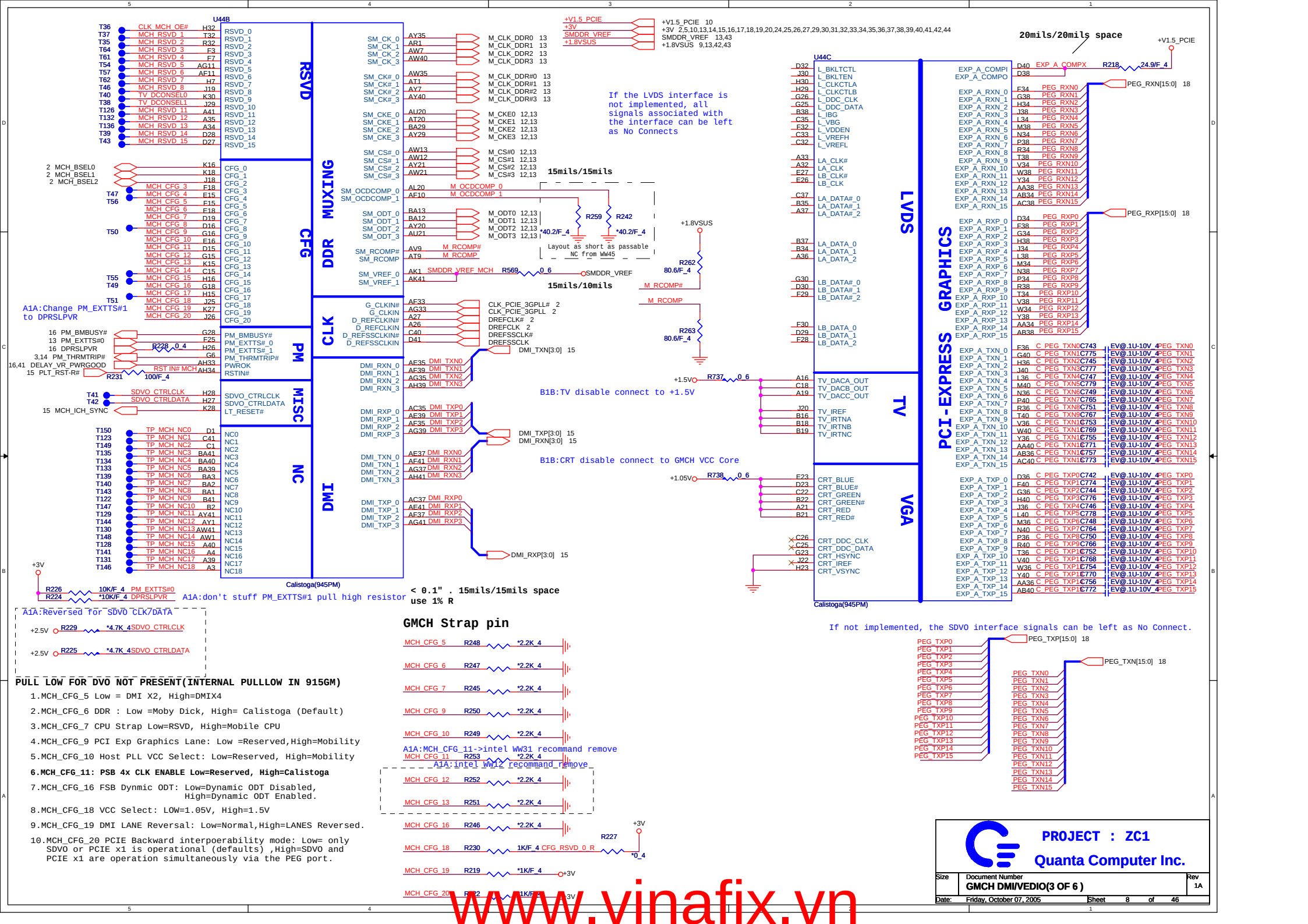


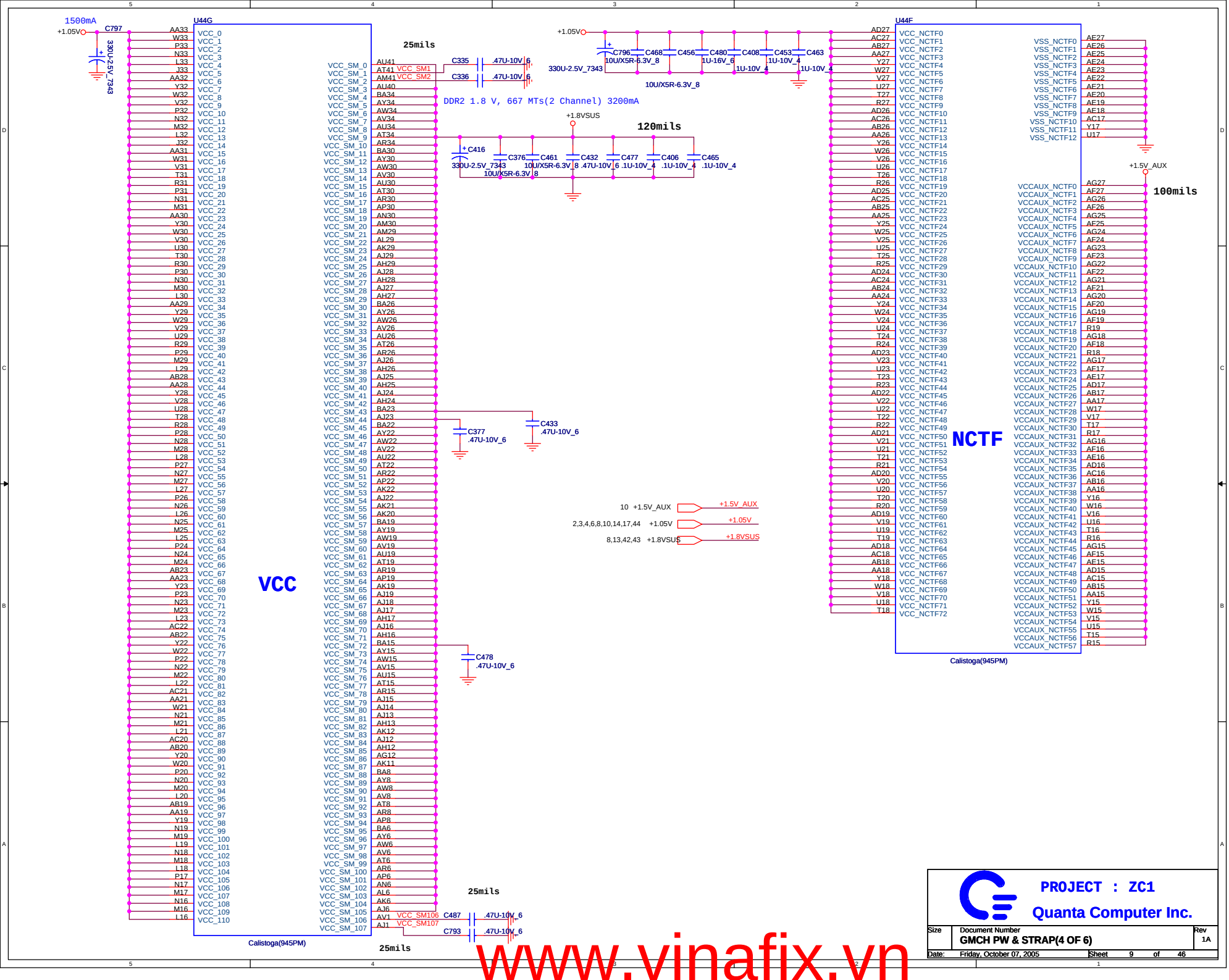


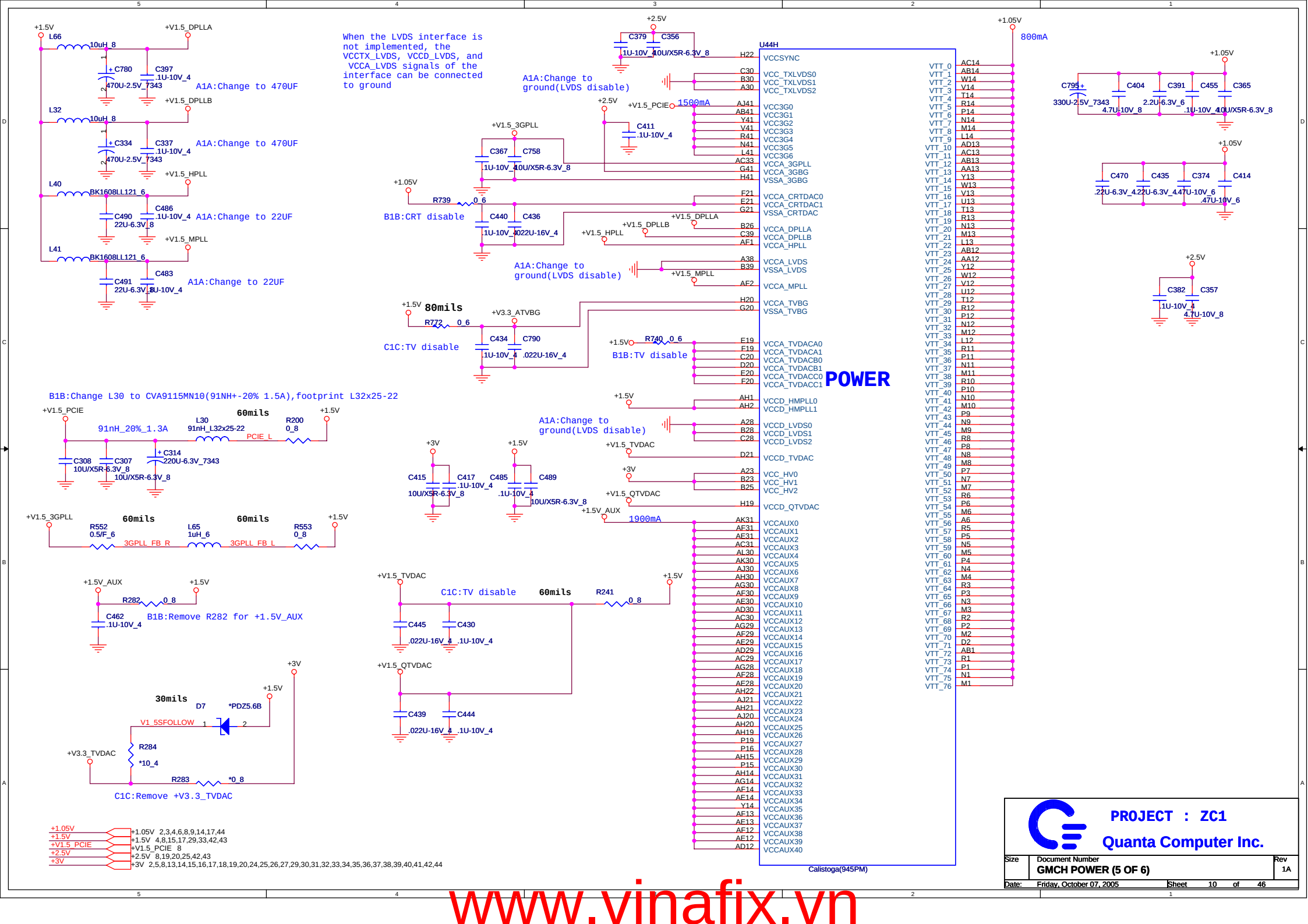
PROJECT : ZC1

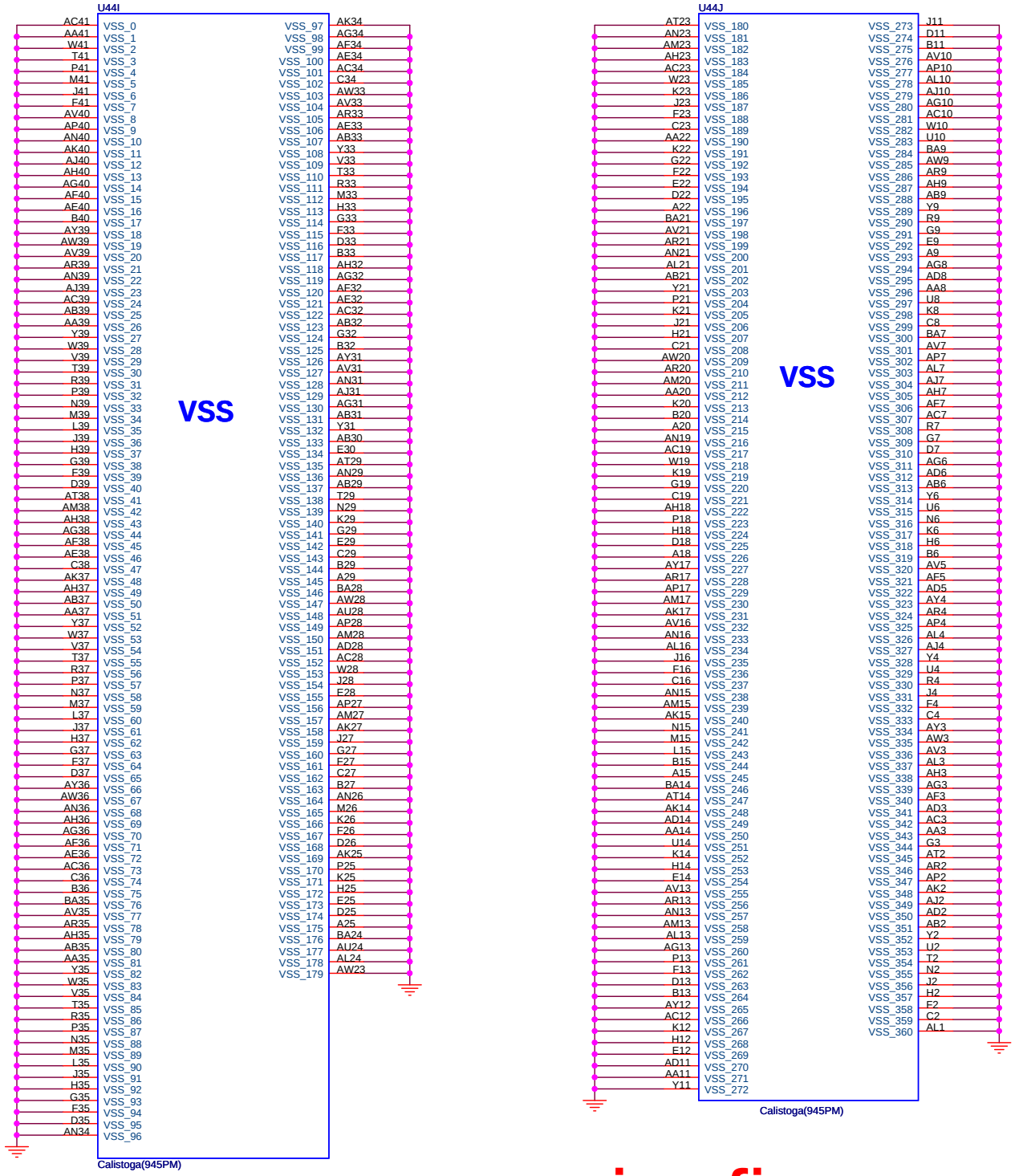
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH DDR(2 OF 6)	1A
Date: Monday, October 03, 2005	Sheet 7 of 46	









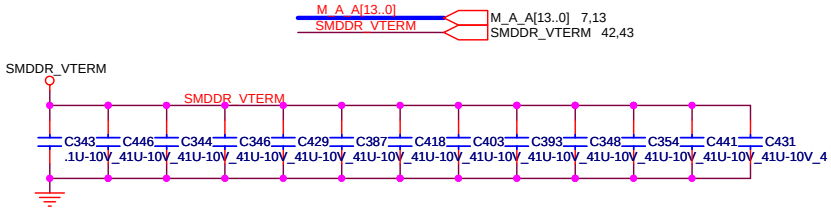
PROJECT : ZC1

Quanta Computer Inc.

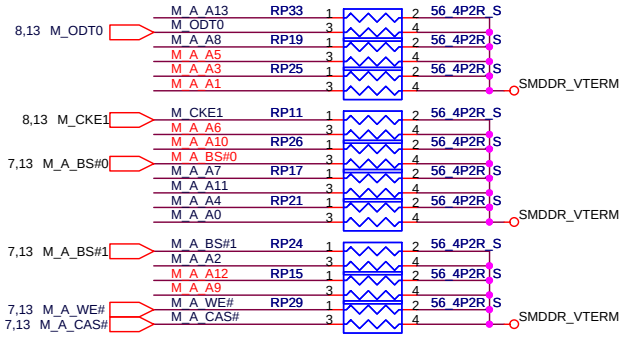
Size	Document Number	Rev
	GMCH GND(6 OF 6)	1A
Date: Monday, October 03, 2005	Sheet 11 of 46	

DDRII DUAL CHANNEL A,B.

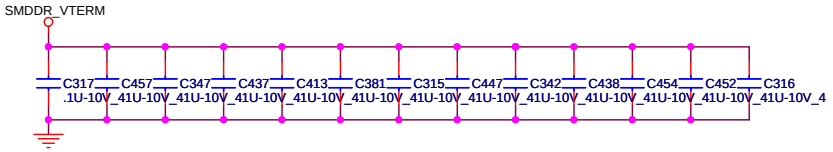
DDRII A CHANNEL



A1A:Swap net

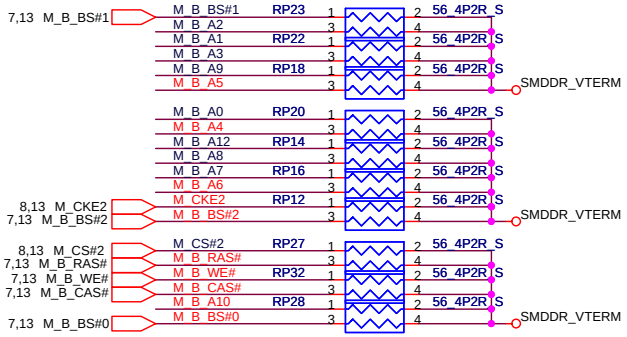


DDRII B CHANNEL

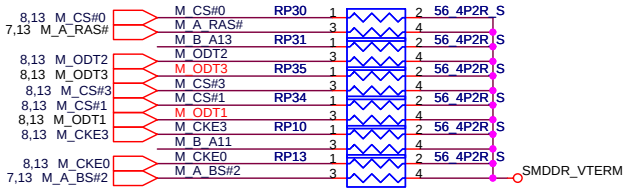


Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

A1A:Swap net



A1A:Swap net



PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	DDR RES. ARRAY	1A

Date: Friday, October 07, 2005 Sheet 12 of 46

+3V
+1.8VSUS
+3V 2,5,8,10,14,15,16,17,18,19,20,24,25,26,27,29,30,31,32,33,34,35,36,37,38,39,40,41,42,44
+1.8VSUS 8,9,42,43

SMDDR_VREF_DIMM
A1A:Swap net

M_A_DM[0..7] 7
M_A_DQ[0..63] 7
M_A_DQS[0..7] 7
M_A_DQS#[0..7] 7
M_A_A[0..13] 7,12

A1A:Change DDRII footprint to same as CT6

CN31

PC4800 DDR2 SDRAM SO-DIMM (200P)

	VREF	VSS46	2
	VSS47	DQ4	4
M_A_DQ1	DQ0	DQ5	6
M_A_DQ5	DQ1	VSS15	8
	VSS37	DM0	10
M_A_DQS#0	DQS#0	VSS5	12
M_A_DQS0	DQS0	DQ6	14
	VSS48	DQ7	16
M_A_DQ2	DQ2	VSS16	18
M_A_DQ3	DQ3	DQ12	20
	VSS38	DQ13	22
M_A_DQ14	DQ8	VSS17	24
M_A_DQ8	DQ9	DM1	26
	VSS49	VSS53	28
M_A_DQS#1	DQS#1	CK0	30
M_A_DQS1	DQS1	CK0#	32
	VSS39	VSS41	34
M_A_DQ9	DQ10	DQ14	36
M_A_DQ15	DQ11	DQ15	38
	VSS50	VSS54	40
	VSS18	VSS20	42
M_A_DQ21	DQ16	DQ20	44
M_A_DQ17	DQ17	DQ21	46
	VSS1	VSS6	48
M_A_DQS#2	DQS#2	NC3	50
M_A_DQS2	DQS2	DM2	52
	VSS19	VSS21	54
M_A_DQ23	DQ18	DQ22	56
M_A_DQ19	DQ19	DQ23	58
	VSS22	VSS24	60
M_A_DQ24	DQ24	DQ28	62
M_A_DQ25	DQ25	DQ29	64
	VSS23	VSS25	66
M_A_DM3	DM3	DQS#3	68
	NC4	DQS3	70
	VSS9	VSS10	72
M_A_DQ30	DQ26	DQ30	74
M_A_DQ31	DQ27	DQ31	76
	VSS4	VSS8	78
8,12 M_CKE0	CKE0	CKE1	80
	VDD7	VDD8	82
	NC1	A15	84
7,12 M_A_BS#2	A16_BA2	A14	86
M_A_A12	VDD9	VDD11	88
M_A_A9	A12	A11	90
M_A_A8	A9	A7	92
	A8	A6	94
M_A_A5	VDD5	VDD4	96
M_A_A3	A5	A4	98
M_A_A1	A3	A2	100
	A1	A0	102
M_A_A10	VDD10	VDD12	104
7,12 M_A_BS#0	A10/AP	BA1	106
7,12 M_A_WE#	BA0	RAS#	108
	WE#	S0#	110
7,12 M_A_CAS#	VDD2	VDD1	112
8,12 M_CS#1	CAS#	ODT0	114
	S1#	A13	116
8,12 M_ODT1	VDD3	VDD6	118
	ODT1	NC2	120
M_A_DQ37	VSS11	VSS12	122
M_A_DQ35	DQ32	DQ36	124
	DQ33	DQ37	126
M_A_DQS#4	VSS26	VSS28	128
M_A_DQS4	DQS#4	DM4	130
	DQS4	VSS42	132
M_A_DQ38	VSS2	DQ38	134
M_A_DQ39	DQ34	DQ39	136
	DQ35	VSS55	138
M_A_DQ41	VSS27	DQ44	140
M_A_DQ40	DQ40	DQ45	142
	DQ41	VSS43	144
M_A_DM5	VSS29	DQS#5	146
	DM5	DQS5	148
M_A_DQ42	VSS51	VSS56	150
M_A_DQ43	DQ42	DQ46	152
	DQ43	DQ47	154
M_A_DQ53	VSS40	VSS44	156
M_A_DQ52	DQ48	DQ52	158
	DQ49	DQ53	160
	VSS52	VSS57	162
	NCTEST	CK1	164
M_A_DQS#6	VSS30	CK1#	166
M_A_DQS6	DQS#6	VSS45	168
	DQS6	DM6	170
M_A_DQ51	VSS31	VSS32	172
M_A_DQ50	DQ50	DQ54	174
	DQ51	DQ55	176
M_A_DQ61	VSS33	VSS35	178
M_A_DQ57	DQ56	DQ60	180
	DQ57	DQ61	182
M_A_DM7	VSS3	VSS7	184
	DM7	DQS#7	186
M_A_DQ63	VSS34	DQS7	188
M_A_DQ59	DQ58	VSS36	190
	DQ59	DQ62	192
	VSS14	DQ63	194
CGDAT_SMB	SDA	VSS13	196
CGCLK_SMB	SCL	SA0	198
	VDD(SPD)	SA1	200

DDR2_SODIMM(1-1734074-1)

M_CLK_DDR0 8
M_CLK_DDR#0 8
PM_EXTTS#0 8
M_CKE1 8,12
M_A_BS#1 7,12
M_A_RAS# 7,12
M_CS#0 8,12
M_ODT0 8,12
M_CLK_DDR1 8
M_CLK_DDR#1 8

R285 10K_4
R287 10K_4

SMbus address A0
2nd source:DGMK00000C0

CLOCK 0,1 CKE 0,1 H 5.2

SMDDR_VREF_DIMM
A1A:Swap net

M_B_DM[0..7] 7
M_B_DQ[0..63] 7
M_B_DQS[0..7] 7
M_B_DQS#[0..7] 7
M_B_A[0..13] 7,12

CN30

PC4800 DDR2 SDRAM SO-DIMM (200P)

	VREF	VSS46	2
	VSS47	DQ4	4
M_B_DQ1	DQ0	DQ5	6
M_B_DQ5	DQ1	VSS15	8
	VSS37	DM0	10
M_B_DQS#0	DQS#0	VSS5	12
M_B_DQS0	DQS0	DQ6	14
	VSS48	DQ7	16
M_B_DQ2	DQ2	VSS16	18
M_B_DQ3	DQ3	DQ12	20
	VSS38	DQ13	22
M_B_DQ8	DQ8	VSS17	24
M_B_DQ9	DQ9	DM1	26
	VSS49	VSS53	28
M_B_DQS#1	DQS#1	CK0	30
M_B_DQS1	DQS1	CK0#	32
	VSS39	VSS41	34
M_B_DQ11	DQ10	DQ14	36
M_B_DQ10	DQ11	DQ15	38
	VSS50	VSS54	40
	VSS18	VSS20	42
M_B_DQ17	DQ16	DQ20	44
M_B_DQ20	DQ17	DQ21	46
	VSS1	VSS6	48
M_B_DQS#2	DQS#2	NC3	50
M_B_DQS2	DQS2	DM2	52
	VSS19	VSS21	54
M_B_DQ19	DQ18	DQ22	56
M_B_DQ23	DQ19	DQ23	58
	VSS22	VSS24	60
M_B_DQ28	DQ24	DQ28	62
M_B_DQ29	DQ25	DQ29	64
	VSS23	VSS25	66
M_B_DM3	DM3	DQS#3	68
	NC4	DQS3	70
	VSS9	VSS10	72
M_B_DQ30	DQ26	DQ30	74
M_B_DQ31	DQ27	DQ31	76
	VSS4	VSS8	78
8,12 M_CKE2	CKE0	CKE1	80
	VDD7	VDD8	82
	NC1	A15	84
7,12 M_B_BS#2	A16_BA2	A14	86
M_B_A12	VDD9	VDD11	88
M_B_A9	A12	A11	90
M_B_A8	A9	A7	92
	A8	A6	94
M_B_A5	VDD5	VDD4	96
M_B_A3	A5	A4	98
M_B_A1	A3	A2	100
	A1	A0	102
M_B_A10	VDD10	VDD12	104
7,12 M_B_BS#0	A10/AP	BA1	106
7,12 M_B_WE#	BA0	RAS#	108
	WE#	S0#	110
7,12 M_B_CAS#	VDD2	VDD1	112
8,12 M_CS#3	CAS#	ODT0	114
	S1#	A13	116
8,12 M_ODT3	VDD3	VDD6	118
	ODT1	NC2	120
M_B_DQ37	VSS11	VSS12	122
M_B_DQ36	DQ32	DQ36	124
	DQ33	DQ37	126
M_B_DQS#4	VSS26	VSS28	128
M_B_DQS4	DQS#4	DM4	130
	DQS4	VSS42	132
M_B_DQ39	VSS2	DQ38	134
M_B_DQ35	DQ34	DQ39	136
	DQ35	VSS55	138
M_B_DQ41	VSS27	DQ44	140
M_B_DQ40	DQ40	DQ45	142
	DQ41	VSS43	144
M_B_DM5	VSS29	DQS#5	146
	DM5	DQS5	148
M_B_DQ47	VSS51	VSS56	150
M_B_DQ42	DQ42	DQ46	152
	DQ43	DQ47	154
M_B_DQ53	VSS40	VSS44	156
M_B_DQ49	DQ48	DQ52	158
	DQ49	DQ53	160
	VSS52	VSS57	162
	NCTEST	CK1	164
M_B_DQS#6	VSS30	CK1#	166
M_B_DQS6	DQS#6	VSS45	168
	DQS6	DM6	170
M_B_DQ50	VSS31	VSS32	172
M_B_DQ55	DQ50	DQ54	174
	DQ51	DQ55	176
M_B_DQ61	VSS33	VSS35	178
M_B_DQ57	DQ56	DQ60	180
	DQ57	DQ61	182
M_B_DM7	VSS3	VSS7	184
	DM7	DQS#7	186
M_B_DQ63	VSS34	DQS7	188
M_B_DQ58	DQ58	VSS36	190
	DQ59	DQ62	192
	VSS14	DQ63	194
2 CGDAT_SMB	SDA	VSS13	196
2 CGCLK_SMB	SCL	SA0	198
	VDD(SPD)	SA1	200

DDR2_SODIMM(2-1734073-2)

M_CLK_DDR3 8
M_CLK_DDR#3 8
PM_EXTTS#0 8
M_CKE3 8,12
M_B_BS#1 7,12
M_B_RAS# 7,12
M_CS#2 8,12
M_ODT2 8,12
M_CLK_DDR2 8
M_CLK_DDR#2 8

R286 10K_4
R288 10K_4

SMbus address A4
2nd source:DGMK0002610

A1A:Change SODIMM1 pin 50 from PM_EXTTS#1 to PM_EXTTS#0(Intel recommend)

+1.8VSUS
Place these Caps near So-Dimm1.
C355 2.2U-6.3V_6
C352 2.2U-6.3V_6
C451 2.2U-6.3V_6
C425 2.2U-6.3V_6
C405 2.2U-6.3V_6

+1.8VSUS
Place these Caps near So-Dimm1.
C396 .1U-10V_4
C424 .1U-10V_4
C358 .1U-10V_4
C395 .1U-10V_4

SMDDR_VREF_DIMM
C267 .1U-10V_4
C250 2.2U-6.3V_6
+3V
C493 2.2U-6.3V_6
C495 .1U-10V_4

Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.

+1.8VSUS
Place these Caps near So-Dimm2.
C366 2.2U-6.3V_6
C345 2.2U-6.3V_6
C426 2.2U-6.3V_6
C351 2.2U-6.3V_6
C353 2.2U-6.3V_6

+1.8VSUS
Place these Caps near So-Dimm1.
C384 .1U-10V_4
C407 .1U-10V_4
C383 .1U-10V_4
C394 .1U-10V_4

SMDDR_VREF_DIMM
C264 .1U-10V_4
C272 2.2U-6.3V_6
+3V
C492 2.2U-6.3V_6
C494 .1U-10V_4

Place these Caps near So-Dimm2.
No Vias Between the Trace of PIN to CAP.

SMDDR_VREF
SMDDR_VREF_DIMM
R170 0_4
SMDDR_VREF 8,43
R162 *10K/F_4
R160 *10K/F_4
+1.8VSUS

PROJECT : ZC1
Quanta Computer Inc.

Size	Document Number	Rev
	DDRII SO-DIMM(200P)	1A
Date: Friday, October 07, 2005	Sheet 13 of 46	

RTC

CKL:C1/C2: 18pF -> CL:12.5pF
C1/C: 10pF -> CL Value = 8.5pF
A1A:Change RTXC1/RTXC2 from 10pf to 18pf

A1A:Change RTC Connector footprint

20MIL 20MIL

B1B:Per Intel comment,don't stuff R307 for CPUSLP#

Should be 2" close ICH7

A series termination resistor is required for the PRIMARY CODEC

B1B:Add R719 for BIT_CLK_MODEM

25mils/15mils

Place within 500 mils of ICH7

CKL:1n ~ 20nF

ICH7 internal VR enable strap

	INTVRMEN
Enable (default)	1
Disable	0

PROJECT :	ZC1
Quanta Computer Inc.	
Size	Document Number: ICH7-M HOST (1 OF 4) — Rev: 1A
Date:	Friday, October 07, 2005 — Sheet 14 of 46

A1A:Change PCIE pin define to meet Acer spec

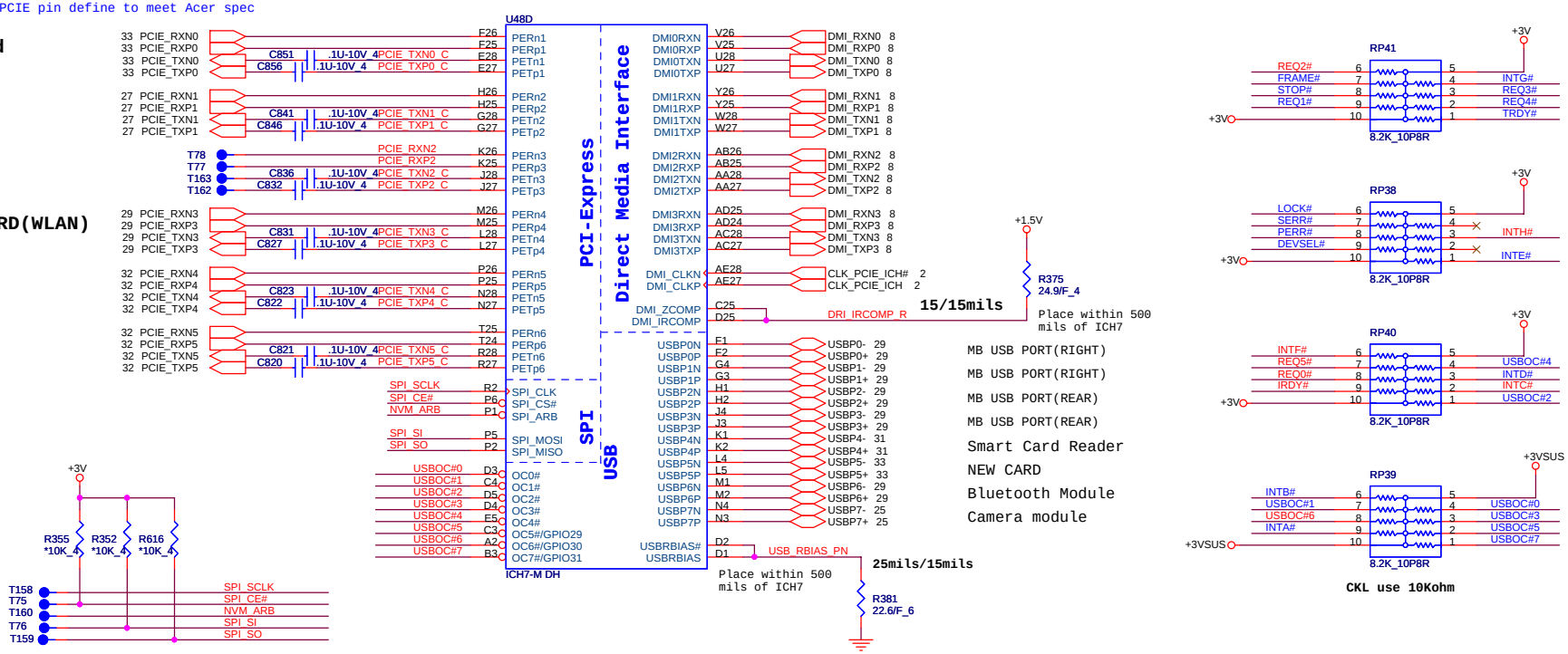
New card

GLAN

MINI CARD(WLAN)

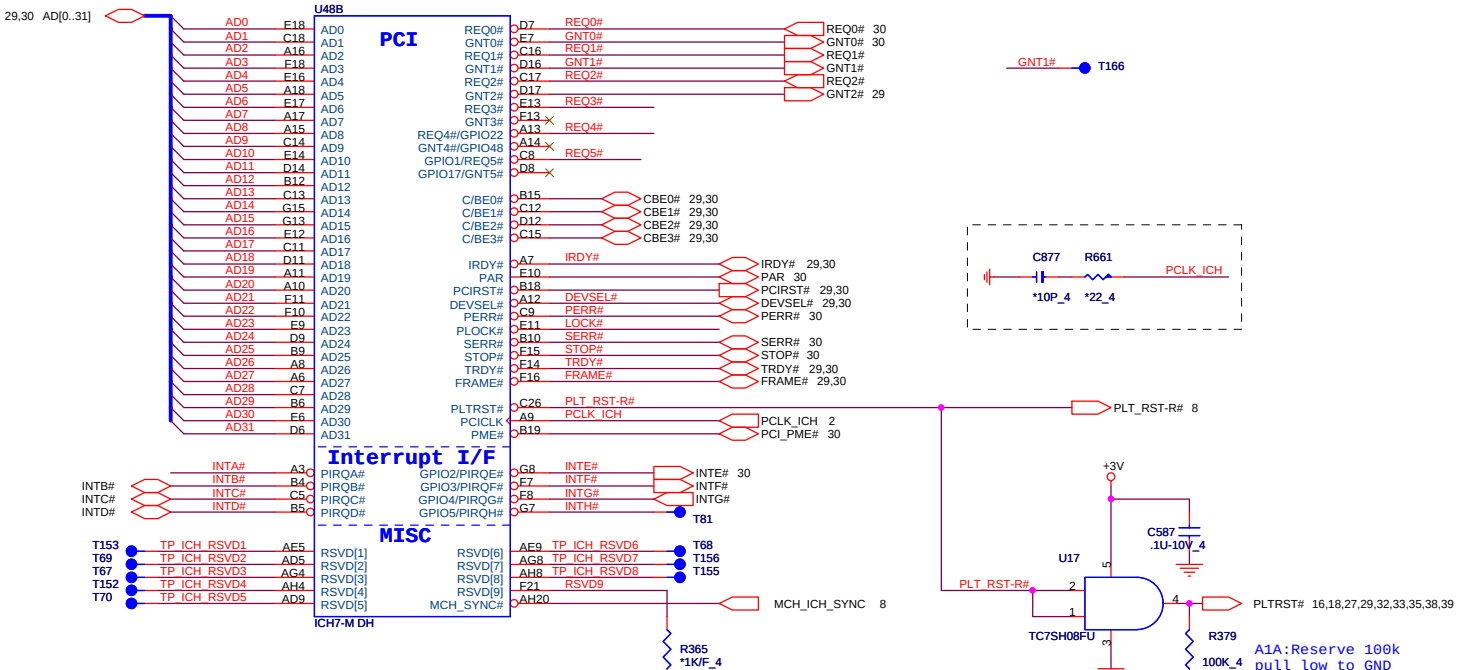
EZ4_1

EZ4_2



ICH7 Boot BIOS select

	STRAP	GNT5# R1	GNT4# R2
LPC (default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF



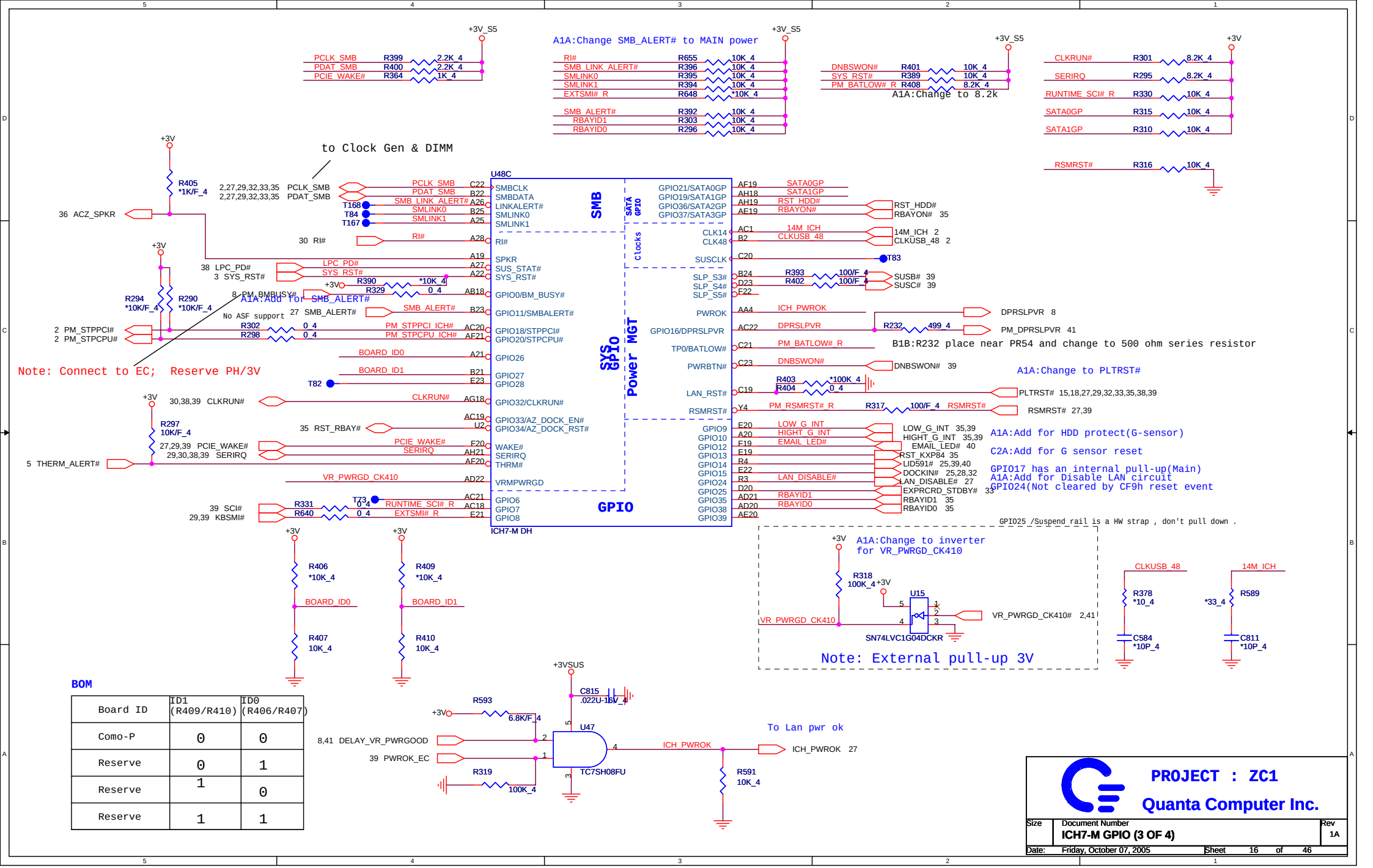
PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
OZ711MP1	AD25	REQ0# / GNT0#	INTE#

PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	ICH7-M PCI E (2 OF 4)	1A

Date: Friday, October 07, 2005 Sheet 15 of 46



BOM

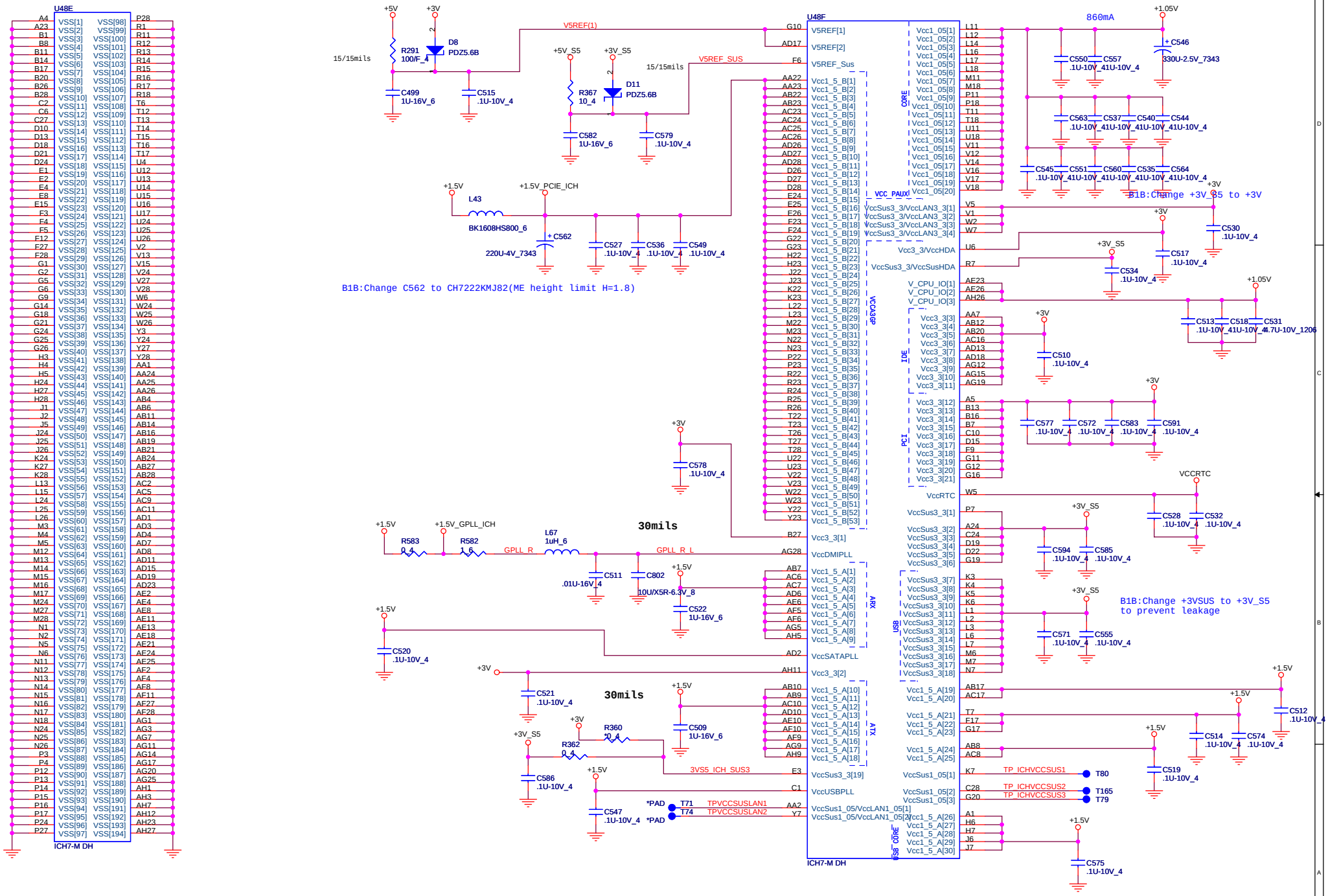
Board ID	ID1 (R409/R410)	ID0 (R406/R407)
Como-P	0	0
Reserve	0	1
Reserve	1	0
Reserve	1	1

PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	ICH7-M GPIO (3 OF 4)	1A

Date: Friday, October 07, 2005 Sheet 16 of 46



PCIE TEST PADS
PCIE TEST POINTS MUST BE WITHIN 250 MILS
OF THE ASIC BALL WITH POSITIVE AND NEGATIVE
SIGNALS THE SAME DISTANCE

8 PEG_RXP[15:0]
8 PEG_RXN[15:0]
8 PEG_TXP[15:0]
8 PEG_TXN[15:0]

U41A

PART 1 OF 7

PEG_TXP0	AJ31	PCIE_RX0P	PCIE_TX0P	AK27	V_GMCHEXP_RXP0	C304	EV@.1U-10V_4	PEG_RXP0
PEG_TXN0	AH31	PCIE_RX0N	PCIE_TX0N	AJ27	V_GMCHEXP_RXN0	C303	EV@.1U-10V_4	PEG_RXN0
PEG_TXP1	AH30	PCIE_RX1P	PCIE_TX1P	AJ25	V_GMCHEXP_RXP1	C333	EV@.1U-10V_4	PEG_RXP1
PEG_TXN1	AG30	PCIE_RX1N	PCIE_TX1N	AH25	V_GMCHEXP_RXN1	C332	EV@.1U-10V_4	PEG_RXN1
PEG_TXP2	AG32	PCIE_RX2P	PCIE_TX2P	AH28	V_GMCHEXP_RXP2	C302	EV@.1U-10V_4	PEG_RXP2
PEG_TXN2	AF32	PCIE_RX2N	PCIE_TX2N	AG28	V_GMCHEXP_RXN2	C301	EV@.1U-10V_4	PEG_RXN2
PEG_TXP3	AF31	PCIE_RX3P	PCIE_TX3P	AG27	V_GMCHEXP_RXP3	C331	EV@.1U-10V_4	PEG_RXP3
PEG_TXN3	AE31	PCIE_RX3N	PCIE_TX3N	AF27	V_GMCHEXP_RXN3	C330	EV@.1U-10V_4	PEG_RXN3
PEG_TXP4	AE30	PCIE_RX4P	PCIE_TX4P	AF25	V_GMCHEXP_RXP4	C300	EV@.1U-10V_4	PEG_RXP4
PEG_TXN4	AD30	PCIE_RX4N	PCIE_TX4N	AE25	V_GMCHEXP_RXN4	C299	EV@.1U-10V_4	PEG_RXN4
PEG_TXP5	AD32	PCIE_RX5P	PCIE_TX5P	AE28	V_GMCHEXP_RXP5	C329	EV@.1U-10V_4	PEG_RXP5
PEG_TXN5	AC32	PCIE_RX5N	PCIE_TX5N	AD28	V_GMCHEXP_RXN5	C328	EV@.1U-10V_4	PEG_RXN5
PEG_TXP6	AC31	PCIE_RX6P	PCIE_TX6P	AD27	V_GMCHEXP_RXP6	C298	EV@.1U-10V_4	PEG_RXP6
PEG_TXN6	AB31	PCIE_RX6N	PCIE_TX6N	AC27	V_GMCHEXP_RXN6	C297	EV@.1U-10V_4	PEG_RXN6
PEG_TXP7	AB30	PCIE_RX7P	PCIE_TX7P	AC25	V_GMCHEXP_RXP7	C327	EV@.1U-10V_4	PEG_RXP7
PEG_TXN7	AA30	PCIE_RX7N	PCIE_TX7N	AB25	V_GMCHEXP_RXN7	C326	EV@.1U-10V_4	PEG_RXN7
PEG_TXP8	AA32	PCIE_RX8P	PCIE_TX8P	AB28	V_GMCHEXP_RXP8	C296	EV@.1U-10V_4	PEG_RXP8
PEG_TXN8	Y32	PCIE_RX8N	PCIE_TX8N	AA28	V_GMCHEXP_RXN8	C295	EV@.1U-10V_4	PEG_RXN8
PEG_TXP9	Y31	PCIE_RX9P	PCIE_TX9P	AA27	V_GMCHEXP_RXP9	C325	EV@.1U-10V_4	PEG_RXP9
PEG_TXN9	W31	PCIE_RX9N	PCIE_TX9N	Y27	V_GMCHEXP_RXN9	C324	EV@.1U-10V_4	PEG_RXN9
PEG_TXP10	W30	PCIE_RX10P	PCIE_TX10P	Y25	V_GMCHEXP_RXP10	C294	EV@.1U-10V_4	PEG_RXP10
PEG_TXN10	V30	PCIE_RX10N	PCIE_TX10N	W25	V_GMCHEXP_RXN10	C293	EV@.1U-10V_4	PEG_RXN10
PEG_TXP11	V32	PCIE_RX11P	PCIE_TX11P	W28	V_GMCHEXP_RXP11	C323	EV@.1U-10V_4	PEG_RXP11
PEG_TXN11	U32	PCIE_RX11N	PCIE_TX11N	V28	V_GMCHEXP_RXN11	C322	EV@.1U-10V_4	PEG_RXN11
PEG_TXP12	U31	PCIE_RX12P	PCIE_TX12P	V27	V_GMCHEXP_RXP12	C292	EV@.1U-10V_4	PEG_RXP12
PEG_TXN12	T31	PCIE_RX12N	PCIE_TX12N	U27	V_GMCHEXP_RXN12	C291	EV@.1U-10V_4	PEG_RXN12
PEG_TXP13	T30	PCIE_RX13P	PCIE_TX13P	U25	V_GMCHEXP_RXP13	C321	EV@.1U-10V_4	PEG_RXP13
PEG_TXN13	R30	PCIE_RX13N	PCIE_TX13N	T25	V_GMCHEXP_RXN13	C320	EV@.1U-10V_4	PEG_RXN13
PEG_TXP14	R32	PCIE_RX14P	PCIE_TX14P	T28	V_GMCHEXP_RXP14	C290	EV@.1U-10V_4	PEG_RXP14
PEG_TXN14	P32	PCIE_RX14N	PCIE_TX14N	R28	V_GMCHEXP_RXN14	C289	EV@.1U-10V_4	PEG_RXN14
PEG_TXP15	P31	PCIE_RX15P	PCIE_TX15P	R27	V_GMCHEXP_RXP15	C319	EV@.1U-10V_4	PEG_RXP15
PEG_TXN15	N31	PCIE_RX15N	PCIE_TX15N	P27	V_GMCHEXP_RXN15	C318	EV@.1U-10V_4	PEG_RXN15

PCI-EXPRESS INTERFACE

Clock

2 CLK_PCIE_M56
2 CLK_PCIE_M56#
AL28 PCIE_REFCLKP
AK28 PCIE_REFCLKN

15,16,27,29,32,33,35,38,39 PLTRST#
PLTRST# M26
AG24 PERSTB
PCIE_TEST
AA24 PCIE_TEST

AF24 PERSTB_MASK
Tie To VSS

Calibration

PCIE_CALRN
PCIE_CALRP
PCIE_CALI

AE24 R156 EV@2K/F_4
AD24 R172 EV@562/F_4
+1.2V_VPCIE
AB24 R167 EV@1.47K/F_4

B1B:PCIE_CALRN(ball AE24) need change to +1.2V_VPCIE

FOR M52P,M54P,M56P
PCIE_CALRN = 2K
PCIE CALRP = 562R
PCIE CALI = 1.47K

EV@M56-P B13

ATI FEATURE NOT ENABLED (M52P,M54P,M56P)
B1B:Don't stuff R153,R166 for PCIE_TEST

+3V
R153 *4.7K_4
PCIE_TEST
R166 *4.7K_4

PROJECT : ZC1				
Quanta Computer Inc.				
Size	Document Number			Rev
	M56P 1 OF 7			1A
Date:	Friday, October 07, 2005	Sheet	18 of	46

MEMORY CLOCK SPREAD SPECTRUM

ANY UNUSED GPIO CAN OPTIONALLY BE MEMORY TYPE CONFIG STRAPS

C1C:Change GPIO27 instead of GPIO25 for MEMTYPE_1

The TMDS termination resistor values (330 ohm) are pcb layout dependent and may require final tuning

B1B:Change R177,R181 to 0 ohm for VGA 27MHZ

FOR M52P,M54P,M56P NOT CONNECTED

B1B:Don't stuff C739

Voltage divider resistor values R181 and R551 to ensure XTALIN/XTALOUT voltage level matches vddc

A1A:Reversed LVDSCLK,LVDSDATA pull high to LVDS side

A1A:Change LVDS_DAT/LVDS_CLK to DVPDATA18/DVPDATA19

A1A:Add pull low 10k
GPIO15 HI = 1.0V VDDC
GPIO15 LO = 1.1V VDDC

V_PWRCNTL DRIVEN HI SELECT 1.0V VDDC
V_PWRCNTL DRIVEN LO SELECT 1.1V VDDC

For m26x,m52p,m54p,m56p thermal interrupt is low edge and connects to gpio17

B1B:Reserved for VREFG

FOR M52P,M54P,M56P CONNECT TO +2.5V

1.2V OR 1.0V @ 20MA ASIC MPVDD
CONNECT TO VDDC

For m26x,m52p,m54p,m56p thermal interrupt is low edge and connects to gpio17

FOR M52P,M54P,M56P CONNECT TO +2.5V

VDD_PNL_PLL25 (2.5V @ 40mA ASIC LPVDD,TPVDD)

AVDD_2.5 (2.5V @ 65mA ASIC AVDD)

VDDDI_2.5 (2.5V @ 40mA ASIC VDD1DI,VDD2DI)

PLACE CLOSE TO ASIC

A1A:Change to 75 ohm
C1A:Remoe 75 ohm to solve CRT/TV hot plug issue

FOR M52P,M54P,M56P A2VDDQ IT IS NO CONNECT

FOR M52P,M54P,M56P CONNECT TO +2.5V

The DDC2 is for DVI (TMDS) reading EDID data, which cannot be shared with other I2C devices.

A1A:Reserve for thermal sensor_CLK/DATA

B1B:Stuff R125,R126 for VGA thermal sensor SMBus

FOR M52P,M54P,M56P GENERICC IT IS GPIO

15 MIL

10 mil trace / 10 mil space

Close to pin ASIC

SLAVE ADDRESS: 9A

B1B:Don't stuff R82,R95 for thermal sensor

A1A:Reserve for VGA thermal sensor

C2A:Stuff Q12,Q31 for VGA thermal sensor

B1B:Remove Q12,Q31 for VGA thermal sensor

PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	M56P 2 OF 7	1A

Date: Friday, October 07, 2005 Sheet 19 of 46

If memory interface has to be up to 600Mhz or above, the GPU core voltage and memory I/O voltage may need to be increased to 1.2~1.3V and 2.0V

A1A:Change to VGA_MEM_IO

U41E

PART 5 OF 7

POWER

Memory I/O

Core

I/O Internal

LVDS PLL, I/O

PCI-Express

Memory I/O Clock

EV@M56-P B13

1.2V ASIC PCIE_PVDD_12 @ 100mA, PCIE_VDDR_12 @ 2000mA

FOR M52P,M54P,M56P CONNECT TO +1.2V

1.2V OR 1.0V @ 18A ASIC VDDC,VDDCI

VDD_PNL_PLL25 (2.5V @ 40mA ASIC LPVDD,TPVDD)

GENERICD : FOR M56P IT IS A BACK BIAS REGULATOR CONTROL

Panel power(LCDVCC) control

GENERICD->FOR M56P IT IS A BACK BIAS REGULATOR CONTROL

U41G

PART 7 OF 7

Forward Compatibility

Control and External SSC

LVDS channel

EV@M56-P B13

A1A:Change to VGA_MEM_IO

U9

MAINON

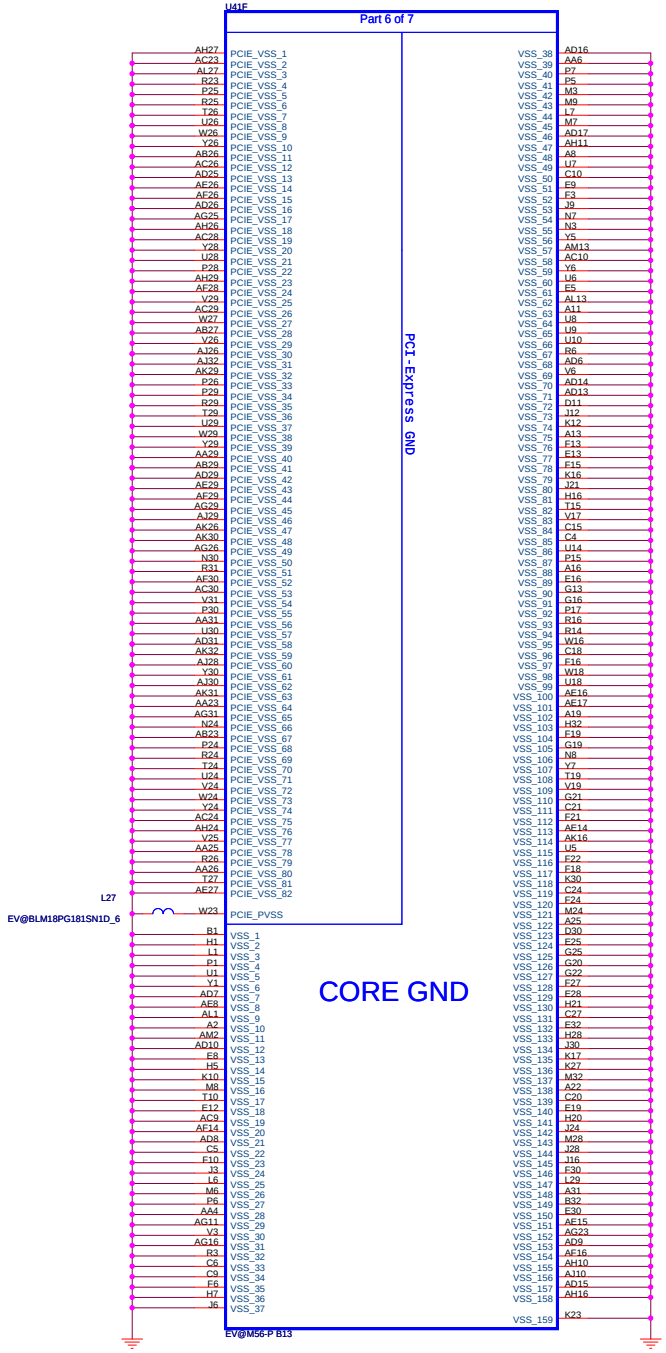
EV@C966

PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	M56P POWER	1A

Date: Friday, October 07, 2005 Sheet 20 of 46



PROJECT : ZC1

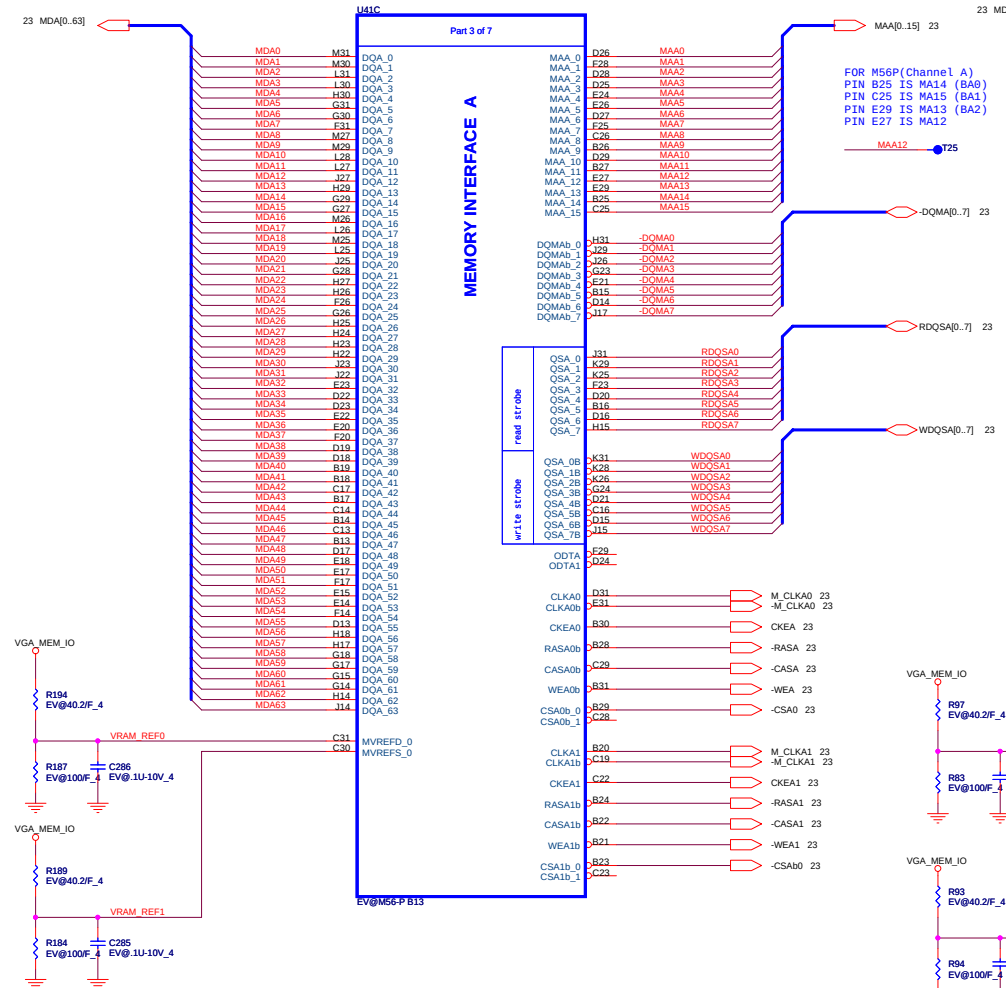
Quanta Computer Inc.

Size	Document Number	Rev
	M56P 6 OF 7	1A

Date: Friday, October 07, 2005 Sheet 21 of 46

RV410 MEMORY CHANNELS A and B

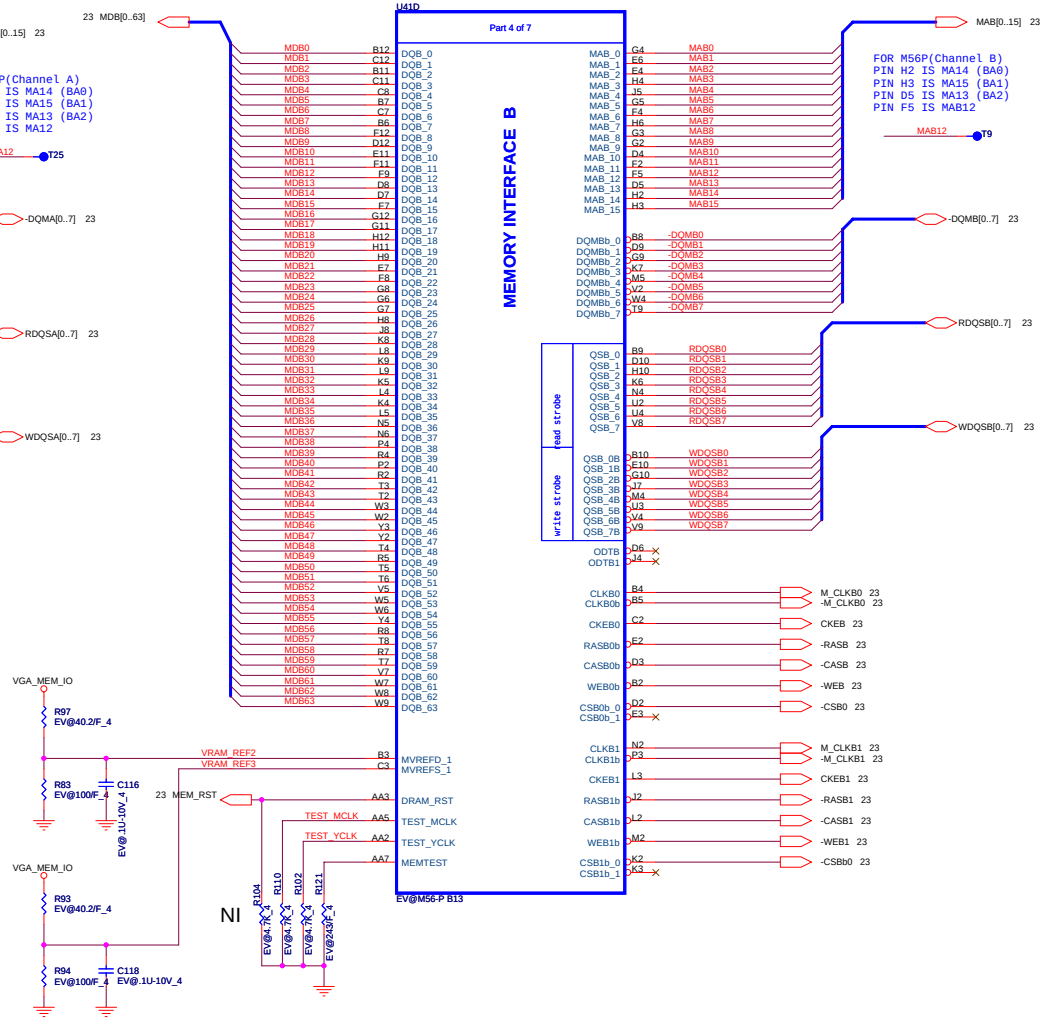
Channel A



Place VRAM_REF0,VRAM_REF1 parts closed M56

Reference voltage per channel (memory data/strobe)
MVREFD_[0:1] (0.7 * VDDR1) (for GDDR3)
MVREFS_[0:1] (0.7 * VDDR1) (for GDDR3)

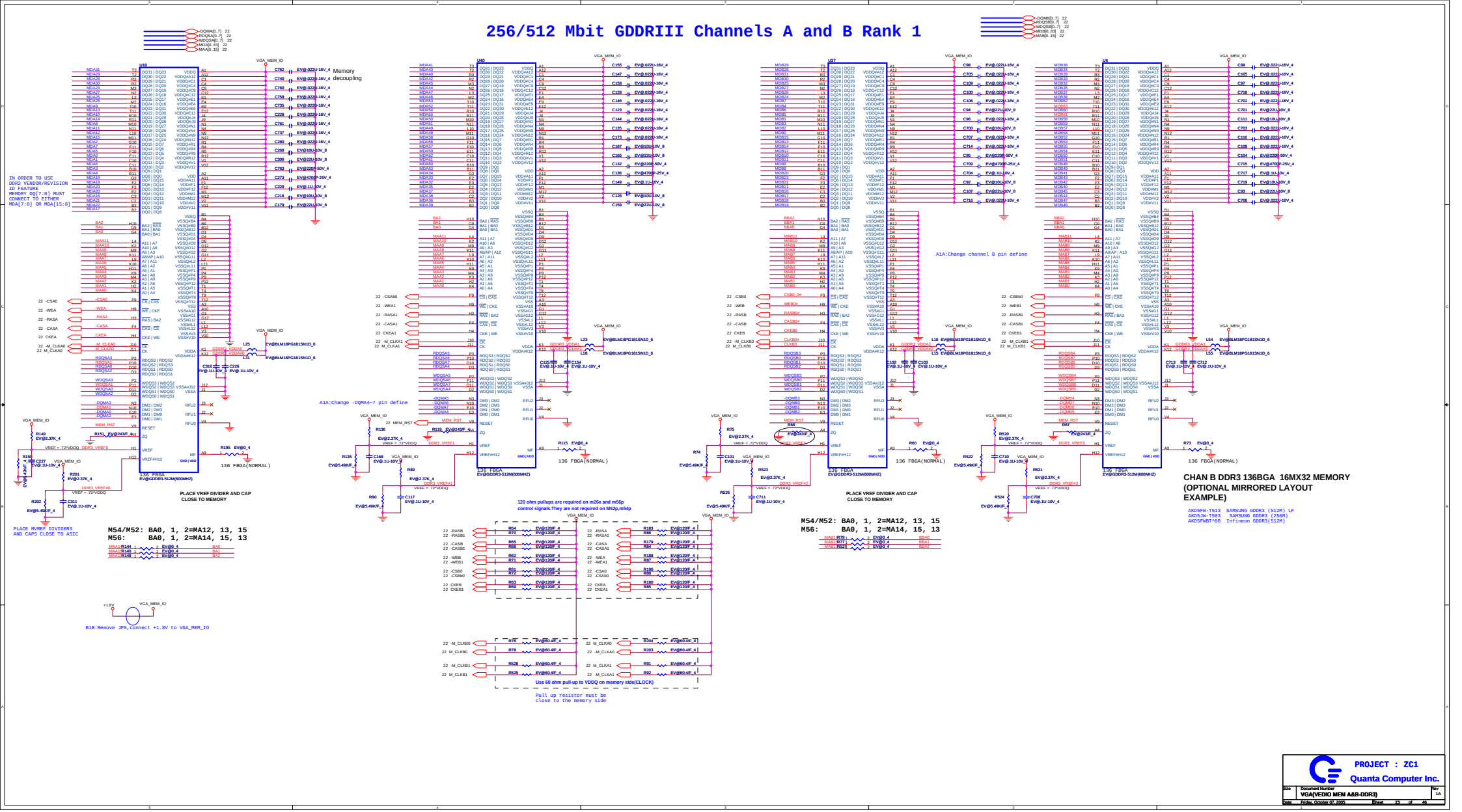
Channel B



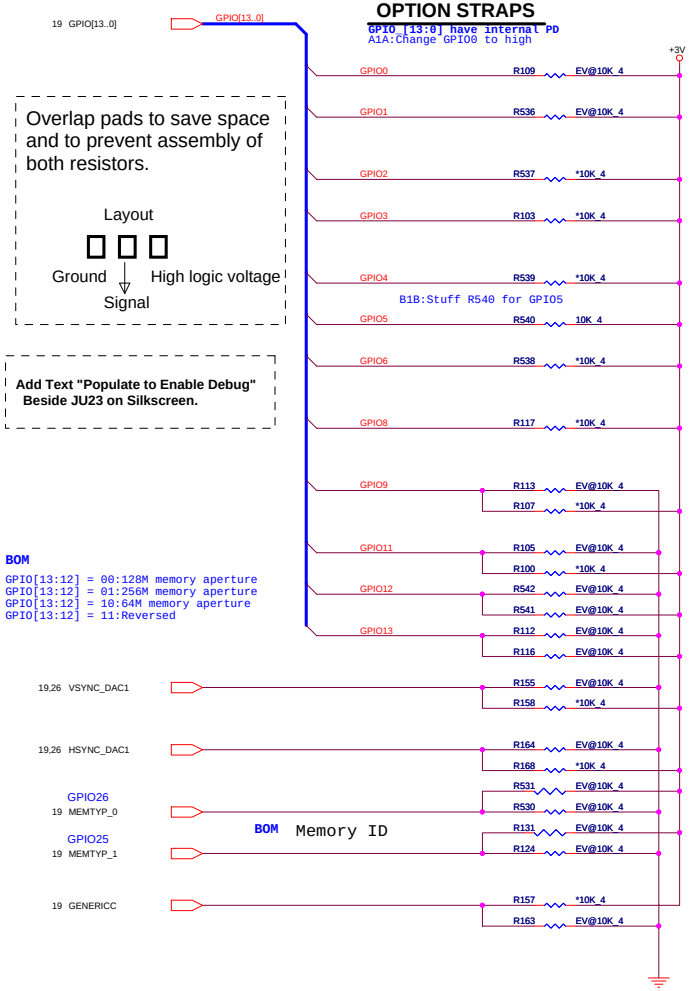
Reference voltage per channel (memory data/strobe)
MVREFD_[0:1] (0.7 * VDDR1) (for GDDR3)
MVREFS_[0:1] (0.7 * VDDR1) (for GDDR3)

PROJECT : ZC1		
Quanta Computer Inc.		
Size	Document Number: M56P 3/4 OF 7	Rev: 1A
Date: Friday, October 07, 2005	Sheet 22 of 46	

256/512 Mbit GDDRIII Channels A and B Rank 1



OPTION STRAPS



Overlap pads to save space and to prevent assembly of both resistors.

Layout

Ground High logic voltage

Signal

Add Text "Populate to Enable Debug" Beside JU23 on Silkscreen.

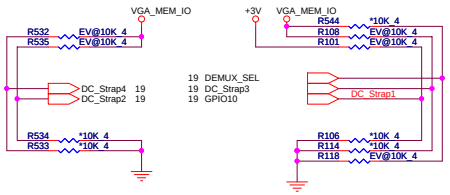
BOM

GPIO[13:12] = 00:128M memory aperture
GPIO[13:12] = 01:256M memory aperture
GPIO[13:12] = 10:64M memory aperture
GPIO[13:12] = 11:Reversed

BOM Memory ID

M56-P Strap

STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED
STRAP_B_PTX_PWRS_ENB	GPIO0	TRANSMITTER POWER SAVINGS ENABLE - FULL TX OUTPUT SWING	INSTALL 10K RESISTOR
STRAP_B_PTX_DEEMPH_EN	GPIO1	TRANSMITTER DE-EMPHASIS ENABLE FOR M26X, M56P: INSTALL WITH ATI RS480,RS480,RX480, RC410,RS482 CHIPSETS DO NOT INSTALL WITH INTEL 915PM CHIPSET FOR M5X - INSTALL	TBD
RSVD	GPIO(3:2)	NO ATI FEATURE ENABLED	DO NOT INSTALL 10K RESISTORS
REVERSE LANES DEBUG ACCESS	GPIO4	NO DEBUG ACCESS (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
STRAP_FORCE_COMPLIANCE RSVD	GPIO5	sets the desired PCIE PLL bandwidth for M5x parts	DO NOT INSTALL 10K RESISTOR
COMMON MODE RANGE	GPIO6	NO ATI FEATURE ENABLED (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
DEBUG ACCESS FORCE_COMPLIANCE	GPIO8	DON'T FORCE COMPLIANCE STATE(M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
ROMIDCFG(3:0) MEMORY APERTURE SIZE	GPIO(9,13:11)	IF NO ROM GPIO11(M26X) AND GPIO12,13(M52,M54,M56) SET MEMORY APERTURE SIZE 000x - No ROM, MEM_AP_SIZE=00(128MB) 001x - No ROM,MEM_AP_SIZE=01(256MB) 010x - No Rom, MEM_AP_SIZE=10(64MB) 011x - No ROM,MEM_AP_SIZE=11(Reserved) 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM **1100 - Serial M25P05 ROM (ST), chip IDis from ROM** 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	A1A:change ROMIDCFG(3:0) to 0010
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this pin low during reset. 0- Slave VIP host port deviced present. 1-No slave VIP port devices reporting presence during reset	No default
NO STRAP FUNCTION	H2SYNC, V2SYNC,GENERICC	ATI FEATURE NOT ENABLED (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
	VSYNC	RSVD	
	HSYNC	RSVD	
	PCIE_TEST	RSVD	



A1A:change video capture enable setting

Board Straps REV. 0.3

STRAPS	PIN	DESCRIPTION	VALUE
MEMTYPE(1:0)	GPIO25,26	MEMORY TYPE AND SPEED SELECT Memory connected to R420 identification for BIOS 00 - Samsung GDDR 3 memory(256Mb) 136 Ball BGA package 01 - Samsung GDDR 3 memory(512Mb) 136 Ball BGA package 10 - Infineon GDDR 3 memory(256Mb) 136 Ball BGA package 11 - Infineon GDDR 3 memory(512Mb) 136 Ball BGA package	00
DC_Strap1	GPIO(10)	Internal TMDS Enabled 0 - Disabled **1 - Enabled**	1
DC_Strap2	LCDDATA(13)	Video Capture Enabled **0 - Disabled** 1 - Enabled	1
DC_Strap3	LCDDATA(14)	HDTV out detect 0 - Detected **1 - Not detected**	1
DC_Strap4, DEMUX_SEL	LCDDATA(15,19)	Video capture enable 00 - DAC2 Off 01 - DAC2 On as CRT **10 - DAC2 On as TVOUT** 11 - DAC2 On as TVOUT and CRT	10
PAL/NTSC	LCDDATA(18)	TVO Standard Default (Resistor pull-up and switch short to GND) **0 - PAL (on board resistor pull-down and switch closed)** **1 -NTSC (on board resistor pull-up)**	1

MEMORY TYPE AND SPEED SELECT

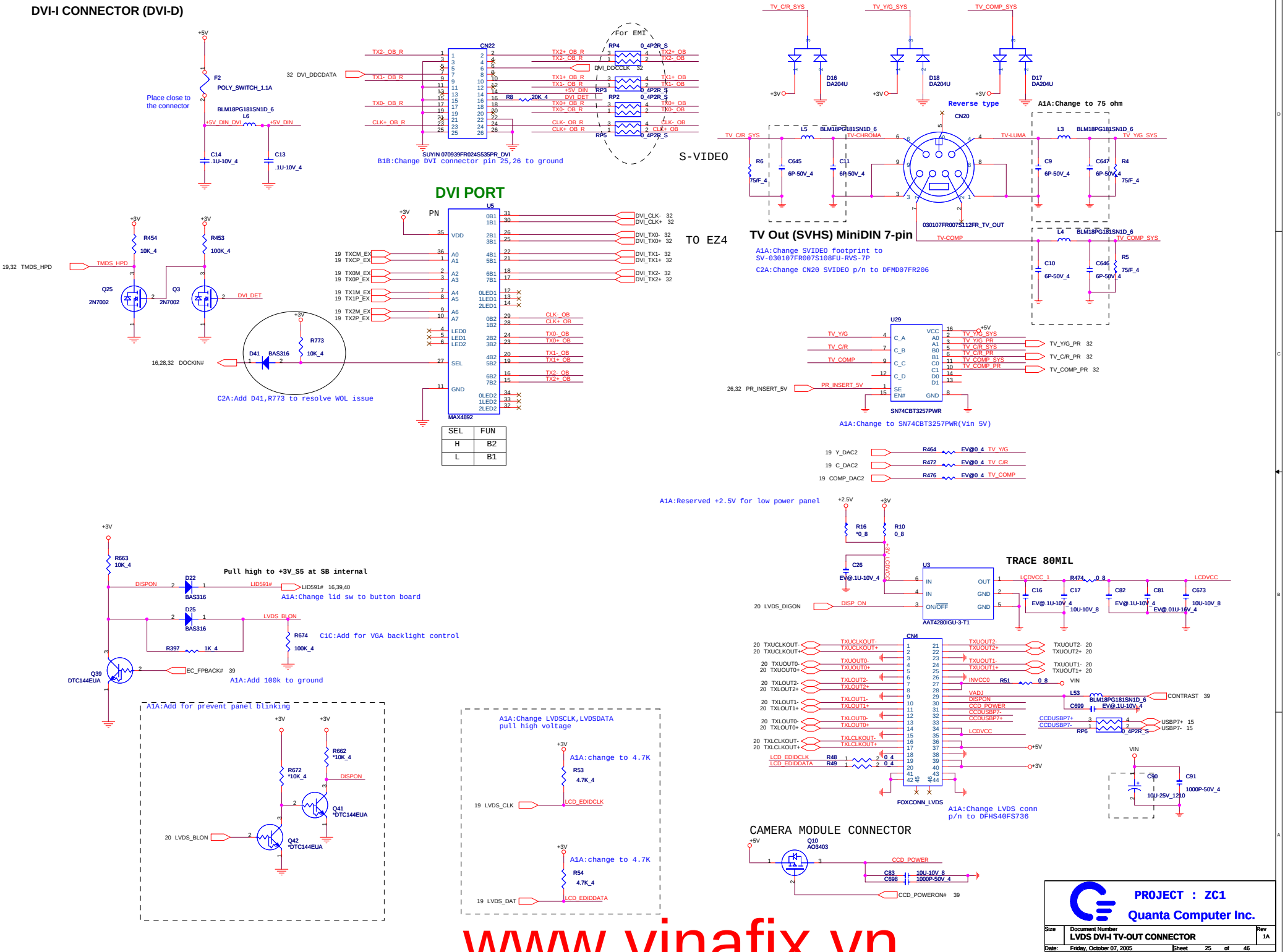
PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	M56P OPTION STRAPS	1A

Date: Friday, October 07, 2005 Sheet 24 of 46

DVI-I CONNECTOR (DVI-D)

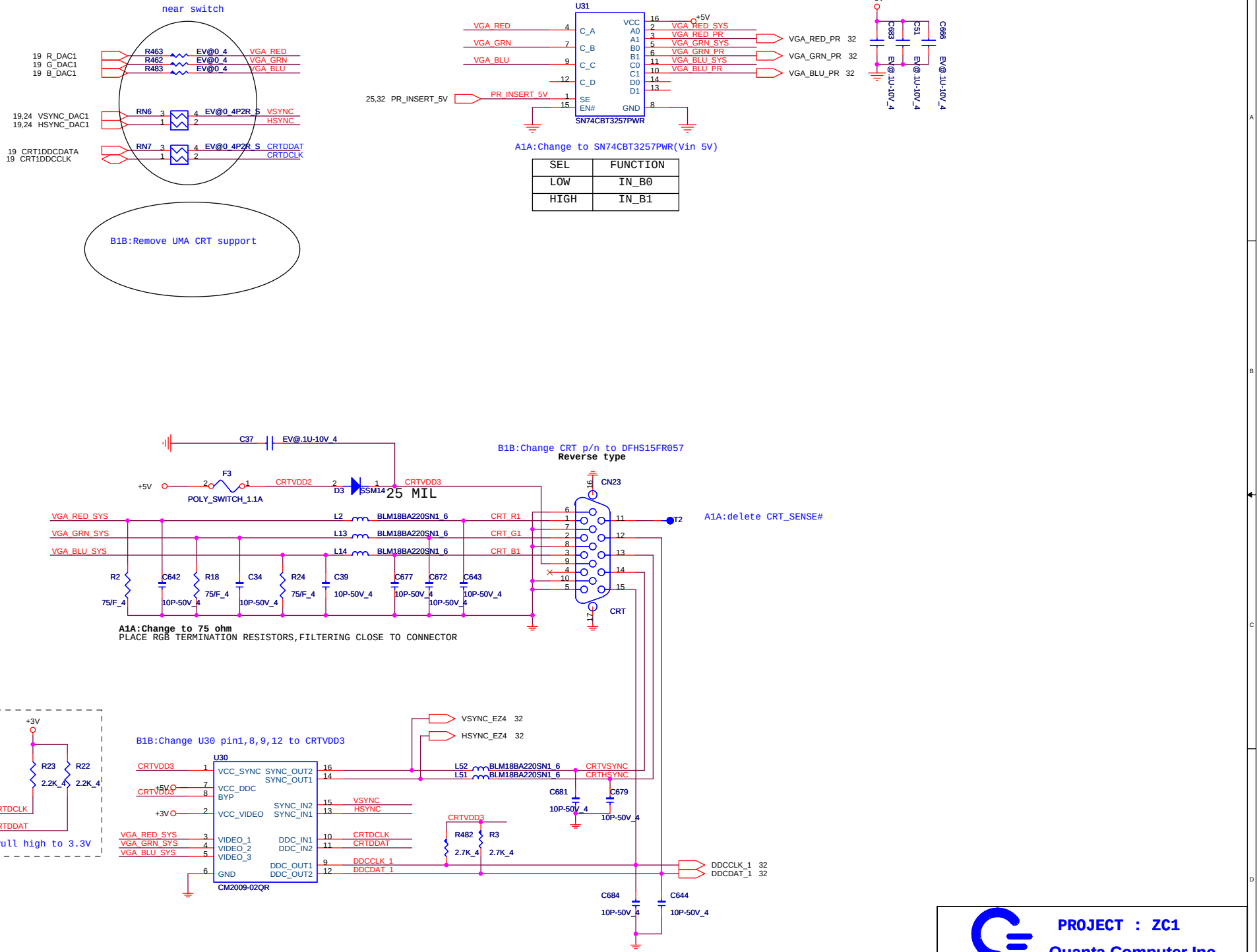


PROJECT : ZC1

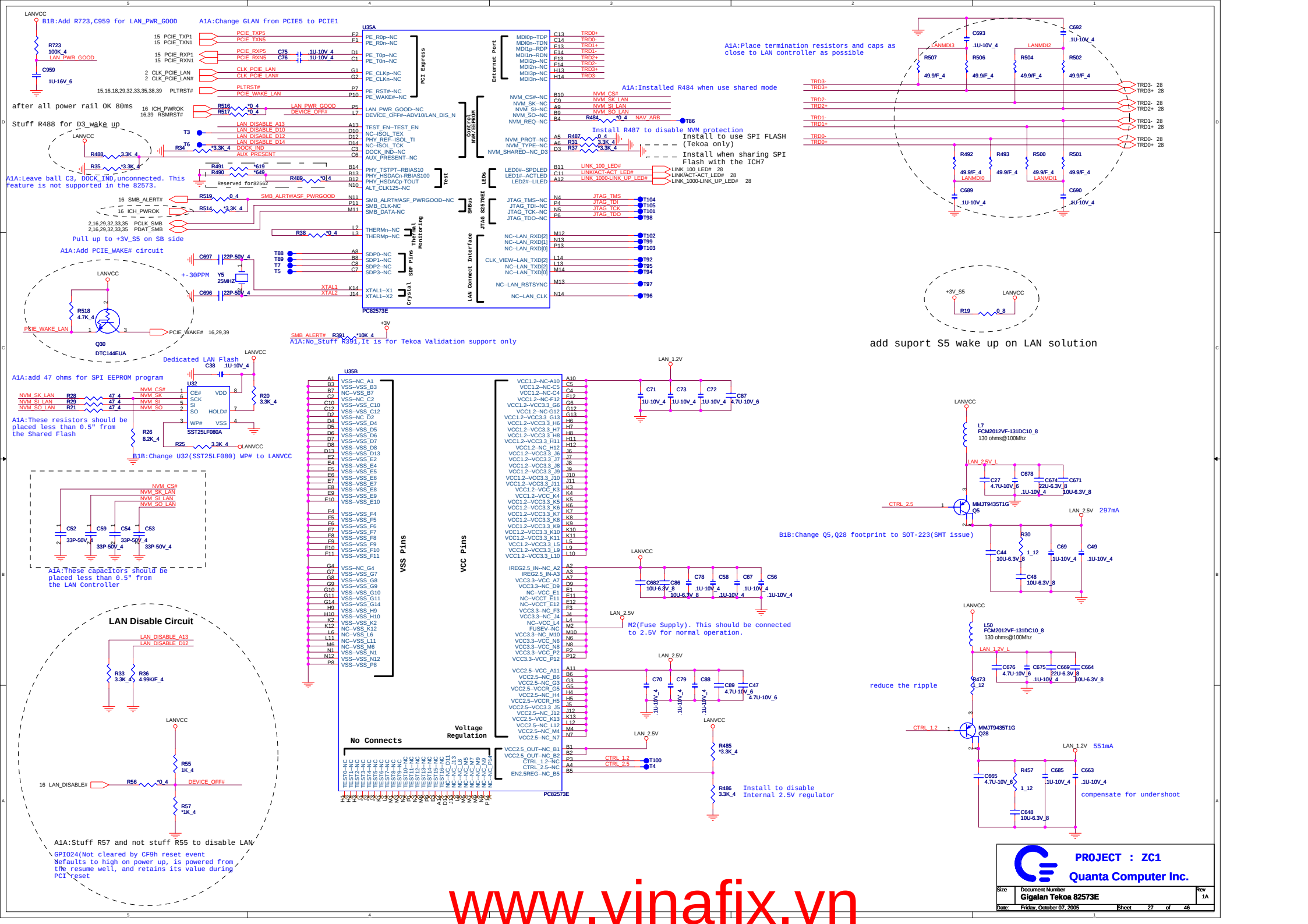
Quanta Computer Inc.

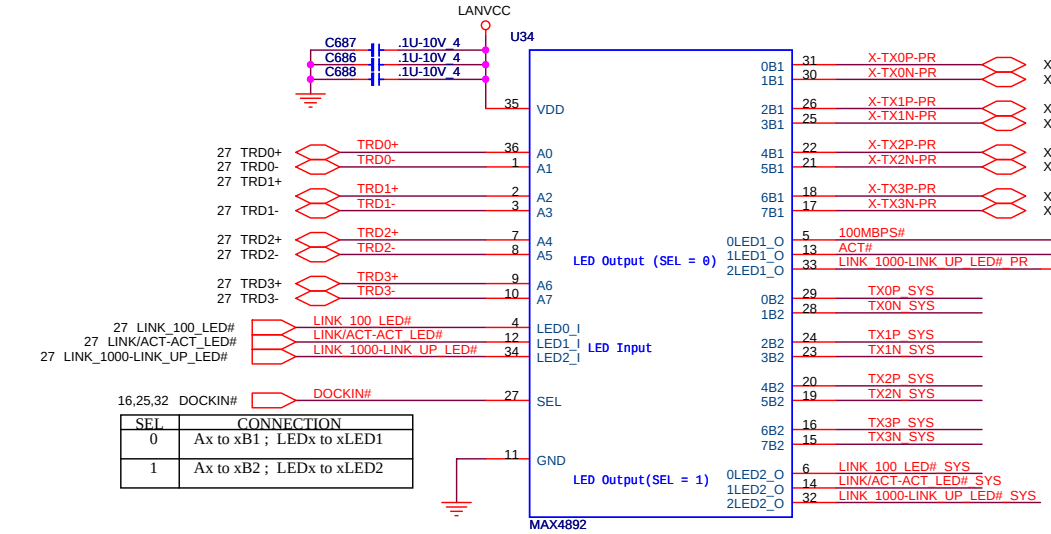
Size	Document Number	Rev
	LVDS DVI-I TV-OUT CONNECTOR	1A

Date: Friday, October 07, 2005 Sheet 25 of 46



PROJECT : ZC1	Quanta Computer Inc.
Size	Document Number: CRT-PORT — Rev: 1A
Date: Friday, October 07, 2005	Sheet 26 of 46


B1B:Add R723,C959 for LAN_PWR_GOOD
A1A:Change GLAN from PCIE5 to PCIE1
U35A
PCIE_TXP5
PCIE_TXN5
PCIE_RXP5
PCIE_RXN5
C75 .1U-10V_4
C76 .1U-10V_4
CLK_PCIE_LAN
CLK_PCIE_LAN#
PLTRST#
PCIE_WAKE_LAN
PCI Express
Enternet Port
MDI0p--TDP
MDI0n--TDN
MDI1p--RDP
MDI1n--RDN
MDI2p--NC
MDI2n--NC
MDI3p--NC
MDI3n--NC
TRD0+
TRD0-
TRD1+
TRD1-
TRD2+
TRD2-
TRD3+
TRD3-
after all power rail OK 80ms
Stuff R488 for D3_wake up
LAN_PWR_GOOD
DEVICE_OFF#
LAN_DISABLE_A13
LAN_DISABLE_D10
LAN_DISABLE_D12
LAN_DISABLE_D14
DOCK_IND
AUX_PRESENT
LAN_PWR_GOOD--NC
DEVICE_OFF#--ADV10/LAN_DIS_N
TEST_EN--TEST_EN
NC--ISOL_TEX
PHY_REF--ISOL_TI
NC--ISOL_TCK
DOCK_IND--NC
AUX_PRESENT--NC
Control NVM/EEPROM
NVM_CS#--NC
NVM_SK--NC
NVM_SI--NC
NVM_SO--NC
NVM_REQ--NC
NVM_PROT--NC
NVM_TYPE--NC
NVM_SHARED--NC_D3
NVM_CS#
NVM_SK_LAN
NVM_SI_LAN
NVM_SO_LAN
NAV_ARB
T86
A1A:Installed R484 when use shared mode
Install R487 to disable NVM protection
Install to use SPI FLASH (Tekoa only)
Install when sharing SPI Flash with the ICH7
A1A:Leave ball C3, DOCK_IND unconnected. This feature is not supported in the 82573.
Reserved for82562
Test
PHY_TSTPT--RBIAS10
PHY_HSDACn-RBIAS100
PHY_HSDACp-TOUT
ALT_CLK125--NC
LEDs
LED0#--SPDLED
LED1#--ACTLED
LED2#--LILED
LINK_100_LED#
LINK/ACT-ACT_LED#
LINK_1000-LINK_UP_LED#
SMBus
SMB_ALRT#/ASF_PWRGOOD--NC
SMB_CLK--NC
SMB_DATA--NC
SMB_ALRT#/ASF_PWRGOOD
Pull up to +3V_S5 on SB side
Thermal Monitoring
THERMn--NC
THERMp--NC
SDP Pins
SDP0--NC
SDP1--NC
SDP2--NC
SDP3--NC
Crystal
XTAL1--X1
XTAL2--X2
+-30PPM
25MHZ
JTAG 82570EI
JTAG_TMS--NC
JTAG_TDI--NC
JTAG_TCK--NC
JTAG_TDO--NC
JTAG_TMS
JTAG_TDI
JTAG_TCK
JTAG_TDO
LAN Connect Interface
NC--LAN_RXD[2]
NC--LAN_RXD[1]
NC--LAN_RXD[0]
NC--LAN_TXD[2]
NC--LAN_TXD[1]
NC--LAN_TXD[0]
NC--LAN_RSTSYNC
NC--LAN_CLK
T104
T105
T101
T98
T102
T99
T103
T92
T95
T94
T97
T96
PC82573E
A1A:Add PCIE_WAKE# circuit
PCIE_WAKE_LAN
PCIE_WAKE#
Q30
DTC144EUA
A1A:No_Stuff R391,It is for Tekoa Validation support only
A1A:Place termination resistors and caps as close to LAN controller as possible
add suport S5 wake up on LAN solution
Dedicated LAN Flash
A1A:add 47 ohms for SPI EEPROM program
A1A:These resistors should be placed less than 0.5" from the Shared Flash
U32
SST25LF080A
B1B:Change U32(SST25LF080) WP# to LANVCC
A1A:These capacitors should be placed less than 0.5" from the LAN Controller
U35B
VSS Pins
VCC Pins
No Connects
Voltage Regulation
LAN_1.2V
LAN_2.5V
M2(Fuse Supply). This should be connected to 2.5V for normal operation.
B1B:Change Q5,Q28 footprint to SOT-223(SMT issue)
LAN_2.5V 297mA
LAN_1.2V 551mA
reduce the ripple
compensate for undershoot
LAN Disable Circuit
A1A:Stuff R57 and not stuff R55 to disable LAN
GPIO24(Not cleared by CF9h reset event
Defaults to high on power up, is powered from the resume well, and retains its value during PCI reset
Install to disable Internal 2.5V regulator
PROJECT : ZC1
Quanta Computer Inc.
Gigalan Tekoa 82573E
Friday, October 07, 2005
Sheet 27 of 46
www.vinafix.vn

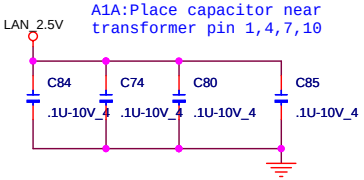


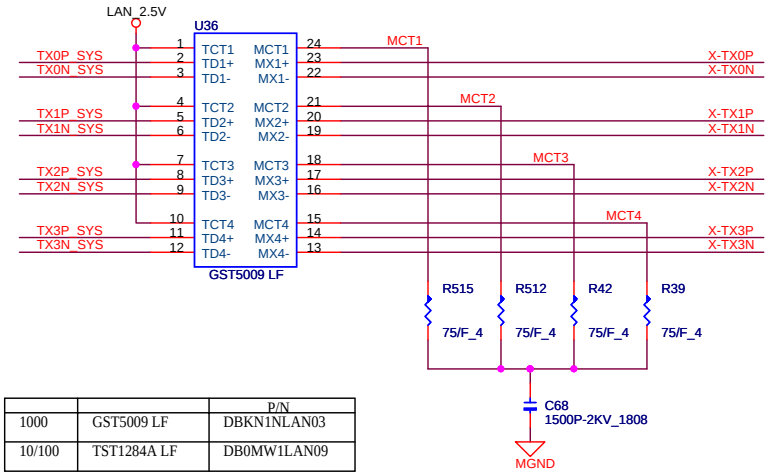
SEL	CONNECTION
0	Ax to xB1 ; LEDx to xLED1
1	Ax to xB2 ; LEDx to xLED2

LED0 Input
0LED1 Output. Connects LED0 to 0LED1 when SEL = 0.
0LED2 Output. Connects LED0 to 0LED2 when SEL = 1.

B1B:Change MAX4892 pin define

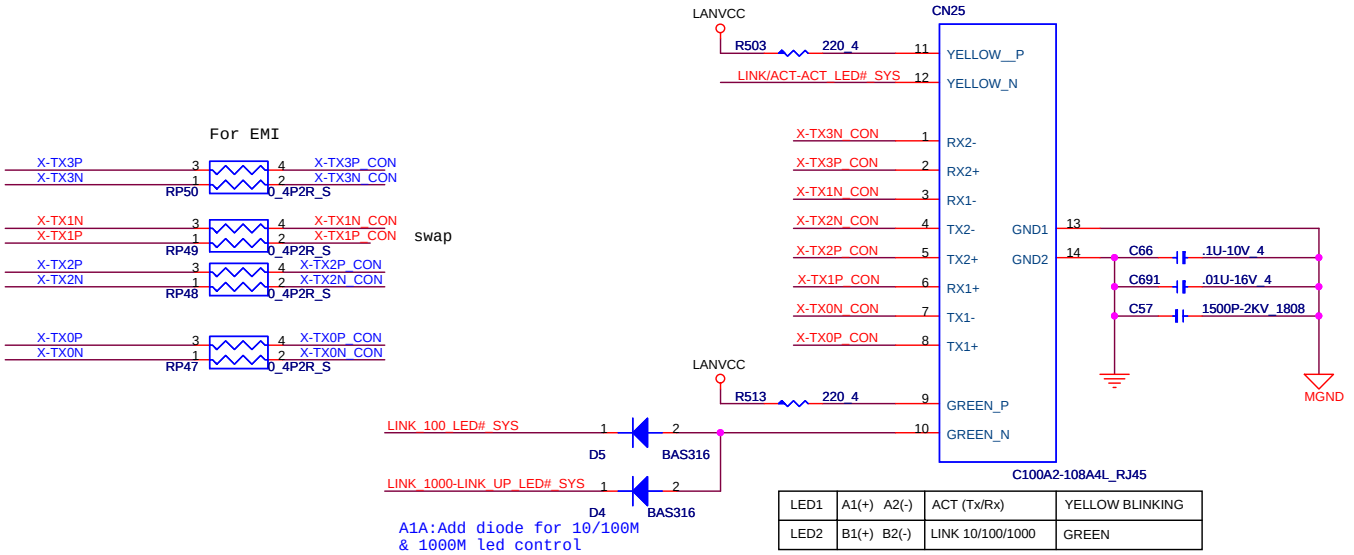
A1A:Place capacitor near transformer pin 1,4,7,10





		P/N
1000	GST5009 LF	DBKN1NLAN03
10/100	TST1284A LF	DB0MW1LAN09

A1A:Change RJ45 CONN to C100A2-108A4L
A1A:Change RJ45 TX,RX pin define



A1A:Add diode for 10/100M & 1000M led control

LED1	A1(+) A2(-)	ACT (Tx/Rx)	YELLOW BLINKING
LED2	B1(+) B2(-)	LINK 10/100/1000	GREEN

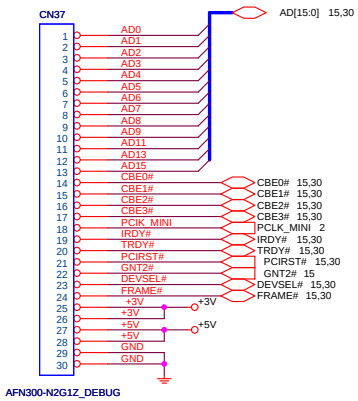
PROJECT : ZC1
Quanta Computer Inc.

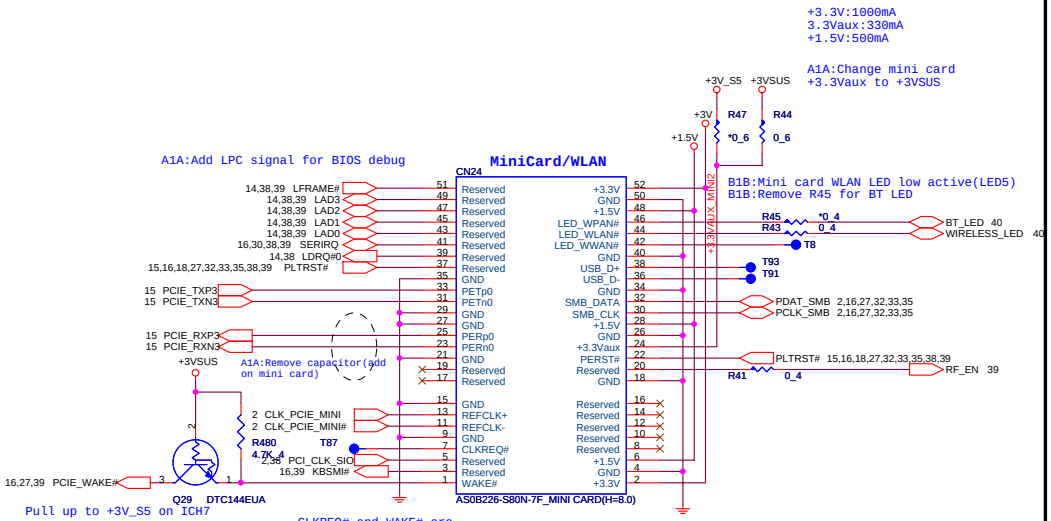
Size	Document Number	Rev
	TRANSFORMER/RJ45	A

Date: Friday, October 07, 2005 Sheet 28 of 46

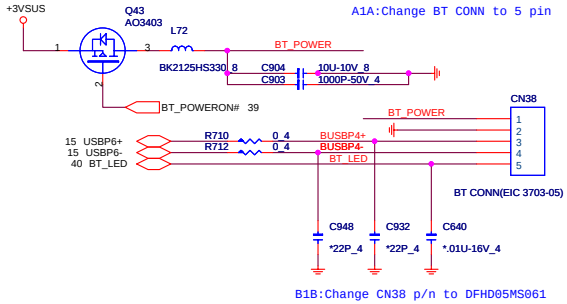
Debug card interface

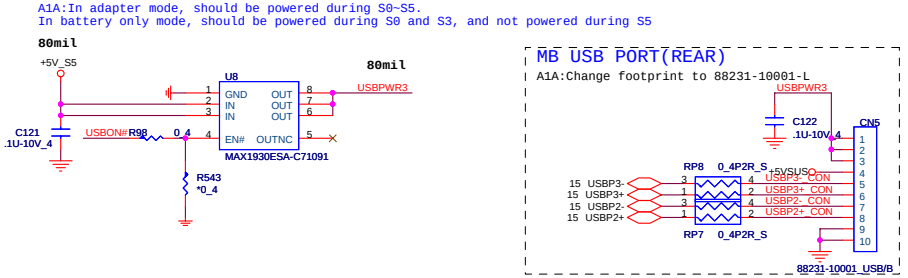
BOT contact

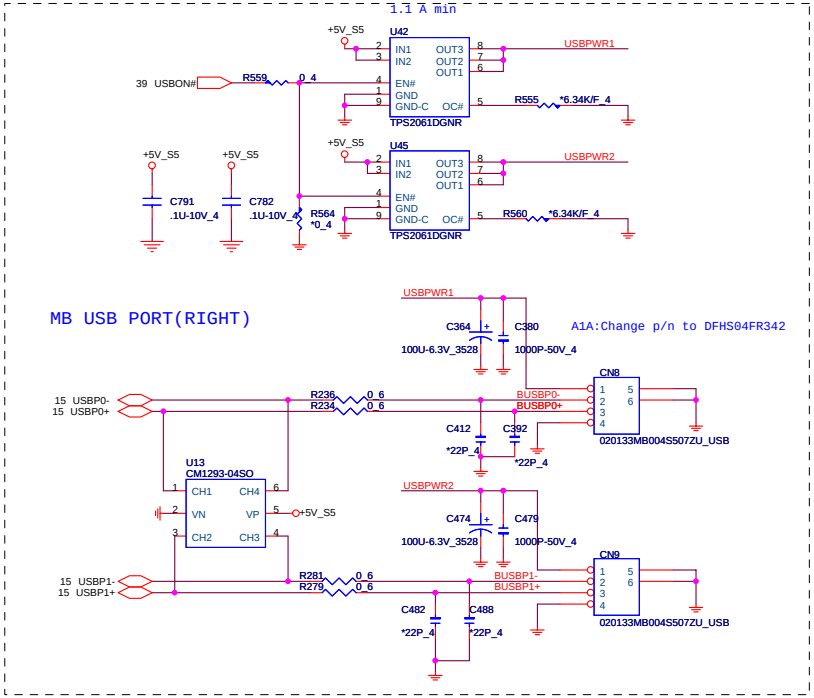




BLUETOOTH MODULE CONNECTOR



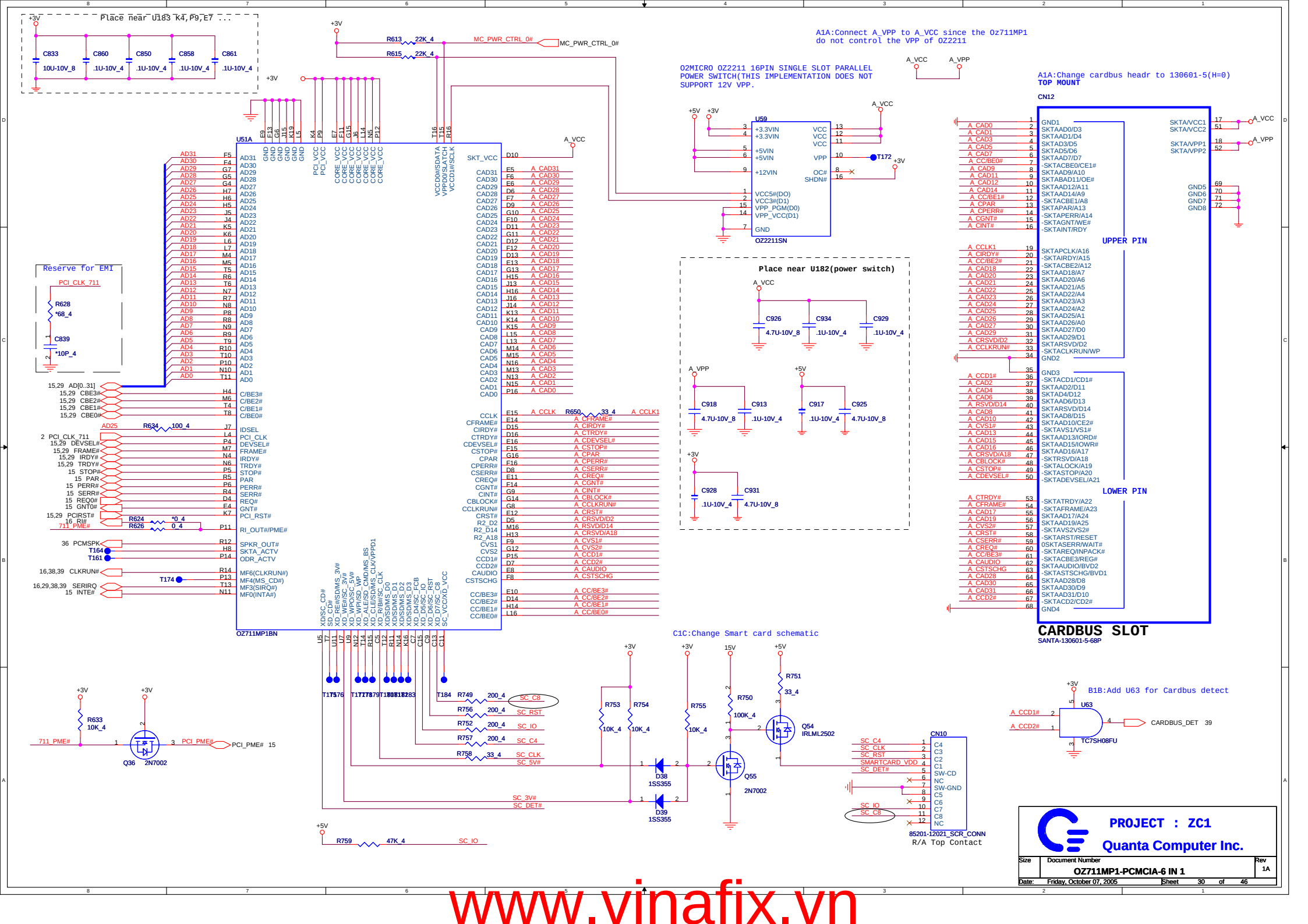




PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	DEBUG CARD&PCI-E card&USB	1A
Date: Friday, October 07, 2005	Sheet 29 of 46	


Place near U183 K4,P9,E7 ...
C833 10U-10V_8
C860 .1U-10V_4
C850 .1U-10V_4
C858 .1U-10V_4
C861 .1U-10V_4
A1A:Connect A_VPP to A_VCC since the Oz711MP1 do not control the VPP of OZ2211
O2MICRO OZ2211 16PIN SINGLE SLOT PARALLEL POWER SWITCH(THIS IMPLEMENTATION DOES NOT SUPPORT 12V VPP.
A1A:Change cardbus headr to 130601-5(H=0)
TOP MOUNT
CN12
U51A
OZ711MP1BN
OZ2211SN
U59
Reserve for EMI
Place near U182(power switch)
UPPER PIN
LOWER PIN
CARDBUS SLOT
SANTA-130601-5-68P
C1C:Change Smart card schematic
B1B:Add U63 for Cardbus detect
CN10
85201-12021_SCR_CONN
R/A Top Contact
PROJECT : ZC1
Quanta Computer Inc.
OZ711MP1-PCMCIA-6 IN 1
Friday, October 07, 2005
www.vinafix.vn

A1A:1394 function of OZ711MP1 do not used the EEPROM , and Oz711MP1 put the GUID in PCI register , So , 24Lc02BT can be remove

U51B

OZ711MP1BN

A1A:Change the C1885 filter Cap value from 270 pf to 820 pf

CN16

020204FR004S5022L_1394 CONN

A1A:Change1394 footprint to 1394-020204fr004s502zx-c-4p-v

B1B:Change pin 7,8 to GND

B1B:Change 1394 p/n to DFHS04FS578

Group 1 and 2 not populated:
Firmware in Internal ROM
No unique serial number

Group 2 populated:
Firmware in External FLASH
Unique serial number and configuration in FLASH

External FLASH

U49

SST39VF010-70-4C-WHE

Check GPIO Pin & Det

SD/MMC

MS/MS pro

SM/xD

CN14

R013-000-XX_CARD READER

6 IN1 CARD READER
(MS,MS pro,SD, MMC,xD,SDIO)

Group 1 populated:
Firmware in Internal ROM
Unique serial number and configuration in EEPROM

External EEPROM

U16

*AT93C66A-10TU-2.7(TSSOP)

5pF attached to SD_D0 and GND for 48M compatibility issue

External xD resistors

U1

USB2228-NU-XX_VTQFP128

Check USB2.0 Power

Place C567 at pin 100, C542 at pin 108, and C524 at pin 89.

20 mil

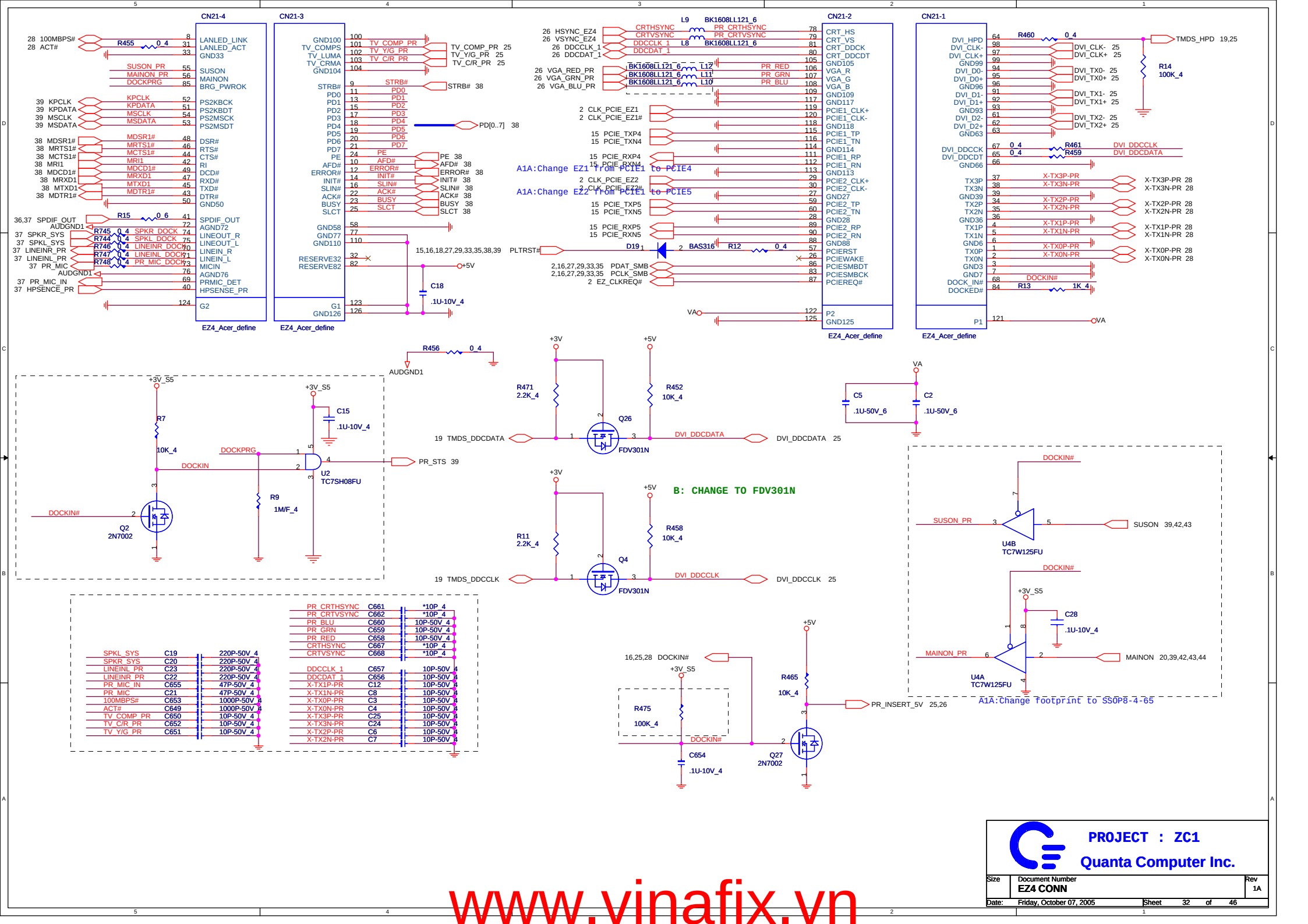
20 mil

20 mil

PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	OZ711MP1-IEEE1394-SMART CARD	1A
Date: Friday, October 07, 2005	Sheet 31 of 46	


CN21-4
CN21-3
CN21-2
CN21-1
EZ4_Acer_define
A1A:Change EZ1 from PCIE1 to PCIE4
A1A:Change EZ2 from PCIE1 to PCIE5
B: CHANGE TO FDV301N
A1A:Change footprint to SSOP8-4-65
PROJECT : ZC1
Quanta Computer Inc.
EZ4 CONN
Friday, October 07, 2005
www.vinafix.vn

+NEW_1.5V Max. 650mA, Average 500mA.
+NEW_3V Max. 1300mA, Average 1000mA.

A1A:Change New card power sw to Oz27c10

A1A:Change New card to small type(130832-1)

U20

ExpressSwitch

R5538D001-TR-F/OZ27C10LN

Place near U20

Place near U20

Place near CN35

CN35

Reverse

130832-1_NEW CARD

TPM

CPU

MDC

POWER/B

MINI CARD

Thermal module

B1B:Change HOLE8,27 footprint

PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	NEW CARD &HOLE	C

Date: Friday, October 07, 2005 Sheet 33 of 46

SATA TO PATA

U50
SPIF3811-HV096
64pin QFN
PH@SPIF3811_QFN64

Stuff all when use ULI M5285

A1A:Change p/n to AL003811010

Close to power pins(pin4,17,44,52) Close to power pins(pin9,41,56)

Unstuff R629 when use ULI M5285

SATA AC coupling is 0.01UF

145mA

Unstuff R366 when use ULI M5285

Stuff L448, C568 when use ULI M5285

Stuff_R374, R653 when use ULI M5285

Unstuff R382, R651, R652 when use ULI M5285

A1A:Change Pin 21 (DD_DISABLE#) 10K ohm PU to +3.3V

A1A:Add 1UF for SYS_RESET
B2B:Unstuff C595 when use SPIF3811

close to IDE Connector

Stuff all when use ULI M5285

1.8 V Supply current for PHY blocks 120 mA
1.8 V Supply current for core logic 90 mA
3.3 V Supply current (for I/O) 55 mA

Reference clock select

ATAIOEN	Note
0	disable PATA output
1	enable PATA output

Operation Mode

MODE[2..0]	
0 0 0	Device mode 100MB/S
0 0 1	Device mode 133MB/S
0 1 0	**Device mode 150MB/S**
0 1 1	RESERVE
1 0 0	Host mode 100MB/S
1 0 1	Host mode 133MB/S
1 1 0	Host mode 150MB/S
1 1 1	RESERVED

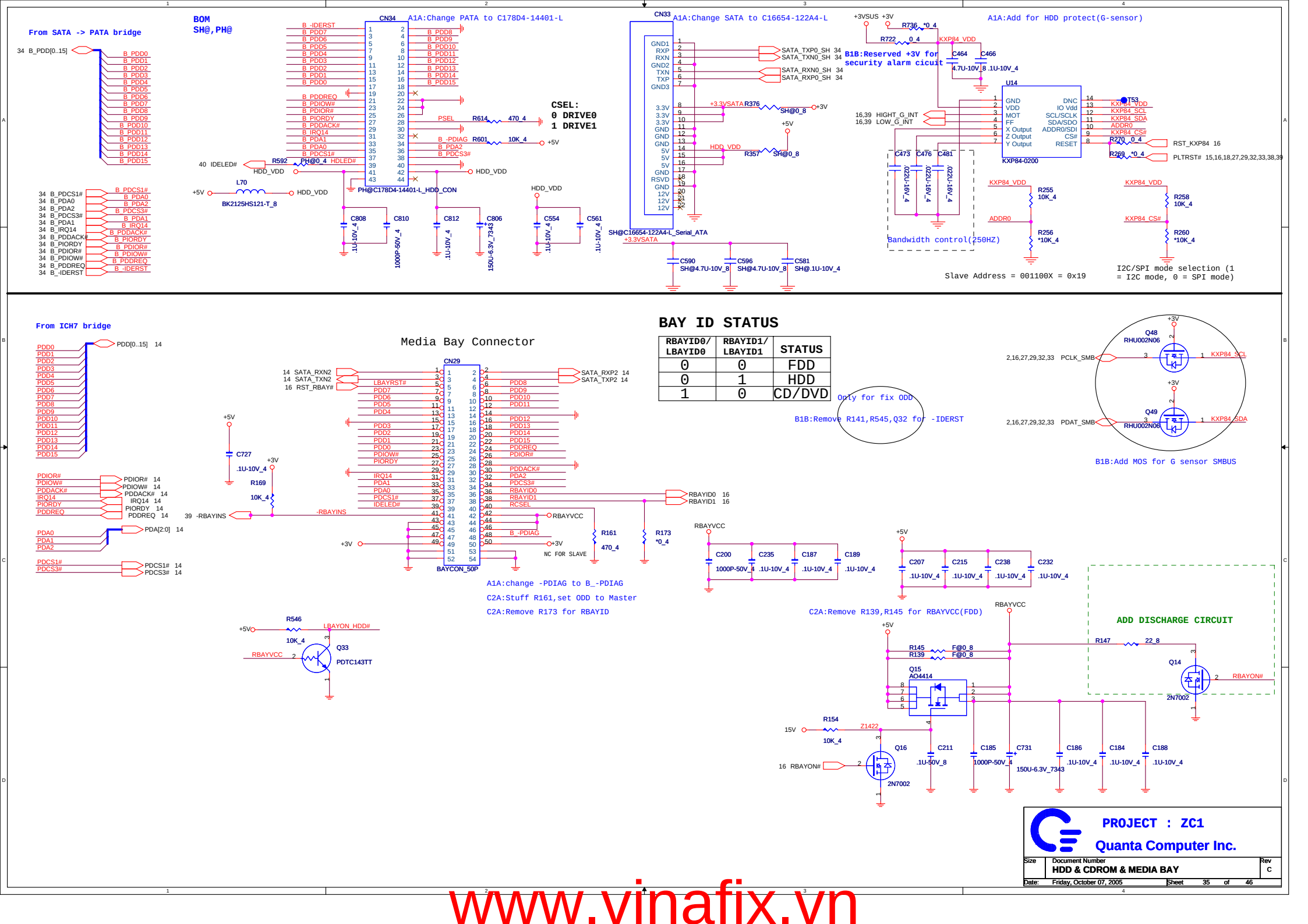
Reference clock select

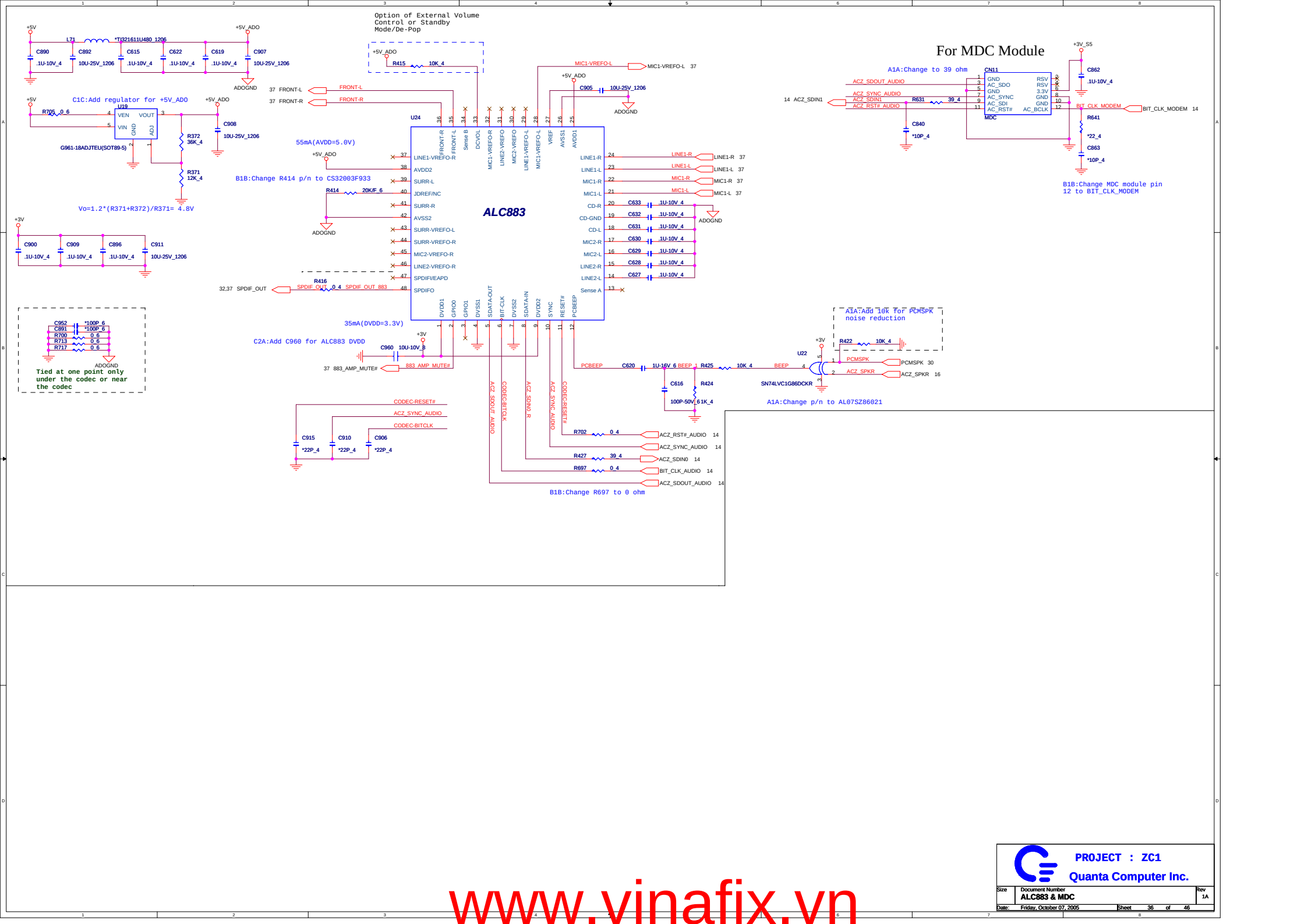
CLKSEL[1..0]	External clock
0 0	20 MHZ
0 1	**25 MHZ**

PROJECT : ZC1
Quanta Computer Inc.

Size	Document Number	Rev
	SATA/PATA	A

Date: Monday, October 03, 2005 Sheet 34 of 46





Audio amplifier

A1A:Change audio amplifier to MAX9750
A1A:Change footprint to tqfn28-5x5-5-33p

Low--->Speak Mode
Hi ---->HP

GAIN2	GAIN1	SPKR MODE	HP MODE
0	0	6	0
0	1	7.5	
1	0	9	3
1	1	10.5	

LINE OUT/SPDIF

BLACK

HPPLG#:
HP not insert->H
HP insert->L

Pin5 connect to
Pin3 on Jack

C2A:Change Line out schematic

C2A:Change Line out schematic

LINE IN

BLUE

MIC

PINK

SPEAKER CONNECTOR

A1A:Change Speaker conn footprint

B1B:Change speaker p/n to DFHD04MR701

SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1

C1C:Reversed for ESD(MIC)

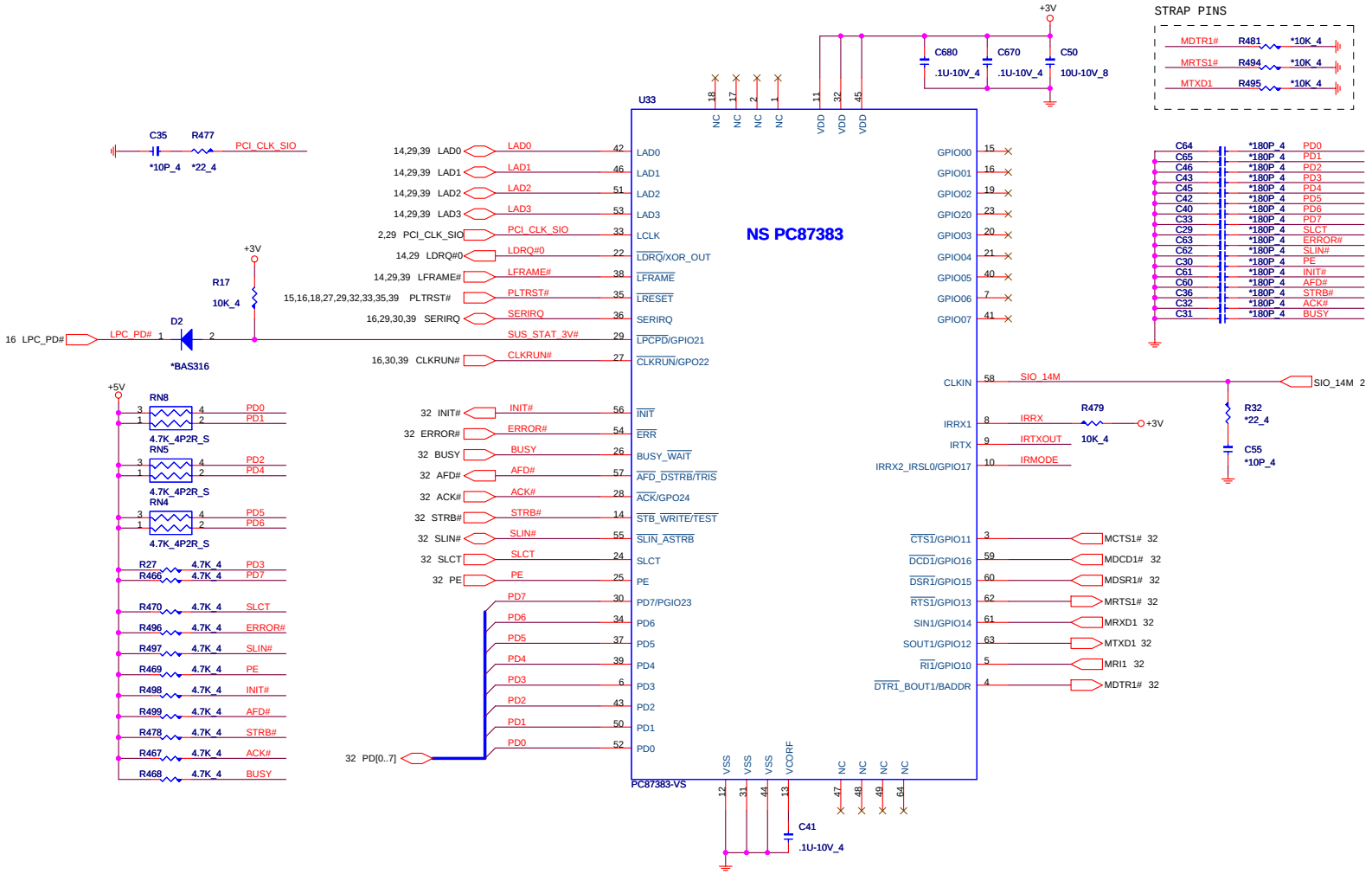
For ESD close to audio out connecter

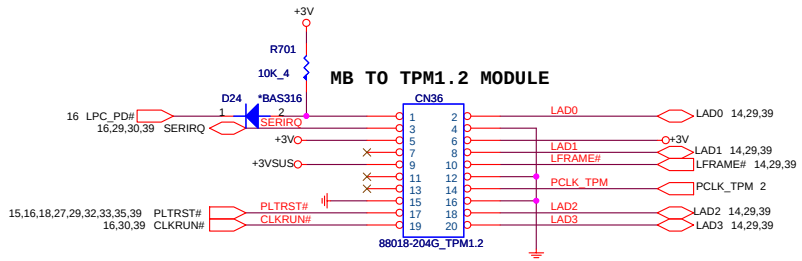
For ESD close to audio out connecter

PROJECT : ZC1
Quanta Computer Inc.

Size	Document Number	Rev
	AUDIO AMP(MAX9750) / JACK	1A

Date: Friday, October 07, 2005 Sheet 37 of 46

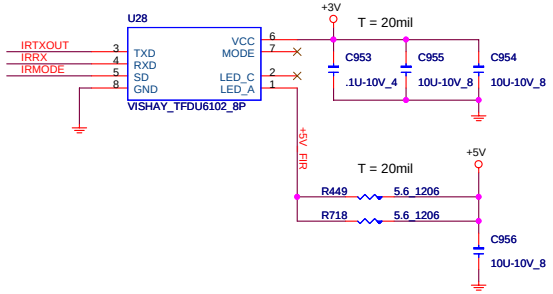




A1A:Change TPM CONN to 88018-204G(Pitch=0.8,H=2.65)

B1B:Change TPM pin define to same as ZH2

B1B:Change TPM connector p/n to



PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	SIO (87383),TPM 1.2	1A
Date: Friday, October 07, 2005	Sheet 38 of 46	

Adapter ID	
Watt	Voltage
65W	0.66 +/- 0.1V
90W	1.32 +/- 0.1V
135W	1.98 +/- 0.1V
150W	2.64 +/- 0.1V
Un-define	3.3 +/- 0.1V

Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.

I/O Address		
BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	

LDRQ#(pin 8) internal is no use

A1A:Reserved GSENSOR-X/Y/Z for security alarm cicuit

A1A:Remove REFON pin (DA3 pin 102)

A1A:Reserved for G-sensor

B1B:Add for Cardbus detect

C2A:Change EC_FPBACK# to IOPC2

SST 1MB BIOS (AKE35ZAKK17)

ST Micro M29W008AB/AMD-29LV081B/SST39VF080

B1B:Reversed for G sensor buzzer

A1A:Reserved for debug use

B1B:Change SW4 p/n to DHP00BB1J03

FOR 97551 ONLY

INTERNAL PULLUP IN SB

BIU configuration should match flash speed used

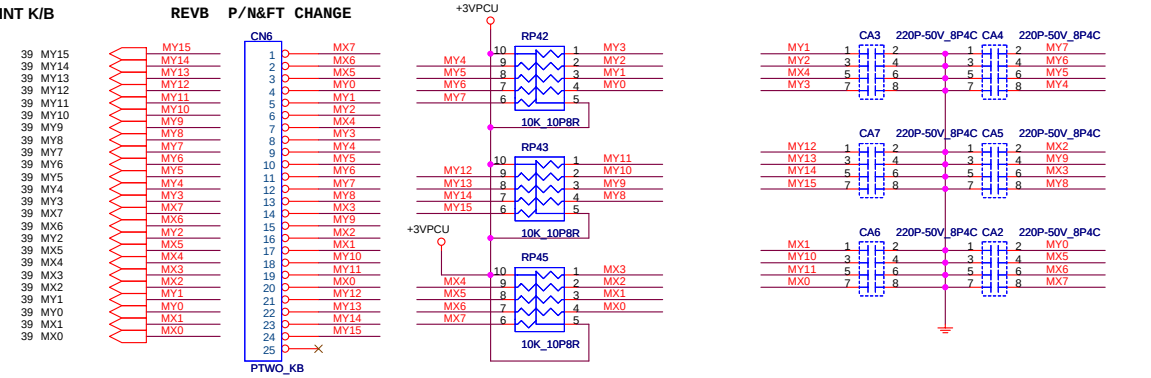
PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	97551 & FLASH	1A
Date: Friday, October 07, 2005	Sheet 39 of 46	

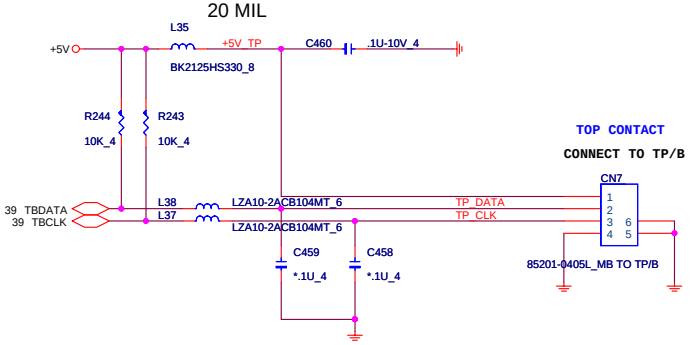
INT K/B

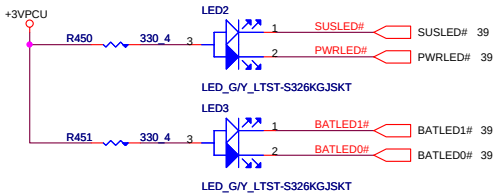
REVB P/N&FT CHANGE



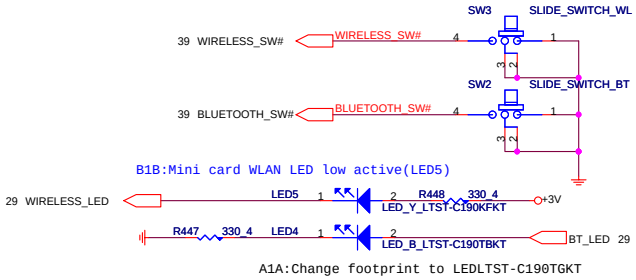
TOUCH PAD

20 MIL

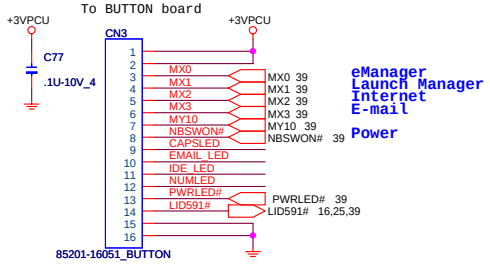


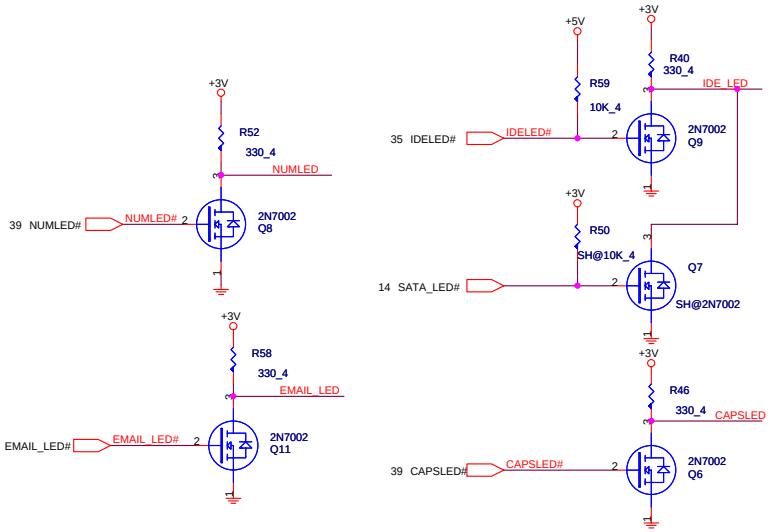


A1A:Change SW p/n



To BUTTON board



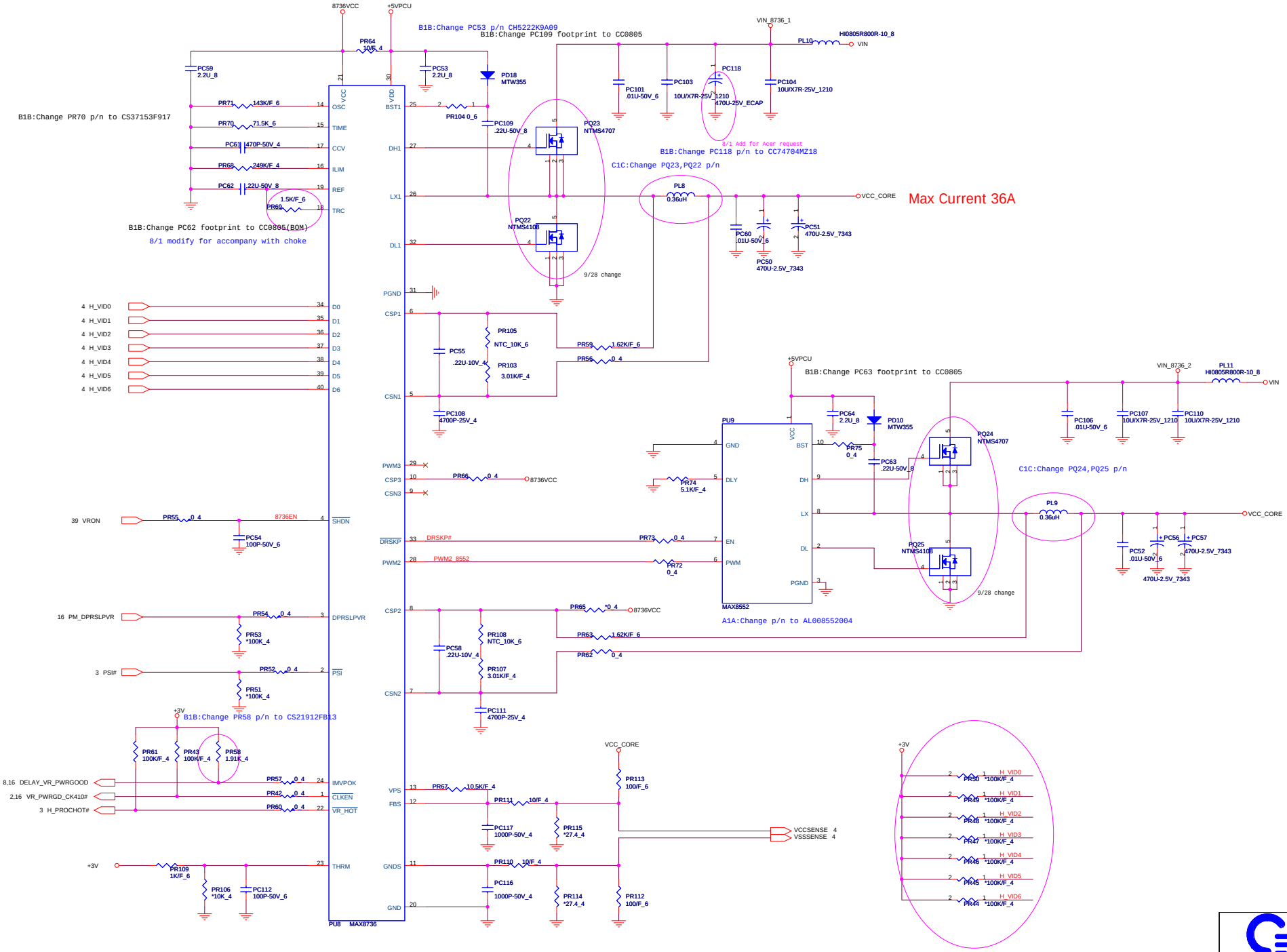


PROJECT : ZC1

Quanta Computer Inc.

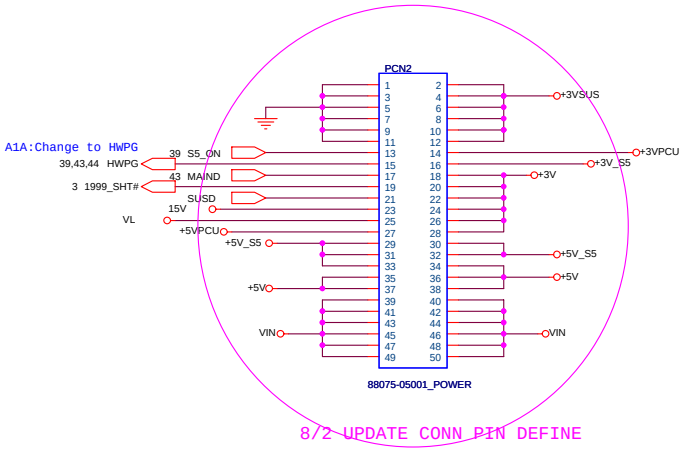
Size	Document Number	Rev
	SWITCH,LED,K/B,TP	1A

Date: Friday, October 07, 2005 Sheet 40 of 46



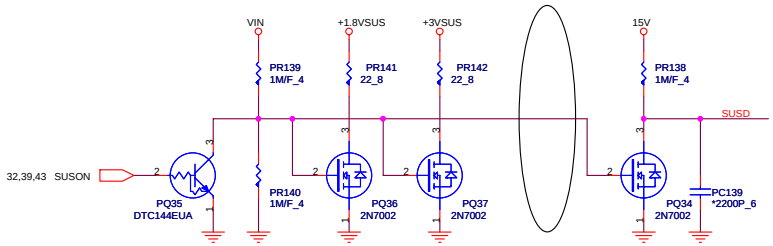
PROJECT : ZC1
Quanta Computer Inc.

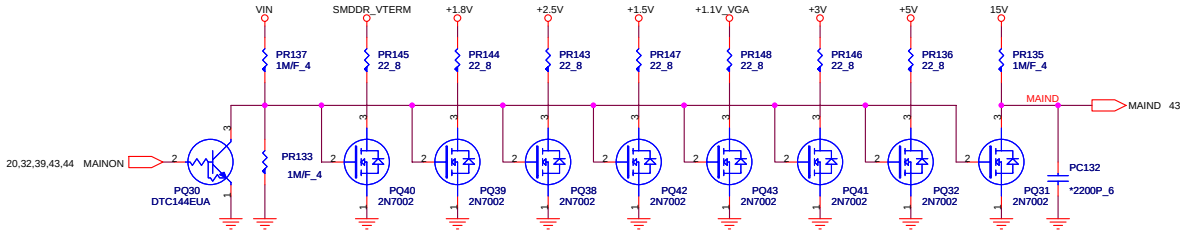
Size	Document Number	Rev
	VCORE (MAX8736)	1A
Date: Friday, October 07, 2005	Sheet 41 of 46	



8/2 UPDATE CONN PIN DEFINE

A1A:Del +5VSUS discharge

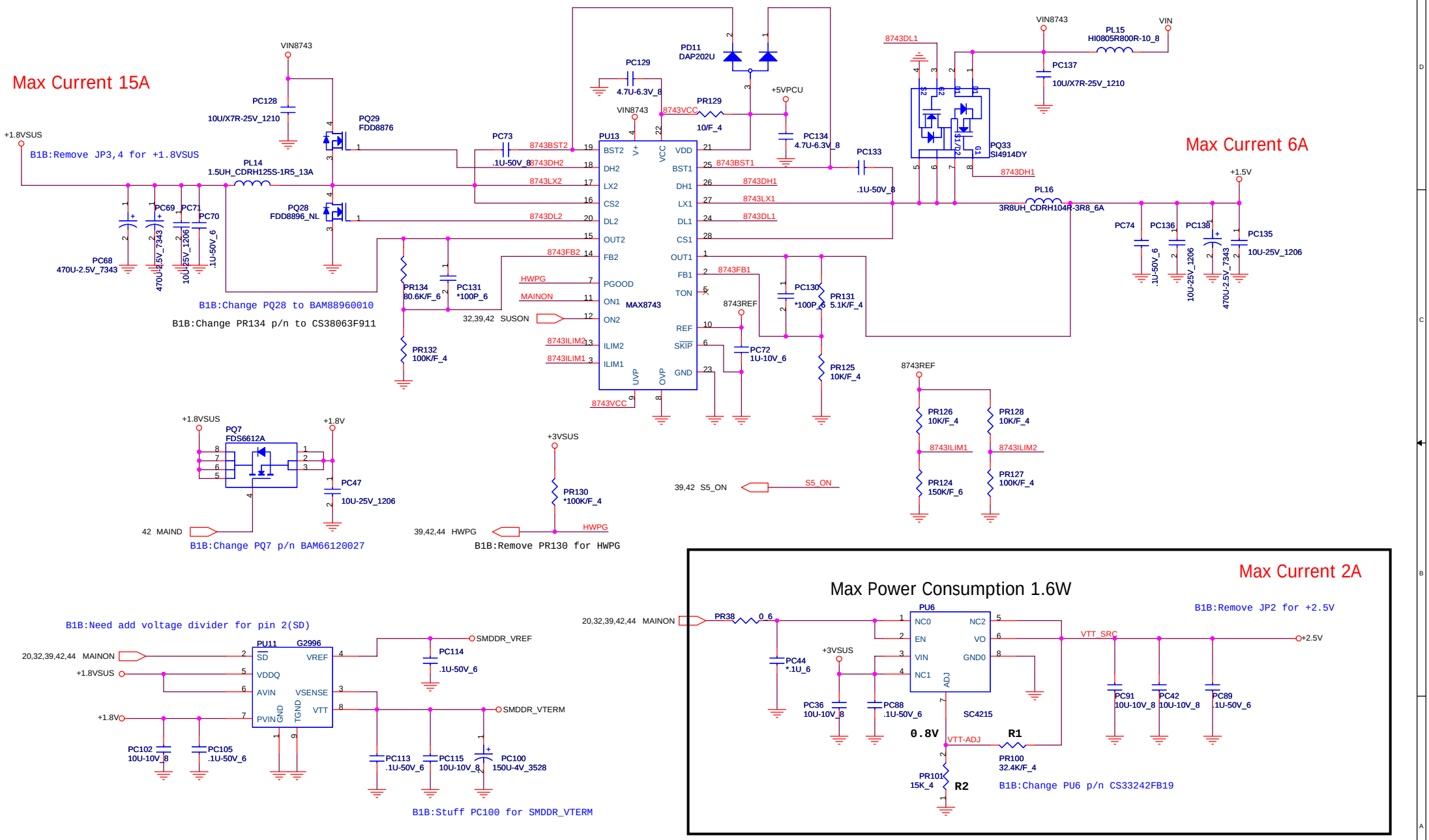


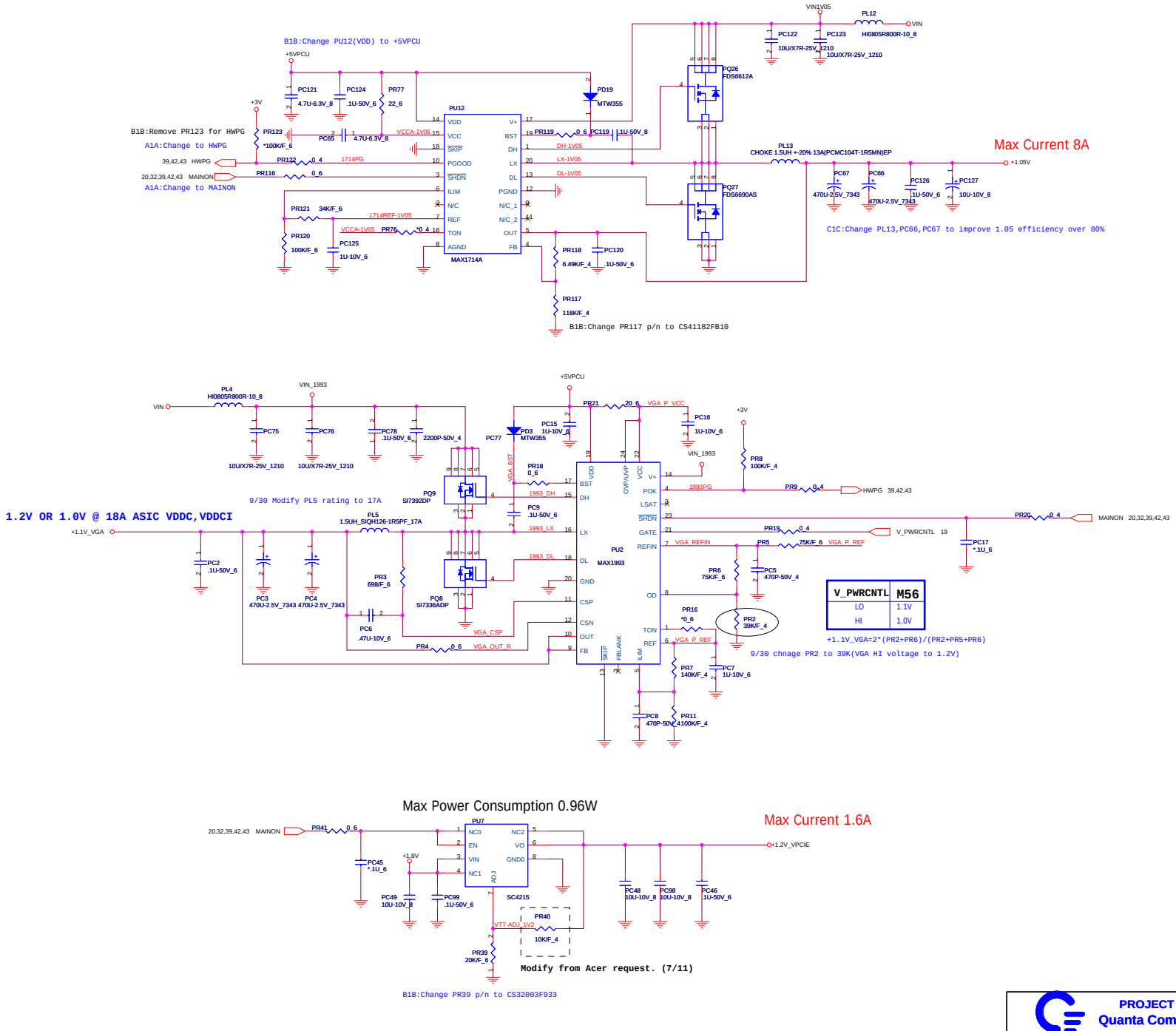


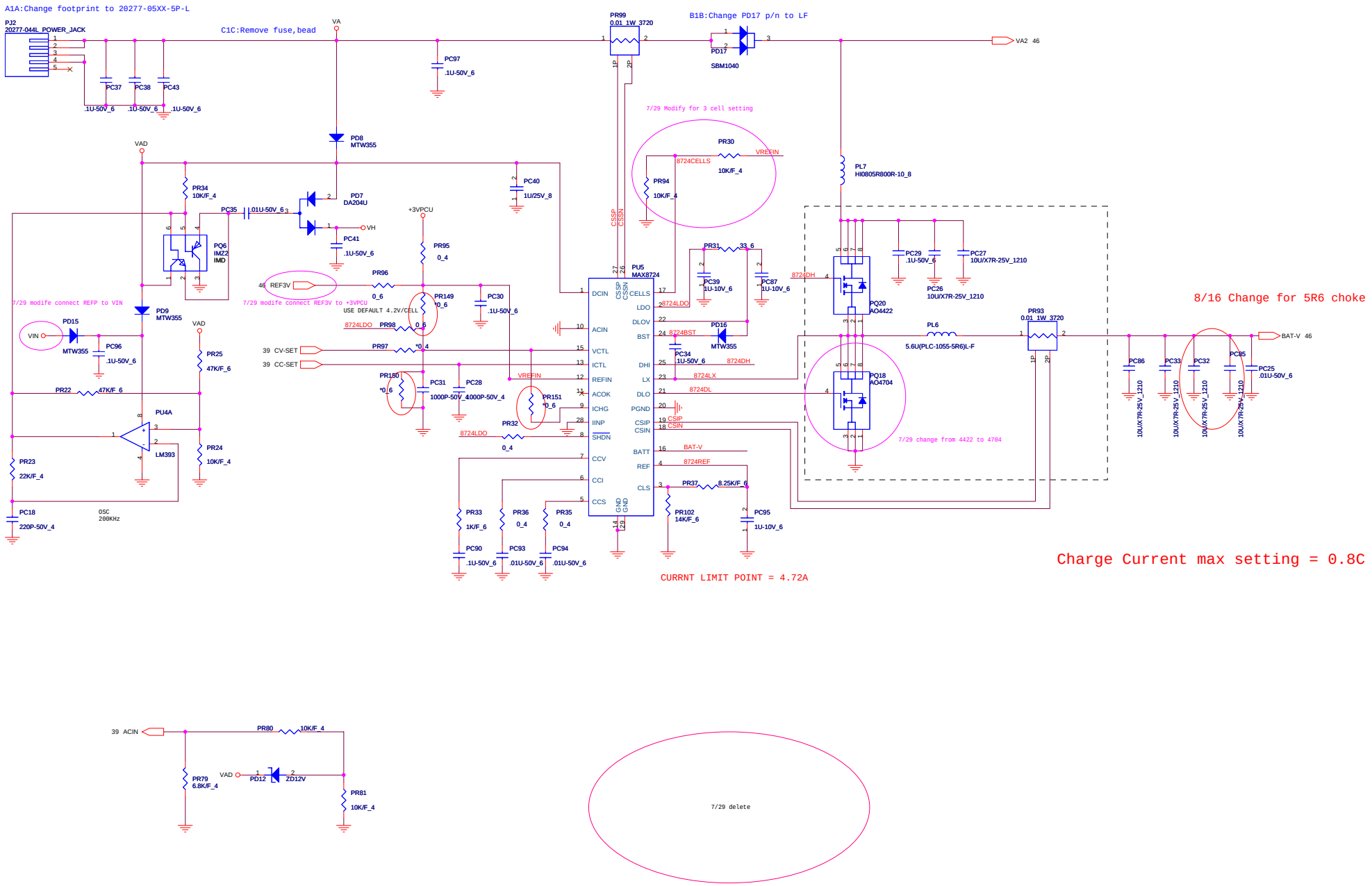
PROJECT : ZC1

Quanta Computer Inc.

Document Number	DISCHARGE/CONNECTOR	Rev 1A
Date: Monday, October 03, 2005	Sheet 42 of 46	







A1A:Change p/n to DFHD07MR391
B1B:Change CN26 footprint to 20175A-07G1-7P-R

1ST_BATT_CONN

C1C:Remove fuse

CN26 — MAIN_BATTERY

TEMP_MBAT — TEMP_MBAT 39

PC12 47P-50V_4 — PC11 47P-50V_4 — PC13 .1U-50V_6 — PC79 47P-50V_4 — PC19 10U/X7R-25V_1210

PR14 330_4 — PR13 330_4

MBDATA_MBAT — MBCLK 5,19,39

PD2 RLZ5.6B — PD4 ZD5.6V

CLOSE TO BATTERY CON

MBAT+

PQ12 AO4411 — PQ16 AO4411

PR89 10K/F_4

PQ4 PDTC143TT — MDISCHG

ADISCHG 2 — PQ10 PDTC143TT — PQ11 IMD2

ACHG

PR86 10K/F_4

VH — PC81 .1U-50V_6

PU10A LM358ADR — PR83 1M/F_4 — MCHG

PR85 470K_6

PD13 RLZ15B

45 BAT-V — PC83 .01U-50V_6

PQ19 AO4414-LF

PU10B LM358ADR — PR84 470K_6 — ACHG — PR82 100K/F_4

PD14 RLZ15B

PQ44 AO4414-LF

C1C:Add PQ44 for charger

REF3V — PR12 10K/F_4 — TEMP_MBAT — PC14 .01U-50V_6

VH — PC92 10U/X7R-25V_1220 — PR15 10K/F_4 — PQ2 PDTC143TT

VIN — PQ21 FDS6612A — PC80 .01U-50V_6 — PC84 .01U-50V_6

VA2 — VA2 45

VL — PU3 74HCT237 (VDD Y0 Y1 Y2 Y3 Y4 Y5 Y7 A B C GL G1 G2 GND)

200mil — PR92 10K/F_4 — PQ5 PDTC143TT — PC10 .1U-50V_6

ADISCHG

39 CELL-SET

39 D/C#

39 BL/C#

REFP — VIN — PR91 160K/F_6

PU4B LM393 — PR17 10K/F_4 — REF3V — PR10 100K/F_4

PQ3 2N7002 — PR26 120K/F_4

2ND_BATT_CONN

CN27 — SECOND_BATTERY

TEMP_ABAT — TEMP_ABAT 39

PR27 330_4 — PC20 47P-50V_4 — PR28 330_4 — PC21 47P-50V_4 — PC24 .1U-50V_6 — PC22 47P-50V_4

MBCLK — MBDATA_ABAT

PD6 ZD5.6V — PD5 ZD5.6V

CLOSE TO BATTERY CON

C1C:Remove fuse

ABAT+

PQ17 AO4411 — PQ15 AO4411

PC82 10U/X7R-25V_1210

MDISCHG 2 — PQ13 PDTC143TT — PQ14 IMD2

MCHG

PR90 10K/F_4

REF3V — REF3V 45 — PR29 10K/F_4 — TEMP_ABAT — PC23 .01U-50V_6

+3VPCU — PR88 10K/F_4 — PR87 10K/F_4

1ST_BATT — MBDATA_MBAT

2ND_BATT — MBDATA_ABAT

U39 NC7SB3157P6X (VCC, IN_B1, IN_B0, SEL, COM, GND)

M/A# — M/A# 39

MBDATA — MBDATA 5,19,39

SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1

PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	BATTERY SELECT	A

Date: Friday, October 07, 2005 — Sheet 46 of 46