1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

K22

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
A	0000774858	PRODUCTION RELEASED	2009-08-21

LAST_MODIFIED=Thu Aug 20 17:40:45 2009

DRAWING
TITLE=K22
ABBREV=DRAWING
LAST_MODIFIED=Thu Aug 20 17:40:45 2009

DRAWING TITLE
SCH,K22,MLB

Apple Inc.

DRAWING NUMBER 051-7845 | SIZE D
REVISION A.0.0
BRANCH
PAGE 1 OF 110
SHEET 1 OF 110

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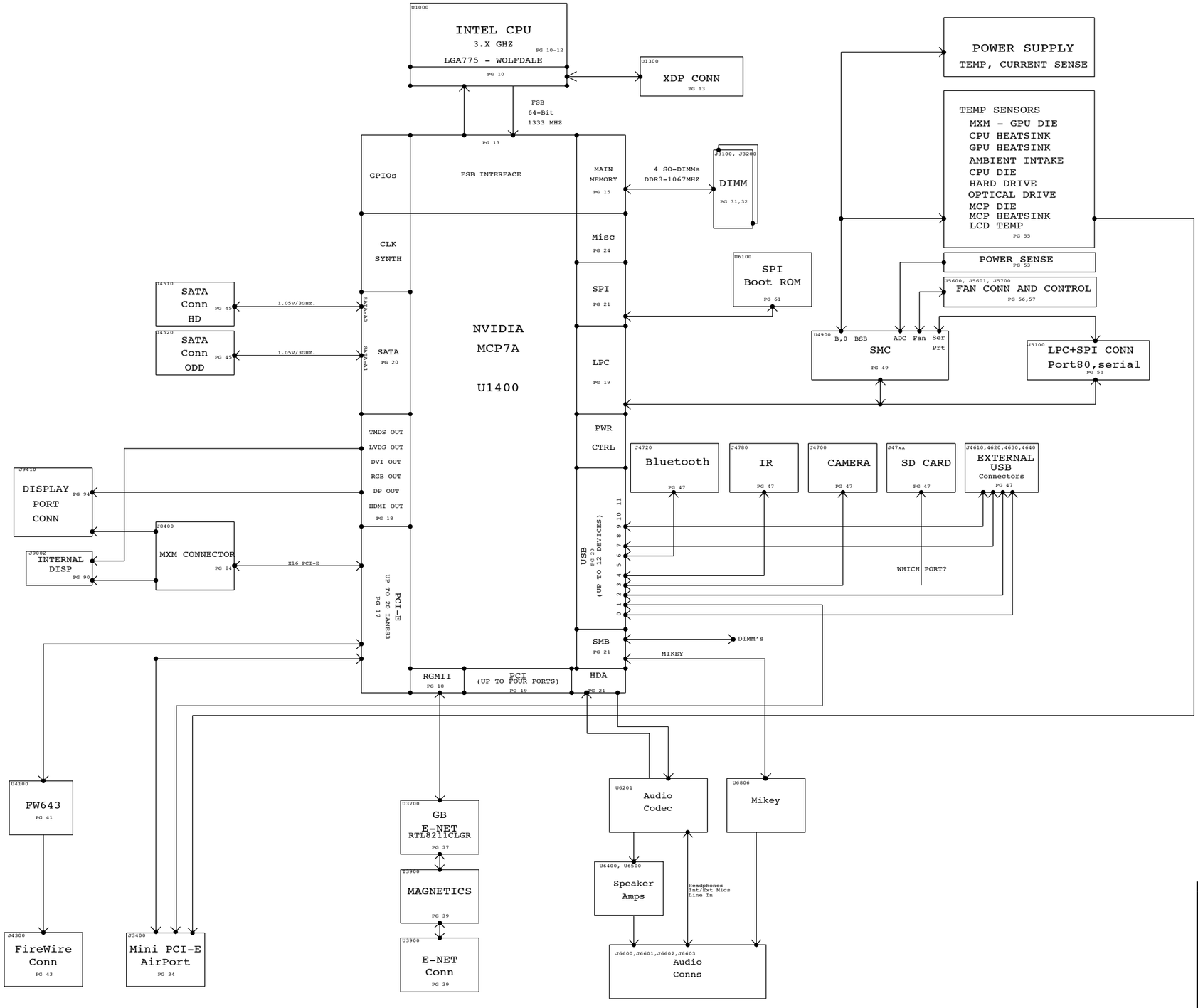

SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE

System Block Diagram

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D

REVISION A.0.0

BRANCH

PAGE 2 OF 110

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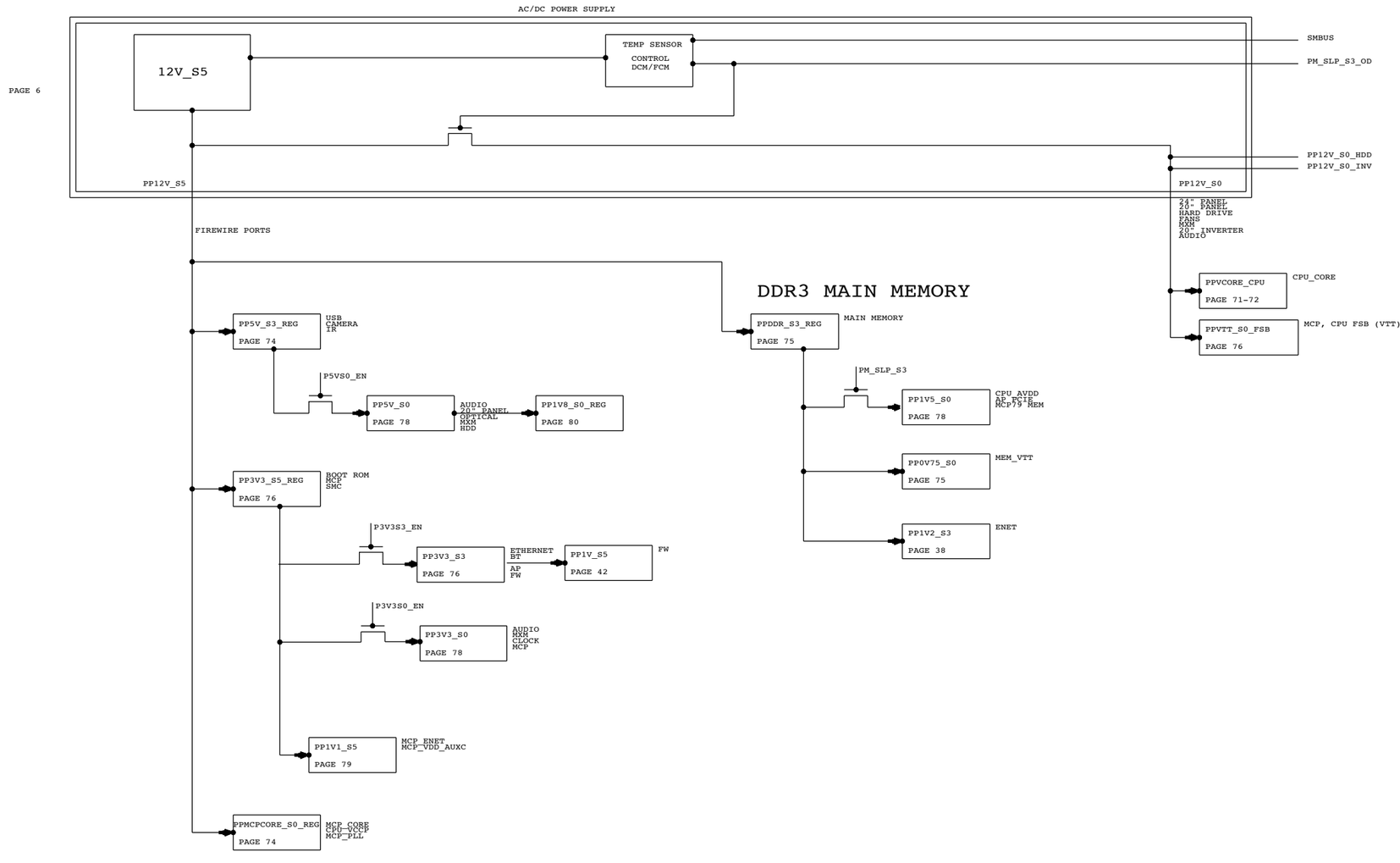

SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE

Power Block Diagram

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D

REVISION A.0.0

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PAGE 3 OF 110

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9768	PCBA,MLB,GOOD,K22	K22,2P80GHZ_CPU,BASIC,IG
639-0036	PCBA,2.8 GHZ CPU,MXM,K22	K22,2P80GHZ_CPU,BASIC,MXM,K22_MXM
639-0184	PCBA,2.93 GHZ CPU,IG,K22	K22,2P93GHZ_CPU,BASIC,IG
639-0186	PCBA,2.93 GHZ CPU,MXM,K22	K22,2P93GHZ_CPU,BASIC,MXM,K22_MXM
639-0037	PCBA,3.0 GHZ CPU,IG,K22	K22,3P0GHZ_CPU,BASIC,IG
630-9878	PCBA,MLB,CTO,K22	K22,3P0GHZ_CPU,BASIC,MXM,K22_MXM
639-0183	PCBA,3.06 GHZ CPU,IG,K22(Investigation)	K22,3P06GHZ_CPU,BASIC,IG
639-0324	PCBA,MLB,3.16GHZ,MXM,K22	K22,3P16GHZ_CPU,BASIC,MXM,K22_MXM
639-0206	PCBA,MLB,3.33GHZ,IG,K22	K22,3P33GHZ_CPU,BASIC,IG
639-0207	PCBA,MLB,3.33GHZ,MXM,K22	K22,3P33GHZ_CPU,BASIC,MXM,K22_MXM
639-0392	PCBA,2.8 GHZ-2M CPU,IG,K22	K22,2P80GHZ_2M_CPU,BASIC,IG
639-0393	PCBA,2.8 GHZ-2M CPU,MXM,K22	K22,2P80GHZ_2M_CPU,BASIC,MXM,K22_MXM
607-4426	PCBA,MLB,DEV,K22	DEVELOPMENT,DEV_GROUP

BOM GROUPS

BOM GROUP	BOM OPTIONS
BASIC	COMMON,ALTERNATE,MCP7A,XDP,BETTER,MCP_ISL9563A,MLB_PNL_PWR,PRODUCTION
MCP7A	BOOT_MODE_USER,MEMRESET_HW,MEMRESET_MCP
DEV_GROUP	XDP_CONN,LPCPLUS,VREFMRGN,MCP_PWR_SENSE,MCP_CPU_TDIODE,PECI_SMB,MOJOMUX

BOARD STACK-UP

TOP	SIGNAL
2	GROUND
3	SIGNAL
4	POWER
5	POWER
6	SIGNAL
7	GROUND
BOTTOM	SIGNAL

COMMON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0731	1	IC,GMCP,MCP7A-JA,B03,35X35MM,BGA1437,DT	U1400	CRITICAL	IG
338S0732	1	IC,MCP,MCP7A-DA,B03,35X35MM,BGA1437,DT	U1400	CRITICAL	MXM
341T0170	1	IC,EFI BOOTROM,K22/K23	U6100	CRITICAL	
338S0765	1	IC,XIO2211ZAY,1394B,167BGA	U4100	CRITICAL	
338S0694	1	IC,RTL8251CA,GIGE TRANSCEIVER, 48P TQFP	U3700	CRITICAL	
825-7122	1	MLB LABEL,48.0X4.8	X14	CRITICAL	

MCP -J SKU HAS INTEGRATED GPU
MCP -D SKU DOES NOT

CPUS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S3745	1	WLF,QXXX,QS,2.80G,65W,1066,R0,3M,LGA	CPU	CRITICAL	2P80GHZ_CPU
337S3742	1	WLF,SLB9J,PRQ,2.83G,65W,1333,E0,6M,LGA	CPU	CRITICAL	2P83GHZ_CPU
337S3726	1	WLF,SLB9J,PRQ,3.0G,65W,1333,E0,6M,LGA	CPU	CRITICAL	3P0GHZ_CPU
337S3715	1	WLF,SLB9K,PRQ,3.16G,65W,1333,E0,6M,LGA	CPU	CRITICAL	3P16GHZ_CPU
337S3727	1	WLF,SLB9L,PRQ,3.33G,65W,1333,E0,6M,LGA	CPU	CRITICAL	3P33GHZ_CPU
337S3807	1	WLF,SLB9L,PRQ,2.93G,65W,1333,E0,6M,LGA	CPU	CRITICAL	2P93GHZ_CPU
337S3766	1	WLF,SLB9L,PRQ,3.06G,65W,1333,E0,6M,LGA	CPU	CRITICAL	3P06GHZ_CPU
337S3804	1	WLF,SLGU9,PRQ,2.80G,65W,1066,R0,2M,LGA	CPU	CRITICAL	2P80GHZ_2M_CPU

K22 PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7845	1	SCH,K22,MLB	SCH1		K22
820-2494	1	PCBF,K22,MLB	MLB1		K22
(338S0563 - BLNK) 341T0168	1	IC,SMC,K22	U4900	CRITICAL	K22

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
127S0111	127S0060		C6211	AUDIO, NEED QUAL

SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE
BOM Configuration

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D
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EMC: C600,C626,C627,C628,C629,C630,C631
PLACE AT J600.

518-0352
CRITICAL
J600
76833-0100
M-RT-TH

=SMB_ACDC_SCL
=PP5V_S0_SATA
PP12V_S5
LCD_PWM
=SMB_ACDC_SDA
PP12V_S0
LCD_BKL_ON

C623 10UF 10% 10V X5R 805
C631 0.001UF 10% 50V X7R 402
C627 0.001UF 10% 50V X7R 402
C626 0.001UF 10% 50V X7R 402
C630 0.001UF 10% 50V X7R 402
C624 10UF 10% 16V X5R-CERM 1210

PM_ACDC_PS_ON
PM_SLPS3_BUF2_L
Q610 2N7002 SOT23-HF1
C600 0.001UF 10% 50V X7R 402

PP3V3_S3
DEVELOPMENT
R600 1K 5% 1/16W MF-LF 402
ITS_ALIVE
DEVELOPMENT
LED605 GREEN-3.6MCD 2.0X1.25MM-SM

PP3V3_S5_REG
R601 1K 5% 1/16W MF-LF 402
ITS_PLUGGED_IN
LED601 GREEN-3.6MCD 2.0X1.25MM-SM SILKSCREEN:1

PP3V3_S3
R602 1K 5% 1/16W MF-LF 402
CORE_VOLTAGES_ON_R
LED602 GREEN-3.6MCD 2.0X1.25MM-SM SILKSCREEN:2
CORE_VOLTAGES_ON
ALL_SYS_PWRGD_R
Q602 2N7002 SOT23-HF1

PP3V3_S0
MXM
R604 1K 5% 1/16W MF-LF 402
GPU_PRESENT_R
MXM
LED604 GREEN-3.6MCD 2.0X1.25MM-SM SILKSCREEN:3
GPU_PRESENT_DRAIN
MXM
Q604 2N7002 SOT23-HF1
MXM_GOOD

PP5V_LCD_CONN
R603 1.5K 5% 1/16W MF-LF 402
LCD_SHOULD_ON
LED603 GREEN-3.6MCD 2.0X1.25MM-SM SILKSCREEN:4

"S0" RAILS
ONLY ON IN RUN

PPVTT_S0_DDR_LDO
MAKE_BASE=TRUE
VOLTAGE=0.75V
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP0V75_S0_MEM_VTT_A
=PP0V75_S0_MEM_VTT_B
=PPVTT_S0_VTTCLAMP

PPVCORE_S0_CPU
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PPVCORE_S0_CPU

PPMCPCORE_S0_REG
MAKE_BASE=TRUE
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PPVCORE_S0_MCP
=PP1V05_S0_MCP_AVDD_UF
=PP1V05_S0_MCP_PEX_DVDD
=PP1V05_S0_MCP_PLL_UF
=PP1V05_S0_MCP_SATA_DVDD0
=PP1V05_S0_MCP_HDMI_VDD_R

PPVTT_S0_FSB_REG
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PPVTT_S0_CPU
=PPVTT_S0_FSB_CPU
=PPVTT_S0_XDP
=PP1V05_S0_MCP_FSB

PP1V5_S0
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.15MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP1V5_S0_CPU_VCCPLL
=PP1V8R1V5_S0_MCP_MEM
=PP1V5_S0_AUD_DIG
=PP1V5_FWRS0_FWXIO

PP1V8_S0_REG
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP3V3R1V8_S0_MCP_IFP_VDD_R
=PP1V8_S0_PGCMP

PP3V3_S0
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.10MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP3V3_S0_FAN
=PP3V3_S0_MCP
=PP3V3_S0_MCP_VPLL_UF
=PP3V3_S0_MCP_GPIO
=PP3V3_S0_MCP_PLL_UF
=PPSPD_S0_MEM_A
=PPSPD_S0_MEM_B
=PP3V3_S0_VRD
=PP3V3_S0_AUDIO
=PP3V3R1V5_S0_MCP_HDA
=PP3V3_S0_SMBUS
=PP3V3_S0_SMC_LS
=PP3V3_S0_SMBUS_SMC_0_S0
=PP3V3_S0_SMBUS_SMC_B_S0
=PP3V3_S0_SMBUS_SMC_MGMT
=PP3V3_S0_DPCONN
=PP3V3_S0_TSENS
=PP3V3_S0_MXM
=PP3V3_S0_XDP
=PP3V3_S0_ODD
=PP3V3_S0_SATALED
=PP3V3_S0_SMC
=PP3V3_S0_PWRCTL
=PP3V3_S0_MCPTHMSNS
=PP3V3_S0_VIDEO
=PP3V3_FW_FWPHY
=PP3V3_FWRS0_FWXIO

PP5V_S0
MAKE_BASE=TRUE
VOLTAGE=5.0V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP5V_S0_LPCPLUS
=PP5V_S0_AUDIO
=PP5V_S0_SATA
=PP5V_S0_MXM
=PP5V_S0_VRD
=PP5V_S0_DP_AUX_MUX
=PP5V_S0_ISENSE
=PP5V_S0_PWRCTL
=PP5V_S0_LCD

PP12V_S0
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=AUDIO
MAX_NECK_LENGTH=3 MM
=PP12V_S0_FAN
=PP12V_S0_AUDIO_SPKRAMP
=PP12V_S0_VRD
=PPV_S0_MXM_PWR
=PPVIN_S0_PPVTT_FSB
=PPVIN_S0_MCPCORE

"S3" RAILS
ON IN RUN AND SLEEP

PPDDR_S3_REG
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PPDDR_MAX
MAX_NECK_LENGTH=3 MM
=PP1V5_S3_MEM_A
=PP1V5_S3_MEM_B
=PP1V5_S3_MEMRESET
=PPDDR_S3_S0FET
=PPDDR_S3_PGCMP

PPVTT_S3_DDR_BUF
MAKE_BASE=TRUE
VOLTAGE=0.75V
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 mm
=PPVTT_S3_DDR_BUF

PP3V3_S3
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP3V3_S3_MINI
=PP3V3_S3_BT
=PP3V3_S3_VREFMRGN
=PP3V3_S3_SDCARD
=PP3V3_S3_MCP_GPIO
=PP3V3_S3_SMC
=PP3V3_S3_SMBUS_SMC_A_S3
=PP3V3_S3_MCPREG

PP5V_S3_REG
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP5V_S3_DDRREG
=PP5V_S3_USB
=PP5V_S3_VTTCLAMP
=PP5V_S3_PWRCTL
=PP5V_S3_S0FET
=PP5V_S3_MCPREG
=PP5V_S3_CAMERA
=PP5V_S3_IR
=PP5V_S3_1V8

"S5" RAILS
ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

PP1V1_S5_REG
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP1V05_S5_MCP_VDD_AUXC
=PP1V1_S5_ENET_FET

PP3V3_S5_REG
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP3V3_S5_MCP
=PP3V3_S5_MCP_GPIO
=PP3V3_S5_SMC
=PP3V3_S5_ROM
=PP3V3_S5_RTC_D
=PP3V3_S5_LPCPLUS
=PP3V3_S5_SMBUS_SMC_BSA
=PP3V3_S5_SMCUSBMUX
=PP3V3_S5_MEMRESET
=PP3V3_S5_P1V1S5
=PP3V3_S5_PWRCTL
=PP3V3_S5_S3FET
=PP3V3_S5_S0FET
=PP3V3_S5_ENET_FET

PP5V_S5_LDO
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP5V_S5_AVREF

PP12V_S5
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP12V_S5_FW
=PPVIN_S5_DDRREG
=PPVIN_S5_P3V3S5
=PPVIN_S5_P5VS3
=PP12V_S5_REG
=PP12V_S5_PWRCTL

GND RAILS

GND
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V
NET_SPACING_TYPE=AUDIO
MAKE_BASE=TRUE
MAX_NECK_LENGTH=4.1 MM

SYNC MASTER=MASTER
SYNC DATE=N/A
PAGE TITLE
Power Conn / Alias

Apple Inc.

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870-1125
FOR MCP HEATSINK
CRITICAL

SC0700
EMI-SPRING
CLIP-SM1

870-1125
FOR MCP HEATSINK
CRITICAL

SC0701
EMI-SPRING
CLIP-SM1

DIMM CONNECTOR NUTS

CRITICAL
SDF0750
NUT-4.25OD1.4H-1.40-3.25-TH

CRITICAL
SDF0751
NUT-4.25OD1.4H-1.40-3.25-TH

CRITICAL
SDF0752
NUT-4.25OD1.4H-1.40-3.25-TH

CRITICAL
SDF0753
NUT-4.25OD1.4H-1.40-3.25-TH

BACKER PLATE NUTS

CRITICAL
SDF0700
NUT-6.5OD1.4H-1.56-3.8-TH

CRITICAL
SDF0701
NUT-6.5OD1.4H-1.56-3.8-TH

CRITICAL
SDF0702
NUT-6.5OD1.4H-1.56-3.8-TH

CRITICAL
SDF0703
NUT-6.5OD1.4H-1.56-3.8-TH

4 MM PLATED HOLES FOR CPU HEATSINK
998-0850

OMIT
ZH0700
4P75R4

OMIT
ZH0701
4P75R4

OMIT
ZH0702
4P75R4

OMIT
ZH0703
4P75R4

REAR COVER STANDOFFS

CRITICAL
SDF0713
STDOFF-6.8OD15.0H-1.56-TH

CRITICAL
SDF0714
STDOFF-6.8OD15.0H-1.56-TH

CRITICAL
SDF0715
STDOFF-6.8OD15.0H-1.56-TH

CRITICAL
SDF0716
STDOFF-6.8OD15.0H-1.56-TH

CRITICAL
SDF0717
STDOFF-6.8OD15.0H-1.56-TH

SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE
HOLES & STANDOFFS

Apple Inc.

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NC ON UNUSED ALIASES

18	MCP_TV_DAC_RSET	=	NC_MCP_TV_DAC_RSET	MAKE_BASE=TRUE NO_TEST=TRUE
18	MCP_TV_DAC_VREF	=	NC_MCP_TV_DAC_VREF	MAKE_BASE=TRUE NO_TEST=TRUE
18	MCP_CLK27M_XTALIN	=	NC_MCP_CLK27M_XTALIN	MAKE_BASE=TRUE NO_TEST=TRUE
18	MCP_CLK27M_XTALOUT	=	NC_MCP_CLK27M_XTALOUT	MAKE_BASE=TRUE NO_TEST=TRUE
18	CRT_IG_R_C_PR	=	NC_CRT_IG_R_C_PR	MAKE_BASE=TRUE NO_TEST=TRUE
18	CRT_IG_G_Y_Y	=	NC_CRT_IG_G_Y_Y	MAKE_BASE=TRUE NO_TEST=TRUE
18	CRT_IG_B_COMP_PB	=	NC_CRT_IG_B_COMP_PB	MAKE_BASE=TRUE NO_TEST=TRUE
18	CRT_IG_HSYNC	=	NC_CRT_IG_HSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
18	CRT_IG_VSYNC	=	NC_CRT_IG_VSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_MCP_RGB_HSYNC	=	NC_MCP_RGB_HSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_MCP_RGB_VSYNC	=	NC_MCP_RGB_VSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_AD<31..15>	=	NC_PCI_AD<31..15>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_IRDY_L	=	NC_PCI_IRDY_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_C_BE_L<1..0>	=	NC_PCI_C_BE_L<1..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_SERR_L	=	NC_PCI_SERR_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_DEVSEL_L	=	NC_PCI_DEVSEL_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_PERR_L	=	NC_PCI_PERR_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_LPC_DRQ0_L	=	NC_LPC_DRQ0_L	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_MCP_BUF_SIO_CLK	=	NC_MCP_BUF_SIO_CLK	MAKE_BASE=TRUE NO_TEST=TRUE

18	TP_ENET_INTR_L	=	NC_ENET_INTR_L	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_ENET_PWRDWN_L	=	NC_ENET_PWDWN_L	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_MCP_KBDRSTIN_L	=	NC_MCP_KBDRSTIN_L	MAKE_BASE=TRUE NO_TEST=TRUE
	TP_MCP_GPIO_18	=	NC_MCP_GPIO_18	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_MLB_RAM_SIZE	=	NC_MLB_RAM_SIZE	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_C_BE_L<3>	=	NC_PCI_C_BE_L<3>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_CLK0	=	NC_PCI_CLK0	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_CLK1	=	NC_PCI_CLK1	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_FRAME_L	=	NC_PCI_FRAME_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_GNT0_L	=	NC_MCP_PCI_GNT0_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_GNT1_L	=	NC_PCI_GNT1_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_INTW_L	=	NC_PCI_INTW_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_INTX_L	=	NC_PCI_INTX_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_INTY_L	=	NC_PCI_INTY_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_INTZ_L	=	NC_PCI_INTZ_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_PAR	=	NC_PCI_PAR	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_RESET1_L	=	NC_PCI_RESET1_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_STOP_L	=	NC_PCI_STOP_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_TRDY_L	=	NC_PCI_TRDY_L	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE4N	=	NC_PCIE_CLK100M_PE4N	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE4P	=	NC_PCIE_CLK100M_PE4P	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE5N	=	NC_PCIE_CLK100M_PE5N	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE5P	=	NC_PCIE_CLK100M_PE5P	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE6P	=	NC_PCIE_CLK100M_PE6P	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE6N	=	NC_PCIE_CLK100M_PE6N	MAKE_BASE=TRUE NO_TEST=TRUE
17	PCIE_EXCARD_PRSNT_L	=	NC_PCIE_EXCARD_PRSNT_L	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PE4_CLKREQ_L	=	NC_PE4_CLKREQ_L	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PE4_PRSNT_L	=	NC_PE4_PRSNT_L	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_SB_A20GATE	=	NC_SB_A20GATE	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_10N	=	NC_USB_10N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_10P	=	NC_USB_10P	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_MINI_N	=	NC_USB_MINI_N	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_MINI_P	=	NC_USB_MINI_P	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_EXCARD_N	=	NC_USB_EXCARD_N	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_EXCARD_P	=	NC_USB_EXCARD_P	MAKE_BASE=TRUE NO_TEST=TRUE
21	ODD_PWR_EN_L	=	NC_ODD_PWR_EN_L	MAKE_BASE=TRUE NO_TEST=TRUE
17	PCIE_CLK100M_EXCARD_P	=	NC_PCIE_CLK100M_EXCARD_P	MAKE_BASE=TRUE NO_TEST=TRUE
17	PCIE_CLK100M_EXCARD_N	=	NC_PCIE_CLK100M_EXCARD_N	MAKE_BASE=TRUE NO_TEST=TRUE
17	EXCARD_CLKREQ_L	=	NC_EXCARD_CLKREQ_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_AD<12..10>	=	NC_PCI_AD<12..10>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_AD<8>	=	NC_PCI_AD<8>	MAKE_BASE=TRUE NO_TEST=TRUE

17	TP_PCIE_PE4_R2D_CP	=	NC_PCIE_PE4_R2D_CP	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PCIE_PE4_R2D_CN	=	NC_PCIE_PE4_R2D_CN	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PCIE_PE4_D2RP	=	NC_PCIE_PE4_D2RP	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PCIE_PE4_D2RN	=	NC_PCIE_PE4_D2RN	MAKE_BASE=TRUE NO_TEST=TRUE
17	PCIE_EXCARD_D2R_P	=	NC_PCIE_EXCARD_D2R_P	MAKE_BASE=TRUE NO_TEST=TRUE
17	PCIE_EXCARD_D2R_N	=	NC_PCIE_EXCARD_D2R_N	MAKE_BASE=TRUE NO_TEST=TRUE
17	PCIE_EXCARD_R2D_C_P	=	NC_PCIE_EXCARD_R2D_C_P	MAKE_BASE=TRUE NO_TEST=TRUE
17	PCIE_EXCARD_R2D_C_N	=	NC_PCIE_EXCARD_R2D_C_N	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_TPAD_N	=	NC_USB_TPAD_N	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_TPAD_P	=	NC_USB_TPAD_P	MAKE_BASE=TRUE NO_TEST=TRUE

MCP HAS INTERNAL 15K PULL-DOWNS

UNUSED MEMORY SIGNALS

15	TP_MEM_A_CLK2P	=	NC_MEM_A_CLK2P	MAKE_BASE=TRUE NO_TEST=TRUE
15	TP_MEM_A_CLK2N	=	NC_MEM_A_CLK2N	MAKE_BASE=TRUE NO_TEST=TRUE
16	TP_MEM_A_CLK5P	=	NC_MEM_A_CLK5P	MAKE_BASE=TRUE NO_TEST=TRUE
16	TP_MEM_A_CLK5N	=	NC_MEM_A_CLK5N	MAKE_BASE=TRUE NO_TEST=TRUE
15	TP_MEM_B_CLK2P	=	NC_MEM_B_CLK2P	MAKE_BASE=TRUE NO_TEST=TRUE
15	TP_MEM_B_CLK2N	=	NC_MEM_B_CLK2N	MAKE_BASE=TRUE NO_TEST=TRUE
16	TP_MEM_B_CLK5P	=	NC_MEM_B_CLK5P	MAKE_BASE=TRUE NO_TEST=TRUE
16	TP_MEM_B_CLK5N	=	NC_MEM_B_CLK5N	MAKE_BASE=TRUE NO_TEST=TRUE

UNUSED GMUX JTAG FROM MCP

17	GMUX_JTAG_TCK_L	=	NC_GMUX_JTAG_TCK_L	MAKE_BASE=TRUE NO_TEST=TRUE
17	GMUX_JTAG_TDO	=	NC_GMUX_JTAG_TDO	MAKE_BASE=TRUE NO_TEST=TRUE
19	GMUX_JTAG_TDI	=	NC_GMUX_JTAG_TDI	MAKE_BASE=TRUE NO_TEST=TRUE
19	GMUX_JTAG_TMS	=	NC_GMUX_JTAG_TMS	MAKE_BASE=TRUE NO_TEST=TRUE

SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE

UNUSED SIGNAL ALIAS

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D

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PAGE 8 OF 110

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SIGNAL ALIAS

21 TP_MLB_RAM_VENDOR = MXM_GOOD (MAKE_BASE=TRUE) 6

102 21 PM_SLP_S3_L — R910 15 5% 1/16W MF-LF 402 — PM_SLPS3_BUF2_L (MAKE_BASE=TRUE) 6 49 50 70

(P50 HAS A 100K TO GROUND)

R911 15 5% 1/16W MF-LF 402 — PM_SLPS3_BUF1_L (MAKE_BASE=TRUE) 73 94

1 R912 100K 5% 1/16W MF-LF 402 2

46 20 USB_EXTC_OC_L (MAKE_BASE=TRUE)

46 USB_EXTD_OC_L

K22/K23 Use one GPIO for both ports 2&3 OC

USB PORT 2 AND 3 (C AND D) SHARE OVER-CURRENT WITH PORT 2
PREVIOUSLY, PORT 3 HAD ITS OWN BUT EFI MAPS THAT TO EXPRESSCARD
SEE RDAR://6250424

PEG Slot Support

17 IN PEG_CLK100M_P = GPU_CLK100M_PCIE_P OUT 87 102 (MAKE_BASE=TRUE)
17 IN PEG_CLK100M_N = GPU_CLK100M_PCIE_N OUT 87 102 (MAKE_BASE=TRUE)
17 IN =PEG_R2D_C_P<0..15> = PEG_R2D_C_P<0..15> OUT 86 102 (MAKE_BASE=TRUE)
17 IN =PEG_R2D_C_N<0..15> = PEG_R2D_C_N<0..15> OUT 86 102 (MAKE_BASE=TRUE)
17 OUT =PEG_D2R_P<0..15> = PEG_D2R_P<0..15> IN 86 102 (MAKE_BASE=TRUE)
17 OUT =PEG_D2R_N<0..15> = PEG_D2R_N<0..15> IN 86 102 (MAKE_BASE=TRUE)
17 IN PEG_PRSNT_L = MXM_DETECT_L OUT 85 (MAKE_BASE=TRUE)

DisplayPort / TMDS Support

18 IN =MCP_HDMI_TXC_P = DP_IG_ML_P<3> OUT 91 107 (MAKE_BASE=TRUE)
18 IN =MCP_HDMI_TXC_N = DP_IG_ML_N<3> OUT 91 107 (MAKE_BASE=TRUE)
18 IN =MCP_HDMI_TXD_P<0..2> = DP_IG_ML_P<2..0> OUT 91 107 (MAKE_BASE=TRUE)
18 IN =MCP_HDMI_TXD_N<0..2> = DP_IG_ML_N<2..0> OUT 91 107 (MAKE_BASE=TRUE)
18 IN =MCP_HDMI_DDC_CLK = DP_IG_DDC_CLK OUT 93 (MAKE_BASE=TRUE)
18 BI =MCP_HDMI_DDC_DATA = DP_IG_DDC_DATA BI 93 (MAKE_BASE=TRUE)
18 OUT =MCP_HDMI_HPD = DP_IG_HPD IN 91 (MAKE_BASE=TRUE)

18 =DVI_HPD_GMUX_INT = HPLUG_DET2 (MAKE_BASE=TRUE) — R900 20K 5% 1/16W MF-LF 402

MCP79 PCIe PRSNT# Straps

= PCIE_FW_PRSNT_L OUT 17
= PCIE_MINI_PRSNT_L OUT 17

Audio Mux aliasing

103 66 IN AUD_SPDIF_IN = AUD_SPDIF_IN_CODEC OUT 62 (MAKE_BASE=TRUE)

this alias connects spdif directly from the I/O port to the codec
K23 uses a mux between the DP audio source and the audio in port

62 IN AUD_MUX_CNTRL = TP_AUD_MUX_CNTRL (MAKE_BASE=TRUE)

K23 Uses this to control the DP audio mux. K22 does not need this signal

Platform Reset Connections

LPC Reset (Unbuffered)

103 19 IN LPC_RESET_L — R981 33 5% 1/16W MF-LF 402 — DEBUG_RESET_L OUT 51
PLACEMENT_NOTE=Place close to U1400
R983 33 5% 1/16W MF-LF 402 — SMC_LRESET_L OUT 49
PLACEMENT_NOTE=Place close to U1400

PCIE Reset (Unbuffered)

17 IN PCIE_RESET_L — R992 0 5% 1/16W MF-LF 402 — FW_RESET_L OUT 41
R991 0 5% 1/16W MF-LF 402 — MINI_RESET_L OUT 34
R990 0 5% 1/16W MF-LF 402 — PEG_RESET_L OUT 87 90
R971 0 5% 1/16W MF-LF 402 — PCA9557D_RESET_L OUT 29
R993 0 5% 1/16W MF-LF 402 — CARDREADER_PLT_RST_L OUT 47

19 IN MEM_VTT_EN_R — R972 33 5% 1/16W MF-LF 402 — DDRVTT_EN OUT 75 78
NO STUFF
1 C973 0.47UF 10% 6.3V CERM-X5R 402 2

LPC_CLK33M_SMC_R

103 19 IN LPC_CLK33M_SMC_R — R925 33 5% 1/16W MF-LF 402 — LPC_CLK33M_SMC OUT 49 103
PLACEMENT_NOTE=Place close to U1400
R926 33 5% 1/16W MF-LF 402 — LPC_CLK33M_LPCPLUS OUT 51 103
PLACEMENT_NOTE=Place close to U1400

PM_CLK32K_SUSCLK_R

103 21 IN PM_CLK32K_SUSCLK_R — R929 22 5% 1/16W MF-LF 402 — PM_CLK32K_SUSCLK OUT 49 103
PLACEMENT_NOTE=Place close to U1400

MCP_CPUVDD_EN WILL ASSERT AFTER MCP_PS_PWRGD IS UP

21 IN MCP_CPUVDD_EN — R930 22 5% 1/16W MF-LF 402 — MCP_CPU_VLD OUT 21
PLACEMENT_NOTE=Place close to U1400

18 =MCP_MII_RXER
18 =MCP_MII_COL
18 =MCP_MII_CRS
= MCP_MII_NU (MAKE_BASE=TRUE) — 1 R955 47K 5% 1/16W MF-LF 402 2

SYNC MASTER=MASTER SYNC DATE=N/A
PAGE TITLE: SIGNAL ALIASES

Apple Inc.

DRAWING NUMBER: 051-7845 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 9 OF 110
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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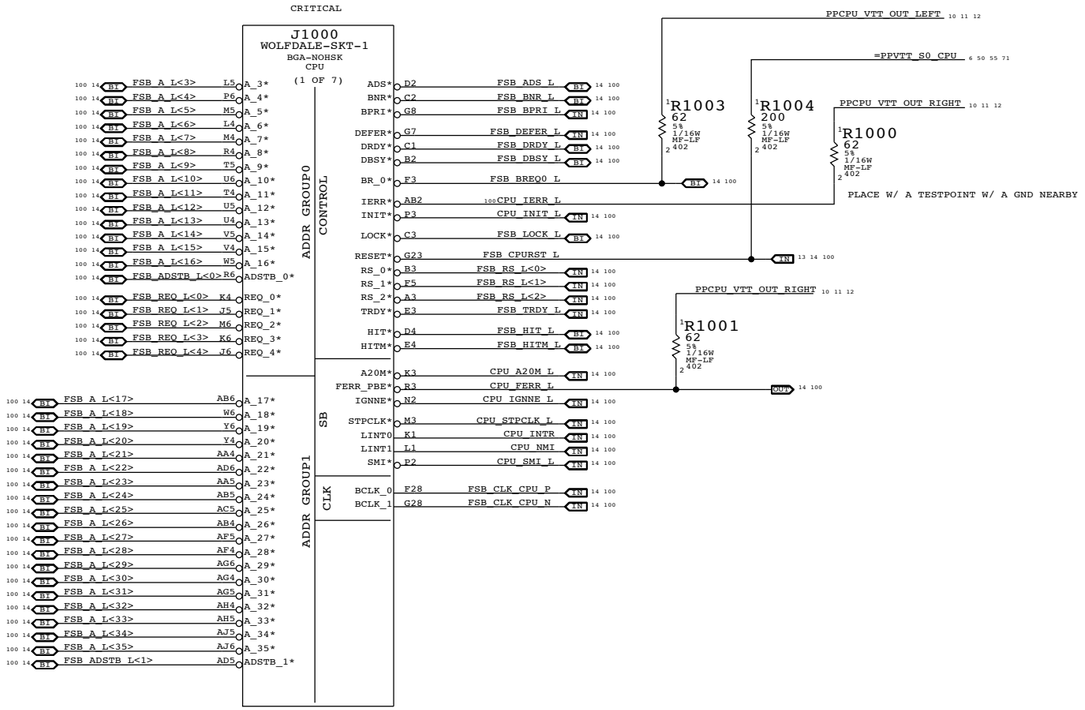
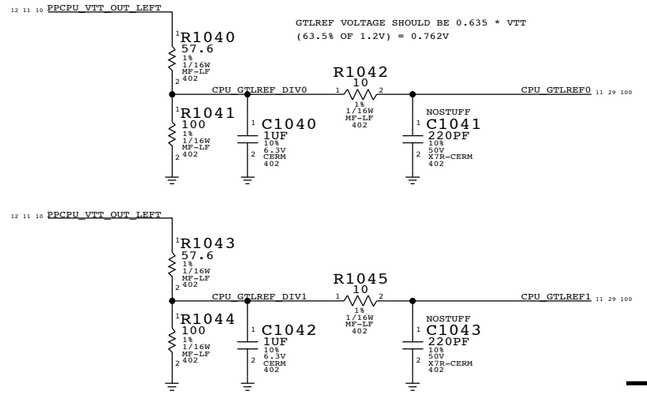


CPU GTLREF



SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE

CPU FSB

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D

REVISION A.0.0

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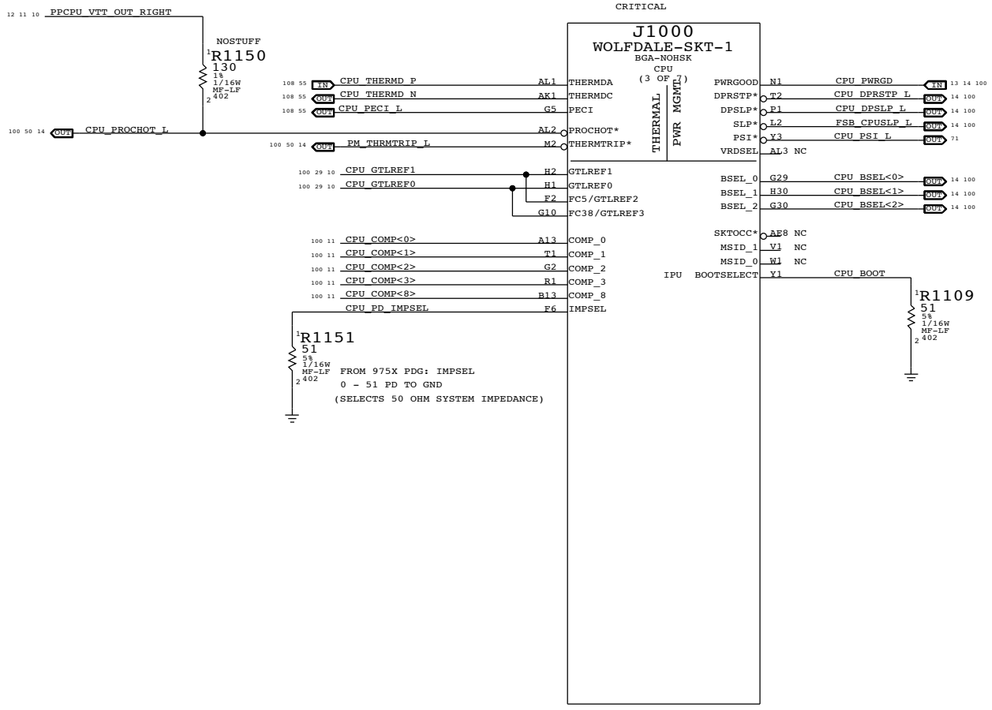
CRITICAL
J1000
WOLFDALE-SKT-1
BGA-NOHSK
CPU
(3 OF 7)
THERMAL
PWR MGMT
12 11 10 PPCPU_VTT_OUT_RIGHT
NOSTUFF
R1150
130
1% 1/16W MF-LF 402
100 50 14 OUT CPU_PROCHOT_L
108 55 IN CPU_THERMD_P
108 55 OUT CPU_THERMD_N
108 55 OUT CPU_PECI_L
100 50 14 OUT PM_THRMTRIP_L
100 29 10 CPU_GTLREF1
100 29 10 CPU_GTLREF0
100 11 CPU_COMP<0>
100 11 CPU_COMP<1>
100 11 CPU_COMP<2>
100 11 CPU_COMP<3>
100 11 CPU_COMP<8>
CPU_PD_IMPSEL
R1151
51
5% 1/16W MF-LF 402
FROM 975X PDG: IMPSEL
0 - 51 PD TO GND
(SELECTS 50 OHM SYSTEM IMPEDANCE)
AL1 THERMDA
AK1 THERMDC
G5 PECI
AL2 PROCHOT*
M2 THERMTRIP*
H2 GTLREF1
H1 GTLREF0
F2 FC5/GTLREF2
G10 FC38/GTLREF3
A13 COMP_0
T1 COMP_1
G2 COMP_2
R1 COMP_3
B13 COMP_8
F6 IMPSEL
PWRGOOD N1 CPU_PWRGD
DPRSTP* T2 CPU_DPRSTP_L
DPSLP* P1 CPU_DPSLP_L
SLP* L2 FSB_CPUSLP_L
PSI* Y3 CPU_PSI_L
VRDSEL AL3 NC
BSEL_0 G29 CPU_BSEL<0>
BSEL_1 H30 CPU_BSEL<1>
BSEL_2 G30 CPU_BSEL<2>
SKTOCC* AE8 NC
MSID_1 Y1 NC
MSID_0 W1 NC
IPU BOOTSELECT Y1 CPU_BOOT
R1109
51
5% 1/16W MF-LF 402
12 11 10 PPCPU_VTT_OUT_LEFT
R1129 R1130 R1133 R1132 R1135
51
5% 1/16W MF-LF 402
12 6 =PPVTT_S0_FSB_CPU
12 11 10 PPCPU_VTT_OUT_RIGHT
R1100
R1101
R1102
51
5% 1/16W MF-LF 402
(TMS)
(TDI)
(TCK)
PPCPU_VTT_OUT_RIGHT 10 11 12
PLACE TMS/TMI/TCK TERMINATION WITHIN 38MM (1.5IN) OF THE CPU
CRITICAL
J1000
WOLFDALE-SKT-1
BGA-NOHSK
CPU
(4 OF 7)
JTAG
TEST
RESERVED
XDP/ITP
100 13 IN CPU_XDP_TCK
100 13 IN CPU_XDP_TDI
100 13 OUT CPU_XDP_TDO
100 13 IN CPU_XDP_TMS
100 13 IN CPU_XDP_TRST_L
CPU_TESTHI_M
CPU_TESTHI_0
CPU_TESTHI_1
CPU_TESTHI_2 7
CPU_TESTHI_10
100 13 11 B1 CPU_XDP_BPM_L<0>
100 13 11 B1 CPU_XDP_BPM_L<1>
100 13 11 B1 CPU_XDP_BPM_L<2>
100 13 11 B1 CPU_XDP_BPM_L<3>
100 13 11 B1 CPU_XDP_BPM_L<4>
100 13 11 B1 CPU_XDP_BPM_L<5>
100 13 11 B1 CPU_XDP_BPMB<0>
100 13 11 B1 CPU_XDP_BPMB<1>
100 13 11 B1 CPU_XDP_BPMB<2>
100 13 11 B1 CPU_XDP_BPMB<3>
28 13 IN XDP_DBRESET_L
NC
AE1 TCK
AD1 TDI
AF1 TDO
AC1 TMS
AG1 TRST*
U1 FC28/TDO_M
W2 TESTHI_12/TDI_M
F26 TESTHI_0
W3 TESTHI_1
F25 TESTHI_2
G25 TESTHI_3
G27 TESTHI_4
G26 TESTHI_5
G24 TESTHI_6
F24 TESTHI_7
H5 TESTHI_10
AJ2 BPM_0*
AJ1 BPM_1*
AD2 BPM_2*
AG2 BPM_3*
AF2 BPM_4*
AG3 BPM_5*
G1 FC27/BPMB0*
C9 FC41/BPMB1*
G4 TESTHI_9/BPMB2*
G3 TESTHI_8/BPMB3*
AC2 DBR*
AK3 ITPCLK_0
AJ3 ITPCLK_1
FC3 J2
FC8 AK6
FC10 E24
FC15 H29
FC18 AF3
FC23 A24
FC26 E29
FC29 U2
FC30 U3
FC31 J16
FC32 H15
FC33 H16
FC34 J17
FC35 H4
FC36 AD3
FC37 AB3
FC39 AA2
FC40 AM6 PM_PGOOD_PVCORE_CPU IN 70 71
RSVD_G6 G6
RSVD_N4 N4
RSVD_P5 P5
RSVD_AC4 AC4
RSVD_AE4 AE4
RSVD_F29 F29
RSVD_AH2 AH2
RSVD_V2 V2
RSVD_N5 N5
RSVD_E7 E7
RSVD_AE6 AE6
RSVD_D16 D16
RSVD_A20 A20
RSVD_E23 E23
RSVD_F23 F23
RSVD_D14 D14
RSVD_E6 E6
RSVD_E5 E5
RSVD_J3 J3
RSVD_D1 D1
CPU BPM TERM
12 11 10 PPCPU_VTT_OUT_RIGHT
R1190 R1191 R1192 R1193 R1194 R1195
51
5% 1/16W MF-LF 402
100 13 11 CPU_XDP_BPM_L<0>
100 13 11 CPU_XDP_BPM_L<1>
100 13 11 CPU_XDP_BPM_L<2>
100 13 11 CPU_XDP_BPM_L<3>
100 13 11 CPU_XDP_BPM_L<4>
100 13 11 CPU_XDP_BPM_L<5>
100 11 CPU_COMP<8>
100 11 CPU_COMP<3>
100 11 CPU_COMP<2>
100 11 CPU_COMP<1>
100 11 CPU_COMP<0>
R1120 R1121 R1122 R1123
49.9
1% 1/16W MF-LF 402
R1128
24.9
1% 1/16W MF-LF 402
CPU BPMB TERM
(ALSO WRITTEN AS BPM2)
KENTSFIELD CPU SUPPORT
PPCPU_VTT_OUT_LEFT 10 11 12
R1180 R1181 R1182 R1183
51
5% 1/16W MF-LF 402
100 13 11 B1 CPU_XDP_BPMB<3>
100 13 11 B1 CPU_XDP_BPMB<2>
100 13 11 B1 CPU_XDP_BPMB<1>
100 13 11 B1 CPU_XDP_BPMB<0>
SYNC MASTER=MASTER
SYNC DATE=N/A
PAGE TITLE
CPU TEST & MISC.
Apple Inc.
DRAWING NUMBER 051-7845
SIZE D
REVISION A.0.0
BRANCH
PAGE 11 OF 110
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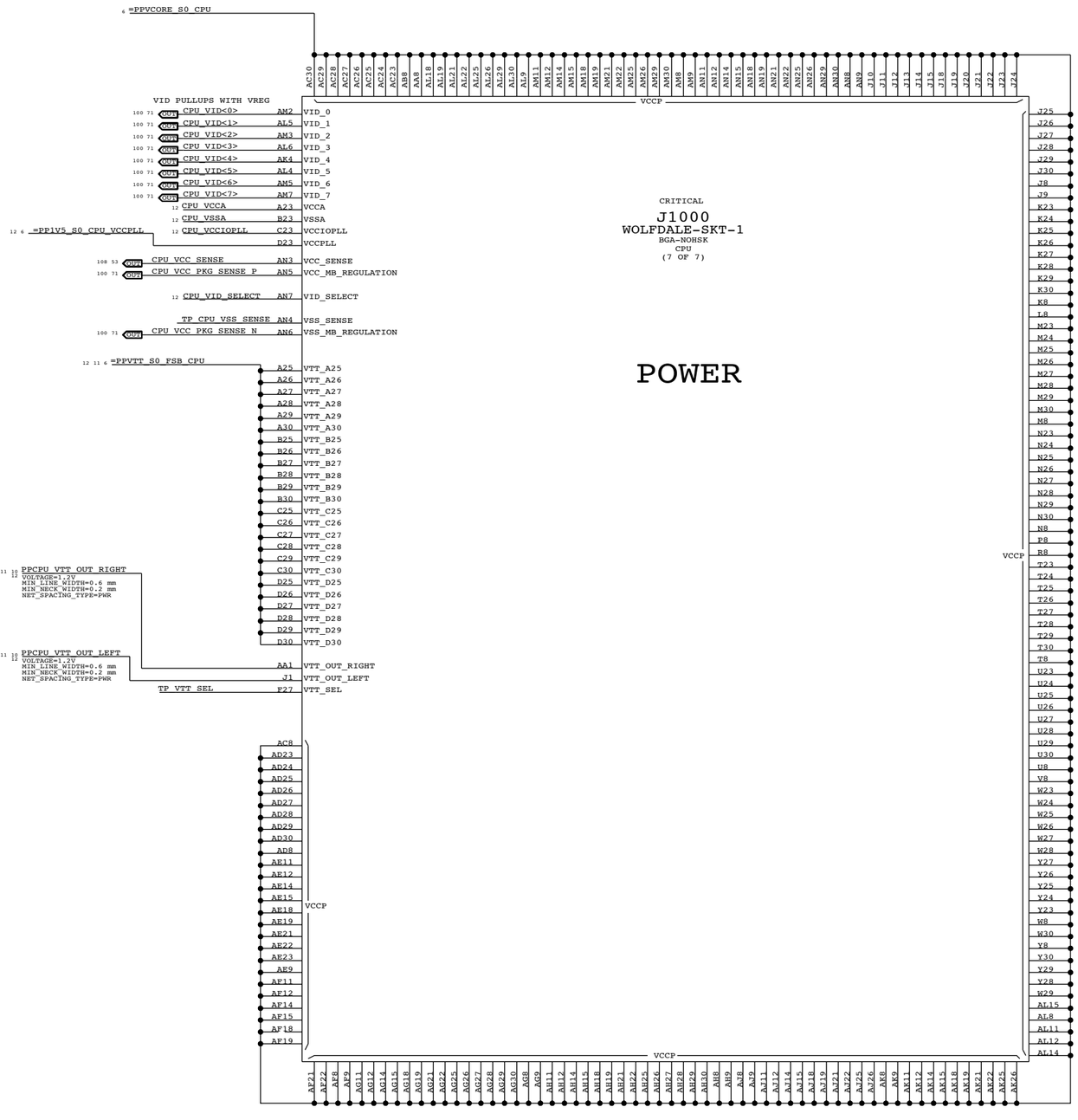
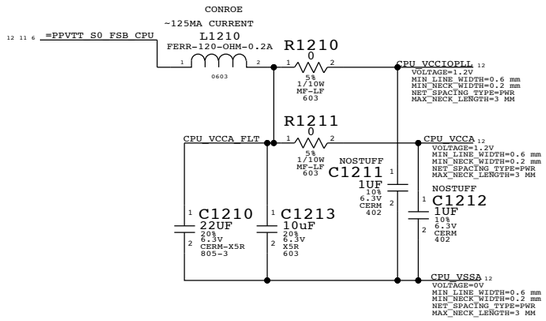
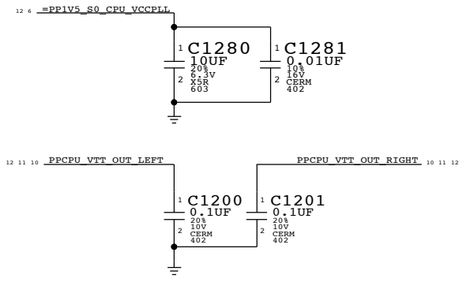


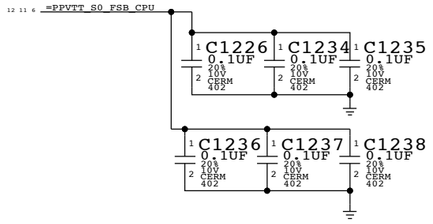
THIS IS FOR OLDER CPU SUPPORT
WILL PLACE FILTER BUT NOT CONNECT FOR WOLFDALE



VCC PLL DECOUPLING

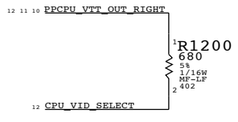


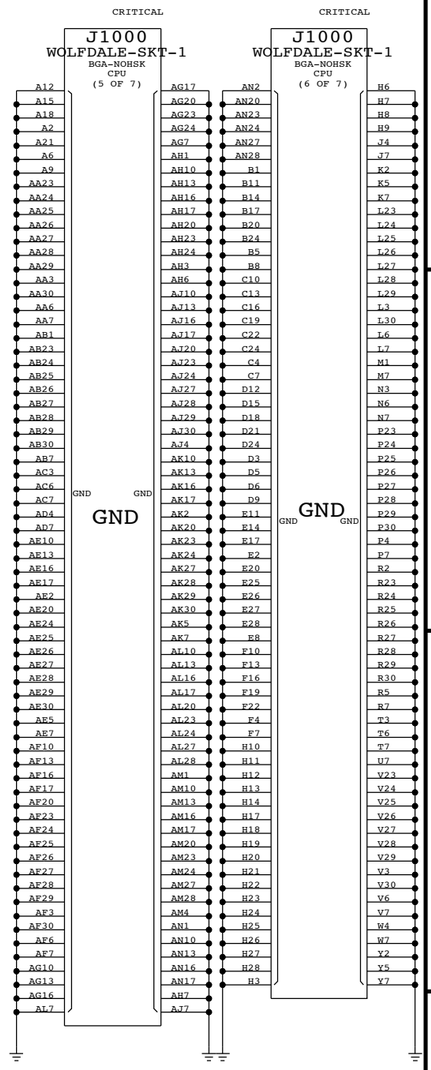
FSB VTT DECOUPLING



VCCP CORE DECOUPLING

(SEE VREG PAGE)





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Apple Inc.

DRAWING NUMBER 051-7845 SIZE D
REVISION A.0.0
BRANCH
PAGE 12 OF 110
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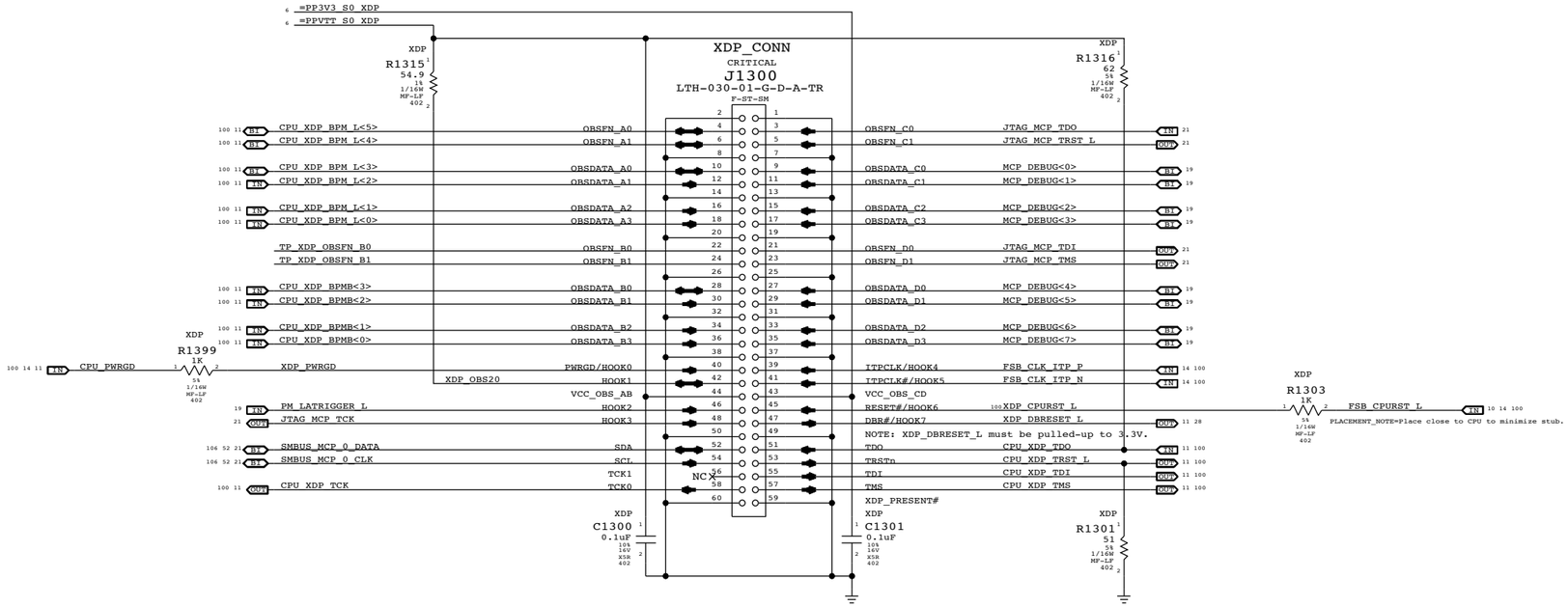
MCP79-specific pinout



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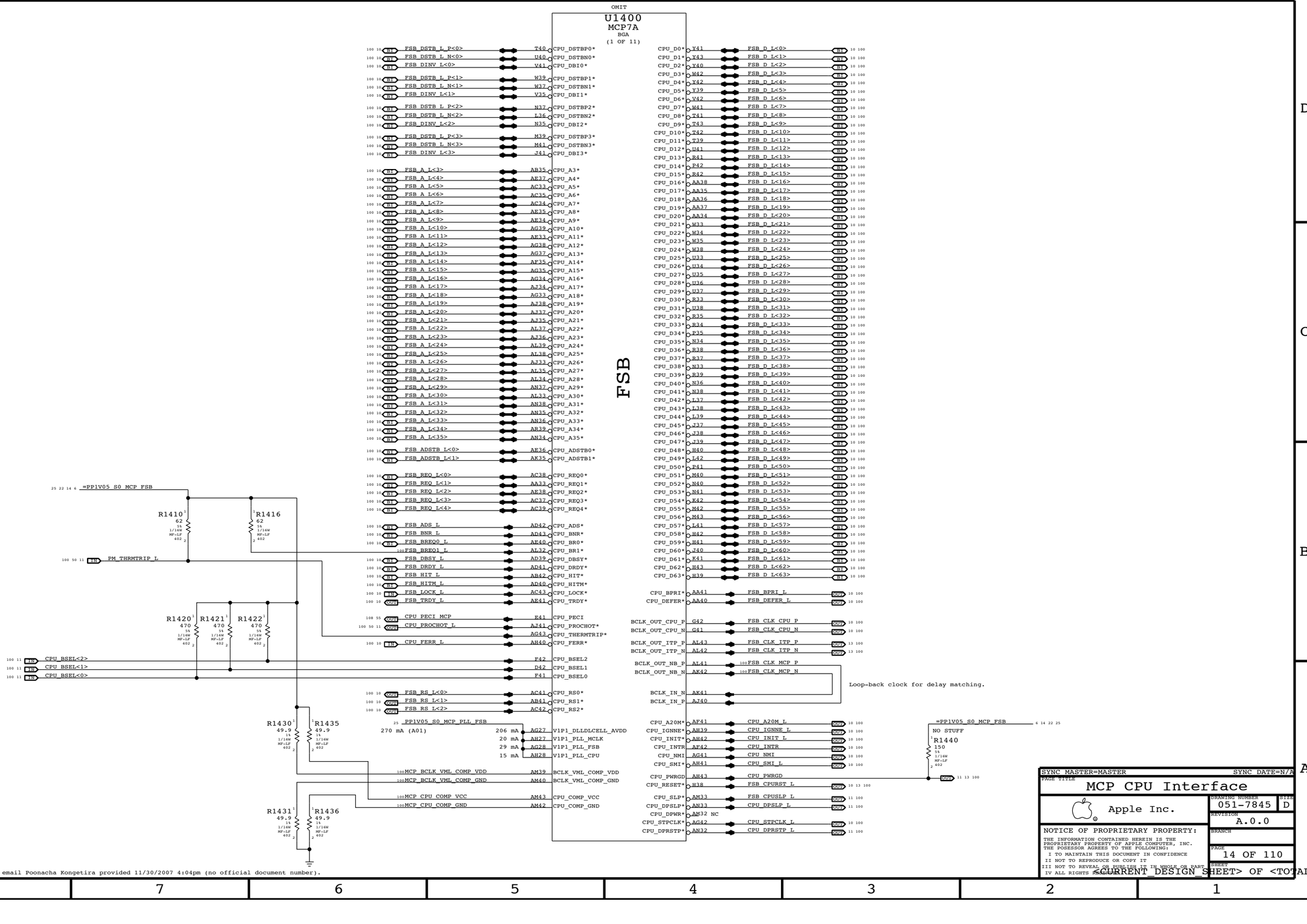
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U1400
MCP7A
BGA
(1 OF 11)
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CPU_PECI_MCP
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CPU_FERR_L
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U40 CPU_DSTBN0*
V41 CPU_DBI0*
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V35 CPU_DBI1*
N37 CPU_DSTBP2*
L36 CPU_DSTBN2*
N35 CPU_DBI2*
M39 CPU_DSTBP3*
M41 CPU_DSTBN3*
J41 CPU_DBI3*
AB35 CPU_A3*
AE37 CPU_A4*
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AC35 CPU_A6*
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CPU_DEFER* AA40 FSB_DEFER_L
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BCLK_OUT_CPU_N G41 FSB_CLK_CPU_N
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BCLK_OUT_NB_P AL41 FSB_CLK_MCP_P
BCLK_OUT_NB_N AK42 FSB_CLK_MCP_N
BCLK_IN_N AK41
BCLK_IN_P AJ40
Loop-back clock for delay matching.
CPU_A20M* AF41 CPU_A20M_L
CPU_IGNNE* AH39 CPU_IGNNE_L
CPU_INIT* AH42 CPU_INIT_L
CPU_INTR AF42 CPU_INTR
CPU_NMI AG41 CPU_NMI
CPU_SMI* AH41 CPU_SMI_L
CPU_PWRGD AH43 CPU_PWRGD
CPU_RESET* H38 FSB_CPURST_L
CPU_SLP* AM33 FSB_CPUSLP_L
CPU_DPSLP* AN33 CPU_DPSLP_L
CPU_DPWR* AM32 NC
CPU_STPCLK* AG42 CPU_STPCLK_L
CPU_DPRSTP* AN32 CPU_DPRSTP_L
=PP1V05_S0_MCP_FSB
NO STUFF
R1440 150 5% 1/16W MF-LF 402
PM_THRMTRIP_L
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F42 CPU_BSEL2
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PP1V05_S0_MCP_PLL_FSB
270 mA (A01)
206 mA AG27 V1P1_DLLDLCELL_AVDD
20 mA AH27 V1P1_PLL_MCLK
29 mA AG28 V1P1_PLL_FSB
15 mA AH28 V1P1_PLL_CPU
MCP_BCLK_VML_COMP_VDD
MCP_BCLK_VML_COMP_GND
AM39 BCLK_VML_COMP_VDD
AM40 BCLK_VML_COMP_GND
MCP_CPU_COMP_VCC
MCP_CPU_COMP_GND
AM43 CPU_COMP_VCC
AM42 CPU_COMP_GND
R1410 62 5% 1/16W MF-LF 402
R1416 62 5% 1/16W MF-LF 402
R1420 470 5% 1/16W MF-LF 402
R1421 470 5% 1/16W MF-LF 402
R1422 470 5% 1/16W MF-LF 402
R1430 49.9 1% 1/16W MF-LF 402
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Apple Inc.
DRAWING NUMBER 051-7845
SIZE D
REVISION A.0.0
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OMIT

U1400
MCP7A
BGA
(2 OF 11)

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MEMORY PARTITION 1

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MEM_B_DQ<46>	BA5	MDQ1_46				
MEM_B_DQ<45>	BA8	MDQ1_45				
MEM_B_DQ<44>	BC8	MDQ1_44				
MEM_B_DQ<43>	BB4	MDQ1_43				
MEM_B_DQ<42>	BC4	MDQ1_42	MRAS1*	AW16	MEM_B_RAS_L	
MEM_B_DQ<41>	BA7	MDQ1_41	MCAS1*	BA15	MEM_B_CAS_L	
MEM_B_DQ<40>	AY8	MDQ1_40	MWE1*	BA16	MEM_B_WE_L	
MEM_B_DQ<39>	BA9	MDQ1_39				
MEM_B_DQ<38>	BB10	MDQ1_38				
MEM_B_DQ<37>	BB12	MDQ1_37				
MEM_B_DQ<36>	AW12	MDQ1_36				
MEM_B_DQ<35>	BB8	MDQ1_35				
MEM_B_DQ<34>	BB9	MDQ1_34	MBA1_2	BB29	MEM_B_BA<2>	
MEM_B_DQ<33>	AY12	MDQ1_33	MBA1_1	BB18	MEM_B_BA<1>	
MEM_B_DQ<32>	BA12	MDQ1_32	MBA1_0	BB17	MEM_B_BA<0>	
MEM_B_DQ<31>	BC32	MDQ1_31				
MEM_B_DQ<30>	AW32	MDQ1_30				
MEM_B_DQ<29>	BA35	MDQ1_29				
MEM_B_DQ<28>	AY36	MDQ1_28				
MEM_B_DQ<27>	BA32	MDQ1_27	MA1_14	BA29	MEM_B_A<14>	
MEM_B_DQ<26>	BB32	MDQ1_26	MA1_13	BA14	MEM_B_A<13>	
MEM_B_DQ<25>	BA34	MDQ1_25	MA1_12	AW28	MEM_B_A<12>	
MEM_B_DQ<24>	AY35	MDQ1_24	MA1_11	BC28	MEM_B_A<11>	
MEM_B_DQ<23>	BC36	MDQ1_23	MA1_10	BA17	MEM_B_A<10>	
MEM_B_DQ<22>	AW36	MDQ1_22	MA1_9	BB28	MEM_B_A<9>	
MEM_B_DQ<21>	BA39	MDQ1_21	MA1_8	AY28	MEM_B_A<8>	
MEM_B_DQ<20>	AY40	MDQ1_20	MA1_7	BA28	MEM_B_A<7>	
MEM_B_DQ<19>	BA36	MDQ1_19	MA1_6	AY27	MEM_B_A<6>	
MEM_B_DQ<18>	BB36	MDQ1_18	MA1_5	BA27	MEM_B_A<5>	
MEM_B_DQ<17>	BA38	MDQ1_17	MA1_4	BA26	MEM_B_A<4>	
MEM_B_DQ<16>	AY39	MDQ1_16	MA1_3	BB26	MEM_B_A<3>	
MEM_B_DQ<15>	BB40	MDQ1_15	MA1_2	BA25	MEM_B_A<2>	
MEM_B_DQ<14>	AW40	MDQ1_14	MA1_1	BB25	MEM_B_A<1>	
MEM_B_DQ<13>	AV42	MDQ1_13	MA1_0	BA18	MEM_B_A<0>	
MEM_B_DQ<12>	AV41	MDQ1_12				
MEM_B_DQ<11>	BA40	MDQ1_11				
MEM_B_DQ<10>	BC40	MDQ1_10				
MEM_B_DQ<9>	AW42	MDQ1_9				
MEM_B_DQ<8>	AW41	MDQ1_8				
MEM_B_DQ<7>	AT40	MDQ1_7				
MEM_B_DQ<6>	AT41	MDQ1_6				
MEM_B_DQ<5>	AP41	MDQ1_5				
MEM_B_DQ<4>	AN40	MDQ1_4				
MEM_B_DQ<3>	AU40	MDQ1_3				
MEM_B_DQ<2>	AU41	MDQ1_2				
MEM_B_DQ<1>	AR41	MDQ1_1				
MEM_B_DQ<0>	AP42	MDQ1_0				
MEM_B_DM<7>	AT5	MDQM1_7	MCS1A_1*	BB14	MEM_B_CS_L<1>	
MEM_B_DM<6>	BA2	MDQM1_6	MCS1A_0*	BB16	MEM_B_CS_L<0>	
MEM_B_DM<5>	AY7	MDQM1_5				
MEM_B_DM<4>	BA11	MDQM1_4	MODT1A_1	BB13	MEM_B_ODT<1>	
MEM_B_DM<3>	BB34	MDQM1_3	MODT1A_0	AY15	MEM_B_ODT<0>	
MEM_B_DM<2>	BB38	MDQM1_2				
MEM_B_DM<1>	AY43	MDQM1_1	MCKE1A_1	AY31	MEM_B_CKE<1>	
MEM_B_DM<0>	AR42	MDQM1_0	MCKE1A_0	BB30	MEM_B_CKE<0>	

MEMORY CONTROL 1A

MCLK1A_2_P	BA42	TP_MEM_B_CLK2P
MCLK1A_2_N	BB42	TP_MEM_B_CLK2N
MCLK1A_1_P	BB22	MEM_B_CLK_P<1>
MCLK1A_1_N	BA22	MEM_B_CLK_N<1>
MCLK1A_0_P	BA19	MEM_B_CLK_P<0>
MCLK1A_0_N	AY19	MEM_B_CLK_N<0>

SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE
MCP Memory Interface

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D
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PAGE 15 OF 110
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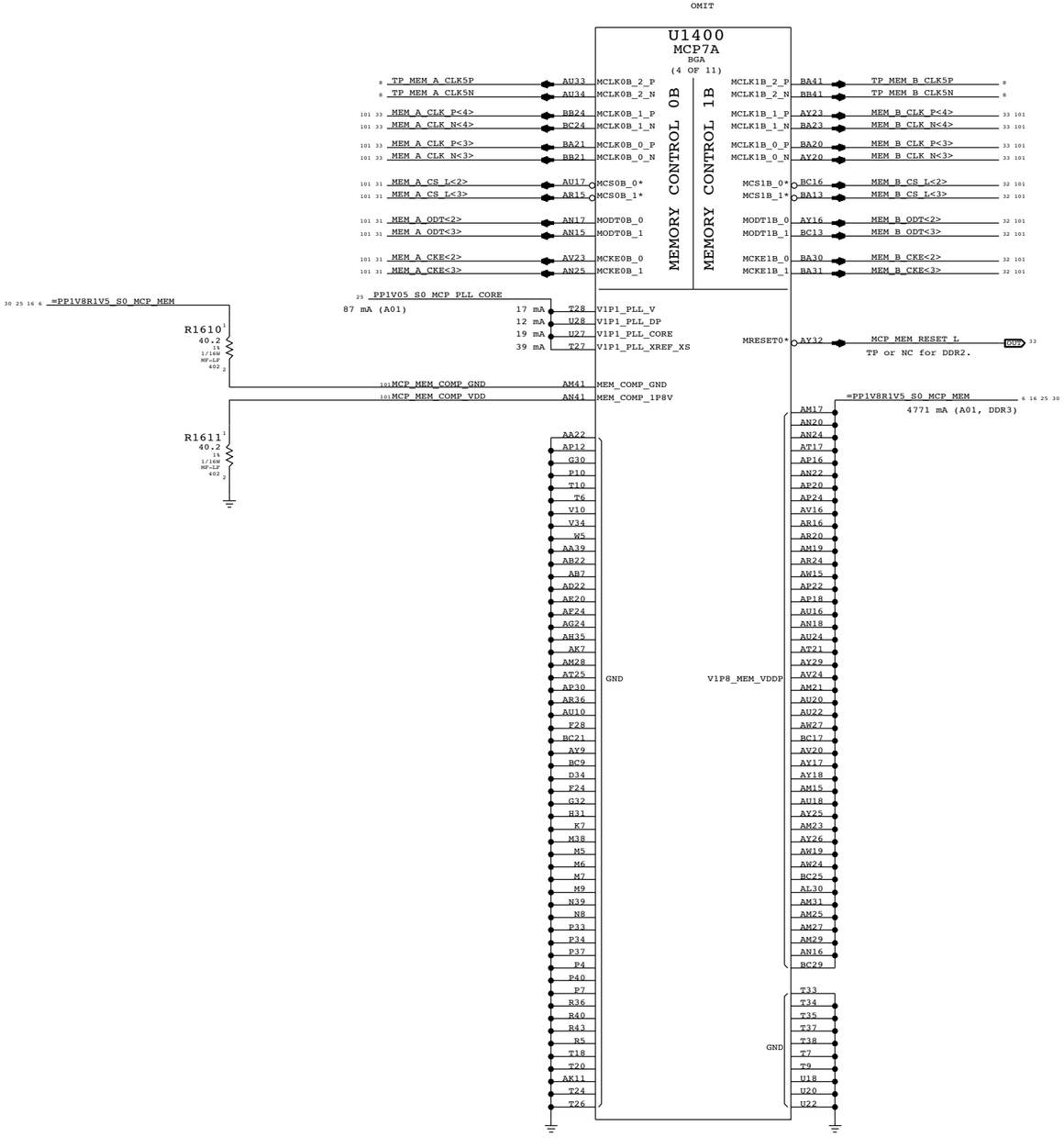

SYNC MASTER=MASTER						SYNC DATE=N/A	
PAGE TITLE: MCP MEMORY CNTRL & MISC							
Apple Inc.						DRAWING NUMBER: 051-7845	SIZE: D
						REVISION: A.0.0	
						BRANCH:	
						PAGE: 16 OF 110	
						SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>	

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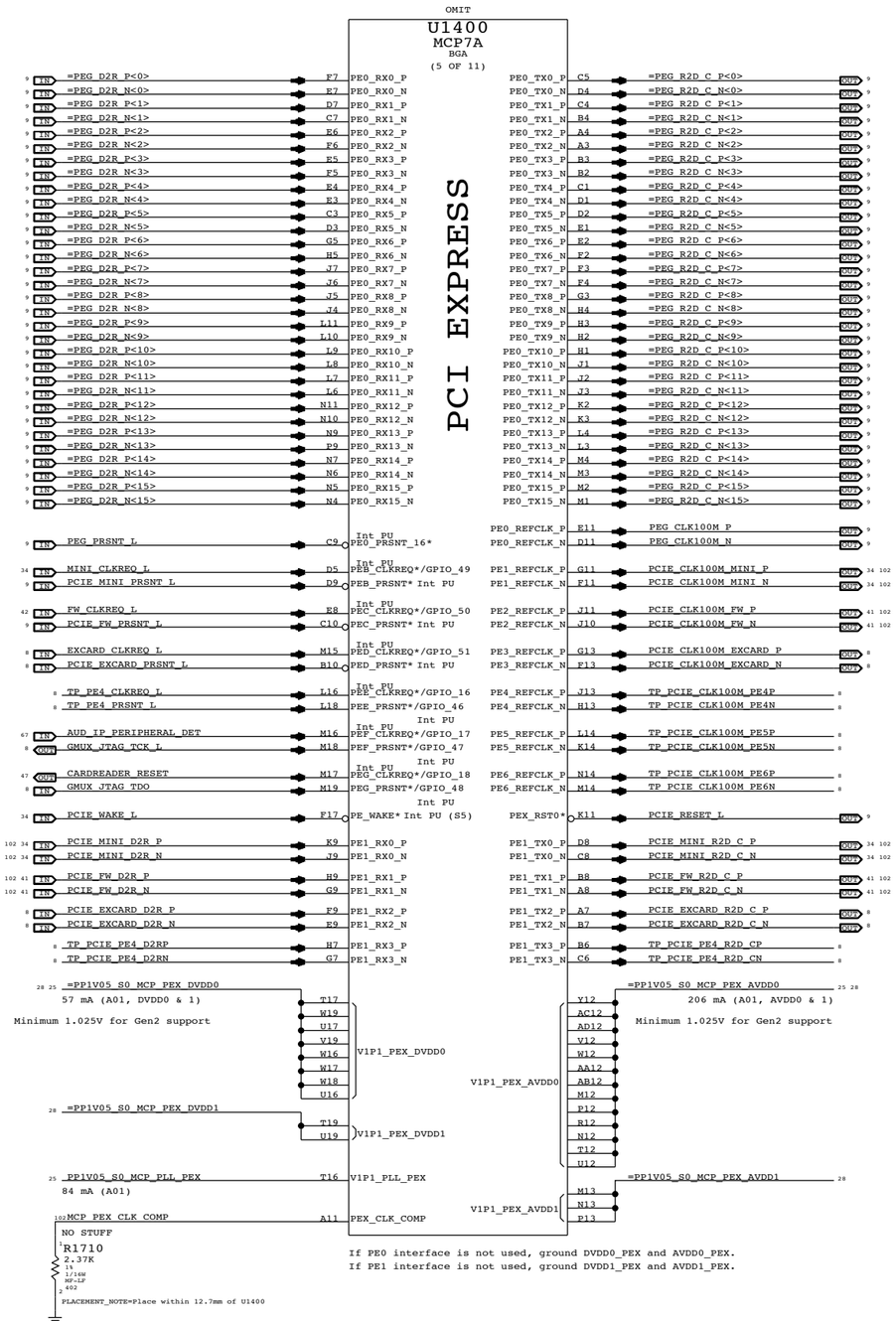

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PAGE TITLE
MCP PCIe Interfaces

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D

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PAGE 17 OF 110

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U1400
MCP7A
BGA
(6 OF 11)

LAN

		V3P3_DUAL_RMGT0	J24
		V3P3_DUAL_RMGT1	K24
		V1P0_DUAL_RMGT_0	U23
		V1P0_DUAL_RMGT_1	V23
104 37	IN	ENET_RXD<0>	C23
104 37	IN	ENET_RXD<1>	B23
104 37	IN	ENET_RXD<2>	E24
104 37	IN	ENET_RXD<3>	A24
104 37	IN	ENET_CLK125M_RXCLK	A23
104 37	IN	ENET_RX_CTRL	C22
9	IN	=MCP_MII_RXER	F23
9	IN	=MCP_MII_COL	B26
9	IN	=MCP_MII_CRS	B22
8	IN	TP_ENET_INTR_L	J22
25		PP1V05_ENET_MCP_PLL_MAC	T23
		5 mA (A01)	
104		MCP_MII_COMP_VDD	C27
104		MCP_MII_COMP_GND	B27
		TP_MCP_RGB_DAC_RSET	C39
		TP_MCP_RGB_DAC_VREF	B38
8	OUT	MCP_TV_DAC_RSET	E36
8	OUT	MCP_TV_DAC_VREF	A35
8	IN	MCP_CLK27M_XTALIN	C38
8	OUT	MCP_CLK27M_XTALOUT	D38
53	BI	LPCPLUS_GPIO	E16
93	IN	DP_IG_CA_DET	B15
89	OUT	LVDS_IG_BKL_PWM	E39
89	OUT	LVDS_IG_BKL_ON	E37
89	OUT	LVDS_IG_PANEL_PWR	F40
9	OUT	=MCP_HDMI_TXC_P	D35
9	OUT	=MCP_HDMI_TXC_N	E35
9	OUT	=MCP_HDMI_TXD_P<0>	G35
9	OUT	=MCP_HDMI_TXD_N<0>	F35
9	OUT	=MCP_HDMI_TXD_P<1>	F33
9	OUT	=MCP_HDMI_TXD_N<1>	G33
9	OUT	=MCP_HDMI_TXD_P<2>	J33
9	OUT	=MCP_HDMI_TXD_N<2>	H33
107 93	OUT	DP_IG_AUX_CH_P	D43
107 93	OUT	DP_IG_AUX_CH_N	C43
9	IN	=DVI_HPD_GMUX_INT	C31
9	IN	=MCP_HDMI_HPD	F31
26		=PP3V3R1V8_S0_MCP_IFP_VDD	M27
		190 mA (A01, 1.8V)	M26
26		PP3V3_S0_MCP_VPLL	M28
		16 mA (A01)	M29
26		=PP1V05_S0_MCP_HDMI_VDD	T25
		95 mA (A01)	
107 26	OUT	MCP_HDMI_RSET	J31
107 26	OUT	MCP_HDMI_VPROBE	J30

V3P3_DUAL_RMGT0	J24	=PP3V3_ENET_MCP_RMGT	18 25 38
V3P3_DUAL_RMGT1	K24	83 mA (A01)	
V1P0_DUAL_RMGT_0	U23	=PP1V05_ENET_MCP_RMGT	25 38
V1P0_DUAL_RMGT_1	V23	131 mA (A01)	
MII_VREF	E28	MCP_MII_VREF	IN 25
MII_TXD0	B24	ENET_TXD<0>	OUT 37 104
MII_TXD1	C24	ENET_TXD<1>	OUT 37 104
MII_TXD2	C25	ENET_TXD<2>	OUT 37 104
MII_TXD3	D25	ENET_TXD<3>	OUT 37 104
MII_TXCLK	D24	ENET_CLK125M_TXCLK	OUT 37 104
MII_TXEN	C26	ENET_TX_CTRL	OUT 37 104
MII_MDC	D21	ENET_MDC	OUT 37 104
MII_MDIO	C21	ENET_MDIO	BI 37 104
MII_PWRDWN/GPIO_37	G23	TP_ENET_PWRDWN_L	8
BUF_25MHZ	E23	MCP_CLK25M_BUF0_R	OUT 38 104
MII_RESET*	J23	ENET_RESET_L	OUT 37
		PP3V3_S0_MCP_DAC	26
V3P3_RGBDAC_VDD	J32	103 mA	206 mA (A01)
V3P3_TVDAC_VDD	K32	103 mA	
DDC_CLK0	B31	MCP_DDC_CLK0	
DDC_DATA0	A31	MCP_DDC_DATA0	

DACS

RGB ONLY

RGB_DAC_RED	B39	TP_MCP_RGB_RED	
RGB_DAC_GREEN	A39	TP_MCP_RGB_GREEN	
RGB_DAC_BLUE	B40	TP_MCP_RGB_BLUE	
RGB_DAC_HSYNC	A40	TP_MCP_RGB_HSYNC	8
RGB_DAC_VSYNC	A41	TP_MCP_RGB_VSYNC	8

TV / Component
C / Pr
Y / Y
Comp / Pb

TV_DAC_RED	A36	CRT_IG_R_C_PR	OUT 8
TV_DAC_GREEN	B36	CRT_IG_G_Y_Y	OUT 8
TV_DAC_BLUE	C36	CRT_IG_B_COMP_PB	OUT 8
TV_DAC_HSYNC/GPIO_44	D36	CRT_IG_HSYNC	OUT 8
TV_DAC_VSYNC/GPIO_45	C37	CRT_IG_VSYNC	OUT 8

FLAT PANEL

IFPA_TXC_P	B35	LVDS_IG_A_CLK_P	OUT 89 107
IFPA_TXC_N	C35	LVDS_IG_A_CLK_N	OUT 89 107
IFPA_TXD0_P	B32	LVDS_IG_A_DATA_P<0>	OUT 89 107
IFPA_TXD0_N	A32	LVDS_IG_A_DATA_N<0>	OUT 89 107
IFPA_TXD1_P	D32	LVDS_IG_A_DATA_P<1>	OUT 89 107
IFPA_TXD1_N	C32	LVDS_IG_A_DATA_N<1>	OUT 89 107
IFPA_TXD2_P	D33	LVDS_IG_A_DATA_P<2>	OUT 89 107
IFPA_TXD2_N	C33	LVDS_IG_A_DATA_N<2>	OUT 89 107
IFPA_TXD3_P	B34	LVDS_IG_A_DATA_P<3>	OUT 89 107
IFPA_TXD3_N	C34	LVDS_IG_A_DATA_N<3>	OUT 89 107
IFPB_TXC_P	L31	LVDS_IG_B_CLK_P	OUT 89 107
IFPB_TXC_N	K31	LVDS_IG_B_CLK_N	OUT 89 107
IFPB_TXD4_P	J29	LVDS_IG_B_DATA_P<0>	OUT 89 107
IFPB_TXD4_N	H29	LVDS_IG_B_DATA_N<0>	OUT 89 107
IFPB_TXD5_P	L29	LVDS_IG_B_DATA_P<1>	OUT 89 107
IFPB_TXD5_N	K29	LVDS_IG_B_DATA_N<1>	OUT 89 107
IFPB_TXD6_P	L30	LVDS_IG_B_DATA_P<2>	OUT 89 107
IFPB_TXD6_N	K30	LVDS_IG_B_DATA_N<2>	OUT 89 107
IFPB_TXD7_P	N30	LVDS_IG_B_DATA_P<3>	OUT 89 107
IFPB_TXD7_N	M30	LVDS_IG_B_DATA_N<3>	OUT 89 107
DDC_CLK2/GPIO_23	C30	LVDS_IG_DDC_CLK	OUT 89
DDC_DATA2/GPIO_24	B30	LVDS_IG_DDC_DATA	BI 89
DDC_CLK3	D31	=MCP_HDMI_DDC_CLK	OUT 9
DDC_DATA3	E31	=MCP_HDMI_DDC_DATA	BI 9
IFPAB_RSET	E32	MCP_IFPAB_RSET	OUT 26 102
IFPAB_VPROBE	G31	MCP_IFPAB_VPROBE	OUT 26 102

38 25 18 =PP3V3_ENET_MCP_RMGT

R1810 49.9 1% 1/16W MF-LF 402

R1811 49.9 1% 1/16W MF-LF 402

20 6 =PP3V3_S5_MCP_GPIO

R1820 47K 5% 1/16W MF-LF 402

R1850 10K 5% 1/16W MF-LF 402

=PP3V3_S0_MCP_GPIO 6 19 21

R1860 100K 5% 1/16W MF-LF 402

R1861 100K 5% 1/16W MF-LF 402

Network Interface Select

Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable:

Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

MCP Signal	Interface Mode: TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CHP/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HPD_DET.
NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.

NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V

(See below)

(See below)

GPIOs 57-59 (if LCD panel is used):

In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT:

Alias to DVI_HPD for systems using IFP for DVI.
Alias to GMUX_INT for systems with GMUX.
Alias to HPLUG_DET2 for other systems.
Pull-down (20k) required in all cases.

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PAGE TITLE
MCP Ethernet & Graphics

Apple Inc.

DRAWING NUMBER 051-7845
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REVISION A.0.0
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PAGE 18 OF 110
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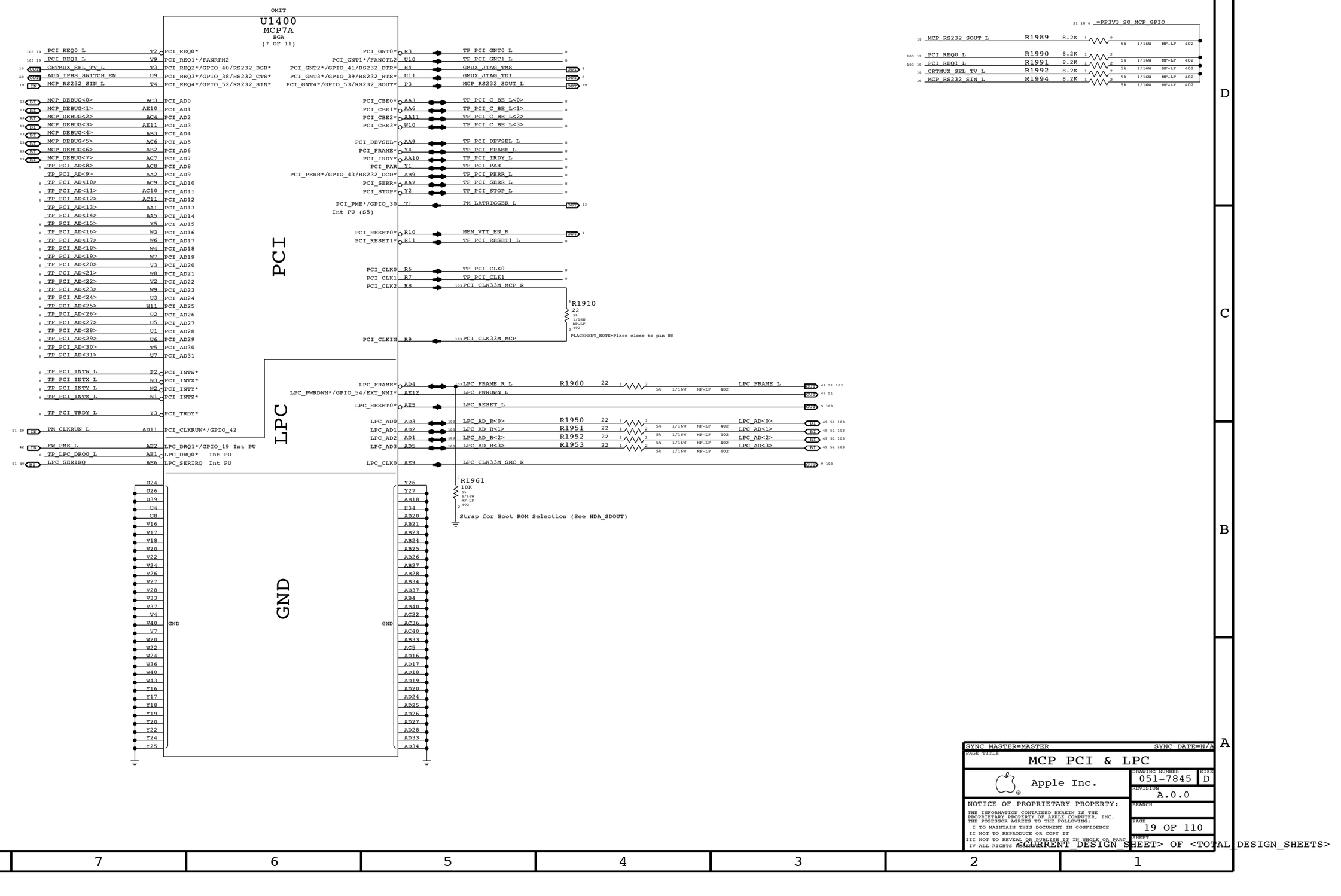

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PAGE TITLE	MCP PCI & LPC
Apple Inc.	DRAWING NUMBER 051-7845 SIZE D
	REVISION A.0.0
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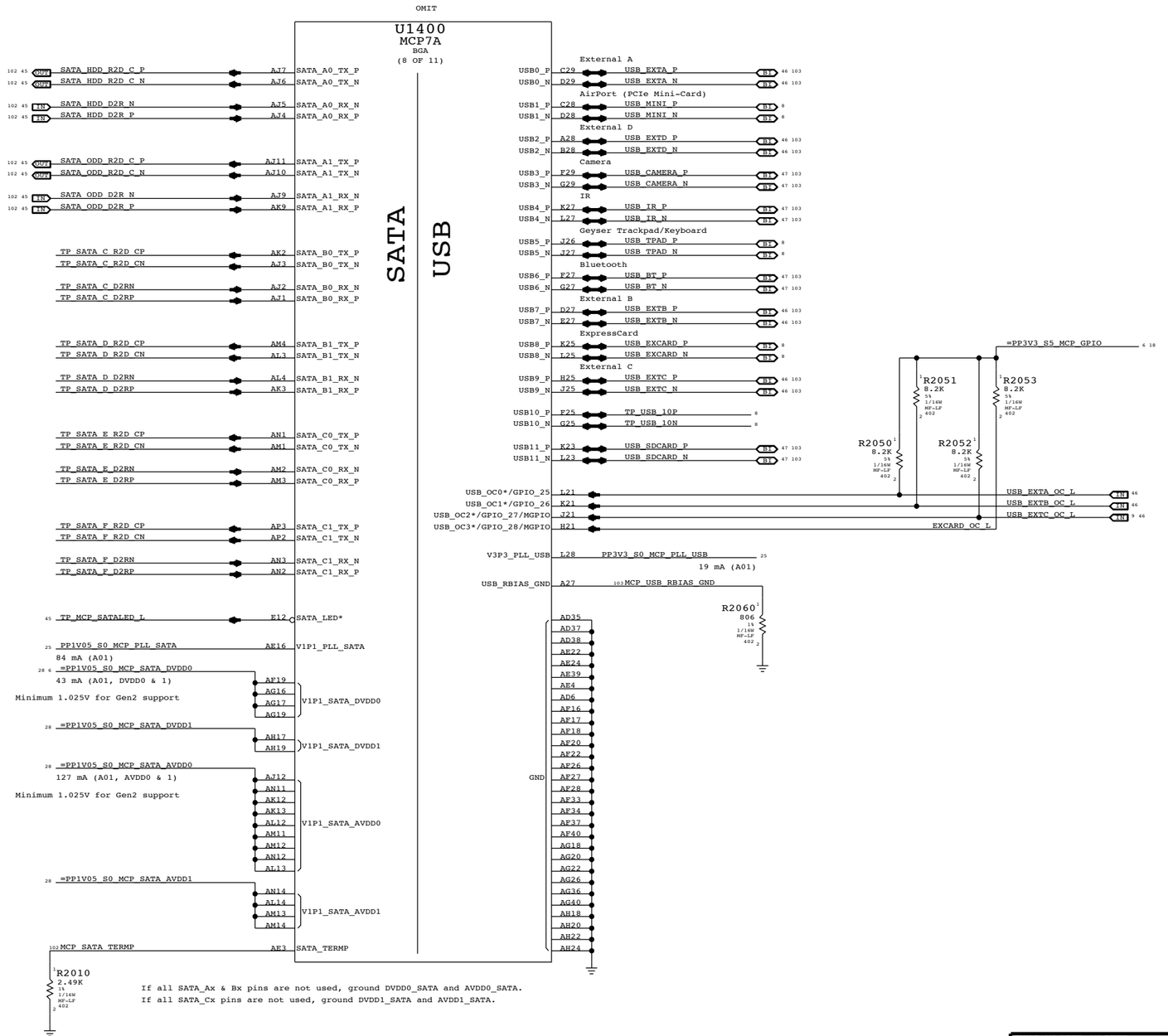

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Apple Inc.	DRAWING NUMBER: 051-7845 SIZE: D
	REVISION: A.0.0
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MCP7A
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HDA

HDA_SDIN0	G15	HDA_SDATA_IN0	Int PD
TP_MLB_RAM_SIZE	J14	GPIO_2/HDA_SDATA_IN1/PS2_KB_CLK	Int PD
TP_MLB_RAM_VENDOR (MXM_OK for MXM systems)	J15	GPIO_3/HDA_SDATA_IN2/PS2_KB_DATA	Int PD
MCP_HDA_PULLDN_COMP	A15	HDA_PULLDN_COMP	
PP1V05_S0_MCP_PLL_NV	AE18	V1P1_PLL_NV_H	20 mA
	AE17	V1P1_PLL_SP_SPREF	17 mA
=SPI_CS1_R_L_USE_MLB	L24	GPIO_1/PWRDN_OK/SPI_CS1	
SMC_ADAPTER_EN	L26	GPIO_12/SUS_STAT*/ACCLMTR_EXT_TRIG	
TP_SB_A20GATE	K13	A20GATE Int PU	
TP_MCP_KBDRSTIN_L	L13	KBRDRSTIN* Int PU	
SMC_WAKE_SCI_L	C19	SIO_PME* Int PU (S5)	
SMC_RUNTIME_SCI_L	C18	EXT_SMI*/GPIO_32 Int PU (S5)	
SM_INTRUDER_L	B20	INTRUDER*	
TP_MCP_LID_L	M25	LID* Int PU (S5)	
PM_BATLOW_L	M24	LLB* Int PU (S5)	
	NC M22	CPU_DPRSLPVR	
PM_PWRBTN_L	C16	PWRBTN* Int PU (S5)	
PM_SYSRST_DEBOUNCE_L	D16	RSTBTN* Int PU	
RTC_RST_L	C20	RTC_RST*	
PM_RSMRST_L	D20	PWRGD_SB	
MCP_PS_PWRGD	E20	PS_PWRGD	
MCP_CPU_VLD	C17	CPU_VLD	
JTAG_MCP_TDI	E19	JTAG_TDI Int PU	
JTAG_MCP_TDO	F19	JTAG_TDO	
JTAG_MCP_TMS	J19	JTAG_TMS Int PU	
JTAG_MCP_TRST_L	J18	JTAG_TRST*	
JTAG_MCP_TCK	G19	JTAG_TCK	
MCP_CLK25M_XTALIN	A16	XTALIN	
MCP_CLK25M_XTALOUT	B16	XTALOUT	
RTC_CLK32K_XTALIN	A19	XTALIN_RTC	
RTC_CLK32K_XTALOUT	B19	XTALOUT_RTC	

=PP3V3R1V5_S0_MCP_HDA — 7 mA (A01)

R2110 49.9 1% 1/16W MF-LF 402 — =PP3V3R1V5_S0_MCP_HDA

R2120 49.9K 1% 1/16W MF-LF 402 — =PP3V3_G3_RTC

R2121 49.9K 1% 1/16W MF-LF 402

R2150 10K 5% 1/16W MF-LF 402

R2151 100K 5% 1/16W MF-LF 402

R2160 8.2K 5% 1/16W MF-LF 402 — =PP3V3R1V5_S0_MCP_HDA

V3P3_DUAL_HDA_0	J16		
V3P3_DUAL_HDA_1	K16		
HDA_SDATA_OUT	F15	HDA_SDOUT_R	R2170 22 5% 1/16W MF-LF 402 → HDA_SDOUT
HDA_BITCLK	E15	HDA_BIT_CLK_R	R2171 22 5% 1/16W MF-LF 402 → HDA_BIT_CLK
HDA_RESET*	K15	HDA_RST_R_L	R2172 22 5% 1/16W MF-LF 402 → HDA_RST_L
HDA_SYNC	L15	HDA_SYNC_R	R2173 22 5% 1/16W MF-LF 402 → HDA_SYNC

MISC

GPIO_4/HDA_DOCK_EN*/PS2_MS_CLK	K17	MCP_GPIO_4	
GPIO_5/HDA_DOCK_RST*/PS2_MS_DATA	L17	AUD_I2C_INT_L	
SLP_S3*	G17	PM_SLP_S3_L	
SLP_RMGT*	J17	PM_SLP_RMGT_L	
SLP_S5*	H17	PM_SLP_S4_L	
THERM_DIODE_P	B11	MCP_THMDIODE_P	
THERM_DIODE_N	C11	MCP_THMDIODE_N	
GPIO_13/MCP_VID0	L20	MCP_VID<0>	
GPIO_14/MCP_VID1	M20	MCP_VID<1>	
GPIO_15/MCP_VID2	M21	MCP_VID<2>	
SPKR	C13	MCP_SPKR	
SMB_CLK0	L19	SMBUS_MCP_0_CLK	
SMB_DATA0	K19	SMBUS_MCP_0_DATA	
SMB_CLK1/MSMB_CLK	G21	SMBUS_MCP_1_CLK	
SMB_DATA1/MSMB_DATA	F21	SMBUS_MCP_1_DATA	
SMB_ALERT*/GPIO_64	M23	AP_PWR_EN	
(MGPIO2) FANRPM0/GPIO_60	B12	MEM_EVENT_L	
FANCTL0/GPIO_61	A12	ODD_PWR_EN_L	
(MGPIO3) FANRPM1/GPIO_63	D12	SMC_IG_THROTTLE_L	
FANCTL1/GPIO_62	C12	ARB_DETECT	
CPUVDD_EN	D17	MCP_CPUVDD_EN	
GPIO_10/SPI_CS0	C14	SPI_CS0_R_L	
GPIO_11/SPI_CLK	D13	SPI_CLK_R	
GPIO_8/SPI_DI	C15	SPI_MISO	
GPIO_9/SPI_DO	B14	SPI_MOSI_R	
SUS_CLK/GPIO_34	B18	PM_CLK32K_SUSCLK_R	
BUF_SIO_CLK	AE7	TP_MCP_BUF_SIO_CLK	
TEST_MODE_EN	K22	MCP_TEST_MODE_EN	
PKG_TEST	L22		

R2163 10K 5% 1/16W MF-LF 402

R2190 1K 1% 1/16W MF-LF 402

=PP3V3_S0_MCP — BOOT_MODE_SAFE

R2180 10K 5% 1/16W MF-LF 402

BOOT_MODE_USER

R2181 10K 5% 1/16W MF-LF 402

USER mode: Normal
SAFE mode: For ROMSIP recovery

Connects to SMC for automatic recovery.

BIOS Boot Select

I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L

R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.

NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

BUF_SIO_CLK Frequency

Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

SPI Frequency Select

Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

HDA Output Caps

For EMI Reduction on HDA interface

HDA_SDOUT_R, HDA_BIT_CLK_R, HDA_RST_R_L, HDA_SYNC_R

C2170 10PF 5% 50V CERM 402

C2172 10PF 5% 50V CERM 402

C2171 10PF 5% 50V CERM 402

C2173 10PF 5% 50V CERM 402

=PP3V3_S0_MCP_GPIO

R2140 10K 5% 1/16W MF-LF 402

R2141 10K 5% 1/16W MF-LF 402

R2142 10K 5% 1/16W MF-LF 402

R2143 10K 5% 1/16W MF-LF 402

MCP_GPIO_4
AUD_I2C_INT_L
MEM_EVENT_L
SMC_IG_THROTTLE_L

ARB_DETECT

R2147 100K 5% 1/16W MF-LF 402

=PP3V3_S3_MCP_GPIO

R2154 100K 5% 1/16W MF-LF 402

AP_PWR_EN

MCP_VID<0>
MCP_VID<1>
MCP_VID<2>

R2155 22K 5% 1/16W MF-LF 402

R2156 22K 5% 1/16W MF-LF 402

R2157 22K 5% 1/16W MF-LF 402

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SYNC MASTER=MASTER — SYNC DATE=N/A

PAGE TITLE: MCP HDA & MISC

Apple Inc.

DRAWING NUMBER: 051-7845 — SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 21 OF 110

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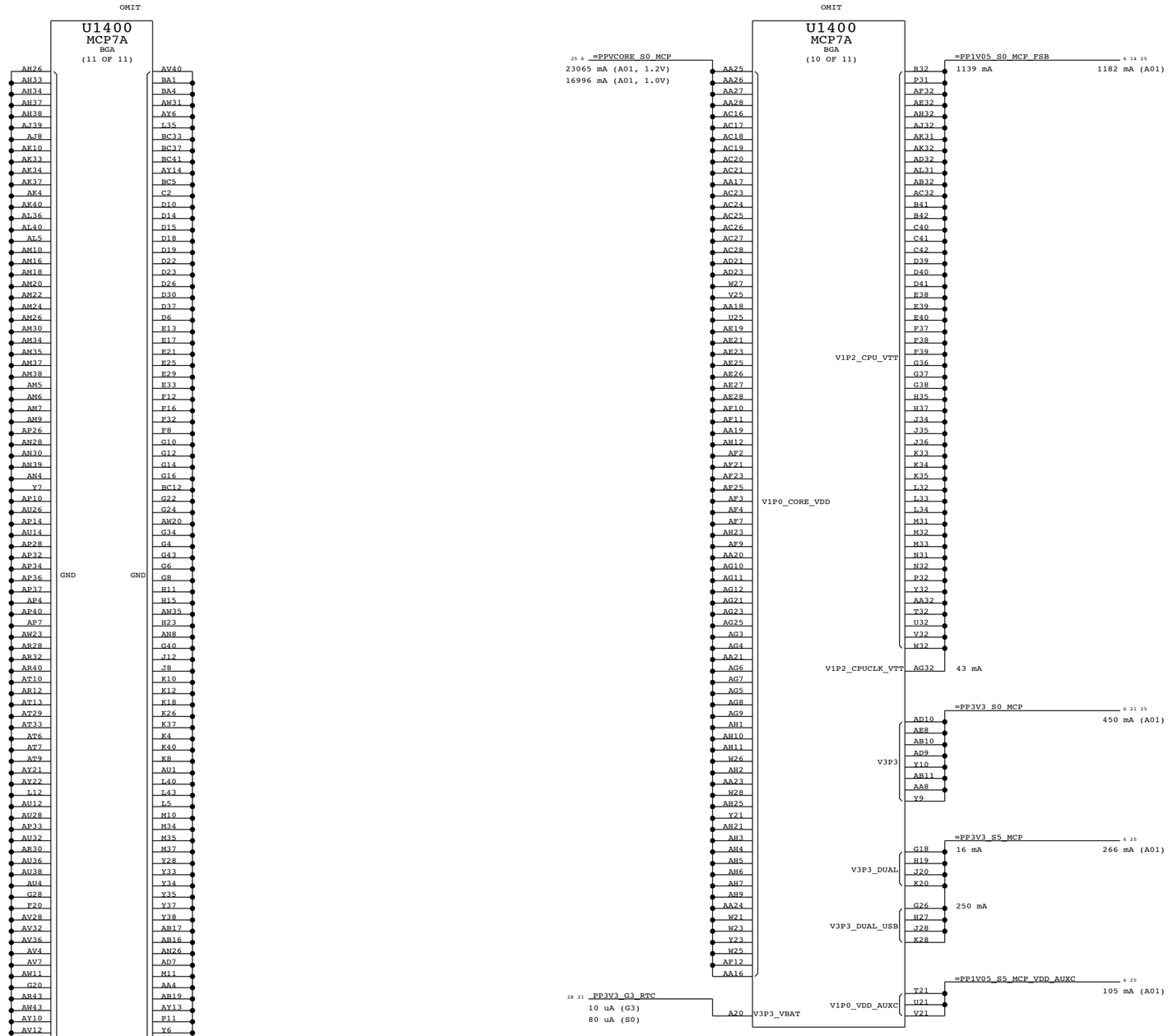

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SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE
MCP Power & Ground

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D

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PAGE 22 OF 110

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8	7	6	5	4	3	2	1

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PAGE TITLE

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DRAWING NUMBER 051-7845 SIZE D

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PAGE 23 OF 110

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8 7 6 5 4 3 2 1

D C B A

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PAGE 24 OF 110

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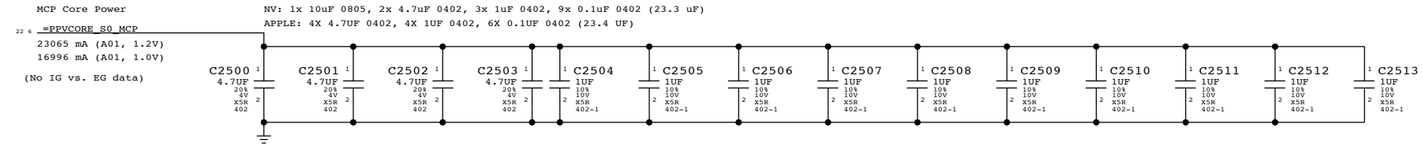
8 7 6 5 4 3 2 1



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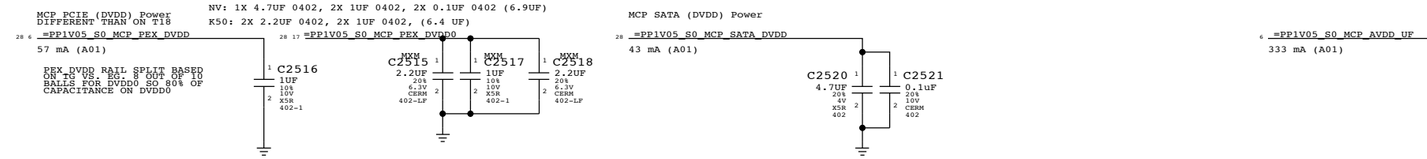
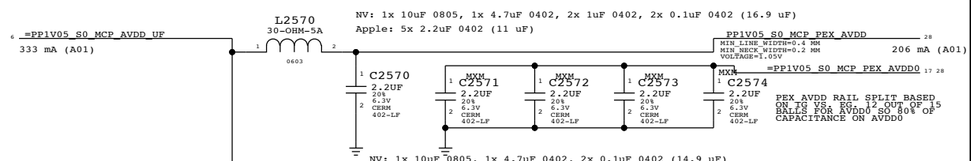
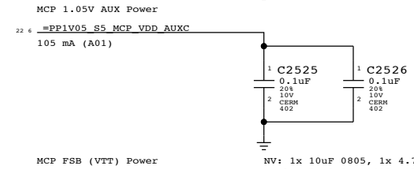
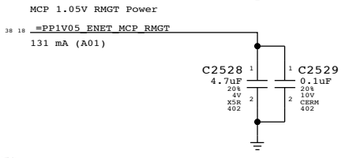
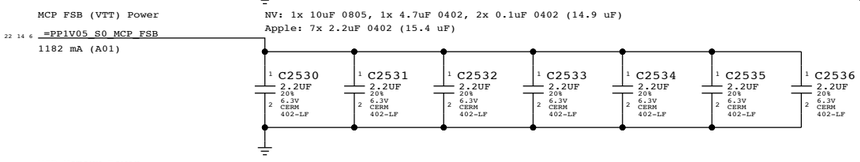
116S0004	2	RES,0,5%,0402	C2574,C2518	IG

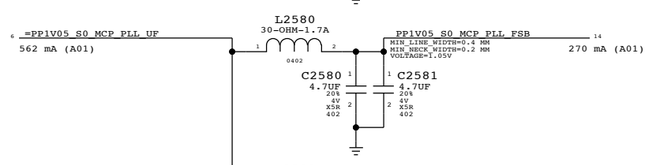


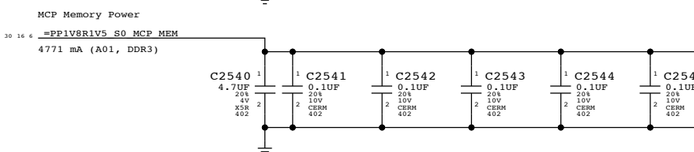


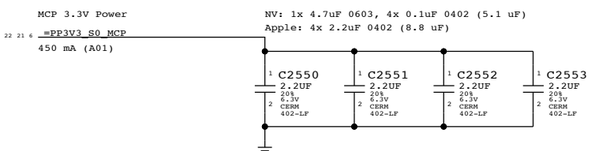


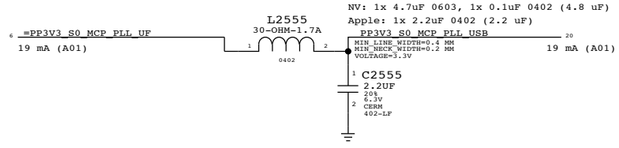


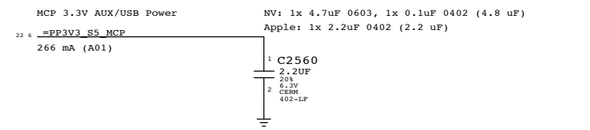


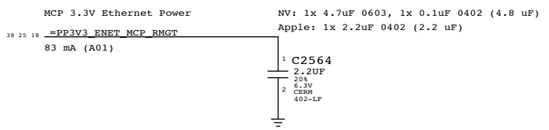


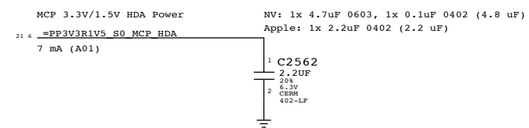


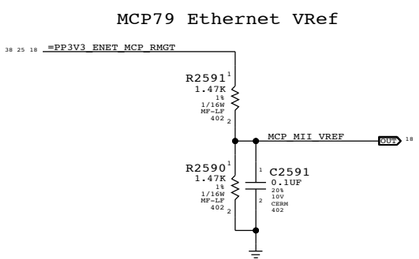


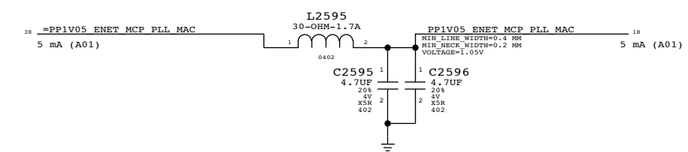












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SYNC MASTER=K51 SYNC DATE=12/08/2008

PAGE TITLE
MCP Standard Decoupling

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D
REVISION A.0.0
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PAGE 25 OF 110
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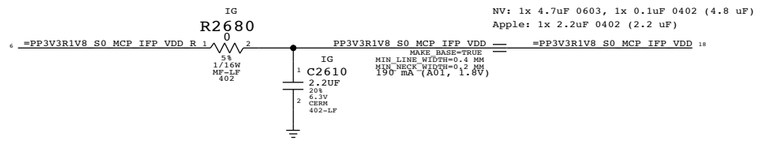
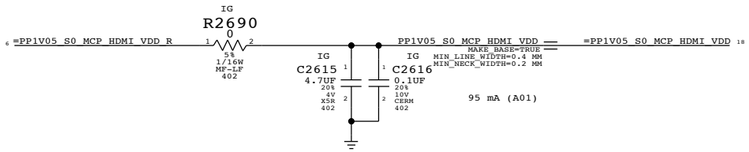
WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

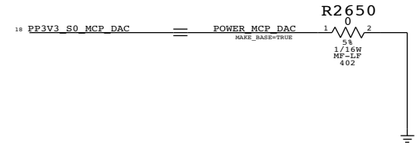


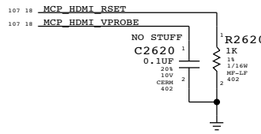
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

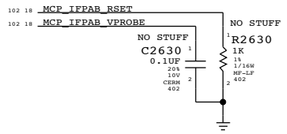
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	1	RES,0,5%,402	C2610		MXM



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	1	RES,0,5%,402	C2616		MXM

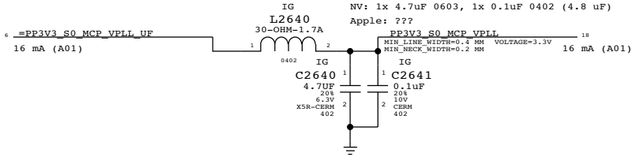






WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: ???



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	1	RES,0,5%,402	C2641		MXM

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PAGE TITLE: MCP Graphics Support

Apple Inc.

DRAWING NUMBER: 051-7845 SIZE: D

REVISION: A.0.0

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PAGE: 26 OF 110

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D C B A

SYNC MASTER=K51 SYNC DATE=12/08/2008

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DRAWING NUMBER 051-7845 SIZE D

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PAGE 27 OF 110

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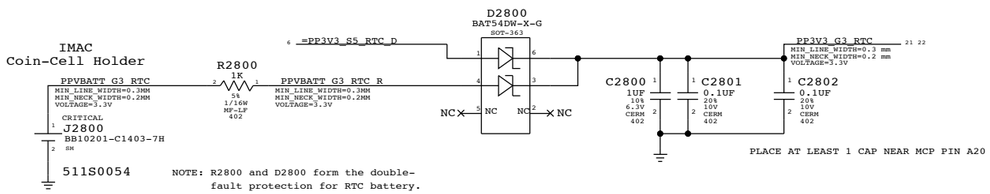
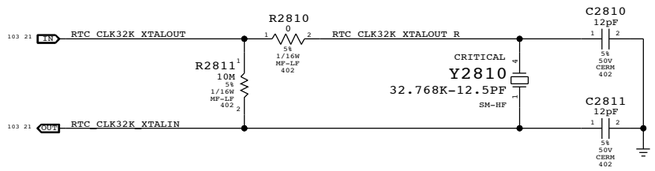
RTC Power Sources

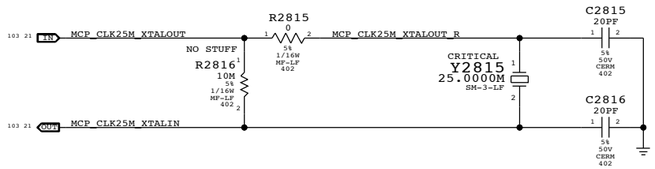


NOTE: R2800 and D2800 form the double-fault protection for RTC battery.

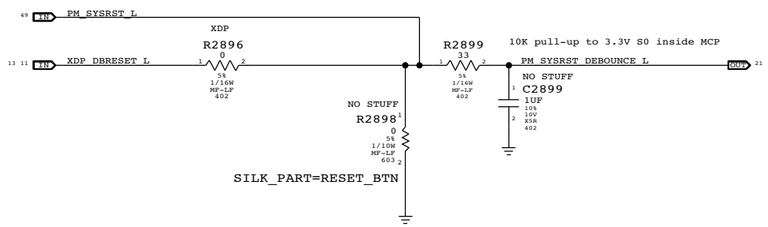
RTC Crystal



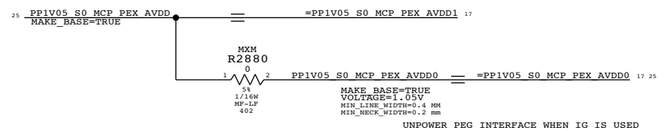
MCP 25MHz Crystal

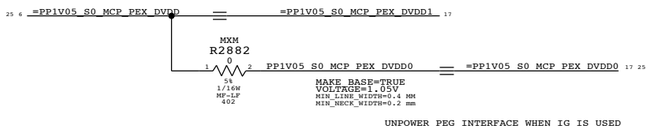


Reset Button

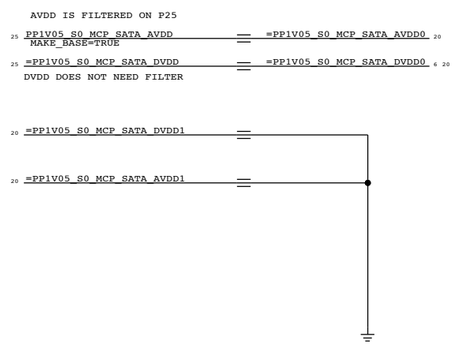


PEG POWER ALIAS/OPTION TO GND UNUSED POWER PIN





SATA ALIAS/GROUNDING UNUSED DVDD1 AND AVDD1



SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE: SB Misc

Apple Inc.

DRAWING NUMBER: 051-7845 SIZE: D

REVISION: A.0.0

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PAGE: 28 OF 110

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Page Notes

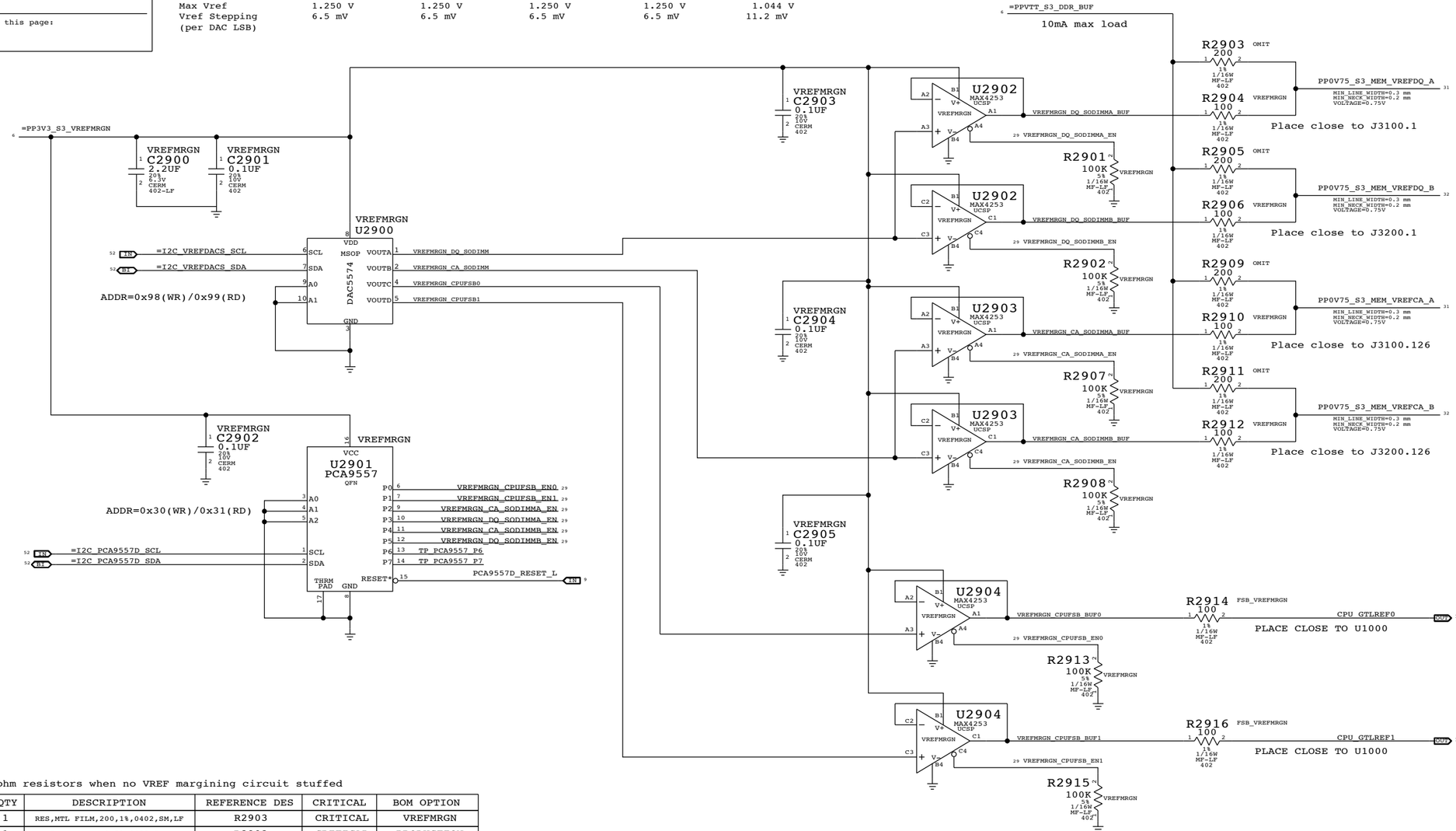
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
PRODUCTION

DAC channel	MEM A VREF DQ A	MEM A VREF CA B	MEM B VREF DQ A	MEM B VREF CA B	CPU FSB VREF C
Min DAC code	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2903	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	PRODUCTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2905	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	PRODUCTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2909	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	PRODUCTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2911	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	PRODUCTION

SYNC MASTER=MASTER SYNC DATE=MASTER

PAGE TITLE
FSB/DDR3 Vref Margining

Apple Inc.

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DIMM A (FURTHER FROM MCP)

CAPS TO COUPLE MCP 1V5_S0_MEM

DIMM B (CLOSER TO MCP)

30 25 16 6 =PP1V8R1V5_S0_MCP_MEM

C3016 0.1UF 20% 10V CERM 402
C3017 0.1UF 20% 10V CERM 402
C3018 0.1UF 20% 10V CERM 402
C3019 0.1UF 20% 10V CERM 402
C3010 0.1UF 20% 10V CERM 402

30 25 16 6 =PP1V8R1V5_S0_MCP_MEM

C3025 0.1UF 20% 10V CERM 402
C3026 0.1UF 20% 10V CERM 402
C3027 0.1UF 20% 10V CERM 402
C3028 0.1UF 20% 10V CERM 402
C3029 0.1UF 20% 10V CERM 402
C3020 0.1UF 20% 10V CERM 402
C3021 0.1UF 20% 10V CERM 402
C3022 0.1UF 20% 10V CERM 402
C3023 0.1UF 20% 10V CERM 402
C3014 0.1UF 20% 10V CERM 402
C3030 0.1UF 20% 10V CERM 402
C3031 0.1UF 20% 10V CERM 402
C3032 0.1UF 20% 10V CERM 402
C3033 0.1UF 20% 10V CERM 402
C3034 0.1UF 20% 10V CERM 402
C3035 0.1UF 20% 10V CERM 402

EXTRA DECOUPLING CAPS FOR MCP MEM RAIL

30 25 16 6 =PP1V8R1V5_S0_MCP_MEM
4771 mA (A01, DDR3)

C3041 0.1UF 20% 10V CERM 402
C3042 0.1UF 20% 10V CERM 402
C3044 0.1UF 20% 10V CERM 402
C3046 0.1UF 20% 10V CERM 402
C3040 1UF 10% 6.3V CERM 402
C3043 1UF 10% 6.3V CERM 402
C3045 1UF 10% 6.3V CERM 402
C3047 1UF 10% 6.3V CERM 402
C3048 1UF 10% 6.3V CERM 402
C3049 1UF 10% 6.3V CERM 402
C3090 1UF 10% 6.3V CERM 402
C3091 1UF 10% 6.3V CERM 402
C3092 1UF 10% 6.3V CERM 402
C3093 1UF 10% 6.3V CERM 402
C3094 1UF 10% 6.3V CERM 402
C3095 1UF 10% 6.3V CERM 402
C3096 1UF 10% 6.3V CERM 402
C3097 1UF 10% 6.3V CERM 402
C3098 1UF 10% 6.3V CERM 402
C3099 1UF 10% 6.3V CERM 402
C3000 1UF 10% 6.3V CERM 402
C3001 1UF 10% 6.3V CERM 402
C3002 1UF 10% 6.3V CERM 402

16 6 =PP1V8R1V5_S0_MCP_MEM
30 25 4771 mA (A01, DDR3)

C30A0 1UF 10% 6.3V CERM 402
C30A1 1UF 10% 6.3V CERM 402
C30A2 1UF 10% 6.3V CERM 402
C30A3 1UF 10% 6.3V CERM 402
C30A4 1UF 10% 6.3V CERM 402
C30A5 1UF 10% 6.3V CERM 402

CAPS TO COUPLE PP5V_S3 UNDER DIMM CONNECTORS

75 30 6 =PP5V_S3_DDRREG

C30B0 1UF 10% 6.3V CERM 402
C30B1 1UF 10% 6.3V CERM 402
C30B2 1UF 10% 6.3V CERM 402
C30B3 1UF 10% 6.3V CERM 402
C30B4 1UF 10% 6.3V CERM 402
C30B5 1UF 10% 6.3V CERM 402
C30B6 1UF 10% 6.3V CERM 402
C30B7 1UF 10% 6.3V CERM 402
C30B8 1UF 10% 6.3V CERM 402
C30B9 1UF 10% 6.3V CERM 402
C30BA 1UF 10% 6.3V CERM 402
C30BB 1UF 10% 6.3V CERM 402
C30BC 1UF 10% 6.3V CERM 402
C30BD 1UF 10% 6.3V CERM 402
C30BE 1UF 10% 6.3V CERM 402
C30BF 1UF 10% 6.3V CERM 402
C30D0 1UF 10% 6.3V CERM 402
C30D1 1UF 10% 6.3V CERM 402
C30D2 1UF 10% 6.3V CERM 402
C30D3 1UF 10% 6.3V CERM 402

75 30 6 =PP5V_S3_DDRREG

C30C0 1UF 10% 6.3V CERM 402
C30C1 1UF 10% 6.3V CERM 402
C30C2 1UF 10% 6.3V CERM 402
C30C3 1UF 10% 6.3V CERM 402
C30C4 1UF 10% 6.3V CERM 402
C30C5 1UF 10% 6.3V CERM 402
C30C6 1UF 10% 6.3V CERM 402
C30C7 1UF 10% 6.3V CERM 402
C30C8 1UF 10% 6.3V CERM 402
C30C9 1UF 10% 6.3V CERM 402
C30CA 1UF 10% 6.3V CERM 402
C30CB 1UF 10% 6.3V CERM 402
C30CC 1UF 10% 6.3V CERM 402
C30CD 1UF 10% 6.3V CERM 402
C30CE 1UF 10% 6.3V CERM 402
C30CF 1UF 10% 6.3V CERM 402
C30E0 1UF 10% 6.3V CERM 402
C30E1 1UF 10% 6.3V CERM 402
C30E2 1UF 10% 6.3V CERM 402
C30E3 1UF 10% 6.3V CERM 402

DECOUPLING CAPS FOR DIMM ON CHANNEL A - AT CONNECTOR

108 31 6 =PP1V5_S3_MEM_A

C3050 10UF 20% 6.3V X5R 603
C3051 10UF 20% 6.3V X5R 603
C3052 1UF 10% 6.3V CERM 402
C3053 1UF 10% 6.3V CERM 402
C3054 1UF 10% 6.3V CERM 402
C3055 1UF 10% 6.3V CERM 402
C3056 1UF 10% 6.3V CERM 402
C3057 1UF 10% 6.3V CERM 402
C3058 1UF 10% 6.3V CERM 402
C3059 1UF 10% 6.3V CERM 402
C3060 1UF 10% 6.3V CERM 402
C3061 1UF 10% 6.3V CERM 402
C3062 1UF 10% 6.3V CERM 402
C3063 1UF 10% 6.3V CERM 402
C3064 1UF 10% 6.3V CERM 402
C3065 1UF 10% 6.3V CERM 402

DECOUPLING CAPS FOR DIMM ON CHANNEL B - AT CONNECTOR

108 32 6 =PP1V5_S3_MEM_B

C3070 10UF 20% 6.3V X5R 603
C3071 10UF 20% 6.3V X5R 603
C3072 1UF 10% 6.3V CERM 402
C3073 1UF 10% 6.3V CERM 402
C3074 1UF 10% 6.3V CERM 402
C3075 1UF 10% 6.3V CERM 402
C3076 1UF 10% 6.3V CERM 402
C3077 1UF 10% 6.3V CERM 402
C3078 1UF 10% 6.3V CERM 402
C3079 1UF 10% 6.3V CERM 402
C3080 1UF 10% 6.3V CERM 402
C3081 1UF 10% 6.3V CERM 402
C3082 1UF 10% 6.3V CERM 402
C3083 1UF 10% 6.3V CERM 402
C3084 1UF 10% 6.3V CERM 402
C3085 1UF 10% 6.3V CERM 402

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PAGE TITLE

MEMORY CAPS

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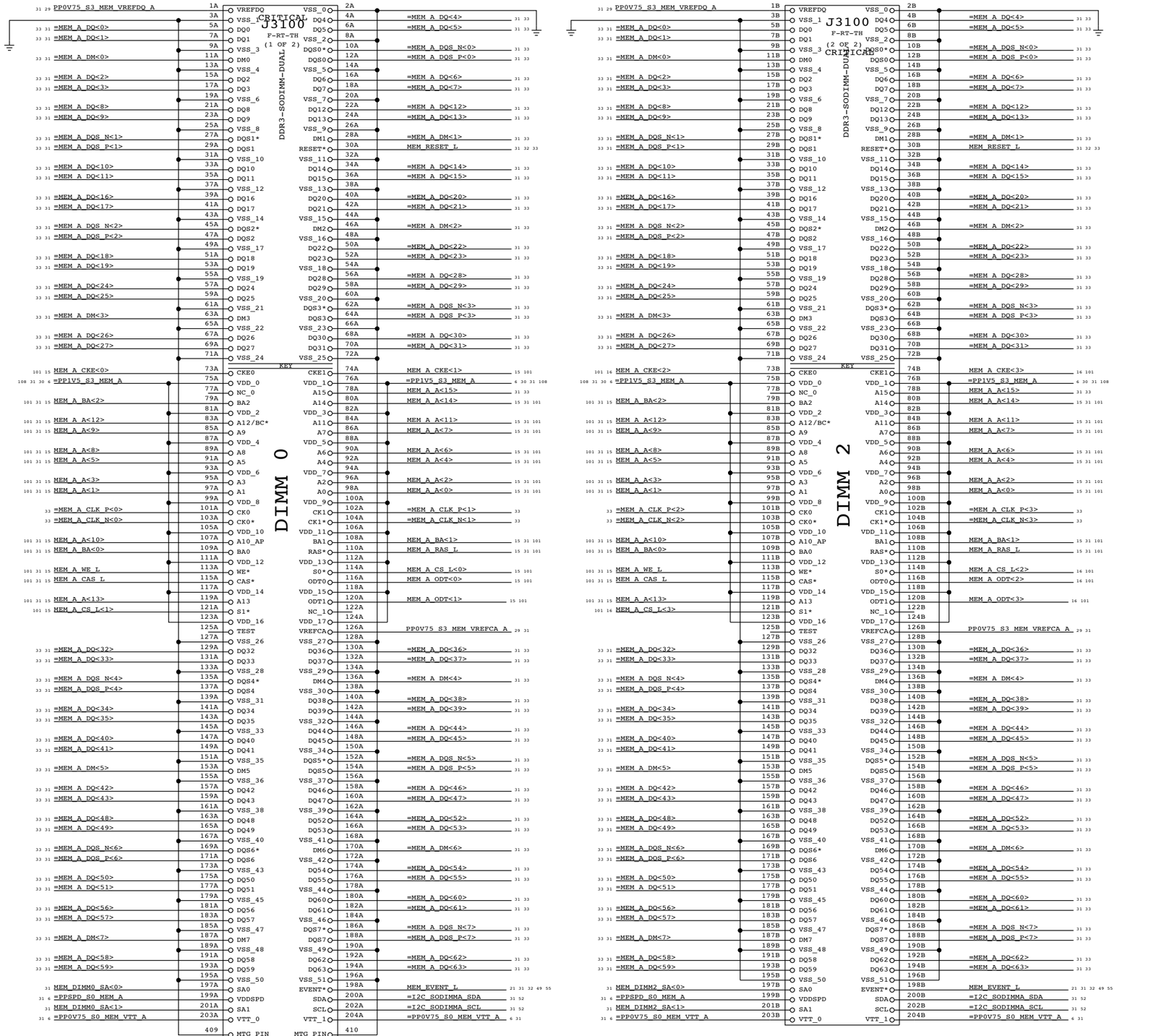

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL - ALL DQ, DQS, DM SIGNALS; TO FACILITATE BITSWAPS WITH ALIASES
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE: DDR3 SO-DIMMs 0 & 2

Apple Inc.

DRAWING NUMBER: 051-7845 SIZE: D

REVISION: A.0.0

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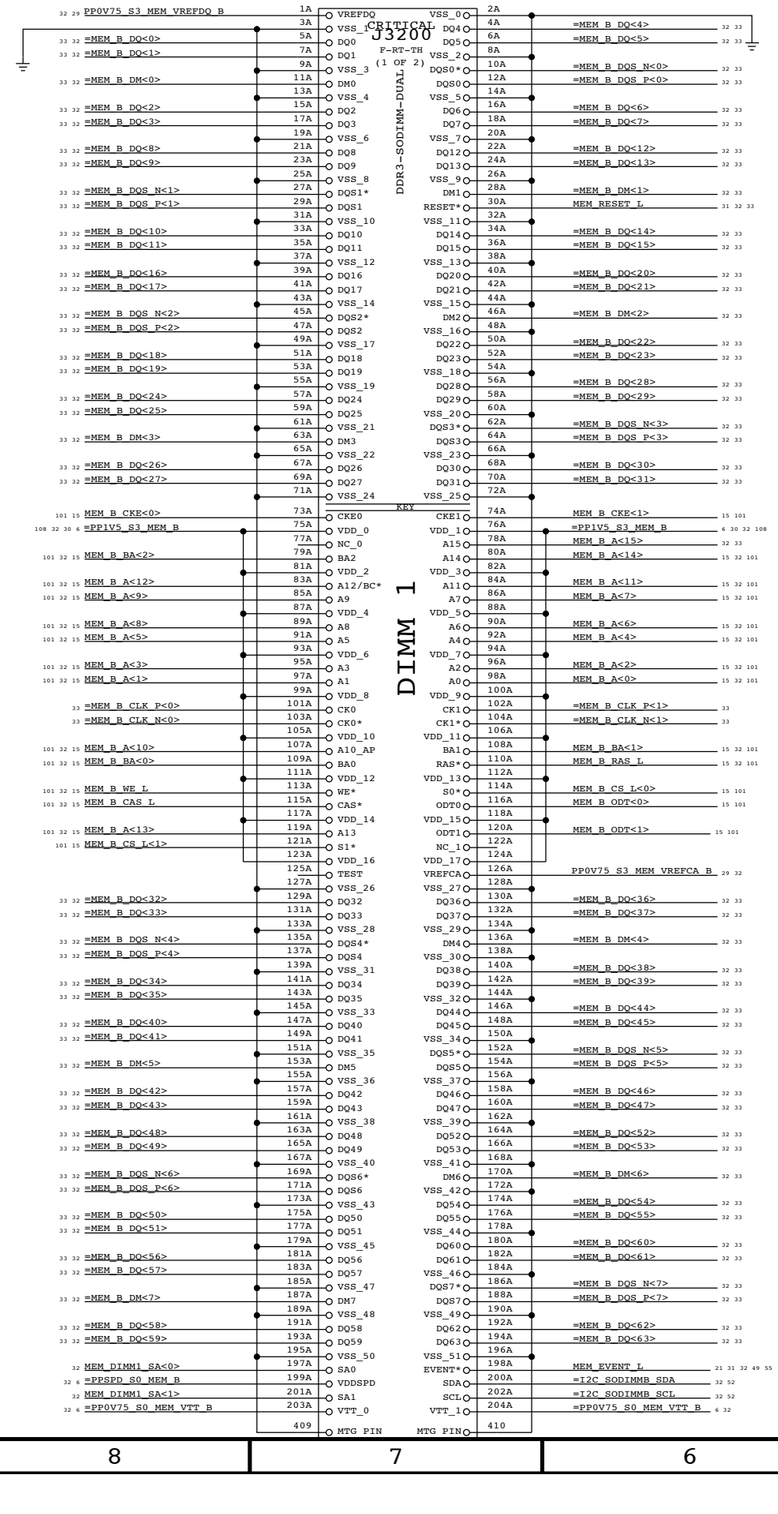

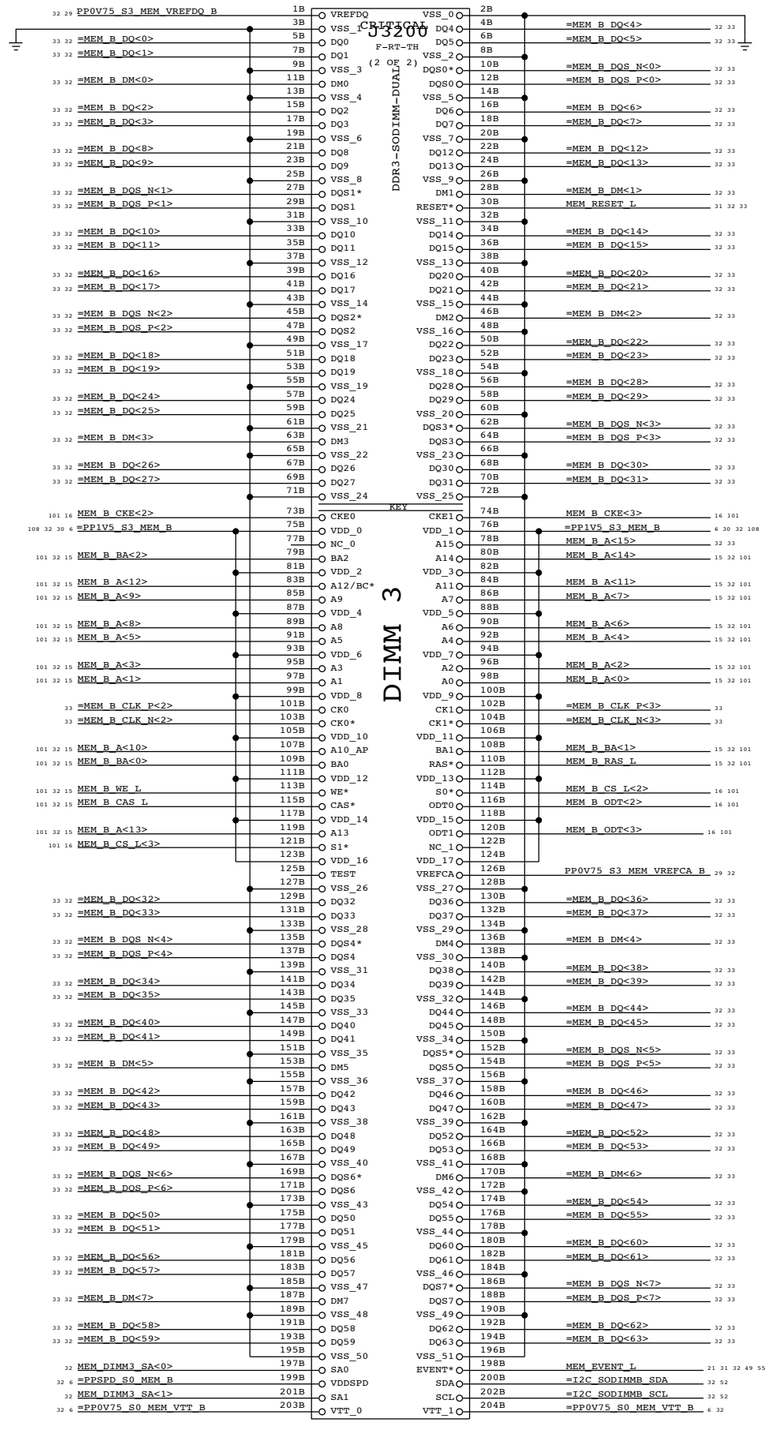

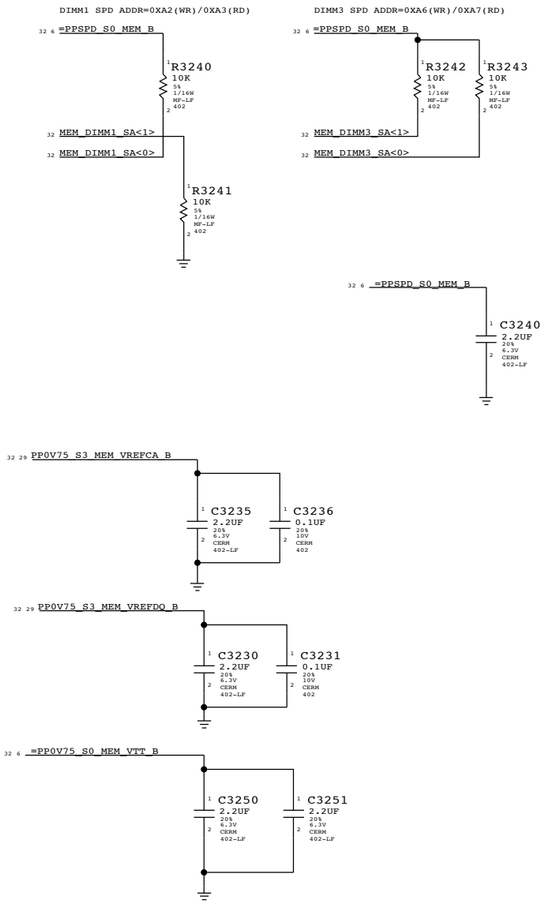

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL — ALL DQ, DQS, DM SIGNALS; TO FACILITATE BITSWAPS WITH ALIASES
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE
DDR3 SO-DIMM CONNECTOR B

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MCP CHANNEL A DQS 0 -> DIMM A DQS 0

MEM_A_DQS_N<0>	MAKE_BASE=TRUE	=MEM_A_DQS_N<0>	31
MEM_A_DQS_P<0>	MAKE_BASE=TRUE	=MEM_A_DQS_P<0>	31
MEM_A_DM<0>	MAKE_BASE=TRUE	=MEM_A_DM<0>	31
MEM_A_DQ<7>	MAKE_BASE=TRUE	=MEM_A_DQ<7>	31
MEM_A_DQ<6>	MAKE_BASE=TRUE	=MEM_A_DQ<6>	31
MEM_A_DQ<5>	MAKE_BASE=TRUE	=MEM_A_DQ<4>	31
MEM_A_DQ<4>	MAKE_BASE=TRUE	=MEM_A_DQ<5>	31
MEM_A_DQ<3>	MAKE_BASE=TRUE	=MEM_A_DQ<3>	31
MEM_A_DQ<2>	MAKE_BASE=TRUE	=MEM_A_DQ<2>	31
MEM_A_DQ<1>	MAKE_BASE=TRUE	=MEM_A_DQ<0>	31
MEM_A_DQ<0>	MAKE_BASE=TRUE	=MEM_A_DQ<1>	31

MCP CHANNEL A DQS 1 -> DIMM A DQS 1

MEM_A_DQS_N<1>	MAKE_BASE=TRUE	=MEM_A_DQS_N<1>	31
MEM_A_DQS_P<1>	MAKE_BASE=TRUE	=MEM_A_DQS_P<1>	31
MEM_A_DM<1>	MAKE_BASE=TRUE	=MEM_A_DM<1>	31
MEM_A_DQ<15>	MAKE_BASE=TRUE	=MEM_A_DQ<15>	31
MEM_A_DQ<14>	MAKE_BASE=TRUE	=MEM_A_DQ<14>	31
MEM_A_DQ<13>	MAKE_BASE=TRUE	=MEM_A_DQ<13>	31
MEM_A_DQ<12>	MAKE_BASE=TRUE	=MEM_A_DQ<12>	31
MEM_A_DQ<11>	MAKE_BASE=TRUE	=MEM_A_DQ<11>	31
MEM_A_DQ<10>	MAKE_BASE=TRUE	=MEM_A_DQ<10>	31
MEM_A_DQ<9>	MAKE_BASE=TRUE	=MEM_A_DQ<8>	31
MEM_A_DQ<8>	MAKE_BASE=TRUE	=MEM_A_DQ<9>	31

MCP CHANNEL A DQS 2 -> DIMM A DQS 2

MEM_A_DQS_N<2>	MAKE_BASE=TRUE	=MEM_A_DQS_N<2>	31
MEM_A_DQS_P<2>	MAKE_BASE=TRUE	=MEM_A_DQS_P<2>	31
MEM_A_DM<2>	MAKE_BASE=TRUE	=MEM_A_DM<2>	31
MEM_A_DQ<23>	MAKE_BASE=TRUE	=MEM_A_DQ<23>	31
MEM_A_DQ<22>	MAKE_BASE=TRUE	=MEM_A_DQ<22>	31
MEM_A_DQ<21>	MAKE_BASE=TRUE	=MEM_A_DQ<16>	31
MEM_A_DQ<20>	MAKE_BASE=TRUE	=MEM_A_DQ<20>	31
MEM_A_DQ<19>	MAKE_BASE=TRUE	=MEM_A_DQ<19>	31
MEM_A_DQ<18>	MAKE_BASE=TRUE	=MEM_A_DQ<17>	31
MEM_A_DQ<17>	MAKE_BASE=TRUE	=MEM_A_DQ<18>	31
MEM_A_DQ<16>	MAKE_BASE=TRUE	=MEM_A_DQ<21>	31

MCP CHANNEL A DQS 3 -> DIMM A DQS 3

MEM_A_DQS_N<3>	MAKE_BASE=TRUE	=MEM_A_DQS_N<3>	31
MEM_A_DQS_P<3>	MAKE_BASE=TRUE	=MEM_A_DQS_P<3>	31
MEM_A_DM<3>	MAKE_BASE=TRUE	=MEM_A_DM<3>	31
MEM_A_DQ<31>	MAKE_BASE=TRUE	=MEM_A_DQ<31>	31
MEM_A_DQ<30>	MAKE_BASE=TRUE	=MEM_A_DQ<30>	31
MEM_A_DQ<29>	MAKE_BASE=TRUE	=MEM_A_DQ<29>	31
MEM_A_DQ<28>	MAKE_BASE=TRUE	=MEM_A_DQ<28>	31
MEM_A_DQ<27>	MAKE_BASE=TRUE	=MEM_A_DQ<27>	31
MEM_A_DQ<26>	MAKE_BASE=TRUE	=MEM_A_DQ<26>	31
MEM_A_DQ<25>	MAKE_BASE=TRUE	=MEM_A_DQ<25>	31
MEM_A_DQ<24>	MAKE_BASE=TRUE	=MEM_A_DQ<24>	31

MCP CHANNEL A DQS 4 -> DIMM A DQS 4

MEM_A_DQS_N<4>	MAKE_BASE=TRUE	=MEM_A_DQS_N<4>	31
MEM_A_DQS_P<4>	MAKE_BASE=TRUE	=MEM_A_DQS_P<4>	31
MEM_A_DM<4>	MAKE_BASE=TRUE	=MEM_A_DM<4>	31
MEM_A_DQ<39>	MAKE_BASE=TRUE	=MEM_A_DQ<39>	31
MEM_A_DQ<38>	MAKE_BASE=TRUE	=MEM_A_DQ<38>	31
MEM_A_DQ<37>	MAKE_BASE=TRUE	=MEM_A_DQ<37>	31
MEM_A_DQ<36>	MAKE_BASE=TRUE	=MEM_A_DQ<36>	31
MEM_A_DQ<35>	MAKE_BASE=TRUE	=MEM_A_DQ<35>	31
MEM_A_DQ<34>	MAKE_BASE=TRUE	=MEM_A_DQ<34>	31
MEM_A_DQ<33>	MAKE_BASE=TRUE	=MEM_A_DQ<33>	31
MEM_A_DQ<32>	MAKE_BASE=TRUE	=MEM_A_DQ<32>	31

MCP CHANNEL A DQS 5 -> DIMM A DQS 5

MEM_A_DQS_N<5>	MAKE_BASE=TRUE	=MEM_A_DQS_N<5>	31
MEM_A_DQS_P<5>	MAKE_BASE=TRUE	=MEM_A_DQS_P<5>	31
MEM_A_DM<5>	MAKE_BASE=TRUE	=MEM_A_DM<5>	31
MEM_A_DQ<47>	MAKE_BASE=TRUE	=MEM_A_DQ<47>	31
MEM_A_DQ<46>	MAKE_BASE=TRUE	=MEM_A_DQ<46>	31
MEM_A_DQ<45>	MAKE_BASE=TRUE	=MEM_A_DQ<45>	31
MEM_A_DQ<44>	MAKE_BASE=TRUE	=MEM_A_DQ<44>	31
MEM_A_DQ<43>	MAKE_BASE=TRUE	=MEM_A_DQ<43>	31
MEM_A_DQ<42>	MAKE_BASE=TRUE	=MEM_A_DQ<42>	31
MEM_A_DQ<41>	MAKE_BASE=TRUE	=MEM_A_DQ<41>	31
MEM_A_DQ<40>	MAKE_BASE=TRUE	=MEM_A_DQ<40>	31

MCP CHANNEL A DQS 6 -> DIMM A DQS 6

MEM_A_DQS_N<6>	MAKE_BASE=TRUE	=MEM_A_DQS_N<6>	31
MEM_A_DQS_P<6>	MAKE_BASE=TRUE	=MEM_A_DQS_P<6>	31
MEM_A_DM<6>	MAKE_BASE=TRUE	=MEM_A_DM<6>	31
MEM_A_DQ<55>	MAKE_BASE=TRUE	=MEM_A_DQ<55>	31
MEM_A_DQ<54>	MAKE_BASE=TRUE	=MEM_A_DQ<54>	31
MEM_A_DQ<53>	MAKE_BASE=TRUE	=MEM_A_DQ<53>	31
MEM_A_DQ<52>	MAKE_BASE=TRUE	=MEM_A_DQ<52>	31
MEM_A_DQ<51>	MAKE_BASE=TRUE	=MEM_A_DQ<51>	31
MEM_A_DQ<50>	MAKE_BASE=TRUE	=MEM_A_DQ<50>	31
MEM_A_DQ<49>	MAKE_BASE=TRUE	=MEM_A_DQ<49>	31
MEM_A_DQ<48>	MAKE_BASE=TRUE	=MEM_A_DQ<48>	31

MCP CHANNEL A DQS 7 -> DIMM A DQS 7

MEM_A_DQS_N<7>	MAKE_BASE=TRUE	=MEM_A_DQS_N<7>	31
MEM_A_DQS_P<7>	MAKE_BASE=TRUE	=MEM_A_DQS_P<7>	31
MEM_A_DM<7>	MAKE_BASE=TRUE	=MEM_A_DM<7>	31
MEM_A_DQ<63>	MAKE_BASE=TRUE	=MEM_A_DQ<63>	31
MEM_A_DQ<62>	MAKE_BASE=TRUE	=MEM_A_DQ<62>	31
MEM_A_DQ<61>	MAKE_BASE=TRUE	=MEM_A_DQ<57>	31
MEM_A_DQ<60>	MAKE_BASE=TRUE	=MEM_A_DQ<56>	31
MEM_A_DQ<59>	MAKE_BASE=TRUE	=MEM_A_DQ<59>	31
MEM_A_DQ<58>	MAKE_BASE=TRUE	=MEM_A_DQ<58>	31
MEM_A_DQ<57>	MAKE_BASE=TRUE	=MEM_A_DQ<61>	31
MEM_A_DQ<56>	MAKE_BASE=TRUE	=MEM_A_DQ<60>	31

MCP CHANNEL B DQS 0 -> DIMM B DQS 0

MEM_B_DQS_N<0>	MAKE_BASE=TRUE	=MEM_B_DQS_N<0>	32
MEM_B_DQS_P<0>	MAKE_BASE=TRUE	=MEM_B_DQS_P<0>	32
MEM_B_DM<0>	MAKE_BASE=TRUE	=MEM_B_DM<0>	32
MEM_B_DQ<7>	MAKE_BASE=TRUE	=MEM_B_DQ<7>	32
MEM_B_DQ<6>	MAKE_BASE=TRUE	=MEM_B_DQ<6>	32
MEM_B_DQ<5>	MAKE_BASE=TRUE	=MEM_B_DQ<1>	32
MEM_B_DQ<4>	MAKE_BASE=TRUE	=MEM_B_DQ<0>	32
MEM_B_DQ<3>	MAKE_BASE=TRUE	=MEM_B_DQ<3>	32
MEM_B_DQ<2>	MAKE_BASE=TRUE	=MEM_B_DQ<2>	32
MEM_B_DQ<1>	MAKE_BASE=TRUE	=MEM_B_DQ<5>	32
MEM_B_DQ<0>	MAKE_BASE=TRUE	=MEM_B_DQ<4>	32

MCP CHANNEL B DQS 1 -> DIMM B DQS 1

MEM_B_DQS_N<1>	MAKE_BASE=TRUE	=MEM_B_DQS_N<1>	32
MEM_B_DQS_P<1>	MAKE_BASE=TRUE	=MEM_B_DQS_P<1>	32
MEM_B_DM<1>	MAKE_BASE=TRUE	=MEM_B_DM<1>	32
MEM_B_DQ<15>	MAKE_BASE=TRUE	=MEM_B_DQ<15>	32
MEM_B_DQ<14>	MAKE_BASE=TRUE	=MEM_B_DQ<14>	32
MEM_B_DQ<13>	MAKE_BASE=TRUE	=MEM_B_DQ<13>	32
MEM_B_DQ<12>	MAKE_BASE=TRUE	=MEM_B_DQ<12>	32
MEM_B_DQ<11>	MAKE_BASE=TRUE	=MEM_B_DQ<11>	32
MEM_B_DQ<10>	MAKE_BASE=TRUE	=MEM_B_DQ<10>	32
MEM_B_DQ<9>	MAKE_BASE=TRUE	=MEM_B_DQ<9>	32
MEM_B_DQ<8>	MAKE_BASE=TRUE	=MEM_B_DQ<8>	32

MCP CHANNEL B DQS 2 -> DIMM B DQS 2

MEM_B_DQS_N<2>	MAKE_BASE=TRUE	=MEM_B_DQS_N<2>	32
MEM_B_DQS_P<2>	MAKE_BASE=TRUE	=MEM_B_DQS_P<2>	32
MEM_B_DM<2>	MAKE_BASE=TRUE	=MEM_B_DM<2>	32
MEM_B_DQ<23>	MAKE_BASE=TRUE	=MEM_B_DQ<23>	32
MEM_B_DQ<22>	MAKE_BASE=TRUE	=MEM_B_DQ<22>	32
MEM_B_DQ<21>	MAKE_BASE=TRUE	=MEM_B_DQ<21>	32
MEM_B_DQ<20>	MAKE_BASE=TRUE	=MEM_B_DQ<20>	32
MEM_B_DQ<19>	MAKE_BASE=TRUE	=MEM_B_DQ<19>	32
MEM_B_DQ<18>	MAKE_BASE=TRUE	=MEM_B_DQ<18>	32
MEM_B_DQ<17>	MAKE_BASE=TRUE	=MEM_B_DQ<17>	32
MEM_B_DQ<16>	MAKE_BASE=TRUE	=MEM_B_DQ<16>	32

MCP CHANNEL B DQS 3 -> DIMM B DQS 3

MEM_B_DQS_N<3>	MAKE_BASE=TRUE	=MEM_B_DQS_N<3>	32
MEM_B_DQS_P<3>	MAKE_BASE=TRUE	=MEM_B_DQS_P<3>	32
MEM_B_DM<3>	MAKE_BASE=TRUE	=MEM_B_DM<3>	32
MEM_B_DQ<31>	MAKE_BASE=TRUE	=MEM_B_DQ<31>	32
MEM_B_DQ<30>	MAKE_BASE=TRUE	=MEM_B_DQ<30>	32
MEM_B_DQ<29>	MAKE_BASE=TRUE	=MEM_B_DQ<29>	32
MEM_B_DQ<28>	MAKE_BASE=TRUE	=MEM_B_DQ<28>	32
MEM_B_DQ<27>	MAKE_BASE=TRUE	=MEM_B_DQ<27>	32
MEM_B_DQ<26>	MAKE_BASE=TRUE	=MEM_B_DQ<26>	32
MEM_B_DQ<25>	MAKE_BASE=TRUE	=MEM_B_DQ<25>	32
MEM_B_DQ<24>	MAKE_BASE=TRUE	=MEM_B_DQ<24>	32

MCP CHANNEL B DQS 4 -> DIMM B DQS 4

MEM_B_DQS_N<4>	MAKE_BASE=TRUE	=MEM_B_DQS_N<4>	32
MEM_B_DQS_P<4>	MAKE_BASE=TRUE	=MEM_B_DQS_P<4>	32
MEM_B_DM<4>	MAKE_BASE=TRUE	=MEM_B_DM<4>	32
MEM_B_DQ<39>	MAKE_BASE=TRUE	=MEM_B_DQ<39>	32
MEM_B_DQ<38>	MAKE_BASE=TRUE	=MEM_B_DQ<38>	32
MEM_B_DQ<37>	MAKE_BASE=TRUE	=MEM_B_DQ<37>	32
MEM_B_DQ<36>	MAKE_BASE=TRUE	=MEM_B_DQ<36>	32
MEM_B_DQ<35>	MAKE_BASE=TRUE	=MEM_B_DQ<35>	32
MEM_B_DQ<34>	MAKE_BASE=TRUE	=MEM_B_DQ<34>	32
MEM_B_DQ<33>	MAKE_BASE=TRUE	=MEM_B_DQ<33>	32
MEM_B_DQ<32>	MAKE_BASE=TRUE	=MEM_B_DQ<32>	32

MCP CHANNEL B DQS 5 -> DIMM B DQS 5

MEM_B_DQS_N<5>	MAKE_BASE=TRUE	=MEM_B_DQS_N<5>	32
MEM_B_DQS_P<5>	MAKE_BASE=TRUE	=MEM_B_DQS_P<5>	32
MEM_B_DM<5>	MAKE_BASE=TRUE	=MEM_B_DM<5>	32
MEM_B_DQ<47>	MAKE_BASE=TRUE	=MEM_B_DQ<47>	32
MEM_B_DQ<46>	MAKE_BASE=TRUE	=MEM_B_DQ<46>	32
MEM_B_DQ<45>	MAKE_BASE=TRUE	=MEM_B_DQ<45>	32
MEM_B_DQ<44>	MAKE_BASE=TRUE	=MEM_B_DQ<44>	32
MEM_B_DQ<43>	MAKE_BASE=TRUE	=MEM_B_DQ<43>	32
MEM_B_DQ<42>	MAKE_BASE=TRUE	=MEM_B_DQ<42>	32
MEM_B_DQ<41>	MAKE_BASE=TRUE	=MEM_B_DQ<41>	32
MEM_B_DQ<40>	MAKE_BASE=TRUE	=MEM_B_DQ<40>	32

MCP CHANNEL B DQS 6 -> DIMM B DQS 6

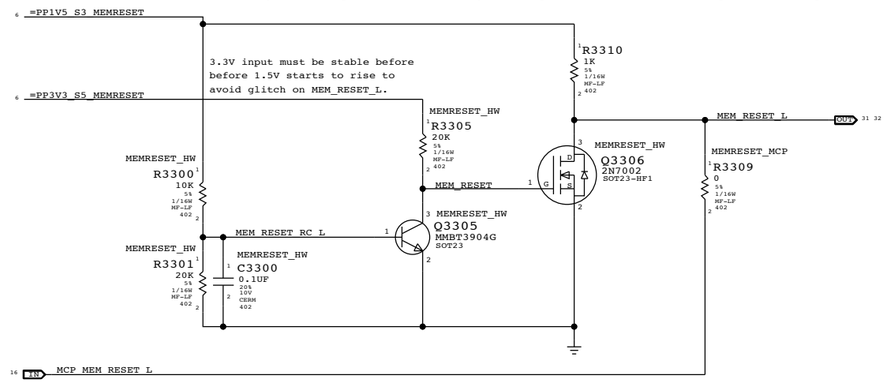
MEM_B_DQS_N<6>	MAKE_BASE=TRUE	=MEM_B_DQS_N<6>	32
MEM_B_DQS_P<6>	MAKE_BASE=TRUE	=MEM_B_DQS_P<6>	32
MEM_B_DM<6>	MAKE_BASE=TRUE	=MEM_B_DM<6>	32
MEM_B_DQ<55>	MAKE_BASE=TRUE	=MEM_B_DQ<55>	32
MEM_B_DQ<54>	MAKE_BASE=TRUE	=MEM_B_DQ<54>	32
MEM_B_DQ<53>	MAKE_BASE=TRUE	=MEM_B_DQ<53>	32
MEM_B_DQ<52>	MAKE_BASE=TRUE	=MEM_B_DQ<52>	32
MEM_B_DQ<51>	MAKE_BASE=TRUE	=MEM_B_DQ<51>	32
MEM_B_DQ<50>	MAKE_BASE=TRUE	=MEM_B_DQ<50>	32
MEM_B_DQ<49>	MAKE_BASE=TRUE	=MEM_B_DQ<49>	32
MEM_B_DQ<48>	MAKE_BASE=TRUE	=MEM_B_DQ<48>	32

MCP CHANNEL B DQS 7 -> DIMM B DQS 7

MEM_B_DQS_N<7>	MAKE_BASE=TRUE	=MEM_B_DQS_N<7>	32
MEM_B_DQS_P<7>	MAKE_BASE=TRUE	=MEM_B_DQS_P<7>	32
MEM_B_DM<7>	MAKE_BASE=TRUE	=MEM_B_DM<7>	32
MEM_B_DQ<63>	MAKE_BASE=TRUE	=MEM_B_DQ<63>	32
MEM_B_DQ<62>	MAKE_BASE=TRUE	=MEM_B_DQ<62>	32
MEM_B_DQ<61>	MAKE_BASE=TRUE	=MEM_B_DQ<61>	32
MEM_B_DQ<60>	MAKE_BASE=TRUE	=MEM_B_DQ<60>	32
MEM_B_DQ<59>	MAKE_BASE=TRUE	=MEM_B_DQ<59>	32
MEM_B_DQ<58>	MAKE_BASE=TRUE	=MEM_B_DQ<58>	32
MEM_B_DQ<57>	MAKE_BASE=TRUE	=MEM_B_DQ<57>	32
MEM_B_DQ<56>	MAKE_BASE=TRUE	=MEM_B_DQ<56>	32

DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.



MCP MEMORY CLOCK ALIASES

MEM_A_CLK_P<0>	MAKE_BASE=TRUE	=MEM_A_CLK_P<0>	31
MEM_A_CLK_N<0>	MAKE_BASE=TRUE	=MEM_A_CLK_N<0>	31
MEM_A_CLK_P<1>	MAKE_BASE=TRUE	=MEM_A_CLK_P<1>	31
MEM_A_CLK_N<1>	MAKE_BASE=TRUE	=MEM_A_CLK_N<1>	31
MEM_A_CLK_P<3>	MAKE_BASE=TRUE	=MEM_A_CLK_P<2>	31
MEM_A_CLK_N<3>	MAKE_BASE=TRUE	=MEM_A_CLK_N<2>	31
MEM_A_CLK_P<4>	MAKE_BASE=TRUE	=MEM_A_CLK_P<3>	31
MEM_A_CLK_N<4>	MAKE_BASE=TRUE	=MEM_A_CLK_N<3>	31

MEM_B_CLK_P<0>	MAKE_BASE=TRUE	=MEM_B_CLK_P<0>	32
MEM_B_CLK_N<0>	MAKE_BASE=TRUE	=MEM_B_CLK_N<0>	32
MEM_B_CLK_P<1>	MAKE_BASE=TRUE	=MEM_B_CLK_P<1>	32
MEM_B_CLK_N<1>	MAKE_BASE=TRUE	=MEM_B_CLK_N<1>	32
MEM_B_CLK_P<3>	MAKE_BASE=TRUE	=MEM_B_CLK_P<2>	32
MEM_B_CLK_N<3>	MAKE_BASE=TRUE	=MEM_B_CLK_N<2>	32
MEM_B_CLK_P<4>	MAKE_BASE=TRUE	=MEM_B_CLK_P<3>	32
MEM_B_CLK_N<4>	MAKE_BASE=TRUE	=MEM_B_CLK_N<3>	32

MCP MEMORY TEST POINT ALIASES

TP_MEM_A_A<15>	MAKE_BASE=TRUE	MEM_A_A<15>	31
TP_MEM_B_A<15>	MAKE_BASE=TRUE	MEM_B_A<15>	32

SYNC MASTER=K51 SYNC DATE=10/13/2008

PAGE TITLE

DDR3 SUPPORT AND BITSWAPS

Apple Inc.

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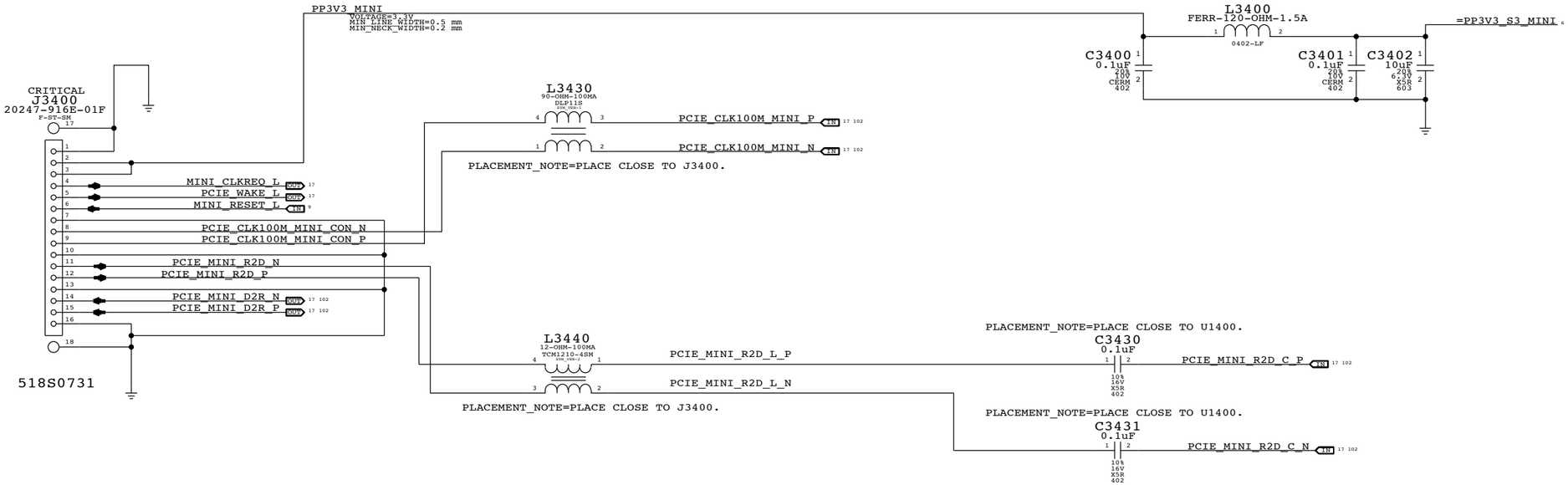

SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE

PCI-E Wireless Connector

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8 7 6 5 4 3 2 1

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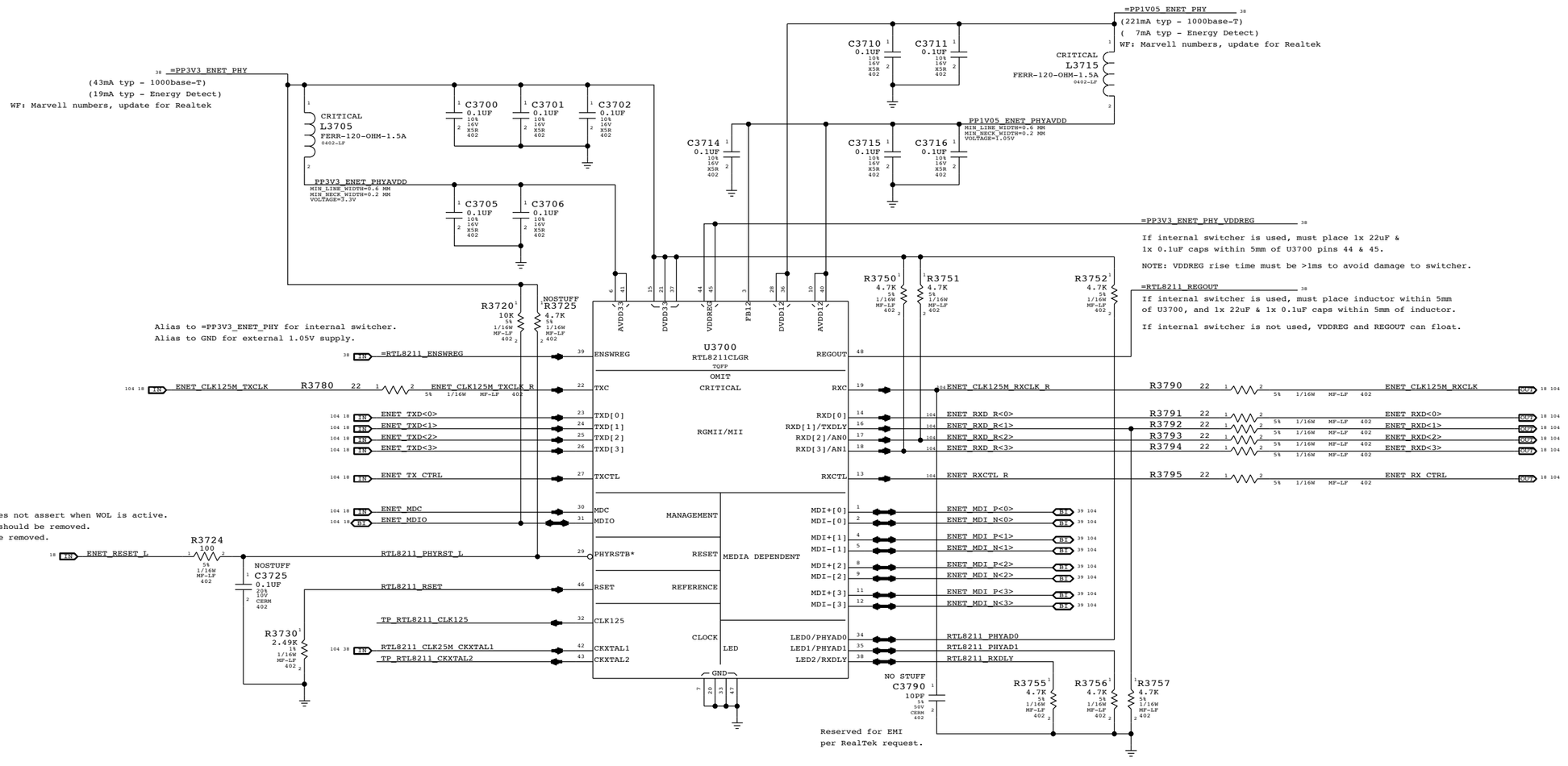

Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

SYNC MASTER=K51 SYNC DATE=12/08/2008

PAGE TITLE
Ethernet PHY (RTL8211CL)

Apple Inc.

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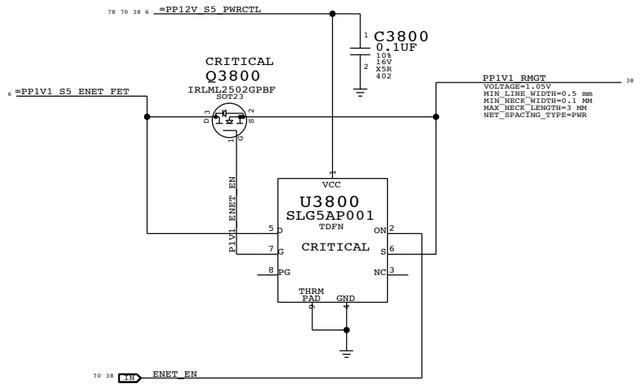
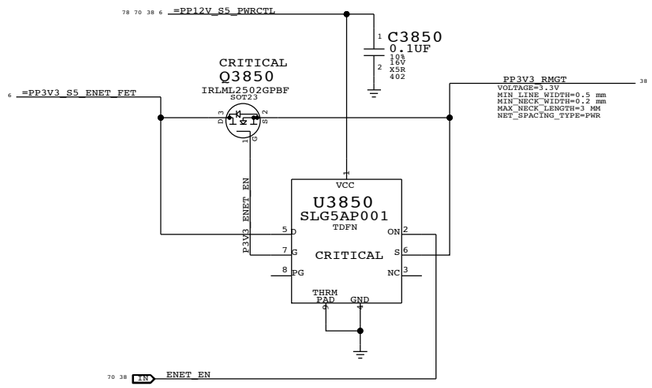
1.1V ENET FET



3.3V ENET FET



ENET ALIASES

38 PP1V1_RMGT
MAKE_BASE=TRUE
=PP1V05_ENET_MCP_RMGT 18 25
=PP1V05_ENET_MCP_PLL_MAC 25
=PP1V05_ENET_PHY 37

38 PP3V3_RMGT
MAKE_BASE=TRUE
=PP3V3_ENET_MCP_RMGT 18 25
=PP3V3_ENET_PHY 37

MAKE_BASE=TRUE
=RTL8211_ENSWREG 37

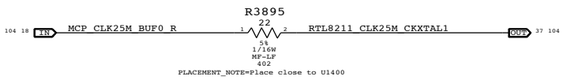
NOTE: NOT USING THE BUILT-IN 1.05V REGULATOR OF THE PHY

NC_RTL8211_REGOUT
MAKE_BASE=TRUE
NO_TEST=TRUE
=RTL8211_REGOUT 37

NC_PP3V3_ENET_PHY_VDDREG
MAKE_BASE=TRUE
NO_TEST=TRUE
=PP3V3_ENET_PHY_VDDREG 37

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



PLACEMENT_NOTE=Place close to U1400

SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE
Ethernet Support

Apple Inc.

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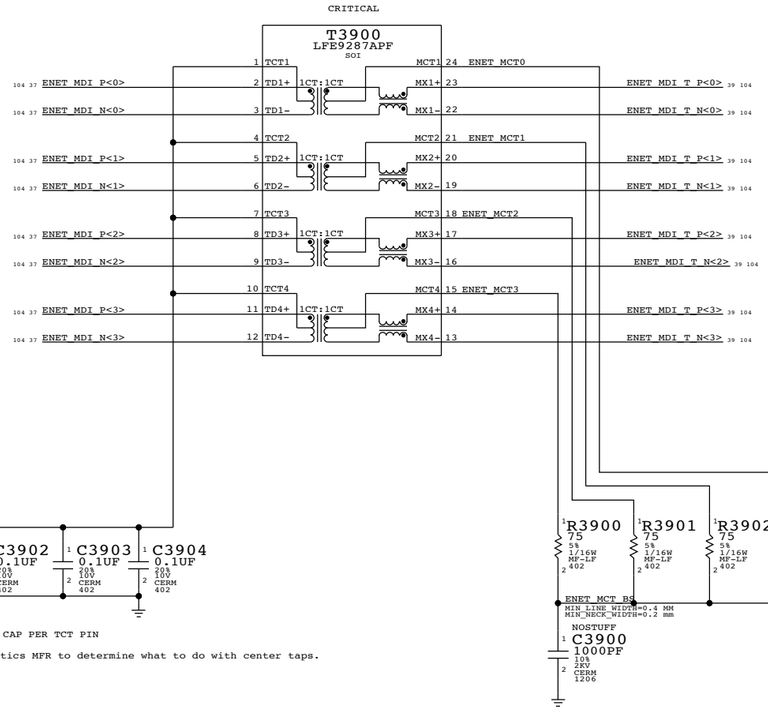
CRITICAL

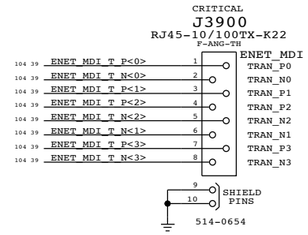


PLACE ONE CAP PER TCT PIN

NOTE: Check with PHY and Magnetics MFR to determine what to do with center taps.

NOTE: BOB SMITH TERMINATION FOR EMC.

CRITICAL



SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE

ETHERNET CONNECTOR

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8 7 6 5 4 3 2 1

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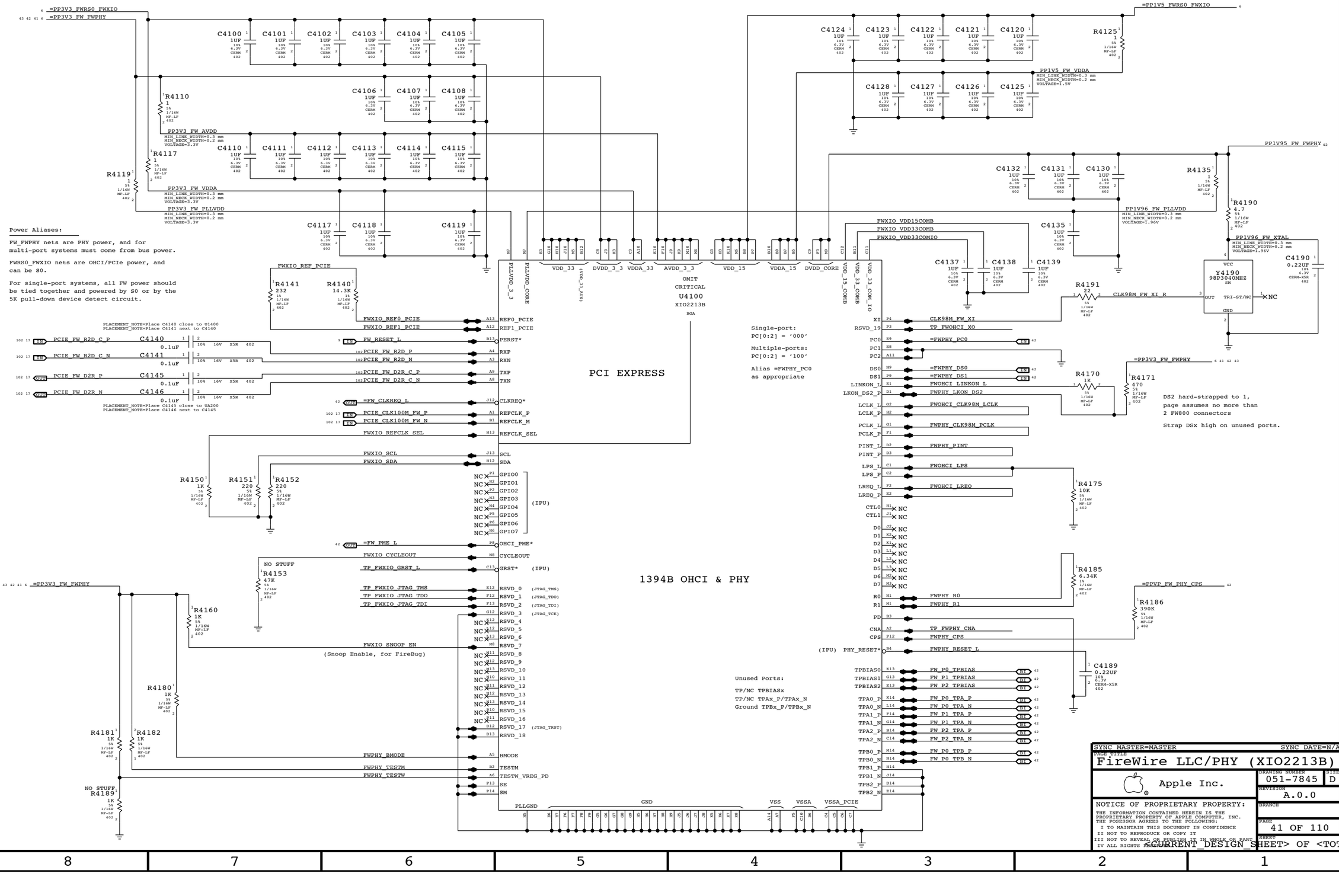
8 7 6 5 4 3 2 1


=PP3V3_FWRS0_FWXIO
=PP3V3_FW_FWPHY
C4100 1UF 10% 6.3V CERM 402
C4101 1UF 10% 6.3V CERM 402
C4102 1UF 10% 6.3V CERM 402
C4103 1UF 10% 6.3V CERM 402
C4104 1UF 10% 6.3V CERM 402
C4105 1UF 10% 6.3V CERM 402
C4106 1UF 10% 6.3V CERM 402
C4107 1UF 10% 6.3V CERM 402
C4108 1UF 10% 6.3V CERM 402
C4110 1UF 10% 6.3V CERM 402
C4111 1UF 10% 6.3V CERM 402
C4112 1UF 10% 6.3V CERM 402
C4113 1UF 10% 6.3V CERM 402
C4114 1UF 10% 6.3V CERM 402
C4115 1UF 10% 6.3V CERM 402
C4117 1UF 10% 6.3V CERM 402
C4118 1UF 10% 6.3V CERM 402
C4119 1UF 10% 6.3V CERM 402
R4110 1 5% 1/16W MF-LF 402
R4117 1 5% 1/16W MF-LF 402
R4119 1 5% 1/16W MF-LF 402
PP3V3_FW_AVDD
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
PP3V3_FW_VDDA
PP3V3_FW_PLLVDD
C4124 1UF 10% 6.3V CERM 402
C4123 1UF 10% 6.3V CERM 402
C4122 1UF 10% 6.3V CERM 402
C4121 1UF 10% 6.3V CERM 402
C4120 1UF 10% 6.3V CERM 402
C4128 1UF 10% 6.3V CERM 402
C4127 1UF 10% 6.3V CERM 402
C4126 1UF 10% 6.3V CERM 402
C4125 1UF 10% 6.3V CERM 402
R4125 1 5% 1/16W MF-LF 402
=PP1V5_FWRS0_FWXIO
PP1V5_FW_VDDA
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
C4132 1UF 10% 6.3V CERM 402
C4131 1UF 10% 6.3V CERM 402
C4130 1UF 10% 6.3V CERM 402
C4135 1UF 10% 6.3V CERM 402
R4135 1 5% 1/16W MF-LF 402
PP1V95_FW_FWPHY
PP1V96_FW_PLLVDD
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.96V
R4190 4.7 5% 1/16W MF-LF 402
PP1V96_FW_XTAL
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.96V
C4190 0.22UF 10% 6.3V CERM-X5R 402
Y4190 98P3040MHZ SM
VCC
OUT
TRI-ST/NC
GND
NC
R4191 22 5% 1/16W MF-LF 402
CLK98M_FW_XI_R
Power Aliases:
FW_FWPHY nets are PHY power, and for multi-port systems must come from bus power.
FWRS0_FWXIO nets are OHCI/PCIe power, and can be S0.
For single-port systems, all FW power should be tied together and powered by S0 or by the 5K pull-down device detect circuit.
FWXIO_REF_PCIE
R4141 232 1% 1/16W MF-LF 402
R4140 14.3K 1% 1/16W MF-LF 402
PLLVDD_3_3
PLLVDD_CORE
VDD_33
(VDD_33_AUX)
DVDD_3_3
VDDA_33
AVDD_3_3
VDD_15
VDDA_15
DVDD_CORE
VDD_15_COMB
VDD_33_COMB
VDD_33_COM_IO
FWXIO VDD15COMB
FWXIO VDD33COMB
FWXIO VDD33COMIO
OMIT
CRITICAL
U4100
XIO2213B
BGA
PCI EXPRESS
PLACEMENT_NOTE=Place C4140 close to U4100
PLACEMENT_NOTE=Place C4141 next to C4140
PCIE_FW_R2D_C_P C4140 0.1uF 10% 16V X5R 402
PCIE_FW_R2D_C_N C4141 0.1uF 10% 16V X5R 402
PCIE_FW_D2R_P C4145 0.1uF 10% 16V X5R 402
PCIE_FW_D2R_N C4146 0.1uF 10% 16V X5R 402
PLACEMENT_NOTE=Place C4145 close to UA200
PLACEMENT_NOTE=Place C4146 next to C4145
FW_RESET_L
FWXIO_REF0_PCIE
FWXIO_REF1_PCIE
REF0_PCIE
REF1_PCIE
PERST*
RXP
RXN
TXP
TXN
=FW_CLKREQ_L
CLKREQ*
PCIE_CLK100M_FW_P
PCIE_CLK100M_FW_N
REFCLK_P
REFCLK_M
FWXIO_REFCLK_SEL
REFCLK_SEL
FWXIO_SCL
FWXIO_SDA
SCL
SDA
R4150 1K 5% 1/16W MF-LF 402
R4151 220 5% 1/16W MF-LF 402
R4152 220 5% 1/16W MF-LF 402
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
(IPU)
=FW_PME_L
OHCI_PME*
FWXIO_CYCLEOUT
CYCLEOUT
NO STUFF
R4153 47K 5% 1/16W MF-LF 402
TP_FWXIO_GRST_L
GRST*
(IPU)
TP_FWXIO_JTAG_TMS
TP_FWXIO_JTAG_TDO
TP_FWXIO_JTAG_TDI
RSVD_0 (JTAG_TMS)
RSVD_1 (JTAG_TDO)
RSVD_2 (JTAG_TDI)
RSVD_3 (JTAG_TCK)
RSVD_4
RSVD_5
RSVD_6
RSVD_7
RSVD_8
RSVD_9
RSVD_10
RSVD_11
RSVD_12
RSVD_13
RSVD_14
RSVD_15
RSVD_16
RSVD_17 (JTAG_TRST)
RSVD_18
FWXIO_SNOOP_EN
(Snoop Enable, for FireBug)
R4160 1K 5% 1/16W MF-LF 402
R4180 1K 5% 1/16W MF-LF 402
R4181 1K 5% 1/16W MF-LF 402
R4182 1K 5% 1/16W MF-LF 402
NO STUFF
R4189 1K 5% 1/16W MF-LF 402
FWPHY_BMODE
FWPHY_TESTM
FWPHY_TESTW
BMODE
TESTM
TESTW_VREG_PD
SE
SM
1394B OHCI & PHY
Single-port:
PC[0:2] = '000'
Multiple-ports:
PC[0:2] = '100'
Alias =FWPHY_PC0 as appropriate
XI
RSVD_19
PC0
PC1
PC2
DS0
DS1
LINKON_L
LKON_DS2_P
LCLK_L
LCLK_P
PCLK_L
PCLK_P
PINT_L
PINT_P
LPS_L
LPS_P
LREQ_L
LREQ_P
CTL0
CTL1
D0
D1
D2
D3
D4
D5
D6
D7
R0
R1
PD
CNA
CPS
PHY_RESET*
CLK98M_FW_XI
TP_FWOHCI_XO
=FWPHY_PC0
=FWPHY_DS0
=FWPHY_DS1
FWOHCI_LINKON_L
FWPHY_LKON_DS2
FWOHCI_CLK98M_LCLK
FWPHY_CLK98M_PCLK
FWPHY_PINT
FWOHCI_LPS
FWOHCI_LREQ
NC
FWPHY_R0
FWPHY_R1
TP_FWPHY_CNA
FWPHY_CPS
FWPHY_RESET_L
=PP3V3_FW_FWPHY
R4170 1K 5% 1/16W MF-LF 402
R4171 470 5% 1/16W MF-LF 402
DS2 hard-strapped to 1, page assumes no more than 2 FW800 connectors
Strap DSx high on unused ports.
R4175 10K 5% 1/16W MF-LF 402
R4185 6.34K 1% 1/16W MF-LF 402
=PPVP_FW_PHY_CPS
R4186 390K 5% 1/16W MF-LF 402
C4189 0.22UF 10% 6.3V CERM-X5R 402
Unused Ports:
TP/NC TPBIASx
TP/NC TPAx_P/TPAx_N
Ground TPBx_P/TPBx_N
TPBIAS0
TPBIAS1
TPBIAS2
TPA0_P
TPA0_N
TPA1_P
TPA1_N
TPA2_P
TPA2_N
TPB0_P
TPB0_N
TPB1_P
TPB1_N
TPB2_P
TPB2_N
FW_P0_TPBIAS
FW_P1_TPBIAS
FW_P2_TPBIAS
FW_P0_TPA_P
FW_P0_TPA_N
FW_P1_TPA_P
FW_P1_TPA_N
FW_P2_TPA_P
FW_P2_TPA_N
FW_P0_TPB_P
FW_P0_TPB_N
PLLGND
GND
VSS
VSSA
VSSA_PCIE
SYNC MASTER=MASTER
SYNC DATE=N/A
PAGE TITLE
FireWire LLC/PHY (XIO2213B)
Apple Inc.
DRAWING NUMBER 051-7845
SIZE D
REVISION A.0.0
BRANCH
PAGE 41 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>
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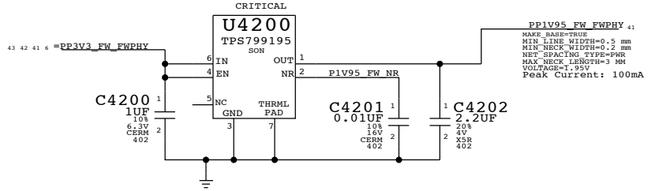
1394 PHY 1.95V SUPPLY



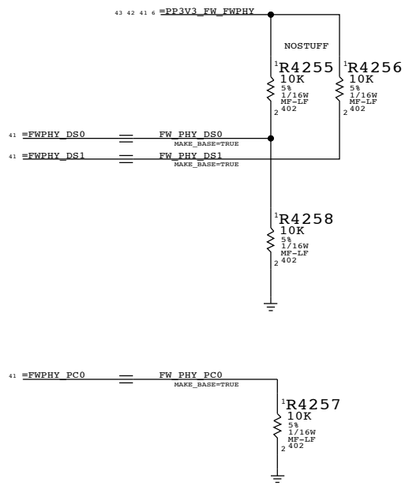
FireWire Aliases For Connectivity

41 =FW_CLKREQ_L = FW_CLKREQ_L 17 (MAKE_BASE=TRUE)

41 =FW_PME_L = FW_PME_L 19 (MAKE_BASE=TRUE)

41 =PPVP_FW_PHY_CPS = PPVP_FW_PHY_CPS 43 (MAKE_BASE=TRUE)

1394 PHY STRAPPING OPTIONS

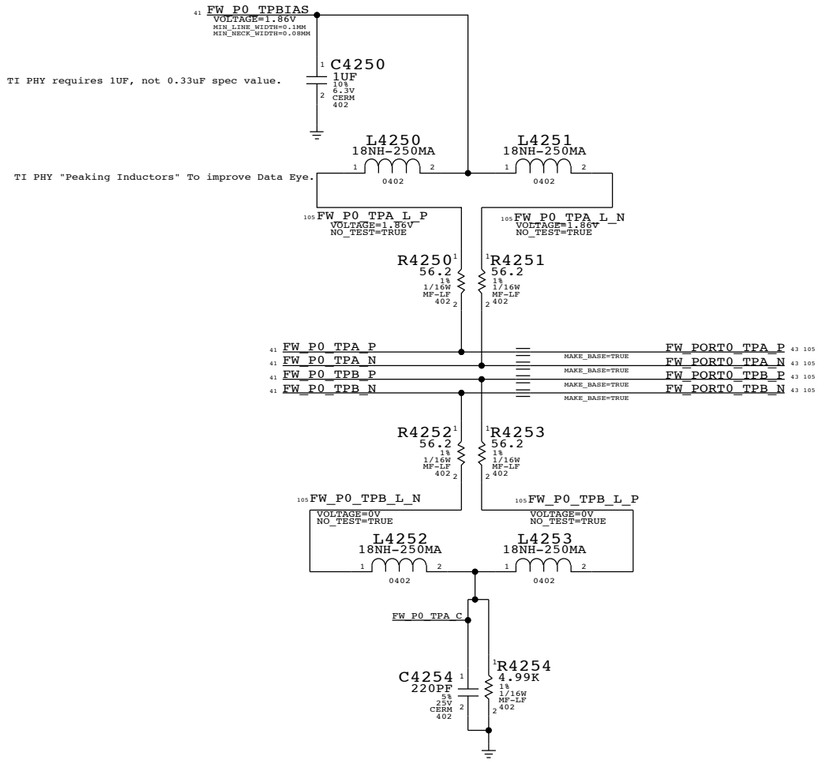


THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED.NO STUFF MEANS THAT IT IS IN BILINGUL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE.

iMacs are now one port only and have Power Code "000"

Termination

Place close to FireWire PHY



2ND & 3RD TPA/TPB PAIR UNUSED

41 FW_P1_TPBIAS = NC_FW_PORT1_TPBIAS (MAKE_BASE=TRUE, NO_TEST=TRUE)

41 FW_P1_TPA_P = NC_FW_PORT1_TPA_P (MAKE_BASE=TRUE, NO_TEST=TRUE)

41 FW_P1_TPA_N = NC_FW_PORT1_TPA_N (MAKE_BASE=TRUE, NO_TEST=TRUE)

41 FW_P2_TPBIAS = NC_FW_PORT2_TPBIAS (MAKE_BASE=TRUE, NO_TEST=TRUE)

41 FW_P2_TPA_P = NC_FW_PORT2_TPA_P (MAKE_BASE=TRUE, NO_TEST=TRUE)

41 FW_P2_TPA_N = NC_FW_PORT2_TPA_N (MAKE_BASE=TRUE, NO_TEST=TRUE)

SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE: FW: 1394B MISC

Apple Inc.

DRAWING NUMBER: 051-7845 SIZE: D

REVISION: A.0.0

BRANCH:

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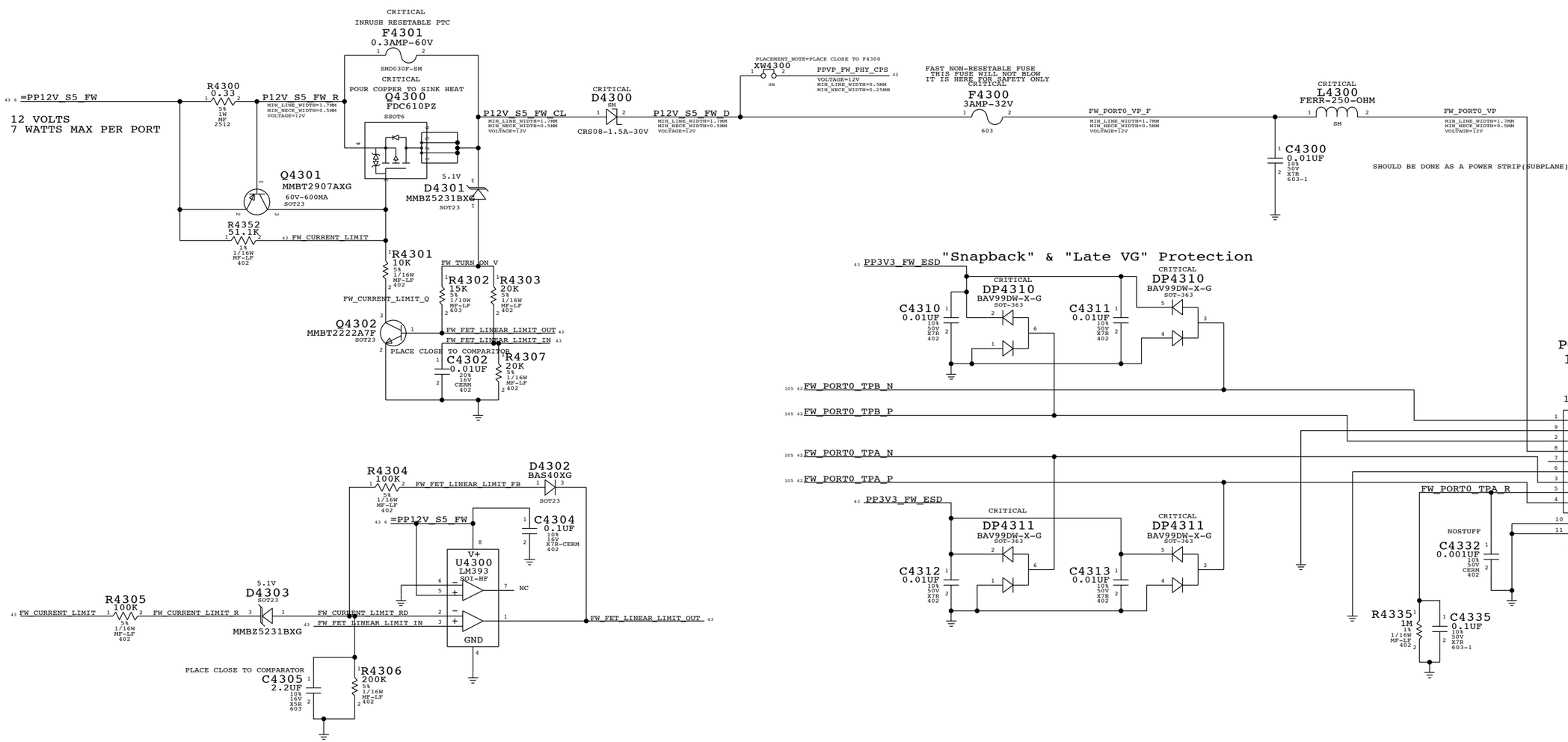

SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE

FIREWIRE CONNECTOR

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D

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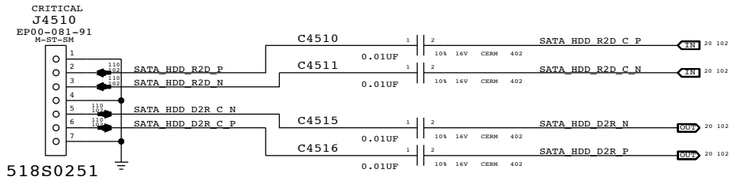
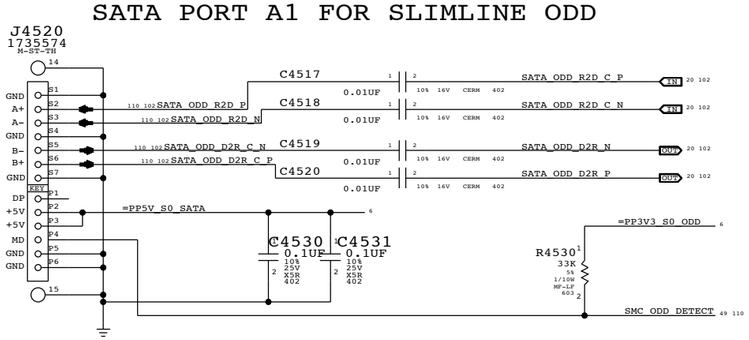
SATA PORT A0 FOR HDD

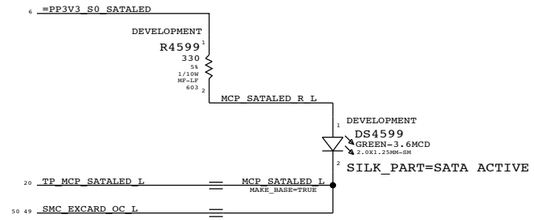


518-0361

SATA PORT A1 FOR SLIMLINE ODD



SATA Activity LED



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PAGE TITLE

SATA Connectors

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D

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USB/SMC DEBUG MUX

PORT 3

=PP5V_S3_USB
U4601 TPS2060 MSOP
USB_EXTC_OC_L
USB_EXTD_OC_L
USB_PWR_ENA_L
R4600 10K 5% 1/16W MF-LF 402
C4605 0.1UF 20% 10V CERM 402
C4606 150UF 20% 6.3V POLY-TANT CASE-D2-SM
OMIT CRITICAL
C4621 0.1UF 20% 10V CERM 402
C4631 0.1UF 20% 10V CERM 402
Q4600 2N7002 SOT23-HF
PM_EN_USB_PWR
=PP3V3_S5_SMCUSBMUX
C4650 0.1UF 20% 10V CERM 402
U4650 PI3USB102ZLE TQFN MOJOMUX
SMC_RX_L
SMC_TX_L
USB_EXTD_P
USB_EXTD_N
USB_DEBUGPRT_EN_L SEL=0: CHOOSE SMC SEL=1: CHOOSE USB
PRODUCTION R4651 0 5% 1/16W MF-LF 402
PRODUCTION R4652 0 5% 1/16W MF-LF 402
USB_D_MUXED_N
USB_D_MUXED_P
L4630 FERR-250-OHM SM
PP5V_USB2_PORT3 VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
PP5V_USB2_PORT3_F VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
C4630 0.01uF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)
L4631 120-OHM-90MA DLP0NS
USB_PORT3_N
USB_PORT3_P
J4630 USB-K22 F-ANG-TH
VDD D- D+ GND VBUS DATA- DATA+ GND
514-0659
D4630 RCLAMP0502N SLP1210N6
VBUS GND NC IO NC IO

PORT 2

=PP5V_S3_USB
U4600 TPS2060 MSOP
USB_EXTA_OC_L
USB_EXTB_OC_L
C4601 0.1UF 20% 10V CERM 402
C4602 330UF 20% 6.3V POLY-TANT CASE-D3L-SM1
OMIT CRITICAL
C4603 0.1UF 20% 10V CERM 402
C4611 0.1UF 20% 10V CERM 402
L4610 FERR-250-OHM SM
PP5V_USB2_PORT1 VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
PP5V_USB2_PORT1_F VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
C4610 0.01uF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)
L4611 120-OHM-90MA DLP0NS
USB_EXTB_N
USB_EXTB_P
USB_PORT1_N
USB_PORT1_P
J4610 USB-K22 F-ANG-TH
514-0672
D4610 RCLAMP0502N SLP1210N6
L4620 FERR-250-OHM SM
PP5V_USB2_PORT2 VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
PP5V_USB2_PORT2_F VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
C4620 0.01uF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)
L4621 120-OHM-90MA DLP0NS
USB_EXTC_N
USB_EXTC_P
USB_PORT2_N
USB_PORT2_P
J4620 USB-K22 F-ANG-TH
514-0659
D4620 RCLAMP0502N SLP1210N6

PORT 1

PORT 0

=PP5V_S3_USB
L4600 FERR-250-OHM SM
PP5V_USB2_PORT0 VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
PP5V_USB2_PORT0_F VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
C4600 0.01uF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)
L4601 120-OHM-90MA DLP0NS
USB_EXTA_N
USB_EXTA_P
USB_PORT0_N
USB_PORT0_P
J4600 USB-K22 F-ANG-TH
514-0672
D4600 RCLAMP0502N SLP1210N6

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
128S0238	1	330UF, TANT-POLY BULK CAP	C4602	CRITICAL	K23
128S0225	1	150UF, TANY-POLY BULK CAP	C4606	CRITICAL	K22

SYNC MASTER=MASTER
SYNC DATE=N/A
PAGE TITLE
EXTERNAL USB CONNECTORS
Apple Inc.
DRAWING NUMBER 051-7845
SIZE D
REVISION A.0.0
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PAGE 46 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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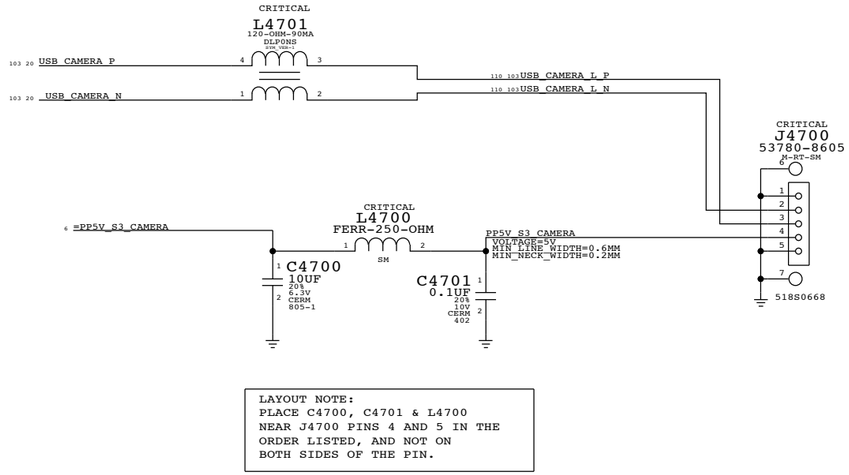
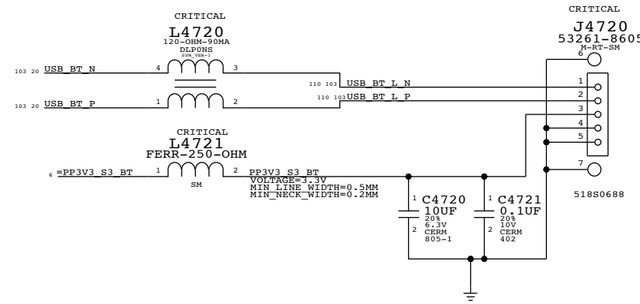
CAMERA CONNECTOR & FILTER

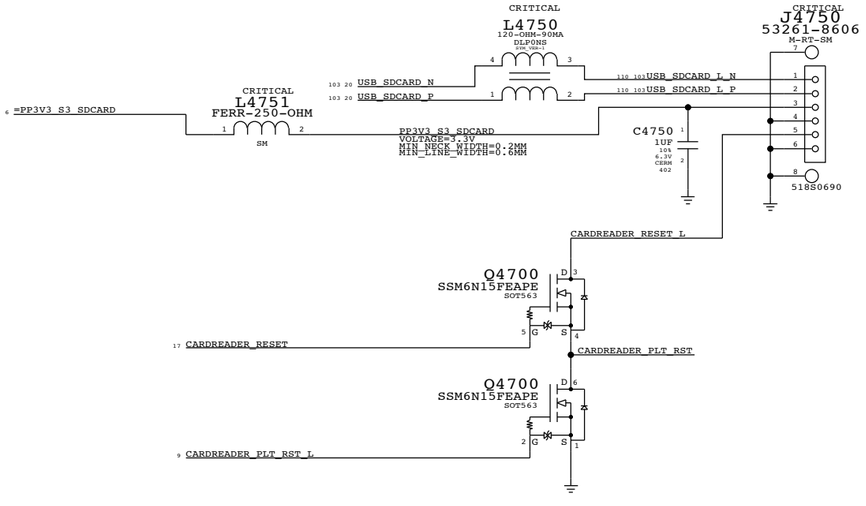


LAYOUT NOTE:
PLACE C4700, C4701 & L4700
NEAR J4700 PINS 4 AND 5 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.

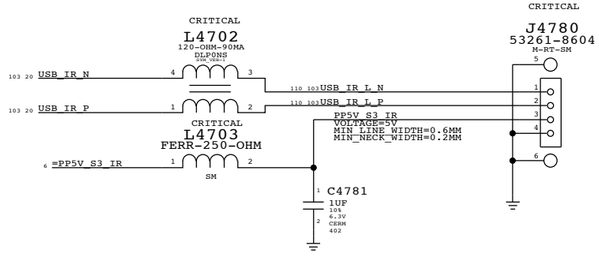
K37L (BLUETOOTH) CONNECTOR



SD Card Reader Board Connector



IR RECEIVER CONNECTOR



SYNC MASTER=MASTER	SYNC DATE=MASTER
PAGE TITLE: Internal USB Connections	
Apple Inc.	DRAWING NUMBER: 051-7845 SIZE: D
	REVISION: A.0.0
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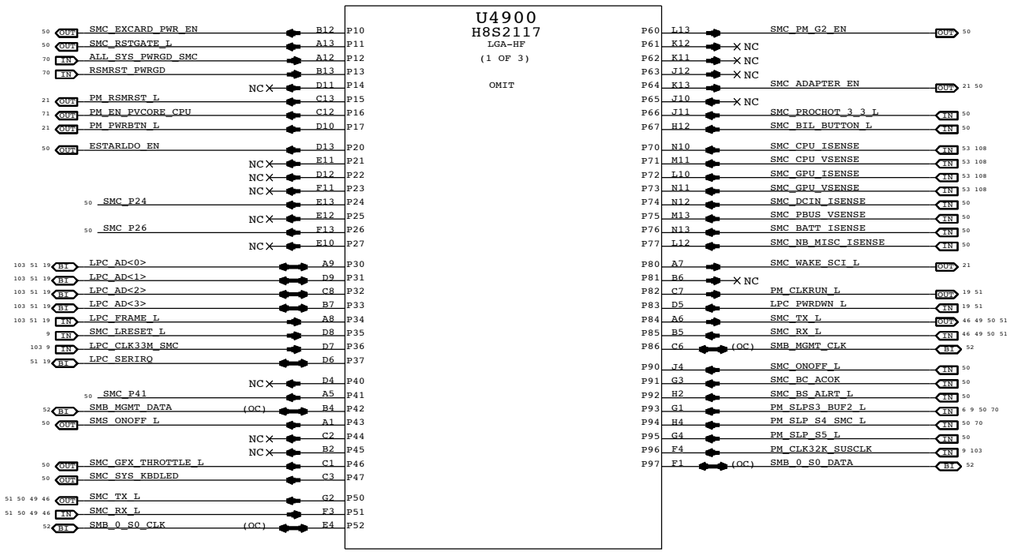
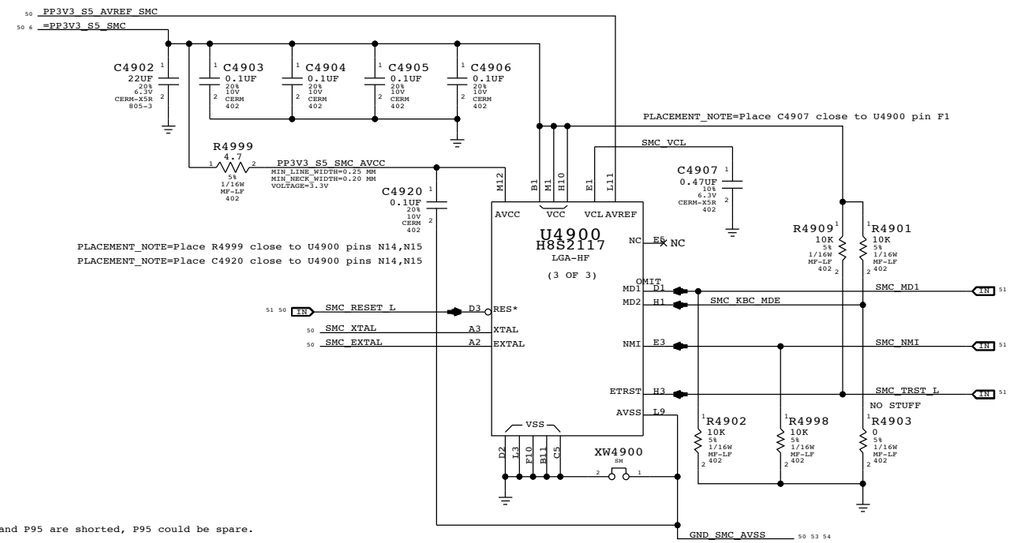
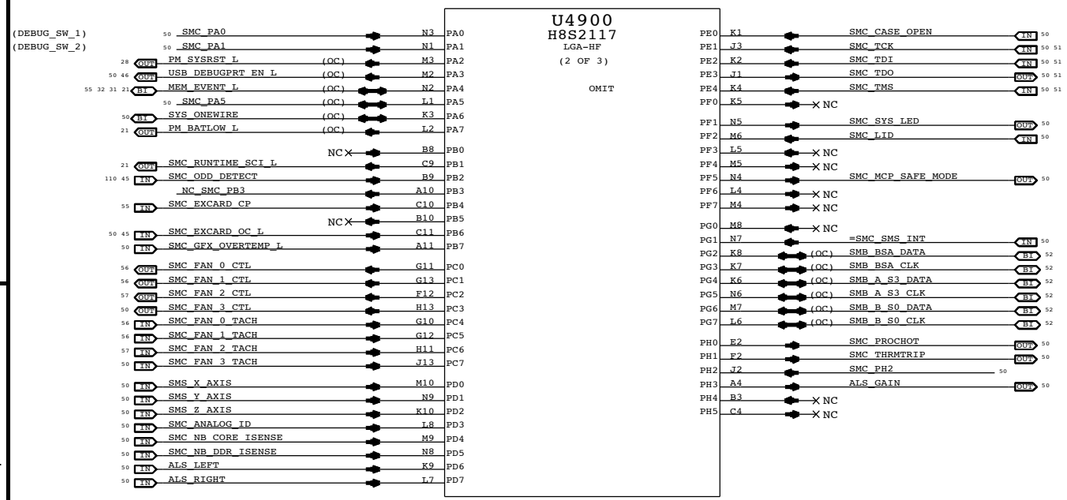
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





NOTE: P94 and P95 are shorted, P95 could be spare.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE

SMC

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D

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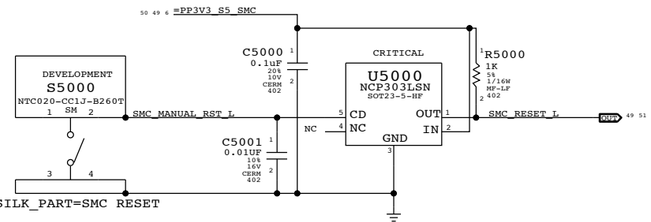
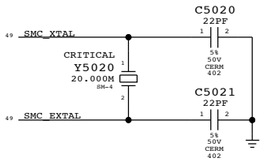
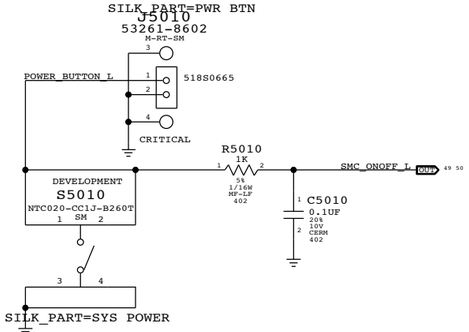
SMC Reset Button / Brownout Detect



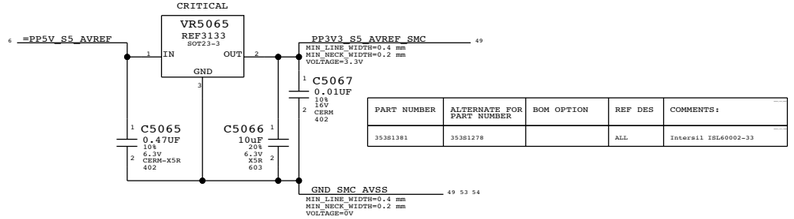
SMC Crystal Circuit



POWER BUTTON



SMC AVREF Supply



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
35381381	35381278		ALL	Intersil ISL60002-33

UNUSED TP/NC ALIASES - PORT D - INTERNAL PULLUPS

SMS_Z_AXIS	NC_SMS_Z_AXIS	MAKE_BASE=TRUE	NO_TEST=TRUE
ALS_LEFT	NC_ALS_LEFT	MAKE_BASE=TRUE	NO_TEST=TRUE
ALS_RIGHT	NC_ALS_RIGHT	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_ANALOG_ID	NC_SMC_ANALOG_ID	MAKE_BASE=TRUE	NO_TEST=TRUE

UNUSED TP/NC ALIASES

SMC_SYS_LED	TP_SMC_SYS_LED	MAKE_BASE=TRUE	
ALS_GAIN	NC_ALS_GAIN	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_PM_G2_EN	TP_SMC_PM_G2_EN	MAKE_BASE=TRUE	
SMC_SYS_KBDLED	TP_SMC_SYS_KBDLED	MAKE_BASE=TRUE	
SMC_EXCARD_PWR_EN	TP_SMC_EXCARD_PWR_EN	MAKE_BASE=TRUE	
SMS_ONOFF_L	TP_SMS_ONOFF_L	MAKE_BASE=TRUE	
SMC_RSTGATE_L	TP_SMC_RSTGATE_L	MAKE_BASE=TRUE	
SMC_P24	TP_SMC_P24	MAKE_BASE=TRUE	
SMC_P26	TP_SMC_P26	MAKE_BASE=TRUE	
SMC_P41	TP_SMC_P41	MAKE_BASE=TRUE	
ESTARLDO_EN	TP_ESTARLDO_EN	MAKE_BASE=TRUE	

ANALOG SENSORS

SMC_DCIN_ISENSE	SMC_CPU_INPUT_ISENSE	MAKE_BASE=TRUE	53
SMC_PBUS_VSENSE	SMC_CPU_INPUT_VSENSE	MAKE_BASE=TRUE	53
SMS_X_AXIS	SMC_1V5_S0_VSENSE	MAKE_BASE=TRUE	54 108
SMS_Y_AXIS	SMC_MCP_CORE_VSENSE	MAKE_BASE=TRUE	54 108
SMC_NB_DDR_ISENSE	SMC_1V5_S0_ISENSE	MAKE_BASE=TRUE	54 108
SMC_NB_CORE_ISENSE	SMC_MCP_CORE_ISENSE	MAKE_BASE=TRUE	54 108
SMC_BATT_ISENSE	SMC_UNUSED_ADC_PORT7	MAKE_BASE=TRUE	
SMC_NB_MISC_ISENSE			

R5050 10K 5% 1/16W MF-LF 402

MISC. SIGNAL ALIASES

SMC_GFX_OVERTEMP_L	MXM_ALERT_L	MAKE_BASE=TRUE	85
SMC_GFX_THROTTLE_L	MXM_PWR_LEVEL	MAKE_BASE=TRUE	85

R5020 51 5% 1/16W MF-LF 402 (IG) — SMC_IG_THROTTLE_L (MAKE_BASE=TRUE) — 21

R5019 0 5% 1/16W MF-LF 402 — SMC_MCP_SAFE_MODE — MCP_SPKR — 21

FOR <RDAR://PROBLEM/5925345>

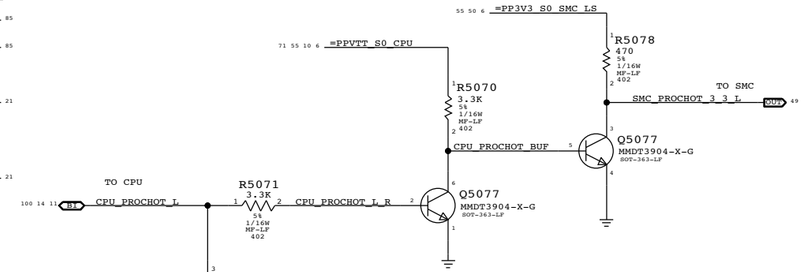
SMC_ONOFF_L	R5032	10K	5% 1/16W MF-LF 402	
SMC_LID	R5033	100K	5% 1/16W MF-LF 402	
SMC_PH2	R5034	10K	5% 1/16W MF-LF 402	
SMC_TX_L	R5035	10K	5% 1/16W MF-LF 402	
SMC_RX_L	R5036	100K	5% 1/16W MF-LF 402	
SYS_ONEWIRE	R5037	2.0K	5% 1/16W MF-LF 402	
SMC_BS_ALRT_L	R5038	100K	5% 1/16W MF-LF 402	
SMC_TMS	R5039	10K	5% 1/16W MF-LF 402	
SMC_TDO	R5040	10K	5% 1/16W MF-LF 402	
SMC_TDI	R5041	10K	5% 1/16W MF-LF 402	
SMC_TCK	R5042	10K	5% 1/16W MF-LF 402	
SMC_EXCARD_OC_L (NO STUFF)	R5043	10K	5% 1/16W MF-LF 402	
SMC_PA0	R5096	10K	5% 1/16W MF-LF 402	
SMC_PA1	R5090	10K	5% 1/16W MF-LF 402	
SMC_BIL_BUTTON_L	R5092	10K	5% 1/16W MF-LF 402	
SMC_FAN_3_CTL	R5095	100K	5% 1/16W MF-LF 402	
SMC_FAN_3_TACH	R5097	100K	5% 1/16W MF-LF 402	
SMC_BC_ACOK	R5047	10K	5% 1/16W MF-LF 402	
SMC_ADAPTER_EN	R5049	10K	5% 1/16W MF-LF 402	
USB_DEBUGPRT_EN_L	R5098	10K	5% 1/16W MF-LF 402	
=SMC_SMS_INT — SMC_SMS_INT (MAKE_BASE=TRUE)	R5091	10K	5% 1/16W MF-LF 402	

=PP3V3_S5_SMC

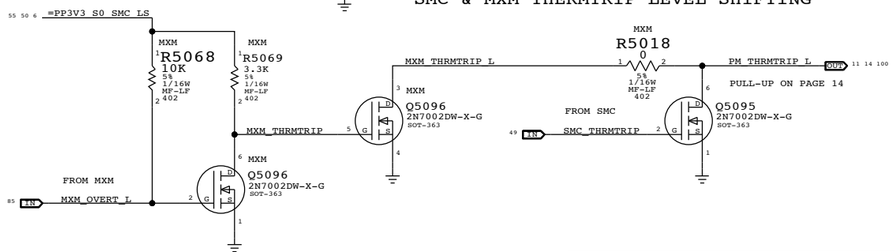
SMC_PA5	R5093	10K	5% 1/16W MF-LF 402
SMC_GFX_OVERTEMP_L	R5099	10K	5% 1/16W MF-LF 402
SMC_CASE_OPEN	R5046	10K	5% 1/16W MF-LF 402
PM_SLPS3_BUF2_L	R5094	100K	5% 1/16W MF-LF 402
PM_SLP_S4_SMC_L (MAKE_BASE=TRUE)	R5089	100K	5% 1/16W MF-LF 402
PM_SLP_S5_L			PLACEMENT_NOTE=PLACE CLOSE TO U4900(SMC)

=PP3V3_S0_SMC

SMC PROCHOT 3.3V LEVEL SHIFTING



SMC & MXM THERMTRIP LEVEL SHIFTING



SYNC MASTER=MASTER — SYNC DATE=N/A

PAGE TITLE: SMC Support

Apple Inc.

DRAWING NUMBER: 051-7845 — SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 50 OF 110

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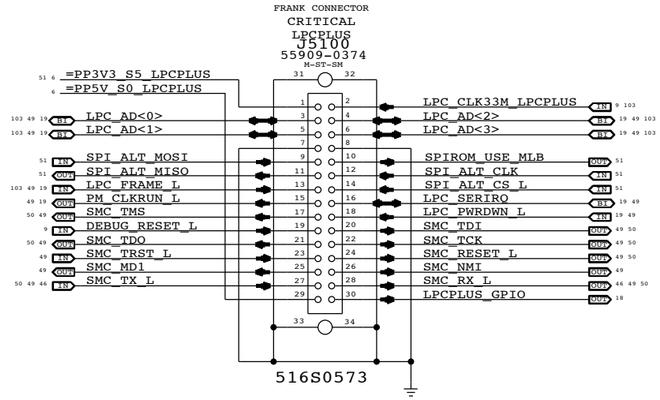
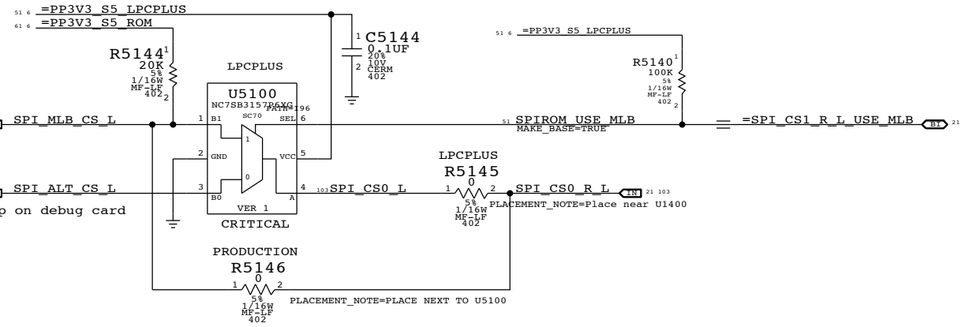
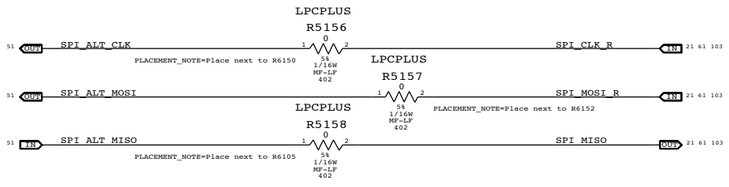
LPC+SPI Connector



Alternate SPI ROM Support



SPI Bus Series Resistance Option



SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE
LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D
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PAGE 51 OF 110
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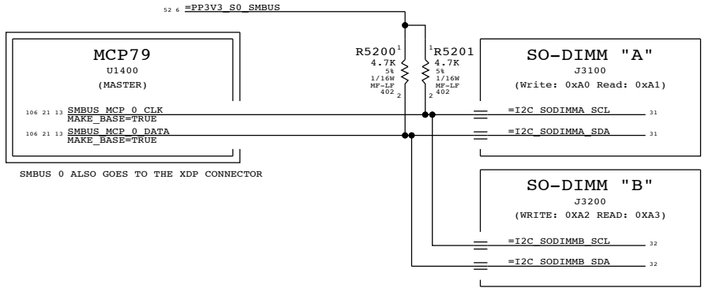
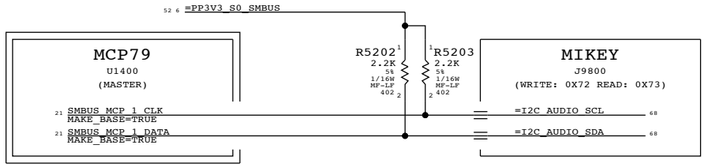
MCP79 SMBUS "0" CONNECTIONS

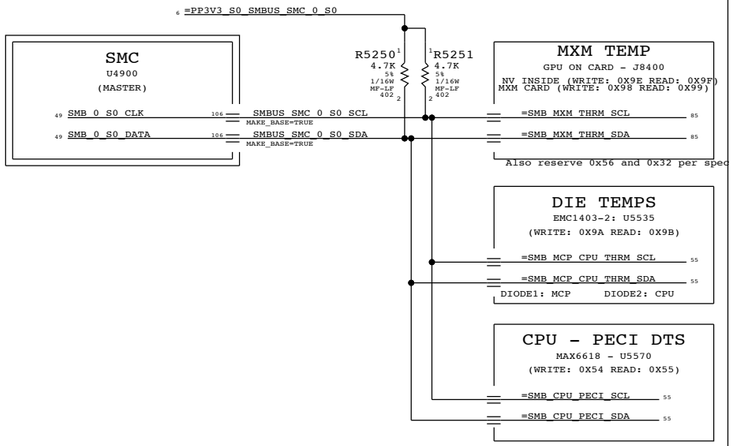


SMBUS 0 ALSO GOES TO THE XDP CONNECTOR

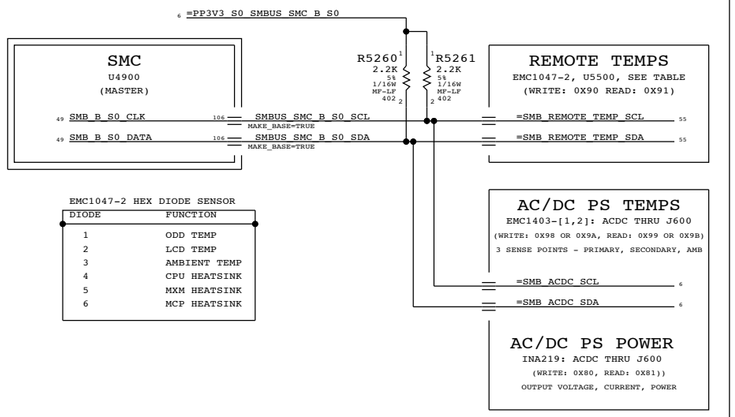
MCP79 SMBUS "1" CONNECTIONS



SMC "0" SMBus Connections



SMC "B" SMBus Connections

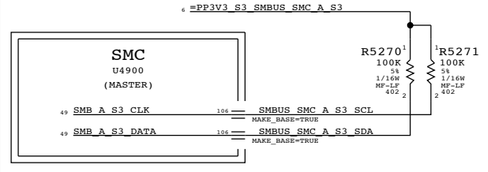


EMC1047-2 HEX DIODE SENSOR

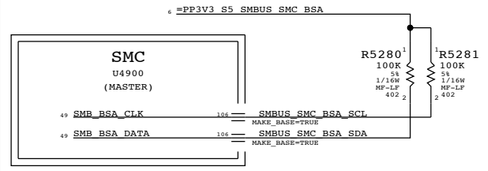
DIODE	FUNCTION
1	ODD TEMP
2	LCD TEMP
3	AMBIENT TEMP
4	CPU HEATSINK
5	MXM HEATSINK
6	MCP HEATSINK

SMC "A" SMBus Connections

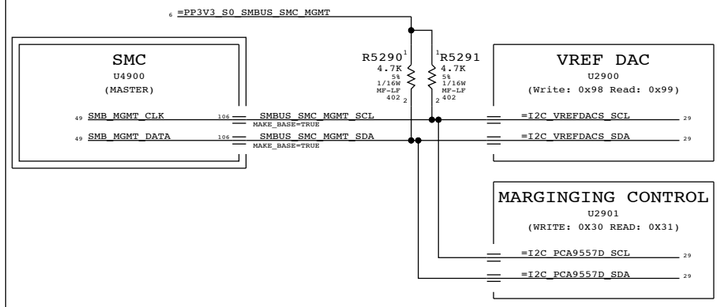
NOTE: SMC RMT BUS REMAINS POWERED AND MAY BE ACTIVE IN S3 STATE



UNUSED SMC "BATTERY A" SMBUS CONNECTIONS



SMC "MANAGEMENT" SMBUS CONNECTIONS



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SMBUS CONNECTIONS

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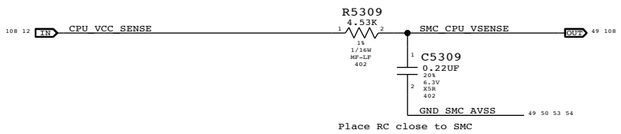
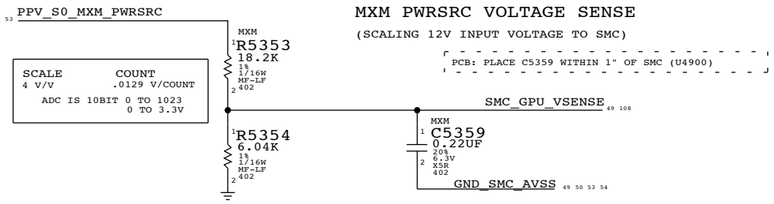
CPU Voltage Sense / Filter



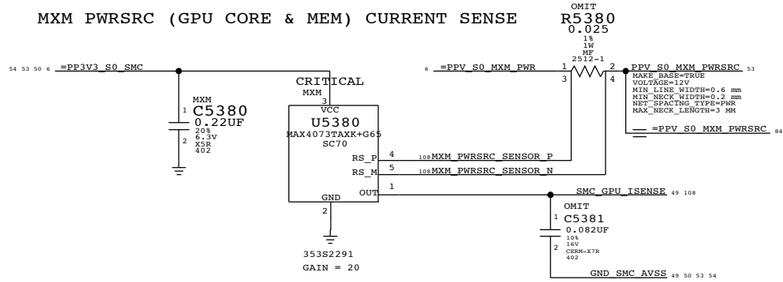
Place RC close to SMC

MXM PWRSRC VOLTAGE SENSE

(SCALING 12V INPUT VOLTAGE TO SMC)



MXM PWRSRC (GPU CORE & MEM) CURRENT SENSE



K50 SET FOR APPROX 2V AT 4A ON PWRSRC

SCALE	COUNT
2 A/V	.0064453 A/COUNT

ADC IS 10BIT 0 TO 1023, 0 TO 3.3V

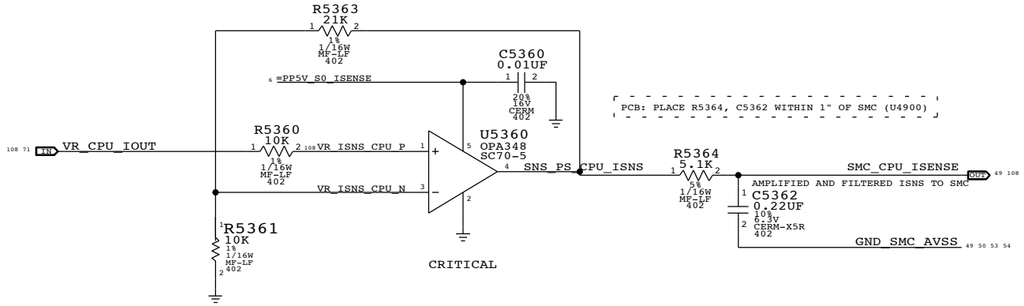
K51 SET FOR APPROX 1.98V AT 5.5A ON PWRSRC

SCALE	COUNT
2.778 A/V	.0087518 A/COUNT

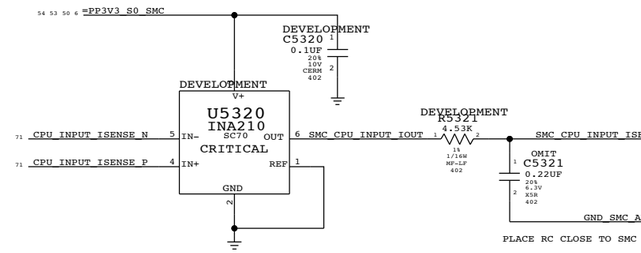
ADC IS 10BIT 0 TO 1023, 0 TO 3.3V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
107S0063	1	25 MILLIOHM	R5380	CRITICAL	K22_MXM
107S0111	1	18 MILLIOHM	R5380	CRITICAL	K23_MXM
132S0242	1	CAP,0.082UF,402	C5381		MXM
116S0090	1	RES,10KOHM,5%,402	C5381		IG

CPU CURRENT SENSE AMP & FILTER



CPU CORE INPUT SIDE CURRENT & VOLTAGE SENSE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0080	1	CAP, 0.22UF, 0402	C5321		DEVELOPMENT
116S0004	1	RES, 0-Ohm, 0402	C5321		PRODUCTION

SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE

CPU/MXM CURRENT AND VOLTAGE SENSE

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D

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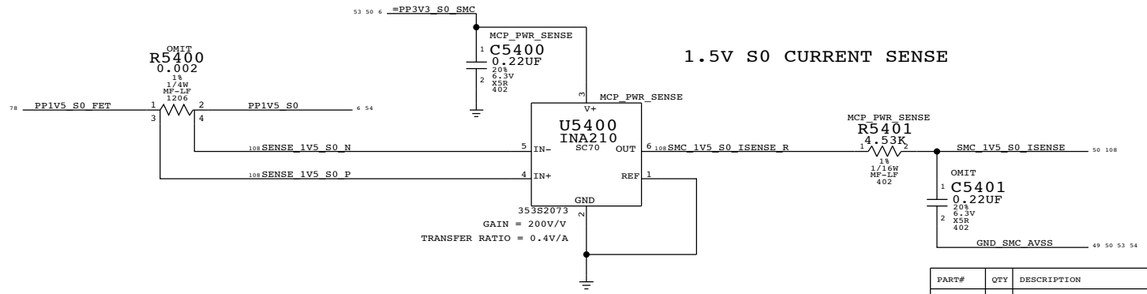
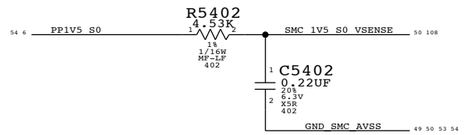
1.5V S0 CURRENT SENSE



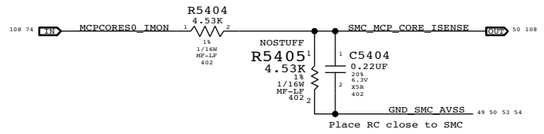
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
104S0018	1	RES,2 MILLIOHM,1206	R5400	CRITICAL	MCP_PWR_SENSE
101S0414	1	RES,0 OHM,1206,20MILLIOHM MAX	R5400	CRITICAL	PRODUCTION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0080	1	CAP, 0.22UF, 0402	C5401		MCP_PWR_SENSE
116S0004	1	RES, 0 OHM, 0402	C5401		PRODUCTION

1.5V S0 VOLTAGE SENSE

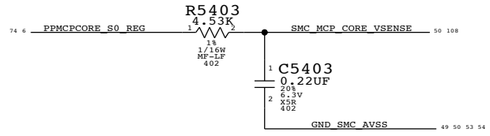


MCP CORE CURRENT SENSE



SCALE IS 0.116 V/A

MCP CORE VOLTAGE SENSE



SYNC MASTER=K51 SYNC DATE=12/08/2008

PAGE TITLE

MCP CURRENT AND VOLTAGE SENSE

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D

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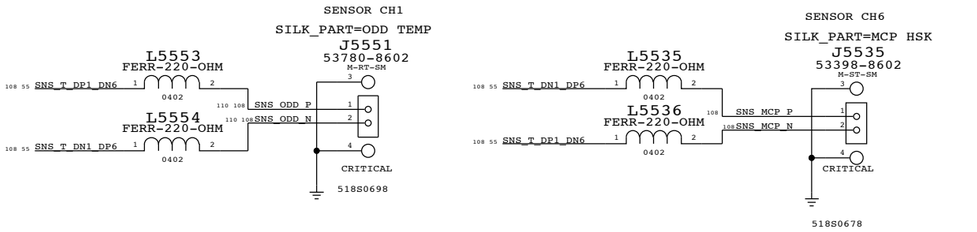
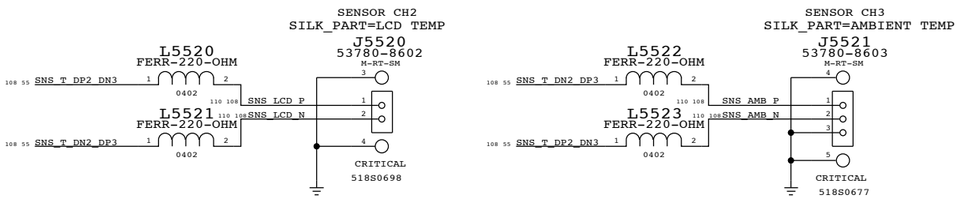
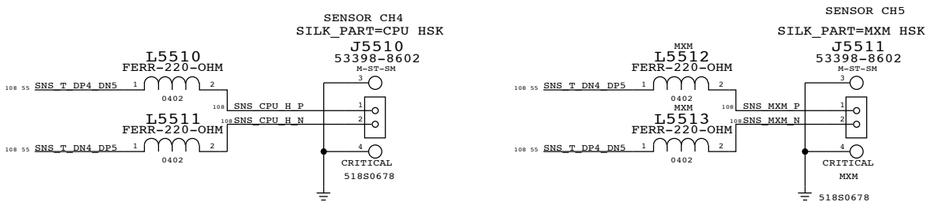
REMOTE THERMAL SENSORS

HEATSINKS, AMBIENT, PANEL AND ODD

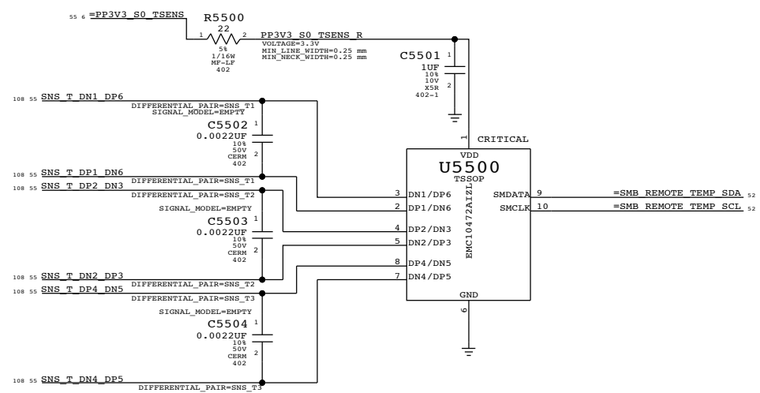




PLACE HSK SENSOR CONN. TOP SIDE NEAR MXM OR CPU

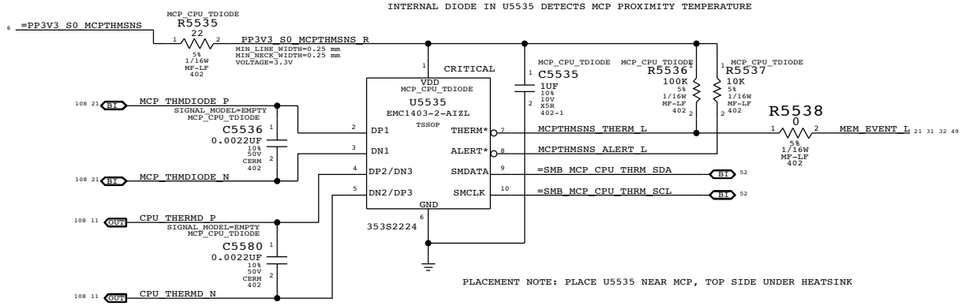


REMOTE THERMAL SENSORS (HEATSINKS AND ODD)



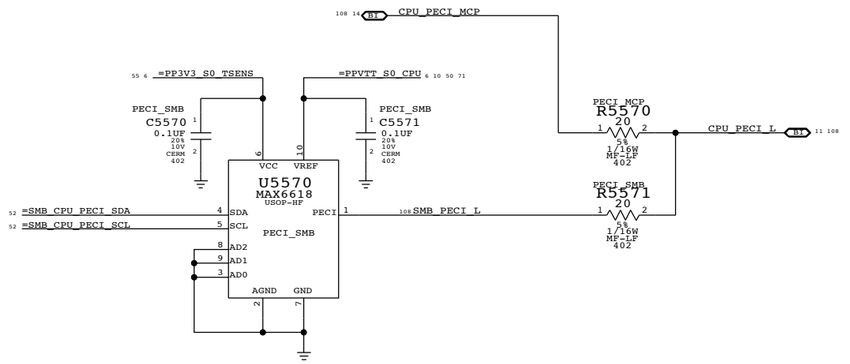
MCP & CPU T-Diode Thermal Sensor

INTERNAL DIODE IN U5535 DETECTS MCP PROXIMITY TEMPERATURE



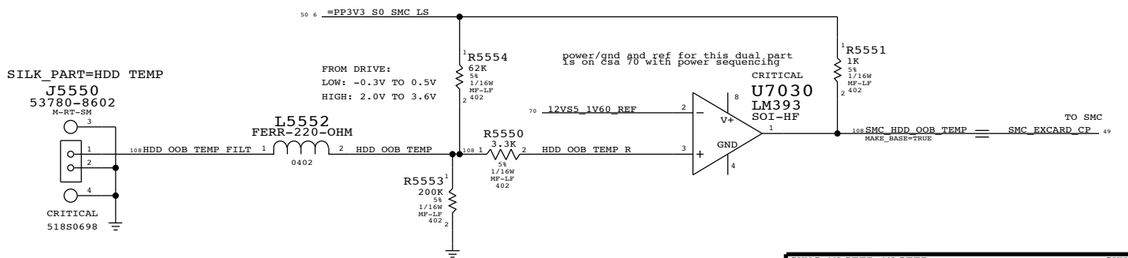
PLACEMENT NOTE: PLACE U5535 NEAR MCP, TOP SIDE UNDER HEATSINK

CPU PECI DTS OPTIONS



Consider 3rd option - direct to SMC

HDD OUT OF BAND TEMPERATURE SENSING LEVEL SHIFTING



Drive active = valid signal protocol
Drive asleep = HDD drives HDD_OOB_TEMP low
Drive disconnected = pulled high

Cannot pull low because some drives use this bit to determine 1.5 Gbps vs. 3.0 Gbps SATA

Must pull high to 2.5V for compatibility with all drives

SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE

Thermal Sensors

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D

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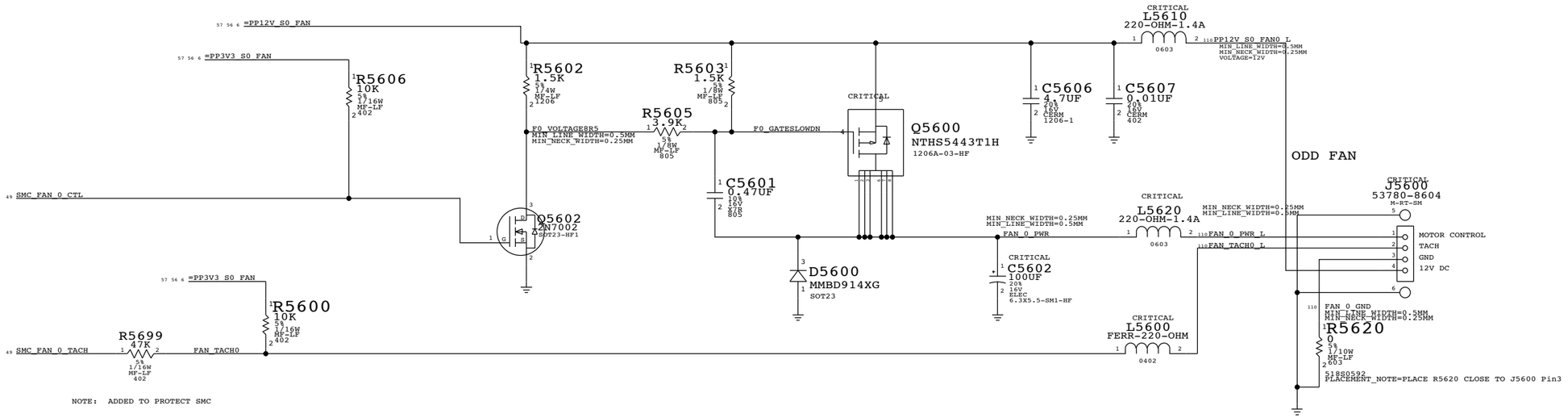
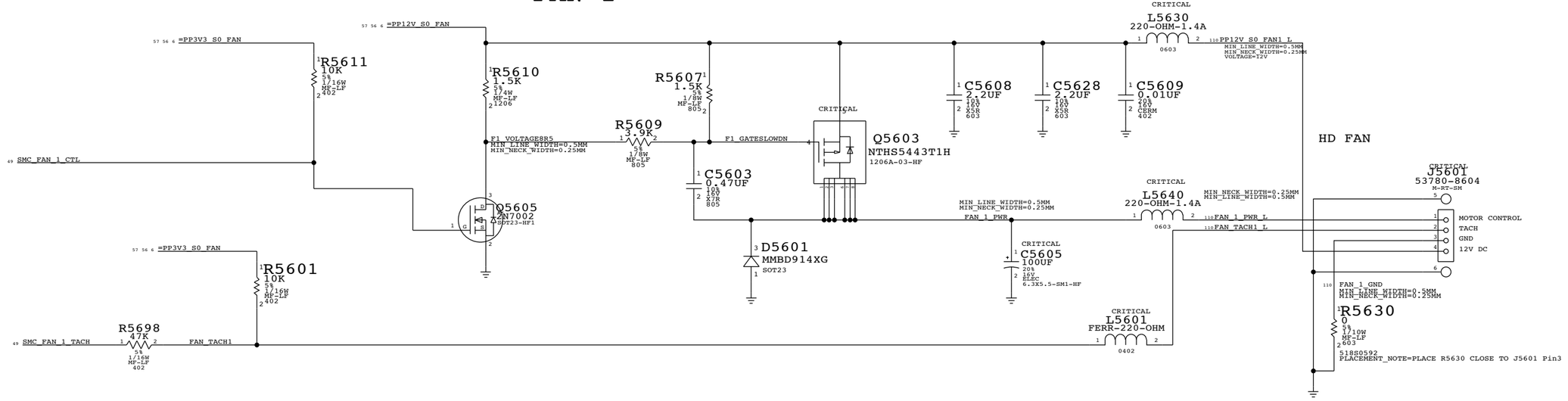
FAN 0



FAN 1



SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE: HD AND OD FAN

Apple Inc.

DRAWING NUMBER: 051-7845 SIZE: D

REVISION: A.0.0

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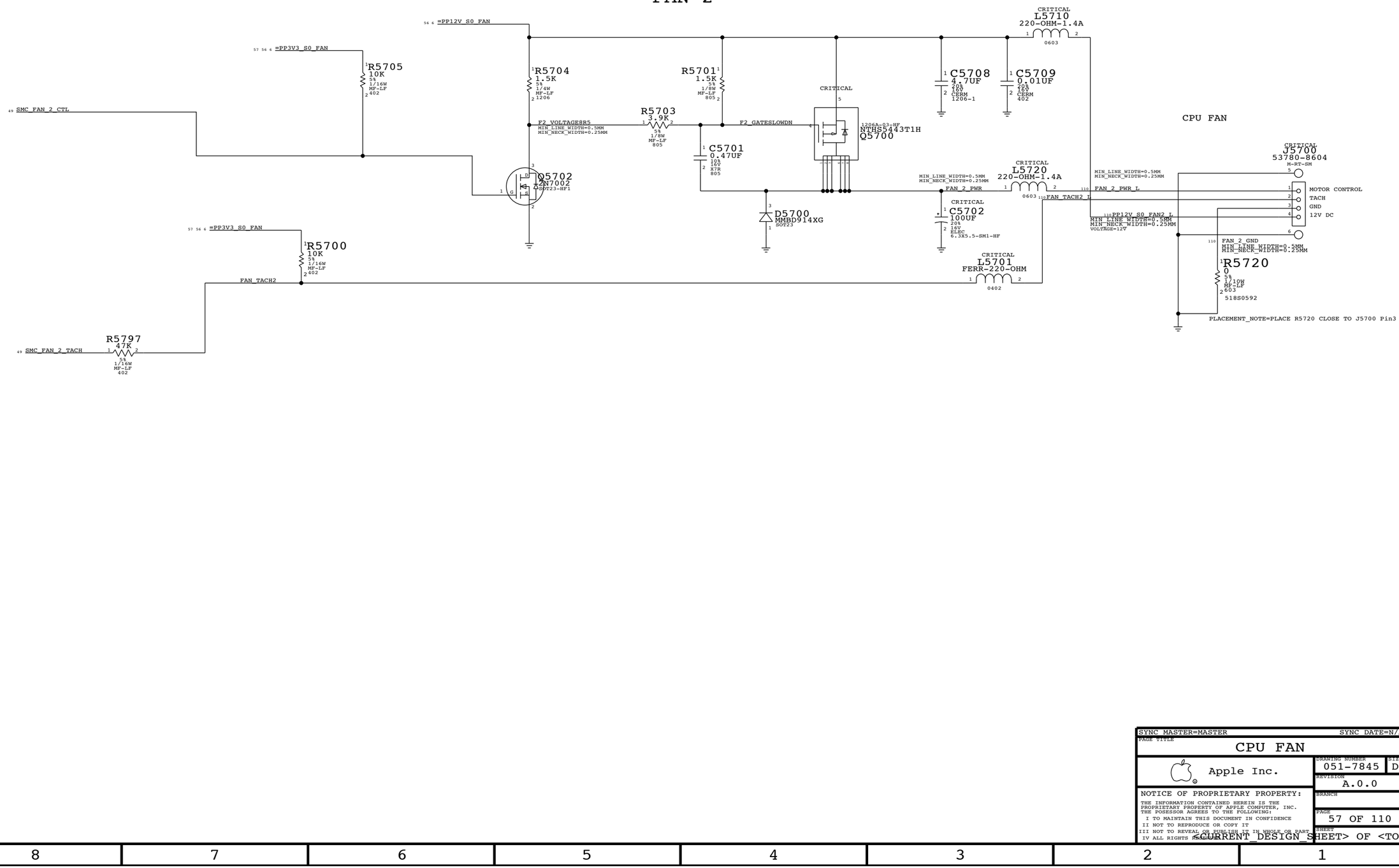
FAN 2



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CPU FAN

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8 7 6 5 4 3 2 1

D C B A

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8 7 6 5 4 3 2 1

D C B A

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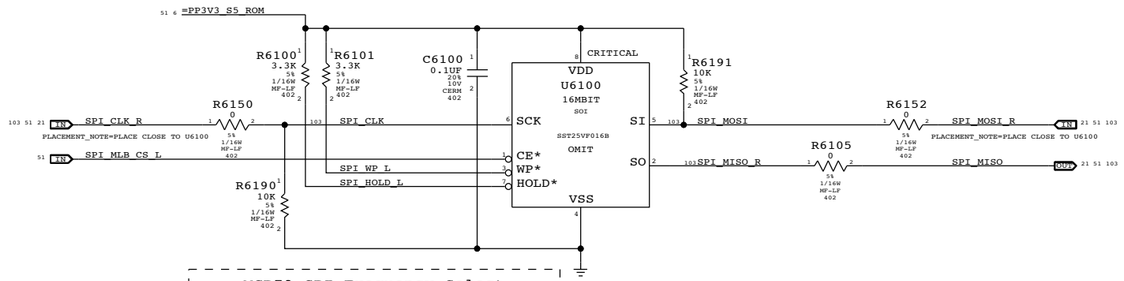
8 7 6 5 4 3 2 1



MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: MCP79 only issues 'READ' (0x03) commands not 'READ_FAST' (0x0B). Limits SPI bus frequency and part selection.

SST25VF016B max speed for READ command is 25MHz.

SYNC MASTER=K51 SYNC DATE=12/08/2008

PAGE TITLE

SPI ROM

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D

REVISION A.0.0

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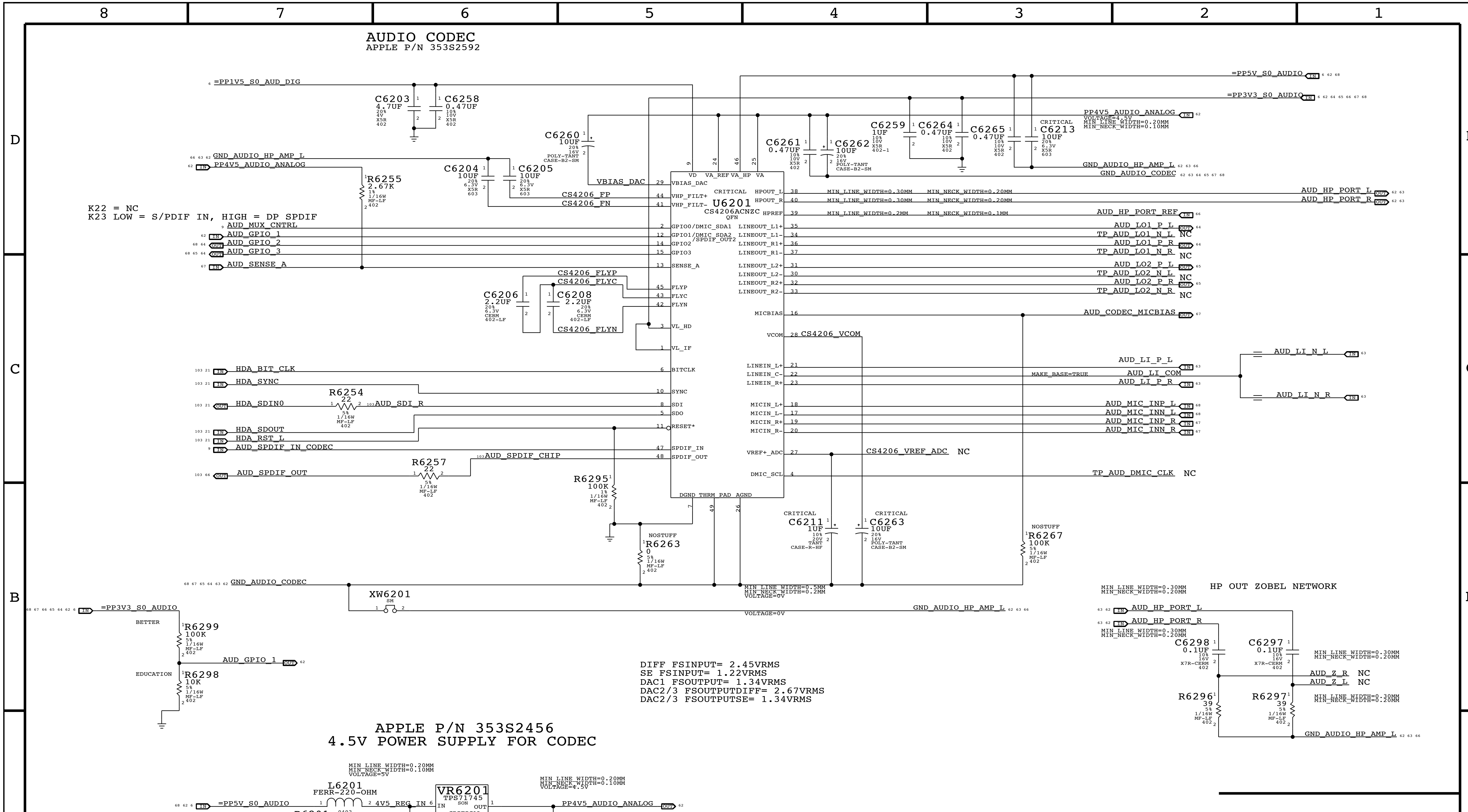

SYNC_MASTER=SKIPAUDIO SYNC_DATE=06/01/2009

PAGE TITLE

AUDIO: CODEC/REGULATOR

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D

REVISION A.0.0

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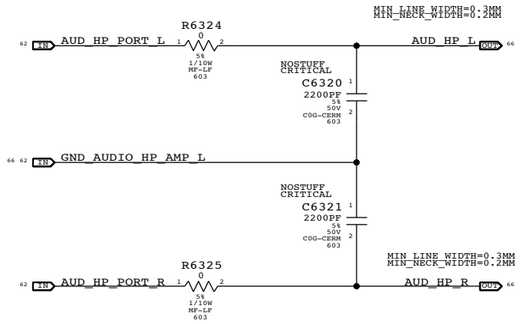
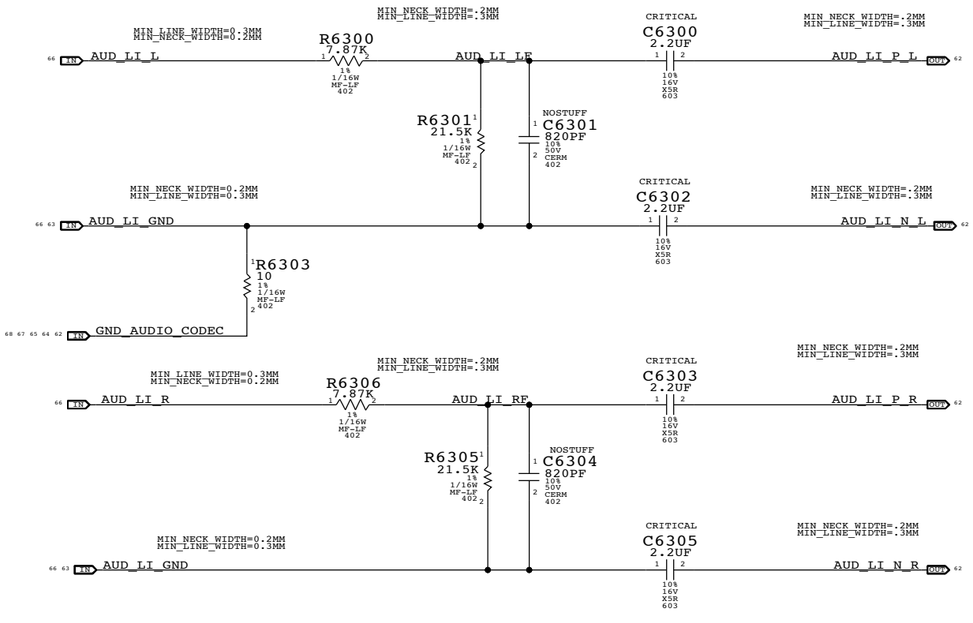
1ST ORDER DAC FILTER PLACEHOLDER



CODEC Nom SE RIN = 20K OHMS
FC = 5 HZ Max
VIN = 2VRMS, CODEC VIN = 1.14 VRMS
NET RIN = 18K OHMS



SYNC MASTER=SKIPAUDIO SYNC DATE=06/01/2009

PAGE TITLE
AUDIO: FILTER/BUFFER

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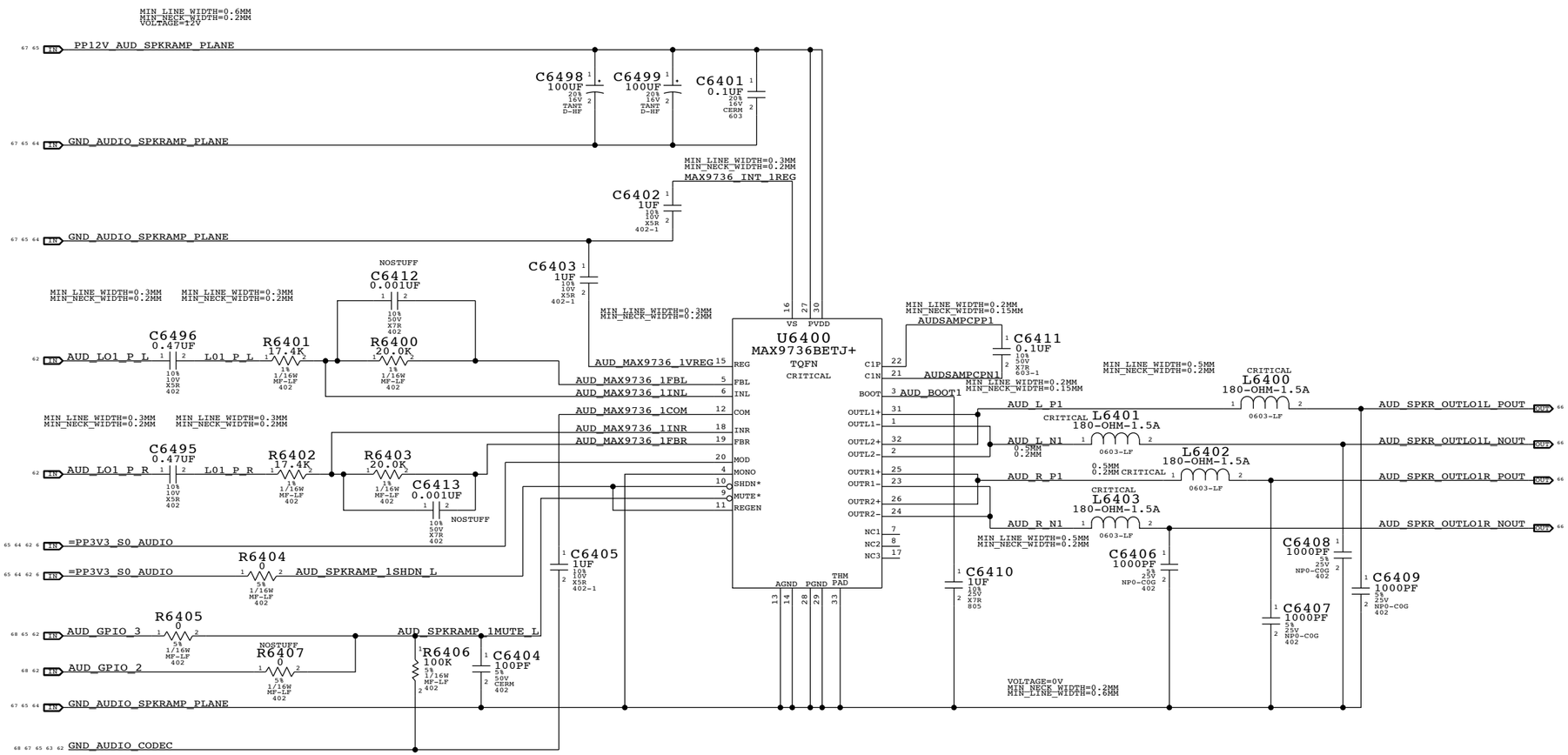
TWEETER SPEAKER AMPLIFIER

MAX9736B APN:353S2042

GAIN = -4.8(20K/17.4K)
CODEC OUT = 1.335VRMS
AMP VOUT = 7.355VRMS

TURN ON TIME: 110MS
TURN ON DELAY: 150MS
RIN = 17.4 OHMS
FC = 19.5 HZ

POUT = 6.76 W INTO 8 OHMS @ 1% THD+N



SYNC MASTER=SKIPAUDIO	SYNC DATE=06/01/2009
PAGE TITLE: AUDIO: SPEAKER AMP	
Apple Inc.	DRAWING NUMBER: 051-7845 SIZE: D
	REVISION: A.0.0
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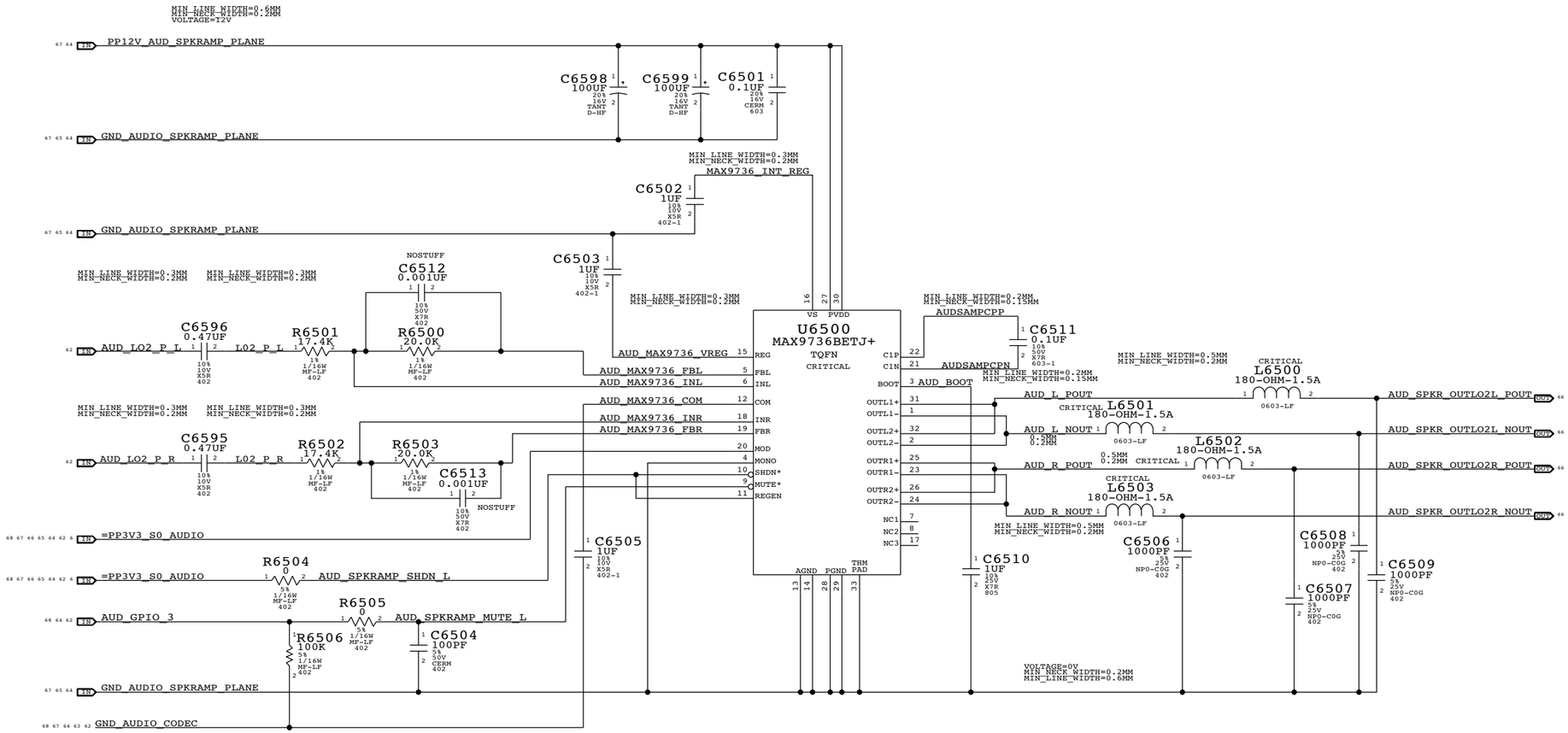
WOOFER SPEAKER AMPLIFIER

MAX9736B APN:353S2042

GAIN = -4.8(20K/17.4K)
CODEC OUT = 1.335VRMS
AMP VOUT = 7.355VRMS
POUT = 6.76 W INTO 8 OHMS @ 1% THD+N

TURN ON TIME: 110MS
TURN ON DELAY: 150MS
RIN = 17.4 OHMS
FC = 19.5 HZ



SYNC MASTER=SKIPAUDIO	SYNC DATE=06/01/2009
PAGE TITLE: AUDIO: SPEAKER AMP	
Apple Inc.	DRAWING NUMBER: 051-7845 SIZE: D
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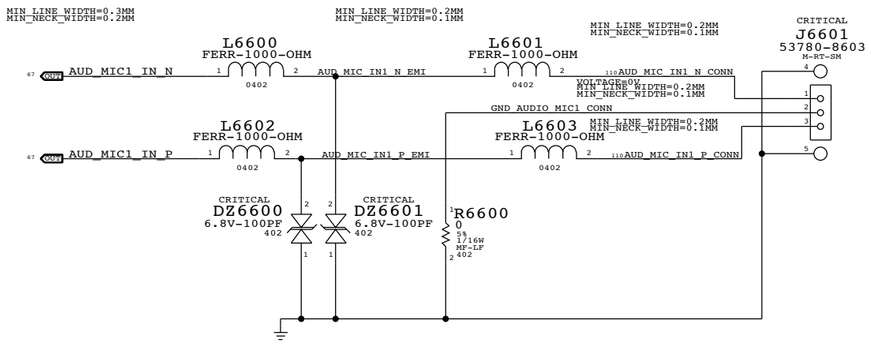
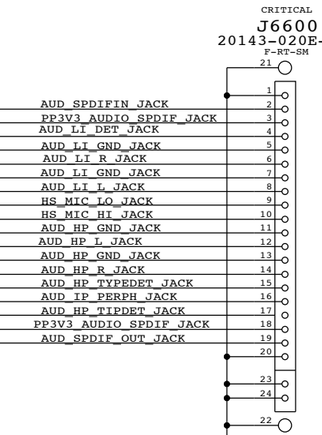
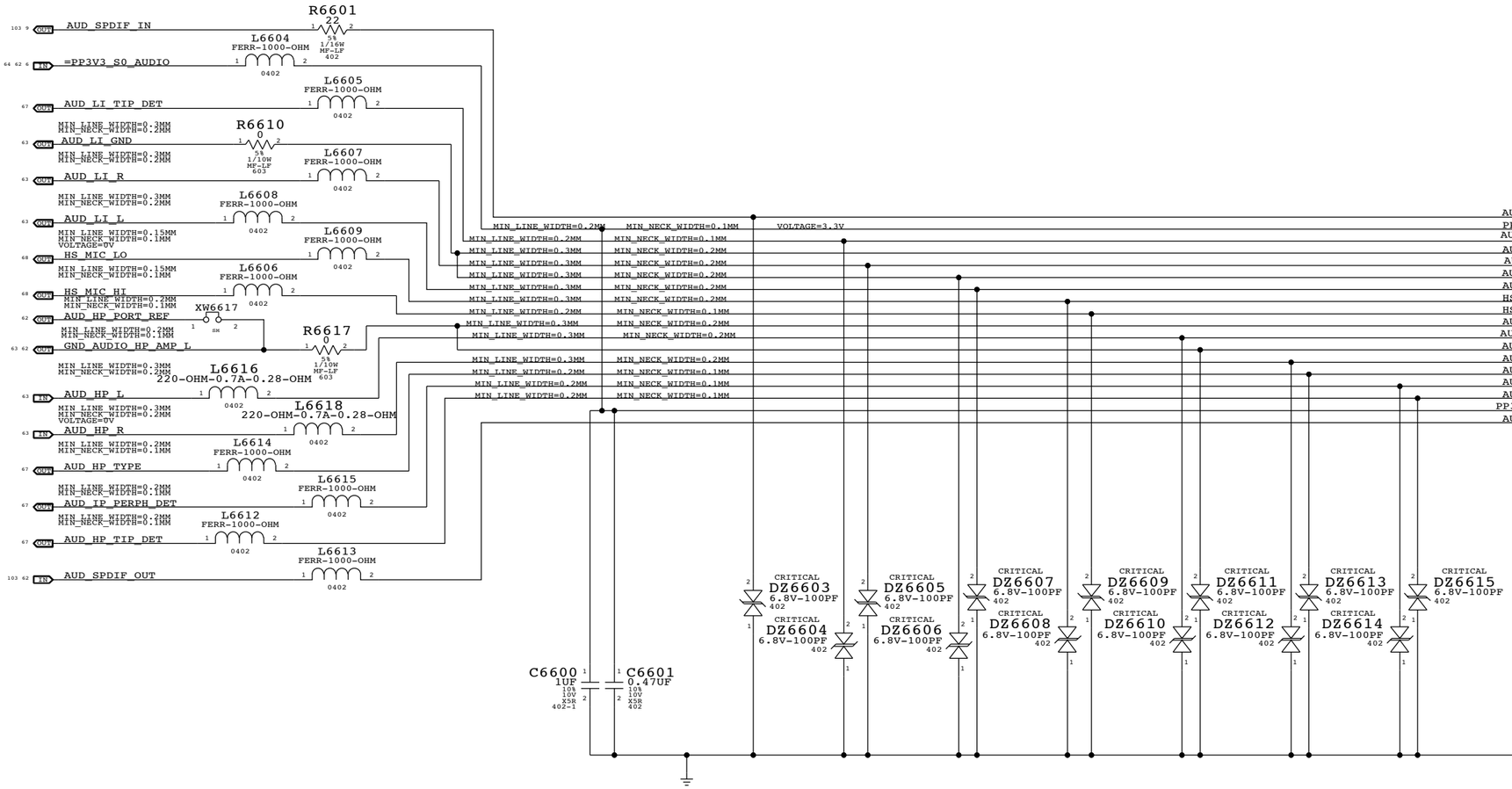
INTERNAL MIC CON
APPLE P/N 518S0677



SPEAKER CABLE CONNECTORS
APPLE P/N 518S0748
APPLE P/N 518S0656

REMOTE I/O CONNECTOR
APPLE P/N 518S0723





SYNC MASTER=SKIPAUDIO SYNC DATE=06/01/2009

PAGE TITLE
Audio: MLB to I/O Conn.

Apple Inc.

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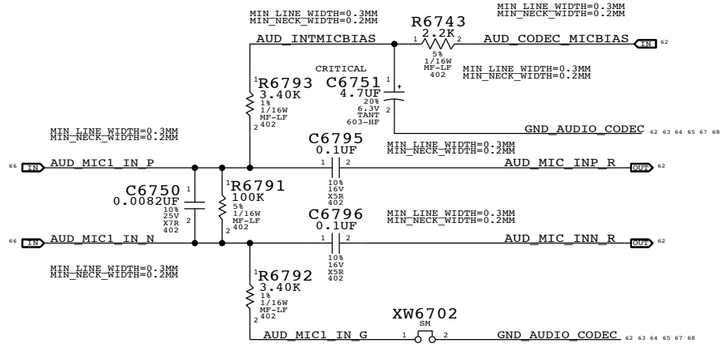
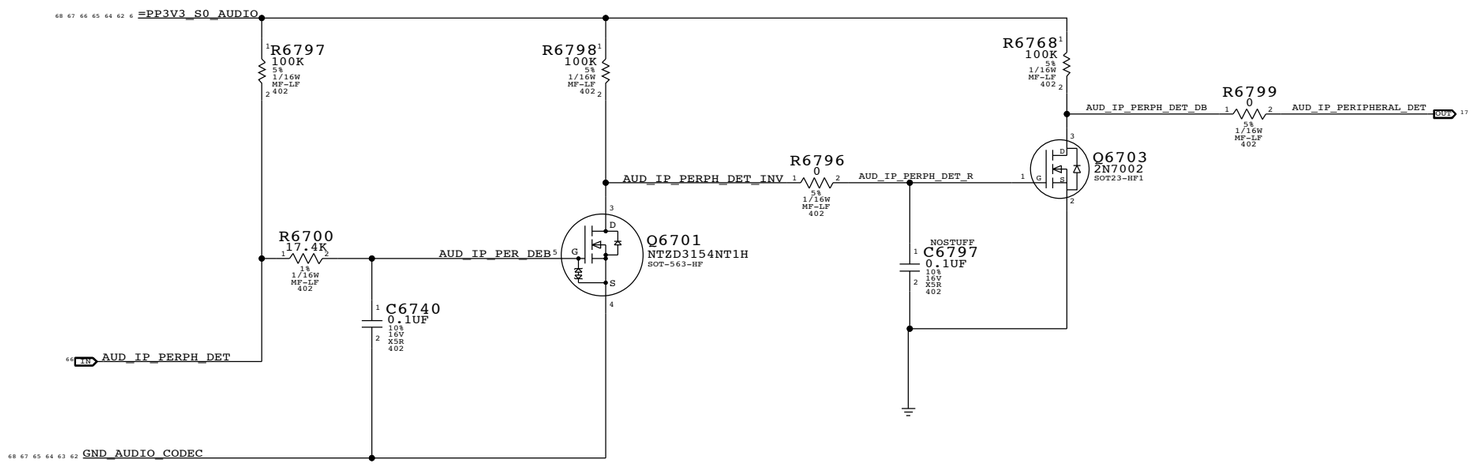
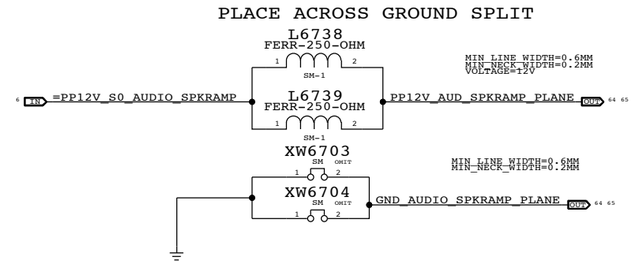
MICROPHONE IMPEDANCE MATCHING CIRCUIT



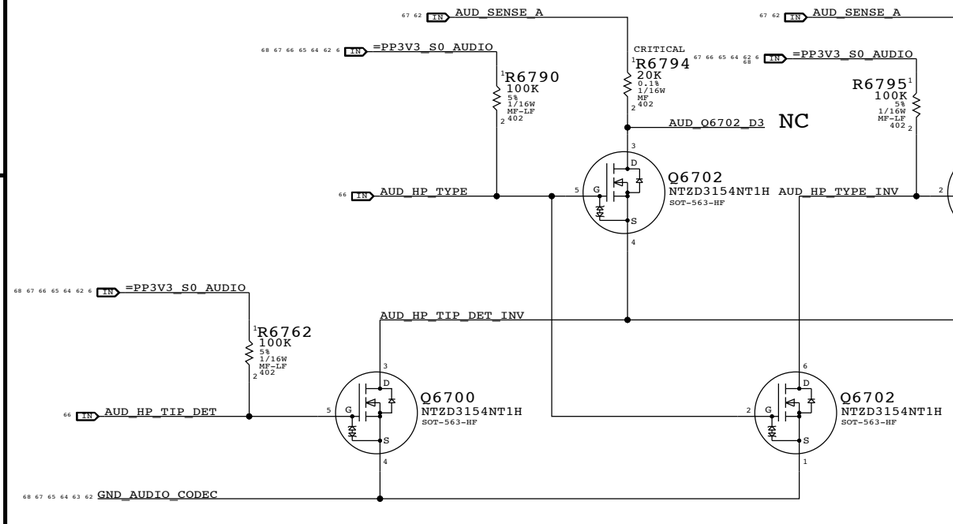
IPHS HS DETECT DEBOUNCE CKT



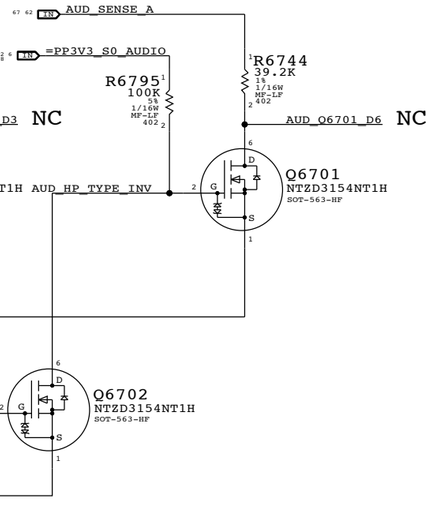
PLACE ACROSS GROUND SPLIT



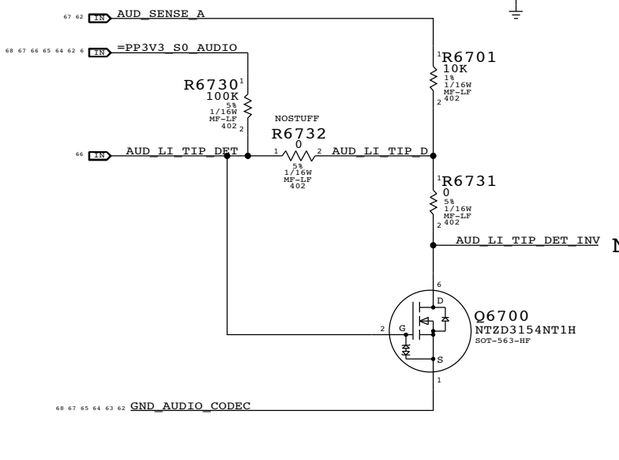
DIGITAL OUT



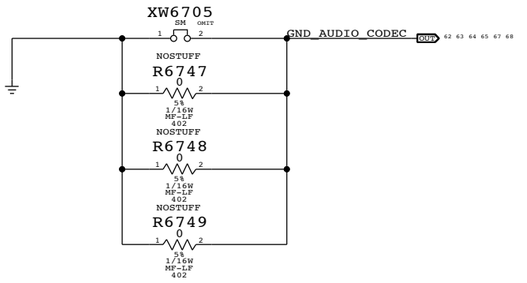
HEADPHONE OUT



LI INSERT DETECT



AUDIO GROUND RETURNS



SYNC MASTER=SKIPAUDIO SYNC DATE=06/01/2009

PAGE TITLE: AUDIO: Detects/Grounding

Apple Inc.

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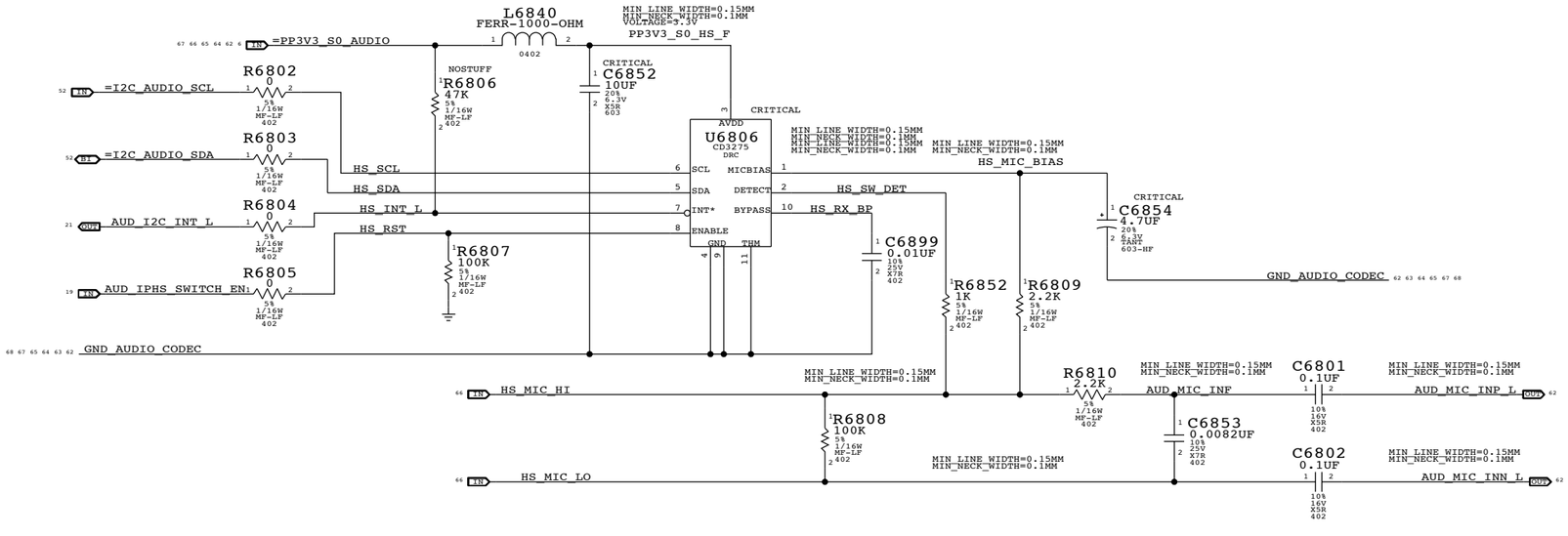
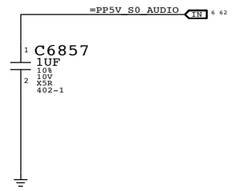
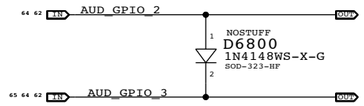
FUNCTION	PIN	CONVERTER	VOLUME	ENABLE/ CNTRL TYPE	DETECT/INTERRUPT
PRIMARY	0X0B	0X04	0X04	GPIO 3	N/A
SECONDARY	0X0A	0X03	0X03	GPIO 3	N/A
HEADPHONES	0X09	0X02	0X02	N/A	0X09 (A)
LINE INPUT	0X0C	0X05	0X05	N/A	LINE IN
BUILT-IN MICROPHONE	0X0D(13,B,RIGHT)	0X06	0X06	MICBIAS 80%	N/A
HEADSET MICROPHONE	0X0D (13,V22,B,LEFT)	0X06	0X06	MIKEY	MIKEY
SPDIF OUT	0X10	0X08	N/A	N/A	0X0C (B)
SPDIF IN	0X0F	0X07	N/A	N/A	N/A
MIKEY	N/A	N/A	N/A	MCP GPIO_38	MCP GPIO_5

MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S2256







FLP = 8.82 KHZ
FHP = 80 HZ

SYNC MASTER=SKIPAUDIO	SYNC DATE=06/01/2009
PAGE TITLE: AUDIO: Mikey	
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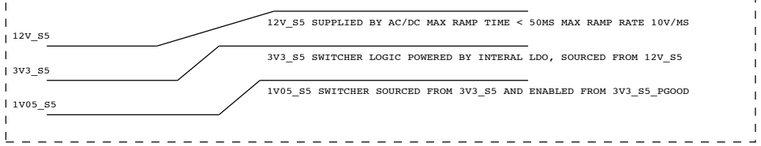
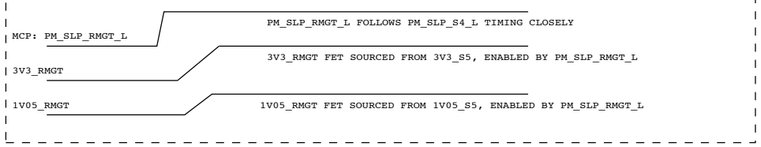
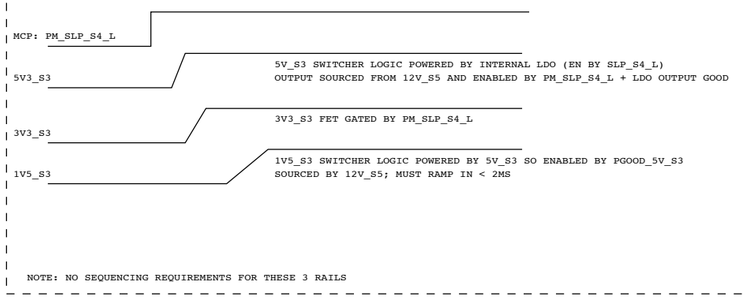
S5 POWER RAIL SEQUENCING



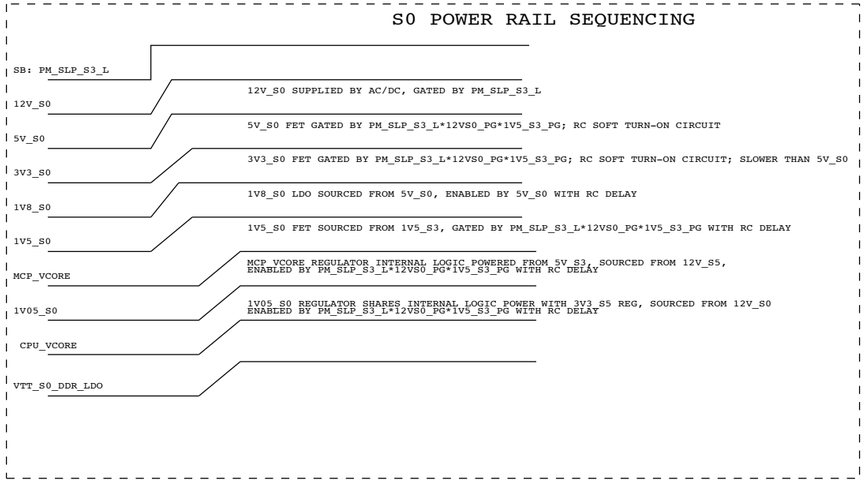
RMGT POWER RAIL SEQUENCING



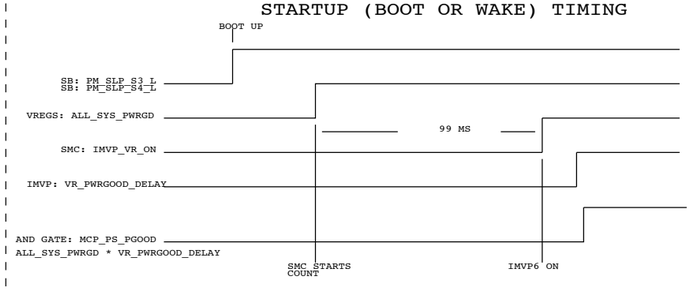
S3 POWER RAIL SEQUENCING



S0 POWER RAIL SEQUENCING

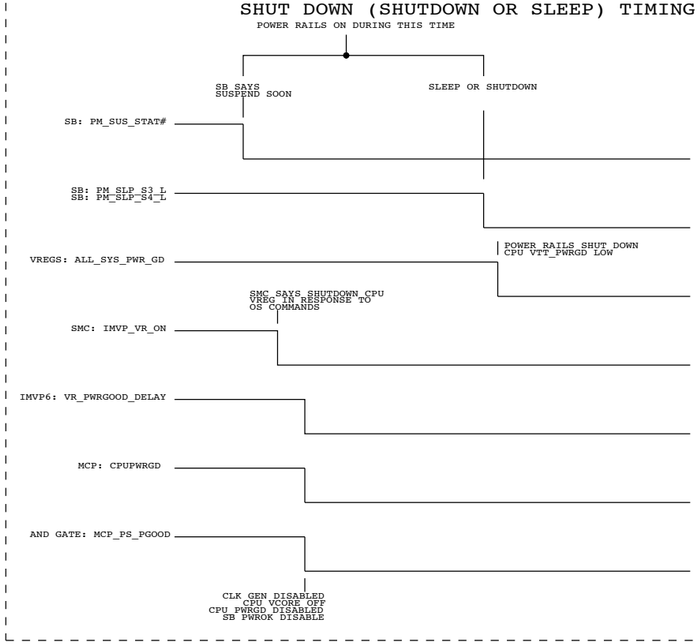


STARTUP (BOOT OR WAKE) TIMING



State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0

SHUT DOWN (SHUTDOWN OR SLEEP) TIMING



SYNC MASTER=K51 SYNC DATE=12/08/2008

PAGE TITLE

POWER SEQUENCING BLOCK DIAGRAM

Apple Inc.

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Power Control Signals
3.3V,5V S3 enable

State	SMC_PM_G2_ENABLE (PORTABLES)	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

R7050 0
PM_SLP_RMGT_L (21) → ENET_EN (38)

FROM MCP (6)
PM_SLP_S4_L (102 21) → R7051 33 (PM_S4_STATE_L)
NOSTUFF
PLACEMENT_NOTE=Place close to U1400

R7052 33 → P3V3S3_EN (78) Enable FET
R7053 33 → 5VREG_EN (73) ENABLE REGULATOR
R7054 33 → PM_SLP_S4_SMC_L (49 50) To SMC
PLACEMENT_NOTE=Place close to U1400

=PP5V_S3_PWRCTL (6) → R7072 100K → PGOOD_5V_S3 (70)
MAKE_BASE=TRUE
PGOOD_5V_S3 (70) → =DDRREG_EN (75) Enable regulator
PGOOD_5V_S3 (70) → PM_EN_USB_PWR (46) USB Port Switch

MXM POWER SEQUENCE

=PM_MXM_PGOOD_PULLUP (85) → ALL_SYS_PWRGD_R (6 70)
MAKE_BASE=TRUE
PM_MXM_EN (85)

MXM CARD INPUT POWER ARE 12V_S0, 3V3_S0, 5V_S0
ALL_SYS_PWRGD ENABLES MXM REGULATORS
PM_MXM_PGOOD IS OPEN DRAIN SIGNAL, IT'S PULLED UP TO ALL_SYS_PWRGD

=PP3V3_S5_PWRCTL (6) → C7058 0.1UF
=PP3V3_S5_PWRCTL (6) → R7040 10K
FROM COMPARATOR PGOOD_1V5_S3 (78)
FROM COMPARATOR PGOOD_12V_S0 (70) → S0_RDY
MAKE_BASE=TRUE
U7059 TC7SZ08AFEAPE SOT665
From SMC (6) PM_SLP_S3_BUF2_L (50 49 9 6) → (PM_SLP_S3_L)
(PM_SLP_S3_L_BUF) → PM_SLP_S3_L_AND_S0_RDY

R7085 33 → P5VS0_EN → =P5VS0_EN (78) Enable FET
MAKE_BASE=TRUE
PLACEMENT_NOTE=Place close to U7059

PM_SLP_S3_L_AND_S0_RDY → R7080 39K, R7081 43K, R7082 10K, R7083 2.2K

P3V3S0_EN → =P3V3S0_EN (78) Enable FET
MCPDDR_EN → =MCPDDR_EN (78) Enable FET DELAY OF ~15MS FROM PM_SLP_S3_L
CPUVTTS0_EN → =PVTT_S0_EN (76) Enable regulator DELAY OF ~18MS FROM PM_SLP_S3_L
MCPCORES0_EN → =MCPCORES0_EN (74) Enable regulator DELAY OF ~16MS FROM PM_SLP_S3_L
MAKE_BASE=TRUE

C7080 0.47UF, C7081 0.47UF, C7082 0.47UF, C7083 0.47UF

1.5V_S3 NEED TO BE ON BEFORE S0 FET ON
12V_S0 NEED TO BE ON BEFORE MCP REG AND 1.05_S0 REG EN

=PP3V3_S5_PWRCTL (6 70) → R7031 1K
PGOOD_1V1_S5 (79) → RSMRST_PWRGD (49) To SMC (2)
1V05V_S0 DERIVES FROM 3.3V_S5
C7031 0.1UF
FROM THIS SMC GENERATES PM_RSMRST_L WHICH GOES INTO PGOOD_SB OF MCP DELAY IS ABOUT 200MS

HYSTERESIS NUMBERS CALCULATED BASED ON OUPTPUT PULL UP OF 3.3V

PGOOD Comparators

=PP12V_S5_PWRCTL (78 38 6)
R7013 33.2K, R7018 84.5K, R7014 100K, R7019 10K
C7010 0.1UF
PLACE SHORTS CLOSE TO PLANE CUTS

PP12V_S0 (6) → XW7000 OMIT → R7000 4.99K → 12VS0_PG_CMP1
(9.91V/9.58V; 330MV HYSTERESIS)
12VS5_9V00_REF, 12VS0_COMP_REF

=PPDDR_S3_PGCMP (6) → XW7001 OMIT → R7001 1.21K → 1V5S3_PG_CMP
(1.30V/1.22V; 80MV HYSTERESIS)
12VS5_1V27_REF, 1V5S3_COMP_REF

CRITICAL
U7010 LM393 SOI-HF
R7007 49.9K, R7008 49.9K
PGOOD_12V_S0 (70)
PGOOD_1V5_S3 (70)

USING COMPARTOR INSTEAD OF REGULATOR PGOOD OUTPUT BECAUSE IF 5V S3 DOES NOT COME UP, PPDDR REGULATOR HAS NO INTERNAL POWER TO PULL PGOOD LOW

(PULLUPS ARE NEAR LOADS)

=PP12V_S0_VRD (71 6)
R7020 64.9K, MXM R7022 100K
(1.679V/1.53V; 132MV HYSTERESIS)
12VS5_1V60_REF
=PP1V8_S0_PGCMP (6) → XW7002 SM OMIT → R7002 2.0K → 1V8S0_PG_CMP
1V8S0_COMP_REF
R7021 10K
CRITICAL
U7030 LM393 SOI-HF
R7006 49.9K
C7025 0.1UF
PGOOD_1V8_S0 (70)

S0 RAILS PGOOD

=PP3V3_S5_PWRCTL (6 70) → R7033 10K
PGOOD_1V8_S0 (70)
PGOOD_1V5_S0 (78)
PGOOD_5V_S0 (78)
C7020 0.1UF

=PP3V3_S0_PWRCTL (6) → R7030 10K
PGOOD_MCPCORE_S0 (74)
PGOOD_1V05_S0 (71)
S0_PWR_REG_PGOOD
S0_PWR_CMP_PGOOD
U7020 TC7SZ08AFEAPE SOT665
ALL_SYS_PWRGD (4)

PLACE RESISTORS CLOSE TO U7020

R7098 33 → ALL_SYS_PWRGD_SMC (49)
R7099 33 → ALL_SYS_PWRGD_R (6 70)

	I	Rds(on)	Vgs +/-
IRF7410	13A	7mOHM	8V
IRF7413	9.6A	18mOHM	20V
FDS4435	8.8A	35mOHM	25V
IRF7406	5.8A	70mOHM	20V
IRF6402	3.7A	65mOHM	12V
SI2302	1.6A	115mOHM	8V

=PP3V3_S5_PWRCTL (6) → C7056 0.1uF
PM_MXM_PGOOD (85)
PM_PGOOD_PVCORE_CPU (71 11)
U7056 MC74VHC1G08 SOT23-5-HF
MCP_PS_PWRGD (21)

ALL SYS_PWRGD IS ALSO AN INPUT TO THIS AND GATE BY THE FACT THAT PM_MXM_PGOOD IS PULLED UP TO IT

SYNC MASTER=MASTER SYNC_DATE=N/A
PAGE TITLE
PGOOD and Power Sequencing

Apple Inc.
DRAWING NUMBER 051-7845
SIZE D
REVISION A.0.0
BRANCH
PAGE 70 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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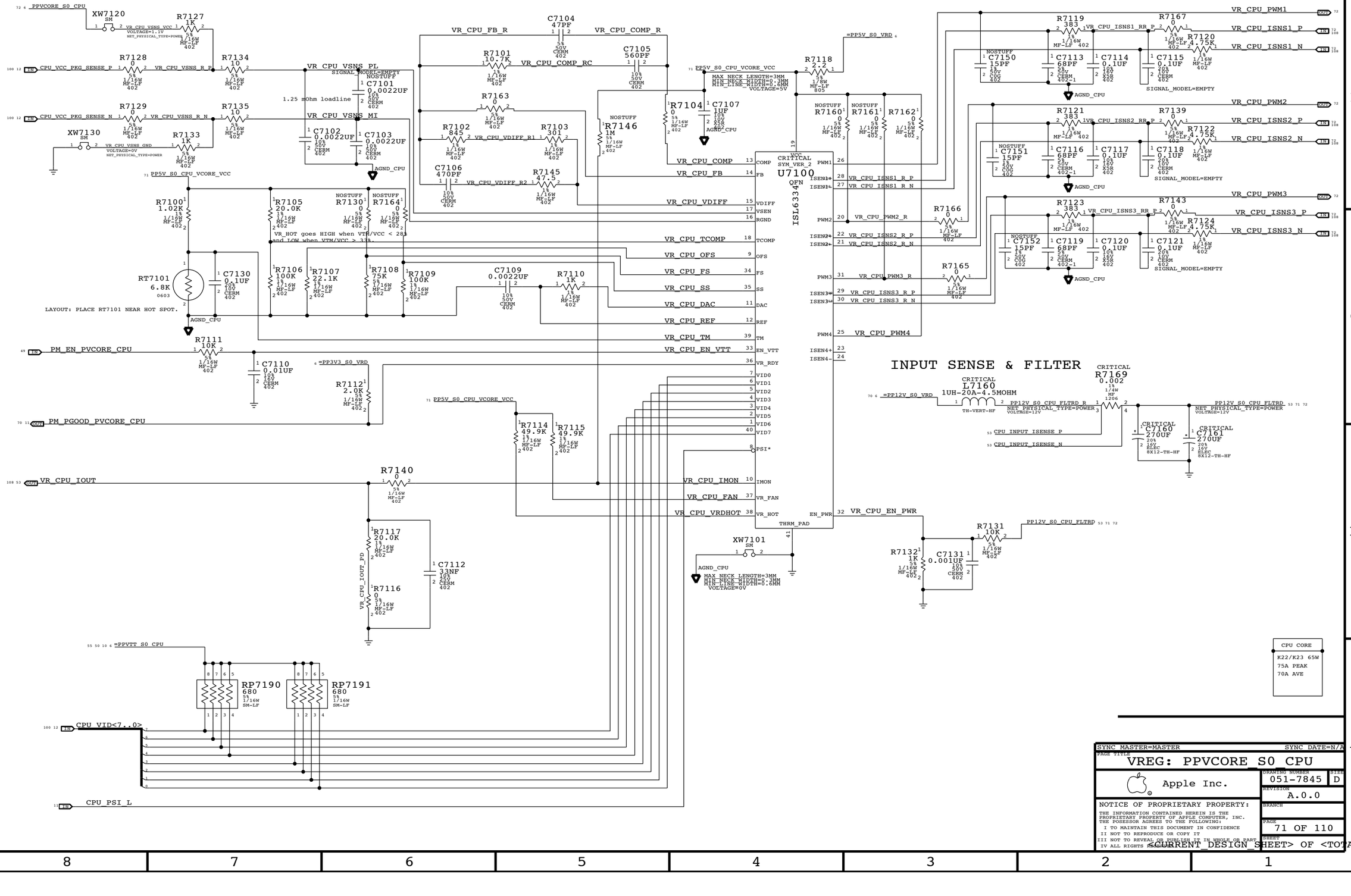

SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE

VREG: PPVCORE_S0_CPU

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DRAWING NUMBER 051-7845 SIZE D

REVISION A.0.0

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PAGE 71 OF 110

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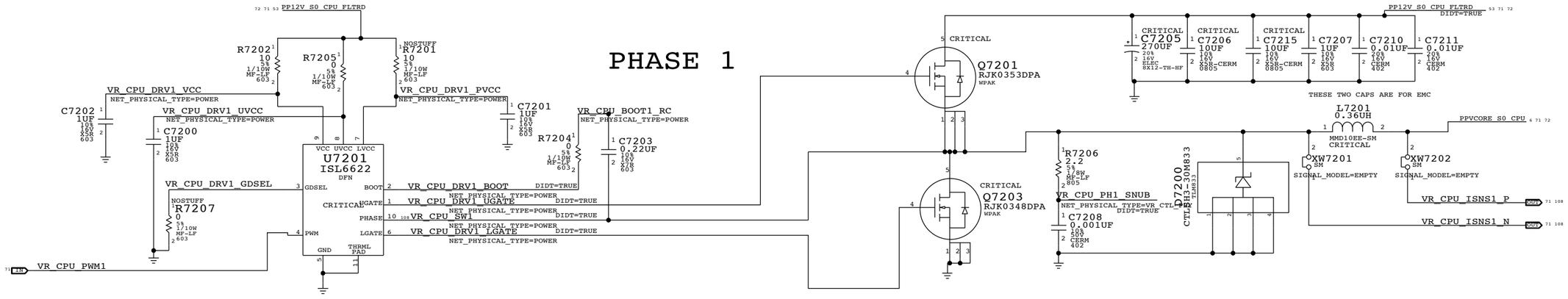
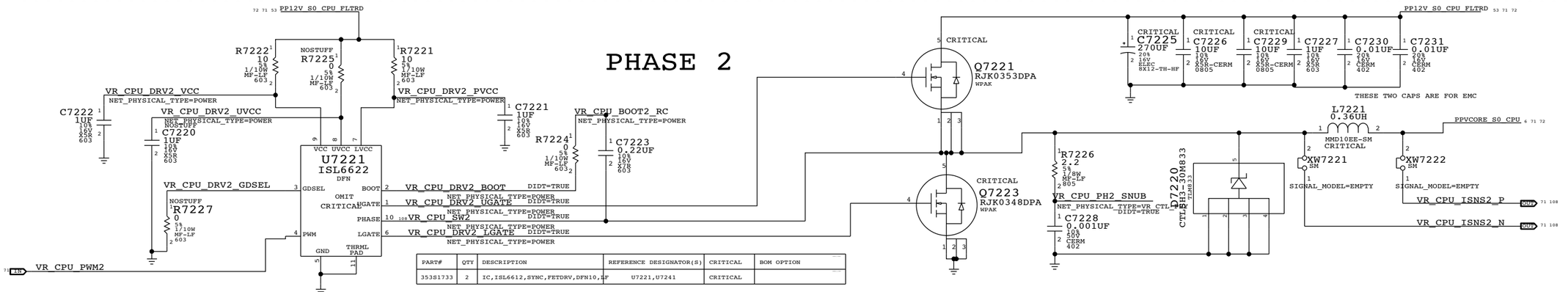
PHASE 1

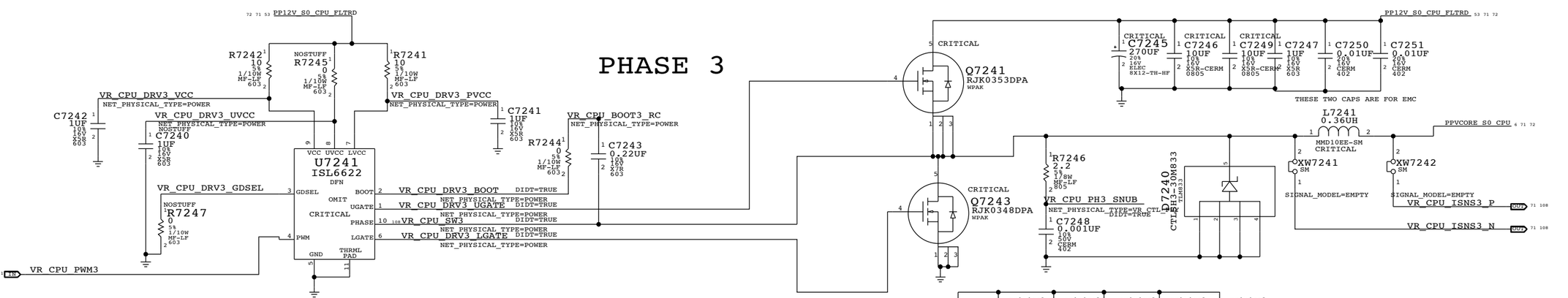


PHASE 2

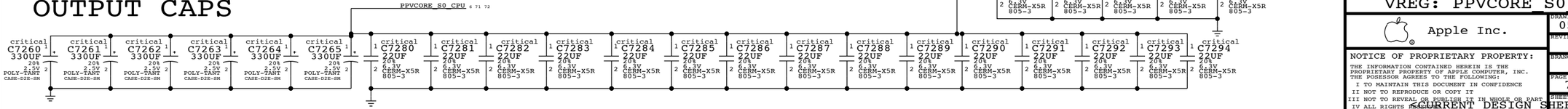


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1733	2	IC,ISL6612,SYNC,FETDRV,DFN10,LF	U7221,U7241	CRITICAL	

PHASE 3



OUTPUT CAPS



SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE

VREG: PPVCORE_S0_CPU

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D

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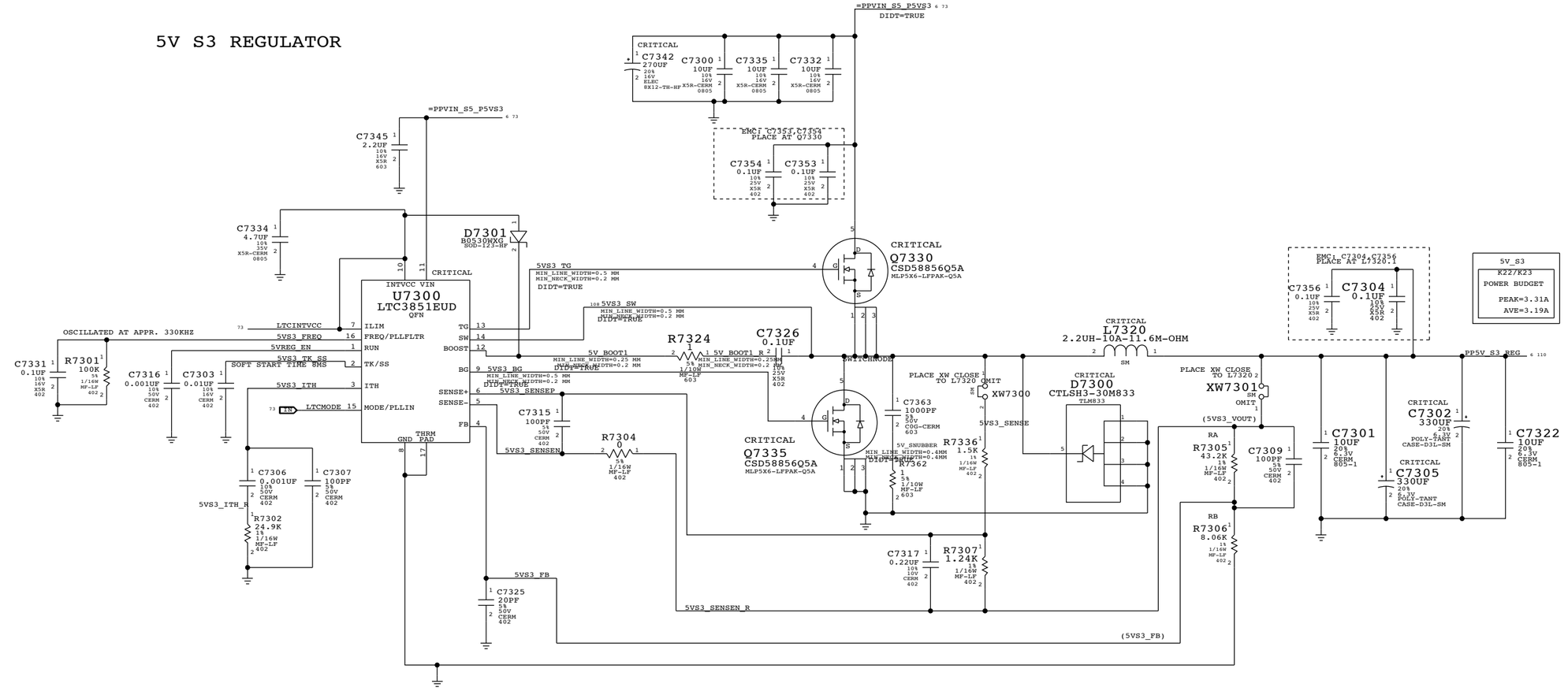
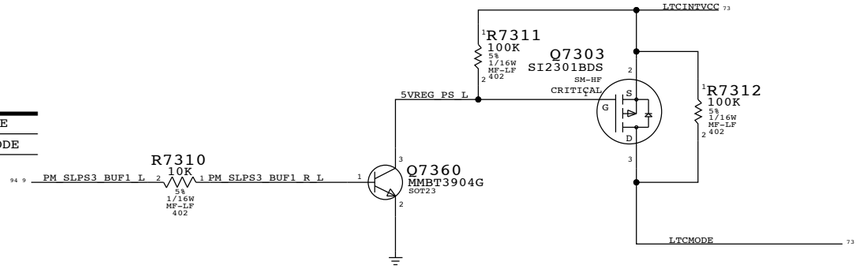
5V S3 REGULATOR





STATE	PM_SLP3_BUF1_L	5VREG_PS_L	LTCMODE	Mode
S0	1	0	1	CONT MODE
S3	0	1	0	BURST MODE

SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE: 5V_S3 REGULATOR

Apple Inc.

DRAWING NUMBER: 051-7845 SIZE: D

REVISION: A.0.0

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PAGE: 73 OF 110

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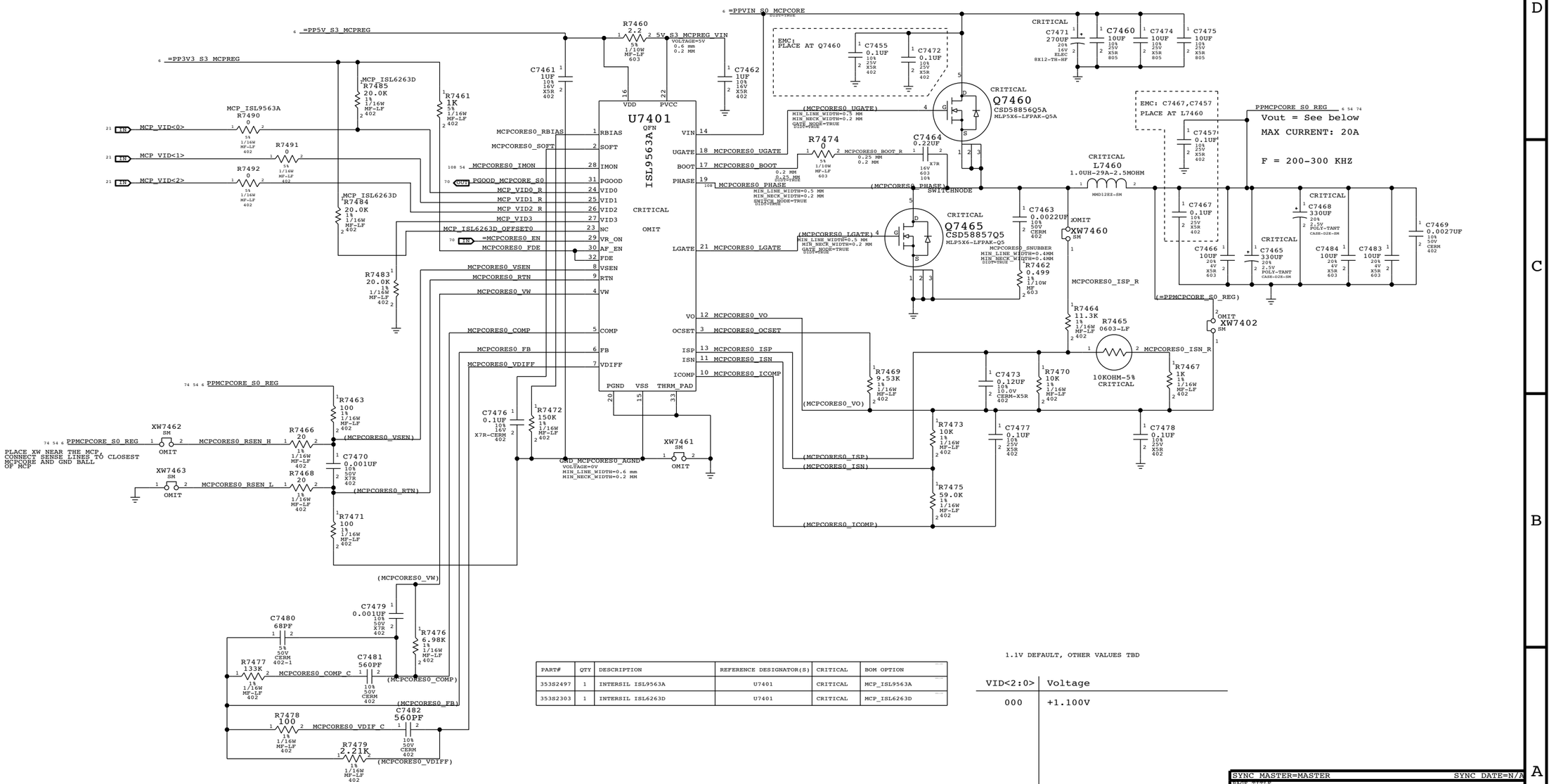
MCP CORE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S2497	1	INTERSIL ISL9563A	U7401	CRITICAL	MCP_ISL9563A
353S2303	1	INTERSIL ISL6263D	U7401	CRITICAL	MCP_ISL6263D

1.1V DEFAULT, OTHER VALUES TBD

VID<2:0>	Voltage
000	+1.100V

SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE: MCP CORE REGULATOR

Apple Inc.

DRAWING NUMBER: 051-7845 SIZE: D

REVISION: A.0.0

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PAGE: 74 OF 110

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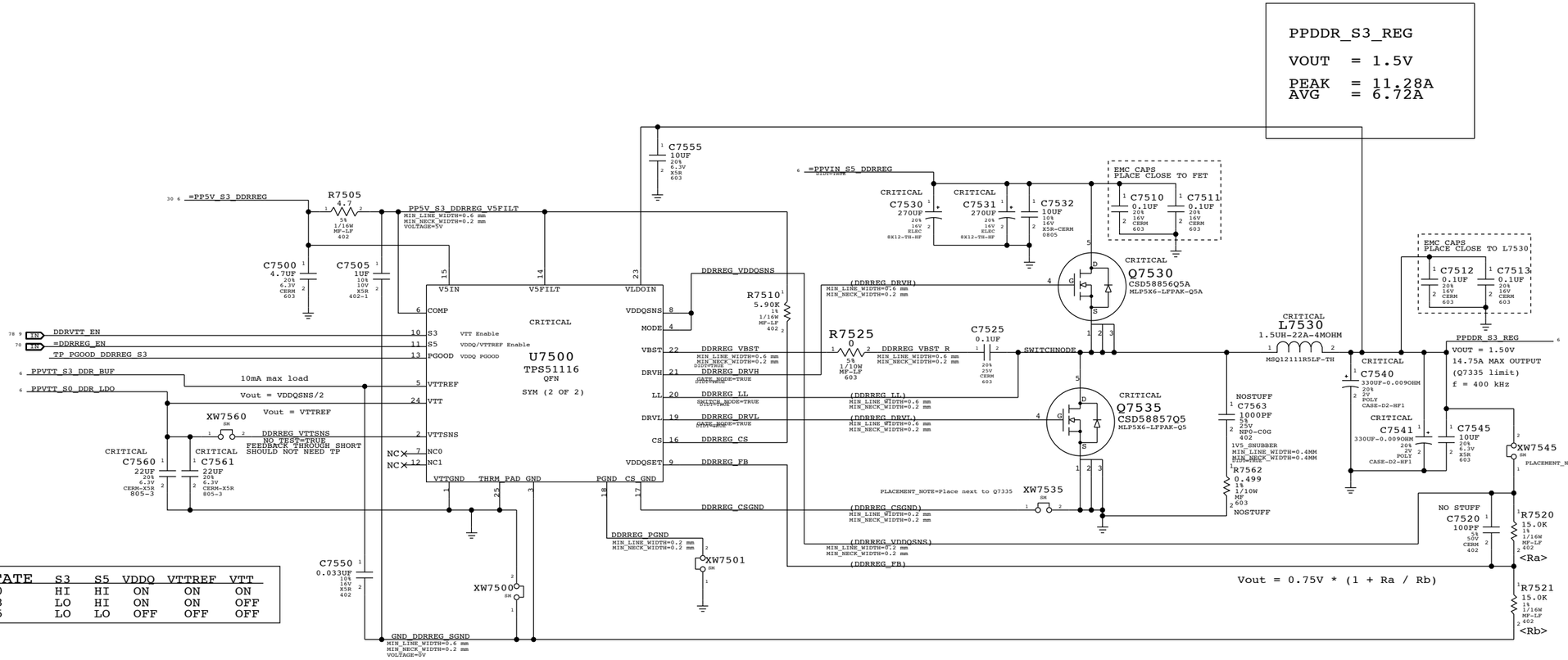
1.5 V DDR SUPPLY

PPDDR_S3_REG
VOUT = 1.5V
PEAK = 11.28A
AVG = 6.72A



STATE	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON
S3	LO	HI	ON	ON	OFF
S5	LO	LO	OFF	OFF	OFF

SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE: 1.5V DDR SUPPLY

Apple Inc.

DRAWING NUMBER: 051-7845 SIZE: D

REVISION: A.0.0

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PAGE: 75 OF 110

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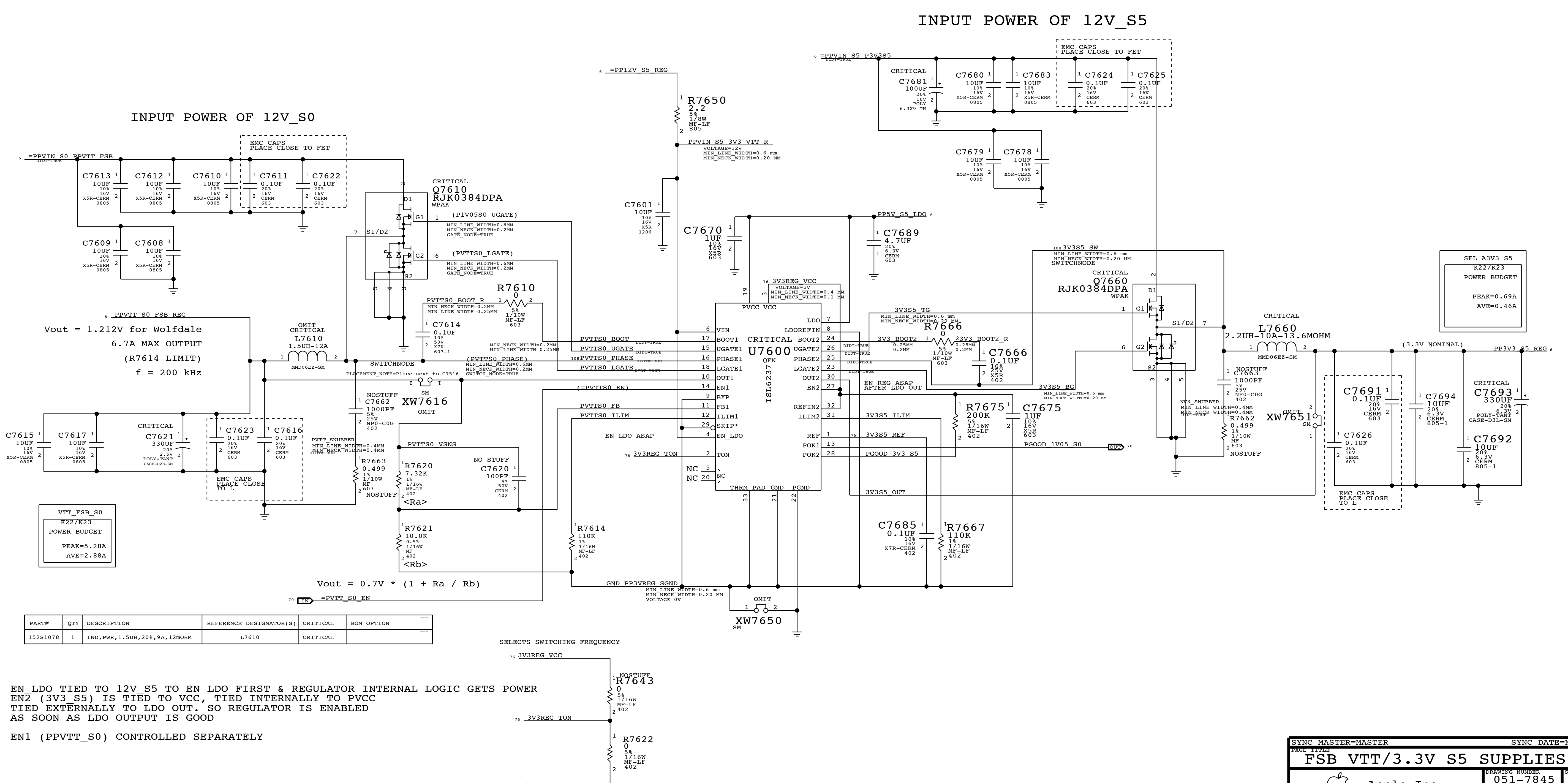
FSB VTT AND 3.3V S5 RAILS



INPUT POWER OF 12V_S5
INPUT POWER OF 12V_S0
=PP12V_S5_REG
R7650 2.2 5% 1/8W MF-LF 805
PPVIN_S5_3V3_VTT_R
=PPVIN_S0_PPVTT_FSB
=PPVIN_S5_P3V3S5
EMC CAPS PLACE CLOSE TO FET
C7613 10UF
C7612 10UF
C7610 10UF
C7611 0.1UF
C7622 0.1UF
C7609 10UF
C7608 10UF
C7681 100UF
C7680 10UF
C7683 10UF
C7624 0.1UF
C7625 0.1UF
C7679 10UF
C7678 10UF
C7601 10UF
CRITICAL Q7610 RJK0384DPA WPAK
CRITICAL Q7660 RJK0384DPA WPAK
C7670 1UF
PP5V_S5_LDO
C7689 4.7UF
3V3REG_VCC
CRITICAL U7600 ISL6237 QFN
VIN BOOT1 UGATE1 PHASE1 LGATE1 OUT1 EN1 BYP FB1 ILIM1 SKIP* EN_LDO TON NC
LDO LDOREFIN UGATE2 BOOT2 PHASE2 LGATE2 OUT2 EN2 REFIN2 ILIM2 REF POK1 POK2
PVCC VCC THRM_PAD GND PGND
PVTTS0_BOOT_R
R7610 0
C7614 0.1UF
PVTTS0_BOOT
PVTTS0_UGATE
PVTTS0_PHASE
PVTTS0_LGATE
PVTTS0_FB
PVTTS0_ILIM
=PPVTT_S0_FSB_REG
Vout = 1.212V for Wolfdale
6.7A MAX OUTPUT
(R7614 LIMIT)
f = 200 kHz
OMIT CRITICAL L7610 1.5UH-12A
SWITCHNODE
XW7616 OMIT
NOSTUFF C7662 1000PF
C7615 10UF
C7617 10UF
CRITICAL C7621 330UF
C7623 0.1UF
C7616 0.1UF
EMC CAPS PLACE CLOSE TO L
PVTT_SNUBBER
R7663 0.499 NOSTUFF
PVTTS0_VSNS
R7620 7.32K <Ra>
NO STUFF C7620 100PF
R7621 10.0K <Rb>
R7614 110K
Vout = 0.7V * (1 + Ra / Rb)
=PVTT_S0_EN
VTT_FSB_S0
K22/K23
POWER BUDGET
PEAK=5.28A
AVE=2.88A
EN LDO ASAP
3V3REG_TON
GND_PP3VREG_SGND
OMIT XW7650 SM
3V3S5_SW
3V3S5_TG
3V3_BOOT2
R7666 0
3V3_BOOT2_R
C7666 0.1UF
EN_REG ASAP AFTER LDO OUT
3V3S5_BG
R7675 200K
C7675 1UF
3V3S5_ILIM
3V3S5_REF
PGOOD_3V3_S5
PGOOD_1V05_S0
3V3S5_OUT
C7685 0.1UF
R7667 110K
CRITICAL L7660 2.2UH-10A-13.6MOHM
NOSTUFF C7663 1000PF
3V3_SNUBBER
R7662 0.499 NOSTUFF
OMIT XW7651 SM
(3.3V NOMINAL)
PP3V3_S5_REG
C7691 0.1UF
C7626 0.1UF
C7694 10UF
CRITICAL C7693 330UF
C7692 10UF
SEL A3V3 S5
K22/K23
POWER BUDGET
PEAK=0.69A
AVE=0.46A
SELECTS SWITCHING FREQUENCY
3V3REG_VCC
NOSTUFF R7643 0
3V3REG_TON
R7622 0
3V3S5_REF

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1078	1	IND,PWR,1.5UH,20%,9A,12mOHM	L7610	CRITICAL	

EN_LDO TIED TO 12V_S5 TO EN LDO FIRST & REGULATOR INTERNAL LOGIC GETS POWER
EN2 (3V3_S5) IS TIED TO VCC, TIED INTERNALLY TO PVCC
TIED EXTERNALLY TO LDO OUT. SO REGULATOR IS ENABLED
AS SOON AS LDO OUTPUT IS GOOD

EN1 (PPVTT_S0) CONTROLLED SEPARATELY

SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE
FSB VTT/3.3V S5 SUPPLIES

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D

REVISION A.0.0

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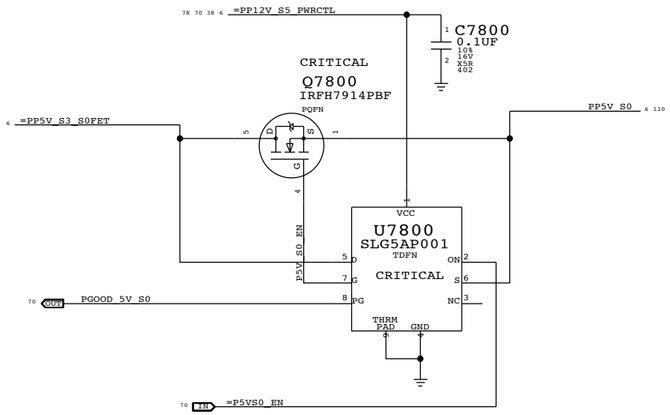
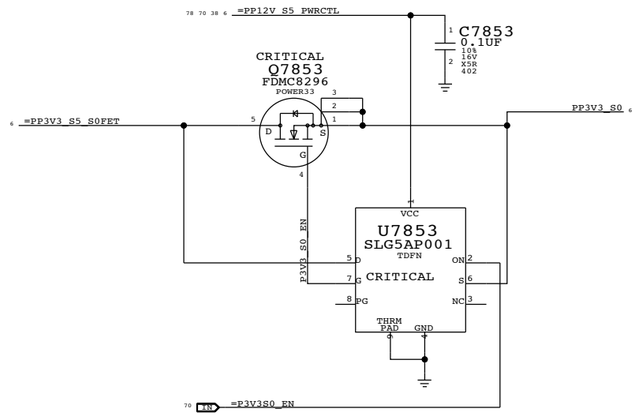
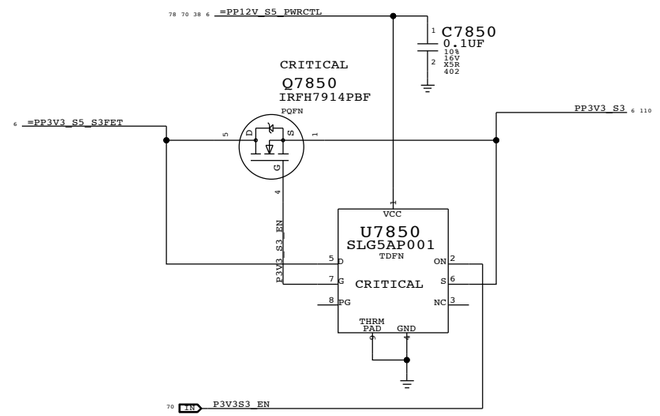
5V S0 FET



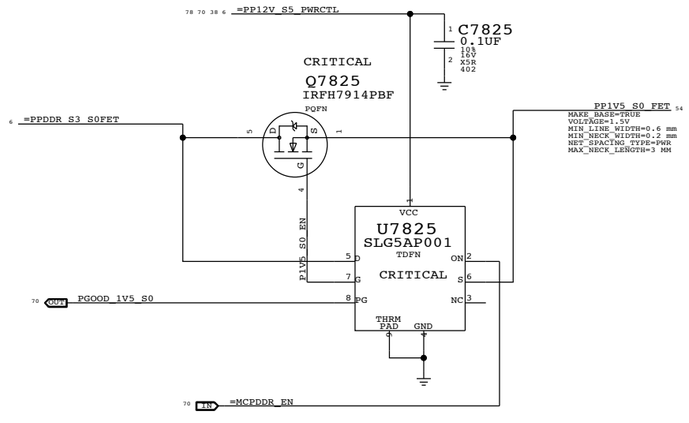
3.3V S0 FET



3.3V S3 FET

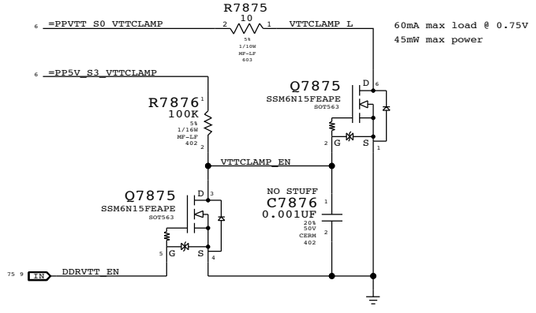


1.5V S0 FET



MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT
NVIDIA RECOMMENDS UNPOWERING DURING SLEEP.
IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE
MUST GUARANTEE MEM_CKE SIGNALS ARE LOW
BEFORE RAIL IS TURNED OFF, AND REMAINS LOW
UNTIL AFTER RAIL TURNS BACK ON OR DIMMS
WILL EXIT SELF-REFRESH PREMATURELY.
MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP
ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS
LOW THROUGH VTT TERMINATION RESISTORS.



SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE

S3 & S0 FETs

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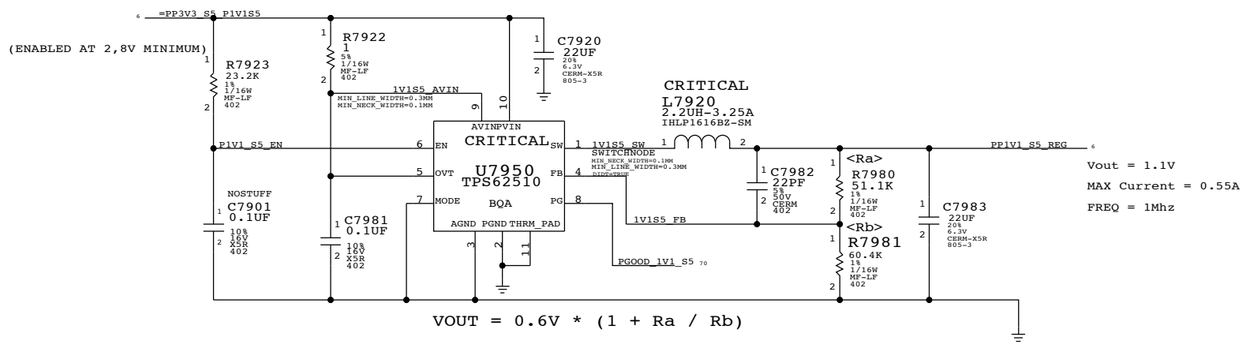
MCP 1.1V_S5 AUXC SUPPLY



SYNC MASTER=K51	SYNC DATE=10/31/2008
PAGE TITLE	1V1 S5 POWER SUPPLY
Apple Inc.	DRAWING NUMBER 051-7845 SIZE D
	REVISION A.0.0
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	PAGE 79 OF 110
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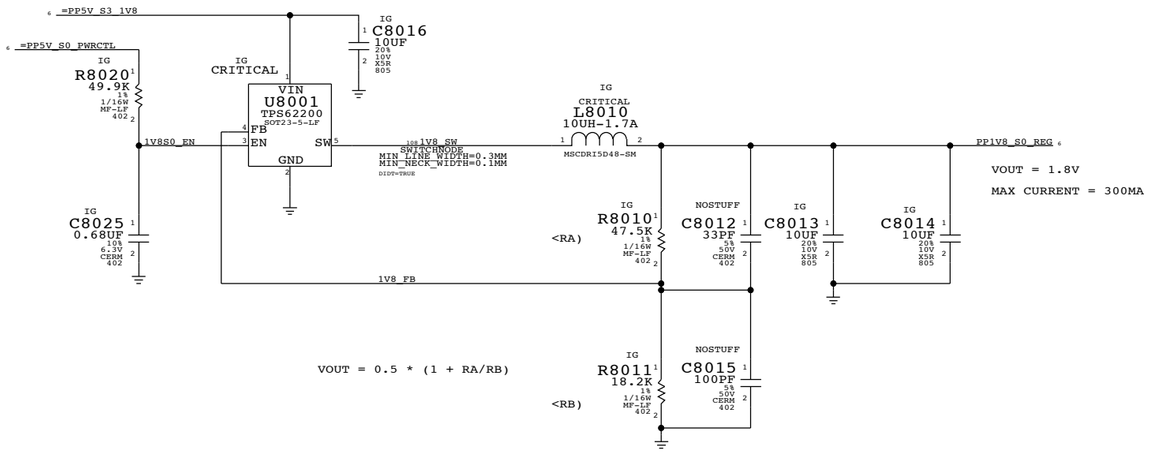
MCP ONLY 1.8V_S0 POWER SUPPLY



SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE

1V8 POWER SUPPLY

Apple Inc.

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PAGE 82 OF 110

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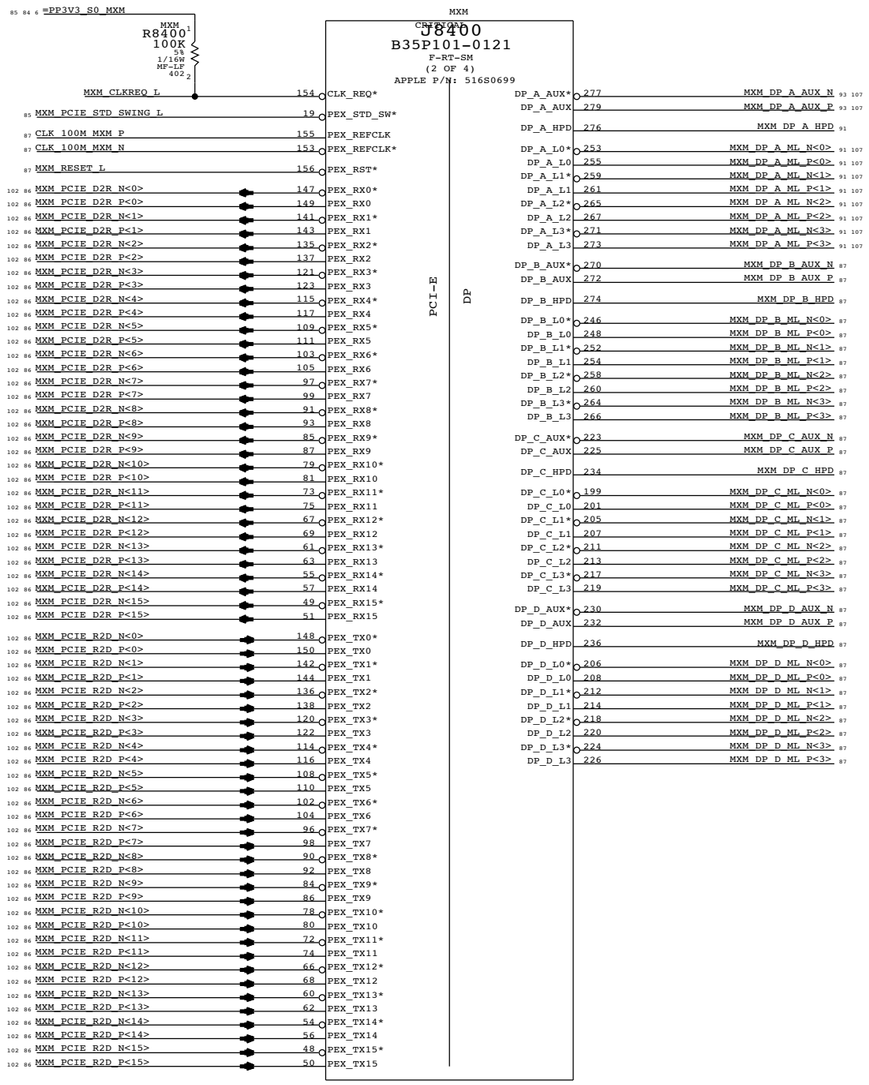
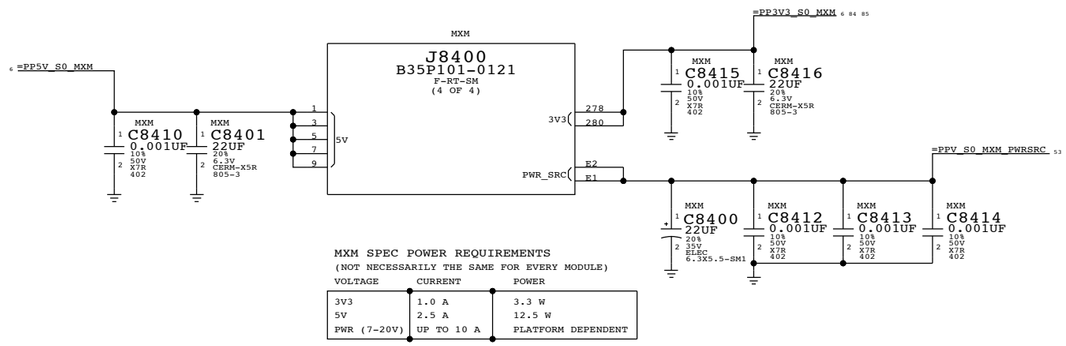
Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP5V_S0_MXM
- =PPV_S0_MXM_PWRSRC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- MXM





MXM SPEC POWER REQUIREMENTS
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.0 A	3.3 W
5V	2.5 A	12.5 W
PWR (7-20V)	UP TO 10 A	PLATFORM DEPENDENT

SYNC MASTER=K51 SYNC DATE=10/31/2008

PAGE TITLE
MXM PCIe, DP & Power

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D
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BRANCH
PAGE 84 OF 110
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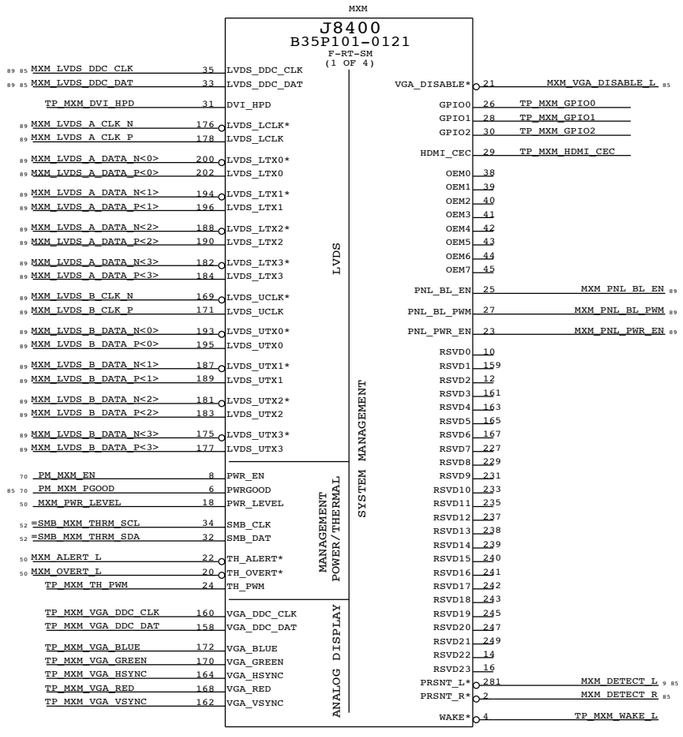
Page Notes

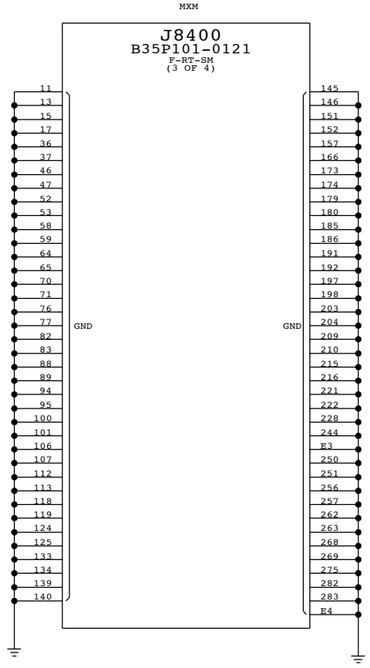
Power aliases required by this page:
- =PP3V3_S0_MXM

Signal aliases required by this page:
- =SMB_MXM_THRM_DATA
- =PM_MXM_PGOOD_PULLUP
- =SMB_MXM_THRM_CLK

BOM options provided by this page:

PULLUPS & PULLDOWNS AT MXM CONNECTOR





FLOAT = NORMAL VGA MODE
GND = SECONDARY DISPLAY CARD

NOSTUFF
R8510
0
MXM_VGA_DISABLE_L
MF-LF 5% 1/16W
402

FLOAT = LOW SWING
GND = HIGH SWING

MXM
R8504
0
MXM_PCIE_STD_SWING_L
MF-LF 5% 1/16W
402

=PP3V3_S0_MXM

R8500
100K
MXM_DETECT_L
MF-LF 5% 1/16W
402

PULLED TO GROUND ON MXM
WE DON'T USE CARD DETECT

R8501
100K
MXM_DETECT_R
MF-LF 5% 1/16W
402

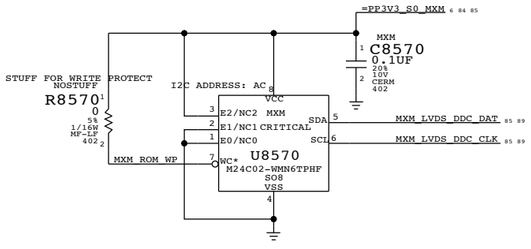
=PM_MXM_PGOOD_PULLUP

SYSTEM INTEGRATOR MUST ALIAS THIS EITHER TO A VOLTAGE RAIL,
OR ANOTHER OPEN-DRAIN PGOOD SIGNAL DEPENDING ON DESIRED BEHAVIOR

R8503
10K
PM_MXM_PGOOD
MF-LF 5% 1/16W
402

MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J7800



SYNC MASTER=K51	SYNC DATE=10/31/2008
PAGE TITLE	MXM I/O
Apple Inc.	DRAWING NUMBER 051-7845 SIZE D
	REVISION A.0.0
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	PAGE 85 OF 110
	SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

MXM TX CAPS

102 9	IN	PEG_R2D_C_N<0>	MXM C8600	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<15>	OUT 84 102
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102 9	IN	PEG_R2D_C_P<1>	MXM C8602	0.1UF	2 10% 16V X5R 402	MXM_PCIE_R2D_P<14>	OUT 84 102
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MXM RX CAPS

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SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE

MXM PCIE CAPS

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D

REVISION A.0.0

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Page Notes

Power aliases required by this page:
- =PP5V_DP_AUX

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

MCP CONNECTIONS

84 CLK_100M_MXM_P — GPU_CLK100M_PCIE_P 9 102
MAKE_BASE=TRUE
84 CLK_100M_MXM_N — GPU_CLK100M_PCIE_N 9 102
MAKE_BASE=TRUE

84 MXM_RESET_L — PEG_RESET_L 9 90
MAKE_BASE=TRUE

UNUSED DP INTERFACES

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84 MXM_DP_C_ML_P<0..3> — NC_MXM_DP_C_ML_P<0..3>
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84 MXM_DP_C_AUX_N — NC_MXM_DP_C_AUX_N
MAKE_BASE=TRUE
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84 MXM_DP_C_AUX_P — NC_MXM_DP_C_AUX_P
MAKE_BASE=TRUE
NO_TEST=TRUE
84 MXM_DP_C_HPD — TP_MXM_DP_C_HPD
MAKE_BASE=TRUE

84 MXM_DP_B_ML_N<0..3> — NC_MXM_DP_B_ML_N<0..3>
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84 MXM_DP_B_ML_P<0..3> — NC_MXM_DP_B_ML_P<0..3>
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84 MXM_DP_B_AUX_N — NC_MXM_DP_B_AUX_N
MAKE_BASE=TRUE
NO_TEST=TRUE
84 MXM_DP_B_AUX_P — NC_MXM_DP_B_AUX_P
MAKE_BASE=TRUE
NO_TEST=TRUE
84 MXM_DP_B_HPD — TP_MXM_DP_B_HPD
MAKE_BASE=TRUE

84 MXM_DP_D_ML_N<0..3> — NC_MXM_DP_D_ML_N<0..3>
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84 MXM_DP_D_ML_P<0..3> — NC_MXM_DP_D_ML_P<0..3>
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84 MXM_DP_D_HPD — TP_MXM_DP_D_HPD
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SYNC_MASTER=MASTER SYNC_DATE=N/A
PAGE TITLE
MXM ALIASES

Apple Inc.

DRAWING NUMBER 051-7845 SIZE D
REVISION A.0.0
BRANCH
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SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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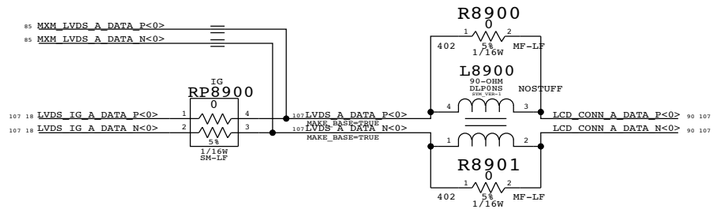
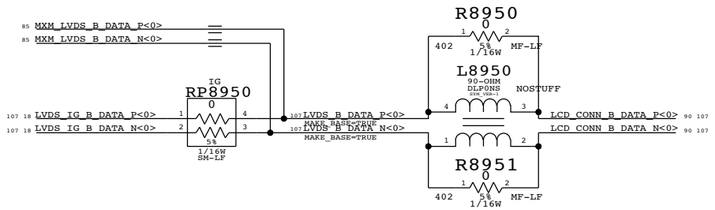
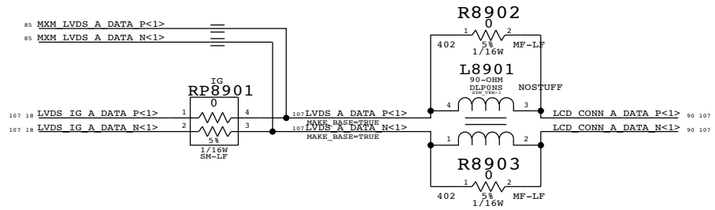
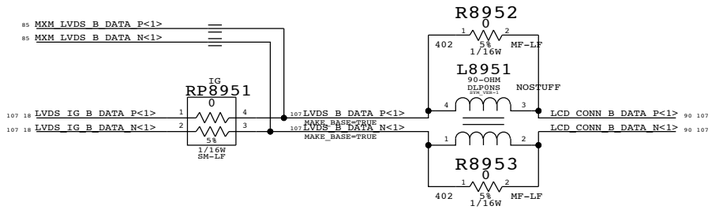
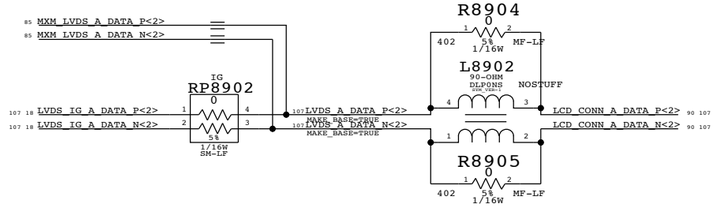
PLACE CHOKES CLOSE TO J9002
SHARE 0-OHM RES WITH CHOKE PADS

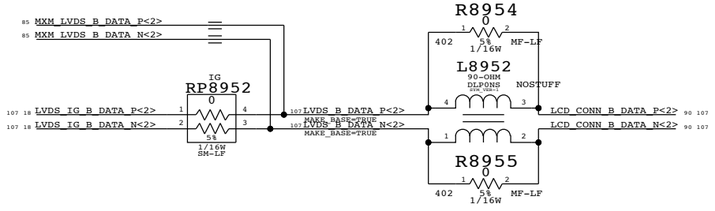


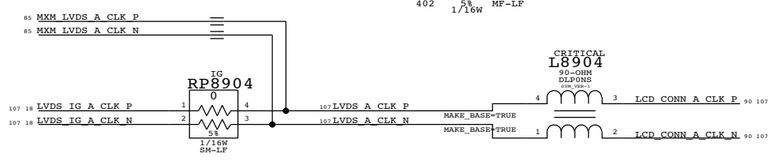


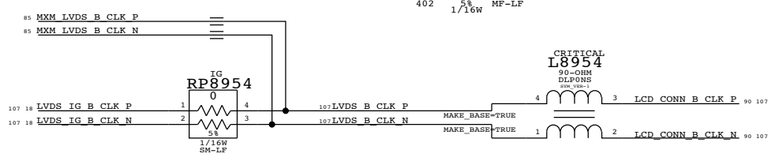


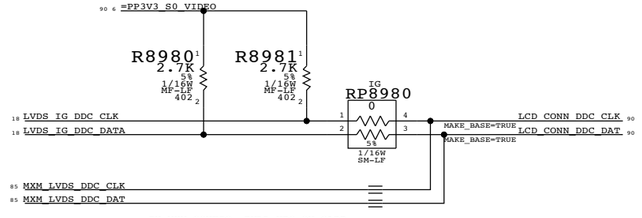




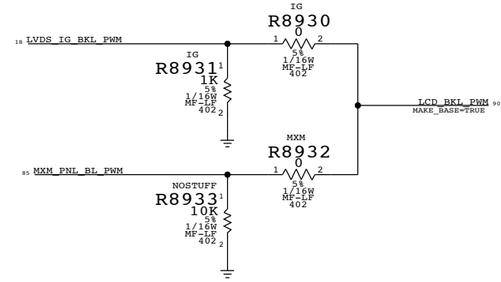


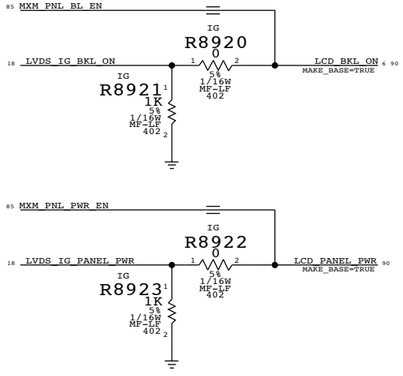






IN MXM CONFIG, PULL-UPS ON CARD
IG pullups always stuffed to prevent floating inputs





THESE RESISTOR OPTIONS SELECT BETWEEN MCP AND MXM TO DRIVE THE INTERNAL DISPLAY

IG-ONLY 0-OHM RESISTORS NEED TO BE PLACED AT THE MXM CONNECTOR TO AVOID STUBS
WE WILL ROUTE FROM MCP TO THE 0-OHM RESISTORS, THEN ON THROUGH MXM TO THE LCD CONNECTOR

IF THIS ROUTING IS NOT FEASIBLE, MXM ALIASES WILL BE REPLACED WITH ADDITIONAL 0-OHM RESISTORS

SYNC MASTER=MASTER SYNC DATE=MASTER

PAGE TITLE
LCD MUX & CHOKES

Apple Inc.

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Page Notes

Power aliases required by this page:

- =PP12V_S0_LCD
- =PP3V3_S0_VIDEO

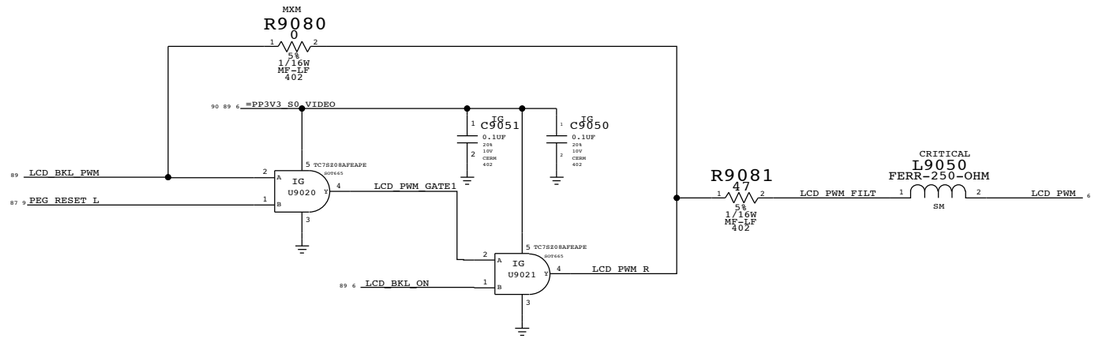
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
IG, MXM

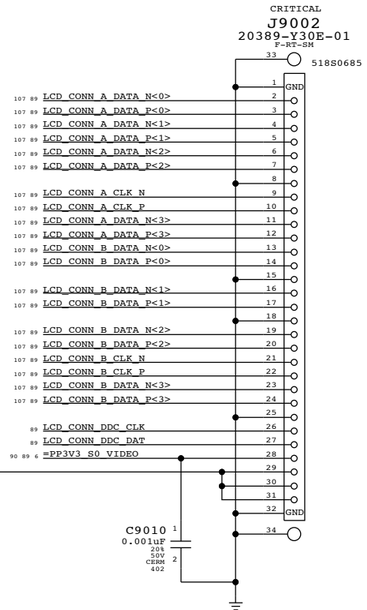
BACKLIGHT CONTROL SUPPORT

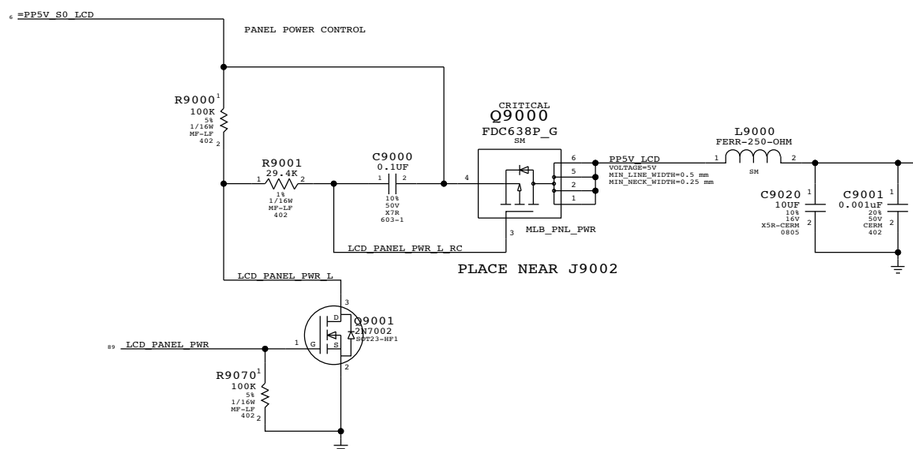
THIS AND GATE CIRCUIT PROVIDES BACKLIGHT GLITCH PREVENTION WHEN MCP GLITCHES GPIOS ON POWERUP
IT MAY BE BYPASSED IF THE PWM SOURCE IS THE MXM

IF NOT BYPASSED, THIS CAN BE USED TO FORCE THE USE OF THE BACKLIGHT ENABLE SIGNAL EVEN IF THE INVERTER DOES NOT TAKE THIS AS AN INPUT



INTERNAL LCD INTERFACE





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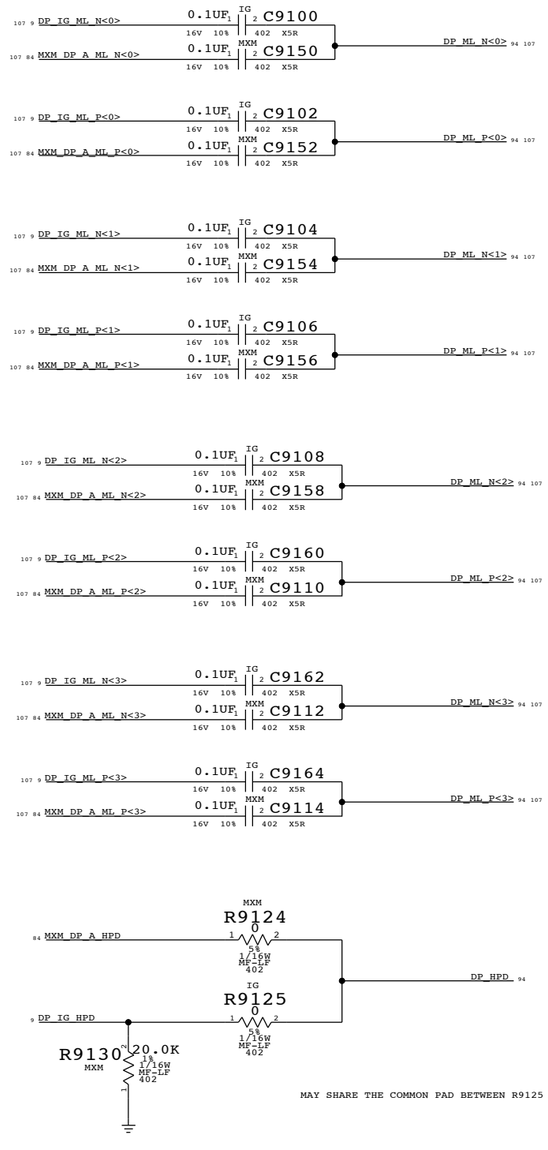
K50 NOTE: PLACE THESE CAPACITORS ATLEAST 1INCH AWAY FROM DP CONNECTOR

DCOX: PLACE AT MXM CONNECTOR IF THERE IS ROOM



MAY SHARE THE COMMON PAD BETWEEN R9125 AND R9130

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DP MUX SUPPORT

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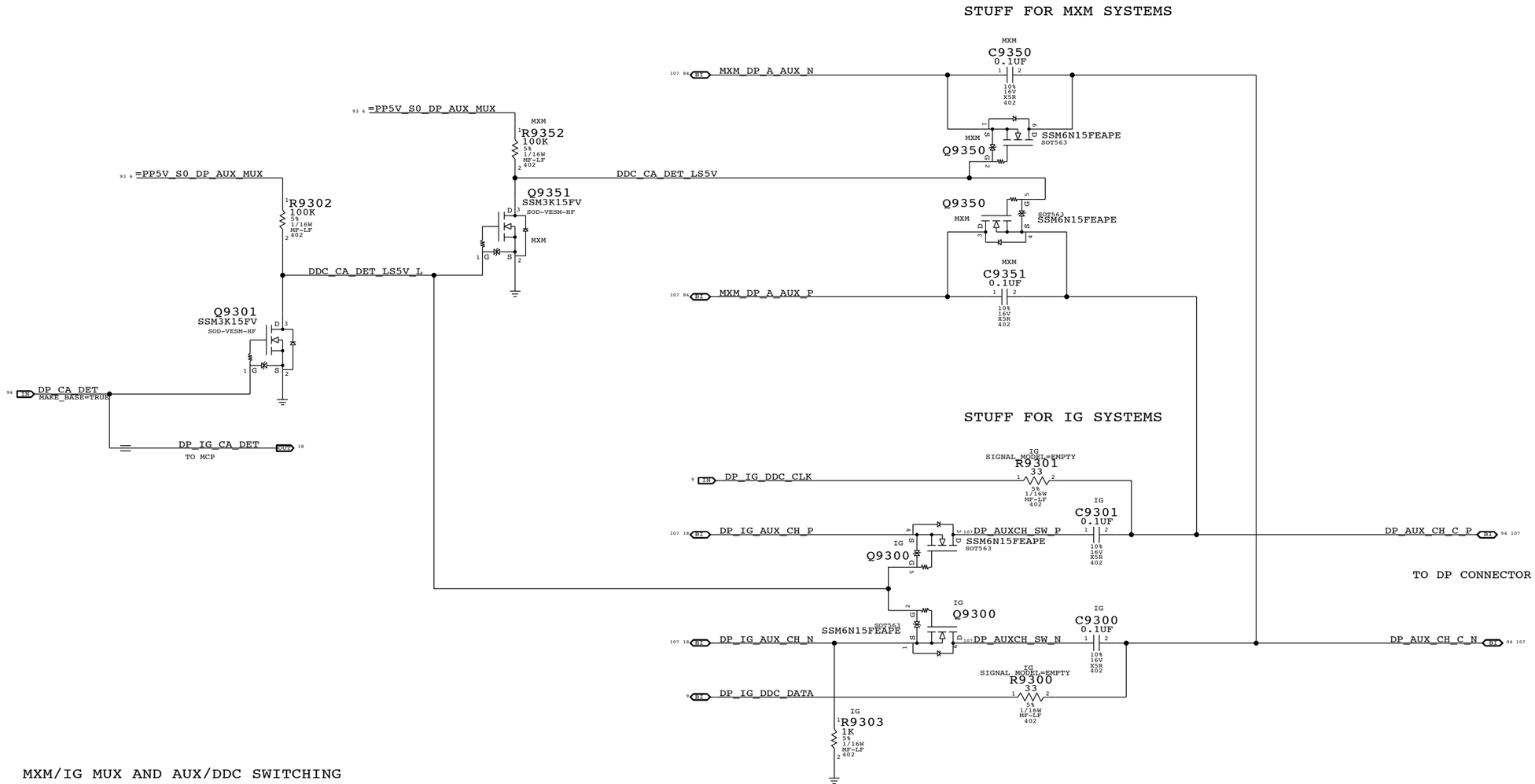

MXM/IG MUX AND AUX/DDC SWITCHING

FOR MXM, Q9350 BYPASSES THE AC COUPLING CAPS
THE CARD IS RESPONSIBLE FOR SWITCHING DDC SIGNALS ONTO THE AUX PAIR

FOR IG SYSTEMS, Q9300 SWITCHES BETWEEN AC COUPLED AUX
AND DC-COUPLED DDC

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DISPLAYPORT SUPPORT

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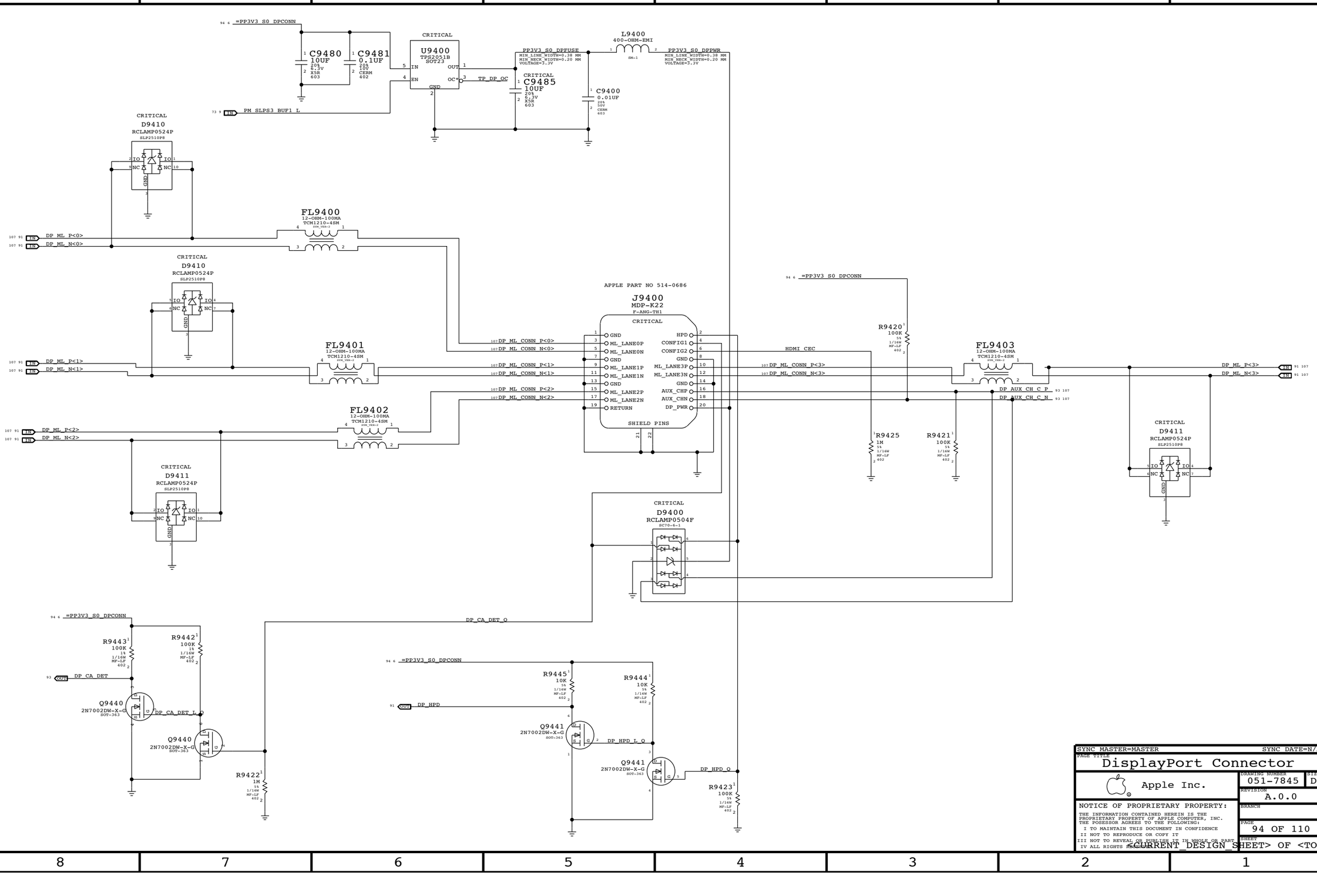

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DisplayPort Connector

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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_42S	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_42S	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 2x/1x/Async FSB signals with impedance requirements are 50-ohm single-ended.
All 4x FSB signals with impedance requirements are 42-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 90 ps. (Tighther than MCP79)
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.175 MM	0.175 MM

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_SMIL	*	0.2 MM	?
CPU_COMP	*	0.6 MM	?
CPU_GTLREF	*	0.6 MM	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	0.6 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

MOST CPU SIGNALS WITH IMPEDANCE REQUIREMENTS ARE 50-OHM SINGLE-ENDED.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB 4X Signal Groups	Group 0	FSB_42S	FSB_DATA	FSB_D_L<15..0>	10 14
		FSB_42S	FSB_DATA	FSB_DINV_L<0>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_P<0>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_N<0>	10 14
	Group 1	FSB_42S	FSB_DATA	FSB_D_L<31..16>	10 14
		FSB_42S	FSB_DATA	FSB_DINV_L<1>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_P<1>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_N<1>	10 14
	Group 2	FSB_42S	FSB_DATA	FSB_D_L<47..32>	10 14
		FSB_42S	FSB_DATA	FSB_DINV_L<2>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_P<2>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_N<2>	10 14
	Group 3	FSB_42S	FSB_DATA	FSB_D_L<63..48>	10 14
		FSB_42S	FSB_DATA	FSB_DINV_L<3>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_P<3>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_N<3>	10 14
FSB 2X Signals	Group 0	FSB_50S	FSB_ADDR	FSB_A_L<16..3>	10 14
		FSB_50S	FSB_ADDR	FSB_REQ_L<4..0>	10 14
		FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0>	10 14
	Group 1	FSB_50S	FSB_ADDR	FSB_A_L<35..17>	10 14
		FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1>	10 14
FSB 1X Signals		FSB_50S	FSB_1X	FSB_ADS_L	10 14
		FSB_50S	FSB_1X	FSB_BREQ0_L	10 14
		FSB_50S	FSB_1X	FSB_BREQ1_L	14
		FSB_50S	FSB_1X	FSB_BNR_L	10 14
		FSB_50S	FSB_1X	FSB_BPRI_L	10 14
		FSB_50S	FSB_1X	FSB_DBSY_L	10 14
		FSB_50S	FSB_1X	FSB_DEFER_L	10 14
		FSB_50S	FSB_1X	FSB_DRDY_L	10 14
		FSB_50S	FSB_1X	FSB_HIT_L	10 14
		FSB_50S	FSB_1X	FSB_HITM_L	10 14
		FSB_50S	FSB_1X	FSB_LOCK_L	10 14
		FSB_50S	FSB_1X	FSB_CPURST_L	10 13 14
		FSB_50S	FSB_1X	FSB_RS_L<2..0>	10 14
		FSB_50S	FSB_1X	FSB_TRDY_L	10 14
		CPU_50S	CPU_AGTL	CPU_A20M_L	10 14
		CPU_50S	CPU_AGTL	CPU_BSEL<2..0>	11 14
		CPU_50S	CPU_SMIL	CPU_FERR_L	10 14
		CPU_50S	CPU_AGTL	CPU_IGNNE_L	10 14
		CPU_50S	CPU_AGTL	CPU_INIT_L	10 14
		CPU_50S	CPU_AGTL	CPU_INTR	10 14
		CPU_50S	CPU_AGTL	CPU_NMI	10 14
		CPU_50S	CPU_AGTL	CPU_PROCHOT_L	11 14 50
		CPU_50S	CPU_AGTL	CPU_PWRGD	11 13 14
		CPU_50S	CPU_AGTL	CPU_SMI_L	10 14
		CPU_50S	CPU_AGTL	CPU_STPCLK_L	10 14
		CPU_50S	CPU_SMIL	PM_THRMTRIP_L	11 14 50
		CPU_50S	CPU_AGTL	FSB_CPUSLP_L	11 14
		CPU_50S	CPU_AGTL	CPU_DPSLP_L	11 14
		CPU_50S	CPU_AGTL	CPU_DPRSTP_L	11 14
		MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	14
		MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	14
		MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	14
		MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	14
		CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	10 14
		CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	10 14
		CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	13 14
		CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	13 14
		CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	14
		CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	14
		CPU_50S	CPU_AGTL	CPU_IERR_L	10
		CPU_50S	CPU_GTLREF	CPU_GTLREF0	10 11 29
		CPU_50S	CPU_GTLREF	CPU_GTLREF1	10 11 29
		CPU_27P4S	CPU_COMP	CPU_COMP<8>	11
		CPU_27P4S	CPU_COMP	CPU_COMP<3>	11
		CPU_27P4S	CPU_COMP	CPU_COMP<2>	11
		CPU_27P4S	CPU_COMP	CPU_COMP<1>	11
		CPU_27P4S	CPU_COMP	CPU_COMP<0>	11
		CPU_50S	CPU_ITP	CPU_XDP_TDI	11 13
		CPU_50S	CPU_ITP	CPU_XDP_TDO	11 13
		CPU_50S	CPU_ITP	CPU_XDP_TMS	11 13
		CPU_50S	CPU_ITP	CPU_XDP_TCK	11 13
		CPU_50S	CPU_ITP	CPU_XDP_TRST_L	11 13
		CPU_50S	CPU_ITP	CPU_XDP_BPM_L<5..0>	11 13
		CPU_50S	CPU_ITP	CPU_XDP_BPMB<3..0>	11 13
		CPU_50S	CPU_ITP	XDP_CPURST_L	13
		CPU_50S	CPU_SMIL	CPU_VID<7..0>	12 71
		CPU_27P4S	CPU_VCCSENSE	CPU_VCC_PKG_SENSE_P	12 71
		CPU_27P4S	CPU_VCCSENSE	CPU_VCC_PKG_SENSE_N	12 71
		CPU_27P4S	CPU_VCCSENSE	VR_CPU_VSNS_R_P	71
		CPU_27P4S	CPU_VCCSENSE	VR_CPU_VSNS_R_N	71

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CPU/FSB Constraints

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	=3:1_SPACING	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:
DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:
DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	0.175 MM	0.175 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_70D_VDD	MEM_CLK	MEM_CLK	MEM_A_CLK_P<1..0>	15 33
MEM_70D_VDD	MEM_CLK	MEM_CLK	MEM_A_CLK_N<1..0>	15 33
MEM_70D_VDD	MEM_CLK	MEM_CLK	MEM_A_CLK_P<4..3>	16 33
MEM_70D_VDD	MEM_CLK	MEM_CLK	MEM_A_CLK_N<4..3>	16 33
MEM_40S_VDD	MEM_CTRL	MEM_CTRL	MEM_A_CKE<3..0>	15 16 31
MEM_40S_VDD	MEM_CTRL	MEM_CTRL	MEM_A_CS_L<3..0>	15 16 31
MEM_40S_VDD	MEM_CTRL	MEM_CTRL	MEM_A_ODT<3..0>	15 16 31
MEM_40S_VDD	MEM_CMD	MEM_CMD	MEM_A_A<14..0>	15 31
MEM_40S_VDD	MEM_CMD	MEM_CMD	MEM_A_BA<2..0>	15 31
MEM_40S_VDD	MEM_CMD	MEM_CMD	MEM_A_RAS_L	15 31
MEM_40S_VDD	MEM_CMD	MEM_CMD	MEM_A_CAS_L	15 31
MEM_40S_VDD	MEM_CMD	MEM_CMD	MEM_A_WE_L	15 31
MEM_40S	MEM_DATA	MEM_DATA	MEM_A_DQ<7..0>	15 33
MEM_40S	MEM_DATA	MEM_DATA	MEM_A_DM<0>	15 33
MEM_40S	MEM_DATA	MEM_DATA	MEM_A_DQ<15..8>	15 33
MEM_40S	MEM_DATA	MEM_DATA	MEM_A_DM<1>	15 33
MEM_40S	MEM_DATA	MEM_DATA	MEM_A_DQ<23..16>	15 33
MEM_40S	MEM_DATA	MEM_DATA	MEM_A_DM<2>	15 33
MEM_40S	MEM_DATA	MEM_DATA	MEM_A_DQ<31..24>	15 33
MEM_40S	MEM_DATA	MEM_DATA	MEM_A_DM<3>	15 33
MEM_40S	MEM_DATA	MEM_DATA	MEM_A_DQ<39..32>	15 33
MEM_40S	MEM_DATA	MEM_DATA	MEM_A_DM<4>	15 33
MEM_40S	MEM_DATA	MEM_DATA	MEM_A_DQ<47..40>	15 33
MEM_40S	MEM_DATA	MEM_DATA	MEM_A_DM<5>	15 33
MEM_40S	MEM_DATA	MEM_DATA	MEM_A_DQ<55..48>	15 33
MEM_40S	MEM_DATA	MEM_DATA	MEM_A_DM<6>	15 33
MEM_40S	MEM_DATA	MEM_DATA	MEM_A_DQ<63..56>	15 33
MEM_40S	MEM_DATA	MEM_DATA	MEM_A_DM<7>	15 33
MEM_70D	MEM_DQS	MEM_DQS	MEM_A_DQS_P<0>	15 33
MEM_70D	MEM_DQS	MEM_DQS	MEM_A_DQS_N<0>	15 33
MEM_70D	MEM_DQS	MEM_DQS	MEM_A_DQS_P<1>	15 33
MEM_70D	MEM_DQS	MEM_DQS	MEM_A_DQS_N<1>	15 33
MEM_70D	MEM_DQS	MEM_DQS	MEM_A_DQS_P<2>	15 33
MEM_70D	MEM_DQS	MEM_DQS	MEM_A_DQS_N<2>	15 33
MEM_70D	MEM_DQS	MEM_DQS	MEM_A_DQS_P<3>	15 33
MEM_70D	MEM_DQS	MEM_DQS	MEM_A_DQS_N<3>	15 33
MEM_70D	MEM_DQS	MEM_DQS	MEM_A_DQS_P<4>	15 33
MEM_70D	MEM_DQS	MEM_DQS	MEM_A_DQS_N<4>	15 33
MEM_70D	MEM_DQS	MEM_DQS	MEM_A_DQS_P<5>	15 33
MEM_70D	MEM_DQS	MEM_DQS	MEM_A_DQS_N<5>	15 33
MEM_70D	MEM_DQS	MEM_DQS	MEM_A_DQS_P<6>	15 33
MEM_70D	MEM_DQS	MEM_DQS	MEM_A_DQS_N<6>	15 33
MEM_70D	MEM_DQS	MEM_DQS	MEM_A_DQS_P<7>	15 33
MEM_70D	MEM_DQS	MEM_DQS	MEM_A_DQS_N<7>	15 33
MEM_70D_VDD	MEM_CLK	MEM_CLK	MEM_B_CLK_P<1..0>	15 33
MEM_70D_VDD	MEM_CLK	MEM_CLK	MEM_B_CLK_N<1..0>	15 33
MEM_70D_VDD	MEM_CLK	MEM_CLK	MEM_B_CLK_P<4..3>	16 33
MEM_70D_VDD	MEM_CLK	MEM_CLK	MEM_B_CLK_N<4..3>	16 33
MEM_40S_VDD	MEM_CTRL	MEM_CTRL	MEM_B_CKE<3..0>	15 16 32
MEM_40S_VDD	MEM_CTRL	MEM_CTRL	MEM_B_CS_L<3..0>	15 16 32
MEM_40S_VDD	MEM_CTRL	MEM_CTRL	MEM_B_ODT<3..0>	15 16 32
MEM_40S_VDD	MEM_CMD	MEM_CMD	MEM_B_A<14..0>	15 32
MEM_40S_VDD	MEM_CMD	MEM_CMD	MEM_B_BA<2..0>	15 32
MEM_40S_VDD	MEM_CMD	MEM_CMD	MEM_B_RAS_L	15 32
MEM_40S_VDD	MEM_CMD	MEM_CMD	MEM_B_CAS_L	15 32
MEM_40S_VDD	MEM_CMD	MEM_CMD	MEM_B_WE_L	15 32
MEM_40S	MEM_DATA	MEM_DATA	MEM_B_DQ<7..0>	15 33
MEM_40S	MEM_DATA	MEM_DATA	MEM_B_DM<0>	15 33
MEM_40S	MEM_DATA	MEM_DATA	MEM_B_DQ<15..8>	15 33
MEM_40S	MEM_DATA	MEM_DATA	MEM_B_DM<1>	15 33
MEM_40S	MEM_DATA	MEM_DATA	MEM_B_DQ<23..16>	15 33
MEM_40S	MEM_DATA	MEM_DATA	MEM_B_DM<2>	15 33
MEM_40S	MEM_DATA	MEM_DATA	MEM_B_DQ<31..24>	15 33
MEM_40S	MEM_DATA	MEM_DATA	MEM_B_DM<3>	15 33
MEM_40S	MEM_DATA	MEM_DATA	MEM_B_DQ<39..32>	15 33
MEM_40S	MEM_DATA	MEM_DATA	MEM_B_DM<4>	15 33
MEM_40S	MEM_DATA	MEM_DATA	MEM_B_DQ<47..40>	15 33
MEM_40S	MEM_DATA	MEM_DATA	MEM_B_DM<5>	15 33
MEM_40S	MEM_DATA	MEM_DATA	MEM_B_DQ<55..48>	15 33
MEM_40S	MEM_DATA	MEM_DATA	MEM_B_DM<6>	15 33
MEM_40S	MEM_DATA	MEM_DATA	MEM_B_DQ<63..56>	15 33
MEM_40S	MEM_DATA	MEM_DATA	MEM_B_DM<7>	15 33

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_70D	MEM_DQS	MEM_DQS	MEM_B_DQS_P<0>	15 33
MEM_70D	MEM_DQS	MEM_DQS	MEM_B_DQS_N<0>	15 33
MEM_70D	MEM_DQS	MEM_DQS	MEM_B_DQS_P<1>	15 33
MEM_70D	MEM_DQS	MEM_DQS	MEM_B_DQS_N<1>	15 33
MEM_70D	MEM_DQS	MEM_DQS	MEM_B_DQS_P<2>	15 33
MEM_70D	MEM_DQS	MEM_DQS	MEM_B_DQS_N<2>	15 33
MEM_70D	MEM_DQS	MEM_DQS	MEM_B_DQS_P<3>	15 33
MEM_70D	MEM_DQS	MEM_DQS	MEM_B_DQS_N<3>	15 33
MEM_70D	MEM_DQS	MEM_DQS	MEM_B_DQS_P<4>	15 33
MEM_70D	MEM_DQS	MEM_DQS	MEM_B_DQS_N<4>	15 33
MEM_70D	MEM_DQS	MEM_DQS	MEM_B_DQS_P<5>	15 33
MEM_70D	MEM_DQS	MEM_DQS	MEM_B_DQS_N<5>	15 33
MEM_70D	MEM_DQS	MEM_DQS	MEM_B_DQS_P<6>	15 33
MEM_70D	MEM_DQS	MEM_DQS	MEM_B_DQS_N<6>	15 33
MEM_70D	MEM_DQS	MEM_DQS	MEM_B_DQS_P<7>	15 33
MEM_70D	MEM_DQS	MEM_DQS	MEM_B_DQS_N<7>	15 33
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	16
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	16

SYNC_MASTER=MASTER SYNC_DATE=N/A
PAGE TITLE: Memory Constraints

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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	0.5 MM	?
MCP_PEX_COMP	*	0.2 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERMP	*	0.2 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCIE GRAPHICS				
	PCIE_90D	PCIE	PEG_R2D_C_P<15..0>	9 86
	PCIE_90D	PCIE	PEG_R2D_C_N<15..0>	9 86
	PCIE_90D	PCIE	PEG_D2R_P<15..0>	9 86
	PCIE_90D	PCIE	PEG_D2R_N<15..0>	9 86
	PCIE_90D	PCIE	MXM_PCIE_R2D_P<15..0>	84 86
	PCIE_90D	PCIE	MXM_PCIE_R2D_N<15..0>	84 86
	PCIE_90D	PCIE	MXM_PCIE_D2R_P<15..0>	84 86
	PCIE_90D	PCIE	MXM_PCIE_D2R_N<15..0>	84 86
PCIE I/O				
	PCIE_90D	PCIE	PCIE_MINI_R2D_P	34
	PCIE_90D	PCIE	PCIE_MINI_R2D_N	34
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P	17 34
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N	17 34
	PCIE_90D	PCIE	PCIE_MINI_R2D_L_P	34
	PCIE_90D	PCIE	PCIE_MINI_R2D_L_N	34
	PCIE_90D	PCIE	PCIE_MINI_D2R_P	17 34
	PCIE_90D	PCIE	PCIE_MINI_D2R_N	17 34
	PCIE_90D	PCIE	PCIE_FW_R2D_P	41
	PCIE_90D	PCIE	PCIE_FW_R2D_N	41
	PCIE_90D	PCIE	PCIE_FW_R2D_C_P	17 41
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N	17 41
	PCIE_90D	PCIE	PCIE_FW_D2R_P	17 41
	PCIE_90D	PCIE	PCIE_FW_D2R_N	17 41
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P	41
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N	41
PCIE REF CLOCKS				
	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_P	9 87
	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_N	9 87
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	17 34
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	17 34
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CON_P	34
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CON_N	34
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P	17 41
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N	17 41
SATA				
	SATA_100D	SATA	SATA_HDD_R2D_C_P	20 45
	SATA_100D	SATA	SATA_HDD_R2D_C_N	20 45
	SATA_100D	SATA	SATA_HDD_R2D_P	45 110
	SATA_100D	SATA	SATA_HDD_R2D_N	45 110
	SATA_100D	SATA	SATA_HDD_D2R_P	20 45
	SATA_100D	SATA	SATA_HDD_D2R_N	20 45
	SATA_100D	SATA	SATA_HDD_D2R_C_P	45 110
	SATA_100D	SATA	SATA_HDD_D2R_C_N	45 110
	SATA_100D	SATA	SATA_ODD_R2D_C_P	20 45
	SATA_100D	SATA	SATA_ODD_R2D_C_N	20 45
	SATA_100D	SATA	SATA_ODD_R2D_P	45 110
	SATA_100D	SATA	SATA_ODD_R2D_N	45 110
	SATA_100D	SATA	SATA_ODD_D2R_P	20 45
	SATA_100D	SATA	SATA_ODD_D2R_N	20 45
	SATA_100D	SATA	SATA_ODD_D2R_C_P	45 110
	SATA_100D	SATA	SATA_ODD_D2R_C_N	45 110
	MCP_SOS	SATA_TERMP	MCP_SATA_TERMP	20
MISC				
	MCP_SOS	MCP_PEX_COMP	MCP_PEX_CLK_COMP	17
	MCP_DV_COMP	MCP_PEX_COMP	MCP_IFPAB_RSET	18 26
	MCP_SOS	MCP_PEX_COMP	MCP_IFPAB_VPROBE	18 26
			PM_SLP_S3_L	9 21
			PM_SLP_S4_L	21 70

SYNC MASTER=MASTER SYNC DATE=N/A

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	0.15 MM	?
CLK_LPC	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	0.2 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

XTAL Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_MCP_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4X_DIELECTRIC	?

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
PCI_55S	PCI	PCI_REQ0_L	19
PCI_55S	PCI	PCI_REQ1_L	19
CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP_R	19
CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP	19
LPC_55S	LPC	LPC_AD<3..0>	19 49 51
LPC_55S	LPC	LPC_AD_R<3..0>	19
LPC_55S	LPC	LPC_FRAME_L	19 49 51
LPC_55S	LPC	LPC_FRAME_R_L	19
LPC_55S	LPC	LPC_RESET_L	9 19
CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	9 19
CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	9 49
CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	9 51
CLK_LPC_55S	CLK_LPC	PM_CLK32K_SUSCLK_R	9 21
CLK_LPC_55S	CLK_LPC	PM_CLK32K_SUSCLK	9 49
MCP_USB_RBIAS		MCP_USB_RBIAS_GND	20
USB_90D	USB	USB_EXTA_P	20 46
USB_90D	USB	USB_EXTA_N	20 46
USB_90D	USB	USB_PORT0_P	46
USB_90D	USB	USB_PORT0_N	46
USB_90D	USB	USB_EXTB_P	20 46
USB_90D	USB	USB_EXTB_N	20 46
USB_90D	USB	USB_PORT1_P	46
USB_90D	USB	USB_PORT1_N	46
USB_90D	USB	USB_EXTC_P	20 46
USB_90D	USB	USB_EXTC_N	20 46
USB_90D	USB	USB_PORT2_P	46
USB_90D	USB	USB_PORT2_N	46
USB_90D	USB	USB_EXTD_P	20 46
USB_90D	USB	USB_EXTD_N	20 46
USB_90D	USB	USB_D_MUXED_P	46
USB_90D	USB	USB_D_MUXED_N	46
USB_90D	USB	USB_PORT3_P	46
USB_90D	USB	USB_PORT3_N	46
USB_90D	USB	USB_CAMERA_P	20 47
USB_90D	USB	USB_CAMERA_N	20 47
USB_90D	USB	USB_CAMERA_L_P	47 110
USB_90D	USB	USB_CAMERA_L_N	47 110
USB_90D	USB	USB_BT_P	20 47
USB_90D	USB	USB_BT_N	20 47
USB_90D	USB	USB_BT_L_P	47 110
USB_90D	USB	USB_BT_L_N	47 110
USB_90D	USB	USB_IR_P	20 47
USB_90D	USB	USB_IR_N	20 47
USB_90D	USB	USB_IR_L_P	47 110
USB_90D	USB	USB_IR_L_N	47 110
USB_90D	USB	USB_SDCARD_P	20 47
USB_90D	USB	USB_SDCARD_N	20 47
USB_90D	USB	USB_SDCARD_L_P	47 110
USB_90D	USB	USB_SDCARD_L_N	47 110
MCP_50S	SPI	SPI_CLK_R	21 51 61
MCP_50S	SPI	SPI_CLK	61
MCP_50S	SPI	SPI_MOSI_R	21 51 61
MCP_50S	SPI	SPI_MOSI	61
MCP_50S	SPI	SPI_MISO	21 51 61
MCP_50S	SPI	SPI_MISO_R	61
MCP_50S	SPI	SPI_CS0_R_L	21 51
MCP_50S	SPI	SPI_CS0_L	51
HDA_55S	HDA	HDA_BIT_CLK	21 62
	MCP_HDA_COMP	MCP_HDA_PULLDN_COMP	21
HDA_55S	HDA	HDA_BIT_CLK_R	21
HDA_55S	HDA	HDA_RST_L	21 62
HDA_55S	HDA	HDA_RST_R_L	21
HDA_55S	HDA	HDA_SDOUT	21 62
HDA_55S	HDA	HDA_SDOUT_R	21
HDA_55S	HDA	HDA_SYNC	21 62
HDA_55S	HDA	HDA_SYNC_R	21
HDA_55S	HDA	HDA_SDIN0	21 62
HDA_55S	HDA	AUD_SDI_R	62
	HDA	AUD_SPDIF_IN	9 66
	HDA	AUD_SPDIF_OUT	62 66
	HDA	AUD_SPDIF_CHIP	62
CLK_MCP_XTAL	XTAL	MCP_CLK25M_XTALOUT	21 28
CLK_MCP_XTAL	XTAL	MCP_CLK25M_XTALIN	21 28
CLK_MCP_XTAL	XTAL	RTC_CLK32K_XTALOUT	21 28
CLK_MCP_XTAL	XTAL	RTC_CLK32K_XTALIN	21 28

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MCP Constraints 2

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	0.2 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	0.3 MM	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

RTL8211CLGR (ETHERNET PHY) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	MCP_MII_COMP		MCP_MII_COMP_VDD	18
	MCP_MII_COMP		MCP_MII_COMP_GND	18
	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	18 38
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	37 38
	ENET_MII_55S	ENET_MII	ENET_MDIO	18 37
	ENET_MII_55S	ENET_MII	ENET_MDC	18 37
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	18 37
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	37
	ENET_MII_55S	ENET_MII	ENET_RXD<0>	18 37
	ENET_MII_55S	ENET_MII	ENET_RXD_R<0>	37
	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	18 37
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..1>	37
	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	18 37
	ENET_MII_55S	ENET_MII	ENET_RXCTL_R	37
	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	18 37
	ENET_MII_55S	ENET_MII	ENET_TXD<0>	18 37
	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	18 37
	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	18 37
	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	37 39
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	37 39
	ENET_MDI_100D	ENET_MDI	ENET_MDI_T_P<3..0>	39
	ENET_MDI_100D	ENET_MDI	ENET_MDI_T_N<3..0>	39

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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
	FW_110D	FW_TP	FW_PORT0_TPA_P	42 43
	FW_110D	FW_TP	FW_PORT0_TPA_N	42 43
	FW_110D	FW_TP	FW_PORT0_TPB_P	42 43
	FW_110D	FW_TP	FW_PORT0_TPB_N	42 43
PORT 1 & 2 NOT USED				
	FW_110D	FW_TP	FW_P0_TPA_L_P	42
	FW_110D	FW_TP	FW_P0_TPA_L_N	42
	FW_110D	FW_TP	FW_P0_TPB_L_P	42
	FW_110D	FW_TP	FW_P0_TPB_L_N	42

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SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_5S8	*	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SMB_5S8	SMB	SMBUS_SMC_A_S3_SCL	52
	SMB_5S8	SMB	SMBUS_SMC_A_S3_SDA	52
	SMB_5S8	SMB	SMBUS_SMC_B_S0_SCL	52
	SMB_5S8	SMB	SMBUS_SMC_B_S0_SDA	52
	SMB_5S8	SMB	SMBUS_SMC_0_S0_SCL	52
	SMB_5S8	SMB	SMBUS_SMC_0_S0_SDA	52
	SMB_5S8	SMB	SMBUS_SMC_BSA_SCL	52
	SMB_5S8	SMB	SMBUS_SMC_BSA_SDA	52
	SMB_5S8	SMB	SMBUS_SMC_MGMT_SCL	52 106
	SMB_5S8	SMB	SMBUS_SMC_MGMT_SDA	52 106
	SMB_5S8	SMB	SMBUS_SMC_MGMT_SCL	52 106
	SMB_5S8	SMB	SMBUS_SMC_MGMT_SDA	52 106
	SMB_5S8	SMB	SMBUS_MCP_0_CLK	13 21 52
	SMB_5S8	SMB	SMBUS_MCP_0_DATA	13 21 52

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	0.08 MM	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	0.5 MM	0.5 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

NET_TYPE

ELECTRICAL_CONSTRAINT_SET ASSINGED IN CONT. MGR.	PHYSICAL	SPACING		
	DP_100D	DISPLAYPORT	MXM_DP_A_ML_P<3..0>	84 91
	DP_100D	DISPLAYPORT	DP_IG_ML_P<3..0>	9 91
	DP_100D	DISPLAYPORT	MXM_DP_A_ML_N<3..0>	84 91
	DP_100D	DISPLAYPORT	DP_IG_ML_N<3..0>	9 91
	DP_100D	DISPLAYPORT	DP_ML_P<3..0>	91 94
	DP_100D	DISPLAYPORT	DP_ML_N<3..0>	91 94
	DP_100D	DISPLAYPORT	DP_ML_CONN_P<3..0>	94
	DP_100D	DISPLAYPORT	DP_ML_CONN_N<3..0>	94
	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_P	18 93
	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_N	18 93
	DP_100D	DISPLAYPORT	DP_AUXCH_SW_P	93
	DP_100D	DISPLAYPORT	DP_AUXCH_SW_N	93
	DP_100D	DISPLAYPORT	DP_AUX_CH_C_P	93 94
	DP_100D	DISPLAYPORT	DP_AUX_CH_C_N	93 94
	DP_100D	DISPLAYPORT	MXM_DP_A_AUX_P	84 93
	DP_100D	DISPLAYPORT	MXM_DP_A_AUX_N	84 93
	LVDS_100D	LVDS	LVDS_IG_A_CLK_P	18 89
	LVDS_100D	LVDS	LVDS_IG_A_CLK_N	18 89
	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<3..0>	18 89
	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<3..0>	18 89
	LVDS_100D	LVDS	LVDS_IG_B_CLK_P	18 89
	LVDS_100D	LVDS	LVDS_IG_B_CLK_N	18 89
	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<3..0>	18 89
	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<3..0>	18 89
	LVDS_100D	LVDS	LVDS_A_DATA_P<3..0>	89
	LVDS_100D	LVDS	LVDS_A_DATA_N<3..0>	89
	LVDS_100D	LVDS	LVDS_B_DATA_P<3..0>	89
	LVDS_100D	LVDS	LVDS_B_DATA_N<3..0>	89
	LVDS_100D	LVDS	LCD_CONN_A_DATA_P<3..0>	89 90
	LVDS_100D	LVDS	LCD_CONN_A_DATA_N<3..0>	89 90
	LVDS_100D	LVDS	LCD_CONN_B_DATA_P<3..0>	89 90
	LVDS_100D	LVDS	LCD_CONN_B_DATA_N<3..0>	89 90
	LVDS_100D	LVDS	LVDS_A_CLK_P	89
	LVDS_100D	LVDS	LVDS_A_CLK_N	89
	LVDS_100D	LVDS	LVDS_B_CLK_P	89
	LVDS_100D	LVDS	LVDS_B_CLK_N	89
	LVDS_100D	LVDS	LCD_CONN_A_CLK_P	89 90
	LVDS_100D	LVDS	LCD_CONN_A_CLK_N	89 90
	LVDS_100D	LVDS	LCD_CONN_B_CLK_P	89 90
	LVDS_100D	LVDS	LCD_CONN_B_CLK_N	89 90
	MCP_DV_COMP		MCP_HDMI_RSET	18 26
	MCP_DV_COMP		MCP_HDMI_VPROBE	18 26

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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PPDDR_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PPDDR_MEM	*	PWR_P2MM
MEM_CMD	PPDDR_MEM	*	PWR_P2MM
MEM_CTRL	PPDDR_MEM	*	PWR_P2MM
MEM_DATA	PPDDR_MEM	*	PWR_P2MM
MEM_DQS	PPDDR_MEM	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	PWR	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
THERMAL	*	*	4:1_SPACING
SWITCHNODE	*	*	SWITCHNODE
THERMAL	PWR	*	PWR_P2MM
THERMAL	GND	*	GND_P2MM
AUDIO	*	*	AUDIO

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
THERM_DIFF	*	1:1_DIFFPAIR
SNS_DIFF	*	1:1_DIFFPAIR

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	TOP			0.1 MM	600 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S_VDD	TOP			0.1 MM	600 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D	TOP			0.1 MM	600 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
PCIE_90D	TOP				500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
USB_90D	TOP				500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP	*			0.25 MM	250 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

K50/K51 SPECIFIC NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
		PPDDR_MEM	=PP1V5_S3_MEM_A	6 30 31
		PPDDR_MEM	=PP1V5_S3_MEM_B	6 30 32
		SWITCHNODE	VR_CPU_SW1	72
		SWITCHNODE	VR_CPU_SW2	72
		SWITCHNODE	VR_CPU_SW3	72
		SWITCHNODE	1V8_SW	80
		SWITCHNODE	1V1S5_SW	79
		SWITCHNODE	PVTTS0_PHASE	76
		SWITCHNODE	3V3S5_SW	76
		SWITCHNODE	5VS3_SW	73
		SWITCHNODE	MCPCORES0_PHASE	74
	THERM_DIFF	THERMAL	SNS_T_DP1_DN6	55
	THERM_DIFF	THERMAL	SNS_T_DN1_DP6	55
	THERM_DIFF	THERMAL	SNS_T_DP2_DN3	55
	THERM_DIFF	THERMAL	SNS_T_DN2_DP3	55
	THERM_DIFF	THERMAL	CPU_THERMD_P	11 55
	THERM_DIFF	THERMAL	CPU_THERMD_N	11 55
	THERM_DIFF	THERMAL	SNS_T_DP4_DN5	55
	THERM_DIFF	THERMAL	SNS_T_DN4_DP5	55
	THERM_DIFF	THERMAL	MCP_THMDIODE_P	21 55
	THERM_DIFF	THERMAL	MCP_THMDIODE_N	21 55
	THERM_DIFF	THERMAL	MXM_PWRSRC_SENSOR_P	53
	THERM_DIFF	THERMAL	MXM_PWRSRC_SENSOR_N	53
	THERM_DIFF	THERMAL	SENSE_1V5_S0_P	54
	THERM_DIFF	THERMAL	SENSE_1V5_S0_N	54
	THERM_DIFF	THERMAL	SNS_LCD_P	55 110
	THERM_DIFF	THERMAL	SNS_LCD_N	55 110
	THERM_DIFF	THERMAL	SNS_ODD_P	55 110
	THERM_DIFF	THERMAL	SNS_ODD_N	55 110
	THERM_DIFF	THERMAL	SNS_CPU_H_P	55
	THERM_DIFF	THERMAL	SNS_CPU_H_N	55
	THERM_DIFF	THERMAL	SNS_MCP_P	55
	THERM_DIFF	THERMAL	SNS_MCP_N	55
	THERM_DIFF	THERMAL	SNS_AMB_P	55 110
	THERM_DIFF	THERMAL	SNS_AMB_N	55 110
	THERM_DIFF	THERMAL	SNS_MXM_P	55
	THERM_DIFF	THERMAL	SNS_MXM_N	55
	SNS_DIFF	THERMAL	VR_CPU_ISNS1_P	71 72
	SNS_DIFF	THERMAL	VR_CPU_ISNS1_N	71 72
	SNS_DIFF	THERMAL	VR_CPU_ISNS1_R_P	71
	SNS_DIFF	THERMAL	VR_CPU_ISNS1_R_N	71
	SNS_DIFF	THERMAL	VR_CPU_ISNS2_P	71 72
	SNS_DIFF	THERMAL	VR_CPU_ISNS2_N	71 72
	SNS_DIFF	THERMAL	VR_CPU_ISNS2_R_P	71
	SNS_DIFF	THERMAL	VR_CPU_ISNS2_R_N	71
	SNS_DIFF	THERMAL	VR_CPU_ISNS3_P	71 72
	SNS_DIFF	THERMAL	VR_CPU_ISNS3_N	71 72
	SNS_DIFF	THERMAL	VR_CPU_ISNS3_R_P	71
	SNS_DIFF	THERMAL	VR_CPU_ISNS3_R_N	71
I2C		THERMAL	SMC_CPU_ISENSE	49 53
I2C		THERMAL	VR_CPU_IOUT	53 71
I2C		THERMAL	VR_ISNS_CPU_P	53
I2C		THERMAL	VR_ISNS_CPU_N	53
I2C		THERMAL	SNS_PS_CPU_ISNS	53
I2C		THERMAL	SMC_CPU_VSENSE	49 53
I2C		THERMAL	CPU_VCC_SENSE	12 53
I2C		THERMAL	SMC_GPU_VSENSE	49 53
I2C		THERMAL	SMC_GPU_ISENSE	49 53
I2C		THERMAL	SMC_1V5_S0_ISENSE	50 54
I2C		THERMAL	SMC_1V5_S0_ISENSE_R	54
I2C		THERMAL	SMC_1V5_S0_VSENSE	50 54
I2C		THERMAL	SMC_MCP_CORE_ISENSE	50 54
I2C		THERMAL	SMC_MCP_CORE_VSENSE	50 54
I2C		THERMAL	MCPCORES0_IMON	54 74
I2C		THERMAL	CPU_PECI_L	11 55
I2C		THERMAL	SMB_PECI_L	55
I2C		THERMAL	CPU_PECI_MCP	14 55
		THERMAL	HDD_OOB_TEMP_FILT	55
I2C		THERMAL	HDD_OOB_TEMP	55
I2C		THERMAL	HDD_OOB_TEMP_R	55
I2C		THERMAL	SMC_HDD_OOB_TEMP	55

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K22/K23 SPECIFIC CONSTRAINTS

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K50/K51 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.5.1

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	100 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.300 MM	0.085 MM	=STANDARD		
27P4_OHM_SE	*	Y	0.275 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.085 MM	=STANDARD		
40_OHM_SE	*	Y	0.15 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
42_OHM_SE	TOP,BOTTOM	Y	0.151 MM	0.085 MM	=STANDARD		
42_OHM_SE	*	Y	0.136 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.1 MM	0.085 MM	15 MM		
50_OHM_SE	*	Y	0.1 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD		
55_OHM_SE	*	Y	0.076 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL6	Y	0.155 MM	0.085 MM	=STANDARD	0.135 MM	0.1 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.085 MM	=STANDARD	0.130 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL6	Y	0.099 MM	0.085 MM	12 MM	0.200 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.110 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL6	Y	0.081 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.085 MM	=STANDARD	0.320 MM	0.15 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM
POWER_WIDTH	*	Y	0.600 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER	*	POWER_WIDTH
VR_CTL_PHY	*	POWER_WIDTH

SPACING RULE SET

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SPACING_0.5MM	*	0.5 MM	?
CLK_SPACING_0.6MM	*	0.6 MM	?
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000
SWITCHNODE	*	0.6 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.150 MM	?
2X_DIELECTRIC	TOP,BOTTOM	0.160 MM	?
3X_DIELECTRIC	*	0.220 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.240 MM	?
4X_DIELECTRIC	*	0.300 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.320 MM	?
5X_DIELECTRIC	*	0.380 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.400 MM	?

CONSTRAINTS FOR BGA AREA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	0.2 MM	?
BGA_P3MM	*	0.3 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P1MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P1MM
CLK_LPC	*	BGA_P1MM	BGA_P1MM
CLK_PCI	*	BGA_P1MM	BGA_P1MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MCP_FSB_COMP	*	BGA_P1MM	BGA_P2MM
MCP_MEM_COMP	*	BGA_P1MM	BGA_P2MM
MCP_PEX_COMP	*	BGA_P1MM	BGA_P2MM

CONSTRAINTS ARE BASED ON MCP79 DESIGN GUIDE DG-03328-001_V06
PCI,LPC,SMB,HDA,SPI,RGMII,SMBUS ARE ROUTED AS 55 OHM SE SIGNALS

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FUNCTIONAL TESTPOINTS FOR MAC-1 & ICT

J4700 USB CAMERA

103 47	IN	USB_CAMERA_L_P	FUNC_TEST=TRUE
103 47	IN	USB_CAMERA_L_N	FUNC_TEST=TRUE

1 PP5V_S3_REG Testpoint near J4700
2 Ground Testpoints near J4700

J4750 USB CARD READER

103 47	IN	USB_SDCARD_L_P	FUNC_TEST=TRUE
103 47	IN	USB_SDCARD_L_N	FUNC_TEST=TRUE

1 PP3V3_S3 Testpoint near J4750
2 Ground Testpoints near J4750

J4720 USB BLUETOOTH

103 47	IN	USB_BT_L_P	FUNC_TEST=TRUE
103 47	IN	USB_BT_L_N	FUNC_TEST=TRUE

1 PP3V3_S3 Testpoint near J4720
2 Ground Testpoints near J4720

J4780 IR BOARD

103 47	IN	USB_IR_L_P	FUNC_TEST=TRUE
103 47	IN	USB_IR_L_N	FUNC_TEST=TRUE

1 PP5V_S3_REG Testpoint near J4780
2 Ground Testpoints near J4780

J4520 SATA ODD (HIGH SPEED)

102 45	IN	SATA_ODD_R2D_P	FUNC_TEST=TRUE
102 45	IN	SATA_ODD_R2D_N	FUNC_TEST=TRUE
102 45	IN	SATA_ODD_D2R_C_N	FUNC_TEST=TRUE
102 45	IN	SATA_ODD_D2R_C_P	FUNC_TEST=TRUE
49 45	IN	SMC_ODD_DETECT	FUNC_TEST=TRUE

1 PP5V_S0 Testpoint near J4520
5 Ground Testpoints near J4520

J4510 SATA HDD (HIGH SPEED)

102 45	IN	SATA_HDD_R2D_P	FUNC_TEST=TRUE
102 45	IN	SATA_HDD_R2D_N	FUNC_TEST=TRUE
102 45	IN	SATA_HDD_D2R_C_N	FUNC_TEST=TRUE
102 45	IN	SATA_HDD_D2R_C_P	FUNC_TEST=TRUE

3 Ground Testpoints near J4510

J5520 ANALOG LCD TEMP SENSOR

108 55	IN	SNS_LCD_P	FUNC_TEST=TRUE
108 55	IN	SNS_LCD_N	FUNC_TEST=TRUE

J5521 AMBIENT TEMP SENSOR

108 55	IN	SNS_AMB_P	FUNC_TEST=TRUE
108 55	IN	SNS_AMB_N	FUNC_TEST=TRUE

J5551 ODD TEMP SENSOR

108 55	IN	SNS_ODD_P	FUNC_TEST=TRUE
108 55	IN	SNS_ODD_N	FUNC_TEST=TRUE

J5600 ODD FAN

56	IN	FAN_0_PWR_L	FUNC_TEST=TRUE
56	IN	FAN_TACH0_L	FUNC_TEST=TRUE
56	IN	PP12V_S0_FAN0_L	FUNC_TEST=TRUE
56	IN	FAN_0_GND	FUNC_TEST=TRUE

J5700 CPU FAN

57	IN	FAN_2_PWR_L	FUNC_TEST=TRUE
57	IN	FAN_TACH2_L	FUNC_TEST=TRUE
57	IN	PP12V_S0_FAN2_L	FUNC_TEST=TRUE
57	IN	FAN_2_GND	FUNC_TEST=TRUE

J5601 HD FAN

56	IN	FAN_1_PWR_L	FUNC_TEST=TRUE
56	IN	FAN_TACH1_L	FUNC_TEST=TRUE
56	IN	PP12V_S0_FAN1_L	FUNC_TEST=TRUE
56	IN	FAN_1_GND	FUNC_TEST=TRUE

J6601 AUDIO MICROPHONE

66	IN	AUD_MIC_IN1_N_CONN	FUNC_TEST=TRUE
66	IN	GND_AUDIO_MIC1_CONN	FUNC_TEST=TRUE
66	IN	AUD_MIC_IN1_P_CONN	FUNC_TEST=TRUE

1 Ground Testpoint near J6601

J6602 AUDIO RIGHT SPEAKER

	IN	AUD_SPKR_OUTLO2R_P	FUNC_TEST=TRUE
	IN	AUD_SPKR_OUTLO2R_N	FUNC_TEST=TRUE
	IN	AUD_SPKR_OUTLO1R_P	FUNC_TEST=TRUE
	IN	AUD_SPKR_OUTLO1R_N	FUNC_TEST=TRUE

J6603 AUDIO LEFT SPEAKER

	IN	AUD_SPKR_OUTLO2L_P	FUNC_TEST=TRUE
	IN	AUD_SPKR_OUTLO2L_N	FUNC_TEST=TRUE
	IN	AUD_SPKR_OUTLO1L_P	FUNC_TEST=TRUE
	IN	AUD_SPKR_OUTLO1L_N	FUNC_TEST=TRUE

		GND	16 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=16
78 6	IN	PP3V3_S3	2 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=2
73 6	IN	PP5V_S3_REG	2 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=2
78 6	IN	PP5V_S0	FUNC_TEST=TRUE MIN_ALLOWED_TPS=1

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