## Post-Ramp

### Schematic / PCB #’s

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DCC</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
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</table>

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- Page 3: SOM Configuration
- Page 4: Motherboard Support
- Page 5: SDRAM Support
- Page 6: Smart Connector Support
- Page 7: Ethernet PHY (RTL8211CL)
- Page 8: DDR3 Support
- Page 9: CPU (SMM)
- Page 10: CPU (I/O)
- Page 11: CPU (USB)
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- Page 13: CPU (I/O)
- Page 14: CPU (I/O)
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- Page 27: CPU (I/O)
- Page 28: CPU (I/O)
- Page 29: CPU (I/O)
- Page 30: CPU (I/O)
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- Page 33: CPU (I/O)
- Page 34: CPU (I/O)
- Page 35: CPU (I/O)

## Revision History

- 03/11/2009: Initial release
- 06/30/2008: Update 1
- 03/30/2008: Update 2
- 02/11/2008: Update 3
- 01/11/2008: Update 4
- 08/22/2007: Update 5

---

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---

**M97A MLB SCHEMATIC**

REFERENCED FROM T18

03/11/2009
### Module Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
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### Programmable Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
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</thead>
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</tr>
</tbody>
</table>

### Alternate Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
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<th>BOM OPTION</th>
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**M97 BOARD STACK-UP**

**Top**
- SIGNAL
- GROUND
- SIGNAL
- SIGNAL
- GROUND
- POWER
- POWER
- GROUND
- SIGNAL
- SIGNAL

**Bottom**
- SIGNAL

---

**RQM Configuration**

- **Revision:**
- **Title:** M97 BOARD STACK-UP
- **Date:**
- **Scale:**
- **Comments:**

---

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**Part Numbers, BOM Options, BOM Groups, Module Parts**

- **BOM Options:**
- **BOM Groups:**
- **Module Parts:**
- **Programmable Parts:**
- **Alternate Parts:**

---

**Table References:**

- **Table Headings:**
- **Table Items:**

---

**Diagram References:**

- **Diagram Sections:**
- **Diagram Elements:**

---

**Website:**

www.bufanxiu.com
Revision History

- ADD INTERSIL ISL60002(353S1381) AS ALTERNATE FOR TI REF3333(353S1912).
- STUFF R5932.

BOM CHANGES FROM M97:
- UPDATE CPU APNS TO R0 STEPPING.
- UPDATE M97A 630 NUMBERS AND EEE CODES, AND 051 NUMBER.
- ... FROM 514-0596 TO 514-0636.
- CHANGE J4600 AND J4610 FROM 514-0606 TO 514-0638.
- CHANGE R6302 FROM 10K(114S315) TO 1K(114S0218).

- REMOVE U5850, L5850, R5854, R5855, C5850, C5855, J5815 ON BETTER BOM.

NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.
1.05V TO 3.3V LEVEL TRANSLATOR (M97: ON ICT FIXTURE)

From XDP connector

U1000 CPU

and/or level translator

To XDP connector

U1400 MCP

From XDP connector or via level translator

XDP connector

JTAG_MCP_TDI

JTAG_MCP_TMS

JTAG_MCP_TCK

JTAG_MCP_TDO

JTAG_MCP_TDO_CONN

JTAG_MCP_TRST_L

JTAG_MCP_TMS

JTAG_SCAN_CHAIN

SYNC_DATE=04/04/2008

SYNC_MASTER=BEN

=PP3V3_S0_XDP

=PP1V05_S0_CPU

JTAG_LVL_TRANS_EN_L

www.bufanxiu.com
## Functional Test Points

### Fan Connectors
- **FUNCTION TEST\[A\]**: TRUE
- **FUNCTION TEST\[B\]**: TRUE
- **FUNCTION TEST\[C\]**: TRUE
- **FUNCTION TEST\[D\]**: TRUE

### MIC Function Test
- **MIC FUNCTION TEST\[A\]**: TRUE
- **MIC FUNCTION TEST\[B\]**: TRUE
- **MIC FUNCTION TEST\[C\]**: TRUE
- **MIC FUNCTION TEST\[D\]**: TRUE

### Speaker Function Test
- **SPEAKER FUNCTION TEST\[A\]**: TRUE
- **SPEAKER FUNCTION TEST\[B\]**: TRUE
- **SPEAKER FUNCTION TEST\[C\]**: TRUE
- **SPEAKER FUNCTION TEST\[D\]**: TRUE

### Thermal Function Test
- **THERMAL FUNCTION TEST\[A\]**: TRUE
- **THERMAL FUNCTION TEST\[B\]**: TRUE
- **THERMAL FUNCTION TEST\[C\]**: TRUE
- **THERMAL FUNCTION TEST\[D\]**: TRUE

### SATA HDD Conn
- **SATA HDD CONN\[A\]**: TRUE
- **SATA HDD CONN\[B\]**: TRUE
- **SATA HDD CONN\[C\]**: TRUE
- **SATA HDD CONN\[D\]**: TRUE

### DC Power Conn
- **DC POWER CONN\[A\]**: TRUE
- **DC POWER CONN\[B\]**: TRUE
- **DC POWER CONN\[C\]**: TRUE
- **DC POWER CONN\[D\]**: TRUE

### Front Flex Conn
- **FRONT FLEX CONN\[A\]**: TRUE
- **FRONT FLEX CONN\[B\]**: TRUE
- **FRONT FLEX CONN\[C\]**: TRUE
- **FRONT FLEX CONN\[D\]**: TRUE

### Batt Power Conn
- **BATT POWER CONN\[A\]**: TRUE
- **BATT POWER CONN\[B\]**: TRUE
- **BATT POWER CONN\[C\]**: TRUE
- **BATT POWER CONN\[D\]**: TRUE

### Batt Signal Conn
- **BATT SIGNAL CONN\[A\]**: TRUE
- **BATT SIGNAL CONN\[B\]**: TRUE
- **BATT SIGNAL CONN\[C\]**: TRUE
- **BATT SIGNAL CONN\[D\]**: TRUE

### Keyboard Conn
- **KEYBOARD CONN\[A\]**: TRUE
- **KEYBOARD CONN\[B\]**: TRUE
- **KEYBOARD CONN\[C\]**: TRUE
- **KEYBOARD CONN\[D\]**: TRUE

### Right Clutch Conn
- **RIGHT CLUTCH CONN\[A\]**: TRUE
- **RIGHT CLUTCH CONN\[B\]**: TRUE
- **RIGHT CLUTCH CONN\[C\]**: TRUE
- **RIGHT CLUTCH CONN\[D\]**: TRUE

### Debug Voltage
- **DEBUG VOLTAGE\[A\]**: TRUE
- **DEBUG VOLTAGE\[B\]**: TRUE
- **DEBUG VOLTAGE\[C\]**: TRUE
- **DEBUG VOLTAGE\[D\]**: TRUE
SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL
CHANGE C1240-C1243 AND C1260 FROM 128S0241 (9 MILLI-OMH) TO 128S0231 (6 MILLI-OMH)

REMOVE C1244 & C1245

REMOVE NO STUFF CAPS C1220 TO C1231

SYNC FROM T18

CPU VCore HF and Bulk Decoupling

- Place 330UF 22UF 0805 CPU VCore HF and Bulk Decoupling
- Place inside socket cavity on secondary side.

VCCP (CPU I/O) DECOUPLING

1x 330UF, 1x 0.1UF

VCCA (CPU AVdd) DECOUPLING

1x 10uF, 1x 0.01uF
MCP79-specific pinout

SYNC FROM T18
CHANGE STANDARD XDP CONNECTOR TO SMALLER ONE 516S0625
RENAME JTAG_MCP_TDO TO JTAG_MCP_TDO_CONN
RENAME XDP_TDO TO XDP_TDO_CONN

NOTE: XDP_DBRESET_L must be pulled-up to 3.3V.
3.3V Interface Pull-ups
These internal pull-ups are missing in Revs A01 & A01P.

R2430 10K MCP_A01&MCP_A01P&MCP_A01Q
R2429 10K MCP_A01&MCP_A01P&MCP_A01Q
R2427 10K MCP_A01&MCP_A01P&MCP_A01Q
R2428 10K MCP_A01&MCP_A01P&MCP_A01Q
R2425 10K MCP_A01&MCP_A01P&MCP_A01Q
R2426 10K MCP_A01&MCP_A01P&MCP_A01Q
R2424 10K MCP_A01&MCP_A01P&MCP_A01Q
R2423 10K MCP_A01&MCP_A01P&MCP_A01Q
R2421 10K MCP_A01&MCP_A01P&MCP_A01Q
R2422 10K MCP_A01&MCP_A01P&MCP_A01Q
R2420 10K MCP_A01&MCP_A01P&MCP_A01Q
R2429 10K MCP_A01&MCP_A01P&MCP_A01Q
R2426 10K MCP_A01&MCP_A01P&MCP_A01Q
R2423 10K MCP_A01&MCP_A01P&MCP_A01Q
R2421 10K MCP_A01&MCP_A01P&MCP_A01Q
R2424 10K MCP_A01&MCP_A01P&MCP_A01Q
R2427 10K MCP_A01&MCP_A01P&MCP_A01Q
R2430 10K MCP_A01&MCP_A01P&MCP_A01Q

MCP_SAFE_MODE SIGNAL TO SUPPORT ROM FAILURE OVERRIDE
SAME VALUE

R2430 10K MCP_A01&MCP_A01P&MCP_A01Q
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

---

**MCP Memory Power**

- **MCP Memory Power**: 1182 mA (A01)
- **MCP FSB (VTT) Power**: 105 mA (A01) 131 mA (A01)
- **MCP 1.05V AUX Power**: 8 mA (A01)

---

**MCP Core Power**

- **MCP Core Power**: 87 mA (A01) 178 mA (A01)

---

**MCP Standard Decoupling**

- **Apple**: 1x 2.2uF 0402 (2.2 uF)
- **NV**: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
  - **MCP 3.3V Ethernet Power**: 1x 4.7uF 0603, 4x 0.1uF 0402 (5.1 uF)
  - **NV**: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
  - **Apple**: 4x 4.7uF 0402, 4x 1uF 0402, 6x 0.1uF 0402 (23.4 uF)
  - **NV**: 1x 10uF 0805, 2x 4.7uF 0402, 3x 1uF 0402, 9x 0.1uF 0402 (23.3 uF)
- **MCP 1.05V RMGT Power**: 37 mA (A01) 206 mA (A01)

---

**SCALE**

- 25 109 21C7 8A8 C051-7918

---

**REV.**

- A 1 D 2 3 4 5 6 7 8

---

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HDCP ROM

- Open question on which Nvidia option(s) Nvidia can support.
- Change to standard.

MCP Graphics Support

- Sync from T18
- Remove MCP 27MHz Crystal Circuit since not supporting TV-out
- Remove DAC terminations R2665, C2665 and R2670 to R2672
- Nostuff PP3V3_S0_MCP_DAC rail components (L2650 and C2650)
- Change C2651 to R2651 to GND PP3V3_S0_MCP_DAC

- No stuff PP3V3_S0_MCP_DAC rail components (L2650 and C2650)
NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

CPU_VDD_EN (which is 40-100ms after PS_PWRGD assertion).

VR_PWRGOOD_DELAY should guarantee CPU_VLD does not go high before SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for results in earlier ROMSIP and MCP FSB I/O interface initialization.

MCPSEQ_MIX is cross between MLB and internal power sequencing, which MCPSEQ_SMC represents MCP79 'MLB' power sequencing connections,

MCP_CPUVDD_EN VR_PWRGOOD_DELAY

MCP S0 PWRGD & CPU_VLD

Reset Button

SYNC FROM T18
CHANGE RESET BUTTON TO RESET PADS
REMOVE UNUSED PCIE RESET SIGNALS
REMOVE R2824 AND NET PCI_CLK33M_SLOT_A
CHANGE RTC COIN CELL TO LDO & SUPERCAP
ALIAS MEM_VTT_EN TO =DDRVTEN
CHANGE Y2810 AND U2850 TO SMALLER PARTS

PLACE C2819 CLOSE TO MCP79
PLACE C2800 AT COOLEST SPOT ON MLB

CHANGE RTC COIN CELL TO LDO & SUPERCAP
PLACE C2800 AT COOLEST SPOT ON MLB

APPLE INC.
So-DIMM A and So-DIMM B Vref settings should be margined separately (i.e., not simultaneously) due to current limitation of TP051116 regulator.

Required zero ohm resistors when no Vref margining circuit stuffed:

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>CRITICAL</th>
<th>NON-OPTIONAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>1160004</td>
<td></td>
<td>CRITICAL</td>
<td>R2909</td>
</tr>
<tr>
<td>1160004</td>
<td></td>
<td>CRITICAL</td>
<td>R2910</td>
</tr>
<tr>
<td>1160004</td>
<td></td>
<td>CRITICAL</td>
<td>R2911</td>
</tr>
<tr>
<td>1160004</td>
<td></td>
<td>CRITICAL</td>
<td>R2912</td>
</tr>
<tr>
<td>1160004</td>
<td></td>
<td>CRITICAL</td>
<td>R2913</td>
</tr>
</tbody>
</table>

Page Notes
DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.

1. DDR3 RESET Support

2. DDR3 Support

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WLAN Enable Generation

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

3.3V ENET FET

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.

1.05V ENET FET

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered. Designs must ensure P1V05 in power whenever RMGT rails are, or use separate crystal.

Ethernet & AirPort Support
We can remove C4690 later if the output cap of the 5V_S5 regulator is close enough.

8D1
20D3 74C3
39B8 39C5 40C2 41C5
=PP3V42_G3H_SMCUSBMUX
OUT
USB_EXTA_N
SMC_RX_L
C4650
0.1UF
CERM
20%
2
MF-LF
1/16W
402
4
7
STUFF R4690 IF USING TPS2064 (ACTIVE HIGH ENABLE)
M+
PI3USB102ZLE
SMC_DEBUG_YES
VCC
20C2
20C3 74B3
20C3 74B3
USB_EXTB_P
USB_EXTB_N
20C3 74B3
USB_PORT B (BACK PORT)
R4652
0
R4650
402
MF-LF
5%
R4690
MF-LF
402
5%
R4691
1/16W
3
4
EN2
U4690
MSOP
91
10UF
6.3V
X5R
20%
C4617
10UF
X5R
20%
2
C4616
100UF
CASE-B2-SM
USB_PWR_EN_R
R4691
402
1/16W
3
VOLTAGE=5V
C4696
PP5V_S3_RTUSB_A_ILIM
POLY-TANT603
20%
2
CRITICAL
C4646
10UF
X5R
20%
2
USB_EXTA_MUXED_P
USB_EXTA_MUXED_N
FERR-220-OHM-2.5A
L4605
90-OHM
SYM_VER-1
0603
PLACEMENT_NOTE=NEAR J4600
L4615
2
MIN_NECK_WIDTH=0.5 mm
L4610
CRITICAL
PP5V_S3_RTUSB_A_F
VOLTAGE=5V
MIN_LINE_WIDTH=0.5 mm
We can add protection to 5V if we want, but leaving NC for now
SLP1210N6
5
IOIO
NC
5 4 2 3
CONN_USB_EXTA_P
CONN_USB_EXTA_N
PLACEHOLDER
PLACEMENT_NOTE=NEAR J4610
Place L4600 and L4605 at connector pin
F-RT-TH-M97-4
514-0638
J4600
CRITICAL
USB
J4610
CRITICAL
8
2
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External USB Connectors
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E
D
C
B
A
SYNC_DATE=01/18/2008
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as capacitors can be left floating. Unused diodes are open-circuit pull-ups.
Alternate SPI ROM Support

SEL LOW OUTPUTS TO M (FRANKCARD ROM)
SEL HIGH OUTPUTS TO D (ON BOARD ROM)

IN 8 7 6 5 4 3 2 1

Alternate SPI ROM Support

1/16W

OUT

IN

10K

2

SPI MUX BYPASS

LPC+SPI Debug Connector

MCP79 Internal SPI MUX Support

MCP SPI Override Options

MCP79 REV A01 REQUIRES EXTERNAL MUX, REV B01 STILL DOES NOT SUPPORT INTERNAL MUX

SPI Frequency Clamp

Ensure MCP79 SPI_CS1_L USE_MLB INPUT IS LOW WHEN STRAP IS LATCHED. NOT NEEDED FOR B01 OR LAYER.

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Keep very short

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SYNC MASTER=CHANGZHANG
SYNC DATE=05/09/2008

MAKE_BASE=TRUE

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CPU T-Diode Thermal Sensor

MCP T-Diode Thermal Sensor

Placement Note: Place U5515 near CPU

PlACEMENT NOTE: PLACE U5535 NEAR MCP

Note: Place U5515 near CPU

Note: Place U5535 near MCP

Replaced 518S0521 with 518S0519
Booster +18.5VDC for sensors

To detect keyboard backlight, SMC will

LOW = keyboard backlight present

SMC keyboard backlight not present

SMC_KBDLED_PRESENT_L

3V3 LDO for IPD

KEYBOARD BACKLIGHT DRIVING AND DETECTION

WELLSPRING 2

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CRITICAL

J5800

R5802

R5801

C5802

C5803

J5815

KBD BACKLIGHT CONNECTOR

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Drawing Number

Size

Page 1 of

Sync Date: 05/02/2008

Sync Master: Changzheng

SPI ROM

http://www.bufanxiu.com

Any of the 4 frequencies can be selected with R6190, R6191, R5190 and R5191.

MC79 SPI Frequency Select

Frequency | SPI_MOSI | SPI_CLK
---|---|---
25 MHz | 0 | 0
42 MHz | 0 | 1
1 MHz | 1 | 0
8 MHz | 1 | 1
PWM FREQ. = 300 KHZ
8D6
8D6
8D6
8D6
8D6
VOLTAGE=5V

Place XW7201 between Pin 15 and Pin 24 of U7200.

VOUT = (2 * RA / RB) + 2
VOUT = (2 * RC / RD) + 2

Place XW7203 by Pin 1 OF L7260. Place XW7204 by Pin 2 of L7220.

Routine Note:

Place XW7202 by C7292.

Critical

6.3V CASE-B2-SMPOLY-TANT 20%

6.3V CASE-B2-SMPOLY-TANT 20%

6.3V CASE-B2-SMPOLY-TANT 20%

33UF CRITICAL POLY-TANT CASED2E-SM 16V

Critical

Place XW7205 by Pin 1 OF L7220.

Place XW7201 by Pin 15 and Pin 24 of U7200.

Place XW7201 by Pin 15 and Pin 24 of U7200.

Place XW7201 by Pin 15 and Pin 24 of U7200.

Place XW7201 by Pin 15 and Pin 24 of U7200.

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Place XW7201 by Pin 15 and Pin 24 of U7200.

Place XW7201 by Pin 15 and Pin 24 of U7200.
1.5V/0.75V (DDR3) POWER SUPPLY

VOUT = 0.75V * (1 + RA / RB)

ROUTING NOTE:
- PUT 6 VIAS UNDER THE THERMAL PAD Q7321 PIN1,2,3
- CONNECT CS_GND TO USING KEVIN CONNECTION.

CRITICAL U7300 TPS51116

CRITICAL Q7320 SI7110DN PWRPK-1212-8-HF

CRITICAL Q7321 SI7108DN PWRPK-1212-8-HF

MAX CURRENT = 12A

PWM FREQ. = 400 KHZ

STATE
- PM_SLP_S4_L
- PM_SLP_S3_L
- PP1V5_S3
- PP0V75_S0

S0 | HIGH | HIGH | 1.5V | 0.75V
S3 | HIGH | LOW  | 1.5V | 0.0V
S5/G3HOT | LOW | LOW | 0.0V | 0.0V

1.5V/0.75V DDR3 SUPPLY

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CPUVTTS0 POWER SUPPLY

Place XW7600 between Pin 7 and Pin 15 of U7600.

ROUTING NOTE:

Place XW7601 by C7660.

Vout = 0.75V * (1 + Ra / Rb)

F = 400 KHZ

Q7620

Critical

SI7108DN
PWRPK-1212-8-HF

X5R
603-1
C7695
1UF
10%
25V

Critical

20%
16V
33UF

6.3V2
2
1
XW7665

Case-C2-SM
2.5V
20%

Critical

Case-D2E-SM
Poly-Tant

C7630

20%
16V
33UF

603-1
X7R

1UF
10%
25V

C7601

10%
64C1
64A5

R7601
6.65K
402
MF-LF
1%
1/16W
20.0K
1
R7603

MF-LF
1/16W
1%
402
1%
1/16W
20.0K
1

R7671

MF-LF
187K
2
1

R7604
6.65K
402
MF-LF
1%
1/16W
20.0K
1

C7696

50VCERM402
0.001UF
20%

2
1

C7661

SM-IHLP-1
1.0UH-13A-5.6M-OHM

L7620

1.0OH-13A-5.6M-OHM

Critical

SWITCH_NODE=TRUE

CPUVTTS0_LL

MIN_LINE_WIDTH=0.6MM

GATE_NODE=TRUE

MIN_NECK_WIDTH=0.2MM

CPUVTTS0_VBST

MIN_LINE_WIDTH=0.6MM

GATE_NODE=TRUE

MIN_NECK_WIDTH=0.2MM

VOLTAGE=0V

GND_CPUVTTS0_SGND

MIN_LINE_WIDTH=0.6MM

VOLTAGE=5V

MIN_NECK_WIDTH=0.2MM

PP5V_S0_CPUVTTS0_V5FILT

=PPCPUVTT_S0_REG

MIN_NECK_WIDTH=0.2MM

CPUVTTS0_TRIP

MIN_LINE_WIDTH=0.6MM

CPUVTTS0_PGOOD

MIN_LINE_WIDTH=0.6MM

CPUVTTS0_VOUT

MIN_LINE_WIDTH=0.6MM

CPUVTTS0_VFB

MIN_LINE_WIDTH=0.6MM

CPUVTTS0_DRVH

MIN_NECK_WIDTH=0.2MM

CPUVTTS0_DRVL

MIN_NECK_WIDTH=0.2MM

Critical

=CPUVTTS0_EN

A8D8 65A6
1.8V S0 SWITCHER

MCP 1.05V_S5 AUXC SUPPLY

MCP79 Rev A01 requires higher voltage

\[ V_{OUT} = 0.6V \times (1 + \frac{R_a}{R_b}) \]

\[ V_{OUT} = 1.102V \]

\( \text{MAX Current} = 1.5A \)

\( \text{FREQ} = 1\text{Mhz} \)

\[ R_{a} \]

\[ R_{b} \]

\( \text{MAX CURRENT} = 200\text{MA} \)

\( \text{INPUT RAIL IS 3.3V} \)

\( S0 \text{ SWITCHER} \)

\( \text{MCP 1.05V_S5 AUXC SUPPLY} \)

\( \text{CRITICAL} \)

\( \text{C7750} \)

\( \text{C7758} \)

\( \text{R7722} \)

\( \text{C7781} \)

\( \text{R7723} \)

\( \text{C7782} \)

\( \text{R7781} \)

\( \text{R7780} \)

\( \text{C7783} \)

\( \text{C7784} \)

\( \text{U7760} \)

\( \text{TPS62202} \)

\( \text{SYNC_DATE=01/23/2008} \)

\( \text{SYNC_MASTER=RAYMOND} \)

\( \text{MISC POWER SUPPLIES} \)

\( \text{PART NUMBER} \)

\( \text{QTY} \)

\( \text{DESCRIPTION} \)

\( \text{REFERENCE DES} \)

\( \text{CRITICAL} \)

\( \text{BOM OPTION} \)

\( \text{MCP_PROD} \)

\( \text{392K} \)

\( \text{56} \)

\( \text{1} \)

\( \text{21} \)

\( \text{2} \)

\( \text{6.3V} \)

\( \text{22UF} \)

\( \text{20\%} \)

\( \text{SOT23-5} \)

\( \text{53} \)

\( \text{4} \)

\( \text{SOT23-5} \)

\( \text{53} \)

\( \text{4} \)

\( \text{SOT23-5} \)

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\( \text{4} \)

\( \text{SOT23-5} \)

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\( \text{SOT23-5} \)

\( \text{53} \)

\( \text{4} \)

\( \text{SOT23-5} \)

\( \text{53} \)

\( \text{4} \)
MCP79 DDRVTT FET

MCP79 DDRVTT FET is a high voltage transistor that provides a dedicated power supply for DDR memory. It is used to regulate the voltage supplied to the DRAM (Dynamic Random Access Memory) devices. The purpose of this transistor is to ensure that the DDR memory operates within the specified voltage range to maintain data integrity and performance.

**Specifications:**
- **Model:** MCP79 DDRVTT
- **Rated Voltage:** 1.5V
- **Max Current:** 1.5A (EDP)
- **RDS(ON) 1.1A:** 26 MOHM @4.5V
- **RDS(ON) 1.431 A:** 26 MOHM @4.5V

**Application Notes:**
- Use the transistor to regulate the voltage supplied to DDR memory to ensure proper operation.
- The transistor can be used in conjunction with other components to provide a stable voltage supply for the DDR3 memory.

**Note:**
- Always consult the datasheet for detailed specifications and operating conditions.
- Ensure proper cooling and heat dissipation to prevent overheating.

APPLE INC.

SYNC_MASTER=YUAN.MA
SYNC_DATE=04/04/2008

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CRITICAL
3.3V S3 FET

CRITICAL
3.3V S0 FET

MCP79 DDRVTT FET

1.5V S0 FET

1.5V S0 FET

1.05V S0 FET

1.05V S0 FET

POWER FETS

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NOTE OF PROPRIETARY PROPERTY
DisplayPort Interoperability spec says that sources or sinks which do both DP and DVI must depend on the external adapter for pull up on DDC lines (since DP Display Port Interoperability spec says that sources AUX CH has 100K pull up/down on the MLB).
**Digital Video Signal Constraints**

- **Max length of LVDS/DisplayPort/TMDS traces**: 12 inches.
- **DisplayPort/TMDS intra-pair matching**: 5 ps. **Inter-pair matching** should be within 150 ps.
- **LVDS intra-pair matching**: 5 mils. **Pairs** should be within 100 mils of clock length.

---

**Physical Rule Set**

<table>
<thead>
<tr>
<th>Layer</th>
<th>Minimum Neck Width</th>
<th>Maximum Neck Length</th>
<th>DiffPair Primary Gap</th>
<th>DiffPair Neck Gap</th>
<th>Physical Rule Set</th>
</tr>
</thead>
<tbody>
<tr>
<td>SATA_100D_HDD</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
</tr>
<tr>
<td>SATA_100D</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
</tr>
<tr>
<td>MCP_DV_COMP</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
</tr>
<tr>
<td>LVDS_100D</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
</tr>
<tr>
<td>DP_100D</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
</tr>
<tr>
<td>CLK_PCIE_100D</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
</tr>
</tbody>
</table>

**Line-to-Line Spacing**

<table>
<thead>
<tr>
<th>Layer</th>
<th>Minimum Line Width</th>
<th>Allow Route</th>
</tr>
</thead>
<tbody>
<tr>
<td>SATA_HDD_D2R</td>
<td>*</td>
<td>*</td>
</tr>
<tr>
<td>SATA_TERMP</td>
<td>*</td>
<td>*</td>
</tr>
<tr>
<td>DP_ML</td>
<td>*</td>
<td>*</td>
</tr>
<tr>
<td>LVDS_ING_A_CLK</td>
<td>*</td>
<td>*</td>
</tr>
<tr>
<td>LVDS_100D</td>
<td>*</td>
<td>*</td>
</tr>
<tr>
<td>DP_AUX_CH</td>
<td>*</td>
<td>*</td>
</tr>
<tr>
<td>TMDS_ING_TXD</td>
<td>*</td>
<td>*</td>
</tr>
<tr>
<td>TMDS_ING_TXC</td>
<td>*</td>
<td>*</td>
</tr>
</tbody>
</table>

**Source:** MCP79 Interface DG (DG-03328-001_v0D), Section 2.4
PCI Bus Constraints

SIO Signal Constraints

SPI Interface Constraints

SMBus Interface Constraints

HD Audio Interface Constraints

LPC Bus Constraints
MCP RGMII (Ethernet) Constraints

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>55_OHM_SE</td>
<td>=100_OHM_DIFF</td>
<td>=100_OHM_DIFF</td>
<td>=100_OHM_DIFF</td>
<td>=100_OHM_DIFF</td>
<td>=100_OHM.Diff</td>
</tr>
<tr>
<td>C</td>
<td>33C4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B</td>
<td>33B6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A</td>
<td>33B6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

88E1116R (Ethernet PHY) Constraints

<table>
<thead>
<tr>
<th>Net Type</th>
<th>Electrical Constraint Set</th>
<th>Property</th>
<th>Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>ENET_MDI_100D</td>
<td>=100_OHM_DIFF</td>
<td></td>
<td>MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4</td>
</tr>
</tbody>
</table>

Ethernet Constraints
### M97 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

<table>
<thead>
<tr>
<th>TABLE BOARD_INFO</th>
<th>LAYER</th>
<th>MINIMUM LINE WIDTH</th>
<th>ALLOW ROUTE</th>
<th>MINIMUM LINE WIDTH</th>
<th>ALLOW ROUTE</th>
<th>MINIMUM LINE WIDTH</th>
<th>ALLOW ROUTE</th>
<th>MINIMUM LINE WIDTH</th>
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<th>MINIMUM LINE WIDTH</th>
<th>ALLOW ROUTE</th>
<th>MINIMUM LINE WIDTH</th>
<th>ALLOW ROUTE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>TOP</td>
<td>0.077 MM</td>
<td>0.330 MM</td>
<td>0.077 MM</td>
<td>0.330 MM</td>
<td>0.077 MM</td>
<td>0.330 MM</td>
<td>0.077 MM</td>
<td>0.330 MM</td>
<td>0.077 MM</td>
<td>0.330 MM</td>
<td>0.077 MM</td>
<td>0.330 MM</td>
</tr>
<tr>
<td></td>
<td>BOTTOM</td>
<td>0.112 MM</td>
<td>0.220 MM</td>
<td>0.112 MM</td>
<td>0.220 MM</td>
<td>0.112 MM</td>
<td>0.220 MM</td>
<td>0.112 MM</td>
<td>0.220 MM</td>
<td>0.112 MM</td>
<td>0.220 MM</td>
<td>0.112 MM</td>
<td>0.220 MM</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.126 MM</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### M97 RULE DEFINITIONS

- **SIZE**
  - **SCALE**
    - **NONE**
      - **SHT OF**
        - **051-7918 C**

- **REV.**
  - **APPLE INC.**

- **AREA_TYPE**
  - **SPACING_RULE_SET**
    - **NET_SPACING_TYPE1**
      - **NET_SPACING_TYPE2**

- **M97 RULE DEFINITIONS**
  - **SYNC_MASTER=M97_MLB**
  - **CLK_PCIE * BGA_P1MM BGA_P2MM**
  - **CLK_PCI * BGA_P2MM BGA_P1MM**
  - **MEM_CLK BGA_P1MM BGA_P2MM**
  - **FSB_DSTB BGA_P3MM FSB_DSTB BGA_P1MM**
  - **BGA_P1MM BGA_P1MM**
  - **BGA_P2MM **CLK_SLOW BGA_P1MM**

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