1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2012-01-12

D7 MLB

LAST_MODIFIED=Thu Jan 12 10:24:09 2012

Schematic / PCB #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-9509	1	SCH,MLB,D7	SCH	CRITICAL	
820-3302	1	PCBF,MLB,D7	PCB	CRITICAL	

DRAWING
TITLE=D7
ABBREV=DRAWING
LAST_MODIFIED=Thu Jan 12 10:24:09 2012

DRAWING TITLE: SCH,D7,MLB

Apple Inc.

DRAWING NUMBER: 051-9509 SIZE: D
REVISION: 4.2.0
BRANCH:
PAGE: 1 OF 113
SHEET: 1 OF 100

System Block diagram can be found on Kismet

PATH: Kismet > K70/72 > Block Diagrams > K70 Block Diagram

SYNC MASTER=K70 MLB SYNC DATE=11/30/2011

PAGE TITLE

System Block Diagram

Apple Inc.

DRAWING NUMBER 051-9509 SIZE D

REVISION 4.2.0

BRANCH

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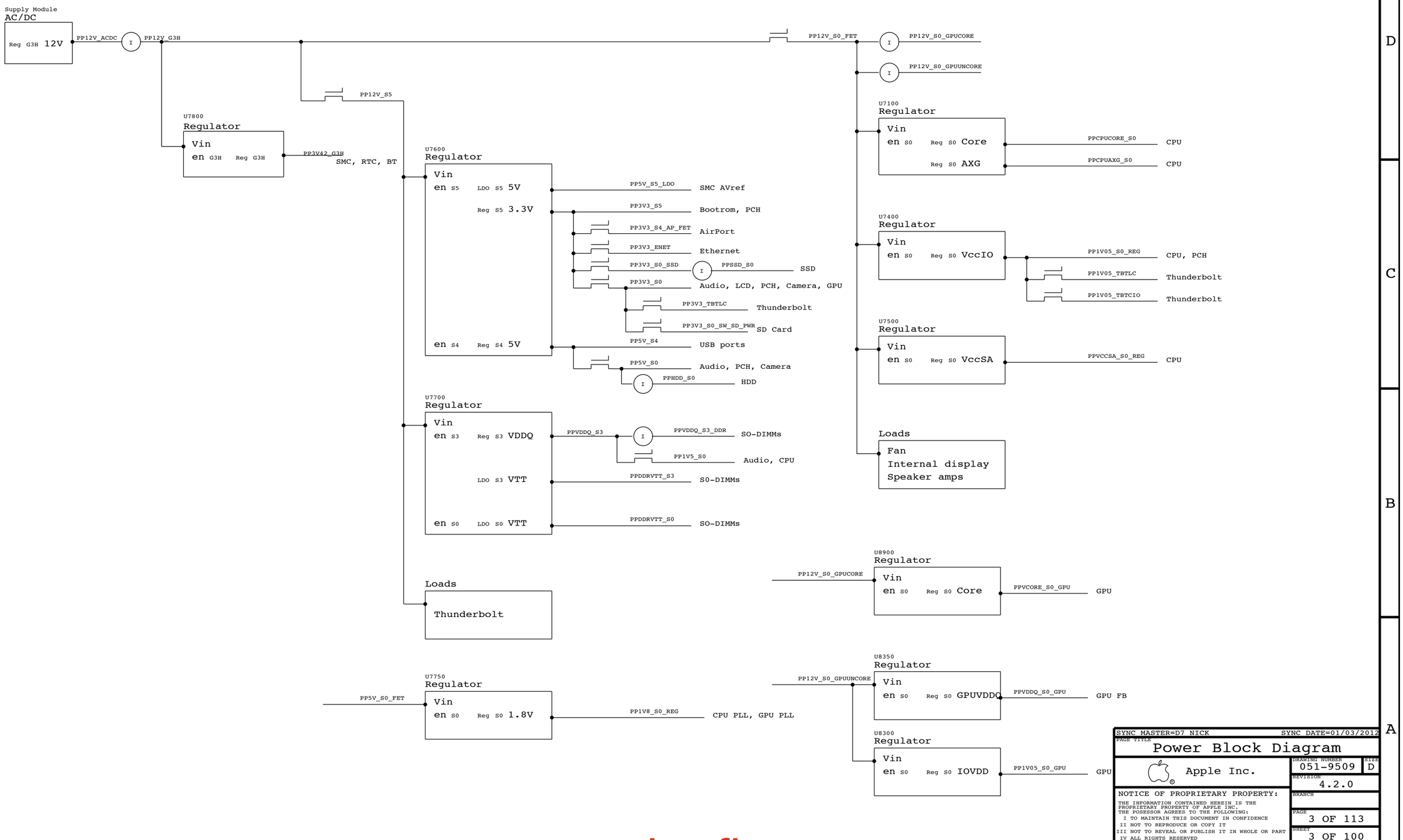

SYNC MASTER=D7 NICK SYNC DATE=01/03/2012

PAGE TITLE

Power Block Diagram

Apple Inc.

DRAWING NUMBER 051-9509 SIZE D

REVISION 4.2.0

BRANCH

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Main BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
085-4441	PCBA,MLB,DEV,D7	DEVELOPMENT,D7_DEVEL
639-3566	PCBA,MLB,D7,GSA,GOOD	D7_COMMON,CPU:GOOD,GPU:GSA,GS,FBA,SSD:N,EEEE:DF98
639-3668	PCBA,MLB,D7,GSB,GOOD	D7_COMMON,CPU:GOOD,GPU:GSB,GS,FBB,SSD:N,EEEE:F117
639-3567	PCBA,MLB,D7,GTX,BETTER	D7_COMMON,CPU:BETTER,GPU:107GTX,FBA,FBB,SSD:Y,EEEE:DT42
639-3665	PCBA,MLB,D7,GTX,CTO	D7_COMMON,CPU:CTO,GPU:107GTX,FBA,FBB,SSD:Y,EEEE:F116

Bar Code Labels / EEEE #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7122	1	MLB LABEL,48.0X4.8	EEEE_DF98	CRITICAL	EEEE:DF98
825-7122	1	MLB LABEL,48.0X4.8	EEEE_DT42	CRITICAL	EEEE:DT42
825-7122	1	MLB LABEL,48.0X4.8	EEEE_F116	CRITICAL	EEEE:F116
825-7122	1	MLB LABEL,48.0X4.8	EEEE_F117	CRITICAL	EEEE:F117

BOM Groups

BOM GROUP	BOM OPTIONS
D7_COMMON	COMMON,ALTERNATE,D7_COMMON1,D7_COMMON2,D7_PROGPARTS
D7_COMMON1	XDP,RSMRST:SMC,SPEAKERID,TBTHV:P12V
D7_COMMON2	SNS_CPUCORE:3PHASE,CPUCOREDRV:ISL6612,IG:N,GPU_ROM:YES,SNS_GPUS0:K70,SNS_VDDQS3_DDR:Y
D7_PROGPARTS	SMC:PROTO1,BOOTROM:PROG,T29ROM:PROG,CIVROM:PROG,CAMROM:PROG
D7_DEVEL	XDP_CONN,LPCPLUS,VREFMRGN:EXT,BKLT_PWM,DEVEL_SENSORS,DEVEL_AUDIO
DEVEL_SENSORS	SNS_VDDQS0_GPU:Y,SNS_VDDQS3:Y,TEMPSNSDEV
D7_PRODUCTION	SNS_VDDQS0_GPU:N,SNS_VDDQS3:N,VREFMRGN:N

Add 'K70_PRODUCTION' at RevA release

CPUs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4240	1	IVB,QC13,QS,E0,2.8G,65W,4+1,1.10,6M,LGA	CPU	CRITICAL	CPU:GOOD
337S4258	1	IVB,QC48,QS,E1,2.9G,65W,4+2,1.10,6M,LGA	CPU	CRITICAL	CPU:BETTER
337S4246	1	IVB,SR0PN,PRQ,E1,3.1G,65W,4+2,1.15,8M,LG	CPU	CRITICAL	CPU:CTO

Replace with 65W part

Module Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4234	1	IC,PCH,PPT-DT,Z77,QS,C1	U1800	CRITICAL	
338S1047	1	IC,TBT,CR-4C,ES1,288 FCBGA,12X12MM	U3600	CRITICAL	
337S4221	1	IC,GPU,NV,GK107-GS-2/1-QS-A	U8000	CRITICAL	GPU:GSA
337S4220	1	IC,GPU,NV,GK107-GS-2/1-QS-A	U8000	CRITICAL	GPU:GSB
337S4239	1	IC,GPU,NV,GK107-GTX-QS-A2	U8000	CRITICAL	GPU:107GTX
343S0592	1	IC,BCM57766,CIV+,A0,8X8	U3900	CRITICAL	
607-9432	1	K70,GDDR5,SAMSUNG	VRAM	CRITICAL	GPU:107GTX

Programmable Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S3493	1	IC,CR,V24.2,D7/D7I	U3690	CRITICAL	T29ROM:PROG
335S0865	1	IC,EEPROM,SERIAL,256KB,MLP8	U3690	CRITICAL	T29ROM:BLANK
335S0807	1	IC,64 MBIT SPI SERIAL FLASH	U5110	CRITICAL	BOOTROM:BLANK
341S3480	1	IC,PROGRMD,EFI ROM,K70	U5110	CRITICAL	BOOTROM:PROG
335S0862	1	IC,SERIAL FLASH,2MBIT,2.7V,REV F	U3990	CRITICAL	CIVROM:BLANK
341S3487	1	IC,ENET 1MBITFLASH,CIV,PVT,J40	U3990	CRITICAL	CIVROM:PROG
338S1098	1	IC,SMC12-A3,BLANK,D7	U4900	CRITICAL	SMC:BLANK
341S3484	1	IC,SMC,PROGRMD,PROTO1,D7	U4900	CRITICAL	SMC:PROTO1
341S3388	1	IC,SMC,PROGRMD,EVT,D7	U4900	CRITICAL	SMC:EVT
341S3389	1	IC,SMC,PROGRMD,DVT,D7	U4900	CRITICAL	SMC:DVT
341S3390	1	IC,SMC,PROGRMD,PVT,D7	U4900	CRITICAL	SMC:PVT
341S3409	1	IC,SMC,PROGRMD,PROD,D7	U4900	CRITICAL	SMC:PROD
341S3453	1	IC,CAMERA FLASH,K70/K72	U4202	CRITICAL	CAMROM:PROG
335S0852	1	IC,FLASH,SPI,1MBIT,3V3	U4202	CRITICAL	CAMROM:BLANK

Alternate: 335S0812

Alternate: 335S0854

Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0107	377S0126		ALL	USB diodes
157S0055	157S0058		ALL	Enet magnetics
376S1081	376S0975		ALL	P/NCh dual FET
341S3486	341S3487		ALL	P/NCh dual FET

CPU Socket

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0073	1	SOCKET,MOLEX,LGA1155,CPU-LF	U1000	CRITICAL	

CPU Socket Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
511S0071	511S0073		ALL	TYCO SOCKET
511S0072	511S0073		ALL	FOXCONN SOCKET

VRAM BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
607-9432	K70,GDDR5,SAMSUNG	FB:BOTH_SAMSUNG
607-9435	K70,GDDR5,HYNIX	FB:BOTH_HYNIX
607-9433	K70,GDDR5,SAMSUNG_CH1	FB:CH1_SAMSUNG
607-9436	K70,GDDR5,HYNIX_CH1	FB:CH1_HYNIX
607-9434	K70,GDDR5,SAMSUNG_CH2	FB:CH2_SAMSUNG
607-9437	K70,GDDR5,HYNIX_CH2	FB:CH2_HYNIX

VRAM Module Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0619	4	IC,8GRAM,GDDR5,32MX32,1.5GHz,G-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB:BOTH_SAMSUNG
333S0620	4	IC,GDDR5,32MX32,1.5GHZ,VEGA 44NM,B-DIE	U8400,U8450,U8500,U8550	CRITICAL	FB:BOTH_HYNIX
333S0631	2	IC,8GRAM,GDDR5,64MX32,4.2GBPS,D-DIE,HF	U8400,U8450	CRITICAL	FB:CH1_SAMSUNG
333S0630	2	IC,GDDR5,2GB,M-DIE,170B FBGA	U8400,U8450	CRITICAL	FB:CH1_HYNIX
333S0631	2	IC,8GRAM,GDDR5,64MX32,4.2GBPS,D-DIE,HF	U8500,U8550	CRITICAL	FB:CH2_SAMSUNG
333S0630	2	IC,GDDR5,2GB,M-DIE,170B FBGA	U8500,U8550	CRITICAL	FB:CH2_HYNIX

VRAM Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
607-9435	607-9432		VRAM	GDDR5_BOTH
607-9436	607-9433	GPU:GSA	VRAM	GDDR5_CH1
607-9437	607-9434	GPU:GSB	VRAM	GDDR5_CH2

GPU Module Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
607-9433	1	K70,GDDR5,SAMSUNG_CH1	VRAM	CRITICAL	GPU:GSA
607-9434	1	K70,GDDR5,SAMSUNG_CH2	VRAM	CRITICAL	GPU:GSB

Programmable Parts (unused)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0724	1	IC,1 MBIT SERIAL FLASH	U8701	CRITICAL	GPUROM:BLANK

SYNC MASTER=D7 NICK SYNC DATE=12/13/2011

PAGE TITLE: BOM Configuration

Apple Inc.

DRAWING NUMBER: 051-9509 SIZE: D

REVISION: 4.2.0

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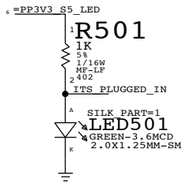
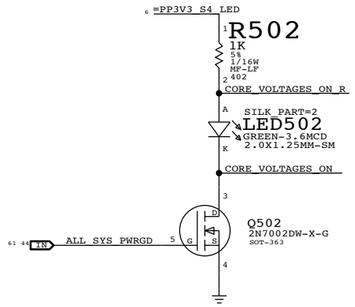
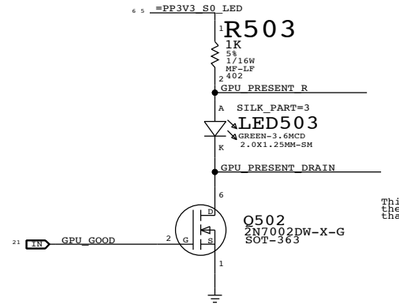
S5 Led



ALL_SYS_PWRGD Led

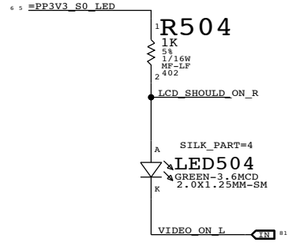


GPU GOOD Led



This LED is a GPIO driven from the southbridge that indicates that chipset has enumerated graphics

VIDEO ON Led



SYNC MASTER=K70 MLB SYNC DATE=11/30/2011

PAGE TITLE: DEBUG LEDS

Apple Inc.

DRAWING NUMBER: 051-9509 SIZE: D

REVISION: 4.2.0

BRANCH:

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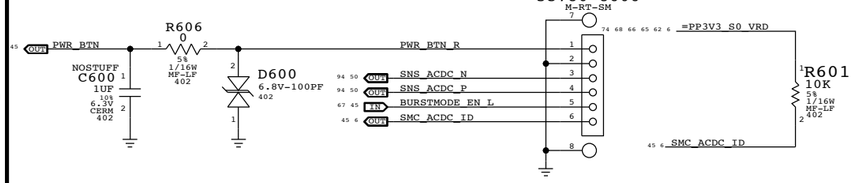
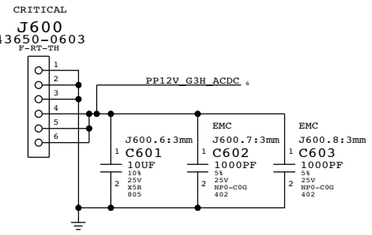
MLB to AC-DC Supplemental Signal Connector



MLB to AC-DC Connector



G3 Rails

Always on: Keeps the PCH RTC alive

PP3V3_G3	PP3V3_G3H_RTC	22 26
MAKE_BASE=TRUE VOLTAGE=3.3V NET_SPACING_TYPE=POWER MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM MAX_NECK_LENGTH=3MM	=PP3V3_G3_PCH	18 19

G3H Rails

97 PP12V_ACDC MAKE_BASE=TRUE	PP12V_G3H_ACDC	6
	=PP12V_G3H_SNS_R	48
97 PP12V_G3H MAKE_BASE=TRUE	PP12V_G3H_SNS	48
	=PP12V_G3H_REG_3V42_G3H	69
	=PP12V_G3H_FET_P12V_S5	69
	=PP12V_G3H_FET_P12V_S0	70
97 PP3V42_G3H MAKE_BASE=TRUE	PP3V42_G3H_REG	69
	=PP3V3_G3H_BT	33
	=PP3V3_G3H_SMC	44 45
	=PP3V3_RTC_D	26
	=PPVIN_G3H_SMCVREF	45
	=PP3V3_G3H_SMC_USBMUX	42

S5 Rails

Enabled when system has AC and is in S5

97 PP12V_S5 MAKE_BASE=TRUE	PP12V_S5_FET	69
	=PP12V_S5_REG_P3V3P5V_S5	67
	=PP12V_S5_REG_VDDQ_S3	68
	=PP12V_S5_PWRCTL	60 61 70
	=PPHV_SW_TBTAPWRSW	84
	=PPHV_SW_TBTBPWRSW	85
	=PP12V_S5_SNS	48
97 PP5V_S5 MAKE_BASE=TRUE	PP5V_S5_LDO	67
	=PP5V_S5_PWRCTL	67 70
	=PP5V_S5_PCH	24
97 PP3V3_S5 MAKE_BASE=TRUE	PP3V3_S5_REG	67
	=PP3V3_S5_LDO_P1V05_S5	67
	=PP3V3_S5_FET_P3V3_S4	70
	=PP3V3_S5_FET_P3V3_S0	70
	=PP3V3_S5_PWRCTL	60 61 70 78
	=PP3V3_S5_VRD	67 68
	=PP3V3_S5_LED	5
	=PP3V3_S5_LPCPLUS	46
	=PP3V3_S5_PCH	19 24 26
	=PP3V3_S5_PCH_STRAPS	15
	=PP3V3_S5_PCH_VCC_DSW	22 24
	=PP3V3_S5_PCH_VCC_SPI	22 24
	=PP3V3_S5_PCH_VCCSUS_HDA	22 24
	=PP3V3_S5_PCH_VCCSUS_USB	22 24
	=PP3V3_S5_ROM	46
	=PP3V3_S5_SENSE	48
	=PP3V3_S5_SMC	45
	=PP3V3_S5_USBMUX	42 43
	=PP3V3_S5_XDP	25

S4 Rails

Enabled when system has AC and is in run or sleep

97 PP5V_S4 MAKE_BASE=TRUE	PP5V_S4_REG	67
	=PP5V_S4_REG_VDDQ_S3	68
	=PP5V_S4_FET_P5V_S0	70
	=PP5V_S4_MEMRESET	28
	=PP5V_S4_PWRCTL	70
	=PP5V_S4_USB	42 43
97 PP3V3_S4 MAKE_BASE=TRUE	PP3V3_S4_FET	70
	=PP3V3_S4_FET_ENET	38
	=PP3V3_S4_PWRCTL	70
	=PP3V3_S4_ALS	40
	=PP3V3_S4_AP	33
	=PP3V3_S4_LED	5
	=PP3V3_S4_MEMRESET	28
	=PP3V3_S4_PCH	15
	=PP3V3_S4_PM	28
	=PP3V3_S4_SDCARD	15 39
	=PP3V3_S4_SMC	45
	=PP3V3_S4_SMBUS_SMC_2	47
	=PP3V3_S4_TBT	34 35 36 84 85
	=PP3V3_S4_TBTAPWRSW	45 84
	=PP3V3_S4_TBTBPWRSW	45 85
	=PP3V3_S4_USB_HUB	27
	=PP3V3_S4_VREFMRGN	32

S3 Rails

Enabled when system is in run or sleep

97 PP3V3_ENET MAKE_BASE=TRUE	PP3V3_ENET_FET	38
	=PP3V3_ENET_PHY	37 38
	=PP3V3_ENET_SYSCLK	26
	=PPVDDIO_ENET_CLK	26
95 PPVDDQ_S3 MAKE_BASE=TRUE	PPVDDQ_S3_REG	68
	=PPVDDQ_S3_FET_VDDQ_S0	70
	=PPVDDQ_S3_LDO_DDRVTT	68
	=PPVDDQ_S3_SNS_DDR_R	49
	=PPVDDQ_S3_VSNS	
95 PPVDDQ_S3_DDR MAKE_BASE=TRUE	PPVDDQ_S3_SNS_DDR	49
	=PPVDDQ_S3_DDR_VREF	32
	=PPVDDQ_S3_MEM_A	29
	=PPVDDQ_S3_MEM_B	30
	=PPVDDQ_S3_MEMRESET	28
95 PPDDRVTT_S3 MAKE_BASE=TRUE	PPDDRVTT_S3_LDO	68
	=PPDDRVTT_S3_VREFCA	32

S0 Rails

Enabled when system is in run

97 PP12V_S0 MAKE_BASE=TRUE	PP12V_S0_FET	70
	=PP12V_S0_REG_CPUCORE_S0	63
	=PP12V_S0_REG_VCCSA_S0	66
	=PP12V_S0_REG_P1V05_S0	65
	=PP12V_S0_SNS_GPUCORE_R	48
	=PP12V_S0_SNS_GPUUNCORE_R	48
	=PP12V_S0_AUDIO_SPKRAMP	54 55
	=PP12V_S0_BKLT	86
	=PP12V_S0_FAN	51
	=PP12V_S0_LCD	81
97 PP12V_S0_GPUCORE MAKE_BASE=TRUE	PP12V_S0_SNS_GPUCORE	48
	=PP12V_S0_REG_GPUCORE_S0	80
97 PP12V_S0_GPUUNCORE MAKE_BASE=TRUE	PP12V_S0_SNS_GPUUNCORE	48
	=PP12V_S0_REG_GPU_P1V05_S0	74
	=PP12V_S0_REG_GPU_VDDQ_S0	74
97 PPHDD_S0 MAKE_BASE=TRUE	PPHDD_S0_SNS	48
	=PP5V_S0_SATA	41
97 PP5V_S0 MAKE_BASE=TRUE	PP5V_S0_FET	70
	=PP5V_S0_REG_CPUCORE_S0	62
	=PP5V_S0_REG_VCCSA_S0	66
	=PP5V_S0_REG_P1V05_S0	65
	=PP5V_S0_REG_GPU_P1V05_S0	74
	=PP5V_S0_REG_P1V8_S0	68
	=PP5V_S0_REG_GPUCORE_S0	80
	=PP5V_S0_REG_GPU_VDDQ_S0	74
	=PP5V_S0_VRD	68
	=PP5V_S0_AUDIO	52 59
	=PP5V_S0_CAMERA	40
	=PP5V_S0_ISENSE	48
	=PP5V_S0_LPCPLUS	46
	=PP5V_S0_PCH	24
	=PP5V_S0_BKLT	86
	=PPHDD_S0_SNS_R	48
97 PP3V3_S0 MAKE_BASE=TRUE	PP3V3_S0_FET	70
	=PP3V3_S0_P3V3TBTFET	36
	=PP3V3_S0_PWRCTL	70 80
	=PP3V3_S0_VRD	6 62 65 66 68 74
	=PP3V3_S0_AUDIO	40 52 54 55 58
	=PP3V3_S0_AUDIO_DIG	56
	=PP3V3_S0_BT	33
	=PP3V3_S0_CAMERA	40
	=PP3V3_S0_DP	47 81 83
	=PP3V3_S0_ENET	37
	=PP3V3_S0_FAN	51
	=PP3V3_S0_INTDPMUX	82
	=PP3V3_S0_LED	5
	=PP3V3_S0_LED_SATA	15 41
	=PP3V3_S0_PCH	18 21 24
	=PP3V3_S0_PCH_GPIO	15 19 20 36
	=PP3V3_S0_PCH_PM	26
	=PP3V3_S0_PCH_STRAPS	15
	=PP3V3_S0_PCH_VCC	22 24
	=PP3V3_S0_PCH_VCC_ADAC	17
	=PP3V3_S0_PCH_VCC_GPIO	22 24
	=PP3V3_S0_PCH_VCC_HVCMOS	22 24
	=PP3V3_S0_PCH_VCC_PCI	22 24
	=PP3V3_S0_RSTBUF	26
	=PP3V3_S0_SDCARD	39
	=PP3V3_S0_SENSE	41 48 49 50
	=PP3V3_S0_SMBUS	47
	=PP3V3_S0_SMBUS_SMC_0	47
	=PP3V3_S0_SMBUS_SMC_1	47
	=PP3V3_S0_SMBUS_SMC_3	47
	=PP3V3_S0_SMC	45
	=PP3V3_S0_TBTPWRCTL	36
	=PP3V3_S0_BKLT_VDDIO	86
	=PP3V3_GPU_IFPX_PLLVDD	77
	=PP3V3_GPU_MISC	77 80
	=PP3V3_GPU_VDD33	71 77 78 79
	=PPSPD_S0_MEM_A	29
	=PPSPD_S0_MEM_B	30
97 PP3V3_S0_SSD MAKE_BASE=TRUE	PP3V3_S0_SSD_FET	70
	=PPSSD_S0_SNS_R	49
97 PPSSD_S0 MAKE_BASE=TRUE	PPSSD_S0_SNS	49
	=PP3V3_S0_SSD	41
	=PP3V3_S0_SATAMUX	41
97 PP1V8_S0 MAKE_BASE=TRUE	PP1V8_S0_REG	68
	=PP1V8_S0_CAMERA	40
	=PP1V8_S0_CPU_PLL	13 16
	=PP1V8_S0_PCH	19
	=PP1V8_S0_PCH_VCC_DFTERM	22 24
	=PP1V8_S0_PCH_VCC_VRM	24
	=PPVDDIO_S0_SBCLK	26
	=PP1V8_S0_GPUVID	80
	=PP1V8_S0_ENET	38

95 PP1V5_S0 MAKE_BASE=TRUE	PP1V5_S0_FET	70
	=PP1V5_S0_CPU_MEM	11 13 16
	=PP1V5_S0_AUD_DIG	52
	=PP1V5_S0_SENSE	41
95 PPDDRVTT_S0 MAKE_BASE=TRUE	PPDDRVTT_S0_LDO	68
	=PPDDRVTT_S0_CLAMP	28
	=PPDDRVTT_S0_MEM_A	29
	=PPDDRVTT_S0_MEM_B	30
97 PPDDRVREF_DQ_MEM_A_S3 MAKE_BASE=TRUE	PPDDRVREF_DQ_MEM_A	32
	=PPDDRVREF_DQ_MEM_A	29
97 PPDDRVREF_CA_MEM_A_S3 MAKE_BASE=TRUE	PPDDRVREF_CA_MEM_A	32
	=PPDDRVREF_CA_MEM_A	29
97 PPDDRVREF_DQ_MEM_B_S3 MAKE_BASE=TRUE	PPDDRVREF_DQ_MEM_B	32
	=PPDDRVREF_DQ_MEM_B	30
97 PPDDRVREF_CA_MEM_B_S3 MAKE_BASE=TRUE	PPDDRVREF_CA_MEM_B	32
	=PPDDRVREF_CA_MEM_B	30
95 PP1V05_S0 MAKE_BASE=TRUE	PP1V05_S0_REG	65
	=PP1V05_S0_DP	
	=PP1V05_S0_P1V05TBTFET	36
	=PP1V05_S0_PCH	18 24
	=PP1V05_S0_PCH_VCC_ADPLL	17
	=PP1V05_S0_PCH_VCC_ASW	22 24
	=PP1V05_S0_PCH_VCC_CORE	22 24
	=PP1V05_S0_PCH_VCC_DMI	22 24
	=PP1V05_S0_PCH_VCC_DIFFCLK	22
	=PP1V05_S0_PCH_VCC_SSC	22
	=PP1V05_S0_PCH_VCCIO_DMI	22
	=PP1V05_S0_PCH_VCCIO_PCIE	18 19 22
	=PP1V05_S0_PCH_VCCIO_SATA	18 22 24
	=PP1V05_S0_PCH_VCCIO_USB	22
	=PP1V05_S0_PCH_V_PROC_IO	22 24
	=PPVCCIO_S0_CPU	10 11 13 16 62
	=PPVCCIO_S0_SMC	45
	=PPVCCIO_S0_XDP	25
96 PPVCORE_S0_CPU MAKE_BASE=TRUE	PPCPUCORE_S0_REG	63
	=PPVCORE_S0_CPU	13 16 48 62
96 PPVAXG_S0 MAKE_BASE=TRUE	PPCPUAXG_S0_REG	64
	=PPVAXG_S0_CPU	13 17 48 62
95 PPVCCSA_S0 MAKE_BASE=TRUE	PPVCCSA_S0_REG	66
	=PPVCCSA_S0_CPU	13 16

Thunderbolt Rails (S0)

Enabled when Thunderbolt cable is plugged in

97 PP3V3_TBTLC MAKE_BASE=TRUE	=PP3V3_TBTLC_FET	36
	=PP3V3_TBT_PCH_GPIO	15
	=PP3V3_TBTLC_RTR	34 35 36
	=PPVDDIO_TBT_CLK	26
95 PP1V05_TBTLC MAKE_BASE=TRUE	=PP1V05_TBTLC_FET	36
	=PP1V05_TBTLC_RTR	35 36
95 PP1V05_TBTCIO MAKE_BASE=TRUE	=PP1V05_TBTCIO_FET	36
	=PP1V05_TBTCIO_RTR	35

GPU Rails (S0)

Enabled when system is in run

97 PPVCORE_S0_GPU MAKE_BASE=TRUE	PPGPUCORE_S0_REG	80
	=PPVCORE_GPU	72 79
97 PP1V05_S0_GPU MAKE_BASE=TRUE	PP1V05_S0_GPU_REG	74
	=PP1V05_GPU_IFPCD_IOVDD	77
	=PP1V05_GPU_IFPEF_IOVDD	77
	=PP1V05_GPU_PEX_IOVDD	73 79
	=PP1V05_GPU_PEX_PLLVDD	77 79
97 PPVDDQ_S0_GPU MAKE_BASE=TRUE	PP1V5R1V35_S0_GPU_REG	74
	=PP1V35_GPU_FBVDDQ	72 75 76
	=PP1V35_GPU_S0_FB	73

Ground/Common

GND
MAKE_BASE=TRUE

SYNC_MASTER=D7 NICK SYNC_DATE=01/11/2012

PAGE TITLE
Power Connectors/Aliases

Apple Inc.

DRAWING NUMBER 051-9509 SIZE D
REVISION 4.2.0
BRANCH
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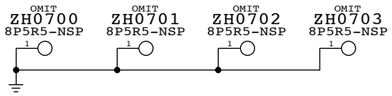
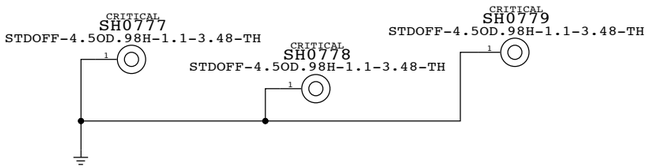
CPU Heatsink

4mm Plated Holes (998-0850)



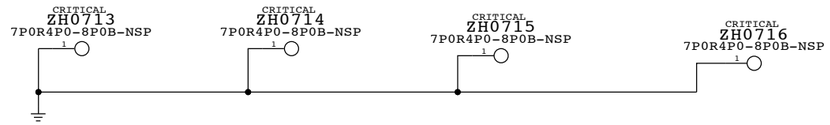
GPU HEATSINK MOUNTING FEATURES

(860-0988)



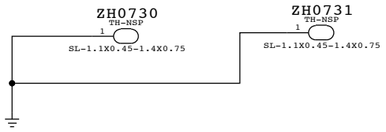
Rear Cover

998-4559 (Plated holes, 4mm inner diameter, 8mm pad)



USB Can holes

998-3975 (Plated slot holes, 1.10mm x 0.45mm)



WIRELESS CARD MTG HOLES

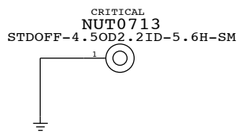
998-4560 (Plated holes, 2.3mm inner diameter, 4.3mm pad)

POGO PINS

APN: 870-1939

SSD STANDOFF

APN: 860-1461



SYNC MASTER=K70 MLB SYNC DATE=11/30/2011

PAGE TITLE

Holes/PD parts

Apple Inc.

DRAWING NUMBER 051-9509 SIZE D

REVISION 4.2.0

BRANCH

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CPU Reserved

10	TP_CPU_RSVD<16..1>	NC_CPU_RSVD<16..1>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_CPU_RSVD<46..19>	NC_CPU_RSVD<46..19>	MAKE_BASE=TRUE NO_TEST=TRUE
91 10	CPU_CFG<15..12>	TP_CPU_CFG<15..12>	MAKE_BASE=TRUE

CPU Memory

12	TP_MEM_A_DQ_CB<7..0>	NC_MEM_A_DQ_CB<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_A_DQS_N<8>	NC_MEM_A_DQSN<8>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_A_DQS_P<8>	NC_MEM_A_DQSP<8>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_B_DQ_CB<7..0>	NC_MEM_B_DQ_CB<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_B_DQS_N<8>	NC_MEM_B_DQSN<8>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_B_DQS_P<8>	NC_MEM_B_DQSP<8>	MAKE_BASE=TRUE NO_TEST=TRUE
88 12	MEM_A_CLK_N<2..3>	NC_MEM_A_CLKN<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
88 12	MEM_A_CLK_P<2..3>	NC_MEM_A_CLKP<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
88 12	MEM_A_CS_L<2..3>	NC_MEM_A_CS_L<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
88 12	MEM_A_CKE<2..3>	NC_MEM_A_CKE<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
88 12	MEM_B_CLK_N<2..3>	NC_MEM_B_CLKN<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
88 12	MEM_B_CLK_P<2..3>	NC_MEM_B_CLKP<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
88 12	MEM_B_CS_L<2..3>	NC_MEM_B_CS_L<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
88 12	MEM_B_CKE<2..3>	NC_MEM_B_CKE<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
88 12	MEM_A_ODT<2..3>	NC_MEM_A_ODT<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
88 12	MEM_B_ODT<2..3>	NC_MEM_B_ODT<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE

PCH USB

20	USB_PCH_4_N	NC_USB_PCH_4_N	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_4_P	NC_USB_PCH_4_P	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_5_N	NC_USB_PCH_5_N	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_5_P	NC_USB_PCH_5_P	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_6_N	NC_USB_PCH_6_N	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_6_P	NC_USB_PCH_6_P	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_11_N	NC_USB_PCH_11_N	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_11_P	NC_USB_PCH_11_P	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_12_N	NC_USB_PCH_12_N	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_12_P	NC_USB_PCH_12_P	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_13_N	NC_USB_PCH_13_N	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_13_P	NC_USB_PCH_13_P	MAKE_BASE=TRUE NO_TEST=TRUE

PCH PLL

22	PP1V05_S0_PCH_VCCAPLLDMI2	NC_PP1V05_S0_PCH_VCCAPLLDMI2	MAKE_BASE=TRUE NO_TEST=TRUE
22	PP1V05_S0_PCH_VCCAPLL_EXP	NC_PP1V05_S0_PCH_VCCAPLL_EXP	MAKE_BASE=TRUE NO_TEST=TRUE
22	PP1V05_S0_PCH_VCCAPLL_SATA	NC_PP1V05_S0_PCH_VCCAPLL_SATA	MAKE_BASE=TRUE NO_TEST=TRUE

PCH Clocks

18	TP_PCIE_CLK100M_PE4N	NC_PCIE_CLK100M_PE4N	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_CLK100M_PE4P	NC_PCIE_CLK100M_PE4P	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE6N	NC_PCIE_CLK100M_PE6N	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE6P	NC_PCIE_CLK100M_PE6P	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE7N	NC_PCIE_CLK100M_PE7N	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE7P	NC_PCIE_CLK100M_PE7P	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_TX_N<3..0>	NC_PE_TXN<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_TX_P<3..0>	NC_PE_TXP<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_RX_N<3..0>	NC_PE_RXN<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_RX_P<3..0>	NC_PE_RXP<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
18	DMI_MIDBUS_CLK100M_N	NC_DMI_MIDBUS_CLK100N	MAKE_BASE=TRUE NO_TEST=TRUE
18	DMI_MIDBUS_CLK100M_P	NC_DMI_MIDBUS_CLK100P	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_CLKOUT_PEG_A_N	NC_CLKOUT_PEG_AN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_CLKOUT_PEG_A_P	NC_CLKOUT_PEG_AP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CLKOUT_DPN	NC_PCH_CLKOUT_DPN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CLKOUT_DPP	NC_PCH_CLKOUT_DPP	MAKE_BASE=TRUE NO_TEST=TRUE
18	PCH_CLK25M_XTALOUT	NC_PCH_CLK25M_XTALOUT	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_GPIO64_CLKOUTFLEX0	NC_PCH_GPIO64_CLKOUTFLEX0	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_GPIO65_CLKOUTFLEX1	NC_PCH_GPIO65_CLKOUTFLEX1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_GPIO66_CLKOUTFLEX2	NC_PCH_GPIO66_CLKOUTFLEX2	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_GPIO67_CLKOUTFLEX3	NC_PCH_GPIO67_CLKOUTFLEX3	MAKE_BASE=TRUE NO_TEST=TRUE

PCH and CPU FDI

91 10	CPU_FDI_TX_N<7..0>	NC_CPU_FDI_TXN<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
91 10	CPU_FDI_TX_P<7..0>	NC_CPU_FDI_TXP<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	PCH_FDI_RX_N<7..0>	NC_PCH_FDI_RXN<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	PCH_FDI_RX_P<7..0>	NC_PCH_FDI_RXP<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
91 10	CPU_FDI_FSYNC<1..0>	NC_CPU_FDI_FSYNC<1..0>	MAKE_BASE=TRUE NO_TEST=TRUE
91 10	CPU_FDI_LSYNC<1..0>	NC_CPU_FDI_LSYNC<1..0>	MAKE_BASE=TRUE NO_TEST=TRUE
91 10	CPU_FDI_INT	NC_CPU_FDI_INT	MAKE_BASE=TRUE NO_TEST=TRUE
19	PCH_FDI_FSYNC<1..0>	NC_PCH_FDI_FSYNC<1..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	PCH_FDI_LSYNC<1..0>	NC_PCH_FDI_LSYNC<1..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	PCH_FDI_INT	NC_PCH_FDI_INT	MAKE_BASE=TRUE NO_TEST=TRUE

PCH Unused Display

19	TP_CRT_IG_RED	NC_CRT_IG_RED	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_GREEN	NC_CRT_IG_GREEN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_BLUE	NC_CRT_IG_BLUE	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_HSYNC	NC_CRT_IG_HSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_VSYNC	NC_CRT_IG_VSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_DDC_CLK	NC_CRT_IG_DDC_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_DDC_DATA	NC_CRT_IG_DDC_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_MLN<3..0>	NC_DP_IG_B_MLN<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_MLP<3..0>	NC_DP_IG_B_MLP<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_AUX_N	NC_DP_IG_B_AUXN	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_AUX_P	NC_DP_IG_B_AUXP	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_HPD	NC_DP_IG_B_HPD	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_DDC_CLK	NC_DP_IG_B_CTRL_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_DDC_DATA	NC_DP_IG_B_CTRL_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_MLN<3..0>	NC_DP_IG_C_MLN<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_MLP<3..0>	NC_DP_IG_C_MLP<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_AUX_N	NC_DP_IG_C_AUXN	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_AUX_P	NC_DP_IG_C_AUXP	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_HPD	NC_DP_IG_C_HPD	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_CTRL_CLK	NC_DP_IG_C_CTRL_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_CTRL_DATA	NC_DP_IG_C_CTRL_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_MLN<3..0>	NC_DP_IG_D_MLN<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_MLP<3..0>	NC_DP_IG_D_MLP<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_AUXN	NC_DP_IG_D_AUXN	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_AUXP	NC_DP_IG_D_AUXP	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_HPD	NC_DP_IG_D_HPD	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_CTRL_CLK	NC_DP_IG_D_CTRL_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_CTRL_DATA	NC_DP_IG_D_CTRL_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_TVCLKINN	NC_SDVO_TVCLKINN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_TVCLKINP	NC_SDVO_TVCLKINP	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_STALLN	NC_SDVO_STALLN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_STALLP	NC_SDVO_STALLP	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_INTN	NC_SDVO_INTN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_INTP	NC_SDVO_INTP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_L_BKLTCTL	NC_PCH_L_BKLTCTL	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_L_BKLTEN	NC_PCH_L_BKLTEN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_L_VDD_EN	NC_PCH_L_VDD_EN	MAKE_BASE=TRUE NO_TEST=TRUE

UNUSED GRAPHICS ALIASES

	TP_DVPCNTL_M<0..1>	NC_DVPCNTL_M<0..1>	MAKE_BASE=TRUE NO_TEST=TRUE
	TP_DVPCNTL<0..2>	NC_DVPCNTL<0..2>	MAKE_BASE=TRUE NO_TEST=TRUE
	TP_DVPCLK	NC_DVPCLK	MAKE_BASE=TRUE NO_TEST=TRUE
	TP_DVPDATA<4..23>	NC_DVPDATA<4..23>	MAKE_BASE=TRUE NO_TEST=TRUE
	HDMI_EG_CLK_C_P	NC_HDMI_EG_CLK_C_P	MAKE_BASE=TRUE NO_TEST=TRUE
	HDMI_EG_CLK_C_N	NC_HDMI_EG_CLK_C_N	MAKE_BASE=TRUE NO_TEST=TRUE
	HDMI_EG_DDC_CLK	NC_HDMI_EG_DDC_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
	HDMI_EG_DDC_DATA	NC_HDMI_EG_DDC_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
	HDMI_EG_DATA_C_P<0..2>	NC_HDMI_EG_DATA_C_P<0..2>	MAKE_BASE=TRUE NO_TEST=TRUE
	HDMI_EG_DATA_C_N<0..2>	NC_HDMI_EG_DATA_C_N<0..2>	MAKE_BASE=TRUE NO_TEST=TRUE
77	GPU_TDIODE_P	NC_GPU_TDIODE_P	MAKE_BASE=TRUE NO_TEST=TRUE
77	GPU_TDIODE_N	NC_GPU_TDIODE_N	MAKE_BASE=TRUE NO_TEST=TRUE
78	EG_LCD_PWR_EN	NC_EG_LCD_PWR_EN	MAKE_BASE=TRUE NO_TEST=TRUE

PCH SATA

18	TP_SATA_C_R2D_CN	NC_SATA_C_R2D_CN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_C_R2D_CP	NC_SATA_C_R2D_CP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_C_D2RN	NC_SATA_C_D2RN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_C_D2RP	NC_SATA_C_D2RP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_D_R2D_CN	NC_SATA_D_R2D_CN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_D_R2D_CP	NC_SATA_D_R2D_CP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_D_D2RN	NC_SATA_D_D2RN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_D_D2RP	NC_SATA_D_D2RP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_E_R2D_CN	NC_SATA_E_R2D_CN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_E_R2D_CP	NC_SATA_E_R2D_CP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_E_D2RN	NC_SATA_E_D2RN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_E_D2RP	NC_SATA_E_D2RP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_F_R2D_CN	NC_SATA_F_R2D_CN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_F_R2D_CP	NC_SATA_F_R2D_CP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_F_D2RN	NC_SATA_F_D2RN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_F_D2RP	NC_SATA_F_D2RP	MAKE_BASE=TRUE NO_TEST=TRUE

PCH Reserved

19	TP_PCH_RESERVE_0	NC_PCH_RESERVE_0	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_1	NC_PCH_RESERVE_1	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_2	NC_PCH_RESERVE_2	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_3	NC_PCH_RESERVE_3	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_4	NC_PCH_RESERVE_4	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_5	NC_PCH_RESERVE_5	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_6	NC_PCH_RESERVE_6	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_7	NC_PCH_RESERVE_7	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_8	NC_PCH_RESERVE_8	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_9	NC_PCH_RESERVE_9	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_10	NC_PCH_RESERVE_10	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_11	NC_PCH_RESERVE_11	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_12	NC_PCH_RESERVE_12	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_13	NC_PCH_RESERVE_13	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_14	NC_PCH_RESERVE_14	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_15	NC_PCH_RESERVE_15	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_16	NC_PCH_RESERVE_16	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_17	NC_PCH_RESERVE_17	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_18	NC_PCH_RESERVE_18	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_19	NC_PCH_RESERVE_19	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_20	NC_PCH_RESERVE_20	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_21	NC_PCH_RESERVE_21	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_22	NC_PCH_RESERVE_22	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_23	NC_PCH_RESERVE_23	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_24	NC_PCH_RESERVE_24	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_25	NC_PCH_RESERVE_25	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_26	NC_PCH_RESERVE_26	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_27	NC_PCH_RESERVE_27	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_28	NC_PCH_RESERVE_28	MAKE_BASE=TRUE NO_TEST=TRUE

PCH Test Points

21	TP_PCH_TP1	NC_PCH_TP1	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP2	NC_PCH_TP2	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP3	NC_PCH_TP3	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP4	NC_PCH_TP4	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP5	NC_PCH_TP5	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP6	NC_PCH_TP6	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP7	NC_PCH_TP7	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP8	NC_PCH_TP8	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP9	NC_PCH_TP9	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP10	NC_PCH_TP10	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP11	NC_PCH_TP11	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP12	NC_PCH_TP12	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP13	NC_PCH_TP13	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP14	NC_PCH_TP14	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP15	NC_PCH_TP15	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP16	NC_PCH_TP16	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP17	NC_PCH_TP17	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP18	NC_PCH_TP18	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP19	NC_PCH_TP19	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP20	NC_PCH_TP20	MAKE_BASE=TRUE NO_TEST=TRUE

PCH PCI

20	TP_PCI_AD<31..0>	NC_PCI_AD<31..0>	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_C_BE_L<3..0>	NC_PCI_C_BE_L<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_PAR	NC_PCI_PAR	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_RESET_L	NC_PCI_RESET_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_INIT3V3_L	NC_PCH_INIT3V3_L	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_LPC_DREQ0_L	NC_LPC_DREQ0_L	MAKE_BASE=TRUE NO_TEST=TRUE

PCH Miscellaneous

18	TP_HDA_SDIN1	NC_HDA_SDIN1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_HDA_SDIN2	NC_HDA_SDIN2	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_HDA_SDIN3	NC_HDA_SDIN3	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM0	NC_PCH_PWM0	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM1	NC_PCH_PWM1	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM2	NC_PCH_PWM2	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM3	NC_PCH_PWM3	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_SST	NC_PCH_SST	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CL_CLK1	NC_PCH_CL_CLK1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CL_DATA1	NC_PCH_CL_DATA1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CL_RST1	NC_PCH_CL_RST1	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_CLK33M_OUT2	NC_PCI_CLK33M_OUT2	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_CLK33M_OUT3	NC_PCI_CLK33M_OUT3	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_GPIO8	NC_PCH_GPIO8	MAKE_BASE=TRUE NO_TEST=TRUE
22	PP1V05_S0_PCH_FDIPLL	NC_PP1V05_S0_PCH_FDIPLL	MAKE_BASE=TRUE NO_TEST=TRUE
22	PP1V05_S0_PCH_VCC_A_CLK	NC_PP1V05_S0_PCH_VCC_A_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
22	TP_PPVOUT_PCH_DCPSUSBYP	NC_PPVOUT_PCH_DCPSUSBYP	MAKE_BASE=TRUE NO_TEST=TRUE

SYNC_MASTER=K70_MLB SYNC_DATE=11/30/2011

PAGE TITLE: Unused Signal Aliases

Apple Inc.

DRAWING NUMBER: 051-9509 SIZE: D

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Whistler aliases

89 71 PEG_D2R_N<0..15> ═══ =PEG_D2R_N<15..0> 10
MAKE_BASE=TRUE

89 71 PEG_D2R_P<0..15> ═══ =PEG_D2R_P<15..0> 10
MAKE_BASE=TRUE

89 71 PEG_R2D_C_N<0..15> ═══ =PEG_R2D_C_N<15..0> 10
MAKE_BASE=TRUE

89 71 PEG_R2D_C_P<0..15> ═══ =PEG_R2D_C_P<15..0> 10
MAKE_BASE=TRUE

SYNC MASTER=K70 MLB SYNC DATE=11/30/2011

PAGE TITLE
Signal Aliases

Apple Inc.

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SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLE 4 MIL TRACE TO R1010.1
ROUTE B5 TO R1010.1 AS A SEPERATE 10 MIL TRACE.

OMIT TABLE
U1000
IVY-BRIDGE
BGA-SKT-K70
SYM 1 OF 10

DMI
DMI_RX_0* W4
DMI_RX_1* V4
DMI_RX_2* Y4
DMI_RX_3* AA5
DMI_RX_0 W5
DMI_RX_1 V3
DMI_RX_2 Y3
DMI_RX_3 AA4
DMI_TX_0* V6
DMI_TX_1* W8
DMI_TX_2* Y7
DMI_TX_3* AA8
DMI_TX_0 V7
DMI_TX_1 W7
DMI_TX_2 Y6
DMI_TX_3 AA7

FLEXIBLE DISPLAY INTERFACE
(Unused)
FDI_TX_0* AC7
FDI_TX_1* AC3
FDI_TX_2* AD1
FDI_TX_3* AD3
FDI_TX_4* AD6
FDI_TX_5* AE8
FDI_TX_6* AF2
FDI_TX_7* AG1
FDI_TX_0 AC8
FDI_TX_1 AC2
FDI_TX_2 AD2
FDI_TX_3 AD4
FDI_TX_4 AD7
FDI_TX_5 AE7
FDI_TX_6 AF3
FDI_TX_7 AG2
FDI_FSYNC_0 AC5
FDI_FSYNC_1 AE5
FDI_INT AG3
FDI_LSYNC_0 AC4
FDI_LSYNC_1 AE4
FDI_COMPIO AE2
FDI_ICOMPIO AE1

PCI EXPRESS -- GRAPHICS
(Available for Workstation only)
PCI EXPRESS
PE_RX_0* P4
PE_RX_1* R1
PE_RX_2* T3
PE_RX_3* U1
PE_RX_0 P3
PE_RX_1 R2
PE_RX_2 T4
PE_RX_3 U2
PE_TX_0* P7
PE_TX_1* T8
PE_TX_2* R5
PE_TX_3* U6
PE_TX_0 P8
PE_TX_1 T7
PE_TX_2 R6
PE_TX_3 U5

PEG_COMPI B4
PEG_ICOMPO B5
PEG_RCOMPO C4
PEG_RX_0* B12
PEG_RX_1* D11
PEG_RX_2* C9
PEG_RX_3* E9
PEG_RX_4* B7
PEG_RX_5* C5
PEG_RX_6* A6
PEG_RX_7* E1
PEG_RX_8* F3
PEG_RX_9* G1
PEG_RX_10* H4
PEG_RX_11* J2
PEG_RX_12* K4
PEG_RX_13* L2
PEG_RX_14* M4
PEG_RX_15* N2
PEG_RX_0 B11
PEG_RX_1 D12
PEG_RX_2 C10
PEG_RX_3 E10
PEG_RX_4 B8
PEG_RX_5 C6
PEG_RX_6 A5
PEG_RX_7 E2
PEG_RX_8 F4
PEG_RX_9 G2
PEG_RX_10 H3
PEG_RX_11 J1
PEG_RX_12 K3
PEG_RX_13 L1
PEG_RX_14 M3
PEG_RX_15 N1
PEG_TX_0* C14
PEG_TX_1* E13
PEG_TX_2* G13
PEG_TX_3* F11
PEG_TX_4* J13
PEG_TX_5* D7
PEG_TX_6* C3
PEG_TX_7* E5
PEG_TX_8* F7
PEG_TX_9* G9
PEG_TX_10* G6
PEG_TX_11* K8
PEG_TX_12* J6
PEG_TX_13* M7
PEG_TX_14* L5
PEG_TX_15* N6
PEG_TX_0 C13
PEG_TX_1 E14
PEG_TX_2 G14
PEG_TX_3 F12
PEG_TX_4 J14
PEG_TX_5 D8
PEG_TX_6 D3
PEG_TX_7 E6
PEG_TX_8 F8
PEG_TX_9 G10
PEG_TX_10 G5
PEG_TX_11 K7
PEG_TX_12 J5
PEG_TX_13 M8
PEG_TX_14 L6
PEG_TX_15 N5

=PPVCCIO_S0_CPU
R1011 24.9 1% 1/16W MF-LF 402
CPU_FDI_COMPIO

PLACE_NEAR=U1000.B4:12.7mm
=PPVCCIO_S0_CPU
R1010 24.9 1% 1/16W MF-LF 402
CPU_PEG_COMP

OMIT TABLE
U1000
IVY-BRIDGE
BGA-SKT-K70
SYM 5 OF 10

RESERVED
RSVD_C38 TP_CPU_RSVD<1>
RSVD_C39 TP_CPU_RSVD<2>
RSVD_D38 TP_CPU_RSVD<3>
RSVD_H7 TP_CPU_RSVD<4>
RSVD_H8 TP_CPU_RSVD<5>
RSVD_J9 TP_CPU_RSVD<6>
RSVD_J31 TP_CPU_RSVD<7>
RSVD_J33 TP_CPU_RSVD<8>
RSVD_J34 TP_CPU_RSVD<9>
RSVD_K9 TP_CPU_RSVD<10>
RSVD_K31 TP_CPU_RSVD<11>
RSVD_K34 TP_CPU_RSVD<12>
RSVD_L9 TP_CPU_RSVD<13>
RSVD_L31 TP_CPU_RSVD<14>
RSVD_L33 TP_CPU_RSVD<15>
RSVD_L34 TP_CPU_RSVD<16>
RSVD_M34 ThermDC NC_SNS_CPU_THERMDN NO_TEST=TRUE
RSVD_N33 ThermDA NC_SNS_CPU_THERMDP NO_TEST=TRUE
RSVD_N34 TP_CPU_RSVD<19>
RSVD_P35 P35 TP_CPU_RSVD<20>
RSVD_P37 P37 TP_CPU_RSVD<21>
RSVD_P39 P39 TP_CPU_RSVD<22>
RSVD_R34 R34 TP_CPU_RSVD<23>
RSVD_R36 R36 TP_CPU_RSVD<24>
RSVD_R38 R38 TP_CPU_RSVD<25>
RSVD_R40 R40 TP_CPU_RSVD<26>
RSVD_AB6 AB6 TP_CPU_RSVD<27>
RSVD_AB7 AB7 TP_CPU_RSVD<28>
RSVD_AD34 AD34 TP_CPU_RSVD<29>
RSVD_AD35 AD35 TP_CPU_RSVD<30>
RSVD_AD37 AD37 TP_CPU_RSVD<31>
RSVD_AE6 AE6 TP_CPU_RSVD<32>
RSVD_AF4 AF4 TP_CPU_RSVD<33>
RSVD_AG4 AG4 TP_CPU_RSVD<34>
RSVD_AJ11 AJ11 TP_CPU_RSVD<35>
RSVD_AJ29 AJ29 TP_CPU_RSVD<36>
RSVD_AJ30 AJ30 TP_CPU_RSVD<37>
RSVD_AJ31 AJ31 TP_CPU_RSVD<38>
RSVD_AN20 AN20 TP_CPU_RSVD<39>
RSVD_AP20 AP20 TP_CPU_RSVD<40>
RSVD_AT11 AT11 TP_CPU_RSVD<41>
RSVD_AT14 AT14 TP_CPU_RSVD<42>
RSVD_AU10 AU10 TP_CPU_RSVD<43>
RSVD_AV34 AV34 TP_CPU_RSVD<44>
RSVD_AW34 AW34 TP_CPU_RSVD<45>
RSVD_AY10 AY10 TP_CPU_RSVD<46>
RSVD_NCTF_AV1 AV1 TP_CPU_RSVD_NCTF<1>
RSVD_NCTF_AW2 AW2 TP_CPU_RSVD_NCTF<2>
RSVD_NCTF_AY3 AY3 TP_CPU_RSVD_NCTF<3>
RSVD_NCTF_B39 B39 TP_CPU_RSVD_NCTF<4>
NCTF_A38 A38 TP_CPU_NCTF<1>
NCTF_C2 C2 TP_CPU_NCTF<2>
NCTF_D1 D1 TP_CPU_NCTF<3>
NCTF_AU40 AU40 TP_CPU_NCTF<4>
NCTF_AW38 AW38 TP_CPU_NCTF<5>

INTEL SUGGESTS TO KEEP THESE TPS

CFG_0 H36 CPU_CFG<0>
CFG_1 J36 CPU_CFG<1>
CFG_2 J37 CPU_CFG<2>
CFG_3 K36 CPU_CFG<3>
CFG_4 L36 CPU_CFG<4>
CFG_5 N35 CPU_CFG<5>
CFG_6 L37 CPU_CFG<6>
CFG_7 M36 CPU_CFG<7>
CFG_8 J38 CPU_CFG<8>
CFG_9 L35 CPU_CFG<9>
CFG_10 M38 CPU_CFG<10>
CFG_11 N36 CPU_CFG<11>
CFG_12 N38 CPU_CFG<12>
CFG_13 N39 CPU_CFG<13>
CFG_14 N37 CPU_CFG<14>
CFG_15 N40 CPU_CFG<15>
CFG_16 G37 CPU_CFG<16>
CFG_17 G36 CPU_CFG<17>

CFG[1:0] Reserved config lane
CFG[2] PCIe Static x16 lane reversal; Refer to page 15 for more info
CFG[3] PCIe Static x4 lane reversal; Refer to page 15 for more info
CFG[4] Reserved config lane
CFG[6:5] PCIe bifurcation; Refer to page 15 for more info
CFG[17:7] Reserved config lanes

SYNC_MASTER=K70_MLB SYNC_DATE=11/30/2011
PAGE TITLE
CPU DMI/PEG/FDI/RSVD
Apple Inc.
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SHEET 10 OF 100

BASED ON INTEL MOBILE SOLUTION

=PPVCCIO_S0_CPU

R1101 51 5% 1/16W MF-LF 402

=PPVCCIO_S0_CPU

PLACE_NEAR=U1000.P36:50mm

R1124 75 5% 1/16W MF-LF 402

CPU_RESET_L

R1125 43 5% 1/16W MF-LF 402

PLT_RESET_LS1V05_L

R1102 0 1/16W MF-LF 5% 402

CPU_PROCHOT_R_L

CPU_SKTOCC_L

CPU_PROC_SEL

CPU_CATERR_L

CPU_PECI

CPU_PROCHOT_L

CPU_THRMTRIP_L

PM_SYNC

CPU_PWRGD

PM_MEM_PWRGD_R

CPU_MEM_RESET_L

CPU_DDR_VREF

CPU_DIMM_VREF_DAC_B

CPU_DIMM_VREF_DAC_A

=PP1V5_S0_CPU_MEM

R1120 200 1% 1/16W MF-LF 402

FROM PCH

PM_MEM_PWRGD

R1121 130 1% 1/16W MF-LF 402

OMIT_TABLE

U1000

IVY-BRIDGE

BGA-SKT-K70

SYM 2 OF 10

AJ33	SKTOCC*	CLOCKS	
K32	PROC_SEL		
E37	CATERR*	THERMAL	
J35	PECI		
H34	PROCHOT*		
G35	THERMTRIP*		
F36	RESET*	PWR MGMT	
E38	PM_SYNC		
J40	UNCOREPWRGOOD		
AJ19	SM_DRAMPWROK	DDR3 MISC	
AW18	SM_DRAMRST*		
AJ22	SM_VREF		
AH1	SB_DIMM_VREFDQ		
AH4	SA_DIMM_VREFDQ		

C40	BCLK_ITP	ITPCPU_CLK100M_P	
D40	BCLK_ITP*	ITPCPU_CLK100M_N	
W2	BCLK_0	DMI_CLK100M_CPU_P	
W1	BCLK_0*	DMI_CLK100M_CPU_N	
K38	PRDY*	XDP_CPU_PRDY_L	
K40	PREQ*	XDP_CPU_PREQ_L	
M40	TCK	XDP_CPU_TCK	
L38	TMS	XDP_CPU_TMS	
J39	TRST*	XDP_CPU_TRST_L	
L40	TDI	XDP_CPU_TDI	
L39	TDO	XDP_CPU_TDO	
E39	DBR*	XDP_DBRESET_L	
H40	BPM[0]*	XDP_BPM_L<0>	
H38	BPM[1]*	XDP_BPM_L<1>	
G38	BPM[2]*	XDP_BPM_L<2>	
G40	BPM[3]*	XDP_BPM_L<3>	
G39	BPM[4]*	XDP_BPM_L<4>	
F38	BPM[5]*	XDP_BPM_L<5>	
E40	BPM[6]*	XDP_BPM_L<6>	
F40	BPM[7]*	XDP_BPM_L<7>	

JTAG & BPM

R1111 1K 5% 1/16W MF-LF 402

=PP1V5_S0_CPU_MEM

R1140 1K 1% 1/16W MF-LF 402

CPU_DDR_VREF

R1141 1K 1% 1/16W MF-LF 402

C1140 0.1UF 10% 10V X7R-CERM 402

SYNC_MASTER=K70_MLB SYNC_DATE=11/30/2011

PAGE TITLE

CPU CLOCK/MISC/JTAG

Apple Inc.

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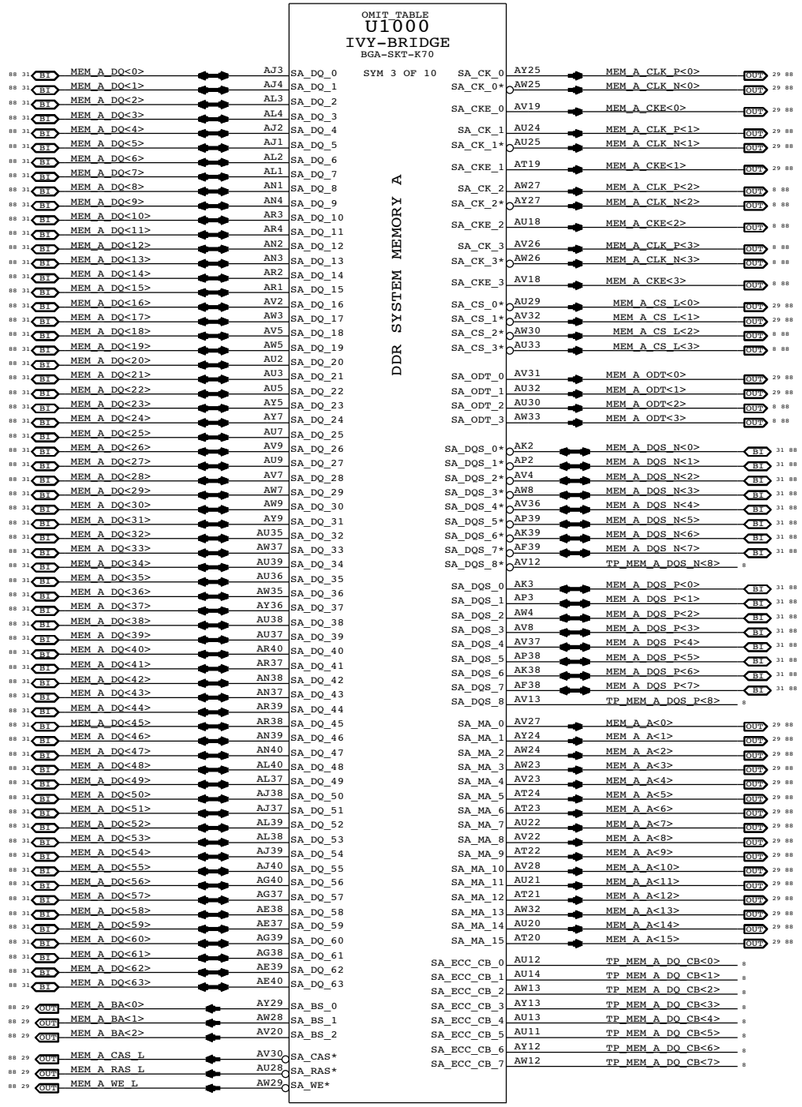

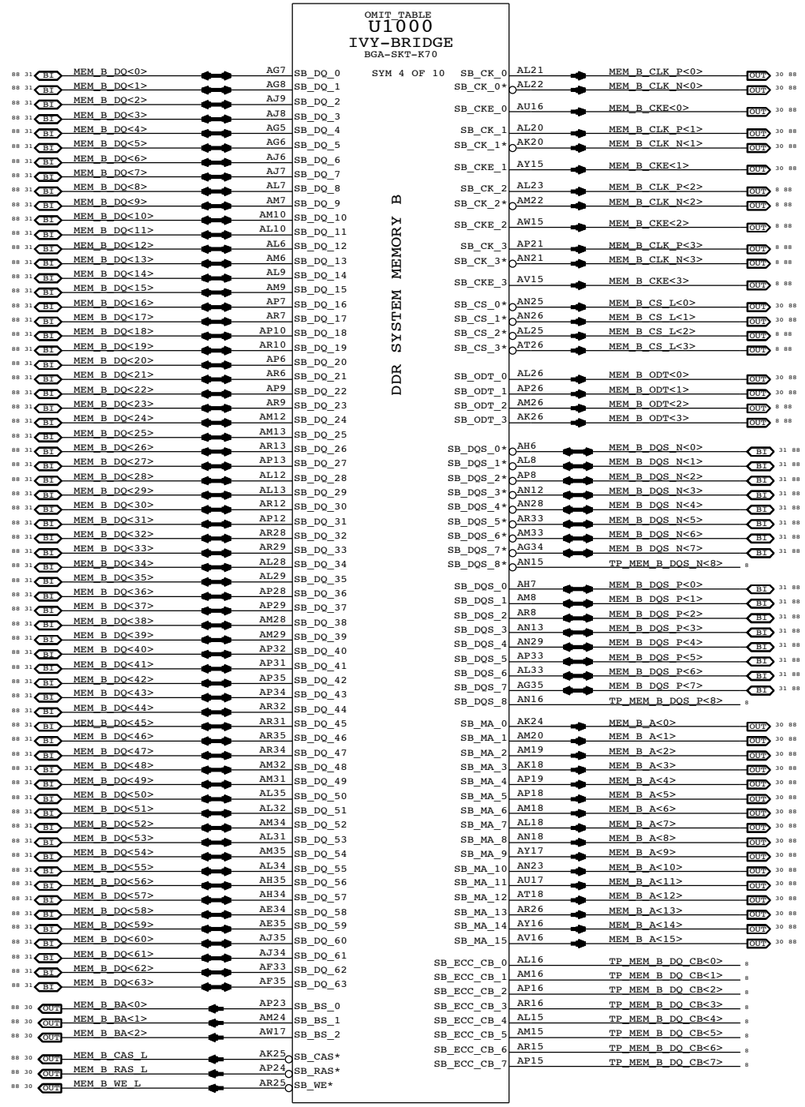

SYNC MASTER=K70 MLB SYNC DATE=11/30/2011

PAGE TITLE

CPU DDR3 INTERFACES

Apple Inc.

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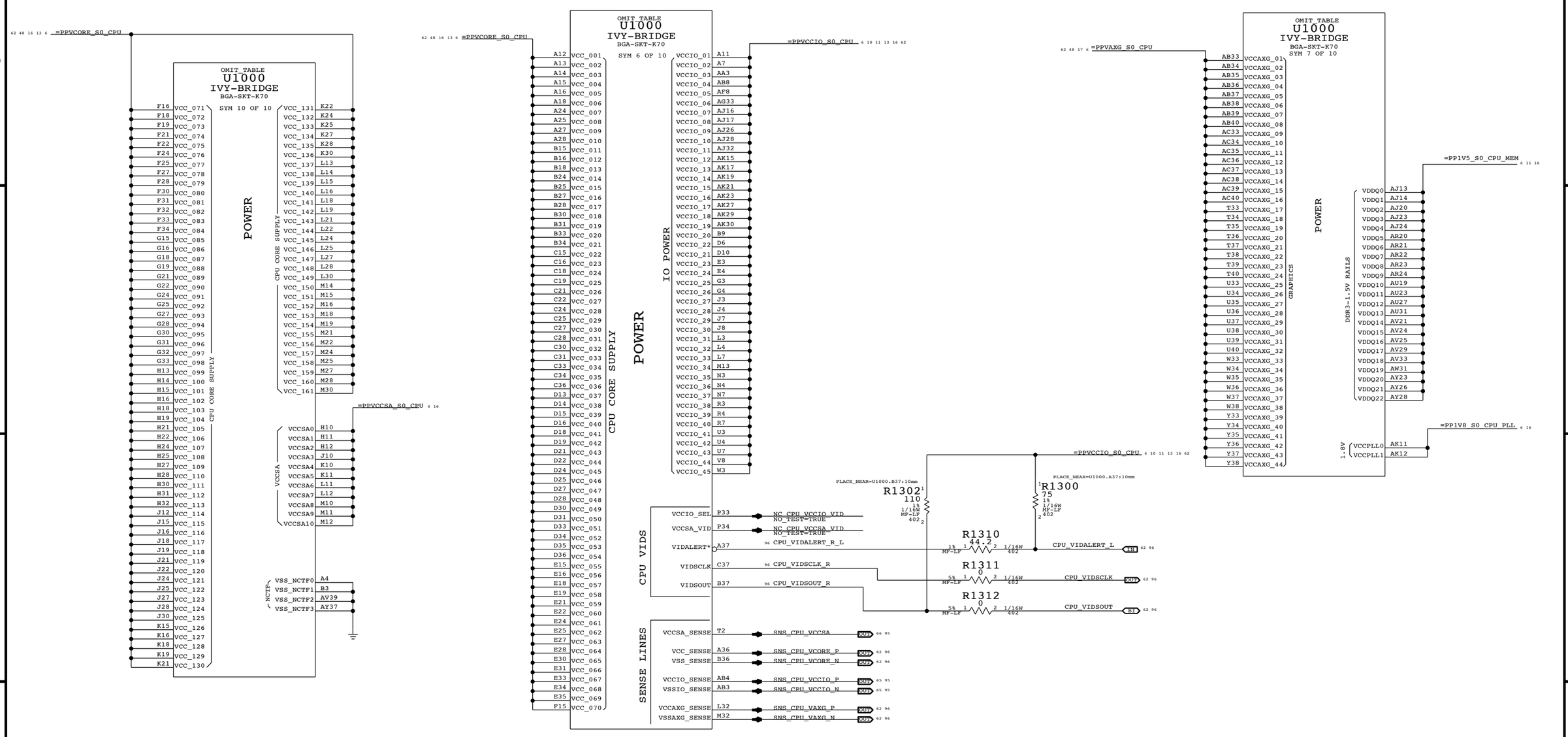

SYNC_MASTER=K70_MLB SYNC_DATE=11/30/2011

PAGE TITLE

CPU POWER

Apple Inc.

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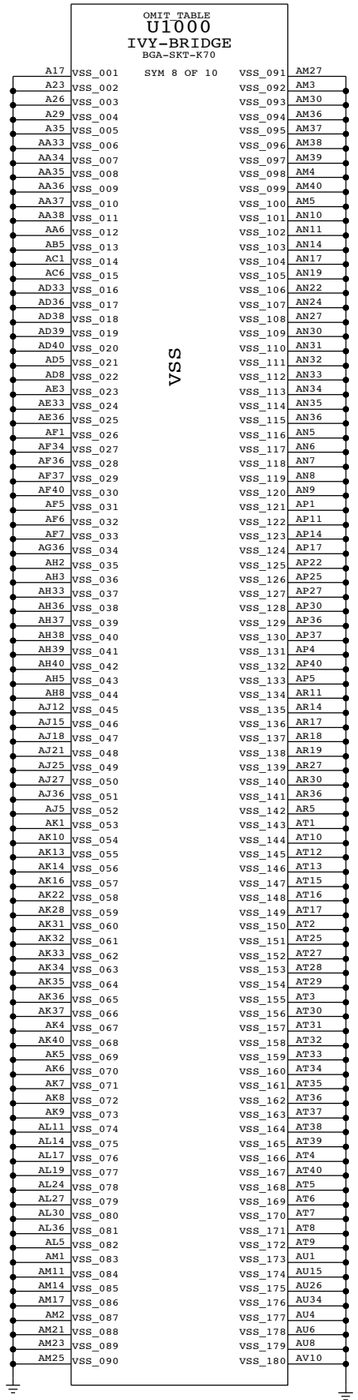

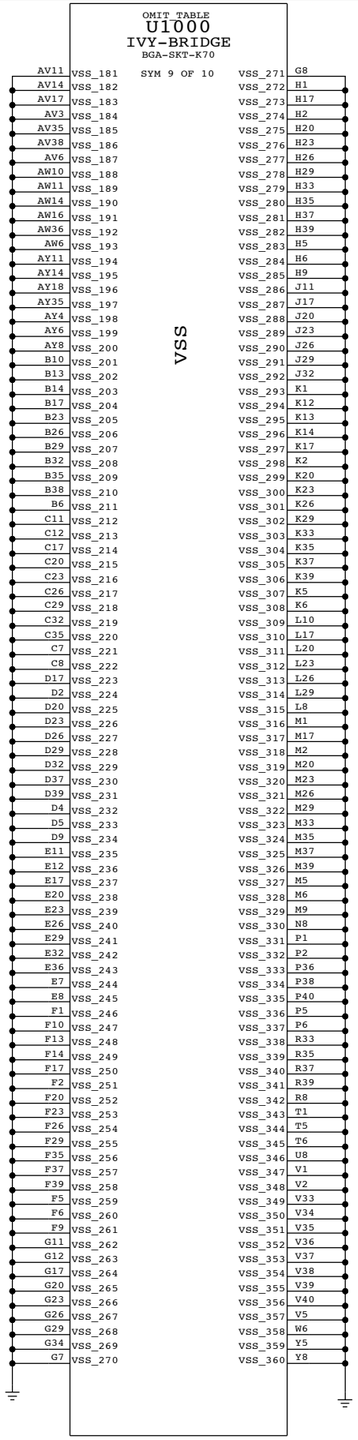

SYNC MASTER=K70 MLB SYNC DATE=11/30/2011

PAGE TITLE

CPU GROUNDS

Apple Inc.

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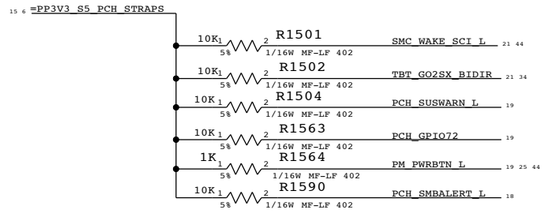
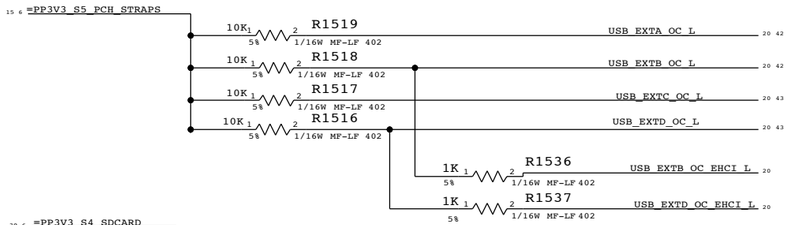
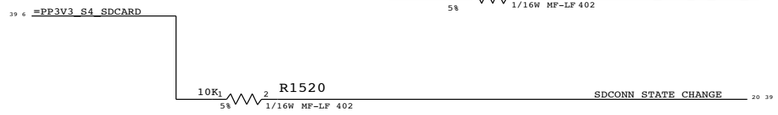
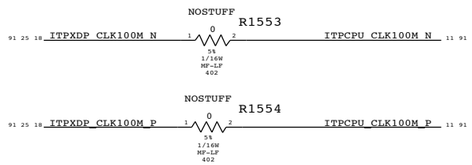
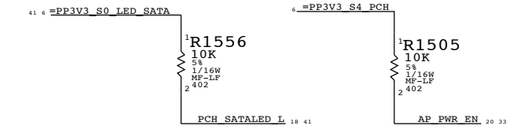
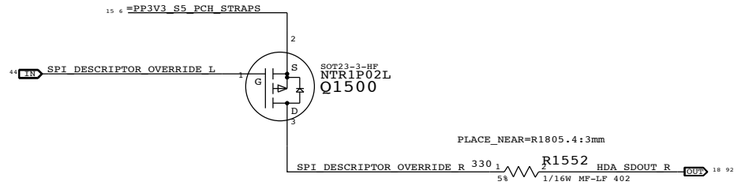


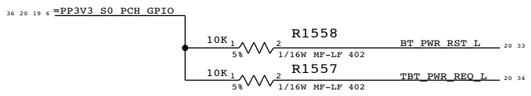


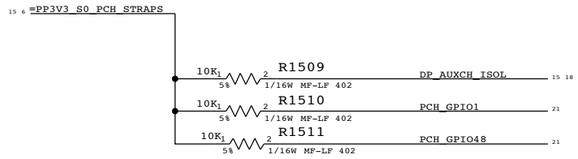






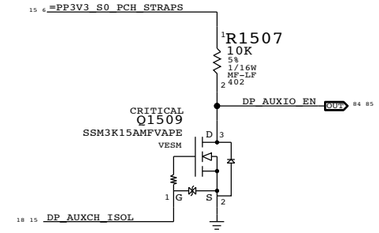


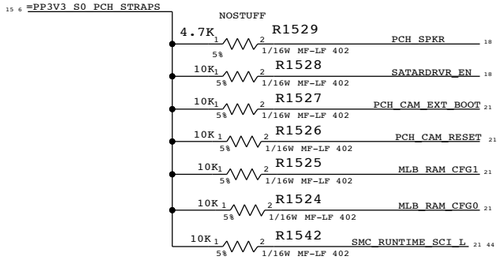


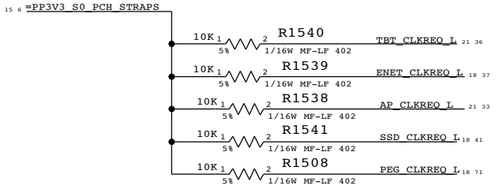


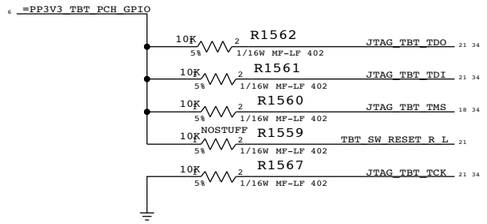
DP_AUXIO_EN Inversion

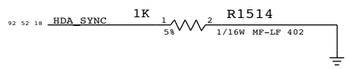
Inverts PCH GPIO DP_AUXCH_ISOL to drive DP_AUXIO_EN for external DP









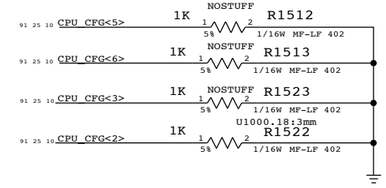


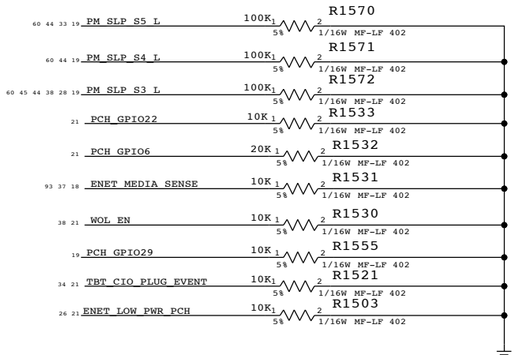
IVB PCIe Straps configuration:

CFG[5:6] = Sel PCIe Cfg
11 = 1x16 (default)
10 = 2x8
00 = 1x8,2x4

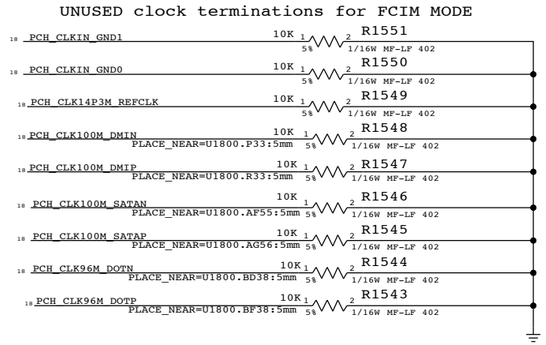
CFG[3]=Direct/Rev for X4
1 = DIR
0 = REV

CFG[2]= Direct/Rev for x16
1 = DIR
0 = REV





UNUSED clock terminations for FCIM MODE



SYNC_MASTER=D7 TONY	SYNC_DATE=01/11/2012
PAGE TITLE: STRAPS,PULL UPS,PULL DOWNS FOR PCH AND CPU	
Apple Inc.	DRAWING NUMBER: 051-9509 SIZE: D
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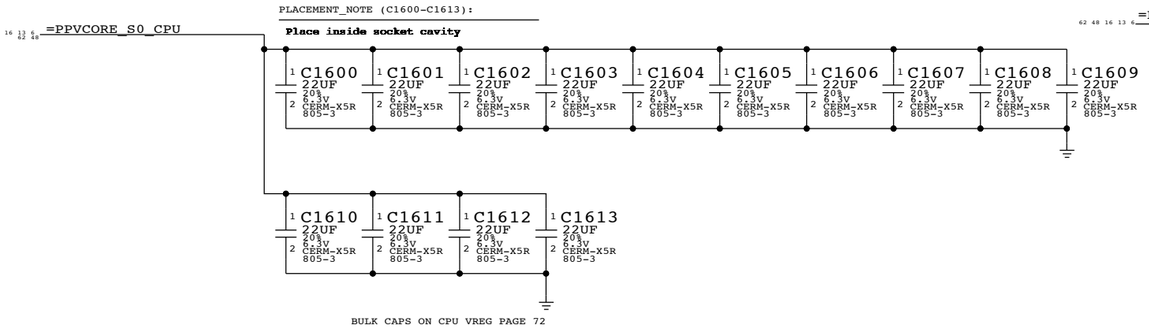
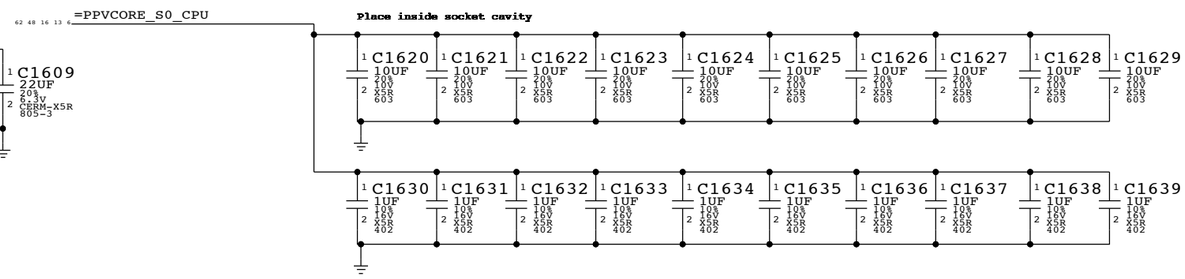
CPU VCORE DECOUPLING

14x 22UF,0805 INTEL RECOMMENDATION 18X 22UF 0805 (14 Inside cavity and 4 North of processor)

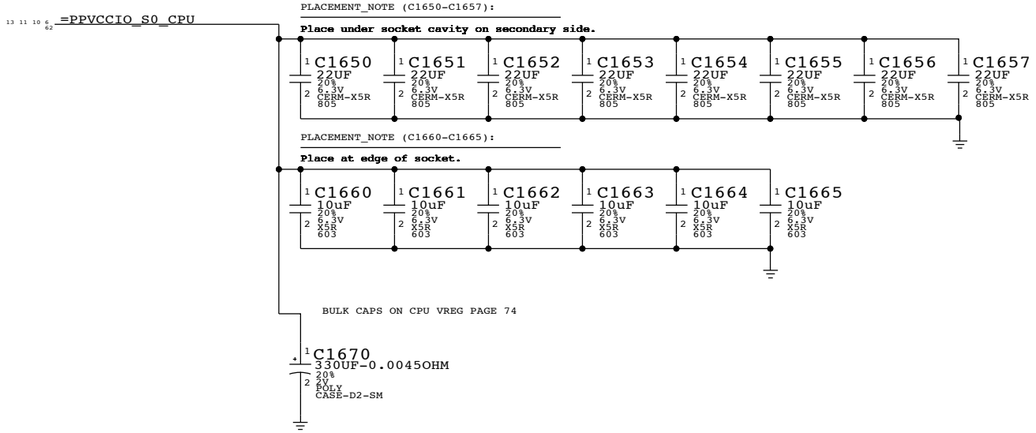


10x 10UF and 10x 1UF CAPACITORS



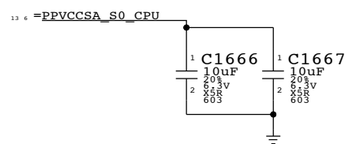
CPU VCCIO DECOUPLING

8X 22UF 0805, 6X 10UF 0805 INTEL RECOMMENDATION 9X22UF 0805,16X 0805 placeholders



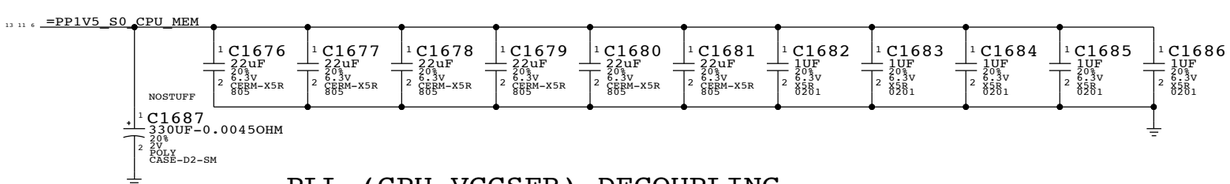
CPU VCCSA DECOUPLING

2x 10uF 0603. INTEL RECOMMENDATION 2X 10uF 0805



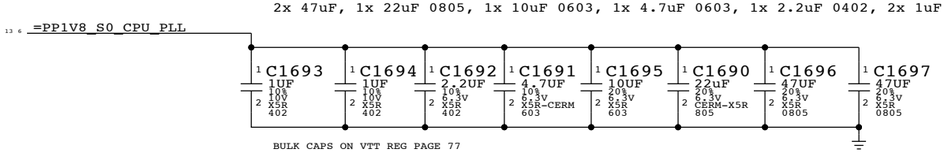
Bulk decoupling is on VCCSA reg page 75

Memory (CPU VCCDDR) DECOUPLING



PLL (CPU VCCSFR) DECOUPLING

2x 47uF, 1x 22uF 0805, 1x 10uF 0603, 1x 4.7uF 0603, 1x 2.2uF 0402, 2x 1uF 0402. INTEL RECOMMENDATION 1x 10uF 0805



SYNC MASTER=K70 MLB SYNC DATE=11/30/2011

PAGE TITLE: CPU NON-GFX DECOUPLING

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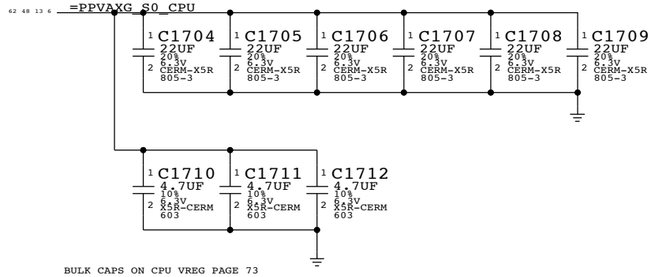
VAXG DECOUPLING

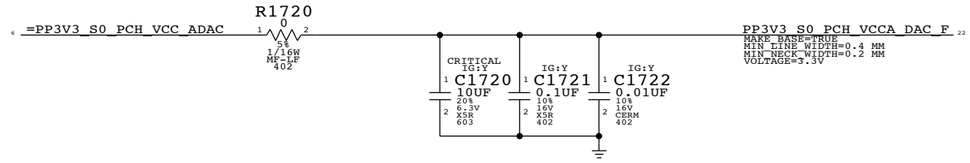
INTEL RECOMMENDATION 4X22UF 0805,3X 4.7UF

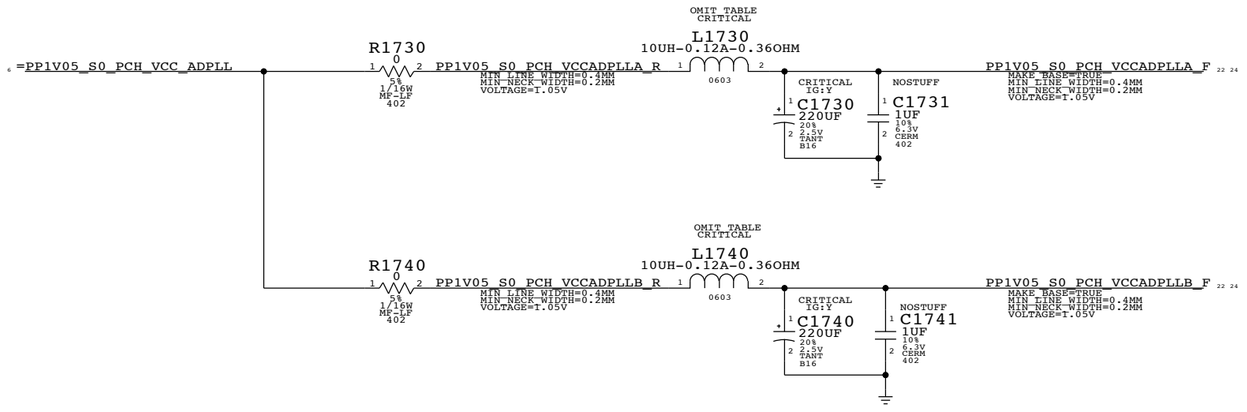
PLACEMENT_NOTE (C1704-C1709):

Place inside socket cavity



BULK CAPS ON CPU VREG PAGE 73





PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1070	2	IND,WW,10UH,20%.120MA,0.36OHMS	L1730,L1740	CRITICAL	IG:Y
113S0022	2	RES,MF,1/10W,0OHM,5,0603,SMD,LF	L1730,L1740		IG:N

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GFX DECOUPLING & PCH PWR ALIAS

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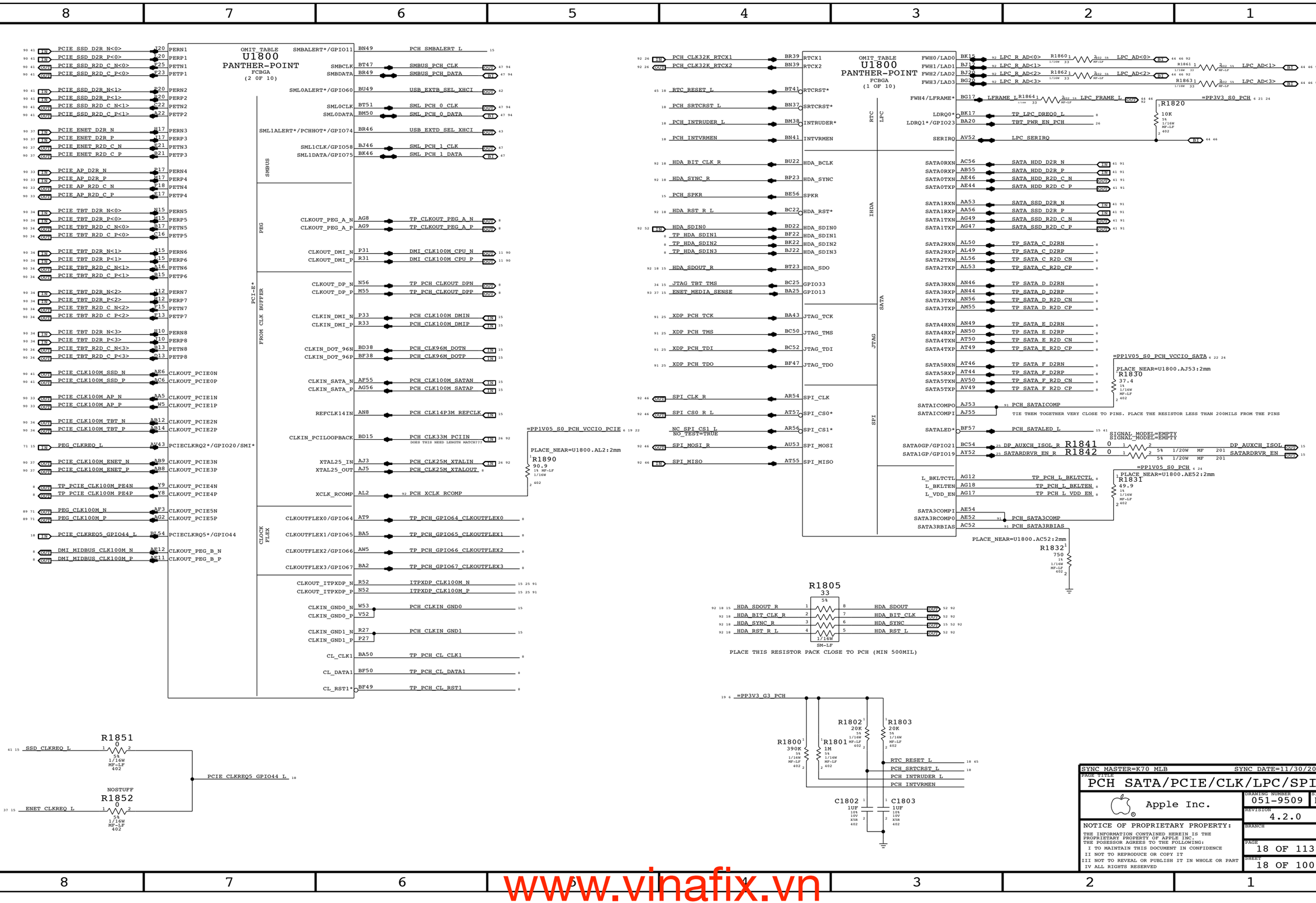

SYNC_MASTER=K70_MLB SYNC_DATE=11/30/2011

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PCH SATA/PCIE/CLK/LPC/SPI

Apple Inc.

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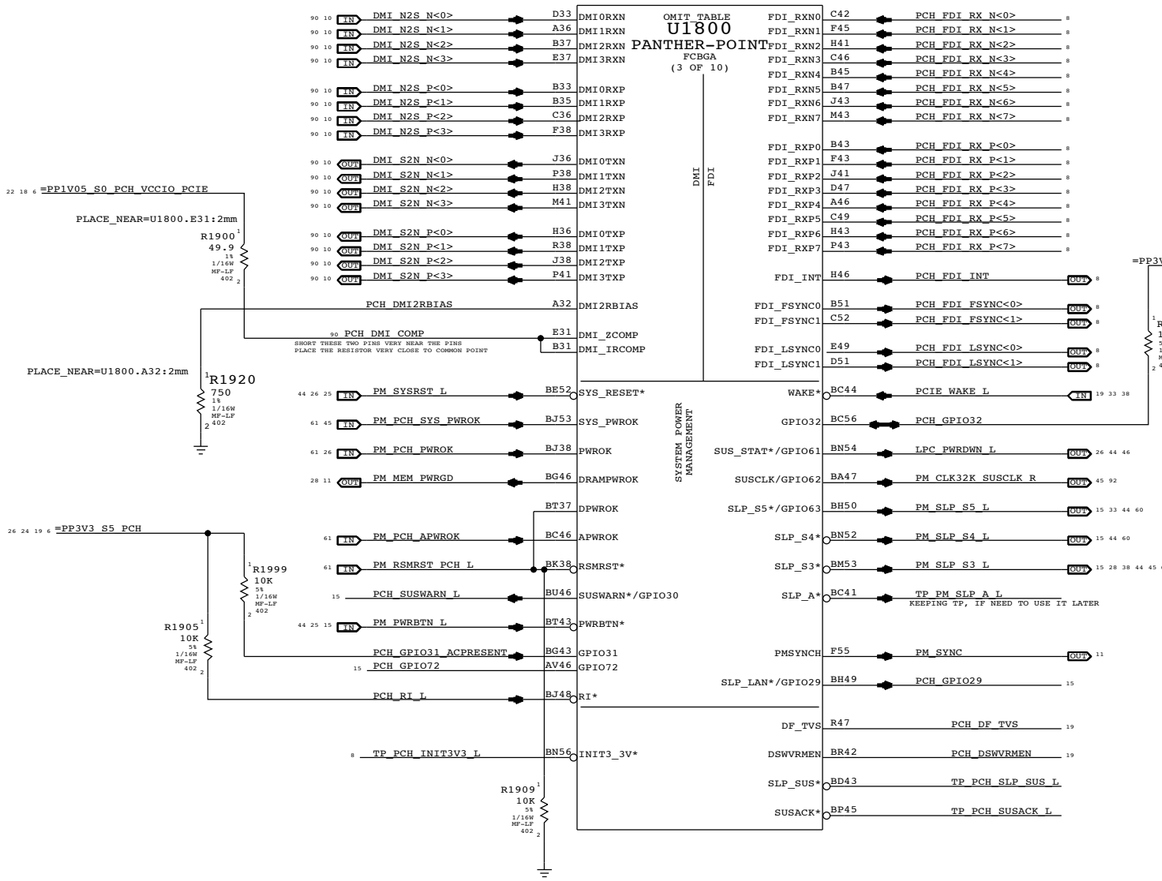

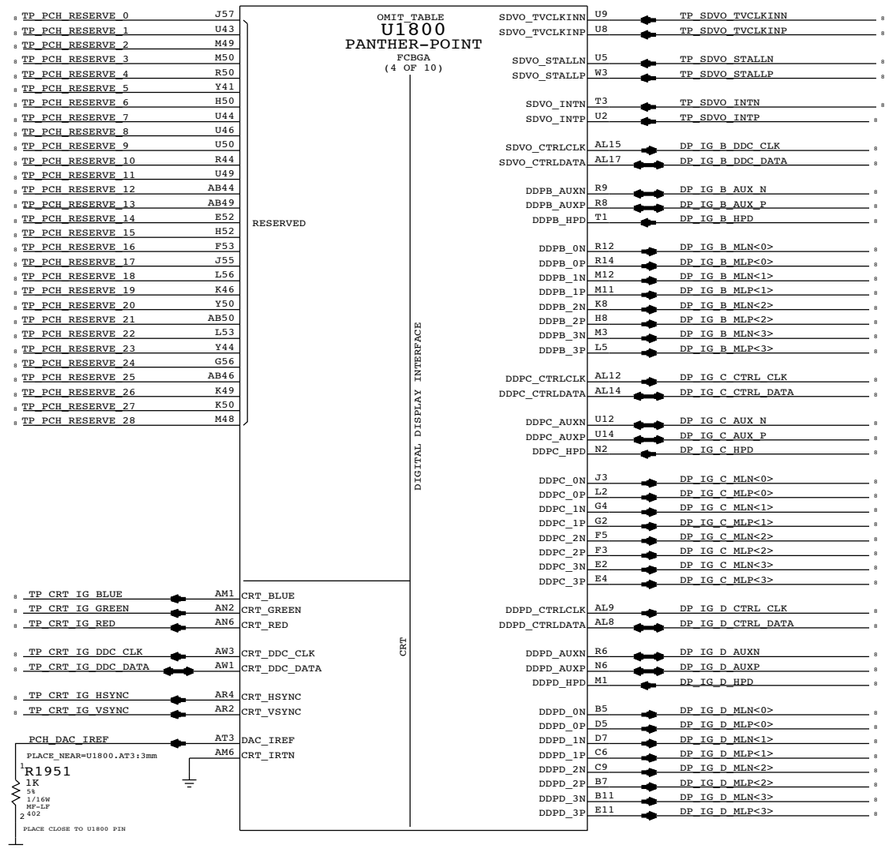

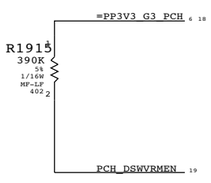

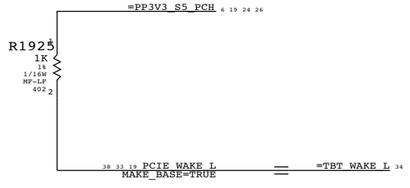

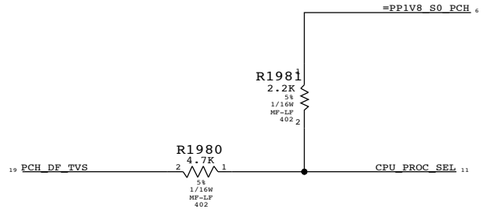

SYNC MASTER=K70_MLB SYNC DATE=11/30/2011

PAGE TITLE
PCH DMI/FDI/GRAPHICS

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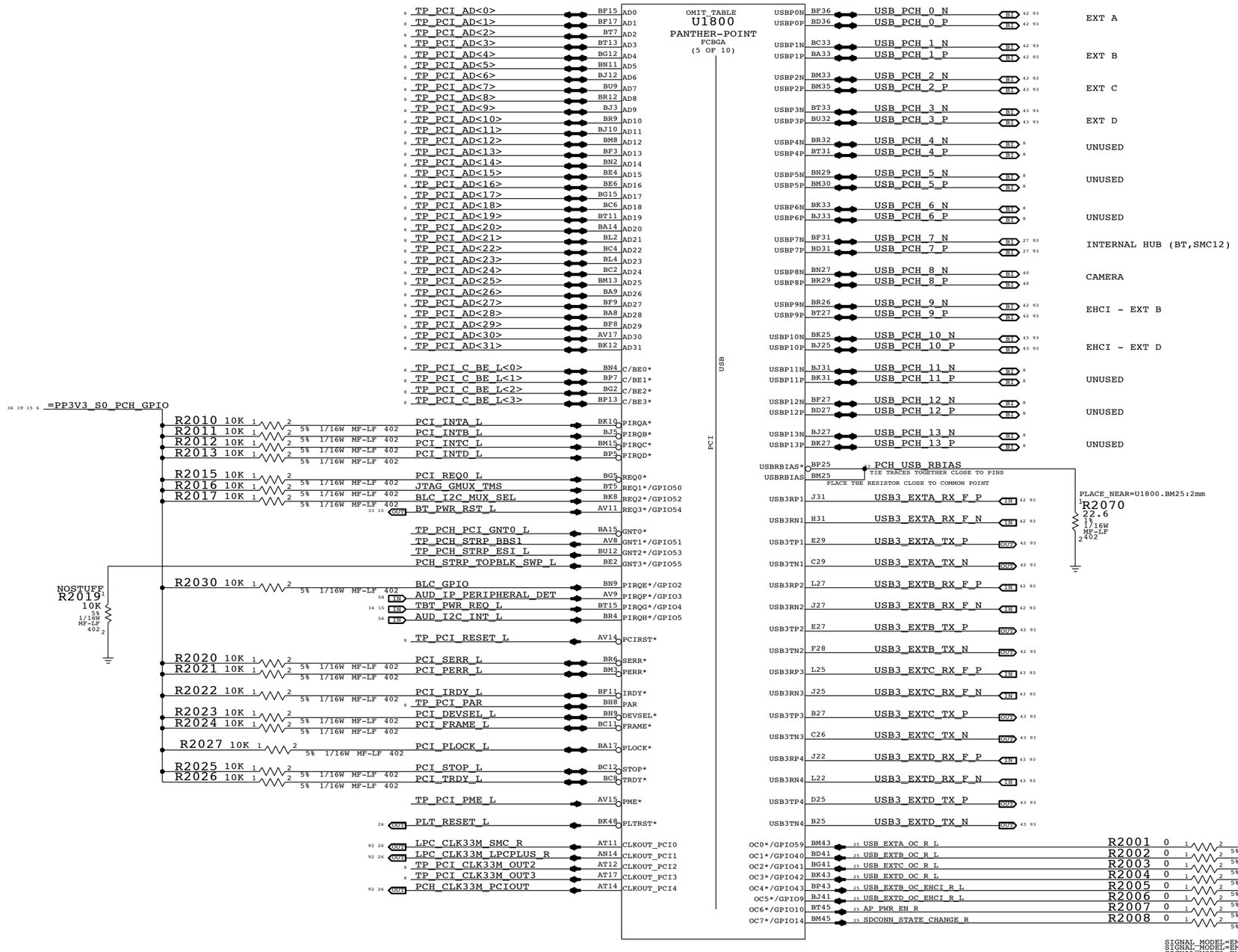

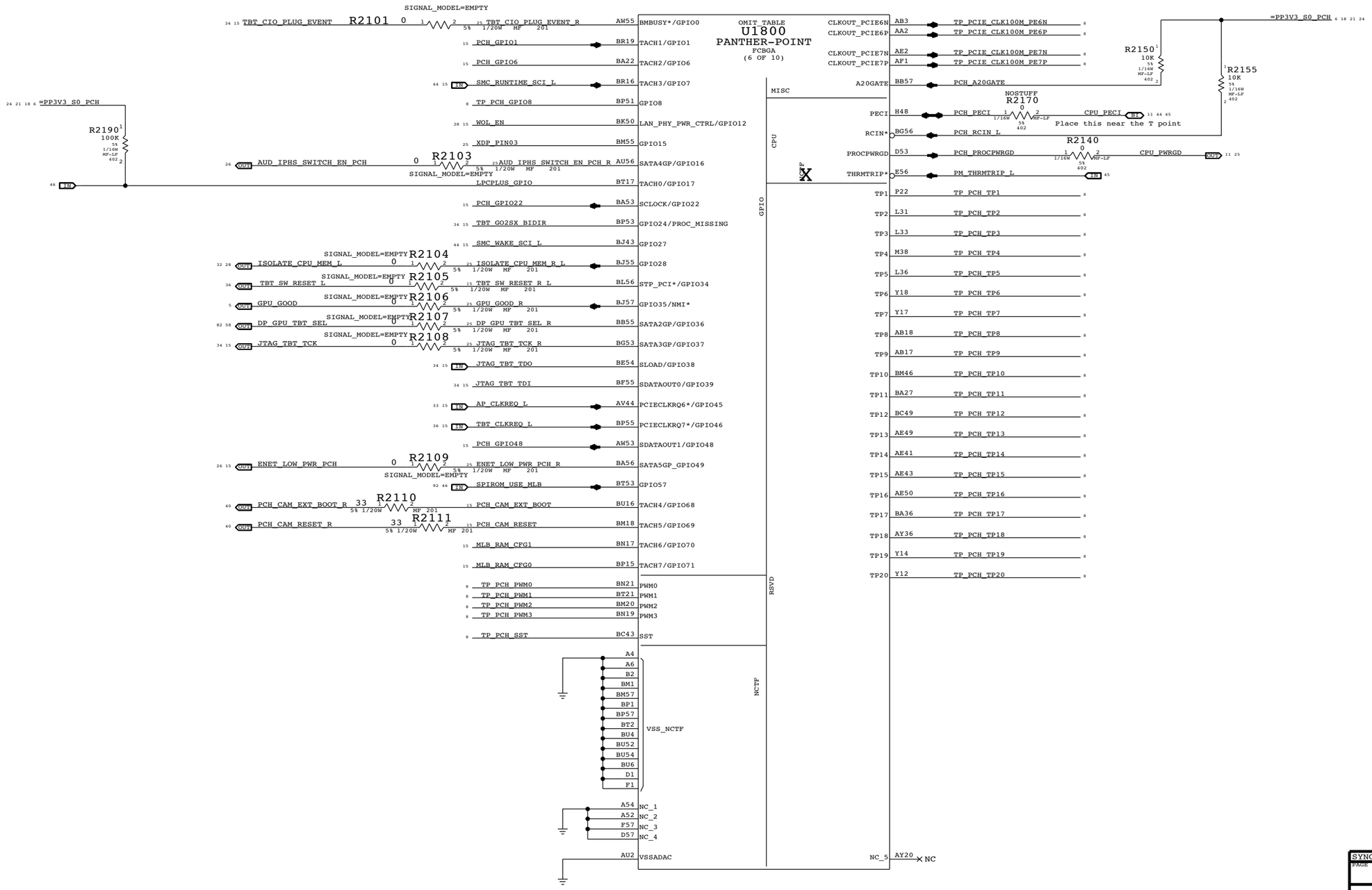

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PCH MISC

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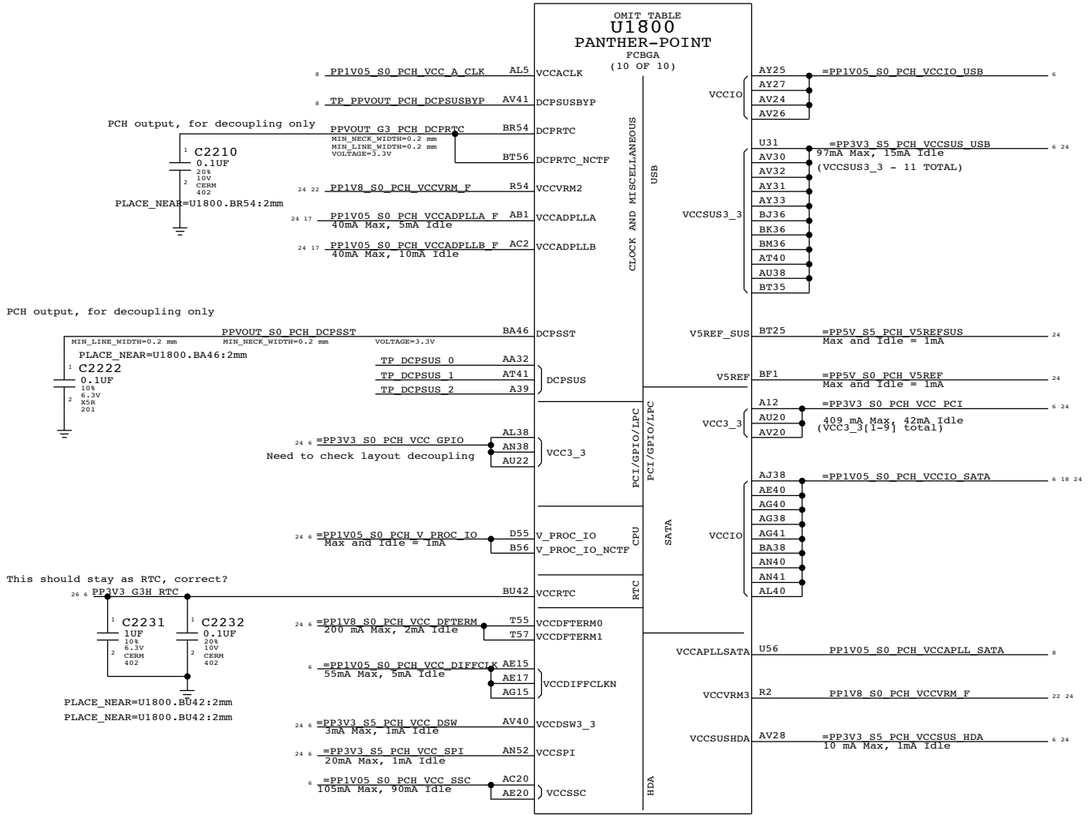

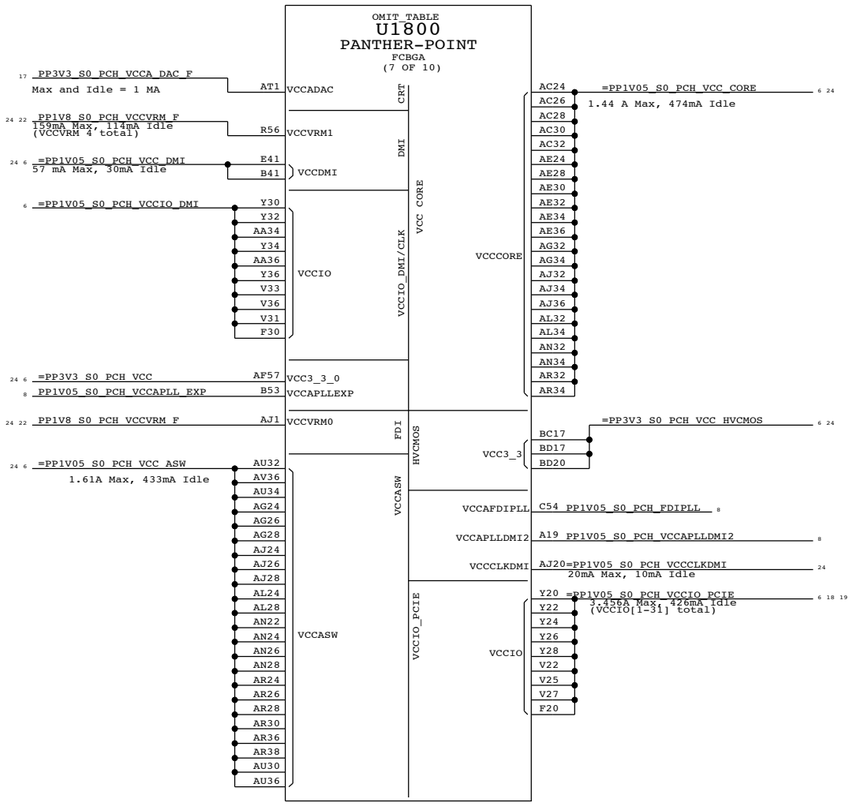

SYNC_MASTER=K70_MLB SYNC_DATE=11/30/2011

PAGE TITLE

PCH POWER

Apple Inc.

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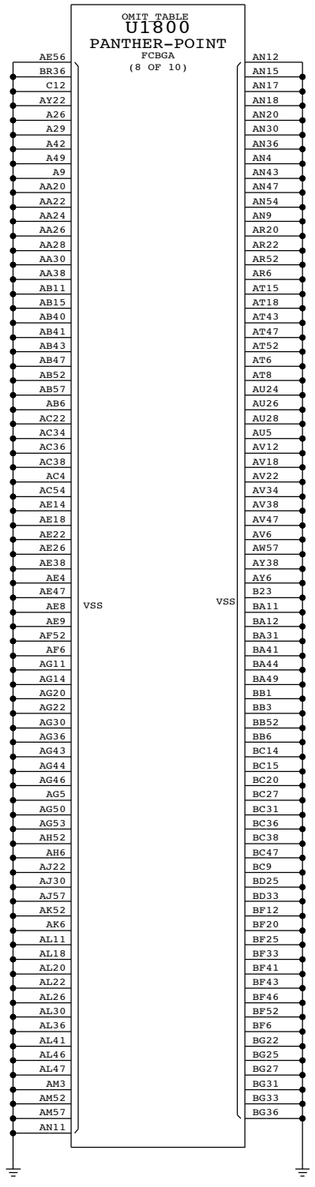

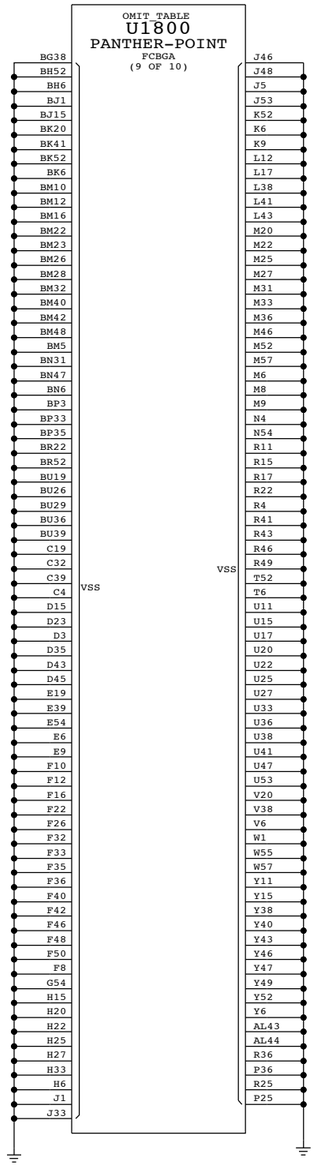

SYNC MASTER=K70 MLB SYNC DATE=11/30/2011

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PCH GROUNDS

Apple Inc.

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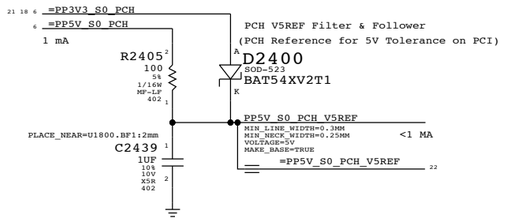
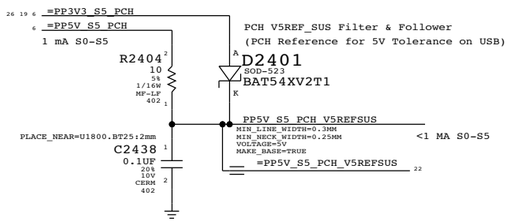
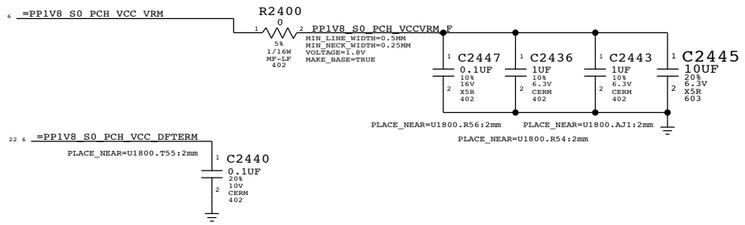
Power Sequencing

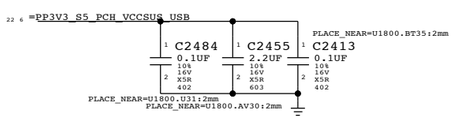


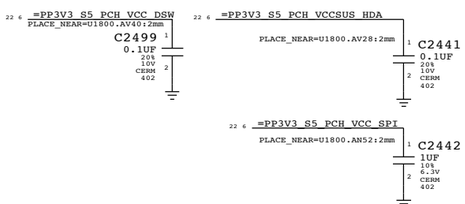


1V8 S0 Rails

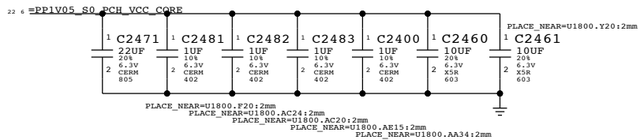


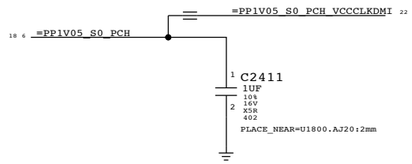
3V3 S5 Rails

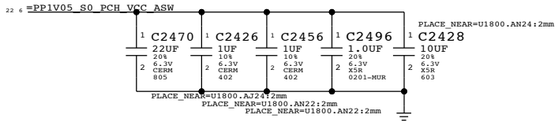


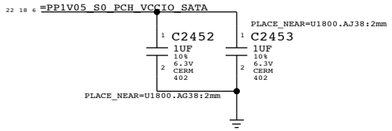


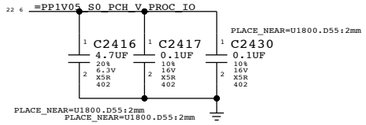
1V05 S0 Rails

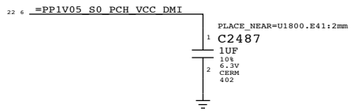


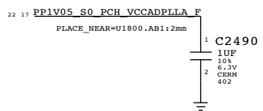


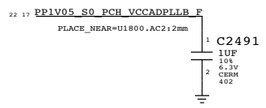




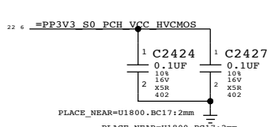


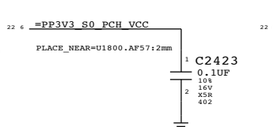


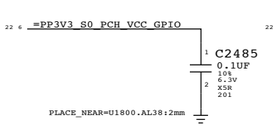


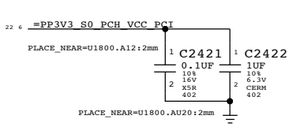


3V3 S0 Rails









SYNC_MASTER=K70_MLB SYNC_DATE=11/30/2011

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PCH DECOUPLING

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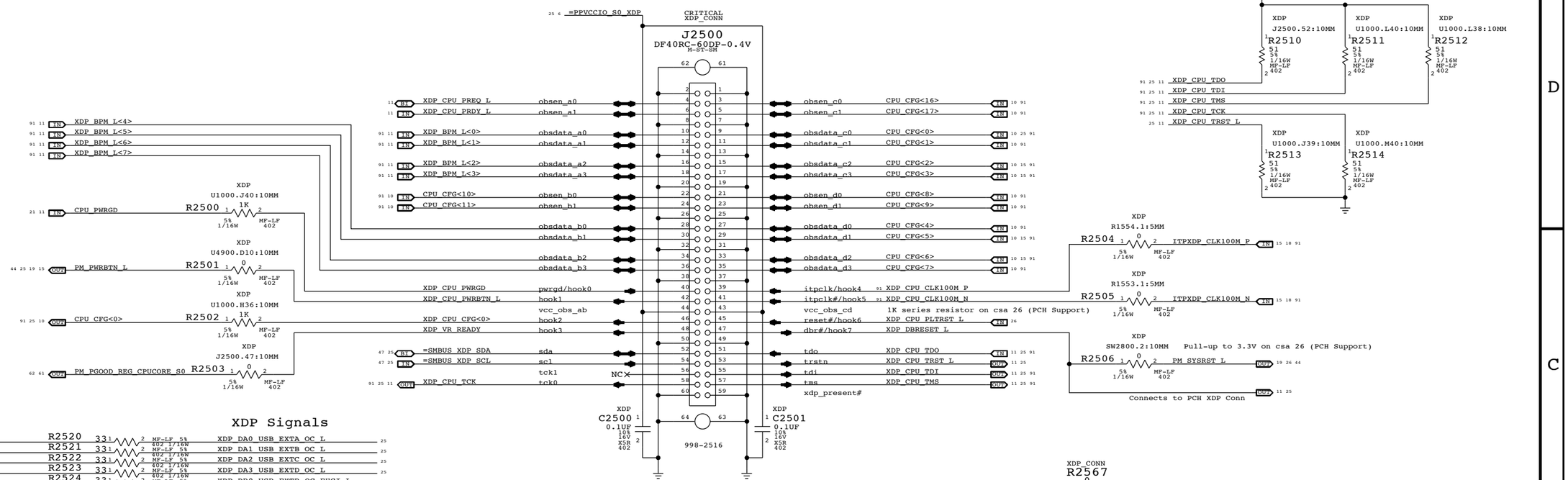
CPU Micro2-XDP



PCH Signals

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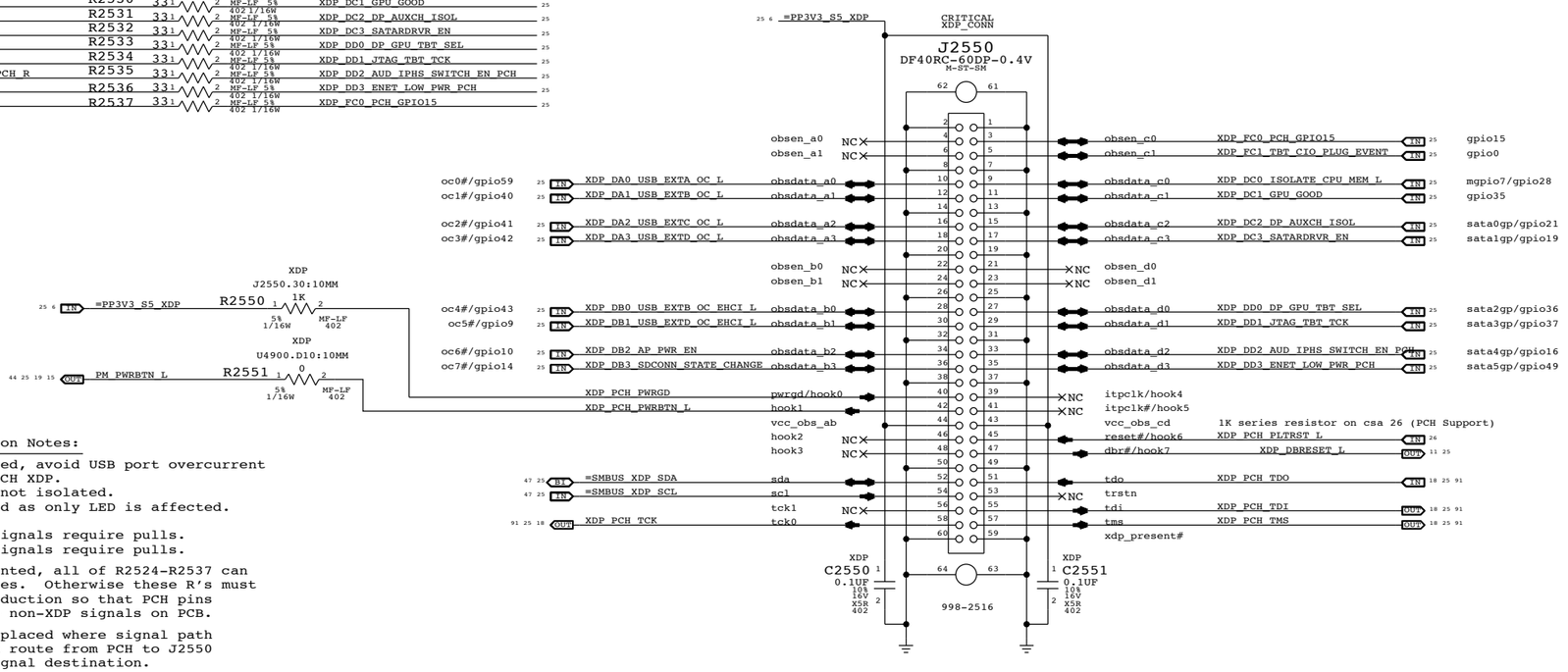
USB_EXTB_OC_R_L	R2521	33 MF-LF 5% 402 1/16W	XDP_DA1_USB_EXTB_OC_L
USB_EXTC_OC_R_L	R2522	33 MF-LF 5% 402 1/16W	XDP_DA2_USB_EXTC_OC_L
USB_EXTD_OC_R_L	R2523	33 MF-LF 5% 402 1/16W	XDP_DA3_USB_EXTD_OC_L
USB_EXTB_OC_EHCI_R_L	R2524	33 MF-LF 5% 402 1/16W	XDP_DB0_USB_EXTB_OC_EHCI_L
USB_EXTD_OC_EHCI_R_L	R2525	33 MF-LF 5% 402 1/16W	XDP_DB1_USB_EXTD_OC_EHCI_L
AP_PWR_EN_R	R2526	33 MF-LF 5% 402 1/16W	XDP_DB2_AP_PWR_EN
SDCONN_STATE_CHANGE_R	R2527	33 MF-LF 5% 402 1/16W	XDP_DB3_SDCONN_STATE_CHANGE
TBT_CIO_PLUG_EVENT_R	R2528	33 MF-LF 5% 402 1/16W	XDP_FC1_TBT_CIO_PLUG_EVENT
ISOLATE_CPU_MEM_R_L	R2529	33 MF-LF 5% 402 1/16W	XDP_DC0_ISOLATE_CPU_MEM_L
GPU_GOOD_R	R2530	33 MF-LF 5% 402 1/16W	XDP_DC1_GPU_GOOD
DP_AUXCH_ISOL_R	R2531	33 MF-LF 5% 402 1/16W	XDP_DC2_DP_AUXCH_ISOL
SATARDRVR_EN_R	R2532	33 MF-LF 5% 402 1/16W	XDP_DC3_SATARDRVR_EN
DP_GPU_TBT_SEL_R	R2533	33 MF-LF 5% 402 1/16W	XDP_DD0_DP_GPU_TBT_SEL
JTAG_TBT_TCK_R	R2534	33 MF-LF 5% 402 1/16W	XDP_DD1_JTAG_TBT_TCK
AUD_IPHS_SWITCH_EN_PCH_R	R2535	33 MF-LF 5% 402 1/16W	XDP_DD2_AUD_IPHS_SWITCH_EN_PCH
ENET_LOW_PWR_PCH_R	R2536	33 MF-LF 5% 402 1/16W	XDP_DD3_ENET_LOW_PWR_PCH
XDP_PIN03	R2537	33 MF-LF 5% 402 1/16W	XDP_FC0_PCH_GPIO15

XDP Signals

PCH Micro2-XDP



PCH/XDP Signal Isolation Notes:

- USB OC#'s not isolated, avoid USB port overcurrent events while using PCH XDP.
- Unused GPIOs 0 & 15 not isolated.
- MXM_GOOD not isolated as only LED is affected.
- For isolated GPIOs:
  - 'Output' non-XDP signals require pulls.
  - 'Output' PCH/XDP signals require pulls.

If PCH XDP not implemented, all of R2524-R2537 can be replaced with aliases. Otherwise these R's must be stuffed even in production so that PCH pins connect to appropriate non-XDP signals on PCB.

R2524-R2537 should be placed where signal path needs to split between route from PCH to J2550 and path to non-XDP signal destination.

PAGE TITLE: CPU and PCH XDP

Apple Inc.

DRAWING NUMBER: 051-9509 SIZE: D
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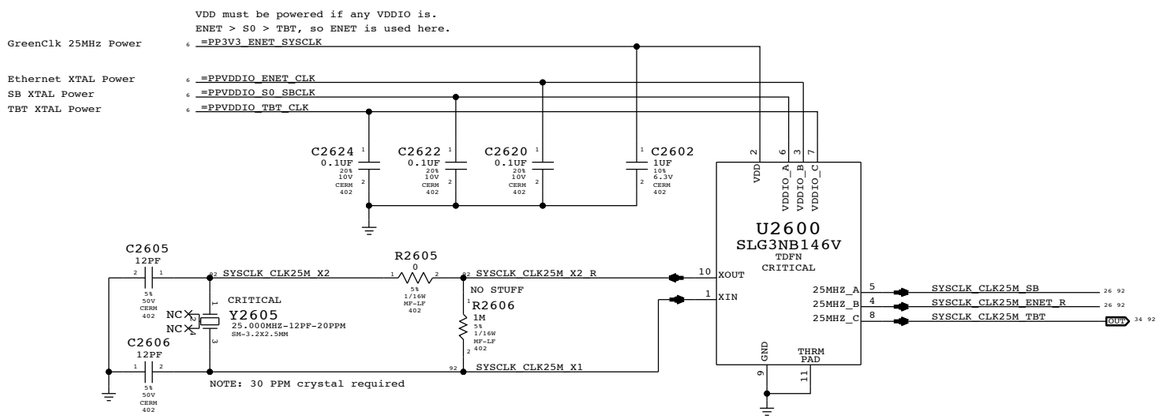
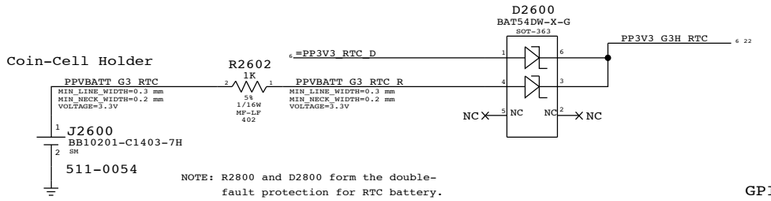
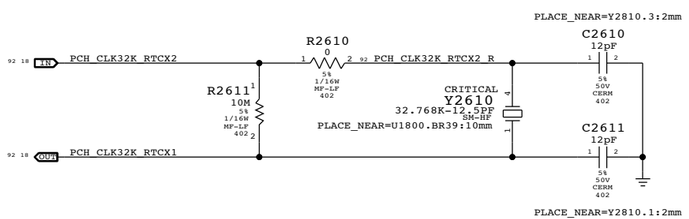
System 25MHz Clock Generator



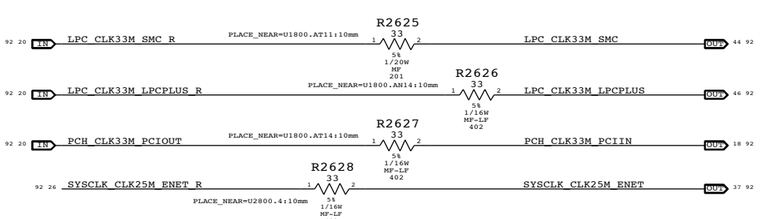
RTC Power Sources



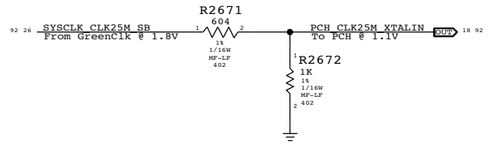
PCH RTC Crystal



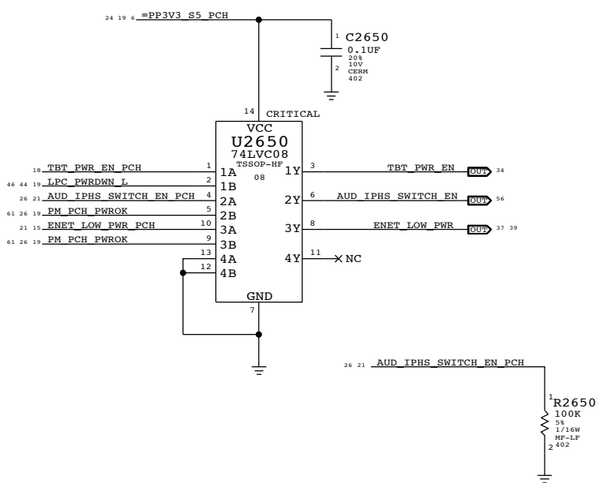
Clock series termination



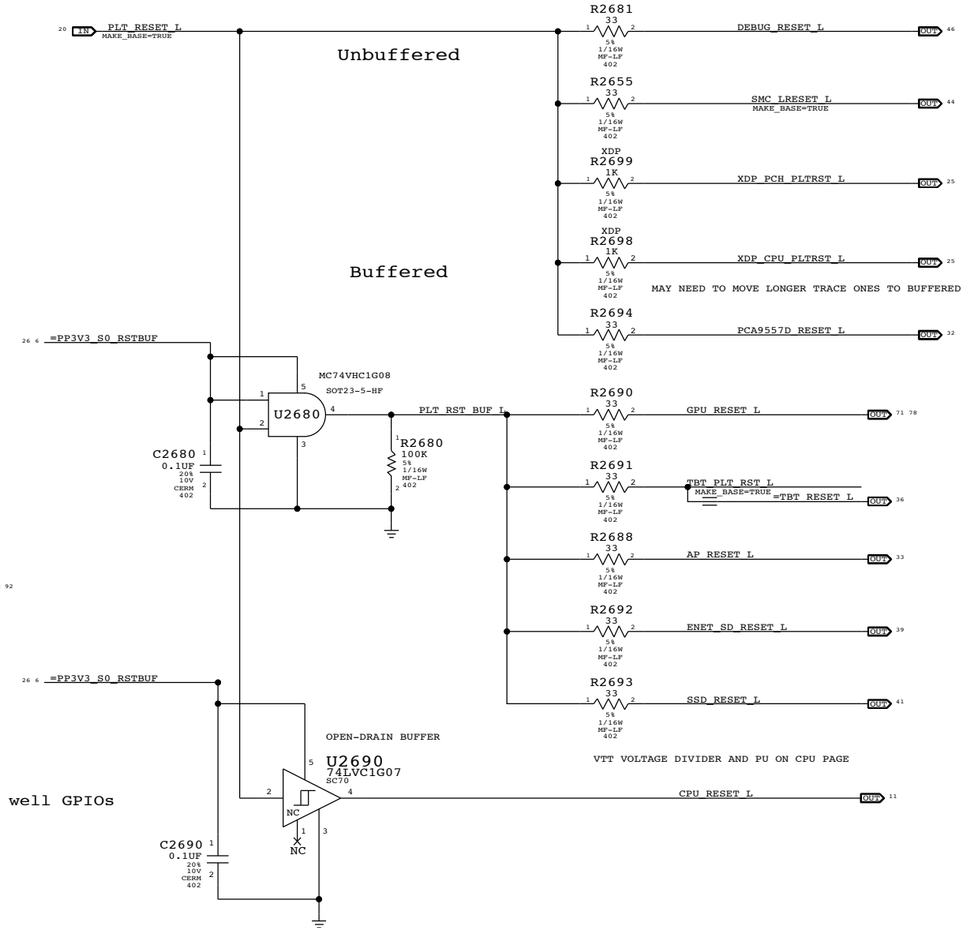
PCH 25MHZ CLOCK



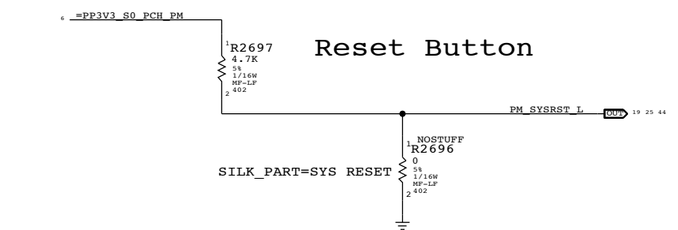
GPIO Isolation to prevent glitches on critical core well GPIOs



Platform Reset Connections



Reset Button



SYNC_MASTER=K70_MLB SYNC_DATE=11/30/2011

PAGE TITLE: CHIPSET SUPPORT

Apple Inc.

DRAWING NUMBER: 051-9509 SIZE: D

REVISION: 4.2.0

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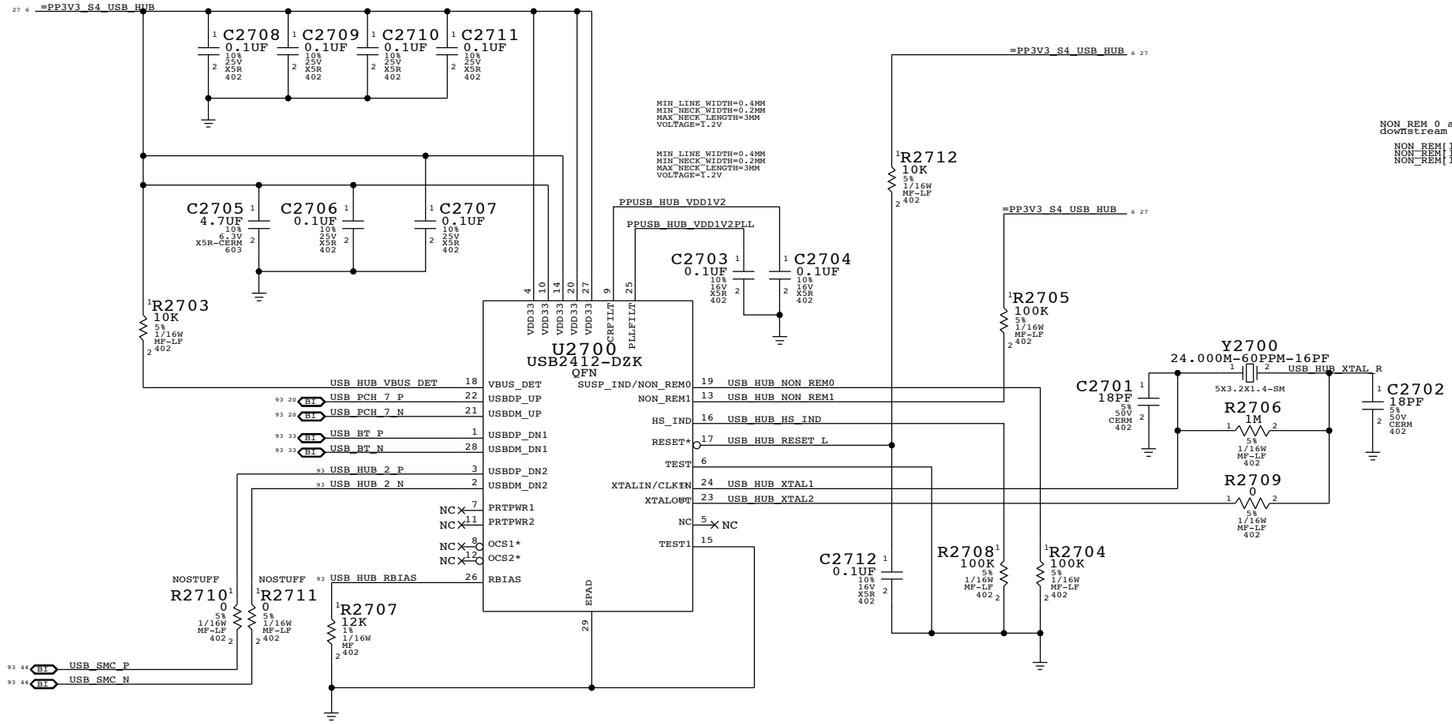

SYNC MASTER=D7 NICK SYNC DATE=12/13/2011

PAGE TITLE

USB HUB

Apple Inc.

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REVISION 4.2.0

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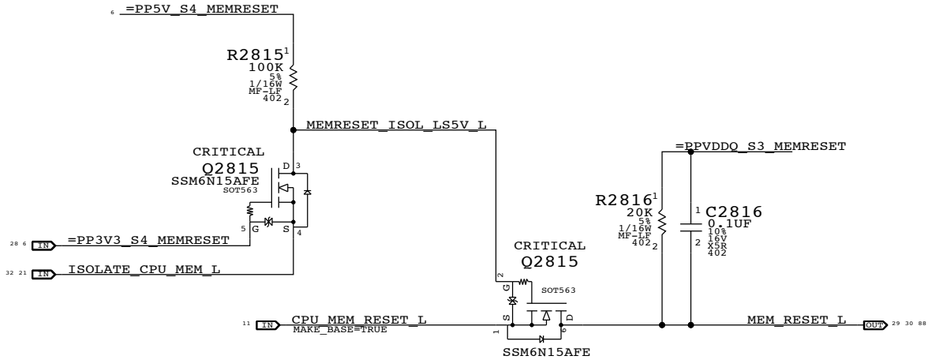
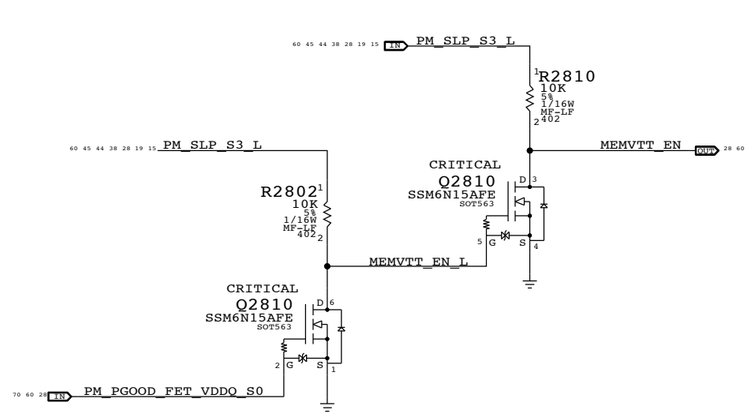
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

MEMVTT_EN = PM_PGOOD_FET_VDDQ_S0 * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L





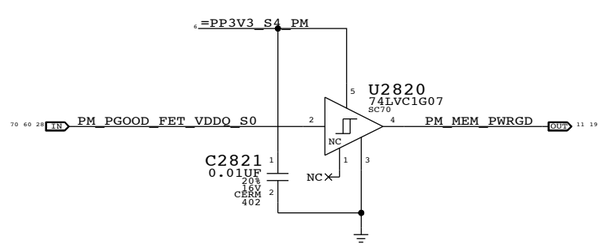
	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1
to	1	0	1	1	1	1	1
S3	2	0	0	1	1	1	0
	3	0	0	0	X	1	0
S3	4	0	0	1	X	1	0
to	5	0	1	1	0 (*)	1	1
S0	6	0	1	1	1	1	1
	7	1	1	1	1	CPU_MEM_RESET_L	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must de-assert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

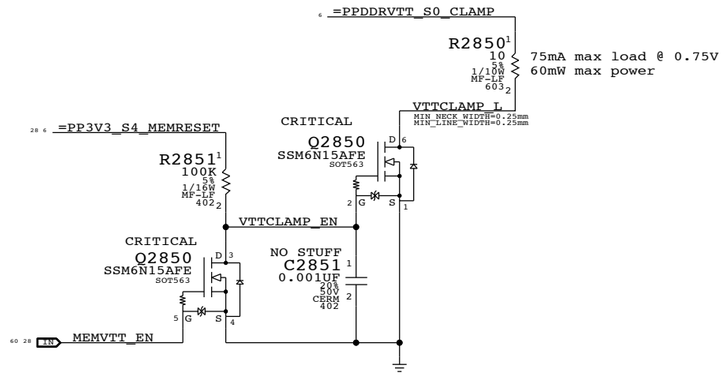
1V5 S0 "PGOOD" for CPU

PM_MEM_PWRGD pull-up to CPU VTT rail is on CPU page



MEMVTT Clamp

Ensures CKE signals are held low in S3



SYNC_MASTER=K70_MLB SYNC_DATE=11/30/2011

PAGE TITLE: CPU Memory S3 Support

Apple Inc.

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DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

=PPDDRVREF_DQ_MEM_A

C2930 2.2UF 20% 6.3V CERM 402-LF
C2931 0.1UF 20% 10V CERM 402

J2900 F-RT-SM
2013311

1	VREFDQ	VSS_0	2
3	VSS_1	DQ4	4
5	DQ0	DQ5	6
7	DQ1	VSS_2	8
9	VSS_3	DQS0*	10
11	DM0	DQS0	12
13	VSS_4	VSS_5	14
15	DQ2	DQ6	16
17	DQ3	DQ7	18
19	VSS_6	VSS_7	20
21	DQ8	DQ12	22
23	DQ9	DQ13	24
25	VSS_8	VSS_9	26
27	DQS1*	DM1	28
29	DQS1	RESET*	30
31	VSS_10	VSS_11	32
33	DQ10	DQ14	34
35	DQ11	DQ15	36
37	VSS_12	VSS_13	38
39	DQ16	DQ20	40
41	DQ17	DQ21	42
43	VSS_14	VSS_15	44
45	DQS2*	DM2	46
47	DQS2	VSS_16	48
49	VSS_17	DQ22	50
51	DQ18	DQ23	52
53	DQ19	VSS_18	54
55	VSS_19	DQ28	56
57	DQ24	DQ29	58
59	DQ25	VSS_20	60
61	VSS_21	DQS3*	62
63	DM3	DQS3	64
65	VSS_22	VSS_23	66
67	DQ26	DQ30	68
69	DQ27	DQ31	70
71	VSS_24	VSS_25	72
KEY			
73	CKE0	CKE1	74
75	VDD_0	VDD_1	76
77	NC_0	A15	78
79	BA2	A14	80
81	VDD_2	VDD_3	82
83	A12/BC*	A11	84
85	A9	A7	86
87	VDD_4	VDD_5	88
89	A8	A6	90
91	A5	A4	92
93	VDD_6	VDD_7	94
95	A3	A2	96
97	A1	A0	98
99	VDD_8	VDD_9	100
101	CK0	CK1	102
103	CK0*	CK1*	104
105	VDD_10	VDD_11	106
107	A10_AP	BA1	108
109	BA0	RAS*	110
111	VDD_12	VDD_13	112
113	WE*	S0*	114
115	CAS*	ODT0	116
117	VDD_14	VDD_15	118
119	A13	ODT1	120
121	S1*	NC_1	122
123	VDD_16	VDD_17	124
125	TEST	VREFCA	126
127	VSS_26	VSS_27	128
129	DQ32	DQ36	130
131	DQ33	DQ37	132
133	VSS_28	VSS_29	134
135	DQS4*	DM4	136
137	DQS4	VSS_30	138
139	VSS_31	DQ38	140
141	DQ34	DQ39	142
143	DQ35	VSS_32	144
145	VSS_33	DQ44	146
147	DQ40	DQ45	148
149	DQ41	VSS_34	150
151	VSS_35	DQS5*	152
153	DM5	DQS5	154
155	VSS_36	VSS_37	156
157	DQ42	DQ46	158
159	DQ43	DQ47	160
161	VSS_38	VSS_39	162
163	DQ48	DQ52	164
165	DQ49	DQ53	166
167	VSS_40	VSS_41	168
169	DQS6*	DM6	170
171	DQS6	VSS_42	172
173	VSS_43	DQ54	174
175	DQ50	DQ55	176
177	DQ51	VSS_44	178
179	VSS_45	DQ60	180
181	DQ56	DQ61	182
183	DQ57	VSS_46	184
185	VSS_47	DQS7*	186
187	DM7	DQS7	188
189	VSS_48	VSS_49	190
191	DQ58	DQ62	192
193	DQ59	DQ63	194
195	VSS_50	VSS_51	196
197	SA0	EVENT*	198
199	VDDSPD	SDA	200
201	SA1	SCL	202
203	VTT_0	VTT_1	204
205	MTG_PIN	MTG_PIN	206

=PPVDDQ_S3_MEM_A

C2910 0.1UF 20% 10V CERM 402
C2911 0.1UF 20% 10V CERM 402
C2912 0.1UF 20% 10V CERM 402
C2913 0.1UF 20% 10V CERM 402
C2914 0.1UF 20% 10V CERM 402
C2915 0.1UF 20% 10V CERM 402
C2916 0.1UF 20% 10V CERM 402
C2917 0.1UF 20% 10V CERM 402
C2902 0.1UF 20% 10V CERM 402

C2900 10UF 20% 6.3V X5R 603
C2901 10UF 20% 6.3V X5R 603
C2918 0.1UF 20% 10V CERM 402
C2919 0.1UF 20% 10V CERM 402
C2920 0.1UF 20% 10V CERM 402
C2921 0.1UF 20% 10V CERM 402
C2922 0.1UF 20% 10V CERM 402
C2923 0.1UF 20% 10V CERM 402
C2924 0.1UF 20% 10V CERM 402

=PPDDRVREF_CA_MEM_A

C2935 2.2UF 20% 6.3V CERM 402-LF
C2936 0.1UF 20% 10V CERM 402

=PPDDRVTT_S0_MEM_A

C2950 1UF 10% 10V X5R 402
C2951 1UF 10% 10V X5R 402
C2952 1UF 10% 10V X5R 402
C2953 1UF 10% 10V X5R 402

MEM_A_SA<1>
MEM_A_SA<0>
=PPSPD_S0_MEM_A

C2940 2.2UF 20% 6.3V CERM 402-LF
R2940 10K 5% 1/16W MF-LF 402
R2941 10K 5% 1/16W MF-LF 402

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MEM_A_SA<0>
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MEM_A_SA<1>

SYNC_MASTER=K70_MLB SYNC_DATE=11/30/2011

PAGE TITLE: DDR3 SO-DIMM Connector A

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REVISION: 4.2.0
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DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

J3100
F-RT-SM
2013290

1	VREFDQ	VSS_0	2
3	VSS_1	DQ4	4
5	DQ0	DQ5	6
7	DQ1	VSS_2	8
9	VSS_3	DQS0*	10
11	DM0	DQS0	12
13	VSS_4	VSS_5	14
15	DQ2	DQ6	16
17	DQ3	DQ7	18
19	VSS_6	VSS_7	20
21	DQ8	DQ12	22
23	DQ9	DQ13	24
25	VSS_8	VSS_9	26
27	DQS1*	DM1	28
29	DQS1	RESET*	30
31	VSS_10	VSS_11	32
33	DQ10	DQ14	34
35	DQ11	DQ15	36
37	VSS_12	VSS_13	38
39	DQ16	DQ20	40
41	DQ17	DQ21	42
43	VSS_14	VSS_15	44
45	DQS2*	DM2	46
47	DQS2	VSS_16	48
49	VSS_17	DQ22	50
51	DQ18	DQ23	52
53	DQ19	VSS_18	54
55	VSS_19	DQ28	56
57	DQ24	DQ29	58
59	DQ25	VSS_20	60
61	VSS_21	DQS3*	62
63	DM3	DQS3	64
65	VSS_22	VSS_23	66
67	DQ26	DQ30	68
69	DQ27	DQ31	70
71	VSS_24	VSS_25	72
KEY			
73	CKE0	CKE1	74
75	VDD_0	VDD_1	76
77	NC_0	A15	78
79	BA2	A14	80
81	VDD_2	VDD_3	82
83	A12/BC*	A11	84
85	A9	A7	86
87	VDD_4	VDD_5	88
89	A8	A6	90
91	A5	A4	92
93	VDD_6	VDD_7	94
95	A3	A2	96
97	A1	A0	98
99	VDD_8	VDD_9	100
101	CK0	CK1	102
103	CK0*	CK1*	104
105	VDD_10	VDD_11	106
107	A10_AP	BA1	108
109	BA0	RAS*	110
111	VDD_12	VDD_13	112
113	WE*	S0*	114
115	CAS*	ODT0	116
117	VDD_14	VDD_15	118
119	A13	ODT1	120
121	S1*	NC_1	122
123	VDD_16	VDD_17	124
125	TEST	VREFCA	126
127	VSS_26	VSS_27	128
129	DQ32	DQ36	130
131	DQ33	DQ37	132
133	VSS_28	VSS_29	134
135	DQS4*	DM4	136
137	DQS4	VSS_30	138
139	VSS_31	DQ38	140
141	DQ34	DQ39	142
143	DQ35	VSS_32	144
145	VSS_33	DQ44	146
147	DQ40	DQ45	148
149	DQ41	VSS_34	150
151	VSS_35	DQS5*	152
153	DM5	DQS5	154
155	VSS_36	VSS_37	156
157	DQ42	DQ46	158
159	DQ43	DQ47	160
161	VSS_38	VSS_39	162
163	DQ48	DQ52	164
165	DQ49	DQ53	166
167	VSS_40	VSS_41	168
169	DQS6*	DM6	170
171	DQS6	VSS_42	172
173	VSS_43	DQ54	174
175	DQ50	DQ55	176
177	DQ51	VSS_44	178
179	VSS_45	DQ60	180
181	DQ56	DQ61	182
183	DQ57	VSS_46	184
185	VSS_47	DQS7*	186
187	DM7	DQS7	188
189	VSS_48	VSS_49	190
191	DQ58	DQ62	192
193	DQ59	DQ63	194
195	VSS_50	VSS_51	196
197	SA0	EVENT*	198
199	VDDSPD	SDA	200
201	SA1	SCL	202
203	VTT_0	VTT_1	204
205	MTG_PIN	MTG_PIN	206

SYNC_MASTER=K70_MLB	SYNC_DATE=11/30/2011
PAGE TITLE: DDR3 SO-DIMM CONNECTOR B	
Apple Inc.	DRAWING NUMBER: 051-9509 SIZE: D
	REVISION: 4.2.0
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MEM_A_DQS_N<0>	MAKE_BASE=TRUE	=MEM_A_DQS_N<0>
MEM_A_DQS_P<0>	MAKE_BASE=TRUE	=MEM_A_DQS_P<0>
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MEM_A_DQS_P<2>	MAKE_BASE=TRUE	=MEM_A_DQS_P<2>
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MEM_A_DQ<17>	MAKE_BASE=TRUE	=MEM_A_DQ<17>
MEM_A_DQ<16>	MAKE_BASE=TRUE	=MEM_A_DQ<16>
MEM_A_DQS_N<3>	MAKE_BASE=TRUE	=MEM_A_DQS_N<3>
MEM_A_DQS_P<3>	MAKE_BASE=TRUE	=MEM_A_DQS_P<3>
MEM_A_DQ<31>	MAKE_BASE=TRUE	=MEM_A_DQ<31>
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MEM_A_DQ<29>	MAKE_BASE=TRUE	=MEM_A_DQ<29>
MEM_A_DQ<28>	MAKE_BASE=TRUE	=MEM_A_DQ<28>
MEM_A_DQ<27>	MAKE_BASE=TRUE	=MEM_A_DQ<27>
MEM_A_DQ<26>	MAKE_BASE=TRUE	=MEM_A_DQ<26>
MEM_A_DQ<25>	MAKE_BASE=TRUE	=MEM_A_DQ<25>
MEM_A_DQ<24>	MAKE_BASE=TRUE	=MEM_A_DQ<24>
MEM_A_DQS_N<4>	MAKE_BASE=TRUE	=MEM_A_DQS_N<4>
MEM_A_DQS_P<4>	MAKE_BASE=TRUE	=MEM_A_DQS_P<4>
MEM_A_DQ<39>	MAKE_BASE=TRUE	=MEM_A_DQ<39>
MEM_A_DQ<38>	MAKE_BASE=TRUE	=MEM_A_DQ<38>
MEM_A_DQ<37>	MAKE_BASE=TRUE	=MEM_A_DQ<37>
MEM_A_DQ<36>	MAKE_BASE=TRUE	=MEM_A_DQ<36>
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SYNC_MASTER=K70_MLB SYNC_DATE=11/30/2011

PAGE TITLE
DDR3 ALIASES AND BITSWAPS

Apple Inc.

DRAWING NUMBER 051-9509 SIZE D

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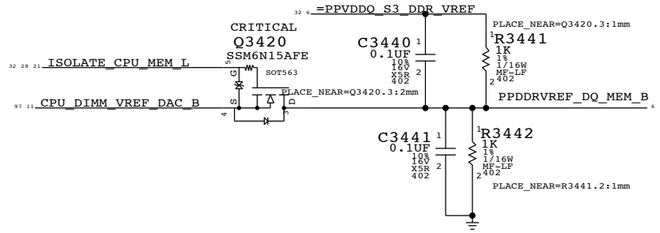
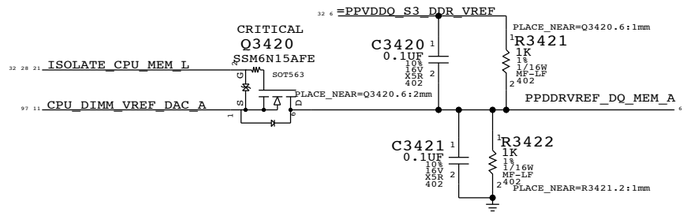
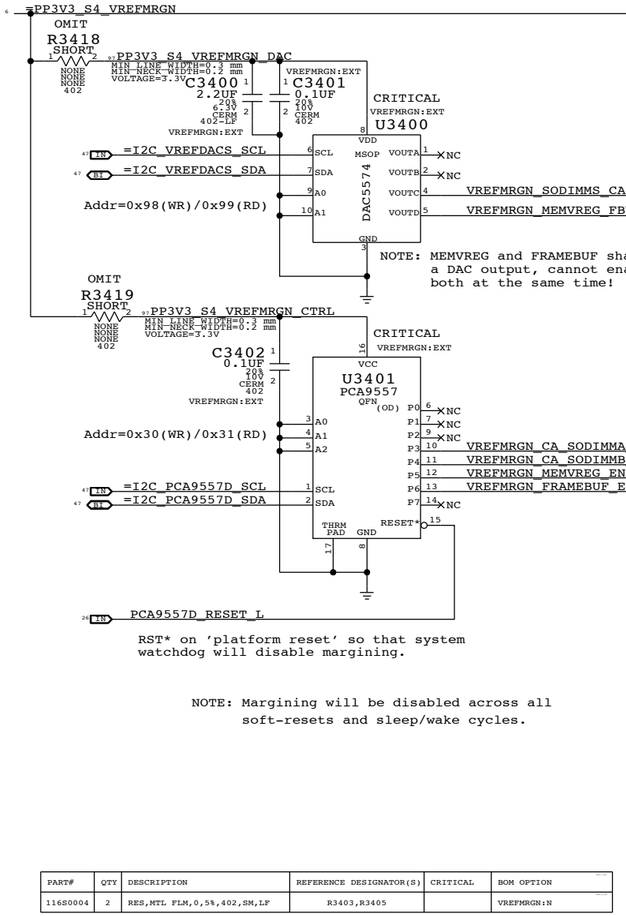
VRef DQ

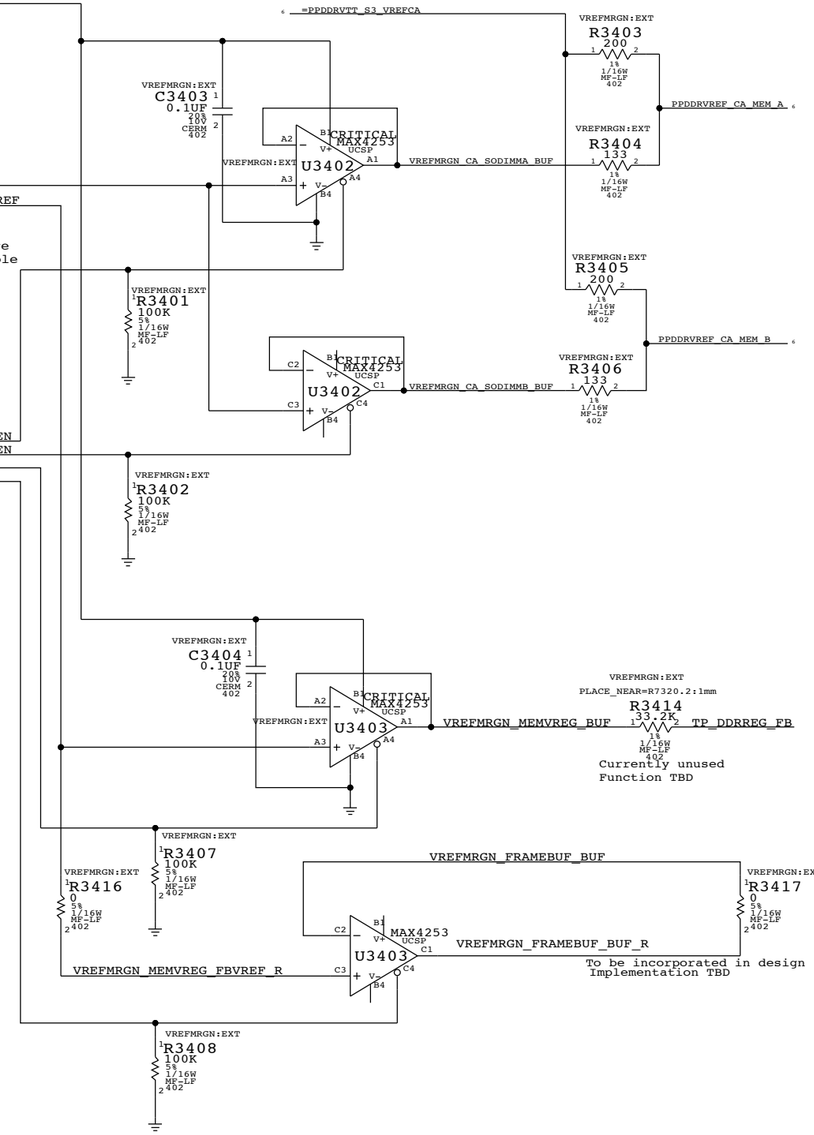
Driven by CPU

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step









PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FLM,0,5%,402,SM,LF	R3403,R3405		VREFMRGN:N

	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	C	C	D	D
PCA9557D Pin:	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)		1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)		1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)		0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)		+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output		8.59mV / step @ output	1.51mV / step @ output

SYNC MASTER=K70_MLB SYNC DATE=11/30/2011

PAGE TITLE
DDR3/FRAMEBUF VREF MARGINING

Apple Inc.

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AIRPORT BLUETOOTH

AP & BT Load Switch

SWITCH	TPS22924B
CHANNEL	N-TYPE
RDS(ON)	18.4 MOHM @3.3V
LOADING	2 A (EDP)

=PP3V3_S4_AP → U3510 TPS22924B CSP (VIN, VOUT, ON, GND) → PP3V3_S4_AP_FET
MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V
AP_PWR_EN

L3502 CRITICAL 220-OHM-1.4A 0603
PP3V3_S4_AP_FET → PP3V3_S4_AP_FLT
MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V

C3502 0.1UF 10% 16V X5R 402
C3503 0.1UF 10% 16V X5R 402
C3504 10UF 20% 6.3V X5R 603

C3505 0.1UF 10% X5R 6.3V 201 (PLACE_NEAR=J3500.4:3mm)
C3506 0.1UF 10% X5R 6.3V 201 (PLACE_NEAR=J3500.5:3mm)

PCIE_AP_R2D_C_N
PCIE_AP_R2D_C_P

514S0335 CRITICAL
J3500 SSD-K99 F-RT-SM1

AP_EVENT_L
PCIE_AP_R2D_N
PCIE_AP_R2D_P
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
PCIE_AP_D2R_P
PCIE_AP_D2R_N
AP_WAKE_L
AP_RESET_CONN_L
AP_CLKREQ_O_L
USB_BT_MUX_N
USB_BT_MUX_P

=PP3V3_G3H_BT → U3540 TPS22924B CSP → PP3V3_G3H_BT_FET
VOLTAGE=3.3V, MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.2MM

L3501 CRITICAL 220-OHM-1.4A 0603
PP3V3_G3H_BT_FET → PP3V3_G3H_BT_FLT
VOLTAGE=3.3V, MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.2MM

C3507 0.1UF 10% 16V X5R 402
C3508 10UF 20% 6.3V X5R 603

SMC_S4_WAKESRC_EN
R3542 10K 5% 1/16W MF-LF 402

CRITICAL
Q3540 SSM6L36FE SOT563 P-CH N-CH
BT_PWR_RST_L
=PP3V3_S0_BT
BT_PWR_RST
BT_PWR_EN
R3543 10K 5% 1/16W MF-LF 402

Wake from BT in G3H circuit

SMC_PME_S4_WAKE_L
Q3501 SSM3K15FV SOD-VESM-HF
R3500 15K 1% 1/20W MF 201
R3501 15K 1% 1/20W MF 201
C3500 0.1UF 20% 10V CERM 402
U3501 USB3740 DFN
USB_BT_N
USB_BT_P
USB_BT_WAKEN
USB_BT_WAKEP
USB_BT_MUX_N
USB_BT_MUX_P
R3502 0 5% 1/16W MF-LF 402
PM_SLP_S5_L
C3501 0.1UF 20% 10V CERM 402 NOSTUFF
SIGNAL_MODEL=SWI_USB3740_DFN_USB3740_MOJO

Supervisor & CLKFREG # Isolation
Delay = 60 ms +/- 20%

PP3V3_S4_AP_FLT
=PP3V3_S4_AP
R3530 100K 1% 1/16W MF-LF 402
R3531 232K 1% 1/16W MF-LF 402
R3532 100K 1% 1/16W MF-LF 402
C3530 0.1uF 20% 10V CERM 402
CRITICAL
U3530 SLG4AP016V TDFN
P3V3AP_VMON
SENSE 0.7V
DLY
RESET*
MR*
EN
OUT (OD)
IN
THRM PAD
GND
AP_RESET_CONN_L
AP_CLKREQ_O_L
AP_RESET_L
AP_PWR_EN
AP_CLKREQ_L

Q3570 SSM3K15FV SOD-VESM-HF
PCIE_WAKE_L
R3570 10K 5% 1/16W MF-LF 402
AP_WAKE_L

SYNC MASTER=D7 NICK	SYNC DATE=12/13/2011
PAGE TITLE	AIRPORT/BT
Apple Inc.	DRAWING NUMBER 051-9509
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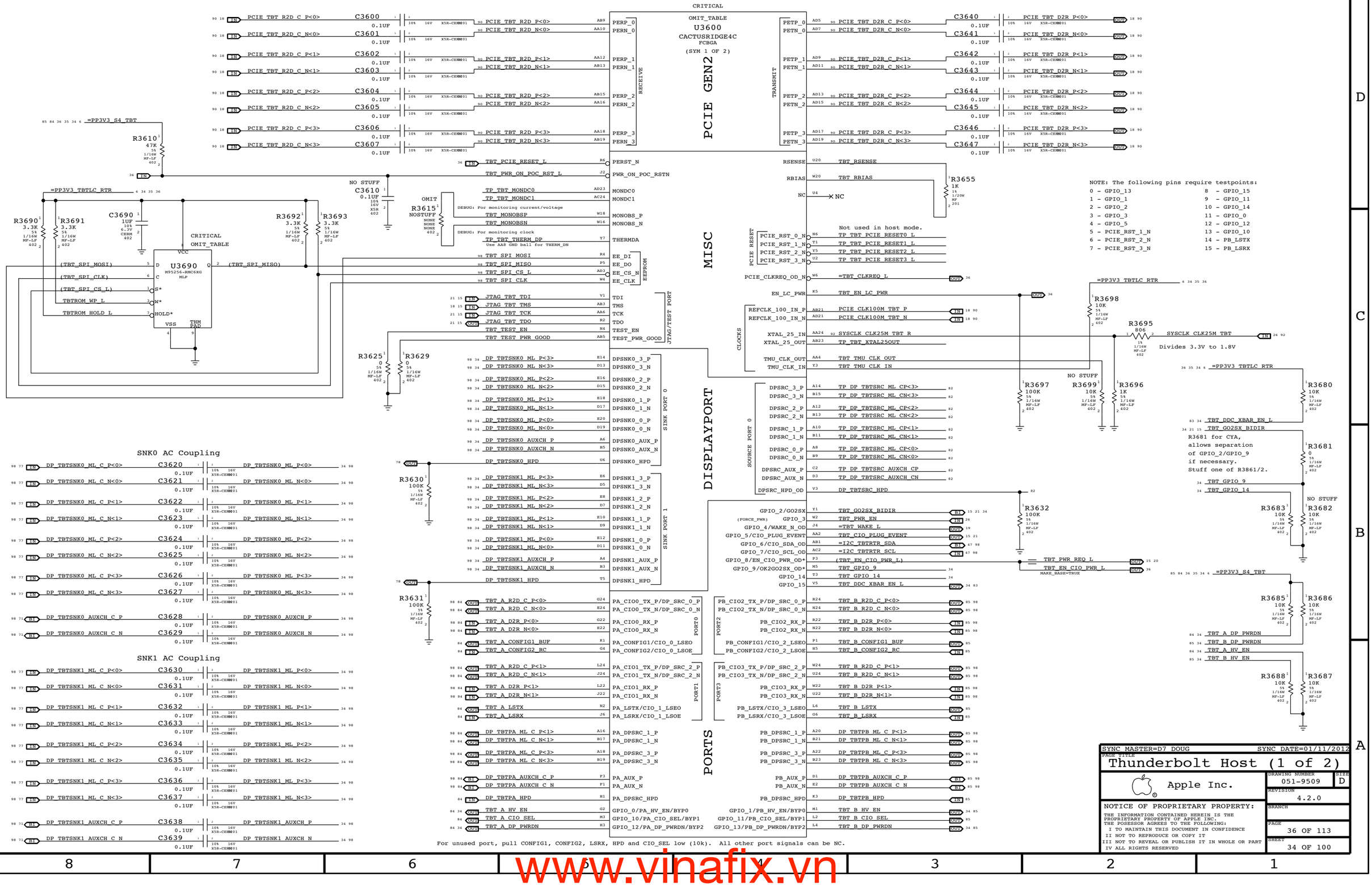

SYNC_MASTER=D7 DOUG SYNC_DATE=01/11/2012

PAGE TITLE

Thunderbolt Host (1 of 2)

Apple Inc.

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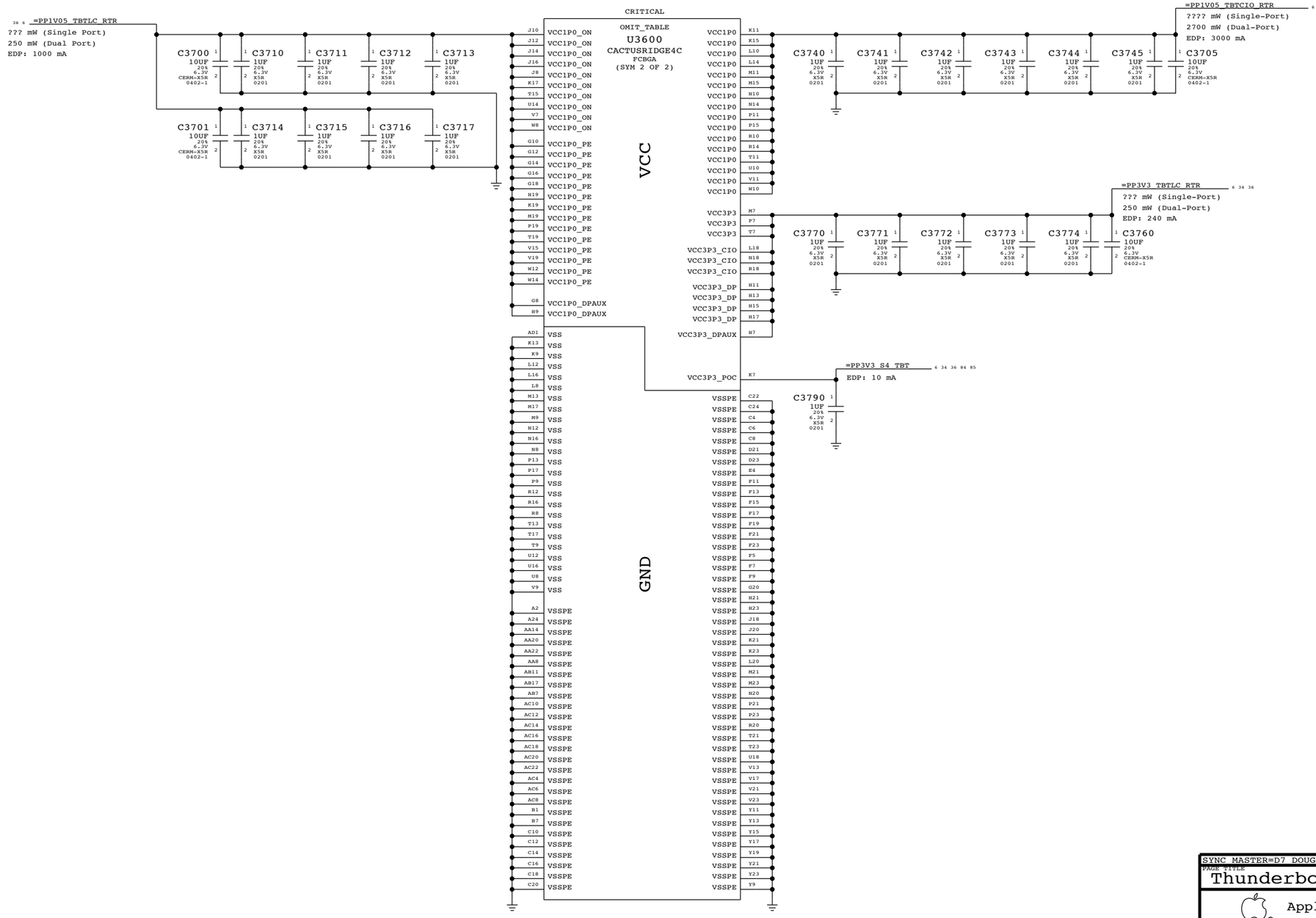

EDP current / power consumption figures from CR DG v0.57, IBL doc #472455.

SYNC MASTER=D7 DOUG SYNC DATE=01/11/2012

PAGE TITLE: Thunderbolt Host (2 of 2)

Apple Inc.

DRAWING NUMBER: 051-9509 SIZE: D

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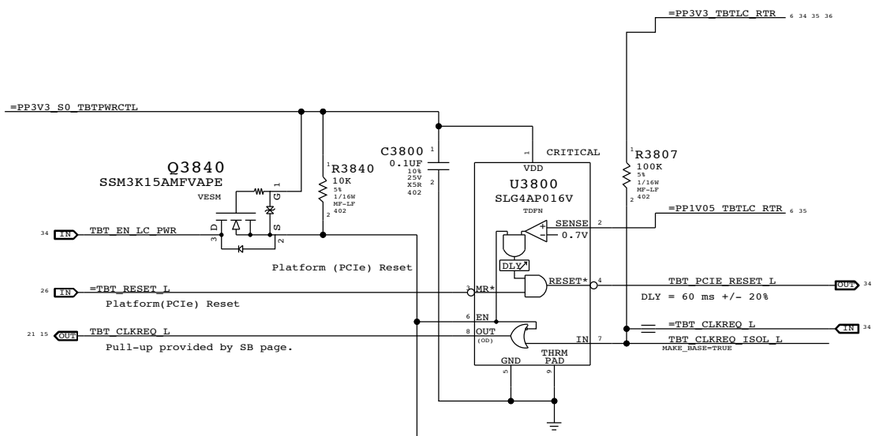
Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)
- =PP3V3_TBT_P3V3TBTFET (3.3V FET Input)
- =PP3V3_TBT_FET (3.3V FET Output)
- =PP3V3_S0_TBTPWRCTL
- =PP1V05_TBT_P1V05TBTFET (1.05V FET Input)
- =PP1V05_TBT_FET (1.05V FET Output)

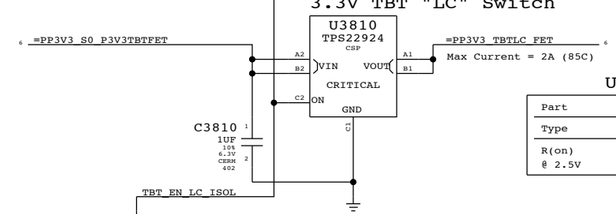
Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

BOM options provided by this page:
TBTBST:Y - Stuffs 15V boost circuitry.

Supervisor & CLKREQ# Isolation

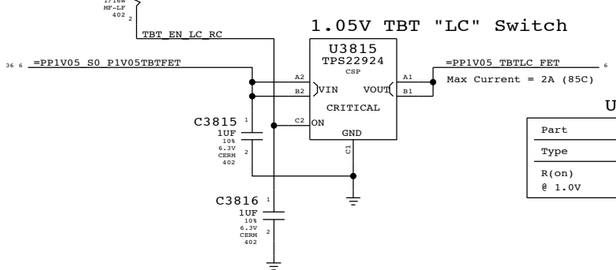


3.3V TBT "LC" Switch



U3810	
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

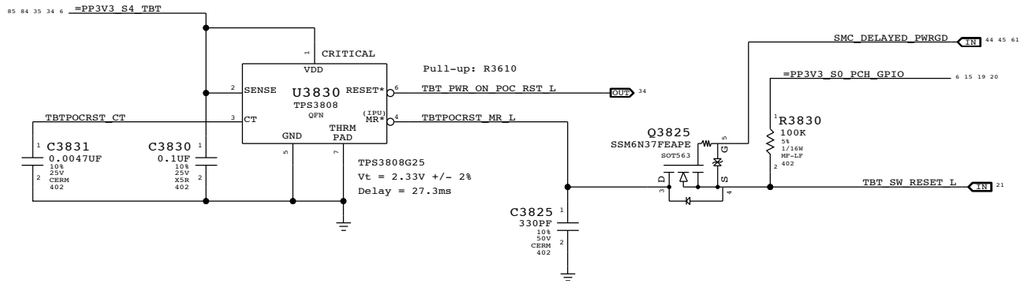
1.05V TBT "LC" Switch



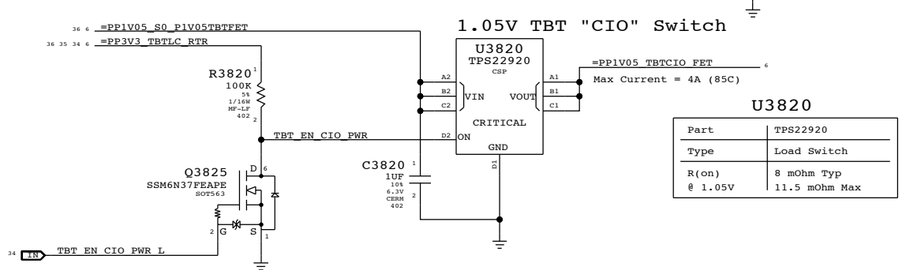
U3815	
Part	TPS22924C
Type	Load Switch
R(on) @ 1.0V	20.3 mOhm Typ 28.6 mOhm Max

TBT "POC" Power-up Reset

Intel investigating whether RC is sufficient.



1.05V TBT "CIO" Switch



U3820	
Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	8 mOhm Typ 11.5 mOhm Max

SYNC_MASTER=D7_DOUG SYNC_DATE=01/11/2012

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Thunderbolt Power Support

Apple Inc.

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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

=PP3V3_ENET_PHY
281mA (1000base-T max power, Caesar IV)

VDD for Card Reader I/O
PP3V3R1V8_CR_VDDIO
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.15 mm
VOLTAGE=3.3V

CRITICAL
L3900
FERR-600-OHM-300MA-0.85OHM
0402
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
C3900 0.1UF 10% 16V X5R-CERM 0201
ENET_XTALVDDH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

CRITICAL
L3905
FERR-600-OHM-300MA-0.85OHM
0402
PP3V3_ENET_PHY_BIASVDDH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
C3905 0.1UF 10% 16V X5R-CERM 0201

CRITICAL
L3910
FERR-600-OHM-300MA-0.85OHM
0402
PP3V3_ENET_PHY_AVDDH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
R3910 4.7K 5% 1/16W MF-LF 402
C3910 0.1UF 10% 16V X5R-CERM 0201
C3911 0.1UF 10% 16V X5R-CERM 0201

R3940 4.7K 5% 1/16W MF-LF 402
R3941 4.7K 5% 1/16W MF-LF 402
C3915 4.7UF 20% 6.3V X5R-CERM1 402
C3916 0.1UF 10% 16V X5R-CERM 0201

=PP3V3_S0_ENET
R3942 1K 5% 1/16W MF-LF 402 Current Limiting Resistor

C3950 0.1UF 10% 16V X5R-CERM 0201
C3951 0.1UF 10% 16V X5R-CERM 0201
C3955 0.1UF 10% 16V X5R-CERM 0201
C3956 0.1UF 10% 16V X5R-CERM 0201

PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_P
PCIE_ENET_R2D_C_N
=ENET_WAKE_L
(See note)

WAKE#

Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

ENET_VMAIN_PRSNT
PCIE_ENET_D2R_C_N
PCIE_ENET_D2R_C_P
PCIE_ENET_R2D_P
PCIE_ENET_R2D_N
PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N
ENET_RESET_L
ENET_CLKREQ_L
ENET_SCLK
ENET_MISO
ENET_MOSI
ENET_CS_L
ENET_CR_3V3_EN_L
ENET_TRAFFICLED_L
SYSCLK_CLK25M_ENET
ENET_RDAC

ENET_SR_LX
ENET_SR_VFB
Internal 1.2V Switching Regulator pins.

=PP1V2_ENET_PHY
396mA (1000base-T, Caesar II)

CRITICAL
L3920
FERR-600-OHM-300MA-0.85OHM
0402
PP1V2_ENET_PHY_AVDDL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
C3921 0.1UF 10% 16V X5R-CERM 0201
C3920 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL
L3925
FERR-600-OHM-0.5A
SM
PP1V2_ENET_PHY_PCIEPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
C3926 0.1UF 10% 16V X5R-CERM 0201
C3925 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL
L3930
FERR-600-OHM-300MA-0.85OHM
0402
PP1V2_ENET_PHY_GPHYPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.15 mm
VOLTAGE=1.2V
C3931 0.1UF 10% 16V X5R-CERM 0201
C3930 4.7UF 20% 6.3V X5R-CERM1 402

C3936 0.1UF 10% 16V X5R-CERM 0201
C3935 10UF 20% 6.3V X5R 603

AVDDH, BIASVDDH, XTALVDDH, VDDO, SR_VDD, SR_VDDP, SR_LX, SR_VFB, AVDDL, PCIE_PLLVDDL, GPHY_PLLVDDL, VDDC

OMIT_TABLE
U3900
BCM57766C0KMLG
QFN-8X8

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

TRD0_P, TRD0_N, TRD1_P, TRD1_N, TRD2_P, TRD2_N, TRD3_P, TRD3_N
ENETCONN_MDI_P<0>, ENETCONN_MDI_N<0>, ENETCONN_MDI_P<1>, ENETCONN_MDI_N<1>, ENETCONN_MDI_P<2>, ENETCONN_MDI_N<2>, ENETCONN_MDI_P<3>, ENETCONN_MDI_N<3>

PP3V3R1V8_ENET_LR_OUT
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.15 mm
VOLTAGE=3.3V

GPIO_0/CR_ACT_LED*
GPIO_1/LR_OUT
GPIO_2/MEDIA_SENSE
ENET_CR_1V8_EN
ENET_MEDIA_SENSE

NOTE: "IPx" == Programmable pull-up/down

SD_DETECT
SD_DETECT can only be used active low due to errata.
ENET_SD_DETECT_L
SDCONN_CMD
SDCONN_CLK
SDCONN_DATA<0>, SDCONN_DATA<1>, SDCONN_DATA<2>, SDCONN_DATA<3>, SDCONN_DATA<4>, SDCONN_DATA<5>, SDCONN_DATA<6>, SDCONN_DATA<7>
R3961 33 5% 1/20W MF 201
R3979 33 5% 1/20W MF 201
R3971 33 5% 1/20W MF 201
R3972 33 5% 1/20W MF 201
R3973 33 5% 1/20W MF 201
R3974 33 5% 1/20W MF 201
R3975 33 5% 1/20W MF 201
R3976 33 5% 1/20W MF 201
R3977 33 5% 1/20W MF 201
R3978 33 5% 1/20W MF 201

CR_CMD, CR_CLK, CR_DATA0, CR_DATA1, CR_DATA2, CR_DATA3, CR_DATA4, CR_DATA5, CR_DATA6, CR_DATA7
ENET_SD_CMD, ENET_SD_CLK
ENET_CR_DATA<0>, ENET_CR_DATA<1>, ENET_CR_DATA<2>, ENET_CR_DATA<3>, ENET_CR_DATA<4>, ENET_CR_DATA<5>, ENET_CR_DATA<6>, ENET_CR_DATA<7>

No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.

MS_INS*
CR_LED*/CR_BUS_PWR
CR_WP*
SR_DISABLE
ENET_CR_PWREN
ENET_SR_DISABLE
R3981 1K 5% 1/16W MF-LF 402
(See note)

SDCONN_WP
ENET supports both active-levels for WP.

ENET 1.2V SR IS ENABLED IF FLOATING.

ENET_CR Signals

BCM requests SD CR[0:7], CMD, CLK termination.

ENET_SR_DISABLE

If ENET switching regulator is used, this pin can float (alias to TP_). If not used, must be pulled to 3.3V ENET via 1K resistor (not provided on this page).

PLACEMENT_NOTE=PLACE R3961 NEAR U3900
PLACEMENT_NOTE=PLACE R3979 NEAR U3900
PLACEMENT_NOTE=PLACE R3971 NEAR U3900
PLACEMENT_NOTE=PLACE R3972 NEAR U3900
PLACEMENT_NOTE=PLACE R3973 NEAR U3900
PLACEMENT_NOTE=PLACE R3974 NEAR U3900
PLACEMENT_NOTE=PLACE R3975 NEAR U3900
PLACEMENT_NOTE=PLACE R3976 NEAR U3900
PLACEMENT_NOTE=PLACE R3977 NEAR U3900
PLACEMENT_NOTE=PLACE R3978 NEAR U3900

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Avoids need for EFI to program at startup.
(Required ROM size 1 Mbit)

=PP3V3_ENET_PHY
C3990 0.1UF 10% 16V X5R-CERM 0201
U3990
AT45DB011D
SOIC-8S1
OMIT_TABLE
VCC, SCK, CS*, WP*, RESET*, SI, SO, GND
ENET_SCLK
ENET_CS_L
ENET_MOSI
ENET_MISO
NOSTUFF
R3990 4.7K 5% 1/16W MF-LF 402
R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC_MASTER=D7 NICK
SYNC_DATE=01/12/2012
PAGE TITLE
ETHERNET PHY (CAESAR IV)
Apple Inc.
DRAWING NUMBER 051-9509
SIZE D
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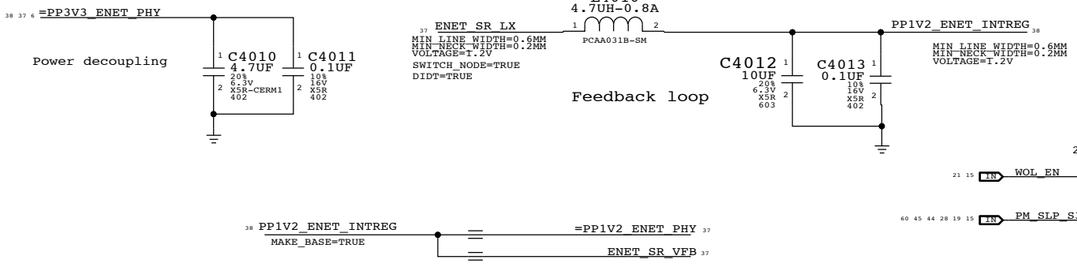
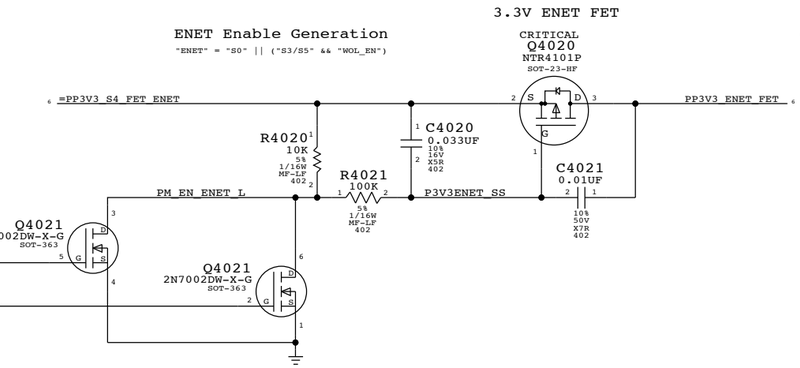
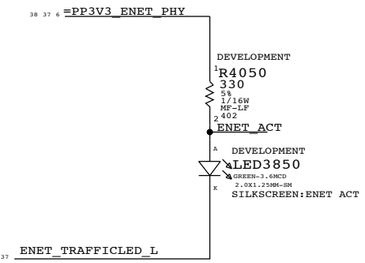
CAESAR IV 1.2V INT.VR CMPTS



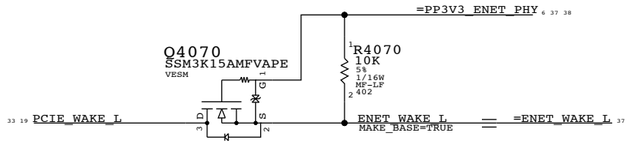
3.3V ENET FET

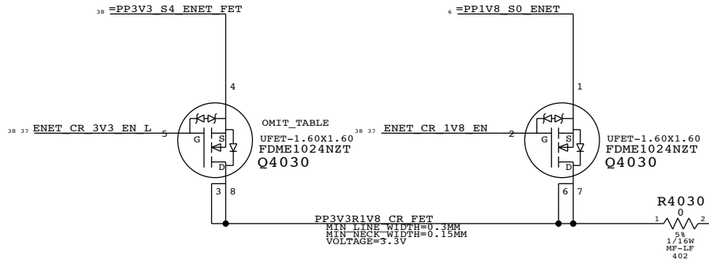


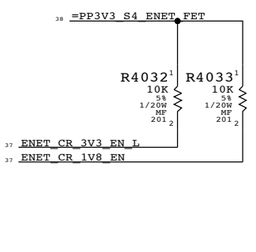
CAESAR IV ACTIVITY LED

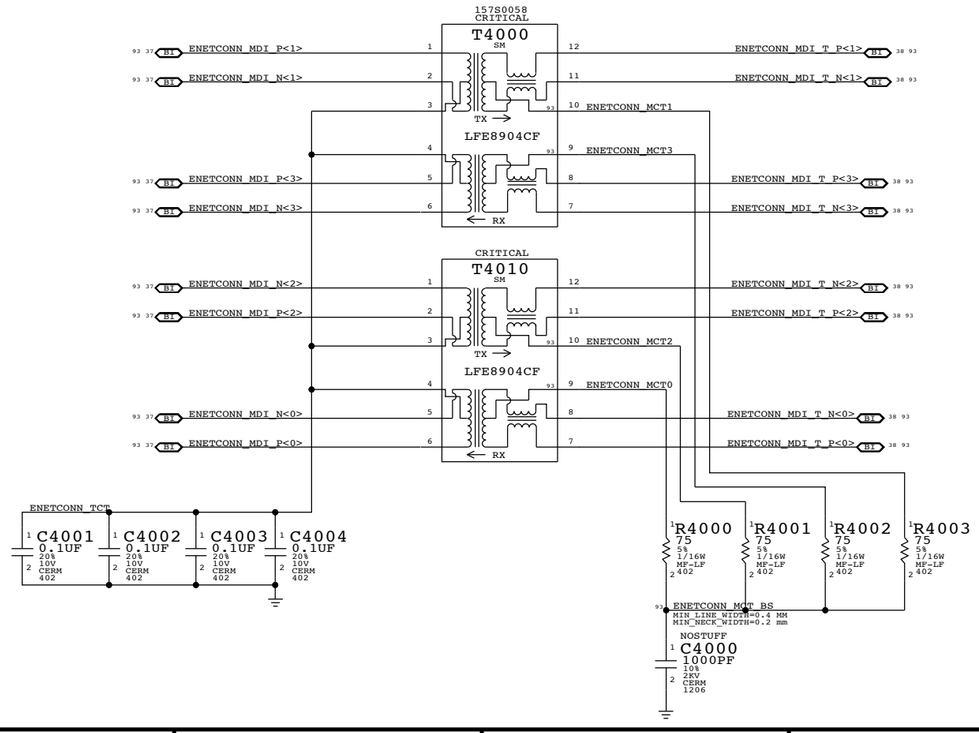


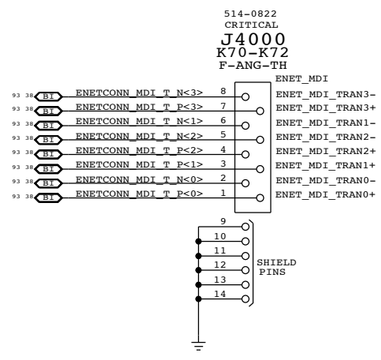
CAESAR IV WAKE# ISOLATION











PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
376S1092	1	MOSFET,COMP N-/P-CH,20V,3.8/2.6A	Q4030	CRITICAL	

SYNC_MASTER=D7 NICK SYNC_DATE=01/12/2012

PAGE TITLE: Ethernet Support & Connector

Apple Inc.

DRAWING NUMBER: 051-9509 SIZE: D

REVISION: 4.2.0

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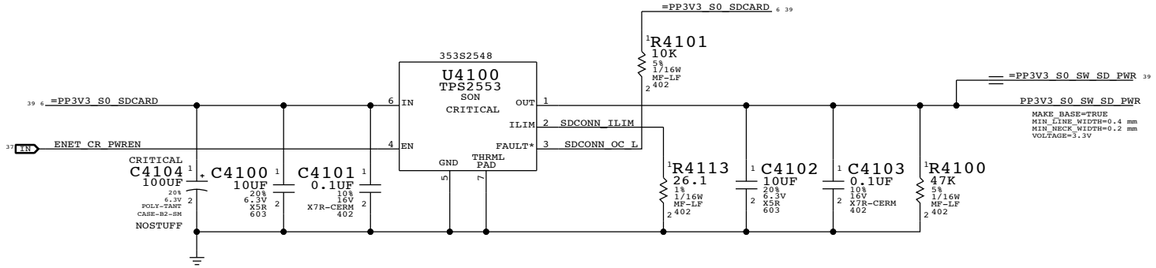
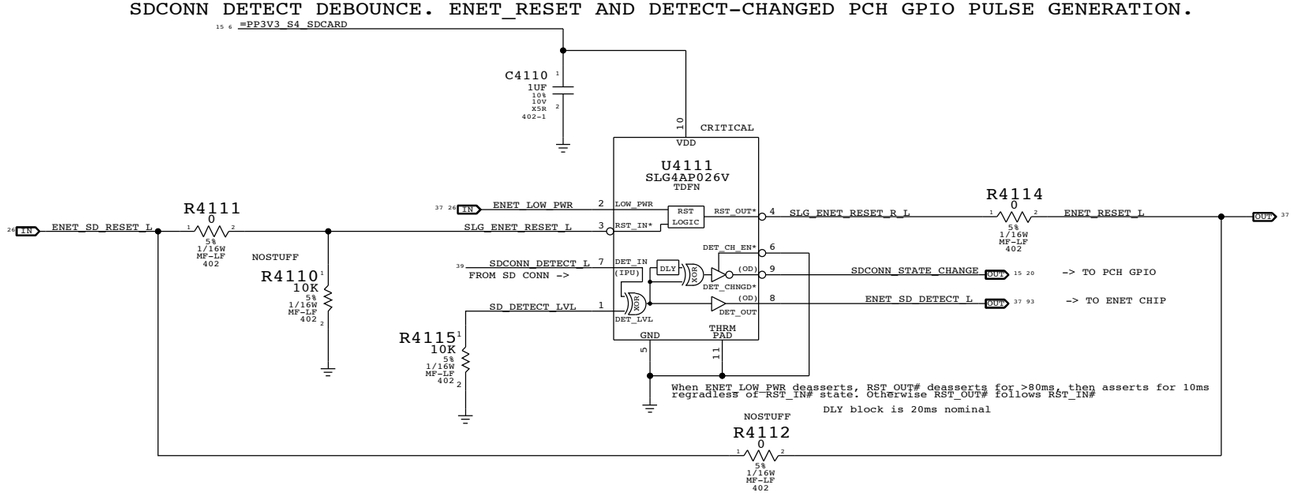
SD CARD 3.3V OVERCURRENT PROTECTION CHIP



SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.



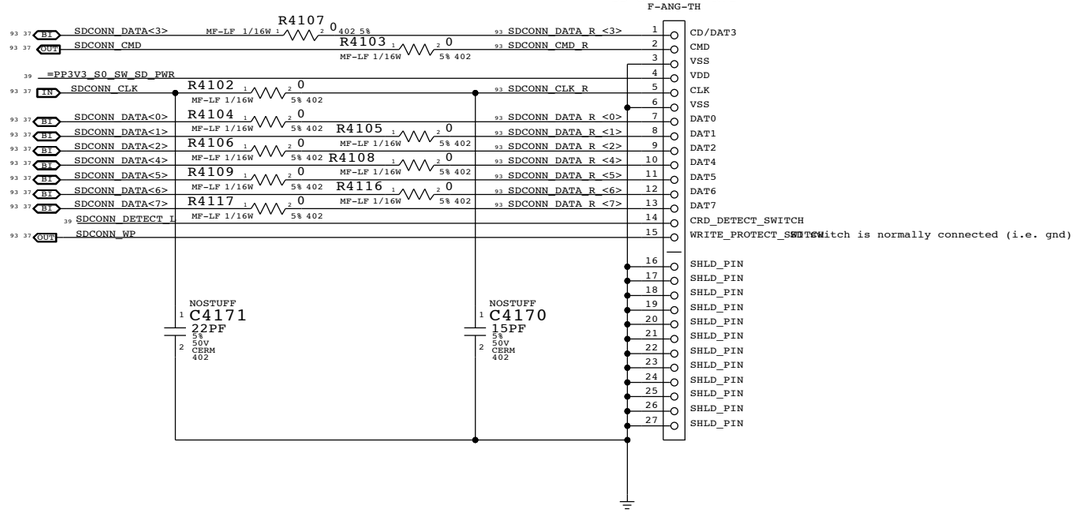
516-0249

SD CARD CONNECTOR

J4100

SD-CARD-K70-K72

F-ANG-TH



SYNC MASTER=D7 NICK SYNC DATE=01/12/2012

PAGE TITLE

SD READER CONNECTOR

Apple Inc.

DRAWING NUMBER 051-9509 SIZE D

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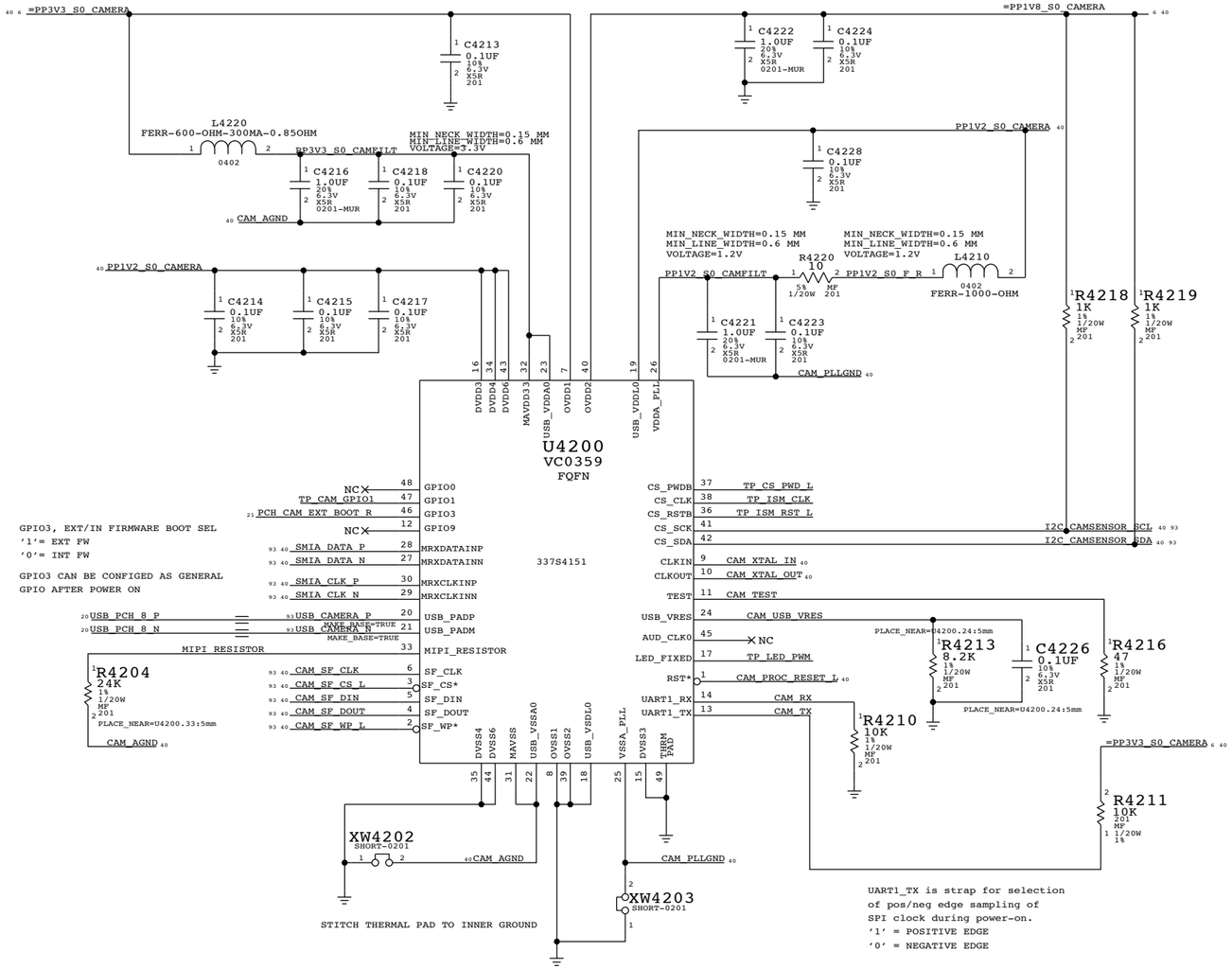
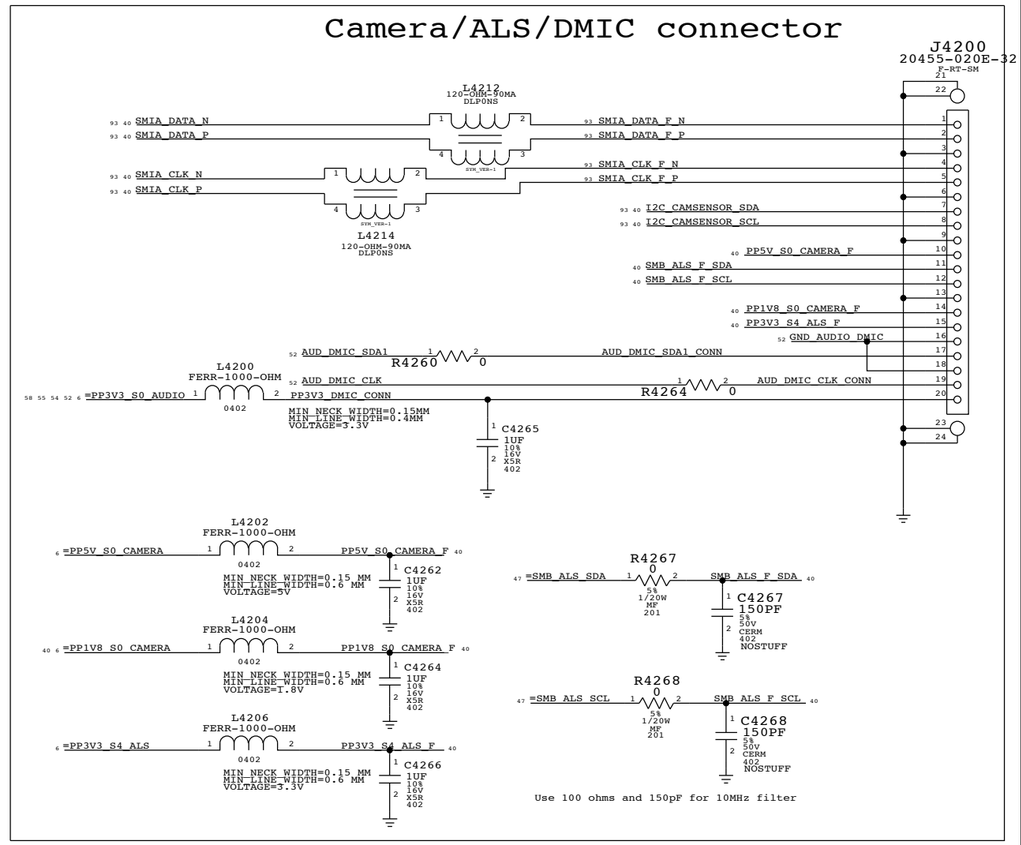
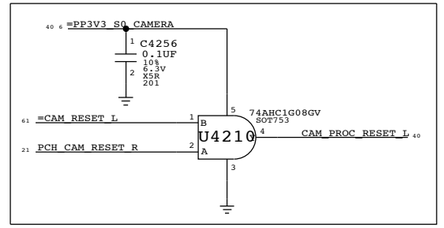
USB CAMERA CONTROLLER

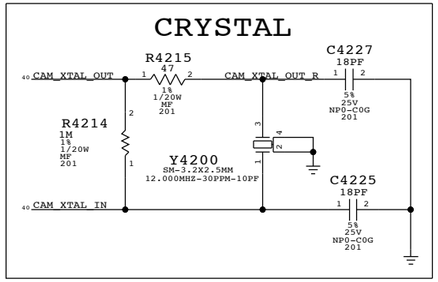


Camera/ALS/DMIC connector

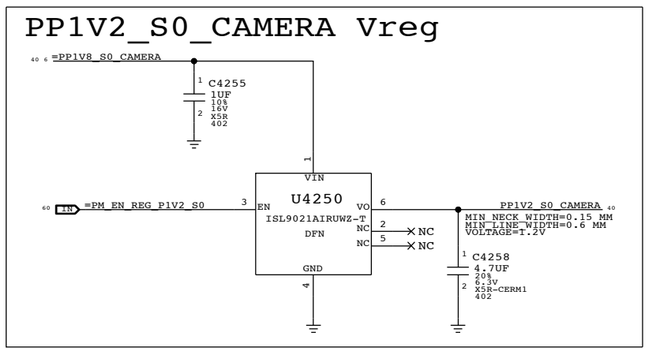




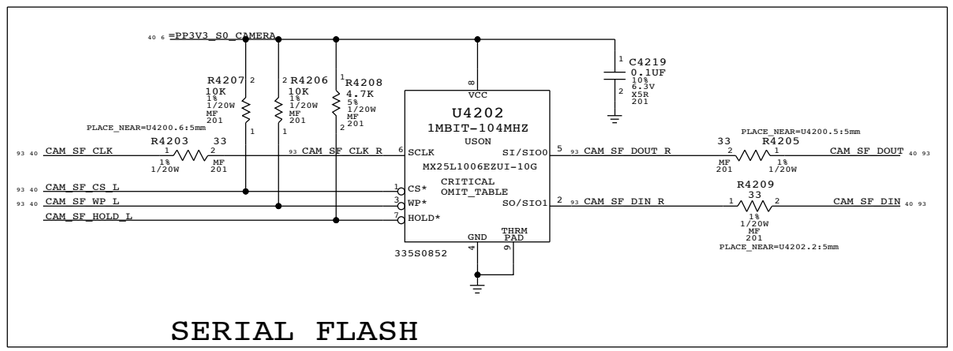
CRYSTAL



PP1V2_S0_CAMERA Vreg



SERIAL FLASH



PAGE TITLE: Camera Controller

Apple Inc.

DRAWING NUMBER 051-9509 SIZE D
REVISION 4.2.0
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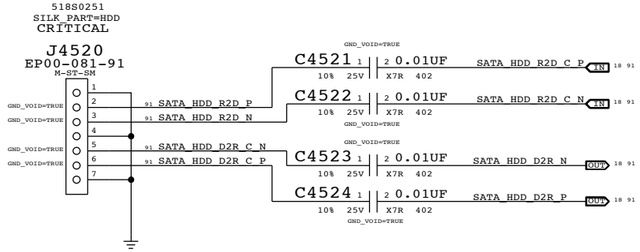
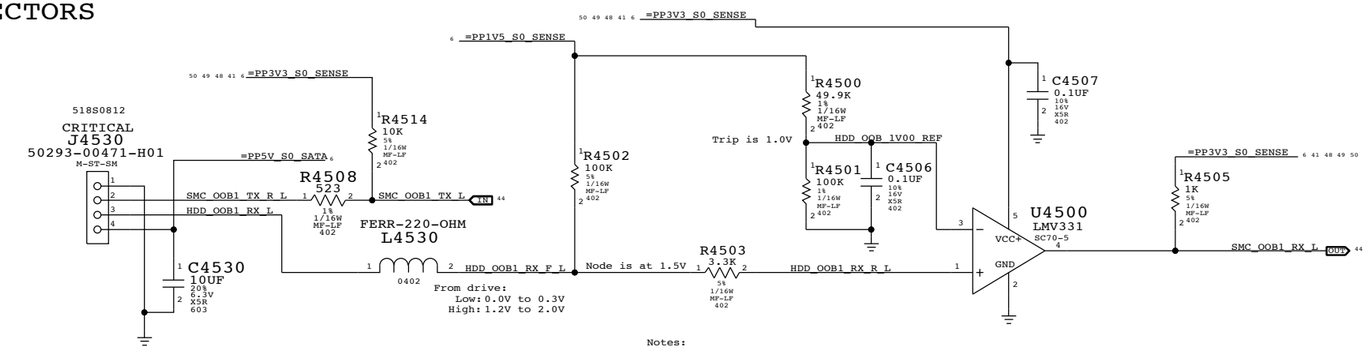
HDD CONNECTORS



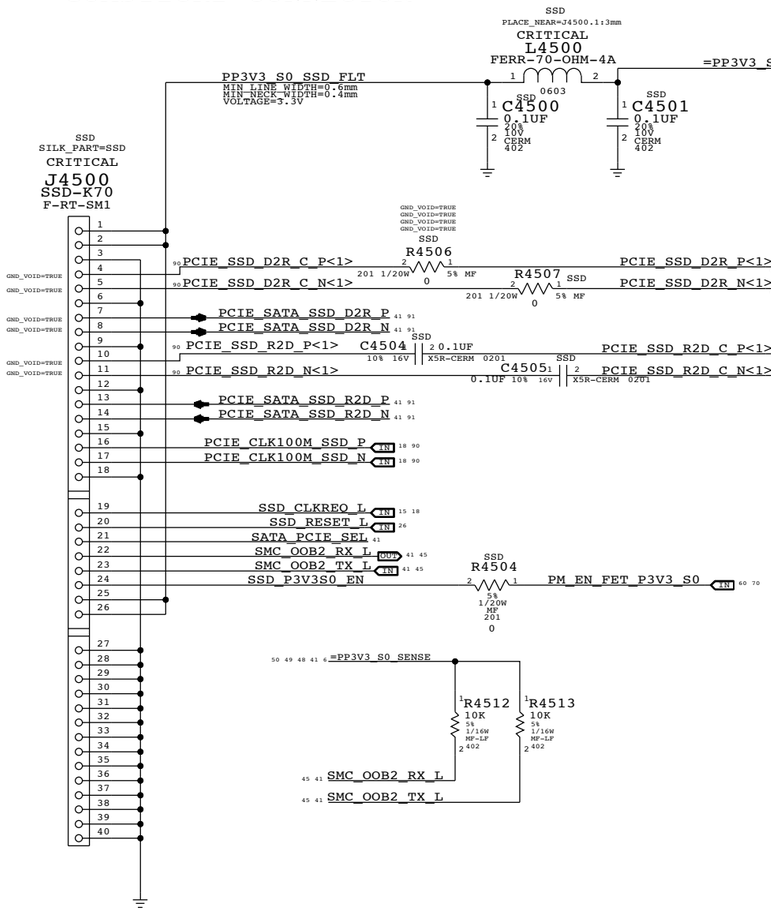
HDD Out-of-Band Temperature Sensing

Temperature read from SATA power connecter pin 11

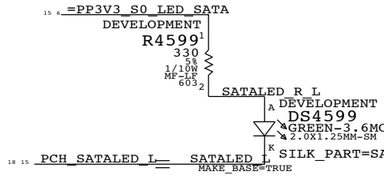


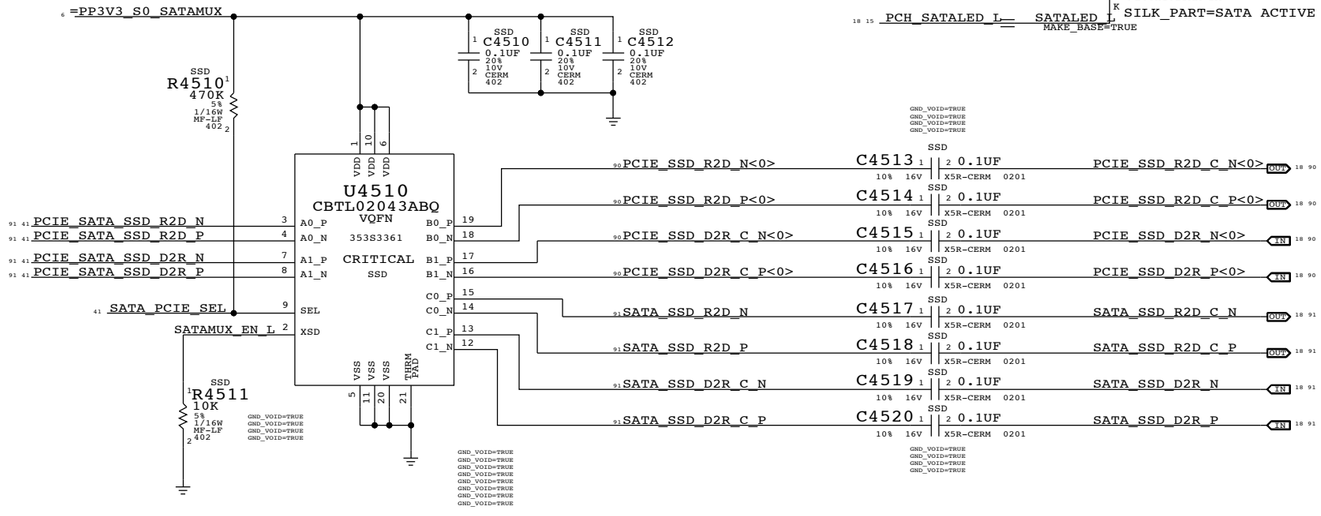
Notes:
Drive active: Valid signal protocol
Drive asleep: HDD drives HDD_OOB_TEMP low
Drive disconnected: Pulled high

GUMSTICK2 CONNECTOR



SATA Activity LED





SYNC_MASTER=D7_NICK SYNC_DATE=12/16/2011

PAGE TITLE

SATA Connectors

Apple Inc.

DRAWING NUMBER 051-9509 SIZE D

REVISION 4.2.0

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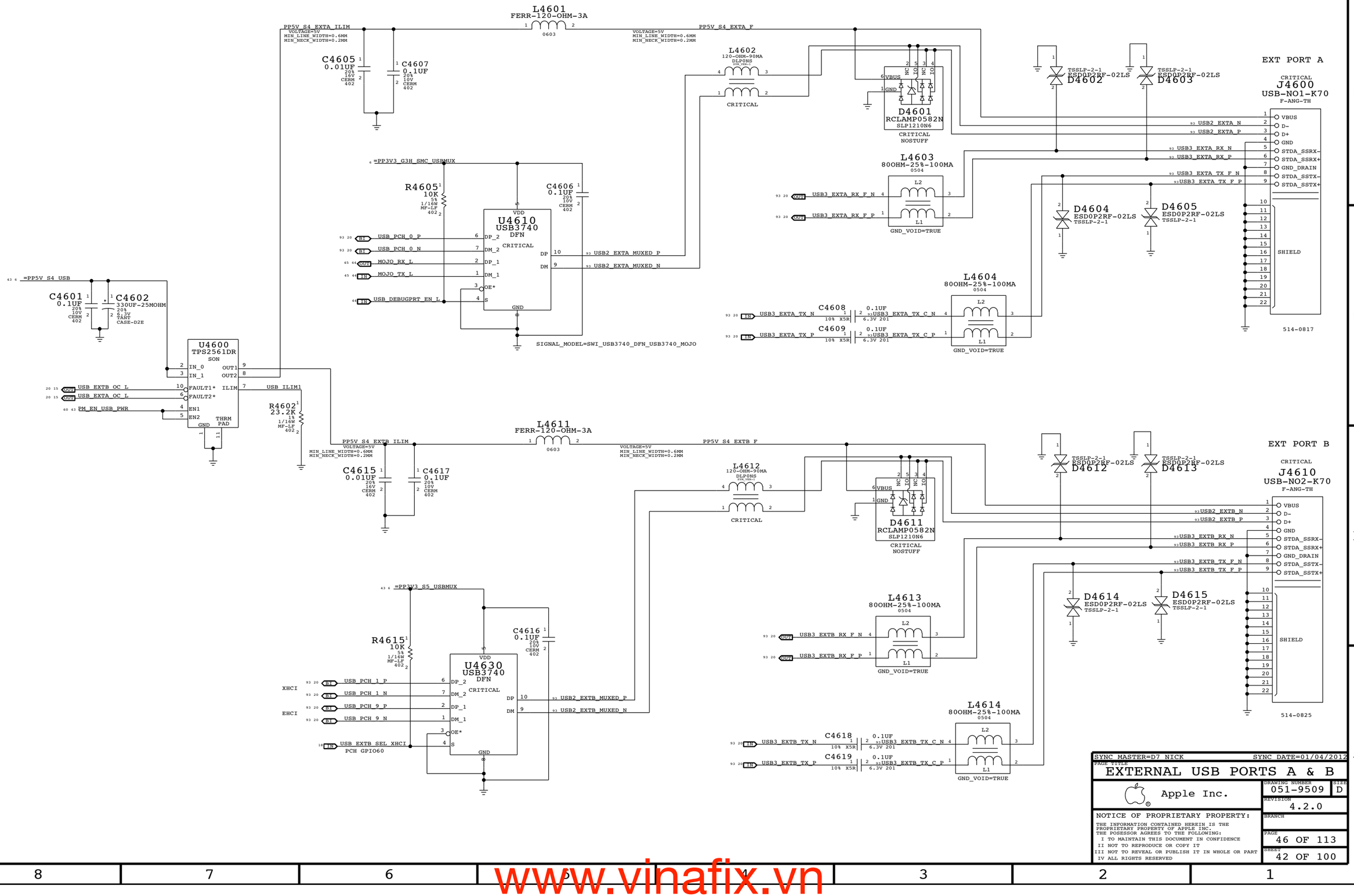
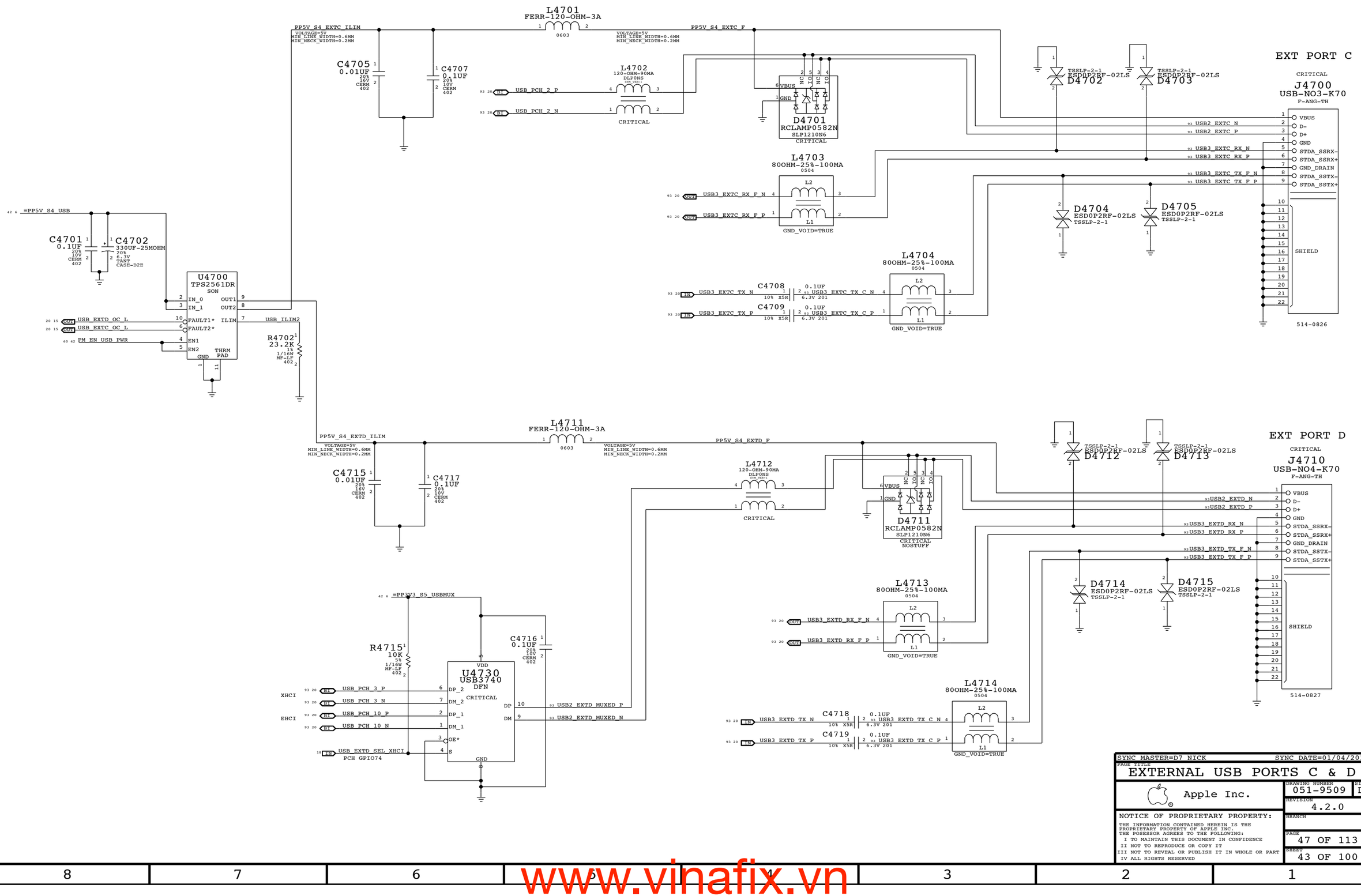
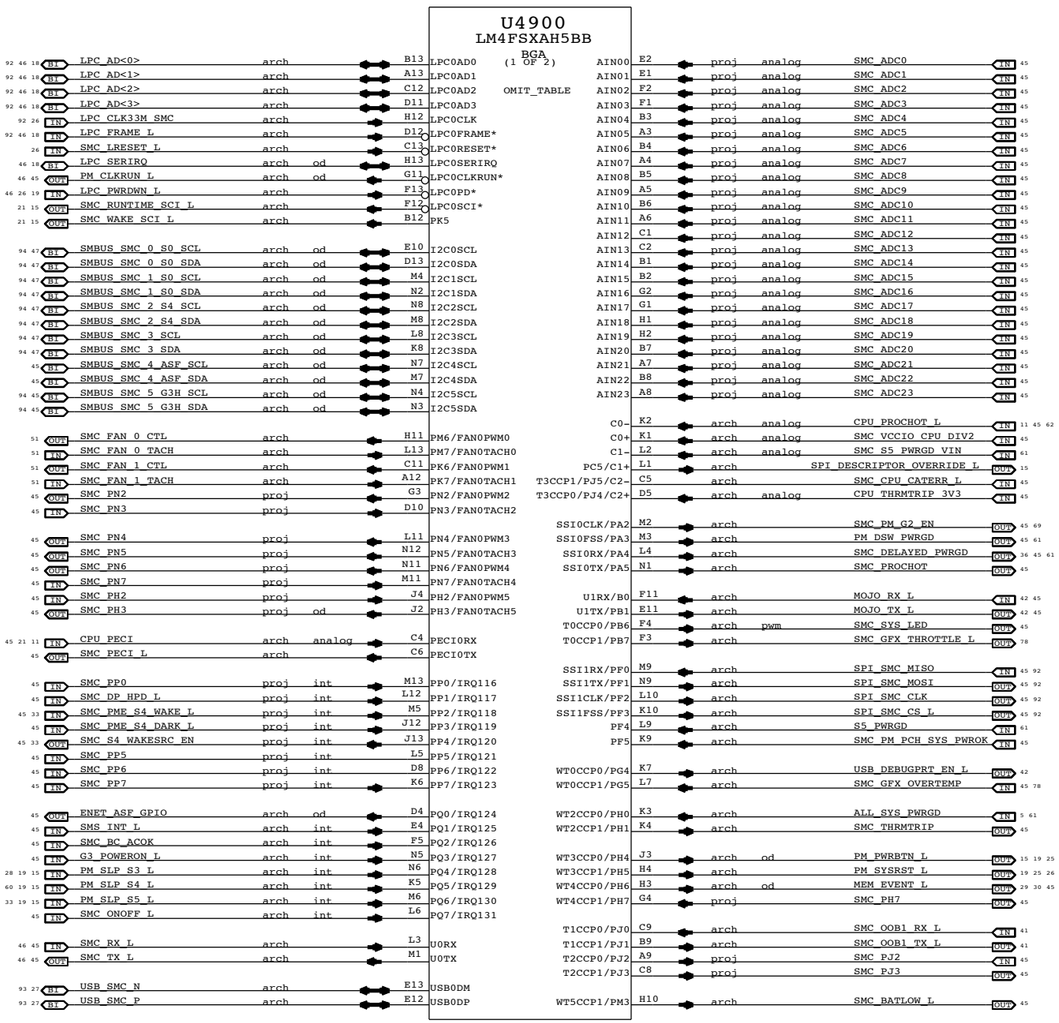
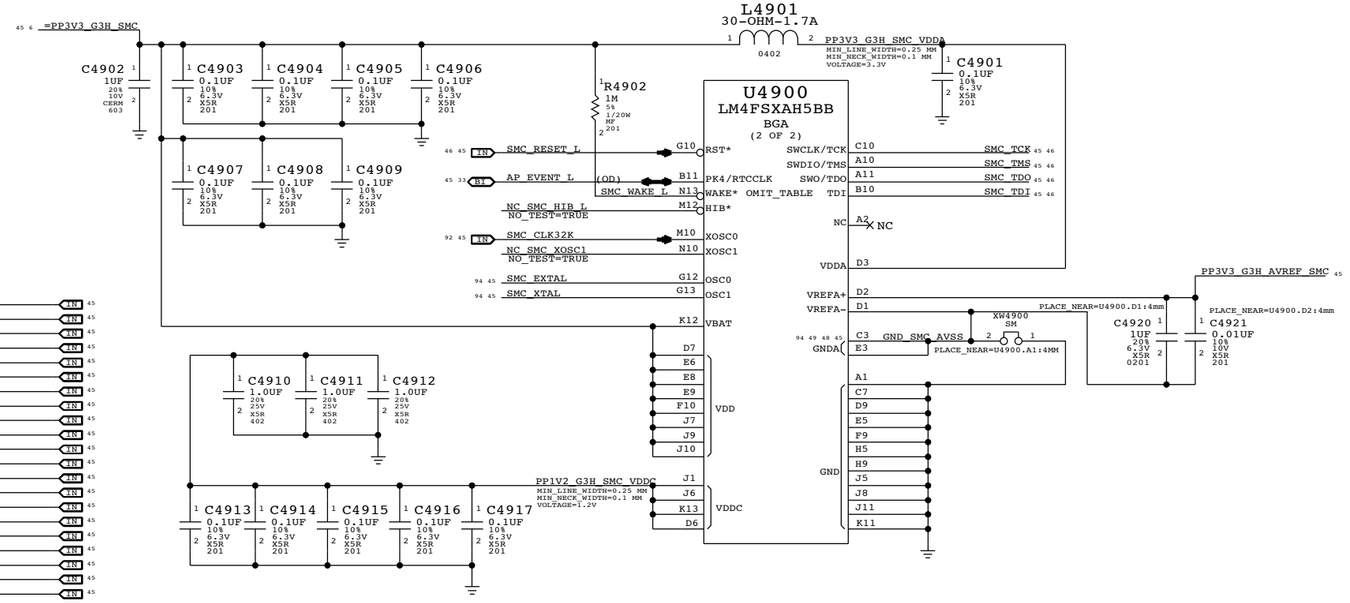




NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





SYNC_MASTER=D7_DOUG SYNC_DATE=01/11/2012

PAGE TITLE: SMC

Apple Inc.

DRAWING NUMBER: 051-9509 SIZE: D

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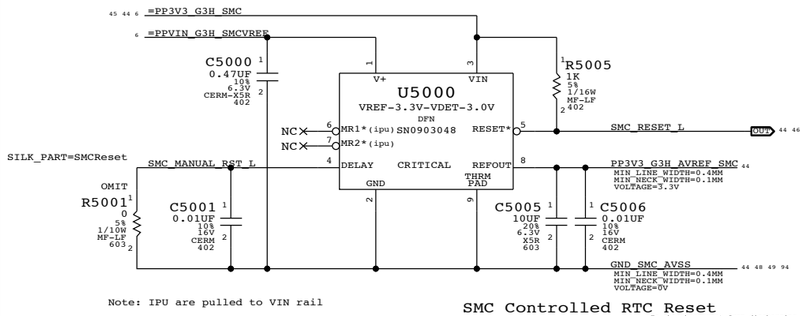
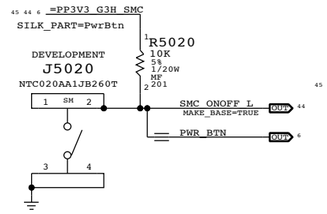
SMC Supervisor and AVREF Supply



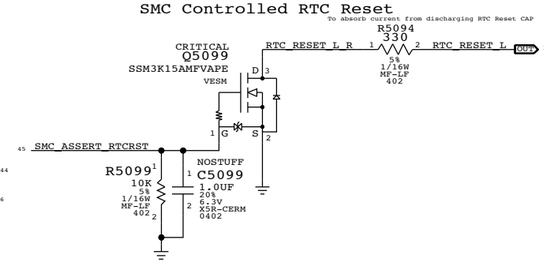
Note: IPU are pulled to VIN rail

Power Button



SMC Controlled RTC Reset

To absorb current from discharging RTC Reset CAP



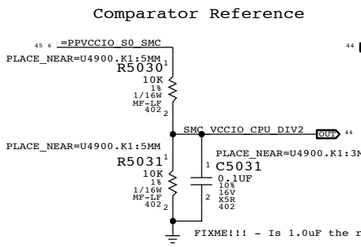
Enable TBT S4 Wake Sources

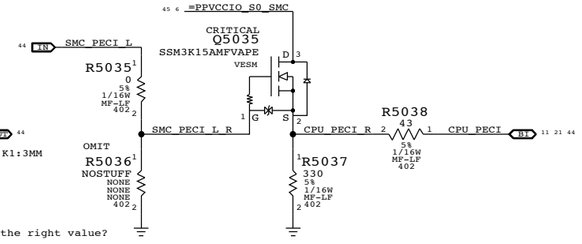
PECI Support

Level-shifter that allows SMC to drive PECI

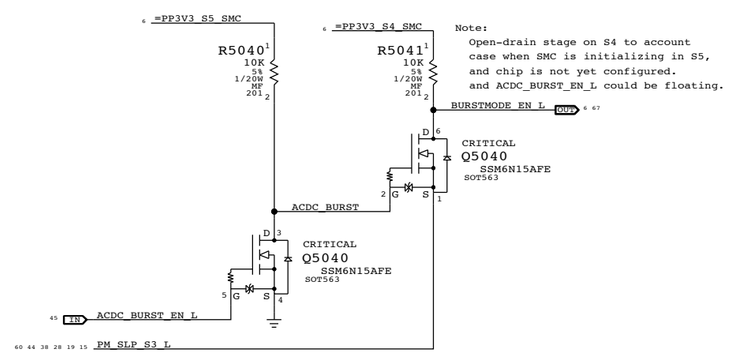
Place this circuit near the Tee point to minimize reflections

Comparator Reference





AC/DC Burst Mode Enable



ADC Channel Aliases

SMC_ADC0	VSNS_P12VG3H	SMC_ADC14	VSNS_HDDS0
SMC_ADC1	ISNS_P12VG3H	SMC_ADC15	ISNS_HDDS0
SMC_ADC2	VSNS_P12VS0_GPUCORE	SMC_ADC16	VSNS_SSDS0
SMC_ADC3	ISNS_P12VS0_GPUCORE	SMC_ADC17	ISNS_SSDS0
SMC_ADC6	VSNS_VDDQS3_DDR	SMC_ADC4	NC_SMC_ADC4
SMC_ADC7	ISNS_VDDQS3_DDR	SMC_ADC5	NC_SMC_ADC5
SMC_ADC8	VSNS_P12VS0_GPUUNCORE	SMC_ADC18	NC_SMC_ADC18
SMC_ADC9	ISNS_P12VS0_GPUUNCORE	SMC_ADC19	NC_SMC_ADC19
SMC_ADC10	VSNS_CPUCORE	SMC_ADC20	NC_SMC_ADC20
SMC_ADC11	ISNS_CPUCORE	SMC_ADC21	NC_SMC_ADC21
SMC_ADC12	VSNS_CPUAXG	SMC_ADC22	NC_SMC_ADC22
SMC_ADC13	ISNS_CPUAXG	SMC_ADC23	NC_SMC_ADC23

Project-specific Aliases

SMC_PH3	BDV_BKL_PWM
SMC_PN5	ACDC_BURST_EN_L
SMC_PJ3	SMC_OOB2_TX_L
SMC_PJ2	SMC_OOB2_RX_L
SMC_PP0	SMC_ACDC_ID
SMC_PH2	SMC_ASSERT_RTCRST

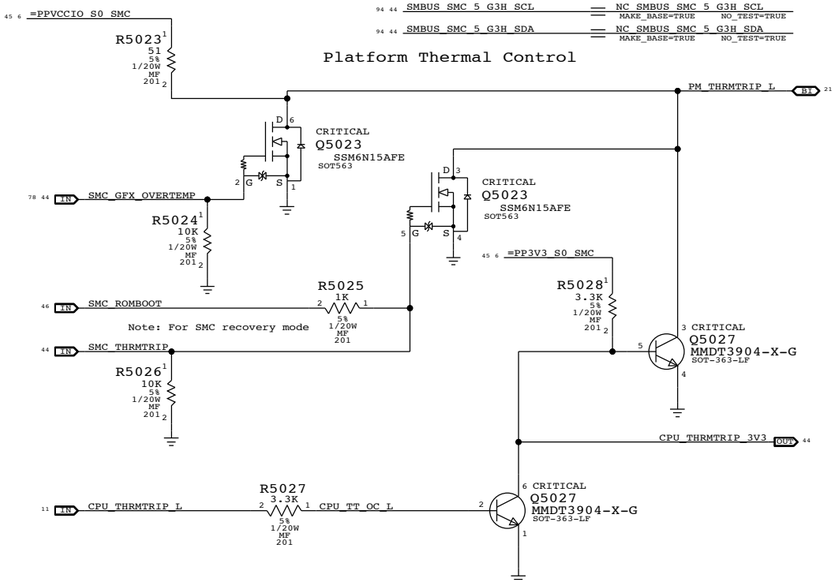
Unused ADC Channels

Unused Project-specific

SMC_PN2	NC_SMC_PN2
SMC_PN3	NC_SMC_PN3
SMC_PN4	NC_SMC_PN4
SMC_PN6	NC_SMC_PN6
SMC_PN7	NC_SMC_PN7
SMC_PP5	NC_SMC_PP5
SMC_PP6	NC_SMC_PP6
SMC_PP7	NC_SMC_PP7
SMC_DP_HPD_L	NC_SMC_DP_HPD_L
SMC_PME_S4_DARK_L	NC_SMC_PME_S4_DARK_L
SMC_PH7	TP_SMC_PH7
SMBUS_SMC_4_ASF_SCL	NC_SMBUS_SMC_4_ASF_SCL
SMBUS_SMC_4_ASF_SDA	NC_SMBUS_SMC_4_ASF_SDA
SMBUS_SMC_5_G3H_SCL	NC_SMBUS_SMC_5_G3H_SCL
SMBUS_SMC_5_G3H_SDA	NC_SMBUS_SMC_5_G3H_SDA

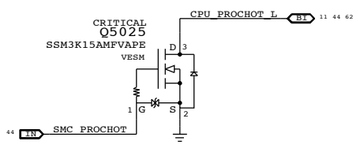
TP for access if ZPB re-intstated

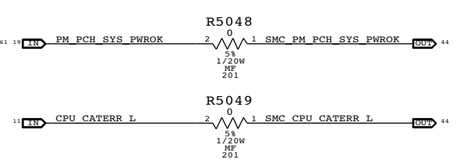
Platform Thermal Control



PROCHOT Support

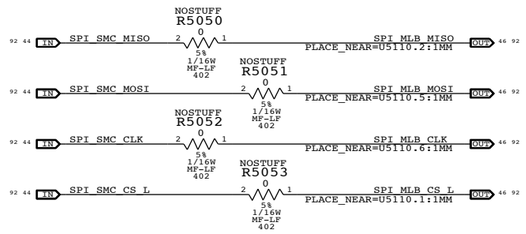
Level-shifter that allows SMC to drive PROCHOT





SMC SPI Support

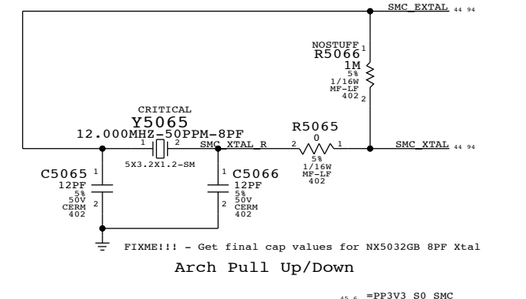
Series R are NOSTUFF until topology of 2 SPI masters is verified



SMC 32KHz Clock

SMC Crystal

NOTE: SMC team wants 12MHz for this Xtal



FIXME!!! - Get final cap values for NX5032GB 8PF Xtal

Arch Pull Up/Down

MEM_EVENT_L	R5070	10K	=PP3V3_S0_SMC	
PM_CLKRUN_L	R5071	10K	=PP3V3_S0_SMC	
ENET_ASF_GPIO	R5075	10K	=PP3V3_G3H_SMC	
G3_POWERON_L	R5076	10K	=PP3V3_G3H_SMC	
SMC_BATLOW_L	R5077	100K	=PP3V3_G3H_SMC	
SMC_BC_ACOK	R5078	100K	=PP3V3_G3H_SMC	
SMC_SYS_LED	R5079	100K	=PP3V3_G3H_SMC	
SMS_INT_L	R5080	10K	=PP3V3_G3H_SMC	
SMC_PME_S4_WAKE_L	R5081	10K	=PP3V3_G3H_SMC	
AP_EVENT_L	R5085	10K	PP3V3_S4_AP_FET	
SMC_S4_WAKESRC_EN	R5017	100K	=PP3V3_G3H_SMC	
SMC_DELAYED_PWRGD	R5086	100K	=PP3V3_G3H_SMC	
PM_DSW_PWRGD	R5084	100K	=PP3V3_G3H_SMC	
SMC_PM_G2_EN	R5087	100K	=PP3V3_G3H_SMC	

Note:
Pull-down needed for SMC SSI signals

Serial/JTAG Interface Pull-ups

SMC_TX_L	R5090	10K	=PP3V3_G3H_SMC
SMC_RX_L	R5091	100K	=PP3V3_G3H_SMC
MOJO_TX_L	R5092	10K	=PP3V3_G3H_SMC
MOJO_RX_L	R5093	100K	=PP3V3_G3H_SMC
SMC_TCK	R5095	10K	=PP3V3_G3H_SMC
SMC_TDI	R5096	10K	=PP3V3_G3H_SMC
SMC_TDO	R5097	10K	=PP3V3_G3H_SMC
SMC_TMS	R5098	10K	=PP3V3_G3H_SMC

SYNC_MASTER=D7_DOUG SYNC_DATE=01/11/2012

PAGE TITLE: SMC Support

Apple Inc.

DRAWING NUMBER: 051-9509 SIZE: D

REVISION: 4.2.0

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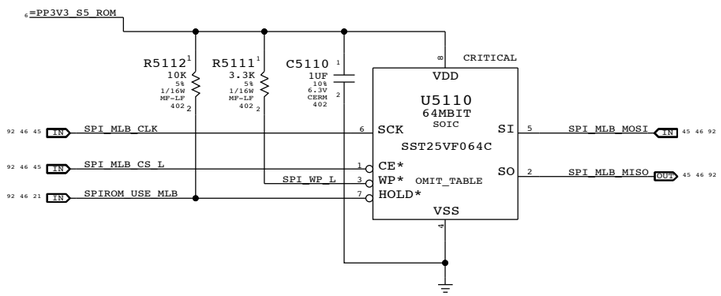
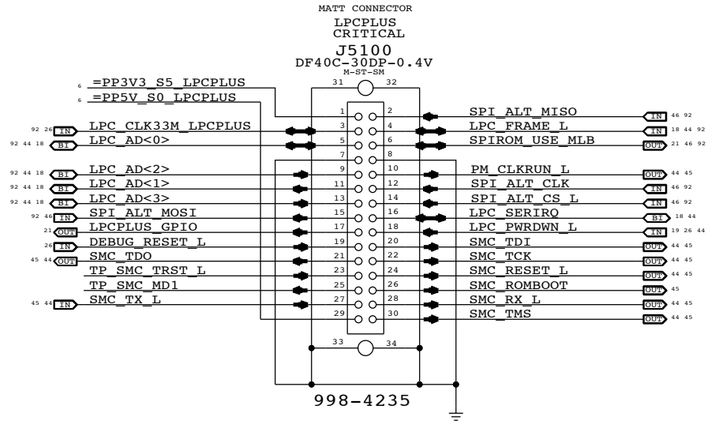
SHEET: 45 OF 100

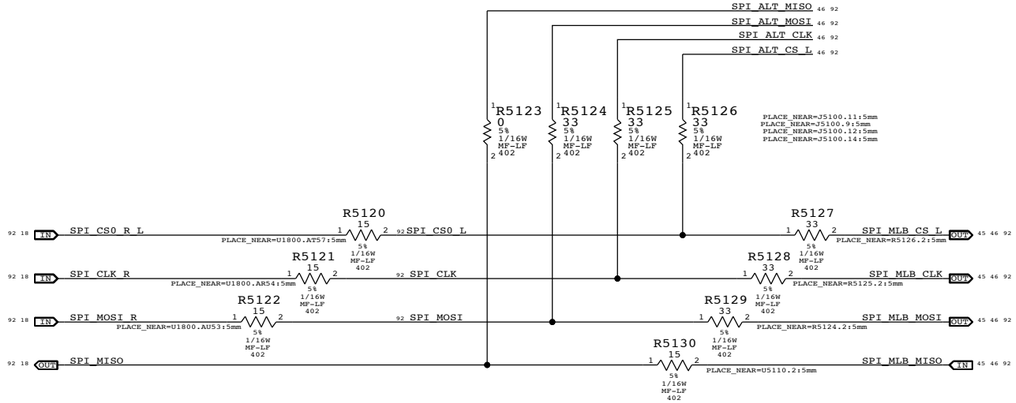
SPI BootROM



LPC+SPI Connector



SPI Series Termination



SYNC_MASTER=D7_NICK SYNC_DATE=12/13/2011

PAGE TITLE
SPI and Debug Connector

Apple Inc.

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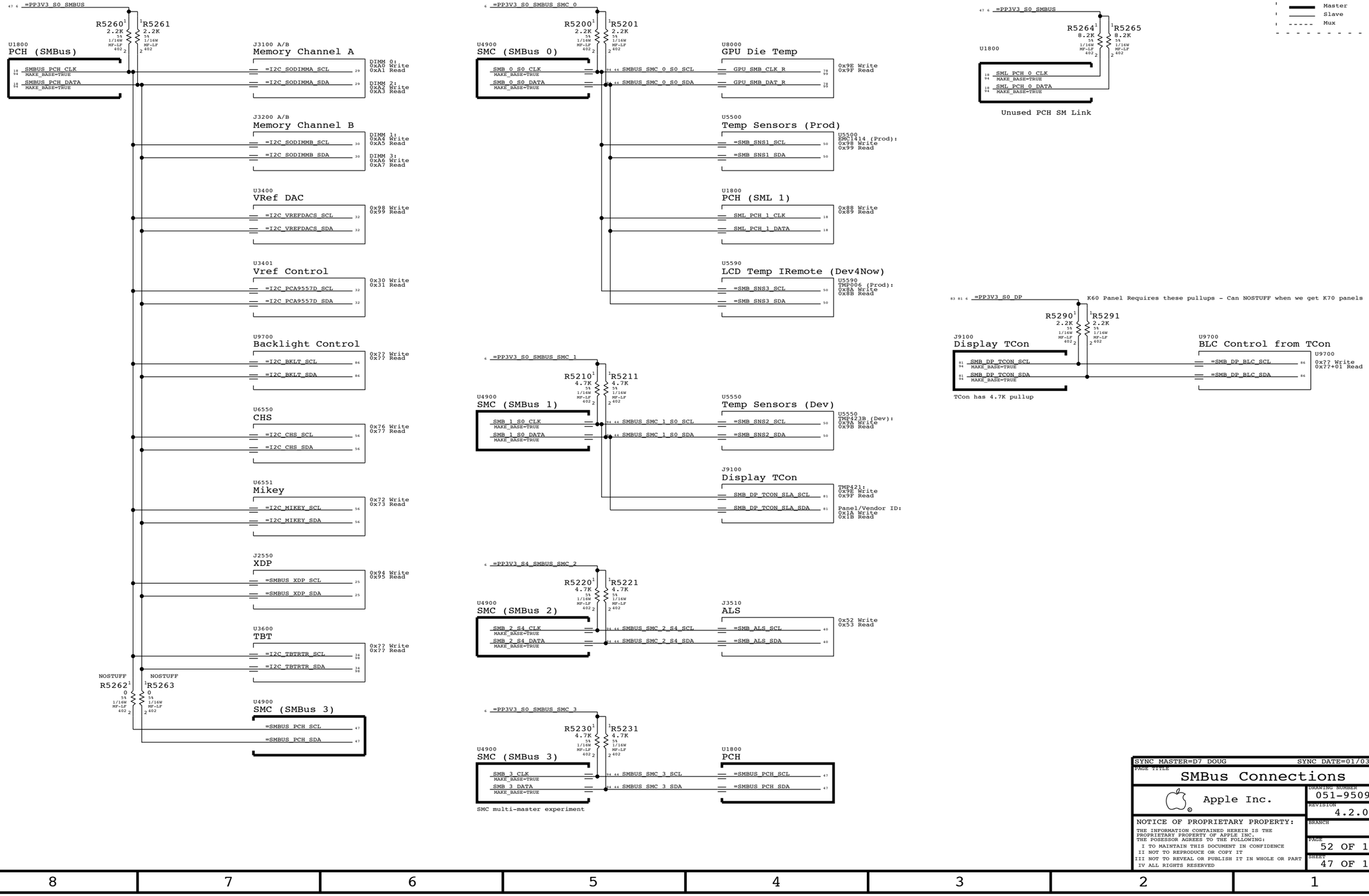
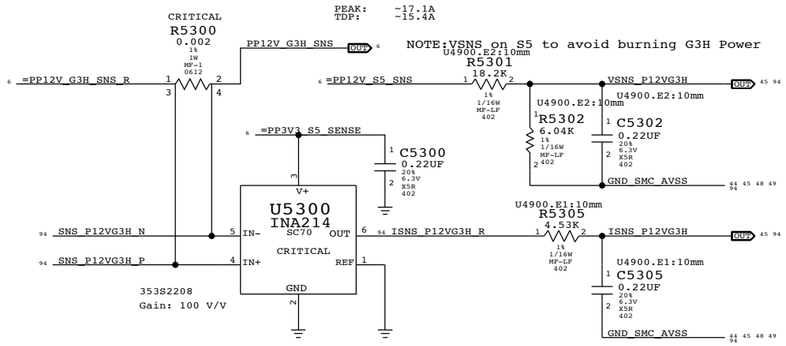
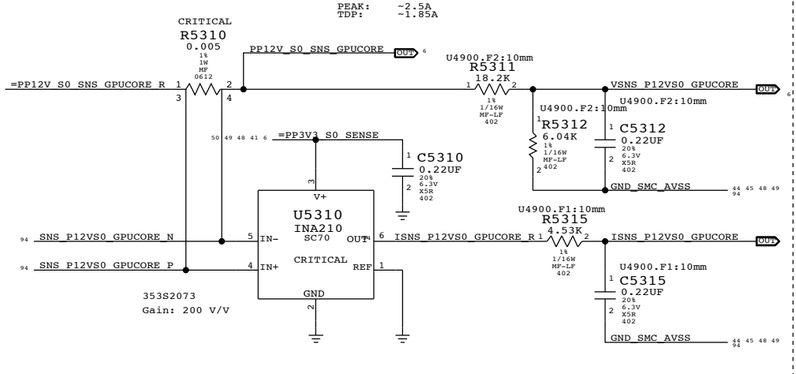


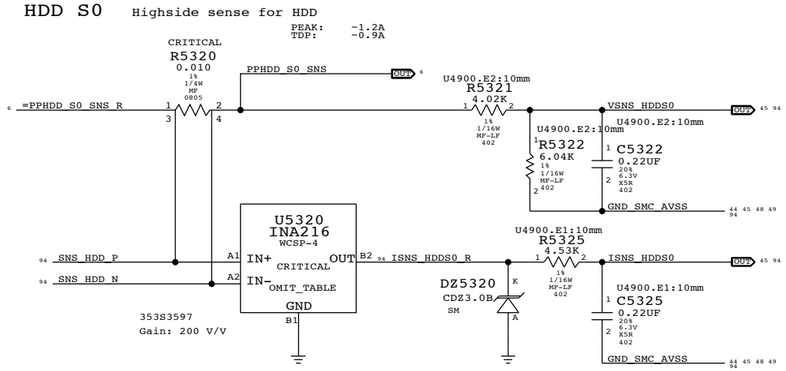
12V G3H AC/DC lowside sense (System total)



12V S0 GPU highside sense for GPU Core Regulator

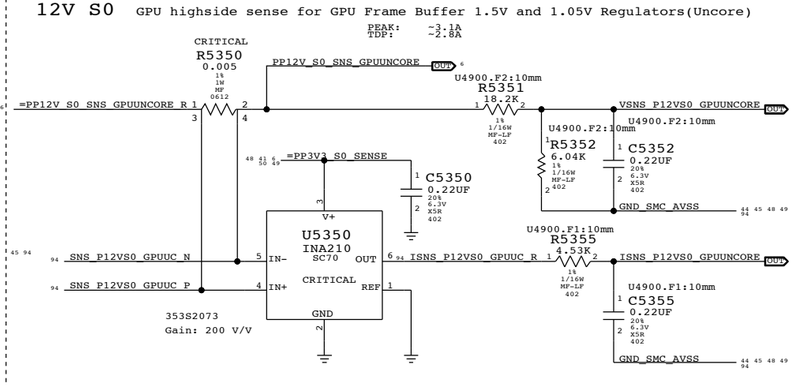


HDD S0 Highside sense for HDD

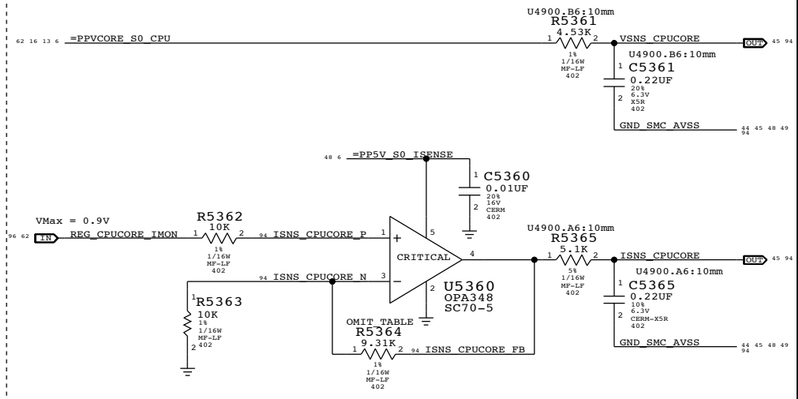


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S3597	1	INA216A4 200V/V Current Sense	U5320	

12V S0 GPU highside sense for GPU Frame Buffer 1.5V and 1.05V Regulators(Uncore)

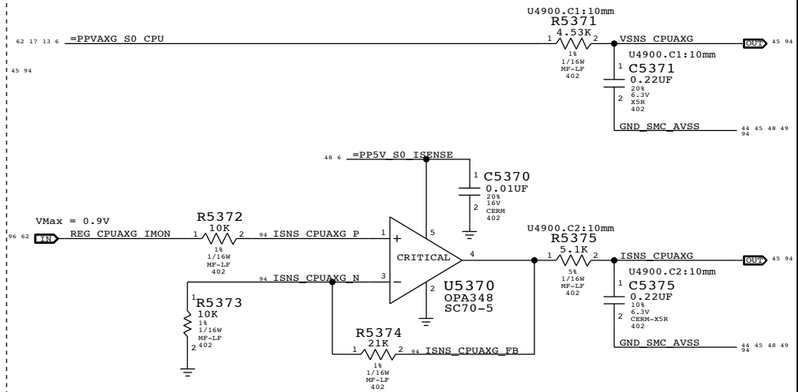


CPU Core Voltage sense and IMON amp (VC0C, IC0C)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0312	1	RES,MTL FILM,1/16W,9.31K,0402	R5364	SNS_CPUCORE:3PHASE
114S0345	1	RES,MTL FILM,1/16W,21K,0402	R5364	SNS_CPUCORE:4PHASE

CPU AXG Voltage sense and IMON amp (VC0G, IC0G)



SYNC_MASTER=D7_DOUG SYNC_DATE=01/06/2012

PAGE TITLE: I and V Sense(Production)

Apple Inc.

DRAWING NUMBER: 051-9509 SIZE: D

REVISION: 4.2.0

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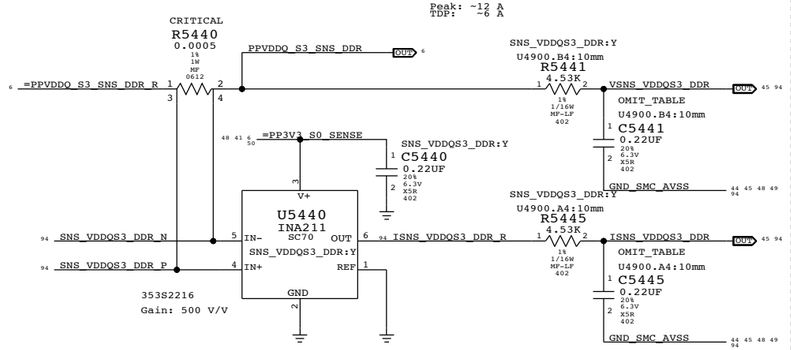
VDDQ S3

VDDQ lowside sense for SO-DIMM modules

Peak: -12 A
TDP: -6 A

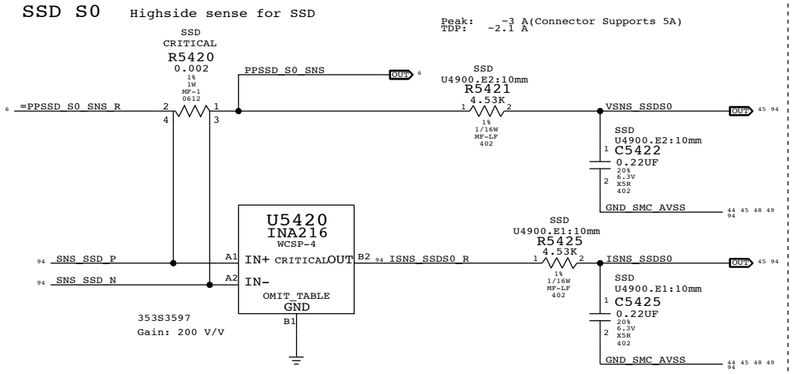


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0080	2	CAP,0.22UF,402	C5441,C5445	SNS_VDDQS3_DDR:Y
116S0004	2	RES,0 OHM,402	C5441,C5445	SNS_VDDQS3_DDR:N

SSD S0

Highside sense for SSD

Peak: ~3 A(Connector Supports 5A)
TDP: ~2.1 A



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S3597	1	INA216A4 200V/V Current Sense	U5420	SSD

SYNC_MASTER=K70_MLB SYNC_DATE=11/30/2011

PAGE TITLE
I and V Sense(Development)

Apple Inc.

DRAWING NUMBER 051-9509 SIZE D
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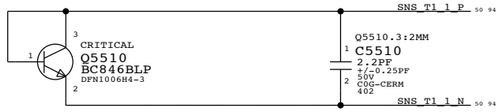
Temperature Sensor T1: Production Bound

GPU Proximity

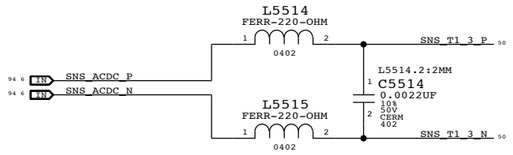


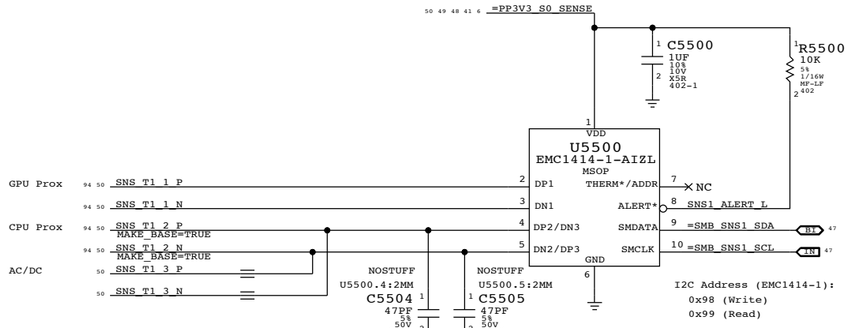
PLACEMENT_NOTE=Place Q5510 near GPU and GDDR5

CPU Proximity

PLACEMENT_NOTE=Place Q5512 in CPU socket cavity

AC/DC Diode on supply

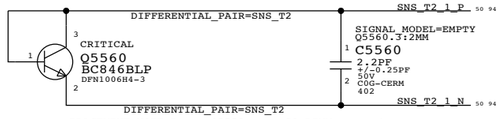




PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
372S0186	372S0185		ALL	Alternate Temp Diode

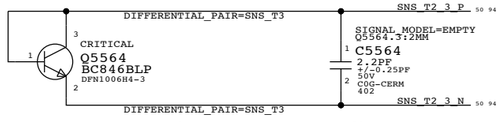
Temperature Sensor T2: Development Only

SO-DIMM Proximity



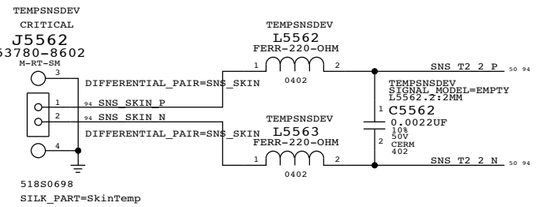
PLACEMENT_NOTE=Place Q5550 near SO-DIMM connectors

BLC Proximity

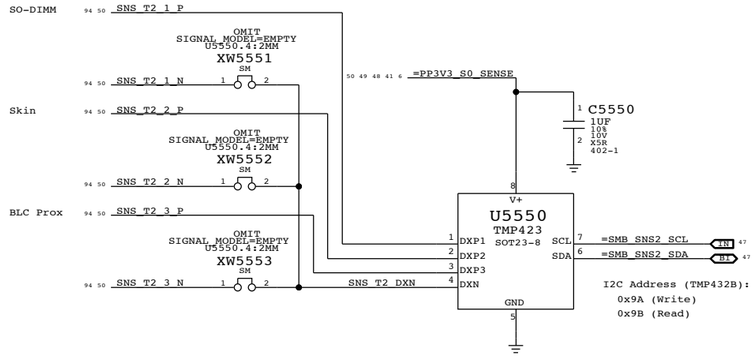


PLACEMENT_NOTE=Place Q5554 near BLC controller

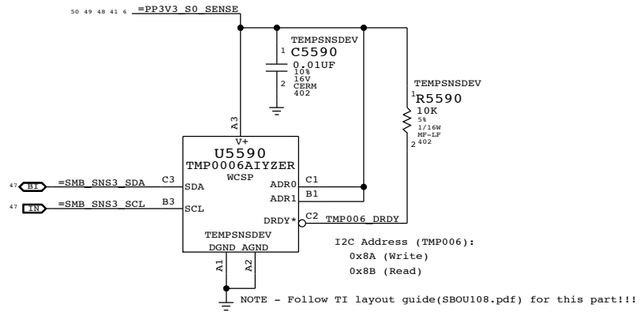
Skin



SILK_PART=SkinTemp



Temperature Sensor T3: LCD Remote Sensor(Dev4Now)



NOTE - Follow TI layout guide(SBOU108.pdf) for this part!!!

SYNC_MASTER=D7_DOUG SYNC_DATE=12/13/2011

PAGE TITLE
Temperature Sensors

Apple Inc.

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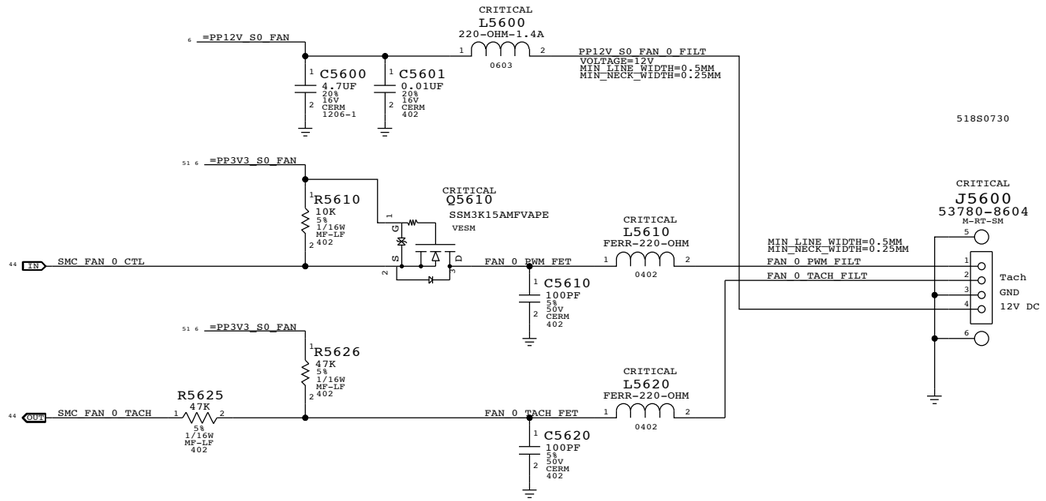
SMC Fan 0 (System)

Note:
The circuit for the PWM input to the fan acts as a non-inverting level-shifter to protect the SMC. It is assumed there is a pull-up to 5V/12V inside the fan, otherwise when the SMC PWM goes low and Q5610 turns on, there would be 5V/12V present on the SMC pin! Then by definition, the drain of Q5610 is at common and the SMC sinks current when Q5610 is on.

This resembles an open-drain if there is a pull-up, going to a Hi-Z FET input.

Otherwise, this is simply a pass-FET.



SMC Fan 1 (Unused)

SYNC_MASTER=K70_MLB SYNC_DATE=11/30/2011

PAGE TITLE
System Fan

Apple Inc.

DRAWING NUMBER 051-9509
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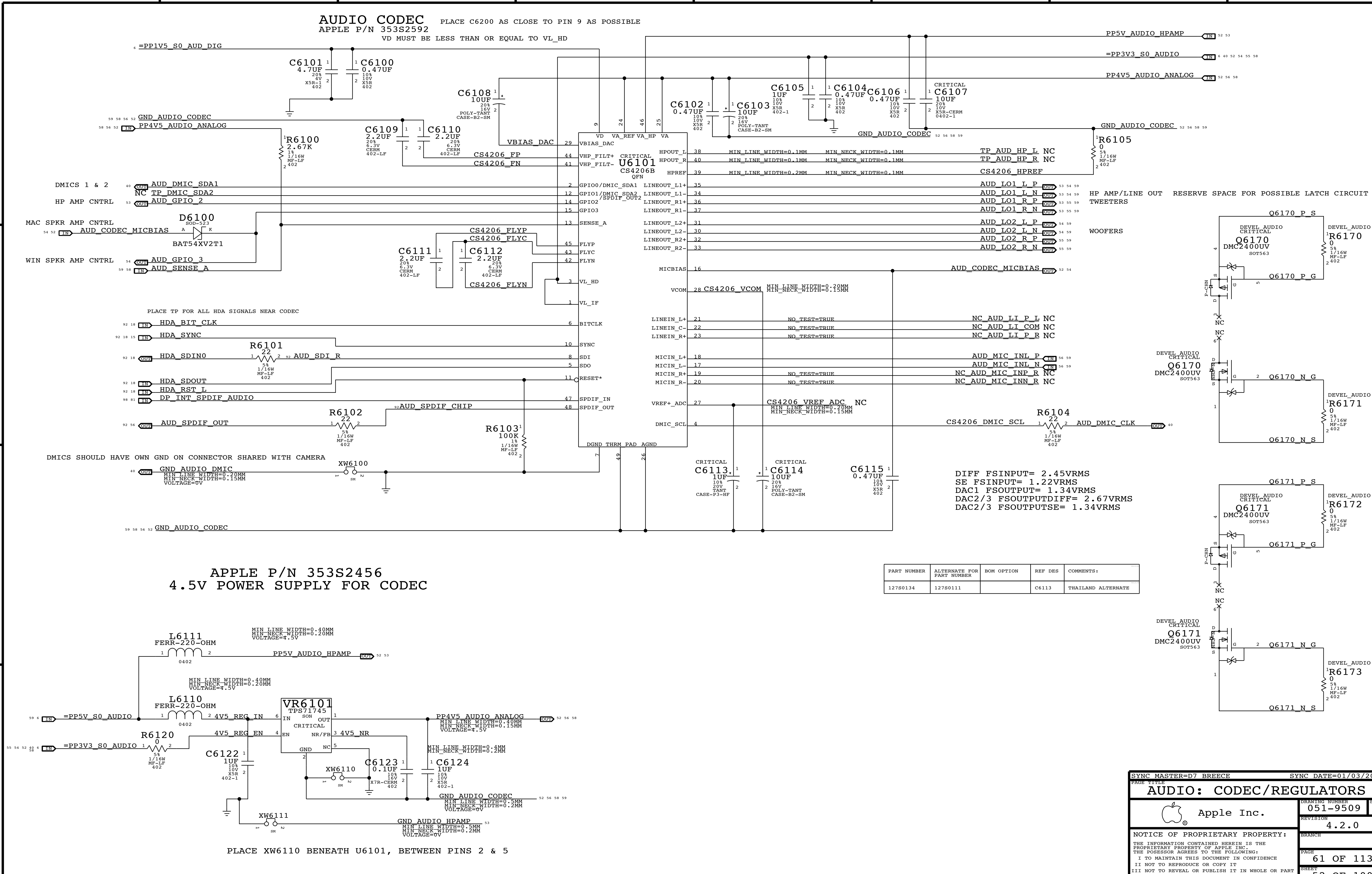


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
127S0134	127S0111		C6113	THAILAND ALTERNATE

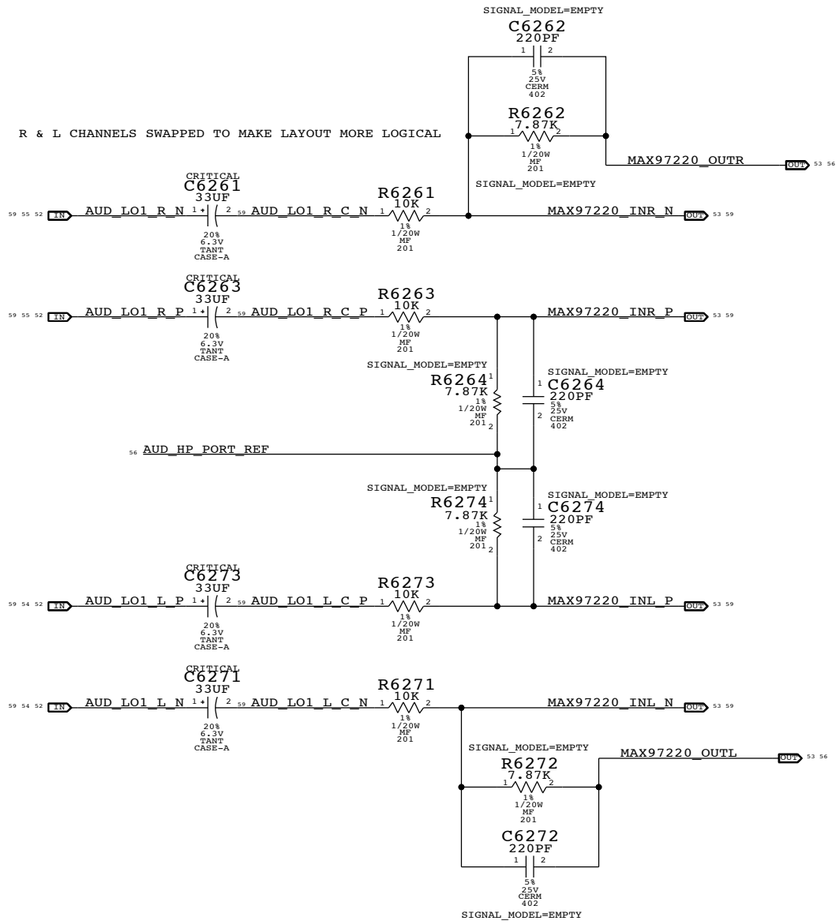
SYNC_MASTER=D7_BREECE SYNC_DATE=01/03/2012

AUDIO: CODEC/REGULATORS

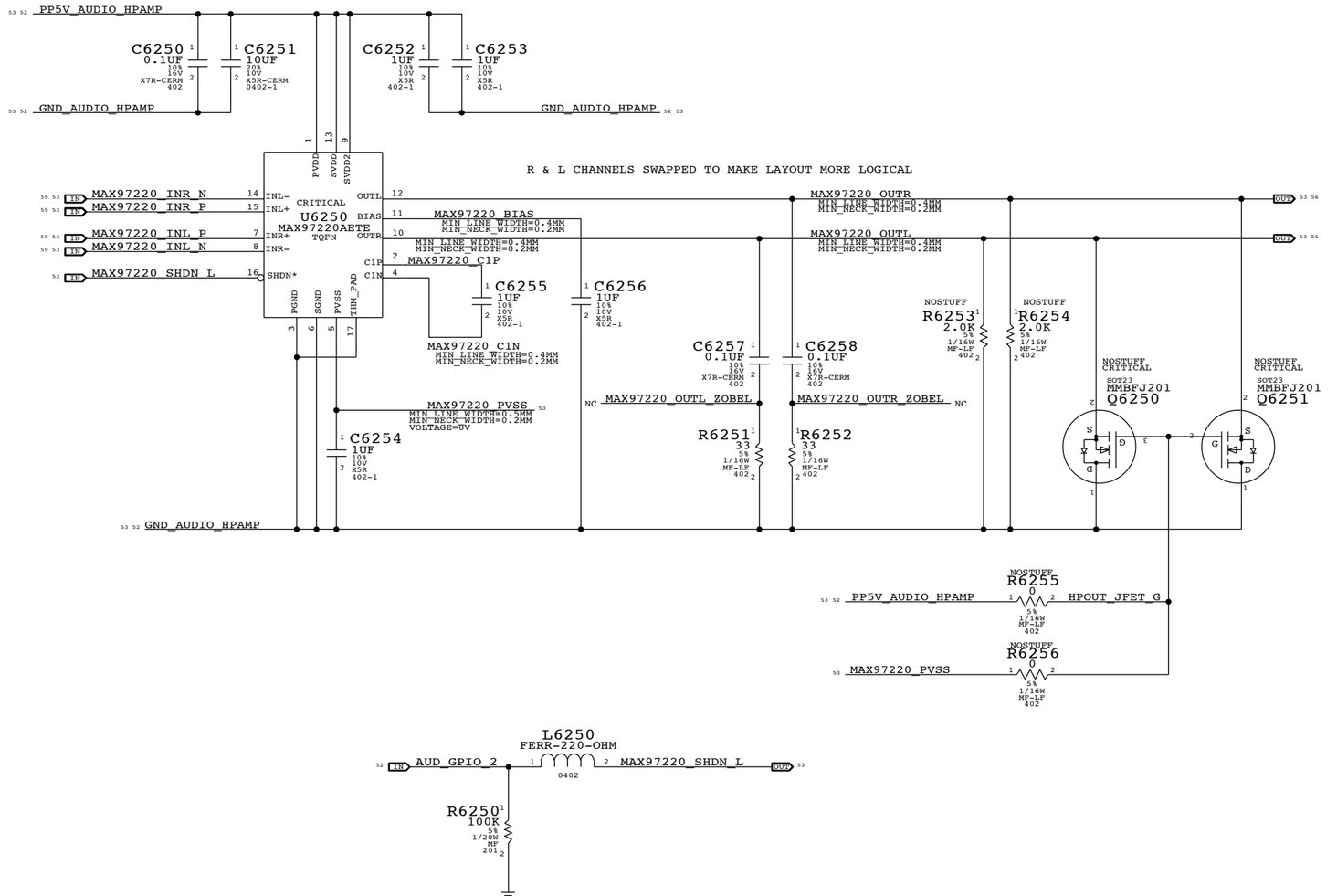
Apple Inc.

DRAWING NUMBER 051-9509 SIZE D

REVISION 4.2.0



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
127S0135	127S0120		C6261	THAILAND ALTERNATE
127S0135	127S0120		C6263	THAILAND ALTERNATE
127S0135	127S0120		C6271	THAILAND ALTERNATE
127S0135	127S0120		C6273	THAILAND ALTERNATE



SYNC MASTER=D7 BREECE SYNC DATE=01/03/2012

PAGE TITLE

AUDIO: HEADPHONE AMP

Apple Inc.

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LEFT CH SPEAKER AMP
APPLE P/N 353S3163

SPEAKER AMP GAIN = +9 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~18 HZ (0.22 UF)

=PP12V_S0_AUDIO_SPKRAMP

C6300 10UF 10% 25V X5R 805
C6301 10UF 10% 25V X5R 805
C6302 0.1UF 10% 25V X5R 402
C6303 1UF 20% 25V X5R 603-1
C6304 0.1UF 10% 25V X5R 402
C6305 1UF 10% 25V X5R 603-1
CRITICAL C6306 470UF 20% 16V POLY SM

INPUT POLARITY FLIP OK -- TRUE DIFF INPUTS

L6303 FERR-1000-OHM 0402 — AUD_LO1_L_N — AUD_LAMP_RINC_P — C6308 4700PF 5% 50V NPO-C0G 805 — AUD_LAMP_RIN_P
L6302 FERR-1000-OHM 0402 — AUD_LO1_L_P — AUD_LAMP_RINC_N — C6309 4700PF 5% 50V NPO-C0G 805 — AUD_LAMP_RIN_N
L6300 FERR-1000-OHM 0402 — AUD_LO2_L_N — AUD_LAMP_LINC_P — C6310 0.22UF 10% 16V CERM 402 — AUD_LAMP_LIN_P
L6301 FERR-1000-OHM 0402 — AUD_LO2_L_P — AUD_LAMP_LINC_N — C6311 0.22UF 10% 16V CERM 402 — AUD_LAMP_LIN_N

INPUT POLARITY FLIP OK -- TRUE DIFF INPUTS

=PP3V3_S0_AUDIO

CRITICAL U6300 SSM3302 LFCSP

PVDD (34, 35, 36, 37)

INR+ 20
INR- 19
STDNR* 22 — AUD_SPKRAMP_MAC_SHDN_L — WOOFERS & TWEETERS ON UNDER MAC OS
MONO 16 — AUD_LAMP_MONO
STDNL* 9 — AUD_SPKRAMP_WIN_SHDN_L — ONLY WOOFERS ON UNDER WINDOWS
INL+ 11
INL- 12
GAIN 21 — AUD_LAMP_GAIN
VREG/AVDD 8 — AUD_LAMP_AVDD (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM, VOLTAGE=5V)
REGEN 23

C6317 2.2UF 20% 10V X5R-CERM 402

AGND (7, 24) THERM_PAD (41) PGND (31, 32, 33, 38, 39, 40)

THERM 17 — TP_AUD_LAMP_THERM — NC
BOOTR+ 30 — AUD_LAMP_BOOTRP (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM) — C6313 0.22UF 20% 25V X5R 603
OUTR+ 28, 29 — AUD_LAMP_OUTRP (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM) — OUTP
OUTR- 26, 27 — AUD_LAMP_OUTRN — OUTP
BOOTR- 25 — AUD_LAMP_BOOTRN (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM) — C6314 0.22UF 20% 25V X5R 603
EDGE 10 — AUD_LAMP_EDGE
BOOTL+ 1 — AUD_LAMP_BOOTLP (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM) — C6315 0.22UF 20% 25V X5R 603
OUTL+ 2, 3 — AUD_LAMP_OUTPL (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM) — OUTP
OUTL- 4, 5 — AUD_LAMP_OUTNL — OUTP
BOOTL- 6 — AUD_LAMP_BOOTLN (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM) — C6316 0.22UF 20% 25V X5R 603
NC 18, 13, 14, 15

PINS 14 & 15 ARE TEST PINS AND SHOULD BE TIED TO GND

OUTPUT POLARITY FLIP TO MAKE LAYOUT MORE LOGICAL

SIGNAL_MODEL=EMPTY
CRITICAL L6305 110-OHM-3A DLY5ATN111SQ2 — AUD_SPKR_LTWT_OUT_P / AUD_SPKR_LTWT_OUT_N — CRITICAL C6323 1000PF 5% 25V NPO-C0G 402
CRITICAL L6307 110-OHM-3A DLY5ATN111SQ2 — AUD_SPKR_LWFR_OUT_N / AUD_SPKR_LWFR_OUT_P — CRITICAL C6324 1000PF 5% 25V NPO-C0G 402

OUTPUT POLARITY FLIP TO MAKE LAYOUT MORE LOGICAL

CRITICAL C6320 1000PF 5% 25V NPO-C0G 402
CRITICAL C6322 1000PF 5% 25V NPO-C0G 402
CRITICAL C6319 1000PF 5% 25V NPO-C0G 402
CRITICAL C6321 1000PF 5% 25V NPO-C0G 402
SIGNAL_MODEL=EMPTY

L6308 FERR-1000-OHM 0402 — AUD_CODEC_MICBIAS — AUD_SPKRAMP_MAC_SHDN_L
R6301 100K 5% 1/16W MF-LF 402 — NOSTUFF C6312 100PF 5% 50V CERM 402

R6308 0 5% 1/16W MF-LF 402 — AUD_GPIO_3 — AUD_SPKRAMP_WIN_SHDN_L
R6309 100K 5% 1/16W MF-LF 402 — NOSTUFF C6318 100PF 5% 50V CERM 402

EDGE RATE CONTROL

	R6304	R6305
ON	0 OHM	NOSTUFF
OFF	NOSTUFF	0 OHM

AUD_RAMP_MONO NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

GAIN	R6306	R6307
+9 DB	NOSTUFF	0 OHM
+12 DB	NOSTUFF	NOSTUFF
+15 DB	0 OHM	NOSTUFF
+18 DB	NOSTUFF	47 KOHM
+24 DB	47 KOHM	NOSTUFF

AUD_LAMP_AVDD
R6304 0 5% 1/16W MF-LF 402 — AUD_LAMP_EDGE
R6305 NOSTUFF 0 5% 1/16W MF-LF 402
R6303 0 5% 1/16W MF-LF 402 — AUD_LAMP_MONO
R6306 NOSTUFF 0 5% 1/16W MF-LF 402 — AUD_LAMP_GAIN
R6307 0 5% 1/16W MF-LF 402

SYNC_MASTER=D7_BREECE SYNC_DATE=01/03/2012
PAGE TITLE: AUDIO: LEFT SPKR AMP

Apple Inc.

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REVISION 4.2.0
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RIGHT CH SPEAKER AMP
APPLE P/N 353S3163

SPEAKER AMP GAIN = +9 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~18 HZ (0.22 UF)

INPUT POLARITY FLIP OK -- TRUE DIFF INPUTS

OUTPUT POLARITY FLIP TO MAKE LAYOUT MORE LOGICAL

ONLY WOOFERS ON UNDER WINDOWS

WOOFERS & TWEETERS ON UNDER MAC OS

PINS 14 & 15 ARE TEST PINS AND SHOULD BE TIED TO GND

EDGE RATE CONTROL	R6404	R6405
ON	0 OHM	NOSTUFF
OFF	NOSTUFF	0 OHM

AUD_RAMP_MONO NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

GAIN	R6406	R6407
+9 DB	NOSTUFF	0 OHM
+12 DB	NOSTUFF	NOSTUFF
+15 DB	0 OHM	NOSTUFF
+18 DB	NOSTUFF	47 KOHM
+24 DB	47 KOHM	NOSTUFF

SYNC MASTER=D7 BREECE SYNC DATE=01/03/2012
PAGE TITLE: AUDIO: RIGHT SPKR AMP
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MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S2640

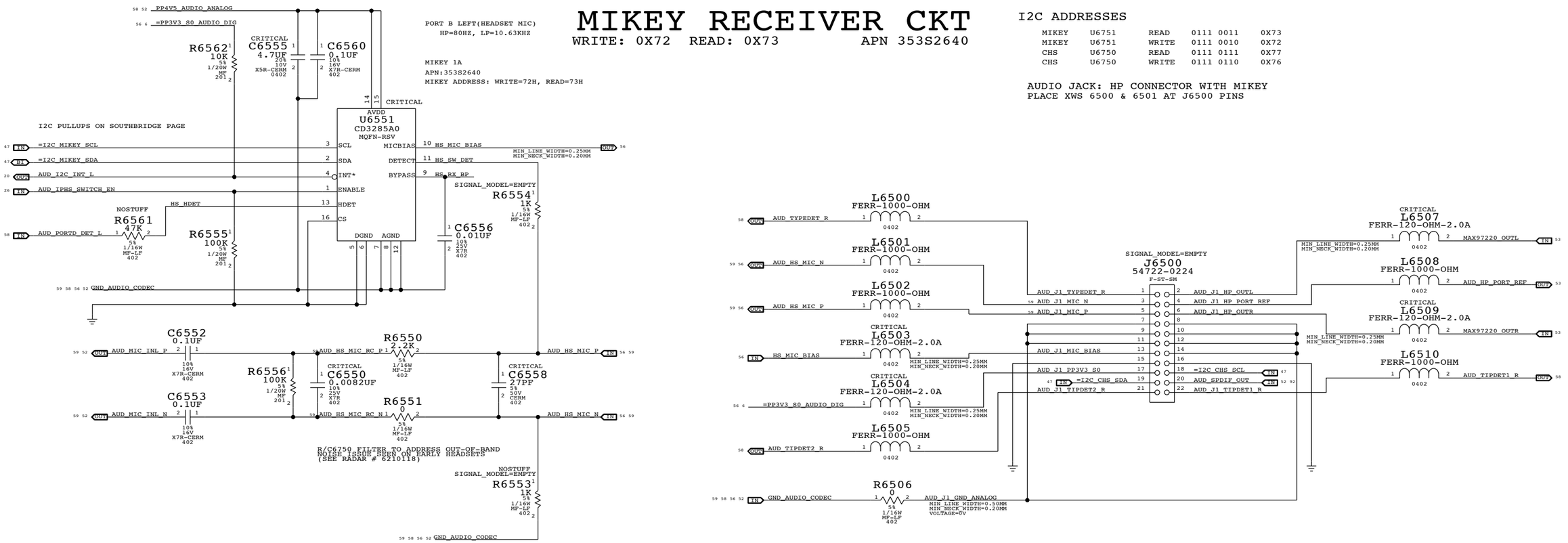
PORT B LEFT(HEADSET MIC)
HP=80HZ, LP=10.63KHZ

MIKEY 1A
APN:353S2640
MIKEY ADDRESS: WRITE=72H, READ=73H

I2C ADDRESSES

MIKEY	U6751	READ	0111 0011	0X73
MIKEY	U6751	WRITE	0111 0010	0X72
CHS	U6750	READ	0111 0111	0X77
CHS	U6750	WRITE	0111 0110	0X76

AUDIO JACK: HP CONNECTOR WITH MIKEY
PLACE XWS 6500 & 6501 AT J6500 PINS



SYNC_MASTER=D7 BREECE SYNC_DATE=01/03/2013

PAGE TITLE: AUDIO: Jack, Mikey, CHS Switch

Apple Inc.

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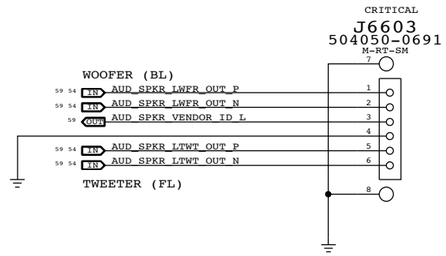
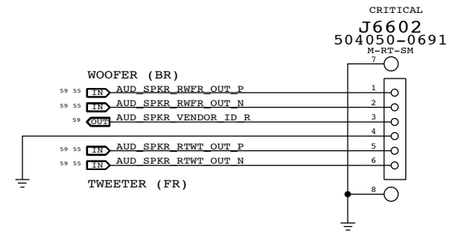
SPEAKER CABLE CONNECTORS

APPLE P/N 998-4119



APPLE P/N 998-4119



SYNC MASTER=D7 BREECE SYNC DATE=01/03/2012

PAGE TITLE
Audio: Spkr/Mic Conn.

Apple Inc.

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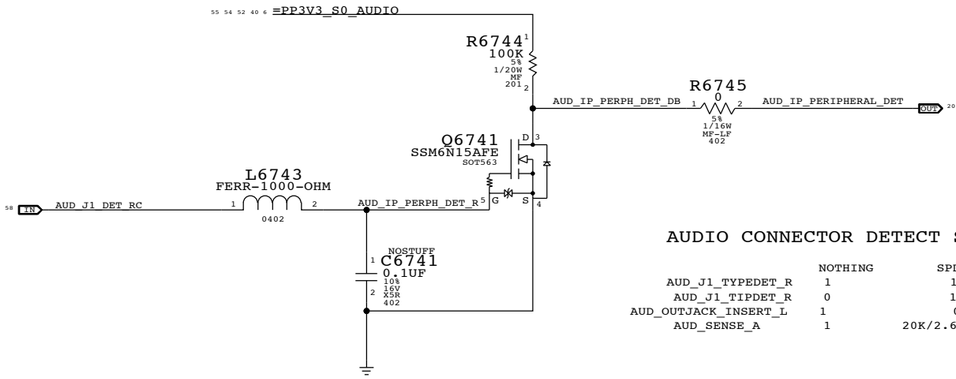
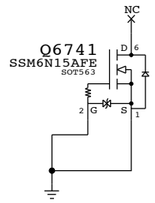
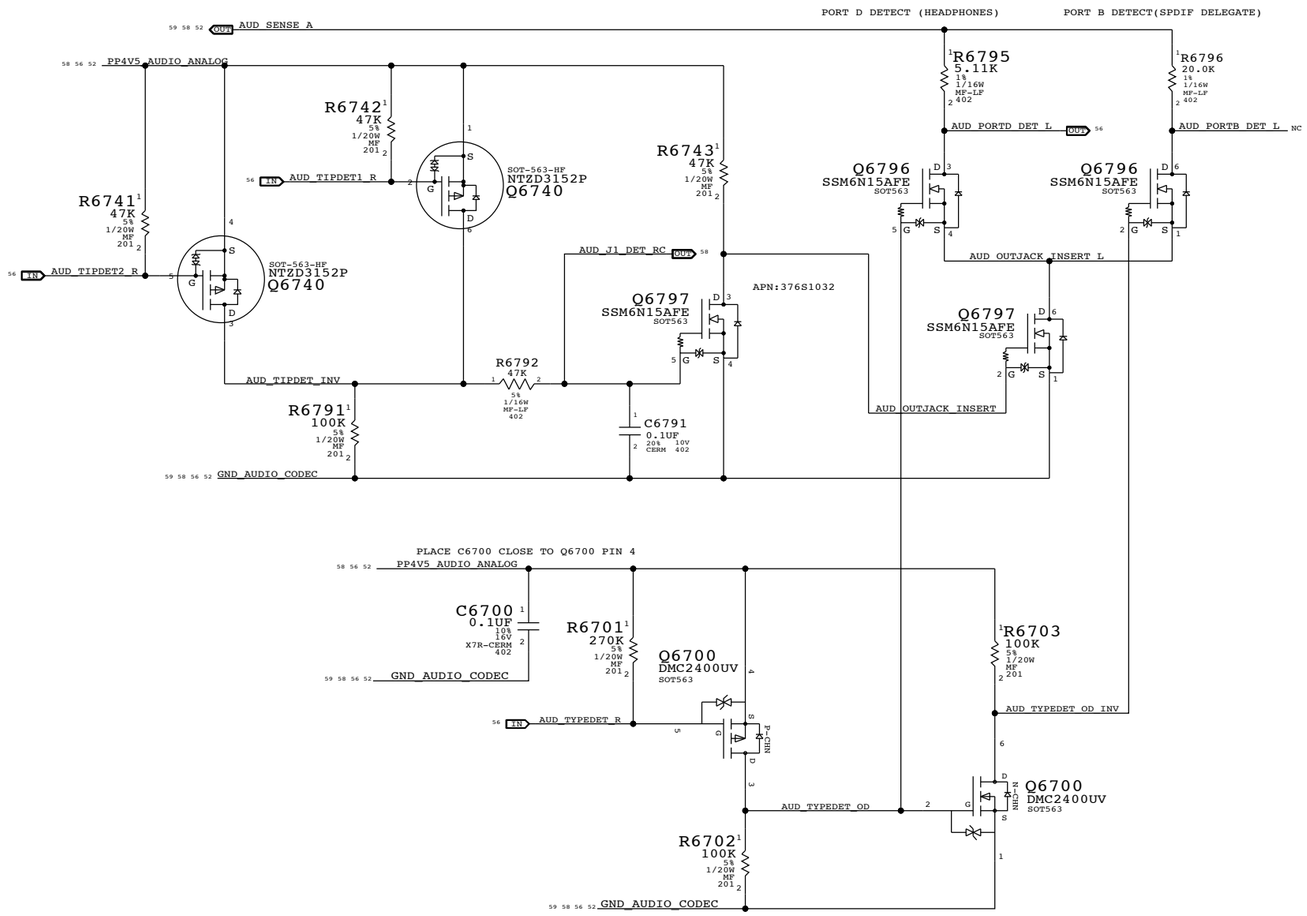
IPHS HS Detect Debounce CKT

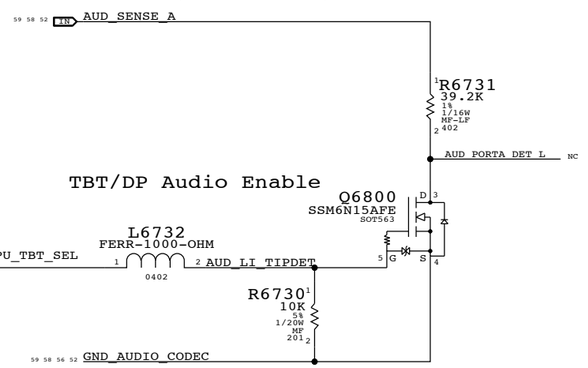


AUDIO CONNECTOR DETECT STATES

	NOTHING	SPDIF	HEADPHONE
AUD_J1_TYPEDET_R	1	1	0
AUD_J1_TIPDET_R	0	1	1
AUD_OUTJACK_INSERT_L	1	0	0
AUD_SENSE_A	1	20K/2.67K RDIV	39.2K/2.67K RDIV







SYNC_MASTER=D7_BREECE SYNC_DATE=01/03/2012

PAGE TITLE
AUDIO: Detects/Grounding

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	MAC SHDN	WIN SHDN	DET ASSIGNMENT
HP/LINE OUT	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	GPIO_2	0X0A (DET D)
PRIMARY SPKRS (WFR)	0X04 (4)	0X04 (4)	0X0B (11)	MICBIAS	GPIO_3	N/A
SECONDARY SPKRS (TWT)	0X03 (3)	0X03 (3)	0X0A (10,V24)	MICBIAS	N/A	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)	N/A	N/A	0X0D (DET B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
SPDIF IN	0X07 (7)	0x0F (15)	N/A	0X09 (DET A)
INTERNAL MIC ARRAY	0X06 (6) 0X05 (5)	0X0E (14,LEFT & RIGHT) 0X12 (18,LEFT)	N/A	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	PANTHER POINT GPIO 16	PANTHER POINT GPIO 5 (RCVR INT) PANTHER POINT GPIO 3 (PERIPH DET)

OTHER DETECT

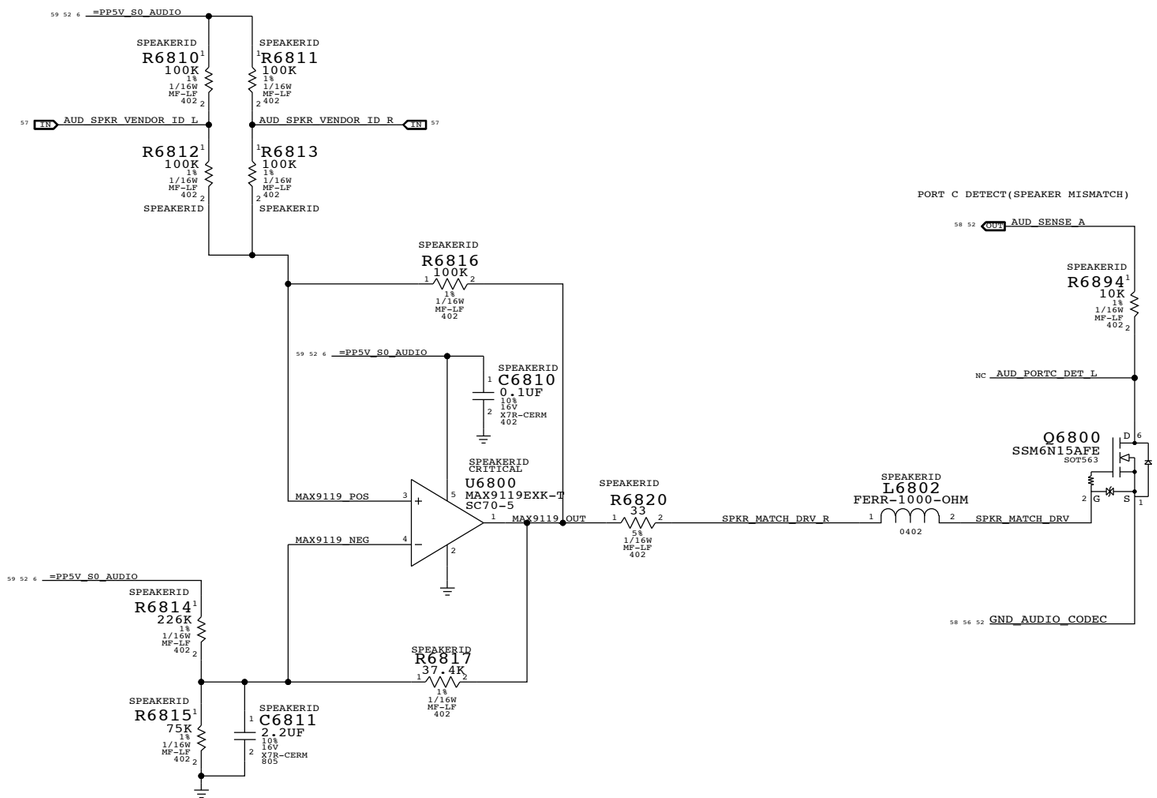
FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
MULTIPLE SPKR VENDORS	N/A	N/A	N/A	0X0C (DET C)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	0.1 MM	?
SPKROUT	*	0.2 MM	?

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
SPKROUTDIFF	*	SPKROUTDIFF

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIODIFF	*	Y	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
SPKROUTDIFF	*	Y	0.6 MM	0.25 MM	10 MM	0.2 MM	0.2 MM

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_P	52 53 54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_N	52 53 54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	52 53 55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_N	52 53 55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	52 54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N	52 54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	52 55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N	52 55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_P	55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_N	55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_P	55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_N	55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_P	55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_N	55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_P	55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_N	55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_P	54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_N	54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_P	54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_N	54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_P	54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_N	54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_P	54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_N	54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INL_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INL_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INR_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INR_N	53
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_P	55 57
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_N	55 57
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_P	55 57
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_N	55 57
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_P	54 57
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_N	54 57
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_P	54 57
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_N	54 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_P	52 56
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_N	52 56
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_RC_P	56
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_RC_N	56
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_P	56
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_N	56
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_J1_MIC_P	56
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_J1_MIC_N	56



SYNC_MASTER=D7 BREECE SYNC_DATE=01/03/2012

PAGE TITLE: AUDIO: Speaker ID

Apple Inc.

DRAWING NUMBER: 051-9509 SIZE: D

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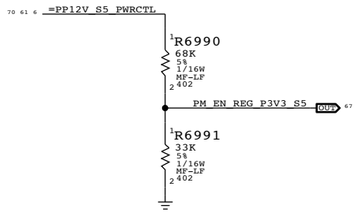
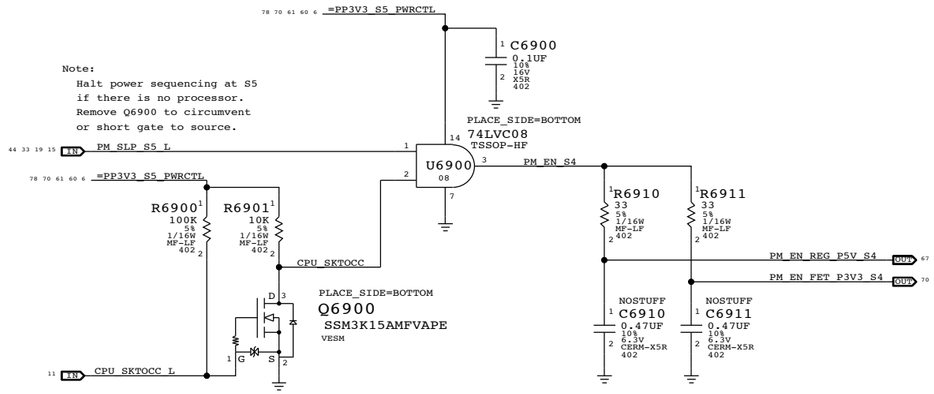
S5 Soft Enable

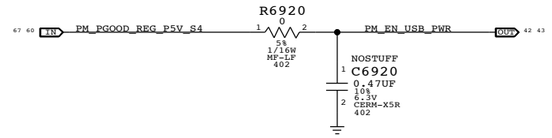


S4 Enables

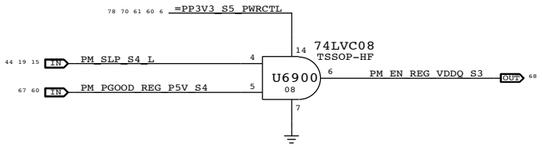


tau (RC delay, ms): 0.0 0.0

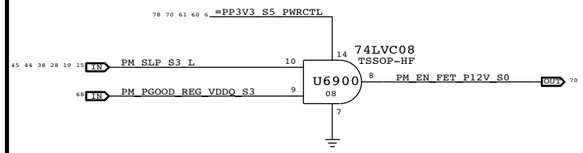
S4 USB Enable

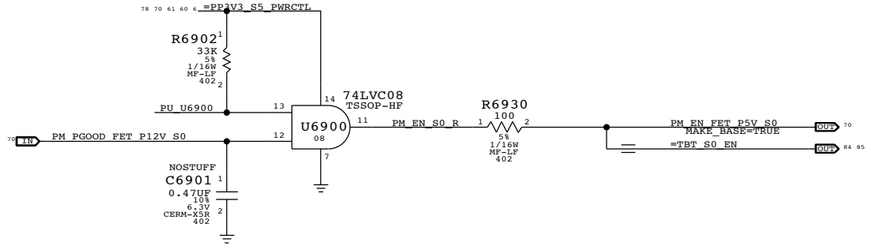


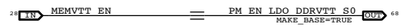
S3 VDDQ Enable

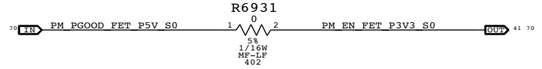


S0 Enables

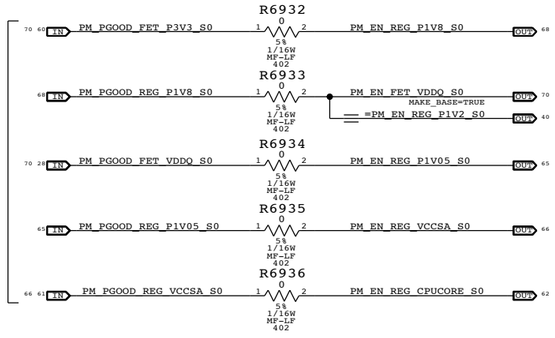




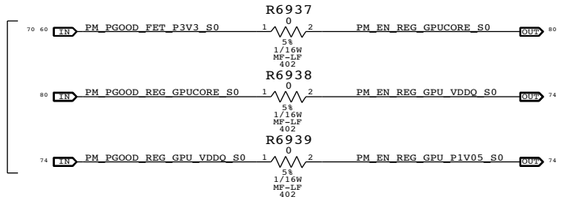




CPU/PCH Sequencing



GPU Sequencing



Rail definitions

Platform: All processor non-Core and non-Graphics (5 V, 3.3 V, 1.8 V 1.5 V, PCH Core/PLL/VRM)
Uncore: VccSA, VDDQ, VccA (1.8 V), VccIO (VccSA, VccA, and VccIO must ramp within 50 ms of each other)

Notes on sequencing requirements

Intel:
1. No hard specification on platform rails
2. SMC guarantees timing on PCH DPWROK and PWROK

NVIDIA:
1. 3V3_S0 must ramp first
2. IFPA/B_IOVDD (1.8 V) can ramp simultaneously or after 3V3_S0 (unused)
3. NVVDD (GPU_CORE) must ramp after IFPA/B_IOVDD
4. VDDQ must ramp after CPU_CORE
5. PEX_VDD with IFPC/D/E/F_IOVDD (1.05V) must ramp after VDDQ
6. All rails must reach their target voltages in more than 40 uS

SYNC_MASTER=D7_NICK SYNC_DATE=12/13/2011

PAGE TITLE
PM Regulator Enables

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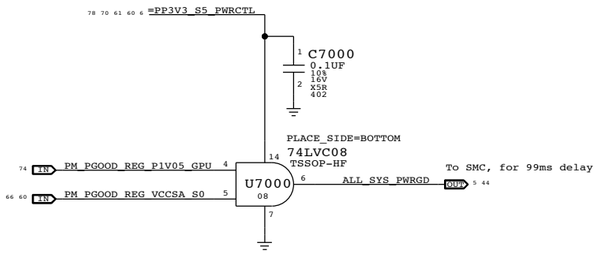
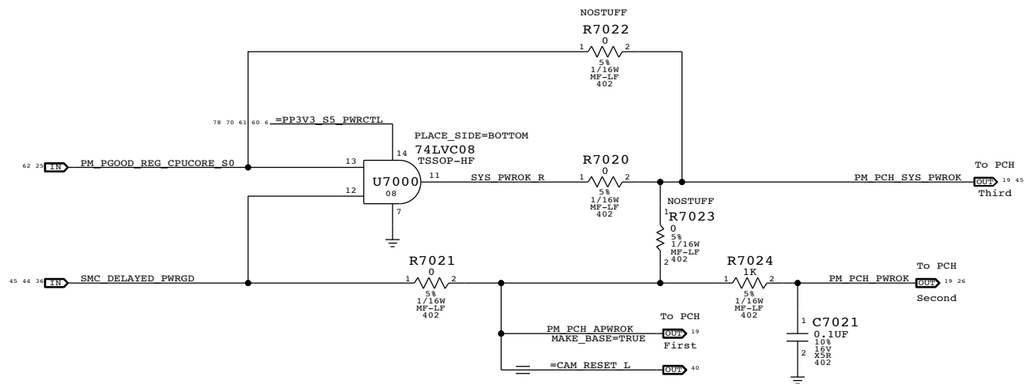
Platform and UnCore Power Good

Derive SMC ALL_SYS_PWRGD

Note: GPU power goods are implicitly included because the power goods for VDDQ, DPVDDC, and GPU Core are wired-or together



PCH Power Goods



Resume Reset

Intel Doc# 29517 Maho Bay PDG, Section 22.13
Intel Doc# 29562 Panther Point EDS, Section 8.7 and 8.8

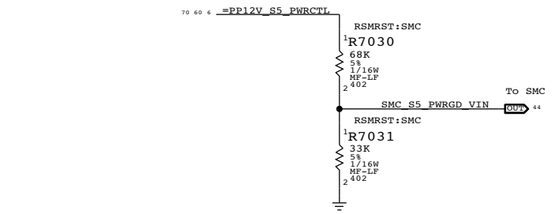
Note:
The iMac K70K72 designs does not support Deep Sx modes so both DPWROK and RSMRST# signals are shorted together

Requirements:
Power on:
Asserted at least 10 ms after all suspend well power is valid
Power off or loss of AC:
Transition to 0.8V or less before VccSUS3_3 drops to 2.90 V to allow PCH to switch suspend well to battery without excessive loading

Primary method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation.

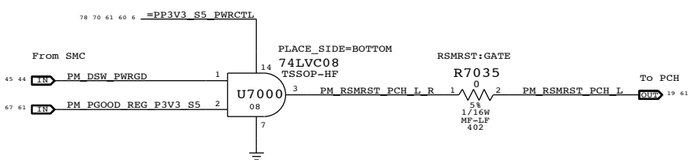
SMC de-asserts RSMRST# (PM_DSW_PWRGD) when S5_PWRGD input is asserted and SMC_S5_PWRGD_VIN input is above comparator input level of 1.5 V.

SMC asserts RSMRST# (PM_DSW_PWRGD) when SMC_S5_PWRGD_VIN input drops from 1.8 V to 1.5 V (as implemented) when 12 V S5 rail drops to 10 V.



Secondary method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation via PM_DSW_PWRGD.

RSMRST# is asserted when power good from regulator is de-asserted in the event AC is lost. Power good de-assertion should happen quickly enough to meet Intel spec.



SYNC_MASTER=D7 NICK SYNC_DATE=12/13/2011

PAGE TITLE
PM Power Good

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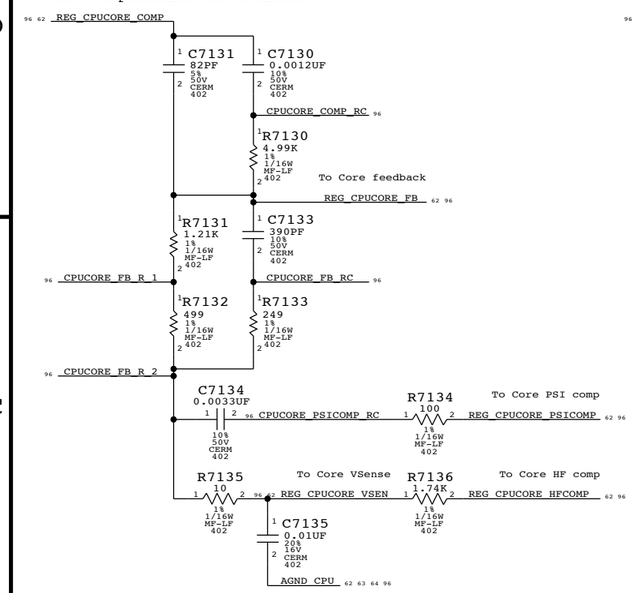
CPU Core S0 Regulator

Max avg current: ? A (design)/ 41.05 A (budget)
Max peak current: ? A (design)/75.05 A (budget)
OC trip point: ? A (nom)/? A (min)
Switching freq: 290 kHz

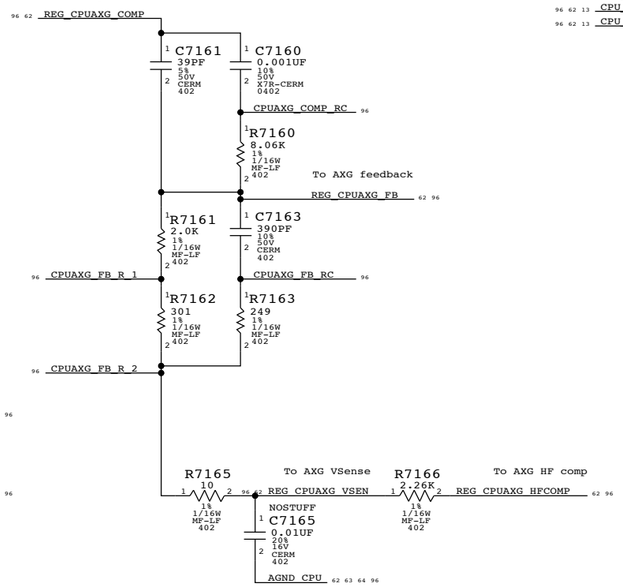
Core compensation and feedback



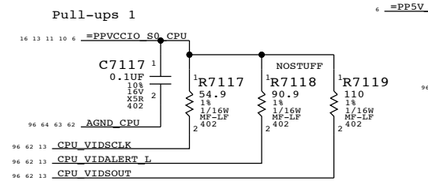
CPU AXG S0 Regulator

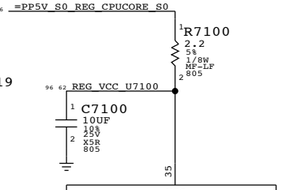
Max avg current: ? A (design)/ 10 A (budget)
Max peak current: ? A (design)/ 30 A (budget)
OC trip point: ? A (nom)/? A (min)
Switching freq: 290 kHz

AXG compensation and feedback

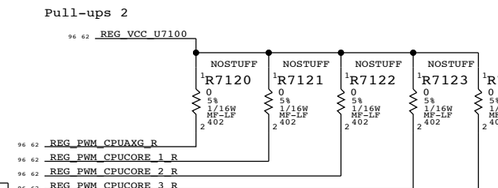


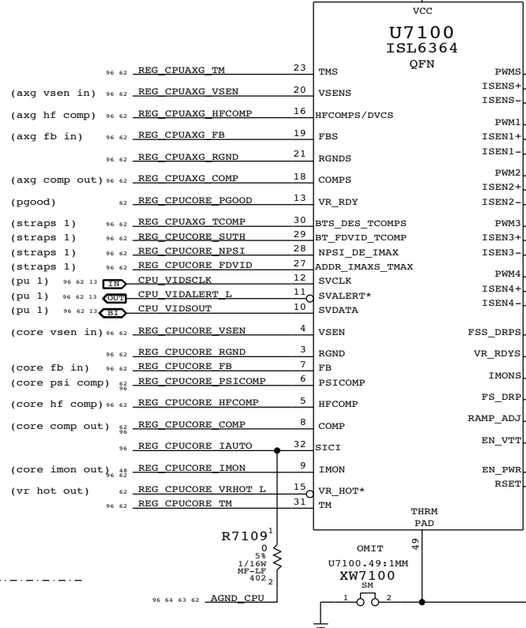
Pull-ups 1



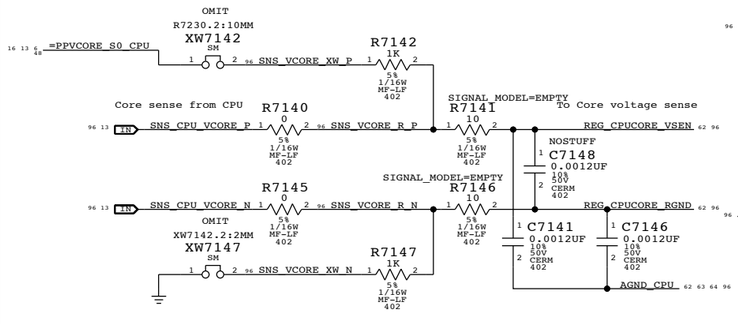


Pull-ups 2

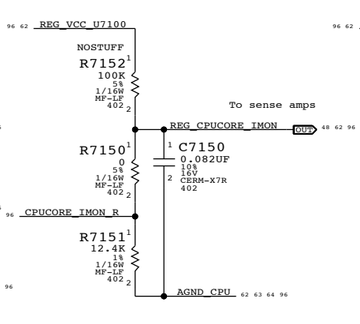




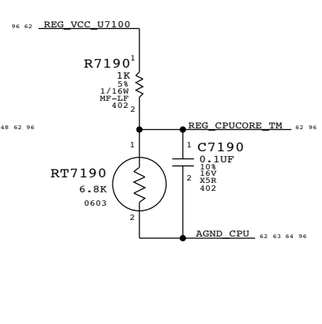
Core voltage sense input



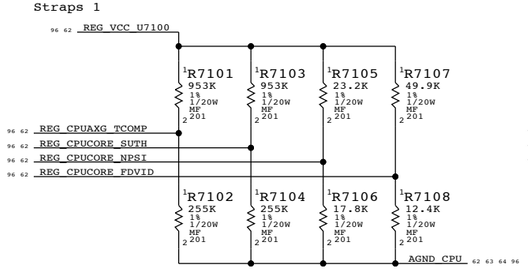
Core IMON output



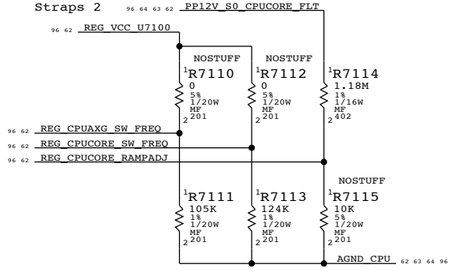
Core temp measurement



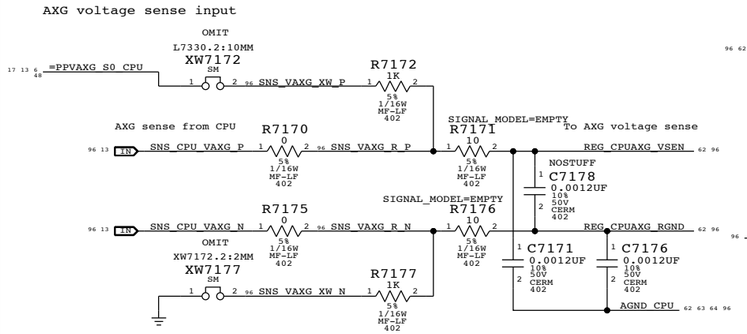
Straps 1



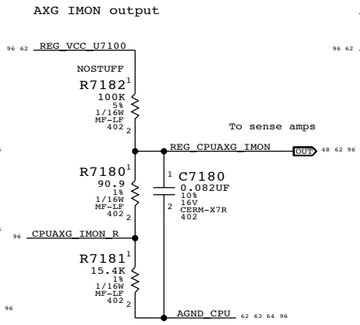
Straps 2



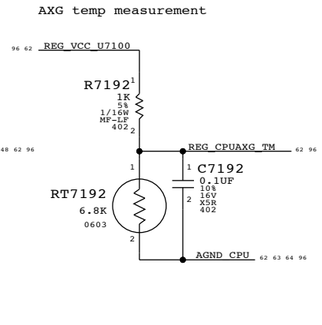
AXG voltage sense input



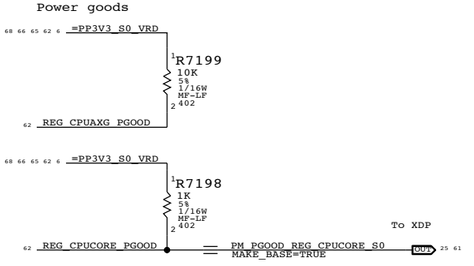
AXG IMON output



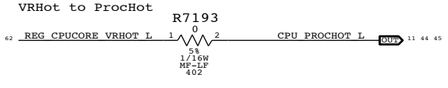
AXG temp measurement



Power goods



VRHot to ProcHot



SYNC_MASTER=D7_NICK SYNC_DATE=01/04/2012

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VReg CPU Core/AXG Cntl

Apple Inc.

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Filtered 12V Rail

CRITICAL L7200 0.36UH-28A-0.66MOHM SDP110808MR36MF-TH

=PP12V_S0_REG_CPUCORE_S0 → PP12V_S0_CPUCORE_FLT

CPU Phase 1

PP12V_S0_CPUCORE_FLT

U7210 ISL6622 DFN
VCC UVCC LVCC
GDSEL BOOT UGATE PHASE PWM LGATE GND THRML PAD

REG_LVCC_U7210
U7210.9:3MM C7225 1UF 10% 16V X5R 603
U7210.8:3MM C7226 1UF 10% 16V X5R 603
U7210.7:3MM C7227 1UF 10% 16V X5R 603

REG_BOOT_CPUCORE_1_RC
R7216 1 5% 1/10W MF-LF 603
C7216 0.22UF 20% 25V X5R 603

REG_BOOT_CPUCORE_1
REG_UGATE_CPUCORE_1
REG_PHASE_CPUCORE_1
REG_PWM_CPUCORE_1
REG_LGATE_CPUCORE_1

EMC Q7210.7:3MM C7218 1000PF 5% 25V NPO-C0G 402
EMC Q7210.8:3MM C7219 1000PF 5% 25V NPO-C0G 402

CRITICAL Q7210 IRF6802SDTRPBF DIRECTFET-SA

CRITICAL C7210 270UF 20% 16V ELEC 8X9-TH1
CRITICAL C7211 270UF 20% 16V ELEC 8X9-TH1
CRITICAL C7212 10UF 20% 25V X5R-CERM 0603
CRITICAL C7213 10UF 20% 25V X5R-CERM 0603
EMC Q7210.7:3MM C7214 1UF 10% 25V X5R 402
EMC Q7210.8:3MM C7215 1UF 10% 25V X5R 402

CRITICAL L7210 0.24UH-30A-0.38MOHM SDP110808M-TH
PPCPUCORE_S0_SENSE_1

CRITICAL R7210 0.0005 1% 1W MF 0612
PPCPUCORE_S0_REG

NCNC
CRITICAL Q7211 IRF6892STR1PBF DIRECTFET_S3C

C7217 0.0022UF 10% 50V CERM 402
REG_SNUBBER_CPUCORE_1
R7217 1 5% 1/8W MF-LF 805

REG_ISENCORE_1_P
SIGNAL_MODEL=EMPTY U7100.76:3MM
C7221 220PF 10% 50V X7R-CERM 402
SIGNAL_MODEL=EMPTY C7221.2:2MM
R7221 1.02K 1% 1/16W MF-LF 402
REG_ISENCORE_1_N
REG_ISENCORE_1_NR
SIGNAL_MODEL=EMPTY C7221.1:2MM
C7220 0.1UF 10% 16V X5R 402
AGND_CPU

CPU Phase 2

PP12V_S0_CPUCORE_FLT

CPUCOREDRV:ISL6612
R7247 10 5% 1/10W MF-LF 603

U7230 ISL6622 DFN
VCC UVCC LVCC
GDSEL BOOT UGATE OMIT_TABLE PHASE PWM LGATE GND THRML PAD

REG_LVCC_U7230
U7230.9:3MM C7245 1UF 10% 16V X5R 603
U7230.7:3MM C7247 1UF 10% 16V X5R 603

REG_BOOT_CPUCORE_2_RC
R7236 1 5% 1/10W MF-LF 603
C7236 0.22UF 20% 25V X5R 603

REG_BOOT_CPUCORE_2
REG_UGATE_CPUCORE_2
REG_PHASE_CPUCORE_2
REG_PWM_CPUCORE_2
REG_LGATE_CPUCORE_2

EMC Q7210.5:3MM C7238 1000PF 5% 25V NPO-C0G 402
EMC Q7210.6:3MM C7239 1000PF 5% 25V NPO-C0G 402

CRITICAL Q7210 IRF6802SDTRPBF DIRECTFET-SA

CRITICAL C7230 270UF 20% 16V ELEC 8X9-TH1
CRITICAL C7232 10UF 20% 25V X5R-CERM 0603
CRITICAL C7233 10UF 20% 25V X5R-CERM 0603
EMC Q7210.5:3MM C7234 1UF 10% 25V X5R 402
EMC Q7210.6:3MM C7235 1UF 10% 25V X5R 402

CRITICAL L7230 0.24UH-30A-0.38MOHM SDP110808M-TH
PPCPUCORE_S0_SENSE_2

CRITICAL R7230 0.0005 1% 1W MF 0612
PPCPUCORE_S0_REG

NCNC
CRITICAL Q7231 IRF6892STR1PBF DIRECTFET_S3C

C7237 0.0022UF 10% 50V CERM 402
REG_SNUBBER_CPUCORE_2
R7237 1 5% 1/8W MF-LF 805

REG_ISENCORE_2_P
SIGNAL_MODEL=EMPTY U7100.42:3MM
C7241 220PF 10% 50V X7R-CERM 402
SIGNAL_MODEL=EMPTY C7241.2:2MM
R7241 1.02K 1% 1/16W MF-LF 402
REG_ISENCORE_2_N
REG_ISENCORE_2_NR
SIGNAL_MODEL=EMPTY C7241.1:2MM
C7240 0.1UF 10% 16V X5R 402
AGND_CPU

CPU Phase 3

PP12V_S0_CPUCORE_FLT

CPUCOREDRV:ISL6612
R7267 10 5% 1/10W MF-LF 603

U7250 ISL6622 DFN
VCC UVCC LVCC
GDSEL BOOT UGATE OMIT_TABLE PHASE PWM LGATE GND THRML PAD

REG_LVCC_U7250
U7250.9:3MM C7265 1UF 10% 16V X5R 603
U7250.7:3MM C7267 1UF 10% 16V X5R 603

REG_BOOT_CPUCORE_3_RC
R7256 1 5% 1/10W MF-LF 603
C7256 0.22UF 20% 25V X5R 603

REG_BOOT_CPUCORE_3
REG_UGATE_CPUCORE_3
REG_PHASE_CPUCORE_3
REG_PWM_CPUCORE_3
REG_LGATE_CPUCORE_3

EMC Q7250.7:3MM C7258 1000PF 5% 25V NPO-C0G 402
EMC Q7250.8:3MM C7259 1000PF 5% 25V NPO-C0G 402

CRITICAL Q7250 IRF6802SDTRPBF DIRECTFET-SA

CRITICAL C7250 270UF 20% 16V ELEC 8X9-TH1
CRITICAL C7252 10UF 20% 25V X5R-CERM 0603
CRITICAL C7253 10UF 20% 25V X5R-CERM 0603
EMC Q7250.7:3MM C7254 1UF 10% 25V X5R 402
EMC Q7250.8:3MM C7255 1UF 10% 25V X5R 402

CRITICAL L7250 0.24UH-30A-0.38MOHM SDP110808M-TH
PPCPUCORE_S0_SENSE_3

CRITICAL R7250 0.0005 1% 1W MF 0612
PPCPUCORE_S0_REG

NCNC
CRITICAL Q7251 IRF6892STR1PBF DIRECTFET_S3C

C7257 0.0022UF 10% 50V CERM 402
REG_SNUBBER_CPUCORE_3
R7257 1 5% 1/8W MF-LF 805

REG_ISENCORE_3_P
SIGNAL_MODEL=EMPTY U7100.48:3MM
C7261 220PF 10% 50V X7R-CERM 402
SIGNAL_MODEL=EMPTY C7261.2:2MM
R7261 1.02K 1% 1/16W MF-LF 402
REG_ISENCORE_3_N
REG_ISENCORE_3_NR
SIGNAL_MODEL=EMPTY C7261.1:2MM
C7260 0.1UF 10% 16V X5R 402
AGND_CPU

CPU Output Decoupling

PPCPUCORE_S0_REG

CRITICAL C7280 330UF-0.006OHM 20% 2V POLY CASE-D2-SM
CRITICAL C7281 330UF-0.006OHM 20% 2V POLY CASE-D2-SM
CRITICAL C7282 330UF-0.006OHM 20% 2V POLY CASE-D2-SM
CRITICAL C7283 330UF-0.006OHM 20% 2V POLY CASE-D2-SM
CRITICAL C7284 330UF-0.006OHM 20% 2V POLY CASE-D2-SM
NOSTUFF CRITICAL C7285 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1733	2	IC,ISL6612,FET DRV,DFN10,LF	U7230,U7250	CRITICAL	CPUCOREDRV:ISL6612

SYNC_MASTER=D7 NICK
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VReg CPU Core Phases

Apple Inc.

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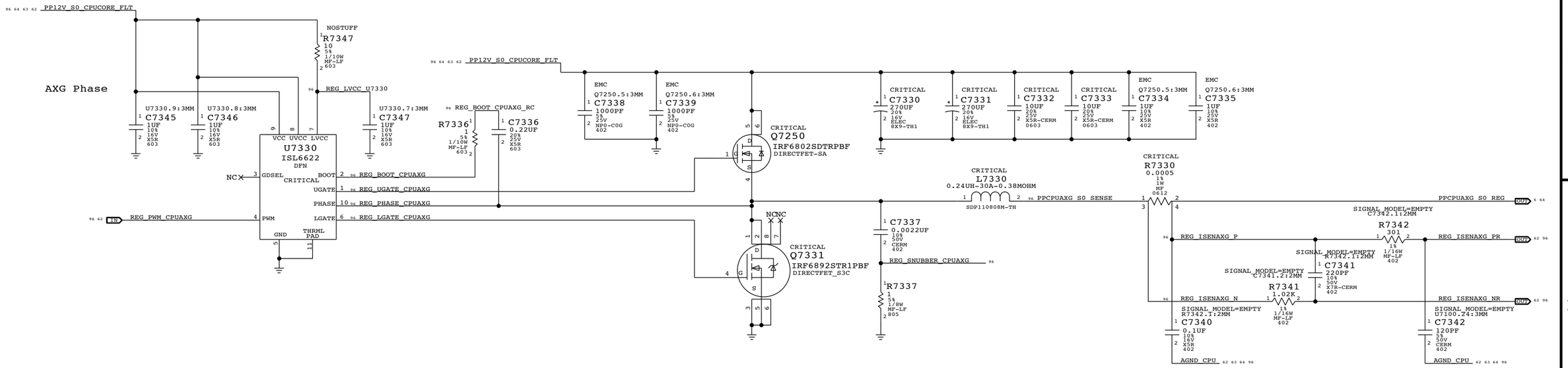

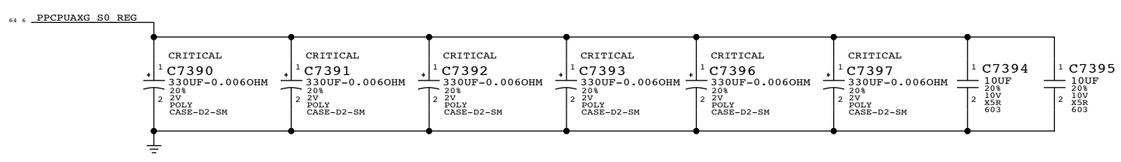

SYNC_MASTER=D7_NICK SYNC_DATE=01/04/2012

PAGE TITLE: VReg CPU AXG Phases

Apple Inc.

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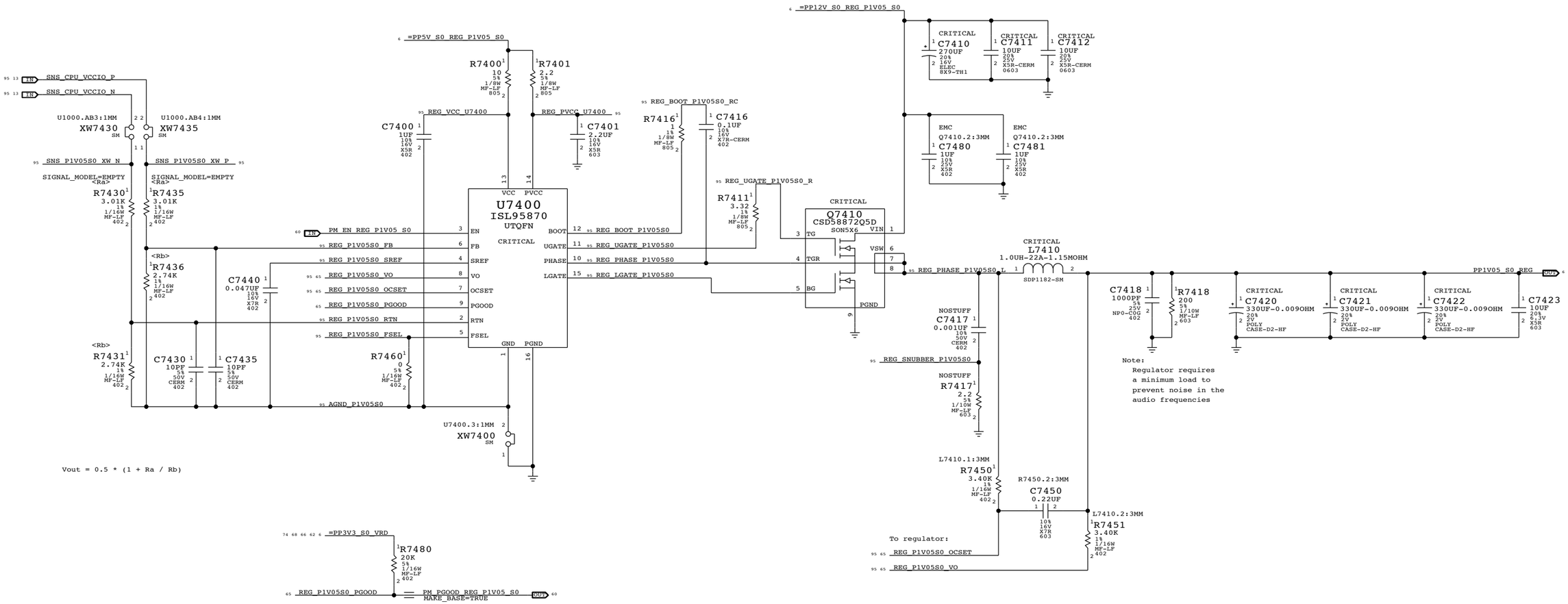
CPU VccIO/PCH (1.05V) S0 Regulator

Max avg current: ? A (design)/ 14.38 A (budget)
Max peak current: ? A (design)/ 18.38 A (budget)
OC trip point: ? A (min)/? A (max)
Switching freq: 500 kHz



SYNC_MASTER=D7 NICK SYNC_DATE=01/04/2012

PAGE TITLE: VReg CPU/PCH 1.05V S0

Apple Inc.

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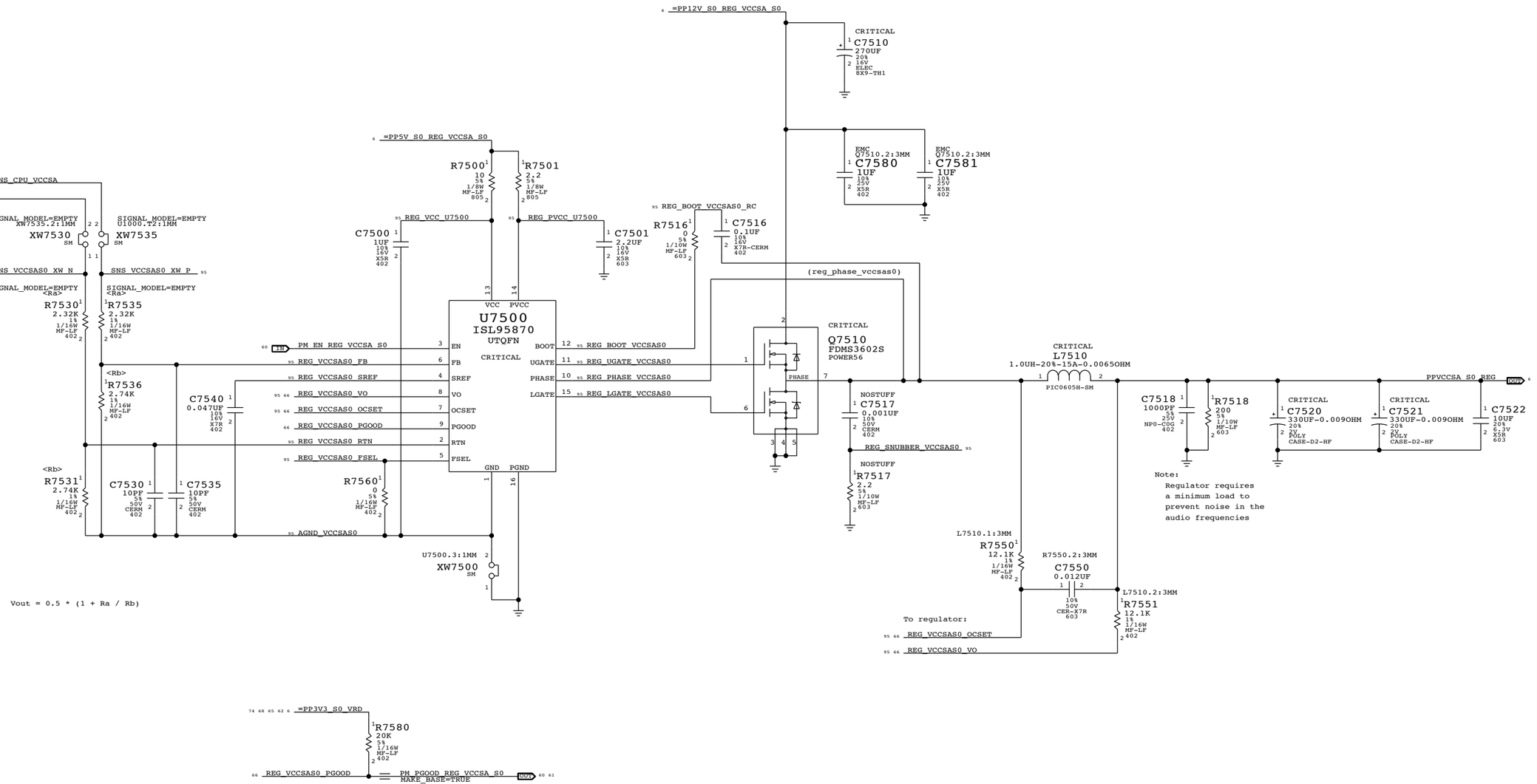
CPU VccSA (0.925V) S0 Regulator

Max avg current: ? A (design)/ 1.51 A (budget)
Max peak current: ? A (design)/ 8.76 A (budget)
OC trip point: ? A (min)/? A (max)
Switching freq: 500 kHz



SYNC_MASTER=D7 NICK SYNC_DATE=01/04/2012

PAGE TITLE: VReg CPU VccSA S0

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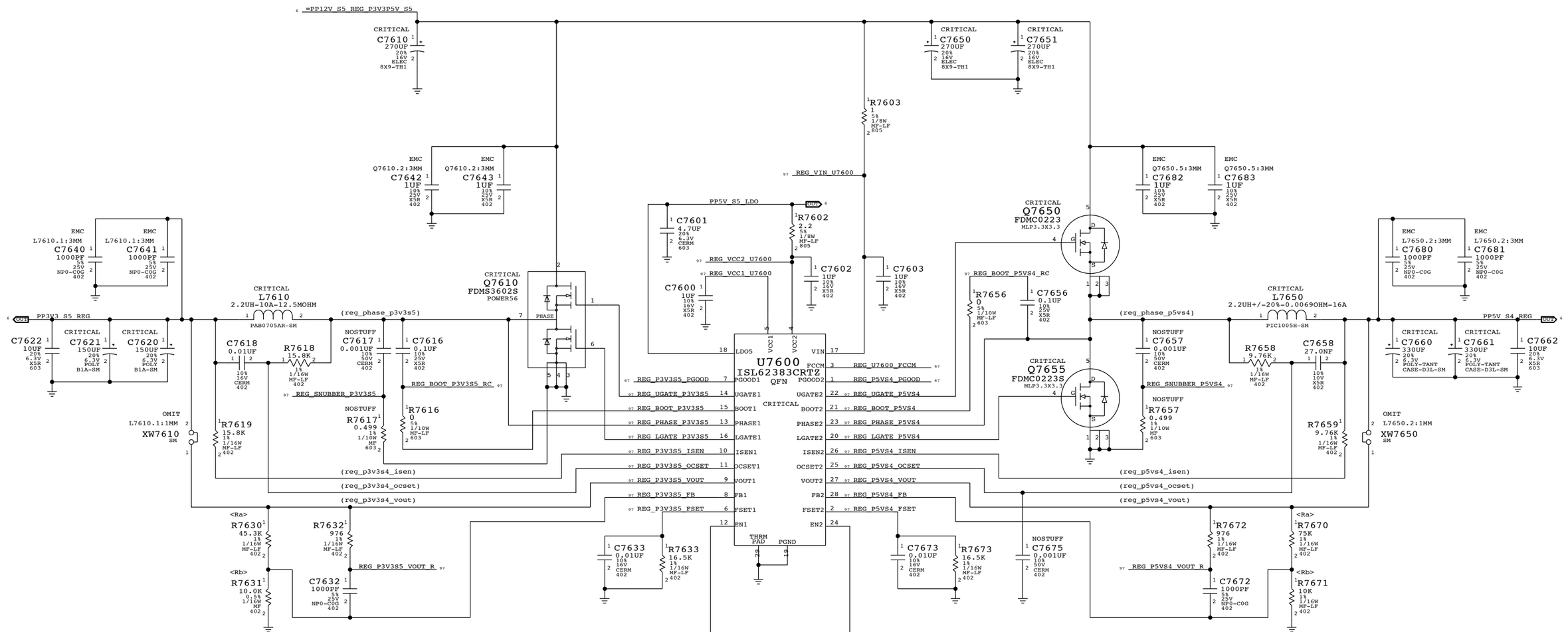
3.3V S5 Regulator

Max avg current: 6 A (design)/ 4.85 A (budget)
Max peak current: ? A (design)/ 6.6 A (budget)
OC trip point: ? A (nom)/? A (min)
Switching freq: 350 kHz

5V S4 Regulator

Max avg current: 10 A (design)/ 6.08 A (budget)
Max peak current: ? A (design)/ 6.9 A (budget)
OC trip point: ? A (nom)/? A (min)
Switching freq: 350 kHz



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PAGE TITLE: VReg 3.3V S5/5V S4

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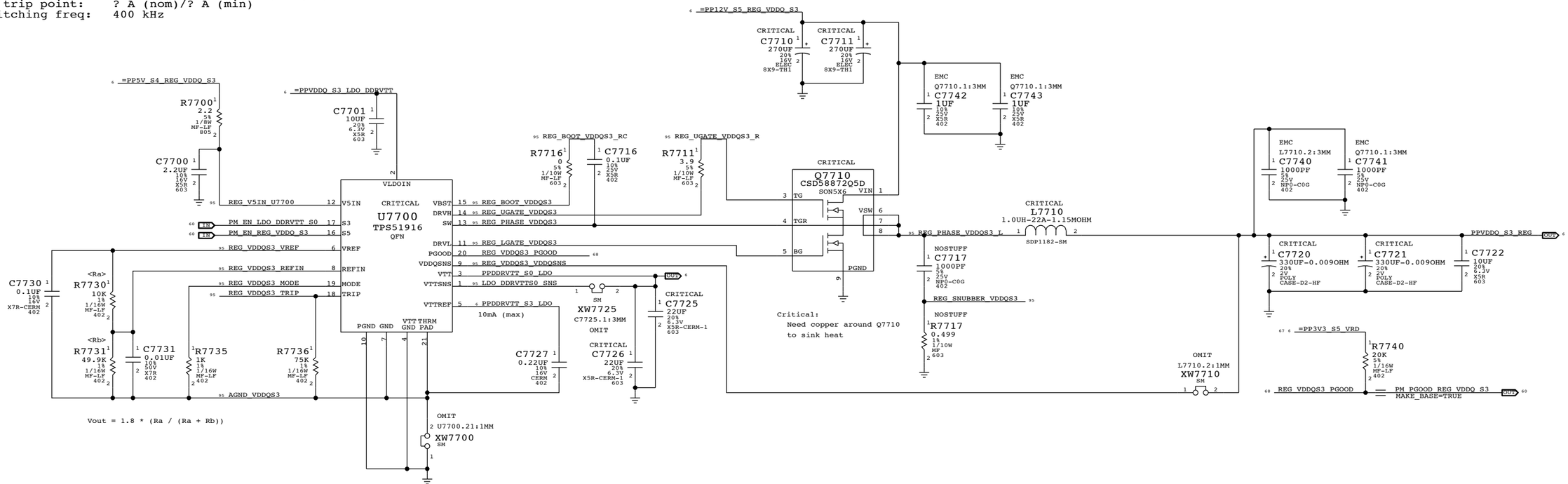
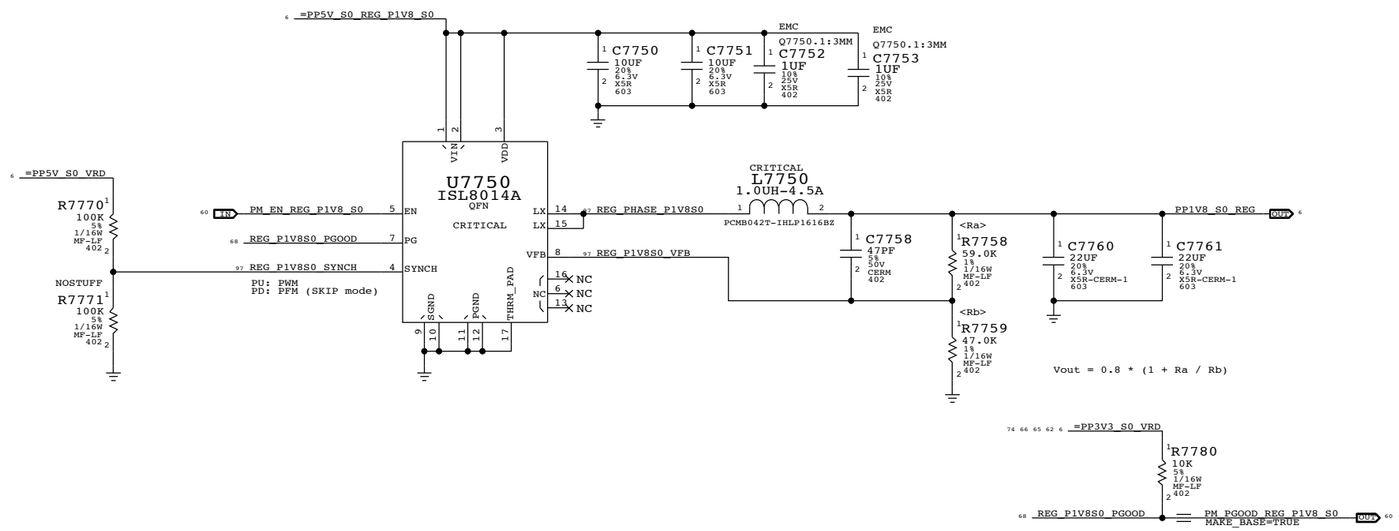
VDDQ (1.5V) S3 Regulator

Max avg current: ? A (design)/ 8 A (budget)
Max peak current: ? A (design)/ 17.8 A (budget)
OC trip point: ? A (nom)/? A (min)
Switching freq: 400 kHz



1.8V S0 Regulator

Max avg current: 3 A (design)/ 0.61 A (budget)
Max peak current: ? A (design)/ 1.83 A (budget)
OC trip point: ? A (nom)/? A (min)
Switching freq: ? kHz



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VReg VDDQ and 1.8V S0

Apple Inc.

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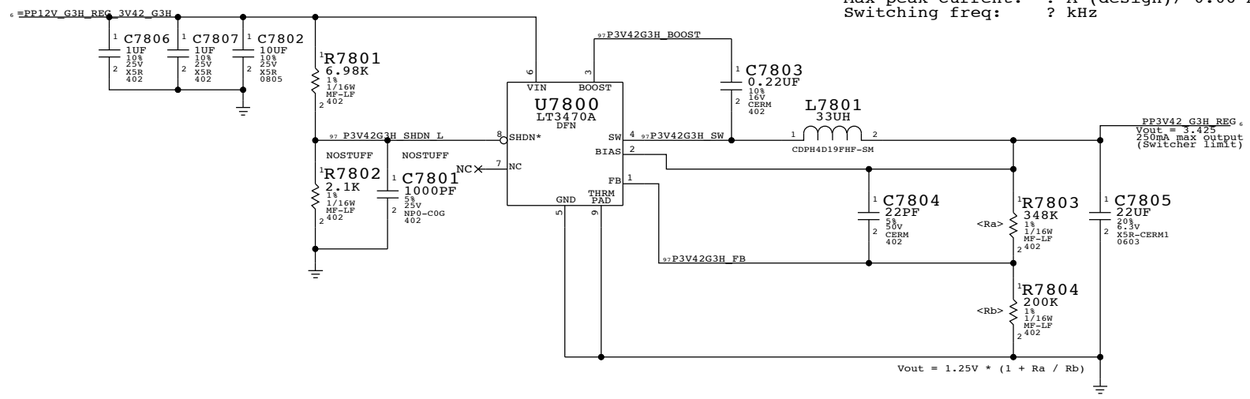
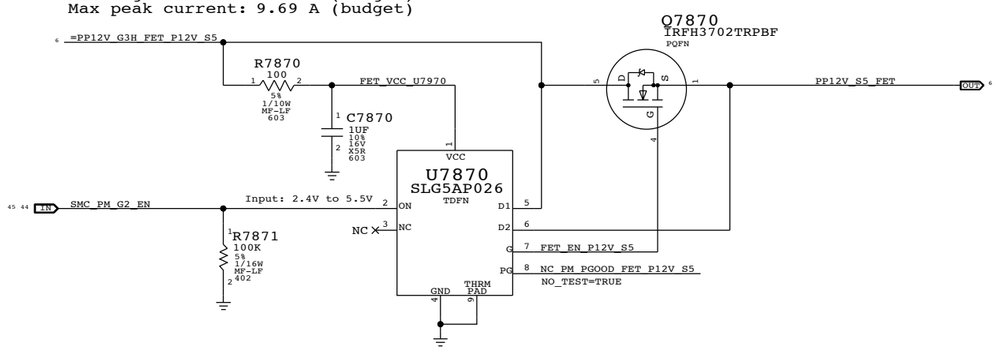
3.425V "G3Hot" Regulator

Max avg current: ? A (design)/ 0 A (budget)
Max peak current: ? A (design)/ 0.06 A (budget)
Switching freq: ? kHz



12V S5 FET

Max avg current: 7.03 A (budget)
Max peak current: 9.69 A (budget)



SYNC_MASTER=D7_NICK SYNC_DATE=01/04/2012

PAGE TITLE: VReg G3Hot

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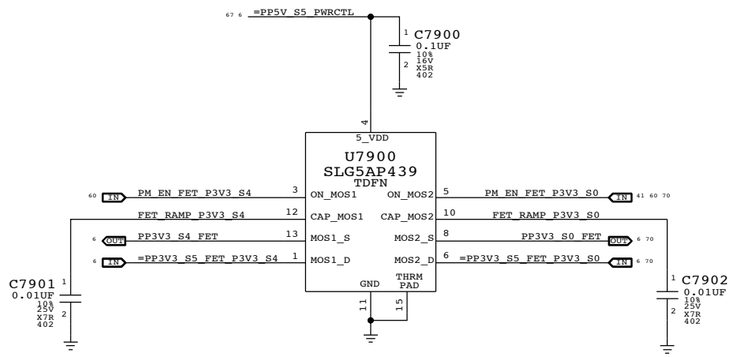
3.3V S4 FET

Max avg current: 0.85 A (budget)
Max peak current: 1.48 A (budget)

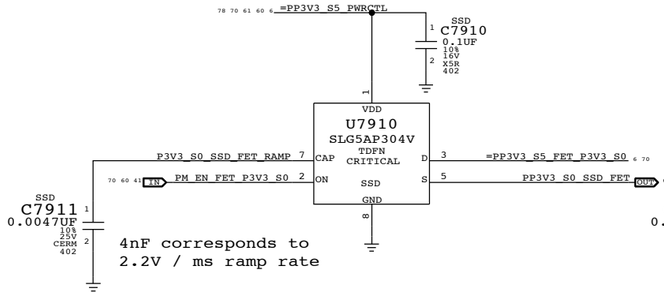


3.3V S0 FET

Max avg current: 1.7 A (budget)
Max peak current: 1.82 A (budget)

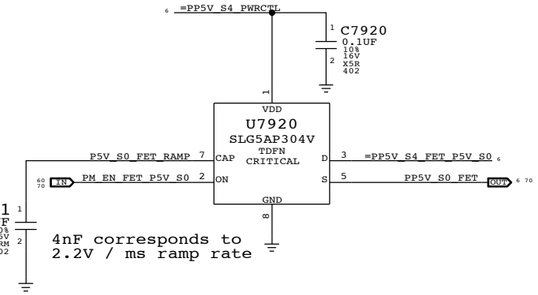
3V3 S0 SSD

Max avg current: 2.12 A (budget)
Max peak current: 3.03 A (budget)

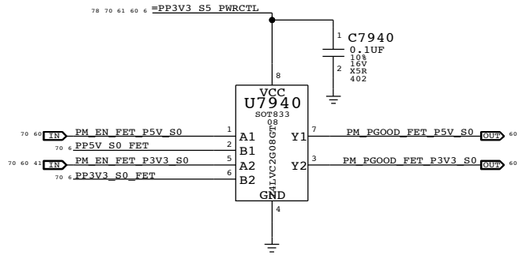


5V S0 FET

Max avg current: 1.26 A (budget)
Max peak current: 2.08 A (budget)

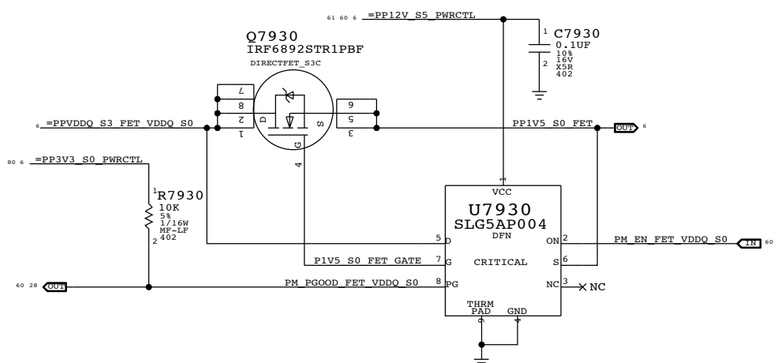


5V / 3V3 S0 PGOODs



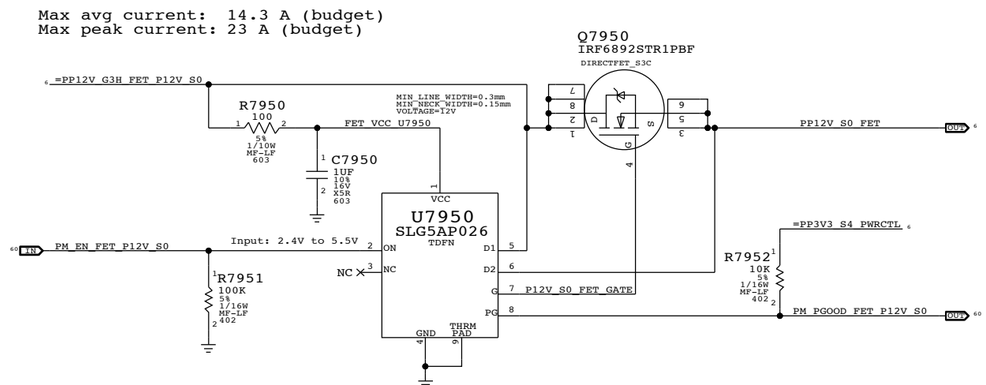
1.5V S0 FET

Max avg current: 1.27 A (budget)
Max peak current: 4.8 A (budget)



12V S0 FET

Max avg current: 14.3 A (budget)
Max peak current: 23 A (budget)



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FET-Controlled S0 and S4

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Page Notes

Power aliases required by this page:

- +PP3V3_GPU_VDD33

Signal aliases required by this page:

(NONE)

ROM options provided by this page:

(NONE)

Polarity swaps intended on Lanes 0, 5, 8, 9, and 11.

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PEG_R2D_C_N<0>	C8021	0.22UF	PEG_R2D_P<0>	PEG_R2D_C_N<8>	C8037	0.22UF	PEG_R2D_P<8>
PEG_R2D_C_P<1>	C8022	0.22UF	PEG_R2D_P<1>	PEG_R2D_C_P<9>	C8038	0.22UF	PEG_R2D_N<9>
PEG_R2D_C_N<1>	C8023	0.22UF	PEG_R2D_N<1>	PEG_R2D_C_N<9>	C8039	0.22UF	PEG_R2D_P<9>
PEG_R2D_C_P<2>	C8024	0.22UF	PEG_R2D_P<2>	PEG_R2D_C_P<10>	C8040	0.22UF	PEG_R2D_P<10>
PEG_R2D_C_N<2>	C8025	0.22UF	PEG_R2D_N<2>	PEG_R2D_C_N<10>	C8041	0.22UF	PEG_R2D_N<10>
PEG_R2D_C_P<3>	C8026	0.22UF	PEG_R2D_P<3>	PEG_R2D_C_P<11>	C8042	0.22UF	PEG_R2D_P<11>
PEG_R2D_C_N<3>	C8027	0.22UF	PEG_R2D_N<3>	PEG_R2D_C_N<11>	C8043	0.22UF	PEG_R2D_N<11>
PEG_R2D_C_P<4>	C8028	0.22UF	PEG_R2D_P<4>	PEG_R2D_C_P<12>	C8044	0.22UF	PEG_R2D_P<12>
PEG_R2D_C_N<4>	C8029	0.22UF	PEG_R2D_N<4>	PEG_R2D_C_N<12>	C8045	0.22UF	PEG_R2D_N<12>
PEG_R2D_C_P<5>	C8030	0.22UF	PEG_R2D_N<5>	PEG_R2D_C_P<13>	C8046	0.22UF	PEG_R2D_N<13>
PEG_R2D_C_N<5>	C8031	0.22UF	PEG_R2D_P<5>	PEG_R2D_C_N<13>	C8047	0.22UF	PEG_R2D_P<13>
PEG_R2D_C_P<6>	C8032	0.22UF	PEG_R2D_P<6>	PEG_R2D_C_P<14>	C8048	0.22UF	PEG_R2D_P<14>
PEG_R2D_C_N<6>	C8033	0.22UF	PEG_R2D_N<6>	PEG_R2D_C_N<14>	C8049	0.22UF	PEG_R2D_N<14>
PEG_R2D_C_P<7>	C8034	0.22UF	PEG_R2D_P<7>	PEG_R2D_C_P<15>	C8050	0.22UF	PEG_R2D_P<15>
PEG_R2D_C_N<7>	C8035	0.22UF	PEG_R2D_N<7>	PEG_R2D_C_N<15>	C8051	0.22UF	PEG_R2D_N<15>

Polarity swapped!!

PEG_D2R_C_N<0>	C8055	0.22UF	PEG_D2R_P<0>	PEG_D2R_C_N<8>	C8071	0.22UF	PEG_D2R_P<8>
PEG_D2R_C_P<0>	C8056	0.22UF	PEG_D2R_N<0>	PEG_D2R_C_P<8>	C8072	0.22UF	PEG_D2R_N<8>
PEG_D2R_C_P<1>	C8057	0.22UF	PEG_D2R_P<1>	PEG_D2R_C_P<9>	C8073	0.22UF	PEG_D2R_N<9>
PEG_D2R_C_N<1>	C8058	0.22UF	PEG_D2R_N<1>	PEG_D2R_C_N<9>	C8074	0.22UF	PEG_D2R_P<9>
PEG_D2R_C_P<2>	C8059	0.22UF	PEG_D2R_P<2>	PEG_D2R_C_P<10>	C8075	0.22UF	PEG_D2R_P<10>
PEG_D2R_C_N<2>	C8060	0.22UF	PEG_D2R_N<2>	PEG_D2R_C_N<10>	C8076	0.22UF	PEG_D2R_N<10>
PEG_D2R_C_P<3>	C8061	0.22UF	PEG_D2R_P<3>	PEG_D2R_C_P<11>	C8077	0.22UF	PEG_D2R_N<11>
PEG_D2R_C_N<3>	C8062	0.22UF	PEG_D2R_N<3>	PEG_D2R_C_N<11>	C8078	0.22UF	PEG_D2R_P<11>
PEG_D2R_C_P<4>	C8063	0.22UF	PEG_D2R_P<4>	PEG_D2R_C_P<12>	C8079	0.22UF	PEG_D2R_P<12>
PEG_D2R_C_N<4>	C8064	0.22UF	PEG_D2R_N<4>	PEG_D2R_C_N<12>	C8080	0.22UF	PEG_D2R_N<12>
PEG_D2R_C_P<5>	C8065	0.22UF	PEG_D2R_P<5>	PEG_D2R_C_P<13>	C8081	0.22UF	PEG_D2R_P<13>
PEG_D2R_C_N<5>	C8066	0.22UF	PEG_D2R_N<5>	PEG_D2R_C_N<13>	C8082	0.22UF	PEG_D2R_N<13>
PEG_D2R_C_P<6>	C8067	0.22UF	PEG_D2R_P<6>	PEG_D2R_C_P<14>	C8083	0.22UF	PEG_D2R_P<14>
PEG_D2R_C_N<6>	C8068	0.22UF	PEG_D2R_N<6>	PEG_D2R_C_N<14>	C8084	0.22UF	PEG_D2R_N<14>
PEG_D2R_C_N<7>	C8069	0.22UF	PEG_D2R_P<7>	PEG_D2R_C_P<15>	C8085	0.22UF	PEG_D2R_P<15>
PEG_D2R_C_P<7>	C8070	0.22UF	PEG_D2R_N<7>	PEG_D2R_C_N<15>	C8086	0.22UF	PEG_D2R_N<15>

Polarity swapped!!

DP_TBTSNK0_EG_AUXCH_P ═ DP_TBTSNK0_AUXCH_C_P (MAKE_BASE=TRUE)
DP_TBTSNK0_EG_AUXCH_N ═ DP_TBTSNK0_AUXCH_C_N (MAKE_BASE=TRUE)
DP_TBTSNK1_EG_AUXCH_P ═ DP_TBTSNK1_AUXCH_C_P (MAKE_BASE=TRUE)
DP_TBTSNK1_EG_AUXCH_N ═ DP_TBTSNK1_AUXCH_C_N (MAKE_BASE=TRUE)

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PEG_R2D_P<0>	AN12	PEX_RX0	PEX_TX0	AK14	PEG_D2R_C_P<0>
PEG_R2D_N<0>	AM12	PEX_RX0*	PEX_TX0*	AJ14	PEG_D2R_C_N<0>
PEG_R2D_P<1>	AN14	PEX_RX1	PEX_TX1	AH14	PEG_D2R_C_P<1>
PEG_R2D_N<1>	AM14	PEX_RX1*	PEX_TX1*	AG14	PEG_D2R_C_N<1>
PEG_R2D_P<2>	AP14	PEX_RX2	PEX_TX2	AK15	PEG_D2R_C_P<2>
PEG_R2D_N<2>	AP15	PEX_RX2*	PEX_TX2*	AJ15	PEG_D2R_C_N<2>
PEG_R2D_P<3>	AN15	PEX_RX3	PEX_TX3	AL16	PEG_D2R_C_P<3>
PEG_R2D_N<3>	AM15	PEX_RX3*	PEX_TX3*	AK16	PEG_D2R_C_N<3>
PEG_R2D_P<4>	AN17	PEX_RX4	PEX_TX4	AK17	PEG_D2R_C_P<4>
PEG_R2D_N<4>	AM17	PEX_RX4*	PEX_TX4*	AJ17	PEG_D2R_C_N<4>
PEG_R2D_P<5>	AP17	PEX_RX5	PEX_TX5	AH17	PEG_D2R_C_P<5>
PEG_R2D_N<5>	AP18	PEX_RX5*	PEX_TX5*	AG17	PEG_D2R_C_N<5>
PEG_R2D_P<6>	AN18	PEX_RX6	PEX_TX6	AK18	PEG_D2R_C_P<6>
PEG_R2D_N<6>	AM18	PEX_RX6*	PEX_TX6*	AJ18	PEG_D2R_C_N<6>
PEG_R2D_P<7>	AN20	PEX_RX7	PEX_TX7	AL19	PEG_D2R_C_P<7>
PEG_R2D_N<7>	AM20	PEX_RX7*	PEX_TX7*	AK19	PEG_D2R_C_N<7>
PEG_R2D_P<8>	AP20	PEX_RX8	PEX_TX8	AK20	PEG_D2R_C_P<8>
PEG_R2D_N<8>	AP21	PEX_RX8*	PEX_TX8*	AJ20	PEG_D2R_C_N<8>
PEG_R2D_P<9>	AN21	PEX_RX9	PEX_TX9	AH20	PEG_D2R_C_P<9>
PEG_R2D_N<9>	AM21	PEX_RX9*	PEX_TX9*	AG20	PEG_D2R_C_N<9>
PEG_R2D_P<10>	AN23	PEX_RX10	PEX_TX10	AK21	PEG_D2R_C_P<10>
PEG_R2D_N<10>	AM23	PEX_RX10*	PEX_TX10*	AJ21	PEG_D2R_C_N<10>
PEG_R2D_P<11>	AP23	PEX_RX11	PEX_TX11	AL22	PEG_D2R_C_P<11>
PEG_R2D_N<11>	AP24	PEX_RX11*	PEX_TX11*	AK22	PEG_D2R_C_N<11>
PEG_R2D_P<12>	AN24	PEX_RX12	PEX_TX12	AK23	PEG_D2R_C_P<12>
PEG_R2D_N<12>	AM24	PEX_RX12*	PEX_TX12*	AJ23	PEG_D2R_C_N<12>
PEG_R2D_P<13>	AN26	PEX_RX13	PEX_TX13	AH23	PEG_D2R_C_P<13>
PEG_R2D_N<13>	AM26	PEX_RX13*	PEX_TX13*	AG23	PEG_D2R_C_N<13>
PEG_R2D_P<14>	AP26	PEX_RX14	PEX_TX14	AK24	PEG_D2R_C_P<14>
PEG_R2D_N<14>	AP27	PEX_RX14*	PEX_TX14*	AJ24	PEG_D2R_C_N<14>
PEG_R2D_P<15>	AN27	PEX_RX15	PEX_TX15	AL25	PEG_D2R_C_P<15>
PEG_R2D_N<15>	AM27	PEX_RX15*	PEX_TX15*	AK25	PEG_D2R_C_N<15>

PEG_CLK100M_P	AL13	PEX_REFCLK	PEX_TSTCLK_OUT	AJ26	PEX_TSTCLK_O_PL
PEG_CLK100M_N	AK13	PEX_REFCLK*	PEX_TSTCLK_OUT*	AK26	PEX_TSTCLK_O_NG
GPU_RESET_L	AJ12	PEX_RST*	PEX_TERMP	AP29	GPU_PEX_TERMP
PEG_CLKREQ_L	AK12	PEX_CLKREQ*			
NC	AJ11	PEX_WAKE*	PEX_SVDD_3V3	AG12	+PP3V3_GPU_VDD33

R8002 200 1% 1/20W MF 201 — NOSTUFF
R8000 0 GPU_RESET_R_L 1% 1/20W MF 201
R8005 2.49K 1% 1/20W MF 201

SYNC_MASTER=D7 TONY	SYNC_DATE=01/10/2012
PAGE TITLE	KEPLER PCI-E
Apple Inc.	DRAWING NUMBER 051-9509
	SIZE D
	REVISION 4.2.0
	BRANCH
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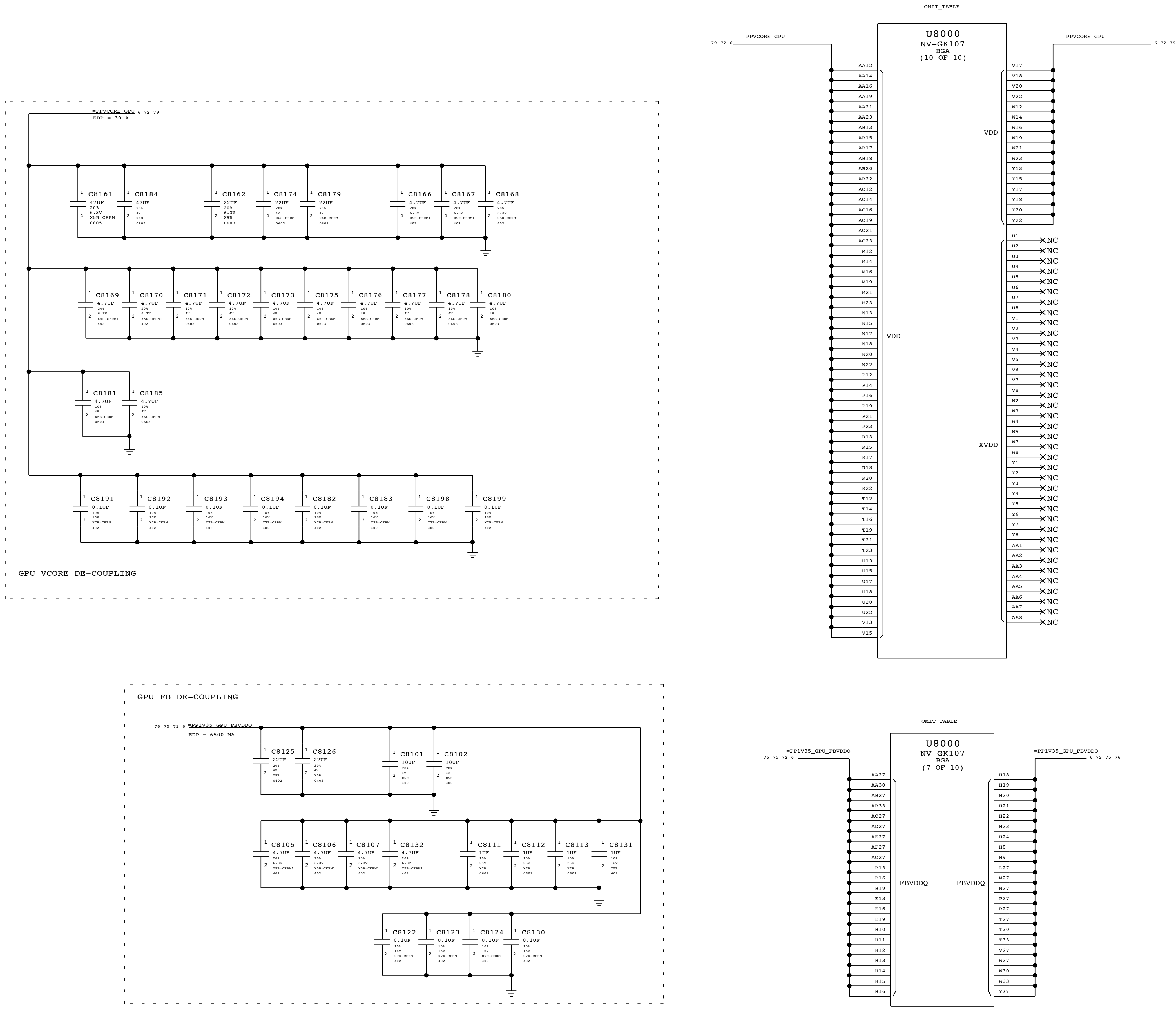
Page Notes



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PAGE TITLE

KEPLER CORE/FB POWER

Apple Inc.

DRAWING NUMBER 051-9509 SIZE D

REVISION 4.2.0

BRANCH

NOTE:GDDR5 MODE N MAPPING

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MEM INTERFACE A

FBA_D0	L28	FBA_CMD0	U30	FB_A0_CS_L	OUT
FBA_D1	M29	FBA_CMD1	T31	FB_A0_A<3>	OUT
FBA_D2	L29	FBA_CMD2	U29	FB_A0_A<2>	OUT
FBA_D3	M28	FBA_CMD3	R34	FB_A0_A<4>	OUT
FBA_D4	N31	FBA_CMD4	R33	FB_A0_A<5>	OUT
FBA_D5	P29	FBA_CMD5	U32	FB_A0_WE_L	OUT
FBA_D6	R29	FBA_CMD6	U33	FB_A0_A<7>	OUT
FBA_D7	P28	FBA_CMD7	U28	FB_A0_A<6>	OUT
FBA_D8	J28	FBA_CMD8	V28	FB_A0_ABI_L	OUT
FBA_D9	H29	FBA_CMD9	V29	FB_A0_A<8>	OUT
FBA_D10	J29	FBA_CMD10	V30	FB_A0_A<0>	OUT
FBA_D11	H28	FBA_CMD11	U34	FB_A0_A<1>	OUT
FBA_D12	G29	FBA_CMD12	V31	FB_A0_RAS_L	OUT
FBA_D13	E31	FBA_CMD13	V34	FB_A0_RESET_L	OUT
FBA_D14	E32	FBA_CMD14	V33	FB_A0_CKE_L	OUT
FBA_D15	F30	FBA_CMD15	Y32	FB_A0_CAS_L	OUT
FBA_D16	C34	FBA_CMD16	AA31	FB_A1_CS_L	OUT
FBA_D17	D32	FBA_CMD17	AA29	FB_A1_A<3>	OUT
FBA_D18	B33	FBA_CMD18	AA28	FB_A1_A<2>	OUT
FBA_D19	C33	FBA_CMD19	AC34	FB_A1_A<4>	OUT
FBA_D20	F33	FBA_CMD20	AC33	FB_A1_A<5>	OUT
FBA_D21	F32	FBA_CMD21	AA32	FB_A1_WE_L	OUT
FBA_D22	H33	FBA_CMD22	AA33	FB_A1_A<7>	OUT
FBA_D23	H32	FBA_CMD23	Y28	FB_A1_A<6>	OUT
FBA_D24	P34	FBA_CMD24	Y29	FB_A1_ABI_L	OUT
FBA_D25	P32	FBA_CMD25	W31	FB_A1_A<8>	OUT
FBA_D26	P31	FBA_CMD26	Y30	FB_A1_A<0>	OUT
FBA_D27	P33	FBA_CMD27	AA34	FB_A1_A<1>	OUT
FBA_D28	L31	FBA_CMD28	Y31	FB_A1_RAS_L	OUT
FBA_D29	L34	FBA_CMD29	Y34	FB_A1_RESET_L	OUT
FBA_D30	L32	FBA_CMD30	Y33	FB_A1_CKE_L	OUT
FBA_D31	L33	FBA_CMD31	V31	FB_A1_CAS_L	OUT
FBA_D32	AG28	FBA_CLK0	R30	FB_A0_CLK_P	OUT
FBA_D33	AF29	FBA_CLK0*	R31	FB_A0_CLK_N	OUT
FBA_D34	AG29	FBA_CLK1	AB31	FB_A1_CLK_P	OUT
FBA_D35	AF28	FBA_CLK1*	AC31	FB_A1_CLK_N	OUT
FBA_D36	AD30				
FBA_D37	AD29	FBA_DQM0	P30	FB_A0_DBI_L<0>	BI
FBA_D38	AC29	FBA_DQM1	F31	FB_A0_DBI_L<1>	BI
FBA_D39	AD28	FBA_DQM2	F34	FB_A0_DBI_L<2>	BI
FBA_D40	AJ29	FBA_DQM3	M32	FB_A0_DBI_L<3>	BI
FBA_D41	AK29	FBA_DQM4	AD31	FB_A1_DBI_L<0>	BI
FBA_D42	AJ30	FBA_DQM5	AL29	FB_A1_DBI_L<1>	BI
FBA_D43	AK28	FBA_DQM6	AM32	FB_A1_DBI_L<2>	BI
FBA_D44	AM29	FBA_DQM7	AF34	FB_A1_DBI_L<3>	BI
FBA_D45	AM30				
FBA_D46	AM31	FBA_DQS_RN0	M30	NC	
FBA_D47	AM30	FBA_DQS_RN1	H30	NC	
FBA_D48	AN31	FBA_DQS_RN2	E34	NC	
FBA_D49	AN32	FBA_DQS_RN3	M34	NC	
FBA_D50	AP30	FBA_DQS_RN4	AF30	NC	
FBA_D51	AP32	FBA_DQS_RN5	AH31	NC	
FBA_D52	AM33	FBA_DQS_RN6	AH34	NC	
FBA_D53	AL31	FBA_DQS_RN7	AF32	NC	
FBA_D54	AK33				
FBA_D55	AK32	FBA_DQS_WP0	M31	FB_A0_EDC<0>	IN
FBA_D56	AD34	FBA_DQS_WP1	G31	FB_A0_EDC<1>	IN
FBA_D57	AD32	FBA_DQS_WP2	E33	FB_A0_EDC<2>	IN
FBA_D58	AC30	FBA_DQS_WP3	M33	FB_A0_EDC<3>	IN
FBA_D59	AD33	FBA_DQS_WP4	AE31	FB_A1_EDC<0>	IN
FBA_D60	AF31	FBA_DQS_WP5	AK30	FB_A1_EDC<1>	IN
FBA_D61	AG34	FBA_DQS_WP6	AN33	FB_A1_EDC<2>	IN
FBA_D62	AG32	FBA_DQS_WP7	AF33	FB_A1_EDC<3>	IN
FBA_D63	AG33				
FBA_WCK01	K31	FB_DLL_AVDD	K27	PP1V05_GPU_FB_DLL_AVDD	
FBA_WCK01*	L30	FBA_PLL_AVDD	U27	PP1V05_GPU_FB_PLL_AVDD	
FBA_WCK23	H34	FBA_DEBUG	R28	GPU_FBA_DEBUG0	
FBA_WCK23*	J34	FBA_DEBUG	AC28	GPU_FBA_DEBUG1	
FBA_WCK45	AG30	FB_CAL_PD_VDDQ	J27	FB_CAL_PD_VDDQ	
FBA_WCK45*	AG31	FB_CAL_PU_GND	H27	FB_CAL_PU_GND	
FBA_WCK67	AJ34	FB_CAL_TERM_GND	H25	FB_CAL_TERM_GND	
FBA_WCK67*	AK34	FB_CLAMP	E1	FB_CLAMP	
FBA_WCKB01	J30	FBA_CMD_RFU	R32	NC	
FBA_WCKB01*	J31	FBA_CMD_RFU	AC32	NC	
FBA_WCKB23	J32				
FBA_WCKB23*	J33				
FBA_WCKB45	AH31				
FBA_WCKB45*	AJ31				
FBA_WCKB67	AJ32				
FBA_WCKB67*	AJ33				
		FB_VDDQ_SENSE	F1	SNS_GPUVDDQ_P	OUT
		FB_GND_SENSE	F2	SNS_GPUVDDQ_N	OUT

FB_A0_RESET_L
R8250 10K 1% 1/20W MF 201
FB_A1_RESET_L
R8251 10K 1% 1/20W MF 201

=PP1V35_GPU_S0_FB
R8252 10K 1% 1/20W MF 201
R8253 10K 1% 1/20W MF 201
FB_A0_CKE_L
FB_A1_CKE_L

=PP1V35_GPU_S0_FB
NOSTUFF R8258 1.33K 1% 1/20W MF 201 PLACE_NEAR=U8000.H26:9.6MM
FB_VREF
NOSTUFF R8259 1.33K 1% 1/20W MF 201
NOSTUFF C8260 0.1UF 10% 6.3V X5R 201
PLACE_NEAR=U8000.H26:9.6MM

FB VREF GEN (TEST ONLY)

NOSTUFF R8203 60.4 1% 1/20W MF 201
NOSTUFF R8202 60.4 1% 1/20W MF 201
R8270 100 5% 1/20W MF 201 NOSTUFF
R8271 100 5% 1/20W MF 201 NOSTUFF

R8201 60.4 1% 1/20W MF 201 PLACE_NEAR=U8000.H25:9.6MM
R8261 10K 1% 1/20W MF 201

PLACE CLOSE TO BGA

FB_CAL_PU_GND
R8204 40.2 1% 1/20W MF 201 PLACE_NEAR=U8000.H27:9.6MM
=PP1V35_GPU_S0_FB
R8205 40.2 1% 1/20W MF 201 PLACE_NEAR=U8000.J27:9.6MM
FB_CAL_PD_VDDQ

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MEM INTRERFACE B

FBB_D0	G9	FBB_CMD0	D13	FB_B0_CS_L	OUT
FBB_D1	E9	FBB_CMD1	E14	FB_B0_A<3>	OUT
FBB_D2	G8	FBB_CMD2	F14	FB_B0_A<2>	OUT
FBB_D3	F9	FBB_CMD3	A12	FB_B0_A<4>	OUT
FBB_D4	F11	FBB_CMD4	B12	FB_B0_A<5>	OUT
FBB_D5	G11	FBB_CMD5	C14	FB_B0_WE_L	OUT
FBB_D6	F12	FBB_CMD6	B14	FB_B0_A<7>	OUT
FBB_D7	G12	FBB_CMD7	G15	FB_B0_A<6>	OUT
FBB_D8	G6	FBB_CMD8	F15	FB_B0_ABI_L	OUT
FBB_D9	F5	FBB_CMD9	E15	FB_B0_A<8>	OUT
FBB_D10	E6	FBB_CMD10	D15	FB_B0_A<0>	OUT
FBB_D11	F6	FBB_CMD11	A14	FB_B0_A<1>	OUT
FBB_D12	F4	FBB_CMD12	D14	FB_B0_RAS_L	OUT
FBB_D13	G4	FBB_CMD13	A15	FB_B0_RESET_L	OUT
FBB_D14	E2	FBB_CMD14	B15	FB_B0_CKE_L	OUT
FBB_D15	F3	FBB_CMD15	C17	FB_B0_CAS_L	OUT
FBB_D16	C2	FBB_CMD16	D18	FB_B1_CS_L	OUT
FBB_D17	D4	FBB_CMD17	E18	FB_B1_A<3>	OUT
FBB_D18	D3	FBB_CMD18	F18	FB_B1_A<2>	OUT
FBB_D19	C1	FBB_CMD19	A20	FB_B1_A<4>	OUT
FBB_D20	B3	FBB_CMD20	B20	FB_B1_A<5>	OUT
FBB_D21	C4	FBB_CMD21	C18	FB_B1_WE_L	OUT
FBB_D22	B5	FBB_CMD22	B18	FB_B1_A<7>	OUT
FBB_D23	C5	FBB_CMD23	G18	FB_B1_A<6>	OUT
FBB_D24	A11	FBB_CMD24	G17	FB_B1_ABI_L	OUT
FBB_D25	C11	FBB_CMD25	F17	FB_B1_A<8>	OUT
FBB_D26	D11	FBB_CMD26	D16	FB_B1_A<0>	OUT
FBB_D27	B11	FBB_CMD27	A18	FB_B1_A<1>	OUT
FBB_D28	D8	FBB_CMD28	D17	FB_B1_RAS_L	OUT
FBB_D29	A8	FBB_CMD29	A17	FB_B1_RESET_L	OUT
FBB_D30	C8	FBB_CMD30	B17	FB_B1_CKE_L	OUT
FBB_D31	B8	FBB_CMD31	E17	FB_B1_CAS_L	OUT
FBB_D32	F24	FBB_CLK0	D12	FB_B0_CLK_P	OUT
FBB_D33	G23	FBB_CLK0*	E12	FB_B0_CLK_N	OUT
FBB_D34	E24	FBB_CLK1	E20	FB_B1_CLK_P	OUT
FBB_D35	G24	FBB_CLK1*	F20	FB_B1_CLK_N	OUT
FBB_D36	D21				
FBB_D37	E21	FBB_DQM0	E11	FB_B0_DBI_L<0>	BI
FBB_D38	G21	FBB_DQM1	E3	FB_B0_DBI_L<1>	BI
FBB_D39	F21	FBB_DQM2	A3	FB_B0_DBI_L<2>	BI
FBB_D40	G27	FBB_DQM3	C9	FB_B0_DBI_L<3>	BI
FBB_D41	D27	FBB_DQM4	F23	FB_B1_DBI_L<0>	BI
FBB_D42	G26	FBB_DQM5	F27	FB_B1_DBI_L<1>	BI
FBB_D43	E27	FBB_DQM6	C30	FB_B1_DBI_L<2>	BI
FBB_D44	E29	FBB_DQM7	A24	FB_B1_DBI_L<3>	BI
FBB_D45	F29				
FBB_D46	E30	FBB_DQS_RN0	D9	NC	
FBB_D47	D30	FBB_DQS_RN1	E4	NC	
FBB_D48	A32	FBB_DQS_RN2	B2	NC	
FBB_D49	C31	FBB_DQS_RN3	A9	NC	
FBB_D50	C32	FBB_DQS_RN4	D22	NC	
FBB_D51	B32	FBB_DQS_RN5	D28	NC	
FBB_D52	D29	FBB_DQS_RN6	A30	NC	
FBB_D53	A29	FBB_DQS_RN7	B23	NC	
FBB_D54	C29				
FBB_D55	B29	FBB_DQS_WP0	D10	FB_B0_EDC<0>	IN
FBB_D56	B21	FBB_DQS_WP1	D5	FB_B0_EDC<1>	IN
FBB_D57	C23	FBB_DQS_WP2	C3	FB_B0_EDC<2>	IN
FBB_D58	A21	FBB_DQS_WP3	B9	FB_B0_EDC<3>	IN
FBB_D59	C21	FBB_DQS_WP4	E23	FB_B1_EDC<0>	IN
FBB_D60	B24	FBB_DQS_WP5	E28	FB_B1_EDC<1>	IN
FBB_D61	C24	FBB_DQS_WP6	B30	FB_B1_EDC<2>	IN
FBB_D62	B26	FBB_DQS_WP7	A23	FB_B1_EDC<3>	IN
FBB_D63	C26				
FBB_WCK01	F8	FBB_PLL_AVDD	H17	PP1V05_GPU_FB_PLL_AVDD	
FBB_WCK01*	E8	FBB_DEBUG0	G14	GPU_FBB_DEBUG0	
FBB_WCK23	A5	FBB_DEBUG1	G20	GPU_FBB_DEBUG1	
FBB_WCK23*	A6	FB_VREF	H26	FB_VREF	
FBB_WCK45	D24	FBB_CMD_RFU0	C12	NC	
FBB_WCK45*	D25	FBB_CMD_RFU1	C20	NC	
FBB_WCK67	B27				
FBB_WCK67*	C27				
FBB_WCKB01	D6				
FBB_WCKB01*	D7				
FBB_WCKB23	C6				
FBB_WCKB23*	B6				
FBB_WCKB45	F26				
FBB_WCKB45*	E26				
FBB_WCKB67	A26				
FBB_WCKB67*	A27				

L8201
30-OHM-25%-5A-0.01-OHM
=PP1V05_GPU_PEX_IOVDD
CRITICAL 0603
ESR = 0.050OHM
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
PP1V05_GPU_FB_PLL_AVDD
C8201 22UF 20% 6V X5R 402
C8202 10UF 20% 6.3V X5R 0201
C8203 0.1UF 10% 16V X7R-CERM 402
C8204 0.1UF 10% 16V X7R-CERM 402

L8202
30-OHM-25%-5A-0.01-OHM
=PP1V05_GPU_PEX_IOVDD
CRITICAL 0603
ESR = 0.050OHM
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
PP1V05_GPU_FB_DLL_AVDD
C8208 22UF 20% 6V X5R 402
C8209 1UF 20% 6.3V X5R 0201
C8205 0.1UF 10% 16V X7R-CERM 402

FB PLL & DLL VDD

FB_B0_RESET_L
R8254 10K 1% 1/20W MF 201
FB_B1_RESET_L
R8255 10K 1% 1/20W MF 201

=PP1V35_GPU_S0_FB
R8256 10K 1% 1/20W MF 201
R8257 10K 1% 1/20W MF 201
FB_B0_CKE_L
FB_B1_CKE_L

C8206 1UF 20% 6.3V X5R 0201
C8207 0.1UF 10% 6.3V X5R 201

=PP1V35_GPU_S0_FB
NOSTUFF R8206 60.4 1% 1/20W MF 201
NOSTUFF R8207 60.4 1% 1/20W MF 201
GPU_FBB_DEBUG0
GPU_FBB_DEBUG1

MEM VREFC & VREFD SWITCH

FB_SW_LEG
CRITICAL
Q8265
SSM3K15AMFVAPE
VESM
GPU_ALT_VREF
R8260 10K 5% 1/20W MF 201

Page Notes

Power aliases required by this page:
- +PP1V35_GPU_S0_FB
- +PP1V05_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

SYNC MASTER=D7 TONY	SYNC DATE=01/10/2012
PAGE TITLE: KEPLER FRAME BUFFER I/F	
Apple Inc.	DRAWING NUMBER: 051-9509 SIZE: D
	REVISION: 4.2.0
	BRANCH:
	PAGE: 82 OF 113
	SHEET: 73 OF 100

GPU VDDQ SUPPLY

VOUT = 1.5V / 1.35V

10 A MAX OUTPUT

F = ??? KHZ

GPIO_16	VID 1	VID 0	GPU VDDQ
	0	0	1.5 V
	1	0	1.35 V

Vout = 0.5 * (1 + Ra / Rb)

GPU 1V05 SUPPLY

VOUT = 1.05V

3.43 A MAX OUTPUT

F = 500 KHZ

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
110S0568	1	RES,MF,3.32 OHM,1/10W,1,603,LF	R8311	CRITICAL	

Vout = 0.5V * (1 + Ra / Rb)

SYNC_MASTER=D7_NICK SYNC_DATE=01/03/2012

PAGE TITLE

1V05 GPU POWER SUPPLY

Apple Inc.

DRAWING NUMBER 051-9509 SIZE D

REVISION 4.2.0

BRANCH

PAGE 83 OF 113

SHEET 74 OF 100

Page Notes

Power aliases required by this page:

- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

This memory device is in Mirrored Mode.

CK TERMINATION - A0

CK TERMINATION - A1

PLACE CLOSE TO U8400

PLACE CLOSE TO U8450

OMIT_TABLE

U8400
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(1 OF 2)

U8400
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(2 OF 2)

U8450
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(1 OF 2)

U8450
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(2 OF 2)

SYNC MASTER=D7 TONY	SYNC DATE=12/13/2011
PAGE TITLE: GDDR5 Frame Buffer A	
Apple Inc.	DRAWING NUMBER: 051-9509 SIZE: D
	REVISION: 4.2.0
	BRANCH:
	PAGE: 84 OF 113
	SHEET: 75 OF 100

Page Notes

Power aliases required by this page:

- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

This memory device is in Mirrored Mode.

CK TERMINATION - B0

CK TERMINATION - B1

U8500
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(1 OF 2)

U8500
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(2 OF 2)

U8550
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(1 OF 2)

U8550
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(2 OF 2)

OMIT_TABLE

PLACE CLOSE TO U8500

PLACE CLOSE TO U8550

SYNC_MASTER=D7_TONY	SYNC_DATE=12/13/2011
PAGE TITLE	GDDR5 Frame Buffer B
Apple Inc.	DRAWING NUMBER 051-9509 SIZE D
	REVISION 4.2.0
	BRANCH
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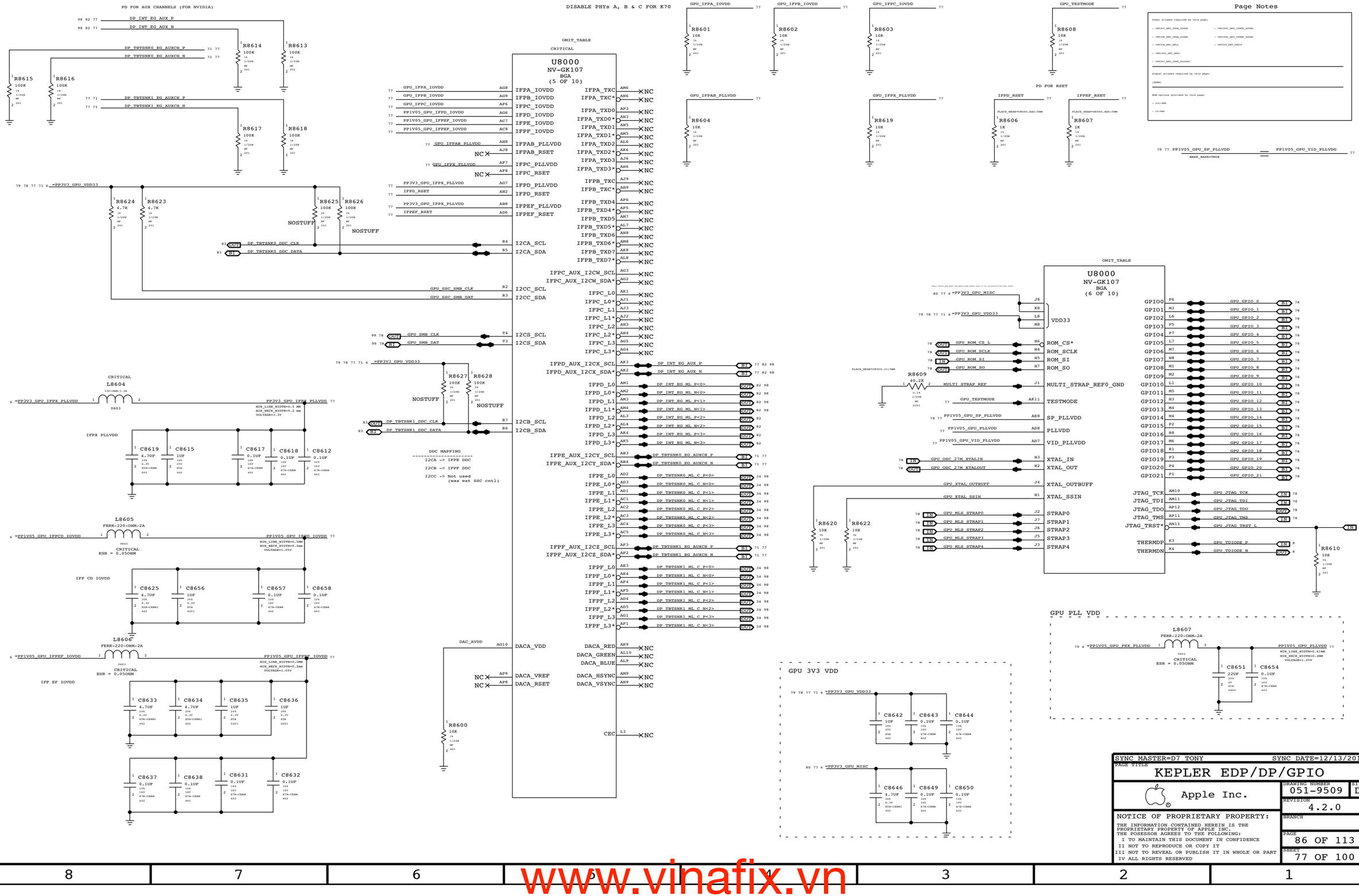

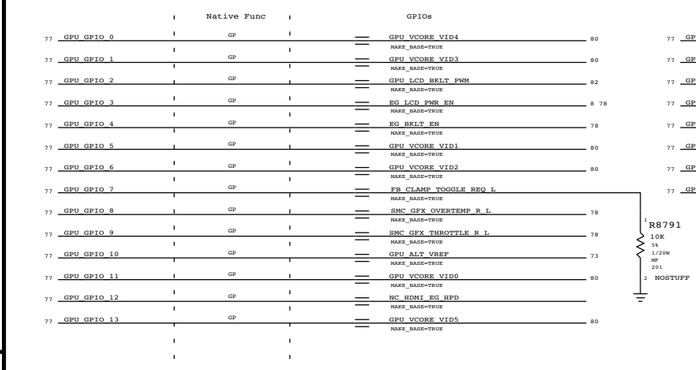

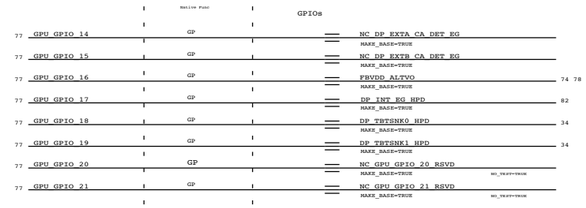

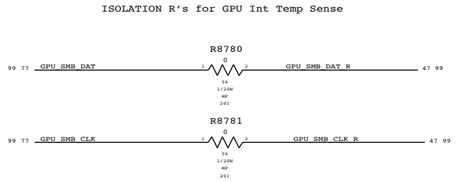

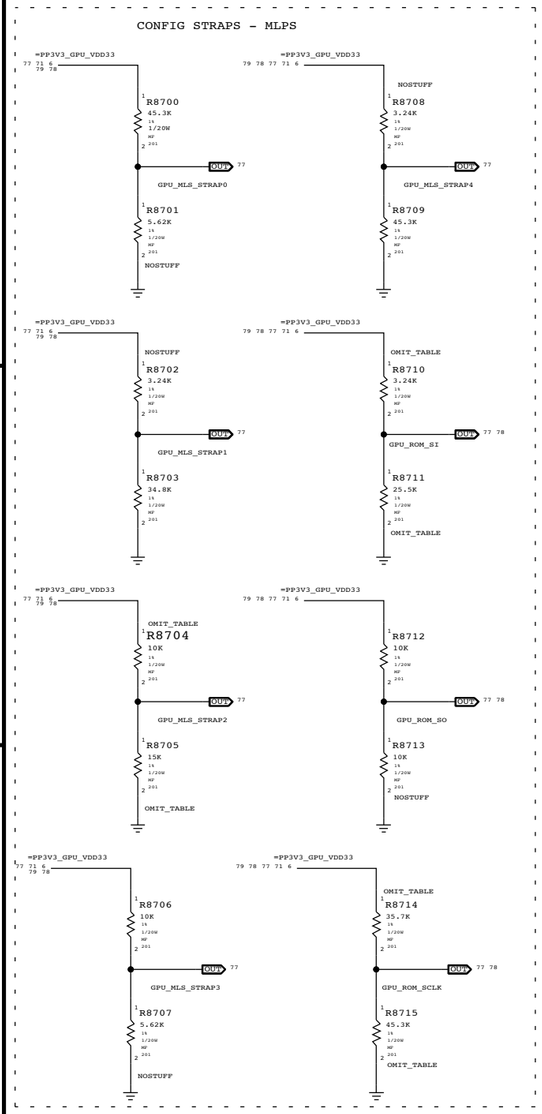

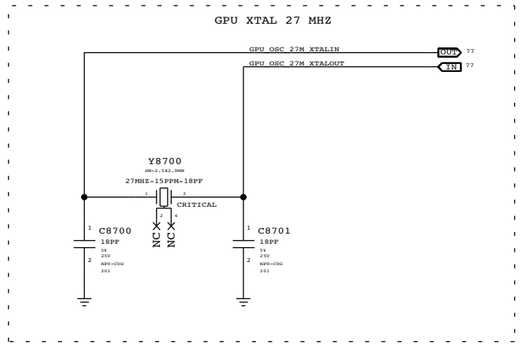

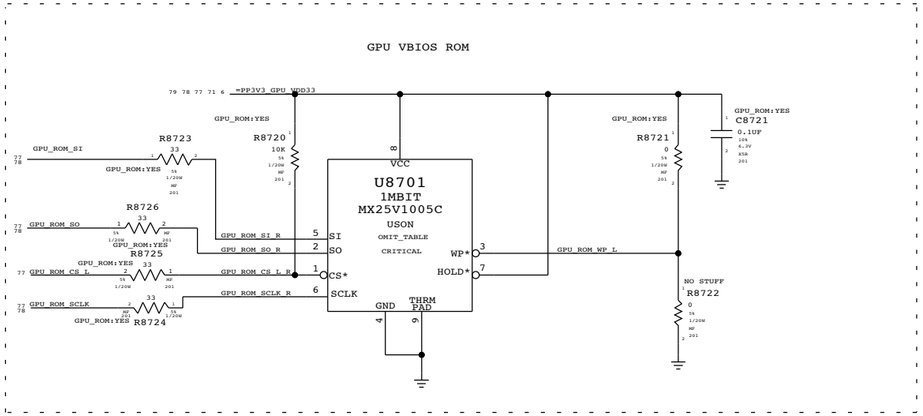

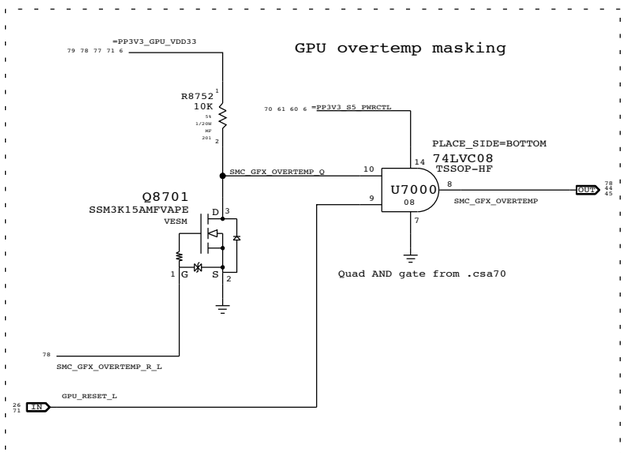

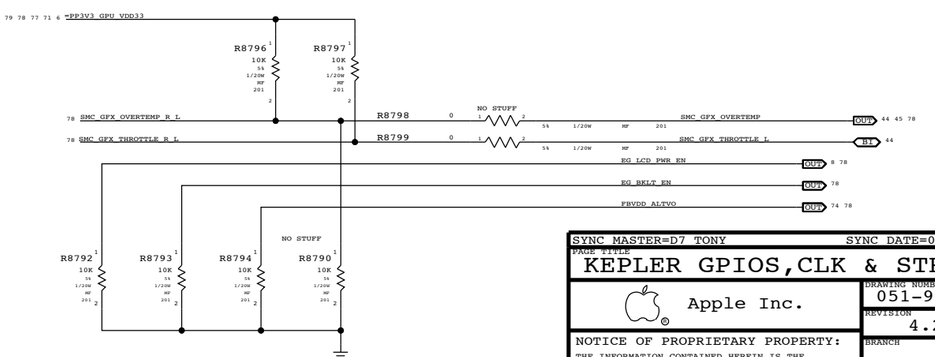

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-3824	1	RES,MF,NOSTUFF,1,1/20W,0201	R8704	CRITICAL	GPU:107GTX
118S0409	1	RES,MF,4.99k ,1,1/20W,0201	R8704	CRITICAL	GS
998-3824	1	RES,MF,NOSTUFF,1,1/20W,0201	R8704	CRITICAL	GPU:107EGE
118S0280	1	RES,MF,30.1k ,1,1/20W,0201	R8705	CRITICAL	GPU:107GTX
998-3824	1	RES,MF,NOSTUFF,1,1/20W,0201	R8705	CRITICAL	GS
118S0409	1	RES,MF,4.99k ,1,1/20W,0201	R8705	CRITICAL	GPU:107EGE
998-3824	1	RES,MF,NOSTUFF,1,1/20W,0201	R8710	CRITICAL	FB:BOTH_SAMSUNG
998-3824	1	RES,MF,NOSTUFF,1,1/20W,0201	R8710	CRITICAL	FB:BOTH_HYNIX
998-3824	1	RES,MF,NOSTUFF,1,1/20W,0201	R8710	CRITICAL	FB:CH1_SAMSUNG
998-3824	1	RES,MF,NOSTUFF,1,1/20W,0201	R8710	CRITICAL	FB:CH2_SAMSUNG
998-3824	1	RES,MF,NOSTUFF,1,1/20W,0201	R8710	CRITICAL	FB:CH1_HYNIX
998-3824	1	RES,MF,NOSTUFF,1,1/20W,0201	R8710	CRITICAL	FB:CH2_HYNIX
118S0175	1	RES,MF,20.0k ,1,1/20W,0201	R8711	CRITICAL	FB:BOTH_SAMSUNG
118S0105	1	RES,MF,15.0k ,1,1/20W,0201	R8711	CRITICAL	FB:BOTH_HYNIX
118S0013	1	RES,MF,10.0k ,1,1/20W,0201	R8711	CRITICAL	FB:CH1_SAMSUNG
118S0013	1	RES,MF,10.0k ,1,1/20W,0201	R8711	CRITICAL	FB:CH2_SAMSUNG
118S0230	1	RES,MF,24.9k ,1,1/20W,0201	R8711	CRITICAL	FB:CH1_HYNIX
118S0230	1	RES,MF,24.9k ,1,1/20W,0201	R8711	CRITICAL	FB:CH2_HYNIX
118S0409	1	RES,MF,4.99k ,1,1/20W,0201	R8714	CRITICAL	GPU:107GTX
118S0409	1	RES,MF,4.99k ,1,1/20W,0201	R8714	CRITICAL	GS
998-3824	1	RES,MF,NOSTUFF,1,1/20W,0201	R8714	CRITICAL	GPU:107EGE
998-3824	1	RES,MF,NOSTUFF,1,1/20W,0201	R8715	CRITICAL	GPU:107GTX
998-3824	1	RES,MF,NOSTUFF,1,1/20W,0201	R8715	CRITICAL	GS
118S0105	1	RES,MF,15.0k ,1,1/20W,0201	R8715	CRITICAL	GPU:107EGE

SYNC_MASTER=D7 TONY SYNC_DATE=01/10/2012

PAGE TITLE
KEPLER GPIOS,CLK & STRAPS

Apple Inc.

DRAWING NUMBER 051-9509 SIZE D
REVISION 4.2.0
BRANCH
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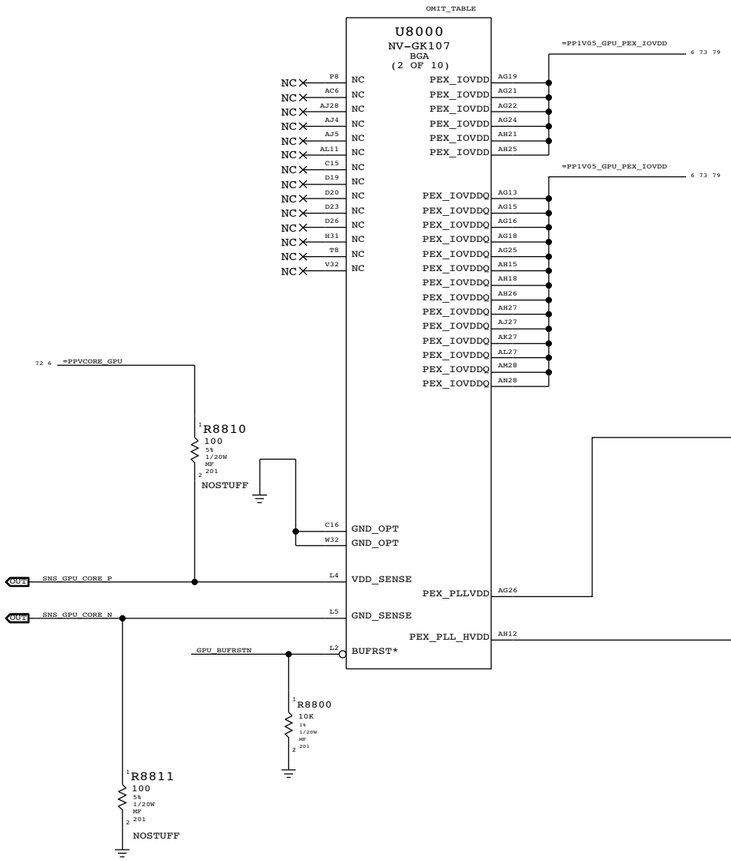

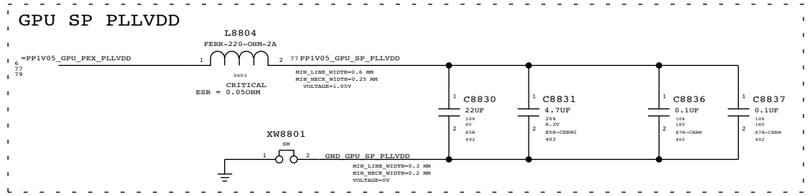

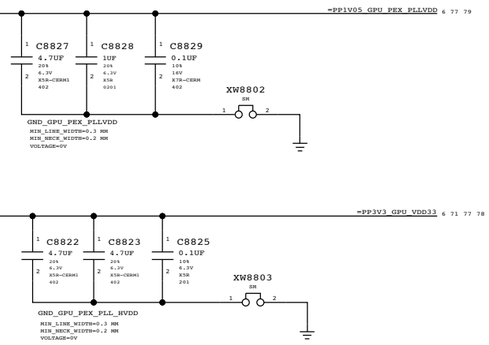

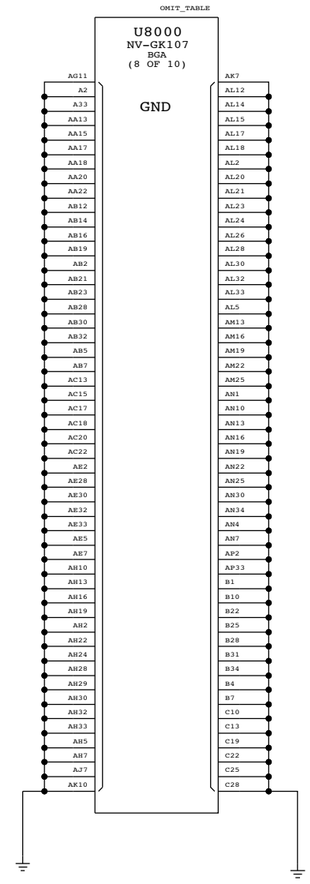

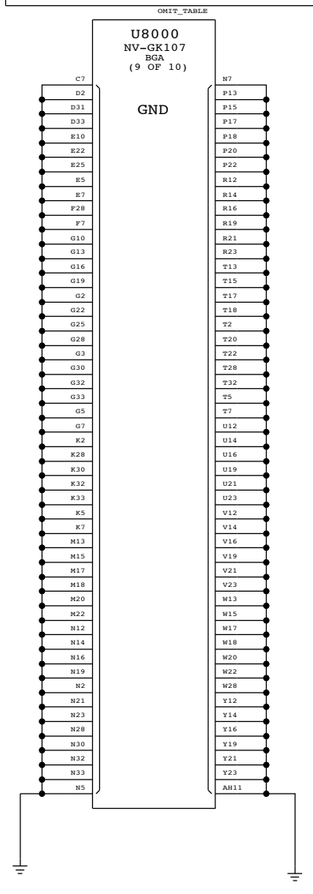

Page Notes

Power aliases required by this page:

- =PP3V3_GPU_VDD33
- =PP1V05_GPU_PEX_IOVDD
- =PP1V05_GPU_PEX_PLLVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

SYNC MASTER=D7 TONY	SYNC DATE=01/10/2012
PAGE TITLE: KEPLER PEX PWR/GNDS	
Apple Inc.	DRAWING NUMBER 051-9509 SIZE D
	REVISION 4.2.0
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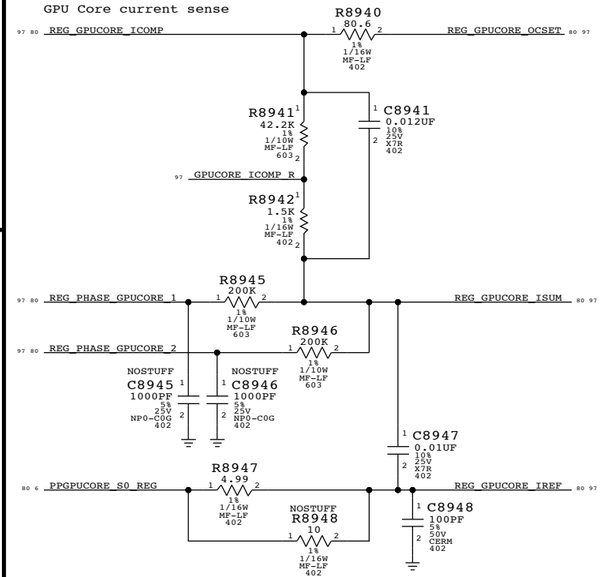
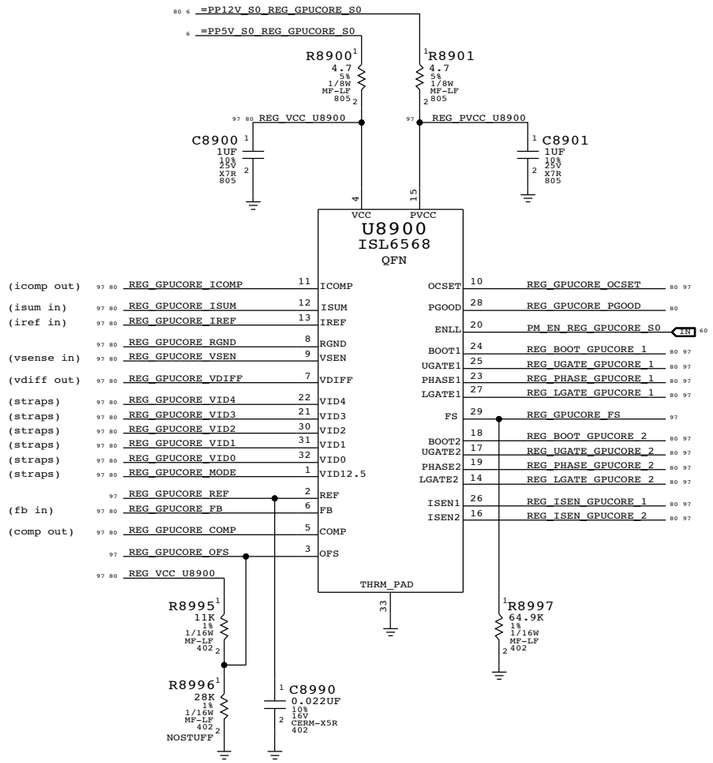
GPU Core S0 Regulator

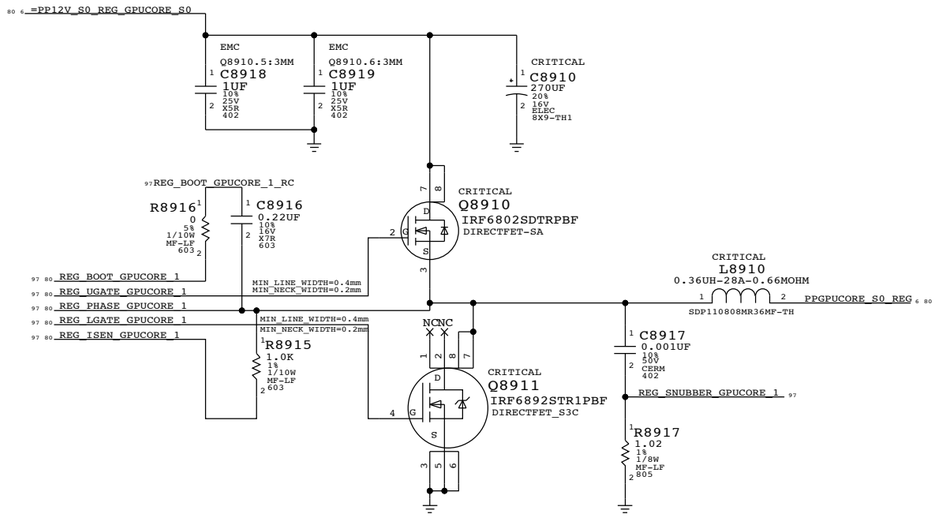
Max avg current: ? A (design)/? A (budget)
Max peak current: ? A (design)/? A (budget)
OC trip point: ? A (nom)/? A (min)
Switching freq: 290 kHz

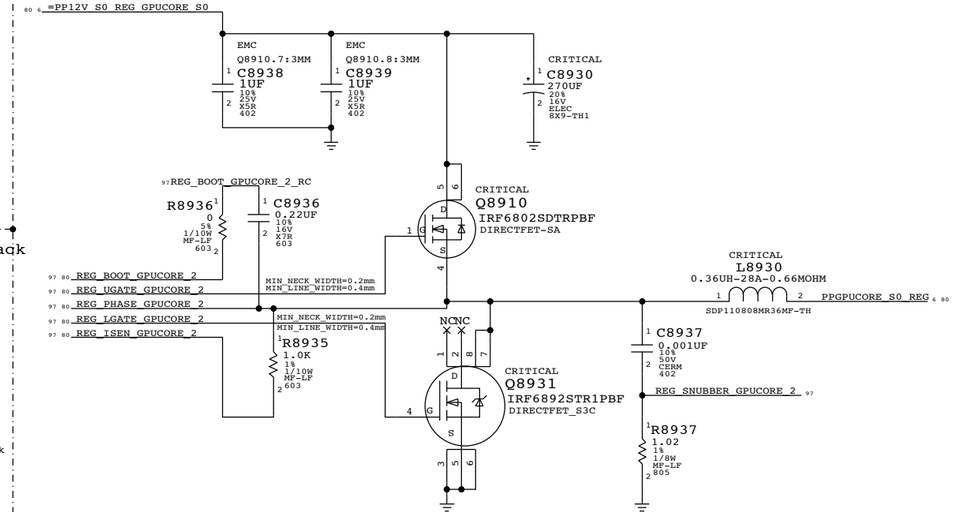
GPU Core current sense



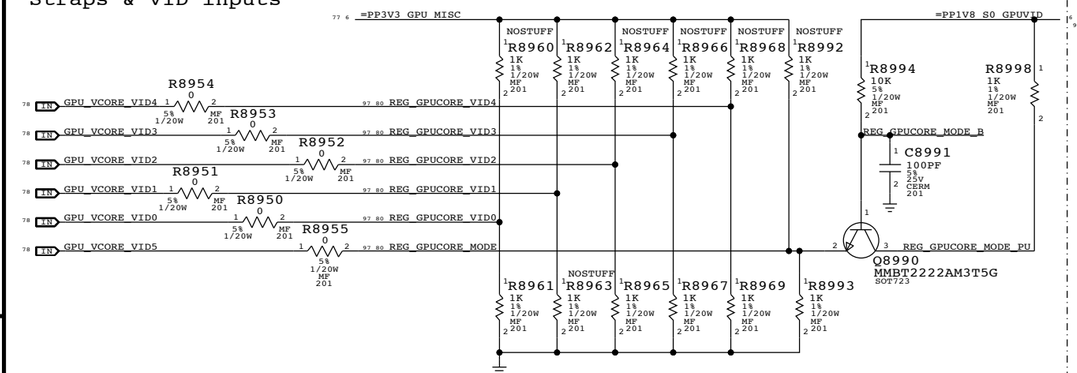


GPU Core Phases

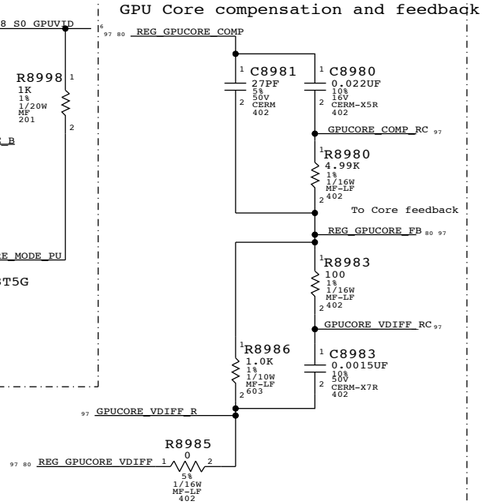




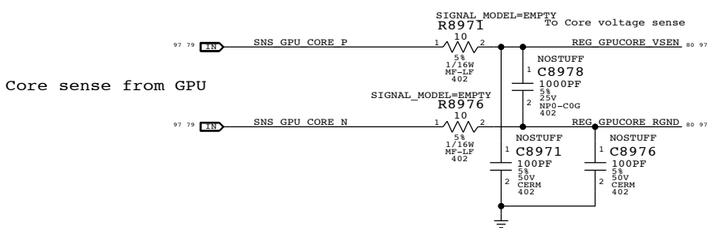
Straps & VID inputs



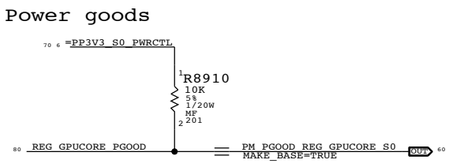
GPU Core compensation and feedback



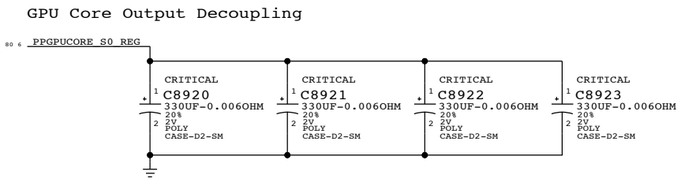
GPU Core voltage sense input



Power goods



GPU Core Output Decoupling



SYNC_MASTER=D7_NICK SYNC_DATE=01/03/2012

PAGE TITLE: VReg GPU Core

Apple Inc.

DRAWING NUMBER: 051-9509 SIZE: D
REVISION: 4.2.0
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PAGE: 89 OF 113
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Internal DP Connector

518S0829

CRITICAL

J9100
20525-130E-01
F-RT-SM

L9100
FERR-250-OHM
SM

=PP12V_S0_LCD → PP12V_LCD
VOLTAGE=12V
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm

C9120 10UF 10% 16V X5R-CERM 0805

C9101 0.001UF 20% 50V CERM 402

Display TCon Master
- SMB_DP_TCON_SDA (94 47) BI
- SMB_DP_TCON_SCL (94 47) OUT

Display TCon Slave
- SMB_DP_TCON_SLA_SDA (47) BI
- SMB_DP_TCON_SLA_SCL (47) IN
- DP_INT_SPDIF_AUDIO (98 52) OUT
- DP_INTPNL_HPD (82) OUT
- DP_INTPNL_AUX_N (98 82) BI
- DP_INTPNL_AUX_P (98 82) BI
- DP_INTPNL_ML_P<0> (98 82) IN
- DP_INTPNL_ML_N<0> (98 82) IN
- DP_INTPNL_ML_P<1> (98 82) IN
- DP_INTPNL_ML_N<1> (98 82) IN
- VIDEO_ON (81) OUT
- BKLT_VSYNC (86) OUT

Backlight Control

U9000 output Y2 is a non-inverted, delayed version of input A
The delay applies only on a L->H transition on A. This guarantees video is valid before the backlight is enabled.
On a H->L transition of A, Y2 follows with standard logic propagation delay. This ensures the backlight is off immediately after loss of video
Y1 is simply an inverted version of A, with no delay

=PP3V3_S0_DP (83 47 6)

C9106 0.1UF 20% 10V CERM 402

U9100
SN1105002
SC70

VCC
VIDEO_ON (81) IN → A
NC → NCX
Y1 → VIDEO_ON_L (OUT) → To Diag LED
Y2 → BKLT_EN (OUT) → To BLC
GND
CRITICAL

SYNC_MASTER=K70_MLB SYNC_DATE=11/30/2011

PAGE TITLE
Internal DP Support

Apple Inc.

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TP to DP aliases

34 IN TP_DP_TBTSRC_ML_CP<0> — DP_TBTSRC_ML_P<0> 82 98 (MAKE_BASE=TRUE)
34 IN TP_DP_TBTSRC_ML_CN<0> — DP_TBTSRC_ML_N<0> 82 98 (MAKE_BASE=TRUE)
34 IN TP_DP_TBTSRC_ML_CP<1> — DP_TBTSRC_ML_P<1> 82 98 (MAKE_BASE=TRUE)
34 IN TP_DP_TBTSRC_ML_CN<1> — DP_TBTSRC_ML_N<1> 82 98 (MAKE_BASE=TRUE)
34 BI TP_DP_TBTSRC_AUXCH_CP — DP_TBTSRC_AUXCH_P 82 98 (MAKE_BASE=TRUE)
34 BI TP_DP_TBTSRC_AUXCH_CN — DP_TBTSRC_AUXCH_N 82 98 (MAKE_BASE=TRUE)

NC aliases

34 IN TP_DP_TBTSRC_ML_CP<2> — NC_DP_TBTSRC_ML_P<2> (NO_TEST=TRUE MAKE_BASE=TRUE)
34 IN TP_DP_TBTSRC_ML_CN<2> — NC_DP_TBTSRC_ML_N<2> (NO_TEST=TRUE MAKE_BASE=TRUE)
34 IN TP_DP_TBTSRC_ML_CP<3> — NC_DP_TBTSRC_ML_P<3> (NO_TEST=TRUE MAKE_BASE=TRUE)
34 IN TP_DP_TBTSRC_ML_CN<3> — NC_DP_TBTSRC_ML_N<3> (NO_TEST=TRUE MAKE_BASE=TRUE)
77 IN DP_INT_EG_ML_P<2> — NC_DP_INT_EG_ML_P<2> (NO_TEST=TRUE MAKE_BASE=TRUE)
77 IN DP_INT_EG_ML_N<2> — NC_DP_INT_EG_ML_N<2> (NO_TEST=TRUE MAKE_BASE=TRUE)
77 IN DP_INT_EG_ML_P<3> — NC_DP_INT_EG_ML_P<3> (NO_TEST=TRUE MAKE_BASE=TRUE)
77 IN DP_INT_EG_ML_N<3> — NC_DP_INT_EG_ML_N<3> (NO_TEST=TRUE MAKE_BASE=TRUE)

=PP3V3_S0_INTDPMUX 6 82

C9268 0.1UF 10% 6.3V X5R 201
C9269 0.1UF 10% 6.3V X5R 201

U9200 PI3VEDP212 TQFN CRITICAL
VDD pins 29 20 16 12 9 5

98 77 IN DP_INT_EG_ML_P<0> → 31 D0+A
98 77 IN DP_INT_EG_ML_N<0> → 30 D0-A
98 77 IN DP_INT_EG_ML_P<1> → 27 D1+A
98 77 IN DP_INT_EG_ML_N<1> → 26 D1-A

98 77 BI DP_INT_EG_AUX_P — C9208 0.1UF 10% 16V X5R 402 — 98 DP_INT_EG_AUX_C_P → 19 AUX+A
98 77 BI DP_INT_EG_AUX_N — C9209 0.1UF 10% 16V X5R 402 — 98 DP_INT_EG_AUX_C_N → 18 AUX-A
82 78 OUT DP_INT_EG_HPD → 17 HPD_A

98 82 DP_TBTSRC_ML_C_P<0> → 25 D0+B
98 82 DP_TBTSRC_ML_C_N<0> → 24 D0-B
98 82 DP_TBTSRC_ML_C_P<1> → 23 D1+B
98 82 DP_TBTSRC_ML_C_N<1> → 22 D1-B

98 82 BI DP_TBTSRC_AUXCH_P — C9210 0.1UF 10% 16V X5R 402 — 98 DP_TBTSRC_AUX_C_P → 15 AUX+B
98 82 BI DP_TBTSRC_AUXCH_N — C9211 0.1UF 10% 16V X5R 402 — 98 DP_TBTSRC_AUX_C_N → 14 AUX-B
34 OUT DP_TBTSRC_HPD → 13 HPD_B
PD is on the CR page

82 58 21 IN DP_GPU_TBT_SEL → 10 SEL, 32 AUX_SEL, 11 HPD_SEL

R9201 10K 5% 1/20W MF 201 — THMPAD_GND (pins 33 34 35)

82 78 DP_INT_EG_HPD — R9200 100K 5% 1/20W MF 201

D0+ 1 98 DP_INTPNL_ML_C_P<0> — C9200 0.1UF 10% 16V X5R 402 — DP_INTPNL_ML_P<0> OUT 81 98
D0- 2 98 DP_INTPNL_ML_C_N<0> — C9201 0.1UF 10% 16V X5R 402 — DP_INTPNL_ML_N<0> OUT 81 98
D1+ 4 98 DP_INTPNL_ML_C_P<1> — C9202 0.1UF 10% 16V X5R 402 — DP_INTPNL_ML_P<1> OUT 81 98
D1- 5 98 DP_INTPNL_ML_C_N<1> — C9203 0.1UF 10% 16V X5R 402 — DP_INTPNL_ML_N<1> OUT 81 98

AUX+ 6 DP_INTPNL_AUX_P BI 81 98
AUX- 7 DP_INTPNL_AUX_N BI 81 98
HPD 8 DP_INTPNL_HPD IN 81

R9202 100K 5% 1/20W MF 201
R9203 100K 5% 1/20W MF 201 — =PP3V3_S0_INTDPMUX 6 82

98 82 IN DP_TBTSRC_ML_P<0> — C9212 0.1UF 10% 16V X5R 402 — DP_TBTSRC_ML_C_P<0> 82 98
98 82 IN DP_TBTSRC_ML_N<0> — C9213 0.1UF 10% 16V X5R 402 — DP_TBTSRC_ML_C_N<0> 82 98
98 82 IN DP_TBTSRC_ML_P<1> — C9214 0.1UF 10% 16V X5R 402 — DP_TBTSRC_ML_C_P<1> 82 98
98 82 IN DP_TBTSRC_ML_N<1> — C9215 0.1UF 10% 16V X5R 402 — DP_TBTSRC_ML_C_N<1> 82 98

R9212 2.7K 5% 1/20W MF 201
R9213 2.7K 5% 1/20W MF 201
R9214 2.7K 5% 1/20W MF 201
R9215 2.7K 5% 1/20W MF 201

82 6 =PP3V3_S0_INTDPMUX

BKLT_PWM C9270 0.1uF 10% 16V X5R 402

BKLT_PWM U9220 74LVC1G157 SOT487
VCC pin 5, GND pin 2, S pin 6, I0 pin 3, I1 pin 1, Y pin 4

45 IN BDV_BKL_PWM → I1
78 IN GPU_LCD_BKLT_PWM → I0
82 58 21 IN DP_GPU_TBT_SEL → S
Y → 85 85 LCD_BKLT_PWM

BKLT_PWM R9222 47 5% 1/16W MF-LP 402 — LCD_BKLT_FILT

BKLT_PWM L9201 FERR-220-OHM 0402 — LCD_BKLT_PWM OUT 82 86

SYNC_MASTER=D7_NICK	SYNC_DATE=12/14/2011
PAGE TITLE: Internal DP MUXing	
Apple Inc.	DRAWING NUMBER: 051-9509 SIZE: D
	REVISION: 4.2.0
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	PAGE: 92 OF 113
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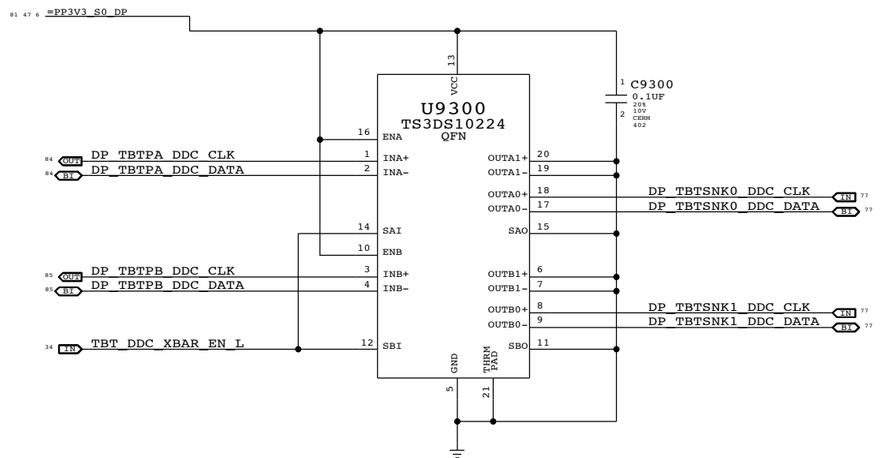
Dual-Port Host DDC Crossbar



SYNC_MASTER=D7_DOUG SYNC_DATE=12/15/2011

PAGE TITLE

TBT DDC Crossbar

Apple Inc.

DRAWING NUMBER 051-9509 SIZE D

REVISION 4.2.0

BRANCH

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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S, 9-12.6V, 7.5-11.7W)

=PP3V3_S4_TBTAPWRSW
CRITICAL C9487 100UF 20% 6.3V POLY-TANT CASE-B2-SM
CRITICAL C9480 22UF 20% 6.3V X5R-CERM-1 603
C9481 0.1UF 20% 10V CERM 402
=PPHV_SW_TBTAPWRSW 18.9V Max
C9415 4.7UF 10% 25V X5R-CERM 0603
C9410 0.1UF 10% 50V X7R 603-1
CRITICAL U9410 CD3210A0RGP QFN
V3P3 V3P3OUT NC
VHV OUT PPHV_SW_TBTAPWR
MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=15V
C9411 0.1UF 10% 50V X7R 603-1
RSVD RSVD
=TBTAPWRSW_EN EN ISET_V3P3 TBTAPWRSW_ISET_V3P3
TBT_A_HV_EN HV_EN ISET_S0 TBTAPWRSW_ISET_S0
=TBT_S0_EN S0 ISET_S3 TBTAPWRSW_ISET_S3
GND THRM PAD
12V: See below
TBTHV:P15V
R9410 22.6K 1% 1/16W MF-LF 402
R9411 22.6K 1% 1/16W MF-LF 402
R9412 36.5K 1% 1/16W MF-LF 402
TBTAPWRSW_ISET_S3_R
TBTAPWRSW_ISET_S0_R
R9413 22.6K 1% 1/16W MF-LF 402
R9414 22.6K 1% 1/16W MF-LF 402
Two Rs in series required by CD3210 for single-fault protection(S0,S3 only)

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R9410,R9413		TBTHV:P12V
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R9411,R9414		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

NOTE: Polarity Swapped for layout!

DP_TBTPA_ML_C_P<3>
DP_TBTPA_ML_C_N<3>
C9478 0.22UF
C9479 0.22UF
TBT: Terminated
R9478 470K 5% 1/20W MF 201
R9479 470K 5% 1/20W MF 201

TBT_A_BIAS
R9498 2.2K 5% 1/20W MF 201
R9499 2.2K 5% 1/20W MF 201

NOTE: Polarity Swapped for layout!

DP_A_AUXCH_DDC_P
DP_A_AUXCH_DDC_N
C9498 30PF 5% 50V CERM 402
C9499 30PF 5% 50V CERM 402

TBT_A_HPD
TBT_A_CONFIG1_RC
TBT_A_CONFIG2_RC
R9452 1M 5% 1/20W MF 201
R9451 1M 5% 1/20W MF 201
C9494 330PF 10% 16V X7R 201
C9495 330PF 10% 16V X7R 201
R9441 100K 5% 1/20W MF 201

L9400 FERR-120-OHM-3A 0603
PP3V3R3HV_SW_TBTAPWR
MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=15V
C9400 0.01UF 10% 50V X7R 402
C9401 0.01UF 10% 50V X7R 402
TBTACONN_20_RC MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18V
R9401 12 5% 1/20W MF 201

TBT Dir DP Dir

R9494 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY
R9495 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY

CRITICAL
D9498 BAR90-02LRH TSLP-2-7
D9499 BAR90-02LRH TSLP-2-7
CRITICAL L9498 650NH-5%-0.430MA-0.52OHM 0603 SIGNAL_MODEL=EMPTY
CRITICAL L9499 650NH-5%-0.430MA-0.52OHM 0603 SIGNAL_MODEL=EMPTY

C9402 0.01UF 10% 25V X5R-CERM 0201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

=PP3V3_S4_TBT
C9420 0.1UF 10% 6.3V X5R 201
C9421 0.1UF 10% 6.3V X5R 201
R9427 10K 5% 1/20W MF 201
R9429 100K 5% 1/20W MF 201
VDD
CRITICAL U9420 CBTL05023 HVQFN
TBT_A_BIAS VOLTAGE=3.3V
C9425 0.1UF 10% 6.3V X5R 201

TBT_A_CIO_SEL
DP_AUXIO_EN
C9430 0.1UF 10% 6.3V X5R 201
C9431 0.1UF 10% 6.3V X5R 201
DP_TBTPA_AUXCH_C_N
DP_TBTPA_AUXCH_C_P
DP_TBTPA_AUXCH_N
DP_TBTPA_AUXCH_P
DP_TBTPA_DDC_DATA
DP_TBTPA_DDC_CLK
TBT_A_CONFIG1_BUF
C9432 0.22UF 20% 6.3V X5R 0201
C9433 0.22UF 20% 6.3V X5R 0201
DP_TBTPA_ML_C_P<1>
DP_TBTPA_ML_C_N<1>
DP_TBTPA_ML_P<1>
DP_TBTPA_ML_N<1>
TBT_A_LSTX
TBT_A_LSRX_UNBUF
TBT_A_DP_PWRDN
DP_TBTPA_HPD
BIASIN AUXIO_EN AUX- AUX+ DDC_DAT DDC_CLK CA_DETOUT DP+ DP- LSTX LSRX DP_PD HPDOUT
BIASOUT AUXIO- AUXIO+ CA_DET DPMLO+ DPMLO- HPD
DP_A_AUXCH_DDC_N
DP_A_AUXCH_DDC_P
TBT: RX_1 Bias Sink
TBT_A_CONFIG1_RC
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)
TBT_A_HPD
GND THMPAD
R9426 1M 5% 1/20W MF 201
R9428 100K 5% 1/20W MF 201

=PP3V3_S4_TBT
U9460 74AUP1T97 SOT891
TBT_A_LSRX
C9460 0.1UF 10% 16V X5R-CERM 0201

Thunderbolt Connector A

CRITICAL
SHLD
J9400 DUAL-MDP-K70
F-ANG-TH
PORT A
SHLD
514-0824

2	HPD	GND0	1
4	CONFIG1	ML_LANE0P	3
6	CONFIG2	ML_LANE0N	5
8	GND2	GND1	7
10	ML_LANE3P	ML_LANE1P	9
12	ML_LANE3N	ML_LANE1N	11
14	GND4	GND3	13
16	AUX_CHP	ML_LANE2P	15
18	AUX_CHN	ML_LANE2N	17
20	DP_PWR	RETURN	19

C9405 0.01UF 10% 25V X5R-CERM 0201
TBTACONN_1_C MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18.9V
(0-18.9V)
DP Dir TBT Dir
TBT_A_R2D_P<0>
TBT_A_R2D_N<0>
TBT: TX_0
C9406 0.01UF 10% 25V X5R-CERM 0201
TBTACONN_7_C MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18.9V
(0-18.9V)
TBT: LSX_R2P/P2R (P/N)
TBT_A_R2D_P<1>
TBT_A_R2D_N<1>
TBT: TX_1

GND_VOID=TRUE (Both C's)
C9470 0.22UF 20% 6.3V X5R 0201
C9471 0.22UF 20% 6.3V X5R 0201
TBT_A_R2D_C_P<0>
TBT_A_R2D_C_N<0>
R9470 470K 5% 1/20W MF 201
R9471 470K 5% 1/20W MF 201

NOTE: Polarity Swapped for layout!
C9472 0.22UF 20% 6.3V X5R 0201
C9473 0.22UF 20% 6.3V X5R 0201
TBT_A_R2D_C_N<1>
TBT_A_R2D_C_P<1>
R9472 470K 5% 1/20W MF 201
R9473 470K 5% 1/20W MF 201
470k R's for ESD protection on AC-coupled signals.

SYNC_MASTER=D7_DOUG SYNC_DATE=12/15/2011
PAGE TITLE: Thunderbolt Connector A
Apple Inc.
DRAWING NUMBER 051-9509 SIZE D
REVISION 4.2.0
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3.3V/HV Power MUX

V3P3 must be S4 to support wake from Thunderbolt devices.

=PP3V3_S4_TBTBPWRSW

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S, 9-12.6V, 7.5-11.7W)

=PPHV_SW_TBTBPWRSW
18.9V Max

U9610 CD3210A0RGP QFN

PPHV_SW_TBTBPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V

=TBTBPWRSW_EN
TBT_B_HV_EN
=TBT_S0_EN

TBTBPWRSW_ISET_V3P3
TBTBPWRSW_ISET_S0
TBTBPWRSW_ISET_S3
TBTBPWRSW_ISET_S3_R
TBTBPWRSW_ISET_S0_R

12V: See below

TBTHV:P15V

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R9610,R9613		TBTHV:P12V
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R9611,R9614		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

Two Rs in series required by CD3210 for single-fault protection(S0,S3 only)

=PP3V3_S4_TBT

U9620 CBTL05023 HVQFN

DP_TBTPB_AUXCH_C_N
DP_TBTPB_AUXCH_C_P
DP_TBTPB_AUXCH_N
DP_TBTPB_AUXCH_P
DP_TBTPB_DDC_DATA
DP_TBTPB_DDC_CLK
DP_TBTPB_ML_C_P<1>
DP_TBTPB_ML_C_N<1>
DP_TBTPB_ML_P<1>
DP_TBTPB_ML_N<1>
DP_TBTPB_HPD

TBT_B_CIO_SEL
DP_AUXIO_EN
TBT_B_CONFIG1_BUF
TBT_B_LSTX
TBT_B_LSRX_UNBUF
TBT_B_DP_PWRDN

TBT_B_BIAS
TBT_B_CONFIG1_RC
TBT_B_HPD
DP_B_AUXCH_DDC_N
DP_B_AUXCH_DDC_P
DP_B_LSX_ML_P<1>
DP_B_LSX_ML_N<1>

TBT: RX_1 Bias Sink
TBT: LSX_A_R2P/P2R (P/N)

U9660 74AUP1T97 SOT891

TBT_B_LSRX

Thunderbolt Connector B

L9600 FERR-120-OHM-3A
PP3V3R3HV_SW_TBTBPWR

TBTBCONN_20_RC
TBT Dir
DP Dir

TBT: Terminated

TBTBCONN_1_C
TBTBCONN_7_C
TBT: TX_0
TBT: LSX_R2P/P2R (P/N)
TBT: TX_1

J9400 DUAL-MDP-K70 F-ANG-TH
514-0824

TBT_B_R2D_C_P<0>
TBT_B_R2D_C_N<0>
TBT_B_R2D_P<0>
TBT_B_R2D_N<0>
TBT_B_R2D_C_P<1>
TBT_B_R2D_C_N<1>
TBT_B_R2D_P<1>
TBT_B_R2D_N<1>
TBT_B_D2R_C_P<0>
TBT_B_D2R_C_N<0>
TBT_B_D2R_P<0>
TBT_B_D2R_N<0>
TBT_B_D2R_C_P<1>
TBT_B_D2R_C_N<1>
TBT_B_D2R_P<1>
TBT_B_D2R_N<1>

NOTE: Polarity Swapped for Layout!

D9698 D9699 BAR90-02LRH
TBT_B_D2R1_AUXDDC_P
TBT_B_D2R1_AUXDDC_N

L9698 L9699 650NH-5%-0.430MA-0.52OHM

DP_B_AUXCH_DDC_P
DP_B_AUXCH_DDC_N

TBT_B_HPD
TBT_B_CONFIG1_RC
TBT_B_CONFIG2_RC

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

470k R's for ESD protection on AC-coupled signals.

SYNC MASTER=D7 DOUG	SYNC DATE=12/15/2011
PAGE TITLE	Thunderbolt Connector B
Apple Inc.	DRAWING NUMBER 051-9509 SIZE D
	REVISION 4.2.0
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0745	138S0743		BLC_CAP	BLC Ouput Cap

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S1592	152S1591		L9700	BLC Switch Inductor
371S0648	371S0694		D9700	BLC Switch Diode

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1054	376S1022		Q9700	BLC Switch FET

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1071	376S1073		ALL	Short Protection FET

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0845	376S1067		Q9702	BLC Inrush FET

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S3665	1	IC,LP8561,LED BKLT CTRLR,LLP24,80	U9700	CRITICAL	

SYNC_MASTER=D7_NICK SYNC_DATE=01/03/2012

PAGE TITLE: LCD Backlight Driver (LP8545)

Apple Inc.

DRAWING NUMBER: 051-9509 SIZE: D

REVISION: 4.2.0

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K70 Board Specific Physical and Spacing Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM	NO_TYPE,BGA	MM	16.2

General Physical Rule Definitions

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.1 MM	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
34_OHM_SE	*	Y	0.215 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
34_OHM_SE	TOP,BOTTOM	Y	0.215 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
39_OHM_SE	*	Y	0.170 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
39_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
42_OHM_SE	*	Y	0.145 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
42_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	*	Y	0.138 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	TOP,BOTTOM	Y	0.138 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	0.110 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
68_OHM_DIFF	*	Y	0.180 MM	0.085 MM	=STANDARD	0.140 MM	0.1 MM
68_OHM_DIFF	TOP,BOTTOM	Y	0.180 MM	0.085 MM	=STANDARD	0.140 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.135 MM	0.085 MM	=STANDARD	0.160 MM	0.1 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.135 MM	0.085 MM	=STANDARD	0.160 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.125 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.111 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.111 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.089 MM	0.085 MM	=STANDARD	0.220 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.085 MM	=STANDARD	0.220 MM	0.1 MM

General Spacing Definitions

Default

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

Fixed and Dielectric

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1X_DIELECTRIC	*	0.076 MM	?
1X_DIELECTRIC	TOP,BOTTOM	0.071 MM	?

BGA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=STANDARD	?

Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
GND_P2MM	*	=2:1_SPACING	1000
PWR_P2MM	*	=2:1_SPACING	1100

BGA Area Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM

Board Stack-up

Finished board thickness: 1.58 mm

	Top	Signal	0.5 oz (Cu plated)
		Prepreg	0.071 mm
	2	Plane	1 oz
		Prepreg	0.076 mm
	3	Signal	0.5 oz
		Prepreg	0.435 mm
	4	Plane	1 oz
		Core	0.127 mm
	5	Plane	1 oz
		Prepreg	0.435 mm
	6	Signal	0.5 oz
		Prepreg	0.076 mm
	2	Plane	1 oz
		Prepreg	0.071 mm
	Btm	Signal	0.5 oz (Cu plated)

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PAGE TITLE: K70 Rule Definitions

Apple Inc.

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DDR3

DDR3-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DDR_34S	*	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	=STANDARD	=STANDARD
DDR_39S	*	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=STANDARD	=STANDARD
DDR_42S	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=STANDARD	=STANDARD
DDR_42S_D	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	0.1016 MM	0.1016 MM
DDR_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
DDR_68D	*	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF

Minimum diff spacing is 4 mil
Table 3-5, Intel Doc# 473718

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
POWER_DDR_P4MM	*	Y	0.400 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER_DDR	*	POWER_DDR_P4MM
DDR_CLK_PHY	*	DDR_68D
DDR_CTRL_PHY	*	DDR_39S
DDR_CMD_PHY	*	DDR_34S
DDR_DQ_PHY	*	DDR_42S
DDR_DQS_PHY	*	DDR_42S_D

DDR3 Power-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
POWER_DDR	*	=2:1_SPACING	?

DDR3-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DDR_CLK_ISO	*	=5:1_SPACING	?
DDR_CTRL_ISO	*	=3.5:1_SPACING	?
DDR_CTRL2CTRL	*	=2.5:1_SPACING	?
DDR_CMD_ISO	*	=3.5:1_SPACING	?
DDR_CMD2CMD	*	=2:1_SPACING	?
DDR_DATA_ISO	*	=3:1_SPACING	?
DDR_DQ2DQ	*	=2:1_SPACING	900
DDR_DQ2DQS	*	=3:1_SPACING	?
DDR_BL2BL	*	=3:1_SPACING	?
DDR_CH2CH	*	=6.5:1_SPACING	?

Main Segment Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Table	Trace	Design	Iso	Design	Comments
3-2	4	(diff)	15	19.69	CLK trace spacing controlled by =68_OHM_DIFF
3-3	8	9.84	12	13.78	
3-4	6	7.87	12	13.78	
3-5	8.5	7.87	12	11.81	DQ or DQS to other signals not in the same bytelane (but not ch)
					DQ to DQ in the same bytelane of the same channel
			10	11.81	DQ to DQS in the same bytelane of the same channel
			12	11.81	DQ or DQS in different bytelanes of the same channel
			25	25.59	DQ or DQS in different channels
			-	25.59	DDR3 to any other signal not DDR3

Constraints

Clocks: CK[3:0], CK#[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CLK	*	*	DDR_CLK_ISO

Control: CS#[3:0], CKE[3:0], ODT[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CTRL	*	*	DDR_CTRL_ISO
DDR_CTRL	DDR_CTRL	*	DDR_CTRL2CTRL

Command: MA[15:0], RAS#, CAS#, WE# BS[2:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CMD	*	*	DDR_CMD_ISO
DDR_CMD	DDR_CMD	*	DDR_CMD2CMD

Data: DQS[7:0], DQS#[7:0], DQ[63:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	
DDR_A_DQ_BYTE*	*	*	DDR_DATA_ISO	
DDR_A_DQS*	*	*	DDR_DATA_ISO	
DDR_B_DQ_BYTE*	*	*	DDR_DATA_ISO	
DDR_B_DQS*	*	*	DDR_DATA_ISO	
DDR_*_DQ_BYTE*	=SAME	*	DDR_DQ2DQ	See Note (3)
DDR_A_DQ_BYTE*	DDR_A_DQS*	*	DDR_DQ2DQS	See Note (1)
DDR_A_DQ_BYTE*	DDR_A_DQ_BYTE*	*	DDR_BL2BL	See Note (3)
DDR_B_DQ_BYTE*	DDR_B_DQS*	*	DDR_DQ2DQS	See Note (1)
DDR_B_DQ_BYTE*	DDR_B_DQ_BYTE*	*	DDR_BL2BL	
DDR_A_*	DDR_B_*	*	DDR_CH2CH	See Note (2)

Note (1):
Deliberately set DQ to DQS spacing to 3:1 to avoid adding complexity to contraints, even though it can be less. Only one rule per channel is needed by trading off a little space.

Note (2):
Intel suggests 25 mil (0.65 mm) spacing for via to channel, and via to pad to two different channels. DDR3 draws about 20 mA per trace with edge rates in the 100s of ps. The main coupling mechanism is capacitive. A 0.65 mm spacing is used for power nets, which draw far more current (inductive coupling however). These rules are far too conservative. To meet these rules, the spacing must be applied to the net.

Note (3):
In order for the constraints DDR_*_DQ_BYTE* to =SAME to win out over DDR_{A,B}_DQ_BYTE* to DDR_{A,B}_DQ_BYTE* so that the small intra-bytelane spacing is used, the spacing rule DDR_DQ2DQ must have a weight greater than DDR_BL2BL.

DDR3

Electrical Contraint Set	Physical	Spacing		
Channel A				
T17 DDR_A_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_P<1..0>	12 29
T17 DDR_A_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_N<1..0>	12 29
T25 DDR_A_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_P<3..2>	8 12
T25 DDR_A_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_N<3..2>	8 12
T18 DDR_A_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CKE<1..0>	12 29
T18 DDR_A_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CS_L<1..0>	12 29
T18 DDR_A_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_ODT<1..0>	12 29
T24 DDR_A_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CKE<3..2>	8 12
T24 DDR_A_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CS_L<3..2>	8 12
T24 DDR_A_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_ODT<3..2>	8 12
T18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_A<15..0>	12 29
T18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_BA<2..0>	12 29
T18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_RAS_L	12 29
T18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_CAS_L	12 29
T18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_WE_L	12 29
T18 DDR_A_DQ_BYTE0	DDR_DQ_PHY	DDR_A_DQ_BYTE0	MEM_A_DQ<7..0>	12 31
T18 DDR_A_DQ_BYTE1	DDR_DQ_PHY	DDR_A_DQ_BYTE1	MEM_A_DQ<15..8>	12 31
T19 DDR_A_DQ_BYTE2	DDR_DQ_PHY	DDR_A_DQ_BYTE2	MEM_A_DQ<23..16>	12 31
T19 DDR_A_DQ_BYTE3	DDR_DQ_PHY	DDR_A_DQ_BYTE3	MEM_A_DQ<31..24>	12 31
T19 DDR_A_DQ_BYTE4	DDR_DQ_PHY	DDR_A_DQ_BYTE4	MEM_A_DQ<39..32>	12 31
T19 DDR_A_DQ_BYTE5	DDR_DQ_PHY	DDR_A_DQ_BYTE5	MEM_A_DQ<47..40>	12 31
T19 DDR_A_DQ_BYTE6	DDR_DQ_PHY	DDR_A_DQ_BYTE6	MEM_A_DQ<55..48>	12 31
T19 DDR_A_DQ_BYTE7	DDR_DQ_PHY	DDR_A_DQ_BYTE7	MEM_A_DQ<63..56>	12 31
T19 DDR_A_DQS0	DDR_DQS_PHY	DDR_A_DQS0	MEM_A_DQS_P<0>	12 31
T19 DDR_A_DQS0	DDR_DQS_PHY	DDR_A_DQS0	MEM_A_DQS_N<0>	12 31
T19 DDR_A_DQS1	DDR_DQS_PHY	DDR_A_DQS1	MEM_A_DQS_P<1>	12 31
T19 DDR_A_DQS1	DDR_DQS_PHY	DDR_A_DQS1	MEM_A_DQS_N<1>	12 31
T20 DDR_A_DQS2	DDR_DQS_PHY	DDR_A_DQS2	MEM_A_DQS_P<2>	12 31
T20 DDR_A_DQS2	DDR_DQS_PHY	DDR_A_DQS2	MEM_A_DQS_N<2>	12 31
T20 DDR_A_DQS3	DDR_DQS_PHY	DDR_A_DQS3	MEM_A_DQS_P<3>	12 31
T20 DDR_A_DQS3	DDR_DQS_PHY	DDR_A_DQS3	MEM_A_DQS_N<3>	12 31
T20 DDR_A_DQS4	DDR_DQS_PHY	DDR_A_DQS4	MEM_A_DQS_P<4>	12 31
T20 DDR_A_DQS4	DDR_DQS_PHY	DDR_A_DQS4	MEM_A_DQS_N<4>	12 31
T20 DDR_A_DQS5	DDR_DQS_PHY	DDR_A_DQS5	MEM_A_DQS_P<5>	12 31
T20 DDR_A_DQS5	DDR_DQS_PHY	DDR_A_DQS5	MEM_A_DQS_N<5>	12 31
T20 DDR_A_DQS6	DDR_DQS_PHY	DDR_A_DQS6	MEM_A_DQS_P<6>	12 31
T20 DDR_A_DQS6	DDR_DQS_PHY	DDR_A_DQS6	MEM_A_DQS_N<6>	12 31
T21 DDR_A_DQS7	DDR_DQS_PHY	DDR_A_DQS7	MEM_A_DQS_P<7>	12 31
T21 DDR_A_DQS7	DDR_DQS_PHY	DDR_A_DQS7	MEM_A_DQS_N<7>	12 31
Channel B				
T21 DDR_B_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_P<1..0>	12 30
T21 DDR_B_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_N<1..0>	12 30
T25 DDR_B_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_P<3..2>	8 12
T25 DDR_B_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_N<3..2>	8 12
T21 DDR_B_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CKE<1..0>	12 30
T21 DDR_B_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CS_L<1..0>	12 30
T21 DDR_B_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_ODT<1..0>	12 30
T25 DDR_B_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CKE<3..2>	8 12
T25 DDR_B_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CS_L<3..2>	8 12
T25 DDR_B_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_ODT<3..2>	8 12
T21 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_A<15..0>	12 30
T21 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_BA<2..0>	12 30
T21 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_RAS_L	12 30
T22 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_CAS_L	12 30
T21 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_WE_L	12 30
T22 DDR_B_DQ_BYTE0	DDR_DQ_PHY	DDR_B_DQ_BYTE0	MEM_B_DQ<7..0>	12 31
T22 DDR_B_DQ_BYTE1	DDR_DQ_PHY	DDR_B_DQ_BYTE1	MEM_B_DQ<15..8>	12 31
T22 DDR_B_DQ_BYTE2	DDR_DQ_PHY	DDR_B_DQ_BYTE2	MEM_B_DQ<23..16>	12 31
T22 DDR_B_DQ_BYTE3	DDR_DQ_PHY	DDR_B_DQ_BYTE3	MEM_B_DQ<31..24>	12 31
T22 DDR_B_DQ_BYTE4	DDR_DQ_PHY	DDR_B_DQ_BYTE4	MEM_B_DQ<39..32>	12 31
T22 DDR_B_DQ_BYTE5	DDR_DQ_PHY	DDR_B_DQ_BYTE5	MEM_B_DQ<47..40>	12 31
T22 DDR_B_DQ_BYTE6	DDR_DQ_PHY	DDR_B_DQ_BYTE6	MEM_B_DQ<55..48>	12 31
T22 DDR_B_DQ_BYTE7	DDR_DQ_PHY	DDR_B_DQ_BYTE7	MEM_B_DQ<63..56>	12 31
T23 DDR_B_DQS0	DDR_DQS_PHY	DDR_B_DQS0	MEM_B_DQS_P<0>	12 31
T23 DDR_B_DQS0	DDR_DQS_PHY	DDR_B_DQS0	MEM_B_DQS_N<0>	12 31
T23 DDR_B_DQS1	DDR_DQS_PHY	DDR_B_DQS1	MEM_B_DQS_P<1>	12 31
T23 DDR_B_DQS1	DDR_DQS_PHY	DDR_B_DQS1	MEM_B_DQS_N<1>	12 31
T23 DDR_B_DQS2	DDR_DQS_PHY	DDR_B_DQS2	MEM_B_DQS_P<2>	12 31
T23 DDR_B_DQS2	DDR_DQS_PHY	DDR_B_DQS2	MEM_B_DQS_N<2>	12 31
T23 DDR_B_DQS3	DDR_DQS_PHY	DDR_B_DQS3	MEM_B_DQS_P<3>	12 31
T23 DDR_B_DQS3	DDR_DQS_PHY	DDR_B_DQS3	MEM_B_DQS_N<3>	12 31
T23 DDR_B_DQS4	DDR_DQS_PHY	DDR_B_DQS4	MEM_B_DQS_P<4>	12 31
T23 DDR_B_DQS4	DDR_DQS_PHY	DDR_B_DQS4	MEM_B_DQS_N<4>	12 31
T24 DDR_B_DQS5	DDR_DQS_PHY	DDR_B_DQS5	MEM_B_DQS_P<5>	12 31
T24 DDR_B_DQS5	DDR_DQS_PHY	DDR_B_DQS5	MEM_B_DQS_N<5>	12 31
T24 DDR_B_DQS6	DDR_DQS_PHY	DDR_B_DQS6	MEM_B_DQS_P<6>	12 31
T24 DDR_B_DQS6	DDR_DQS_PHY	DDR_B_DQS6	MEM_B_DQS_N<6>	12 31
T24 DDR_B_DQS7	DDR_DQS_PHY	DDR_B_DQS7	MEM_B_DQS_P<7>	12 31
T24 DDR_B_DQS7	DDR_DQS_PHY	DDR_B_DQS7	MEM_B_DQS_N<7>	12 31
Reset				
T24	DDR_50S		MEM_RESET_L	28 29 30

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PCI Express/DMI

PCIe-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
PCIE_COMP	*	Y	0.305 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCIE3_PHY	*	PCIE_80D
CLK_PCIE_PHY	*	PCIE_90D
COMP_PCIE_PHY	*	PCIE_COMP

PCIe and DMI Compensation Rules (mils)

Table	Imp	Design	Iso	Design	Comments
4-5	50	50	15	15.75	PCIe. Impedance inferred from Table 4-7.
4-7	50	50	8	15.75	DMI. Numbers based on Intel stack-up.

PCIe-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_ISO	*	=5:1_SPACING	?
COMP_PCIE_ISO	*	=4:1_SPACING	?

Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	*	*	CLK_PCIE_ISO
COMP_PCIE	*	*	COMP_PCIE_ISO
PEG_R2D	PEG_R2D	*	PEG_SAME_DIR
PEG_D2R	PEG_D2R	*	PEG_SAME_DIR
PEG_D2R	PEG_R2D	*	PEG_ALT_DIR
PEG_D2R	*	*	PEG_ISO
PEG_R2D	*	*	PEG_ISO

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_SAME_DIR	TOP,BOTTOM	=5X_DIELECTRIC	?
PEG_SAME_DIR	*	=3.5X_DIELECTRIC	?
PEG_ALT_DIR	*	=7X_DIELECTRIC	?
PEG_ISO	*	=4:1_SPACING	?

PEG Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
4.2.1	80	80	16	15.75	PCIe Gen3. Allow looser spacing for same direction on stripline per Anil

PCIe (CPU)

Electrical Contraint Set	Physical	Spacing	
x16 Graphics			
R440 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<15> 71
R441 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<15> 71
R442	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<15> 9 71
R443	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<15> 9 71
R444 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<15> 9 71
R445 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<15> 9 71
R446	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<15> 71
R447	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<15> 71
R448 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<14> 71
R449 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<14> 71
R450	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<14> 9 71
R451	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<14> 9 71
R452 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<14> 9 71
R453 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<14> 9 71
R454	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<14> 71
R455	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<14> 71
R456 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<13> 71
R457 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<13> 71
R458	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<13> 9 71
R459	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<13> 9 71
R460 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<13> 9 71
R461 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<13> 9 71
R462	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<13> 71
R463	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<13> 71
R464 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<12> 71
R465 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<12> 71
R466	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<12> 9 71
R467	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<12> 9 71
R468 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<12> 9 71
R469 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<12> 9 71
R470	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<12> 71
R471	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<12> 71
R472 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<11> 71
R473 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<11> 71
R474	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<11> 9 71
R475	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<11> 9 71
R476 PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<11> 9 71
R477 PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<11> 9 71
R478	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<11> 71
R479	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<11> 71
R480 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<10> 71
R481 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<10> 71
R482	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<10> 9 71
R483	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<10> 9 71
R484 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<10> 9 71
R485 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<10> 9 71
R486	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<10> 71
R487	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<10> 71
R488 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<9> 71
R489 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<9> 71
R490	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<9> 9 71
R491	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<9> 9 71
R492 PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<9> 9 71
R493 PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<9> 9 71
R494	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<9> 71
R495	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<9> 71
R496 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<8> 71
R497 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<8> 71
R498	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<8> 9 71
R499	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<8> 9 71
R500 PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<8> 9 71
R501 PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<8> 9 71
R502	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<8> 71
R503	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<8> 71

PCIe (CPU)

Electrical Contraint Set	Physical	Spacing	
x16 Graphics			
R504 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<7> 71
R505 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<7> 71
R506	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<7> 9 71
R507	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<7> 9 71
R508 PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<7> 9 71
R509 PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<7> 9 71
R510	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<7> 71
R511	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<7> 71
R512 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<6> 71
R513 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<6> 71
R514	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<6> 9 71
R515	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<6> 9 71
R516 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<6> 9 71
R517 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<6> 9 71
R518	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<6> 71
R519	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<6> 71
R520 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<5> 71
R521 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<5> 71
R522	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<5> 9 71
R523	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<5> 9 71
R524 PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<5> 9 71
R525 PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<5> 9 71
R526	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<5> 71
R527	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<5> 71
R528 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<4> 71
R529 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<4> 71
R530	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<4> 9 71
R531	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<4> 9 71
R532 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<4> 9 71
R533 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<4> 9 71
R534	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<4> 71
R535	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<4> 71
R536 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<3> 71
R537 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<3> 71
R538	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<3> 9 71
R539	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<3> 9 71
R540 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<3> 9 71
R541 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<3> 9 71
R542	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<3> 71
R543	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<3> 71
R544 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<2> 71
R545 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<2> 71
R546	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<2> 9 71
R547	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<2> 9 71
R548 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<2> 9 71
R549 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<2> 9 71
R550	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<2> 71
R551	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<2> 71
R552 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<1> 71
R553 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<1> 71
R554	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<1> 9 71
R555	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<1> 9 71
R556 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<1> 9 71
R557 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<1> 9 71
R558	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<1> 71
R559	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<1> 71
R560 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<0> 71
R561 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<0> 71
R562	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<0> 9 71
R563	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<0> 9 71
R564 PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<0> 9 71
R565 PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<0> 9 71
R566	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<0> 71
R567	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<0> 71
CPU PCIe Clocks			
R568 PEG_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PEG_CLK100M_P 10 71
R569 PEG_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PEG_CLK100M_N 10 71
CPU PCIe Compensation			
R570	COMP_PCIE_PHY	COMP_PCIE	CPU_PEG_COMP 10

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Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCIE_PHY	*	PCIE_85D
COMP_DMI_PHY	*	50_OHM_SE

PCIe-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_SAME_DIR	TOP,BOTTOM	=5X_DIELECTRIC	?
PCIE_SAME_DIR	*	=3.5X_DIELECTRIC	?
PCIE_ALT_DIR	*	=7X_DIELECTRIC	?
PCIE_ISO	*	=4:1_SPACING	?

TBT x4 PCIE Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_TBT_R2D	PCIE_TBT_R2D	*	PCIE_SAME_DIR
PCIE_TBT_D2R	PCIE_TBT_D2R	*	PCIE_SAME_DIR
PCIE_TBT_D2R	PCIE_TBT_R2D	*	PCIE_ALT_DIR
PCIE_TBT_D2R	*	*	PCIE_ISO
PCIE_TBT_R2D	*	*	PCIE_ISO

SSD x2 PCIE Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_SSD_R2D	PCIE_SSD_R2D	*	PCIE_SAME_DIR
PCIE_SSD_D2R	PCIE_SSD_D2R	*	PCIE_SAME_DIR
PCIE_SSD_D2R	PCIE_SSD_R2D	*	PCIE_ALT_DIR
PCIE_SSD_D2R	*	*	PCIE_ISO
PCIE_SSD_R2D	*	*	PCIE_ISO

PCH x1 PCIE Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE	*	*	PCIE_ISO

DMI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_SAME_DIR	TOP,BOTTOM	=5X_DIELECTRIC	?
DMI_SAME_DIR	*	=4X_DIELECTRIC	?
DMI_ALT_DIR	*	=5X_DIELECTRIC	?
DMI_ISO	*	=4X_DIELECTRIC	?

DMI x4 PCIE Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_N2S	DMI_N2S	*	DMI_SAME_DIR
DMI_S2N	DMI_S2N	*	DMI_SAME_DIR
DMI_N2S	DMI_S2N	*	DMI_ALT_DIR
DMI_N2S	*	*	DMI_ISO
DMI_S2N	*	*	DMI_ISO

PCIe (PCH)

Electrical Contraint Set	Physical	Spacing		
x4 Thunderbolt				
H137 PCIE_GEN2_R2D	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_P<3..0>	34
H138 PCIE_GEN2_R2D	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_N<3..0>	34
H139	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_C_P<3..0>	18 34
H140	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_C_N<3..0>	18 34
H141 PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_P<3..0>	18 34
H142 PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_N<3..0>	18 34
H143	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_C_P<3..0>	34
H144	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_C_N<3..0>	34
H145 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_TBT_P	18 34
H146 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_TBT_N	18 34
x2 SSD				
H174 PCIE_GEN2_R2D_CONN_SSD	PCIE_PHY	PCIE_SSD_R2D	PCIE_SSD_R2D_P<1>	41
H175 PCIE_GEN2_R2D_CONN_SSD	PCIE_PHY	PCIE_SSD_R2D	PCIE_SSD_R2D_N<1>	41
H176	PCIE_PHY	PCIE_SSD_R2D	PCIE_SSD_R2D_C_P<1>	18 41
H177	PCIE_PHY	PCIE_SSD_R2D	PCIE_SSD_R2D_C_N<1>	18 41
H178 PCIE_GEN2_D2R_CONN_SSD	PCIE_PHY	PCIE_SSD_D2R	PCIE_SSD_D2R_P<1>	18 41
H179 PCIE_GEN2_D2R_CONN_SSD	PCIE_PHY	PCIE_SSD_D2R	PCIE_SSD_D2R_N<1>	18 41
H180	PCIE_PHY	PCIE_SSD_D2R	PCIE_SSD_D2R_C_P<1>	41
H181	PCIE_PHY	PCIE_SSD_D2R	PCIE_SSD_D2R_C_N<1>	41
H182 PCIE_GEN2_R2D_MUX_SSD	PCIE_PHY	PCIE_SSD_R2D	PCIE_SSD_R2D_P<0>	41
H183 PCIE_GEN2_R2D_MUX_SSD	PCIE_PHY	PCIE_SSD_R2D	PCIE_SSD_R2D_N<0>	41
H184	PCIE_PHY	PCIE_SSD_R2D	PCIE_SSD_R2D_C_P<0>	18 41
H185	PCIE_PHY	PCIE_SSD_R2D	PCIE_SSD_R2D_C_N<0>	18 41
H186 PCIE_GEN2_D2R_MUX_SSD	PCIE_PHY	PCIE_SSD_D2R	PCIE_SSD_D2R_P<0>	18 41
H187 PCIE_GEN2_D2R_MUX_SSD	PCIE_PHY	PCIE_SSD_D2R	PCIE_SSD_D2R_N<0>	18 41
H188	PCIE_PHY	PCIE_SSD_D2R	PCIE_SSD_D2R_C_P<0>	41
H189	PCIE_PHY	PCIE_SSD_D2R	PCIE_SSD_D2R_C_N<0>	41
H190 PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_SSD_P	18 41
H191 PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_SSD_N	18 41
x1 AirPort				
H152 PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_R2D_P	33
H153 PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_R2D_N	33
H154	PCIE_PHY	PCIE	PCIE_AP_R2D_C_P	18 33
H155	PCIE_PHY	PCIE	PCIE_AP_R2D_C_N	18 33
H156 PCIE_GEN2_D2R_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_D2R_P	18 33
H157 PCIE_GEN2_D2R_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_D2R_N	18 33
H158	PCIE_PHY	PCIE	PCIE_AP_D2R_C_P	
H159	PCIE_PHY	PCIE	PCIE_AP_D2R_C_N	
H160 PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_AP_P	18 33
H161 PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_AP_N	18 33
x1 Caesar IV				
H151 PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_ENET_R2D_P	37
H150 PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_ENET_R2D_N	37
H149	PCIE_PHY	PCIE	PCIE_ENET_R2D_C_P	18 37
H148	PCIE_PHY	PCIE	PCIE_ENET_R2D_C_N	18 37
H147 PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_ENET_D2R_P	18 37
H146 PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_ENET_D2R_N	18 37
H145	PCIE_PHY	PCIE	PCIE_ENET_D2R_C_P	37
H144	PCIE_PHY	PCIE	PCIE_ENET_D2R_C_N	37
H135 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_ENET_P	18 37
H136 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_ENET_N	18 37

DMI

Electrical Contraint Set	Physical	Spacing		
DMI				
H165 DMI_N2S	PCIE_PHY	DMI_N2S	DMI_N2S_P<3..0>	10 19
H166 DMI_N2S	PCIE_PHY	DMI_N2S	DMI_N2S_N<3..0>	10 19
H167 DMI_S2N	PCIE_PHY	DMI_S2N	DMI_S2N_P<3..0>	10 19
H168 DMI_S2N	PCIE_PHY	DMI_S2N	DMI_S2N_N<3..0>	10 19
H169 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	DMI_CLK100M_CPU_P	11 18
H170 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	DMI_CLK100M_CPU_N	11 18
DMI Compensation				
H171	COMP_DMI_PHY	COMP_PCIE	PCH_DMI_COMP	19

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SATA

SATA-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SATA_PHY	*	SATA_90D
COMP_SATA_PHY	*	SATA_50S

SATA-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ISO	*	=6:1_SPACING	?
COMP_SATA_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA	*	*	SATA_ISO
COMP_SATA	*	*	COMP_SATA_ISO

SATA Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
15.2.1	90	95	20	23.62	SATA Gen2, SATA Gen3

SATA Compensation Rules (mils)

Table	Imp	Design	Iso	Design	Comments
15-3	50	50	15	15.75	SATA Gen2, SATA Gen3

FDI

FDI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FDI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
COMP_FDI	*	Y	0.25 MM	0.25 MM	3 MM	=STANDARD	=STANDARD
FDI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
FDI_DIFF_PHY	*	FDI_85D
FDI_SE_PHY	*	FDI_50S
COMP_FDI_PHY	*	COMP_FDI

FDI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FDI_ISO	*	=3:1_SPACING	?
COMP_FDI_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FDI	*	*	FDI_ISO
COMP_FDI	*	*	COMP_FDI_ISO

FDI Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Table	Imp	Design	Iso	Design	Comments
6-1/6-2	85	85	12	11.81	FDI main length

FDI Compensation Rules (mils)

Table	Trace	Design	Iso	Design	Comments
6-4	10	11.81	-	15.75	Using PCIe guidelines

XDP

XDP-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
XDP_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
XDP_PHY	*	XDP_55S

XDP-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XDP_ISO	*	=2:1_SPACING	?
CLK_JTAG_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
XDP	*	*	XDP_ISO
CLK_JTAG	*	*	CLK_JTAG_ISO

Desktop Debug Design Guide (Intel Doc# 430883)

Section	Imp	Design	Iso	Design	Comments
1.5	45-65	55	-	15.75	Isolation is for JTAG clocks. All signals default are 50 Ohm SE.

SATA

Electrical Contraint Set	Physical	Spacing		
PCH SATA Port 0 (HDD)				
E90 SATA_R2D	SATA_PHY	SATA	SATA_HDD_R2D_P	41
E92 SATA_R2D	SATA_PHY	SATA	SATA_HDD_R2D_N	41
E89	SATA_PHY	SATA	SATA_HDD_R2D_C_P	10 41
E89	SATA_PHY	SATA	SATA_HDD_R2D_C_N	10 41
E84 SATA_D2R	SATA_PHY	SATA	SATA_HDD_D2R_P	10 41
E85 SATA_D2R	SATA_PHY	SATA	SATA_HDD_D2R_N	10 41
E91	SATA_PHY	SATA	SATA_HDD_D2R_C_P	41
E93	SATA_PHY	SATA	SATA_HDD_D2R_C_N	41
PCH SATA Port 1 (SSD)				
E97 SATA_R2D_MUX_SSD	SATA_PHY	SATA	SATA_SSD_R2D_P	41
E99 SATA_R2D_MUX_SSD	SATA_PHY	SATA	SATA_SSD_R2D_N	41
E96	SATA_PHY	SATA	SATA_SSD_R2D_C_P	10 41
E98	SATA_PHY	SATA	SATA_SSD_R2D_C_N	10 41
E109 SATA_D2R_MUX_SSD	SATA_PHY	SATA	SATA_SSD_D2R_P	10 41
E107 SATA_D2R_MUX_SSD	SATA_PHY	SATA	SATA_SSD_D2R_N	10 41
E106	SATA_PHY	SATA	SATA_SSD_D2R_C_P	41
E105	SATA_PHY	SATA	SATA_SSD_D2R_C_N	41
SSD PCIe/SATA Mux Output				
E113 PCIE_SATA_R2D_MUX_CONN	SATA_PHY	SATA	PCIE_SATA_SSD_R2D_P	41
E114 PCIE_SATA_R2D_MUX_CONN	SATA_PHY	SATA	PCIE_SATA_SSD_R2D_N	41
E117 PCIE_SATA_D2R_MUX_CONN	SATA_PHY	SATA	PCIE_SATA_SSD_D2R_P	41
E116 PCIE_SATA_D2R_MUX_CONN	SATA_PHY	SATA	PCIE_SATA_SSD_D2R_N	41
PCH SATA Compensation				
E102	COMP_SATA_PHY	COMP_SATA	PCH_SATAICOMP	10
E103	COMP_SATA_PHY	COMP_SATA	PCH_SATA3COMP	10
E101	COMP_SATA_PHY	COMP_SATA	PCH_SATA3RBIAS	10

FDI

Electrical Contraint Set	Physical	Spacing		
FDI				
E120 FDI_TX	FDI_DIFF_PHY	FDI	CPU_FDI_TX_P<7..0>	8 10
E119 FDI_TX	FDI_DIFF_PHY	FDI	CPU_FDI_TX_N<7..0>	8 10
E111	FDI_SE_PHY	FDI	CPU_FDI_FSYNC<1..0>	8 10
E112	FDI_SE_PHY	FDI	CPU_FDI_LSYNC<1..0>	8 10
E110	FDI_SE_PHY	FDI	CPU_FDI_INT	8 10
FDI Compensation				
E115	COMP_FDI_PHY	COMP_FDI	CPU_FDI_COMPIO	10

XDP

Electrical Contraint Set	Physical	Spacing		
CPU XDP				
J37	XDP_PHY	XDP	XDP_BPM_L<7..0>	11 25
J38	XDP_PHY	XDP	CPU_CFG<17..0>	8 10 15 25
J39 TTP_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	ITPCPU_CLK100M_P	11 15
J40 TTP_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	ITPCPU_CLK100M_N	11 15
E41	CLK_PCIE_PHY	CLK_PCIE	ITPXDP_CLK100M_P	15 18 25
E43	CLK_PCIE_PHY	CLK_PCIE	ITPXDP_CLK100M_N	15 18 25
E42	CLK_PCIE_PHY	CLK_PCIE	XDP_CPU_CLK100M_P	25
E44	CLK_PCIE_PHY	CLK_PCIE	XDP_CPU_CLK100M_N	25
E45	XDP_PHY	CLK_JTAG	XDP_CPU_TCK	11 25
E46	XDP_PHY	XDP	XDP_CPU_TMS	11 25
E47	XDP_PHY	XDP	XDP_CPU_TDI	11 25
E48	XDP_PHY	XDP	XDP_CPU_TDO	11 25
PCH XDP				
E49	XDP_PHY	CLK_JTAG	XDP_PCH_TCK	18 25
E50	XDP_PHY	XDP	XDP_PCH_TMS	18 25
E51	XDP_PHY	XDP	XDP_PCH_TDI	18 25
E52	XDP_PHY	XDP	XDP_PCH_TDO	18 25

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PCH

PCH-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

PCH-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCH	*	=4:1_SPACING	?
COMP_PCH	*	=2:1_SPACING	?

PCI

PCI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

PCI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCI	*	=2:1_SPACING	?

LPC

LPC-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

LPC-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=1.5:1_SPACING	?
CLK_LPC	*	=2:1_SPACING	?

HDA

HDA-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

HDA-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

Crystal

Crystal-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

Crystal-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4X_DIELECTRIC	?

SPI

SPI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=2:1_SPACING	?

PCI

Electrical Contraint Set	Physical	Spacing		
PCI Clock				
B33	CLK_PCI_55S	CLK_PCI	PCH_CLK33M_PCIIN	18 26
B32	CLK_PCI_55S	CLK_PCI	PCH_CLK33M_PCIOUT	20 26

LPC

Electrical Contraint Set	Physical	Spacing		
LPC				
B32	LPC_55S	LPC	LPC_AD<3..0>	18 44 46
B33	LPC_55S	LPC	LPC_R_AD<3..0>	18
B33	LPC_55S	LPC	LPC_FRAME_L	18 44 46
B37	LPC_55S	LPC	LFRAME_L	18
LPC Clocks				
B33	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	26 46
B34	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS_R	20 26
B43	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	26 44
B42	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	20 26

PCH Clocks

Electrical Contraint Set	Physical	Spacing		
PCH Reference Clock				
E18	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_SB	26
E40	CLK_PCH_55S	CLK_PCH	PCH_CLK25M_XTALIN	18 26
PCH Ref Clock Comp				
E40	PCH_55S	COMP_PCH	PCH_XCLK_RCOMP	18
PCH RTC 32K				
E43	CLK_XTAL	XTAL	PCH_CLK32K_RTCX1	18 26
E44	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2	18 26
E52	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2_R	26
SMC 32K				
E24	CLK_PCH_55S	CLK_PCH	PM_CLK32K_SUSCLK_R	19 45
F50	CLK_PCH_55S	CLK_PCH	SMC_CLK32K	44 45

25 MHz Reference Clocks

Electrical Contraint Set	Physical	Spacing		
25M Reference Crystal				
B20	CLK_XTAL	XTAL	SYSCLK_CLK25M_X1	26
B19	CLK_XTAL	XTAL	SYSCLK_CLK25M_X2	26
B21	CLK_XTAL	XTAL	SYSCLK_CLK25M_X2_R	26
25M Reference Clocks				
E16	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_ENET	26 37
E16	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_ENET_R	26
E18	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_TBT	26 34
E18	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_TBT_R	34

HDA

Electrical Contraint Set	Physical	Spacing		
HDA				
B33	HDA_55S	HDA	HDA_BIT_CLK	18 52
B40	HDA_55S	HDA	HDA_BIT_CLK_R	18
B36	HDA_55S	HDA	HDA_RST_L	18 52
B40	HDA_55S	HDA	HDA_RST_R_L	18
B46	HDA_55S	HDA	HDA_SDOUT	18 52
B46	HDA_55S	HDA	HDA_SDOUT_R	15 18
B46	HDA_55S	HDA	HDA_SYNC	15 18 52
B40	HDA_55S	HDA	HDA_SYNC_R	18
B46	HDA_55S	HDA	HDA_SDIN0	18 52
B46	HDA_55S	HDA	AUD_SDI_R	52
SPDIF				
B47		HDA	AUD_SPDIF_CHIP	52
B47		HDA	AUD_SPDIF_OUT	52 56

SPI Bootrom

Electrical Contraint Set	Physical	Spacing		
SPI ROM				
B31	SPI_50S	SPI	SPI_CLK_R	18 46
B42	SPI_50S	SPI	SPI_CLK	46
B39	SPI_50S	SPI	SPI_ALT_CLK	46
B40	SPI_50S	SPI	SPI_SMC_CLK	44 45
B40	SPI_50S	SPI	SPI_MLB_CLK	45 46
B34	SPI_50S	SPI	SPI_CS0_R_L	18 46
B33	SPI_50S	SPI	SPI_CS0_L	46
B39	SPI_50S	SPI	SPI_ALT_CS_L	46
B40	SPI_50S	SPI	SPI_SMC_CS_L	44 45
B37	SPI_50S	SPI	SPI_MLB_CS_L	45 46
B39	SPI_50S	SPI	SPI_MOSI_R	18 46
B40	SPI_50S	SPI	SPI_MOSI	46
B40	SPI_50S	SPI	SPI_ALT_MOSI	46
B41	SPI_50S	SPI	SPI_SMC_MOSI	44 45
B41	SPI_50S	SPI	SPI_MLB_MOSI	45 46
B40	SPI_50S	SPI	SPI_MISO	18 46
B40	SPI_50S	SPI	SPI_ALT_MISO	46
B41	SPI_50S	SPI	SPI_SMC_MISO	44 45
B41	SPI_50S	SPI	SPI_MLB_MISO	45 46
B40	SPI_50S	SPI	SPIROM_USE_MLB	21 46

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USB

USB-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB2_PHY	*	USB_90D
USB3_PHY	*	USB_85D

USB-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2_ISO	*	=3:1_SPACING	?
USB2_ISO	TOP,BOTTOM	=3:1_SPACING	?
USB3_ISO	*	=5.5:1_SPACING	?
USB3_ISO	TOP,BOTTOM	=5.5:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB2	*	*	USB2_ISO
USB3	*	*	USB3_ISO

USB Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
12.2.1	90	90	12	11.81	USB 2.0
13.3.1	85	85	20	21.65	USB 3.0

Caesar IV (Ethernet/SD)

CIV-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SD_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
ENET_COMP_PHY	*	ENET_50S
ENET_DIFF_PHY	*	ENET_100D
SD_PHY	*	SD_50S
CIV_SPI	*	SPI_55S

CIV-specific Spacing Definitions

Ethernet

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_DIFF_ISO	*	=6:1_SPACING	?
ENET_DIFF2DIFF	*	=3:1_SPACING	?
ENET_TRANS_ISO	*	1.27 MM	?
COMP_ENET_ISO	*	=4:1_SPACING	?

SD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_ISO	*	=3:1_SPACING	?

Constraints

Ethernet

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_DIFF	*	*	ENET_DIFF_ISO
ENET_DIFF	ENET_DIFF	*	ENET_DIFF2DIFF
ENET_TRANS	*	*	ENET_TRANS_ISO
COMP_ENET	*	*	COMP_ENET_ISO
ENET_TRANS	ENET_TRANS	*	ENET_DIFF2DIFF

2 kV isolation

SD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SD	*	*	SD_ISO

Camera Processor-to-Camera Sensor I/F (SMIA/MIPI)

Camera Processor's SMIA Interface Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMIA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMIA_DIFF_PHY	*	SMIA_100D

Camera Processor's SMIA Interface Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMIA_DIFF_ISO	*	=6:1_SPACING	?
SMIA_DIFF2DIFF	*	=3:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMIA_DIFF	*	*	SMIA_DIFF_ISO
SMIA_DIFF	SMIA_DIFF	*	SMIA_DIFF2DIFF

USB 3.0 and USB 2.0 Trixies Muxing

Electrical Contraint Set	Physical	Spacing	
External Port A (J4600)			
H32 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTA_RX_P 42
H31 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTA_RX_N 42
H30	USB3_PHY	USB3	USB3_EXTA_RX_F_P 20 42
H29	USB3_PHY	USB3	USB3_EXTA_RX_F_N 20 42
H41 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTA_TX_P 20 42
H40 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTA_TX_N 20 42
H38	USB3_PHY	USB3	USB3_EXTA_TX_F_P 42
H37	USB3_PHY	USB3	USB3_EXTA_TX_F_N 42
H49	USB3_PHY	USB3	USB3_EXTA_TX_C_P 42
H48	USB3_PHY	USB3	USB3_EXTA_TX_C_N 42
H47 USB2_MUXED_MOJO_CONN	USB2_PHY	USB2	USB_PCH_0_P 20 42
H46 USB2_MUXED_MOJO_CONN	USB2_PHY	USB2	USB_PCH_0_N 20 42
H45	USB2_PHY	USB2	USB2_EXTA_MUXED_P 42
H42	USB2_PHY	USB2	USB2_EXTA_MUXED_N 42
H39	USB2_PHY	USB2	USB2_EXTA_P 42
H36	USB2_PHY	USB2	USB2_EXTA_N 42
External Port B (J4610)			
H32 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTB_RX_P 42
H31 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTB_RX_N 42
H30	USB3_PHY	USB3	USB3_EXTB_RX_F_P 20 42
H29	USB3_PHY	USB3	USB3_EXTB_RX_F_N 20 42
H41 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTB_TX_P 20 42
H40 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTB_TX_N 20 42
H38	USB3_PHY	USB3	USB3_EXTB_TX_F_P 42
H37	USB3_PHY	USB3	USB3_EXTB_TX_F_N 42
H49	USB3_PHY	USB3	USB3_EXTB_TX_C_P 42
H48	USB3_PHY	USB3	USB3_EXTB_TX_C_N 42
H47 USB2_MUXED_CONN	USB2_PHY	USB2	USB_PCH_1_P 20 42
H46 USB2_MUXED_CONN	USB2_PHY	USB2	USB_PCH_1_N 20 42
H45	USB2_PHY	USB2	USB_PCH_9_P 20 42
H43	USB2_PHY	USB2	USB_PCH_9_N 20 42
H42	USB2_PHY	USB2	USB2_EXTB_MUXED_P 42
H33	USB2_PHY	USB2	USB2_EXTB_MUXED_N 42
H39	USB2_PHY	USB2	USB2_EXTB_P 42
H36	USB2_PHY	USB2	USB2_EXTB_N 42
External Port C (J4700)			
H32 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTC_RX_P 43
H31 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTC_RX_N 43
H30	USB3_PHY	USB3	USB3_EXTC_RX_F_P 20 43
H29	USB3_PHY	USB3	USB3_EXTC_RX_F_N 20 43
H41 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTC_TX_P 20 43
H40 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTC_TX_N 20 43
H38	USB3_PHY	USB3	USB3_EXTC_TX_F_P 43
H37	USB3_PHY	USB3	USB3_EXTC_TX_F_N 43
H49	USB3_PHY	USB3	USB3_EXTC_TX_C_P 43
H48	USB3_PHY	USB3	USB3_EXTC_TX_C_N 43
H47 USB2_CONN	USB2_PHY	USB2	USB_PCH_2_P 20 43
H46 USB2_CONN	USB2_PHY	USB2	USB_PCH_2_N 20 43
H45	USB2_PHY	USB2	USB2_EXTC_P 43
H42	USB2_PHY	USB2	USB2_EXTC_N 43
External Port D (J4710)			
H32 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTD_RX_P 43
H31 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTD_RX_N 43
H30	USB3_PHY	USB3	USB3_EXTD_RX_F_P 20 43
H29	USB3_PHY	USB3	USB3_EXTD_RX_F_N 20 43
H41 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTD_TX_P 20 43
H40 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTD_TX_N 20 43
H38	USB3_PHY	USB3	USB3_EXTD_TX_F_P 43
H37	USB3_PHY	USB3	USB3_EXTD_TX_F_N 43
H49	USB3_PHY	USB3	USB3_EXTD_TX_C_P 43
H48	USB3_PHY	USB3	USB3_EXTD_TX_C_N 43
H47 USB2_MUXED_CONN	USB2_PHY	USB2	USB_PCH_3_P 20 43
H46 USB2_MUXED_CONN	USB2_PHY	USB2	USB_PCH_3_N 20 43
H45	USB2_PHY	USB2	USB_PCH_10_P 20 43
H44	USB2_PHY	USB2	USB_PCH_10_N 20 43
H43	USB2_PHY	USB2	USB2_EXTD_MUXED_P 43
H40	USB2_PHY	USB2	USB2_EXTD_MUXED_N 43
H46	USB2_PHY	USB2	USB2_EXTD_P 43
H44	USB2_PHY	USB2	USB2_EXTD_N 43
Camera (J3510)			
H32 USB2_CONN_INT	USB2_PHY	USB2	USB_CAMERA_P 40
H30 USB2_CONN_INT	USB2_PHY	USB2	USB_CAMERA_N 40
PCH USB Compensation			
H12	PCH_55S	COMP_PCH	PCH_USB_RBIAS 20

RMH Love

Electrical Contraint Set	Physical	Spacing	
USB 2.0 Hub			
H40 USB2_HUB	USB2_PHY	USB2	USB_PCH_7_P 20 27
H39 USB2_HUB	USB2_PHY	USB2	USB_PCH_7_N 20 27
H49 USB2_HUB_CONN	USB2_PHY	USB2	USB_BT_P 27 33
H41 USB2_HUB_CONN	USB2_PHY	USB2	USB_BT_N 27 33
H50 USB2_HUB_CONN	USB2_PHY	USB2	USB_BT_MUX_P 33
H56 USB2_HUB_CONN	USB2_PHY	USB2	USB_BT_MUX_N 33
H37 USB2_HUB_RES	USB2_PHY	USB2	USB_SMC_P 27 44
H37 USB2_HUB_RES	USB2_PHY	USB2	USB_SMC_N 27 44
H46	USB2_PHY	USB2	USB_HUB_2_P 27
H47	USB2_PHY	USB2	USB_HUB_2_N 27
USB 2.0 Hub Compensation			
H47	PCH_55S	COMP_PCH	USB_HUB_RBIAS 27
USB 2.0 Hub Crystal			
H12	CLK_XTAL	XTAL	USB_HUB_XTAL1 27
H27	CLK_XTAL	XTAL	USB_HUB_XTAL2 27

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Electrical Contraint Set	Physical	Spacing	
Ethernet			
H47 ENET_MDI	ENET_DIFF_PHY	ENET_DIFF	ENETCONN_MDI_P<3..0> 37 38
H48 ENET_MDI	ENET_DIFF_PHY	ENET_DIFF	ENETCONN_MDI_N<3..0> 37 38
H47	ENET_DIFF_PHY	ENET_TRANS	ENETCONN_MDI_T_P<3..0> 38
H47	ENET_DIFF_PHY	ENET_TRANS	ENETCONN_MDI_T_N<3..0> 38
H51		ENET_TRANS	ENETCONN_MCT0 38
H50		ENET_TRANS	ENETCONN_MCT1 38
H52		ENET_TRANS	ENETCONN_MCT2 38
H52		ENET_TRANS	ENETCONN_MCT3 38
H52		ENET_TRANS	ENETCONN_MCT_BS 38
H47	ENET_COMP_PHY	COMP_ENET	ENET_RDAC 37
SD			
H47 SD_DATA	SD_PHY	SD	ENET_CR_DATA<7..0> 37
H48	SD_PHY	SD	SDCONN_DATA<7..0> 37 39
H51	SD_PHY	SD	SDCONN_DATA_R <7..0> 39
H48 SD_CMD	SD_PHY	SD	ENET_SD_CMD 37
H49	SD_PHY	SD	SDCONN_CMD 37 39
H51	SD_PHY	SD	SDCONN_CMD_R 39
H48 SD_CLK	SD_PHY	SD	ENET_SD_CLK 37
H48	SD_PHY	SD	SDCONN_CLK 37 39
H46	SD_PHY	SD	SDCONN_CLK_R 39
H48	SD_PHY	SD	ENET_MEDIA_SENSE 15 18 37
H48	SD_PHY	SD	ENET_SD_DETECT_L 37 39
H48	SD_PHY	SD	SDCONN_WP 37 39
CIV SPI			
H42	CIV_SPI	SPI	ENET_SCLK 37
H48	CIV_SPI	SPI	ENET_MISO 37
H42	CIV_SPI	SPI	ENET_MOSI 37
H42	CIV_SPI	SPI	ENET_CS_L 37

Camera Processor-Camera Sensor I/F

Electrical Contraint Set	Physical	Spacing	
H59 SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_P 40
H60 SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_N 40
H62 SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_F_P 40
H52 SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_F_N 40
H59 SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_P 40
H60 SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_N 40
H62 SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_F_P 40
H62 SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_F_N 40
H50	SPI_50S	SPI	CAM_SF_CLK 40
H60	SPI_50S	SPI	CAM_SF_CLK_R 40
H50	SPI_50S	SPI	CAM_SF_DIN 40
H51	SPI_50S	SPI	CAM_SF_DIN_R 40
H51	SPI_50S	SPI	CAM_SF_CS_L 40
H51	SPI_50S	SPI	CAM_SF_WP_L 40
H52	SPI_50S	SPI	CAM_SF_DOUT 40
H51	SPI_50S	SPI	CAM_SF_DOUT_R 40
H61	SMB_PHY	SMB	I2C_CAMSENSOR_SDA 40
H61	SMB_PHY	SMB	I2C_CAMSENSOR_SCL 40

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SMBus

SMBus-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMB_PHY	*	SMB_55S

SMBus-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB_ISO	*	=2x_DIELECTRIC	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMB	*	*	SMB_ISO

Sensor

Sensor-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SNS_DIFF_PHY	*	1:1_DIFFPAIR

Sensor-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SENSE	*	*	SENSE_ISO
SENSE	POWER	*	PWR_P2MM
SENSE	GND	*	GND_P2MM

SMBus

Electrical Contraint Set	Physical	Spacing		
SMC				
I10	SMB_PHY	SMB	SMBUS_SMC_0_S0_SCL	44 47
I9	SMB_PHY	SMB	SMBUS_SMC_0_S0_SDA	44 47
I11	SMB_PHY	SMB	SMBUS_SMC_1_S0_SCL	44 47
I12	SMB_PHY	SMB	SMBUS_SMC_1_S0_SDA	44 47
I13	SMB_PHY	SMB	SMBUS_SMC_2_S4_SCL	44 47
I14	SMB_PHY	SMB	SMBUS_SMC_2_S4_SDA	44 47
I15	SMB_PHY	SMB	SMBUS_SMC_3_SCL	44 47
I16	SMB_PHY	SMB	SMBUS_SMC_3_SDA	44 47
I19	SMB_PHY	SMB	SMBUS_SMC_5_G3H_SCL	44 45
I20	SMB_PHY	SMB	SMBUS_SMC_5_G3H_SDA	44 45
PCH				
I21	TBT_I2C_55S	TBT_I2C	SMBUS_PCH_CLK	18 47
I22	TBT_I2C_55S	TBT_I2C	SMBUS_PCH_DATA	18 47
I53	SMB_PHY	SMB	SML_PCH_0_CLK	18 47
I54	SMB_PHY	SMB	SML_PCH_0_DATA	18 47
Display TCon				
I55	SMB_PHY	SMB	SMB_DP_TCON_SCL	47 81
I56	SMB_PHY	SMB	SMB_DP_TCON_SDA	47 81

Temperature Sense

Electrical Contraint Set	Physical	Spacing		
EMC1414-1 (Production)				
I57 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_1_P	50
I58 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_1_N	50
I59 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_2_P	50
I60 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_2_N	50
I65 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_ACDC_P	6 50
I66 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_ACDC_N	6 50
TMP423 (Development)				
I67 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_1_P	50
I68 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_1_N	50
I69 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_2_P	50
I70 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_2_N	50
I61 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_SKIN_P	50
I62 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_SKIN_N	50
I71 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_3_P	50
I72 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_3_N	50
HDD Out-of-Band				
I73		SENSE	SMC_HDD_OOB_TEMP	
I74		SENSE	HDD_OOB_TEMP_CONN	
I75		SENSE	HDD_OOB_TEMP_FILT	
I76		SENSE	HDD_OOB_TEMP_R	
SSD Out-of-Band				
I77		SENSE	SMC_SSD_OOB_TEMP	
I78		SENSE	SMC_SSD_TEMP_CTL	
I79		SENSE	SSD_OOB_TEMP	

SMC

Electrical Contraint Set	Physical	Spacing		
SMC				
I1	CLK_XTAL	XTAL	SMC_XTAL	44 45
I2	CLK_XTAL	XTAL	SMC_EXTAL	44 45

Current/Voltage Sense

Electrical Contraint Set	Physical	Spacing		
Common				
I3		SENSE	GND_SMC_AVSS	44 45 48 49
12V S5 (System Total)				
I4 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VG3H_P	48
I5 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VG3H_N	48
I6		SENSE	ISNS_P12VG3H_R	48
I7		SENSE	ISNS_P12VG3H	45 48
I8		SENSE	VSNS_P12VG3H	45 48
12V S0 (GPU Core)				
I22 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_GPUCORE_P	48
I23 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_GPUCORE_N	48
I24		SENSE	ISNS_P12VS0_GPUCORE_R	48
I25		SENSE	ISNS_P12VS0_GPUCORE	45 48
I26		SENSE	VSNS_P12VS0_GPUCORE	45 48
HDD				
I80 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_HDD_P	48
I82 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_HDD_N	48
I81		SENSE	ISNS_HDDS0_R	48
I83		SENSE	ISNS_HDDS0	45 48
I84		SENSE	VSNS_HDDS0	45 48
SSD				
I85 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_SSD_P	49
I87 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_SSD_N	49
I86		SENSE	ISNS_SSDS0_R	49
I88		SENSE	ISNS_SSDS0	45 49
I89		SENSE	VSNS_SSDS0	45 49
VDDQ S3 (DDR)				
I33 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_VDDQS3_DDR_P	49
I32 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_VDDQS3_DDR_N	49
I31		SENSE	ISNS_VDDQS3_DDR_R	49
I34		SENSE	ISNS_VDDQS3_DDR	45 49
I35		SENSE	VSNS_VDDQS3_DDR	45 49
VDDQ S0 (GPU Uncore)				
I37 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_GPUUC_P	48
I38 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_GPUUC_N	48
I39		SENSE	ISNS_P12VS0_GPUUC_R	48
I40		SENSE	ISNS_P12VS0_GPUUNCORE	45 48
I41		SENSE	VSNS_P12VS0_GPUUNCORE	45 48
CPU Core				
I42 SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNS_CPUCORE_P	48
I43 SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNS_CPUCORE_N	48
I44		SENSE	ISNS_CPUCORE_FB	48
I45		SENSE	ISNS_CPUCORE	45 48
I46		SENSE	VSNS_CPUCORE	45 48
CPU AXG				
I47 SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNS_CPUAXG_P	48
I48 SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNS_CPUAXG_N	48
I49		SENSE	ISNS_CPUAXG_FB	48
I50		SENSE	ISNS_CPUAXG	45 48
I51		SENSE	VSNS_CPUAXG	45 48

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DC-DC

Power-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GND_P3MM	*	Y	0.300 MM	0.150 MM	3.0 MM	=STANDARD	=STANDARD
GND_P5MM	*	Y	0.500 MM	0.150 MM	3.0 MM	=STANDARD	=STANDARD
POWER_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
POWER_P3MM	*	Y	0.300 MM	0.150 MM	3.0 MM	=STANDARD	=STANDARD
POWER_P6MM	*	Y	0.600 MM	0.150 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GND	*	GND_P5MM
GND	BGA	GND_P3MM
POWER	*	POWER_P6MM
POWER	BGA	POWER_P3MM
VR_CTL_PHY	*	POWER_P3MM
VR_CTL_PHY	BGA	STANDARD
VR_VID_PHY	*	POWER_50S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
VR_DIDT_PHY	*	POWER_P6MM
VR_DIDT_PHY	BGA	STANDARD

Power-specific Spacing Definitions
Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
POWER_ISO	*	=STANDARD	?
GND_ISO	*	=STANDARD	?

Constraints
Power and Common

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER	*	*	POWER_ISO
GND	*	*	GND_ISO

DC-DC Baddies

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SWNODE_ISO	*	=8:1_SPACING	1000
SWNODE_SW2SW	*	=1:1_SPACING	?
SWNODE_SW2PWR	*	=2:1_SPACING	?
SWNODE_SW2GND	*	=2:1_SPACING	?

DC-DC Baddies

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_SWITCH	*	*	SWNODE_ISO
VR_SWITCH	*	BGA	BGA_P1MM
VR_SWITCH	VR_SWITCH	*	SWNODE_SW2SW
VR_SWITCH	POWER	*	SWNODE_SW2PWR
VR_SWITCH	GND	*	SWNODE_SW2GND

DC-DC Control

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL_ISO	*	=3:1_SPACING	?
VR_VID_ISO	*	=4X_DIELECTRIC	?

DC-DC Control

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_CTL	*	*	VR_CTL_ISO
VR_VID	*	*	VR_VID_ISO

VDDQ S3 (1.5V)/VTT S0

	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
I43	POWER	POWER	5V			REG_V5IN_U7700 68
Local Ground						
I44	GND	GND	0V			AGND_VDDQS3 68
VDDQ S3						
I45	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_VDDQS3 68
I46	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_VDDQS3_L 68
I47	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_VDDQS3 68
I48	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_VDDQS3_RC 68
I49	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_VDDQS3 68
I50	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_VDDQS3_R 68
I52	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_VDDQS3 68
I51	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_VDDQS3 68
I54	POWER	POWER	1.5V			PPVDDQ_S3_SENSE
I53	VR_CTL_PHY	VR_CTL				REG_VDDQS3_VDDQSNS 68
I55	VR_CTL_PHY	VR_CTL				REG_VDDQS3_VREF 68
I56	VR_CTL_PHY	VR_CTL				REG_VDDQS3_REFIN 68
I57	VR_CTL_PHY	VR_CTL				REG_VDDQS3_MODE 68
I58	VR_CTL_PHY	VR_CTL				REG_VDDQS3_TRIP 68
I59	VR_CTL_PHY	VR_CTL				LDO_DDRVTTS0_SNS 68
Output Bus						
I60	POWER	POWER	1.5V			PPVDDQ_S3 6
I61	POWER_DDR	POWER_DDR	0.75V			PPDDRVTT_S3 6
I62	POWER_DDR	POWER_DDR	0.75V			PPDDRVTT_S0 6
FET Switched						
I63	POWER	POWER	1.5V			PP1V5_S0 6
Sensed						
I64	POWER	POWER	1.5V			PPVDDQ_S3_DDR 6

CPU VccIO/ PCH 1.05V S0

	Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus							
I1		POWER	POWER	5V			REG_VCC_U7400 65
I2		POWER	POWER	5V			REG_PVCC_U7400 65
Local Ground							
I3		GND	GND	0V			AGND_P1V05S0 65
1.05V S0							
I5		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P1V05S0 65
I4		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P1V05S0_L 65
I7		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P1V05S0 65
I6		VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P1V05S0_RC 65
I8		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P1V05S0 65
I9		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P1V05S0_R 65
I10		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_P1V05S0 65
I12		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P1V05S0 65
I11		VR_CTL_PHY	VR_CTL				REG_P1V05S0_OCSET 65
I14		VR_CTL_PHY	VR_CTL				REG_P1V05S0_VO 65
I13	VSNS_CPU_VCCIO	SNS_DIFF_PHY	SENSE				SNS_CPU_VCCIO_P 13 65
I15	VSNS_CPU_VCCIO	SNS_DIFF_PHY	SENSE				SNS_CPU_VCCIO_N 13 65
I16		SNS_DIFF_PHY	SENSE				SNS_P1V05S0_XW_P 65
I17		SNS_DIFF_PHY	SENSE				SNS_P1V05S0_XW_N 65
I19			SENSE				REG_P1V05S0_FB 65
I18			SENSE				REG_P1V05S0_RTN 65
I21		VR_CTL_PHY	VR_CTL				REG_P1V05S0_SREF 65
I20		VR_CTL_PHY	VR_CTL				REG_P1V05S0_FSEL 65
Output Bus							
I22		POWER	POWER	1.05V			PP1V05_S0 6
FET Switched							
I23		POWER	POWER	1.05V			PP1V05_TBTLC 6
I66		POWER	POWER	1.05V			PP1V05_TBTCIO 6

CPU VccSA

	Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus							
I24		POWER	POWER	5V			REG_VCC_U7500 66
I25		POWER	POWER	5V			REG_PVCC_U7500 66
Local Ground							
I26		GND	GND	0V			AGND_VCCSAS0 66
VCCIO							
I27		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_VCCSAS0 66
I28		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_VCCSAS0 66
I29		VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_VCCSAS0_RC 66
I31		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_VCCSAS0 66
I30		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_VCCSAS0 66
I33		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_VCCSAS0 66
I32		VR_CTL_PHY	VR_CTL				REG_VCCSAS0_OCSET 66
I35		VR_CTL_PHY	VR_CTL				REG_VCCSAS0_VO 66
I34			SENSE				SNS_CPU_VCCSA 13 66
I37	VSNS_CPU_VCCSA	SNS_DIFF_PHY	SENSE				SNS_VCCSAS0_XW_P 66
I36	VSNS_CPU_VCCSA	SNS_DIFF_PHY	SENSE				SNS_VCCSAS0_XW_N 66
I38			SENSE				REG_VCCSAS0_FB 66
I39			SENSE				REG_VCCSAS0_RTN 66
I40		VR_CTL_PHY	VR_CTL				REG_VCCSAS0_SREF 66
I41		VR_CTL_PHY	VR_CTL				REG_VCCSAS0_FSEL 66
Output Bus							
I42		POWER	POWER	0.925V			PPVCCSA_S0 6

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CPU Core Phases

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
J11B	POWER	POWER	12V			PP12V_S0_CPUCORE_FLT	62 63 64
J11B	POWER	POWER	5V			REG_VCC_U7100	62
Local Ground							
J12C	GND	GND	0V			AGND_CPU	62 63 64
Phase 1							
J11B	POWER	POWER	12V			REG_LVCC_U7210	63
J12B	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_1	62 63
J13B	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_1_R	62
J11B	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUCORE_1	63
J11B	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUCORE_1	63
J12B	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUCORE_1_RC	63
J13B	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUCORE_1	63
J11B	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_CPUCORE_1	63
J12B	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_CPUCORE_1	63
J10B	POWER	POWER	1.1V			PPCPUCORE_S0_SENSE_1	63
J12B ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_1_P	62 63
J13B ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_1_N	63
J13A		SENSE				REG_ISENCORE_1_NR	62 63
Phase 2							
J11B	POWER	POWER	12V			REG_LVCC_U7230	63
J12B	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_2	62 63
J13B	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_2_R	62
J11B	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUCORE_2	63
J11B	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUCORE_2	63
J12B	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUCORE_2_RC	63
J13B	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUCORE_2	63
J11B	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_CPUCORE_2	63
J12B	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_CPUCORE_2	63
J10B	POWER	POWER	1.1V			PPCPUCORE_S0_SENSE_2	63
J12B ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_2_P	62 63
J13B ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_2_N	63
J13A		SENSE				REG_ISENCORE_2_NR	62 63
Phase 3							
J11B	POWER	POWER	12V			REG_LVCC_U7250	63
J12B	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_3	62 63
J13B	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_3_R	62
J11B	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUCORE_3	63
J11B	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUCORE_3	63
J12B	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUCORE_3_RC	63
J13B	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUCORE_3	63
J11B	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_CPUCORE_3	63
J12B	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_CPUCORE_3	63
J10B	POWER	POWER	1.1V			PPCPUCORE_S0_SENSE_3	63
J12B ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_3_P	62 63
J13B ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_3_N	63
J13A		SENSE				REG_ISENCORE_3_NR	62 63

CPU AXG Phase and Core Controller

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
AXG							
J11B	POWER	POWER	12V			REG_LVCC_U7330	64
J12B	VR_CTL_PHY	VR_CTL				REG_PWM_CPUAXG	62 64
J13B	VR_CTL_PHY	VR_CTL				REG_PWM_CPUAXG_R	62
J11B	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUAXG	64
J11B	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUAXG	64
J12B	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUAXG_RC	64
J13B	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUAXG	64
J11B	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_CPUAXG	64
J12B	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_CPUAXG	64
J10B	POWER	POWER	1.1V			PPCPUAXG_S0_SENSE	64
J12B ISNS_CPU_AXG	SNS_DIFF_PHY	SENSE				REG_ISENAXG_P	64
J13B ISNS_CPU_AXG	SNS_DIFF_PHY	SENSE				REG_ISENAXG_N	64
J13B		SENSE				REG_ISENAXG_PR	62 64
J13B		SENSE				REG_ISENAXG_NR	62 64
ISL6364							
J10C	VR_CTL_PHY	VR_CTL				REG_CPUCORE_COMP	62
J10C	VR_CTL_PHY	VR_CTL				CPUCORE_COMP_RC	62
J10C	VR_CTL_PHY	VR_CTL				REG_CPUCORE_FB	62
J10C	VR_CTL_PHY	VR_CTL				CPUCORE_FB_RC	62
J10C	VR_CTL_PHY	VR_CTL				CPUCORE_FB_R_1	62
J10C	VR_CTL_PHY	VR_CTL				CPUCORE_FB_R_2	62
J10C	VR_CTL_PHY	VR_CTL				CPUCORE_PSICOMP_RC	62
J10C	VR_CTL_PHY	VR_CTL				REG_CPUCORE_PSICOMP	62
J10C	VR_CTL_PHY	VR_CTL				REG_CPUCORE_HFCOMP	62
J10C VSNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CPU_VCORE_P	13 62
J10C VSNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CPU_VCORE_N	13 62
J10C	SNS_DIFF_PHY	SENSE				SNS_VCORE_R_P	62
J10C	SNS_DIFF_PHY	SENSE				SNS_VCORE_R_N	62
J10C	SNS_DIFF_PHY	SENSE	1.1V			SNS_VCORE_XW_P	62
J10C	SNS_DIFF_PHY	SENSE	0V			SNS_VCORE_XW_N	62
J10C		SENSE				REG_CPUCORE_VSEN	62
J10C		SENSE				REG_CPUCORE_RGND	62
J10C	VR_CTL_PHY	VR_CTL				REG_CPUCORE_IMON	48 62
J10C	VR_CTL_PHY	VR_CTL				CPUCORE_IMON_R	62
J10C	VR_CTL_PHY	VR_CTL				REG_CPUCORE_TM	62
J10C	VR_CTL_PHY	VR_CTL				REG_CPUCORE_SUTH	62
J10C	VR_CTL_PHY	VR_CTL				REG_CPUCORE_NPSI	62
J10C	VR_CTL_PHY	VR_CTL				REG_CPUCORE_FDVID	62
J10C	VR_CTL_PHY	VR_CTL				REG_CPUCORE_IAUTO	62
J10C	VR_CTL_PHY	VR_CTL				REG_CPUCORE_SW_FREQ	62
J10C	VR_CTL_PHY	VR_CTL				REG_CPUCORE_RAMPADJ	62
J10C	VR_CTL_PHY	VR_CTL				REG_CPUCORE_EN_PWR	62
J10C	VR_CTL_PHY	VR_CTL				CPUCORE_EN_PWR_R	62
J10C	VR_CTL_PHY	VR_CTL				REG_CPUCORE_RSET	62
J10A	VR_CTL_PHY	VR_CTL				REG_CPUAXG_COMP	62
J10A	VR_CTL_PHY	VR_CTL				CPUAXG_COMP_RC	62
J10A	VR_CTL_PHY	VR_CTL				REG_CPUAXG_FB	62
J10A	VR_CTL_PHY	VR_CTL				CPUAXG_FB_RC	62
J10A	VR_CTL_PHY	VR_CTL				CPUAXG_FB_R_1	62
J10A	VR_CTL_PHY	VR_CTL				CPUAXG_FB_R_2	62
J11A	VR_CTL_PHY	VR_CTL				REG_CPUAXG_HFCOMP	62
J10A VSNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CPU_VAXG_P	13 62
J10A VSNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CPU_VAXG_N	13 62
J10A	SNS_DIFF_PHY	SENSE				SNS_VAXG_R_P	62
J10A	SNS_DIFF_PHY	SENSE				SNS_VAXG_R_N	62
J10A	SNS_DIFF_PHY	SENSE	1.1V			SNS_VAXG_XW_P	62
J10A	SNS_DIFF_PHY	SENSE	0V			SNS_VAXG_XW_N	62
J10A		SENSE				REG_CPUAXG_VSEN	62
J10A		SENSE				REG_CPUAXG_RGND	62
J10A	VR_CTL_PHY	VR_CTL				REG_CPUAXG_IMON	48 62
J10A	VR_CTL_PHY	VR_CTL				CPUAXG_IMON_R	62
J10A	VR_CTL_PHY	VR_CTL				REG_CPUAXG_TM	62
J10A	VR_CTL_PHY	VR_CTL				REG_CPUAXG_TCOMP	62
J10A	VR_CTL_PHY	VR_CTL				REG_CPUAXG_SW_FREQ	62
J10C	VR_VID_PHY	VR_VID				CPU_VIDSCLK	13 62
J10C	VR_VID_PHY	VR_VID				CPU_VIDSCLK_R	13
J10C	VR_VID_PHY	VR_VID				CPU_VIDALERT_L	13 62
J10C	VR_VID_PHY	VR_VID				CPU_VIDALERT_R_L	13
J10C	VR_VID_PHY	VR_VID				CPU_VIDSOUT	13 62
J10C	VR_VID_PHY	VR_VID				CPU_VIDSOUT_R	13
Output Bus							
J10C	POWER	POWER	1.1V			PPVCORE_S0_CPU	6
J10A	POWER	POWER	1.1V			PPVAXG_S0	6

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GPU Core Phases and Controller

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
U129	POWER	POWER	12V			REG_PVCC_U8900 80
U129	POWER	POWER	5V			REG_VCC_U8900 80
Phase 1						
U127	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_1 80
U127	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUCORE_1 80
U127	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_1_RC 80
U129	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_1 80
U129	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_GPUCORE_1 80
U129	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_ISEN_GPUCORE_1 80
U129	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_GPUCORE_1 80
Phase 2						
U129	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_2 80
U129	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUCORE_2 80
U130	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_2_RC 80
U130	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_2 80
U130	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_GPUCORE_2 80
U130	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_ISEN_GPUCORE_2 80
U130	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_GPUCORE_2 80
ISL6568						
U127	VR_CTL_PHY	VR_CTL				REG_GPUCORE_ICOMP 80
U127	VR_CTL_PHY	VR_CTL				REG_GPUCORE_OCSET 80
U129	VR_CTL_PHY	VR_CTL				GPUCORE_ICOMP_R 80
U129	VR_CTL_PHY	VR_CTL				REG_GPUCORE_IREF 80
U129	VR_CTL_PHY	VR_CTL				REG_GPUCORE_ISUM 80
U126	VR_CTL_PHY	VR_CTL				REG_GPUCORE_COMP 80
U126	VR_CTL_PHY	VR_CTL				GPUCORE_COMP_RC 80
U126	VR_CTL_PHY	VR_CTL				REG_GPUCORE_VDIFF 80
U131	VR_CTL_PHY	VR_CTL				GPUCORE_VDIFF_R 80
U131	VR_CTL_PHY	VR_CTL				GPUCORE_VDIFF_RC 80
U131	VR_CTL_PHY	VR_CTL				REG_GPUCORE_FB 80
U130 VSNS_GPU_CORE	SNS_DIFF_PHY	SENSE				SNS_GPU_CORE_P 79 80
U130 VSNS_GPU_CORE	SNS_DIFF_PHY	SENSE				SNS_GPU_CORE_N 79 80
U131		SENSE				REG_GPUCORE_VSEN 80
U131		SENSE				REG_GPUCORE_RGND 80
U131	VR_VID_PHY	VR_VID				REG_GPUCORE_VID4 80
U131	VR_VID_PHY	VR_VID				REG_GPUCORE_VID3 80
U131	VR_VID_PHY	VR_VID				REG_GPUCORE_VID2 80
U131	VR_VID_PHY	VR_VID				REG_GPUCORE_VID1 80
U132	VR_VID_PHY	VR_VID				REG_GPUCORE_VID0 80
U132	VR_CTL_PHY	VR_CTL				REG_GPUCORE_MODE 80
U132	VR_CTL_PHY	VR_CTL				REG_GPUCORE_REF 80
U132	VR_CTL_PHY	VR_CTL				REG_GPUCORE_OFS 80
U132	VR_CTL_PHY	VR_CTL				REG_GPUCORE_FS 80
Output Bus						
U122	POWER	POWER	1.0V			PPVCORE_S0_GPU 6

GPU 1.05V S0

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
U139	POWER	POWER	5V			REG_VCC_U8300 74
Local Ground						
U139	GND	GND	0V			P1V05_GPU_AGND 74
1.05V S0						
U135	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPU_P1V05S0 74
U135	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPU_P1V05S0_L 74
U135	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPU_P1V05S0 74
U137	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPU_P1V05S0_RC 74
U140	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPU_P1V05S0 74
U140	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPU_P1V05S0_R 74
U140	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_GPU_P1V05S0 74
U141	VR_CTL_PHY	VR_CTL				REG_GPU_P1V05S0_OCSET_R 74
U141	VR_CTL_PHY	VR_CTL				REG_GPU_P1V05S0_VO_R 74
U140	VR_CTL_PHY	VR_CTL				REG_GPU_P1V05S0_OCSET 74
U140	VR_CTL_PHY	VR_CTL				REG_GPU_P1V05S0_VO 74
U140 VSNS_GPU_P1V05	SNS_DIFF_PHY	SENSE				SNS_GPU_PEX_IOVDD_P 74 79
U140 VSNS_GPU_P1V05	SNS_DIFF_PHY	SENSE				SNS_GPU_PEX_IOVDD_N 74 79
U141		SENSE				REG_GPU_P1V05S0_FB 74
U141		SENSE				REG_GPU_P1V05S0_RTN 74
U141	VR_CTL_PHY	VR_CTL				REG_GPU_P1V05S0_SREF 74
U141	VR_CTL_PHY	VR_CTL				REG_GPU_P1V05S0_FSEL 74
Output Bus						
U141	POWER	POWER	1.05V			PP1V05_S0_GPU 6

GPU VDDQ

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
U143	POWER	POWER	5V			REG_VCC_U8350 74
U143	POWER	POWER	5V			REG_PVCC_U8350 74
Local Ground						
U143	GND	GND	0V			AGND_GPUVDDQ 74
GPU VDDQ						
U142	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUVDDQ 74
U142	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUVDDQ 74
U142	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUVDDQ_RC 74
U142	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUVDDQ 74
U142	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_GPUVDDQ 74
U142	VR_CTL_PHY	VR_CTL				REG_GPUVDDQ_OCSET 74
U142	VR_CTL_PHY	VR_CTL				REG_GPUVDDQ_VO 74
U143 VSNS_GPU_VDDQ	SNS_DIFF_PHY	SENSE				SNS_GPUVDDQ_P 73 74
U143 VSNS_GPU_VDDQ	SNS_DIFF_PHY	SENSE				SNS_GPUVDDQ_N 73 74
U143		SENSE				REG_GPUVDDQ_FB 74
U143		SENSE				REG_GPUVDDQ_RTN 74
U143	VR_CTL_PHY	VR_CTL				REG_GPUVDDQ_SREF 74
U143	VR_CTL_PHY	VR_CTL				REG_GPUVDDQ_FSEL 74
U144	VR_CTL_PHY	VR_CTL				REG_GPUVDDQ_SET0 74
U144	VR_CTL_PHY	VR_CTL				REG_GPUVDDQ_SET1 74
U144	VR_CTL_PHY	VR_CTL				REG_GPUVDDQ_SET1_R 74
Output Bus						
U144	POWER	POWER	1.5V			PPVDDQ_S0_GPU 6

3.3V S5/5V S4

Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus					
U144 POWER	POWER	12V			REG_VIN_U7600 67
U129 POWER	POWER	5V			REG_VCC1_U7600 67
U129 POWER	POWER	5V			REG_VCC2_U7600 67
3.3V S5					
U144 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P3V3S5 67
U144 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P3V3S5 67
U053 VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P3V3S5_RC 67
U048 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P3V3S5 67
U050 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_P3V3S5 67
U052 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P3V3S5 67
U107 VR_CTL_PHY	VR_CTL				REG_P3V3S5_ISEN 67
U100 VR_CTL_PHY	VR_CTL				REG_P3V3S5_OCSET 67
U118 VR_CTL_PHY	VR_CTL				REG_P3V3S5_FSET 67
U100 VR_CTL_PHY	VR_CTL				REG_P3V3S5_VOUT 67
U107 VR_CTL_PHY	VR_CTL				REG_P3V3S5_VOUT_R 67
U107 VR_CTL_PHY	VR_CTL				REG_P3V3S5_FB 67
5V S3					
U113 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P5VS4 67
U113 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P5VS4 67
U113 VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P5VS4_RC 67
U114 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P5VS4 67
U114 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_P5VS4 67
U114 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P5VS4 67
U113 VR_CTL_PHY	VR_CTL				REG_P5VS4_ISEN 67
U113 VR_CTL_PHY	VR_CTL				REG_P5VS4_OCSET 67
U114 VR_CTL_PHY	VR_CTL				REG_P5VS4_FSET 67
U118 VR_CTL_PHY	VR_CTL				REG_P5VS4_VOUT 67
U113 VR_CTL_PHY	VR_CTL				REG_P5VS4_VOUT_R 67
U114 VR_CTL_PHY	VR_CTL				REG_P5VS4_FB 67
Output Bus					
U115 POWER	POWER	5V			PP5V_S5 6
U115 POWER	POWER	5V			PP5V_S4 6
U114 POWER	POWER	3.3V			PP3V3_S5 6
FET Switched					
U122 POWER	POWER	5V			PP5V_S0 6
U122 POWER	POWER	3.3V			PP3V3_S4 6
U122 POWER	POWER	3.3V			PP3V3_S0 6
U145 POWER	POWER	3.3V			PP3V3_S0_SSD 6
U122 POWER	POWER	3.3V			PP3V3_ENET 6
U130 POWER	POWER	3.3V			PP3V3_TBTLC 6
Sensed					
U145 POWER	POWER	3.3V			PPSSD_S0 6

DDR3 Vref

Physical	Spacing	Voltage	DIDT	NO_TEST	
Memory Vref					
U133 POWER	POWER	3.3V			PP3V3_S4_VREFMRGN_DAC 32
U133 POWER	POWER	3.3V			PP3V3_S4_VREFMRGN_CTRL 32
U133 POWER_DDR	POWER_DDR	0.75V			PPDDRVREF_DQ_MEM_A_S3 6
U133 POWER_DDR	POWER_DDR	0.75V			PPDDRVREF_DQ_MEM_B_S3 6
U133 POWER_DDR	POWER_DDR	0.75V			PPDDRVREF_CA_MEM_A_S3 6
U133 POWER_DDR	POWER_DDR	0.75V			PPDDRVREF_CA_MEM_B_S3 6
U145 POWER_DDR	POWER_DDR	0.75V			CPU_DIMM_VREF_DAC_A 11 32
U145 POWER_DDR	POWER_DDR	0.75V			CPU_DIMM_VREF_DAC_B 11 32
U130 POWER_DDR	POWER_DDR	0.75V			CPU_DDR_VREF 11

3.42V G3H

Physical	Spacing	Voltage	DIDT	NO_TEST	
3.42V G3H					
U144 POWER	VR_SWITCH	12V			P3V42G3H_BOOST 69
U144 POWER	VR_SWITCH	12V			P3V42G3H_SW 69
U144 VR_CTL_PHY	VR_CTL				P3V42G3H_FB 69
U144 VR_CTL_PHY	VR_CTL				P3V42G3H_SHDN_L 69
Output Bus					
U144 POWER	POWER	3.425V			PP3V42_G3H 6

1.8V S0

Physical	Spacing	Voltage	DIDT	NO_TEST	
1.8V S0					
U116 POWER	VR_SWITCH	5V			REG_PHASE_P1V8S0 68
U116 VR_CTL_PHY	VR_CTL				REG_P1V8S0_VFB 68
U116 VR_CTL_PHY	VR_CTL				REG_P1V8S0_SYNCH 68
Output Bus					
U116 POWER	POWER	1.8V			PP1V8_S0 6

HDD S0

Physical	Spacing	Voltage	DIDT	NO_TEST	
HDD S0					
U139 POWER	POWER	5V			PPHDD_S0 6

12V

Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus					
U114 POWER	POWER	12V			PP12V_ACDC 6
FET Switched					
U124 POWER	POWER	12V			PP12V_S5 6
U124 POWER	POWER	12V			PP12V_S0 6
Sensed					
U145 POWER	POWER	12V			PP12V_G3H 6
U145 POWER	POWER	12V			PP12V_S0_GPUCORE 6
U145 POWER	POWER	12V			PP12V_S0_GPUUNCORE 6

Ground/Common

Physical	Spacing	Voltage	DIDT	NO_TEST	
Common					
U132 GND	GND	0V			GND

SYNC_MASTER=D7_DAVE SYNC_DATE=12/12/2011

PAGE TITLE: Platform VReg Constraints

Apple Inc.

DRAWING NUMBER: 051-9509 SIZE: D

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Thunderbolt

Thunderbolt-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TBT_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TBTDP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Thunderbolt-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_I2C	*	=2x_DIELECTRIC	?
TBT_SPI	*	=2x_DIELECTRIC	?
TBTDP	*	=5x_DIELECTRIC	?
TBTDP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

DisplayPort

DP-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.08MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

DP-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3:1_SPACING	?

Pairs should be within 100 mils of clock length.
Max length of DisplayPort traces: 12 inches

DisplayPort intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DisplayPort AUX channel intra-pair matching should be 5 ps. No relationship to other signals.

TBT IC Net Properties

	Electrical Contraint Set	Physical	Spacing		
I651		DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	34 77
I652		DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	34 77
I653	DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	34
I654	DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	34
I655		DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_P	34 71
I656		DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_N	34 71
I657	DP_TBTSNK0_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_P	34
I658	DP_TBTSNK0_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_N	34
I659		DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	34 77
I6A1		DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	34 77
I6A0	DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	34
I6A2	DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	34
I6A3		DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_P	34 71
I6A4		DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_N	34 71
I6A5	DP_TBTSNK1_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_P	34
I6A6	DP_TBTSNK1_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_N	34
I6B0	DP_INTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_P<3..0>	82
I6B1	DP_INTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_N<3..0>	82
I6B2	DP_INTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>	82
I6B3	DP_INTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>	82
I6B4	DP_INTPNL_TBT_AUX_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_P	82
I6B5	DP_INTPNL_TBT_AUX_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_N	82
I6B6		DP_85D	DISPLAYPORT	DP_TBTSRC_AUX_C_P	82
I6B7		DP_85D	DISPLAYPORT	DP_TBTSRC_AUX_C_N	82
I6A7		TBT_I2C_55S	TBT_I2C	=I2C_TBTRTR_SCL	34 47
I6A8		TBT_I2C_55S	TBT_I2C	=I2C_TBTRTR_SDA	34 47
I6A9	TBT_SPI_CLK	TBT_SPI_55S	TBT_SPI	TBT_SPI_CLK	34
I6AA	TBT_SPI_MOSI	TBT_SPI_55S	TBT_SPI	TBT_SPI_MOSI	34
I6AB	TBT_SPI_MISO	TBT_SPI_55S	TBT_SPI	TBT_SPI_MISO	34
I6AC	TBT_SPI_CS_L	TBT_SPI_55S	TBT_SPI	TBT_SPI_CS_L	34

*: Only used on hosts supporting T29 video-in

DisplayPort

	Electrical Contraint Set	Physical	Spacing		
	Graphics Source				
I6A9	DP_INTPNL_EG_ML_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_ML_P<1..0>	77 82
I6AA	DP_INTPNL_EG_ML_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_ML_N<1..0>	77 82
I6AB	DP_INTPNL_EG_AUX_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_P	77 82
I6AC	DP_INTPNL_EG_AUX_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_N	77 82
I6AD		DP_85D	DISPLAYPORT	DP_INT_EG_AUX_C_P	82
I6AE		DP_85D	DISPLAYPORT	DP_INT_EG_AUX_C_N	82
	Internal Panel				
I6B8		DP_85D	DISPLAYPORT	DP_INTPNL_ML_C_P<3..0>	82
I6B9		DP_85D	DISPLAYPORT	DP_INTPNL_ML_C_N<3..0>	82
I6BA	DP_INTPNL_ML_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_ML_P<3..0>	81 82
I6BB	DP_INTPNL_ML_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_ML_N<3..0>	81 82
I6BC	DP_INTPNL_AUX_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_P	81 82
I6BD	DP_INTPNL_AUX_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_N	81 82
	Internal DP SPDIF				
I6BE			HDA	DP_INT_SPDIF_AUDIO	52 81

TBT/DP Net Properties

	Electrical Contraint Set	Physical	Spacing		
	Port A				
I6C1	TBT_A_R2D	TBTDP_90D	TBTDP	TBT_A_R2D_C_P<1..0>	34 84
I6C2	TBT_A_R2D	TBTDP_90D	TBTDP	TBT_A_R2D_C_N<1..0>	34 84
I6C3		TBTDP_90D	TBTDP	TBT_A_R2D_P<1..0>	84
I6C4		TBTDP_90D	TBTDP	TBT_A_R2D_N<1..0>	84
I6C5	DP_TBTPA_ML1	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<1>	34 84
I6C6	DP_TBTPA_ML1	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<1>	34 84
I6C7	DP_TBTPA_ML3	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3>	34 84
I6C8	DP_TBTPA_ML3	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3>	34 84
I6C9		DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<1>	84
I6CA		DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<1>	84
I6CB		DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3>	84
I6CC		DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3>	84
I6CD	DP_A_LSX	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1>	84
I6CE	DP_A_LSX	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1>	84
I6CF		TBTDP_90D	TBTDP	TBT_A_D2R_C_P<1..0>	84
I6D0		TBTDP_90D	TBTDP	TBT_A_D2R_C_N<1..0>	84
I6D1	TBT_A_D2R1	TBTDP_90D	TBTDP	TBT_A_D2R_P<1>	34 84
I6D2	TBT_A_D2R1	TBTDP_90D	TBTDP	TBT_A_D2R_N<1>	34 84
I6D3	TBT_A_D2R0	TBTDP_90D	TBTDP	TBT_A_D2R_P<0>	34 84
I6D4	TBT_A_D2R0	TBTDP_90D	TBTDP	TBT_A_D2R_N<0>	34 84
I6D5	TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_P	34 84
I6D6	TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_N	34 84
I6D7		DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_P	84
I6D8		DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_N	84
I6D9	DP_A_AUXCH_DDC	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_P	84
I6DA	DP_A_AUXCH_DDC	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_N	84
I6DB		TBTDP_90D	TBTDP	TBT_A_D2R1_AUXDDC_P	84
I6DC		TBTDP_90D	TBTDP	TBT_A_D2R1_AUXDDC_N	84
	Port B				
I6E0	TBT_B_R2D	TBTDP_90D	TBTDP	TBT_B_R2D_C_P<1..0>	34 85
I6E1	TBT_B_R2D	TBTDP_90D	TBTDP	TBT_B_R2D_C_N<1..0>	34 85
I6E2		TBTDP_90D	TBTDP	TBT_B_R2D_P<1..0>	85
I6E3		TBTDP_90D	TBTDP	TBT_B_R2D_N<1..0>	85
I6E4	DP_TBTPB_ML1	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<1>	34 85
I6E5	DP_TBTPB_ML1	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<1>	34 85
I6E6	DP_TBTPB_ML3	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3>	34 85
I6E7	DP_TBTPB_ML3	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3>	34 85
I6E8		DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<1>	85
I6E9		DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<1>	85
I6EA		DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3>	85
I6EB		DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3>	85
I6EC	DP_B_LSX	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1>	85
I6ED	DP_B_LSX	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1>	85
I6EE		TBTDP_90D	TBTDP	TBT_B_D2R_C_P<1..0>	85
I6EF		TBTDP_90D	TBTDP	TBT_B_D2R_C_N<1..0>	85
I6F0	TBT_B_D2R1	TBTDP_90D	TBTDP	TBT_B_D2R_P<1>	34 85
I6F1	TBT_B_D2R1	TBTDP_90D	TBTDP	TBT_B_D2R_N<1>	34 85
I6F2	TBT_B_D2R0	TBTDP_90D	TBTDP	TBT_B_D2R_P<0>	34 85
I6F3	TBT_B_D2R0	TBTDP_90D	TBTDP	TBT_B_D2R_N<0>	34 85
I6F4	TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_P	34 85
I6F5	TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_N	34 85
I6F6		DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_P	85
I6F7		DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_N	85
I6F8	DP_B_AUXCH_DDC	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_P	85
I6F9	DP_B_AUXCH_DDC	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_N	85
I6FA		TBTDP_90D	TBTDP	TBT_B_D2R1_AUXDDC_P	85
I6FB		TBTDP_90D	TBTDP	TBT_B_D2R1_AUXDDC_N	85

SYNC MASTER=D7 NICK SYNC DATE=12/13/2011

PAGE TITLE

TBT/DP Constraints

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GDDR5

GDDR5-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12 MM	=STANDARD	=STANDARD
GDDR_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GDDR_MA_PHY	*	GDDR_45S
GDDR_ADBI_PHY	*	GDDR_45S
GDDR_CTRL_PHY	*	GDDR_45S
GDDR_CLK_PHY	*	GDDR_80D
GDDR_DQ_PHY	*	GDDR_45S
GDDR_EDC_PHY	*	GDDR_45S
GDDR_DBI_PHY	*	GDDR_45S
GDDR_WCK_PHY	*	GDDR_80D

Main Segment Min Spacing Rules for 4.5 Gbps or Less (AMD Doc# 49919)

	Trace-to-Trace				Isolation				
Table	Micro	Design	Strip	Design	Micro	Design	Strip	Design	Comments
5-6/5-7	2:1	2:1	2:1	2:1	5:1	5:1	5:1	5:1	Memory address (MA). Implented 4.5 Gbps or less rules for K70.
5-6/5-7	2:1	2:1	2:1	2:1	5:1	5:1	5:1	5:1	Address dynamic bus inversion (ADBI)
5-6/5-7	2:1	2:1	2:1	2:1	5:1	5:1	5:1	5:1	Control (CTRL)
5-6/5-7	5:1	5:1	5:1	5:1	5:1	5:1	5:1	5:1	Clock (CLK)
5-6/5-7	3:1	3:1	3:1	3:1	5:1	5:1	5:1	5:1	Data (DQ)
5-6/5-7	7:1	7:1	7:1	7:1	7:1	7:1	7:1	7:1	Error detection pins (EDC). Using larger isolation rules,
5-6/5-7	3:1	3:1	3:1	3:1	5:1	5:1	5:1	5:1	Data dynamic bus inversion (DBI)
5-6/5-7	5:1	5:1	5:1	5:1	5:1	5:1	5:1	5:1	Forwarded clock (WCK)

GDDR5-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR_ISO	*	=5x_DIELECTRIC	?
GDDR_ISO	TOP,BOTTOM	=5x_DIELECTRIC	?
GDDR_MA2MA	*	=2x_DIELECTRIC	?
GDDR_MA2MA	TOP,BOTTOM	=2x_DIELECTRIC	?
GDDR_ADBI2ADBI	*	=2x_DIELECTRIC	?
GDDR_ADBI2ADBI	TOP,BOTTOM	=2x_DIELECTRIC	?
GDDR_CTRL2CTRL	*	=2x_DIELECTRIC	?
GDDR_CTRL2CTRL	TOP,BOTTOM	=2x_DIELECTRIC	?
GDDR_CLK2CLK	*	=5x_DIELECTRIC	?
GDDR_CLK2CLK	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR_DQ2DQ	*	=3x_DIELECTRIC	?
GDDR_DQ2DQ	TOP,BOTTOM	=3x_DIELECTRIC	?
GDDR_EDC_ISO	*	=7x_DIELECTRIC	?
GDDR_EDC_ISO	TOP,BOTTOM	=7x_DIELECTRIC	?
GDDR_EDC2EDC	*	=7x_DIELECTRIC	?
GDDR_EDC2EDC	TOP,BOTTOM	=7x_DIELECTRIC	?
GDDR_DBI2DBI	*	=3x_DIELECTRIC	?
GDDR_DBI2DBI	TOP,BOTTOM	=3x_DIELECTRIC	?
GDDR_WCK2WCK	*	=5x_DIELECTRIC	?
GDDR_WCK2WCK	TOP,BOTTOM	=5x_DIELECTRIC	?

Constraints (x in {A, B}, y in {0, 1})

Memory Address: MAxy[8:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_MA	*	*	GDDR_ISO
GDDR_*_*_MA	=SAME	*	GDDR_MA2MA

Data: DQxy[31:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_DQ	*	*	GDDR_ISO
GDDR_*_*_DQ	=SAME	*	GDDR_DQ2DQ

Address Dynamic Bus Inversion: ADBIxy

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_ADBI	*	*	GDDR_ISO
GDDR_*_*_ADBI	=SAME	*	GDDR_ADBI2ADBI

Error Detection: EDCxy[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_EDC	*	*	GDDR_EDC_ISO
GDDR_*_*_EDC	=SAME	*	GDDR_EDC2EDC

Control: Reset, CKExy, CSxy, WExy, RASxy, CASxy

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_CTRL	*	*	GDDR_ISO
GDDR_*_*_CTRL	*	*	GDDR_ISO
GDDR_*_*_CTRL	=SAME	*	GDDR_CTRL2CTRL

Data Dynamic Bus Inversion: DDBIxy[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_DBI	*	*	GDDR_ISO
GDDR_*_*_DBI	=SAME	*	GDDR_DBI2DBI

Clock: CKxy

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_CLK	*	*	GDDR_ISO
GDDR_*_*_CLK	=SAME	*	GDDR_CLK2CLK

Forwarded Clock: WCKxy[1:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_WCK	*	*	GDDR_ISO
GDDR_*_*_WCK	=SAME	*	GDDR_WCK2WCK

GDDR5 Frame Buffer A

Electrical Contraint Set	Physical	Spacing		
Memory Address				
164 GDDR_A0_MA	GDDR_MA_PHY	GDDR_A_0_MA	FB_A0_A<8..0>	?3 ?5
164 GDDR_A1_MA	GDDR_MA_PHY	GDDR_A_1_MA	FB_A1_A<8..0>	?3 ?5
Address Dynamic Bus Inv				
164 GDDR_A0_ADBI	GDDR_ADBI_PHY	GDDR_A_0_ADBI	FB_A0_ABI_L	?3 ?5
164 GDDR_A1_ADBI	GDDR_ADBI_PHY	GDDR_A_1_ADBI	FB_A1_ABI_L	?3 ?5
Control				
164 GDDR_A0_CKE	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_CKE_L	?3 ?5
164 GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_CS_L	?3 ?5
164 GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_WE_L	?3 ?5
165 GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_CAS_L	?3 ?5
165 GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_RAS_L	?3 ?5
165 GDDR_A1_CKE	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_CKE_L	?3 ?5
165 GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_CS_L	?3 ?5
165 GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_WE_L	?3 ?5
165 GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_CAS_L	?3 ?5
165 GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_RAS_L	?3 ?5
Clock				
165 GDDR_A0_CLK	GDDR_CLK_PHY	GDDR_A_0_CLK	FB_A0_CLK_P	?3 ?5
165 GDDR_A0_CLK	GDDR_CLK_PHY	GDDR_A_0_CLK	FB_A0_CLK_N	?3 ?5
166 GDDR_A1_CLK	GDDR_CLK_PHY	GDDR_A_1_CLK	FB_A1_CLK_P	?3 ?5
165 GDDR_A1_CLK	GDDR_CLK_PHY	GDDR_A_1_CLK	FB_A1_CLK_N	?3 ?5
Data				
166 GDDR_A0_DQ_BYTE0	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<7..0>	?3 ?5
166 GDDR_A0_DQ_BYTE1	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<15..8>	?3 ?5
166 GDDR_A0_DQ_BYTE2	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<23..16>	?3 ?5
166 GDDR_A0_DQ_BYTE3	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<31..24>	?3 ?5
166 GDDR_A1_DQ_BYTE0	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<7..0>	?3 ?5
165 GDDR_A1_DQ_BYTE1	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<15..8>	?3 ?5
166 GDDR_A1_DQ_BYTE2	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<23..16>	?3 ?5
166 GDDR_A1_DQ_BYTE3	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<31..24>	?3 ?5
Error Detection				
167 GDDR_A0_EDC0	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<0>	?3 ?5
166 GDDR_A0_EDC1	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<1>	?3 ?5
167 GDDR_A0_EDC2	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<2>	?3 ?5
167 GDDR_A0_EDC3	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<3>	?3 ?5
167 GDDR_A1_EDC0	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<0>	?3 ?5
167 GDDR_A1_EDC1	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<1>	?3 ?5
167 GDDR_A1_EDC2	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<2>	?3 ?5
167 GDDR_A1_EDC3	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<3>	?3 ?5
Data Dynamic Bus Inv				
167 GDDR_A0_DBI0	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<0>	?3 ?5
167 GDDR_A0_DBI1	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<1>	?3 ?5
168 GDDR_A0_DBI2	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<2>	?3 ?5
167 GDDR_A0_DBI3	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<3>	?3 ?5
168 GDDR_A1_DBI0	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<0>	?3 ?5
168 GDDR_A1_DBI1	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<1>	?3 ?5
168 GDDR_A1_DBI2	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<2>	?3 ?5
168 GDDR_A1_DBI3	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<3>	?3 ?5
Forwarded Clock				
168 GDDR_A0_WCK0	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_P<0>	?3 ?5
168 GDDR_A0_WCK0	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_N<0>	?3 ?5
168 GDDR_A0_WCK1	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_P<1>	?3 ?5
168 GDDR_A0_WCK1	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_N<1>	?3 ?5
168 GDDR_A1_WCK0	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_P<0>	?3 ?5
169 GDDR_A1_WCK0	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_N<0>	?3 ?5
169 GDDR_A1_WCK1	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_P<1>	?3 ?5
169 GDDR_A1_WCK1	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_N<1>	?3 ?5

GDDR5 Frame Buffer B

Electrical Contraint Set	Physical	Spacing		
Memory Address				
169 GDDR_B0_MA	GDDR_MA_PHY	GDDR_B_0_MA	FB_B0_A<8..0>	?3 ?6
169 GDDR_B1_MA	GDDR_MA_PHY	GDDR_B_1_MA	FB_B1_A<8..0>	?3 ?6
Address Dynamic Bus Inv				
169 GDDR_B0_ADBI	GDDR_ADBI_PHY	GDDR_B_0_ADBI	FB_B0_ABI_L	?3 ?6
169 GDDR_B1_ADBI	GDDR_ADBI_PHY	GDDR_B_1_ADBI	FB_B1_ABI_L	?3 ?6
Control				
169 GDDR_B0_CKE	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_CKE_L	?3 ?6
170 GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_CS_L	?3 ?6
170 GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_WE_L	?3 ?6
170 GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_CAS_L	?3 ?6
170 GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_RAS_L	?3 ?6
170 GDDR_B1_CKE	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_CKE_L	?3 ?6
170 GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_CS_L	?3 ?6
170 GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_WE_L	?3 ?6
170 GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_CAS_L	?3 ?6
170 GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_RAS_L	?3 ?6
Clock				
169 GDDR_B0_CLK	GDDR_CLK_PHY	GDDR_B_0_CLK	FB_B0_CLK_P	?3 ?6
171 GDDR_B0_CLK	GDDR_CLK_PHY	GDDR_B_0_CLK	FB_B0_CLK_N	?3 ?6
170 GDDR_B1_CLK	GDDR_CLK_PHY	GDDR_B_1_CLK	FB_B1_CLK_P	?3 ?6
171 GDDR_B1_CLK	GDDR_CLK_PHY	GDDR_B_1_CLK	FB_B1_CLK_N	?3 ?6
Data				
171 GDDR_B0_DQ_BYTE0	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<7..0>	?3 ?6
171 GDDR_B0_DQ_BYTE1	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<15..8>	?3 ?6
171 GDDR_B0_DQ_BYTE2	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<23..16>	?3 ?6
171 GDDR_B0_DQ_BYTE3	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<31..24>	?3 ?6
171 GDDR_B1_DQ_BYTE0	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<7..0>	?3 ?6
171 GDDR_B1_DQ_BYTE1	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<15..8>	?3 ?6
171 GDDR_B1_DQ_BYTE2	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<23..16>	?3 ?6
171 GDDR_B1_DQ_BYTE3	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<31..24>	?3 ?6
Error Detection				
172 GDDR_B0_EDC0	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<0>	?3 ?6
172 GDDR_B0_EDC1	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<1>	?3 ?6
172 GDDR_B0_EDC2	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<2>	?3 ?6
172 GDDR_B0_EDC3	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<3>	?3 ?6
172 GDDR_B1_EDC0	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<0>	?3 ?6
172 GDDR_B1_EDC1	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<1>	?3 ?6
172 GDDR_B1_EDC2	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<2>	?3 ?6
172 GDDR_B1_EDC3	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<3>	?3 ?6
Data Dynamic Bus Inv				
172 GDDR_B0_DBI0	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<0>	?3 ?6
172 GDDR_B0_DBI1	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<1>	?3 ?6
173 GDDR_B0_DBI2	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<2>	?3 ?6
173 GDDR_B0_DBI3	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<3>	?3 ?6
173 GDDR_B1_DBI0	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<0>	?3 ?6
173 GDDR_B1_DBI1	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<1>	?3 ?6
173 GDDR_B1_DBI2	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<2>	?3 ?6
173 GDDR_B1_DBI3	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<3>	?3 ?6
Forwarded Clock				
173 GDDR_B0_WCK0	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_P<0>	?3 ?6
173 GDDR_B0_WCK0	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_N<0>	?3 ?6
173 GDDR_B0_WCK1	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_P<1>	?3 ?6
173 GDDR_B0_WCK1	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_N<1>	?3 ?6
174 GDDR_B1_WCK0	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_P<0>	?3 ?6
174 GDDR_B1_WCK0	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_N<0>	?3 ?6
174 GDDR_B1_WCK1	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_P<1>	?3 ?6
174 GDDR_B1_WCK1	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_N<1>	?3 ?6

GPU Misc.

Electrical Contraint Set	Physical	Spacing		
SMB				
154	SMB_PHY	SMB	GPU_SMB_CLK	?7 ?8
154	SMB_PHY	SMB	GPU_SMB_DAT	?7 ?8
154	SMB_PHY	SMB	GPU_SMB_CLK_R	47 ?8
154	SMB_PHY	SMB	GPU_SMB_DAT_R	47 ?8

Frame Buffer Reset

Electrical Contraint Set	Physical	Spacing		
Reset				
174 GDDR_A0_RESET	GDDR_50S	GDDR_CTRL	FB_A0_RESET_L	?3 ?5
174 GDDR_A1_RESET	GDDR_50S	GDDR_CTRL	FB_A1_RESET_L	?3 ?5
174 GDDR_B0_RESET	GDDR_50S	GDDR_CTRL	FB_B0_RESET_L	?3 ?6
174 GDDR_B1_RESET	GDDR_50S	GDDR_CTRL	FB_B1_RESET_L	?3 ?6

SYNC_MASTER=D7 DAVE SYNC_DATE=12/12/2011

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Backlight Controller

BLC-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BLC_P6MM	*	Y	0.600 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD
BLC_P3MM	*	Y	0.300 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER_BLC	*	BLC_P6MM
POWER_BLC_RET	*	BLC_P3MM
BLC_CTL_PHY	*	BLC_P3MM

BLC-specific Spacing Definitions
BLC High Voltage Output

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BLC_HV_ISO	*	0.45mm	1000

Constraints
BLC High Voltage Output

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_HV	BLC_CTL	*	BLC_CTL_ISO
BLC_HV	BLC_HV	*	BLC_CTL_ISO
BLC_HV	*	*	BLC_HV_ISO

BLC Baddies

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PHASE_ISO	*	=8:1_SPACING	2000
PHASE_SW2SW	*	=1:1_SPACING	?
PHASE_SW2PWR	*	=2:1_SPACING	?
PHASE_SW2GND	*	=2:1_SPACING	?

BLC Baddies

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_PHASE	*	*	PHASE_ISO
BLC_PHASE	BLC_PHASE	*	PHASE_SW2SW
BLC_PHASE	POWER	*	PHASE_SW2PWR
BLC_PHASE	GND	*	PHASE_SW2GND

BLC Control

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BLC_CTL_ISO	*	=3:1_SPACING	?

BLC Control

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_CTL	*	*	BLC_CTL_ISO

Is it chel'oh or sel'oh?

	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
B24	POWER	POWER	12V			PP12V_S0_BKLT_FUSED
B25	POWER	POWER	12V			PP12V_S0_BKLT_FILT
B27	POWER	POWER	12V			PP12V_S0_BKLT_PWR
B28	POWER	POWER	12V			PP12V_S0_BKLT_PWR_R
B29	POWER	POWER	5V			PP5V_S0_BKLT_R
B30	POWER	POWER	3.3V			PP3V3_S0_BKLT_VDDIO_R
Local Ground						
B53	BLC_CTL_PHY	BLC_PHASE	0V			PGND_BKLT
B79	BLC_CTL_PHY	BLC_PHASE	0V			DGND_BKLT
B80	BLC_CTL_PHY	BLC_PHASE	0V			LGND_BKLT
Backlight						
B52	POWER_BLC	BLC_PHASE	80V	TRUE		BKLT_PHASE
B54	BLC_CTL_PHY	BLC_PHASE	80V	TRUE		BKLT_GATE
B55	BLC_CTL_PHY	BLC_PHASE	80V	TRUE		BKLT_GATE_R
B56	BLC_CTL_PHY	BLC_PHASE	80V	TRUE	TRUE	BKLT_SNUBBER
B57	BLC_CTL_PHY	BLC_PHASE	12V	TRUE		BKLT_SW_R
B58	BLC_CTL_PHY	BLC_CTL				BKLT_ISET
B76	BLC_CTL_PHY	BLC_CTL				BKLT_FLT
B75	BLC_CTL_PHY	BLC_CTL				BKLT_FLT_RC
B77	SNS_DIFF_PHY	SENSE				BKLT_SW_P
B78	SNS_DIFF_PHY	SENSE				BKLT_SW_N
B62		SENSE				BKLT_FB
B59		BLC_HV	67V			BKLT_FB_XW
B74		BLC_HV	67V			BKLT_FB_R
B70	POWER_BLC_RET	BLC_CTL				BKLT_ISEN1
B69	POWER_BLC_RET	BLC_CTL				BKLT_ISEN2
B68	POWER_BLC_RET	BLC_CTL				BKLT_ISEN3
B67	POWER_BLC_RET	BLC_CTL				BKLT_ISEN4
B66	POWER_BLC_RET	BLC_CTL				BKLT_ISEN5
B65	POWER_BLC_RET	BLC_CTL				BKLT_ISEN6
B48	POWER_BLC_RET	BLC_HV				BKLT_ISEN1_R
B49	POWER_BLC_RET	BLC_HV				BKLT_ISEN2_R
B50	POWER_BLC_RET	BLC_HV				BKLT_ISEN3_R
B51	POWER_BLC_RET	BLC_HV				BKLT_ISEN4_R
B52	POWER_BLC_RET	BLC_HV				BKLT_ISEN5_R
B53	POWER_BLC_RET	BLC_HV				BKLT_ISEN6_R
B39	POWER_BLC_RET	BLC_HV				LED_RETURN_1
B38	POWER_BLC_RET	BLC_HV				LED_RETURN_2
B36	POWER_BLC_RET	BLC_HV				LED_RETURN_3
B35	POWER_BLC_RET	BLC_HV				LED_RETURN_4
B34	POWER_BLC_RET	BLC_HV				LED_RETURN_5
B33	POWER_BLC_RET	BLC_HV				LED_RETURN_6
Output Bus						
B60	POWER_BLC	BLC_HV	67V			BKLT_BOOST
B73	POWER_BLC	BLC_HV	67V			BKLT_BOOST_1
B72	POWER_BLC	BLC_HV	67V			BKLT_BOOST_2

Cello Miscellaneous

Electrical Contraint Set	Physical	Spacing	
SPI			
B64	SMB_PHY	SMB	BKLT_SCL
B63	SMB_PHY	SMB	BKLT_SDA

SYNC_MASTER=D7_DAVE SYNC_DATE=12/12/2011

PAGE TITLE: BLC Constraints

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