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<td></td>
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<tr>
<td>18</td>
<td>CPU SM/PCI/ATT/RTC/RTC/SM/PCI/PCI/RTC</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>CPU SM/PCI/ATT/RTC/RTC/PCI/PCI/RTC/RTC</td>
<td></td>
</tr>
<tr>
<td>20</td>
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</tr>
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<td>DEVI v1.0.0 (V)</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>MEMORY CARS</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>DEVI v1.0.0 (V)</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>DEVI v1.0.0 (V)</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>DEVI v1.0.0 (V)</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>PCI-X WIRELESS CONNECTOR</td>
<td></td>
</tr>
<tr>
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<td>USB Slot</td>
<td></td>
</tr>
<tr>
<td>35</td>
<td>USB Slot</td>
<td></td>
</tr>
<tr>
<td>36</td>
<td>ETHERNET (CAGE 11)</td>
<td></td>
</tr>
<tr>
<td>37</td>
<td>CAGE 11 SUPPORT</td>
<td></td>
</tr>
<tr>
<td>38</td>
<td>ETHERNET CONNECTOR</td>
<td></td>
</tr>
<tr>
<td>39</td>
<td>FIREWIRE LLC/PCI (X1022114)</td>
<td></td>
</tr>
<tr>
<td>40</td>
<td>FIREWIRE CONNECTOR</td>
<td></td>
</tr>
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<td></td>
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<td></td>
</tr>
<tr>
<td>44</td>
<td>External USB Connections</td>
<td></td>
</tr>
<tr>
<td>45</td>
<td>Internal USB Connections</td>
<td></td>
</tr>
<tr>
<td>46</td>
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<td></td>
</tr>
<tr>
<td>47</td>
<td>LPC-SPI Debug Connector</td>
<td></td>
</tr>
<tr>
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<td></td>
</tr>
</tbody>
</table>
### BOM Variants

<table>
<thead>
<tr>
<th>BOM GROUP</th>
<th>BOM NAME</th>
<th>BOM OPTIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>321-1409</td>
<td>FOXCONN_CPU_G000</td>
<td>SUBassy,FOXCONN_CPU_G000</td>
</tr>
<tr>
<td>607-6876</td>
<td>FOXCONN_CPU_G000</td>
<td>SUBassy,FOXCONN_CPU_G000</td>
</tr>
<tr>
<td>607-6877</td>
<td>MOLEX_CPU_G000</td>
<td>SUBassy,MOLEX_CPU_G000</td>
</tr>
</tbody>
</table>

### CPU SOCKET & ILM SUB-BOMS

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PART#</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>639-1106</td>
<td>639-1106</td>
<td>ALTERNATE FOR MOLEX CPU SOCKET AND ILM ASSY, PURCHASED, ILM, FOXCONN, K75 SOCKET, LGA1156, CPU-LF</td>
</tr>
<tr>
<td>639-1104</td>
<td>639-1104</td>
<td>ALTERNATE FOR MOLEX CPU SOCKET AND ILM ASSY, PURCHASED, ILM, MOLEX, K75 SOCKET, LGA1156, CPU-LF</td>
</tr>
</tbody>
</table>

### COMMON

<table>
<thead>
<tr>
<th>ITEM</th>
<th>DESCRIPTION</th>
<th>REFERENCE DESIGNATOR(S)</th>
<th>MATERIAL/REMARKS</th>
<th>ASSEMBLY</th>
</tr>
</thead>
<tbody>
<tr>
<td>604-0988</td>
<td>CPUS</td>
<td>U1000</td>
<td>CRITICAL</td>
<td></td>
</tr>
<tr>
<td>511S0069</td>
<td>CPUS</td>
<td>U1000</td>
<td>CRITICAL</td>
<td></td>
</tr>
<tr>
<td>604-0942</td>
<td>CPUS</td>
<td>U1000</td>
<td>CRITICAL</td>
<td></td>
</tr>
</tbody>
</table>

### ALTERNATES

<table>
<thead>
<tr>
<th>ITEM</th>
<th>DESCRIPTION</th>
<th>REFERENCE DESIGNATOR(S)</th>
<th>MATERIAL/REMARKS</th>
<th>ASSEMBLY</th>
</tr>
</thead>
<tbody>
<tr>
<td>337S3828</td>
<td>ILM</td>
<td>U1000</td>
<td>CRITICAL</td>
<td></td>
</tr>
<tr>
<td>337S3861</td>
<td>ILM</td>
<td>U1000</td>
<td>CRITICAL</td>
<td></td>
</tr>
<tr>
<td>337S3910</td>
<td>ILM</td>
<td>U1000</td>
<td>CRITICAL</td>
<td></td>
</tr>
</tbody>
</table>

### BOARD STACK-UP

- **TOP**
  - SIGNAL
  - GROUND
  - POWER
  - DATA
  - GROUND
- **BOTTOM**
  - SIGNAL
  - GROUND

---

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**SYNC_DATE=N/A**

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**APPLE INC.**

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**BOM Configuration**

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### CAN DELETE THESE FOR PROTO1 AND BEYOND

| State                  | Identifiability | PM_SLP_M_L   | PM_SLP_S3_L   | PM_SLP_S4_3_L | PM_PGOOD_PVCORE_CPU | PM_PGOOD_DDRREG_PVCORE_S3 | PM_PGOOD_DDRREG_PVCORE_S4 | PM_PGOOD_DDRREG_PCHCORE | PM_PGOOD_PCHCORE | SMC_PM_G2_ENABLE | PM_S4_STATE_L | PM_SLP_S3_L | PM_SLP_S4_L | PM_PGOOD_S3_L | PM_PGOOD_S4_L | PM_PGOOD_S5_L |
|------------------------|-----------------|---------------|---------------|---------------|---------------------|------------------------|------------------------|------------------------|----------------|----------------|----------------|-------------|-------------|-------------|----------------|----------------|----------------|
| ON                     | 1               | 1             | 1             | 1             | 1                   | 1                      | 1                      | 1                      | 1              | 0              | 1             | 0           | 1           | 1           | 1              | 0              | 0             |
| Sleep (S3/M-Off)       | Off             | 0             | 0             | 1             | 1                   | 1                      | 1                      | 0                      | 0              | 0              | 0             | 0           | 1           | 1           | 0              | 0              | 0             |
| Sleep (S3/M-Off)       | On              | 1             | 1             | 0             | 1                   | 0                      | 0                      | 0                      | 0              | 0              | 0             | 0           | 1           | 1           | 0              | 0              | 0             |
| Manageability (S3/M-Off)| Off             | 1             | 1             | 0             | 1                   | 0                      | 0                      | 0                      | 0              | 0              | 0             | 0           | 1           | 1           | 0              | 0              | 0             |
| Battery Off (S5/M-Off) | Off             | 0             | 0             | 1             | 1                   | 1                      | 1                      | 0                      | 0              | 0              | 0             | 0           | 1           | 1           | 0              | 0              | 0             |

### Table of Components

- **SILK_PART=VCORE_PGOOD**
  - **LED550** Green-3.6MCD 2.0X1.25MM-SM
  - **R520** MF-LF 1/10W 3.3K 5%

- **SILK_PART=SLP_M**
  - **LED520** Green-3.6MCD 2.0X1.25MM-SM
  - **Q520** SOT-363 2N7002DW-X-G

- **SILK_PART=SLP_S3**
  - **LED510** Green-3.6MCD 2.0X1.25MM-SM
  - **Q500** SOT-363 2N7002DW-X-G

- **SILK_PART=SLP_S4**
  - **LED530** Green-3.6MCD 2.0X1.25MM-SM
  - **Q540** SOT-363 2N7002DW-X-G

- **SILK_PART=DDR_PGOOD**
  - **LED540** Green-3.6MCD 2.0X1.25MM-SM
  - **Q540** SOT-363 2N7002DW-X-G

- **SILK_PART=PCHCORE_PGOOD**
  - **LED500** Green-3.6MCD 2.0X1.25MM-SM
  - **Q500** SOT-363 2N7002DW-X-G

- **SILK_PART=SLP_S4**
  - **LED500** Green-3.6MCD 2.0X1.25MM-SM
  - **Q500** SOT-363 2N7002DW-X-G

- **SILK_PART=SLP_S3**
  - **LED510** Green-3.6MCD 2.0X1.25MM-SM
  - **Q510** MF-LF 1/10W 3.3K 5%

- **SILK_PART=SLP_S4**
  - **LED530** Green-3.6MCD 2.0X1.25MM-SM
  - **Q530** MF-LF 1/10W 3.3K 5%

- **SILK_PART=SLP_S3**
  - **LED510** Green-3.6MCD 2.0X1.25MM-SM
  - **Q530** MF-LF 1/10W 3.3K 5%

- **SILK_PART=SLP_S4**
  - **LED530** Green-3.6MCD 2.0X1.25MM-SM
  - **Q530** MF-LF 1/10W 3.3K 5%

- **SILK_PART=SLP_S3**
  - **LED510** Green-3.6MCD 2.0X1.25MM-SM
  - **Q510** MF-LF 1/10W 3.3K 5%

- **SILK_PART=SLP_S4**
  - **LED530** Green-3.6MCD 2.0X1.25MM-SM
  - **Q530** MF-LF 1/10W 3.3K 5%

- **SILK_PART=SLP_S3**
  - **LED510** Green-3.6MCD 2.0X1.25MM-SM
  - **Q510** MF-LF 1/10W 3.3K 5%

- **SILK_PART=SLP_S4**
  - **LED530** Green-3.6MCD 2.0X1.25MM-SM
  - **Q530** MF-LF 1/10W 3.3K 5%
Grounding the Rail because Integrated Graphics won't be used.
Current numbers from Ibex Peak EDS Spec Update rev 0.71, doc #386904 (Table 8-3). Pre-Silicon Mobile Estimates.

MIN_NECK_WIDTH = 0.25MM

PLACE C2400 NEAR BALL AW1
PLACE C2401 NEAR BALL AN1

PLACE C2419 AT BALL AA1
PLACEMENT_NOTE:

PLACE C2420 AT BALL AJ1

PLACE C2421 NEAR BALL AY29
PLACE C2426 NEAR BALL AW39

PLACE C2435 NEAR BALL AE27
PLACE C2437 NEAR BALL A21
PLACE C2438 NEAR BALL AH16
PLACE C2439 NEAR BALL A9

PLACE C2440 NEAR BALL P30
PLACE C2445 NEAR BALL P18
PLACE C2450 NEAR BALL B39

PLACE C2465 NEAR BALL AB15
PLACE C2467 NEAR BALL AH1
PLACE C2468 NEAR BALL AJ4

PLACE C2471 NEAR BALL AE18
PLACE C2472 NEAR BALL AE18
PLACE C2473 NEAR BALL AE18

PLACE C2480 NEAR BALL AE18
PLACE C2485 NEAR BALL AE18

PLACE C2491 NEAR BALL P18
PLACE C2492 NEAR BALL P15
PLACE C2493 NEAR BALL U15
NOTE: DELTA RECOMMENDS CENTER-TAP BE FLOATING

R3900
MF-LF
75
402
1/16W

R3901
MF-LF
75
402
5%

R3902
MF-LF
75
1/16W

R3903
MF-LF
402
5%

C3900
NOSTUFF
1206
1000PF
10%

C3901
402
20%
10V

C3902
402
20%
0.1UF

C3903
402
20%
10V

C3904
402
20%
0.1UF

T3900
LFE9287APF
SOI

J3900
CRITICAL
F-ANG-TH
RJ45-10/100TX-K22

ETHERNET CONNECTOR
SYNC_MASTER=K75F_MLB
SYNC_DATE=04/14/2010

MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.4 MM

NOTE: BOB SMITH TERMINATION FOR EMC INVESTIGATION.

PLACE ONE CAP PER TCT PIN
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5K pull-down device detect circuit.

The FWXIO nets are OHCI/PCIe power, and multi-port systems must come from bus power. The FW_PHY nets are PHY power, and for Power Aliases:

- PLACEMENT_NOTE=Place C4140 close to U1400
- MIN_LINE_WIDTH=0.3 mm
- MIN_NECK_WIDTH=0.2 mm

Power Buses:

- VOLTAGE=3.3V
- 1UF CERM 6.3V
- 220 OHM LF
- 47K OHM
- 1/16W MF-LF
- 390K OHM 5%
- 6.34K OHM 10K

- NC
- SMD
- BI
- BI
- BI
- BI
- BI

- BI
- BI
- BI
- BI
- BI

- BI
- BI
- BI
- BI
- BI
1394 PHY 1.95V SUPPLY

FireWire Aliases For Connectivity

1394 PHY STRAPPING OPTIONS

2ND & 3RD TPA/TPB PAIR UNUSED

There are three Firewire ports, but only one is used. No stuff means that it is to include more full line asserts/balanced data chains only used.
NOTE: Unused pins have "NC," blank. Unused pins designated as inputs can be left floating, those designated as inputs require pullups.

NOTE: SMI interrupt can be active high or low, resolve accordingly. If SMI interrupt is not used, pull up to GND rail.
IBEX PEAK CORE REG 1.05V  OUTPUT = PP1V05_S0_REG

=PP12V_S0_PCH_CORE_VREG

=PP5V_S0_PCH_CORE_VREG

=PP3V3_S0_PCH

PCHCORE_REG_PGOOD

PCHCORE_REG_EN

PCHCORE_REG_BOOT

PCHCORE_REG_TON

PCHCORE_REG_LGATE

PCHCORE_REG_PHASE_C

PCHCORE_REG_BOOT_R

PCHCORE_REG_5V_FLT

PCHCORE_REG_UGATE

PCHCORE_REG_PHASE

PP1V05_S0_REG

OP PSG GOOD

OP PSG REG

PP1V05_S0_REG

PP1V05_S0_REG

MIN LINE WIDTH=0.6MM

MIN TIE_WIDTH=0.2MM

DIDT=TRUE

NET PHYSICAL TYPE=POWER

SWITCHNODE

IBEX PEAK CORE

Apple Inc.

051-8600 D

A.O.S

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Apple Inc.

2005

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1.5 V DDR SUPPLY

Vout = 0.75V * (1 + Ra / Rb)

1.8 V SUPPLY

Vo=0.8*(1+ Ra/Rb)
Vo=0.8*(1+ 59/47)=1.804V
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

Vout = 1.25V * (1 + Ra / Rb)

<Ra>  <Rb>

Vout = 3.425
250mA max output
(Switcher limit)

Remove R7911 after Proto-1

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

Vout = 1.25V * (1 + Ra / Rb)

<Ra>  <Rb>

Vout = 3.425
250mA max output
(Switcher limit)

Remove R7911 after Proto-1

1.05V S5 SUPPLY

REMOVE for K60/K61
Page Notes

Power plane required by this page:
- SMB_MXM_THRM_CLK
- SMB_MXM_THRM_DATA
- PP3V3_S0_MXM

MXM SYSTEM INFORMATION ROM

MXM I/O

Apple Inc.

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PAGE TITLE

SYNC_DATE=04/14/2010

REVISION

051-8600

SIZE

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74 OF 92

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## Unused MXM Interfaces

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Make_Base</th>
<th>No_Test</th>
<th>Signal Alias</th>
</tr>
</thead>
<tbody>
<tr>
<td>MXM_LVDS_B_DATA_P&lt;3&gt;</td>
<td>TRUE</td>
<td>TRUE</td>
<td>NC_MXM_LVDS_B_DATA_P&lt;3&gt;</td>
</tr>
<tr>
<td>MXM_LVDS_B_DATA_N&lt;3&gt;</td>
<td>TRUE</td>
<td>TRUE</td>
<td>NC_MXM_LVDS_B_DATA_N&lt;3&gt;</td>
</tr>
<tr>
<td>MXM_LVDS_B_DATA_P&lt;2&gt;</td>
<td>TRUE</td>
<td>TRUE</td>
<td>NC_MXM_LVDS_B_DATA_P&lt;2&gt;</td>
</tr>
<tr>
<td>MXM_LVDS_B_DATA_N&lt;2&gt;</td>
<td>TRUE</td>
<td>TRUE</td>
<td>NC_MXM_LVDS_B_DATA_N&lt;2&gt;</td>
</tr>
<tr>
<td>MXM_LVDS_B_DATA_P&lt;1&gt;</td>
<td>TRUE</td>
<td>TRUE</td>
<td>NC_MXM_LVDS_B_DATA_P&lt;1&gt;</td>
</tr>
<tr>
<td>MXM_LVDS_B_DATA_N&lt;1&gt;</td>
<td>TRUE</td>
<td>TRUE</td>
<td>NC_MXM_LVDS_B_DATA_N&lt;1&gt;</td>
</tr>
<tr>
<td>MXM_LVDS_B_DATA_P&lt;0&gt;</td>
<td>TRUE</td>
<td>TRUE</td>
<td>NC_MXM_LVDS_B_DATA_P&lt;0&gt;</td>
</tr>
<tr>
<td>MXM_LVDS_B_DATA_N&lt;0&gt;</td>
<td>TRUE</td>
<td>TRUE</td>
<td>NC_MXM_LVDS_B_DATA_N&lt;0&gt;</td>
</tr>
<tr>
<td>MXM_LVDS_B_CLK_P</td>
<td>TRUE</td>
<td>TRUE</td>
<td>NC_MXM_LVDS_B_CLK_P</td>
</tr>
<tr>
<td>MXM_LVDS_B_CLK_N</td>
<td>TRUE</td>
<td>TRUE</td>
<td>NC_MXM_LVDS_B_CLK_N</td>
</tr>
</tbody>
</table>

## Unused MXM DP Interfaces

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Make_Base</th>
<th>No_Test</th>
<th>Signal Alias</th>
</tr>
</thead>
<tbody>
<tr>
<td>MXM_DP_B_ML_P&lt;0..3&gt;</td>
<td>TRUE</td>
<td>TRUE</td>
<td>NC_MXM_DP_B_ML_P&lt;0..3&gt;</td>
</tr>
<tr>
<td>MXM_DP_B_ML_N&lt;0..3&gt;</td>
<td>TRUE</td>
<td>TRUE</td>
<td>NC_MXM_DP_B_ML_N&lt;0..3&gt;</td>
</tr>
<tr>
<td>MXM_DP_B_AUX_P</td>
<td>TRUE</td>
<td>TRUE</td>
<td>NC_MXM_DP_B_AUX_P</td>
</tr>
<tr>
<td>MXM_DP_B_AUX_N</td>
<td>TRUE</td>
<td>TRUE</td>
<td>NC_MXM_DP_B_AUX_N</td>
</tr>
<tr>
<td>MXM_DP_B_HPD</td>
<td>TRUE</td>
<td>TRUE</td>
<td>NC_MXM_DP_B_HPD</td>
</tr>
<tr>
<td>MXM_DP_D_ML_P&lt;0..3&gt;</td>
<td>TRUE</td>
<td>TRUE</td>
<td>NC_MXM_DP_D_ML_P&lt;0..3&gt;</td>
</tr>
<tr>
<td>MXM_DP_D_ML_N&lt;0..3&gt;</td>
<td>TRUE</td>
<td>TRUE</td>
<td>NC_MXM_DP_D_ML_N&lt;0..3&gt;</td>
</tr>
<tr>
<td>MXM_DP_D_AUX_P</td>
<td>TRUE</td>
<td>TRUE</td>
<td>NC_MXM_DP_D_AUX_P</td>
</tr>
<tr>
<td>MXM_DP_D_AUX_N</td>
<td>TRUE</td>
<td>TRUE</td>
<td>NC_MXM_DP_D_AUX_N</td>
</tr>
<tr>
<td>MXM_DP_D_HPD</td>
<td>TRUE</td>
<td>TRUE</td>
<td>NC_MXM_DP_D_HPD</td>
</tr>
</tbody>
</table>
**PHYSICAL_RULE_SET**

**PHYSICAL_RULE_SET**

**PHYSICAL_RULE_SET**

**PHYSICAL_RULE_SET**

**PHYSICAL_RULE_SET**

**PHYSICAL_RULE_SET**

**PHYSICAL_RULE_SET**

**K60/K61 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS**

**SPACING RULE SET**

**SPACING RULE SET**

**SPACING RULE SET**

**SPACING RULE SET**

**SPACING RULE SET**

**SPACING RULE SET**

**K60/K61 RULE DEFINITIONS**

**THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY**

**OF APPLE INC.**
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.

DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.

DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.

Pairs should be within 100 mils of clock length.

**Table:**

<table>
<thead>
<tr>
<th>Pair</th>
<th>Description</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>0-11</td>
<td>LVDS/B_CLK_N</td>
<td><a href="#">Reference</a></td>
</tr>
<tr>
<td>1-22</td>
<td>LVDS/B_CLK_P</td>
<td><a href="#">Reference</a></td>
</tr>
<tr>
<td>2-33</td>
<td>LVDS/A_CLK_N</td>
<td><a href="#">Reference</a></td>
</tr>
<tr>
<td>3-44</td>
<td>LVDS/A_CLK_P</td>
<td><a href="#">Reference</a></td>
</tr>
</tbody>
</table>

**Physical Rule Set:**

```
LINE-TO-LINE SPACING = 85_OHM_DIFF
TABLE_SPACING_RULE_ITEM
```

**Spacing Rule Set:**

```
MINIMUM LINE WEIGHT
```

**Layer:**

```
LAYER 1
```

**Physical Constraints:**

```
MAXIMUM NECK LENGTH = 85_OHM_DIFF
```

### PM NET PROPERTIES

<table>
<thead>
<tr>
<th>Net Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PM</td>
<td></td>
</tr>
<tr>
<td>PM_VTT</td>
<td></td>
</tr>
</tbody>
</table>

### Table Spacing Assignment

#### Table Spacing Assignment Item

<table>
<thead>
<tr>
<th>Item</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>I1</td>
<td></td>
</tr>
</tbody>
</table>