

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.  
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.  
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
4	0001109172	ENGINEERING RELEASED		2011-04-18

# SCHEM, PCB, LIO, K78

## EVT 1, 2011-04-18

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### Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0694	155S0387		ALL	Murata alt to TDK
155S0661	155S0511		ALL	Murata alt to TDK
155S0660	155S0513		ALL	Murata alt to TDK

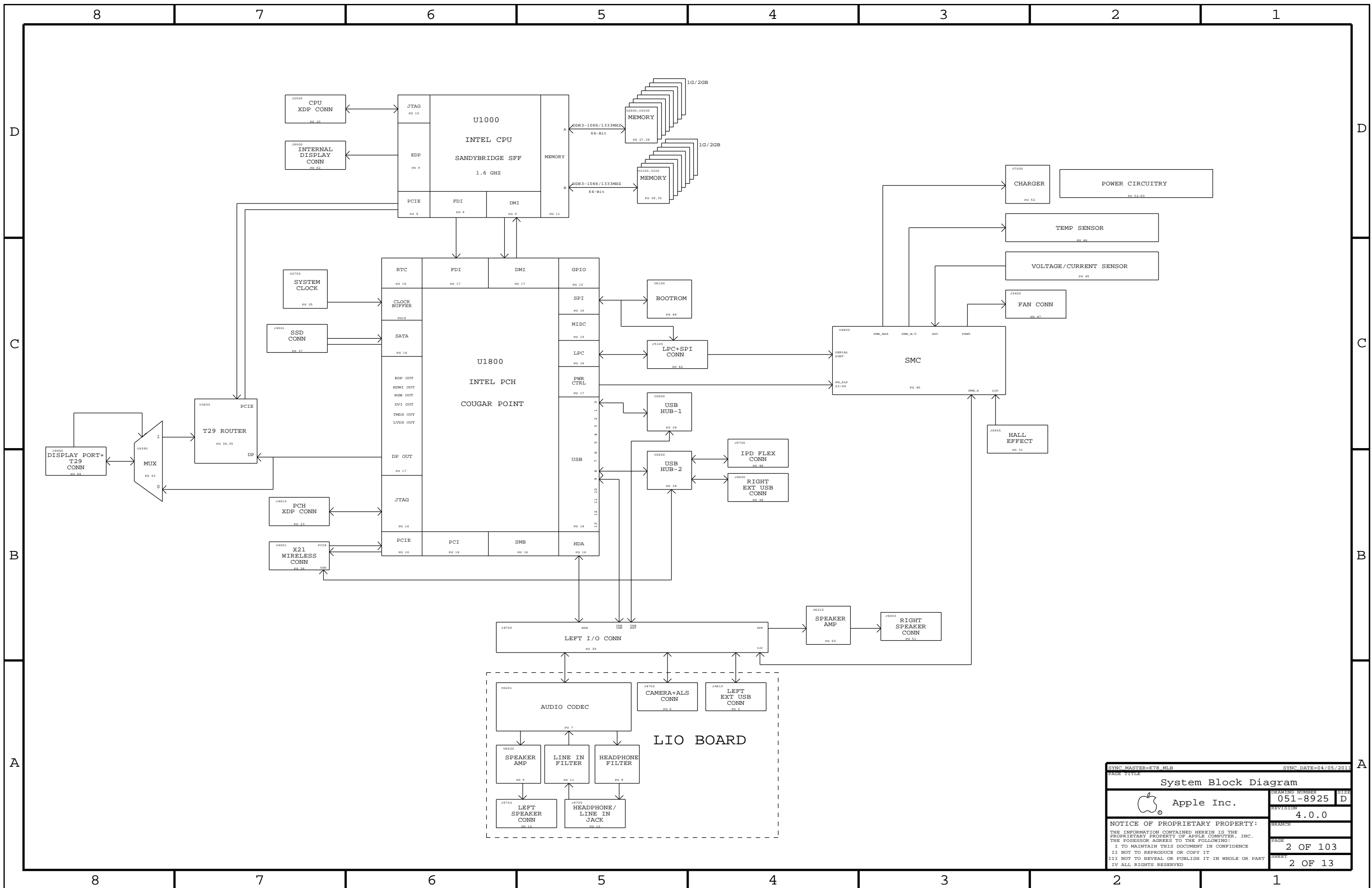
### Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8540	1	SCHEM, PCB, LIO, K78	SCH	CRITICAL	
820-3053	1	PCBF, LIO, K78	PCB	CRITICAL	
946-3092	1	LIO LOCTITE UV EB 0.08, K78	UV_GLUE	CRITICAL	

BOM: 639-1784 PCBA, LIO, K78  
 MCO: 056-4207 MCO, LIO, K78  
 EEEE: DK05

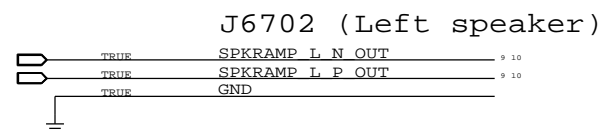
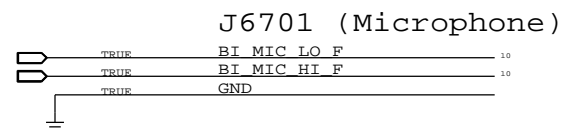
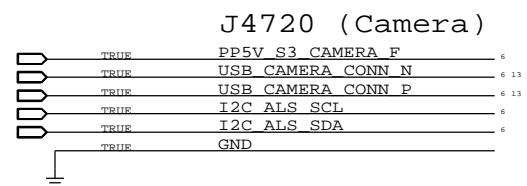
PRODUCT SAFETY REQUIREMENTS:  
 PCB, UL RECOGNIZED, MIN. 130-C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94.  
 PCB TO BE SILKSCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP. RATING AND V-0 FLAME RATING

DRAWING TITLE		DRAWING NUMBER	SIZE
SCHEM, PCB, LIO, K78		051-8925	D
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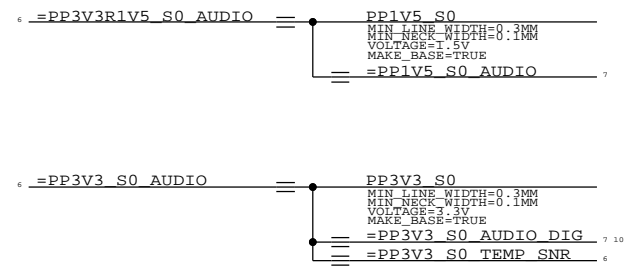
SYNC MASTER=K78_MLB		SYNC DATE=04/05/2011	
PAGE TITLE System Block Diagram			
DRAWING NUMBER 051-8925		SIZE D	
REVISION 4.0.0		BRANCH	
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# Functional Test Points

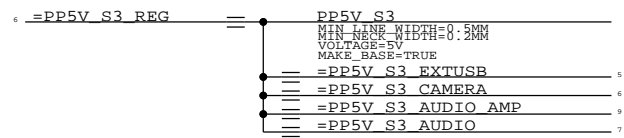


SYNC_MASTER=(K6_MLB)		SYNC_DATE=(12/11/2009)	
PAGE TITLE: <b>FUNC TEST</b>			
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	REVISION	4.0.0	
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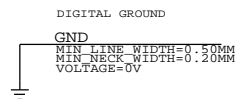
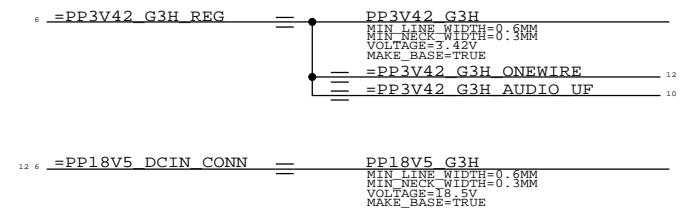
"S0,S0M" RAILS



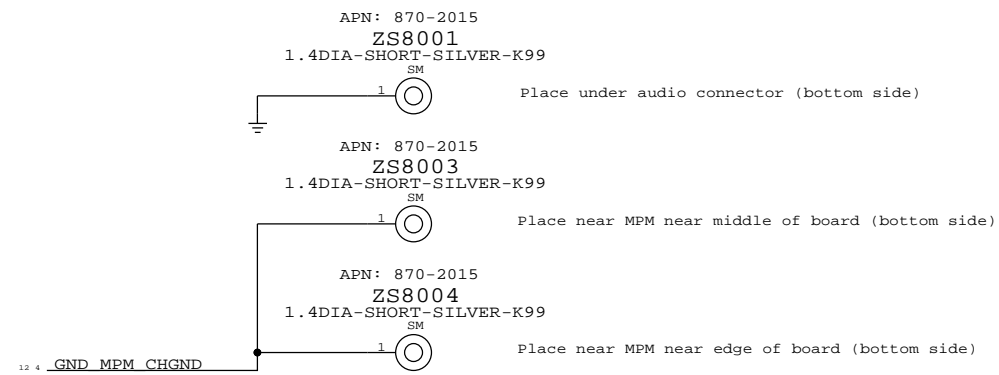
"S3" RAILS



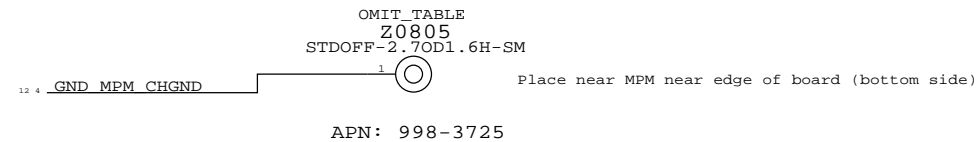
"G3H" RAILS



Pogo pins



ESD Boss



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
860-1427	1	ESD STANDOFF,K21/K78	Z0805		

SYNC MASTER=(K24\_MLB) SYNC DATE=(02/04/2009)

Power Aliases

Apple Inc.

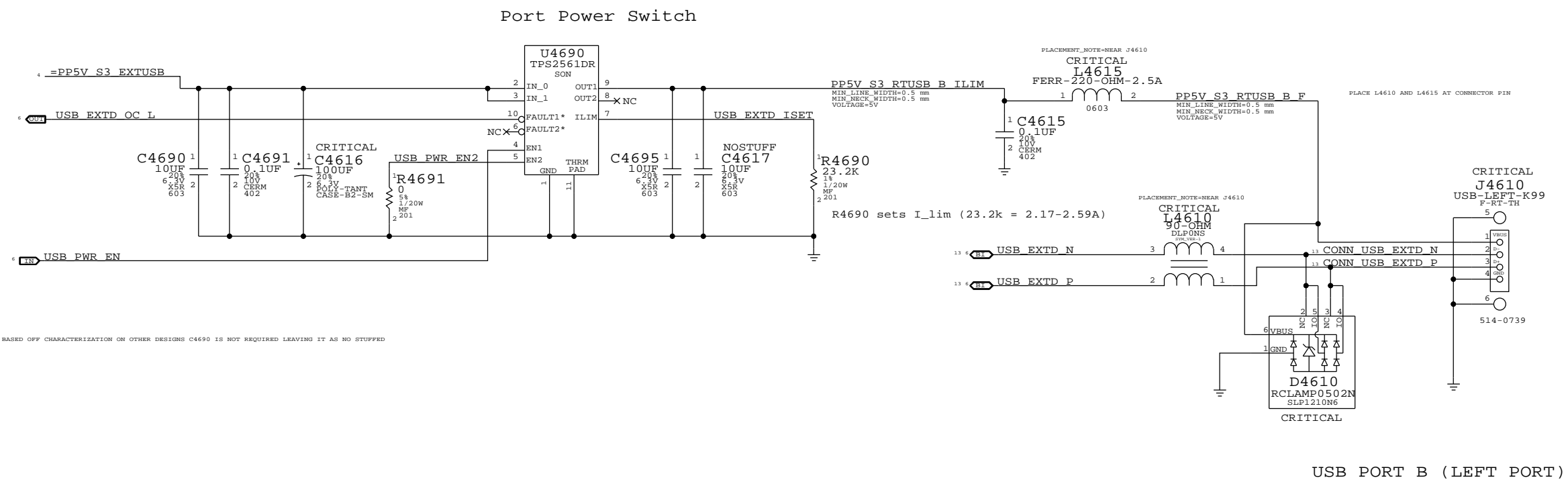
051-8925 D

4.0.0

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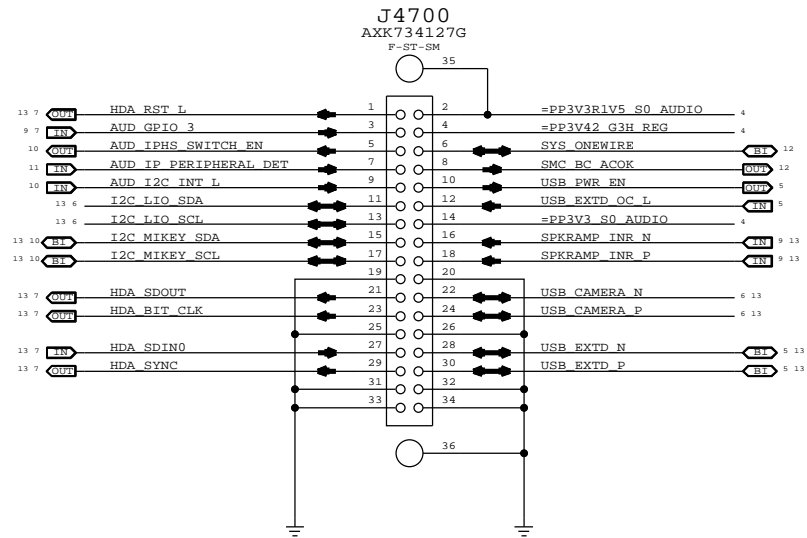
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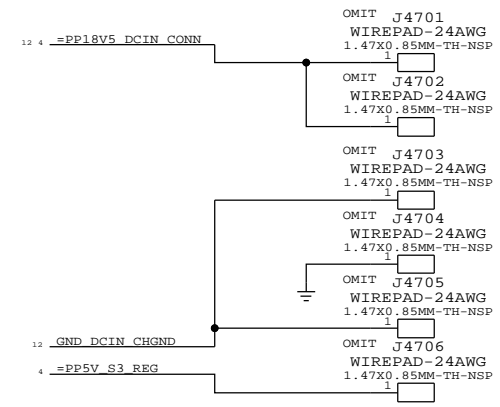
USB PORT B (LEFT PORT)

SYNC MASTER=(K84_MLB)		SYNC DATE=(11/09/2009)	
<b>External USB Connectors</b>			
Apple Inc.		DRAWING NUMBER	051-8925
		REVISION	4.0.0
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34 Pin LIO Flex Connector  
APN: 516S0859

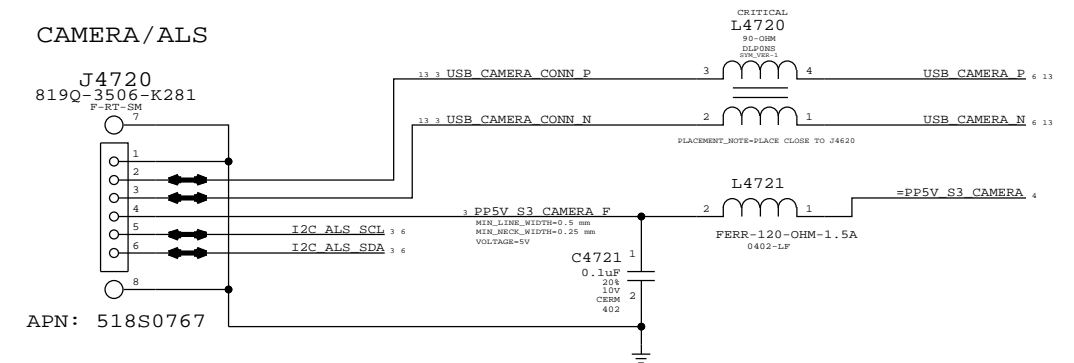


LIO POWER

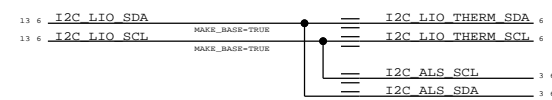


SPACE THE HOLES 2MM APART CENTER TO CENTER

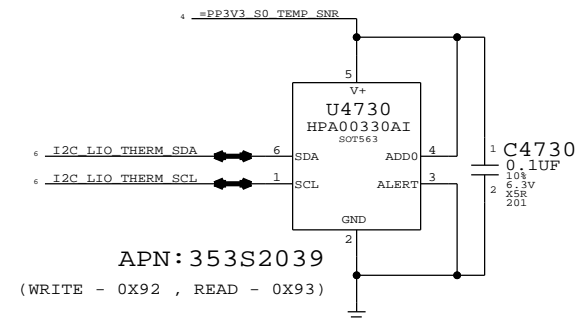
CAMERA/ALS



I2C aliases



Temp Sensor

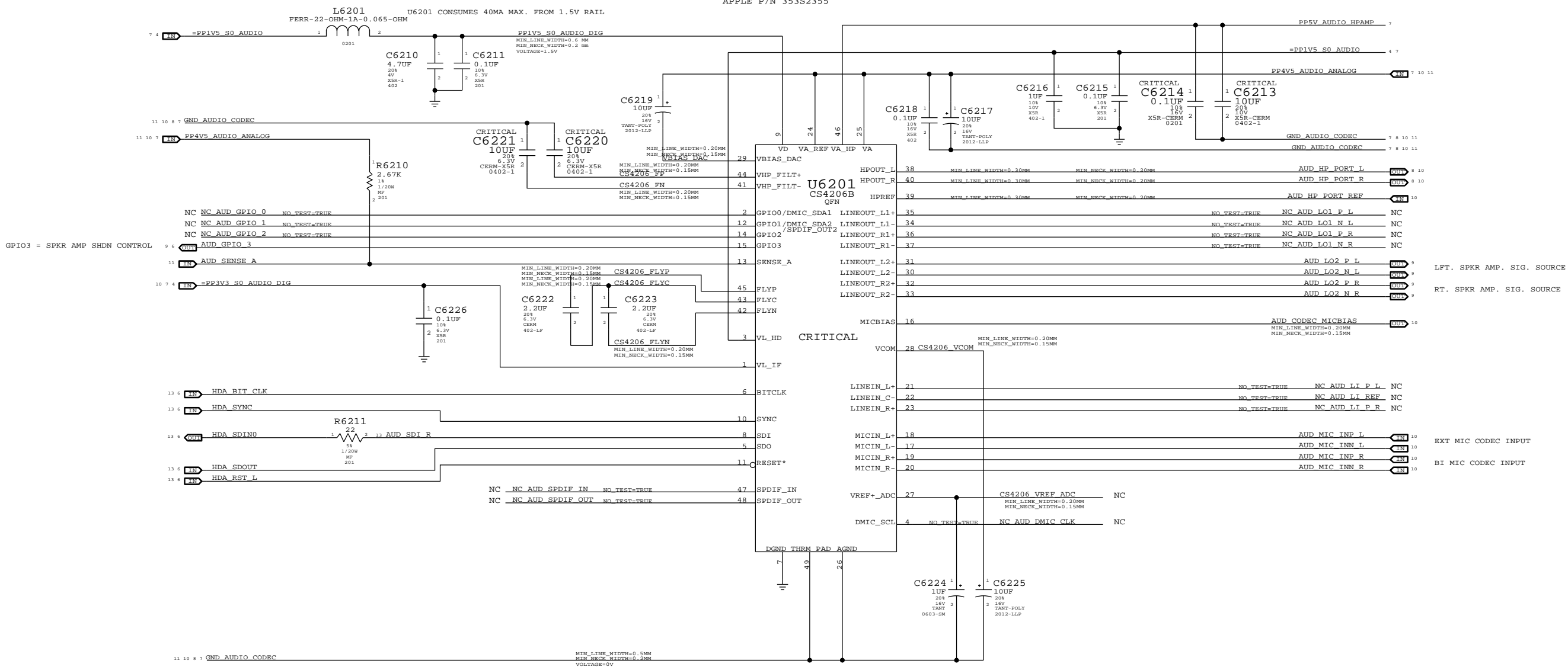


APN: 353S2039

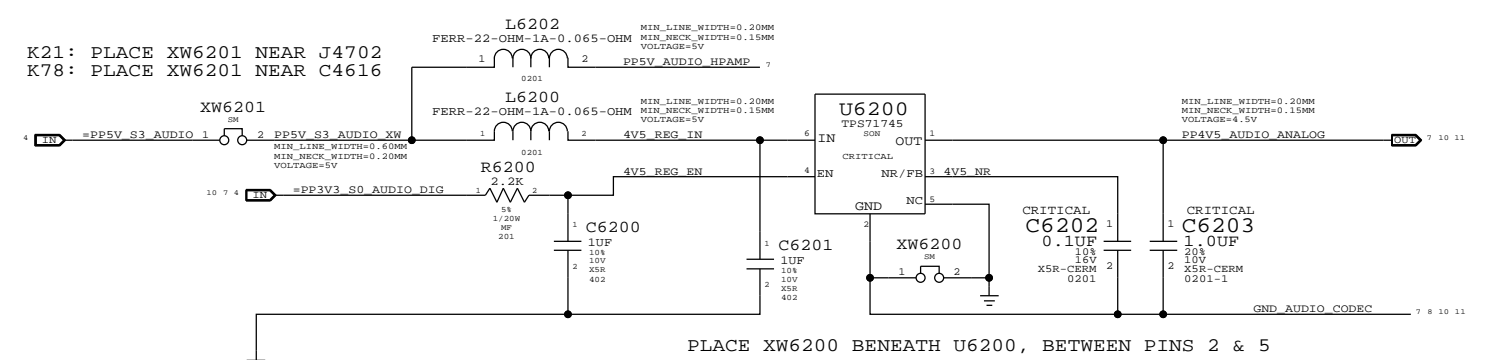
(WRITE - 0X92 , READ - 0X93)

PAGE TITLE		SYNC DATE=MASTER	
<b>LIO CONNECTORS</b>			
DRAWING NUMBER		051-8925	
		SIZE D	
REVISION		4.0.0	
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**AUDIO CODEC**  
APPLE P/N 353S2355



**4.5V POWER SUPPLY FOR CODEC**  
APPLE P/N 353S2456



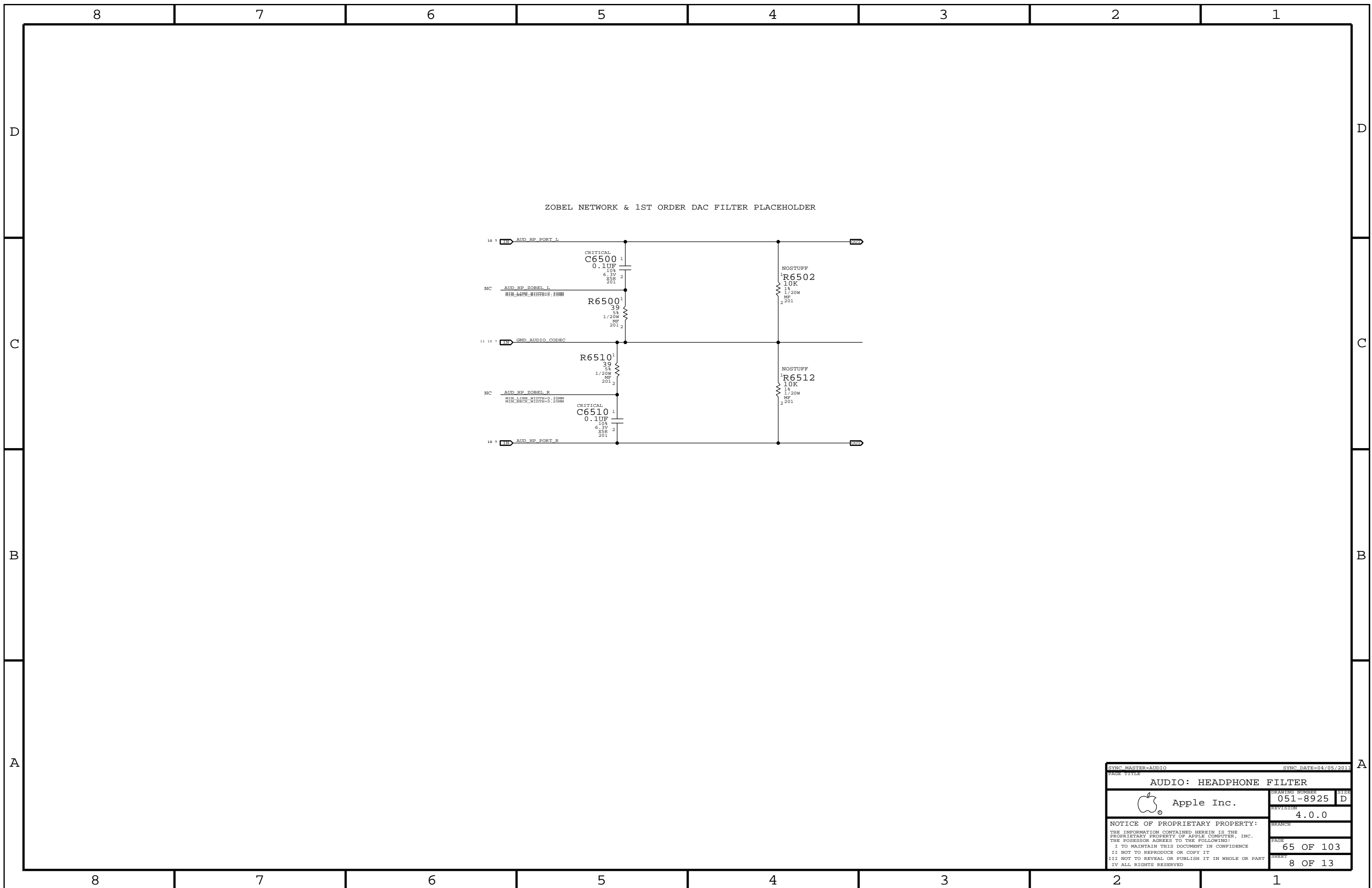
**NOTES ON CODEC I/O**  
 DIFF FSINPUT= 2.45VRMS  
 SE FSINPUT= 1.22VRMS  
 DAC1 FSOUTPUT= 1.34VRMS  
 DAC2/3 FSOUTPUTDIFF= 2.67VRMS  
 DAC2/3 FSOUTPUTSE= 1.34VRMS


PLACE XW6200 BENEATH U6200, BETWEEN PINS 2 & 5

D  
C  
B  
A

D  
C  
B  
A

PAGE TITLE		SYNC DATE=04/05/2011	
<b>AUDIO: CODEC/REGULATOR</b>		DRAWING NUMBER	SIZE
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AUDIO: HEADPHONE FILTER			
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		REVISION	4.0.0
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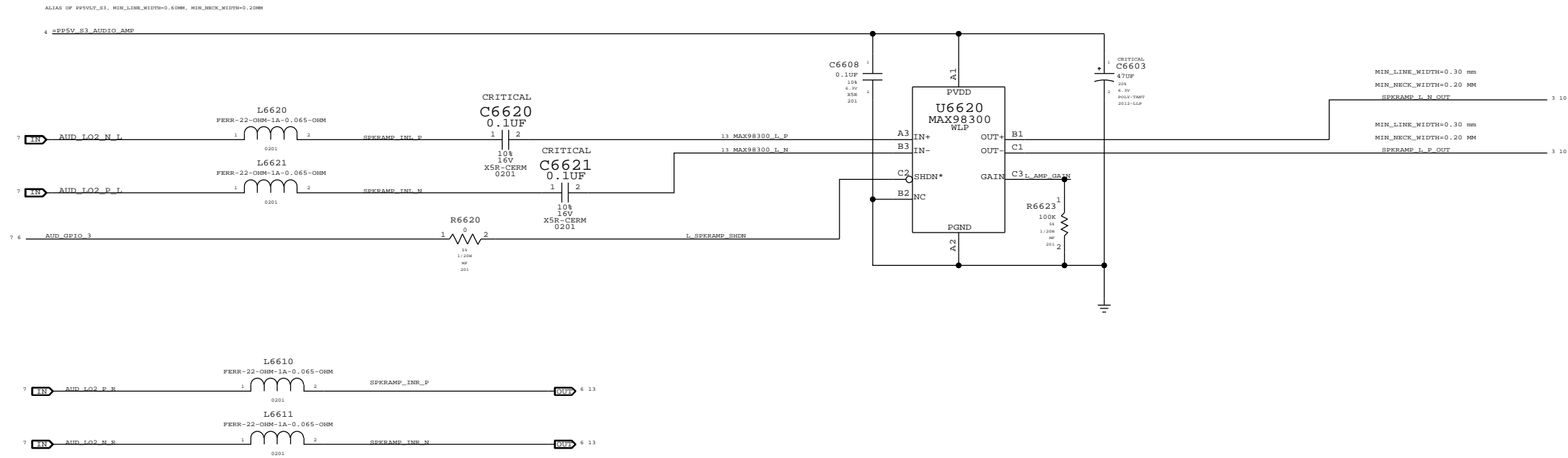
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SPEAKER AMPLIFIERS

APN:353S2888

SPEAKER LOWPASS 80 HZ < FC < 132 HZ

GAIN 6DB



SYMC MASTER-AUDIO		SYMC_DATE=04/05/2011	
PAGE TITLE			
AUDIO: SPEAKER AMP			
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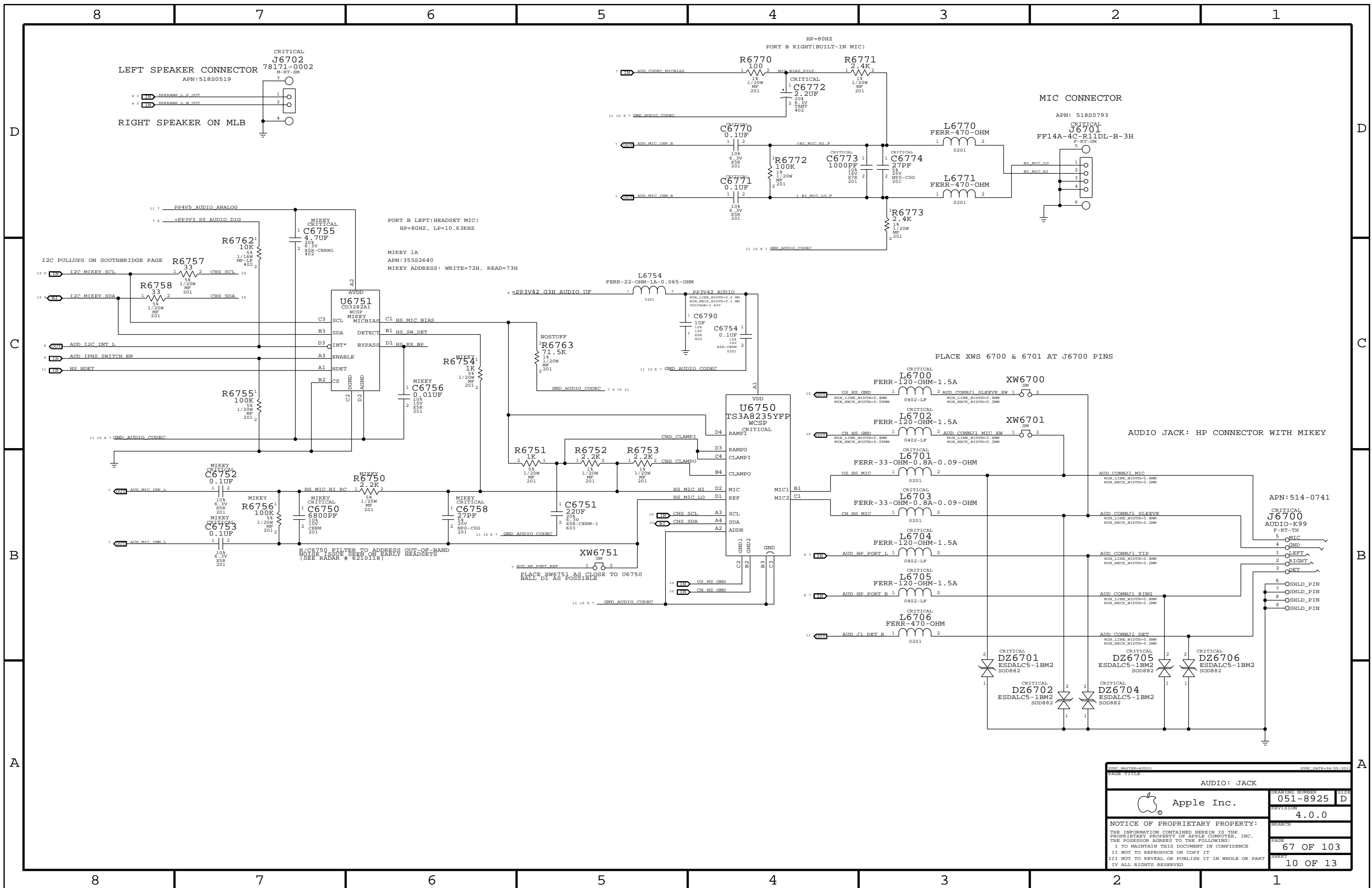
5

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AUDIO: JACK	
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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	GPIO_0 AND GPIO_1	0X09 (A)
SPEAKERS	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A

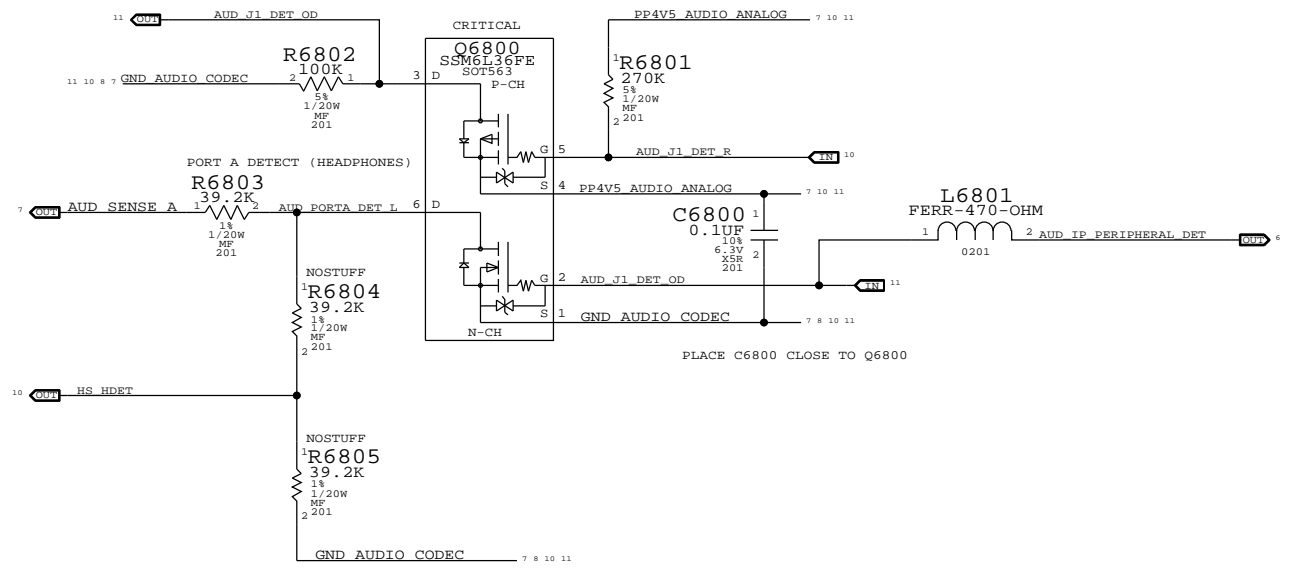
CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

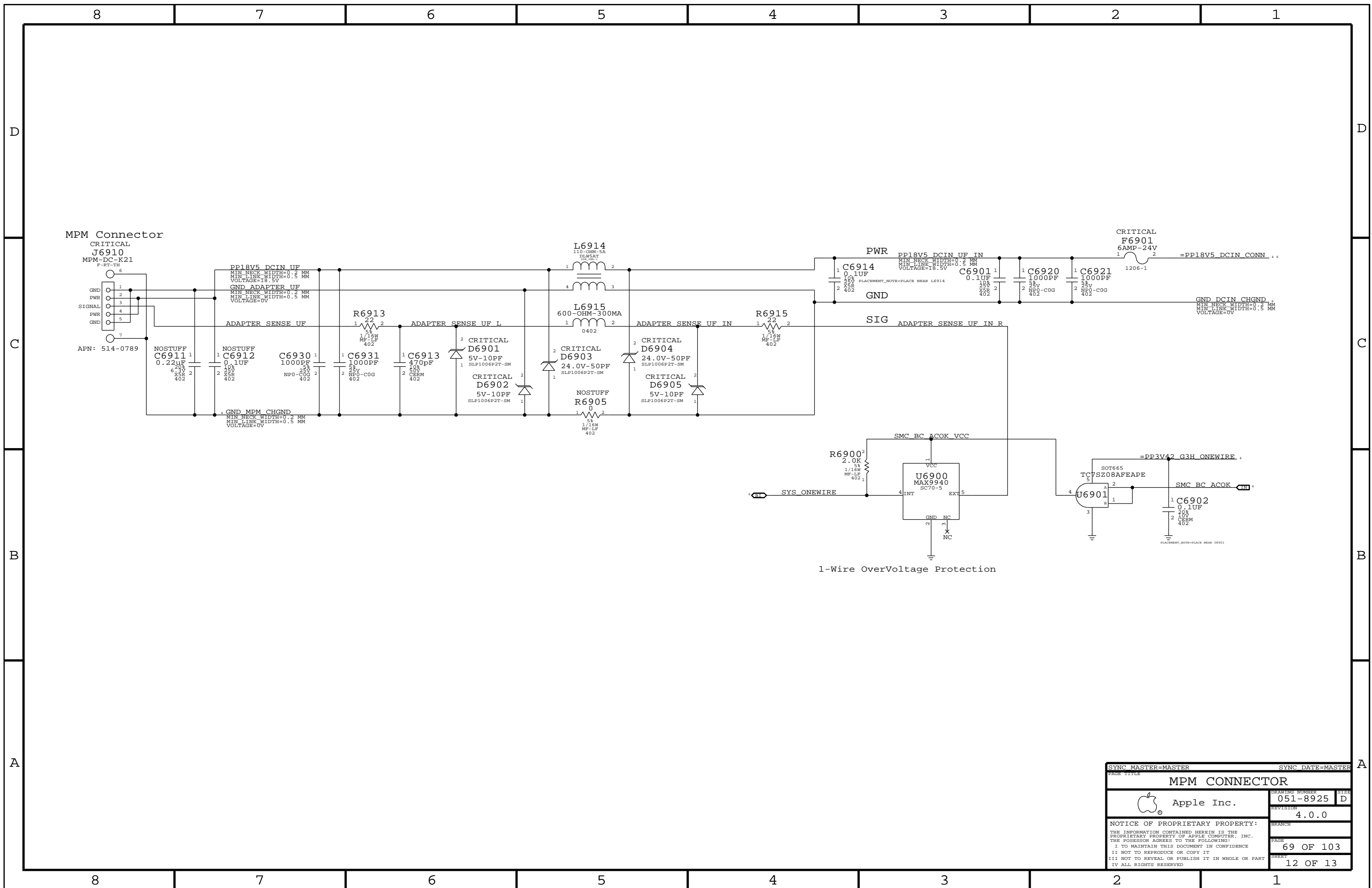
  


SOUTHBIDGE RESOURCE/PIN ALLOCATIONS

FUNCTION	NET NAME	SB GPIO/INT
PERIPHERAL/EXTRACTION DETECT	AUD_IP_PERIPHERAL_DET	GPIO 38
MIKEY INTERRUPT	AUD_I2C_INT_L	GPIO 55
MIKEY ENABLE	AUD_IPHS_SWITCH_EN	GPIO 7
MIKEY I2C BUS	I2C_MIKEY_SDA/SCL	MCP89 SMBUS 0



SYNC MASTER=AUDIO		SYNC DATE=04/05/2011	
PAGE TITLE <b>AUDIO: JACK TRANSLATORS</b>			
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SYNC MASTER=MASTER		SYNC DATE=MASTER	
<b>MPM CONNECTOR</b>			
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		SHEET	12 OF 13

K16 LIO BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, L2L2, L2L3, L2L4, L2L5, BOTTOM	NO_TYPE, BGA_P10M	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	0.100MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.120 MM	0.120 MM			
55_OHM_SE	*	Y	0.125 MM	0.125 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	L2L3, L2L4	Y	0.115 MM	0.115 MM		0.130 MM	0.130 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.125 MM		0.110 MM	0.110 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
50_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
36_DIELECTRIC	TOP, BOTTOM	0.180 MM	?
36_DIELECTRIC	TOP, BOTTOM	0.180 MM	?
24_DIELECTRIC	-	0.254 MM	?
46_DIELECTRIC	-	0.508 MM	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=24_DIELECTRIC	?
USB	TOP, BOTTOM	=46_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=24_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=24_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.12.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
USB_EXTN	USB_90D	USB	CONN USB_EXTD N	5
USB_EXTP	USB_90D	USB	CONN USB_EXTD P	5
USB_EXTN	USB_90D	USB	USB_EXTD N	5 6
USB_EXTP	USB_90D	USB	USB_EXTD P	5 6
USB_CAMERA	USB_90D	USB	USB_CAMERA P	6
USB_CAMERA	USB_90D	USB	USB_CAMERA N	6
USB_CAMERA	USB_90D	USB	USB_CAMERA CONN P	3 6
USB_CAMERA	USB_90D	USB	USB_CAMERA CONN N	3 6
	SMB_55S	SMB	I2C LIO_SDA	6
	SMB_55S	SMB	I2C LIO_SCL	6
	SMB_55S	SMB	I2C MIKEY_SCL	6 10
	SMB_55S	SMB	I2C MIKEY_SDA	6 10
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	6 7
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	6 7
	HDA_55S	HDA	HDA_RST_L	6 7
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	6 7
	HDA_55S	HDA	AUD_SDI_R	7
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	6 7
	DIFFPAIR	AUDIO	SPKRAMP INL N	9
	DIFFPAIR	AUDIO	SPKRAMP INL P	9
	DIFFPAIR	AUDIO	SPKRAMP INR N	6 9
	DIFFPAIR	AUDIO	SPKRAMP INR P	6 9
	DIFFPAIR	AUDIO	MAX98300 L N	9
	DIFFPAIR	AUDIO	MAX98300 L P	9

SYNC MASTER=(K24\_MLB) SYNC DATE=(04/06/2009)

MCP Constraints 2

Apple Inc.

DRAWING NUMBER: 051-8925 SIZE: D

REVISION: 4.0.0

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