<table>
<thead>
<tr>
<th>BOM Option</th>
<th>QTY</th>
<th>Description</th>
<th>Reference Set</th>
<th>Critical</th>
<th>BOM Option</th>
</tr>
</thead>
</table>
| Bar Code Labels / EEEE #'s
| 1 | 1 | 825-7563 CRITICAL1 EEEE:DK9L | 825-7563 CRITICAL1 EEEE:DLCL | 825-7563 CRITICAL1 EEEE:DLCQ | 825-7563 CRITICAL1 EEEE:DLCR |

| Sub-BOMs
<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>825-7563</td>
<td>1</td>
<td>CMN PTS,PCBA,MLB,K78</td>
<td>1607-8084 CMNPTS</td>
<td>085-2714 K78 MLB DEVELOPMENT BOM</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Apple Inc.</th>
</tr>
</thead>
<tbody>
<tr>
<td>051-8871</td>
</tr>
</tbody>
</table>

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**SYNC_MASTER=K21_MLB**
**SYNC_DATE=11/16/2010**
### X78 BOM GROUPS

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>138S0679</td>
<td>138S0678</td>
<td></td>
<td></td>
</tr>
<tr>
<td>377S0107</td>
<td>ONsemi alt to Semtech</td>
<td></td>
<td></td>
</tr>
<tr>
<td>376S0972</td>
<td>376S0612</td>
<td>ALL</td>
<td></td>
</tr>
</tbody>
</table>

### Alternate Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>VENDOR</th>
<th>CRITICAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>138S0691</td>
<td>ALL</td>
<td></td>
</tr>
<tr>
<td>138S0676</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Programmable Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>338S0895</td>
<td>1</td>
<td>U49001</td>
<td></td>
<td></td>
</tr>
<tr>
<td>337S3997</td>
<td>1</td>
<td>U9330</td>
<td>CRITICAL</td>
<td></td>
</tr>
</tbody>
</table>

### DDR3:

- SAMSUNG_4GB
- SAMSUNG_2GB
- ELPIDA_4GB
- MICRON_2GB
- HYNIX_4GB

### T29:

- T29ROM:BLANK
- T29ROM:PROG

### T29 MCU:

- IC, MCU: 32B, LPC1112A, 16KB/2KB, HVQFN25
- T29MCU:BLANK

### EEPROM:

- 32KBIT, 2X3QFN

### PARTS:

- All
- All
- All
- All

### Diodes:

- All
- Diodes alt to Toshiba

### Inductor:

- All
- 152S1295
- 152S1462 Toko alt to NEC

### Table:

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>CRITICAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>337S4100</td>
<td></td>
</tr>
<tr>
<td>337S4092</td>
<td>EARLY 1.5GHZ CPU SAMPLES</td>
</tr>
</tbody>
</table>

### Module Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>CRITICALU61001</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T29ROM:PROG</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>U3000,U3010,U3020,U3030</td>
<td>CRITICAL</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CRITICALU3100,U3110,U3120,U3130</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IC, SDRAM, 1GBIT, DDR3-1333, 78P FBGA, V68A-D, MICRON</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IC, SDRAM, 2GBIT, DDR3-1333, 78P FBGA, C-DIE, ELPIDA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IC, SDRAM, 2GBIT, DDR3-1333, 78P FBGA, B-DIE, HYNIX</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>U3200, U3210, U3220, U3230</td>
<td>CRITICAL</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CRITICALU3200, U3210, U3220, U3230</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IC, SDRAM, 1GBIT, DDR3-1333, 78P FBGA, T-DIE, HYNIX</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### BKLT:

- ENG
- PROD
- SMC_DEBUG_YES
- XDP
- VREFMRGN
- NOT

### Additional Information:

- BRANCH CENTER
- DRAWING NUMBER SIZE
- DRAWING NUMBER
- SIZE
- 051-8871
- 2.5.0
### Functional Test Points

- **J4001: AirPort / BT Connector**
- **J4002: Fan Connector**
- **J4501: SATA 5G Connector**
- **J4701: LDO Connector**
- **J5701: HDBM Connector**
- **J6955: HALL EFFECT Connector**
- **J6900: DC-in Connector**
- **J6903: Speaker Connector**
- **J6905: Battery Connector**
- **J6906: Internal I/O Connector**

### NO_TEST Nets

### Misc. Voltages & Control Signals

- **J6100: LPC+SPI Connector**

---

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**X.5.5**

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---

*Made in China*
PROCESSOR MICRO2-XDP CONNECTOR
NOTE: This is not the standard XDP pinout
Use with 920-0782 Adapter Flex to support chipset debug

PCH MICRO2-XDP CONNECTOR
NOTE: This is not the standard XDP pinout
Use with 920-0782 Adapter Flex to support chipset debug

**WARNING:** Even pins should be facing edge of the board.
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

**NOTE:** In the event of a S3->S0 transition ISOLATE_CPU_MEM_L will still be asserted on next S0->S3 transition.

**MEM_RESET_L** = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

**MEMVTT_EN** = ISOLATE_CPU_MEM_L + PLT_RESET_L * PM_SLP_S3_L

**ISOLATE_CPU_MEM_L** GPIO state during S3<->S0 transitions determines behavior of signals.

The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.
Current numbers from Vendor slide (REDACTED power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

EDP: 3000 mA
2250 mA (Dual Port)
2100 mA (Single Port)

C3701 CERM-X5R
C3710 CERM-X5R
10UF 10UF
6.3V 6.3V
20% 20%

C3705 1.0UF 1.0UF
0402 0402
X5R X5R
20% 20%

R3720 10K 10K
201 201
MF MF
5% 5%

C3714 1.0UF 1.0UF
0201-MUR 0201-MUR
X5R X5R
6.3V 6.3V
20% 20%

R3724 10K 10K
MF MF
1/20W 1/20W
5% 5%

T29_GPIO<4>
T29_GPIO<5>
T29_GPIO<10>
T29_GPIO<7>
T29_GPIO<11>
Current limit (R4600): 2.17-2.59A

USB/SMC Debug Mux

USB Port Power Switch

Right USB Port A

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2.5.0

www.vinafix.vn
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as inputs require pull-ups.
SMC Reset "Button", Supervisor & AVREF Supply

**SMC Reset "Button"**
- R5000
- SMC_XTAL
- TP_SMC_RSTGATE_L

**Supervisor & AVREF Supply**
- Used on mobiles to support SMC reset via keyboard.
- MR1* and MR2* must both be low to cause manual reset.
- PLACEMENT_NOTE: Place R5001 on BOTTOM side

**Mobiles:**
- 3.42V

**Desktops:**
- 5V

**Warning:**
- Be cautious when handling internal pull-ups as they can affect normal function.

**Internal Pull-Up Resistors**
- Q5040
- SSM6N37FEAPE
- R5095

**Additional Notes**
- BATLOW# Isolation
- Internal 20K pull-up on PM_BATLOW_L in PCH.
- Below connections are different from K91

**Other Components**
- SMC_RESETGATE_L
- SMC_PME_S4_WAKE_L
- SMC_GFX_THROTTLE_L
- SMC_S4_WAKESRC_EN
- PM_THRMTRIP_L_R
- NC_SMC_FAN_1_TACH
- NC_SMC_FAN_2_TACH
- NC_SMC_FAN_2_CTL
- NC_SMC_FAN_3_TACH
- NC_SMC_FAN_3_CTL
- SMC_BMON_MUX_SEL
- SMC_BMON_ISENSE
- SMC_PBUS_VSENSE
- SMC_WLAN_ISENSE
- SMC_LCDBKLT_ISENSE
- SMC_CPUVCCIO_ISENSE
- CPU_PROCHOT_L
- SMC_1V5S3_ISENSE
- SMC_GFX_VSENSE
- SMC_DCIN_ISENSE
- SMC_BC_ACOK
- SMC_HS_COMPUTING_ISENSE
- SMC_GFX_OVERTEMP_L
- SMC_ADC14
- SMC_FAN_1_TACH
- SMC_PA0_PU
- PM_THRMTRIP_L_R

**Schematic Details**
- MAKE_BASE = TRUE
- SOT-563
- NOSTUFF
- X5R
- MF-LF
- 1/20W
- 5%
- 201
- MF
- 5%
- 1/20W
- 10K
- 100K
- 0.47UF
- 201
- 5%
- 15PF
- 201
- 5%
- 201
- 5%
- 21
- 5%
- 10uF
- 201
- 5%
- 1/10W
- 201
- 1/10W
- 201
- 1/20W
- 1/20W
- 1/20W
Replacing caps with 100K PD on ISENSE SMC inputs
FAN CONNECTOR
To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:

If HIGH, keyboard backlight not present
If LOW, keyboard backlight present

R5853 always stuffed, R5854 only grounded when KB BL flex connected.

---

www.vinafix.vn
CPU=Sandy Bridge ULV, AXG=GT2
CPU VCCIO (1.05V S0) Regulator

- VOLTAGE=5V
- MIN_NECK_WIDTH=0.2 mm
- MIN_LINE_WIDTH=0.6 mm
- R7603
- 0
- 201
- MF
- 5%
- 1/20W
- C7619
- 62UF
- CRITICAL
- ELEC
- 20%
- 2V
- 44 73
- 44 73
- R7630
- 1/10W
- MF-LF
- 603
- 0
- 2
- 1
- C7630
- 1UF
- X5R
- 16V
- 10%
- 15
- 10
- 11
- 11V
- 20%
- 0612
- MF
- 1W
- 1%
- POWER_SUPPLY_CURRENT=21A Max Output
- PP_CPUVCCIO_S0_REG: f = 300 kHz
- Vout = 1.05V
- Vout = 0.5V * (1 + Ra / Rb)
- OCP = 25.6A
- OCP = R7641 x 8.5uA / R7640

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www.vinafix.vn
1.8V S0 Regulator

\[ V_{out} = 0.8V \times (1 + \frac{R_a}{R_b}) \]

Max Current = 1.8A
Freq = 1 MHz

1.5V S0 LDO

Vout = 1.5V
Max Current = 1.0A

1.05V S0 LDO

Vout = 1.05V
Max Current = 0.02A

Misc Power Supplies

77 OF 109
Some signals require 27.4-ohm single-ended impedance. Most CPU signals with impedance requirements are 50-ohm single-ended.

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

NOTE: CPU_XDP_BPM physical constraint is to prevent routing on outer layers.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.

CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0.0mm] of CLK pairs. per Huron River SFF DG rev1.0 (#438297).

DDR3:

Memory Bus Spacing Group Assignments

Spacing Rule Sets

Memory to Power Spacing

Memory to GND Spacing

Memory Bus Spacing Group Assignments

Memory Net Properties

Memory Constraints
DP/T29 Connector Signal Constraints

T29 I2C Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

DisplayPort Signal Constraints

T29 Net Properties

T29/DP Net Properties

T29 IC Net Properties

T29 IC Net Properties

SOURCE: Bill Cornelius's T29 Routing Notes
<table>
<thead>
<tr>
<th>SMBus Charger Net Properties</th>
</tr>
</thead>
<tbody>
<tr>
<td>NET_TYPE</td>
</tr>
<tr>
<td>SMBUS_SMC_B_SA_SCL</td>
</tr>
<tr>
<td>SMBUS_SMC_B_SA_SDA</td>
</tr>
<tr>
<td>SMBUS_SMC_B_SA_SCL</td>
</tr>
<tr>
<td>SMBUS_SMC_B_SA_SDA</td>
</tr>
<tr>
<td>SMBUS_SMC_MGMT_SCL</td>
</tr>
<tr>
<td>SMBUS_SMC_MGMT_SDA</td>
</tr>
</tbody>
</table>

| SMBUS_SMC_A_S3_SCL | SMBUS_SMC_A_S3_SCL |
| SMBUS_SMC_A_S3_SDA | SMBUS_SMC_A_S3_SDA |
| SMBUS_SMC_A_S3_SCL | SMBUS_SMC_A_S3_SCL |
| SMBUS_SMC_A_S3_SDA | SMBUS_SMC_A_S3_SDA |

| PCHR_CSI_N | 1TO1_DIFFPAIR |
| PCHR_CSI_P | 1TO1_DIFFPAIR |
| PCHR_CSI_N | 1TO1_DIFFPAIR |
| PCHR_CSI_P | 1TO1_DIFFPAIR |

| SMBUS_SMC_B_SA_SCL | SMBUS_SMC_B_SA_SCL |
| SMBUS_SMC_B_SA_SDA | SMBUS_SMC_B_SA_SDA |
| SMBUS_SMC_B_SA_SCL | SMBUS_SMC_B_SA_SCL |
| SMBUS_SMC_B_SA_SDA | SMBUS_SMC_B_SA_SDA |

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Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

Memory Constraint Relaxations

- OVERRIDE OVERRIDE OVERRIDE OVERRIDE OVERRIDE OVERRIDE OVERRIDE OVERRIDE
- MEM_40S * 400 MIL
- 0.09 MM

Audio Net Properties
- AREA_TYPE SPACING_RULE_SET
- NET_SPACING_TYPE1 NET_SPACING_TYPE2
- GND
- MEM_DQS
- GND_P2MM
- GND_P2MM
- CPU_VCC
- SENSE
- SATA
- PCIE
- GND_P2MM
- CPU_COMP
- THERM
- =1:1_DIFFPAIR
- =1:1_DIFFPAIR
- =55_OHM_SE
- =55_OHM_SE
- THERM_1TO1_55S

Misc Net Properties
- AREA_TYPE SPACING_RULE_SET
- NET_SPACING_TYPE1 NET_SPACING_TYPE2
- USB
- ENET
- SATA
- =1:1_DIFFPAIR
- =1:1_DIFFPAIR
**NOTE:** These are Intel recommended impedances for PEG, unused on K90i.

**NOTE:** 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.

<table>
<thead>
<tr>
<th>Impedance</th>
<th>Layers</th>
<th>Minimum Neck Width</th>
<th>Maximum Neck Length</th>
<th>Pair Primary Gap</th>
<th>Pair Neck Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>100_OHM_DIFF</td>
<td>ISL4, ISL9</td>
<td>0.085 mm</td>
<td>0.250 mm</td>
<td>0.200 mm</td>
<td>0.200 mm</td>
</tr>
<tr>
<td>110_OHM_DIFF</td>
<td>ISL4, ISL9</td>
<td>0.071 mm</td>
<td>0.300 mm</td>
<td>0.200 mm</td>
<td>0.200 mm</td>
</tr>
<tr>
<td>110_OHM_DIFF</td>
<td>*</td>
<td>STANDARDS</td>
<td>STANDARDS</td>
<td>STANDARDS</td>
<td>STANDARDS</td>
</tr>
<tr>
<td>100_OHM_DIFF</td>
<td>ISL3, ISL10</td>
<td>0.074 mm</td>
<td>0.250 mm</td>
<td>0.200 mm</td>
<td>0.200 mm</td>
</tr>
<tr>
<td>80_OHM_DIFF</td>
<td>ISL3, ISL10</td>
<td>0.110 mm</td>
<td>0.170 mm</td>
<td>0.180 mm</td>
<td>0.180 mm</td>
</tr>
<tr>
<td>85_OHM_DIFF</td>
<td>ISL4, ISL9</td>
<td>0.115 mm</td>
<td>0.170 mm</td>
<td>0.180 mm</td>
<td>0.180 mm</td>
</tr>
<tr>
<td>80_OHM_DIFF</td>
<td>*</td>
<td>STANDARDS</td>
<td>STANDARDS</td>
<td>STANDARDS</td>
<td>STANDARDS</td>
</tr>
<tr>
<td>55_OHM_SE</td>
<td></td>
<td>0.090 mm</td>
<td>0.130 mm</td>
<td>0.130 mm</td>
<td>0.130 mm</td>
</tr>
<tr>
<td>48_OHM_SE</td>
<td></td>
<td>0.097 mm</td>
<td>0.120 mm</td>
<td>0.160 mm</td>
<td>0.160 mm</td>
</tr>
<tr>
<td>40_OHM_SE</td>
<td></td>
<td>0.090 mm</td>
<td>0.120 mm</td>
<td>0.160 mm</td>
<td>0.160 mm</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Impedance</th>
<th>Layers</th>
<th>Minimum Neck Width</th>
<th>Maximum Neck Length</th>
<th>Pair Primary Gap</th>
<th>Pair Neck Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>90_OHM_DIFF</td>
<td>ISL4, ISL9</td>
<td>0.115 mm</td>
<td>0.210 mm</td>
<td>0.200 mm</td>
<td>0.200 mm</td>
</tr>
<tr>
<td>85_OHM_DIFF</td>
<td>*</td>
<td>STANDARDS</td>
<td>STANDARDS</td>
<td>STANDARDS</td>
<td>STANDARDS</td>
</tr>
<tr>
<td>72_OHM_DIFF</td>
<td>ISL3, ISL10</td>
<td>0.135 mm</td>
<td>0.135 mm</td>
<td>0.210 mm</td>
<td>0.210 mm</td>
</tr>
</tbody>
</table>

**NOTE:** 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

<table>
<thead>
<tr>
<th>Impedance</th>
<th>Layers</th>
<th>Minimum Neck Width</th>
<th>Maximum Neck Length</th>
<th>Pair Primary Gap</th>
<th>Pair Neck Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>100_DIFF_BGA</td>
<td>ISL3, ISL4</td>
<td>0.075 mm</td>
<td>0.125 mm</td>
<td>0.125 mm</td>
<td>0.125 mm</td>
</tr>
<tr>
<td>90_DIFF_BGA</td>
<td>ISL9, ISL10</td>
<td>0.075 mm</td>
<td>0.125 mm</td>
<td>0.125 mm</td>
<td>0.125 mm</td>
</tr>
<tr>
<td>90_DIFF_BGA</td>
<td>*</td>
<td>STANDARDS</td>
<td>STANDARDS</td>
<td>STANDARDS</td>
<td>STANDARDS</td>
</tr>
<tr>
<td>85_DIFF_BGA</td>
<td>ISL9, ISL10</td>
<td>0.075 mm</td>
<td>0.125 mm</td>
<td>0.125 mm</td>
<td>0.125 mm</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Line-to-Line Spacing</th>
<th>Layers</th>
<th>Minimum Width</th>
<th>Maximum Width</th>
<th>Minimum Gap</th>
<th>Maximum Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1 mm</td>
<td>1:1_DIFFPAIR</td>
<td>0.1 mm</td>
<td>0.1 mm</td>
<td>0.1 mm</td>
<td>0.1 mm</td>
</tr>
<tr>
<td>0.2 mm</td>
<td>2:1_SPACING</td>
<td>0.2 mm</td>
<td>0.2 mm</td>
<td>0.2 mm</td>
<td>0.2 mm</td>
</tr>
<tr>
<td>0.25 mm</td>
<td>2.5:1_SPACING</td>
<td>0.25 mm</td>
<td>0.25 mm</td>
<td>0.25 mm</td>
<td>0.25 mm</td>
</tr>
<tr>
<td>0.3 mm</td>
<td>5:1_SPACING</td>
<td>0.3 mm</td>
<td>0.3 mm</td>
<td>0.3 mm</td>
<td>0.3 mm</td>
</tr>
</tbody>
</table>

**TABLE SPACING_RULE_ITEM**

<table>
<thead>
<tr>
<th>Spacing Rule Item</th>
<th>Weight</th>
<th>Dielectric</th>
<th>Minimum Width</th>
<th>Maximum Width</th>
<th>Minimum Gap</th>
<th>Maximum Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.140 mm</td>
<td>2x</td>
<td>Dielectric</td>
<td>0.140 mm</td>
<td>0.140 mm</td>
<td>0.140 mm</td>
<td>0.140 mm</td>
</tr>
<tr>
<td>0.350 mm</td>
<td>5x</td>
<td>Dielectric</td>
<td>0.350 mm</td>
<td>0.350 mm</td>
<td>0.350 mm</td>
<td>0.350 mm</td>
</tr>
</tbody>
</table>

**TABLE SPACING_ASSIGNMENT_ITEM**

<table>
<thead>
<tr>
<th>Assignment Item</th>
<th>Weight</th>
<th>Dielectric</th>
<th>Minimum Width</th>
<th>Maximum Width</th>
<th>Minimum Gap</th>
<th>Maximum Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEM_CLK</td>
<td>1</td>
<td>Dielectric</td>
<td>0.140 mm</td>
<td>0.140 mm</td>
<td>0.140 mm</td>
<td>0.140 mm</td>
</tr>
<tr>
<td>BGA_P2MM</td>
<td>2</td>
<td>Dielectric</td>
<td>0.350 mm</td>
<td>0.350 mm</td>
<td>0.350 mm</td>
<td>0.350 mm</td>
</tr>
</tbody>
</table>

**TABLE BOARD_INFO**

<table>
<thead>
<tr>
<th>Layer</th>
<th>Minimum Neck Width</th>
<th>Maximum Neck Length</th>
<th>Pair Primary Gap</th>
<th>Pair Neck Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.076 mm</td>
<td>0.076 mm</td>
<td>STANDARDS</td>
<td>STANDARDS</td>
</tr>
<tr>
<td>2</td>
<td>0.075 mm</td>
<td>0.075 mm</td>
<td>STANDARDS</td>
<td>STANDARDS</td>
</tr>
</tbody>
</table>

**TABLE PHYSICAL_RULE_ITEM**

<table>
<thead>
<tr>
<th>Physical Rule Item</th>
<th>Minimum Width</th>
<th>Maximum Width</th>
<th>Minimum Gap</th>
<th>Maximum Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>PHYSICAL_RULE_SET</td>
<td>0.140 mm</td>
<td>0.140 mm</td>
<td>0.140 mm</td>
<td>0.140 mm</td>
</tr>
<tr>
<td>PHYSICAL_RULE_SET</td>
<td>0.350 mm</td>
<td>0.350 mm</td>
<td>0.350 mm</td>
<td>0.350 mm</td>
</tr>
</tbody>
</table>