# SCHEM, MLB DVT, K99

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## Acoustic Cap BOM Config Tables

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K99 Power System Architecture

Need to update!!!

Power Block Diagram
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<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
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### ALTERNATE FORPART NUMBER BOM OPTION

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### ONSEMI AS ALTERNATE

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### Programmable Parts

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<tr>
<td>ALL</td>
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</tbody>
</table>

### DDR3:ELPIDA_4GB DRAM

- CONFIG0: H
- CONFIG2: H
- CONFIG3: L
- TYPE: ELPIDA_4GB

### DDR3:ELPIDA_2GB DRAM

- CONFIG0: H
- CONFIG2: L
- CONFIG3: L
- TYPE: ELPIDA_2GB

### K99_PROGPARTS

- BOOTROM: UNLOCKED
- SMC: PROG

### K99_MISC

- CAPS: TY CAP_2_2UF, TY CAP_10UF, TY CAP_1UF, TY CAP_22UF
- CAPS: MU CAP_2_2UF, MU CAP_10UF, MU CAP_1UF, MU CAP_22UF

### TPS71725DCK

- IC ASSY, EFI, UNLOCKED, K99
- CRITICAL

### TAIYO ASS ALTERNATE

<table>
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<th>PART NUMBER</th>
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### COMMON, ALTERNATE

- PROJ: K99
- MCP89U: A03
- DEBUG: ENG
- SMC, PROG
- SPI: 41MHZ
- LVDDR3: YES
- WLAN_PCTL: HW
- IPD_5V: S5_INT
- IPD_3V3: S5

### BKLT: ENG, BMON: ENG

- XDP, CONN, LPCPLUS, VREFMRGN: YES
- EFI_DEBUG, S0PGOOD, ISL
- MCPPLL_LDO, S3_S0, LED

### COMMON

- PROJ: K99, MCP89U: A03, K99_MISC
- DEBUG: ENG
- SMC, PROG
- SPI: 41MHZ
- LVDDR3: YES
- WLAN_PCTL: HW
- IPD_5V: S5_INT
- IPD_3V3: S5

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- MCP89U: A03
- DEBUG: ENG
- SMC, PROG
- SPI: 41MHZ
- LVDDR3: YES
- WLAN_PCTL: HW
- IPD_5V: S5_INT
- IPD_3V3: S5
CPU Power & Ground

Apple Inc. 051-8373 1
4.4.0

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PAGE TITLE

OMIT_TABLE

www.vinafix.vn
Micro2-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with X20-0782 Adapter Flex to support chipset debug.

Direction of XDP adapter flex

Please place J1300 within 1" of board edge with odd-numbered pins facing edge. Avoid any tall components between J1300 and edge.

PE0 ports are Gen2-capable.  4 RCs: x4, x2, x1, x1

PE1 ports are Gen1-only.  2 RCs: x1, x1

+VIO_PE_AVDD0 and +VIO_PE_DVDD0 can be GND
If PE0[3:0] are not used,

+VIO_PE_AVDD1 and +VIO_PE_DVDD1 can be GND
If PE0[4:5] and PE1[0:1] are not used,

www.vinafix.vn
DDC Mode Pull-downs

NOTE: 100k pull-downs required if HPLUG_DET0/HPLUG_DET1 are not used.

GPIO Pull-Ups

NOTE: Pull-ups are necessary if used for TMDS/HDMI only then dual-mode DisplayPort (DP++). If unused no pulls are necessary.

HPLUG_DET0/HPLUG_DET1 are not used.

NOTE: 100K pull-downs required if HPLUG_DET0/HPLUG_DET1 are not used.

8 7 5 4 2 1

8 17 19

8 20 23

MXM_GOOD_L

R1800 100K MF1/20W 5%

R1801 100K MF1/20W 1%

R1805 2.49K MF1/20W 1%

35 67 35 67 35 67 35 67 9 67 9 67 9 67 9 69 9 69 9 69 9 69 9 69 9 67 OUT OUT OUT OUT IN IN IN IN IN IN IN IN IN IN

49.9 49.9 20 mA

SATA_ODD_D2R_P

SATA_ODD_D2R_N

ENET_RXD<2>

MCP_MII_COMP_GND

MCP_MII_COMP_VDD

PP3V3_ENET_MCP_PLL_MAC

ENET_ENERGY_DET

ENET_RX_CTRL

ENET_CLK125M_RXCLK

SATA_ODD_R2D_C_N

SATA_ODD_R2D_C_P

SATA_HDD_D2R_N

SATA_HDD_R2D_C_N

SATA_HDD_R2D_C_P

Connect RGMII_MDIO to 10K pull-down.

All other pins can be left TP or NC.

Connect RGMII_RXCTL to 10K pull-down.

Connect RGMII_VREF to 10K pull-down.

RGMII_COMP_VDD/_GND must remain connected as shown.

+3.3V_PLL_MAC_DUAL must remain connected to 3.3V RMGT rail.

Connect RGMII_INTR to 10K pull-down (if not used as GPIO).

Connect RGMII_RXCLK to 10K pull-down.

Internal MAC Disable:

Connect RGMII_RESET* together to 10K pull-down.

Connect RGMII_RDPRI to 10K pull-down.

Connect RGMII_RPDUP to 10K pull-down (if not used as GPIO).

+3.3V_PLL_MAC_DUAL must remain connected to 3.3V RMGT rail.

RGMII_COMP_VDD/_GND must remain connected as shown.

Connect RGMII_VREF to 10K pull-down.

Connect RGMII_MDI0 to 10K pull-down.

All other pins can be left TP or NC.
NOTE: "SW" rails are dynamically switched in the SO state as needed, controlled by MCP89 GPIOs.


NOTE: VDD_CORE_BYTES signals should NOT be used for system enabling unless VDD_COREA/COREB are powered by separate regulators. Instead, connect regulators closest to COREA/B as possible.
DIMM CKE Clamps

CKE must be held low to keep memory in self-refresh. Clamps enable after MCP89 MEMVDD rail switched off. Clamps release after MCP89 MEMVDD is up and CKEs are driven by MCP89. A clamp is used on each CKE signal on DIMM. Q2355/Q2356 chosen for low output capacitance.

Approx. Rise Time (EN to 1.35V, uS): 7.91 + 0.0678 * R1 (Kohms)

Gated Rail Savings: 120mW

NV Requirements:
- Min Ramp-Up Time: 20 uS (10% to 90%)
- Max Ramp-Up Time: 65 uS (ENABLE to 90%)

- FET Ron <= 3.8 mOhms

- Max Current: 4.3 A (EDP)

Q2300

Type: N-Channel

Part: STMFS4854N

Rds(on) 10 mOhm @3.2V

C2300 helps reduce input rail droop during Q2300 turn-on.
Approx. Ramp Time (EN to 1V, uS): \(43.9 + 0.6943 \times C1(pF)\)

- Min Ramp-Up Time: 100 uS (10% to 90%)
- Max Ramp-Up Time: 1500 uS (ENABLE to 90%)
- FET \(R_{on} \leq 2.5\) mOhms
- Gated Rail Savings: 860mW

NOTE: nVidia recommends Infineon BSC020N03MS for Q2400.

C2400 helps reduce input rail droop during Q2400 turn-on.

\(C_{2400}\) helps reduce input rail droop during Q2400 turn-on.

Approx. Ramp Time (EN to 1V, uS): \(43.9 + 0.6943 \times C1(pF)\)

- Min Ramp-Up Time: 100 uS (10% to 90%)
- Max Ramp-Up Time: 1500 uS (ENABLE to 90%)
- FET \(R_{on} \leq 2.5\) mOhms
- Gated Rail Savings: 860mW

NOTE: nVidia recommends Infineon BSC020N03MS for Q2400.
MCP 3.3V RGBDAC Power

MCP 1.05V DisplayPort Power

If RGBDAC is used, requires ferrite (155S0382)
plus 1x 4.7µF 0603 & 1x 0.1µF 0402 cap.

If RGBDAC is not used, tie to GND.


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A14/A15 FOR 2G/4G MODE ONLY
CS1 IS FOR 2G DOP RANK CONTROL
NOTE: Unused pins have "(SMC_PWR_EN)" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.
Another slave port is available at 0x10/0x11, probably not used.

MCP89 SMBus 1 is slave port to EFI Debug Serial
(Write: 0xE0 Read: 0xE1)
(Write: 0x30 Read: 0x31)
(Write: 0x98 Read: 0x99)

XDP Connector
(Write: 0xAD/0xAF)
(Write: 0xAC/0xAE)

MCP89 SMBus "1" Connections
(Write: 0xA9/0xAA)

MCP89 SMBus "0" Connections
(Write: 0x9F/0xA0)

SMC "0" SMBus Connections
(Write: 0x72 Read: 0x73)

Internal DP
(Write: 0x58 Read: 0x59)

Battery
Battery Charger - (Write: 0xB7 Read: 0xB8)
Battery LED Circuit - (Write: 0x68 Read: 0x69)

Battery Temp - (Write: 0x98 Read: 0x99)

ALS           - N/A (Feature Removed)

Mikey
Finstack Temp - (Write: 0x98 Read: 0x99)

SMC "Management" SMBus Connections
See Table

SMC "Battery A" SMBus Connections
See Table

SMC "A" SMBus Connections
(Write: 0x12 Read: 0x13)

SMC "B" SMBus Connections
(Write: 0x90 Read: 0x91)
**DCIN (AMON) Current Sense, RMUX & Filter**

**ISL6259 Gain: 20x**
- Gain: 200x
- Notes: Place near sense resistor
- From charger
- Sense R: R7022
- Value: 20 mOhm
- Max Vdiff: 2.3mV

**Battery (BMON) Current Sense, MUX & Filter**

- Gain: 36x
- Notes: Place near sense resistor
- From charger
- Sense R: R7050
- Value: 10 mOhm
- Max Vdiff = 24.8mV

**Chipset Regulators High-Side Current Sense / Filter**
- ISL6259 Gain: 20x
- Notes: Place near sense resistor
- Max Vdiff: 80mV

**VERIFY ALL RESISTOR AND GAINS**

**MCP VCore Current Sense Filter**
- Gain: 100x
- Notes: Do not stuff R5415 and R7593 at the same time!

**MCP MEM VDD Current Sense / Filter**
- Notes: Place near sense resistor

**CPU VCore Load Side Current Sense / Filter**
- Notes: Place near sense resistor

---

**PLACEMENT_NOTEs:**
- Place near sense resistor
- Place close to BNC

**NOTE:**
- Monitoring current from battery to BMON (battery discharge, access R7050)

---

**Apple Inc.**

**Current Sensing**

**911-03773 4.4.0**

**Silicon Gardens, CA USA 92676-2835**

**www.vinafix.vn**
FAN CONNECTOR
NOTE: 42 & 62 MHz use FAST_READ command.

ROM will ignore SPI cycles.

NOTE: If HOLD* is asserted, ROM will ignore SPI cycles.

MCP2202 SPI Frequency Select:

<table>
<thead>
<tr>
<th>Frequency</th>
<th>SPI_MOSI</th>
<th>SPI_CLK</th>
</tr>
</thead>
<tbody>
<tr>
<td>25.0 MHz</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>41.7 MHz</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>62.5 MHz</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

NOTE: 42 & 62 MHz use FAST_READ command.
SPEAKER AMPLIFIERS

APN: 353S2888

SPEAKER LOWPASS 80 Hz < FC < 132 Hz
GAIN 6dB

---

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SYNC_MASTER=AUDIO
AUDI0: SPEAKER AMP
VOLTAGE=5V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
PP5V_S3_U6610
MAX98300_R_N = PP5V_S3_AUDIO_AMP
SPKRAMP_INR_N
R_AMP_GAIN
SPKRAMP_INR_P
AUD_GPIO_3
MIN_NECK_WIDTH=0.20 MM
MIN_LINE_WIDTH=0.30 mm
SPKRAMP_R_N_OUT
MIN_NECK_WIDTH=0.20 MM
MIN_LINE_WIDTH=0.30 mm
SPKRAMP_R_P_OUT
MAX98300_R_P
66 OF 110
4.4.0
051-8379
48 OF 73

---

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IMVP6 CPU VCore Regulator

OCP = 21.5MV / R7480 + 3.1A
VPMON = 90 X R7480 X VO X IO
18A @ 3V = 1.62V
LOAD LINE = R7480 X 6 / (500U X R7414)

CPU_VCCSENSE_N

CPU_VCCSENSE_P

R7480

1/20W

5%
Vimon = 31 * Io * R7525 * (1 + R7575/R7573)

OCP = R7569 X 100A / ( R7525 X (1 + R7575/R7573) )

\[ \text{Vimon} = 31 \times \text{Io} \times R7525 \times (1 + \frac{R7575}{R7573}) \]

\[ \text{OCP} = \frac{R7569 \times 100A}{R7525 \times (1 + \frac{R7575}{R7573})} \]
Place XM7610, XM7611 at desired location for remote sensing.

VOLTAGE = 5V
MIN_NECK_WIDTH = 0.2 mm
MIN_LINE_WIDTH = 0.6 mm

CPUVTTS0_AGND
CPUVTTS0_FB
CPUVTTS0_RTN
CPUVTTS0_VO
CPUVTTS0_PGOOD
PP5V_S0_CPUVTTS0

Vout = 1.05V
11.5A Max Output
f = 300 kHz

OCP = R7641 x 8.5mA / R7640
Vout = 0.5V * (1 + Ra / Rb)
NOTE: Pulled up to 5V on DP connector page. FET spec’ed for 1.5V Vgs operation.

Q9302  Ssignal_model=DP_AUXCH_FET  SSM6N37F EAPE  SOT563

C9302  3300PF 10%  10V  X7R

R9302  MF  1/20W  5%  201

External DisplayPort Support

SYNC_MASTER=K16_MLB  SYNC_DATE=07/07/2010

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A

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

FSB Clock Constraints

MCP FSB COMP Signal Constraints

CPU Signal Constraints

Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 270 ps.

Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.

Signals within each 4x group should be matched within 5 ps of strobe.

Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.1

SOURCE: Santa Rosa Platform DG, Rev 1.3 (A22241), Sections 4.4 & 4.5

CPU/FSB Constraints

MCP FSB COMP Signal Constraints

RULES

FSB Clock Constraints

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.1.4

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.1
PCI-Express

SATA Interface Constraints

Source: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.6

DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.

DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 100 ps.

Source: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.1.

- 75-ohm from output of three-pole filter to connector (if possible).
- 50-ohm from first to second termination resistor.

CRT signal single-ended impedence varies by location:

Analog Video Signal Constraints

NEED PCIe Gen1/Gen2 notes!

Source: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.3

Digital Video Signal Constraints

PCI-Express

MCP89 Net Properties

MCP Constraints 1

Apple Inc.

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### SD Card Interface Constraints

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<td>MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4</td>
<td>- Platform-specific constraints for SD Card interfaces</td>
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### SD Card Net Properties

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<tbody>
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<td>SD_D&lt;7..5&gt;</td>
<td>Different to support different controllers.</td>
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### SD_55S Interface

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### Ethernet Net Properties

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<td>ENET_RESET_L</td>
<td>- Minimum length constraints for Ethernet reset lines</td>
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<tr>
<td>ENET_MDI_N&lt;3..0&gt;</td>
<td>- Minimum length constraints for Ethernet MDI pins</td>
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### MCP RGMII (Ethernet) Constraints

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<td>ENET_CLK125M_RXCLK_R</td>
<td>- Clock delay constraints for RGMII RXCLK pin</td>
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### RGMII Net Properties

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### Ethernet Constraints

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### Electrical Constraints

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<td>SD_55S</td>
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### Note

- SD Card interfaces have specific constraints to support different controllers.
- Ethernet interfaces have specific delay constraints for RGMII RXCLK pin.
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<tr>
<th>NET_ID</th>
<th>NET_NAME</th>
<th>NET_TYPE</th>
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**SMC SMBus Net Properties**

**SMC SMBus Charger Net Properties**
K99 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

| TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | TABLE_PHYSICAL_RULE_ITEM | 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A

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**10UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS**

**SAMSUNG**

**MURATA**

**TAIYO YUDEN**

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**2.2UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS**

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