### Bar Code Label / EEE #'s

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>630-9516</td>
<td>LBL, P/N LABEL, PCB, 28MM X 6 MM</td>
<td>CRITICAL</td>
<td>EEE:4DA</td>
</tr>
<tr>
<td>630-9514</td>
<td>LBL, P/N LABEL, PCB, 28MM X 6 MM</td>
<td>CRITICAL</td>
<td>EEE:4DB</td>
</tr>
<tr>
<td>630-9735</td>
<td>LBL, P/N LABEL, PCB, 28MM X 6 MM</td>
<td>CRITICAL</td>
<td>EEE:4DC</td>
</tr>
<tr>
<td>630-9734</td>
<td>LBL, P/N LABEL, PCB, 28MM X 6 MM</td>
<td>CRITICAL</td>
<td>EEE:2AL</td>
</tr>
</tbody>
</table>

### Module Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>376S0410</td>
<td>IC, GMCP, MCP79U-B01, 27MMX27MM, BGA1588</td>
<td>CRITICAL</td>
<td>EEE:2AP</td>
</tr>
<tr>
<td>376S0411</td>
<td>IC, GMCP, MCP79U-B02, 27MMX27MM, BGA1588</td>
<td>CRITICAL</td>
<td>EEE:2AN</td>
</tr>
<tr>
<td>376S0627</td>
<td>IC, ISL6258, REV2, BAT CHGR, 28P QFN</td>
<td>CRITICAL</td>
<td>EEE:4DB</td>
</tr>
</tbody>
</table>

### Alternate Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>337S3658</td>
<td>IC, PRGRM, SMC (NEW), M96</td>
<td>CRITICAL</td>
<td>EEE:4DC</td>
</tr>
<tr>
<td>338S0637</td>
<td>IC, 32MBIT 8-PIN SERIAL FLASH, WSON8</td>
<td>CRITICAL</td>
<td>EEE:4DA</td>
</tr>
</tbody>
</table>

### BOMS

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>376S0466</td>
<td>EEE:2AN</td>
</tr>
<tr>
<td>376S0723</td>
<td>EEE:2AP</td>
</tr>
<tr>
<td>152S0684</td>
<td>EEE:2AN</td>
</tr>
<tr>
<td>333S0475</td>
<td>EEE:4DC</td>
</tr>
<tr>
<td>333S0476</td>
<td>EEE:4DA</td>
</tr>
</tbody>
</table>

### BOM OPTION Groups

<table>
<thead>
<tr>
<th>BOM OPTION</th>
<th>CRITICAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU_1_8GHZ</td>
<td>CRITICAL</td>
</tr>
<tr>
<td>CPU_1_6GHZ</td>
<td>CRITICAL</td>
</tr>
</tbody>
</table>
### 1UF 0402 Capacitor Vendor Tables for Acoustics

<table>
<thead>
<tr>
<th>Vendor</th>
<th>Part Number</th>
<th>QTY</th>
<th>Description</th>
<th>Reference Des</th>
<th>Critical</th>
<th>BOM Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>SAMSUNG</td>
<td>138S0626</td>
<td>10</td>
<td>CAP, 2.2UF, 6.3V, 20%, 0402</td>
<td></td>
<td></td>
<td>CRITICAL</td>
</tr>
<tr>
<td></td>
<td>138S0632</td>
<td>12</td>
<td>CAP, 10UF, 6.3V, 20%, 0603</td>
<td></td>
<td></td>
<td>CRITICAL</td>
</tr>
<tr>
<td>TAIYO YUDEN</td>
<td>138S0625</td>
<td>5</td>
<td>CAP, 1UF, 6.3V, 10%, 0402</td>
<td></td>
<td></td>
<td>CRITICAL</td>
</tr>
</tbody>
</table>

### 2.2UF 0402 Capacitor Vendor Tables for Acoustics

<table>
<thead>
<tr>
<th>Vendor</th>
<th>Part Number</th>
<th>QTY</th>
<th>Description</th>
<th>Reference Des</th>
<th>Critical</th>
<th>BOM Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>SAMSUNG</td>
<td>138S0627</td>
<td>5</td>
<td>CAP, 2.2UF, 6.3V, 20%, 0402</td>
<td></td>
<td></td>
<td>CRITICAL</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3</td>
<td>CAP, 10UF, 6.3V, 20%, 0603</td>
<td></td>
<td></td>
<td>CRITICAL</td>
</tr>
<tr>
<td>TAIYO YUDEN</td>
<td>138S0630</td>
<td>7</td>
<td>CAP, 1UF, 6.3V, 10%, 0402</td>
<td></td>
<td></td>
<td>CRITICAL</td>
</tr>
</tbody>
</table>

### 10UF 0603 Capacitor Vendor Tables for Acoustics

<table>
<thead>
<tr>
<th>Vendor</th>
<th>Part Number</th>
<th>QTY</th>
<th>Description</th>
<th>Reference Des</th>
<th>Critical</th>
<th>BOM Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>SAMSUNG</td>
<td></td>
<td>10</td>
<td>CAP, 2.2UF, 6.3V, 20%, 0402</td>
<td></td>
<td></td>
<td>CRITICAL</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5</td>
<td>CAP, 10UF, 6.3V, 20%, 0603</td>
<td></td>
<td></td>
<td>CRITICAL</td>
</tr>
<tr>
<td>TAIYO YUDEN</td>
<td></td>
<td>2</td>
<td>CAP, 1UF, 6.3V, 10%, 0402</td>
<td></td>
<td></td>
<td>CRITICAL</td>
</tr>
</tbody>
</table>

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SYNC FROM M97
CPU VCORE HF AND BULK DECOUPLING

- Intel recommends 3x220UF @ 9mOHM
- 10UF 0603 = APN:138S0568 = MURATA,TAIYO,TDK,SAMSUNG
- C1270 330UF CRITICAL
- C1260 C1240 CRITICAL
- C1230 2.2UF
- C1220 6.3V 20%
- D2T-SM1 20%
- 1x 330UF, 12X 2.2UF
- MAKE_BASE=TRUE
- CPU VCORE VID CONNECTIONS
- VCCA (CPU AVdd) DECOUPLING
- VCCP (CPU I/O) DECOUPLING
- CPU Decoupling & VID

**LAYOUT NOTE:**
- PLACE ON OPPOSITE SIDE OF CPU
- PLACE ON SAME SIDE AS CPU

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**SYNC_DATE=04/26/2006**

**DRAWING NUMBER**
- 051-7631

**www.vinafix.vn**
WF: Checklist says 0-ohm resistor placeholder for ferrite bead.
WF: 1 ohm (1k) in 0.25W, in 0.1uf 0402 (1.6k ohm)
Apple: 1 ohm (1k) in 0.1uf 0402 (1.6k ohm)

MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.4 MM
=PP1V05_S0_MCP_HDMI_VDD
=PP3V3R1V8_S0_MCP_IFP_VDD
=PP3V3_S0_MCP_VPLL_UF
PP3V3_S0_MCP_DAC
SYNC FROM M97
CHANGED RTC POWER SOURCE TO DIRECT CONNECTION
ADDED MCPSEQ_SMC LOGIC
FEF/DDR3 Vref Margining

Required zero ohm resistors when no VREF margining circuit stuff

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BCM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>116350094</td>
<td>3</td>
<td>RES,MTL FILM,0,5%,0402,SM,LF</td>
<td>R2922</td>
<td>CRITICAL</td>
<td>NO_VREFMRGN</td>
</tr>
<tr>
<td>116350095</td>
<td>3</td>
<td>RES,MTL FILM,0,5%,0402,SM,LF</td>
<td>R2923</td>
<td>CRITICAL</td>
<td>NO_VREFMRGN</td>
</tr>
</tbody>
</table>
DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.

Before 1.5V starts to rise to avoid glitch on MEM_RESET_L.

3.3V input must be stable before R3010

1K

C3000

10%
6.3V
X5R
0.1UF

R3000

10K
5%

Q3005

SOT-363-LF
MMDT3904-X-G
MEMRESET_HW

Q3005

SOT-363-LF
MMDT3904-X-G
MEMRESET_HW

R3005

20K

Www.vinafix.vn
MEM CLOCK TERMINATION
Place RC end termination after last DRAM
Place Source there at backbone at first DRAM

JEDEC recommends 30 Ohm term to VTT for CS, CKE, ODT and 36 Ohm for BA, A, RAS, CAS, WE
Micro-DisplayPort / USB to RIO Hatch Assembly

Audio Connector

Hatch and Audio Connectors
USB 2.0 CONNECTOR

CONNECT TO 5V S5 or S3 PER LAYOUT

DUAL SWITCH HAS GANGED OUTPUT
BOTH SWITCHES WILL TRIP TOGETHER AT 1.5A-2.2A

USB/SMC MUX

PLACE NEAR U4675
USB/SMC MUXED

PLACE NEAR U4675
USB DEBUG PRT EN L

USB DEBUG PRT EN R
USB_CONN_3923

USB DEBUG PRT EN
USB_CONN_3923

USB EXTERNAL CONNECTORS

USB EXTERNAL CONNECTORS

<table>
<thead>
<tr>
<th>REF. DESIGNATION</th>
<th>VALUE</th>
<th>PARTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>R4677</td>
<td>1M</td>
<td></td>
</tr>
<tr>
<td>C4675</td>
<td>0.1UF</td>
<td></td>
</tr>
<tr>
<td>R4650</td>
<td>1K</td>
<td></td>
</tr>
<tr>
<td>C4650</td>
<td>0.47UF</td>
<td></td>
</tr>
<tr>
<td>L4600</td>
<td>90-OHM-100MA</td>
<td></td>
</tr>
<tr>
<td>D4600</td>
<td></td>
<td>CRITICAL</td>
</tr>
<tr>
<td>R4650</td>
<td>1K</td>
<td>CERM-X5R</td>
</tr>
<tr>
<td>C4612</td>
<td>0.01UF</td>
<td></td>
</tr>
</tbody>
</table>

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INSTRUCTIONS FOR USE

1. Place R4675 near U4675.
2. Place C4612 near U4675.
3. Place L4600 near U4675.
4. Place D4600 near U4675.
5. Place C4650 near U4675.
6. Place R4650 near U4675.

USB EXTERNAL CONNECTORS

<table>
<thead>
<tr>
<th>REF. DESIGNATION</th>
<th>VALUE</th>
<th>PARTS</th>
</tr>
</thead>
<tbody>
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<td></td>
</tr>
<tr>
<td>R4650</td>
<td>1K</td>
<td></td>
</tr>
<tr>
<td>C4650</td>
<td>0.47UF</td>
<td></td>
</tr>
<tr>
<td>L4600</td>
<td>90-OHM-100MA</td>
<td></td>
</tr>
<tr>
<td>D4600</td>
<td></td>
<td>CRITICAL</td>
</tr>
<tr>
<td>R4650</td>
<td>1K</td>
<td>CERM-X5R</td>
</tr>
<tr>
<td>C4612</td>
<td>0.01UF</td>
<td></td>
</tr>
</tbody>
</table>

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INSTRUCTIONS FOR USE

1. Place R4675 near U4675.
2. Place C4612 near U4675.
3. Place L4600 near U4675.
4. Place D4600 near U4675.
5. Place C4650 near U4675.
6. Place R4650 near U4675.
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Inverted to drive SMC_RESET logic

PLACE R4800, R4801 UNDER L4800

Critical

Power Button Inverter

Inverted to drive SMC_RESET logic

IPD Connector

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ACIN VOLTAGE SENSE

MAX 16.5V ± 10% ACIN = 3.0V SMACIN_VSENSE

R5300 and R5301 values chosen for RC filter @ 4.53Kohm thevenin resistance

MCP VOLTAGE SENSE

R5310 and R5310 values chosen for RC filter @ 4.53Kohm thevenin resistance

PBUS VOLTAGE SENSE

R5315 and R5315 values chosen for RC filter @ 4.53Kohm thevenin resistance

**Voltage Sensors**

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For more information, please visit [www.vinafix.vn](http://www.vinafix.vn).
MCP VCore Current Sense

MCP VCore Current Sense Filter

PBUS Current Sense

Current Sensing

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REV. A

SYNC_DATE=02/04/2008

SYNC_MASTER=YUNWU
CPU/MCP T-Diode Thermal Sensor

LOCAL TEMP NEAR FRONT EDGE

LOCAL TEMP NEAR AIR VENT

LOCAL TEMP NEAR POWER SUPPLIES

(Write: 0x90 Read: 0x91)

(Write: 0x92 Read: 0x93)

(Write: 0x92 Read: 0x93)

(Write: 0x92 Read: 0x93)
Sudden Motion Sensor (SMS)

Desired orientation when placed on board top-side:

Circle indicates pin 1 location when placed in correct orientation.
and the power button is depressed.

generated when left shift, option, and control

critical

WTB-PWR-M82

J6900

Critical

PP18V5_DCIN

MIN_NECK_WIDTH=0.2 mm

MIN_LINE_WIDTH=0.25 mm

VOLTAGE=18.5V

D6900

G

S

2

1

SYS_ONEWIRE_BILAT

2

1

SC-75

3

805

MF-LF

1/8W

5%

12

12

805

MF-LF

1/8W

5%

C6994

22PF

201

50V

5%

C6995

22PF

201

50V

5%

C6999

22UF

CERM

6.3V

20%

R6990

R6931

100K

200K

1/16W

5%

200K

1/16W

5%

R6940

12

12

1/20W

201

MF

1%

1/20W

201

MF

1%

R6911

47K

1/16W

5%

201

MF-LF

5%

10

R6940

FERR-50-OHM

12

L6995

Critical

Critical

Vout = 1.25V * (1 + Ra / Rb)

Vout = 3.425V

Other max output

(Witcher output limit)

Q6990 will pull down

protected mes 1 in the event

generated when left shift, option, and control

and the power button is depressed.

supply needs to guarantee 3.31V delivered to SMC VRef generator

Supply needs to guarantee 3.31V delivered to SMC VRef generator
1.8V S0 LDO

- PPVIN S0 PIUSO = PPVIN S0 REG
- CRITICAL
- P1V8S0_NR = P1V8S0_EN
- 1.8V LDO Supply
- TPS79918
- C7360
- C7361
- C7362
- 1.8V S0 LDO

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www.vinafix.vn
1V05 S5 POWER SUPPLY

supply for MCP1V05 AUX, FSB (CPU & MCP) VTT, 1V05 S0
1.5V/0.75V POWER SUPPLY

<table>
<thead>
<tr>
<th>State</th>
<th>PM_S4_STATE_L</th>
<th>PM_SLP_S3</th>
<th>PP1V5_S3</th>
<th>PP0V75_S0</th>
</tr>
</thead>
<tbody>
<tr>
<td>S0</td>
<td>HIGH</td>
<td>HIGH</td>
<td>1.5V</td>
<td>0.75V</td>
</tr>
<tr>
<td>S3</td>
<td>HIGH</td>
<td>LOW</td>
<td>1.5V</td>
<td>0.0V</td>
</tr>
<tr>
<td>S5/G3Hot</td>
<td>LOW</td>
<td>LOW</td>
<td>0.0V</td>
<td>0.0V</td>
</tr>
</tbody>
</table>

Vout = 0.75V * (1 + Ra / Rb)

Routing Note:
- 402-1 X5R 10V 10%
- 402 X5R 16V 10%
- 1UF C7500
- 0.033UF C7502
- OMIT C7540

Routing Note:
- Place XW7502 near L7520
- C7511 2.2UF 402-LF CERM

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Scale
Size
Drawing Number
Sht
Rev.
Date
Notice of Proprietary Property
1.5V/0.75V Supplies
PWM FREQ. = 400 kHz
MAX CURRENT = 5.35A??
(AC adapter limited?)
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DRAWING NUMBER
SHT
OF
SIZE
D

REV.

87
6
5
4
3
2
1

2.3.0

PPBUS_S0_LCDBKLT_EN_DIV = PPBUS_S0_LCDBKLT
MIN_NECK_WIDTH = 0.25 mm
VOLTAGE = 12.6V
MIN_LINE_WIDTH = 0.4 mm

PPBUS_S0_LCDBKLT_PWR
PPBUS_S0_LCDBKLT_EN_L
PPBUS_S0_LCDBKLT_FUSED

LCDBKLT_ENA

BKLT_PWM

LVDS_IG_BKL_PWM

LVDS_IG_BKL_ON

MIN_NECK_WIDTH = 0.25 mm
VOLTAGE = 12.6V
MIN_LINE_WIDTH = 0.4 mm

SYNC_DATE = 02/04/2008
SYNC_MASTER = M97

APPLE INC.
D 051-7631

www.vinafix.vn
Most CPU signals with impedance requirements are 50-ohm single-ended.

Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.

FSB 2x signals / groups shown in signal table on right.

DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.

<table>
<thead>
<tr>
<th>Physical Rule Set</th>
<th>Layer</th>
<th>Line-to-Line Spacing</th>
<th>Allow Route</th>
<th>Weight</th>
</tr>
</thead>
<tbody>
<tr>
<td>FSB 1x</td>
<td></td>
<td>2x Dielectric</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSB 1x</td>
<td></td>
<td>3x Dielectric</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSB 1x</td>
<td></td>
<td>4x Dielectric</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSB 1x</td>
<td></td>
<td>5x Dielectric</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSB 2x</td>
<td></td>
<td>100_ohm_diff</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSB 2x</td>
<td></td>
<td>50_ohm_se</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSB 2x</td>
<td></td>
<td>3x Dielectric</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSB 2x</td>
<td></td>
<td>2x Dielectric</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Timing Constraint</th>
<th>Layer</th>
<th>Net Type</th>
<th>Matched To</th>
<th>Weight</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU_VCCSENSE</td>
<td></td>
<td>CPU_50S</td>
<td></td>
<td>50_ohm_se</td>
</tr>
<tr>
<td>CPU_50S</td>
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<td>50_ohm_se</td>
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<td>50_ohm_se</td>
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<td>50_ohm_se</td>
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<td>FSB_DSTB_50S</td>
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<td>FSB_1X</td>
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</tr>
</tbody>
</table>

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Max length of LVDS/DisplayPort/TMDS traces: 12 inches.

DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.

- 75-ohm from output of three-pole filter to connector (if possible).

Analog Video Signal Constraints

Luke-Express

PHYSICAL RULE SET

CRT_2SWITCHER

CLK_PCIE_100D

MCP_DV_COMP

SATA_TERMP

CRT_SYNC

CRT_2CRT

CLK_PCIE

LAYER

LAYER

LAYER

LAYER

LAYER

LAYER

LAYER

LAYER

100_OHM_DIFF_HDD = 100_OHM_DIFF

ALLOW ROUTE ON LAYER?

= 3x_DIELECTRIC

MINIMUM LINE WIDTH

MINIMUM NECK WIDTH

MAXIMUM NECK LENGTH

DIFFPAIR PRIMARY GAP

DIFFPAIR NECK GAP

TABLE PHYSICAL RULE HEAD

TABLE PHYSICAL RULE ITEM

TABLE PHYSICAL RULE ITEM

TABLE PHYSICAL RULE ITEM

TABLE PHYSICAL RULE ITEM

TABLE PHYSICAL RULE ITEM

TABLE PHYSICAL RULE ITEM

WEIGHT

WEIGHT

WEIGHT

WEIGHT

WEIGHT

WEIGHT

TABLE SPACING RULE HEAD

TABLE SPACING RULE ITEM

TABLE SPACING RULE ITEM

TABLE SPACING RULE ITEM

TABLE SPACING RULE ITEM

TABLE SPACING RULE ITEM

TABLE SPACING RULE ITEM

MINIMUM NECK WIDTH

MINIMUM NECK LENGTH

MAXIMUM NECK LENGTH

DIFFPAIR PRIMARY GAP

DIFFPAIR NECK GAP

TABLE PHYSICAL RULE HEAD

TABLE PHYSICAL RULE ITEM

TABLE PHYSICAL RULE ITEM

TABLE PHYSICAL RULE ITEM

TABLE PHYSICAL RULE ITEM

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TABLE SPACING RULE HEAD

TABLE SPACING RULE ITEM

TABLE SPACING RULE ITEM

TABLE SPACING RULE ITEM

TABLE SPACING RULE ITEM

TABLE SPACING RULE ITEM

TABLE SPACING RULE ITEM
# Device Interface Constraints

## USB 2.0 Interface Constraints

Source: MCP Interface DG (DG-03328-001_v0D), Section 2.9.1.

### PHYSICAL_RULE_SET

- **SPACING_RULE_SET**
  - **MCP_USB_RBIAS**
  - **CLK_SLOW_55S**
  - **MCP_HDA_COMP**
  - **SMB_55S**
  - **USB_90D**
  - **LPC_55S**
  - **PCI_55S**
  - **SPI**
  - **SMB**
  - **USB**

### LAYER

- **LINE-TO-LINE SPACING**
  - **ON LAYER?**
  - **ALLOW ROUTE**
  - **=55_OHM_SE**
  - **=2x_DIELECTRIC**
  - **=8_MIL**
  - **=STANDARD**

### TABLE_PHYSICAL_RULE_ITEM

- **MINIMUM LINE WIDTH**
  - **MINIMUM NECK WIDTH**
  - **MAXIMUM NECK LENGTH**
  - **DIFFPAIR PRIMARY GAP**
  - **DIFFPAIR NECK GAP**

## SPI Interface Constraints

Source: MCP Interface DG (DG-03328-001_v0D), Section 1.9.

### TABLE_PHYSICAL_RULE_ITEM

- **TABLE_SPACING_RULE_ITEM**
  - **TABLE_SPACING_RULE_HEAD**
  - **TABLE_SPACING_RULE_ITEM**
  - **TABLE_SPACING_RULE_ITEM**
  - **TABLE_PHYSICAL_RULE_ITEM**
  - **TABLE_PHYSICAL_RULE_ITEM**
  - **TABLE_PHYSICAL_RULE_ITEM**
  - **TABLE_PHYSICAL_RULE_ITEM**

---

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### SMBus Charger Net Properties

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<th>NET_TYPE</th>
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<th>PHYSICAL</th>
<th>SPACING</th>
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<tbody>
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<td>Sync Date = 02/04/2008, SYNC_MASTER = M97</td>
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### SMC SMBus Net Properties

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<th>SPACING</th>
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</table>

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### Table 1: Physical Rules

<table>
<thead>
<tr>
<th>Layer</th>
<th>Isolation Type</th>
<th>Rule Set</th>
<th>Min Width</th>
<th>Min Neck Width</th>
<th>Max Neck Length</th>
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<tbody>
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<td>1.1:1 Spacing</td>
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<td>0.120 MM</td>
<td>0.066 MM</td>
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<tr>
<td>C</td>
<td>3:1 Spacing</td>
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<td>0.220 MM</td>
<td>0.132 MM</td>
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<tr>
<td>D</td>
<td>4:1 Spacing</td>
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<td>0.575 MM</td>
<td>0.180 MM</td>
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</tr>
</tbody>
</table>

### Table 2: Spacing Rules

| Line/Neck | Layer | Rule Set | Min D 1 | Min D 2 | Min D 3 | Min D 4 | Min D 5 | Min D 6 | Min D 7 | Min D 8 | Min D 9 | Min D 10 | Min D 11 | Min D 12 | Min D 13 | Min D 14 | Min D 15 | Min D 16 | Min D 17 | Min D 18 | Min D 19 | Min D 20 | Min D 21 | Min D 22 | Min D 23 | Min D 24 | Min D 25 | Min D 26 | Min D 27 | Min D 28 | Min D 29 | Min D 30 | Min D 31 | Min D 32 | Min D 33 | Min D 34 | Min D 35 | Min D 36 | Min D 37 | Min D 38 | Min D 39 | Min D 40 | Min D 41 | Min D 42 | Min D 43 | Min D 44 | Min D 45 | Min D 46 | Min D 47 | Min D 48 | Min D 49 | Min D 50 | Min D 51 | Min D 52 | Min D 53 | Min D 54 | Min D 55 | Min D 56 | Min D 57 | Min D 58 | Min D 59 | Min D 60 | Min D 61 | Min D 62 | Min D 63 | Min D 64 | Min D 65 | Min D 66 | Min D 67 | Min D 68 | Min D 69 | Min D 70 | Min D 71 | Min D 72 | Min D 73 | Min D 74 | Min D 75 | Min D 76 | Min D 77 | Min D 78 | Min D 79 | Min D 80 | Min D 81 | Min D 82 | Min D 83 | Min D 84 | Min D 85 | Min D 86 | Min D 87 | Min D 88 | Min D 89 | Min D 90 | Min D 91 | Min D 92 | Min D 93 | Min D 94 | Min D 95 | Min D 96 | Min D 97 | Min D 98 | Min D 99 | Min D 100 |