Modify from Acer request. (7/11)
Charge Current max setting = 0.8C
DDR2 1.8 V, 667 MT/s (2 Channel) 3200mA
When the LVDS interface is not implemented, the VCCA_LVDS, VCCD_LVDS, and VCCA_LVDSA signals of the interface can be connected to ground.

**A1A:** Change to 470UF

**A1A:** Change to 22UF

**B1B:** CRT disable

**B1B:** Remove R282 for +1.5V_AUX

**B1B:** CRT disable

**B1B:** TV disable

**B1B:** Remove R282 for +1.5V_AUX

**B1B:** CRT disable

**B1B:** CRT disable

**B1B:** TV disable

**B1B:** CRT disable

**B1B:** TV disable

**B1B:** CRT disable

**B1B:** TV disable

**B1B:** CRT disable

**B1B:** TV disable

**B1B:** CRT disable

**B1B:** TV disable
B1B: Change C562 to CH7222KMJ82 (ME height limit H=1.8)

B1B: Change +3V_S5 to +3V

B1B: Change +3V_S5 to +3V

to prevent leakage