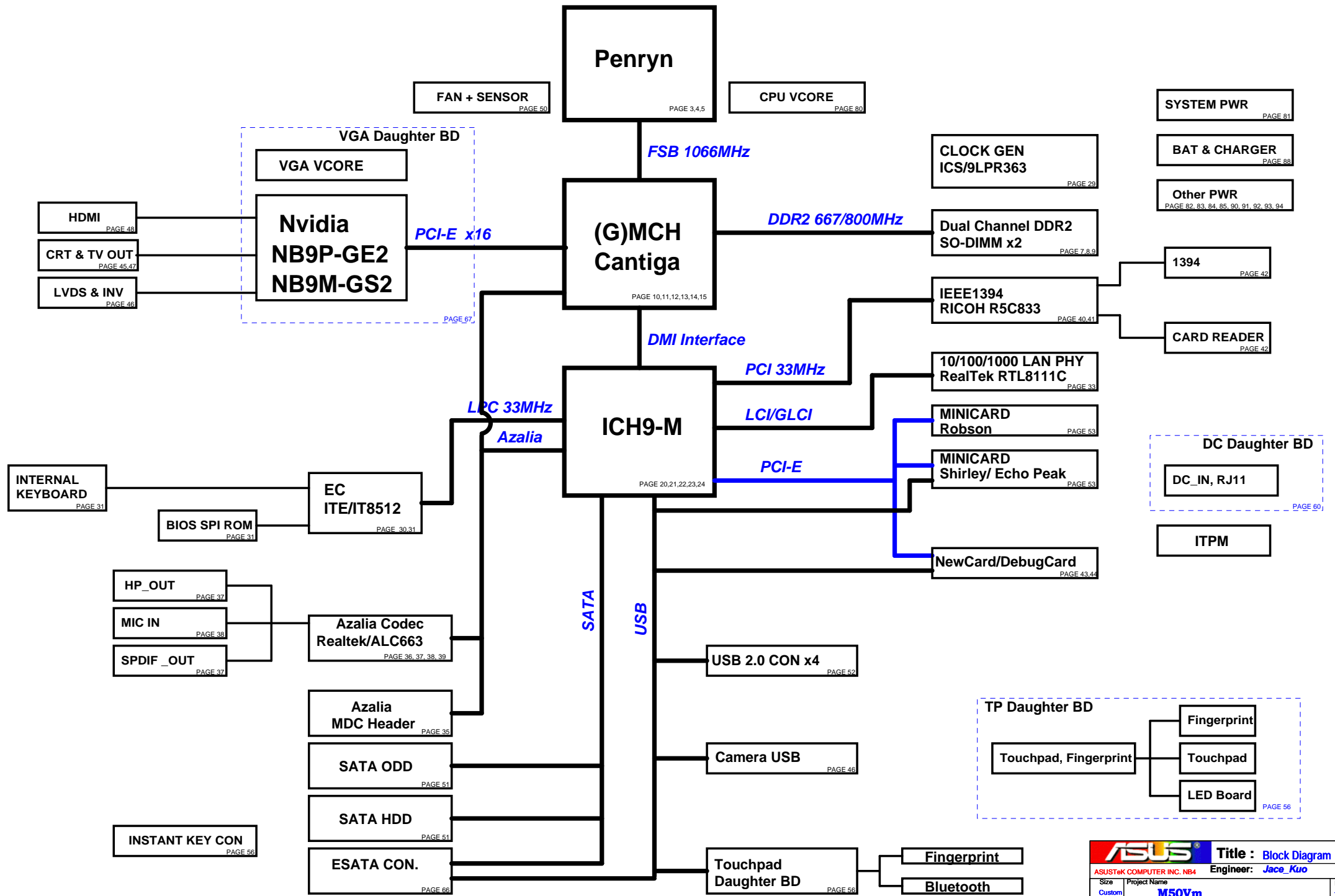


M50Vm Montevina Block Diagram



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ICH9-M GPIO	Use As	Signal Name	Power
GPIO 00	GPI	PM_SYNC#	+3VS
GPIO 01	GPI	-	+3VS
GPIO [2:5]	GPI	PCI_INT[E:H]#	+3VS
GPIO 06	GPI	SIO_SMI#	+3VS
GPIO 07	GPI	WLAN_LED_ON	+3VS
GPIO 08	GPI	EXT_SMI#	+3VSUS
GPIO 09	GPI	LAN_WOL_EN	+3VSUS
GPIO 10	GPI	SUSPWR_ACK	+3VSUS
GPIO 11	GPI	EXT_SCI#	+3VSUS
GPIO 12	GPO	-	+3VSUS
GPIO 13	GPI	-	+3VSUS
GPIO 14	GPI	AC_PRESENT	+3VSUS
GPIO 15	Native	STP_PCI#	+3VSUS
GPIO 16	Native	PM DPRSLPVR	+3VS
GPIO 17	GPI	WLAN_ON#	+3VS
GPIO 18	GPO	PD_RST#	+3VS
GPIO 19	GPI	-	+3VS
GPIO 20	GPO	-	+3VS
GPIO 21	GPI	-	+3VS
GPIO 22	GPI	-	+3VS
GPIO 23	Native	LPC_DRQ1#	+3VS
GPIO 24	GPO	PD_EN	+3VSUS
GPIO 25	Native	STP_CPU#	+3VSUS
GPIO 26	Native	PM_S4_STATE#	+3VSUS
GPIO 27	GPO	BT_ON	+3VSUS
GPIO 28	GPO	CB_SD#	+3VSUS
GPIO 29	Native	USB_OC#5	+3VSUS
GPIO 30	Native	USB_OC#6	+3VSUS
GPIO 31	Native	USB_OC#7	+3VSUS
GPIO 32	GPO	PM_CLKRUN#	+3VS
GPIO 33	GPO	-	+3VS
GPIO 34	GPO	-	+3VS
GPIO 35	GPO	-	+3VS
GPIO 36	GPI	EMAIL_LED#	+3VS
GPIO 37	GPI	PCB_ID0	+3VS
GPIO 38	GPI	PCB_ID1	+3VS
GPIO 39	GPI	PCB_ID2	+3VS
GPIO 40	Native	USB_OC#1	+3VSUS
GPIO 41	Native	USB_OC#2	+3VSUS
GPIO 42	Native	USB_OC#3	+3VSUS
GPIO 43	Native	USB_OC#4	+3VSUS
GPIO 44	Native	USB_OC#8#	N/A
GPIO 45	Native	USB_OC9#	N/A
GPIO 46	Native	USB_OC10#	N/A
GPIO 47	Native	USB_OC11#	N/A
GPIO 48	GPI	-	+3VS
GPIO 49	GPO	HDTV_EN#	+3VS
GPIO 50	Native	PCI_REQ#1	+3VS
GPIO 51	Native	-	+3VS
GPIO 52	Native	PCI_REQ#2	+3VS
GPIO 53	Native	-	+3VS
GPIO 54	Native	PCI_REQ#3	+3VS
GPIO 55	Native	-	+3VS
GPIO 56	-	-	+3VSUS
GPIO 57	GPI	-	+3VSUS
GPIO 58	GPI	SPI_CS#1	+3VSUS
GPIO 59	Native	USB_OC0#	+3VSUS
GPIO 60	Native	-	+3VSUS

EC GPIO	Use As	Signal Name	Power
GPA0	GPO	PWR_LED_UP#	
GPA1	GPO	CHG_LED_UP#	
GPA2	GPO	BATSEL_3S#	
GPA3	-	-	
GPA4	GPO	LCD_BL_PWM	
GPA5	GPO	FAN0_PWM	
GPA6	GPO	BAT1_CNT1#	
GPA7	GPO	BAT2_CNT1#	
GPB0	GPO	CHG_EN#	
GPB1	GPO	PRECHG	
GPB2	GPI	DISTP#	
GPB3	ALT	SMB0_CLK	
GPB4	ALT	SMB0_DAT	
GPB5	OD	A20GATE	
GPB6	OD	RCIN#	
GPB7	GPO	PM_RSMRST#	
GPC0	GPI	MARATHON#	
GPC1	ALT	SMB1_CLK	
GPC2	ALT	SMB1_DAT	
GPC3	GPO	PM_PWRBTN#	
GPC4	ALT	AC_IN_OC#	
GPC5	GPO	OP_SD#	
GPC6	ALT	BAT1_IN_OC#	
GPC7	GPO	3G_ON#	
GPD0	GPI	PWRLIMIT#	
GPD1	ALT	PM_S4_STATE#	
GPD2	ALT	BUF_PLT_RST#	
GPD3	OD	EXT_SCI#	
GPD4	OD	EXT_SMI#	
GPD5	GPO	LCD_BACKOFF#	
GPD6	ALT	FAN0_TACH	
GPD7	GPI	COLOREN#	
GPE0	GPO	VSUS_ON	
GPE1	GPO	SUSC_EC#	
GPE2	GPO	SUSB_EC1#	
GPE3	GPO	CPU_VRON	
GPE4	ALT	PWR_SW#	
GPE5	ALT	BAT2_IN_OC#	
GPE6	GPI	LID_SW#	
GPE7	GPO	PM_THERM#	
GPFO	GPI	BLUETOOTH#	
GPF1	GPI	WIRELESS#	
GPF2	ALT	PS2_CLK_5S_PD	
GPF3	ALT	PS2_DATA_5S_PD	
GPF4	ALT	TP_CLK	
GPF5	ALT	TP_DAT	
GPF6	GPO	THRO_CPU	
GPF7	GPO	PS_SHDN#	
GPFO	GPI	INSTANT_ON#	
GPG1	ALT	PM_SUSB#	
GPG2	GPO	BAT1_CNT2#	
-	-	-	
-	-	-	

EC GPIO	Use As	Signal Name	Power
-	-	-	
GPG6	GPO	BAT2_CNT2#	
-	-	-	
GPH0	OD	PM_CLKRUN#	
GPH1	ALT	-	
GPH2	ALT	-	
GPH3	GPO	BAT_LEARN	
GPH4	GPO	-	
GPH5	GPO	NUM_LED	
GPH6	GPO	CAP_LED	
-	-	-	
GP10	GPI	-	
GP11	GPI	SUS_PWRGD	
GP12	GPI	ALL_SYSTEM_PWRGD	
GP13	GPI	VRM_PWRGD	
GP14	GPI	PWR_MON	
GP15	GPI	PD_DET#	
GP16	GPI	KB_ID0	
GP17	GPI	KB_ID1	
GPJ0	GPO	EC_CLK_EN	
GPJ1	GPO	PM_PWROK	
GPJ2	GPI	UNDOCK#_PD	
GPJ3	-	-	
GPJ4	GPO	BL_DA	
GPJ5	GPO	FAN_DA	
GPK0	GPI	PM_SLP_M#	
GPK1	GPI	SUSPWR_ACK	
GPK2	GPI	PM_SUSC#	
GPK3	GPI	+3VM_PG	
GPK4	GPI	+1.05VM_+3VMCLK_PG	
GPK5	GPI	LAN_WOL_EN	
GPL0	GPI	AC_APR_UC#	
GPL1	GPI	-	
GPL2	GPO	-	
GPL3	GPO	LAN_RST#	
GPL4	GPO	CL_PWROK	
GPL5	GPO	EC_WLAN_PWR	
GPL6	GPO	SLP_M_ON	
GPL7	GPO	S4_STATE_ON	
GPK6	GPO	AC_PRESENT	
GPK7	GPI	PS_CPPE#	
-	-	-	
-	-	-	

10 H_D#[63:0] \hookrightarrow H_D#[63:0]
 10 H_A#[35:3] \hookrightarrow H_A#[35:3]
 10 H_REQ#[4:0] \hookrightarrow H_REQ#[4:0]

U0301A

ADDR GROUP 0

H_A#3 J4 A[3]#
 H_A#4 L5 A[4]#
 H_A#5 L4 A[5]#
 H_A#6 K5 A[6]#
 H_A#7 M3 A[7]#
 H_A#8 N2 A[8]#
 H_A#9 J1 A[9]#
 H_A#10 N3 A[10]#
 H_A#11 P5 A[11]#
 H_A#12 P2 A[12]#
 H_A#13 L2 A[13]#
 H_A#14 P4 A[14]#
 H_A#15 R1 A[15]#
 H_A#16 M1 A[16]#

CONTROL

ADSR# H1 H_ADS# 10
 BPR# E2 H_BNR# 10
 G5 H_BPR# 10
 DEFER# H5 H_DEFER# 10
 DRDY# E21 H_DRDY# 10
 DBSY# E1 H_DBSY# 10
 BR0# F1 H_BR0# 10
 IERR# D20 H_IERR# 2
 INIT# B3 H_INIT# 20
 LOCK# H4 H_LOCK# 10
 C1 H_CPURST# 30
 RS[0]# F3 H_RS#0 10
 RS[1]# F4 H_RS#1 10
 RS[2]# G3 H_RS#2 10
 TRDY# G2 H_TRDY# 10
 REQ[0]# K3
 REQ[1]# H2
 REQ[2]# J3
 REQ[3]# L1
 REQ[4]#

ADDR GROUP 1

H_A#17 Y2 A[17]#
 H_A#18 U5 A[18]#
 H_A#19 R3 A[19]#
 H_A#20 W6 A[20]#
 H_A#21 U4 A[21]#
 H_A#22 Y5 A[22]#
 H_A#23 U1 A[23]#
 H_A#24 R4 A[24]#
 H_A#25 T5 A[25]#
 H_A#26 T3 A[26]#
 H_A#27 W2 A[27]#
 H_A#28 W5 A[28]#
 H_A#29 Y4 A[29]#
 H_A#30 U2 A[30]#
 H_A#31 V4 A[31]#
 H_A#32 W3 A[32]#
 H_A#33 A4 A[33]#
 H_A#34 A2 A[34]#
 H_A#35 A3 A[35]#

STANDBY/SIGNAL

XDP/ITP#
 PREQ# AC1 H_PREQ#
 TCK AC5 H_TCK
 TDI AA6 H_TDI
 TDO AB3 H_TDO
 TMS AB5 H_TMS
 TRST# AB6 H_TRST#
 DBR# C20 H_DBR#

THERMAL

PROCHOT# D21 H_PROCHOT_S#
 THRMDC A24 CPU_THRM_DA 50
 THRMDC B25 CPU_THRM_DC 50
 THERMTRIP# C7 H_THERMTRIP# 5,20,32

H CLK

BCLK[0] A22
 BCLK[1] A21

RESERVED

RSVD1 M4
 RSVD2 N5
 RSVD3 T2
 RSVD4 V3
 RSVD5 B2
 RSVD6 C3
 RSVD7 D2
 RSVD8 D22
 RSVD9 D3
 RSVD10 F6

U0301B

DATA GRP 0

H_D#0 E22 D[0]#
 H_D#1 E24 D[1]#
 H_D#2 E26 D[2]#
 H_D#3 G22 D[3]#
 H_D#4 F23 D[4]#
 H_D#5 G25 D[5]#
 H_D#6 E25 D[6]#
 H_D#7 E23 D[7]#
 H_D#8 K24 D[8]#
 H_D#9 G24 D[9]#
 H_D#10 J24 D[10]#
 H_D#11 L23 D[11]#
 H_D#12 H22 D[12]#
 H_D#13 F26 D[13]#
 H_D#14 K22 D[14]#
 H_D#15 H23 D[15]#
 J26 DSTBN[0]#
 H26 DSTBN[1]#
 H25 DINV[0]#

DATA GRP 1

H_D#16 N22 D[16]#
 H_D#17 K25 D[17]#
 H_D#18 P26 D[18]#
 H_D#19 R23 D[19]#
 H_D#20 L23 D[20]#
 H_D#21 M24 D[21]#
 H_D#22 L22 D[22]#
 H_D#23 M23 D[23]#
 H_D#24 P25 D[24]#
 H_D#25 P23 D[25]#
 H_D#26 P22 D[26]#
 H_D#27 T24 D[27]#
 H_D#28 R24 D[28]#
 H_D#29 L25 D[29]#
 H_D#30 T25 D[30]#
 H_D#31 N25 D[31]#
 L26 DSTBN[1]#
 M26 DSTBN[2]#
 N24 DINV[1]#

DATA GRP 2

Y22 H_D#32
 AB24 H_D#33
 V24 H_D#34
 V26 H_D#35
 T22 H_D#36
 T23 H_D#37
 U25 H_D#38
 U23 H_D#39
 Y25 H_D#40
 W22 H_D#41
 Y23 H_D#42
 W25 H_D#43
 AA23 H_D#44
 AA24 H_D#45
 AB25 H_D#46
 Y26 H_D#47
 AA26 H_D#48
 U22 H_D#49

DATA GRP 3

AE24 H_D#48
 AD24 H_D#49
 AA21 H_D#50
 AB22 H_D#51
 AB21 H_D#52
 AC26 H_D#53
 AD20 H_D#54
 AE22 H_D#55
 AF23 H_D#56
 AC25 H_D#57
 AE21 H_D#58
 AF21 H_D#59
 AC22 H_D#60
 AD23 H_D#61
 AF22 H_D#62
 AC23 H_D#63
 AE25 H_D#64
 AF24 H_D#65
 AC20 H_D#66

MISC

COMP[0] R26 H_COMP0
 COMP[1] U26 H_COMP1
 COMP[2] AA1 H_COMP2
 COMP[3] Y1 H_COMP3

DPRSTP# E5 H_DPRSTP# 11,20,80
 DPSP# B5 H_DPSP# 20
 DPWR# D24 H_DPWR# 10
 D6 H_PWRGD 20
 D7 H_CPUSLP# 10
 AE6 PM_PSI# 80

10 H_ADSTB#0
 20 H_A20M#
 20 H_FERR#
 20 H_IGNNE#
 20 H_STPCLK#
 20 H_INTR#
 20 H_NMI#
 20 H_SMI#

T0313
 T0314
 T0320
 T0321
 T0302
 T0303

R0301 2KOhm 1%
 R0302 1KOhm 1%
 R0303 1KOhm 1%
 R0304 2KOhm 1%
 R0305 1KOhm 1%
 R0306 1KOhm 1%
 R0307 1KOhm 1%
 R0308 1KOhm 1%

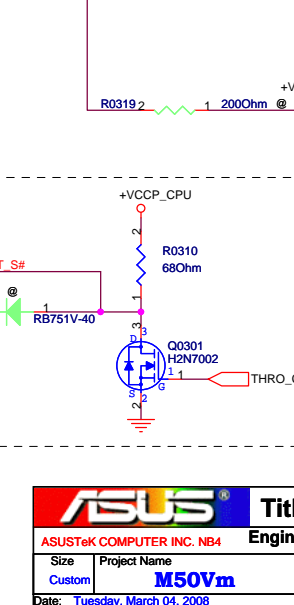
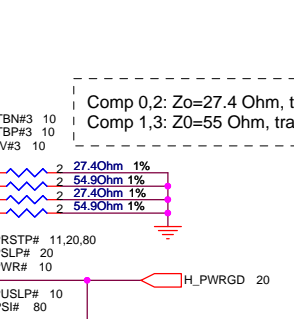
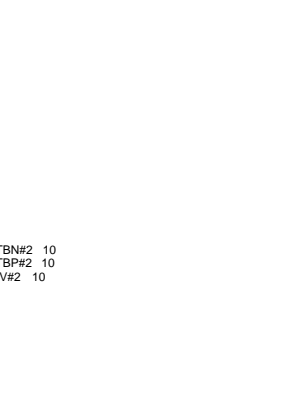
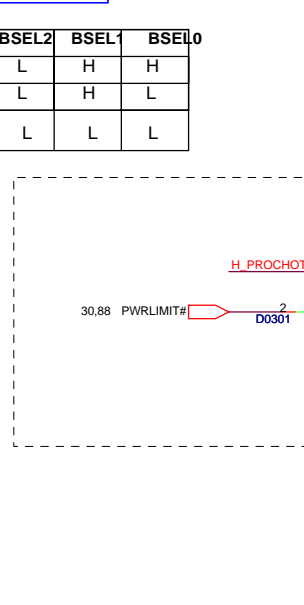
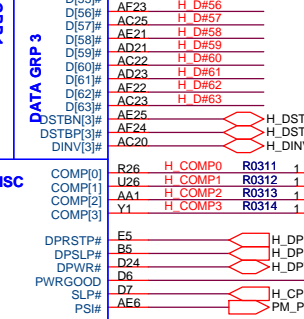
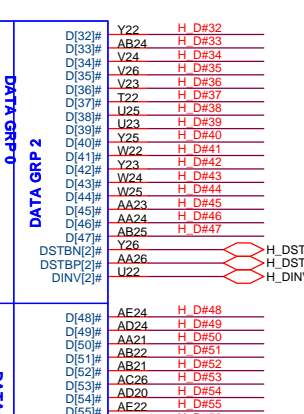
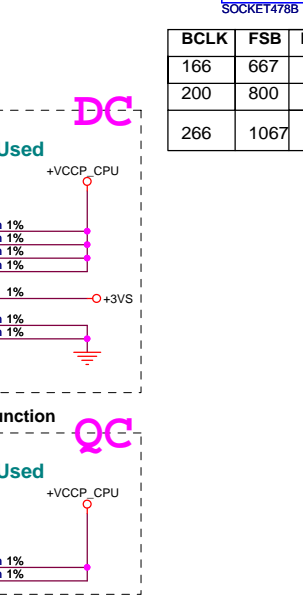
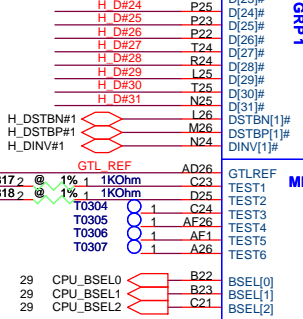
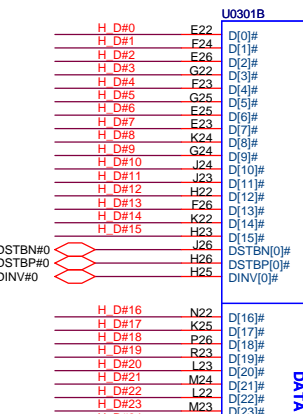
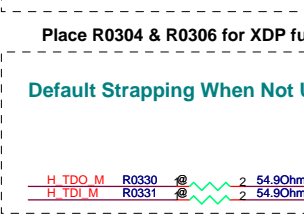
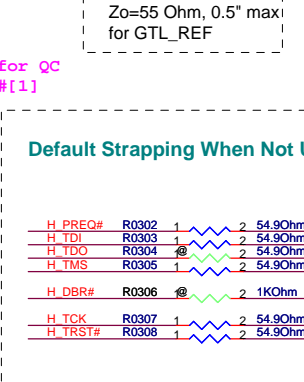
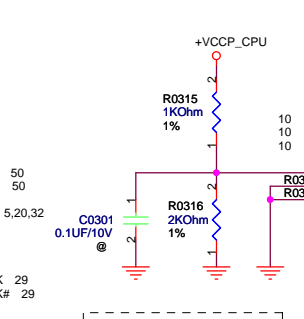
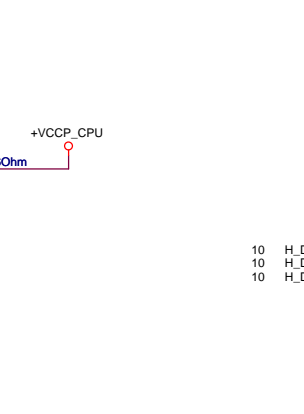
C0302 0.1UF/10V
 C0301 0.1UF/10V
 C0303 0.1UF/10V

R0315 1KOhm 1%
 R0316 2KOhm 1%
 R0317 2KOhm 1%
 R0318 2KOhm 1%
 R0319 1KOhm 1%
 R0320 1KOhm 1%
 R0321 1KOhm 1%
 R0322 1KOhm 1%
 R0323 1KOhm 1%
 R0324 1KOhm 1%
 R0325 1KOhm 1%
 R0326 1KOhm 1%
 R0327 1KOhm 1%
 R0328 1KOhm 1%
 R0329 1KOhm 1%
 R0330 1KOhm 1%
 R0331 1KOhm 1%

C0301 0.1UF/10V
 C0302 0.1UF/10V
 C0303 0.1UF/10V

C0302 0.1UF/10V
 R0301 2KOhm 1%
 R0302 1KOhm 1%
 R0303 1KOhm 1%
 R0304 2KOhm 1%
 R0305 1KOhm 1%
 R0306 1KOhm 1%
 R0307 1KOhm 1%
 R0308 1KOhm 1%

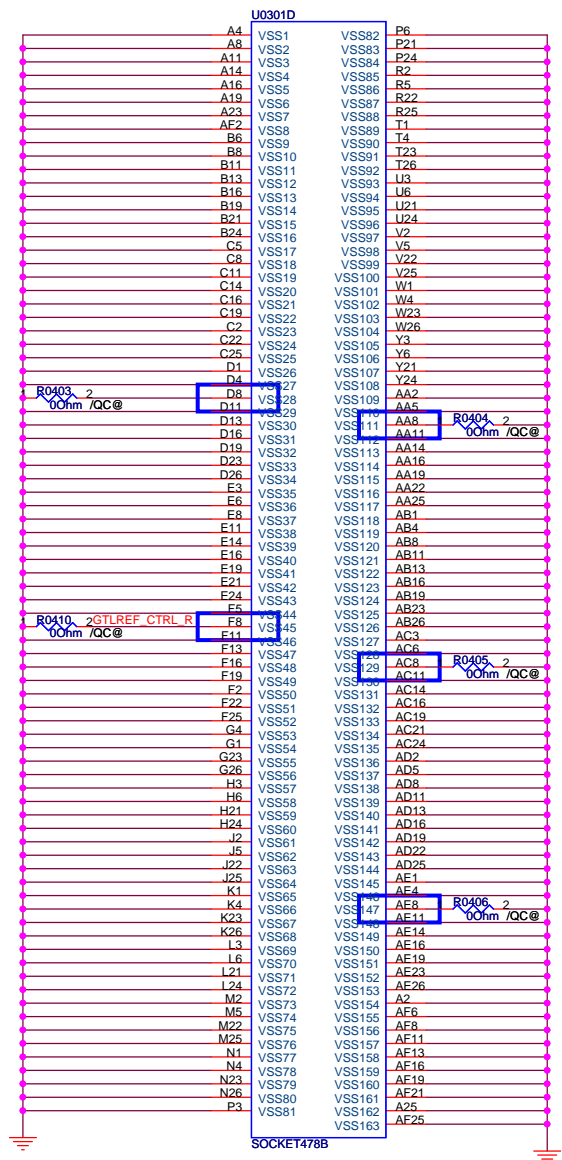
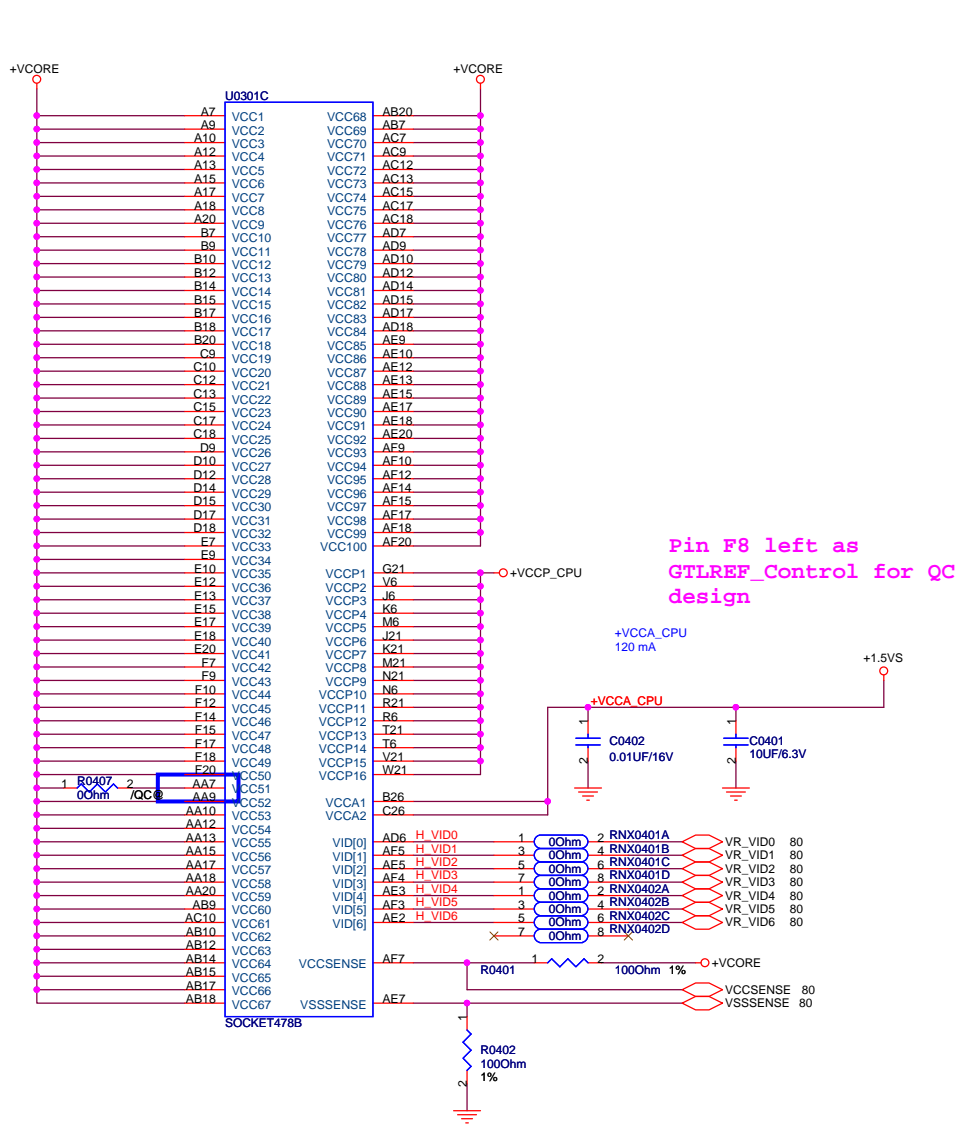
C0302 0.1UF/10V
 R0301 2KOhm 1%
 R0302 1KOhm 1%
 R0303 1KOhm 1%
 R0304 2KOhm 1%
 R0305 1KOhm 1%
 R0306 1KOhm 1%
 R0307 1KOhm 1%
 R0308 1KOhm 1%

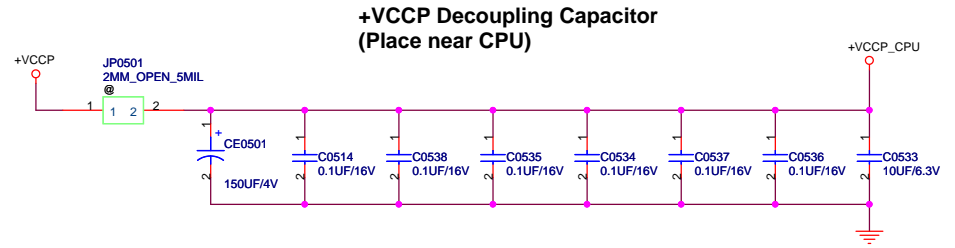
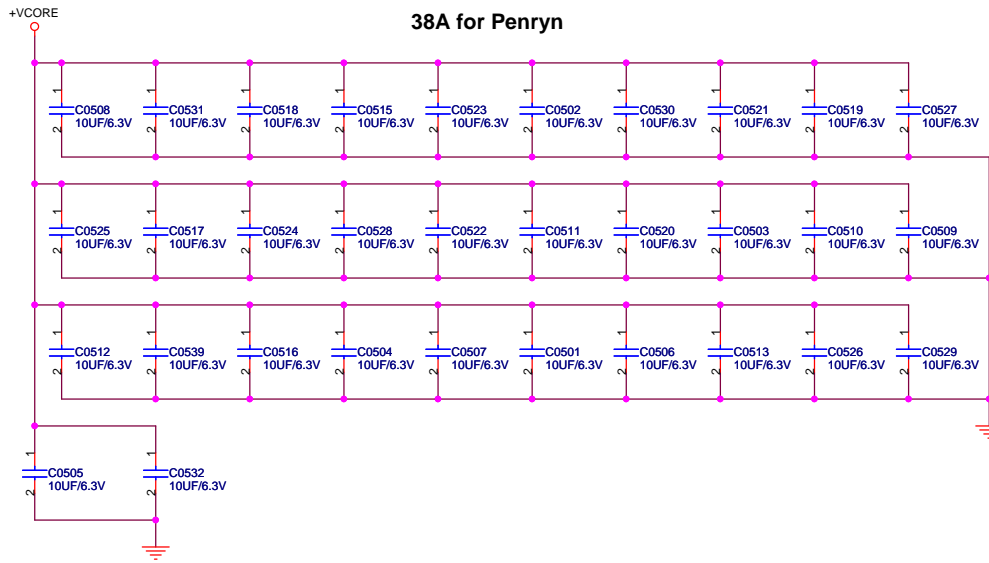


Comp 0,2: Zo=27.4 Ohm, trace length < 0.5"
 Comp 1,3: Zo=55 Ohm, trace length < 0.5"

BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	L	H	H
200	800	L	H	L
266	1067	L	L	L

/QC only QC mount
 /QC@ DC mount



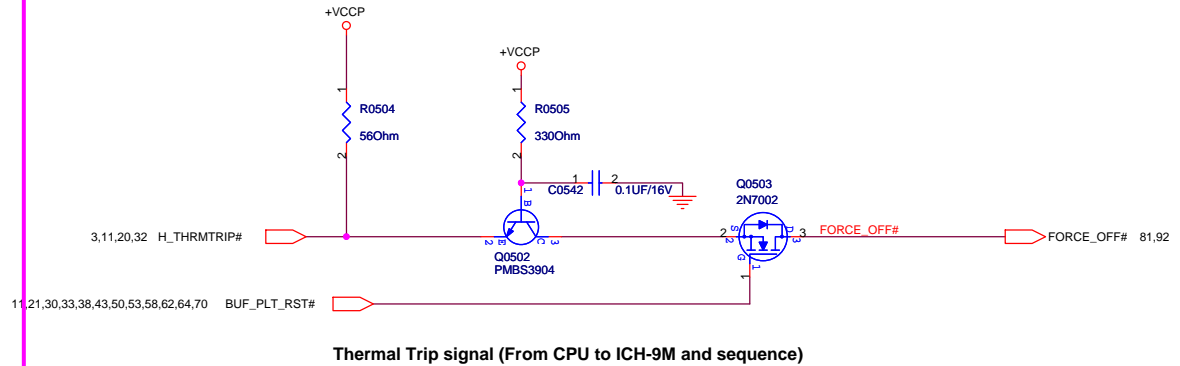
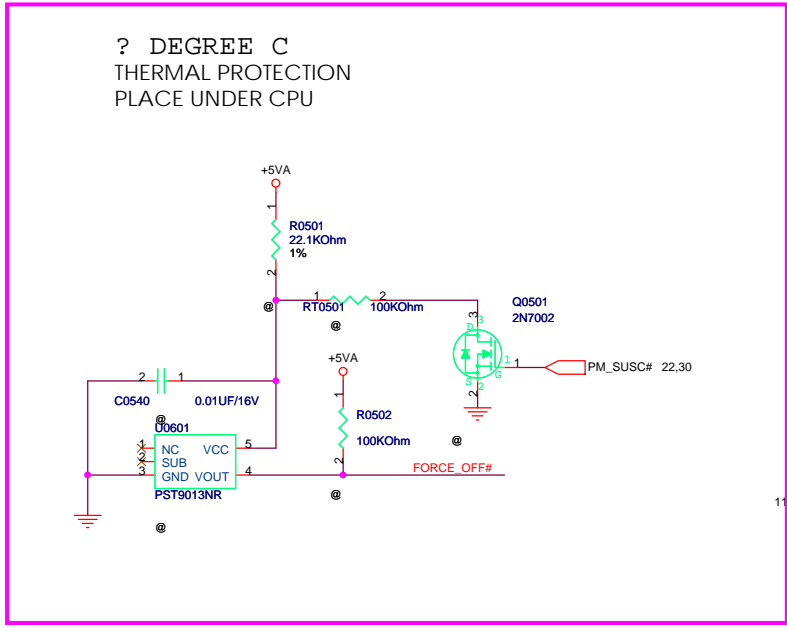


Decoupling guide from Intel

VCCORE	22uF/10V r 10uF	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs
	150uF	* 1pcs ?
	10uF	* 1pcs ?

+VCCORE Mid-Frequency Capacitor
 Intel: 22UF *32
 F3S: 10UF *16
 A7S: 10UF *10 11/17
 V1V: ?

+VCCP Decoupling Capacitor
 Intel: 270UF *1, 0.1UF *6
 F3S: 100UF *1, 0.1UF *4
 V1V: ?



5

4

3

2

1

D

D

C


C

B

B

A

A

		Title :	
ASUSTeK COMPUTER INC. NB6		Engineer:	
Size	Project Name	Rev	
A		1.0	
Date: <u>Wednesday, February 13, 2008</u>		Sheet	<u>6</u> of <u>96</u>

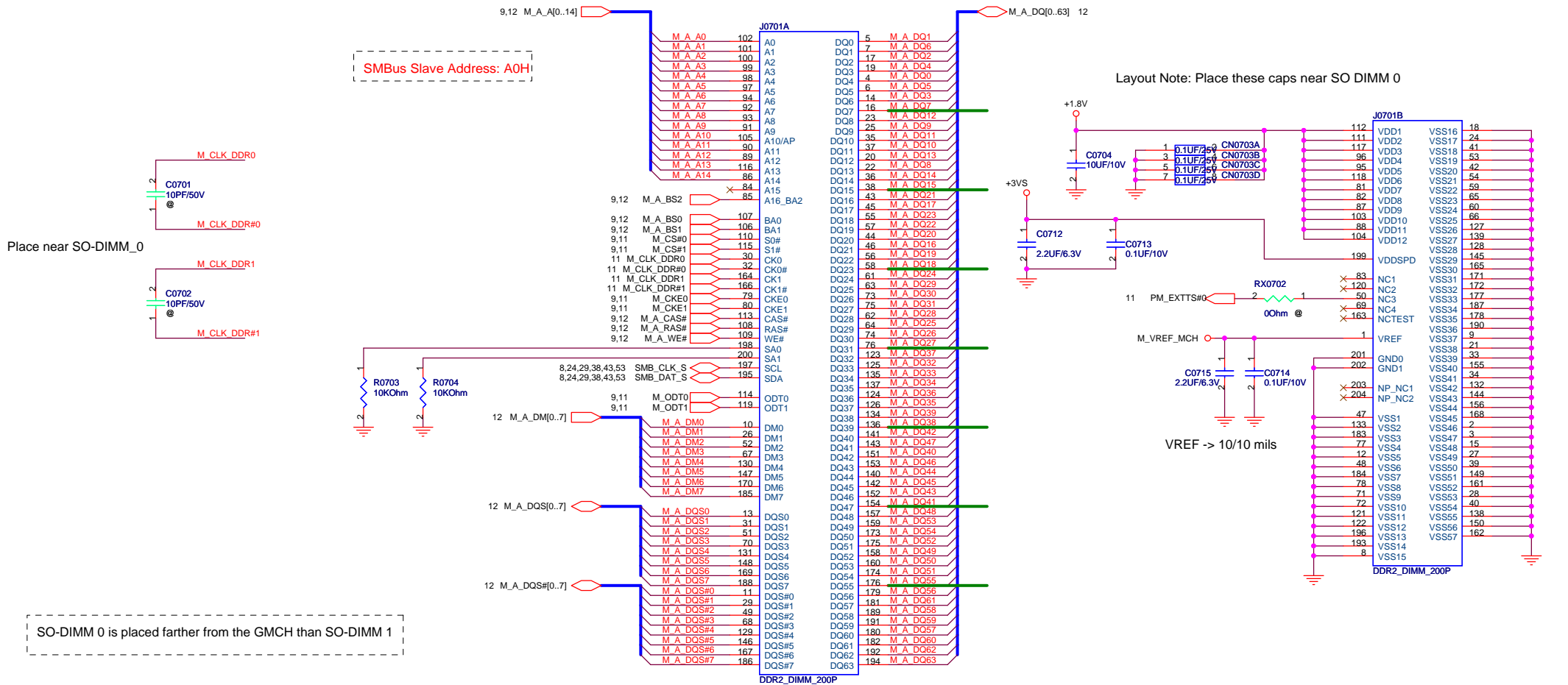
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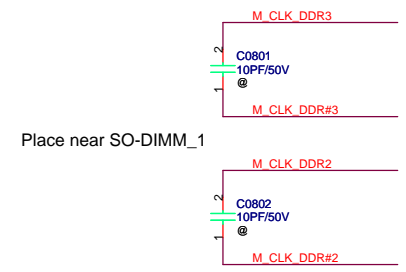
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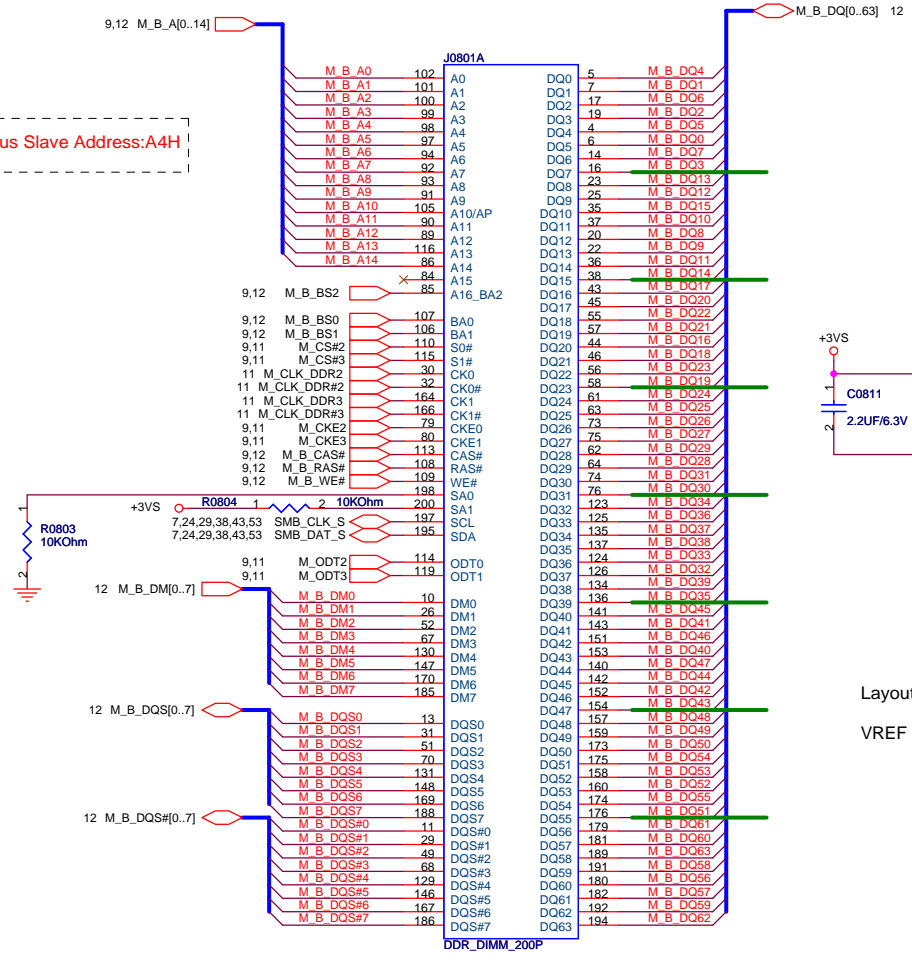
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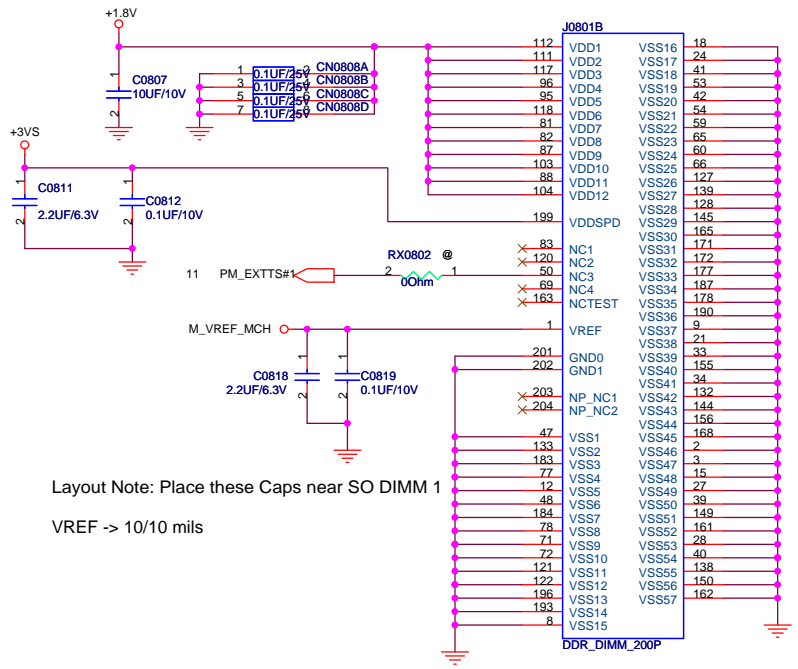
SMBus Slave Address:A4H



Place near SO-DIMM_1

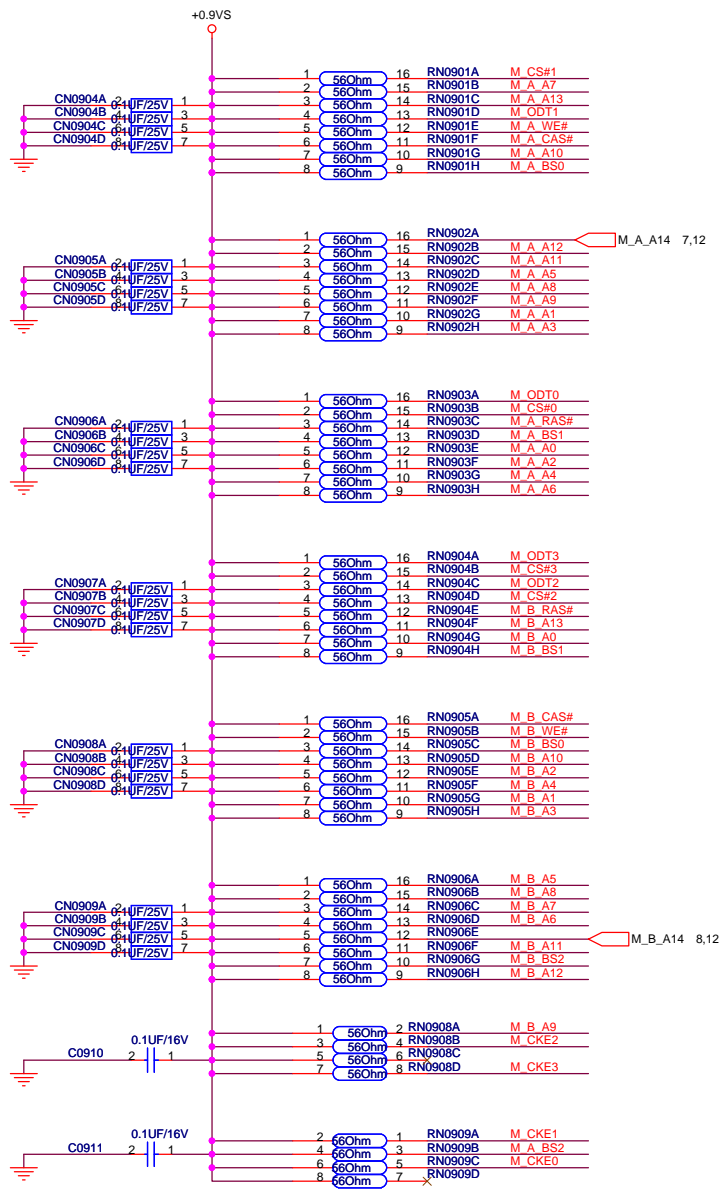
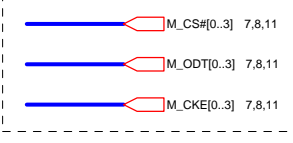
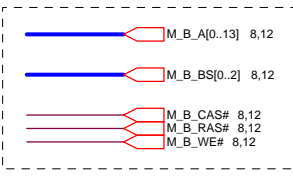
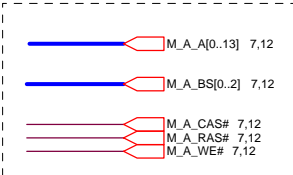
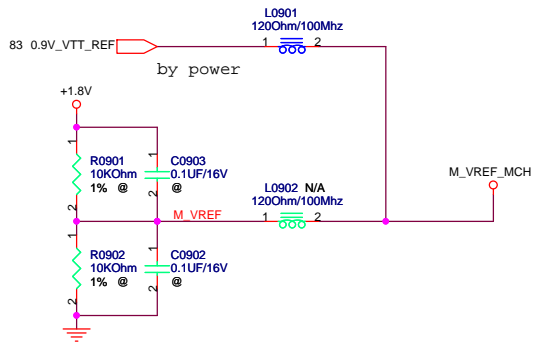


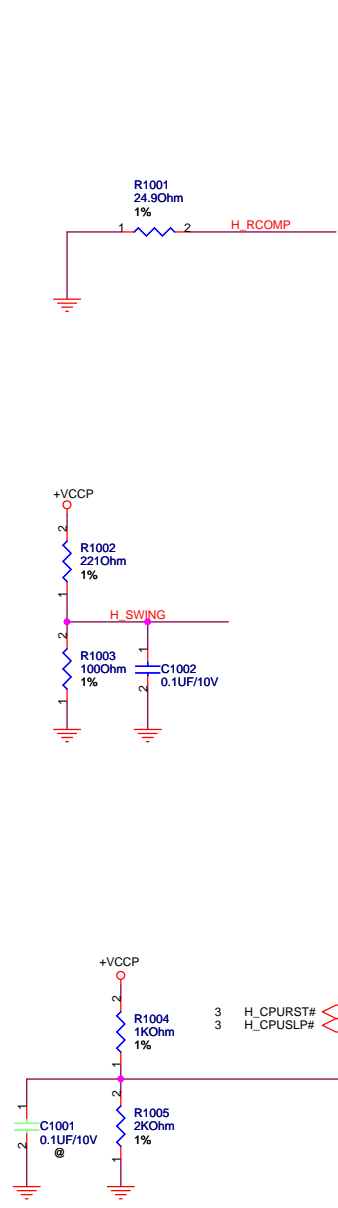
Layout Note: Place these Caps near SO DIMM 1



Layout Note: Place these Caps near SO DIMM 1

VREF -> 10/10 mils



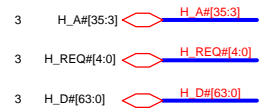


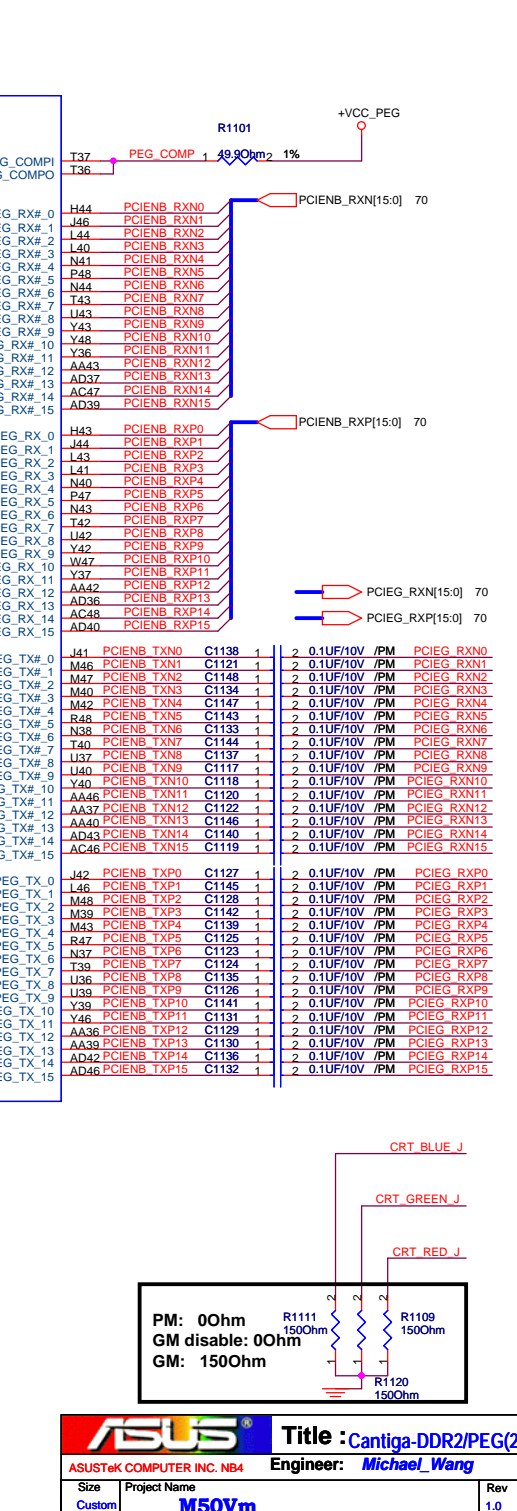
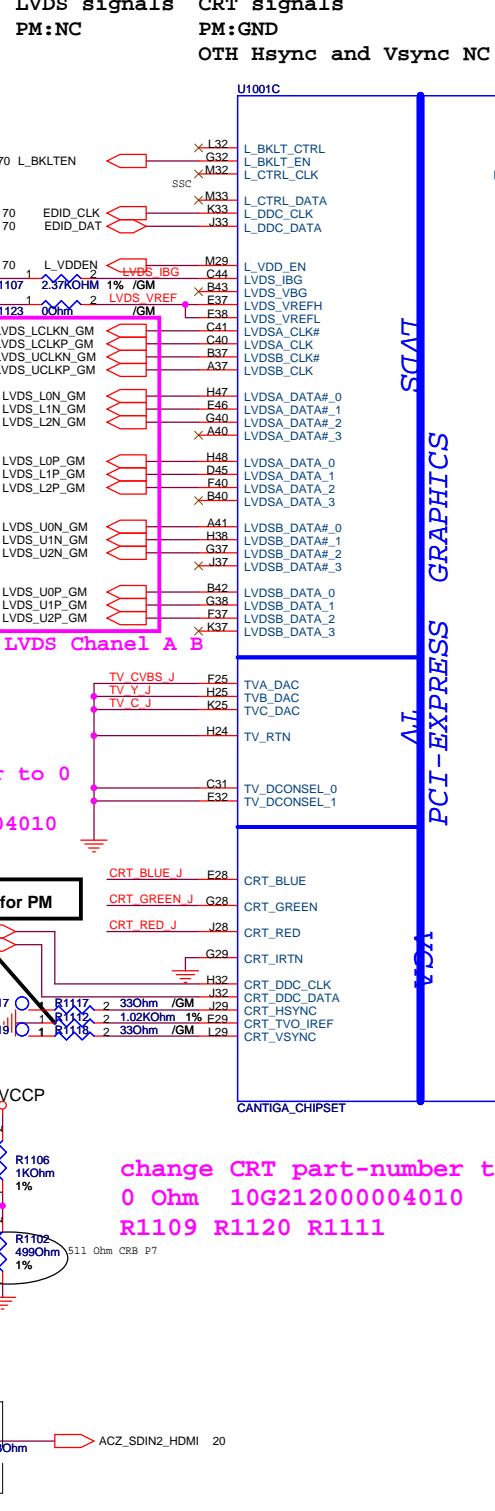
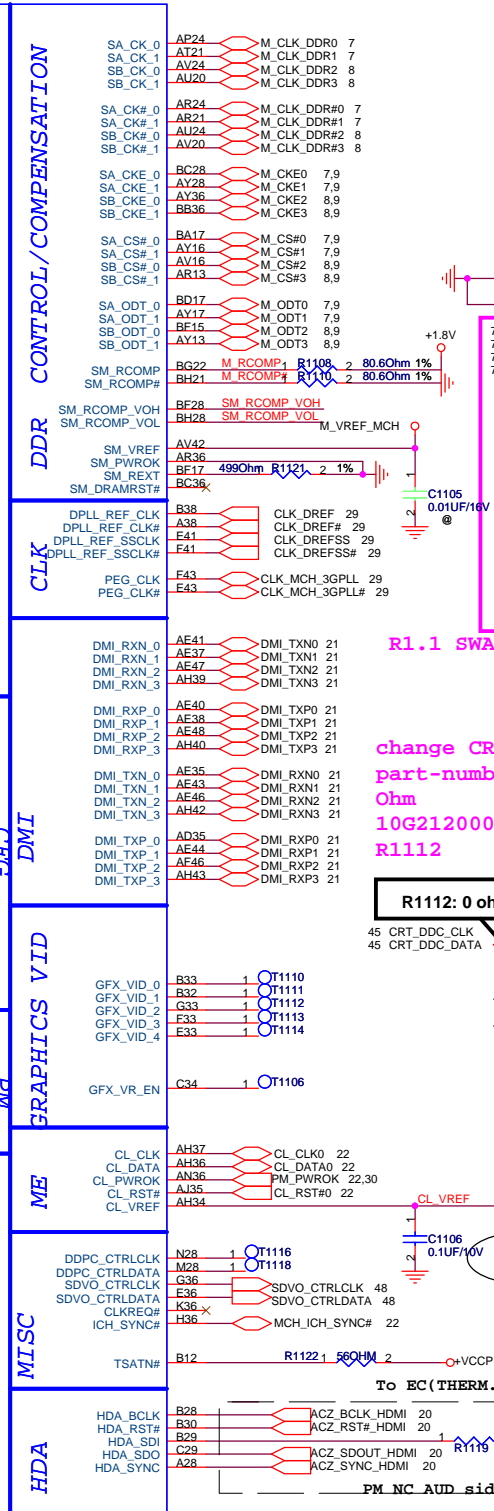
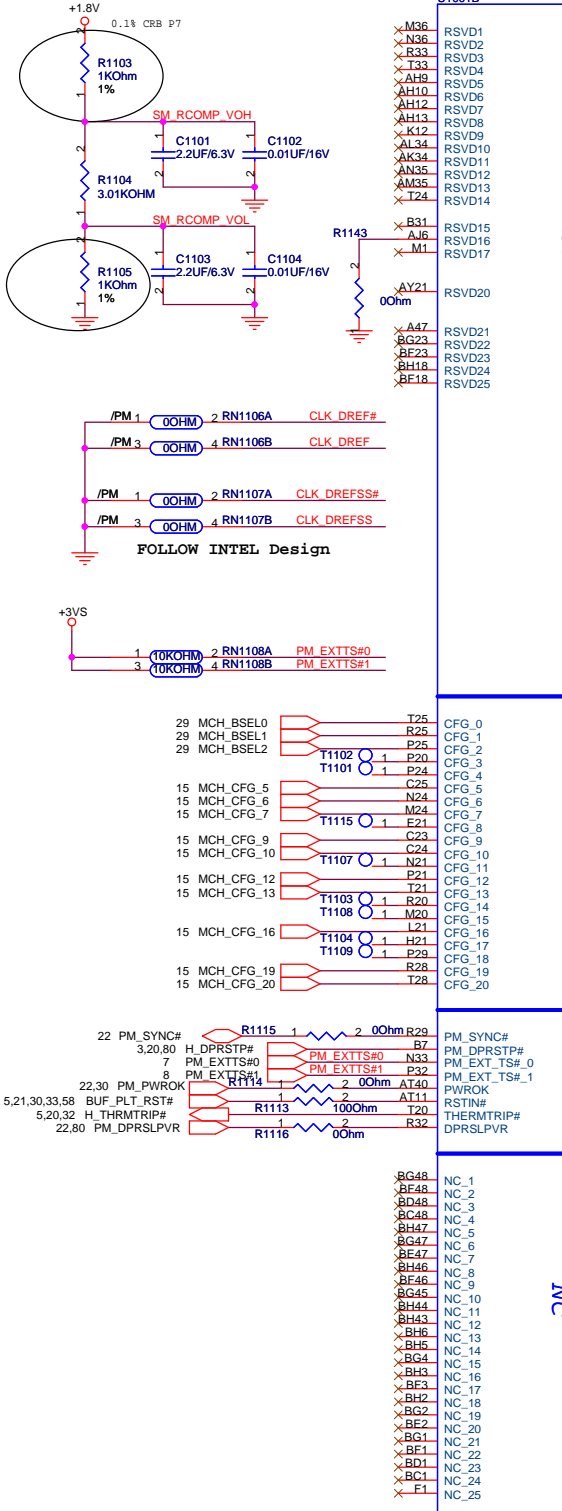
Cap 0.1uF within 500 mils from GMCH

U1001A		CANTIGA_CHIPSET	
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H_D#1	G8	H_D#_1	
H_D#2	F8	H_D#_2	
H_D#3	E6	H_D#_3	
H_D#4	G2	H_D#_4	
H_D#5	H6	H_D#_5	
H_D#6	H2	H_D#_6	
H_D#7	F6	H_D#_7	
H_D#8	D4	H_D#_8	
H_D#9	H3	H_D#_9	
H_D#10	M9	H_D#_10	
H_D#11	M11	H_D#_11	
H_D#12	J1	H_D#_12	
H_D#13	J2	H_D#_13	
H_D#14	N12	H_D#_14	
H_D#15	J6	H_D#_15	
H_D#16	L2	H_D#_16	
H_D#17	R2	H_D#_17	
H_D#18	R2	H_D#_18	
H_D#19	N9	H_D#_19	
H_D#20	L6	H_D#_20	
H_D#21	M5	H_D#_21	
H_D#22	J3	H_D#_22	
H_D#23	N2	H_D#_23	
H_D#24	R1	H_D#_24	
H_D#25	N5	H_D#_25	
H_D#26	N6	H_D#_26	
H_D#27	P13	H_D#_27	
H_D#28	N8	H_D#_28	
H_D#29	L7	H_D#_29	
H_D#30	N10	H_D#_30	
H_D#31	M3	H_D#_31	
H_D#32	Y3	H_D#_32	
H_D#33	AD14	H_D#_33	
H_D#34	Y6	H_D#_34	
H_D#35	Y10	H_D#_35	
H_D#36	Y12	H_D#_36	
H_D#37	Y14	H_D#_37	
H_D#38	Y7	H_D#_38	
H_D#39	W2	H_D#_39	
H_D#40	AA8	H_D#_40	
H_D#41	Y9	H_D#_41	
H_D#42	AA13	H_D#_42	
H_D#43	AA9	H_D#_43	
H_D#44	AA11	H_D#_44	
H_D#45	AD11	H_D#_45	
H_D#46	AD10	H_D#_46	
H_D#47	AD13	H_D#_47	
H_D#48	AE12	H_D#_48	
H_D#49	AE9	H_D#_49	
H_D#50	AA2	H_D#_50	
H_D#51	AD8	H_D#_51	
H_D#52	AA3	H_D#_52	
H_D#53	AD3	H_D#_53	
H_D#54	AD7	H_D#_54	
H_D#55	AE14	H_D#_55	
H_D#56	AE3	H_D#_56	
H_D#57	AC1	H_D#_57	
H_D#58	AE3	H_D#_58	
H_D#59	AC3	H_D#_59	
H_D#60	AE11	H_D#_60	
H_D#61	AE8	H_D#_61	
H_D#62	AG2	H_D#_62	
H_D#63	AD6	H_D#_63	
H_SWING	C5	H_SWING	
H_RCOMP	E3	H_RCOMP	
H_CPURST#		H_CPURST#	
H_CPUSLP#		H_CPUSLP#	
H_VREF		H_VREF	
H_DVREF		H_DVREF	

HOST

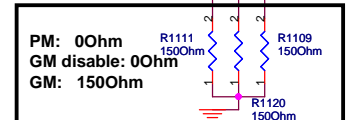
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H_A#_6	H13	H_A#6
H_A#_7	C18	H_A#7
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H_A#_9	J13	H_A#9
H_A#_10	P16	H_A#10
H_A#_11	R16	H_A#11
H_A#_12	N17	H_A#12
H_A#_13	M13	H_A#13
H_A#_14	E17	H_A#14
H_A#_15	P17	H_A#15
H_A#_16	E17	H_A#16
H_A#_17	G20	H_A#17
H_A#_18	B19	H_A#18
H_A#_19	J16	H_A#19
H_A#_20	E20	H_A#20
H_A#_21	H16	H_A#21
H_A#_22	J20	H_A#22
H_A#_23	L17	H_A#23
H_A#_24	A17	H_A#24
H_A#_25	B17	H_A#25
H_A#_26	L16	H_A#26
H_A#_27	C21	H_A#27
H_A#_28	J17	H_A#28
H_A#_29	H20	H_A#29
H_A#_30	B18	H_A#30
H_A#_31	K17	H_A#31
H_A#_32	B20	H_A#32
H_A#_33	F21	H_A#33
H_A#_34	K21	H_A#34
H_A#_35	L20	H_A#35
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H_ADSTB#_1	G17	H_ADSTB#1 3
H_BNR#	A9	H_BNR# 3
H_BPR#	E11	H_BPR# 3
H_BR0#	G12	H_BR0# 3
H_DEFER#	E9	H_DEFER# 3
H_DBSY#	B10	H_DBSY# 3
HPLL_CLK	AH7	CLK_MCH_BCLK# 29
HPLL_CLK#	J11	CLK_MCH_BCLK# 29
H_DPWR#	F9	H_DPWR# 3
H_DRDY#	H9	H_DRDY# 3
H_HIT#	E12	H_HIT# 3
H_LOCK#	H11	H_LOCK# 3
H_TRDY#	C9	H_TRDY# 3
H_DINV#_0	J8	H_DINV#0 3
H_DINV#_1	L3	H_DINV#1 3
H_DINV#_2	Y13	H_DINV#2 3
H_DINV#_3	Y1	H_DINV#3 3
H_DSTBN#_0	L10	H_DSTBN#0 3
H_DSTBN#_1	M7	H_DSTBN#1 3
H_DSTBN#_2	AA5	H_DSTBN#2 3
H_DSTBN#_3	AE6	H_DSTBN#3 3
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H_DSTBP#_2	AA6	H_DSTBP#2 3
H_DSTBP#_3	AE5	H_DSTBP#3 3
H_REQ#_0	B15	H_REQ#0
H_REQ#_1	K13	H_REQ#1
H_REQ#_2	F13	H_REQ#2
H_REQ#_3	B13	H_REQ#3
H_REQ#_4	B14	H_REQ#4
H_RS#_0	B6	H_RS#0 3
H_RS#_1	F12	H_RS#1 3
H_RS#_2	C8	H_RS#2 3





R1.1 SWAP LVDS Channel A B
change CRT part-number to 0 Ohm
10G212000004010
R1112

change CRT part-number to 0 Ohm 10G212000004010
R1109 R1120 R1111

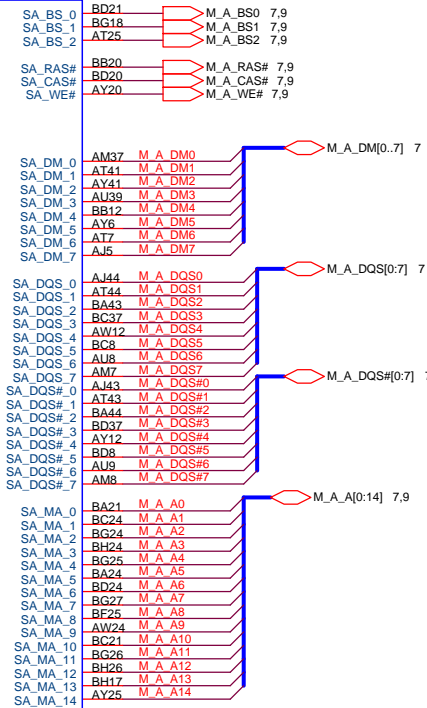


7 M_A_DQ[0:63]

M A DQ0	AJ38	SA_DQ_0
M A DQ1	AJ41	SA_DQ_1
M A DQ2	AN38	SA_DQ_2
M A DQ3	AJ38	SA_DQ_3
M A DQ4	AJ36	SA_DQ_4
M A DQ5	AJ40	SA_DQ_5
M A DQ6	AM44	SA_DQ_6
M A DQ7	AM42	SA_DQ_7
M A DQ8	AN43	SA_DQ_8
M A DQ9	AN44	SA_DQ_9
M A DQ10	AJ40	SA_DQ_10
M A DQ11	AT38	SA_DQ_11
M A DQ12	AN41	SA_DQ_12
M A DQ13	AN39	SA_DQ_13
M A DQ14	AU44	SA_DQ_14
M A DQ15	AU42	SA_DQ_15
M A DQ16	AV39	SA_DQ_16
M A DQ17	AY44	SA_DQ_17
M A DQ18	BA40	SA_DQ_18
M A DQ19	BD43	SA_DQ_19
M A DQ20	AV41	SA_DQ_20
M A DQ21	AY43	SA_DQ_21
M A DQ22	BA41	SA_DQ_22
M A DQ23	BC40	SA_DQ_23
M A DQ24	AY37	SA_DQ_24
M A DQ25	BD38	SA_DQ_25
M A DQ26	AV37	SA_DQ_26
M A DQ27	AT36	SA_DQ_27
M A DQ28	AY38	SA_DQ_28
M A DQ29	BC38	SA_DQ_29
M A DQ30	AV36	SA_DQ_30
M A DQ31	AW36	SA_DQ_31
M A DQ32	BD13	SA_DQ_32
M A DQ33	AU11	SA_DQ_33
M A DQ34	BC11	SA_DQ_34
M A DQ35	BA12	SA_DQ_35
M A DQ36	AU13	SA_DQ_36
M A DQ37	AV13	SA_DQ_37
M A DQ38	BD12	SA_DQ_38
M A DQ39	BC12	SA_DQ_39
M A DQ40	BB9	SA_DQ_40
M A DQ41	BA9	SA_DQ_41
M A DQ42	AU10	SA_DQ_42
M A DQ43	AV9	SA_DQ_43
M A DQ44	BA11	SA_DQ_44
M A DQ45	BD9	SA_DQ_45
M A DQ46	AY8	SA_DQ_46
M A DQ47	BA6	SA_DQ_47
M A DQ48	AV5	SA_DQ_48
M A DQ49	AV7	SA_DQ_49
M A DQ50	AT9	SA_DQ_50
M A DQ51	AN8	SA_DQ_51
M A DQ52	AU5	SA_DQ_52
M A DQ53	AU6	SA_DQ_53
M A DQ54	AT5	SA_DQ_54
M A DQ55	AN10	SA_DQ_55
M A DQ56	AM11	SA_DQ_56
M A DQ57	AM5	SA_DQ_57
M A DQ58	AJ9	SA_DQ_58
M A DQ59	AJ8	SA_DQ_59
M A DQ60	AN12	SA_DQ_60
M A DQ61	AM13	SA_DQ_61
M A DQ62	AJ11	SA_DQ_62
M A DQ63	AJ12	SA_DQ_63

CANTIGA_CHIPSET

DDR SYSTEM MEMORY A

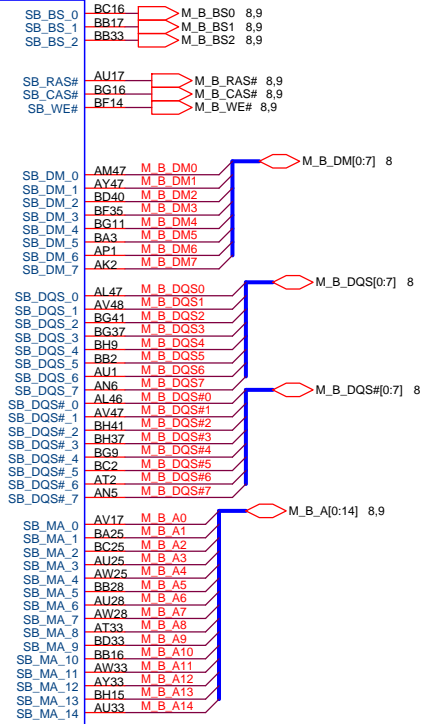


8 M_B_DQ[0:63]

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M B DQ1	AH46	SB_DQ_1
M B DQ2	AP47	SB_DQ_2
M B DQ3	AP46	SB_DQ_3
M B DQ4	AJ46	SB_DQ_4
M B DQ5	AJ48	SB_DQ_5
M B DQ6	AM48	SB_DQ_6
M B DQ7	AP48	SB_DQ_7
M B DQ8	AU47	SB_DQ_8
M B DQ9	AU46	SB_DQ_9
M B DQ10	BA48	SB_DQ_10
M B DQ11	AY48	SB_DQ_11
M B DQ12	AT47	SB_DQ_12
M B DQ13	AR47	SB_DQ_13
M B DQ14	BA47	SB_DQ_14
M B DQ15	BC47	SB_DQ_15
M B DQ16	BC46	SB_DQ_16
M B DQ17	BC44	SB_DQ_17
M B DQ18	BG43	SB_DQ_18
M B DQ19	BF43	SB_DQ_19
M B DQ20	BE45	SB_DQ_20
M B DQ21	BC41	SB_DQ_21
M B DQ22	BF40	SB_DQ_22
M B DQ23	BF41	SB_DQ_23
M B DQ24	BG38	SB_DQ_24
M B DQ25	BF38	SB_DQ_25
M B DQ26	BH35	SB_DQ_26
M B DQ27	BG35	SB_DQ_27
M B DQ28	BH40	SB_DQ_28
M B DQ29	BG39	SB_DQ_29
M B DQ30	BG34	SB_DQ_30
M B DQ31	BH34	SB_DQ_31
M B DQ32	BH14	SB_DQ_32
M B DQ33	BG12	SB_DQ_33
M B DQ34	BH11	SB_DQ_34
M B DQ35	BG8	SB_DQ_35
M B DQ36	BH12	SB_DQ_36
M B DQ37	BF11	SB_DQ_37
M B DQ38	BF8	SB_DQ_38
M B DQ39	BG7	SB_DQ_39
M B DQ40	BC5	SB_DQ_40
M B DQ41	BC6	SB_DQ_41
M B DQ42	AY3	SB_DQ_42
M B DQ43	AY1	SB_DQ_43
M B DQ44	BF6	SB_DQ_44
M B DQ45	BF5	SB_DQ_45
M B DQ46	BA1	SB_DQ_46
M B DQ47	BD3	SB_DQ_47
M B DQ48	AV2	SB_DQ_48
M B DQ49	AU3	SB_DQ_49
M B DQ50	AR3	SB_DQ_50
M B DQ51	AN2	SB_DQ_51
M B DQ52	AY2	SB_DQ_52
M B DQ53	AV1	SB_DQ_53
M B DQ54	AP3	SB_DQ_54
M B DQ55	AR1	SB_DQ_55
M B DQ56	AL1	SB_DQ_56
M B DQ57	AL2	SB_DQ_57
M B DQ58	AJ1	SB_DQ_58
M B DQ59	AH1	SB_DQ_59
M B DQ60	AM2	SB_DQ_60
M B DQ61	AM3	SB_DQ_61
M B DQ62	AH3	SB_DQ_62
M B DQ63	AJ3	SB_DQ_63

CANTIGA_CHIPSET

DDR SYSTEM MEMORY B



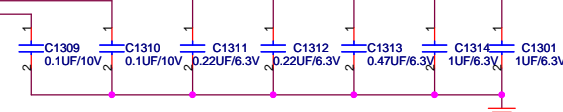
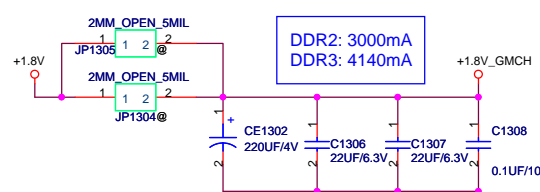
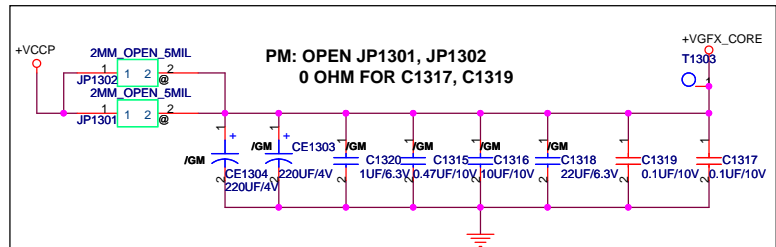
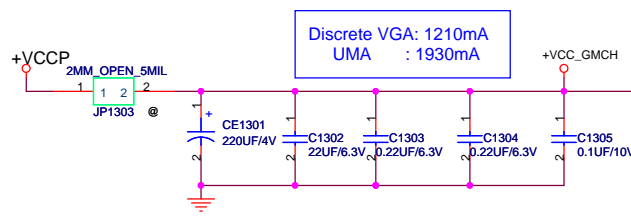
Pin	Label	Function
AP33	VCC_SM_1	
AN33	VCC_SM_2	
BH32	VCC_SM_3	
BG32	VCC_SM_4	
BF32	VCC_SM_5	
BD32	VCC_SM_6	
BC32	VCC_SM_7	
BB32	VCC_SM_8	
BA32	VCC_SM_9	
AY32	VCC_SM_10	
AW32	VCC_SM_11	
AV32	VCC_SM_12	
AU32	VCC_SM_13	
AT32	VCC_SM_14	
AR32	VCC_SM_15	
AP32	VCC_SM_16	
AN32	VCC_SM_17	
BH31	VCC_SM_18	
BG31	VCC_SM_19	
BF31	VCC_SM_20	
BG30	VCC_SM_21	
BH29	VCC_SM_22	
BG29	VCC_SM_23	
BF29	VCC_SM_24	
BC29	VCC_SM_25	
BB29	VCC_SM_26	
BA29	VCC_SM_27	
AY29	VCC_SM_28	
AW29	VCC_SM_29	
AV29	VCC_SM_30	
AU29	VCC_SM_31	
AT29	VCC_SM_32	
AR29	VCC_SM_33	
AP29	VCC_SM_34	
BA36	VCC_SM_36/NC	
BB36	VCC_SM_37/NC	
BD16	VCC_SM_38/NC	
BB21	VCC_SM_39/NC	
AW16	VCC_SM_40/NC	
AW13	VCC_SM_41/NC	
AT13	VCC_SM_42/NC	

Pin	Label	Function
Y26	VCC_AGX_1	
AE25	VCC_AGX_2	
AB25	VCC_AGX_3	
AA25	VCC_AGX_4	
AE24	VCC_AGX_5	
AC24	VCC_AGX_6	
AA24	VCC_AGX_7	
Y24	VCC_AGX_8	
AE23	VCC_AGX_9	
AC23	VCC_AGX_10	
AB23	VCC_AGX_11	
AA23	VCC_AGX_12	
AJ21	VCC_AGX_13	
AG21	VCC_AGX_14	
AE21	VCC_AGX_15	
AC21	VCC_AGX_16	
AA21	VCC_AGX_17	
Y21	VCC_AGX_18	
AH20	VCC_AGX_19	
AF20	VCC_AGX_20	
AE20	VCC_AGX_21	
AC20	VCC_AGX_22	
AB20	VCC_AGX_23	
AA20	VCC_AGX_24	
T17	VCC_AGX_25	
T16	VCC_AGX_26	
AM15	VCC_AGX_27	
AL15	VCC_AGX_28	
AE15	VCC_AGX_29	
AJ15	VCC_AGX_30	
AH15	VCC_AGX_31	
AG15	VCC_AGX_32	
AF15	VCC_AGX_33	
AB15	VCC_AGX_34	
AA15	VCC_AGX_35	
Y15	VCC_AGX_36	
V15	VCC_AGX_37	
U15	VCC_AGX_38	
AN14	VCC_AGX_39	
AM14	VCC_AGX_40	
U14	VCC_AGX_41	
T14	VCC_AGX_42	

Pin	Label	Function
VCC_AGX_SENSE	AJ14	
VSS_AGX_SENSE	AH14	

Pin	Label	Function
VCC_AGX_NCTF_1	W28	
VCC_AGX_NCTF_2	V28	
VCC_AGX_NCTF_3	V26	
VCC_AGX_NCTF_4	V26	
VCC_AGX_NCTF_5	V25	
VCC_AGX_NCTF_6	V24	
VCC_AGX_NCTF_7	V24	
VCC_AGX_NCTF_8	V23	
VCC_AGX_NCTF_9	V23	
VCC_AGX_NCTF_10	V23	
VCC_AGX_NCTF_11	AM21	
VCC_AGX_NCTF_12	AL21	
VCC_AGX_NCTF_13	AK21	
VCC_AGX_NCTF_14	W21	
VCC_AGX_NCTF_15	V21	
VCC_AGX_NCTF_16	U21	
VCC_AGX_NCTF_17	AM20	
VCC_AGX_NCTF_18	AK20	
VCC_AGX_NCTF_19	U20	
VCC_AGX_NCTF_20	AM19	
VCC_AGX_NCTF_21	AL19	
VCC_AGX_NCTF_22	AK19	
VCC_AGX_NCTF_23	AH19	
VCC_AGX_NCTF_24	AF19	
VCC_AGX_NCTF_25	AG19	
VCC_AGX_NCTF_26	AE19	
VCC_AGX_NCTF_27	AB19	
VCC_AGX_NCTF_28	AA19	
VCC_AGX_NCTF_29	X19	
VCC_AGX_NCTF_30	W19	
VCC_AGX_NCTF_31	V19	
VCC_AGX_NCTF_32	U19	
VCC_AGX_NCTF_33	AM17	
VCC_AGX_NCTF_34	AK17	
VCC_AGX_NCTF_35	AH17	
VCC_AGX_NCTF_36	AF17	
VCC_AGX_NCTF_37	AG17	
VCC_AGX_NCTF_38	AE17	
VCC_AGX_NCTF_39	AC17	
VCC_AGX_NCTF_40	AB17	
VCC_AGX_NCTF_41	Y17	
VCC_AGX_NCTF_42	W17	
VCC_AGX_NCTF_43	V17	
VCC_AGX_NCTF_44	U16	
VCC_AGX_NCTF_45	AM16	
VCC_AGX_NCTF_46	AL16	
VCC_AGX_NCTF_47	AK16	
VCC_AGX_NCTF_48	AJ16	
VCC_AGX_NCTF_49	AH16	
VCC_AGX_NCTF_50	AG16	
VCC_AGX_NCTF_51	AF16	
VCC_AGX_NCTF_52	AE16	
VCC_AGX_NCTF_53	AC16	
VCC_AGX_NCTF_54	AB16	
VCC_AGX_NCTF_55	AA16	
VCC_AGX_NCTF_56	V16	
VCC_AGX_NCTF_57	U16	
VCC_AGX_NCTF_58	U16	
VCC_AGX_NCTF_59	U16	
VCC_AGX_NCTF_60	U16	

Pin	Label	Function
VCC_SM_LF1	AV44	
VCC_SM_LF2	BA37	
VCC_SM_LF3	AM40	
VCC_SM_LF4	AV21	
VCC_SM_LF5	AY5	
VCC_SM_LF6	AM10	
VCC_SM_LF7	BB13	



Pin	Label	Function
AG34	VCC_1	
AC34	VCC_2	
AB34	VCC_3	
AA34	VCC_4	
Y34	VCC_5	
U34	VCC_6	
AM33	VCC_7	
AK33	VCC_8	
AJ33	VCC_10	
AG33	VCC_11	
AF33	VCC_12	
AE33	VCC_13	
AC33	VCC_14	
AA33	VCC_15	
Y33	VCC_16	
W33	VCC_17	
V33	VCC_18	
U33	VCC_19	
AH28	VCC_20	
AF28	VCC_21	
AC28	VCC_22	
AA28	VCC_23	
AJ26	VCC_24	
AG26	VCC_25	
AE26	VCC_26	
AC26	VCC_27	
AH25	VCC_28	
AG25	VCC_29	
AF25	VCC_30	
AG24	VCC_31	
AJ23	VCC_32	
AH23	VCC_33	
AF23	VCC_34	
T32	VCC_35	

Pin	Label	Function
VCC_NCTF_1	AM32	
VCC_NCTF_2	AL32	
VCC_NCTF_3	AK32	
VCC_NCTF_4	AJ32	
VCC_NCTF_5	AG32	
VCC_NCTF_6	AE32	
VCC_NCTF_7	AC32	
VCC_NCTF_8	AA32	
VCC_NCTF_9	V32	
VCC_NCTF_10	U32	
VCC_NCTF_11	U32	
VCC_NCTF_12	AM30	
VCC_NCTF_13	AL30	
VCC_NCTF_14	AK30	
VCC_NCTF_15	AH30	
VCC_NCTF_16	AG30	
VCC_NCTF_17	AE30	
VCC_NCTF_18	AC30	
VCC_NCTF_19	AA30	
VCC_NCTF_20	AB30	
VCC_NCTF_21	AA30	
VCC_NCTF_22	V30	
VCC_NCTF_23	V30	
VCC_NCTF_24	V30	
VCC_NCTF_25	U30	
VCC_NCTF_26	AL29	
VCC_NCTF_27	AK29	
VCC_NCTF_28	AJ29	
VCC_NCTF_29	AJ29	
VCC_NCTF_30	AG29	
VCC_NCTF_31	AE29	
VCC_NCTF_32	AC29	
VCC_NCTF_33	AA29	
VCC_NCTF_34	AA29	
VCC_NCTF_35	Y29	
VCC_NCTF_36	V29	
VCC_NCTF_37	U29	
VCC_NCTF_38	AL28	
VCC_NCTF_39	AK28	
VCC_NCTF_40	AL26	
VCC_NCTF_41	AK26	
VCC_NCTF_42	AK25	
VCC_NCTF_43	AK24	
VCC_NCTF_44	AK23	

Route VCC_AGX_SENSE and VSS_AGX_SENSE differentially.

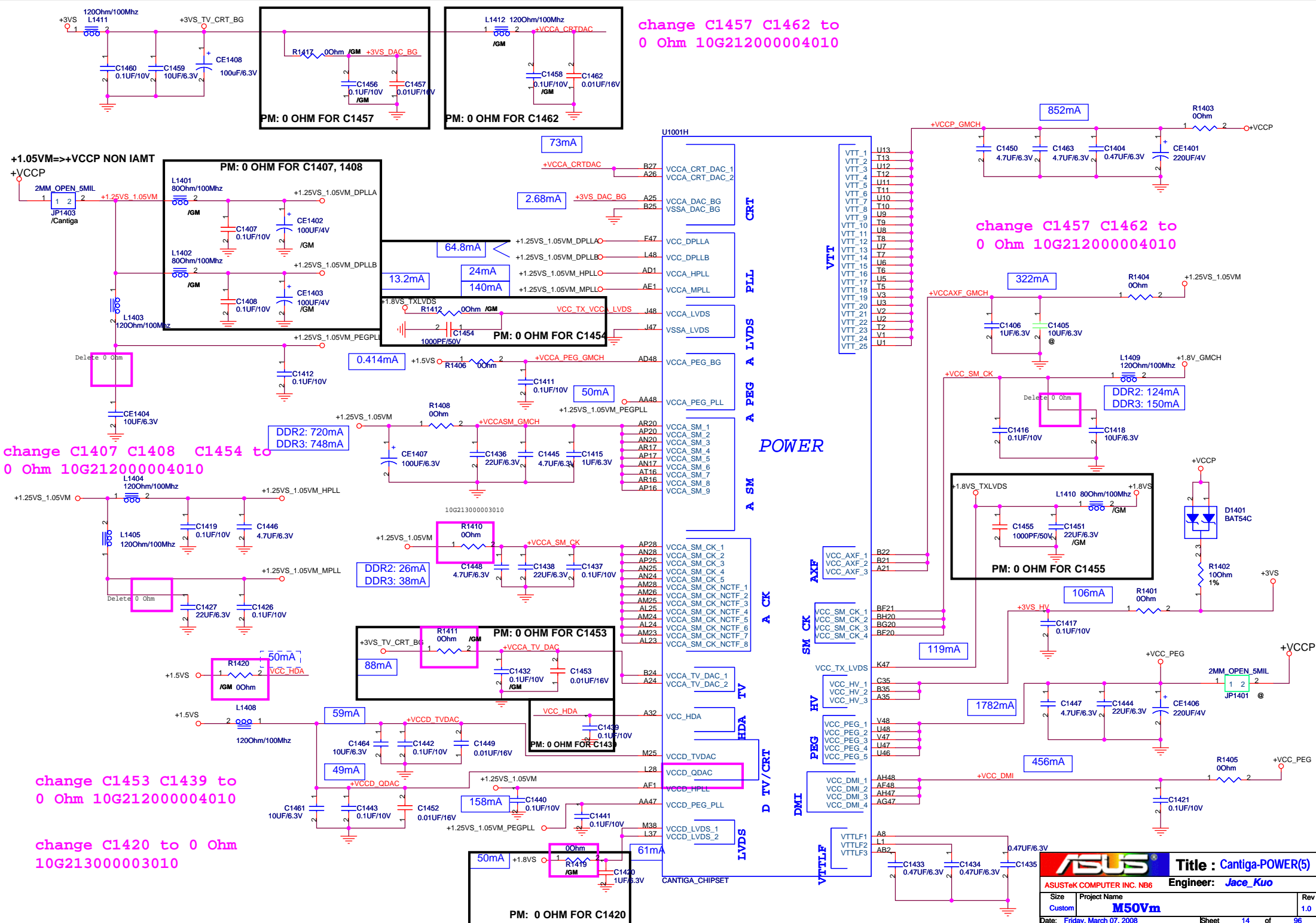
change C1457 C1462 to 0 Ohm 10G212000004010

change C1457 C1462 to 0 Ohm 10G212000004010

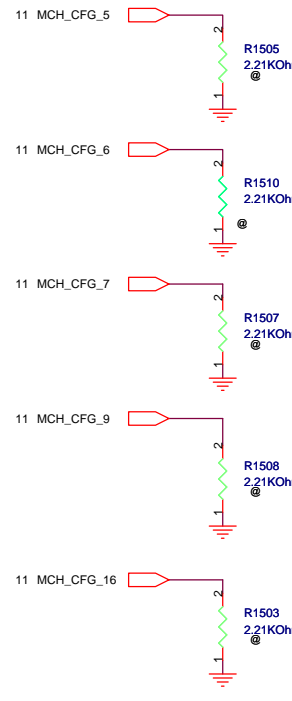
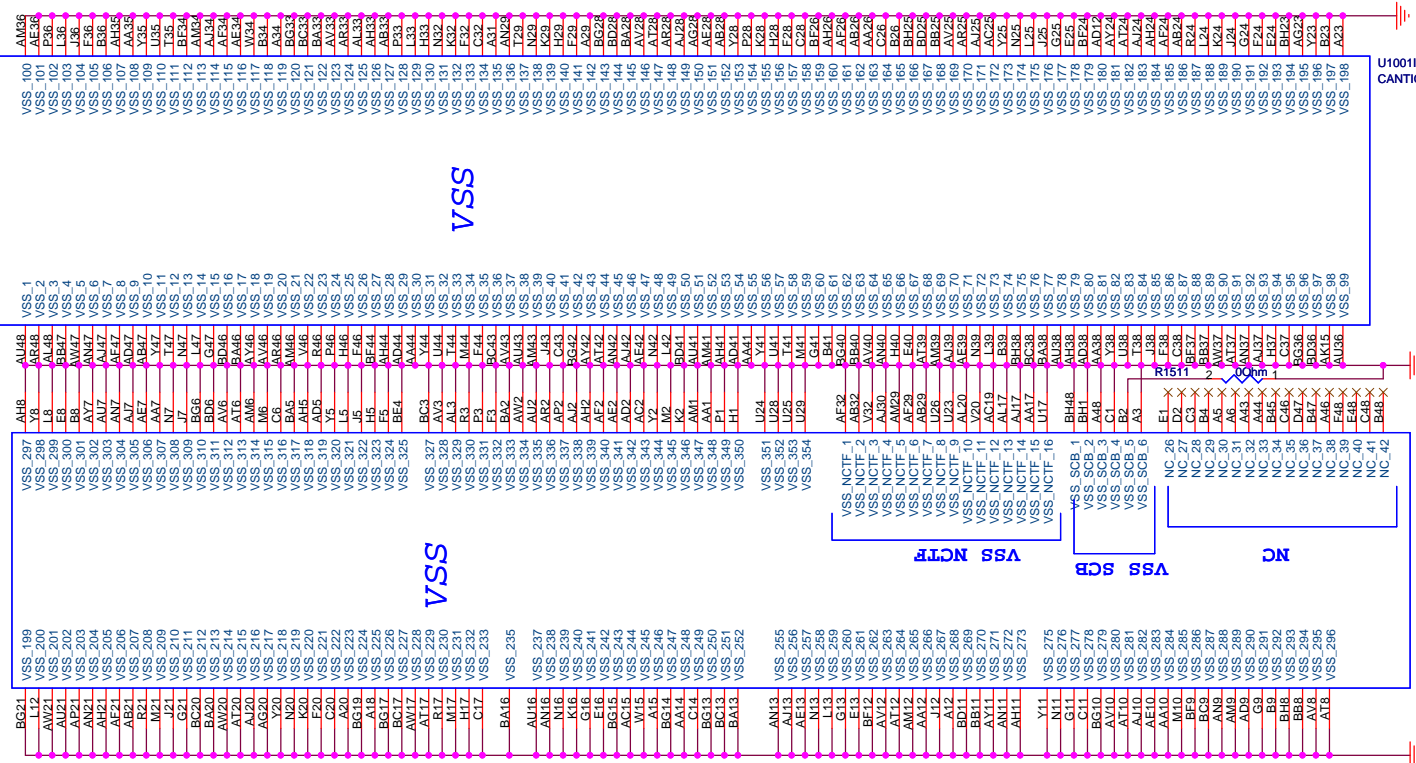
change C1407 C1408 C1454 to 0 Ohm 10G212000004010

change C1453 C1439 to 0 Ohm 10G212000004010

change C1420 to 0 Ohm 10G213000003010



ASUS		Title : Cantiga-POWER(5)	
ASUSTek COMPUTER INC. N66		Engineer: Jace_Kuo	
Size	Project Name	Rev	
Custom	M50Vm	1.0	
Date: Friday, March 07, 2008	Sheet 14 of 96		



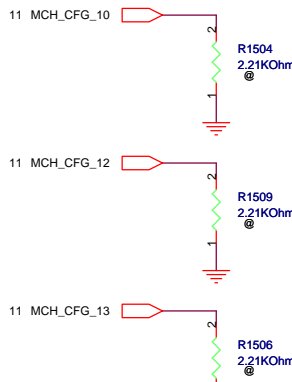
CFG5 : DMI STRAP
HIGH = DMI X 4 (Default)
LOW = DMI X 2

CFG6 : Integrated TPM Host Interface
HIGH = iTPM disable (Default)
LOW = iTPM enable

CFG7 : Intel ME Crypto Strap Transport Layer Security cipher suite
HIGH = With confidentiality (Default)
LOW = Without confidentiality

CFG9 : PCIE GRAPHIC LANE
HIGH = Normal Operation (Default)
LOW = Reverse Lanes

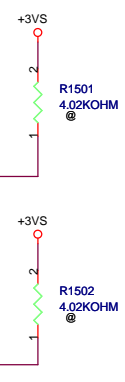
CFG16 : FSB Dynamic ODT
HIGH = Enable (Default)
LOW = Disable



CFG10 : PCIe Loopback
HIGH = Disable (Default)
LOW = Enable

CFG [13:12] : XOR/ALL-Z
00 = Reserved
01 = XOR Mode Enabled
10 = All-Z Mode Enabled
11 = Normal Operation (Default)

CFG19 : DMI Lane Reversal
LOW = NORMAL (default)
HIGH = Reverse Lanes



CFG20 : SDVO/PCIE CONCURRENT MODE
LOW = ONLY SDVO or PCIE is Operational (Default)
HIGH = SDVO and PCIE are operating simultaneously via the PEG port

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Title :

Engineer:

Size	Project Name	Rev
A		1.0
Date: Wednesday, February 13, 2008		Sheet 16 of 96

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Title :

Engineer:

Size	Project Name	Rev
A		1.0

Date: Wednesday, February 13, 2008 Sheet 17 of 96

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Title :

Engineer:

Size	Project Name	Rev
A		1.0

Date: Wednesday, February 13, 2008 Sheet 18 of 96

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		Title :	
Engineer:			
Size	Project Name		Rev
A			1.0
Date: Wednesday, February 13, 2008		Sheet	19 of 96

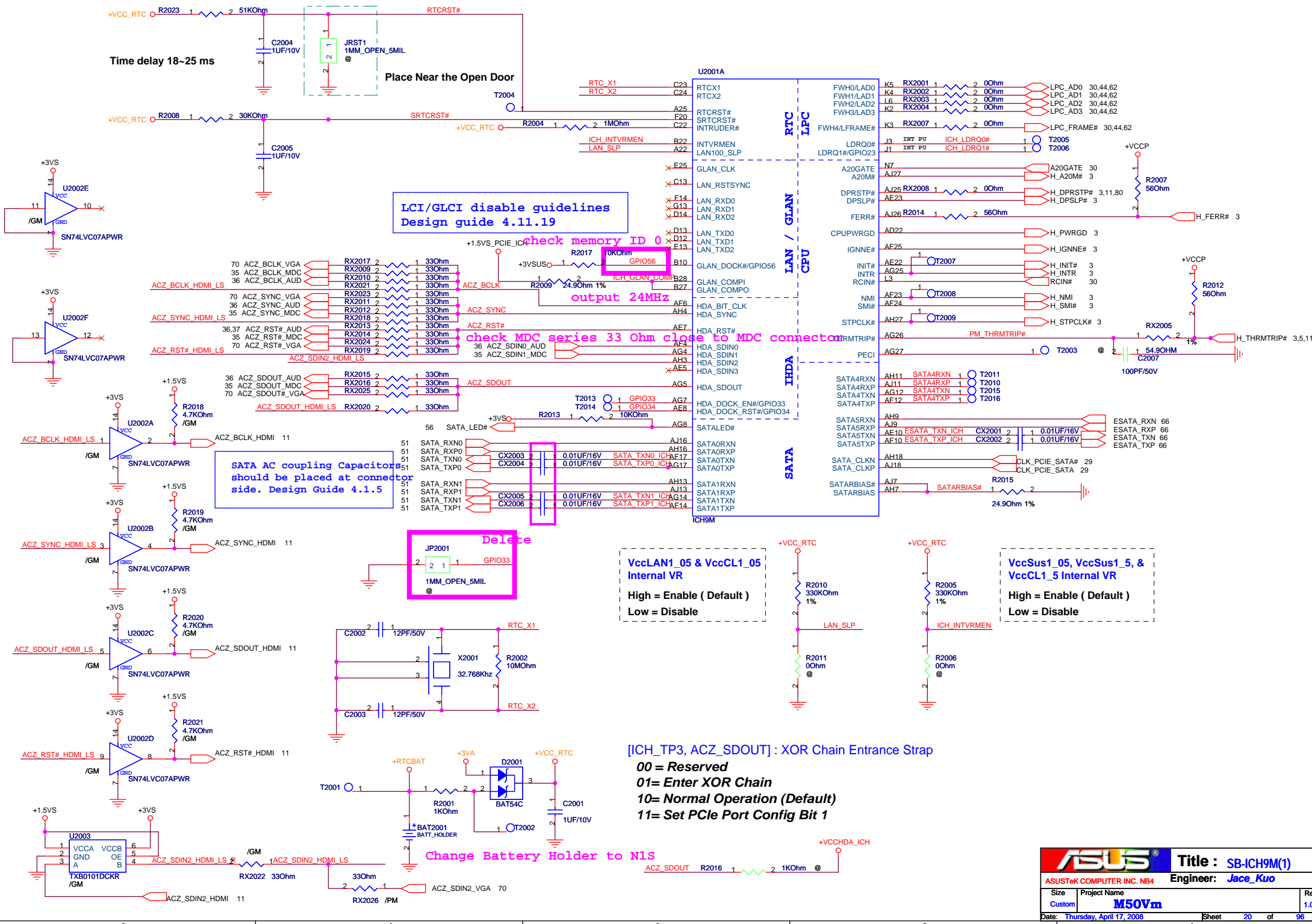
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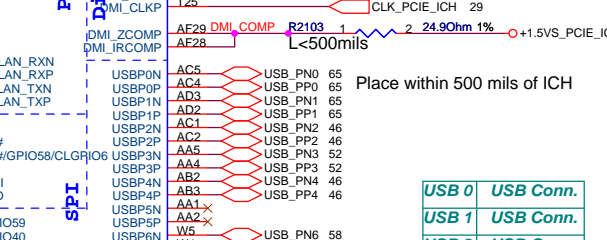
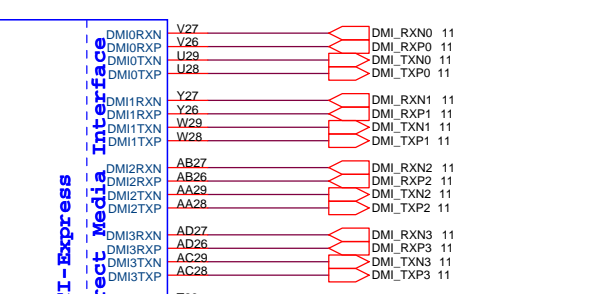
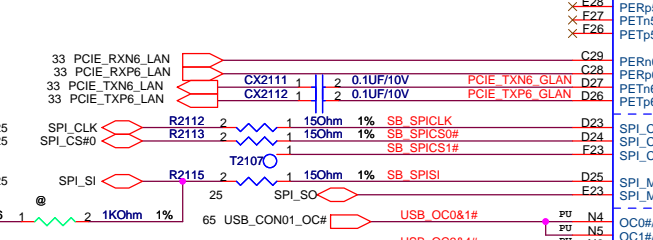
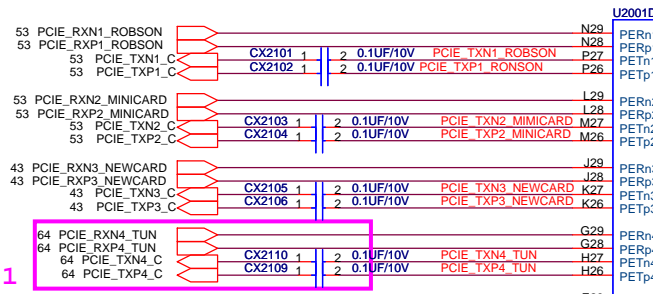
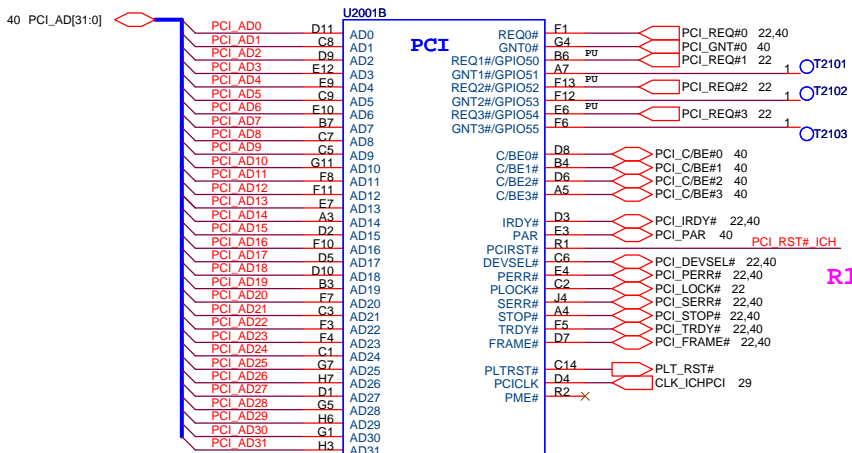
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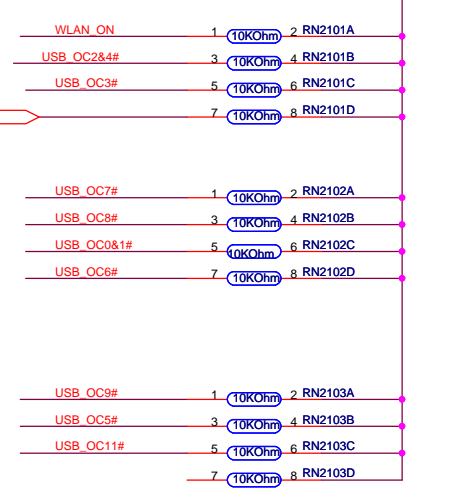
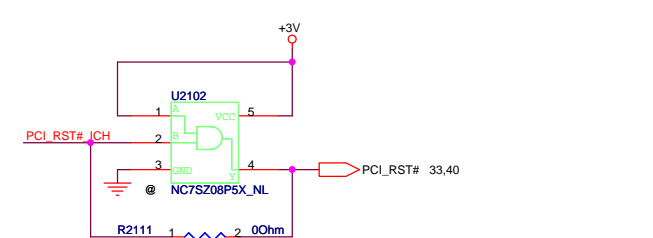
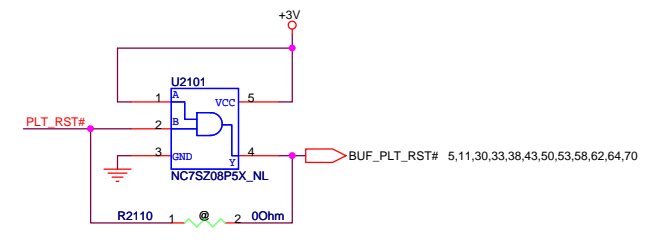
2

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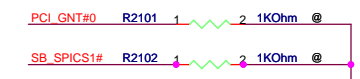
USB 0	USB Conn.
USB 1	USB Conn.
USB 2	USB Conn.
USB 3	USB Conn.
USB 4	Camera
USB 5	
USB 6	UWB
USB 7	WiMAX
USB 8	NewCard
USB 9	TV Tuner
USB 10	Bluetooth
USB 11	Fingerprint

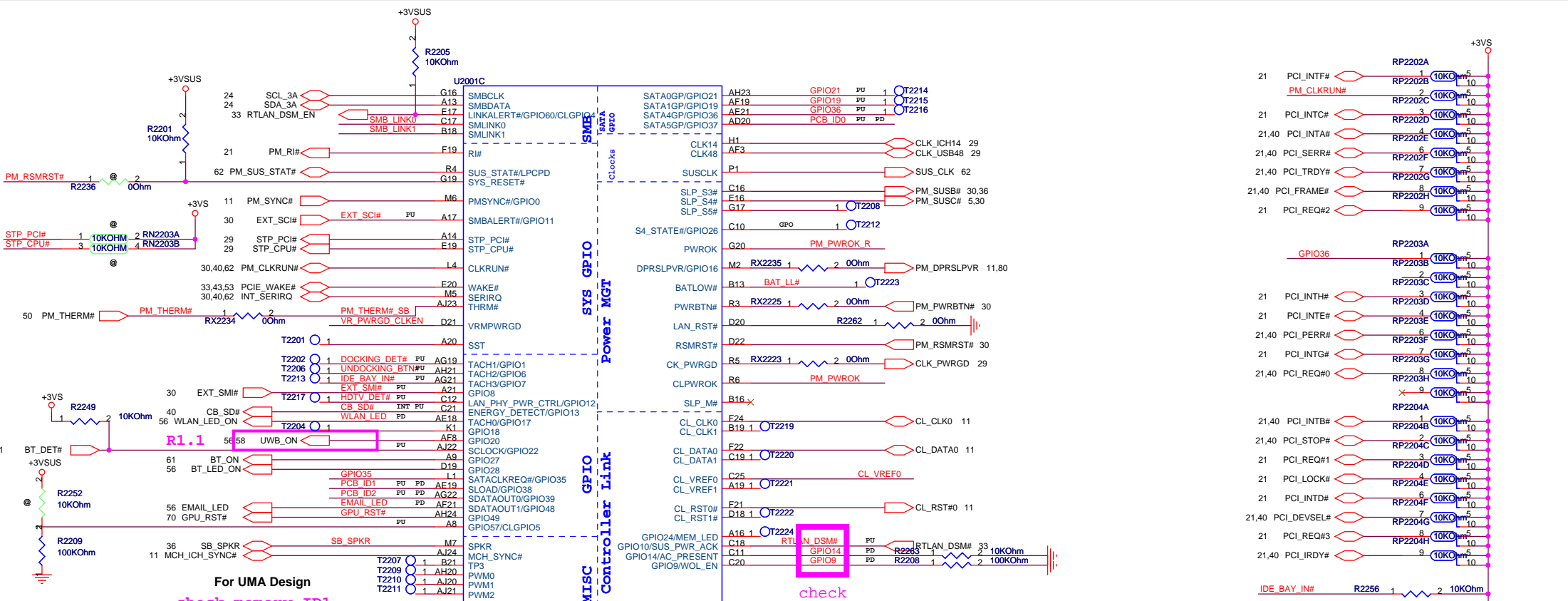


ICH9 Boot BIOS select

	GNT#0	CS#1
LPC	11	1 1
PCI	10	1 0
SPI	01	0 1

(default)

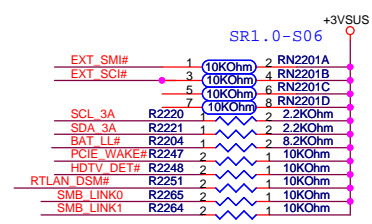




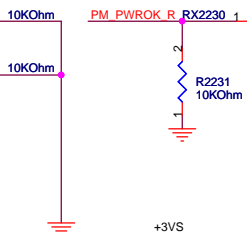
For UMA Design
check memory ID1

check

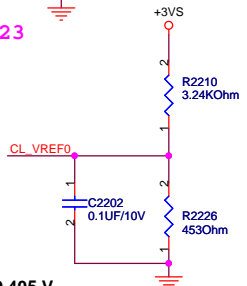
Mount/unmount as same R2236



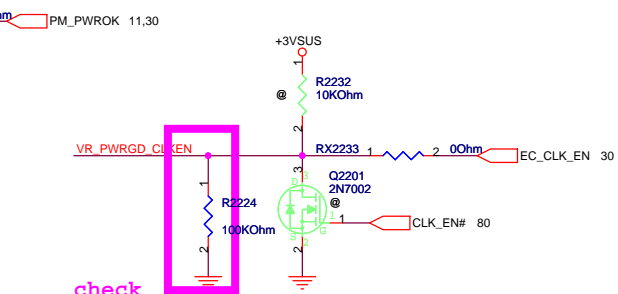
CB_SD# (GPIO13) 10K pull-up check CRB P.23



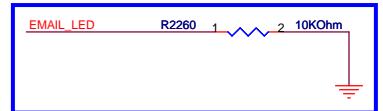
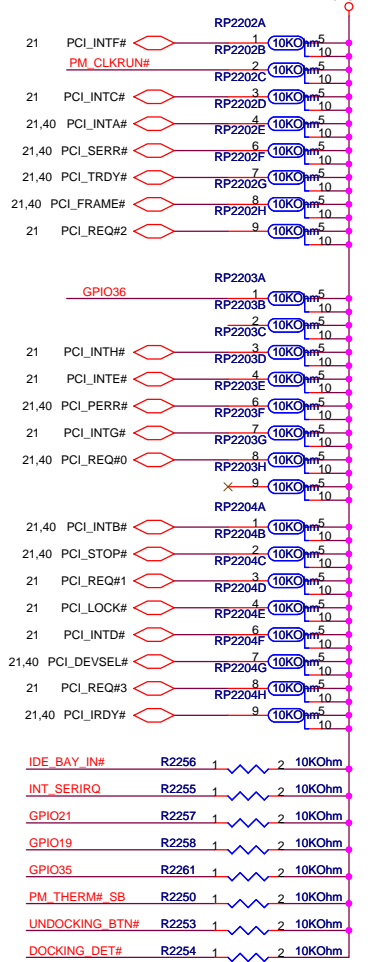
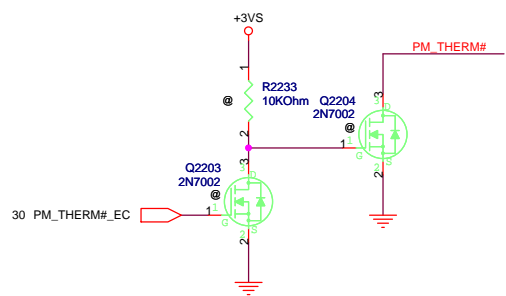
check

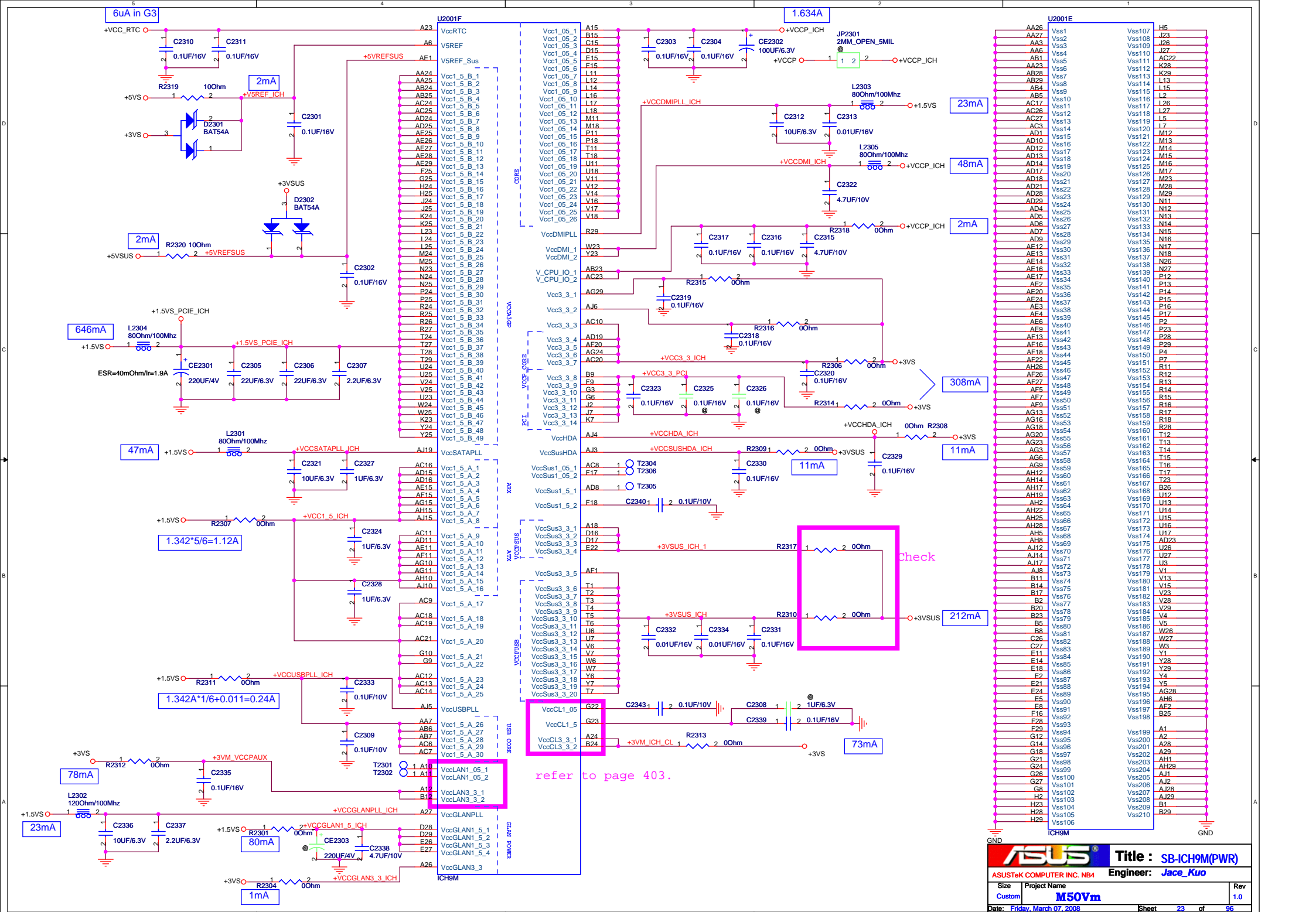


CL_VREF0/1 ~ 0.405 V
CL_VREF [0:1] routing rules
Width = 12 mils min
Spacing = 12 mils min
Break-out: 5 mils on 5 mils for 300 mils max



check





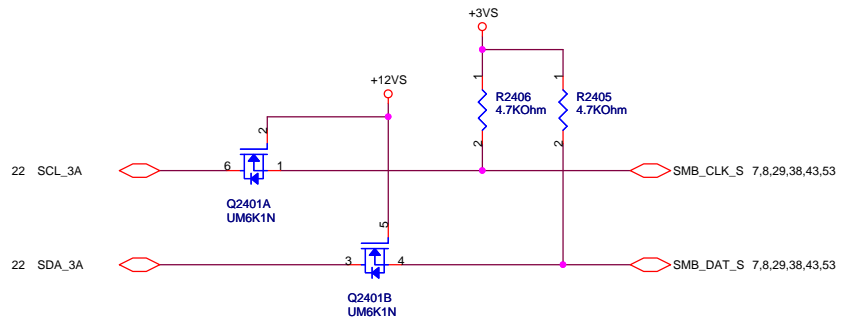
U2001F

A23	VccRTC
A6	V5REF
A6	V5REF_Sus
AA24	Vcc1_5_B_1
AA25	Vcc1_5_B_2
AB24	Vcc1_5_B_3
AB25	Vcc1_5_B_4
AC24	Vcc1_5_B_5
AD24	Vcc1_5_B_6
AD25	Vcc1_5_B_7
AE25	Vcc1_5_B_8
AE26	Vcc1_5_B_9
AE27	Vcc1_5_B_10
AE28	Vcc1_5_B_11
AE29	Vcc1_5_B_12
F25	Vcc1_5_B_14
G25	Vcc1_5_B_15
H24	Vcc1_5_B_16
H25	Vcc1_5_B_17
H26	Vcc1_5_B_18
J25	Vcc1_5_B_19
K24	Vcc1_5_B_20
K25	Vcc1_5_B_21
L24	Vcc1_5_B_22
L25	Vcc1_5_B_23
M24	Vcc1_5_B_24
M25	Vcc1_5_B_26
N23	Vcc1_5_B_27
N24	Vcc1_5_B_28
N25	Vcc1_5_B_29
P24	Vcc1_5_B_30
P25	Vcc1_5_B_31
R24	Vcc1_5_B_32
R25	Vcc1_5_B_33
R26	Vcc1_5_B_34
R27	Vcc1_5_B_35
T24	Vcc1_5_B_36
T27	Vcc1_5_B_37
T28	Vcc1_5_B_38
T29	Vcc1_5_B_39
U24	Vcc1_5_B_40
U25	Vcc1_5_B_41
Y24	Vcc1_5_B_42
Y25	Vcc1_5_B_43
Y26	Vcc1_5_B_44
W24	Vcc1_5_B_45
W25	Vcc1_5_B_46
K23	Vcc1_5_B_47
Y24	Vcc1_5_B_48
Y25	Vcc1_5_B_49
A19	VccSATAPLL
AC16	Vcc1_5_A_1
AD15	Vcc1_5_A_2
AD16	Vcc1_5_A_3
AE15	Vcc1_5_A_4
AF15	Vcc1_5_A_5
AG15	Vcc1_5_A_6
AH15	Vcc1_5_A_7
AJ15	Vcc1_5_A_8
AC11	Vcc1_5_A_9
AD11	Vcc1_5_A_10
AE11	Vcc1_5_A_11
AG10	Vcc1_5_A_12
AG11	Vcc1_5_A_13
AH10	Vcc1_5_A_14
AJ10	Vcc1_5_A_15
AC9	Vcc1_5_A_16
AC18	Vcc1_5_A_17
AC19	Vcc1_5_A_18
AC21	Vcc1_5_A_19
G10	Vcc1_5_A_20
G9	Vcc1_5_A_21
AC12	Vcc1_5_A_23
AC13	Vcc1_5_A_24
AC14	Vcc1_5_A_25
AJ5	VccUSBPLL
AA7	Vcc1_5_A_26
AB6	Vcc1_5_A_27
AB7	Vcc1_5_A_28
AC6	Vcc1_5_A_29
AC7	Vcc1_5_A_30
A10	VccLAN1_05_1
A11	VccLAN1_05_2
A12	VccLAN3_3_1
B12	VccLAN3_3_2
A27	VccGLANPLL
D28	VccGLAN1_5_1
D29	VccGLAN1_5_2
E26	VccGLAN1_5_3
E27	VccGLAN1_5_4
A26	VccGLAN3_3

U2001E

AA26	Vss1
AA27	Vss2
AA3	Vss3
AA6	Vss4
AB1	Vss5
AA23	Vss6
AB28	Vss7
AB4	Vss8
AB5	Vss9
AC17	Vss10
AC26	Vss11
AC27	Vss12
AD1	Vss13
AD10	Vss14
AD12	Vss15
AD13	Vss16
AD14	Vss17
AD17	Vss18
AD18	Vss19
AD21	Vss20
AD28	Vss21
AD29	Vss22
AD4	Vss23
AD5	Vss24
AD6	Vss25
AD7	Vss26
AD9	Vss27
AE12	Vss28
AE13	Vss29
AE14	Vss30
AE16	Vss31
AE17	Vss32
AE18	Vss33
AE2	Vss34
AE22	Vss35
AE24	Vss36
AE3	Vss37
AE6	Vss38
AE9	Vss39
AF13	Vss40
AF16	Vss41
AF18	Vss42
AF22	Vss43
AH26	Vss44
AE26	Vss45
AE27	Vss46
AE5	Vss47
AE7	Vss48
AE8	Vss49
AE9	Vss50
AG13	Vss51
AG16	Vss52
AG18	Vss53
AG20	Vss54
AG23	Vss55
AG6	Vss56
AG9	Vss57
AH12	Vss58
AH14	Vss59
AH17	Vss60
AH19	Vss61
AH2	Vss62
AH22	Vss63
AH25	Vss64
AH28	Vss65
AH5	Vss66
AH8	Vss67
AH12	Vss68
AJ14	Vss69
AJ7	Vss70
AJ8	Vss71
B11	Vss72
B14	Vss73
B2	Vss74
B20	Vss75
B23	Vss76
B5	Vss77
B8	Vss78
C26	Vss79
C27	Vss80
E11	Vss81
E14	Vss82
E18	Vss83
E2	Vss84
E21	Vss85
E24	Vss86
E5	Vss87
E8	Vss88
F16	Vss89
F28	Vss90
F29	Vss91
G12	Vss92
G14	Vss93
G18	Vss94
G21	Vss95
G24	Vss96
G26	Vss97
G27	Vss98
G8	Vss99
H2	Vss100
H23	Vss101
H28	Vss102
H29	Vss103
H29	Vss104
H29	Vss105
H29	Vss106
H5	Vss107
J23	Vss108
J26	Vss109
J27	Vss110
AC22	Vss111
K28	Vss112
K29	Vss113
L13	Vss114
L15	Vss115
L2	Vss116
L26	Vss117
L27	Vss118
L5	Vss119
L7	Vss120
M12	Vss121
M13	Vss122
M14	Vss123
M15	Vss124
M16	Vss125
M17	Vss126
M23	Vss127
M28	Vss128
M29	Vss129
N11	Vss130
N12	Vss131
N13	Vss132
N14	Vss133
N15	Vss134
N16	Vss135
N17	Vss136
N18	Vss137
N18	Vss138
N26	Vss139
P12	Vss140
P13	Vss141
P14	Vss142
P15	Vss143
P16	Vss144
P2	Vss145
P23	Vss146
P28	Vss147
P29	Vss148
P4	Vss149
P7	Vss150
R11	Vss151
R17	Vss152
R12	Vss153
R13	Vss154
R14	Vss155
R15	Vss156
R16	Vss157
R17	Vss158
R18	Vss159
T12	Vss160
T13	Vss161
T14	Vss162
T15	Vss163
T16	Vss164
T17	Vss165
T23	Vss166
T26	Vss167
U2	Vss168
U12	Vss169
U13	Vss170
U14	Vss171
U15	Vss172
U16	Vss173
U17	Vss174
U27	Vss175
U3	Vss176
U3	Vss177
V1	Vss178
V1	Vss179
V13	Vss180
V15	Vss181
V23	Vss182
V28	Vss183
V29	Vss184
V4	Vss185
V5	Vss186
W26	Vss187
W27	Vss188
W3	Vss189
Y1	Vss190
Y28	Vss191
Y29	Vss192
Y4	Vss193
Y5	Vss194
AG28	Vss195
AH6	Vss196
AF2	Vss197
B25	Vss198
A1	Vss199
A2	Vss200
A28	Vss201
A29	Vss202
AH1	Vss203
AH29	Vss204
AJ1	Vss205
AJ2	Vss206
AJ28	Vss207
AJ29	Vss208
B1	Vss209
B29	Vss210

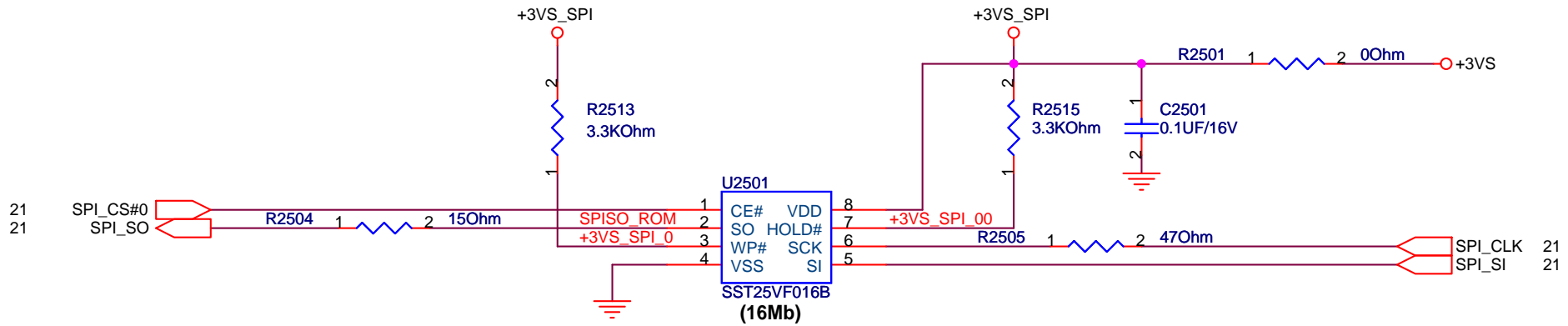
ICH9-M



- 7 SO-DIMM0
- 8 SO-DIMM1
- 29 CLK-GEN
- 39 AUD-DSP
- 43 NEWCARD
- 53 WLAN

EC-IT8752

Master	Slave
SCL_3A SDA_3A (ICH9M)	A. SMB_CLK_S → SO-DIMM0; SO-DIMM1; SMB_DAT_S → Debug; WLAN Card B. SMB_CLK_M → CLK Generator SMB_DAT_M
SMB0_CLK SMB0_DAT (EC)	BATTERY
SMB1_CLK SMB1_DAT (EC)	Thermal Sensor



FOR iTPM

		Title : SPI ROM	
ASUSTeK COMPUTER INC. NB4		Engineer: Jace_Kuo	
Size A	Project Name M50Vm	Rev 1.0	
Date: Friday, March 07, 2008		Sheet 25 of 96	

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Title :

Engineer:

Size	Project Name	Rev
A		1.0
Date: Wednesday, February 13, 2008		Sheet 26 of 96

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Title :

ASUSTeK COMPUTER INC. NB6

Engineer: *Raphael_Chen*

Size	Project Name	Rev
A	M50Vm	1.0

Date: *Wednesday, February 13, 2008*

Sheet *27* of *96*

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Title :

ASUSTeK COMPUTER INC. NB6

Engineer: *Raphael_Chen*

Size	Project Name	Rev
A	M50Vm	1.0

Date: *Wednesday, February 13, 2008*

Sheet *28* of *96*

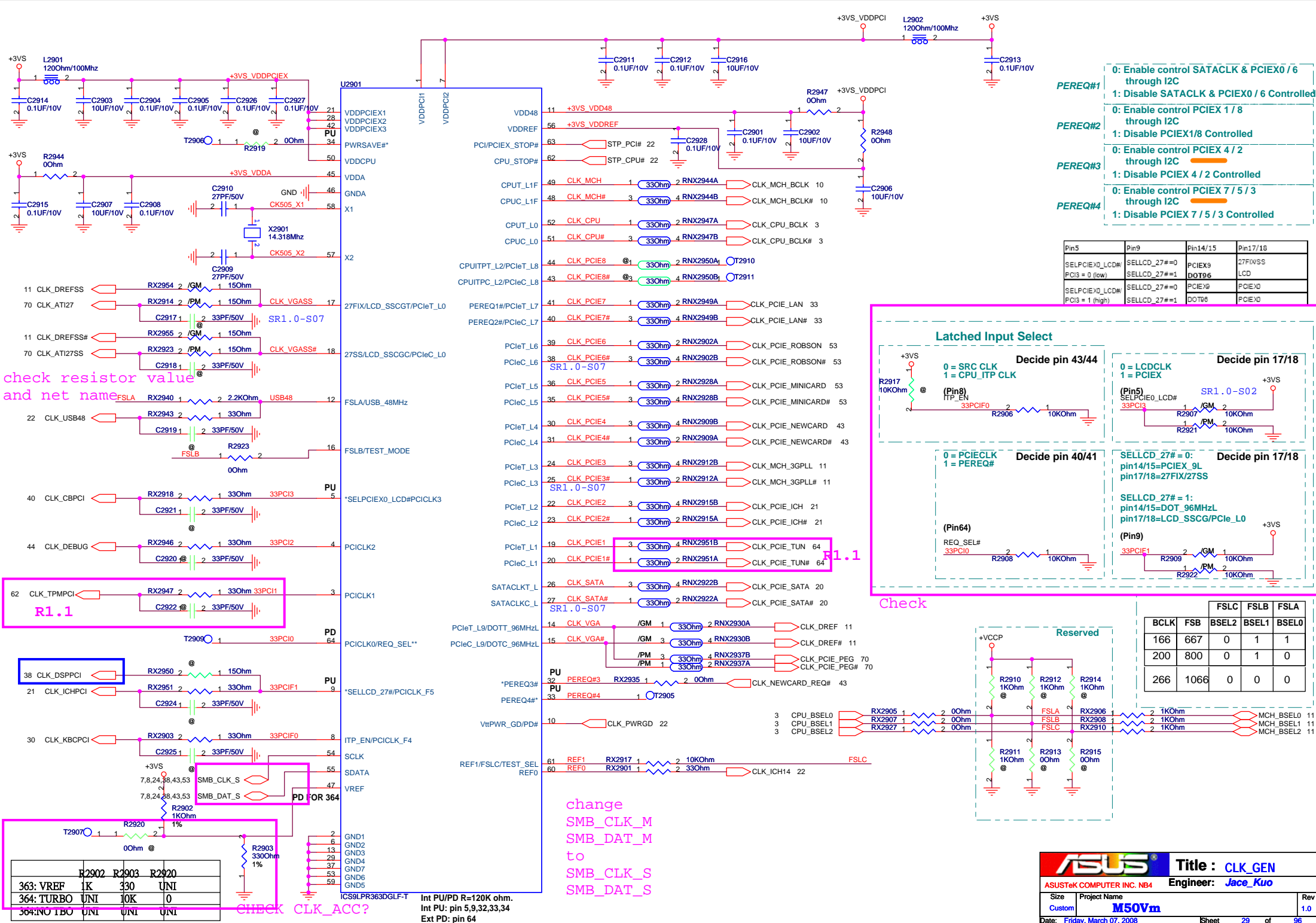
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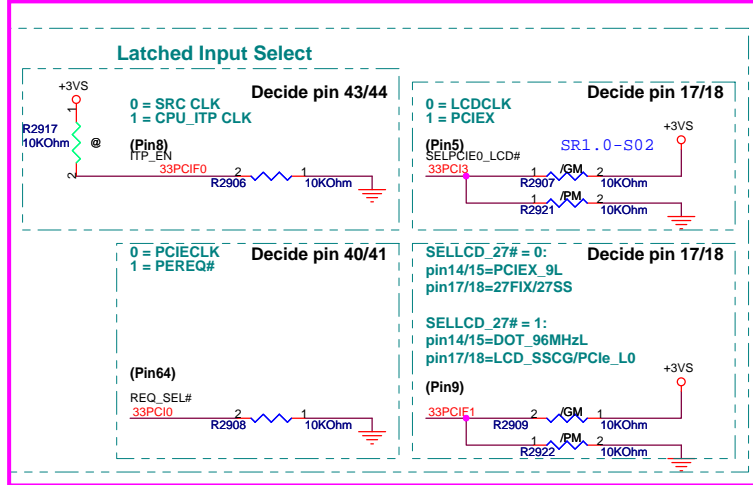
2

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- PEREQ#1:
 - 0: Enable control SATACLK & PCIEX0 / 6 through I2C
 - 1: Disable SATACLK & PCIEX0 / 6 Controlled
- PEREQ#2:
 - 0: Enable control PCIE1 / 8 through I2C
 - 1: Disable PCIE1/8 Controlled
- PEREQ#3:
 - 0: Enable control PCIE4 / 2 through I2C
 - 1: Disable PCIE4 / 2 Controlled
- PEREQ#4:
 - 0: Enable control PCIE7 / 5 / 3 through I2C
 - 1: Disable PCIE7 / 5 / 3 Controlled

Pin5	Pin9	Pin14/15	Pin17/18
SELPCIE_X_LCD# FCI3 = 0 (low)	SELLCD_27# = 0 SELLCD_27# = 1 DOT96	PCIE_X9 DOT96	27FIWSS LCD
SELPCIE_X_LCD# FCI3 = 1 (high)	SELLCD_27# = 0 SELLCD_27# = 1 DOT96	PCIE_X9 DOT96	PCIE_X0 PCIE_X0



check resistor value and net name

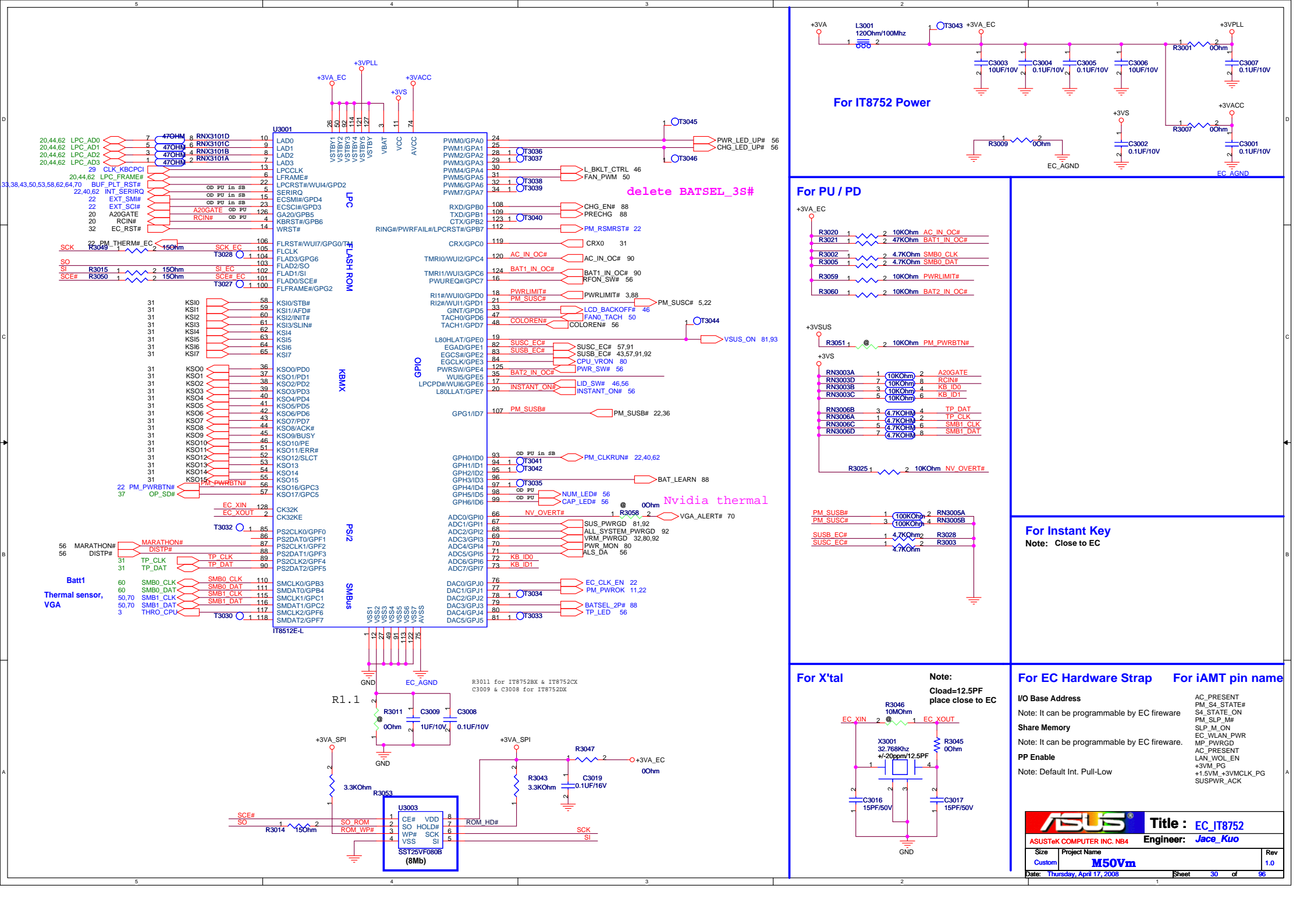
R1.1

change SMB_CLK_M
SMB_DAT_M to
SMB_CLK_S
SMB_DAT_S

CHECK CLK_ACC?

	R2902	R2903	R2920
363: VREF	1K	330	UNI
364: TURBO UNI	10K	0	
364: NO TBO UNI	UNI	UNI	UNI

Int PU/PD R=120K ohm.
Int PU: pin 5,9,32,33,34
Ext PD: pin 64



For IT8752 Power

For PU / PD

For Instant Key
Note: Close to EC

For X'tal

Note:
Load=12.5PF
place close to EC

For EC Hardware Strap For iAMT pin name

I/O Base Address
Note: It can be programmable by EC firmware
Share Memory
Note: It can be programmable by EC firmware.
PP Enable
Note: Default Int. Pull-Low

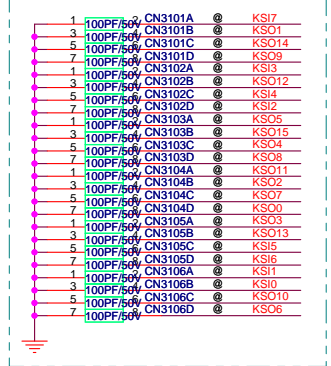
AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
SUSPWR_ACK

ASUS Title : **EC_I78752**
ASUSTeK COMPUTER INC. NB4 Engineer: **Jace_Kuo**

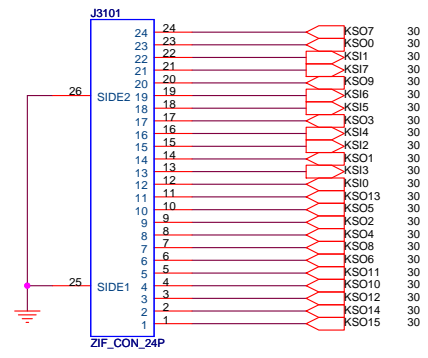
Size	Project Name	Rev
Custom	M50Vm	1.0

Date: Thursday, April 17, 2008 Sheet 30 of 96

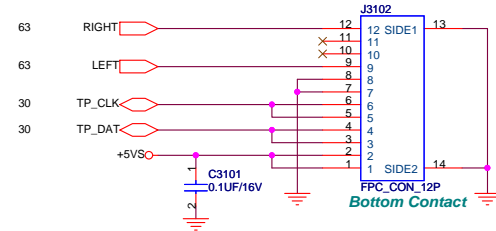
EMI



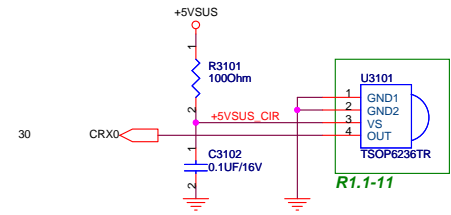
Keyboard

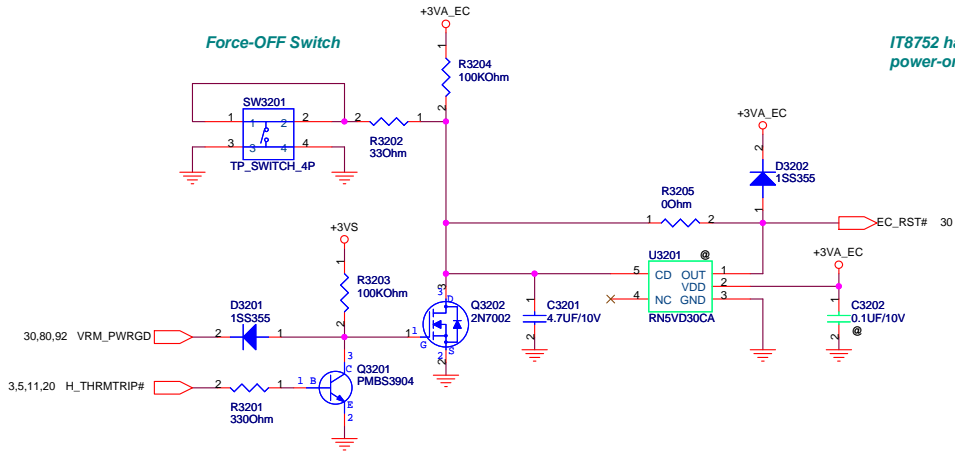


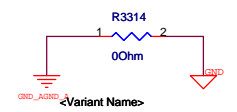
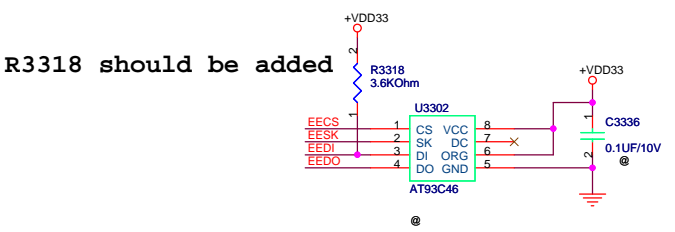
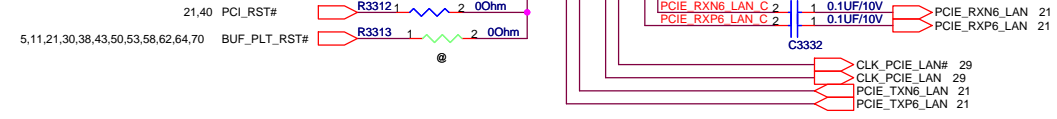
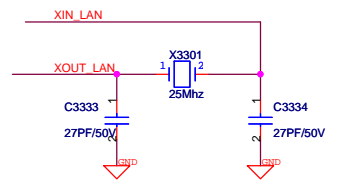
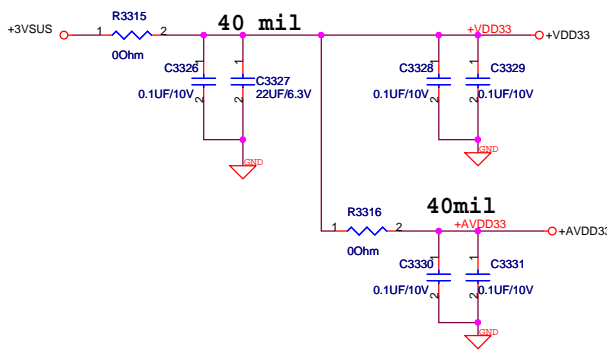
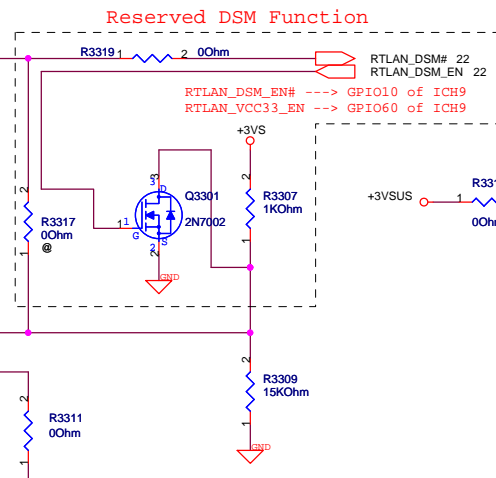
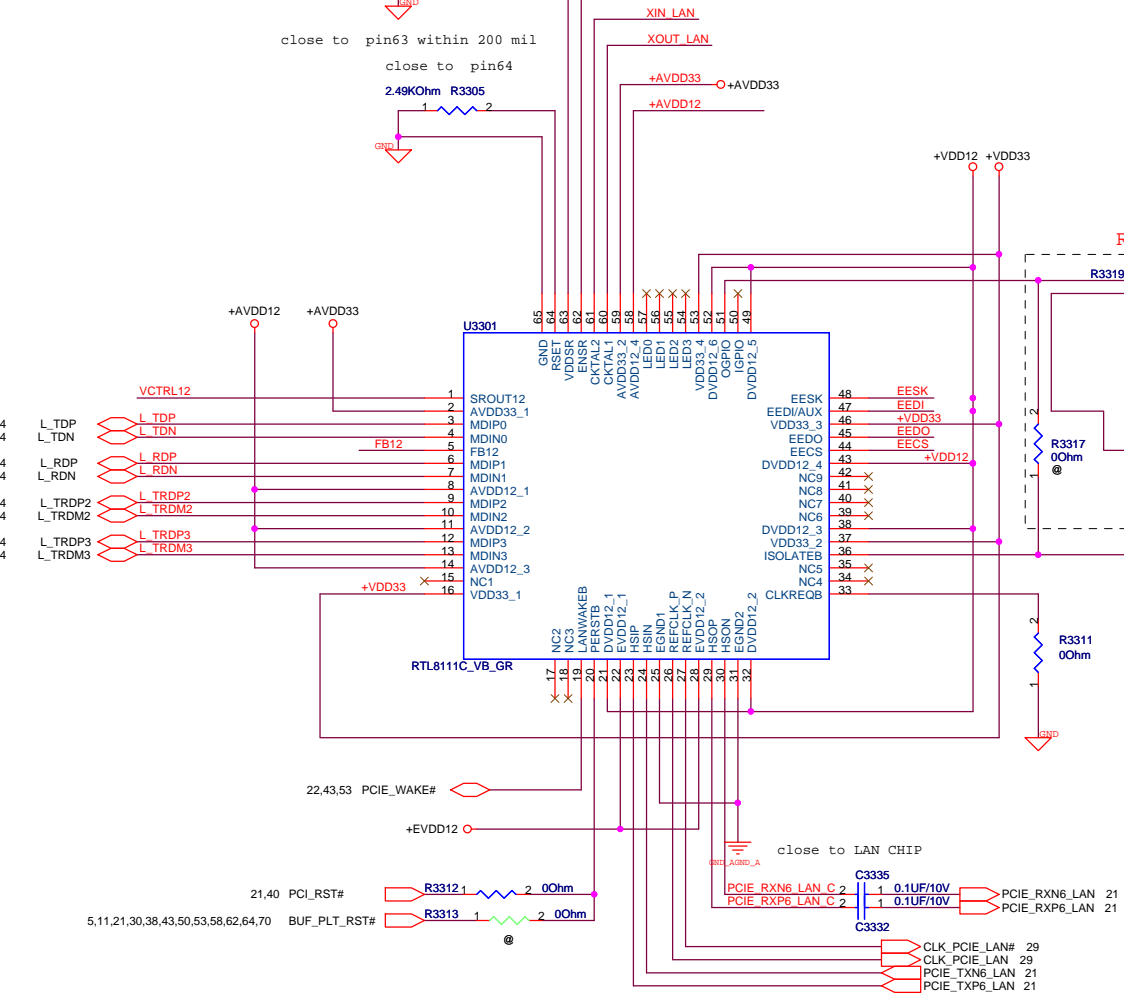
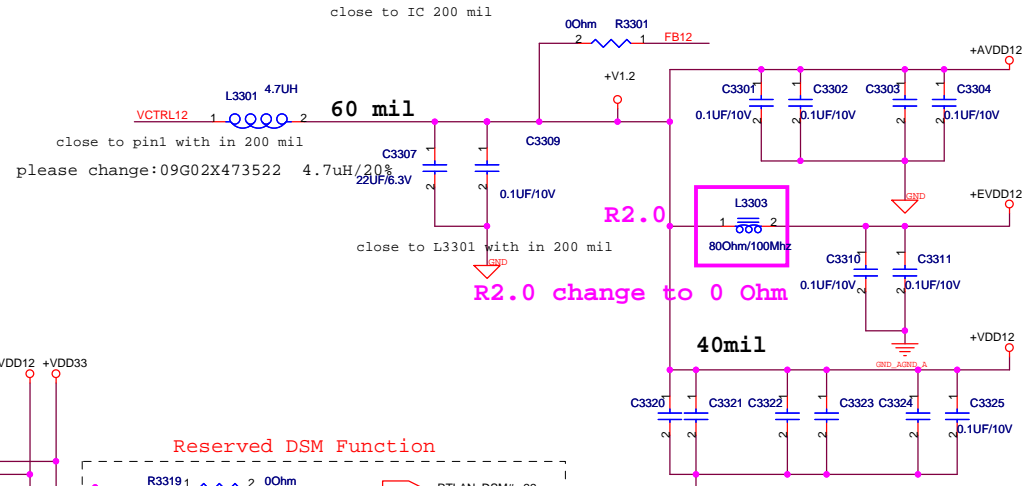
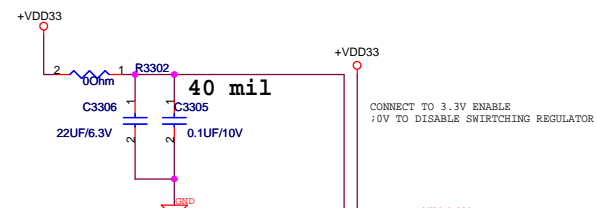
Touchpad



CIR

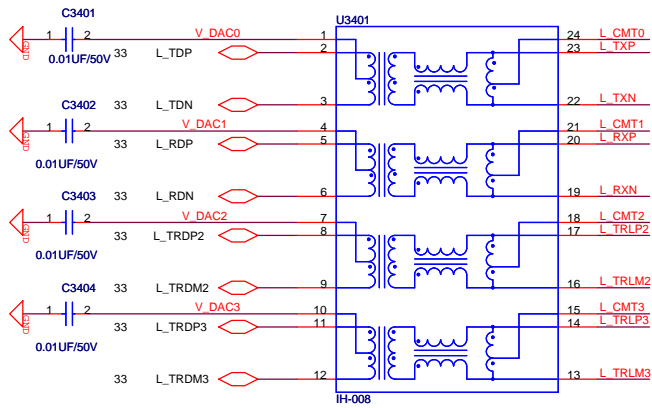
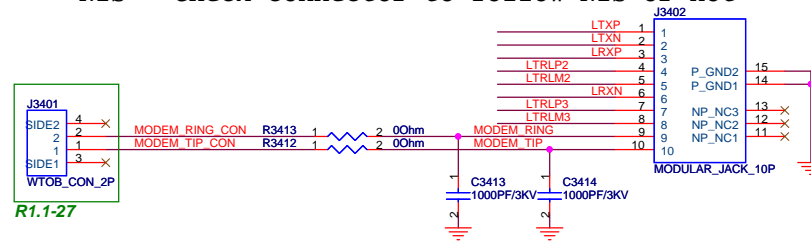




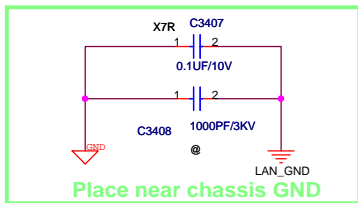
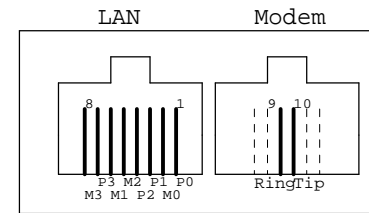
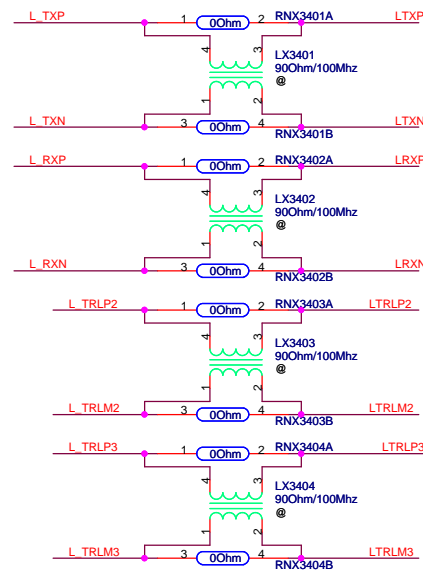
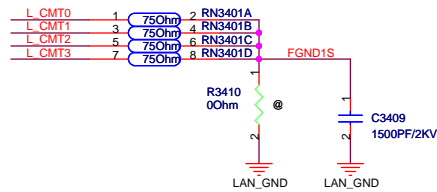


ASUS Title : REALTEK 8111C
 ASUSTeK COMPUTER INC Engineer:
 Size Project Name Rev
 Custom Date: Wednesday, April 23, 2008 Sheet 33 of 96

N1S Check connector to follow N1S or not



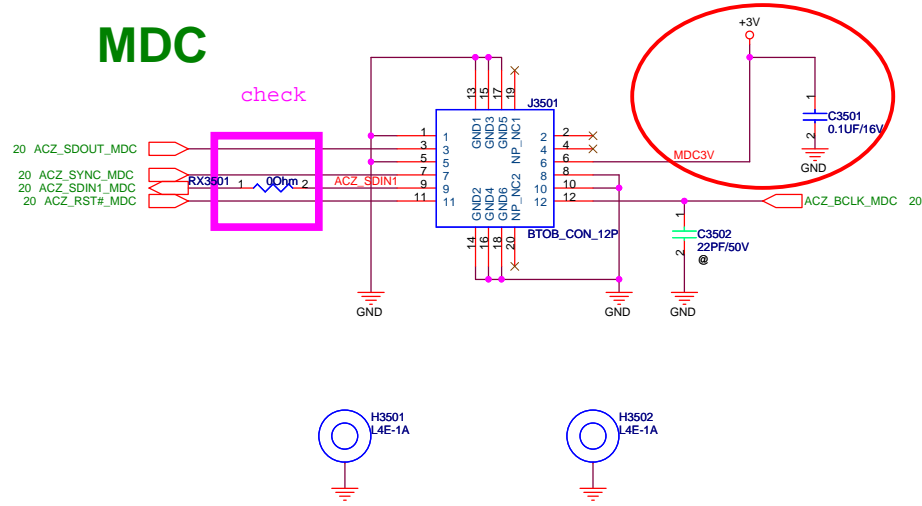
Transformer close CN3402



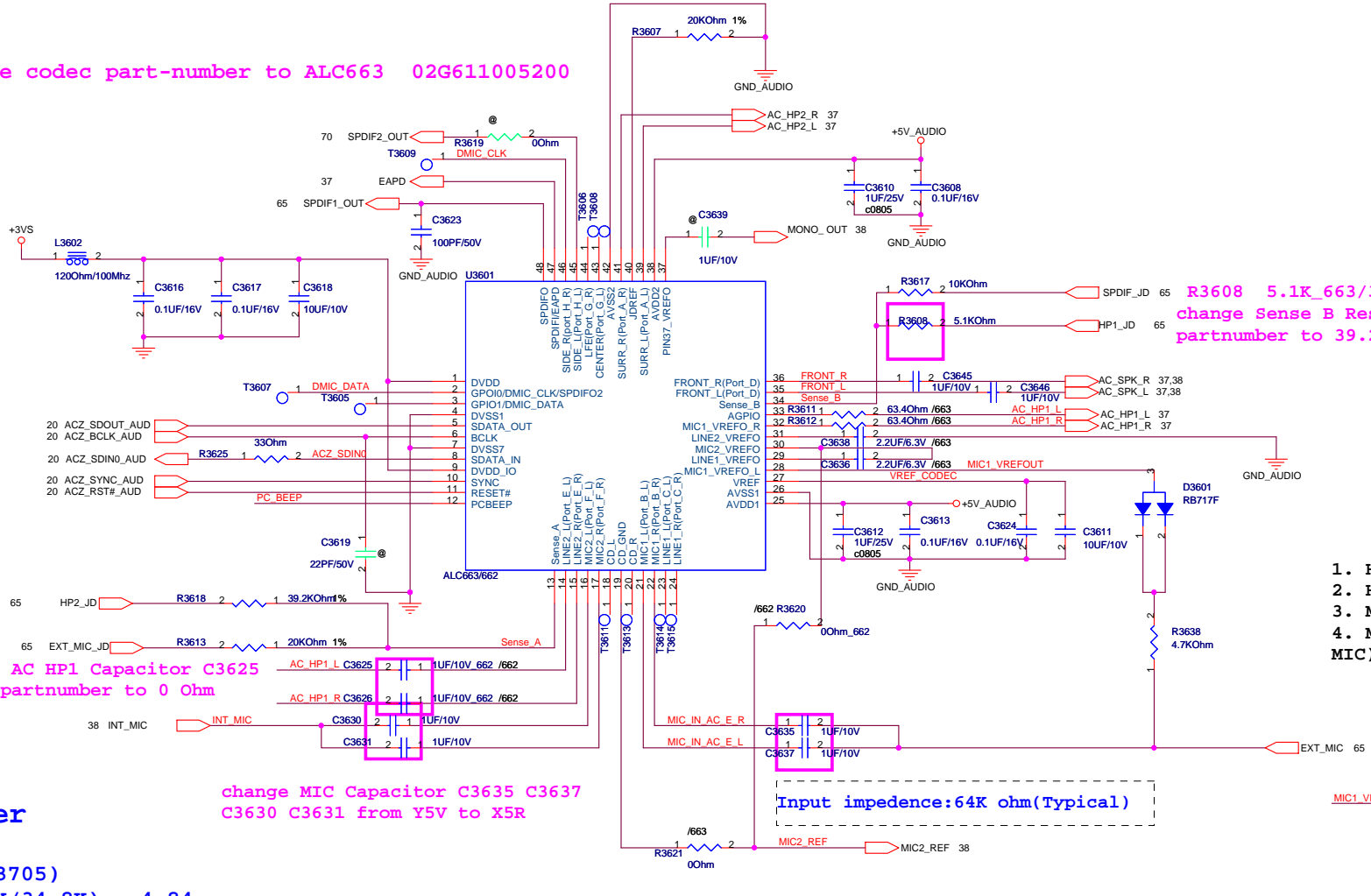
<Variant Name>

ASUS		Title : 10
ASUSTeK COMPUTER INC		Engineer:
Size	Project Name	Rev
Custom		1.01
Date: Wednesday, April 16, 2008	Sheet 34 of 96	

MDC



change codec part-number to ALC663 02G611005200

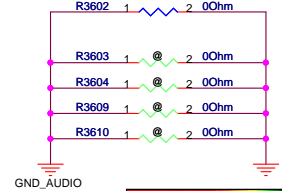
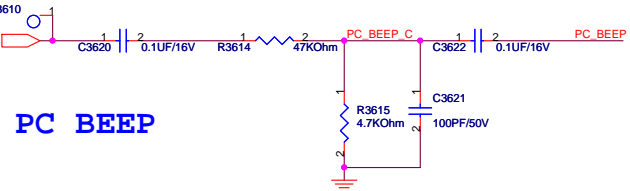
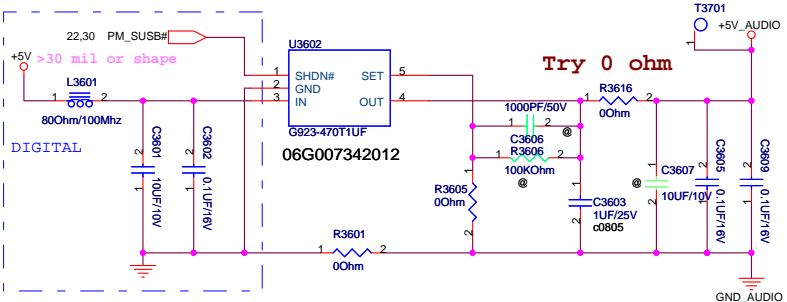


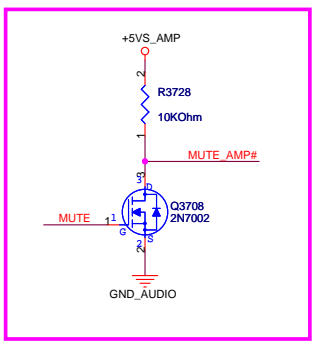
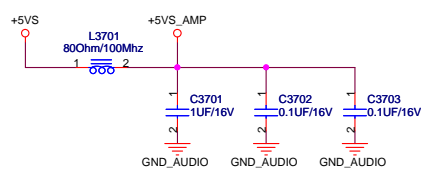
R3608 5.1K_663/39.2K_660
change Sense B Resistor R3608
partnumber to 39.2KOhm for 662

1. HP1 with S/PDIF
2. HP2
3. MIC1(Jack)
4. MIC2 (Digital INT MIC)

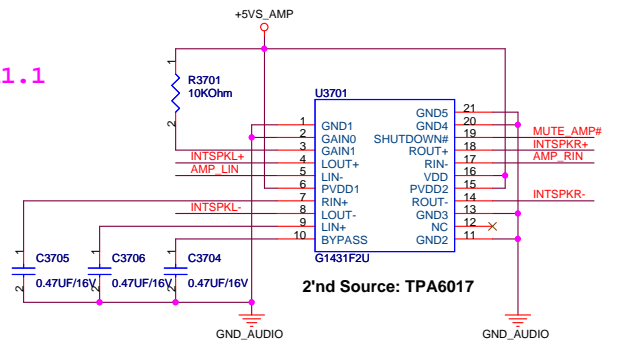
Input impedance: 64K ohm(Typical)

Audio Power
FOR ADJUST MODE:
 $V_o = 1.25 * (1 + R3706 / R3705)$
 $= 1.25 * (1 + 100K / 34.8K) = 4.84$



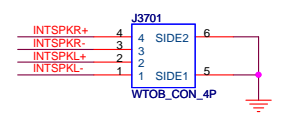


R1.1

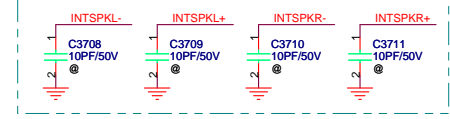


GAIN0	GAIN1	Av (inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

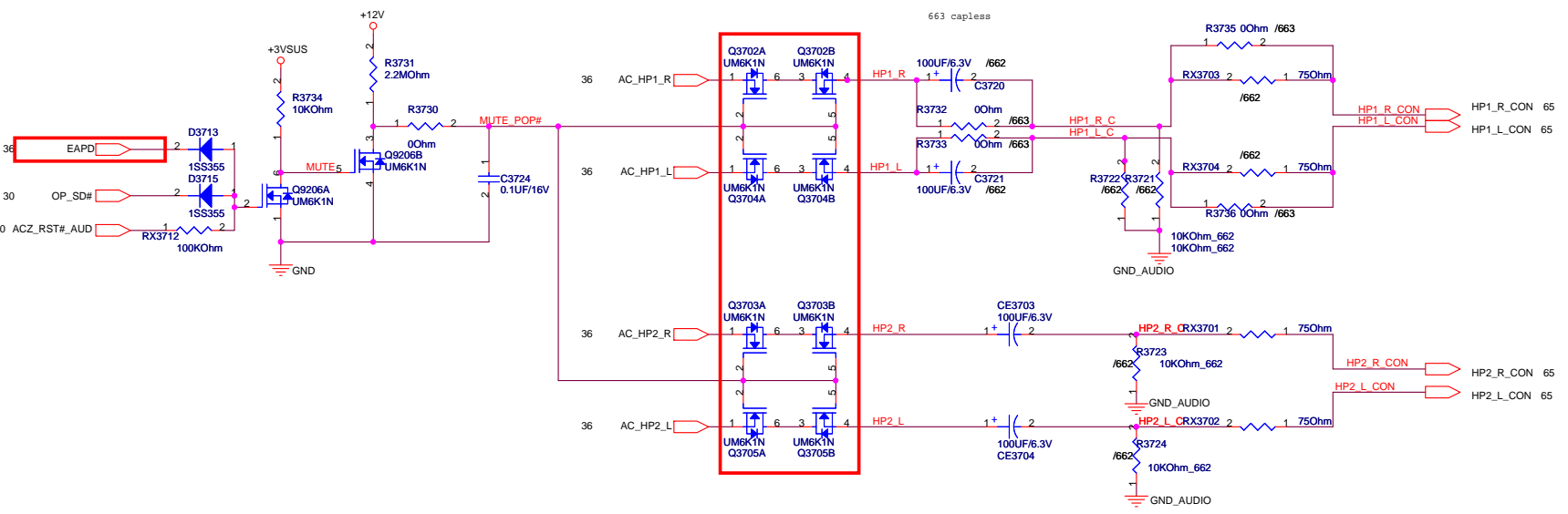
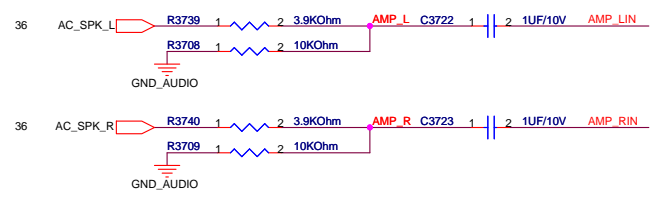
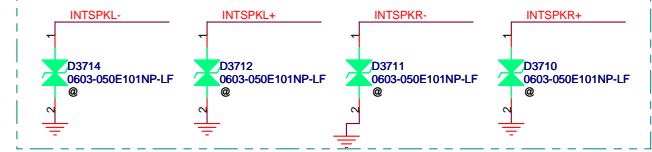
Internal Speaker Conn.

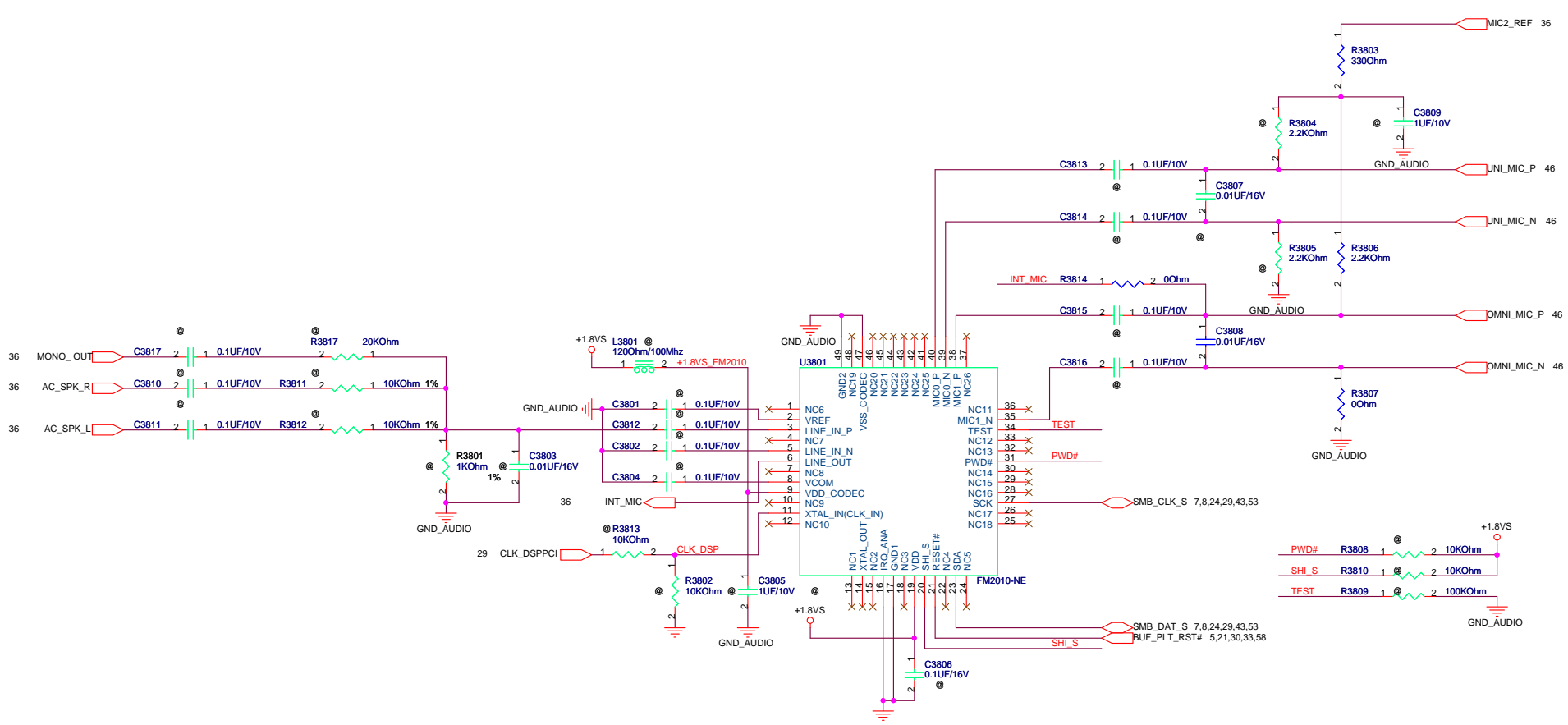


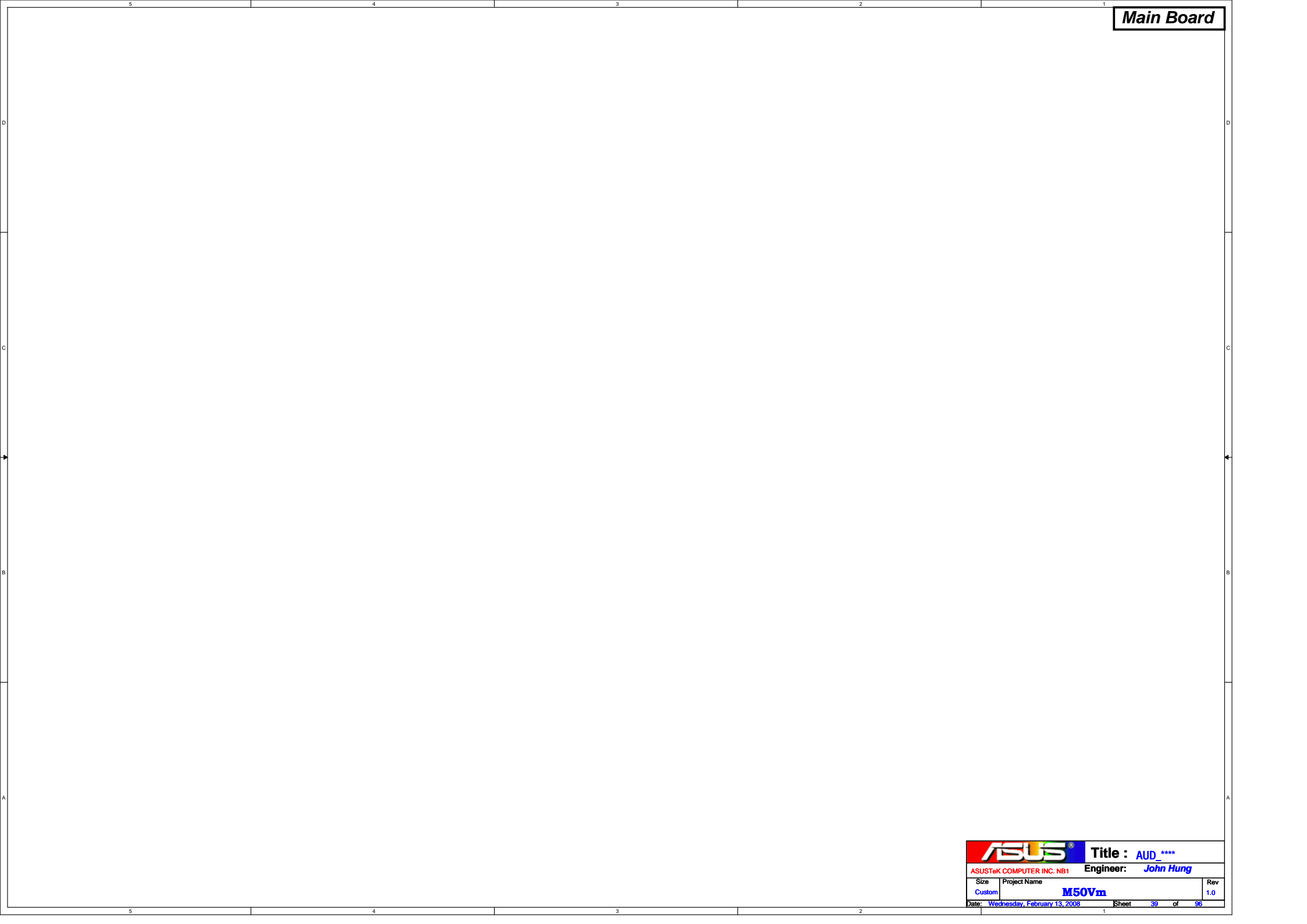
Reserved for 3G



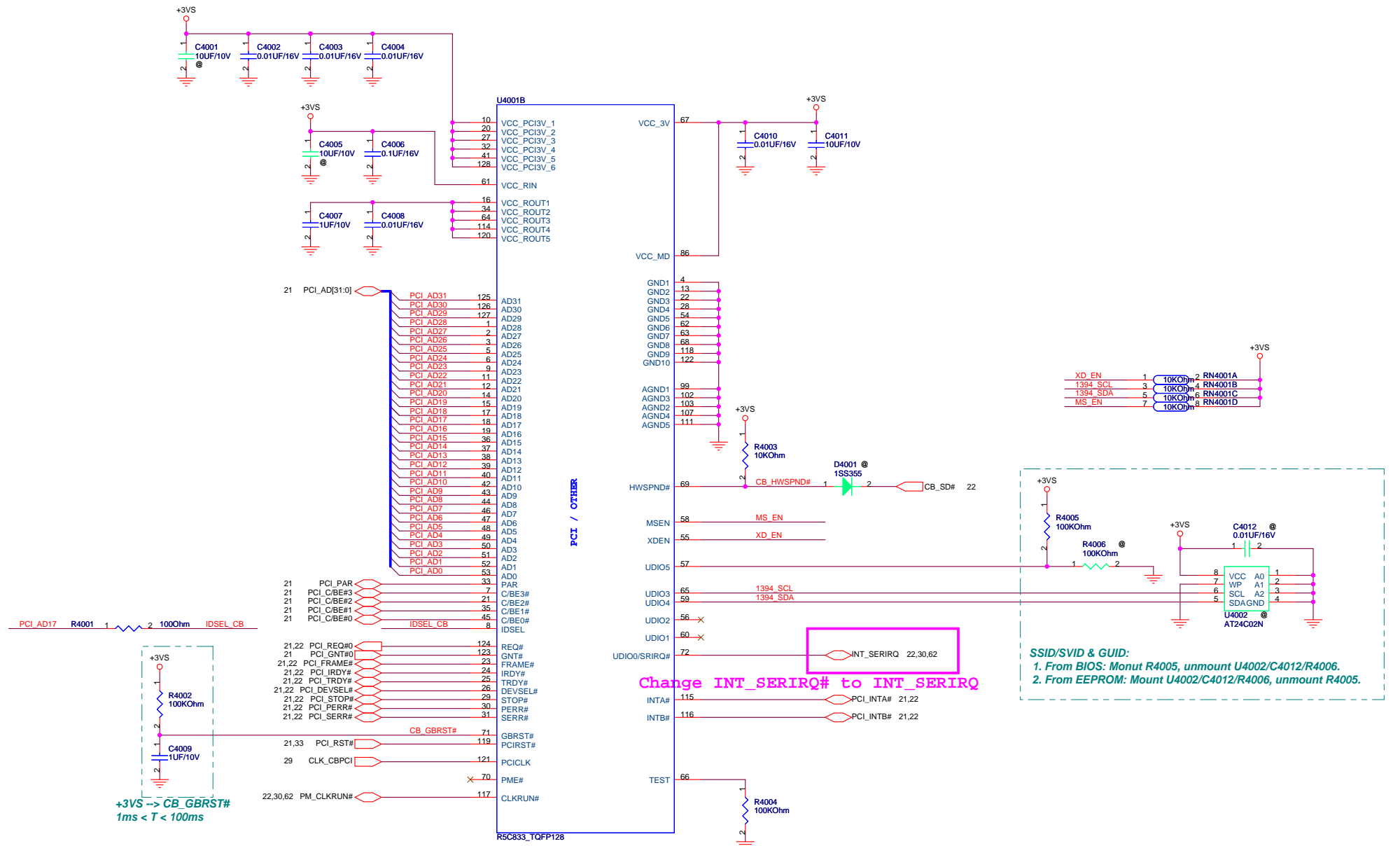
Reserved for EMI

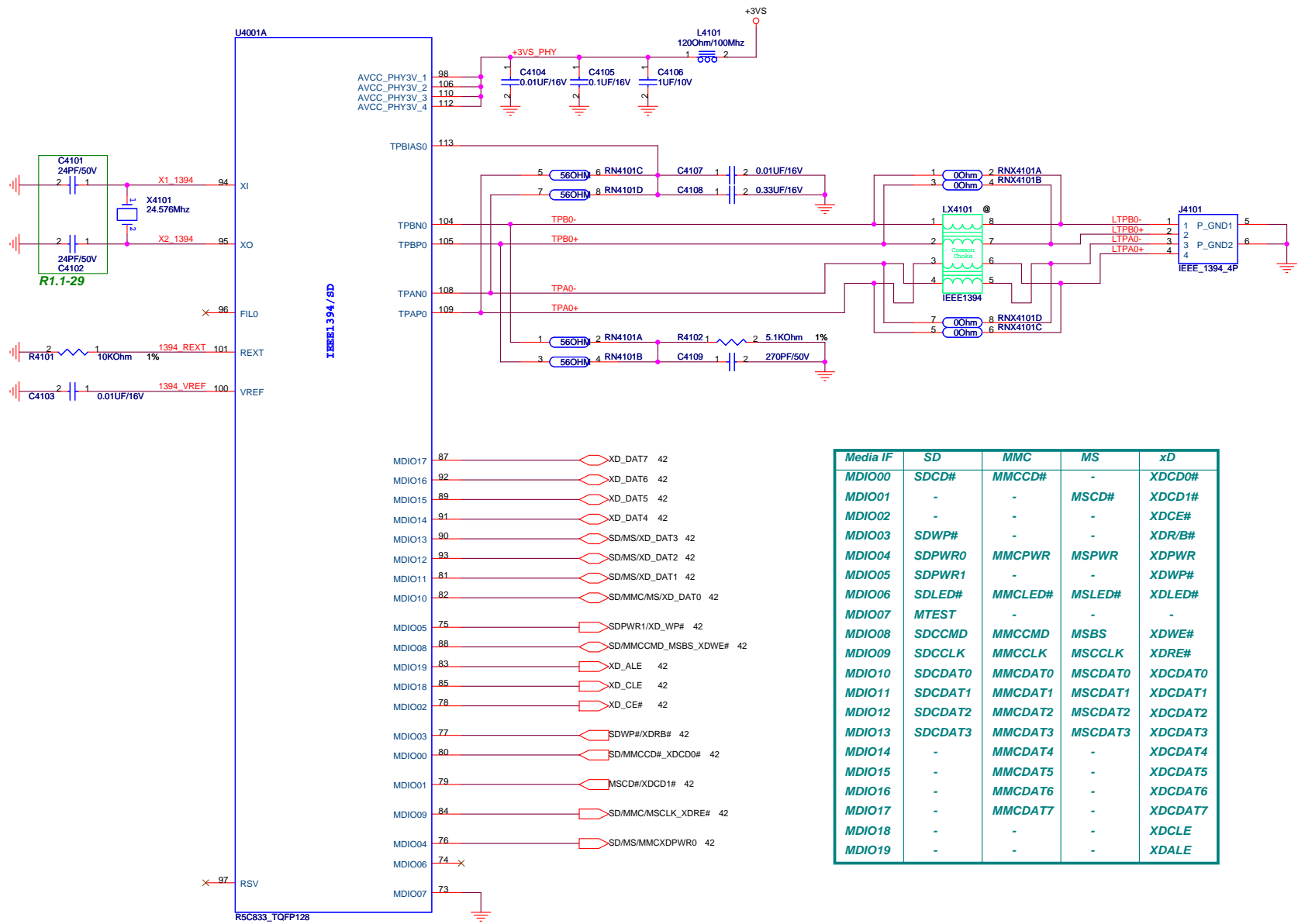




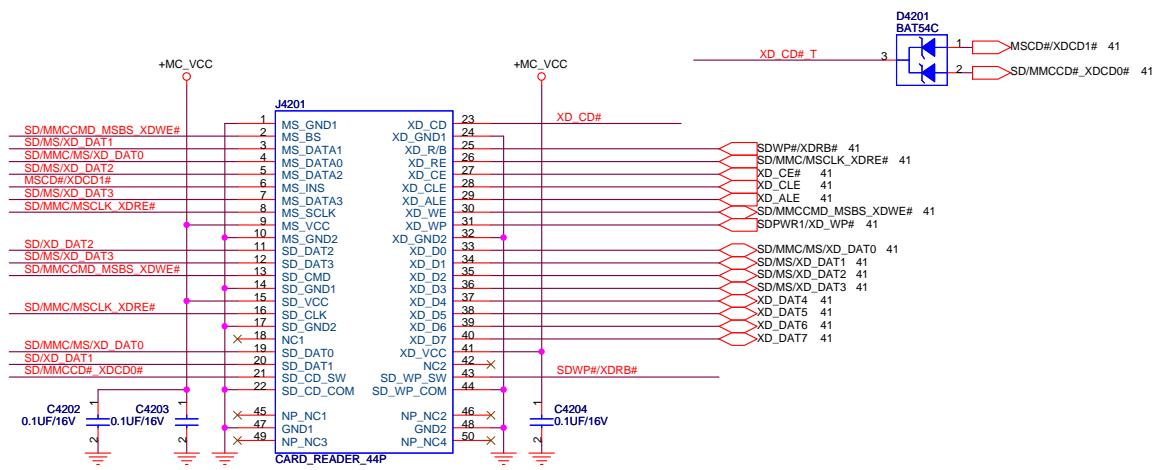
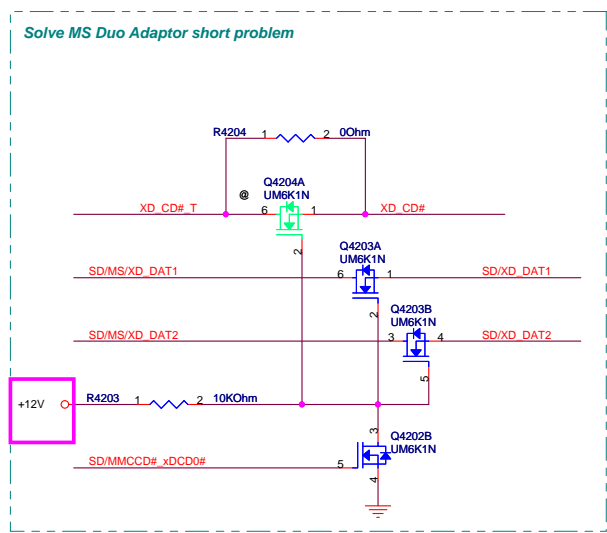
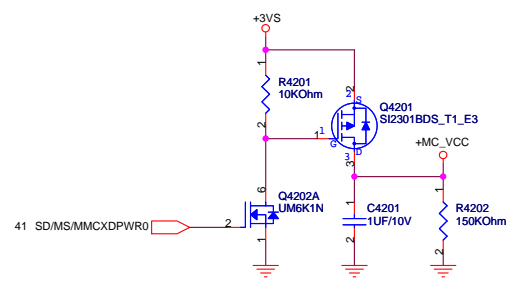


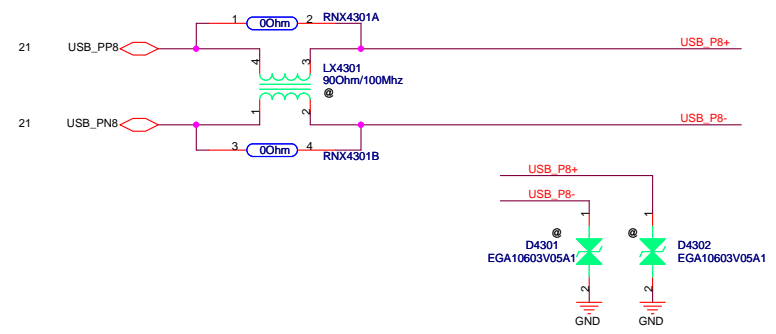
		Title : AUD ****	
ASUSTeK COMPUTER INC. NB1		Engineer: <i>John Hung</i>	
Size	Project Name	Rev	
Custom	M50Vm	1.0	
Date: <i>Wednesday, February 13, 2008</i>		Sheet	39 of 96



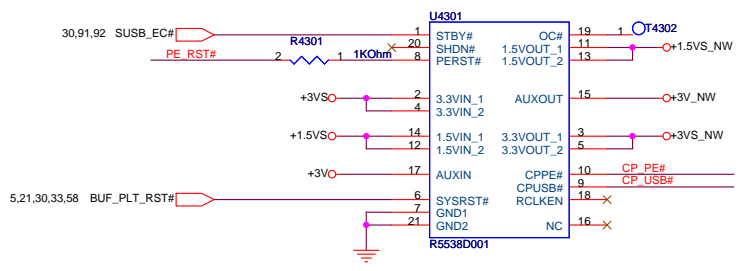


Media IF	SD	MMC	MS	xD
MDIO00	SDCD#	MMCCD#	-	XDCD0#
MDIO01	-	-	MSCD#	XDCD1#
MDIO02	-	-	-	XDCE#
MDIO03	SDWP#	-	-	XDR/B#
MDIO04	SDPWR0	MMCPWR	MSPWR	XD PWR
MDIO05	SDPWR1	-	-	XDWP#
MDIO06	SDLED#	MMCLE#	MSLED#	XDLED#
MDIO07	MTEST	-	-	-
MDIO08	SDCCMD	MMCCMD	MSBS	XDWE#
MDIO09	SDCCLK	MMCCLK	MSCCLK	XDRE#
MDIO10	SDCDAT0	MMCDAT0	MSCDAT0	XDCDAT0
MDIO11	SDCDAT1	MMCDAT1	MSCDAT1	XDCDAT1
MDIO12	SDCDAT2	MMCDAT2	MSCDAT2	XDCDAT2
MDIO13	SDCDAT3	MMCDAT3	MSCDAT3	XDCDAT3
MDIO14	-	MMCDAT4	-	XDCDAT4
MDIO15	-	MMCDAT5	-	XDCDAT5
MDIO16	-	MMCDAT6	-	XDCDAT6
MDIO17	-	MMCDAT7	-	XDCDAT7
MDIO18	-	-	-	XD CLE
MDIO19	-	-	-	XD ALE

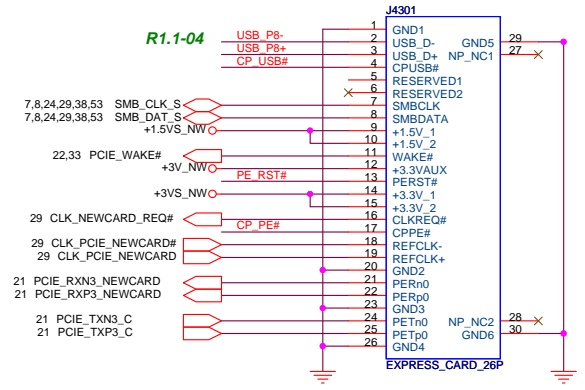




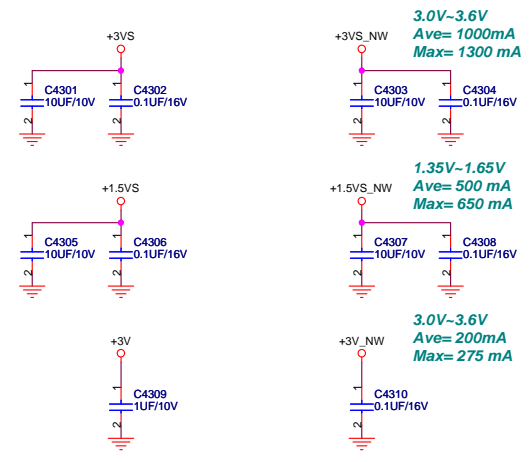
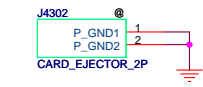
R1.1-04



NewCard Header



NewCard Ejector

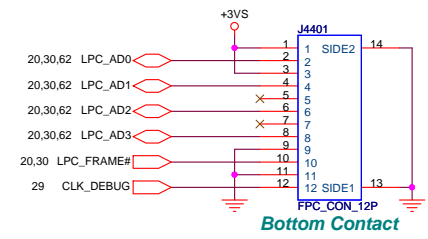


3.0V-3.6V
Ave= 1000mA
Max= 1300 mA

1.35V-1.65V
Ave= 500 mA
Max= 650 mA

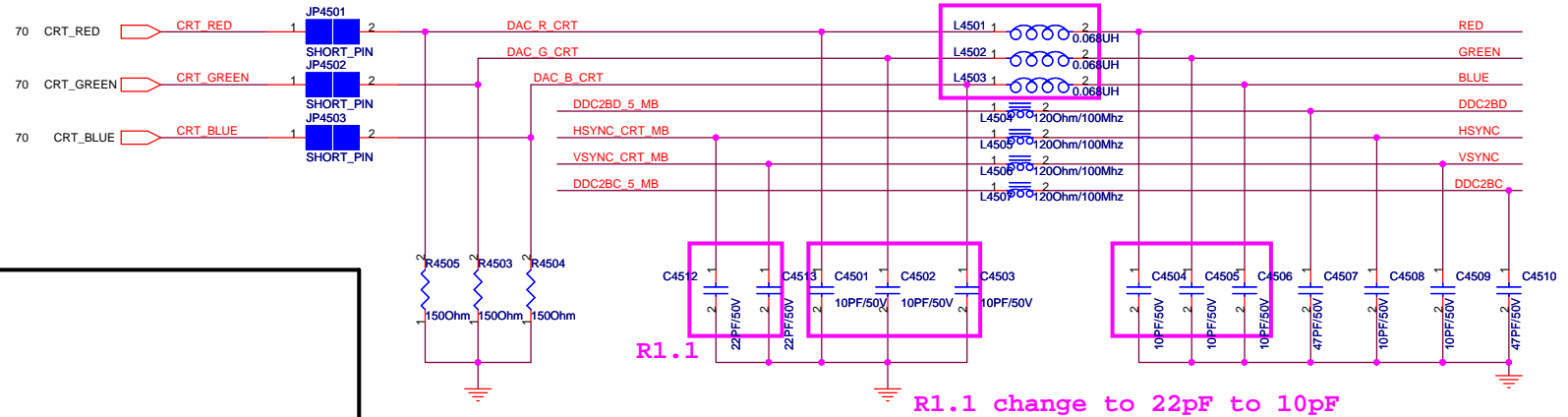
3.0V-3.6V
Ave= 200mA
Max= 275 mA

LPC Debug Port

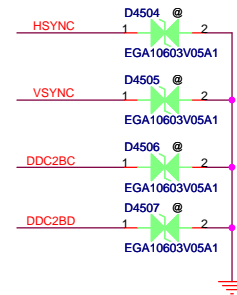
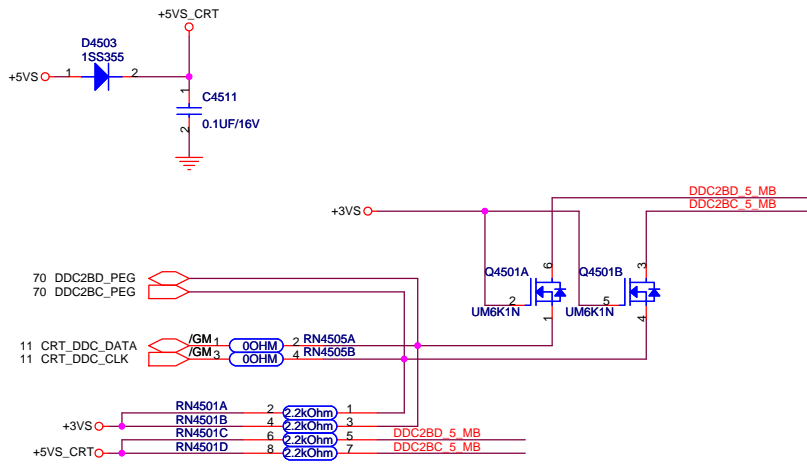


For NewCard Debug Card

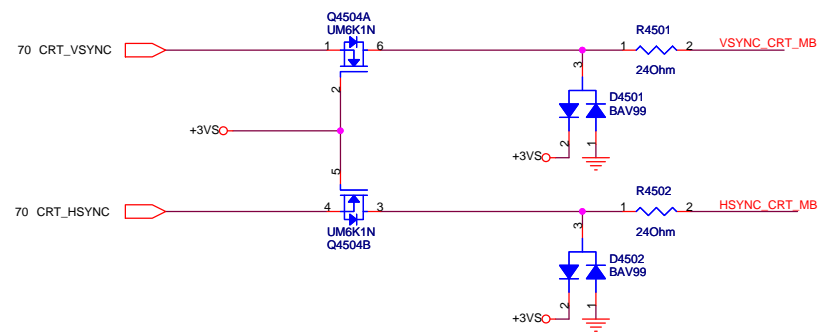
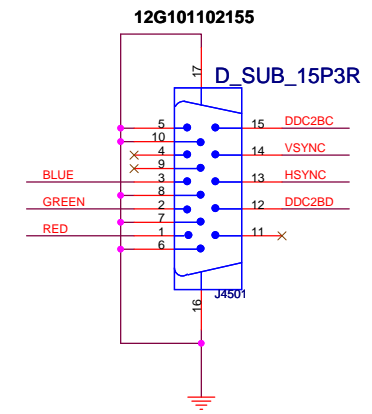
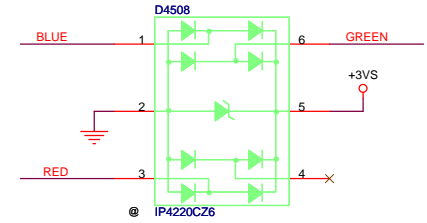


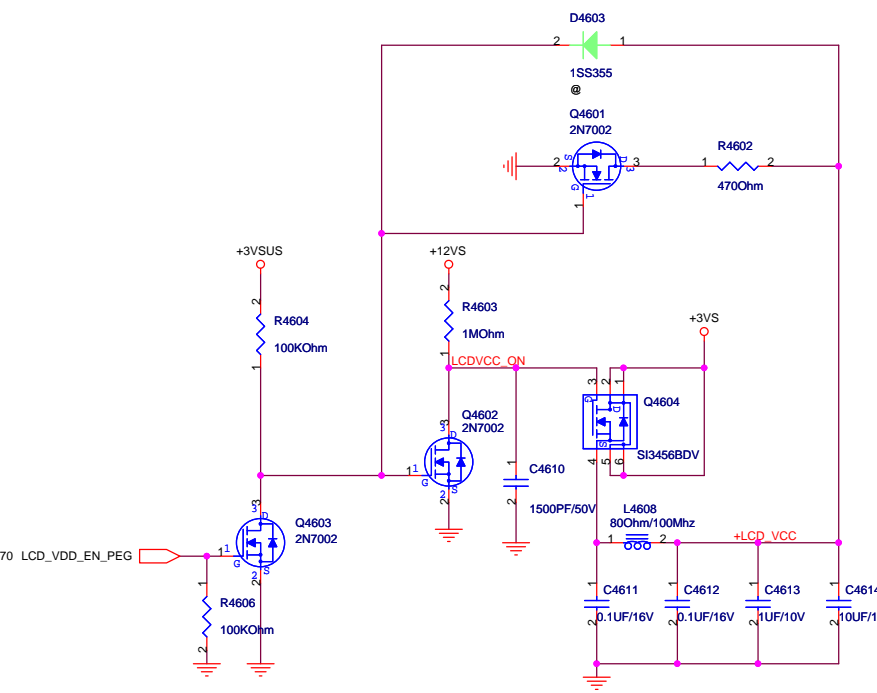


MXM CONNECTOR SIDE

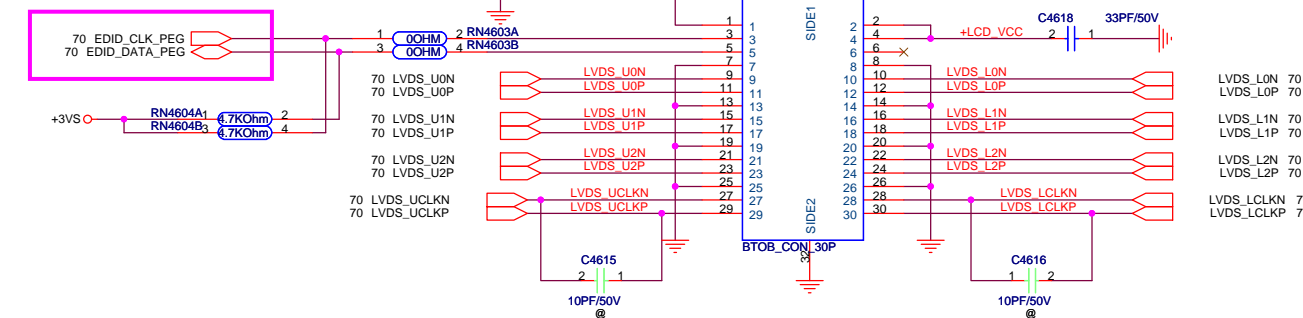


PLACE ESD Diodes near VGA port

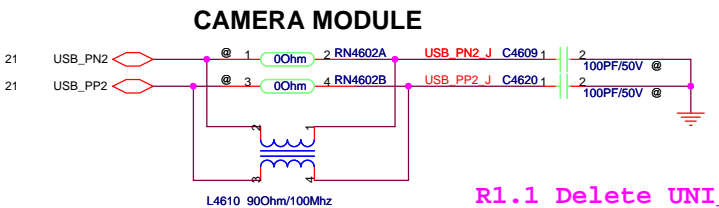
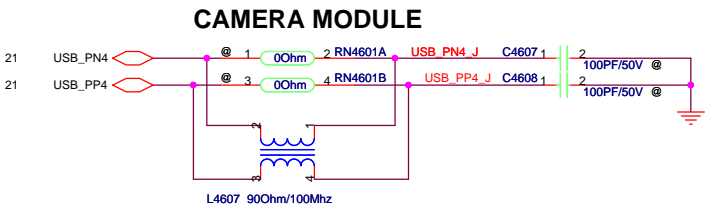




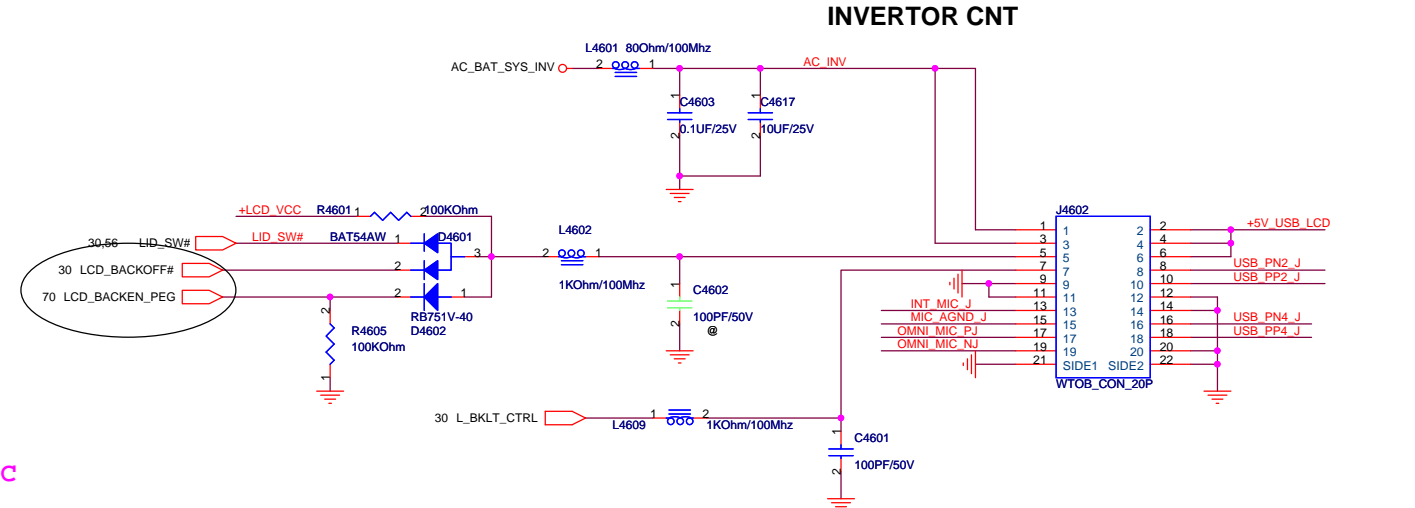
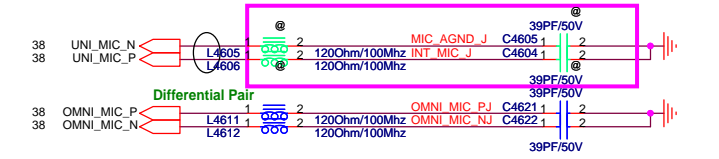
R1.1 SWAP EDID CLK DATA



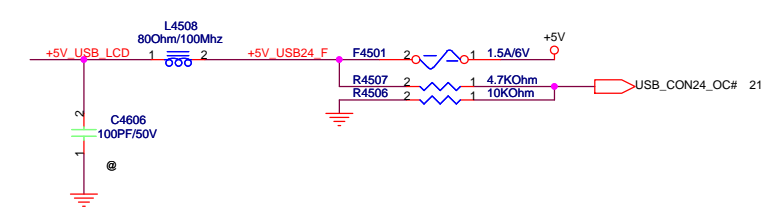
LVDS CNT



R1.1 Delete UNI_MIC



INVERTOR CNT



5

4

3

2

1

D

D

C


C

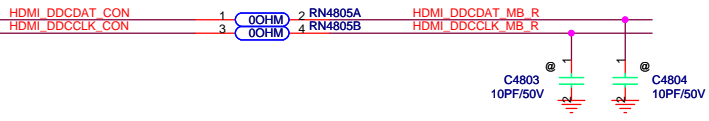
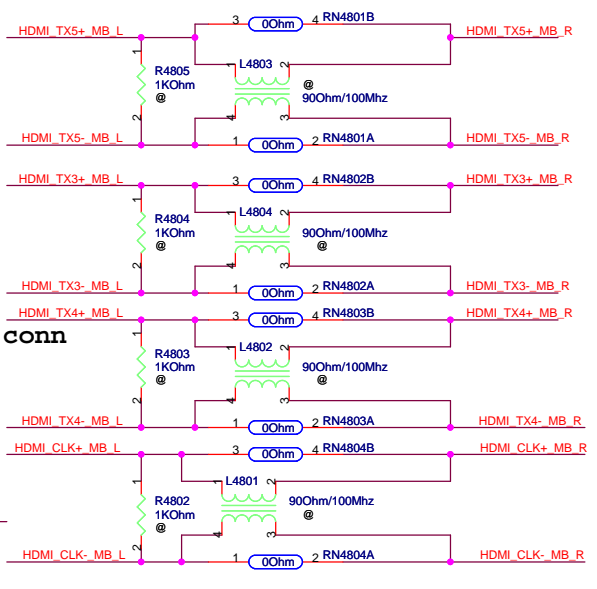
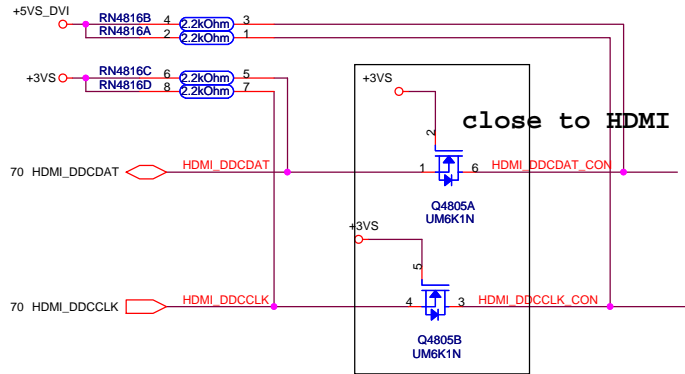
B

B

A

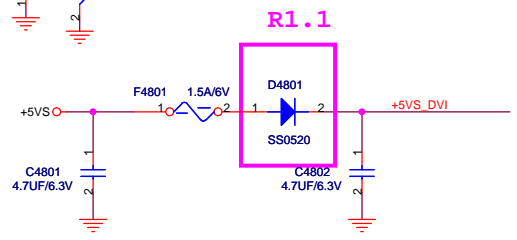
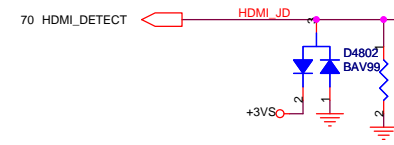
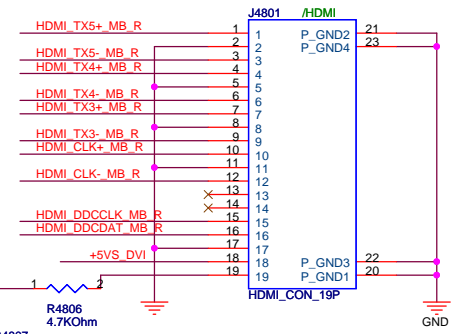
A

		Title : TV_OUT CON	
ASUSTeK COMPUTER INC. NB6		Engineer: <i>Jace_Kuo</i>	
Size	Project Name	Rev	
Custom	M50Vm	1.0	
Date: Wednesday, February 13, 2008		Sheet	47 of 96



HDMI CNT

12G241101928



R1.1

Delete HDMI UMA

HDMI TX3- MB L	VGA_HDMI_TX3- 70
HDMI TX3+ MB L	VGA_HDMI_TX3+ 70
HDMI TX4- MB L	VGA_HDMI_TX4- 70
HDMI TX4+ MB L	VGA_HDMI_TX4+ 70
HDMI TX5- MB L	VGA_HDMI_TX5- 70
HDMI TX5+ MB L	VGA_HDMI_TX5+ 70
HDMI CLK- MB L	VGA_HDMI_CLKB- 70
HDMI CLK+ MB L	VGA_HDMI_CLKB+ 70

5

4

3

2

1

D

D

C


C

B

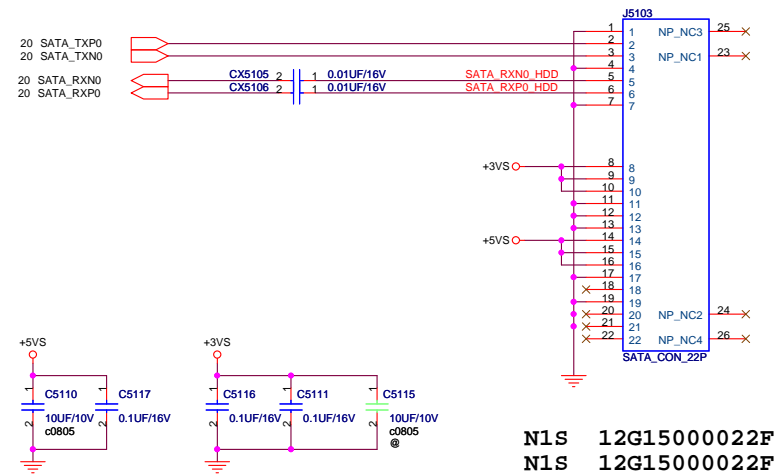
B

A

A

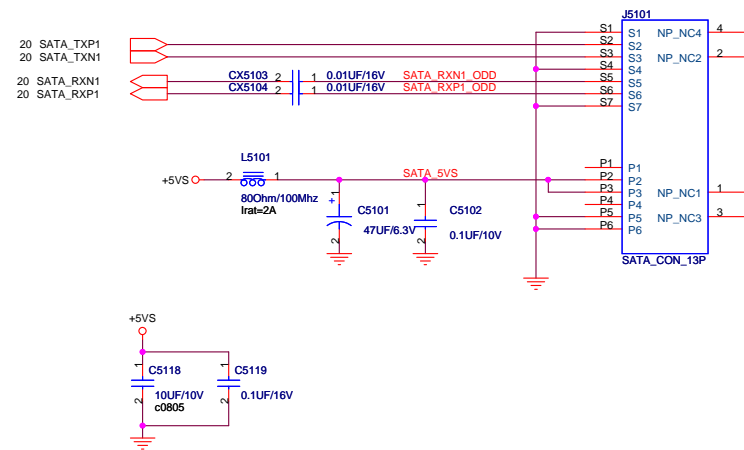
		Title :	
ASUSTeK COMPUTER INC. NB6		Engineer: <i>Jace_Kuo</i>	
Size	Project Name	Rev	
Custom	M50Vm	1.0	
Date: <i>Wednesday, February 13, 2008</i>		Sheet	49 of 96

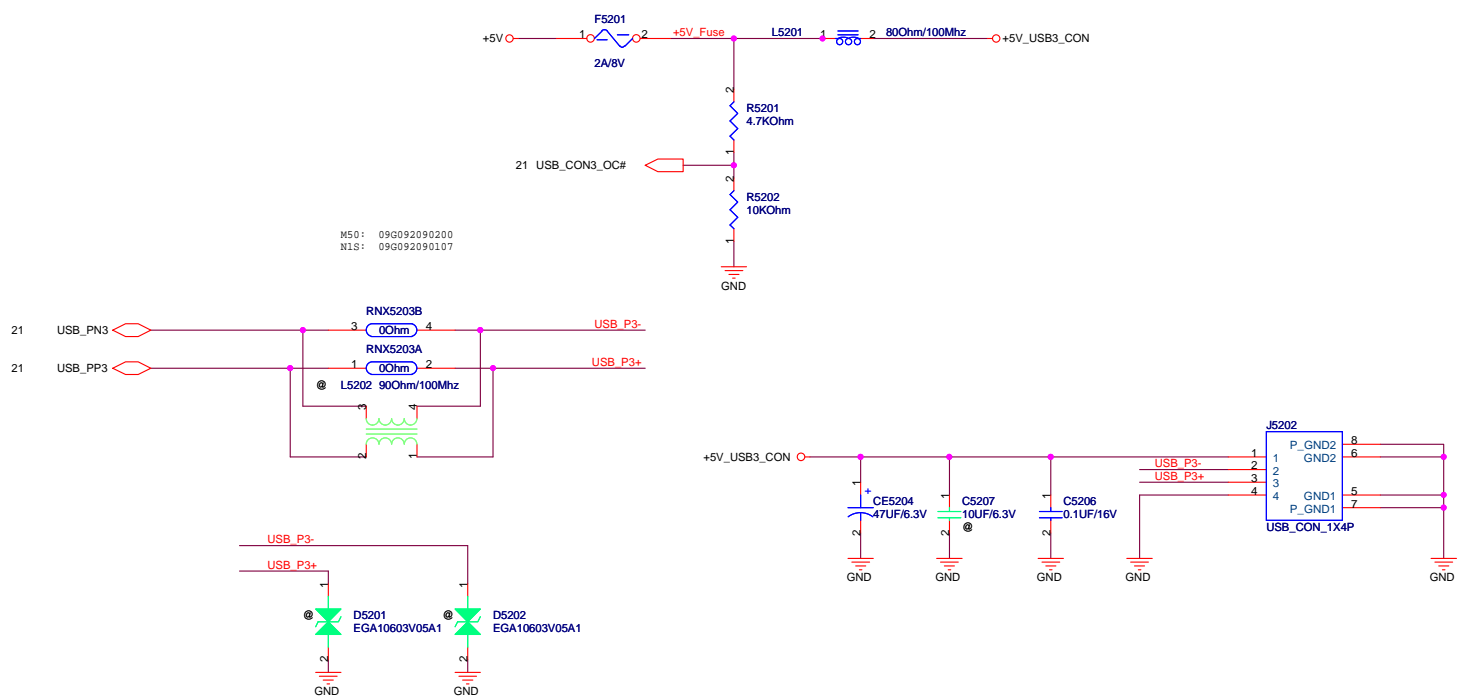
SATA0 HDD CON

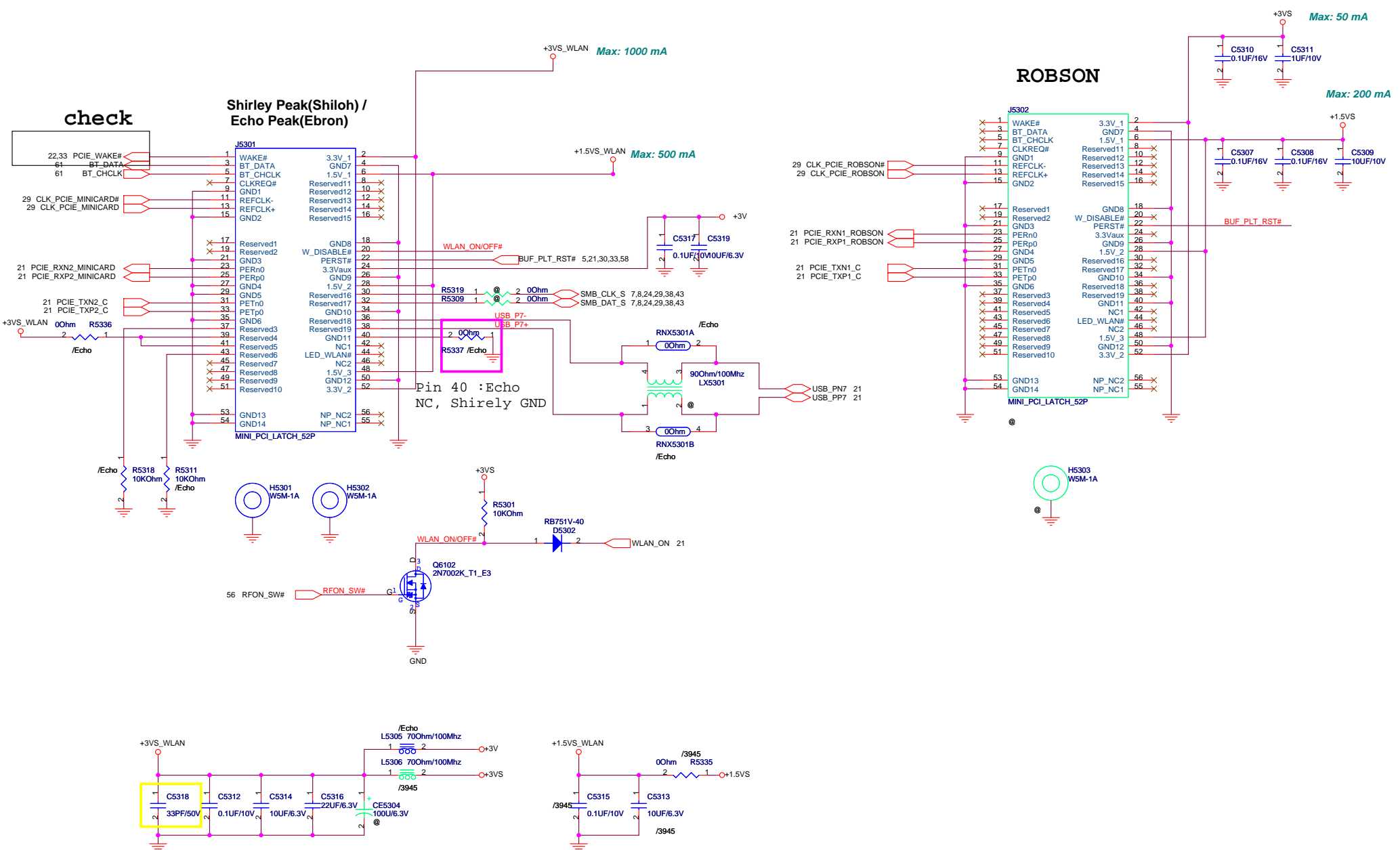


LAYOUT NOTE:
Two Strobes : Matched within 100 mils of each other
D[0:15] : Matched within +/- 450 mils of two strobes

ODD CNT







5

4

3

2

1

D

D

C


C

B

B

A

A

		Title :
Engineer:		
Size	Project Name	Rev
A		1.0
Date: Wednesday, February 13, 2008		Sheet 54 of 96

5

4

3

2

1

5

4

3

2

1

D

D

C

C

B

B

A

A



Title :

Engineer:

Size	Project Name	Rev
A		1.0

Date: Wednesday, February 13, 2008 Sheet 55 of 96

5

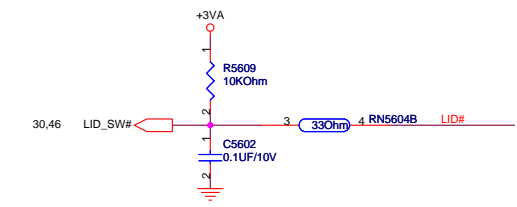
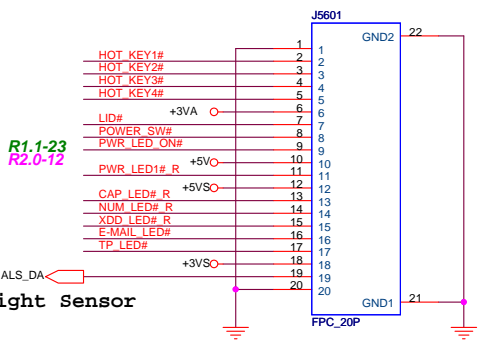
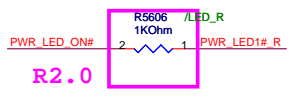
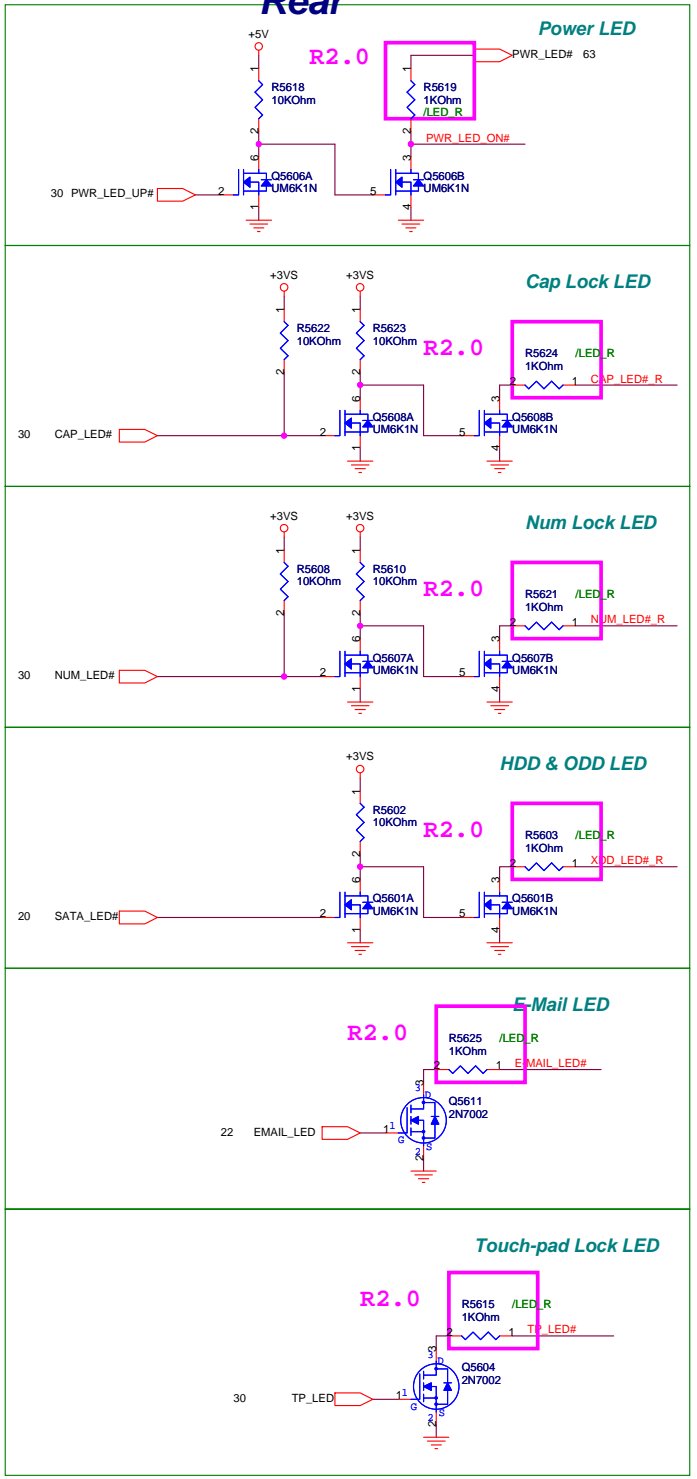
4

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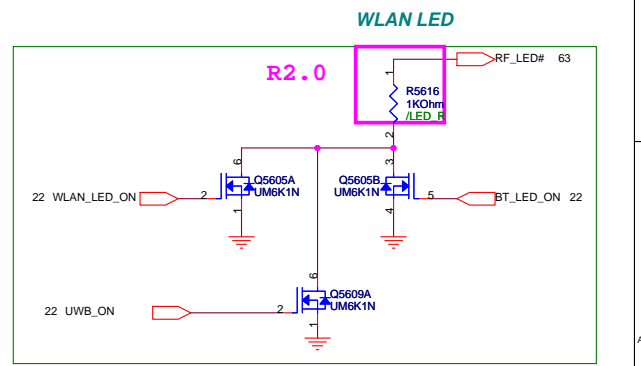
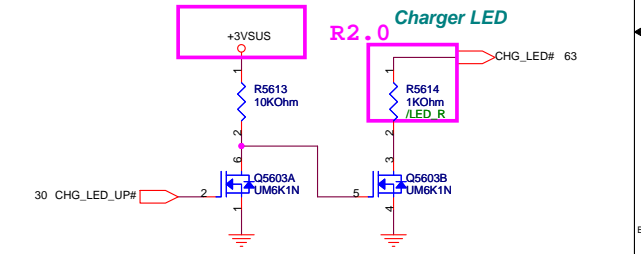
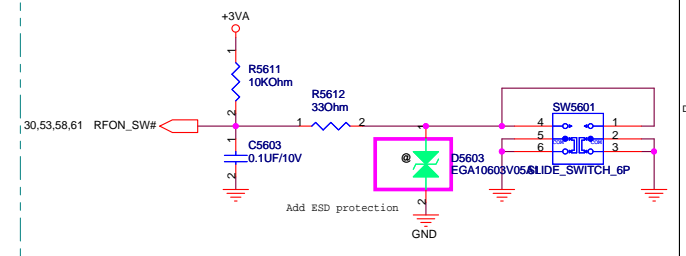
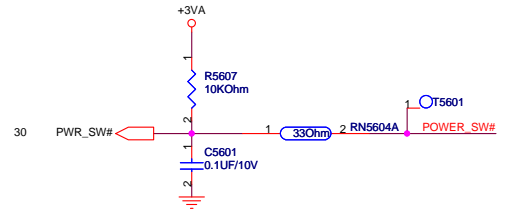
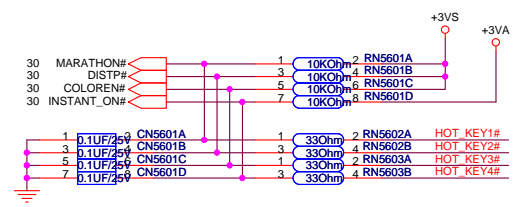
2

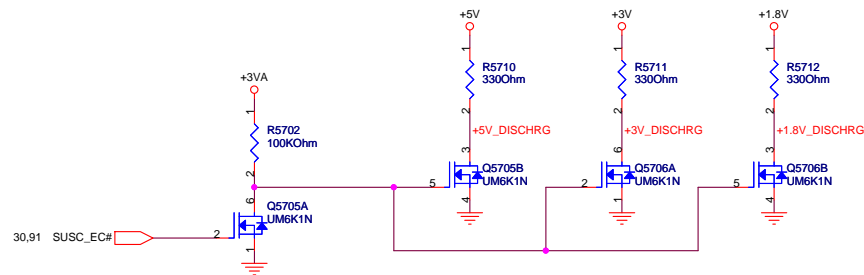
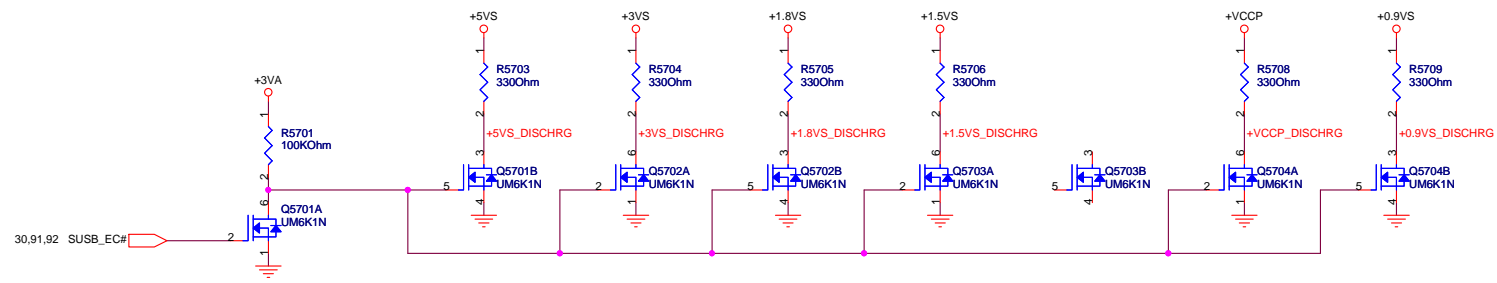
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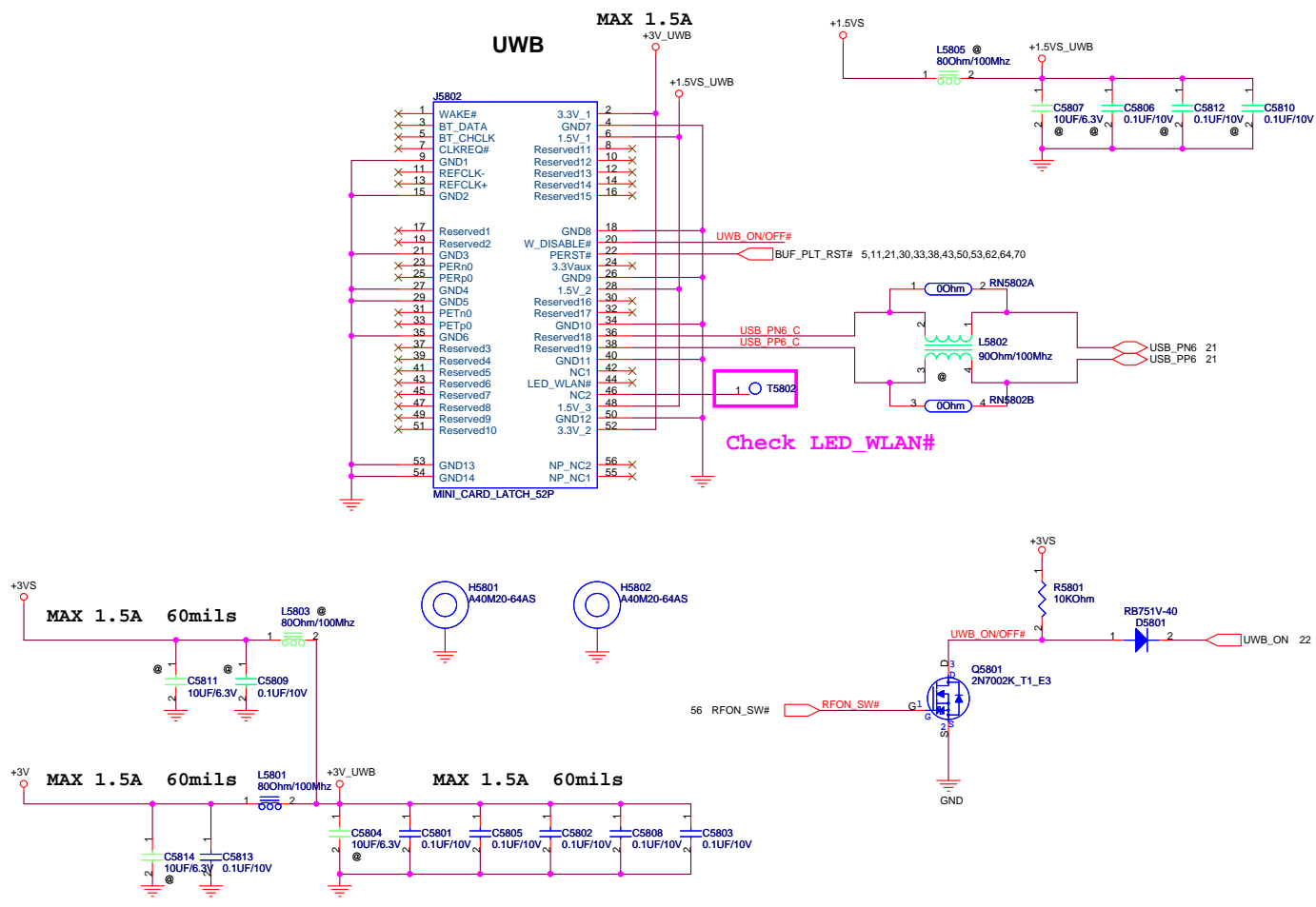
Rear



1. Power4Gear
2. Touch-Pad ON/OFF
3. Splendid
4. Instant Fun Plus
5. Power Button







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Title :

ASUSTeK COMPUTER INC. NB6

Engineer:

Size	Project Name	Rev
A		1.0

Date: Wednesday, February 13, 2008 Sheet 59 of 96

5

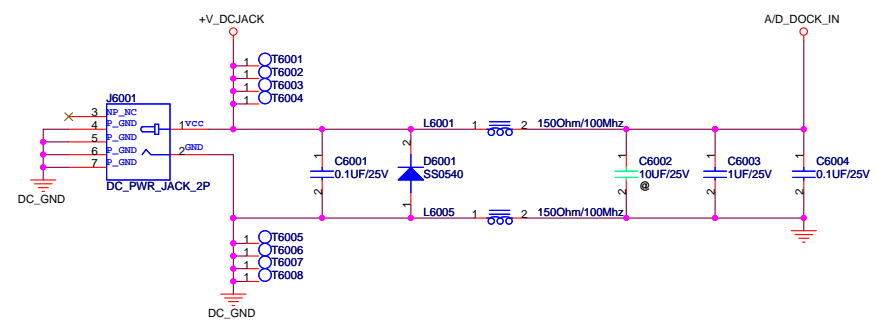
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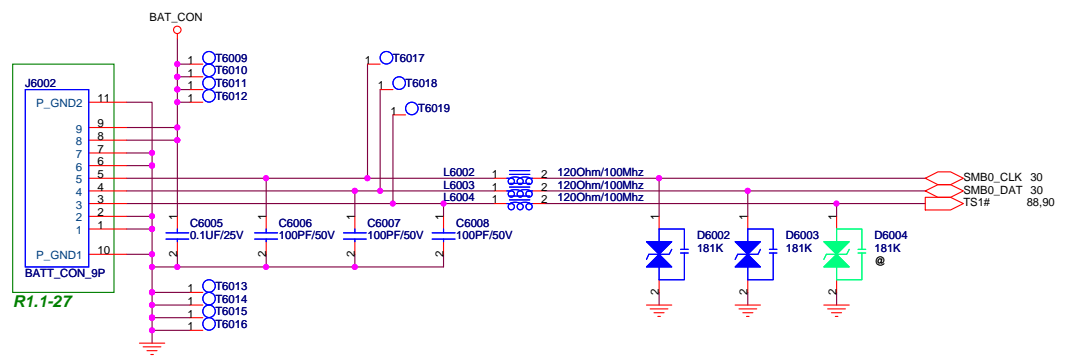
2

1

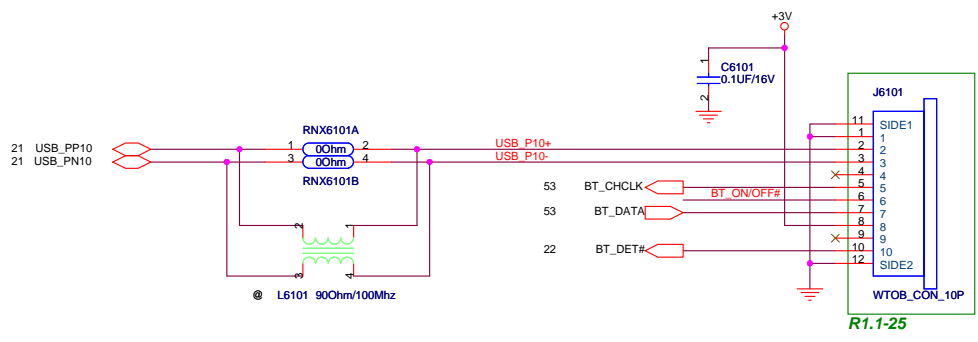
DC Jack



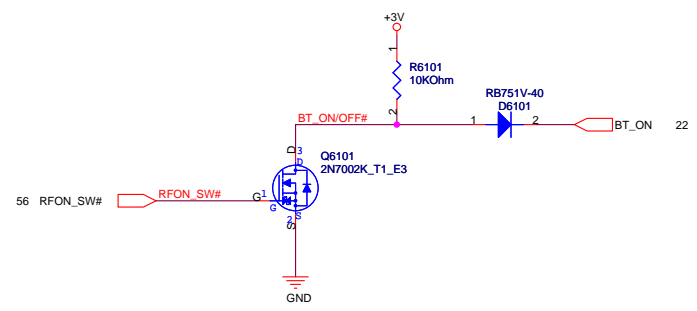
Battery Connector

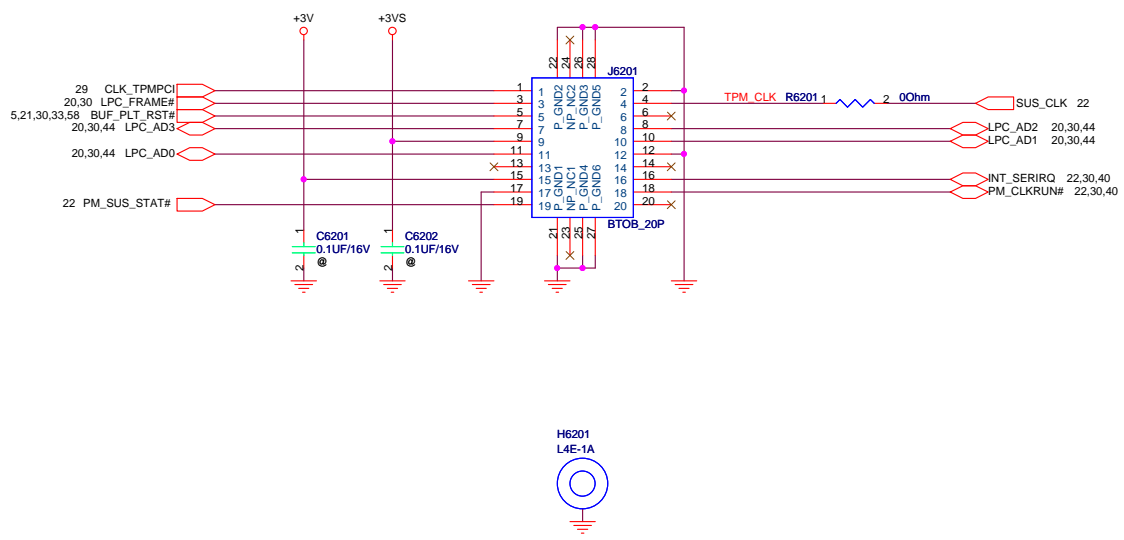


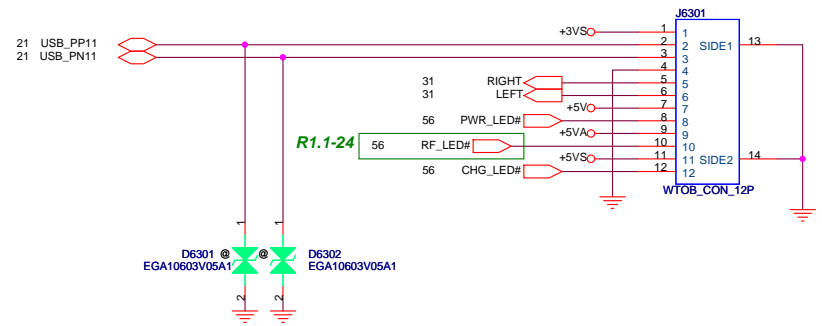
R1.1-27

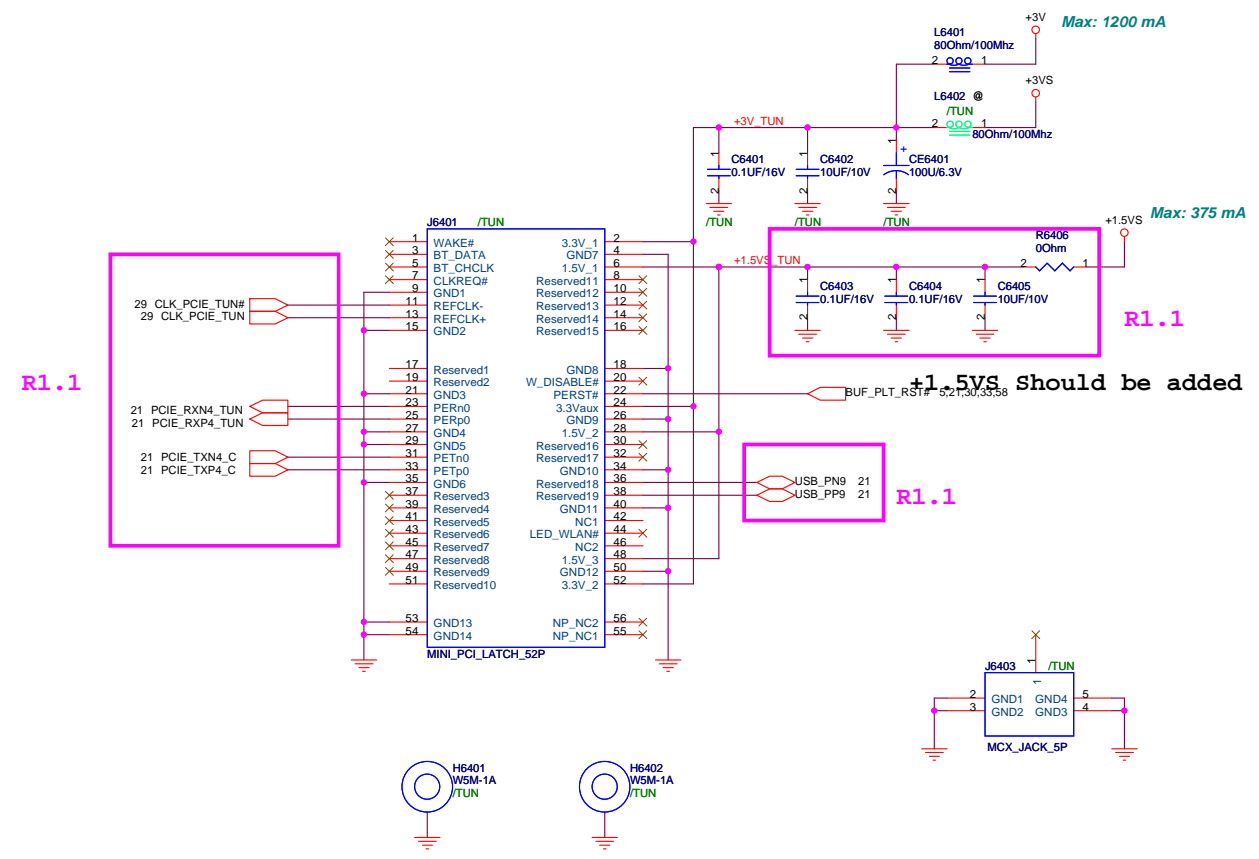


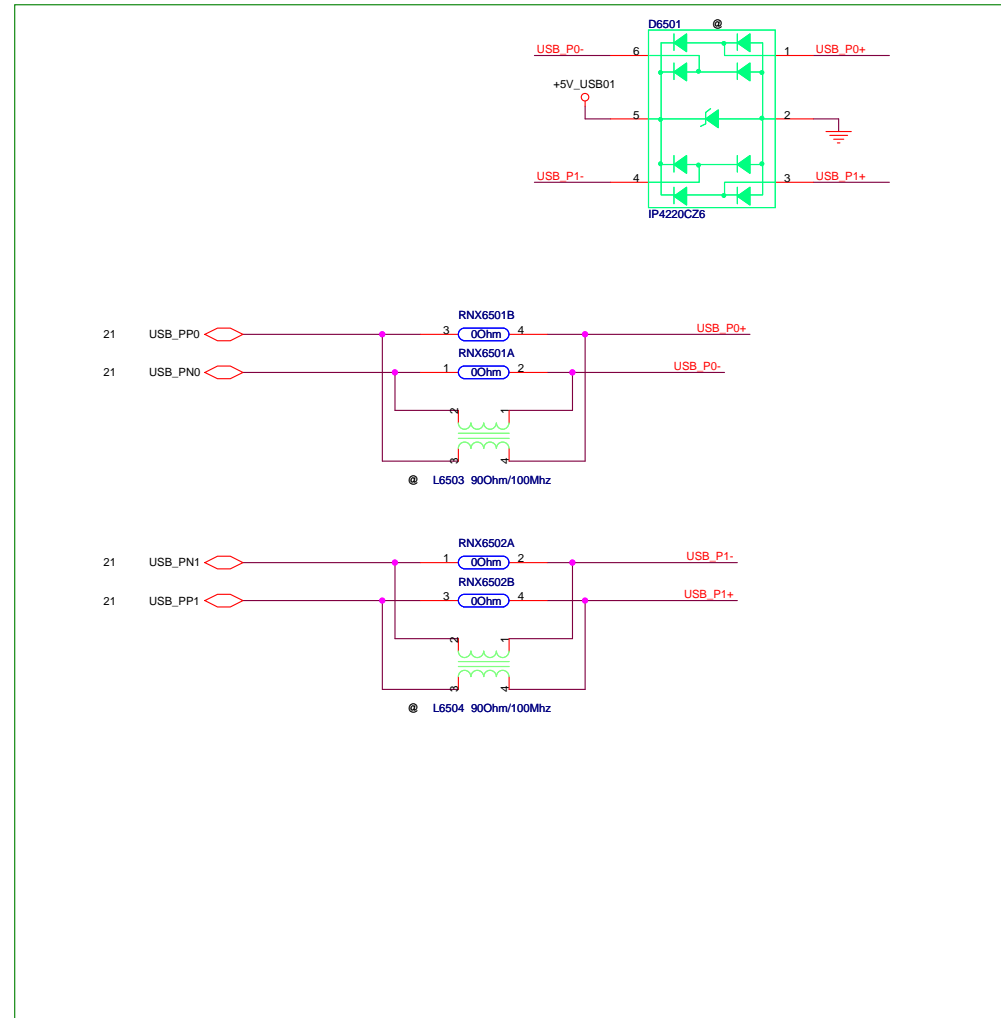
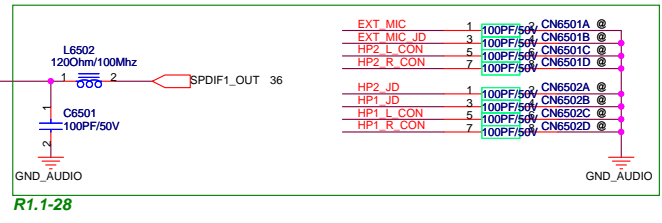
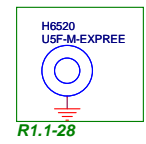
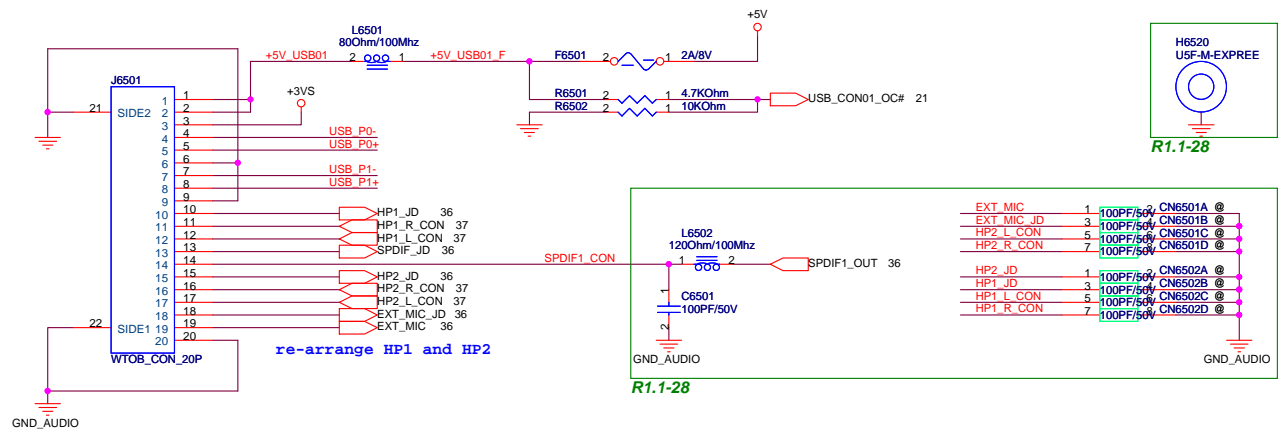
BT change from 2.0 to 2.1



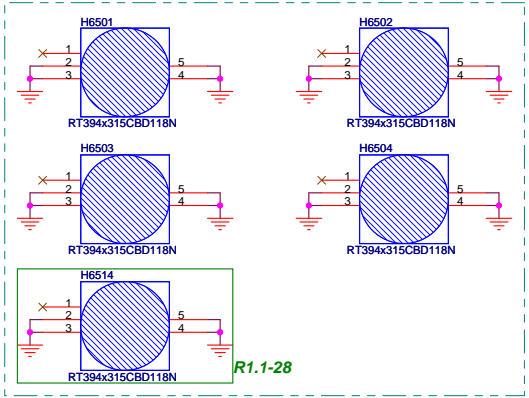




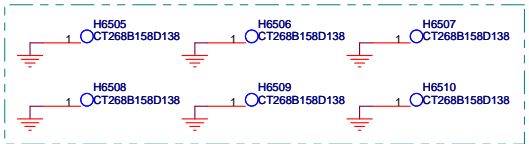




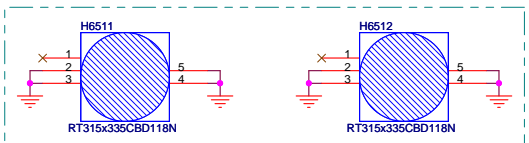
Screw Hole A



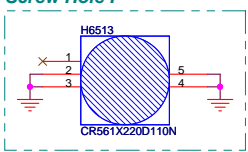
Screw Hole B



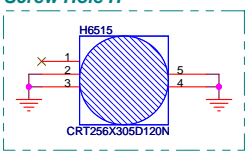
Screw Hole C



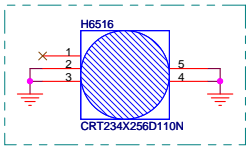
Screw Hole F



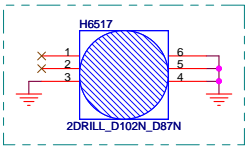
Screw Hole H



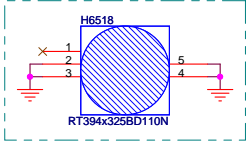
Screw Hole I



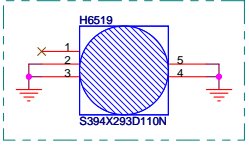
Screw Hole J

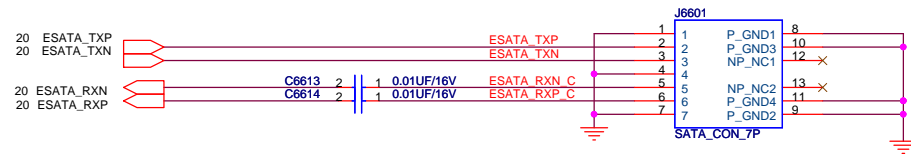


Screw Hole K



Screw Hole L







		Title : PCI_WWAN
ASUSTeK COMPUTER INC. NB1		Engineer: <i>John Hung</i>
Size	Project Name	Rev
Custom	M50Vm	1.0
Date: <i>Wednesday, February 13, 2008</i>		Sheet 67 of 96

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		Title :	
Engineer:			
Size	Project Name		Rev
A			1.0
Date: Wednesday, February 13, 2008		Sheet	68 of 96

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		Title :	
Engineer:			
Size	Project Name		Rev
A			1.0
Date: Wednesday, February 13, 2008		Sheet	69 of 96

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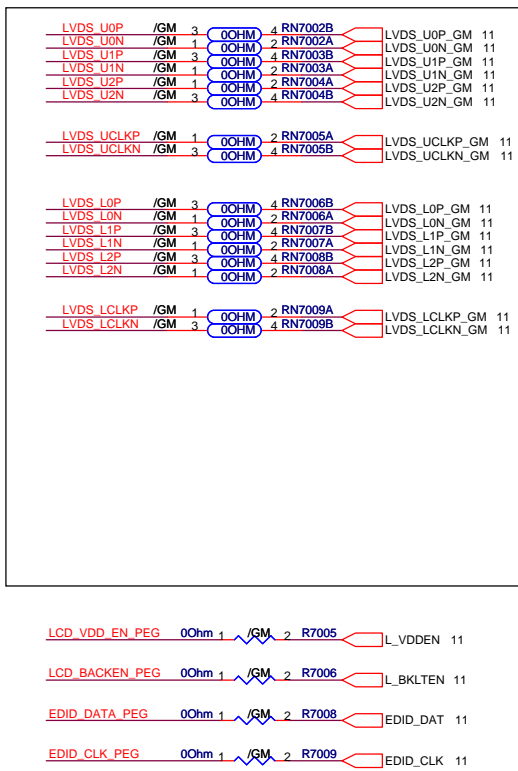
4

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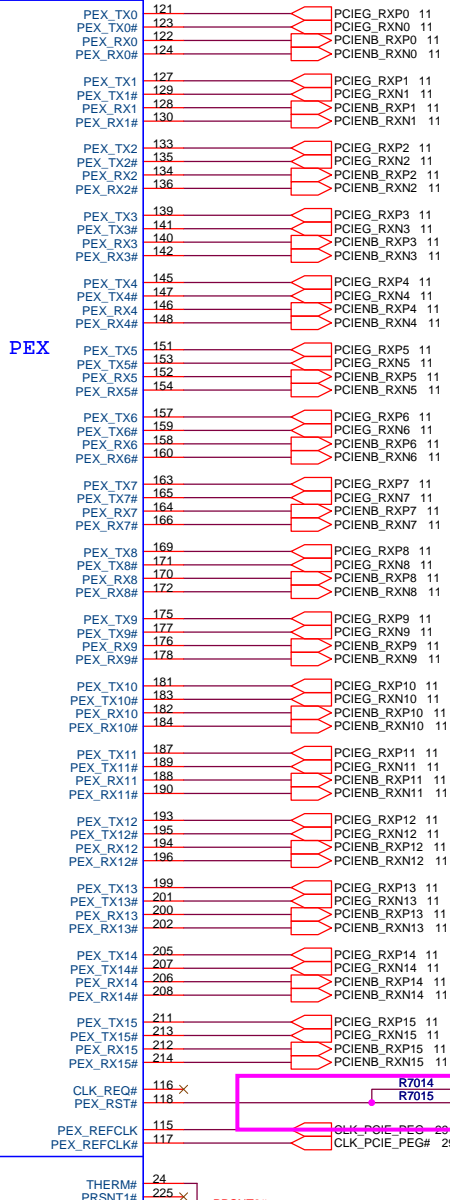
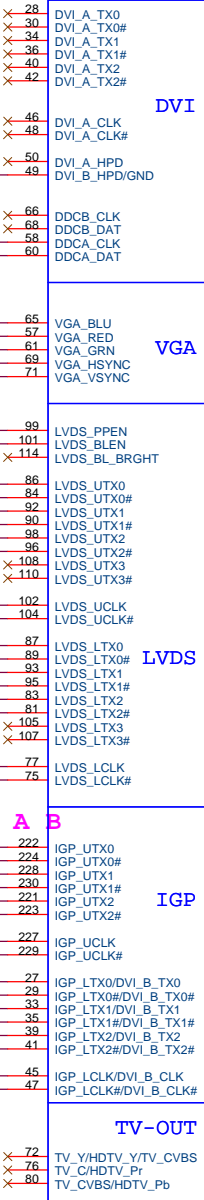
2

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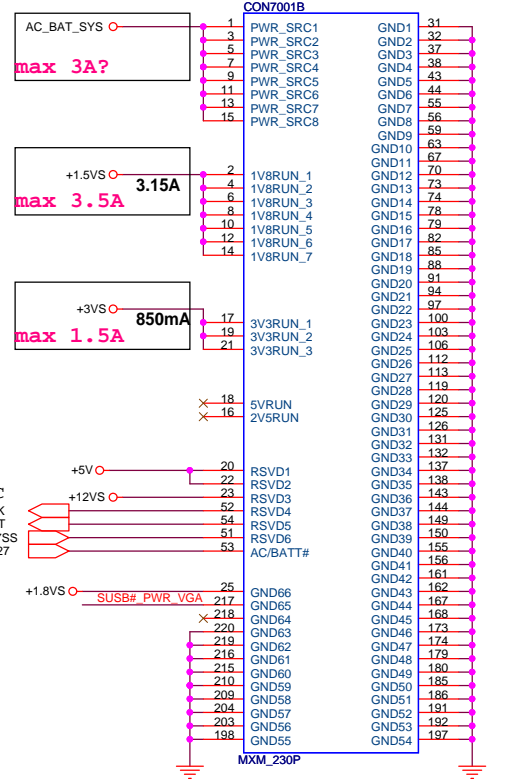
RESISTORS CLOSE TO MXM



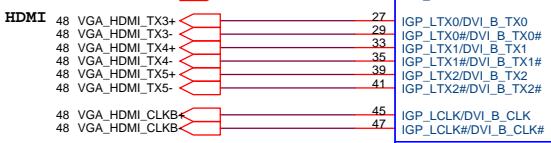
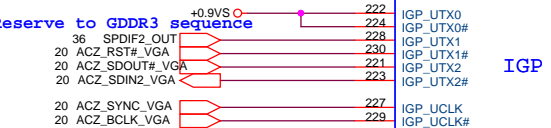
CON7001A



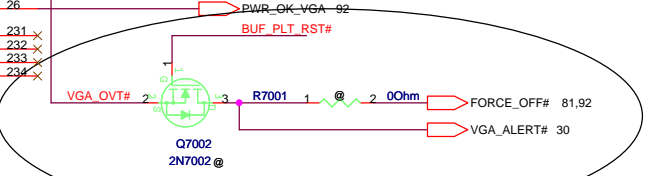
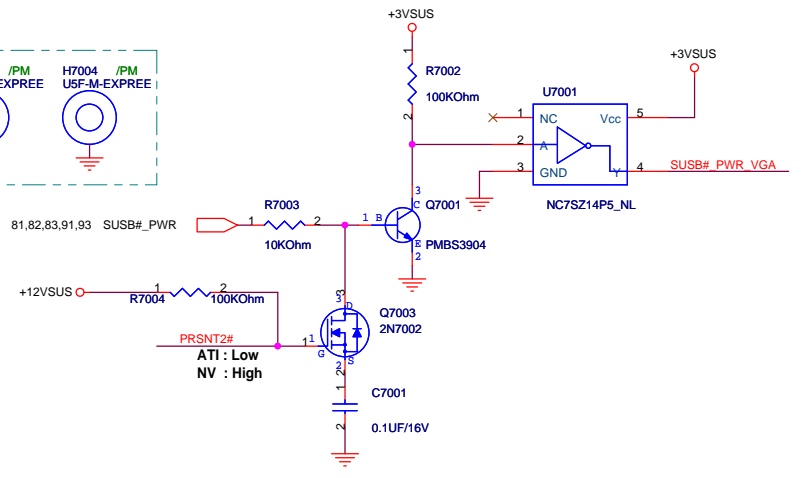
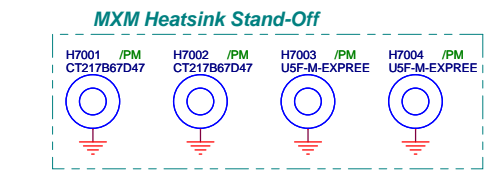
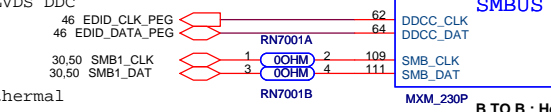
CON7001B



R1.1 SWAP LVDS Channel A B



OTHER



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		Title :	
Engineer:			
Size	Project Name		Rev
A			1.1
Date: Wednesday, February 13, 2008		Sheet	71 of 96

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		Title :	
Engineer:			
Size	Project Name		Rev
A			1.1
Date: Wednesday, February 13, 2008		Sheet	72 of 96

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Title :

Engineer:

Size	Project Name	Rev
A		1.1

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Title :

Engineer:

Size A	Project Name	Rev 1.1
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		Title :	
Engineer:			
Size	Project Name		Rev
A			1.1
Date: <u>Wednesday, February 13, 2008</u>		Sheet	<u>75</u> of <u>96</u>

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		Title :	
Engineer:			
Size	Project Name		Rev
A			1.1
Date: Wednesday, February 13, 2008		Sheet	76 of 96

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		Title :
Engineer:		
Size	Project Name	Rev
A		1.1
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		Title :	
Engineer:			
Size	Project Name		Rev
A			1.1
Date: <u>Wednesday, February 13, 2008</u>		Sheet	<u>78</u> of <u>96</u>

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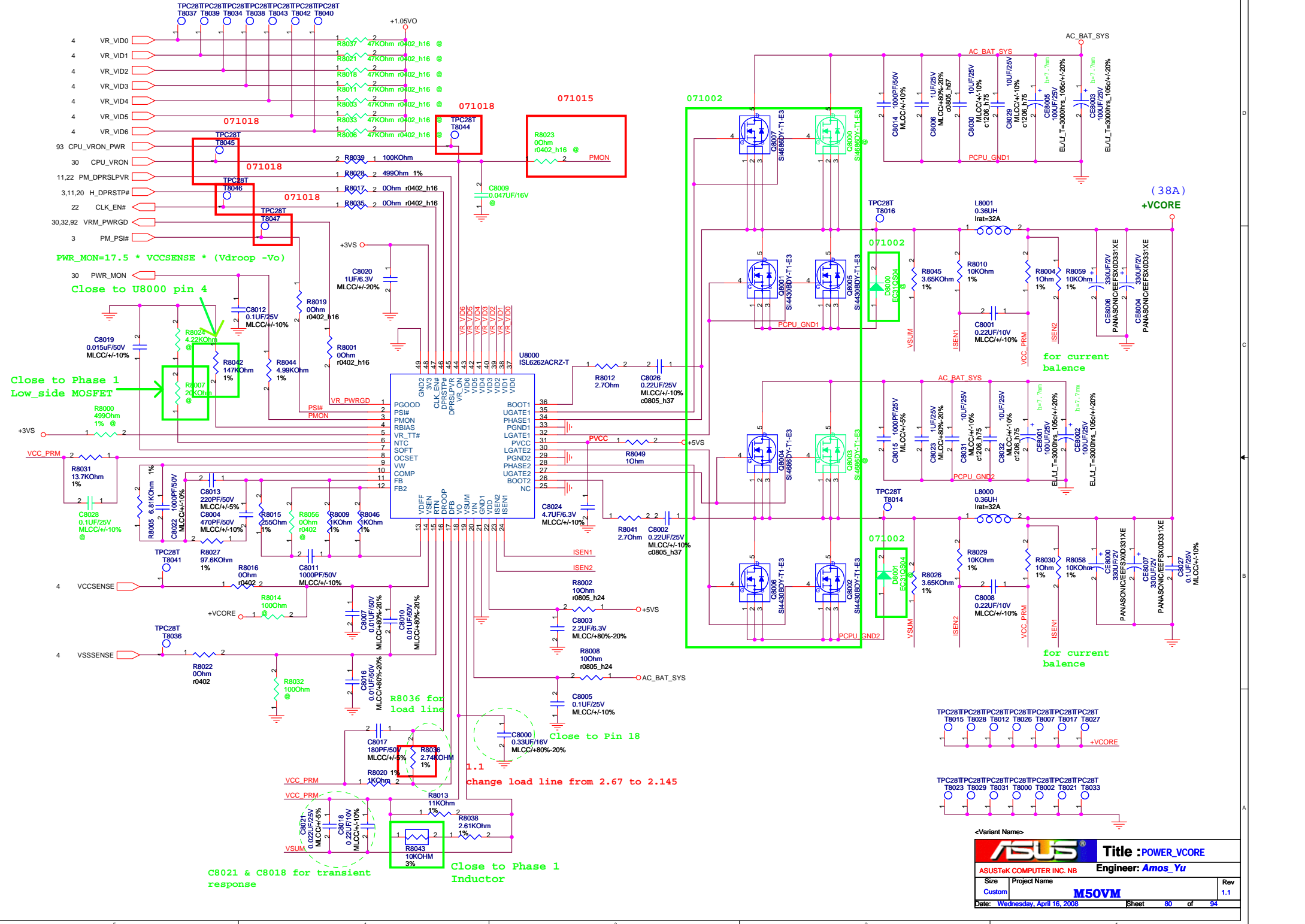
1

History

20070820 R1.01:

1. RTL8111C first release.
2. Remove RTL8111B co-lay circuit.
3. Change the L3404 part-name for the same part reference.

		Title : History
ASUSTeK COMPUTER INC		Engineer:
Size Custom	Project Name	Rev 1.01
Date: Wednesday, February 13, 2008	Sheet 79 of 96	1



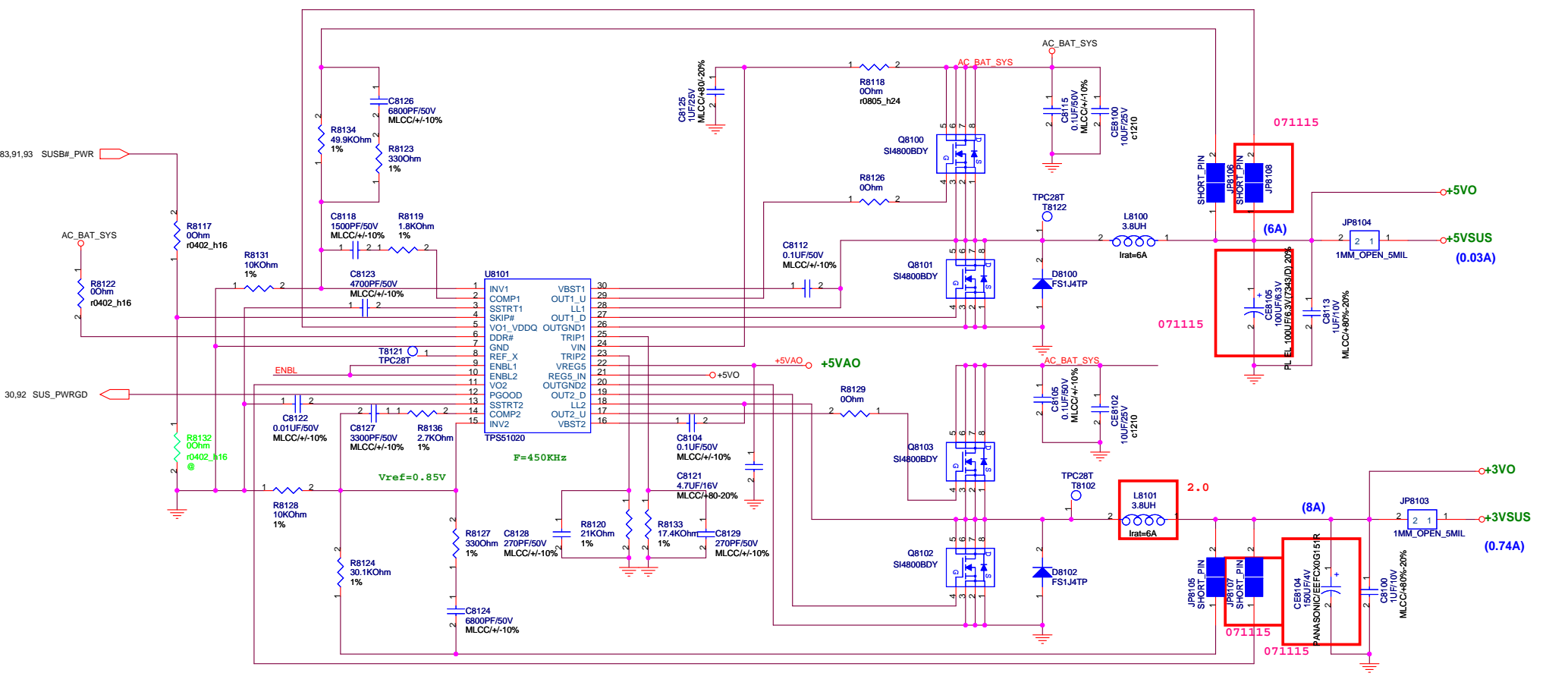
$PWR_MON = 17.5 * VCCSENSE * (Vdroop - V_o)$
 Close to U8000 pin 4

Close to Phase 1 Low_side MOSFET

Close to Pin 18
 change load line from 2.67 to 2.145

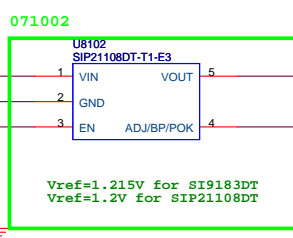
C8021 & C8018 for transient response

Close to Phase 1 Inductor



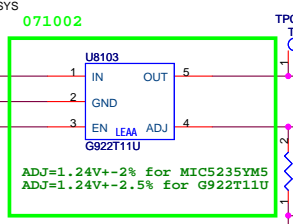
+3VAO

BOM need add second source:
SI9183 (06G007055114)



+12VSUS

BOM need add second source:
MIC5235YM5 (06G007137020)

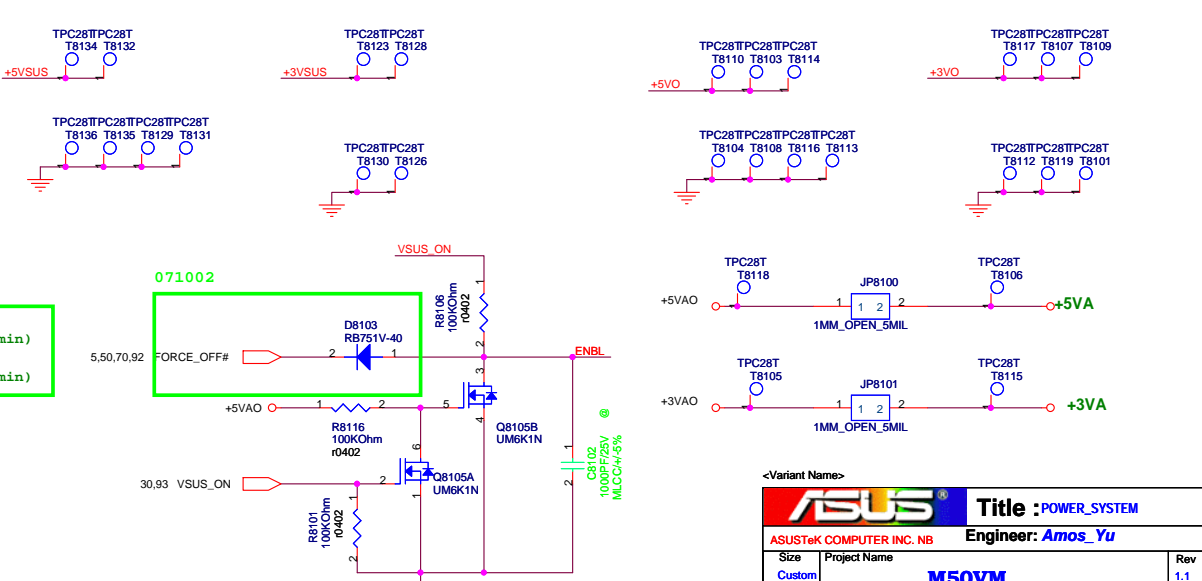


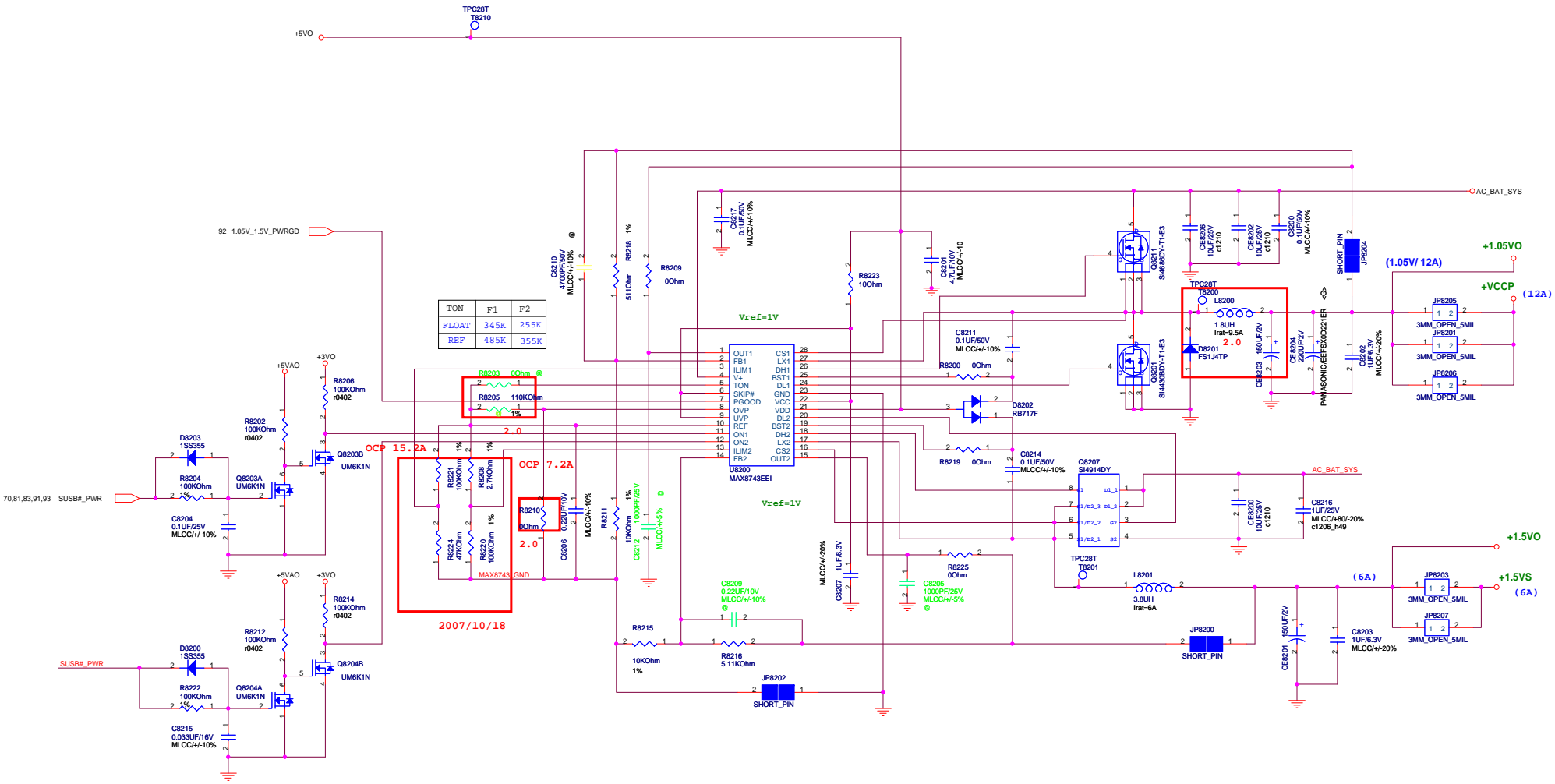
For SI9183DT:
3.329V(TYP), 3.473V(Max), 3.178V(min)

For SIP21108DT:
3.288V(TYP), 3.413V(Max), 3.163V(min)

For MIC5235YM5:
12.235V(TYP), 12.706V(Max), 11.777V(min)

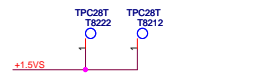
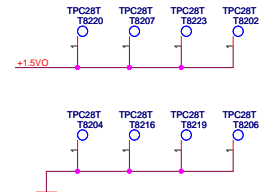
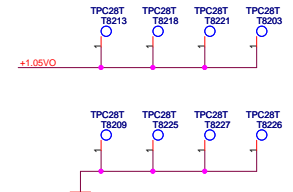
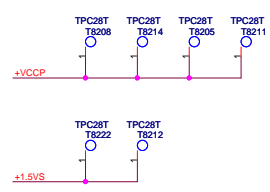
For G922T11U:
12.235V(TYP), 12.768V(Max), 11.717V(min)

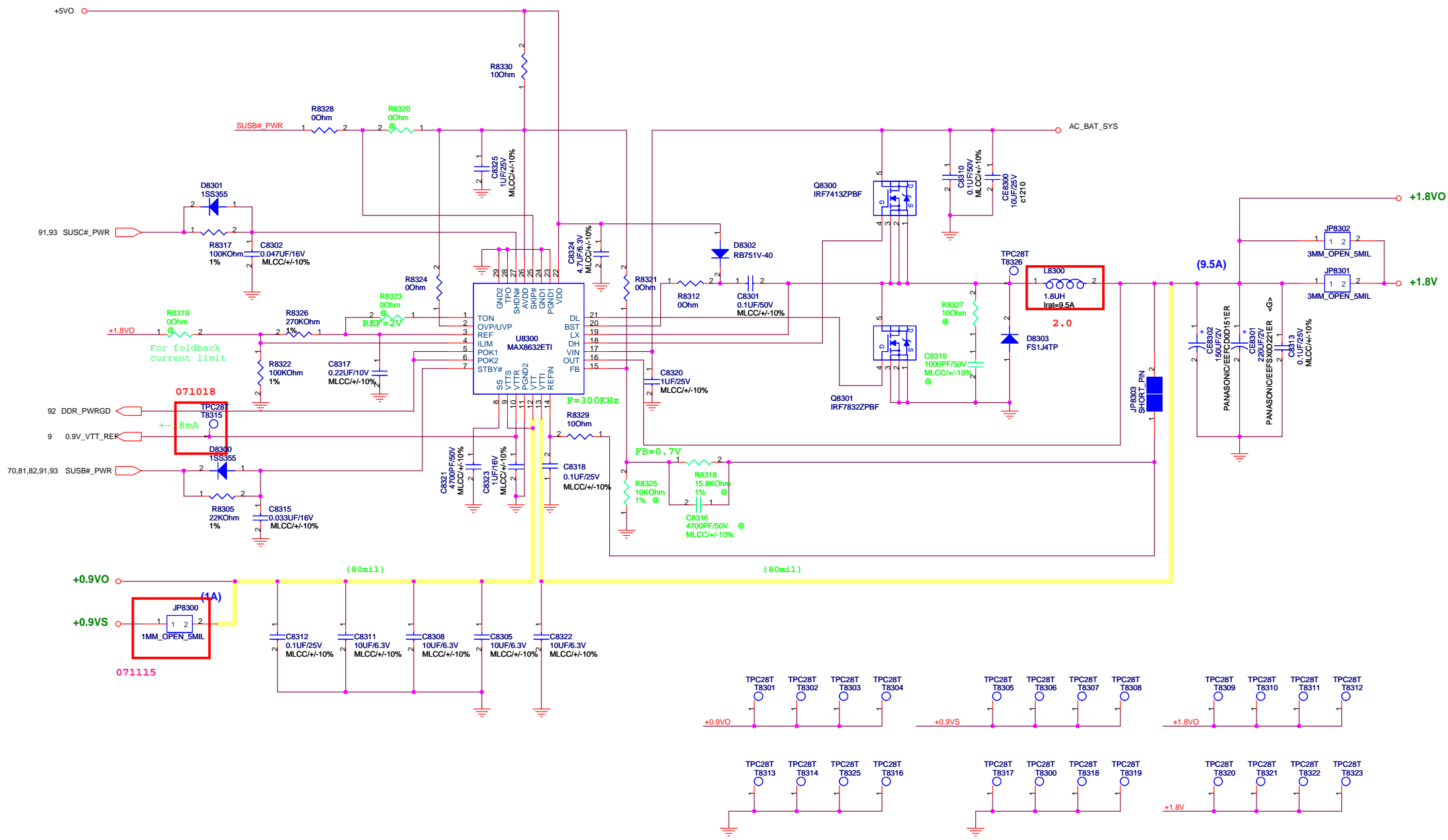




TON	F1	F2
FLOAT	345K	255K
REF	485K	355K

2007/10/18





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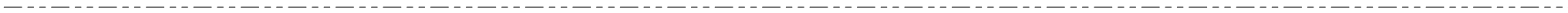
C

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071002

<Variant Name>

		Title : POWER_IC_+2.5VS	
ASUSTeK COMPUTER INC. NB		Engineer: Amos_Yu	
Size	Project Name	Rev	
Custom	M50VM	1.0	
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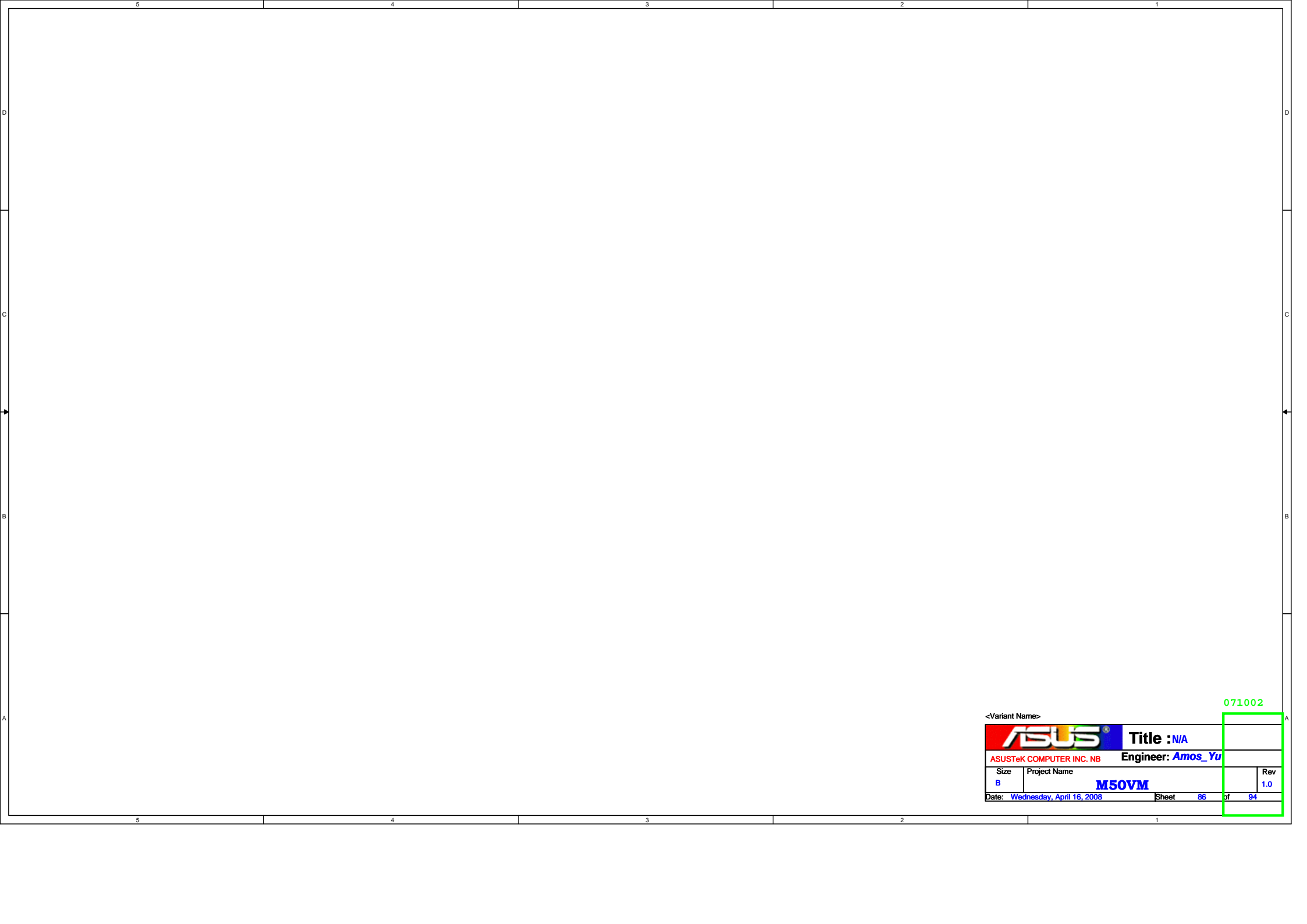
2

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071002


<Variant Name>

		Title : POWER_IO_1.5VS & 1.05VS	
ASUSTeK COMPUTER INC. NB		Engineer: <i>Amos_Yu</i>	
Size	Project Name		Rev
Custom	M50VM		1.0
Date: Wednesday, April 16, 2008		Sheet	85 of 94



071002

<Variant Name>

		Title : N/A	
ASUSTeK COMPUTER INC. NB		Engineer: Amos_Yu	
Size	Project Name		Rev
B	M50VM		1.0
Date: Wednesday, April 16, 2008		Sheet	86 of 94

071002



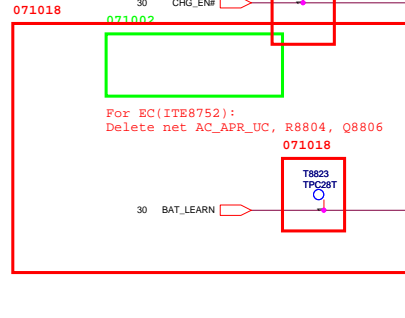
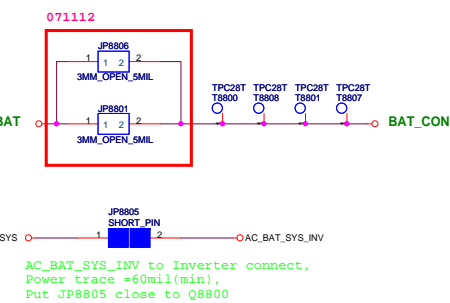
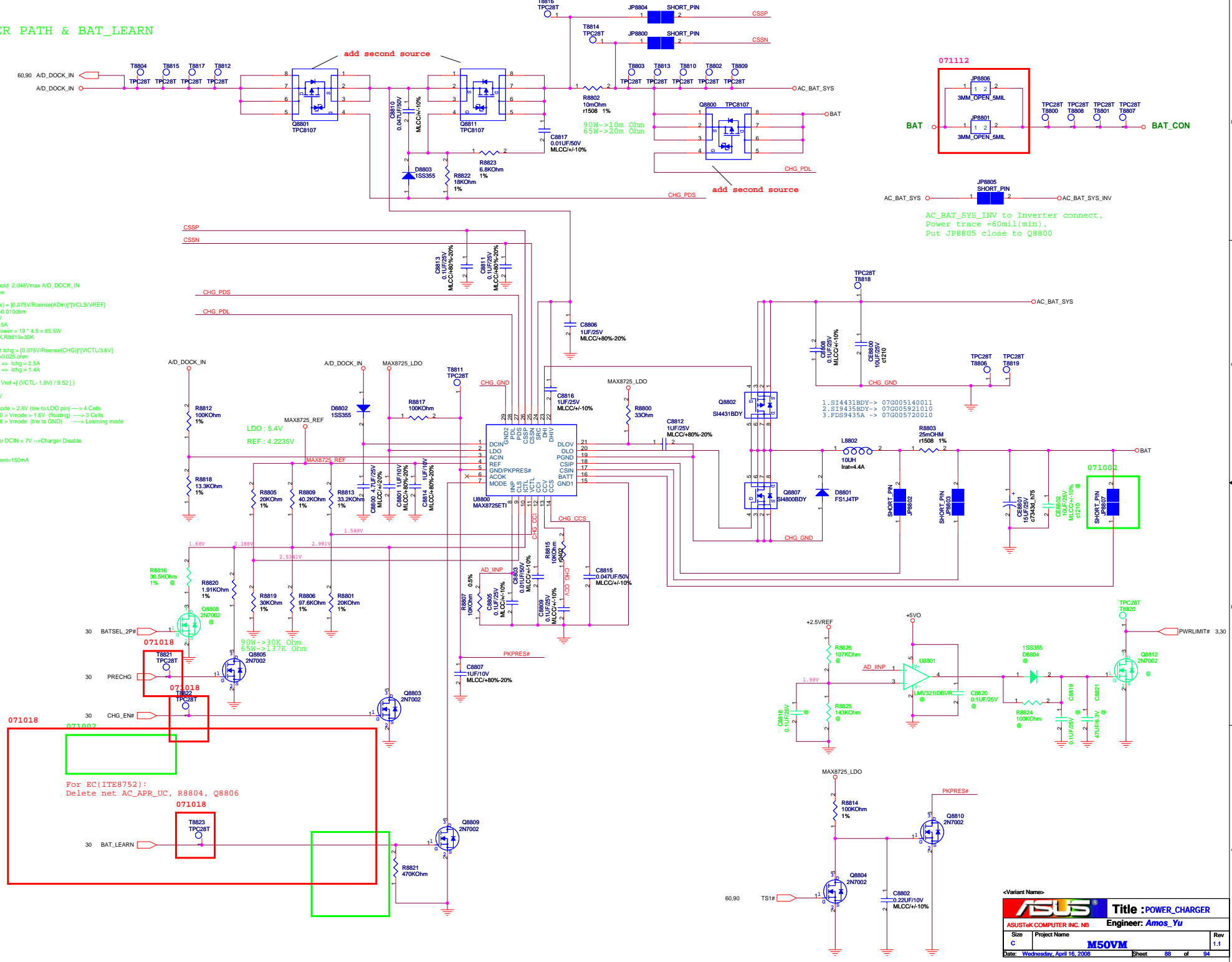
<Variant Name>

071002

		Title : POWER_SHUTDOWN#	
ASUSTeK COMPUTER INC. NB		Engineer: Amos_Yu	
Size Custom	Project Name M50VM	Rev 1.0	
Date: Wednesday, April 16, 2008		Sheet	87 of 94

POWER PATH & BAT_LEARN

AC_IN Threshold 2.048Vmax A/D_DOCK_IN > 17.44V active
 Adapter lin(max) = [0.075V/Rsense(ADin)]*[VCLSL/VREF]
 Rsense(ADin)=0.010ohm
 VCLSL=2.5541V
 => lin(max)=4.5A
 => Constant Power = 19 * 4.5 = 85.5W
 => R8805=20K, R8819=30K
 Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
 Rsense(CHG)=0.025 ohm
 VICTL= 3V => Ichg = 2.5A
 VICTL= 1.68V => Ichg = 1.4A
 Vbatt = Cell * (Vref - (VICTL - 1.8V) / 9.52)
 VCTL= 1.588V
 => Vbatt = 4.2V
 Mode pin : Vmode > 2.8V (tie to LDO pin) -> 4 Cells
 2.0 > Vmode = 1.6V (floating) -> 3 Cells
 0.8 > Vmode (tie to GND) -> Learning mode
 VICTL < 0.8V or DCIN < 7V -> Charger Disable
 Precharge current=150mA



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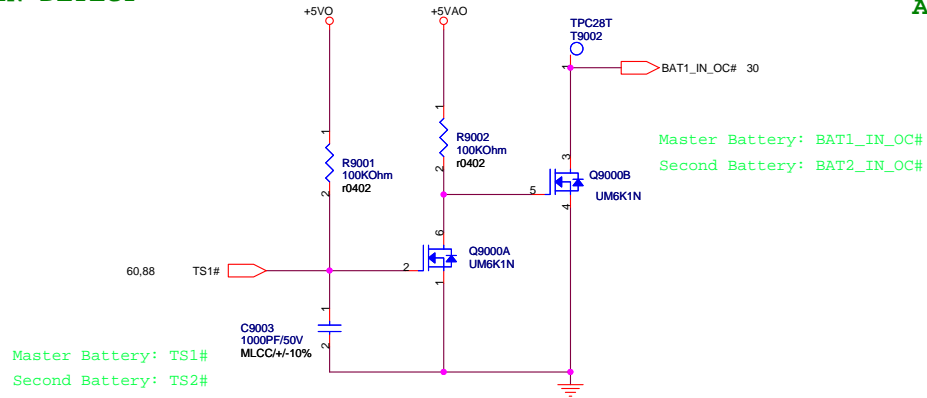
A

071002

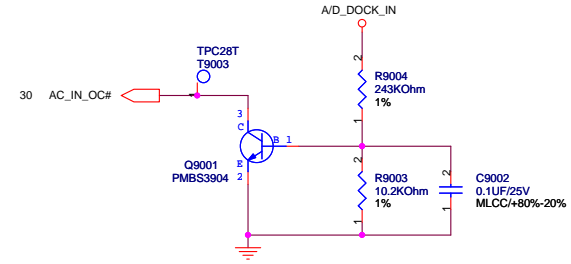
<Variant Name>

		Title : <i>N/A</i>	
ASUSTeK COMPUTER INC. NB		Engineer: <i>Amos_Yu</i>	
Size	Project Name	Rev	
Custom	M50VM	1.0	
Date: Wednesday, April 16, 2008	Sheet	89	of 94

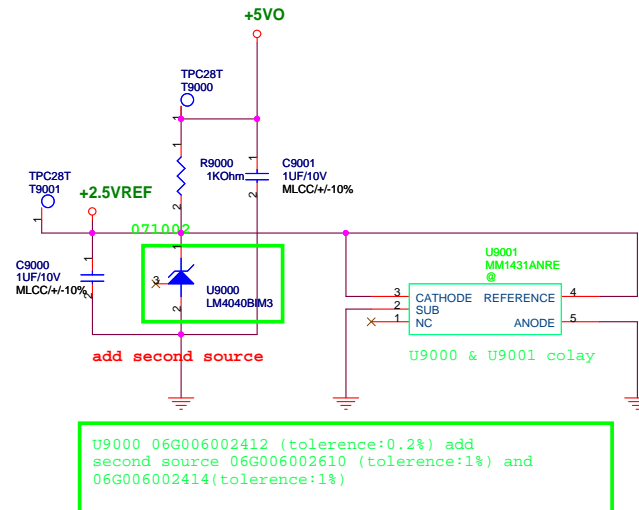
BATTERY IN DETECT



ADAPTER IN DETECT

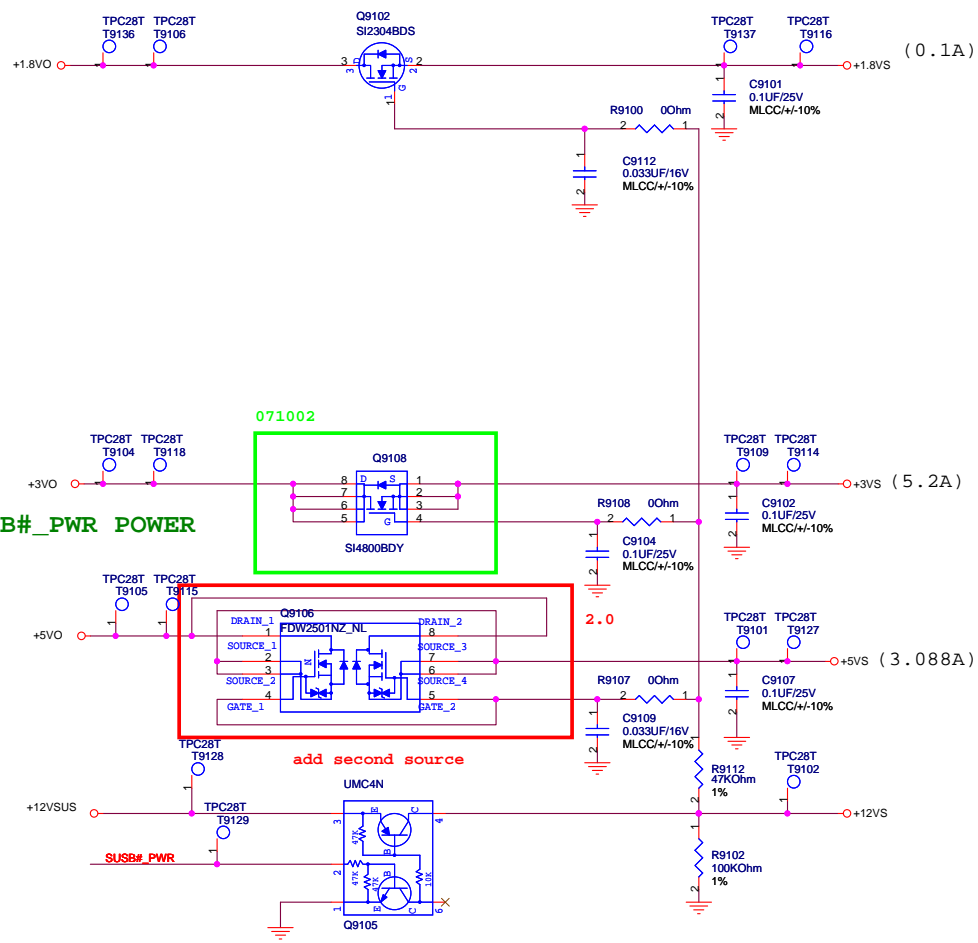


+2.5VREF

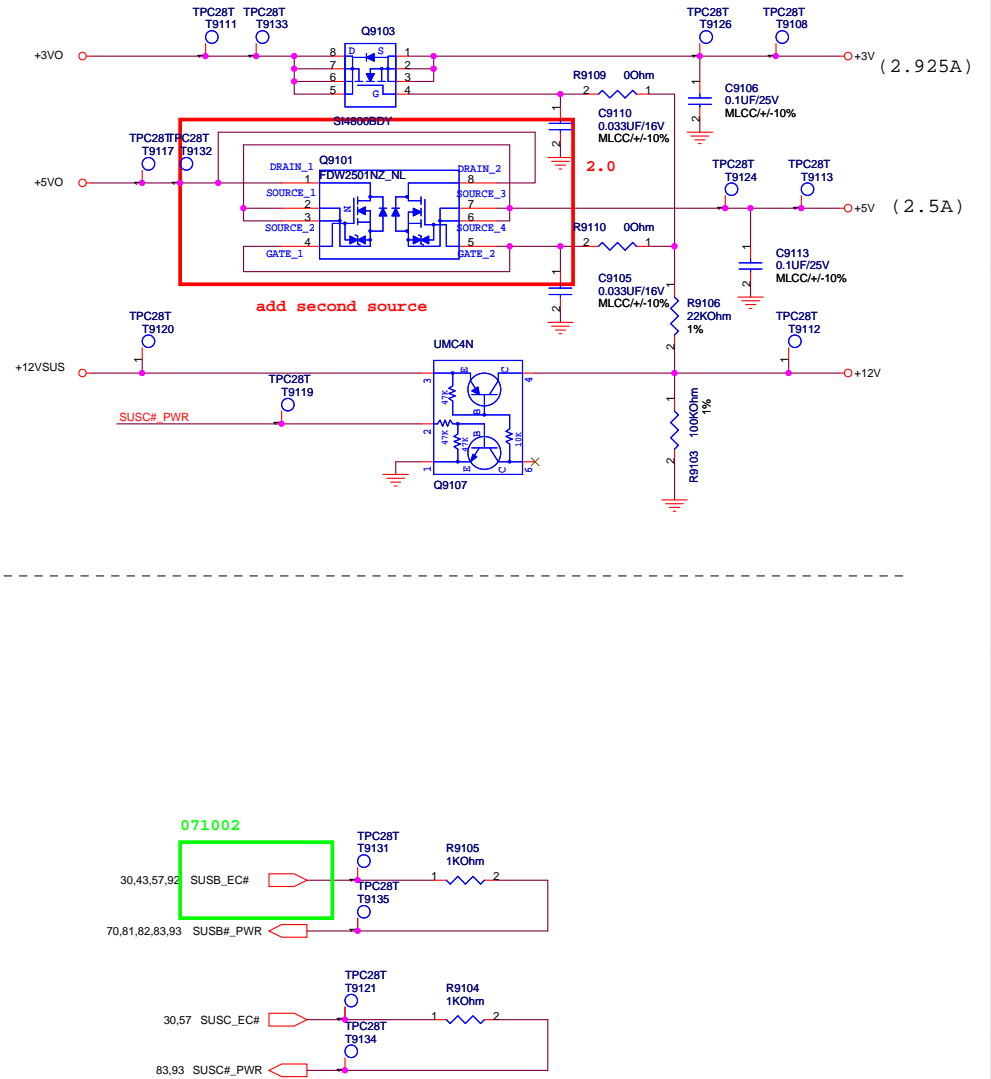


<Variant Name>

		Title :POWER_DETECT	
ASUSTeK COMPUTER INC. NB		Engineer: Amos_Yu	
Size	Project Name	Rev	
Custom	M50VM	1.1	
Date: Wednesday, April 16, 2008	Sheet	90	of 94



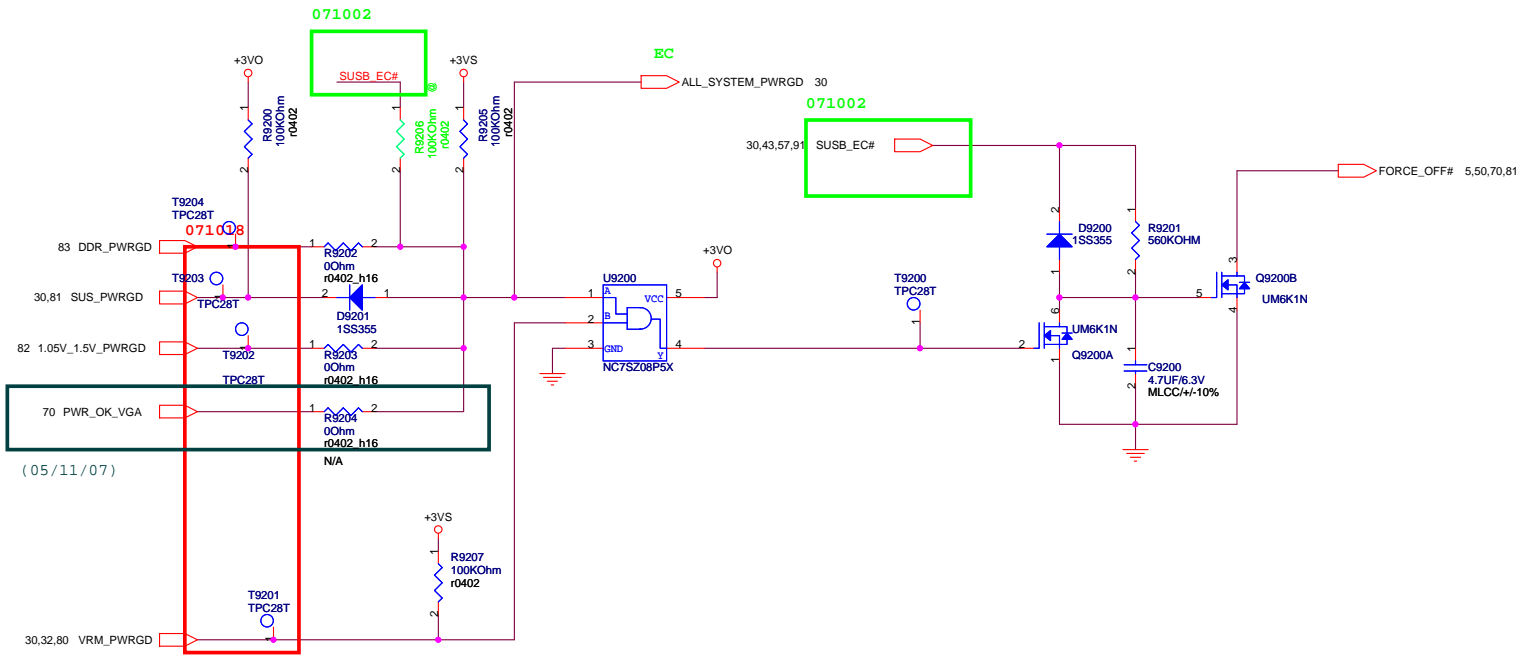
SUSC#_PWR POWER



<Variant Name>

ASUS		Title : POWER_LOAD SWITCH	
ASUSTeK COMPUTER INC. NB		Engineer: Amos_Yu	
Size	Project Name		Rev
Custom	M50VM		1.1
Date: Wednesday, April 16, 2008		Sheet	91 of 94

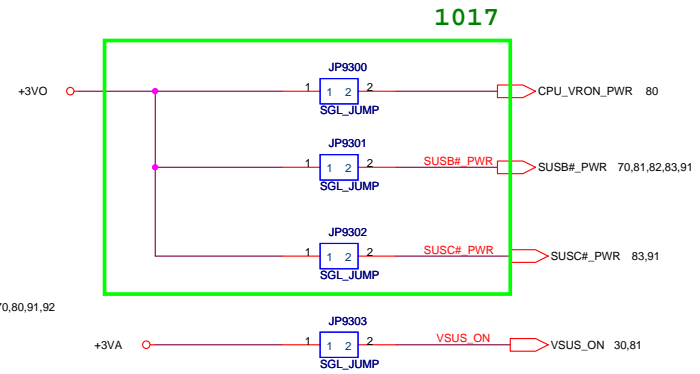
POWER GOOD DETECTOR

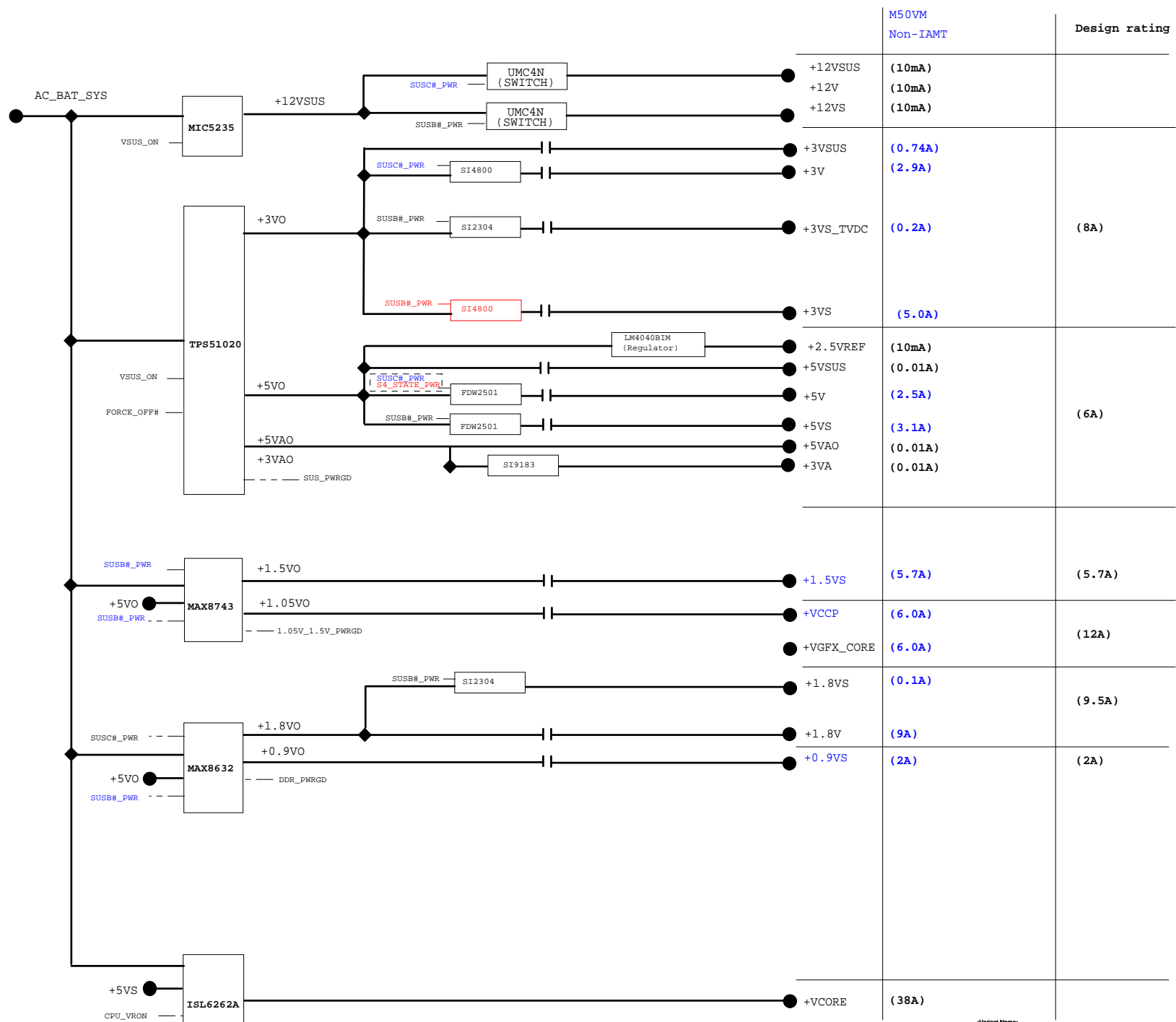


(05/11/07)

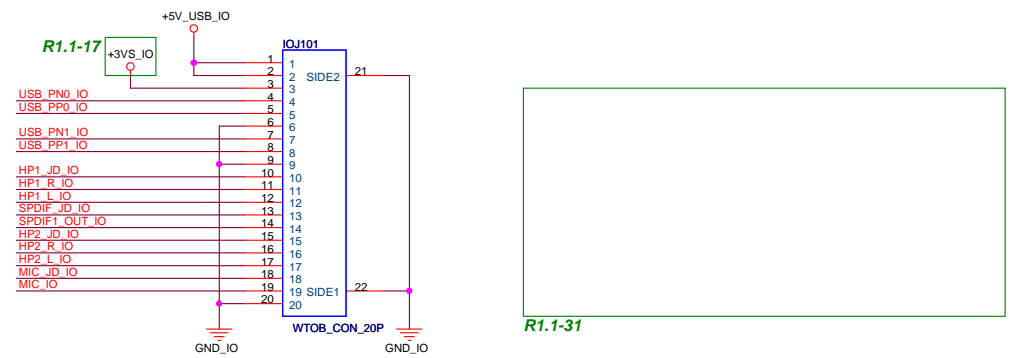
AC_BAT_SYS	AC_BAT_SYS	70,80,81,82,83,88
BAT	BAT	88
BAT_CON	BAT_CON	60,88
+2.5VREF	+2.5VREF	88,90
+3VA	+3VA	20,30,56,57,81
+5VAO	+5VAO	81,82,90
+5VO	+5VO	81,82,83,88,90,91
+5VSUS	+5VSUS	23,31,81
+5V	+5V	36,46,52,56,57,63,65,70,91
+5VS	+5VS	23,31,37,45,48,50,51,56,57,63,80,91
+3VO	+3VO	81,82,91,92
+3VSUS	+3VSUS	20,21,22,23,30,33,37,46,56,70,81
+3V	+3V	21,35,43,53,57,61,64,91
+3VS	+3VS	3,7,8,11,14,15,20,21,22,23,24,25,29,30,32,33,36,37,40,41,42,43,44,45,46,48,50,51,53,56,57,63,64,65,70,80,91,92
+12VSUS	+12VSUS	70,81,91
+12V	+12V	37,91
+12VS	+12VS	24,42,46,70,91
+1.8VO	+1.8VO	83,91
+1.8V	+1.8V	7,8,9,11,13,57,83
+1.8VS	+1.8VS	14,20,38,57,70,91
+0.9VS	+0.9VS	9,57,70,83
+0.9VO	+0.9VO	83
+1.05VO	+1.05VO	80,82
+VCCP	+VCCP	5,10,11,13,14,20,23,29,57,82
+1.5VO	+1.5VO	82
+1.5VS	+1.5VS	4,14,20,23,43,53,57,64,70,82
+VCORE	+VCORE	4,5,80

FOR POWER TEST

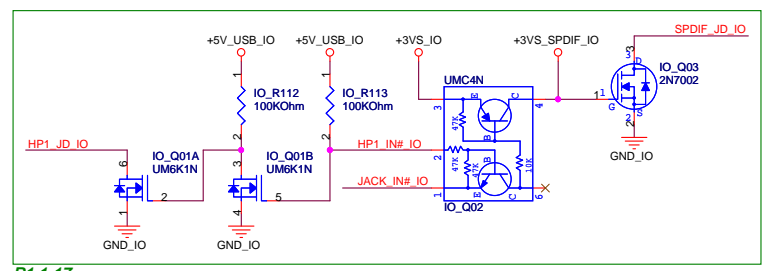
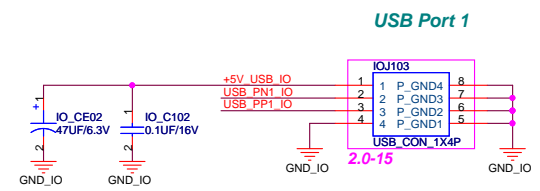
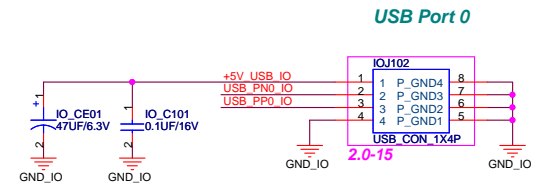




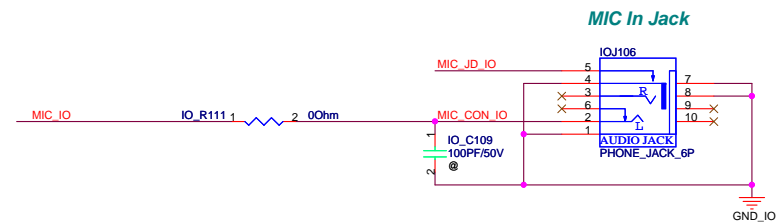
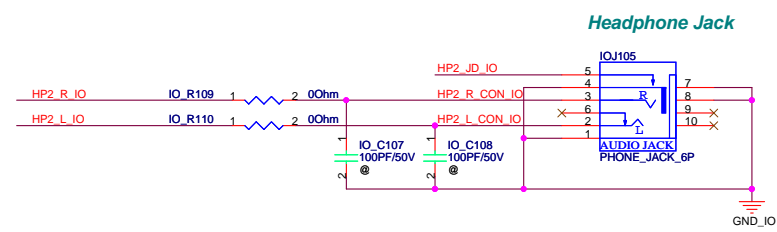
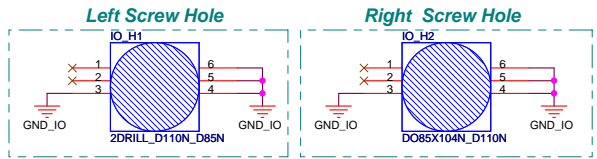
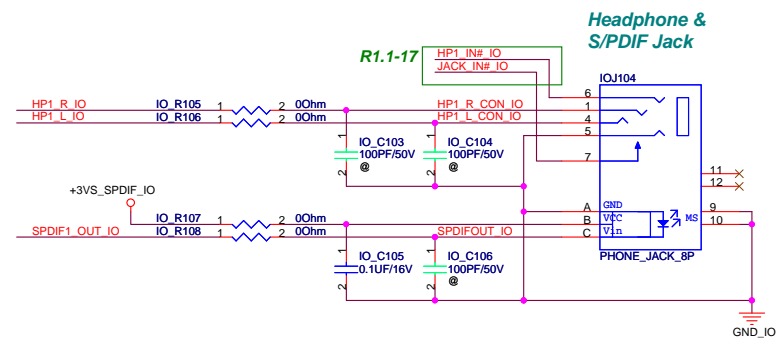
VR_VID0~VR_VID6, B_DPRSTP#,
MCH_OK, PM_DPRSLPR, PW_PSI#,
VCCSENSE, VSSSENSE, STP_CPU#,
PWR_MON



R1.1-31



R1.1-17



Rev	Date	Description
R1.0		First Release!
R1.1 Green Block		<p>** Merge IO board into main board PCB. Page 95.</p> <p>01.Remove VR_VID[6:0] testing series 0 Ohm. Page 4.</p> <p>02.Change 6pcs +VCORE capacitors to No-Stuff for cost down. Page 5.</p> <p>03.Change 3pcs +0.9VS capacitors to No-Stuff for cost down. Page 9.</p> <p>04.Change N1Sv USB port to follow N2Sv, and modify USB_OC#. Page 21,43,45.</p> <p>05.PM Request: Change Bluetooth LED tp E-Mail LED. Page 22,56.</p> <p>06.Follow Intel to change C2304 to 1uF/16V(XR). Page 23.</p> <p>07.Follow R1E to change R2904 to 270ohm. Page 29.</p> <p>08.Follow IT8752/8512 EC Common Hardware Pin Assignment v0.005, change GPE7 to INSTANT_ON# and GPG0 to PM_THERM#. Page 30.</p> <p>09.PM REquest: Remove USB port charger function. Page 30,65.</p> <p>10.PM change WWAN LED to touch-pad lock LED. Page 30,56.</p> <p>11.Change IR to 36KHz to meet Vista remote control Min. range requirement. Page 31.</p> <p>12.Remove testing 2nd CIR design. Page 31.</p> <p>13.Change X3301 to 49S type for cost down. Page 33.</p> <p>14.LAN chip version change. Page 33.</p> <p>15.Audio codec chip change version. Page 36.</p> <p>16.N1Sv/X55 will not supprot 3G function. Page 36,67.</p> <p>17.Add S/PDIF & HDMI jack detect by Realtek sugesstion. Page 36,65,70,95.</p> <p>18.Modify audio de-pop circuit. Page 36,37.</p> <p>19.Modify LVDS power sequence failed bug. Page 45.</p> <p>20.Modify LCD abnormal display bug due to LVDS pair mismatch. Page 45,70.</p> <p>21.Remove HDTV support function. Page 47,70.</p> <p>22.Remove HDMI EMI filter design. Page 48.</p> <p>23.X55 need two pwer LEDs. Page 56.</p> <p>24.PM change WLAN LED to RF LED. Page 56,63.</p> <p>25.Bluetooth pin define error. Page 61.</p> <p>26.Remove co-layout sequence logic control circuit. Page 68.</p> <p>27.ME change parts: J3401,J5102,J6002,J6501. Page 34,51,60,65.</p> <p>28.EMI modification. Page 34,36,65.</p> <p>29.Crystal accuracy fine-tune. Page</p> <p>30.USB droop test fail. Page 65.</p> <p>31.Remove IO board USB common choke design. Page 95.</p> <p>32.Speaker fine-tune. Page 37.</p> <p>33.Cost down for 4-wire PWM fan. Page 50.</p> <p>34.Cost down: Change RB717F to BAT54AW. Page 37,45,48,56.</p>
R2.0 Pink Block		<p>01.Change +1.25VS_MPLL, +1.25VS_PEGPLL & +1.8V_SM_CK PLL design. Page 15.</p> <p>02.Add CMOS crack protection circuit. Page 22.</p> <p>03.Reserve C2337 (10UF/16V) for +5VREF_1CH. Page 23.</p> <p>04.With EMI RD's confirmation, remove reserved LAN common choke circuit. Page 34.</p> <p>05.With EMI RD's confirmation, change R3612, R3614, R3615, R3616, R3622, R3624,R3626 to short-pad. Page 36.</p> <p>06.With EMI RD's confirmation, remove reserved 1394 common choke circuit. Page 41.</p> <p>07.With EMI RD's confirmation, remove reserved NewCard USB common choke circuit. Page 43.</p> <p>08.Add NewCard debug card co-layout circuit. Page 44.</p> <p>09.EMI modification: change reserved common choke circuit from USB port to internal camera port. Page 45.</p> <p>10.HDMI jack detection modification. Page 48,70.</p> <p>11.Change FAN capacitors to 10UF. Page 50.</p> <p>12.Modify X55 power LED design. Page 56.</p>

Rev	Date	Description
		<p>13.With EMI RD's confirmation, remove reserved e-SATA/USB combo port USB common choke circuit. Page 41.</p> <p>14.Reserve R8023 for shortage issue of ISL6262A. Page 80.</p> <p>15.QTR USB plug test failed, change USB connector. Page 95.</p>