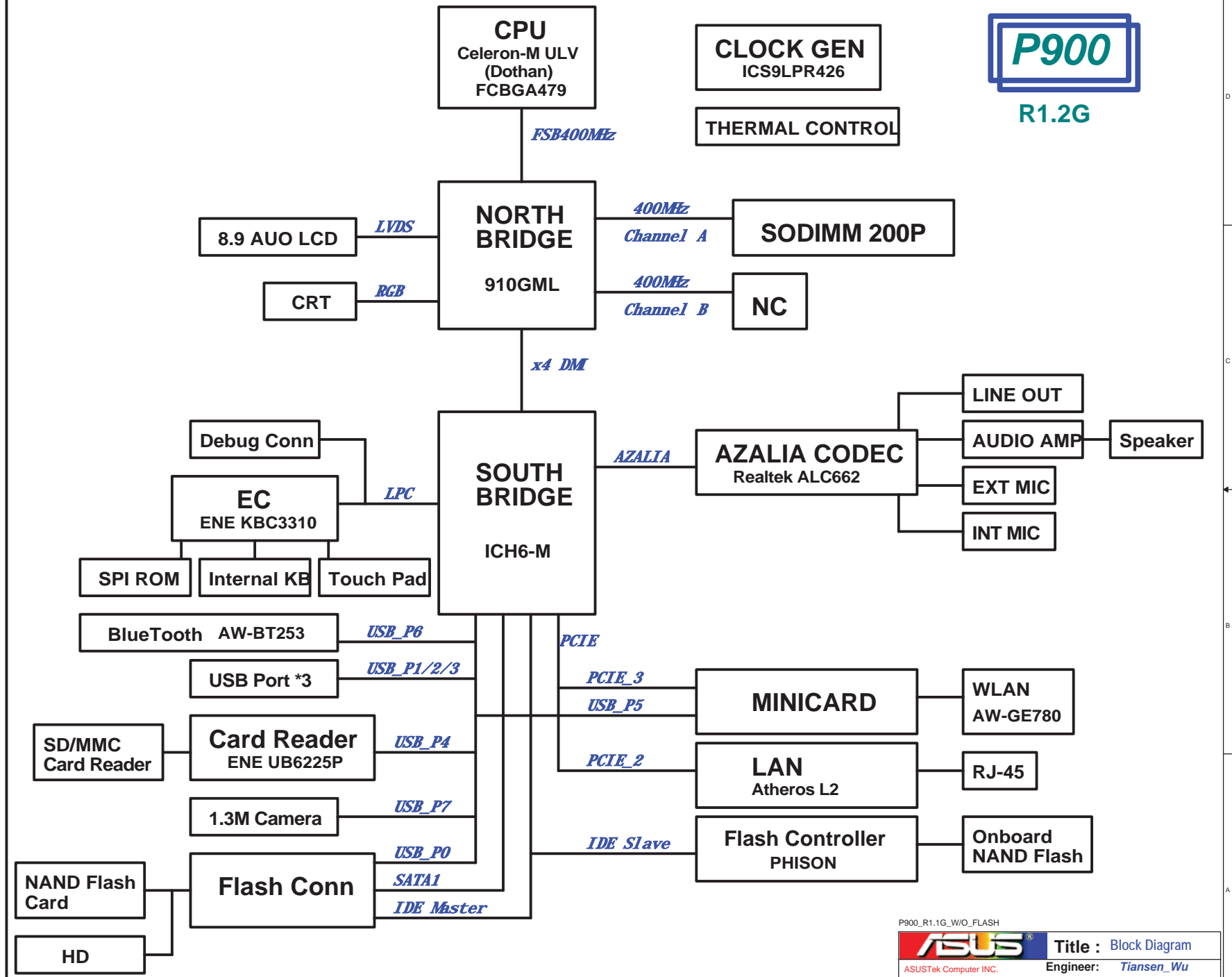


- 01_Block Diagram
- 02_System Setting
- 03_Power Sequence
- 04_EC Pin Define
- 05_History
- 06_*
- 07_Clock Gen_ICS9LPR426
- 08_Dothan_HOST
- 09_Dothan_PWR_GND
- 10_910GML_HOST_DMI
- 11_910GML_DRAM
- 12_910GML_VGA_LVDS_TV
- 13_910GML_PWR
- 14_910GML_GND
- 15_ICH6-M_Azalia_GPIO_PCI_LAN
- 16_ICH6-M_USB_PCIE_DMI_IDE_SATA
- 17_ICH6-M_PWR_GND
- 18_DDR2_SODIMM
- 19_DDR2_Termination
- 20_Onboard_VGA
- 21_LCD Conn
- 22_Minicard
- 23_LAN_Atheros L2
- 24_RJ45/BlueTooth
- 25_Onboard Flash
- 26_Flash Conn
- 27_USB Port
- 28_Card Reader_ENE UB6225P
- 29_Camera Conn
- 30_Codec_ALC662
- 31_Audio_AMP_Jack
- 32_EC_ENE KB3310
- 33_Switch_SPI ROM_Debug Conn
- 34_KB_Touch Pad
- 35_Thermal Sensor_FAN
- 36_LED_THERMTRIP
- 37_Discharge
- 38_PWR Jack
- 39_Srew Hole
- 40_EMI
- 41_POWER FLOW
- 42_CHARGER
- 43_VCORE(7A)
- 44_POWER_3V_5V_VTT_DDR
- 45_POWER_3VA_3VSB
- 46_POWER_1.05V_1.5V_2.5V
- 47_POWER_1.8V_DUAL_5VSB



P900_R1.1G_WO_FLASH		Title : Block Diagram	
ASUS		Engineer: Tiansen_Wu	
Size	Project Name	Rev	
A3	P900	1.2G	
Date: Wednesday, February 27, 2008	Sheet	1	of 47

ICH6 GPIO SETTING

Pin	Pin Name	Connect to	Type	Input/Output Set
B7	GPI0/REQ6#	10K Pull +3V	I	fixed as Input only
E8	GPI1 / REQ5#	10K Pull +3V	I	fixed as Input only
D9	GPI2 / PIRQE#	10K Pull +3V	I	fixed as Input only
C7	GPI3 / PIRQF#	10K Pull +3V	I	fixed as Input only
C6	GPI4 / PIRQG#	10K Pull +3V	I	fixed as Input only
M3	GPI5 / PIRQH#	10K Pull +3V	I	fixed as Input only
AD19	GPI6 / BMBUSY#	NB BMBUSY#	I	Input
AE19	GPI7	NC	GPI	fixed as Input only
R1	GPI8	EC KBC_SCI#	GPI	fixed as Input only
C23	GPI9/OC4#	10K Pull +3V	I	Input
D23	GPI10/OC5#	10K Pull +3V	I	Input
W6	GPI11 / SMBALERT#	S_SMBALERT#	I	Input
M2	GPI12	NC	GPI	fixed as Input only
R6	GPI13	EC EXTSMI#	GPI	fixed as Input only
C25	GPI14/OC6#	10K Pull +3V	I	Input
C24	GPI15 /OC7#	10K Pull +3V	I	Input
D8	GPO16/GTN6#	NC	O	Output
F6	GPO17 / GNT5#	NC	O	Output
AC21	GPO18 / STP_PC#	Clock GEN STP_PC#	O	Output
AB21	GPO19	WLAN_LED#	GPO	fixed as Output only
AD22	GPO20 / STP_CPU#	STP_CPU#	O	Output
AD20	GPO21	CAMERA_EN	GPO	fixed as Output only
NA	GPI022	NC	NA	NA
AD21	GPO23	SPEAKER_EN#	GPO	fixed as Output only
V3	GPI024	MINICARD_EN#	I/O	Output
P5	GPI025	WLAN_ON#	I/O	Output

Pin	Pin Name	Connect to	Type	Input/Output Set
AF17	GPI26/SATA0GP	NC	GPI	(GPI)Input
R3	GPI027	CARD_READER_EN#	I/O	Output
T3	GPI028	NC	I/O	Output
AE18	GPI29 / SATA1GP	PCBVER0	GPI	(GPI)Input
AF18	GPI30 / SATA2GP	NC	GPI	(GPI)Input
AG18	GPI31 / SATA3GP	PCBVER1	GPI	(GPI)Input
AF19	GPI032 / CLKRUN#	10K Pull +3V	I/O	Input
AF20	GPI033	PM_VCOREL1	I/O	Output
AC18	GPI034	PM_VCOREL2	I/O	Output
NA	GPI035	NA	NA	NA
NA	GPI036	NA	NA	NA
NA	GPI037	NA	NA	NA
NA	GPI038	NA	NA	NA
NA	GPI039	NA	NA	NA
F7	GPI40 / REQ4#	10K Pull +3V	I	Input
P4	GPI41 / LDRQ1#	NC	I	Input
NA	GPI042	NA	NA	NA
NA	GPI043	NA	NA	NA
NA	GPI044	NA	NA	NA
NA	GPI045	NA	NA	NA
NA	GPI046	NA	NA	NA
NA	GPI047	NA	NA	NA
E7	GPO48 / GNT4#	NC	O	Output
AC25	GPO49 / CPUPWRGD	CPU Power Ok	O	Output

P900_R1.1G_WO_FLASH

		Title : System Setting	
ASUSTek Computer INC.		Engineer: <i>Tiansen_Wu</i>	
Size	Project Name		Rev
A3	P900		1.2G
Date: Wednesday, February 27, 2008		Sheet	2 of 47

EC KB3310 GPIO SETTING

Pin No.	Pin Name	Signal Name	Type	NOTE
1	GA20	A20GATE	O	A20GATE
2	KBRST#	RC_IN#	O	KBRST#
6	GPIO04	EMAIL_SW#	I	EMAIL_SW#, *
13	PCIRST#	PCI_RST#	I	PCI Reset
14	GPIO07	BAT_EXT	O	Reserved
15	GPIO08	EXTSMH#	O	EXTSMH#, 10K Pull +3VSUS
16	GPIO0A	LID_EC#	I	LID_EC#, *
17	GPIO0B	NC	O	LCD chip select
18	GPIO0C	NC	I/O	LCD Data
19	GPIO0D	DISTP_SW#	I	Touch Pad Disabled, *
20	SC#	KBC_SC#	O	KBC_SC#, 10K Pull +3VSUS
21	PWM1	BL_PWM_DA	O	LCD Light Switch
23	PWM2	BAT_CRITICAL	O	LCD clock
25	GPIO11	PM_PWRBTN#	OD	Power Button to SB, *
26	FANPWM1	FAN0_PWM	O	CPU Fan(Unused)
27	FANPWM2	FAN1_PWM	O	VGA Fan(Unused)
28	FANFB1	FAN0_TACH	I	CPU FanTach(Unused)
29	FANFB2	FAN1_TACH	I	VGA FanTach(Unused)
30	GPIO16	E51_TX	O	RS232 debug port
31	GPIO17	E51_RX	O	Reserved
32	GPIO18	PWR_SW#	I	power button, *
34	GPIO19	MAIL_LED#	O	Mail LED(Unused)
36	GPIO1A	NUM_LED#	O	EC H/W controls(Unused)
38	CLKRUN#	N.C	O	Reserved
39	KSO0	KSO0	O	For Keyboard interface
40	KSO1	KSO1	O	For Keyboard interface
41	KSO2	KSO2	O	For Keyboard interface
42	KSO3	KSO3	O	For Keyboard interface
43	KSO4	KSO4	O	For Keyboard interface
44	KSO5	KSO5	O	For Keyboard interface
45	KSO6	KSO6	O	For Keyboard interface
46	KSO7	KSO7	O	For Keyboard interface
47	KSO8	KSO8	O	For Keyboard interface
48	KSO9	KSO9	O	For Keyboard interface
49	KSO10	KSO10	O	For Keyboard interface
50	KSO11	KSO11	O	For Keyboard interface
51	KSO12	KSO12	O	For Keyboard interface
52	KSO13	KSO13	O	For Keyboard interface
53	KSO14	KSO14	O	For Keyboard interface
54	KSO15	KSO15	O	For Keyboard interface
55	KSI0	KSI0	I	For Keyboard interface
56	KSI1	KSI1	I	For Keyboard interface
57	KSI2	KSI2	I	For Keyboard interface
58	KSI3	KSI3	I	For Keyboard interface
59	KSI4	KSI4	I	For Keyboard interface
60	KSI5	KSI5	I	For Keyboard interface
61	KSI6	KSI6	I	For Keyboard interface
62	KSI7	KSI7	I	For Keyboard interface
63	AD0	BAT_ICHG	I	Sense Power Loading
64	AD1	BAT_CONFIG	I	sense Battery
65	AD2	BAT_SENT	I	Reserved
66	AD3	BAT_TS	I	Reserved
68	GPO3C	DOC	O	Trigger Clock Gen

Pin No.	Pin Name	Signal Name	Type	NOTE
70	GPO3D	LCD_BACKOFF#	O	LCD_BACKOFF#
71	GPO3E	CLK_PWRSERVE#	O	Active when BAT_IN=1 and AC_OK=0(Unused)
72	GPO3F	PM_BATLOW#	O	Battery Low Low
73	GPIO40	AC_OK	I	AC Adaptor Plug in
74	GPIO41	PM_RSMRST#	O	10K Pull GND
75	GPIO42	N.C	O	Reserved
76	GPIO43	N.C	O	Reserved
77	SCL1	SMB1_CLK	I/OD	4.7K Pull +3VA_EC
78	SDA1	SMB1_DAT	I/OD	4.7K Pull +3VA_EC
79	SCL2	SMB2_CLK	I/OD	10K Pull +3VS
80	SDA2	SMB2_DAT	I/OD	10K Pull +3VS
81	KSO16	N.C	O	Reserved
82	KSO17	N.C	O	Reserved
83	PSCLK1	LCD_SCL	O	Reserved
84	PSDAT1	LCD_SDA	O	Reserved
85	PSCLK2	LCD_CSB	O	Reserved
86	PSDAT2	LCD_VSYNC	O	Reserved
87	PSCLK3	TP_CLK	I/OD	10K Pull +3VS
88	PSDAT3	TP_DAT	I/OD	10K Pull +3VS
89	GPIO50	BATSEL_3S	O	Battery series. Hi:3S, Lo:4S(Unused)
90	GPIO52	CHG_LED_UP#	O	charger LED
91	GPIO53	CAP_LED#	O	EC H/W controls
92	GPIO54	PWR_LED_UP	O	EC H/W blinking
93	GPIO55	SCRL_LED#	O	EC H/W controls
95	GPIO56	PWR4G_SW#	I	*
97	GPXOA00	SPI_MODE#	O	*HW Strap for SPI Flash deExternal Pull Down 100K ohm to GND*
98	GPXOA01	SUSC_ON	O	
99	GPXOA02	VSUS_ON	O	
100	GPXOA03	CPU_VRON	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	PWROK	O	
103	GPXOA06	PM_LEVELDOWN#	O	Reserved
104	GPXOA07	CHG_EN#	O	Battery charging enabled
105	GPXOA08	PRECHG	O	
106	GPXOA09	SPI_WP#	O	
107	GPXOA10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	
109	GPXID0	BATSEL_2P#	O	Battery parallel. Hi:1P, Lo:2P-3P
110	GPXID1	CPU_LEVELDOWN#	O	Reserved
112	GPXID2	THRO_CPU	O	Active if Battery Temperature is over spec
114	GPXID3	SUSB#	I	Pull Down 100K ohm to GND
115	GPXID4	SUSC#	I	Pull Down 100K ohm to GND
116	GPXID5	CPUPWR_GD	I	10K Pull +3VS
117	GPXID6	VSUS_GD	I	Disabled **
118	GPXID7	BAT_VOLSEL	O	Reserved
121	GPIO57	INTERNET#	I	*
126	SPICLK	SPI_CLK	O	SPI Clock
127	GPIO59	N.C	O	Reserved

EC KB3310 Other Pin SETTING

Pin No.	Pin Name	Signal Name	Type	NOTE
3	SERIRQ	INT_SERIRQ	I/OD	8.2K Pull +3VS
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA_EC	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCJ_EC	I	
22	VCC	+3VA_EC	P	
24	GND	GND	P	
33	VCC	+3VA_EC	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	Add 100K ohm to GND
67	AVCC	+3VACC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA_EC	P	
111	VCC	+3VA_EC	P	
113	GND	GND	P	
119	RD#	SPI_SO	I	
120	WR#	SPI_SI	O	
112	XCLKI	32KXCLKI	I	
123	XCLKO	32KXCLKO	O	
124	V18R	K_V18R		Reserved 1uF to GND
125	VCC	+3VA_EC	P	
128	SPICS#	SPI_CE#	O	

P900_R1.1G_WO_FLASH

		Title : EC Pin Define	
ASUSTek Computer INC.		Engineer: Tiansen_Wu	
Size	Project Name	Rev	
A3	P900	1.2G	
Date: Wednesday, February 27, 2008		Sheet	4 of 47

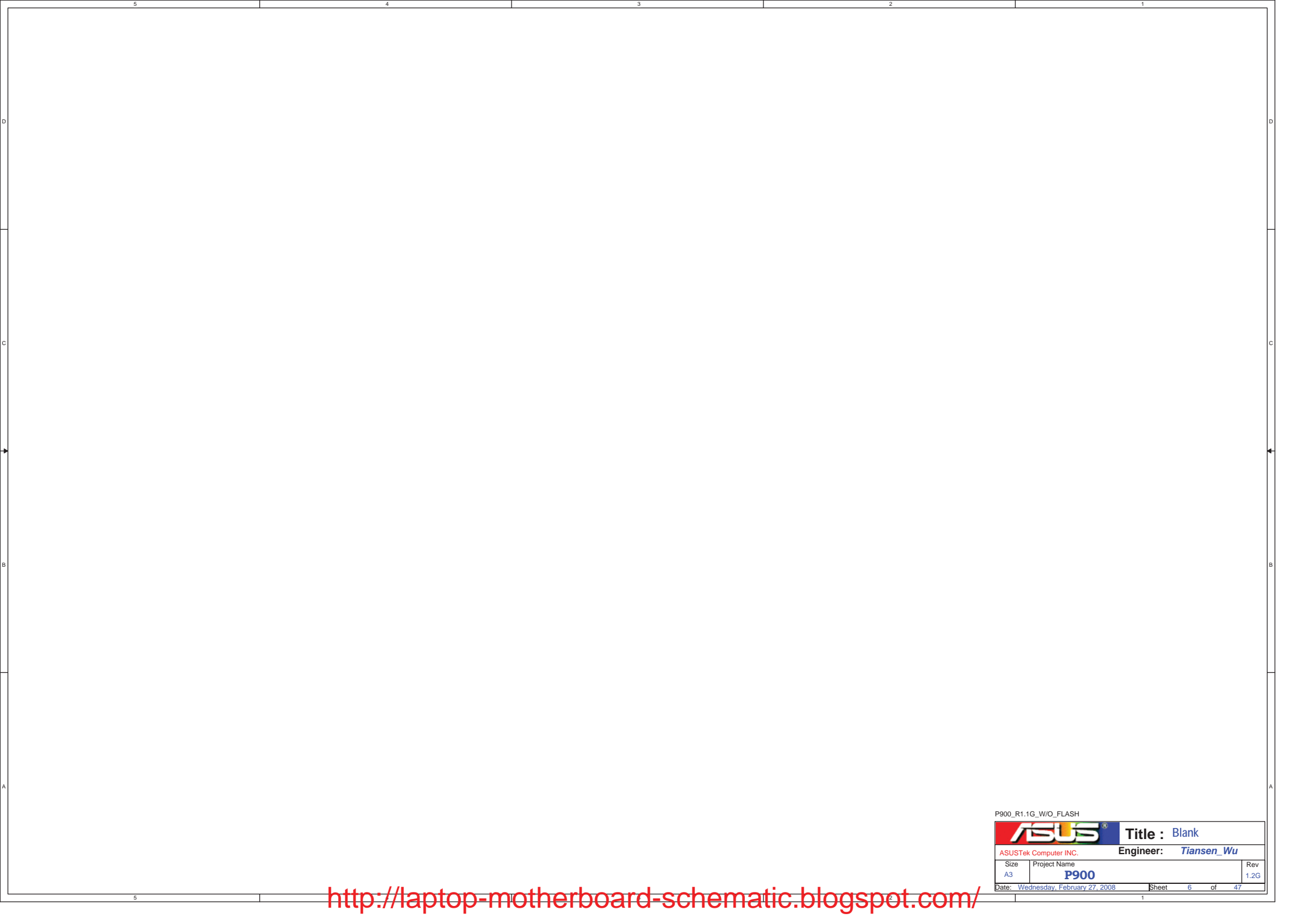
P701 CIRCUIT UPDATED HISTORY

Rev	Date	Description
1.0G	2007/02/26 }	S701L Schematic 1.0G Beginning
	2007/03/16 }	S701L 1.0G Gerber Out
1.1G	2007/03/24 }	S701L Schematic 1.1G Beginning
	2007/04/19 }	S701L 1.1G Gerber Out
1.0G	2007/04/24 }	P701(S701L renamed) Schematic 1.0G Beginning 1. PC8054, PR6075 /X to N/A 2. Attansic L2 change to Atheros L2(pin to pin) 3. LC1, LC33 /CAP/X to N/A 4. C87 change to X5R to cost down 5. L1, L2, L3 change to 56 NH, R5, R6 change to 75 Ohm to pass CRT EA measure 6. PR48 change to 22K Ohm, PC35 change to 4700PF to fix no VCORE issue 7. PR6074 change to 4.7K Ohm to fix +3VSB OCP issue 8. Clock Gen CY28442-2 change to ICS9LPR367 9. Phase in Power Level Reduce solution, mark "Taipei0508" 10. Card Reader Socket change to SD Socket 12G25100091E 11. Add System FAN circuit 12. Camera change to USB port 7, Minicard change to USB port 5 13. Use SB GPIO27 to Enable/Disable Card Reader UB6225P 14. Use SB GPIO28 to Enable/Disable Modem 15. Card Reader UB6225P share 48M clock from CLock Gen with SB USB part 16. Add D29 to fix LCD_CSB leakage current issue 17. LC29, LC30 change to 27PF to pass EA crystal measure 18. Change vaule of PR73, PR74, PC56 and add PC60 to adjust the power sequence timing between Stand By power and RSMRST# 19. Remove USB port 1 20. Add +5V generate +3V_LCD circuit 21. Remove +5V_CHG generate circuit 22. Use SB GPIO33, GPIO34 to controll the level of VCORE 23. U31 use APL5315BI-TRL to replace MAX8863TEUK(pin to pin, but reference voltage level different) 24. PR59 change to 130K Ohm for both 12V Adapter and 9.8V Adapter
	2007/05/22 }	P701 1.0G Gerber Out
1.1G	2007/05/31 }	P701 Schematic 1.1G Beginning 1. Remove the 48M clock from CLock Gen to Card Reader UB6225P 2. Clock Gen ICS9LPR367 change to ICS9LPR426 3. Flash Connector increase SATA and USB interface 4. Add Onboard Flash(SM223 + NAND Flash x4) 5. BATT_CON pin 5 connect to GND 6. Q34 pin 1 connect to +3V to fix EC reset issue 7. Remove J1, J2 8. KB pin 28 connect to GND for P701-ISP_CARD 9. Use SB GPO23 to Enable/Disable Audio Amplifier 10. Use SB GPO21 to controll Camera Power 11. Use SB GPIO24 to controll Minicard Power 12. Use SB GPIO25 to Enable/Disable WLAN Ratio 13. Atheros L2 and Minicard SMBUS interface directly pull high 14. LCD_CON pin 20 connect to AC_BAT_SYS
	2007/06/07 }	P701 1.1G Gerber Out


Rev	Date	Description
1.2G	2007/06/30 }	P701 Schematic 1.2G Beginning 1. Add R174 to short DASP pins of Master IDE device and SLave IDE device 2. Use SB GPIO27 to controll Card Reader UB6225P Power 3. PR606084.2 connect to +5V to fix LCD flash issue 4. Adjust SPEAKER pin define 5. Adjust CHARGE LED and WLAN LED lightness 6. Use SB GPI 26, 29, 30, 31 for PCB version 7. Change USB ESD diode for EMI request 8. Add Floating GND TP_GND and Spring TP1 & TP2 for EMI request 9. Change PM_VCOREL1, PM_VCOREL2 default level 10. Add PQ48 to controll +3V_PE to fix WLAN AW-GE780 can't detect issue 11. Power Charger part update circuit for new Adapter 12. Use SB GPI12 to detect LID signal level 13. Add H/W THERMTRIP circuit (page 36) 14. Add U40 to prevent system auto power on after clear CMOS 15. Use SB GPI7 for THRO_CPU 16. Power Charger part update circuit to prevent incorrect Adapter damage boards 17. Q1.1, Q2.1 change to +3V
	2007/07/06 }	P701 1.2G Gerber Out
1.2G	2007/07/26 }	P701 Schematic 1.3G Beginning 1. Add R11 for 801

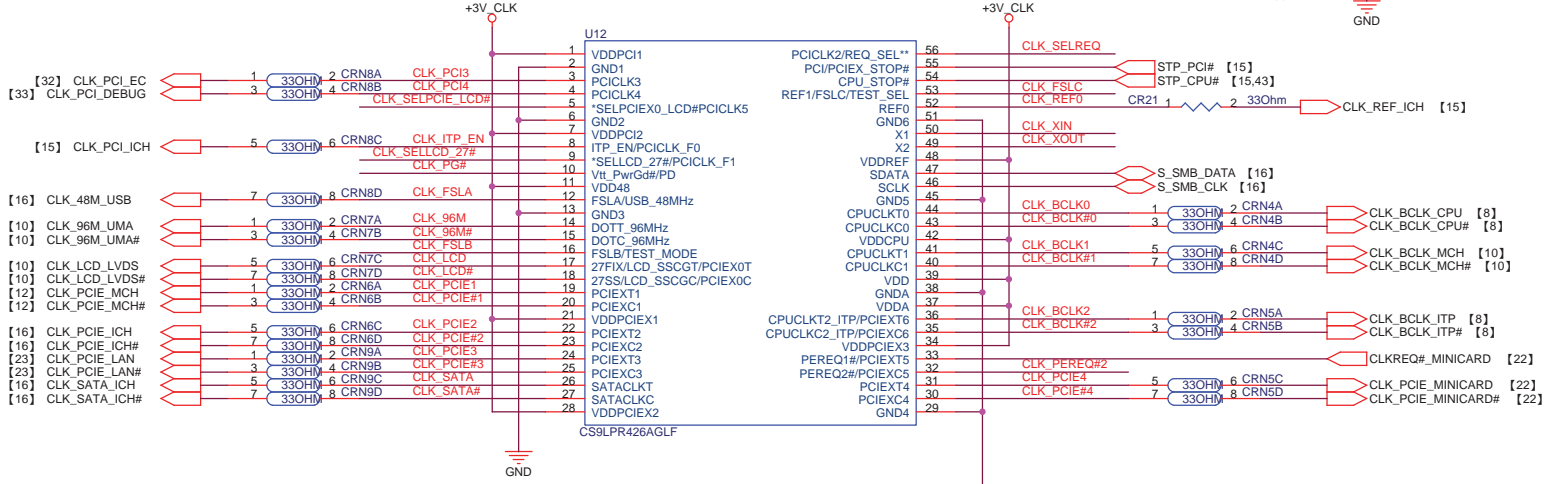
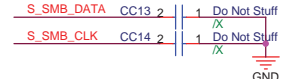
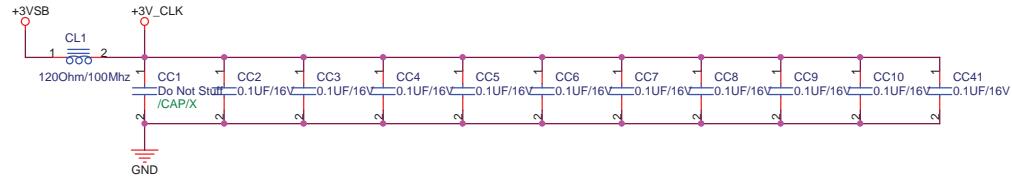
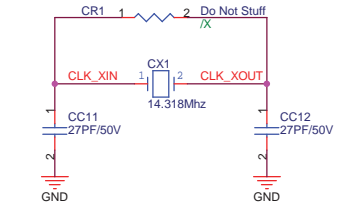
P900_R1.1G_WO_FLASH

		Title : History	
ASUSTek Computer INC.		Engineer: Tiansen_Wu	
Size	Project Name	Rev	
A3	P900	1.2G	
Date: Wednesday, February 27, 2008		Sheet	5 of 47

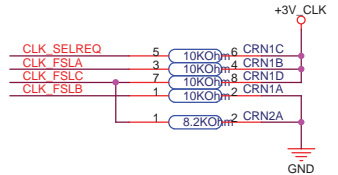
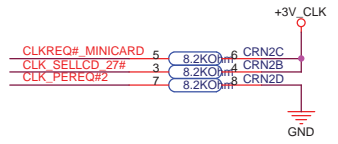


P900_R1.1G_WO_FLASH

		Title : Blank	
ASUSTek Computer INC.		Engineer: <i>Tiansen_Wu</i>	
Size	Project Name		Rev
A3	P900		1.2G
Date: Wednesday, February 27, 2008		Sheet	6 of 47

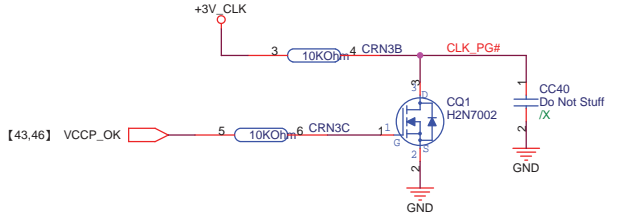


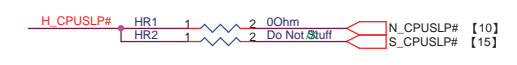
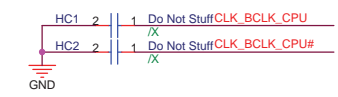
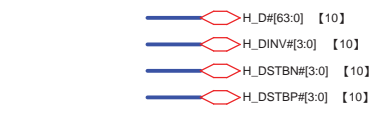
- CLK_BCLK_CPU CC15 2 1 Do Not Stuff /X
- CLK_BCLK_CPU# CC16 2 1 Do Not Stuff /X
- CLK_BCLK_MCH CC17 2 1 Do Not Stuff /X
- CLK_BCLK_MCH# CC18 2 1 Do Not Stuff /X
- CLK_BCLK_ITP CC19 2 1 Do Not Stuff /ITP/X
- CLK_BCLK_ITP# CC20 2 1 Do Not Stuff /ITP/X
- CLK_PCIE_MCH CC21 2 1 Do Not Stuff /X
- CLK_PCIE_MCH# CC22 2 1 Do Not Stuff /X
- CLK_PCIE_ICH CC23 2 1 Do Not Stuff /X
- CLK_PCIE_ICH# CC24 2 1 Do Not Stuff /X
- CLK_PCIE_MINICARD CC25 2 1 Do Not Stuff /X
- CLK_PCIE_MINICARD# CC26 2 1 Do Not Stuff /X
- CLK_PCIE_LAN CC27 2 1 Do Not Stuff /X
- CLK_PCIE_LAN# CC28 2 1 Do Not Stuff /X
- CLK_96M_UMA CC29 2 1 Do Not Stuff /X
- CLK_96M_UMA# CC30 2 1 Do Not Stuff /X
- CLK_LCD_LVDS CC31 2 1 10PF/50V
- CLK_LCD_LVDS# CC32 2 1 10PF/50V
- CLK_SATA_ICH CC38 2 1 Do Not Stuff /X
- CLK_SATA_ICH# CC39 2 1 Do Not Stuff /X
- CLK_PCI_ICH CC33 2 1 Do Not Stuff /X
- CLK_PCI_EC CC34 2 1 Do Not Stuff /X
- CLK_PCI_DEBUG CC35 2 1 Do Not Stuff /DEBUG/X
- CLK_REF_ICH CC36 2 1 Do Not Stuff /X
- CLK_48M_USB CC37 2 1 Do Not Stuff /X



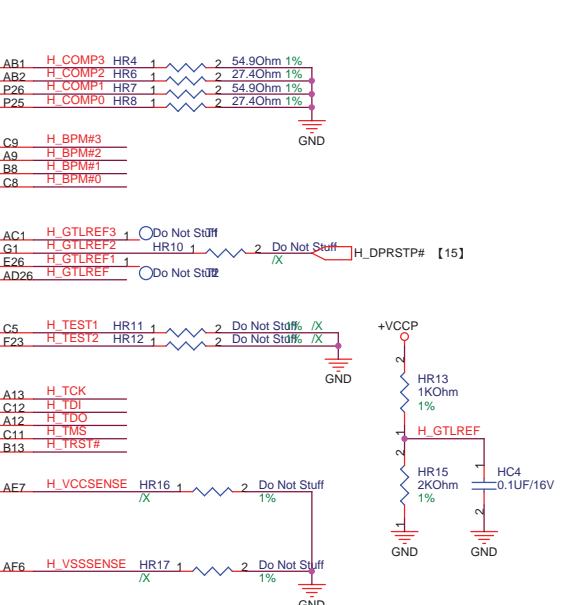
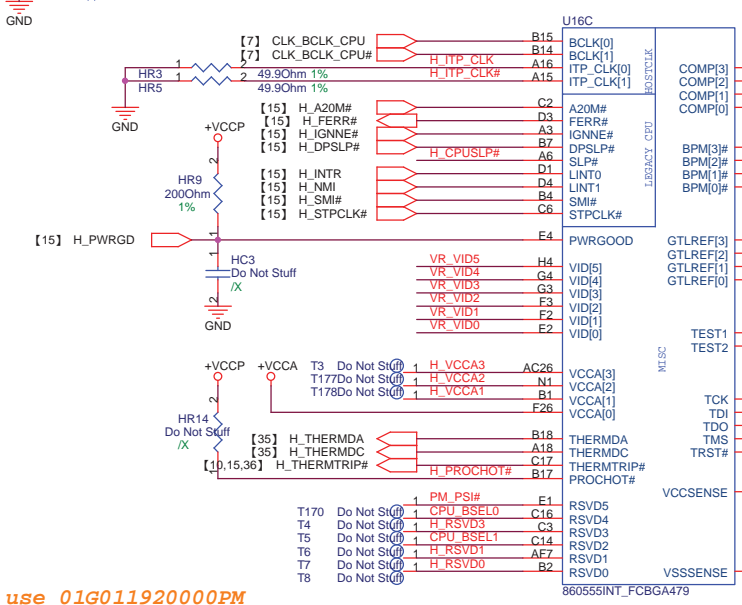
FSB clock fix 100MHz

	100MHz	1.33MHz
FSLA	1	1
FSLB	0	0
FSLC	1	0



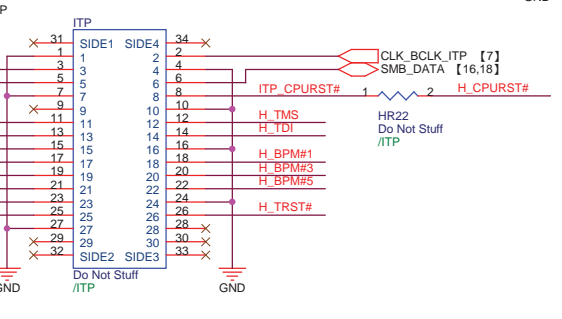
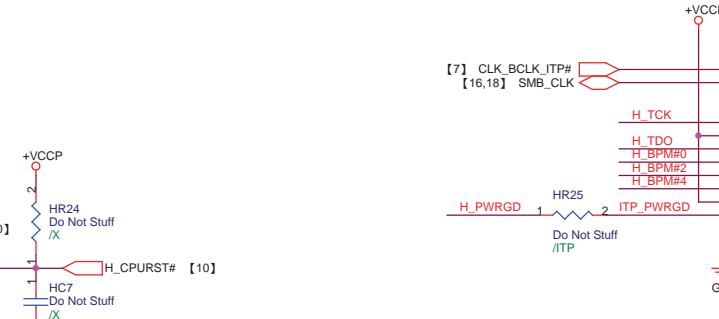
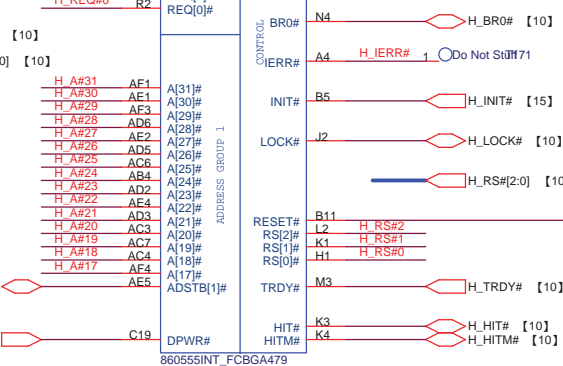
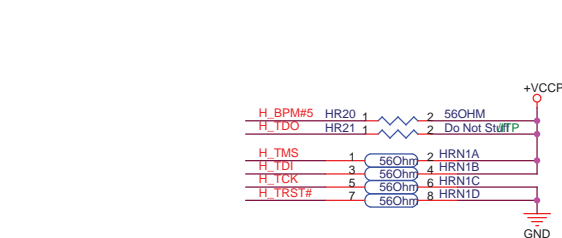
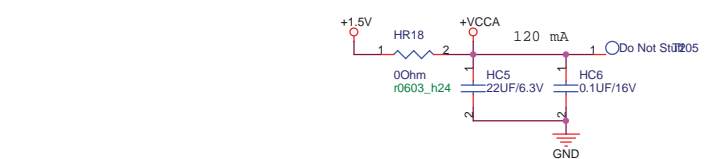


U16A		DATA GROUP 0		DATA GROUP 2		DATA GROUP 1		DATA GROUP 3	
H_D#15	C25	D[15]#	D[47]#	Y25	H_D#47	D[31]#	D[63]#	AE26	H_D#63
H_D#14	E23	D[14]#	D[46]#	AA26	H_D#46	H_D#30	D[30]#	AE22	H_D#62
H_D#13	B23	D[13]#	D[45]#	Y23	H_D#45	H_D#28	D[28]#	AE25	H_D#61
H_D#12	C26	D[12]#	D[44]#	V26	H_D#44	H_D#27	D[27]#	AD21	H_D#59
H_D#11	E24	D[11]#	D[43]#	U25	H_D#43	H_D#26	D[26]#	AE21	H_D#58
H_D#10	D24	D[10]#	D[42]#	U26	H_D#42	H_D#25	D[25]#	AD20	H_D#57
H_D#9	B24	D[9]#	D[41]#	L26	H_D#41	H_D#24	D[24]#	AE23	H_D#56
H_D#8	C20	D[8]#	D[40]#	D[9]#	H_D#40	H_D#23	D[23]#	AE22	H_D#55
H_D#7	B20	D[7]#	D[39]#	R23	H_D#39	H_D#22	D[22]#	AD23	H_D#54
H_D#6	A21	D[6]#	D[38]#	R26	H_D#38	H_D#21	D[21]#	AC22	H_D#52
H_D#5	B26	D[5]#	D[37]#	R24	H_D#37	H_D#20	D[20]#	AC20	H_D#51
H_D#4	A24	D[4]#	D[36]#	U23	H_D#36	H_D#19	D[19]#	AD20	H_D#49
H_D#3	B21	D[3]#	D[35]#	U23	H_D#35	H_D#18	D[18]#	AD20	H_D#48
H_D#2	A22	D[2]#	D[34]#	T25	H_D#34	H_D#17	D[17]#	AC23	H_D#47
H_D#1	A25	D[1]#	D[33]#	AA24	H_D#33	H_D#16	D[16]#	AD20	H_D#46
H_D#0	A19	D[0]#	D[32]#	Y26	H_D#32	H_D#15	D[15]#	AD20	H_D#45
H_DINV#0	D25	DINV[0]#	DINV[2]#	T24	H_DINV#2	H_D#14	D[14]#	AD20	H_D#44
H_DSTBN#0	C23	DSTBN[0]#	DSTBN[2]#	W25	H_DSTBN#2	H_D#13	D[13]#	AD20	H_D#43
H_DSTBP#0	C22	DSTBP[0]#	DSTBP[2]#	W24	H_DSTBP#2	H_D#12	D[12]#	AE25	H_DSTBN#3
H_D#31	K25	D[31]#	D[63]#	AE26	H_D#63	H_D#11	D[11]#	AE25	H_DSTBP#3
H_D#30	N25	D[30]#	D[62]#	D[30]#	H_D#62	H_D#10	D[10]#		
H_D#29	H26	D[29]#	D[61]#	D[29]#	H_D#61	H_D#9	D[9]#		
H_D#28	H26	D[28]#	D[60]#	D[28]#	H_D#60	H_D#8	D[8]#		
H_D#27	M25	D[27]#	D[59]#	D[27]#	H_D#59	H_D#7	D[7]#		
H_D#26	L26	D[26]#	D[58]#	D[26]#	H_D#58	H_D#6	D[6]#		
H_D#25	J25	D[25]#	D[57]#	D[25]#	H_D#57	H_D#5	D[5]#		
H_D#24	M23	D[24]#	D[56]#	D[24]#	H_D#56	H_D#4	D[4]#		
H_D#23	J23	D[23]#	D[55]#	D[23]#	H_D#55	H_D#3	D[3]#		
H_D#22	G24	D[22]#	D[54]#	D[22]#	H_D#54	H_D#2	D[2]#		
H_D#21	G24	D[21]#	D[53]#	D[21]#	H_D#53	H_D#1	D[1]#		
H_D#20	H24	D[20]#	D[52]#	D[20]#	H_D#52				
H_D#19	M26	D[19]#	D[51]#	D[19]#	H_D#51				
H_D#18	L23	D[18]#	D[50]#	D[18]#	H_D#50				
H_D#17	G25	D[17]#	D[49]#	D[17]#	H_D#49				
H_D#16	H23	D[16]#	D[48]#	D[16]#	H_D#48				
H_DINV#1	J26	DINV[1]#	DINV[3]#	AE24	H_DSTBN#3				
H_DSTBN#1	K24	DSTBN[1]#	DSTBN[3]#	AE25	H_DSTBP#3				
H_DSTBP#1	L24	DSTBP[1]#	DSTBP[3]#						



U16 use 01G01192000PM

U16B		ADDRESS GROUP 0		ADDRESS GROUP 1		ADDRESS GROUP 2	
H_A#16	AA2	A[16]#	ADS#	N2	H_BPM#4	H_ADS#	[10]
H_A#15	Y3	A[15]#	PRDY#	A10	H_BPM#5		
H_A#14	AA3	A[14]#	PREQ#	B10			
H_A#13	U1	A[13]#		L1	H_BNR#	[10]	
H_A#12	Y1	A[12]#		J3	H_BPRI#	[10]	
H_A#11	Y4	A[11]#		A7	H_DBR#	1	Do Not Stuff
H_A#10	W2	A[10]#					
H_A#9	T4	A[9]#		L4	H_DEFER#	[10]	
H_A#8	W2	A[8]#		H2	H_DRDY#	[10]	
H_A#7	V2	A[7]#		M2	H_DBSY#	[10]	
H_A#6	R3	A[6]#					
H_A#5	V3	A[5]#					
H_A#4	U4	A[4]#					
H_A#3	P4	A[3]#					
[10] H_ADSTB#0	H_REQ#4	T1	ADSTB[0]#				
	H_REQ#3	P1	REQ[4]#				
	H_REQ#2	T2	REQ[3]#				
	H_REQ#1	P3	REQ[2]#				
	H_REQ#0	R2	REQ[1]#				
			REQ[0]#				
[10] H_A# [31:3]	[10]						
[10] H_REQ# [4:0]	[10]						
H_A#31	AE1	A[31]#	INIT#	B5	H_INIT#	[15]	
H_A#30	AE1	A[30]#					
H_A#29	AE3	A[29]#					
H_A#28	AD6	A[28]#					
H_A#27	AE2	A[27]#					
H_A#26	AD5	A[26]#					
H_A#25	AB4	A[25]#					
H_A#24	AC6	A[24]#					
H_A#23	AD2	A[23]#					
H_A#22	AE4	A[22]#					
H_A#21	AD3	A[21]#					
H_A#20	AC3	A[20]#					
H_A#19	AC7	A[19]#					
H_A#18	AC4	A[18]#					
H_A#17	AE5	A[17]#					
[10] H_ADSTB#1	AE5	ADSTB[1]#					
[10] H_DPWR#	C19	DPWR#					



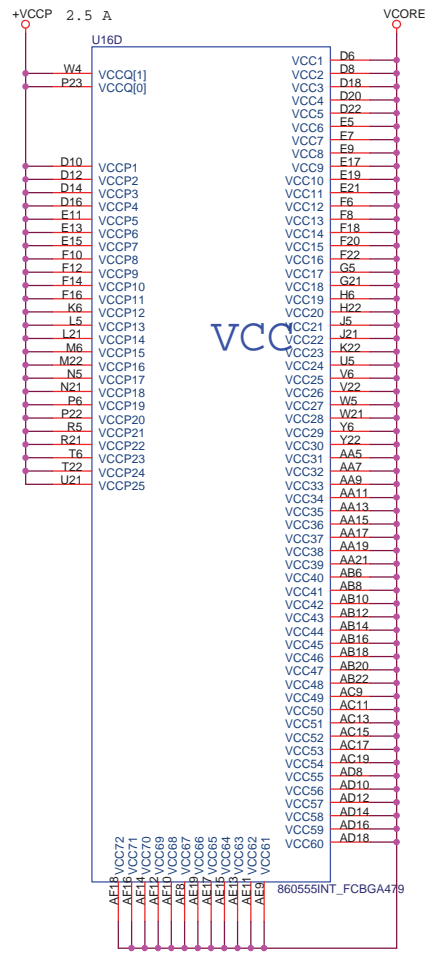
P900_R1.1G_WO_FLASH

ASUS Title: Dothan_HOST

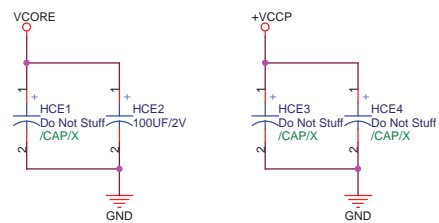
ASUSTek Computer INC. Engineer: Tiansen_Wu

Size: A3 Project Name: P900 Rev: 1.2G

Date: Wednesday, February 27, 2008 Sheet: 8 of 47

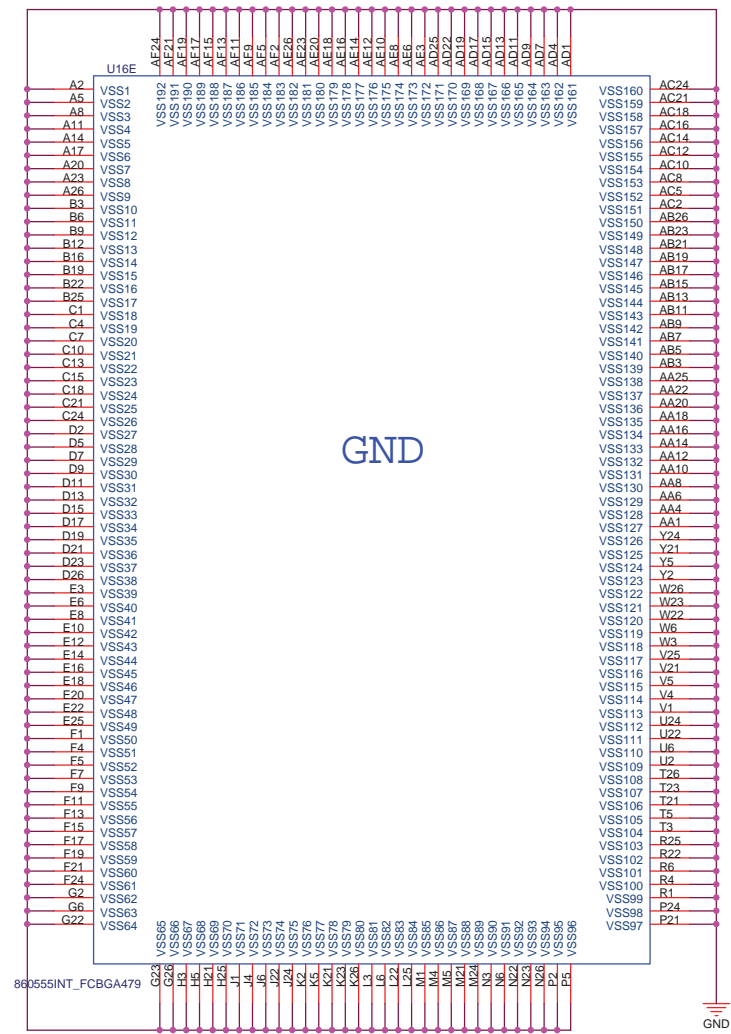
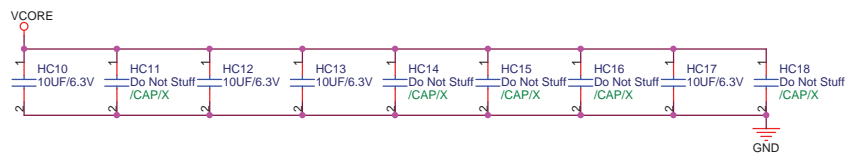
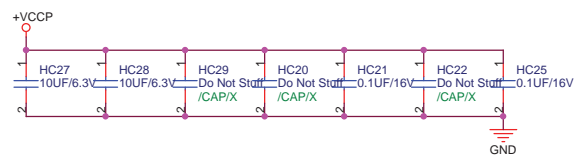
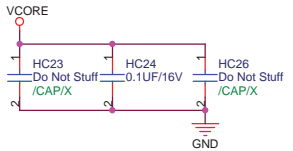


Celeron-M(Dothan) ULV max 7 A



U16 use 01G011920000PM

0.1U All X7R



P900_R1.1G_WO_FLASH

ASUS Title: Dothan_PWR_GND

ASUSTek Computer INC. Engineer: Tiansen_Wu

Size	Project Name	Rev
A3	P900	1.2G

Date: Wednesday, February 27, 2008 Sheet 9 of 47



U1 use 02G010007612

U1B		U1C	
MA_DQ0	AG35	SA_DQ0	SA_BS0 AK15 MA_BA0
MA_DQ1	AH35	SA_DQ1	SA_BS1 AK16 MA_BA1
MA_DQ2	AL35	SA_DQ2	SA_BS2 AL21 MA_BA2
MA_DQ3	AL37	SA_DQ3	
MA_DQ4	AH36	SA_DQ4	SA_DM0 AJ37 MA_DM0
MA_DQ5	AJ35	SA_DQ5	SA_DM1 AP35 MA_DM1
MA_DQ6	AK37	SA_DQ6	SA_DM2 AL29 MA_DM2
MA_DQ7	AL34	SA_DQ7	SA_DM3 AP24 MA_DM3
MA_DQ8	AM36	SA_DQ8	SA_DM4 AP4 MA_DM4
MA_DQ9	AN35	SA_DQ9	SA_DM5 AP4 MA_DM5
MA_DQ10	AP32	SA_DQ10	SA_DM6 AJ2 MA_DM6
MA_DQ11	AM31	SA_DQ11	SA_DM7 AD3 MA_DM7
MA_DQ12	AM34	SA_DQ12	
MA_DQ13	AM35	SA_DQ13	SA_DQS0 AK36 MA_DQS0
MA_DQ14	AL32	SA_DQ14	SA_DQS1 AP33 MA_DQS1
MA_DQ15	AM32	SA_DQ15	SA_DQS2 AN29 MA_DQS2
MA_DQ16	AN31	SA_DQ16	SA_DQS3 AP23 MA_DQS3
MA_DQ17	AP31	SA_DQ17	SA_DQS4 AM8 MA_DQS4
MA_DQ18	AN28	SA_DQ18	SA_DQS5 AM4 MA_DQS5
MA_DQ19	AL30	SA_DQ19	SA_DQS6 AJ1 MA_DQS6
MA_DQ20	AP28	SA_DQ20	SA_DQS7 AE5 MA_DQS7
MA_DQ21	AM30	SA_DQ21	
MA_DQ22	AM28	SA_DQ22	SA_DQS0# AK35 MA_DQS0#
MA_DQ23	AL28	SA_DQ23	SA_DQS1# AP34 MA_DQS1#
MA_DQ24	AP27	SA_DQ24	SA_DQS2# AN30 MA_DQS2#
MA_DQ25	AM27	SA_DQ25	SA_DQS3# AN23 MA_DQS3#
MA_DQ26	AM23	SA_DQ26	SA_DQS4# AN8 MA_DQS4#
MA_DQ27	AM22	SA_DQ27	SA_DQS5# AM5 MA_DQS5#
MA_DQ28	AL23	SA_DQ28	SA_DQS6# AH1 MA_DQS6#
MA_DQ29	AM24	SA_DQ29	SA_DQS7# AE4 MA_DQS7#
MA_DQ30	AN22	SA_DQ30	
MA_DQ31	AP22	SA_DQ31	SA_MA0 AL17 MA_MA0
MA_DQ32	AM9	SA_DQ32	SA_MA1 AP18 MA_MA1
MA_DQ33	AL9	SA_DQ33	SA_MA2 AP18 MA_MA2
MA_DQ34	AL6	SA_DQ34	SA_MA3 AM17 MA_MA3
MA_DQ35	AP7	SA_DQ35	SA_MA4 AN18 MA_MA4
MA_DQ36	AP11	SA_DQ36	SA_MA5 AM18 MA_MA5
MA_DQ37	AP10	SA_DQ37	SA_MA6 AL19 MA_MA6
MA_DQ38	AL7	SA_DQ38	SA_MA7 AP20 MA_MA7
MA_DQ39	AM7	SA_DQ39	SA_MA8 AM19 MA_MA8
MA_DQ40	AN5	SA_DQ40	SA_MA9 AL20 MA_MA9
MA_DQ41	AN6	SA_DQ41	SA_MA10 AM16 MA_MA10
MA_DQ42	AN3	SA_DQ42	SA_MA11 AN20 MA_MA11
MA_DQ43	AP3	SA_DQ43	SA_MA12 AM20 MA_MA12
MA_DQ44	AP6	SA_DQ44	SA_MA13 AM15 MA_MA13
MA_DQ45	AM6	SA_DQ45	
MA_DQ46	AL4	SA_DQ46	SA_CAS# AN15 MA_CAS# [18,19]
MA_DQ47	AM3	SA_DQ47	SA_RAS# AP16 MA_RAS# [18,19]
MA_DQ48	AK2	SA_DQ48	SA_RCVENIN# AF29 MA_RCVENIN# 1 Do Not StuiB7
MA_DQ49	AK3	SA_DQ49	SA_RCVENOUT# AF28 MA_RCVENOUT# 1 Do Not StuiB8
MA_DQ50	AG2	SA_DQ50	SA_WE# AP15 MA_WE# [18,19]
MA_DQ51	AG1	SA_DQ51	
MA_DQ52	AL3	SA_DQ52	
MA_DQ53	AM2	SA_DQ53	
MA_DQ54	AH3	SA_DQ54	
MA_DQ55	AG3	SA_DQ55	
MA_DQ56	AF3	SA_DQ56	
MA_DQ57	AE3	SA_DQ57	
MA_DQ58	AD6	SA_DQ58	
MA_DQ59	AC4	SA_DQ59	
MA_DQ60	AF2	SA_DQ60	
MA_DQ61	AF1	SA_DQ61	
MA_DQ62	AD4	SA_DQ62	
MA_DQ63	AD5	SA_DQ63	

NQ82915PM

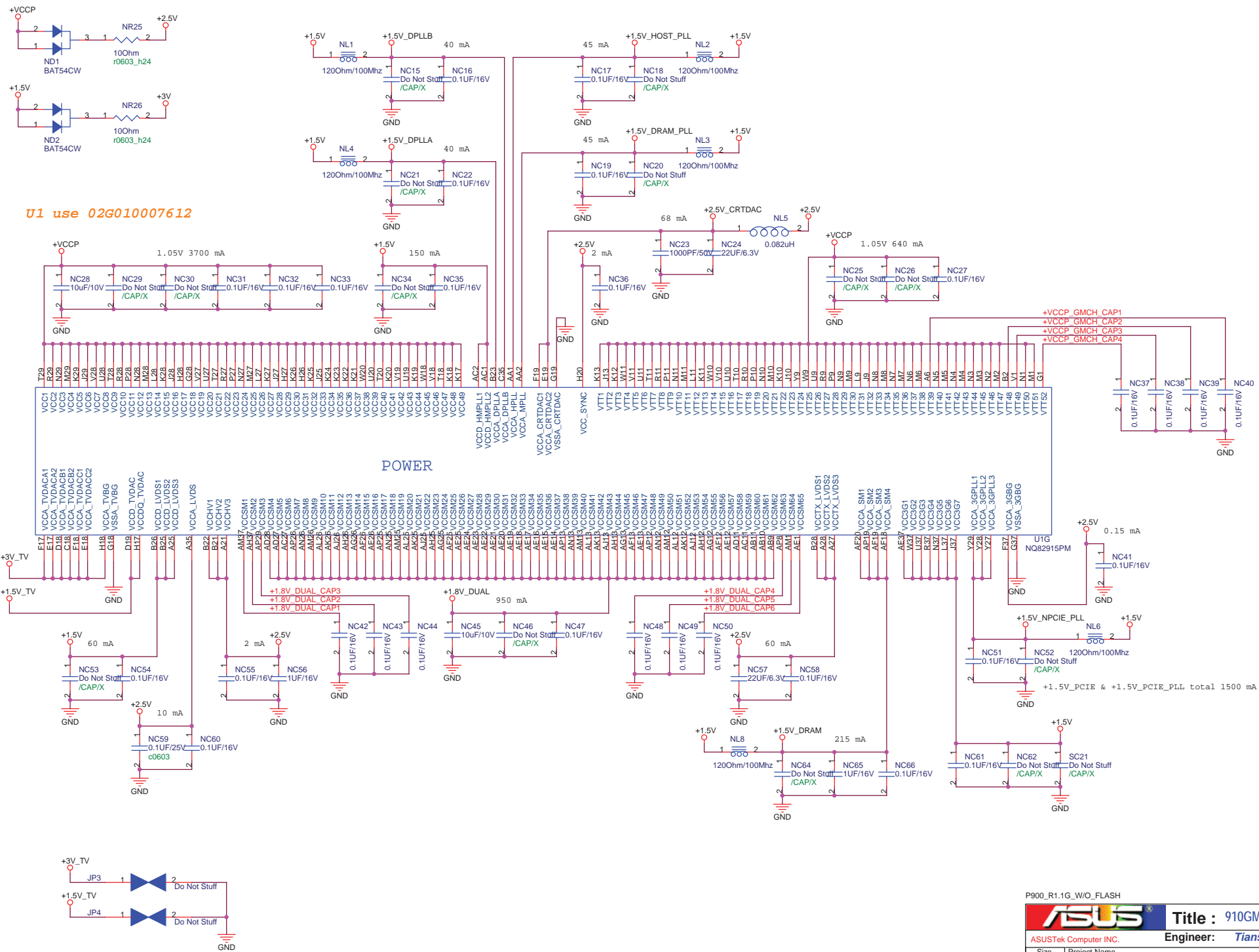
DDR SYSTEM MEMORY A

U1C		DDR SYSTEM MEMORY B	
AE31	SB_DQ0	SB_BS0	AH15
AE32	SB_DQ1	SB_DM2	AG17
AG32	SB_DQ2	SB_BS1	AG21
AG36	SB_DQ3	SB_BS2	
AE34	SB_DQ4		AF32
AE33	SB_DQ5	SB_DM0	AK34
AF31	SB_DQ6	SB_DM1	AK27
AF30	SB_DQ7	SB_DM2	AK24
AH33	SB_DQ8	SB_DM3	AJ10
AH32	SB_DQ9	SB_DM4	AK5
AK31	SB_DQ10	SB_DM5	AF7
AG30	SB_DQ11	SB_DM6	AB7
AG34	SB_DQ12	SB_DM7	
AG33	SB_DQ13		AF34
AH31	SB_DQ14	SB_DQS0	AK32
AJ31	SB_DQ15	SB_DQS1	AJ28
AK30	SB_DQ16	SB_DQS2	AK23
AJ30	SB_DQ17	SB_DQS3	AM10
AH29	SB_DQ18	SB_DQS4	AH6
AH28	SB_DQ19	SB_DQS5	AF8
AK29	SB_DQ20	SB_DQS6	AB4
AH30	SB_DQ21	SB_DQS7	
AH27	SB_DQ22		AF35
AG28	SB_DQ23	SB_DQS0#	AK33
AF24	SB_DQ24	SB_DQS1#	AK28
AG23	SB_DQ25	SB_DQS2#	AJ23
AJ22	SB_DQ26	SB_DQS3#	AL10
AK22	SB_DQ27	SB_DQS4#	AH7
AH24	SB_DQ28	SB_DQS5#	AF7
AH23	SB_DQ29	SB_DQS6#	AB5
AG22	SB_DQ30	SB_DQS7#	
AJ21	SB_DQ31		AH17
AG10	SB_DQ32	SB_MA0	AK17
AG9	SB_DQ33	SB_MA1	AH18
AG8	SB_DQ34	SB_MA2	AH18
AH8	SB_DQ35	SB_MA3	AH18
AH11	SB_DQ36	SB_MA4	AJ19
AH10	SB_DQ37	SB_MA5	AJ19
AJ9	SB_DQ38	SB_MA6	AK19
AK9	SB_DQ39	SB_MA7	AH19
AJ7	SB_DQ40	SB_MA8	AJ20
AK6	SB_DQ41	SB_MA9	AH20
AJ4	SB_DQ42	SB_MA10	AH18
AH5	SB_DQ43	SB_MA11	AG18
AK8	SB_DQ44	SB_MA12	AG20
AJ8	SB_DQ45	SB_MA13	AG18
AJ5	SB_DQ46		AH14
AK4	SB_DQ47	SB_CAS#	AK14
AG5	SB_DQ48	SB_RAS#	AF15
AG4	SB_DQ49	SB_RCVENIN#	AF14
AD8	SB_DQ50	SB_RCVENOUT#	AH16
AD9	SB_DQ51	SB_WE#	
AH4	SB_DQ52		
AG6	SB_DQ53		
AE8	SB_DQ54		
AD7	SB_DQ55		
AC5	SB_DQ56		
AB8	SB_DQ57		
AB6	SB_DQ58		
AA8	SB_DQ59		
AC7	SB_DQ60		
AC8	SB_DQ61		
AA4	SB_DQ62		
AA5	SB_DQ63		

NQ82915PM

P900_R1.1G_WO_FLASH

ASUS		Title : 910GML_DRAM	
ASUSTek Computer INC.		Engineer: Tiansen_Wu	
Size	Project Name	Rev	
A3	P900	1.2G	
Date: Wednesday, February 27, 2008	Sheet	11 of 47	

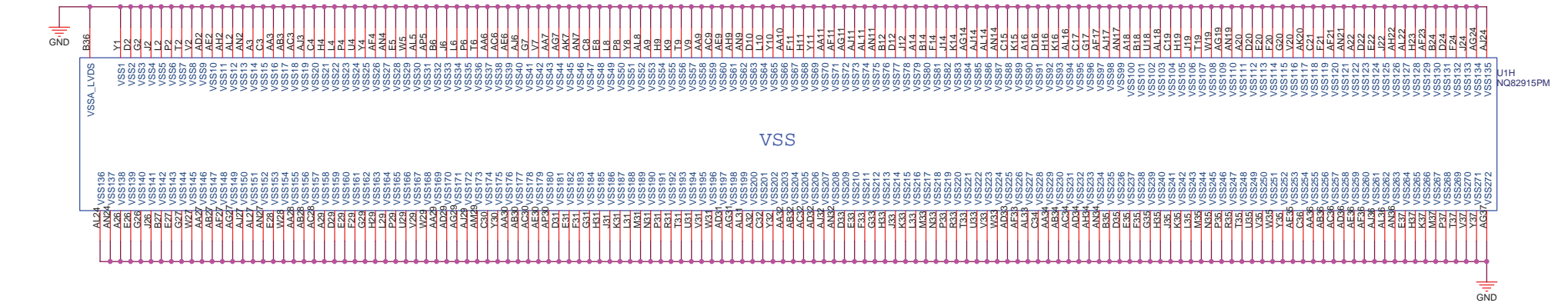
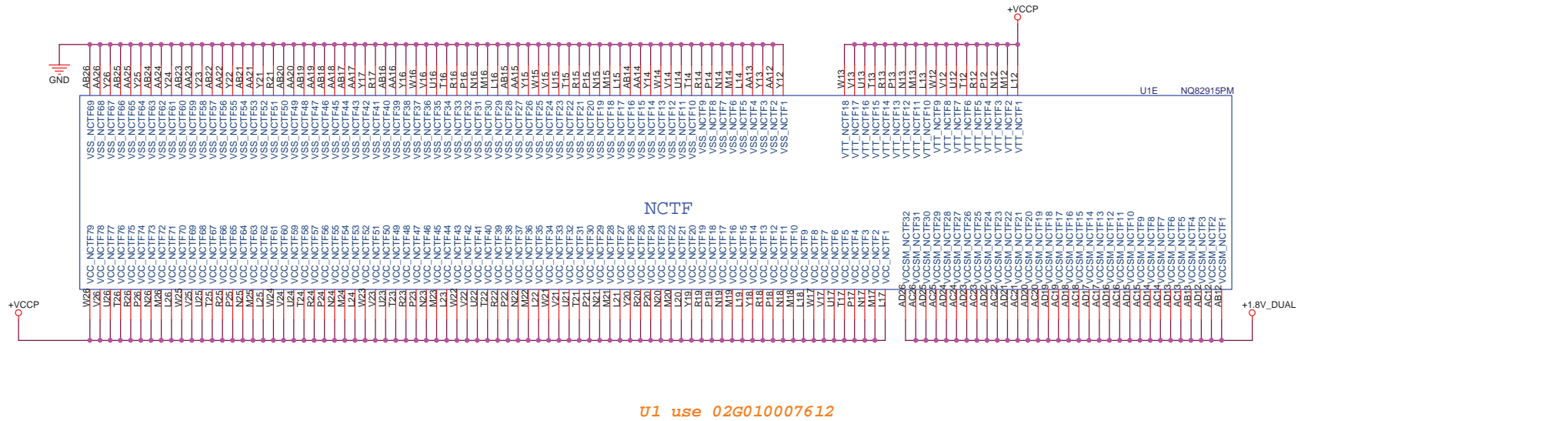


U1 use 02G010007612

POWER

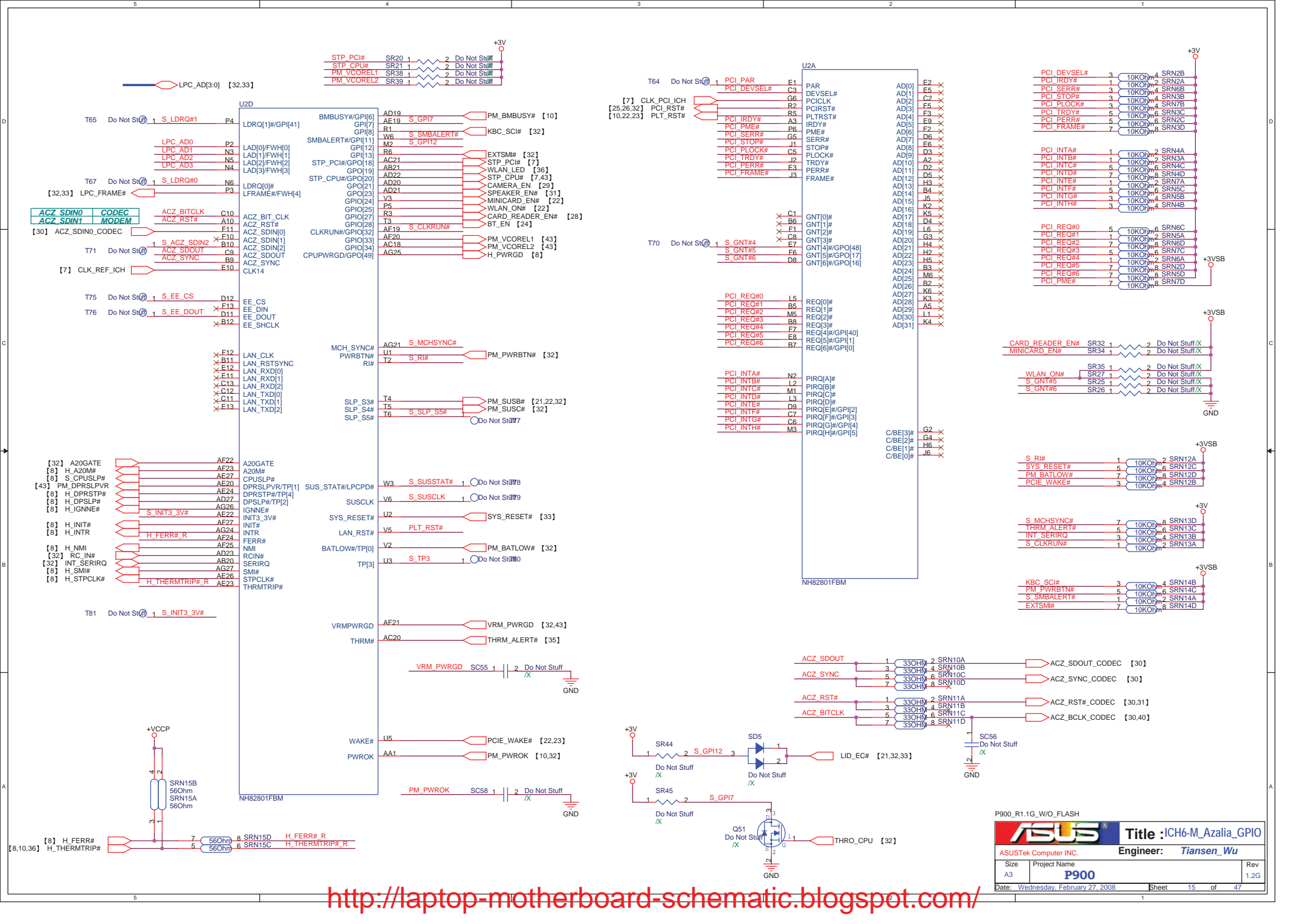
P900_R1.1G_WO_FLASH

ASUS		Title : 910GML_PWR	
ASUSTek Computer INC.		Engineer: <i>Tiansen_Wu</i>	
Size	A3	Project Name	P900
Date:	Wednesday, February 27, 2008	Sheet	13 of 47
Rev	1.2G		



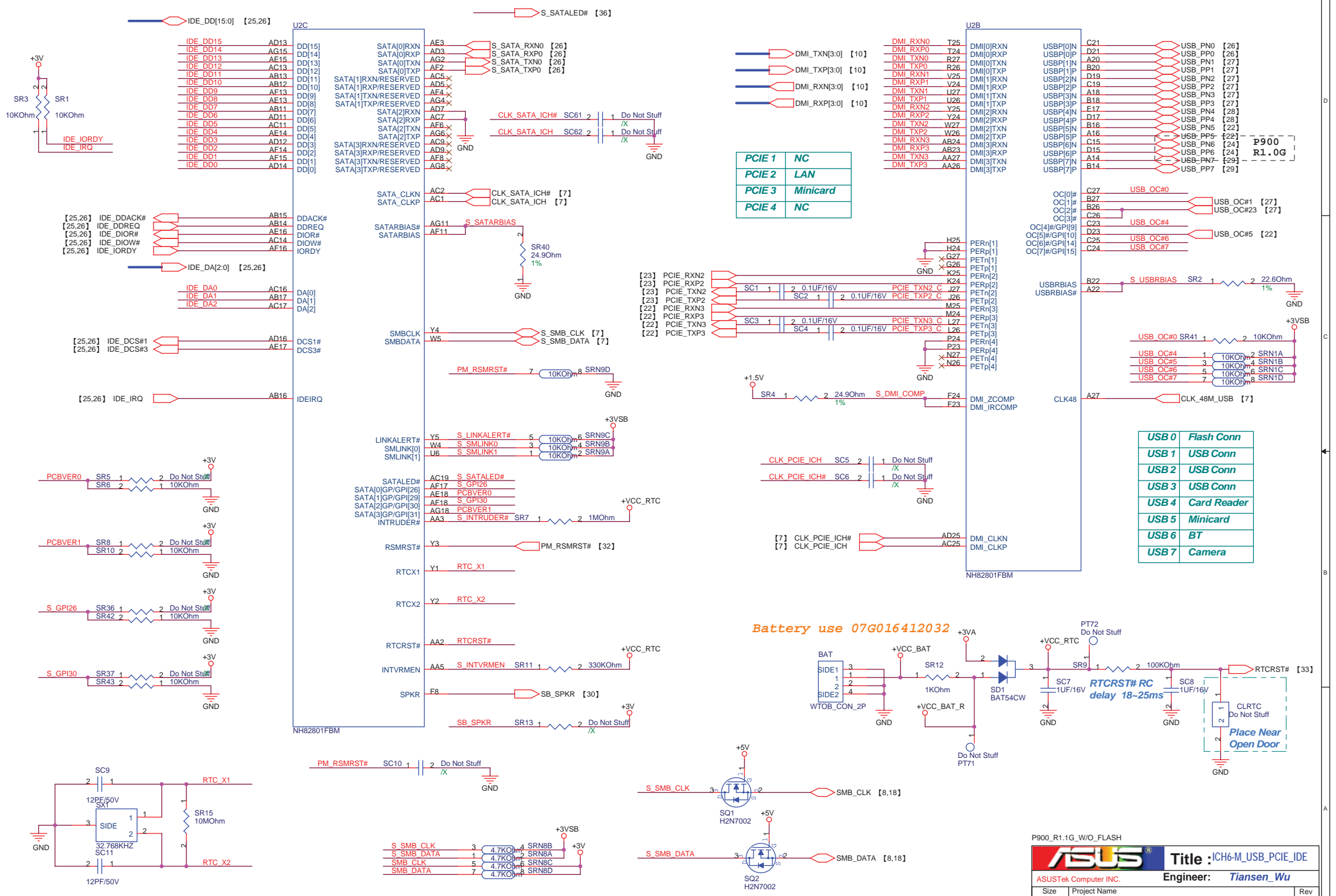
P900_R1.1G_W/O_FLASH

ASUS		Title : 910GML_GND	
ASUSTek Computer INC.		Engineer: <i>Tiansen_Wu</i>	
Size	Project Name	Rev	
A3	P900	1.2G	
Date: Wednesday, February 27, 2008		Sheet	14 of 47



P900_R1.1G_WO_FLASH

ASUS		Title :ICH6-M_Azalia_GPIO	
ASUSTek Computer INC.		Engineer: <i>Tiansen_Wu</i>	
Size A3	Project Name P900	Rev 1.2G	
Date: Wednesday, February 27, 2008	Sheet 15	of 47	



PCIE 1	NC
PCIE 2	LAN
PCIE 3	Minicard
PCIE 4	NC

USB 0	Flash Conn
USB 1	USB Conn
USB 2	USB Conn
USB 3	USB Conn
USB 4	Card Reader
USB 5	Minicard
USB 6	BT
USB 7	Camera

Battery use 07G016412032

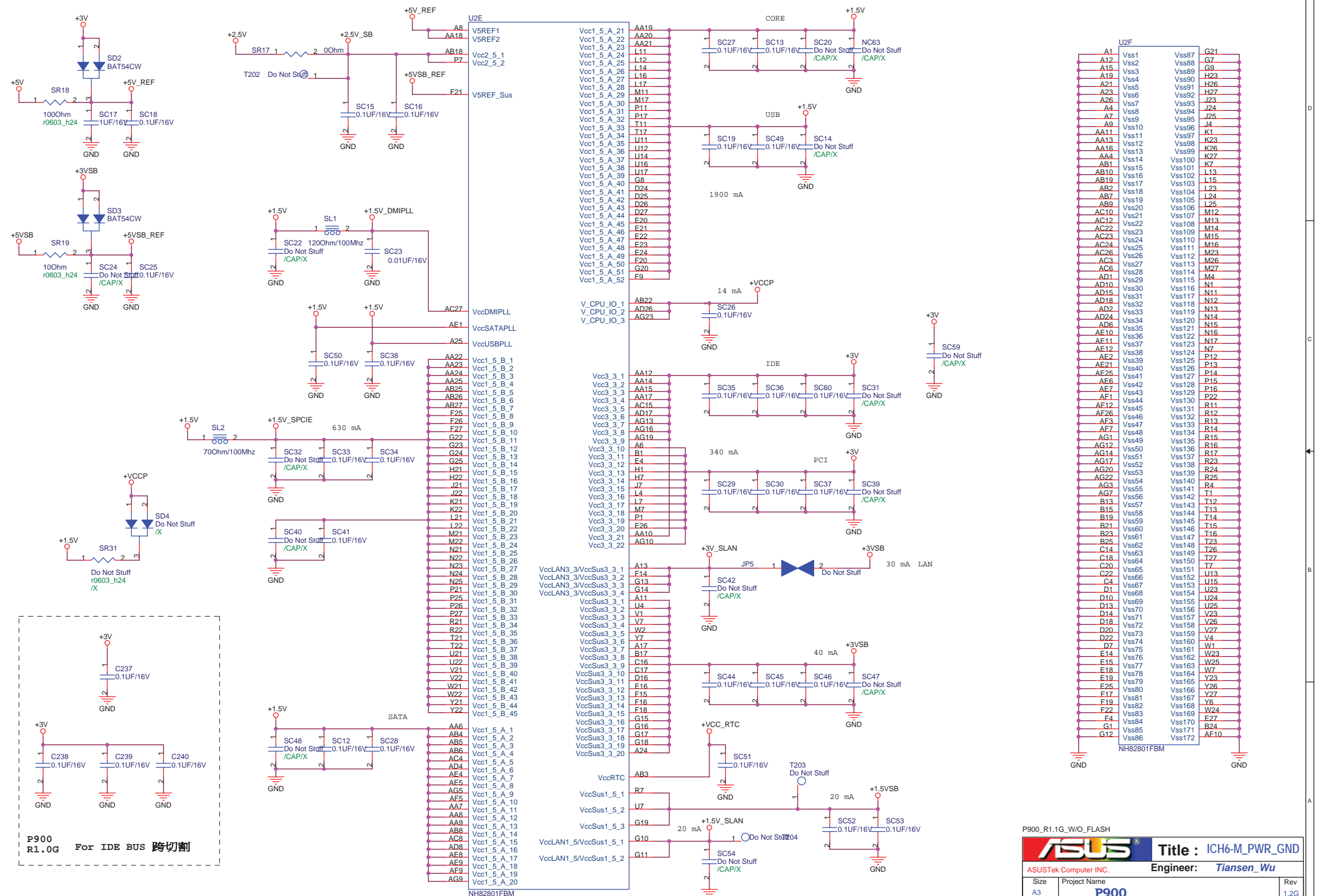
P900_R1.0G_WO_FLASH

ASUS Title : ICH6-M_USB_PCIE_IDE

ASUSTek Computer INC. Engineer: Tiansen_Wu

Size A3 Project Name **P900** Rev 1.2G

Date: Wednesday, February 27, 2008 Sheet 16 of 47



Vcc1_5_A_21	AA19	Vcc3_3_1	AA12	VccLAN3_3/VccSus3_3_1	A13	VccRTC	AB3	VccSus1_5_1	R7	VccLAN1_5/VccSus1_5_1	G19	VccLAN1_5/VccSus1_5_2	G10
Vcc1_5_A_22	AA20	Vcc3_3_2	AA14	VccLAN3_3/VccSus3_3_2	F14	VccRTC	AB4	VccSus1_5_2	U7	VccLAN1_5/VccSus1_5_2	G10		
Vcc1_5_A_23	AA21	Vcc3_3_3	AA15	VccLAN3_3/VccSus3_3_3	G13	VccRTC	AB5						
Vcc1_5_A_24	L11	Vcc3_3_4	AA16	VccLAN3_3/VccSus3_3_4	G14	VccRTC	AB6						
Vcc1_5_A_25	L14	Vcc3_3_5	AC15	VccSus3_3_1	A11	VccRTC	AC4						
Vcc1_5_A_26	L16	Vcc3_3_6	AD17	VccSus3_3_2	V1	VccRTC	AC5						
Vcc1_5_A_27	L17	Vcc3_3_7	AG13	VccSus3_3_3	V7	VccRTC	AC6						
Vcc1_5_A_28	M11	Vcc3_3_8	AG16	VccSus3_3_4	W2	VccRTC	AC7						
Vcc1_5_A_29	M17	Vcc3_3_9	AG19	VccSus3_3_5	Y7	VccRTC	AC8						
Vcc1_5_A_30	P17	Vcc3_3_10	A6	VccSus3_3_6	L7	VccRTC	AC9						
Vcc1_5_A_31	T11	Vcc3_3_11	B1	VccSus3_3_7	M7	VccRTC	AC10						
Vcc1_5_A_32	T17	Vcc3_3_12	E4	VccSus3_3_8	P1	VccRTC	AC11						
Vcc1_5_A_33	U11	Vcc3_3_13	H1	VccSus3_3_9	E26	VccRTC	AC12						
Vcc1_5_A_34	U12	Vcc3_3_14	H7	VccSus3_3_10	AA10	VccRTC	AC13						
Vcc1_5_A_35	U14	Vcc3_3_15	J7	VccSus3_3_11	AG10	VccRTC	AC14						
Vcc1_5_A_36	U16	Vcc3_3_16	L4	VccSus3_3_12	L7	VccRTC	AC15						
Vcc1_5_A_37	U17	Vcc3_3_17	M7	VccSus3_3_13	L17	VccRTC	AC16						
Vcc1_5_A_38	G8	Vcc3_3_18	M7	VccSus3_3_14	B17	VccRTC	AC17						
Vcc1_5_A_39	D24	Vcc3_3_19	P1	VccSus3_3_15	C16	VccRTC	AC18						
Vcc1_5_A_40	D25	Vcc3_3_20	E26	VccSus3_3_16	C17	VccRTC	AC19						
Vcc1_5_A_41	D26	Vcc3_3_21	E26	VccSus3_3_17	D16	VccRTC	AC20						
Vcc1_5_A_42	D27	Vcc3_3_22	AA10	VccSus3_3_18	F16	VccRTC	AC21						
Vcc1_5_A_43	E20			VccSus3_3_19	F15	VccRTC	AC22						
Vcc1_5_A_44	E21			VccSus3_3_20	F18	VccRTC	AC23						
Vcc1_5_A_45	E22				F18	VccRTC	AC24						
Vcc1_5_A_46	E23				G15	VccRTC	AC25						
Vcc1_5_A_47	E24				G16	VccRTC	AC26						
Vcc1_5_A_48	E25				G17	VccRTC	AC27						
Vcc1_5_A_49	F20				G18	VccRTC	AC28						
Vcc1_5_A_50	G20				G18	VccRTC	AC29						
Vcc1_5_A_51	G20				A24	VccRTC	AC30						
Vcc1_5_A_52	F9					VccRTC	AC31						

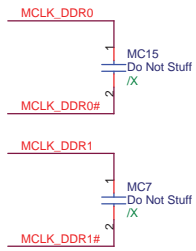
P900_R1.0G_W/O_FLASH

ASUS Title: ICH6-M_PWR_GND

ASUSTek Computer INC. Engineer: Tiansen_Wu

Size	Project Name	Rev
A3	P900	1.2G

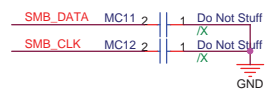
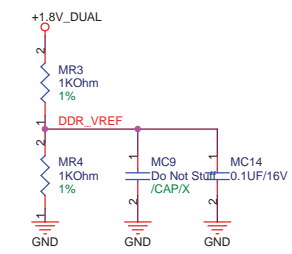
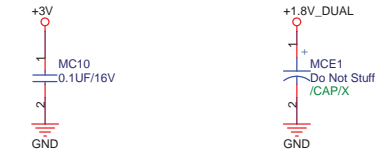
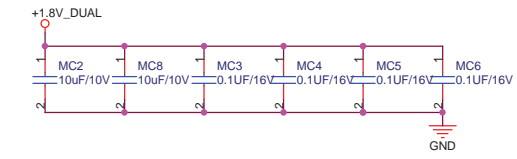
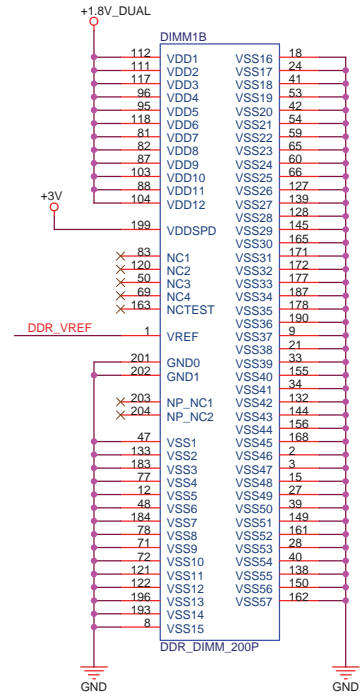
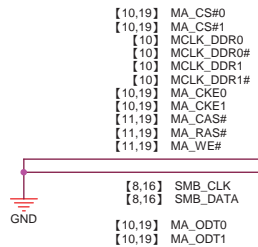
Date: Wednesday, February 27, 2008 Sheet 17 of 47



STD Type



DIMM1A		DIMM1B	
MA_MA0	102	A0	DQ0
MA_MA1	101	A1	DQ1
MA_MA2	100	A2	DQ2
MA_MA3	99	A3	DQ3
MA_MA4	98	A4	DQ4
MA_MA5	97	A5	DQ5
MA_MA6	94	A6	DQ6
MA_MA7	93	A7	DQ7
MA_MA8	91	A8	DQ8
MA_MA9	91	A9	DQ9
MA_MA10	105	A10/AP	DQ10
MA_MA11	90	A11	DQ11
MA_MA12	89	A12	DQ12
MA_MA13	116	A13	DQ13
	86	A14	DQ14
	84	A15	DQ15
	85	A16_BA2	DQ16
MA_BA2	107	BA0	DQ17
MA_BA0	106	BA1	DQ18
MA_BA1	110	S0#	DQ19
	115	S1#	DQ20
	30	CK0#	DQ21
	32	CK1#	DQ22
	164	CKE0	DQ23
	166	CKE1	DQ24
	79	CAS#	DQ25
	80	RAS#	DQ26
	113	WE#	DQ27
	108	SA0	DQ28
	109	SA1	DQ29
	200	SCL	DQ30
	197	SDA	DQ31
	195	ODT0	DQ32
	114	ODT1	DQ33
	119	DM0	DQ34
	10	DM1	DQ35
	26	DM2	DQ36
	52	DM3	DQ37
	67	DM4	DQ38
	130	DM5	DQ39
	147	DM6	DQ40
	170	DM7	DQ41
	185	DM8	DQ42
	13	DM9	DQ43
	31	DM10	DQ44
	51	DM11	DQ45
	70	DM12	DQ46
	131	DM13	DQ47
	148	DM14	DQ48
	169	DM15	DQ49
	188	DM16	DQ50
	11	DM17	DQ51
	29	DM18	DQ52
	49	DM19	DQ53
	68	DM20	DQ54
	129	DM21	DQ55
	146	DM22	DQ56
	167	DM23	DQ57
	186	DM24	DQ58
		DM25	DQ59
		DM26	DQ60
		DM27	DQ61
		DM28	DQ62
		DM29	DQ63



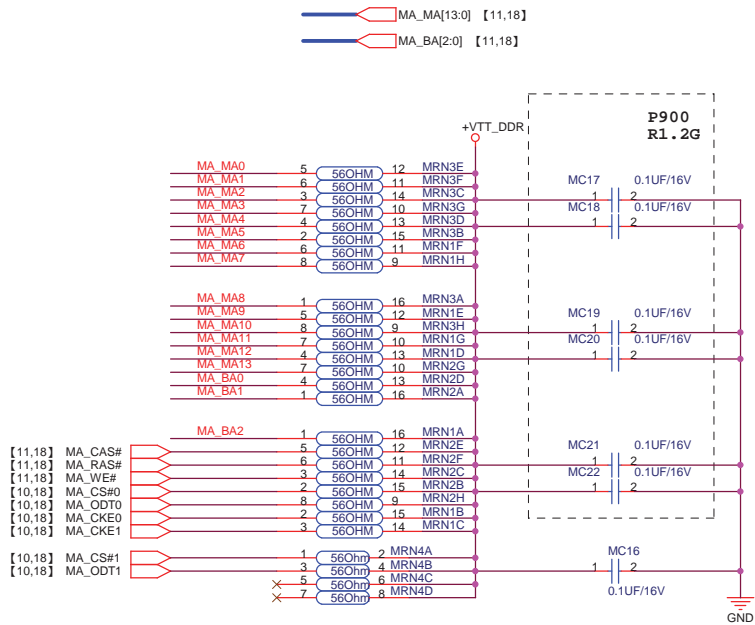
P900_R1.1G_WO_FLASH

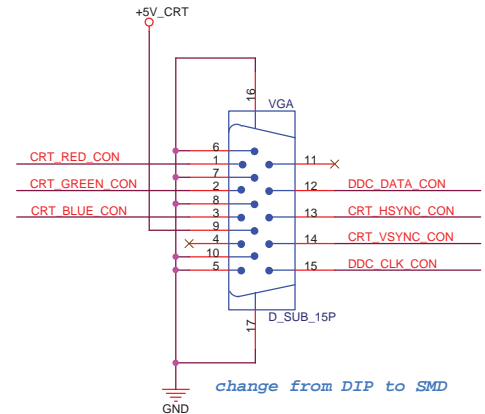
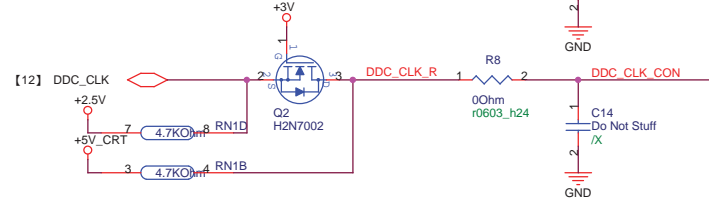
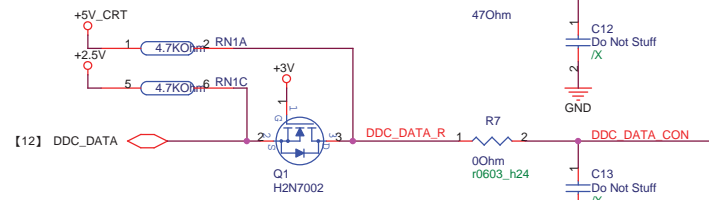
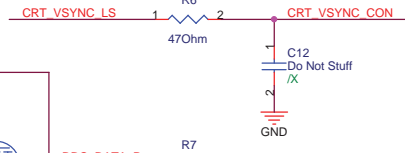
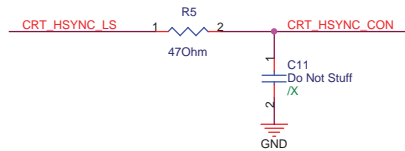
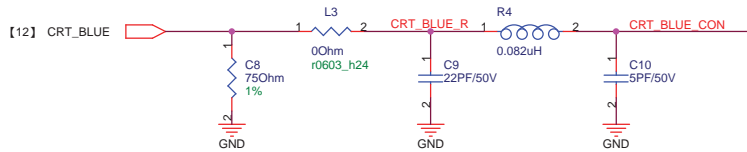
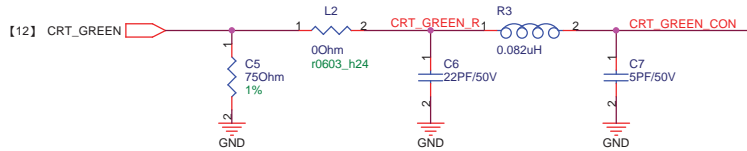
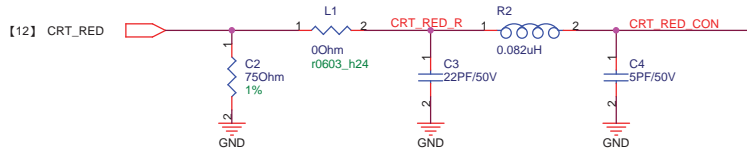
ASUS Title: DDR2 SODIMM

ASUSTek Computer INC. Engineer: Tiansen_Wu

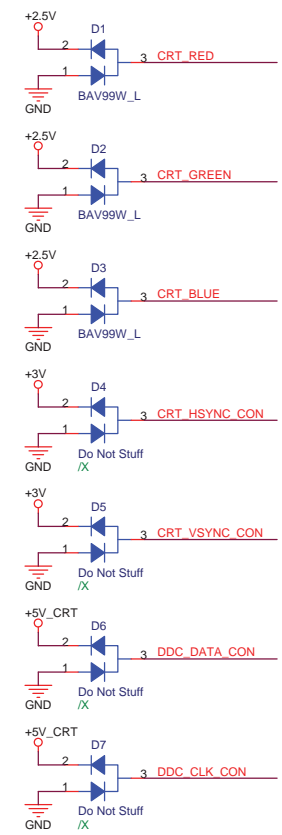
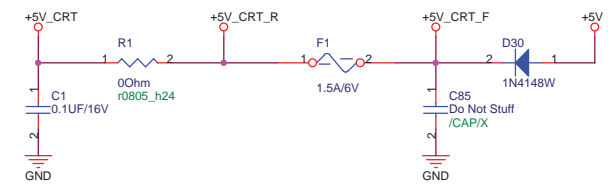
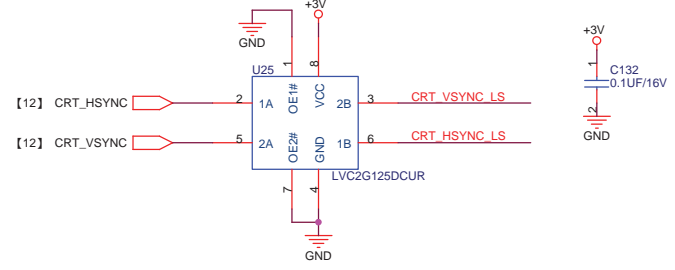
Size	Project Name	Rev
A3	P900	1.2G

Date: Wednesday, February 27, 2008 Sheet 18 of 47



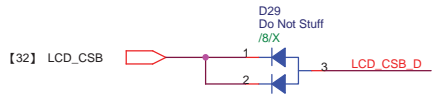


VGA use 12G10110015W & 12G10110015N

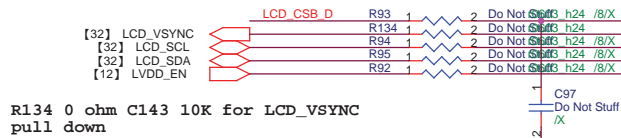


P900_R1.1G_WO_FLASH

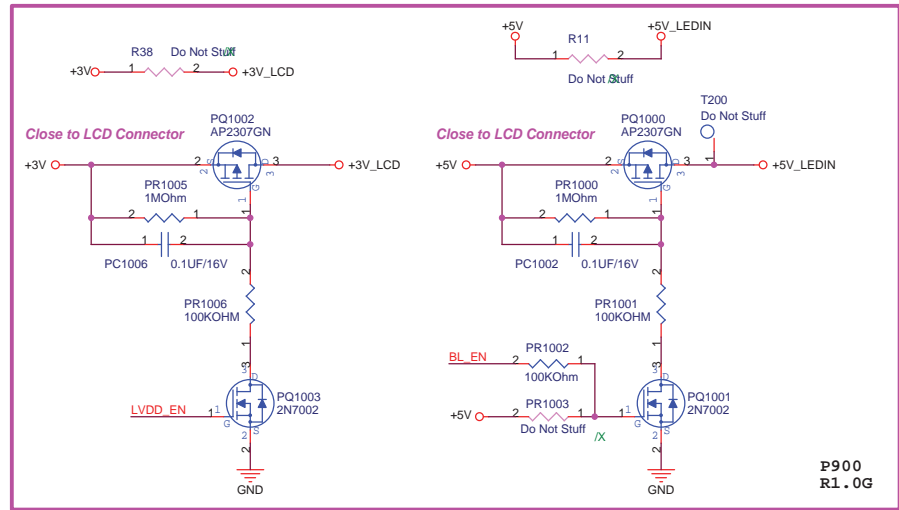
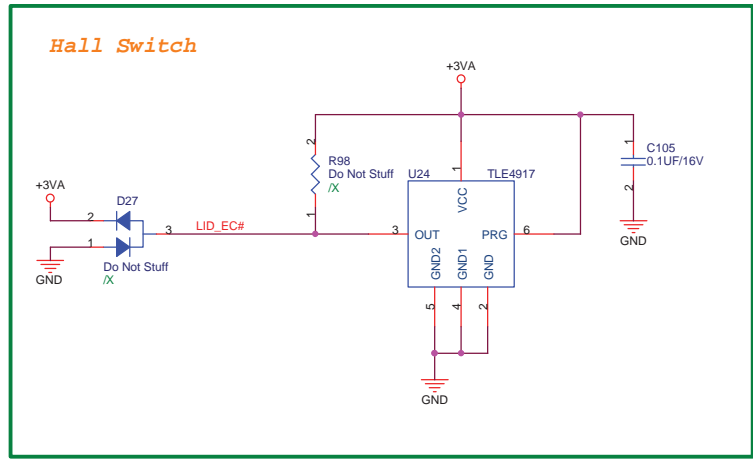
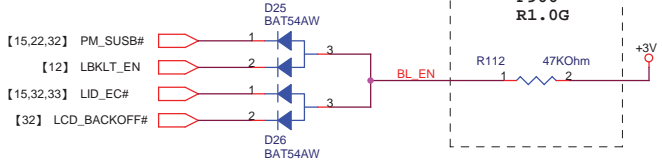
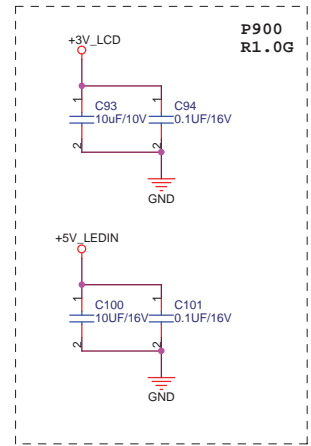
ASUS		Title : Onboard VGA	
ASUSTek Computer INC.		Engineer: Tiansen_Wu	
Size	Project Name		Rev
A3	P900		1.2G
Date: Wednesday, February 27, 2008	Sheet	20 of 47	



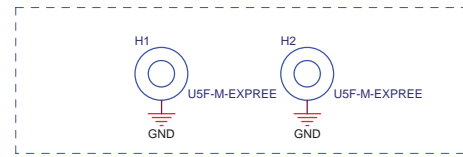
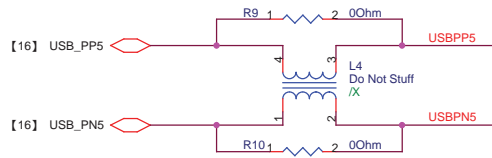
Remove R134 for LCD Board 1.4G, need rework



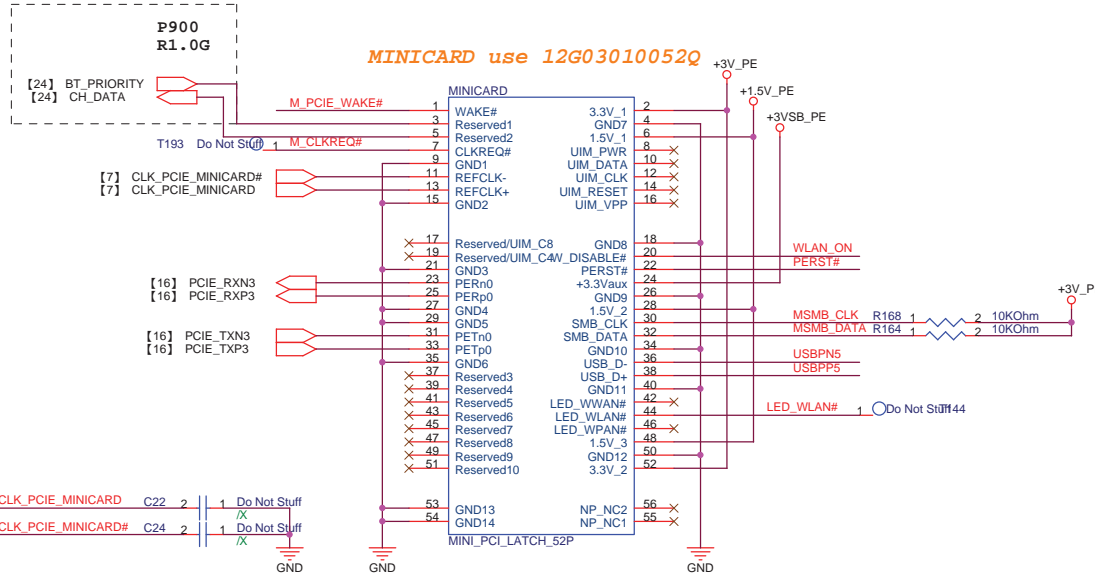
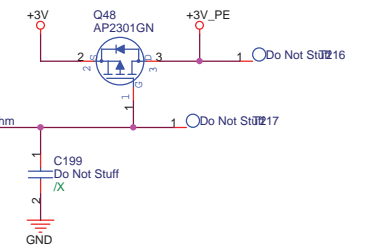
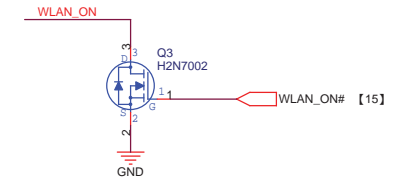
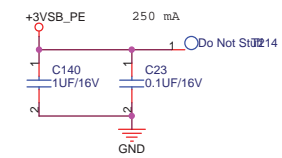
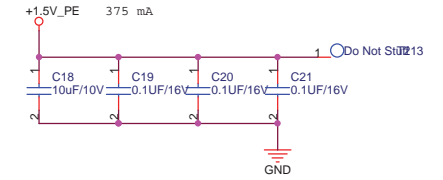
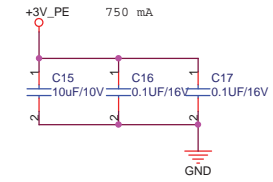
LCD_CON use 12G171040204



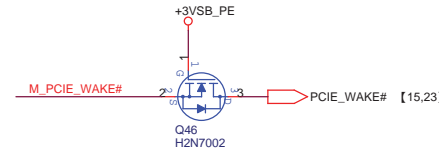
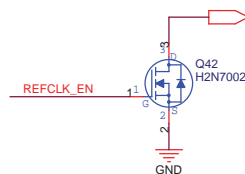
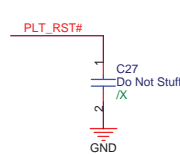
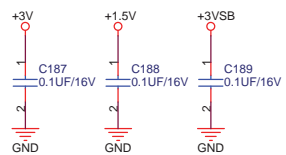
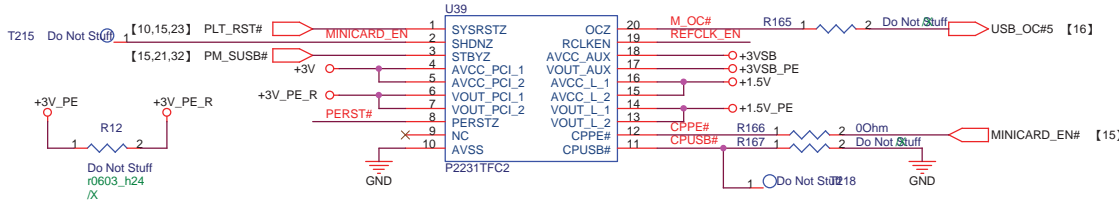
ASUS		Title : LCD Conn	
ASUSTek Computer INC.		Engineer: Tiansen_Wu	
Size	Project Name	Rev	
A3	P900	1.2G	
Date: Wednesday, February 27, 2008	Sheet	21	of 47



MINI CARD NUT(1.6mm) *2

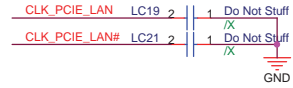
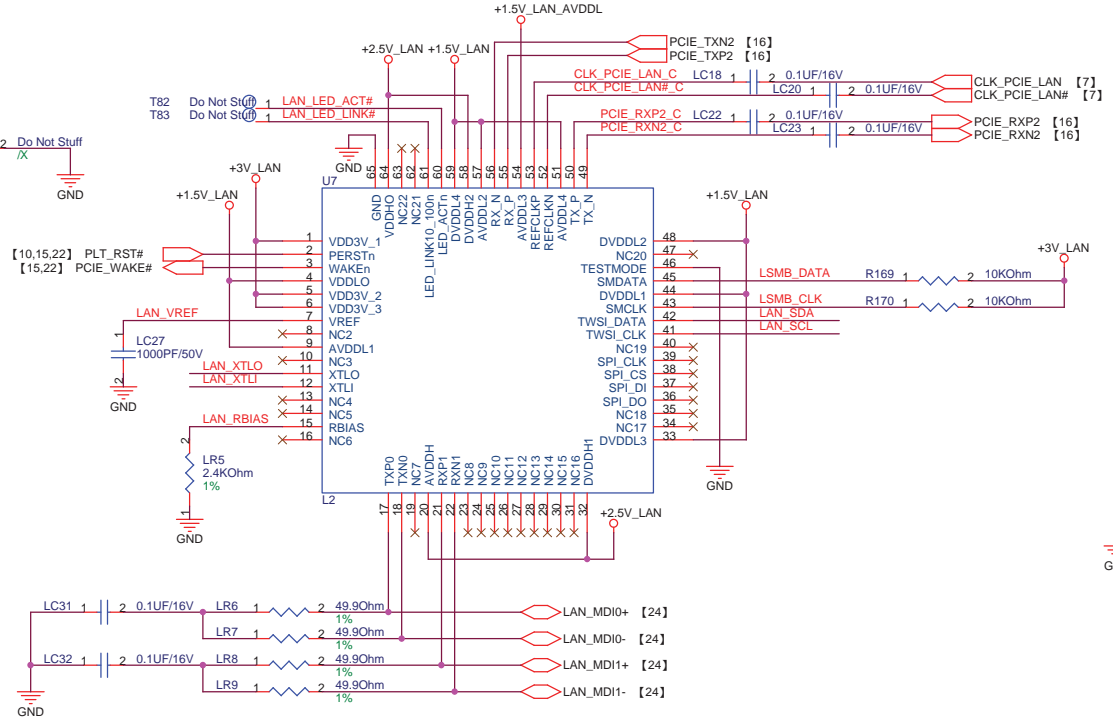
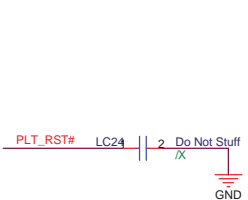
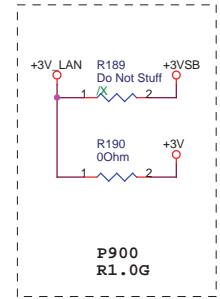
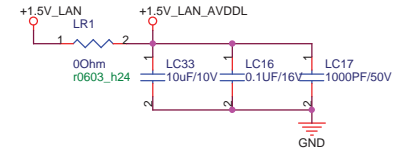
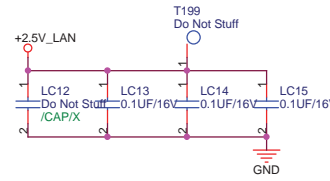
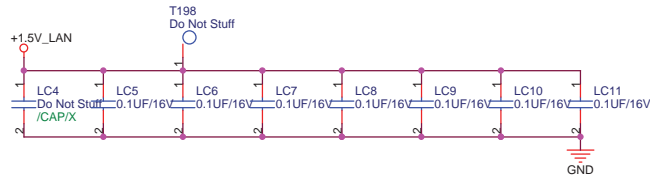
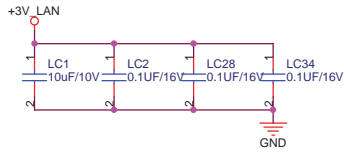


U39 use 06G030057011

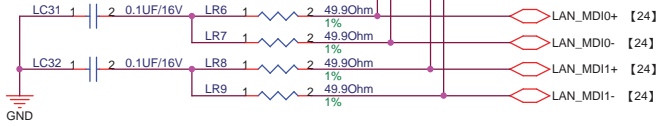
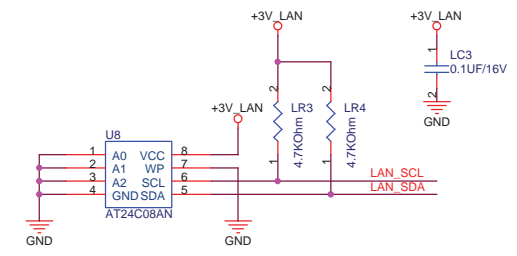
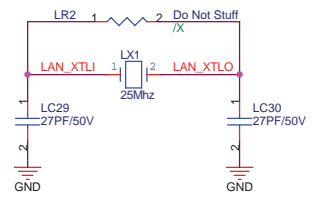


P900_R1.1G_WO_FLASH

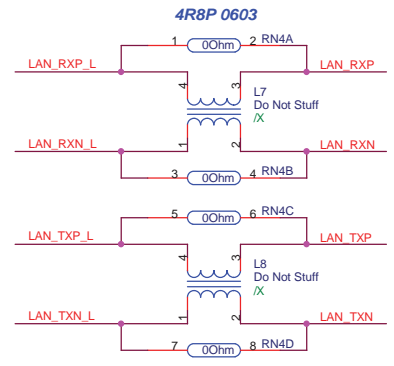
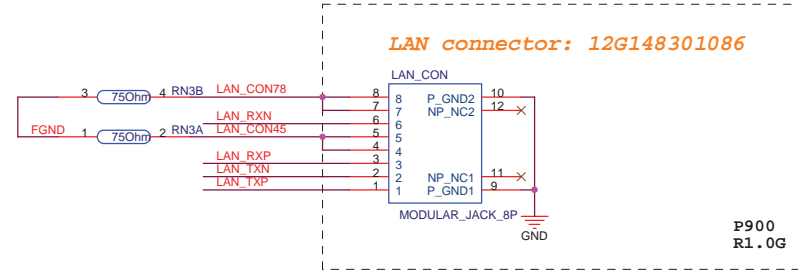
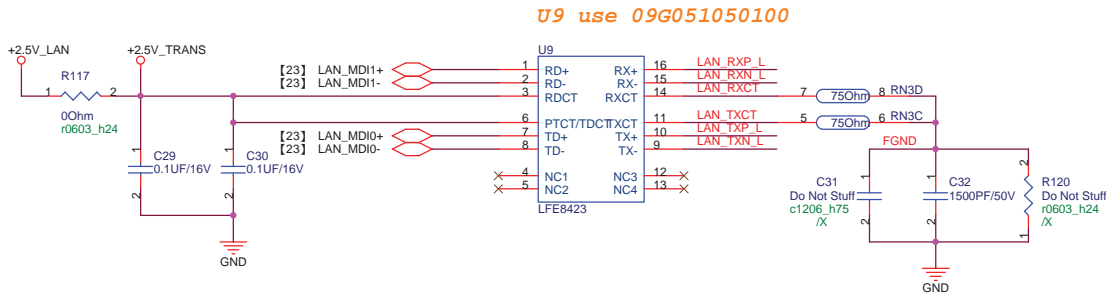
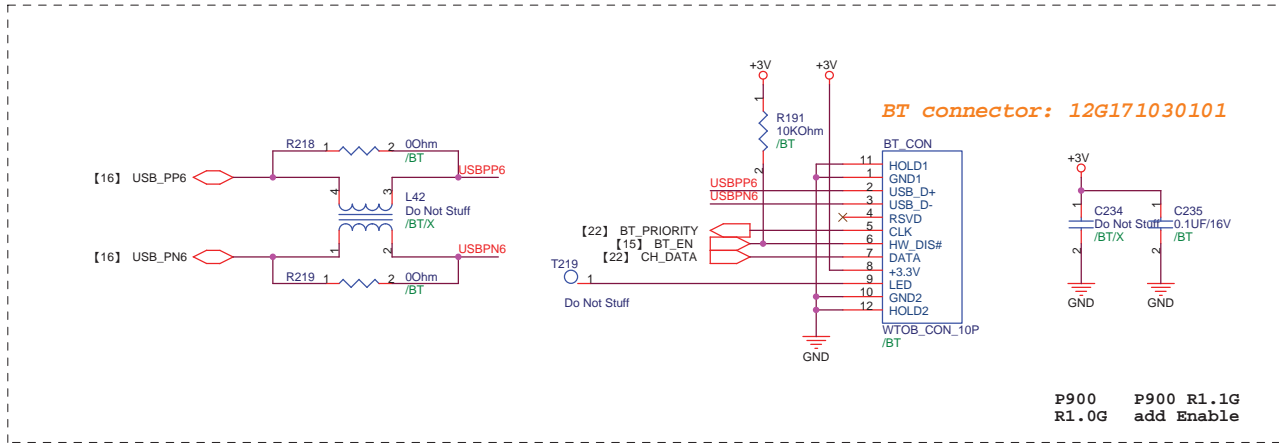
ASUS		Title : Minicard	
ASUSTek Computer INC.		Engineer: Tiansen_Wu	
Size A3	Project Name P900	Rev 1.2G	
Date: Wednesday, February 27, 2008		Sheet	22 of 47



LX1 use 07G010212502

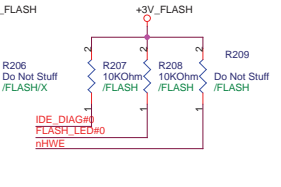
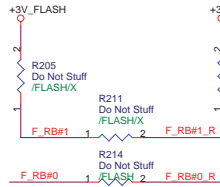
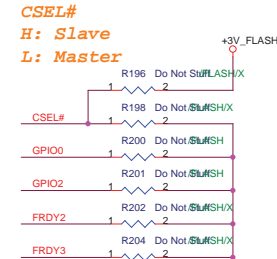
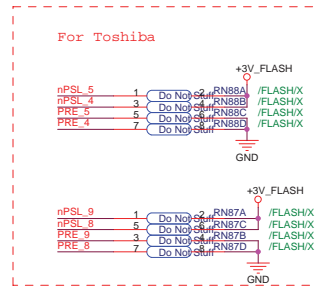
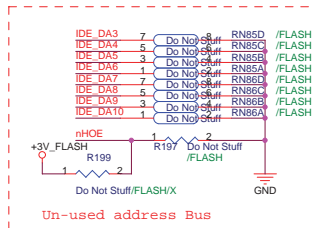
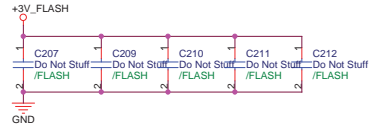
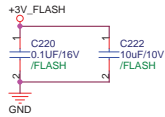
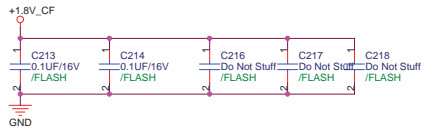


P900_R1.1G_WO_FLASH		Title : LAN_Atheros L2	
ASUSTek Computer INC.		Engineer: Tiansen_Wu	
Size	Project Name	Rev	
A3	P900	1.2G	
Date: Wednesday, February 27, 2008	Sheet 23 of 47		



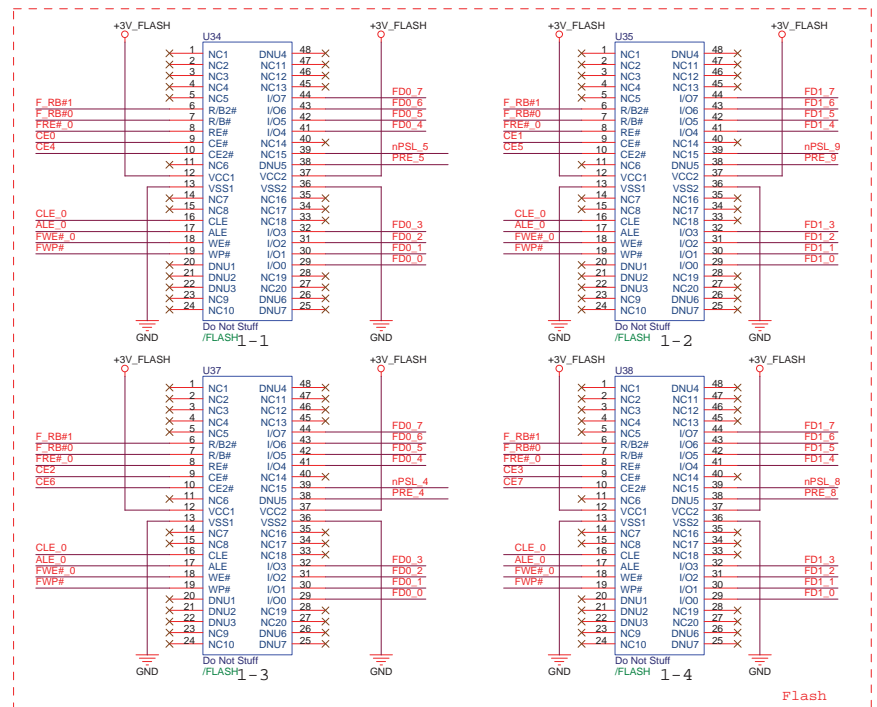
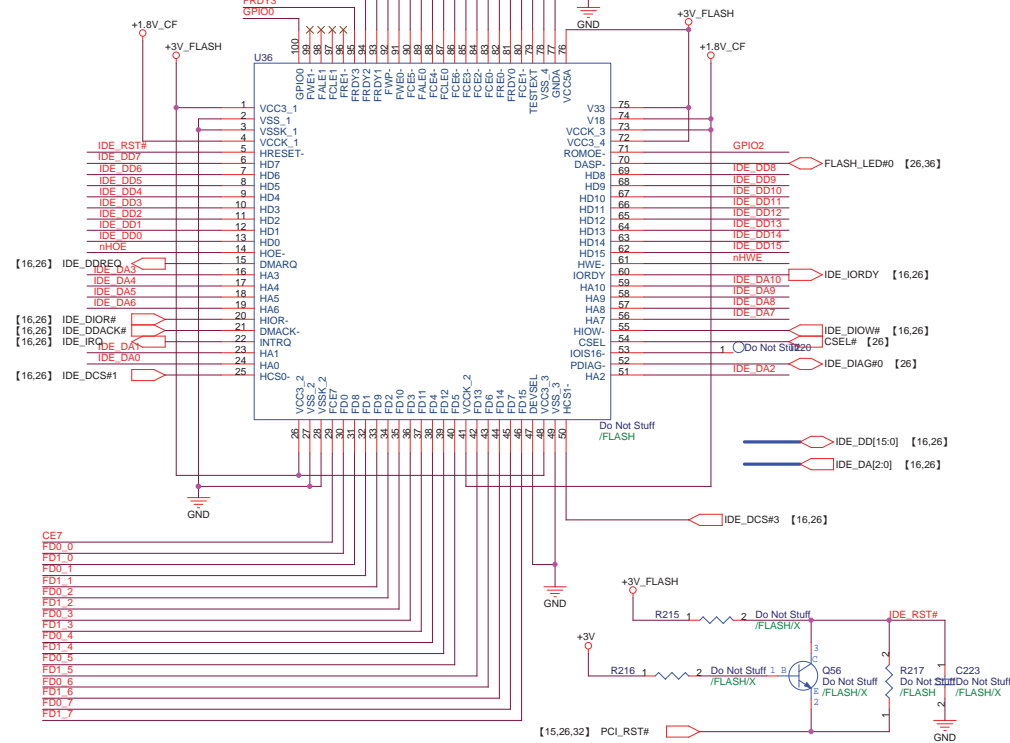
P900_R1.1G_WO_FLASH

ASUS		Title : RJ45/BlueTooth	
ASUSTek Computer INC.		Engineer: <i>Tiansen_Wu</i>	
Size	Project Name		Rev
A3	P900		1.2G
Date: Wednesday, February 27, 2008		Sheet	24 of 47

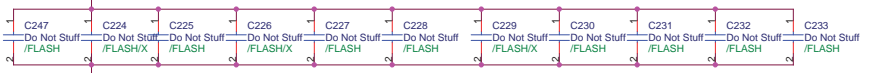


1. 1C: R203
2. 2C: R203, R210

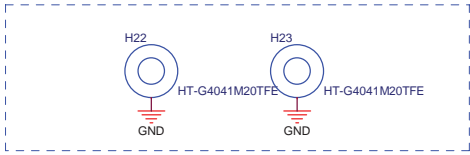
U36: USE 02G113000302



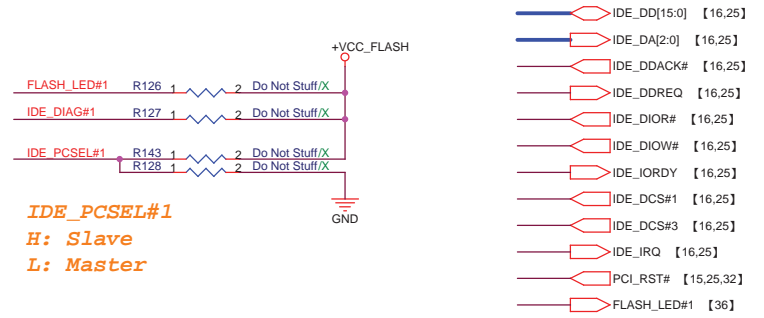
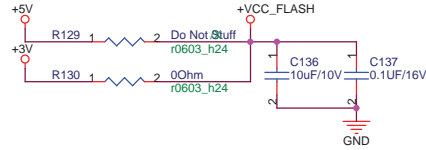
Near to Flash VCC1 PIN



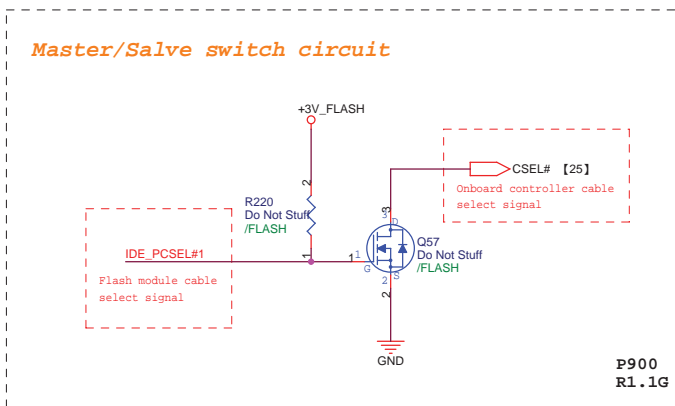
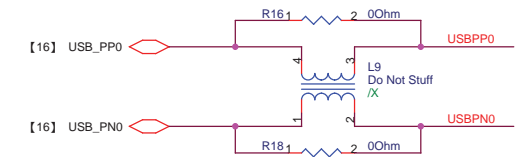
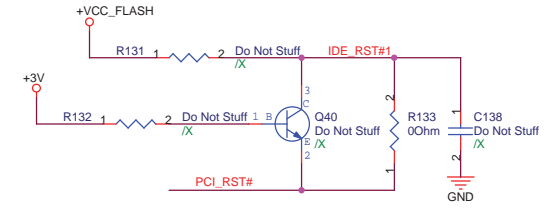
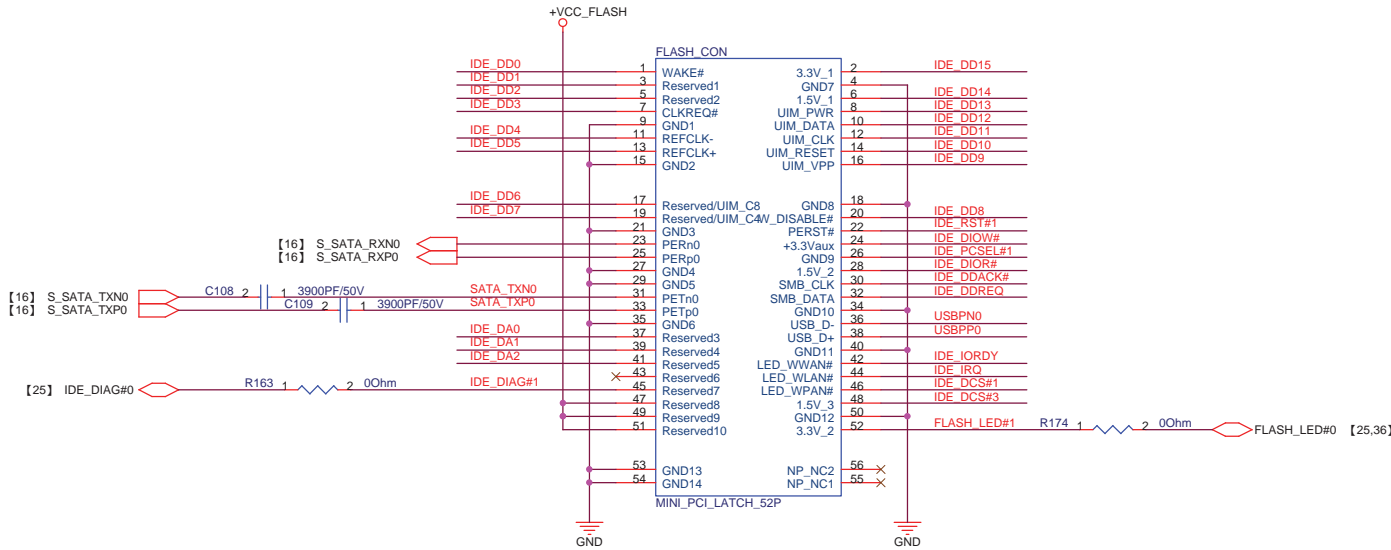
P900_R1.1G_W/O_FLASH		Title : Onboard Flash	
ASUSTek Computer INC.		Engineer: Tiansen_Wu	
Size	Project Name	P900	Rev 1.2G
Custom			
Date: Wednesday, February 27, 2008	Sheet 25 of 47		



FLASH CARD NUT(3.3mm) *2



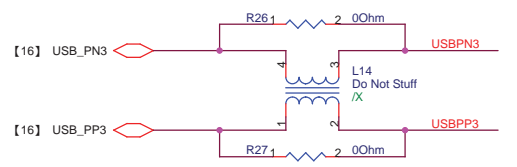
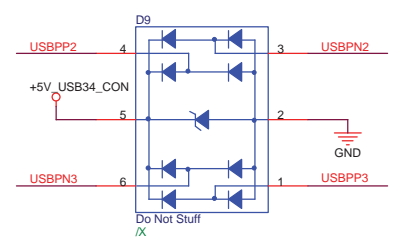
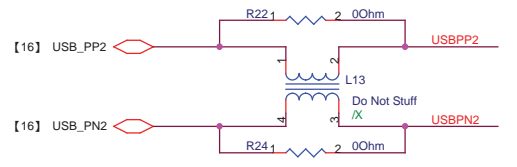
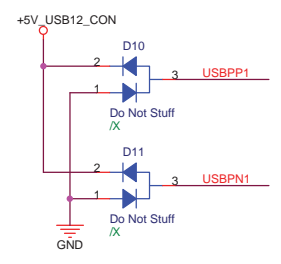
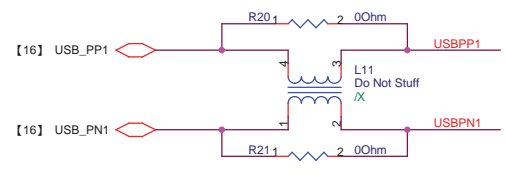
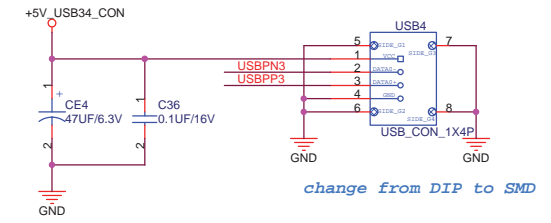
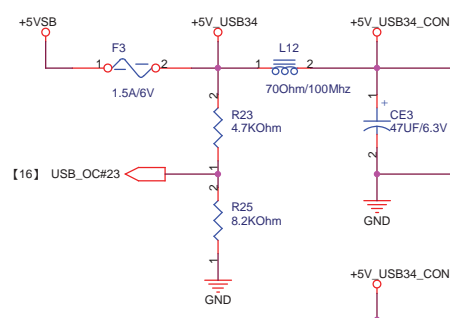
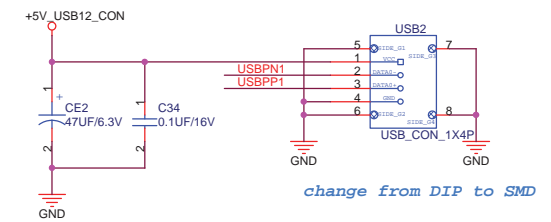
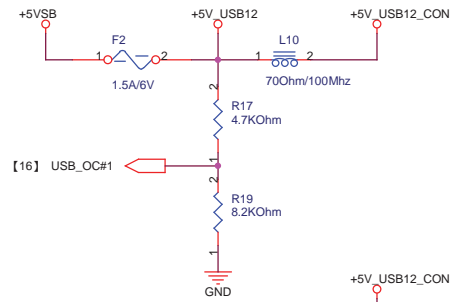
IDE_PCSEL#1
H: Slave
L: Master



P900
R1.1G

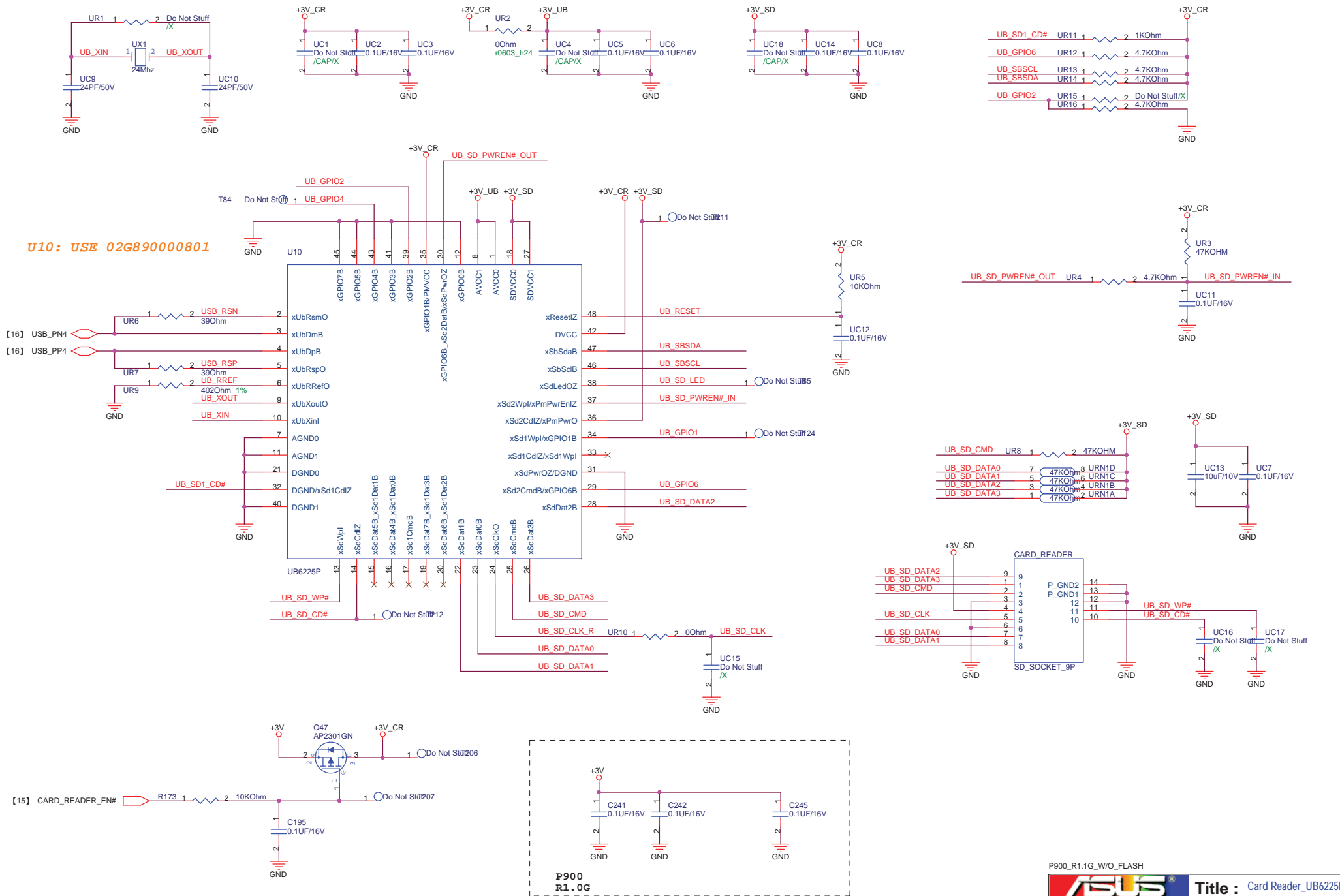
P900_R1.1G_WO_FLASH

ASUS		Title : Flash Conn	
ASUSTek Computer INC.		Engineer: <i>Tiansen_Wu</i>	
Size A3	Project Name P900	Rev 1.2G	
Date: Wednesday, February 27, 2008		Sheet	26 of 47



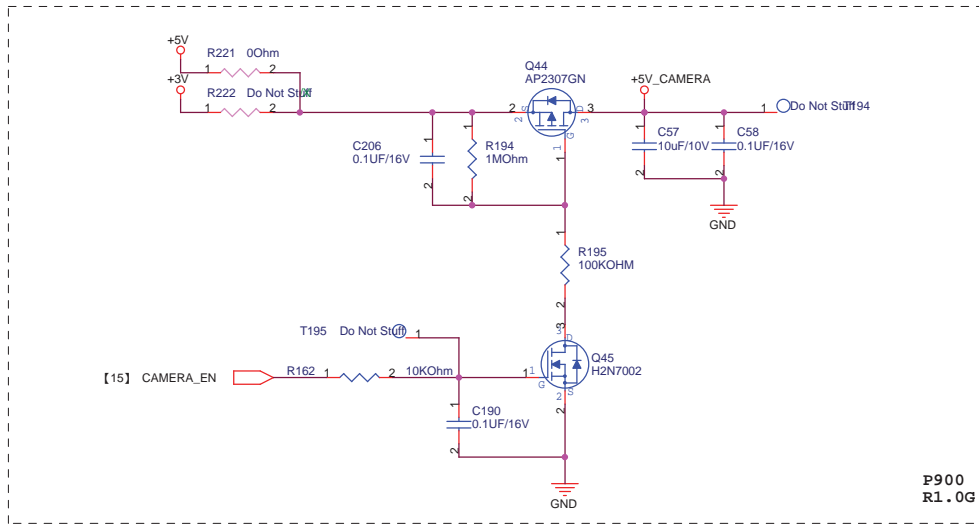
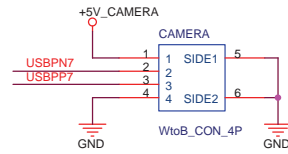
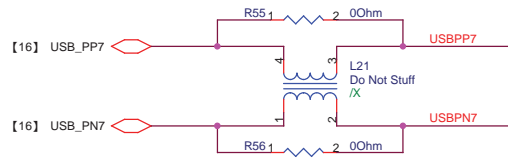
P900_R1.1G_WO_FLASH

ASUS		Title : USB Port	
ASUSTek Computer INC.		Engineer: <i>Tiansen_Wu</i>	
Size	Project Name	Rev	
A3	P900	1.2G	
Date:	Wednesday, February 27, 2008	Sheet	27 of 47



P900_R1.1G_WO_FLASH

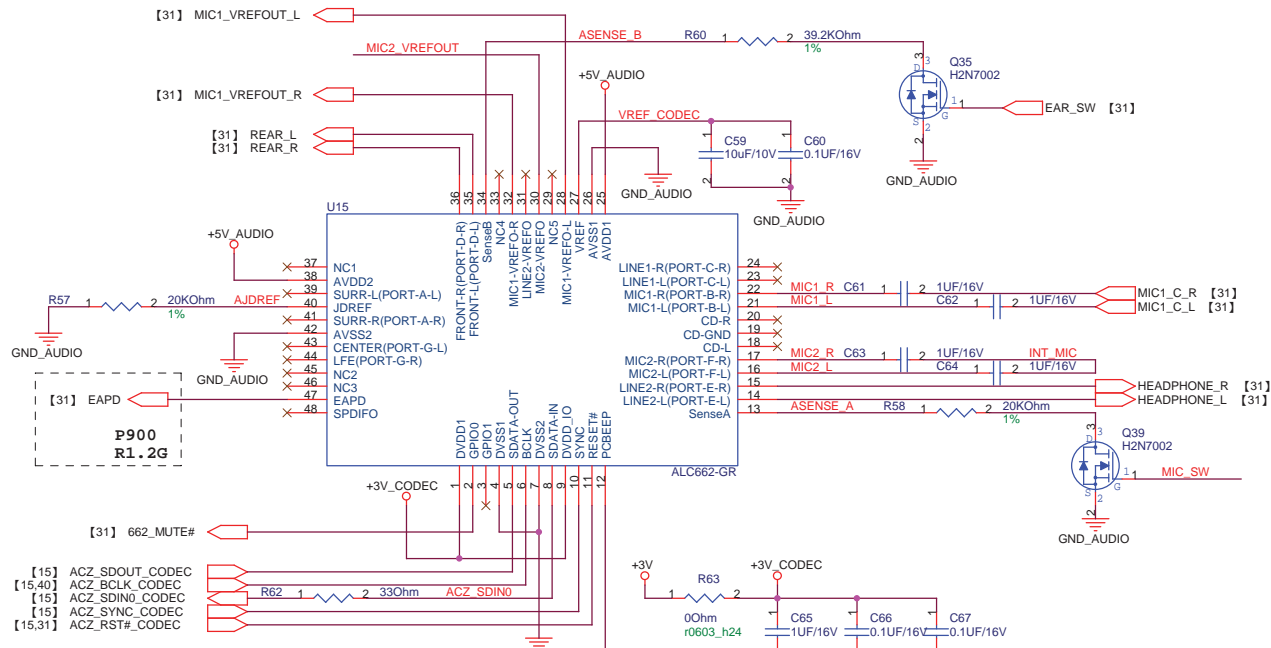
ASUS		Title : Card Reader_UB6225P	
ASUSTek Computer INC.		Engineer: <i>Tiansen_Wu</i>	
Size	Project Name	Rev	
A3	P900		1.2G
Date: Wednesday, February 27, 2008	Sheet 28 of 47		



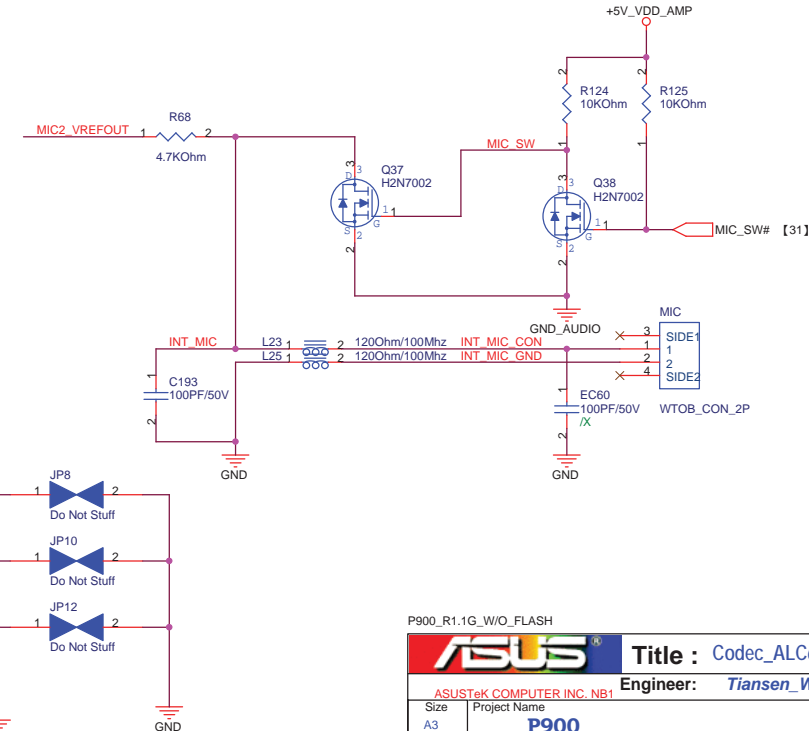
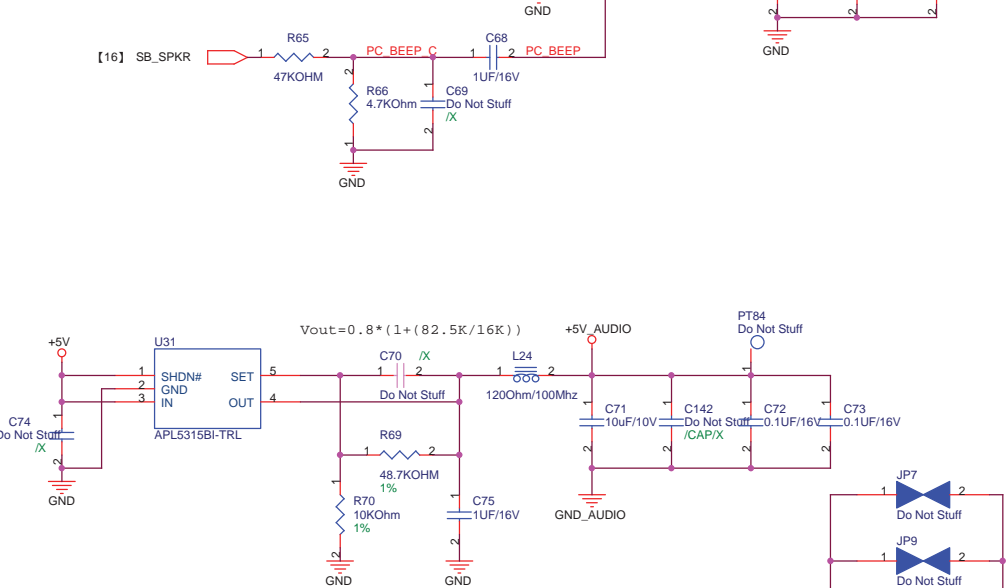
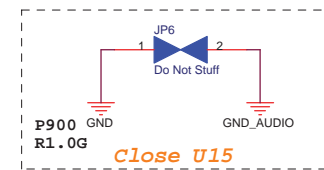
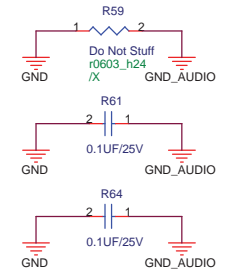
P900
R1.0G

P900_R1.1G_WO_FLASH

ASUS		Title : Camera Conn	
ASUSTek Computer INC.		Engineer: <i>Tiansen_Wu</i>	
Size A3	Project Name P900	Rev 1.2G	
Date: Wednesday, February 27, 2008		Sheet	29 of 47



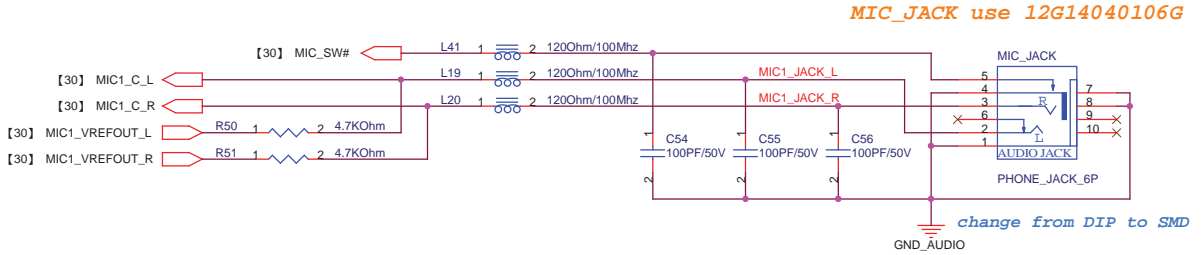
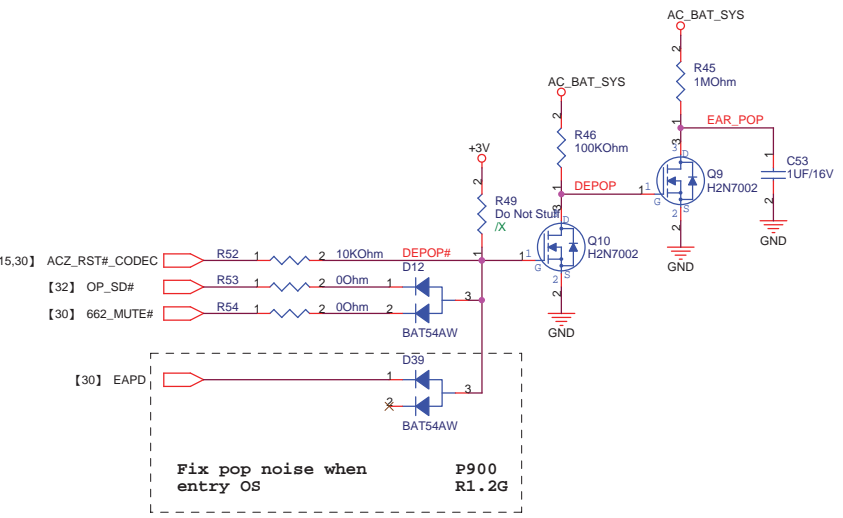
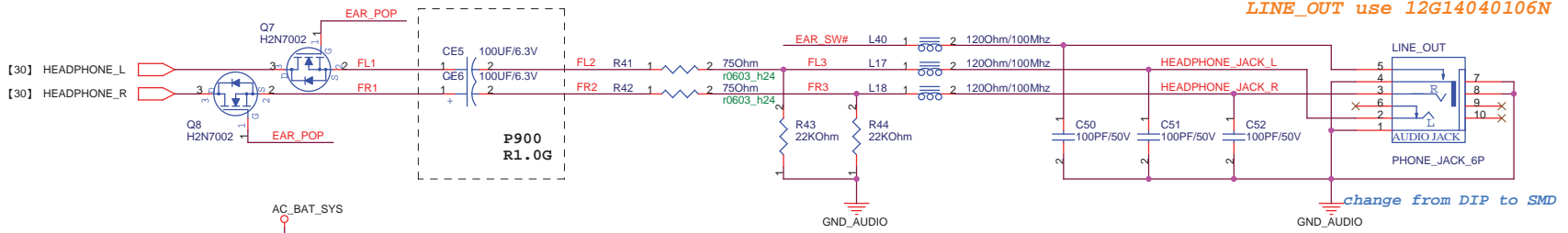
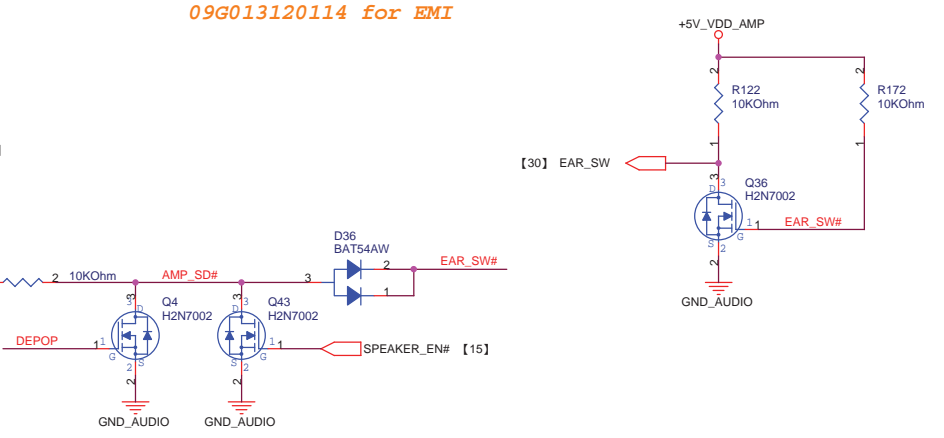
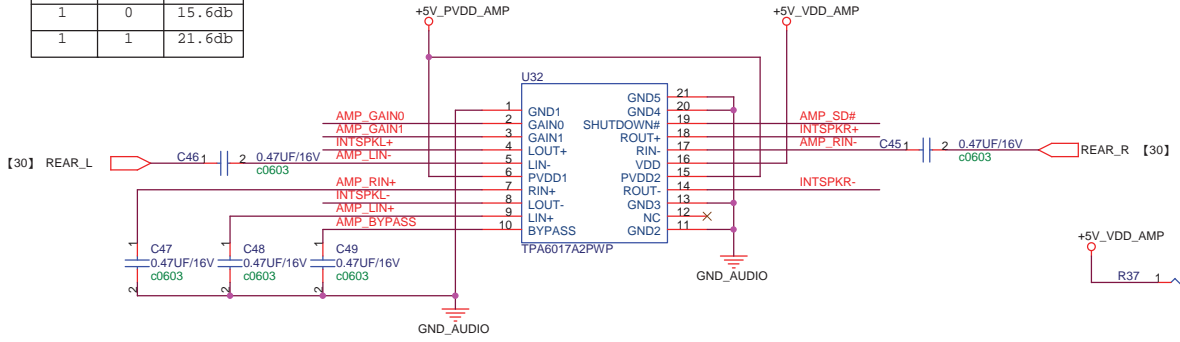
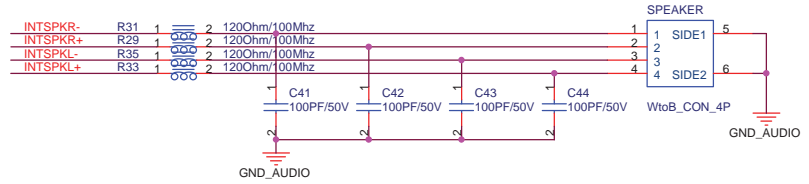
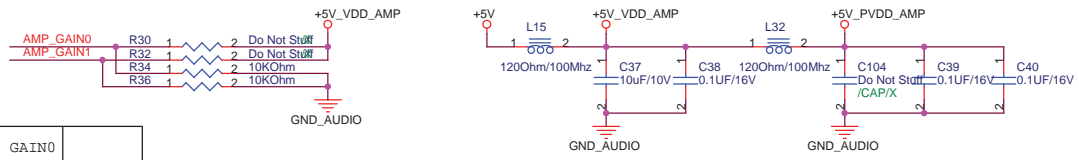
R61, R64 use 0.1UF
11G233310432320 for EMI



P900_R1.1G_WO_FLASH

ASUS		Title : Codec_ALC662	
ASUSTek COMPUTER INC. NB1		Engineer: Tiansen_Wu	
Size	Project Name	Rev	
A3	P900	1.2G	
Date: Wednesday, February 27, 2008	Sheet	30	of 47

GAIN1	GAIN0	
0	0	6db
0	1	10db
1	0	15.6db
1	1	21.6db



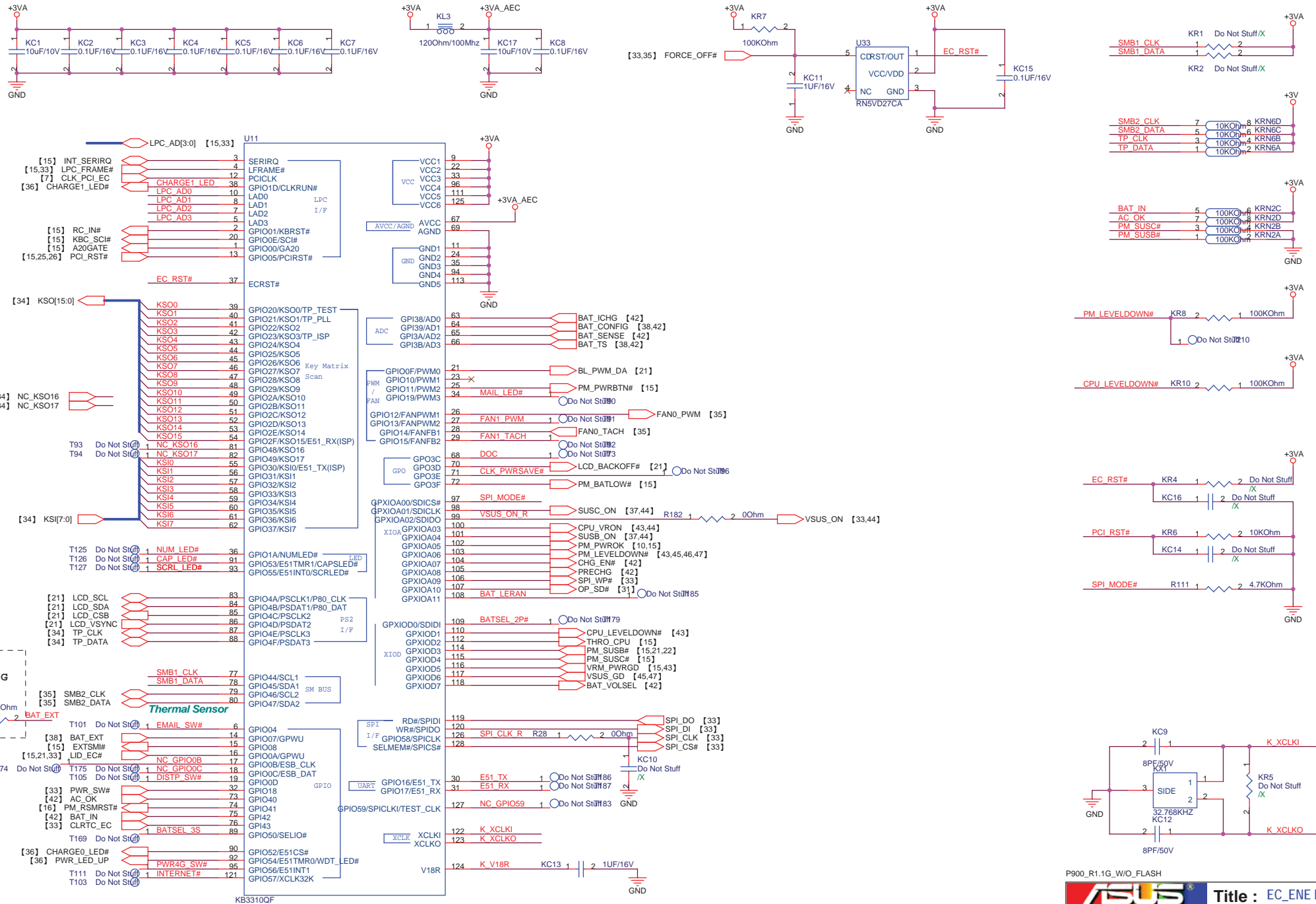
P900_R1.1G_WO_FLASH

ASUS Title : Audio_AMP_Jack

ASUSTek Computer INC. Engineer: Tiansen_Wu

Size	Project Name	Rev
A3	P900	1.2G

Date: Wednesday, February 27, 2008 Sheet 31 of 47



P900_R1.1G_WO_FLASH

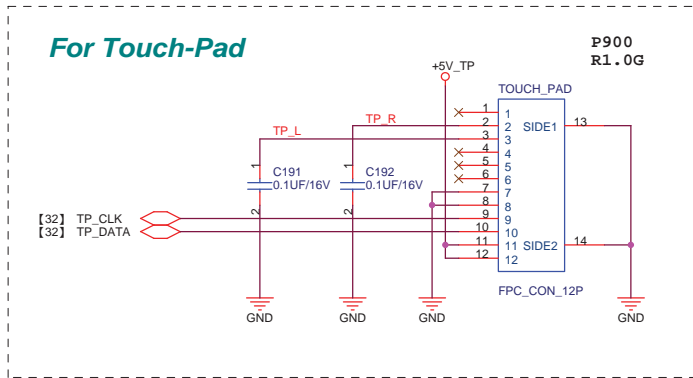
ASUS Title: EC_ENE KB3310

ASUSTek Computer INC. Engineer: Tiansen_Wu

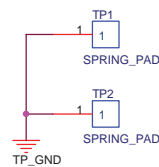
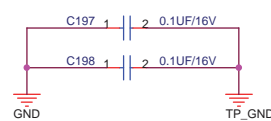
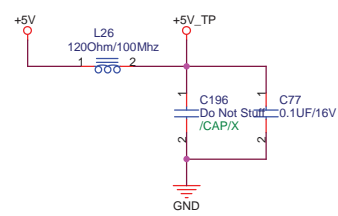
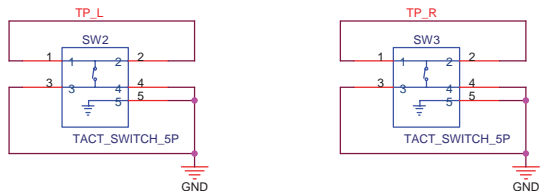
Size	Project Name	Rev
A3	P900	1.2G

Date: Wednesday, February 27, 2008 Sheet 32 of 47

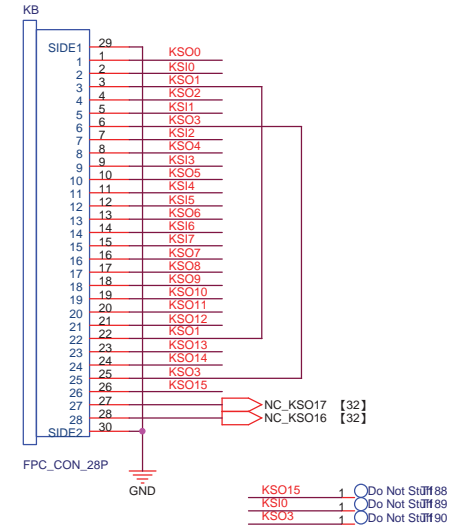
For Touch-Pad



SW2, SW3 use 12G09103305N



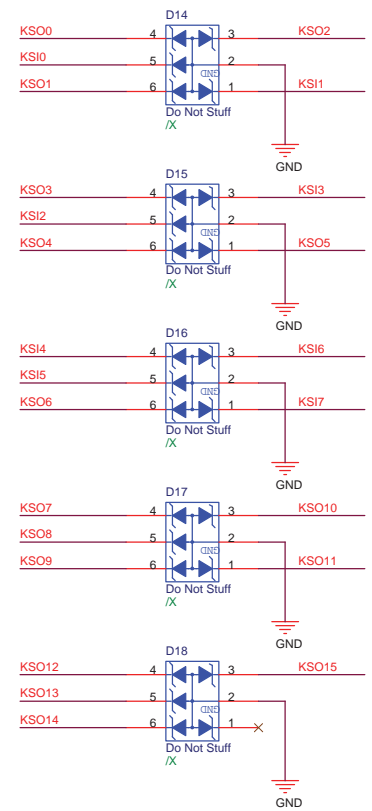
For Keyboard



KSO15 1 Do Not Stuff 88
 KSI0 1 Do Not Stuff 89
 KSO3 1 Do Not Stuff 90

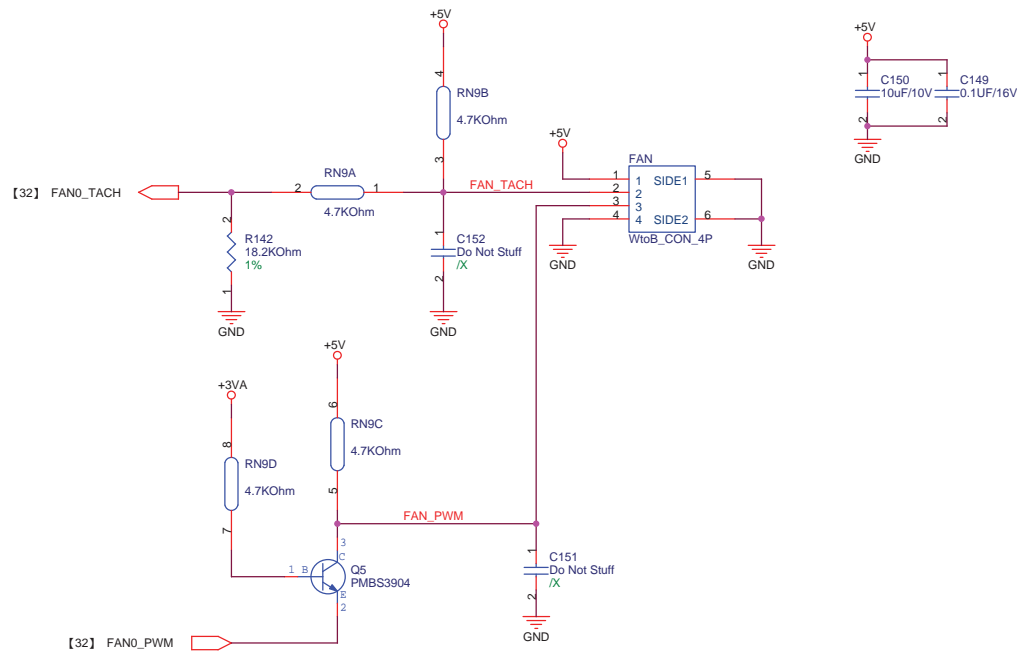
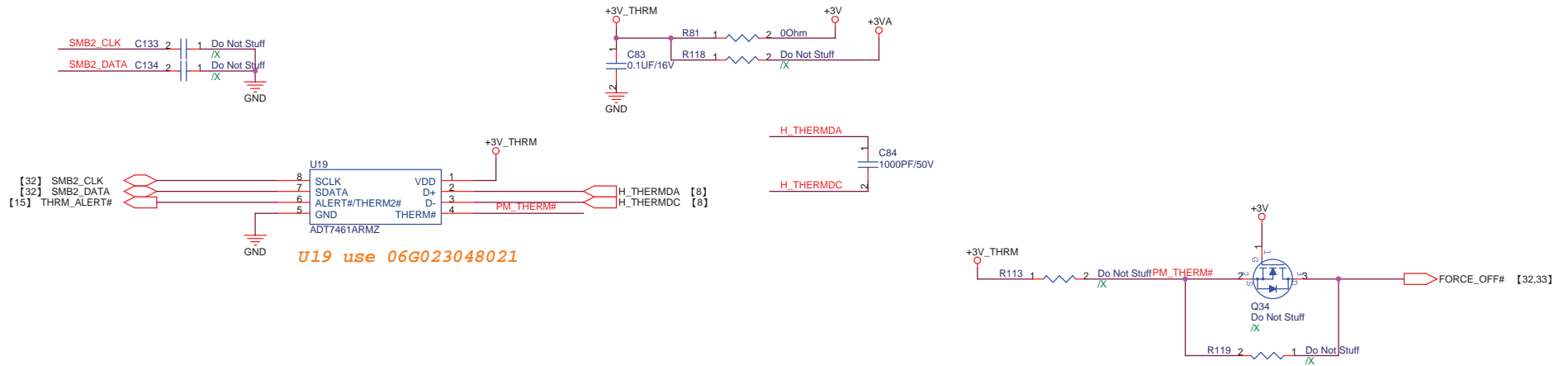


KSO[15:0] [32]
 KSI[7:0] [32]



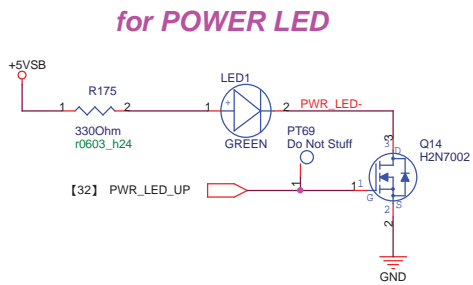
P900_R1.1G_WO_FLASH

ASUS		Title : KB_Touch Pad	
ASUSTek Computer INC.		Engineer: <i>Tiansen_Wu</i>	
Size	Project Name	Rev	
A3	P900	1.2G	
Date: Wednesday, February 27, 2008		Sheet	34 of 47

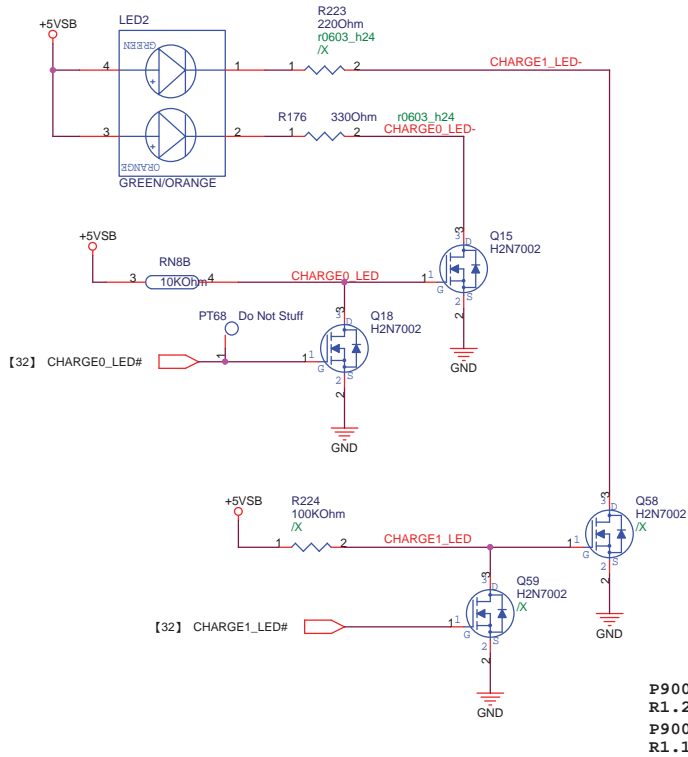


P900_R1.1G_WO_FLASH

ASUS		Title : Thermal Sensor_FAN	
ASUSTek Computer INC.		Engineer: <i>Tiansen_Wu</i>	
Size	Project Name	Rev	
A3	P900	1.2G	
Date: Wednesday, February 27, 2008	Sheet	35	of 47

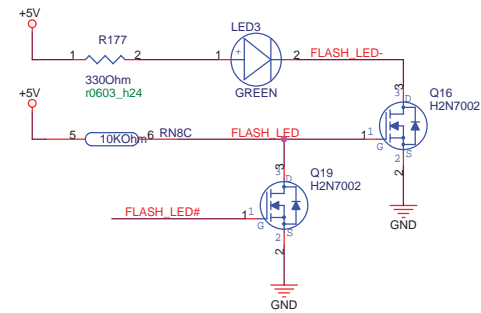


for CHARGE LED

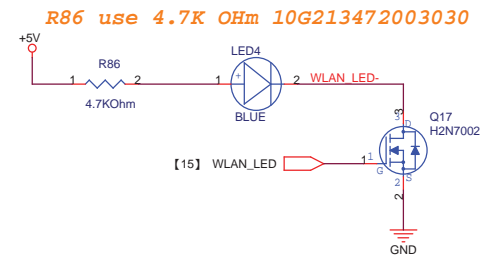


P900
R1.2G
P900
R1.1G

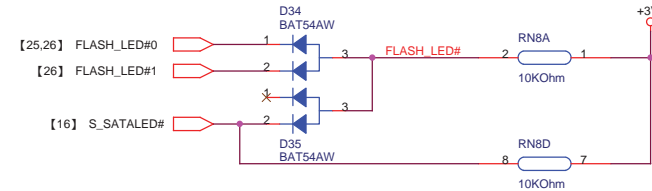
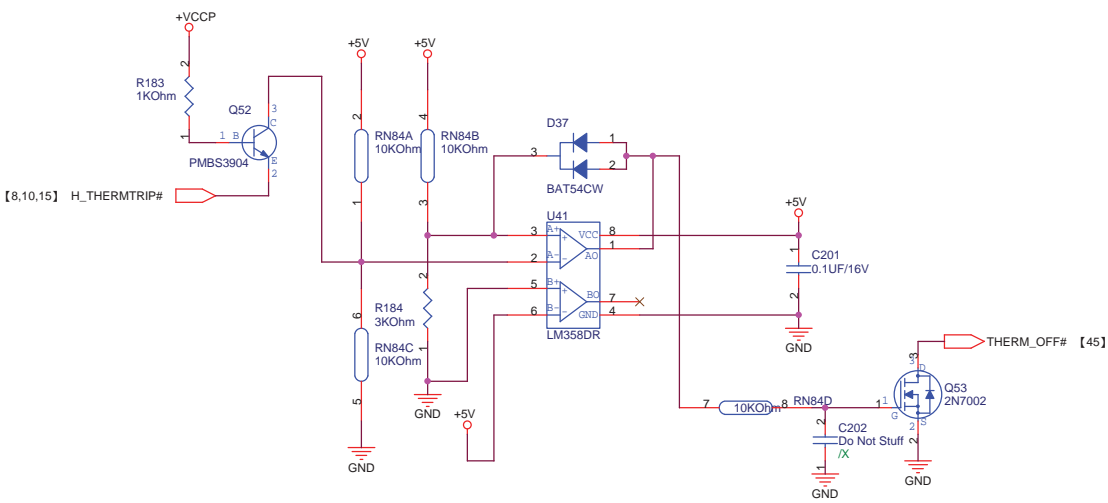
for FLASH LED



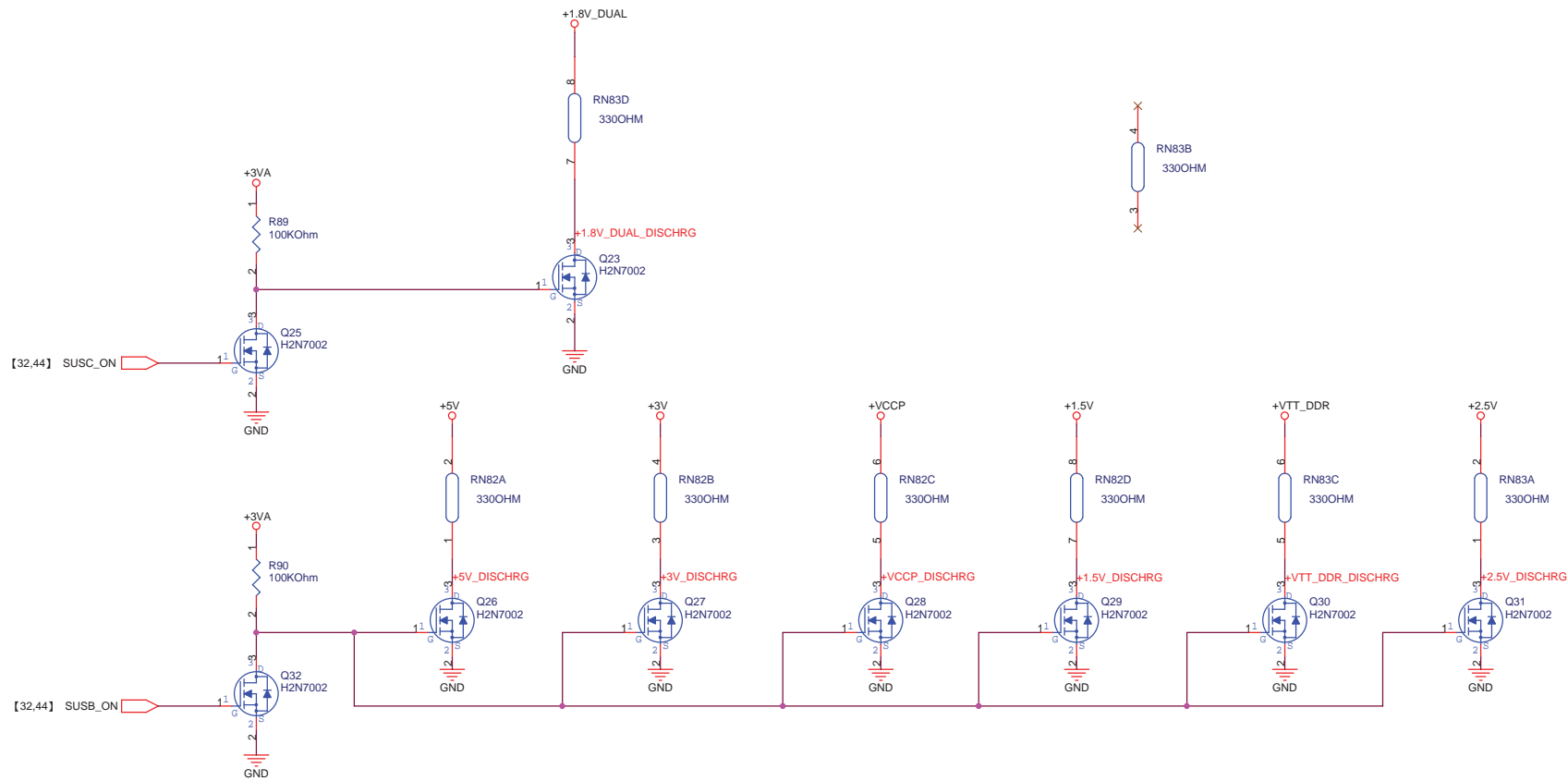
for WLAN LED



For THERMTRIP



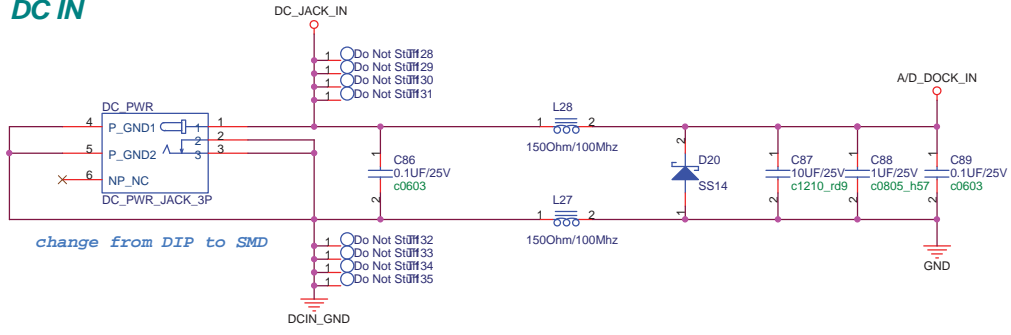
P900_R1.1G_WO_FLASH		ASUS		Title : LED_THERMTRIP	
ASUSTek Computer INC.		Engineer: <i>Tiansen_Wu</i>			
Size	Project Name	Rev			
A3	P900	1.2G			
Date: Wednesday, February 27, 2008	Sheet	36	of	47	



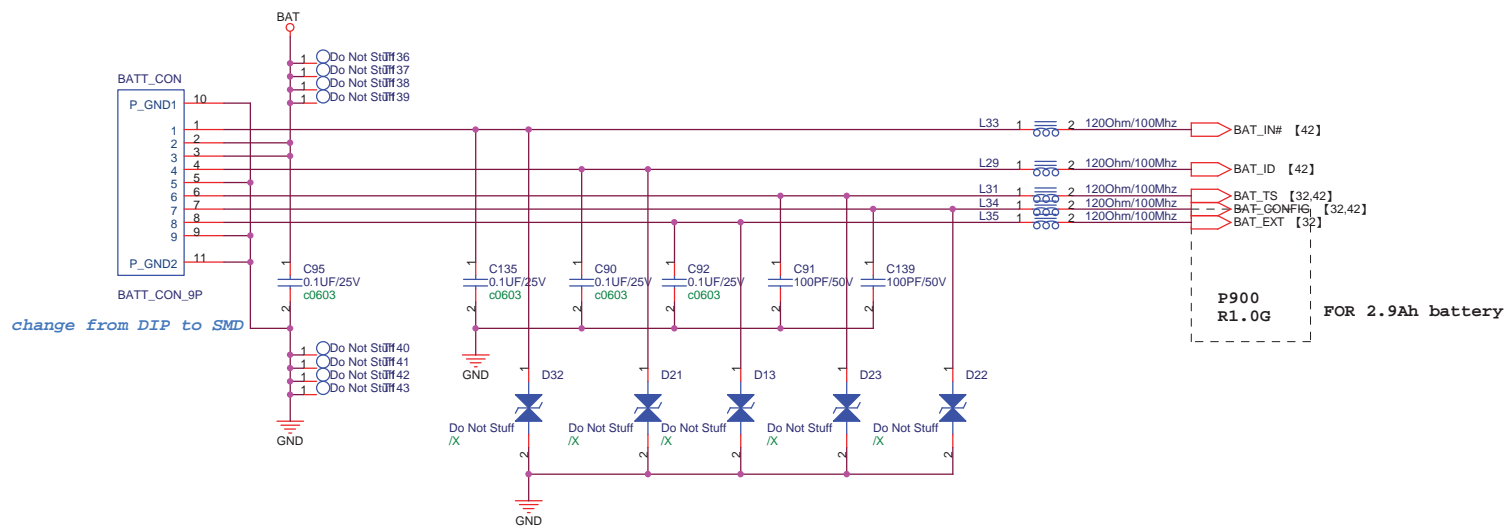
P900_R1.1G_WO_FLASH

ASUS		Title : Discharge	
ASUSTek Computer INC.		Engineer: <i>Tiansen_Wu</i>	
Size	Project Name	Rev	
A3	P900	1.2G	
Date: Wednesday, February 27, 2008	Sheet	37	of 47

DC IN

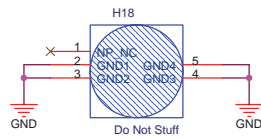
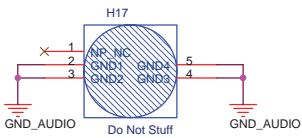
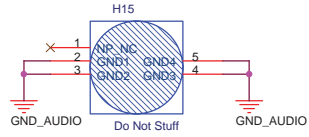
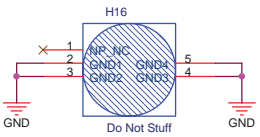
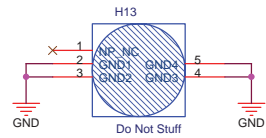
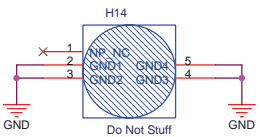
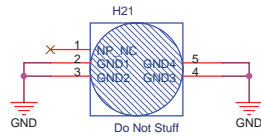
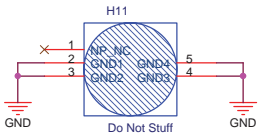
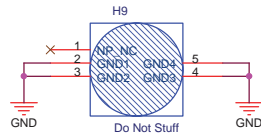
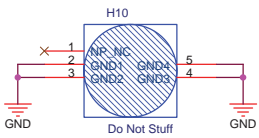
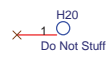
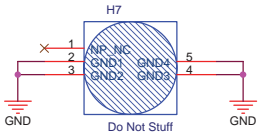
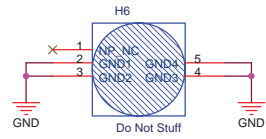
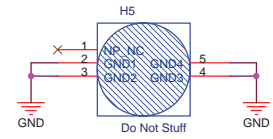


BAT IN



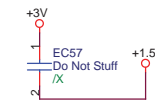
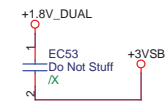
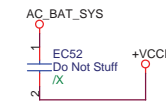
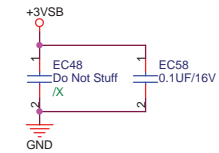
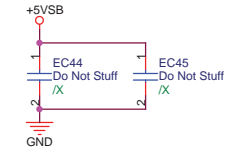
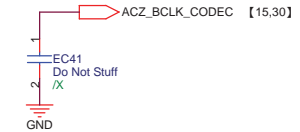
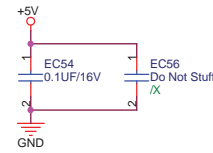
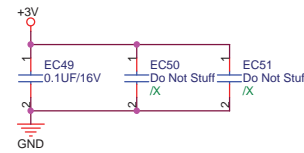
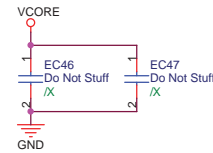
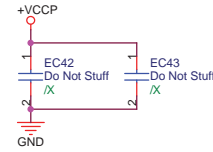
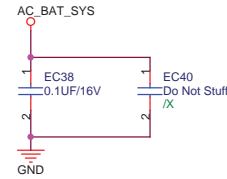
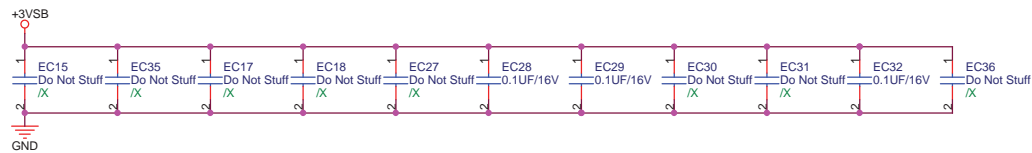
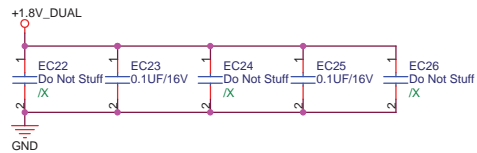
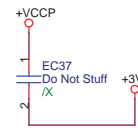
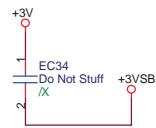
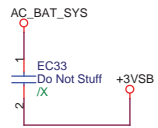
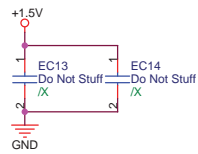
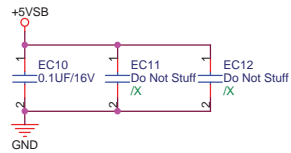
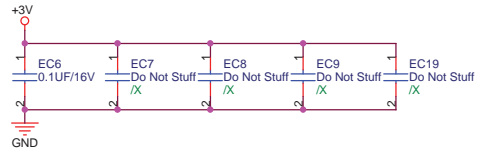
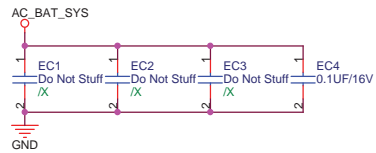
P900_R1.1G_WO_FLASH

ASUS		Title : PWR Jack	
ASUSTek Computer INC.		Engineer: <i>Tiansen_Wu</i>	
Size	Project Name	Rev	
A3	P900	1.2G	
Date: Wednesday, February 27, 2008		Sheet	38 of 47



P900_R1.1G_WO_FLASH

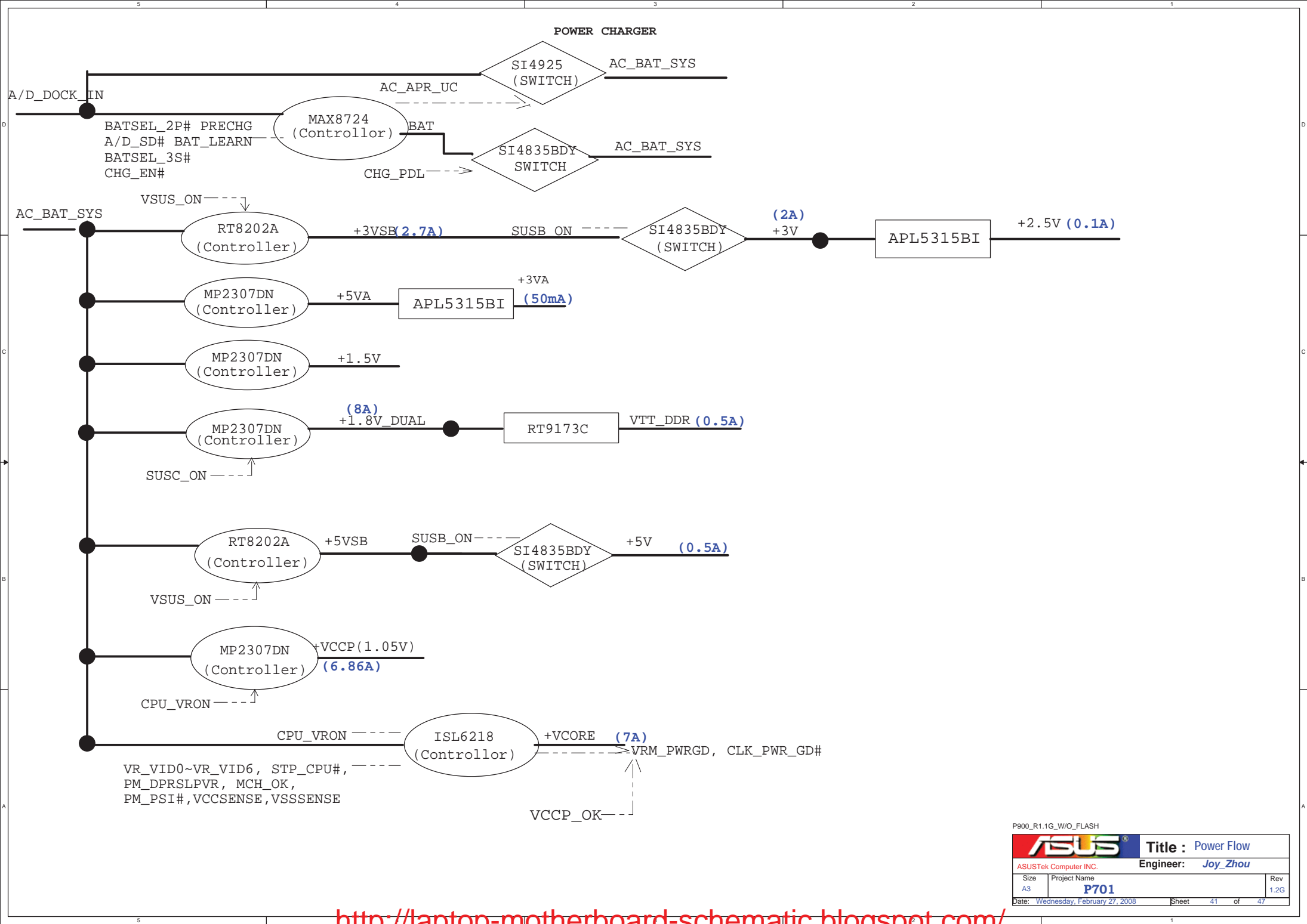
ASUS		Title : Screw Hole	
ASUSTek Computer INC.		Engineer: <i>Tiansen_Wu</i>	
Size	Project Name		Rev
A3	P900		1.2G
Date: Wednesday, February 27, 2008		Sheet	39 of 47



P900
R1.00

P900_R1.1G_WO_FLASH

ASUS		Title : EMI	
ASUSTek Computer INC.		Engineer: <i>Tiansen_Wu</i>	
Size A3	Project Name P900	Rev 1.2G	
Date: Wednesday, February 27, 2008	Sheet 40 of 47		



P900_R1.1G_W/O_FLASH

ASUS		Title : Power Flow	
ASUSTek Computer INC.		Engineer: Joy Zhou	
Size	Project Name	Rev	
A3	P701	1.2G	
Date: Wednesday, February 27, 2008		Sheet	41 of 47

Prevent Input from 19V :
 Adaptor > 14.1V, PQ1 & PQ11 Turn-off
 Adaptor < 14.1V, PQ1 & PQ11 Turn-on

Fast Charging :
 Adaptor > 11V, PQ4 Turn-on, Adaptor current~2.85A
 Adaptor < 11V, PQ4 Turn-off, Adaptor current~2.17A

VREFIN = 3.396V
 MAX8724_REF : 4.096V
 MAX8724_LDO : 5.4V

Pre-Charging Mode :
 Precharging current = 150mA
 Vctl = 169.8mV

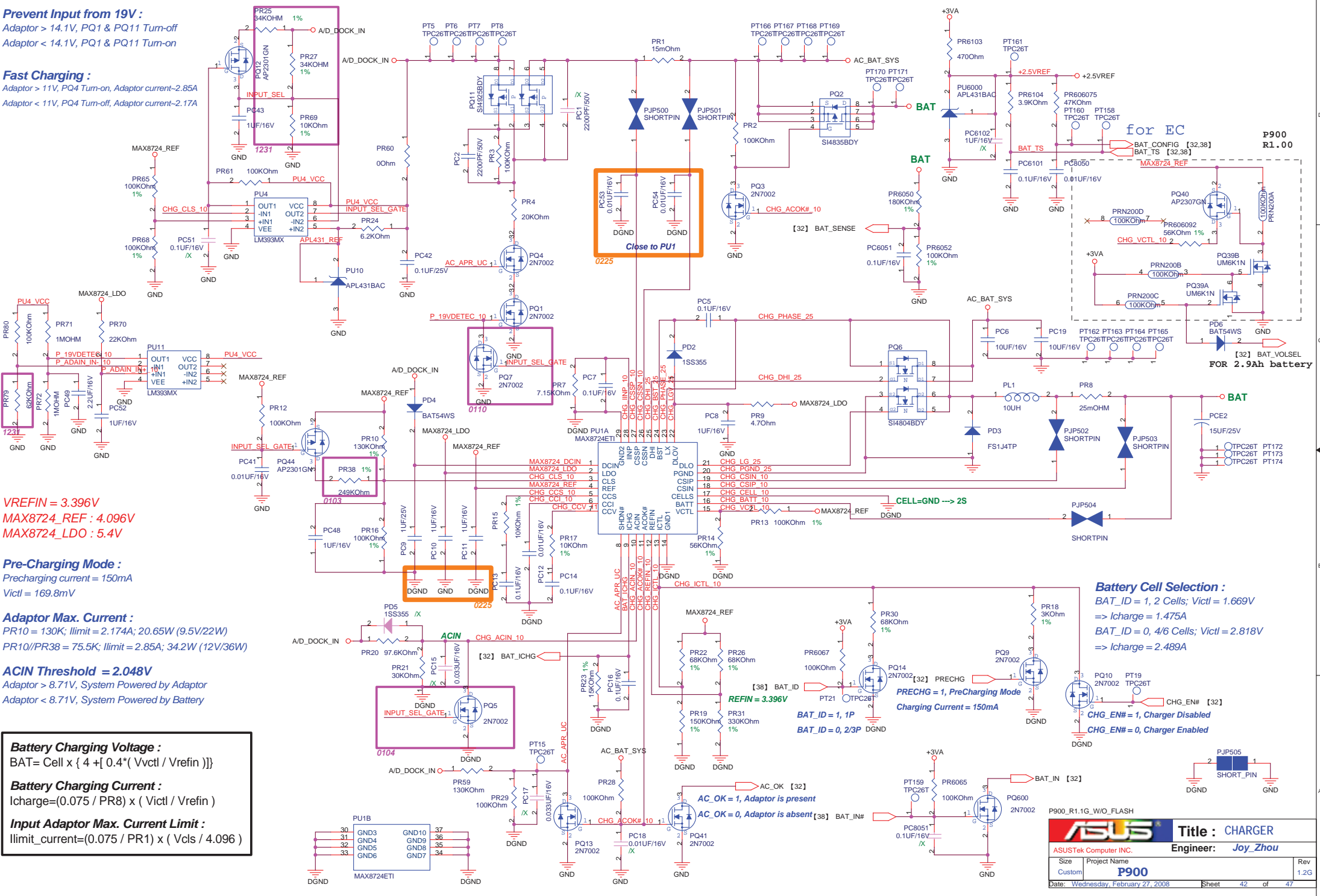
Adaptor Max. Current :
 PR10 = 130K; Ilimit = 2.174A; 20.65W (9.5V/22W)
 PR10/PR38 = 75.5K; Ilimit = 2.85A; 34.2W (12V/36W)

ACIN Threshold = 2.048V
 Adaptor > 8.71V, System Powered by Adaptor
 Adaptor < 8.71V, System Powered by Battery

Battery Charging Voltage :
 $BAT = Cell \times \{ 4 + [0.4 * (V_{ctl} / V_{refin})] \}$

Battery Charging Current :
 $I_{charge} = (0.075 / PR8) \times (V_{ctl} / V_{refin})$

Input Adaptor Max. Current Limit :
 $I_{limit_current} = (0.075 / PR1) \times (V_{cls} / 4.096)$

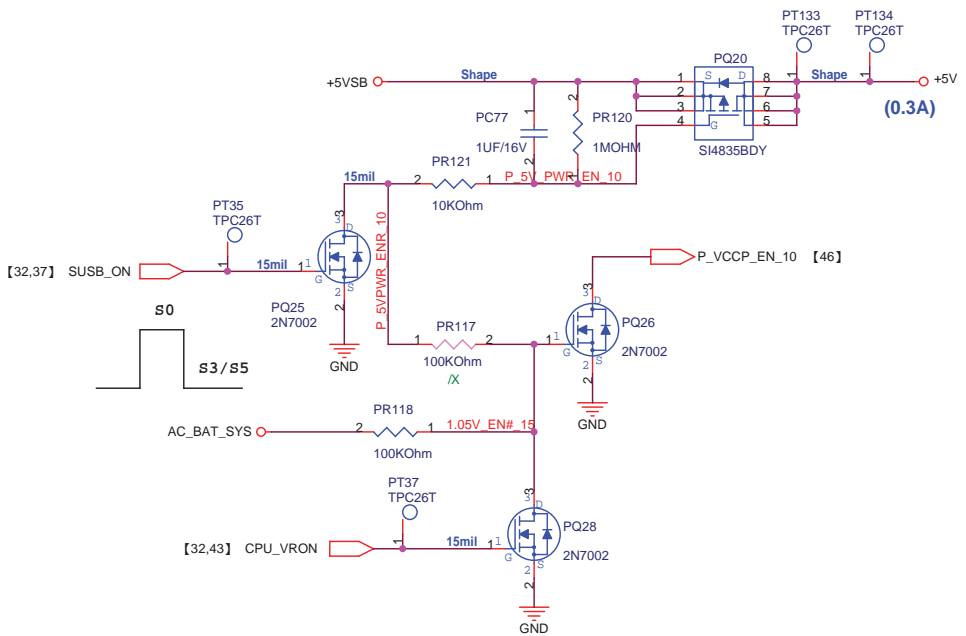
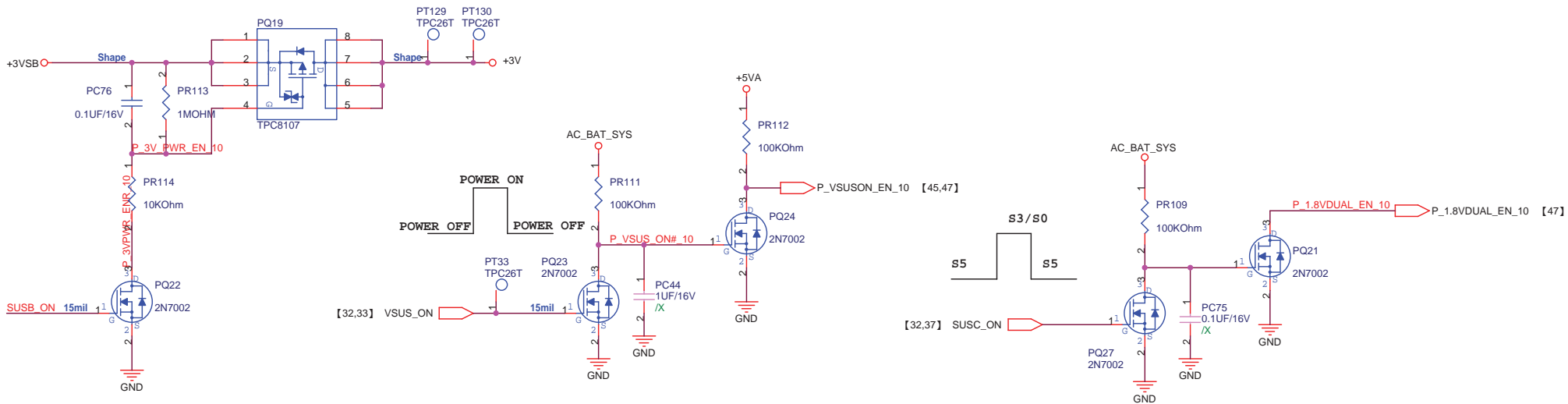


Battery Cell Selection :
 BAT_ID = 1, 2 Cells; Vctl = 1.669V
 => Icharge = 1.475A
 BAT_ID = 0, 4/6 Cells; Vctl = 2.818V
 => Icharge = 2.489A

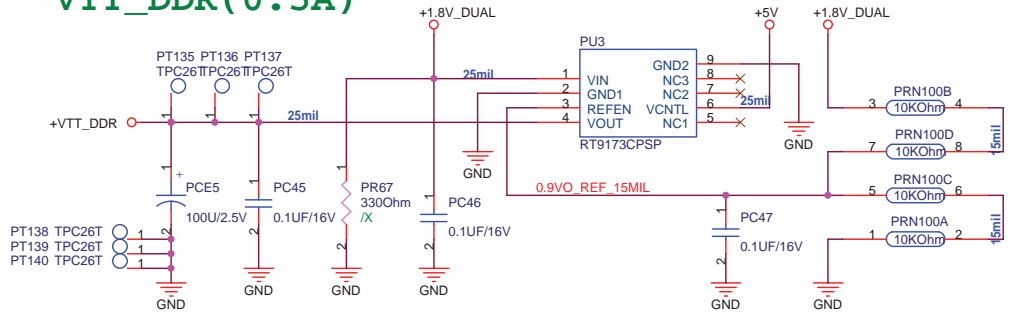
PRECHG = 1, PreCharging Mode
 Charging Current = 150mA

CHG_EN# = 1, Charger Disabled
 CHG_EN# = 0, Charger Enabled

ASUS		Title : CHARGER	
ASUSTek Computer INC.		Engineer: Joy_Zhou	
Size	Project Name	Rev	
Custom	P900	1.2G	
Date: Wednesday, February 27, 2008	Sheet 42 of 47		

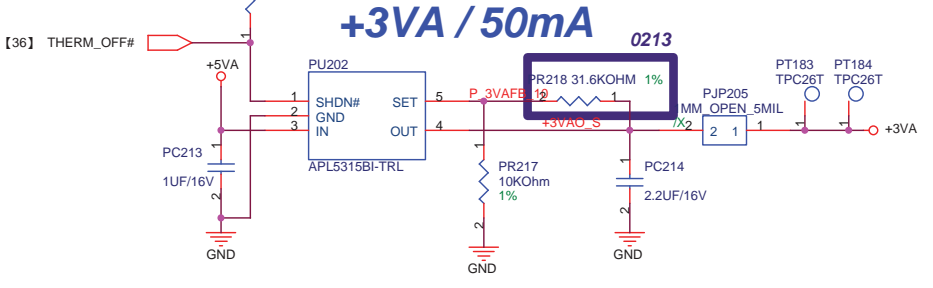
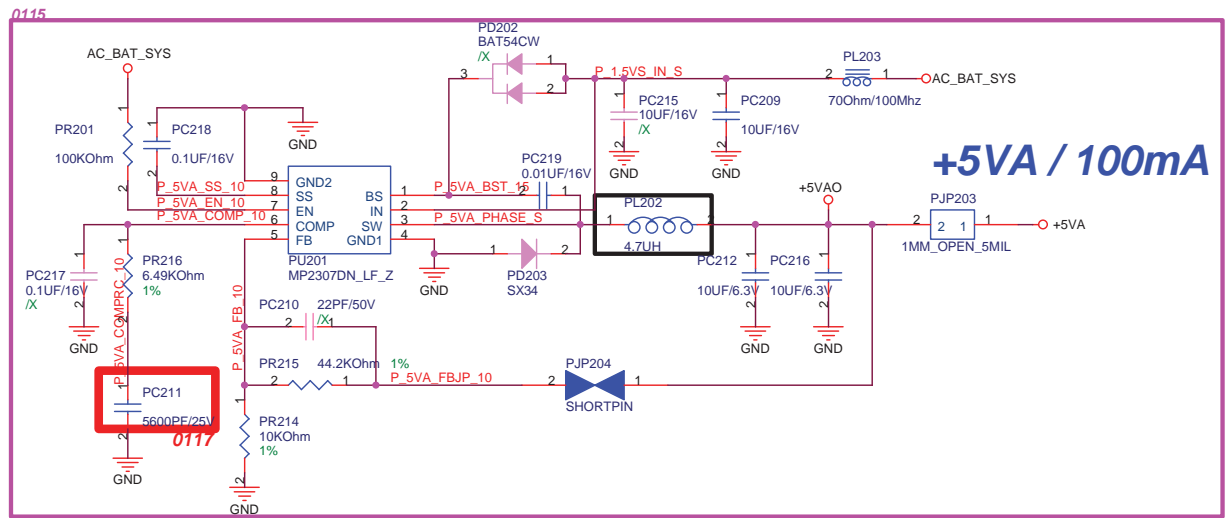
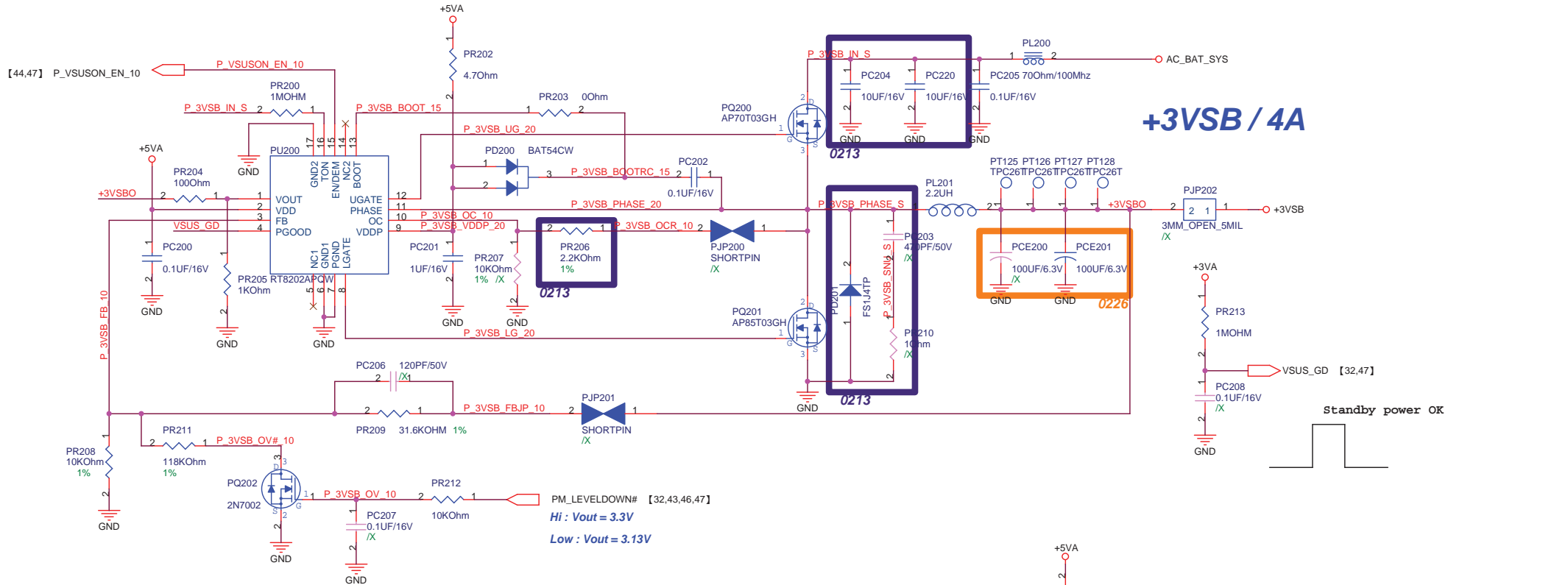


VTT_DDR (0.5A)



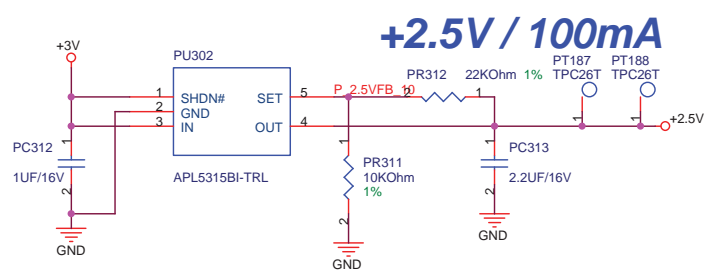
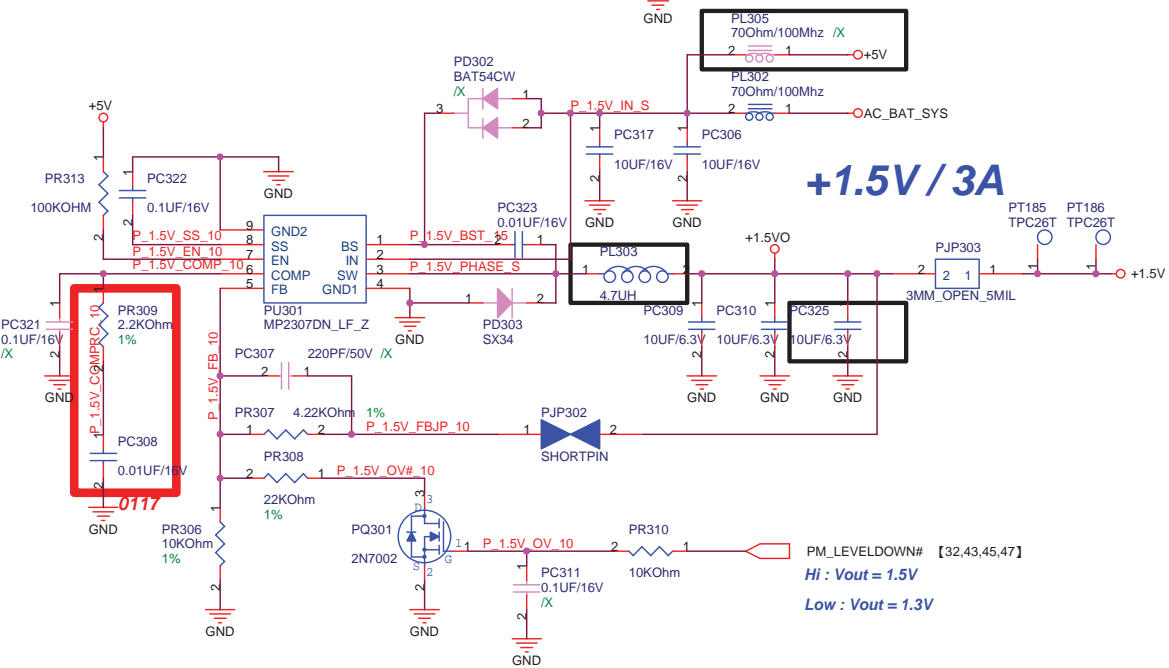
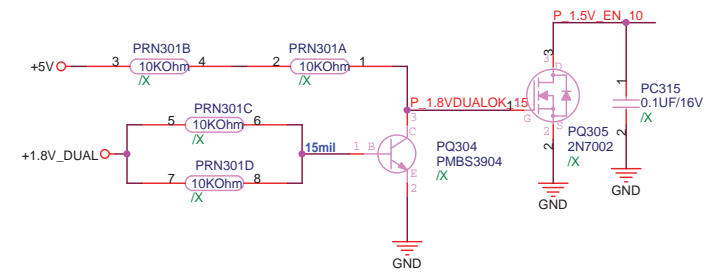
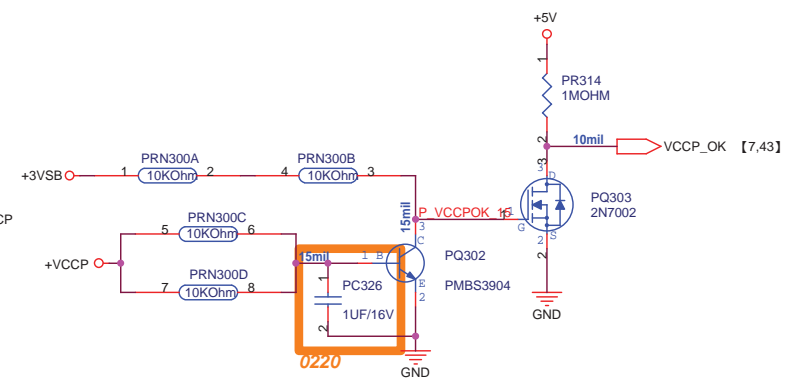
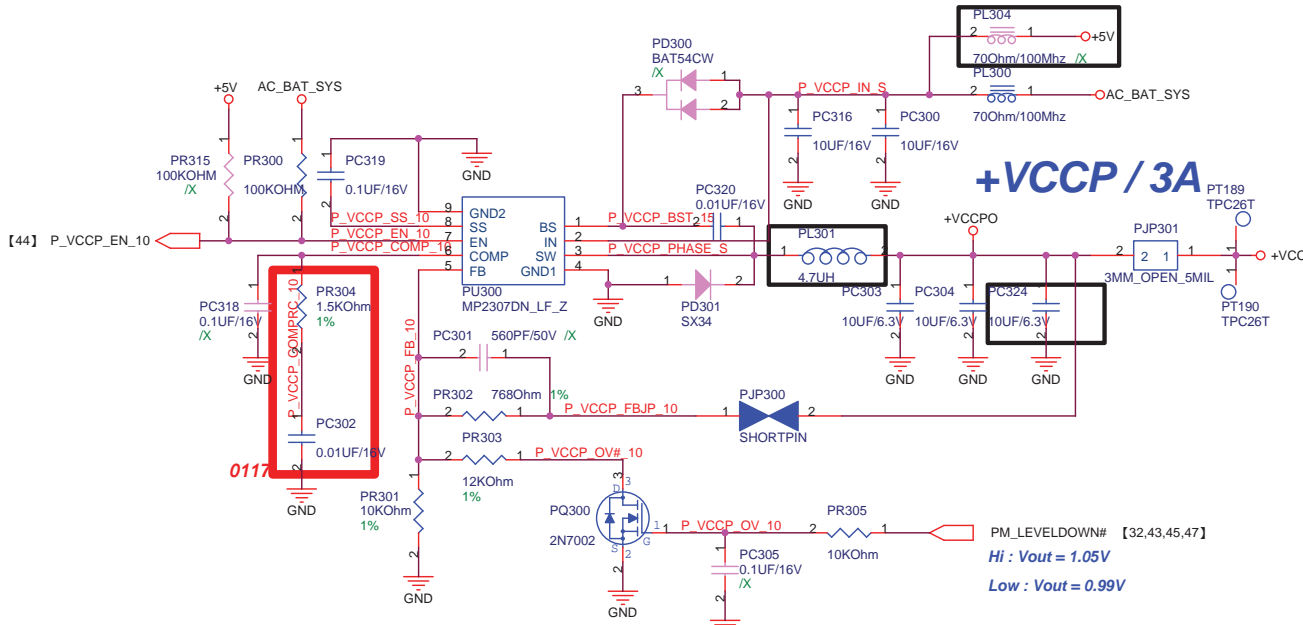
P900_R1.1G_W/O_FLASH

		Title : 3V_5V_VTT_DDR	
ASUSTek Computer INC.		Engineer: <i>Joy_Zhou</i>	
Size B	Project Name P900		Rev 1.2G
Date: Wednesday, February 27, 2008	Sheet	44	of 47



P900_R1.1G_W/O_FLASH

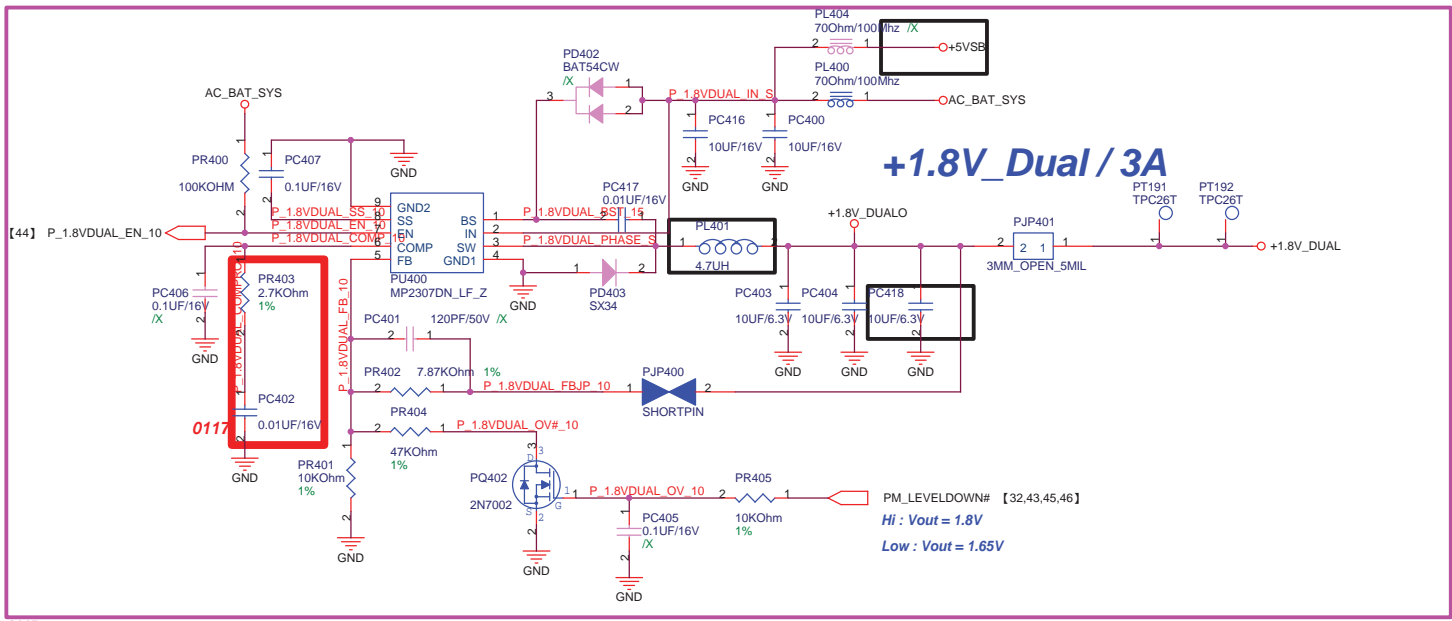
		Title : 3VA_3VSB	
ASUSTek Computer INC.		Engineer: Joy_Zhou	
Size	Project Name		Rev
B	P900		1.2G
Date: Wednesday, February 27, 2008	Sheet	45 of 47	



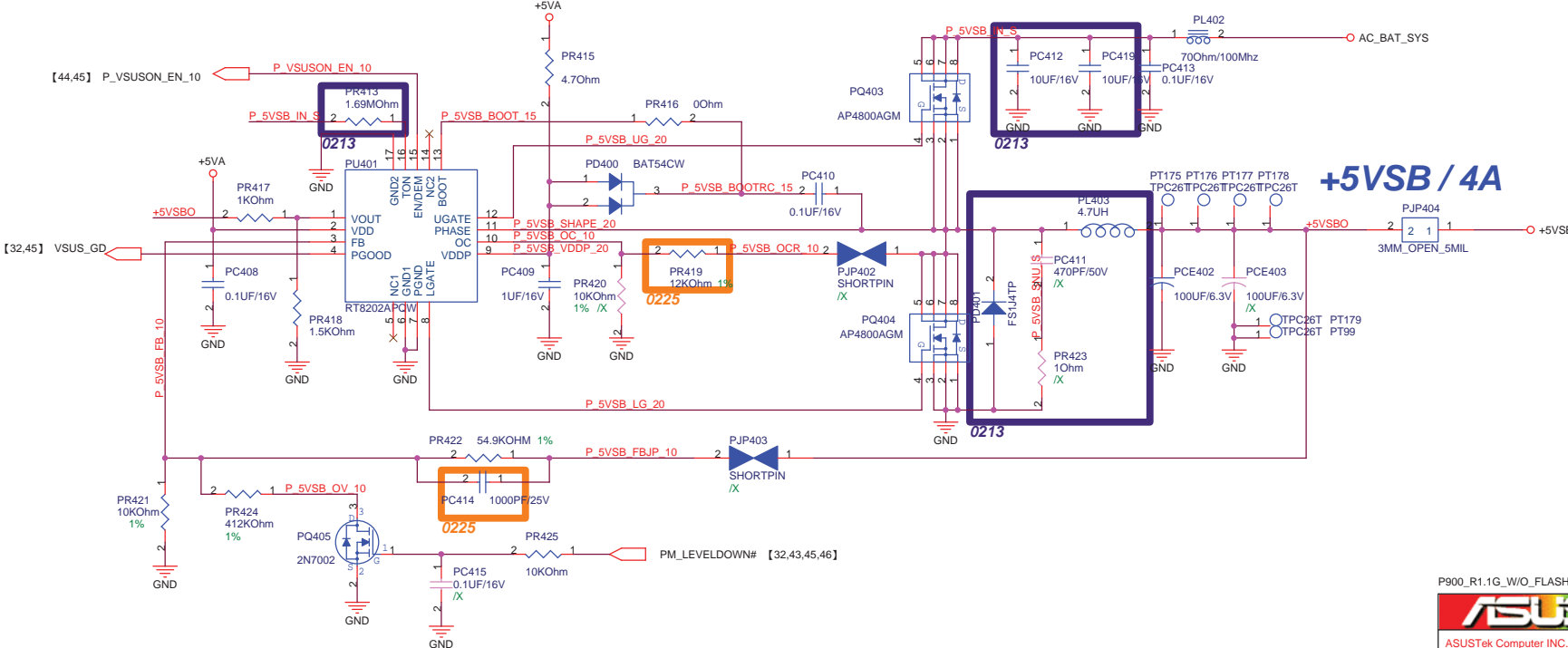
0115

P900_R1.1G_W/O_FLASH

		Title : 1.05V_1.5V_2.5V	
ASUSTek Computer INC.		Engineer: Joy_Zhou	
Size	Project Name		Rev
B	P900		1.2G
Date: Wednesday, February 27, 2008	Sheet	46	of 47



0115



P900_R1.1G_W/O_FLASH

ASUS		Title : 1.8V_DUAL_5VSB	
ASUSTek Computer INC.		Engineer: <i>Joy_Zhou</i>	
Size	Project Name		Rev
A3	P900		1.2G
Date:	Wednesday, February 27, 2008	Sheet	47 of 47