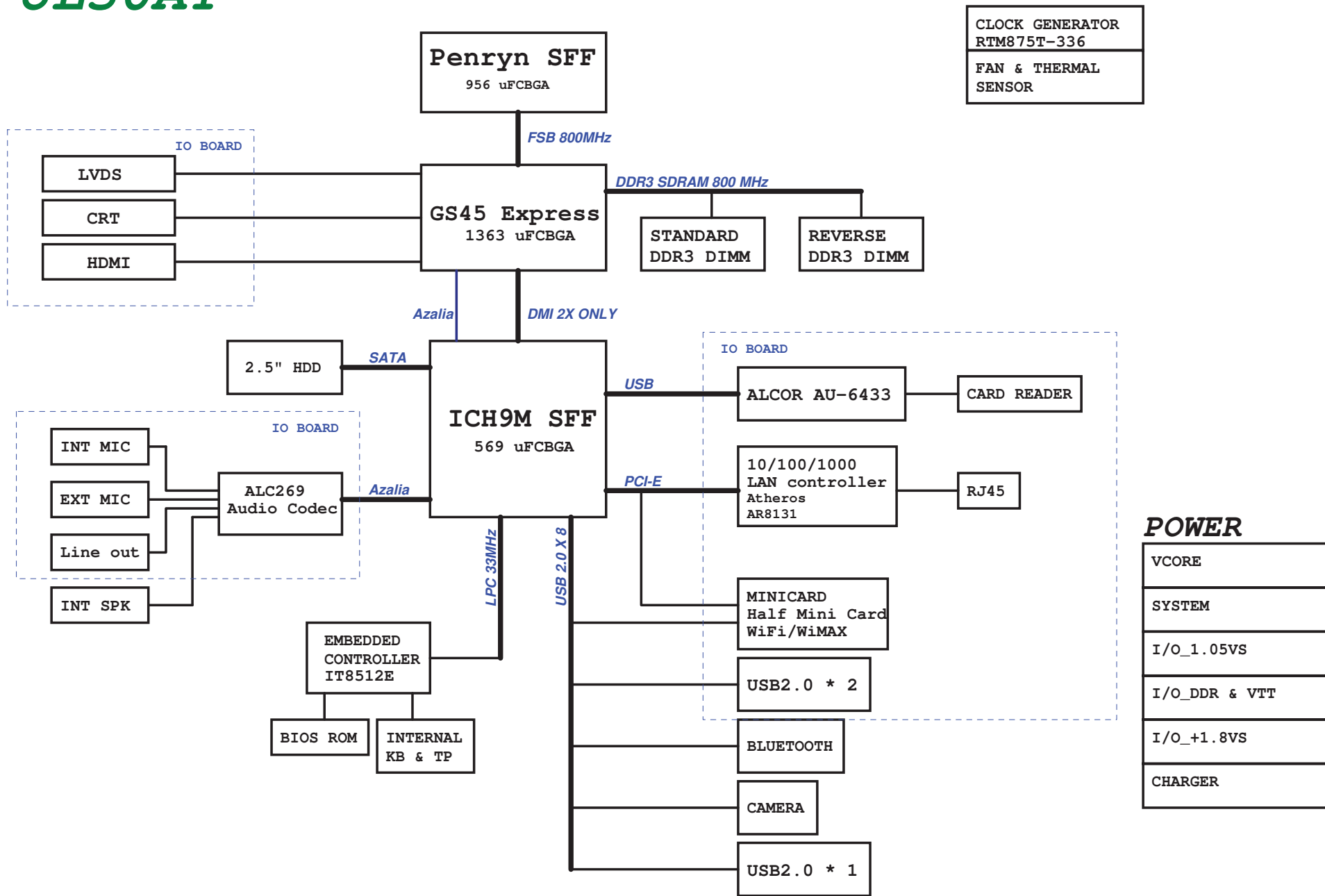


UL50AT



CLOCK GENERATOR
RTM875T-336

FAN & THERMAL
SENSOR

POWER

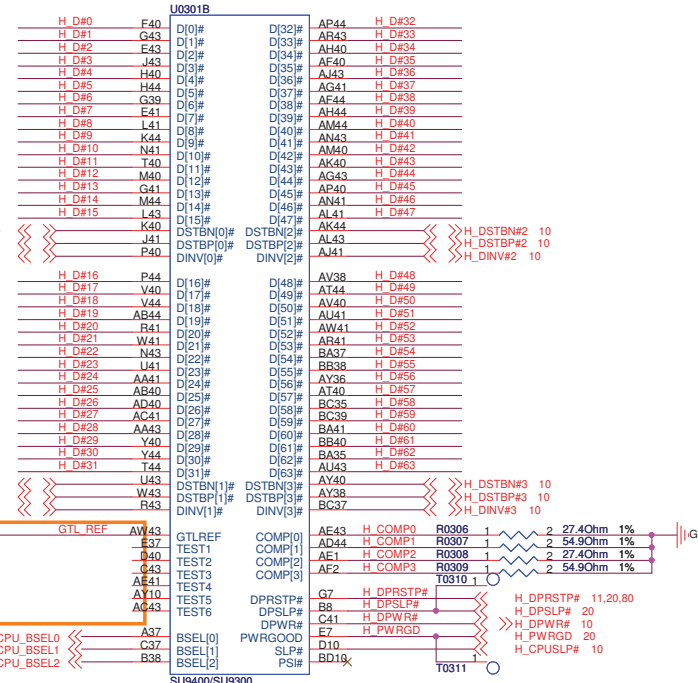
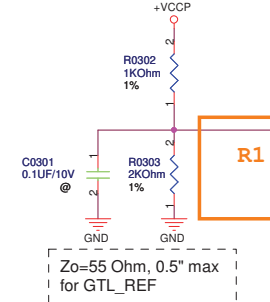
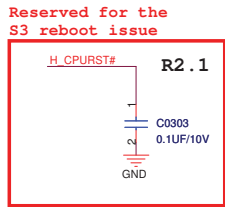
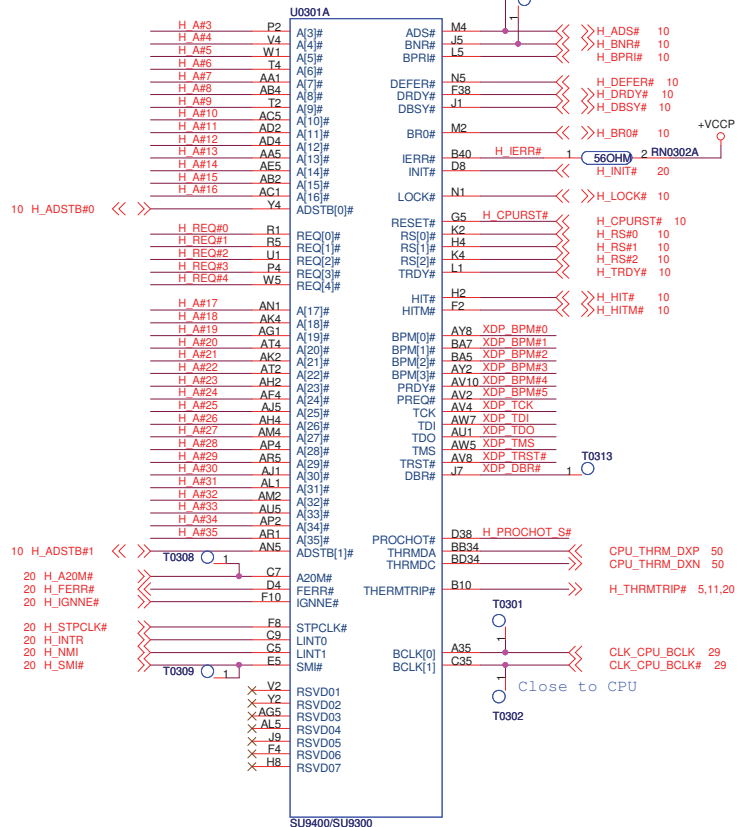
VCORE
SYSTEM
I/O_1.05VS
I/O_DDR & VTT
I/O_+1.8VS
CHARGER

<Variant Name>

ASUS Title : Block Diagram
ASUSTeK COMPUTER INC. Engineer: Jack Hsu

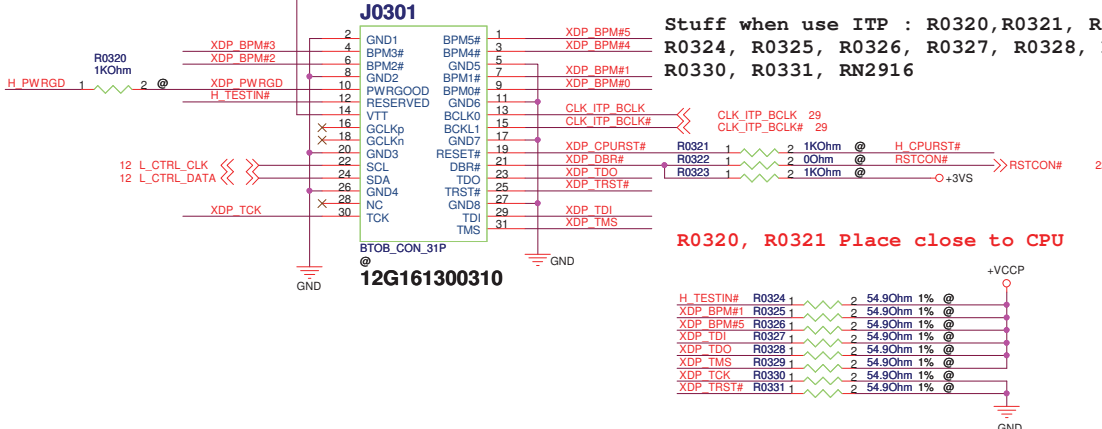
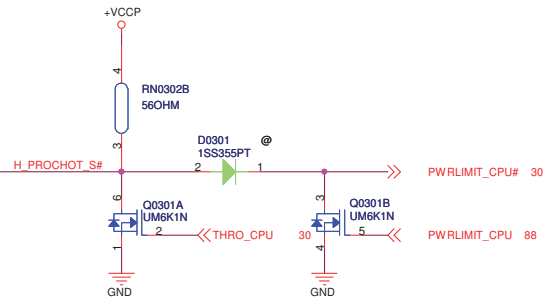
Size	Project Name	Rev
Custom	UL50AT	2.0
Date: Friday, October 16, 2009	Sheet	1 of 97

10 H_D#(63:0) << H_D#(63:0)
 10 H_A#(35:3) << H_A#(35:3)
 10 H_REQ#(4:0) << H_REQ#(4:0)



BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	0	1	1
200	800	0	1	0
266	1067	0	0	0

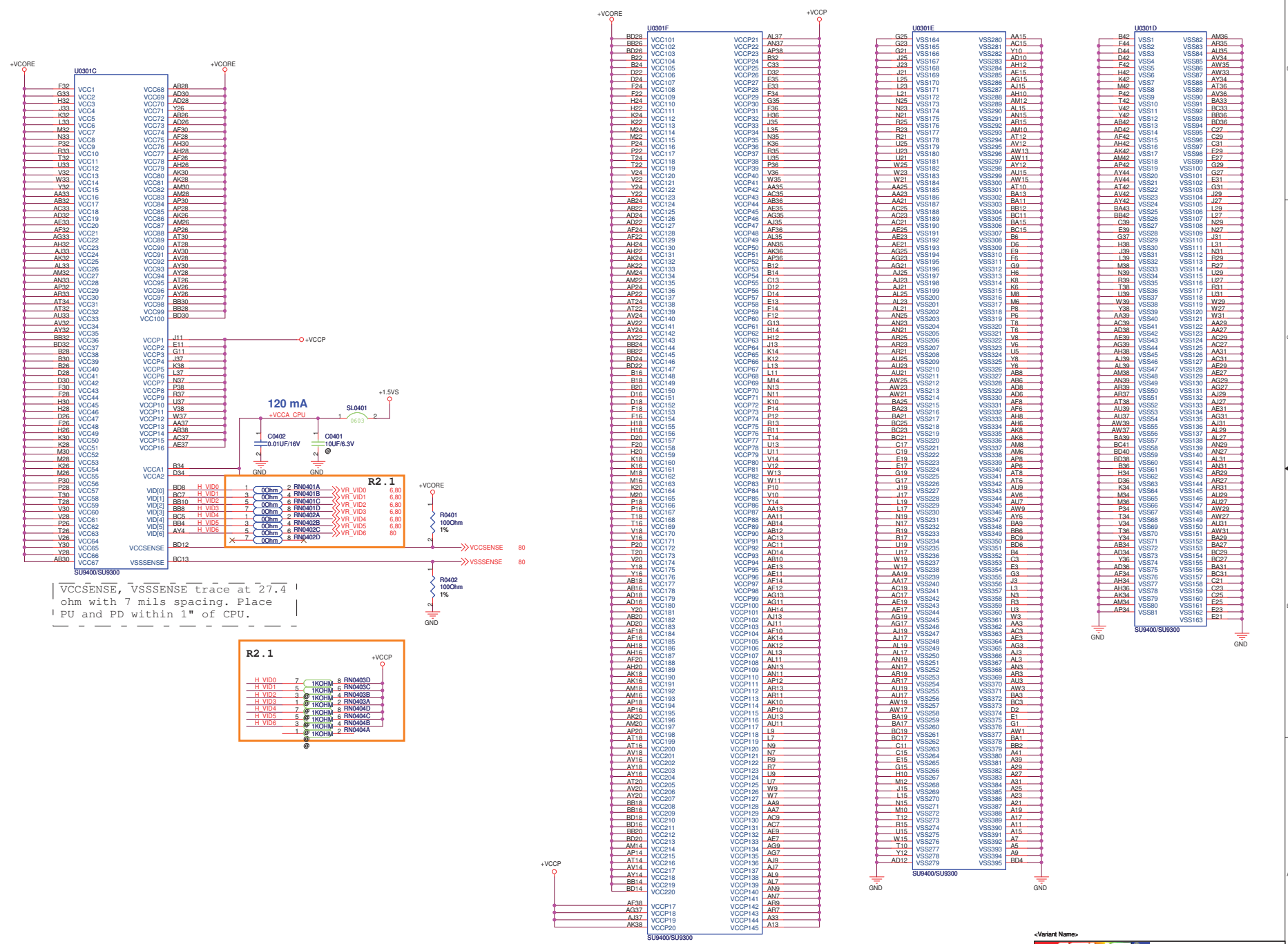
Comp 0,2: Zo=27.4 Ohm, trace length < 0.5"
 Comp 1,3: Zo=55 Ohm, trace length < 0.5"



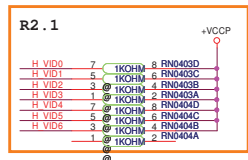
Stuff when use ITP : R0320, R0321, R0322, R0324, R0325, R0326, R0327, R0328, R0329, R0330, R0331, RN2916

R0320, R0321 Place close to CPU

ASUS Logo
Title : PENRYN ULV FSB
 ASUSTeK COMPUTER INC. Engineer: Jack Hsu
 Size: Custom Project Name: UL50AT Rev: 2.0
 Date: Friday, October 16, 2009 Sheet: 3 of 97



VCCSENSE, VSSSENSE trace at 27.4 ohm with 7 mils spacing. Place CPU and PD within 1" of CPU.

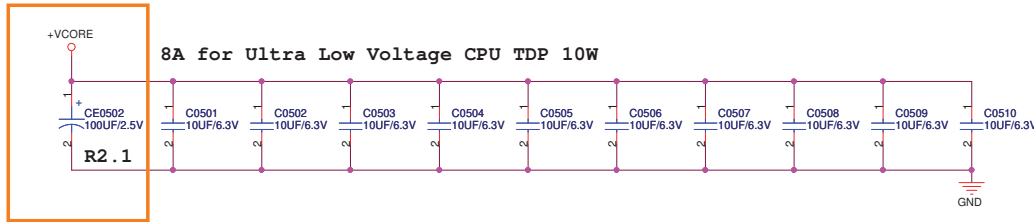


ASUS Logo

Title : PENRYN ULV POWER

ASUSTek COMPUTER INC. Engineer: Jack Hsu

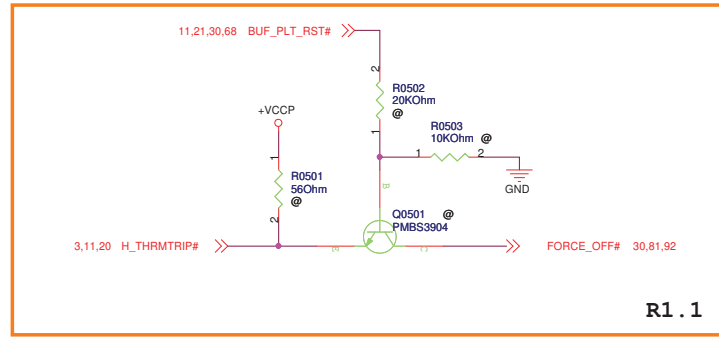
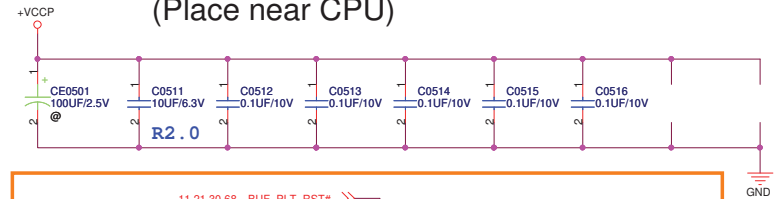
Size C	Project Name	Rev 2.0
Date: Friday, October 16, 2009		Sheet 4 of 97

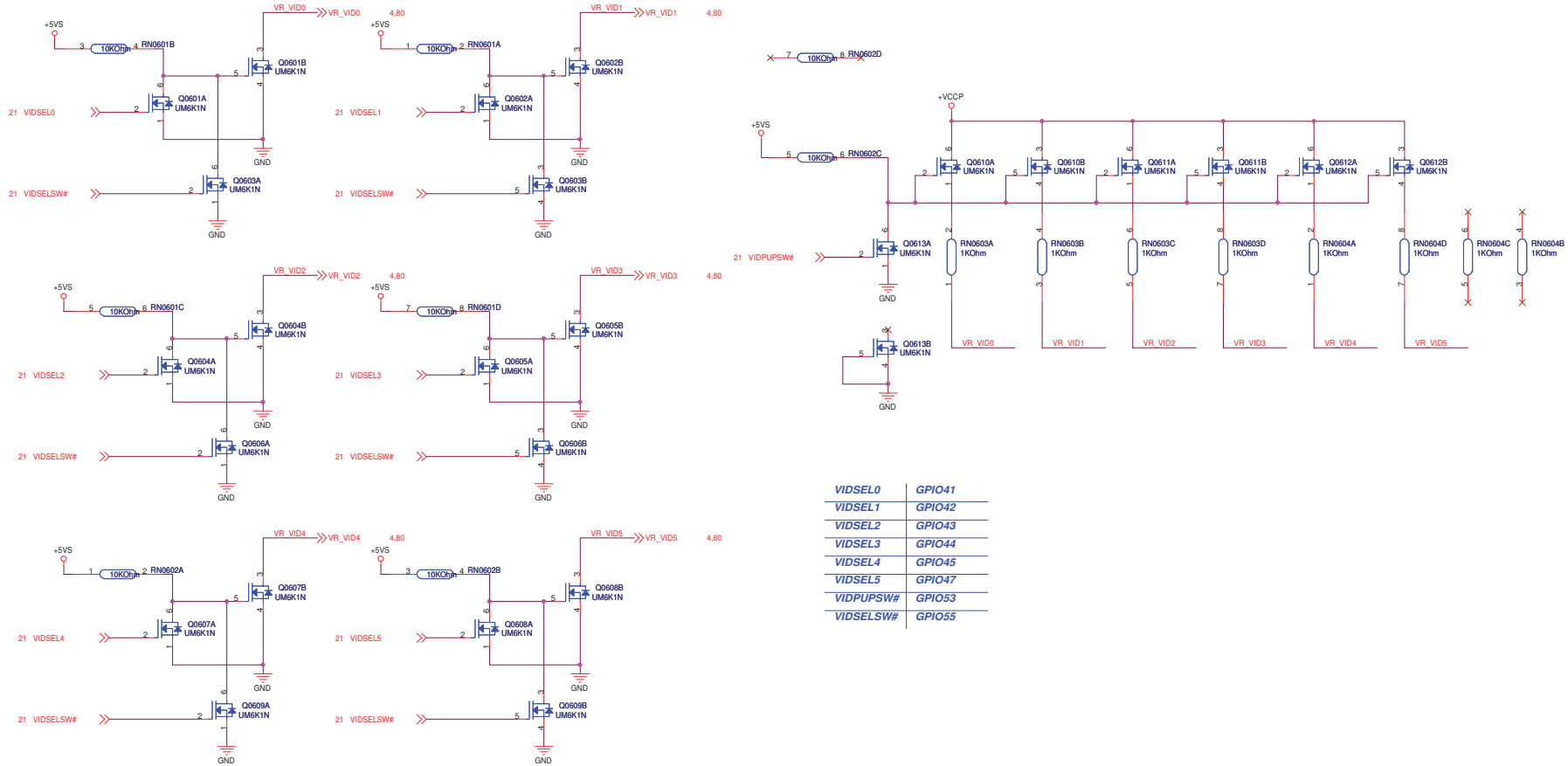


Decoupling guide from Intel

V CORE	10uF mount	*4pcs
	0.1uF mount	*5pcs
V CCP	1uF	* 12pcs
	270uF	* 1pcs
V CCA	0.01uF	* 1 pcs
	10uF	* 1 pcs

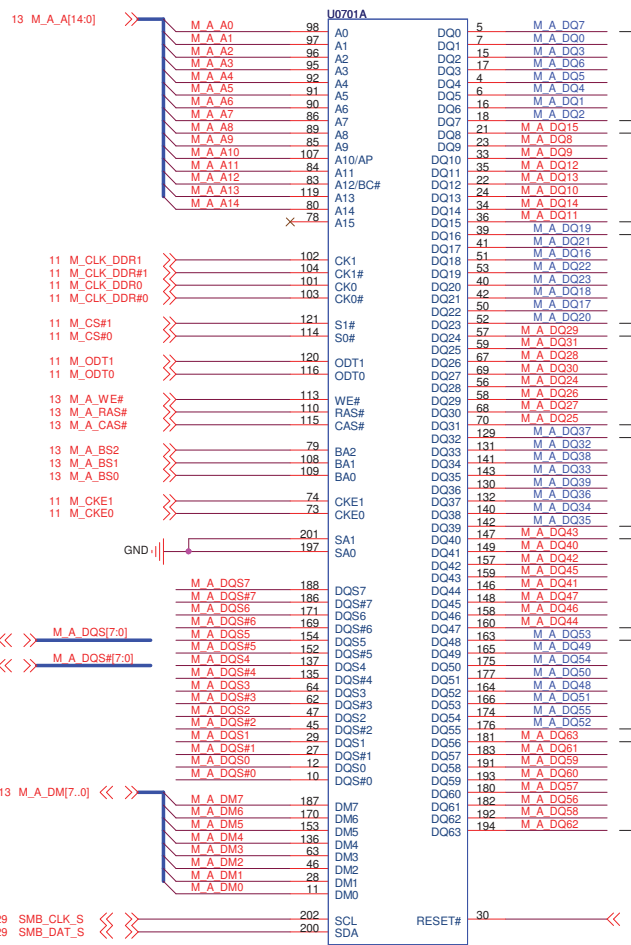
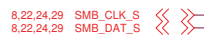
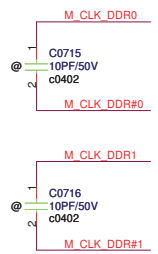
**+VCCP Decoupling Capacitor
(Place near CPU)**



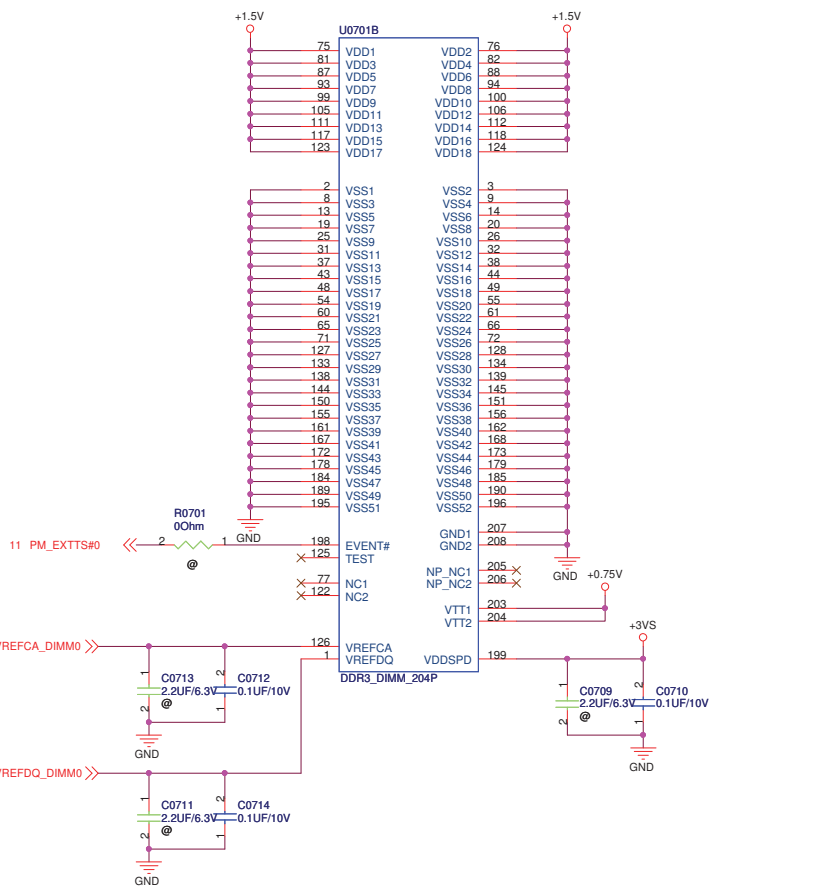
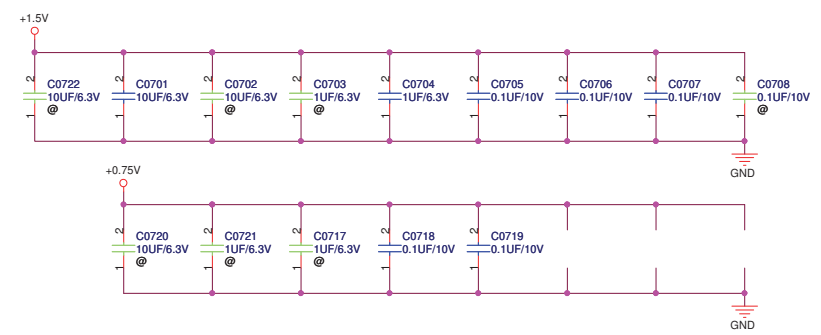


VIDSEL0	GPIO41
VIDSEL1	GPIO42
VIDSEL2	GPIO43
VIDSEL3	GPIO44
VIDSEL4	GPIO45
VIDSEL5	GPIO47
VIDPUPSW#	GPIO53
VIDSELW#	GPIO55

Place near SO-DIMM_0



DDR3_DIMM_204P
12G02553204W
DDR3 DIMM 204P,1.5V,5.2H,REV



<Variant Name>

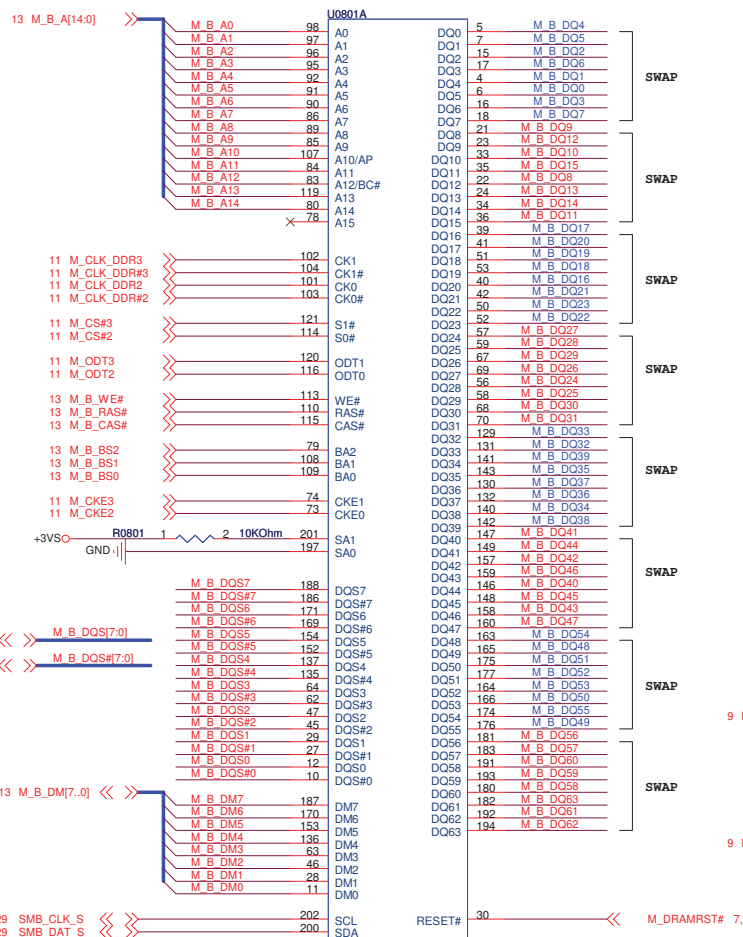
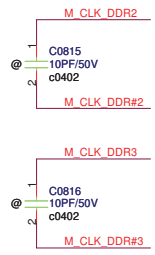
Title : DDR3 SO-DIMM A

ASUSTeK COMPUTER INC. Engineer: **Jack Hsu**

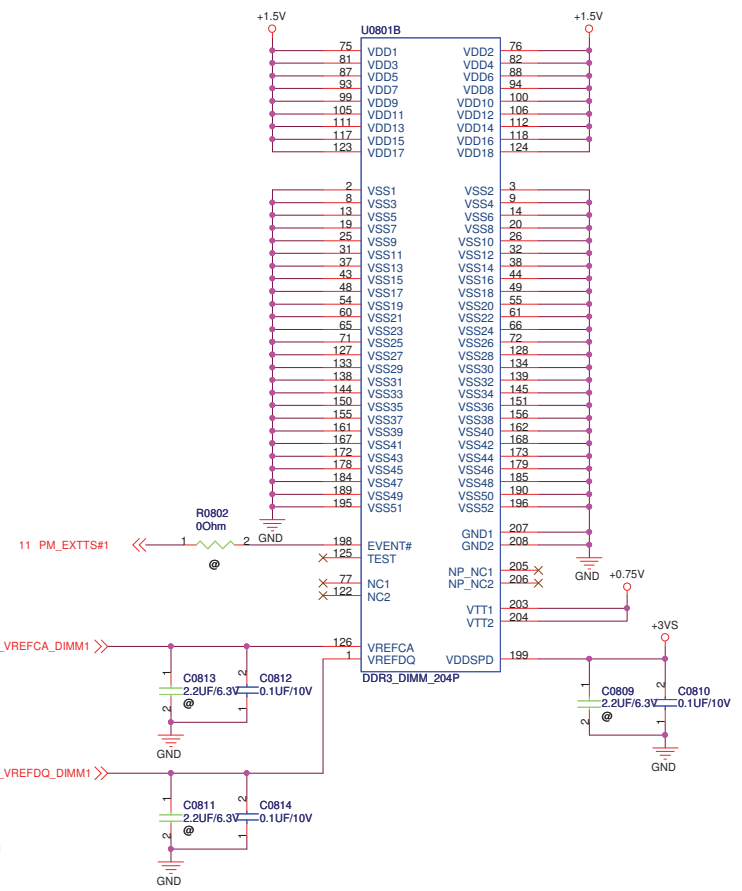
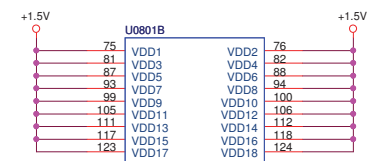
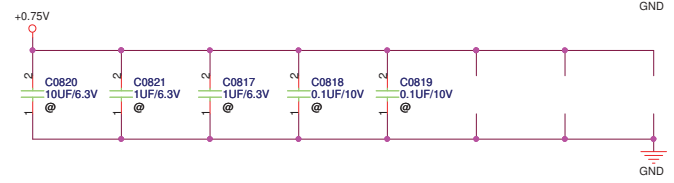
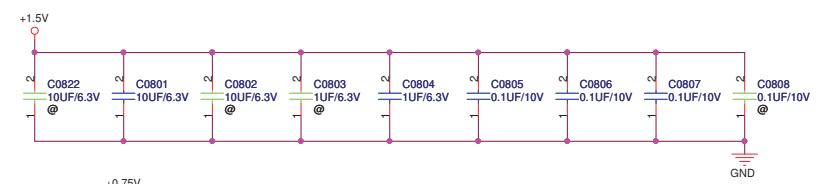
Size Project Name
 Custom **UL50AT**

Date: Friday, October 16, 2009 Sheet 7 of 97

Place near SO-DIMM_1



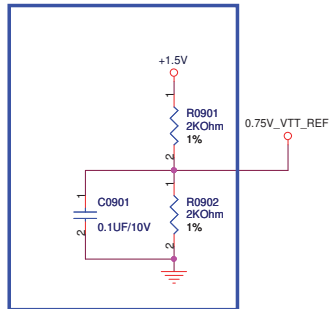
DDR3 DIMM_204P
12G02553204K
DDR3 DIMM 204P, 1.5V, 5.2H, STD



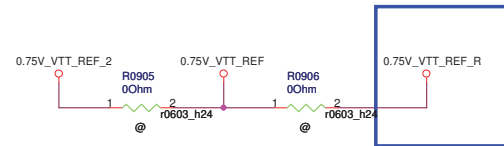
<Variant Name>

ASUS		Title : DDR3 SO-DIMM B	
ASUSTek COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	UL50AT	2.0	
Date: Friday, October 16, 2009	Sheet	8	of 97

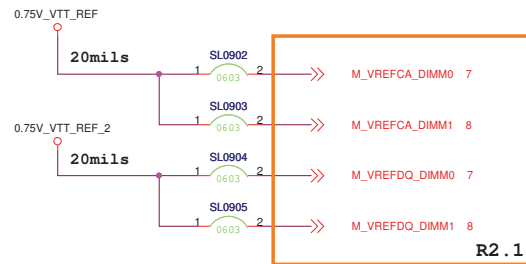
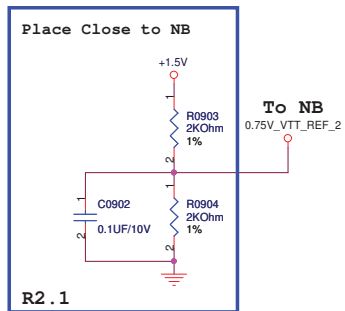
R2.1



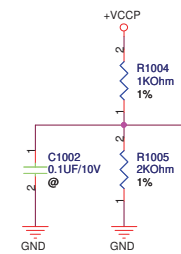
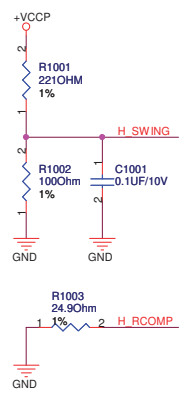
From DDR/VTT Power Circuit



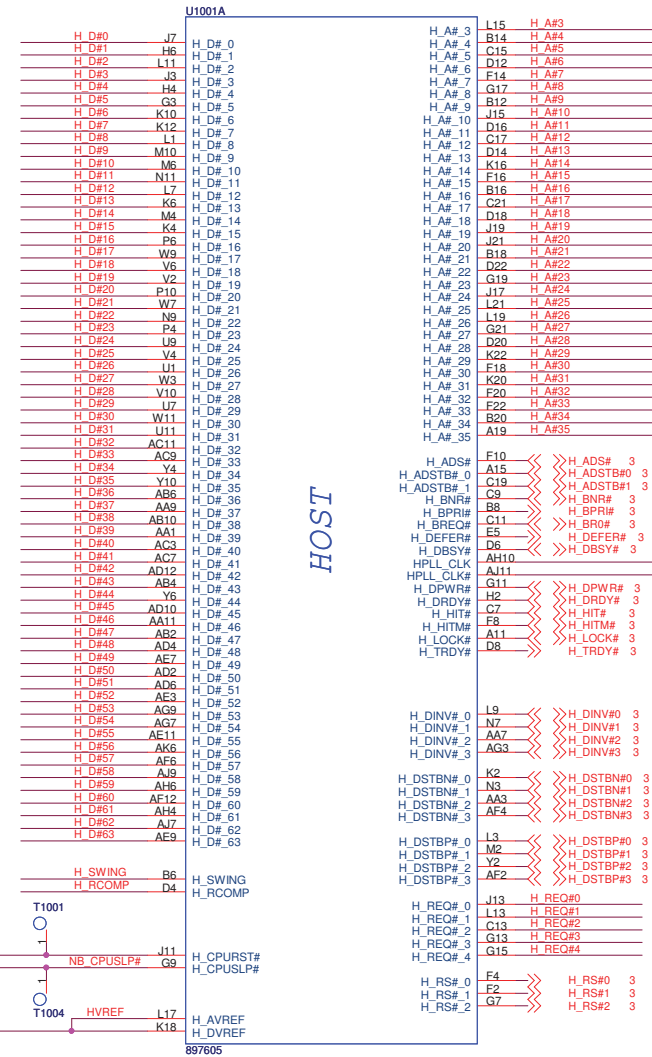
Place Close to NB



R2.1



3 H_A#[35:3] <<>> H_A#[35:3]
 3 H_REQ#[4:0] <<>> H_REQ#[4:0]
 3 H_D#[63:0] <<>> H_D#[63:0]

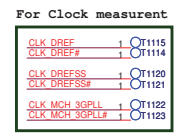
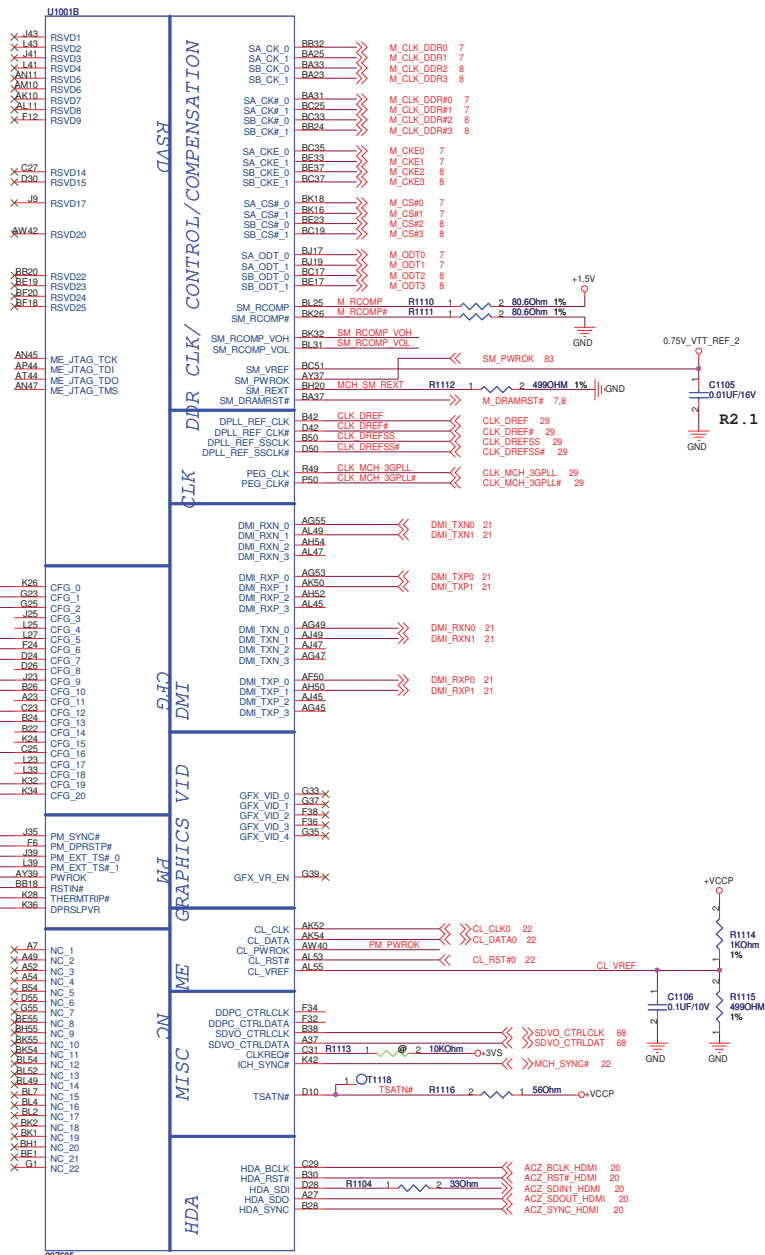
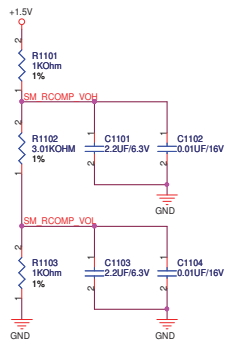


<Variant Name>

ASUS Title : NB GS45 HOST
 ASUSTeK COMPUTER INC. Engineer: Jack Hsu

Size	Project Name	Rev
Custom	UL50AT	2.0

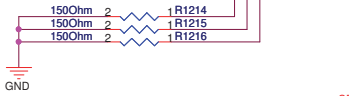
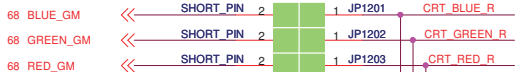
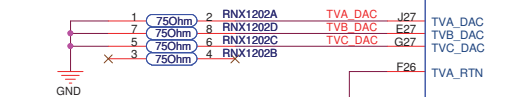
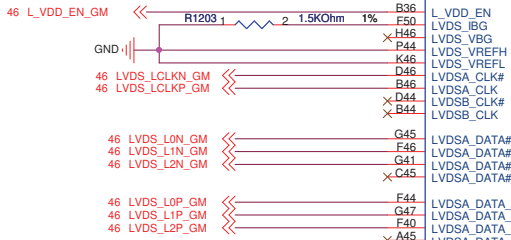
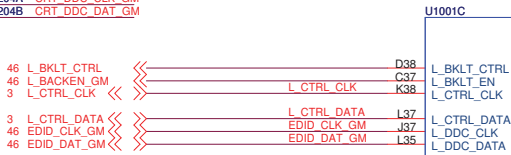
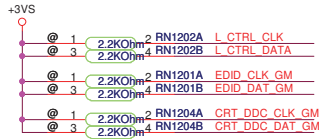
Date: Friday, October 16, 2009 Sheet 10 of 97



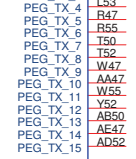
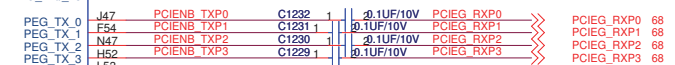
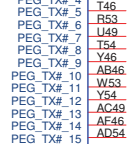
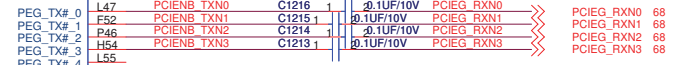
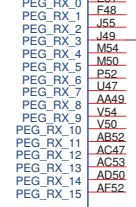
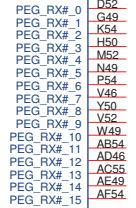
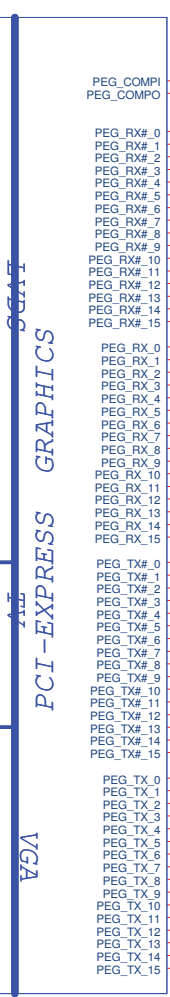
DG, Checklist: 500ohm
CRB: 510ohm



897605



897605
 R1208 1KOhm 1%
 Check : R1208
 如果CRT Trace 12"以内,放1kohm
 如果CRT Trace 12~15.3",放976ohm



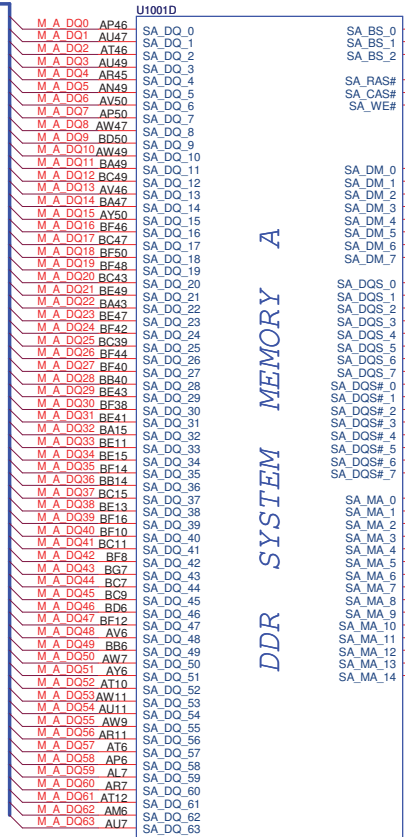
<Variant Name>

ASUS Title : NB GS45 DISPLAY
 ASUSTeK COMPUTER INC. Engineer: Jack Hsu

Size Project Name
 Custom UL50AT Rev 2.0

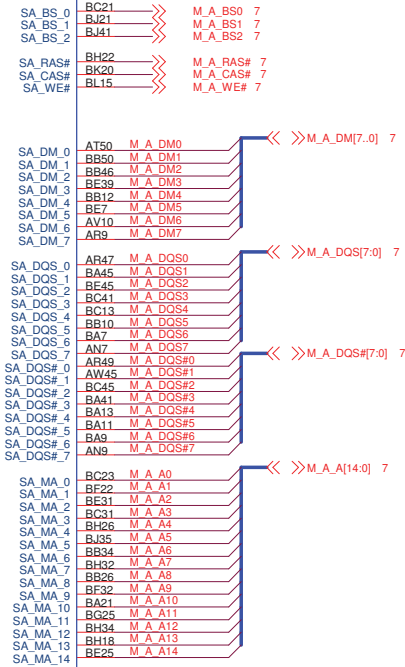
Date: Friday, October 16, 2009 Sheet 12 of 97

7 M_A_DQ[63:0] << >>

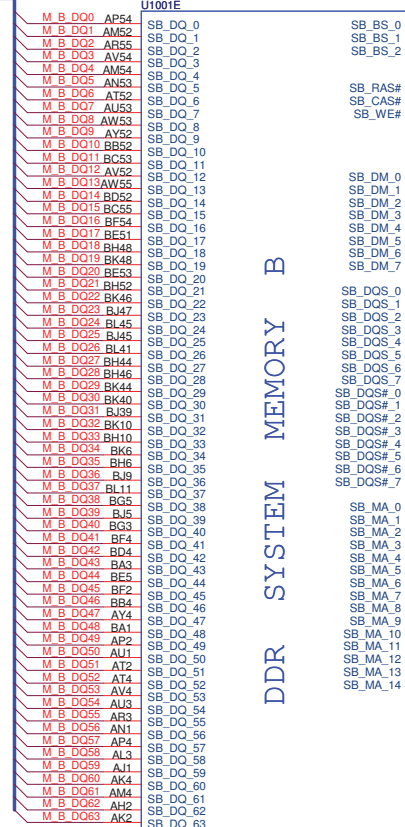


U1001D

DDR SYSTEM MEMORY A

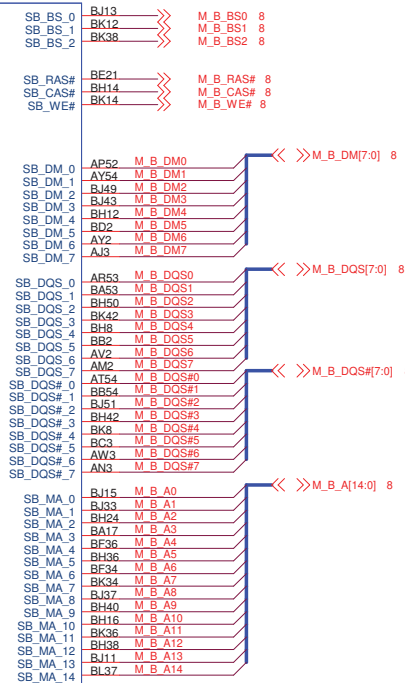


8 M_B_DQ[63:0] << >>



U1001E

DDR SYSTEM MEMORY B



<Variant Name>

Title : NB GS45 DDR3 BUS
ASUSTeK COMPUTER INC. Engineer: Jack Hsu

Size	Project Name	Rev
Custom	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 13 of 97

- BB36 VCC_SM_1
- BE35 VCC_SM_2
- AW34 VCC_SM_3
- BK30 VCC_SM_4
- BH30 VCC_SM_5
- BF30 VCC_SM_6
- BQ30 VCC_SM_7
- BB30 VCC_SM_8
- AW30 VCC_SM_9
- BL29 VCC_SM_10
- BJ29 VCC_SM_11
- BG29 VCC_SM_12
- BE29 VCC_SM_13
- BC29 VCC_SM_14
- BA29 VCC_SM_15
- AY29 VCC_SM_16
- BK28 VCC_SM_17
- BH28 VCC_SM_18
- BF28 VCC_SM_19
- BD28 VCC_SM_20
- BB28 VCC_SM_21
- BL27 VCC_SM_22
- BJ27 VCC_SM_23
- BK27 VCC_SM_24
- BE27 VCC_SM_25
- BC27 VCC_SM_26
- BA27 VCC_SM_27
- AY27 VCC_SM_28
- AW26 VCC_SM_29
- BL19 VCC_SM_30
- BL19 VCC_SM_31
- BB16 VCC_SM_32
- BB16 VCC_SM_33

- VCC_AXG_1
- VCC_AXG_2
- VCC_AXG_3
- VCC_AXG_4
- VCC_AXG_5
- VCC_AXG_6
- VCC_AXG_7
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- VCC_AXG_60
- VCC_AXG_61

- VCC_AXG_NCTF_1
- VCC_AXG_NCTF_2
- VCC_AXG_NCTF_3
- VCC_AXG_NCTF_4
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- VCC_AXG_100

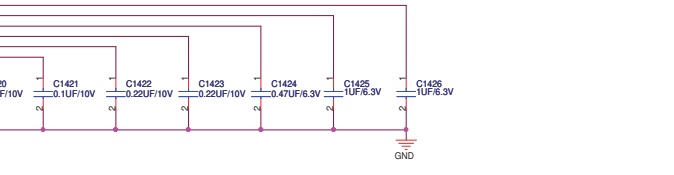
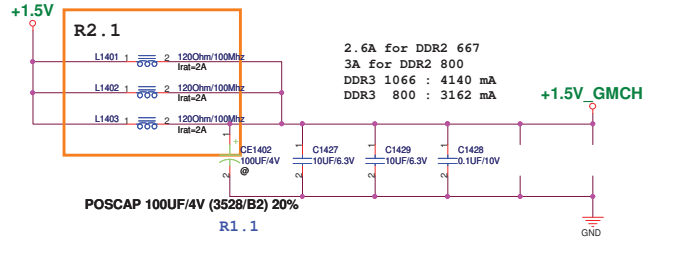
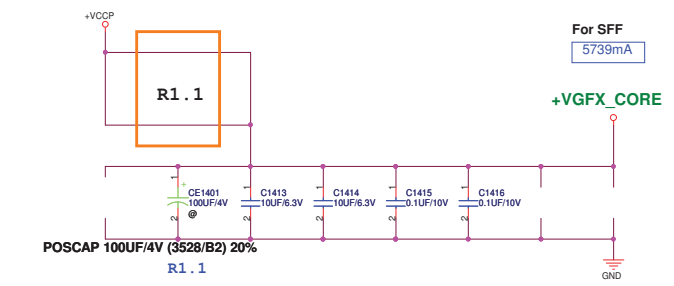
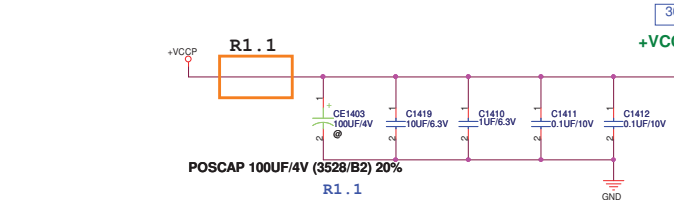
- VCC_AXG_LF1
- VCC_AXG_LF2
- VCC_AXG_LF3
- VCC_AXG_LF4
- VCC_AXG_LF5
- VCC_AXG_LF6
- VCC_AXG_LF7

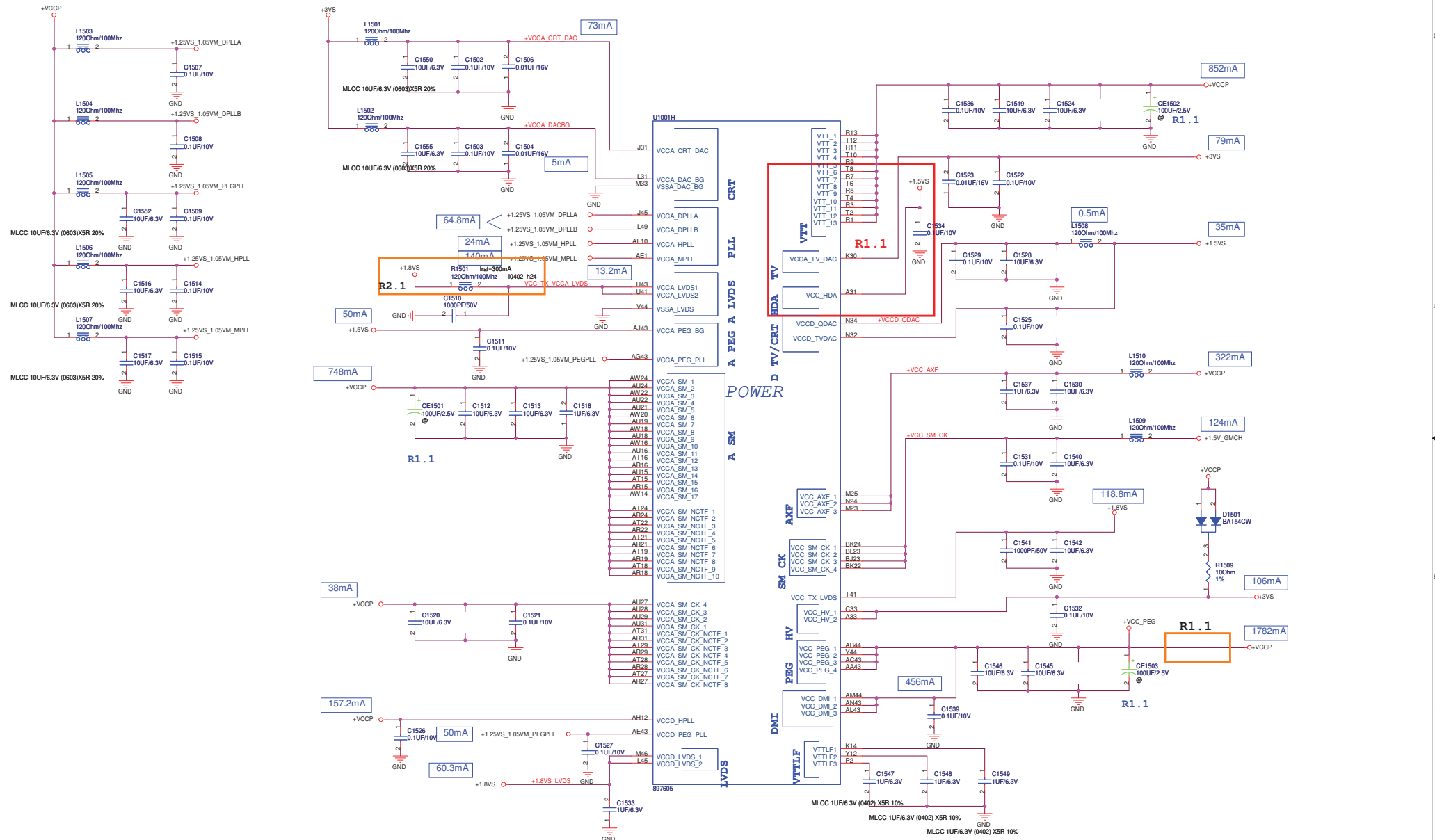
- VCC_1
- VCC_2
- VCC_3
- VCC_4
- VCC_5
- VCC_6
- VCC_7
- VCC_8
- VCC_9
- VCC_10
- VCC_11
- VCC_12
- VCC_13
- VCC_14
- VCC_15
- VCC_16
- VCC_17
- VCC_18
- VCC_19
- VCC_20
- VCC_21
- VCC_22
- VCC_23
- VCC_24
- VCC_25
- VCC_26
- VCC_27
- VCC_28
- VCC_29
- VCC_30
- VCC_31
- VCC_32
- VCC_33
- VCC_34
- VCC_35
- VCC_36
- VCC_37
- VCC_38
- VCC_39
- VCC_40
- VCC_41
- VCC_42
- VCC_43
- VCC_44
- VCC_45
- VCC_46
- VCC_47
- VCC_48
- VCC_49
- VCC_50
- VCC_51
- VCC_52
- VCC_53
- VCC_54
- VCC_55
- VCC_56
- VCC_57
- VCC_58
- VCC_59
- VCC_60
- VCC_61

- VCC_NCTF_1
- VCC_NCTF_2
- VCC_NCTF_3
- VCC_NCTF_4
- VCC_NCTF_5
- VCC_NCTF_6
- VCC_NCTF_7
- VCC_NCTF_8
- VCC_NCTF_9
- VCC_NCTF_10
- VCC_NCTF_11
- VCC_NCTF_12
- VCC_NCTF_13
- VCC_NCTF_14
- VCC_NCTF_15
- VCC_NCTF_16
- VCC_NCTF_17
- VCC_NCTF_18
- VCC_NCTF_19
- VCC_NCTF_20
- VCC_NCTF_21
- VCC_NCTF_22
- VCC_NCTF_23
- VCC_NCTF_24
- VCC_NCTF_25
- VCC_NCTF_26
- VCC_NCTF_27
- VCC_NCTF_28
- VCC_NCTF_29
- VCC_NCTF_30
- VCC_NCTF_31
- VCC_NCTF_32
- VCC_NCTF_33
- VCC_NCTF_34
- VCC_NCTF_35
- VCC_NCTF_36
- VCC_NCTF_37
- VCC_NCTF_38



Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially.





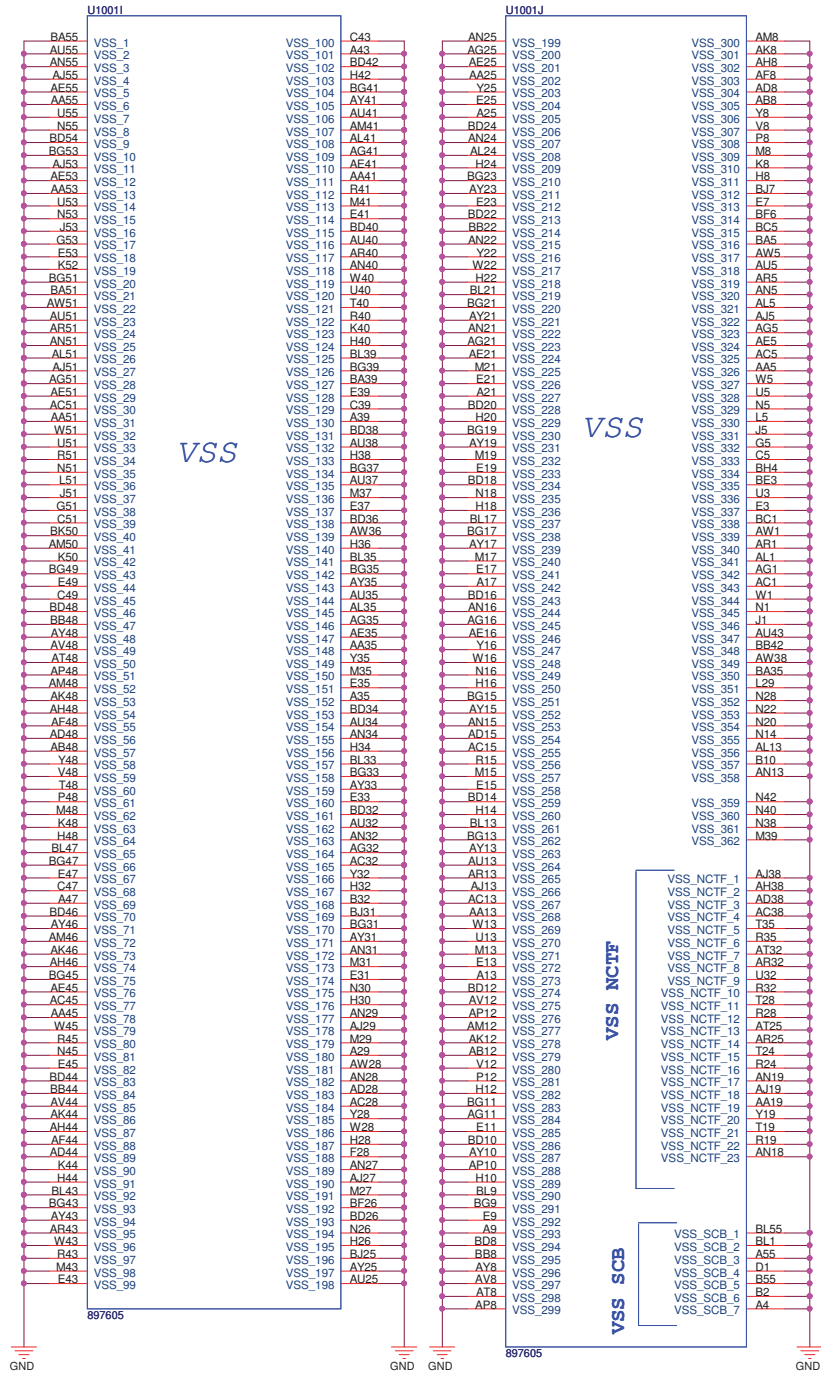
<http://laptop-motherboard-schematic.blogspot.com/>

-Variant Name-

ASUS **Title :NB GS45 POWER**

ASUSTeK COMPUTER INC. **Engineer: Jack Hsu**

Size	Project Name	Rev
C	UL50AT	2.0
Date: Friday, October 16, 2009		Sheet 15 of 97



<Variant Name>

ASUS Title : NB GS45 GND
 ASUSTek COMPUTER INC. Engineer: Jack Hsu

Size	Project Name	Rev
Custom	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 16 of 97



CFG5 : DMI STRAP
H = DMI X 4 (Default)
L = DMI X 2



CFG6 : ITPM Host Interface (Relate to SPI_MOSI)
H = ITPM Disable (Default)
L = ITPM enable (Can disable by SW)



CFG7 : Intel ME Crypto Strap
H = With confidentiality (Default)
L = Without confidentiality



CFG9 : PCIE Graphic Lane Reverse
H = Normal (Default)
L = Lanes Reverse



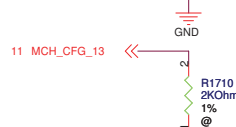
CFG10 : PCIE Loopback
H = Disable (Default)
L = Enable



CFG16 : FSB Dynamic ODT
H = Enable (Default)
L = Disable

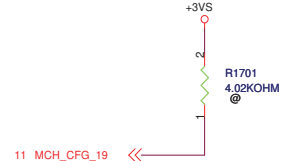


CFG12 : ALL-Z Mode
H = Disable (Default)
L = Enable

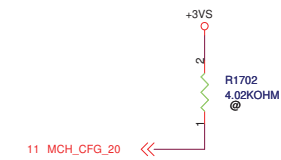


CFG13 : XOR Mode
H = Disable (Default)
L = Enable

CFG [13:12] : XOR/ALL-Z
 00 = Reserved
 01 = XOR Mode Enabled
 10 = All-Z Mode Enabled
 11 = Normal Operation (Default)



CFG19 : DMI Lane Reversal
H = DMI Lane Reversal
L = Normal (Default)



CFG20 : SDVO/PCIE CONCURRENT MODE
L = Only Digital display port or PCIE is Operational (Default)
H = Digital display port and PCIE are operating simultaneously via the PEG port

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<http://laptop-motherboard-schematic.blogspot.com/>

-Variant Name-		
		Title :
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu
Size	Project Name	Rev
C	UL50AT	2.0
Date: Friday, October 16, 2009		Sheet 18 of 97

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<http://laptop-motherboard-schematic.blogspot.com/>

-Variant Name-		
		Title :
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu
Size	Project Name	Rev
C	UL50AT	2.0
Date: Friday, October 16, 2009		Sheet 19 of 97

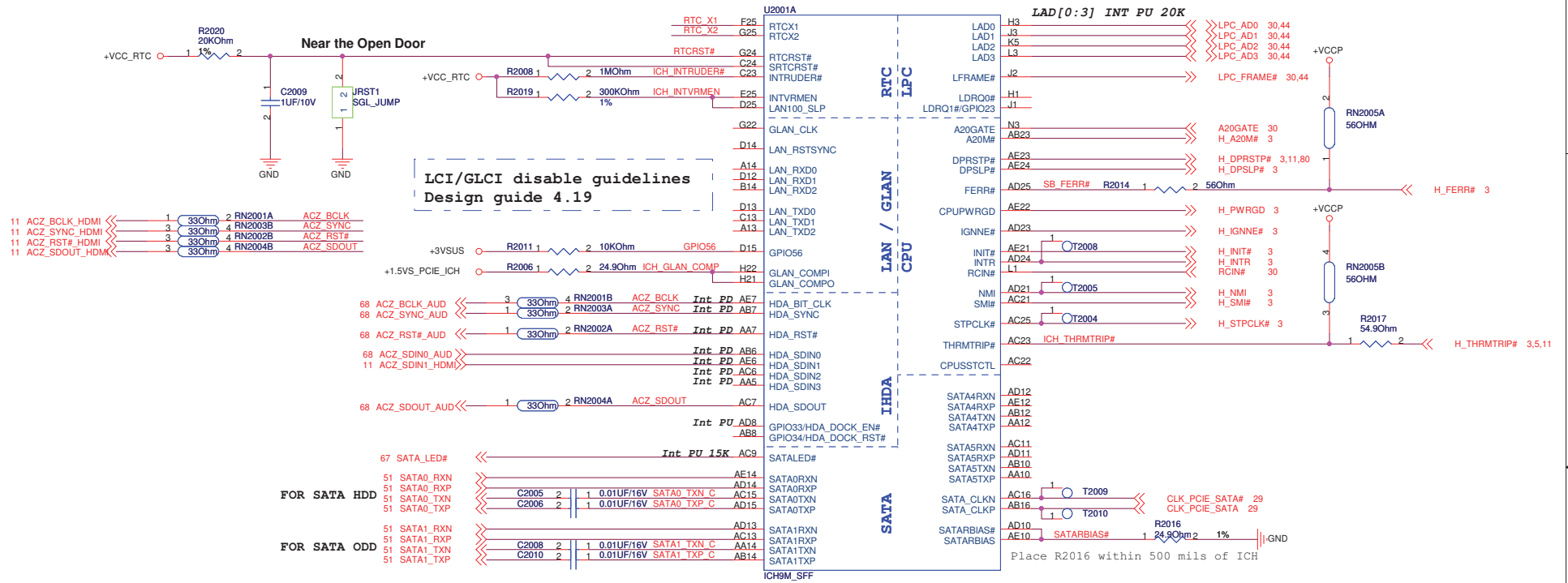
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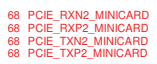
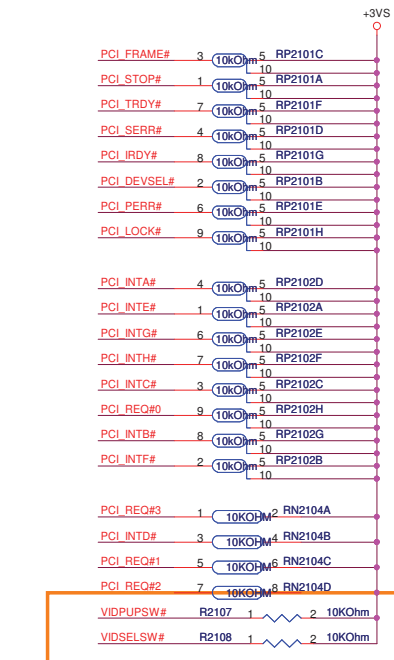
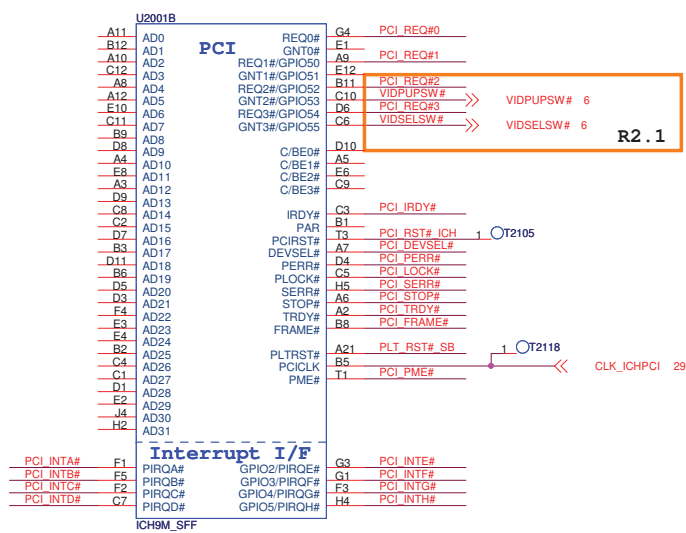
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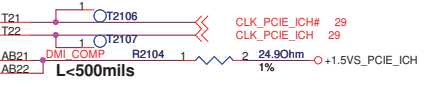
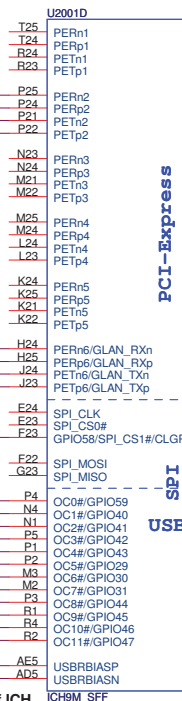
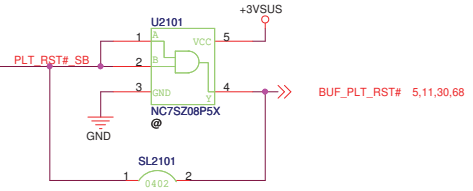
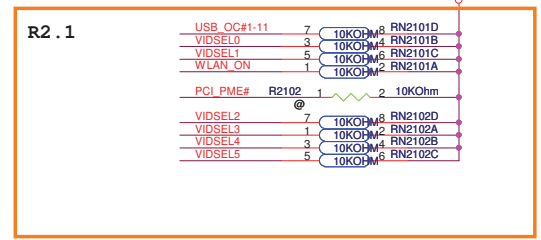
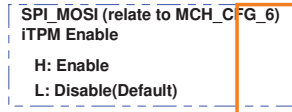
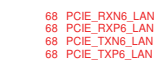
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PCIE 1	
PCIE 2	WLAN
PCIE 3	
PCIE 4	
PCIE 5	
PCIE 6	GLAN



ICH9 Boot BIOS select

	GNT#0	SPICS#1	(default)
LPC	11	1	1
PCI	10	1	0
SPI	01	0	1

- USB 0 USB Conn.
- USB 1 USB Conn.
- USB 2 Bluetooth
- USB 3
- USB 4 CMOS Camera
- USB 5 Card Reader
- USB 6 WiMax
- USB 7
- USB 8
- USB 9
- USB 10 USB Conn.
- USB 11

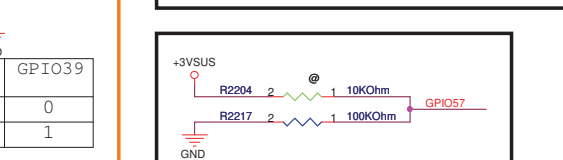
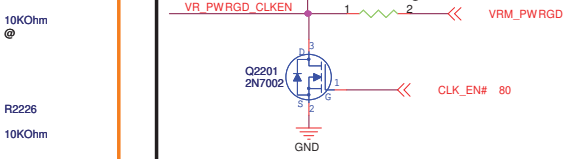
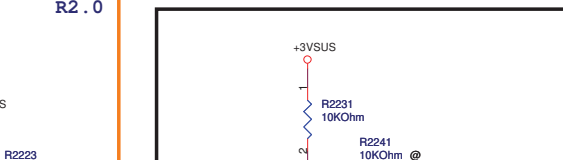
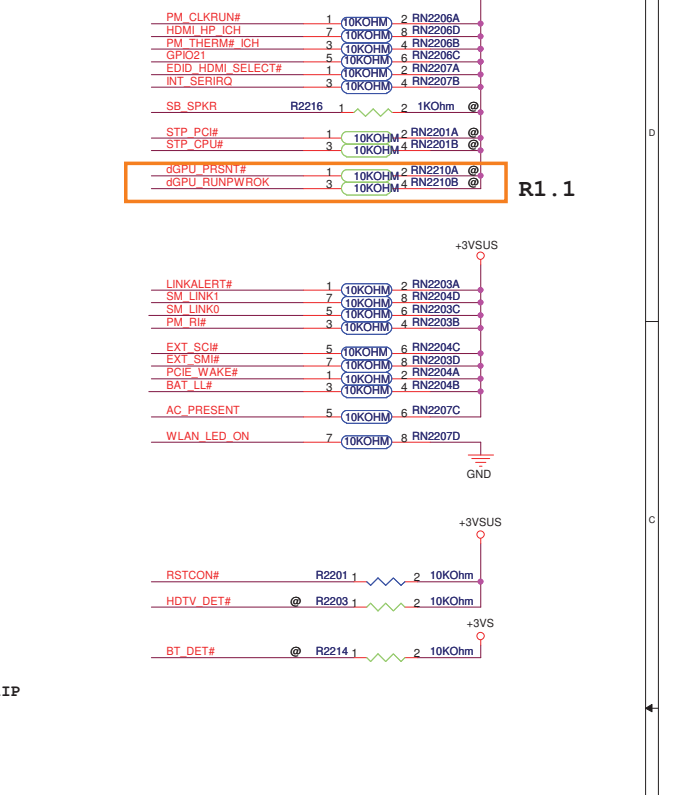
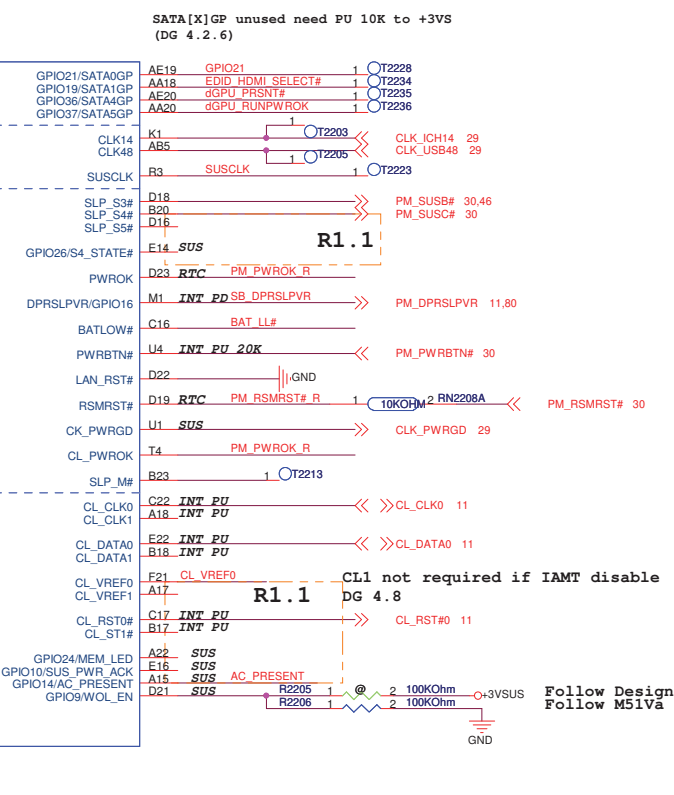
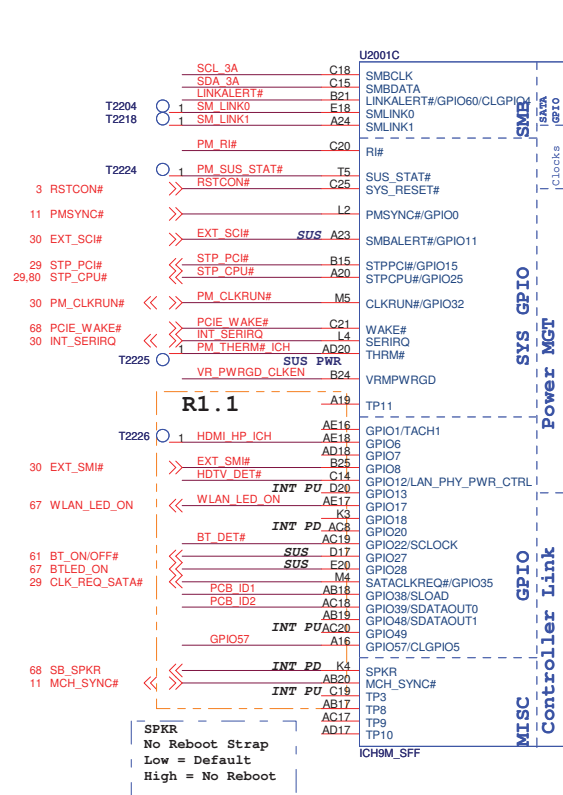
ASUS Title : SB ICH9M (2)

ASUSTeK COMPUTER INC. Engineer: Jack Hsu

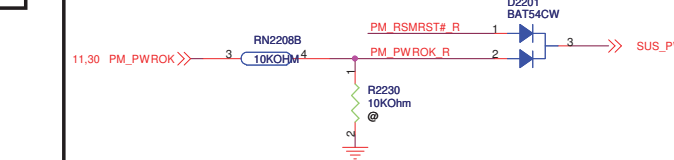
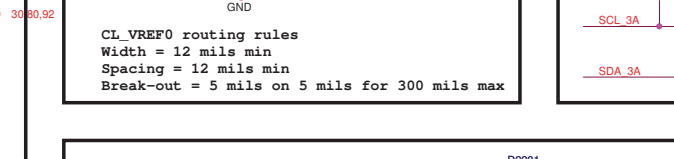
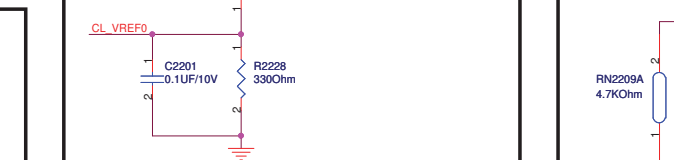
Size Project Name

Custom **UL50AT**

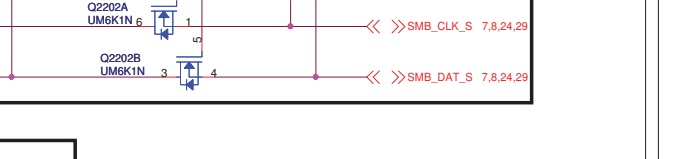
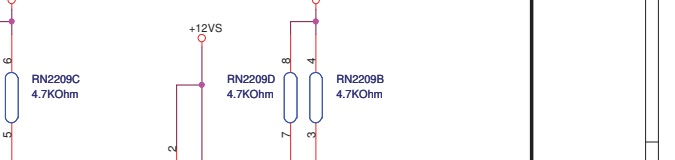
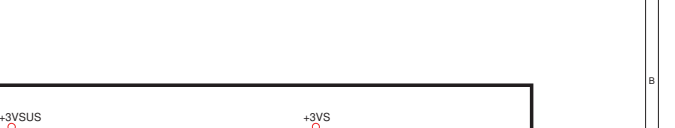
Date: Friday, October 16, 2009 Sheet 21 of 97



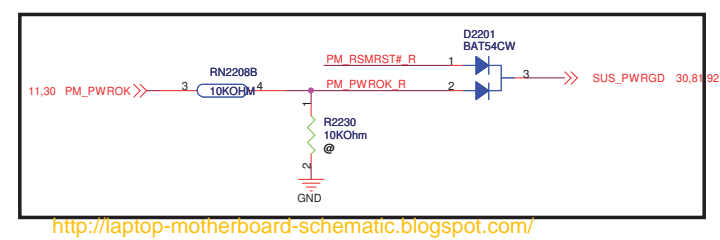
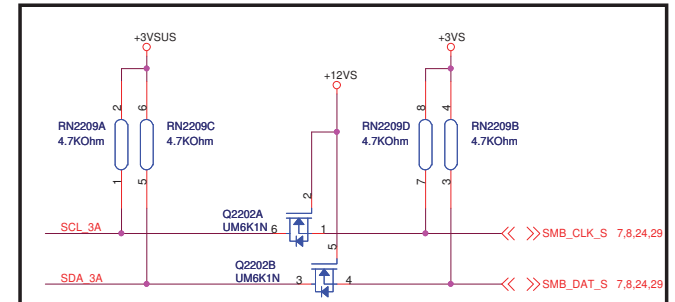
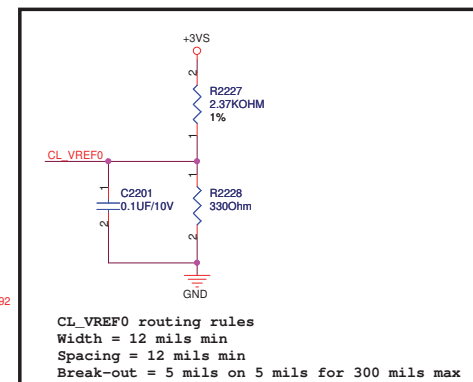
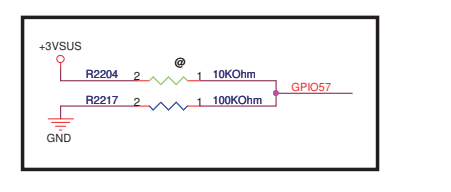
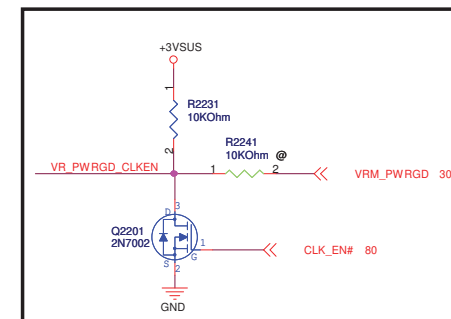
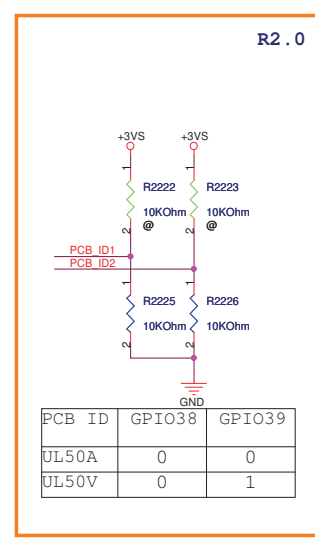
PCB ID	GPIO38	GPIO39
UL50A	0	0
UL50V	0	1



PCB ID	GPIO38	GPIO39
UL50A	0	0
UL50V	0	1



PCB ID	GPIO38	GPIO39
UL50A	0	0
UL50V	0	1



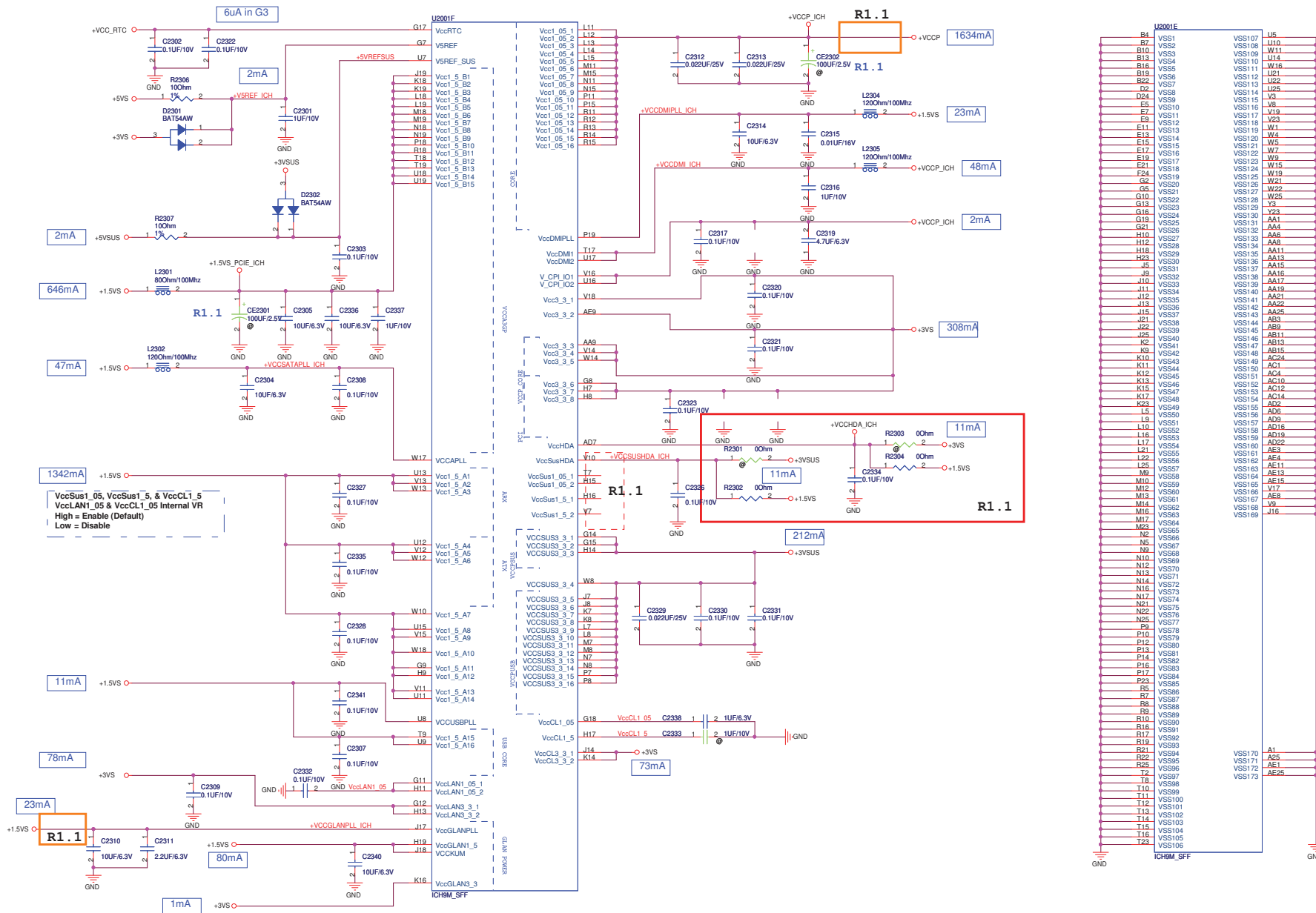
<Variant Name>

ASUS Title: **SB ICH9M (3)**

ASUSTeK COMPUTER INC. Engineer: **Jack Hsu**

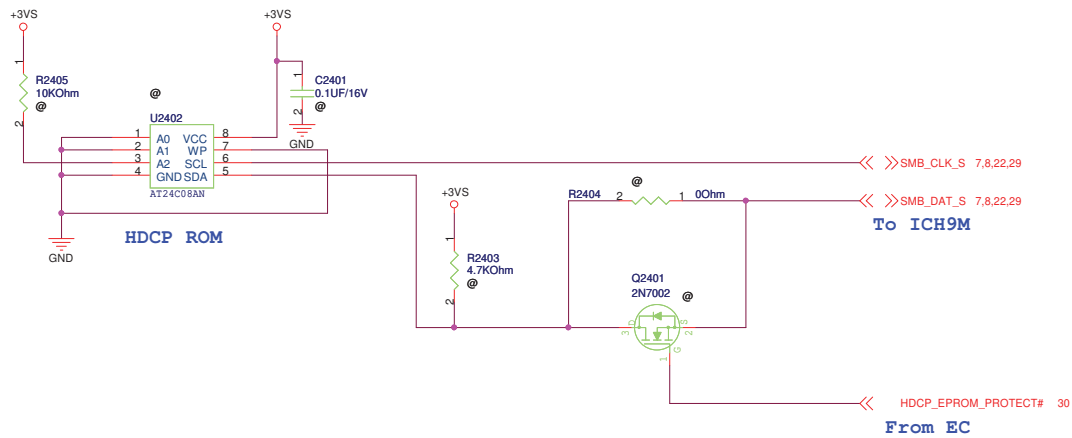
Size: **UL50AT** Project Name: **UL50AT**

Date: **Friday, October 16, 2009** Sheet: **22** of **97**



VccSus1_05, VccSus1_5, & VccCL1_5
 VccLAN1_05 & VccCL1_05 Internal VR
 High = Enable (Default)
 Low = Disable

U2001E	VSS107	U15
B4	VSS107	L15
B7	VSS108	L10
B10	VSS109	LW11
B13	VSS110	L14
B16	VSS111	LW16
B19	VSS112	L21
B22	VSS113	L22
D2	VSS114	L25
D24	VSS115	V3
E7	VSS116	V8
E9	VSS117	V9
E11	VSS118	W1
E13	VSS119	W2
E16	VSS120	W4
E17	VSS121	W5
E19	VSS122	W7
E21	VSS123	W9
F24	VSS124	W15
G5	VSS125	W22
G6	VSS126	W21
G8	VSS127	W25
G10	VSS128	W22
G12	VSS129	Y23
G13	VSS130	AA1
G16	VSS131	AA6
G19	VSS132	AA4
G21	VSS133	AA8
H10	VSS134	AA6
H12	VSS135	AA11
H18	VSS136	AA19
H23	VSS137	AA15
J5	VSS138	AA16
J6	VSS139	AA17
J9	VSS140	AA19
J11	VSS141	AA1
J12	VSS142	AA2
J15	VSS143	AA25
J21	VSS144	AB3
J22	VSS145	AB9
J25	VSS146	AB11
K2	VSS147	AB13
K9	VSS148	AB15
K10	VSS149	AC24
K11	VSS150	AC1
K12	VSS151	AC4
K13	VSS152	AC10
K15	VSS153	AC12
K17	VSS154	AC14
K23	VSS155	AD2
L5	VSS156	AD6
L9	VSS157	AD9
L10	VSS158	AD16
L16	VSS159	AD19
L17	VSS160	AD22
L21	VSS161	AE3
L22	VSS162	AE4
M5	VSS163	AE11
M9	VSS164	AE13
M10	VSS165	AE15
M12	VSS166	V17
M14	VSS167	AE8
M16	VSS168	V9
M17	VSS169	J16
M23	VSS170	A1
N2	VSS171	A25
N5	VSS172	AE1
N9	VSS173	AE25
N10		
N12		
N13		
N14		
N16		
N17		
N22		
N25		
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R10		
R16		
R16		
R17		
R19		
R21		
R21		
R22		
R25		
T2		
T2		
T8		
T10		
T11		
T12		
T13		
T14		
T15		
T16		
T23		



<Variant Name>

ASUS		Title : SB ICH9M (5)	
ASUSTeK COMPUTER INC.		Engineer: <i>Jack Hsu</i>	
Size	Project Name		Rev
Custom	UL50AT		2.0
Date: Friday, October 16, 2009	Sheet	24	of 97

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-Variant Name-		
		Title :
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu
Size	Project Name	Rev
C	UL50AT	2.0
Date: Friday, October 16, 2009		Sheet 26 of 97

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<http://laptop-motherboard-schematic.blogspot.com/>

-Variant Name-		Title :	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	26 of 97

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<http://laptop-motherboard-schematic.blogspot.com/>

-Variant Name-		Title :	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	27 of 97

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<http://laptop-motherboard-schematic.blogspot.com/>

<Variant Name>

		Title :
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu
Size C	Project Name UL50AT	Rev 2.0
Date: Friday, October 16, 2009		Sheet 28 of 97

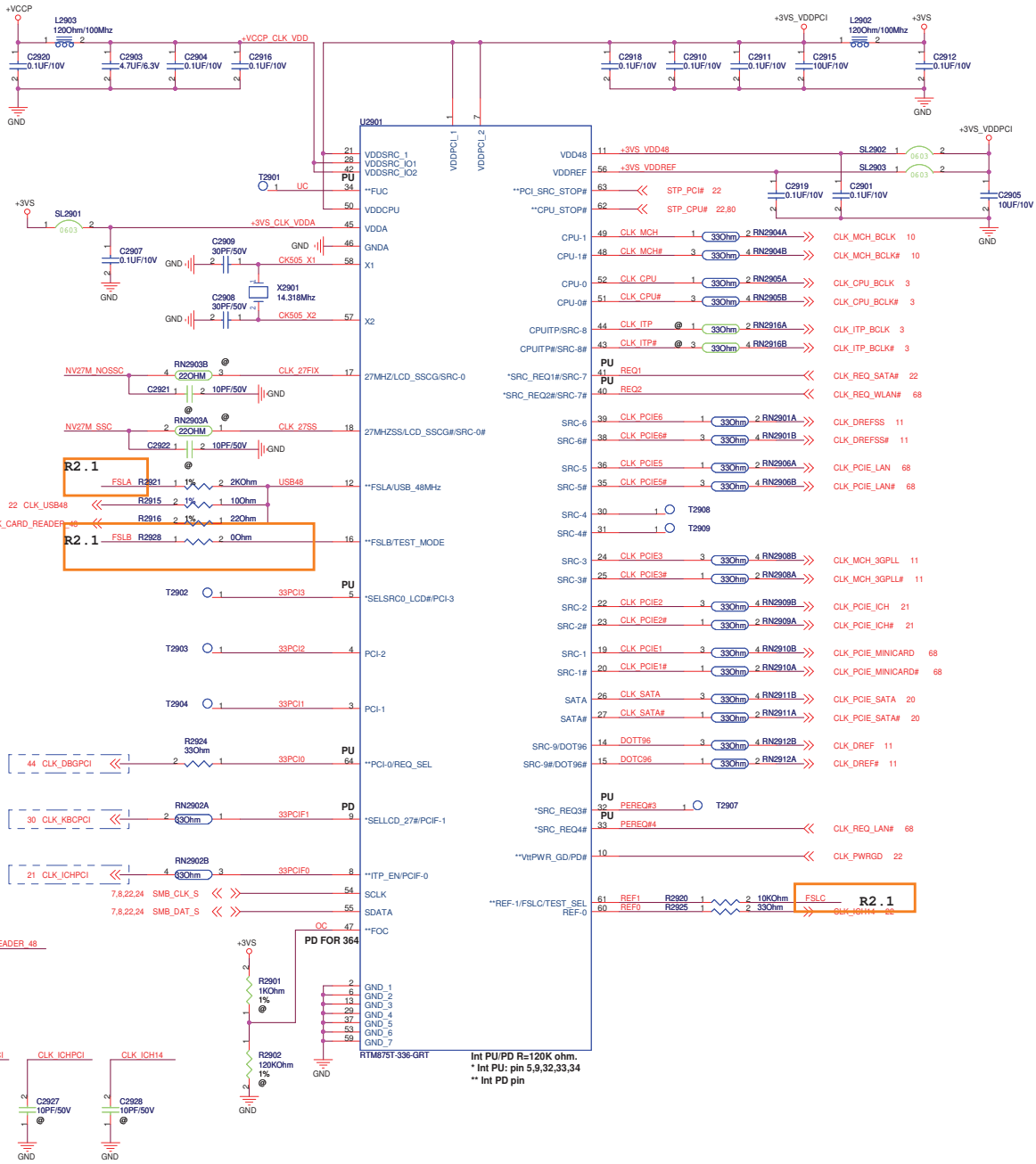
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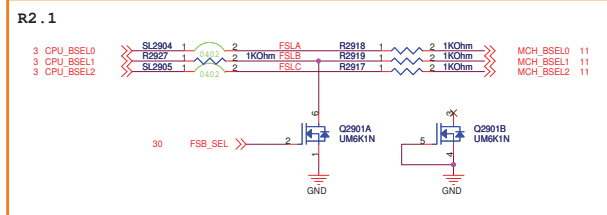
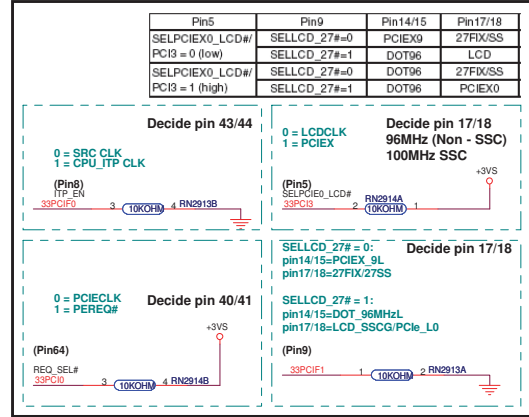
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Latched Input Select



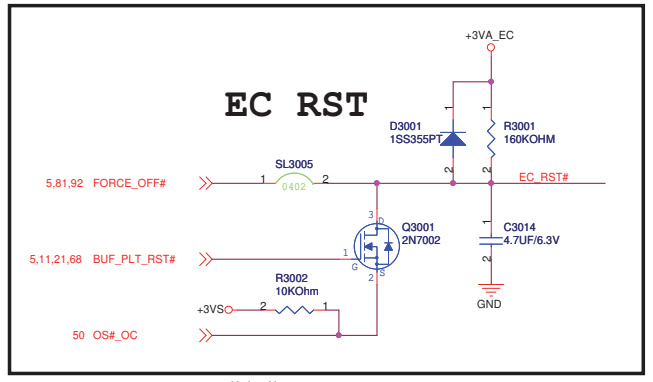
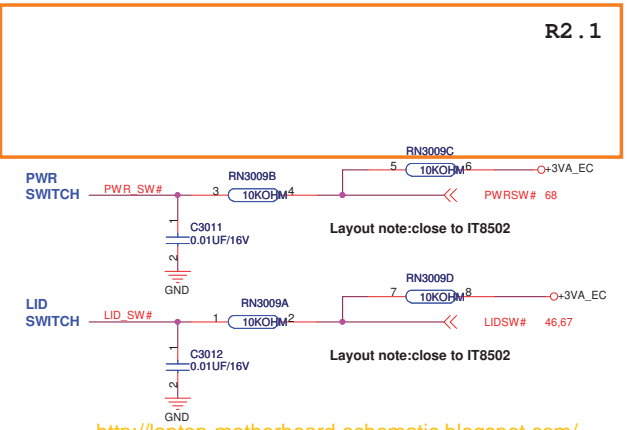
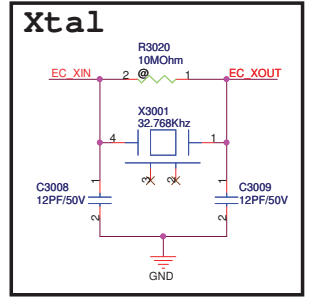
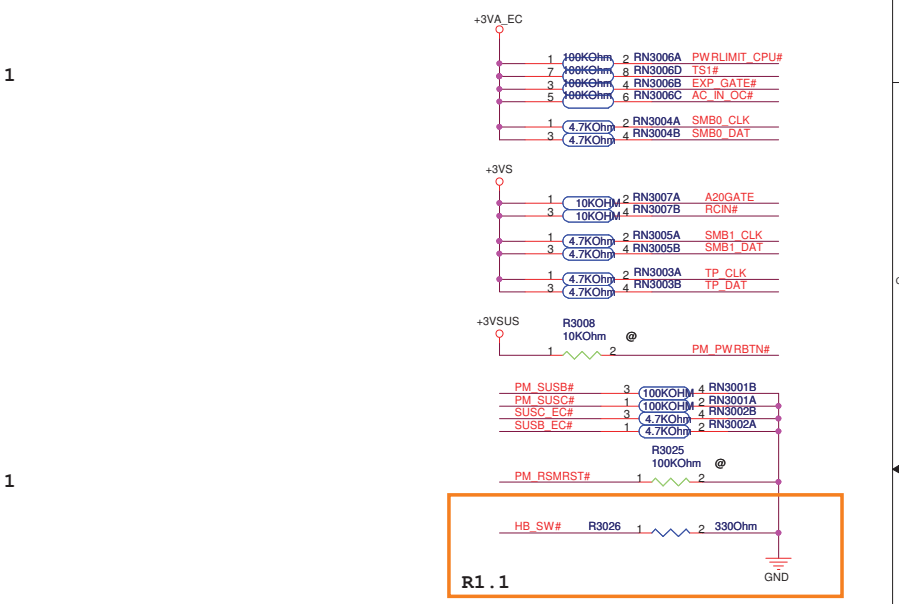
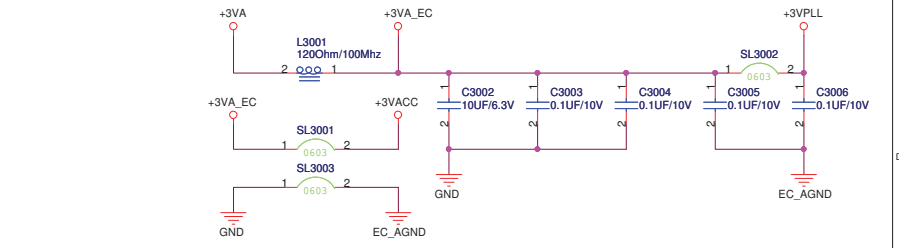
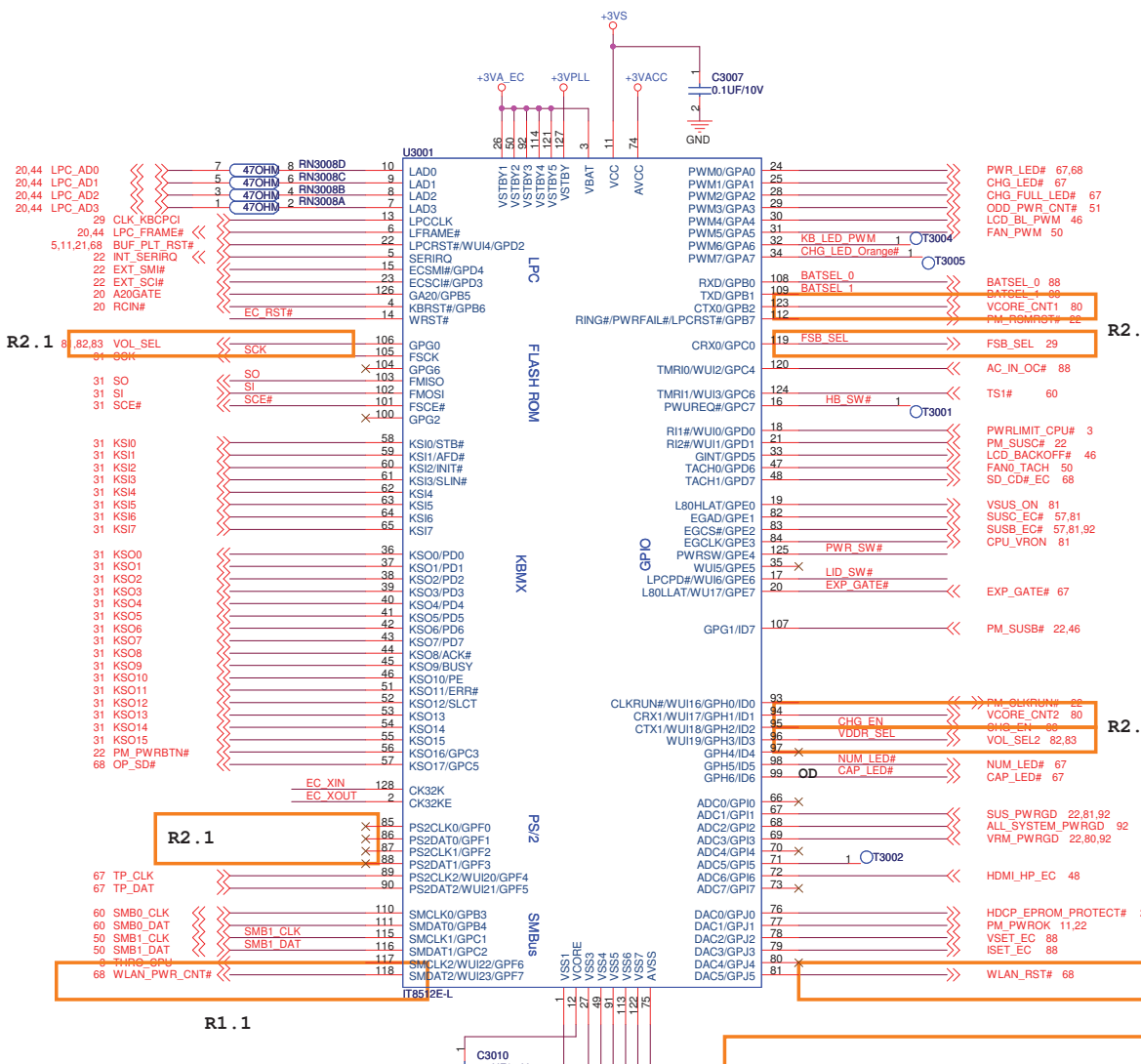
BCLK	FSB	FSLC	FSLB	FSLA
166	667	0	1	1
200	800	0	1	0
266	1066	0	0	0

to 12p-DB

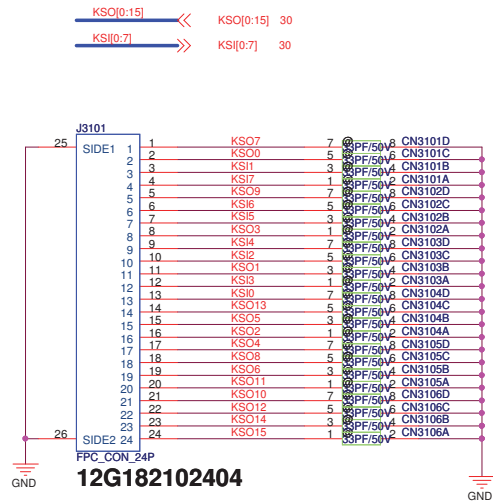
to EC-8512

to ICH9M

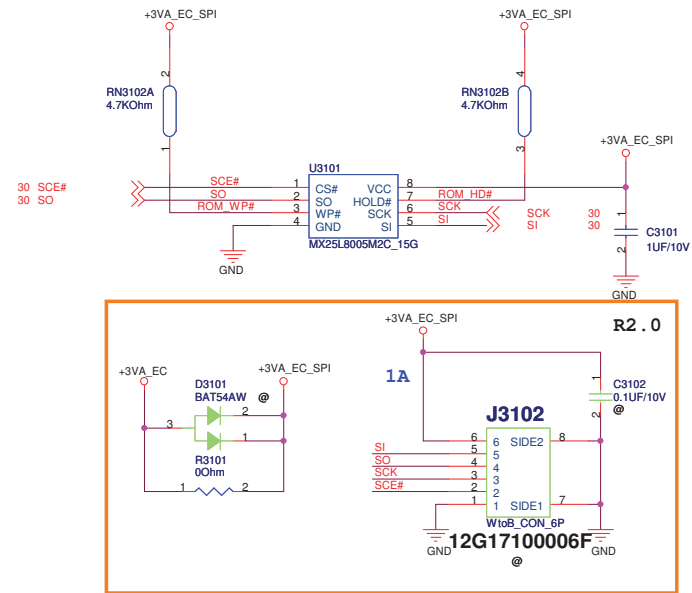
Int PU/PD R=120K ohm.
* Int PU: pin 5,9,32,33,34
** Int PD pin



Internal Keyboard



SPI Flash ROM (8Mb)



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<http://laptop-motherboard-schematic.blogspot.com/>

-Variant Name-		Title: <Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	32 of 97

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<http://laptop-motherboard-schematic.blogspot.com/>

-Variant Name-		Title : <Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet 33 of 97	

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<http://laptop-motherboard-schematic.blogspot.com/>

-Variant Name-		Title :<Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	34 of 97

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<http://laptop-motherboard-schematic.blogspot.com/>

-Variant Name>

		Title :<Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	35 of 97

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<http://laptop-motherboard-schematic.blogspot.com/>

-Variant Name>

		Title :<Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	38 of 97

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<http://laptop-motherboard-schematic.blogspot.com/>

-Variant Name>

		Title :<Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	37 of 97

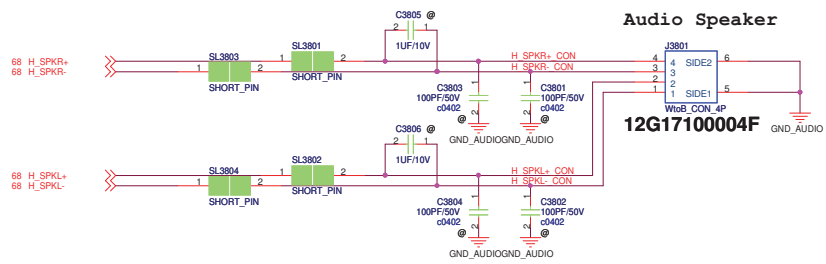
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<http://laptop-motherboard-schematic.blogspot.com/>

-Variant Name-		Title :<Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	39 of 97

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<http://laptop-motherboard-schematic.blogspot.com/>

-Variant Name-		
		Title :
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu
Size	Project Name	Rev
C	UL50AT	2.0
Date: Friday, October 16, 2009		Sheet 40 of 97

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<http://laptop-motherboard-schematic.blogspot.com/>

-Variant Name-		
		Title :
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu
Size	Project Name	Rev
C	UL50AT	2.0
Date: Friday, October 16, 2009		Sheet 41 of 97

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<http://laptop-motherboard-schematic.blogspot.com/>

-Variant Name-		Title :<Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
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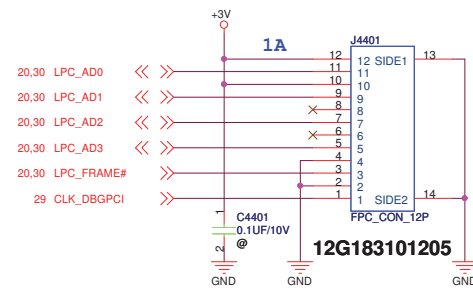
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<http://laptop-motherboard-schematic.blogspot.com/>

-Variant Name>

		Title :<Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	43 of 97

LPC DEBUG PORT



<Variant Name>

ASUS		Title : DEBUG PORT
ASUSTeK COMPUTER INC.		Engineer: <i>Jack Hsu</i>
Size	Project Name	Rev
Custom	UL50AT	2.0
Date: Friday, October 16, 2009	Sheet 44 of 97	

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<http://laptop-motherboard-schematic.blogspot.com/>

-Variant Name>

		Title :<Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	45 of 97

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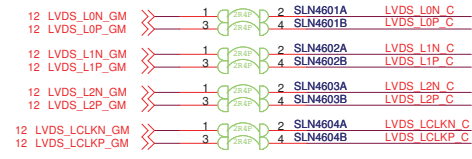
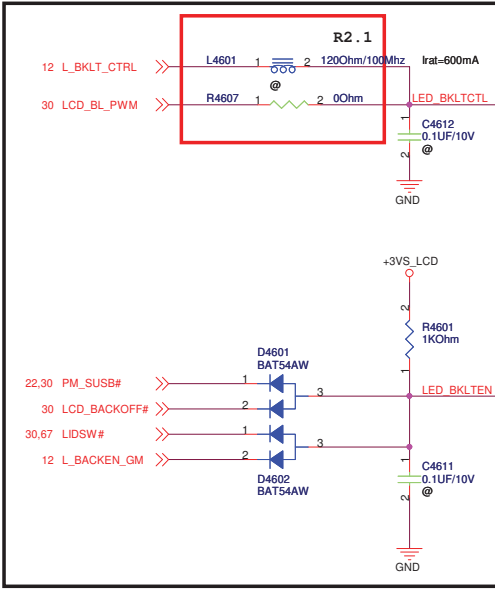
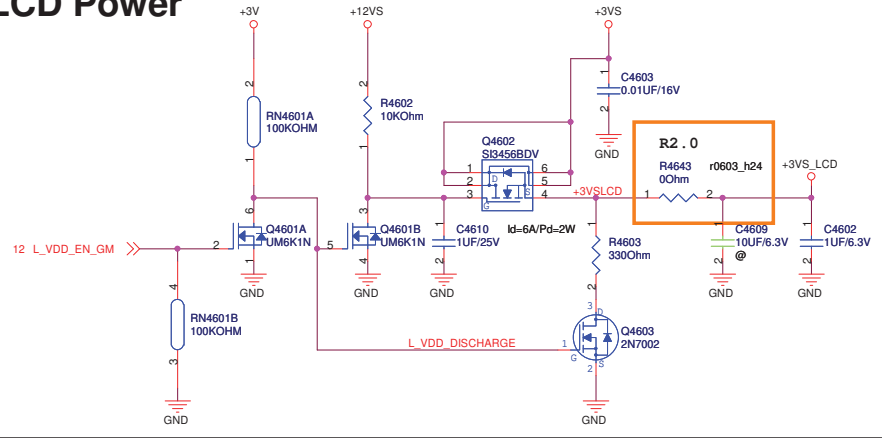
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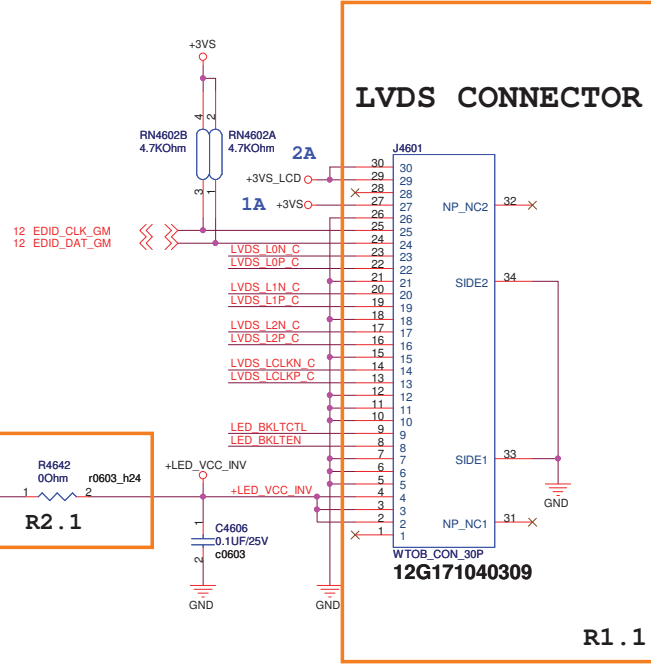
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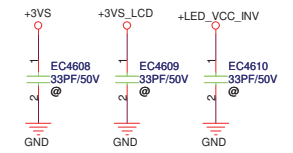
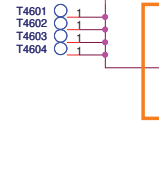
LCD Power



LVDS CONNECTOR



AC_BAT_SYS



<Variant Name>

ASUS Title : LVDS CONNECTOR

ASUSTeK COMPUTER INC. Engineer: Jack Hsu

Size	Project Name	Rev
Custom	UL50AT	2.0

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<http://laptop-motherboard-schematic.blogspot.com/>

-Variant Name>

		Title :<Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	47 of 97



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<http://laptop-motherboard-schematic.blogspot.com/>

-Variant Name-			
		Title : HDMI LEVEL SHIFT	
ASUSTeK COMPUTER INC.		Engineer: <i>Jack Hsu</i>	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	49 of 97

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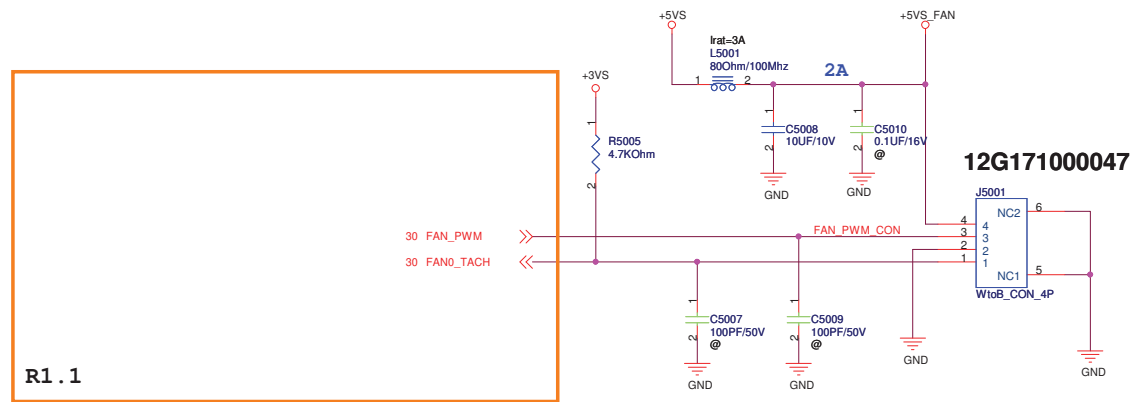
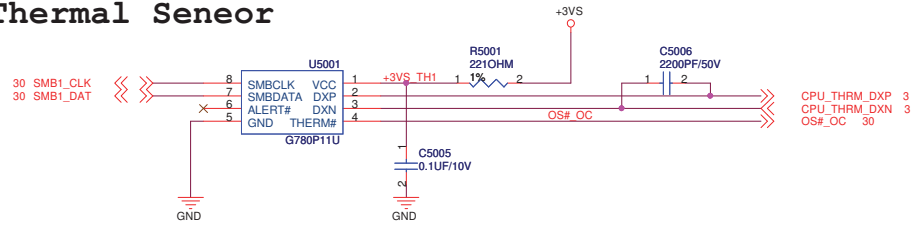
1nd: 06G023096010 G780P11U SOP-8
 2nd: 06G023026012 MAX6657YMS+ SOP-8

Route CPU_THRM_DA , CPU_THRM_DC and MEM_THERM_DA , MEM_THERM_DC on the same layer

-----OTHER SIGNALS
 10 mils
 =====GND
 10 mils
 =====H_THERMDA(10 mils)
 10 mils
 =====H_THERMDC(10 mils)
 10 mils
 =====GND
 10 mils
 -----OTHER SIGNALS

Avoid FSB,Power

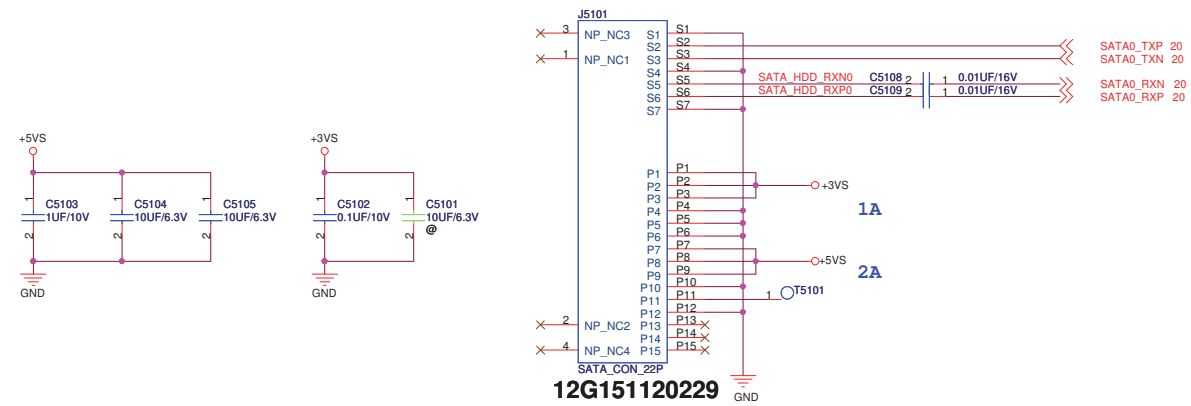
Thermal Seneor



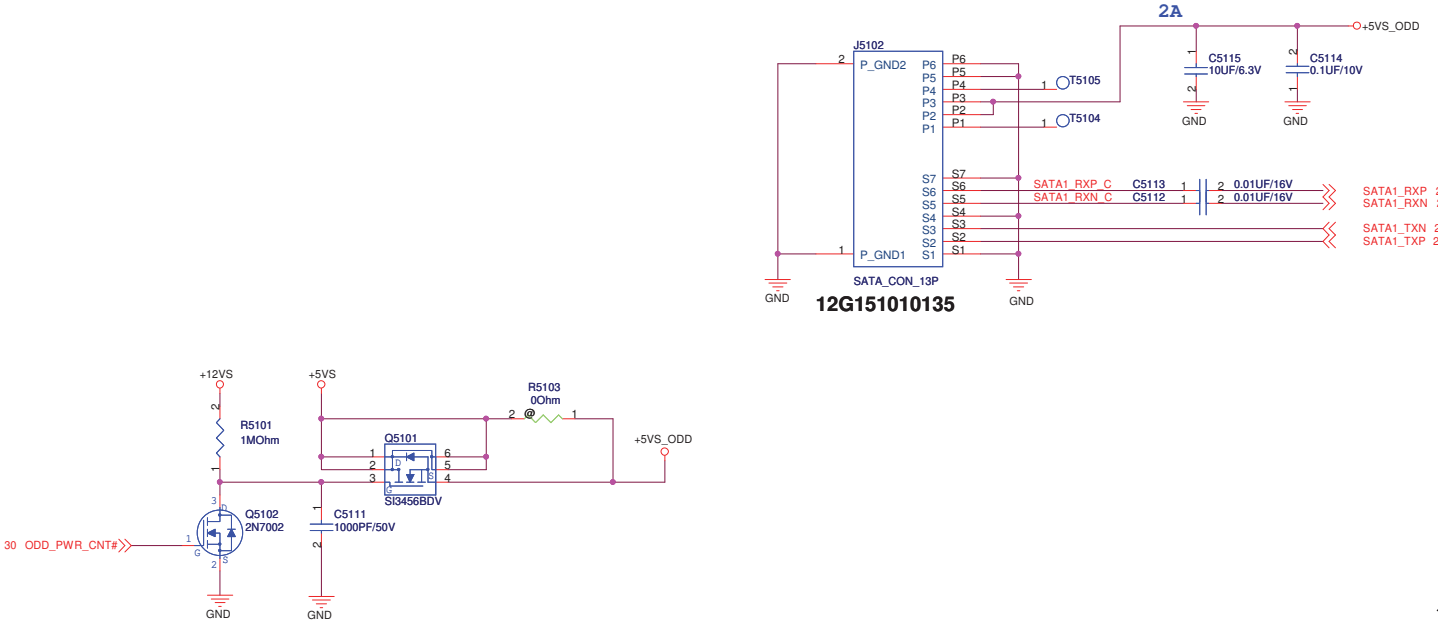
<Variant Name>

ASUS		Title : THERMAL & FAN	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	UL50AT	2.0	
Date: Friday, October 16, 2009	Sheet	50	of 97

SATA HDD



SATA ODD



<Variant Name>

ASUS		Title : SATA HDD & ODD	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	UL50AT	2.0	
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<http://laptop-motherboard-schematic.blogspot.com/>

<Variant Name>

		Title : <Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
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<http://laptop-motherboard-schematic.blogspot.com/>

-Variant Name>

		Title : <Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	53 of 97

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<http://laptop-motherboard-schematic.blogspot.com/>

-Variant Name-		Title : <Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet 54 of 97	

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<http://laptop-motherboard-schematic.blogspot.com/>

-Variant Name-		Title : <Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet 55 of 97	

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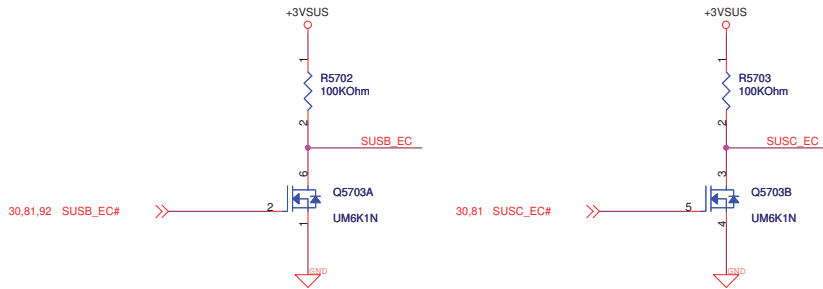
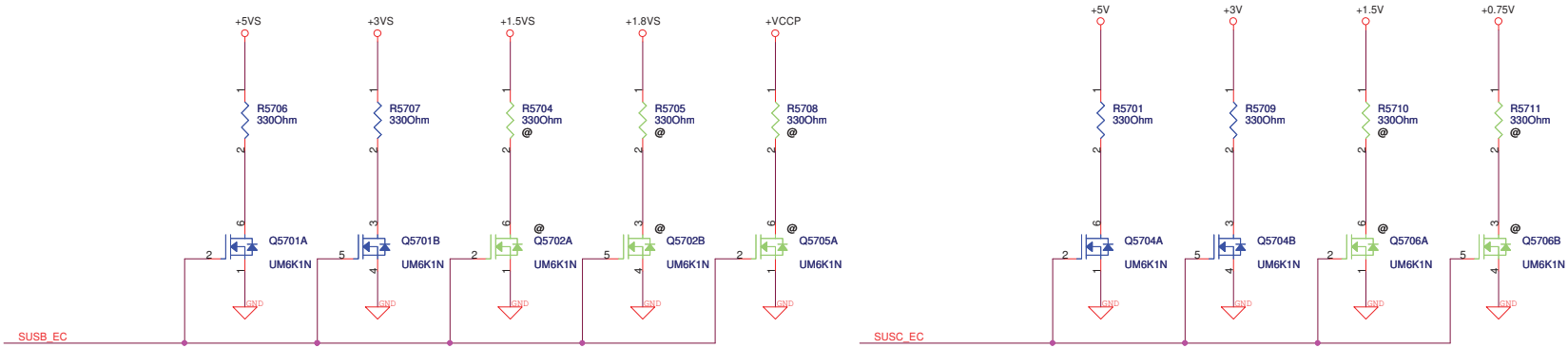
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<Variant Name>

		Title : LID	
ASUSTeK COMPUTER INC.		Engineer: <i>Jack Hsu</i>	
Size	Project Name	Rev	
Custom	UL50AT	2.0	
Date: Friday, October 16, 2009	Sheet	56	of 97

Discharge Circuit



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<http://laptop-motherboard-schematic.blogspot.com/>

-Variant Name-		Title : <Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet 58 of 97	

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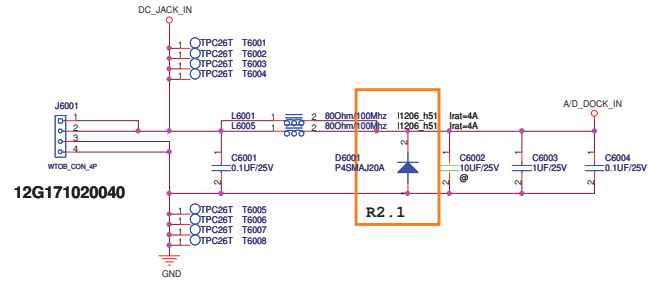
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<http://laptop-motherboard-schematic.blogspot.com/>

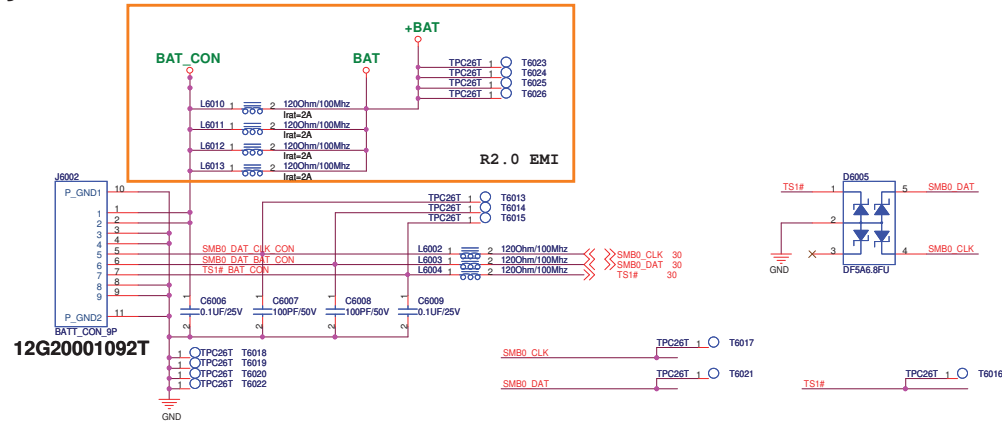
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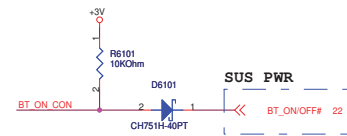
		Title :
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu
Size	Project Name	Rev
C	UL50AT	2.0
Date: Friday, October 16, 2009		Sheet 59 of 97

DC-IN



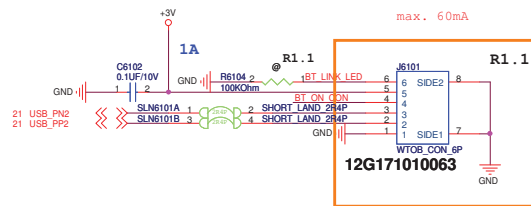
Battery Connector





Bluetooth Connector

max. 60mA



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<http://laptop-motherboard-schematic.blogspot.com/>

-Variant Name-		Title : <Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet 62 of 97	

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<http://laptop-motherboard-schematic.blogspot.com/>

-Variant Name-		Title : <Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	63 of 97

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<http://laptop-motherboard-schematic.blogspot.com/>

-Variant Name-		Title : <Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet 64 of 97	

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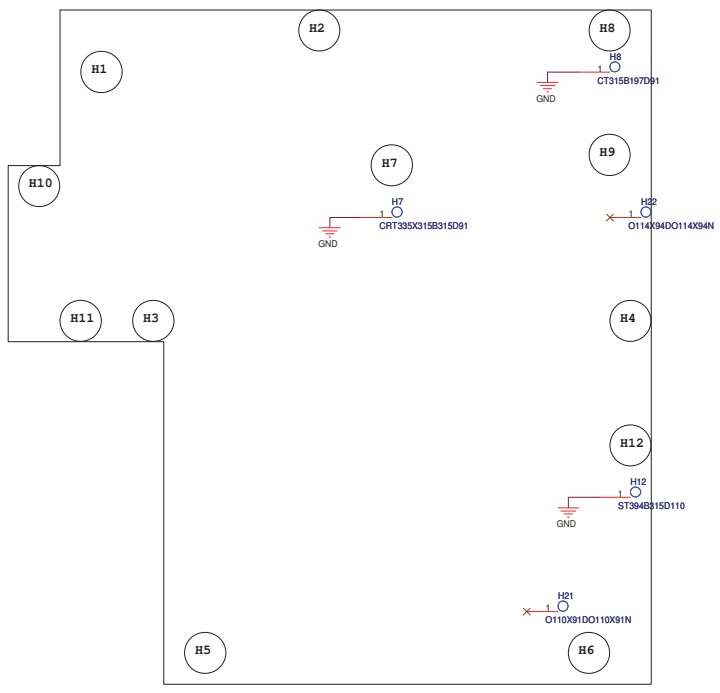
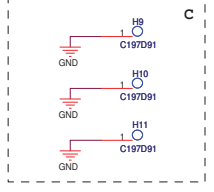
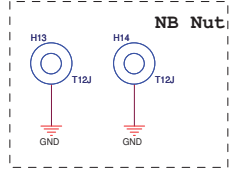
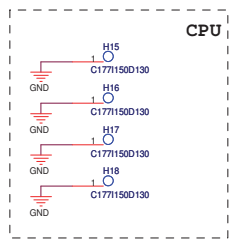
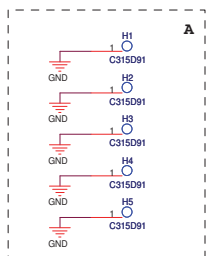
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Screw Hole & SMT Nut



<http://laptop-motherboard-schematic.blogspot.com/>

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<http://laptop-motherboard-schematic.blogspot.com/>

-Variant Name-		
		Title :
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu
Size	Project Name	Rev
C	UL50AT	2.0
Date: Friday, October 16, 2009		Sheet 66 of 97

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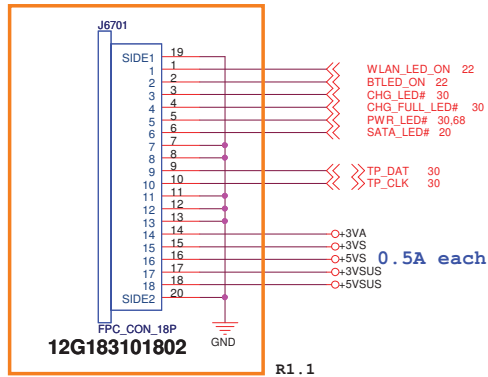
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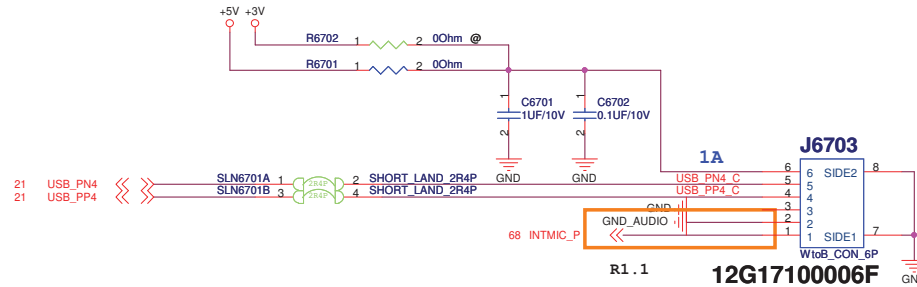
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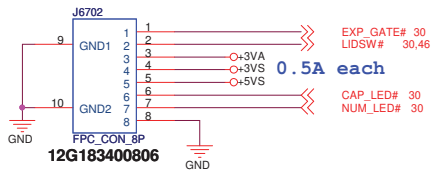
Touch Pad / LED Board



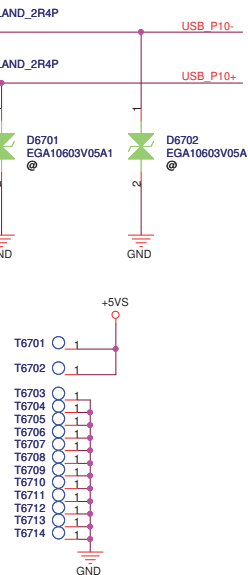
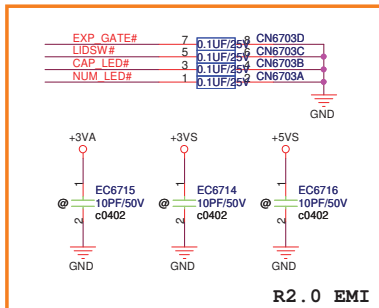
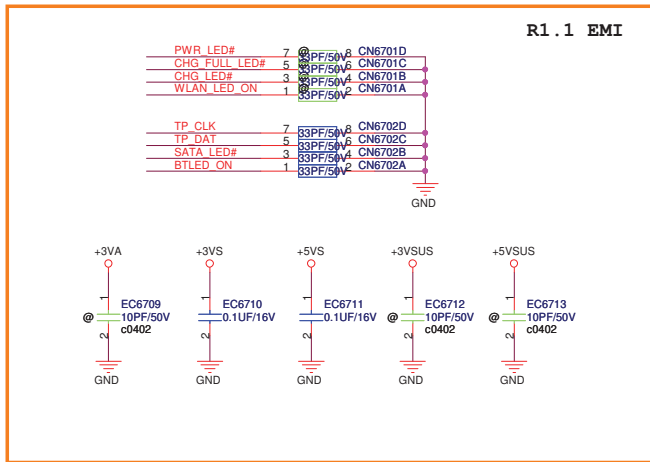
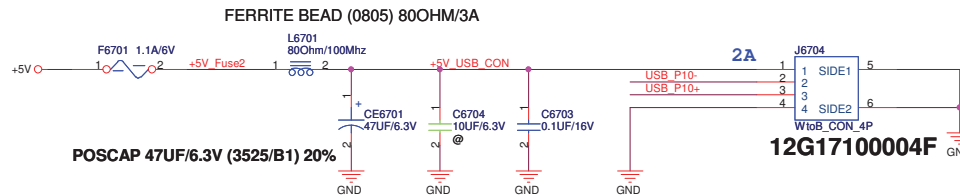
Camera Module



Function Board

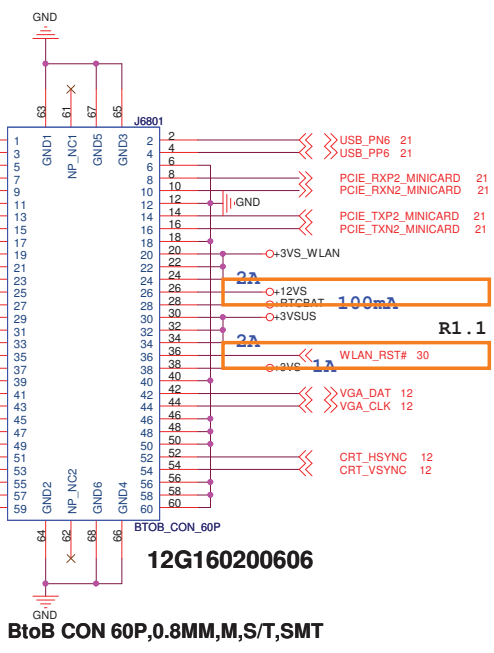
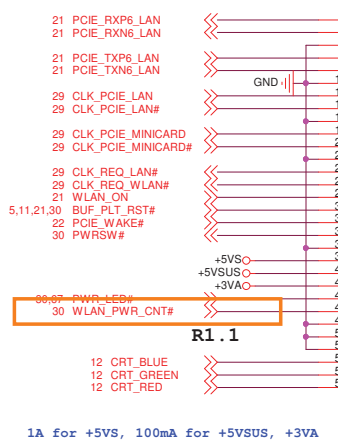
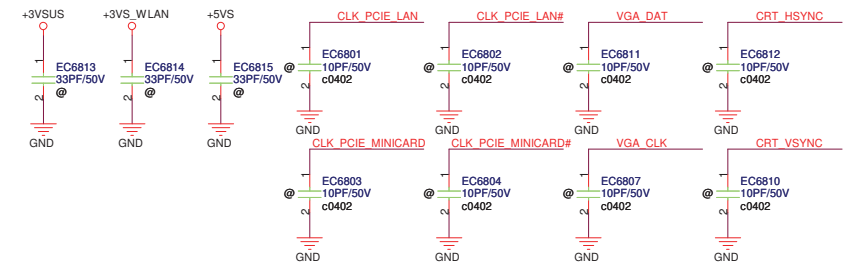
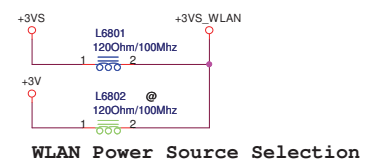


FLY USB Cable



IO BOARD - 02

- LAN IC
- RJ45
- CRT
- RTC Conn.
- MiniCard

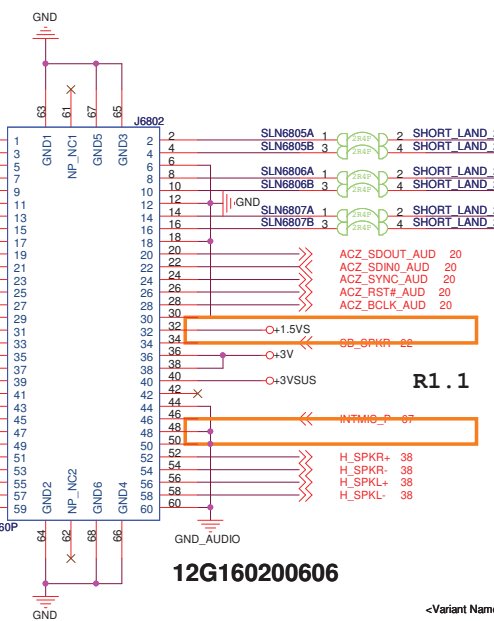
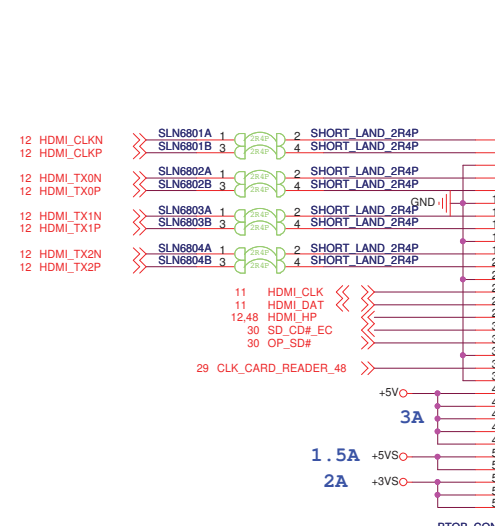
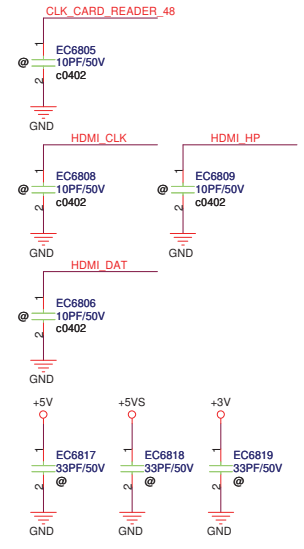


USB 0	USB Conn.
USB 1	USB Conn.
USB 2	Bluetooth
USB 3	
USB 4	CMOS Camera
USB 5	Card Reader
USB 6	WiMax
USB 7	
USB 8	
USB 9	
USB 10	USB Conn.
USB 11	

12G16020060
BtoB CON 60P,0.8MM,M,S/T,SMT

IO BOARD - 01

- HDMI Conn.
- USB Conn. x2
- MIC-IN Conn.
- Head Phone Conn.
- Audio IC
- Card Reader IC
- Card Reader Conn.



USB P5	21
USB PP5	21
USB PN0	21
USB PP0	21
USB PN1	21
USB PP1	21
ACZ_SDOUT_AUD	20
ACZ_SDI0_AUD	20
ACZ_SYNC_AUD	20
ACZ_RST#_AUD	20
ACZ_BCLK_AUD	20
H_SPKR+	38
H_SPKR-	38
H_SPKL+	38
H_SPKL-	38

12G16020060
BtoB CON 60P,0.8MM,M,S/T,SMT

ASUS Logo
Title : B TO B CONNECTOR
 ASUSTeK COMPUTER INC. Engineer: Jack Hsu
 Size Project Name
 Custom UL50AT
 Date: Friday, October 16, 2009 Sheet 68 of 97

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<http://laptop-motherboard-schematic.blogspot.com/>

-Variant Name-	
	
Title : <Title>	
ASUSTeK COMPUTER INC. Engineer: Jack Hsu	
Size	Project Name
C	UL50AT
Date: Friday, October 16, 2009	Rev 2.0
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<http://laptop-motherboard-schematic.blogspot.com/>

		Title: N10M-GE1 (1)	
ASUSTeK COMPUTER INC.		Engineer: Alan Chen	
Size C	Project Name UL50AT	Name	Rev 2.0
Date: Friday, October 16, 2009		Sheet	70 of 97

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<http://laptop-motherboard-schematic.blogspot.com/>

		Title: N10M-GE1 (2)	
ASUSTeK COMPUTER INC.		Engineer: Alan Chen	
Size	Project Name	Rev	
C	UL50AT	2.0	
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<http://laptop-motherboard-schematic.blogspot.com/>

		Title: N10M-GE1 (3)	
<small>ASUSTeK Corporation</small>		Engineer: Alan Chen	
Size C	Project Name UL50AT	Rev 2.0	
<small>Date: Friday, October 16, 2009</small>		<small>Sheet</small> 72	<small>of</small> 97

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<http://laptop-motherboard-schematic.blogspot.com/>

		Title: N10M-GE1 (4)	
ASUSTeK COMPUTER INC.		Engineer: Alan Chen	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	78 of 97

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<http://laptop-motherboard-schematic.blogspot.com/>

		Title: M10M-GE1 (5)	
ASUSTeK COMPUTER INC.		Engineer: Alan Chen	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	74 of 97

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<http://laptop-motherboard-schematic.blogspot.com/>

		Title: N10M-GE1 (6)	
ASUSTeK COMPUTER INC.		Engineer: Alan Chen	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	78 of 97

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<http://laptop-motherboard-schematic.blogspot.com/>

		Title: VGA Power Sequence	
ASUSTeK COMPUTER INC.		Engineer: Alan Chen	
Size C	Project Name UL50AT	Rev 2.0	
Date: Friday, October 16, 2009		Sheet	76 of 97

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<http://laptop-motherboard-schematic.blogspot.com/>

		Title: <input type="text" value="Title"/>	
ASUSTeK COMPUTER INC.		Engineer: Alan Chen	
Size	Project Name	Rev	
C	UL50AT	2.0	<Variant Name>
Date: Friday, October 16, 2009		Sheet	77 of 97

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<http://laptop-motherboard-schematic.blogspot.com/>

		Title: 	
ASUSTeK COMPUTER INC.		Engineer: Alan Chen	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	78 of 97

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<http://laptop-motherboard-schematic.blogspot.com/>

		Title:	
ASUSTeK COMPUTER INC.		Engineer: <i>Alan Chen</i>	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	79 of 97

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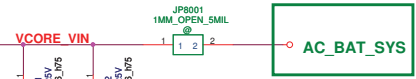
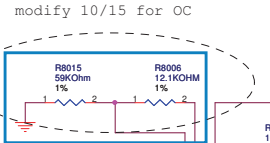
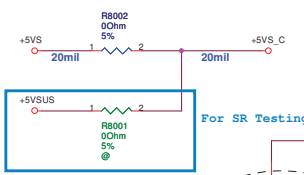
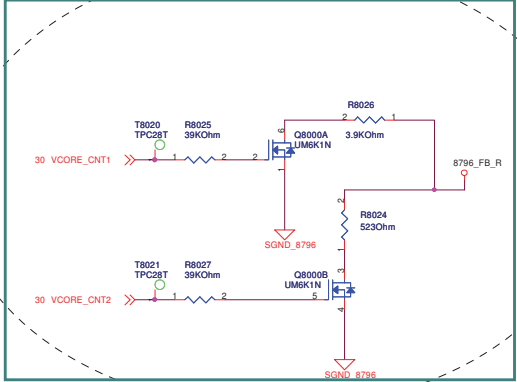
2

1

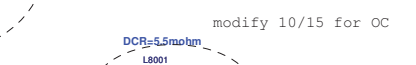
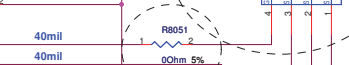
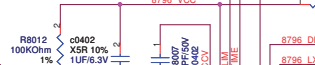
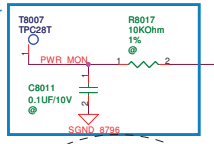
R2.1 7/29 for OC

CPU VID=1.2V

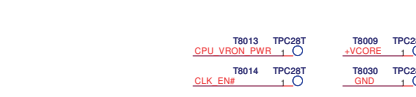
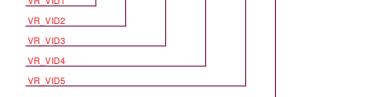
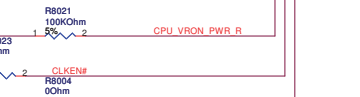
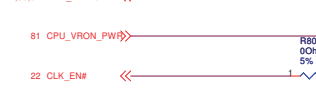
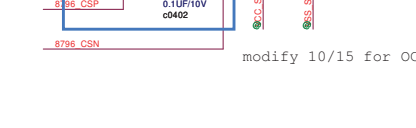
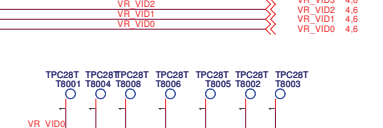
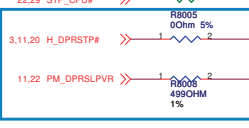
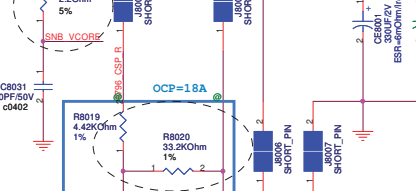
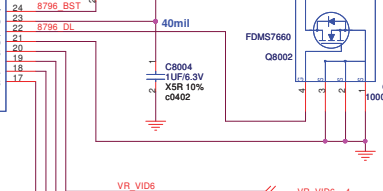
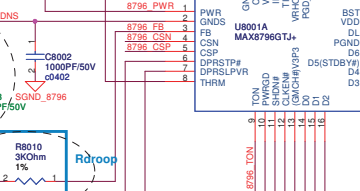
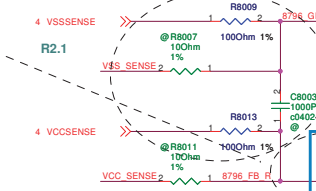
VCORE_CNT1	VCORE_CNT2	Voltage	Offset
H	H	1.3988V	VID+222mV
H	L	1.3488V	VID+26mV
L	H	1.25V	VID+196mV
L	L	1.2V	VID



Power monitor



modify 10/15 for OC



Total count: 37 pcs

- T8013 TPC28T CPU_VRON_PWR 1 0
- T8014 TPC28T CLK_EN# 1 0
- T8015 TPC28T VRM_PWRGD 1 0
- T8028 TPC28T GND 1 0
- T8029 TPC28T GND 1 0
- T8032 TPC28T VCCSENSE 1 0
- T8018 TPC28T VSSSENSE 1 0
- T8019 TPC28T +SYS_C 1 0
- T8009 TPC28T +VCORE 1 0
- T8030 TPC28T GND 1 0
- T8023 TPC28T GND 1 0
- T8028 TPC28T GND 1 0
- T8029 TPC28T GND 1 0

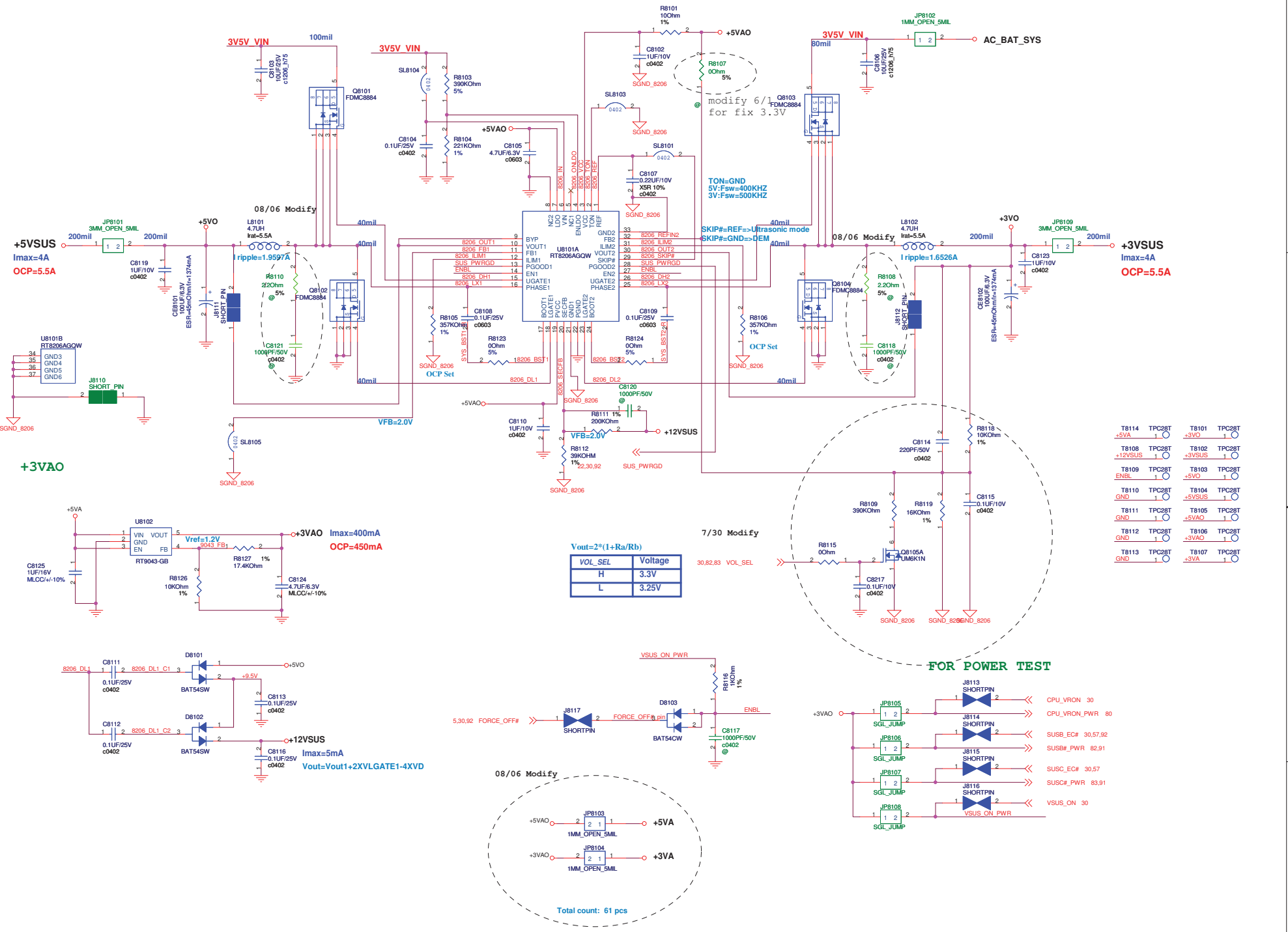
<Variant Name>

Title : POWER_VCORE

ASUSTeK COMPUTER INC. CH/Fre Engineer:

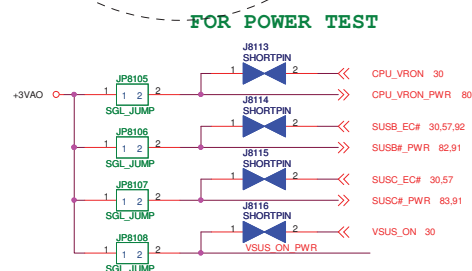
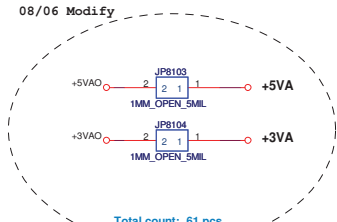
Size	Project Name	Rev
Custom	UL50AT	2.0

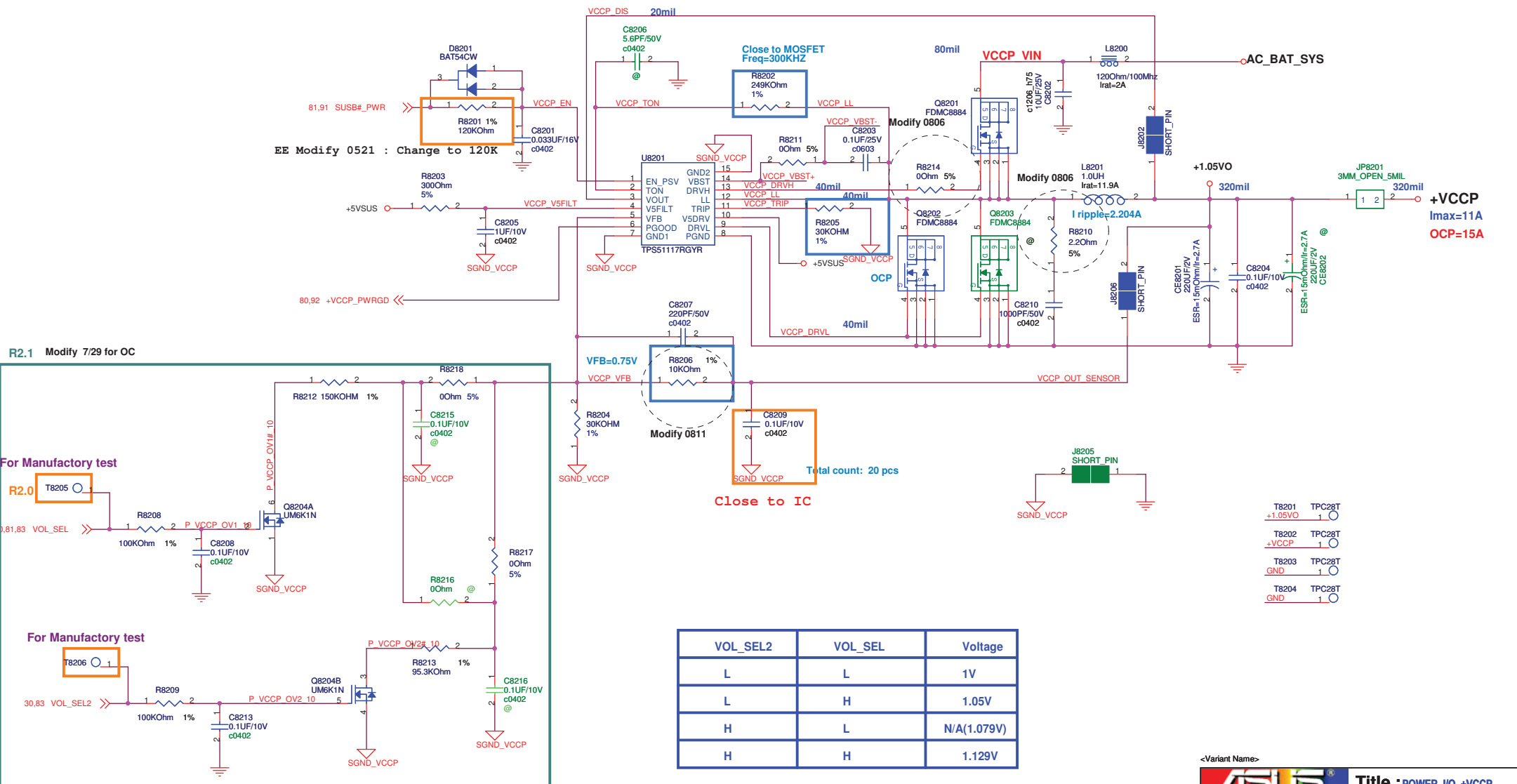
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- T8114 TPC28T -5VA
- T8108 TPC28T +12VSUS
- T8109 ENBL
- T8110 TPC28T GND
- T8111 TPC28T GND
- T8112 TPC28T GND
- T8113 TPC28T GND
- T8101 TPC28T +3VO
- T8102 TPC28T +3VSUS
- T8103 TPC28T +5VO
- T8104 TPC28T +5VSUS
- T8105 TPC28T +5VAO
- T8106 TPC28T +3VAO
- T8107 TPC28T +3VA

VOL_SEL	Voltage
H	3.3V
L	3.25V





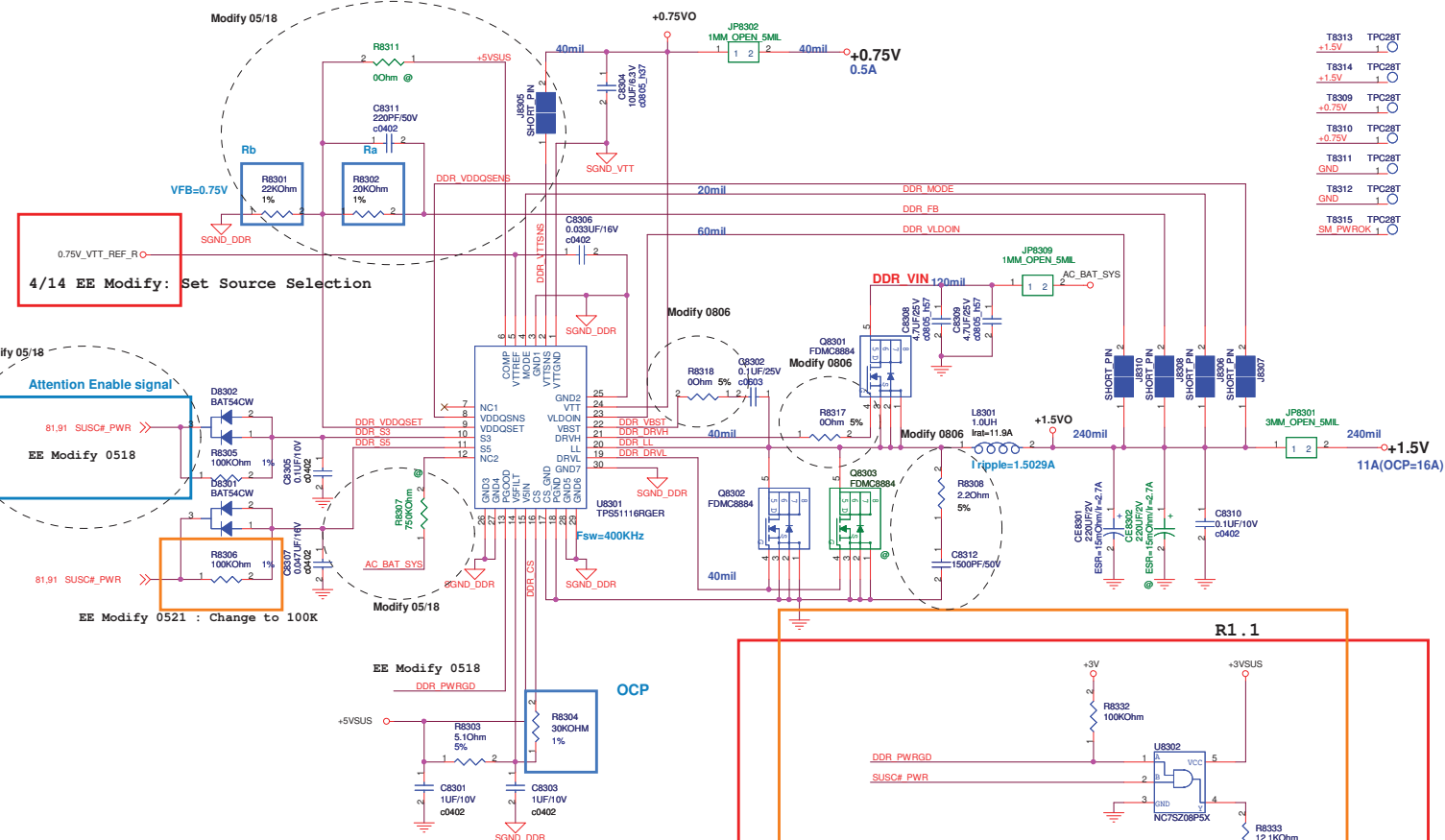
<Variant Name>

ASUS Title : POWER_IO +VCCP

ASUSTek COMPUTER INC. Engineer:

Size	Project Name	Rev
Custom	UL50AT	2.0

Date: Friday, October 16, 2009 Sheet 82 of 97



- T8313 TPC28T 1 1.5V
- T8314 TPC28T 1 1.5V
- T8309 TPC28T 1 0.75V
- T8310 TPC28T 1 0.75V
- T8311 TPC28T 1 GND
- T8312 TPC28T 1 GND
- T8315 TPC28T 1 SM_PWROK

4/14 EE Modify: Set Source Selection

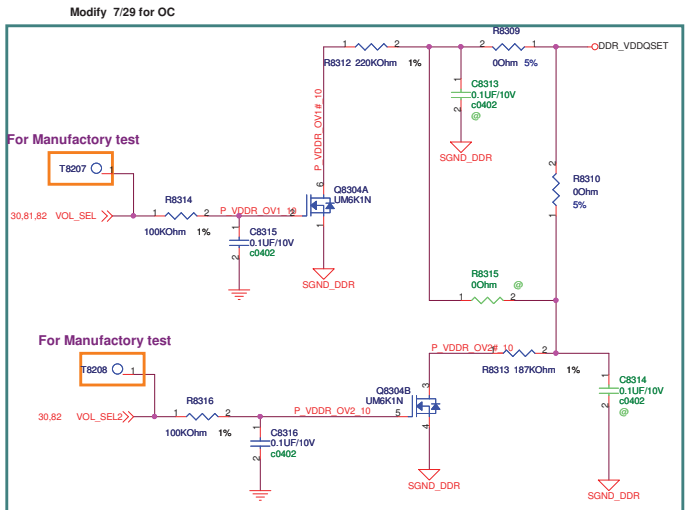
Attention Enable signal
EE Modify 0518

EE Modify 0521 : Change to 100K

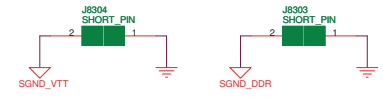
EE Modify 0518
DDR_PWRGD

OCP

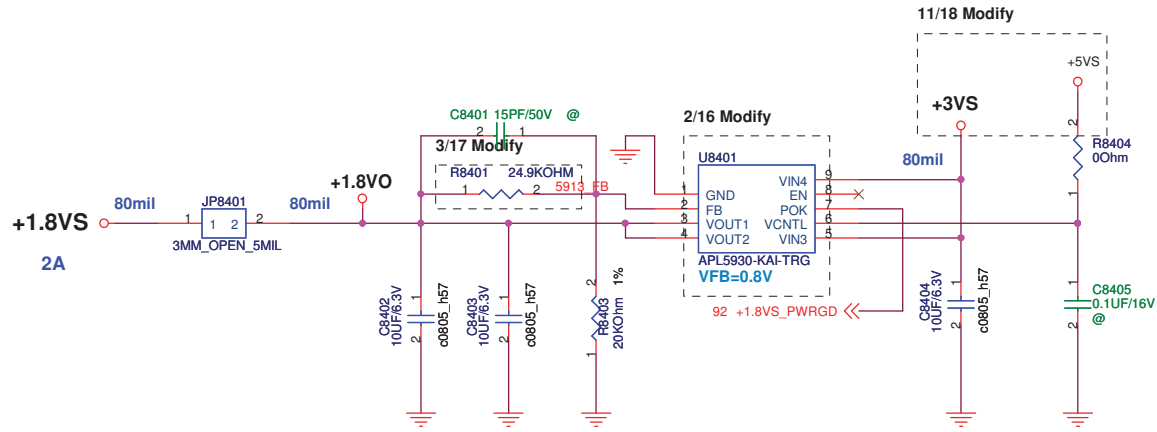
4/14 EE Modify: Add for DDR3 SM_PWROK



VOL_SEL2	VOL_SEL	Voltage
L	L	1.43V
L	H	1.5V
H	L	N/A(1.512V)
H	H	1.58V



+1.8VS



T8401	TPC28T
+1.8VO	1
T8402	TPC28T
+1.8VS	1
T8403	TPC28T
GND	1
T8404	TPC28T
GND	1

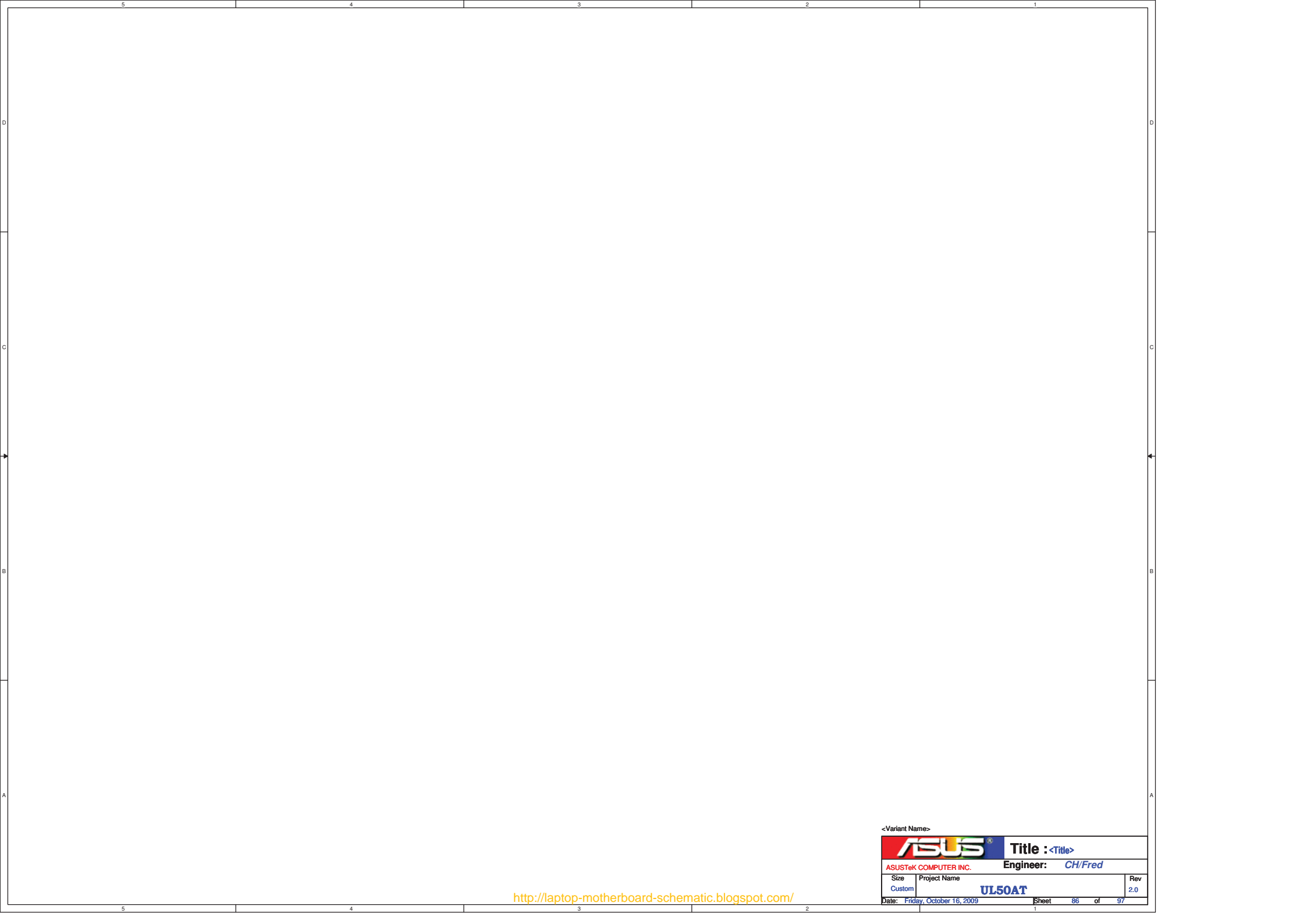
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		Title : POWER_IO_+1.8VS	
ASUSTeK COMPUTER INC.		Engineer: CH/Fred	
Size	Project Name	Rev	
Custom	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	84 of 97



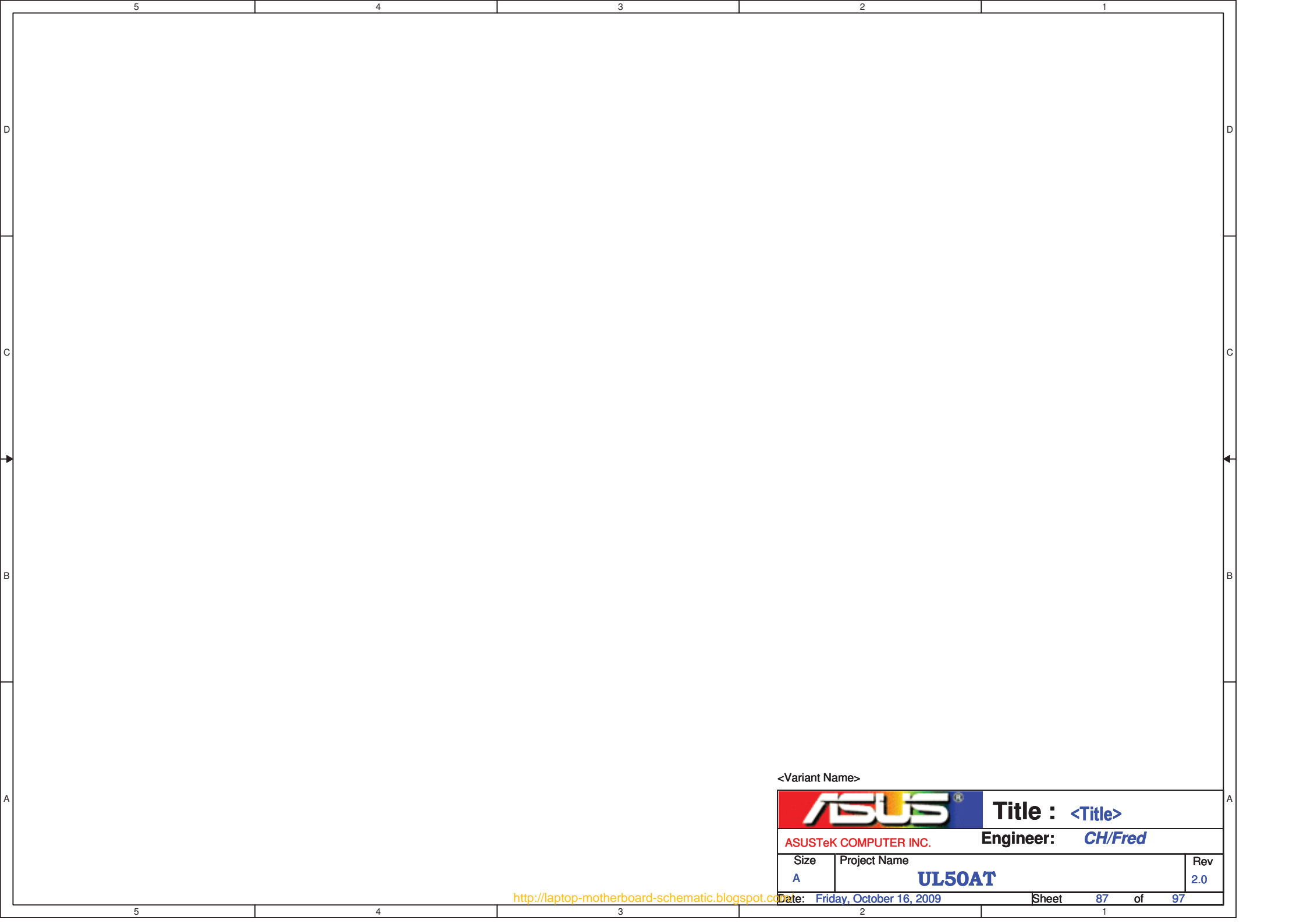
<Variant Name>

		Title : POWER_I/O_VGA
ASUSTeK COMPUTER INC.		Engineer: CH/Fred
Size	Project Name	Rev
B	UL50AT	2.0
Date: Friday, October 16, 2009	Sheet 85	of 97




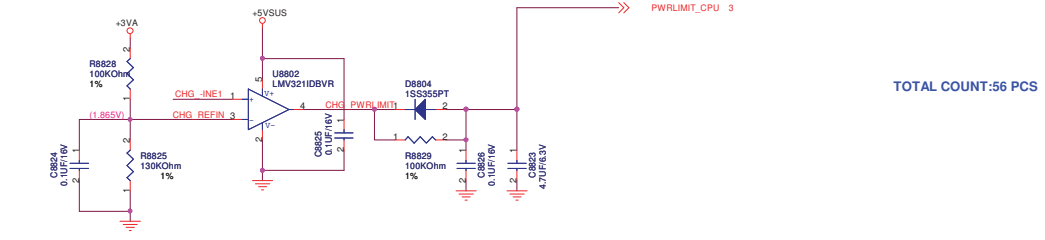
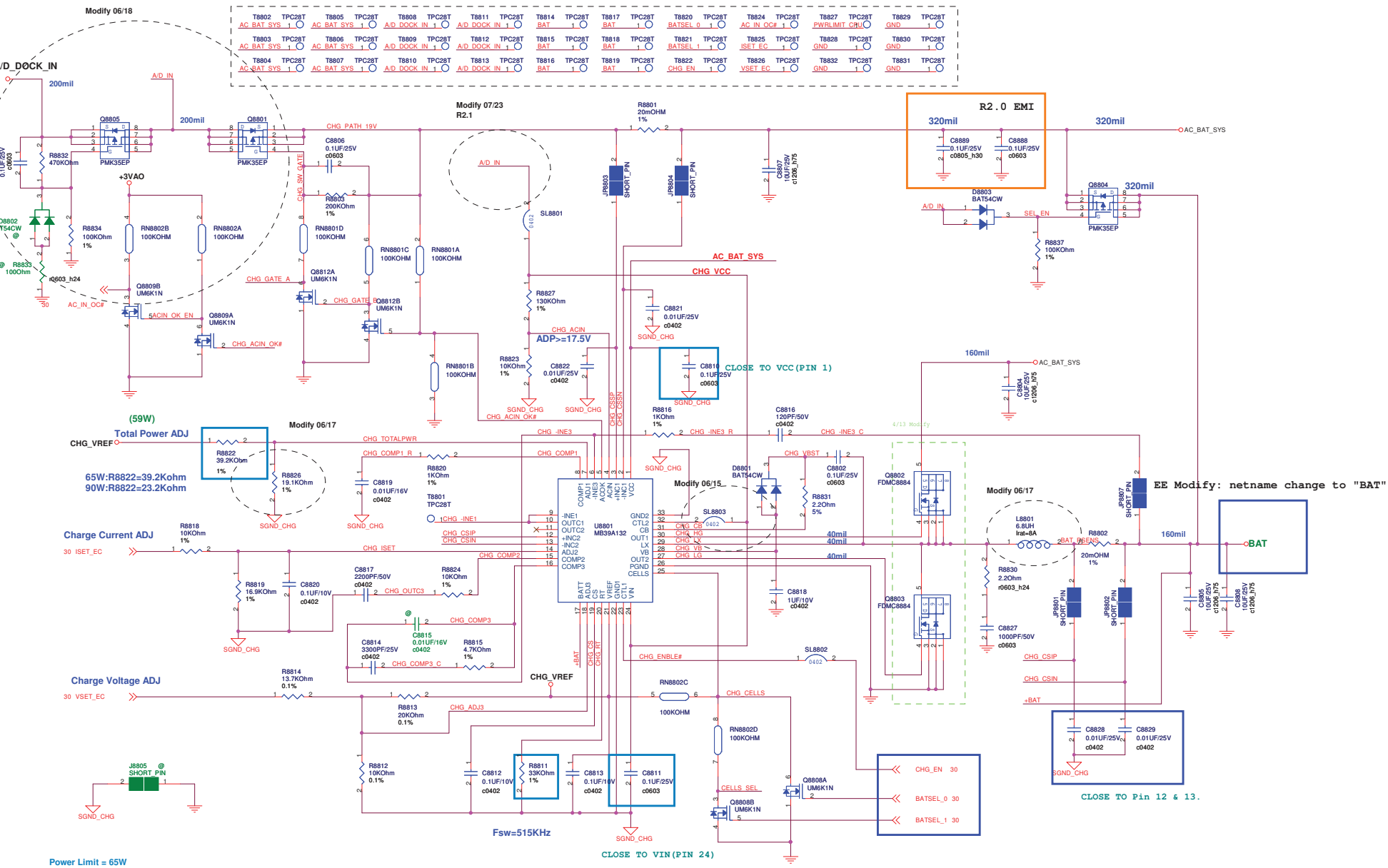
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		Title : <Title>	
ASUSTeK COMPUTER INC.		Engineer: CH/Fred	
Size Custom	Project Name UL50AT	Rev 2.0	
Date: Friday, October 16, 2009	Sheet	86	of 97



<Variant Name>

		Title : <Title>
ASUSTeK COMPUTER INC.		Engineer: CH/Fred
Size A	Project Name UL50AT	Rev 2.0
Date: Friday, October 16, 2009		Sheet 87 of 97



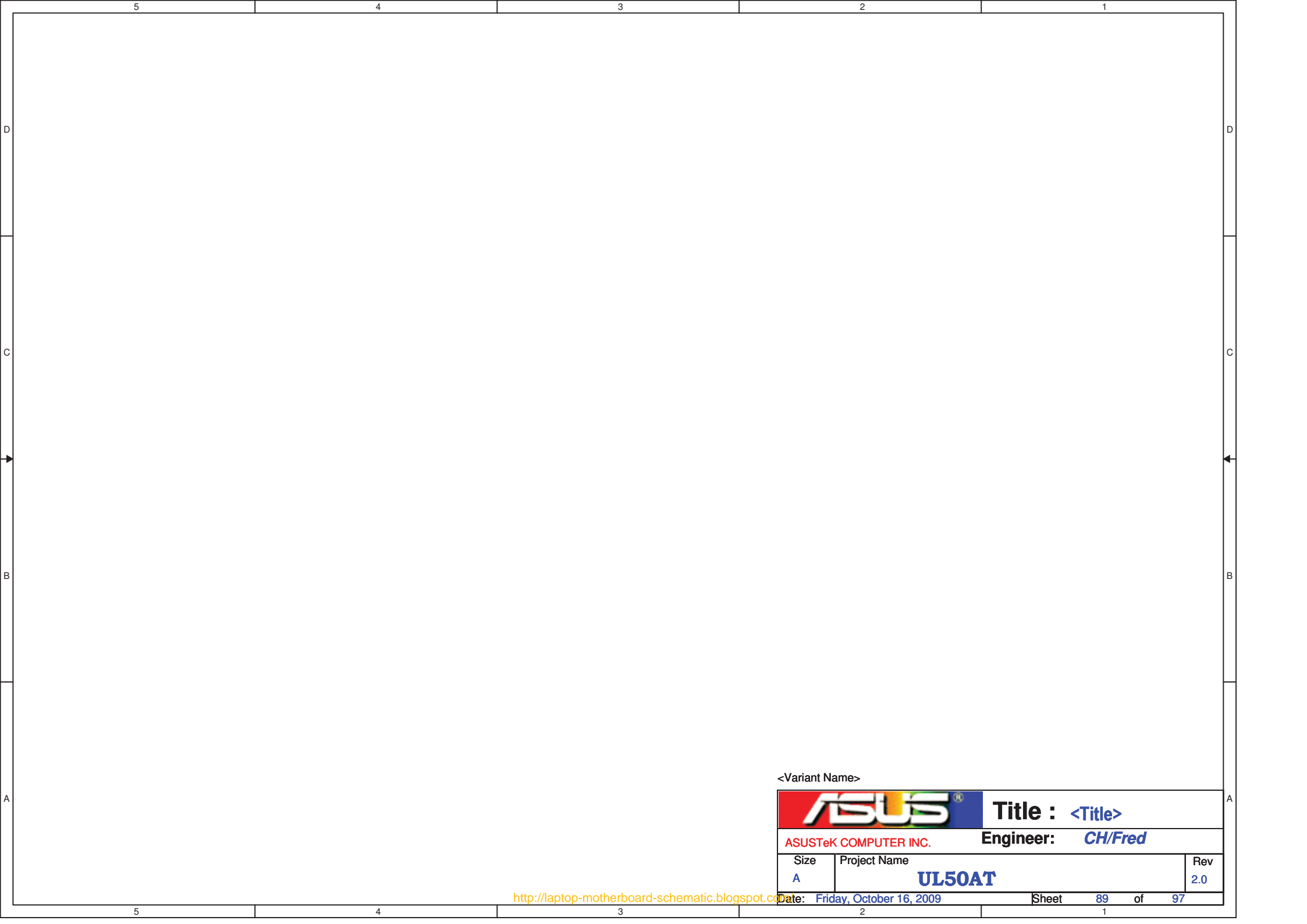
Battery Cells

BATSEL_1	BATSEL_0	CELLS
H	H	2 CELLS
L	H	2 CELLS
H	L	3 CELLS
L	L	4 CELLS


TOTAL COUNT:56 PCS

Charger IC and EC Code correlation sheet :
 Charger MAX8725 => EC CODE : 200
 Charger MAX17015 => EC CODE : 201
 Charger MB39A132 => EC CODE : 202

ASUS
 ASUSTek COMPUTER INC. **Engineer: CH/Fred**
 Project Name: **UL50AT**
 Date: Friday, October 16, 2009 Sheet 88 of 97



<Variant Name>

		Title : <Title>
ASUSTeK COMPUTER INC.		Engineer: CH/Fred
Size A	Project Name UL50AT	Rev 2.0
Date: Friday, October 16, 2009		Sheet 89 of 97

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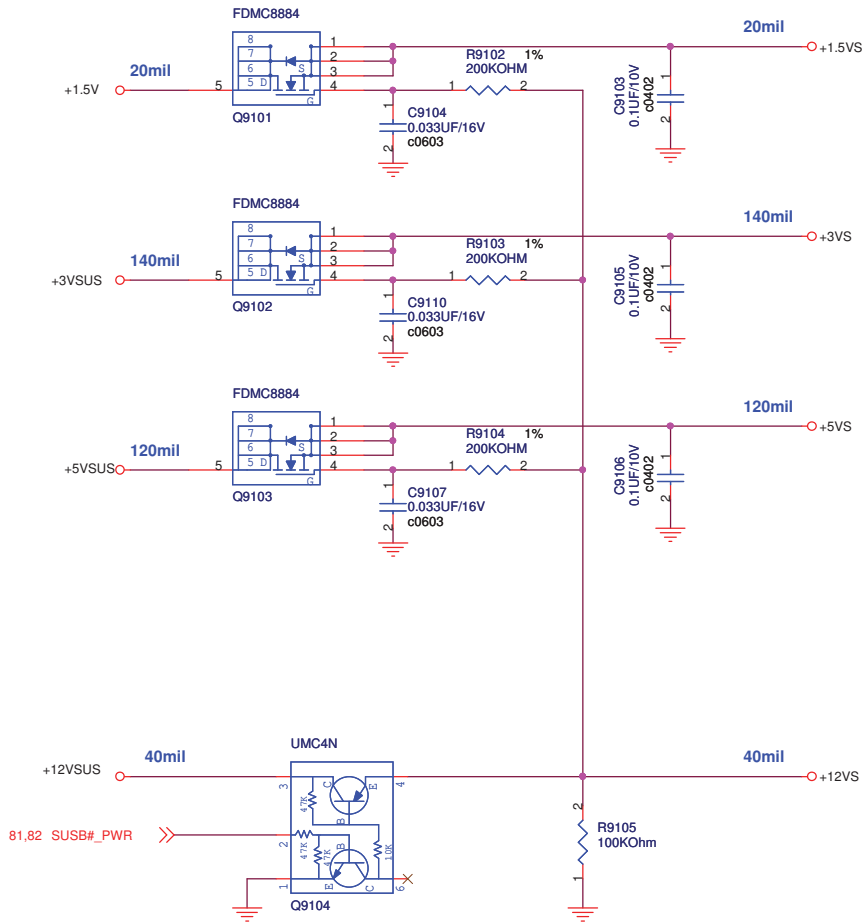
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A

<Variant Name>

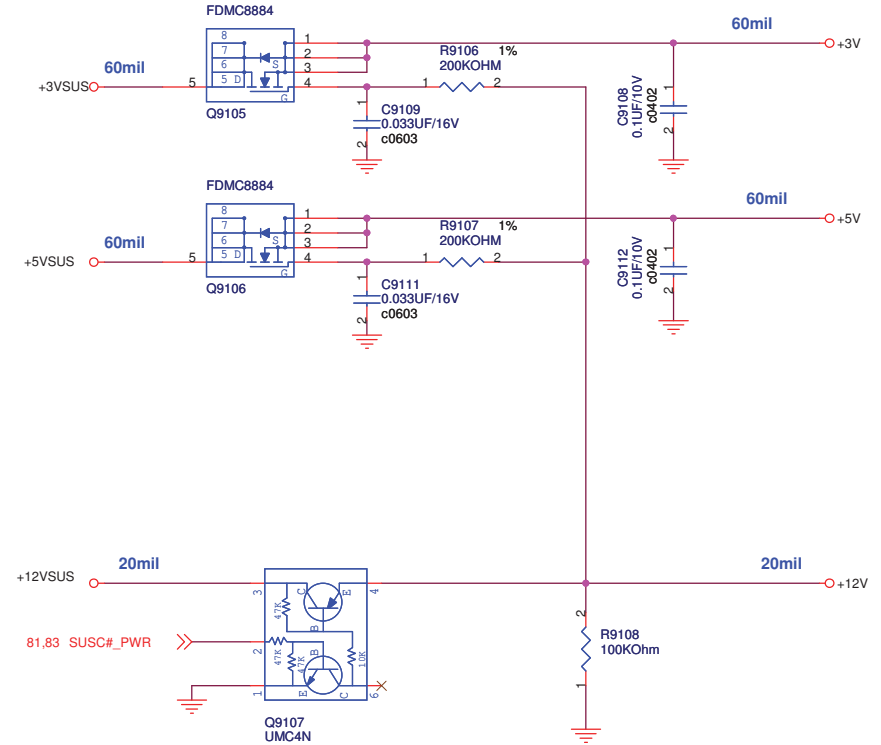
		Title : POWER_DETECT	
ASUSTeK COMPUTER INC.		Engineer: CH/Fred	
Size	Project Name	Rev	
Custom	UL50AT	2.0	
Date: Friday, October 16, 2009	Sheet	90	of 97

SUSB#_PWR POWER



Total count: 19 pcs

SUSC#_PWR POWER

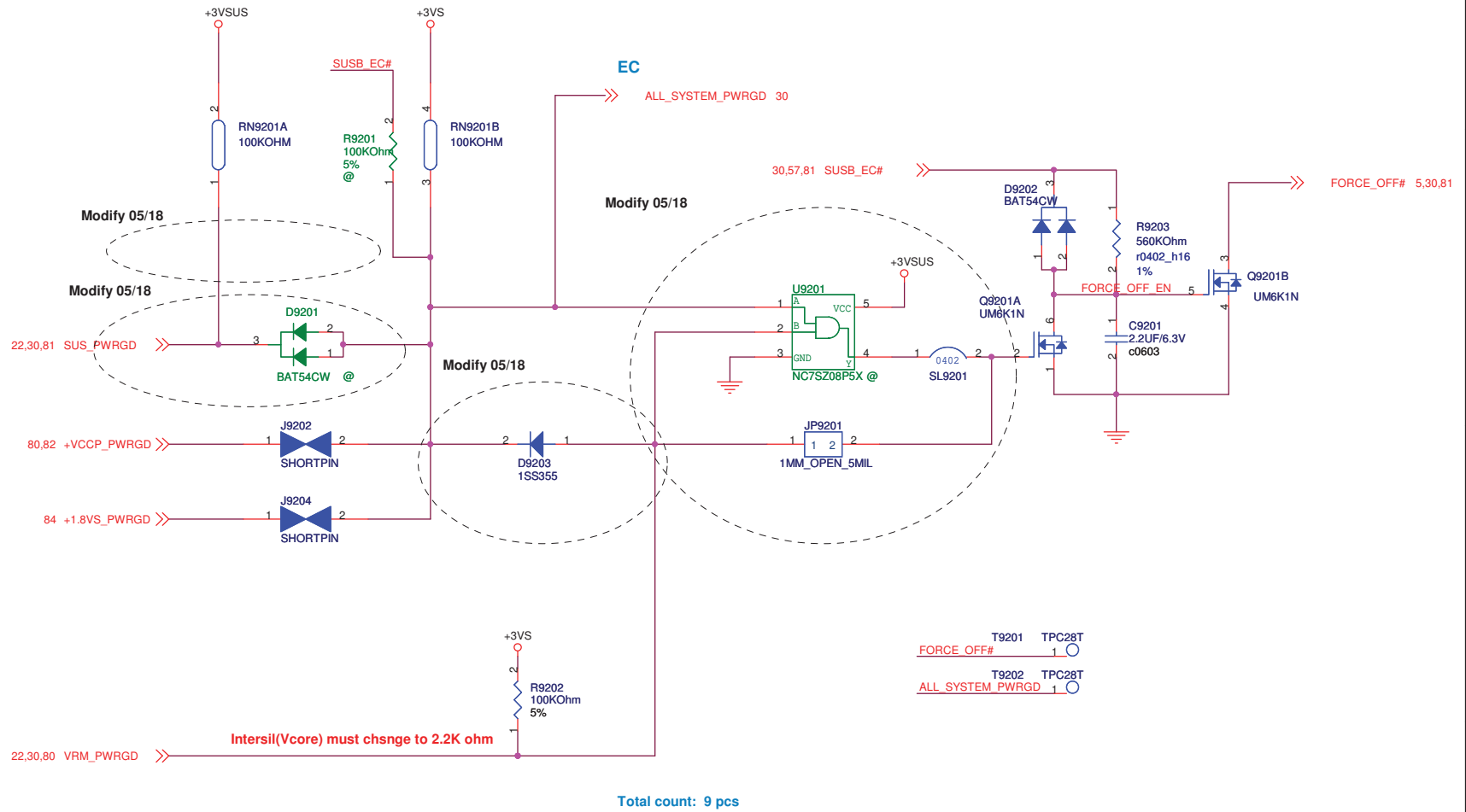


T9101	TPC28T	T9111	TPC28T
+12VSUS	1	+3VSUS	1
T9102	TPC28T	T9113	TPC28T
+12VS	1	+3VS	1
T9103	TPC28T	T9115	TPC28T
+12V	1	+3V	1
T9104	TPC28T	T9120	TPC28T
+5VSUS	1	+1.5V	1
T9106	TPC28T	T9121	TPC28T
+5V	1	+1.5VS	1
T9110	TPC28T	T9123	TPC28T
+5V	1	SUSB#_PWR1	1
		T9114	TPC28T
		SUSC#_PWR1	1

<Variant Name>

ASUS		Title :POWER_LOAD SWITCH	
ASUSTeK COMPUTER INC.		Engineer: CH/Fred	
Size B	Project Name UL50AT	Rev 2.0	
Date: Friday, October 16, 2009	Sheet 91	of 97	

POWER GOOD DETECTOR



<Variant Name>		ASUS		Title :POWER_PROTECT	
ASUSTeK COMPUTER INC.		Engineer:		CH/Fred	
Size	Project Name			Rev	
B	UL50AT			2.0	
Date: Friday, October 16, 2009		Sheet		92	of 97

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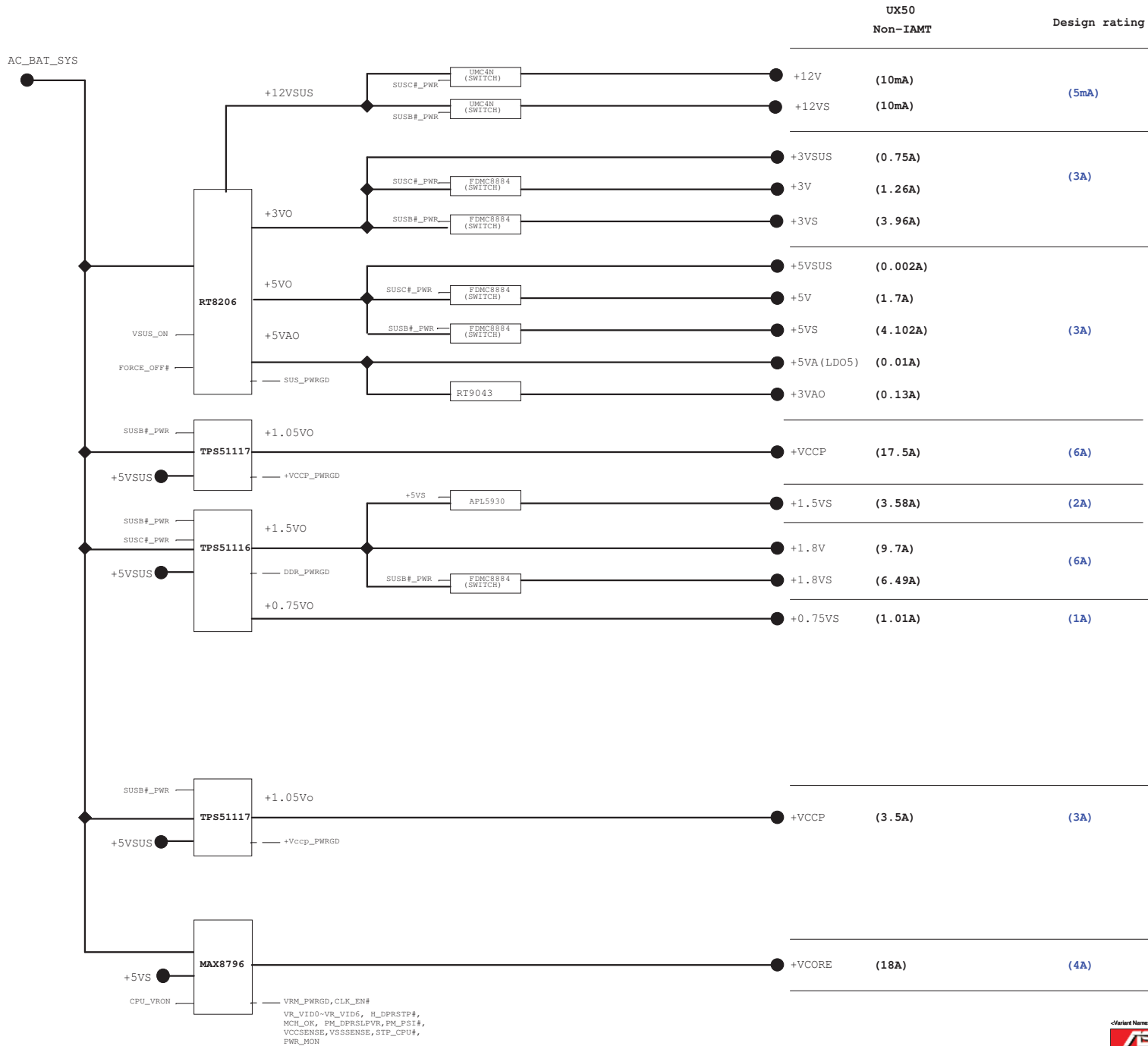
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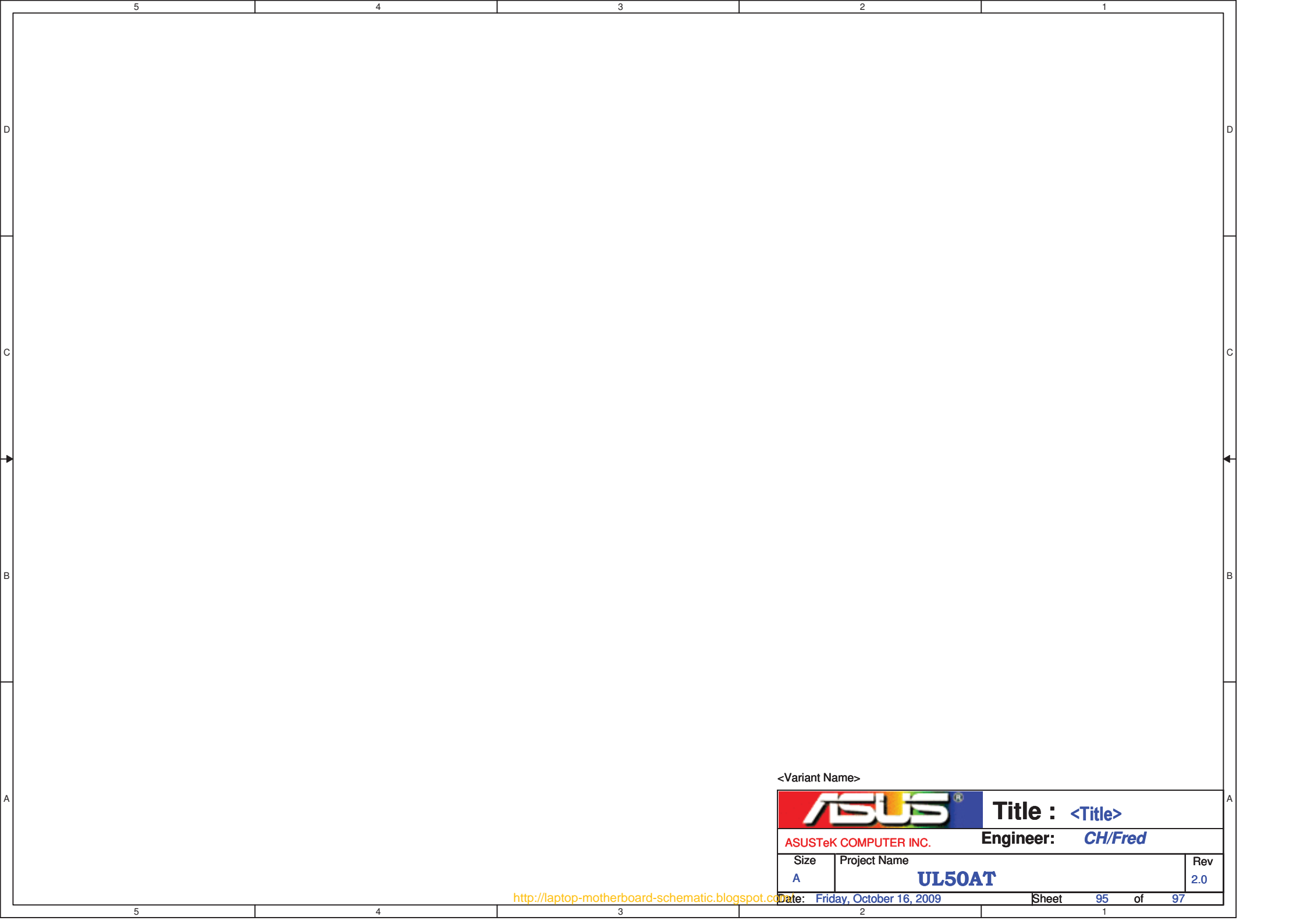
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<Variant Name>

		Title : POWER_SIGNAL	
ASUSTeK COMPUTER INC.		Engineer: CH/Fred	
Size	Project Name	Rev	
Custom	UL50AT	2.0	
Date: Friday, October 16, 2009	Sheet	93	of 97



<http://laptop-motherboard-schematic.blogspot.com/>




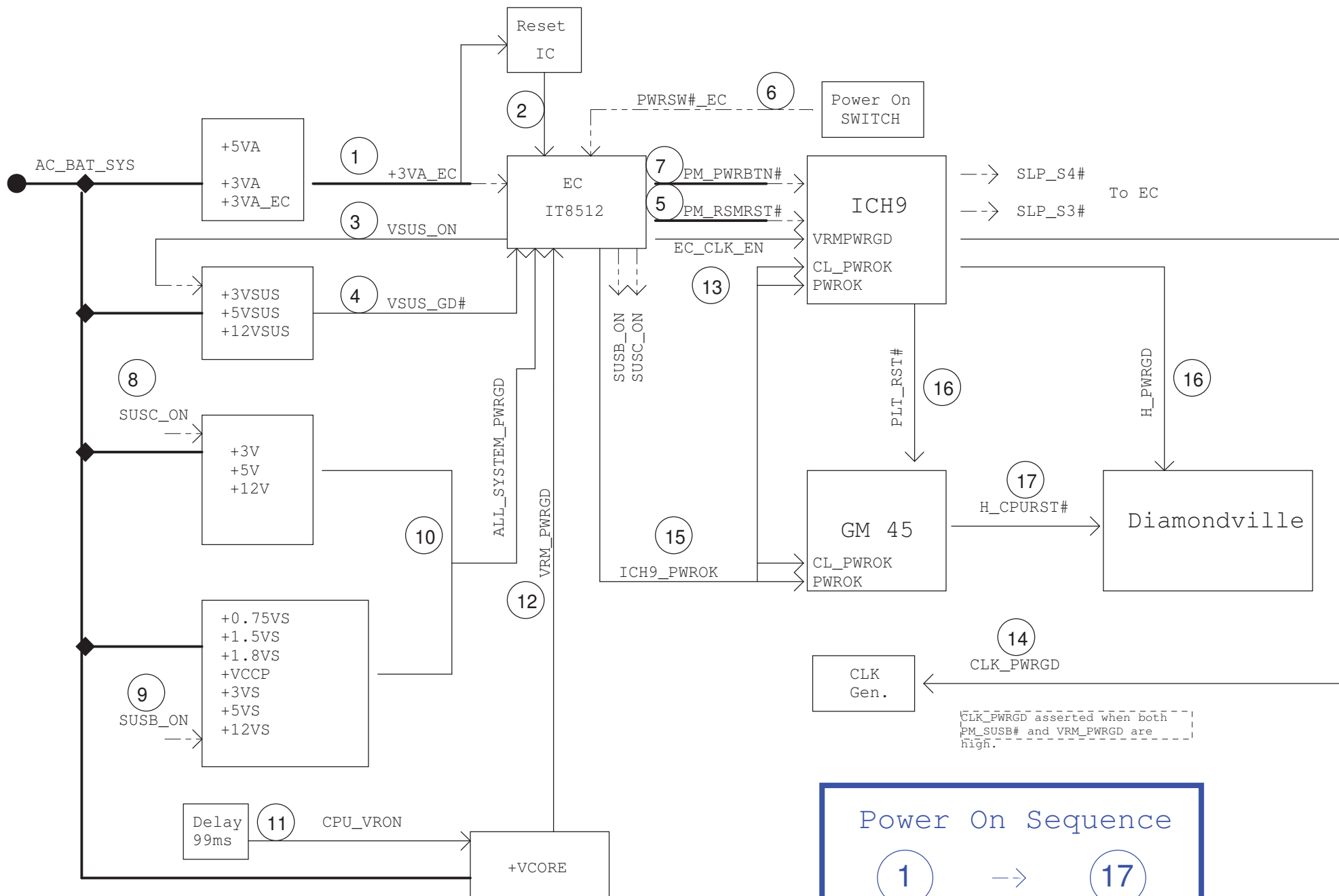
<Variant Name>

		Title : <Title>
ASUSTeK COMPUTER INC.		Engineer: CH/Fred
Size A	Project Name UL50AT	Rev 2.0
Date: Friday, October 16, 2009		Sheet 95 of 97

Rev	Date	Description
1.00		First Release!
1.10		
2.00		

<Variant Name>

		Title : HISTORY
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu
Size Custom	Project Name UL50AT	Rev 2.0
Date: Friday, October 16, 2009	Sheet 96 of 97	



<Variant Name>

ASUS		Title : POWER SEQUENCE	
ASUSTeK COMPUTER INC.		Engineer: Eric_Ho	
Size	Project Name	UL50AT	Rev
Custom			2.0
Date: Friday, October 16, 2009	Sheet	97	of 97