

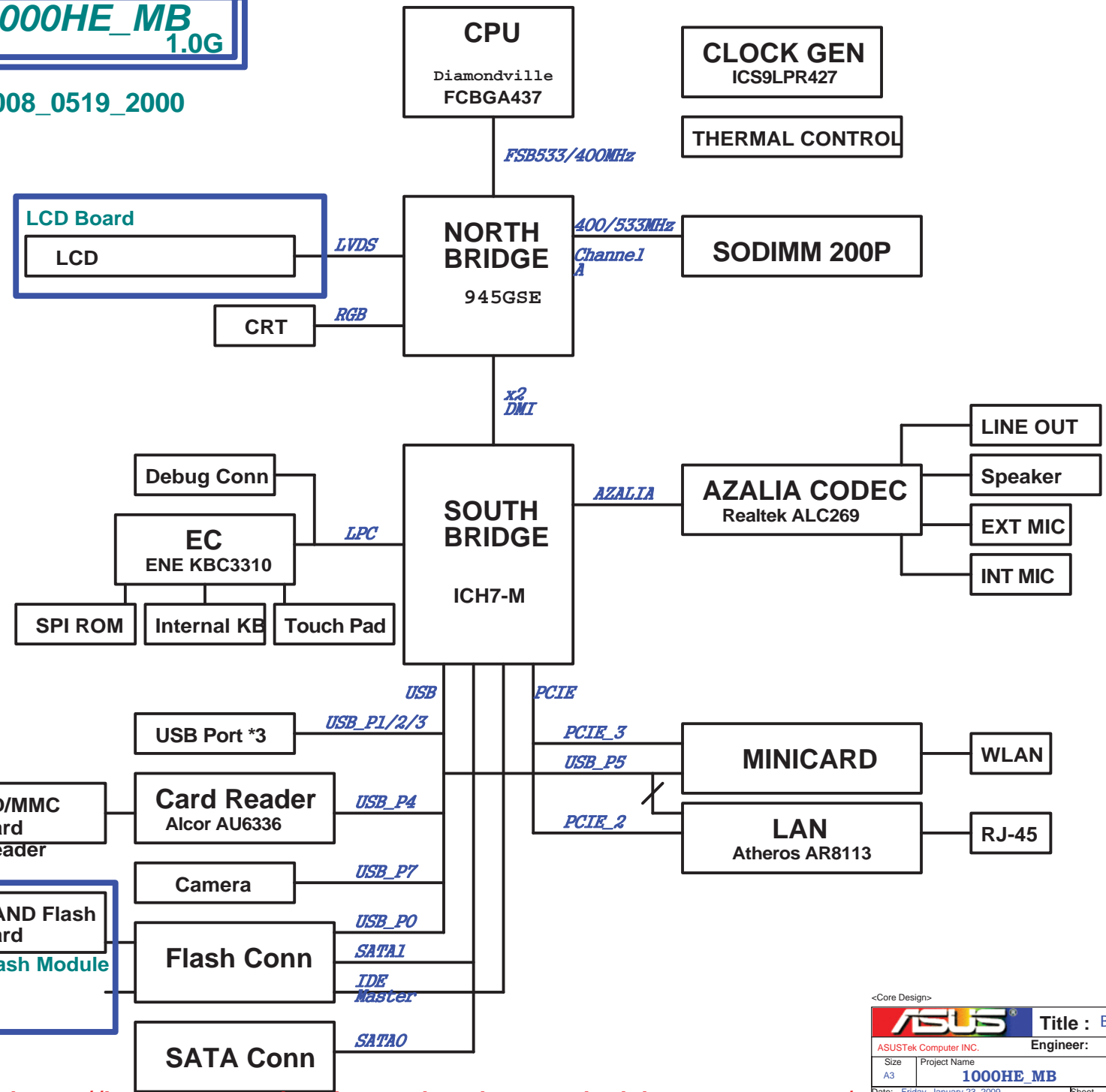
- 01_Block Diagram
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- 03_Power Sequence
- 04_Clock Gen_ICS9LPR426
- 05_Diamondville_BUS
- 06_Diamondville_PWR
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- 09_NB-945GMS(GRAPHIC)
- 10_NB-945GMS(DDR2)
- 11_NB-945GMS(PWR)
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- 24_LAN_Atheros AR8113
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- 28_USB Port
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- 30_Card Reader_AU6336C52
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- 34_EC_UART controller
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1000HE_MB
1.0G

2008_0519_2000

LCD Board
LCD

NAND Flash Card
Flash Module




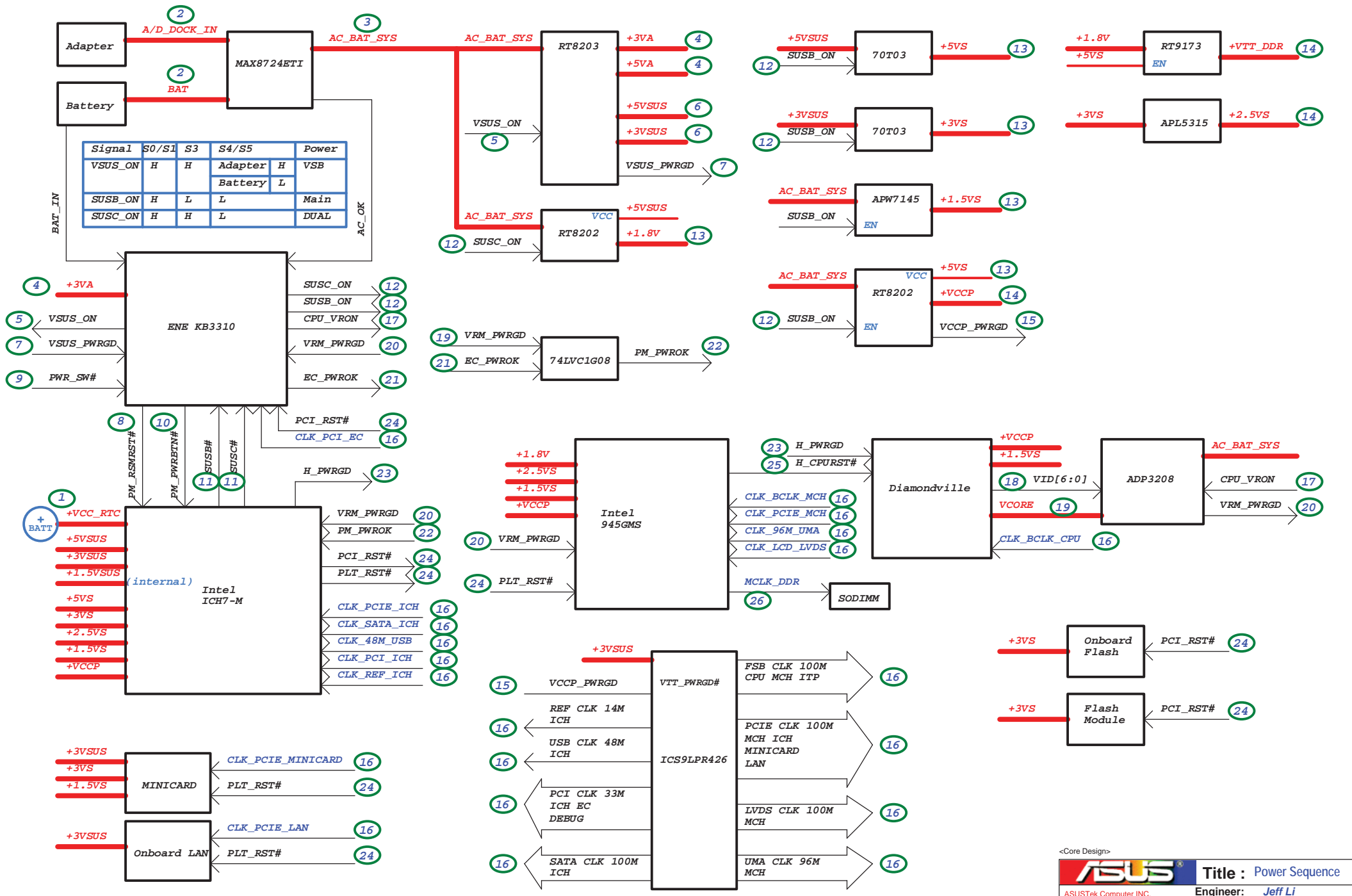
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ASUS		Title : Block Diagram	
ASUSTek Computer INC.		Engineer: Echo_Huang	
Size	Project Name	Rev	
A3	1000HE_MB	1.1G	
Date: Friday, January 23, 2009	Sheet	1	of 47



<Core Design>

		Title : History	
ASUSTek Computer INC.		Engineer: KingCa_Jin	
Size	Project Name		Rev
A3	1000HE_MB		1.0G
Date: Friday, January 23, 2009		Sheet	2 of 47



Signal	S0/S1	S3	S4/S5	Power
VSUS_ON	H	H	Adapter	H
			Battery	L
SUSB_ON	H	L		Main
SUSC_ON	H	H		DUAL

EC KB3310 GPIO SETTING

Pin	Pin Name	Signal Name	Type	Note
1	GPIO00/GA20	A20GATE	O	
2	GPIO01/KBRST#	RC_IN#	O	
6	GPIO04	EMAIL_SW#	I	Internal pull high
13	GPIO05/PCIRST#	PCI_RST#	I	
14	GPIO07	BAT_OTP	I	Battery over temperature
15	GPIO08	EXTSMH#	OD	10K pull high to +3VSB
16	GPIO0A	LID_EC#	I	Internal pull high
17	GPIO0B/ESB_CLK	NC	O	
18	GPIO0C/ESB_DAT	NC	O	
19	GPIO0D	DISTP_SW#	I	Internal pull high
20	GPIO0E/SC#	EXT_SC#	O	10K pull high to +3VSB
21	GPIO0F/PWM0	BL_PWM_DA	O	
23	GPIO10/PWM1	BAT_CRITICAL	I	Battery critical capacity
25	GPIO11/PWM2	PM_PWRBTN#	OD	Internal pull high in ICH
26	GPIO12/FANPWM1	FAN0_PWM	O	CPU Fan
27	GPIO13/FANPWM2	FAN1_PWM	O	VGA Fan
28	GPIO14/FANFB1	FAN0_TACH	I	CPU FanTach
29	GPIO15/FANFB2	FAN1_TACH	I	VGA FanTach
30	GPIO16/E51_TX	E51_TX	O	RS232 debug port
31	GPIO17/E51_RX	E51_RX	I	RS232 debug port
32	GPIO18	PWR_SW#	I	Internal pull high
34	GPIO19/PWM3	MAIL_LED#	O	
36	GPIO1A/NUMLED	NUM_LED#	O	
38	GPIO1D/CLKRUN#	NC	O	
39	GPIO20/KSO0/TP_TEST	KSO0	O	
40	GPIO21/KSO1/TP_PLL	KSO1	O	
41	GPIO22/KSO2	KSO2	O	
42	GPIO23/KSO3	KSO3	O	
43	GPIO24/KSO4	KSO4	O	
44	GPIO25/KSO5	KSO5	O	
45	GPIO26/KSO6	KSO6	O	
46	GPIO27/KSO7	KSO7	O	
47	GPIO28/KSO8	KSO8	O	
48	GPIO29/KSO9	KSO9	O	
49	GPIO2A/KSO10	KSO10	O	
50	GPIO2B/KSO11	KSO11	O	
51	GPIO2C/KSO12	KSO12	O	
52	GPIO2D/KSO13	KSO13	O	
53	GPIO2E/KSO14	KSO14	O	
54	GPIO2F/KSO15	KSO15	O	
55	GPIO30/KSI0	KSI0	I	Internal pull high
56	GPIO31/KSI1	KSI1	I	Internal pull high
57	GPIO32/KSI2	KSI2	I	Internal pull high
58	GPIO33/KSI3	KSI3	I	Internal pull high
59	GPIO34/KSI4	KSI4	I	Internal pull high
60	GPIO35/KSI5	KSI5	I	Internal pull high
61	GPIO36/KSI6	KSI6	I	Internal pull high
62	GPIO37/KSI7	KSI7	I	Internal pull high
63	GPI38/AD0	BAT_ICHG	I	
64	GPI39/AD1	BAT_CONFIG	I	Battery configuration
65	GPIO3A/AD2	BAT_SENSE	I	Battery Voltage Sensor
66	GPIO3B/AD3	BAT_TS	I	Battery Thermal Sensor
68	GPO3C/DA0	DOC	O	Trigger Clock Gen

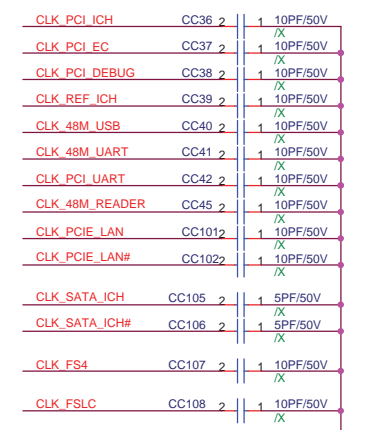
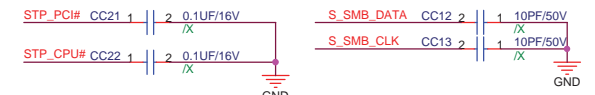
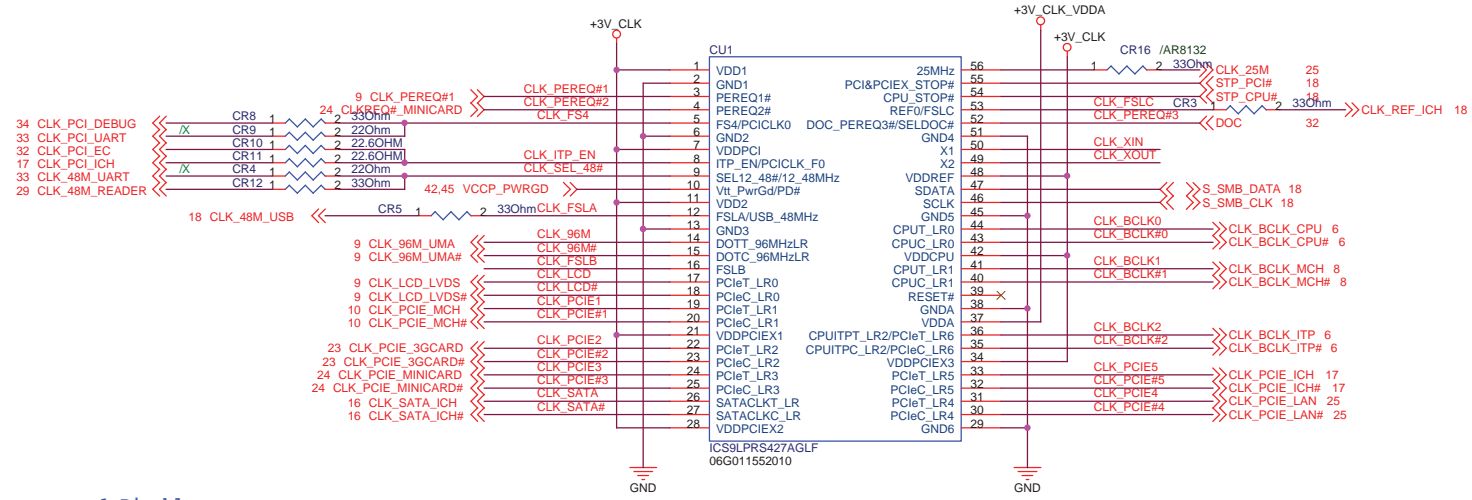
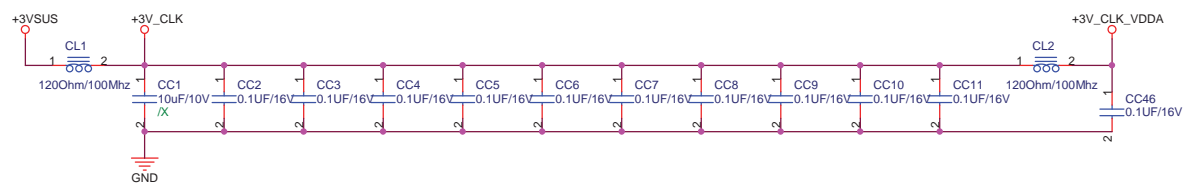
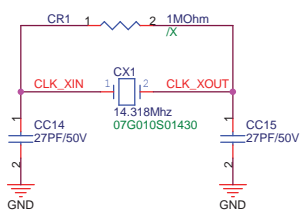
EC KB3310 Other Pin SETTING

Pin	Pin Name	Signal Name	Type	Note
3	SERIRQ	INT_SERIRQ	I/O	10K pull high to +3V
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA_EC	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCI_EC	I	
22	VCC	+3VA_EC	P	
24	GND	GND	P	
33	VCC	+3VA_EC	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	100K pull high to +3VA_EC
67	AVCC	+3VACC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA_EC	P	
111	VCC	+3VA_EC	P	
113	GND	GND	P	
119	RD#/SPIDI	SPL_SO	I	
120	WR#/SPIDO	SPL_SI	O	
112	XCLKI	32KXCLKI	I	
123	XCLKO	32KXCLKO	O	
124	V18R	V18R	P	Reserved 1uF to GND
125	VCC	+3VA_EC	P	
128	SPICS#/SELMEM#	SPL_CE#	O	

Pin	Pin Name	Signal Name	Type	Note
70	GPO3D/DA1	LCD_BACKOFF#	O	
71	GPO3E/DA2	CLK_PWRSERVE#	O	
72	GPO3F/DA3	BAT_LL#	O	Battery Low Low
73	GPIO40	AC_OK	I	AC Adaptor Plug in
74	GPIO41	PM_RSMRST#	O	10K pull down to GND
75	GPI42	BAT_IN	I	
76	GPI43	CLRTC_EC	I	
77	GPIO44/SCL1	SMB0_CLK	I/O	4.7K pull high to +3VA_EC
78	GPIO45/SDA1	SMB0_DAT	I/O	4.7K pull high to +3VA_EC
79	GPIO46/SCL2	SMB1_CLK	I/O	10K pull high to +3V
80	GPIO47/SDA2	SMB1_DAT	I/O	10K pull high to +3V
81	GPIO48/KSO16	KB pin 28	I	for KB type detection
82	GPIO49/KSO17	KB pin 27	I	for KB type detection
83	GPIO4A/PSCLK1	AUO_SCL	O	for AUO, default H at S0
84	GPIO4B/PSDAT1	AUO_SDA	O	for AUO, default L at S0
85	GPIO4C/PSCLK2	AUO_CSB	O	for AUO, default H at S0
86	GPIO4D/PSDAT2	LVDD_EN	I	for AUO 7" Panel
87	GPIO4E/PSCLK3	TP_CLK	I/O	10K pull high to +3V
88	GPIO4F/PSDAT3	TP_DAT	I/O	10K pull high to +3V
89	GPIO50/SELIO#	BATSEL_3S	O	Battery series, H:3S, L:4S
90	GPIO52/E51_CS#	CHG_LED_UP#	O	
91	GPIO53/CAPLED	CAP_LED#	O	
92	GPIO54	PWR_LED_UP	O	
93	GPIO55/SCRLED	SCR_LED#	O	
95	GPIO56	PWR4G_SW#	I	Internal pull high
97	GPXOA00/SDICS#	SPI_MODE#	O	4.7K pull down to GND
98	GPXOA01/SDICLK	SUSC_ON	O	
99	GPXOA02/SDIDO	VSUS_ON	O	
100	GPXOA03	CPU_VRON	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	ICH_PWROK	O	
103	GPXOA06	VOLT_CTRL	O	
104	GPXOA07	CHG_EN#	O	Battery charging enabled
105	GPXOA08	PRECHG	O	
106	GPXOA09	SPI_WP#	O	
107	GPXOA10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	
109	GPXID0/SDIDI	BATSEL_2P#	O	Battery parallel, H:1P, L:2P-3P
110	GPXID1	NC	O	
112	GPXID2	THRO_CPU	O	Active if CPU temperature over spec
114	GPXID3	SUSB#	I	100K pull down to GND
115	GPXID4	SUSC#	I	100K pull down to GND
116	GPXID5	CPUPWR_GD	I	Pull high to +3V
117	GPXID6	VSUS_GD	I	
118	GPXID7	NC	O	
121	GPIO57	INTERNET#	I	Internal pull high
126	GPIO57/SPICLK	SPI_CLK	O	
127	GPIO59/TEST_CLK	NC	O	

<Core Design>

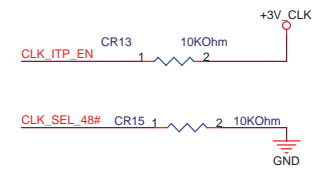
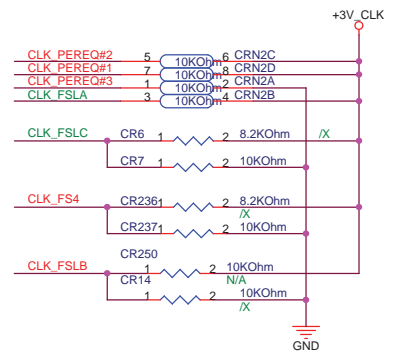
		Title : EC Pin Define	
ASUSTek Computer INC.		Engineer: Jeff Li	
Size	Project Name	Rev	
A3	1000HO_MB	1.0G	
Date: Friday, January 23, 2009	Sheet	4	of 47



1:Disable
0:Enable

PEREQ1:PCIEx0 & PCIEx1
PEREQ2:PCIEx2 & PCIEx3 & SATA
PEREQ3:PCIEx4 & PCIEx5 & PCIEx6

FSC	FSB	FSA	CPU	PCIE	SATA
0	1	1	166	100	100
0	0	1	133	100	100
1	0	1	100	100	100

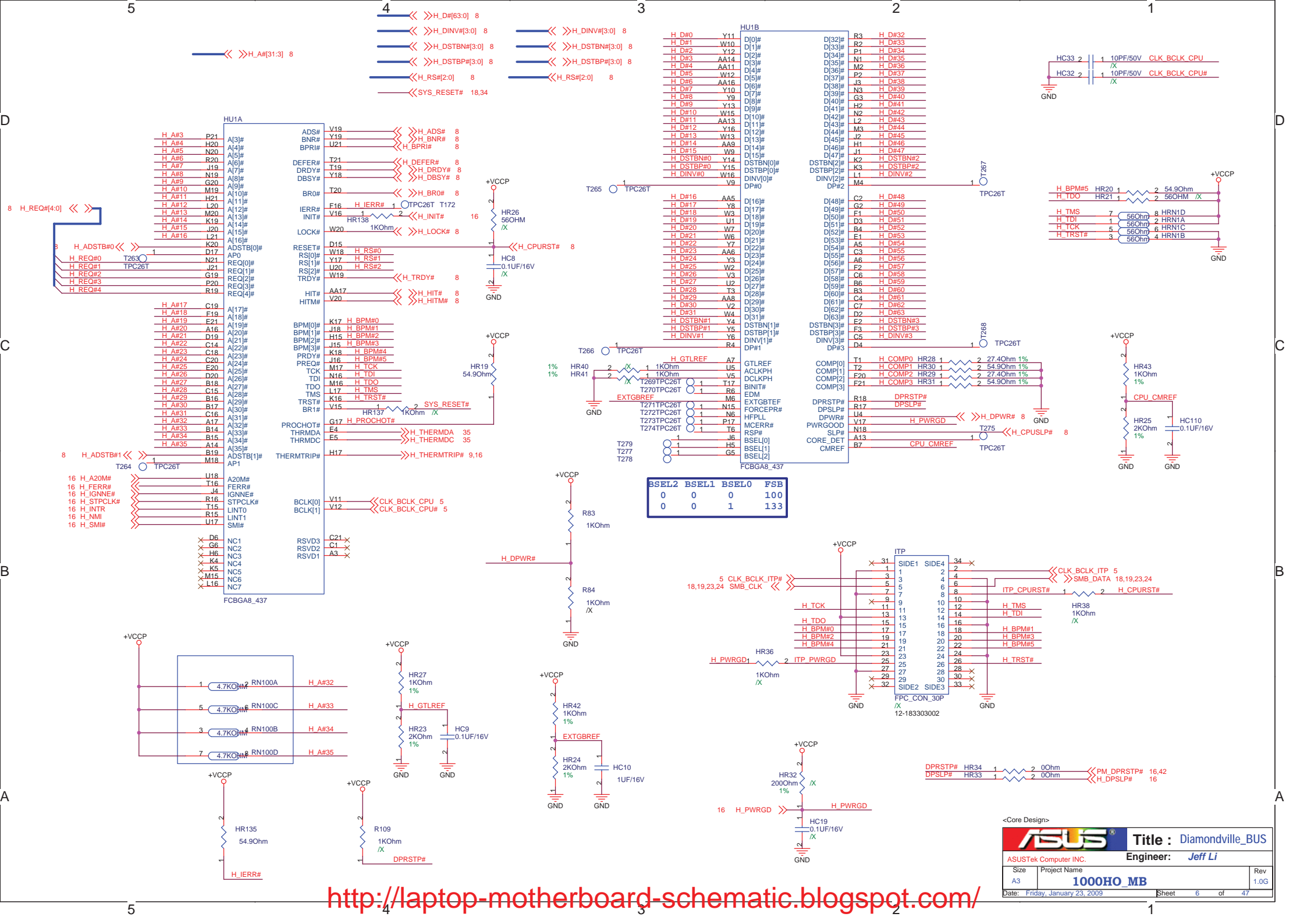


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ASUS Title : Clock Gen_ICS9LPRS427

ASUSTek Computer INC. Engineer: Jeff Li

Size	Project Name	Rev
A3	1000HO_MB	1.0G
Date: Friday, January 23, 2009	Sheet 5 of 47	



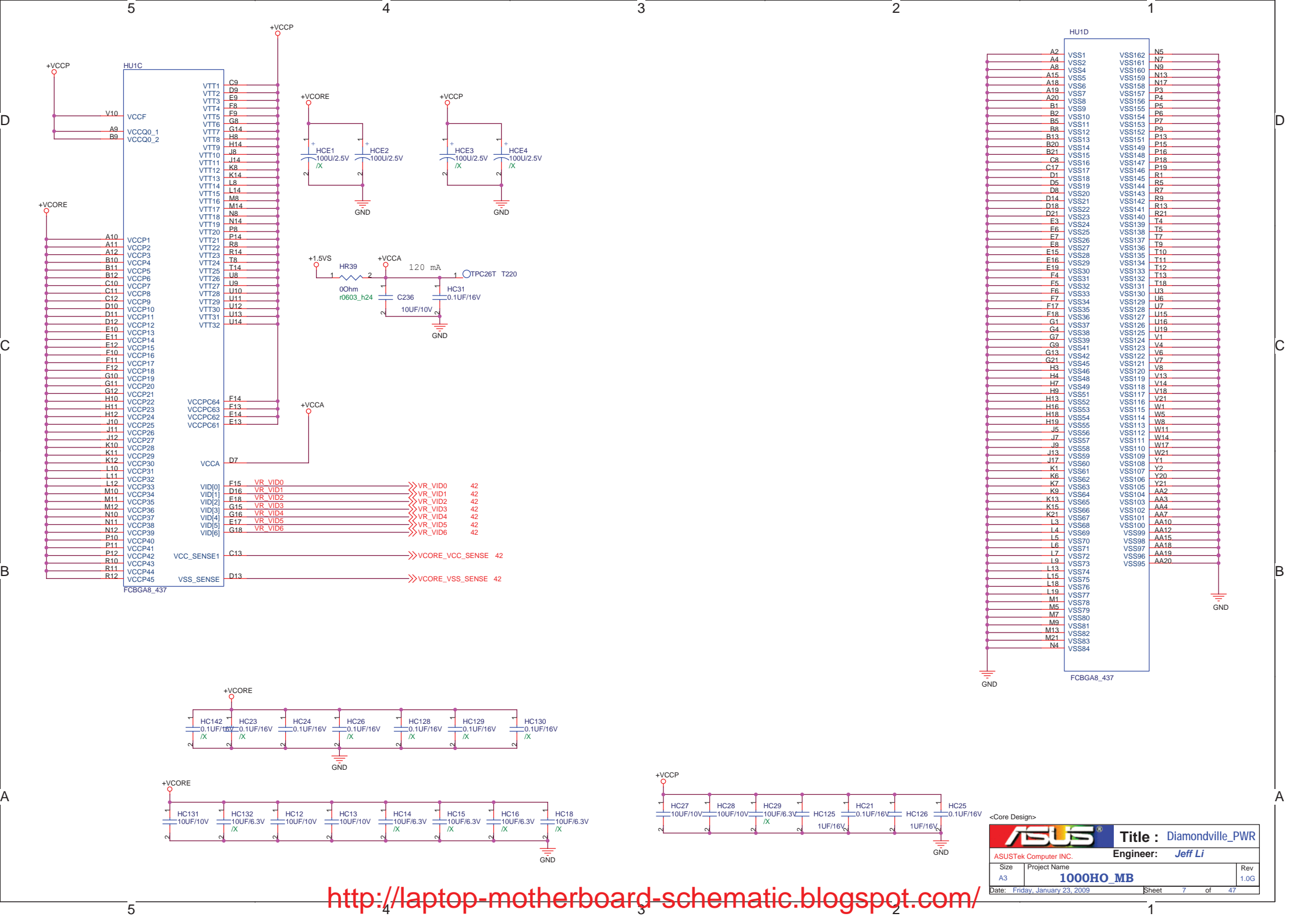
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ASUS Title : Diamondville_BUS

ASUSTek Computer INC. Engineer: Jeff Li

Size	Project Name	Rev
A3	1000HO_MB	1.0G

Date: Friday, January 23, 2009 Sheet 6 of 47



<Core Design>

ASUS Title : Diamondville_PWR

ASUSTek Computer INC. Engineer: Jeff Li

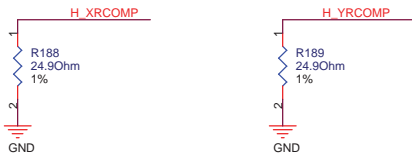
Size	Project Name	Rev
A3	1000HO_MB	1.0G

Date: Friday, January 23, 2009 Sheet 7 of 47

Power :
+VCCP

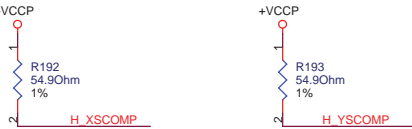
RCOMP

For Calibrating the FSB I/O Buffer



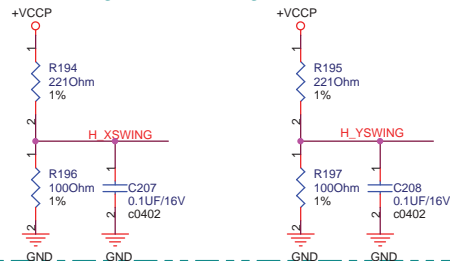
SCOMP

For Slow Rate Compensation on the FSB

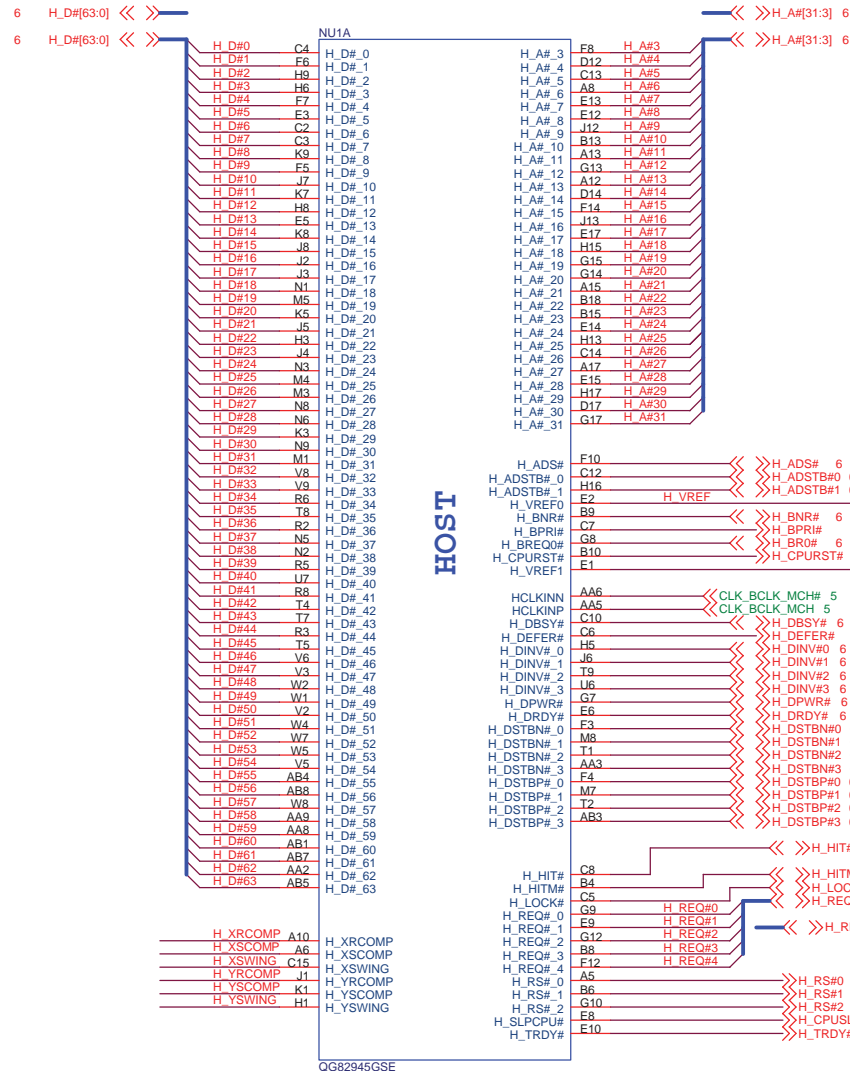


Voltage Swing

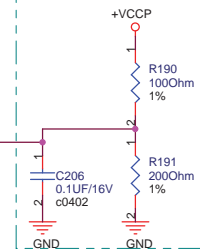
For Providing a Reference Voltage to The FSB RCOMP circuits



Signal voltage level =
0.3125*VCCP
Trace should be 10 mil wide
with 20 mil spacing



AGTL+ I/O Voltage Reference



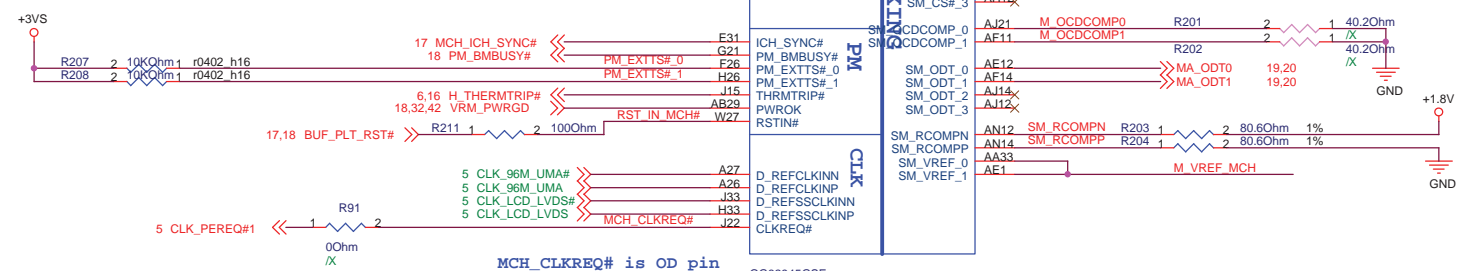
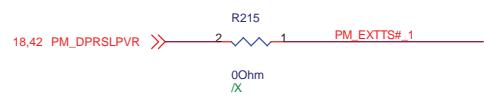
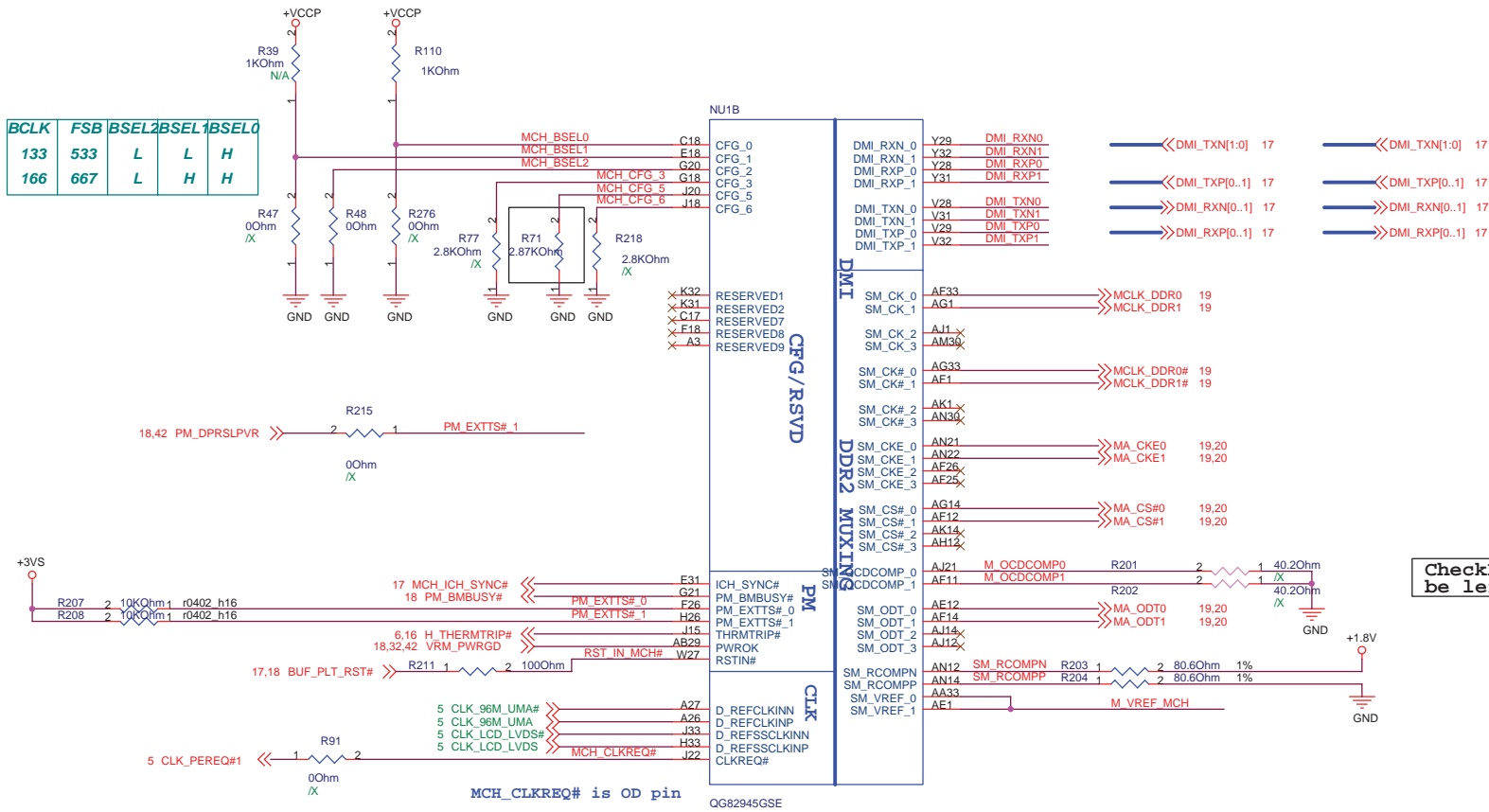
Layout Note:
0.1uF should be placed 100mils or less from GMCH pin.

QG82945GSE

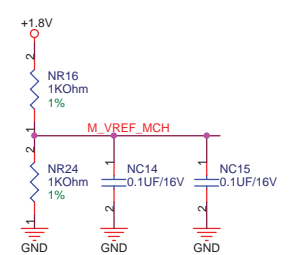
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ASUS		Title : NB-945GMS(HOST)	
ASUSTek COMPUTER INC.		Engineer: Jeff Li	
Size	Project Name	Rev	
A3	1000HO_MB		1.0G
Date:	Friday, January 23, 2009	Sheet	8 of 47

BCLK	FSB	BSEL0	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H



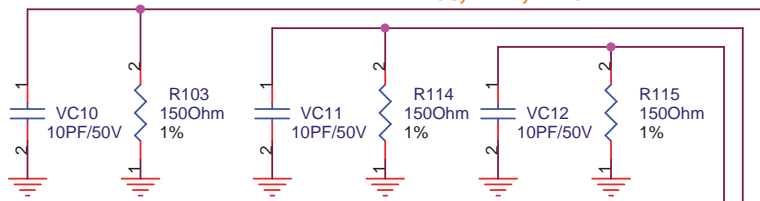
CheckList notes :Can be left as NC



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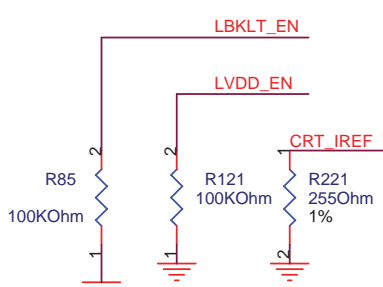
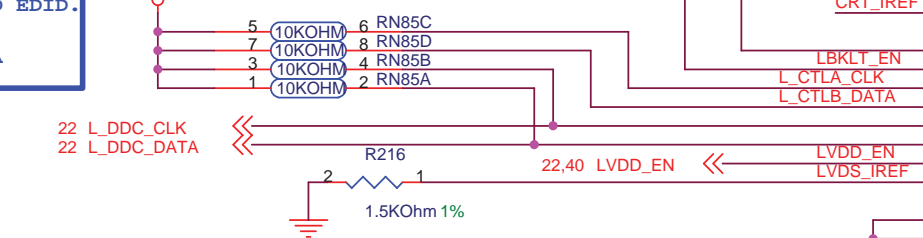
ASUS		Title : NB-945GMS(DMI & CFG)
ASUSTeK COMPUTER INC.		Engineer: Jeff Li
Size A3	Project Name 100HO_MB	Rev 1.0G
Date: Friday, January 23, 2009	Sheet	9 of 47

Close to GMCH
R103,R114,R115

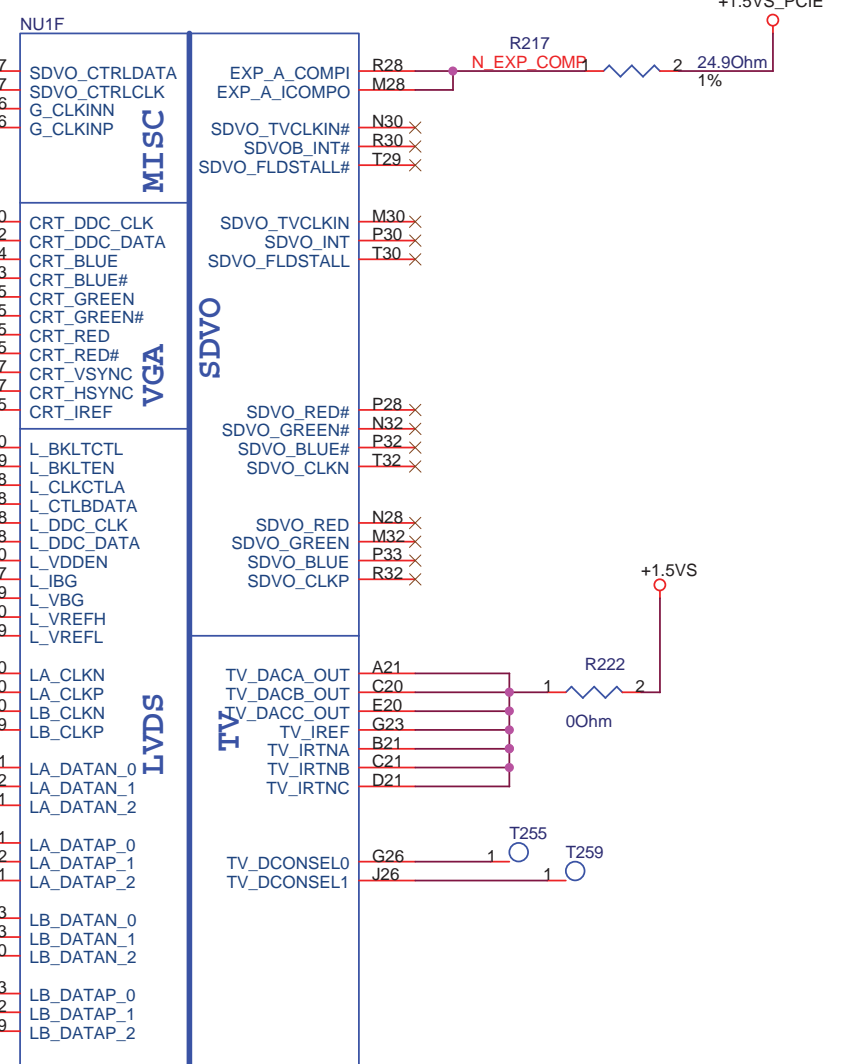


IF USE NB READ EDID.
MUST CONNECT
L_DDC_CLK&DATA

+3VS



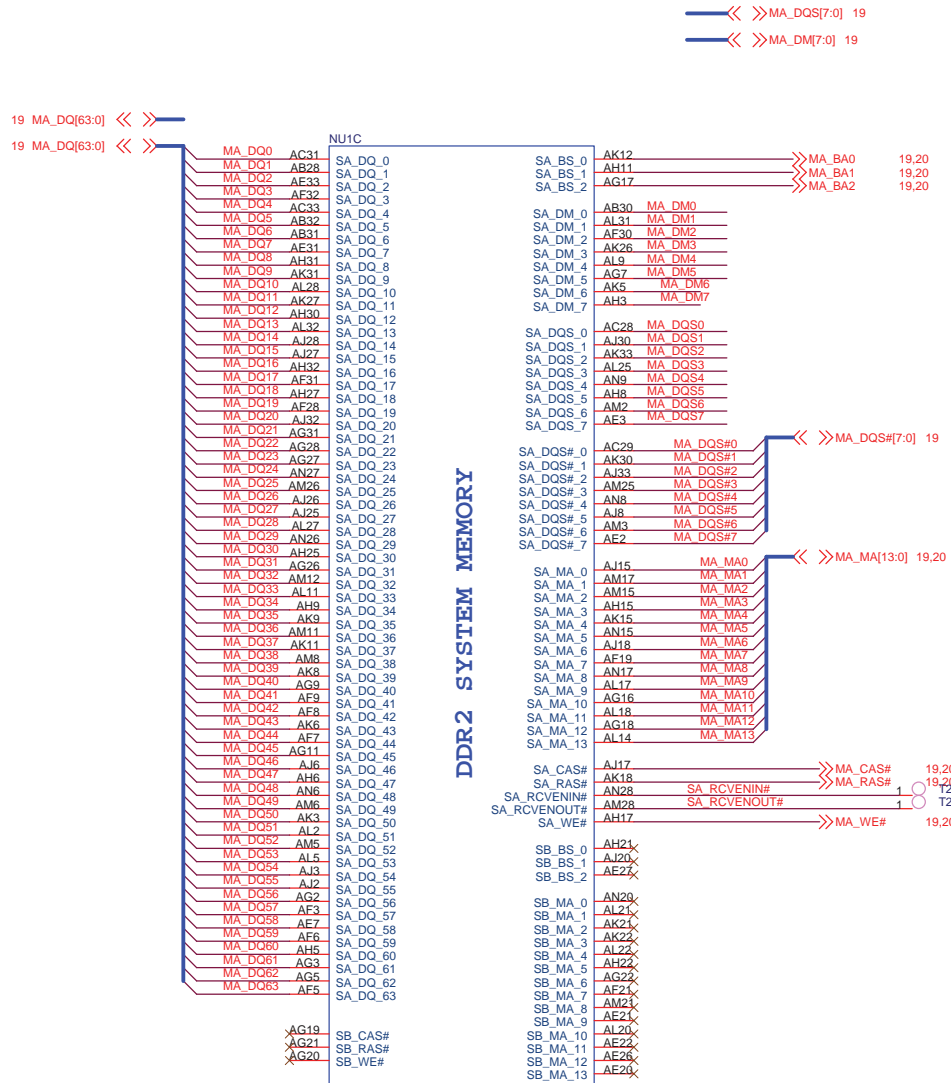
Close to GMCH



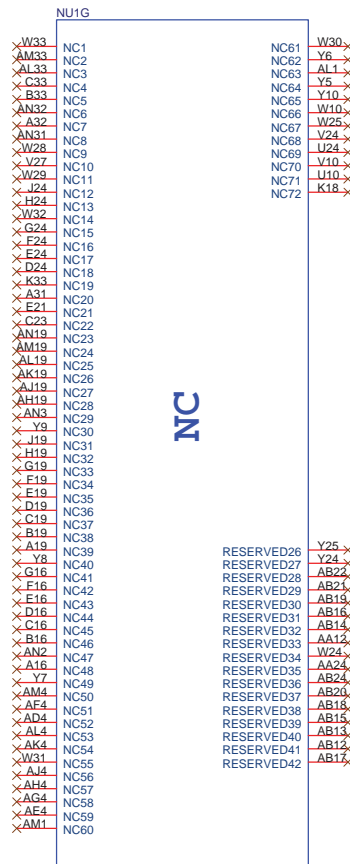
QG82945GSE

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		Title : NB-945GMS(GRAPHIC)	
ASUSTeK COMPUTER INC.		Engineer: <i>Jeff Li</i>	
Size A4	Project Name 1000HO_MB	Rev 1.0G	
Date: Friday, January 23, 2009	Sheet	10	of 47



QG82945GSE

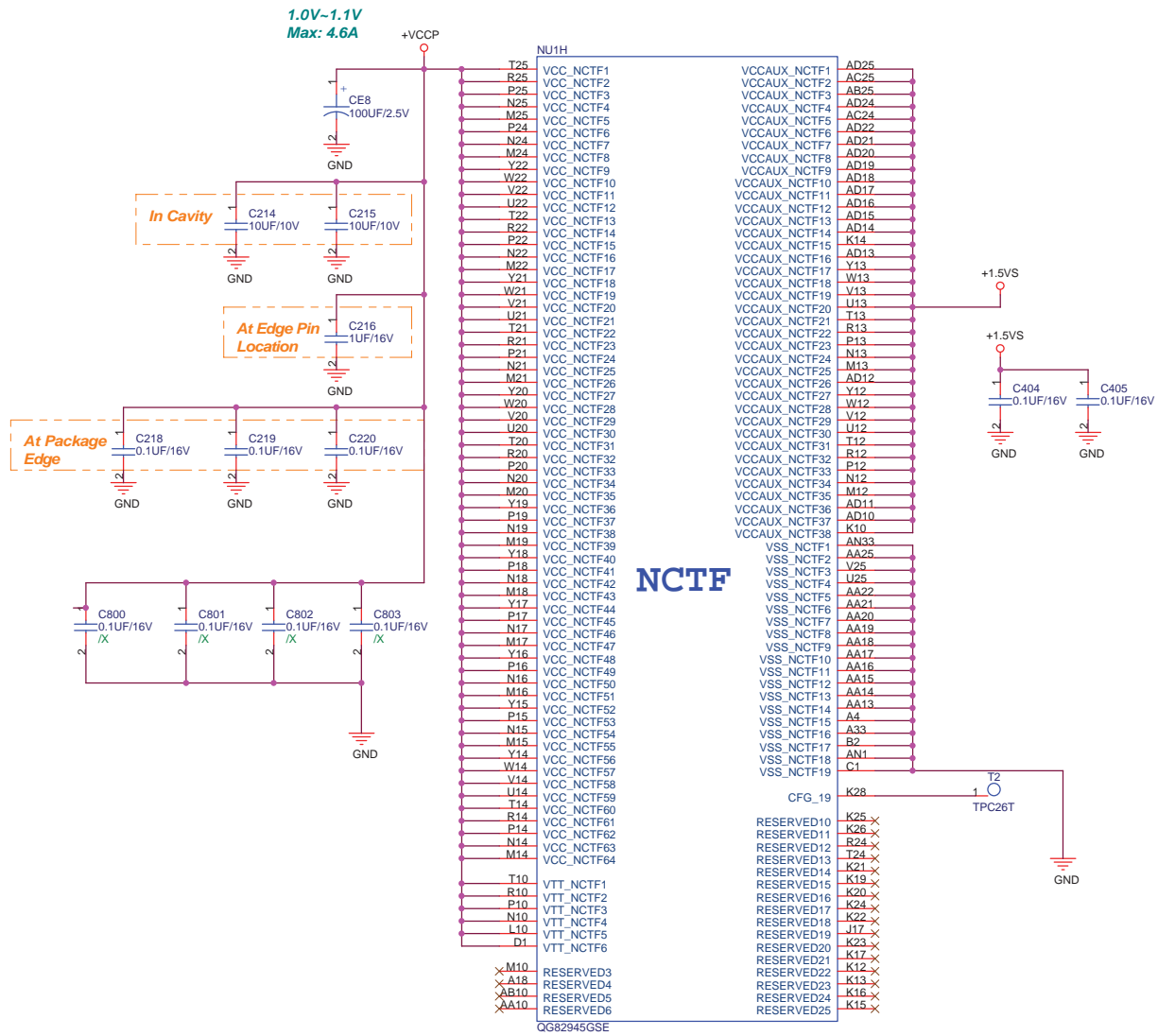


QG82945GSE

<Core Design>

ASUS Title : NB-945GMS(DDR2)
 ASUSTek COMPUTER INC. Engineer: Jeff Li

Size	Project Name	Rev
A3	1000HO_MB	1.0G
Date: Friday, January 23, 2009		Sheet 11 of 47

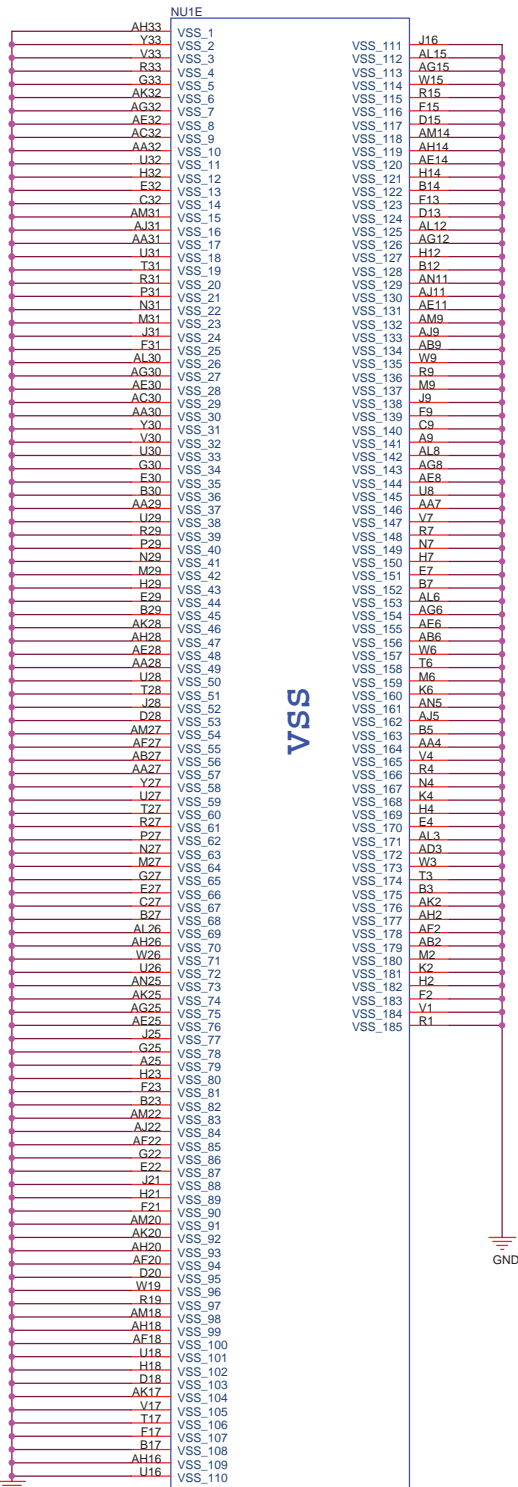


CFG_19(K28) Strapping :
DMI LANE Reversal:
 0:Normal Operation (Default)
 1.:Reversal Lanes, 3->0,2->1..etc
 Note:945GMS doesn't support DMI Lane Reversal

<Core Design>

ASUS Title : NB-945GMS(PWR)
 ASUSTEK COMPUTER INC. Engineer: Jeff Li

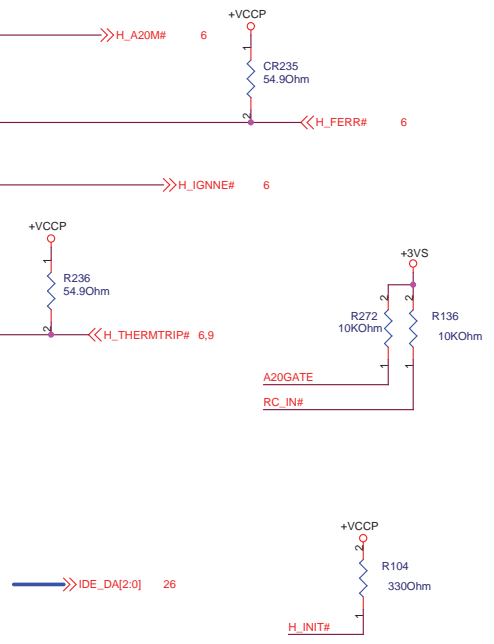
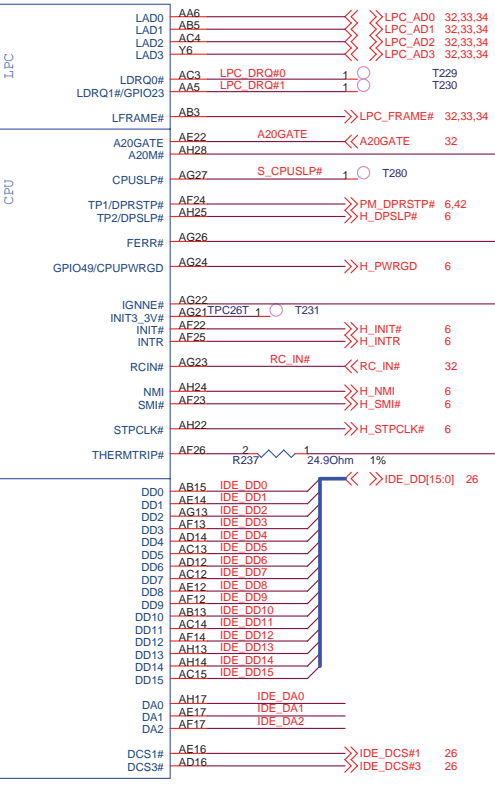
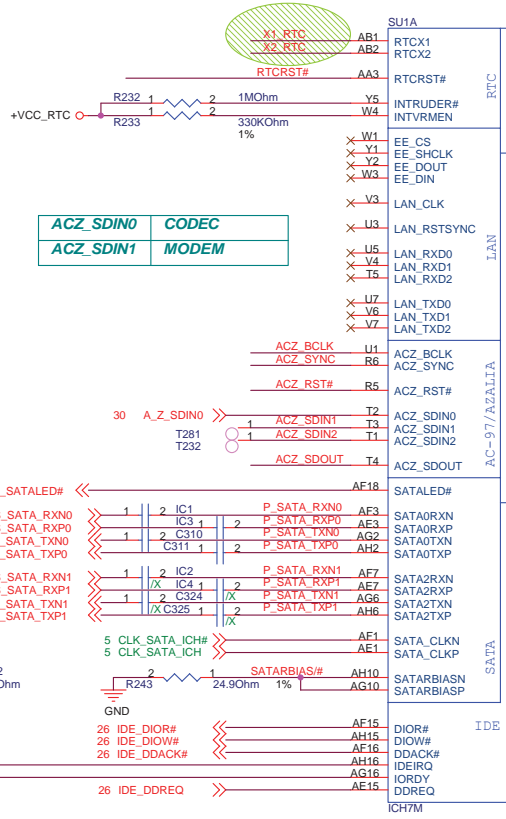
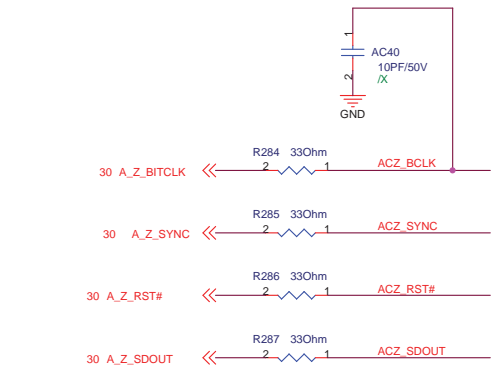
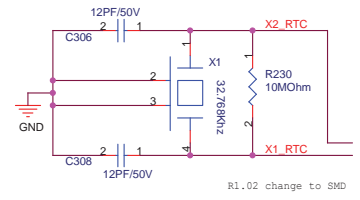
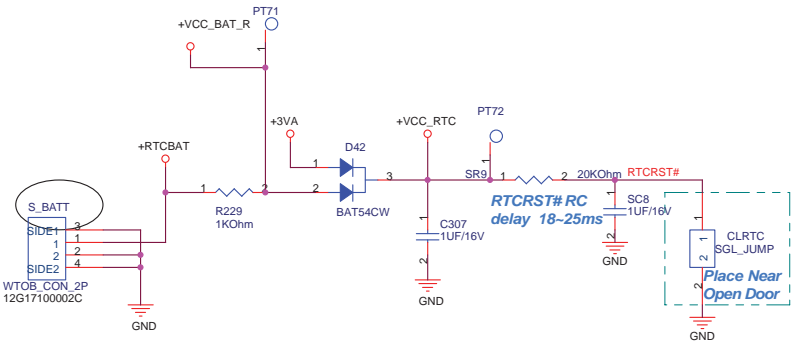
Size	Project Name	Rev
A3	1000HO_MB	1.0G
Date: Friday, January 23, 2009		
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GND

<Core Design>

		Title : NB-945PMS(GND)	
ASUSTeK COMPUTER INC.		Engineer: Jeff Li	
Size	Project Name	Rev	
A3	1000HO_MB	1.0G	
Date: Friday, January 23, 2009	Sheet	14	of 47



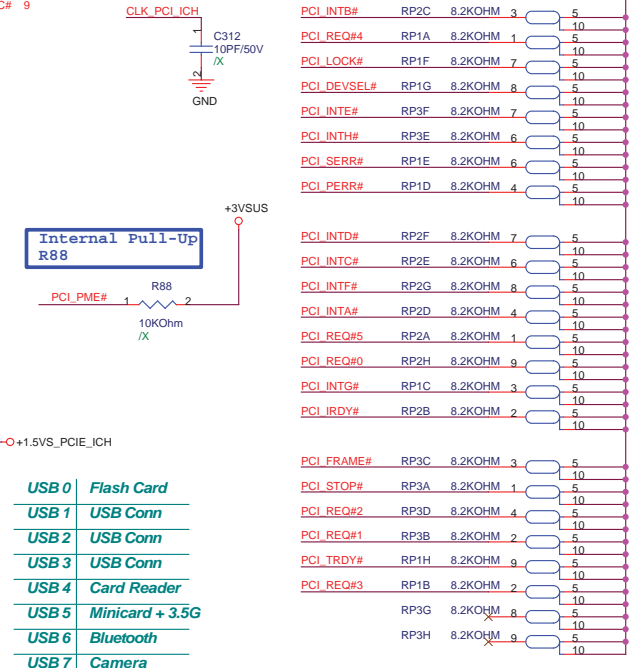
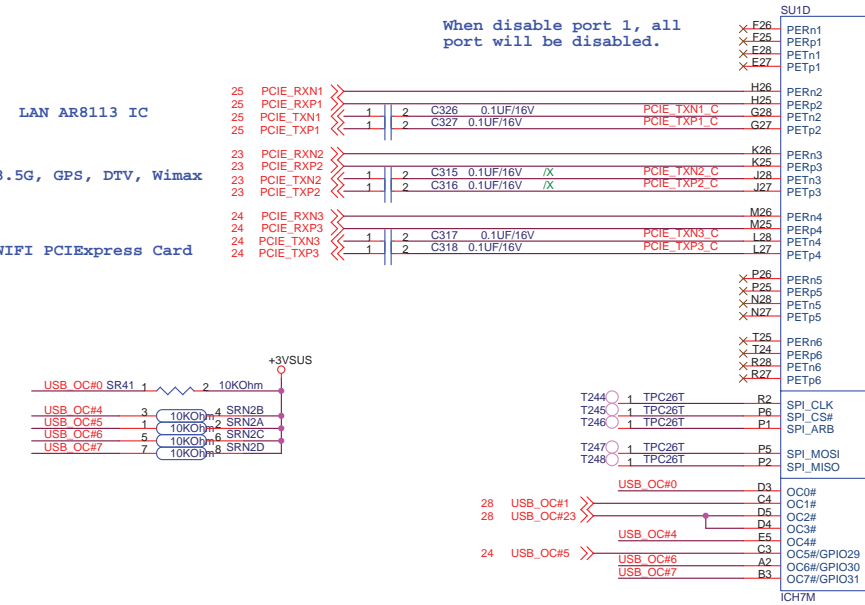
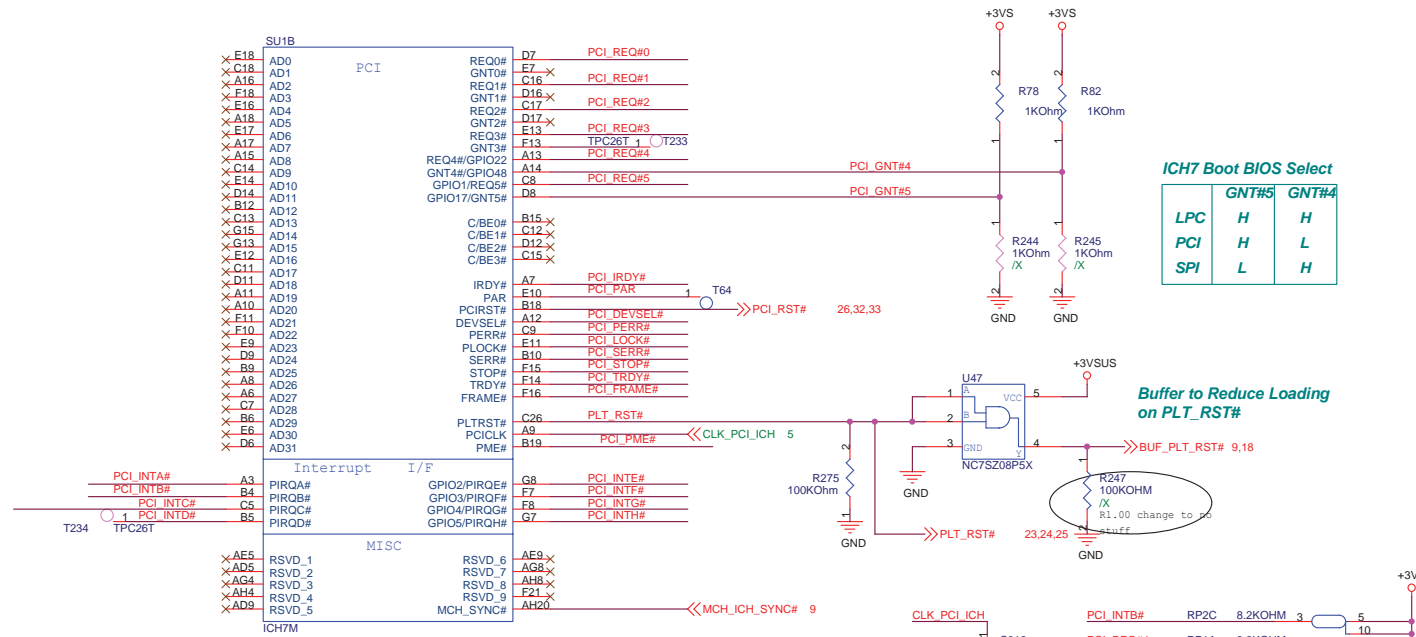
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ASUS Title : SB-ICH7-M(1)

ASUSTek COMPUTER INC. Engineer: Jeff Li

Size	Project Name	Rev
Custom	1000HO_MB	1.0G

Date: Friday, January 23, 2009 Sheet 16 of 47



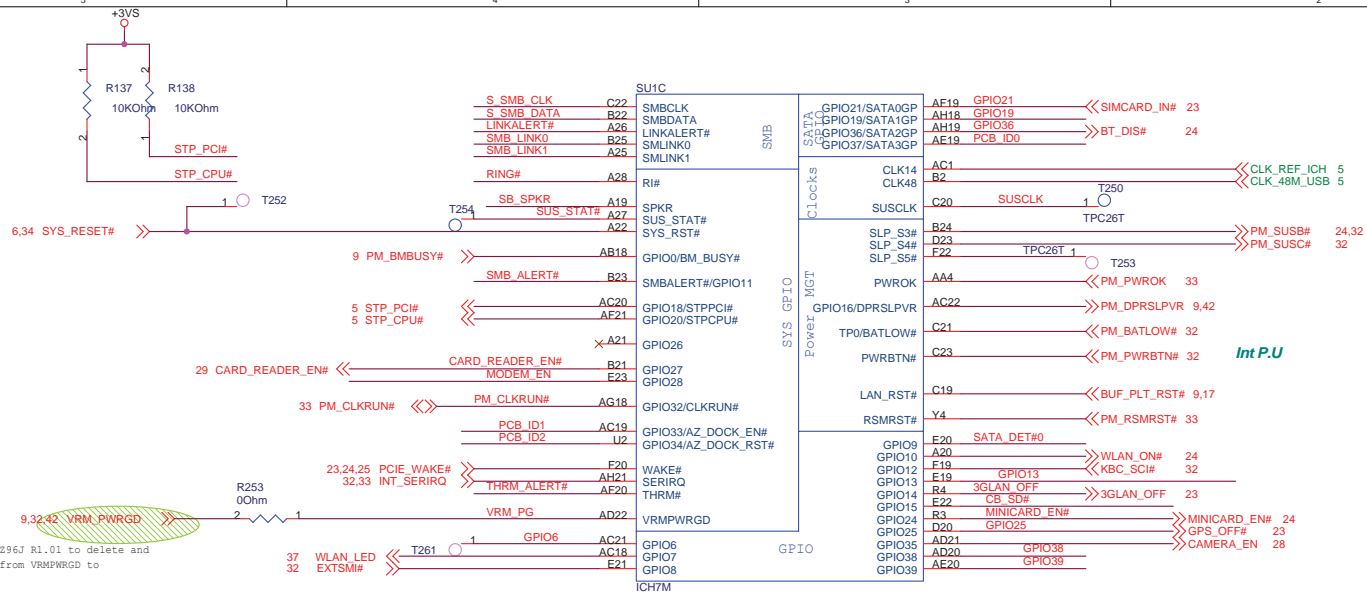
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ASUS Title : SB-ICH7M(2)

ASUSTeK COMPUTER INC. Engineer: Jeff Li

Size	Project Name	Rev
Custom	1000HO_MB	1.0G

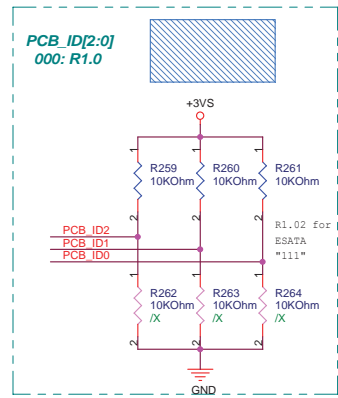
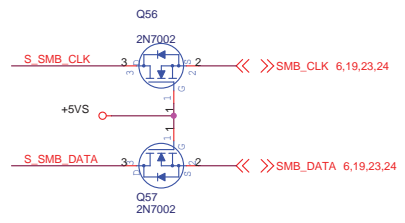
Date: Friday, January 23, 2009 Sheet 17 of 47



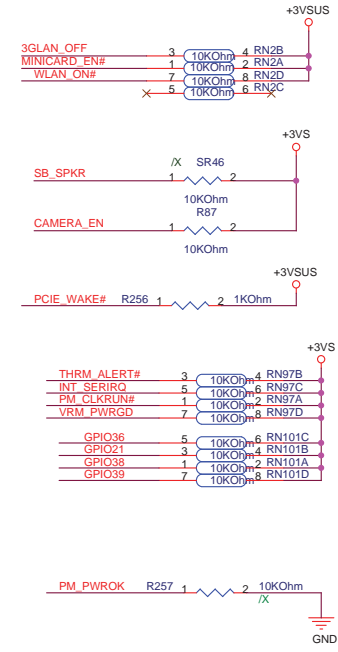
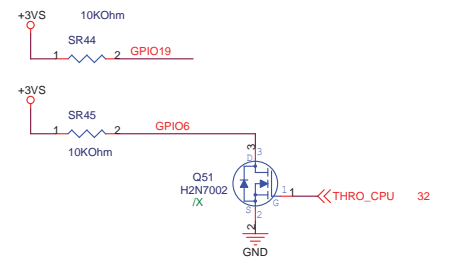
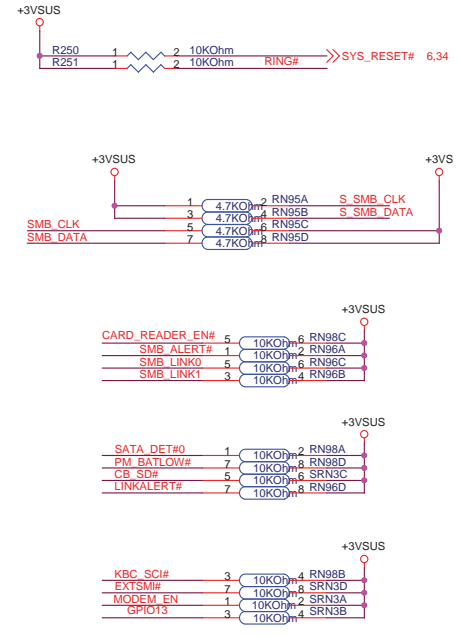
05/12/30, refer Z96J R1.01 to delete and change net name from VRM_PWRGD to VRM_PWRGD.

S_SMB_CLK <<< S_SMB_CLK 5
S_SMB_DATA <<< S_SMB_DATA 5

WLAN_LED	WLAN	BT
High	v	v
High	v	x
High	x	v
Low	x	x

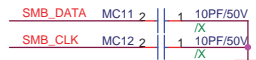
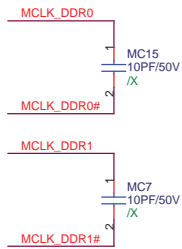


PCB_VID3 : PROJECT CODE



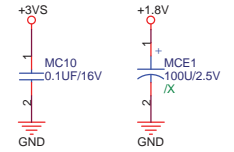
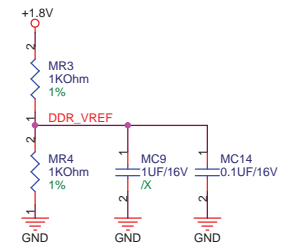
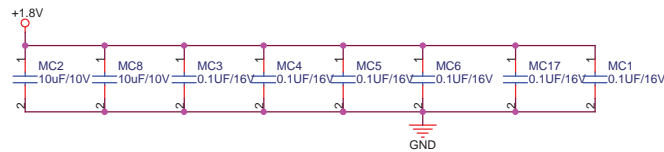
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ASUS		Title : SB-ICH7M(3)	
ASUSTek COMPUTER INC		Engineer: Jeff Li	
Size	Project Name	Rev	
Custom	1000HO_MB	1.0G	
Date: Friday, January 23, 2009	Sheet	18	of 47



STD Type

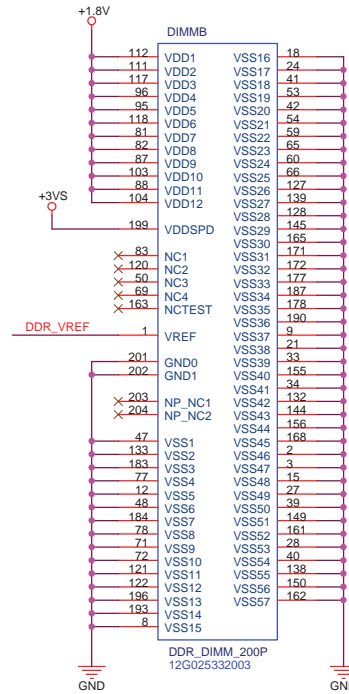
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- << >> MA_DQS[7:0] 11
- << >> MA_DQS#[7:0] 11
- << >> MA_DM[7:0] 11
- << >> MA_MA[13:0] 11,20
- << >> MA_BA[2:0] 11,20



DIMMA		DIMMB	
MA_MA0	102	A0	DQ0
MA_MA1	101	A1	DQ1
MA_MA2	100	A2	DQ2
MA_MA3	99	A3	DQ3
MA_MA4	98	A4	DQ4
MA_MA5	97	A5	DQ5
MA_MA6	94	A6	DQ6
MA_MA7	92	A7	DQ7
MA_MA8	93	A8	DQ8
MA_MA9	91	A9	DQ9
MA_MA10	105	A10/AP	DQ10
MA_MA11	90	A11	DQ11
MA_MA12	89	A12	DQ12
MA_MA13	116	A13	DQ13
	X 86	A14	DQ14
MA_BA2	X 85	A15	DQ15
	X 84	A16_BA2	DQ16
MA_BA0	107	BA0	DQ17
MA_BA1	106	BA1	DQ18
	110	BA2	DQ19
9,20 MA_CS#0	X 115	S0#	DQ20
9,20 MA_CS#1	X 114	S1#	DQ21
9 MCLK_DDR0	30	CK0	DQ22
9 MCLK_DDR#0	32	CK0#	DQ23
9 MCLK_DDR1	164	CK1	DQ24
9 MCLK_DDR1#	166	CK1#	DQ25
9,20 MA_CKE0	79	CKE0	DQ26
9,20 MA_CKE1	80	CKE1	DQ27
11,20 MA_CAS#	113	CAS#	DQ28
11,20 MA_RAS#	108	RAS#	DQ29
11,20 MA_WE#	109	WE#	DQ30
	198	SA0	DQ31
	200	SA1	DQ32
6,18,23,24 SMB_CLK	X 197	SCL	DQ33
6,18,23,24 SMB_DATA	X 195	SDA	DQ34
		DQ35	DQ35
9,20 MA_ODT0	X 114	ODT0	DQ36
9,20 MA_ODT1	X 119	ODT1	DQ37
		DQ38	DQ38
MA_DM0	10	DM0	DQ39
MA_DM2	26	DM1	DQ40
MA_DM1	52	DM2	DQ41
MA_DM3	67	DM3	DQ42
MA_DM4	147	DM4	DQ43
MA_DM5	130	DM4	DQ43
MA_DM6	170	DM5	DQ44
MA_DM7	185	DM6	DQ45
		DM7	DQ46
		DQ47	DQ47
MA_DQS0	13	DQ48	DQ48
MA_DQS2	31	DQ49	DQ49
MA_DQS1	51	DQ50	DQ50
MA_DQS3	70	DQ51	DQ51
MA_DQS4	131	DQ52	DQ52
MA_DQS5	148	DQ53	DQ53
MA_DQS6	169	DQ54	DQ54
MA_DQS7	188	DQ55	DQ55
MA_DQS#0	11	DQ56	DQ56
MA_DQS#2	29	DQ57	DQ57
MA_DQS#1	49	DQ58	DQ58
MA_DQS#3	68	DQ59	DQ59
MA_DQS#4	129	DQ60	DQ60
MA_DQS#5	146	DQ61	DQ61
MA_DQS#6	167	DQ62	DQ62
MA_DQS#7	186	DQ63	DQ63

DDR_DIMM_200P
12G025332003



GROUP1
GROUP2
SWAP

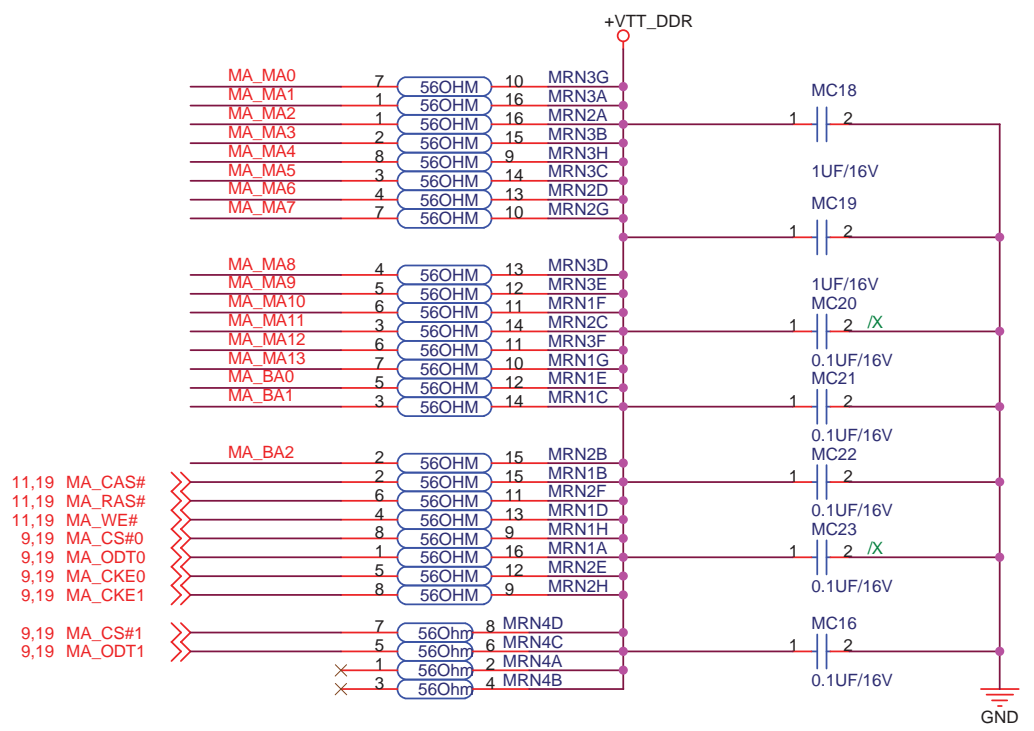


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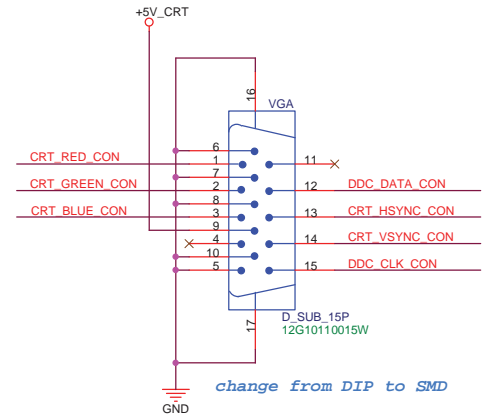
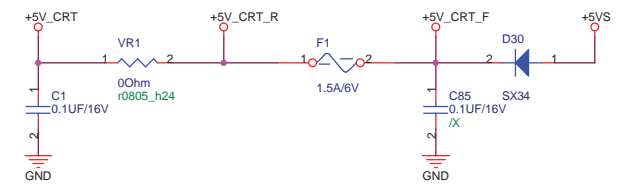
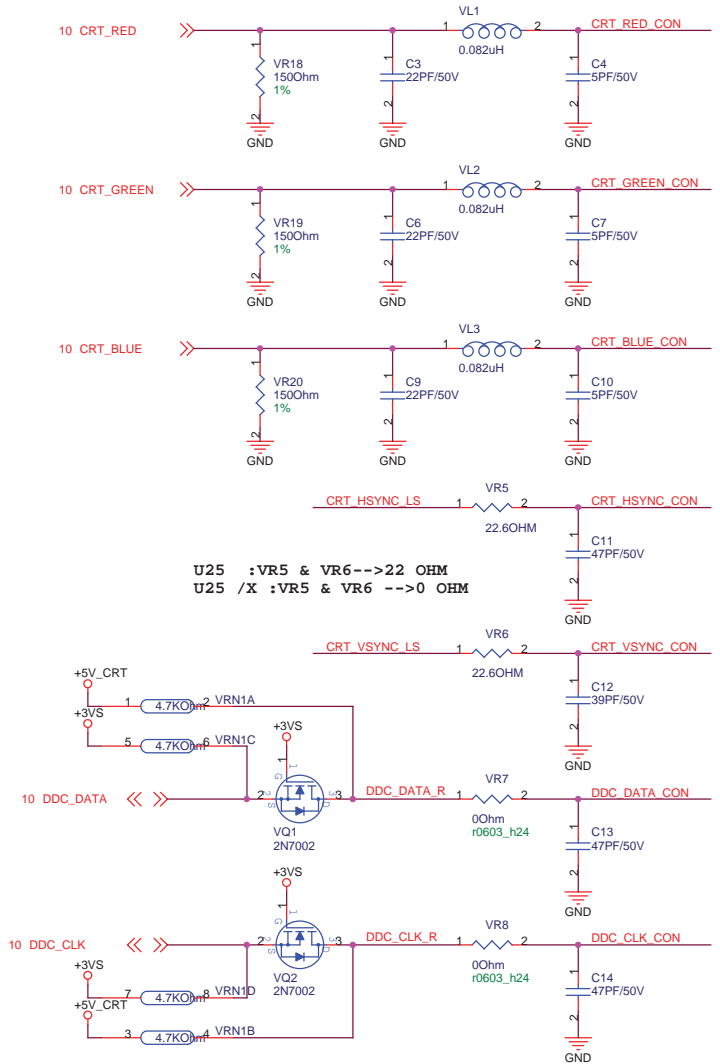
ASUS		Title : DDR2 SODIMM	
ASUSTek Computer INC.		Engineer: Jeff Li	
Size A3	Project Name 1000HO_MB	Rev 1.0G	
Date: Friday, January 23, 2009	Sheet	19	of 52

 << MA_MA[13:0] 11,19
 << MA_BA[2:0] 11,19

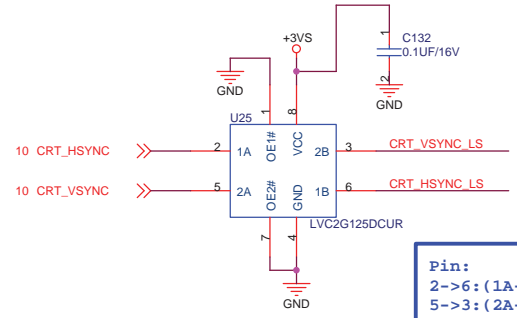


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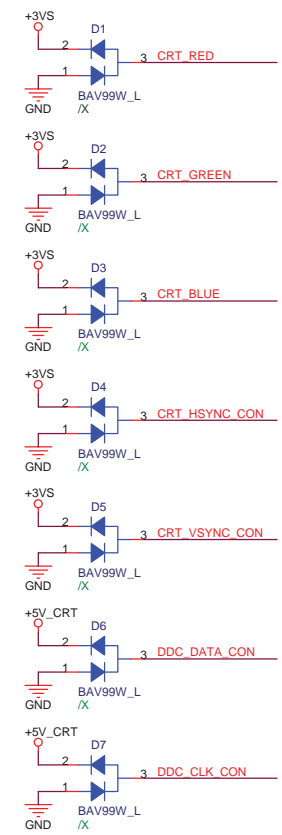
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ASUSTek Computer INC.		Engineer: <i>Jeff Li</i>	
Size	Project Name	Rev	
A4	1000HO_MB	1.0G	
Date: Friday, January 23, 2009	Sheet	20	of 52



VGA use 12G10110015W & 12G10110015N

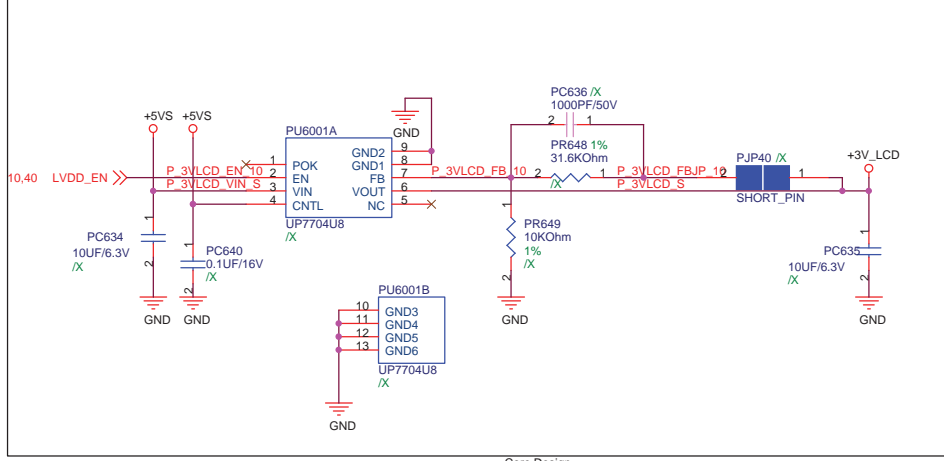
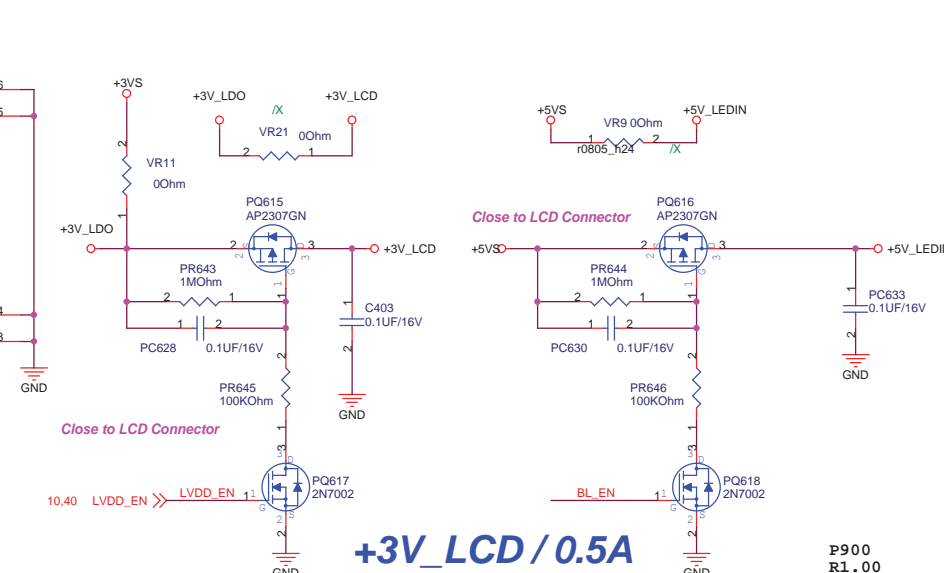
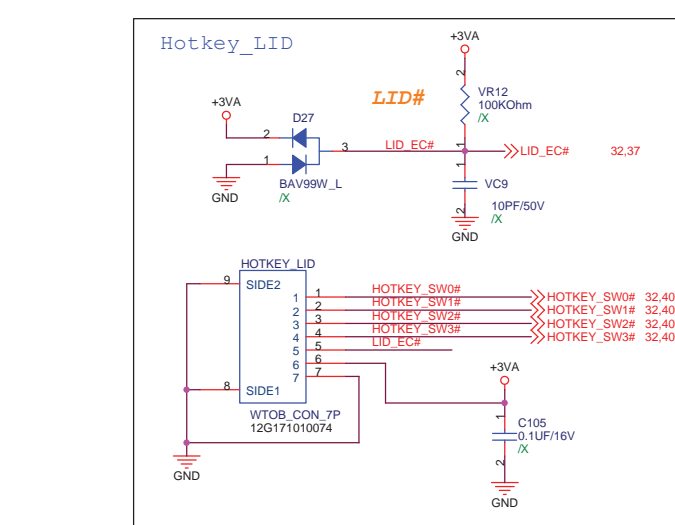
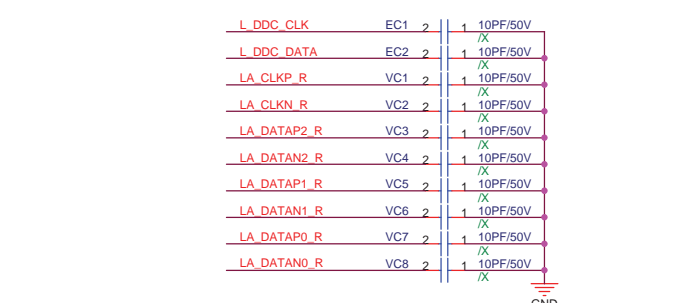
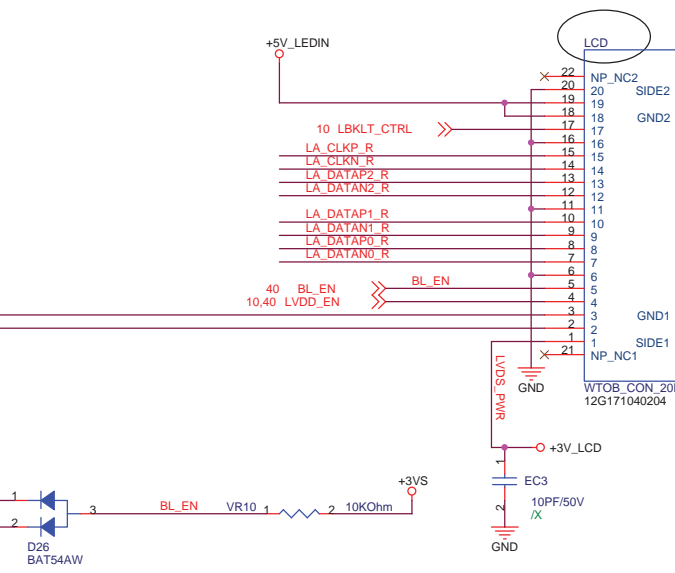
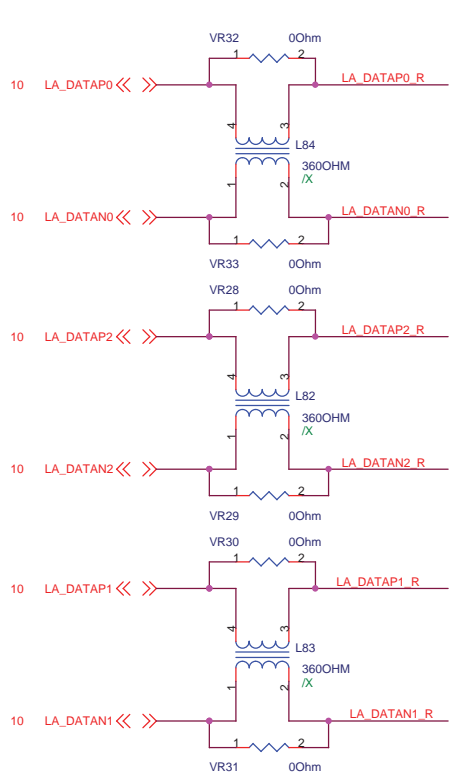
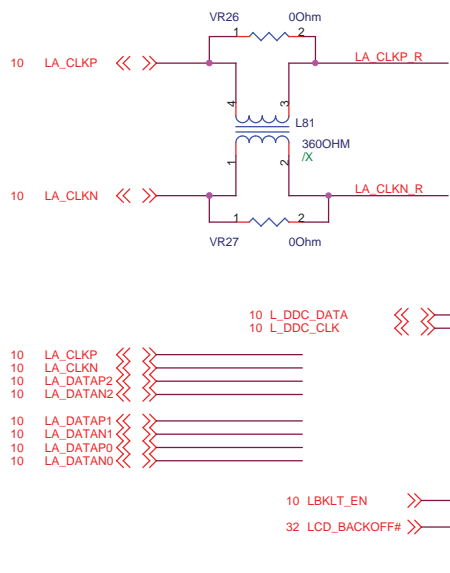


Pin:
2->6: (1A->1B)
5->3: (2A->2B)



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ASUS		Title : Onboard VGA	
ASUSTek Computer INC.		Engineer: Jeff Li	
Size	Project Name		Rev
A3	1000HO_MB		1.0G
Date:	Friday, January 23, 2009	Sheet	21 of 52

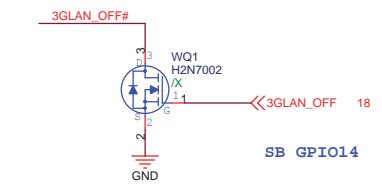
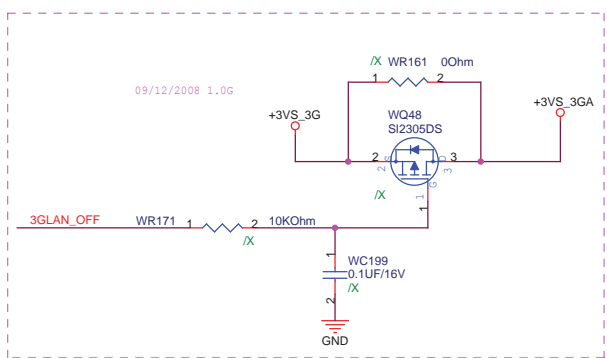
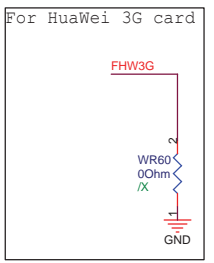
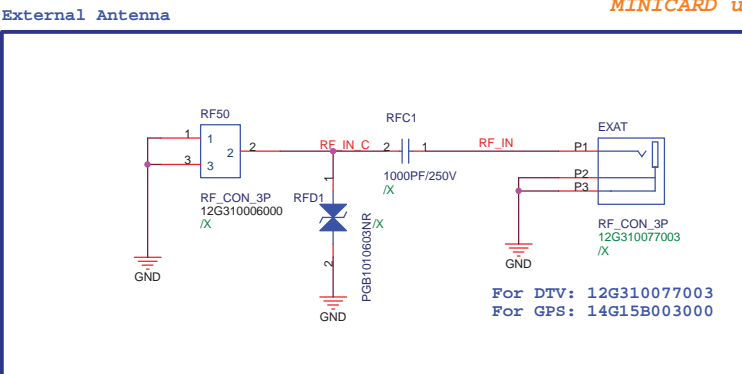
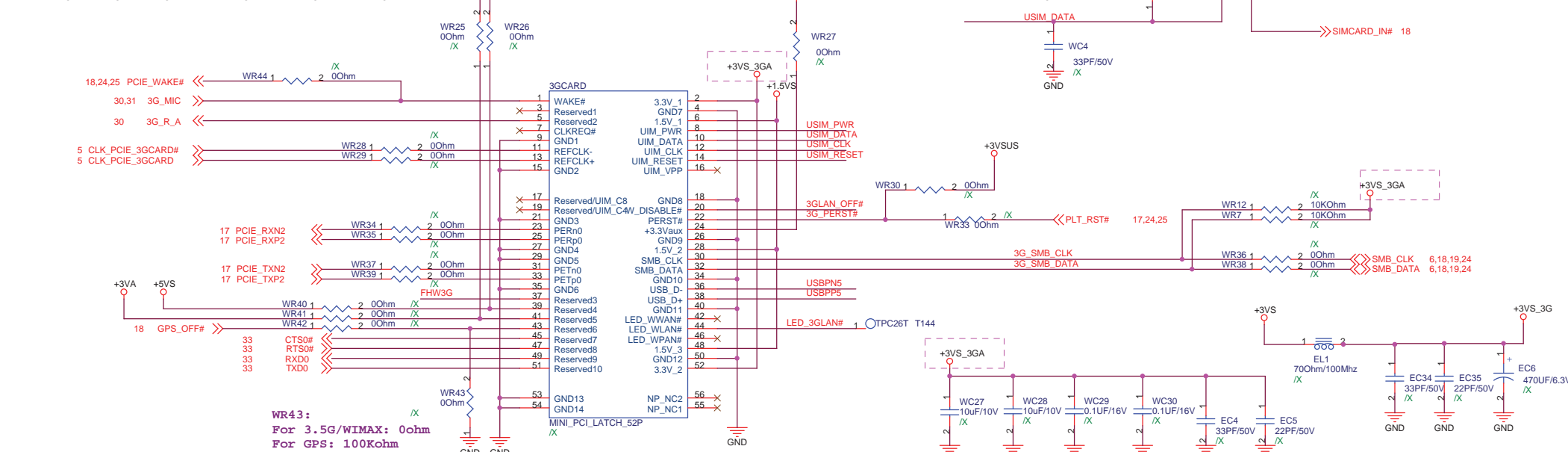
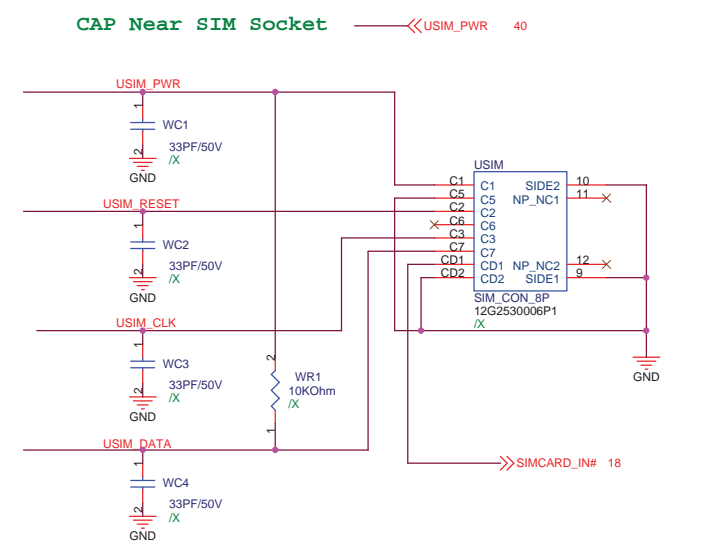
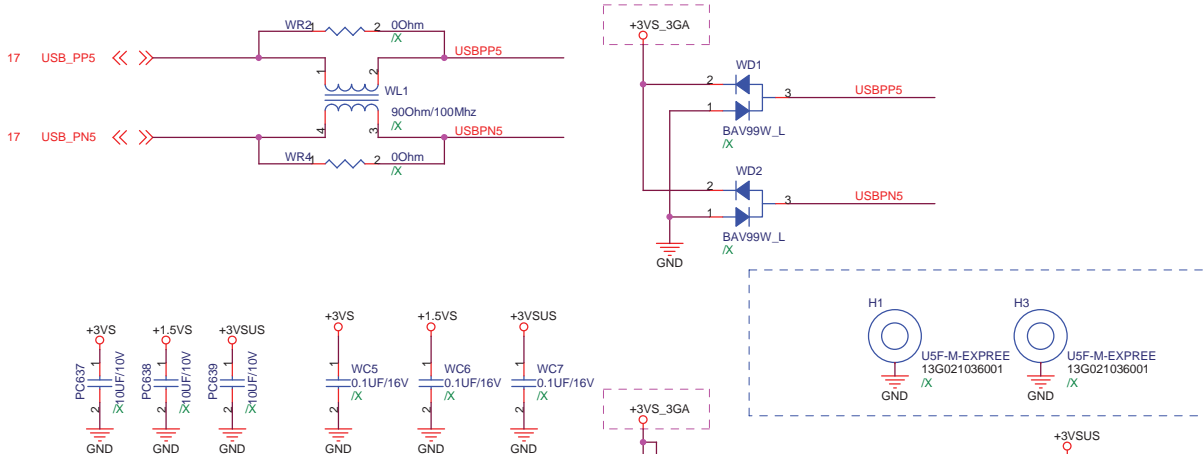


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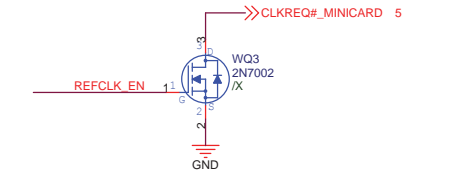
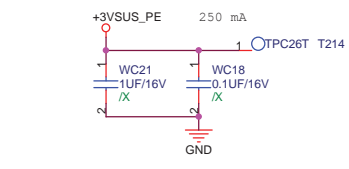
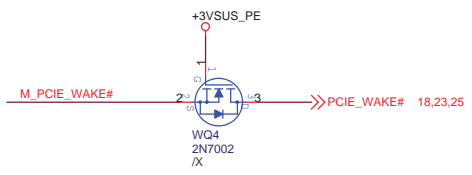
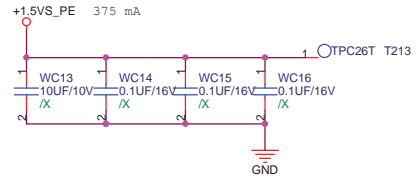
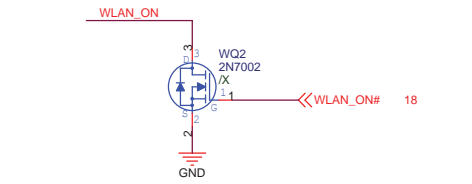
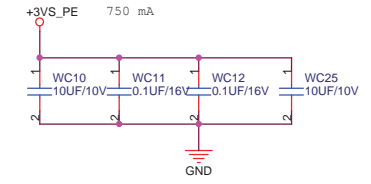
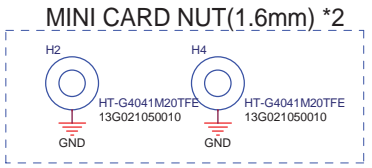
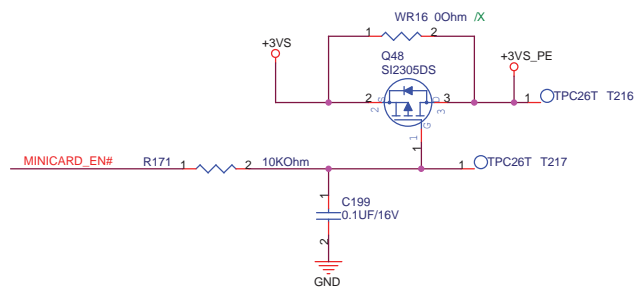
ASUSTek Computer INC. Engineer: Jeff Li

Size	Project Name	Rev
A3	1000HO_MB	1.0G
Date: Friday, January 23, 2009	Sheet 22 of 52	

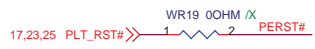
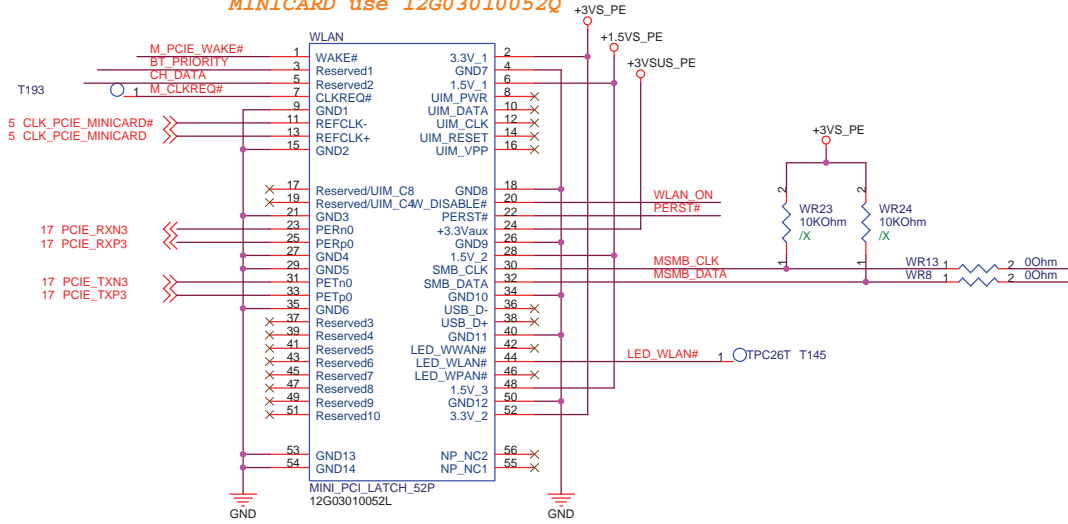


<Core Design> 3.5G Module & External Antenna

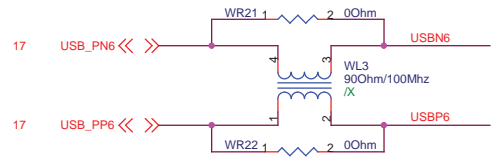
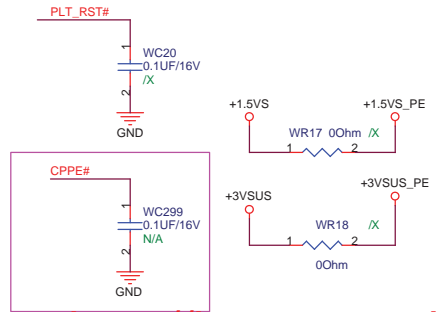
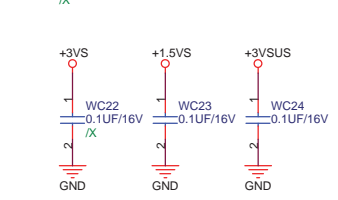
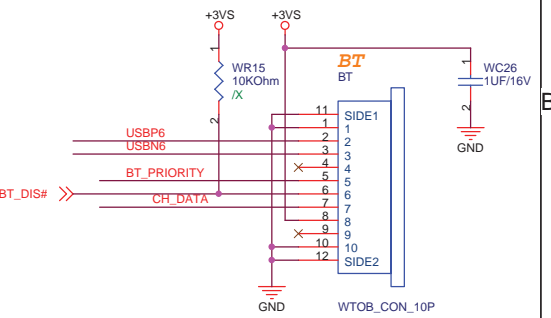
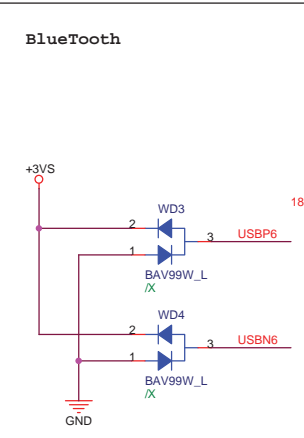
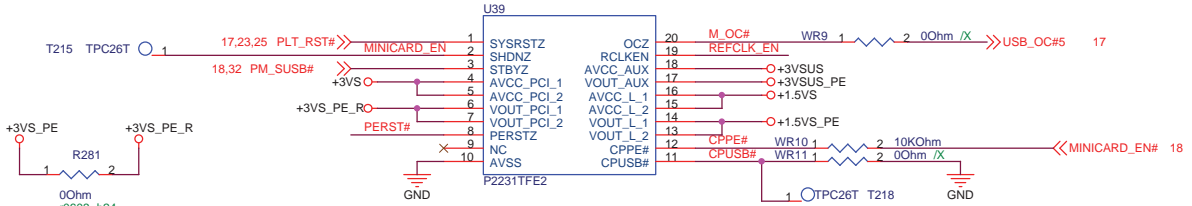
ASUS Title :	
ASUSTek Computer INC. Engineer: Jeff Li	
Size A3 Project Name	1000HO_MB
Date: Friday, January 23, 2009	Sheet 23 of 52



MINICARD use 12G03010052Q

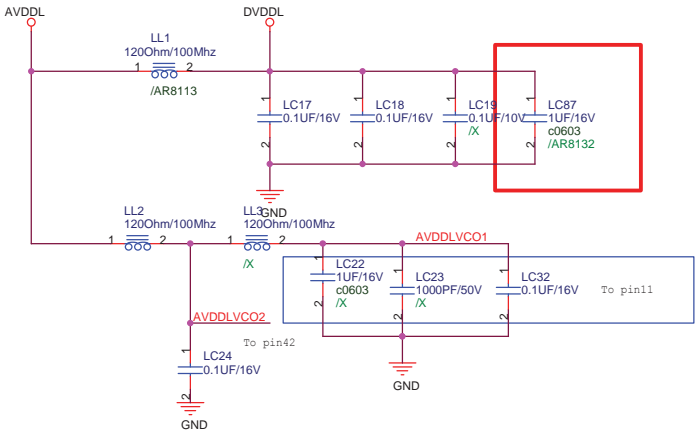
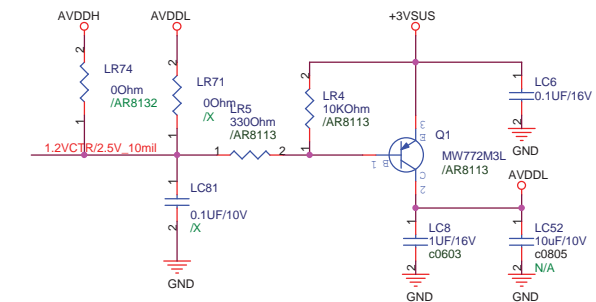
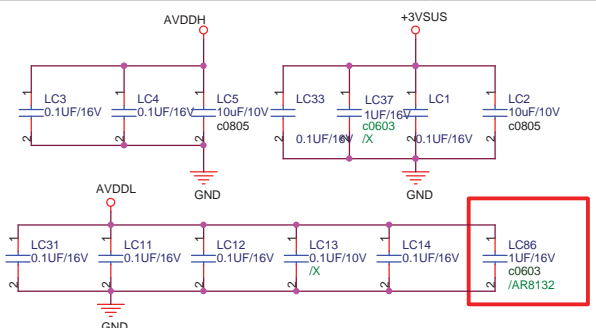


U39 use 06G030057013

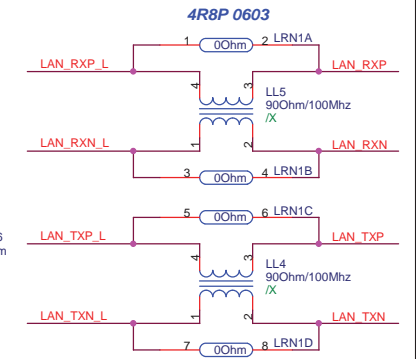
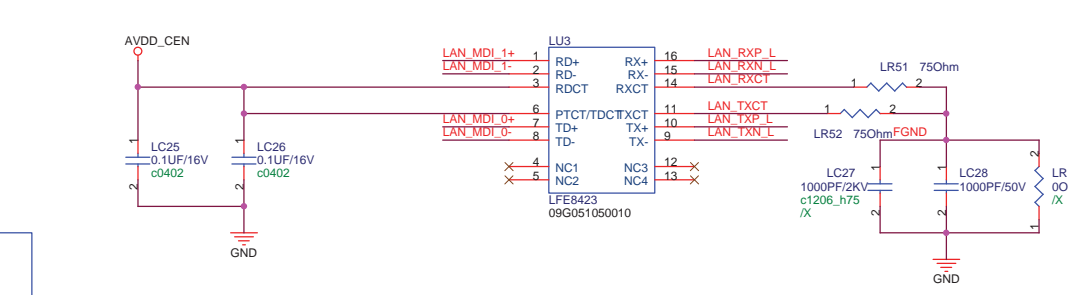
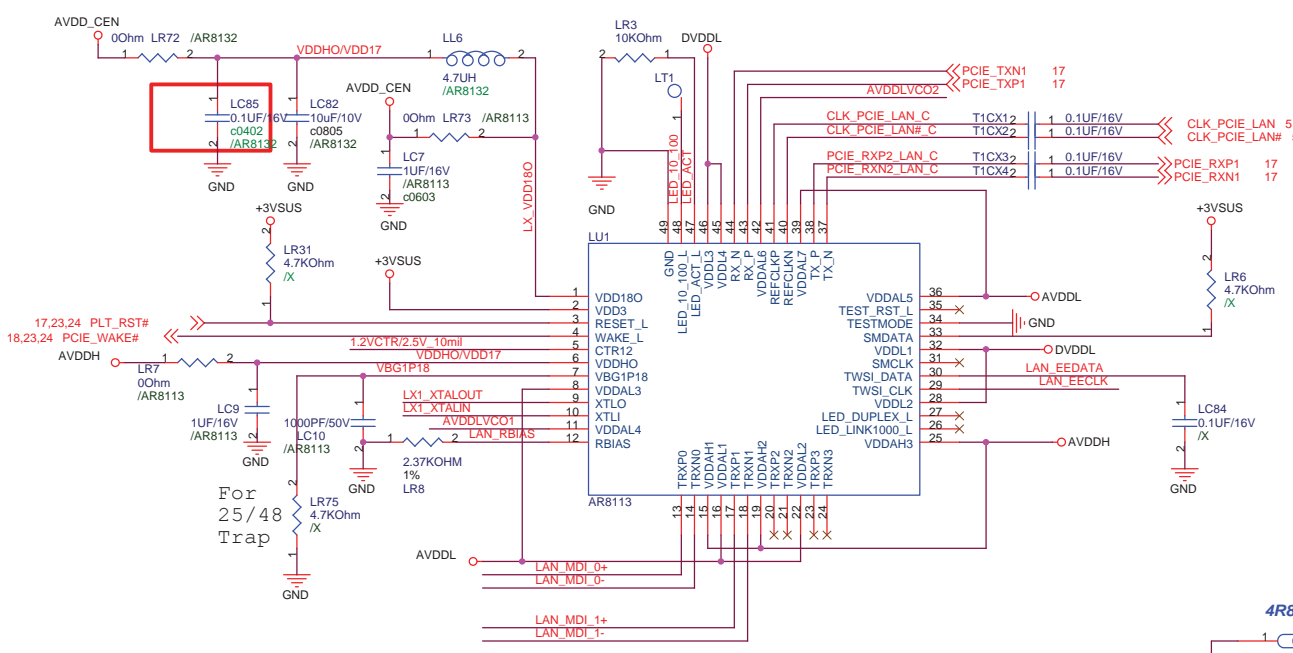
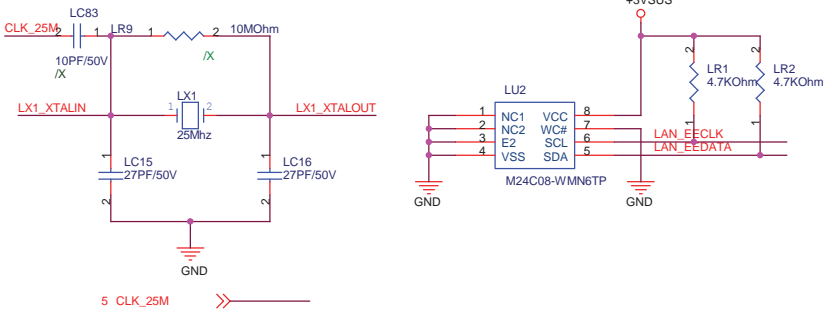


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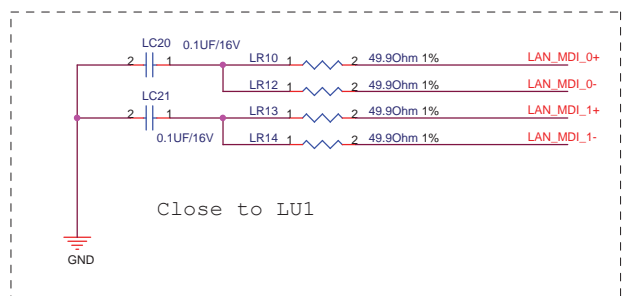
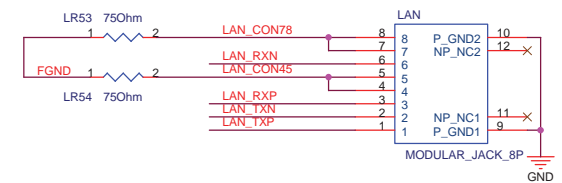
ASUS		Title : Minicard	
ASUSTek Computer INC.		Engineer: Jeff Li	
Size A3	Project Name	1000HO_MB	Rev 1.0G
Date: Friday, January 23, 2009	Sheet	24	of 47



if overclocking LL3 Kept and LL2 removed
if not overclocking LL3 removed and LL2 Kept



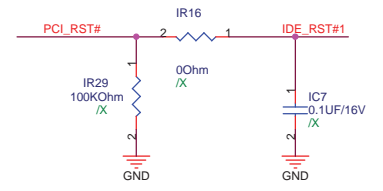
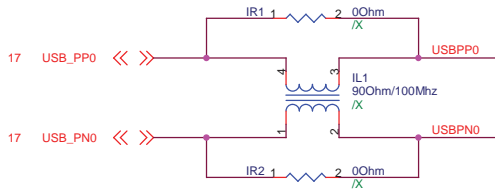
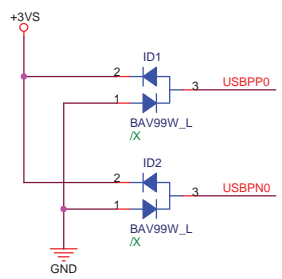
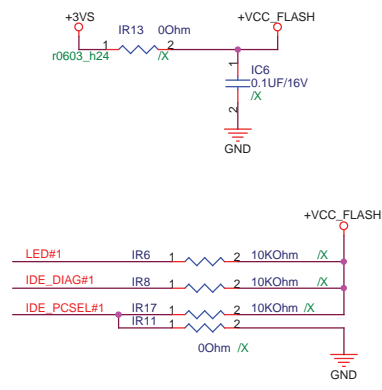
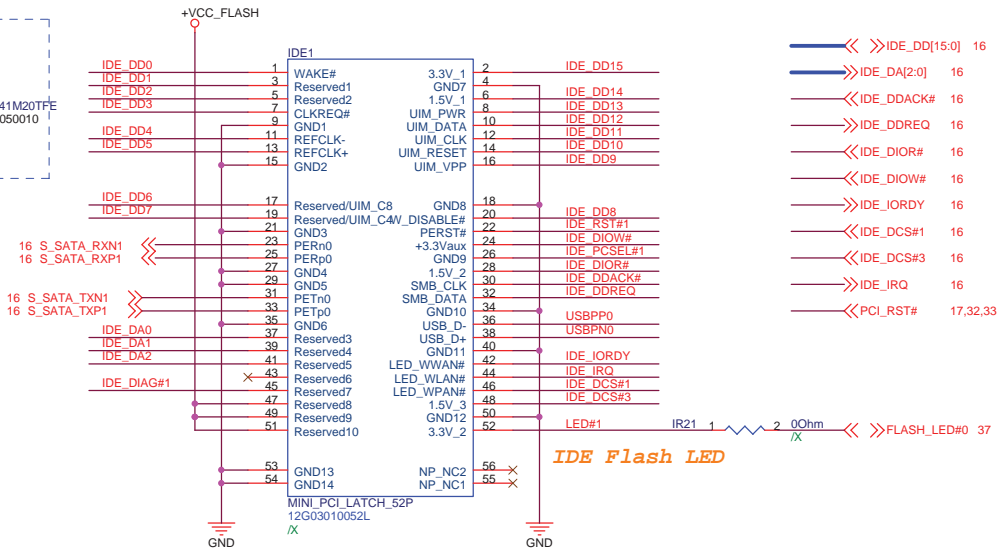
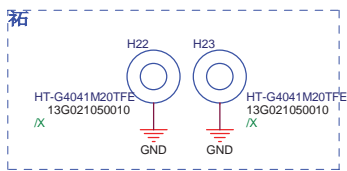
LAN connector: 12G148301086



Close to LU1

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Title : AR8113 / AR8132
ASUS Computer INC **Engineer:** Jeff Li
 Size A3 Project Name **1000HO_MB** Rev 1.0G
 Date: Friday, January 23, 2009 Sheet 25 of 47

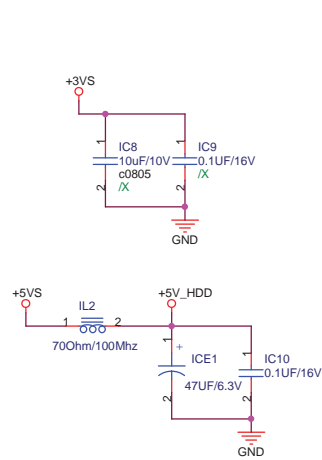
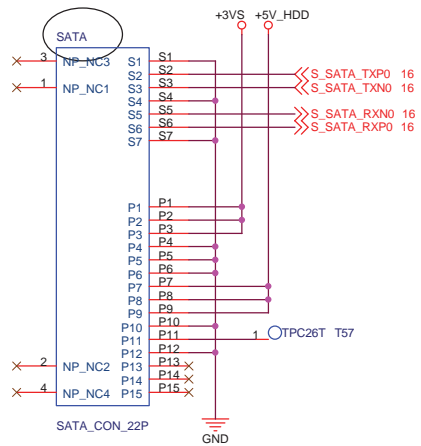


Naming Rule:
 IC: IU?
 R: IR?
 C: IC?
 L: IL?

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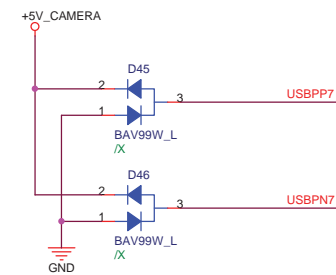
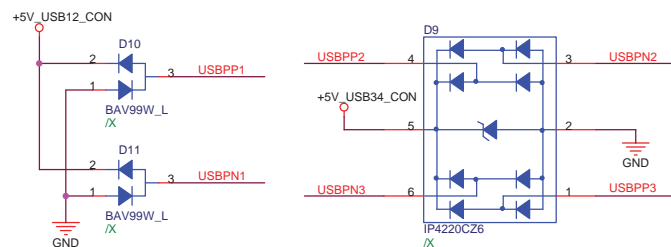
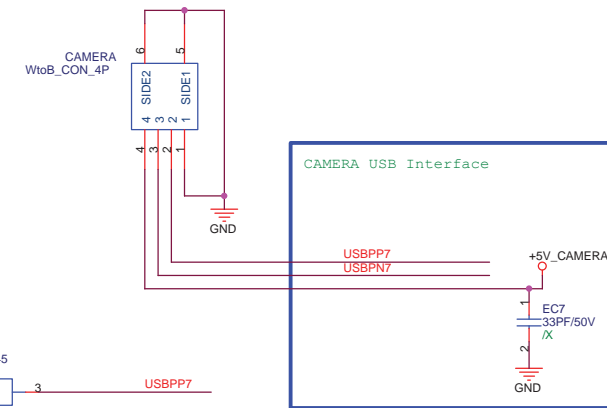
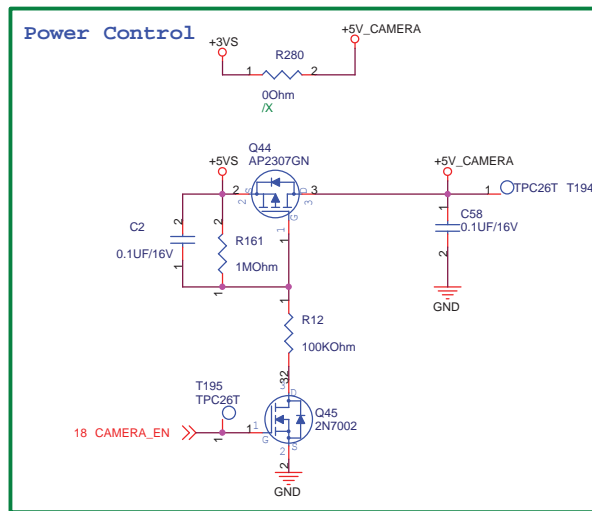
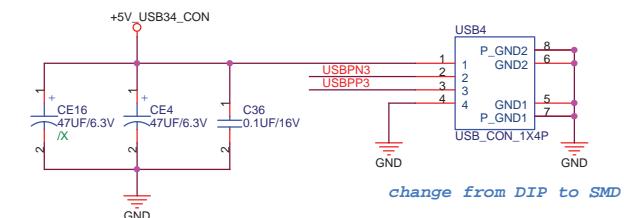
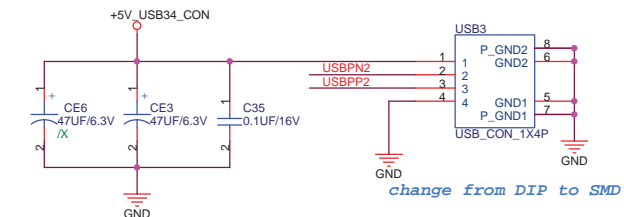
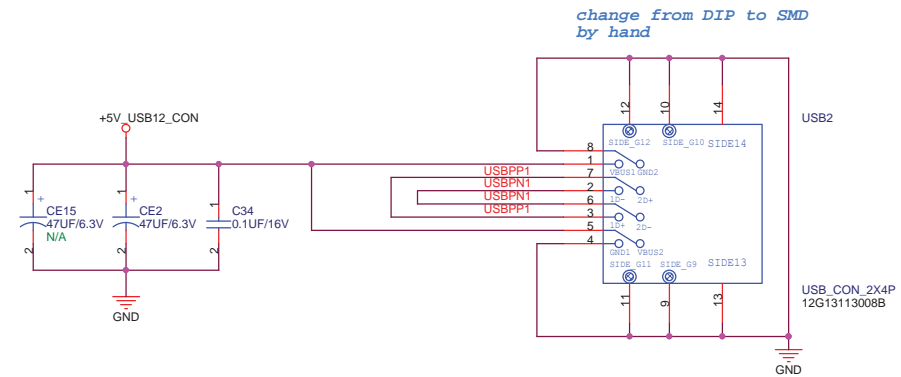
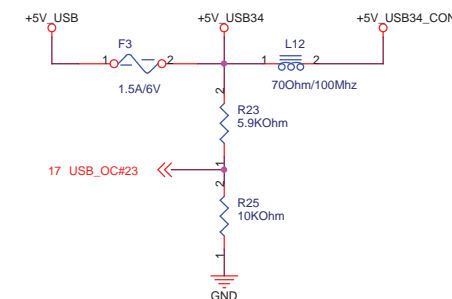
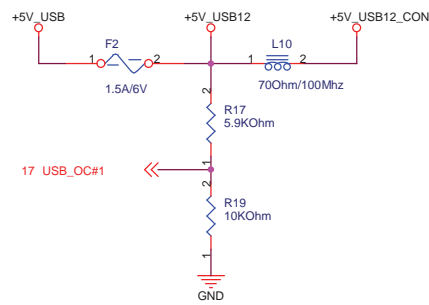
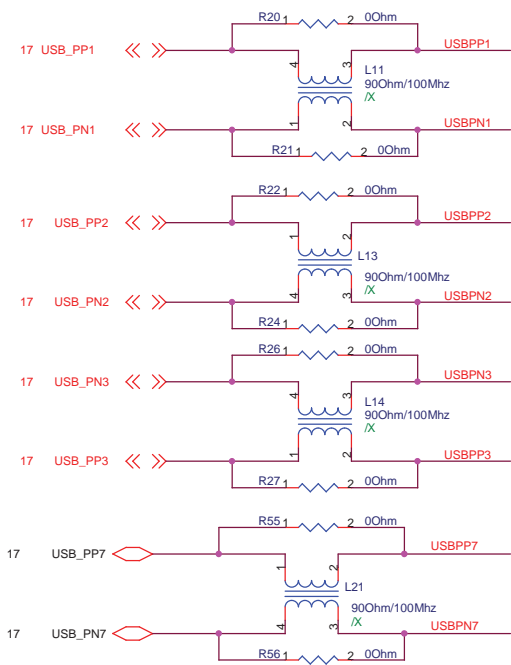
ASUS		Title : HD + Flash Conn	
ASUSTek Computer INC.		Engineer: <i>Kell_Huang</i>	
Size	Project Name	Rev	
A3	1000H_MB	1.1G	
Date: Friday, January 23, 2009	Sheet	26	of 47

SATA HDD Connector



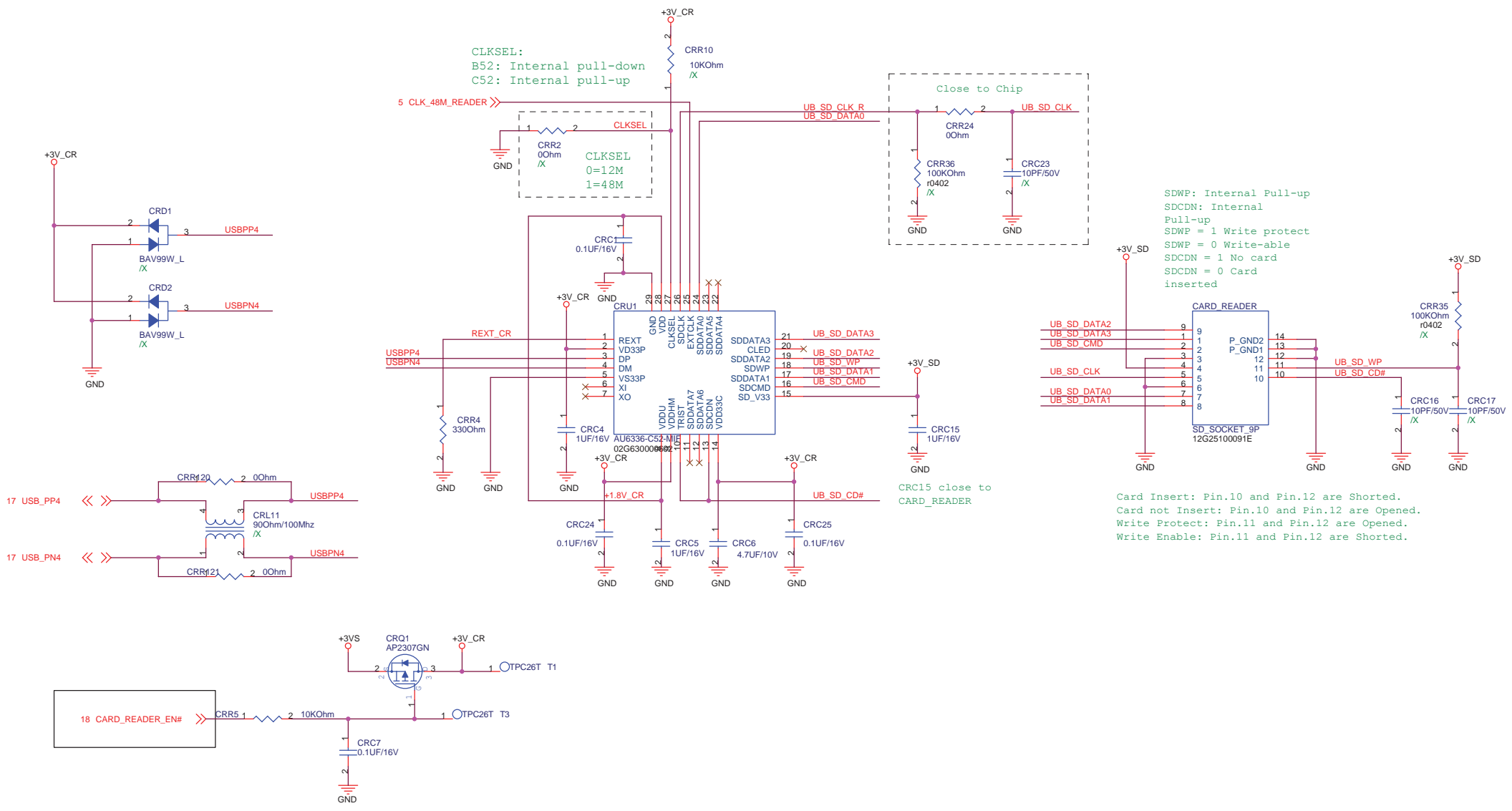
<Core Design>

ASUS		Title : HDD	
ASUSTek Computer INC.		Engineer: Jeff Li	
Size	Project Name		Rev
A3	1000HO_MB		1.0G
Date: Friday, January 23, 2009	Sheet	27 of 47	



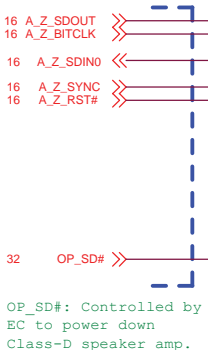
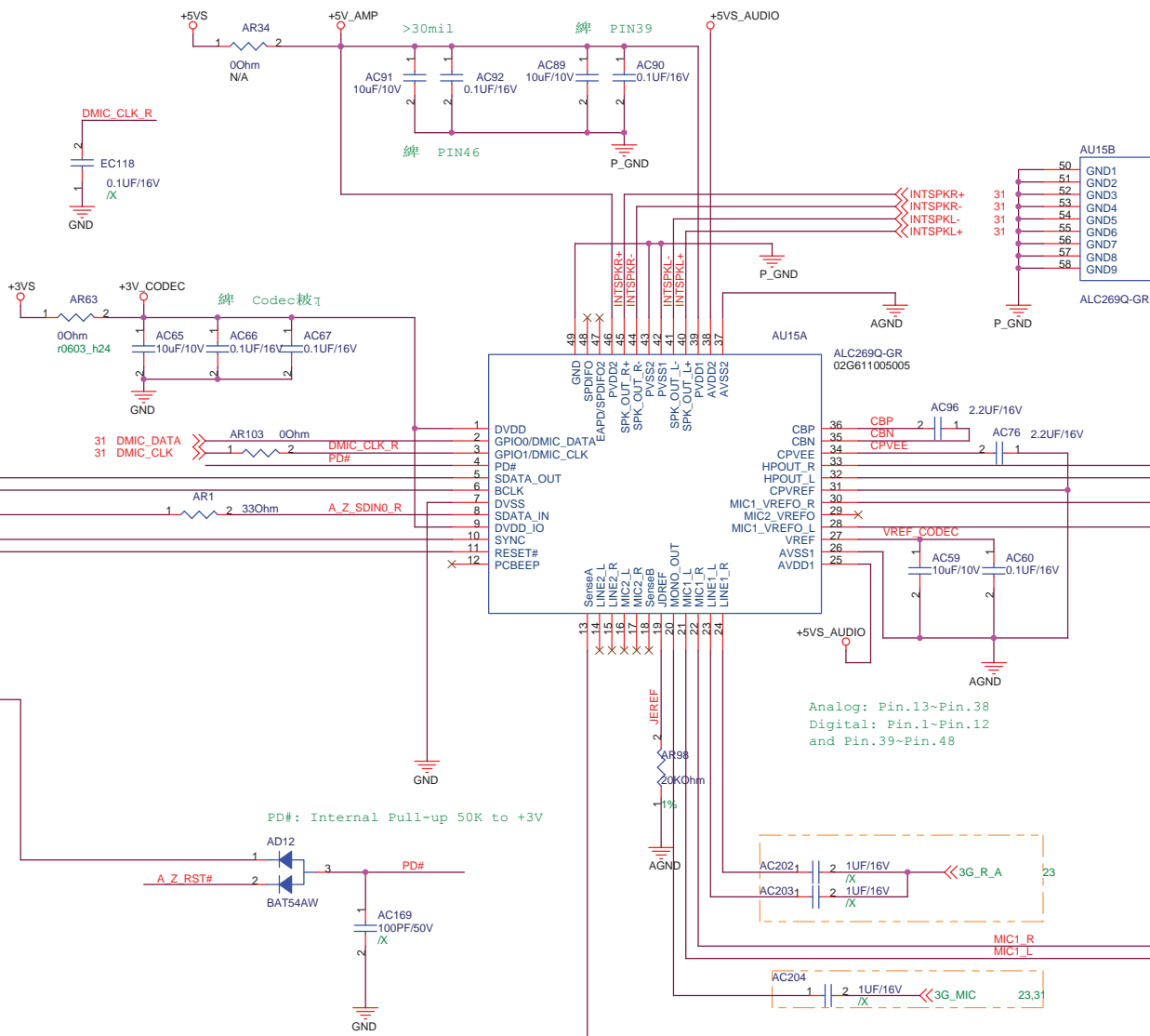
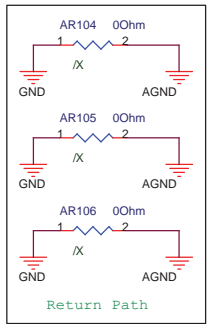
<Core Design>

ASUS		Title : USB Port	
ASUSTek Computer INC.		Engineer: Jeff Li	
Size	Project Name	Rev	
A3	1000HO_MB		1.0G
Date: Friday, January 23, 2009	Sheet	28 of 52	

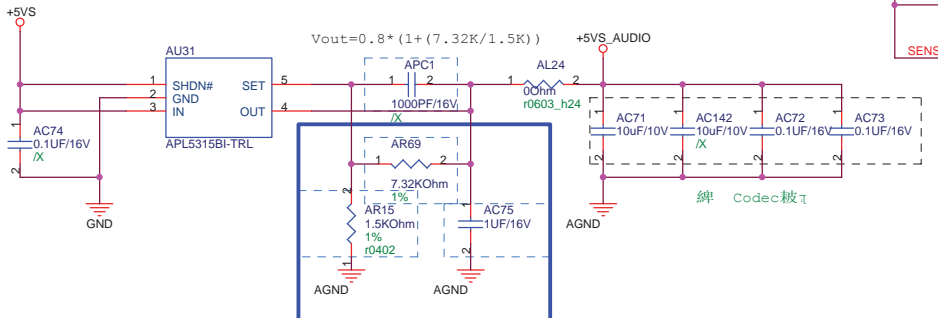
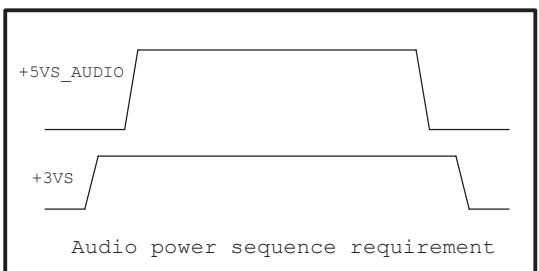


<Core Design>

ASUS		Title : AU6336-C52	
ASUSTek Computer Inc.		Engineer: Jeff Li	
Size A3	Project Name 1000HO_MB	Rev 1.0G	
Date: Friday, January 23, 2009	Sheet 29	of 47	



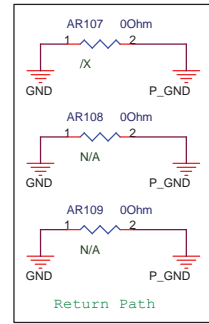
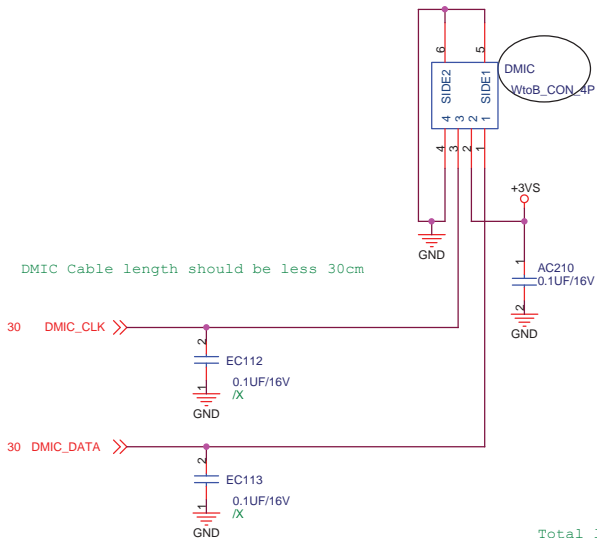
PD#: Internal Pull-up 50K to +3V



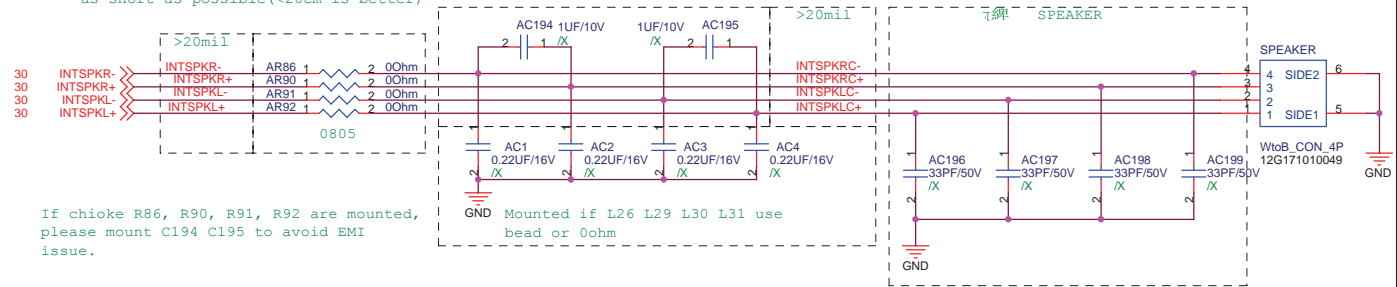
Need 4.7u/10V X5R to prevent poor THD+N

<Core Design>

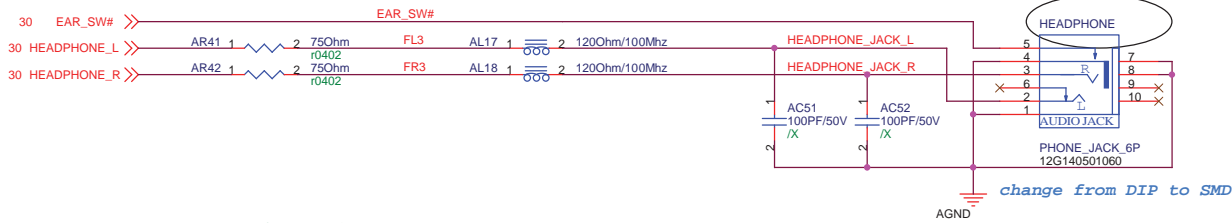
ASUS		Title : ALC269-1	
ASUSTek Computer Inc.		Engineer: Jeff Li	
Size A3	Project Name 1000HO_MB	Rev 1.0G	
Date: Friday, January 23, 2009	Sheet	30 of	47



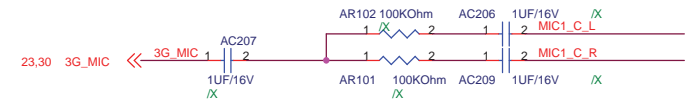
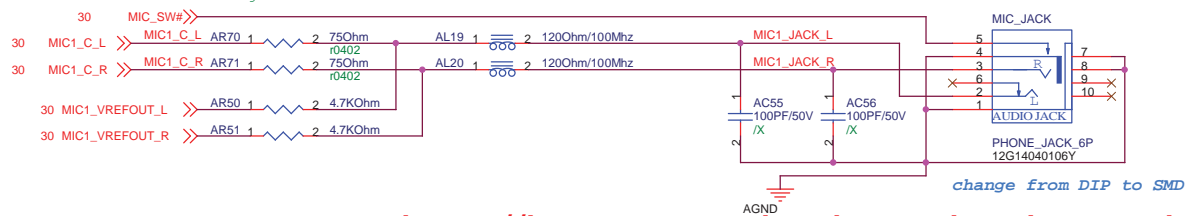
Total length from speakerR+- L+- (pin40 41 44 45) to internal speaker please as short as possible (<20cm is better)



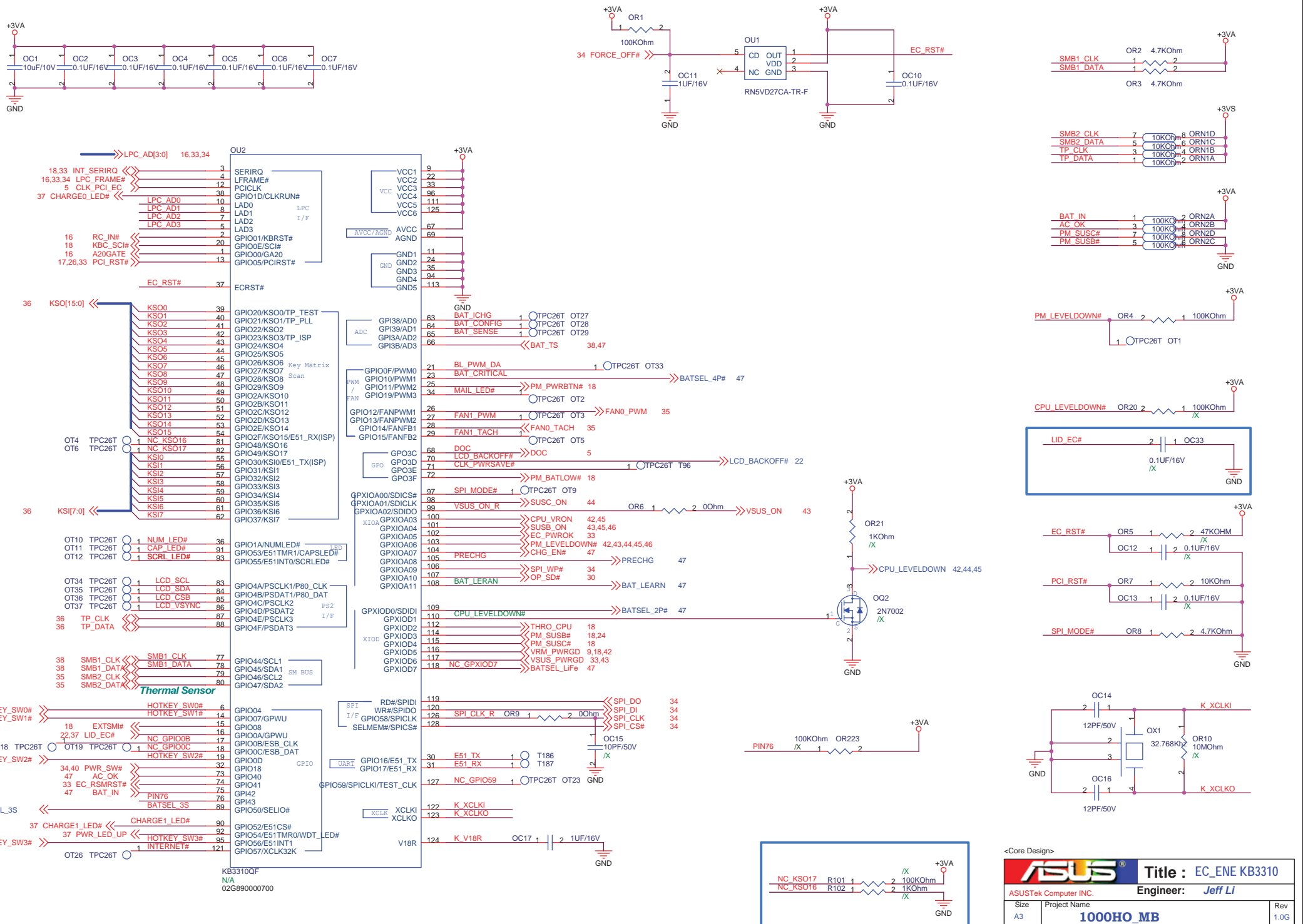
LINE_OUT use 12G140501060



MIC_JACK use 12G14040106Y



ASUS		Title : ALC269-2	
ASUSTek Computer Inc.		Engineer: Jeff Li	
Size A3	Project Name 1000HO_MB	Rev 1.0G	
Date: Friday, January 23, 2009	Sheet 31	of 47	



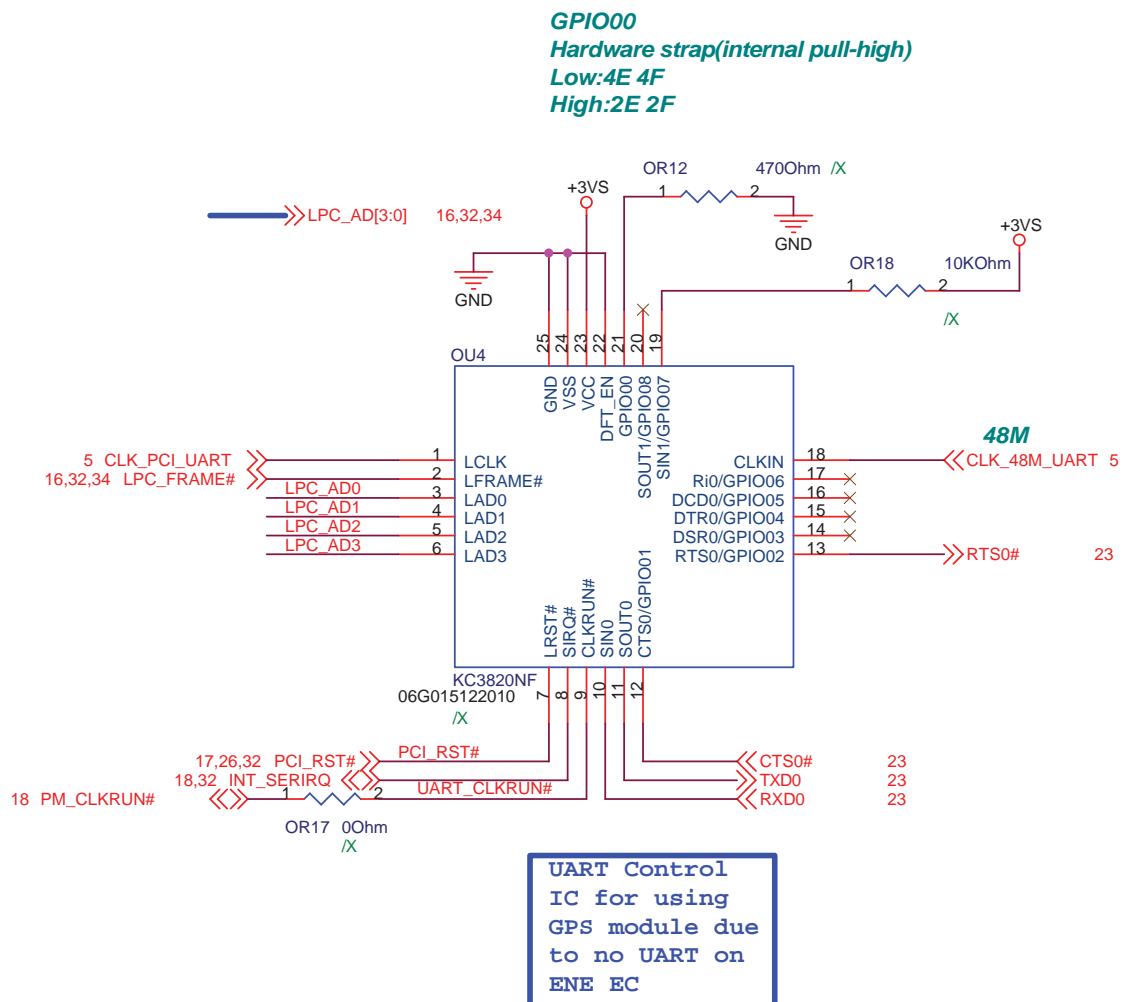
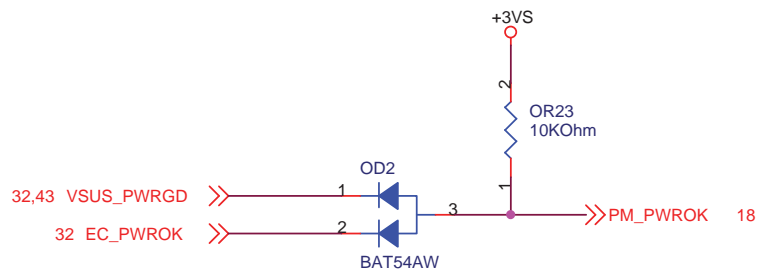
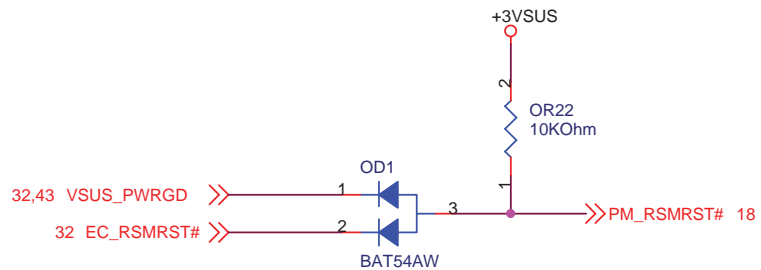
<Core Design>

ASUS Title : EC_ENE KB3310

ASUSTek Computer INC. Engineer: Jeff Li

Size	Project Name	Rev
A3	1000HO_MB	1.0G

Date: Friday, January 23, 2009 Sheet 32 of 47

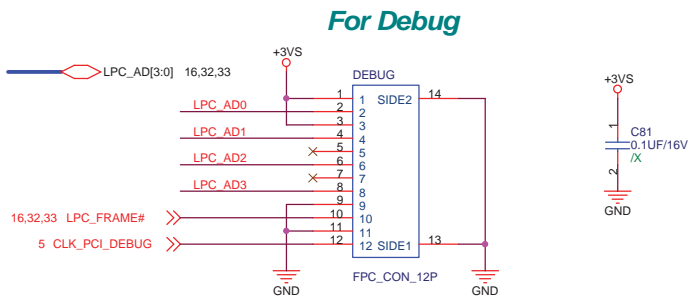
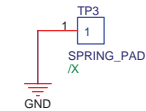
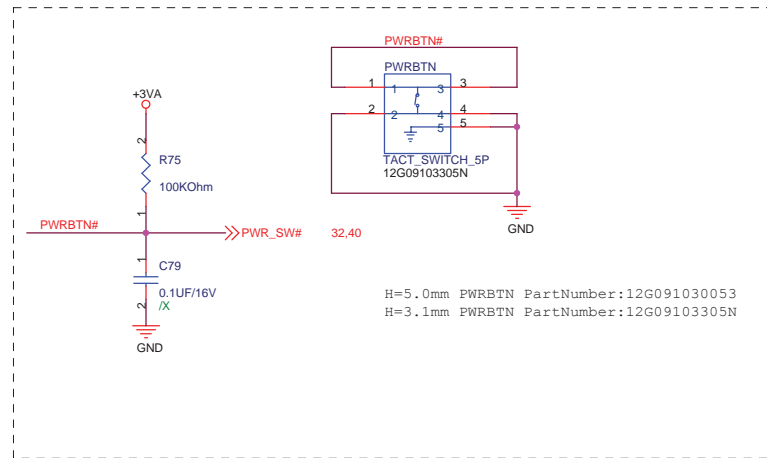
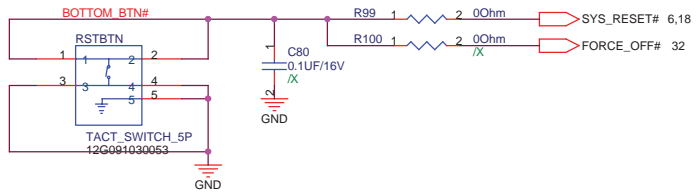


GPIO00
 Hardware strap(internal pull-high)
 Low:4E 4F
 High:2E 2F

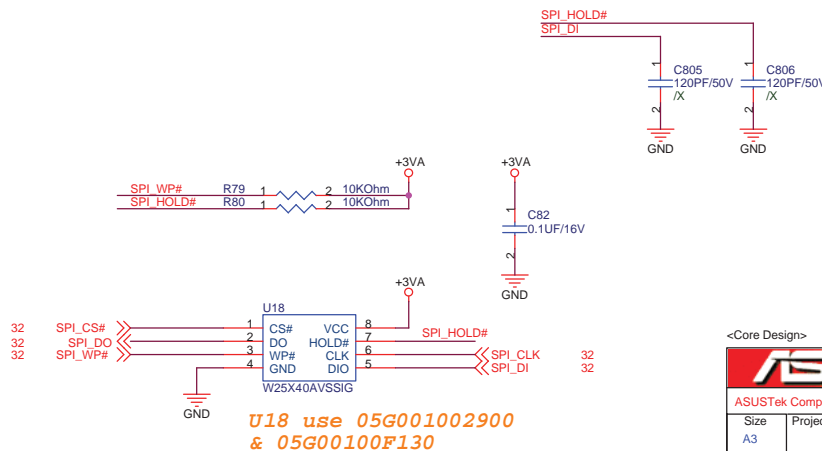
UART Control
 IC for using
 GPS module due
 to no UART on
 ENE EC

<Core Design>

		Title : EC_UART_KC3820	
ASUSTek Computer INC.		Engineer: Jeff Li	
Size A4	Project Name 1000HO_MB	Date Friday, January 23, 2009	Rev 1.0G
		Sheet	33 of 47



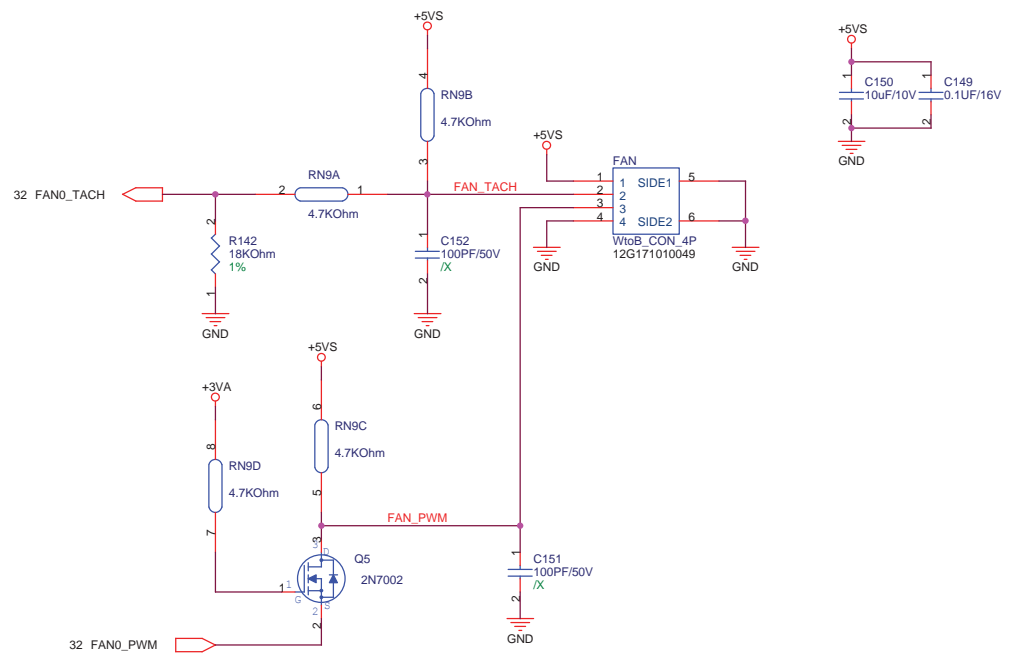
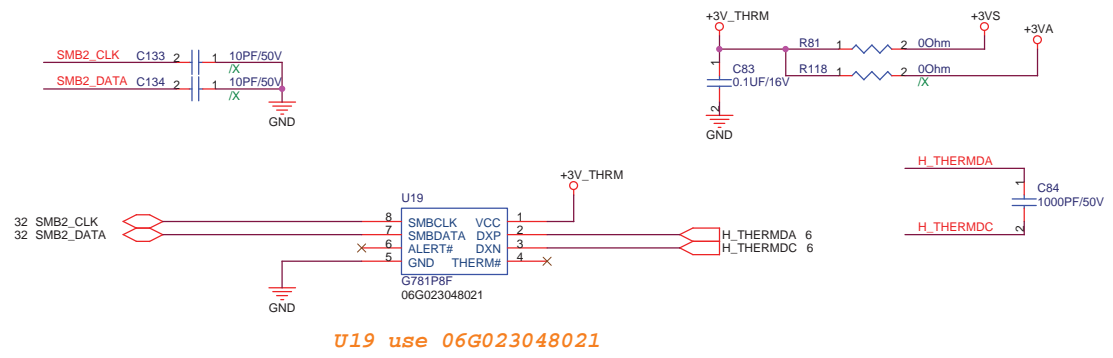
For Debug
 Debug Card cable use Z96 Touch Pad cable, P/N:
 14G124110126, 14G124110120, 14G124110121
 14G124110124, 14G124110125



U18 use 05G001002900
 & 05G00100F130

<Core Design>

ASUS		Title : Switch_SPI ROM_Debug	
ASUSTek Computer INC.		Engineer: Jeff Li	
Size	Project Name		Rev
A3	1000HO_MB		1.0G
Date: Friday, January 23, 2009	Sheet	34 of 52	

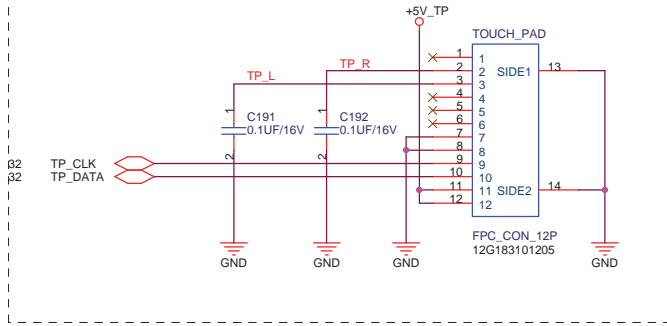


<Core Design>

ASUS		Title : Thermal Sensor_FAN	
ASUSTek Computer INC.		Engineer: <i>Jeff Li</i>	
Size	Project Name	Rev	
A3	1000HO_MB	1.0G	
Date: Friday, January 23, 2009	Sheet	35	of 52

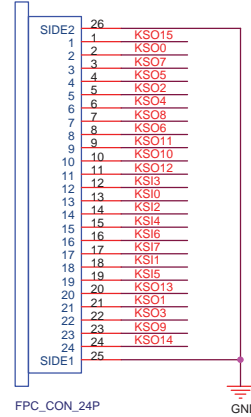
For Touch-Pad

P900 R1.0G

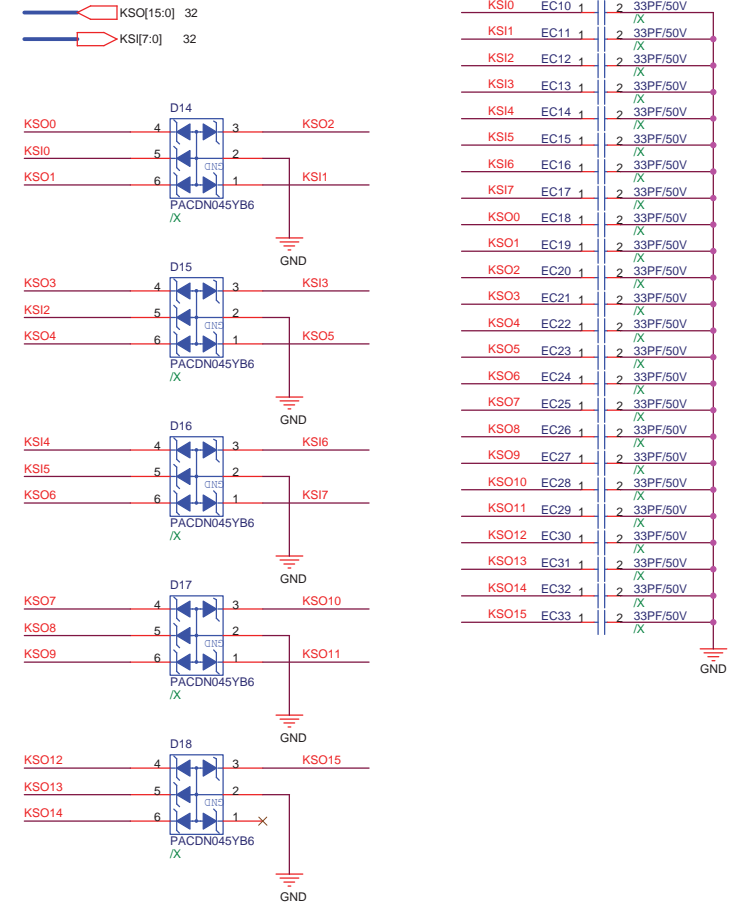
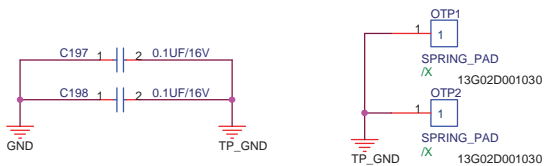
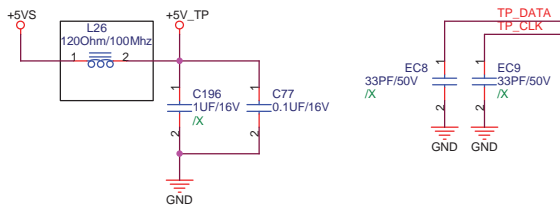
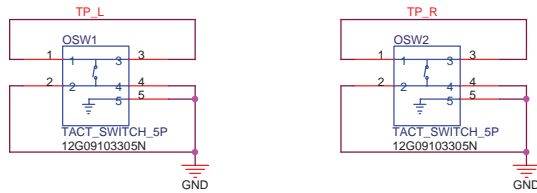


For Keyboard Connector

KB



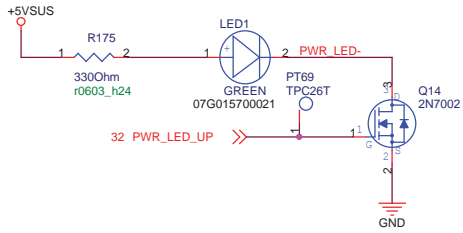
SW2, SW3 use 12G09103305N



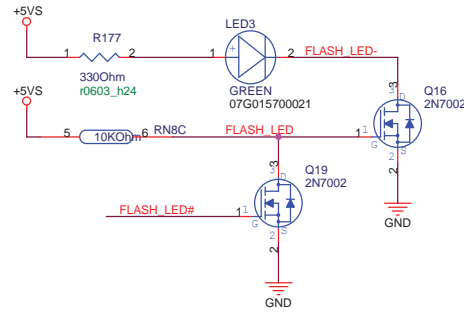
<Core Design>

ASUS		Title : KB_Touch Pad	
ASUSTek Computer INC.		Engineer: Jeff Li	
Size	Project Name		Rev
A3	1000HO_MB		1.0G
Date: Friday, January 23, 2009	Sheet	36	of 52

for POWER LED

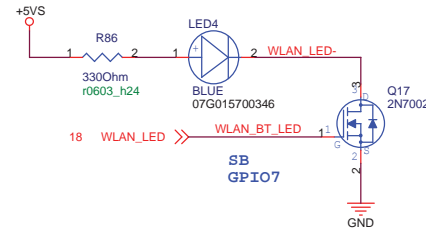


for FLASH LED

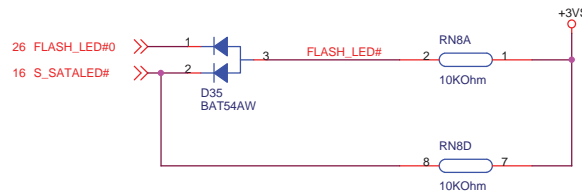
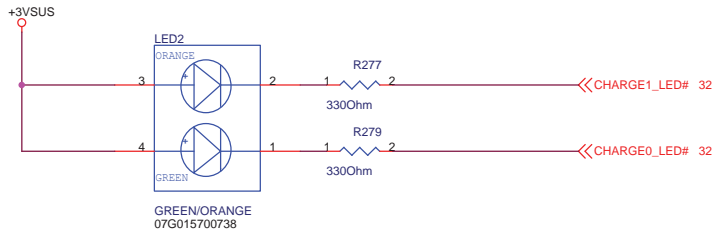


for WLAN/BlueTooth LED

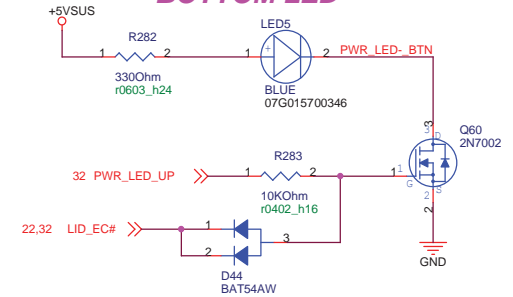
R86 use 4.7K OHm 10G213472003030



for CHARGE LED

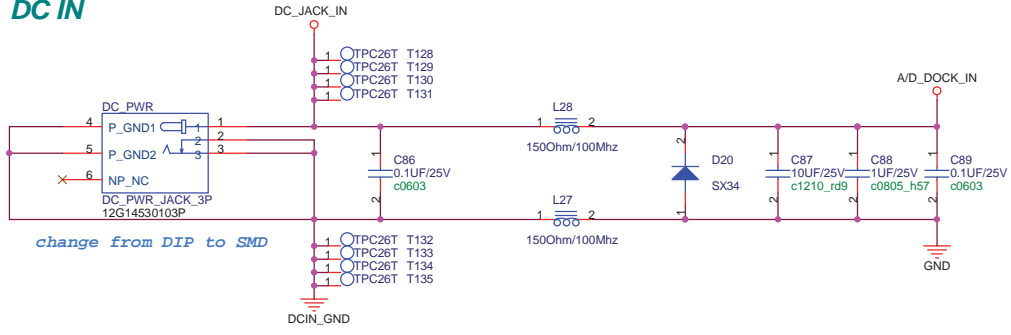


for POWER BOTTOM LED



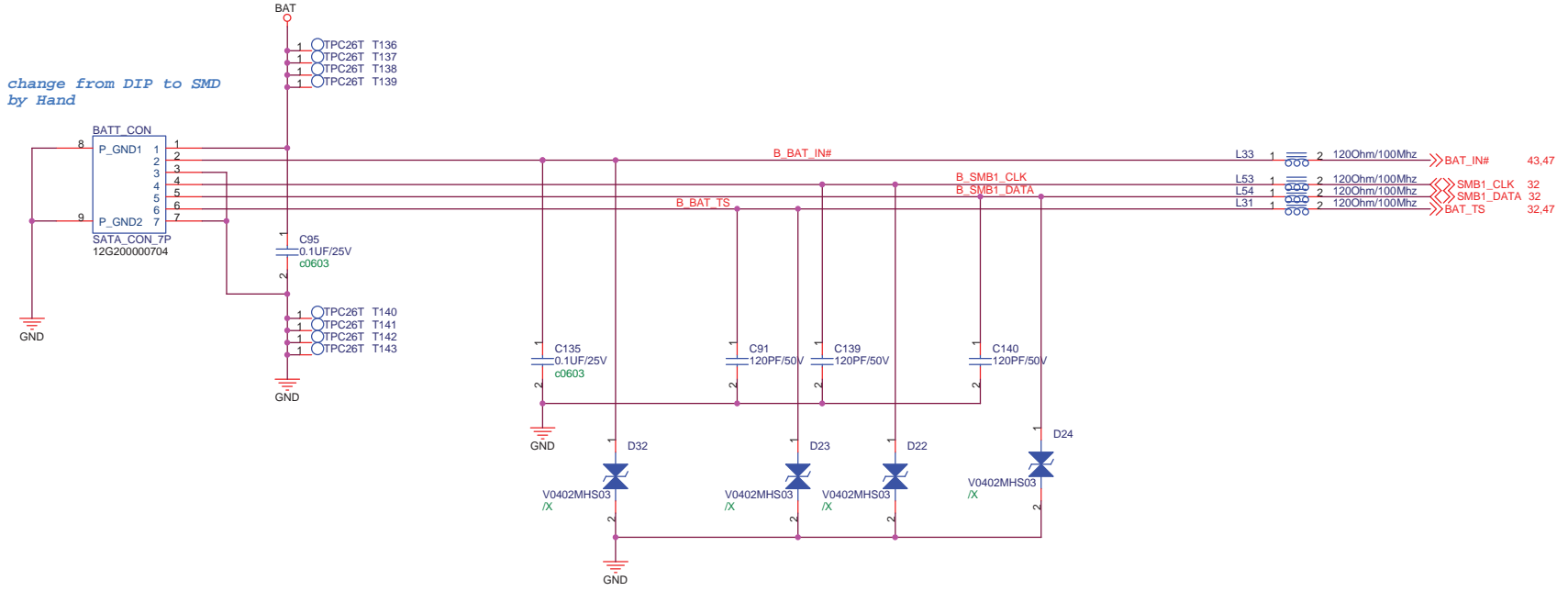
<Core Design>	
ASUS Title : LED	
ASUSTek Computer INC. Engineer: Kell_Huang	
Size A3	Project Name 1000H_MB
Date: Friday, January 23, 2009	Rev 1.1G
Sheet 37 of 47	

DC IN



change from DIP to SMD

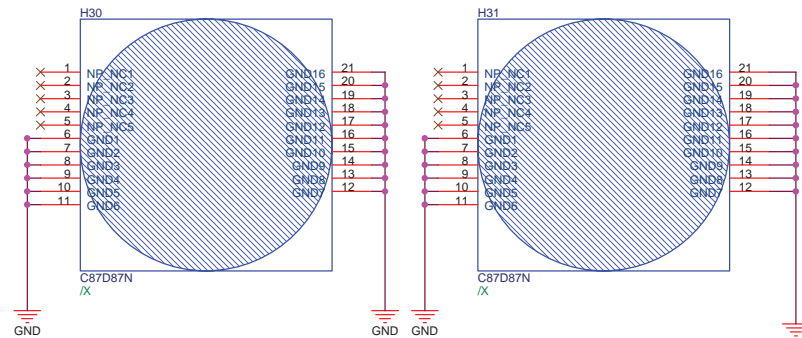
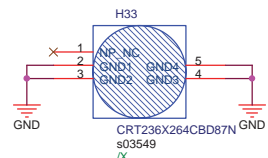
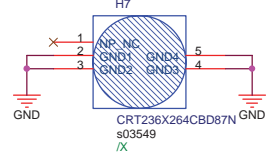
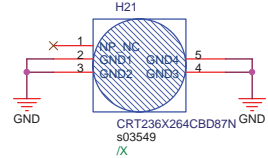
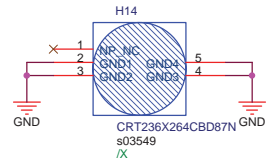
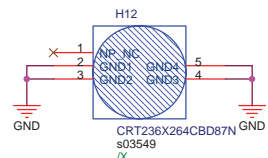
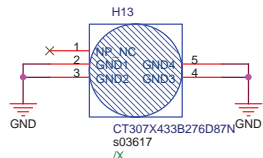
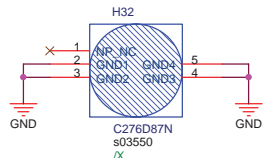
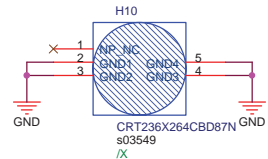
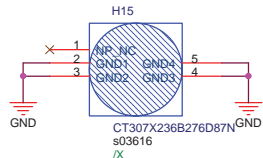
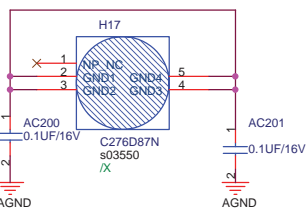
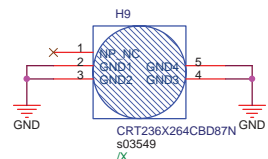
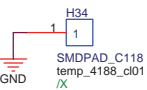
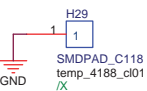
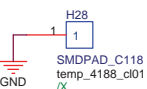
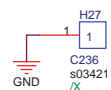
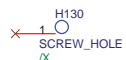
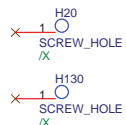
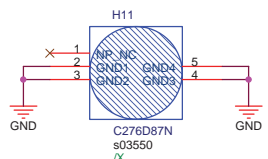
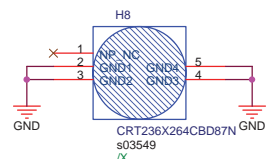
BAT IN



change from DIP to SMD by Hand

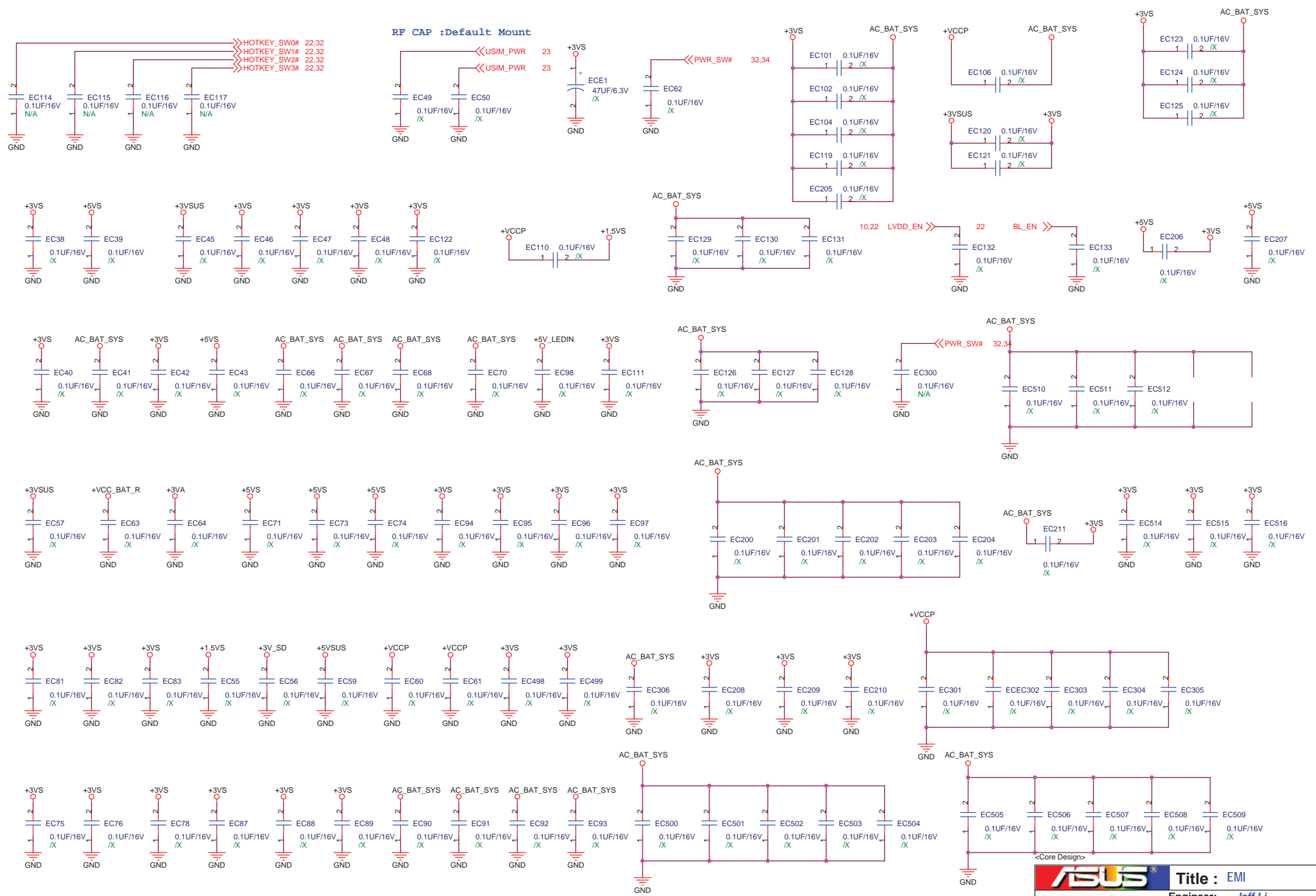
<Core Design>

ASUS		Title : PWR Jack	
ASUSTek Computer INC.		Engineer: <i>Jeff Li</i>	
Size	Project Name		Rev
A3	100HO_MB		1.0G
Date: Friday, January 23, 2009	Sheet	38 of 52	

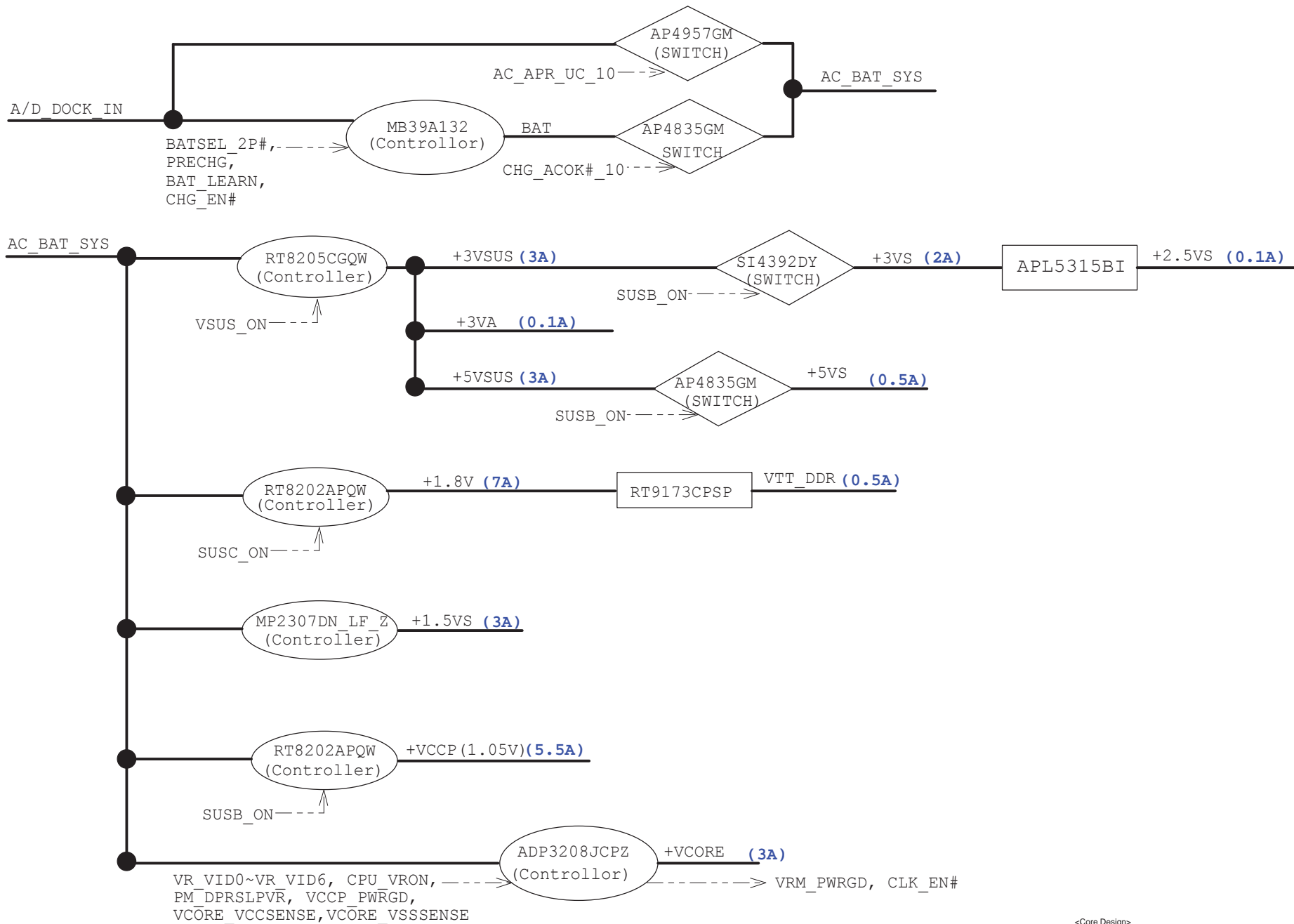


<Core Design>

ASUS		Title : Screw Hole	
ASUSTek Computer INC.		Engineer: <i>Kell_Huang</i>	
Size A3	Project Name 1000H_MB	Rev 1.1G	
Date: Friday, January 23, 2009	Sheet	39 of 47	

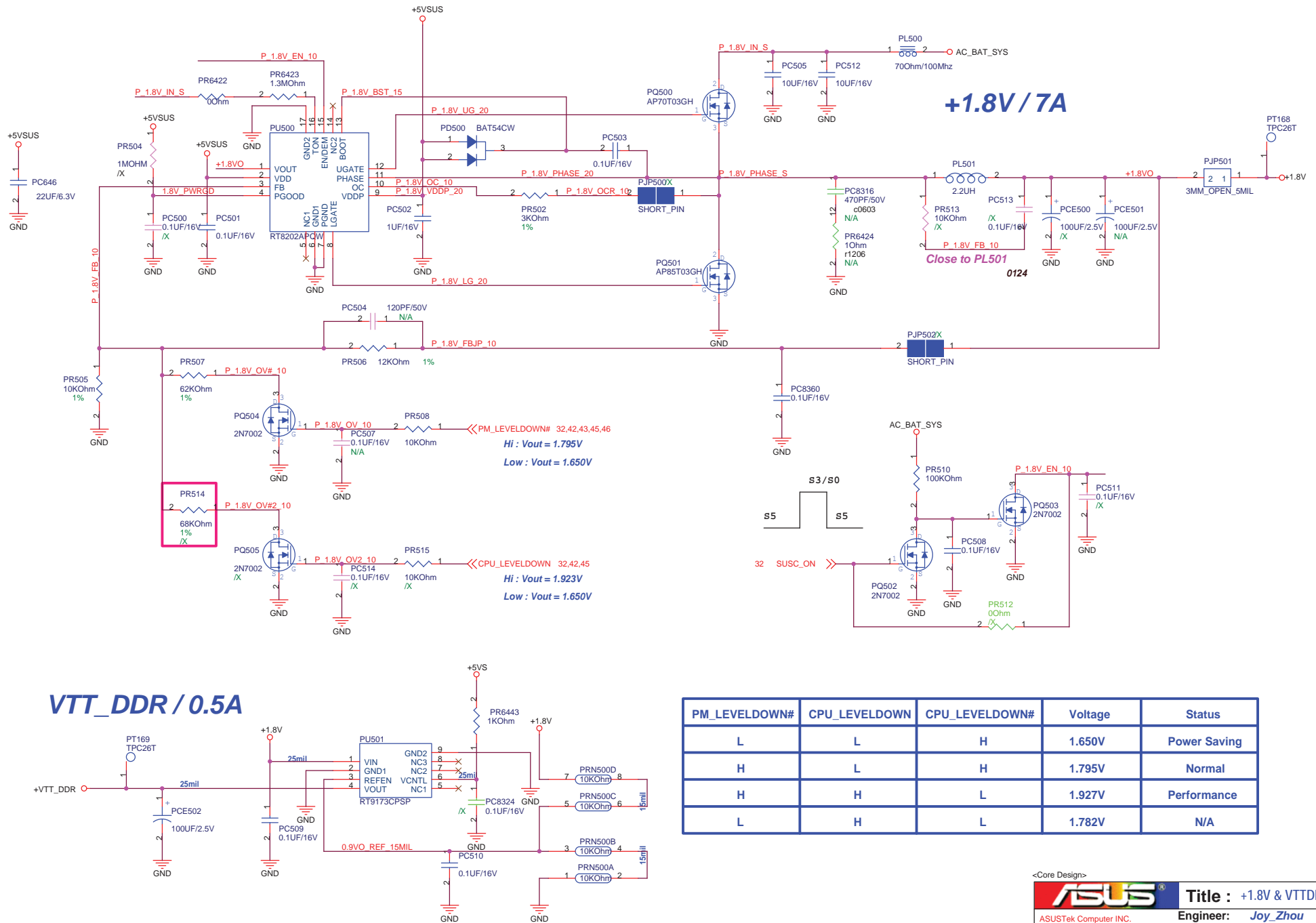


ASUS		Title : EMI	
ASUSTek Computer INC.		Engineer: Jeff Li	
Size A3	Project Name 100HO_MB	Rev 1.0G	
Date: Friday, January 23, 2009	Sheet	40 of 52	



<Core Design>

ASUS		Title : Power Flow	
ASUSTek Computer INC.		Engineer: Joy_Zhou	
Size	Project Name	Rev	
A3	1000H_MB	1.1G	
Date: Friday, January 23, 2009	Sheet 41 of 47		



PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	1.650V	Power Saving
H	L	H	1.795V	Normal
H	H	L	1.927V	Performance
L	H	L	1.782V	N/A

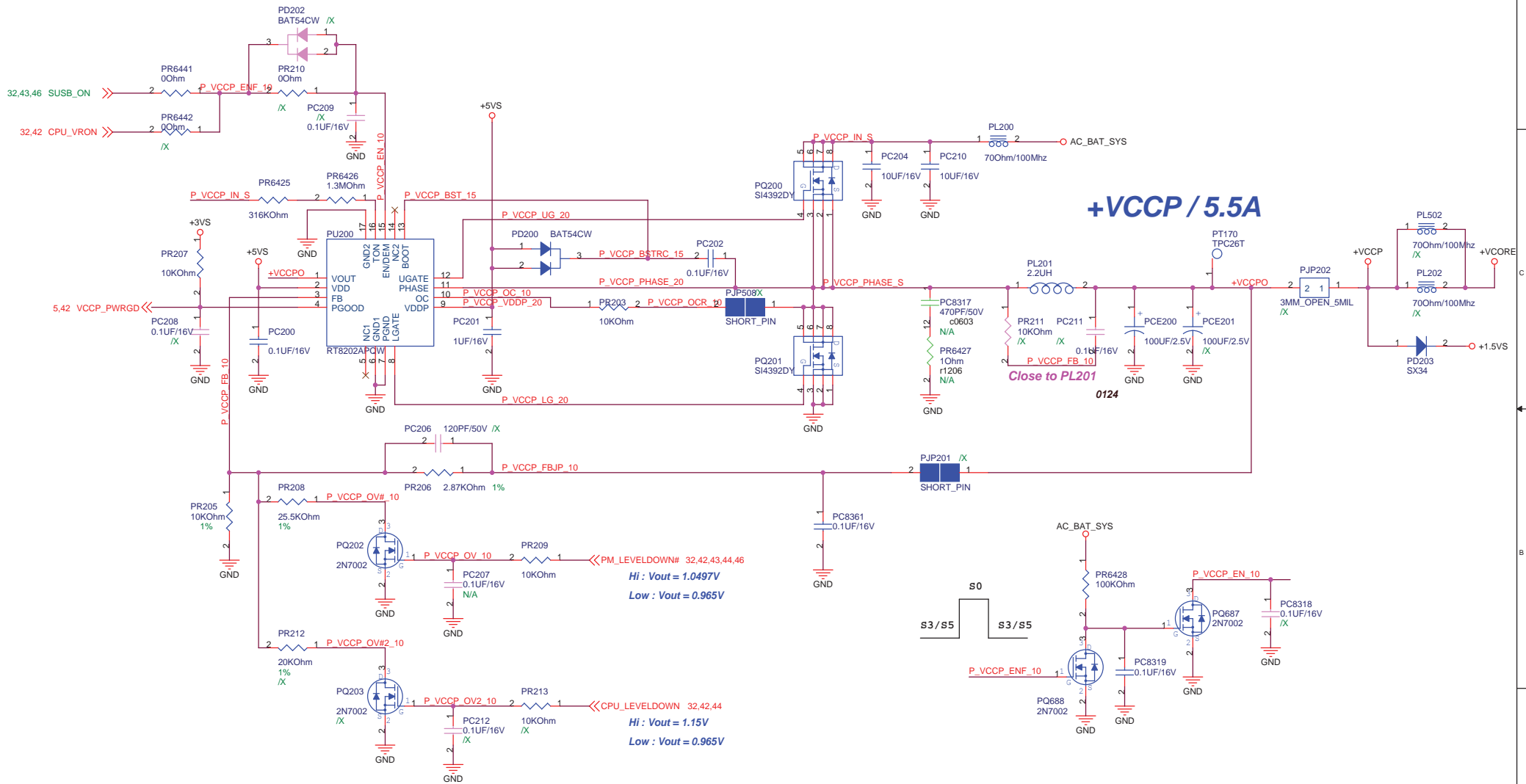
<Core Design>

ASUS Title : +1.8V & VTTDDR

ASUSTek Computer INC. Engineer: Joy_Zhou

Size	Project Name	Rev
A3	1000H_MB	1.1G

Date: Friday, January 23, 2009 Sheet 44 of 47

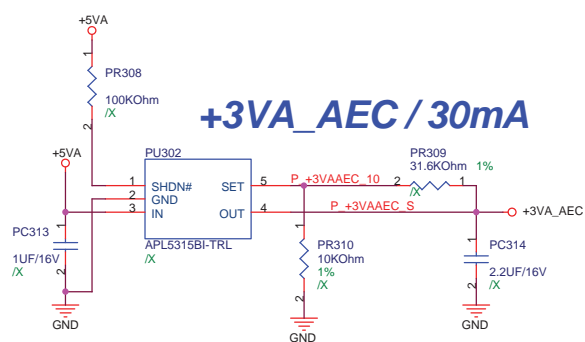
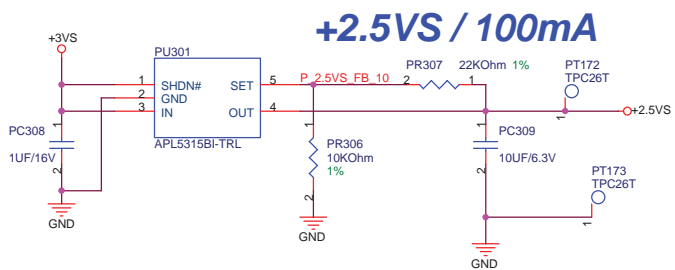
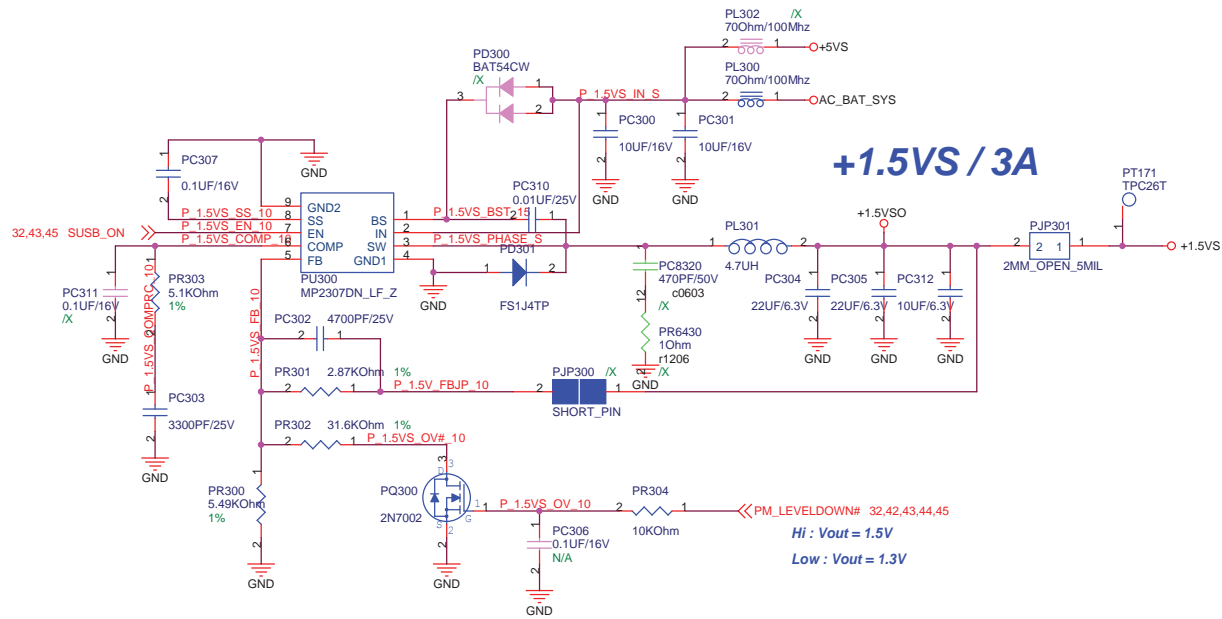


PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	0.965V	Power Saving
H	L	H	1.048V	Normal
H	H	L	1.157V	Performance
L	H	L	1.072V	N/A

<Core Design>

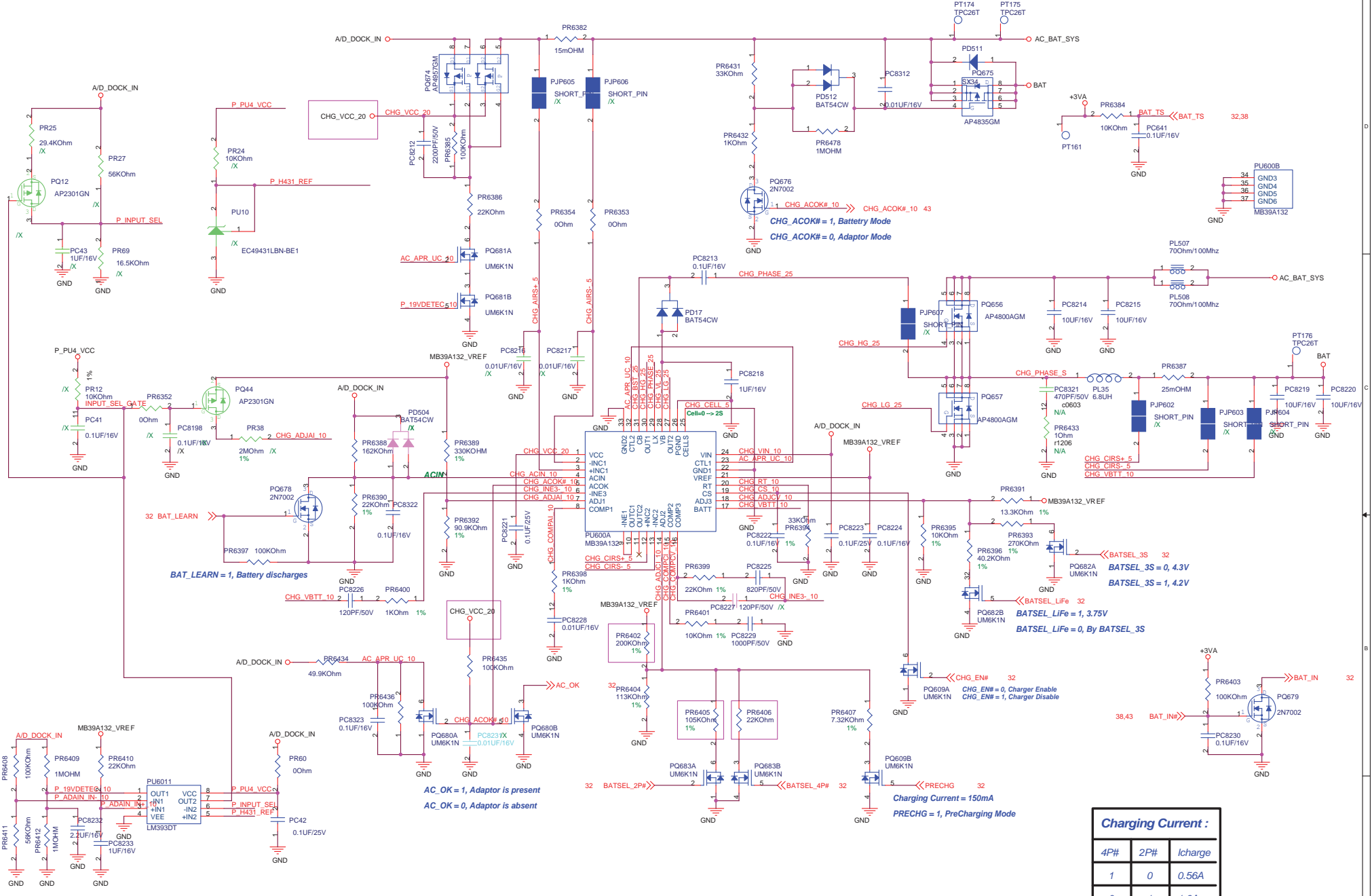
Title : VCCP
Engineer: Joy_Zhou

ASUSTek Computer INC.
 Size: A3 Project Name: **1000H_MB** Rev: 1.1G
 Date: Friday, January 23, 2009 Sheet: 45 of 47



<Core Design>

ASUS		Title : +1.5VS & +2.5VS	
ASUSTek Computer INC.		Engineer: Joy_Zhou	
Size	Project Name	Rev	
A3	1000H_MB	1.1G	
Date: Friday, January 23, 2009	Sheet	46	of 47



Battery Charging Voltage :
 $V_{adj3} > 4.1V \implies V_{bat} = 4.2V / \text{cell}$
 $2.2V > V_{adj3} > 1.1V \implies V_{bat} = 2 * V_{adj3}$

Battery Charging Current :
 $4.4V > V_{adj2} > 0V \implies I_{chg} = (V_{adj2} - 0.075) / (25 * R_s)$

Input Adaptor Max. Current Limit :
 $I_{limit_current} = (V_{adj1} - 0.075) / (25 * R_s)$

Pre-Charging Mode :
 Precharging current = 150mA
 $V_{adj2} = 168.75mV$

Adaptor Max. Current :
 $PR600 = 235.8K; I_{limit} = 2.170A; 20.615W (9.5V/22W)$
 $PR600 = 185.3K; I_{limit} = 2.677A; 32.124W (12V/36W)$

ACIN Threshold = 1.25V
 Adaptor > 8.63V, System Powered by Adaptor
 Adaptor < 8.63V, System Powered by Battery

Prevent Input from 19V :
 Adaptor > 13.06V, PQ603B Turn-off
 Adaptor < 13.06V, PQ603B Turn-on

Battery Cell Selection :
 $BAT_ID = 1, 2 \text{ Cells}; V_{adj2} = 0.998V \implies I_{charge} = 1.477A$
 $BAT_ID = 0, 4/6 \text{ Cells}; V_{adj2} = 1.648V \implies I_{charge} = 2.517A$

VREF = 5.0V
 $f_{osc}(KHz) = 17000 / RT (KOhm)$
Soft start: $t_s(s) = 0.13 * CS(uF)$

VTH of -IN1: $5V / 62 * (100+62) = 13.06V$

VTH of ACIN: $1.25V / 25 * (185+25) = 10.5V$
 Change PR607 and PR608 value

Charging Current :

4P#	2P#	Icharge
1	0	0.56A
0	1	1.6A
0	0	2.8A

<Core Design>

ASUS Title : Charger


ASUSTek Computer INC. Engineer: Joy Zhou

Size	Project Name	Rev
Custom	1000H MB	1.1G

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<Core Design>

		Title : Note	
ASUSTek Computer INC.		Engineer: KingCa_Jin	
Size	Project Name		Rev
A3	1000HE_MB		1.0G
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