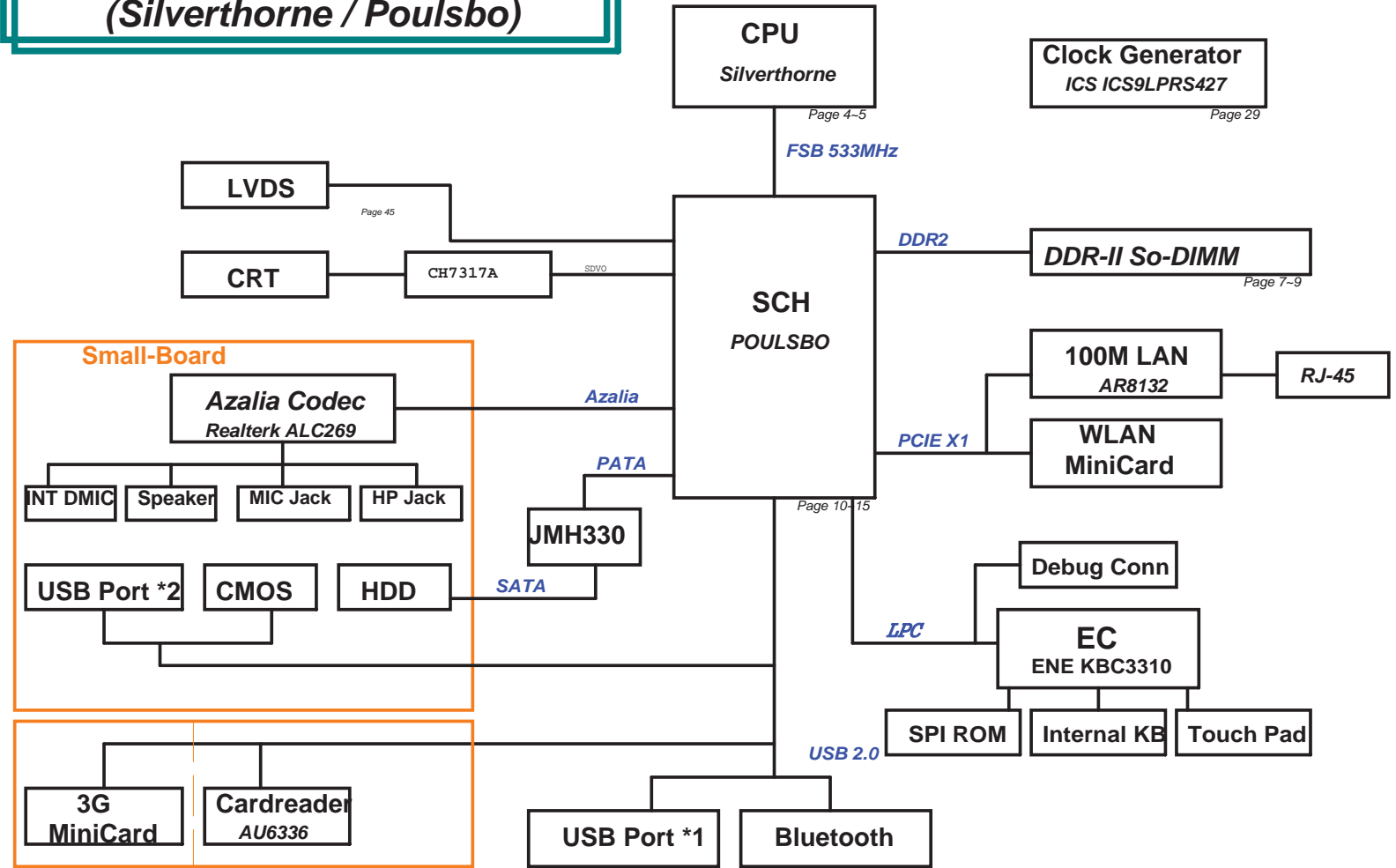


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- 04_Power Sequense DC
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- 28_RJ45
- 29_Small brd Conn
- 30_PATA TO SATA
- 31_USB Port
- 32_EC_ENE KB3310
- 33_SPI ROM_Debug Conn
- 34_Reset Map
- 35_KB_Touch Pad
- 36_
- 37_Discharge
- 38_PWR Jack
- 39_Screw Hole
- 40_EMI
- 41_Power Flow
- 42_Vcore
- 43_Power System
- 44_Power_+1.8V & VTDDR
- 45_Power_VCCP
- 46_Power_+1.5VS & +2.5VS
- 47_Charger
- 48_Power_Load Switch
- 49_Power Latch
- 50_HISTORY

1101HA Block Diagram (Silverthorne / Poulsbo)



SCH GPIO SETTING

Pin	Pin Name	Connect to	Type	Power Well	S3	S4/ S5	Input/Output Set
U41	GPIO_SUS0	PM_LEVELDOWN#	I/O CMOS3.3	Sus	VIX-unknown	OFF	Output
N43	GPIO_SUS1	CPU_LEVELDOWN	I/O CMOS3.3	Sus	VIX-unknown	OFF	Output
N45	GPIO_SUS2	PM_PWRBTN#	I/O CMOS3.3	Sus	VIX-unknown	OFF	Input
R41	GPIO_SUS3/ USBCC	+VCCP_OV0	I/O CMOS3.3	Sus	VIX-unknown	OFF	output
G29	GPIO0	Strap CMC/ BT_Disable	I/O CMOS3.3	Core	OFF	OFF	Input
K30	GPIO1	CARD_READER_EN#	I/O CMOS3.3	Core	OFF	OFF	Output
F34	GPIO2	SIMCARD_IN#	I/O CMOS3.3	Core	OFF	OFF	Input
G33	GPIO3	Strap CMC	I/O CMOS3.3	Core	OFF	OFF	Input
K36	GPIO4	3GLAN_OFF	I/O CMOS3.3	Core	OFF	OFF	Output
H36	GPIO5	MINICARD_EN#	I/O CMOS3.3	Core	OFF	OFF	Output
F36	GPIO6	DDR_MEM_CONFIG	I/O CMOS3.3	Core	OFF	OFF	Input
J31	GPIO7/ SLPIOVR#	SLPIOVR#	I/O CMOS3.3	Core	OFF	OFF	Output
H34	GPIO8/ PROCHOT#	CAMERA_EN	I/O CMOS3.3/ OD	Core	OFF	OFF	Output
K28	GPIO9/ EXTTS1#	WLAN_LED	I/O CMOS3.3	Core	OFF	OFF	Output

<Variant Name>

EC KB3310 GPIO SETTING

Pin	Pin Name	Signal Name	Type	Note
1	GPIO00/GA20	A20GATE	O	
2	GPIO01/KBRST#	RC_IN#	O	
6	GPIO04	HOTKEY_SW0#	I	Internal pull high
13	GPIO05/PCIRST#	BUF_RST#	I	
14	GPIO07	HOTKEY_SW1#(no use)		
15	GPIO08	EXT_SMI#	OD	10K pull high to +3VSB
16	GPIO0A	LID_EC_R#	I	Internal pull high
17	GPIO0B/ESB_CLK	PCB_ID0	I	
18	GPIO0C/ESB_DAT	PCB_ID1	I	
19	GPIO0D	LID_EC_L#(no use)	I	Internal pull high
20	GPIO0E/SC#	KBC_SC#	O	10K pull high to +3VSB
21	GPIO0F/PWM0	BL_PWM_DA	O	
23	GPIO10/PWM1	BATSEL#	I	Battery critical capacity
25	GPIO11/PWM2	PM_PWRBTN#	OD	Internal pull high in ICH
26	GPIO12/FANPWM1	FAN0_PWM	O	CPU Fan
27	GPIO13/FANPWM2	FAN1_PWM	O	VGA Fan
28	GPIO14/FANFB1	FAN0_TACH	I	CPU FanTach
29	GPIO15/FANFB2	FAN1_TACH	I	VGA FanTach
30	GPIO16/E51_TX	E51_TX	O	RS232 debug port
31	GPIO17/E51_RX	E51_RX	I	RS232 debug port
32	GPIO18	PWR_SW#	I	Internal pull high
34	GPIO19/PWM3	PS-ON	O	latch power
36	GPIO1A/NUMLED	NUM_LED#	O	
38	GPIO1D/CLKRUN#	LPC_CLKRUN#	O	
39	GPIO20/KSO0/TP_TEST	KSO0	O	
40	GPIO21/KSO1/TP_PLL	KSO1	O	
41	GPIO22/KSO2	KSO2	O	
42	GPIO23/KSO3	KSO3	O	
43	GPIO24/KSO4	KSO4	O	
44	GPIO25/KSO5	KSO5	O	
45	GPIO26/KSO6	KSO6	O	
46	GPIO27/KSO7	KSO7	O	
47	GPIO28/KSO8	KSO8	O	
48	GPIO29/KSO9	KSO9	O	
49	GPIO2A/KSO10	KSO10	O	
50	GPIO2B/KSO11	KSO11	O	
51	GPIO2C/KSO12	KSO12	O	
52	GPIO2D/KSO13	KSO13	O	
53	GPIO2E/KSO14	KSO14	O	
54	GPIO2F/KSO15	KSO15	O	
55	GPIO30/KSI0	KSI0	I	Internal pull high
56	GPIO31/KSI1	KSI1	I	Internal pull high
57	GPIO32/KSI2	KSI2	I	Internal pull high
58	GPIO33/KSI3	KSI3	I	Internal pull high
59	GPIO34/KSI4	KSI4	I	Internal pull high
60	GPIO35/KSI5	KSI5	I	Internal pull high
61	GPIO36/KSI6	KSI6	I	Internal pull high
62	GPIO37/KSI7	KSI7	I	Internal pull high
63	GPI38/AD0	BAT_A	I	
64	GPI39/AD1	BAT_B	I	
65	GPIO3A/AD2	BAT_C	I	
66	GPIO3B/AD3	BAT_D	I	
68	GPO3C/DA0	CHG_EN#	O	battery charger enabled

<http://hobi-elektronika.net>

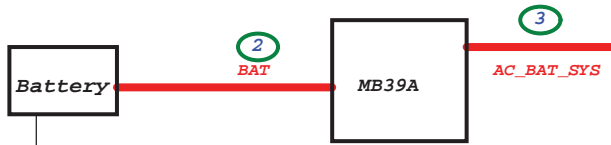
Pin	Pin Name	Signal Name	Type	Note
70	GPO3D/DA1	LCD_BACKOFF#	O	
71	GPO3E/DA2	THRO_CPU_VOLT#	O	
72	GPO3F/DA3	BAT_LL#	O	Battery Low Low
73	GPIO40	AC_OK	I	AC Adaptor Plug in
74	GPIO41	PM_RSMRST#	O	10K pull down to GND
75	GPI42	BAT_IN	I	Batt1 (Small/Internal): + present, 0 absent
76	GPI43	BAT2_IN	I	Batt2 (Small/Internal): + present, 0 absent
77	GPIO44/SCL1	SMB0_CLK	I/OD	4.7K pull high to +3VA_EC
78	GPIO45/SDA1	SMB0_DAT	I/OD	4.7K pull high to +3VA_EC
79	GPIO46/SCL2	SMB1_CLK	I/OD	10K pull high to +3V
80	GPIO47/SDA2	SMB1_DAT	I/OD	10K pull high to +3V
81	GPIO48/KSO16	KB_ID0	I	for KB type detection
82	GPIO49/KSO17	KB_ID1	I	for KB type detection
83	GPIO4A/PSCLK1	N.C.	O	
84	GPIO4B/PSDAT1	CRT_IN	I	
85	GPIO4C/PSCLK2	CRT_DACPWR_EN#	O	
86	GPIO4D/PSDAT2	CRTDAC_RST#	O	
87	GPIO4E/PSCLK3	TP_CLK	I/OD	10K pull high to +3V
88	GPIO4F/PSDAT3	TP_DAT	I/OD	10K pull high to +3V
89	GPIO50/SELIO#	CHG_LED_GREEN#	O	Green charger LED
90	GPIO52/E51_CS#	CHG_LED_UP#	O	Orange charger LED
91	GPIO53/CAPLED	CAP_LED#	O	
92	GPIO54	PWR_LED_UP	O	
93	GPIO55/SCRLLED	SCRL_LED#	O	
95	GPIO56	GS1_INT1(no use)	I	Internal pull high
97	GPX0A00/SDICS#	SPI_MODE#	O	4.7K pull down to GND
98	GPX0A01/SDICLK	SUSC_ON	O	
99	GPX0A02/SDIDO	VSUS_ON	O	
100	GPX0A03	CPU_VRON	O	
101	GPX0A04	SUSB_ON	O	
102	GPX0A05	CNT1_CHG#	O	batt1 (Big/External) charging enabled. Batt1 is discharging priority in AC mode.
103	GPX0A06	CNT1_DIS#	O	batt1 discharging enabled
104	GPX0A07	CNT2_CHG#	O	batt2 (Big/External) charging enabled. Batt2 is discharging priority in AC mode.
105	GPX0A08	CNT2_CHG#	O	batt2 discharging enabled
106	GPX0A09	SPI_WP#	O	
107	GPX0A10	OP_SD#	O	Audio OP
108	GPX0A11	BAT_LEARN	O	
109	GPXID0/SDIDI	PM_PWROK	O	Battery parallel, H:1P, L:2P-3P
110	GPXID1	RST#	O	
112	GPXID2	THRO_CPU	O	Active if CPU temperature over spec
114	GPXID3	PM_SLPRDY#	I	SLPRDY#, 100K pull down to GND
115	GPXID4	SLPMODE	I	SUSC#, 100K pull down to GND
116	GPXID5	VRM_PWRGD	I	Pull high to +3V
117	GPXID6	PM_RSTRDY#	I	
118	GPXID7	RSTWARN	O	
121	GPIO57	GS1_INT2(no use)	I	Internal pull high
126	GPIO58/SPICLK	SPI_CLK	O	
127	GPIO59/TEST_CLK	GS2_INT1(no use)	O	

EC KB3310 Other Pin SETTING

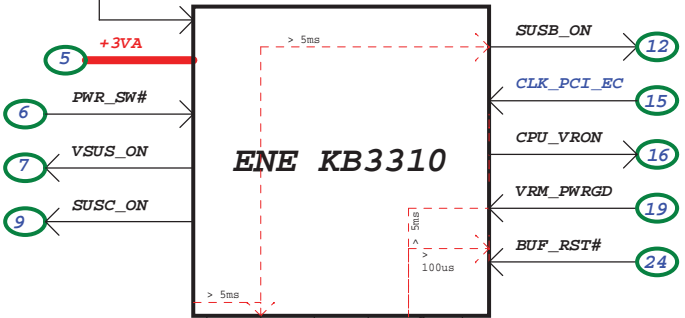
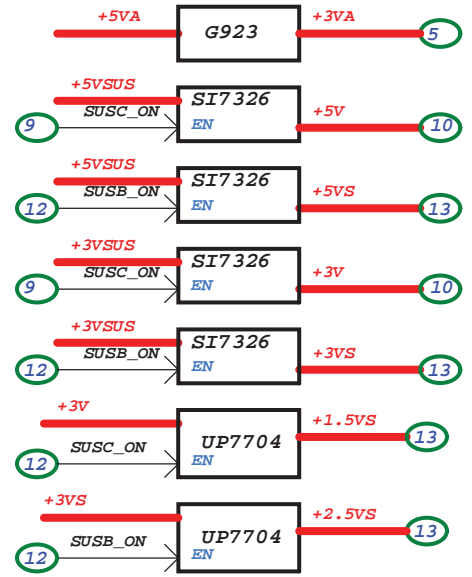
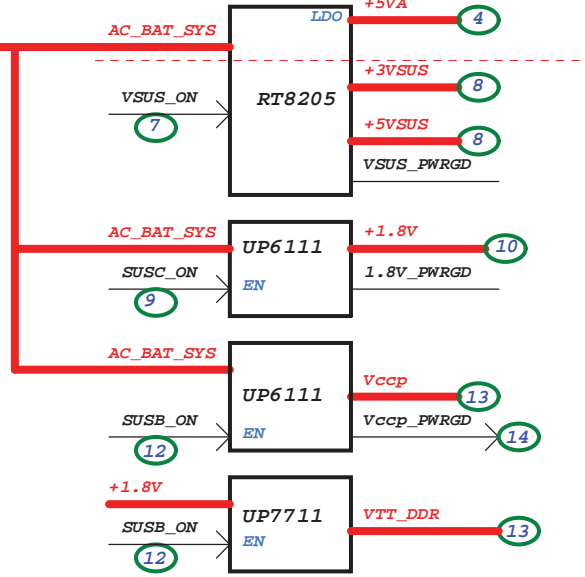
Pin	Pin Name	Signal Name	Type	Note
3	SERIRQ	INT_SERIRQ	I/OD	10K pull high to +3V
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCI_EC	I	
22	VCC	+3VA	P	
24	GND	GND	P	
33	VCC	+3VA	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	100K pull high to +3VA_EC
67	AVCC	+3VA_AEC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA	P	
111	VCC	+3VA	P	
113	GND	GND	P	
119	RD#/SPIDI	SPI_SO	I	
120	WR#/SPIDO	SPI_SI	O	
122	XCLKI	K_XCLKI	I	
123	XCLKO	K_XCLKO	O	
124	V18R	V18R	P	Reserved 1uF to GND
125	VCC	+3VA	P	
128	SPICS#/SELMEM#	SPI_CS#	O	

<Variant Name>

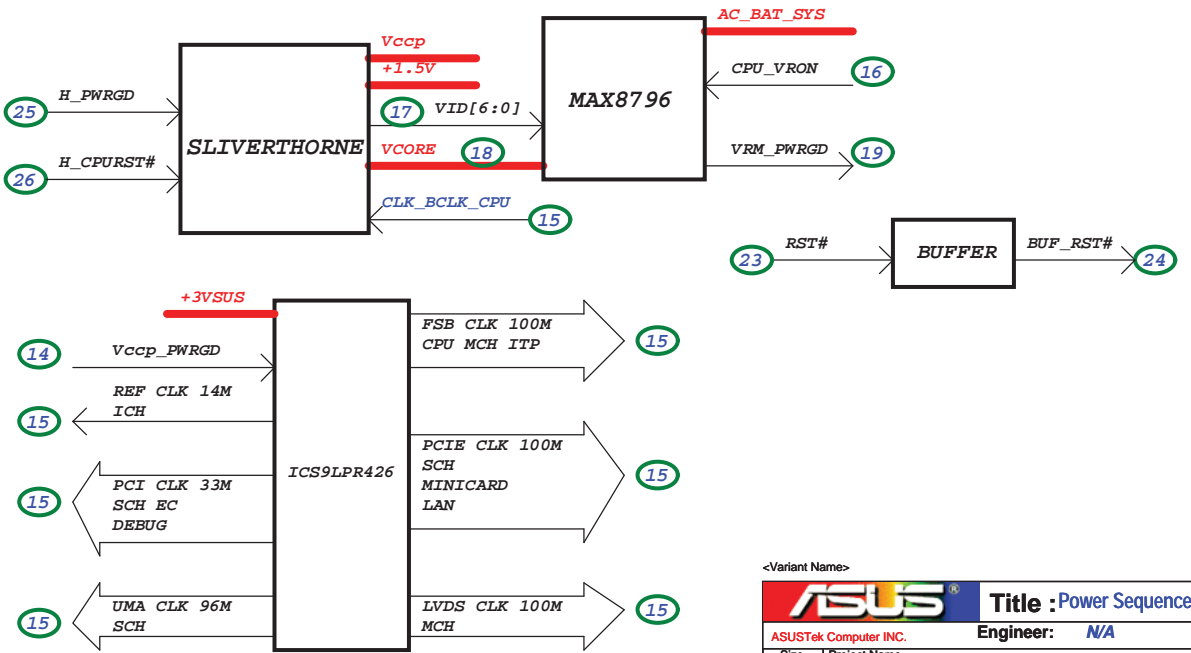
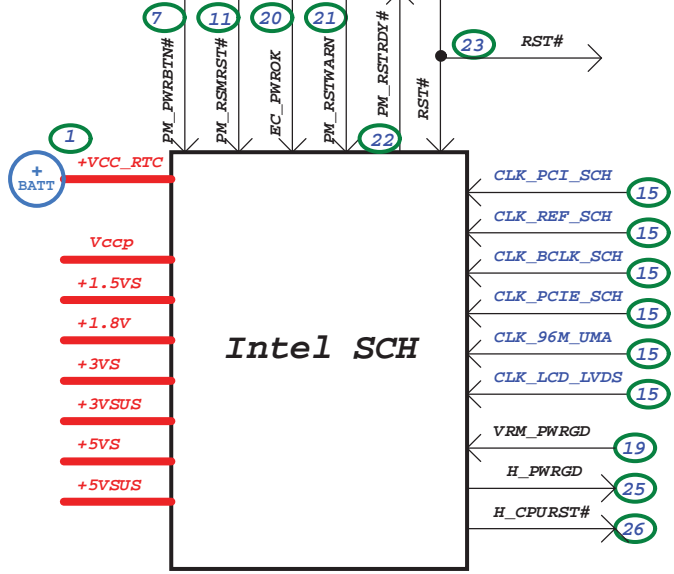
		Title : EC Pin Define	
ASUSTek Computer INC.		Engineer: N/A	
Size A3	Project Name 1101HA	Rev 1.2	
Date: Tuesday, July 21, 2009	Sheet 3 of 50		

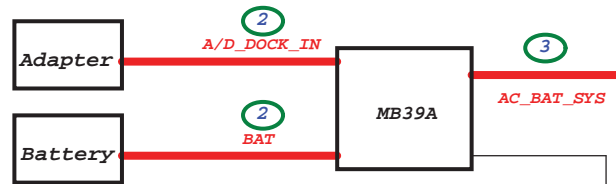


Signal	S0/S1	S3	S4/S5	Power
VSUS_ON	H	H	Adapter H Battery L	VSB
SUSB_ON	H	L	L	Main
SUSC_ON	H	H	L	DUAL

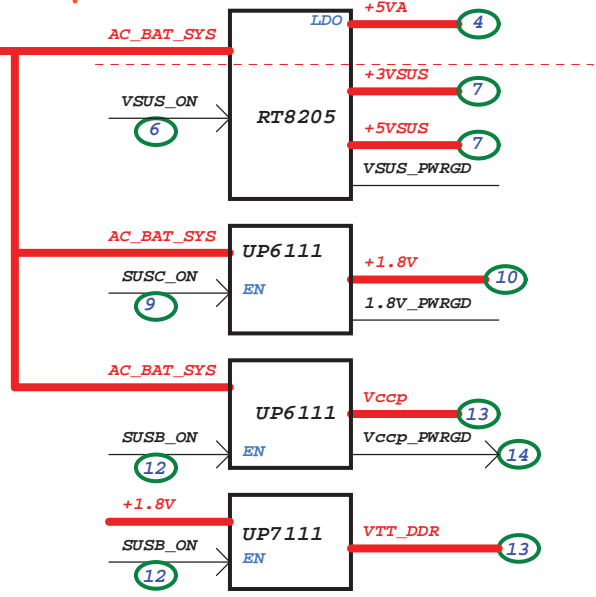
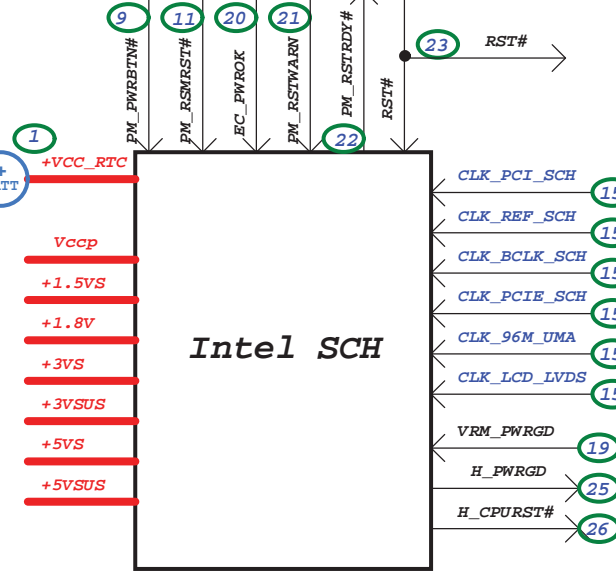
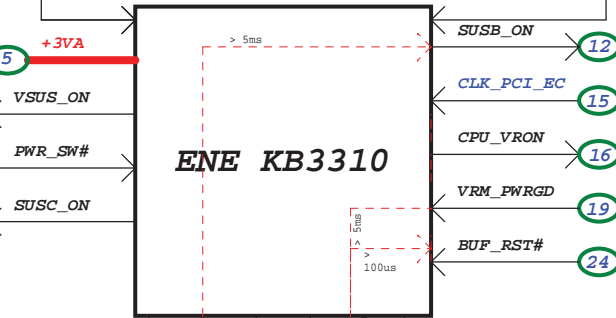


	+5VA	+3VA	+3VSUS	+5VSUS	+1.8V	+3V	+5V	VTT_DDR	Vccp	+1.5V	+3VS	+5VS	+2.5VS
S0/S1	V	V	V	V	V	V	V	V	V	V	V	V	V
S3	V	V	V	V	V	V	V	--	--	--	--	--	--
S4/S5	V	V	--	--	--	--	--	--	--	--	--	--	--

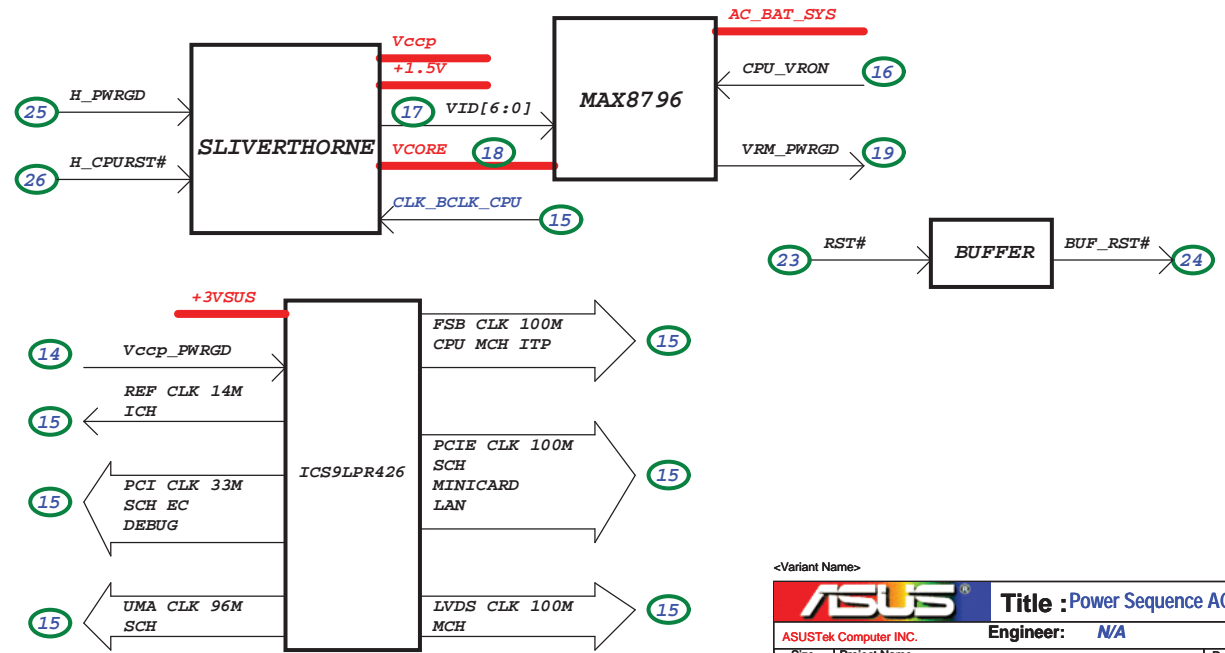
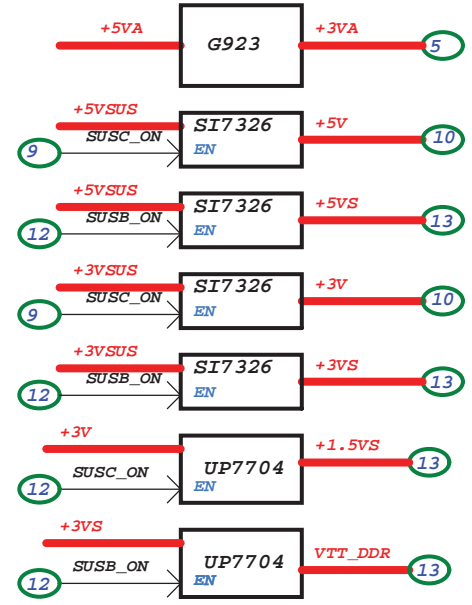




Signal	S0/S1	S3	S4/S5	Power
VSUS_ON	H	H	Adapter	H
			Battery	L
SUSB_ON	H	L	L	Main
SUSC_ON	H	H	L	DUAL



	+5VA	+3VA	+3VSUS	+5VSUS	+1.8V	+3V	+5V	VTT_DDR	Vccp	+1.5VS	+3VS	+5VS	+2.5VS
S0/S1	V	V	V	V	V	V	V	V	V	V	V	V	V
S3	V	V	V	V	V	V	V	--	--	--	--	--	--
S4/S5	V	V	V	V	--	--	--	--	--	--	--	--	--



S4/S5 to S0(Adapter Mode)

This sequence will occur whenever the system is in S4/S5 and the EC initiates a sleep exit sequence from S4/S5 to S0.

Initial EC state: VSUS_ON=0, SUSB_ON=0, SUSC_ON=0, A20GA=X, KBRST=X, CPU_VRON=0, ICH_PWROK=0, RSTWARN=0, and PM_RSMRST#=0, RESET#=0.

- 1.Waiting for AC_OK until adaptor power is good, then
- 2.At least **5mS** after AC_OK is asserted, EC asserts VSUS_ON to enable VSUS power.
- 3.At least **20mS** after VSUS power is stable, waiting for PWR_SW# until user is pressed. (Or waiting for SCH deasserted SLPRDY#, too?)
- 4.EC asserts RSTWARN.
- 5.SUSC_ON is asserted at least 20mS (de-bounce) after receiving PWR_SW#.
- 6.PM_RSMRST# is deasserted at least **5mS** after SUSC power is stable.
- 7.At least **5mS** after PM_RSMRST# is deasserted, SUSB_ON is enabled.
- 8.CPU_VRON is deasserted at least **100mS** after SUSB power is stable.
- 9.Waiting for CPUPWR_GD (VRM_PWRGD) until CPU_VRON power is stable.
- 10.At least **10mS** after receiving CPUPWR_GD, PM_PWROK is asserted, and then deasserts RSTWARN.
- 11.Waiting for RSTRDY# until deasserted by SCH.
- 12.RESET# can be deasserted at lease **100uS** after PM_PWROK is asserted.

S4/S5 to S0(Battery Mode)

This sequence will occur whenever the system is in S4/S5 and the EC initiates a sleep exit sequence from S4/S5 to S0.

Initial EC state: VSUS_ON=0, SUSB_ON=0, SUSC_ON=0, A20GA=X, KBRST=X, CPU_VRON=0, ICH_PWROK=0, RSTWARN=0, and PM_RSMRST#=0, RESET#=0.

- 1.Waiting for BAT_IN until battery power is good, then
- 2.Waiting for PWR_SW# until user is pressed.
- 3.EC asserts VSUS_ON to enable VSUS power.
- 4.At least **20mS** after VSUS power is stable.
- 5.EC asserts RSTWARN.
- 6.SUSC_ON is asserted at least 20mS (de-bounce) after receiving PWR_SW#.
- 7.PM_RSMRST# is deasserted at least 5mS after SUSC power is stable.
- 8.At least 5mS after PM_RSMRST# is deasserted, SUSB_ON is enabled.
- 9.CPU_VRON is deasserted at least 10mS after SUSB power is stable.
- 10.Waiting for CPUPWR_GD (VRM_PWRGD) until CPU_VRON power is stable.
- 11.At least 10mS after receiving CPUPWR_GD, PM_PWROK is asserted, and then deasserts RSTWARN.
- 12.Waiting for RSTRDY# until deasserted by SCH.
- 13.RESET# can be deasserted at lease 100uS after ICH_PWROK is asserted.

S0 to S3/S4/S5

This sequence will occur when system entry to sleep states, or all power planes are shut down.

Initial EC state: VSUS_ON=1, SUSB_ON=1, SUSC_ON=1, CPU_VRON=1, ICH_PWROK=1, and PM_RSMRST#=1, RESET#=1, RSTWARN=0, PM_PWRBTN#=1.

- 1.Waiting for PWR_SW# until user is pressed (go to 2), or waiting for SLPRDY# is asserted (go to 3).
- 2.At least **20mS** after PWR_SW# is asserted, EC asserts PM_PWRBTN# (50mS width) to SCH.
- 3.Waiting for SLPRDY# until has been asserted.
- 4.EC asserts RSTWARN to SCH to begin internal sequence.
- 5.SCH asserts RSTRDY# to EC to indicate all outstanding transactions are completed.
- 6.EC asserts RESET# after detecting RSTRDY# asserted.
- 7.EC deasserts ICH_PWROK.
- 8.EC deasserts SUSB_ON and CPU_VRON to turn off power planes.

This completes the entry to S3 (SLPMODE=1).

If SLPMODE=0, this indicates S4/S5 was the desired state, EC takes additional actions:

- 9.EC asserts PM_RSMRST#.
- 10.EC deasserts SUSC_ON to turn off the other power planes.
- 11.EC deasserts VSUS_ON if in battery mode.
- 12.EC deasserts RSTWARN to save more power.

Power Sequence Description: S3 to S0

This sequence will occur in S3, and wake event is detected by EC or SCH.

Initial EC state: SUSB_ON=0, CPU_VRON=0, ICH_PWROK=0, PM_RSMRST#=1, PM_PWRBTN#=1, and VSUS_ON=1, RSTWARN=1, SUSC_ON=1, RESET#=0.

- 1.For internal wake event, SCH deasserts SLPRDY# to EC, than 4.
- 2.For external wake event (PWR_SW#, keyboard wake up), then
- 3.EC asserts PM_PWRBTN# at least **50mS** to wake SCH, and waiting for SLPRDY# until SCH deasserted.
- 4.EC asserts SUSB_ON to enable SUSB power.
- 5.CPU_VRON is deasserted at least **100mS** after SUSB power is stable.
- 6.Waiting for CPUPWR_GD (VRM_PWRGD) until CPU_VRON power is stable.
- 7.At least **5mS** after receiving CPUPWR_GD, ICH_PWROK is asserted.
- 8.Deasserts RSTWARN after ICH_PWROK is asserted.
- 9.RESET# can be deasserted **100uS** after RSTWARN is deasserted.

Warm Reset (SLPMODE=1)

The warm reset sequence results in reset without remove any power supplies.

Initial EC state: SUSB_ON=1, CPU_VRON=1, ICH_PWROK=1, PM_RSMRST#=1, PM_PWRBTN#=1, and VSUS_ON=1, RSTWARN=1, SUSC_ON=1, RESET#=1.

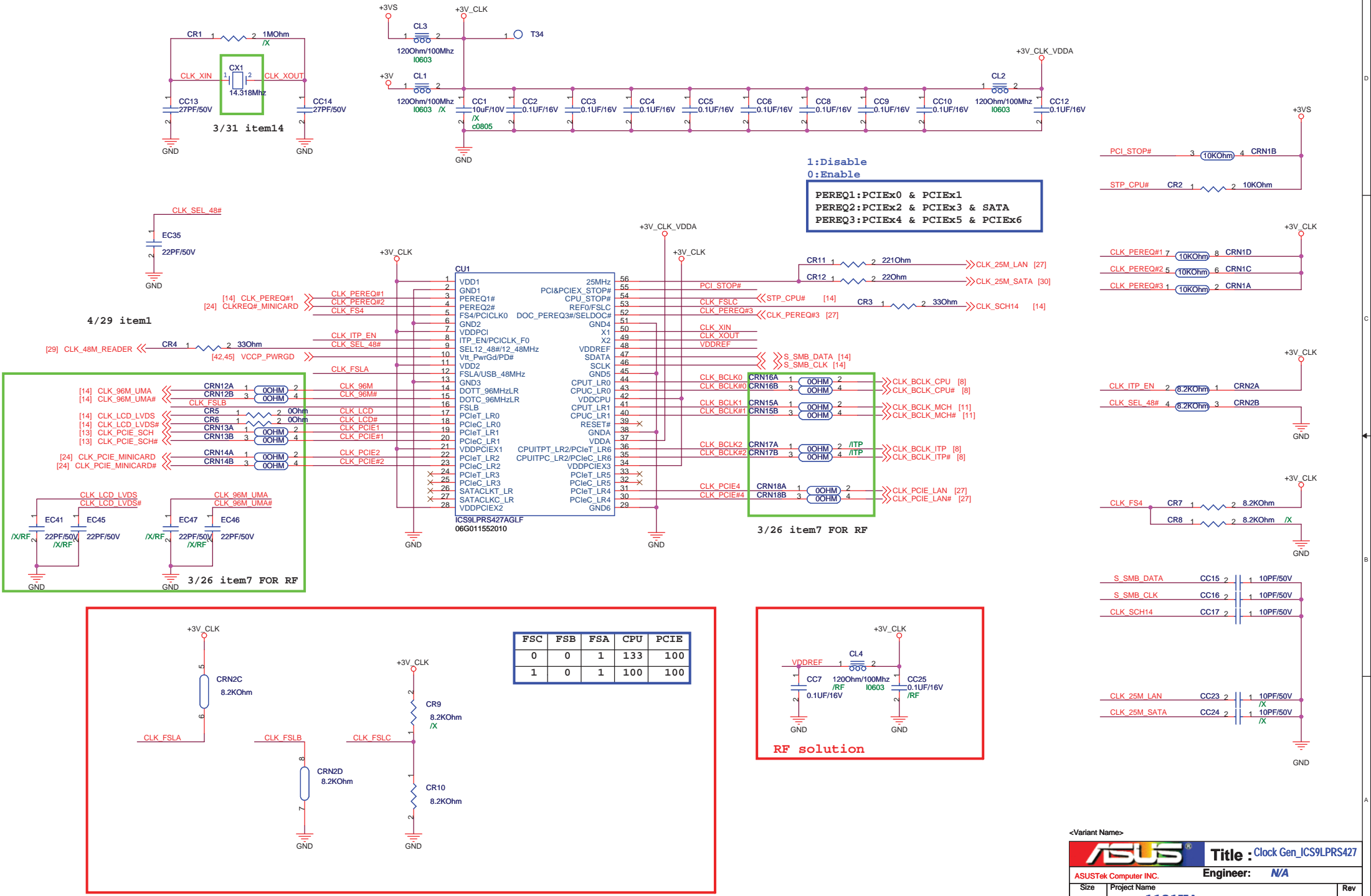
- 1.SCH asserts RSTRDY# at the same time as driving SLPMODE=1 to EC.
- 2.EC asserts RSTWARN to SCH.
- 3.EC asserts RESET# for **1200uS** to SCH after asserts RSTWARN.
- 4.EC deasserts RSTWARN.
- 5.EC deasserts RESET# after at least **100uS** delay from RSTWARN.

Cold Reset (SLPMODE=0)

The cold reset sequence results in a power cycling of all but the RTC power well.

Initial EC state: SUSB_ON=1, CPU_VRON=1, ICH_PWROK=1, PM_RSMRST#=1, PM_PWRBTN#=1, and VSUS_ON=1, RSTWARN=1, SUSC_ON=1, RESET#=1.

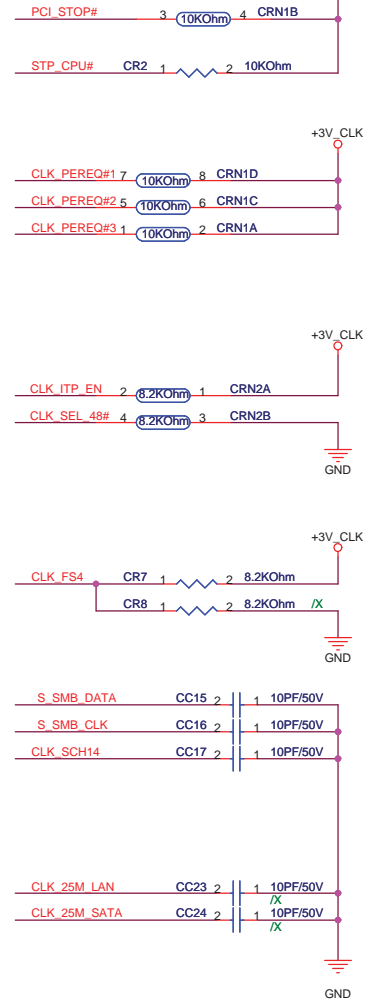
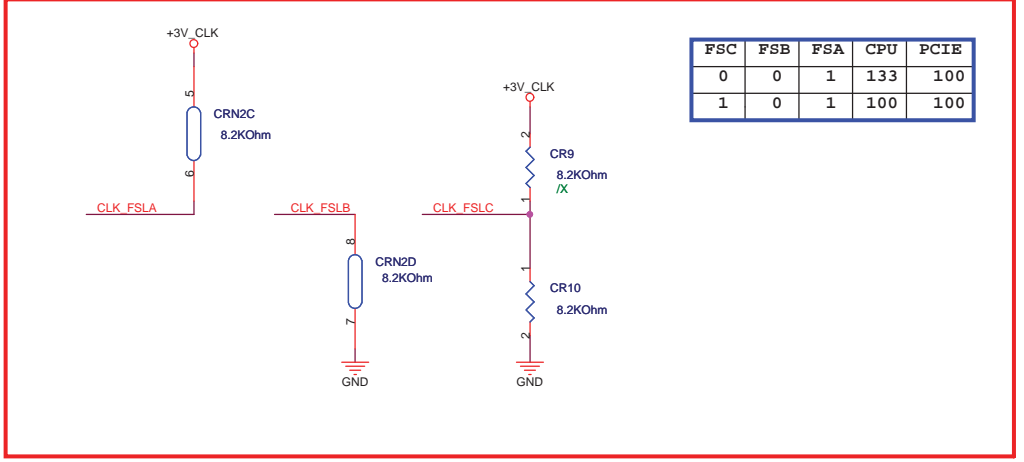
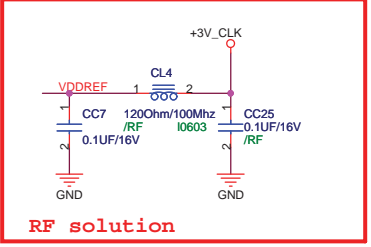
- 1.SCH asserts RSTRDY# at the same time as driving SLPMODE=0 to EC.
- 2.EC asserts RSTWARN to SCH.
- 3.EC asserts RESET# to SCH after asserts RSTWARN.
- 4.EC deasserts PM_PWROK and disables SUSB_ON and CPU_VRON power.
- 5.EC asserts PM_RSMRST# after CPU_VRON power is off.
- 6.EC disables SUSC_ON power for 3~5 seconds.
- 7.S4/S5 to S0 sequence is automatically followed to bring the system back to S0 when SUSC_ON power is enable.

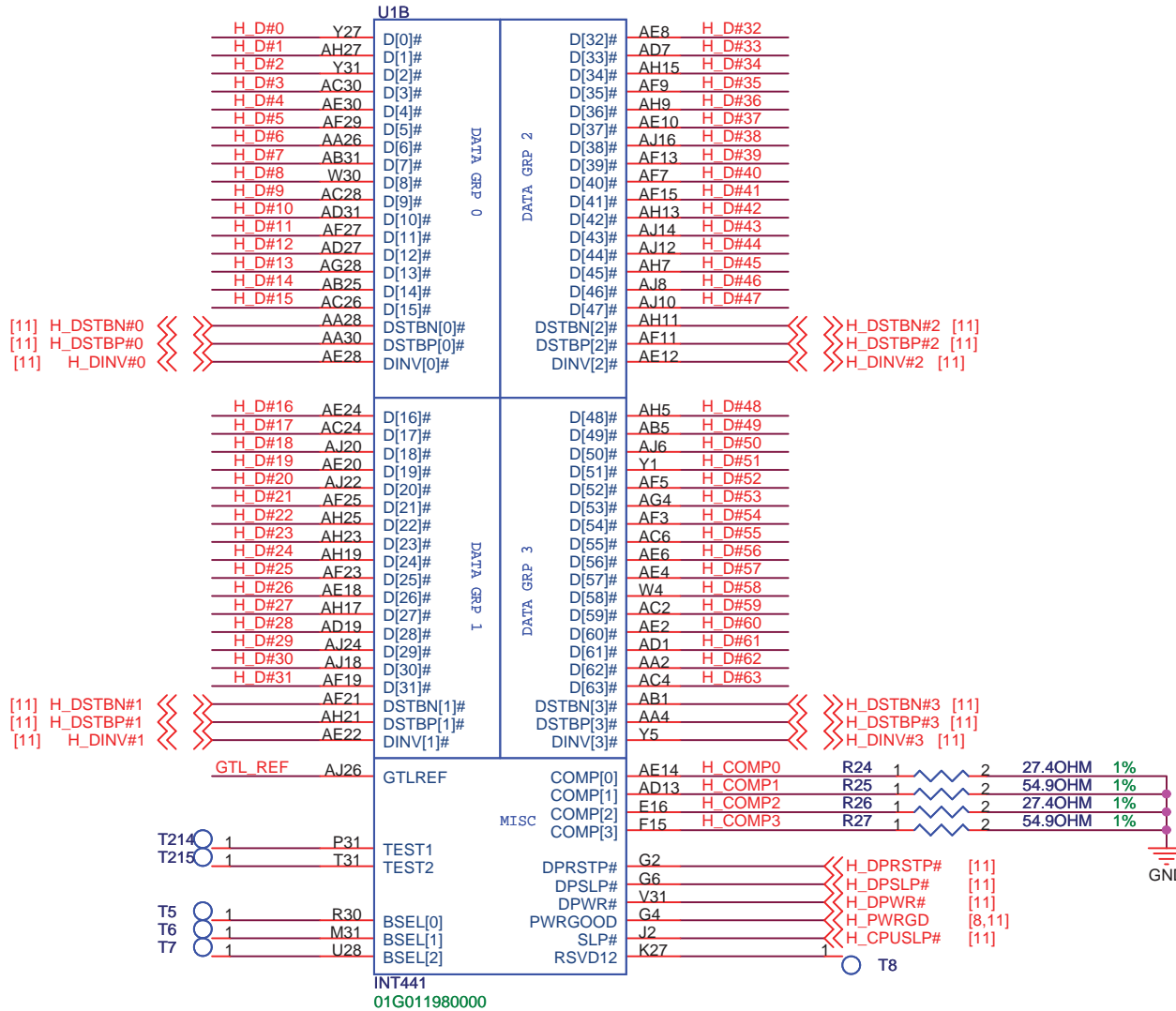


1:Disable
0:Enable

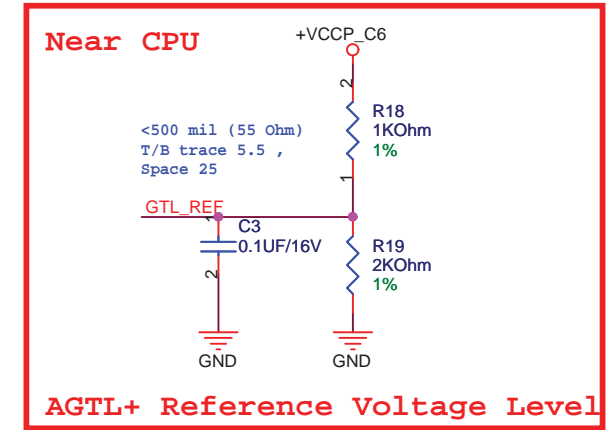
PEREQ1:PCIe#0 & PCIe#1
PEREQ2:PCIe#2 & PCIe#3 & SATA
PEREQ3:PCIe#4 & PCIe#5 & PCIe#6

FSC	FSB	FSA	CPU	PCIE
0	0	1	133	100
1	0	1	100	100





H_D#[63:0] << >>H_D#[63:0] [11]



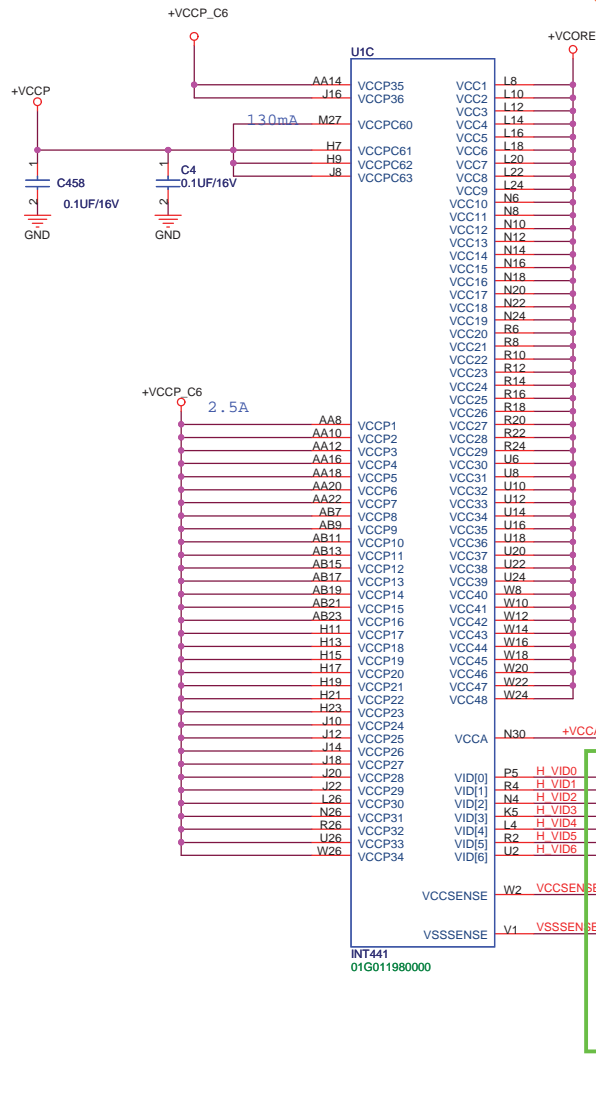
Layout Note

COMP 0 2 connect with Z0=27.4 ohm,L<0.5"

COMP 1 3 connect with Z0=55 ohm,L<0.5"

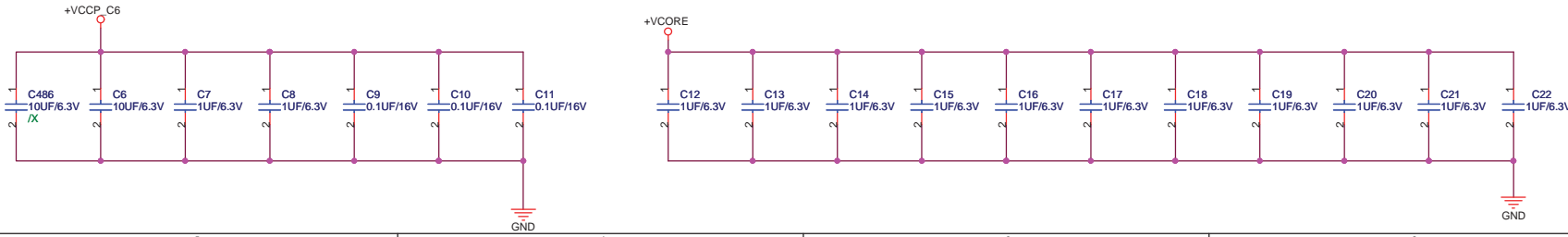
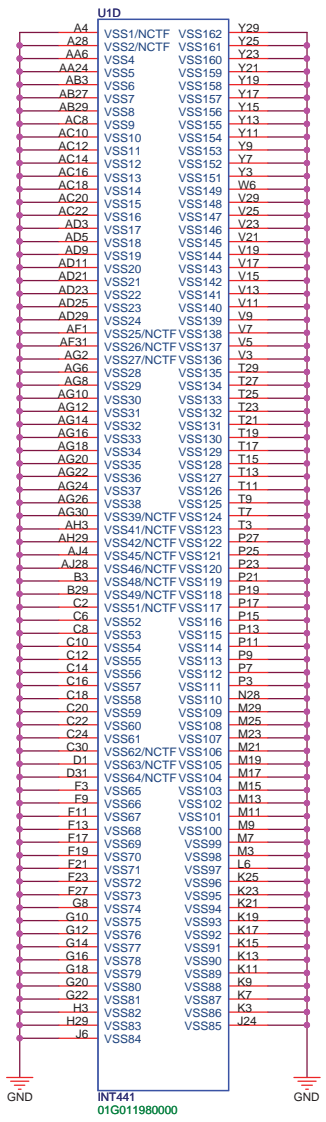
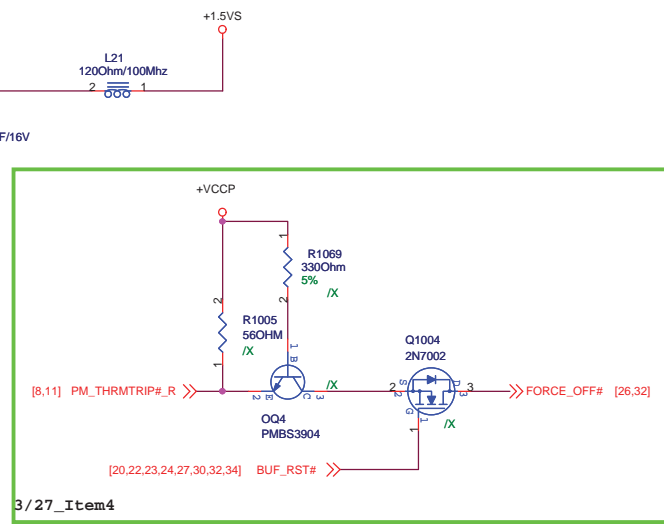
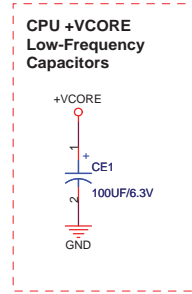
<Variant Name>

ASUS		Title : CPU-SLIVERTHORNE(1)	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name		Rev
A4	1101HA		1.2
Date: Tuesday, July 21, 2009		Sheet	9 of 50



CPU TYPE	Vcore	Freq
Silverthorne Standard Voltage	0.98V @HFM TBD @LFM	TBD
Process@Silverthorne Medium Voltage	0.8V @HFM TBD @LFM	TBD
Process@Silverthorne Low Voltage	0.76V @HFM TBD @LFM	TBD

Processor



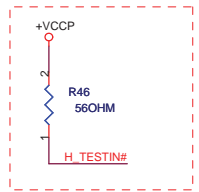
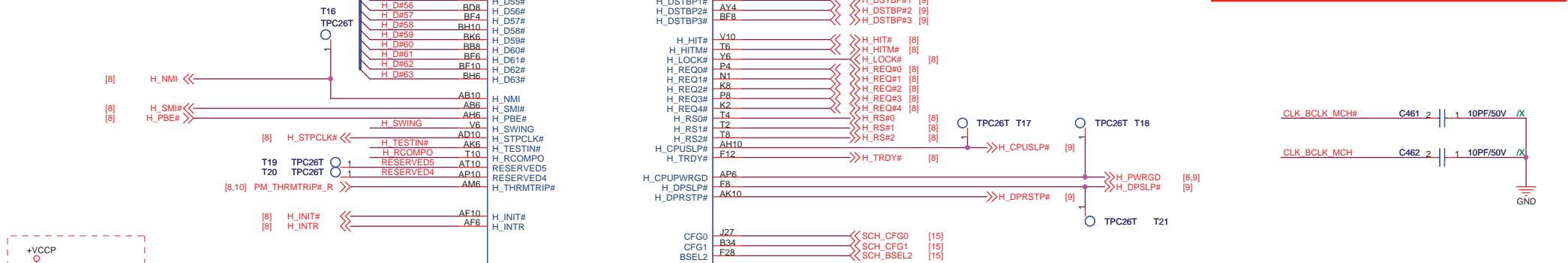
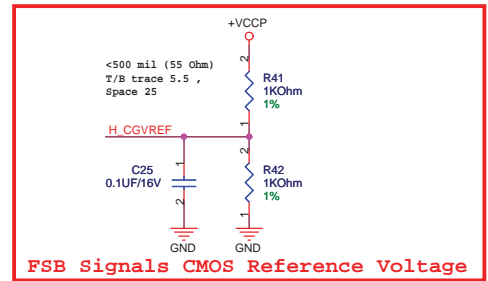
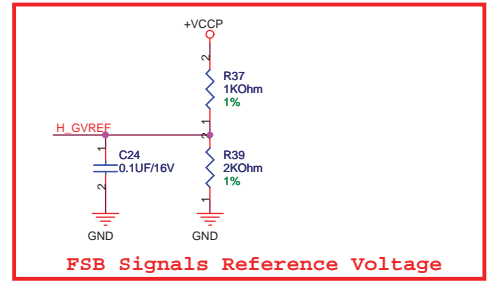
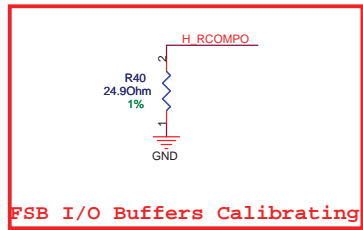
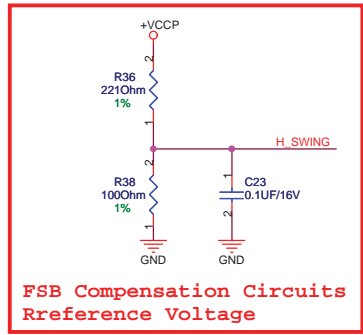
<Variant Name>

ASUS Title : CPU-SILVERTHORNE (2)

ASUSTeK COMPUTER INC Engineer: N/A

Size	Project Name	Rev
Custom	1101HA	1.2

Date: Tuesday, July 21, 2009 Sheet 10 of 50



[18] MA_DQ[63:0] << >>

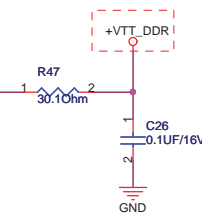
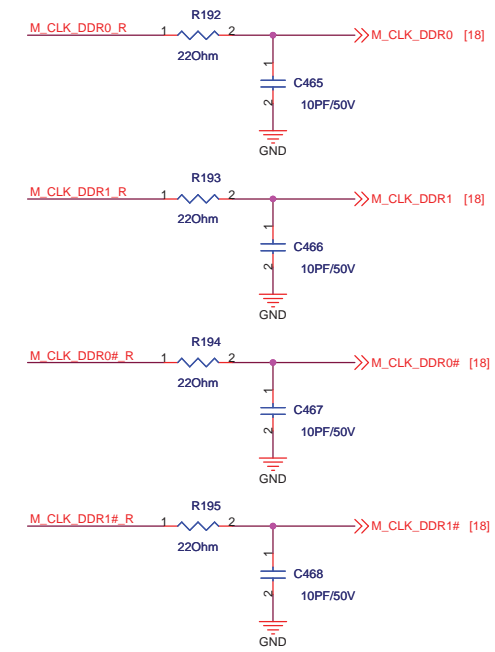
DDR SYSTEM MEMORY

MA	SM	U2D
MA_DQ0	SM_DQ0	BG49
MA_DQ1	SM_DQ1	BG47
MA_DQ2	SM_DQ2	BE45
MA_DQ3	SM_DQ3	BC43
MA_DQ4	SM_DQ4	BE47
MA_DQ5	SM_DQ5	BC47
MA_DQ6	SM_DQ6	BC45
MA_DQ7	SM_DQ7	BK44
MA_DQ8	SM_DQ8	BK42
MA_DQ9	SM_DQ9	BG41
MA_DQ10	SM_DQ10	BK40
MA_DQ11	SM_DQ11	BC41
MA_DQ12	SM_DQ12	BG43
MA_DQ13	SM_DQ13	BJ43
MA_DQ14	SM_DQ14	BJ39
MA_DQ15	SM_DQ15	BG39
MA_DQ16	SM_DQ16	BC39
MA_DQ17	SM_DQ17	BK38
MA_DQ18	SM_DQ18	BG37
MA_DQ19	SM_DQ19	BK36
MA_DQ20	SM_DQ20	BJ37
MA_DQ21	SM_DQ21	BG35
MA_DQ22	SM_DQ22	BJ35
MA_DQ23	SM_DQ23	BC35
MA_DQ24	SM_DQ24	BK34
MA_DQ25	SM_DQ25	BG31
MA_DQ26	SM_DQ26	BG33
MA_DQ27	SM_DQ27	BK30
MA_DQ28	SM_DQ28	BC33
MA_DQ29	SM_DQ29	BJ31
MA_DQ30	SM_DQ30	BK28
MA_DQ31	SM_DQ31	BC29
MA_DQ32	SM_DQ32	BE27
MA_DQ33	SM_DQ33	BG29
MA_DQ34	SM_DQ34	BK28
MA_DQ35	SM_DQ35	BC29
MA_DQ36	SM_DQ36	BE27
MA_DQ37	SM_DQ37	BK26
MA_DQ38	SM_DQ38	BG25
MA_DQ39	SM_DQ39	BJ25
MA_DQ40	SM_DQ40	BC25
MA_DQ41	SM_DQ41	BG23
MA_DQ42	SM_DQ42	BK22
MA_DQ43	SM_DQ43	BJ21
MA_DQ44	SM_DQ44	BK24
MA_DQ45	SM_DQ45	BJ23
MA_DQ46	SM_DQ46	BG21
MA_DQ47	SM_DQ47	BC21
MA_DQ48	SM_DQ48	BK20
MA_DQ49	SM_DQ49	BJ19
MA_DQ50	SM_DQ50	BG17
MA_DQ51	SM_DQ51	BJ17
MA_DQ52	SM_DQ52	BG19
MA_DQ53	SM_DQ53	BC19
MA_DQ54	SM_DQ54	BC17
MA_DQ55	SM_DQ55	BK16
MA_DQ56	SM_DQ56	BG15
MA_DQ57	SM_DQ57	BC15
MA_DQ58	SM_DQ58	BJ13
MA_DQ59	SM_DQ59	BK12
MA_DQ60	SM_DQ60	BK14
MA_DQ61	SM_DQ61	BJ15
MA_DQ62	SM_DQ62	BC13
MA_DQ63	SM_DQ63	BC11

02G010018700

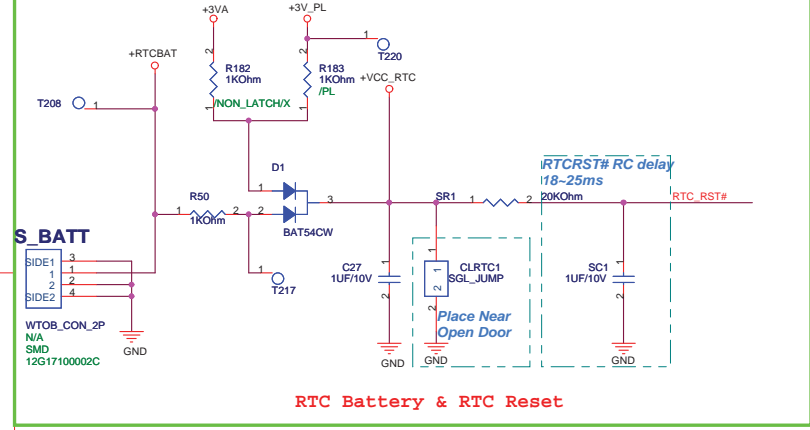
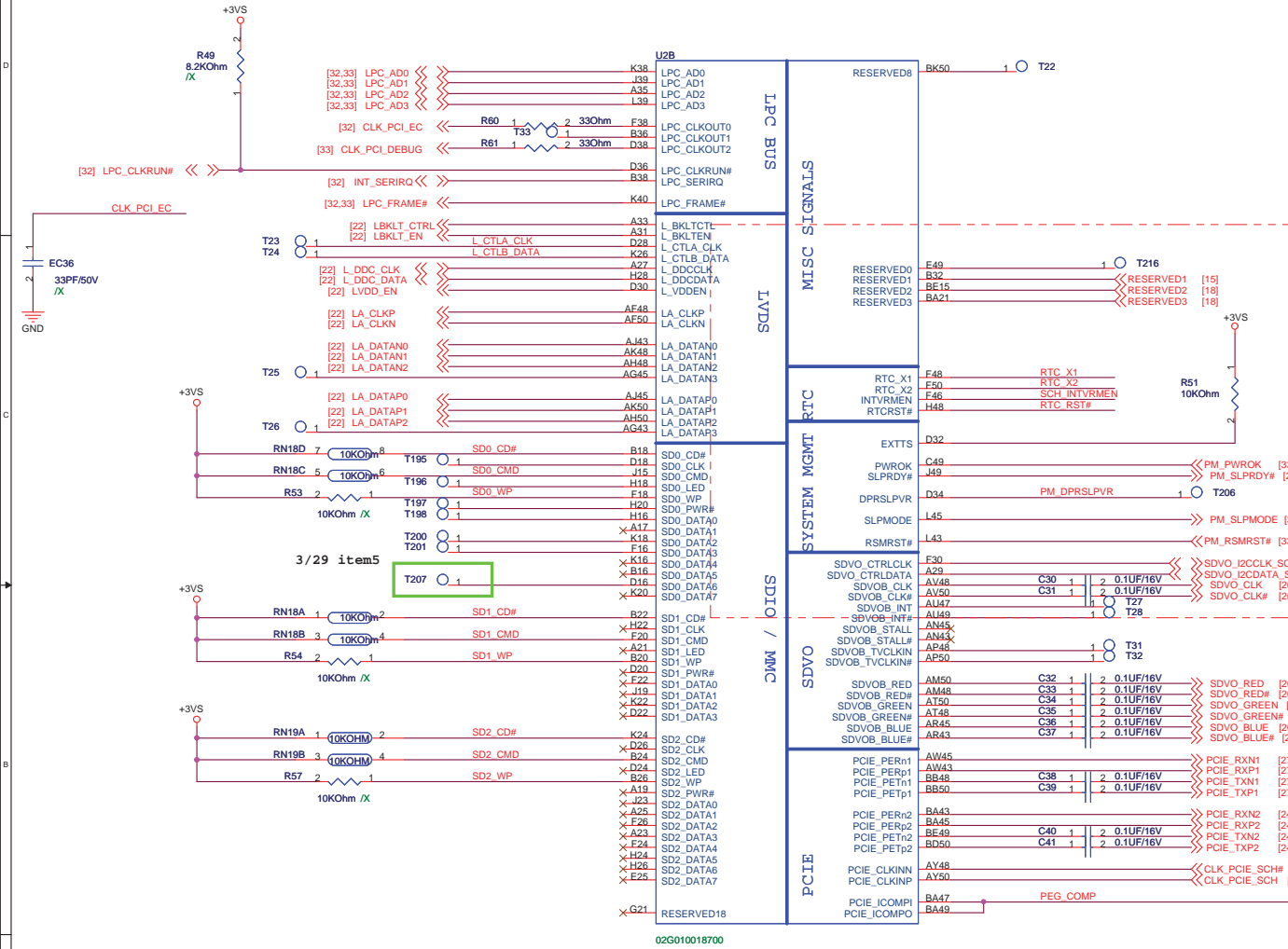
SM_BS0	BC27	MA_BA0	<< >>MA_BA[2:0] [18,19]
SM_BS1	BE25	MA_BA1	
SM_BS2	BA35	MA_BA2	
SM_CK0	BG45	M_CLK_DDR0_R	
SM_CK1	BE11	M_CLK_DDR1#_R	
SM_CK0#	BJ45	M_CLK_DDR0#_R	
SM_CK1#	BG11	M_CLK_DDR1#_R	
SM_CKE0	BE39	>>MA_CKE0 [18,19]	
SM_CKE1	BE37	>>MA_CKE1 [18,19]	
SM_DQS0	BJ47	MA_DQS0	<< >>MA_DQS[7:0] [18]
SM_DQS1	BJ41	MA_DQS1	
SM_DQS2	BC37	MA_DQS2	
SM_DQS3	BK32	MA_DQS3	
SM_DQS4	BG27	MA_DQS4	
SM_DQS5	BE23	MA_DQS5	
SM_DQS6	BK18	MA_DQS6	
SM_DQS7	BG13	MA_DQS7	
SM_MA0	BJ27	MA_MA0	<< >>MA_MA[14:0] [18,19]
SM_MA1	BA19	MA_MA1	
SM_MA2	BA27	MA_MA2	
SM_MA3	BA25	MA_MA3	
SM_MA4	BE29	MA_MA4	
SM_MA5	BC23	MA_MA5	
SM_MA6	BE31	MA_MA6	
SM_MA7	BA31	MA_MA7	
SM_MA8	BA33	MA_MA8	
SM_MA9	BA29	MA_MA9	
SM_MA10	BE17	MA_MA10	
SM_MA11	BE35	MA_MA11	
SM_MA12	BE33	MA_MA12	
SM_MA13	BE19	MA_MA13	
SM_MA14	BA37	MA_MA14	
SM_VREF	BE43	<<DDR_VREF [18]	
SM_RAS#	BE21	>>MA_RAS# [18,19]	
SM_CAS#	BA13	>>MA_CAS# [18,19]	
SM_WE#	BA17	>>MA_WE# [18,19]	
SM_CS0#	BA23	>>MA_CS#0 [18,19]	
SM_CS1#	BA15	>>MA_CS#1 [18,19]	
SM_RCMP0	BE13	SM_RCMP0	
SM_RCVENIN	BA39	MA_RCVENIN	
SM_RCVENOUT	BE41	MA_RCVENOUT	

Note: TOTAL LENGTH <1"

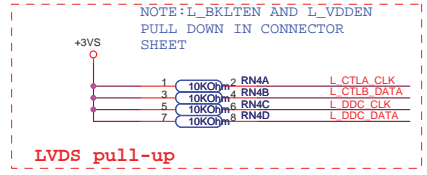
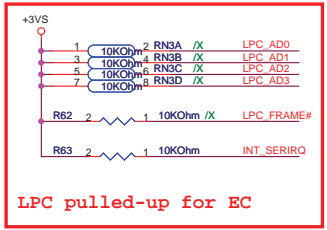
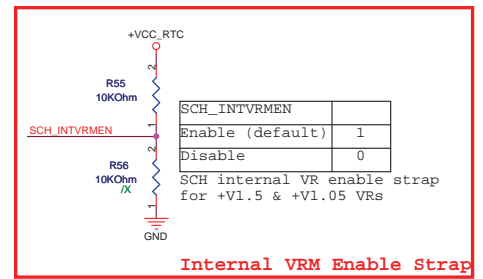
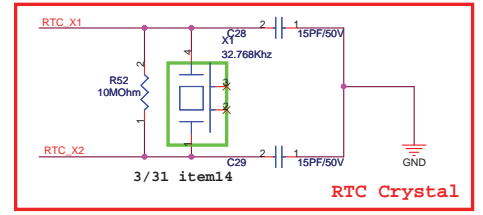


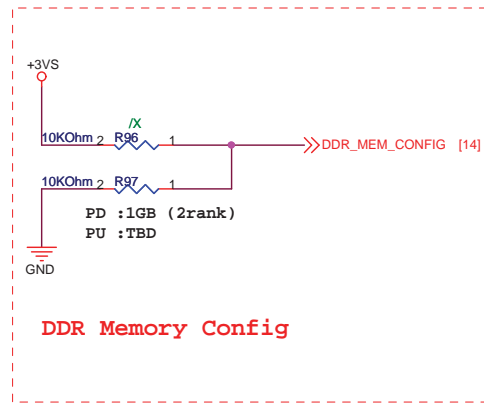
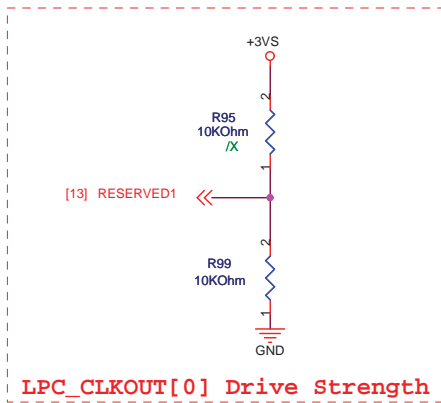
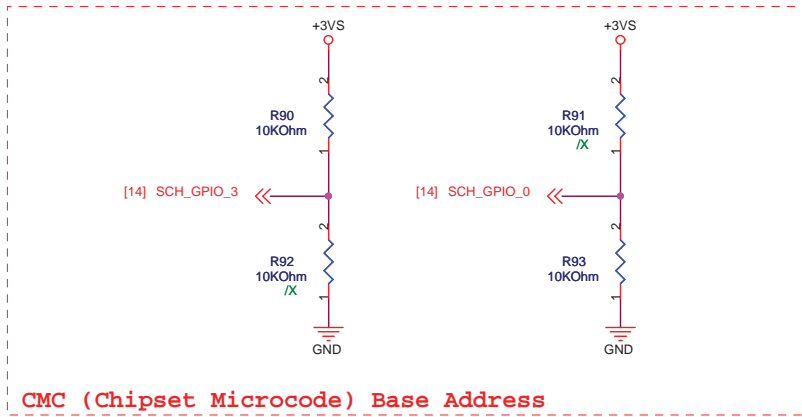
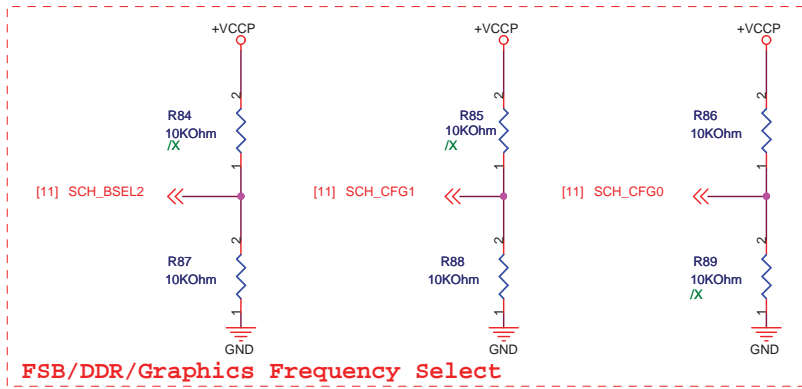
<Variant Name>

ASUS		Title : Poulsbo_DDR2 (2)	
ASUSTek Computer INC.		Engineer: N/A	
Size	Project Name	Rev	
Custom	1101HA	1.2	
Date: Tuesday, July 21, 2009	Sheet	12	of 50

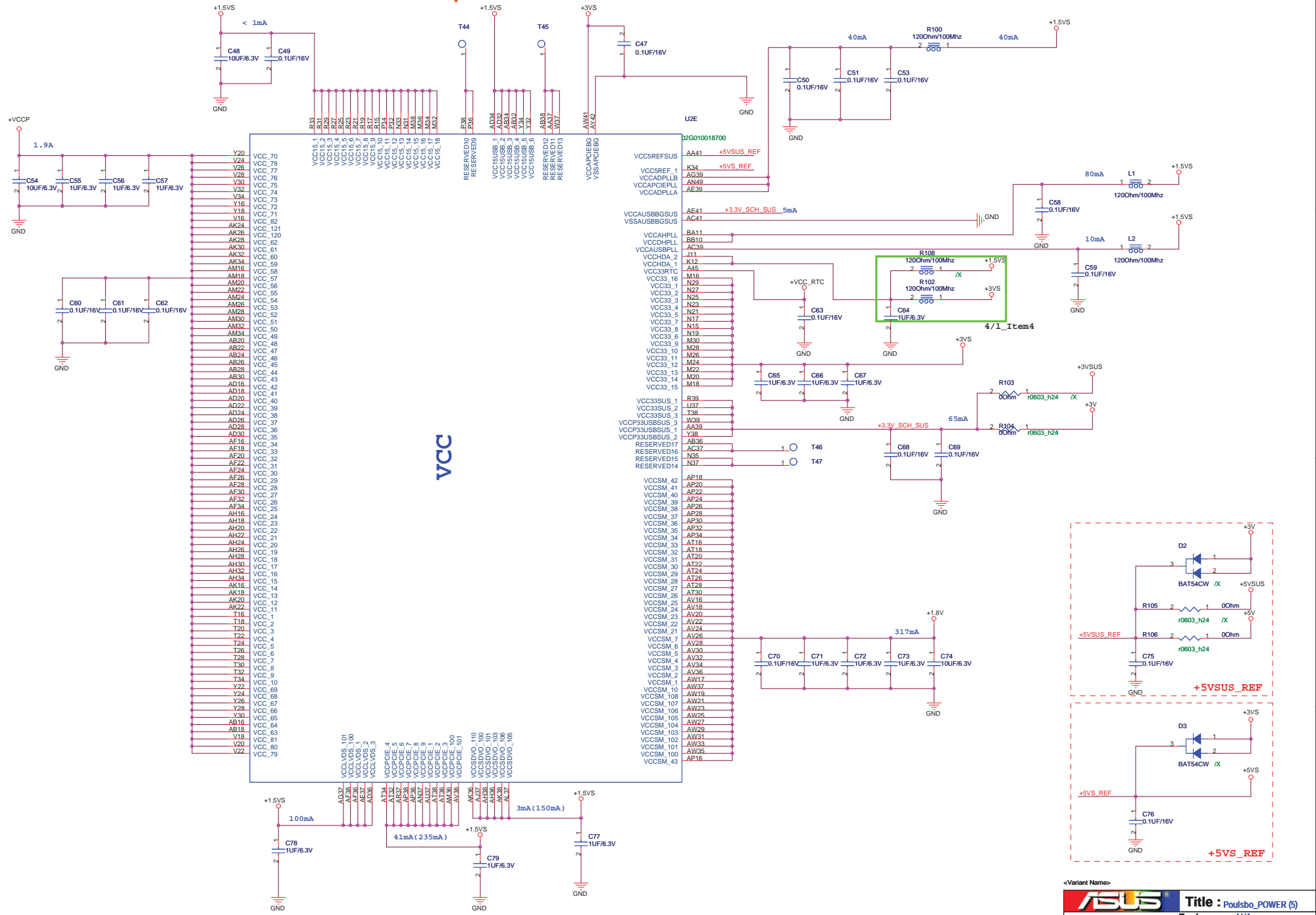


PM_SLPDRY#	PM_SLPMODE	System Behavior
0	1	SCH ready to enter S3
0	0	SCH ready to enter S4/S5



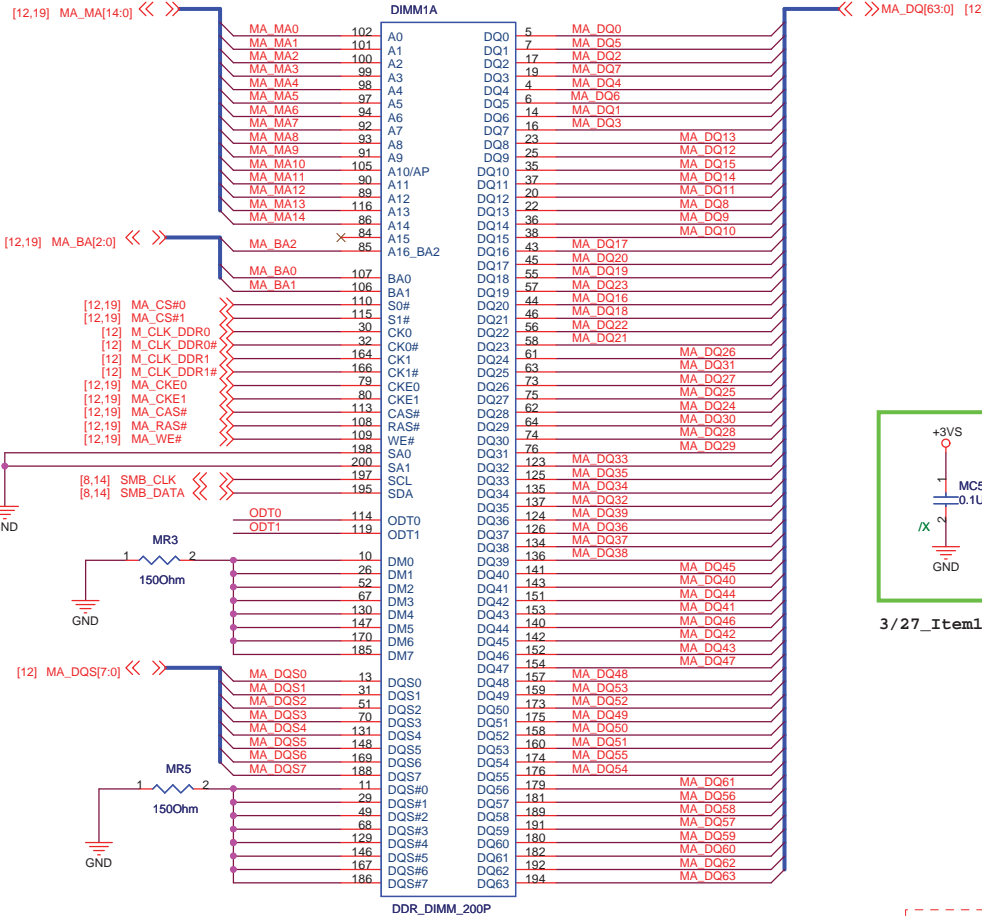


Strap Function	Singal Name			Strap		Comment	
FSB/DDR Frequency Select Graphics Frequency Select	SCH_BSEL2	SCH_CFG1	SCH_CFG0	Gfx_Freq	FSB	Note: Clock Frequencies are in Mhz Default Frequency determined by FSB speed	
	0	0	0	200	400		
	0	0	1	200	533		
CMC (Chipset Microcode) Base Address	GPIO3		GPIO0		Address		Selects the starting address that the CMC will use to start fetching code. (GPIO3 is the most significant)
	0	0		0xFFFF0000			
	0	1		0xFFFC0000			
	1	0		0xFFFD0000 (default)			
	1	1		0xFFFE0000			
LPC_CLKOUT[0] Buffer Strength	RESERVED1			Value		Selects the drive strength of the LPC_CLKOUT[0] clock.	
	0			Reserved			
	0			1 Load (Default)			
	1			Reserved			
	1			2 Loads			

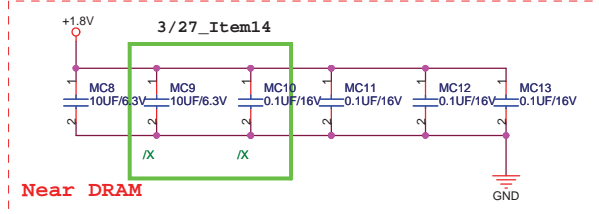
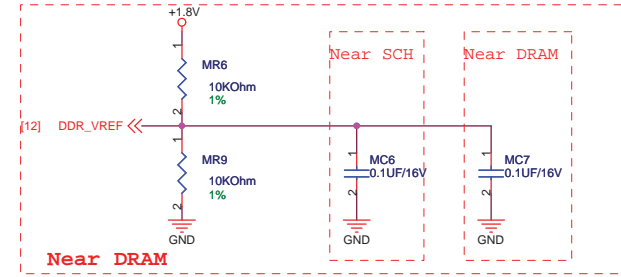
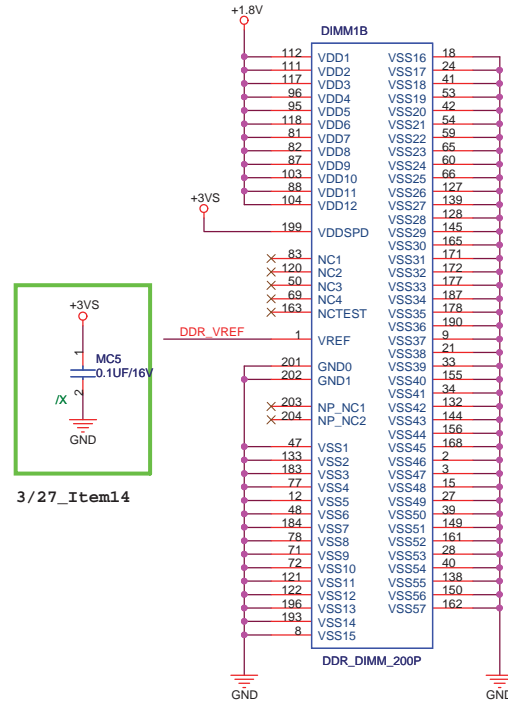


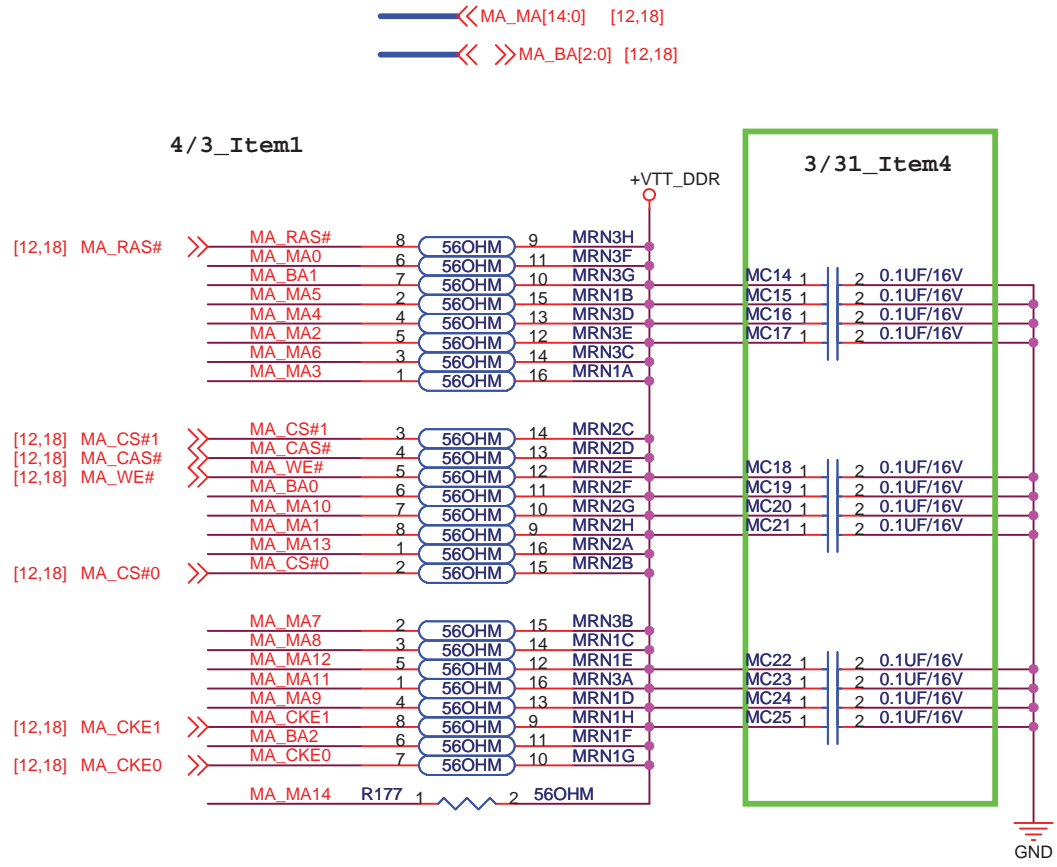
VCC

4/3_Item1



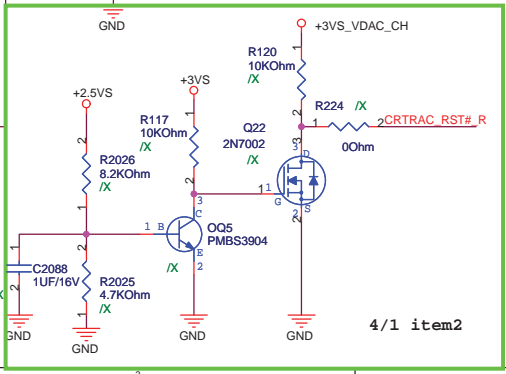
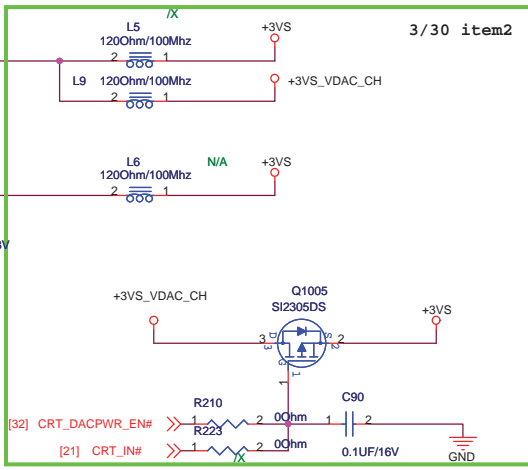
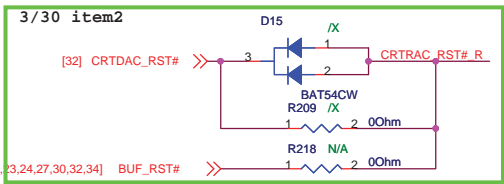
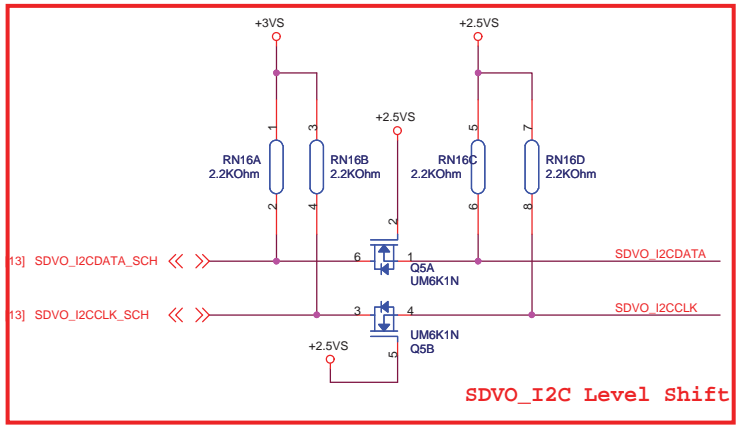
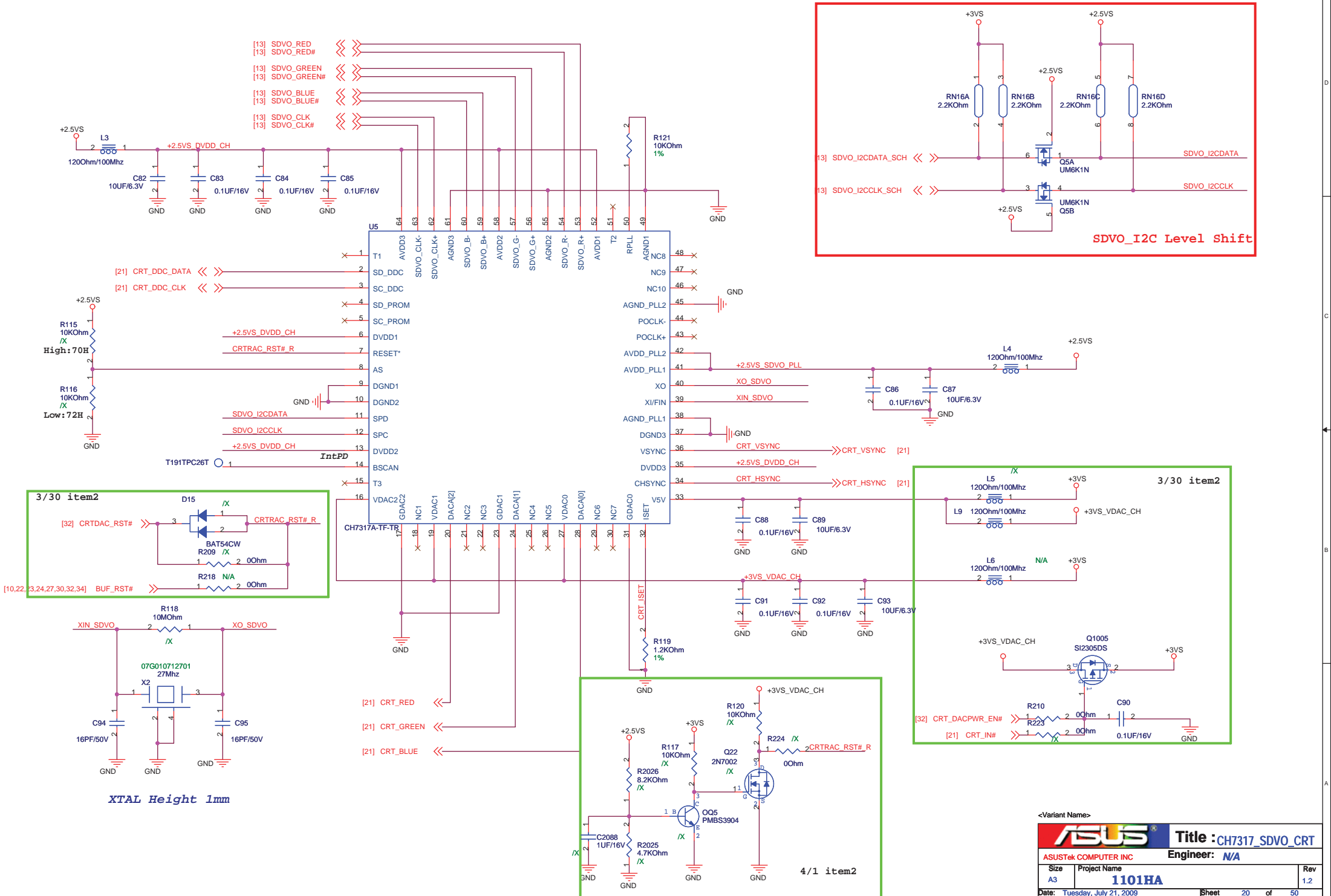
DDR II slot Symbol use 12G025332003

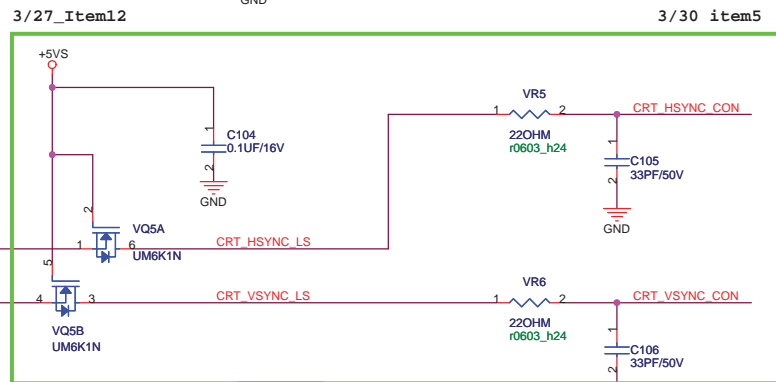
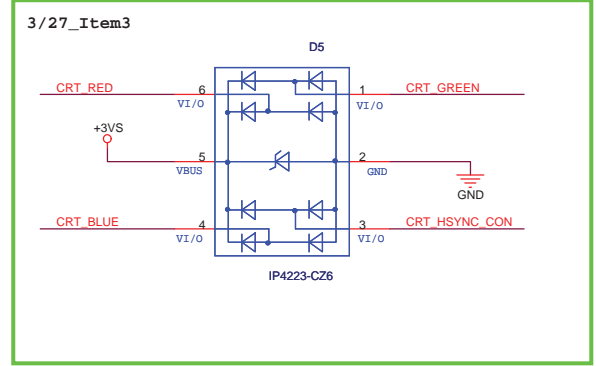
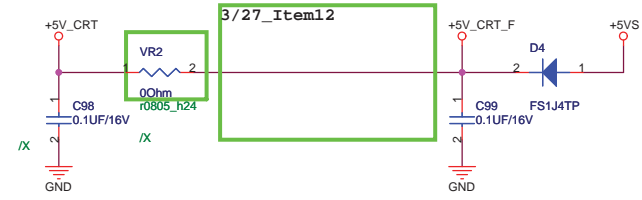
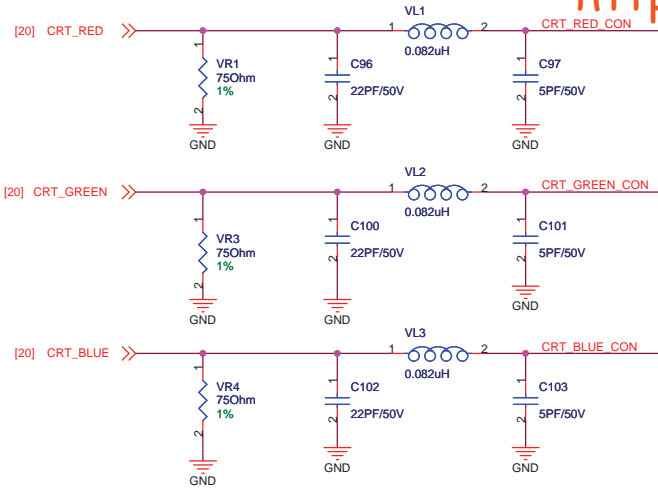




<Variant Name>

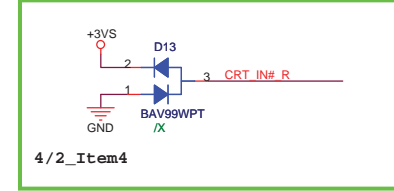
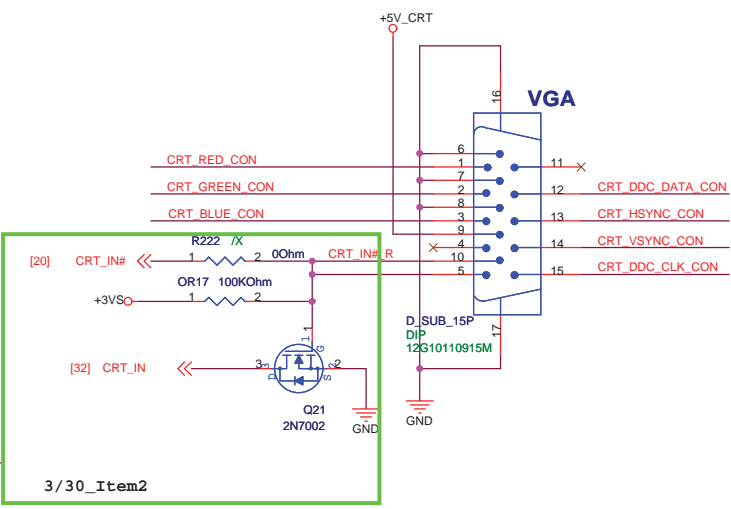
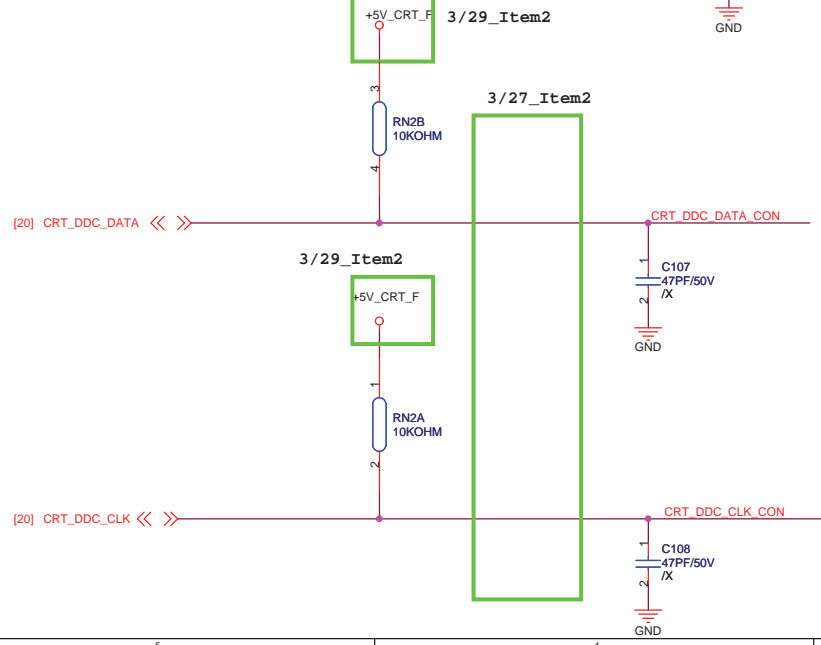
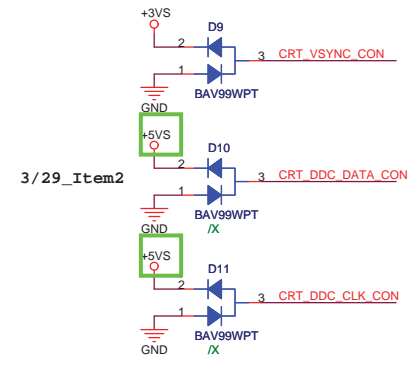
ASUS		Title : DDR2_Termination	
ASUSTek Computer INC.		Engineer: <i>N/A</i>	
Size	Project Name		Rev
A4	1101HA		1.2
Date: Tuesday, July 21, 2009		Sheet	19 of 50

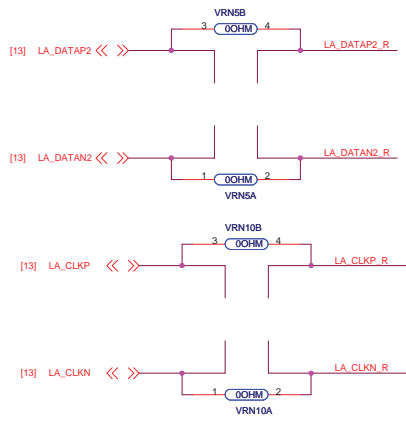




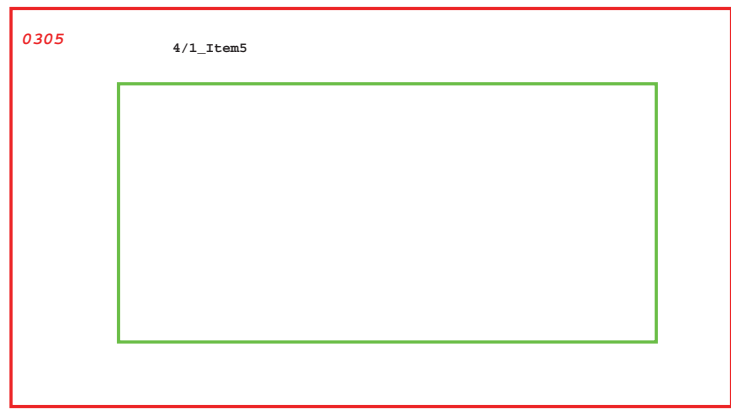
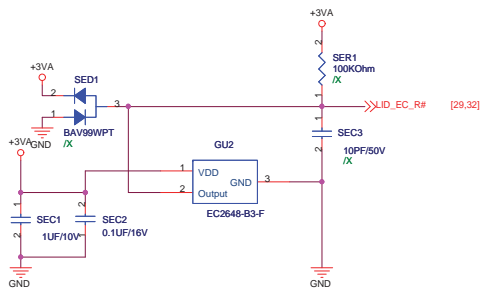
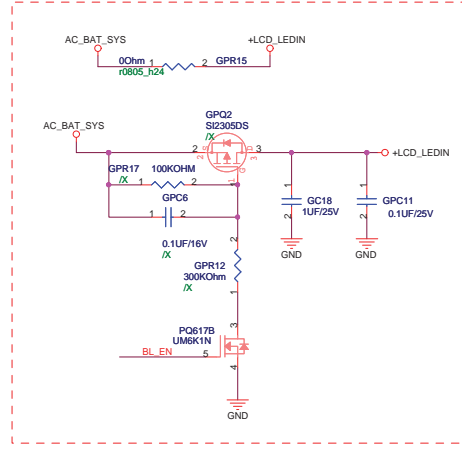
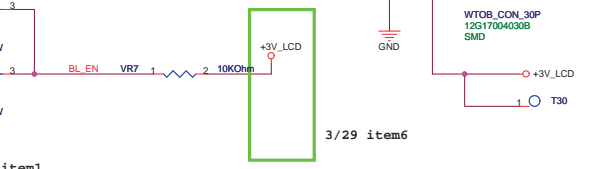
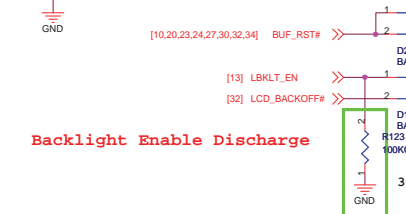
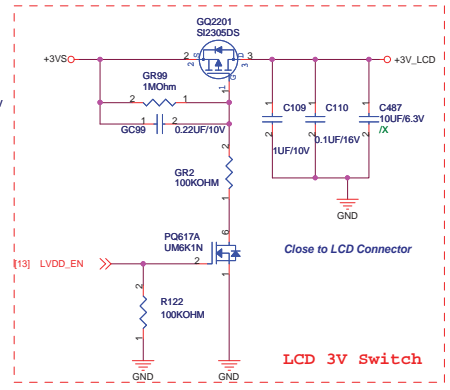
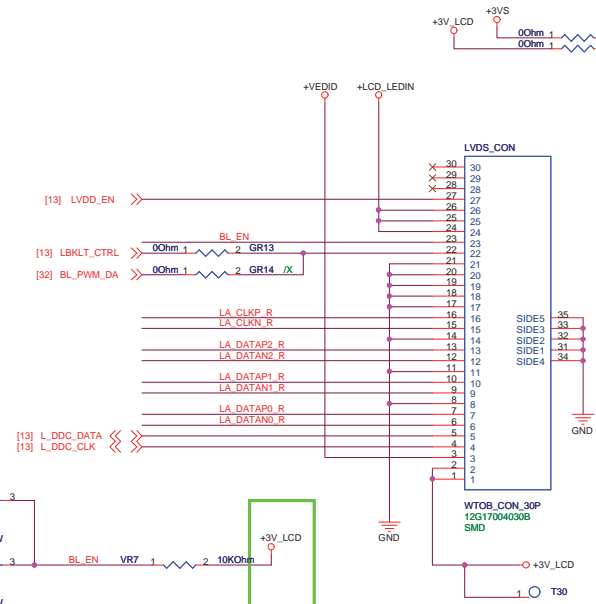
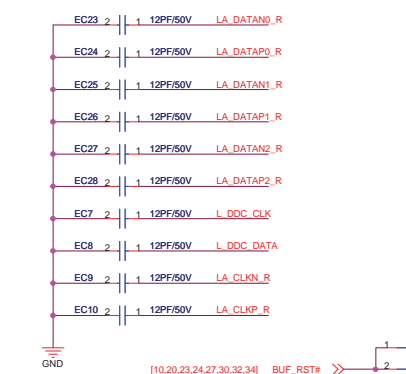
C105 C106 for EA measurement
 U6上:VR5 & VR6-->22 OHM
 U6 /X :VR5 & VR6 -->0 OHM

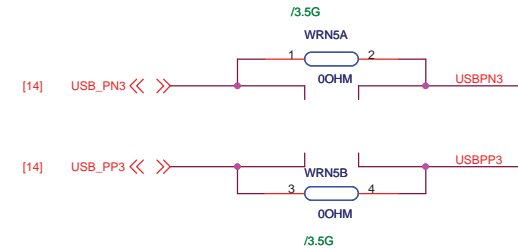
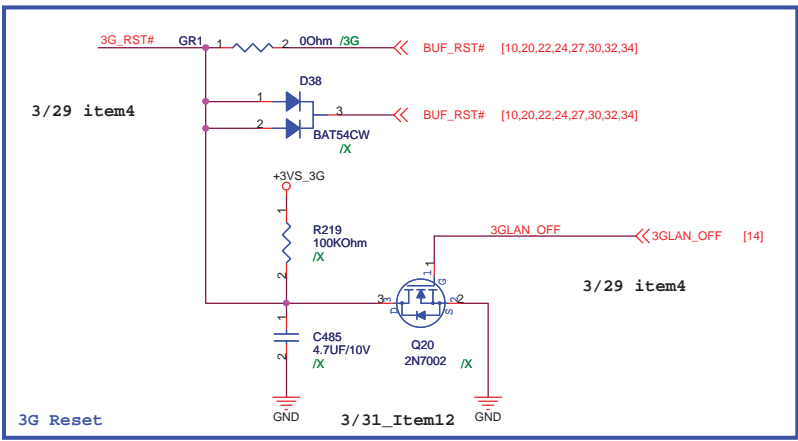
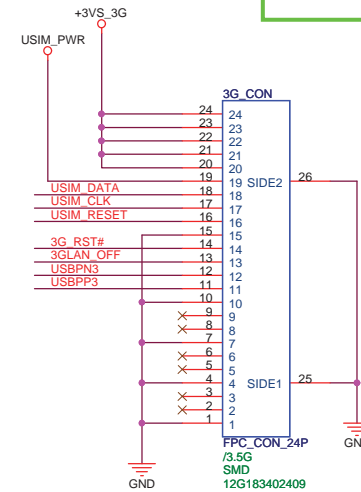
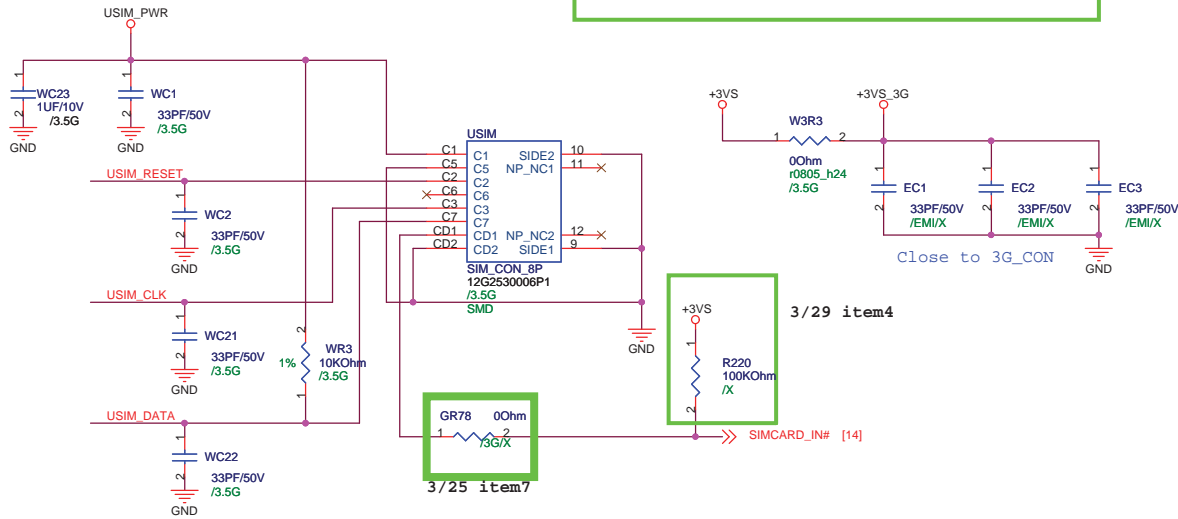
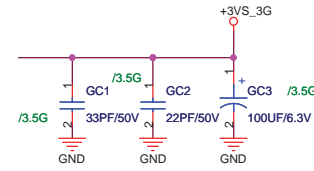
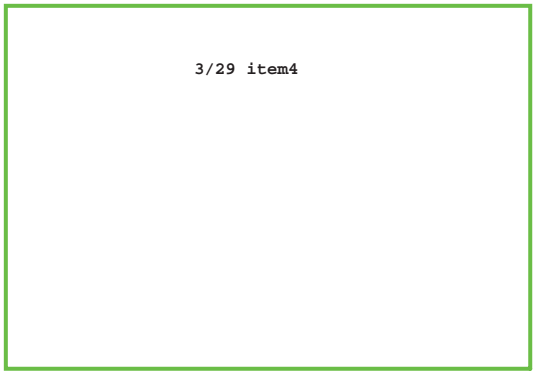
BUS BUFFER:
 Unidirectional buffers (high impedance buffers) are required on both HSYNC and VSYNC to prevent potential electrical overstress and illegal operation of the GMCH, since some display monitors may attempt to drive HSYNC and VSYNC signals back to GMCH.

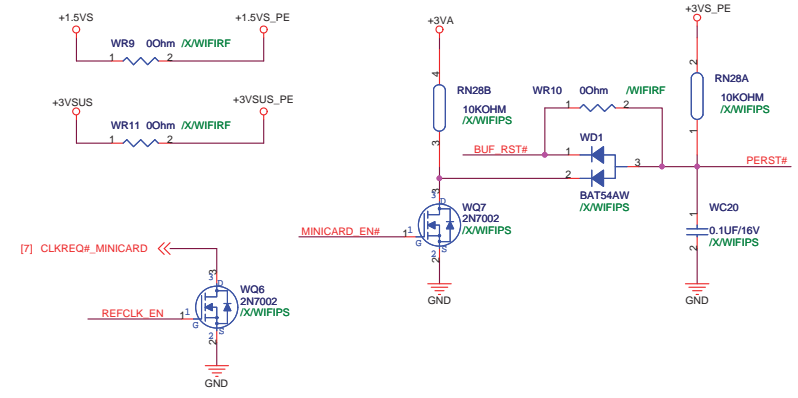
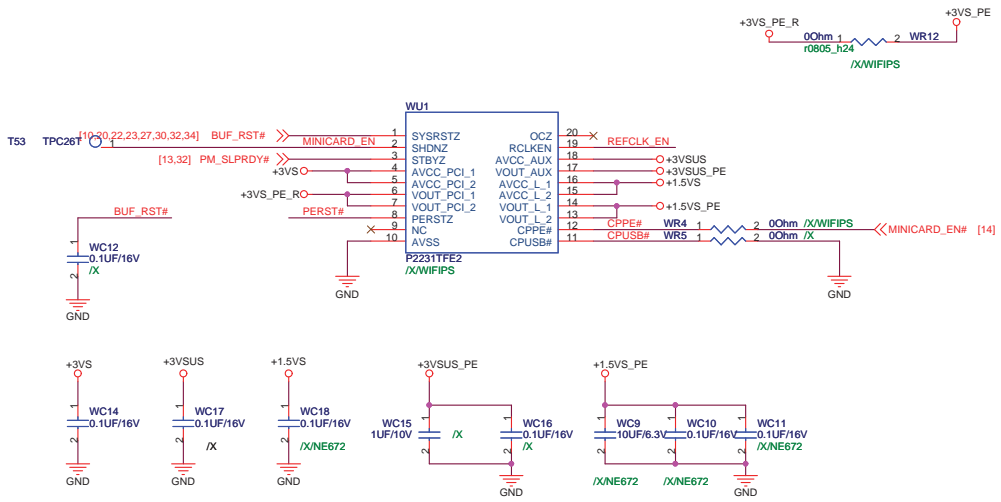
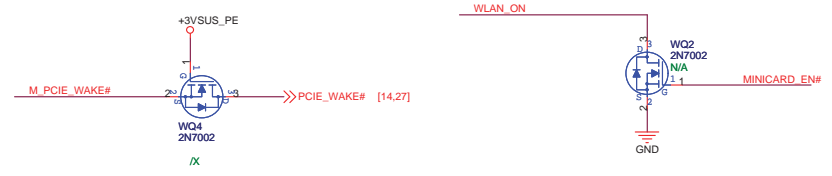
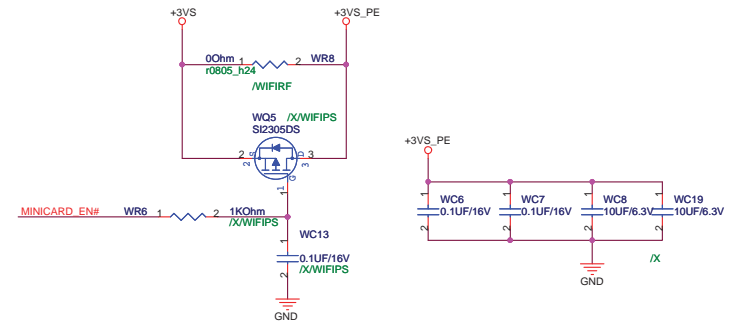
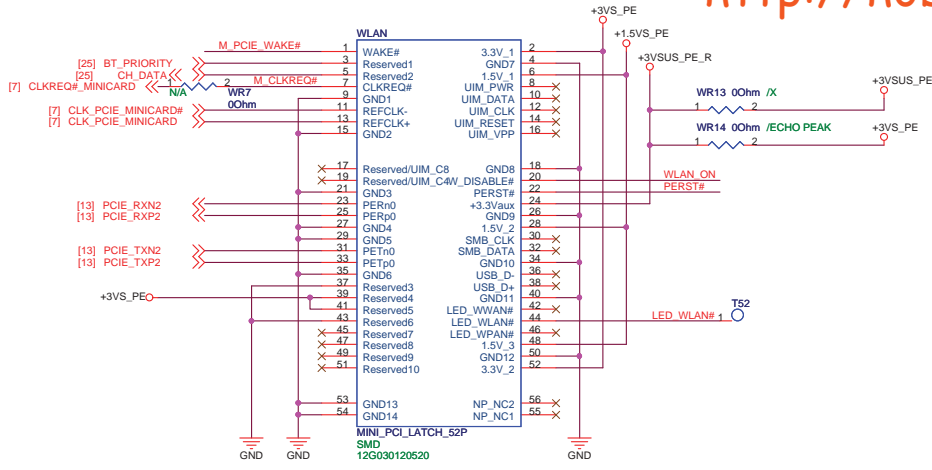


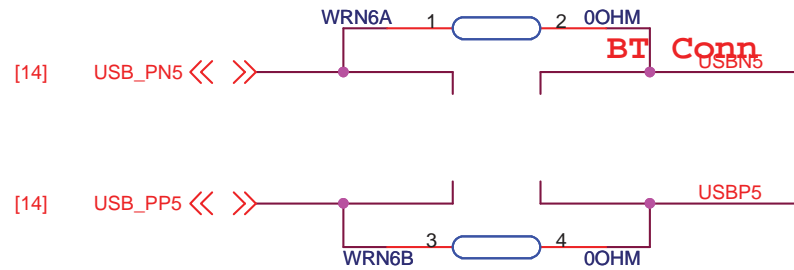
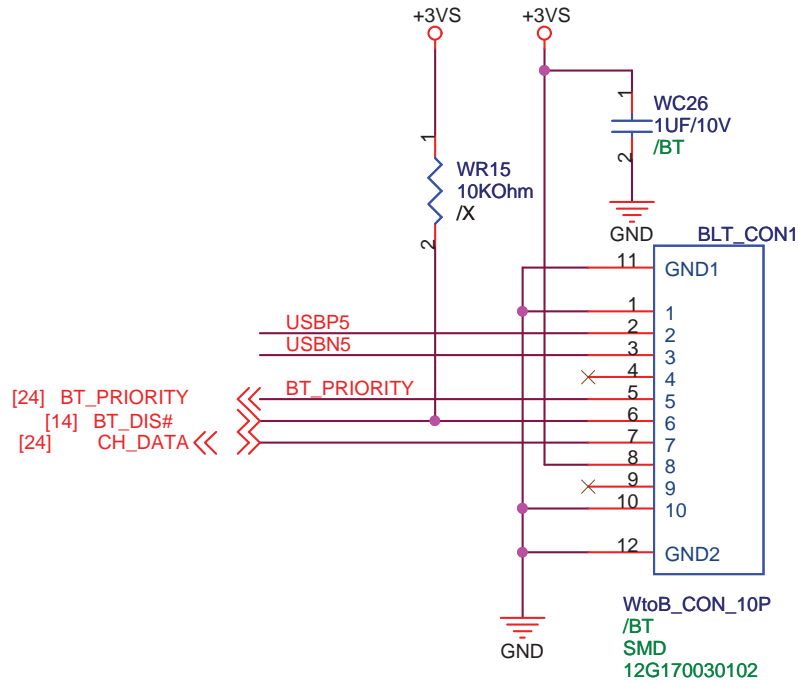


3/26_Item7 FOR RF



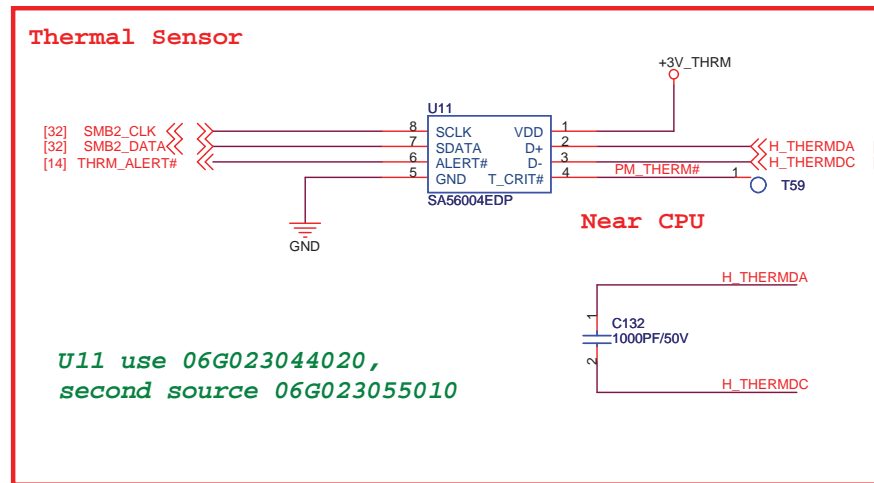
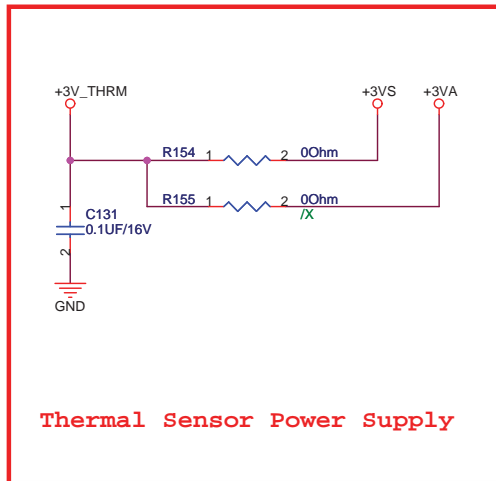
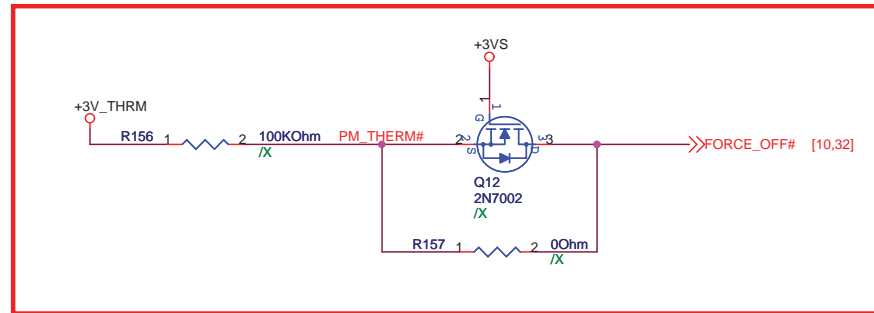
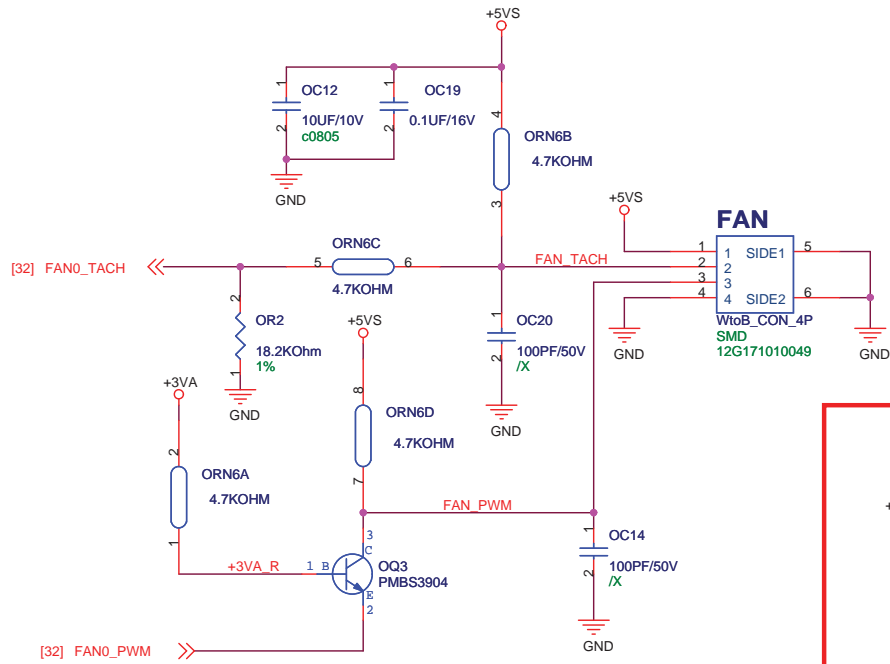






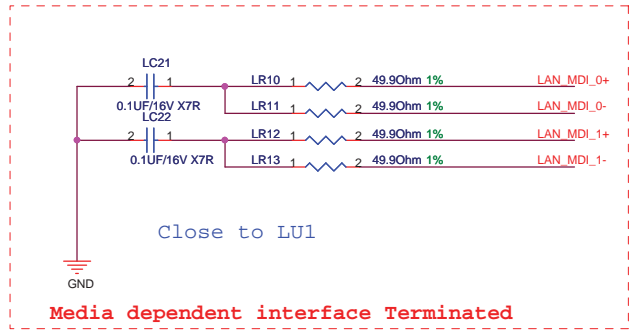
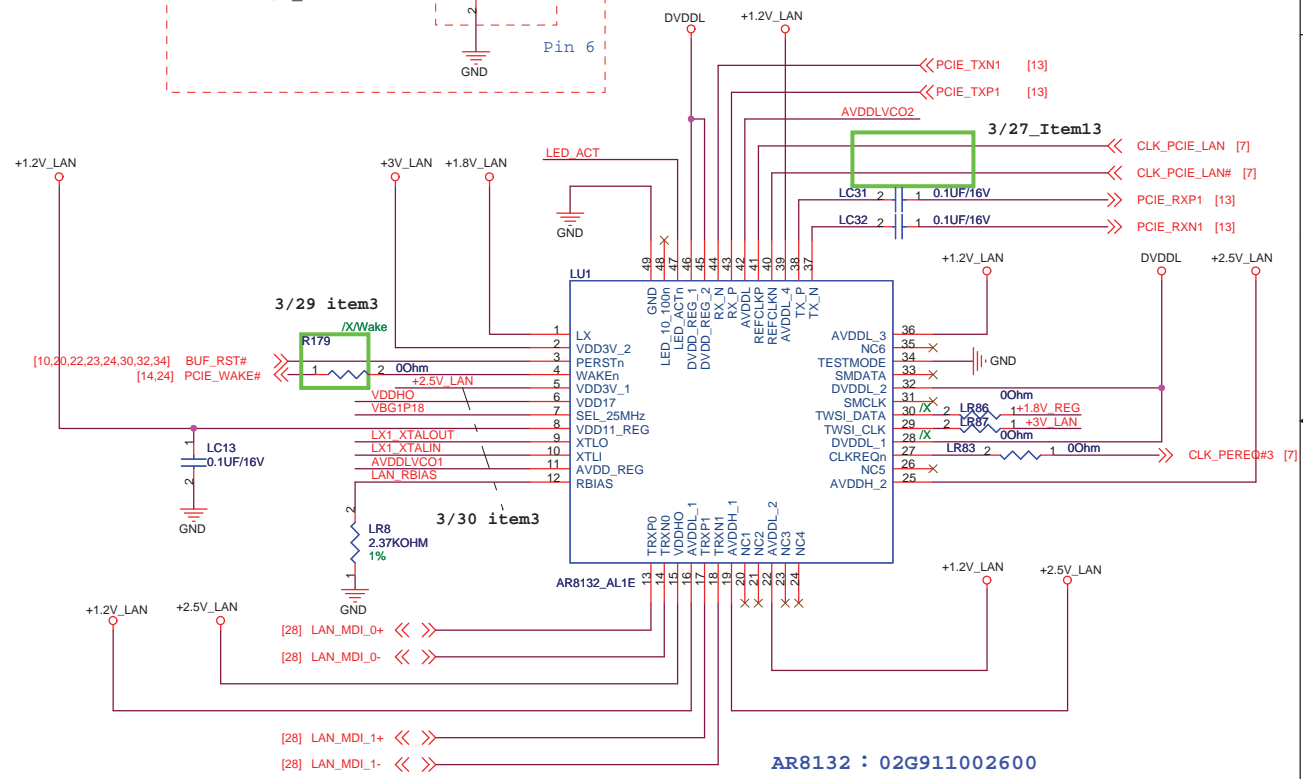
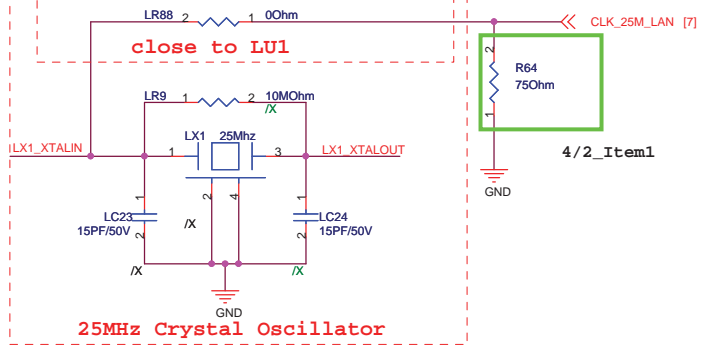
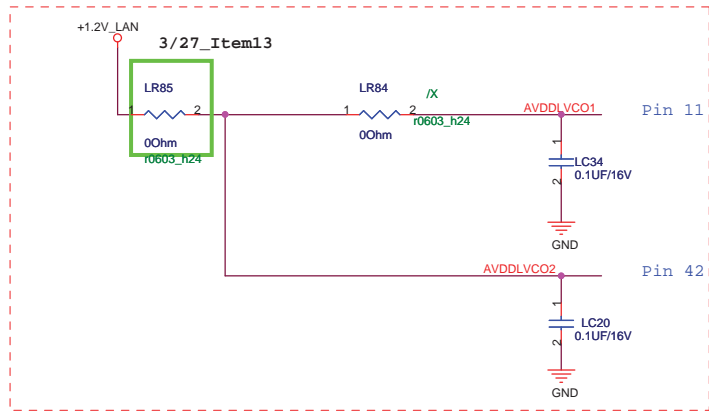
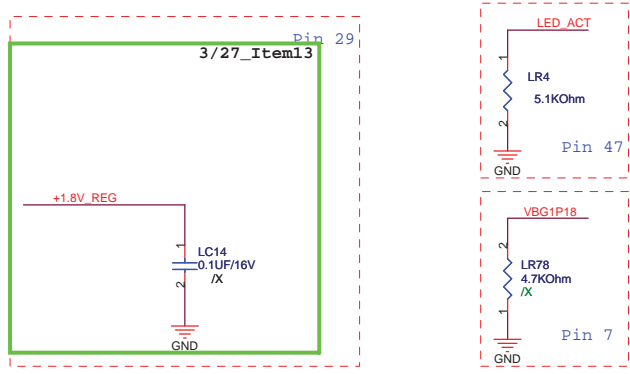
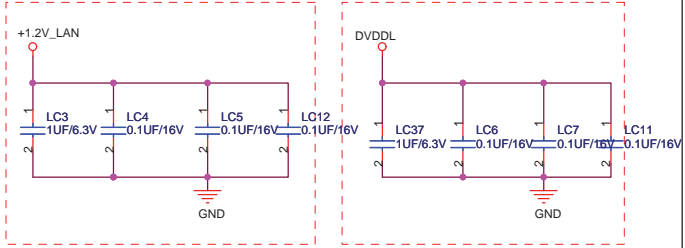
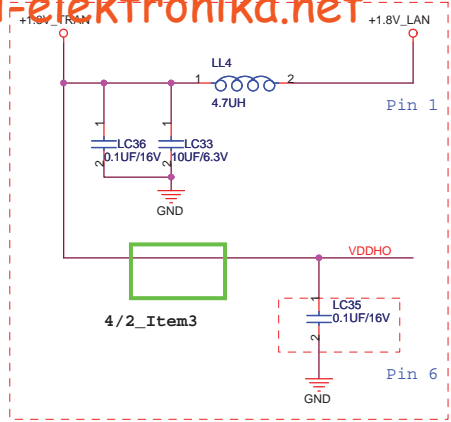
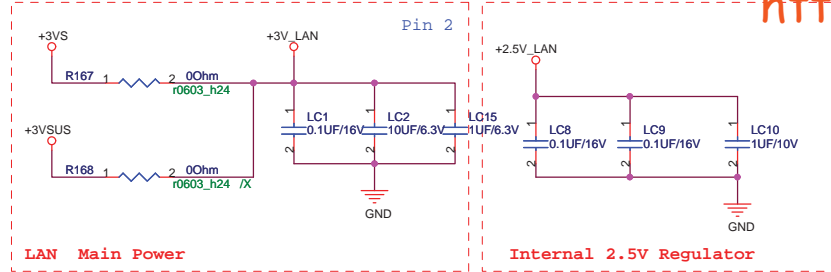
<Variant Name>

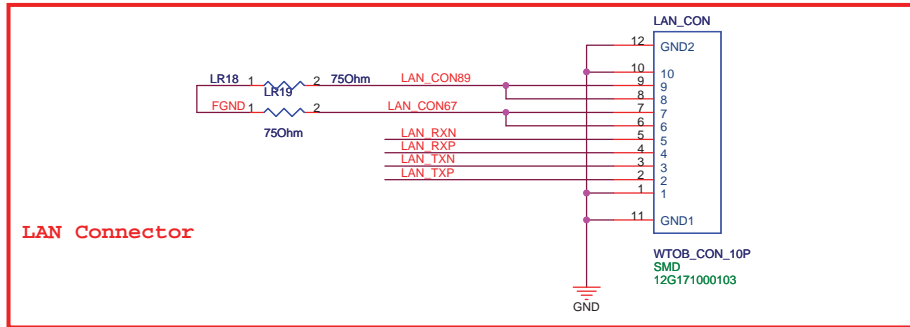
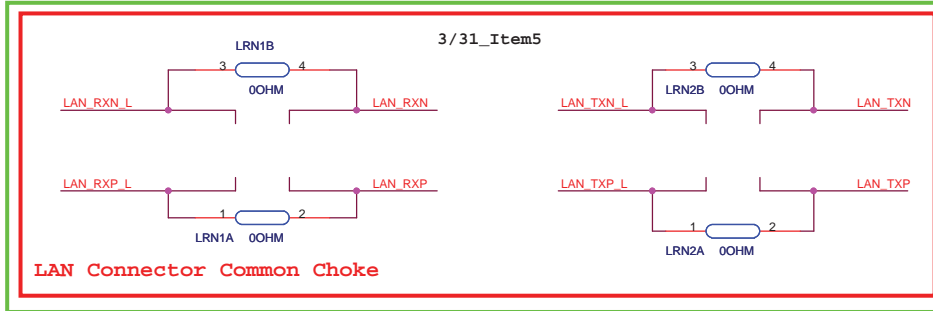
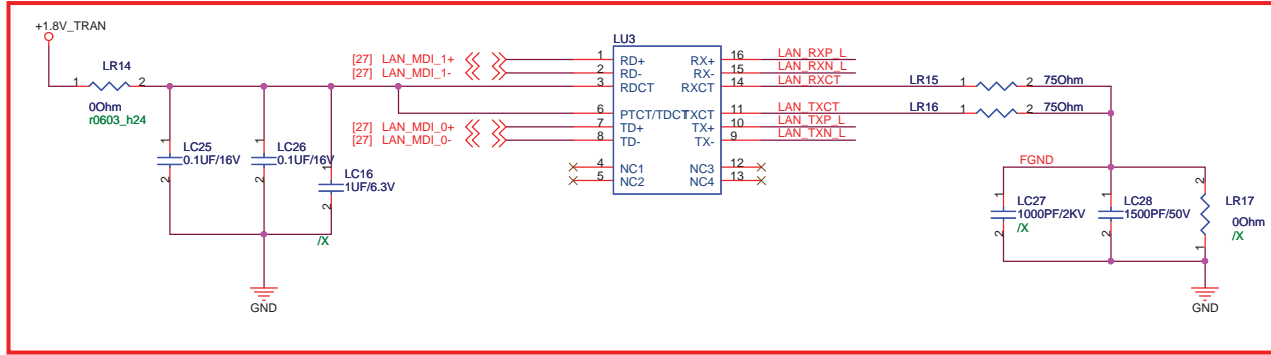
		Title : Bluetooth	
ASUSTek Computer INC.		Engineer: N/A	
Size A	Project Name 1101HA		Rev 1.2
Date: Tuesday, July 21, 2009		Sheet 25 of 50	



<Variant Name>

		Title : FAN_THERMAL SENSOR	
ASUSTek Computer INC.		Engineer: N/A	
Size Custom	Project Name 1101HA	Rev 1.2	
Date: Tuesday, July 21, 2009		Sheet 26 of 50	

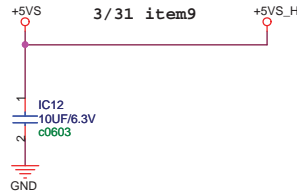




<Variant Name>

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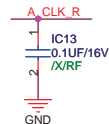
3/25 item4



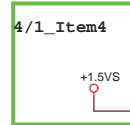
3/27 item8

3/26 item7 FOR RF

Camera USB Common Choke

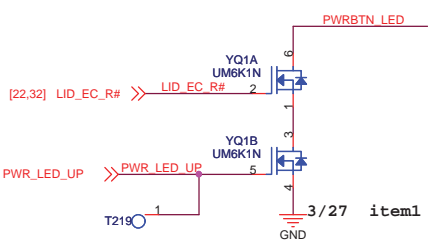
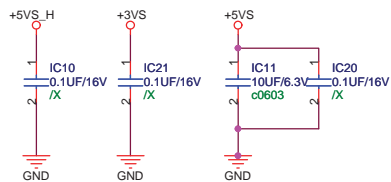
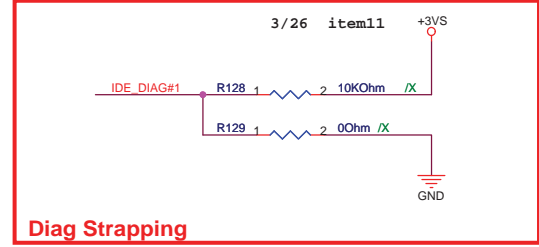
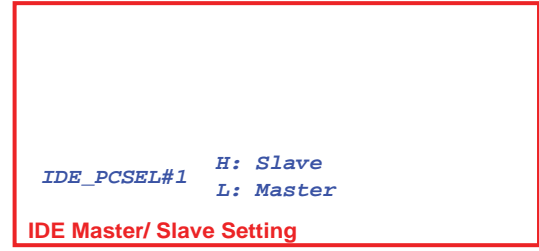
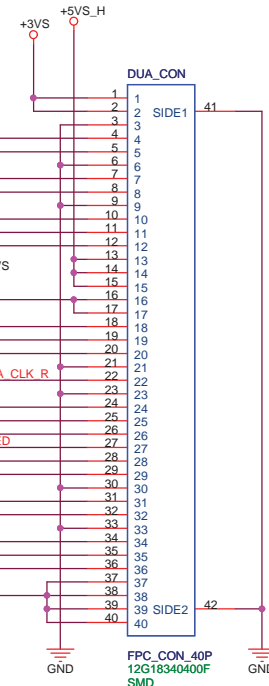


3/30 item6

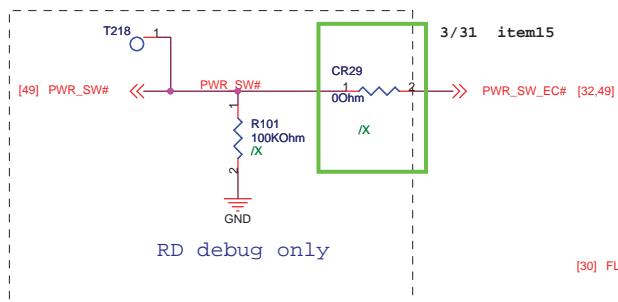
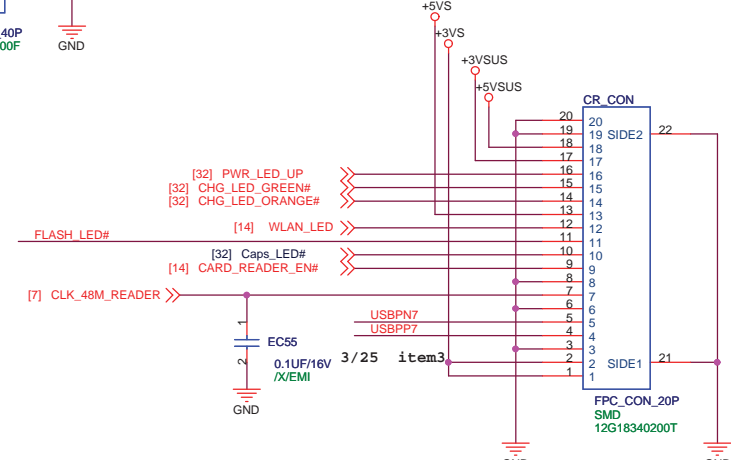


3/25 item3

+3V [14] USB_PN1 [14] USB_PP1

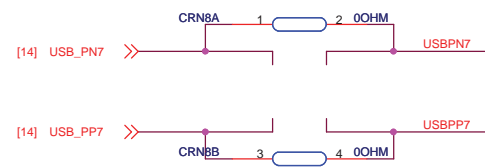


3/25 item2



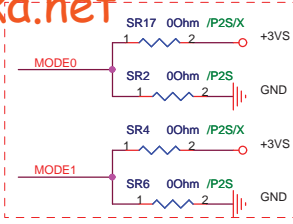
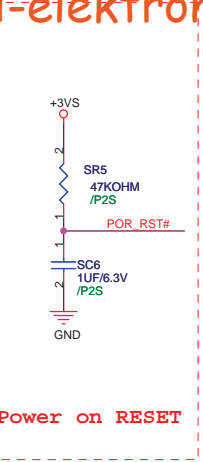
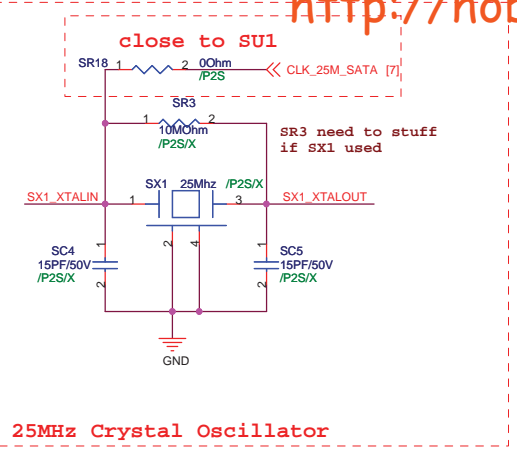
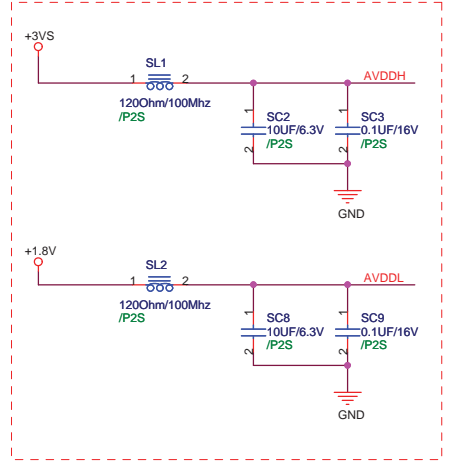
Flash LED

[30] FLASH_LED_S# >> FLASH_LED#

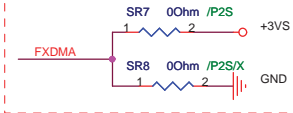


3/26 item11

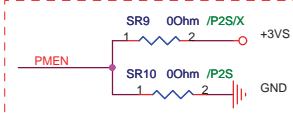
3/25 item3



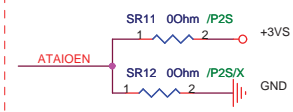
1.MODE[1:0]=Select UDMA speed when FXDMA is set
 00:100MB/s ; 01:133MB/s
 10:150MB/s ; 11:Reserved



2.FXDMA=0,Auto adjustable speed rate according set Feature Command
 FXDMA=1,speed rate depend on Mode[1:0] setting

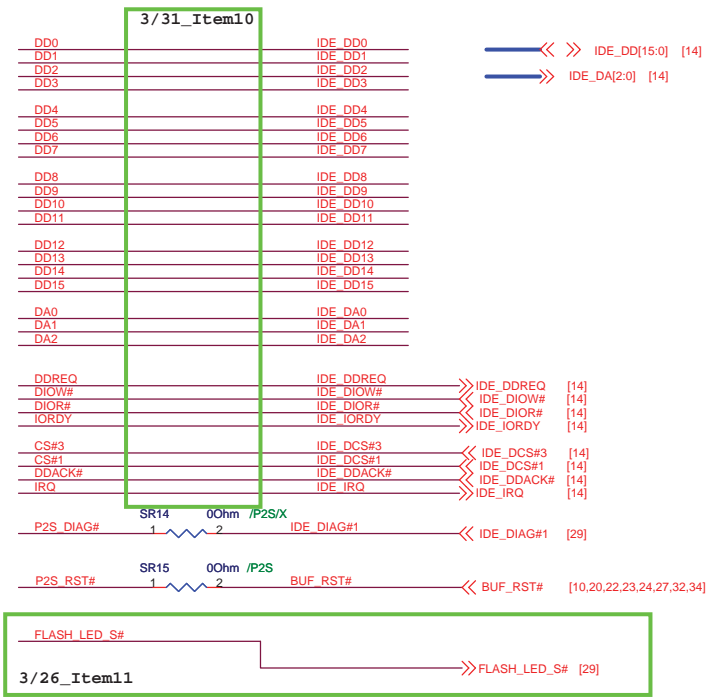
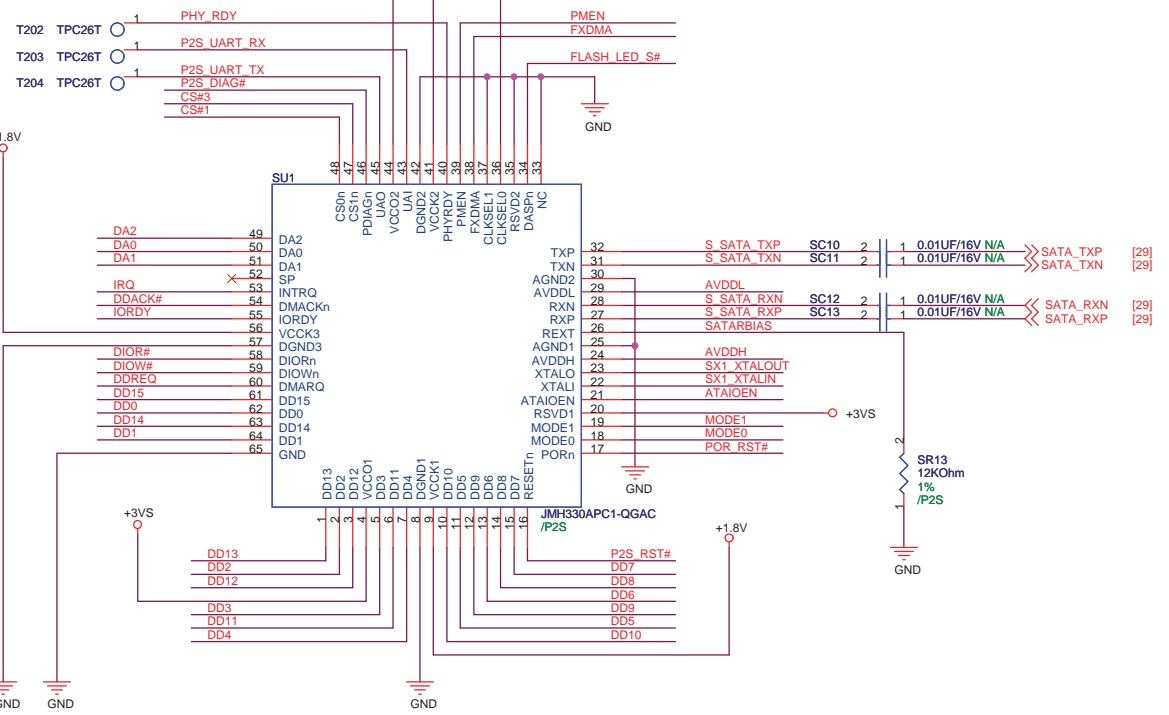
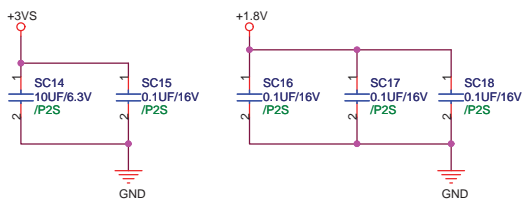


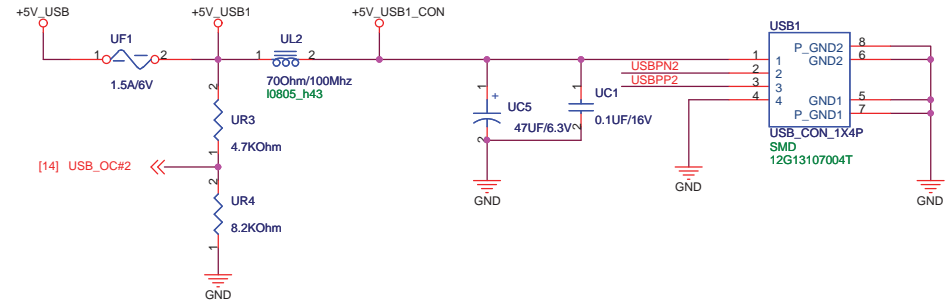
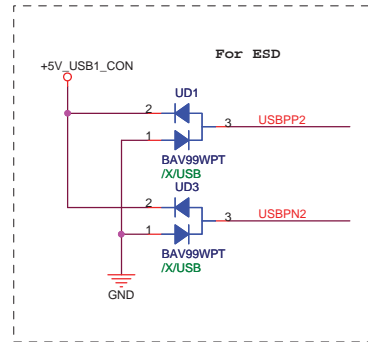
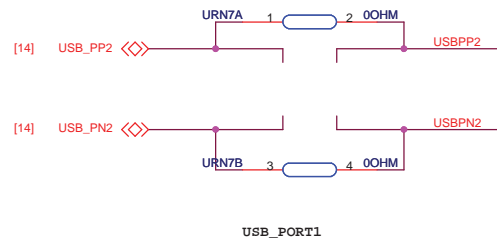
3.PMEN=0 power management function Disable
 PMEN=1 power management function Enable

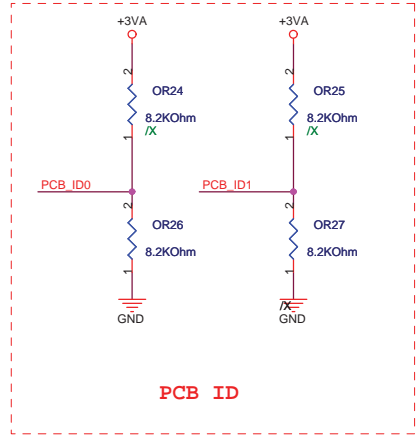
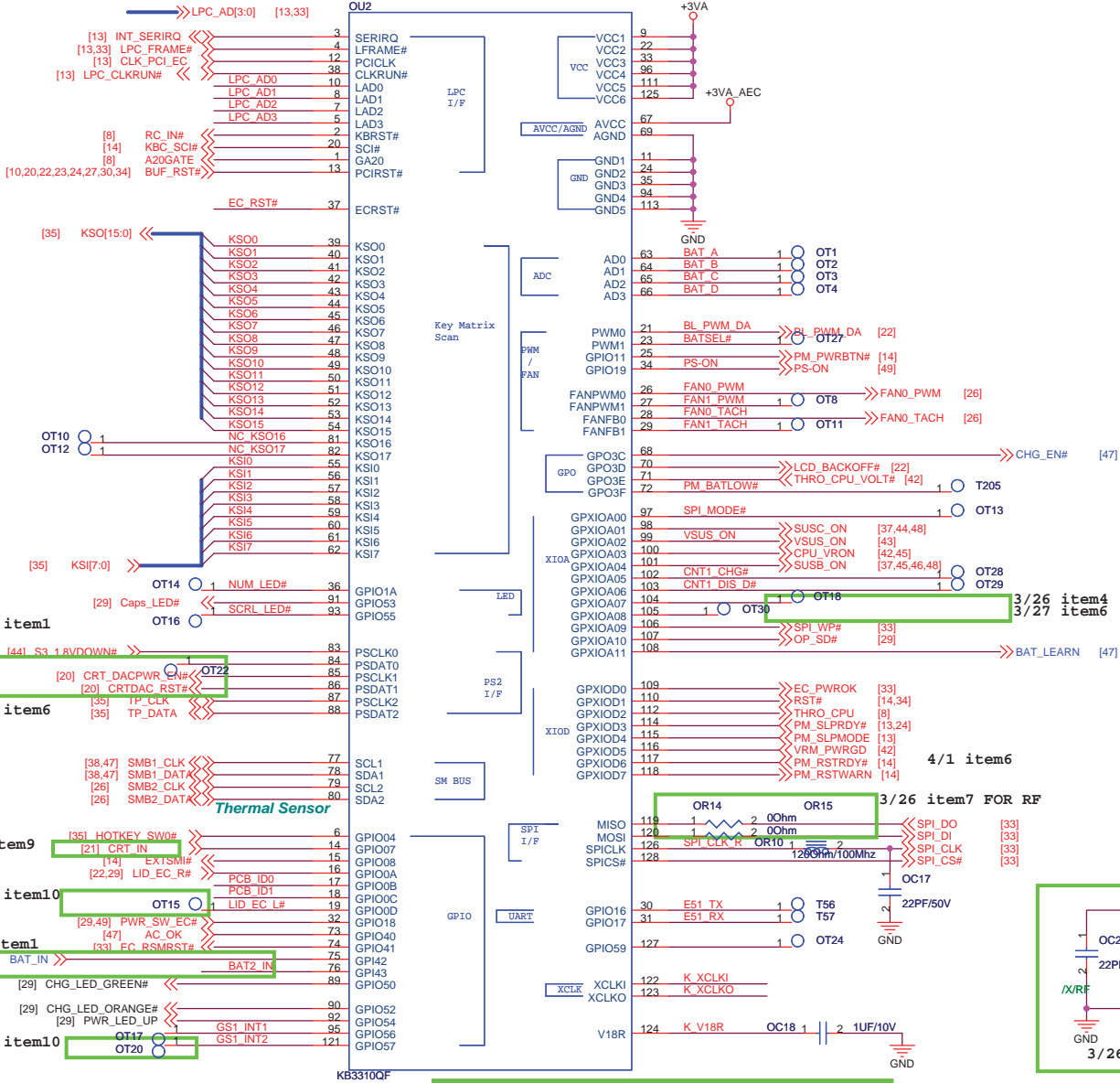
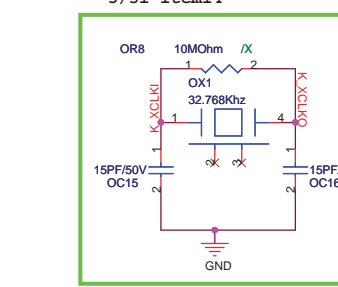
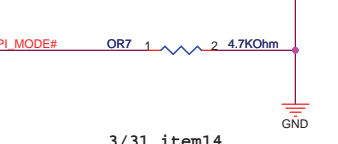
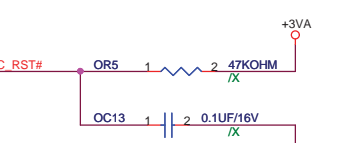
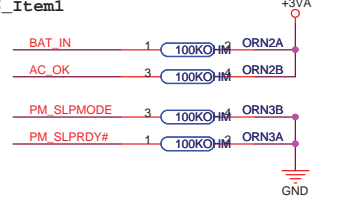
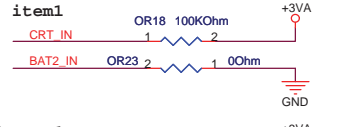
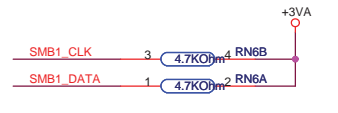
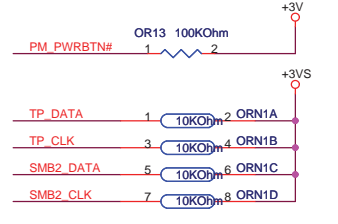
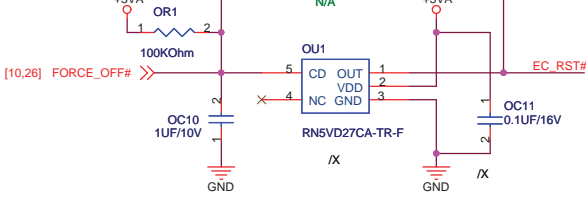
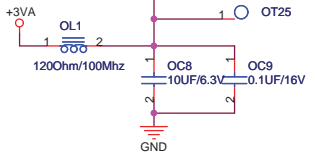
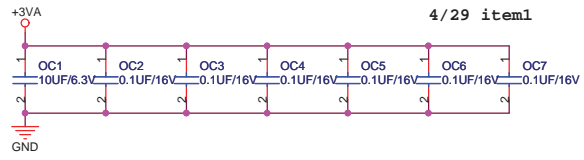


4.ATAIOEN=0,Disable the ATA output pins, ATA I/O output pins are Hi-Z.
 ATAIOEN=1,Enable ATA output

JMH330 only simulate PATA as Device 0

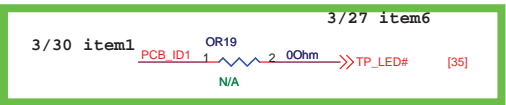
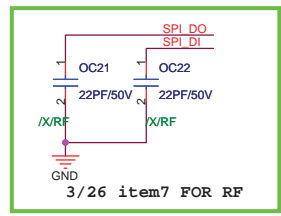






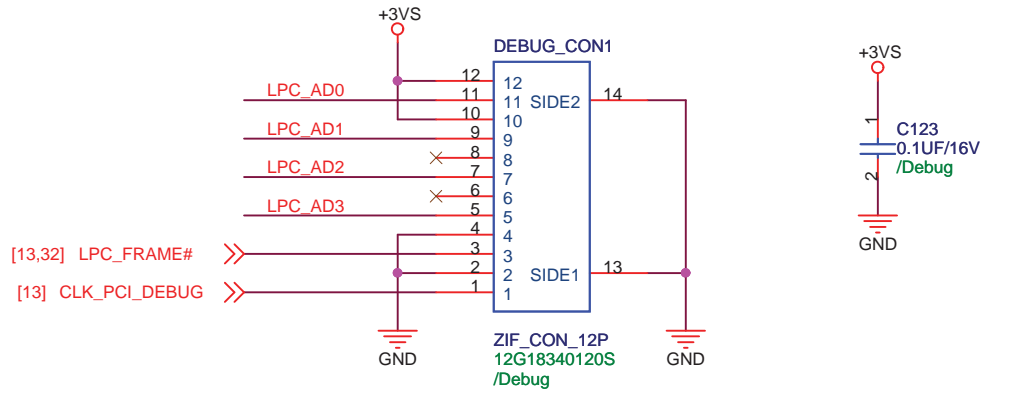
Hotkey Table

Item	Pin Name	Function
0	HOTKEY_SW0#	Home

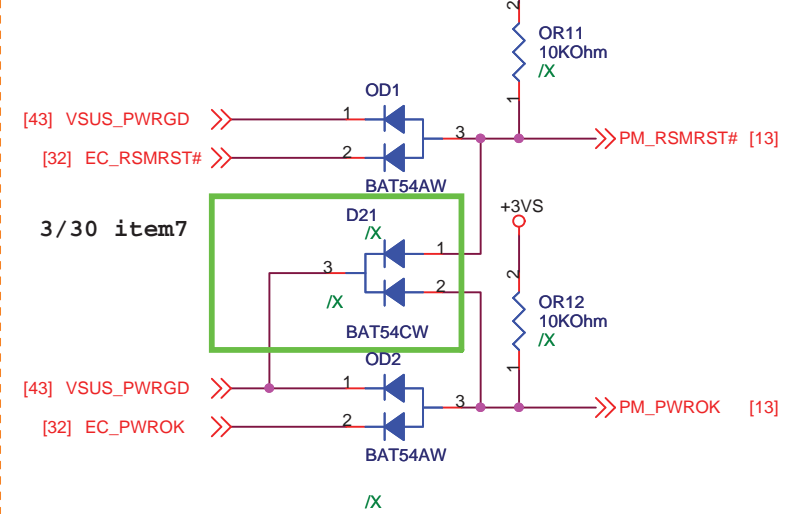


HOTKEY_SW0# - HOTKEY_SW3# internal PU

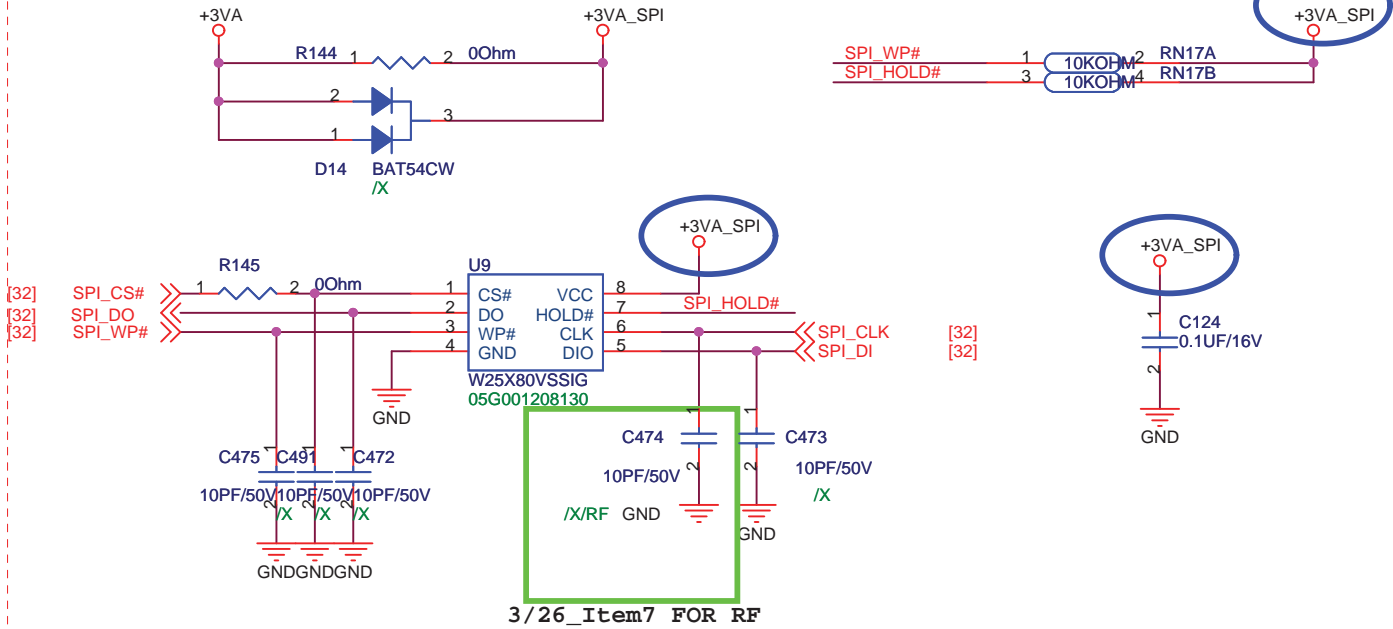
For Debug



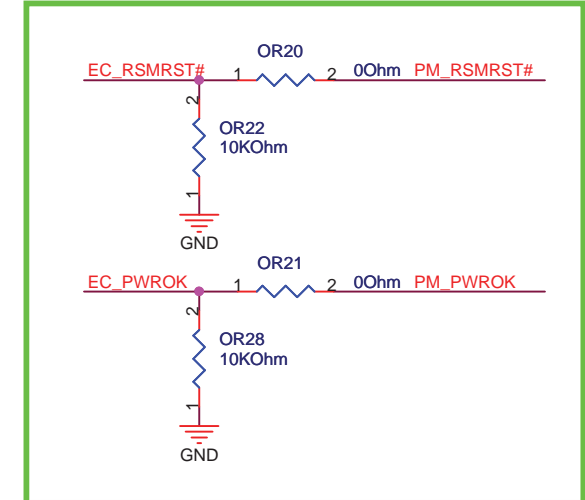
Resolve auto-boot issue



SPI ROM

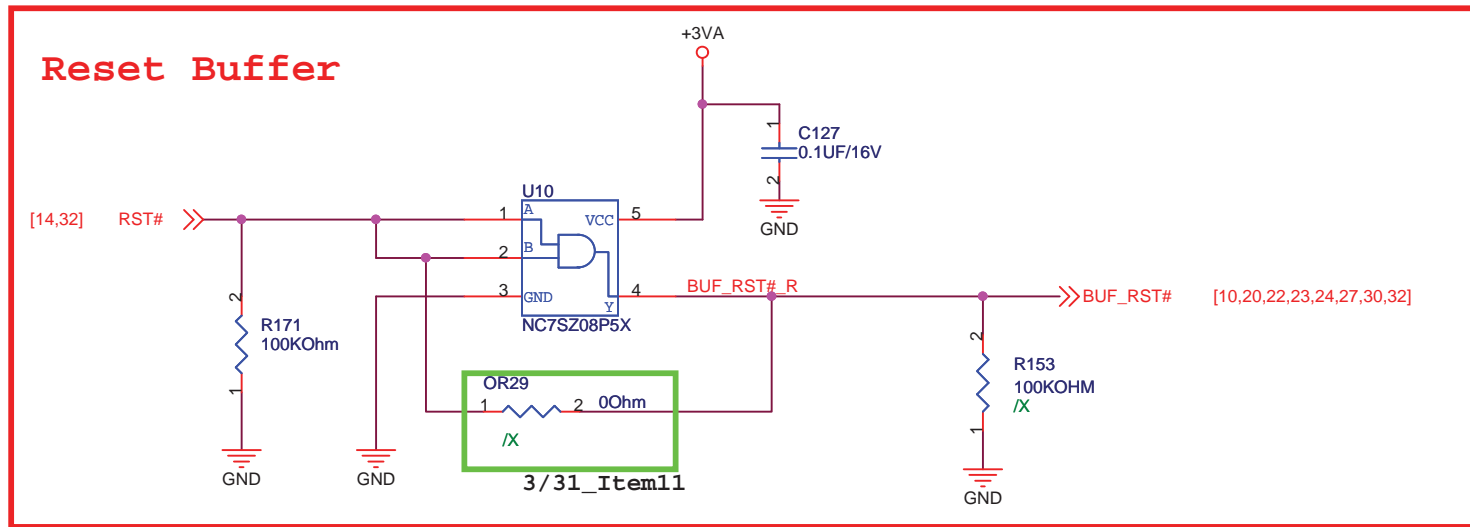
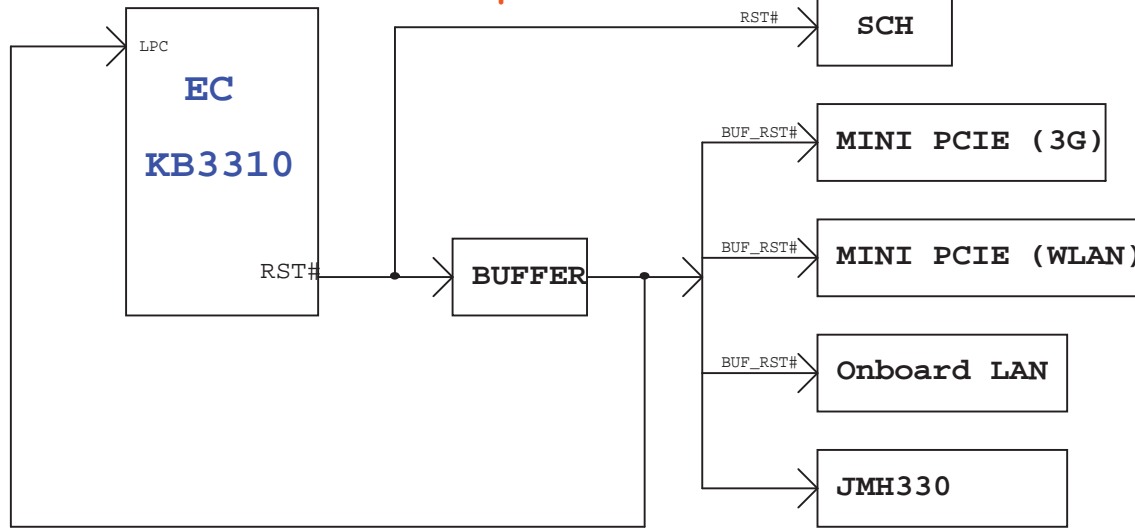


3/30 item7



<Variant Name>

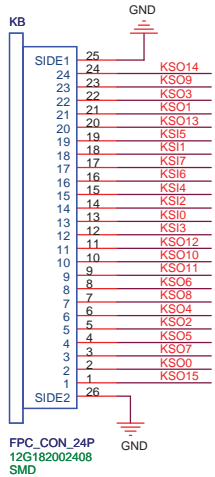
ASUS		Title : SPI ROM/ Debug	
ASUSTek Computer INC.		Engineer: N/A	
Size A4	Project Name 1101HA		Rev 1.2
Date: Tuesday, July 21, 2009	Sheet	33	of 50



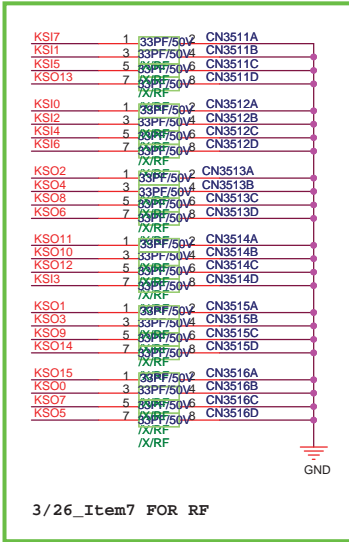
<Variant Name>

		Title : Reset Map
ASUSTeK COMPUTER INC		Engineer: N/A

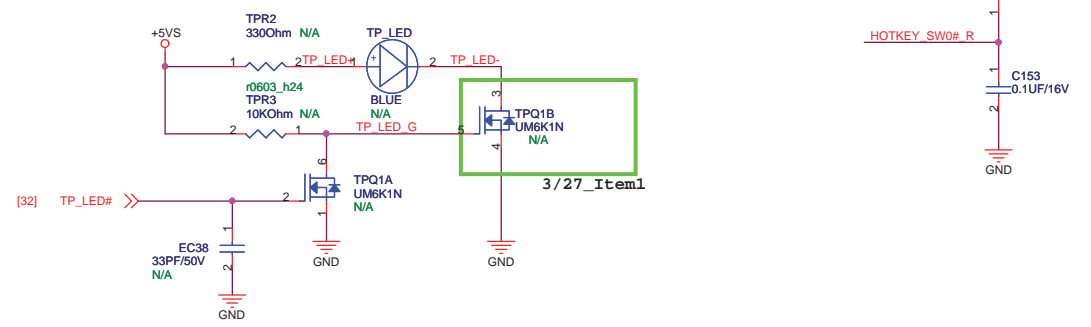
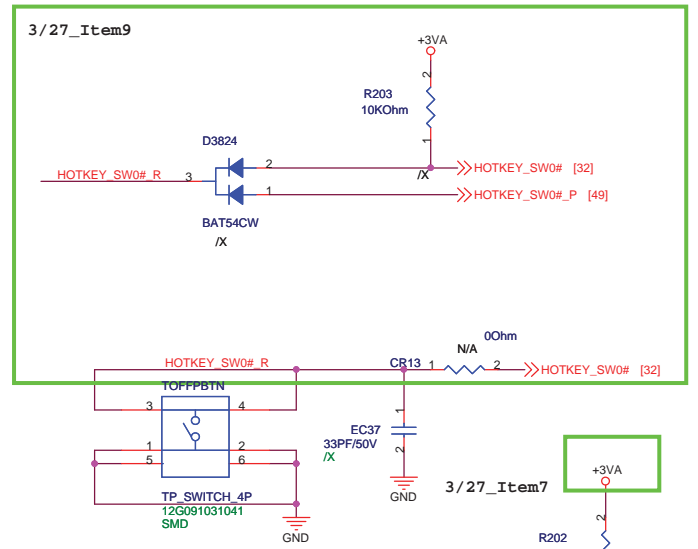
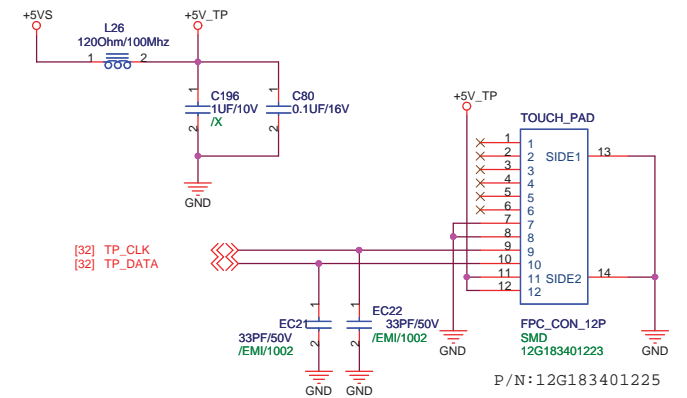
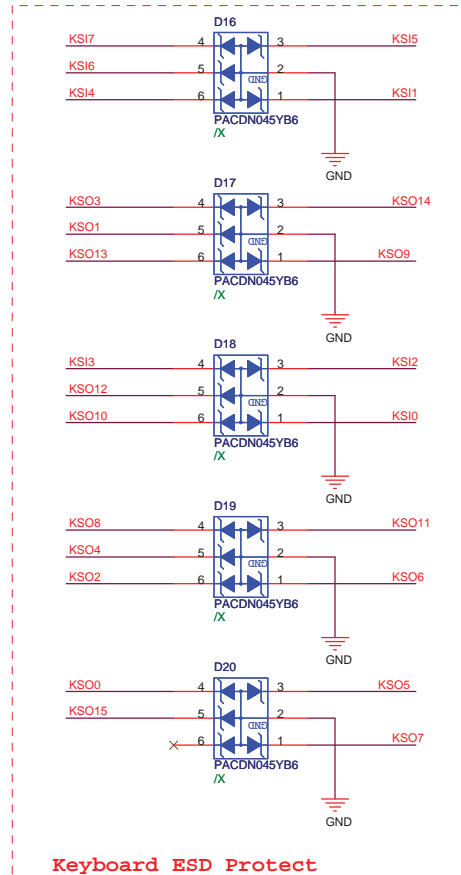
Size	Project Name	Rev
A4	1101HA	1.2




← KSO[15:0] [32]
→ KSI[7:0] [32]

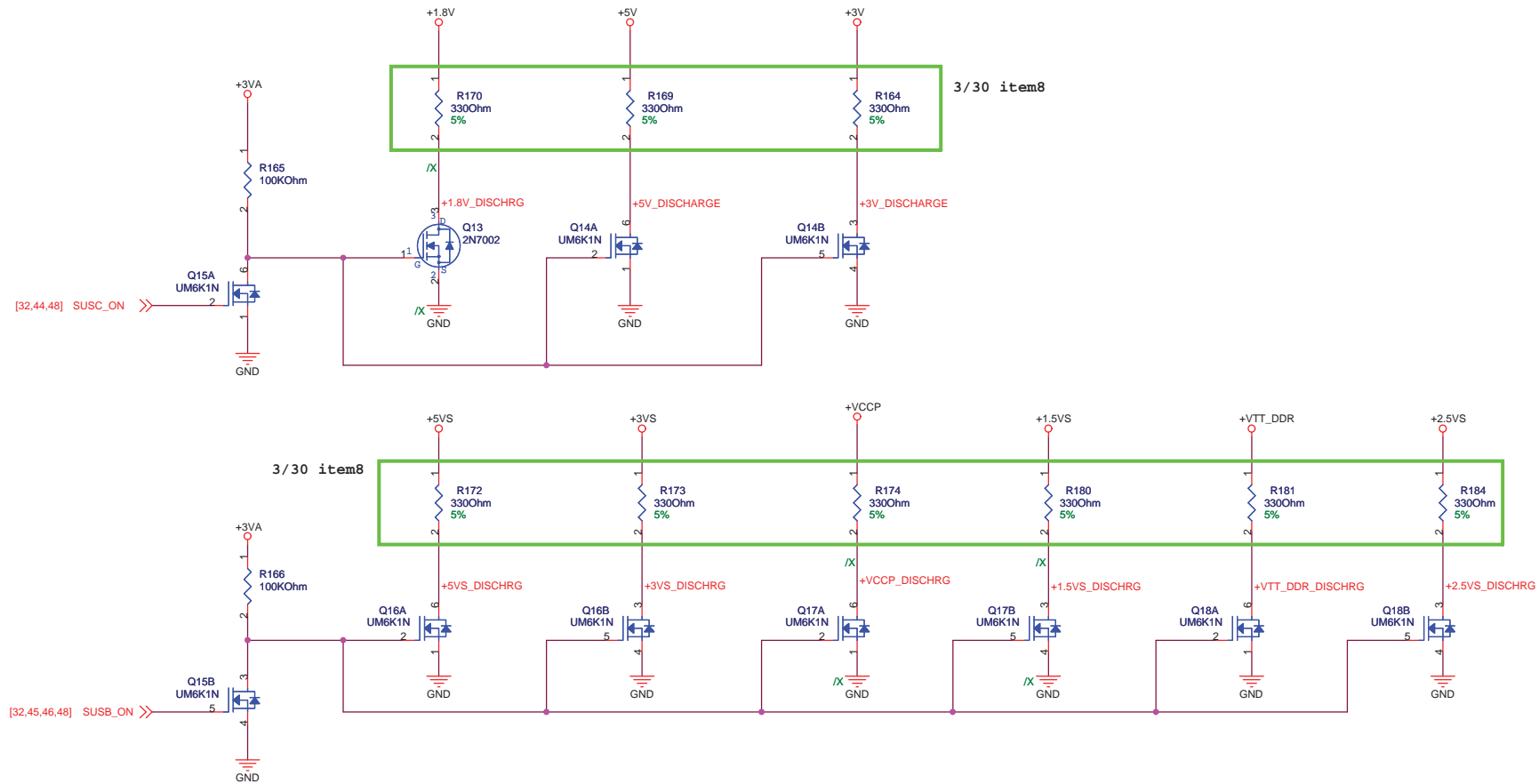


For Keyboard Connector



<Variant Name>

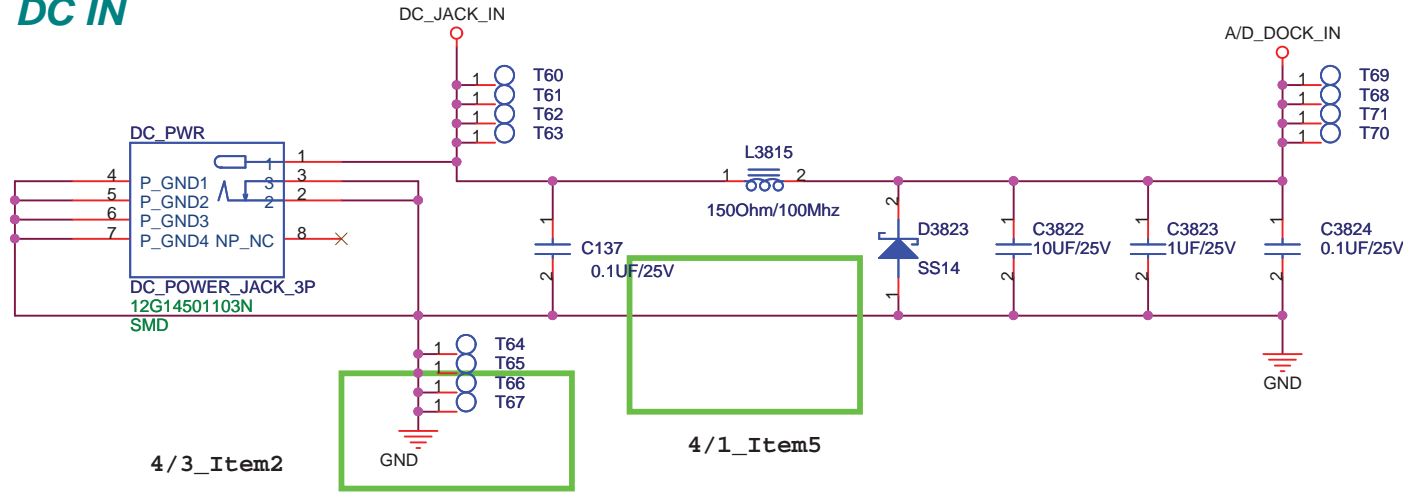
		Title : G-Sensor	
ASUSTek Computer INC.		Engineer: N/A	
Size A4	Project Name 1101HA	Rev 1.2	
Date: Tuesday, July 21, 2009		Sheet	36 of 50



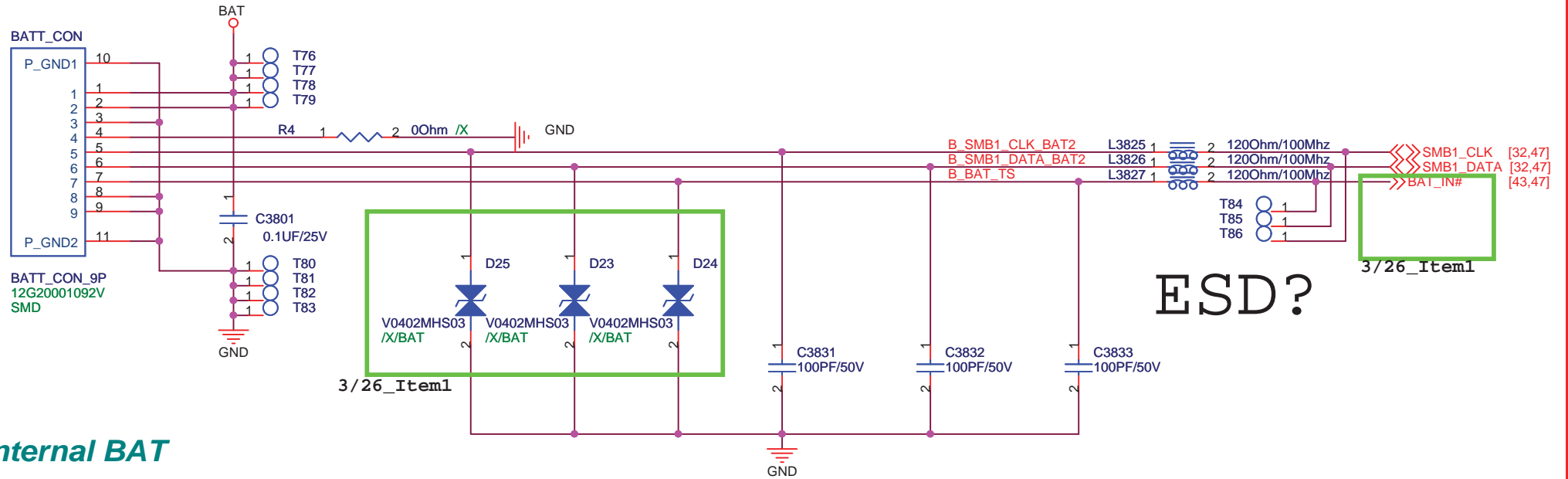
<Variant Name>

ASUS		Title : Discharge
ASUSTek Computer INC.		Engineer: N/A
Size A3	Project Name 1101HA	Rev 1.2
Date: Tuesday, July 21, 2009		Sheet 37 of 50

DC IN



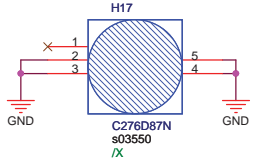
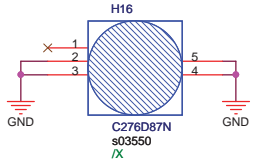
BATT_CON



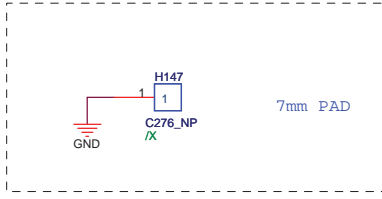
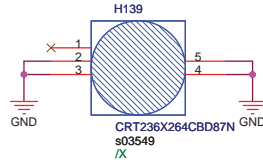
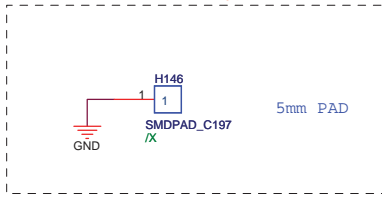
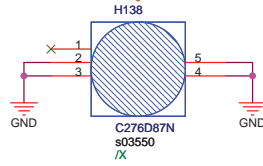
Internal BAT

<Variant Name>

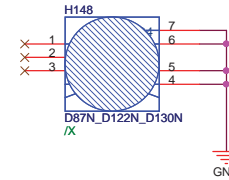
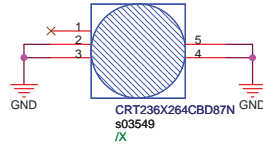
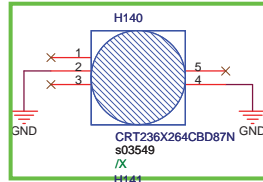
ASUS		Title : PWR Jack	
ASUSTek Computer INC.		Engineer: N/A	
Size A4	Project Name 1101HA		Rev 1.2
Date: Tuesday, July 21, 2009		Sheet	38 of 50



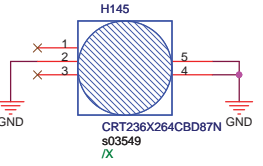
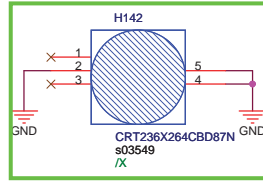
3/27_Item15



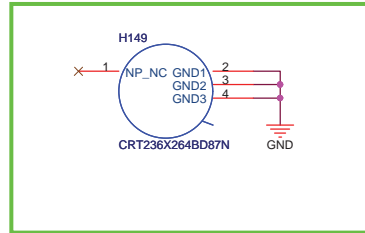
4/3_Item3



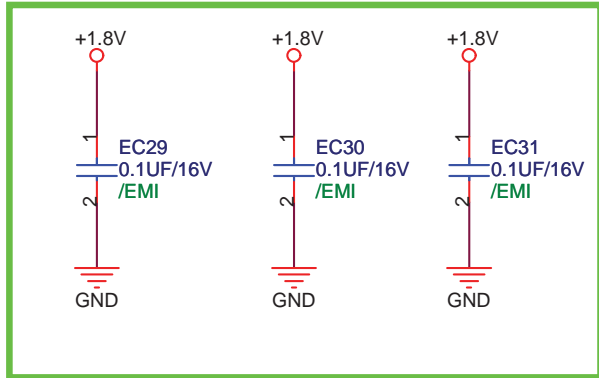
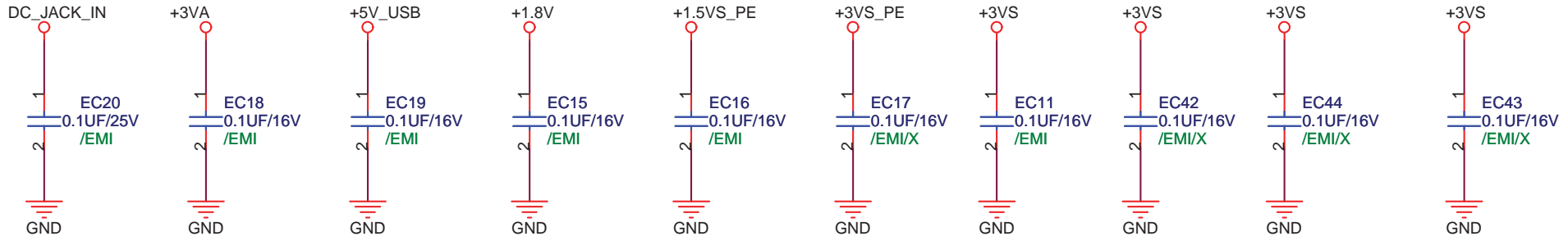
4/8_Item1



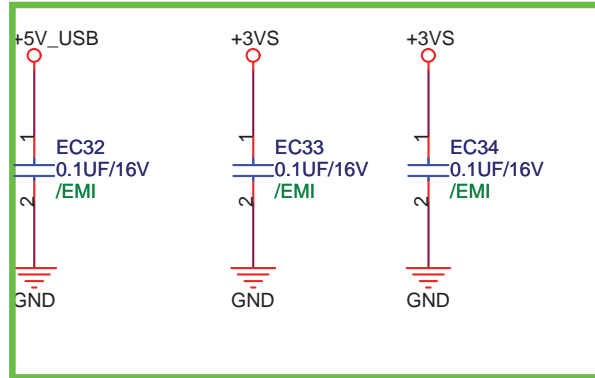
4/6_Item4



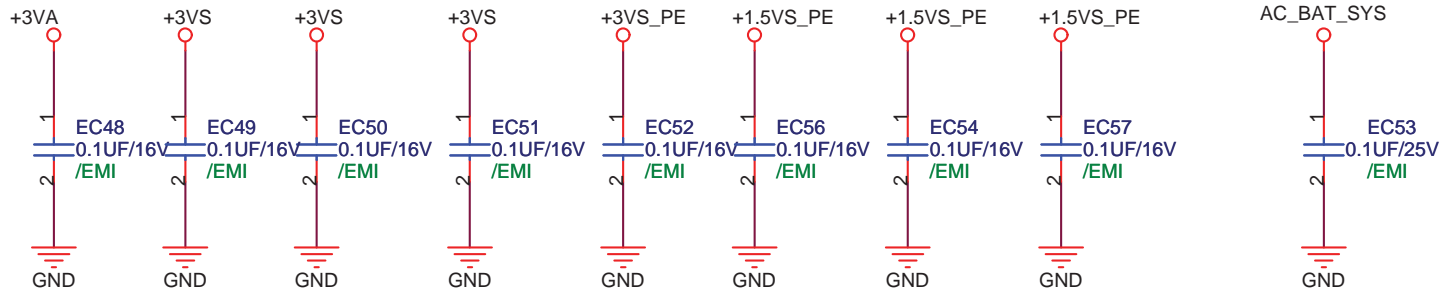
<Variant Name>



4/6_Item1



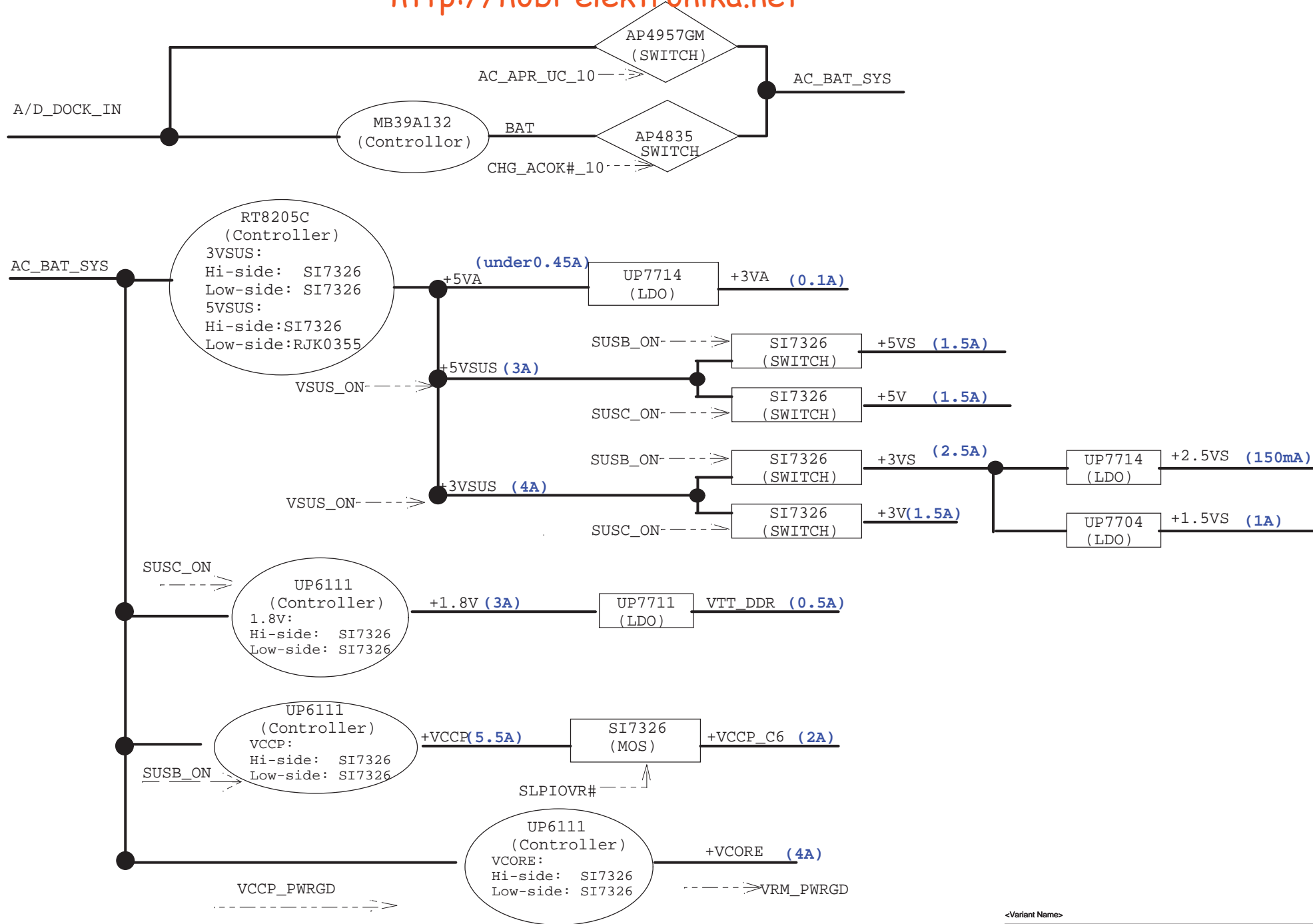
4/6_Item2

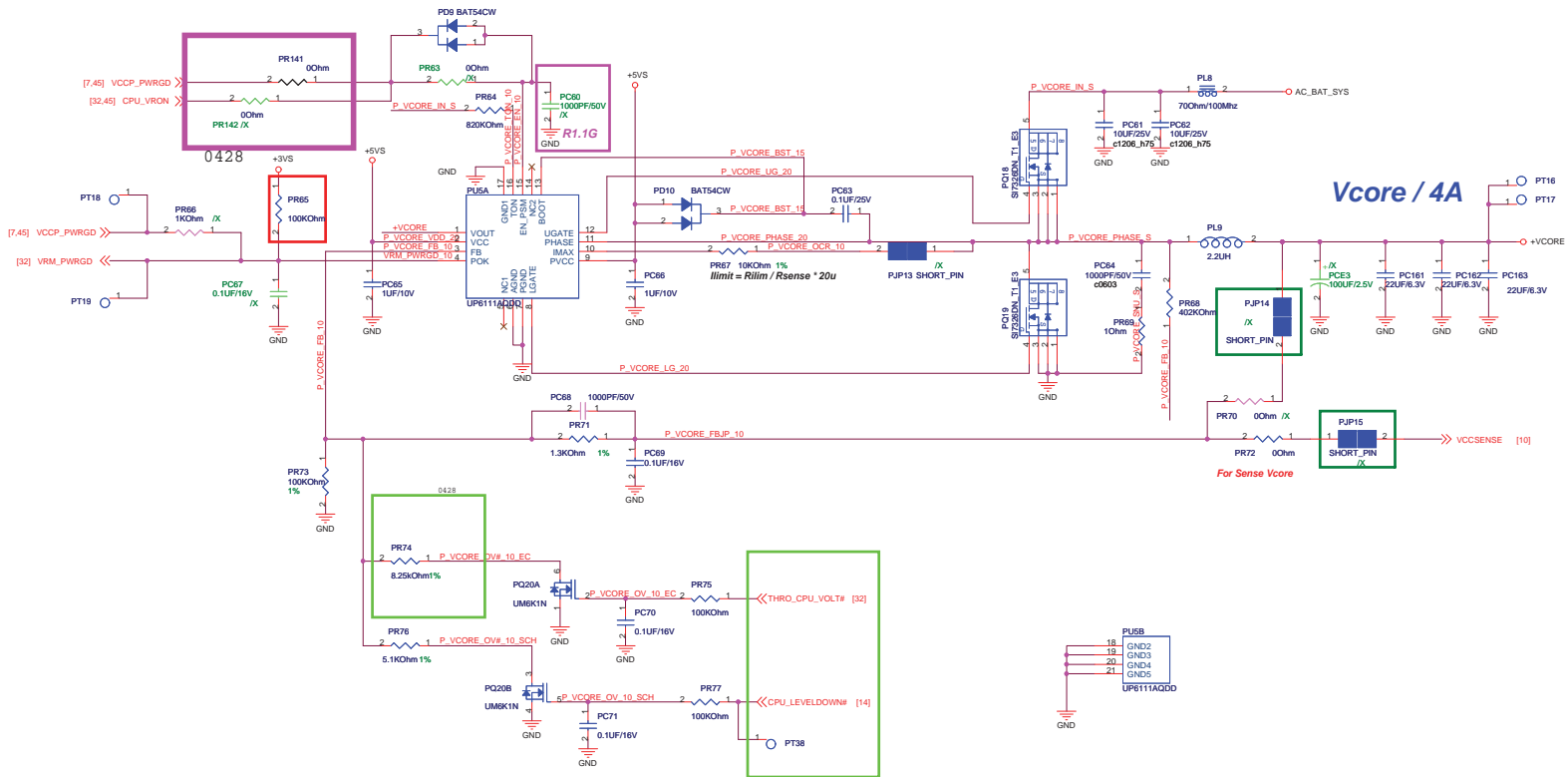


4/8_Item2

<Variant Name>

		Title : EMI	
ASUSTek Computer INC.		Engineer: N/A	
Size A	Project Name 1101HA		Rev 1.2
Date: Tuesday, July 21, 2009		Sheet 40 of 50	





R1.2G

	Status			
	H	L	H	L
THRO_CPU_VOLT#	H	L	H	L
CPU_LEVELDOWN#	H	L	H	L
Voltage	1.068V	0.9502V	0.8775V	0.7597V
	Normal	Normal + Throttle	Power Saving	Power Saving + Throttle

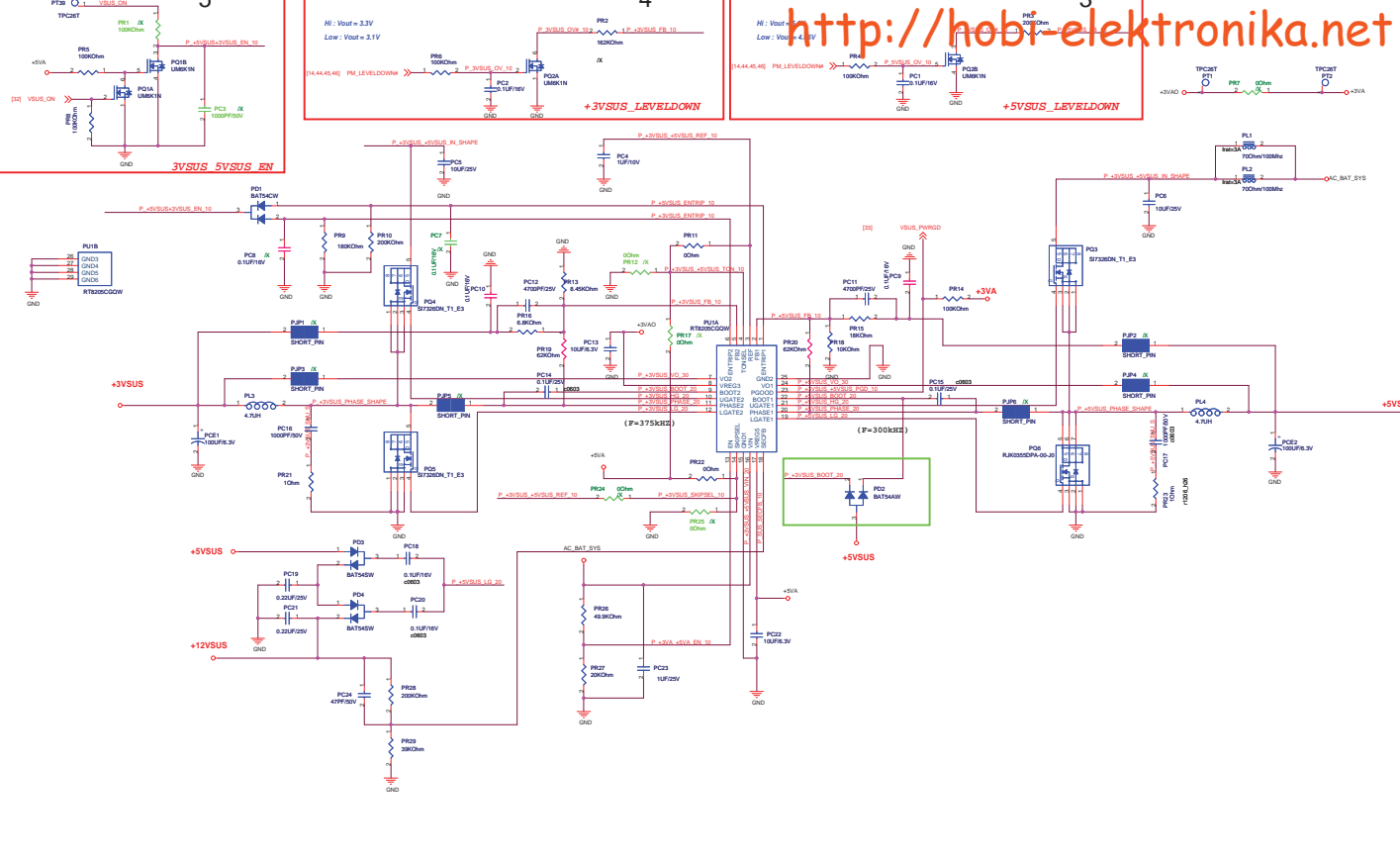
Vcore / 4A

Power stage

- I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 0.47A$
- Ripple Current:**
 $I_{rip} = 1.28A$
 $I_{spec} = 2.5A \cdot 2 \text{ pcs}$
- Dynamic:**
 $I_{peak} = 4A$
 $ESR / 1 \text{ pcs} = 18 \text{ mohm}$
 $\Delta V = 72mV$
- Inductor Spec:**
 $I_{sat} = 14A$
 $I_{dc} = 8A$
 $DCR = 18 \text{ mohm}$
- MOSFET Spec:**
H-side MOSFET: SI7326DN_T1_E3
 $R_{ds(ON)} = 22 \text{ mohm}$ ($V_{gs} = 4.5V$)
 $I_{cont} = 6.5A$ ($T = 25^\circ C$)
 $I_{peak} = 40A$ (Pause < 10 us)
L-side MOSFET: SI7326DN_T1_E3
 $R_{ds(ON)} = 22 \text{ mohm}$ ($V_{gs} = 4.5V$)
 $I_{cont} = 6.5A$ ($T = 25^\circ C$)
 $I_{peak} = 40A$ (Pause < 10 us)

Controller

- Voltage & Current:**
 $+0.7598 \sim 1.048V @ 4A$
- Frequency:**
 $PR7 = 1M \text{ ohm}$ $F_{osc} = 250KHz$
- OCP:**
 $PR13 = 10K \text{ ohm} \rightarrow 9.09A$
- POR:**
 $POR \text{ Hysteresis} = 0.2V$
 $V_{on} = 3.9V$
- UVP:**
 $V_{out} * 70\%$
- OVP:**
 $V_{out} * 115\%$
- Enable Voltage:**
 $V = 2.9V$
- Soft start time:**
 $T_{ss} = 1.2ms$
- Phase selection:**
N/A
- Inrush Current:**
 $C_{total} = 100 \mu F$
 $I_{inrush} = 0.088A$

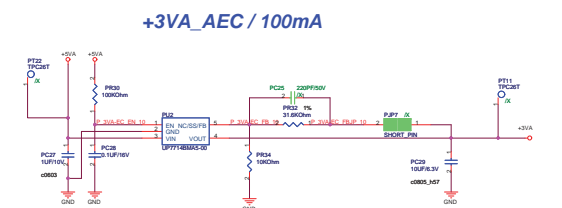
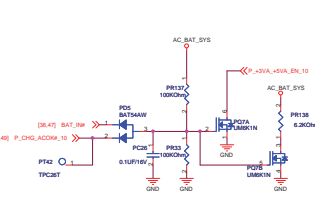


Power stage	+3VSUS
1. I/P Current:	$I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 1.832A$
2. Ripple Current:	$I_{rip} = 1.92A$ $I_{spec} = 2.5A \times 1 \text{ pcs}$
3. Dynamic:	$I_{peak} = 4A$ $ESR / 1 \text{ pcs} = 18 \text{ mohm}$ $\Delta V = 72mV$
4. Inductor Spec:	$I_{sat} = 10A$ $I_{dc} = 5.5A$ $DCR = 37 \text{ mohm}$
5. MOSFET Spec:	H-side MOSFET: SI7326DN_T1_E3 $R_{ds(ON)} = 22 \text{ mohm}$ ($V_{gs} = 4.5V$) $I_{cont} = 6.5A$ ($T = 25^\circ C$) $I_{peak} = 40A$ (Pause < 10 us)
	L-side MOSFET: SI7326DN_T1_E3 $R_{ds(ON)} = 22 \text{ mohm}$ ($V_{gs} = 4.5V$) $I_{cont} = 6.5A$ ($T = 25^\circ C$) $I_{peak} = 40A$ (Pause < 10 us)

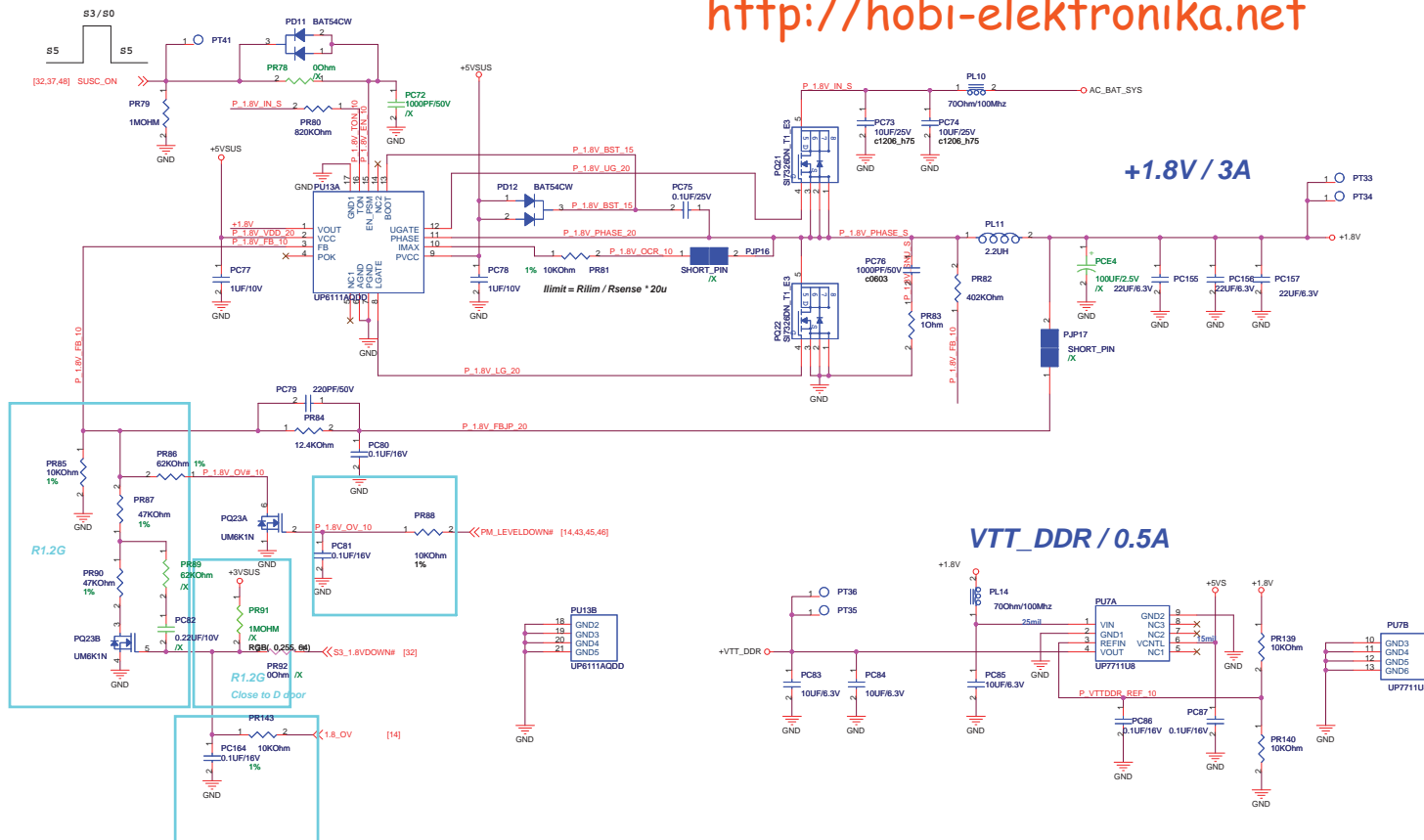
Power stage	+5VSUS
1. I/P Current:	$I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 2.082A$
2. Ripple Current:	$I_{rip} = 1.482A$ $I_{spec} = 2.5A \times 1 \text{ pcs}$
3. Dynamic:	$I_{peak} = 3A$ $ESR / 1 \text{ pcs} = 18 \text{ mohm}$ $\Delta V = 54mV$
4. Inductor Spec:	$I_{sat} = 10A$ $I_{dc} = 5.5A$ $DCR = 37 \text{ mohm}$
5. MOSFET Spec:	H-side MOSFET: SI7326DN_T1_E3 $R_{ds(ON)} = 22 \text{ mohm}$ ($V_{gs} = 4.5V$) $I_{cont} = 6.5A$ ($T = 25^\circ C$) $I_{peak} = 40A$ (Pause < 10 us)
	L-side MOSFET: RJK0355DPA-00-J0 WPAK $R_{ds(ON)} = 11.8 \text{ mohm}$ ($V_{gs} = 4.5V$) $I_{cont} = 30A$ ($T = 25^\circ C$) $I_{peak} = 120A$ (Pause < 10 us)

Controller	+3VSUS
1. Voltage & Current:	$+3VSUS = 3.3V @ 4A$
2. Frequency:	$f_{osc} = 375KHz$
3. OCP:	Set $PR9 = 180Kohm$ $I_{ocp} = 8.18A$
4. POR:	$V_{on} = 4.35 - 4.5V$ $V_{off} = 3.9 - 4.25V$
5. UVP:	$V_{uvp} = 70\% V_{out}$
6. OVP:	$V_{ovp} = 115\% V_{out}$
7. Enable Voltage:	$V_{rising} = 1V$ $V_{falling} = 0.4V$
8. Soft start time:	$T_{ss} = 2ms$
9. Phase selection:	/X
10. Inrush Current:	$C_{total} = 110 \mu F$ $I_{inrush} = 0.165A$

Controller	+5VSUS
1. Voltage & Current:	$+5VSUS = 5V @ 3A$
2. Frequency:	$f_{osc} = 300KHz$
3. OCP:	Set $PR8 = 200Kohm$ $I_{ocp} = 17A$
4. POR:	$V_{on} = 4.35 - 4.5V$ $V_{off} = 3.9 - 4.25V$
5. UVP:	$V_{uvp} = 70\% V_{out}$
6. OVP:	$V_{ovp} = 115\% V_{out}$
7. Enable Voltage:	$V_{rising} = 1V$ $V_{falling} = 0.4V$
8. Soft start time:	$T_{ss} = 2ms$
9. Phase selection:	/X
10. Inrush Current:	$C_{total} = 110 \mu F$ $I_{inrush} = 0.275A$



1. Dropout Voltage:	$\Delta V = 210mV$ ($I_o = 300mA$)
2. Current Limit:	$I_{limit} = 480mA$
3. Continue Current:	$I_{cont} = 100mA$
4. Pd:	$R_{thjc} = 5C/W$ $P_d = 0.4W$
5. EN Voltage:	$V_{rising} = 2V$ $V_{falling} = 0.8V$
6. Supply Voltage:	$V_{cc} = 3.3V$
7. Inrush current:	$T_{ss} = 400us$ $C_{total} = 10 \mu F$ $I_{inrush} = 62.5mA$

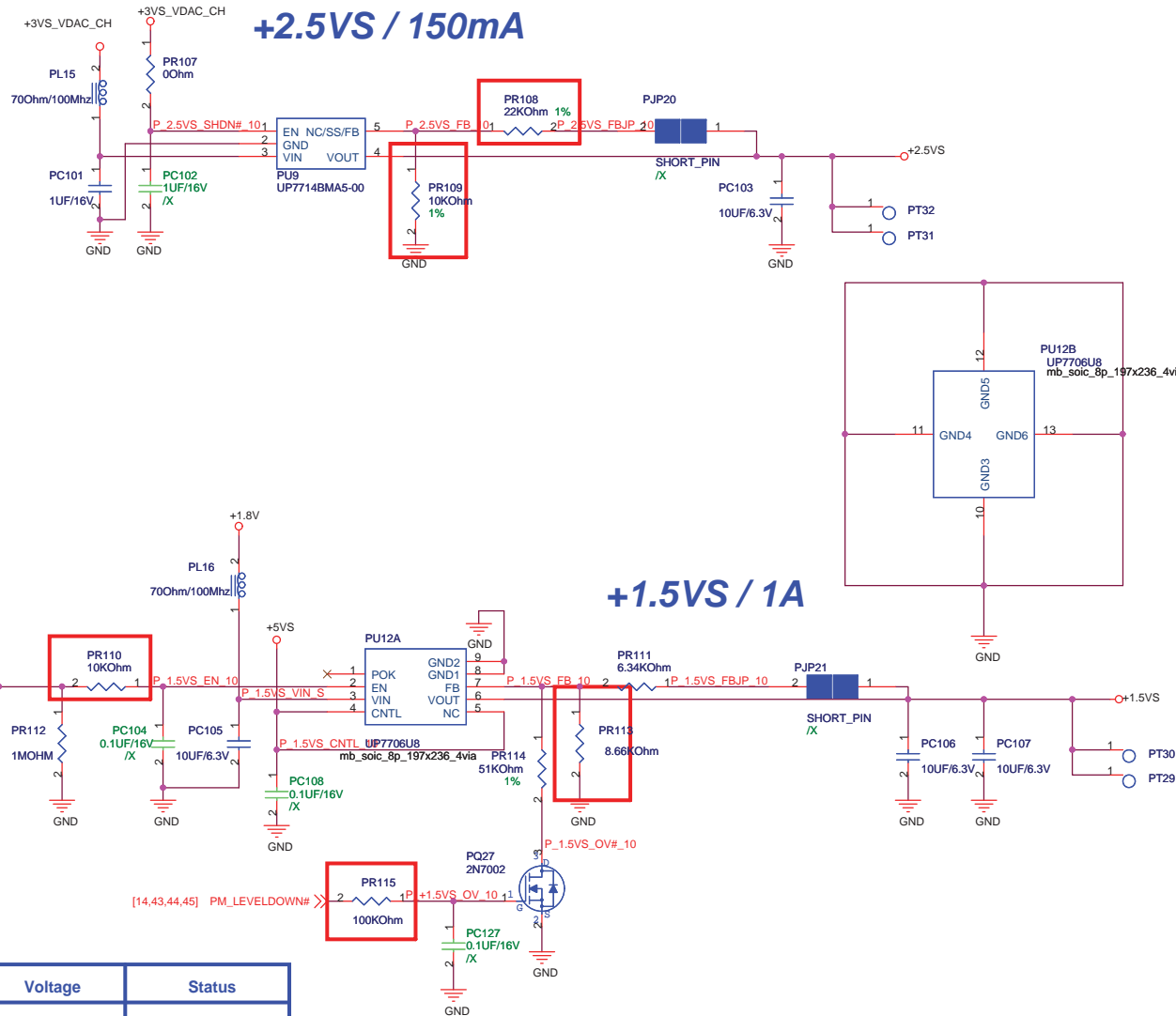


- ### Power stage
- I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 0.75A$
 - Ripple Current:**
 $I_{rip} = 1.2A$
 $I_{spec} = 2.5A \cdot 1 pcs$
 - Dynamic:**
 $I_{peak} = 3A$
 $ESR / 1 pcs = 18 mohm$
 $\Delta V = 54mV$
 - Inductor Spec:**
 $I_{sat} = 14 A$
 $I_{dc} = 8 A$
 $DCR = 18 mohm$
 - MOSFET Spec:**
H-side MOSFET: SI7326DN_T1_E3
 $R_{ds(ON)} = 22 mohm$ ($V_{gs} = 4.5 V$)
 $I_{cont} = 6.5 A$ ($T = 25 ^\circ C$)
 $I_{peak} = 40 A$ (Pause < 10 us)
L-side MOSFET: SI7326DN_T1_E3
 $R_{ds(ON)} = 22 mohm$ ($V_{gs} = 4.5 V$)
 $I_{cont} = 6.5 A$ ($T = 25 ^\circ C$)
 $I_{peak} = 40 A$ (Pause < 10 us)

1.8_OV	PM_LEVELDOWN#	Voltage	Status
L	L	1.65V	Power Saving
L	H	1.795V	Normal
H	H	1.89V	Super performance
H	L	1.746V	

- ### +VTTDDR@1A
- Dropout Voltage:**
 $\Delta V = 0.3V$ ($I_o = 2 A$)
 - Current Limit:**
 $I_{limit} = 4 A$
 - Continue Current:**
 $I_{cont} = 3 A$
 - Power Dissipation:**
 $R_{thjc} = 52 ^\circ C/W$
 $P_d = 1.9 W$
 - EN Voltage:**
 $V_{en} = 1.4V$
 $V_{sd} = 0.8 V$
 - Supply Voltage:**
 $V_{cc} = 5 V$
 - Inrush current:**
 $T_{ss} = 5 ms$
 $C_{total} = 20 \mu F$
 $I_{inrush} = 3.6 mA$

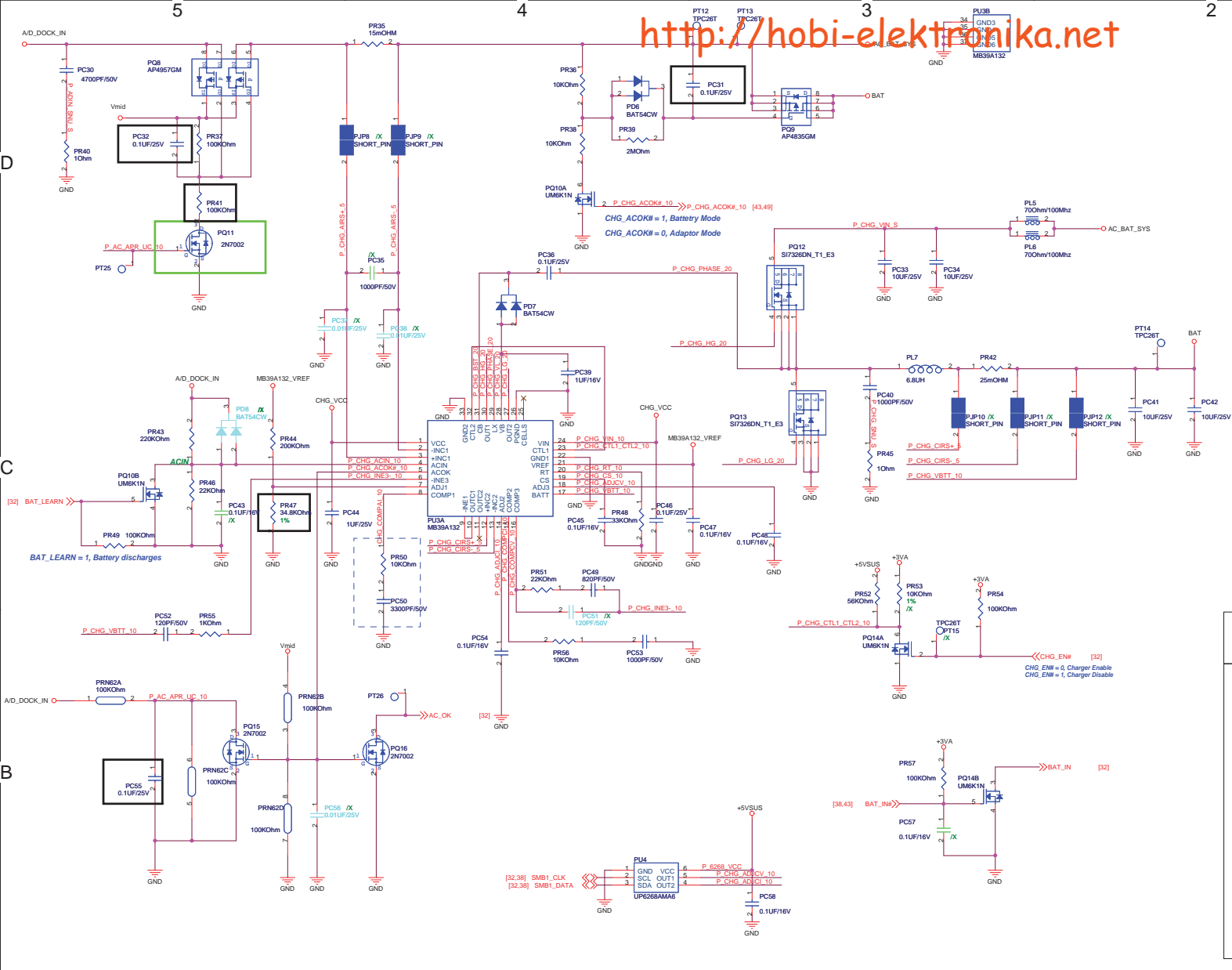
- ### Controller
- Voltage & Current:**
 $+1.8V @ 3A$
 - Frequency:**
 $PR80 = 820K ohm$
 $F_{osc} = 300KHz$
 - OCP:**
 $PR184 = 10K ohm \rightarrow 9A$
 - POR:**
 $V_{ccrth} = 3.7 \sim 4.1V$
 $V_{ccchys} = 0.2V$
 - UVP:**
 $V_{out} * 70\%$
 - OVP:**
 $V_{out} * 115\%$
 - Enable Voltage:**
 $V = 2.9V$
 - Soft start time:**
 $T_{ss} = 1.2 ms$
 - Phase selection:**
 $/X$
 - Inrush Current:**
 $C_{total} = 100 \mu F$
 $I_{inrush} = 0.15 A$



- | | |
|---|--|
| 1. Dropout Voltage:
$\Delta V = 210\text{mV}$ ($I_o = 300\text{mA}$) | 5. EN Voltage:
V rising = 2 V
V falling = 0.8 V |
| 2. Current Limit:
I limit = 480mA | 6. Supply Voltage:
Vcc = 3.3V |
| 3. Continue Current:
I cont = 150mA | 7. Inrush current:
Tss = 400us
C total = 10 uF
I inrush = 62.5 mA |
| 4. Pd:
R thjc = 5 C/W
Pd = 0.4W | |

- | | |
|--|---|
| 1. Dropout Voltage:
$\Delta V = 300\text{mV}$ ($I_o = 2\text{A}$) | 5. EN Voltage:
V rising = 1.4 V
V falling = 0.4 V |
| 2. Current Limit:
I limit = 2.8 A | 6. Supply Voltage:
Vcc = 5V |
| 3. Continue Current:
I cont = 1A | 7. Inrush current:
Tss = 4 ms
C total = 20 uF
I inrush = 7.5mA |
| 4. Pd:
R thjc = 5 C/W
Pd = 1.9W | |

PM_LEVELDOWN#	Voltage	Status
L	1.38V	Power Saving
H	1.48V	Normal

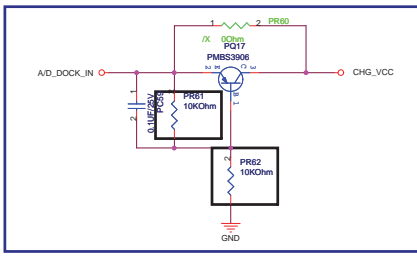


Power stage

- I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 1.64A$
- Ripple Current:**
 $I_{rip} = 1.18A$
 $I_{spec} = 2A \times 1 \text{ pcs}$
- Inductor Spec:**
 $I_{sat} = 10 A$
 $I_{dc} = 5.5A$
 $DCR = 37 \text{ mohm}$
- MOSFET Spec:**
H-side MOSFET: SI7326DN_T1_E3
 $R_{ds(ON)} = 22 \text{ mohm}$ ($V_{gs} = 4.5 V$)
 $I_{cont} = 6.5 A$ ($T = 25^\circ C$)
 $I_{peak} = 40 A$ (Pause < 10 us)
L-side MOSFET: SI7326DN_T1_E3
 $R_{ds(ON)} = 22 \text{ mohm}$ ($V_{gs} = 4.5 V$)
 $I_{cont} = 6.5 A$ ($T = 25^\circ C$)
 $I_{peak} = 40 A$ (Pause < 10 us)

Controller

- Voltage & Current:**
 $+12.6V @ 2.5A$
- Frequency:**
 $PR122 = 33KOHM,$
 $F_{osc} = 515KHz$
- OCP:**
- POR:**
 $POR \text{ Hysteresis} = 0.1V$
 $V_{on} = 7.5V$
- Enable Voltage:**
 $V = 2.9 V$
- Soft start time:**
 $T_{ss} = 23ms$
- Phase selection:**
 N/A
- Inrush Current:**
 $C_{total} = 20uF$
 $I_{inrush} = 0.01A$

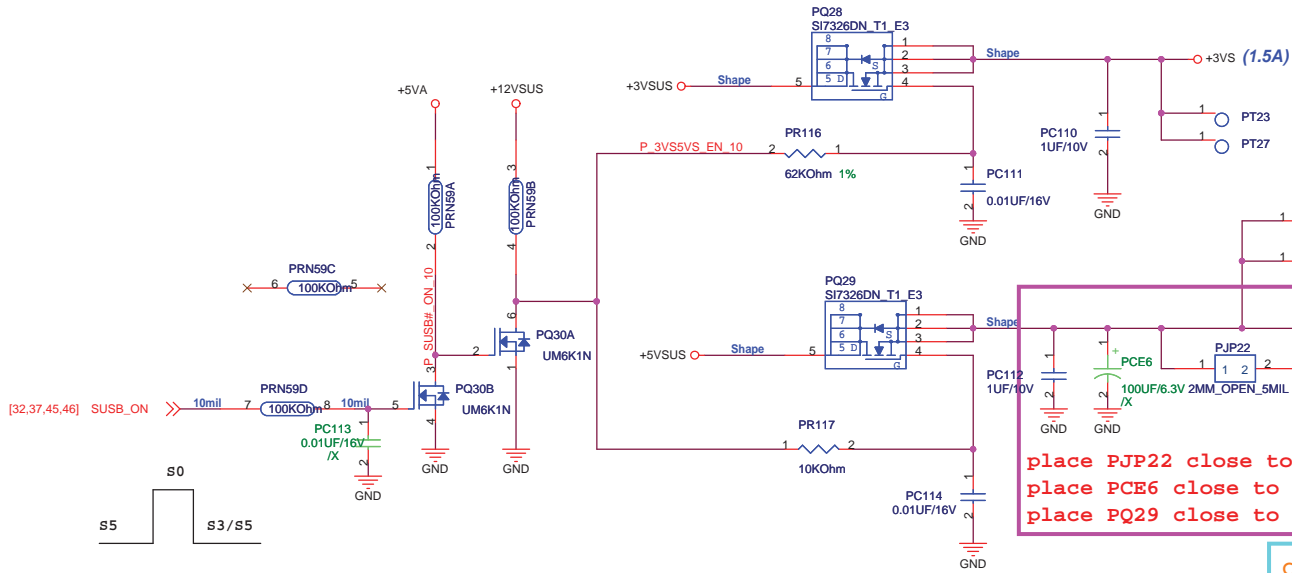


Battery Charging Current :
 $4.4V > V_{adj2} \geq 0V \implies$
 $I_{chg} = (V_{adj2} - 0.075) / (25 \cdot R_s)$
 $BATSEL_2P\# = 1, I_{ch} = 1.49A$
 $BATSEL_2P\# = 0, I_{ch} = 2.62A$
Input Adaptor Max. Current Limit :
 $I_{limit_current} = (V_{adj1} - 0.075) / (25 \cdot R_s) = 1.90A$

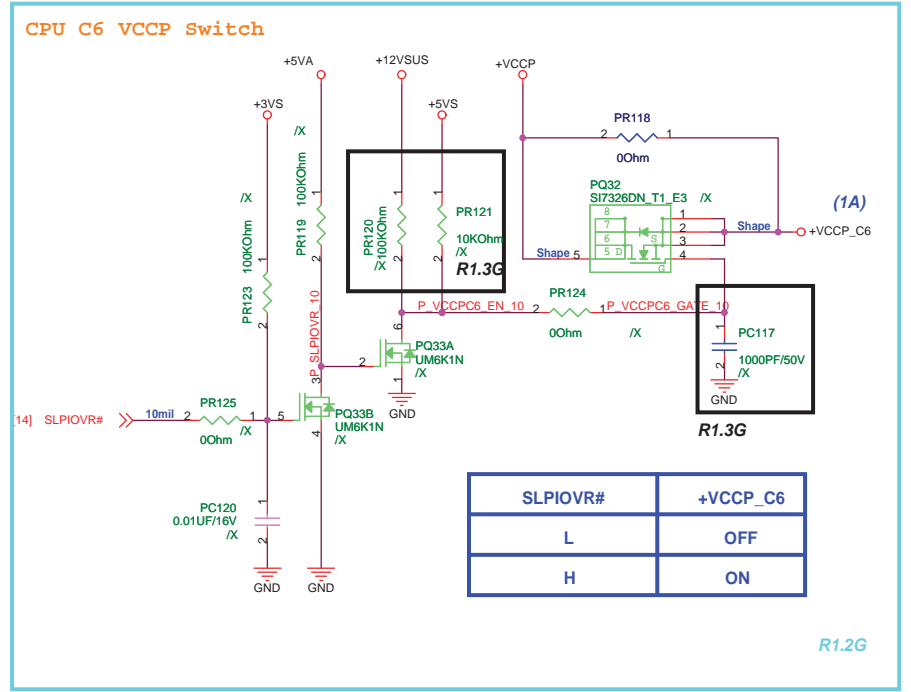
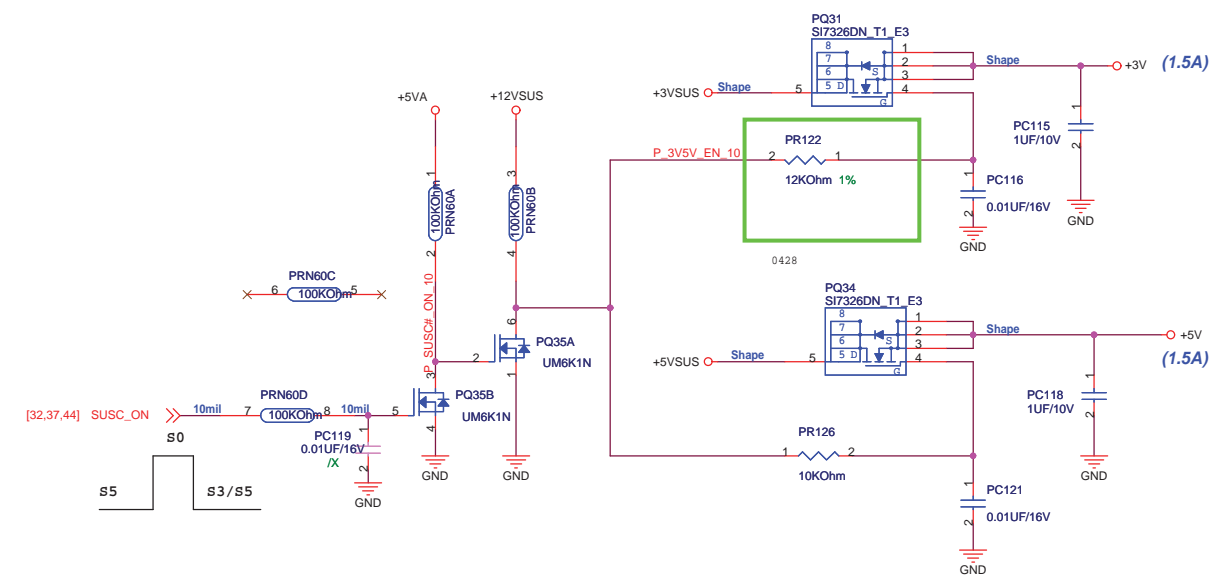
Pre-Charging Mode :
 Precharging current = 149.2mA
 $V_{adj2} = 168mV$
ACIN Threshold = 1.25V
 Adaptor > 13.75V, System Powered by Adaptor
 Adaptor < 13.75V, System Powered by Battery

Battery Charging Voltage :
 $V_{adj3} : VREF \implies V_{bat} = 4.2V / \text{cell}$
 $3.9V > V_{adj3} > 2.4V \implies V_{bat} = 4.35V / \text{cell}$
 $V_{adj3} : GND \implies V_{bat} = 4.0V / \text{cell}$
 $2.2V > V_{adj3} > 1.1V \implies V_{bat} = 2 \cdot V_{adj3}$
Battery Cell Selection :
 CELLS: VREF \implies 4 Cells;
 CELLS: OPEN \implies 3 Cells;
 CELLS: GND \implies 2 Cells;

VREF = 5.0V
 $f_{osc} (KHz) = 17000 / RT (KOhm)$
 Soft start: $t_s(s) = 0.13 \cdot CS (uF)$



place PJP22 close to PCE6
place PCE6 close to PQ29
place PQ29 close to PCE2



SLPIOVR#	+VCCP_C6
L	OFF
H	ON

DATE
3/25_Item1 Page30 del IDE_PCSEL#1 circuit
3/25_Item2 Page30 change S_SATALED# to FLASH_LED#
3/25_Item3 Page14 USB_OC#0&USB_OC#1 combine to USB_OC#01 Page30 USB_OC#0 change to USB_OC#01 Page14/30/32 exchange USB port2 /port7 net name
3/25_Item4 Page34 circuit move to Page30
3/25_Item5 Page37 EC pin14 use as TP_LED#
3/25_Item6 Page13 del R196& CLK_PC_UART
3/25_Item7 Page14 SCH GPIO2--> SIMCARD_IN#;GPIO1 -->HDD_ON Page23 add GR2
3/25_Item8 Page14 add Test point for USB port4&SB_SPKR
3/25_Item9 Page7 del EC34,CLK_48M_READER2
3/25_Item10 Page37 add TP for LID_EC_L#, CNT2_CHG#, CNT2_DIS#, GS1_INT1, GS1_INT2
3/25_Item11 Page32 add +5V_USB source(+5VS&JP3201)
3/26_Item0 DEL unused page& rename page No.
3/26_Item1 P38 BAT2_IN#-->BAT_IN#; Reserve ESD Diode for SMB&BAT_IN# P32 BAT1_IN# -->BAT_IN ;Del BAT2_IN off-page
3/26_Item2 P10 Add VID & VSSSENCE for OCUG Go back T91 solution
3/26_Item3 P31 Add JP3101 for +5VS /+5V_USB
3/26_Item4 P32 Define EC pin102 --> CPU_OV0; pin103 --> CPU_OV1 Define EC pin104 -->+VCCP_OV0; pin105 -->+VCCP_OV4 Define EC pin85 -->DDR_OV0; pin86 -->DDR_OV1
3/26_Item5 P08 Add net name H_IGNNE#
3/26_Item6 P13 Modify RTC circuit
3/26_Item7 P07,P14,P22,P32,P33,P35 Add RF optional circuit
3/26_Item8 P39 correct screw hole
3/26_Item9 P24 add short point for intel Echo peak pin define; ADD optional 0 ohm for Echo peak and NE672 Aux power pin define
3/26_Item10 P27 Decrease component for LAN circuit
3/26_Item11 P29 Del D36 & FLASH_LED_P# & R123; Add CSL2; +VCC_FLASH change to +3VS P30 Del FLASH_LED_P# & SR16
3/26_Item12 P41--P49 add power new schematic
3/26_Item13 P31 del JP3201 (power page has this JP)
3/27_Item1 P29 YQ2B-->YQ1B; P35 TPQ2B-->TPQ1B
3/27_Item2 P21 VR8,VR9 Change to short JP
3/27_Item3 P21 Costdown RGB ESD Diode
3/27_Item4 P10 ADD optional Thermtrip# circuit
3/27_Item5 P41-P49 ADD power new circuit
3/27_Item6 P32 +VCCP_OV0 changed from EC pin104 to SCH GPIOUS3 P32 TP_LED# changed from EC pin14 to EC pin85 P14 CARD_READER_EN# changed from SCH GPIOUS3 to SCH GPIO1
3/27_Item7 P35 HOTKEY_SW0# Pull up change to +3VA
3/27_Item8 P29 Del HDD_ON CIRCUIT
3/27_Item9 P35 add CIRCUIT for EXPRESS GATE
3/27_Item10 P41-P49 add power new circuit
3/27_Item11 P18 change DIMM con to STD Type
3/27_Item12 P21 cost down U6, Del F1 Fuse
3/27_Item13 P27 LAN chip change to 02G911002601,modify LAN circuit (need check pin define)
3/27_Item14 P08 R14,R16 120 -->56 OHM; R15 68-->56OHM P18 MC5, MC9, MC10 -->/X P19 Cap Change to Array Cap for Costdown
3/27_Item15 P39 del H143,H144 for ME change

3/29_Item1 P22 add pull down 100k for LBKLT1_EN
3/29_Item2 model name change to N12L
3/29_Item3 P21+5V_CRT -->+5V_CRT_F ,VR2 --> /X
3/29_Item4 P23 del power control circuit, add pull up for SIMCARD_IN#; 3G reset circuit-->/X
3/29_Item5 P13 add Test point T207 (strap pin)
3/29_Item6 P22 +3VS --> +3V_LCD
3/29_Item7 P27 add R179 -->/X (no WOL function)
3/30_Item1 P32 EC pin32 -->CRT_IN (pull up); pin85-->CRT_DACPWR_EN#; pin86 -->CRTDAC_RST# ; TP_LED--> Pin18
3/30_Item2 P20 add CRT DAC power control circuit & CRT reset circuit P21 add CRT conn in circuit
3/30_Item3 P27 LAN pin5 connect to pin15 (not +3V_LAN)
3/30_Item4 P18 go back to STD. DIMM Conn
3/30_Item5 P21 correct Vsync & Hsync
3/30_Item6 P29 Re-define +5VSUS for I/O Brd pin 21 for PWR Led
3/30_Item7 P14 add pull down for WLAN_LED; P33 add cost down solution for Auto-boot circuit
3/30_Item8 P37 Array Resistor change to single type for future cost down
3/30_Item9 P32 CRT_IN change to EC pin14 (hot key 1)
3/31_Item1 P39 Add screw hole H149
3/31_Item2 P41-P49 add power new circuit
3/31_Item3 P24 WR9,WR11,WR13,WR14 Change to 0603 type
3/31_Item4 P19 change array cap to single type
3/31_Item5 P28 change 4R8p 0ohm to 2R4p type
3/31_Item6 P22 L84,L85,L86,L87 change to low cost part
3/31_Item7 P29 del camera USB common chock and 0 ohm (I/O brd already has)
3/31_Item8 All Colay 0 OHM Change to array type
3/31_Item9 P29 del IR3 (I/O brd already has a bead)
3/31_Item10 P30 del SRN1-SRN7 for costdown&layout
3/31_Item11 P34 Reserve OR29 for cost down
3/31_Item12 P23 Q20 change to 2N7002
3/31_Item13 P22 chage the RF Cap position for LVDS signals
3/31_Item14 P7,P13,P32 chage the crystal to low cost part
3/31 item15 Reserve CR29 for future cost down power latch circuit
4/1 item1 P14 add Pull up for PM_LEVELDOWN#/CPU_LEVELDOWN#,Pull down for +VCCP_OV0
4/1 item2 P20,21 add back up CRT DAC Reset&Power control solution
4/1 item3 P24 WU1 change to 06G030057013
4/1 item4 P16 Reserve HDA I/O power to +1.5VS ,P29 Camera_EN to +1.5VS P14 del CAMERA_EN
4/1 item5 P22 del GU13(+3V_LCD circuit) , P38 Del L3816 for Layout placement space
4/1 item6 P32 add OSL5,OSL6 for PM_RSTRDY#&PM_RSTWARN (debug)
4/2 item1 P27 swap LAN pin29/30 net name(add LR86,LR87 for 8132), add R64 for clock Voltage swing,add LC11,12,13,15 decoupling
4/2 item2 P32 modify BAT_IN2 pull down,BAT_IN pull High
4/2 item3 P27 del LR80 ,P28 add LC18 (/X)
4/2 item4 P21 reserve D13 for ESD
4/3 item1 P18/19/22/35 swap memory data/address/command, common choke, Keyboard I/O chip capacitors.
4/3 item2 P38 change DCIN_GND to GND.
4/3 item3 P39 change H140 pin 3&5 from GND to NC.
4/3 item4 P32 OR10 change to 0603 size
4/3 item5 P20 R209-->/X,R218,L6-->N/A (for Pre-ER)
4/5 item1 P24 del WLAN SMB for layout routing
4/5 item2 P40 add EMI cap
4/5 item3 swap for DIMM & chip resistors of clock Gen.

4/6 item1 P40 add EC29-EC31 as stitched CAPs.
4/6 item2 P40 add EC32-EC34 for EMI needed.
4/6 item3 swap RN6/RN18.
4/6 item4 P39 change H149 from s03549 to s04146.
4/6 item5 P14 change EC39 PIN1 definition from A_CLK to A_Z_BITCLK for EMI
4/6 item6 P29 exchange DUA_CON PIN 12&21 definition for EMI which was found problem in 1005.
4/7 item1 P39 change H142 pin 3 from GND to NC.
4/7 item2 P40 add CAPs for EMI request.
4/28 item1 P22 GC99 change to 0.22UF
4/28 item2 P24 add WC19,unstuff cut off power circuit
4/28 item3 P14 SCH GPIO8 use as +1.8V OV, and add pull up R228
4/28 item4 P41-P49add power circuit
4/28 item5 P37 /X Q13,Q17,R170,R174,R180 (costdown)
4/28 item6 P22 reserve EC back light control ,reserve C487 for +3V_LCD,reserve D22 for BL_EN control
4/29 item1 P7,P32 reserve PCLCLK for EC for OC consideration
4/29 item2 P7 CR14 change from 10 to 30 ohm,add CC7 for VDDREF power noise
4/29 item3 P27 C457 change to 0 ohm
5/4 item1 add R145 & C475 for RF request.
5/4 item2 delete SL & JP for factory request.
5/6 VGA connector P/N change to 12G10110915M
5/7 Touchpad connector P/N change to 12G183401225

		Title : HISTORY	
<small><OrgName></small>		Engineer: <OrgAddr1>	
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