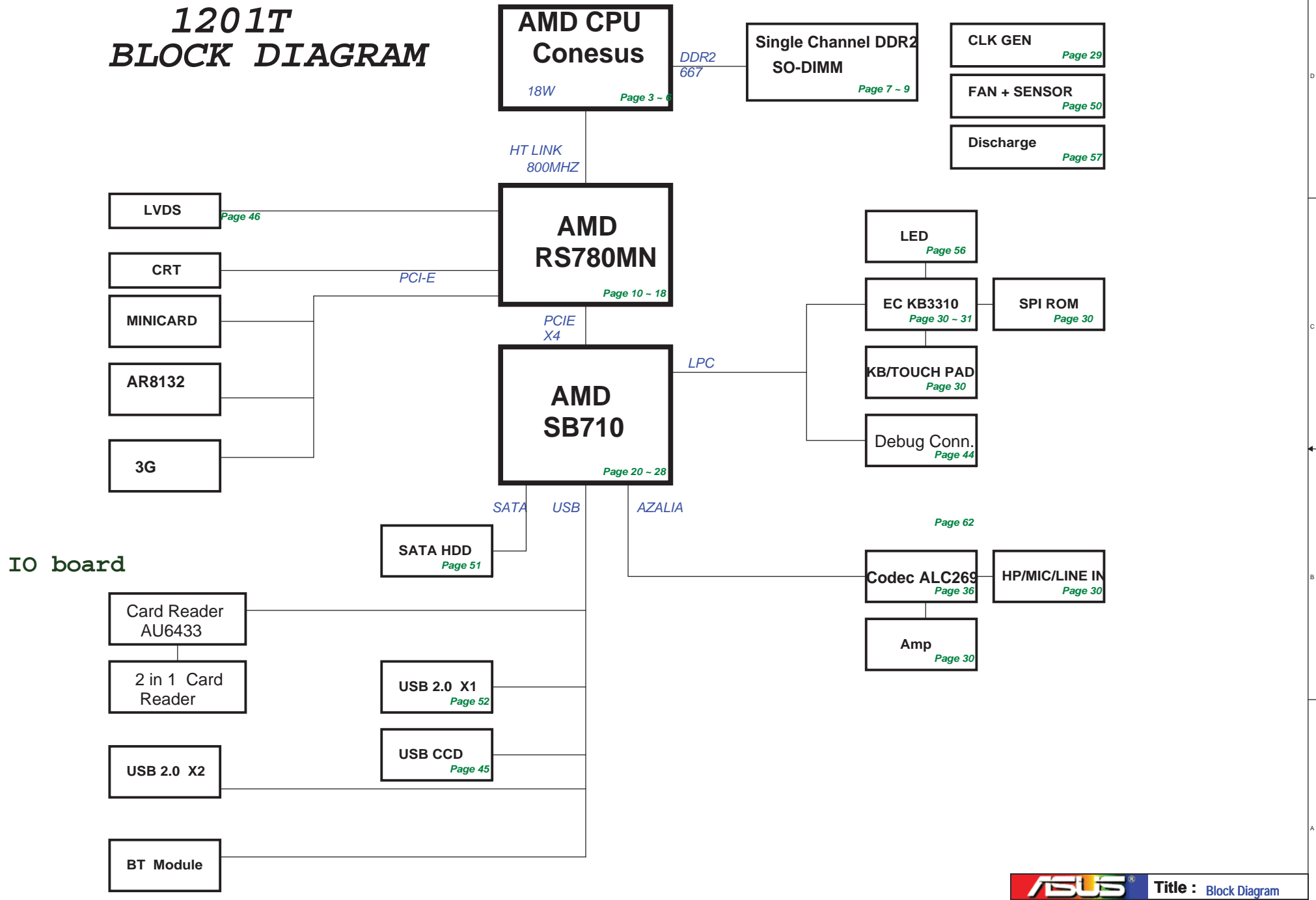
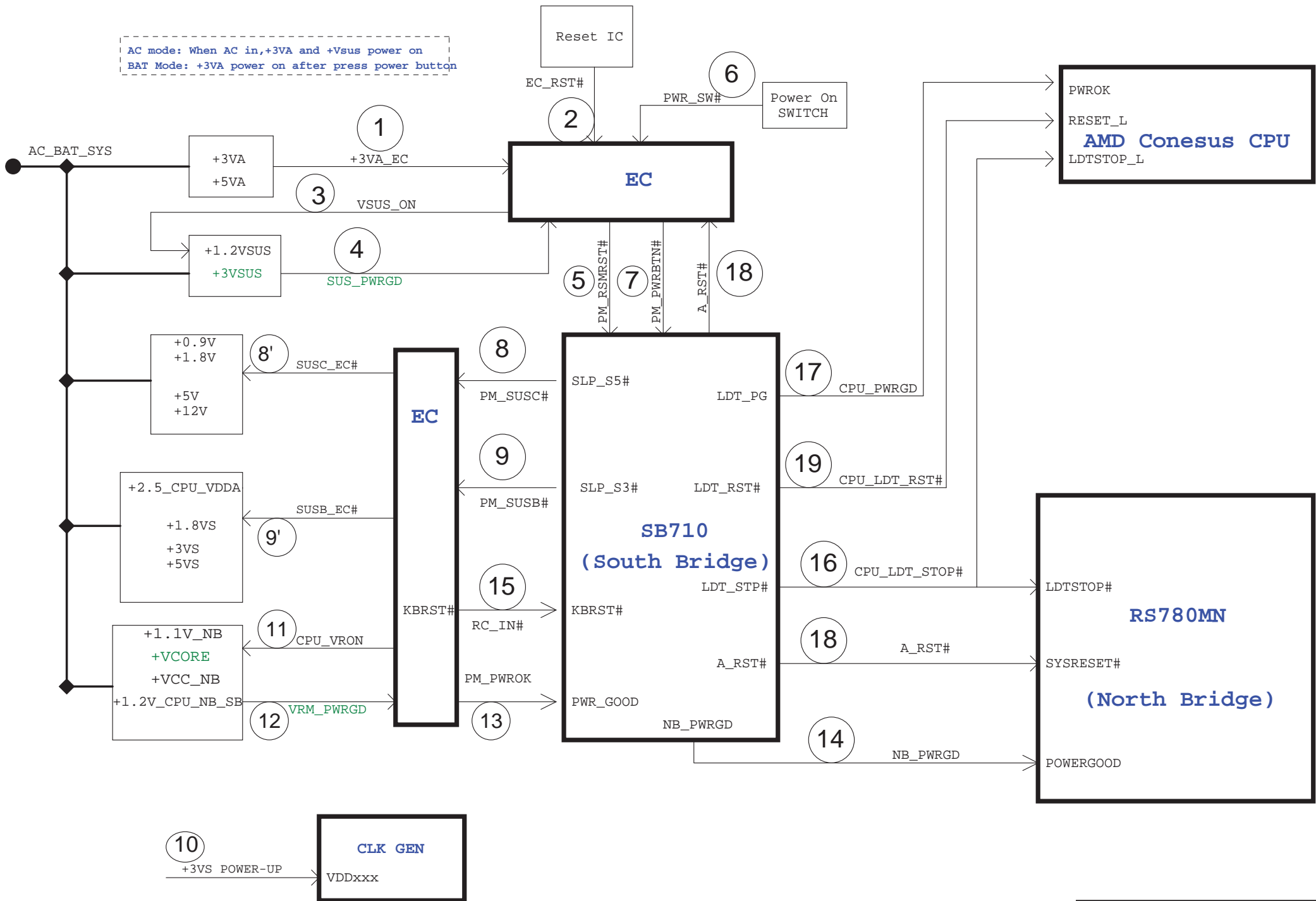
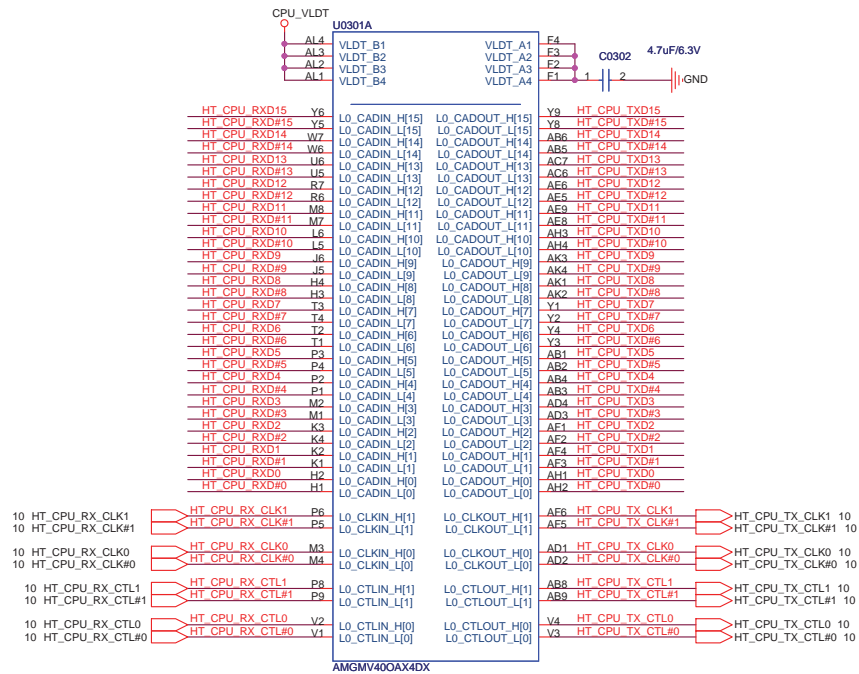


# 1201T BLOCK DIAGRAM

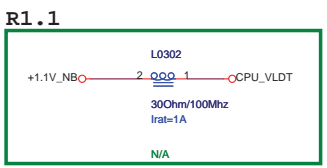
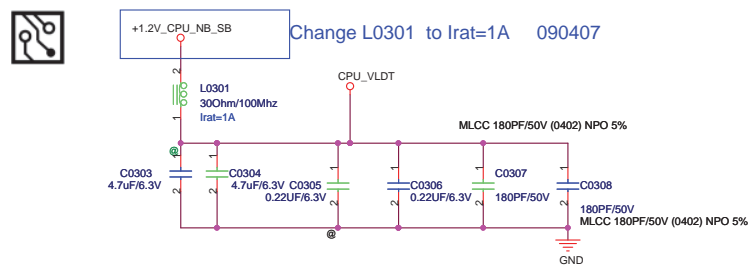


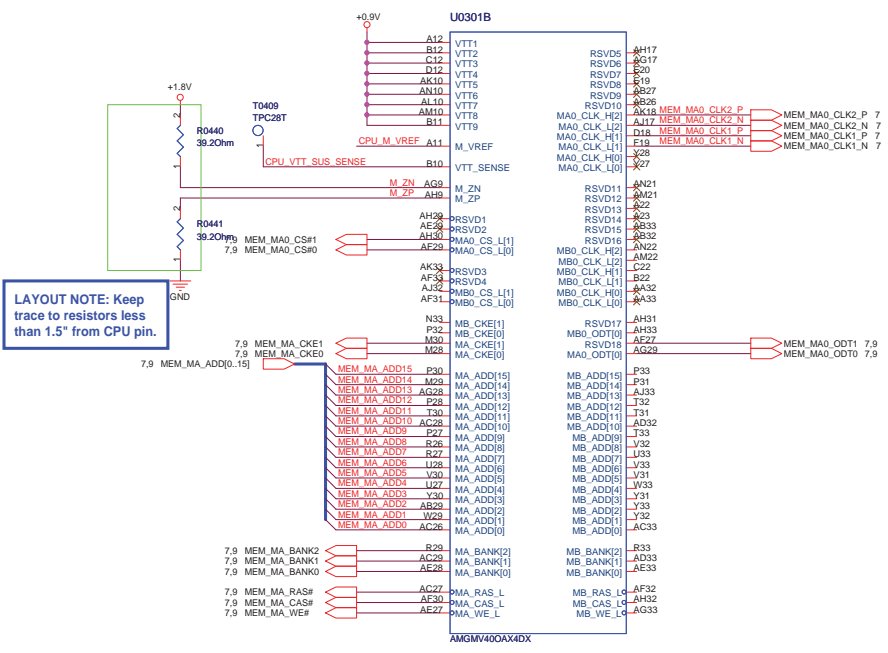
AC mode: When AC in, +3VA and +Vsus power on  
 BAT Mode: +3VA power on after press power button



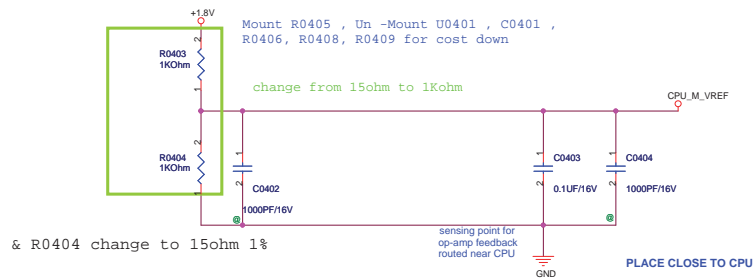


**DESIGN NOTE:**  
 VLDT must be routed as a pour or a trace at least 200 mils wide.  
 VLDT may be routed from the source to either ALx balls or Fx balls.  
 Choose whichever makes routing simpler.  
 These six capacitors must be placed very near the selected balls.  
 The "other" set of balls must be decoupled with a 4.7uF cap.

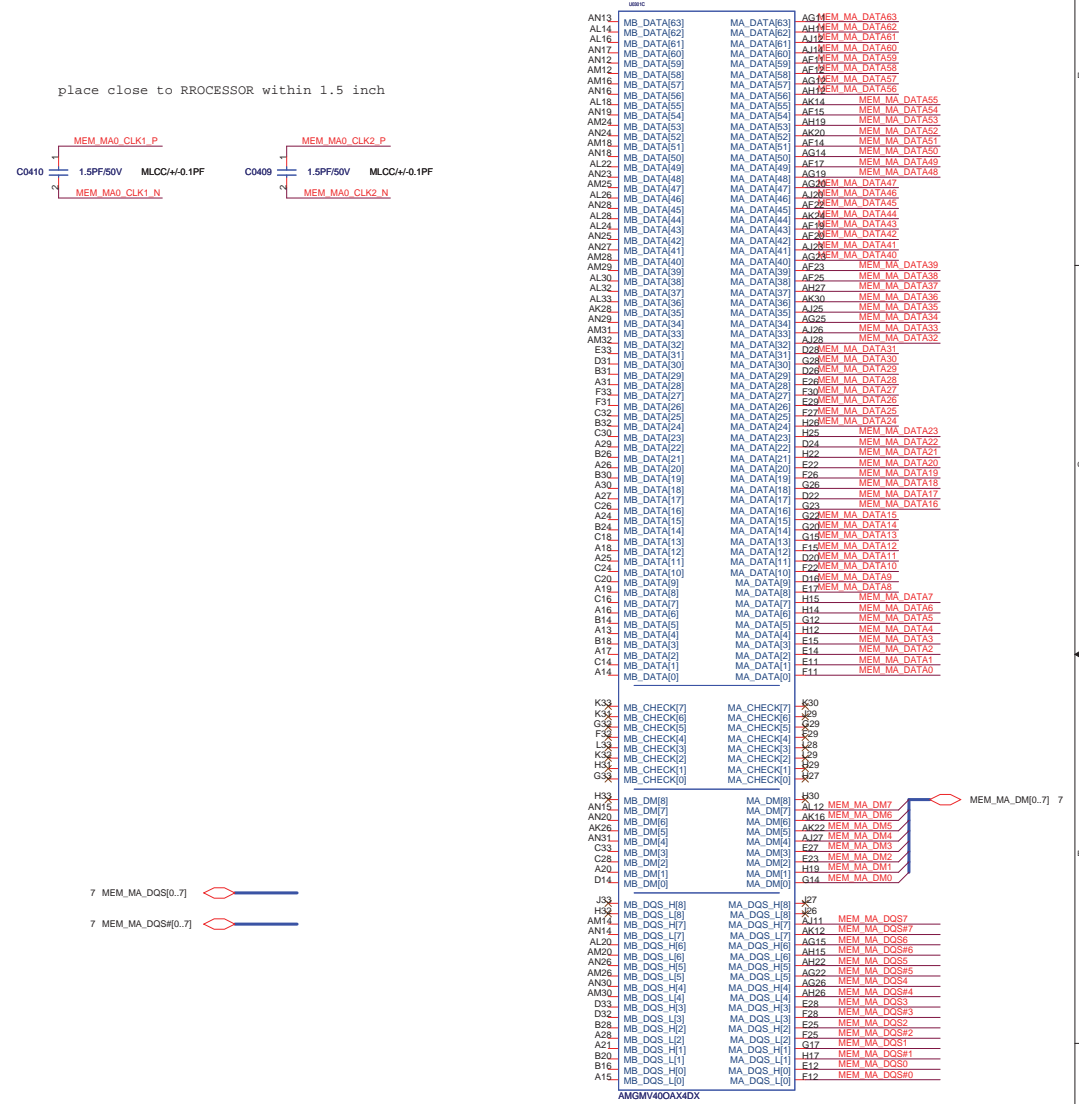




LAYOUT NOTE: Keep trace to resistors less than 1.5" from CPU pin.



R0403 & R0404 change to 150hm 1%

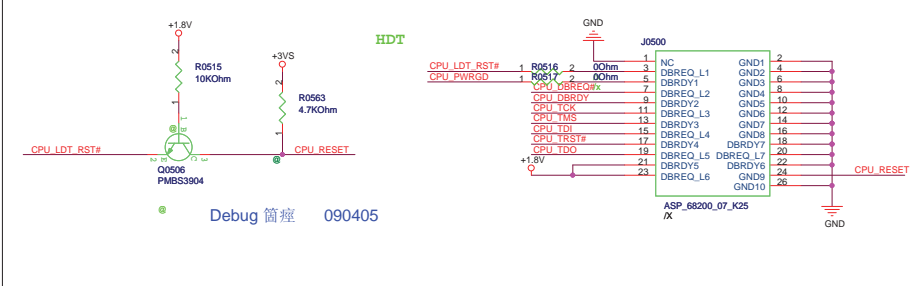
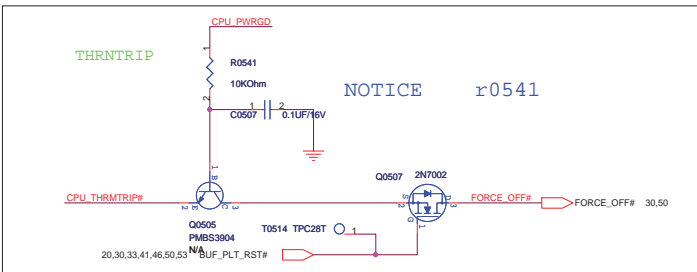
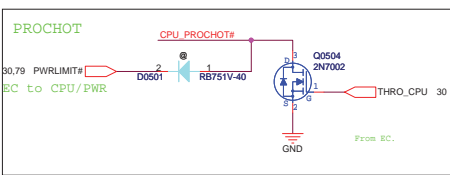
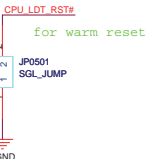
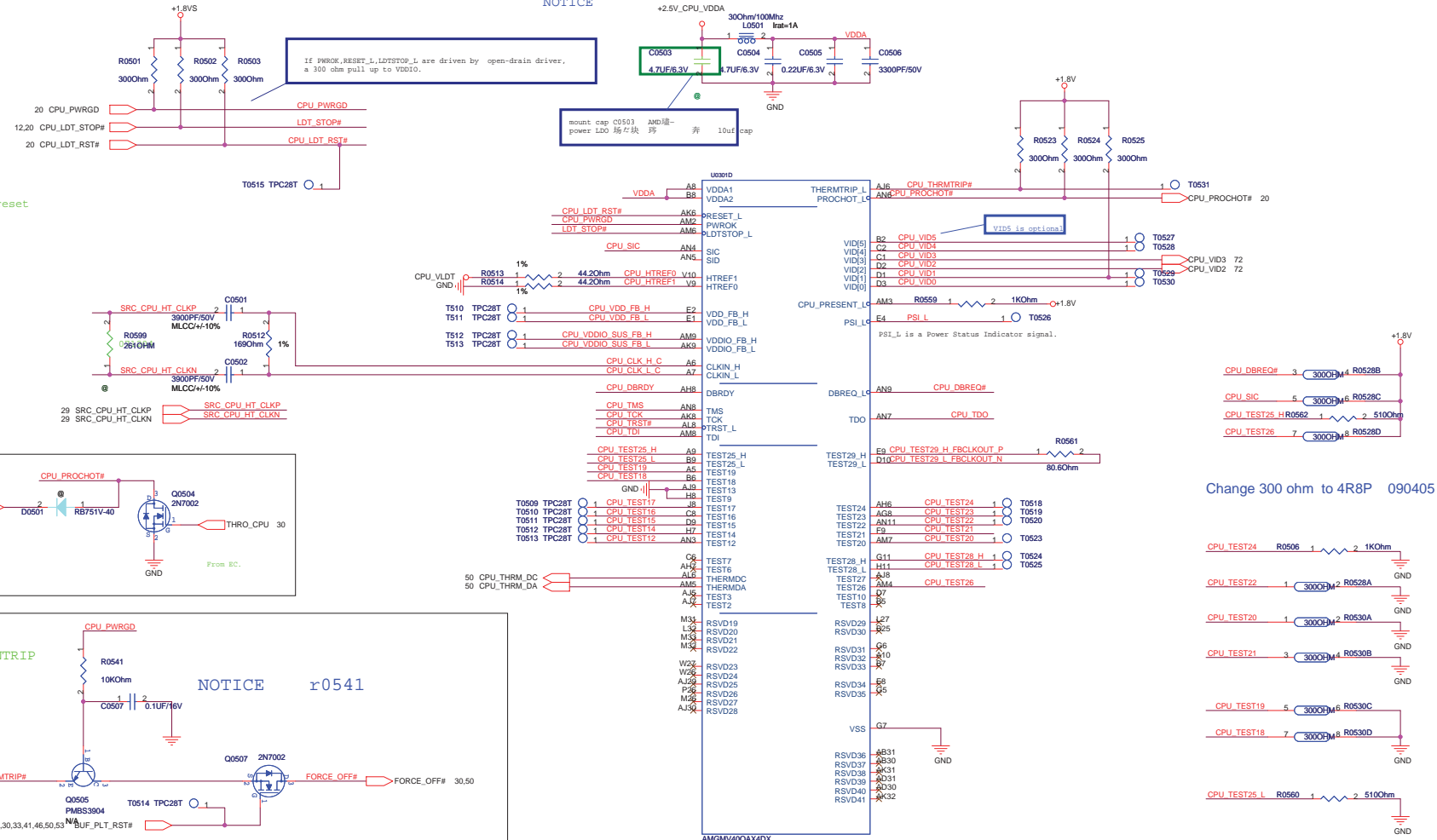


**NOTICE**

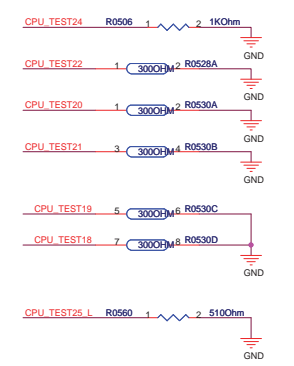
If PWROK, RESET\_L, LDTSTOP\_L are driven by open-drain driver, a 300 ohm pull up to VDDIO.

mount cap C0503 AMD 漏- 跨 奔 10uF cap

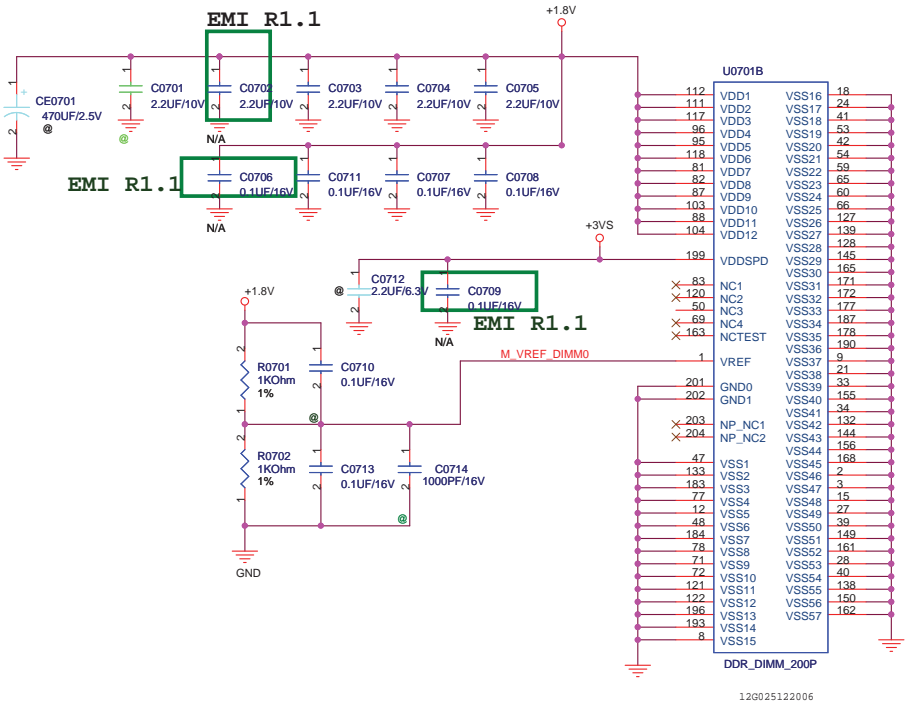
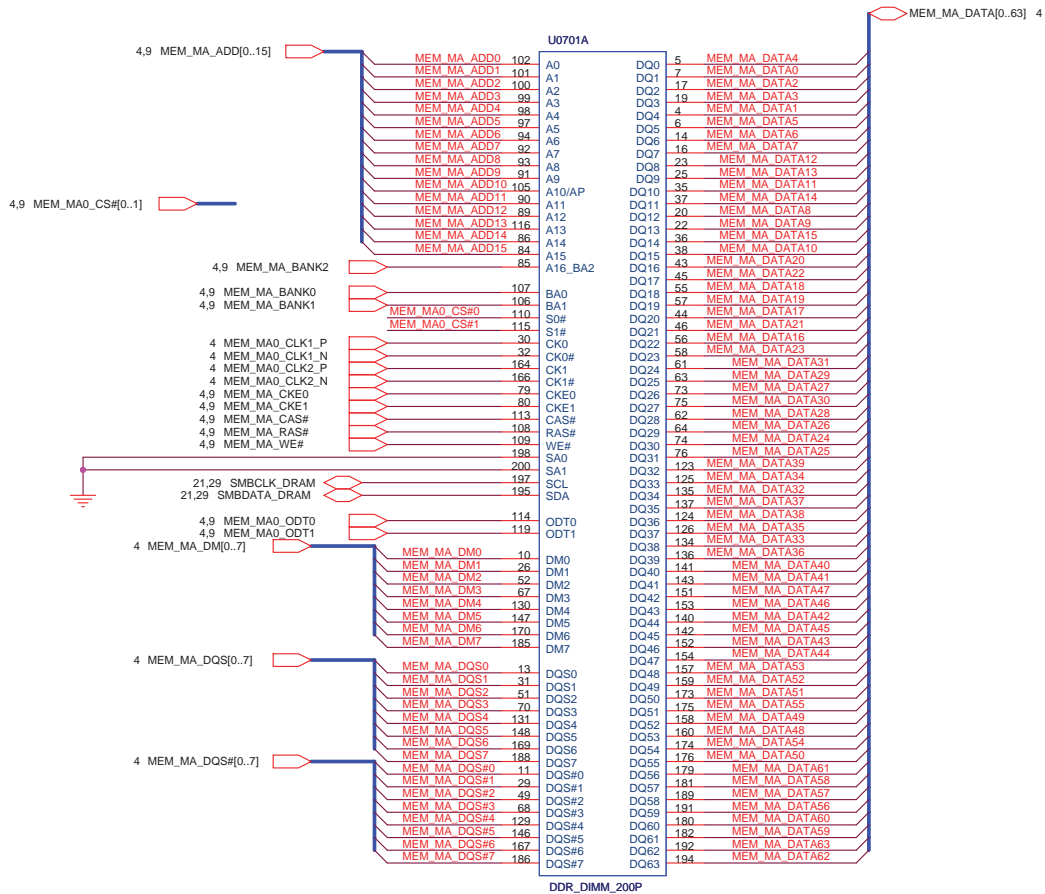
VID5 is optional



Change 300 ohm to 4R8P 090405







12G02533200D

<Variant Name>

**ASUS** Title : DDR2 SO-DIMM

ASUSTeK COMPUTER INC Engineer:

Size	Project Name	Rev
Custom	1201T	2.0

Date: Wednesday, October 14, 2009 Sheet 7 of 79

5

4

3

2

1

D

D

C

C

B

B

A

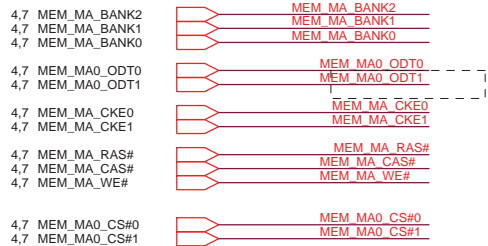
A

<http://laptop-motherboard-schematic.blogspot.com/>

		<b>Title :</b> DDR2 SO-DIMM1	
ASUSTeK COMPUTER INC		<b>Engineer:</b>	
Size	Project Name	Rev	
Custom	1201T	2.0	
Date: Wednesday, October 14, 2009		Sheet	8 of 79

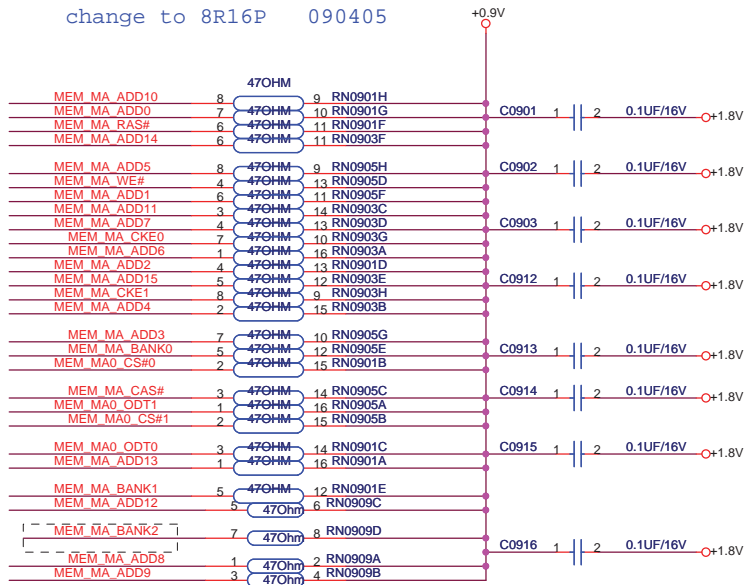


4,7 MEM\_MA\_ADD[0..15]

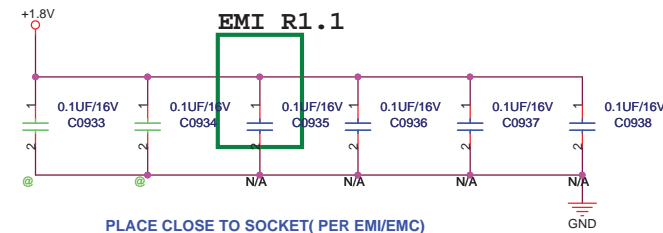
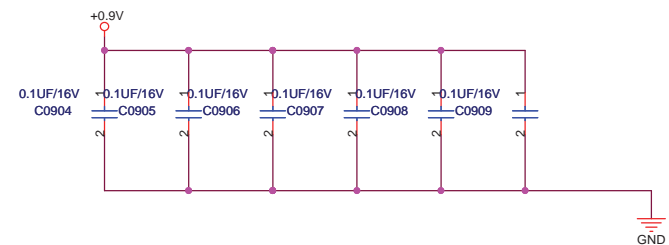


090818 Swap for Layout

change to 8R16P 090405



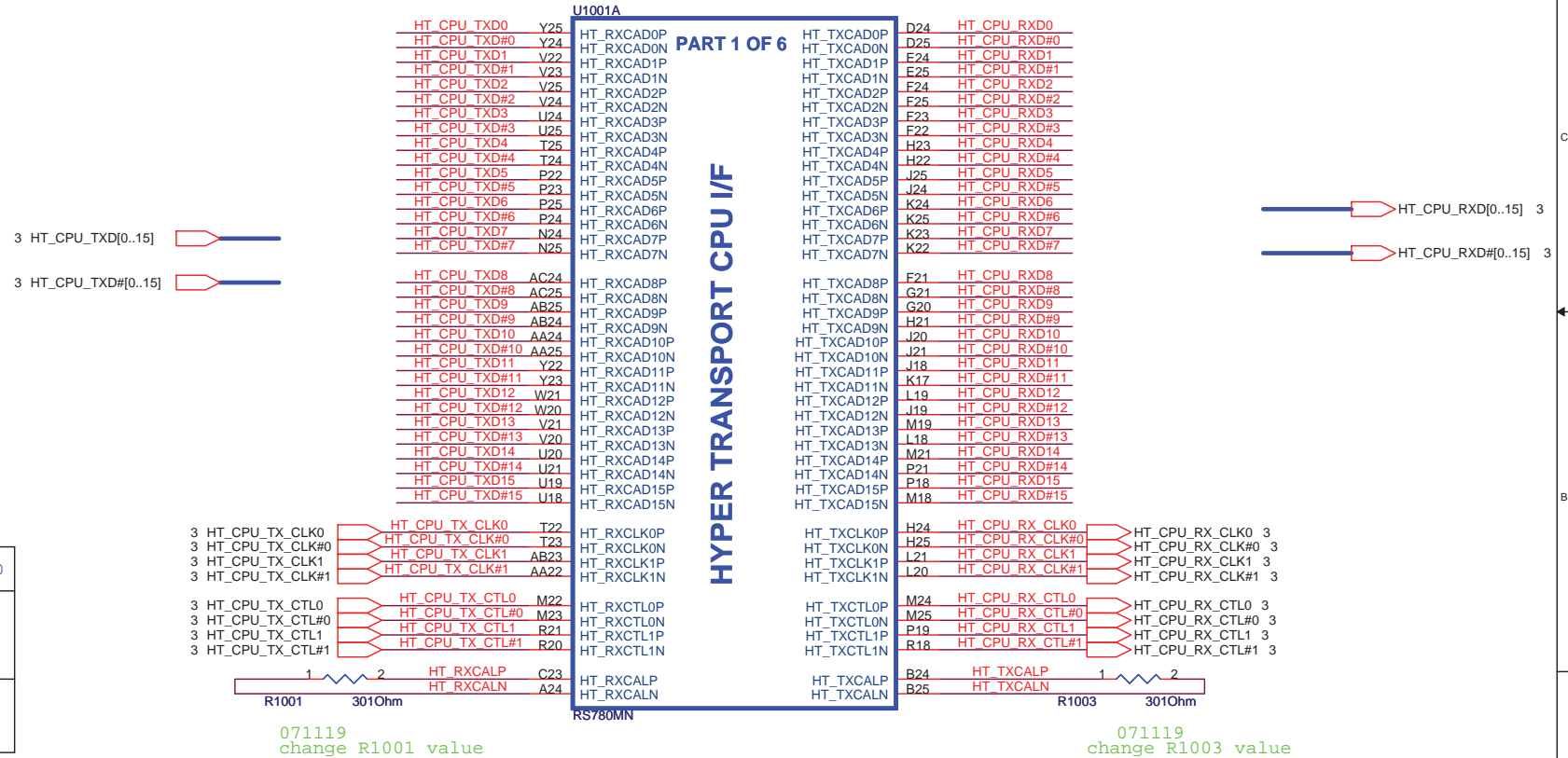
Remove 1.8V C0910,C0911 0.1uF 090405



<b>ASUS</b>		<b>Title : DDR2_TERMINATIONS</b>	
ASUSTeK COMPUTER INC		Engineer:	
Size Custom	Project Name <b>1201T</b>	Rev 2.0	
Date: Wednesday, October 14, 2009		Sheet	9 of 79

R1.11 080319

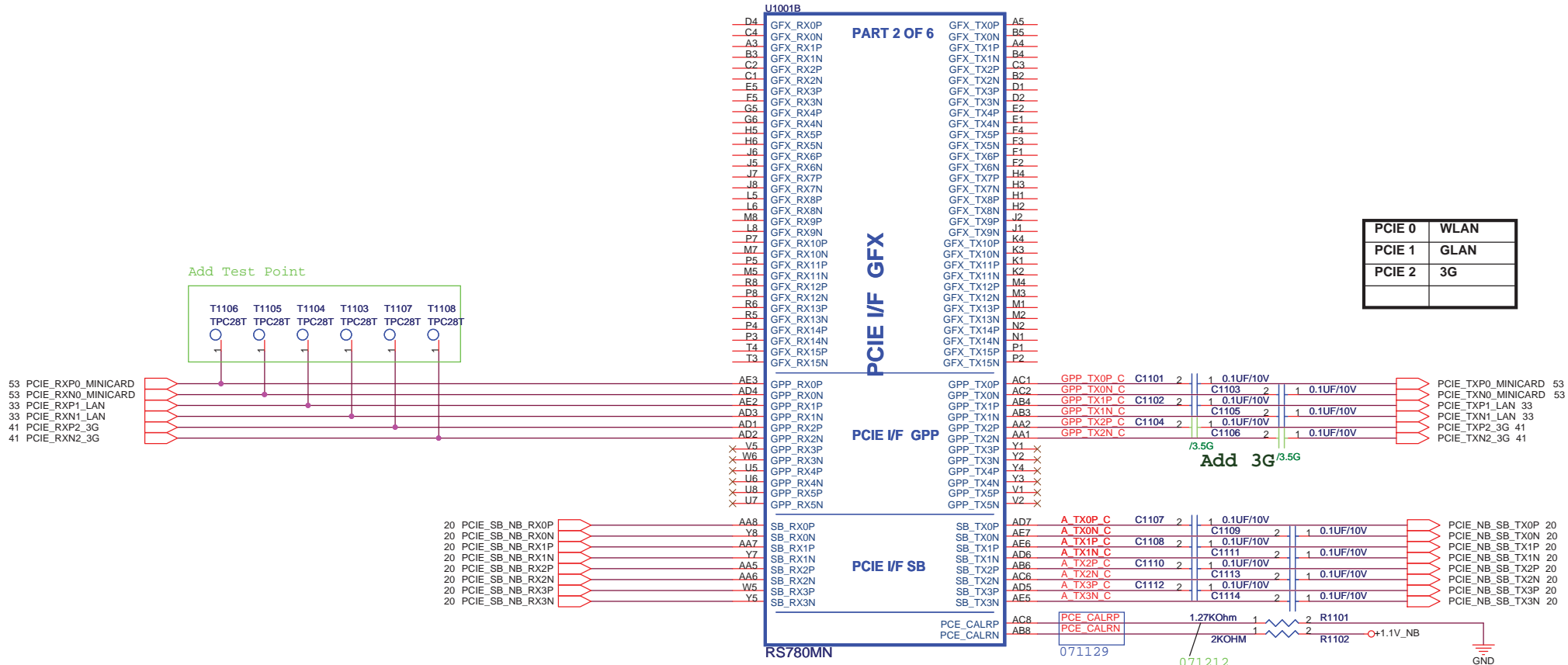
Change the NB Part number to RS780 (A13)



Signal	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)		
HT_TXCALP	100R	1.21K	301R
HT_TXCALN			

R1.11 080319

Change the NB Part number to RS780 (A13)



PCIE 0	WLAN
PCIE 1	GLAN
PCIE 2	3G

**ASUS** Title : RS780M-PCIE LINK I/F  
 ASUSTeK Computer, INC. Engineer: N/A

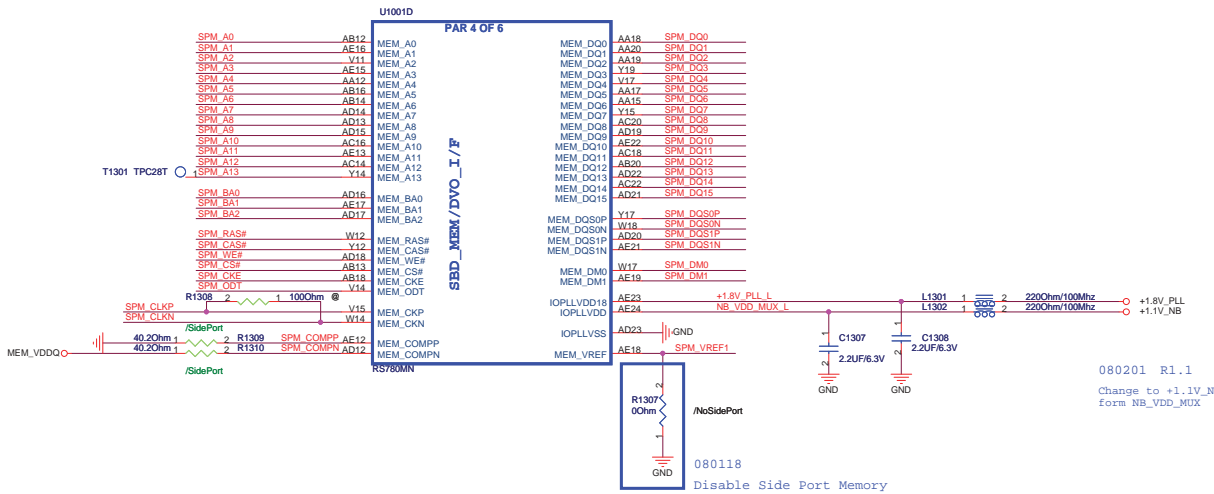
Size	Project Name	Rev
Custom	1201T	2.0

Date: Wednesday, October 14, 2009 Sheet 11 of 79



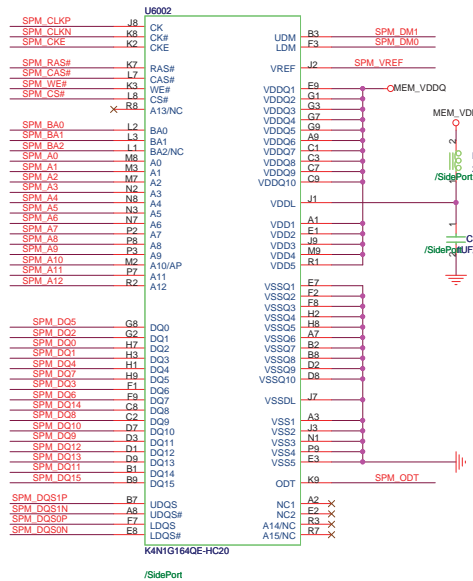
R1.11 080319

Change the NB Part number to RS780 (A13)

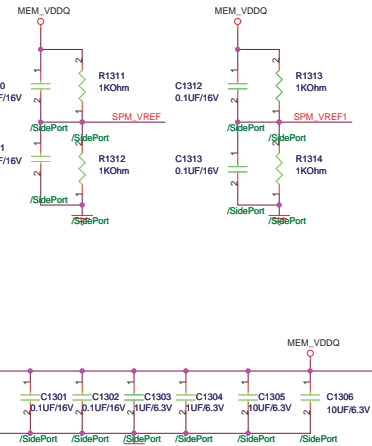


080201 R1.1  
Change to +1.1V\_NB  
form NB\_VDD\_MUX

090813  
Reserve Side Port Memory



080118  
Disable Side Port Memory  
R1.1



DFT\_GPI01: LOAD\_EEPROM\_STRAPS

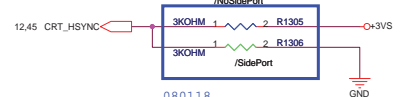
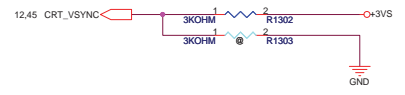
Selects Loading of STRAPS from EPROM  
1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected  
RS780:SUS\_STAT

STRAP\_DEBUG\_BUS\_PCIE\_ENABLE

Enables the Test Debug Bus using PCIE bus:  
1 : Disable ( Can still be enabled using nbcfg register access )  
0 : Enable  
RS780: configurable thru register setting only

RS740/RS780: Enables Side port memory

RS780:HSYNCS#  
Selects if Memory SIDE PORT is available or not  
1 = Memory Side port Not available  
0 = Memory Side port available  
Register Readback of strap: NB\_CLKCFG:CLK\_TOP\_SPARE\_D[1]

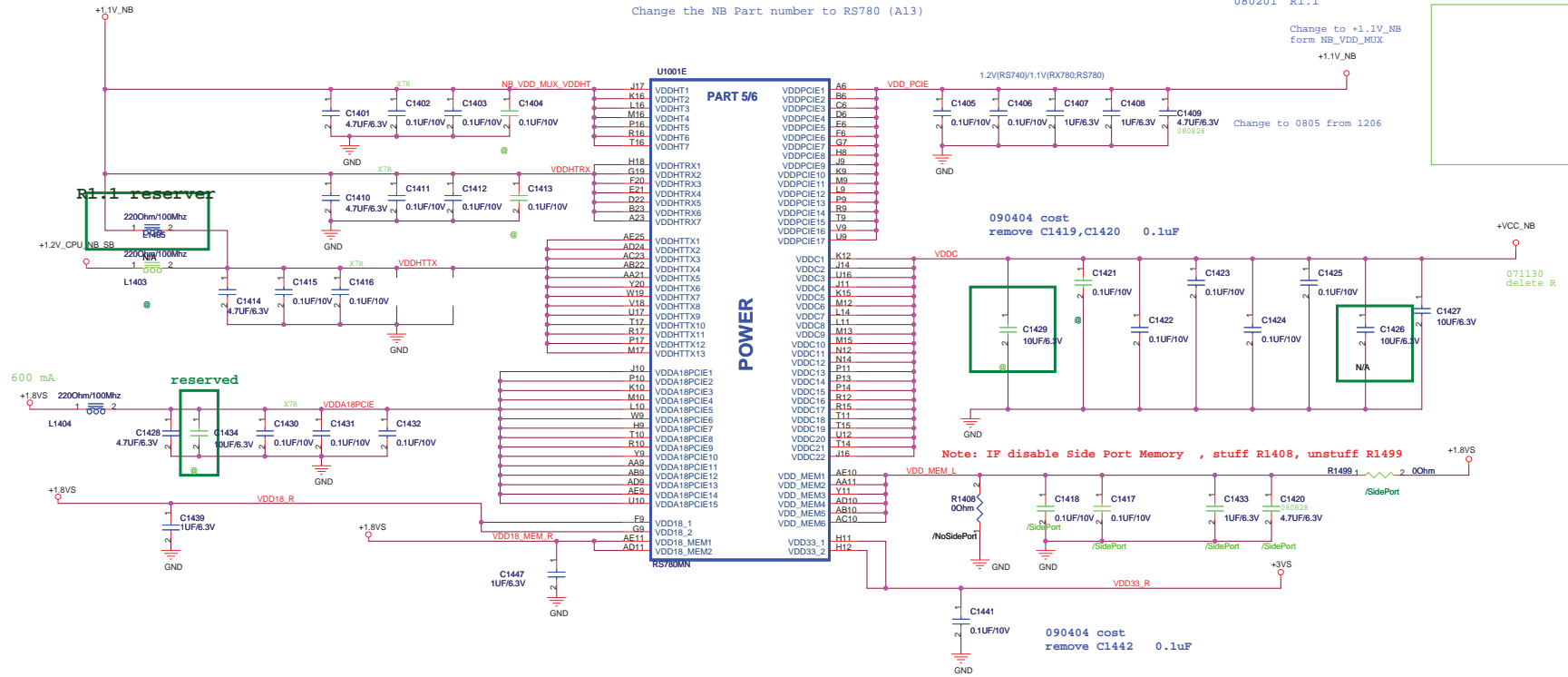


080118  
Disable Side Port Memory  
R1.1

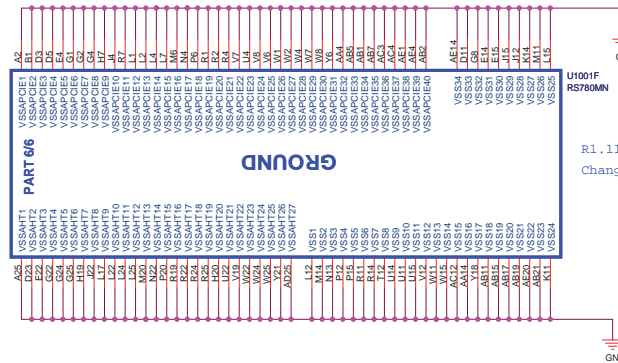
R1.11 080319  
Change the NB Part number to RS780 (A13)

080201 R1.1

Change to +1.1V\_NB  
form NB\_VDD\_MIX

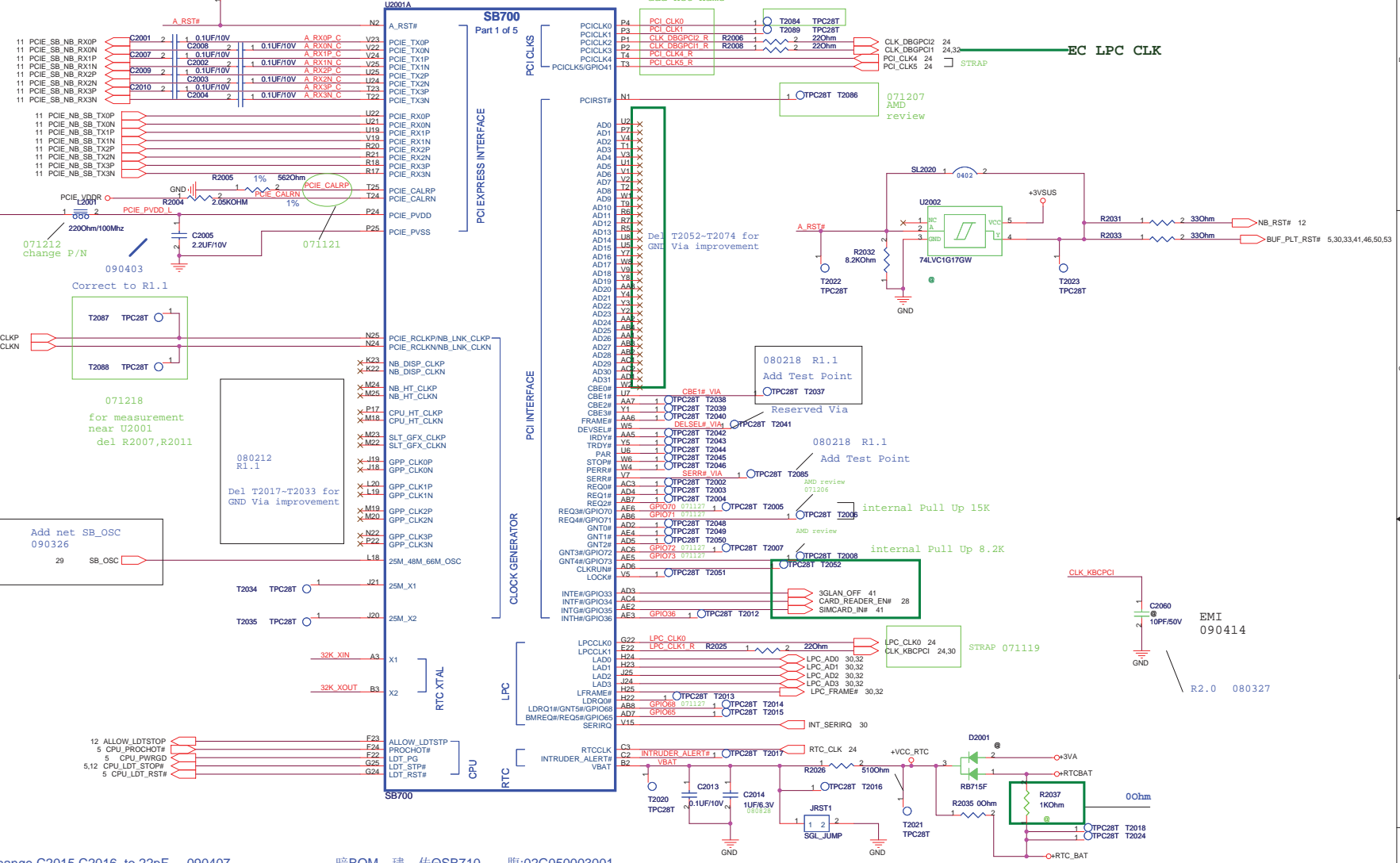


R1.11 080319  
Change the NB Part number to RS780 (A13)



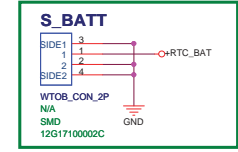
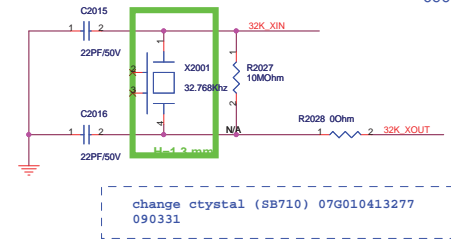
R2.0 080327  
Add test point for factory ICT test

R1.11 080319  
Change the SB Part number to SB700 (A12)



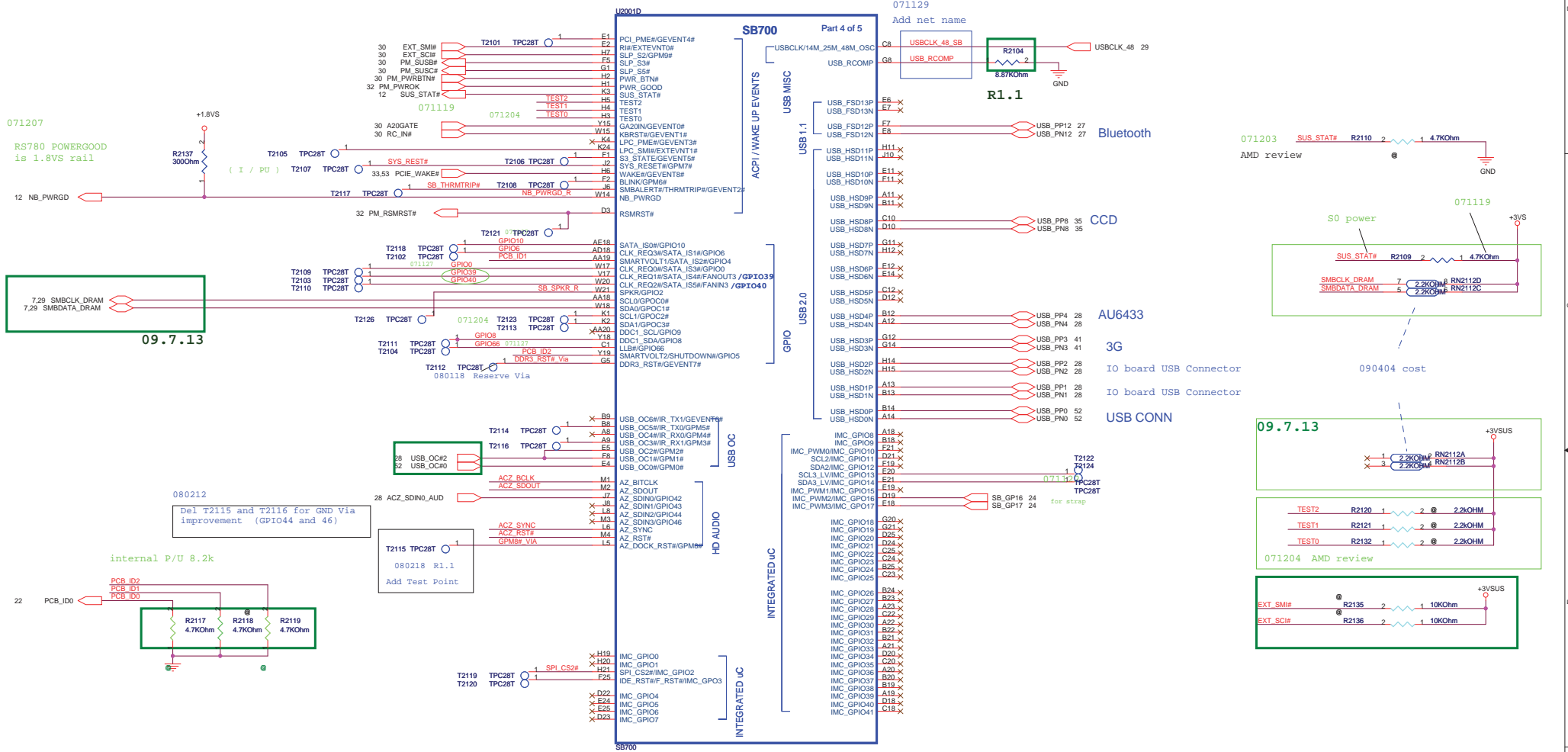
change C2015, C2016 to 22pF 090407

暗BOM 璣 传OSB710 腹:02G050003001  
090406



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R1.11 080319  
Change the SB Part number to SB700 (A12)



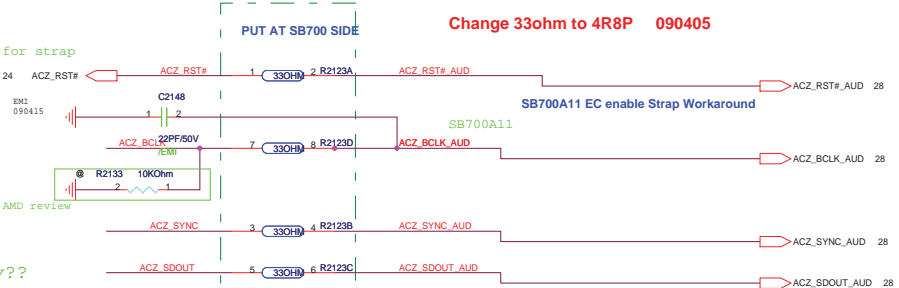
071207  
RS780 POWERGOOD  
is 1.8VS rail

7.29 SMBCLK\_DRAM  
7.29 SMBDATA\_DRAM  
**09.7.13**

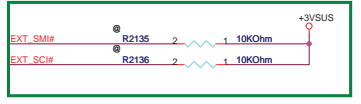
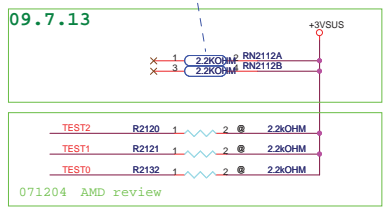
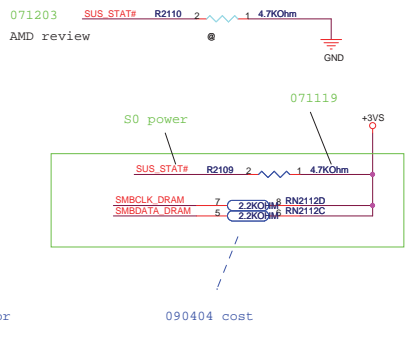
PCB\_ID2  
PCB\_ID1  
PCB\_ID0  
R2117 4.7KOhm  
R2118 4.7KOhm  
R2119 4.7KOhm  
internal P/U 8.2k

071204 AMD review  
ACZ\_SDIN0\_AUD  
R2134 2 1 10KOhm

need to modify topology??

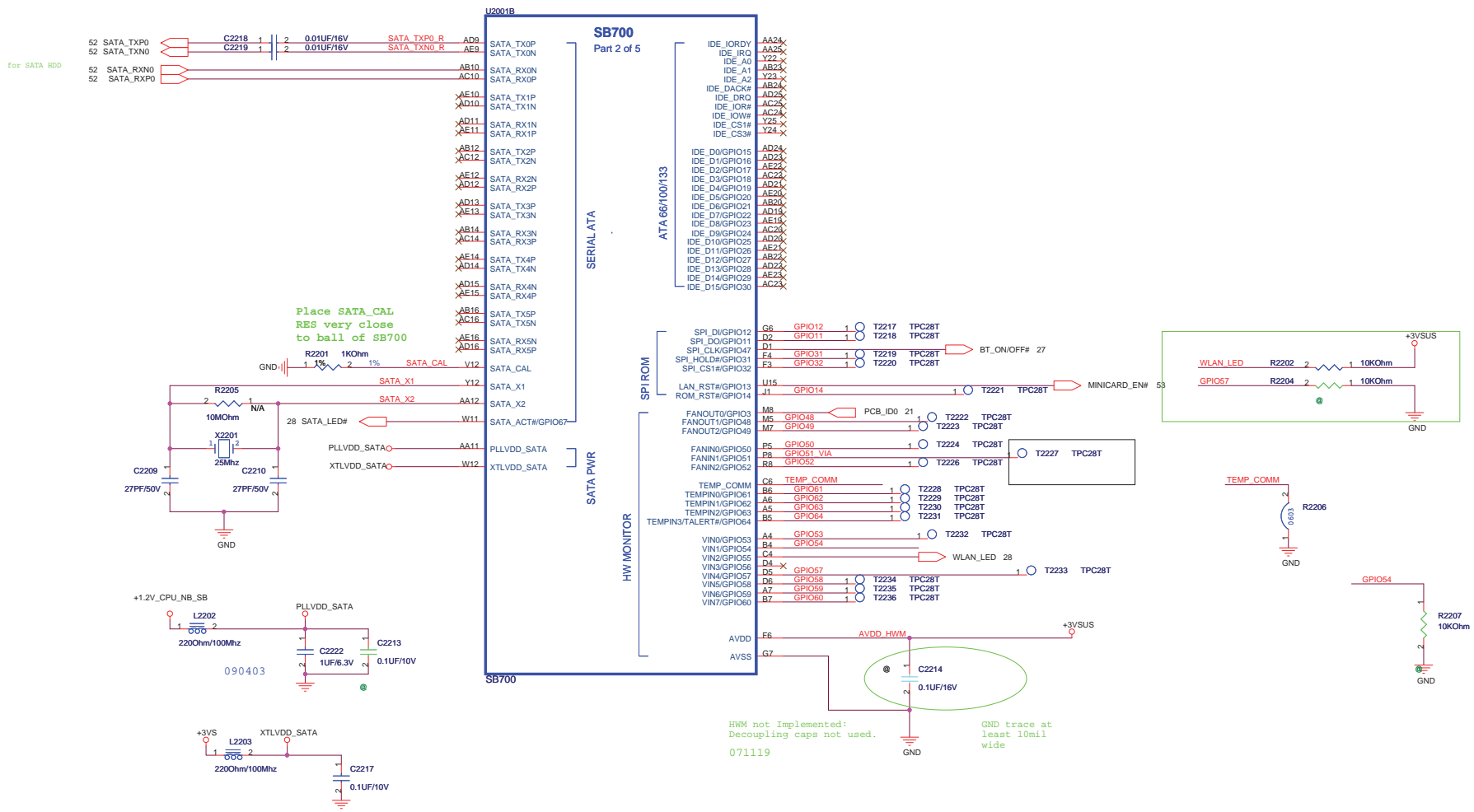


<http://laptop-motherboard-schematic.blogspot.com/>





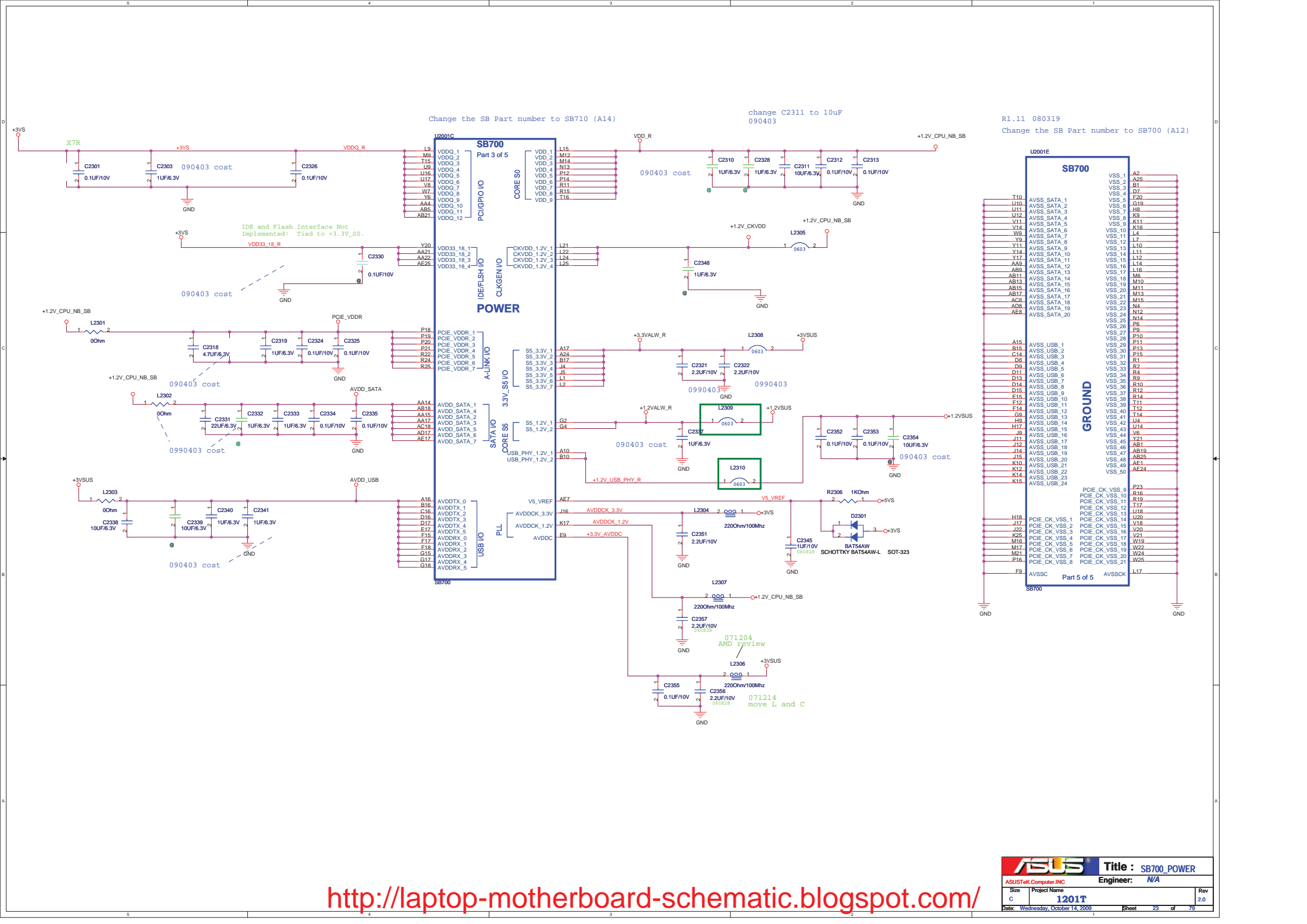
Change the SB Part number to SB710 (A14)



Place SATA\_CAL RES very close to ball of SB700

HWM not Implemented: Decoupling caps not used. 071119 GND trace at least 10mil wide

<b>ASUS</b>		<b>Title : SB700_PATA/SATA</b>
ASUSTek Computer, INC		Engineer: N/A
Size	Project Name	Rev
Custom	<b>1201T</b>	2.0
Date: Wednesday, October 14, 2009		Sheet 22 of 79



Change the SB Part number to SB710 (A14)

change C2311 to 10uF 090403

R1.11 080319

Change the SB Part number to SB700 (A12)

**SB700**  
Part 3 of 5

L9	VDDQ_1
M9	VDDQ_2
T15	VDDQ_3
U9	VDDQ_4
U16	VDDQ_5
U17	VDDQ_6
Y8	VDDQ_7
Y6	VDDQ_8
W7	VDDQ_9
Y5	VDDQ_10
AA4	VDDQ_11
AB5	VDDQ_12
AB21	VDDQ_13
Y20	VDD33_18_1
AA21	VDD33_18_2
AE25	VDD33_18_3
AE25	VDD33_18_4
P18	PCIE_VDDR_1
P19	PCIE_VDDR_2
P20	PCIE_VDDR_3
P21	PCIE_VDDR_4
R22	PCIE_VDDR_5
R24	PCIE_VDDR_6
R25	PCIE_VDDR_7
AA14	AVDD_SATA_1
AA15	AVDD_SATA_2
AA16	AVDD_SATA_3
AA17	AVDD_SATA_4
AC18	AVDD_SATA_5
AD12	AVDD_SATA_6
AE17	AVDD_SATA_7
A16	AVDDTX_0
B16	AVDDTX_1
C16	AVDDTX_2
D16	AVDDTX_3
E17	AVDDTX_4
F17	AVDDTX_5
F18	AVDDRX_0
G15	AVDDRX_1
G17	AVDDRX_2
G18	AVDDRX_3
G18	AVDDRX_4
G18	AVDDRX_5

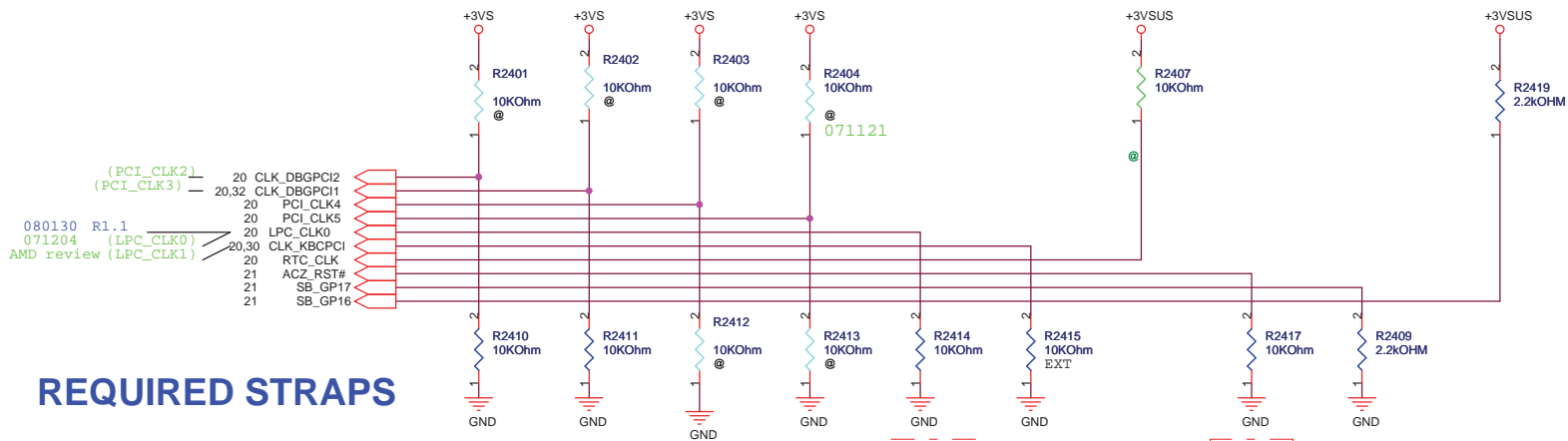
**SB700**  
Part 5 of 5

VSS_1	A2
VSS_2	A25
VSS_3	B1
VSS_4	D7
VSS_5	F20
VSS_6	G19
VSS_7	H8
VSS_8	K9
VSS_9	K11
VSS_10	K16
VSS_11	L4
VSS_12	L10
VSS_13	L12
VSS_14	L11
VSS_15	L14
VSS_16	L14
VSS_17	L16
VSS_18	M6
VSS_19	M10
VSS_20	M11
VSS_21	M13
VSS_22	M15
VSS_23	N4
VSS_24	N12
VSS_25	N14
VSS_26	P9
VSS_27	P10
VSS_28	P13
VSS_29	P11
VSS_30	P11
VSS_31	P15
VSS_32	R2
VSS_33	R2
VSS_34	R4
VSS_35	R10
VSS_36	R12
VSS_37	R12
VSS_38	R9
VSS_39	T11
VSS_40	T12
VSS_41	T14
VSS_42	U4
VSS_43	U14
VSS_44	V6
VSS_45	Y21
VSS_46	AB1
VSS_47	AB19
VSS_48	AB25
VSS_49	AE1
VSS_50	AE24
PCIE_CK_VSS_9	P23
PCIE_CK_VSS_10	R16
PCIE_CK_VSS_11	R19
PCIE_CK_VSS_12	T17
PCIE_CK_VSS_13	U18
PCIE_CK_VSS_14	V18
PCIE_CK_VSS_15	V20
PCIE_CK_VSS_16	V21
PCIE_CK_VSS_17	W19
PCIE_CK_VSS_18	W21
PCIE_CK_VSS_19	W22
PCIE_CK_VSS_20	W24
PCIE_CK_VSS_21	W25
PCIE_CK_VSS_8	L17

Remove R2405, R2406, R2416  
R2408, R2418, R2420, R2418

090405

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC\_CLK



**REQUIRED STRAPS**

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	ACZ_RST#	GP17	GP16
<b>PULL HIGH</b>	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	EC ENABLED	CLKGEN ENABLED	INTERNAL RTC  DEFAULT	ENABLE PCI MEM BOOT	H,H = Reserved H,L = SPI ROM	
<b>PULL LOW</b>	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI MEM BOOT DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM	

For SB700 A12 and later version

080204 R1.1  
Change the Text Comment

<b>ASUS</b>		<b>Title : SB700_STRAP</b>	
ASUSTeK Computer, INC		Engineer: N/A	
Size	Project Name		Rev
Custom	1201T		2.0
Date: Wednesday, October 14, 2009		Sheet	24 of 79

5

4

3

2

1

D

D

C

C

B


B

A

A

<http://laptop-motherboard-schematic.blogspot.com/>

<Variant Name>

		<b>Title : HDMI</b>	
ASUSTek COMPUTER INC		<b>Engineer: N/A</b>	
Size	Project Name	Rev	
A3	<b>1201T</b>	2.0	
Date: Wednesday, October 14, 2009		Sheet	25 of 79

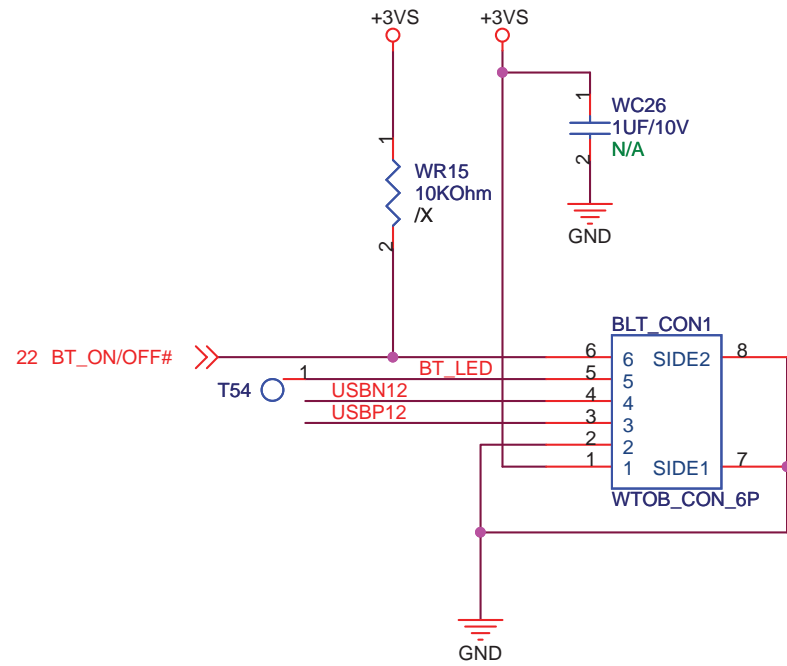
5

4

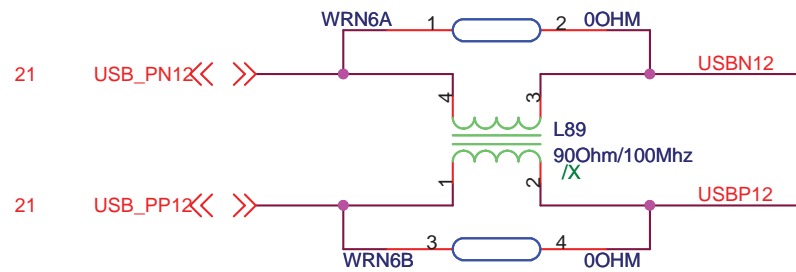
3

2

1

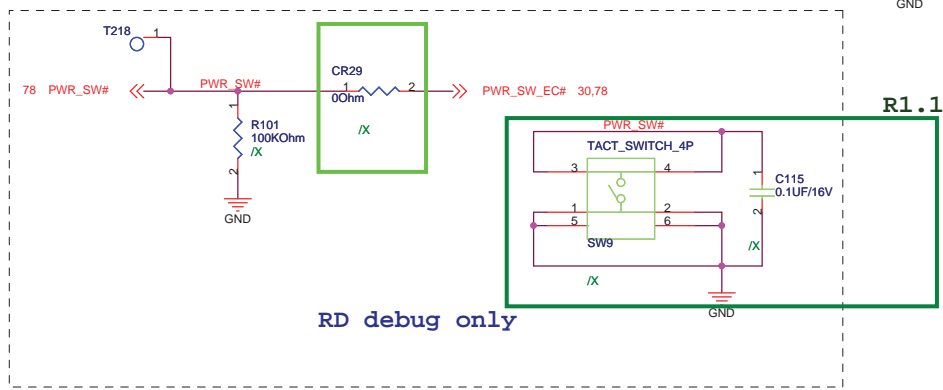
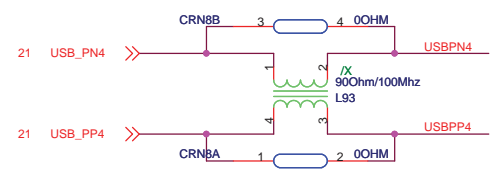
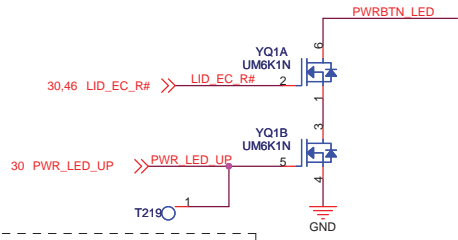
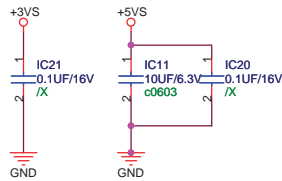
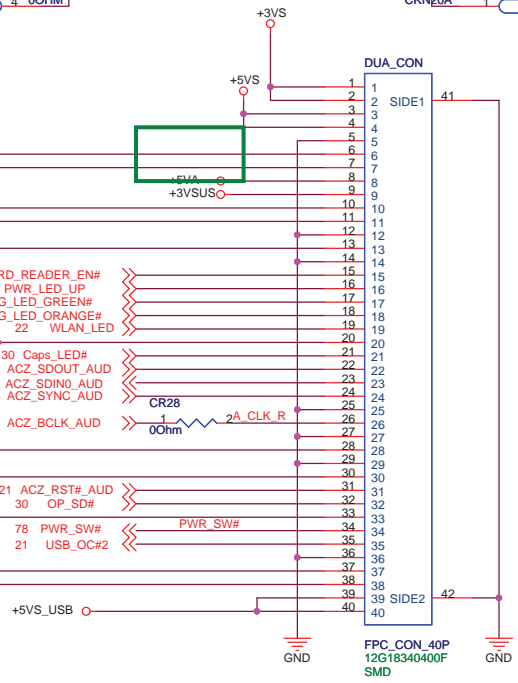
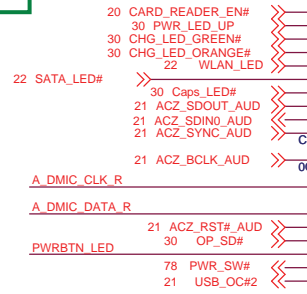
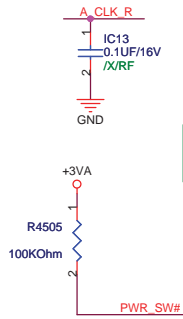
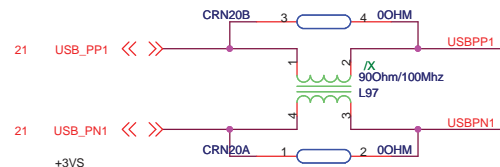
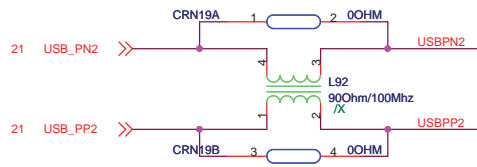


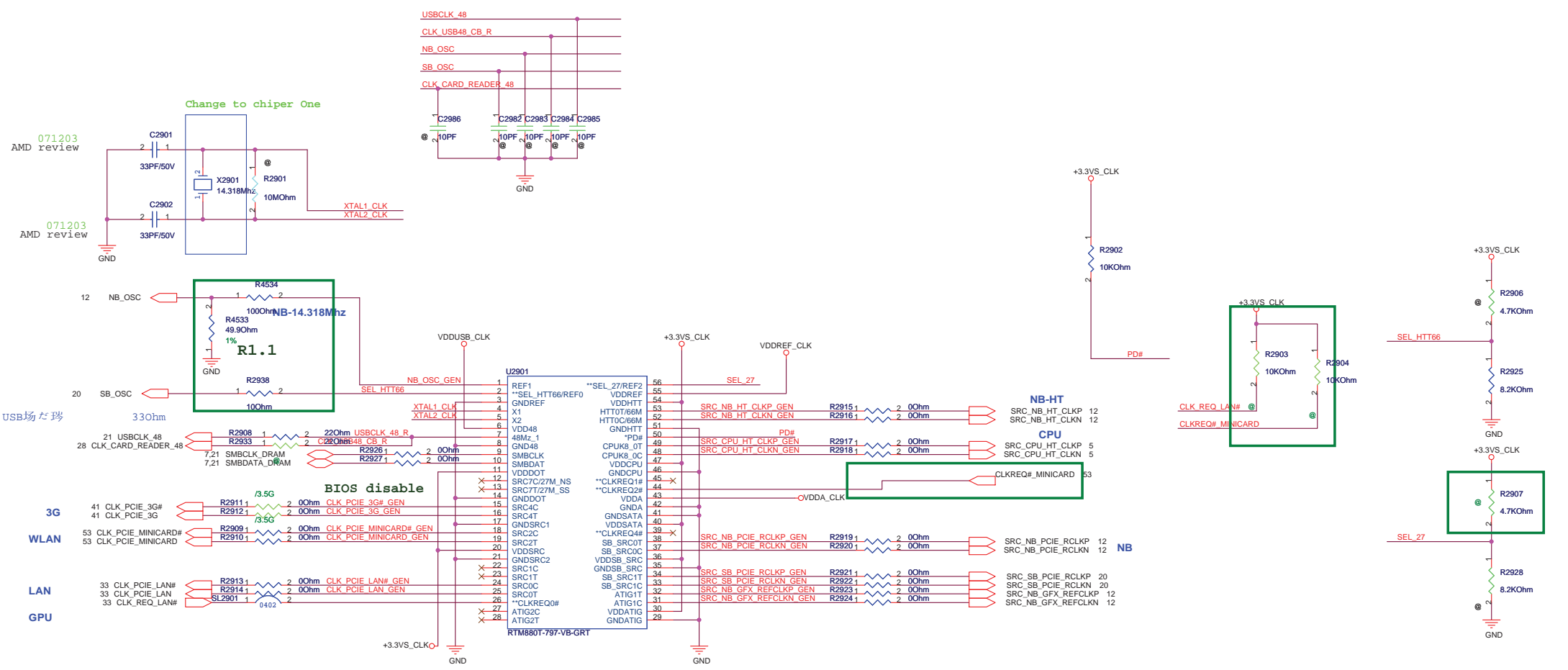
**BT Conn**



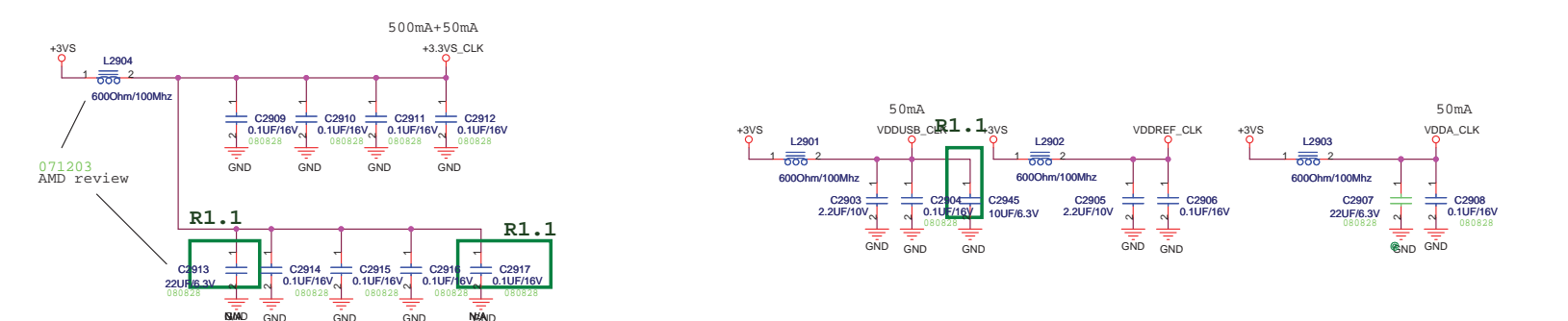
<Variant Name>

		<b>Title : Bluetooth</b>	
ASUSTek Computer INC.		Engineer: N/A	
Size A	Project Name <b>1201T</b>		Rev 2.0
Date Wednesday, October 14, 2009	Sheet 27	of 79	

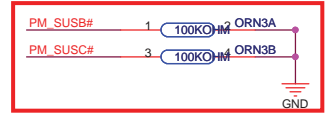
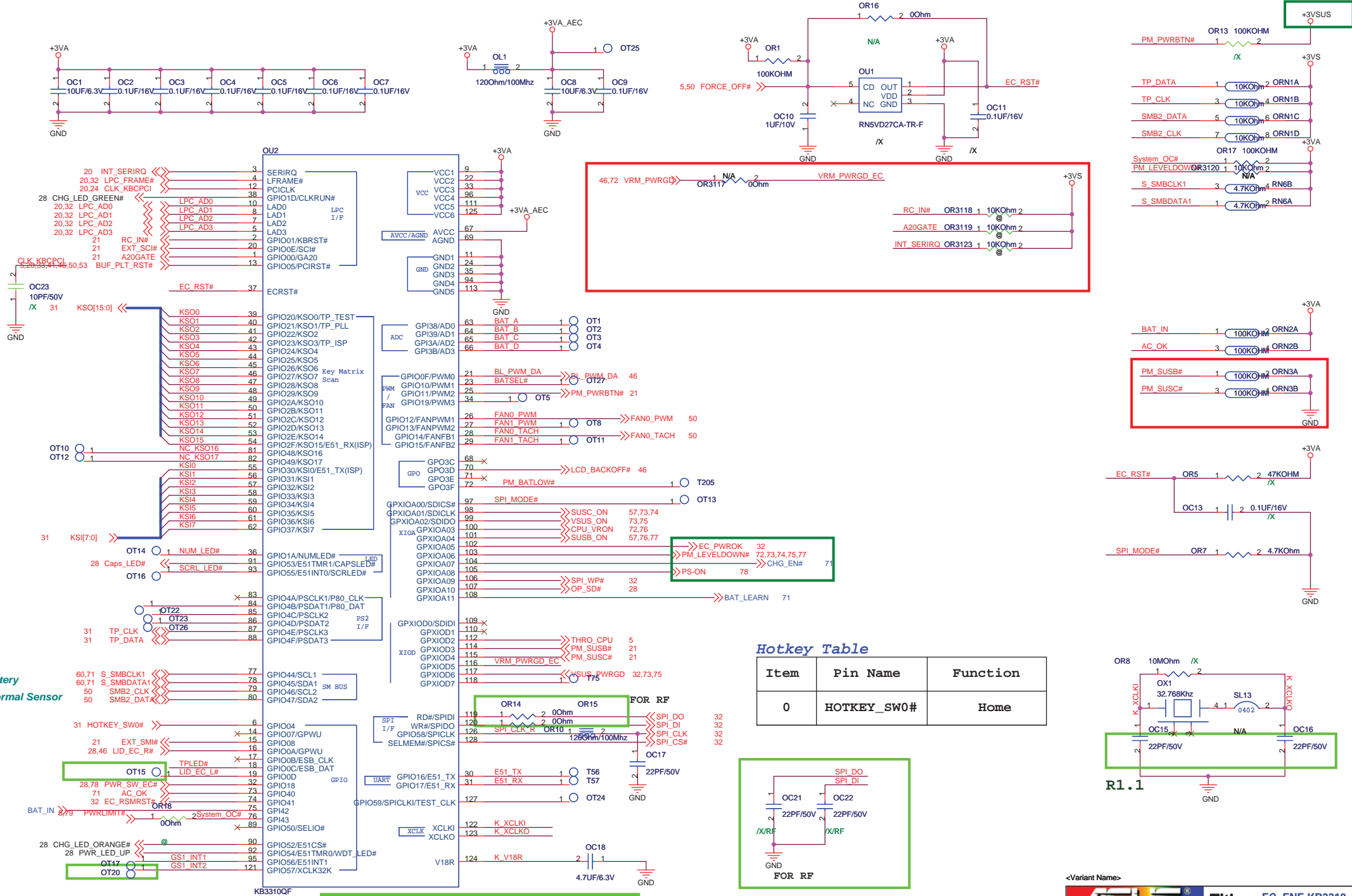




SEL_27	0	100 MHz differential spreading SRC clock
	1	27MHz non-spreading singled clock on pin12 27MHz spread clock on pin13.
SEL_HTT66	0	100 MHz differential HTT clock
	1	66MHz 3.3V single ended HTT clock

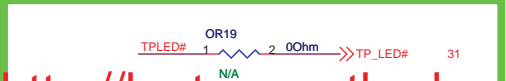
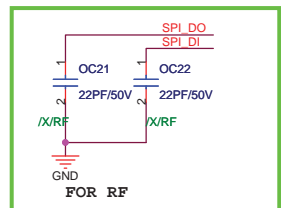
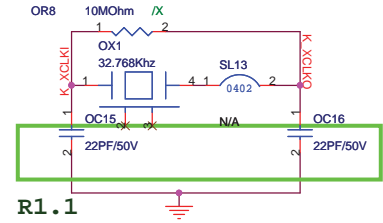


ASUS  
ASUSTeK COMPUTER INC  
Title: RTM880T-797-VB-GRT  
Engineer: N/A  
Size: Project Name  
Custom: 1201T  
Rev: 2.0  
Date: Wednesday, October 14, 2009  
Sheet: 29 of 79



### Hotkey Table

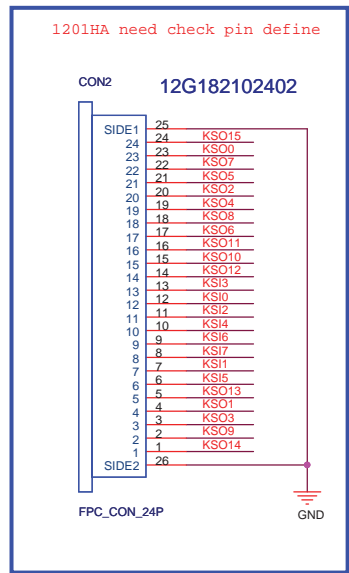
Item	Pin Name	Function
0	HOTKEY_SW0#	Home



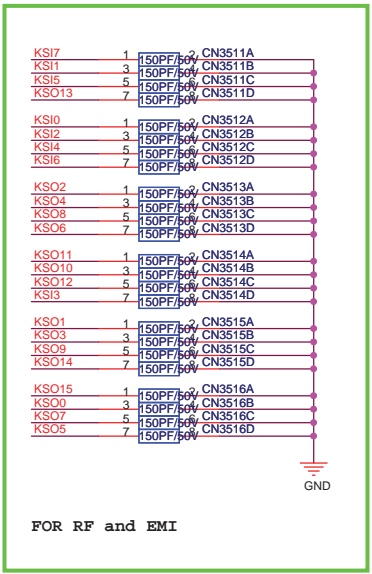
<http://laptop-motherboard-schematic.blogspot.com/>



1201HA need check pin define



<<KSO[15:0] 30  
 >>KSI[7:0] 30

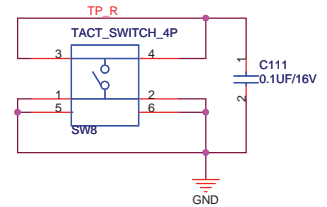
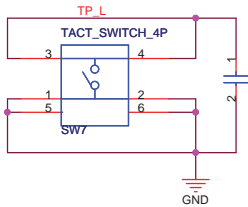


FOR RF and EMI

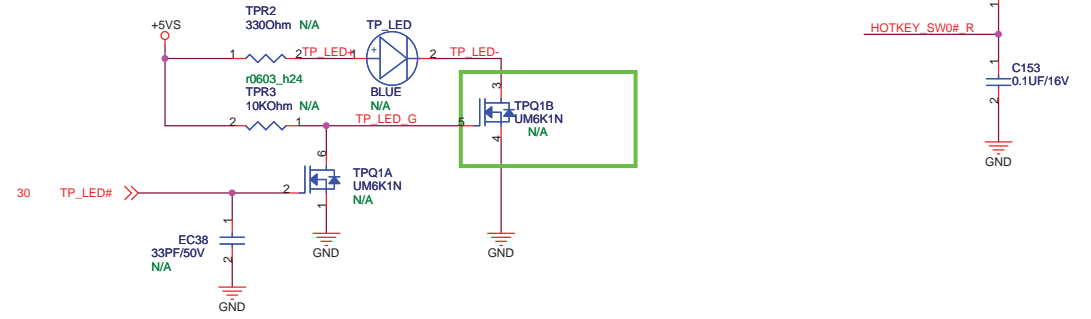
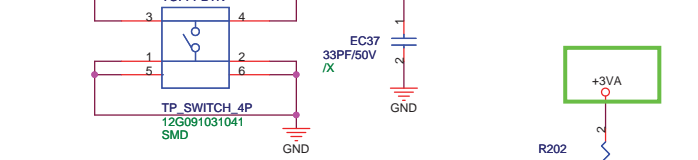
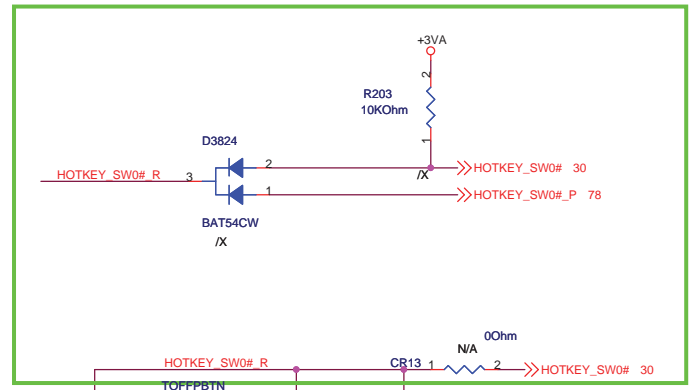
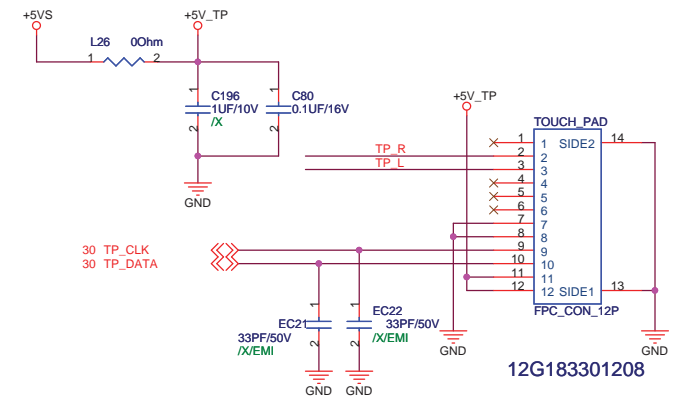
R1.1 change to 150pf

For Keyboard Connector

8/3 Del Keyboard ESD Protect



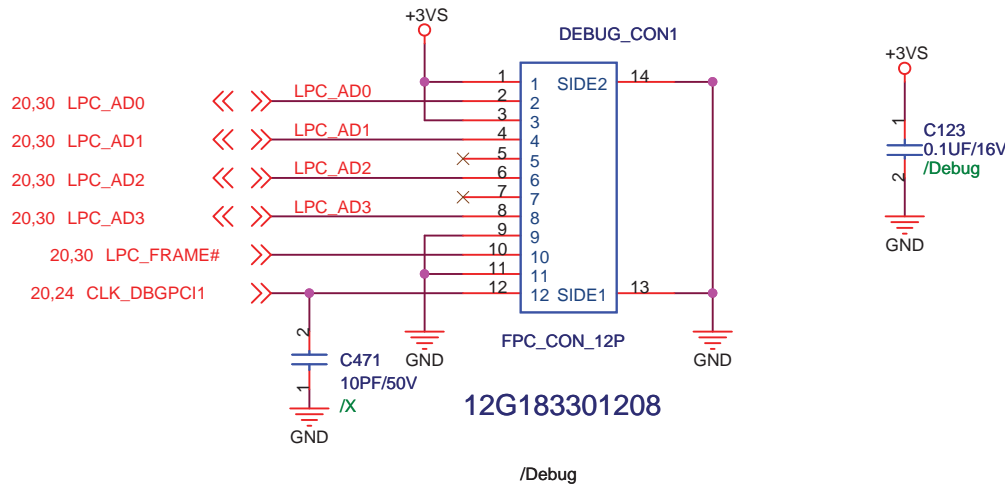
For Touch-Pad



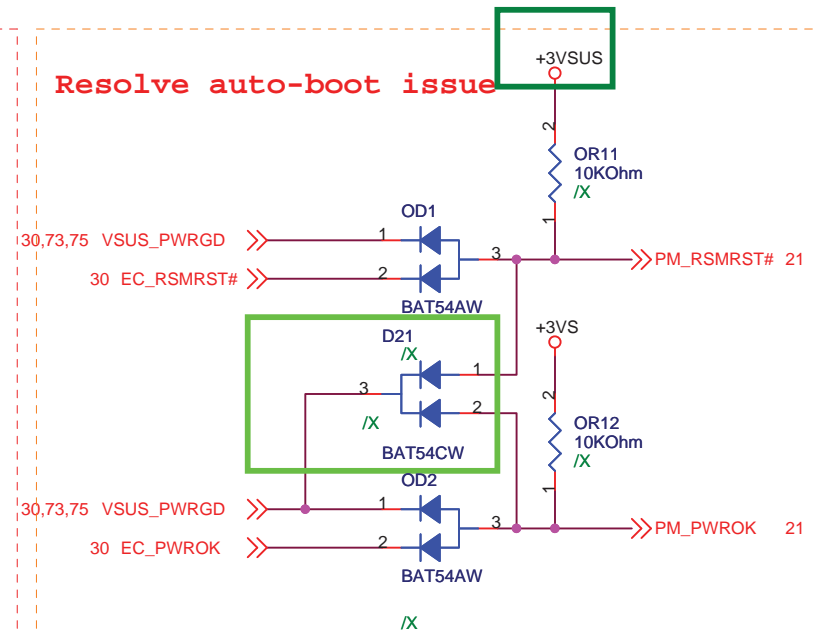
<Variant Name>

<b>ASUS</b>		<b>Title : KB_Touch Pad</b>	
ASUSTek Computer INC.		Engineer: N/A	
Size	Project Name		Rev
A3	1201T		2.0
Date: Wednesday, October 14, 2009		Sheet	31 of 79

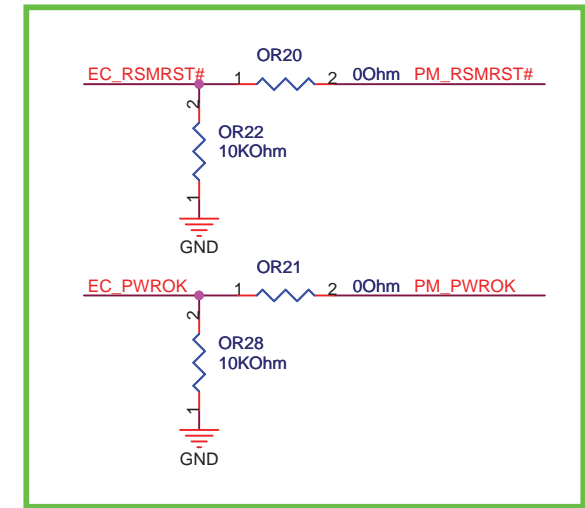
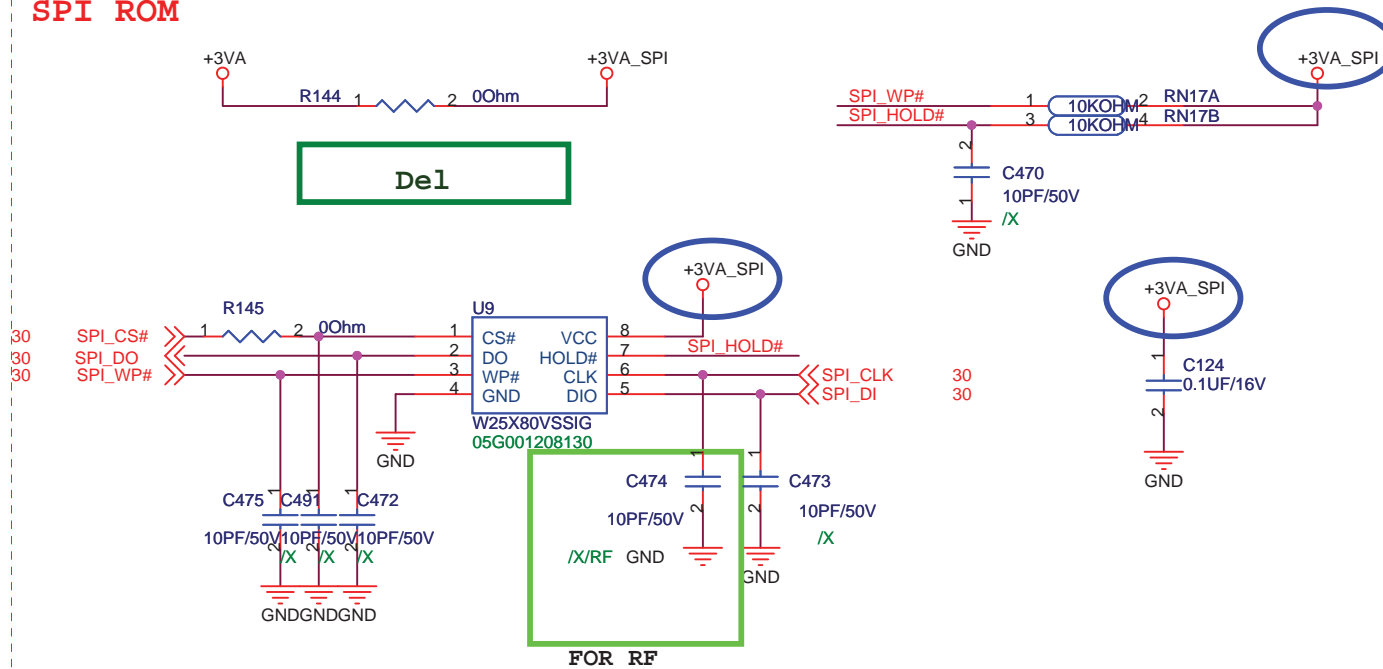
**For Debug**



**Resolve auto-boot issue**

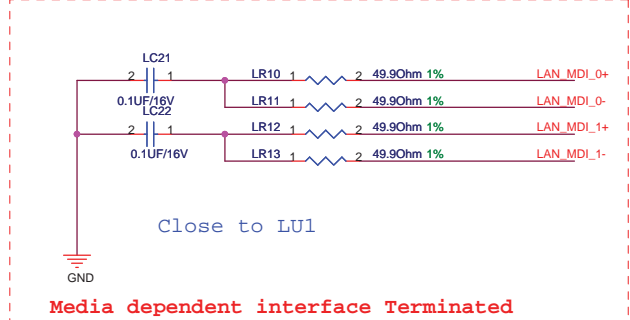
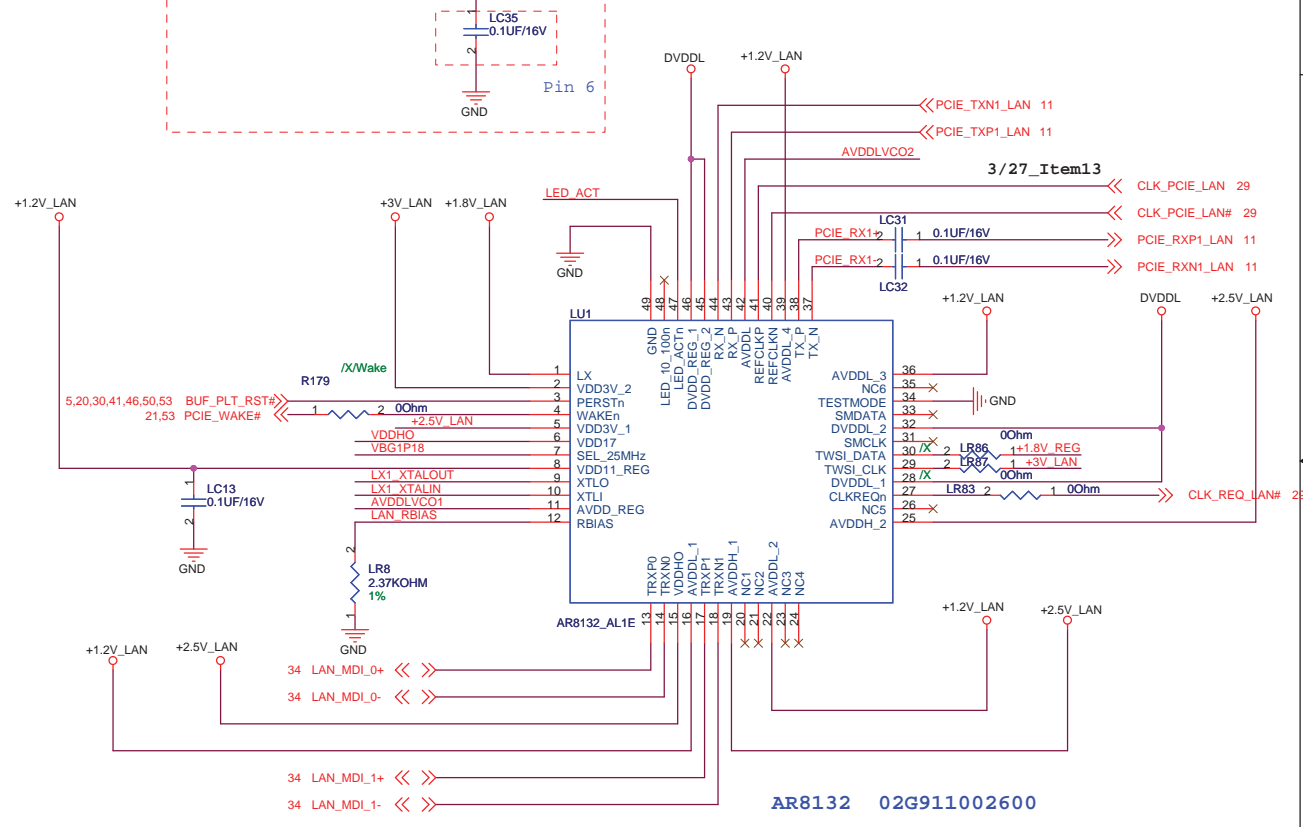
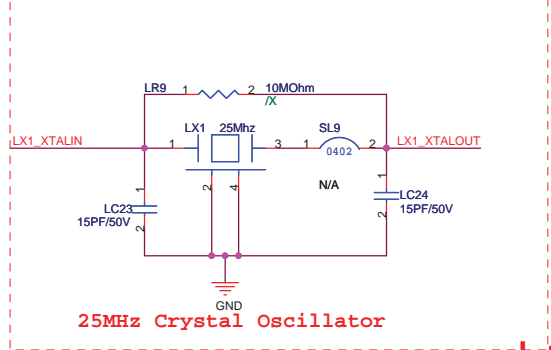
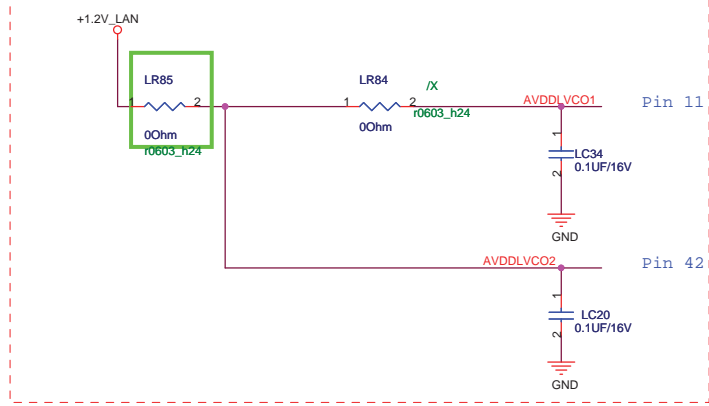
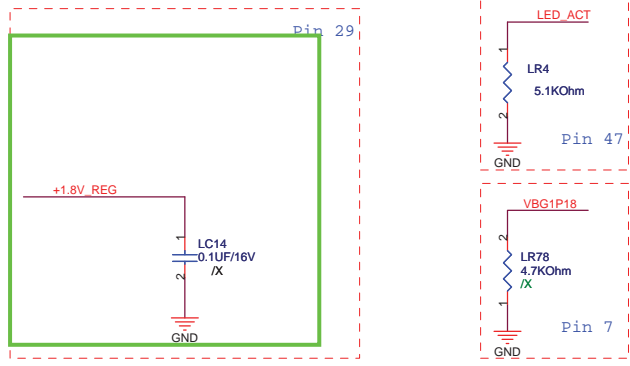
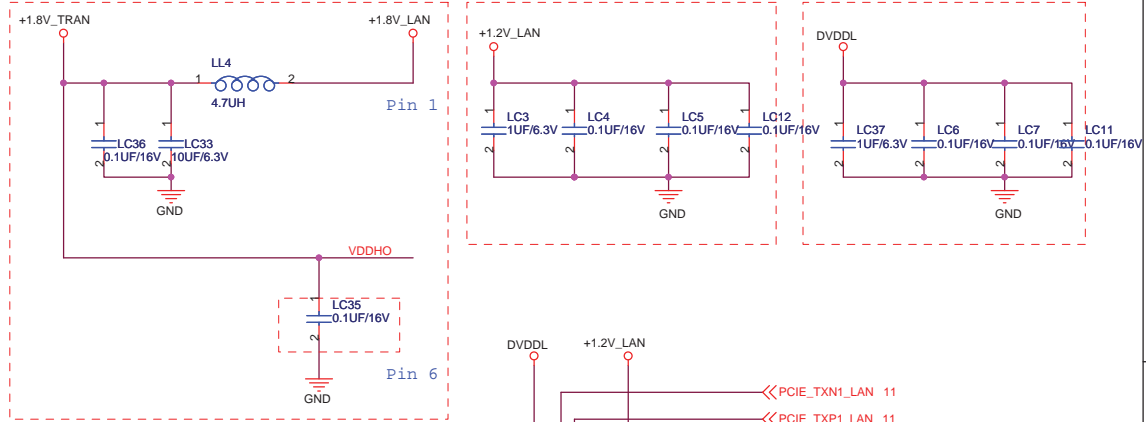
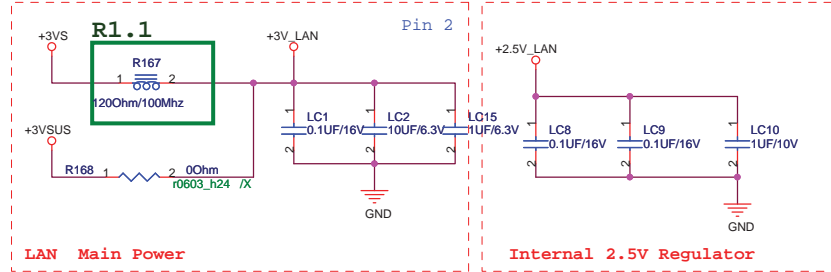


**SPI ROM**



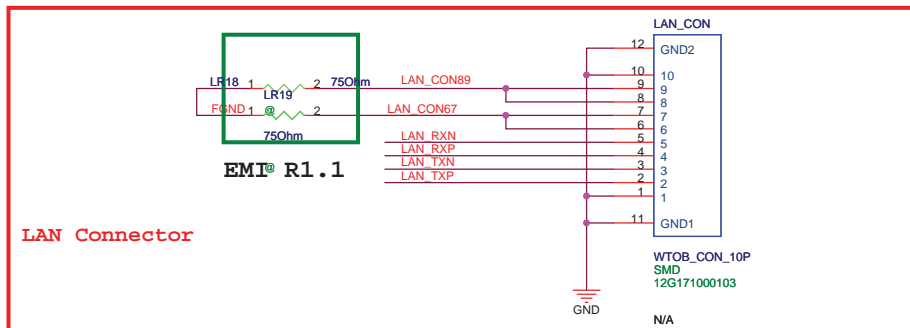
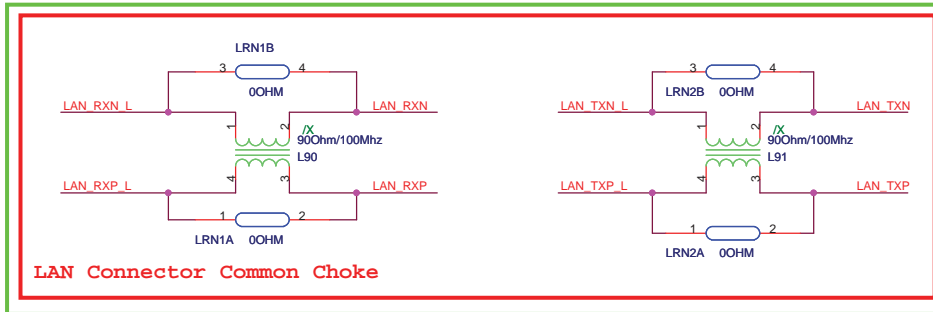
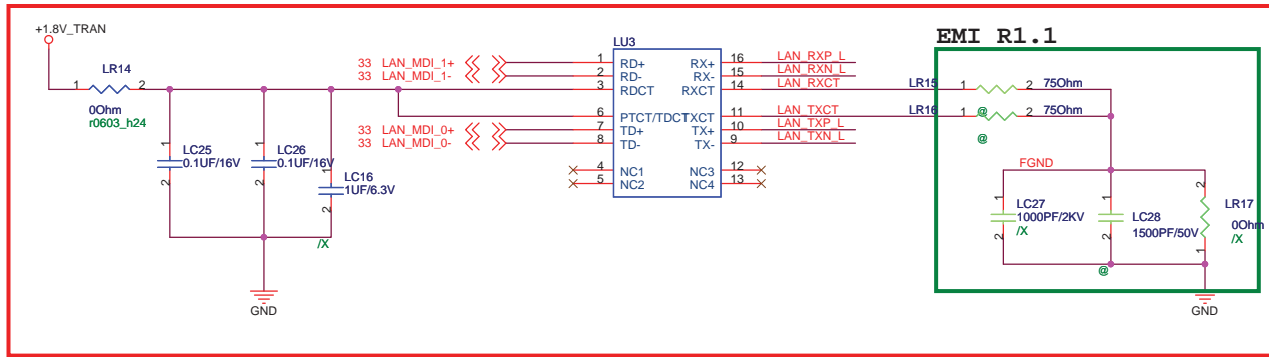
<Variant Name>

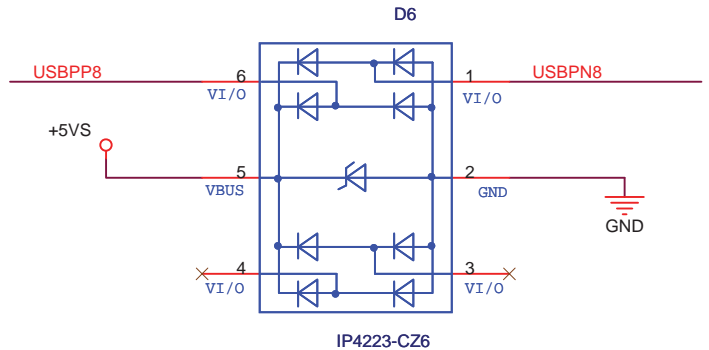
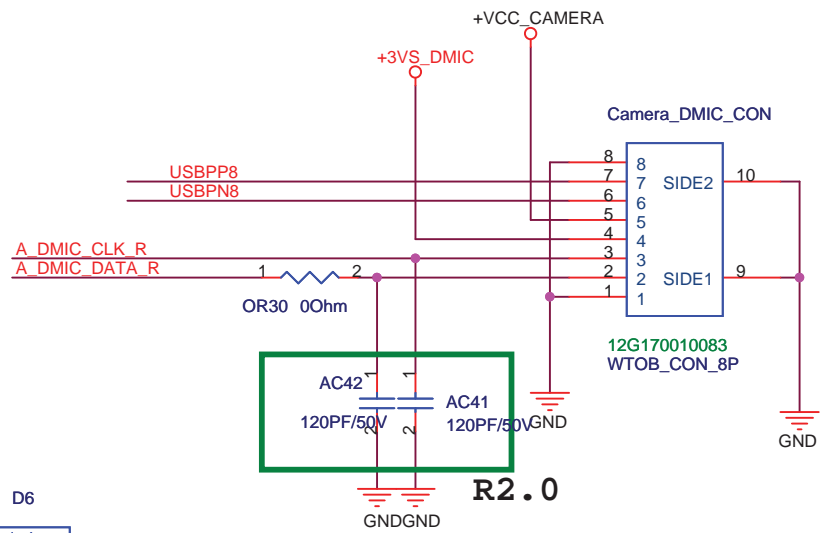
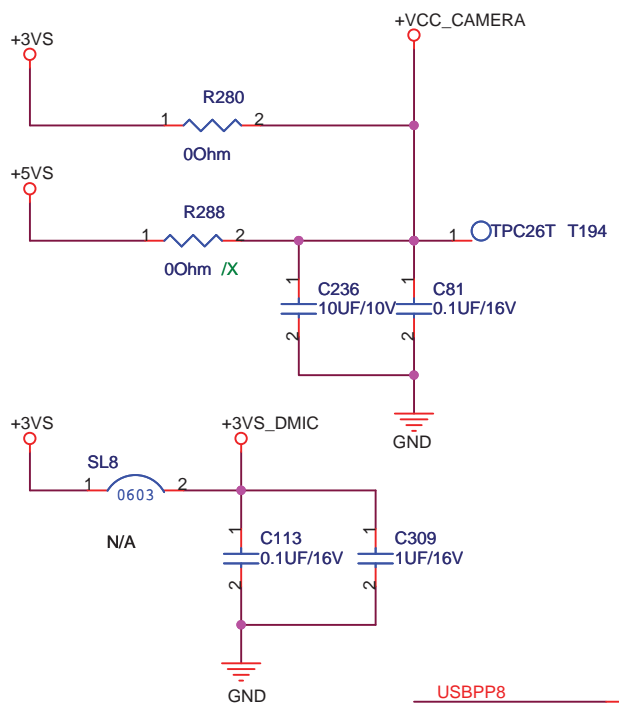
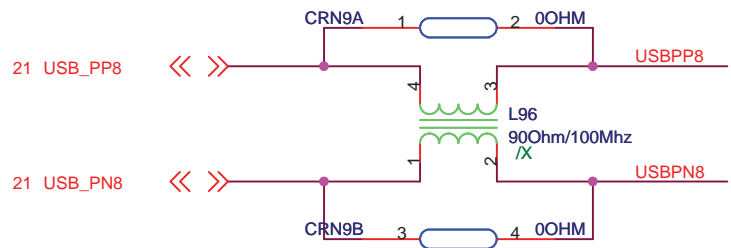
<b>ASUS</b>		<b>Title : SPI ROM/ Debug</b>	
ASUSTek Computer INC.		Engineer: N/A	
Size A4	Project Name 1201T	Rev 2.0	
Date: Wednesday, October 14, 2009	Sheet	32	of 79



<Variant Name>

<b>ASUS</b>		<b>Title : AR8113/AR8132</b>
ASUSTek Computer INC		Engineer: N/A
Size A3	Project Name <b>1201T</b>	Rev 2.0
Date: Wednesday, October 14, 2009		Sheet 33 of 79






<Variant Name>

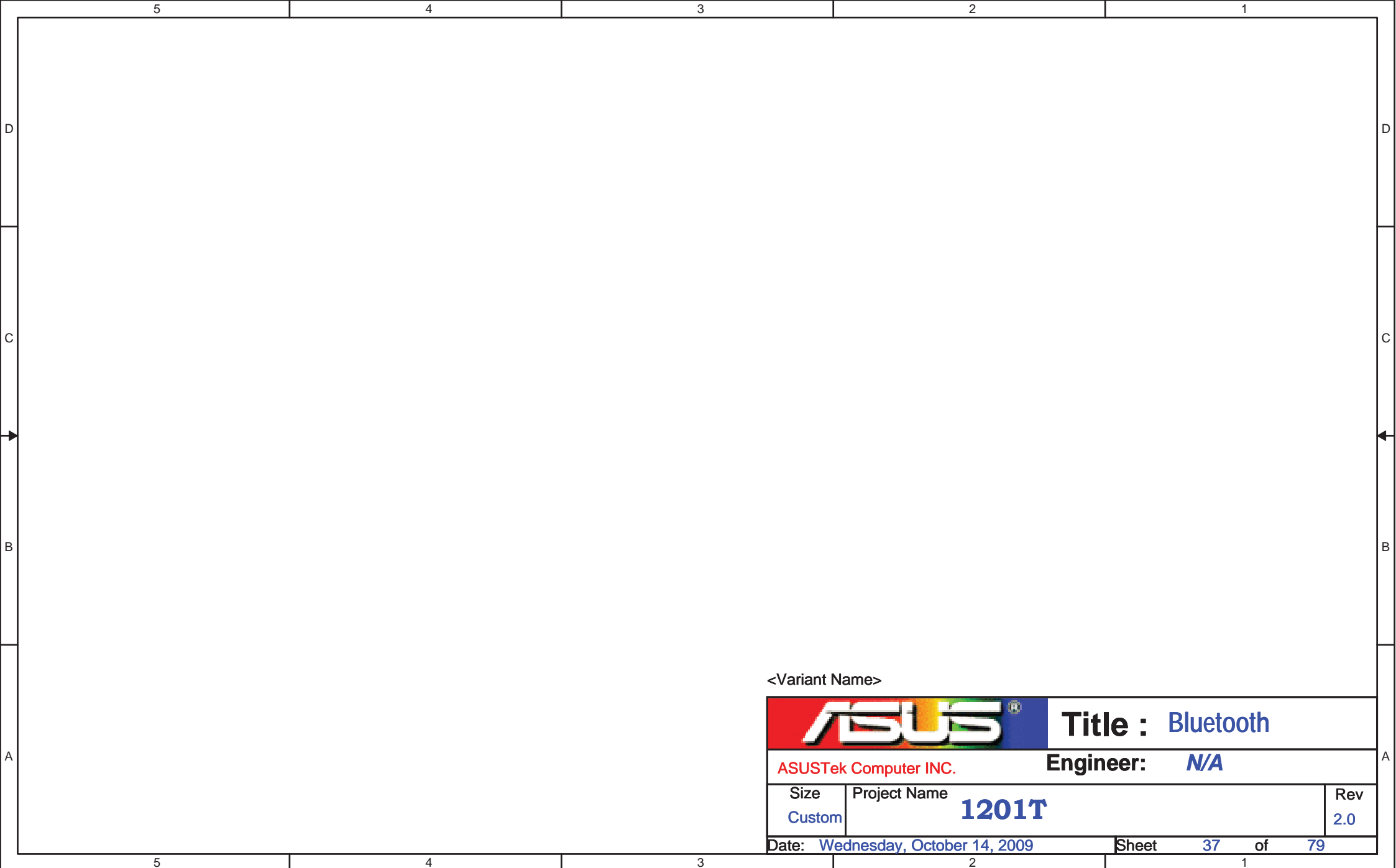
<b>ASUS</b>		<b>Title : CMOS</b>	
ASUSTek Computer INC.		Engineer: N/A	
Size	Project Name	Rev	
A4	<b>1201T</b>	2.0	
Date:	Wednesday, October 14, 2009	Sheet	35 of 79

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<http://laptop-motherboard-schematic.blogspot.com/>

<Variant Name>

		<b>Title : Bluetooth</b>	
ASUSTek Computer INC.		<b>Engineer: N/A</b>	
Size Custom	Project Name <b>1201T</b>	Rev 2.0	
Date: Wednesday, October 14, 2009		Sheet	36 of 79



<Variant Name>

		<b>Title :</b> Bluetooth	
ASUSTek Computer INC.		<b>Engineer:</b> N/A	
Size Custom	Project Name <b>1201T</b>		Rev 2.0
Date: Wednesday, October 14, 2009		Sheet 37 of 79	

5

4

3

2

1

D

D

C

C

B

B

A

A

<Variant Name>

		<b>Title :</b> Bluetooth	
ASUSTek Computer INC.		<b>Engineer:</b> N/A	
Size Custom	Project Name <b>1201T</b>		Rev 2.0
Date: Wednesday, October 14, 2009		Sheet 38 of 79	

5

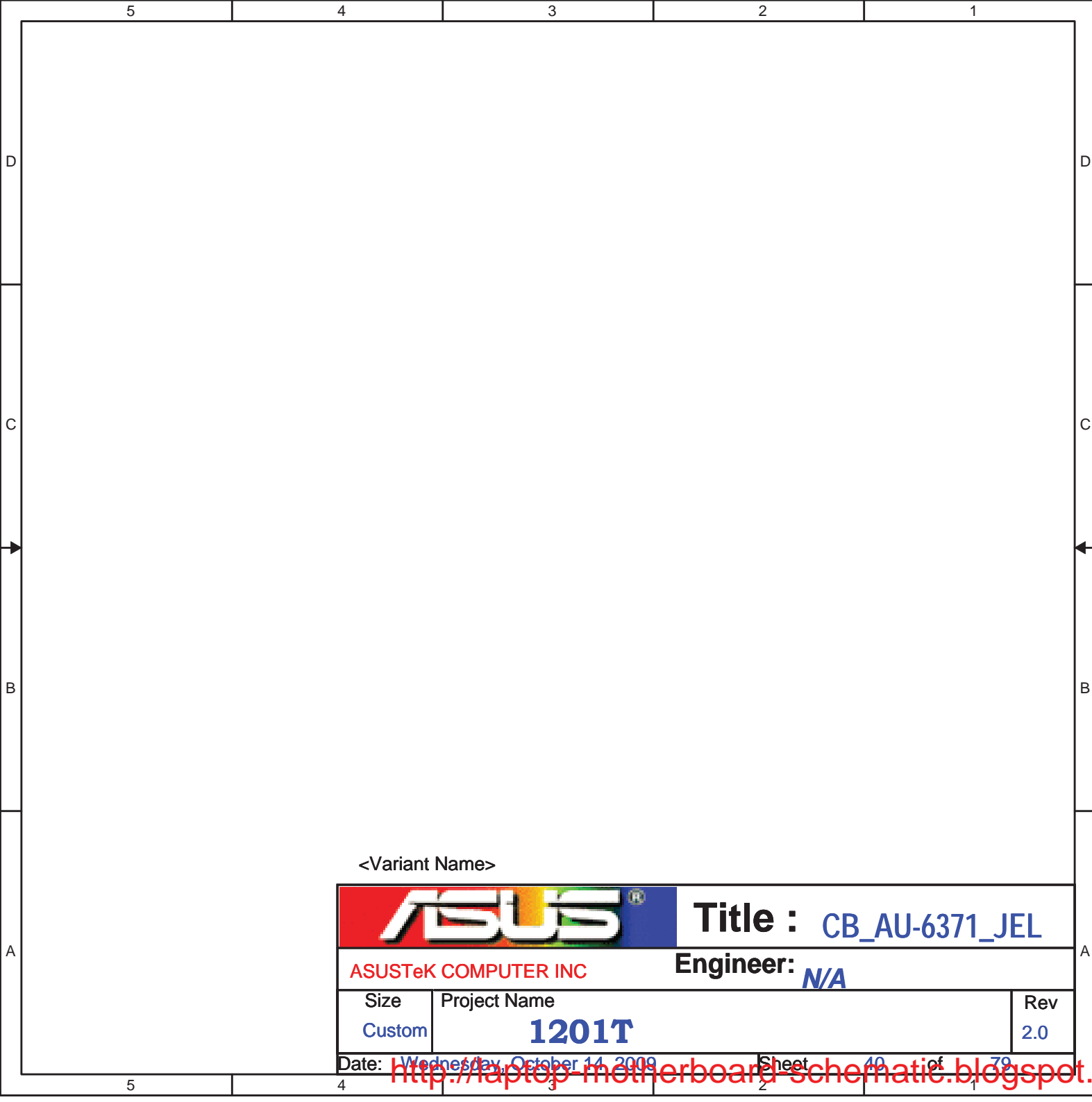
4

3


2

1

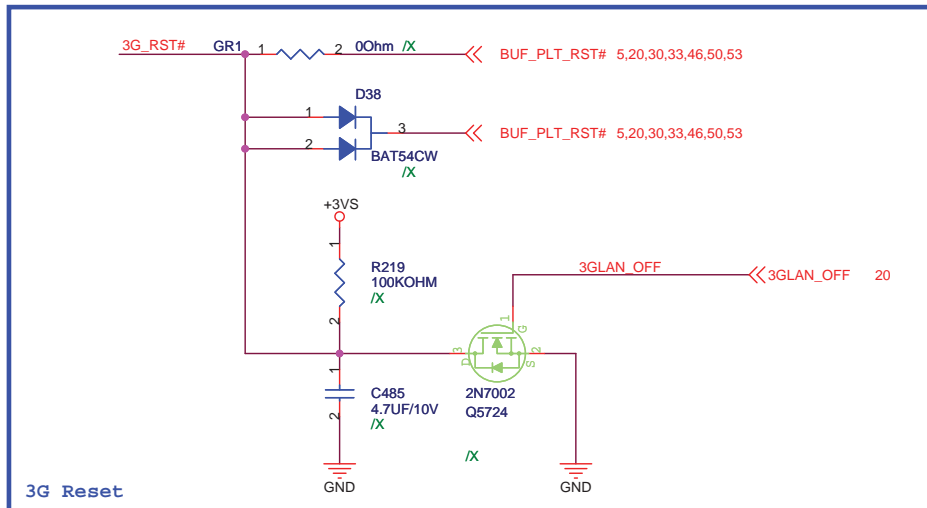
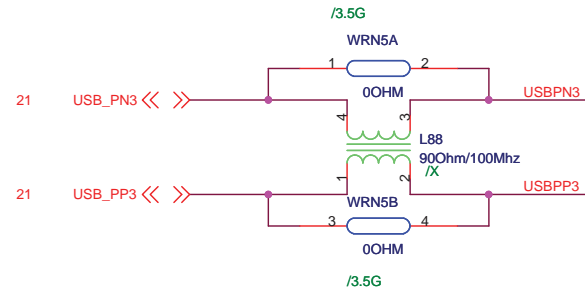
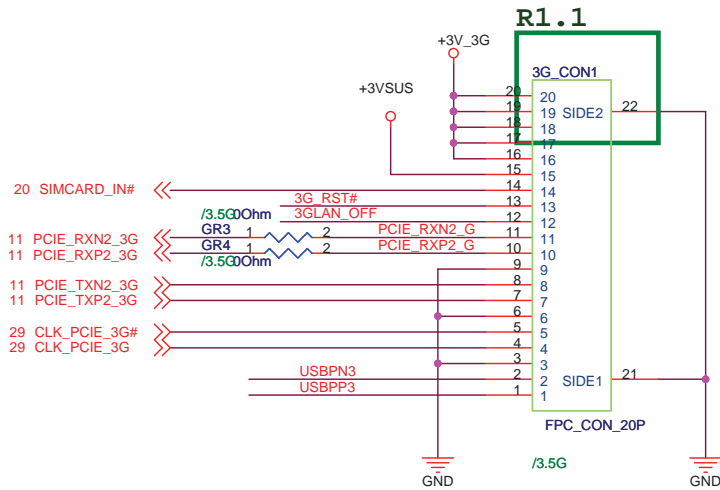
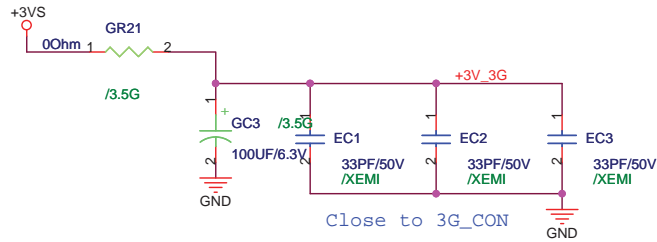




<Variant Name>

		<b>Title :</b> CB_AU-6371_JEL
ASUSTeK COMPUTER INC		<b>Engineer:</b> N/A
Size Custom	Project Name <b>1201T</b>	Rev 2.0

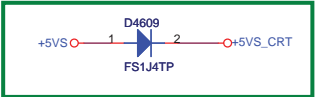
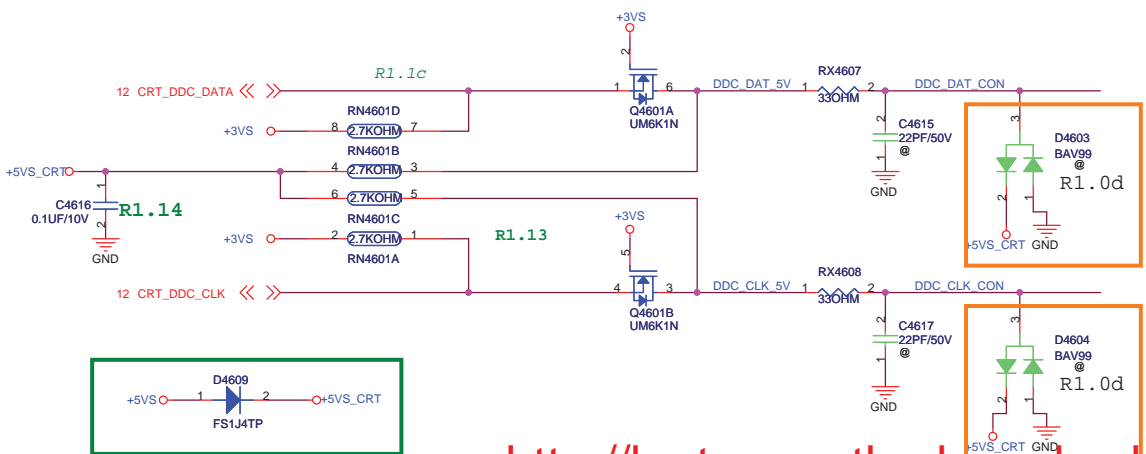
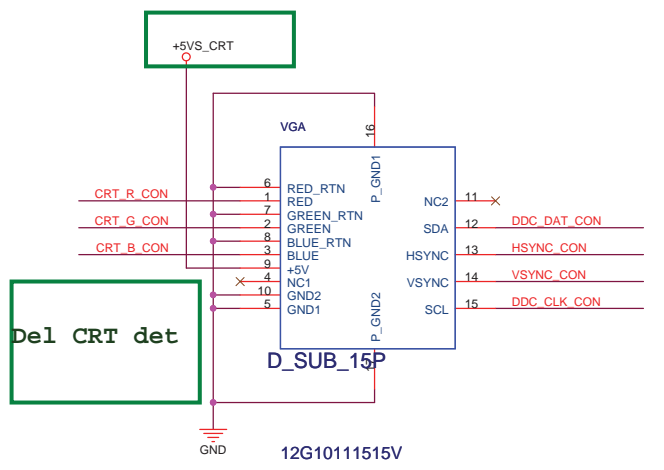
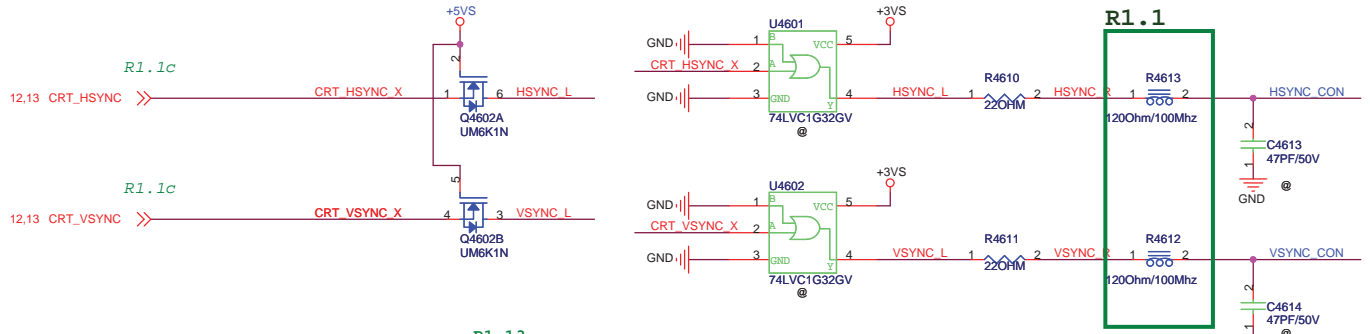
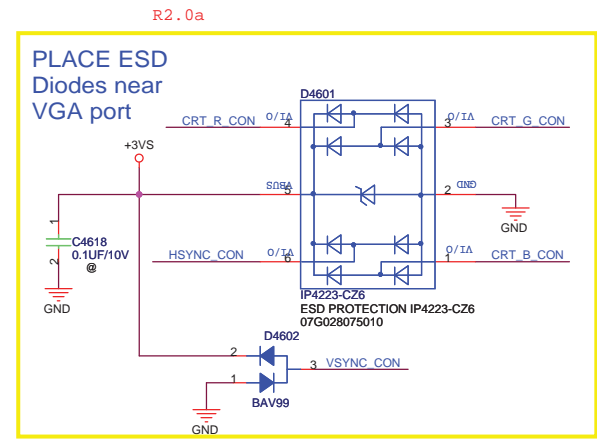
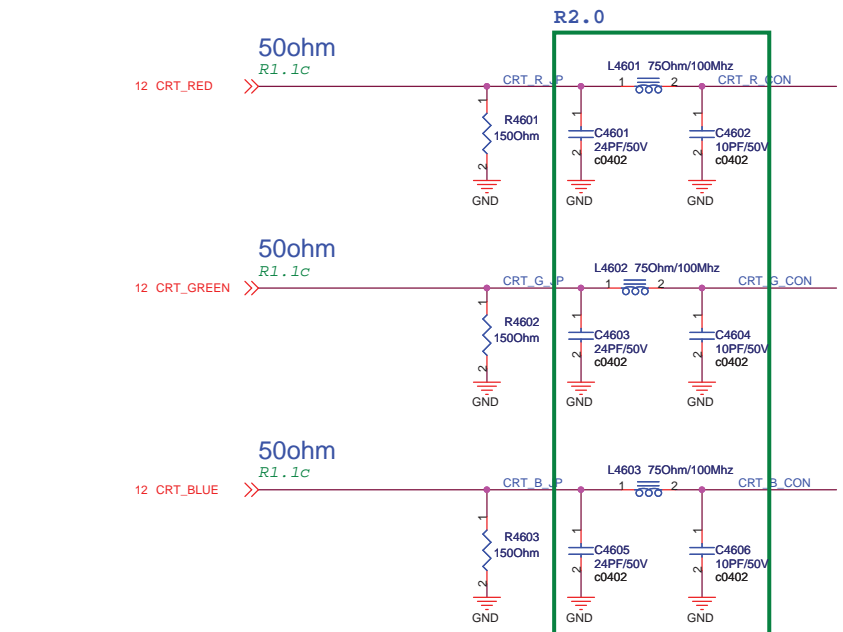
Date: Wednesday, October 14, 2009 Sheet 40 of 78



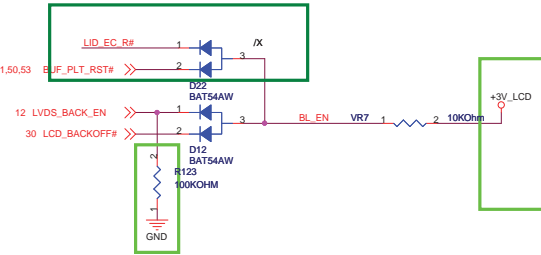
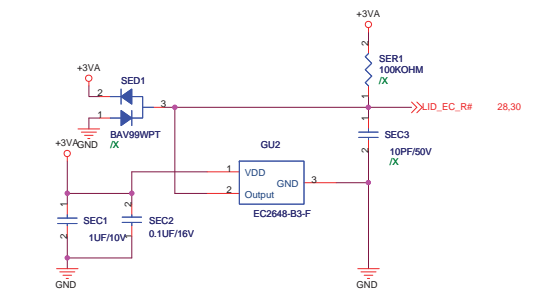
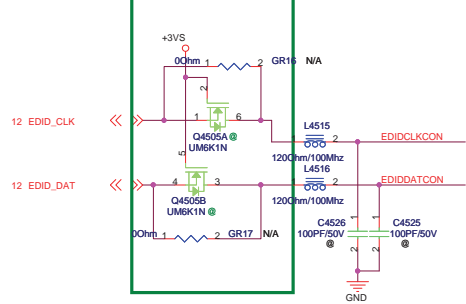
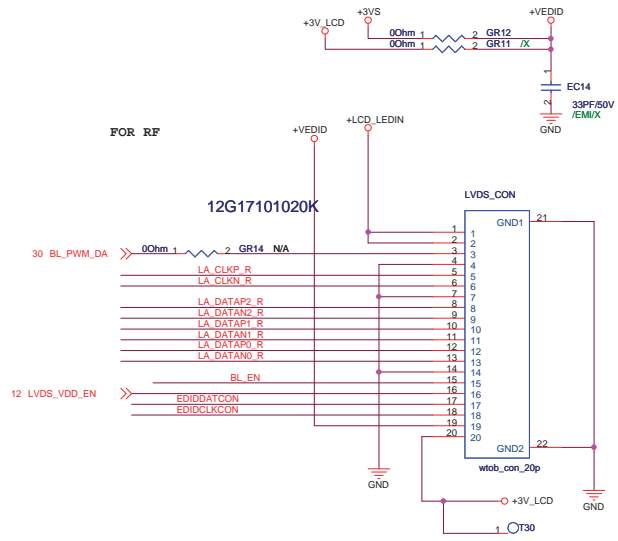
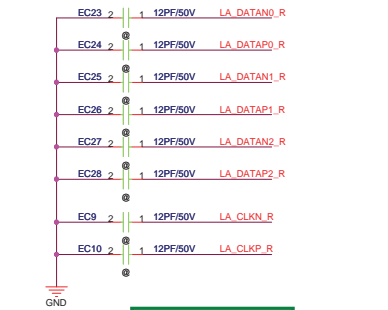
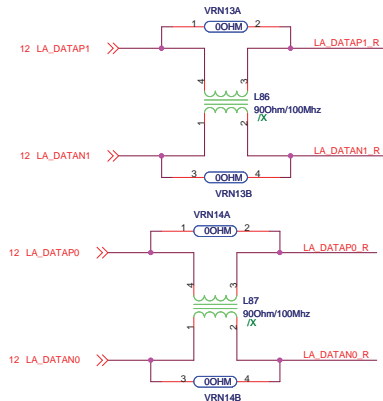
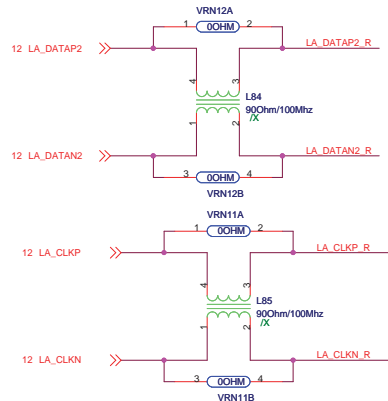
<Variant Name> 3.5G Module & External Antenna

**ASUS** Title : **ASUSTek Computer INC.** Engineer: **N/A**

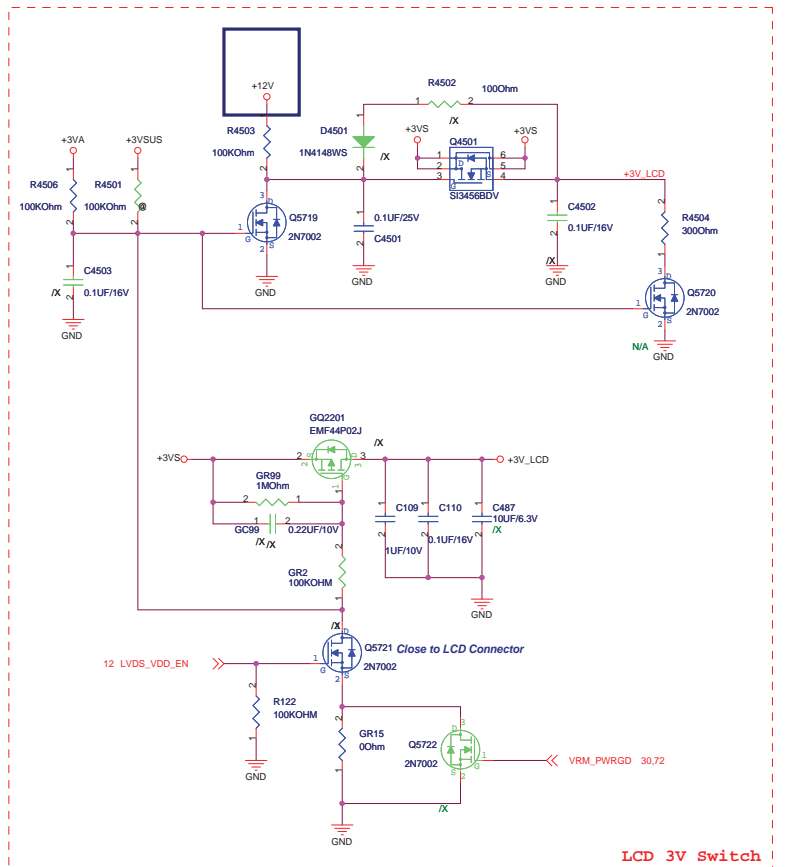
Size	Project Name	Rev
Custom	1201T	2.0
Date: Wed 8/21/2013 12:09	Sheet	41 of 79



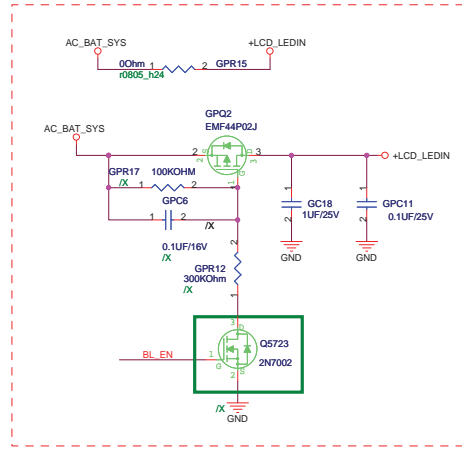
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Backlight Enable Discharge

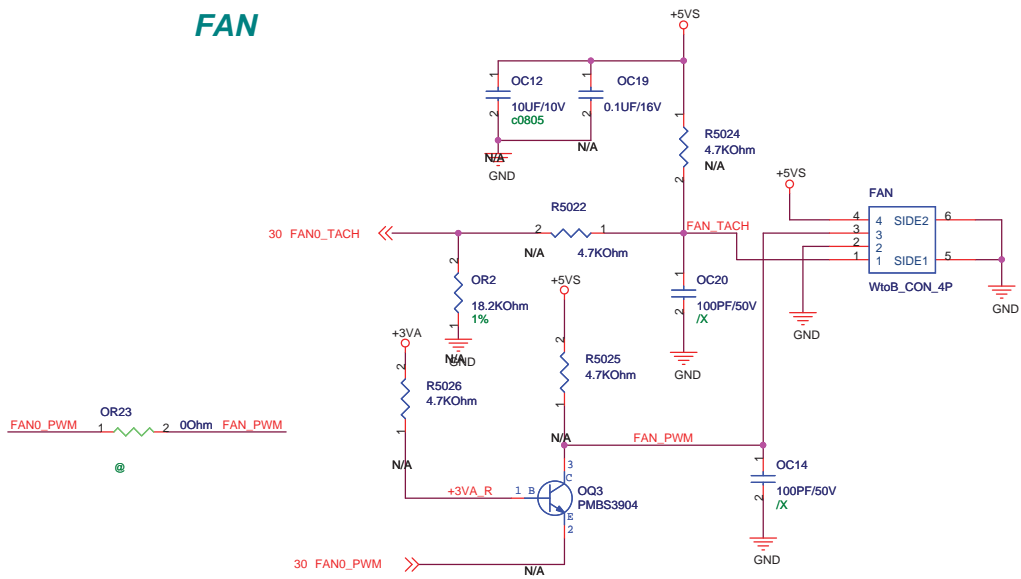


LCD 3V Switch

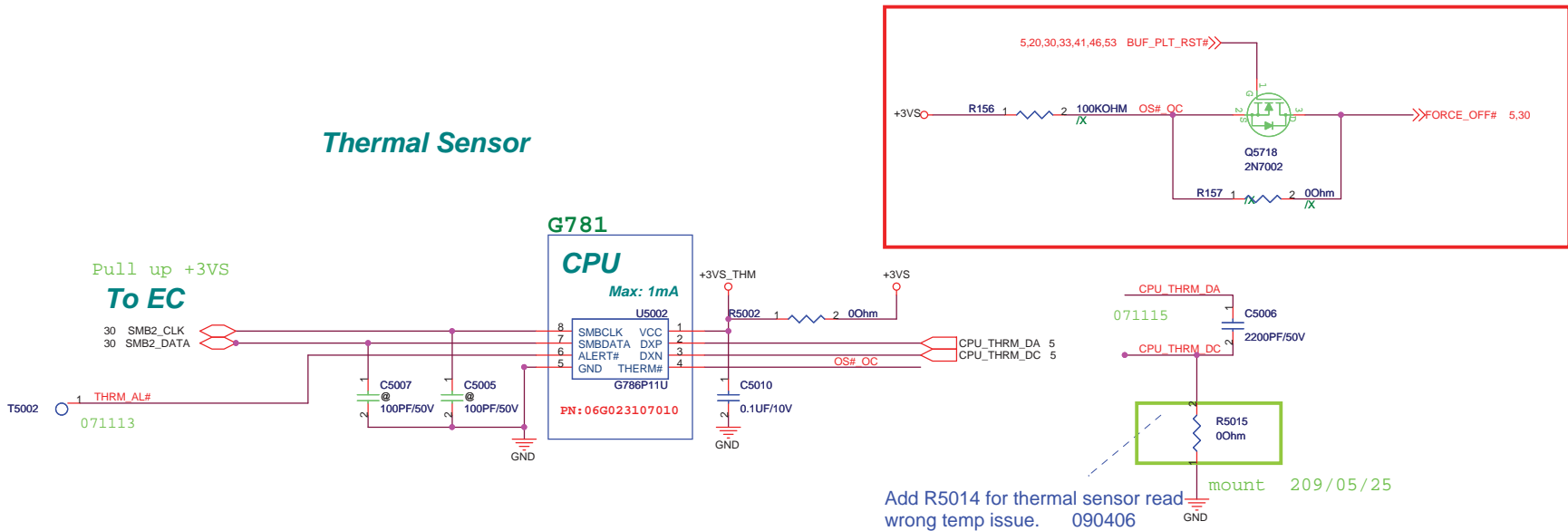


ASUS		Title : LVDS Conn
ASUSTek Computer INC.		Engineer: N/A
Size	Project Name	Rev 2.0
Date	Wednesday, 23 October 2008	Sheet 46 of 79

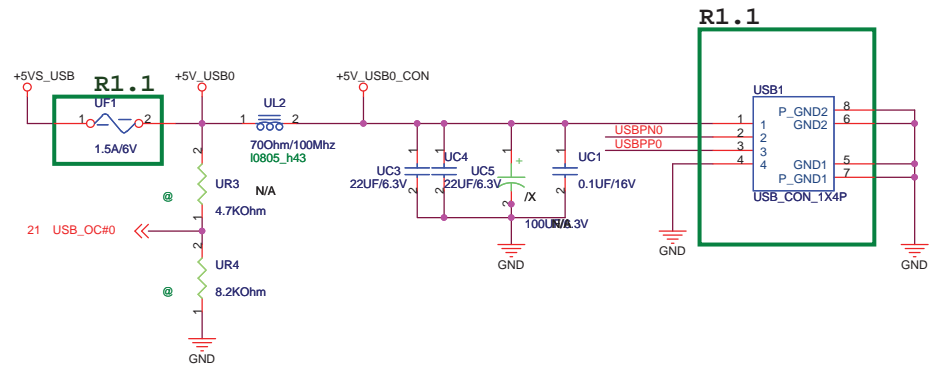
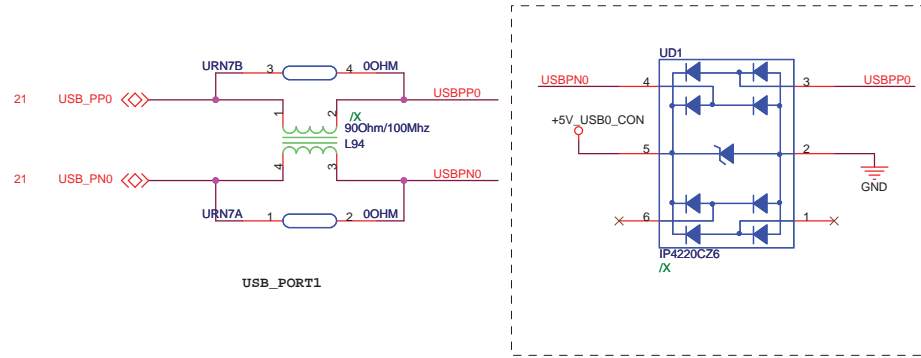
# FAN



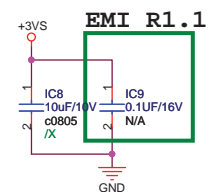
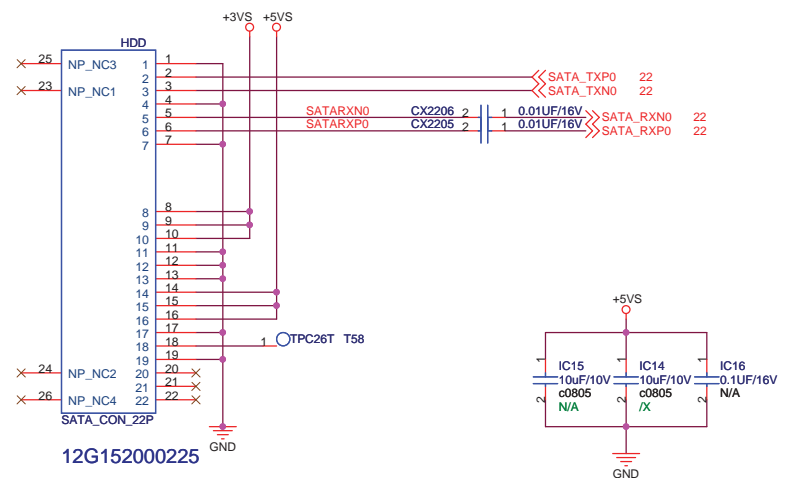
# Thermal Sensor



ASUS		Title : FAN_THERMAL SENSOR	
ASUSTek Computer INC.		Engineer: N/A	
Size	Project Name	Rev	
Custom	1201T	2.0	
Date: Wednesday, October 14, 2009	Sheet	50	of 79

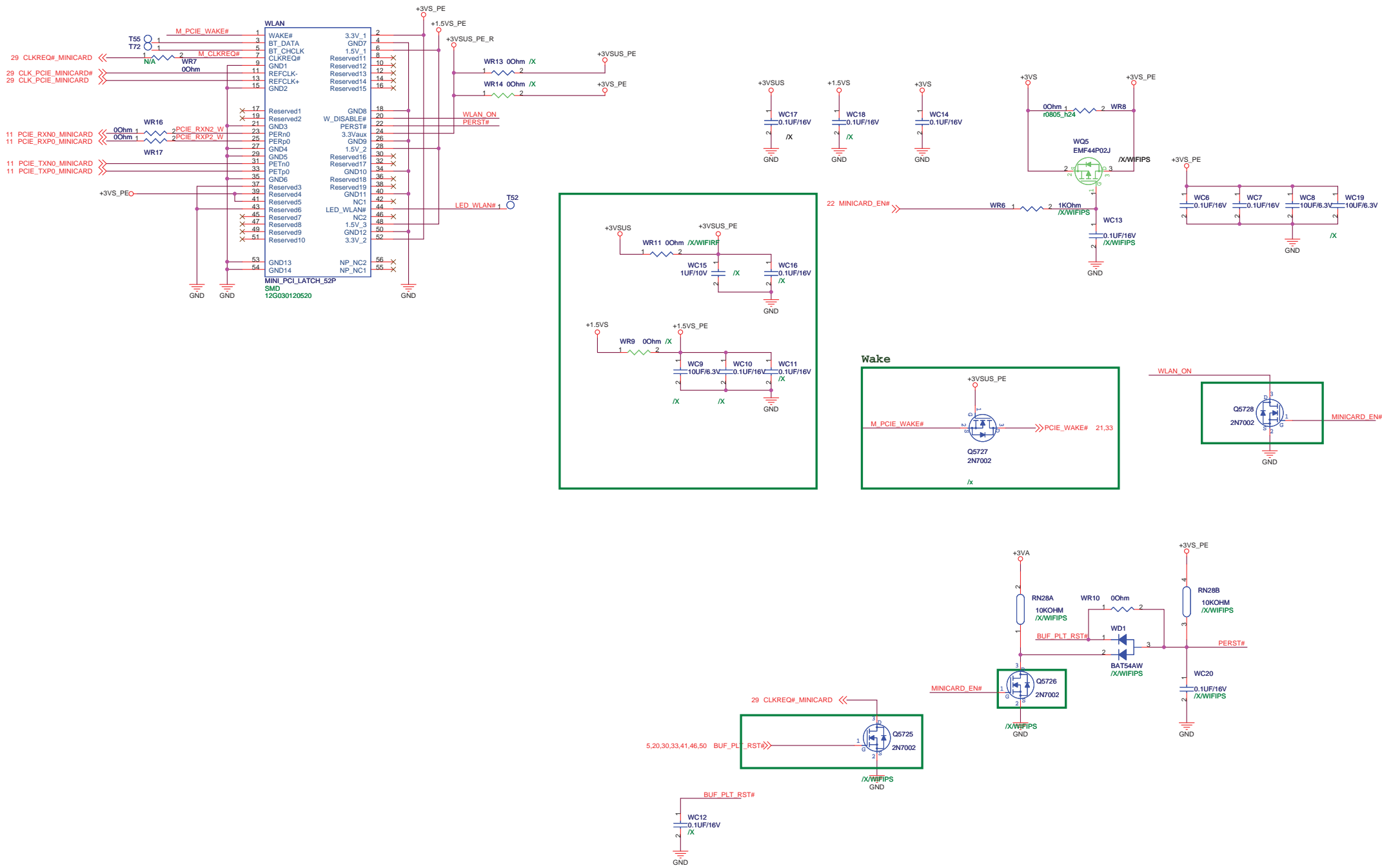


## SATA HDD Connector

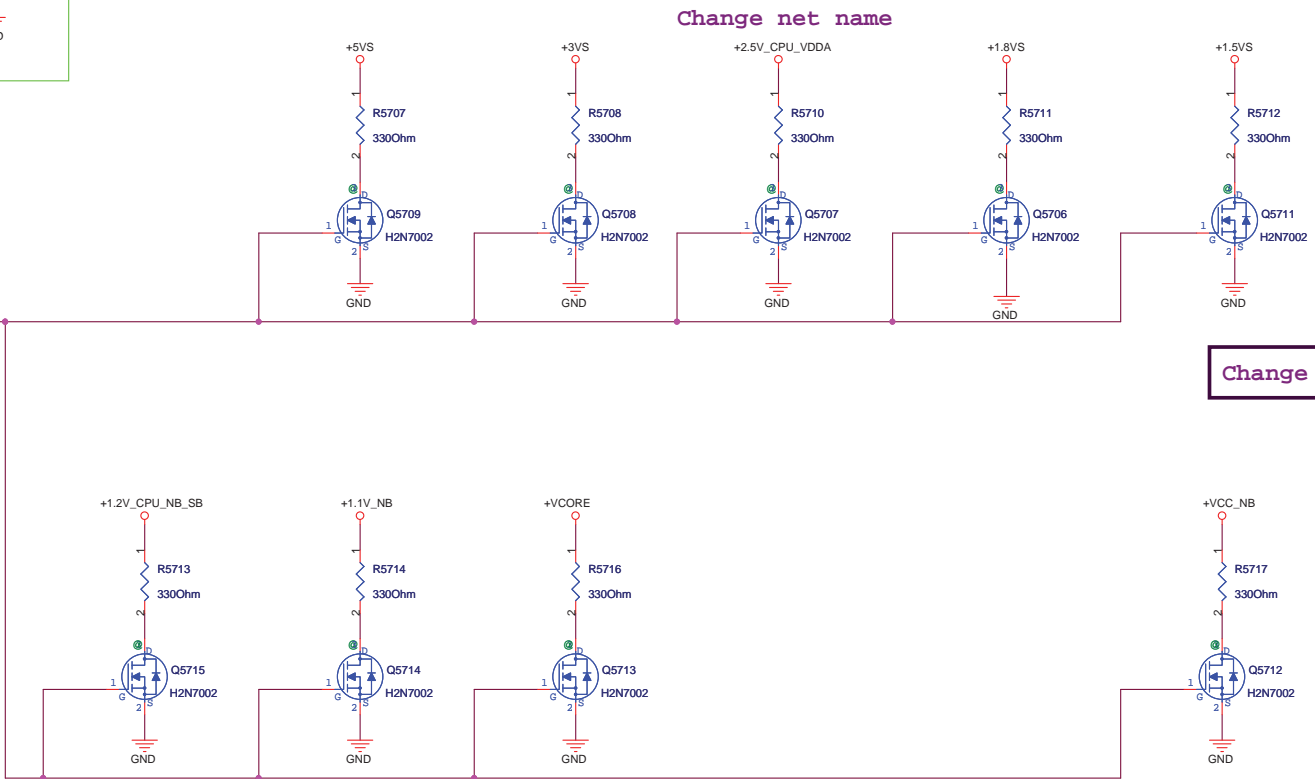
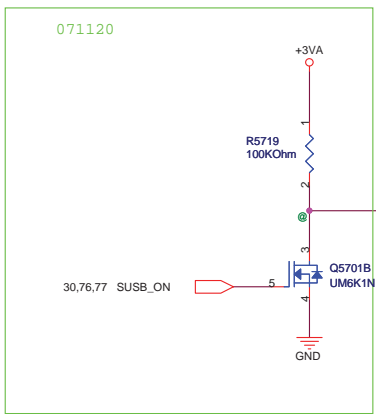
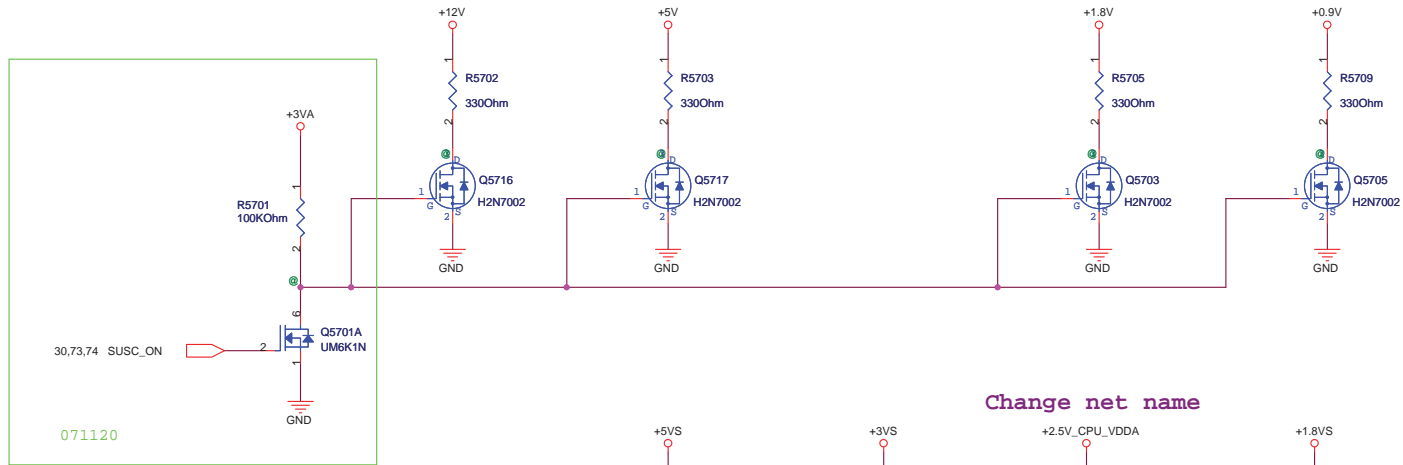


<http://laptop-motherboard-schematic.blogspot.com/>

<Variant Name>		<b>ASUS</b>		<b>Title : USB Port</b>	
ASUSTek Computer INC.		Engineer: N/A			
Size	Project Name			Rev	
A3	1201T			2.0	
Date: Wednesday, October 14, 2009		Sheet 52 of 79			



ASUS		Title : Mini WiFi	
ASUSTek Computer INC.		Engineer: N/A	
Size Custom	Project Name <b>1201T</b>	Rev 2.0	
Date: Wednesday, October 14, 2009		Sheet	53 of 79

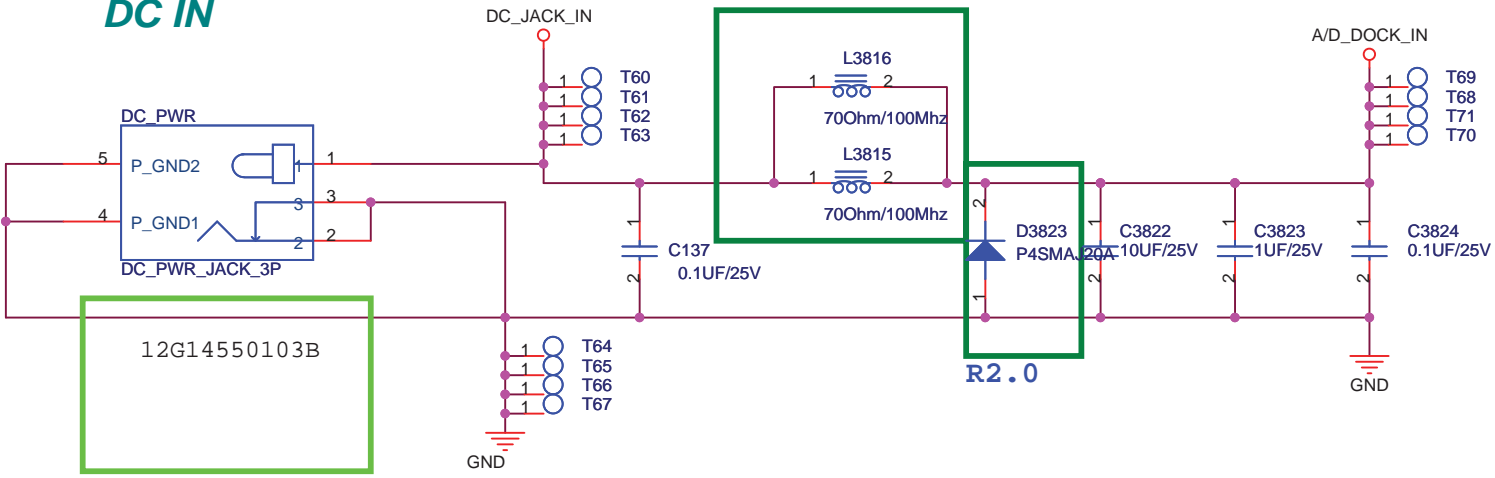


Change net name

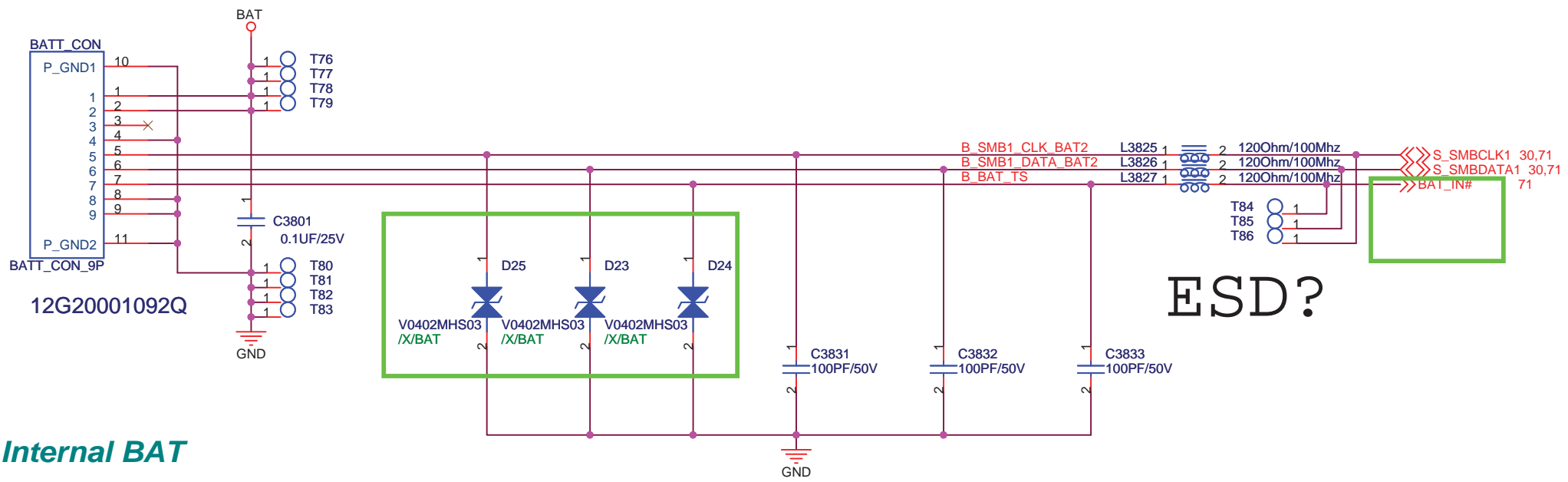
Change all MOS with ESD part



# DC IN



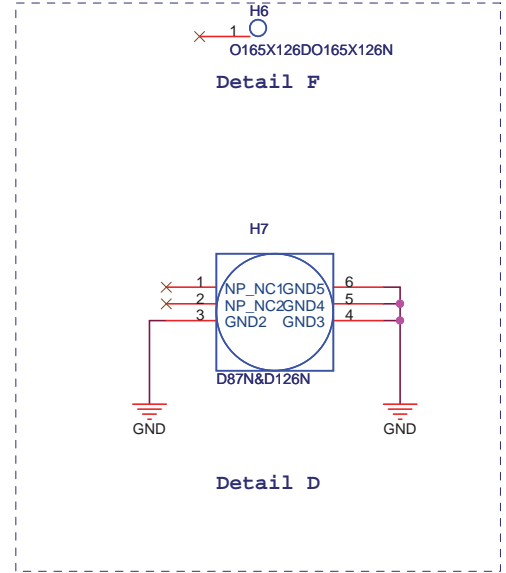
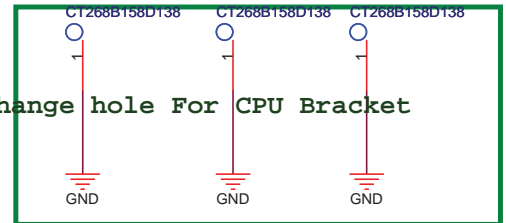
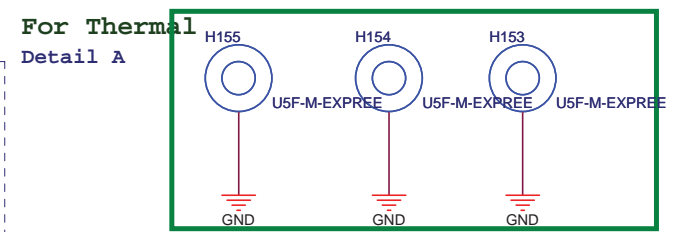
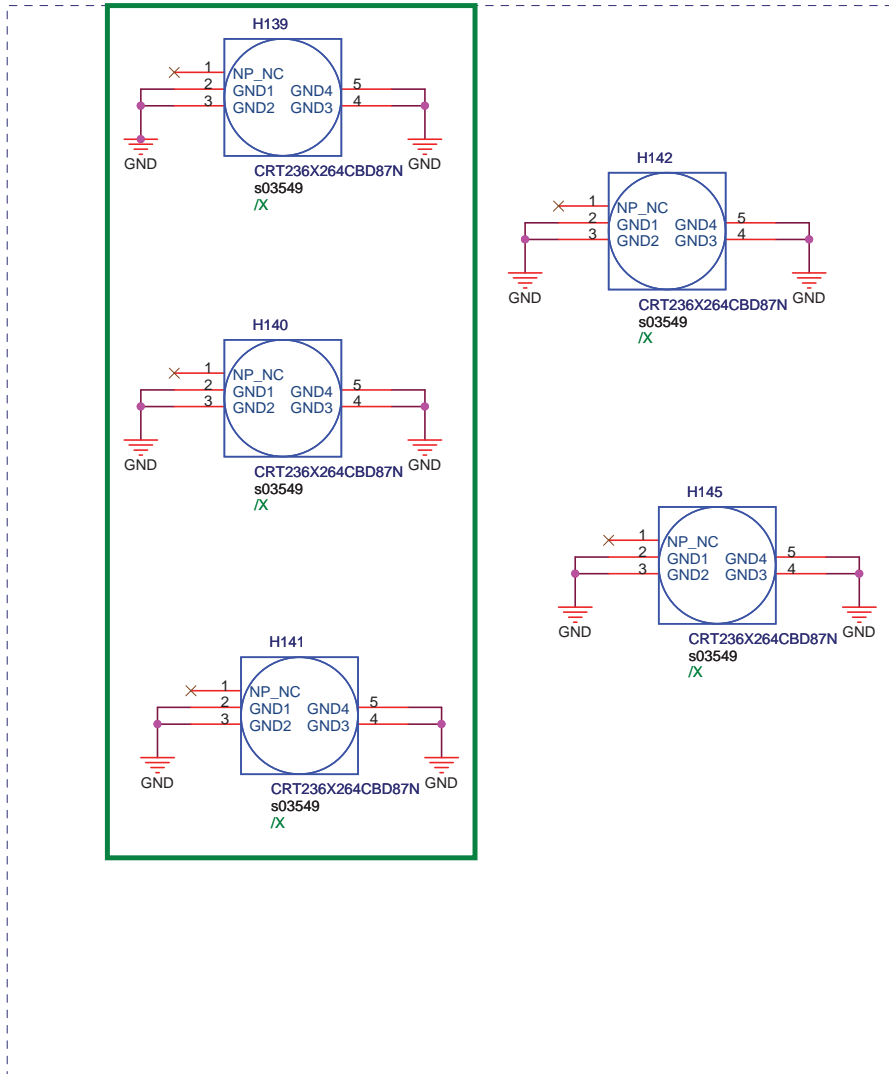
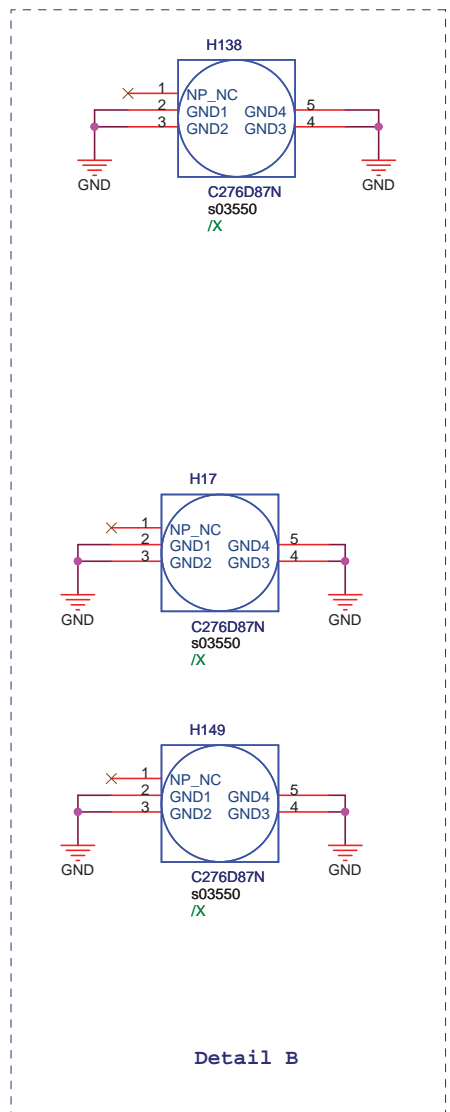
# Internal BAT



<Variant Name>

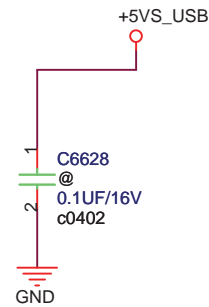
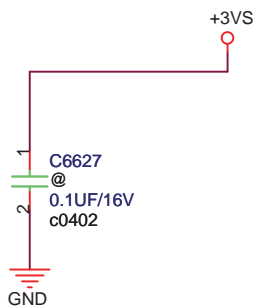
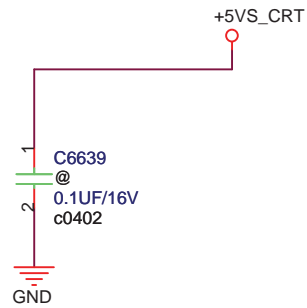
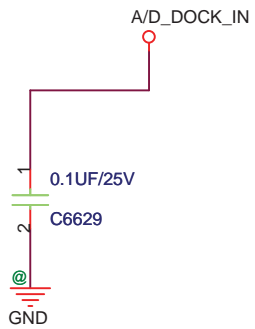
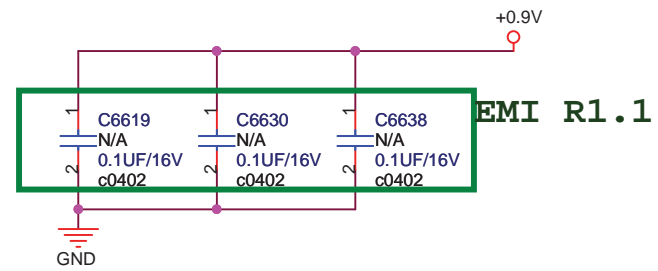
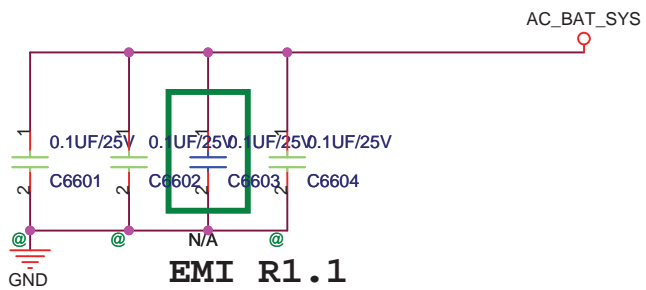
<b>ASUS</b>		<b>Title : PWR Jack</b>	
ASUSTek Computer INC.		Engineer: N/A	
Size	Project Name		Rev
A4	1201T		2.0
Date:	Wednesday, October 14, 2009		Sheet 60 of 79

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<Variant Name>

		<b>Title : Screw Hole</b>	
ASUSTek Computer INC.		Engineer: N/A	
Size Custom	Project Name <b>1201T</b>		Rev 2.0
Date: Wednesday, October 14, 2009		Sheet	65 of 79



<Variant Name>

		<b>Title :</b> EMI	
ASUSTeK COMPUTER INC		<b>Engineer:</b> N/A	
Size	Project Name	Rev	
Custom	1201T	2.0	
Date: November 12, 2019		Sheet	66 of 79

## R1.0

8/14: change DC-in jack to 12G14550103B  
add 1.8VS power for sideport

8/17: Swap DDR address for layout request  
add cap for EMI request

8/18: Swap DDR address for layout request  
P33 del CLK\_25M\_LAN  
P60 change L3815 to other parts, add L3816  
add L1211

8/19: P50 change FAN CON and some related components  
P12 change LVDS BL enable singal LVDS\_BACK\_EN, del L\_G\_BKLT\_CTRL


## R1.1

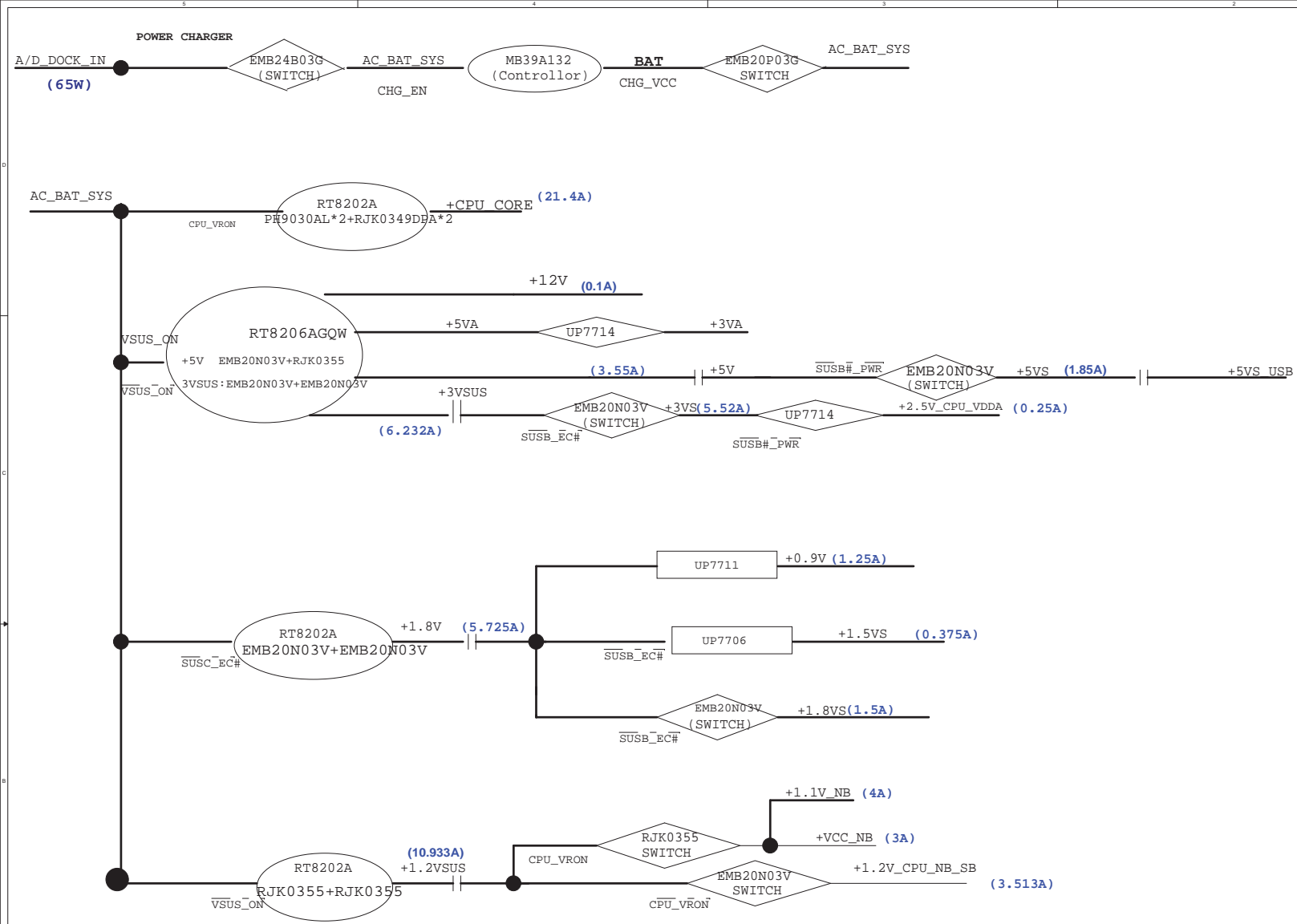
- 1.change 3G\_CON to 3G\_CON1
- 2.H150, H151, H152 no need NUT, and change hole size
- 3.OC15 OC16 change to 22pf
- 4.UF1 fuse change to 07G014150121
- 5.R4612, R4613 change to 120ohm/100Mhz bead for EA test
- 6.R2104 change to 8.87K 10G213887113030 for EA
- 7.mount C2913, C2917 , add C2945, change R2938 to 22ohm;  
change R4534 to 100Ohm, R4533 to 49.9Ohm
- 8.change some parts for EMI request
- 9.VDDHTTX 与CPU\_VLDT分别预留0 ohm到+1.1V\_NB
10. CN3511-CN3516 change to 150pf array CAP
- 11.Unmount SW9, C115
- 12.change R2938 to 10ohm,
- 13.change R167 to 120Ohm/100Mhz bead for noise test
- 14.USB1 change Part Number to 12G13107004E
15. unmount L0301, mount L0302; unmount L1403, mount L1405;

## R2.0

1. DMIC:AC41, AC42 change to 120pf CAP
2. P45 CRT:C4601/C4603/C4605: 24PF/50V  
L4601/L4602/L4603: 75Ohm/100Mhz Bead  
C4602/C4604/C4606: 10PF/50V
3. change D3823 to a TVS diode

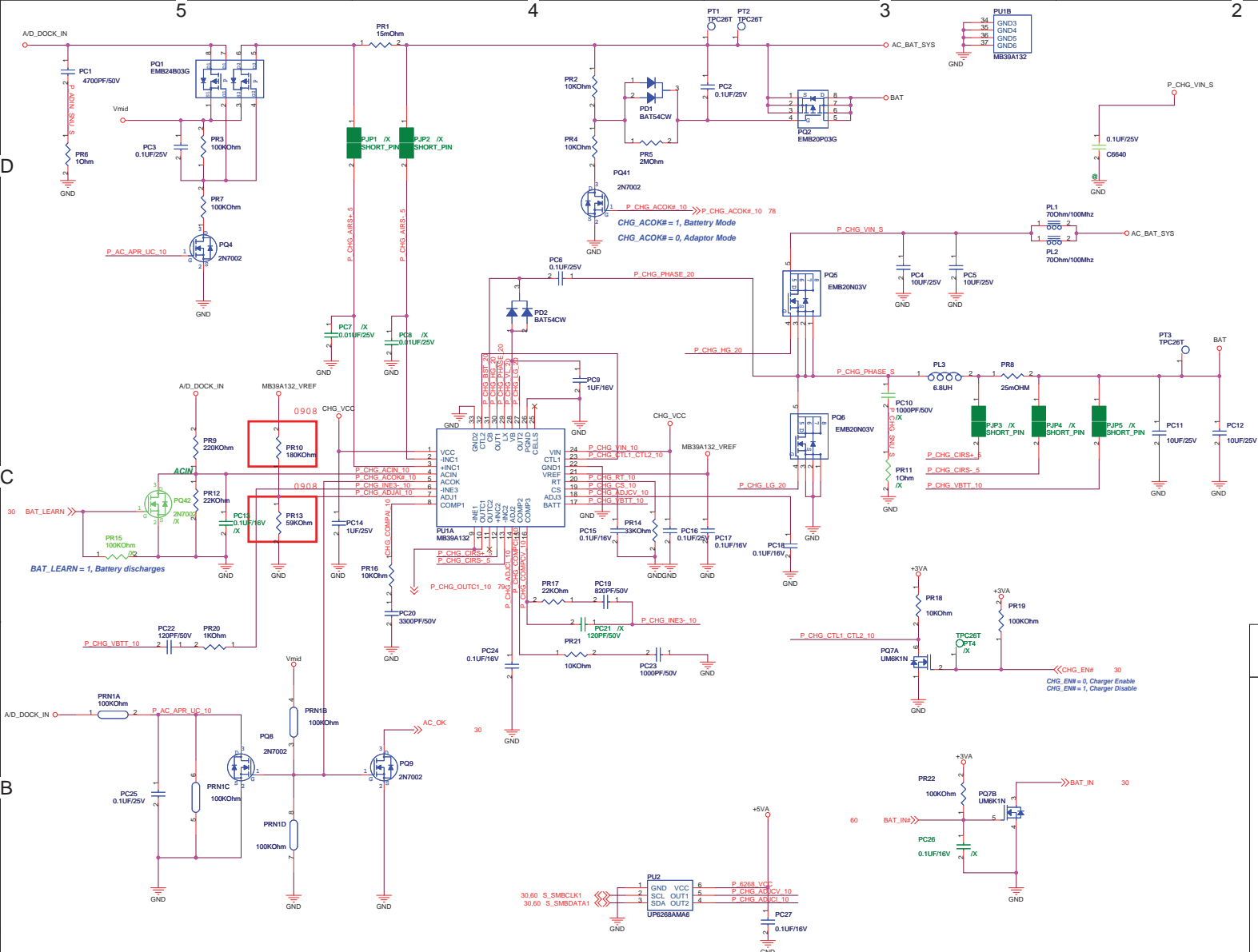
<Variant Name>

		<b>Title : History</b>	
ASUSTek Computer INC.		Engineer: N/A	
Size A	Project Name <b>1201T</b>	Rev 2.0	
Date	Version	Sheet	68 of 79



STD version :1.00g(08/05/09)

ASUS		Title : Power_FLOW	
ASUSTEK COMPUTER INC		Engineer :	
Size	Project Name	Rev	
A2		2.0	
Date: Thursday, October 15, 2009	Sheet	70	of 70

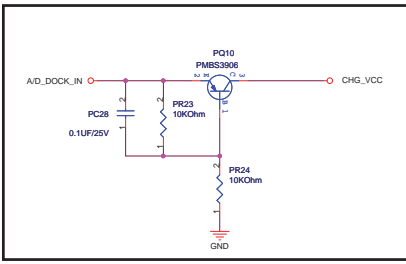


**Power stage**

- I/P Current:**  
 $I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 1.64A$
- Ripple Current:**  
 $I_{ripple} = 0.875A$   
 $I_{spec} = 2A @ 1\text{ pcs}$
- Inductor Spec:**  
 $I_{sat} = 8A$   
 $I_{dc} = 4.5A$   
 $DCR = 60\text{mohm}$
- MOSFET Spec:**  
**H-side MOSFET: EMB20N03V**  
 $R_{ds(ON)} = 23\text{ mohm}$  ( $V_{gs} = 5V$ )  
 $I_{cont} = 6A$  ( $T = 25^\circ C$ )  
 $I_{peak} = 32A$   
**L-side MOSFET: EMB20N03V**  
 $R_{ds(ON)} = 23\text{ mohm}$  ( $V_{gs} = 5V$ )  
 $I_{cont} = 6A$  ( $T = 25^\circ C$ )  
 $I_{peak} = 32A$

**Controller**

- Voltage & Current:**  
 $+12.6V @ 2.5A$
- Frequency:**  
 $PR14 = 33KOHM$ ,  
 $F_{osc} = 17000 / RT(Kohm) = 515KHz$
- OCP:**
- POR:**  
 $POR\ Hysteresis = 0.1V$   
 $V_{on} = 7.5V$
- Enable Voltage:**  
 $V = 2.9V$
- Soft start time:**  
 $T_{ss} = 23ms$
- Phase selection:**  
 $N/A$
- Inrush Current:**  
 $C_{total} = 20\mu F$   
 $I_{inrush} = 0.01A$



**Battery Charging Current:**  
 $I_{chg} = (V_{adj} - 0.075) / (25 \cdot R_s)$

**Input Adaptor Max. Current Limit:**  
 $I_{limit\_current} = (V_{adj} - 1 - 0.075) / (25 \cdot R_s) = 1.90A$

**ACIN Threshold = 1.25V**

Adaptor > 13.75V, System Powered by Adaptor

Adaptor < 13.75V, System Powered by Battery

**Battery Charging Voltage:**

$V_{adj3} : VREF \implies V_{bat} = 4.2V / cell$   
 $3.9V > V_{adj3} > 2.4V \implies V_{bat} = 4.35V / cell$   
 $V_{adj3} : GND \implies V_{bat} = 4.0V / cell$   
 $2.2V > V_{adj3} > 1.1V \implies V_{bat} = 2 \cdot V_{adj3} / cell$

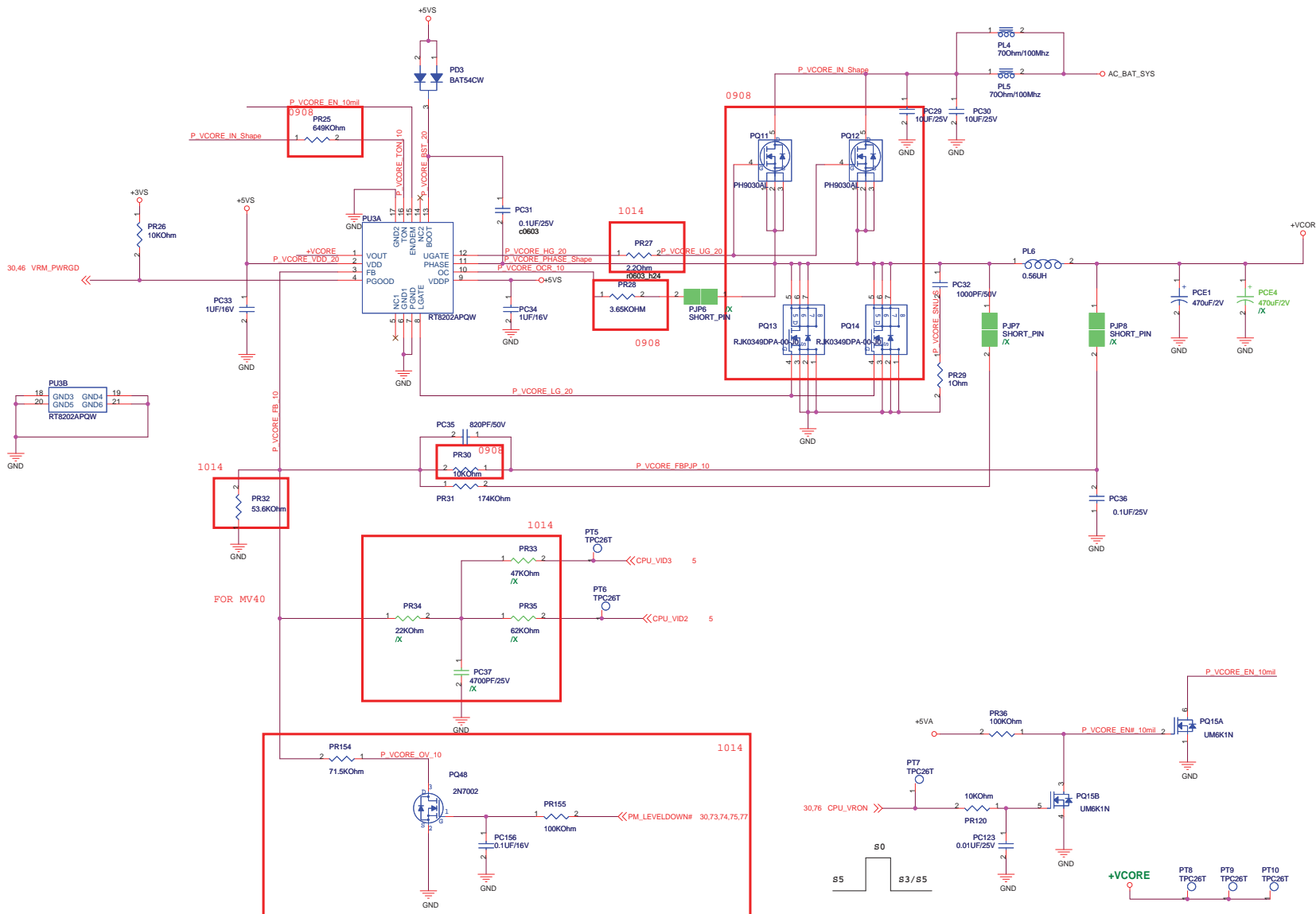
**Battery Cell Selection:**

CELLS: VREF  $\implies 4\text{ Cells}$ ;  
 CELLS: OPEN  $\implies 3\text{ Cells}$ ;  
 CELLS: GND  $\implies 2\text{ Cells}$ ;

**VREF = 5.0V**

$f_{osc}(KHz) = 17000 / RT(KOhm)$

Soft start:  $t_s(s) = 0.23 \cdot C \cdot CS(\mu F)$



- Controller**
- Voltage & Current:**  
VCORE: 18A
  - Frequency:**  
Ton=3.85p\*Rt(on)\*Vout/Vin-05=0.3us  
Frequency=Vout/(Vin\*Ton)=500KHZ
  - OCp:**  
SetPR28=6.34K  
Iocp=Rocpp\*20/Rds(on)=20\*6.34/3.8=31.6A
  - Soft start time:**  
Soft-Start duration is 1.35ms
  - Inrush Current:**  
C total =470UF  
I inrush=0.35A

- Power stage**
- IP Current:**  
I in = Vo\*Io/(0.8 \* Vin) =2.5A
  - Ripple Current:**  
Iripple=5.66A
  - Dynamic:**  
Ipeak=18A  
ESR=9mohm  
V=162mV
  - Inductor Spec:**  
Isat=40A  
Idc=25A  
DCR=1.6mohm
  - MOSFET Spec:**  
L-side MOSFET: RJK0353DPA-00-J0  
Rds(on)max=7.6mOhm (Vgs=4.5V)  
Icont=35A (T=25)  
Ipeak=140A (Pause<10us)  
H-side MOSFET: RJK0355DPA-00-J0  
WPAK  
Rds(ON)= 11.8 mohm (Vgs=4.5 V)  
I cont = 30 A (T =25 )  
I peak = 120 A (Pause <10 us)

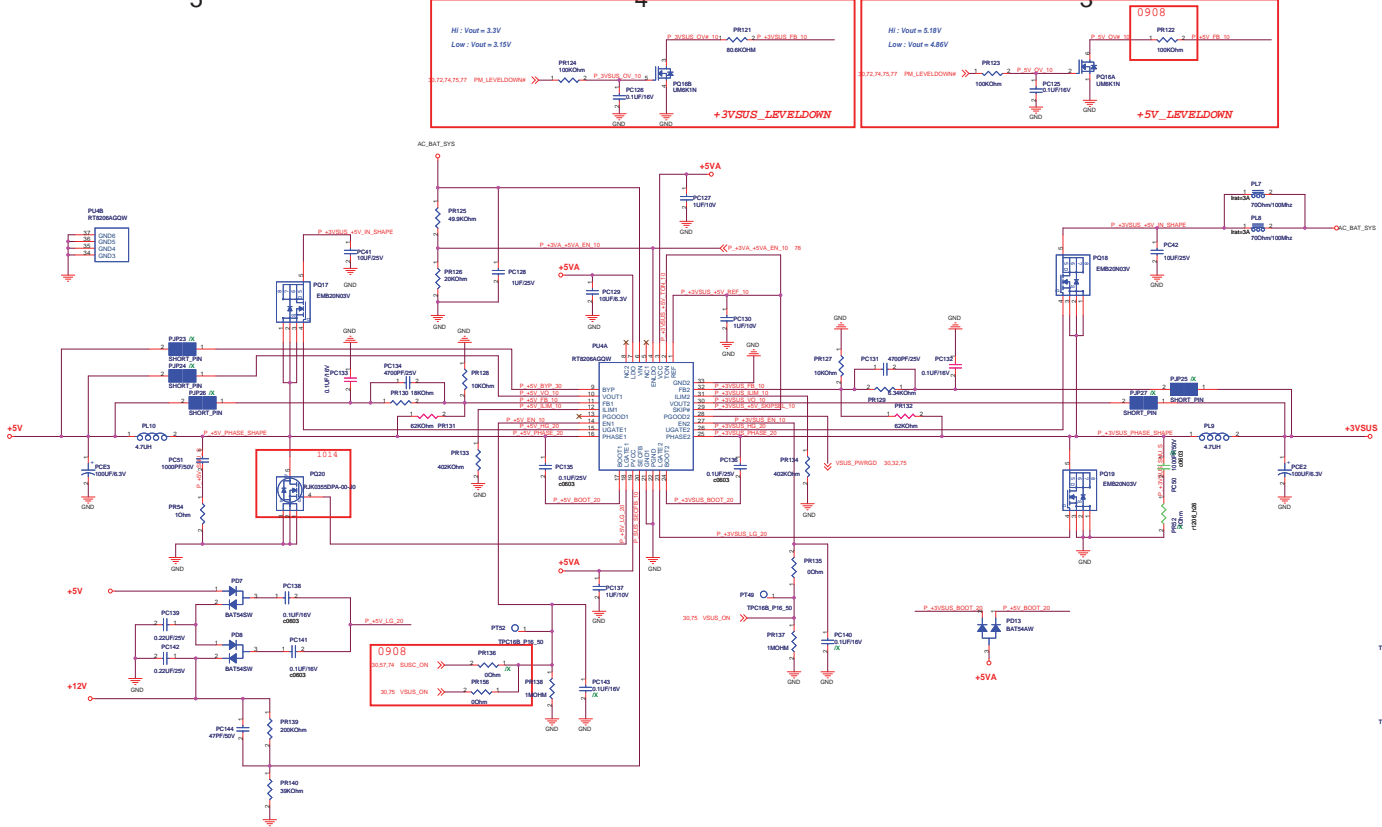
FOR MV40

PM_LEVELDOWN#	VID3	VID2	Voltage
0	0	0	/
0	0	1	0.90V
0	1	0	/
0	1	1	/
1	0	0	/
1	0	1	1.00V
1	1	0	/
1	1	1	/

FOR L335

PM_LEVELDOWN#	VID3	VID2	Voltage
0	0	0	1.10V
0	0	1	0.95V
0	1	0	0.90V
0	1	1	0.75V
1	0	0	1.14V
1	0	1	1.00V
1	1	0	0.94V
1	1	1	0.80V

<http://laptop-motherboard-schematic.blogspot.com/>



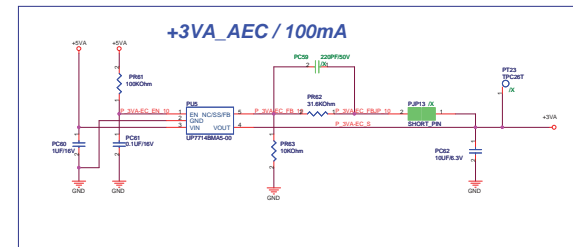
Power stage	+3VSUS
1. I/P Current:	$I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 1.832A$
2. Ripple Current:	$I_{rip} = 1.92A$ $I_{spec} = 2.5A$ $Q1$ pcs
3. Dynamic:	$I_{peak} = 4A$ $ESR / 1 \text{ pcs} = 18 \text{ mohm}$ $V = 72mV$
4. Inductor Spec:	$I_{sat} = 10 A$ $I_{dc} = 5.5 A$ $DCR = 37 \text{ mohm}$
5. MOSFET Spec:	H-side MOSFET: EMB20N03V $R_{ds(ON)} = 23 \text{ mohm}$ ( $V_{gs} = 4.5 V$ ) $I_{cont} = 8 A$ ( $T = 25$ ) $I_{peak} = 32A$ (Pause $\geq 10$ us)
	L-side MOSFET: EMB20N03V $R_{ds(ON)} = 23 \text{ mohm}$ ( $V_{gs} = 4.5 V$ ) $I_{cont} = 8 A$ ( $T = 25$ ) $I_{peak} = 32 A$ (Pause $\geq 10$ us)

Power stage	+5VSUS
1. I/P Current:	$I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 2.082A$
2. Ripple Current:	$I_{rip} = 1.482A$ $I_{spec} = 2.5A$ $Q1$ pcs
3. Dynamic:	$I_{peak} = 3A$ $ESR / 1 \text{ pcs} = 18 \text{ mohm}$ $V = 54mV$
4. Inductor Spec:	$I_{sat} = 10 A$ $I_{dc} = 5.5 A$ $DCR = 37 \text{ mohm}$
5. MOSFET Spec:	H-side MOSFET: SI7326DN_T1_E3 $R_{ds(ON)} = 23 \text{ mohm}$ ( $V_{gs} = 4.5 V$ ) $I_{cont} = 8 A$ ( $T = 25$ ) $I_{peak} = 32 A$ (Pause $\geq 10$ us)
	L-side MOSFET: RJK0355DPA-00-J0 WPAK $R_{ds(ON)} = 11.8 \text{ mohm}$ ( $V_{gs} = 4.5 V$ ) $I_{cont} = 30 A$ ( $T = 25$ ) $I_{peak} = 120 A$ (Pause $\geq 10$ us)

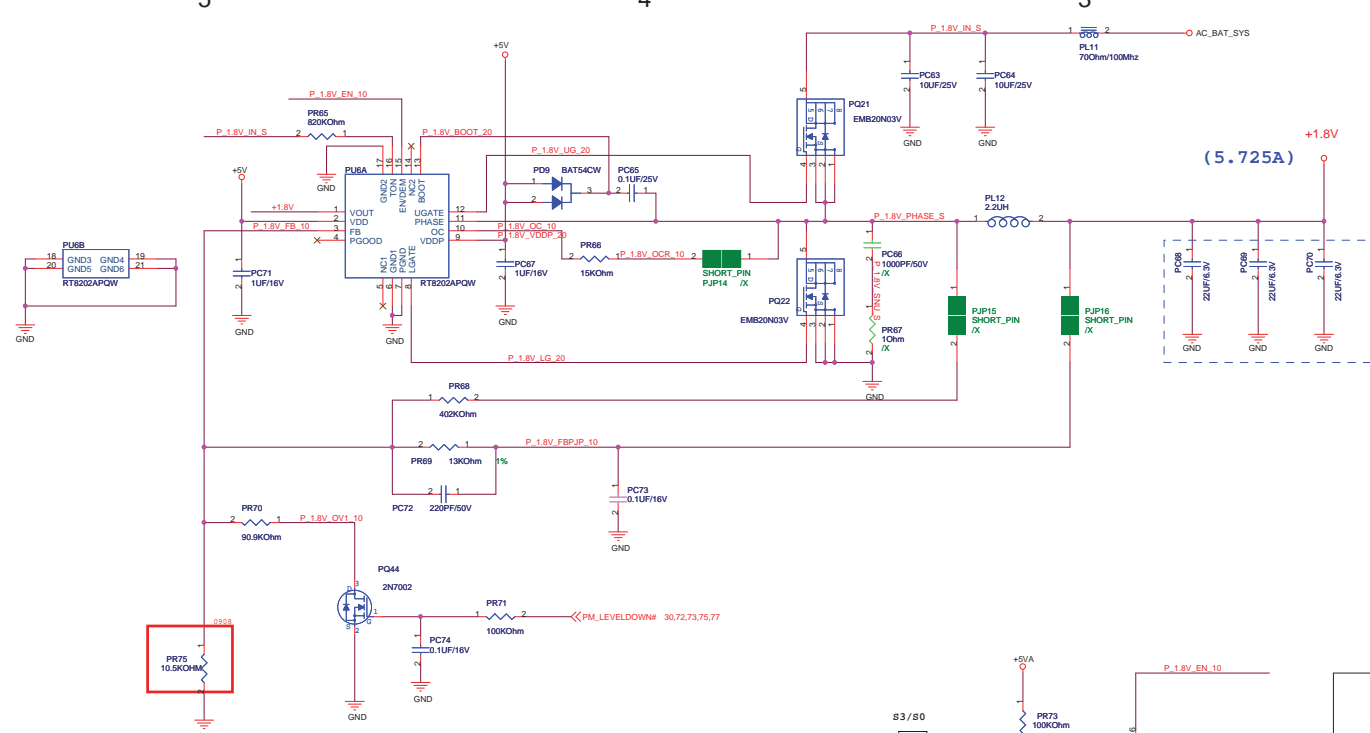
Controller	+3VSUS
1. Voltage & Current:	+3VSUS=3.3V@4A
2. Frequency:	fosc=375KHz
3. OCP:	Set PR134=402Kohm fosc=0.74A
4. POR:	V on = 4.35-4.5 V V off = 3.9-4.25 V
5. UVP:	V uvp= 70% Vout
6. OVP:	V ovp=115%Vout
7. Enable Voltage:	V rising = 1V V falling = 0.4
8. Soft start time:	Tss=2ms
9. Phase selection:	/X
10. Inrush Current:	C total = 110 uF I inrush= 0.165 A

Controller	+5VSUS
1. Voltage & Current:	+5VSUS=5V@3A
2. Frequency:	fosc=300KHz
3. OCP:	Set PR133=402Kohm fosc=17A
4. POR:	V on = 4.35-4.5 V V off = 3.9-4.25 V
5. UVP:	V uvp= 70% Vout
6. OVP:	V ovp=115%Vout
7. Enable Voltage:	V rising = 1V V falling = 0.4
8. Soft start time:	Tss=2ms
9. Phase selection:	/X
10. Inrush Current:	C total = 110 uF I inrush= 0.275 A

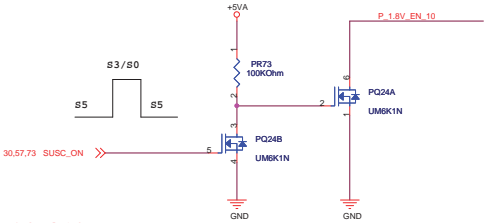
1. Dropout Voltage: 5. EN Voltage:	$V = 210mV$ ( $I_o = 300mA$ )	$V_{rising} = 2 V$ $V_{falling} = 0.8$
2. Current Limit:	$I_{limit} = 480mA$	$V_{cc} = 3.3V$
3. Continue Current:	$I_{cont} = 100mA$	
4. Pd:	$R_{thjc} = 5 C/W$ $Pd = 0.4W$	$T_{ss} = 400us$ $C_{total} = 10 uF$ $I_{inrush} = 62.5 mA$







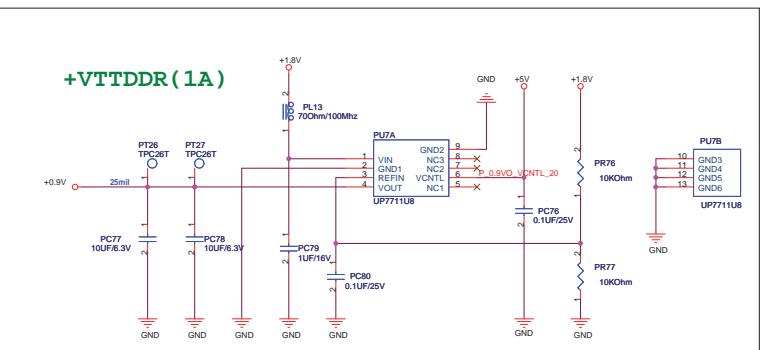
- Power stage**
- I/P Current:**  
 $I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 1.43A$
  - Ripple Current:**  
 $I_{rip} = 2.29A$   
 $I_{spec} = 2.5A @ 2pcs$
  - Dynamic:**  
 $I_{peak} = 5.725A$   
 $ESR / 1 pcs = 18 mohm$   
 $V = 103mV$
  - Inductor Spec:**  
 $I_{sat} = 14 A$   
 $I_{dc} = 8 A$   
 $DCR = 18 mohm$
  - MOSFET Spec:**  
**H-side MOSFET: EMB20N03V**  
 $R_{ds(ON)} = 23 mohm$  ( $V_{gs} = 5 V$ )  
 $I_{cont} = 6 A$  ( $T = 25$ )  
 $I_{peak} = 32 A$   
**L-side MOSFET: EMB20N03V**  
 $R_{ds(ON)} = 23 mohm$  ( $V_{gs} = 5 V$ )  
 $I_{cont} = 6 A$  ( $T = 25$ )  
 $I_{peak} = 32 A$

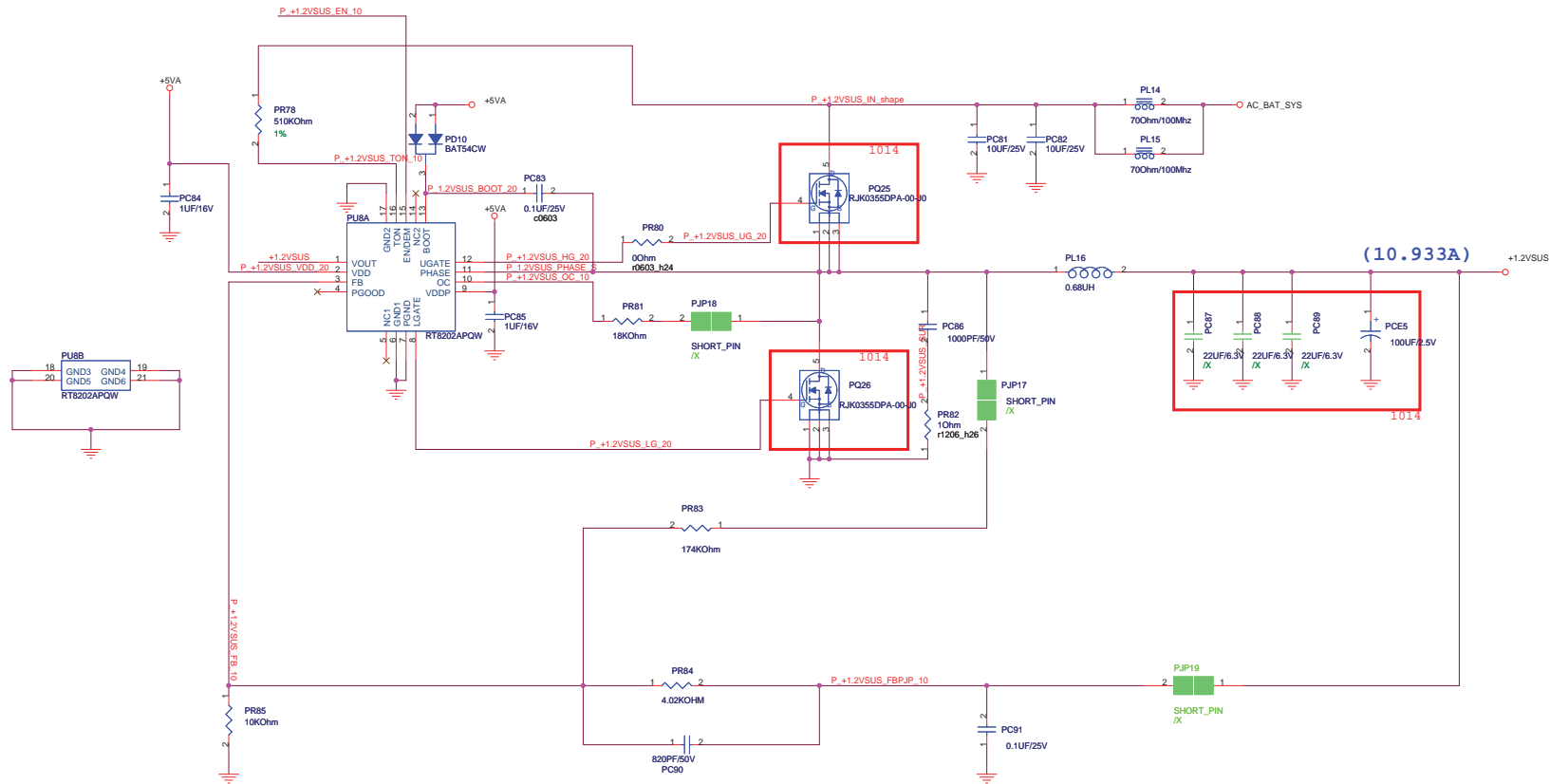


- 0.9V@1.25**
- Dropout Voltage:**  
 $V = 0.3V$  ( $I_o = 2 A$ )
  - Current Limit:**  
 $I_{limit} = 4 A$
  - Continue Current:**  
 $I_{cont} = 3 A$
  - Power Dissipation:**  
 $R_{thjc} = 52 /W$   
 $P_d = 1.9 W$
  - EN Voltage:**  
 $V_{en} = 1.4V$   
 $V_{sd} = 0.8 V$
  - Supply Voltage:**  
 $V_{cc} = 5 V$
  - Inrush current:**  
 $T_{ss} = 5 ms$   
 $C_{total} = 10 uF$   
 $I_{inrush} = 3 mA$

PM_LEVELDOWN#	Voltage	Status
L	1.70V	Power Saving
H	1.8V	Normal

- Controller**
- Voltage & Current:**  
**+1.8V@5.725A**
  - Frequency:**  
 $PR65 = 820K ohm$   
 $F_{osc} = 300KHz$
  - OCp:**  
 $PR66 = 15K ohm \rightarrow 13A$
  - POR:**  
 $V_{ccrth} = 3.7 \sim 4.1V$   
 $V_{ccchs} = 0.2V$
  - UVP:**  
 $V_{out} * 70\%$
  - OVP:**  
 $V_{out} * 115\%$
  - Enable Voltage:**  
 $V = 2.9V$
  - Soft start time:**  
 $T_{ss} = 1.2 ms$
  - Phase selection:**  
/X
  - Inrush Current:**  
 $C_{total} = 100 uF$   
 $I_{inrush} = 0.15 A$



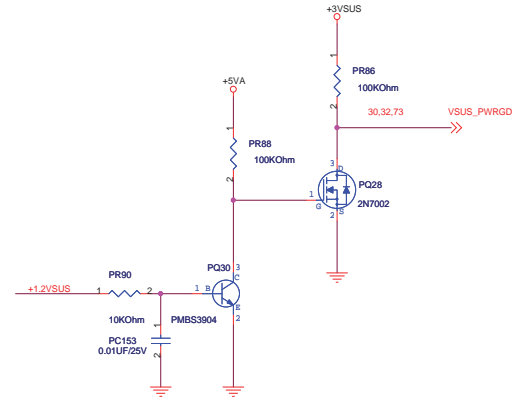
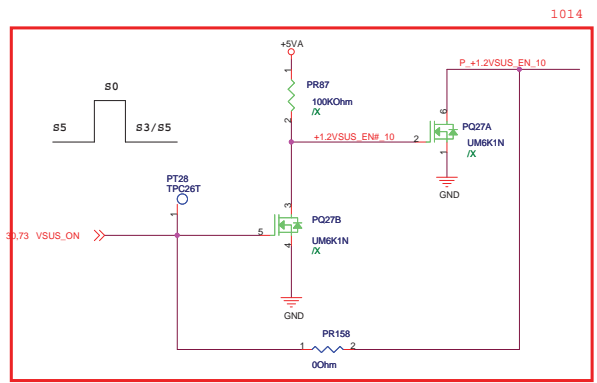
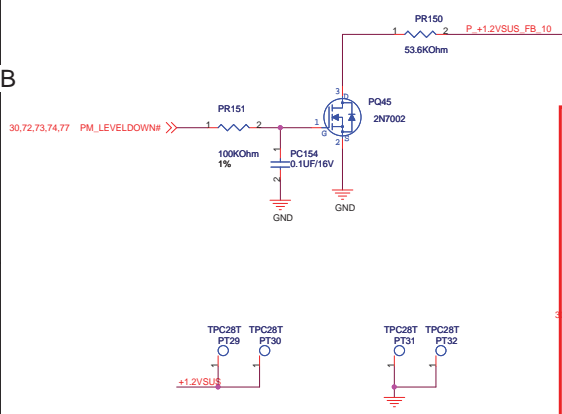


**Power stage**

- I/P Current:**  
 $I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 1.822A$
- Ripple Current:**  
 $I_{ripple} = 3.73A$
- Ripple Voltage:**  
 $I_{peak} = 10.933$   
 $ESR = 18m\Omega$   
 $V = 197mV$
- Inductor Spec:**  
 $I_{sat} = 25A$   
 $I_{dc} = 15.5A$   
 $DCR = 5.5m\Omega$
- MOSFET Spec:**  
**H-side and L-side MOSFET:**  
 $R_{ds(on)} = 16.5m\Omega$  ( $V_{gs} = 4.5V$ )  
 $I_{cont} = 30A$  ( $T = 25$ )  
 $I_{peak} = 120A$  (Pause < 10us)

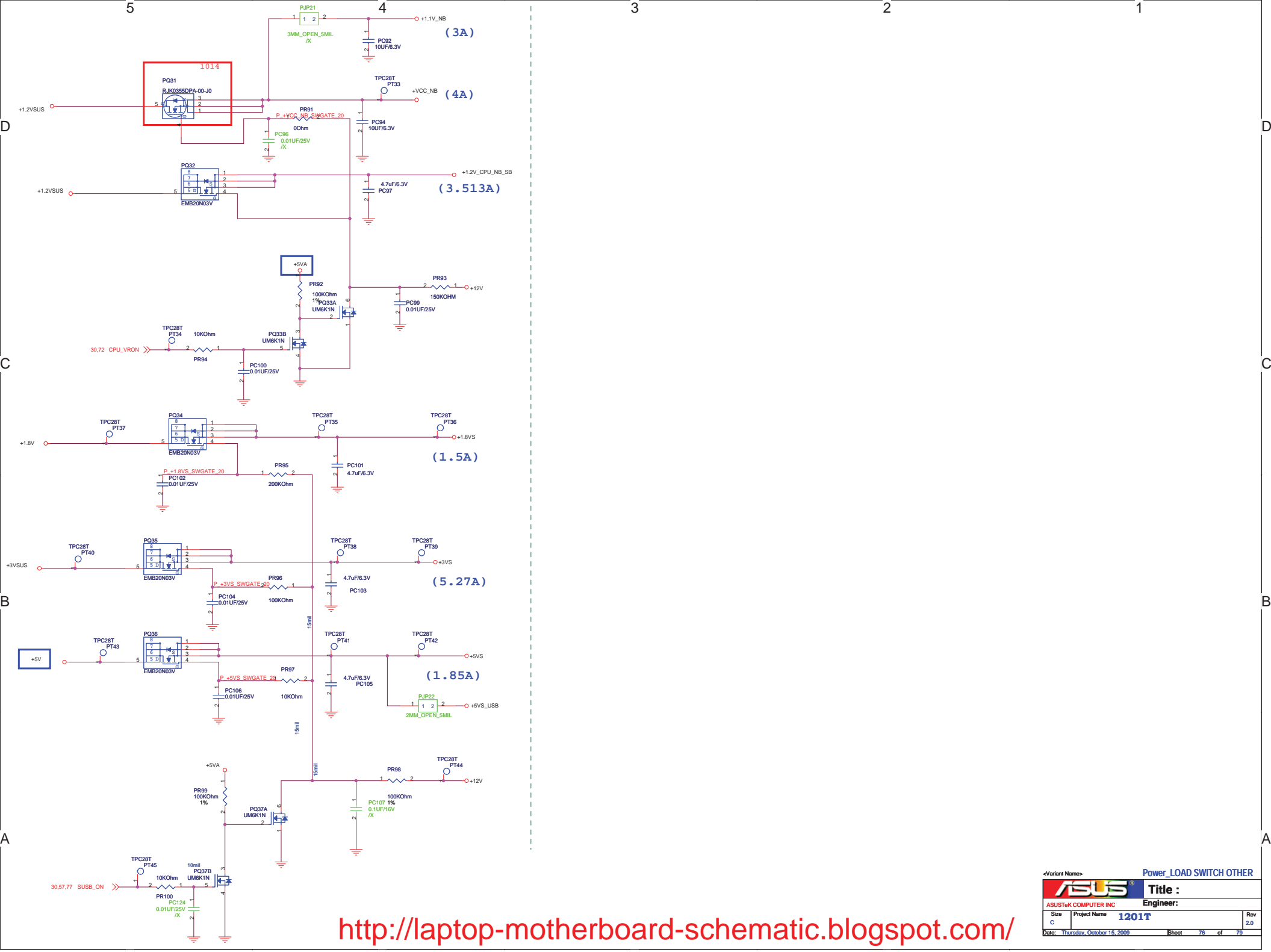
**Controller**

- Voltage & Current:**  
**+1.2VSUS: 1.2V & 10.933A**
- Frequency:**  
**Frequency = 500KHZ**
- OCP:**  
 $R_{set} = PR81 = 18K\Omega$   
 $I_{ocp} = R_{ocp} \cdot 20 / R_{ds(on)} = 21.9A$
- Soft start time:**  
**Soft-Star duration is 1.35ms**
- Inrush Current:**  
 $C_{total} = 66\mu F$   
 $I_{inrush} = 0.088A$



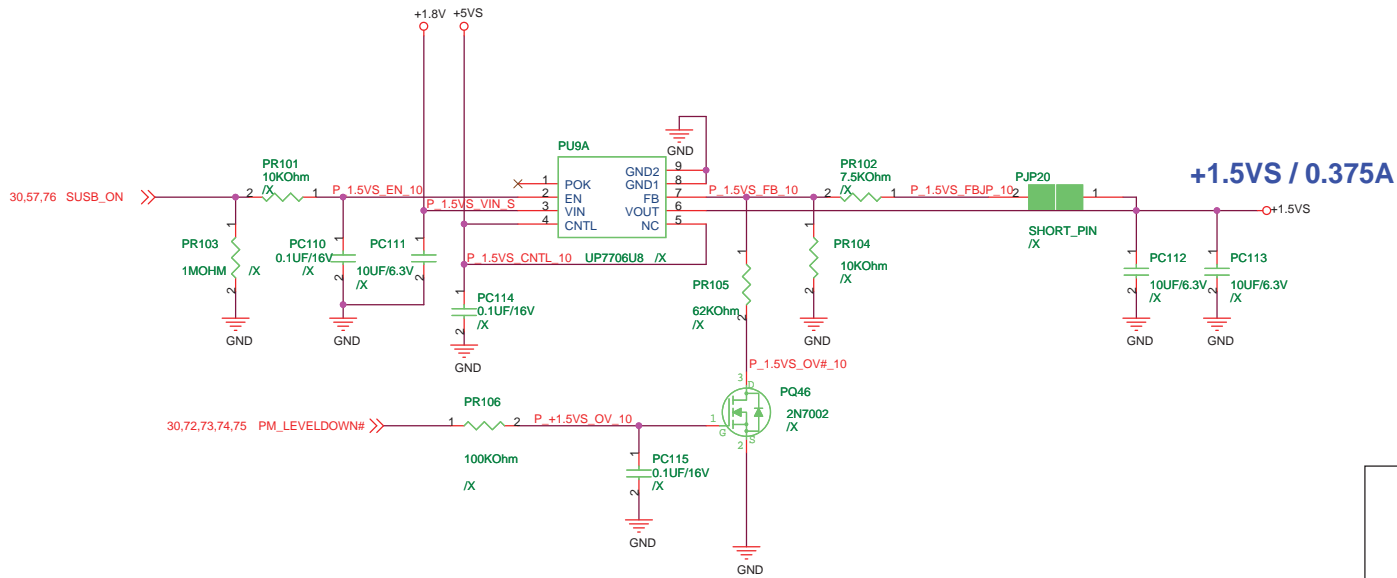
PM_LEVELDOWN#	Voltage	Status
L	1.15V	Power Saving
H	1.2V	Normal

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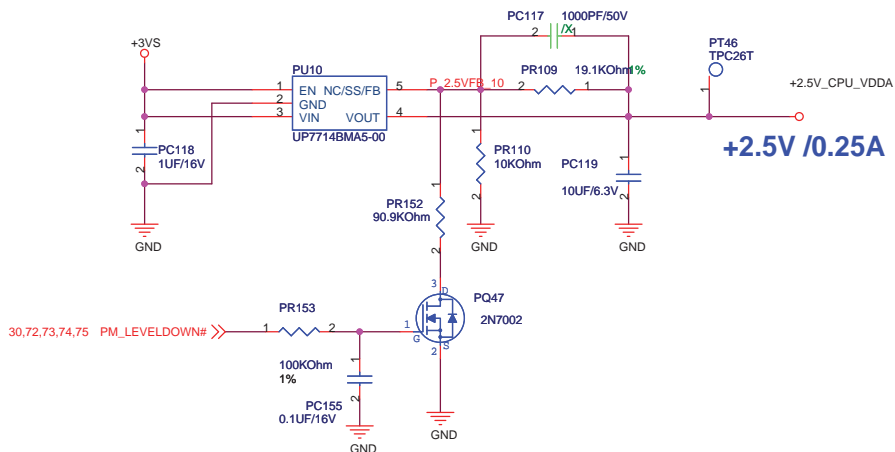
ASUS		Title :	
ASUSTeK COMPUTER INC		Engineer :	
Size	Project Name	Rev	
C	1201T	2.0	
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**+1.5V / 0.375A**

PM_LEVELDOWN#	Voltage	Status
L	1.4V	Power Saving
H	1.5V	Normal

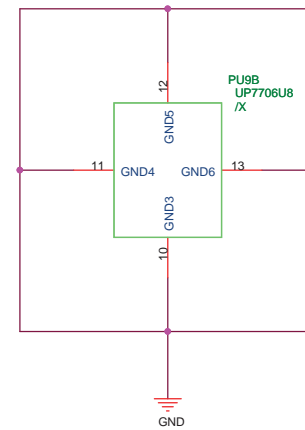
PM_LEVELDOWN#	Voltage	Status
L	2.35V	Power Saving
H	2.5V	Normal



**+2.5V / 0.25A**

**2.5V @ 0.25A**

1. Dropout Voltage:  
V = 0.21V (Io = 0.3A)
2. Current Limit:  
I limit = 320mA
3. Continue Current:  
I cont = 300mA
4. Power Dissipation:  
Rthjc = 250 /W  
Pd = 0.4W
5. EN Voltage:  
V rising = 2V  
V falling = 0.8V
6. Supply Voltage:  
Vcc = 3V
7. Inrush current:  
Tss = 400us  
C total = 10uF  
I inrush = 0.063A



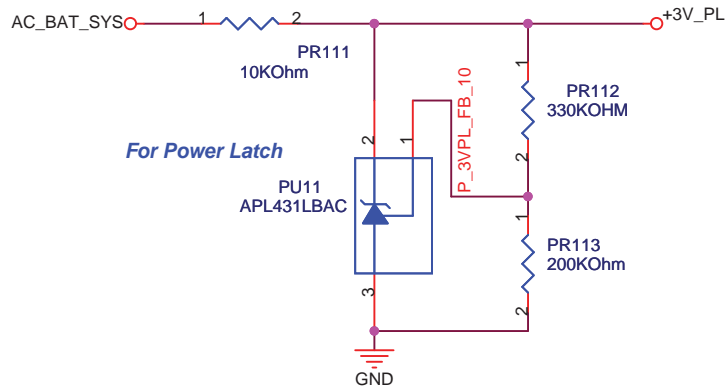
1. Dropout Voltage:  
V = 300 mV (Io=2 A)
2. Current Limit:  
I limit= 2.8 A
3. Continue Current:  
I cont= 1A
4. Pd:  
R thjc =5 C/W  
Pd =1.9W
5. EN Voltage:  
V rising = 1.4 V  
V falling = 0.4 V
6. Supply Voltage:  
Vcc=5V
7. Inrush current:  
Tss = 4 ms  
C total = 20 uF  
I inrush= 7.5mA

<Variant Names>

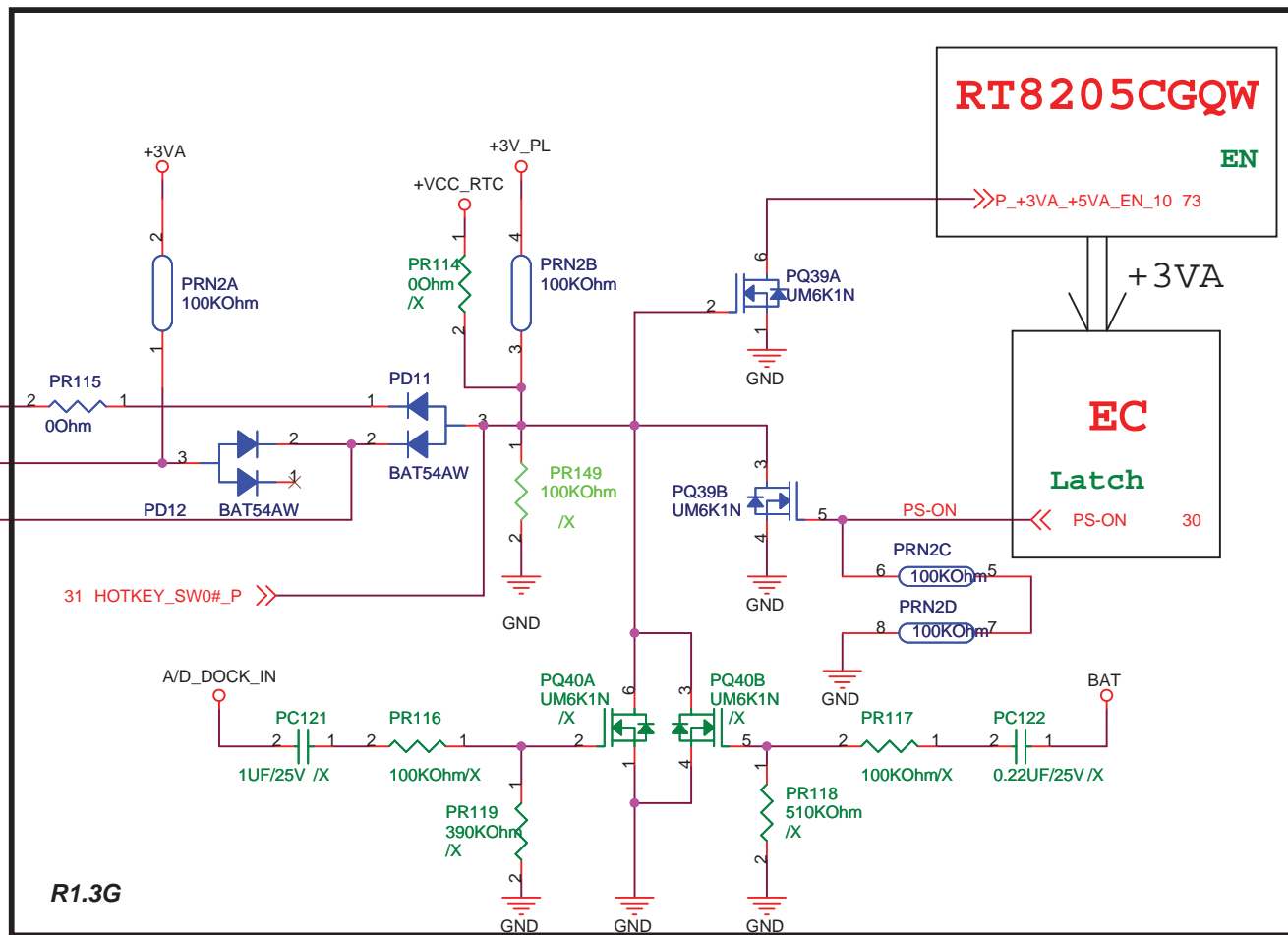
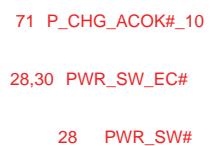
<b>ASUS</b>		<b>Title : +1.5VS &amp; +2.5VS</b>	
ASUSTek Computer INC		Engineer: N/A	
Size A3	Project Name <b>1201T</b>	Rev 2.0	
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# +3V\_PL

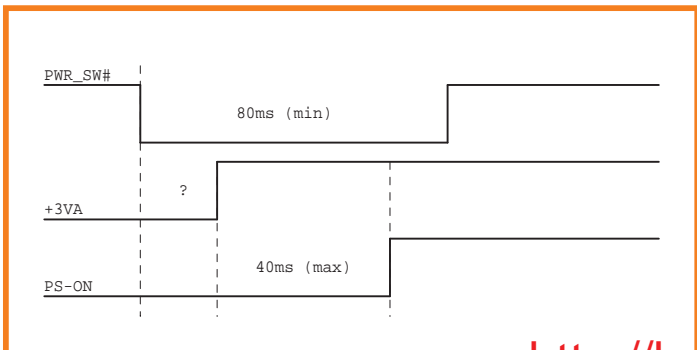
20mil



For Power Latch



R1.3G



<Variant Name>

<b>ASUS</b>		<b>Title : Power Latch</b>	
ASUSTek Computer INC.		Engineer: N/A	
Size A4	Project Name <b>1201T</b>	Rev 2.0	
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