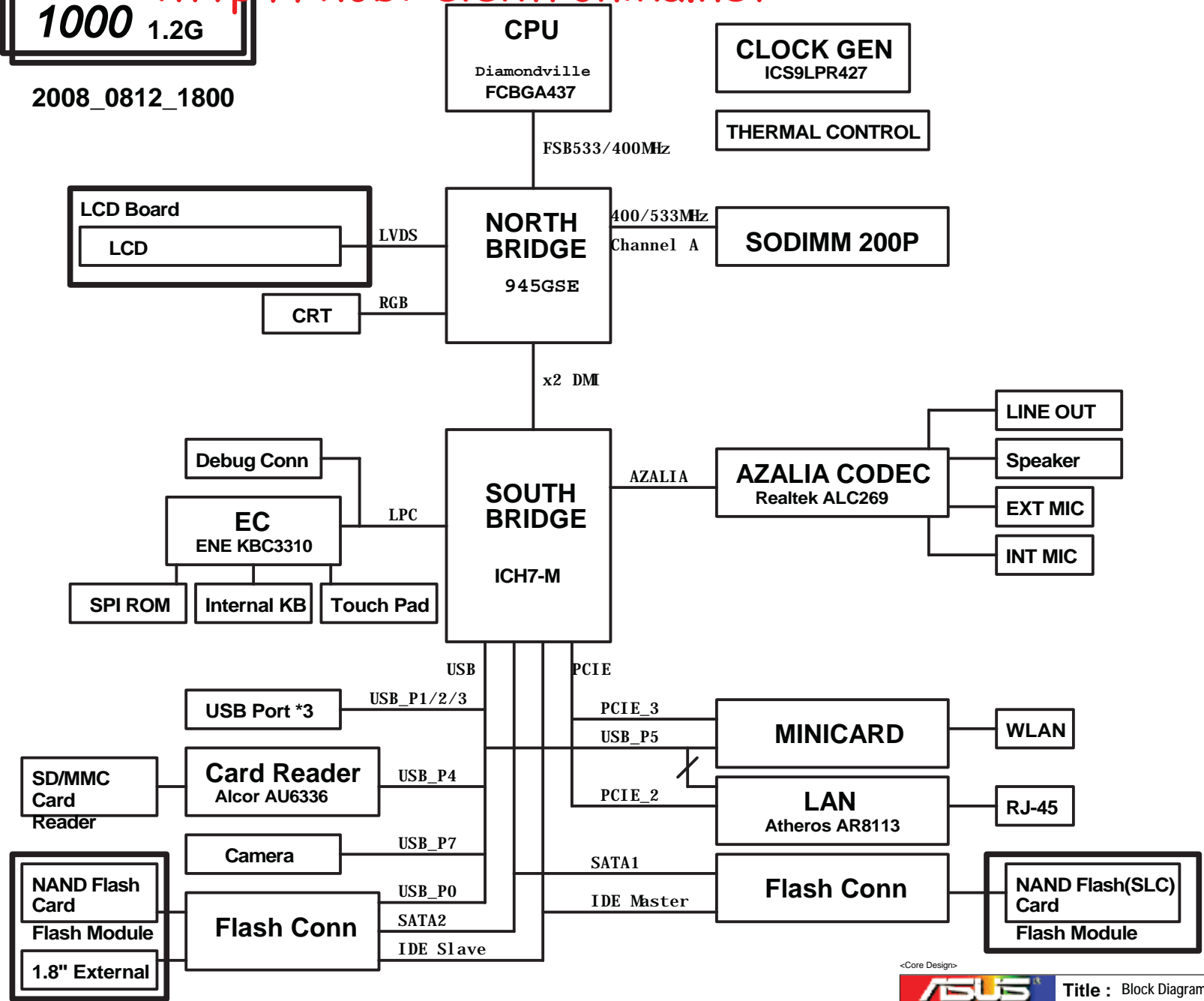


**1000 1.2G**

2008\_0812\_1800

- 01\_Block Diagram
- 02\_System Setting
- 03\_Power Sequence
- 04\_Clock Gen\_ICS9LPR426
- 05\_Diamondville\_BUS
- 06\_Diamondville\_PWR
- 07\_NB-945GMS(HOST)
- 08\_NB-945GMS(DMI)
- 09\_NB-945GMS(GRAPHIC)
- 10\_NB-945GMS(DDR2)
- 11\_NB-945GMS(PWR)
- 12\_NB-945GMS(PWR2)
- 13\_NB-945GMS(GND)
- 14\_SB-ICH7M(PWR)
- 15\_SB-ICH7M(1)
- 16\_SB-ICH7M(2)
- 17\_SB-ICH7M(3)
- 18\_DDR2 SODIMM
- 19\_DDR2 Termination
- 20\_Onboard VGA
- 21\_LCD Conn\_LID
- 22\_PCIE 3.5G & Ext. Antenna
- 23\_Mini WiFi+ BT
- 24\_LAN\_Atheros AR8113
- 25\_MDC\_RJ11\_RJ45
- 26\_HD + Flash Conn
- 27\_USB Port
- 28\_Camera Conn
- 29\_Card Reader\_AU6336C52
- 30\_Codec\_ALC269
- 31\_Audio\_AMP\_Jack
- 32\_EC\_ENE KB3310
- 33\_EC\_UART controller
- 34\_Switch\_SPI ROM\_Debug Conn
- 35\_Thermal Sensor\_FAN
- 36\_KB\_Touch Pad
- 37\_LED\_THERMTRIP
- 38\_Discharge
- 39\_PWR Jack
- 40\_Srew Hole
- 41\_EMI
- 42\_POWER FLOW
- 43\_Vcore
- 44\_Power System
- 45\_Power\_+1.8V & VTTDDR
- 46\_Power\_VCCP
- 47\_Power\_+1.5VS & +2.5VS
- 48\_Power\_Charger
- 49\_EC Pin Define
- History



### EEE PC 701 PCB version

GPI37	GPI38	GPI39	PCB version
0	0	0	
0	0	0	
0	0	1	
0	0	1	
0	1	0	
0	1	0	
0	1	1	
0	1	1	
1	0	0	
1	0	0	
1	0	1	
1	0	1	
1	1	0	
1	1	0	
1	1	1	
1	1	1	

### USB

USB 0	Flash Conn
USB 1	USB Conn
USB 2	USB Conn
USB 3	USB Conn
USB 4	Card Reader
USB 5	Minicard
USB 6	NC
USB 7	Camera

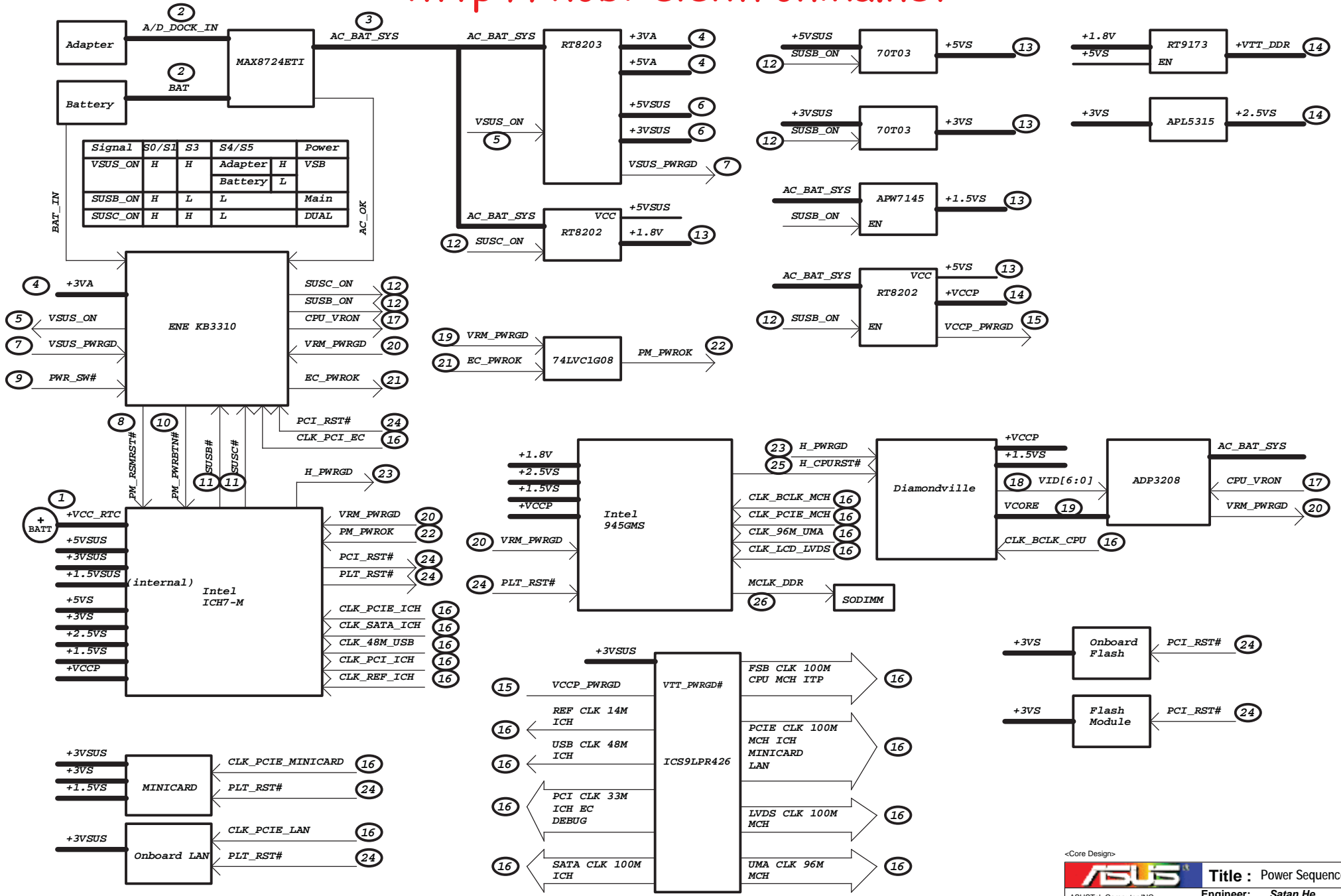
### PCIE

PCIE 1	NC
PCIE 2	LAN
PCIE 3	Minicard
PCIE 4	NC

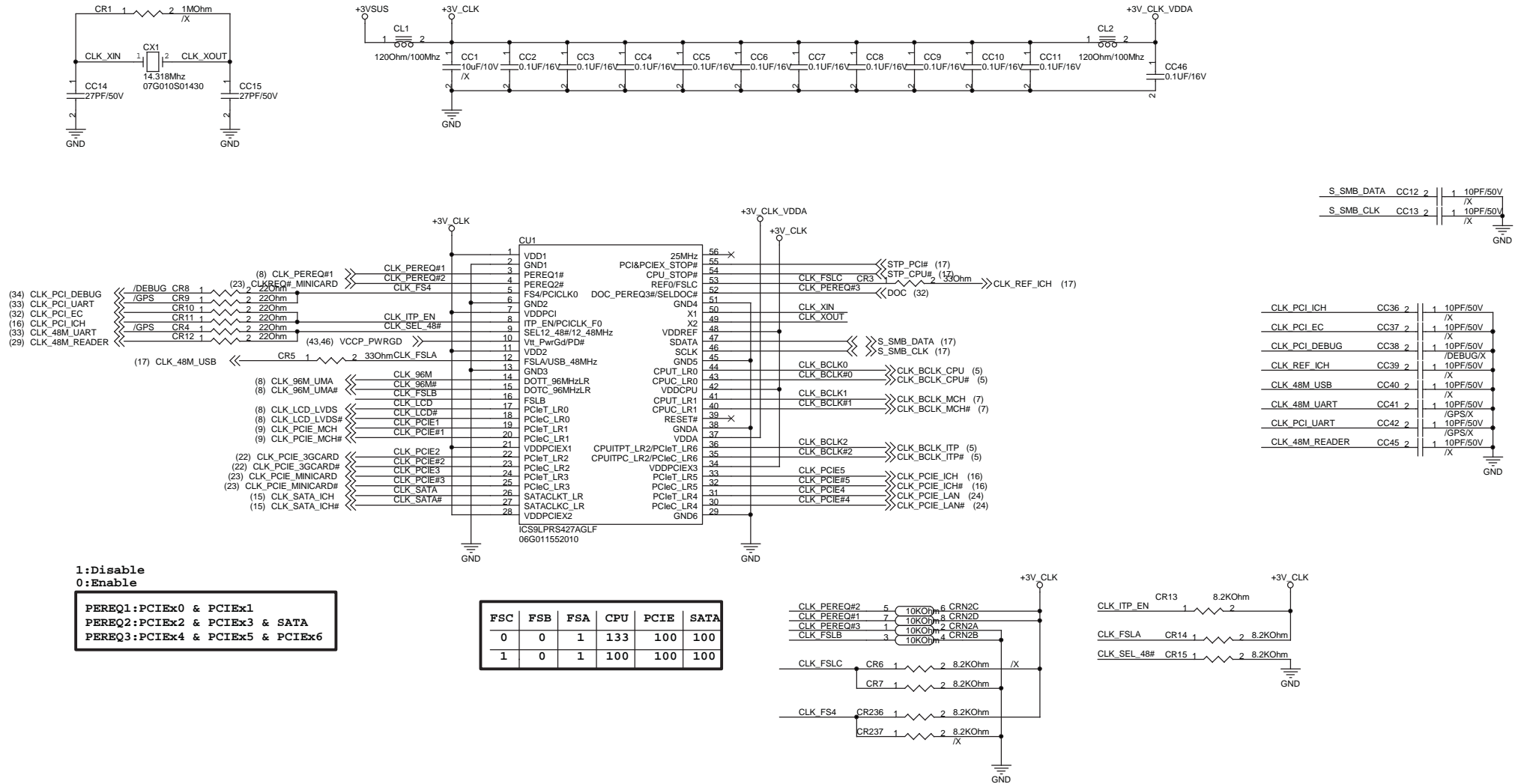
### Azalia

ACZ_SDIN0	CODEC
ACZ_SDIN1	MODEM
ACZ_SDIN2	NC

<Core Design>



Signal	S0/S1	S3	S4/S5	Power
VSUS_ON	H	H	Adapter	VSUS
			Battery	L
SUSB_ON	H	L	L	Main
SUSC_ON	H	H	L	DUAL

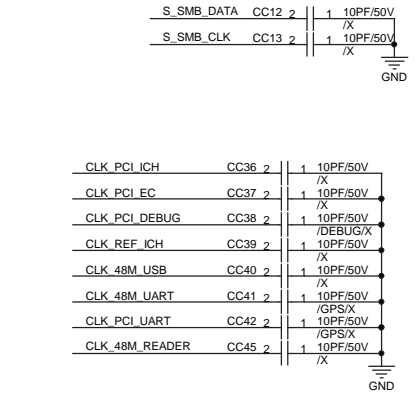


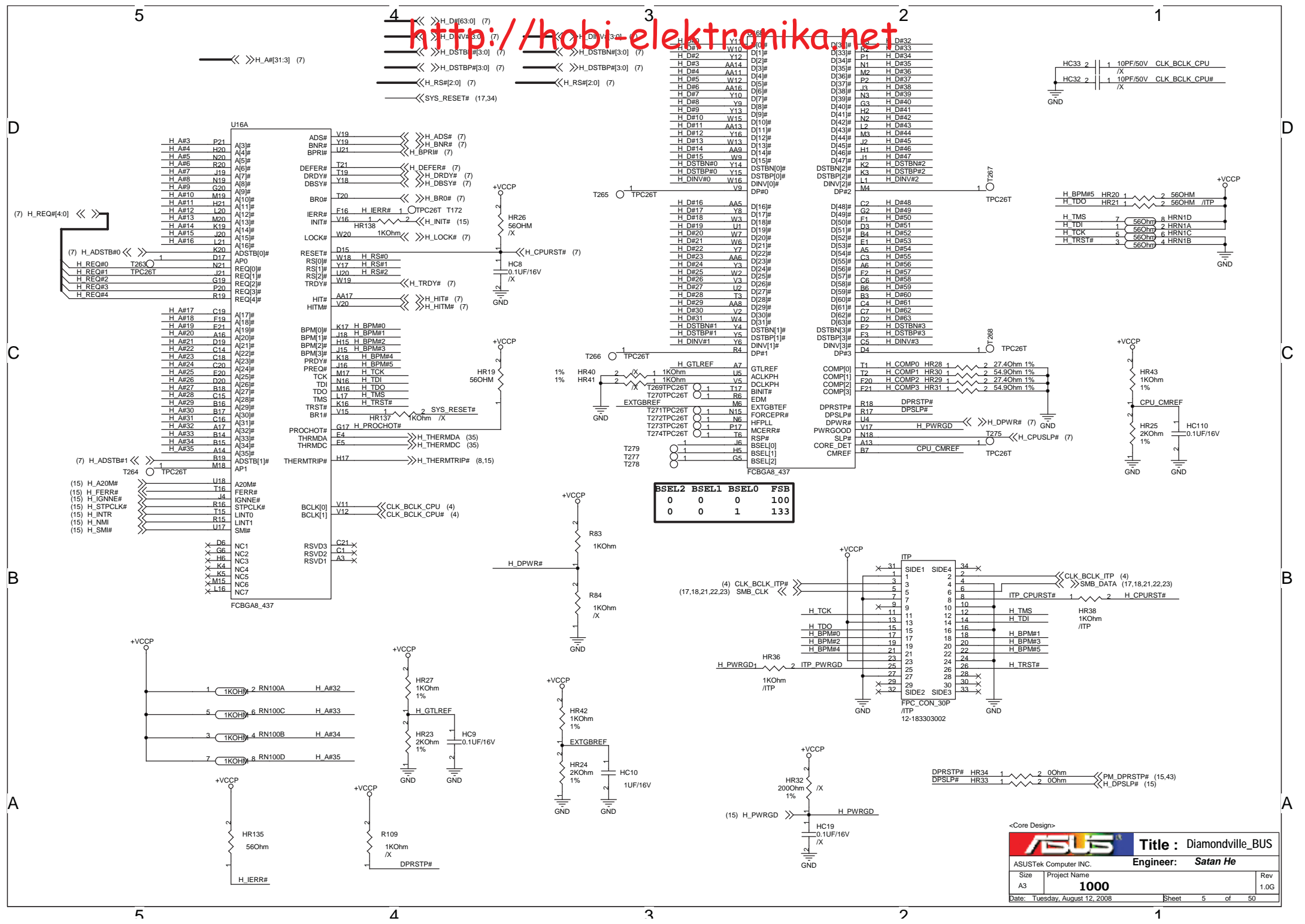
- (34) CLK\_PCL\_DEBUG
- (33) CLK\_PCL\_UART
- (32) CLK\_PCL\_EC
- (16) CLK\_PCL\_ICH
- (33) CLK\_48M\_UART
- (29) CLK\_48M\_READER

1:Disable  
0:Enable

PEREQ1:PCIEx0 & PCIEx1  
 PEREQ2:PCIEx2 & PCIEx3 & SATA  
 PEREQ3:PCIEx4 & PCIEx5 & PCIEx6

FSC	FSB	FSA	CPU	PCIE	SATA
0	0	1	133	100	100
1	0	1	100	100	100





BSEL2	BSEL1	BSEL0	FSB
0	0	0	100
0	0	1	133

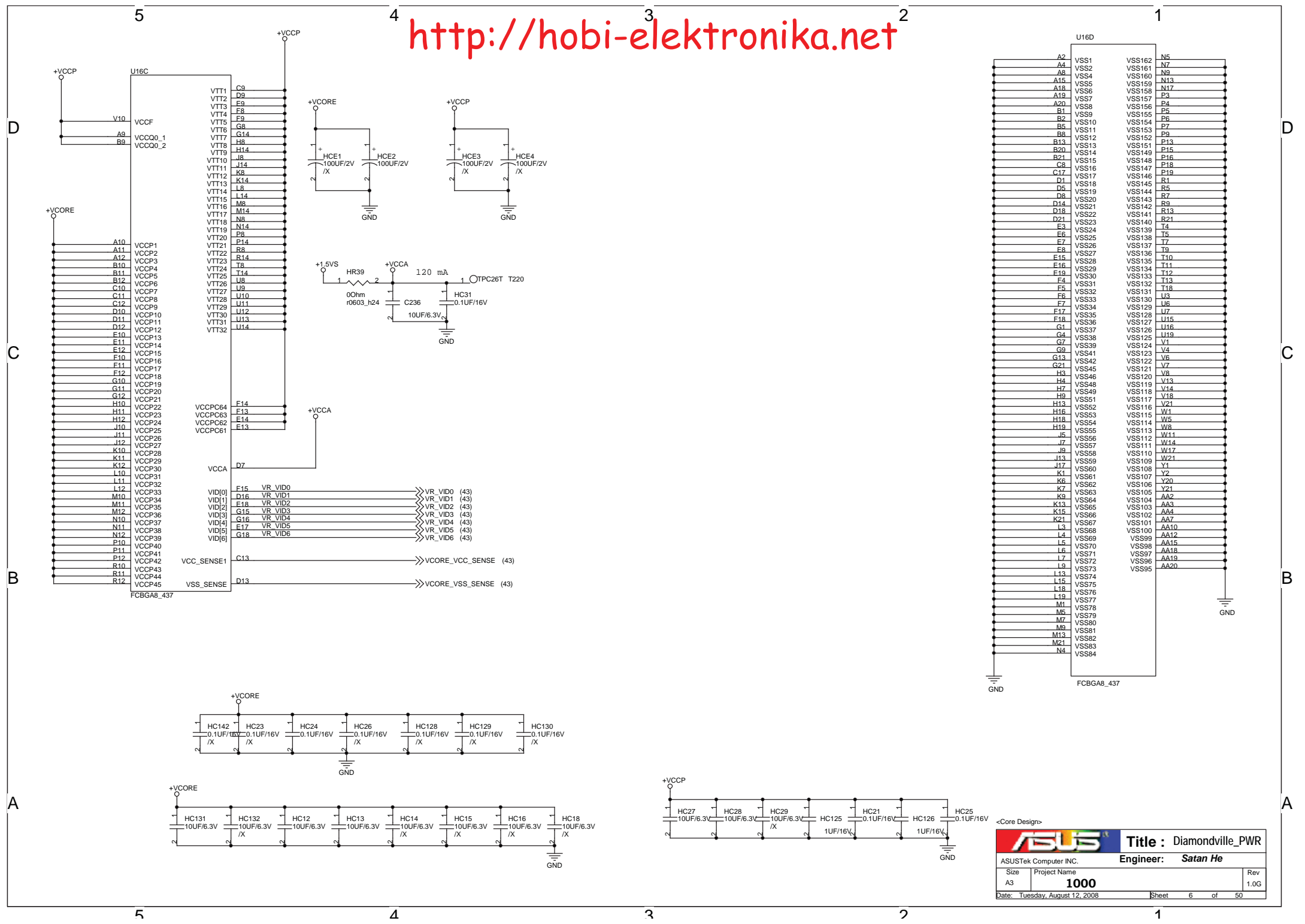
<Core Design>

**ASUS** Title : Diamondville\_BUS

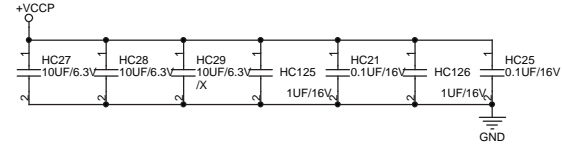
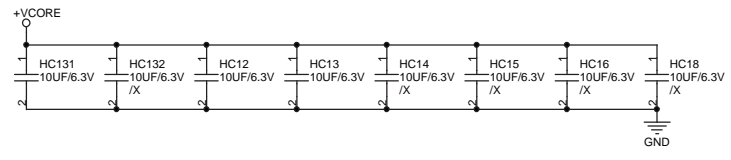
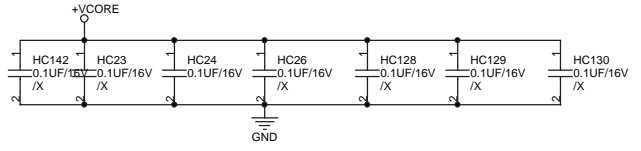
ASUSTek Computer INC. Engineer: **Satan He**

Size	Project Name	Rev
A3	1000	1.0G

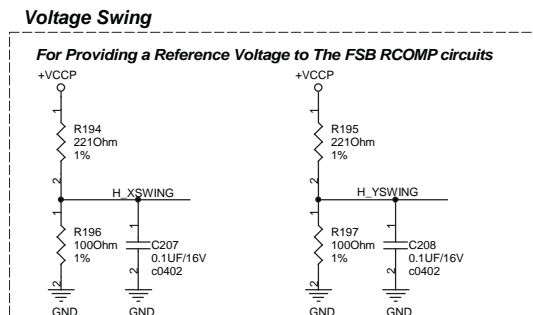
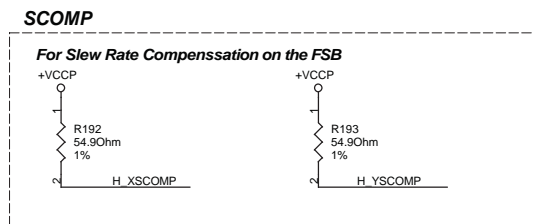
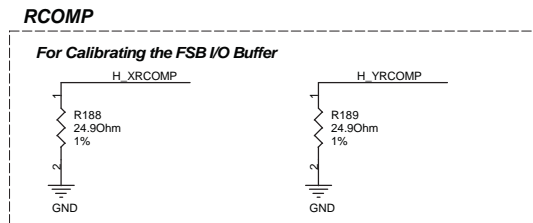
Date: Tuesday, August 12, 2008 Sheet 5 of 50



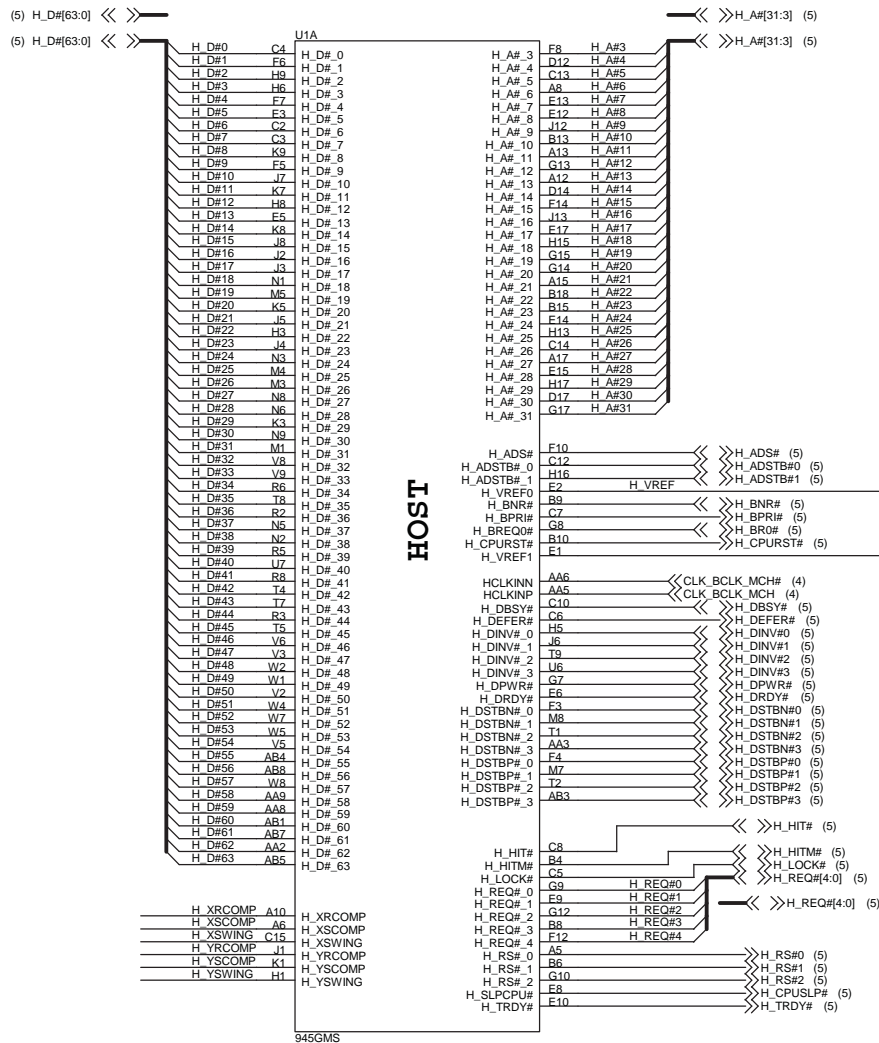
U16D		
A2	VSS1	N5
A4	VSS2	N7
A6	VSS4	N9
A15	VSS5	N13
A18	VSS6	N17
A19	VSS7	P3
A20	VSS8	P4
B1	VSS9	P6
B2	VSS10	P7
B5	VSS11	P9
B8	VSS12	P13
B13	VSS13	P14
B20	VSS14	P15
B21	VSS15	P16
C8	VSS16	P18
C17	VSS17	P19
D1	VSS18	R1
D8	VSS19	R5
D8	VSS20	R9
D14	VSS21	R13
D18	VSS22	R21
D21	VSS23	R21
E3	VSS24	T4
E6	VSS25	T7
E7	VSS26	T9
E8	VSS27	T10
F15	VSS28	T11
F19	VSS29	T12
F4	VSS30	T13
F5	VSS31	T18
F6	VSS32	U3
F7	VSS33	U6
F17	VSS34	U7
F18	VSS35	U15
G1	VSS36	U16
G4	VSS37	U19
G7	VSS38	V1
G9	VSS39	V4
G13	VSS41	V6
G21	VSS42	V7
H3	VSS43	V8
H4	VSS44	V13
H7	VSS45	V14
H9	VSS46	V18
H13	VSS47	V21
H16	VSS48	W1
H18	VSS49	W5
H19	VSS50	W8
J5	VSS51	W11
J7	VSS52	W14
J9	VSS53	W17
J13	VSS54	W21
J17	VSS55	Y1
K1	VSS56	Y2
K6	VSS57	Y20
K7	VSS58	Y21
K9	VSS59	AA2
K13	VSS60	AA3
K15	VSS61	AA4
K21	VSS62	AA7
L4	VSS63	AA10
L5	VSS64	AA12
L6	VSS65	AA15
L7	VSS66	AA18
L9	VSS67	AA19
L13	VSS68	AA20
L15	VSS69	
L18	VSS70	
L19	VSS71	
M1	VSS72	
M5	VSS73	
M7	VSS74	
M9	VSS75	
M13	VSS76	
M21	VSS77	
N4	VSS78	
	VSS79	
	VSS80	
	VSS81	
	VSS82	
	VSS83	
	VSS84	



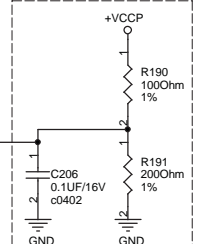
Power :  
+VCCP



Signal voltage level =  
0.3125 \* VCCP  
Trace should be 10 mil wide  
with 20 mil spacing



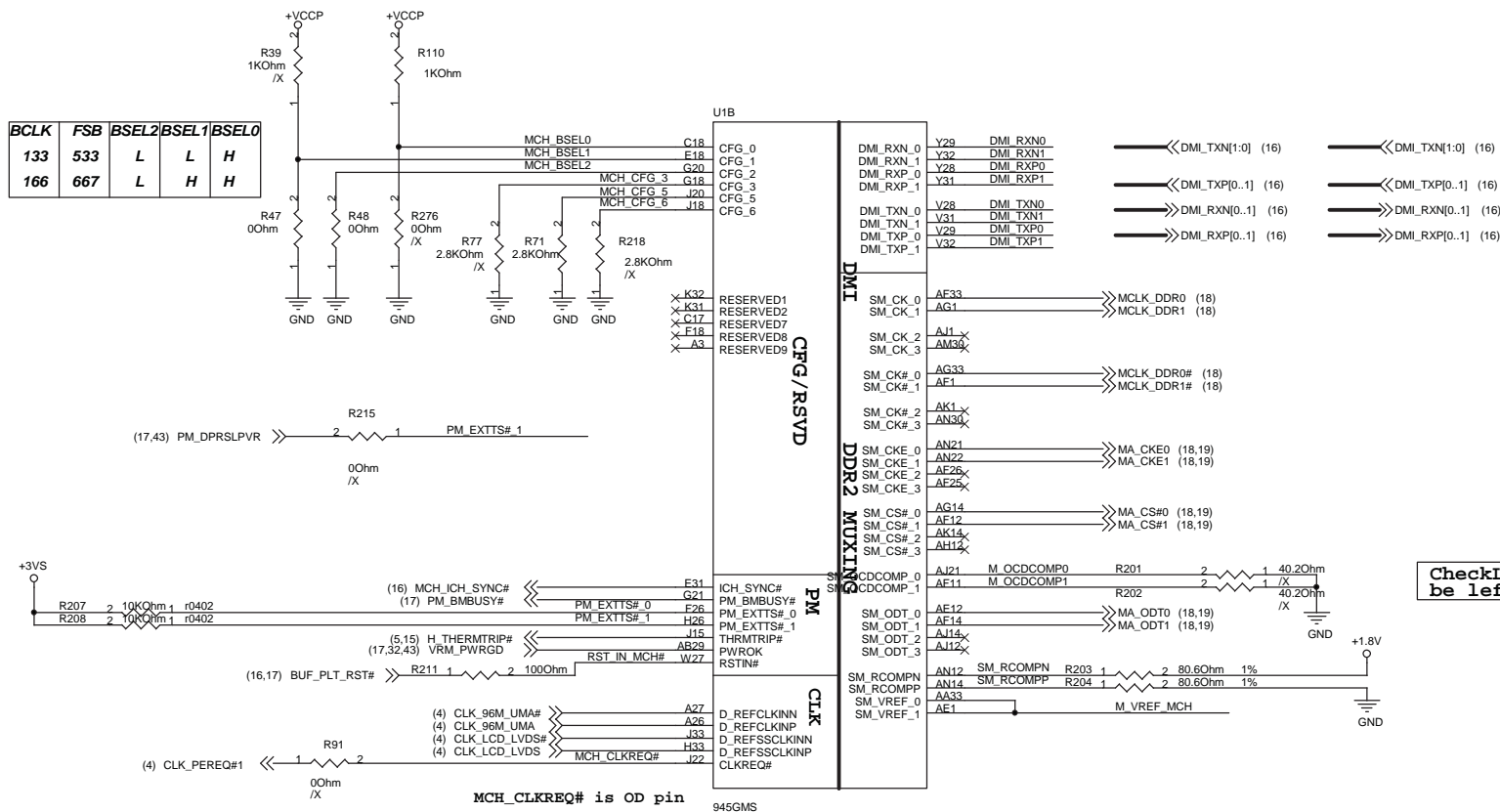
AGTL+ I/O Voltage Reference



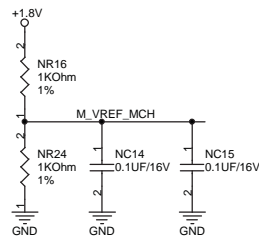
Layout Note:  
0.1uF should be placed 100mils or less from GMCH pin.

<Core Design>

		Title : NB-945GMS(HOST)	
ASUSTek COMPUTER INC.		Engineer: Satan He	
Size	Project Name	Rev	
A3	1000	1.0G	
Date: Tuesday, August 12, 2008		Sheet 7 of 50	



CheckList notes : Can be left as NC

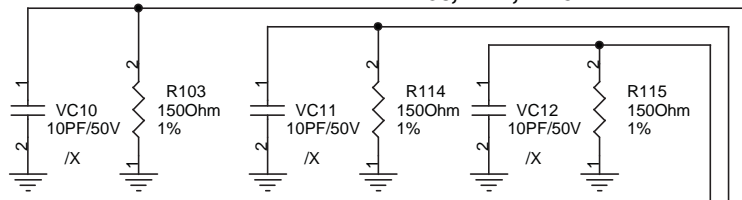


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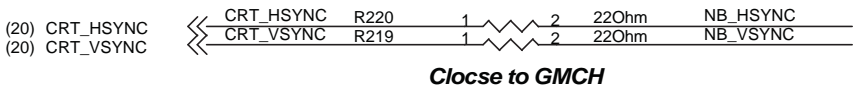
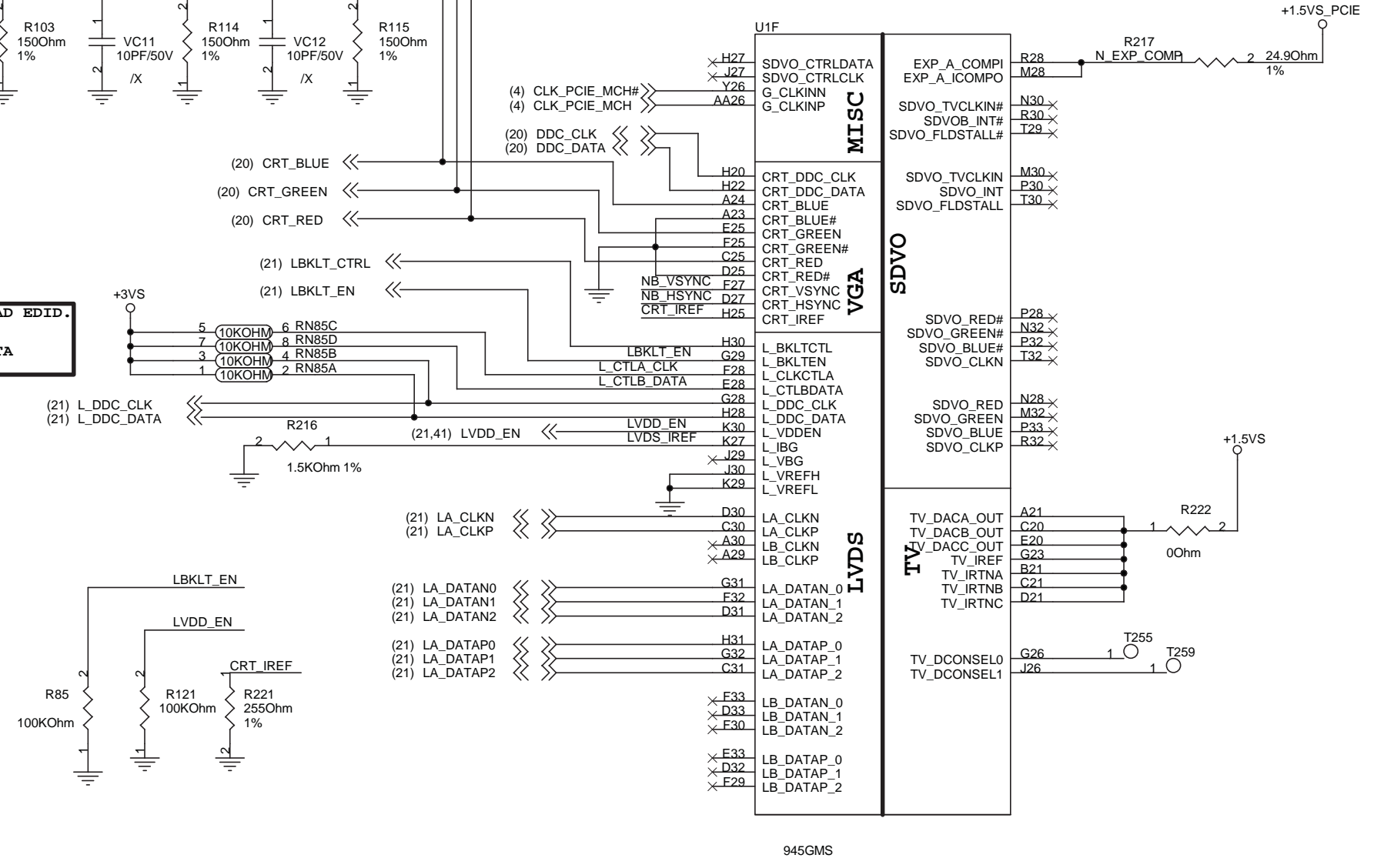
<b>ASUS</b>		<b>Title : NB-945GMS(DMI &amp; CFG)</b>	
ASUSTeK COMPUTER INC.		<b>Engineer: Satan He</b>	
Size	Project Name	Rev	
A3	<b>1000</b>	1.0G	
Date: Tuesday, August 12, 2008		Sheet 8 of 50	



Close to GMCH  
R103,R114,R115



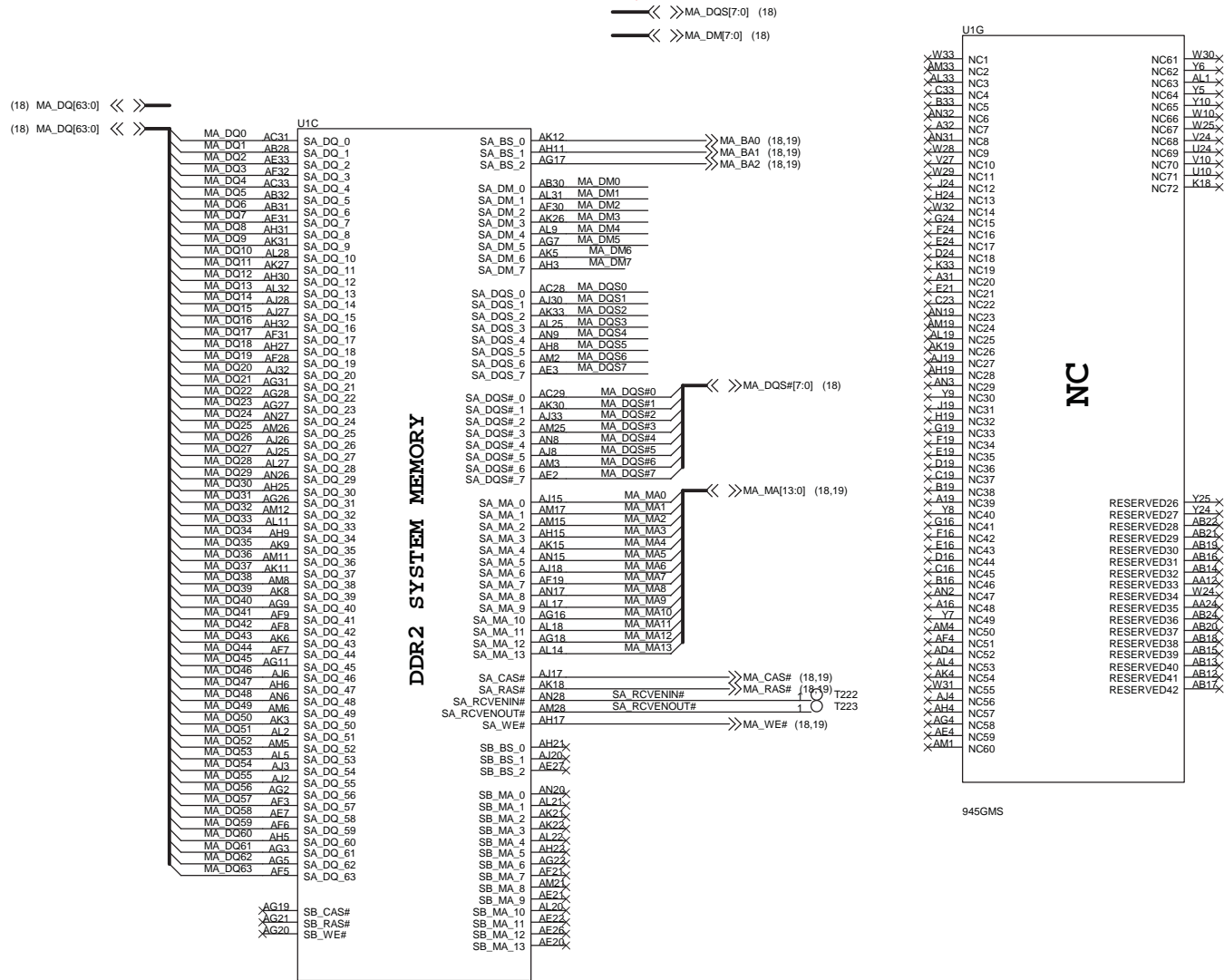
IF USE NB READ EDID.  
MUST CONNECT  
L\_DDC\_CLK&DATA



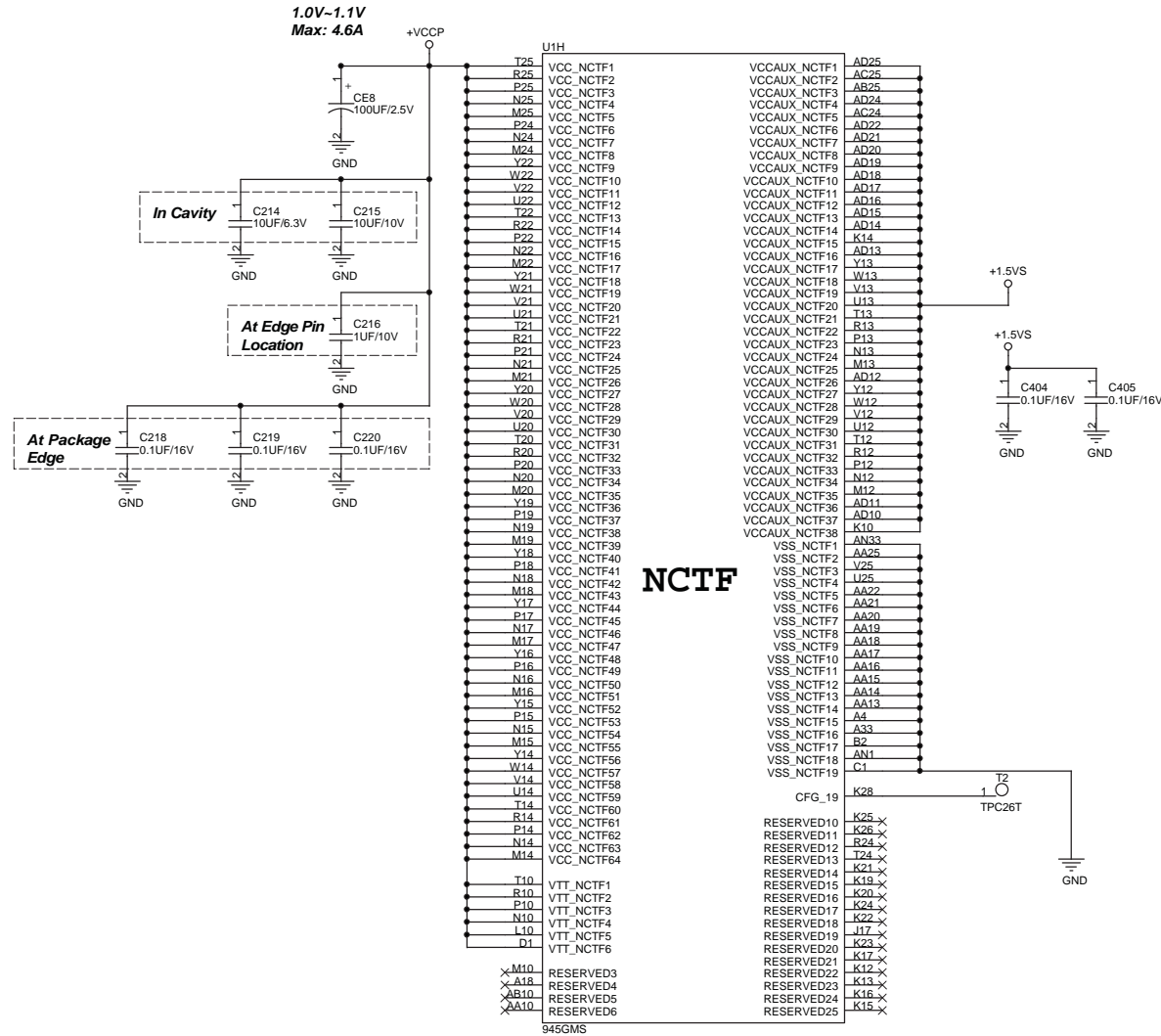
945GMS

<Core Design>

		<b>Title :</b> NB-945GMS(GRAPHIC)	
ASUSTeK COMPUTER INC.		<b>Engineer:</b> Satan_He	
Size A4	Project Name <b>1000</b>	Rev 1.0G	
Date: Tuesday, August 12, 2008		Sheet	9 of 50

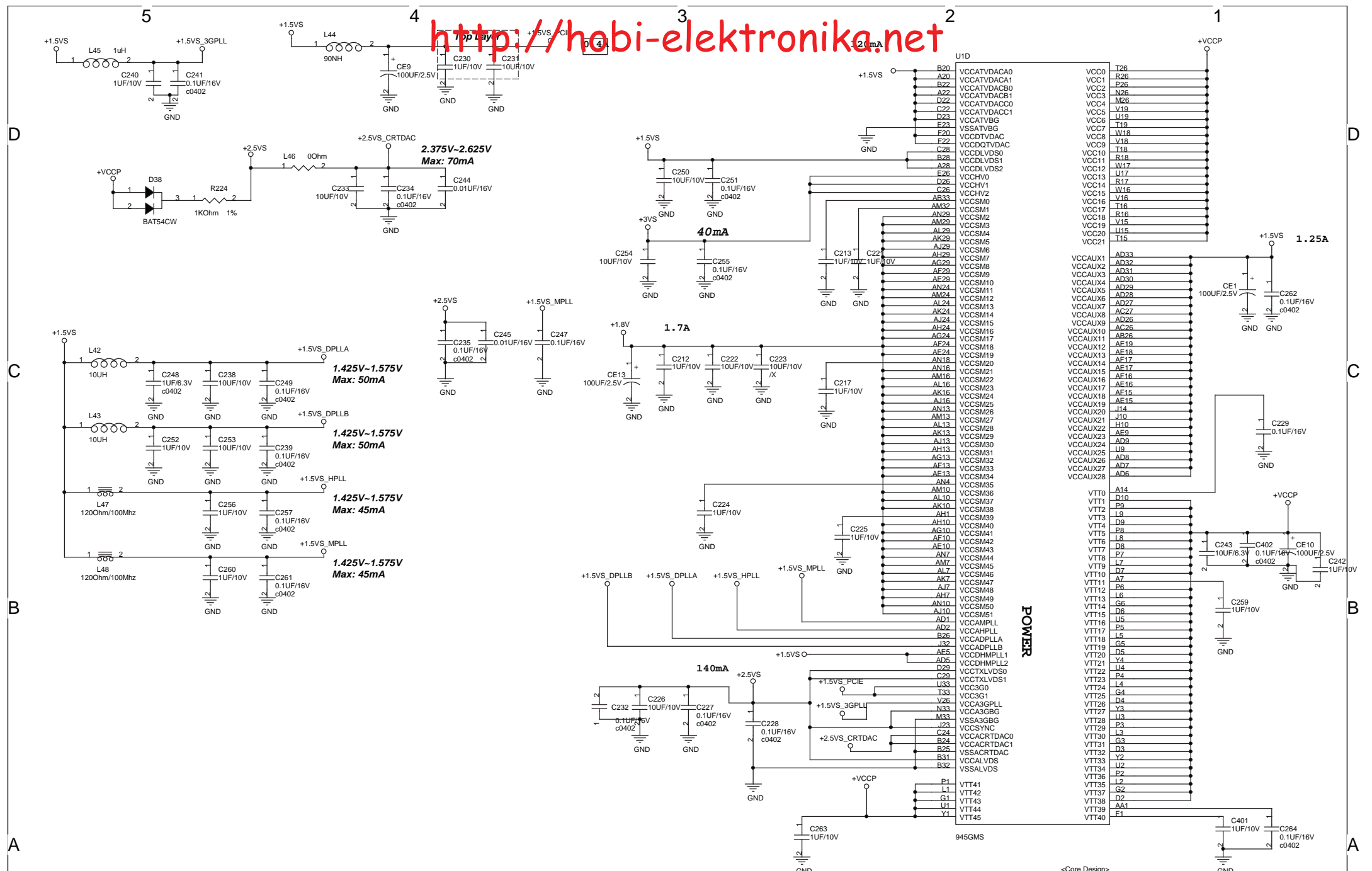


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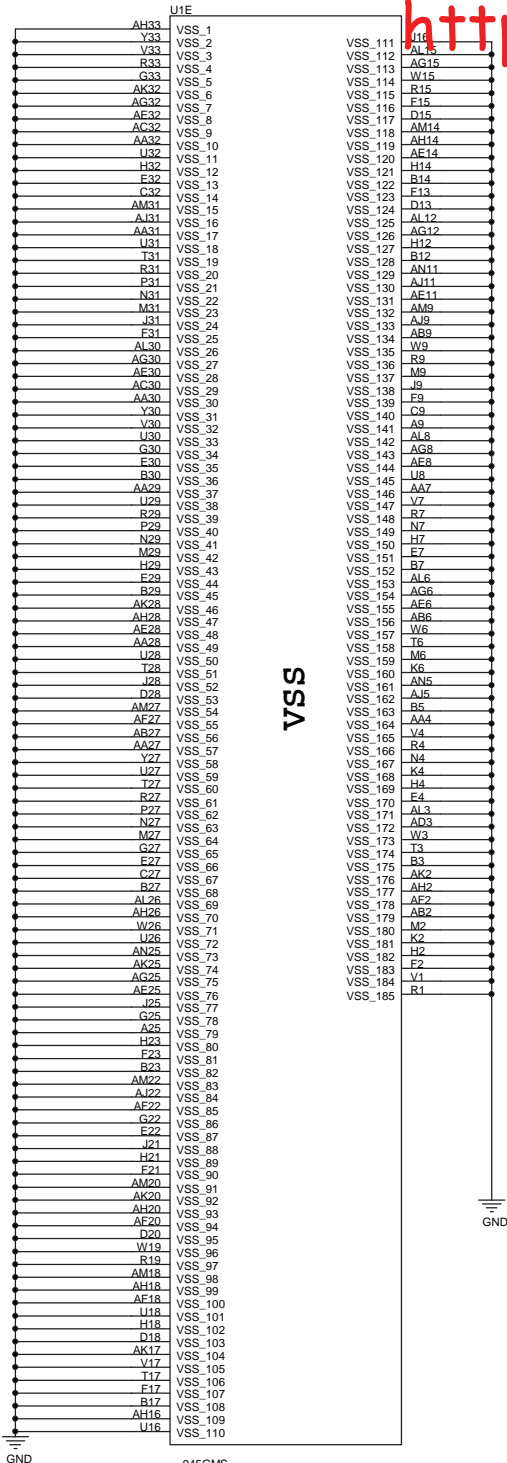


**CFG\_19(K28) Strapping :**  
**DMI LANE Reversal:**  
**0:Normal Operation (Default)**  
**1.:Reversal Lanes, 3->0,2->1..etc**  
**Note:945GMS doesn't support DMI Lane Reversal**

<Core Design>

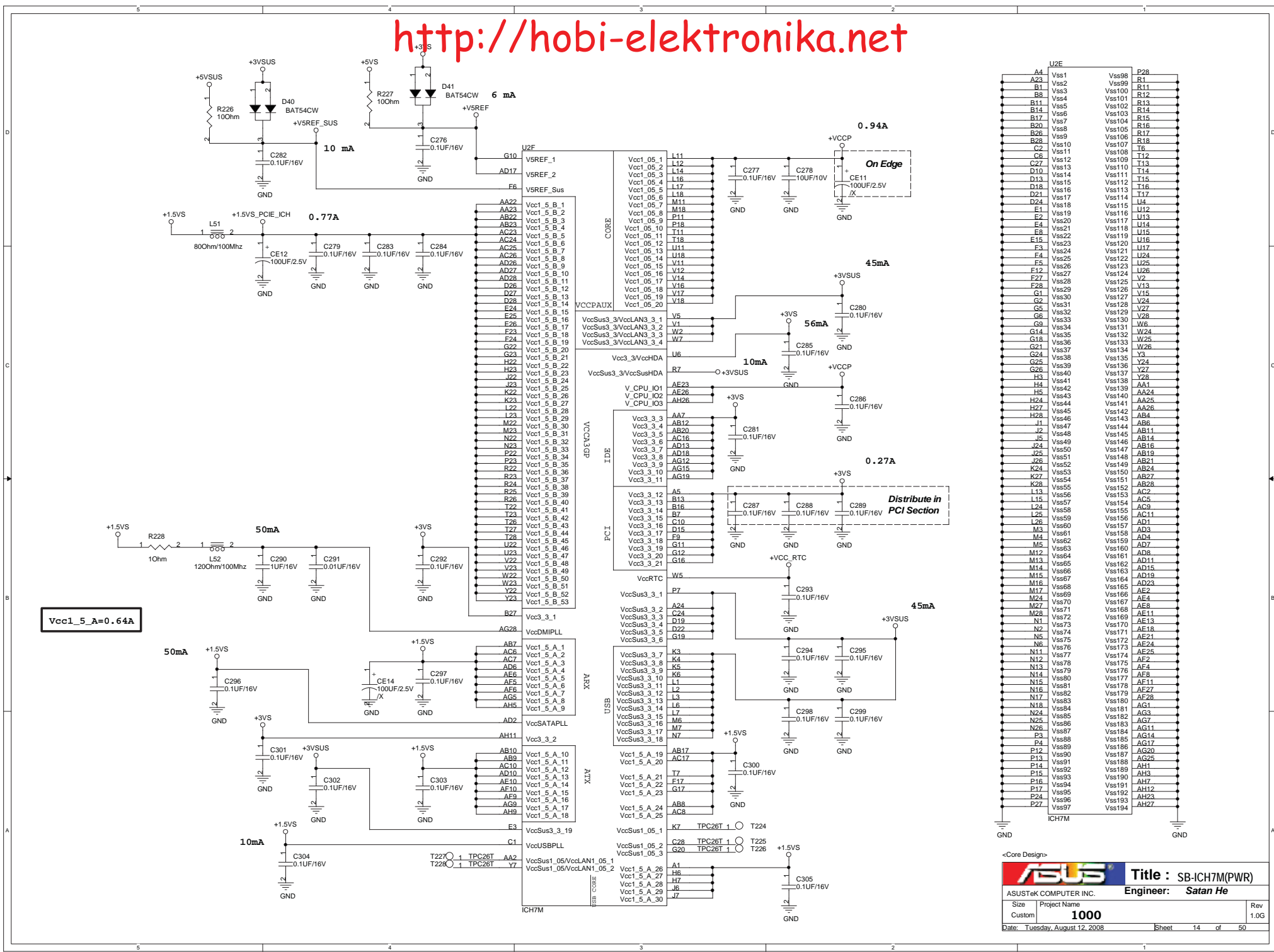


<http://hobi-elektronika.net>



<Core Design>

		<b>Title :</b> NB-945PMS(GND)	
ASUSTeK COMPUTER INC.		<b>Engineer:</b> Satan_He	
Size	Project Name	Rev	
A3	<b>1000</b>	1.0G	
Date:	Tuesday, August 12, 2008	Sheet	13 of 50



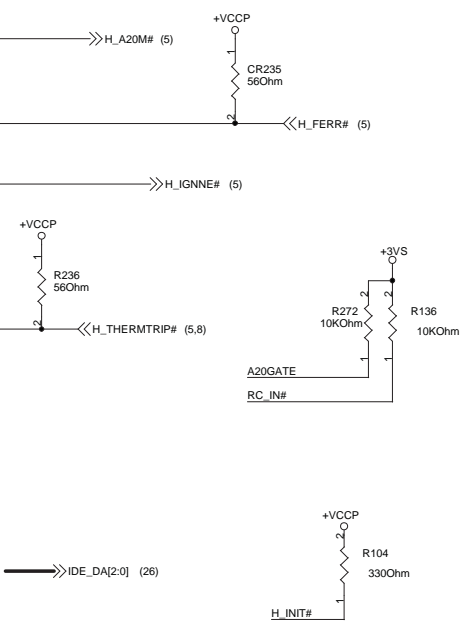
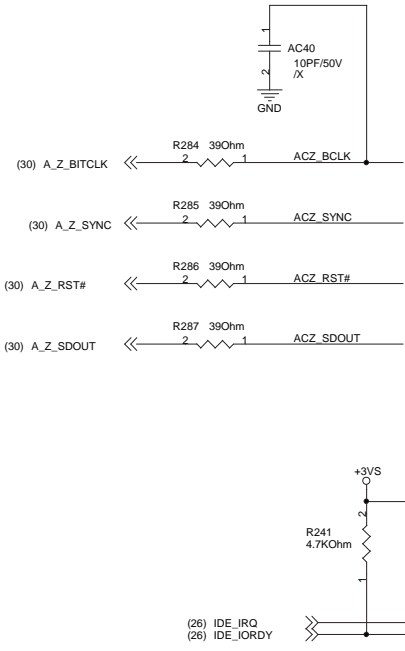
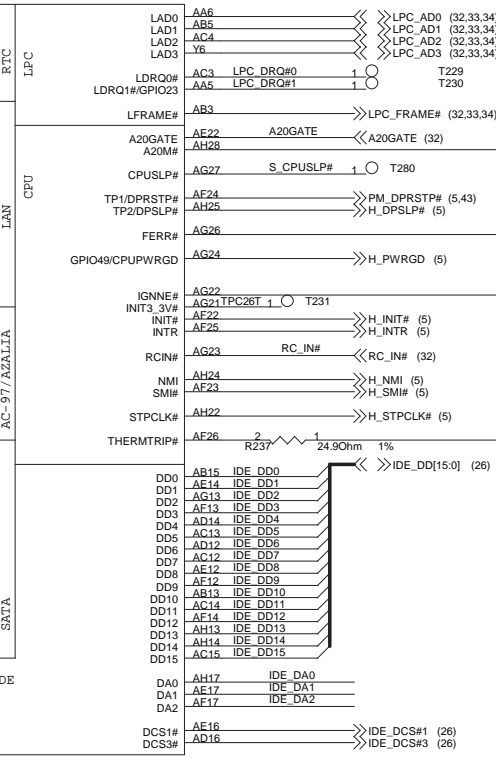
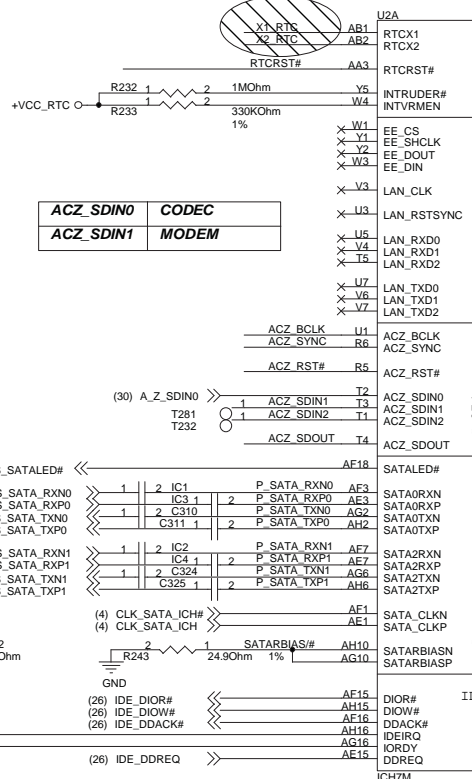
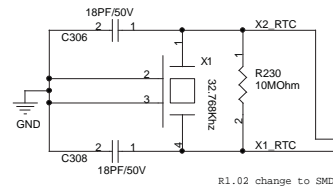
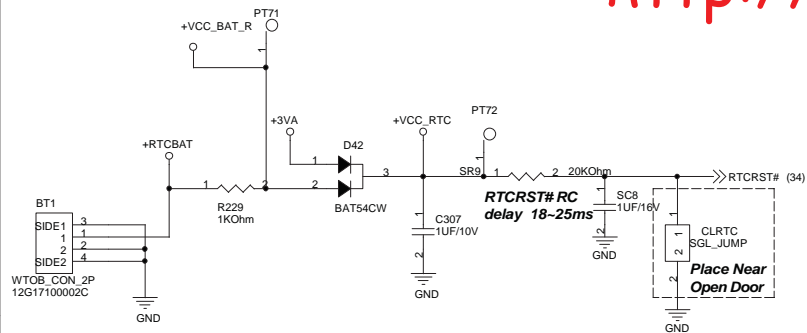
U2E		
A4	Vss1	Vss98
A23	Vss2	P28
B1	Vss3	R1
B8	Vss4	R11
B11	Vss5	Vss100
B14	Vss6	Vss101
B17	Vss7	Vss102
B20	Vss8	Vss103
B26	Vss9	Vss104
B28	Vss10	Vss105
C2	Vss11	Vss106
C6	Vss12	Vss107
C7	Vss13	Vss108
D10	Vss14	Vss109
D13	Vss15	Vss110
D18	Vss16	Vss111
D21	Vss17	Vss112
D22	Vss18	Vss113
D24	Vss19	Vss114
E1	Vss20	Vss115
E2	Vss21	Vss116
E4	Vss22	Vss117
E8	Vss23	Vss118
F15	Vss24	Vss119
F4	Vss25	Vss120
F4	Vss26	Vss121
F5	Vss27	Vss122
F12	Vss28	Vss123
F27	Vss29	Vss124
F28	Vss30	Vss125
G1	Vss31	Vss126
G2	Vss32	Vss127
G5	Vss33	Vss128
G6	Vss34	Vss129
G9	Vss35	Vss130
G14	Vss36	Vss131
G18	Vss37	Vss132
G21	Vss38	Vss133
G24	Vss39	Vss134
G25	Vss40	Vss135
G26	Vss41	Vss136
H3	Vss42	Vss137
H4	Vss43	Vss138
H5	Vss44	Vss139
H24	Vss45	Vss140
H27	Vss46	Vss141
H28	Vss47	Vss142
J1	Vss48	Vss143
J2	Vss49	Vss144
J5	Vss50	Vss145
J25	Vss51	Vss146
J26	Vss52	Vss147
K24	Vss53	Vss148
K27	Vss54	Vss149
K28	Vss55	Vss150
L13	Vss56	Vss151
L15	Vss57	Vss152
L24	Vss58	Vss153
L25	Vss59	Vss154
L26	Vss60	Vss155
M3	Vss61	Vss156
M4	Vss62	Vss157
M5	Vss63	Vss158
M12	Vss64	Vss159
M13	Vss65	Vss160
M14	Vss66	Vss161
M15	Vss67	Vss162
M16	Vss68	Vss163
M17	Vss69	Vss164
M24	Vss70	Vss165
M27	Vss71	Vss166
M28	Vss72	Vss167
N1	Vss73	Vss168
N2	Vss74	Vss169
N5	Vss75	Vss170
N6	Vss76	Vss171
N11	Vss77	Vss172
N12	Vss78	Vss173
N13	Vss79	Vss174
N14	Vss80	Vss175
N15	Vss81	Vss176
N16	Vss82	Vss177
N17	Vss83	Vss178
N18	Vss84	Vss179
N24	Vss85	Vss180
N25	Vss86	Vss181
N26	Vss87	Vss182
P1	Vss88	Vss183
P4	Vss89	Vss184
P12	Vss90	Vss185
P13	Vss91	Vss186
P14	Vss92	Vss187
P15	Vss93	Vss188
P16	Vss94	Vss189
P17	Vss95	Vss190
P24	Vss96	Vss191
P27	Vss97	Vss192
P28	Vss98	Vss193
P29	Vss99	Vss194
P30	Vss100	Vss195

<Core Design>

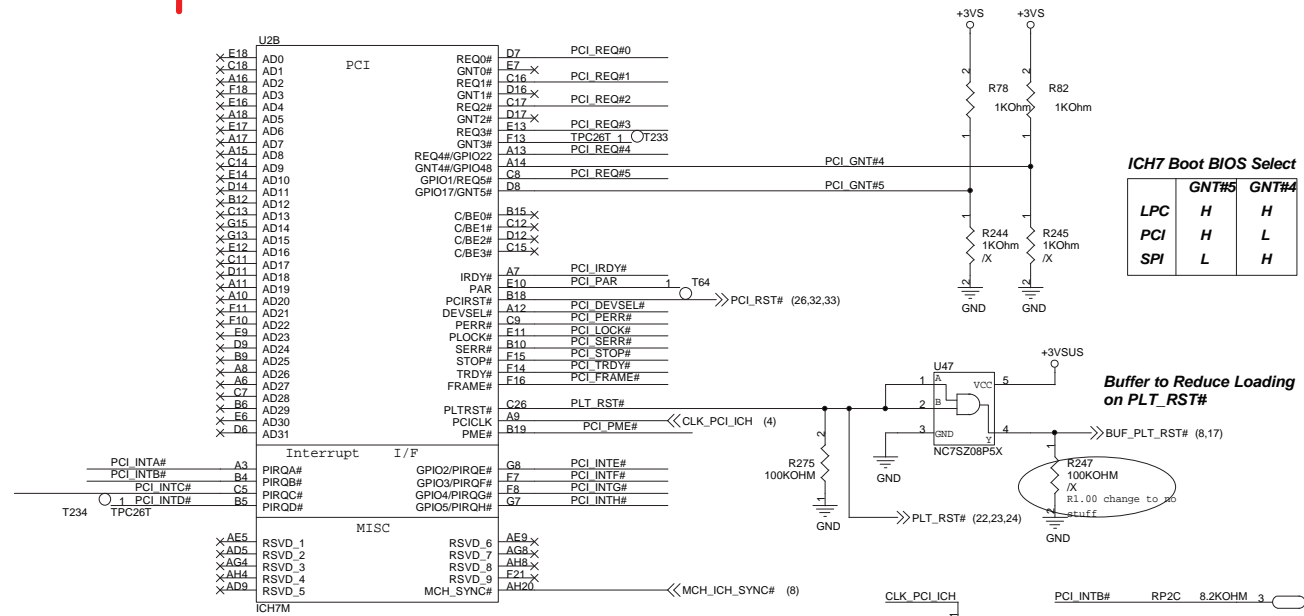
**Title : SB-ICH7M(PWR)**  
**Engineer: Satan He**

Size	Project Name	Rev
Custom	<b>1000</b>	1.0G

Date: Tuesday, August 12, 2008 Sheet 14 of 50





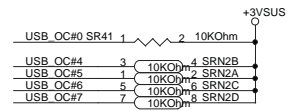


**ICH7 Boot BIOS Select**

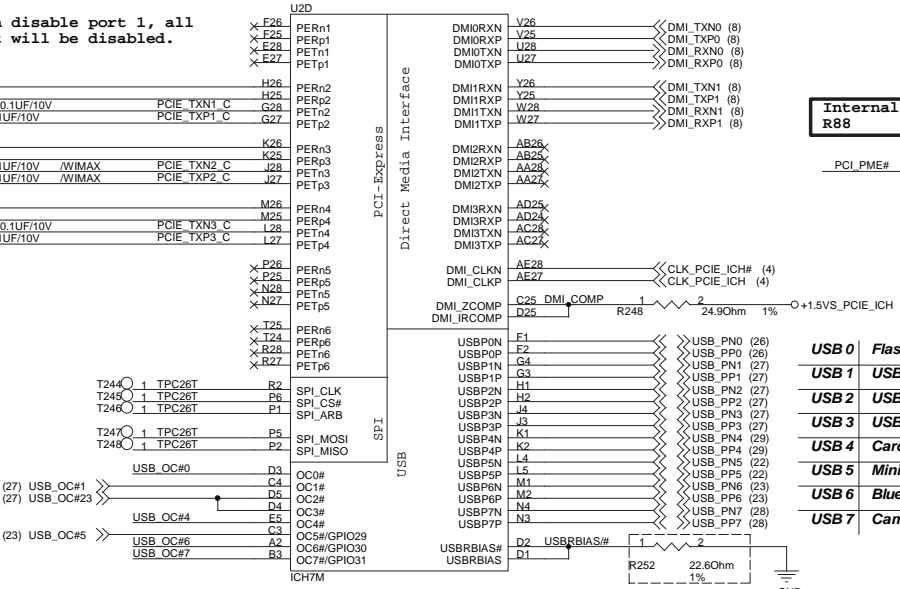
	GNT#5	GNT#4
LPC	H	H
PCI	H	L
SPI	L	H

**Buffer to Reduce Loading on PLT\_RST#**

- LAN AR8113 IC
- 3.5G, GPS, DTV, Wimax
- WiFi PCIExpress Card

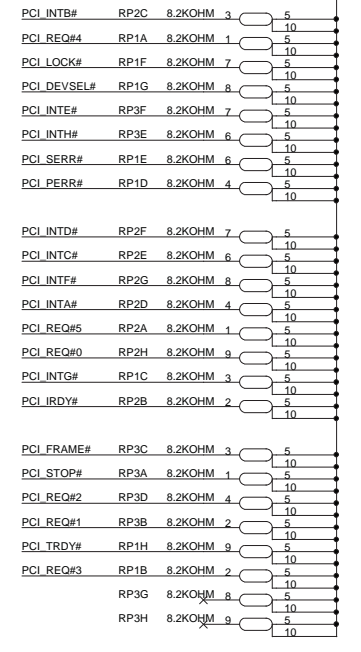


When disable port 1, all port will be disabled.

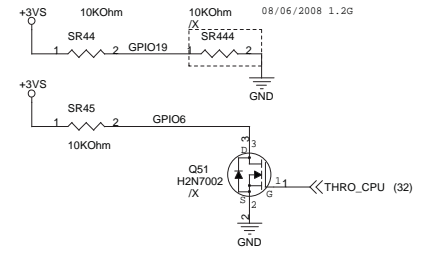
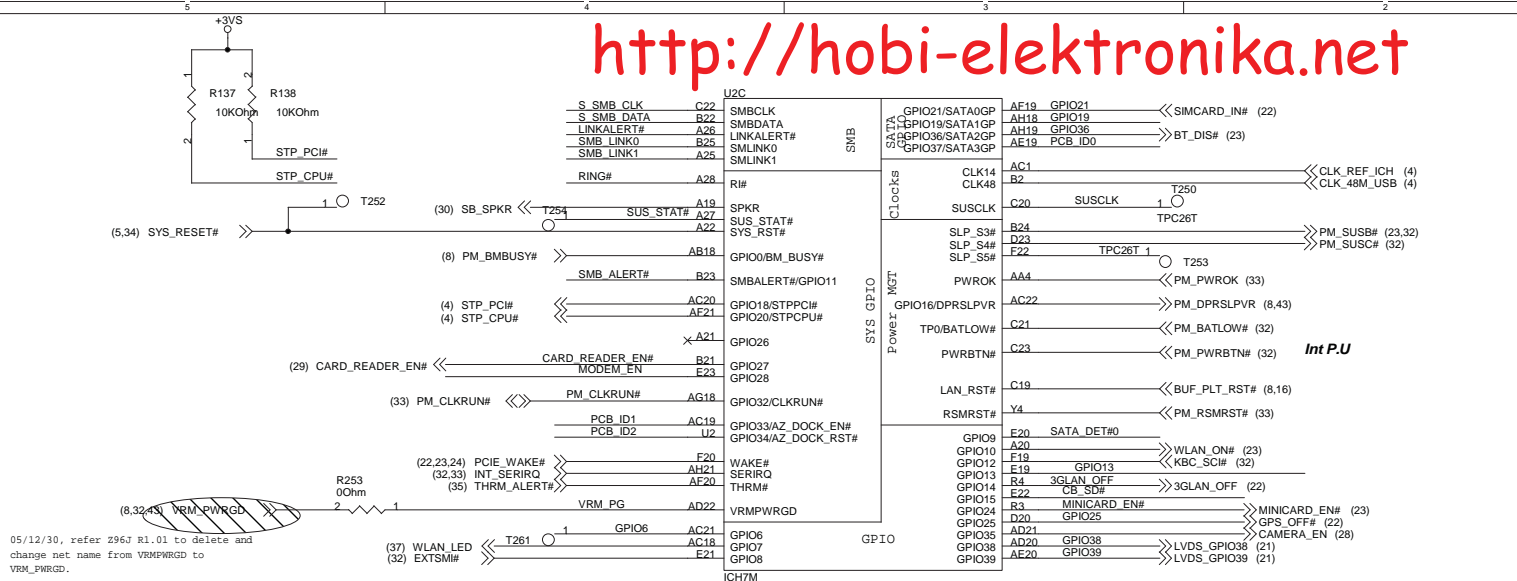


**Internal Pull-Up R88**

**CRB & Checklist**



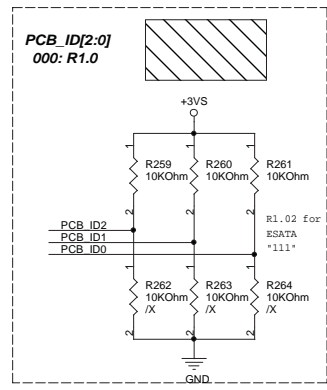
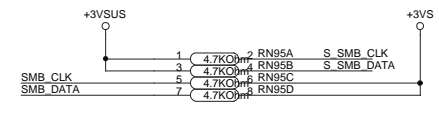
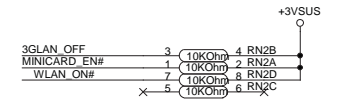
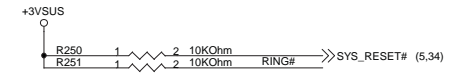
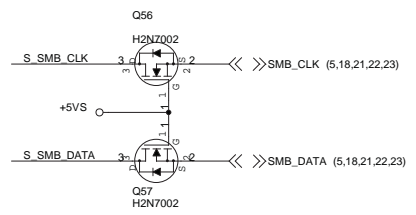




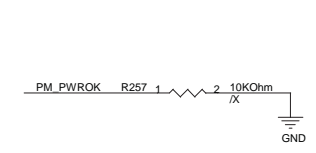
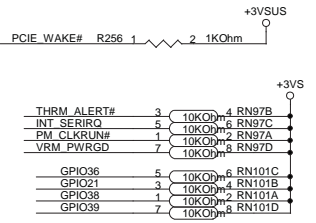
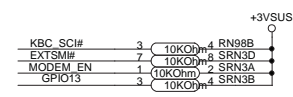
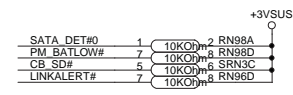
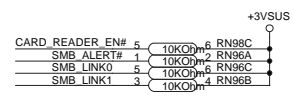
05/12/30, refer Z961 R1.01 to delete and change net name from VRMPWRGD to VRM\_PWRGD.

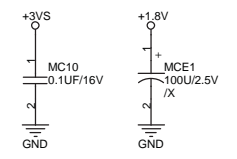
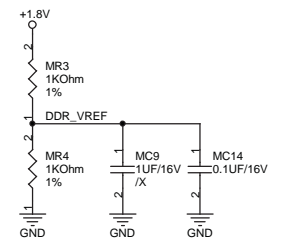
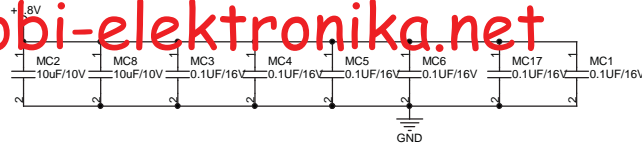
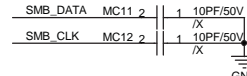
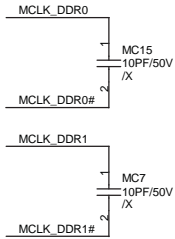
S\_SMB\_CLK << S\_SMB\_CLK (4)  
S\_SMB\_DATA << S\_SMB\_DATA (4)

WLAN_LED	WLAN	BT
High	v	v
High	v	x
High	x	v
Low	x	x



SKU	PCB_ID3 SB GPIO 19	PCB_ID2 SB GPIO 34	PCB_ID1 SB GPIO 33	PCB_ID0 SB GPIO 37
DTV	1	1	1	1
BASIC	1	1	1	0
3.5G	1	1	0	1
GPS	1	1	0	0
WiMAX	1	0	1	1
BASIC (SATA)	1	0	1	0

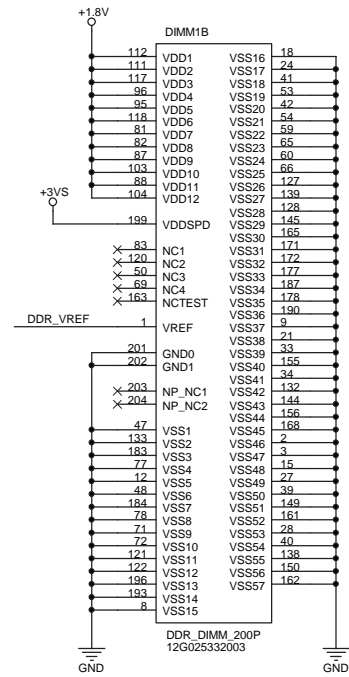




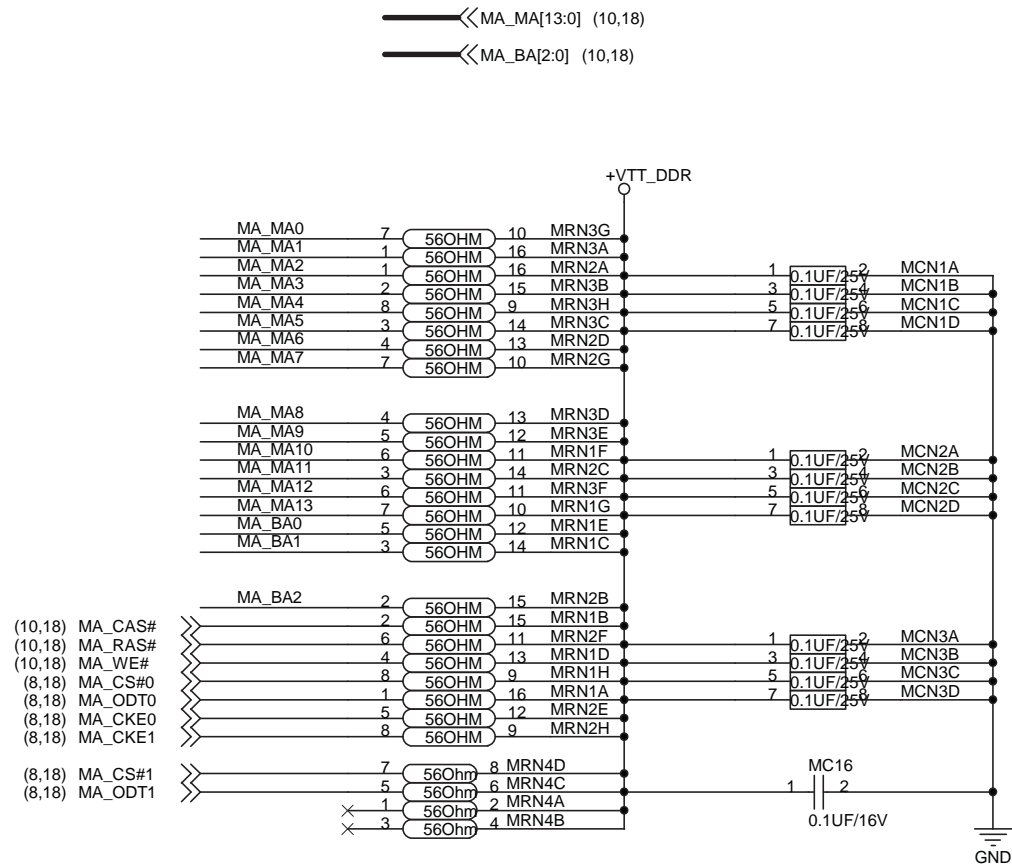
STD Type

DIMM1A			
MA_MA0	102	A0	5
MA_MA1	101	A1	7
MA_MA2	100	A2	17
MA_MA3	99	A3	19
MA_MA4	98	A4	4
MA_MA5	97	A5	6
MA_MA6	94	A6	14
MA_MA7	93	A7	16
MA_MA8	92	A8	23
MA_MA9	91	A9	25
MA_MA10	105	A10/AP	35
MA_MA11	90	A11	37
MA_MA12	89	A12	20
MA_MA13	116	A13	22
	86	A14	38
	84	A15	38
	85	A16_BA2	43
MA_BA0	107	BA0	45
MA_BA1	106	BA1	57
	110	BA1	57
	115	BA1	57
	30	CK0	56
	32	CK0#	58
	166	CK1	61
	79	CK1#	63
	80	CKE0	73
	80	CKE1	75
	113	CAS#	77
	108	RAS#	62
	109	RAS#	64
	198	WE#	74
	200	SA0	76
	197	SCL	123
	195	SDA	125
	114	ODT0	135
	119	ODT1	137
	10	DM0	124
	26	DM1	126
	52	DM2	134
	67	DM3	136
	130	DM4	141
	147	DM5	143
	170	DM6	151
	185	DM7	153
	13	DQS0	140
	31	DQS1	142
	51	DQS2	152
	70	DQS3	154
	131	DQS4	157
	148	DQS5	159
	169	DQS6	173
	188	DQS7	175
	11	DQS#0	158
	29	DQS#1	160
	49	DQS#2	174
	68	DQS#3	176
	129	DQS#4	193
	146	DQS#5	193
	167	DQS#6	194
	186	DQS#7	194

GROUP1  
GROUP2  
SWAP

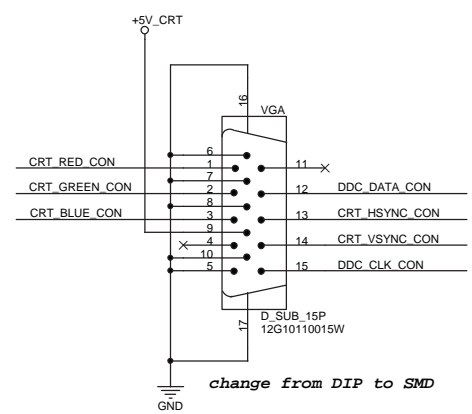
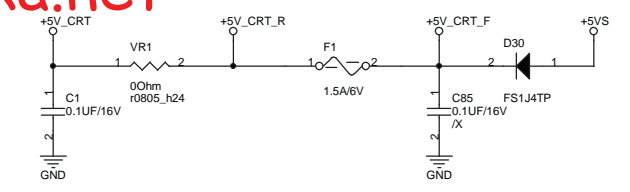
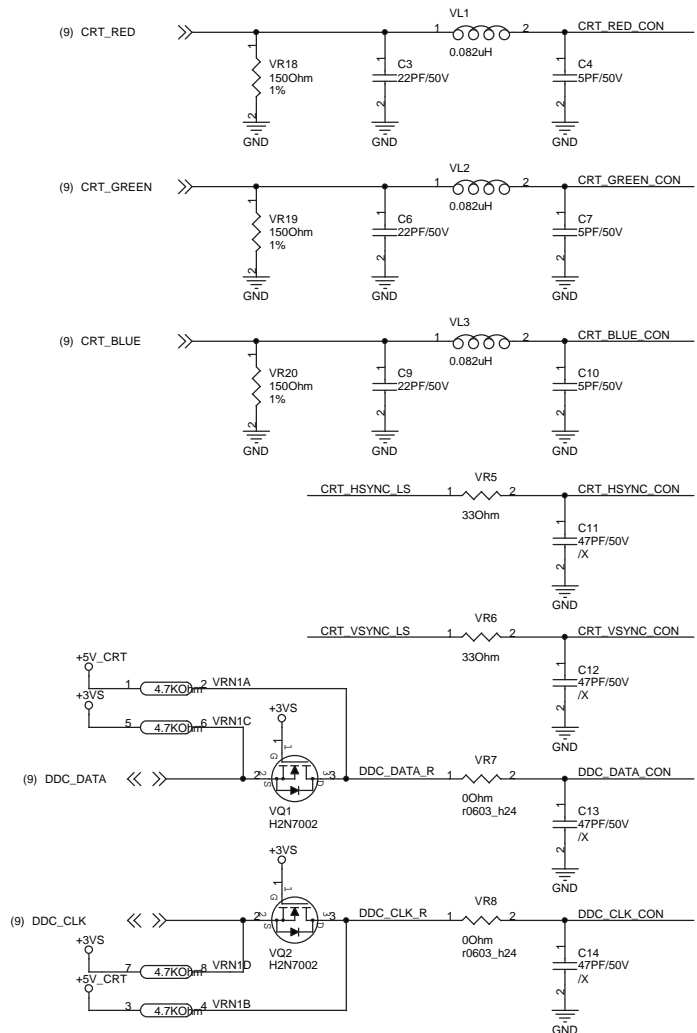


DDR\_DIMM\_200P  
12G025332003

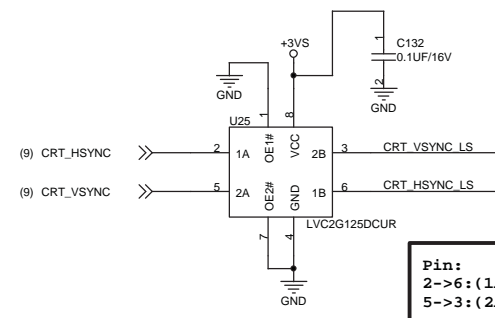
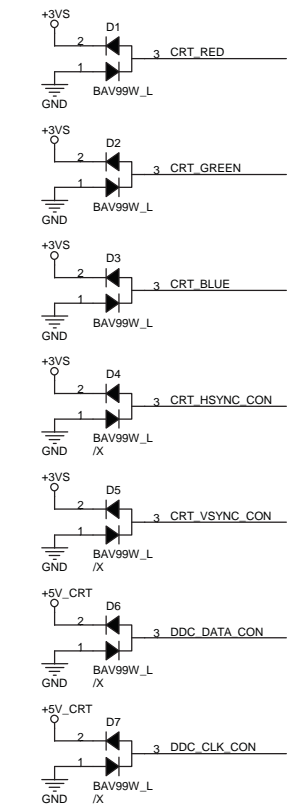


<Core Design>

		<b>Title :</b> DDR2_Termination	
ASUSTek Computer INC.		<b>Engineer:</b> Kell_Huang	
Size	Project Name	Rev	
A4	<b>1000</b>	1.0G	
Date: Tuesday, August 12, 2008		Sheet	19 of 47



VGA use 12G10110015W & 12G10110015N



Pin:  
2->6: (1A->1B)  
5->3: (2A->2B)

- (9) LA\_CLKP <<>
- (9) LA\_CLKN <<>
- (9) LA\_DATAP2 <<>
- (9) LA\_DATAN2 <<>
- (9) LA\_DATAP1 <<>
- (9) LA\_DATAN1 <<>
- (9) LA\_DATAP0 <<>
- (9) LA\_DATAN0 <<>

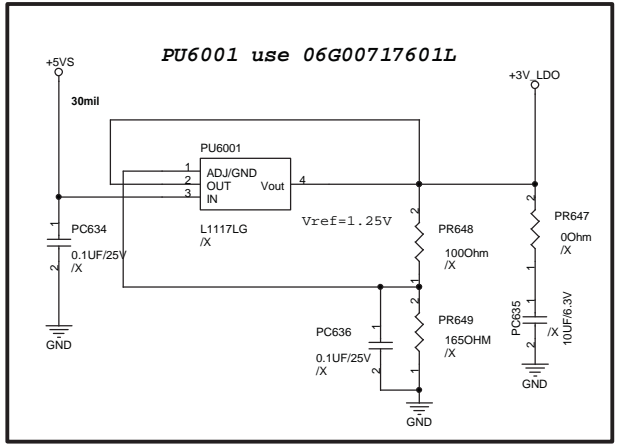
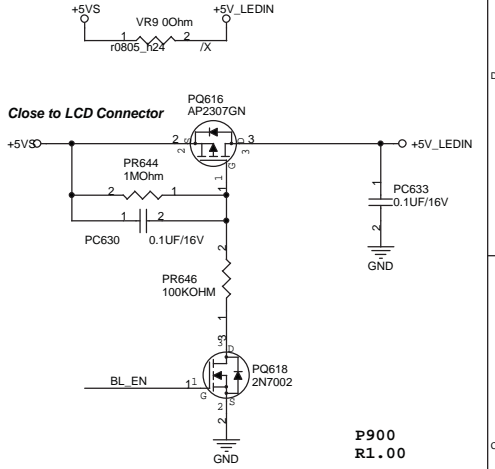
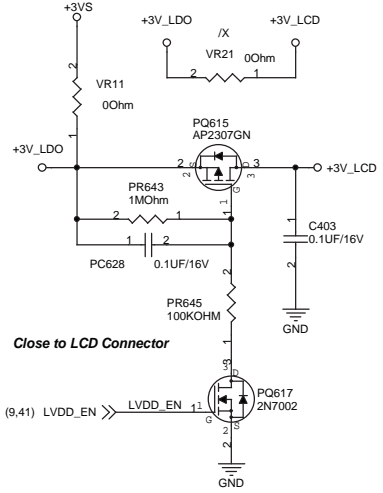
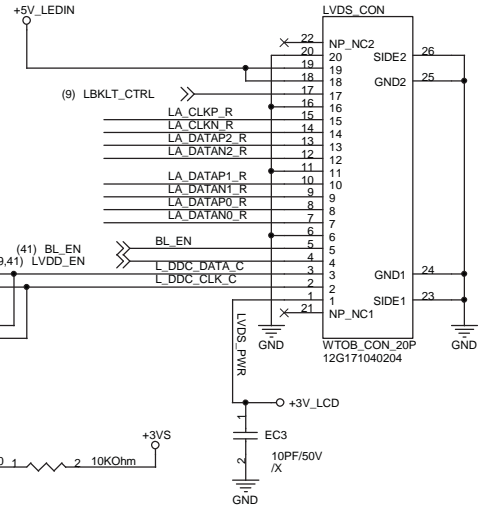
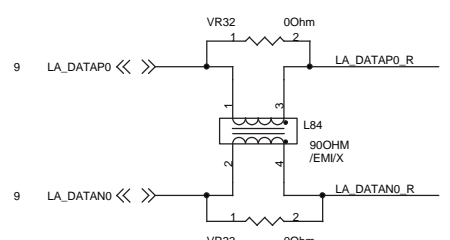
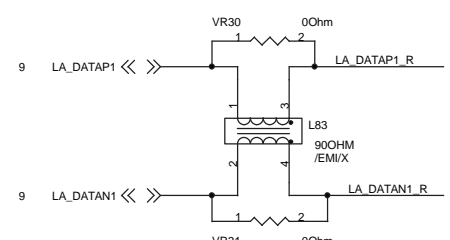
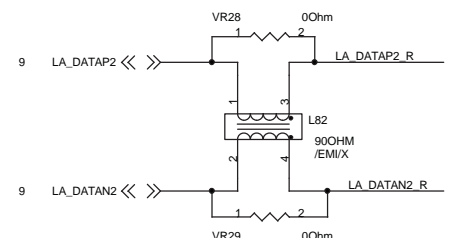
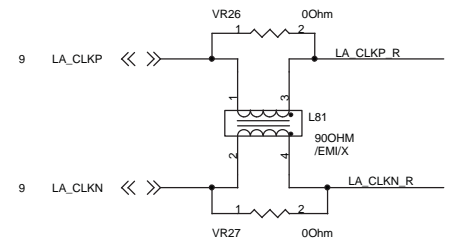
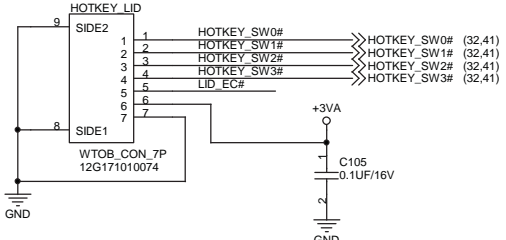
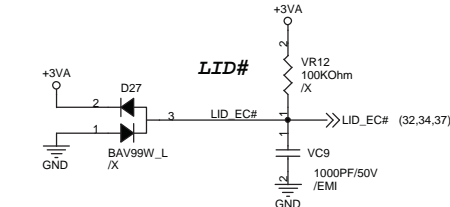
- (5,17,18,22,23) SMB\_DATA <<>
- (5,17,18,22,23) SMB\_CLK <<>

- (9) L\_DDC\_DATA <<>
- (9) L\_DDC\_CLK <<>

- (17) LVDS\_GPIO38 <<>
- (17) LVDS\_GPIO39 <<>

- (9) LBKLT\_EN <<>
- (32) LCD\_BACKOFF# <<>

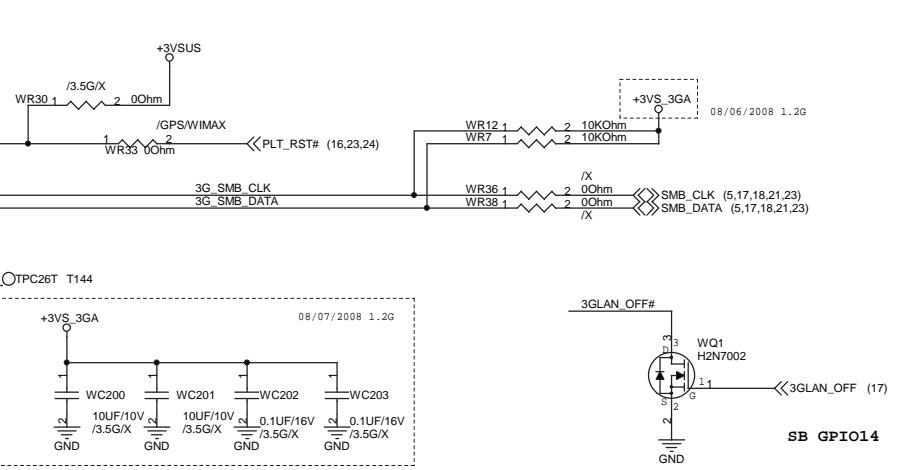
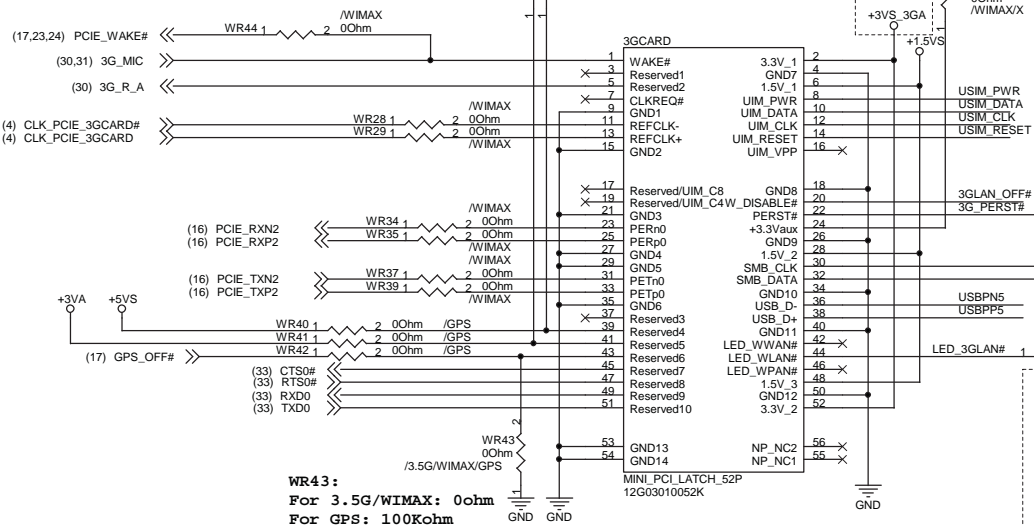
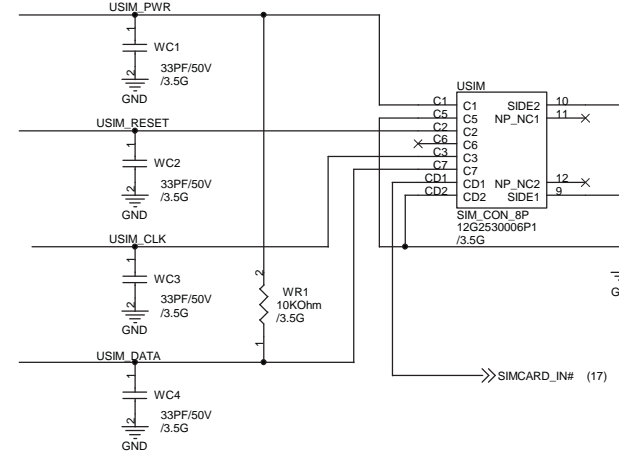
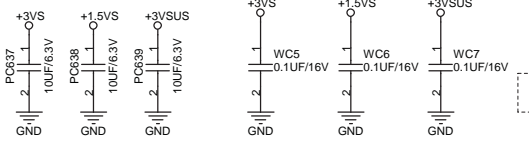
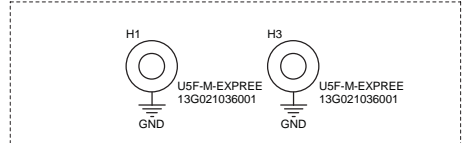
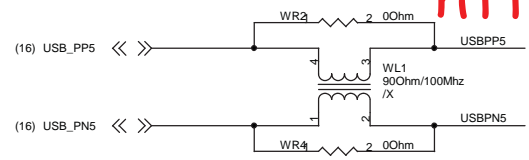
L DDC CLK C	EC1	2	1	10PF/50V
L DDC DATA C	EC2	2	1	10PF/50V
LA_CLKP_R	VC1	2	1	10PF/50V
LA_CLKN_R	VC2	2	1	10PF/50V
LA_DATAP2_R	VC3	2	1	10PF/50V
LA_DATAN2_R	VC4	2	1	10PF/50V
LA_DATAP1_R	VC5	2	1	10PF/50V
LA_DATAN1_R	VC6	2	1	10PF/50V
LA_DATAP0_R	VC7	2	1	10PF/50V
LA_DATAN0_R	VC8	2	1	10PF/50V



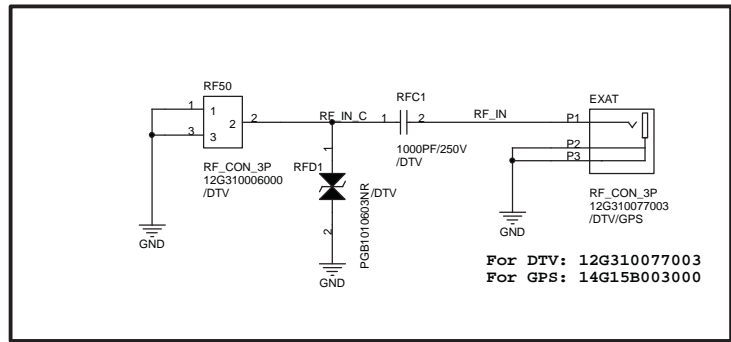
/GPS: AW GPS-M09  
 /DTV: ASUS MC3100U  
 /3.5G: SIERRA 8780  
 /WIMAX: INTEL5050

CAP Near SIM Socket

USIM\_PWR (41)

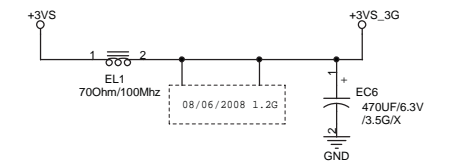
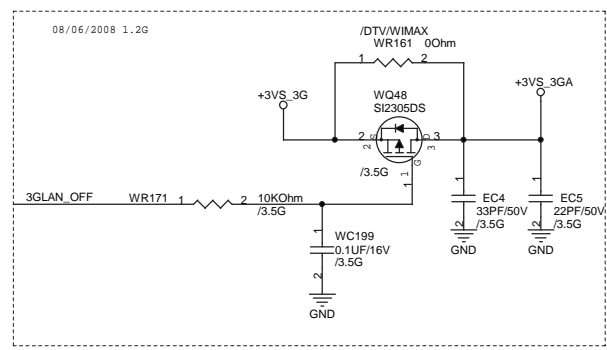


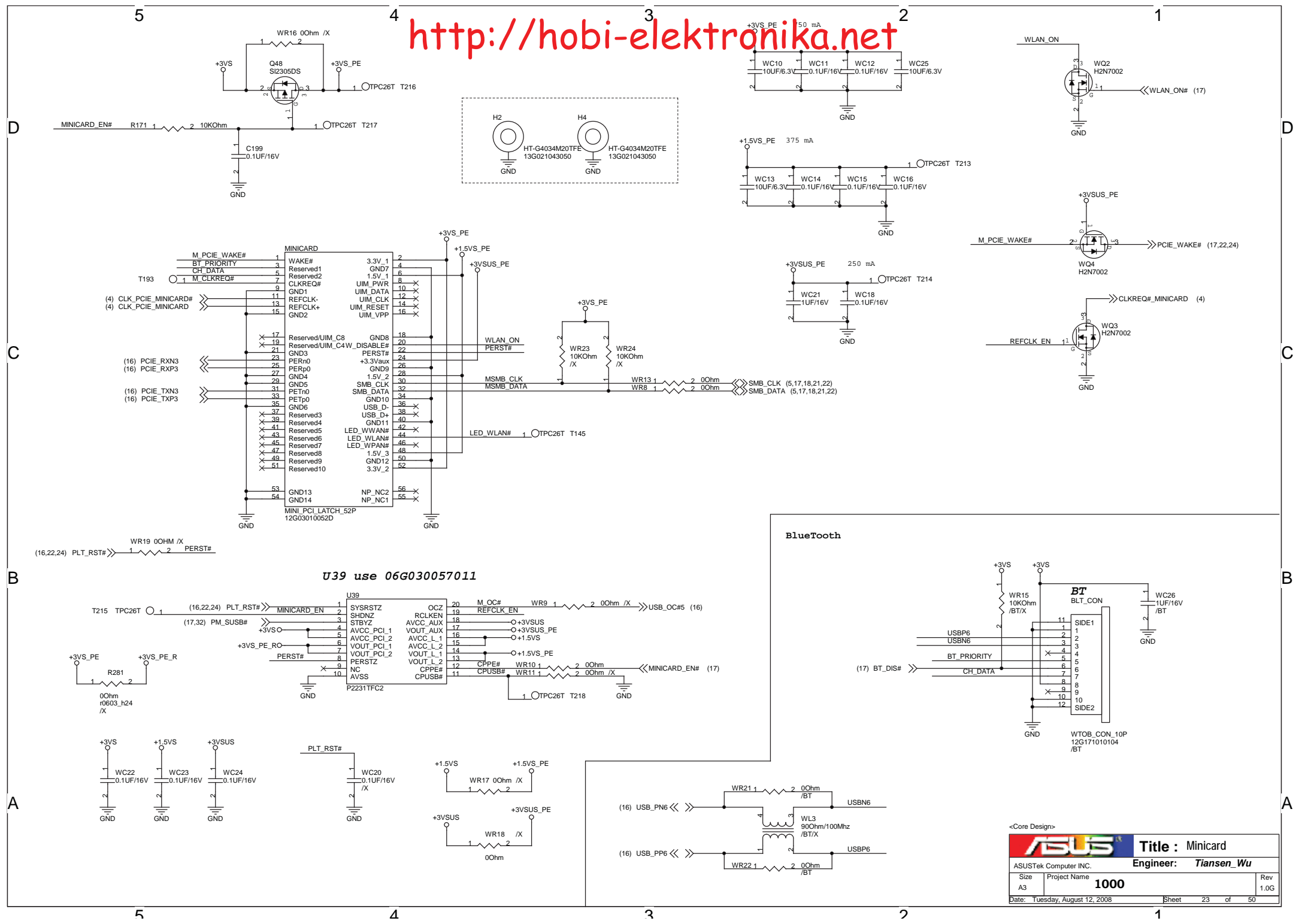
External Antenna



For DTV: 12G310077003  
 For GPS: 14G15B003000

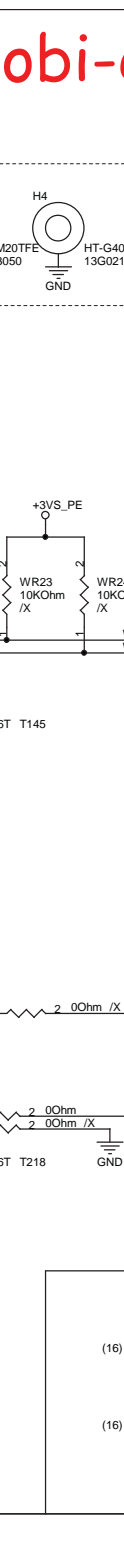
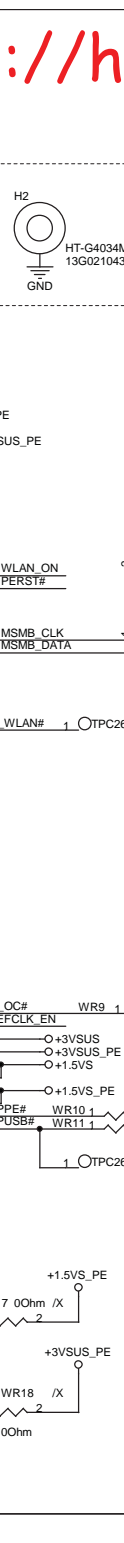
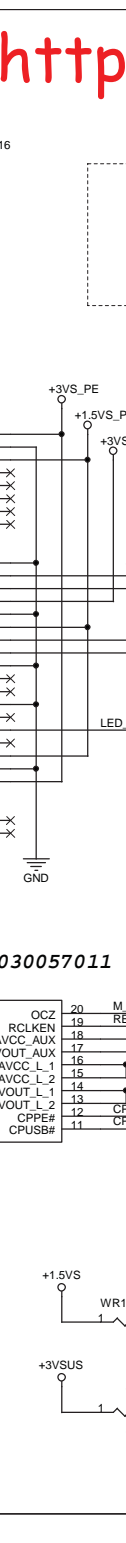
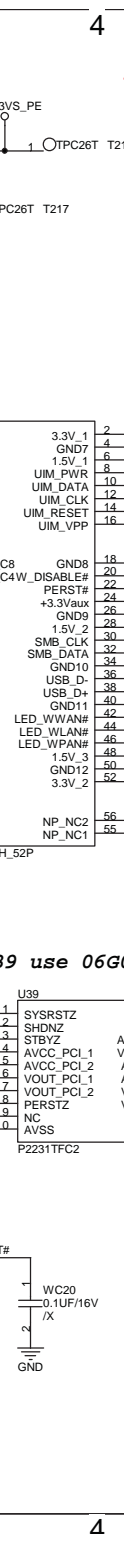
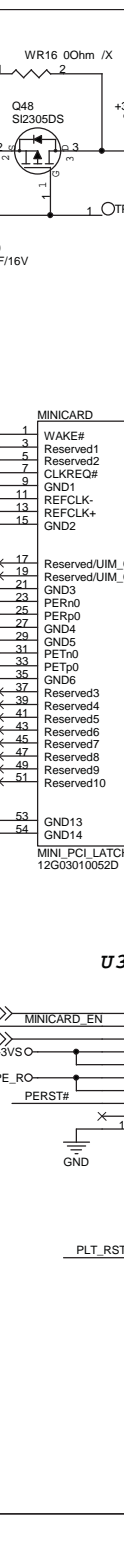
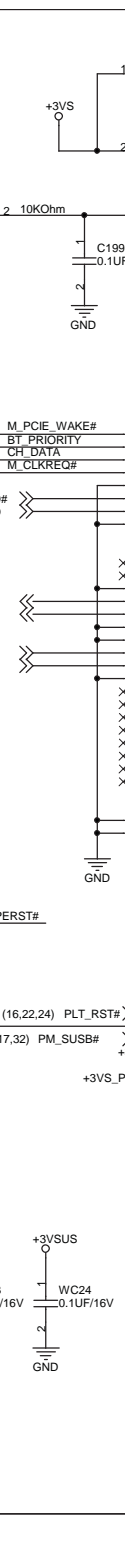
MINICARD use 12G03010052K



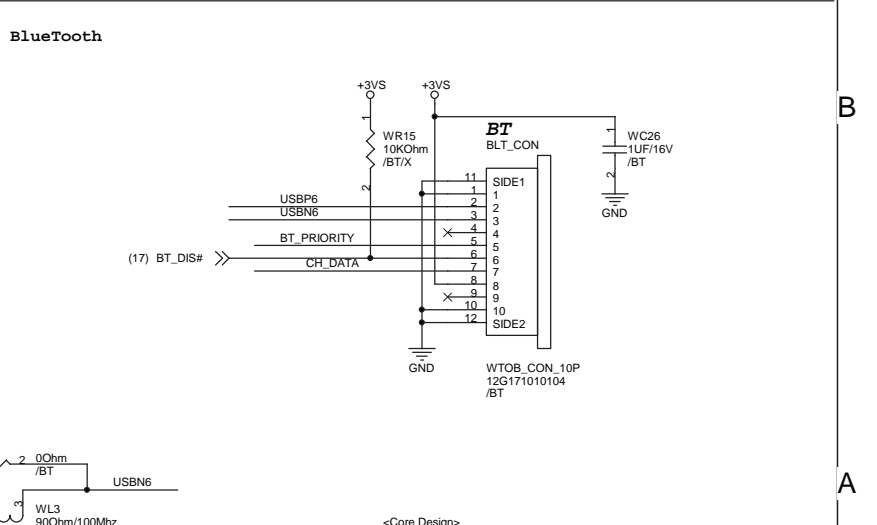
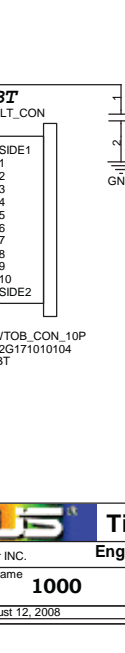
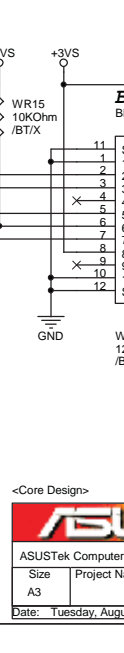
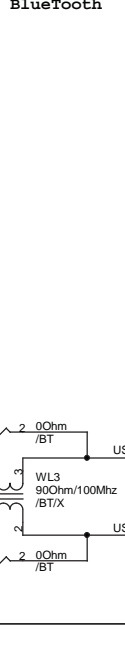
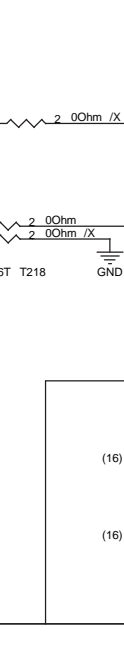
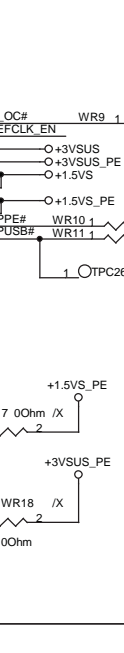
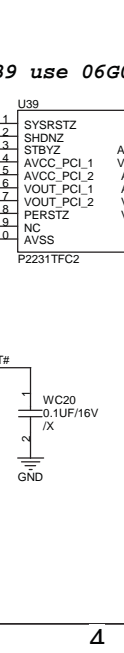
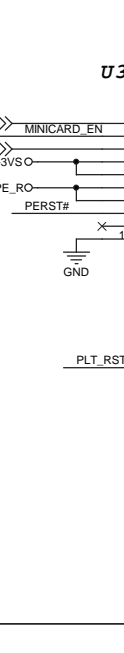
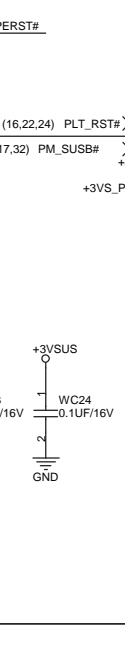
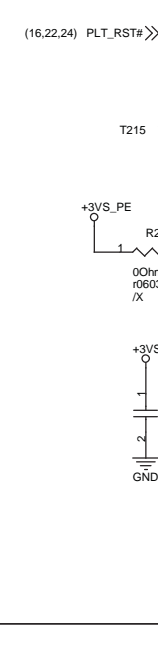


5  
4  
3  
2  
1  
D  
C  
B  
A

MINICARD\_EN# R171 1 2 10KOhm

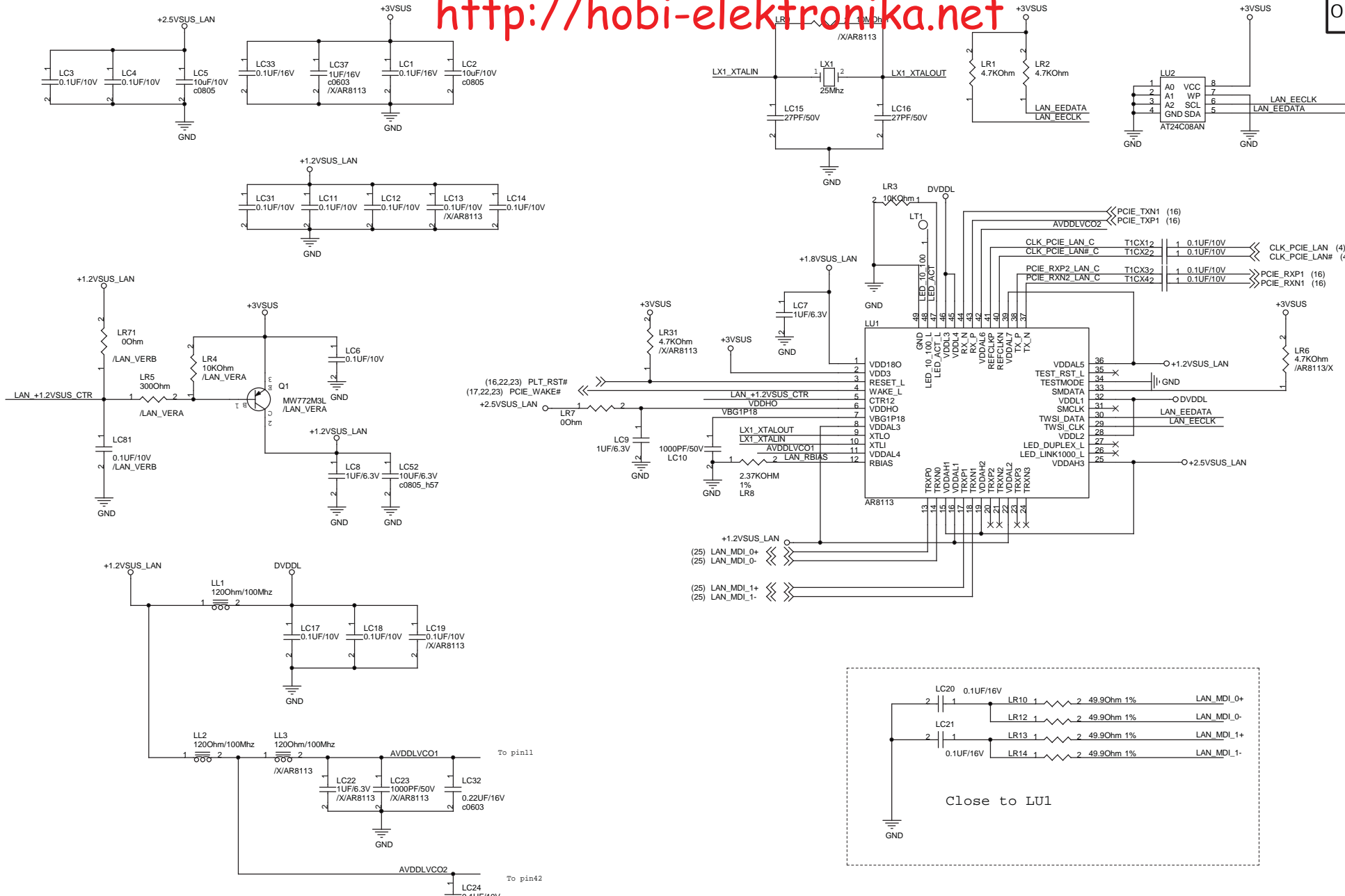


WR19 00hm /X PERST#



-Core Design-

		Title : Minicard	
ASUSTek Computer INC.		Engineer: Tiansen_Wu	
Size A3	Project Name <b>1000</b>	Rev 1.0G	
Date: Tuesday, August 12, 2008		Sheet	23 of 50



if overclocking LL3 Kept and LL2 removed  
if not overclocking LL3 removed and LL2 Kept

<Core Design>

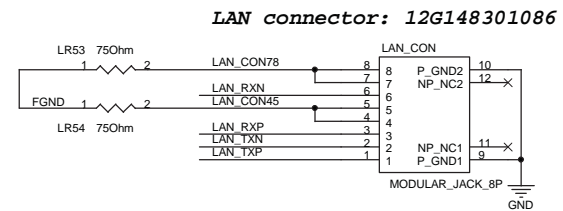
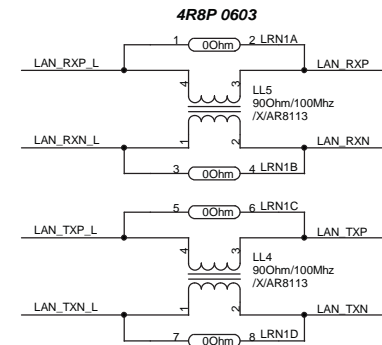
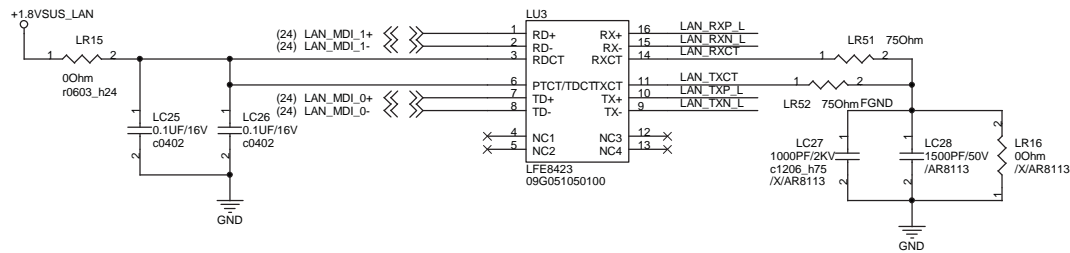
**Title :** AR8113

ASUSTek Computer INC      **Engineer:** Jenen\_wang

Size A3	Project Name <b>1000</b>	Rev 1.0G
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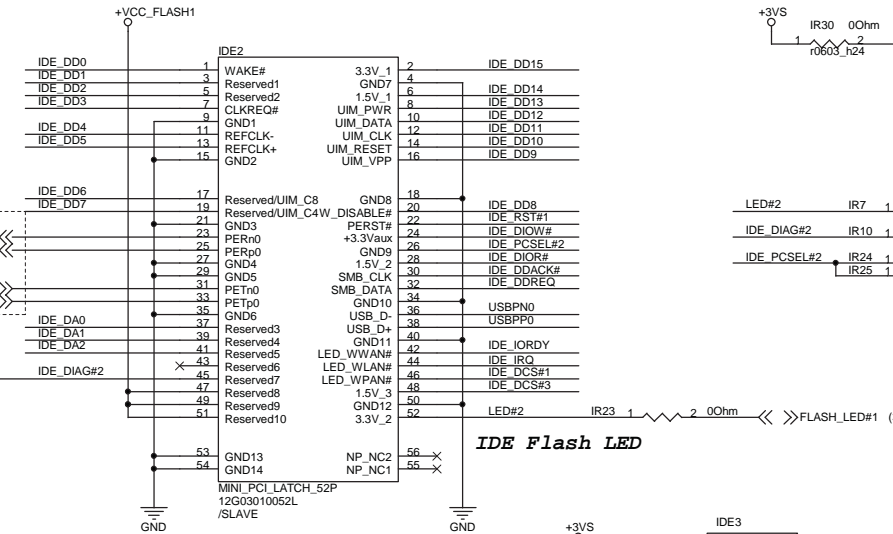
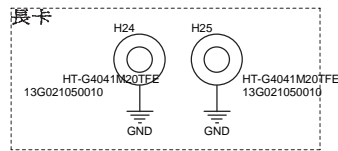
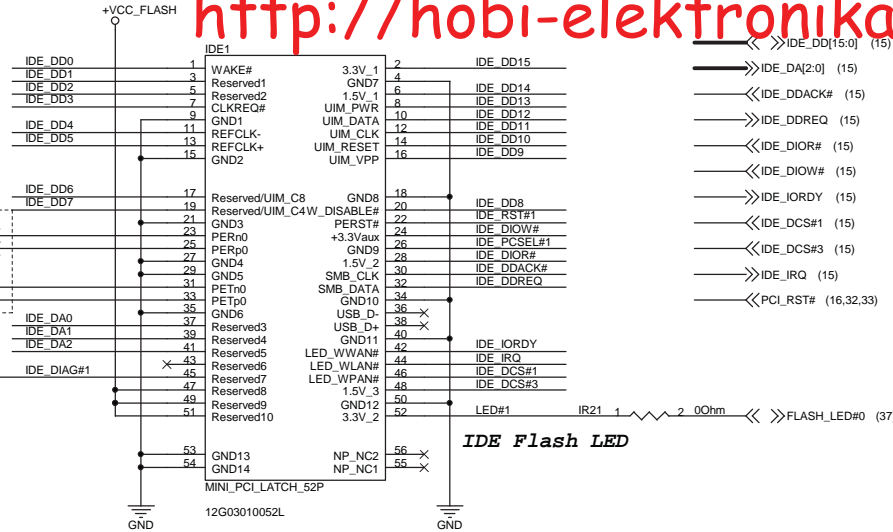
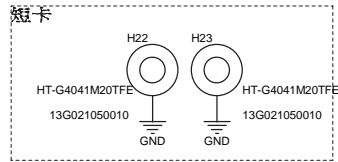
Date: Tuesday, August 12, 2008      Sheet 24 of 50



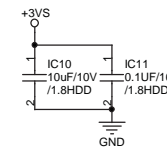
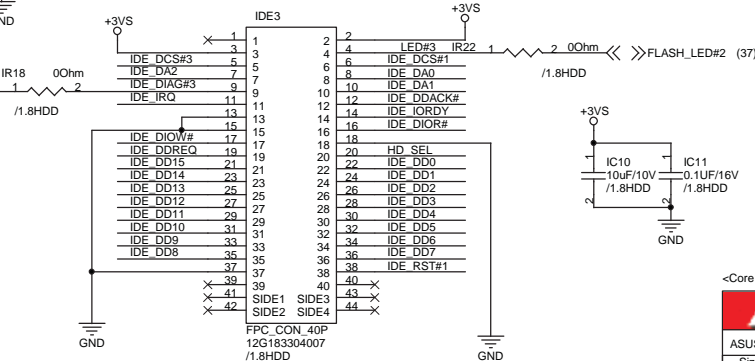
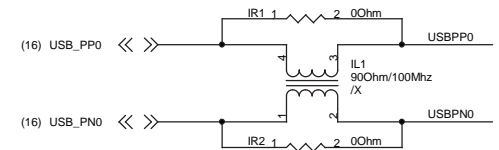
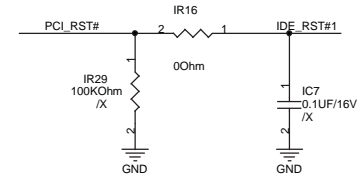
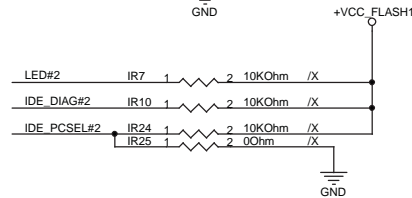
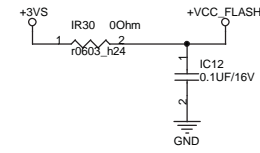
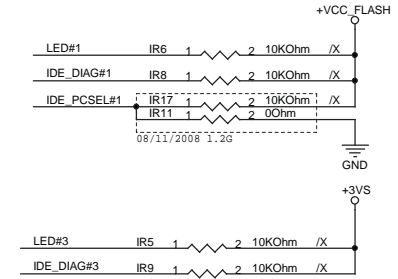
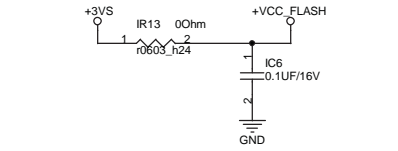
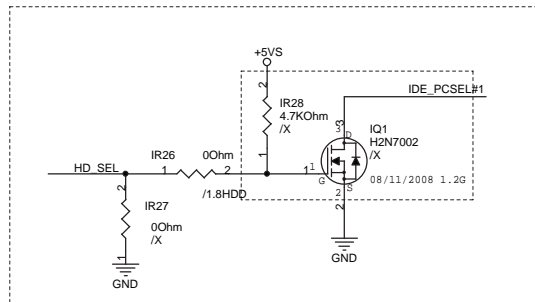


<Core Design>

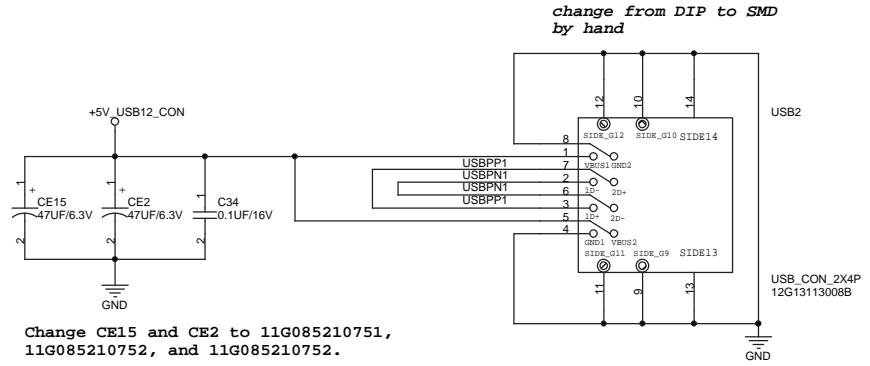
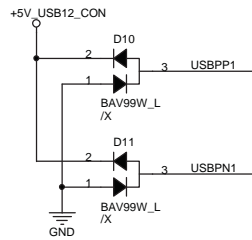
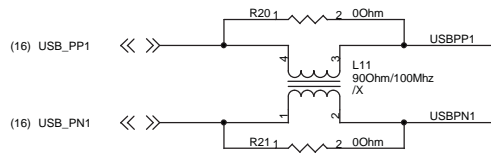
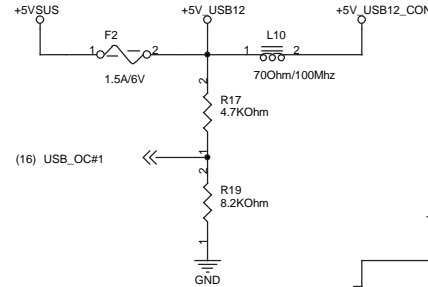
		<b>Title : MDC_RJ11_RJ45</b>	
ASUSTek Computer INC.		Engineer: <b>Kell_Huang</b>	
Size	Project Name	Rev	
A3	<b>1000</b>	1.0G	
Date: Tuesday, August 12, 2008		Sheet 25 of 47	



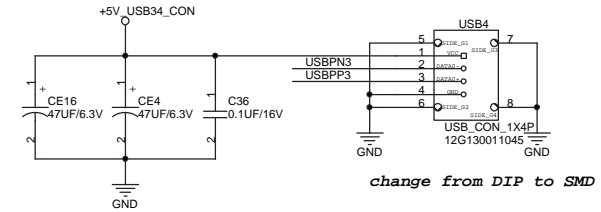
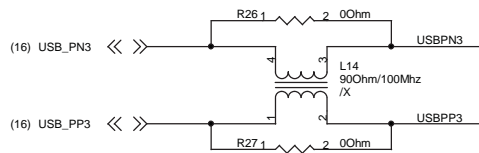
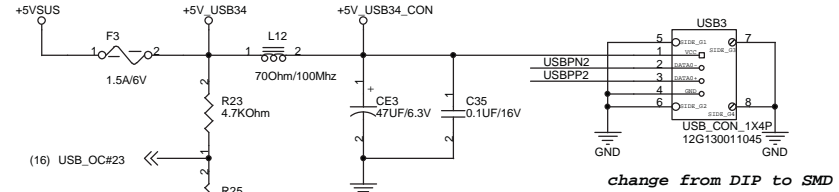
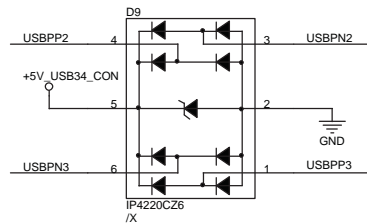
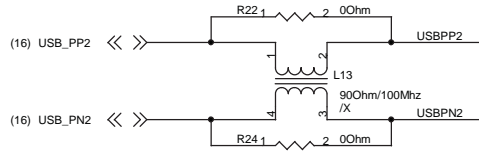
**HD Master/Slave:**  
**Master:Low**  
**Slave :NC or High**  
**Default :High**



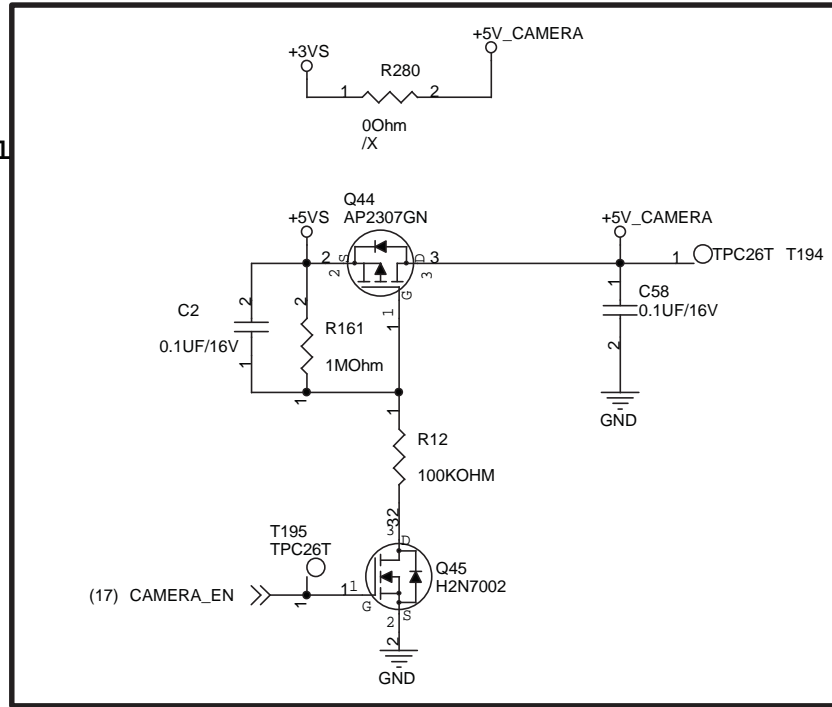
**Naming Rule:**  
**IC: IU?**  
**R: IR?**  
**C: IC?**  
**L: IL?**



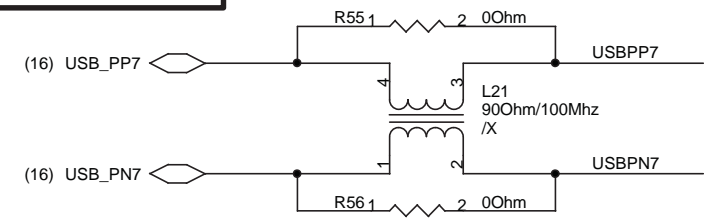
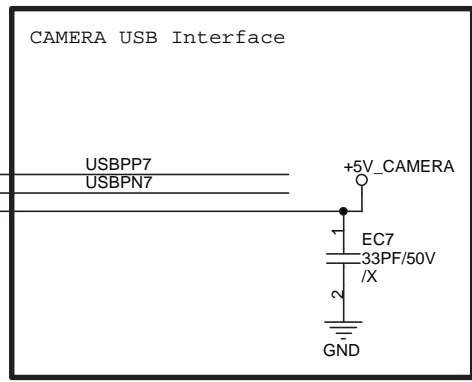
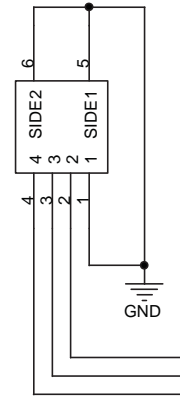
Change CE15 and CE2 to 11G085210751, 11G085210752, and 11G085210752.



Power Control

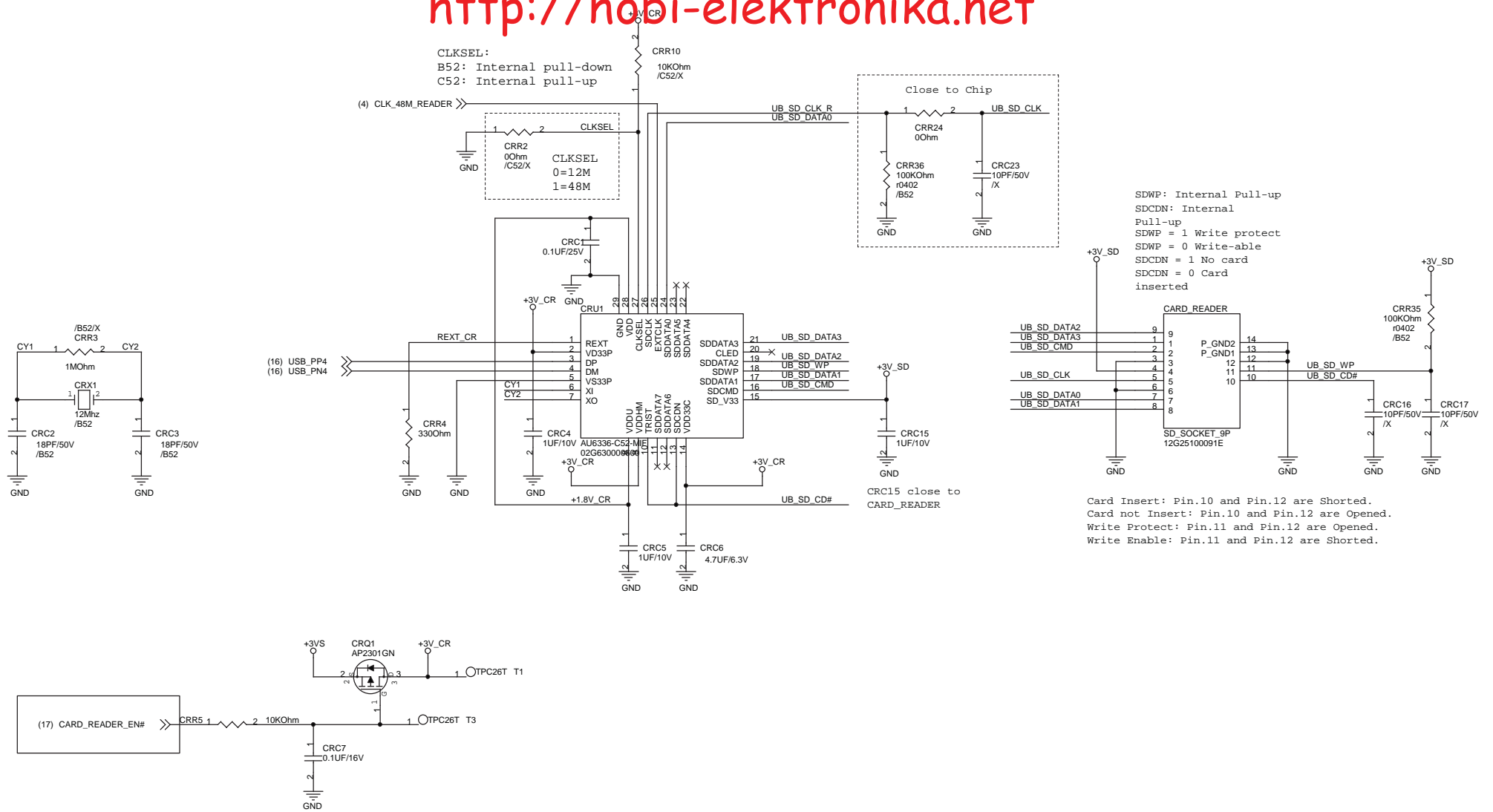


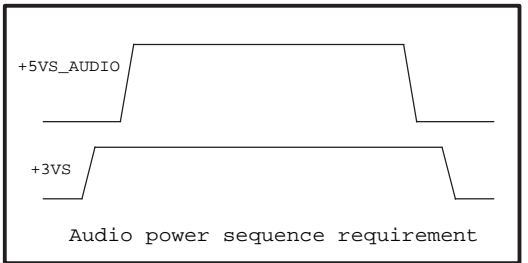
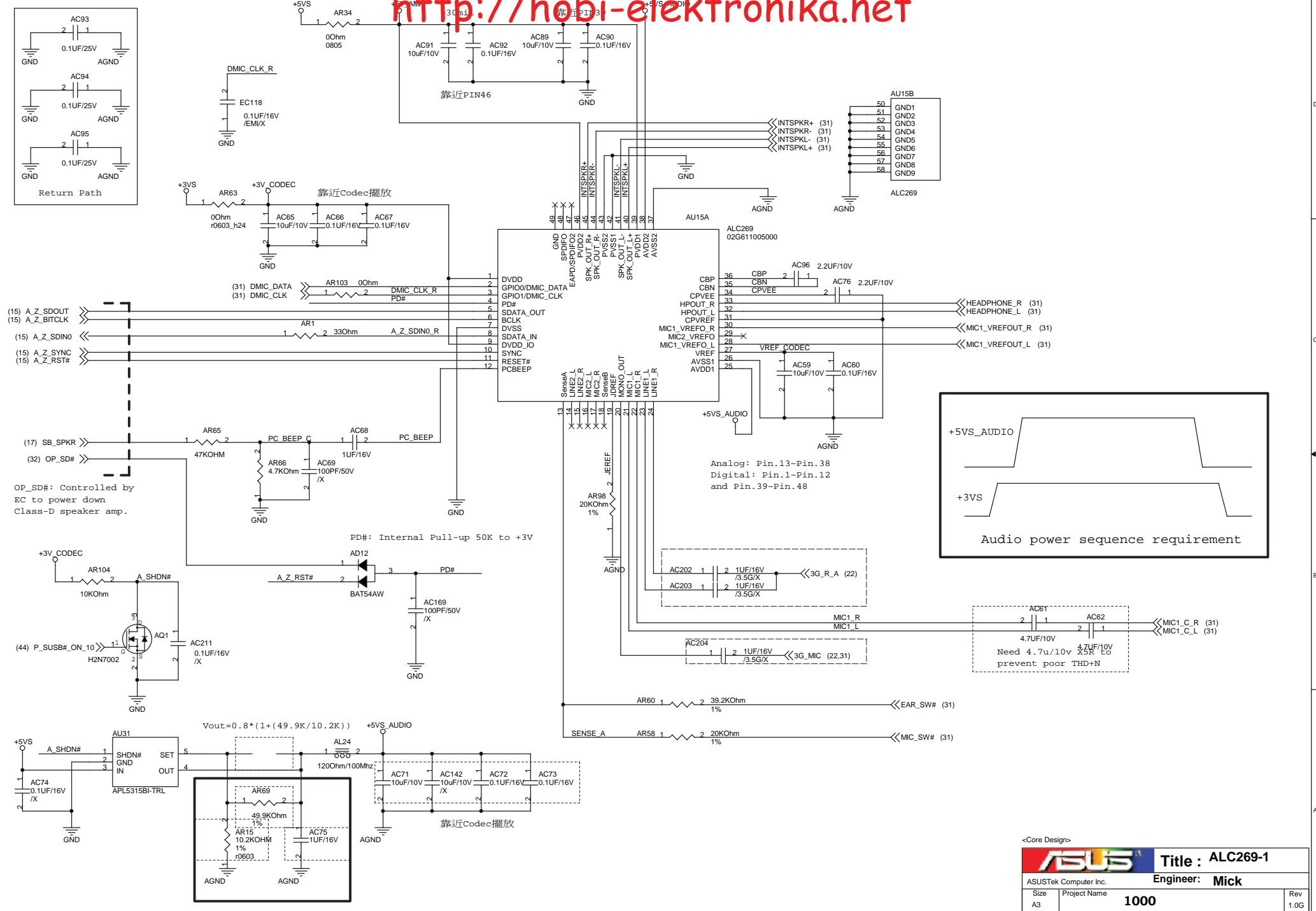
CAMERA  
WtoB\_CON\_4P



<Core Design>

		<b>Title : Camera Power</b>	
ASUSTek Computer INC.		<b>Engineer: Kell_Huang</b>	
Size A4	Project Name <b>1000</b>	Rev 1.0G	
Date: Tuesday, August 12, 2008		Sheet 28 of 47	



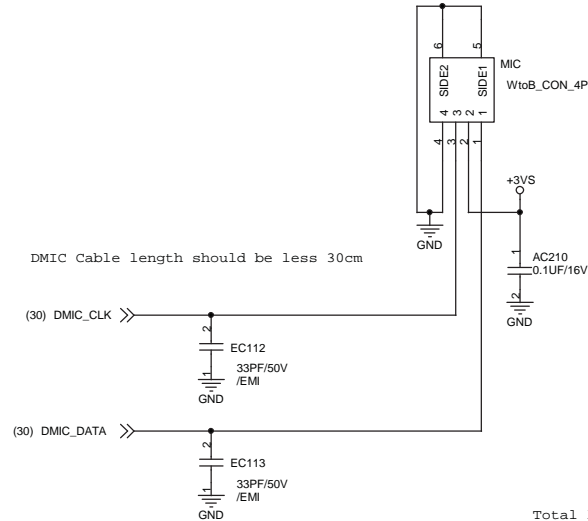


Analog: Pin.13~Pin.38  
Digital: Pin.1~Pin.12 and Pin.39~Pin.48

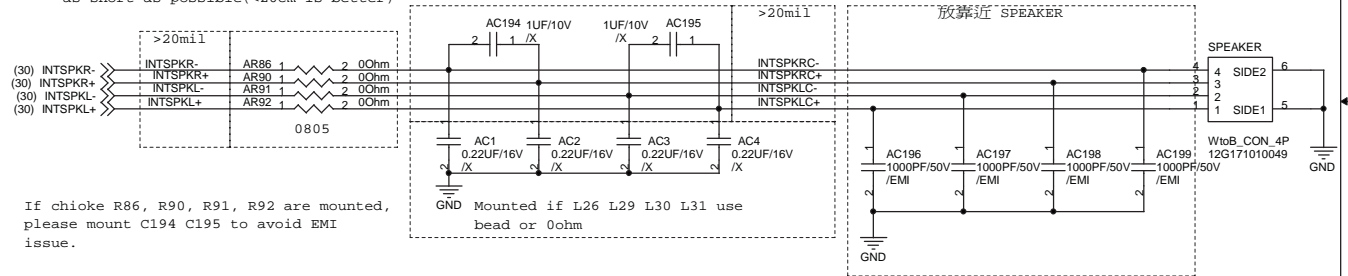
PD#: Internal Pull-up 50K to +3V

AC61 4.7uF/10V  
AC62 2.2uF/10V  
Need 4.7u/10v & 2.2uF/10V prevent poor THD+N

For Audio Noise Issue

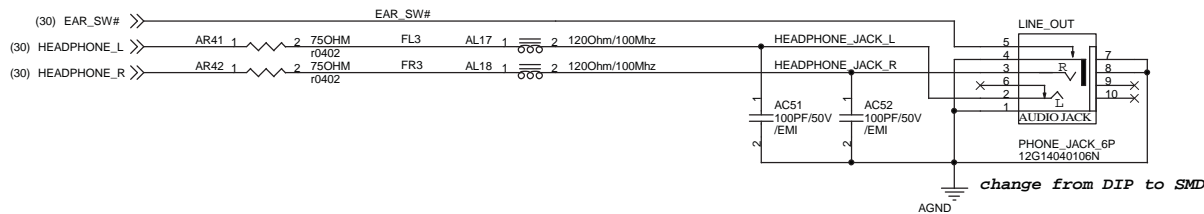


Total length from speakerR+- L+-(pin40 41 44 45) to internal speaker please as short as possible(<20cm is better)

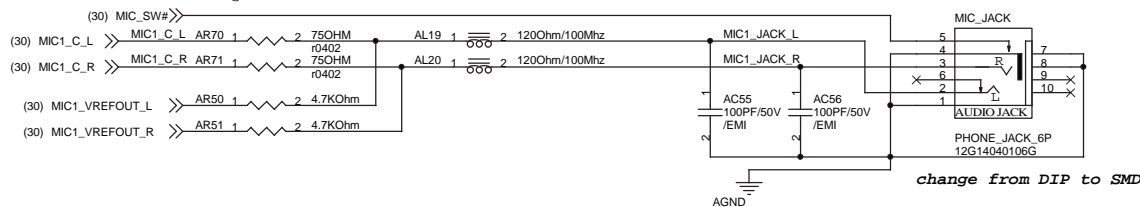


If choke R86, R90, R91, R92 are mounted, please mount C194 C195 to avoid EMI issue.

**LINE\_OUT use 12G14040106N**

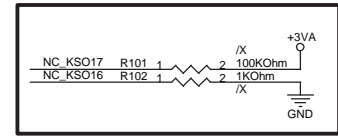
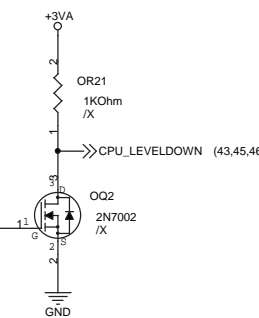
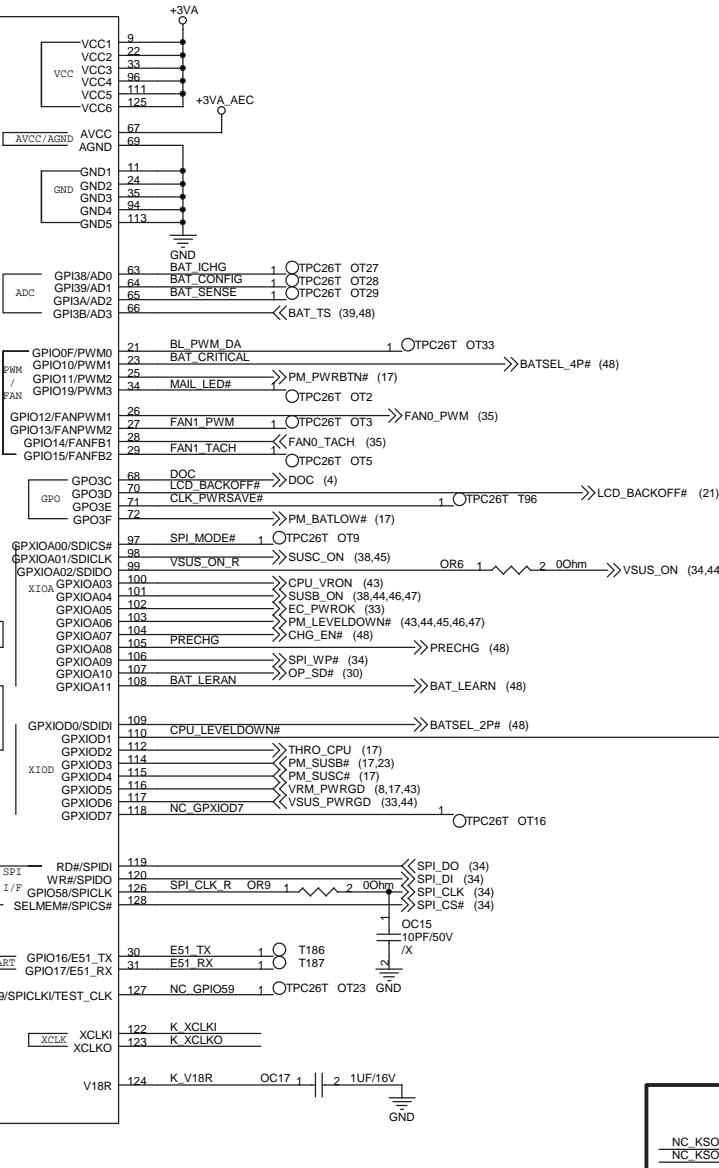
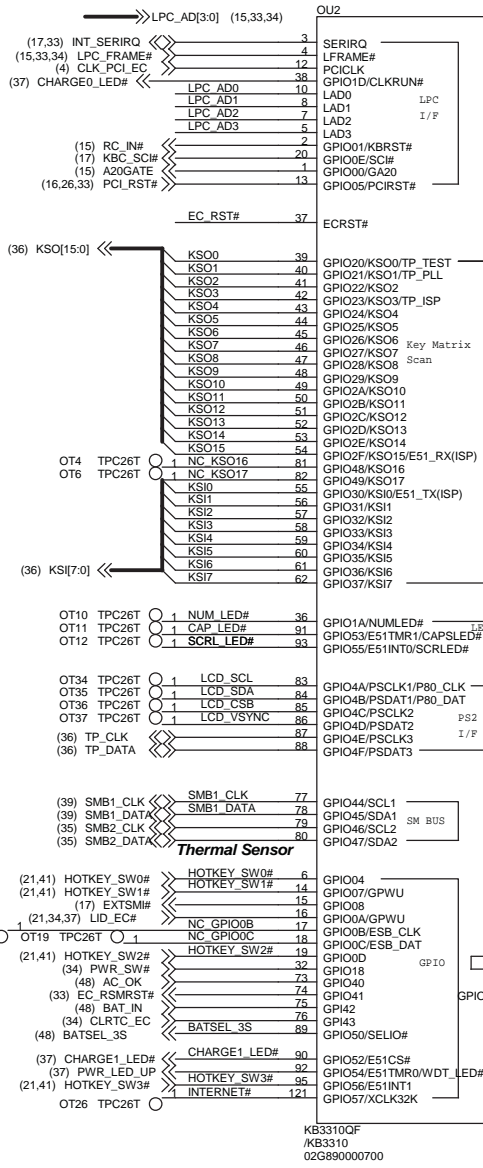
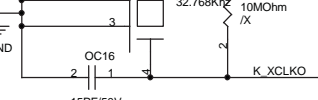
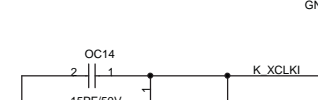
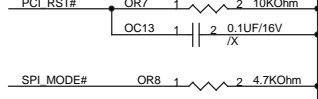
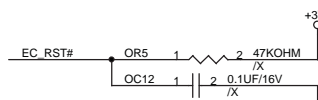
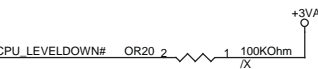
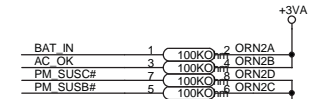
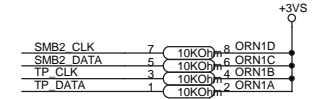
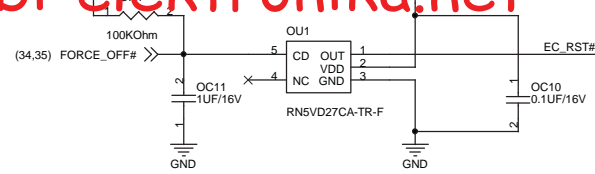
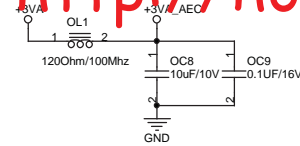
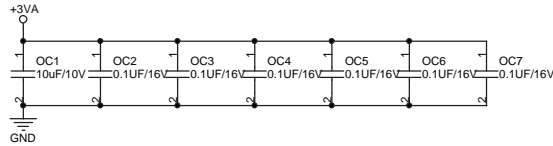


**MIC\_JACK use 12G14040106G**



<Core Design>

<b>ASUS</b>		<b>Title : ALC269-2</b>	
ASUSTek Computer Inc.		Engineer: MICK	
Size A3	Project Name <b>1000</b>	Rev 1.0G	
Date: Tuesday, August 12, 2008		Sheet	31 of 50



ASUS logo and title information: Title: EC\_ENE KB3310, Engineer: Kell Huang, Date: Tuesday, August 12, 2008, Sheet 32 of 50.

Vertical coordinate labels: D, C, B, A

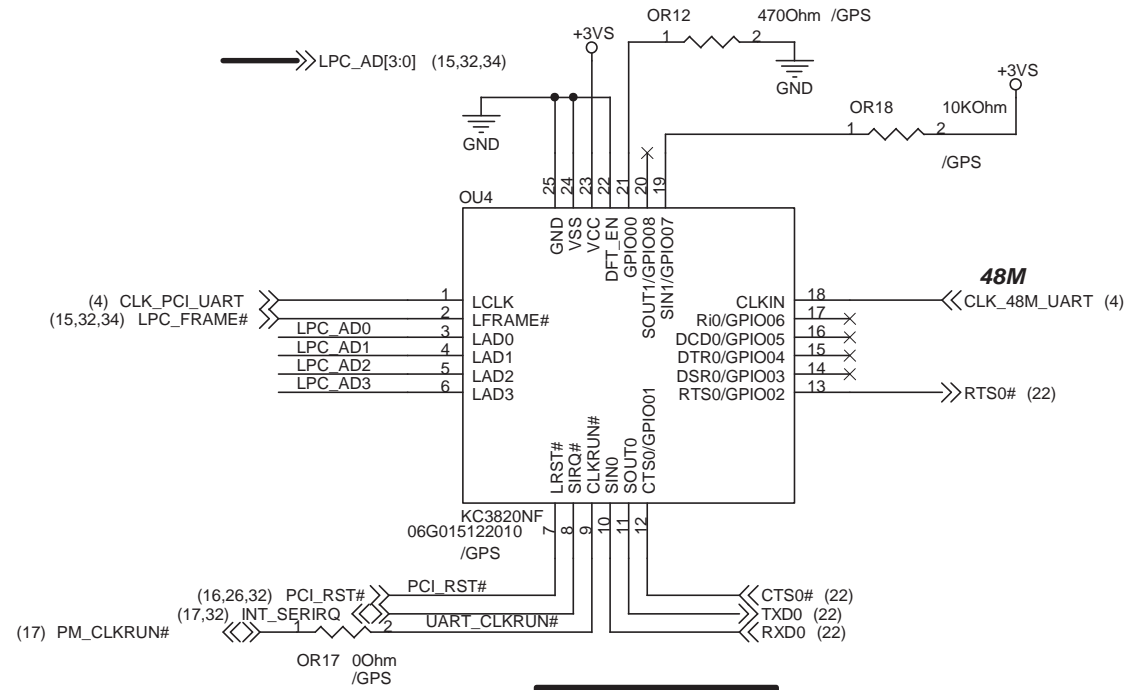
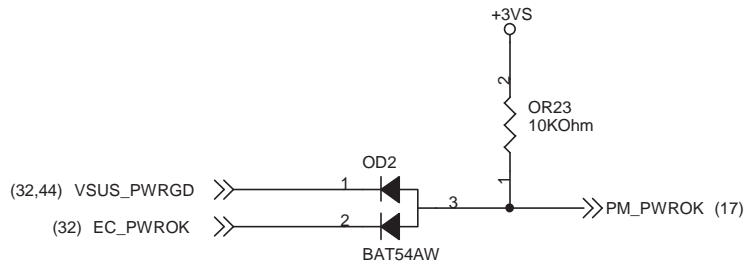
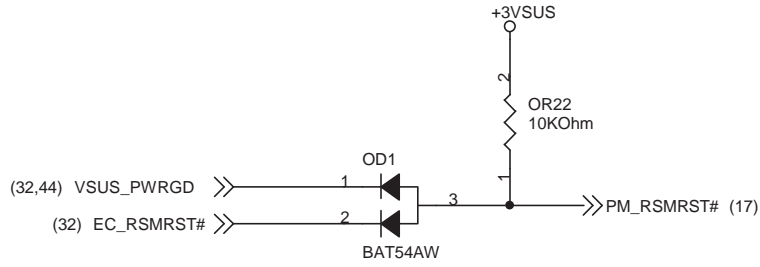
Vertical coordinate labels: D, C, B, A

Horizontal coordinate labels: 5, 4, 3, 2, 1

Horizontal coordinate labels: 5, 4, 3, 2, 1

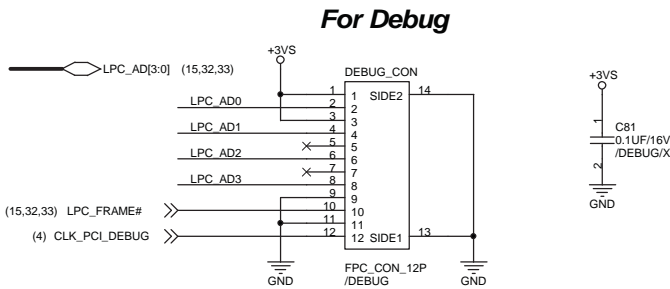
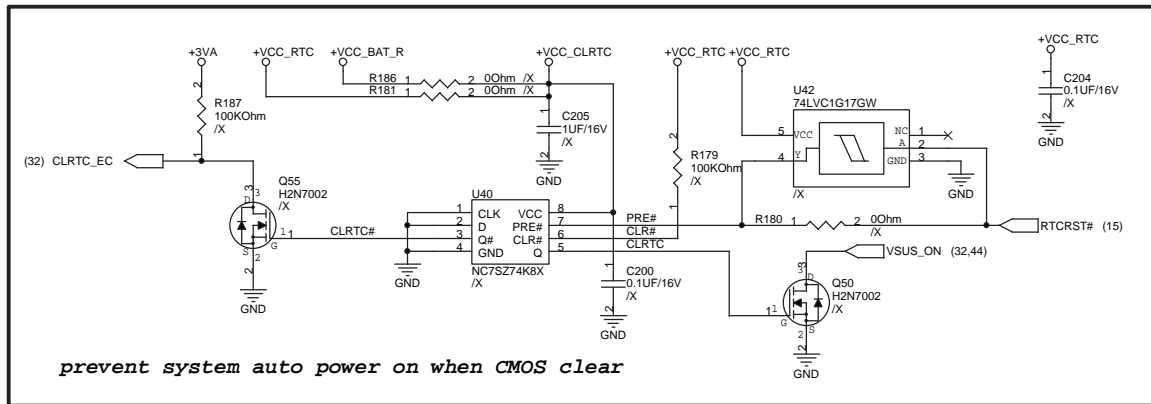
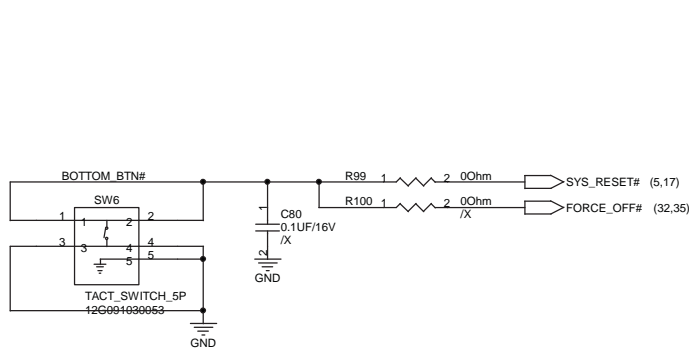
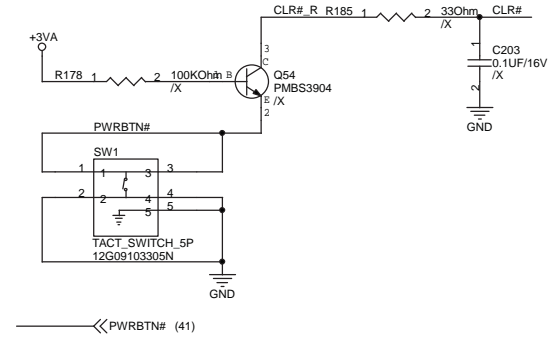
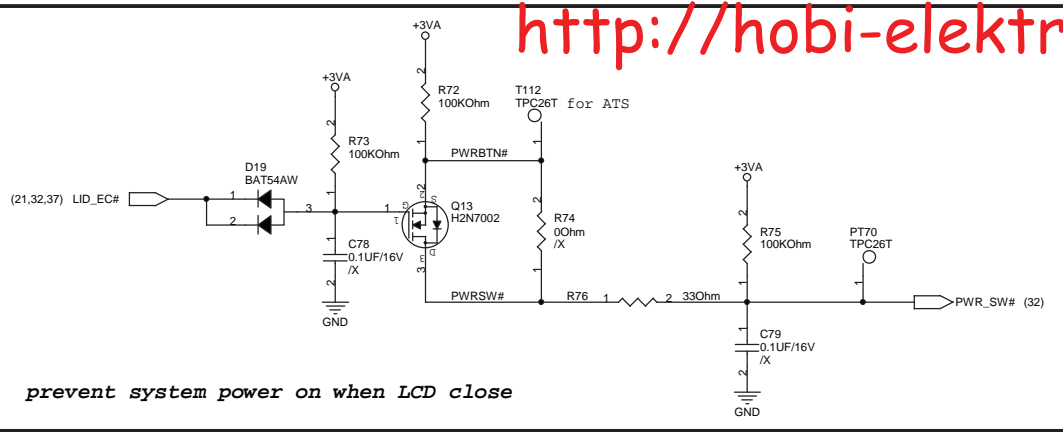


**GPIO00**  
**Hardware strap(internal pull-high)**  
**Low:4E 4F**  
**High:2E 2F**

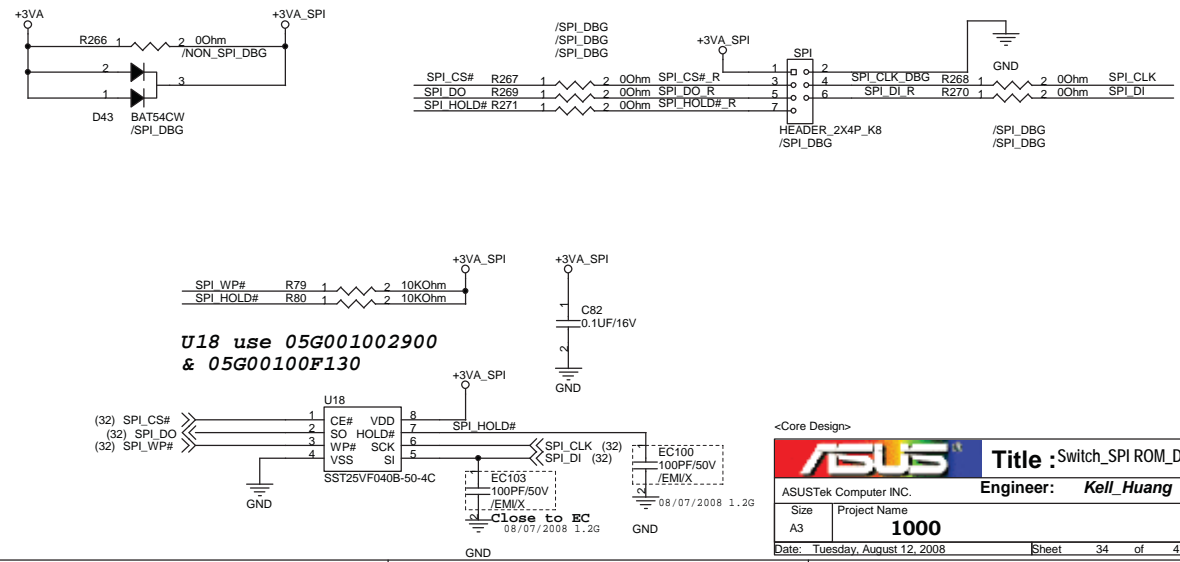


**UART Control**  
**IC for using**  
**GPS module due**  
**to no UART on**  
**ENE EC**

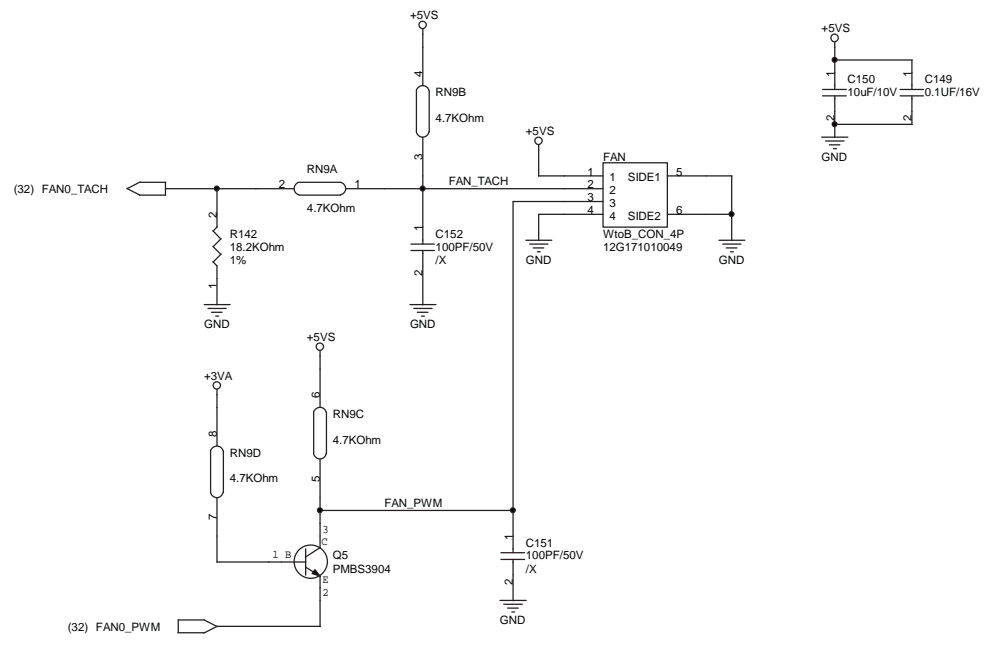
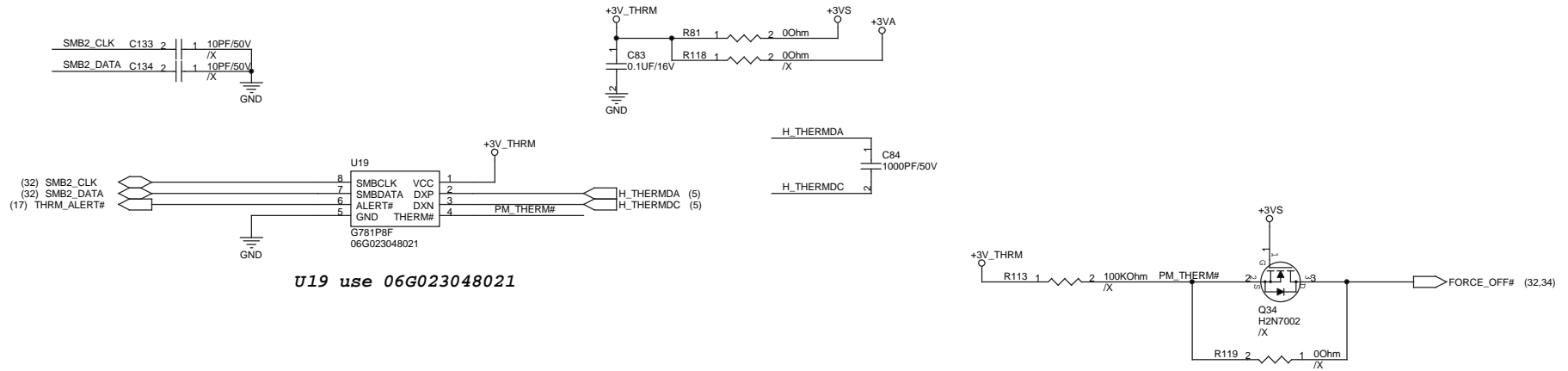
<Core Design>



Debug Card cable use Z96 Touch Pad cable, P/N:  
 14G124110126, 14G124110120, 14G124110121  
 14G124110124, 14G124110125

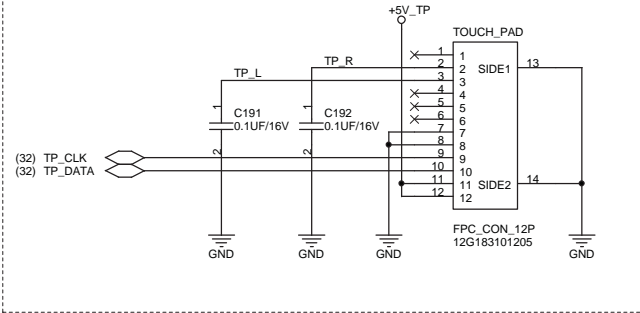


ASUS		Title : Switch_SPI ROM_Debug	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size	Project Name		Rev
A3	1000		1.0G
Date: Tuesday, August 12, 2008		Sheet	34 of 47

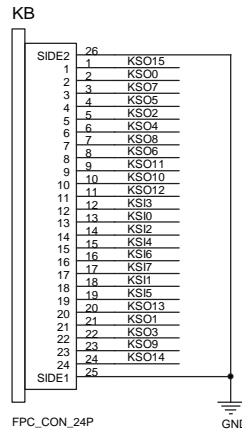


**For Touch-Pad**

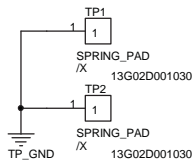
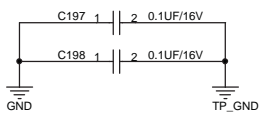
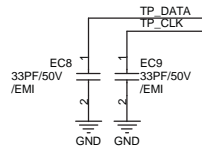
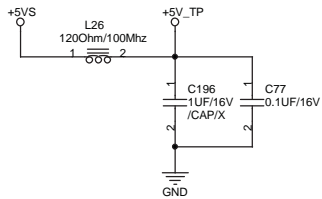
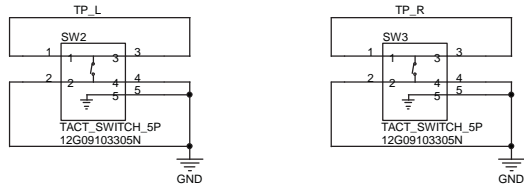
P900 R1.0G



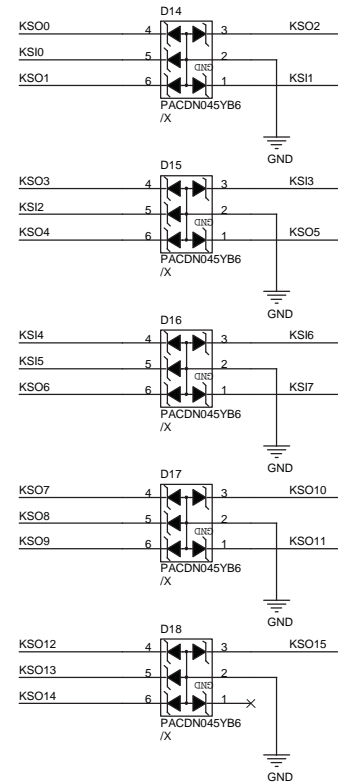
**For Keyboard Connector**



SW2, SW3 use 12G09103305N



KSO[15:0] (32)  
KSI[7:0] (32)

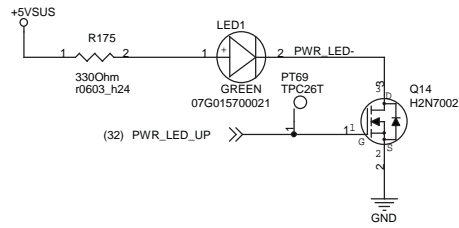


KSI0	EC10	1	2	33PF/50V
				/X
KSI1	EC11	1	2	33PF/50V
				/X
KSI2	EC12	1	2	33PF/50V
				/X
KSI3	EC13	1	2	33PF/50V
				/X
KSI4	EC14	1	2	33PF/50V
				/X
KSI5	EC15	1	2	33PF/50V
				/X
KSI6	EC16	1	2	33PF/50V
				/X
KSI7	EC17	1	2	33PF/50V
				/X
KSO0	EC18	1	2	33PF/50V
				/X
KSO1	EC19	1	2	33PF/50V
				/X
KSO2	EC20	1	2	33PF/50V
				/X
KSO3	EC21	1	2	33PF/50V
				/X
KSO4	EC22	1	2	33PF/50V
				/X
KSO5	EC23	1	2	33PF/50V
				/X
KSO6	EC24	1	2	33PF/50V
				/X
KSO7	EC25	1	2	33PF/50V
				/X
KSO8	EC26	1	2	33PF/50V
				/X
KSO9	EC27	1	2	33PF/50V
				/X
KSO10	EC28	1	2	33PF/50V
				/X
KSO11	EC29	1	2	33PF/50V
				/X
KSO12	EC30	1	2	33PF/50V
				/X
KSO13	EC31	1	2	33PF/50V
				/X
KSO14	EC32	1	2	33PF/50V
				/X
KSO15	EC33	1	2	33PF/50V
				/X

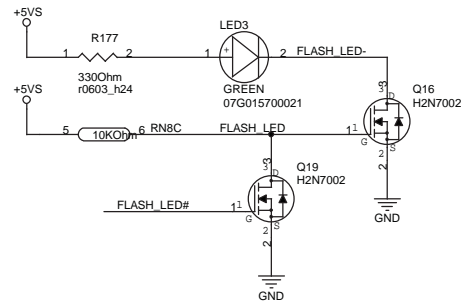
<Core Design>

		<b>Title : KB_Touch Pad</b>	
ASUSTek Computer INC.		Engineer: <b>Kell_Huang</b>	
Size	Project Name		Rev
A3	<b>1000</b>		1.0G
Date: Tuesday, August 12, 2008		Sheet 36 of 47	

**for POWER LED**

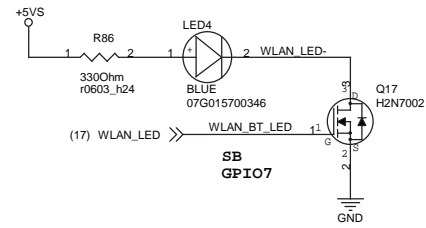


**for FLASH LED**

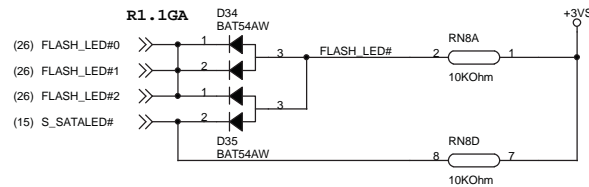
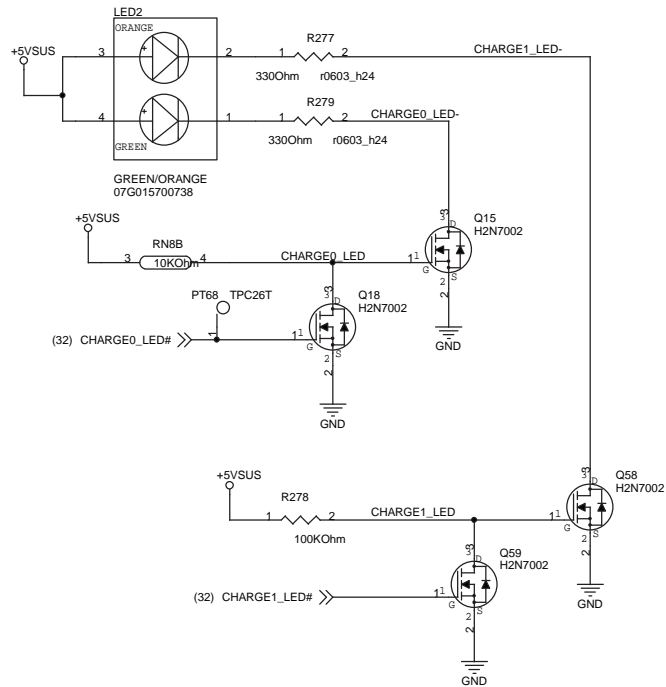


**for WLAN/BlueTooth LED**

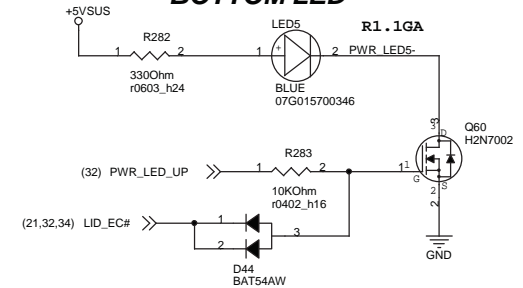
R86 use 4.7K Ohm 10G213472003030

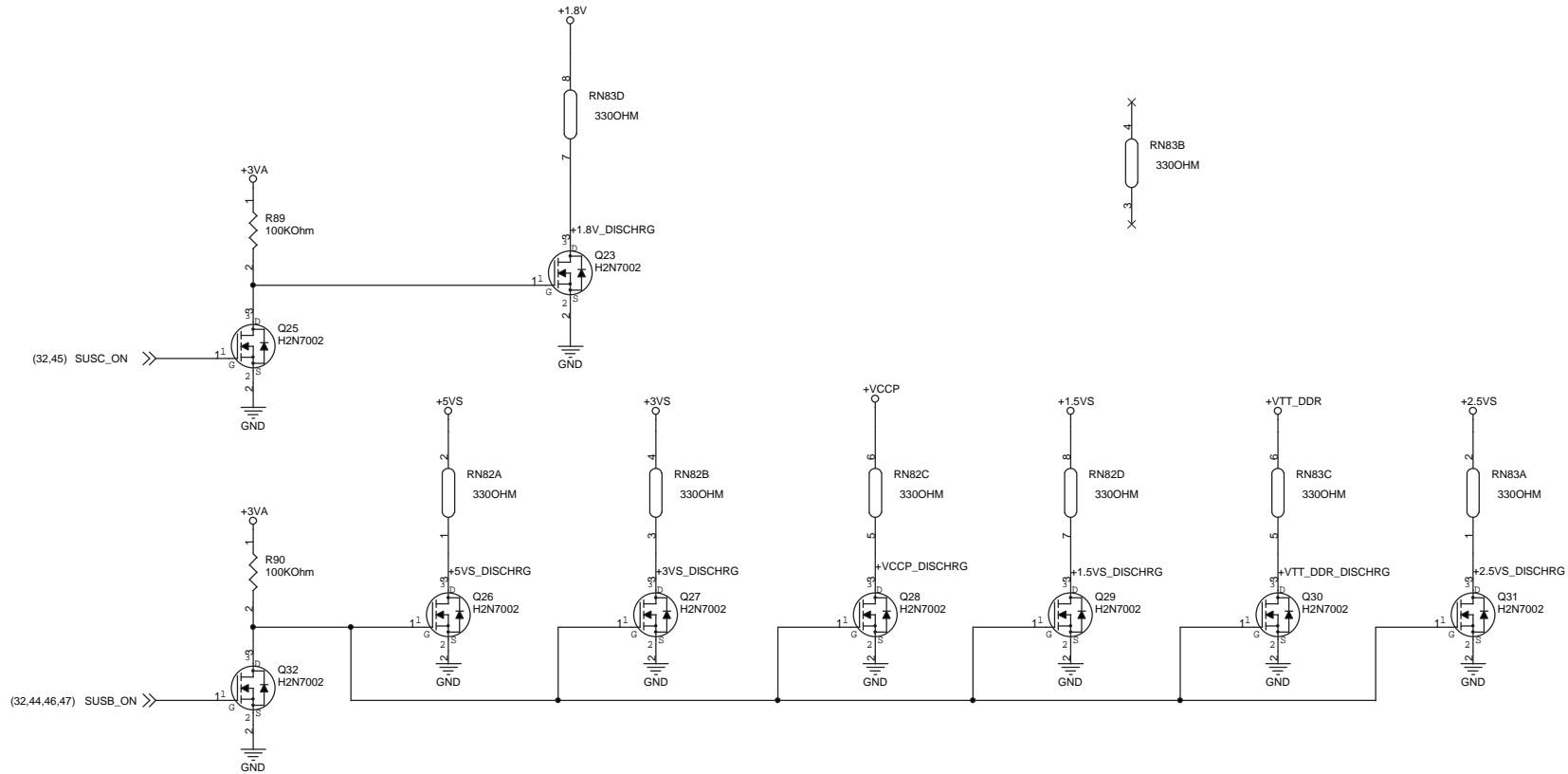


**for CHARGE LED**



**for POWER BOTTOM LED**

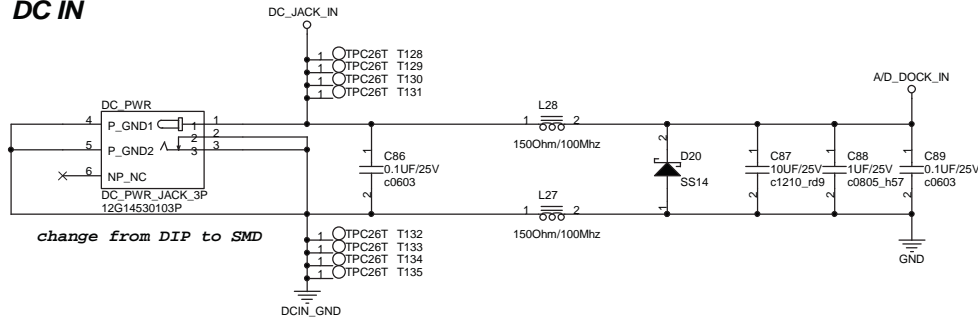




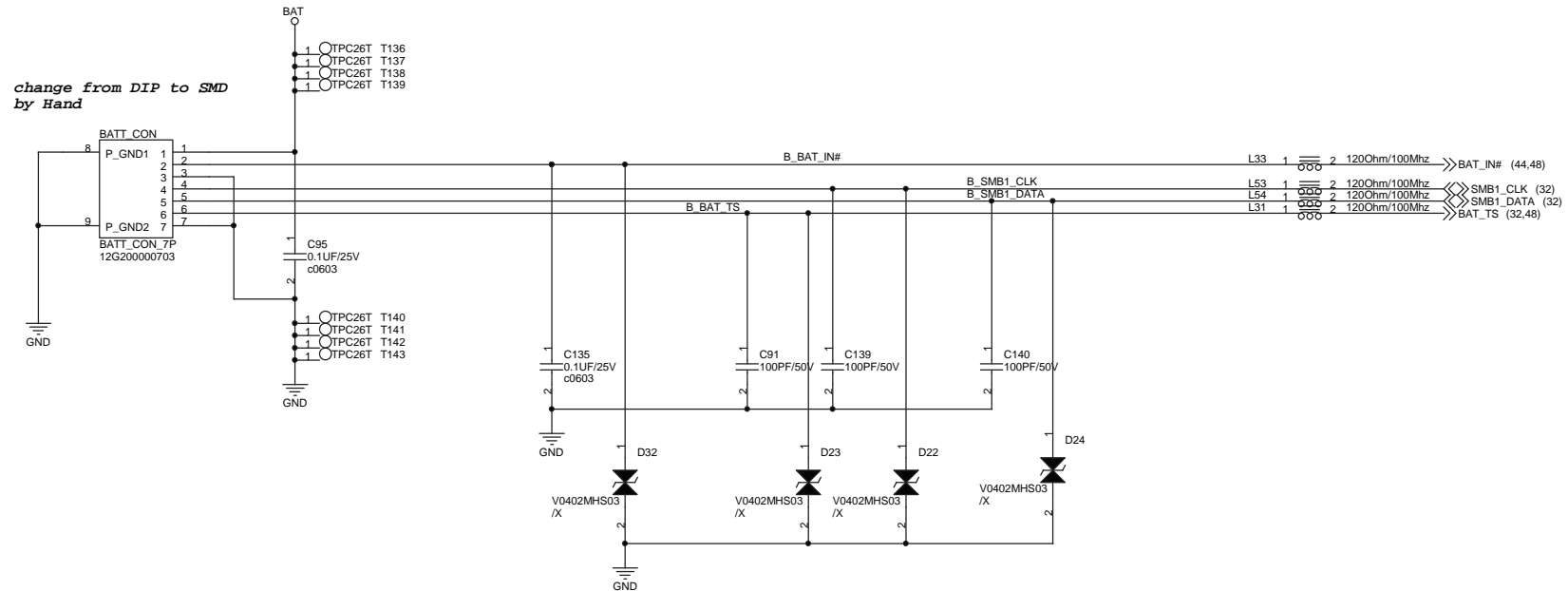
<Core Design>

		Title : Discharge	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size A3	Project Name <b>1000</b>	Rev 1.0G	
Date: Tuesday, August 12, 2008		Sheet 38 of 47	

**DC IN**

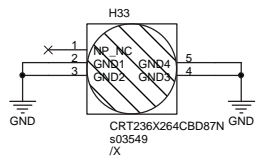
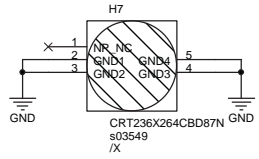
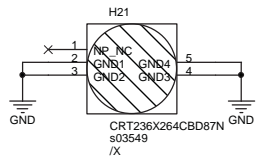
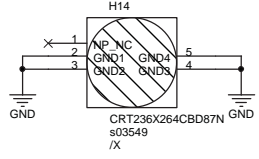
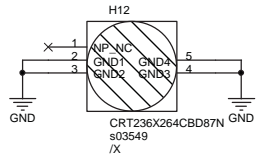
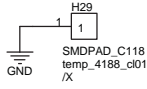
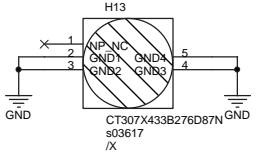
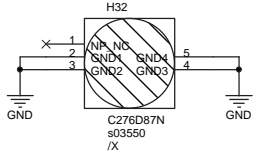
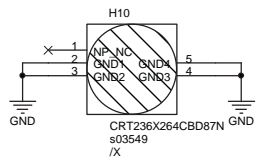
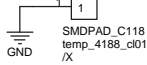
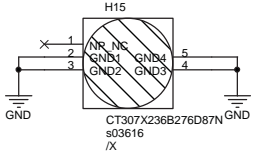
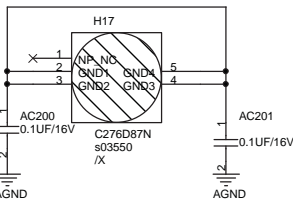
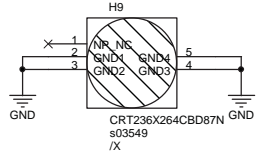
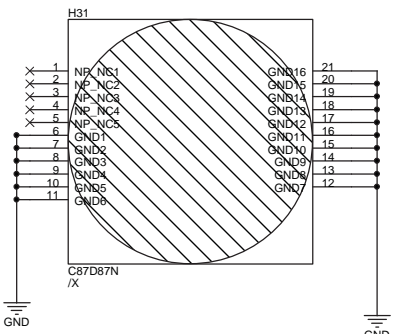
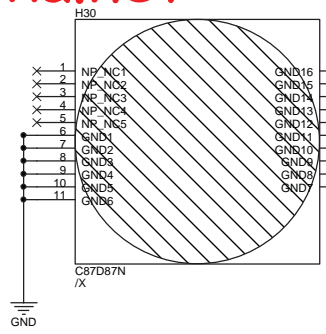
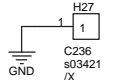
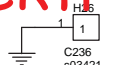
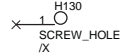
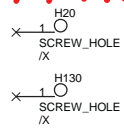
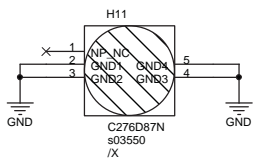
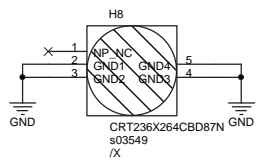


**BAT IN**



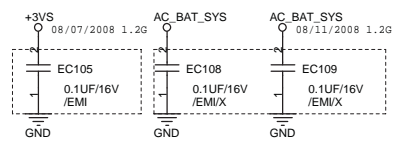
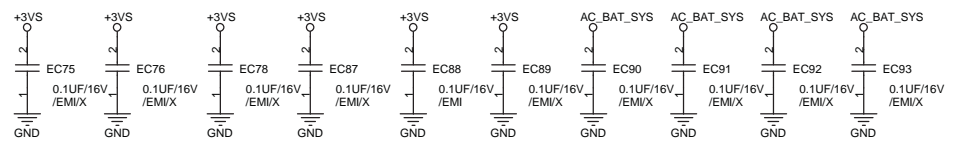
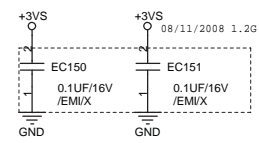
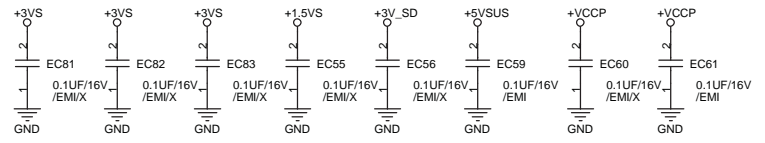
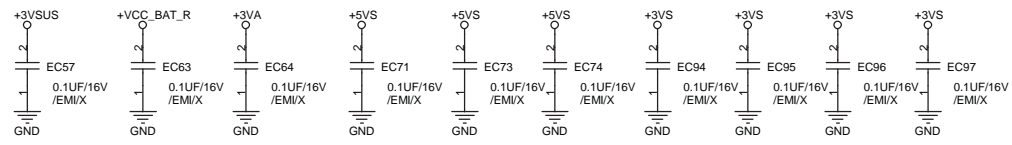
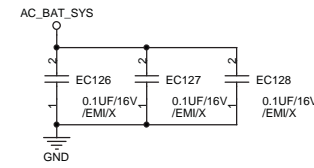
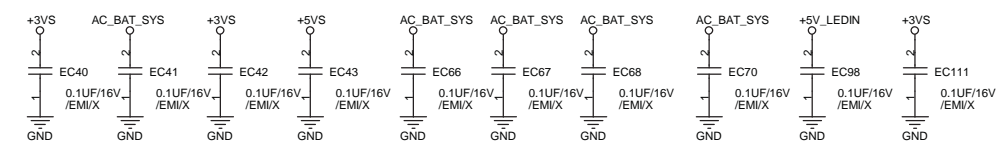
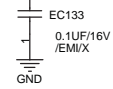
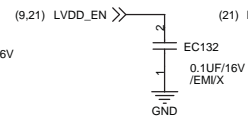
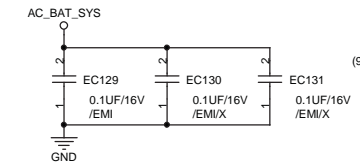
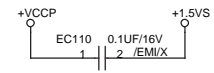
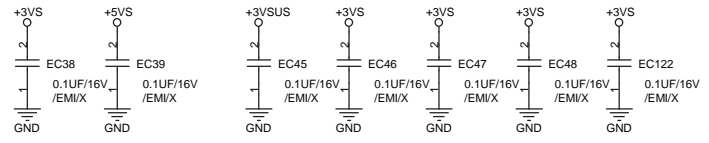
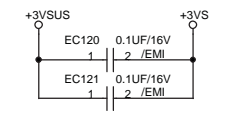
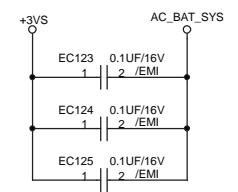
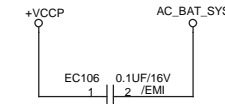
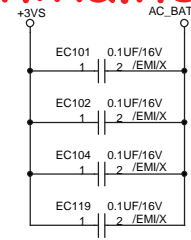
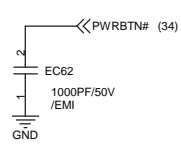
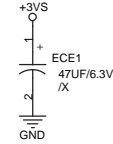
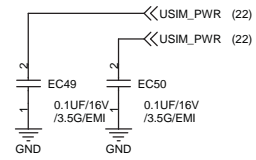
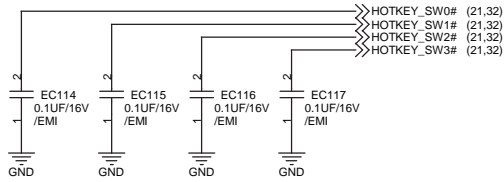
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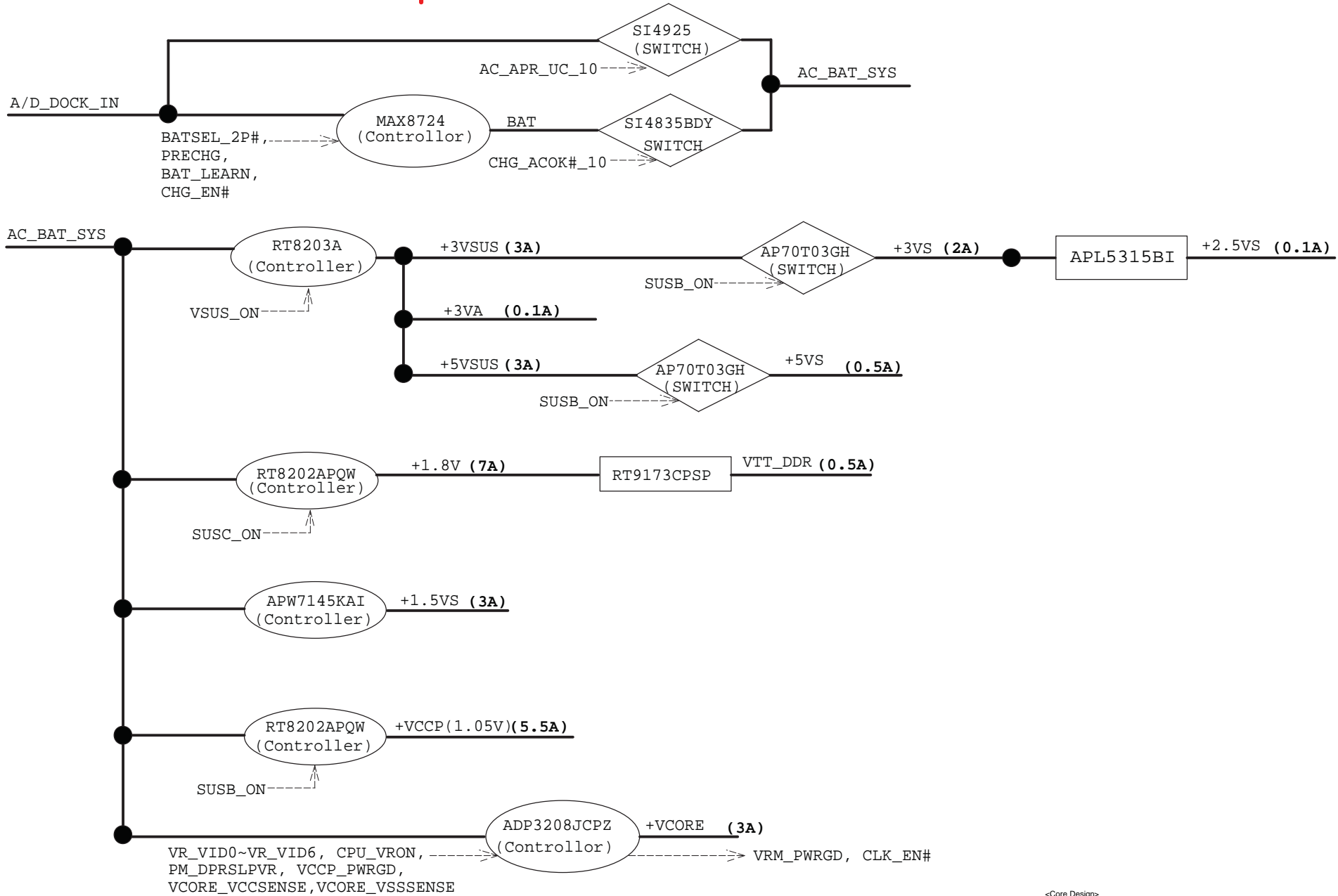
		<b>Title : PWR Jack</b>	
ASUSTek Computer INC.		Engineer: <b>Kell_Huang</b>	
Size A3	Project Name <b>1000</b>	Rev 1.0G	
Date: Tuesday, August 12, 2008		Sheet 39 of 47	

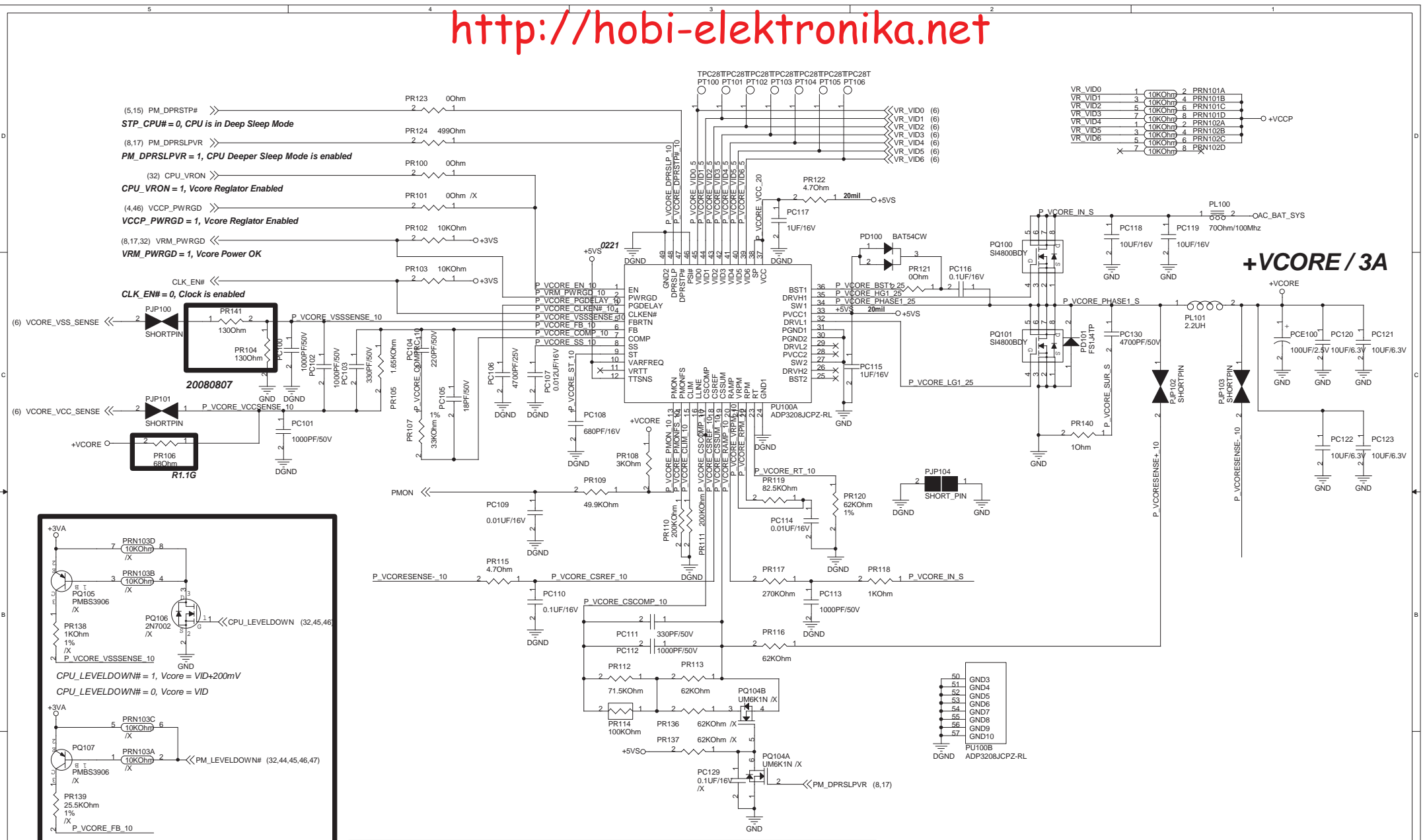




RF CAP :Default Mount



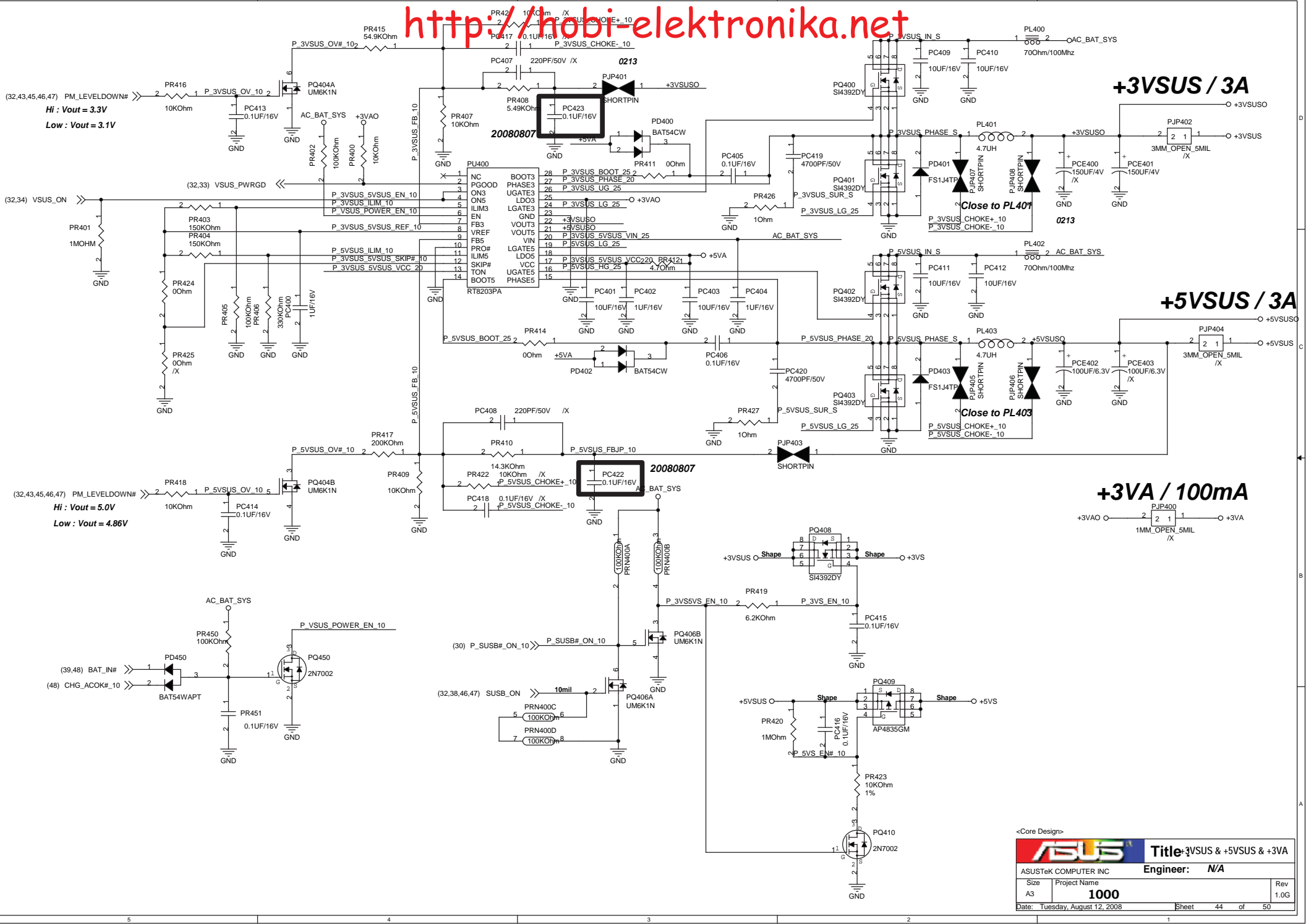


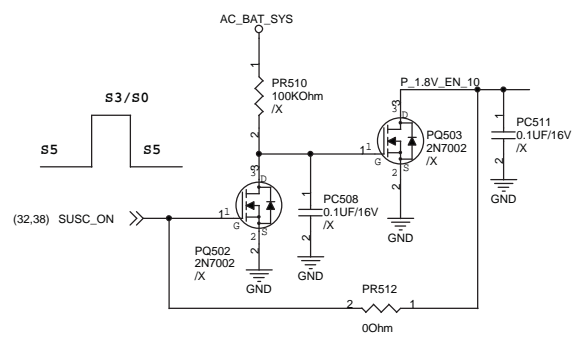
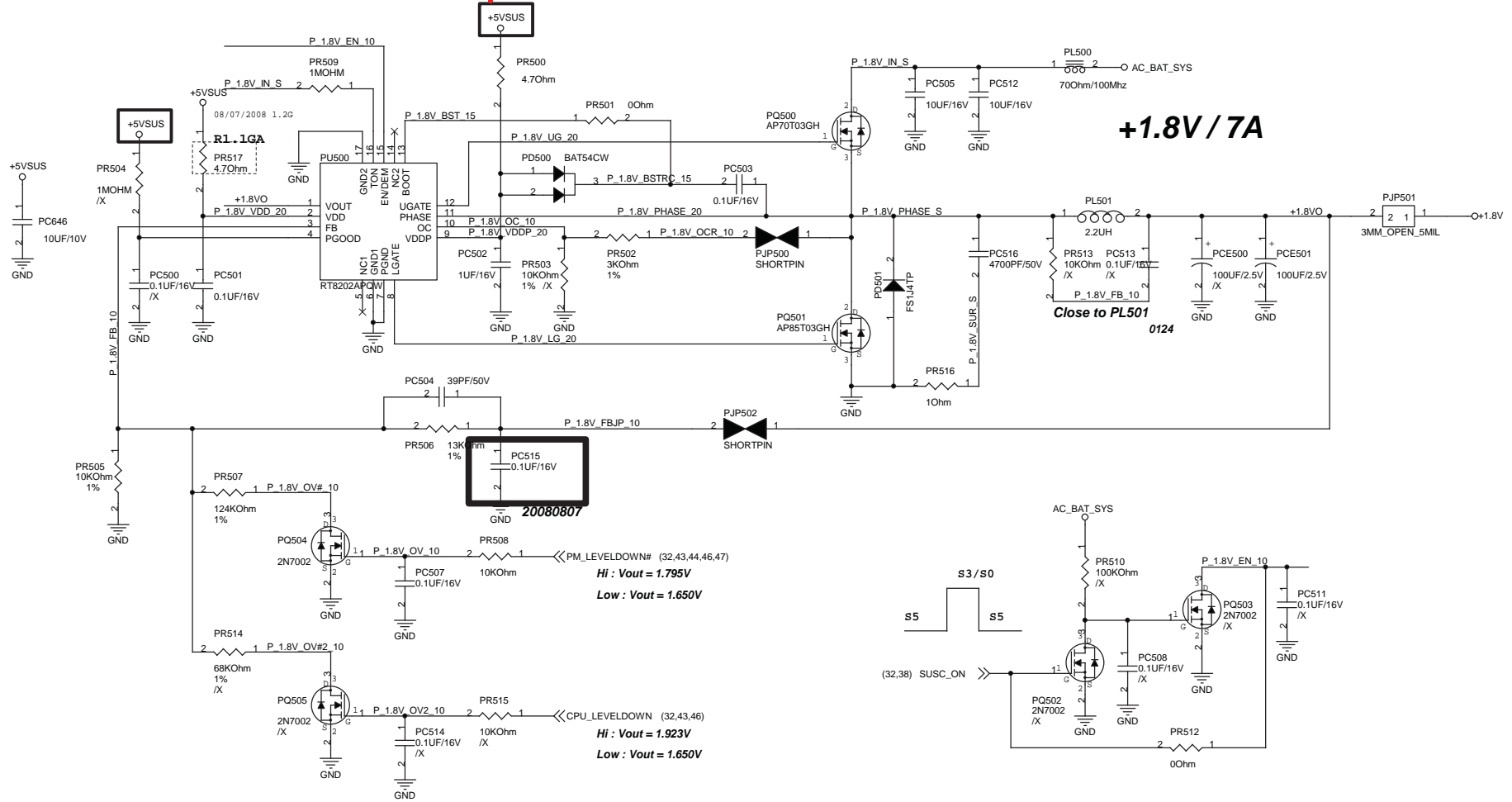


PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	VID-150mV	Power Saving
H	L	H	VID	Normal
H	H	L	VID + 200mV	Performance
L	H	L	VID + 50mV	N/A

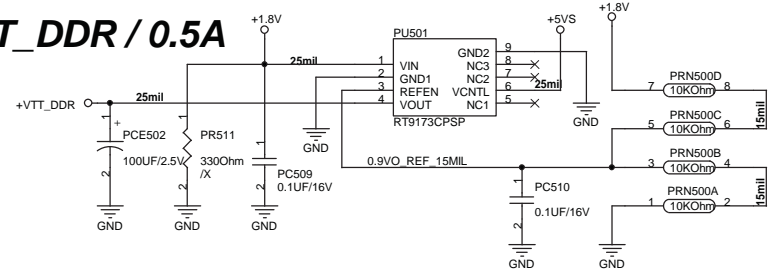
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**Title :** Vcore  
**Engineer:** Joy\_Zhou  
**ASUSTek Computer INC.**  
 Size Project Name  
 Custom **P901** Rev 1.2G  
 Date: Tuesday, August 12, 2008 Sheet 43 of 50

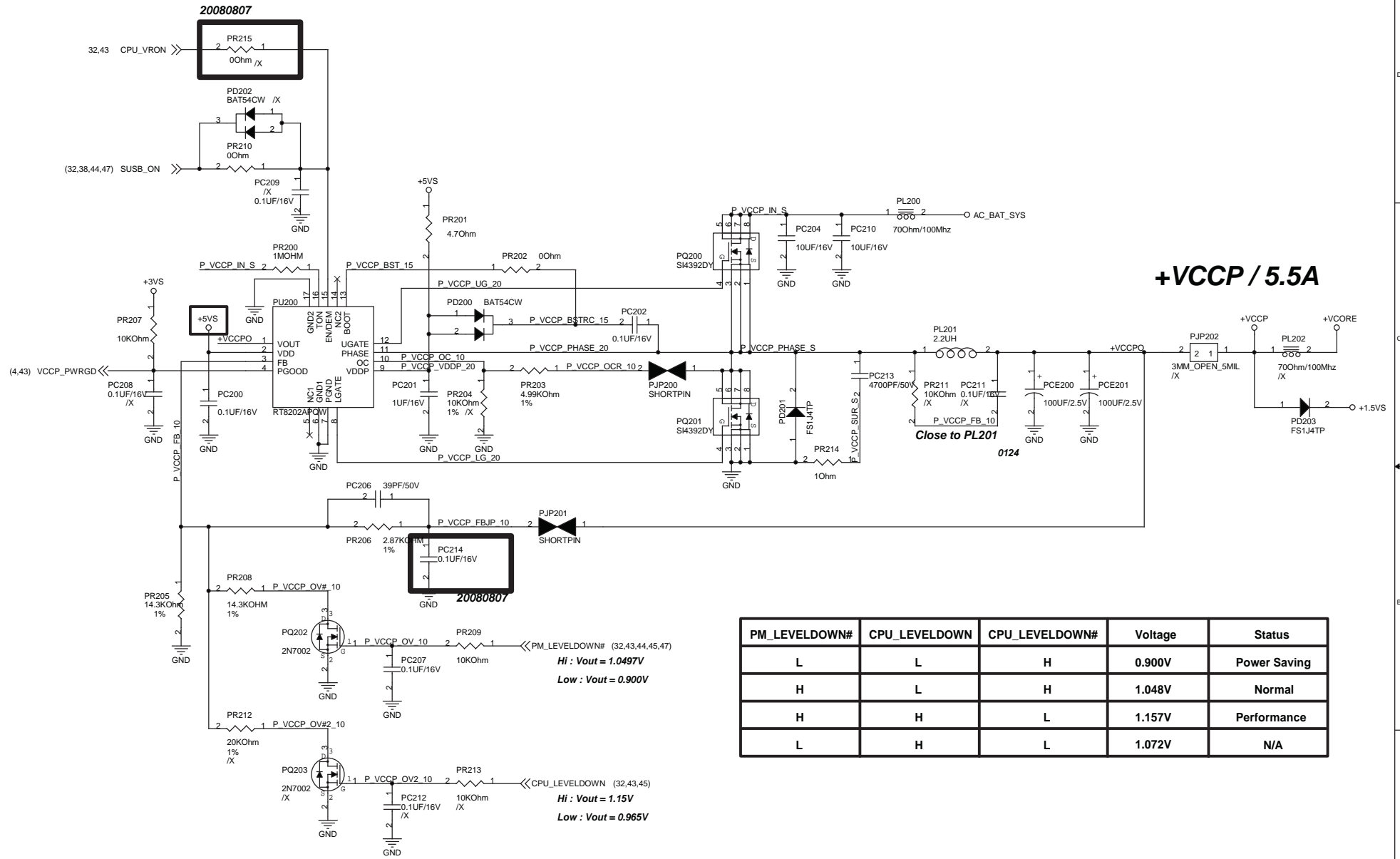




**VTT\_DDR / 0.5A**



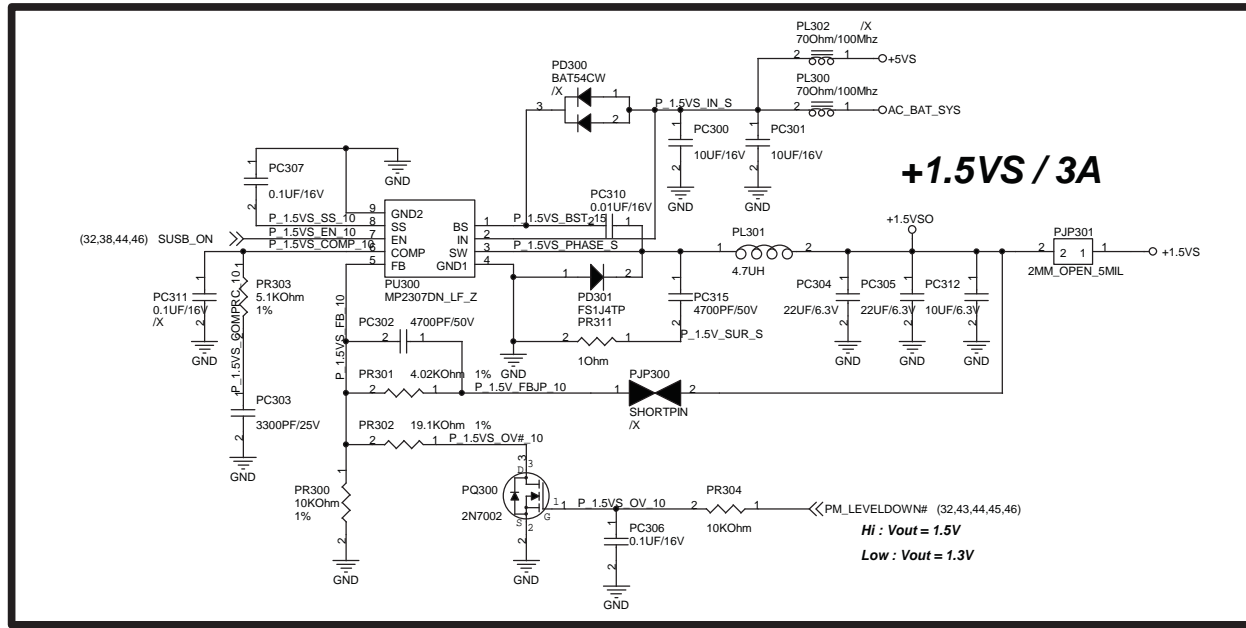
PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	1.720V	Power Saving
H	L	H	1.795V	Normal
H	H	L	1.927V	Performance
L	H	L	1.782V	N/A



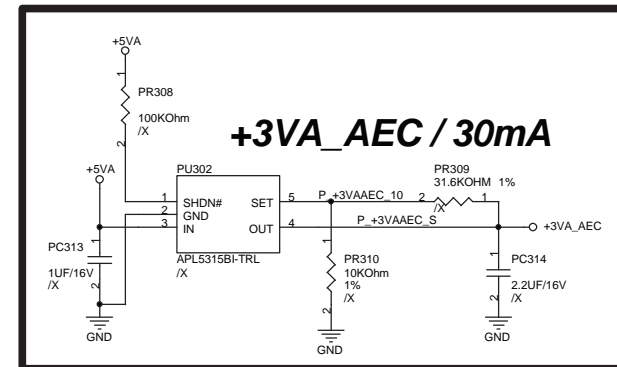
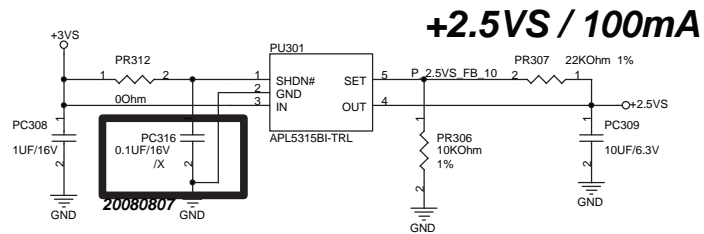
PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	0.900V	Power Saving
H	L	H	1.048V	Normal
H	H	L	1.157V	Performance
L	H	L	1.072V	N/A

<-Core Design>

		<b>Title : VCCP</b>	
ASUSTek Computer INC.		Engineer: <b>Joy_Zhou</b>	
Size A3	Project Name <b>1000</b>	Rev 1.0G	
Date: Tuesday, August 12, 2008		Sheet 46 of 50	

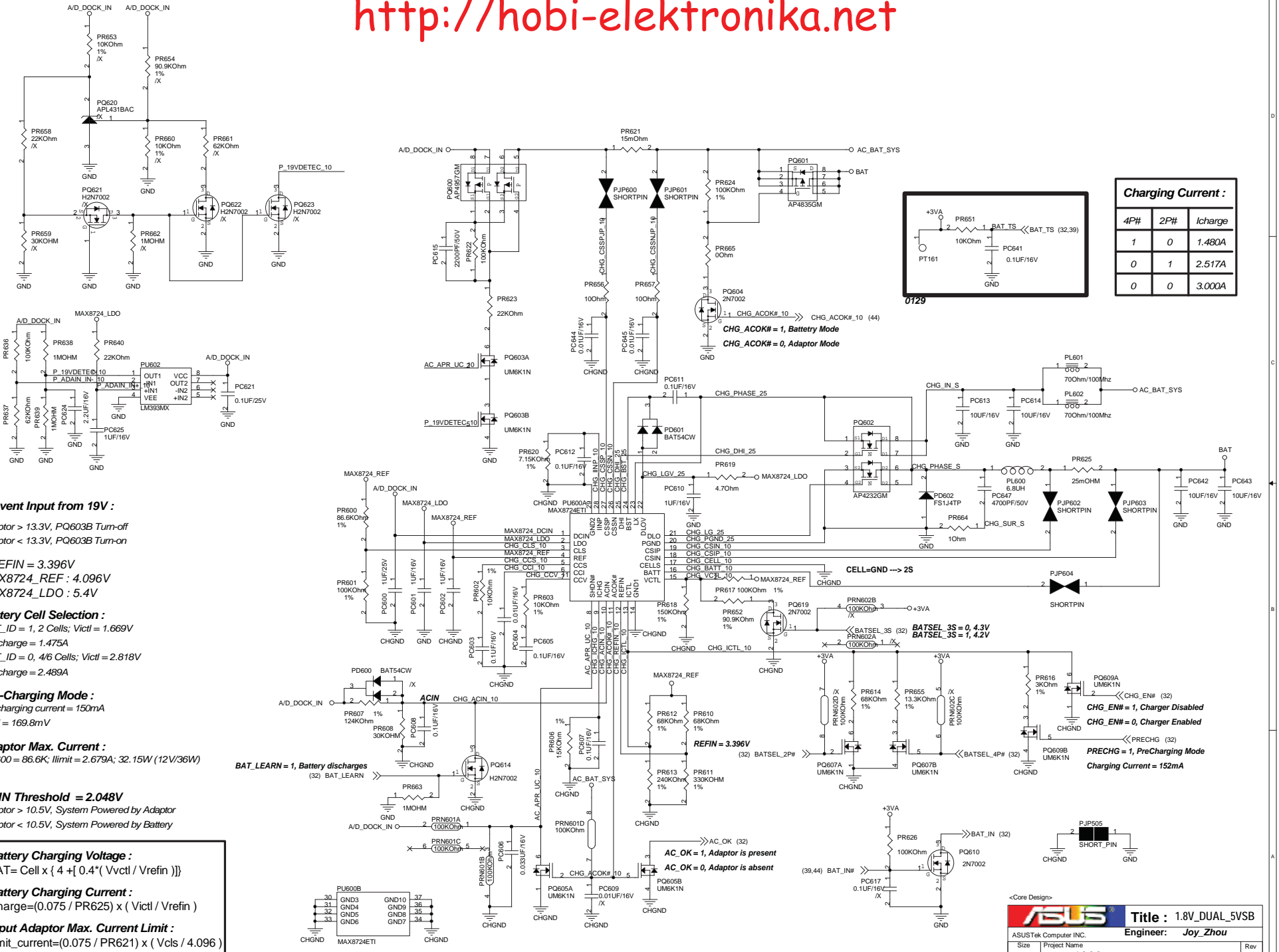


0115



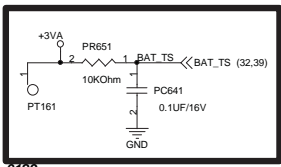
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		Title : +1.5VS +2.5VS	
ASUSTek Computer INC.		Engineer: Joy_Zhou	
Size	Project Name	Rev	
A3	1000	1.0G	
Date: Tuesday, August 12, 2008		Sheet	47 of 50



**Charging Current :**

4P#	2P#	Icharge
1	0	1.480A
0	1	2.517A
0	0	3.000A



**Prevent Input from 19V :**  
 Adaptor > 13.3V, PQ603B Turn-off  
 Adaptor < 13.3V, PQ603B Turn-on

$V_{REFIN} = 3.396V$   
 $MAX8724\_REF = 4.096V$   
 $MAX8724\_LDO = 5.4V$

**Battery Cell Selection :**  
 $BAT\_ID = 1, 2\ Cells; V_{ictl} = 1.669V$   
 $\Rightarrow I_{charge} = 1.475A$   
 $BAT\_ID = 0, 4/6\ Cells; V_{ictl} = 2.818V$   
 $\Rightarrow I_{charge} = 2.489A$

**Pre-Charging Mode :**  
 Precharging current = 150mA  
 $V_{ictl} = 169.8mV$

**Adaptor Max. Current :**  
 $PR600 = 86.6K; I_{limit} = 2.679A; 32.15W (12V/36W)$

**ACIN Threshold = 2.048V**  
 Adaptor > 10.5V, System Powered by Adaptor  
 Adaptor < 10.5V, System Powered by Battery

**Battery Charging Voltage :**  
 $BAT = Cell \times \{ 4 + [ 0.4 * ( V_{vctl} / V_{refin} ) ] \}$

**Battery Charging Current :**  
 $I_{charge} = (0.075 / PR625) \times ( V_{ictl} / V_{refin} )$

**Input Adaptor Max. Current Limit :**  
 $I_{limit\_current} = (0.075 / PR621) \times ( V_{cls} / 4.096 )$

**BAT\_LEARN = 1, Battery discharges**  
 (32) BAT\_LEARN

**AC\_OK = 1, Adaptor is present**  
**AC\_OK = 0, Adaptor is absent**

ASUS Logo

**Title : 1.8V\_DUAL\_5VSB**

ASUSTek Computer INC. Engineer: **Joy\_Zhou**

Size: Custom Project Name: **1000** Rev: 1.0G

Date: Tuesday, August 12, 2008 Sheet 48 of 50



**EC KB3310 GPIO SETTING**

**EC KB3310 Other Pin SETTING**


Pin	Pin Name	Signal Name	Type	Note
1	GPIO00/GA20	A20GATE	O	
2	GPIO01/KBRST#	RC_IN#	O	
6	GPIO04	EMAIL_SW#	I	Internal pull high
13	GPIO05/PCIRST#	PCI_RST#	I	
14	GPIO07	BAT_OTP	I	Battery over temperature
15	GPIO08	EXTSM#	OD	10K pull high to +3VSB
16	GPIO0A	LID_EC#	I	Internal pull high
17	GPIO0B/ESB_CLK	NC	O	
18	GPIO0C/ESB_DAT	NC	O	
19	GPIO0D	DISTP_SW#	I	Internal pull high
20	GPIO0E/SC#	EXT_SC#	O	10K pull high to +3VSB
21	GPIO0F/PWM0	BL_PWM_DA	O	
23	GPIO10/PWM1	BAT_CRITICAL	I	Battery critical capacity
25	GPIO11/PWM2	PM_PWRBTN#	OD	Internal pull high in ICH
26	GPIO12/FANPWM1	FAN0_PWM	O	CPU Fan
27	GPIO13/FANPWM2	FAN1_PWM	O	VGA Fan
28	GPIO14/FANFB1	FAN0_TACH	I	CPU FanTach
29	GPIO15/FANFB2	FAN1_TACH	I	VGA FanTach
30	GPIO16/E51_TX	E51_TX	O	RS232 debug port
31	GPIO17/E51_RX	E51_RX	I	RS232 debug port
32	GPIO18	PWR_SW#	I	Internal pull high
34	GPIO19/PWM3	MAIL_LED#	O	
36	GPIO1A/NUMLED	NUM_LED#	O	
38	GPIO1D/CLKRUN#	NC	O	
39	GPIO20/KSO0/TP_TEST	KSO0	O	
40	GPIO21/KSO1/TP_PLL	KSO1	O	
41	GPIO22/KSO2	KSO2	O	
42	GPIO23/KSO3	KSO3	O	
43	GPIO24/KSO4	KSO4	O	
44	GPIO25/KSO5	KSO5	O	
45	GPIO26/KSO6	KSO6	O	
46	GPIO27/KSO7	KSO7	O	
47	GPIO28/KSO8	KSO8	O	
48	GPIO29/KSO9	KSO9	O	
49	GPIO2A/KSO10	KSO10	O	
50	GPIO2B/KSO11	KSO11	O	
51	GPIO2C/KSO12	KSO12	O	
52	GPIO2D/KSO13	KSO13	O	
53	GPIO2E/KSO14	KSO14	O	
54	GPIO2F/KSO15	KSO15	O	
55	GPIO30/KSI0	KSI0	I	Internal pull high
56	GPIO31/KSI1	KSI1	I	Internal pull high
57	GPIO32/KSI2	KSI2	I	Internal pull high
58	GPIO33/KSI3	KSI3	I	Internal pull high
59	GPIO34/KSI4	KSI4	I	Internal pull high
60	GPIO35/KSI5	KSI5	I	Internal pull high
61	GPIO36/KSI6	KSI6	I	Internal pull high
62	GPIO37/KSI7	KSI7	I	Internal pull high
63	GPI38/AD0	BAT_ICHG	I	
64	GPI39/AD1	BAT_CONFIG	I	Battery configuration
65	GPIO3A/AD2	BAT_SENSE	I	Battery Voltage Sensor
66	GPIO3B/AD3	BAT_TS	I	Battery Thermal Sensor
68	GPO3C/DA0	DOC	O	Trigger Clock Gen

Pin	Pin Name	Signal Name	Type	Note
70	GPO3D/DA1	LCD_BACKOFF#	O	
71	GPO3E/DA2	CLK_PWRSERVE#	O	
72	GPO3F/DA3	BAT_LL#	O	Battery Low Low
73	GPIO40	AC_OK	I	AC Adaptor Plug in
74	GPIO41	PM_RSMRST#	O	10K pull down to GND
75	GPI42	BAT_IN	I	
76	GPI43	CLRTC_EC	I	
77	GPIO44/SCL1	SMB0_CLK	I/OD	4.7K pull high to +3VA_EC
78	GPIO45/SDA1	SMB0_DAT	I/OD	4.7K pull high to +3VA_EC
79	GPIO46/SCL2	SMB1_CLK	I/OD	10K pull high to +3V
80	GPIO47/SDA2	SMB1_DAT	I/OD	10K pull high to +3V
81	GPIO48/KSO16	KB pin 28	I	for KB type detection
82	GPIO49/KSO17	KB pin 27	I	for KB type detection
83	GPIO4A/PSCLK1	AUO_SCL	O	for AUO, default H at S0
84	GPIO4B/PSDAT1	AUO_SDA	O	for AUO, default L at S0
85	GPIO4C/PSCLK2	AUO_CSB	O	for AUO, default H at S0
86	GPIO4D/PSDAT2	LVDD_EN	I	for AUO 7" Panel
87	GPIO4E/PSCLK3	TP_CLK	I/OD	10K pull high to +3V
88	GPIO4F/PSDAT3	TP_DAT	I/OD	10K pull high to +3V
89	GPIO50/SELIO#	BATSEL_3S	O	Battery series, H:3S, L:4S
90	GPIO52/E51_CS#	CHG_LED_UP#	O	
91	GPIO53/CAPLED	CAP_LED#	O	
92	GPIO54	PWR_LED_UP	O	
93	GPIO55/SCRLED	SCRLED#	O	
95	GPIO56	PWR4G_SW#	I	Internal pull high
97	GPX0A00/SDICS#	SPI_MODE#	O	4.7K pull down to GND
98	GPX0A01/SDICLK	SUSC_ON	O	
99	GPX0A02/SDIDO	VSUS_ON	O	
100	GPX0A03	CPU_VRON	O	
101	GPX0A04	SUSB_ON	O	
102	GPX0A05	ICH_PWROK	O	
103	GPX0A06	VOLT_CTRL	O	
104	GPX0A07	CHG_EN#	O	Battery charging enabled
105	GPX0A08	PRECHG	O	
106	GPX0A09	SPI_WP#	O	
107	GPX0A10	OP_SD#	O	Audio OP
108	GPX0A11	BAT_LEARN	O	
109	GPXID0/SDIDI	BATSEL_2P#	O	Battery parallel, H:1P, L:2P-3P
110	GPXID1	NC	O	
112	GPXID2	THRO_CPU	O	Active if CPU temperature over spec
114	GPXID3	SUSB#	I	100K pull down to GND
115	GPXID4	SUSC#	I	100K pull down to GND
116	GPXID5	CPUPWR_GD	I	Pull high to +3V
117	GPXID6	VSUS_GD	I	
118	GPXID7	NC	O	
121	GPI057	INTERNET#	I	Internal pull high
126	GPIO57/SPICLK	SPI_CLK	O	
127	GPIO59/TEST_CLK	NC	O	

Pin	Pin Name	Signal Name	Type	Note
3	SERIRQ	INT_SERIRQ	I/OD	10K pull high to +3V
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA_EC	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCI_EC	I	
22	VCC	+3VA_EC	P	
24	GND	GND	P	
33	VCC	+3VA_EC	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	100K pull high to +3VA_EC
67	AVCC	+3VACC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA_EC	P	
111	VCC	+3VA_EC	P	
113	GND	GND	P	
119	RD#/SPIDI	SPI_SO	I	
120	WR#/SPIDO	SPI_SI	O	
112	XCLKI	32KXCLKI	I	
123	XCLKO	32KXCLKO	O	
124	V18R	V18R	P	Reserved 1uF to GND
125	VCC	+3VA_EC	P	
128	SPICS#/SELMEM#	SPI_CE#	O	

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<Core Design>

		<b>Title :</b> History	
ASUSTek Computer INC.		<b>Engineer:</b> <i>Satan He</i>	
Size	Project Name	Rev	
A3	<b>1000</b>	1.0G	
Date: Tuesday, August 12, 2008		Sheet	50 of 50