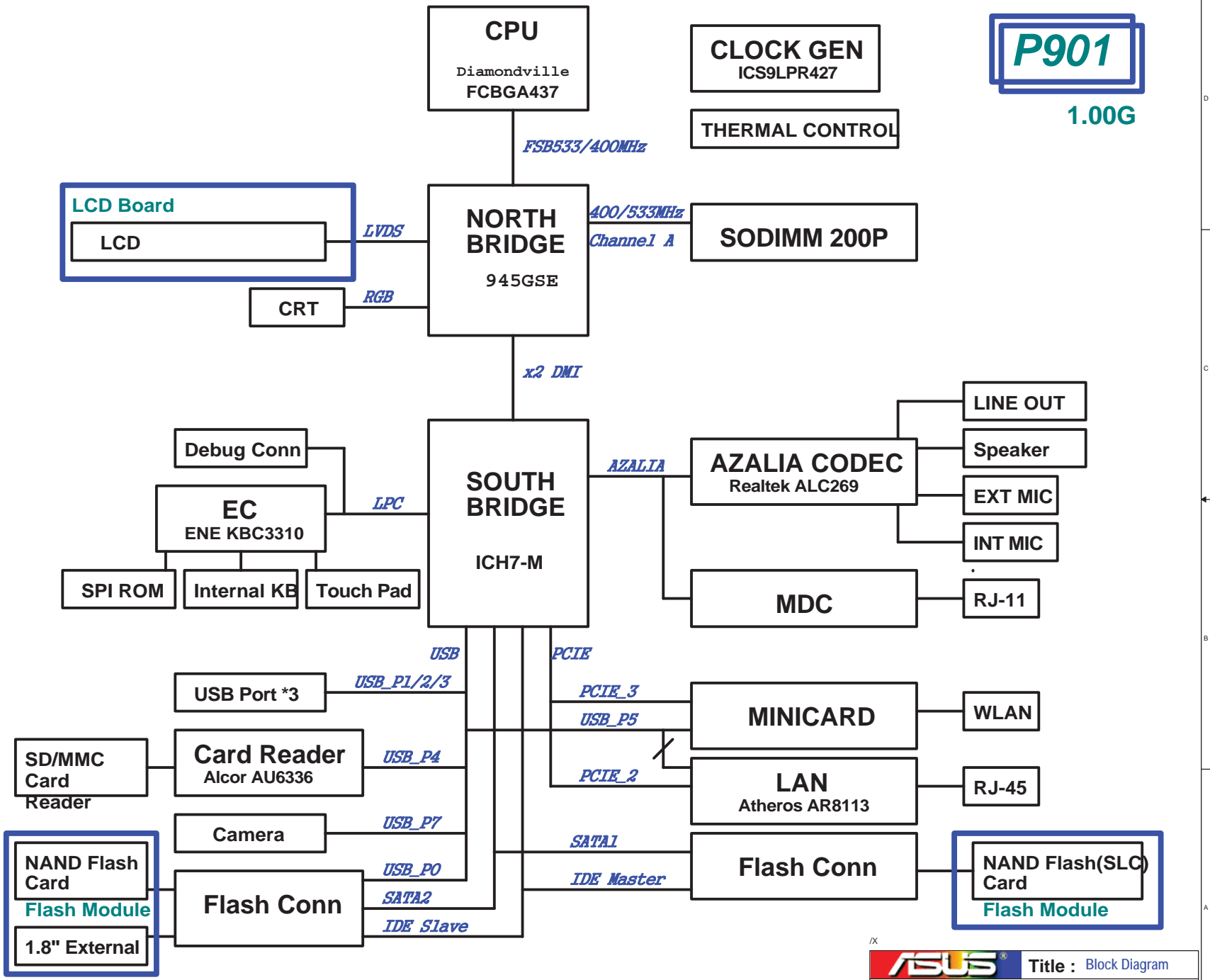


- 01\_Block Diagram
- 02\_System Setting
- 03\_Power Sequence
- 04\_Clock Gen\_ICS9LPR426
- 05\_Diamondville\_BUS
- 06\_Diamondville\_PWR
- 07\_NB-945GMS(HOST)
- 08\_NB-945GMS(DMI)
- 09\_NB-945GMS(GRAPHIC)
- 10\_NB-945GMS(DDR2)
- 11\_NB-945GMS(PWR)
- 12\_NB-945GMS(PWR2)
- 13\_NB-945GMS(GND)
- 14\_SB-ICH7M(PWR)
- 15\_SB-ICH7M(1)
- 16\_SB-ICH7M(2)
- 17\_SB-ICH7M(3)
- 18\_DDR2 SODIMM
- 19\_DDR2 Termination
- 20\_Onboard VGA
- 21\_LCD Conn\_LID
- 22\_PCIEx 3.5G & Ext. Antenna
- 23\_Mini WIFI+ BT
- 24\_LAN\_Atheros AR8113
- 25\_MDC\_RJ11\_RJ45
- 26\_HD + Flash Conn
- 27\_USB Port
- 28\_Camera Conn
- 29\_Card Reader\_AU6336C52
- 30\_Codec\_ALC269
- 31\_Audio\_AMP\_Jack
- 32\_EC\_ENE KB3310
- 33\_EC\_UART controller
- 34\_Switch\_SPI ROM\_Debug Conn
- 35\_Thermal Sensor\_FAN
- 36\_KB\_Touch Pad
- 37\_LED\_THERMTRIP
- 38\_Discharge
- 39\_PWR Jack
- 40\_Srew Hole
- 41\_EMI
- 42\_POWER FLOW
- 43\_Vcore
- 44\_Power System
- 45\_Power\_+1.8V & VTTDDR
- 46\_Power\_VCCP
- 47\_Power\_+1.5VS & +2.5VS
- 48\_Power\_Charger
- 49\_EC Pin Define
- 49\_History



**P901**

1.00G

<b>ASUS</b>		Title : Block Diagram	
ASUSTek Computer INC.		Engineer: Regin Chiang	
Size	Project Name	Rev	
A3	P901	1.00G	
Date: Tuesday, April 01, 2008	Sheet	1	of 50

**EEE PC 701 PCB version**

GPI37	GPI38	GPI39	PCB version
0	0	0	
0	0	0	
0	0	1	
0	0	1	
0	1	0	
0	1	0	
0	1	1	
0	1	1	
1	0	0	
1	0	0	
1	0	1	
1	0	1	
1	1	0	
1	1	0	
1	1	1	
1	1	1	

**USB**

USB 0	Flash Conn
USB 1	USB Conn
USB 2	USB Conn
USB 3	USB Conn
USB 4	Card Reader
USB 5	Minicard
USB 6	NC
USB 7	Camera

**PCIE**

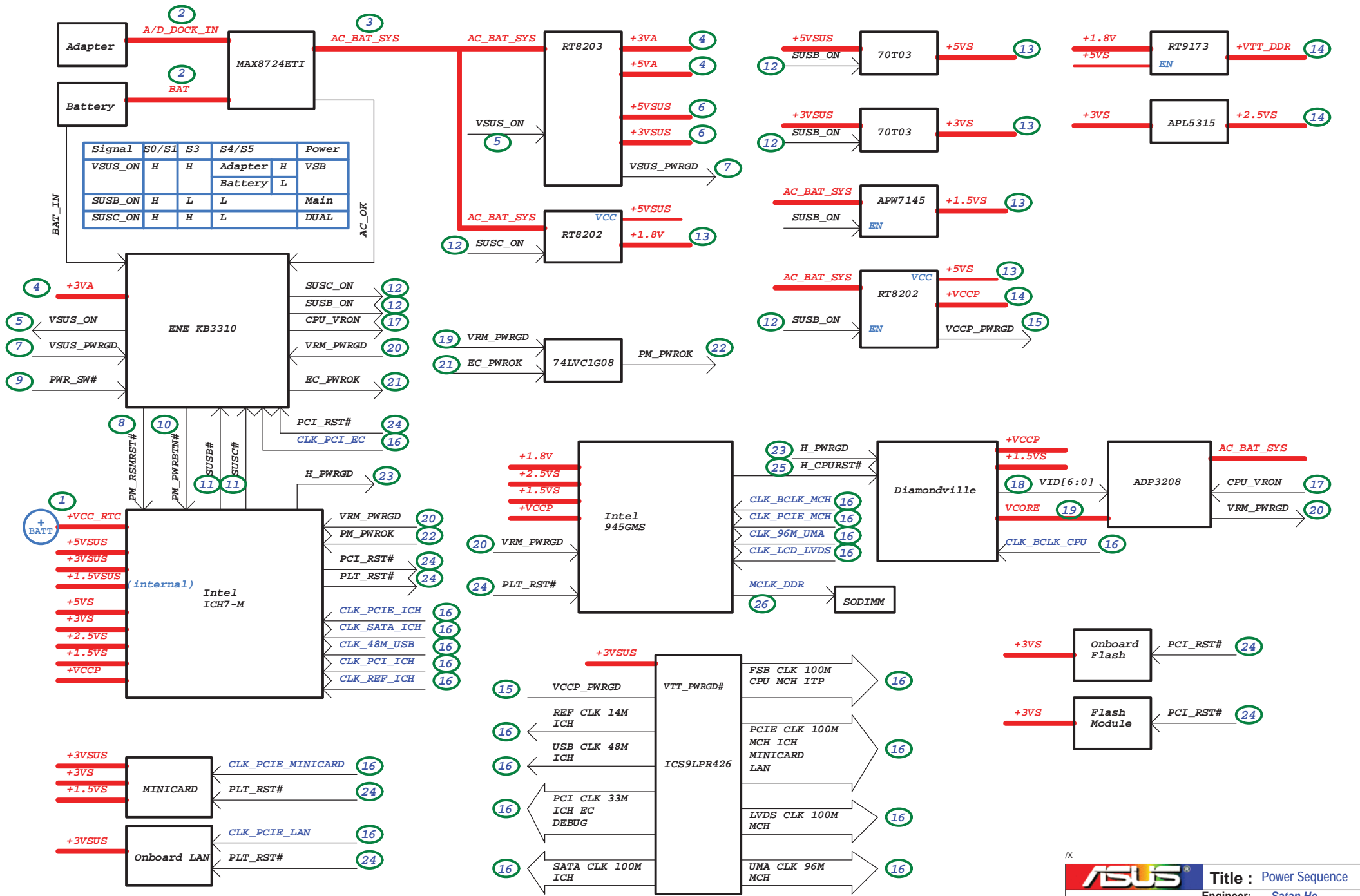
PCIE 1	NC
PCIE 2	LAN
PCIE 3	Minicard
PCIE 4	NC

**Azalia**

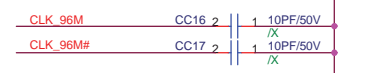
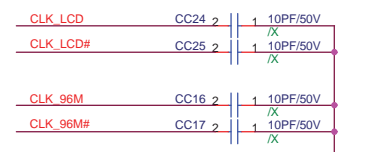
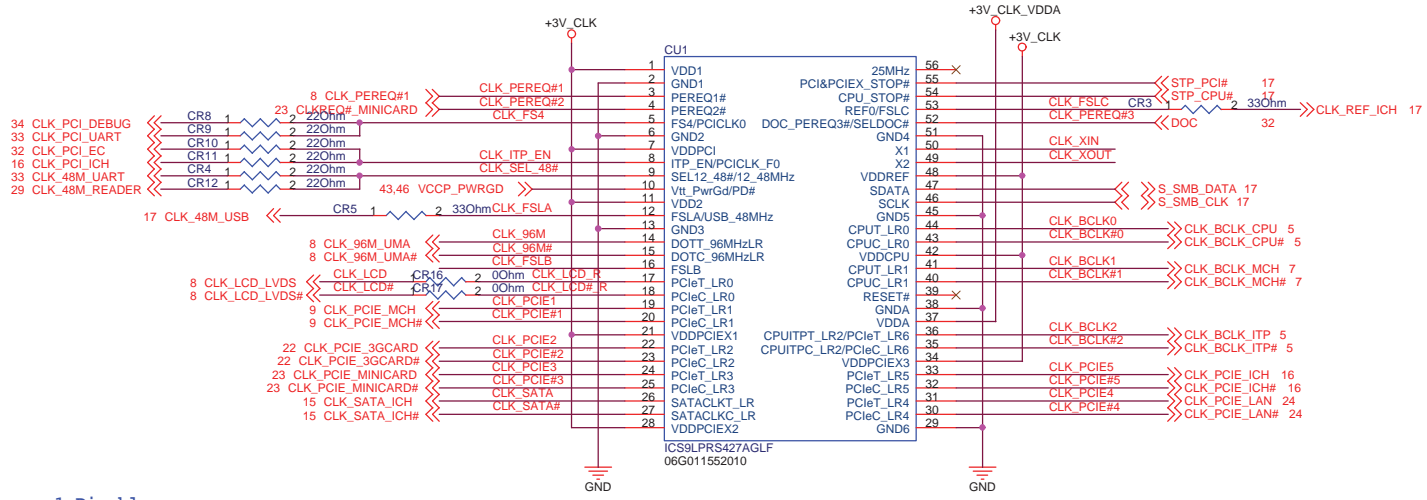
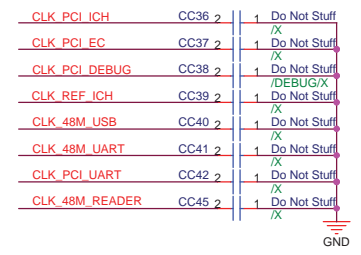
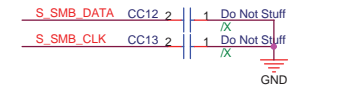
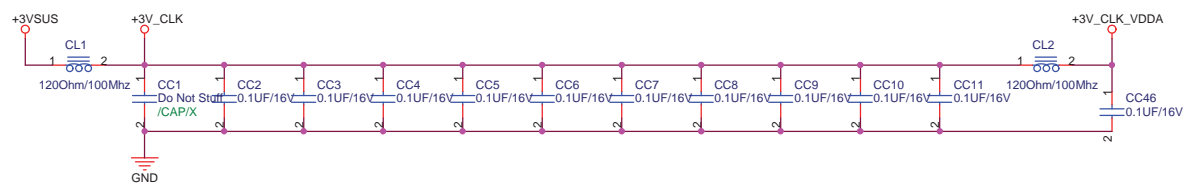
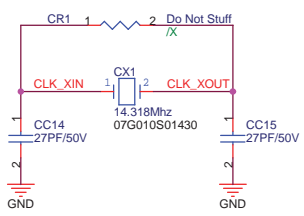
ACZ_SDIN0	CODEC
ACZ_SDIN1	MODEM
ACZ_SDIN2	NC

<http://hobi-elektronika.net>

		<b>Title : System Setting</b>	
ASUSTek Computer INC.		Engineer: <i>Satan_He</i>	
Size	Project Name		Rev
A3	<b>P901</b>		1,00G
Date: Monday, March 31, 2008		Sheet	2 of 50



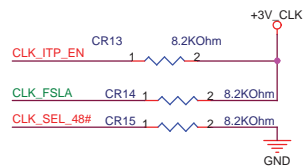
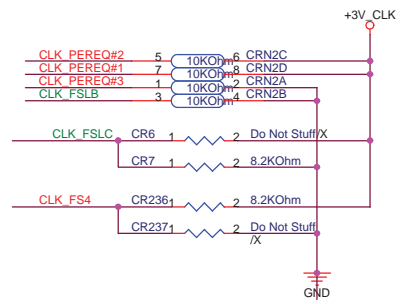
<http://hobi-elektronika.net>



1:Disable  
0:Enable

PEREQ1:PCIEx0 & PCIEx1  
PEREQ2:PCIEx2 & PCIEx3 & SATA  
PEREQ3:PCIEx4 & PCIEx5 & PCIEx6

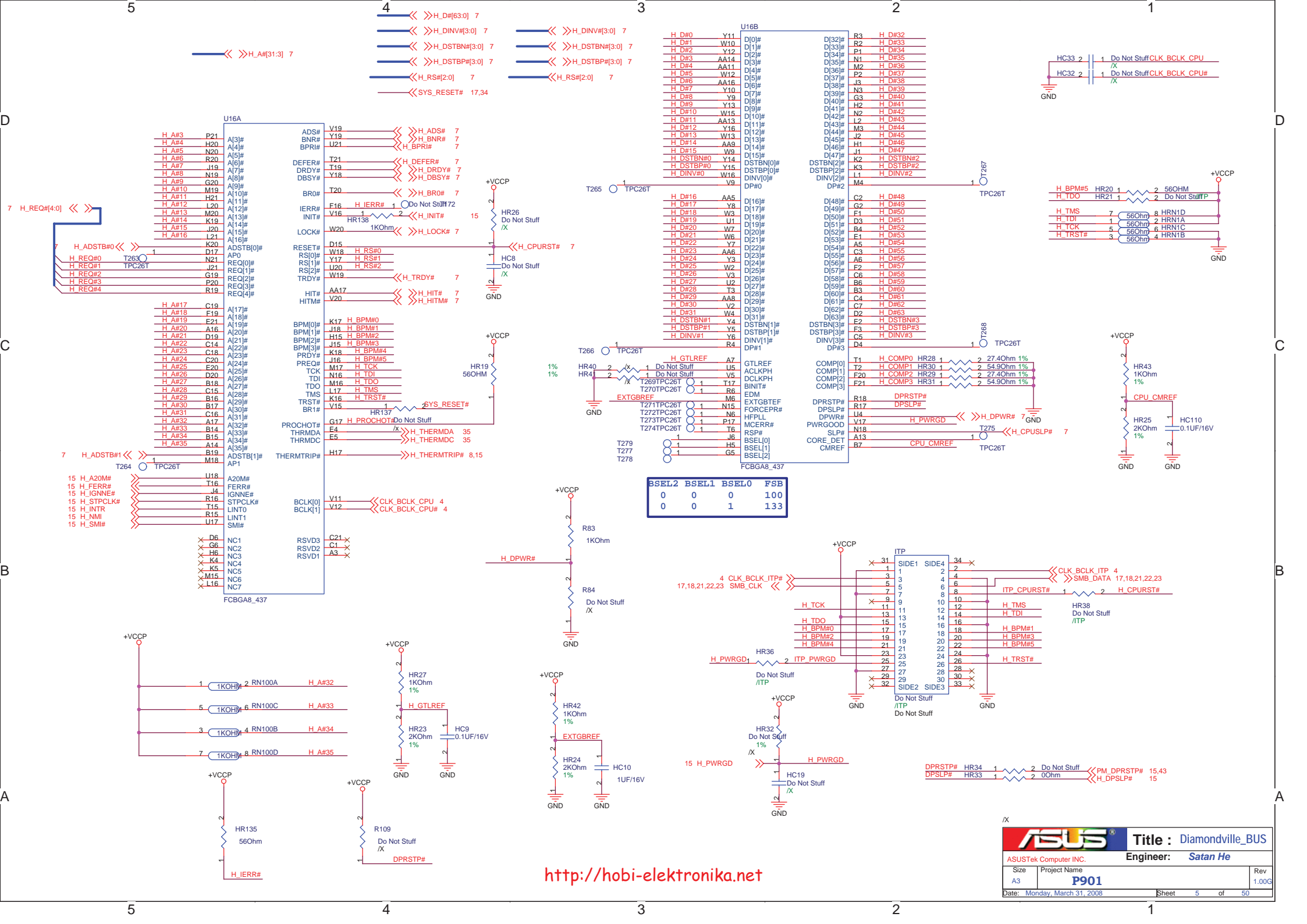
FSC	FSB	FSA	CPU	PCIE	SATA
0	0	1	133	100	100
1	0	1	100	100	100



<http://hobi-elektronika.net>

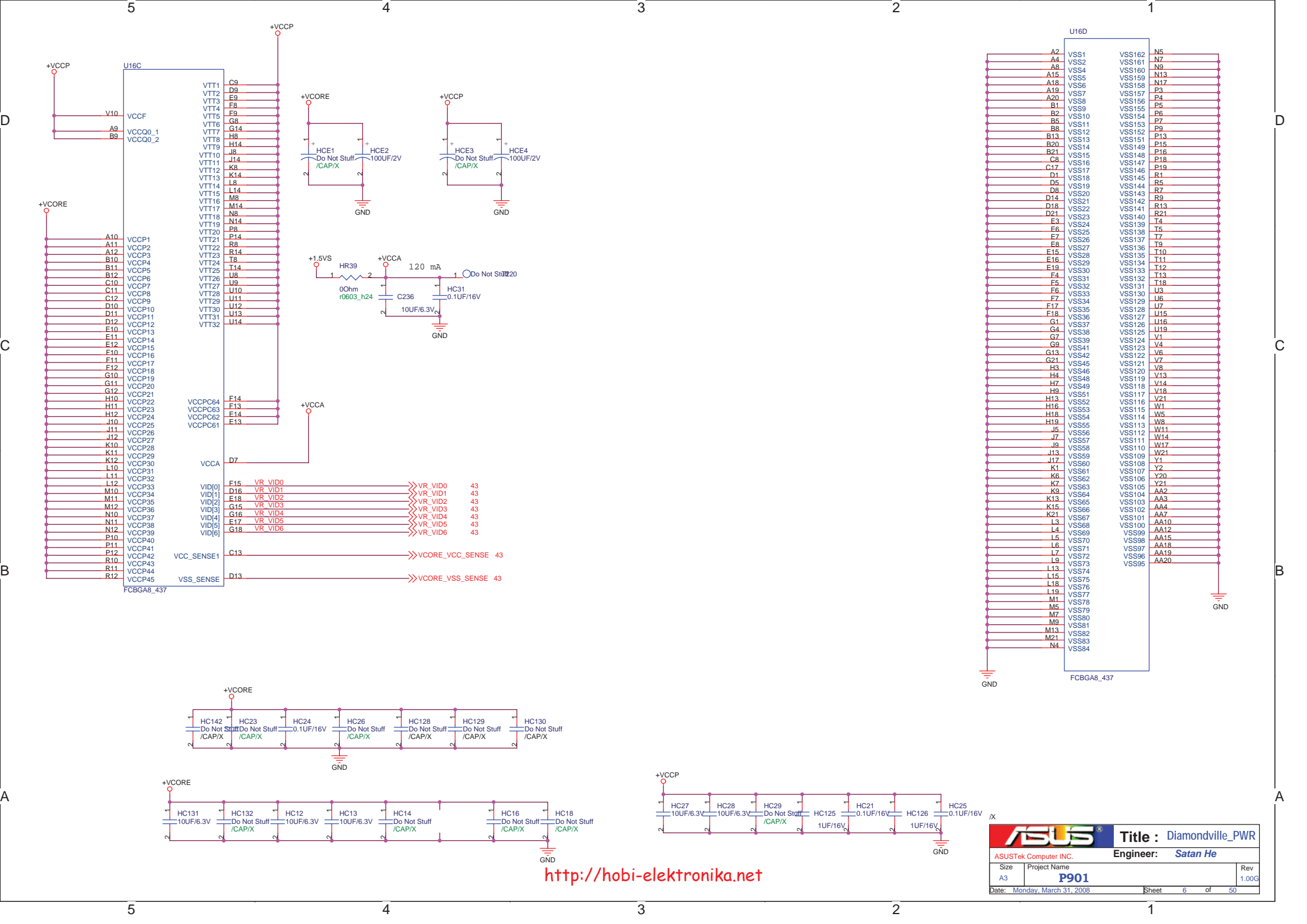
ASUS® Title : Clock Gen\_ICS9LPRS427  
ASUSTek Computer INC. Engineer: **Satan He**

Size	Project Name	Rev
A3	<b>P901</b>	1.0G
Date: Monday, March 31, 2008	Sheet 4 of 50	



BSEL2	BSEL1	BSEL0	FSB
0	0	0	1.00
0	0	1	1.33

<http://hobi-elektronika.net>



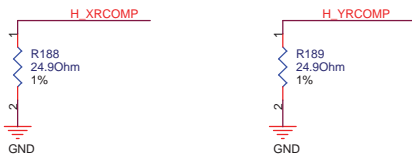
<http://hobi-elektronika.net>

<b>ASUS</b>		<b>Title : Diamondville_PWR</b>	
ASUSTek Computer INC.		Engineer: <b>Satan He</b>	
Size	Project Name		Rev
A3	<b>P901</b>		1.00G
Date:	Monday, March 31, 2008	Sheet	6 of 50

Power :  
+VCCP

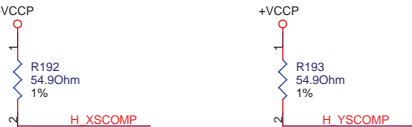
### RCOMP

For Calibrating the FSB I/O Buffer



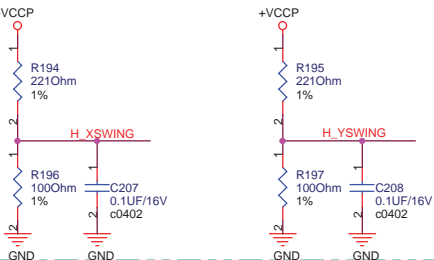
### SCOMP

For Slew Rate Compensation on the FSB

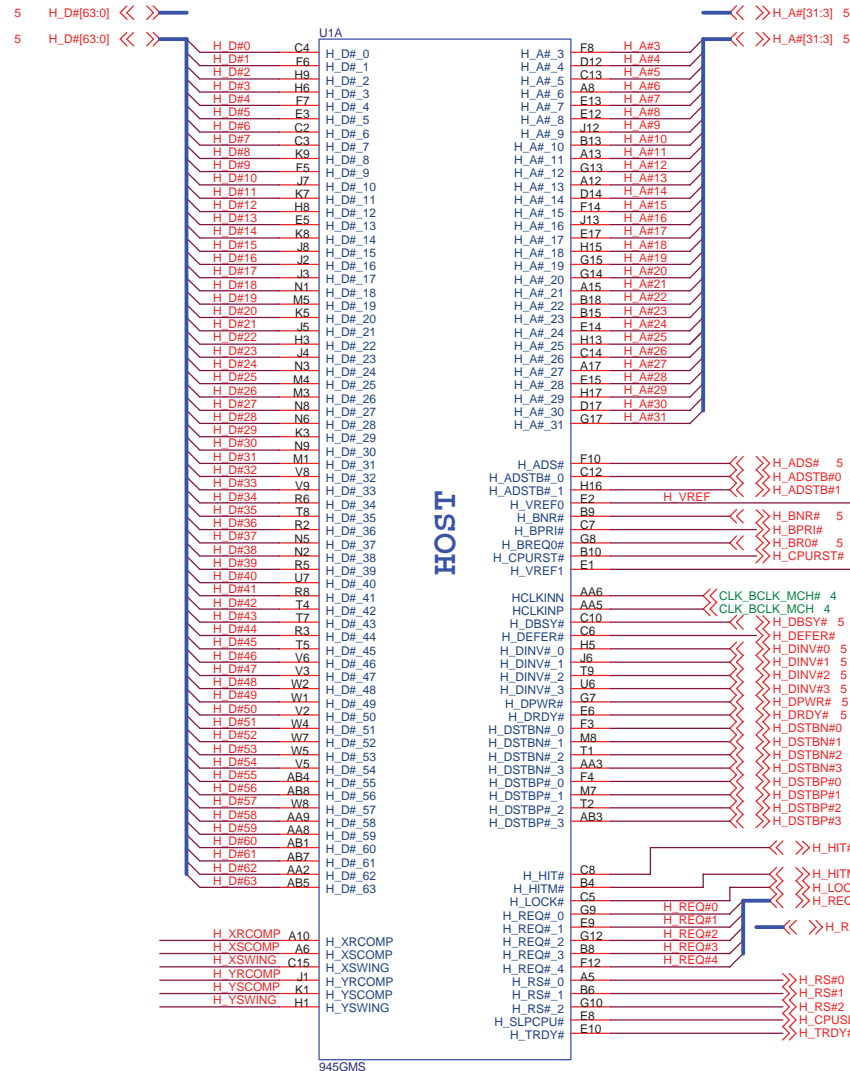


### Voltage Swing

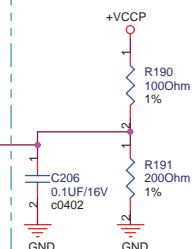
For Providing a Reference Voltage to The FSB RCOMP circuits



Signal voltage level =  
0.3125\*VCCP  
Trace should be 10 mil wide  
with 20 mil spacing

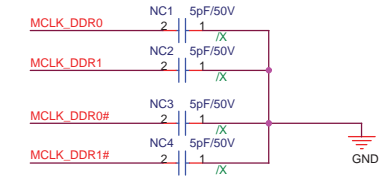
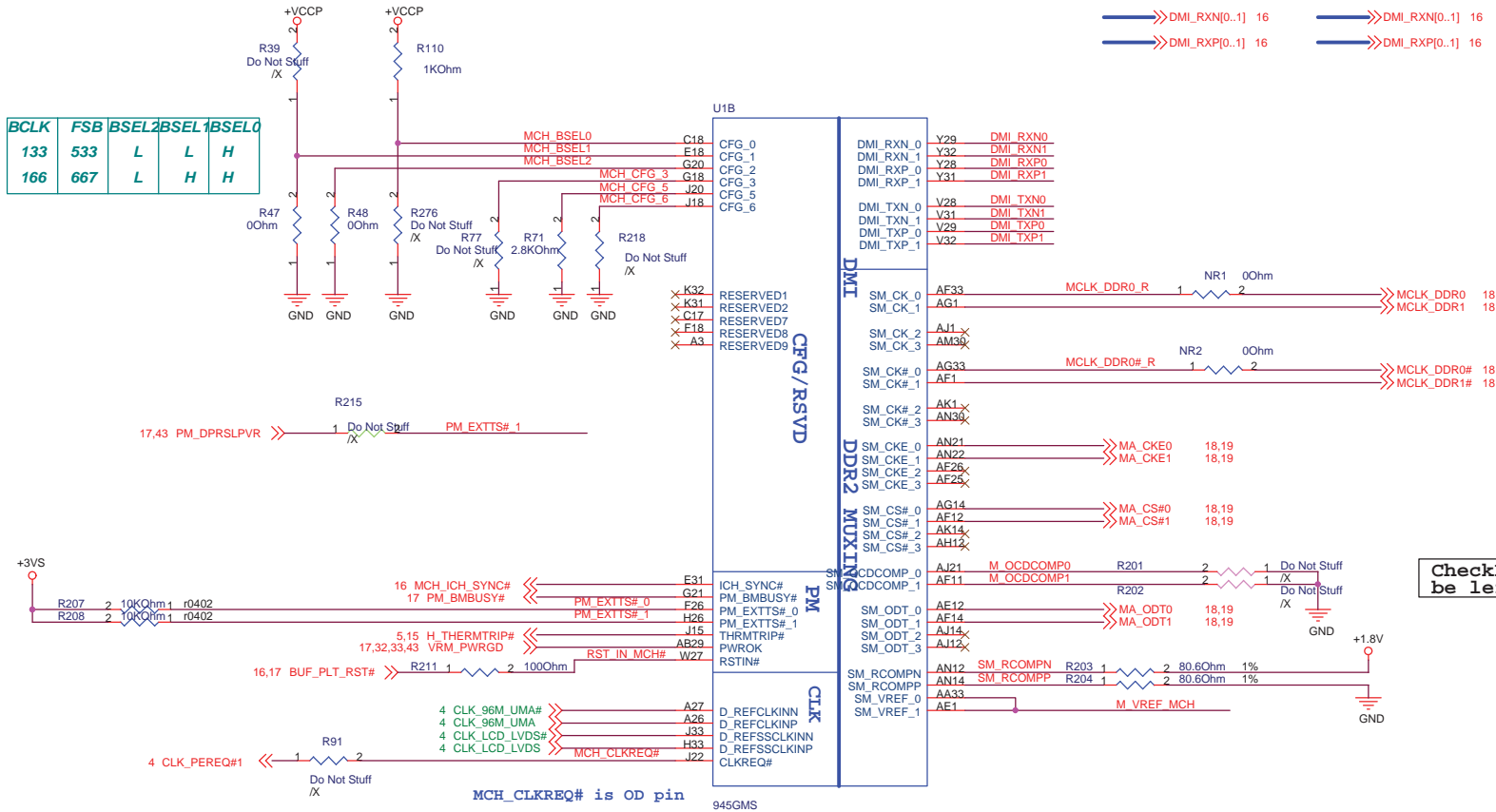


### AGTL+ I/O Voltage Reference

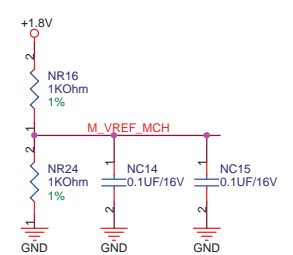


Layout Note:  
0.1uF should be placed 100mils or less from GMCH pin.

BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H



CheckList notes :Can be left as NC

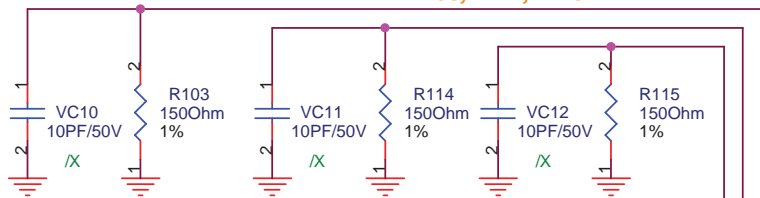


<http://hobi-elektronika.net>

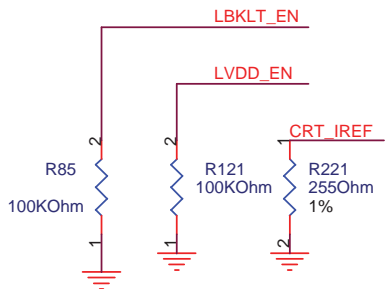
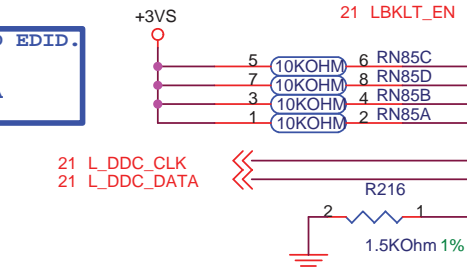
<b>ASUS</b>		<b>Title :</b> NB-945GMS(DMI & CFG)	
ASUSTeK COMPUTER INC.		Engineer: <i>Satan He</i>	
Size A3	Project Name <b>P901</b>	Rev 1.00G	
Date: Monday, March 31, 2008	Sheet	8	of 50



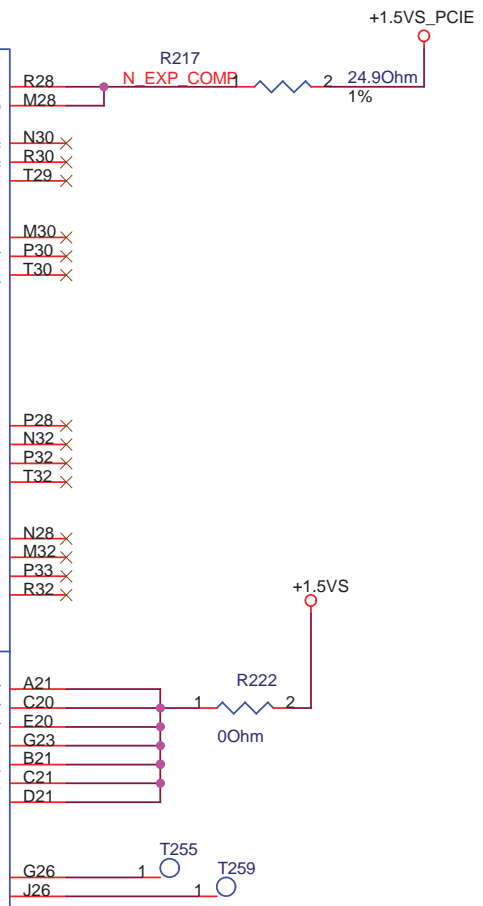
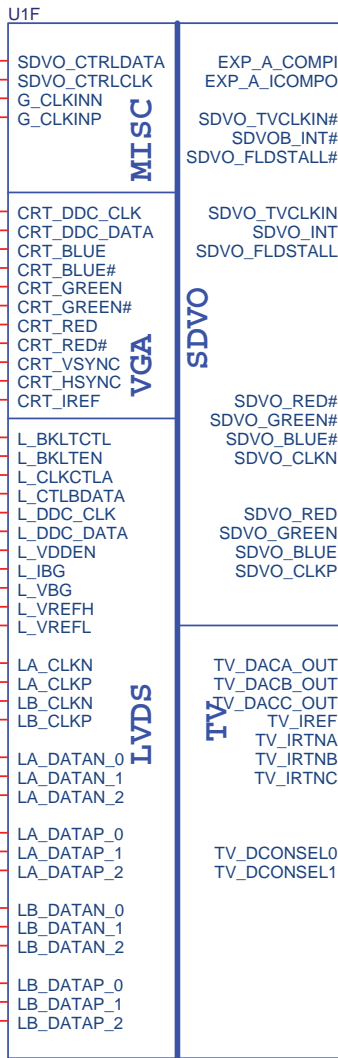
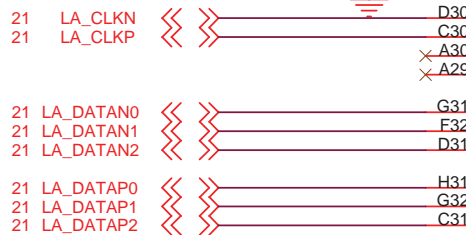
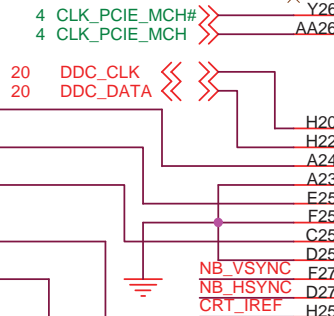
Close to GMCH  
R103,R114,R115



IF USE NB READ EDID.  
MUST CONNECT  
L\_DDC\_CLK&DATA



Close to GMCH



945GMS

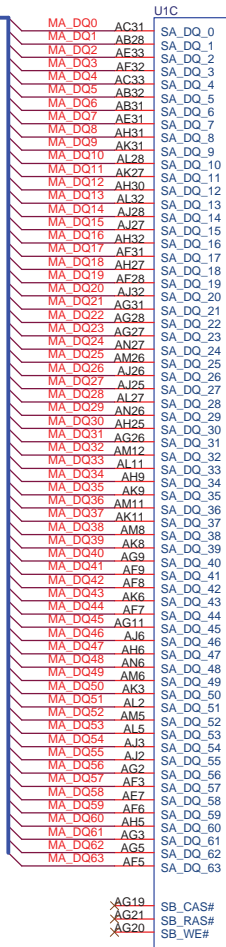
/X

		<b>Title :</b> NB-945GMS(GRAPHIC)	
ASUSTeK COMPUTER INC.		<b>Engineer:</b> Satan_He	
Size A4	Project Name <b>P901</b>	Rev 1.00G	
Date: Monday, March 31, 2008	Sheet 9 of 50		

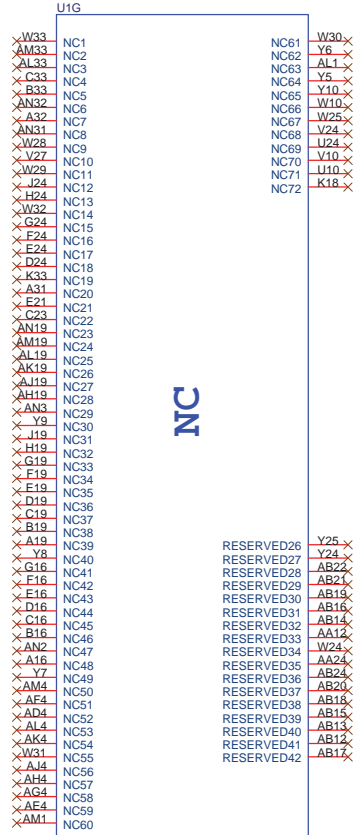
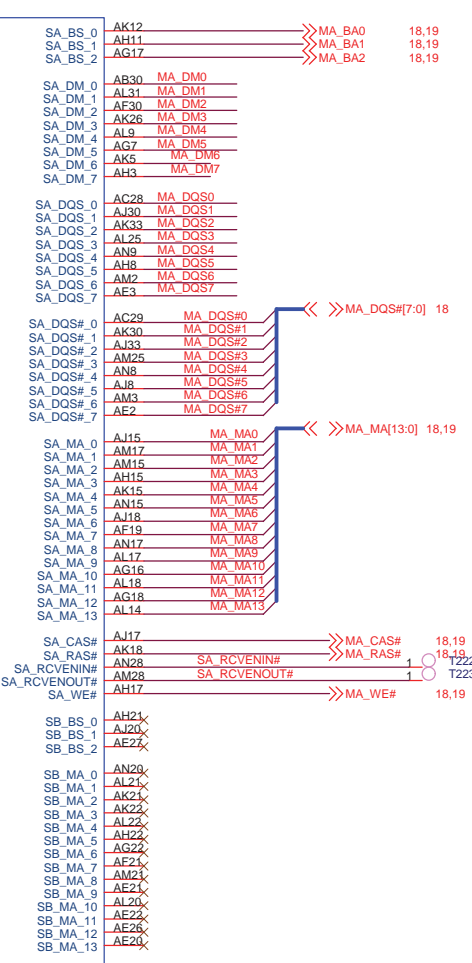
<http://hobi-elektronika.net>

18 MA\_DQ[63:0] << >>  
 18 MA\_DQ[63:0] << >>

<< >> MA\_DQS[7:0] 18  
 << >> MA\_DM[7:0] 18



DDR2 SYSTEM MEMORY

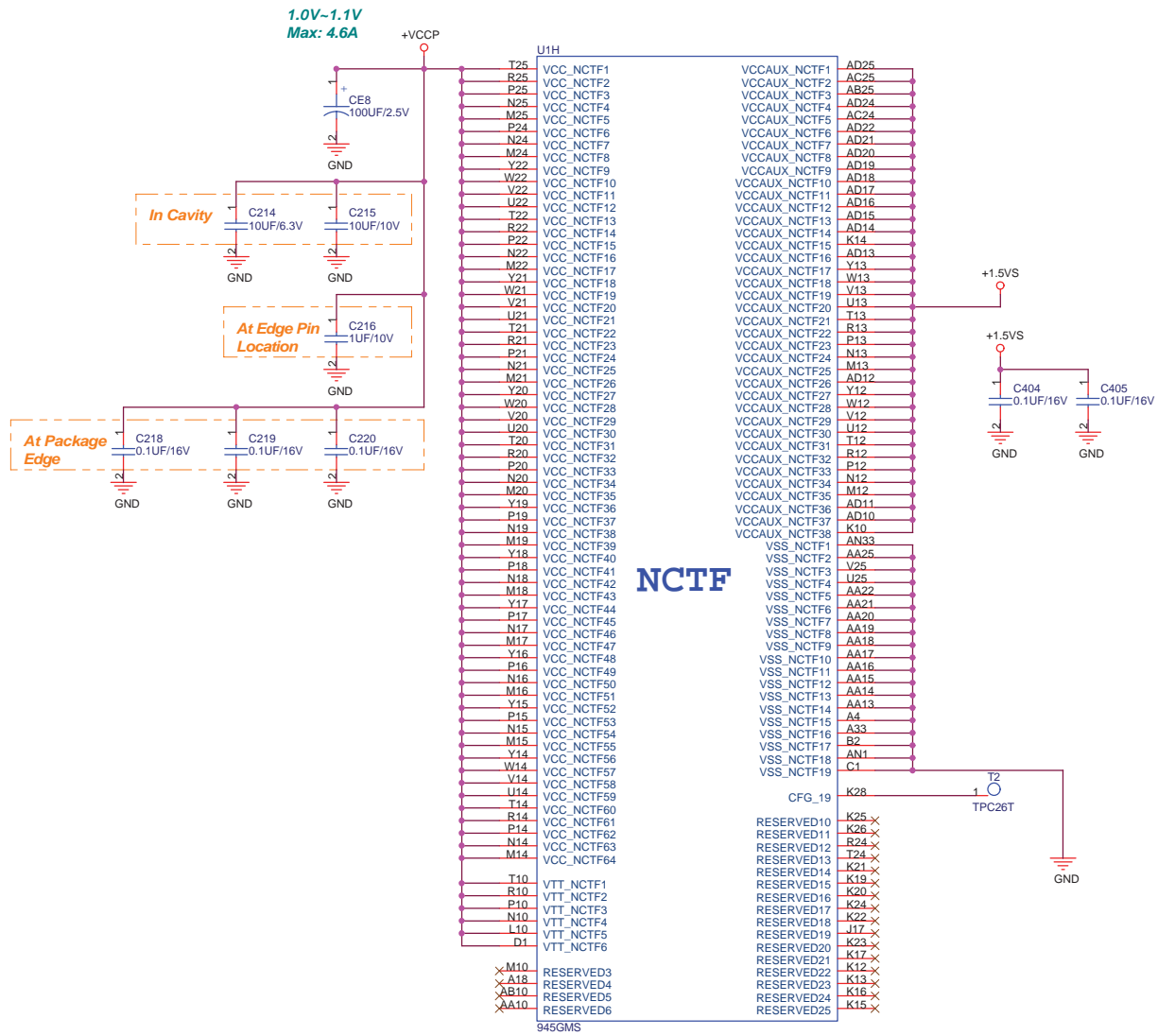


945GMS

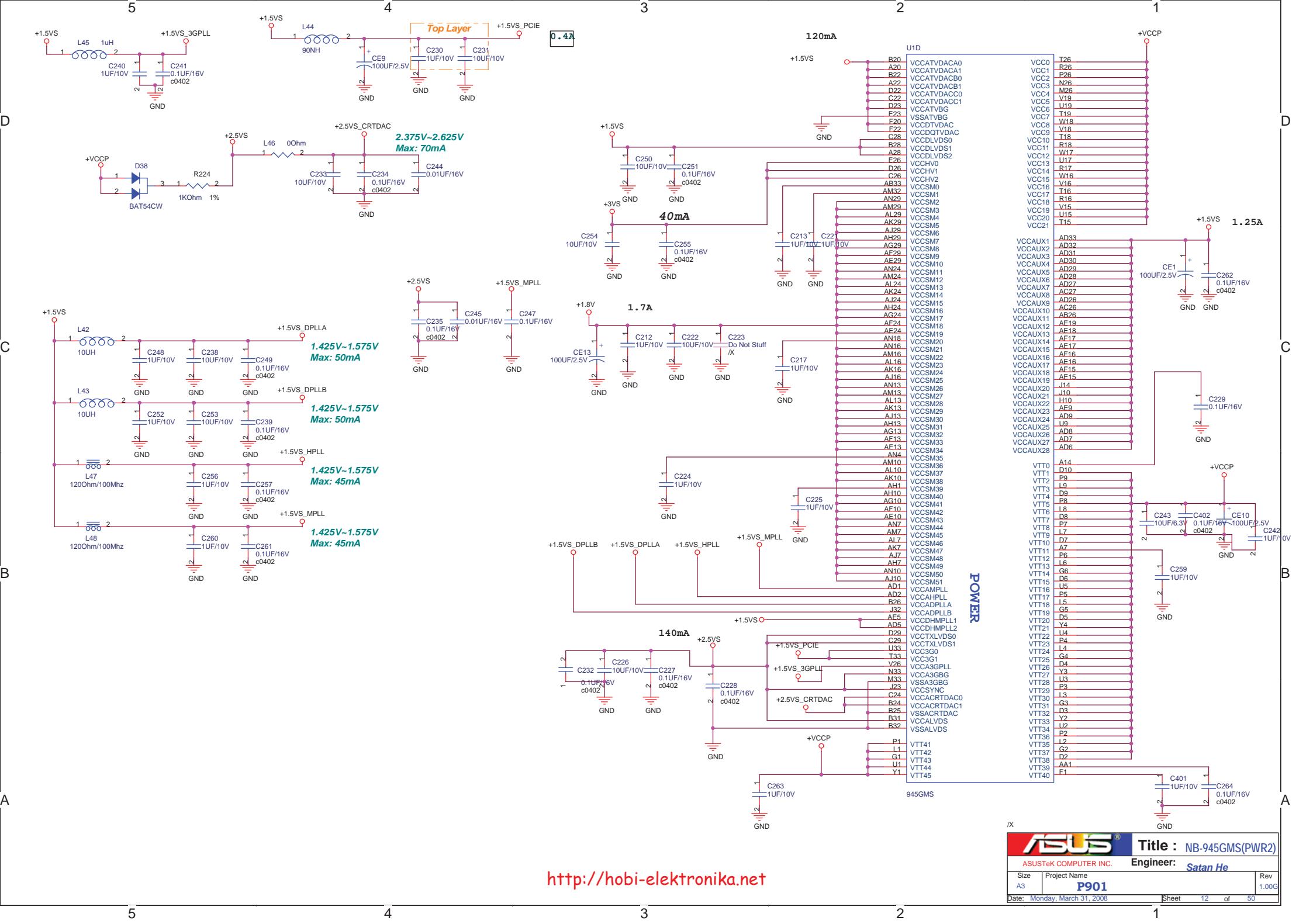
945GMS

ASUS Title : NB-945GMS(DDR2)  
 ASUSTek COMPUTER INC. Engineer: Satan He

Size A3	Project Name P901	Rev 1.00G
Date: Monday, March 31, 2008		Sheet 10 of 50

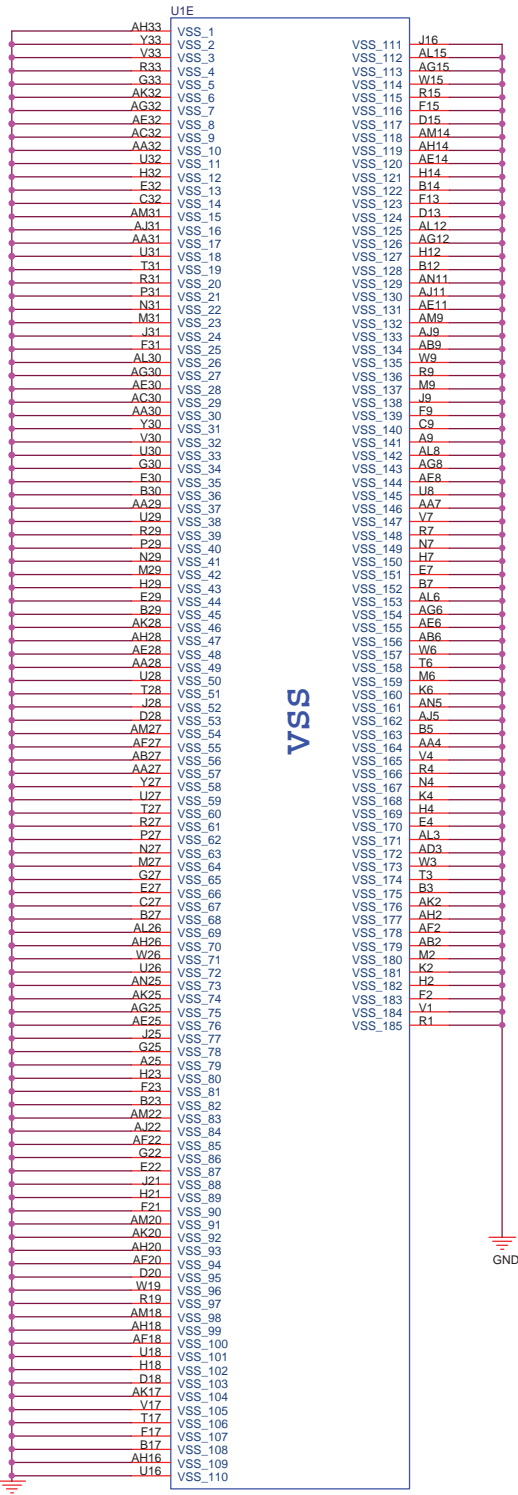


**CFG\_19(K28) Strapping :**  
**DMI LANE Reversal:**  
 0:Normal Operation (Default)  
 1.:Reversal Lanes, 3->0,2->1..etc  
 Note:945GMS doesn't support DMI Lane Reversal



<http://hobi-elektronika.net>

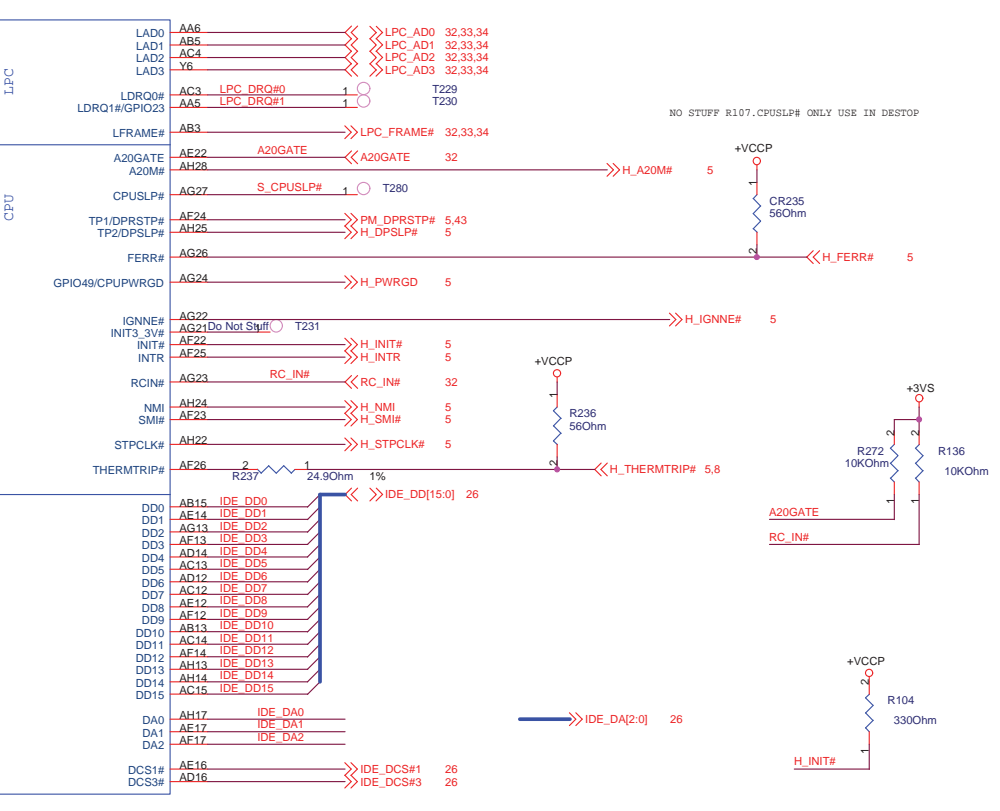
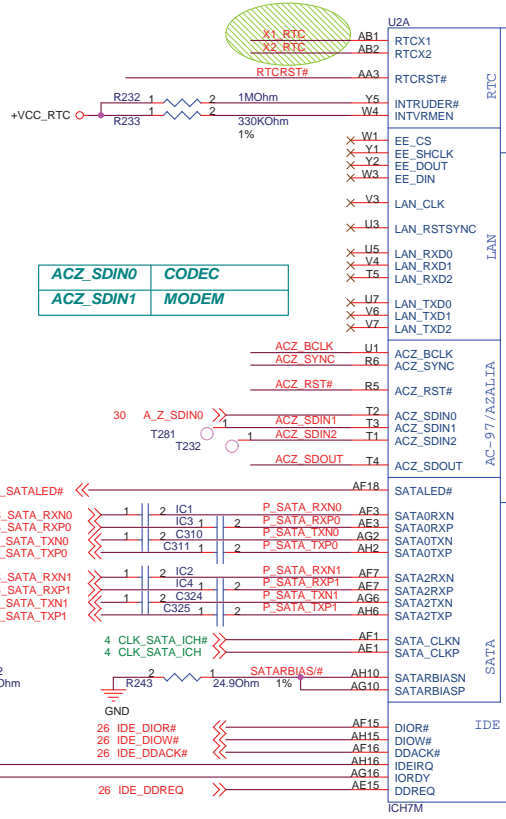
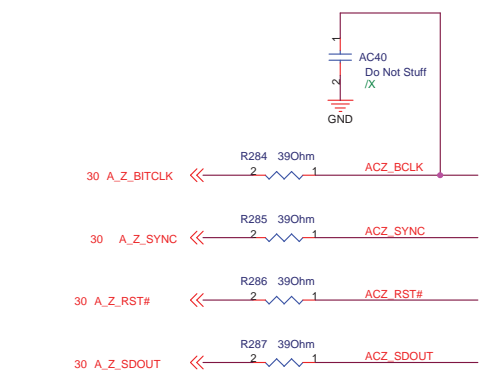
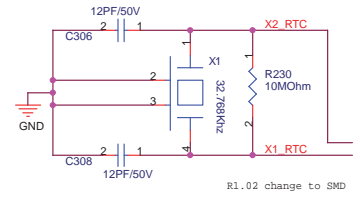
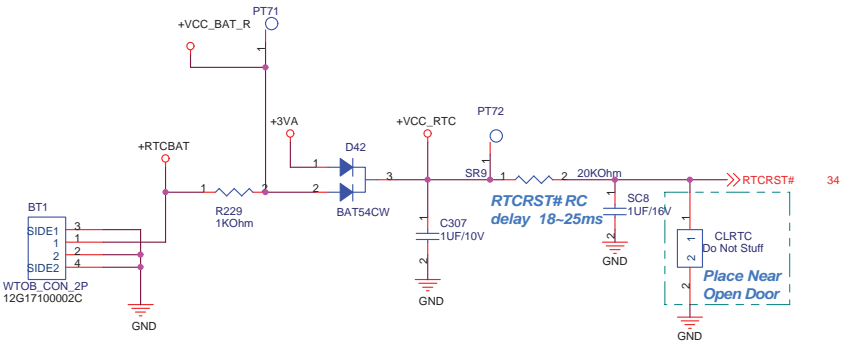
<b>ASUS</b>		<b>Title : NB-945GMS(PWR2)</b>	
ASUSTeK COMPUTER INC.		Engineer: <b>Satan He</b>	
Size	Project Name		Rev
A3	P901		1.00G
Date: Monday, March 31, 2008		Sheet 12 of 50	



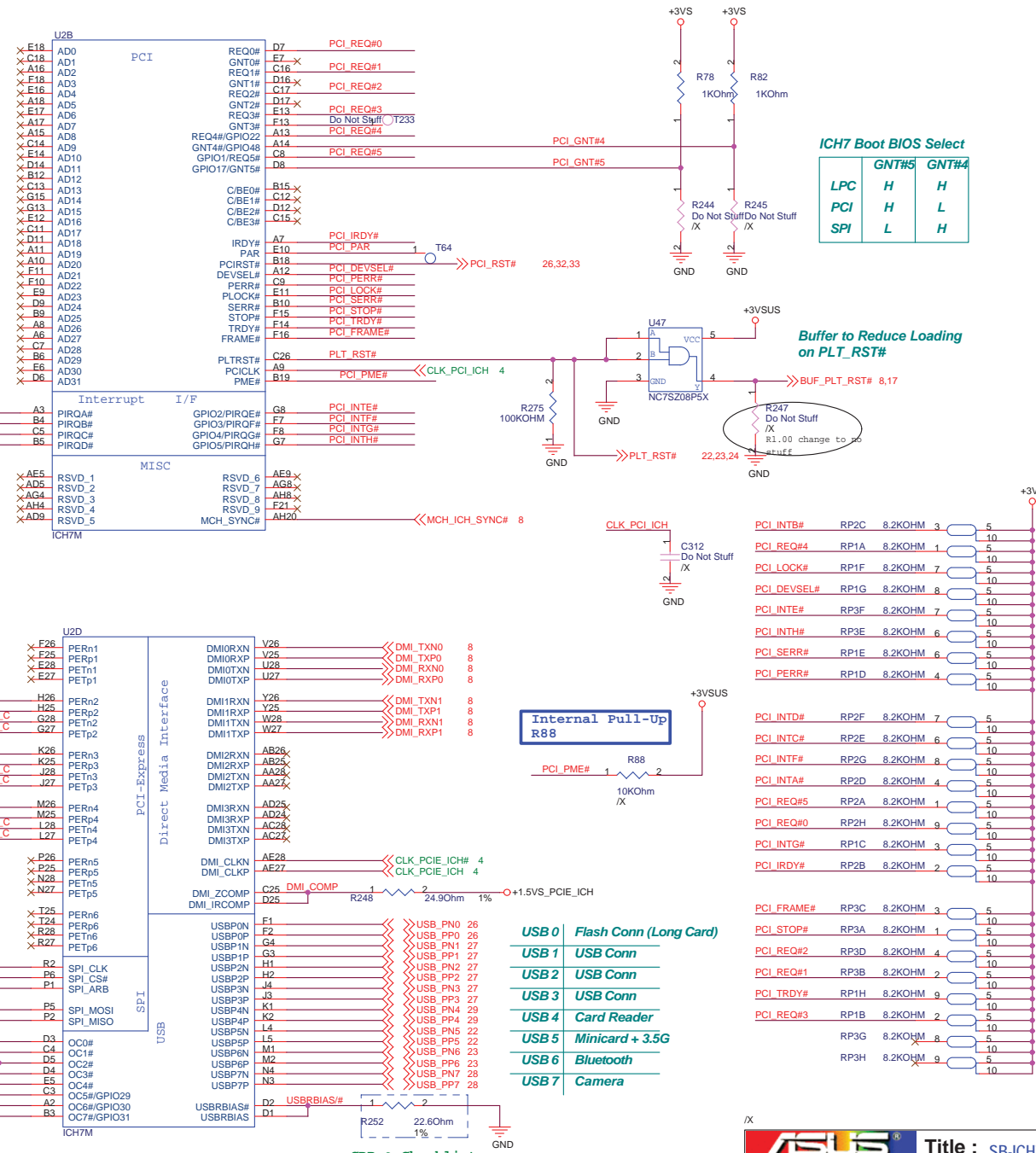
<http://hobi-elektronika.net>

		<b>Title :</b> NB-945PMS(GND)	
ASUSTeK COMPUTER INC.		<b>Engineer:</b> Satan_He	
Size	Project Name	Rev	
A3	<b>P901</b>	1.00G	
Date: Monday, March 31, 2008		Sheet	13 of 50







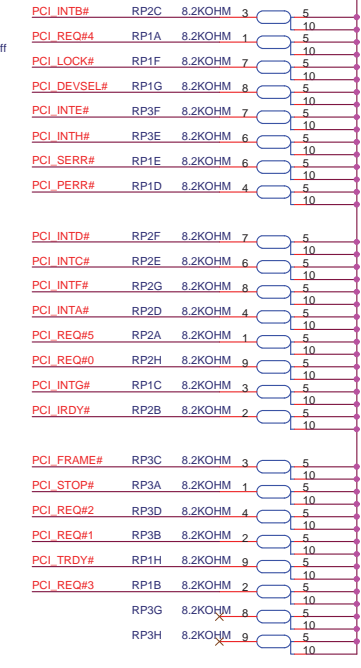


**ICH7 Boot BIOS Select**

	GNT#5	GNT#4
LPC	H	H
PCI	H	L
SPI	L	H

**Buffer to Reduce Loading on PLT\_RST#**

**Internal Pull-Up R88**

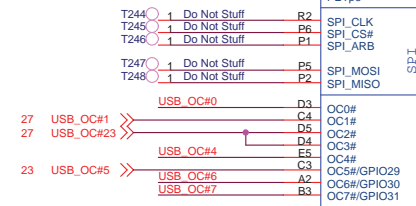
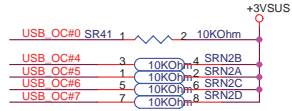


<b>ASUS</b>		<b>Title : SB-ICH7M(2)</b>	
ASUSTek COMPUTER INC.		Engineer: <b>Satan He</b>	
Size	Project Name		Rev
Custom	<b>P901</b>		1.00G
Date: Monday, March 31, 2008		Sheet 16 of 50	

LAN AR8113 IC

3.5G PCIExpress Card

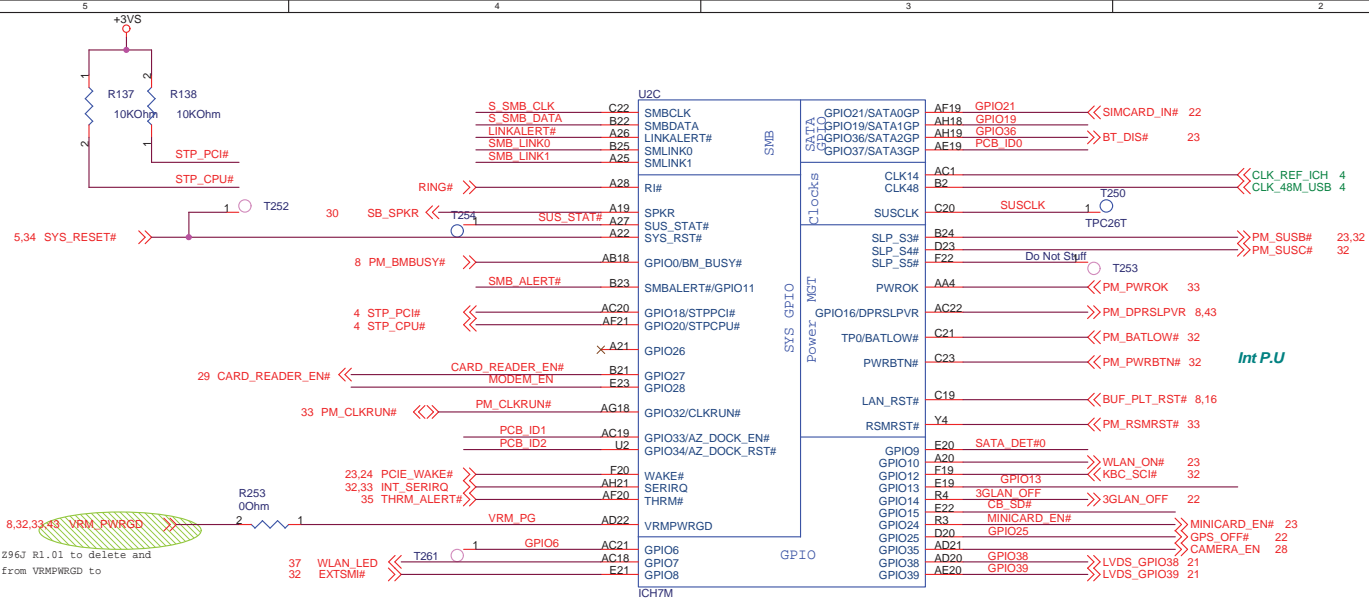
WIFI PCIExpress Card



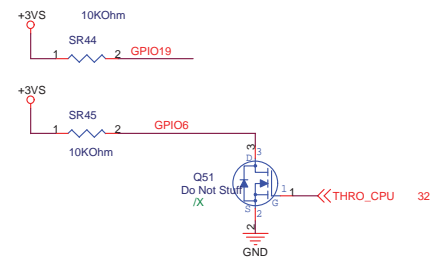
<http://hobi-elektronika.net>

CRB & Checklist



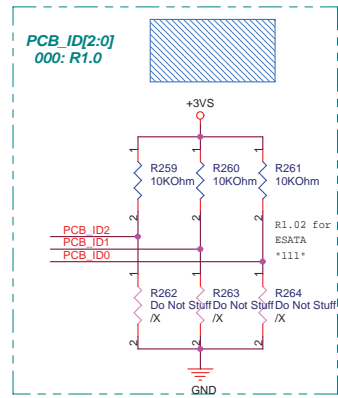
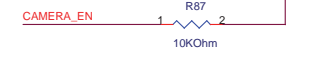
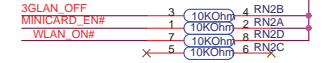
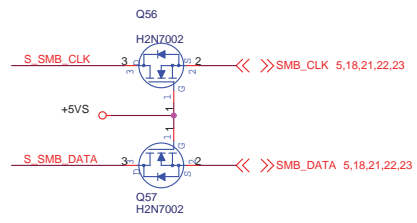


05/12/30, refer Z963 R1.01 to delete and change net name from VRMPWRGD to VRM\_PWRGD.

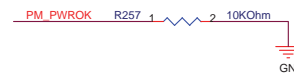
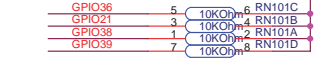
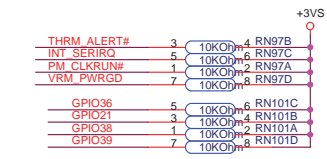
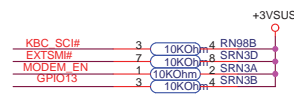
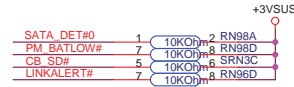
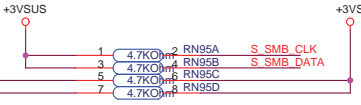


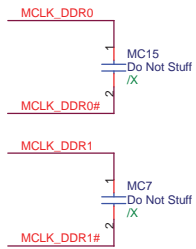
S SMB\_CLK <<> S SMB\_CLK 4  
S SMB\_DATA <<> S SMB\_DATA 4

WLAN_LED	WLAN	BT
High	v	v
High	v	x
High	x	v
Low	x	x



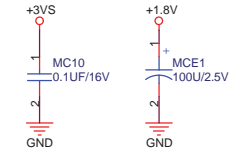
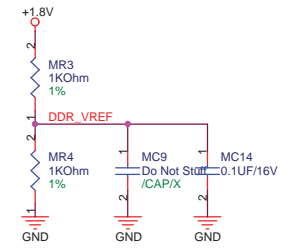
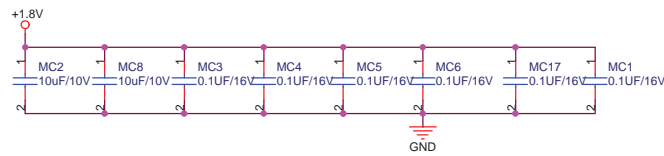
PCB\_VID3 : PROJECT CODE





STD Type

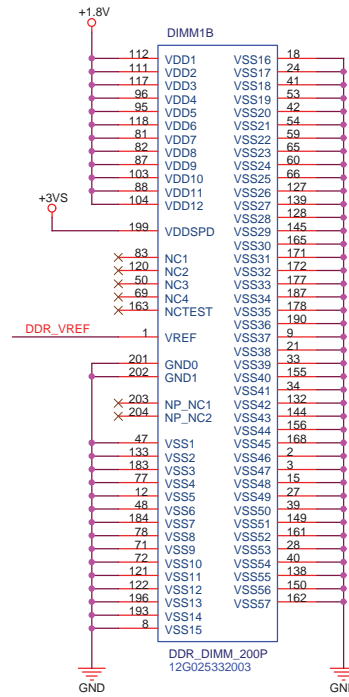
- MA\_DQ[63:0] 10
- MA\_DQS[7:0] 10
- MA\_DQS#[7:0] 10
- MA\_DM[7:0] 10
- MA\_MA[13:0] 10,19
- MA\_BA[2:0] 10,19



DIMM1A		DIMM1B	
MA_MA0	102	A0	DQ0
MA_MA1	101	A1	DQ1
MA_MA2	100	A2	DQ2
MA_MA3	99	A3	DQ3
MA_MA4	98	A4	DQ4
MA_MA5	97	A5	DQ5
MA_MA6	94	A6	DQ6
MA_MA7	92	A7	DQ7
MA_MA8	93	A8	DQ8
MA_MA9	91	A9	DQ9
MA_MA10	105	A10/AP	DQ10
MA_MA11	90	A11	DQ11
MA_MA12	89	A12	DQ12
MA_MA13	116	A13	DQ13
	X 86	A14	DQ14
	X 85	A15	DQ15
MA_BA2	X 84	A16_BA2	DQ16
	X 85		DQ17
MA_BA0	107	BA0	DQ18
MA_BA1	106	BA1	DQ19
	110	S0#	DQ20
8,19 MA_CS#0	X 115	S1#	DQ21
8,19 MA_CS#1	30	CK0#	DQ22
8 MCLK_DDR0#	32	CK0#	DQ23
8 MCLK_DDR1	164	CK1	DQ24
8 MCLK_DDR1#	166	CK1#	DQ25
	79	CKE0	DQ26
8,19 MA_CKE0	80	CKE1	DQ27
8,19 MA_CKE1	113	CAS#	DQ28
10,19 MA_CAS#	108	RAS#	DQ29
10,19 MA_RAS#	109	WE#	DQ30
10,19 MA_WE#	198	SA0	DQ31
	200	SA1	DQ32
5,17,21,22,23 SMB_CLK	X 197	SCL	DQ33
5,17,21,22,23 SMB_DATA	X 195	SDA	DQ34
	114	ODT0	DQ35
8,19 MA_ODT0	X 119	ODT1	DQ36
8,19 MA_ODT1			DQ37
	10	DM0	DQ38
MA_DM0	26	DM1	DQ39
MA_DM2	52	DM2	DQ40
MA_DM3	67	DM3	DQ41
MA_DM4	130	DM4	DQ42
MA_DM5	147	DM5	DQ43
MA_DM6	170	DM6	DQ44
MA_DM7	185	DM7	DQ45
	13	DQS0	DQ46
MA_DQS0	31	DQS1	DQ47
MA_DQS2	51	DQS2	DQ48
MA_DQS3	70	DQS3	DQ49
MA_DQS4	131	DQS4	DQ50
MA_DQS5	148	DQS5	DQ51
MA_DQS6	169	DQS6	DQ52
MA_DQS7	188	DQS7	DQ53
	11	DQS#0	DQ54
MA_DQS#0	29	DQS#1	DQ55
MA_DQS#1	49	DQS#2	DQ56
MA_DQS#2	68	DQS#3	DQ57
MA_DQS#3	129	DQS#4	DQ58
MA_DQS#4	146	DQS#5	DQ59
MA_DQS#5	167	DQS#6	DQ60
MA_DQS#6	186	DQS#7	DQ61
		DQ62	DQ62
		DQ63	DQ63

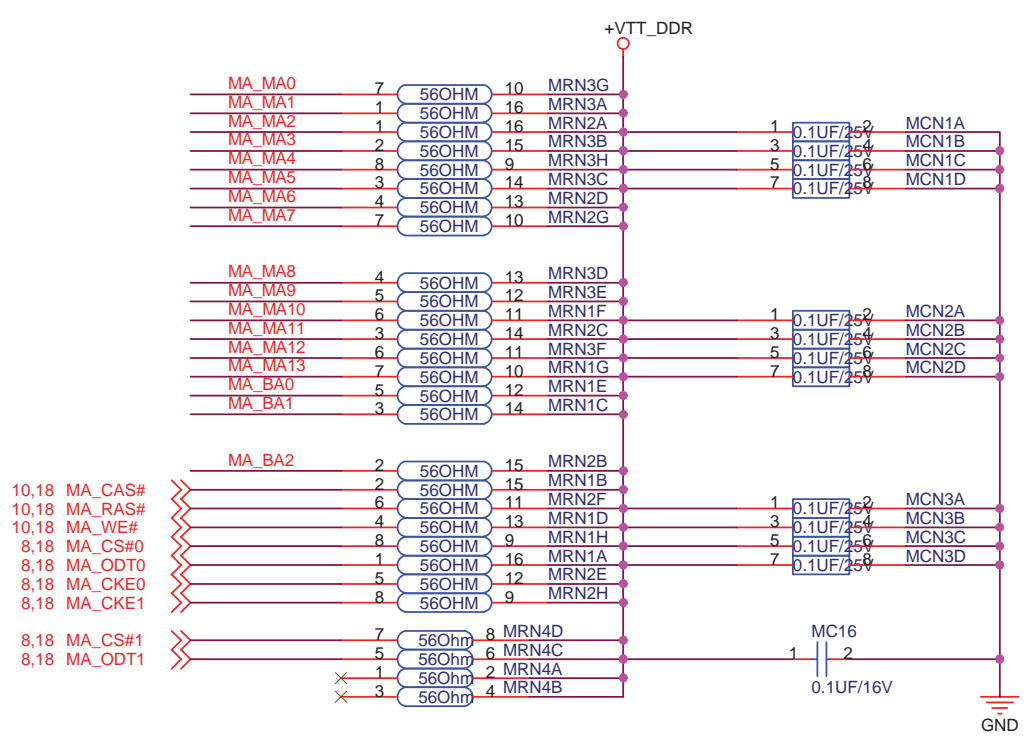
DDR\_DIMM\_200P  
12G025332003

GROUP1  
GROUP2  
SWAP



DDR\_DIMM\_200P  
12G025332003

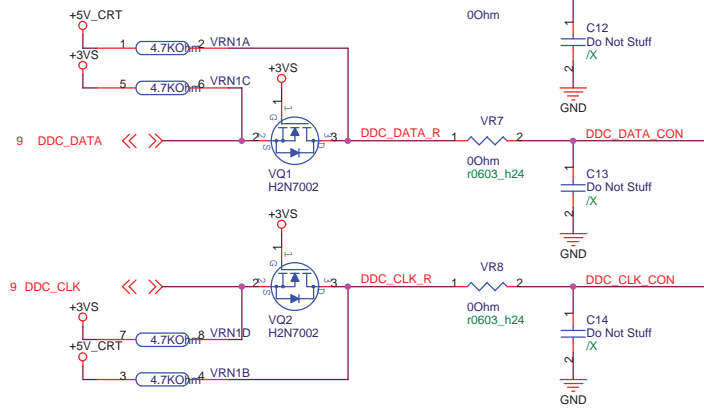
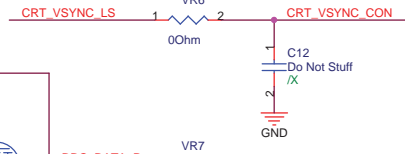
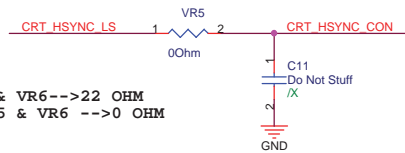
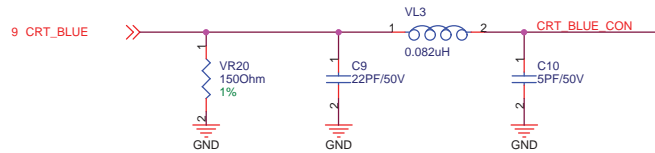
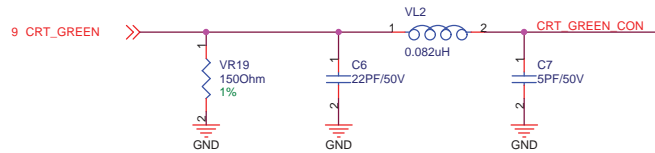
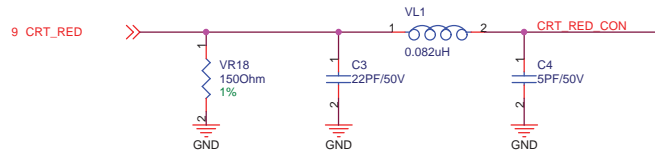
<< MA\_MA[13:0] 10,18  
<< MA\_BA[2:0] 10,18



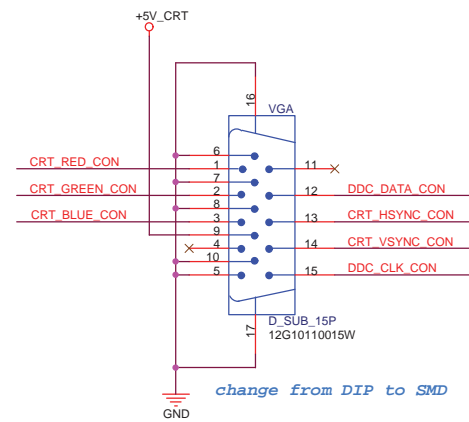
<http://hobi-elektronika.net>

/X

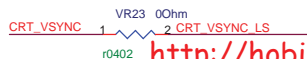
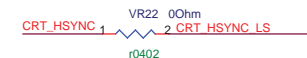
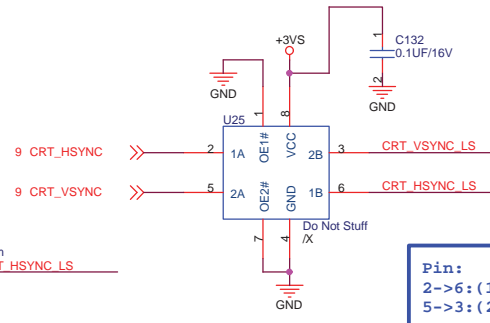
<b>ASUS</b>		<b>Title : DDR2_Termination</b>	
ASUSTek Computer INC.		Engineer: <i>Kell_Huang</i>	
Size A4	Project Name <b>P901</b>		Rev 1.00G
Date: Monday, March 31, 2008		Sheet 19 of 47	



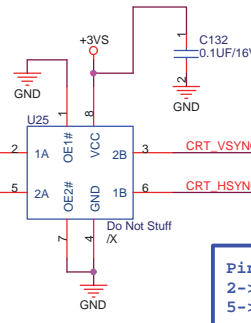
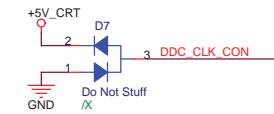
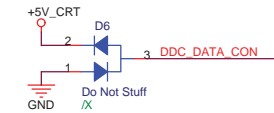
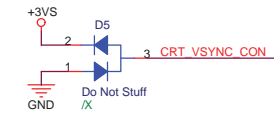
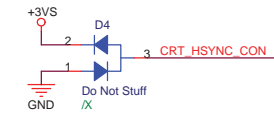
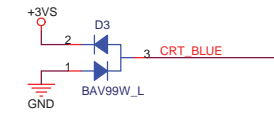
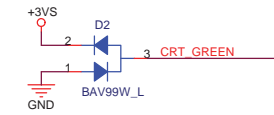
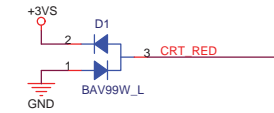
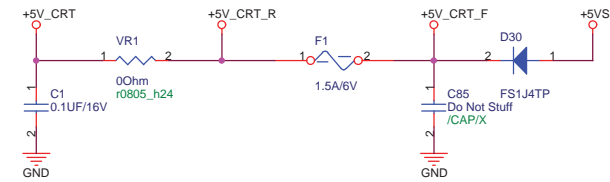
U25上:VR5 & VR6-->22 OHM  
U25 /X :VR5 & VR6 -->0 OHM



VGA use 12G10110015W & 12G10110015N

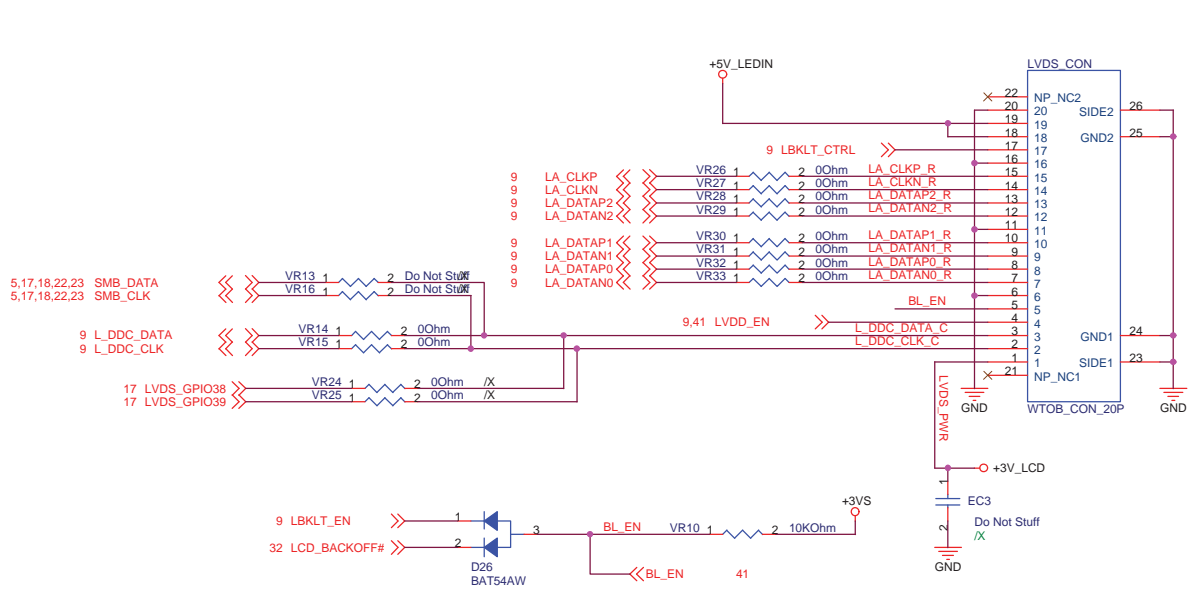


<http://hobi-elektronika.net>

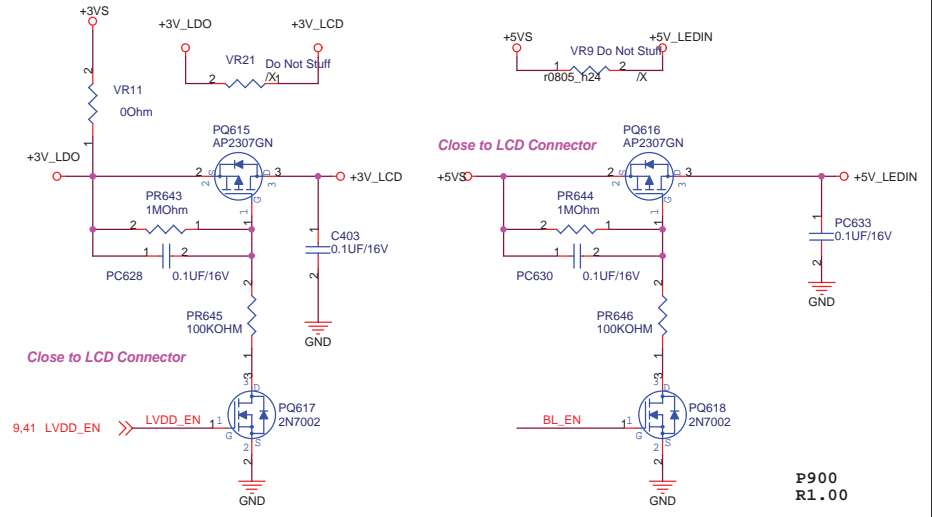
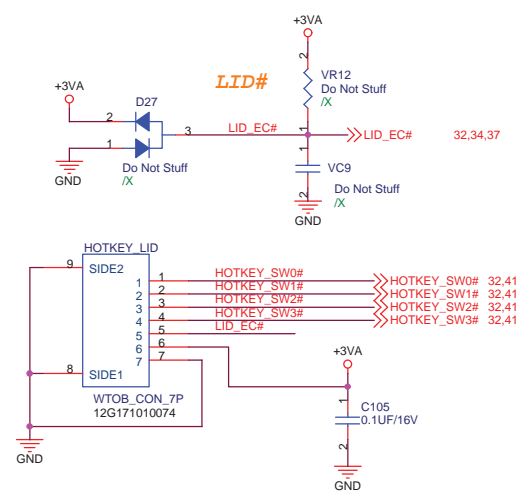


Pin:  
2->6: (1A->1B)  
5->3: (2A->2B)

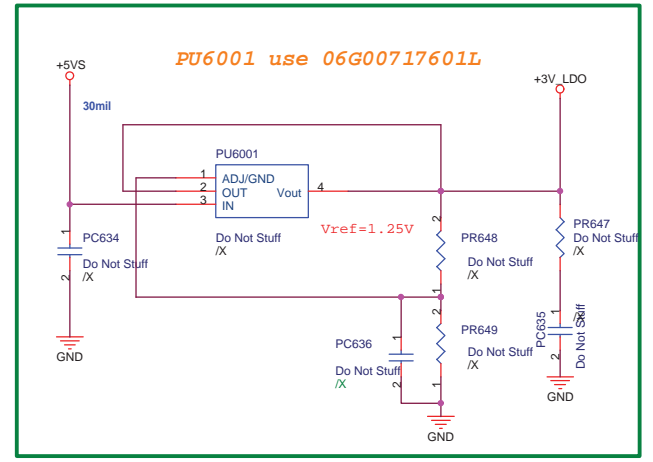
<b>ASUS</b>		<b>Title : Onboard VGA</b>	
ASUSTek Computer INC.		Engineer: <b>Kell Huang</b>	
Size A3	Project Name <b>P901</b>	Rev 1.00G	
Date: Monday, March 31, 2008	Sheet	20 of 47	



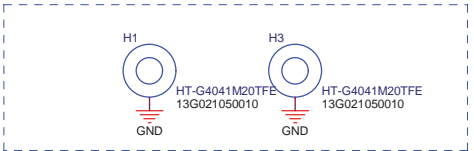
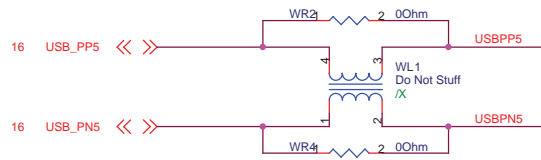
L_DDC_CLK_C	EC1	2	1	Do Not Stuff
L_DDC_DATA_C	EC2	2	1	Do Not Stuff
LA_CLKP_R	VC1	2	1	Do Not Stuff
LA_CLKN_R	VC2	2	1	Do Not Stuff
LA_DATAP2_R	VC3	2	1	Do Not Stuff
LA_DATAN2_R	VC4	2	1	Do Not Stuff
LA_DATAP1_R	VC5	2	1	Do Not Stuff
LA_DATAN1_R	VC6	2	1	Do Not Stuff
LA_DATAP0_R	VC7	2	1	Do Not Stuff
LA_DATAN0_R	VC8	2	1	Do Not Stuff



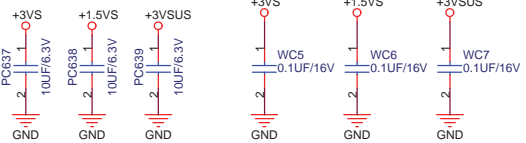
P900  
R1.00



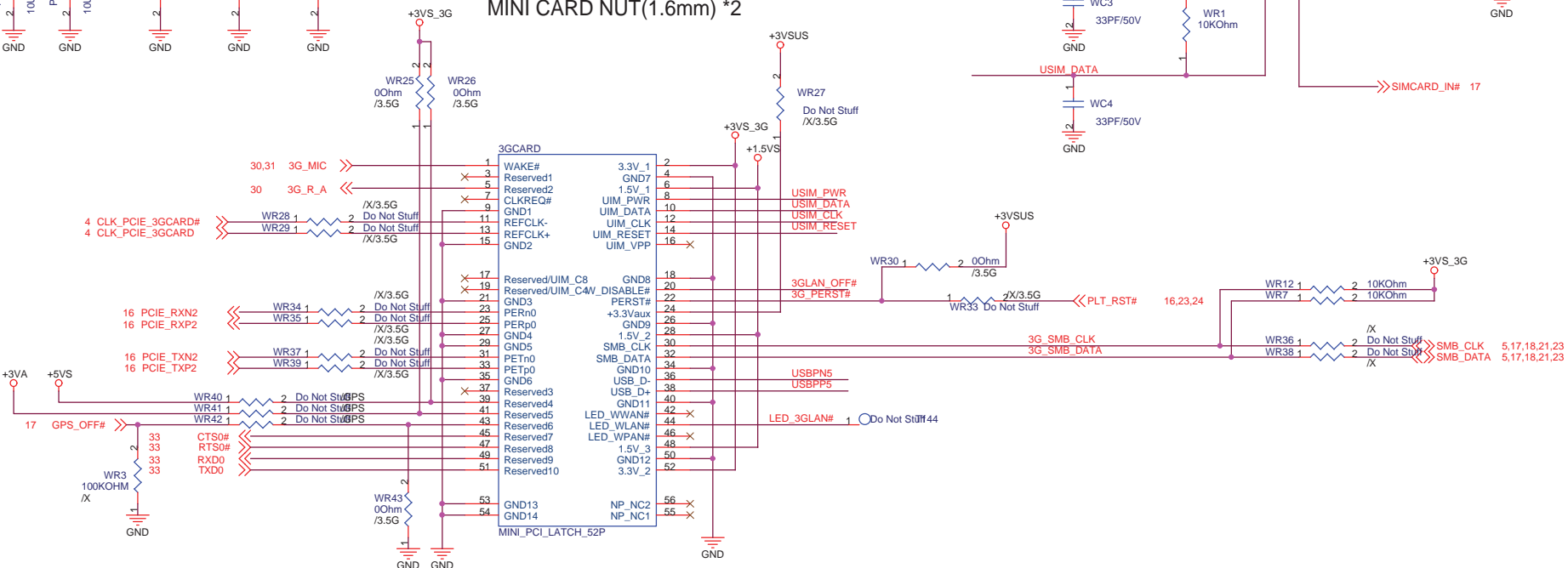
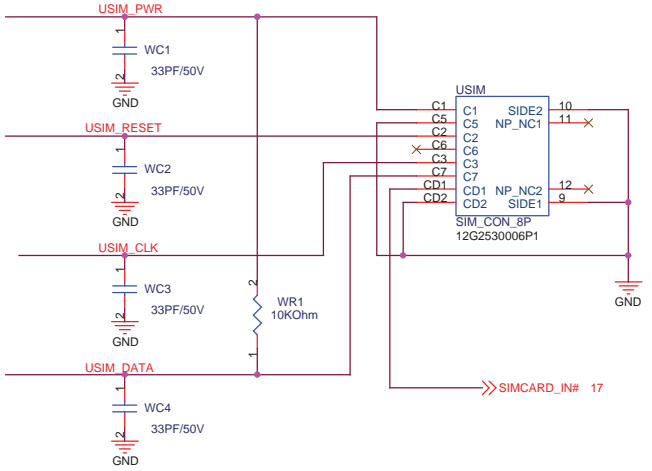
<http://hobi-elektronika.net>



MINI CARD NUT(1.6mm) \*2

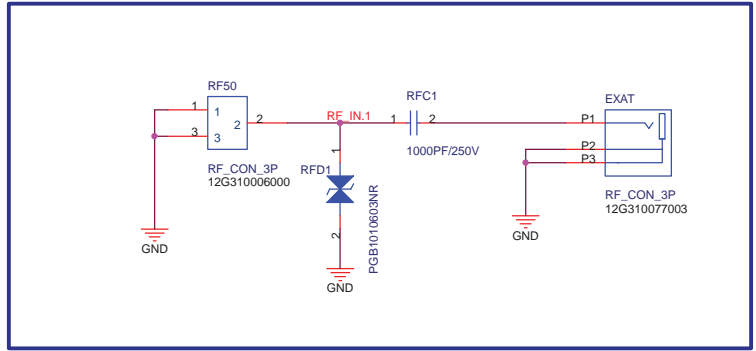


CAP  
Near  
SIM  
Socket

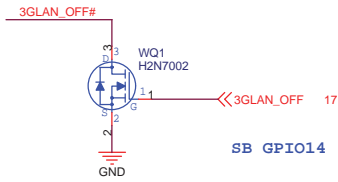
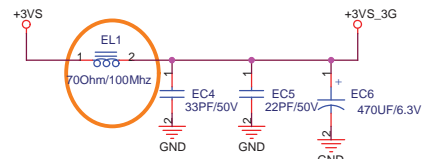


MINICARD use 12G03010052Q

External Antenna



2008/03/11 change



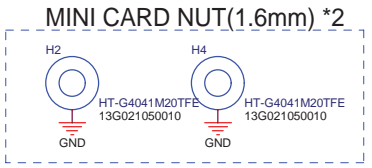
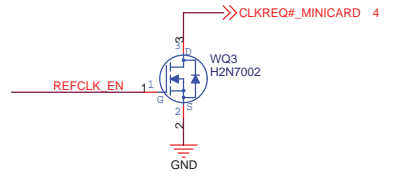
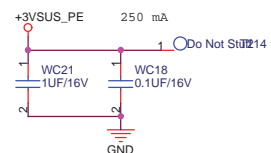
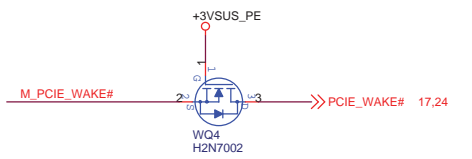
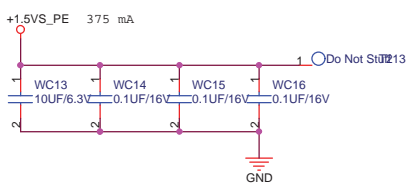
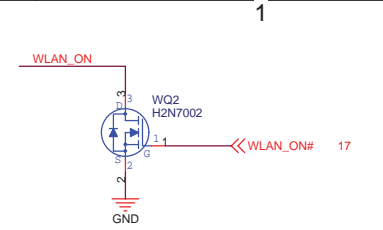
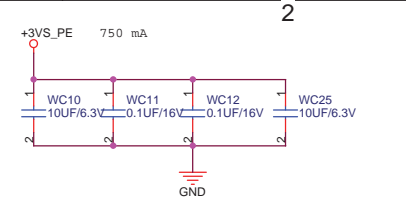
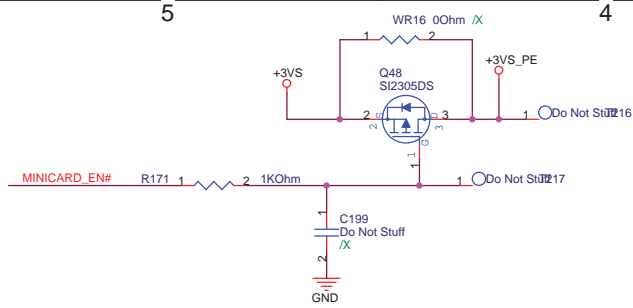
<http://hobi-elektronika.net>

3.5G Module & External Antenna

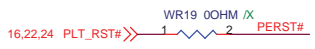
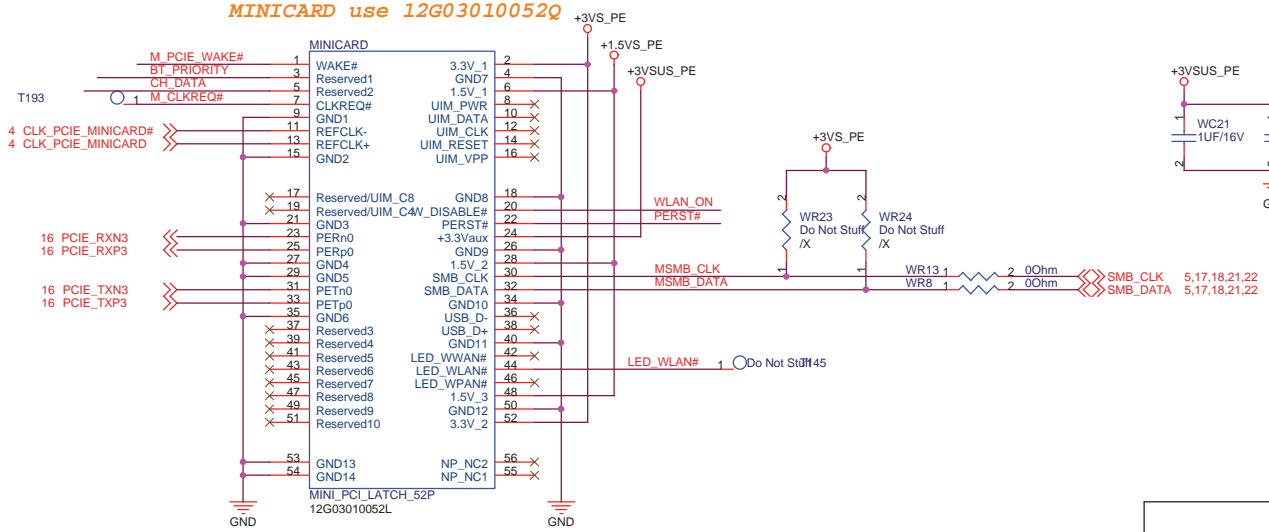
**ASUS** Title : **Kell Huang**

ASUSTek Computer INC. Engineer: **Kell Huang**

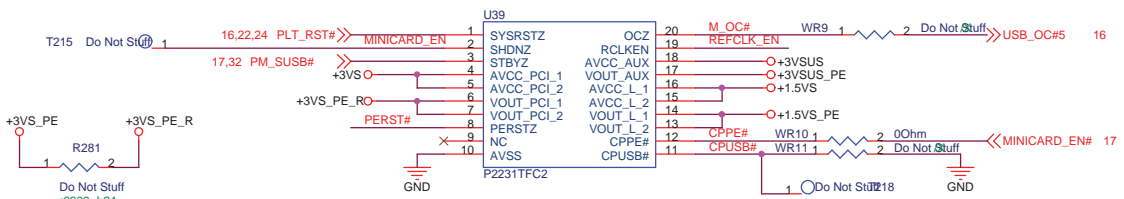
Size	Project Name	Rev
A3	<b>P901</b>	1.00G
Date: Monday, March 31, 2008	Sheet 22 of 47	



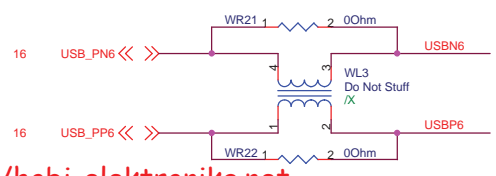
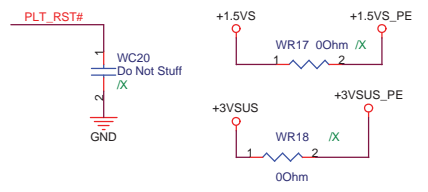
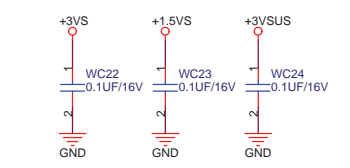
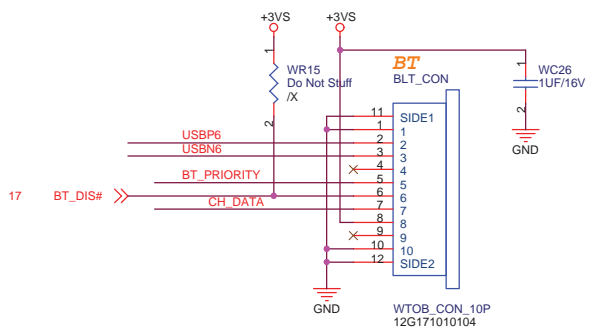
MINICARD use 12G03010052Q



U39 use 06G030057011

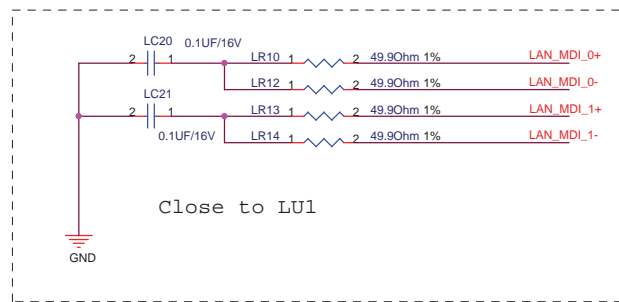
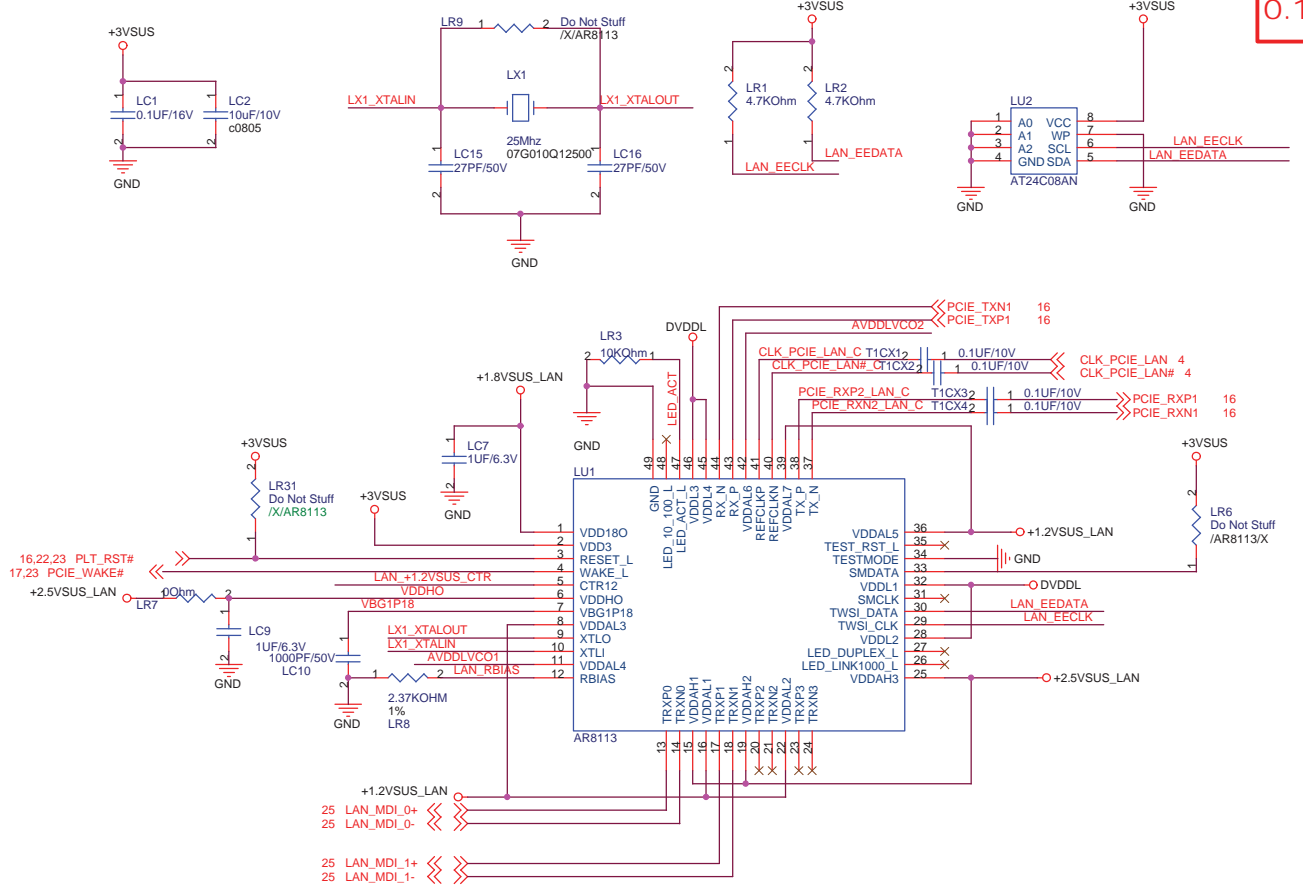
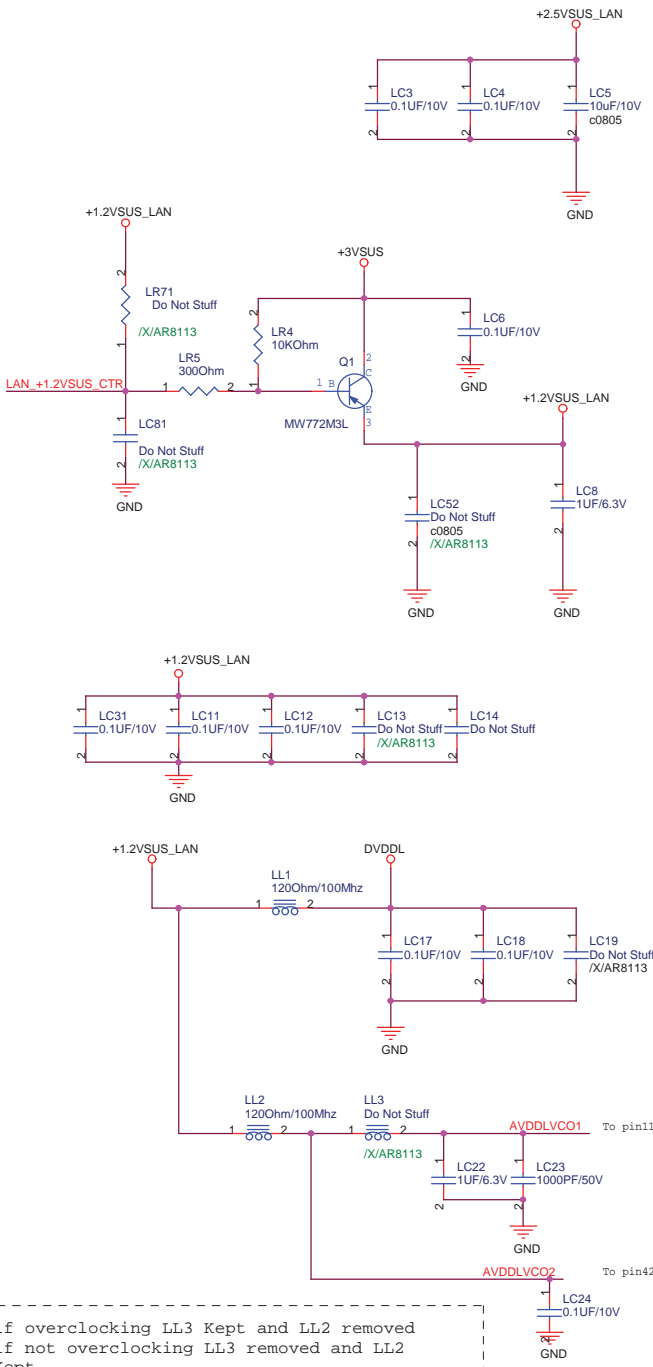


BlueTooth



		Title : Minicard	
ASUSTek Computer INC.		Engineer: Tiansen_Wu	
Size A3	Project Name P901	Rev 1.00	
Date: Monday, March 31, 2008	Sheet 23 of 50		

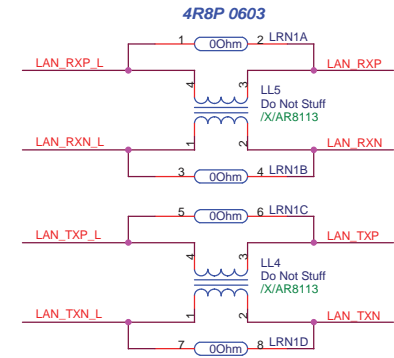
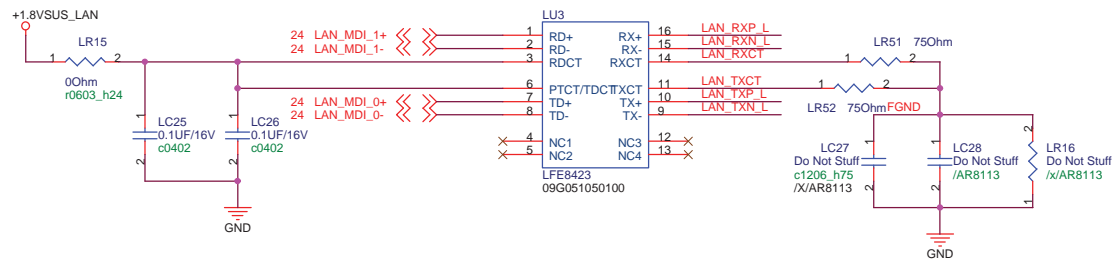
<http://hobi-elektronika.net>



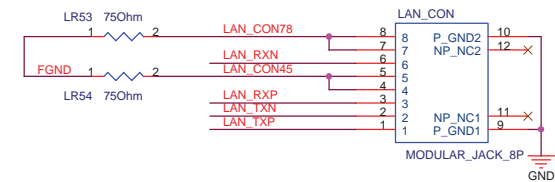
Close to LU1

if overclocking LL3 Kept and LL2 removed  
if not overclocking LL3 removed and LL2 Kept

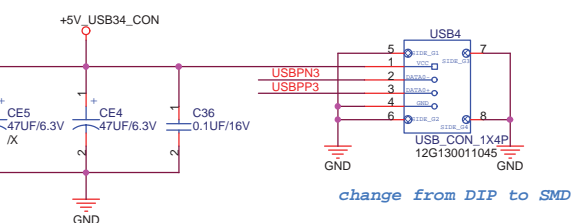
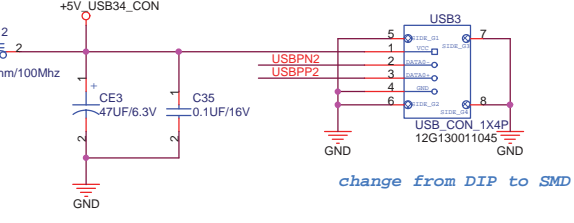
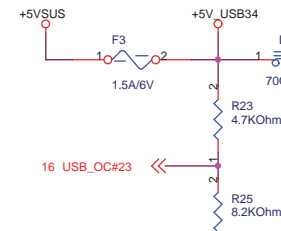
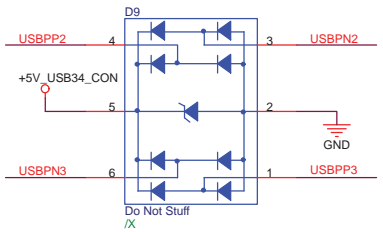
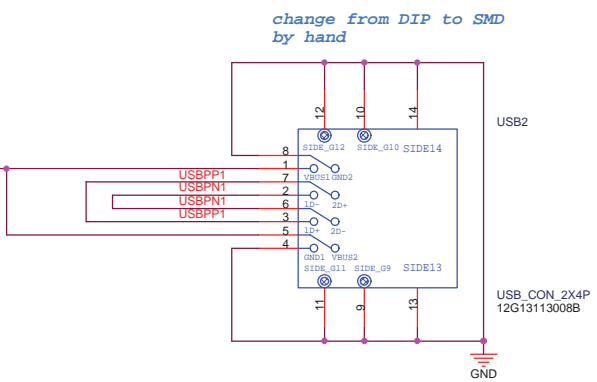
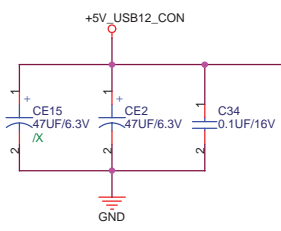
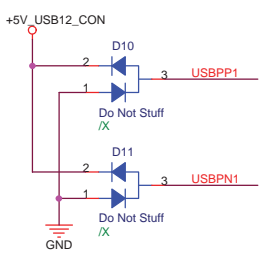
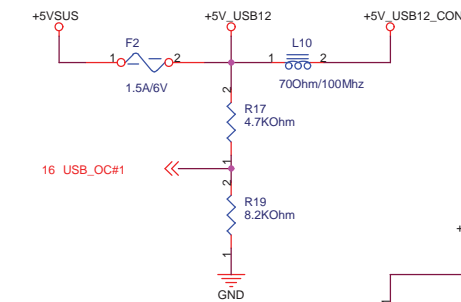
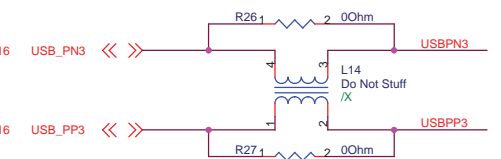
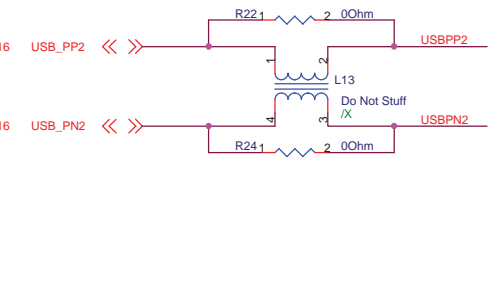




LAN connector: 12G148301086

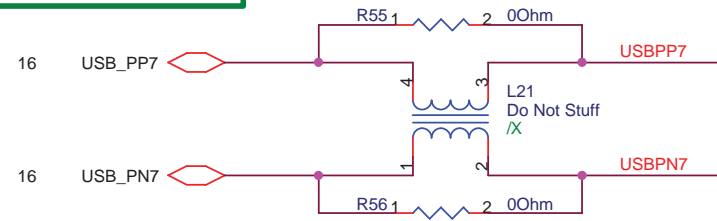
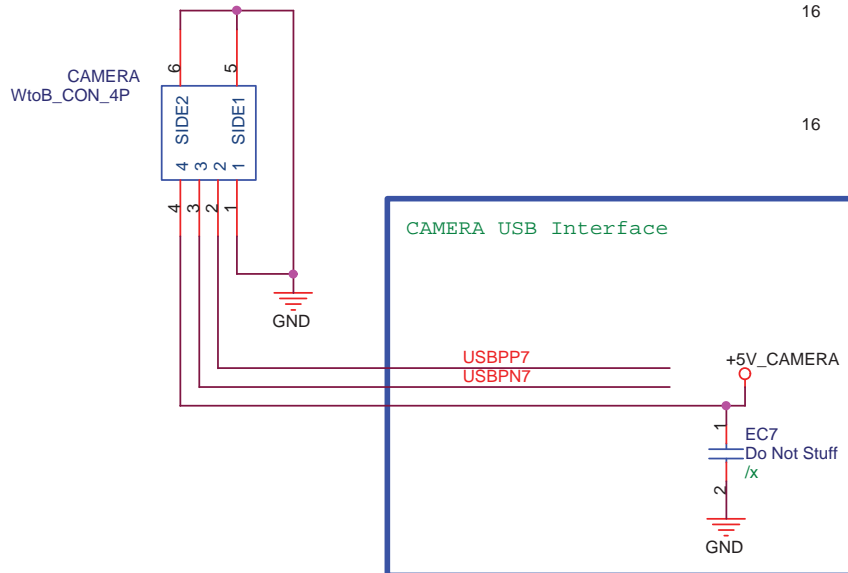
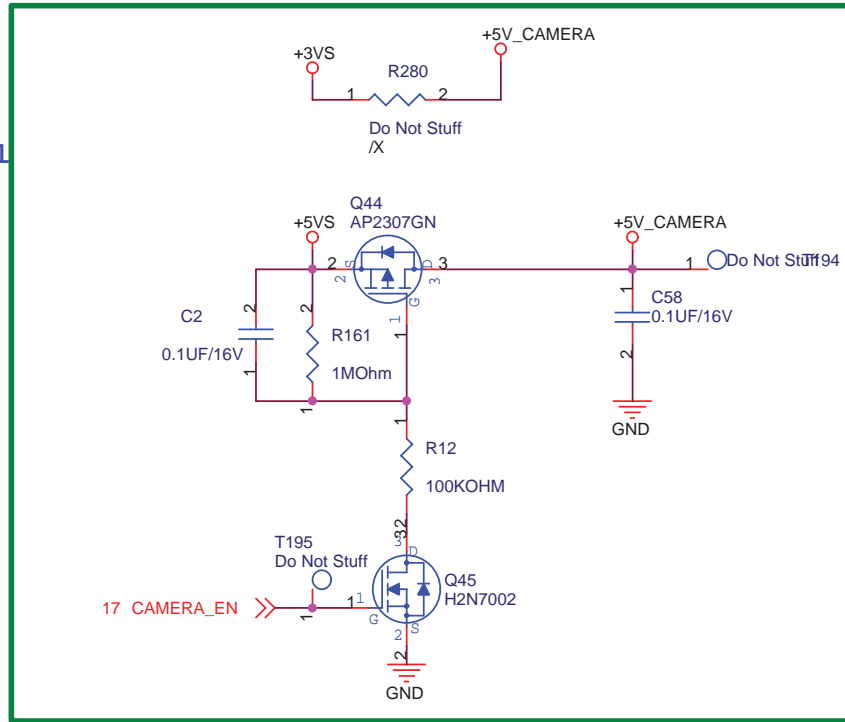






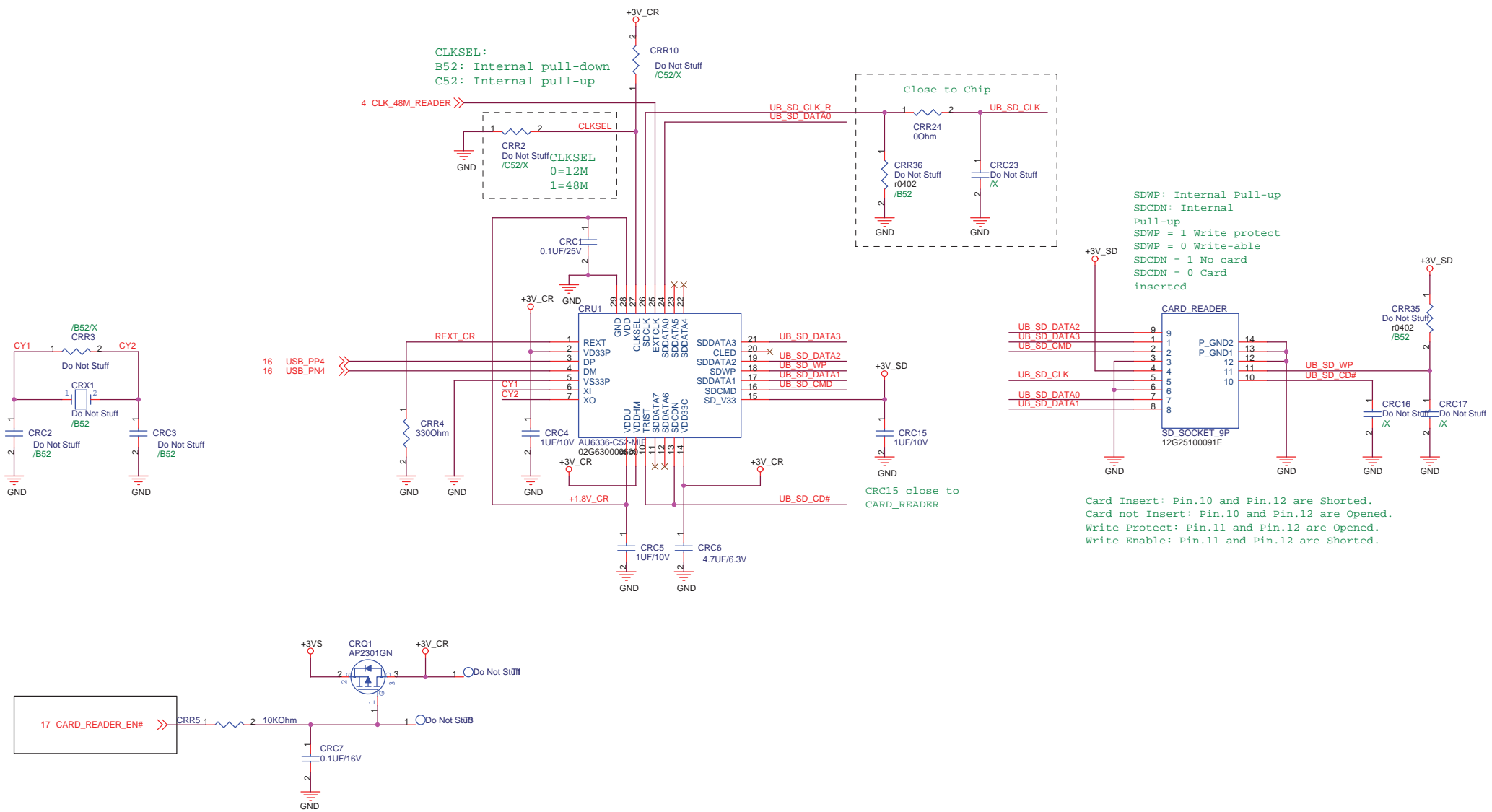
<b>ASUS</b>		<b>Title : USB Port</b>	
ASUSTek Computer INC.		Engineer: <i>Kell_Huang</i>	
Size A3	Project Name <b>P901</b>	Date: Monday, March 31, 2008	Rev 1.00G
Sheet 27 of 47			

Power Control



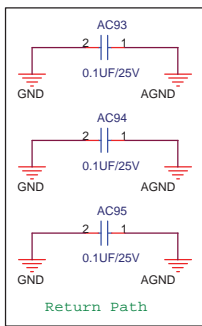
<http://hobi-elektronika.net>

<b>ASUS</b>		<b>Title : Camera Power</b>	
ASUSTek Computer INC.		Engineer: <i>Kell_Huang</i>	
Size A4	Project Name <b>P901</b>	Rev 1.00G	
Date: Monday, March 31, 2008		Sheet 28 of 47	

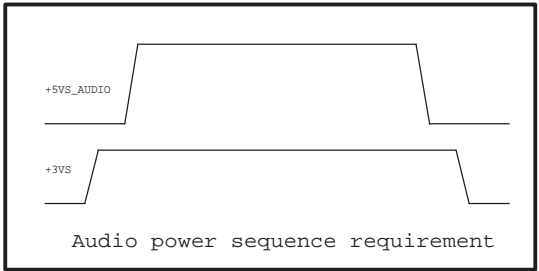
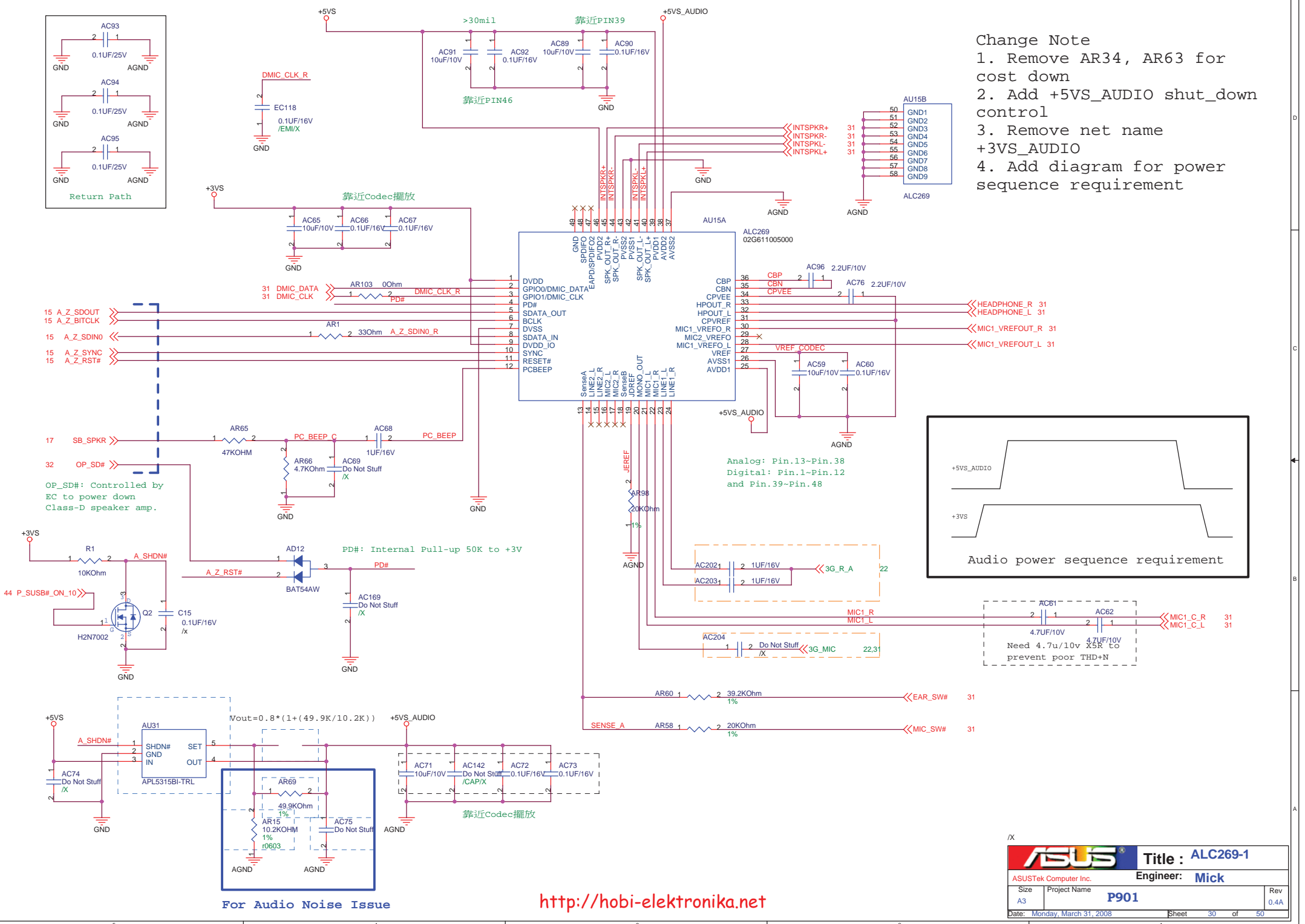


SDWP: Internal Pull-up  
 SDCDN: Internal  
 Pull-up  
 SDWP = 1 Write protect  
 SDWP = 0 Write-able  
 SDCDN = 1 No card  
 SDCDN = 0 Card inserted

Card Insert: Pin.10 and Pin.12 are Shorted.  
 Card not Insert: Pin.10 and Pin.12 are Opened.  
 Write Protect: Pin.11 and Pin.12 are Opened.  
 Write Enable: Pin.11 and Pin.12 are Shorted.

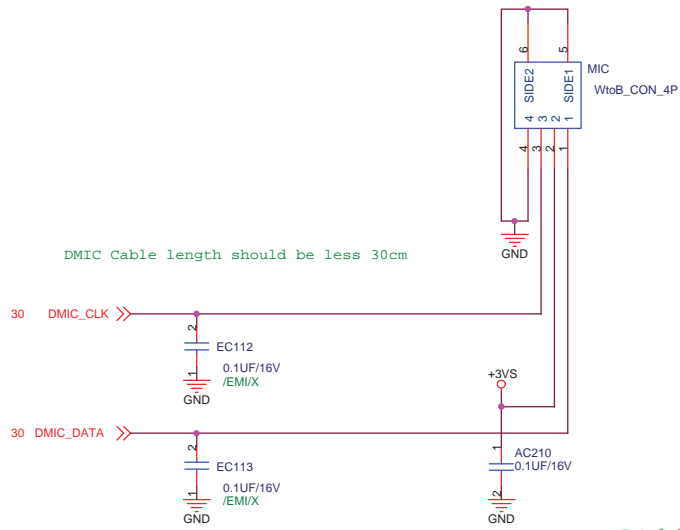


- Change Note
1. Remove AR34, AR63 for cost down
  2. Add +5VS\_AUDIO shut\_down control
  3. Remove net name +3VS\_AUDIO
  4. Add diagram for power sequence requirement

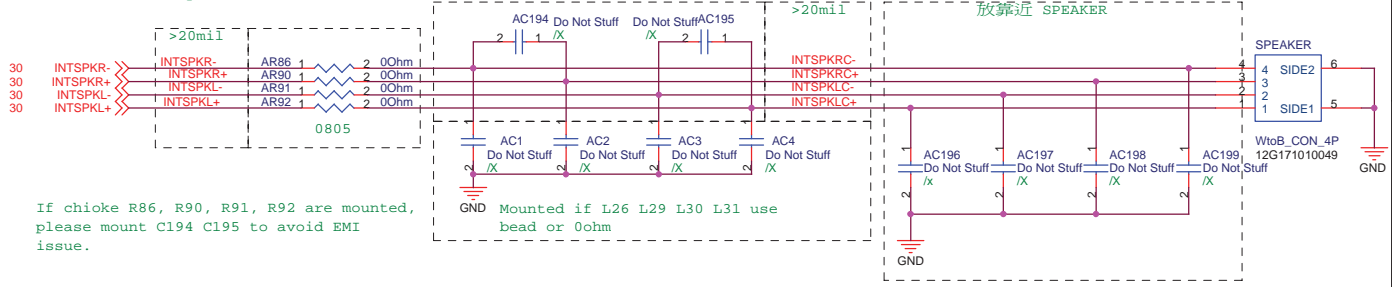


Need 4.7u/10v X5R to prevent poor THD+N

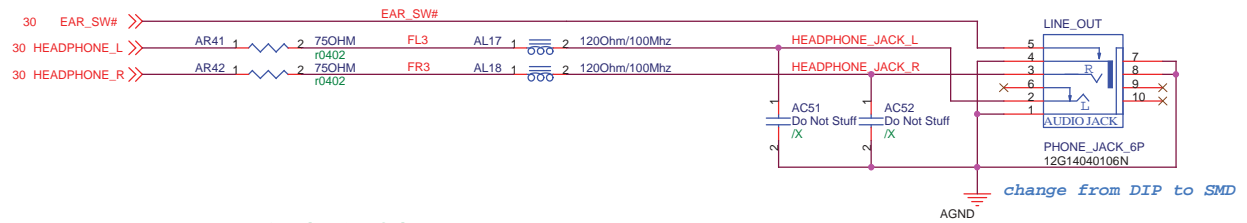
<http://hobi-elektronika.net>



Total length from speakerR+- L+- (pin40 41 44 45) to internal speaker please as short as possible (<20cm is better)

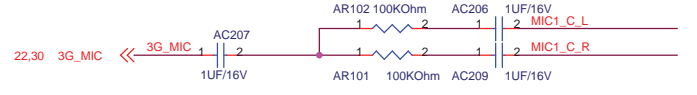
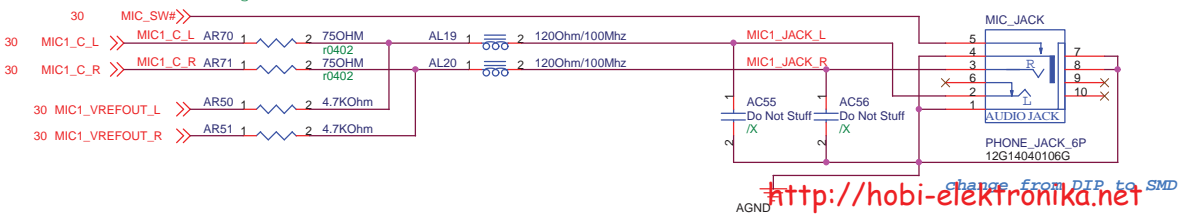


**LINE\_OUT use 12G14040106N**



R70 and R71: If don't need retasking function, change to 1K.

**MIC\_JACK use 12G14040106G**

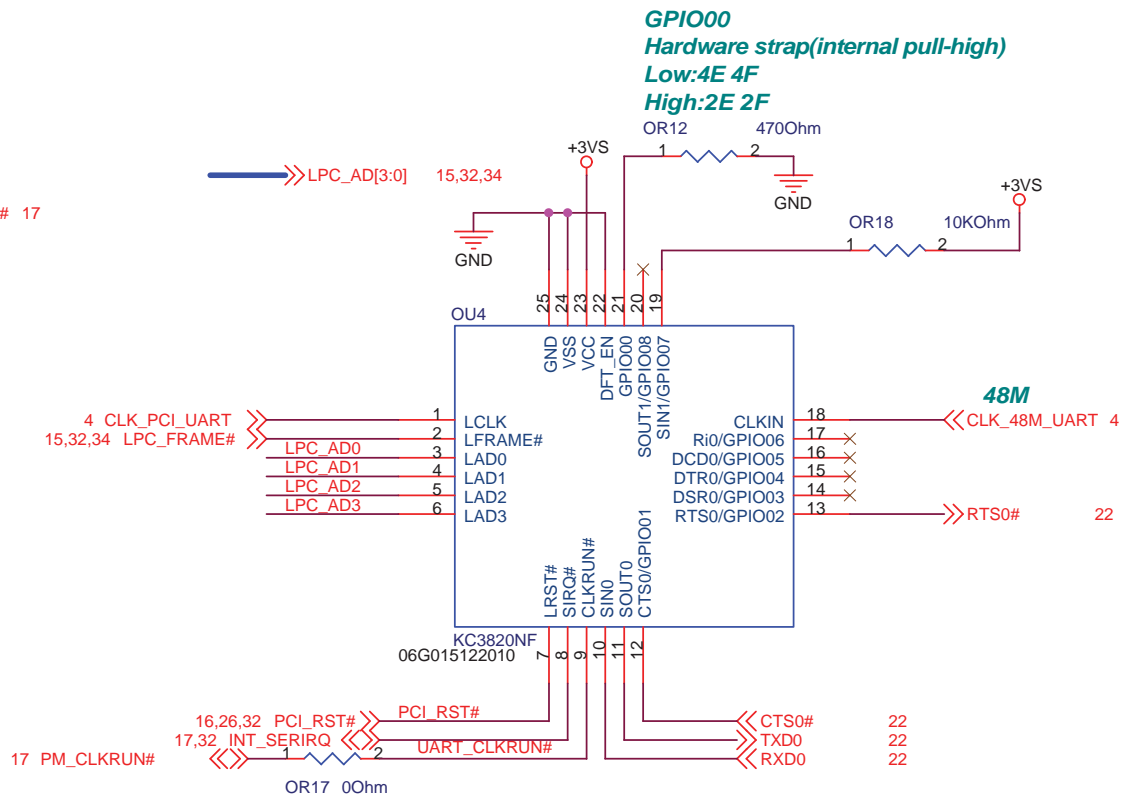
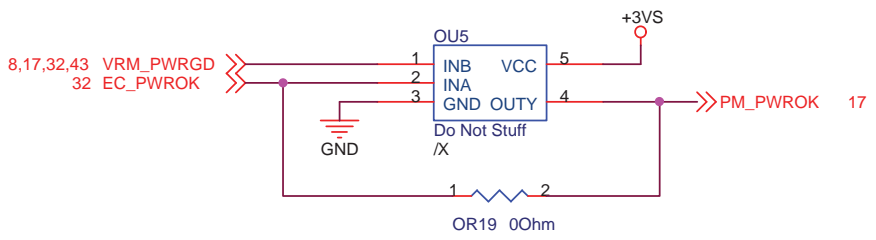
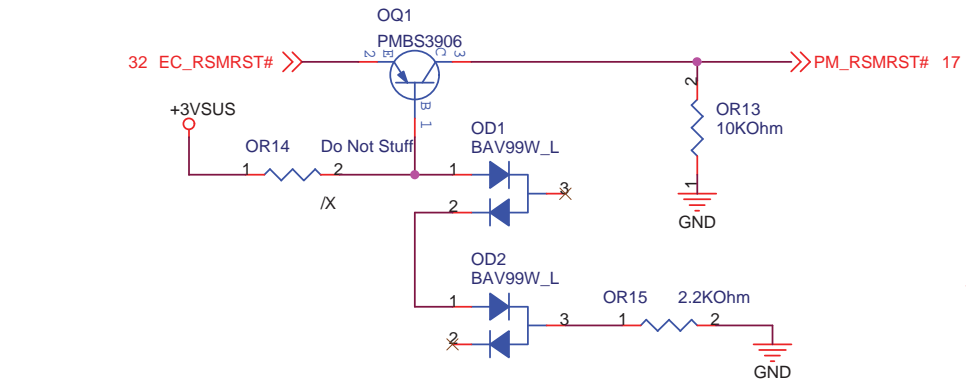


<http://hobi-elektronika.net>

<b>ASUS</b>		<b>Title : ALC269-2</b>	
ASUSTek Computer Inc.		Engineer: MICK	
Size A3	Project Name <b>P901</b>	Rev 0.4A	
Date: Monday, March 31, 2008	Sheet	31	of 50



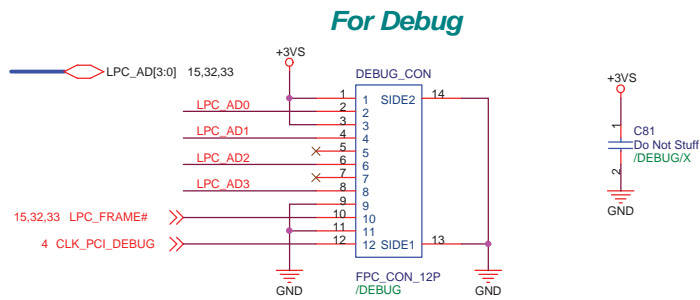
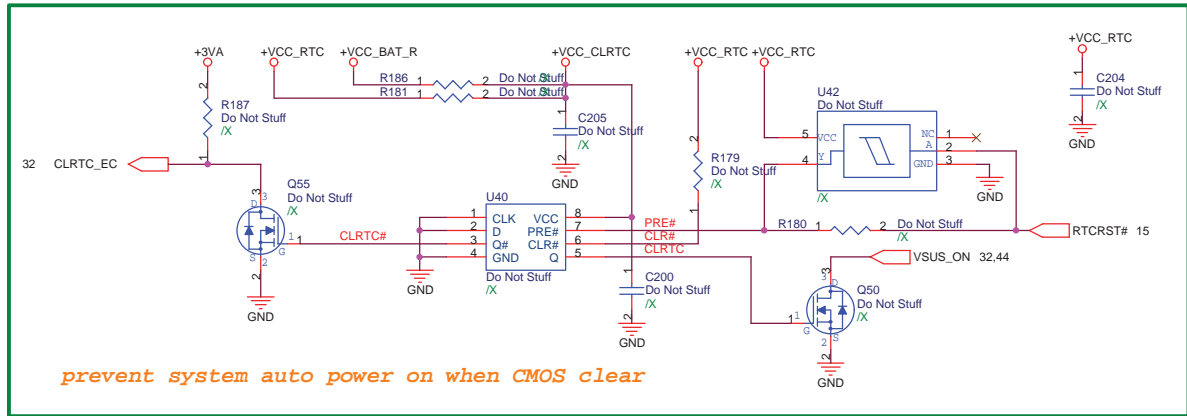
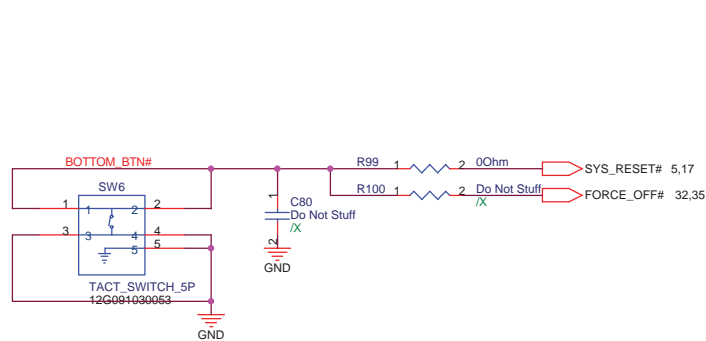
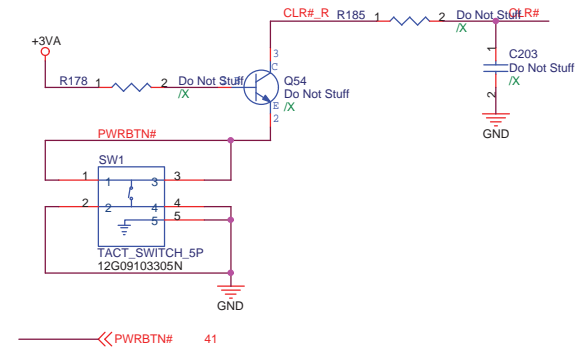
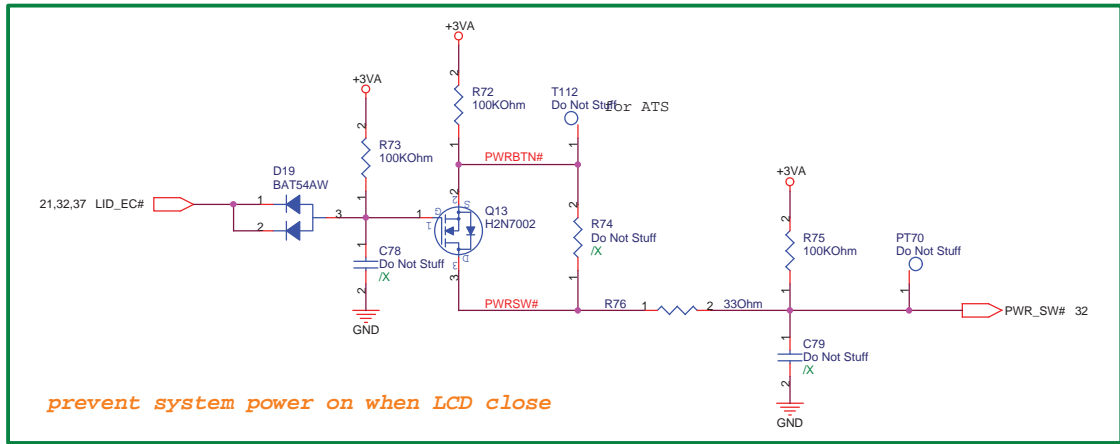




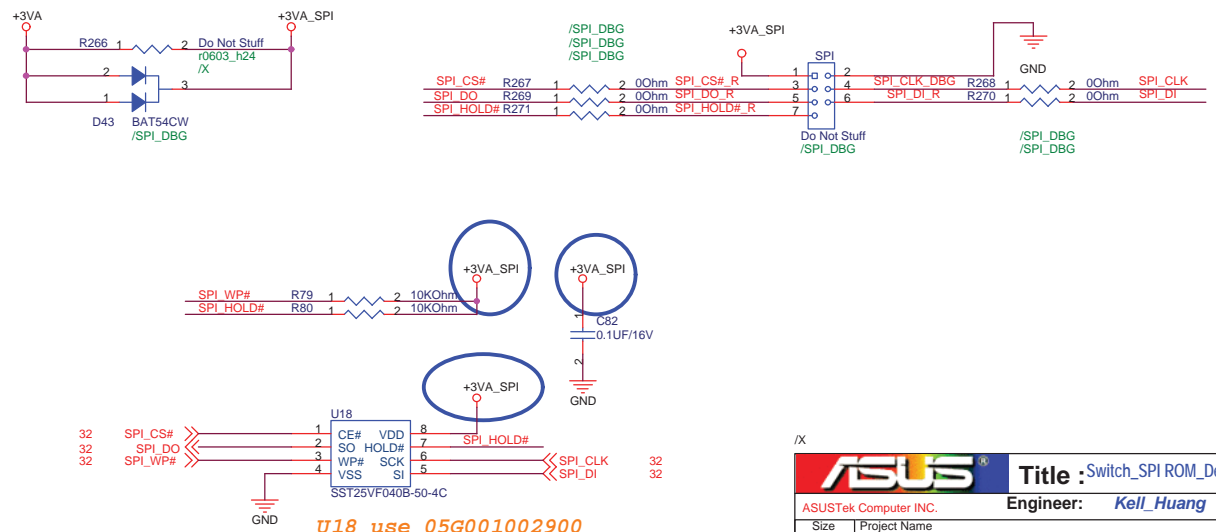
<http://hobi-elektronika.net>

UART Control  
IC for using  
GPS module due  
to no UART on  
ENE EC

		<b>Title :</b> EC_UART_KC3820	
ASUSTek Computer INC.		<b>Engineer:</b> Kell Huang	
Size A4	Project Name <b>P901</b>	Rev 1.4G	
Date: Monday, March 31, 2008		Sheet 33 of 50	

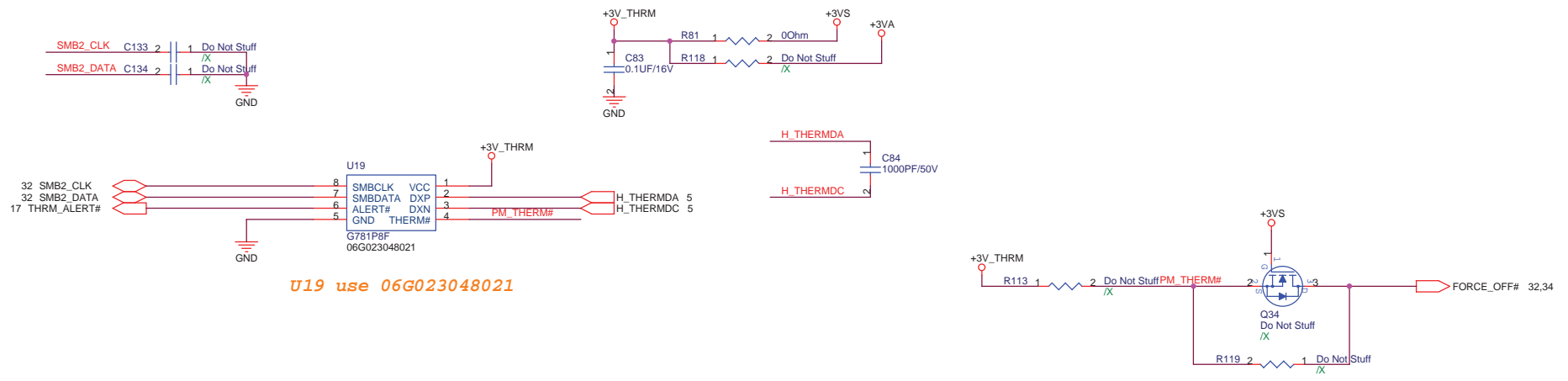


Debug Card cable use Z96 Touch Pad cable, P/N:  
 14G124110126, 14G124110120, 14G124110121  
 14G124110124, 14G124110125

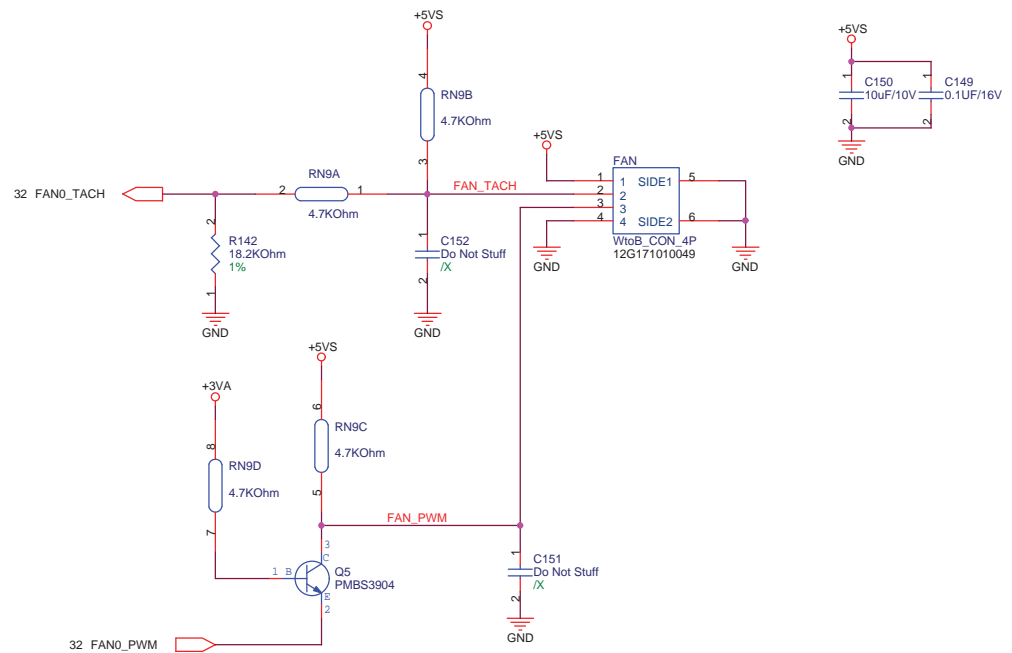


<b>ASUS</b>		Title : Switch_SPI ROM_Debug	
ASUSTek Computer INC.		Engineer: <i>Keil Huang</i>	
Size	Project Name		Rev
A3	P901		1.00G
Date: Monday, March 31, 2008	Sheet	34 of 47	

<http://hobi-elektronika.com>



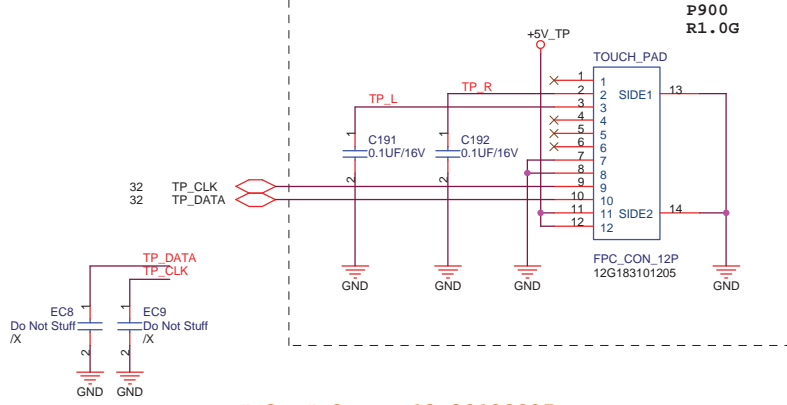
U19 use 06G023048021



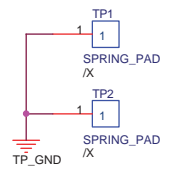
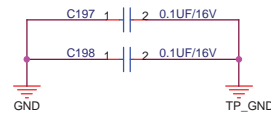
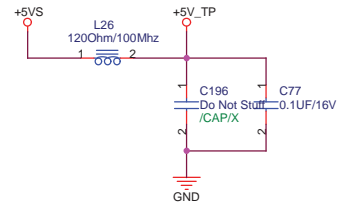
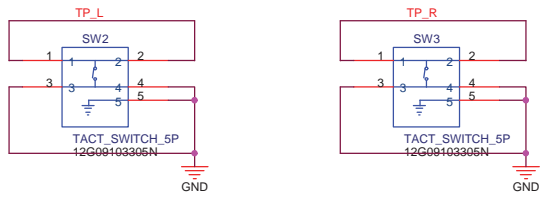
<http://hobi-elektronika.net>

<b>ASUS</b>		<b>Title : Thermal Sensor_FAN</b>	
ASUSTek Computer INC.		Engineer: <i>Kell_Huang</i>	
Size	Project Name	Rev	
A3	<b>P901</b>	1,00G	
Date: Monday, March 31, 2008	Sheet	35 of 47	

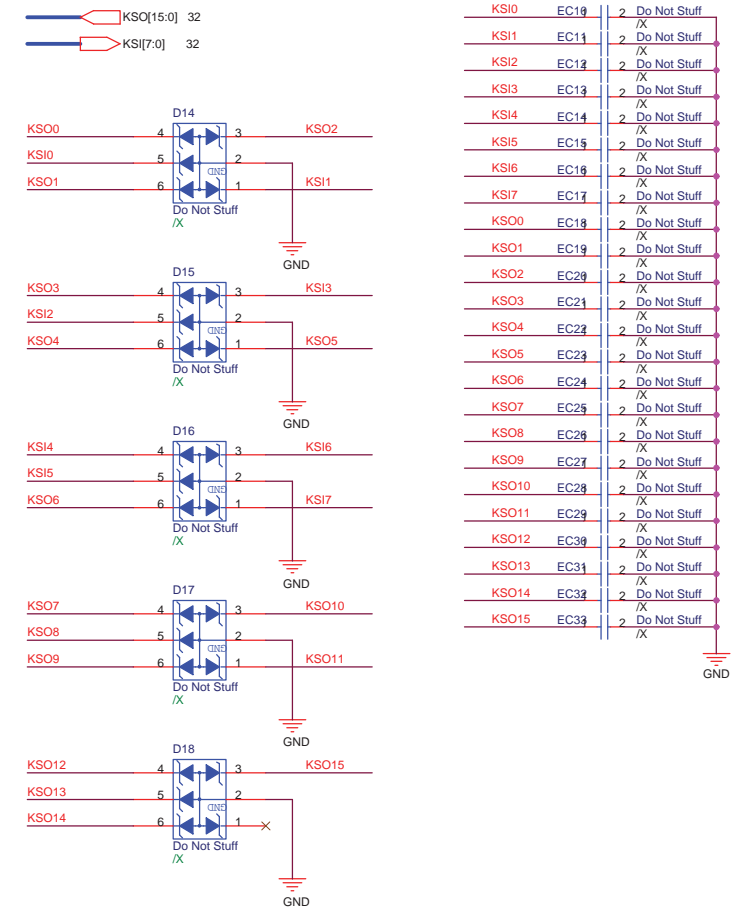
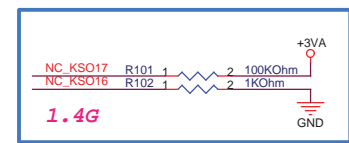
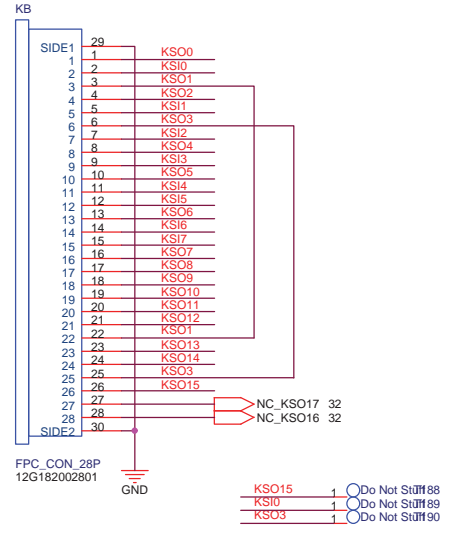
### For Touch-Pad



SW2, SW3 use 12G09103305N

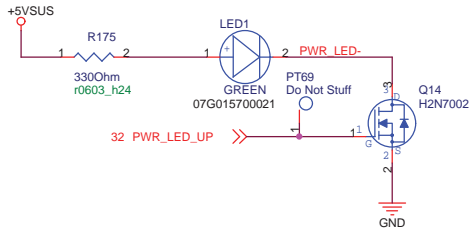


### For Keyboard Connector

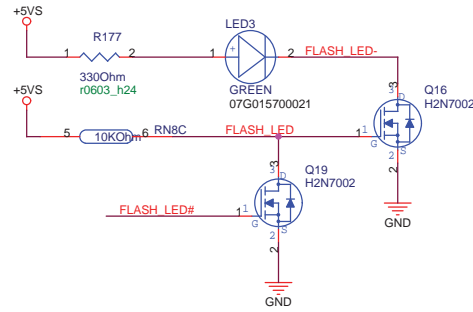


KSI0	EC19	2	Do Not Stuff /X
KSI1	EC11	2	Do Not Stuff /X
KSI2	EC13	2	Do Not Stuff /X
KSI3	EC14	2	Do Not Stuff /X
KSI4	EC14	2	Do Not Stuff /X
KSI5	EC15	2	Do Not Stuff /X
KSI6	EC16	2	Do Not Stuff /X
KSI7	EC17	2	Do Not Stuff /X
KSO0	EC19	2	Do Not Stuff /X
KSO1	EC19	2	Do Not Stuff /X
KSO2	EC20	2	Do Not Stuff /X
KSO3	EC21	2	Do Not Stuff /X
KSO4	EC22	2	Do Not Stuff /X
KSO5	EC23	2	Do Not Stuff /X
KSO6	EC24	2	Do Not Stuff /X
KSO7	EC25	2	Do Not Stuff /X
KSO8	EC26	2	Do Not Stuff /X
KSO9	EC27	2	Do Not Stuff /X
KSO10	EC28	2	Do Not Stuff /X
KSO11	EC29	2	Do Not Stuff /X
KSO12	EC30	2	Do Not Stuff /X
KSO13	EC31	2	Do Not Stuff /X
KSO14	EC32	2	Do Not Stuff /X
KSO15	EC33	2	Do Not Stuff /X

for POWER LED

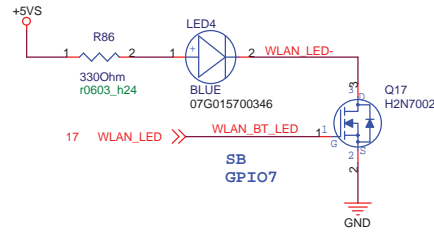


for FLASH LED

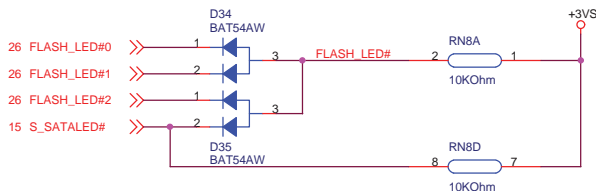
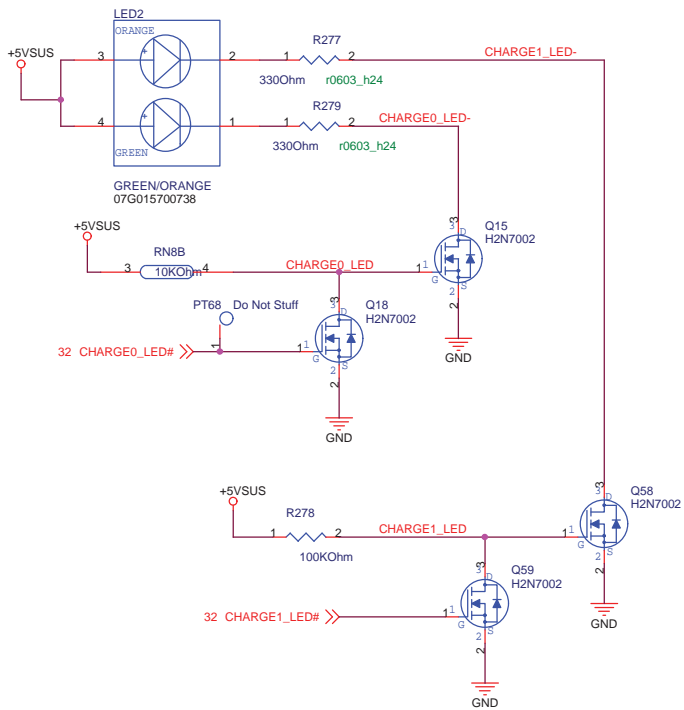


for WLAN/BlueTooth LED

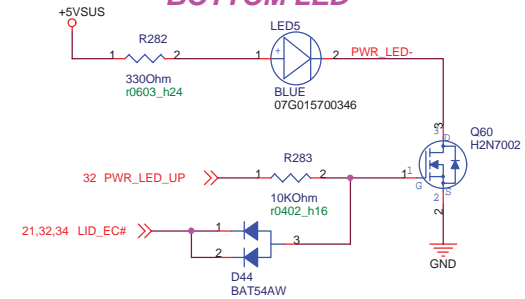
R86 use 4.7K OHm 10G213472003030

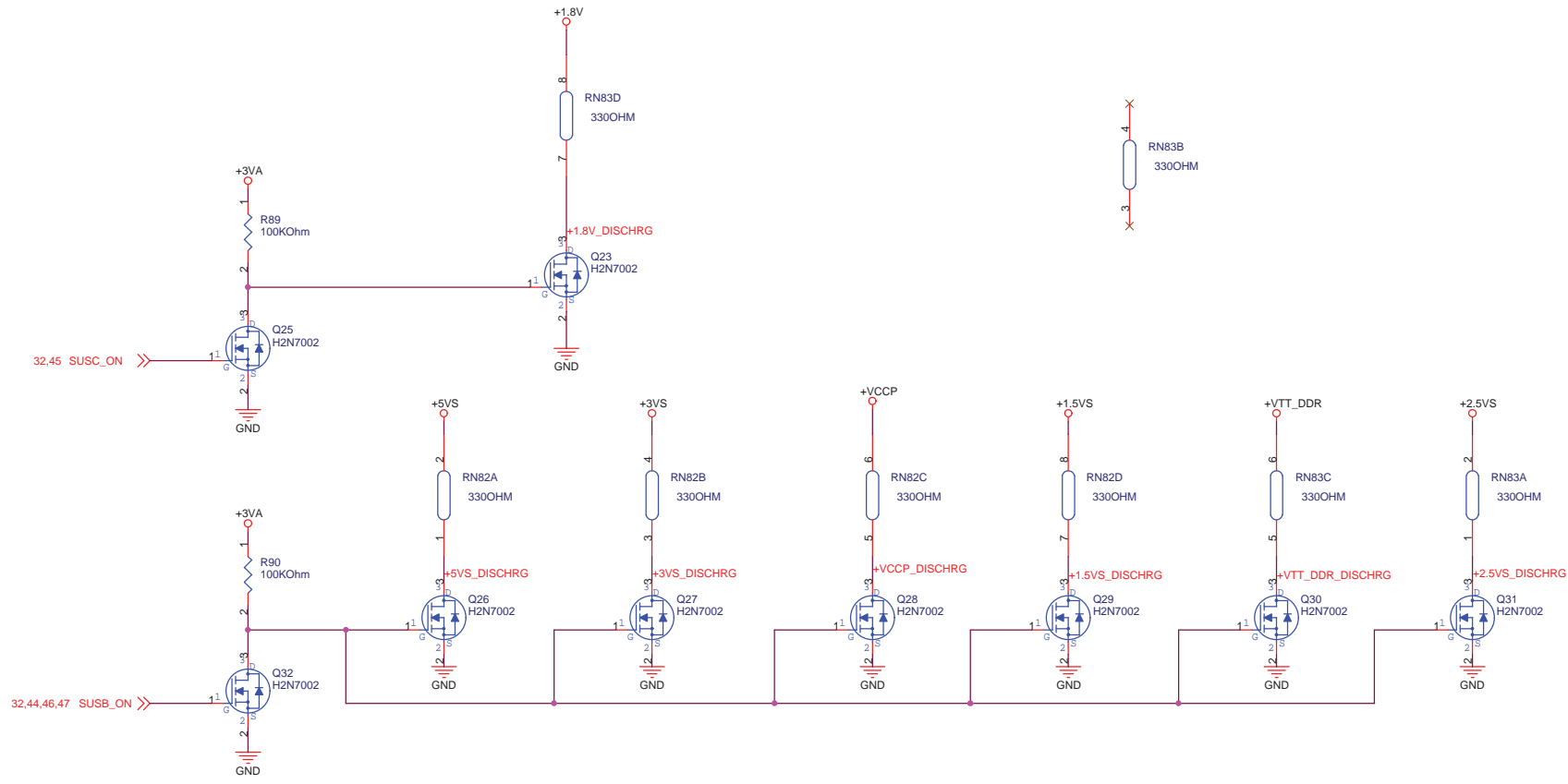


for CHARGE LED



for POWER BOTTOM LED

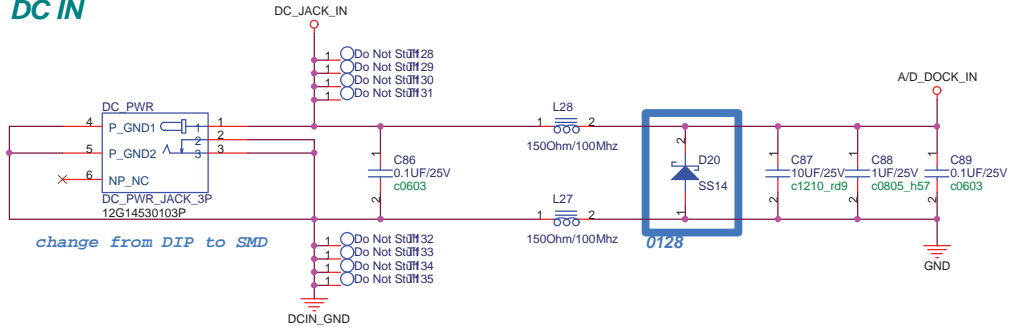




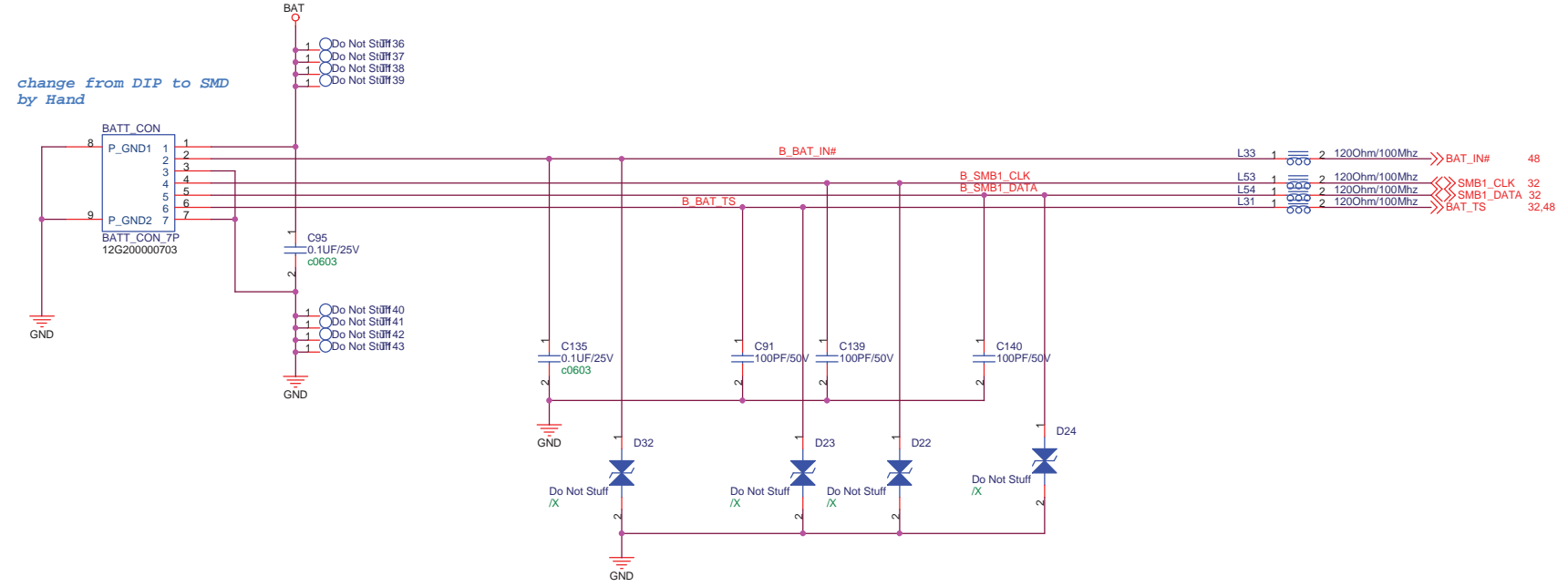
<http://hobi-elektronika.net>

<b>ASUS</b>		<b>Title : Discharge</b>	
ASUSTek Computer INC.		Engineer: <i>Kell_Huang</i>	
Size	Project Name	Rev	
A3	<b>P901</b>	1.00G	
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**DC IN**

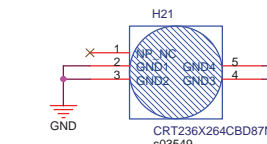
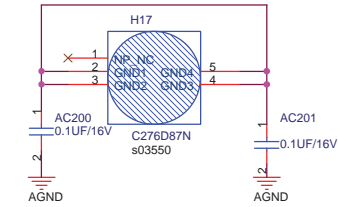
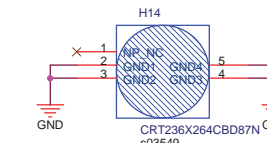
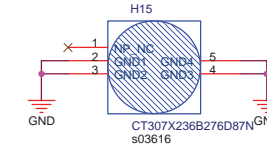
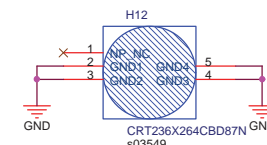
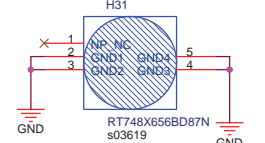
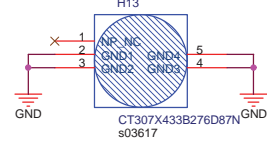
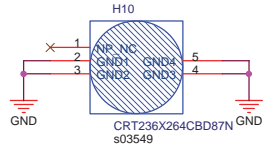
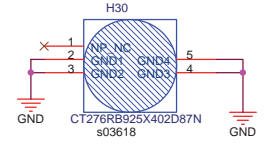
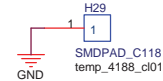
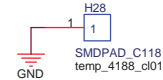
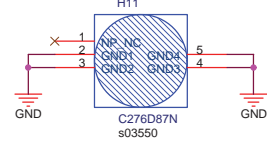
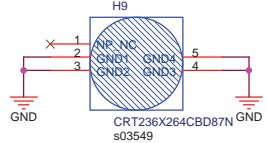
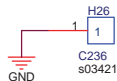
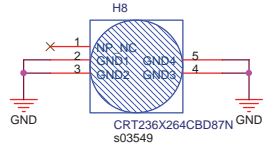
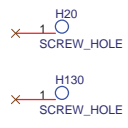
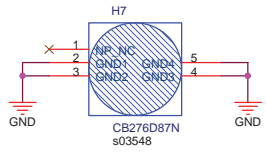


**BAT IN**

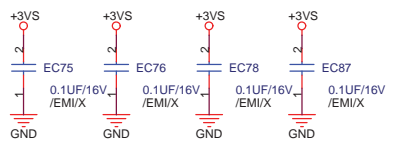
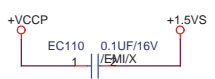
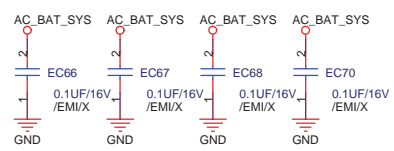
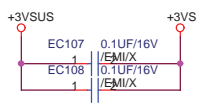
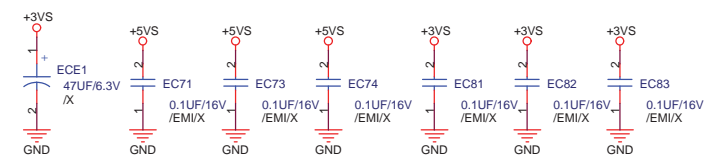
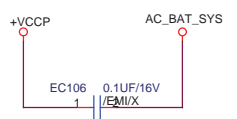
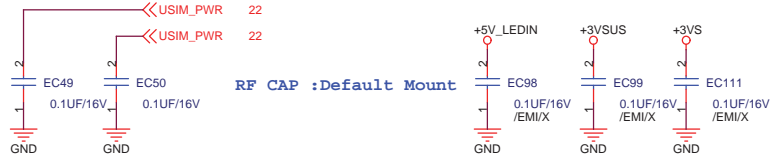
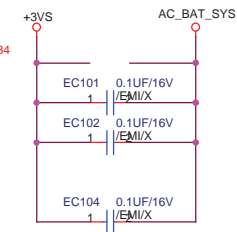
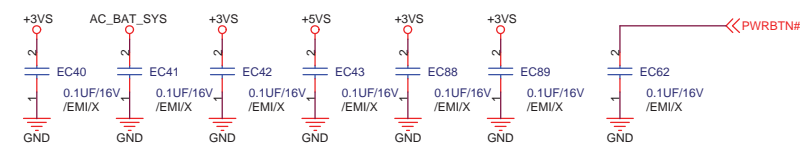
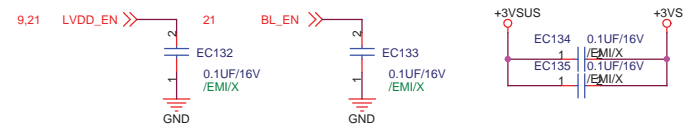
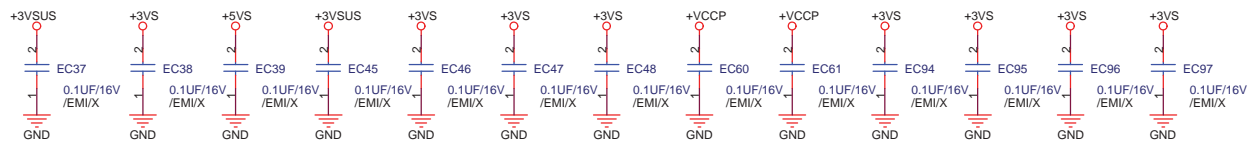
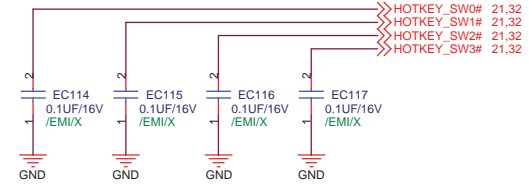
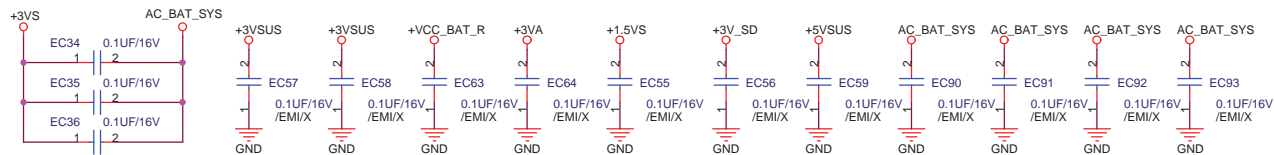


<http://hobi-elektronika.net>

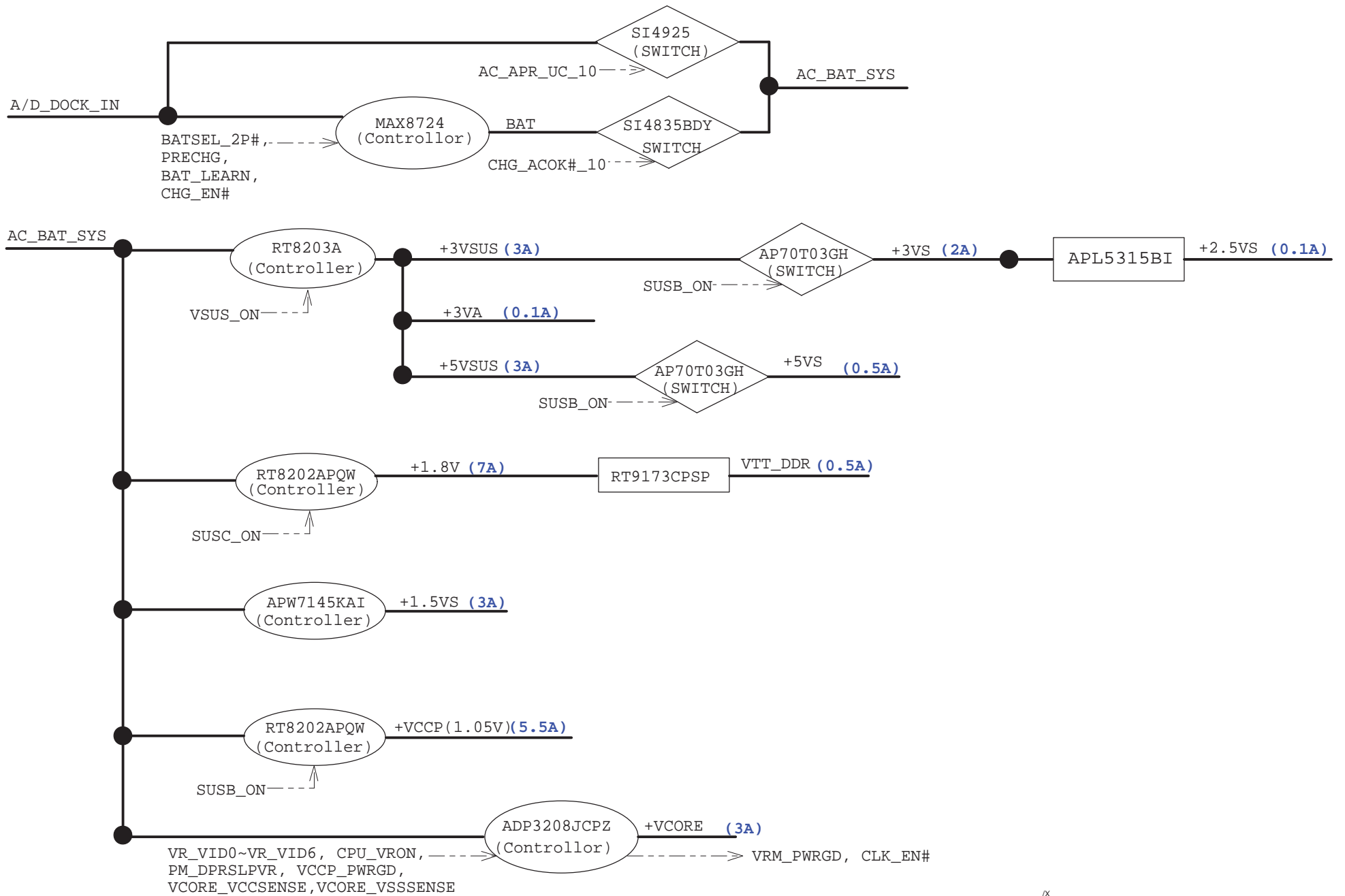
<b>ASUS</b>		<b>Title : PWR Jack</b>	
ASUSTek Computer INC.		Engineer: <i>Kell_Huang</i>	
Size	Project Name	Rev	
A3	<b>P901</b>	1.00G	
Date: Monday, March 31, 2008		Sheet	39 of 47







		Title : EMI	
ASUSTek Computer INC.		Engineer: Keli_Huang	
Size	Project Name		Rev
A3	P901		1.00G
Date: Monday, March 31, 2008	Sheet	41 of 47	

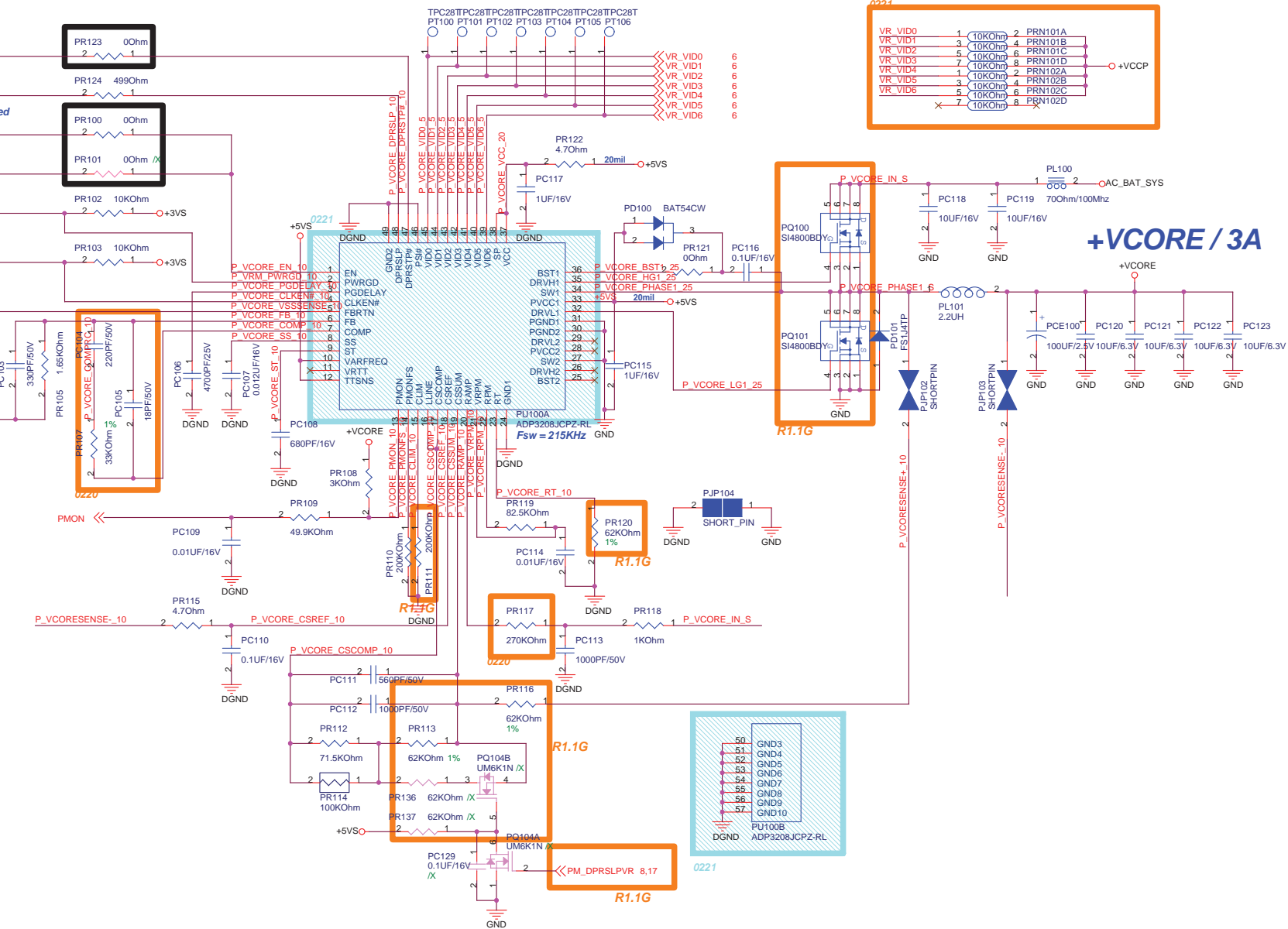
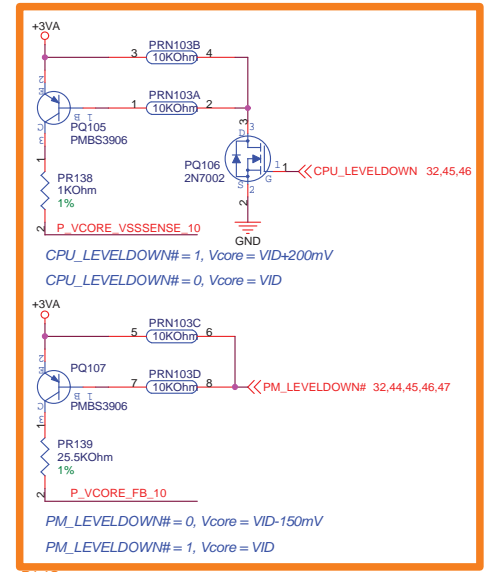
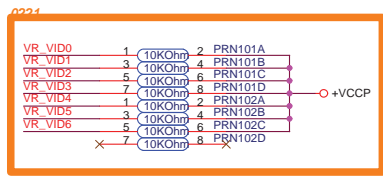


<http://hobi-elektronika.net>

<b>ASUS</b>		<b>Title : Power Flow</b>	
ASUSTek Computer INC.		Engineer: <i>Joy_Zhou</i>	
Size	Project Name	Rev	
A3	<b>P901</b>	1.00G	
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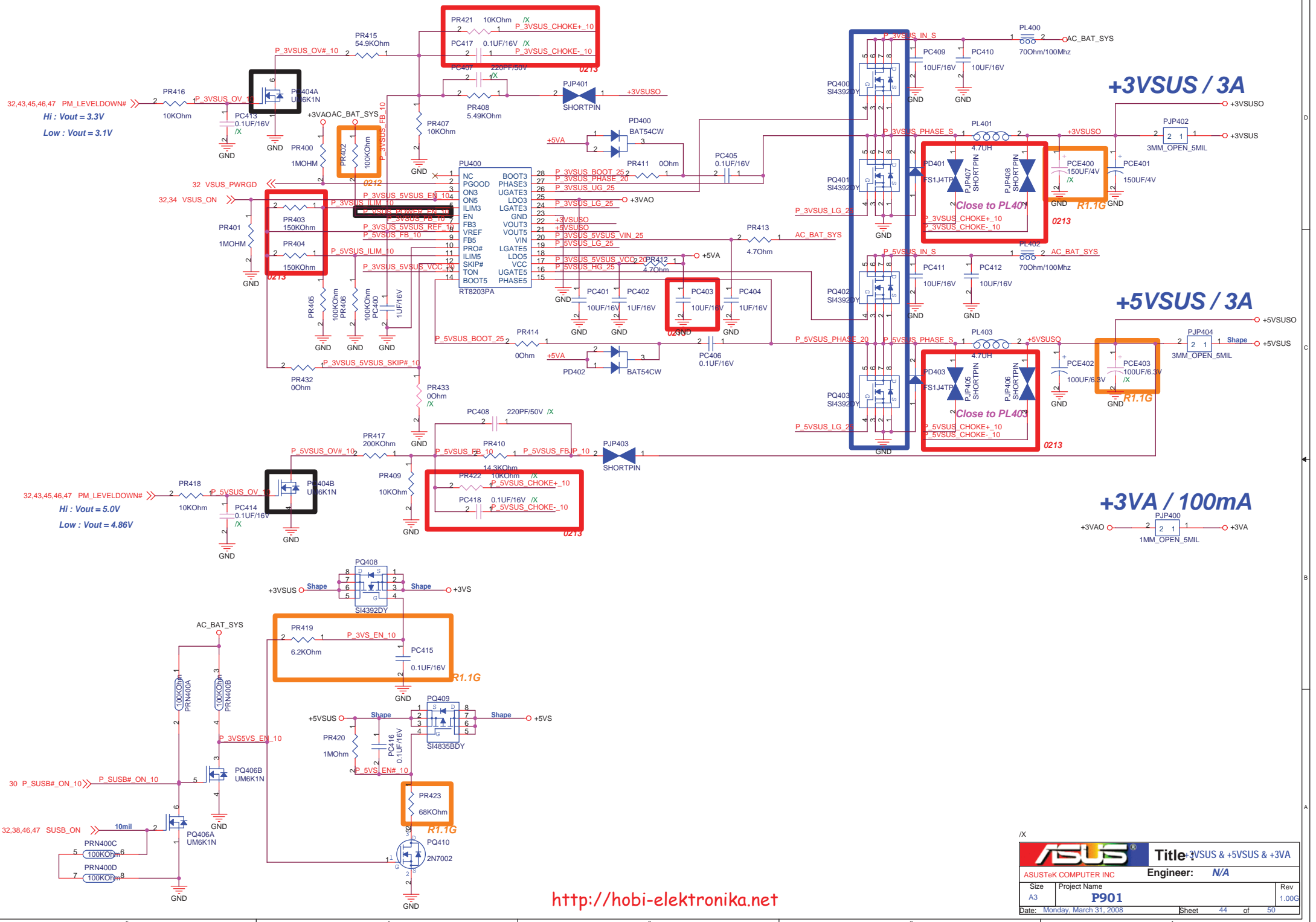
5.15 PM\_DPRSTP# >> STP\_CPU# = 0, CPU is in Deep Sleep Mode  
 8.17 PM\_DPRSLPVR >> PM\_DPRSLPVR = 1, CPU Deeper Sleep Mode is enabled  
 32 CPU\_VRON >> CPU\_VRON = 1, Vcore Reglator Enabled  
 4.46 VCCP\_PWRGD >> VCCP\_PWRGD = 1, Vcore Reglator Enabled  
 8.17.32.33 VRM\_PWRGD << VRM\_PWRGD = 1, Vcore Power OK

CLK\_EN# << CLK\_EN# = 0, Clock is enabled



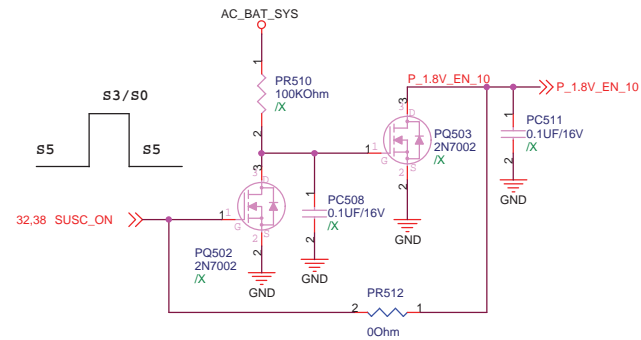
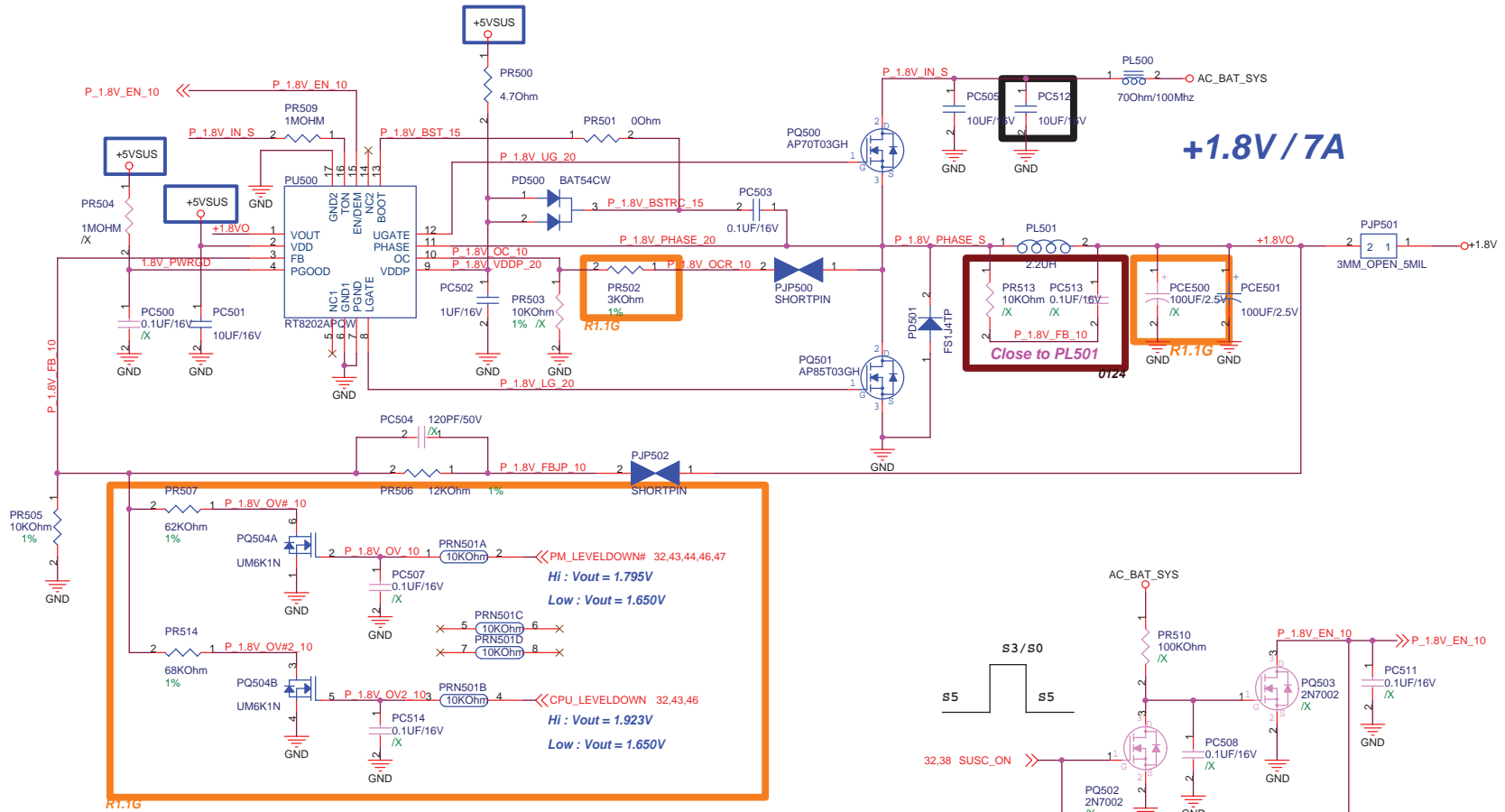
PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Vcore	Status
L	L	H	VID-150mV	Power Saving
H	L	H	VID	Normal
H	H	L	VID + 200mV	Performance
L	H	L	VID + 50mV	N/A

ASUS Title : Vcore  
 ASUSTek Computer INC. Engineer: Joy\_Zhou  
 Size Project Name  
 Custom P901 Rev 1.2G  
 Date: Monday, March 31, 2008 Sheet 43 of 50

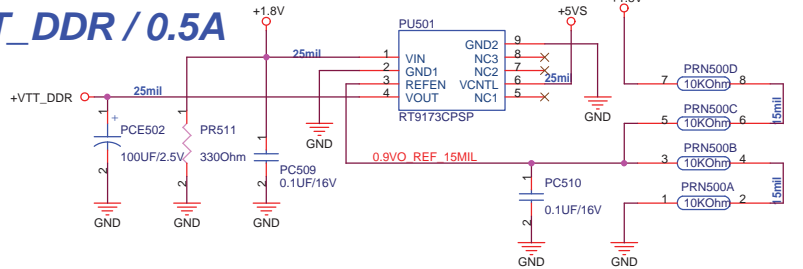


<http://hobi-elektronika.net>

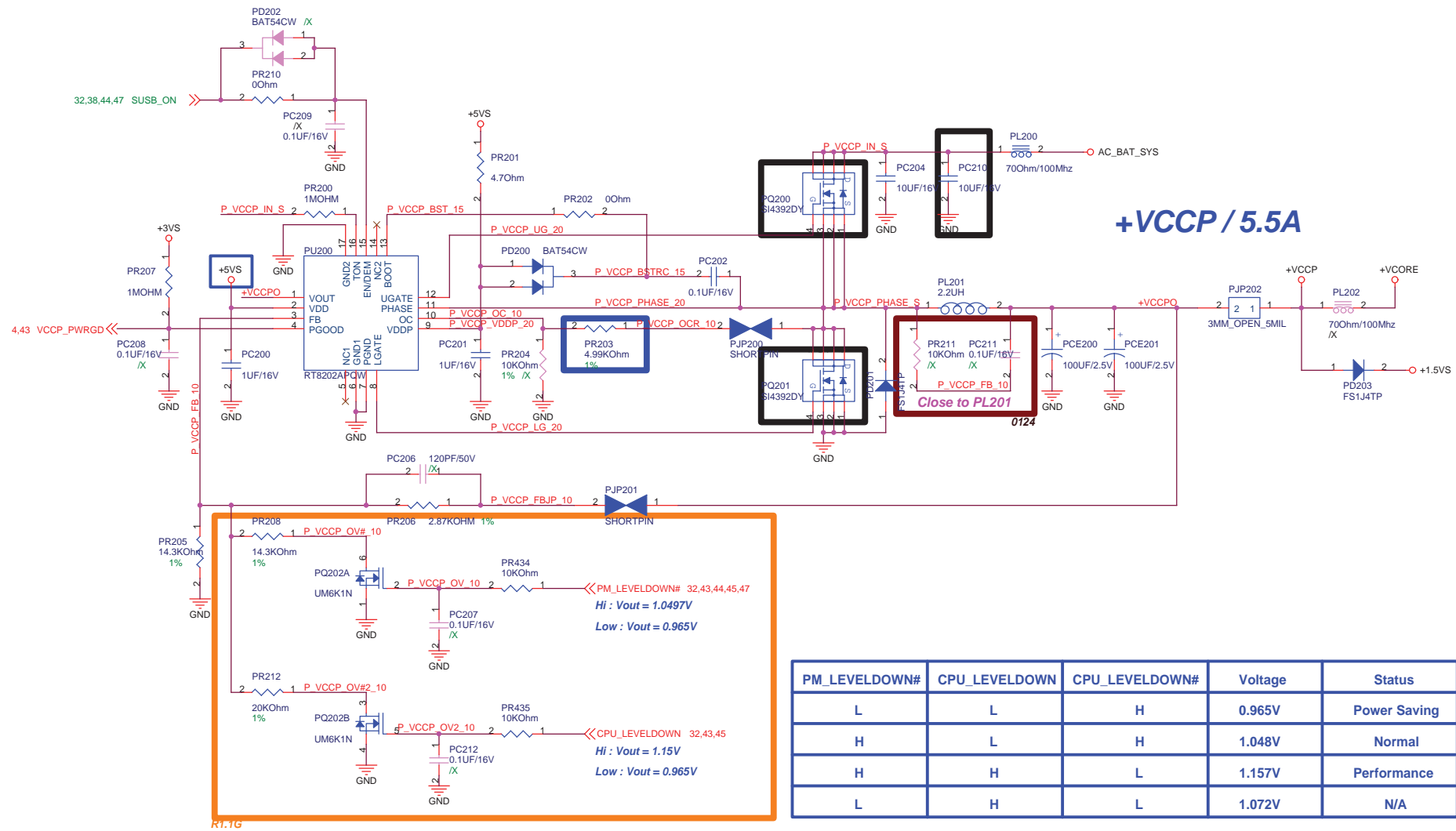
<b>ASUS</b>		<b>Title:</b> 3VSUS & +5VSUS & +3VA	
ASUSTeK COMPUTER INC		<b>Engineer:</b> N/A	
Size A3	Project Name <b>P901</b>	Rev 1.00G	
Date: Monday, March 31, 2008	Sheet 44	of 50	



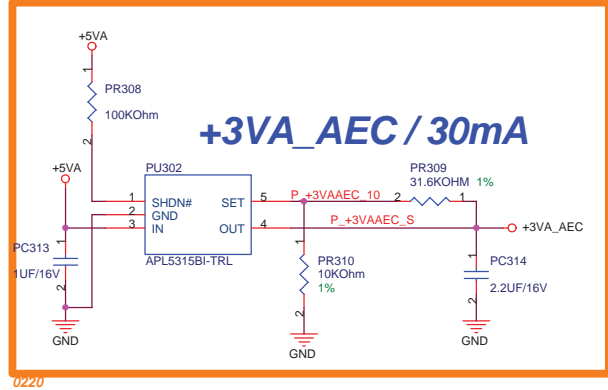
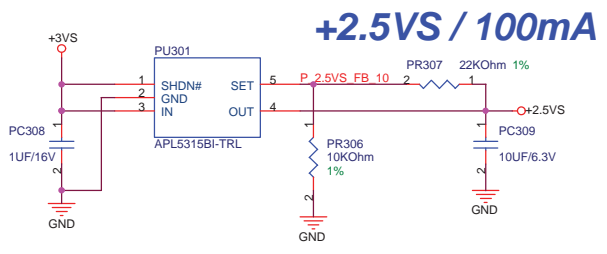
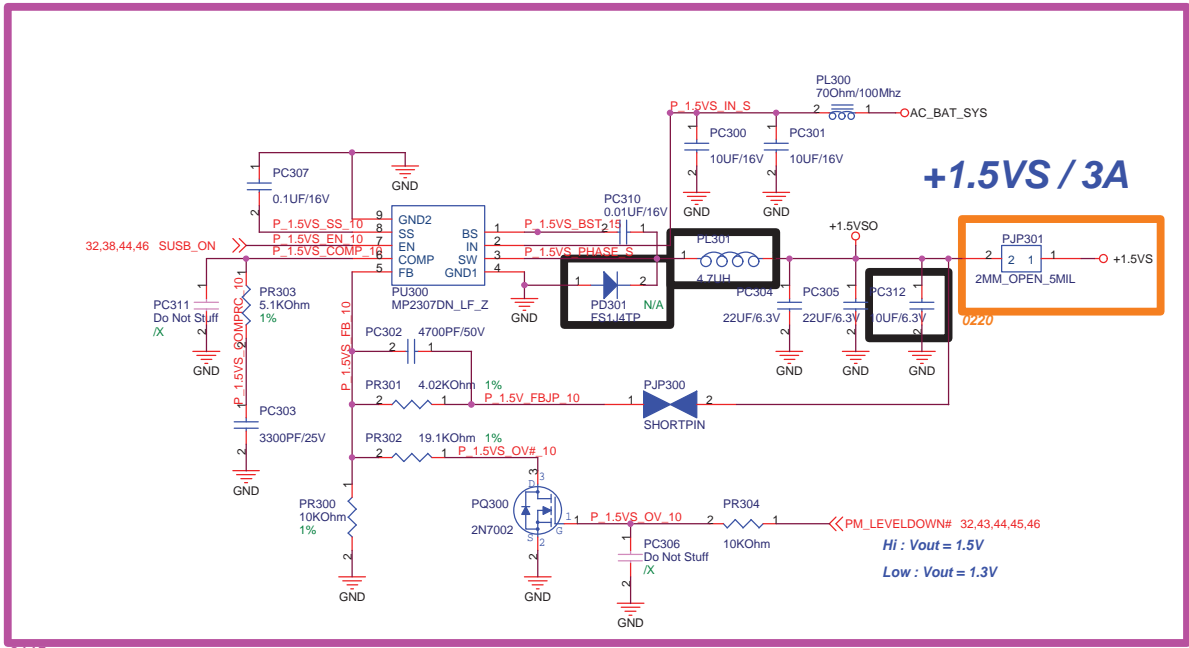
### VTT\_DDR / 0.5A



PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	1.650V	Power Saving
H	L	H	1.795V	Normal
H	H	L	1.927V	Performance
L	H	L	1.782V	N/A

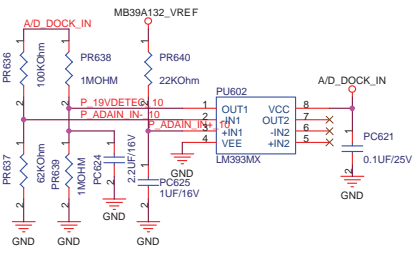


PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	0.965V	Power Saving
H	L	H	1.048V	Normal
H	H	L	1.157V	Performance
L	H	L	1.072V	N/A



<http://hobi-elektronika.net>

<b>ASUS</b>		<b>Title : +1.5VS &amp; +2.5VS</b>	
ASUSTek Computer INC.		Engineer: <i>Joy_Zhou</i>	
Size A3	Project Name <b>P901</b>	Date: Monday, March 31, 2008	Rev 1.2G
		Sheet 47 of 50	



**VREF = 5.0V**  
 $f_{osc}(KHz) = 17000 / RT (KOhm)$   
 Soft start:  $t_s(s) = 0.13 * CS (\mu F)$   
 $VTH \text{ of } -IN1: 5V / 62 * (100+62) = 13.06V$   
 $VTH \text{ of } ACIN: 1.25V / 25 * (185+25) = 10.5V$   
 Change PR607 and PR608 value

**Prevent Input from 19V :**  
 Adaptor > 13.06V, PQ603B Turn-off  
 Adaptor < 13.06V, PQ603B Turn-on

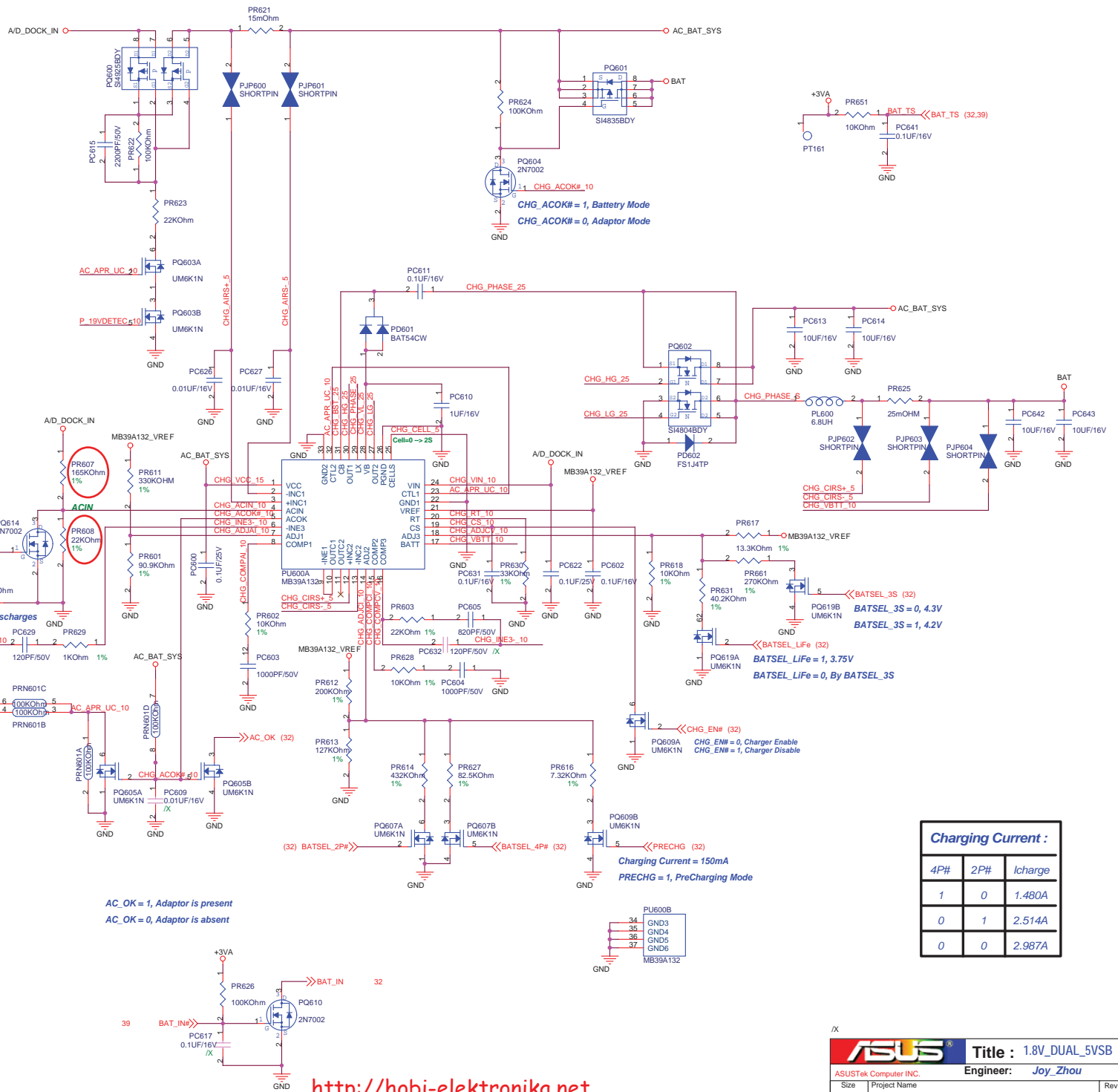
**Battery Cell Selection :**  
 $BAT\_ID = 1, 2 \text{ Cells; } V_{adj2} = 0.998V$   
 $\Rightarrow I_{charge} = 1.477A$   
 $BAT\_ID = 0, 4/6 \text{ Cells; } V_{adj2} = 1.648V$   
 $\Rightarrow I_{charge} = 2.517A$

**Pre-Charging Mode :**  
 Precharging current = 150mA  
 $V_{adj2} = 168.75mV$

**Adaptor Max. Current :**  
 $PR600=235.8K; I_{limit} = 2.170A; 20.615W (9.5V/22W)$   
 $PR600=185.3K; I_{limit} = 2.677A; 32.124W (12V/36W)$

**ACIN Threshold = 1.25V**  
 Adaptor > 10.5V, System Powered by Adaptor  
 Adaptor < 10.5V, System Powered by Battery

**Battery Charging Voltage :**  
 $V_{adj3} > 4.1V \Rightarrow V_{bat} = 4.2V / \text{cell}$   
 $2.2V > V_{adj3} > 1.1V \Rightarrow V_{bat} = 2 * V_{adj3}$   
**Battery Charging Current :**  
 $4.4V > V_{adj2} > 0V \Rightarrow$   
 $I_{chg} = V_{adj2} * 0.075 / (25 * R_s)$   
**Input Adaptor Max. Current Limit :**  
 $I_{limit\_current} = (V_{adj1} - 0.075) / (25 * R_s)$

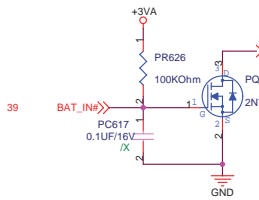


$AC\_OK = 1, \text{ Adaptor is present}$   
 $AC\_OK = 0, \text{ Adaptor is absent}$

Charging Current = 150mA  
 $PRECHG = 1, \text{ PreCharging Mode}$

**Charging Current :**

4P#	2P#	Icharge
1	0	1.480A
0	1	2.514A
0	0	2.987A



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## EC KB3310 GPIO SETTING

Pin	Pin Name	Signal Name	Type	Note
1	GPIO00/GA20	A20GATE	O	
2	GPIO01/KBRST#	RC_IN#	O	
6	GPIO04	EMAIL_SW#	I	Internal pull high
13	GPIO05/PCIRST#	PCI_RST#	I	
14	GPIO07	BAT_OTP	I	Battery over temperature
15	GPIO08	EXTSMIH#	OD	10K pull high to +3VSB
16	GPIO0A	LID_EC#	I	Internal pull high
17	GPIO0B/ESB_CLK	NC	O	
18	GPIO0C/ESB_DAT	NC	O	
19	GPIO0D	DISTP_SW#	I	Internal pull high
20	GPIO0E/SC#	EXT_SC#	O	10K pull high to +3VSB
21	GPIO0F/PWM0	BL_PWM_DA	O	
23	GPIO10/PWM1	BAT_CRITICAL	I	Battery critical capacity
25	GPIO11/PWM2	PM_PWRBTN#	OD	Internal pull high in ICH
26	GPIO12/FANPWM1	FAN0_PWM	O	CPU Fan
27	GPIO13/FANPWM2	FAN1_PWM	O	VGA Fan
28	GPIO14/FANFB1	FAN0_TACH	I	CPU FanTach
29	GPIO15/FANFB2	FAN1_TACH	I	VGA FanTach
30	GPIO16/E51_TX	E51_TX	O	RS232 debug port
31	GPIO17/E51_RX	E51_RX	I	RS232 debug port
32	GPIO18	PWR_SW#	I	Internal pull high
34	GPIO19/PWM3	MAIL_LED#	O	
36	GPIO1A/NUMLED	NUM_LED#	O	
38	GPIO1D/CLKRUN#	NC	O	
39	GPIO20/KSO0/TP_TEST	KSO0	O	
40	GPIO21/KSO1/TP_PLL	KSO1	O	
41	GPIO22/KSO2	KSO2	O	
42	GPIO23/KSO3	KSO3	O	
43	GPIO24/KSO4	KSO4	O	
44	GPIO25/KSO5	KSO5	O	
45	GPIO26/KSO6	KSO6	O	
46	GPIO27/KSO7	KSO7	O	
47	GPIO28/KSO8	KSO8	O	
48	GPIO29/KSO9	KSO9	O	
49	GPIO2A/KSO10	KSO10	O	
50	GPIO2B/KSO11	KSO11	O	
51	GPIO2C/KSO12	KSO12	O	
52	GPIO2D/KSO13	KSO13	O	
53	GPIO2E/KSO14	KSO14	O	
54	GPIO2F/KSO15	KSO15	O	
55	GPIO30/KSI0	KSI0	I	Internal pull high
56	GPIO31/KSI1	KSI1	I	Internal pull high
57	GPIO32/KSI2	KSI2	I	Internal pull high
58	GPIO33/KSI3	KSI3	I	Internal pull high
59	GPIO34/KSI4	KSI4	I	Internal pull high
60	GPIO35/KSI5	KSI5	I	Internal pull high
61	GPIO36/KSI6	KSI6	I	Internal pull high
62	GPIO37/KSI7	KSI7	I	Internal pull high
63	GPI38/AD0	BAT_ICHG	I	
64	GPI39/AD1	BAT_CONFIG	I	Battery configuration
65	GPIO3A/AD2	BAT_SENSE	I	Battery Voltage Sensor
66	GPIO3B/AD3	BAT_TS	I	Battery Thermal Sensor
68	GPO3C/DA0	DOC	O	Trigger Clock Gen

Pin	Pin Name	Signal Name	Type	Note
70	GPO3D/DA1	LCD_BACKOFF#	O	
71	GPO3E/DA2	CLK_PWRSERVE#	O	
72	GPO3F/DA3	BAT_LL#	O	Battery Low Low
73	GPIO40	AC_OK	I	AC Adaptor Plug in
74	GPIO41	PM_RSMRST#	O	10K pull down to GND
75	GPI42	BAT_IN	I	
76	GPI43	CLRTC_EC	I	
77	GPIO44/SCL1	SMB0_CLK	I/O	4.7K pull high to +3VA_EC
78	GPIO45/SDA1	SMB0_DAT	I/O	4.7K pull high to +3VA_EC
79	GPIO46/SCL2	SMB1_CLK	I/O	10K pull high to +3V
80	GPIO47/SDA2	SMB1_DAT	I/O	10K pull high to +3V
81	GPIO48/KSO16	KB pin 28	I	for KB type detection
82	GPIO49/KSO17	KB pin 27	I	for KB type detection
83	GPIO4A/PSCLK1	AUO_SCL	O	for AUO, default H at S0
84	GPIO4B/PSDAT1	AUO_SDA	O	for AUO, default L at S0
85	GPIO4C/PSCLK2	AUO_CSB	O	for AUO, default H at S0
86	GPIO4D/PSDAT2	LVDD_EN	I	for AUO 7" Panel
87	GPIO4E/PSCLK3	TP_CLK	I/O	10K pull high to +3V
88	GPIO4F/PSDAT3	TP_DAT	I/O	10K pull high to +3V
89	GPIO50/SELIO#	BATSEL_3S	O	Battery series, H:3S, L:4S
90	GPIO52/E51_CS#	CHG_LED_UP#	O	
91	GPIO53/CAPLED	CAP_LED#	O	
92	GPIO54	PWR_LED_UP	O	
93	GPIO55/SCRLED	SCRLED#	O	
95	GPIO56	PWR4G_SW#	I	Internal pull high
97	GPXOA00/SDICS#	SPI_MODE#	O	4.7K pull down to GND
98	GPXOA01/SDICLK	SUSC_ON	O	
99	GPXOA02/SDIDO	VSUS_ON	O	
100	GPXOA03	CPU_VRON	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	ICH_PWROK	O	
103	GPXOA06	VOLT_CTRL	O	
104	GPXOA07	CHG_EN#	O	Battery charging enabled
105	GPXOA08	PRECHG	O	
106	GPXOA09	SPI_WP#	O	
107	GPXOA10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	
109	GPXID0/SDIDI	BATSEL_2P#	O	Battery parallel, H:1P, L:2P-3P
110	GPXID1	NC	O	
112	GPXID2	THRO_CPU	O	Active if CPU temperature over spec
114	GPXID3	SUSB#	I	100K pull down to GND
115	GPXID4	SUSC#	I	100K pull down to GND
116	GPXID5	CPUPWR_GD	I	Pull high to +3V
117	GPXID6	VSUS_GD	I	
118	GPXID7	NC	O	
121	GPIO57	INTERNET#	I	Internal pull high
126	GPIO57/SPICLK	SPI_CLK	O	
127	GPIO59/TEST_CLK	NC	O	

## EC KB3310 Other Pin SETTING


Pin	Pin Name	Signal Name	Type	Note
3	SERIRQ	INT_SERIRQ	I/O	10K pull high to +3V
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA_EC	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCL_EC	I	
22	VCC	+3VA_EC	P	
24	GND	GND	P	
33	VCC	+3VA_EC	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	100K pull high to +3VA_EC
67	AVCC	+3VACC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA_EC	P	
111	VCC	+3VA_EC	P	
113	GND	GND	P	
119	RD#/SPIDI	SPL_SO	I	
120	WR#/SPIDO	SPL_SI	O	
112	XCLKI	32KXCLKI	I	
123	XCLKO	32KXCLKO	O	
124	V18R	V18R	P	Reserved 1uF to GND
125	VCC	+3VA_EC	P	
128	SPICS#/SELMEM#	SPI_CE#	O	

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		<b>Title : EC Pin Define</b>	
ASUSTek Computer INC.		Engineer: <b>Satan He</b>	
Size A3	Project Name <b>P901</b>	Rev 1.00G	
Date: Monday, March 31, 2008	Sheet 49 of 50		

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		Title : History	
ASUSTek Computer INC.		Engineer: <i>Satan He</i>	
Size	Project Name		Rev
A3	<b>P901</b>		1,00G
Date: Monday, March 31, 2008		Sheet	50 of 50