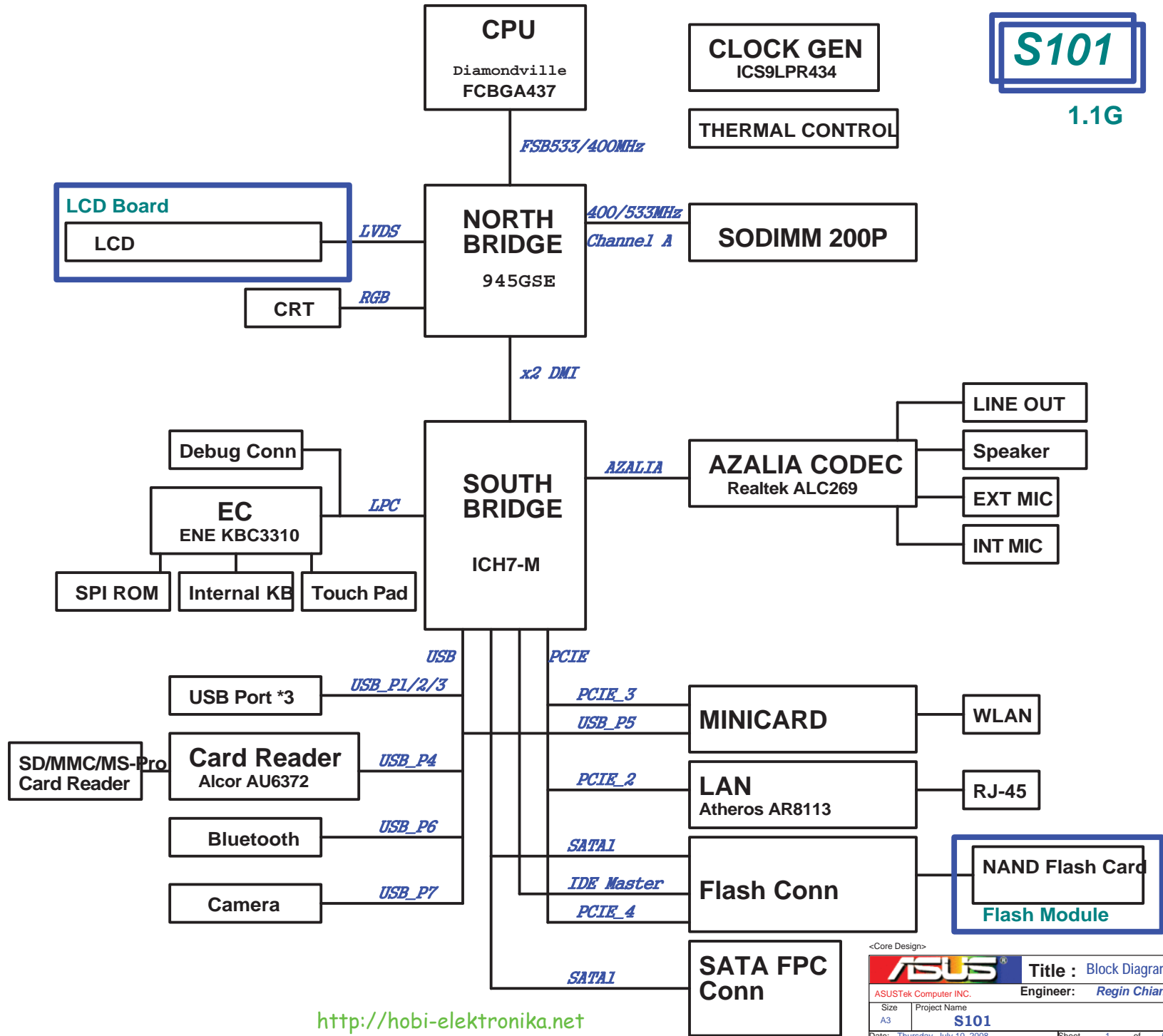


- 01_Block Diagram
- 02_System Setting
- 03_Power Sequence
- 04_Clock Gen_ICS9LPR434
- 05_Diamondville_BUS
- 06_Diamondville_PWR
- 07_NB-945GMS(HOST)
- 08_NB-945GMS(DMI)
- 09_NB-945GMS(GRAPHIC)
- 10_NB-945GMS(DDR2)
- 11_NB-945GMS(PWR)
- 12_NB-945GMS(PWR2)
- 13_NB-945GMS(GND)
- 14_SB-ICH7M(PWR)
- 15_SB-ICH7M(1)
- 16_SB-ICH7M(2)
- 17_SB-ICH7M(3)
- 18_DDR2 SODIMM
- 19_DDR2 Termination
- 20_Onboard VGA
- 21_LCD Conn_LID
- 22_Blank
- 23_Mini WIFI+ BT
- 24_LAN_Atheros AR8113
- 25_RJ45
- 26_Flash Conn
- 27_USB Port
- 28_Camera Conn
- 29_Card Reader_AU6372A51
- 30_Codec_ALC269
- 31_Audio_AMP_Jack
- 32_EC_ENE KB3310
- 33_EC
- 34_Switch_SPI ROM_Debug Conn
- 35_Thermal Sensor_FAN
- 36_KB_Touch Pad
- 37_LED_THERMTRIP
- 38_Discharge
- 39_PWR Jack
- 40_Srew Hole
- 41_EMI
- 42_POWER FLOW
- 43_Vcore
- 44_Power System
- 45_Power_+1.8V & VTTDDR
- 46_Power_VCCP
- 47_Power_+1.5V & +2.5V
- 48_Power_Charger
- 49_EC Pin Define
- 49_History



S101

1.1G

<http://hobi-elektronika.net>

<Core Design>	
ASUS	Title : Block Diagram
ASUSTek Computer INC.	Engineer: Regin Chiang
Size A3	Project Name S101
Date: Thursday, July 10, 2008	Sheet 1 of 50

EEE PC 701 PCB version

GPI37	GPI38	GPI39	PCB version
0	0	0	
0	0	0	
0	0	1	
0	0	1	
0	1	0	
0	1	0	
0	1	1	
0	1	1	
1	0	0	
1	0	0	
1	0	1	
1	0	1	
1	1	0	
1	1	0	
1	1	1	
1	1	1	

USB

USB 0	NC
USB 1	USB Conn
USB 2	USB Conn
USB 3	USB Conn
USB 4	Card Reader
USB 5	Minicard
USB 6	Bluetooth
USB 7	Camera


PCIE

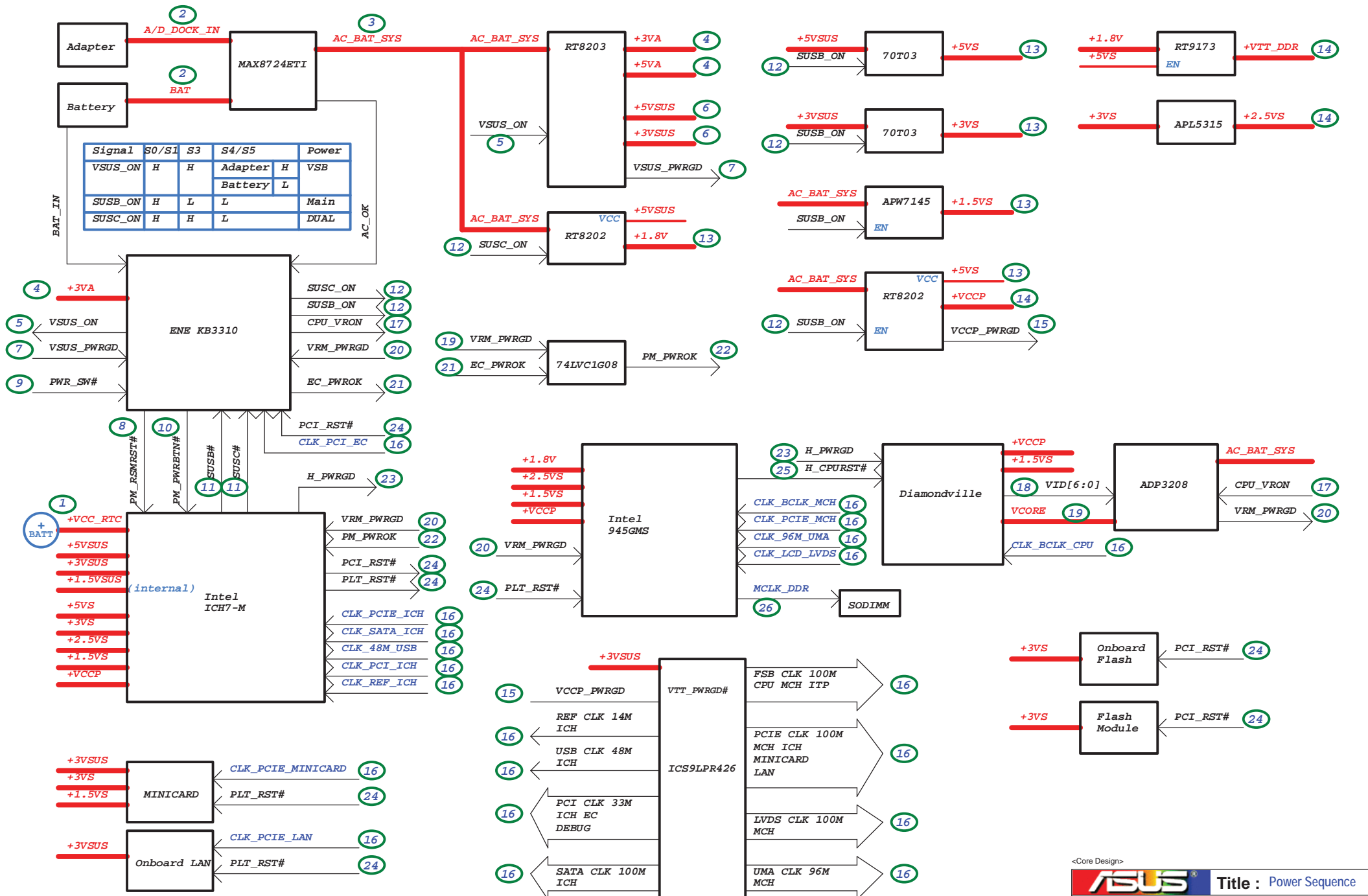
PCIE 1	NC
PCIE 2	LAN
PCIE 3	Minicard
PCIE 4	SSD

Azalia

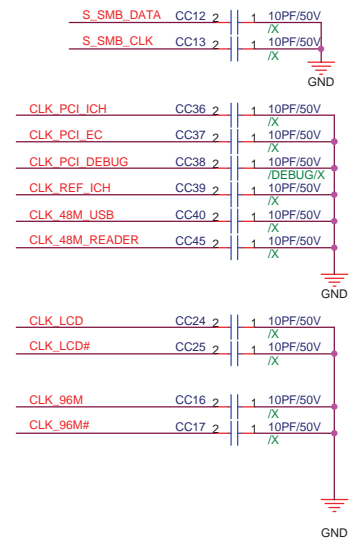
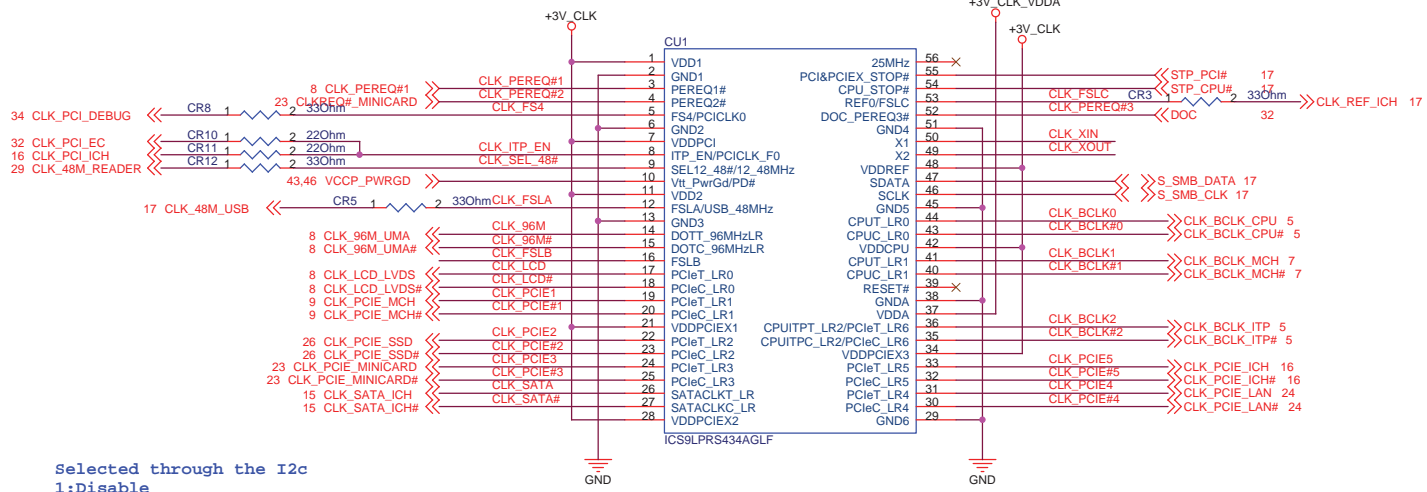
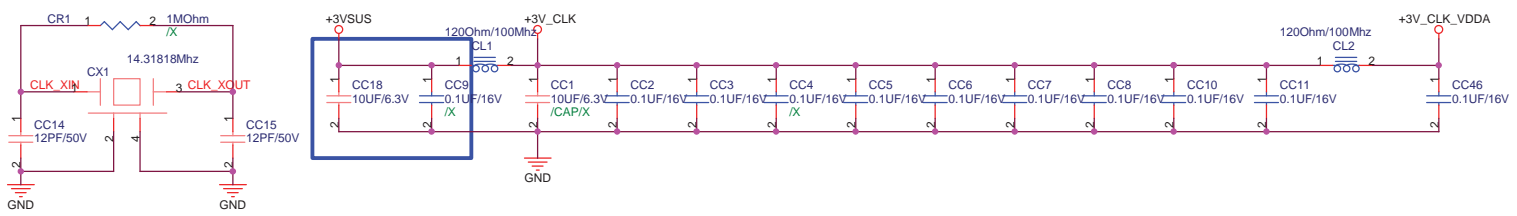
ACZ_SDIN0	CODEC
ACZ_SDIN1	NC
ACZ_SDIN2	NC

<Core Design>

		Title : System Setting	
ASUSTek Computer INC.		Engineer: Satan_He	
Size	Project Name	Rev	
A3	S101	1.1G	
Date: Thursday, July 10, 2008		Sheet	2 of 50



<http://hobi-elektronika.net>

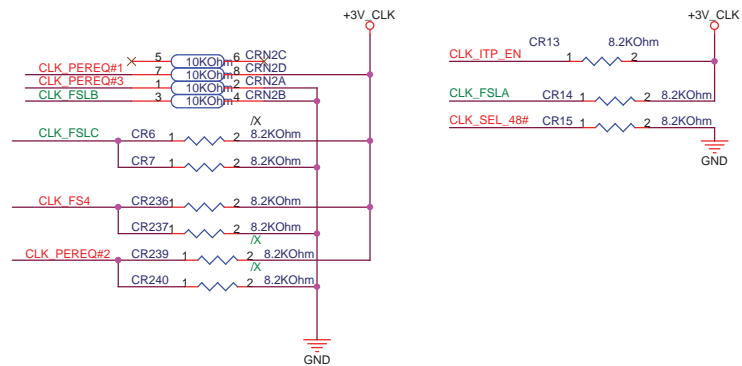
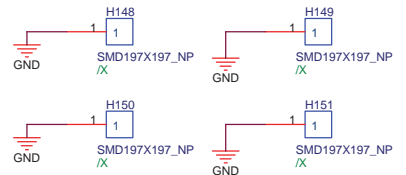


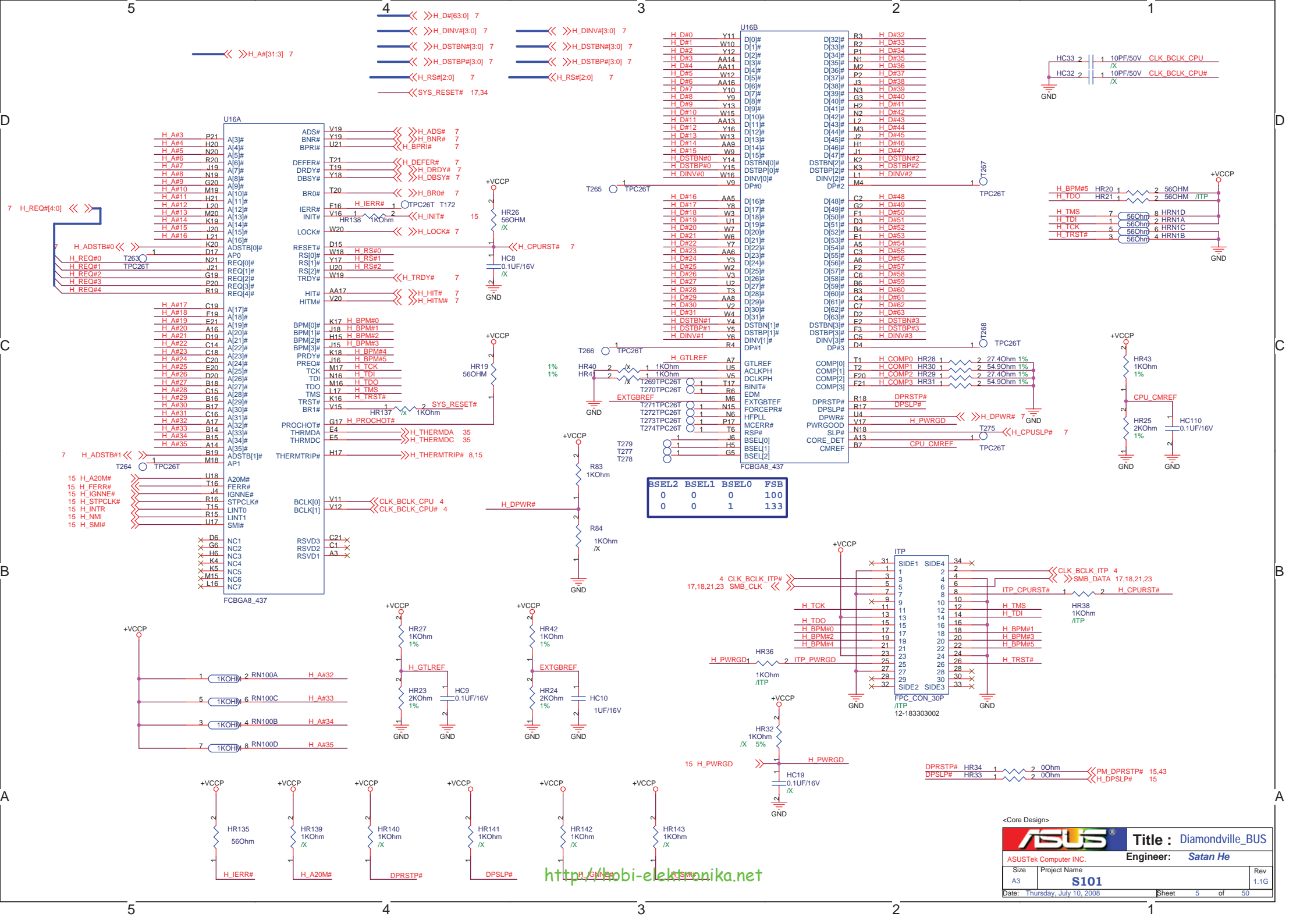
Selected through the I2c
1:Disable
0:Enable

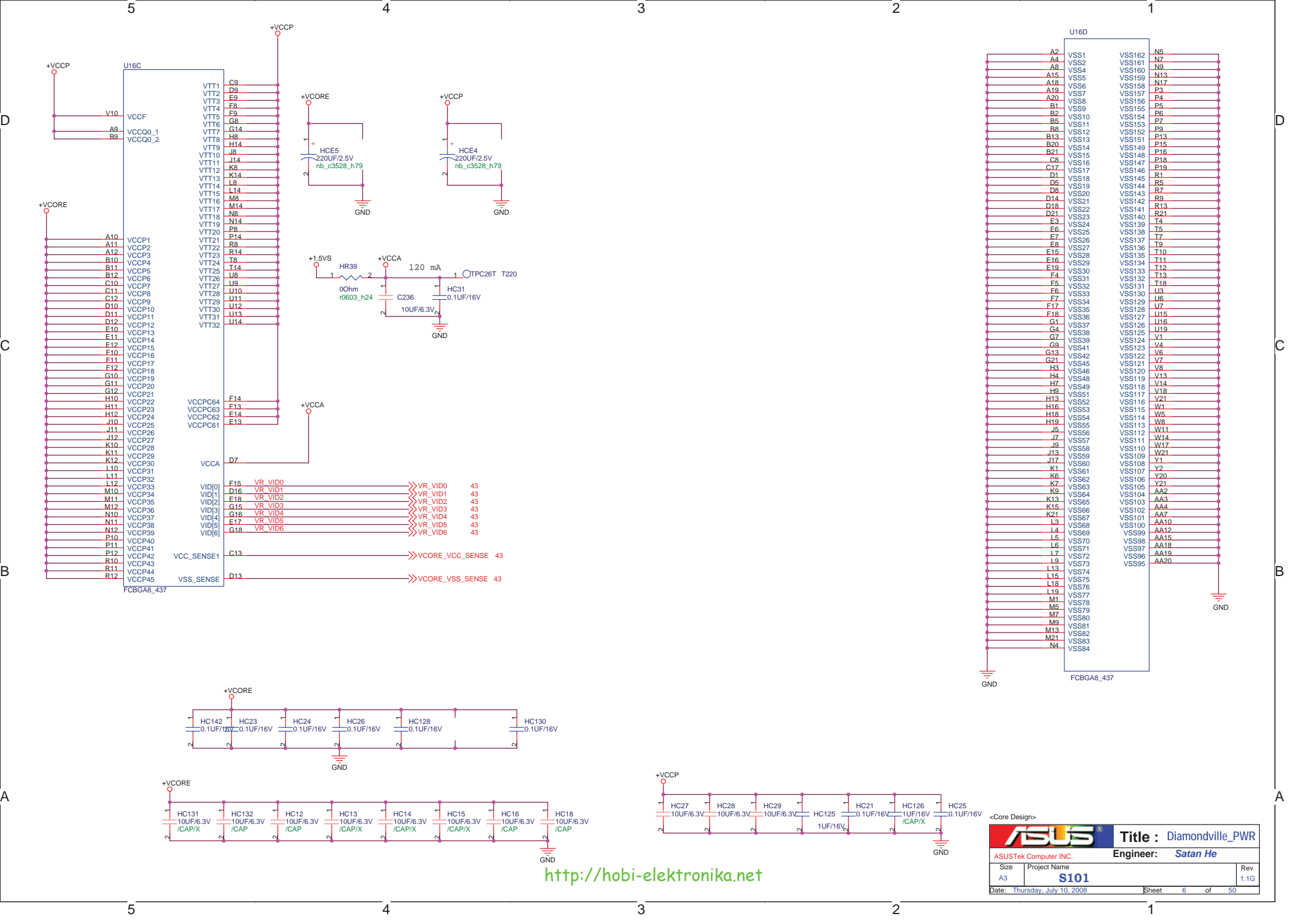
PEREQ1:PCIEx0 & PCIEx1
PEREQ2:PCIEx2 & PCIEx3 & SATA
PEREQ3:PCIEx4 & PCIEx5 & PCIEx6

FSC	FSB	FSA	CPU	PCIE	SATA
0	0	1	133	100	100
1	0	1	100	100	100

H148-H151 reserve to place GASKET for EMI







<http://hobi-elektronika.net>

<Core Design>

Title : Diamondville_PWR

ASUSTek Computer INC. **Engineer: Satan He**

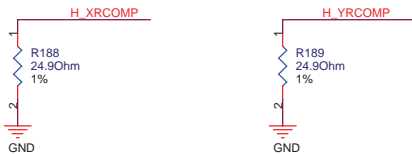
Size	Project Name	Rev
A3	S101	1.1G

Date: Thursday, July 10, 2008 Sheet 6 of 50

Power :
+VCCP

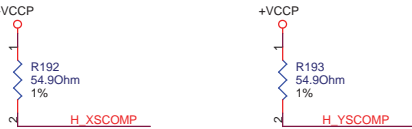
RCOMP

For Calibrating the FSB I/O Buffer



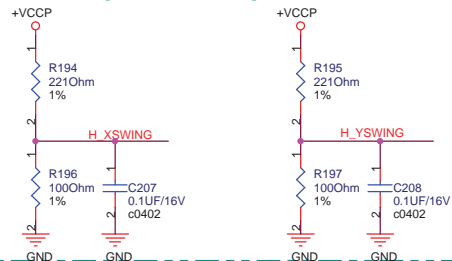
SCOMP

For Slow Rate Compensation on the FSB

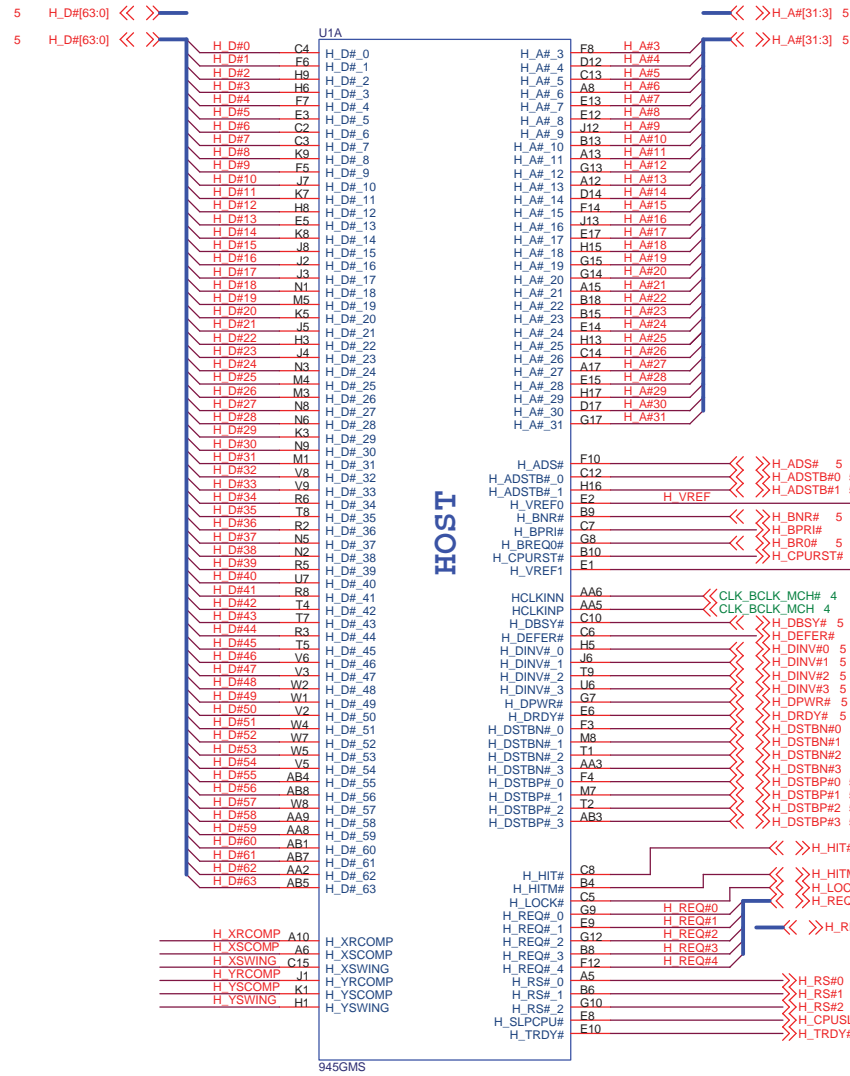


Voltage Swing

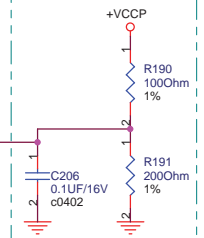
For Providing a Reference Voltage to The FSB RCOMP circuits



Signal voltage level =
0.3125*VCCP
Trace should be 10 mil wide
with 20 mil spacing

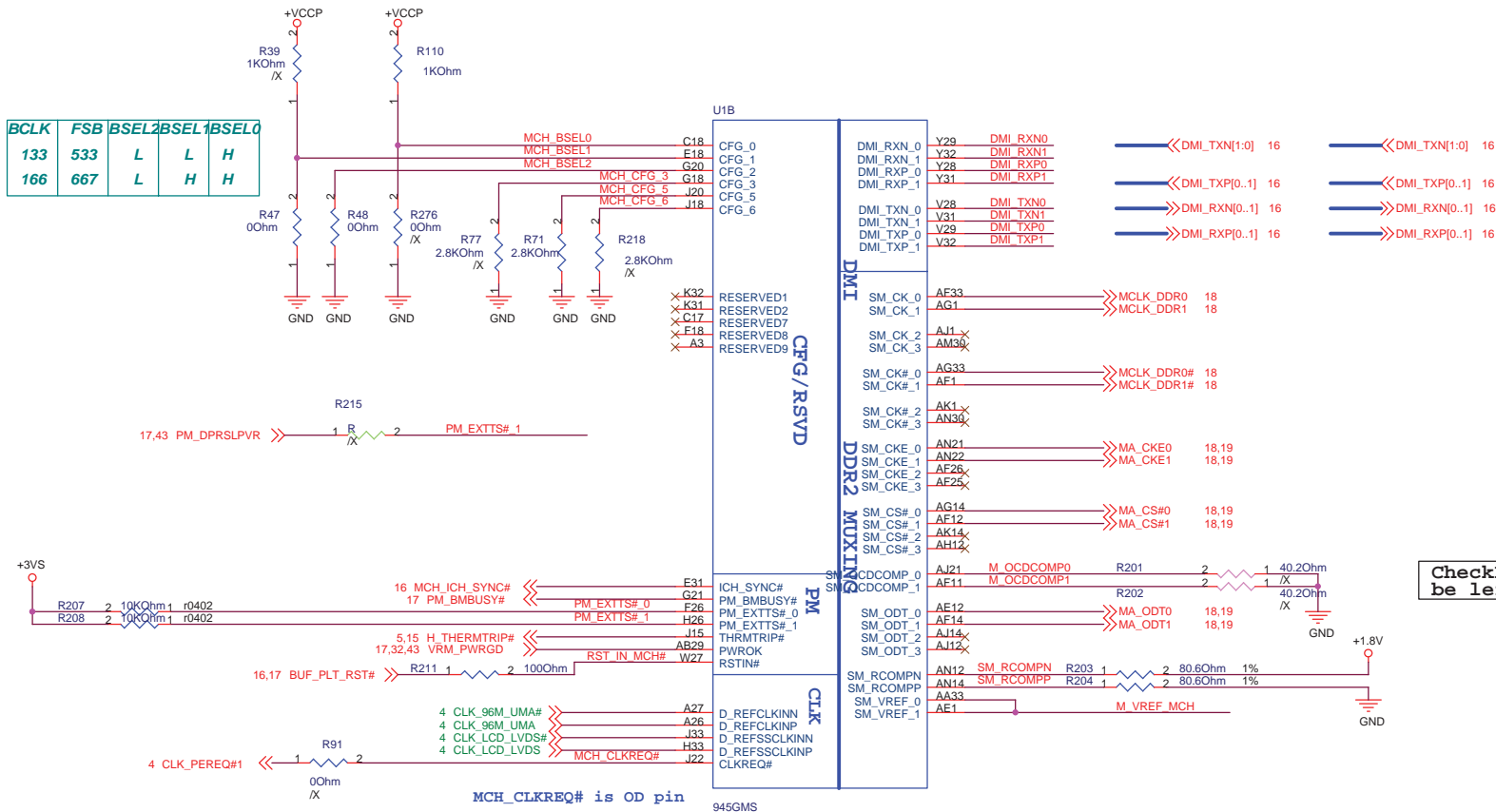


AGTL+ I/O Voltage Reference

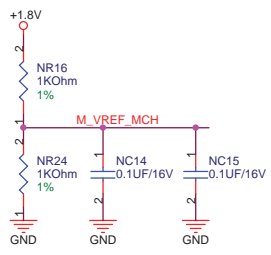


Layout Note:
0.1uF should be placed 100mils or
less from GMCH pin.

BCLK	FSB	BSEL0	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H



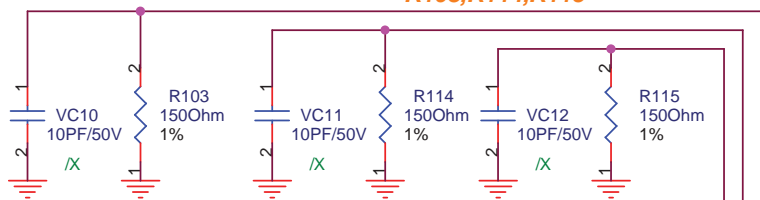
CheckList notes :Can be left as NC



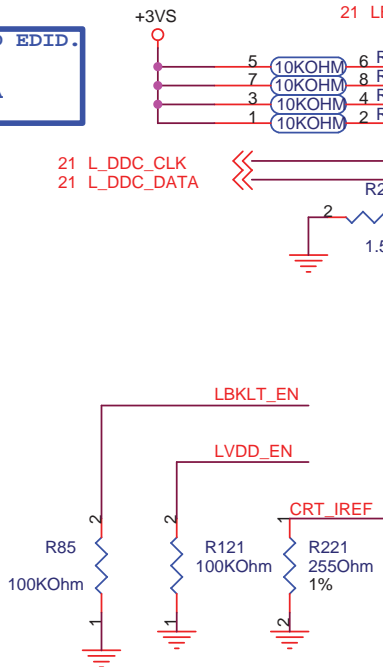
<Core Design>

ASUS		Title : NB-945GMS(DMI & CFG)
ASUSTEK COMPUTER INC.		Engineer: <i>Satan He</i>
Size A3	Project Name S101	Rev 1.1G
Date: Thursday, July 10, 2008	Sheet 8	of 50

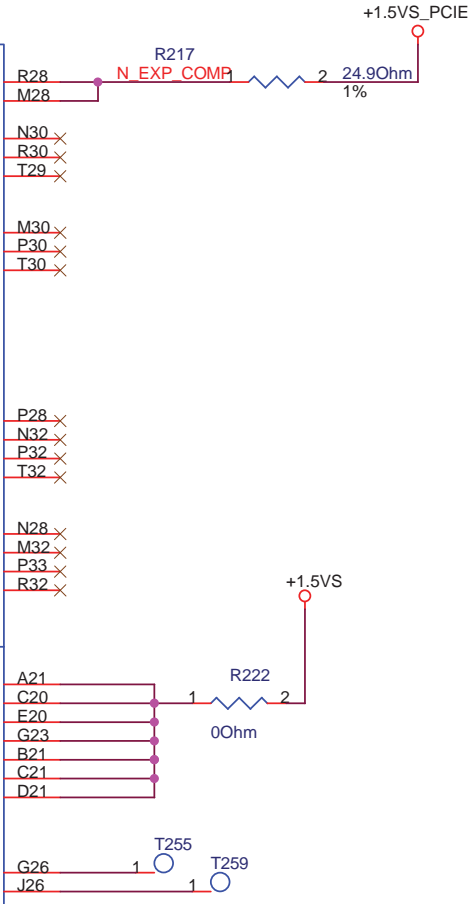
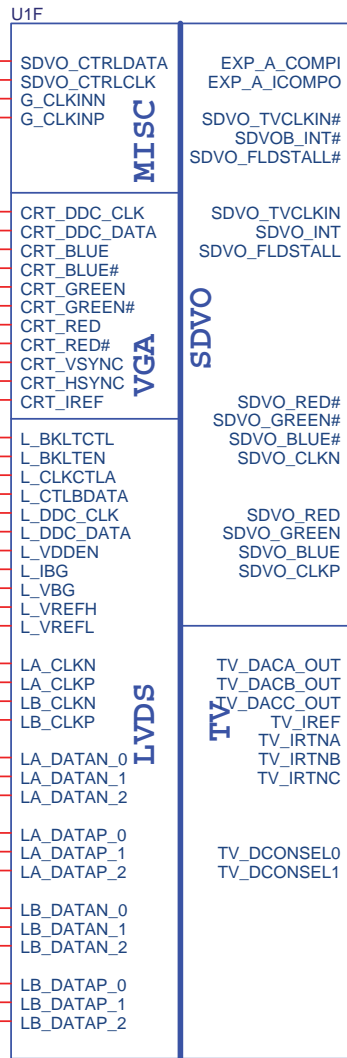
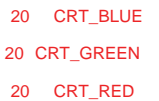
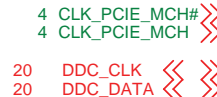
Close to GMCH
R103,R114,R115



IF USE NB READ EDID.
MUST CONNECT
L_DDC_CLK&DATA



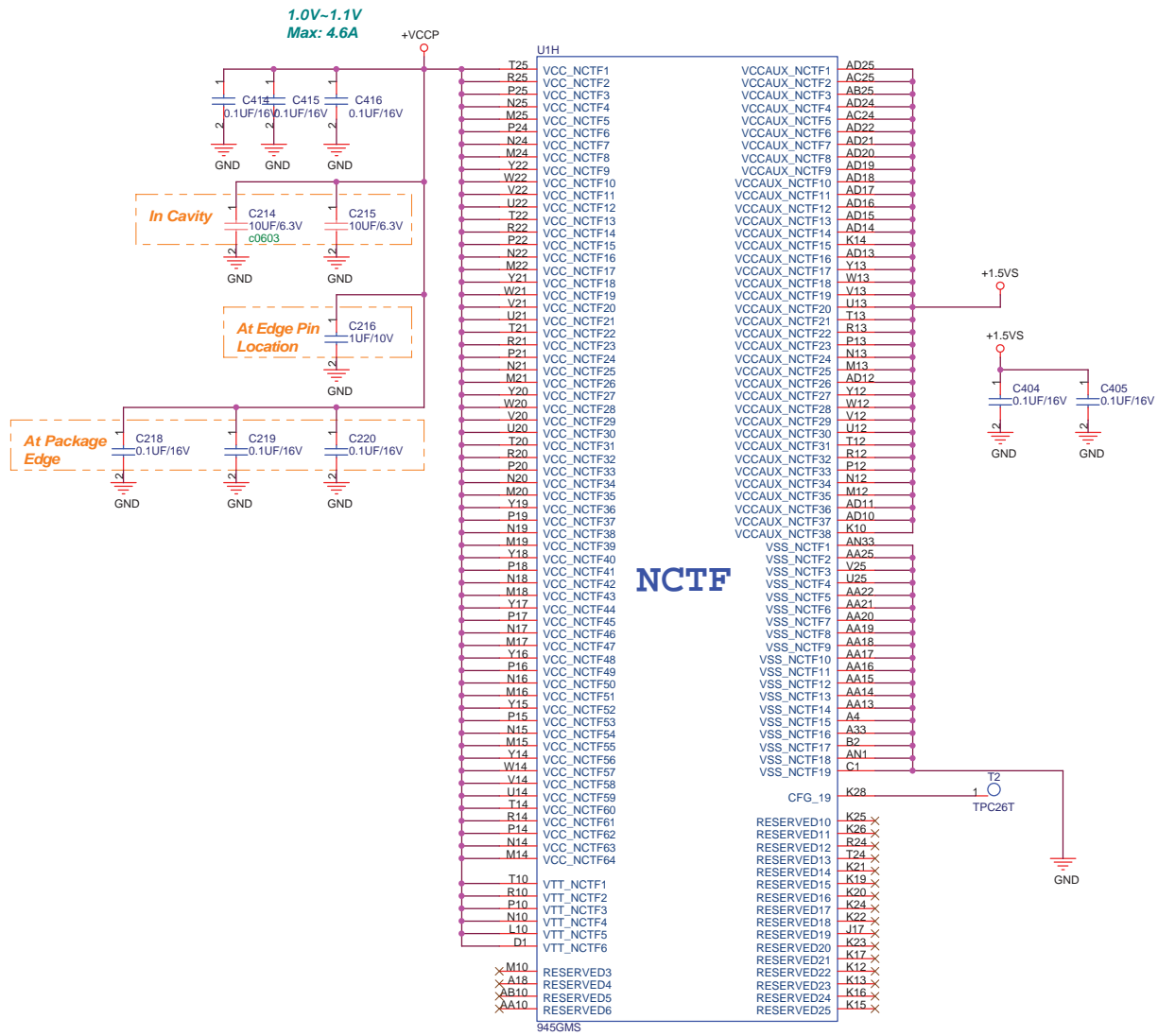
Close to GMCH



945GMS

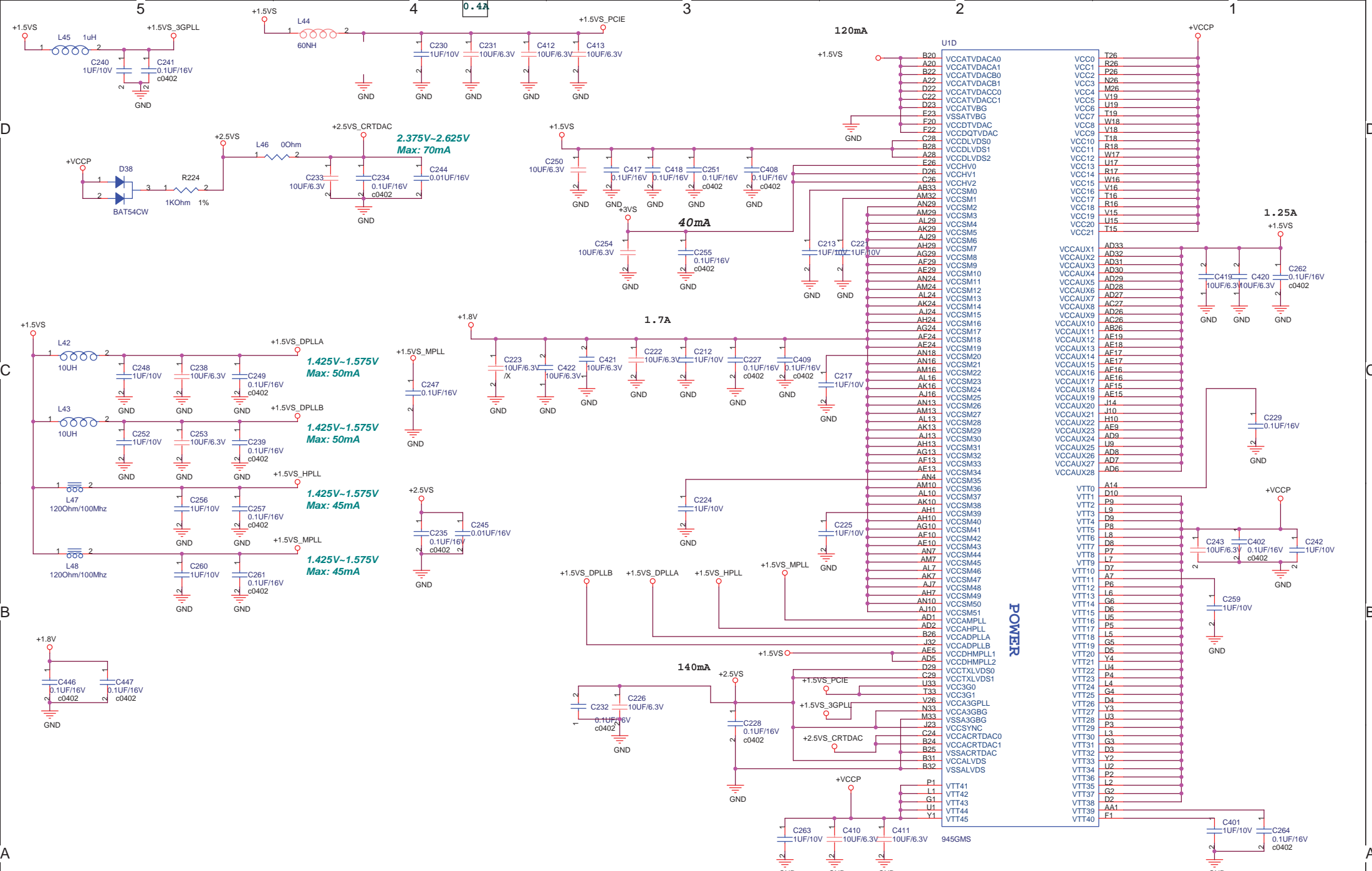
<Core Design>

		Title : NB-945GMS(GRAPHIC)	
ASUSTeK COMPUTER INC.		Engineer: <i>Satan_He</i>	
Size A4	Project Name S101	Rev 1.1G	
Date: Thursday, July 10, 2008	Sheet	9	of 50



NCTF

CFG_19(K28) Strapping :
DMI LANE Reversal:
 0:Normal Operation (Default)
 1.:Reversal Lanes, 3->0,2->1..etc
 Note:945GMS doesn't support DMI Lane Reversal



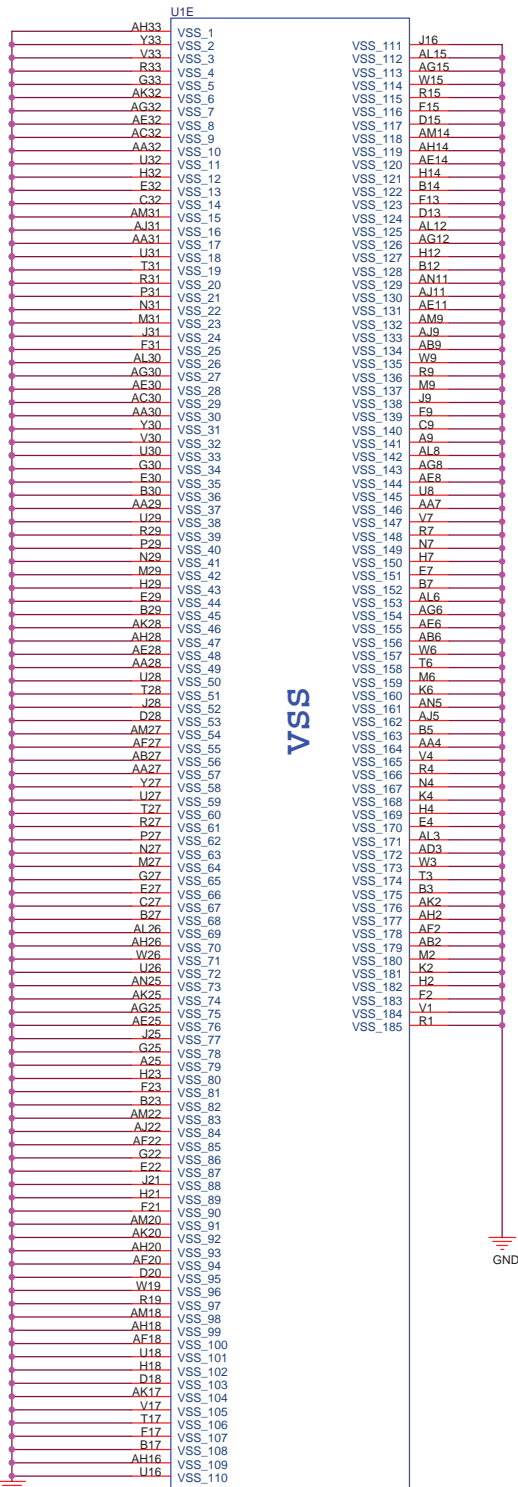
<Core Design>

ASUS Title : NB-945GMS(PWR2)

ASUSTeK COMPUTER INC. Engineer: *Satan He*

Size	Project Name	Rev
A3	S101	1.1G
Date: Thursday, July 10, 2008	Sheet 12 of 50	

<http://hobi-elektronika.net>



U1E

AH33	VSS_1
V33	VSS_2
V33	VSS_3
R33	VSS_4
G33	VSS_5
AK32	VSS_6
AG32	VSS_7
AE32	VSS_8
AC32	VSS_9
AA32	VSS_10
U32	VSS_11
H32	VSS_12
E32	VSS_13
C32	VSS_14
AM31	VSS_15
AJ31	VSS_16
AA31	VSS_17
U31	VSS_18
T31	VSS_19
R31	VSS_20
P31	VSS_21
N31	VSS_22
M31	VSS_23
J31	VSS_24
F31	VSS_25
AL30	VSS_26
AG30	VSS_27
AE30	VSS_28
AC30	VSS_29
AA30	VSS_30
Y30	VSS_31
V30	VSS_32
U30	VSS_33
G30	VSS_34
E30	VSS_35
B30	VSS_36
AA29	VSS_37
U29	VSS_38
R29	VSS_39
P29	VSS_40
N29	VSS_41
M29	VSS_42
H29	VSS_43
E29	VSS_44
B29	VSS_45
AK28	VSS_46
AH28	VSS_47
AE28	VSS_48
AA28	VSS_49
U28	VSS_50
T28	VSS_51
J28	VSS_52
D28	VSS_53
AM27	VSS_54
AE27	VSS_55
AB27	VSS_56
AA27	VSS_57
Y27	VSS_58
U27	VSS_59
T27	VSS_60
R27	VSS_61
P27	VSS_62
N27	VSS_63
M27	VSS_64
G27	VSS_65
E27	VSS_66
C27	VSS_67
B27	VSS_68
AL26	VSS_69
AH26	VSS_70
W26	VSS_71
U26	VSS_72
AN25	VSS_73
AK25	VSS_74
AG25	VSS_75
AE25	VSS_76
J25	VSS_77
G25	VSS_78
A25	VSS_79
H23	VSS_80
F23	VSS_81
B23	VSS_82
AM22	VSS_83
AJ22	VSS_84
AE22	VSS_85
G22	VSS_86
E22	VSS_87
J21	VSS_88
H21	VSS_89
F21	VSS_90
AM20	VSS_91
AK20	VSS_92
AH20	VSS_93
AE20	VSS_94
D20	VSS_95
W19	VSS_96
R19	VSS_97
AM18	VSS_98
AH18	VSS_99
AE18	VSS_100
U18	VSS_101
H18	VSS_102
D18	VSS_103
AK17	VSS_104
V17	VSS_105
T17	VSS_106
F17	VSS_107
B17	VSS_108
AH16	VSS_109
U16	VSS_110

J16

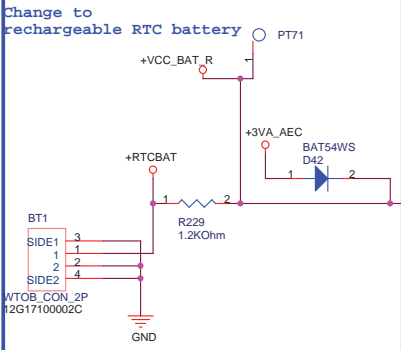
VSS_111	AL15
VSS_112	AG15
VSS_113	W15
VSS_114	R15
VSS_115	F15
VSS_116	D15
VSS_117	AM14
VSS_118	AH14
VSS_119	AE14
VSS_120	H14
VSS_121	B14
VSS_122	F13
VSS_123	D13
VSS_124	AL12
VSS_125	AG12
VSS_126	H12
VSS_127	B12
VSS_128	AM11
VSS_129	AJ11
VSS_130	AE11
VSS_131	AM9
VSS_132	AJ9
VSS_133	AB9
VSS_134	W9
VSS_135	R9
VSS_136	M9
VSS_137	J9
VSS_138	F9
VSS_139	O8
VSS_140	A9
VSS_141	AL8
VSS_142	AG8
VSS_143	AE8
VSS_144	U8
VSS_145	AA7
VSS_146	V7
VSS_147	R7
VSS_148	N7
VSS_149	H7
VSS_150	E7
VSS_151	B7
VSS_152	AL6
VSS_153	AG6
VSS_154	AE6
VSS_155	AB6
VSS_156	W6
VSS_157	T6
VSS_158	M6
VSS_159	K6
VSS_160	AN5
VSS_161	AJ5
VSS_162	B5
VSS_163	AA4
VSS_164	V4
VSS_165	R4
VSS_166	N4
VSS_167	K4
VSS_168	H4
VSS_169	E4
VSS_170	AL3
VSS_171	AD3
VSS_172	W3
VSS_173	T3
VSS_174	B3
VSS_175	AK2
VSS_176	AH2
VSS_177	AE2
VSS_178	AB2
VSS_179	M2
VSS_180	K2
VSS_181	H2
VSS_182	F2
VSS_183	V1
VSS_184	R1
VSS_185	

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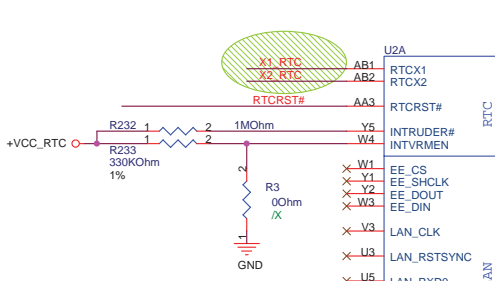
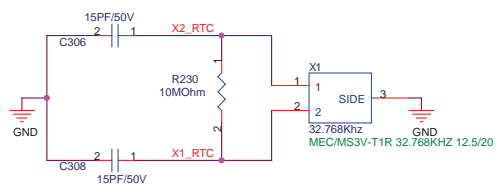
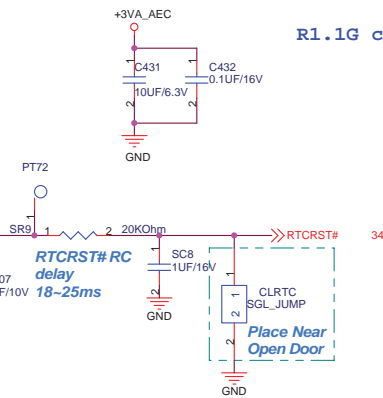
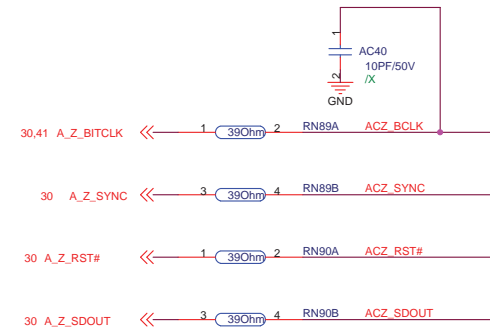
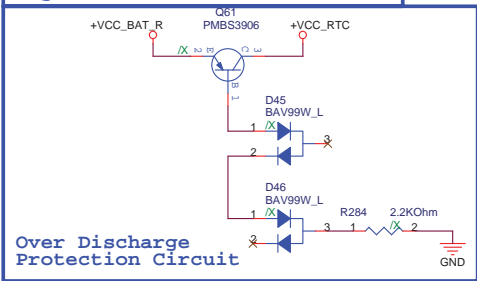
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		Title : NB-945PMS(GND)	
ASUSTeK COMPUTER INC.		Engineer: Satan_He	
Size	Project Name	Rev	
A3	S101	1.1G	
Date: Thursday, July 10, 2008	Sheet	13	of 50

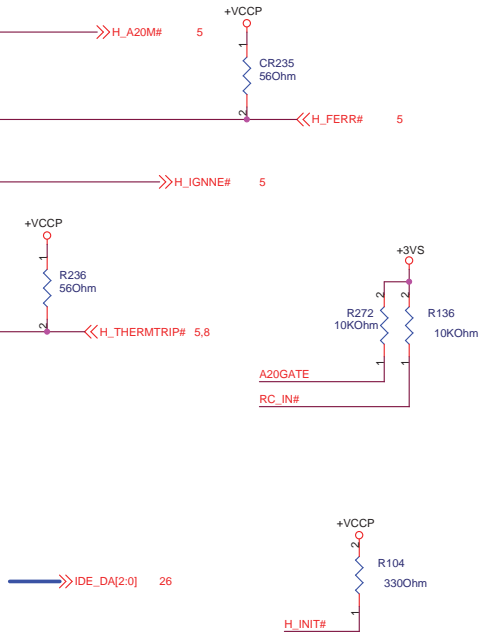
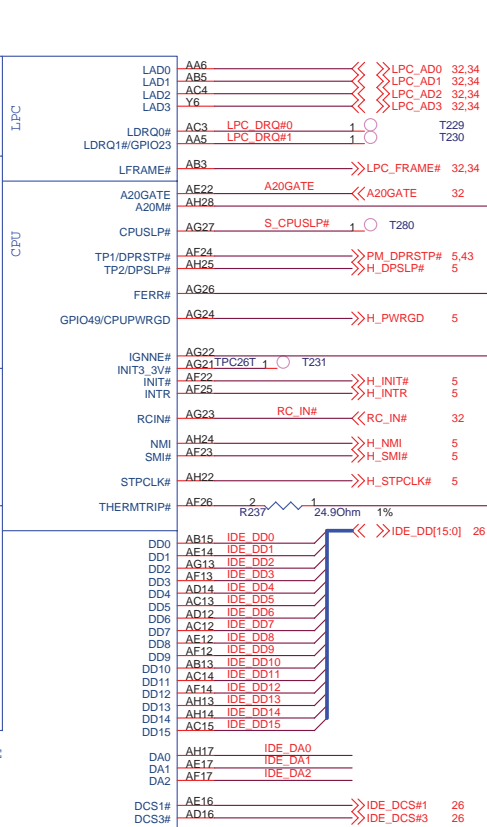
R1.1G change +3VA net to +3VA_AEC

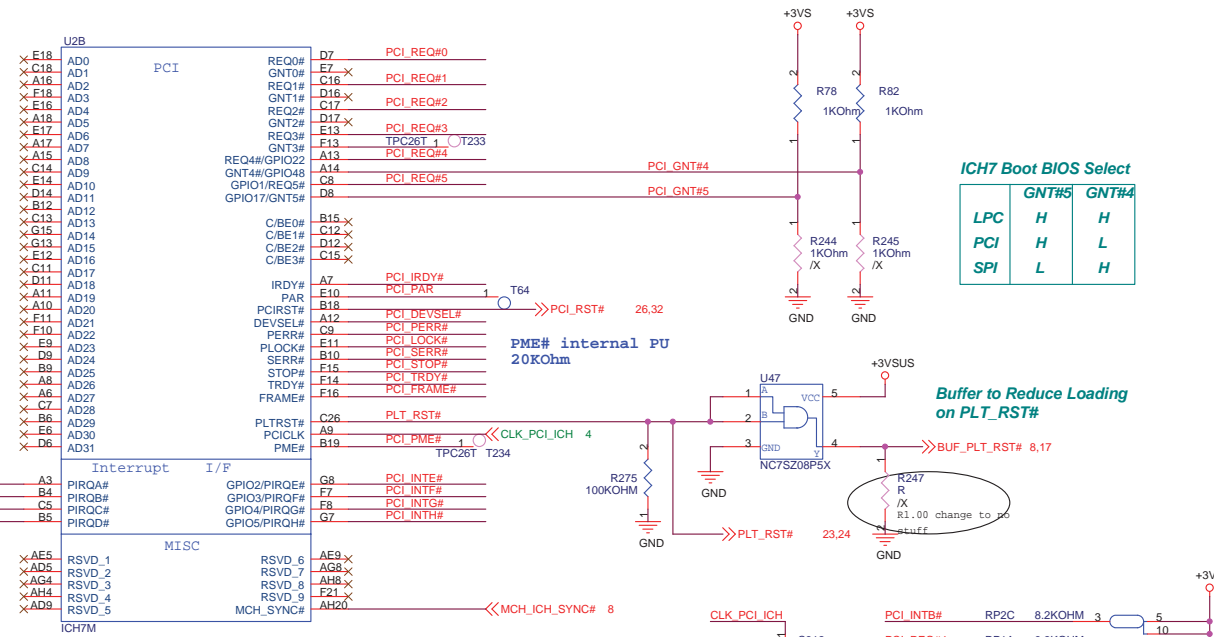


Height : 3.4 mm



ACZ_SDIN0	CODEC
ACZ_SDIN1	NA





ICH7 Boot BIOS Select

	GNT#5	GNT#4
LPC	H	H
PCI	H	L
SPI	L	H

Buffer to Reduce Loading on PLT_RST#

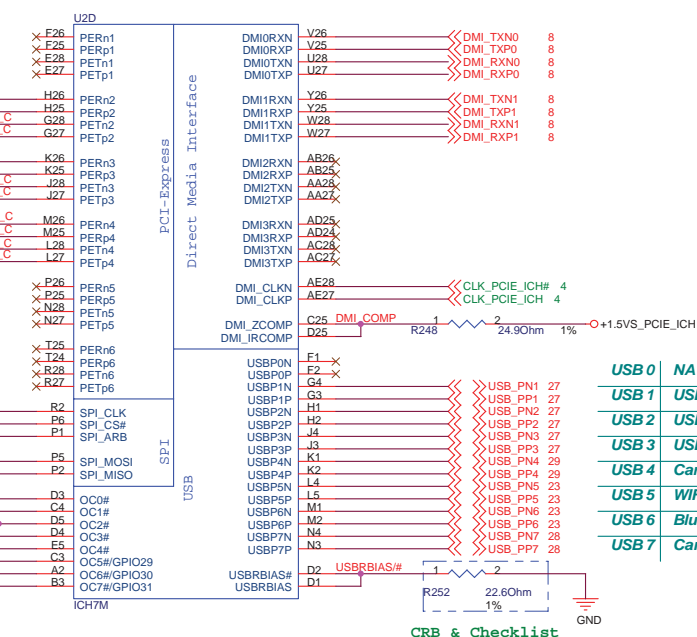
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ASUS Title : SB-ICH7M(2)

ASUSTeK COMPUTER INC. Engineer: Satan He

Size	Project Name	Rev
Custom	S101	1.1G

Date: Thursday, July 10, 2008 Sheet 16 of 50



USB 0	NA
USB 1	USB Conn
USB 2	USB Conn
USB 3	USB Conn
USB 4	Card Reader
USB 5	WIFI
USB 6	Bluetooth
USB 7	Camera

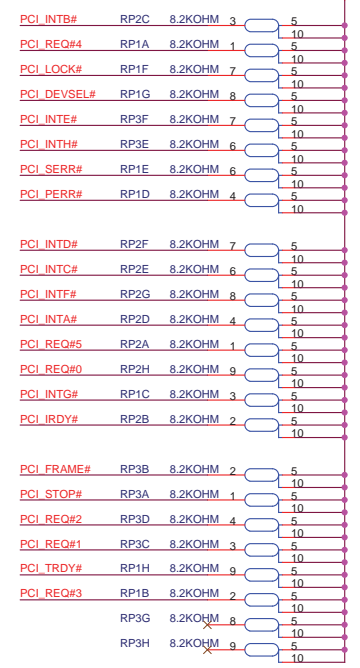
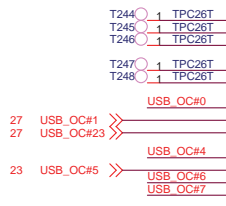
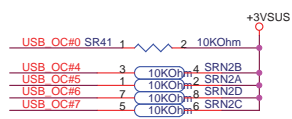
CRB & Checklist

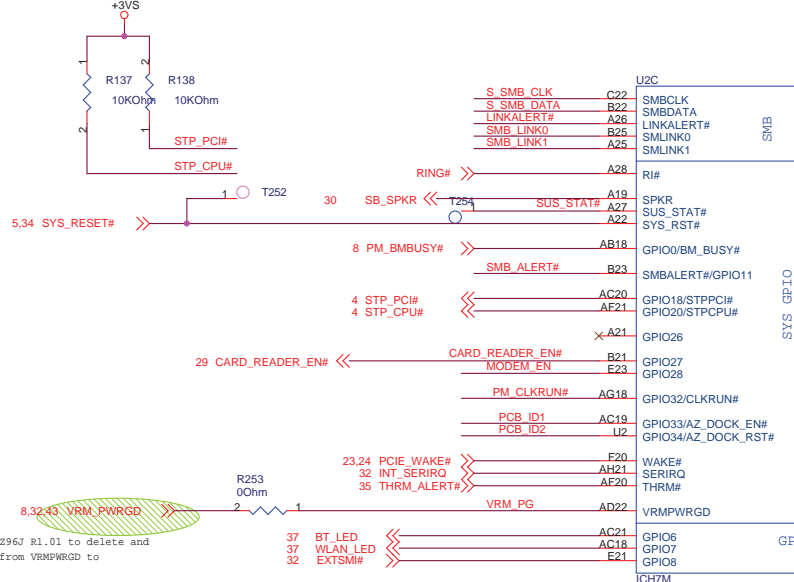
<http://hobi-elektronika.net>

LAN AR8113 IC

WIFI PCIExpress Card

PCIe Interface SSD



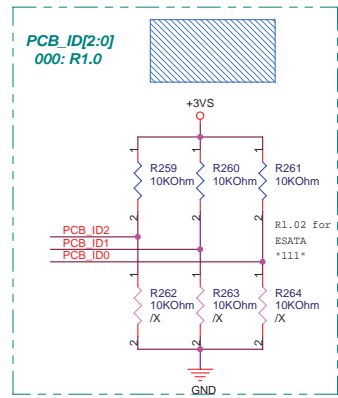
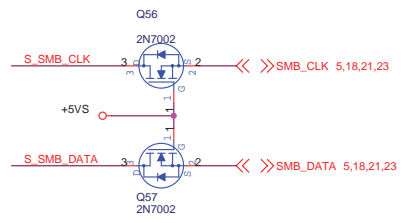


05/12/30, refer Z963 R1.01 to delete and change net name from VRMPWRGD to VRM_PWRGD.

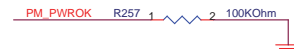
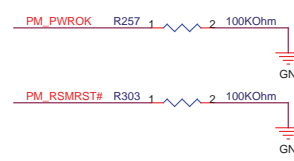
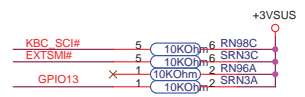
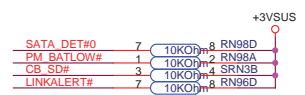
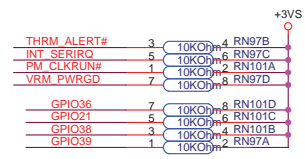
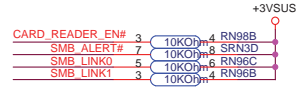
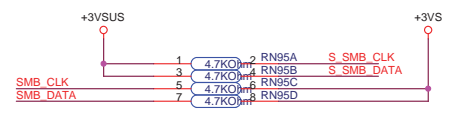
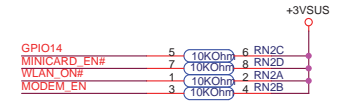
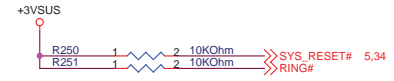
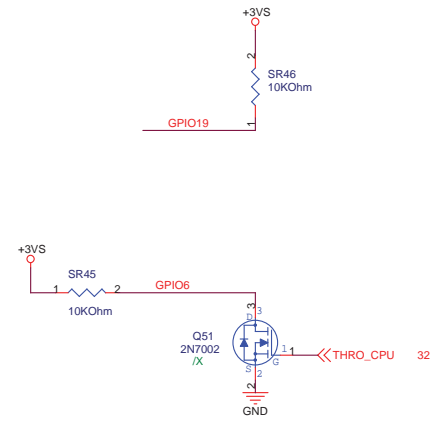
GPIO25 Internal PU 20KOhm

	WLAN_LED	WLAN	BT
High	v	v	v
High	v	v	x
High	x	x	v
Low	x	x	x

S_SMB_CLK >>> S_SMB_CLK 4
S_SMB_DATA >>> S_SMB_DATA 4

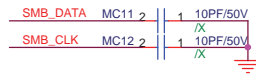
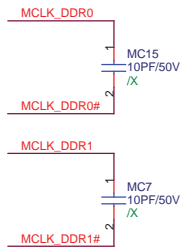


PCB_VID3 : PROJECT CODE



<Core Design>

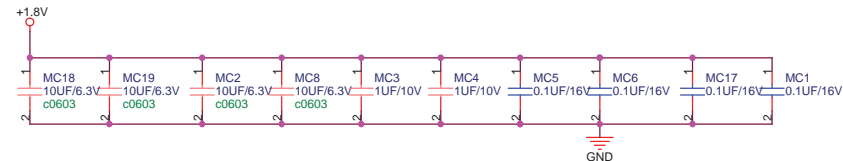
ASUS		Title : SB-ICH7M(3)	
ASUSTek COMPUTER INC		Engineer: Satan He	
Size	Project Name	Rev	
Custom	S101	1.1G	
Date: Thursday, July 10, 2008	Sheet	17	of 50



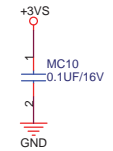
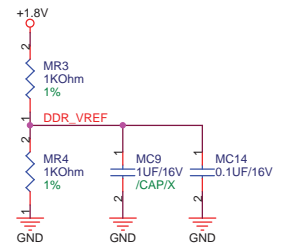
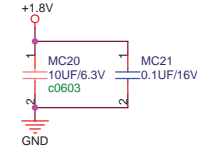
STD Type

- MA_DQ[63:0] 10
- MA_DQS[7:0] 10
- MA_DQS#[7:0] 10
- MA_DM[7:0] 10
- MA_MA[13:0] 10,19
- MA_BA[2:0] 10,19

DDR2 Conn. Height=4.0mm



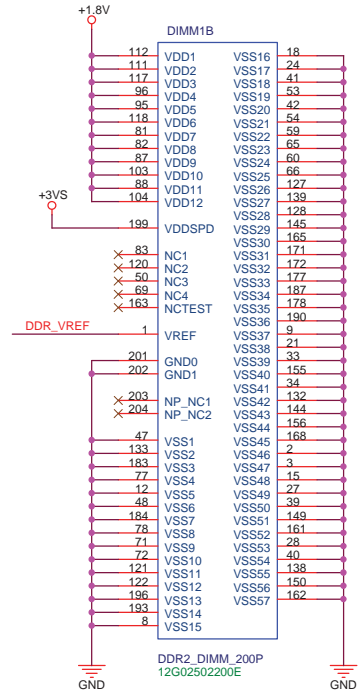
R1.1G MC3 MC4 change to 0603 1uF



DIMM1A		DIMM1B	
MA_MA0	102	A0	DQ0
MA_MA1	101	A1	DQ1
MA_MA2	100	A2	DQ2
MA_MA3	99	A3	DQ3
MA_MA4	98	A4	DQ4
MA_MA5	97	A5	DQ5
MA_MA6	94	A6	DQ6
MA_MA7	92	A7	DQ7
MA_MA8	93	A8	DQ8
MA_MA9	91	A9	DQ9
MA_MA10	105	A10/AP	DQ10
MA_MA11	90	A11	DQ11
MA_MA12	89	A12	DQ12
MA_MA13	116	A13	DQ13
	X 86	A14	DQ14
MA_BA2	X 84	A15	DQ15
	X 85	A16_BA2	DQ16
MA_BA0	107	BA0	DQ17
MA_BA1	106	BA1	DQ18
	110	BA2	DQ19
8,19 MA_CS#0	115	S0#	DQ20
8,19 MA_CS#1	115	S1#	DQ21
8 MCLK_DDR0	30	CK0	DQ22
8 MCLK_DDR0#	32	CK0#	DQ23
8 MCLK_DDR1	164	CK1	DQ24
8 MCLK_DDR1#	166	CK1#	DQ25
8,19 MA_CKE0	79	CKE0	DQ26
8,19 MA_CKE1	80	CKE1	DQ27
10,19 MA_CAS#	113	CAS#	DQ28
10,19 MA_RAS#	108	RAS#	DQ29
10,19 MA_WE#	109	WE#	DQ30
	198	SA0	DQ31
	200	SA1	DQ32
5,17,21,23 SMB_CLK	197	SCL	DQ33
5,17,21,23 SMB_DATA	195	SDA	DQ34
		DQ35	DQ35
8,19 MA_ODT0	114	ODT0	DQ36
8,19 MA_ODT1	119	ODT1	DQ37
		DQ38	DQ38
MA_DM0	10	DM0	DQ39
MA_DM2	26	DM1	DQ40
MA_DM1	52	DM2	DQ41
MA_DM3	67	DM3	DQ42
MA_DM4	147	DM4	DQ43
MA_DM5	130	DM4	DQ43
MA_DM6	170	DM5	DQ44
MA_DM7	185	DM6	DQ45
		DM7	DQ46
		DQ47	DQ47
MA_DQS0	13	DQ48	DQ48
MA_DQS2	31	DQ49	DQ49
MA_DQS1	51	DQ50	DQ50
MA_DQS3	70	DQ51	DQ51
MA_DQS4	131	DQ52	DQ52
MA_DQS5	148	DQ53	DQ53
MA_DQS6	169	DQ54	DQ54
MA_DQS7	188	DQ55	DQ55
MA_DQS#0	11	DQ56	DQ56
MA_DQS#2	29	DQ57	DQ57
MA_DQS#1	49	DQ58	DQ58
MA_DQS#3	68	DQ59	DQ59
MA_DQS#4	129	DQ60	DQ60
MA_DQS#5	146	DQ61	DQ61
MA_DQS#6	167	DQ62	DQ62
MA_DQS#7	186	DQ63	DQ63

DDR2_DIMM_200P
12G02502200E

GROUP1
GROUP2
SWAP



DDR2_DIMM_200P
12G02502200E

<http://hobi-elektronika.net>



<Core Design>

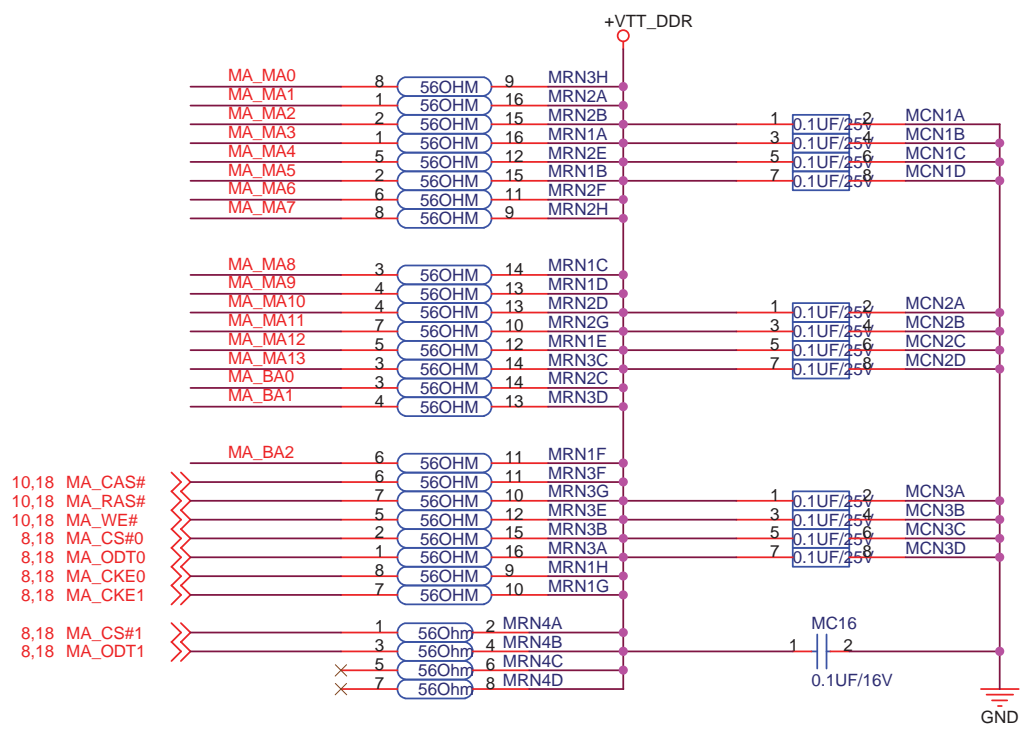
ASUS Title : DDR2 SODIMM

ASUSTek Computer INC. Engineer: *Kell_Huang*


Size	Project Name	Rev
A3	S101	1.1G

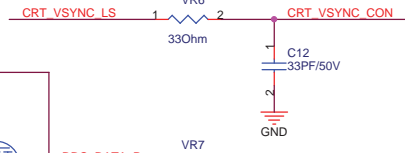
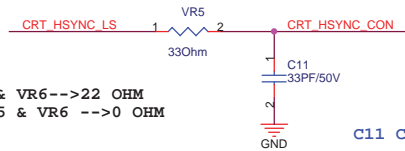
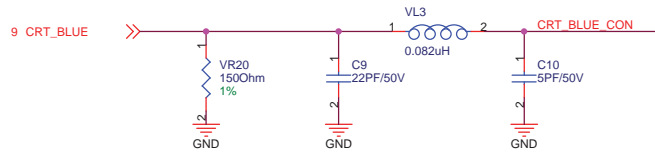
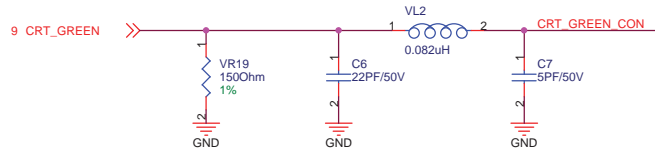
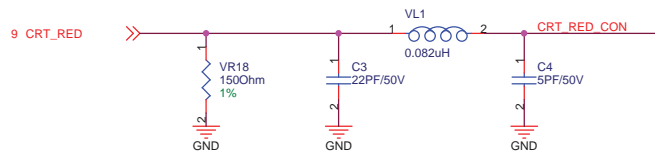
Date: Thursday, July 10, 2008 Sheet 18 of 50

 << MA_MA[13:0] 10,18
 << MA_BA[2:0] 10,18



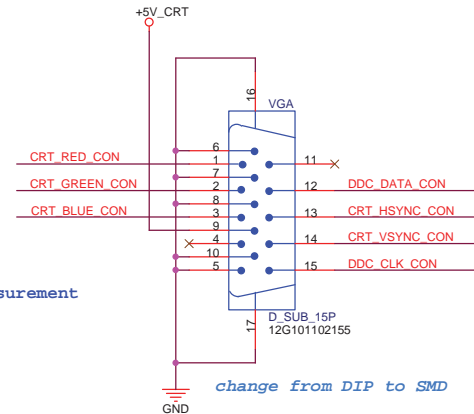
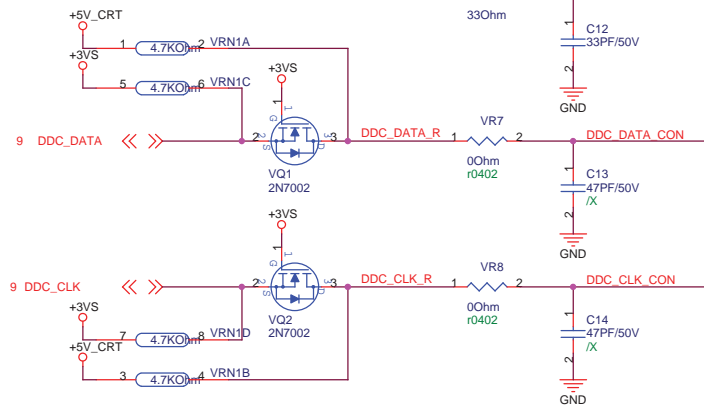
<Core Design>

		Title : DDR2_Termination	
ASUSTek Computer INC.		Engineer: <i>Kell_Huang</i>	
Size A4	Project Name S101	Rev 1.1G	
Date: Thursday, July 10, 2008		Sheet	19 of 50

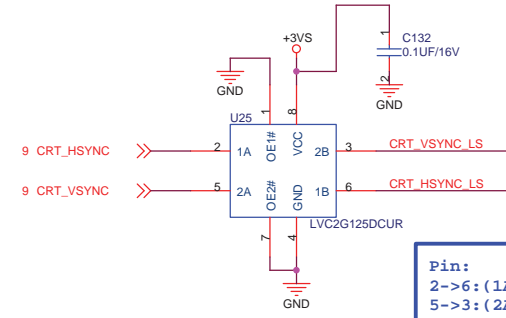


U25上:VR5 & VR6-->22 OHM
U25 /X :VR5 & VR6 -->0 OHM

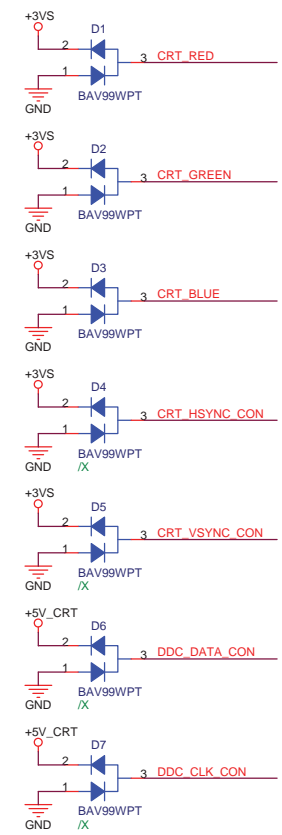
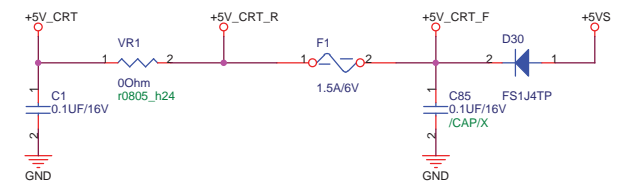
C11 C12 for EA measurement

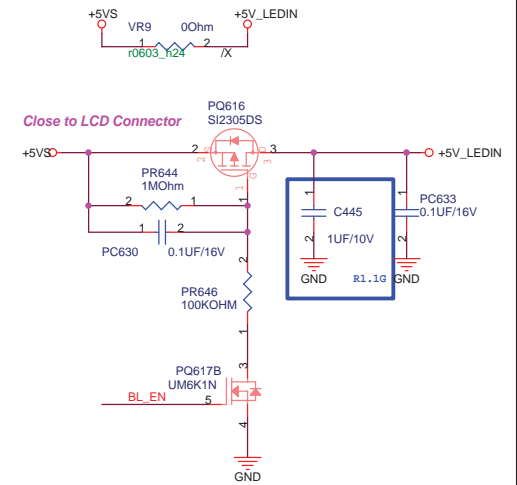
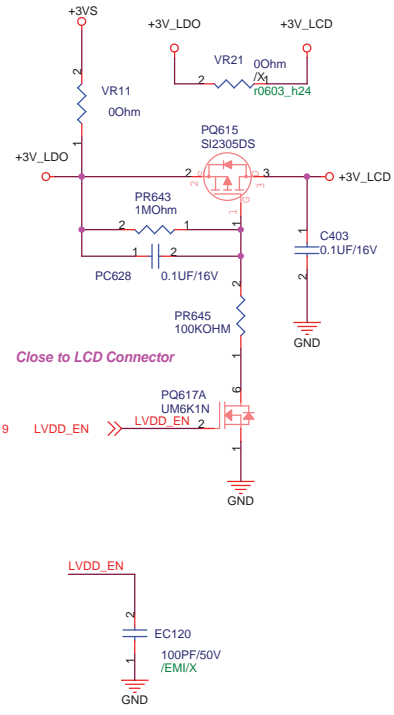
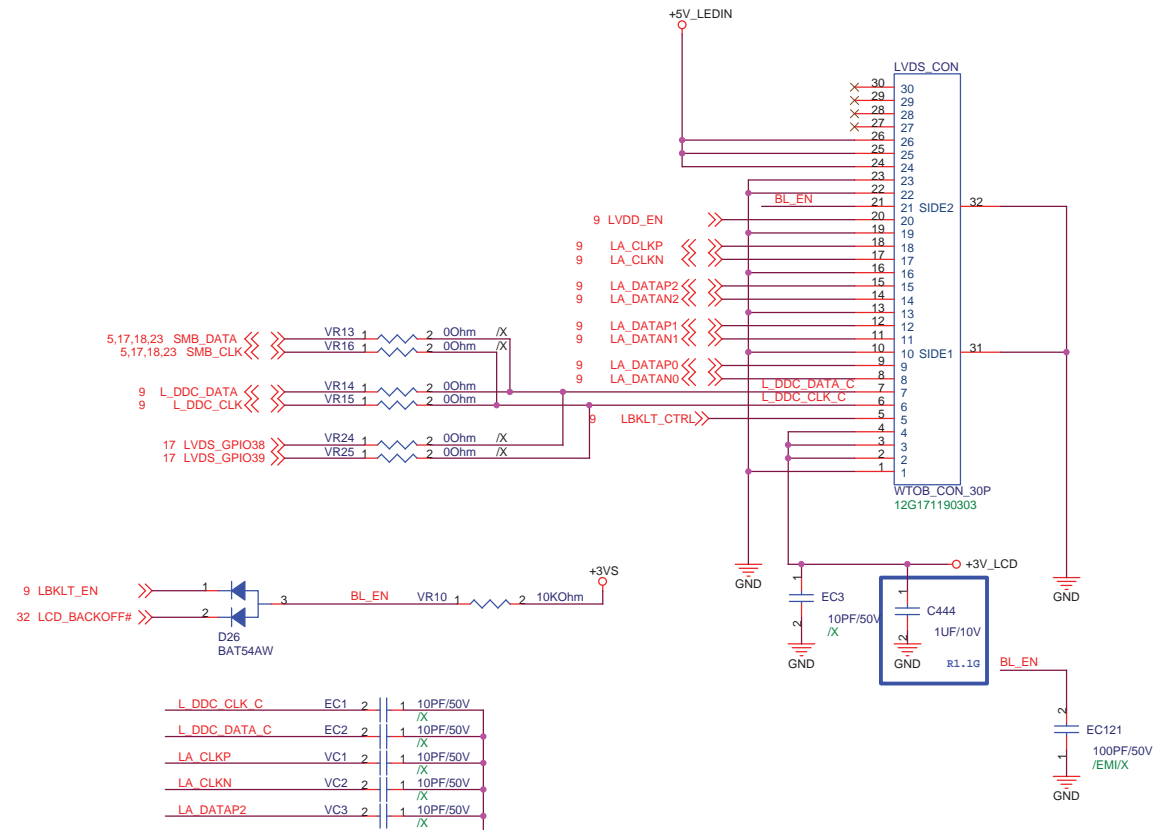


VGA use 12G10110015W
VGA use 12G101102155, but use 12G10110015W footprint



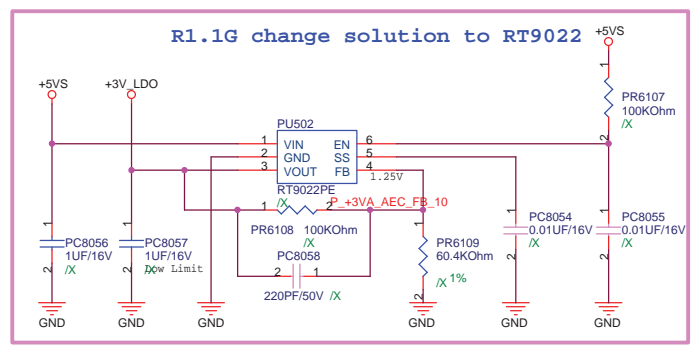
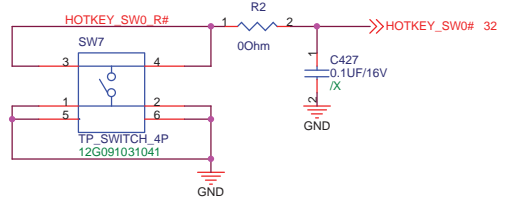
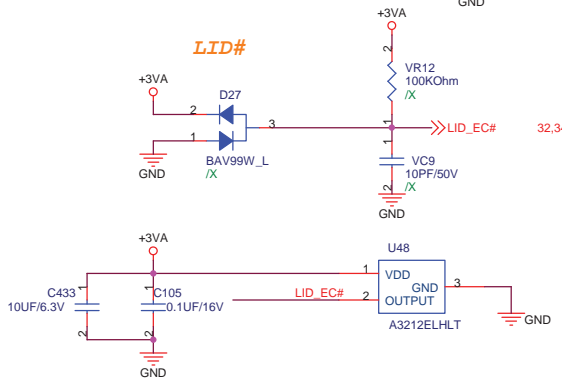
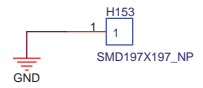
Pin:
2->6: (1A->1B)
5->3: (2A->2B)





L_DDC_CLK C	EC1	2	1	10PF/50V
L_DDC_DATA C	EC2	2	1	10PF/50V
LA_CLKP	VC1	2	1	10PF/50V
LA_CLKN	VC2	2	1	10PF/50V
LA_DATAP2	VC3	2	1	10PF/50V
LA_DATAN2	VC4	2	1	10PF/50V
LA_DATAP1	VC5	2	1	10PF/50V
LA_DATAN1	VC6	2	1	10PF/50V
LA_DATAP0	VC7	2	1	10PF/50V
LA_DATAN0	VC8	2	1	10PF/50V

H153 : Pad for EMI




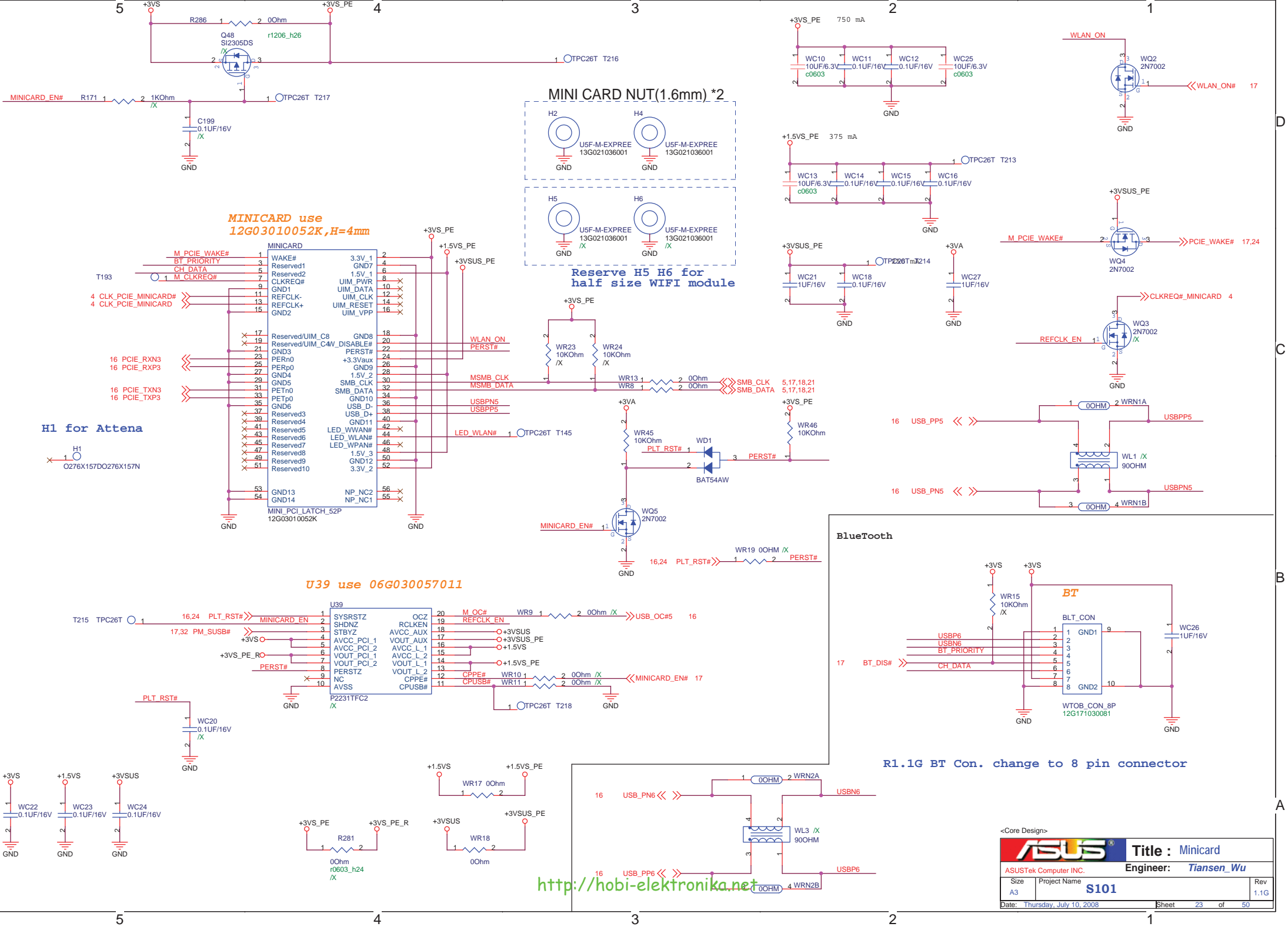
<http://hobi-elektronika.net>

<Core Design>		ASUS Title : LVDS Conn_LID	
ASUSTek Computer INC.		Engineer: <i>Kell_Huang</i>	
Size	A3	Project Name	S101
Date:	Thursday, July 10, 2008	Sheet	21 of 50
		Rev	1.1G

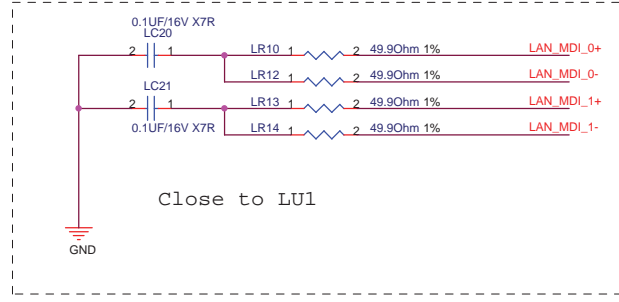
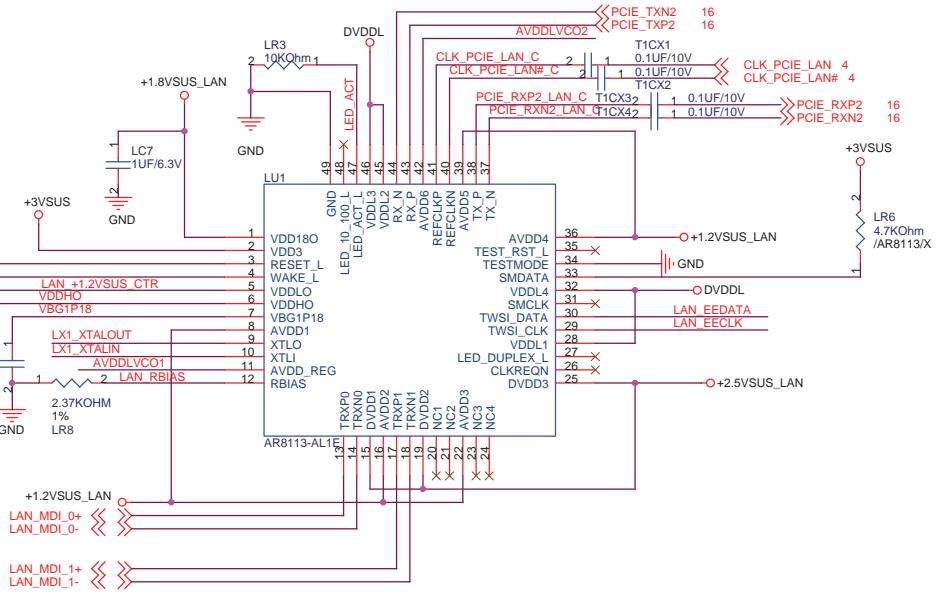
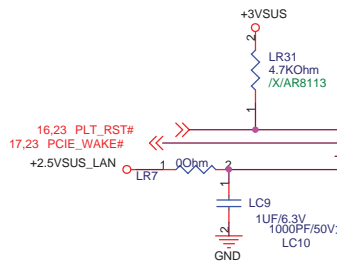
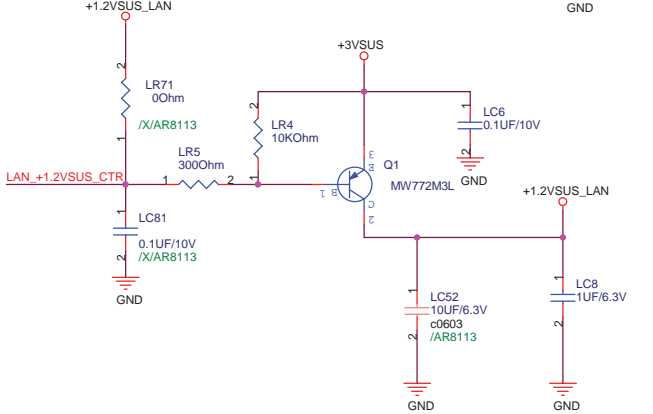
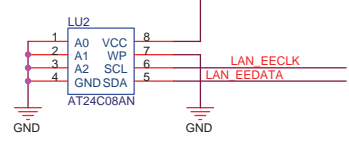
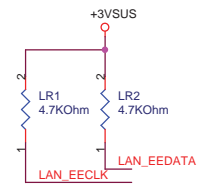
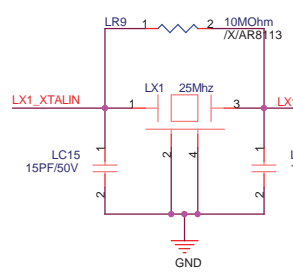
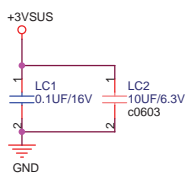
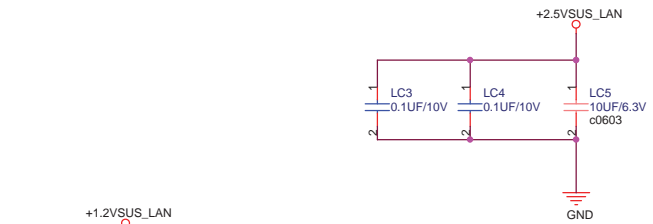
<http://hobi-elektronika.net>

<Core Design>

		Title : Blank	
ASUSTek Computer INC.		Engineer: <i>Kell_Huang</i>	
Size	Project Name		Rev
A3	S101		1.1G
Date: Thursday, July 10, 2008		Sheet	22 of 50

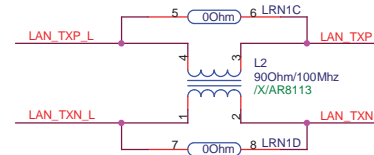
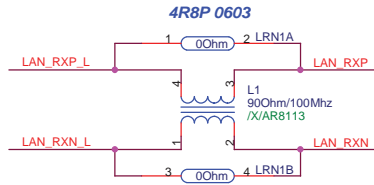


<http://hobi-elektronika.net>

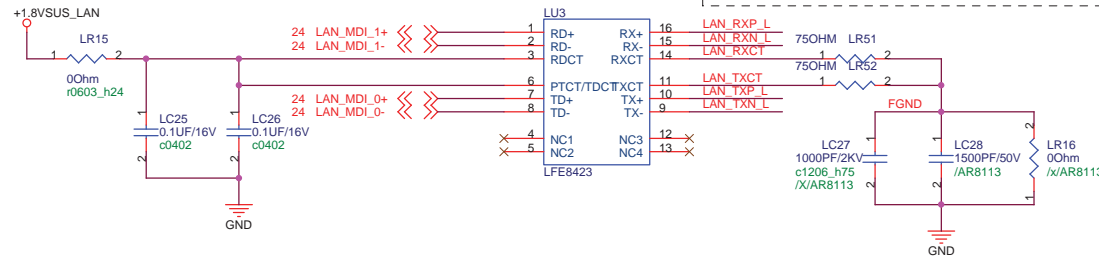
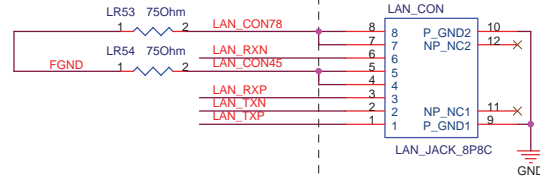


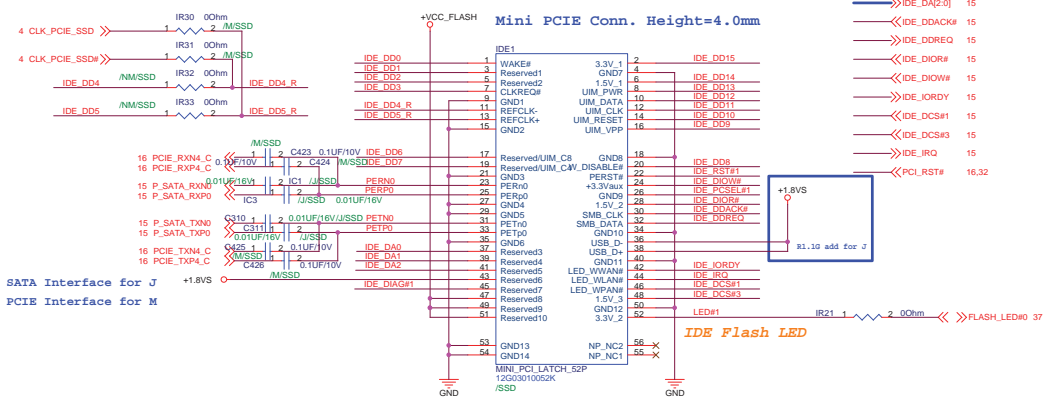
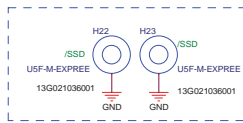
Close to LU1

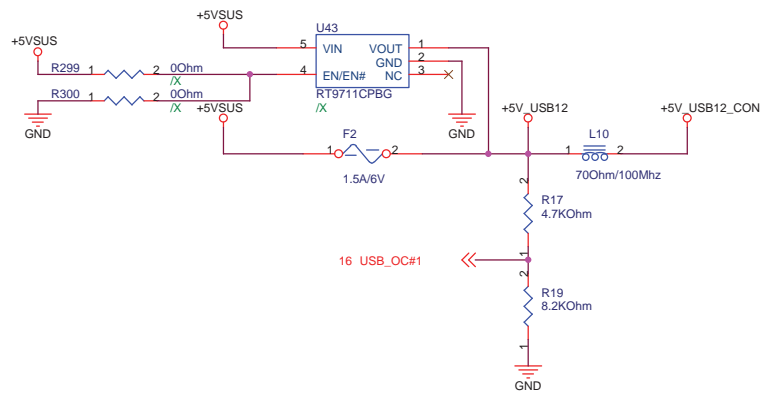
if overclocking LL3 Kept and LL2 removed
if not overclocking LL3 removed and LL2 Kept



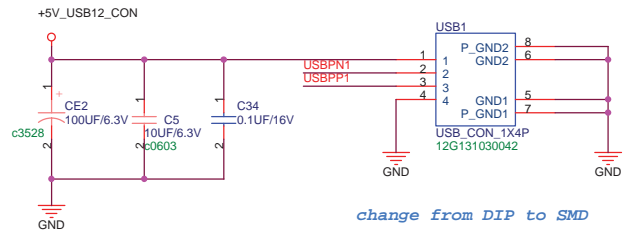
LAN connector: 12G148101086
SMT type





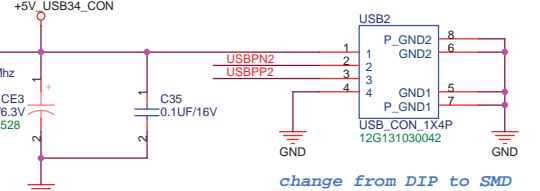
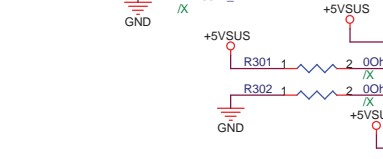
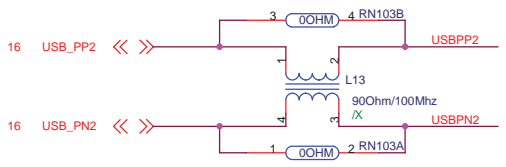
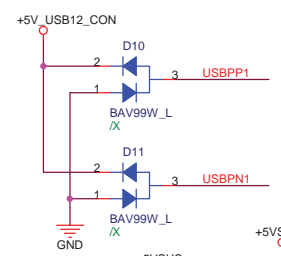
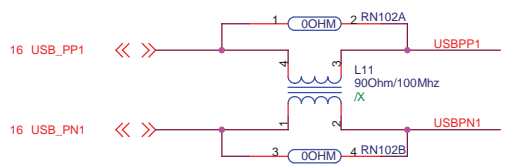


1.1G change USB con. to 12G131030042

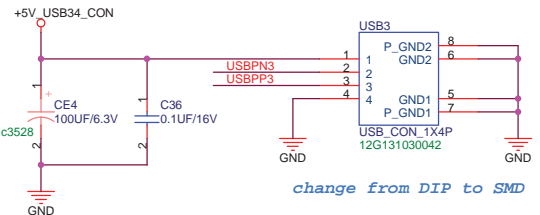
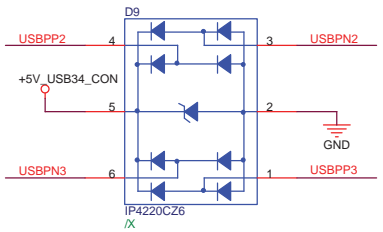
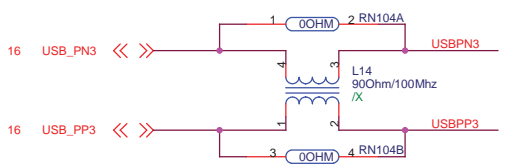


change from DIP to SMD

1.1G change CE2 CE3 CE4 to POSCAP, 100uF/6.3V



change from DIP to SMD

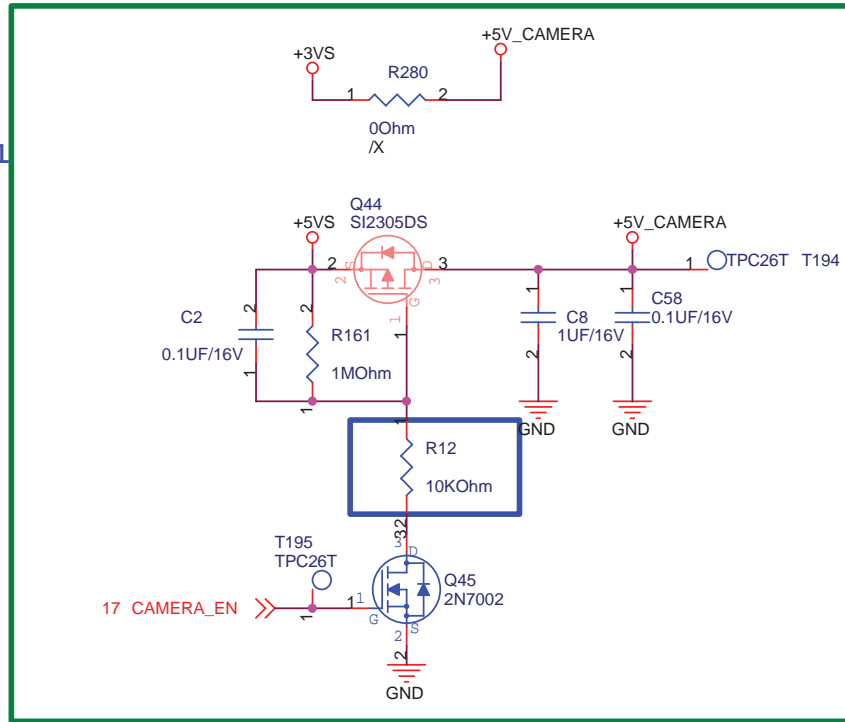


change from DIP to SMD

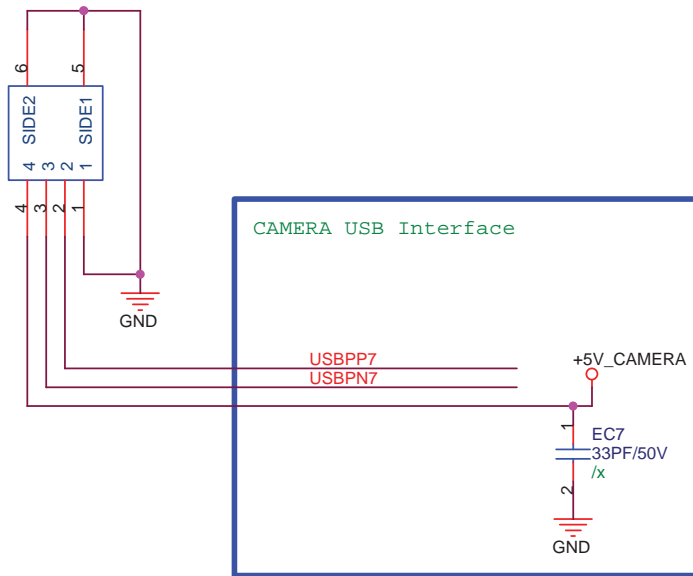
<http://hobi-elektronika.net>

<Core Design>		ASUS Title : USB Port	
ASUSTek Computer INC.		Engineer: <i>Kell_Huang</i>	
Size	Project Name		
A3	S101		
Date: Thursday, July 10, 2008	Sheet	27 of 50	Rev 1.1G

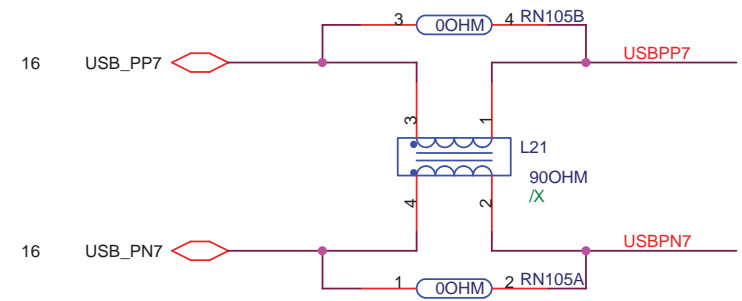
Power Control



CAMERA
WTOB_CON_4P
12G171030040

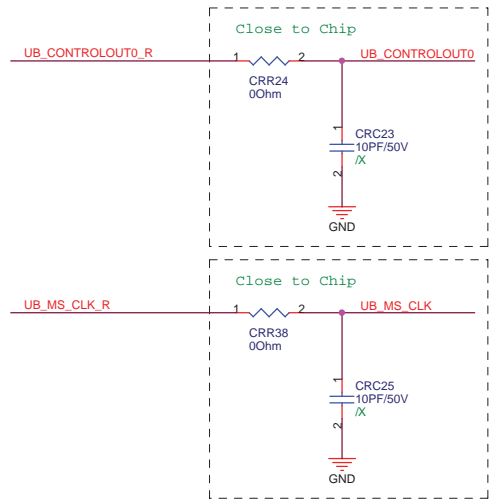
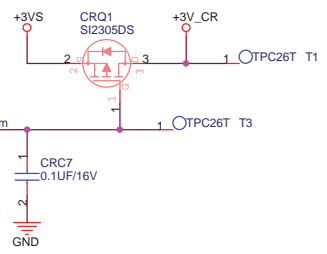
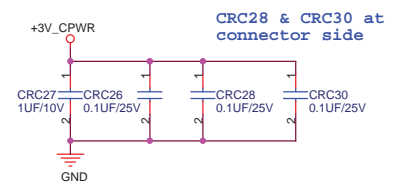
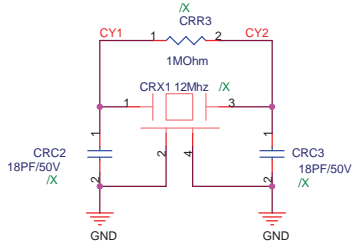
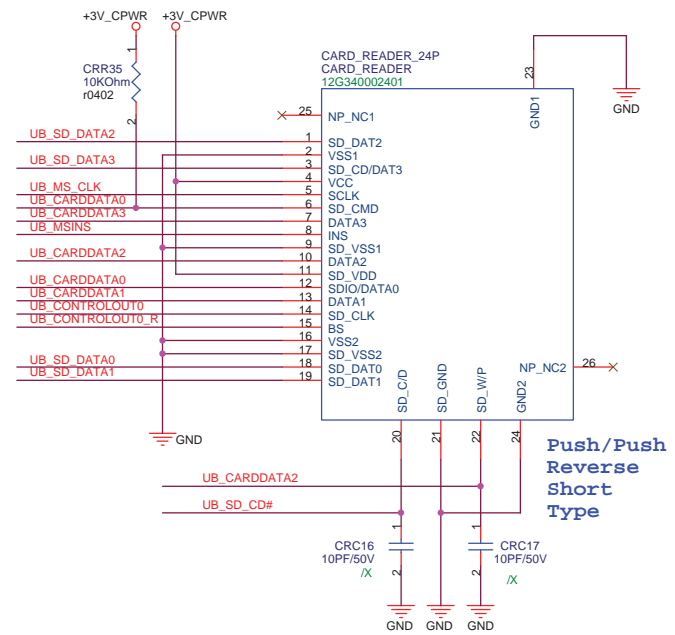
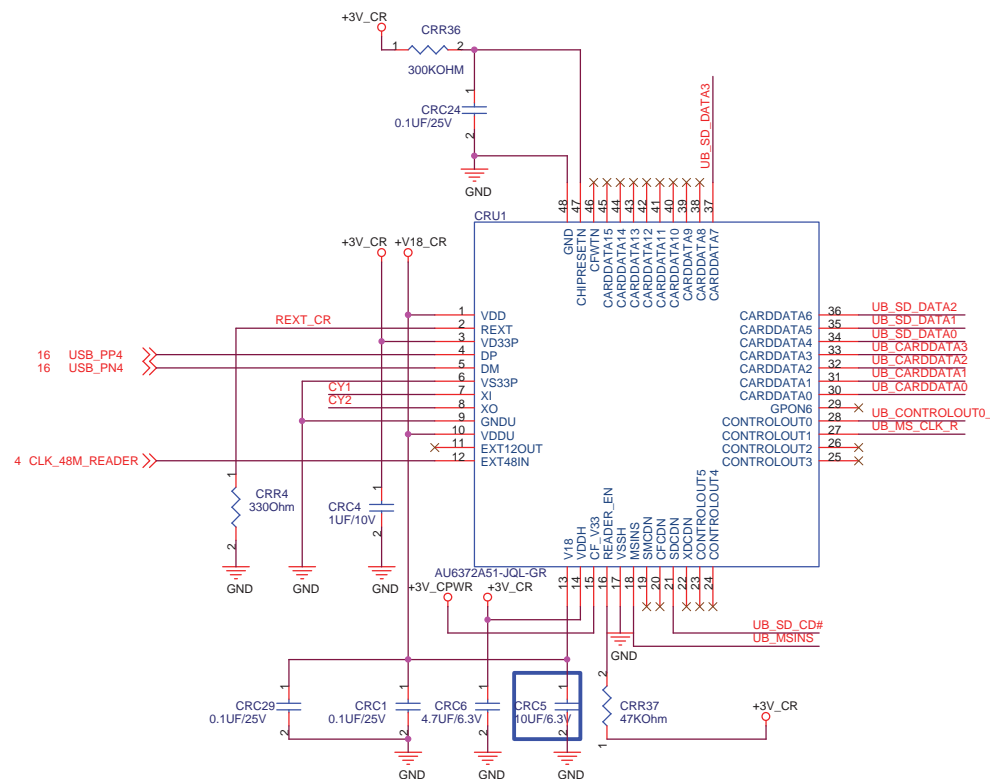


<http://hobi-elektronika.net>



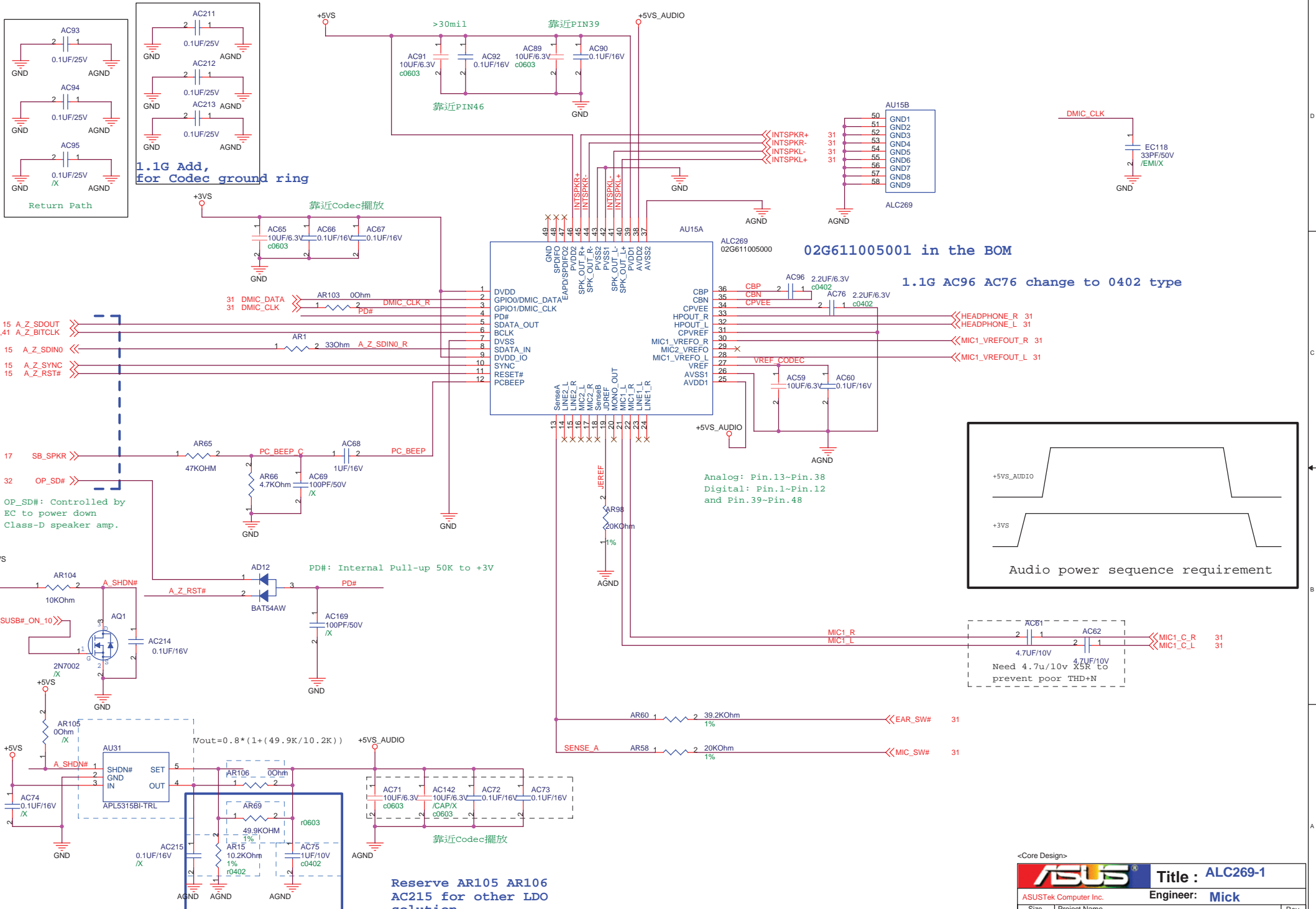
<Core Design>

ASUS		Title : Camera Power	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size A4	Project Name S101	Rev 1.1G	
Date: Thursday, July 10, 2008		Sheet	28 of 50



SDWP: Internal Pull-up
 SDCDN: Internal Pull-up
 SDWP = 1 Write protect
 SDWP = 0 Write-able
 SDCDN = 1 No card
 SDCDN = 0 Card inserted

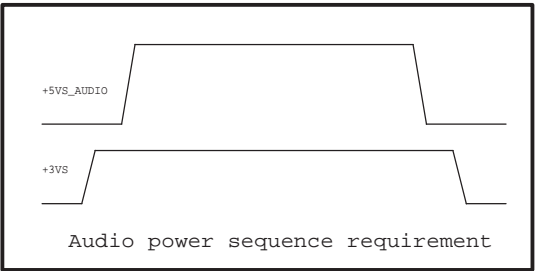
Card Insert: Pin.10 and Pin.12 are Shorted.
 Card not Insert: Pin.10 and Pin.12 are Opened.
 Write Protect: Pin.11 and Pin.12 are Opened.
 Write Enable: Pin.11 and Pin.12 are Shorted.



1.1G Add,
for Codec ground ring

02G611005001 in the BOM

1.1G AC96 AC76 change to 0402 type



Analog: Pin.13~Pin.38
Digital: Pin.1~Pin.12
and Pin.39~Pin.48

For Audio Noise Issue

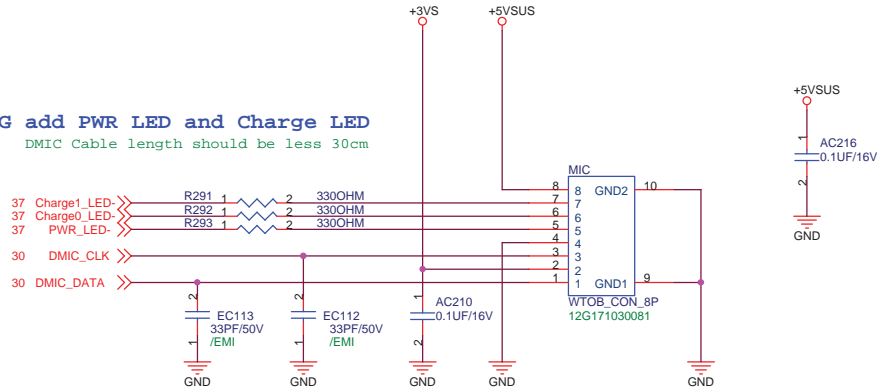
Reserve AR105 AR106
AC215 for other LDO
solution

<http://hobi-elektronika.net>

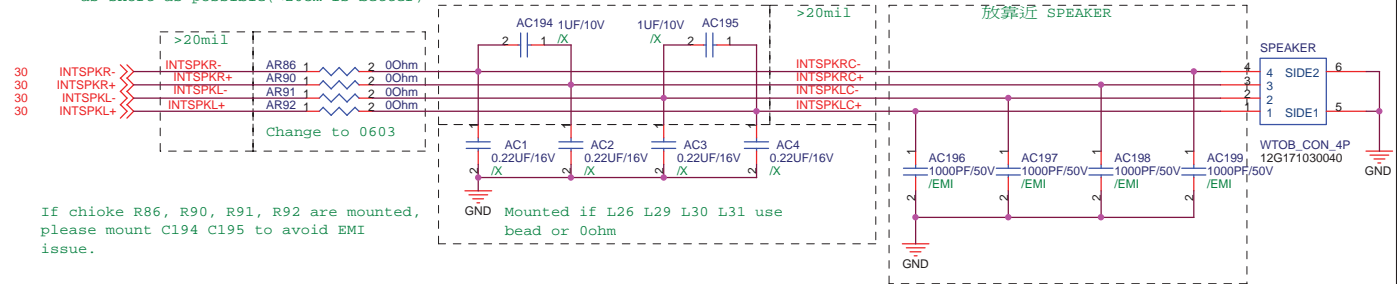
ASUS		Title : ALC269-1	
ASUSTek Computer Inc.		Engineer: Mick	
Size A3	Project Name S101	Rev 1.1G	
Date: Thursday, July 10, 2008	Sheet	30	of 50

1.1G add PWR LED and Charge LED

DMIC Cable length should be less 30cm

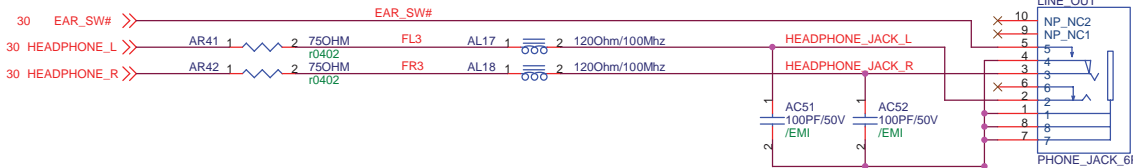


Total length from speakerR+- L+- (pin40 41 44 45) to internal speaker please as short as possible (<20cm is better)



If choke R86, R90, R91, R92 are mounted, please mount C194 C195 to avoid EMI issue.

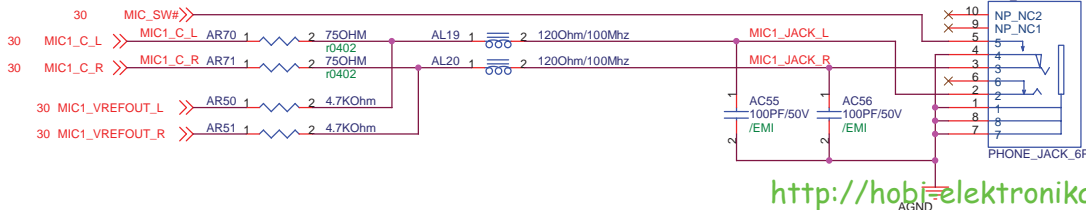
LINE_OUT use
12G14050106P(SINGATRON)
Black



1.1G Change audio con. to black
 change from DIP to SMD

R70 and R71: If don't need retasking function, change to 1K.

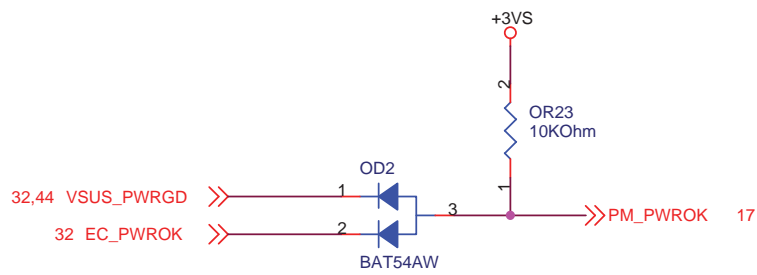
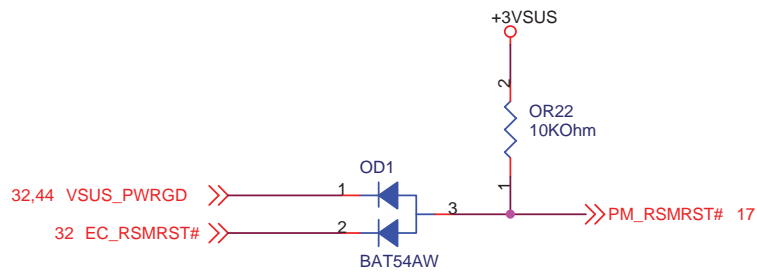
MIC JACK use
12G14050106P(SINGATRON)
Black



1.1G Change audio con. to black
 change from DIP to SMD


<http://hobbyelektronika.net>

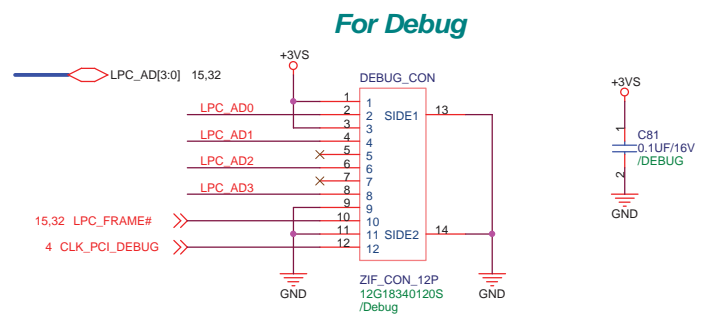
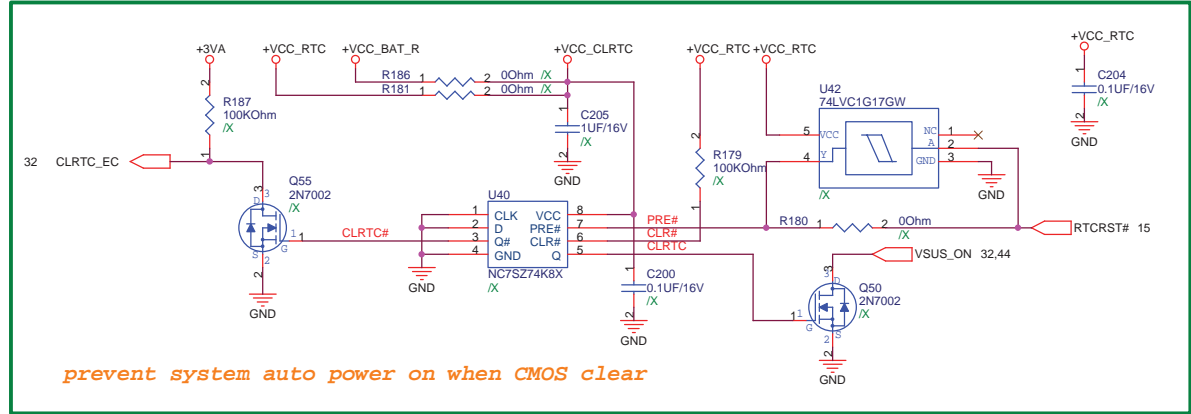
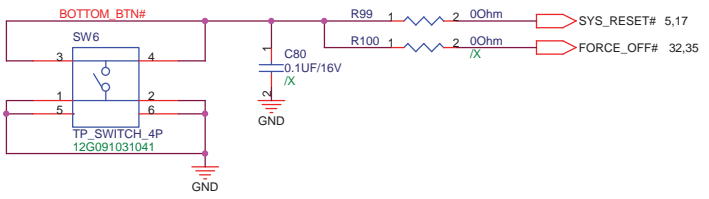
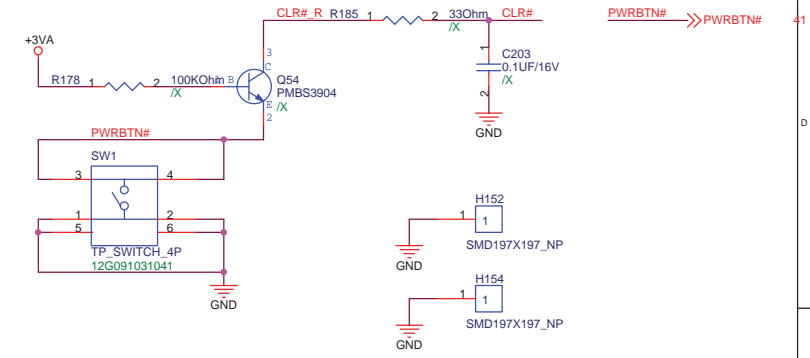
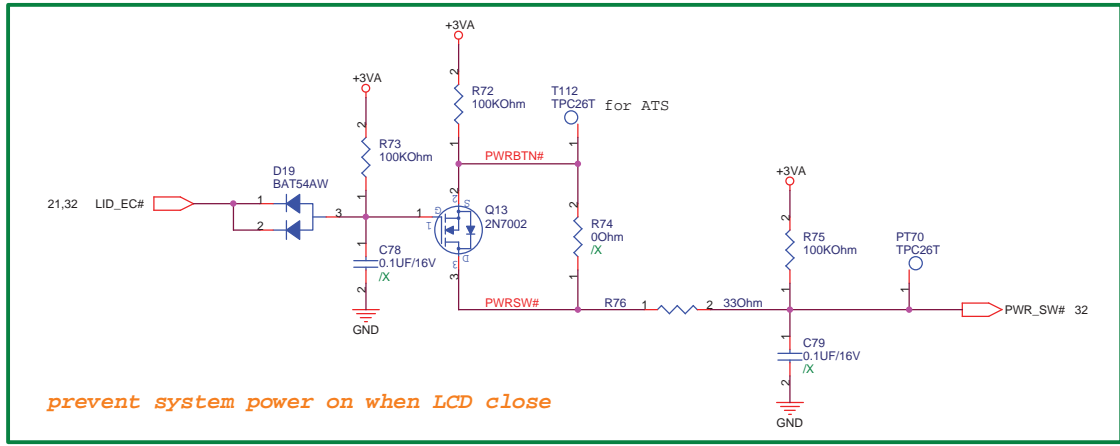
ASUS		Title : ALC269-2	
ASUSTek Computer Inc.		Engineer: MICK	
Size A3	Project Name S101	Rev 1.1G	
Date: Thursday, July 10, 2008	Sheet	31	of 50



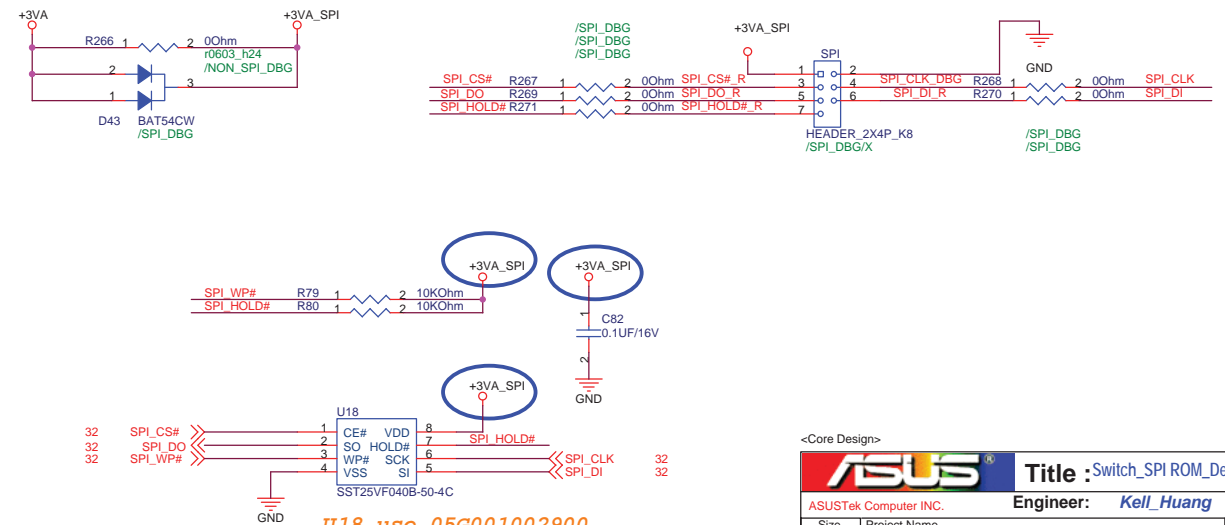
<http://hobi-elektronika.net>

<Core Design>

		Title : EC_UART_KC3820
ASUSTek Computer INC.		Engineer: Kell_Huang
Size A4	Project Name S101	Rev 1.1G
Date: Thursday, July 10, 2008	Sheet 33 of 50	

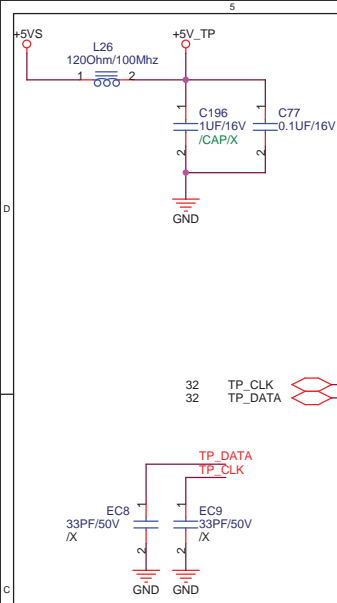


Debug Card cable use Z96 Touch Pad cable, P/N:
 14G124110126, 14G124110120, 14G124110121
 14G124110124, 14G124110125

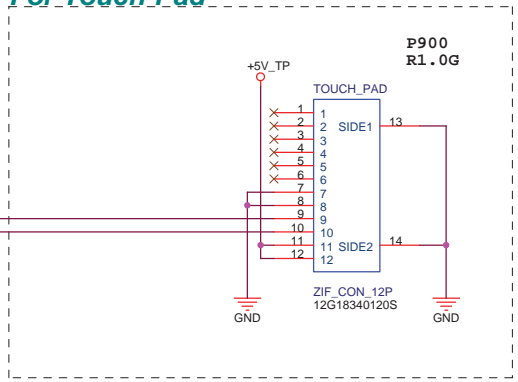


ASUS		Title : Switch_SPI ROM_Debug	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size	Project Name		Rev
A3	S101		1.1G
Date: Thursday, July 10, 2008	Sheet	34 of 50	

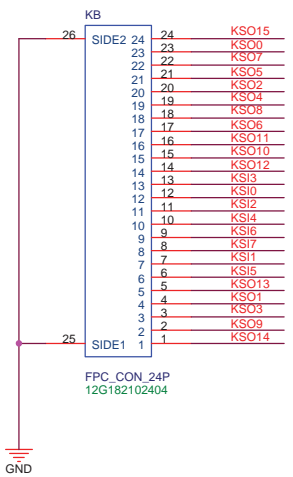
<http://hobi-elektronika.net>



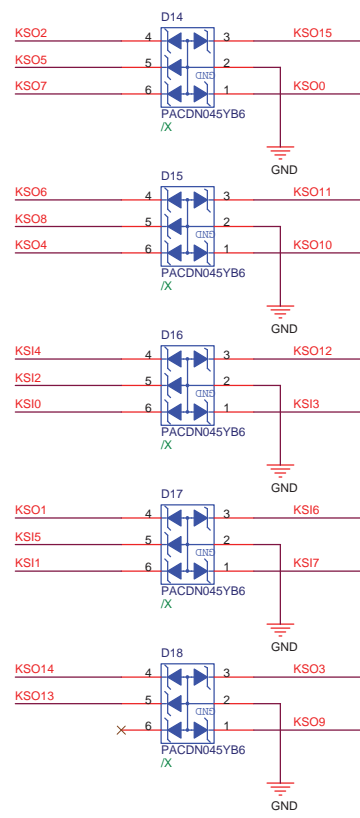
For Touch-Pad



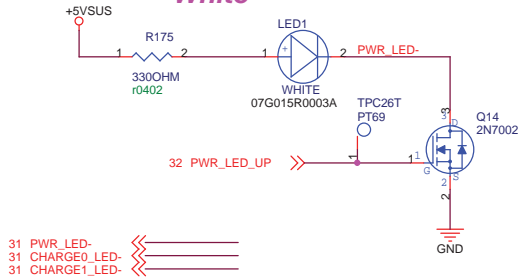
For Keyboard Connector



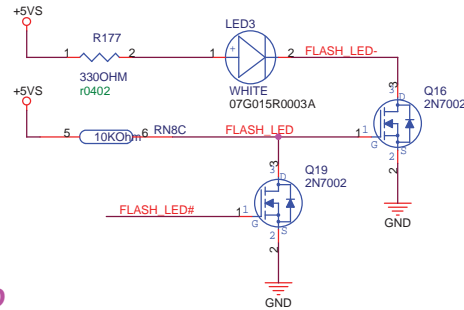
For assembly direction, KB pin1 to KB conn. pin24



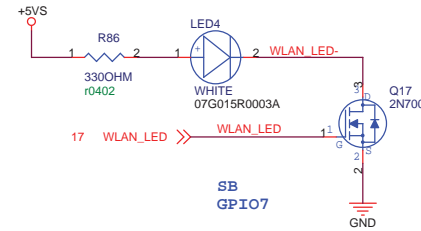
**for POWER LED
White**



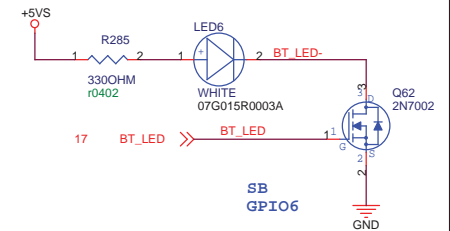
**for FLASH LED
White**



**for WLAN LED
White**



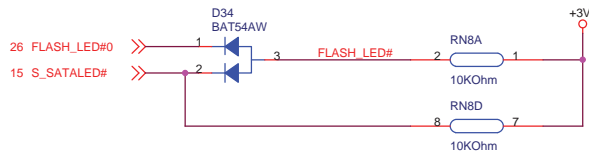
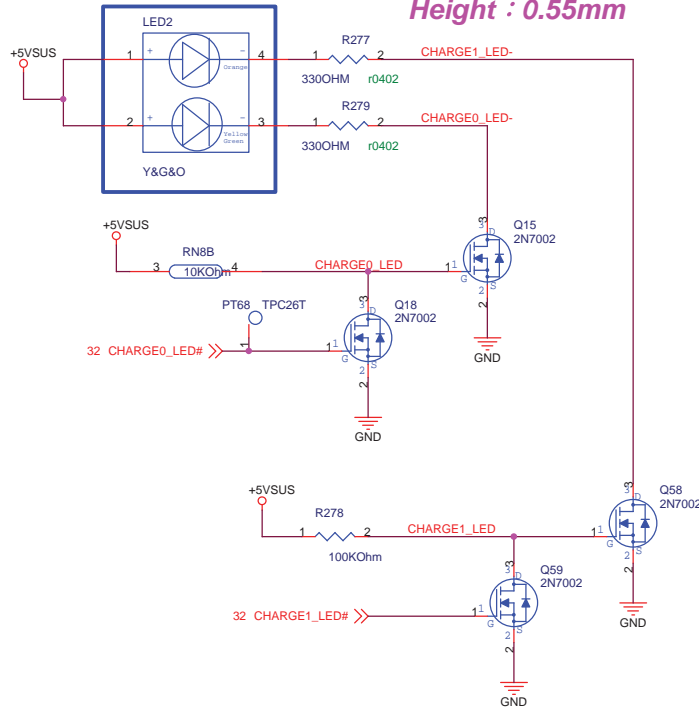
**for BlueTooth LED
White**



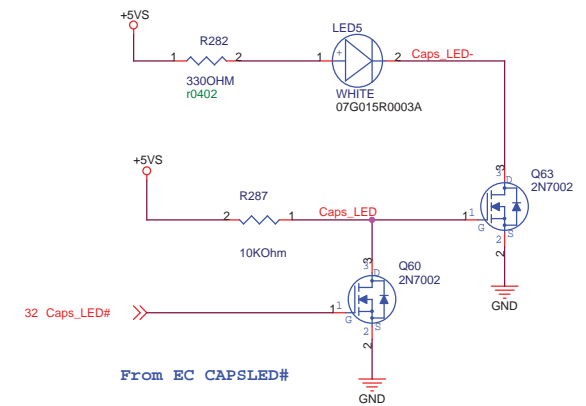
31 PWR_LED-
31 CHARGE0_LED-
31 CHARGE1_LED-

1.1G change to EVERLIGHT

**for CHARGE LED
Height : 0.55mm**



**for Caps Lock LED
White**



The battery charge indicator (LED) shows the status of the battery's power as follows:

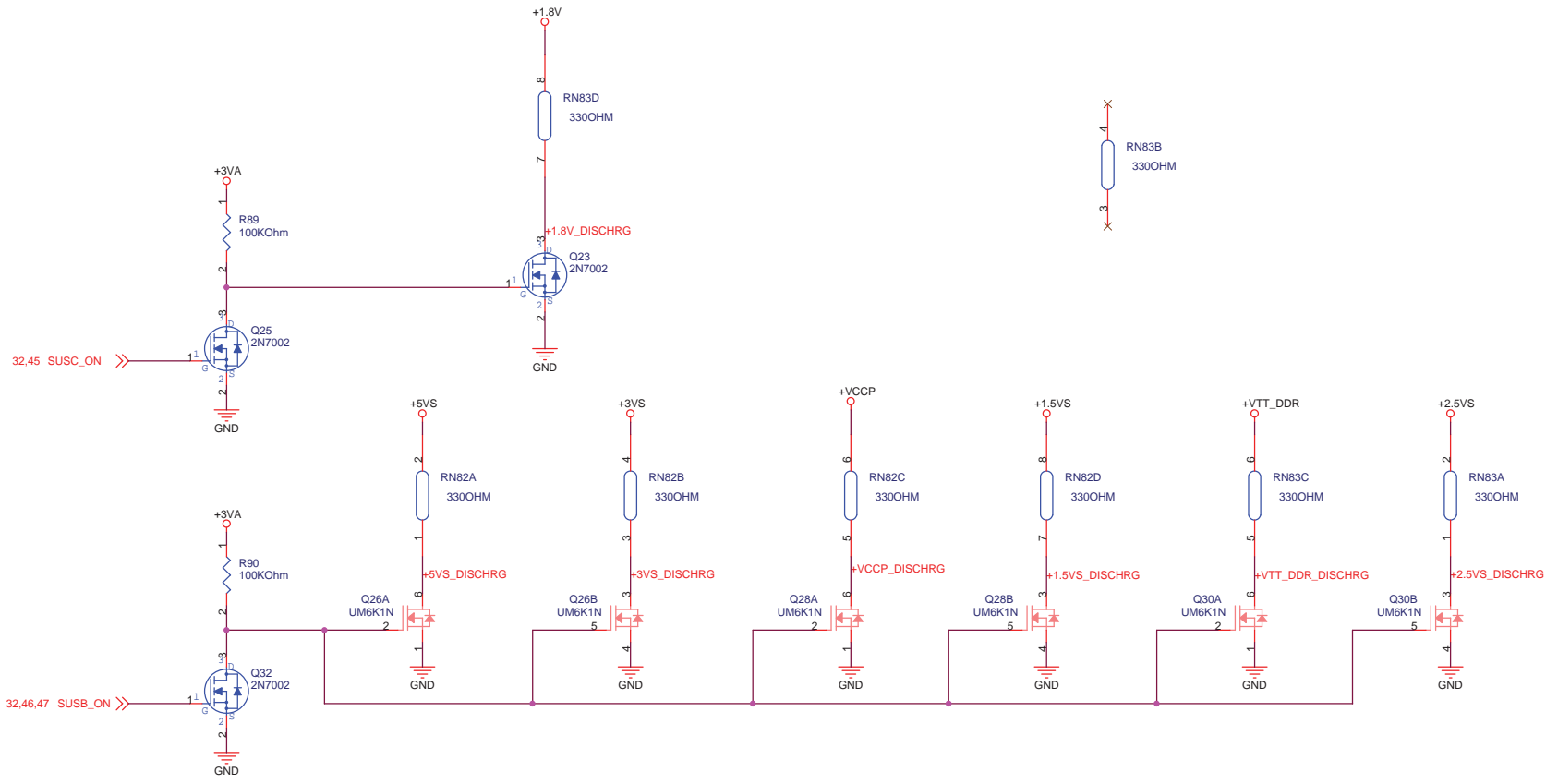
scenario	Adapter mode	Battery mode
Battery power is between 100%~80%	Orange ON	Green ON
Battery power is between 80%~10%	Orange Blinking Slowly	Green Blinking Slowly
Battery power is less than 10%	Orange Blinking Quickly	Green Blinking Quickly
S3/S5 Mode	Scenario the same as above	Off

Note: The BATTERY LED should be off when the machine has no battery attached.

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<Core Design>

ASUS		Title : LED	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size	Project Name	Rev	
A3	S101	1.1G	
Date: Thursday, July 10, 2008	Sheet	37	of 50

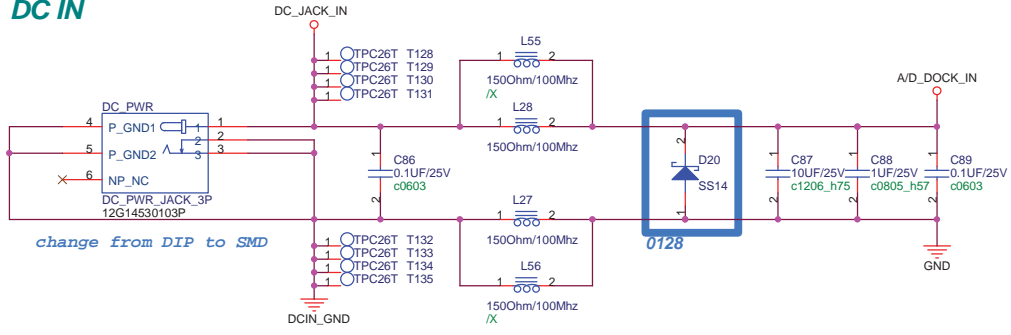


<http://hobi-elektronika.net>

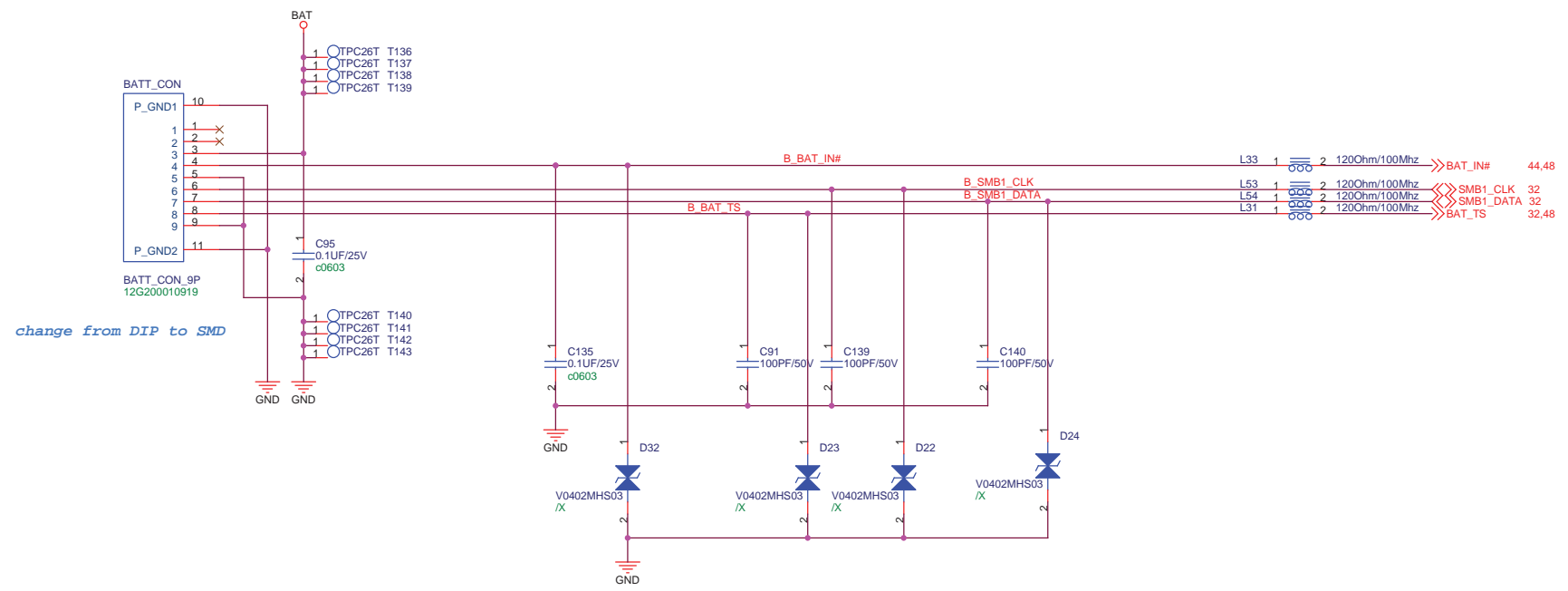
<Core Design>

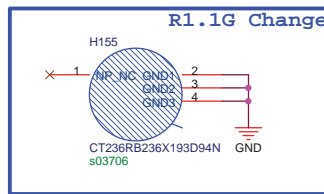
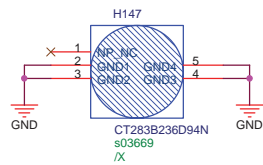
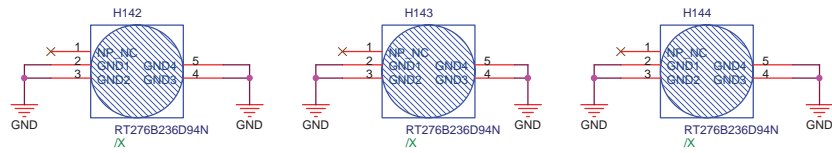
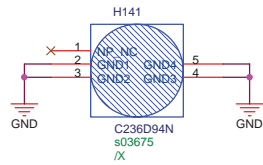
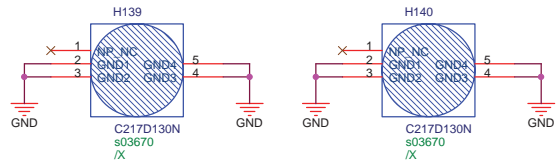
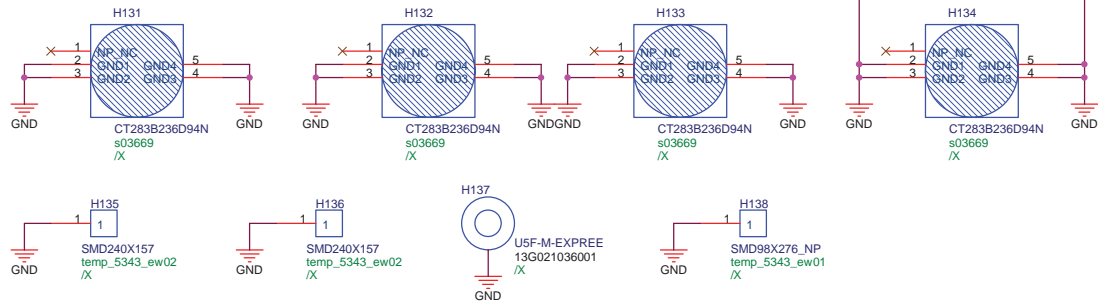
ASUS		Title : Discharge	
ASUSTek Computer INC.		Engineer: <i>Kell_Huang</i>	
Size	Project Name	Rev	
A3	S101	1.1G	
Date: Thursday, July 10, 2008		Sheet	38 of 50

DC IN



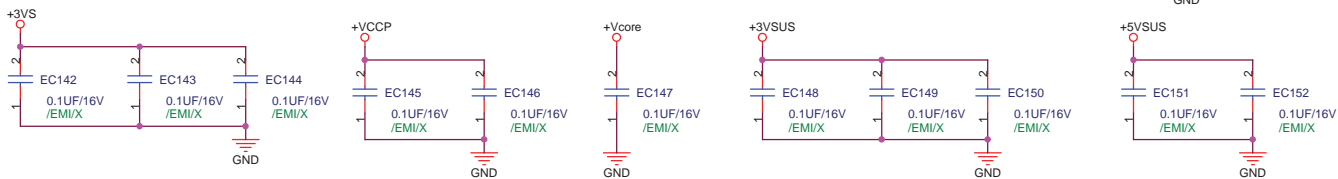
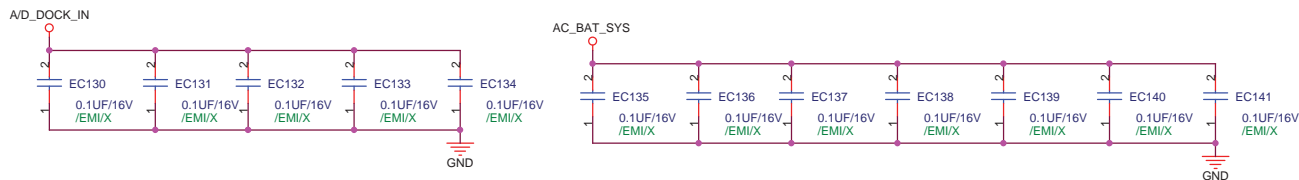
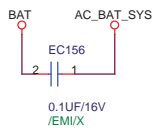
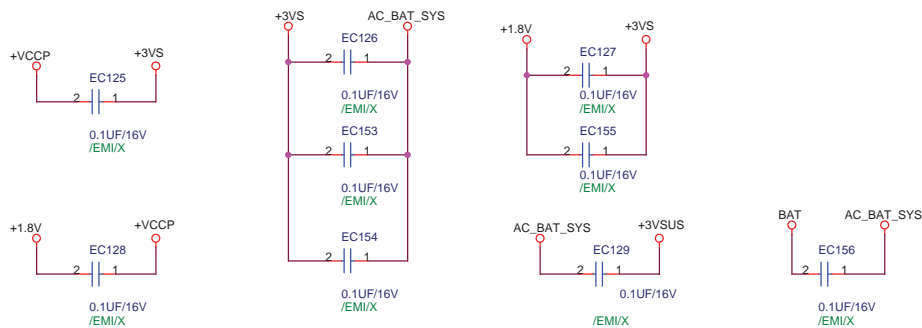
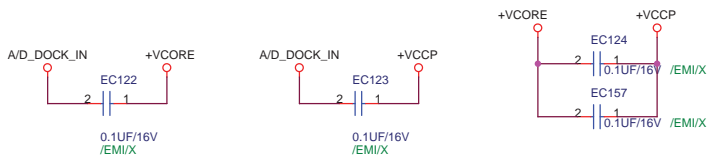
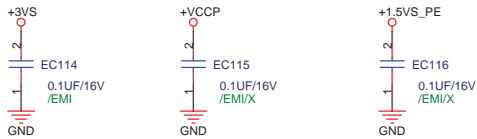
BAT IN





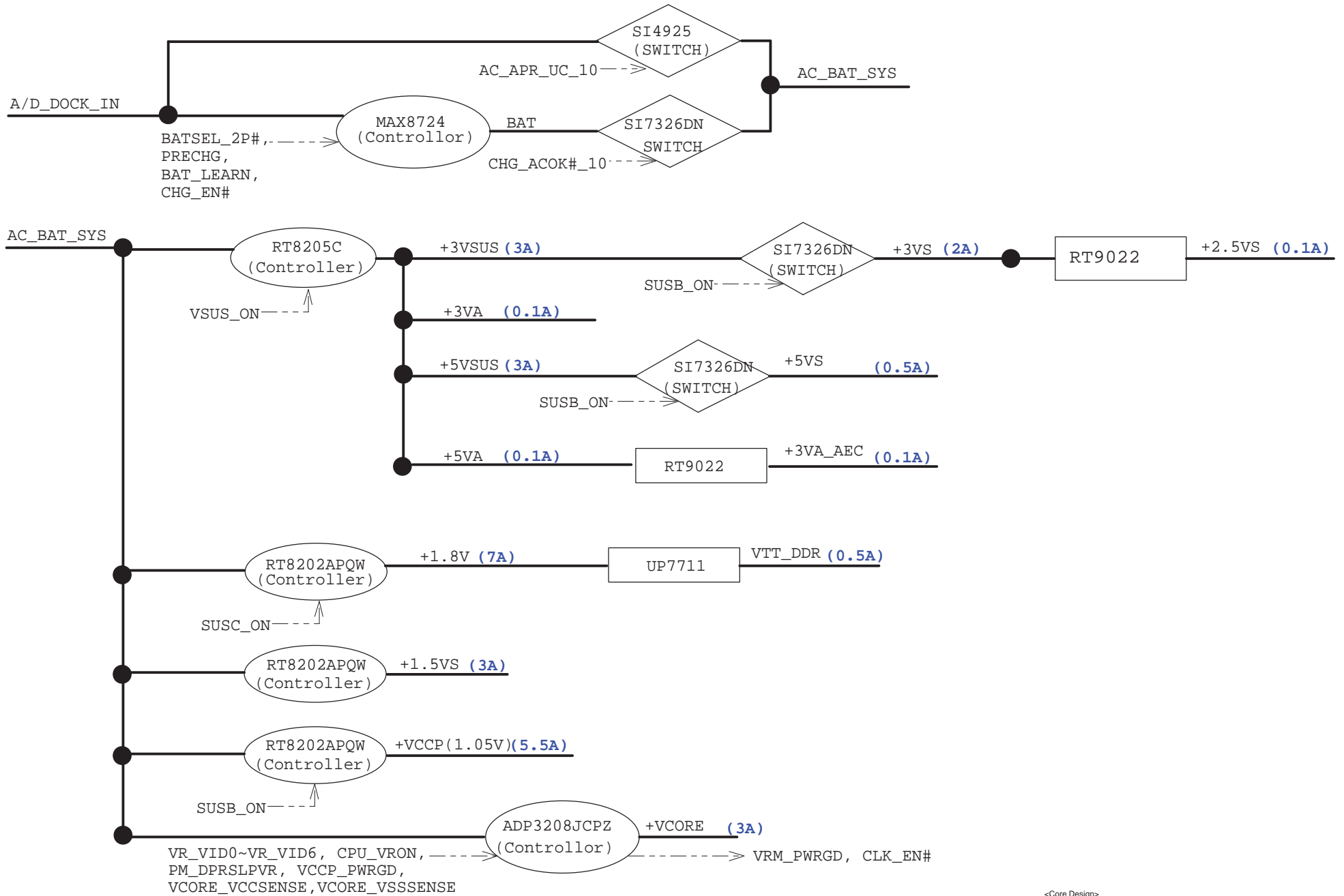
<Core Design>

ASUS		Title : Srew Hole	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size	Project Name	Rev	
A3	S101	1.1G	
Date: Thursday, July 10, 2008	Sheet	40	of 50



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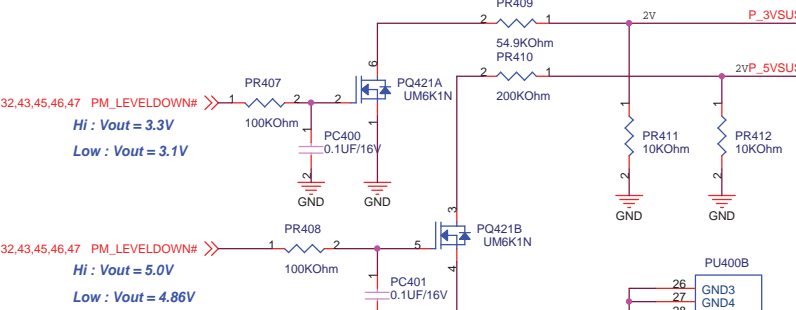
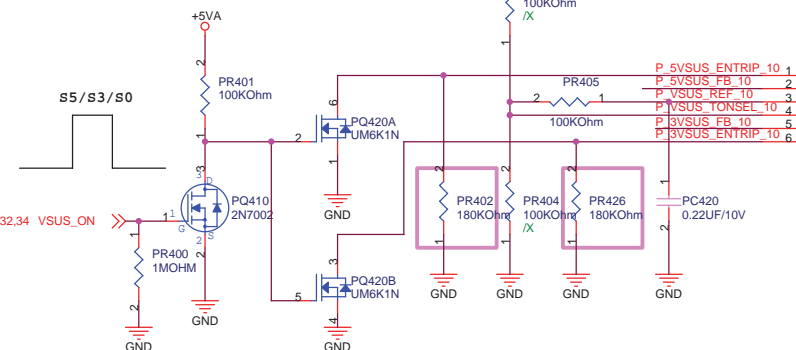
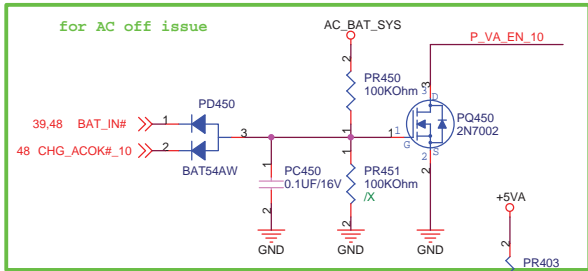
<Core Design>		ASUS		Title : EMI	
ASUSTek Computer INC.		Engineer: <i>Kell_Huang</i>			
Size	Project Name	Rev			
A3	S101	1.1G			
Date: Thursday, July 10, 2008	Sheet	41	of	50	



<http://hobi-elektronika.net>

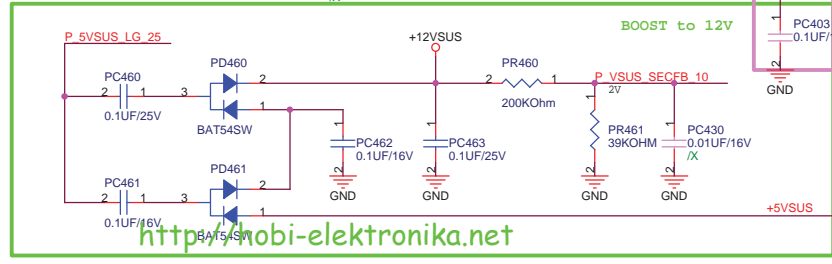
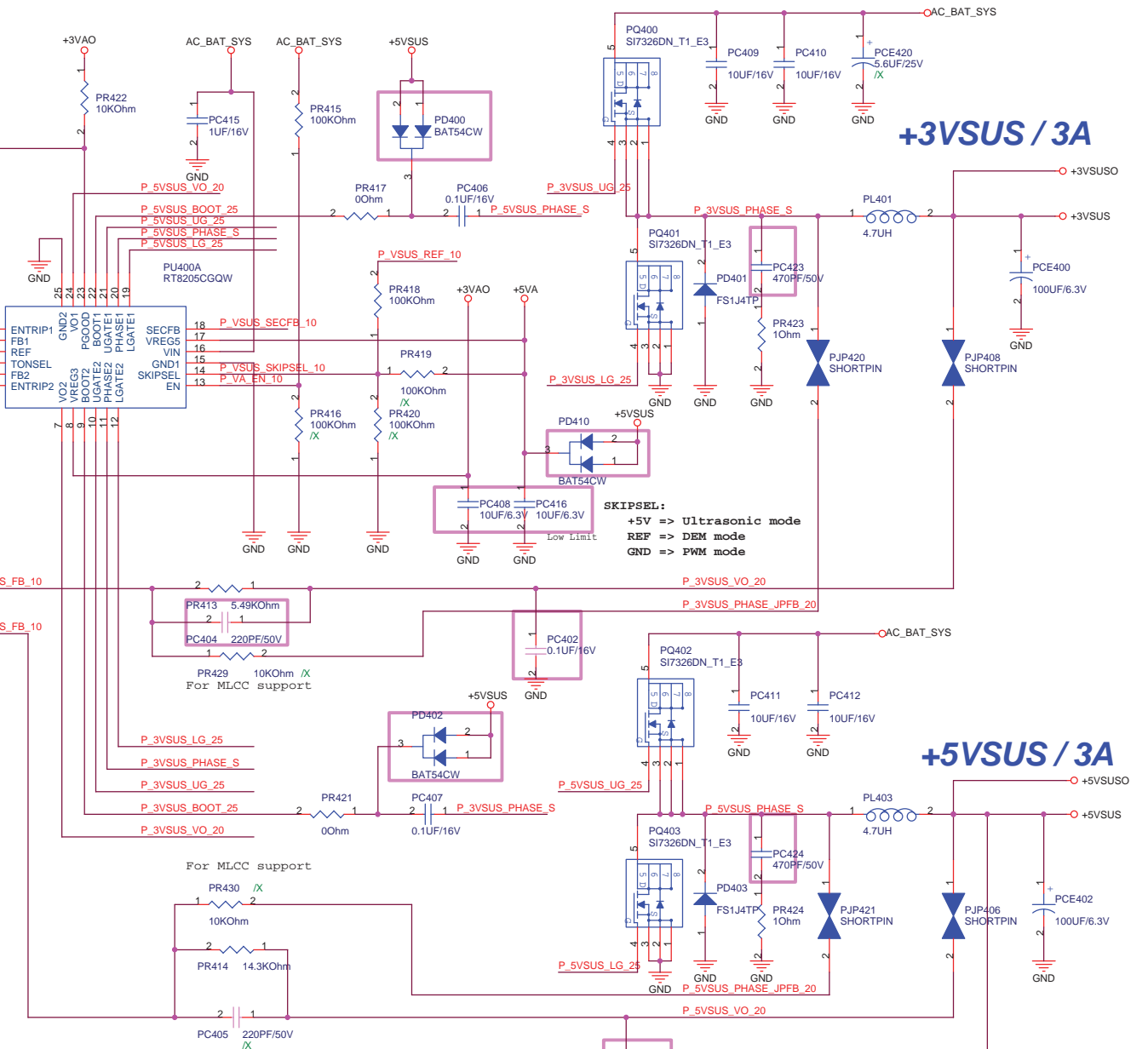
<Core Design>

ASUS		Title : Power Flow	
ASUSTek Computer INC.		Engineer: <i>Joy_Zhou</i>	
Size	Project Name	Rev	
A3	S101	1.1G	
Date: Thursday, July 10, 2008	Sheet	42	of 50



ENTRIP:
 GND => Disable
 OCF => $(10\mu A \times R) / 10 / R_{dson}$

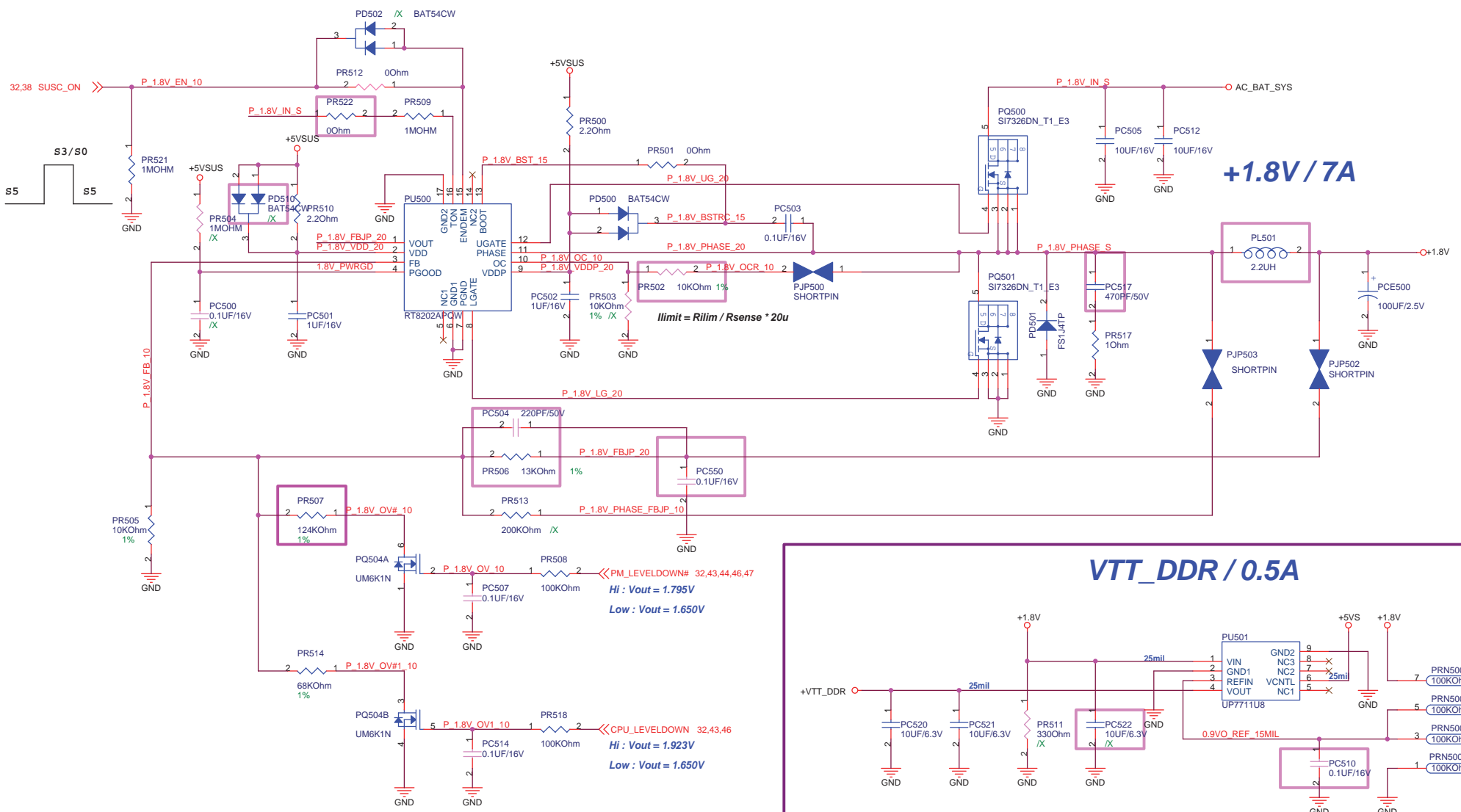
TONSEL:
 +5V => 400KHz / 500KHz
 REF => 300KHz / 375KHz
 GND => 200KHz / 250KHz



<Core Design>

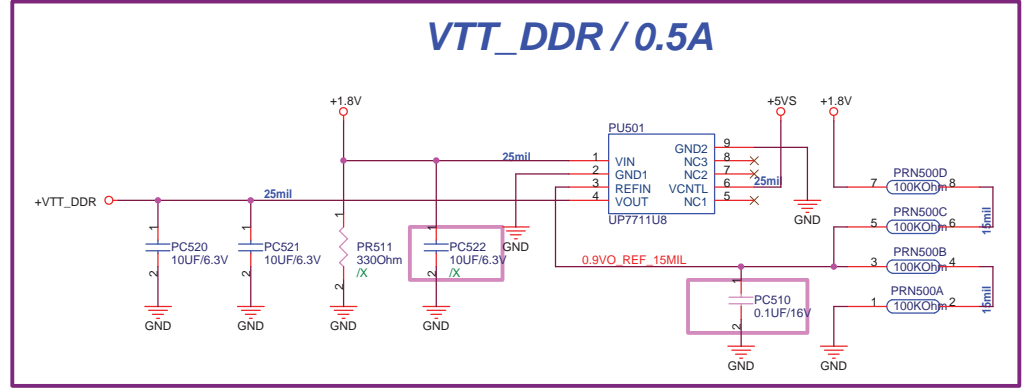
ASUS		Title: +3VSUS & +5VSUS & +3VA	
ASUSTek COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
A3	1001	1.1G	
Date: Thursday, July 10, 2008	Sheet 44 of 50		

<http://nobi-elektronika.net>

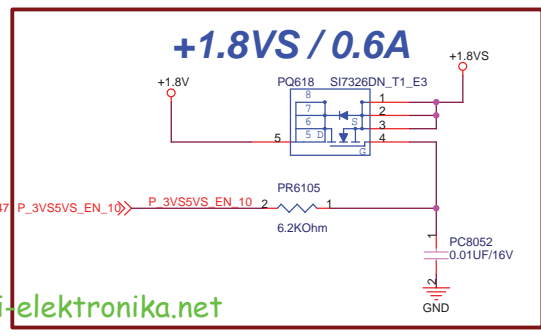


+1.8V / 7A

VTT_DDR / 0.5A



+1.8VS / 0.6A



PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	1.72V	Power Saving
H	L	H	1.795V	Normal
H	H	L	1.927V	Performance
L	H	L	1.782V	N/A

<http://hobi-elektronika.net>

<Core Design>

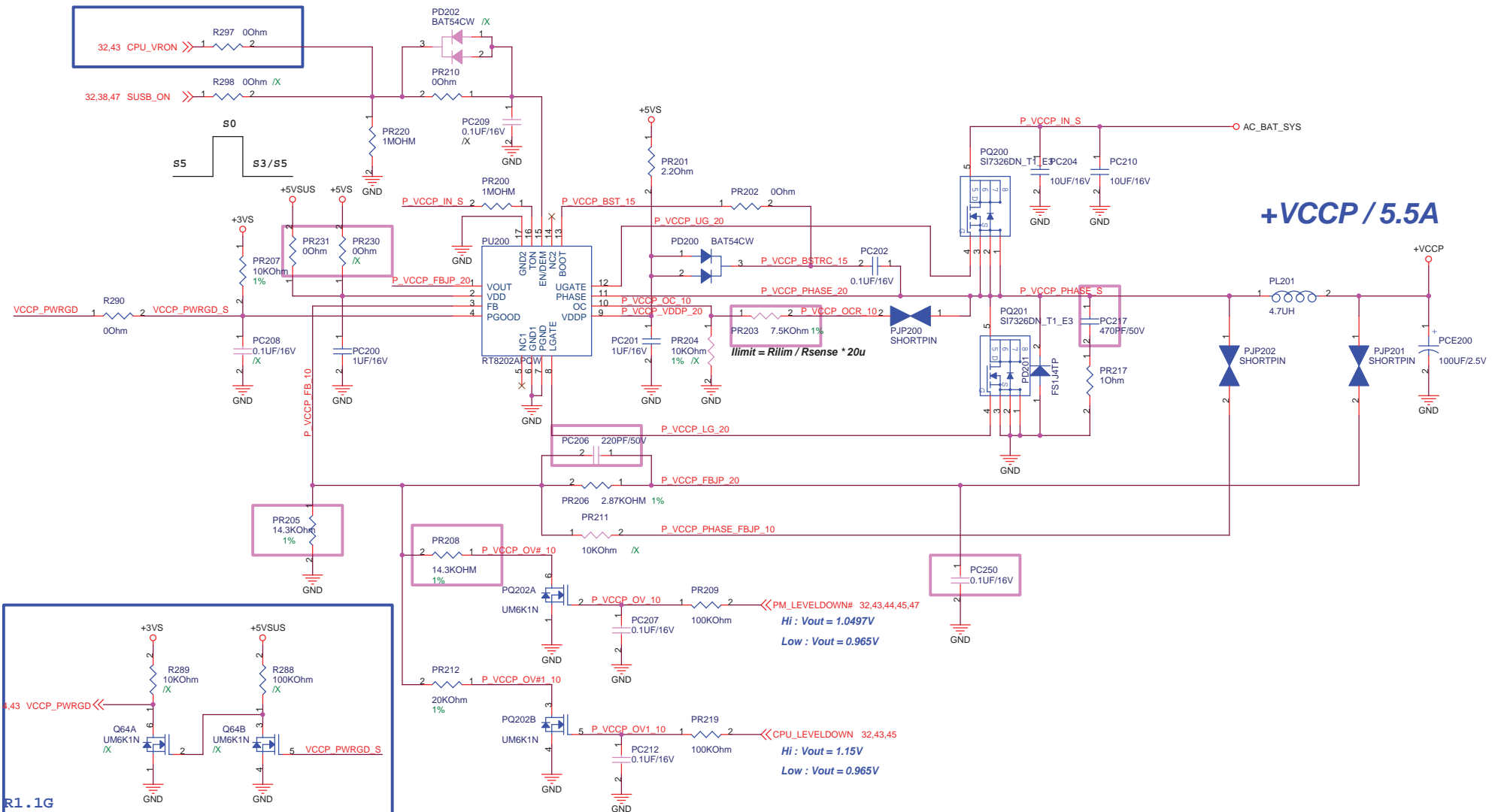
Title : +1.8V & VTTDDR

ASUSTek Computer INC. **Engineer: Joy_Zhou**

Size	Project Name	Rev
A3	1001	1.1G

Date: Thursday, July 10, 2008 Sheet 45 of 50

1.1G change Enable signal from CPU_VRON



+VCCP / 5.5A

To remove VCCP_PWRGD glitch

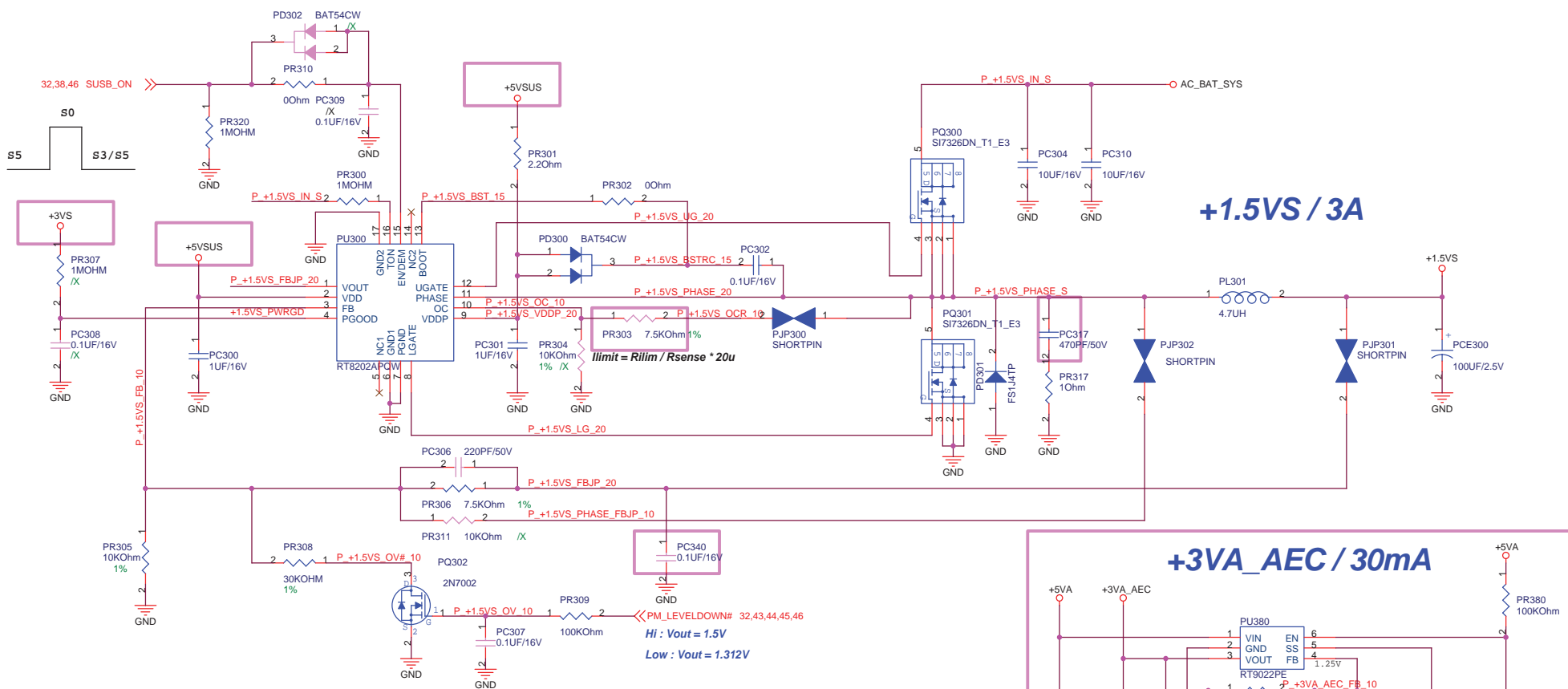
PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	0.965V	Power Saving
H	L	H	1.048V	Normal
H	H	L	1.157V	Performance
L	H	L	1.072V	N/A

<http://hobi-elektronika.net>

<Core Design>

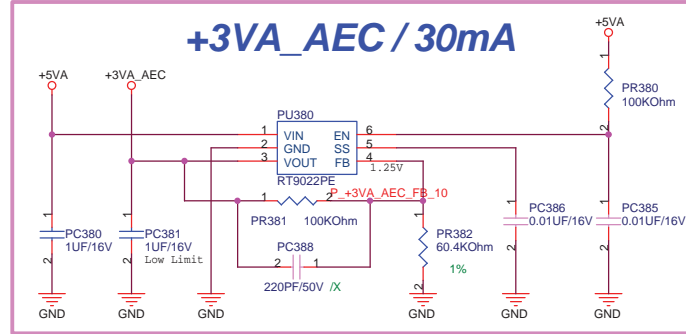
Title : VCCP
 ASUSTek Computer INC. **Engineer: Joy_Zhou**

Size A3	Project Name 1001	Rev 1.1G
Date: Thursday, July 10, 2008		Sheet 46 of 50

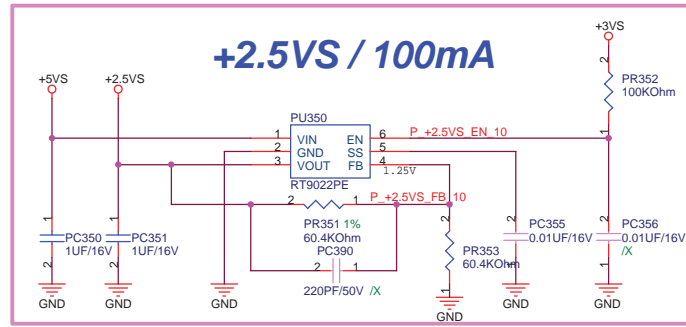


+1.5VS / 3A

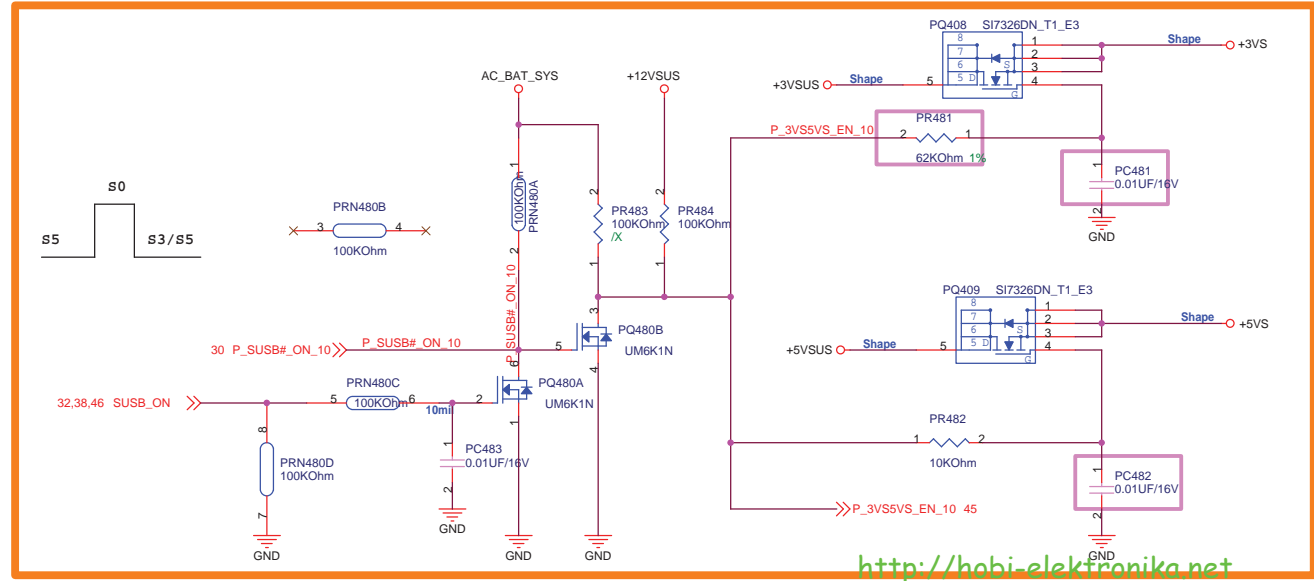
Hi : Vout = 1.5V
Low : Vout = 1.312V



+3VA_AEC / 30mA



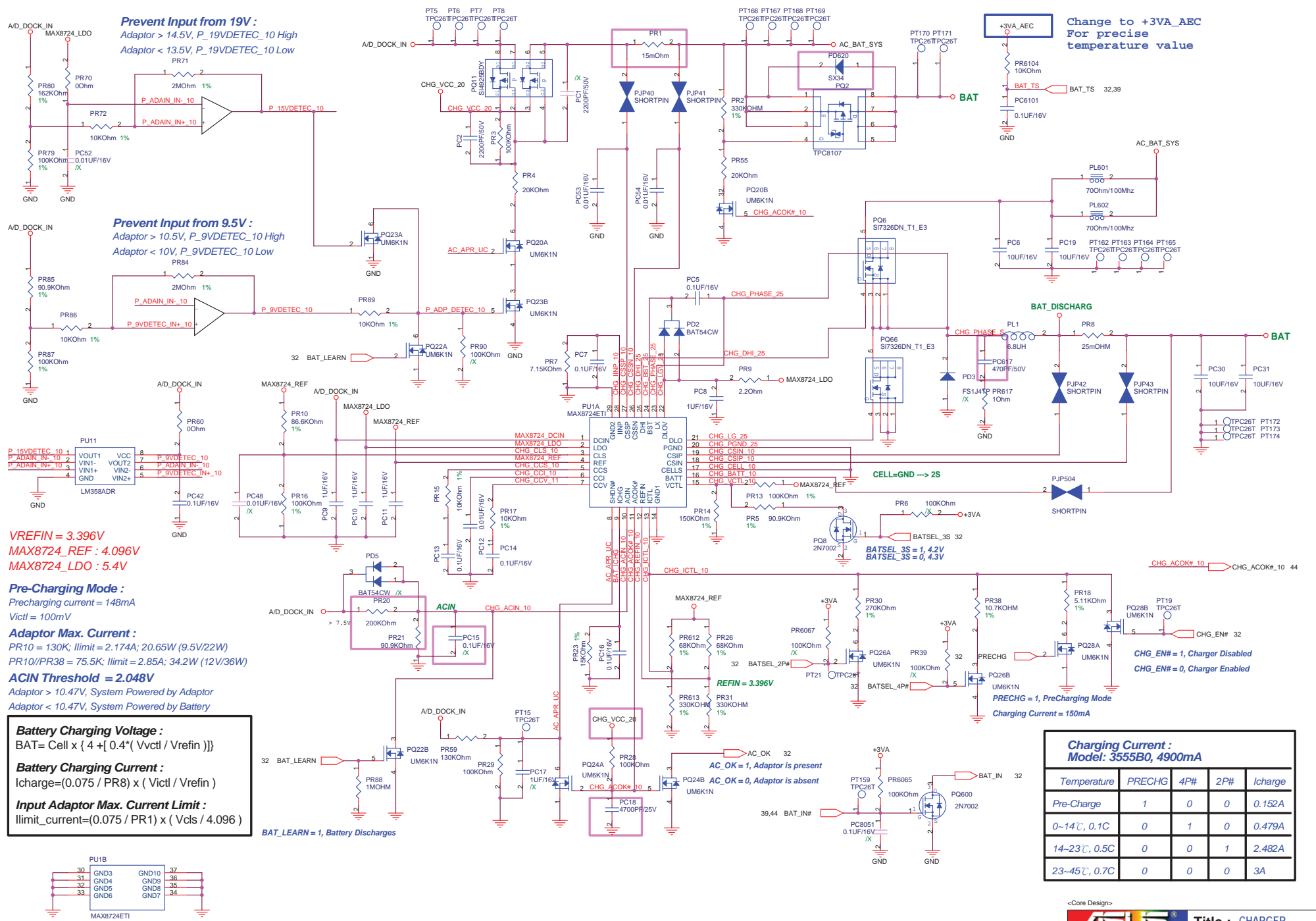
+2.5VS / 100mA



<http://hobi-elektronika.net>

<Core Design>

ASUS		Title : +1.5VS & +2.5VS	
ASUSTek Computer INC.		Engineer: Joy Zhou	
Size	A3	Project Name	1001
Date:	Thursday, July 10, 2008	Sheet	47 of 50
		Rev	1.1G



Prevent Input from 19V :
 Adaptor > 14.5V, P_19VDETEC_10 High
 Adaptor < 13.5V, P_19VDETEC_10 Low

Prevent Input from 9.5V :
 Adaptor > 10.5V, P_9VDETEC_10 High
 Adaptor < 10V, P_9VDETEC_10 Low

Change to +3VA_AEC
 For precise temperature value

VREFIN = 3.396V
 MAX8724_REF = 4.096V
 MAX8724_LDO = 5.4V

Pre-Charging Mode :
 Precharging current = 148mA
 V_{ictl} = 100mV
Adaptor Max. Current :
 PR10 = 130K; I_{limit} = 2.174A; 20.65W (9.5V/22W)
 PR10/PR38 = 75.5K; I_{limit} = 2.85A; 34.2W (12V/36W)
ACIN Threshold = 2.048V
 Adaptor > 10.47V, System Powered by Adaptor
 Adaptor < 10.47V, System Powered by Battery

Battery Charging Voltage :
 BAT = Cell x { 4 + [0.4 * (V_{vctl} / V_{refin})] }
Battery Charging Current :
 I_{charge} = (0.075 / PR8) x (V_{victl} / V_{refin})
Input Adaptor Max. Current Limit :
 I_{limit} = (0.075 / PR1) x (V_{vcls} / 4.096)

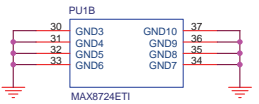
BAT_LEARN = 1, Battery Discharges

AC_OK = 1, Adaptor is present
 AC_OK = 0, Adaptor is absent

PRECHG = 1, PreCharging Mode
 Charging Current = 150mA

Charging Current :
 Model: 3555B0, 4900mA

Temperature	PRECHG	4P#	2P#	I _{charge}
Pre-Charge	1	0	0	0.152A
0-14°C, 0.1C	0	1	0	0.479A
14-23°C, 0.5C	0	0	1	2.482A
23-45°C, 0.7C	0	0	0	3A



EC KB3310 GPIO SETTING

Pin	Pin Name	Signal Name	Type	Note
1	GPIO0/GA20	A20GATE	O	
2	GPIO01/KBRST#	RC_IN#	O	
6	GPIO4	HOTKEY_SW0#	I	Internal pull high
13	GPIO05/PCIRST#	PCI_RST#	I	
14	GPIO07	HOTKEY_SW1#	I	Internal Pull Up
15	GPIO08	EXTSMH#	OD	10K ohm Pull Up to +3VSU
16	GPIO0A	LID_EC#	I	Internal pull high
17	GPIO0B/ESB_CLK	NC	O	
18	GPIO0C/ESB_DAT	NC	O	
19	GPIO0D	HOTKEY_SW2#	I	Internal pull high
20	GPIO0E/SC#	KBC_SC#	OD	10K ohm Pull Up to +3VSUS
21	GPIO0F/PWM0	BL_PWM_DA	O	
23	GPIO10/PWM1	BATSEL_4P#	O	Battery charging current setting
25	GPIO11/PWM2	PM_PWRBTN#	OD	Internal pull high in ICH
26	GPIO12/FANPWM1	FAN0_PWM	O	CPU Fan
27	GPIO13/FANPWM2	FAN1_PWM	O	VGA Fan
28	GPIO14/FANFB1	FAN0_TACH	I	CPU FanTach
29	GPIO15/FANFB2	FAN1_TACH	I	VGA FanTach
30	GPIO16/E51_TX	E51_TX	O	RS232 debug port
31	GPIO17/E51_RX	E51_RX	O	RS232 debug port
32	GPIO18	PWR_SW#	I	Internal pull high
34	GPIO19/PWM3	MAIL_LED#	O	
36	GPIO1A/NUMLED	NUM_LED#	O	
38	GPIO1D/CLKRUN#	NC	O	
39	GPIO20/KSO0/TP_TEST	KSO0	O	
40	GPIO21/KSO1/TP_PLL	KSO1	O	
41	GPIO22/KSO2	KSO2	O	
42	GPIO23/KSO3	KSO3	O	
43	GPIO24/KSO4	KSO4	O	
44	GPIO25/KSO5	KSO5	O	
45	GPIO26/KSO6	KSO6	O	
46	GPIO27/KSO7	KSO7	O	
47	GPIO28/KSO8	KSO8	O	
48	GPIO29/KSO9	KSO9	O	
49	GPIO2A/KSO10	KSO10	O	
50	GPIO2B/KSO11	KSO11	O	
51	GPIO2C/KSO12	KSO12	O	
52	GPIO2D/KSO13	KSO13	O	
53	GPIO2E/KSO14	KSO14	O	
54	GPIO2F/KSO15	KSO15	O	
55	GPIO30/KSI0	KSI0	I	Internal pull high
56	GPIO31/KSI1	KSI1	I	Internal pull high
57	GPIO32/KSI2	KSI2	I	Internal pull high
58	GPIO33/KSI3	KSI3	I	Internal pull high
59	GPIO34/KSI4	KSI4	I	Internal pull high
60	GPIO35/KSI5	KSI5	I	Internal pull high
61	GPIO36/KSI6	KSI6	I	Internal pull high
62	GPIO37/KSI7	KSI7	I	Internal pull high
63	GPI38/AD0	BAT_ICHG	I	
64	GPI39/AD1	BAT_CONFIG	I	Battery configuration
65	GPIO3A/AD2	BAT_SENSE	I	Battery Voltage Sensor
66	GPIO3B/AD3	BAT_TS	I	Battery Thermal Sensor
68	GPO3C/DA0	DOC	O	Trigger Clock Gen

Pin	Pin Name	Signal Name	Type	Note
70	GPO3D/DA1	LCD_BACKOFF#	O	
71	GPO3E/DA2	CLK_PWRSERVE#	O	
72	GPO3F/DA3	BAT_LL#	O	Battery Low Low
73	GPIO40	AC_OK	I	AC Adaptor Plug in
74	GPIO41	PM_RSMRST#	O	10K pull down to GND
75	GPI42	BAT_IN	I	
76	GPI43	CLRTC_EC	I	
77	GPIO44/SCL1	SMB0_CLK	I/O	4.7K pull high to +3VA_EC
78	GPIO45/SDA1	SMB0_DAT	I/O	4.7K pull high to +3VA_EC
79	GPIO46/SCL2	SMB1_CLK	I/O	10K pull high to +3V
80	GPIO47/SDA2	SMB1_DAT	I/O	10K pull high to +3V
81	GPIO48/KSO16	KB pin 28	I	for KB type detection
82	GPIO49/KSO17	KB pin 27	I	for KB type detection
83	GPIO4A/PSCLK1	AUO_SCL	O	for AUO, default H at S0
84	GPIO4B/PSDAT1	AUO_SDA	O	for AUO, default L at S0
85	GPIO4C/PSCLK2	AUO_CSB	O	for AUO, default H at S0
86	GPIO4D/PSDAT2	LVDD_EN	I	for AUO 7" Panel
87	GPIO4E/PSCLK3	TP_CLK	I/O	10K pull high to +3V
88	GPIO4F/PSDAT3	TP_DAT	I/O	10K pull high to +3V
89	GPIO50/SELIO#	BATSEL_3S	O	Battery series, H:3S, L:4S
90	GPIO52/E51_CS#	CHG_LED_UP#	O	
91	GPIO53/CAPLED	CAP_LED#	O	
92	GPIO54	PWR_LED_UP	O	
93	GPIO55/SCRLED	SCR_LED#	O	
95	GPIO56	PWR4G_SW#	I	Internal pull high
97	GPXOA00/SDICS#	SPI_MODE#	O	4.7K pull down to GND
98	GPXOA01/SDICLK	SUSC_ON	O	
99	GPXOA02/SDIDO	VSUS_ON	O	
100	GPXOA03	CPU_VRON	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	ICH_PWROK	O	
103	GPXOA06	VOLT_CTRL	O	
104	GPXOA07	CHG_EN#	O	Battery charging enabled
105	GPXOA08	PRECHG	O	
106	GPXOA09	SPI_WP#	O	
107	GPXOA10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	
109	GPXID0/SDIDI	BATSEL_2P#	O	Battery parallel, H:1P, L:2P~3P
110	GPXID1	NC	O	
112	GPXID2	THRO_CPU	O	Active if CPU temperature over spec
114	GPXID3	SUSB#	I	100K pull down to GND
115	GPXID4	SUSC#	I	100K pull down to GND
116	GPXID5	CPUPWR_GD	I	Pull high to +3V
117	GPXID6	VSUS_GD	I	
118	GPXID7	NC	O	
121	GPIO57	INTERNET#	I	Internal pull high
126	GPIO57/SPICLK	SPI_CLK	O	
127	GPIO59/TEST_CLK	NC	O	

EC KB3310 Other Pin SETTING

Pin	Pin Name	Signal Name	Type	Note
3	SERIRQ	INT_SERIRQ	I/O	10K pull high to +3V
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA_EC	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCI_EC	I	
22	VCC	+3VA_EC	P	
24	GND	GND	P	
33	VCC	+3VA_EC	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	100K pull high to +3VA_EC
67	AVCC	+3VACC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA_EC	P	
111	VCC	+3VA_EC	P	
113	GND	GND	P	
119	RD#/SPIDI	SPL_SO	I	
120	WR#/SPIDO	SPL_SI	O	
112	XCLKI	32KXCLKI	I	
123	XCLKO	32KXCLKO	O	
124	V18R	V18R	P	Reserved 1uF to GND
125	VCC	+3VA_EC	P	
128	SPICS#/SELMEM#	SPI_CE#	O	

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		Title : History	
ASUSTek Computer INC.		Engineer: <i>Satan He</i>	
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